AN3743

VSC74xx/VSC84xx SerDes Macro

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1.0 INTRODUCTION

In the past, most VSC switches and 10G PHYs have been using the 65 nm SerDes macros and 5G PLLs developed by the German Design Center. This application note describes many of the SerDes macros features.

Supported VSC switches are the following:

- VSC7410
- VSC7414
- VSC7415
- VSC7416
- VSC7418
- VSC7420
- VSC7421
- VSC7422
- VSC7423
- VSC7424
- VSC7425
- VSC7426
- VSC7427
- VSC7428
- VSC7429
- VSC7430
- VSC7431
- VSC7432
- VSC7434
- VSC7435
- VSC7436
- VSC7437
- VSC7438
- VSC7440
- VSC7442
- VSC7444
- VSC7448
- VSC7449
- VSC7460
- VSC7462
- VSC7464
- VSC7468
- VSC7511
- VSC7512
- VSC7513
- VSC7514
- VSC8484
- VSC8486
- VSC8487
- VSC8488
- VSC8489
- VSC8490
- VSC8491

1.1 Sections

This document includes the following topics:

1.2 Terms and Abbreviations

Table 1-1 lists special terms and abbreviations used in this document.

TABLE 1-1: TERMS AND ABBREVIATIONS

Term	Description	Term	Description
APC	Automatic Parameter Control	OB	Output Buffer
BIST	Build-In Self Test	PCS	Physical Coding Sublayer
CDR	Clock and Data Recovery	PLL	Phase Locked Loop
DES	Deserializer	SER	Serializer
DFE	Decision Feedback Equalization	SerDes	Serializer-Deserializer Macro
DFT	Design For Test	SGMII	Serial Gigabit Media Independent Interface
EEE	Energy Efficient Ethernet (Green Ethernet) according to IEEE802.3az	SPI	Serial Peripheral Interface
IB	Input Buffer	SSC	Spread Spectrum Clocking
KR	Shortcut for 10GBASE-KR according to IEEE802.3 Clause 72	TCE	Time Continuous Equalization
MLD	Multi-Lane Distribution	XAUI	10 Gigabit Attachment Unit Interface

2.0 VSC 65 NANOMETER SERDES MACRO

This section gives an overview of and how to access the VSC 65 nm SerDes macros.

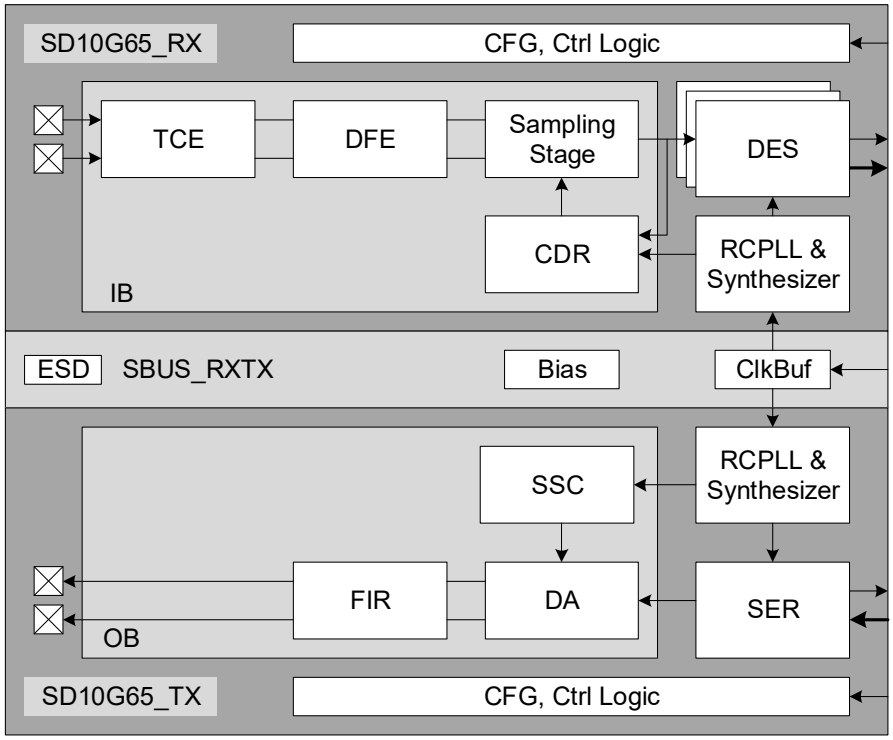
2.1 SerDes Macro Types

There are three types of VSC SerDes macros: 1G, 6G, and 10G. Each type name indicates maximum frequency and becomes more complex and feature-rich with the higher frequency.

2.2 Block Diagram

Figure 2-1 shows the typical blocks inside a VSC SerDes macro.

FIGURE 2-1: TYPICAL SERDES BLOCK DIAGRAM



2.3 Accessing the Control and Status Registers

Because of the number of 1G and 6G SerDes macros instantiated into the VSC switches, these macros are configured using a configuration bus (MCB). This is a serial bus connecting a set of 'shadow' configuration and status registers to all the SerDes macros. See Appendix A: "SerDes Shadow Registers" for description.

The configuration bus is used for both reading from and writing to the macros. A mask register is used to point out the specific macro to access. With this approach, it is possible to write to multiple macros in one step, if the setup is the same for all. This is done by setting more bits in the MCB mask field. Reading is only possible with one macro at the time.

MCB_SERDES1G_ADDR_CFG register is used for the 1G SerDes macros, and MCB_SERDES6G_ADDR_CFG register is used for the 6G SerDes macros.

When debugging and changing any bit in a specific SerDes register, it is required to read out all macro registers first to the shadow registers. Modify the setting in the shadow register, and then write back all shadow registers to the SerDes macro registers.

There is no Macro Control Bus (MCB) configuration bus for the 10G SerDes macros because of lower 10G port count. Hence, the access to the configuration and status registers are made directly.

3.0 LOOPBACK

3.1 1G and 6G SerDes Loopback

The 1G and 6G SerDes macros support different loopback modes for testing and debugging the data paths:

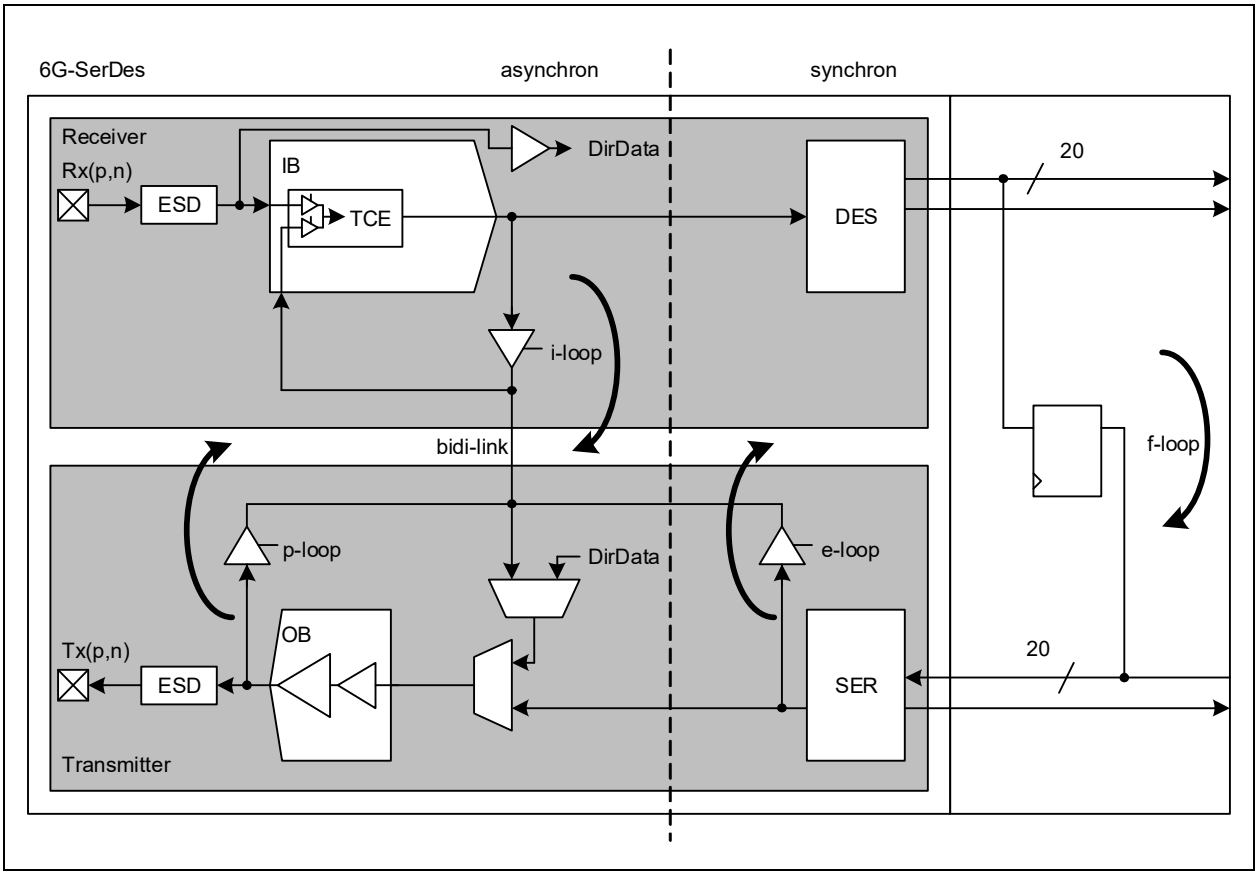
- Equipment Loopback Mode
- Facility Loopback Mode
- Input Loopback Mode
- Pad Loopback Mode

Input loopback and Pad loopback are normally not used. See Appendix C: "Loopback Register Description" for description.

Note:	Only one loopback can be enabled at a time.

Figure 3-1 shows the loopback paths.

FIGURE 3-1: 1G AND 6G SERDES MACRO LOOPBACK PATHS



3.1.1 EQUIPMENT LOOPBACK MODE

Equipment Loopback mode is enabled by setting SERDESxG_COMMON_CFG.ENA_ELOOP. Data is looped back from the Serializer output to the Deserializer input, and the receive clock is recovered. The Equipment Loopback mode includes all transmit (Tx) and receive (Rx) functions, except for the Input and Output Buffers. Tx data can still be observed in the output (squelching data in the output is not possible).

3.1.2 FACILITY LOOPBACK MODE

Facility Loopback mode is enabled by setting SERDESxG_COMMON_CFG.ENA_FLOOP. The clock and parallel data outputs from the Deserializer are looped back to the Serializer input. Incoming serial data passes through the Input Buffer (IB), through the sampling stage controlled by the clock and data recovery (CDR) block, through the Deserializer, then back to the Serializer, and finally out through the Output Buffer (OB).

Note:	This loopback requires additional settings in the Serializer, SERDESxG_SER_CFG.

3.1.3 INPUT LOOPBACK MODE

Input Loopback mode is enabled by setting SERDESxG_COMMON_CFG.ENA_ILOOP. Data is asynchronously looped back from the IB to the OB.

3.1.4 PAD LOOPBACK MODE

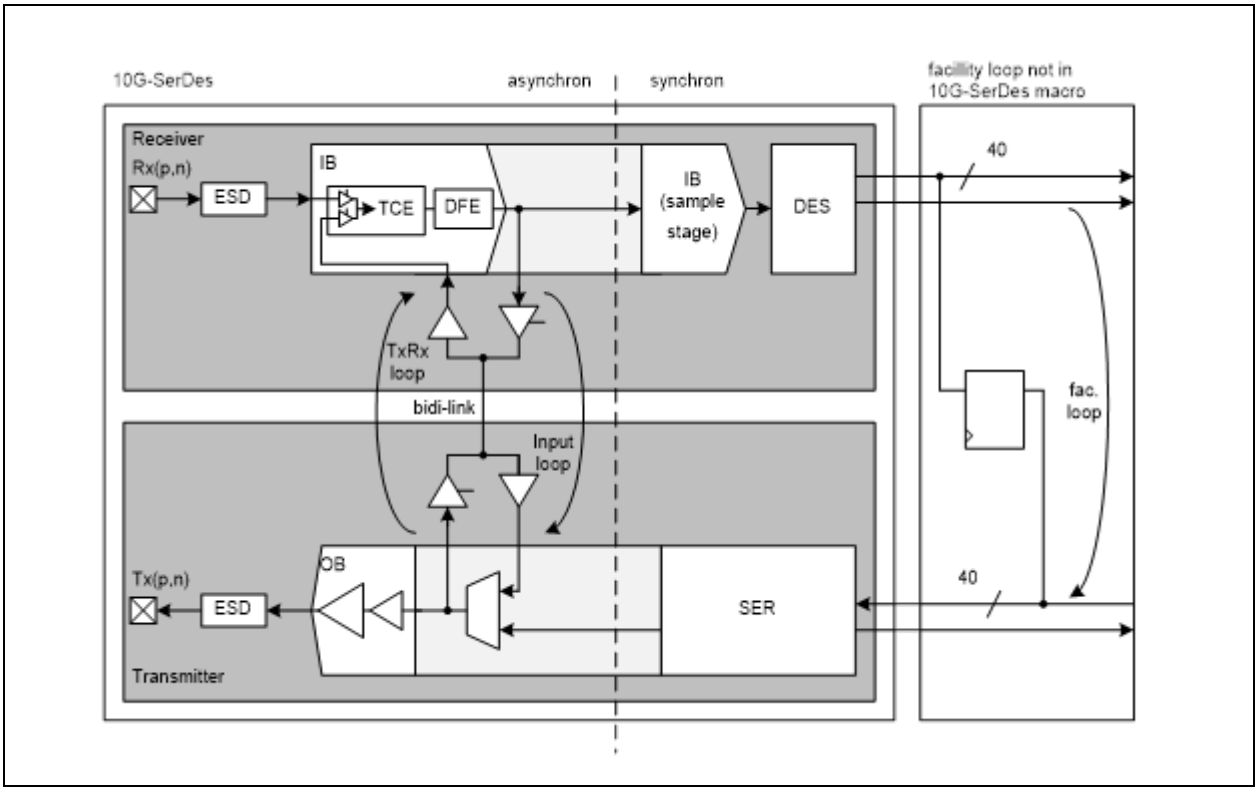
Pad Loopback mode is enabled by setting SERDESxG_COMMON_CFG.ENA_PLOOP. The Serializer output is feed back to the input of the Deserializer. This loopback includes both IB and OB.

3.2 10G SerDes Loopback

The 10G SerDes macro supports Input Loopback and Pad Loopback modes. Both loopback modes are asynchronous serial loops. The parallel facility loopback between the receiver and the transmitter is made outside the 10G SerDes macro in the PCS layer. See Appendix C: "Loopback Register Description" for description.

Figure 3-2 shows the loopback paths.

FIGURE 3-2: 10G SERDES MACRO LOOPBACK PATHS



3.2.1 INPUT LOOPBACK RX TO TX

Input Loopback is controlled by SD10G65_OB_CFG0.EN_INPUT_LOOP and SD10G65_IB_CFG10. IB_LOOP_DRV. This loopback is used to test the 10G-IB and 10G-OB buffers (the asynchronous part of the I/Os only). In Input Loopback mode serial data is traveling from the input pads through the IB's TCE and DFE stages, and further through the OB's predriver and driver stages to the output pads.

3.2.2 PAD LOOPBACK TX TO RX

Pad Loopback is controlled by SD10G65_OB_CFG0.EN_PAD_LOOP and SD10G65_IB_CFG10. IB_LOOP_REC. This loopback is the closest to the 10G pads from a core perspective. However, it is more of an Equipment Loopback than a Pad Loopback. The loop starts in the Tx buffer after the Serializer output (but before the filter stage, that is, predriver and driver stages) and is injected into the to the TCE stage of the Rx buffer, which is located before the Deserializer.

There is no interference with the external equipment connected to the I/Os, because TxRx Loop is establishing a connection between the transmitter and the receiver without connecting the I/O pads directly.

There is no common register to set up complete loopback. Therefore, both the `OB_CFG0` and `IB_CFG10` must be set up to enable the bidirectional multiplexers between Tx and Rx. Likewise, the Signal Detection (SD) circuitry is being bypassed, so SD must be forced high.

1. Set SD10G65_OB_CFG0.EN_PAD_LOOP = `1` (bit 16). Enable pad loop.
2. Set SD10G65_IB_CFG0.IB_SIG_SEL = `2` (bits 13:12). Input buffer source, OB to IB.
3. Set SD10G65_IB_CFG3.IB_SET_SDET = `1` (bit 26). Force Signal Detection to high.
4. Set SD10G65_IB_CFG10.IB_LOOP_REC = `1` (bit 17). Receive enable for BiDi loop.

See 4.3.4 "Enabling 10G SerDes PAD (Tx to Rx) Loopback".

See 4.4.2 "Enabling PCS PMA Loopback (Tx to Rx)".

3.3 Loopback Testing

Note:	All testing procedures in this section were done on a VSC5628EV reference board (PCB110).

3.3.1 1G SERDES EQUIPMENT LOOPBACK USING DEBUG COMMAND

```
// Enable debug commands
# platform debug allow

// Isolate the port when doing loopback test to avoid loops in the network,
// and stop protocols from transmitting frames. Port 1 use a 1G SerDes macro.
# configure terminal
(config)# interface GigabitEthernet 1/1
(config-if)# pvlan isolation
(config-if)# no spanning-tree
(config-if)# no lldp transmit
(config-if)# debug loopback equipment
(config-if)# end

// It is also a good idea to stop the DHCP client from sending ARP requests.
# configure terminal
(config)# interface vlan 1
(config-if-vlan)# no ip address
(config-if-vlan)# no ipv6 address
(config-if-vlan)# end

// Check for linkup
# show interface GigabitEthernet 1/1 status
Interface            Mode     Speed&Duplex  FlowControl  MaxFrame  Excessive  Link
-------------------  -------  ------------  -----------  --------  ---------  -----
GigabitEthernet 1/1  enabled  Auto          disabled     10240     Discard    Down

// If there is no linkup on the connected CuPHY port, the Switch Application
// doesn't allow you to transmit frames for testing the loopback. A way to simulate
// linkup is to enable the CuPHY near-end loopback also. The CuPHY loopback can
// also be used without having the SerDes equipment loopback enabled.
# configure terminal
(config)# interface GigabitEthernet 1/1
(config-if)# debug loopback near-end
(config-if)# end

# show interface GigabitEthernet 1/1 status
Interface            Mode     Speed&Duplex  FlowControl  MaxFrame  Excessive  Link
-------------------  -------  ------------  -----------  --------  ---------  -----
GigabitEthernet 1/1  enabled  Auto          disabled     10240     Discard    1Gfdx

// Clear statistics before test
# clear statistics *

//Setup the Switch Application to send 10,000 frames with packet size of 1234 bytes
# debug frame tx-cnt 10000
# debug frame tx interface GigabitEthernet 1/1 packet-length 1234
Transmitting 10000 frames...Done in 7.721 seconds.

# show interface GigabitEthernet 1/1 statistics
GigabitEthernet 1/1 Statistics:
Rx Packets:                    10000   Tx Packets:                    10000
Rx Octets:                  12380000   Tx Octets:                  12380000
Rx Unicast:                        0   Tx Unicast:                        0
Rx Multicast:                      0   Tx Multicast:                      0
Rx Broadcast:                  10000   Tx Broadcast:                  10000
Rx Pause:                          0   Tx Pause:                          0

Rx 64:                             0   Tx 64:                             0
Rx 65-127:                         0   Tx 65-127:                         0
Rx 128-255:                        0   Tx 128-255:                        0
Rx 256-511:                        0   Tx 256-511:                        0
Rx 512-1023:                       0   Tx 512-1023:                       0
Rx 1024-1526:                  10000   Tx 1024-1526:                  10000
Rx 1527-    :                      0   Tx 1527-    :                      0
```

3.3.2 1G SERDES FACILITY LOOPBACK MANUAL REGISTER SETUP

This setup uses the NPI port 48, which is using SerDes1G_0.

Note: The MAC counters will only count the Rx side and does not count on the Tx side.

```
// Enable debug commands
# platform debug allow

// Read out current SerDes settings from SerDes1G_0 to all shadow registers
# debug sym write ::MCB_SERDES1G_ADDR_CFG 0x40000001
Register                                    Value
HSIO:MCB_SERDES1G_CFG:MCB_SERDES1G_ADDR_CFG 0x40000001

// See current Serializer register value
# debug sym read ::SERDES1G_SER_CFG
Register                                  Value
HSIO:SERDES1G_ANA_CFG:SERDES1G_SER_CFG 0x00000000

// Change SERDES1G_SER_CFG.SER_ENALI = 1, SERDES1G_SER_CFG.SER_ALISEL = 0
# debug sym write ::SERDES1G_SER_CFG 0x1
Register                                  Value
HSIO:SERDES1G_ANA_CFG:SERDES1G_SER_CFG 0x00000001

// See current Common configuration register value
# debug sym read ::SERDES1G_COMMON_CFG
Register                                    Value
HSIO:SERDES1G_ANA_CFG:SERDES1G_COMMON_CFG 0x80040001

// Setup Facility loopback
# debug sym write ::SERDES1G_COMMON_CFG 0x80040401
Register                                    Value
HSIO:SERDES1G_ANA_CFG:SERDES1G_COMMON_CFG 0x80040401

// Write changes back to SerDes1G_0
# debug sym write ::MCB_SERDES1G_ADDR_CFG 0x80000001
Register                                    Value
HSIO:MCB_SERDES1G_CFG:MCB_SERDES1G_ADDR_CFG 0x80000001
#
```

3.3.3 1G SERDES FACILITY LOOPBACK USING DEBUG COMMAND

The NPI port is located on the Gigabit Ethernet port 1/21.

```
// Use debug loopback command,
# configure terminal
(config)# interface GigabitEthernet 1/21
(config-if)# debug loopback facility

// Do your external testing

// Disable loopback again
(config-if)# debug loopback disable
(config-if)# end
#
```

3.3.4 6G SERDES EQUIPMENT LOOPBACK USING DEBUG COMMAND

```
// Enable debug commands
# platform debug allow

// Isolate the port when doing loopback test to avoid loops, and stop protocols
// from transmitting frames. (Additionally, setup the port for 2G5 speed.)
# configure terminal
(config)# interface 2.5GigabitEthernet 1/1
(config-if)# pvlan isolation
(config-if)# no spanning-tree
(config-if)# no lldp transmit
(config-if)# speed 2500
(config-if)# debug loopback equipment
(config-if)# end

// It is also a good idea to stop the DHCP client from sending ARP requests.
# configure terminal
(config)# interface vlan 1
(config-if-vlan)# no ip address
(config-if-vlan)# no ipv6 address
(config-if-vlan)# end

// Check for linkup
# show interface 2.5GigabitEthernet 1/1 status
Interface               Mode     Speed&Duplex FlowControl MaxFrame Excessive Link
----------------------  -------  ------------ ----------- -------- --------- -----
2.5GigabitEthernet 1/1  enabled  2.5Gfdx      disabled    10240    Discard   Down

// If there is no linkup on the SFP port, the Switch Application doesn't allow you // to
transmit frames for testing the loopback. For linkup there needs at least to // be a module
detected on the SFP port - and it must be a 4G/8G/10G speed grade to // complying the 2G5 speed
setup - otherwise for 1G, a 1G module is sufficient.
// Also because a fiber is not used, signal detection in the PCS layer is disabled.

# debug sym read dev2g5[0]::pcs1g_link_status
Register                                      Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_LINK_STATUS 0x00005000

# debug sym read dev2g5[0]::pcs1g_sd_cfg
Register                                      Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_SD_CFG      0x00000011

# debug sym write dev2g5[0]::pcs1g_sd_cfg 0x0
Register                                      Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_SD_CFG      0x00000000

# debug sym read dev2g5[0]::pcs1g_link_status
Register                                      Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_LINK_STATUS 0x00005011

// Ups. Lost link again - Switch Application may have re-stored signal detection.
// Trying again
# debug sym read dev2g5[0]::pcs1g_link_status
Register                                      Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_LINK_STATUS 0x00005000

# debug sym read dev2g5[0]::pcs1g_sd_cfg
Register                                      Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_SD_CFG      0x00000011

# debug sym write dev2g5[0]::pcs1g_sd_cfg 0x0
Register                                      Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_SD_CFG      0x00000000
```

```
# debug sym read dev2g5[0]::pcs1g_link_status
Register                                    Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_LINK_STATUS 0x00005000

// Hmm. Trying again...
# debug sym write dev2g5[0]::pcs1g_sd_cfg 0x0
Register                                    Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_SD_CFG      0x00000000

# debug sym read dev2g5[0]::pcs1g_link_status
Register                                    Value
DEV2G5[0]:PCS1G_CFG_STATUS:PCS1G_LINK_STATUS 0x0000501

// Now finally, the Switch Application finds likup, so we can transmit frames.
# show interface 2.5GigabitEthernet 1/1 status
Interface              Mode     Speed&Duplex FlowControl MaxFrame Excessive Link
---------------------  -------  ------------ ----------- -------- --------- ------
2.5GigabitEthernet 1/1  enabled  2.5Gfdx      disabled    10240    Discard   2G5fdx

// Clear statistics before test
# clear statistics *

//Setup the Switch Application to send 10,000 frames with packet size of 1234 bytes
# debug frame tx-cnt 10000
# debug frame tx interface 2.5GigabitEthernet 1/1 packet-length 1234
Transmitting 10000 frames...Done in 12.921 seconds.

// Show statistics
# show interface 2.5GigabitEthernet 1/1 statistics
2.5GigabitEthernet 1/1 Statistics:
Rx Packets:                      10000   Tx Packets:                      10000
Rx Octets:                    12380000   Tx Octets:                    12380000
Rx Unicast:                          0   Tx Unicast:                          0
Rx Multicast:                        0   Tx Multicast:                        0
Rx Broadcast:                    10000   Tx Broadcast:                    10000
Rx Pause:                            0   Tx Pause:                            0

Rx 64:                               0   Tx 64:                               0
Rx 65-127:                           0   Tx 65-127:                           0
Rx 128-255:                          0   Tx 128-255:                          0
Rx 256-511:                          0   Tx 256-511:                          0
Rx 512-1023:                         0   Tx 512-1023:                         0
Rx 1024-1526:                    10000   Tx 1024-1526:                    10000
Rx 1527-    :                        0   Tx 1527-    :                        0

Rx Priority 0:                   10000   Tx Priority 0:                       0
Rx Priority 1:                       0   Tx Priority 1:                       0
Rx Priority 2:                       0   Tx Priority 2:                       0
Rx Priority 3:                       0   Tx Priority 3:                       0
Rx Priority 4:                       0   Tx Priority 4:                       0
Rx Priority 5:                       0   Tx Priority 5:                       0
Rx Priority 6:                       0   Tx Priority 6:                       0
Rx Priority 7:                       0   Tx Priority 7:                   10000

Rx Drops:                            0   Tx Drops:                            0
Rx CRC/Alignment:                    0   Tx Late/Exc. Coll.:                  0
Rx Undersize:                        0
Rx Oversize:                         0
Rx Fragments:                        0
Rx Jabbers:                          0
Rx Filtered:                         0
#
```

3.3.5 10G SERDES PAD LOOPBACK USING DEBUG COMMANDS

See 4.3.4 "Enabling 10G SerDes PAD (Tx to Rx) Loopback".

4.0 PRBS GENERATOR AND CHECKER

4.1 1G and 6G SerDes Device For Test (DFT) Features

The SerDes macro can do both pseudo random binary sequence (PRBS) generation and checking. The task is to provide a test pattern for the Tx path and to check the pattern received on the Rx path. For the 1G and 6G SerDes macros, the selected pattern is used on both the generator and checker; while for the 10G SerDes macro, the generator and checker have their own individual selection.

The generator and checker can be configured to use different test patterns:

- PRBS7 x^7 + x^6 + 1
- PRBS15 x^15 + x^14 + 1
- PRBS23 x^23 + x^18 + 1
- PRBS31 x^31 + x^28 + 1

In addition, the 10G SerDes macro can also perform PRBS9 and PRBS11.

Note:	A reboot does not alter back the SerDes settings, so when doing different testing, it is always a good starting point to perform it right after a power-cycle. With this, all test register settings are at their default value.

4.1.1 GENERATOR AND CHECKER COMMON CONFIGURATION

The DFT is controlled by SERDESxG_DFT_CFG0.TEST_MODE. To enable the predefined PRBS pattern generation and checking, the test mode should be set to BIST (= PRBS). Fixed and Random test patterns are also possible.

4.1.2 CHECKER STATUS

The DFT status can be monitored from SERDESxG_DFT_STATUS. There are several BIST status bits indicating active, sync result, complete, and error. Additionally, the 6G SerDes macro has a register for PRBS error counts, SERDES6G_ERR_CNT.PRBS_ERR_CNT.

4.1.3 GENERATING A FIXED PATTERN

As an example, below description shows *how to force idles out* using a fixed or constant pattern.

An Idle sequence (Clause 36) consists of two symbols /K28.5/D16.2/. The translation into “bits” is either /283/2B6/ or /17C/289/ depending on the last running disparity. (The sequence itself does not change the running disparity since the number of 0’s and 1’s are the same.)

Therefore, in a IEEE 802.3 compliant system, only /17C/289/ is transferred. The bit sequence to program is `0101111100_1010001001` = `0101 1111 0010 1000 1001` = `0x5F289`.

Note:	Since the sequence is transferred repeatedly, another valid sequence to program could be `1010_0010_0101_0111_1100` = `0xA257C` to get the same serial sequence out.

To make a fixed pattern, the steps are as follows:

1. Transfer the current SerDes macro settings to the shadow registers using the MCB register.
2. Set SERDESxG_TP_CFG0.STATIC_PATTERN0 = `0x5F289`.
3. Set SERDESxG_DFT_CFG0.TEST_MODE = `2`; # fixed/constant pattern generation.
4. Transfer settings back to SerDes macro using the MCB register.

4.2 6G SerDes PRBS Setup and Testing

Note:	All testing procedures in this section were done on a VSC7514EV reference board (PCB123).

4.2.1 TEST SETUP

The two outer most ports on the VSC7514EV reference board are interconnected using either DAC cabling (coax) or Optical SFP modules/fiber (4G optical SFP or higher, when testing 2.5G speed).

```
# show interface * status
Interface              Mode   Speed&Duplex FlowControl MaxFrame Excessive Link
---------------------- ------ ------------ ----------- -------- --------- --------
GigabitEthernet 1/1    enable Auto         disabled    10240    Discard   Down
GigabitEthernet 1/2    enable Auto         disabled    10240    Discard   Down
GigabitEthernet 1/3    enable sfp_auto_ams disabled    10240    Discard   Down
GigabitEthernet 1/4    enable sfp_auto_ams disabled    10240    Discard   Down
GigabitEthernet 1/5    enable Auto         disabled    10240    Discard   Down
GigabitEthernet 1/6    enable Auto         disabled    10240    Discard   Down
GigabitEthernet 1/7    enable Auto         disabled    10240    Discard   Down
GigabitEthernet 1/8    enable Auto         disabled    10240    Discard   Down
2.5GigabitEthernet 1/1 enable Auto         disabled    10240    Discard   Down
2.5GigabitEthernet 1/2 enable Auto         disabled    10240    Discard   1GfdxFiber
2.5GigabitEthernet 1/3 enable Auto         disabled    10240    Discard   1GfdxFiber
```

As shown, linkup is already present, which might be the full objective of testing the connection between ports, so there might not be a linkup initially in the test.

4.2.2 DETERMINING SERDES MACRO

A way of determine which SerDes macro a front port is using is to find out what internal port the Switch Application is using, and then look up the internal port against SerDes macro in the data sheet.

```
# platform debug allow

# deb api ail port in 2.5g 1/2
Application Interface Layer
===========================
Mapping:
Port  Chip Port  Chip  MIIM Bus  MIIM Addr  MIIM Chip
8     7          0     -1        0          0
Configuration:
Port  Interface  Serdes     Mode      Obey      Generate  Max Length
8     SERDES     1000BaseX  1Gfdx     Disabled  Disabled  10240+0
Forwarding:
Port  State  Forwarding  STP State   Auth State  Rx Fwd    Tx Fwd    Aggr Fwd
8     Up     Enabled     Forwarding  Both        Enabled   Enabled   Enabled

# deb api ail port in 2.5g 1/3
Application Interface Layer
===========================
Mapping:
Port  Chip Port  Chip  MIIM Bus  MIIM Addr  MIIM Chip
9     8          0     -1        0          0
Configuration:
Port  Interface  Serdes     Mode      Obey      Generate  Max Length
9     SERDES     1000BaseX  1Gfdx     Disabled  Disabled  10240+0
Forwarding:
Port  State  Forwarding  STP State   Auth State  Rx Fwd    Tx Fwd    Aggr Fwd
9     Up     Enabled     Forwarding  Both        Enabled   Enabled   Enabled
```

Referencing the data sheet, it can be seen that internal ports 7 and 8 are connected to SerDes 6G macro #0 and #1.

Note: It might be necessary to read out the internal port multiplexer settings by looking at the HW_CFG register to find the correct mapping between internal ports and SerDes macro numbers.

4.2.3 6G SERDES PRBS TESTING

```
// Readout SerDes6G macro #0
# deb sym write ::mcb_serdes6g_addr_cfg 0x40000001
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x40000001

// If you are doing some script automation, always ensure the last (write) command
// is finish. That is to expect 0x00000001, when the mask register is being read.
# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000001

// See current PRBS status
# deb sym read ::serdes6g_dft_status ( -> BIST not started and not completed)
Register                                     Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_DFT_STATUS 0x000000c2

// Always start a test by disabling the BIST engine. This is important - as first
// (or last) step. Otherwise the status does not change or update between tests.
# deb sym write ::serdes6g_dft_cfg0 0
Register                                 Value
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG0 0x00000000

// Write to SerDes6G macro #0 (mask bit 0 = 1) to update it
# deb sym write ::mcb_serdes6g_addr_cfg 0x80000001
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x80000001

// Read back status of last write command
# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000001

// Now Setup for PRBS-31 testing (Pattern=3, Test mode=1 BIST)
# deb sym write ::serdes6g_dft_cfg0 0x00310000
Register                                 Value
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG0 0x00310000

// Write to SerDes6G macro #0 (mask bit 0 = 1)
# deb sym write ::mcb_serdes6g_addr_cfg 0x80000001
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x80000001
# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000001

// Readout SerDes6G macro #1 to get status value
# deb sym write ::mcb_serdes6g_addr_cfg 0x40000002
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x40000002
# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000002

// See current status
# deb sym read ::serdes6g_dft_status (-> BIST not started and not completed)
Register                                     Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_DFT_STATUS 0x000000c2

// Now setup the other port for BIST. Always start disabling bist testing
# deb sym write ::serdes6g_dft_cfg0 0
Register                                 Value
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG0 0x00000000
```

```
// Write to SerDes6G macro #1 (mask bit 1 = 1)
# deb sym write ::mcb_serdes6g_addr_cfg 0x80000002
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x80000002
# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000002

// Setup for PRBS-31 testing (Pattern=3, Test mode=1 BIST)
# deb sym write ::serdes6g_dft_cfg0 0x00310000
Register                                  Value
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG0 0x00310000
// Write to SerDes6G macro #1 (mask bit 1 = 1)
# deb sym write ::mcb_serdes6g_addr_cfg 0x80000002
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x80000002
# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000002
```

Then find the current status for the PRBS testing, when both ends run the same PRBS pattern.

```
// Readout SerDes6G macro #1 (mask bit 1 = 1)
# deb sym write ::mcb_serdes6g_addr_cfg 0x40000002
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x40000002

# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000002

// See current status (-> PRBS checker synchronized, BIST active, Errors were found)
# deb sym read ::serdes6g_dft_status
Register                                     Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_DFT_STATUS 0x000001c0

// See current error counts
# deb sym read ::serdes6g_err_cnt
Register                                  Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_ERR_CNT 0x00000000

// Readout SerDes6G macro #0 (mask bit 0 = 1)
# deb sym write ::mcb_serdes6g_addr_cfg 0x40000001
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x40000001

# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000001

// See current status
# deb sym read ::serdes6g_dft_status (-> Synchronization on BIST data failed)
Register                                     Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_DFT_STATUS 0x000000c6

// See current error counts
# deb sym read ::serdes6g_err_cnt
Register                                  Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_ERR_CNT 0x00000000

// Try to reset PRBS test to get new status
# deb sym write ::mcb_serdes6g_addr_cfg 0x40000001
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x40000001

# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000001

// Disabling bist testing on macro #0
# deb sym write ::serdes6g_dft_cfg0 0
Register                                 Value
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG0 0x00000000

// Write to SerDes6G macro #0 (mask bit 0 = 1)
# deb sym write ::mcb_serdes6g_addr_cfg 0x80000001
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x80000001

# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000001
```

```
// Setup for PRBS-31 testing (Pattern=3, Test mode=1 BIST)
# deb sym write ::serdes6g_dft_cfg0 0x00310000
Register                                Value
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG0 0x00310000

# deb sym write ::mcb_serdes6g_addr_cfg 0x80000001
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x80000001

# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000001

// Readout SerDes6G macro #0 (mask bit 0 = 1)
# deb sym wr ::mcb_serdes6g_addr_cfg 0x40000001
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x40000001

# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000001
// See current status
# deb sym read ::serdes6g_dft_status (-> PRBS checker synchronized)
Register                                     Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_DFT_STATUS 0x000001c0

// See current error counts
# deb sym read ::serdes6g_err_cnt
Register                                  Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_ERR_CNT 0x00000000

// Readout SerDes6G macro #1 (mask bit 1 = 1)
# deb sym write ::mcb_serdes6g_addr_cfg 0x40000002
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x40000002

# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000002

// See current status
# deb sym read ::serdes6g_dft_status (-> PRBS checker synchronized)
Register                                     Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_DFT_STATUS 0x000001c0

// See past error counts -> counter satuated at 0xffff
# deb sym read ::serdes6g_err_cnt
Register                                  Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_ERR_CNT 0x0000ffff

// The counter can be cleared by writing 0 to the register.
# deb sym write ::serdes6g_err_cnt 0
Register                                  Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_ERR_CNT 0x00000000

// Write back to update SerDes6G macro #1 (mask bit 1 = 1)
# deb sym write ::mcb_serdes6g_addr_cfg 0x80000002
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x80000002
# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000002
```

```
// Readout SerDes6G macro #1 (mask bit 1 = 1)
# deb sym write ::mcb_serdes6g_addr_cfg 0x40000002
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x40000002

# deb sym read ::mcb_serdes6g_addr_cfg
Register                                    Value
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x00000002
// See current error counts

# deb sym read ::serdes6g_err_cnt
Register                                  Value
HSIO:SERDES6G_DIG_STATUS:SERDES6G_ERR_CNT 0x00000000
```

4.3 10G SerDes PRBS Setup and Testing

The 10G DFT BIST PRBS generator and checker work independently; thus each must be set up individually.

4.3.1 PRBS GENERATOR SETUP

1. Set DFT_TX_CFG to `0x1920` for PRBS31. For PRBS9, use `0x1960`.
2. Set DFT_TX_CFG to `0x1921`; enable the PRBS generator. For PRBS9, use `0x1961`.

4.3.2 PRBS CHECKER SETUP

1. Set DFT_BIST_CFG0 to `0x000A0000` (`WAKEUP_DLY_CFG`).
2. Set DFT_BIST_CFG3 to `0x0000000A` (`MAX_STABLE_ATTEMPT_CFG`).
3. Set DFT_BIST_CFG1 to `0x00140000` (`MAX_UNSTABLE_CYC_CFG`).
4. Set DFT_BIST_CFG1 to `0x0014000A` (`STABLE_THRES_CFG`).
5. Set DFT_BIST_CFG2 to `0x000003E7` (`FRAME_LEN_CFG`).
6. Set DFT_BIST_CFG0 to `0x000A7A11` (`MAX_BIST_FRAMES_CFG`).
7. Set DFT_RX_CFG to `0x002225C0`; BIST checker for PRBS31. For PRBS9, use `0x00222DC0`.
8. Set DFT_RX_CFG to `0x002225C4`; enable the PRBS checker. For PRBS9, use `0x00222DC4`.

Note: Steps 1 to 6 set up the BIST FSM. Please follow these steps without any variation.

4.3.3 CHECKER STATUS: ENABLE/DISABLE SHOWING ERROR COUNTER

Once the PRBS generator is enabled, the PCS_10GBASE_R::PCS_STATUS register will not be `0x8` (= Sync acquired), because the PRBS pattern is not sending normal symbols.

1. Read DFT_MAIN_STAT. Read to confirm a good link with BIST established, that is, `0x0001`. Without a good link, the error counter readout will be useless.
2. Set DFT_RX_CFG to `0x012225C4`. Capture internal error counter to read back register.
3. Read DFT_ERR_STAT (ERR_CNT).
4. Set DFT_RX_CFG to `0x002225C4`. Release capture from internal error counter.

Note: When using the PRBS BIST engine, the error counter will indicate zero error count if either there are no transmission errors or the link is broken.

If the error counter is steady `0x0` when the PRBS BIST engine is enabled, a quick and alternative way to check the error counter is to press a thumb on the exposed portion of the 10G traces or at the AC-coupling of the 10G traces. Because of the change of capacitance, it usually generates a couple of errors. If DFT_ERR_STAT counts errors, when the trace is pressed by the thumb, it means that the link is good and the error counter is functioning properly.

4.3.4 ENABLING 10G SERDES PAD (TX TO RX) LOOPBACK

```
# deb sym write pcs10g_br[0]::pcs_sd_cfg 0x11
Register                              Value
PCS10G_BR[0]:PCS_10GBR_CFG:PCS_SD_CFG 0x00000011

# deb sym read  xgana[0]::sd10g65_ob_cfg0
Register                             Value
XGANA[0]:SD10G65_OB:SD10G65_OB_CFG0 0x00002187

# deb sym write xgana[0]::sd10g65_ob_cfg0 0x00012187
Register                             Value
XGANA[0]:SD10G65_OB:SD10G65_OB_CFG0 0x00012187

# deb sym read  xgana[0]::sd10g65_ib_cfg0
Register                             Value
XGANA[0]:SD10G65_IB:SD10G65_IB_CFG0 0x04004ea6

# deb sym write xgana[0]::sd10g65_ib_cfg0 0x04006ea6
Register                             Value
XGANA[0]:SD10G65_IB:SD10G65_IB_CFG0 0x04006ea6

# deb sym read  xgana[0]::sd10g65_ib_cfg3
Register                             Value
XGANA[0]:SD10G65_IB:SD10G65_IB_CFG3 0x28014042

# deb sym write xgana[0]::sd10g65_ib_cfg3 0x2c014042
Register                             Value
XGANA[0]:SD10G65_IB:SD10G65_IB_CFG3 0x2c014042

# deb sym read  xgana[0]::sd10g65_ib_cfg10
Register                              Value
XGANA[0]:SD10G65_IB:SD10G65_IB_CFG10 0x04000080

# deb sym write xgana[0]::sd10g65_ib_cfg10 0x00020080
Register                              Value
XGANA[0]:SD10G65_IB:SD10G65_IB_CFG10 0x00020080
#
```

4.3.5 10G SERDES PRBS31 TESTING

```
// See current status
# deb sym read pcs10g_br[0]::pcs_status
Register                                  Value
PCS10G_BR[0]:PCS_10GBR_STATUS:PCS_STATUS 0x00000008       <-- linkup

// Enable PRBS generator with PRBS31
# deb sym write xgdig[0]::dft_tx_cfg 0x1921
Register                        Value
XGDIG[0]:SD10G65_DFT:DFT_TX_CFG 0x00001921

# deb sym write xgdig[0]::dft_bist_cfg0 0x000a0000
Register                            Value
XGDIG[0]:SD10G65_DFT:DFT_BIST_CFG0 0x000a0000

# deb sym write xgdig[0]::dft_bist_cfg3 0x0000000a
Register                            Value
XGDIG[0]:SD10G65_DFT:DFT_BIST_CFG3 0x0000000a

# deb sym write xgdig[0]::dft_bist_cfg1 0x00140000
Register                            Value
XGDIG[0]:SD10G65_DFT:DFT_BIST_CFG1 0x00140000

# deb sym write xgdig[0]::dft_bist_cfg1 0x0014000a
Register                            Value
XGDIG[0]:SD10G65_DFT:DFT_BIST_CFG1 0x0014000a

# deb sym write xgdig[0]::dft_bist_cfg2 0x000003e7
Register                            Value
XGDIG[0]:SD10G65_DFT:DFT_BIST_CFG2 0x000003e7

# deb sym write xgdig[0]::dft_bist_cfg0 0x000a7a11
Register                            Value
XGDIG[0]:SD10G65_DFT:DFT_BIST_CFG0 0x000a7a11

# deb sym write xgdig[0]::dft_rx_cfg 0x002225c0
Register                        Value
XGDIG[0]:SD10G65_DFT:DFT_RX_CFG 0x002225c0

# deb sym write xgdig[0]::dft_rx_cfg 0x002225c4
Register                        Value
XGDIG[0]:SD10G65_DFT:DFT_RX_CFG 0x002225c4

# deb sym read xgdig[0]::dft_main_stat
Register                            Value
XGDIG[0]:SD10G65_DFT:DFT_MAIN_STAT 0x00000000       <-- BIST NOT ACTIVE???
#
```

4.4 10G PCS Layer PRBS31 Generator and Checker

An alternative for PRBS31 generation and checking other than the 10G SerDes macro is to use 10G PCS layer test features.

Once the PRBS generator is enabled (either using that in the SerDes block or that in the PCS block), the PCS_10GBASE_R::PCS_STATUS register will not show `0x8` (= Sync acquired), because the PRBS pattern is not sending normal symbols. Instead, the register will show `0x10` if the pattern checker finds a match.

If possible, make sure that the link status is good first by checking the PCS_10GBASE_R::PCS_STATUS register, which should consistently read back as `0x8` before enabling the PRBS BIST engine.

If the PCS TEST_ERR_CNT is steady `0x0` when the PRBS generator is enabled, a quick check is to press a thumb on the exposed portion of the 10G traces or at the AC-coupling of the 10G traces. Because of the change of capacitance, it usually generates a couple of errors. If the register then counts errors, it means the link is good and the error counter is functioning properly.

4.4.1 PCS PRBS GENERATOR AND CHECKER SETUP

1. Read PCS_10GBASE_R::PCS_STATUS and expect `0x8`.
2. Set PCS_10GBASE_R::TEST_CFG to `0x20002` to select PRBS31 test pattern.
3. Set PCS_10GBASE_R::PCS_CFG to `0x80002010` to enable the BIST generator and checker.
4. Read PCS_10GBASE_R::TEST_ERR_CNT for error counts.

4.4.2 ENABLING PCS PMA LOOPBACK (TX TO RX)

Set PCS_10GBASE_R::PCS_CFG.PMA_LOOPBACK_ENA.

4.4.3 10G PCS PRBS31 TEST

```
// 10G port 1 and 2 are interconnected using DAC cabling
# deb sym read pcs10g_br[0-1]::pcs_status
Register                                  Value
PCS10G_BR[0]:PCS_10GBR_STATUS:PCS_STATUS 0x00000008       <-- linkup
PCS10G_BR[1]:PCS_10GBR_STATUS:PCS_STATUS 0x00000008

// Setup PRBS31 in Tx and Rx side
# deb sym write pcs10g_br[0-1]::test_cfg 0x20002
Register                              Value
PCS10G_BR[0]:PCS_10GBR_CFG:TEST_CFG 0x00020002
PCS10G_BR[1]:PCS_10GBR_CFG:TEST_CFG 0x00020002

// Enable PMA loopback
# deb sym read pcs10g_br[0-1]::pcs_cfg
Register                             Value
PCS10G_BR[0]:PCS_10GBR_CFG:PCS_CFG 0xbf000000
PCS10G_BR[1]:PCS_10GBR_CFG:PCS_CFG 0xbf000000

// Enable BIST engine
# deb sym write pcs10g_br[0-1]::pcs_cfg 0xff002010
Register                             Value
PCS10G_BR[0]:PCS_10GBR_CFG:PCS_CFG 0xff002010
PCS10G_BR[1]:PCS_10GBR_CFG:PCS_CFG 0xff002010

// Check for Pattern Match
# deb sym read pcs10g_br[0-1]::pcs_status
Register                                  Value
PCS10G_BR[0]:PCS_10GBR_STATUS:PCS_STATUS 0x00000010       <-- Match
PCS10G_BR[1]:PCS_10GBR_STATUS:PCS_STATUS 0x00000010       <-- Match

// Read error counts
# deb sym read pcs10g_br[0-1]::test_err_cnt
Register                                       Value
PCS10G_BR[0]:PCS_10GBR_HA_STATUS:TEST_ERR_CNT 0x000000a3
PCS10G_BR[1]:PCS_10GBR_HA_STATUS:TEST_ERR_CNT 0x00000069

# deb sym read pcs10g_br[0-1]::test_err_cnt
Register                                       Value
PCS10G_BR[0]:PCS_10GBR_HA_STATUS:TEST_ERR_CNT 0x000000a3  <-- No change
PCS10G_BR[1]:PCS_10GBR_HA_STATUS:TEST_ERR_CNT 0x00000069  <-- No change

// Remove loopback
# deb sym write pcs10g_br[0-1]::pcs_cfg 0xbf002010
Register                             Value
PCS10G_BR[0]:PCS_10GBR_CFG:PCS_CFG 0xbf002010
PCS10G_BR[1]:PCS_10GBR_CFG:PCS_CFG 0xbf002010

// Read error counts
# deb sym read pcs10g_br[0-1]::test_err_cnt
Register                                       Value
PCS10G_BR[0]:PCS_10GBR_HA_STATUS:TEST_ERR_CNT 0xd523e7e3  <-- errors
PCS10G_BR[1]:PCS_10GBR_HA_STATUS:TEST_ERR_CNT 0xdad82da7

# deb sym read pcs10g_br[0-1]::test_err_cnt
Register                                       Value
PCS10G_BR[0]:PCS_10GBR_HA_STATUS:TEST_ERR_CNT 0xf78fb3f8
PCS10G_BR[1]:PCS_10GBR_HA_STATUS:TEST_ERR_CNT 0x01d8d6d9
#
```

5.0 OUTPUT BUFFER CONTROL

5.1 1G SerDes Output Buffer Configuration

The 1G SerDes Output Buffer (OB) supports the following configurable options:

- Amplitude Control
- Slope/Slew Rate Control
- Common-Mode Voltage Control
- Tx and Rx Polarity Inversion (P and N Swap)
- Selectable 3 dB De-Emphasis
- DC Level or Idle Mode

5.1.1 AMPLITUDE CONTROL

The amplitude of the OB is controlled by SERDES1G_OB_CFG.ob_amp_ctrl. The output amplitude can be adjusted in 50 mV peak-to-peak differential steps from 0.4 Vppd to 1.1 Vppd.

The output amplitude depends on the OB's supply voltage. The OB can be supplied with 1.0V or 1.2V for increased amplitudes. In 1V mode, the amplitude setting is limited around the value ~6 (~700 mVppd). In 1.2V mode, maximum amplitude setting is 15 (~1100 mVppd).

5.1.2 SLOPE/SLEW RATE CONTROL

The slew rate of the OB is controlled by SERDES1G_OB_CFG.ob_slp. The slew rate is adjustable with the following control settings:

- 0: 45 ps
- 1: 85 ps
- 2: 105 ps
- 3: 115 ps (default)

5.1.3 COMMON-MODE VOLTAGE CONTROL

Common-mode voltage of the OB is controlled by SERDES1G_OB_CFG.ob_vcm_ctrl. The common-mode voltage is adjustable in a range from 440 mV to 570 mV.

- 0000: Reserved. (Off ' CMV ~500 mV)
- 0001: 440 mV
- 0011: 460 mV
- 0010: 480 mV
- 0110: 500 mV
- 0100: 530 mV (default)
- 1100: 550 mV
- 1000: 570 mV

All other settings are not applicable. Note that the control settings are (grayed) encoded.

5.1.4 TX AND RX POLARITY INVERSION (P AND N SWAP)

The data streams in the Tx and Rx directions can be inverted by:

- SERDES1G_MISC_CFG.TX_DATA_INV_ENA
- SERDES1G_MISC_CFG.RX_DATA_INV_ENA

This effectively allows for swapping the P and N lines of the high-speed serial link to ease the layout process.

5.1.5 SELECTABLE 3 DB DE-EMPHASIS

The 1G OB supports a fixed 3 dB de-emphasis that can be enabled by setting SERDES1G_SER_CFG.ser_deemph.

5.1.6 DC LEVEL OR IDLE MODE

Idle mode is enabled by SERDES1G_SER_CFG.ser_idle. The OB supports an Idle mode that results in a differential peak-to-peak output swing of less than 30 mV. A constant pattern (either 0's or 1's) must be selected as input data for the OB (test-pattern register can be used).

Note:	Idle mode should not be mistaken as the 10b8b-defined Idle sequences, IEEE 802.3 Clause 36.

5.2 SerDes6G Output Buffer Configuration

The 6G SerDes OB supports the following configurable options:

- Amplitude Control
- De-Emphasis and Amplitude Settings
- Slew Rate/Slope Control
- Skew Adjustment
- Tx and Rx Polarity Inversion (P and N Swap)
- DC Level or (PCIe®) Idle Mode

5.2.1 AMPLITUDE CONTROL

The amplitude of the OB is controlled by SERDES6G_OB_CFG1.ob_lev. The absolute level of the output amplitude can be adjusted in steps of 6.7 mV peak-to-peak differential from 520 mVppd to around 960 mVppd.

The maximum output amplitude depends on the OB's supply voltage. For interface standards requiring higher output amplitudes (backplane application, interfacing to optical modules), the 6G SerDes OB can be supplied from a 1.2V instead of a 1.0V supply. As default configuration, the OB is set to 1.0V mode. Enabling the 1.0V mode when supplied from 1.2V must be avoided.

In 1V mode, the amplitude setting is limited around ob_lev value ~48 (~760 mVppd). In 1.2V mode, maximum amplitude setting is ob_lev value of 63 (~920 mVppd).

FIGURE 5-1: 6G SERDES AMPLITUDE VS. OB_LEV SETTING AND INTERFACE FREQUENCY

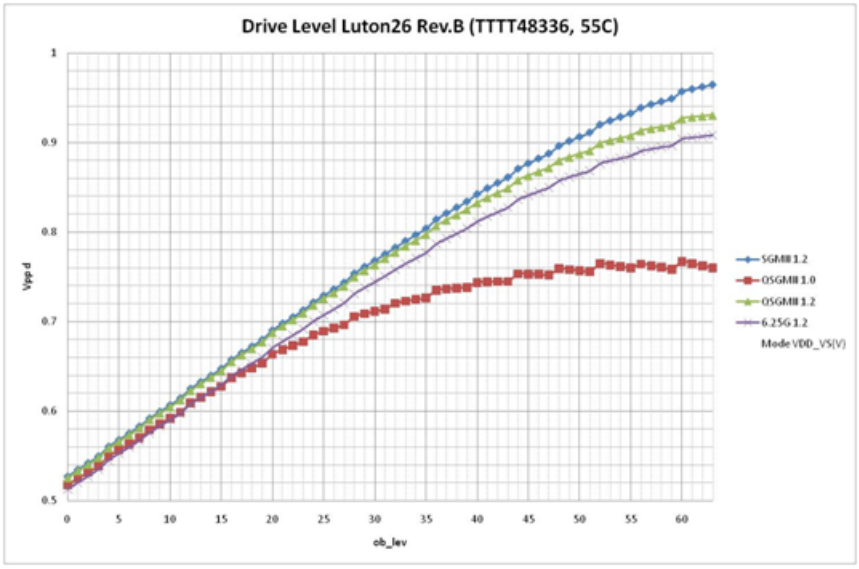


Figure 5-1 shows the following interface modes:

- Red: 1.0V running QSGMII (5 GHz)
- Green: 1.2V running QSGMII (5 GHz)
- Blue: 1.2V running SGMII (1.25 GHz)
- Violet: 1.2V running RXAUI (6.25 GHz)

5.2.2 DE-EMPHASIS AND AMPLITUDE SETTINGS

The 6G SerDes OB can provide up to 12 dB of de-emphasis. A rule of thumb is for each 3 dB de-emphasis the transmission length doubles.

The OB supports a four-tap de-emphasis filter consisting of one precursor, a center tap, and two post-cursors.

- The precursor coefficient, C_0, is configured by ob_prec. C_0 is a 5-bit value, with the msb defining the polarity. The lower 4-bit value is defined as B_0.
- The first post-cursor coefficient, C_2, is configured by ob_post0. C_2 is a 6-bit value, with the msb defining the polarity. The lower 5-bit value is defined as B_2.
- The second post-cursor coefficient, C_3, is configured by ob_post1. C_3 is 5-bit value, with the msb defining the polarity. The lower 4-bit value is defined as B_3.
- The center-tap coefficient, C_1, is a 6-bit value. Its polarity can be programmed by ob_pol, which is defined as p_1. For normal operation, the polarity must be set to 1. The value of the 6 bits forming C_1 is internally calculated using Equation 5-1.

EQUATION 5-1: CENTER-TAP COEFFICIENT, C1

$$C_1 = (64 - (B_0 + B_2 + B_3)) * p_1$$

The output amplitude is programmed by SERDES6G_OB_CFG1.OB_LEV, which is a 6-bit value. This value is internally increased by 64 and defines the amplitude coefficient, K. The range of K is therefore 64 to 127. The differential peak-to-peak output amplitude calculates to 6.7 mVppd * K.

The maximum peak-to-peak output amplitude depends on the data stream and can be calculated using Equation 5-2:

EQUATION 5-2: MAXIMUM PEAK-TO-PEAK OUTPUT AMPLITUDE

$$H(Z) = 3.375\ mVpp * K * (C_0 z^1 + C_1 z^0 + C_2 z^{-1} + C_3 z^{-2})/64$$

Where, z^x denotes the current bits of the data pattern defining the amplitude of Z.

The output amplitude also depends on the OB's supply voltage. Refer to Section 5.2.1, "Amplitude Control" for the dependencies between the maximum achievable output amplitude and the supply voltage.

The configuration bits are summarized in Table 5-1.

TABLE 5-1: 6G DE-EMPHASIS REGISTERS

Register Name	Description
SERDES6G_OB_CFG.OB_POL	Selects the output to be inverted p_1
SERDES6G_OB_CFG.OB_POST0	Coefficient for first post-cursor setting C_2 Range: –31 to 31
SERDES6G_OB_CFG.OB_POST1	Coefficient for second post-cursor setting C_3 Range: –15 to 15
SERDES6G_OB_CFG.OB_PREC	Coefficient for precursor setting C_0 Range: –15 to 15
SERDES6G_OB_CFG1.OB_LEV	Amplitude coefficient, K = ob_lev + 64 Range: 0 to 63

Initially, it is recommended to keep the precursor and second post-cursor at 0 and only use the first post-cursor. The center-cursor is internally adjusted, as it is related to the other cursor settings.

When using the first post-cursor, the first bit after a transition is emphasized, resulting in a higher amplitude compared to the consecutive bits of the same polarity. Note that, at some point, higher values might excessively reduce the amplitude, which is the nature of how de-emphasis is implemented.

When interconnecting two devices, sometimes it is not always the best approach to comply strictly to specific standardized transmission template. Often, the test result for best interconnect involves setting the de-emphasis higher than the template allows. This may be due to the resulting damping; thus, lowering cross-talk between lanes.

- Equalization: SERDES6G_OB_CFG.OB_PREC = `0` (default is `0`)
- Short channel: SERDES6G_OB_CFG.OB_POST0 = `4...6` (default is `0`)
- Long channel: SERDES6G_OB_CFG.OB_POST0 = `7...20` or so

5.2.3 SLEW RATE/SLOPE CONTROL

The OB slew rate is controlled by two configuration settings: (a) coarse adjustment that is done with SERDES6G_OB_CFG.OB_SR_H and (b) fine adjustment that is done with SERDES6G_OB_CFG.OB_SR.

Note: The ob_sr ranges from 0 to 15 but does not care about the lsb setting.

- Setting OB_SR_H = `0`, the slew rate range between 30 ps to 60 ps using OB_SR.
- Setting OB_SR_H = `1`, the slew rate range between 60 ps to 140 ps using OB_SR.

For faster edge rates than the default setting (1.25 Gb/s SGMII), you can set:

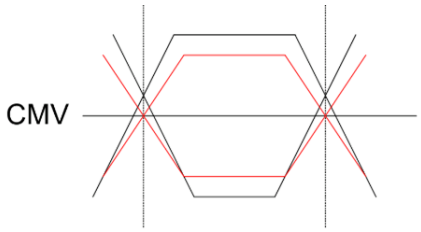
- SERDES6G_OB_CFG.OB_SR_H = `0` (default is `1`)
- SERDES6G_OB_CFG.OB_SR = `0` (default is `7`)

5.2.4 SKEW ADJUSTMENT

Skew-adjustment or common-mode noise minimization can be controlled by SERDES6G_OB_CFG1. OB_ENA_CAS. It is important to understand that there is a principal side effect of the CAS setting to the amplitude and rise/fall (r/f) time.

Figure 5-2 shows: (a) red is ob_ena_cas = `b'001`, and (b) black is ob_ena_cas = `b'100`.

FIGURE 5-2: DEPENDENCIES BETWEEN CAS SETTING AND AMPLITUDE, RISE/FALL TIME



The control setting is (1-bit-hot) encoded (all other settings are not applicable):

- 000: QSGMII mode. Lowest r/f time and highest amplitude for higher data rate.
- 001: Lowest skew. Lower r/f time and with reduced amplitude.
- 010: SGMII mode. Medium r/f time with adequate common-mode noise for lower data rate.
- 100: Highest skew. Highest r/f time and highest amplitude, lowest common-mode noise.

Note: Skew adjustment is only required for 1 Gbps SGMII mode.

5.2.5 TX AND RX POLARITY INVERSION (P AND N SWAP)

The data streams in the Tx and Rx direction can be inverted by:

- SERDES6G_MISC_CFG.TX_DATA_INV_ENA
- SERDES6G_MISC_CFG.RX_DATA_INV_ENA

This allows for swapping the P and N lines of the high-speed serial link to ease the layout process.

Note:	SERDES6G_OB_CFG.OB_POL also controls the output to be non-inverted or inverted (default). OB_POLI = 1 (inverted) should be set for all operation modes to comply to standards.

5.2.6 DC LEVEL OR (PCIE®) IDLE MODE

The OB supports an Idle mode, which forces the output to 0V (the differential peak-to-peak output swing is less than 30 mV). Idle mode is controlled by SERDES6G_OB_CFG.OB_IDLE.

Note:	Idle mode should not be mistaken as the 10b8b defined Idle sequences, IEEE 802.3 Clause 36.

5.3 SerDes10G Output Buffer Configuration

The 10G SerDes OB supports the following configurable options:

- Amplitude Control
- De-Emphasis (CM, C0, and CP)
- Slew Rate Control
- Tx and Rx Polarity Inversion (P and N Swap)
- 10G KR Auto-Negotiation, Training and FEC

5.3.1 AMPLITUDE CONTROL

The amplitude of the OB is controlled by two configuration settings: (a) coarse adjustment is done with SD10G65_OB_CFG0.INCR_LEVn and (b) fine adjustment is done with SD10G65_OB_CFG0.LEVn. Set INCR_LEVn to 0 (default is 1) to select highest amplitude range.

The output amplitude can be adjusted in 25 mV peak-to-peak differential steps. The amplitude level ranges from 0 to 31 with decreasing amplitude, when increasing the LEVn control value:

- Setting INCR_LEVn = 0, the amplitude range between 31:500 to 0:1275 mVpp
- Setting INCR_LEVn = 1, the amplitude range between 31:300 to 0:1075 mVpp

The output amplitude depends on the OB's supply voltage. The OB can be supplied by 1.0V or 1.2V. Normally, it is recommended to use 1.2V for increased amplitudes.

It is advised to use a lower amplitude, as the OB performs better jitterwise, when it gets more linear (refer to the red line on Figure 5-1). By default, LEVn = 0x7 and INCR_LEVn = 0.

5.3.2 DE-EMPHASIS (CM, C0, AND CP)

The OB supports a four-tap de-emphasis filter controlled by SD10G65_OB_CFG2.d_filter register to set up the precursor CM, the first post-cursor C0, and the second post-cursor CP parameters adjusting the 10G output FIR control.

The d_filter value consists of four 6-bit precalculated DA input values. A spreadsheet (kr_taps_conv.xlsx) exists, which gives the precalculated d_filter value conforming the four-tap de-emphasis from an input of CM, C0, and CP parameters.

Note:	Each input value (CM, C0, and CP) must be in the range of [–31...31], and the sum of abs(CM)+abs(C0)+abs(CP) <= 31.

Table 5-2 shows some precalculated settings using the kr_taps_conv.xlsx spreadsheet.

TABLE 5-2: PRECALCULATED D_FILTER VALUE

De-emphasis	Pre/CM	Post1/C0	Post2/CP	d_filter
0.0 dB	0	31	0	0x7DF820
~0.7 dB	0	30	–1	0x75F822
~1.5 dB	0	29	–2	0x6DF824
~2.2 dB	0	28	–3	0x65F826
~3.0 dB	0	27	–4	0x5DF828
~3.7 dB	0	26	–5	0x55F82A

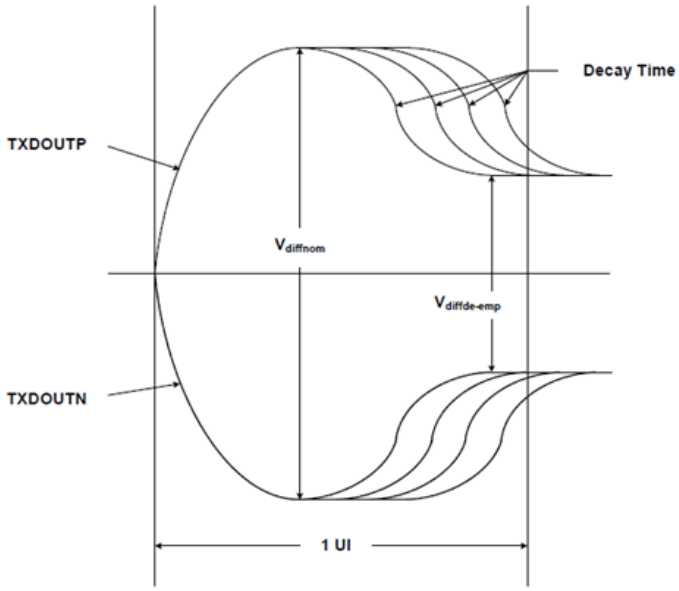
TABLE 5-2: PRECALCULATED D_FILTER VALUE (CONTINUED)

De-emphasis	Pre/CM	Post1/C0	Post2/CP	d_filter
~4.5 dB	0	25	–6	0x4DF82C
~5.2 dB	0	24	–7	0x45F82E
~6.0 dB	0	23	–8	0x3DF830
~7.5 dB	0	22	–9	0x35F832

The de-emphasis level is 20 x $Log_{10}(V_{diffnom}/V_{diffde-emp})$ dB (see Figure 5-3).

De-emphasis affects the peaking and decay time (slew rate) of the transmitted bit. Figure 5-3 shows the de-emphasized waveform.

FIGURE 5-3: TRANSMITTER AMPLITUDE LEVEL WITH DE-EMPHASIS



Note: Figure 5-3 is for reference only and is not intended to represent an actual waveform.

When used, de-emphasis shapes the transmitter signal to mitigate dielectric and skin-effect distortion and loss. This results in a higher quality waveform at the receiving end.

Note: It is a misconception that the signal is boosted when being shaped by de-emphasis. Instead, the signal is damped.

5.3.3 SLEW RATE CONTROL

The OB slew rate is controlled by two configuration settings: (a) SD10G65::SD10G65_OB_CFG1.PREDRV_C_CTRL controls the C part and (b) SD10G65::SD10G65_OB_CFG1.PREDRV_R_CTRL controls the R part of the encoding.

The slew rate is adjustable using the following control settings:

- C = 3, R = 3: 25 ps (default setting)
- C = 3, R = 0: 35 ps
- C = 0, R = 3: 55 ps
- C = 1, R = 0: 70 ps
- C = 0, R = 0: 120 ps

5.3.4 TX AND RX POLARITY INVERSION (P AND N SWAP)

The data streams in the Tx and Rx direction can be inverted by:

- XFI_MODE.TX_INVERT. Invert data received from the SerDes macro.
- XFI_MODE.RX_INVERT. Invert data into the SerDes macro.

This allows for swapping the P and N lines of the high-speed serial link to ease the layout process.

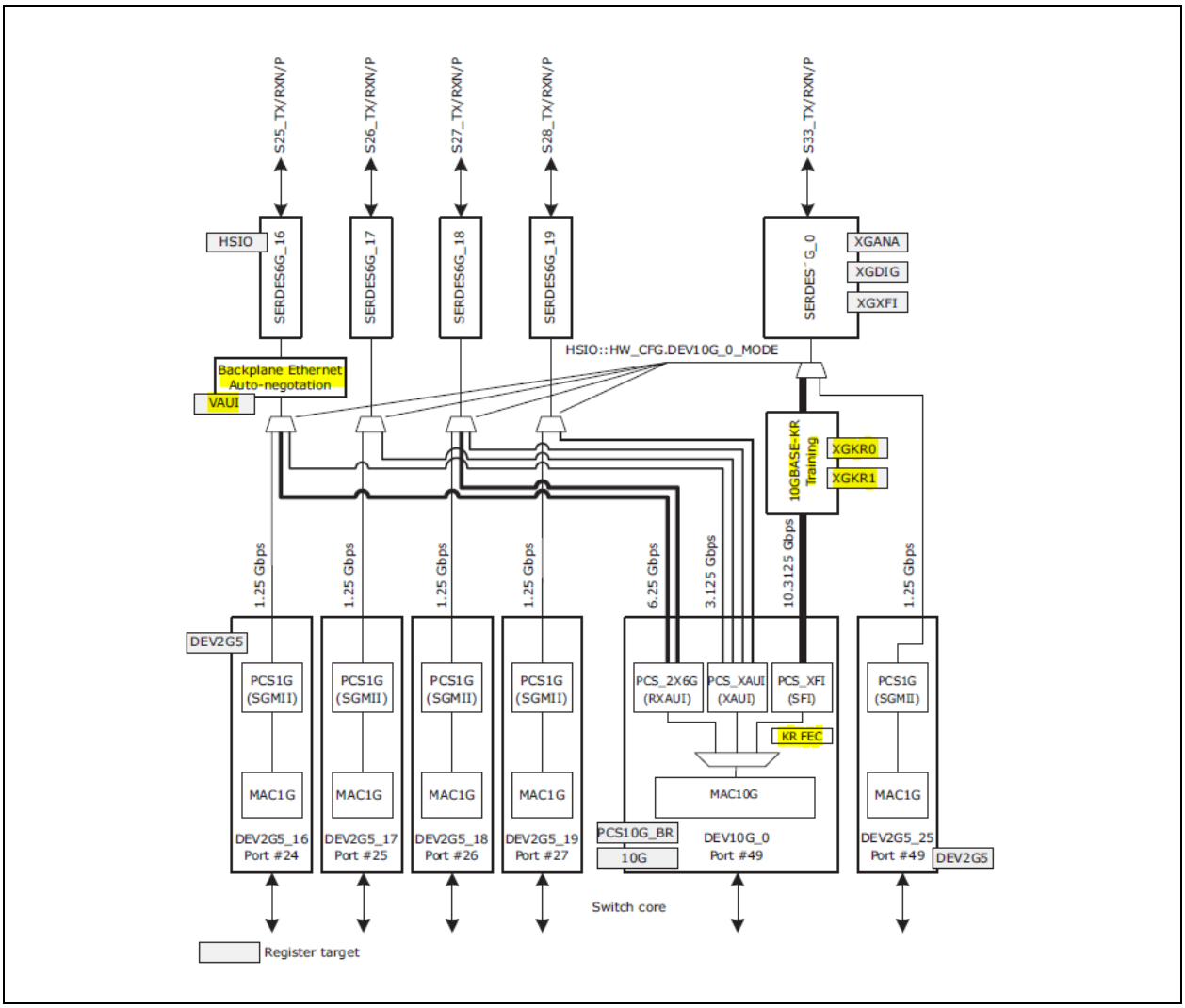
5.3.5 10G KR AUTO-NEGOTIATION, TRAINING AND FEC

The 10G XFI/SFI ports support backplane operation, that is:

- 10GBASE-KR Auto-negotiation: For negotiating between 1000BASE-KX (1 Gbps Ethernet) and 10GBASE-KR (10 Gbps Ethernet) PHY types per Clause 73 of the IEEE 802.3ap-2007
- KR Link training: To automatically configure the remote link partner transmitter physical media driver (PMD) for the lowest bit error rate (BER) per Clause 72 of IEEE 802.3ap-2007
- Forward error correction (FEC): To minimize retransmission in accordance to IEEE 802.3 and 802.3ba Clause 74

Additionally, the XAUI ports support 10GBASE-KX4 Auto-negotiation. Each of the 16 associated lanes supports running 1000BASE-KX ANEG (only auto-negotiation, no training).

FIGURE 5-4: 10G PORT MULTIPLEXING IN JAGUAR-2 SWITCH ARCHITECTURE



5.3.6 SERDES10G OUTPUT BUFFER TEST

All 10G SerDes macro settings can be changed manually using the symbolic register read/write debug command.

```
// Readout all output buffer settings for the first 10G port
# platform debug allow
# debug sym read xgana[0]::sd10g65_ob_cfg*
Register                              Value
XGANA[0]:SD10G65_OB:SD10G65_OB_CFG0 0x00002187
XGANA[0]:SD10G65_OB:SD10G65_OB_CFG1 0x042f0820
XGANA[0]:SD10G65_OB:SD10G65_OB_CFG2 0x007df820
XGANA[0]:SD10G65_OB:SD10G65_OB_CFG3 0x00002000

// Change De-emphasis level to 3dB
# debug sym write xgana[0]::sd10g65_ob_cfg2 0x5DF828
Register                    Value
XGANA[0]:SD10G65_OB:SD10G65_OB_CFG2 0x5DF828
#
```

5.3.7 1000BASE-KX ANEG TEST

The following test uses two of the upper 8x SFP ports on a Jaguar-2 reference board, VSC5628EV. These eight ports are controlled by VAUI0. (The other eight ports, controlled by VAUI1, are not accessible as SFP ports, unless using a Xenpak-to-SFP adapter PCB080, but is used as XAUI0 and XAUI1 lanes on the VSC5628EV.)

SerDes ports S17 and S18 are connected to each other using DAC cabling (that is, internal port 16 and 17, DEV2G5[8:9].) These two ports are the first instances in the VAUI0:ANEG block.

```
// First disable Clause 37 - normally speed is set to Auto, that is 1000Base-X ANEG
# configure terminal
(config)# interface GigabitEtherne 1/13-14
(config-if)# speed 1000                          <- change to 1000Base-X wo/ANEG
(config-if)# end

// See new link status
# show interface GigabitEthernet 1/13-14 status
Interface             Mode     Speed&Duplex  FlowControl  MaxFrame  Excessive Link
--------------------  -------  ------------  -----------  --------  --------- -----
GigabitEthernet 1/13  enabled  1Gfdx         disabled     10240     Discard   1Gfdx
GigabitEthernet 1/14  enabled  1Gfdx         disabled     10240     Discard   1Gfdx

// See current Clause 73 ANEG advertising settings for the two ports
# platform debug allow
# debug sym read vaui0:aneg_cfg[0-1]
Register                              Value
VAUI0:ANEG_CFG[0]:ANEG_CFG            0x00001500
VAUI0:ANEG_CFG[0]:ANEG_ADV_ABILITY_0 0x00210001  <- default advertising 1000Base-KX
VAUI0:ANEG_CFG[0]:ANEG_ADV_ABILITY_1 0x00000000
VAUI0:ANEG_CFG[0]:ANEG_NEXT_PAGE_0    0x00000000
VAUI0:ANEG_CFG[0]:ANEG_NEXT_PAGE_1    0x00000000
VAUI0:ANEG_CFG[1]:ANEG_CFG            0x00001500
VAUI0:ANEG_CFG[1]:ANEG_ADV_ABILITY_0 0x00210001
VAUI0:ANEG_CFG[1]:ANEG_ADV_ABILITY_1 0x00000000
VAUI0:ANEG_CFG[1]:ANEG_NEXT_PAGE_0    0x00000000
VAUI0:ANEG_CFG[1]:ANEG_NEXT_PAGE_1    0x00000000

// See current Clause 73 ANEG status for the two ports
# debug sym read vaui0:aneg_status[0-1]
Register                                    Value
VAUI0:ANEG_STATUS[0]:ANEG_LP_ADV_ABILITY_0 0x00000000
VAUI0:ANEG_STATUS[0]:ANEG_LP_ADV_ABILITY_1 0x00000000
VAUI0:ANEG_STATUS[0]:ANEG_STATUS           0x00000000
VAUI0:ANEG_STATUS[1]:ANEG_LP_ADV_ABILITY_0 0x00000000
VAUI0:ANEG_STATUS[1]:ANEG_LP_ADV_ABILITY_1 0x00000000
VAUI0:ANEG_STATUS[1]:ANEG_STATUS           0x00000000

// (Re)Start ANEG on the two ports featuring Clause 73 ANEG
# debug sym write vaui0:aneg_cfg[0-1]:aneg_cfg 0x1503
Register                    Value
VAUI0:ANEG_CFG[0]:ANEG_CFG 0x00001503
VAUI0:ANEG_CFG[1]:ANEG_CFG 0x00001503

// See new link partner advertisement; 1GKX, ANEG was acknowledge by link partner
// ANEG status; Link control for 1G enabled, ANEG_GOOD state, ANEG completed
# debug sym read vaui0:aneg_status[0-1]
Register                                    Value
VAUI0:ANEG_STATUS[0]:ANEG_LP_ADV_ABILITY_0 0x00354141
VAUI0:ANEG_STATUS[0]:ANEG_LP_ADV_ABILITY_1 0x00000000
VAUI0:ANEG_STATUS[0]:ANEG_STATUS           0x0400060b
VAUI0:ANEG_STATUS[1]:ANEG_LP_ADV_ABILITY_0 0x002a42a1
VAUI0:ANEG_STATUS[1]:ANEG_LP_ADV_ABILITY_1 0x00000000
VAUI0:ANEG_STATUS[1]:ANEG_STATUS           0x0400060b
#
```

5.3.8 10GBASE-KR TEST

In the following tests, 10G port 1/1 and 1/2 are interconnected using a 2m DAC SFP+, and 10G port 1/3 and 1/4 with 5m DAC SFP+ cabling on a Jaguar-2 reference board, VSC5628EV.

```
// Show initial linkup status and De-emphasis settings with KR disabled
# show interface 10GigabitEthernet * status
Interface              Mode     Speed&Duplex FlowControl MaxFrame  Excessive Link
---------------------  -------  ------------ ----------- --------  --------- ------
10GigabitEthernet 1/1  enabled  10Gfdx       disabled    10240     Discard   10Gfdx
10GigabitEthernet 1/2  enabled  10Gfdx       disabled    10240     Discard   10Gfdx
10GigabitEthernet 1/3  enabled  10Gfdx       disabled    10240     Discard   10Gfdx
10GigabitEthernet 1/4  enabled  10Gfdx       disabled    10240     Discard   10Gfdx

# show interface 10GigabitEthernet * statistics pac
Interface               Rx Packets          Tx Packets
----------------------  ------------------  ------------------
10GigabitEthernet 1/1   6                   224
10GigabitEthernet 1/2   224                 6
10GigabitEthernet 1/3   6                   224
10GigabitEthernet 1/4   224                 6

# platform debug allow
# debug sym read ::sd10g65_ob_cfg2
Register                  Value
XGANA[0]::SD10G65_OB_CFG2 0x007df820
XGANA[1]::SD10G65_OB_CFG2 0x007df820
XGANA[2]::SD10G65_OB_CFG2 0x007df820
XGANA[3]::SD10G65_OB_CFG2 0x007df820
#
// Show initial Equalizer APC (Automatic Parameter Control) status with KR disabled
# debug api cil port in 10g 1/1
Chip Interface Layer[0]
=======================

Port
----
Port 49 (24)                 Tgt   Addr    Hex
PCS_EXT_CFG_49               0x39  0x0040: 0x00000000
PCS_CFG_49                   0x39  0x003f: 0x00000000
PCS_SD_CFG_49                0x39  0x0041: 0x00000011
PCS_XAUI_RX_STATUS_49        0x39  0x0046: 0x00000000
PCS_XAUI_RX_ERROR_STATUS_49  0x39  0x0049: 0x00000000
MAC_TX_MONITOR_STICKY_49     0x39  0x000c: 0x00000002
MAC_ENA_CFG_49               0x39  0x0000: 0x00000011
MAC_MODE_CFG_49              0x39  0x0001: 0x00000000
RX_PAUSE_CFG_49              0x05  0x0180: 0x00000000
ETH_FC_CFG_49                0x05  0x01b7: 0x00000001

APC status:
port    gain   g.adj   ldlev  offs    agc     c     l     dfe1   dfe2   dfe3   dfe4
49      0      43      24     514     124     15    31     78     21     11     15
50      0      53      24     514     119     15    29     69     23     11     14
51      0      47      24     493     103     12    25     76     24     12     14
52      0      38      24     524     103     12    25     65     27     11     14

Link status (MAC/SD/PCS):
port     local_fault   remote_fault  idle_state    SD       rx_blk_lock   rx_hi_ber
49       0             0             1             1        1             0
50       0             0             1             1        1             0
51       0             0             1             1        1             0
52       0             0             1             1        1             0
```

```
// Enable KR ANEG and training (and FEC) manually on the 4x 10G ports
// all=Advertise all, fec-abil=Advertise FEC ability, fec-req=Request FEC ability
# configure terminal
(config)# interface 10g *
(config-if)# debug kr-aneg all fec-abil fec-req
(config-if)# debug kr-status
Port 25
LP aneg ability                 :Yes
Aneg active (running)           :No
PCS block lock                  :Yes
Aneg complete                   :Yes
  Enable 10G request            :No
  Enable 1G request             :No
  FEC change request            :No
Training complete (BER method)  :Yes
  CM OB tap (7-bit signed)      :-2 (126)
  CP OB tap (7-bit signed)      :-5 (123)
  C0 OB tap (7-bit signed)      :+23 (23)
FEC                             :Enabled
  Corrected block count         :0
  Un-corrected block count      :0
Port 26
LP aneg ability                 :Yes
Aneg active (running)           :No
PCS block lock                  :Yes
Aneg complete                   :Yes
  Enable 10G request            :No
  Enable 1G request             :No
  FEC change request            :No
Training complete (BER method)  :Yes
  CM OB tap (7-bit signed)      :-2 (126)
  CP OB tap (7-bit signed)      :-4 (124)
  C0 OB tap (7-bit signed)      :+24 (24)
FEC                             :Enabled
  Corrected block count         :0
  Un-corrected block count      :0
Port 27
LP aneg ability                 :Yes
Aneg active (running)           :No
PCS block lock                  :Yes
Aneg complete                   :Yes
  Enable 10G request            :No
  Enable 1G request             :No
  FEC change request            :No
Training complete (BER method)  :Yes
  CM OB tap (7-bit signed)      :-2 (126)
  CP OB tap (7-bit signed)      :-5 (123)
  C0 OB tap (7-bit signed)      :+23 (23)
FEC                             :Enabled
  Corrected block count         :0
  Un-corrected block count      :0
Port 28
LP aneg ability                 :Yes
Aneg active (running)           :No
PCS block lock                  :Yes
Aneg complete                   :Yes
  Enable 10G request            :No
  Enable 1G request             :No
  FEC change request            :No
Training complete (BER method)  :Yes
  CM OB tap (7-bit signed)      :-2 (126)
  CP OB tap (7-bit signed)      :-2 (126)
  C0 OB tap (7-bit signed)      :+23 (23)
```

```
FEC                             :Enabled
  Corrected block count         :0
  Un-corrected block count      :0
(config-if)# end

// Show linkup status and new De-emphasis settings with KR enabled
# show interface 10GigabitEthernet * status
Interface              Mode     Speed&Duplex FlowControl MaxFrame  Excessive Link
---------------------  -------  ------------ ----------- --------  --------- ------
10GigabitEthernet 1/1  enabled  10Gfdx       disabled    10240     Discard   10Gfdx
10GigabitEthernet 1/2  enabled  10Gfdx       disabled    10240     Discard   10Gfdx
10GigabitEthernet 1/3  enabled  10Gfdx       disabled    10240     Discard   10Gfdx
10GigabitEthernet 1/4  enabled  10Gfdx       disabled    10240     Discard   10Gfdx

# show interface 10GigabitEthernet * statistics pac
Interface              Rx Packets          Tx Packets
---------------------  ------------------  ------------------
10GigabitEthernet 1/1  18                  1066
10GigabitEthernet 1/2  1066                18
10GigabitEthernet 1/3  18                  1066
10GigabitEthernet 1/4  1066                18

# debug sym read ::sd10g65_ob_cfg2
Register                  Value
XGANA[0]::SD10G65_OB_CFG2 0x0051e9b0
XGANA[1]::SD10G65_OB_CFG2 0x0059e9ae
XGANA[2]::SD10G65_OB_CFG2 0x0051e9b0
XGANA[3]::SD10G65_OB_CFG2 0x005dba6d
#

// Show APC status with KR enabled
# deb api cil port in 10g 1/1
Chip Interface Layer[0]
=======================

Port
----
Port 49 (24)                Tgt   Addr    31    24.23    16.15     8.7      0 Hex
PCS_EXT_CFG_49              0x39  0x0040: 0x00000000
PCS_CFG_49                  0x39  0x003f: 0x00000000
PCS_SD_CFG_49               0x39  0x0041: 0x00000011
PCS_XAUI_RX_STATUS_49       0x39  0x0046: 0x00000000
PCS_XAUI_RX_ERROR_STATUS_49 0x39  0x0049: 0x00000000
MAC_TX_MONITOR_STICKY_49    0x39  0x000c: 0x00000002
MAC_ENA_CFG_49              0x39  0x0000: 0x00000011
MAC_MODE_CFG_49             0x39  0x0001: 0x00000000
RX_PAUSE_CFG_49             0x05  0x0180: 0x00000000
ETH_FC_CFG_49               0x05  0x01b7: 0x00000001

APC status:
port    gain    g.adj   ldlev  offs    agc     c     l     dfe1   dfe2   dfe3   dfe4
49      65      48      24     515     128     16    32     84     16     11     14
50      137     56      24     515     120     15    30     67     19     9      12
51      29      70      24     497     100     12    25     67     24     11     14
52      113     52      24     525     98      12    24     62     26     10     12

Link status (MAC/SD/PCS):
port     local_fault   remote_fault  idle_state    SD       rx_blk_lock   rx_hi_ber
49       0             0             1             1        1             0
50       0             0             1             1        1             0
51       0             0             1             1        1             0
52       0             0             1             1        1             0
#
```

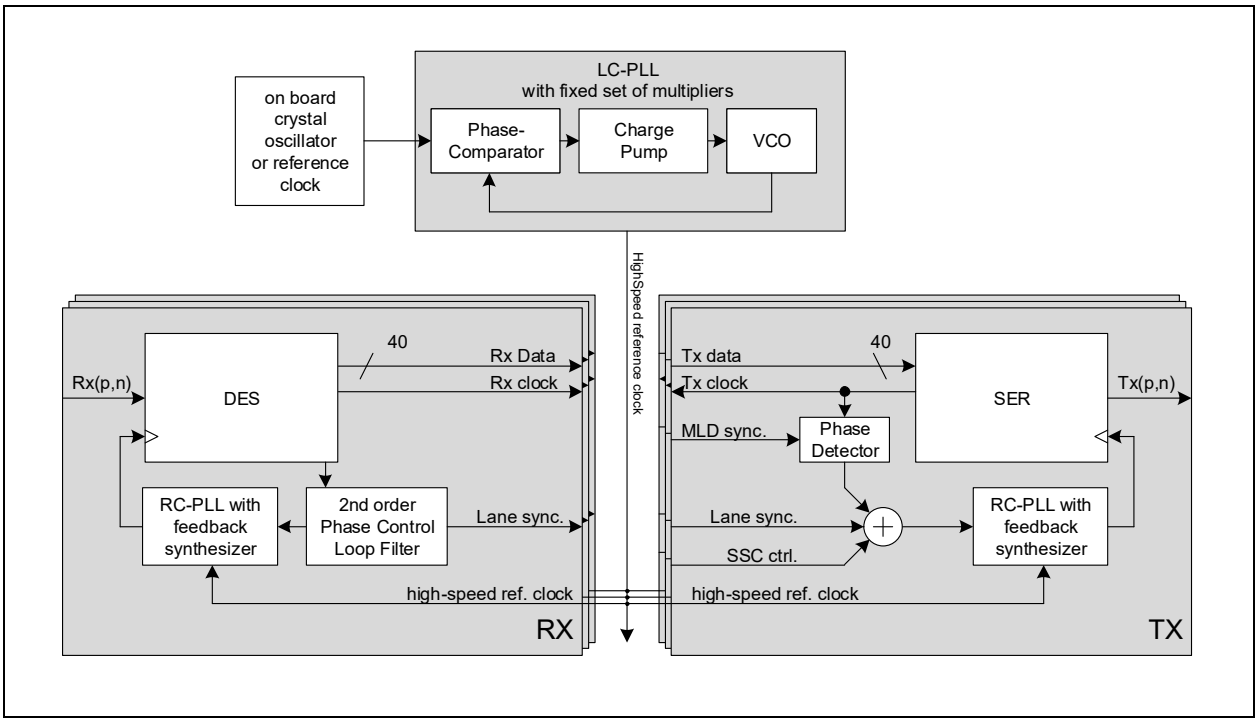
```
// When testing, it is desired, that counters only count test transmitted frames.
// So isolate the 10G ports from other Switch ports and each other.
// Stop protocols that are transmitting BPDU's.
# configure terminal
(config)# interface 10GigabitEthernet *
(config-if)# no pvlan 1
(config-if)# pvlan 2
(config-if)# pvlan isolation
(config-if)# no spanning-tree
(config-if)# no lldp transmit
(config-if)# end

// Send frames between the 10G ports
# clear statistics *
# debug frame tx-cnt 10000
# debug frame tx interface 10GigabitEthernet * packet-length 1234
Transmitting 10000 frames...Done in 20.367 seconds.

# show interface 10GigabitEthernet * statistics pac
Interface               Rx Packets          Tx Packets
----------------------  ------------------  ------------------
10GigabitEthernet 1/1   10000               10000
10GigabitEthernet 1/2   10000               10000
10GigabitEthernet 1/3   10000               10000
10GigabitEthernet 1/4   10000               10000

# show in 10GigabitEthernet 1/1 statistics
10GigabitEthernet 1/1 Statistics:
Rx Packets:                      10000   Tx Packets:                      10000
Rx Octets:                    12380000   Tx Octets:                    12380000
Rx Unicast:                          0   Tx Unicast:                          0
Rx Multicast:                        0   Tx Multicast:                        0
Rx Broadcast:                    10000   Tx Broadcast:                    10000
Rx Pause:                            0   Tx Pause:                            0

Rx 64:                               0   Tx 64:                               0
Rx 65-127:                           0   Tx 65-127:                           0
Rx 128-255:                          0   Tx 128-255:                          0
Rx 256-511:                          0   Tx 256-511:                          0
Rx 512-1023:                         0   Tx 512-1023:                         0
Rx 1024-1526:                    10000   Tx 1024-1526:                    10000
Rx 1527-    :                        0   Tx 1527-    :                        0

Rx Priority 0:                   10000   Tx Priority 0:                       0
Rx Priority 1:                       0   Tx Priority 1:                       0
Rx Priority 2:                       0   Tx Priority 2:                       0
Rx Priority 3:                       0   Tx Priority 3:                       0
Rx Priority 4:                       0   Tx Priority 4:                       0
Rx Priority 5:                       0   Tx Priority 5:                       0
Rx Priority 6:                       0   Tx Priority 6:                       0
Rx Priority 7:                       0   Tx Priority 7:                   10000

Rx Drops:                            0   Tx Drops:                            0
Rx CRC/Alignment:                    0   Tx Late/Exc. Coll.:                  0
Rx Undersize:                        0
Rx Oversize:                         0
Rx Fragments:                        0
Rx Jabbers:                          0
Rx Filtered:                         0
#
```

6.0 LC-PLL AND RC-PLL: VSC CLOCKING CONCEPT

The VSC switches and 10G PHYs operate under the following clocking concept.

From an external reference clock that is selectable over a wide range, one central LC-PLL generates an internal high-speed reference clock, which is distributed to up to 64 SerDes lanes (receiver and transmitter).

FIGURE 6-1: VSC CLOCKING CONCEPT



In each SerDes transmitter and receiver, an RC-Phase-Locked-Loop (RC-PLL) (with feedback synthesizer) can individually support any desired Tx baud rate, and likewise high-resolution phase rotators are used for the purpose of Rx baud rate adaptation.

Note:	The VSC devices might have more than one LC-PLL for other purposes (for example, to separate SyncE (SerDes) and IEEE 1588 timing by clocking the VCORE (CPU) separately, or to have separate clock domains in PHYs on the MAC side and Media side).

6.1 LC-PLL Recalibration

The LC-PLL performs initial calibration at power-up, *independent of the HW-RESET to the chip*. If a valid input clock is not present when the LC-PLL is performing this calibration, it can result in a bad operation point of the LC-PLL.

To recalibrate the LC-PLL manually, it is recommended to toggle-restart its state machine:

PLL5G_CFG2.DISABLE_FSM (0 to 1 to 0) (The recalibration time takes around 1 ms.)

Four status fields can be checked to verify if the LC-PLL has locked to the reference clock:

- PLL5G-STATUS0.LOCK_STATUS = 1
- PLL5G-STATUS1.FSM_LOCK = 1
- PLL5G-STATUS1.FSM_STAT = 6
- PLL5G-STATUS1.GAIN_STAT >= 2

Reading a GAIN_STAT value less than 2 (normally 0) would mean a HW failure or OSC not present, as the hardware design should ensure that the reference clock input has a valid and stable frequency.

As mentioned, the LC-PLL state machine is doing initial ramp-up already during power-up and is not influenced by the HW RESET pin. At power-up, the external reference oscillator also ramps-up the frequency, and that might last longer (10-20 ms) than the PLL5G state machine ramp-up (1 ms). So, it is possible that the PLL5G state machine falsely detects the target frequency, but at a too low frequency (coming from the ramping oscillator), and closes the loop.

Therefore, the VSC software always performs an LC-PLL recalibration during boot-up as a precaution to avoid having the PLL to lock to a wrong frequency at power-up. The issue seldom occurs, but in principle there is no negative effect of doing an initial recalibration, and the reference clock is then expected to be up and running.

The LC-PLL state machine restarts automatically when it detects that the frequency variation between the reference clock and the VCO clock is higher than a certain limit. However, although the frequency is within this limit, the closed loop PLL may lose a clock cycle and jitter may increased significantly.

6.1.1 RECALIBRATE LC-PLL ON VSC7514 TEST

Note: The following test is made on the VSC7514EV board. Recalibration is normally part of the switch initialization.

```
// Get current status - just to show the values, before doing manual re-calibration
# platform debug allow
# deb sym read ::pll5g_status*
Register            Value
HSIO::PLL5G_STATUS0 0x00000001
HSIO::PLL5G_STATUS1 0x1fe83ffd

// Read current configuration value
# deb sym read ::pll5g_cfg2
Register                  Value
HSIO:PLL5G_CFG:PLL5G_CFG2 0x00106114

//Disable FSM
# deb sym write ::pll5g_cfg2 0x00106116
Register                  Value
HSIO:PLL5G_CFG:PLL5G_CFG2 0x00106116

//Enable FSM
# deb sym write ::pll5g_cfg2 0x00106114
Register                  Value
HSIO:PLL5G_CFG:PLL5G_CFG2 0x00106114

//Get new status
# deb sym read ::pll5g_status*
Register            Value
HSIO::PLL5G_STATUS0 0x00000001
HSIO::PLL5G_STATUS1 0x1fe83ffd
```

6.1.2 RECALIBRATE HOST LC-PLL ON VSC8490

Note: The following test is done on VSC8490 using the XAUI-to-SFP+ add-on attached to a VSC5628EV. Recalibration is normally part of the PHY setup, phy_10g_mode_conf_set.

To perform the recalibration, perform the following steps:

1. Read `0x1e 0x8104`.
2. Write `0x1e 0x8104`, change bit 1 from `0` to `1` to disable FSM.
3. Write `0x1e 0x8104`, change bit 1 from `1` back to `0` to enable FSM.
4. Wait 1 ms.
5. Read `0x1e 0x810d`, expect bit 0 = `1`.
6. Read `0x1e 0x810e`, expect bit 3:1 to be `6`.
7. Read `0x1e 0x810f`, expect bit 4:0 to be normally around `8` (6 to 10 is valid).
8. Repeat from step 2 until lock has been acquired.

To get a general status dump, perform the following steps:

1. Read `0x4 0xE634/0xE63B/0xE642/0xE649` for lane 0, 1, 2, 3, expect bit 12, 11 to be `0` (RC).
2. Read `0x1e 0x810E`, expect bit 3:1 to be `6` in decimal (host LC-PLL status).
3. Read `0x1e 0x8211`, expect bit 3:1 to be `6` in decimal (line LC-PLL status).

Note: Always use channel 0 when accessing vital parts in VSC8490.

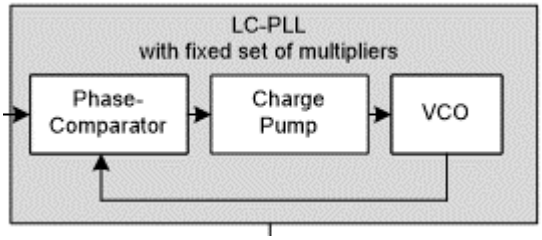
6.1.3 RECALIBRATE HOST LC-PLL TEST

```
// Re-calibrate host LC-PLL from mdio
# configure terminal
# interface 10g 1/1
(config-if)# deb phy mmd read 0x1e 0x0000
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0x0000   0x8490  1000.0100.1001.0000
(config-if)# deb phy mmd read 0x1e 0x8104
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0x8104   0x6014  0110.0000.0001.0100
(config-if)# deb phy mmd write 0x1e 0x8104 0x6016
(config-if)# deb phy mmd write 0x1e 0x8104 0x6014
(config-if)# deb phy mmd read 0x1e 0x810d
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0x810d   0x12a2  0001.0010.1010.0010       ?
(config-if)# deb phy mmd read 0x1e 0x810e
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0x810e   0x3ffd  0011.1111.1111.1101
(config-if)# deb phy mmd read 0x1e 0x810f
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0x810f   0x1fe8  0001.1111.1110.1000

// General status dump
(config-if)# deb phy mmd read 0x4 0xe634
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0xe634   0x0030  0000.0000.0011.0000
(config-if)# deb phy mmd read 0x4 0xe63b
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0xe63b   0x0030  0000.0000.0011.0000
(config-if)# deb phy mmd read 0x4 0xe642
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0xe642   0x0030  0000.0000.0011.0000
(config-if)# deb phy mmd read 0x4 0xe649
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0xe649   0x0030  0000.0000.0011.0000
(config-if)# deb phy mmd read 0x1e 0x8210
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0x8210   0x0001  0000.0000.0000.0001
(config-if)# deb phy mmd read 0x1e 0x8211
ISID  Iport  Addr     Value   15      8 7       0
   1     27  0x8211   0x3ffd  0011.1111.1111.1101
(config-if)# end
```

6.2 LC-PLL GAIN_STAT Variations

During device initialization, the main PLLs (called LC-PLL) are normally recalibrated and checked for having a valid 'gain'. LC-PLL is illustrated in Figure 6-2.

FIGURE 6-2: LC-PLL PLL COMPONENTS

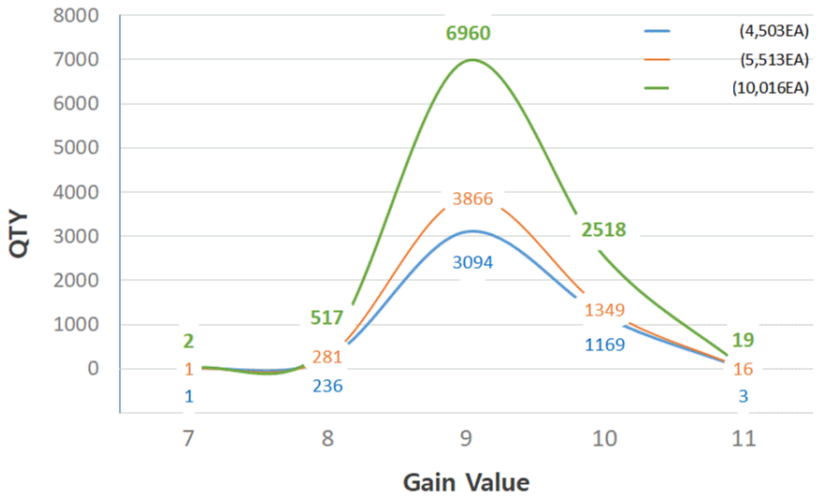


For every change of GAIN_STAT, an internal capacitance is switched on or off from the LC-PLLs VCO input. This results in a small change of the VCO output frequency. Each GAIN_STAT increment or decrement gives a static frequency step in the range of 30-40 MHz, which is related to the 5 GHz of the VCO.

This frequency stepping has been implemented to account for variations across PVT die materials, although that of all the different devices using the LC-PLL implementation, there is only a very minor variation across PVT of around +/-2. The state machine ramps the 'gain' value from 0 to 31 (that is, ramping up the frequency of the VCO) and stops when the frequency is close enough to the target value of 5 GHz. Then, the state machine closes the loop, and the PLL accurately locks to the exact phase of the applied reference clock.

The LC-PLL implementation has evolved over time, for example, by having a finer resolution by adding more and smaller capacitance steps. Therefore, the expected GAIN_STAT value varies across the different VSC switch families. For Jaguar-1/VSC7460, the nominal 'gain' value (that is, closest to the target frequency of 5 GHz) is in the range of 4-6; for Jaguar-2/VSC7468 and Venice/VSC8490, it is in the range of 7-9; and for Ocelot-1/VSC7514, it is in the range of 8-10.

FIGURE 6-3: VSC7514 GAIN_STAT VARIATION OVER 10,000 SAMPLES (TWO PRODUCTION DATES)



In principle, a 'gain' value other than the nominal gain values results in a higher frequency jitter. However, characterization data indicates that the influence of a 'gain' value is 0 to the jitter and to the performance of the SerDes macros.

6.3 Manually Changing GAIN_STAT Value

The GAIN_STAT value can be set manually as long as ENA_GAIN_TEST is set.

Note: This setting survives a reboot but not a power-cycle.

VSC7514

```
# deb sym read ::pll5g_status*
Register            Value
HSIO::PLL5G_STATUS0 0x00000001
HSIO::PLL5G_STATUS1 0x1fe83ffd

//Change GAIN_STAT to 10
# deb sym write ::pll5g_cfg2 0x00106155
Register                  Value
HSIO:PLL5G_CFG:PLL5G_CFG2 0x00106155

# deb sym read ::pll5g_status*
Register            Value
HSIO::PLL5G_STATUS0 0x00000001
HSIO::PLL5G_STATUS1 0x1fea00b0

//Disable forced value
# deb sym write ::pll5g_cfg2 0x00106114
Register                  Value
HSIO:PLL5G_CFG:PLL5G_CFG2 0x00106114

# deb sym read ::pll5g_status*
Register            Value
HSIO::PLL5G_STATUS0 0x00000001
HSIO::PLL5G_STATUS1 0x1fe83ffd
#
```

VSC8490

```
//Read current PLL5G status
# HOST LCPLL status0
deb phy mmd read  0x1e 0x810d >   0x1293
# HOST LCPLL status1A
deb phy mmd read  0x1e 0x810e >   0x000d
# HOST LCPLL status1B
deb phy mmd read  0x1e 0x810f >   0x1fe7

//Change GAIN_STAT to 8 ( ~ +7ppm)
(1 gain step is about 30-40MHz in relation to 5GMhz.)
deb phy mmd read  0x1e 0x8104 >   0x6014
deb phy mmd write 0x1e 0x8104 0x6115
# HOST LCPLL status0
deb phy mmd read  0x1e 0x810d >   0x1293
# HOST LCPLL status1A
deb phy mmd read  0x1e 0x810e >   0x000d
# HOST LCPLL status1B
deb phy mmd read  0x1e 0x810f >   0x1fe8

//Disable forced value
deb phy mmd write 0x1e 0x8104 0x6114
# HOST LCPLL status0
deb phy mmd read  0x1e 0x810d >   0x1293
# HOST LCPLL status1A
deb phy mmd read  0x1e 0x810e >   0x000d
# HOST LCPLL status1B
deb phy mmd read  0x1e 0x810f >   0x1fe7
#
```

7.0 INPUT BUFFER CONTROL

7.1 1G SerDes Input Buffer

The 1G SerDes Input Buffer (IB) provides support for:

- CDR with programmable loop-bandwidth and phase regulation
- Input Buffer signal detect/loss of signal (LOS) options
- Common-mode termination and DC-coupling
- Input Buffer with equalization

7.1.1 CDR PHASE REGULATION LOOP

The Deserializer and the Clock and Data Recovery (CDR) unit includes control logic that interacts with the analog parts within the macro and compensates for the frequency offset between the received data and the internal high-speed reference clock (see Figure 6-1). To obtain good jitter performance, the phase regulation used is a PI-type regulator, with which proportional (P) and integrative (I) characteristics can be set independently.

The integrative part of the phase regulation loop is controlled by the SERDES1G_DES_CFG. DES_PHS_CTRL register field. The limits of the integrator are programmable, allowing different settings for the integrative regulation, while guaranteeing that the proportional part is still stronger than the integrative part. Integrative regulation compensates frequency modulation from DC up to a cut-off frequency. Frequencies above the cut-off frequency are compensated by the proportional part.

The time constant of the integrator is controlled independently of the proportional regulation by SERDES1G_DES_CFG.DES_BW_HYST. The DES_BW_HYST register field is programmable in a range from 3 to 7. The lower the configuration setting, the smaller the time constant of the integrative regulation. For normal operation, configure DES_BW_HYST to 5.

The integrative regulation can compensate a static frequency offset within the programmed limits down to a remaining frequency error of below 4 ppm. In a steady state, the integrator toggles between two values around the exact value, and the proportional part of the phase regulation takes care of the remaining phase error.

The loop bandwidth for the proportional portion of the phase regulation loop is controlled by the SERDES1G_DES_CFG.DES_BW_ANA register field.

The fastest loop bandwidth setting (lowest configuration value) results in a loop bandwidth that is equal to the maximum frequency offset compensation capability. For improved jitter performance, use a setting with sufficient margin to track the expected frequency offset rather than using the maximum frequency offset. For example, if a 100 ppm offset is expected, use a setting that is four times higher than the offset.

The following list provides the limits for the frequency offset compensation. The values are theoretical limits for input signals without jitter, because the actual frequency offset compensation capability is dependent on the toggle rate of the input data and the input jitter. Only the applicable configuration values are listed below.

- DES_BW_ANA = 4; loop bandwidth is 1953 ppm.
- DES_BW_ANA = 5; loop bandwidth is 977 ppm.
- DES_BW_ANA = 6; loop bandwidth is 488 ppm.
- DES_BW_ANA = 7; loop bandwidth is 244 ppm.

After a reset of the SerDes macro, the phase regulation may be 180° out of phase compared to the incoming data, resulting in a deadlock condition at the sampling stage of the Deserializer. To prevent this situation, the 1G SerDes provides a 180° deadlock protection mechanism through the SERDES1G_DES_CFG.DES_MBTR_CTRL register field. If the deadlock protection mechanism is enabled, a small frequency offset is applied to the phase regulation loop. The offset is sufficient to move the sampling point out of the 180° deadlock region, while at the same time, small enough to allow the regulation loop to compensate, when the sample point is within the data eye.

7.1.2 SIGNAL DETECTION

The 1G SerDes IB provides an option to configure the threshold level of the signal detect circuit to adapt to different input amplitudes. The signal detect circuit can be configured by SERDES1G_IB_CFG.IB_ENA_DETLEV and SERDES1G_IB_CFG.IB_DET_LEV.

The signal detect circuitry generates a pulse for every recognized signal activity on the input. This sequence of pulses is compared to internal clock pulses. Whenever the number of signal pulses exceeds the number of the clock pulses, the signal detect bit is set. This means that for slow input signals a divider setting is required. For 100BASE-FX set SERDES1G_IB_CFG.IB_FX100_ENA.

7.1.3 COMMON-MODE TERMINATION AND DC-COUPLING

The Common-Mode Voltage (CMV) input termination can either be set to an internal reference voltage 0.7*Vdda or to Vdda. SERDES1G_IB_CFG.IB_ENA_CMV_TERM controls the CMV input termination, and SERDES1G_IB_CFG.IB_ENA_DC_COUPLING controls internal DC-coupling mode.

The following modes are defined by CMV input termination and DC-coupling:

TABLE 7-1: 1G SERDES TERMINATION MODES

CMV_TERM	DC_COUPLING	Description
0	0	VSC-mode, DC coupling between two VSC devices
1	0	SGMII compliant mode with external AC coupling
1	1	100BASE-FX low frequency mode

7.1.4 1G SERDES EQUALIZATION

The 1G SerDes macro offers options to compensate for channel loss. Degraded signals can be equalized, and the corner frequency of the equalization filter can be adapted to the channel behavior. The equalization settings are configured by SERDES1G_IB_CFG.IB_EQ_GAIN and SERDES1G_IB_CFG. IB_CORNER_FREQ.

The 1G SerDes macro can compensate for possible DC offset, which can distort the received input signal, by enabling SERDES1G_IB_CFG.IB_ENA_OFFSET_COMP during normal reception.

The 1G SerDes maco supports input hysteresis, which is required for some standards (SGMII). The hysteresis function is enabled by SERDES1G_IB_CFG.IB_ENA_HYST, and hysteresis levels are defined by SERDES1G_IB_CFG.IB_HYST_LEV.

Note: Hysteresis and DC-offset compensation cannot be enabled at the same time.

7.2 6G SerDes Input Buffer

The 6G SerDes Input Buffer provides support for:

- RC-PLL baud rate support, configurable from 1 Gbps to 3.75 Gbps
- CDR with programmable loop-bandwidth and phase regulation
- High precision signal detect functionality
- Silicon process variation compensation
- Automatic data independent input voltage offset compensation
- Continuous automatic adaptive equalization

7.2.1 RC-PLL BAUD RATE SUPPORT

The 6G SerDes IB has been designed to recover data signals at different baud rates. To operate at the correct frequency, the RC-PLL must be configured to the appropriate reference point in PLL_CTRL_DATA. The RC-PLL calibration is enabled through SERDES6G_PLL_CFG.PLL_FSM_ENA, and the RC-PLL reference point and phase rotator must be set based on Table 7-2.

TABLE 7-2: RC-PLL SETTINGS ON DIFFERENT SPEEDS

Configuration register	1G SGMII	2.5G or XAUI	5G QSGMII	6.25G RXAUI
SERDES6G_PLL_CFG.PLL_FSM_CTRL_DATA	60/0x3C	48/0x30	120/0x78	96/0x60
SERDES6G_PLL_CFG.PLL_ROT_FRQ	0	1	0	1
SERDES6G_PLL_CFG.PLL_ENA_ROT	0	1	0	1
SERDES6G_PLL_COMMON_CFG.QRATE	1	0	0	0
SERDES6G_PLL_COMMON_CFG.HRATE	0	1	0	0

7.2.2 RC-PLL STATUS: CLOCK PERIOD MEASUREMENT TEST

The SerDes6G IB CDR or clock recovering unit (CRU) is used to extract the remote end transmission clock from the incoming bitstream. The clock is being used for sampling the data bits, preferably in the 'middle' of the eye. The SerDes6G IB CDR uses the RC-PLL to recover the clock.

The SerDes6G_PLL_STATUS provides information about the current calibration status and a read-back of calibration settings or measured period through SERDES6G_PLL_STATUS.PLL_RB_DATA. Selection of what to read back is done from SERDES6G_PLL_CFG.PLL_RB_DATA_SEL.

The measured period should match the settings in the SERDES6G_PLL_CFG.PLL_FSM_CTRL_DATA. The following test is done on VSC8490 XAUI interface (channel 0).

```
// (default) Read measured period for each XAUI lane
> read 0x4 0xe634 : 0x002f  0000.0000.0010.1111  <- 0x2f is also fine
> read 0x4 0xe63b : 0x0030  0000.0000.0011.0000
> read 0x4 0xe642 : 0x0030  0000.0000.0011.0000
> read 0x4 0xe649 : 0x0030  0000.0000.0011.0000
// Change read-out to PLL calibration settings
> read 0x4 0xe62c : 0x3082  0011.0000.1000.0010
> write 0x4 0xe62c 0x308a

// Read calibration setting for each XAUI lane
> read 0x4 0xe634 : 0x0097  0000.0000.1001.0111
> read 0x4 0xe63b : 0x0097  0000.0000.1001.0111
> read 0x4 0xe642 : 0x0097  0000.0000.1001.0111
> read 0x4 0xe649 : 0x0097  0000.0000.1001.0111

// Change back read-out to measured period for each XAUI lane
> write 0x4 0xe62c 0x3082

// Read measured period for each XAUI lane
> read 0x4 0xe634 : 0x002f  0000.0000.0010.1111
> read 0x4 0xe63b : 0x0030  0000.0000.0011.0000
> read 0x4 0xe642 : 0x0030  0000.0000.0011.0000
> read 0x4 0xe649 : 0x0030  0000.0000.0011.0000
```

7.2.3 CDR PHASE REGULATION LOOP

The Deserializer and the CDR unit includes a control logic that interacts with the analog parts within the macro and compensates for the frequency offset between the received data and the internal high-speed reference clock (see Figure 6-1). To obtain good jitter performance, the phase regulation used is a PI-type regulator, with which proportional (P) and integrative (I) characteristics can be set independently.

The phase regulation loop integrative part is controlled by SERDES6G_DES_CFG.DES_PHS_CTRL. The limits of the integrator are programmable, allowing different settings for the integrative regulation, while guaranteeing that the proportional part is still stronger than the integrative part.

The integrator time constant is controlled independently of the proportional regulation by SERDES6G_DES_CFG.DES_BW_HYST, which is programmable in a range from 3 to 7 in Full Rate mode, and 1 to 7 in Quarter Rate mode. The lower the configuration setting, the smaller the time constant of the integrative regulation. For normal operation, configure DES_BW_HYST to 5.

The integrative regulation can compensate a static frequency offset within the programmed limits down to a remaining frequency error of below 4 ppm. In a steady state, the integrator toggles between two values around the exact value, and the proportional part of the phase regulation takes care of the remaining phase error.

The loop bandwidth for the proportional portion of the phase regulation loop is controlled by SERDES6G_DES_CFG.DES_BW_ANA. The fastest loop bandwidth setting (lowest configuration value) results in a loop bandwidth that is equal to the maximum frequency offset compensation capability. For improved jitter performance, use a setting with sufficient margin to track the expected frequency offset rather than using the maximum frequency offset. For example, if a 200 ppm offset is expected, use a setting that is four times higher than the offset.

Table 7-3 provides the limits for the frequency offset compensation. The values are theoretical limits for input signals without jitter, because the actual frequency offset compensation capability is dependent on the toggle rate of the input data and the input jitter. Only applicable configuration values are listed.

TABLE 7-3: 6G FREQUENCY OFFSET COMPENSATION CAPABILITY

DES_BW_ANA	Full rate RXAUI (HRATE = 0, QRATE = 0)	Half rate XAUI (HRATE = 1, QRATE = 0)	Quarter rate SGMII (HRATE = 0, QRATE = 1)
2	—	—	1953 ppm
3	—	1953 ppm	**977 ppm**
4	1953 ppm	**977 ppm**	488 ppm
5	**977 ppm**	488 ppm	244 ppm
6	488 ppm	244 ppm	122 ppm
7	244 ppm	122 ppm	61 ppm

After a reset of the 6G SerDes macro, the phase regulation may be 180° out of phase compared to the incoming data, resulting in a deadlock condition in the Deserializer sampling stage. To prevent this situation, the 6G SerDes provides a 180° deadlock protection mechanism through the SERDES6G_DES_CFG.DES_MBTR_CTRL register field. If the deadlock protection mechanism is enabled, a small frequency offset is applied to the phase regulation loop. The offset is sufficient to move the sampling point out of the 180° deadlock region, while at the same time, small enough to allow the regulation loop to compensate, when the sample point is within the data eye.

7.2.4 SIGNAL DETECTION

The 6G SerDes IB provides an option to configure the threshold level of the signal detect circuit in steps of 20 mV to adapt to different input amplitudes. The signal detect circuit is enabled by SERDES6G_IB_CFG.IB_SIG_DET_ENA and level set in SERDES6G_IB_CFG1.IB_TSDET.

The signal detection circuitry generates a pulse for every recognized signal activity on the input. This sequence of pulses is compared to an internal clock. Whenever the number of signal pulses exceeds the number of the clock pulses, the Signal Detect bit is set. This means that for slow input signals like 1000BASE-FX, a divider setting is required. The internal 125 MHz clock can be divided down to 1 MHz by setting SERDES6G_IB_CFG.IB_SIG_DET_CLK_SEL. Note that a slow clock selection will increase the delay between signal recognition and update of the status register.

The Signal Detect information is normally passed directly to the PCS layer. It is possible to enable a hysteresis, such that the Signal Detect condition must be active or inactive for a certain time before it is signaled to the PCS layer. The Signal Detect assertion time (the time signal detect must be active before the information is passed to the PCS) can be set in SERDES6G_DIG_CFG. SIGDET_AST. The deassertion time (the time signal detect must be inactive before the information is passed to the PCS) is set in SERDES6G_DIG_CFG.SIGDET_DST.

7.2.5 CHANGE SIGNAL DETECTION THRESHOLD TEST

```
// Readout current settings from 6G SerDes macro #0 (internal port 9)
# deb sym write ::mcb_serdes6g_addr_cfg 0x40000001
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x40000001

// Read current ib_tsdet value
# deb sym read  ::serdes6g_ib_cfg1
HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG1 0x00103ff0

// Increase signal detect threshold to 100mV
# deb sym write  ::serdes6g_ib_cfg1 0x00104ff0
HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG1 0x00104ff0

// Update 6G SerDes macro #0 (internal port 9)
# deb sym write ::mcb_serdes6g_addr_cfg 0x80000001
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x80000001
#
```

7.2.6 COMMON-MODE TERMINATION AND DC-COUPLING

The IB is normally AC-coupled, and thus the CMV input termination is switched off. To support type-2 loads (DC-coupling at 1.0V termination voltage) according to the OIF CEI specifications, common-mode termination must be enabled. SERDES6G_IB_CFG.IB_TERM_MODE_SEL controls the CMV input termination. The following modes defines the CMV input termination and DC-coupling:

TABLE 7-4: 6G SERDES TERMINATION MODES

IB_TERM_MODE_SEL	Selected common-mode termination voltage
0	Open (VSC mode). DC coupling between two VSC devices.
1	0.7*Vdda. SGMII-compliant mode with external AC coupling.
2	Vdda. Increase amplitude in certain DC-coupled modes (OIF CEI specification).
3	Capacitance only - reserved for debug test purpose

7.2.7 OFFSET CALIBRATION

For asymmetrical data eyes, as they occur for example on optical channels, a non-zero offset can be selected. The offset value is controlled by setting SERDES6G_IB_CFG2.ib_ocals. The value ranges from 0 to 63 and corresponds setting the offset between –70 mV and 70 mV. Default setting is 32, which is 0V. The setting will first be applied when the automatic calibration procedure has been restarted.

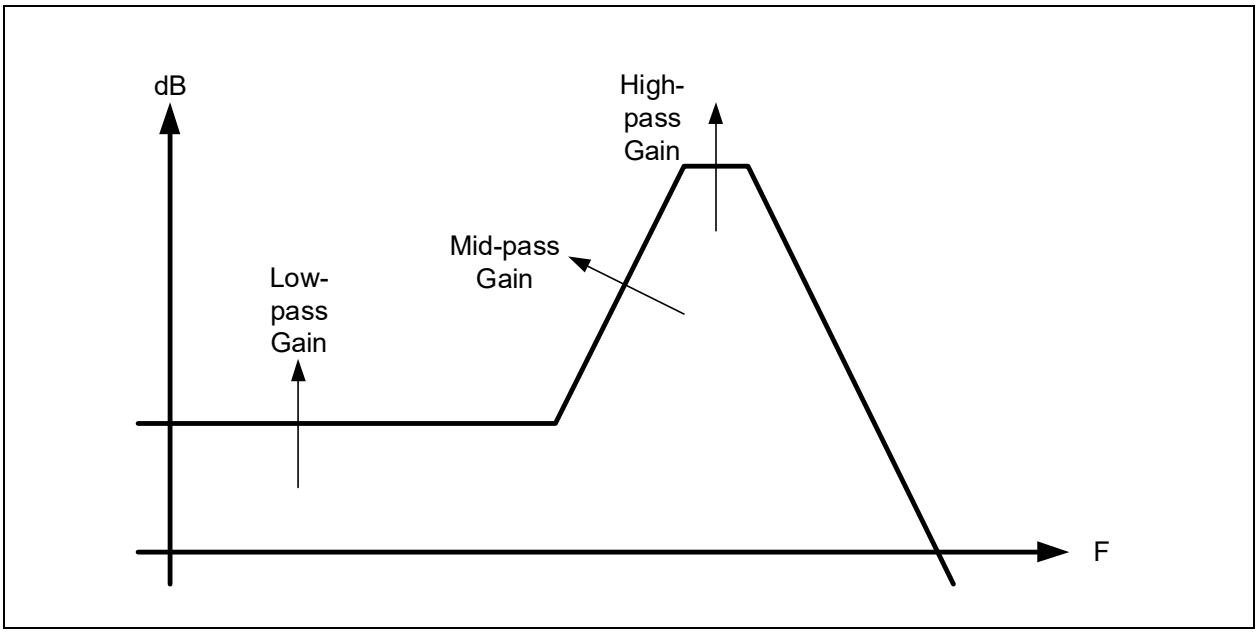
7.2.8 IB EQUALIZATION

The equalizer is automatically adapting to the channel's characteristics using its default setup, thus no user interaction is normally required. Only for channels that have a negligible loss like short PCB connections between two devices mounted on the same board or short, high-quality cable connections, the default setup might not be adequate. In these cases, alternative setup can be applied, which is described in the following sections.

The 6G SerDes IB has been designed to recover data signals at different baud rates and transmitted over channels with different loss characteristics. Channels with low loss are ideal from a signal point of view, but do not provide information where the emphasis of automatic regulation needs to operate.

The damping caused by the connection lines is very dependent on the frequency of the transmitted signal. Therefore, the IB contains an equalizer, which allows to process three different frequency ranges independently. The theoretical behavior is shown in below figure.

FIGURE 7-1: BAND-DEPENDENT GAIN ADJUSTMENT



For short connection lines, the low frequency parts of the signal suffer only very little damping. Consequently, the default regulation behavior of the IB might cause too much gain in this band.

This situation can be prevented by changing the default settings to the following:

1. Select recognition-bit-pattern for low pass gain adjustment

   SERDES6G_IB_CFG0.IB_REG_PAT_SEL_LP 2

2. Select initial low pass gain value at startup

   SERDES6G_IB_CFG3.IB_INI_LP 0

3. Select upper limit for automatic low-pass gain regulation

   SERDES6G_IB_CFG4.liB_MAX_LP 2

Activation of these new settings is done by toggling the following two register fields:

- Force user settings for low pass gain

  SERDES6G_IB_CFG1.IB_FILT_LP to `0`, and SERDES6G_IB_CFG1.IB_FORCE_LP to `1`.

- Clock user settings into register by setting both fields back to `1` and `0`, respectively.

The above way of changing initial, minimum, and/or maximum values can be applied for the LP, MP, HP, or sampling offset, individually or all together. Note that when changing the settings, it must be guaranteed that IB_INI_xx is always within the range defined by IB_MIN_xx and IB_MAX_xx.

7.2.9 IB EQUALIZATION: FIXED FILTERING AND OFFSET TEST

In the following example, the VSC8490 10G PHY is used as a demonstration vehicle. The VSC8490 has two channels, where each channel XAUI host interface has four 6G SerDes lanes. The example demonstrates how to set the equalizer into different modes of operation and how to set initial values and/or minimum and maximum values to decrease the range of possible dynamic settings.

In VSC8490, the IB setting is applied to all four lanes from one common set of configuration registers (although the status registers are kept separate).

Note:	The configuration registers are divided into A and B parts, as the MDIO access data width is only 16-bit wide, wheres the VSC switches are always 32 bits.

A static value applied to all lanes should work in general, if the traces, and so on are the same. Otherwise the settings for each individual XAUI lane found in the dynamic 'Auto-tuning' mode can be frozen.

Table 7-5 shows the active SERDES6G_IB_CFGx configuration registers:

TABLE 7-5: VSC8490 XAUI HOST 0 EQUALIZER CONFIGURATION

Name	Bits 13:8	Bits 5:0	Address	API value
SERDES6G_IB_CFG3A	Init HP (0x00)	Init MP (0x1f)	4xe61f	0x001f
SERDES6G_IB_CFG3B	Init LP (0x01)	Init Offset (0x1f)	4xe620a	0x011f
SERDES6G_IB_CFG4A	Max HP (0x3f)	Max MP (0x3f)	4xe621	0x3f3f
SERDES6G_IB_CFG4B	Max LP (0x02)	Max Offset (0x3f)	4xe622	0x023f
SERDES6G_IB_CFG5A	Min HP (0x00)	Min MP (0x00)	4xe623	0x0000
SERDES6G_IB_CFG5B	Min LP (0x00)	Min Offset (0x00)	4xe624	0x0000
SERDES6G_IB_CFG0B	Toggle enable bit 0 to apply settings to the Equalizer		4xe61a	0x583f
SERDES6G_IB_CFG1B	‘Mode’ select		4xe61c	0x0ff0

The last configuration register CFG1B (4xe61c) is used to change between Dynamic or Static mode.

TABLE 7-6: SERDES6G_IB_CFG1B REGISTER DESCRIPTION

Bit	Name	Access	Description	Default
11:8	IB_SCALY	R/W	Selects the number of calibration cycles for the equalizer, sampling stage, signal-detect, and AC-JTAG comparator, BIAS. 0: No calibration --> neutral values are used.	0x0
7	IB_FILT_HP	R/W	Selects doubled filtering of high-pass-gain regulation or sets it to hold if ib_frc_hp = 1.	0x1
6	IB_FILT_MID	R/W	Selects doubled filtering of mid-pass-gain regulation or sets it to hold if ib_frc_mid = 1.	0x1
5	IB_FILT_LP	R/W	Selects doubled filtering of low-pass-gain regulation or sets it to hold if ib_frc_lp = 1.	0x1
4	IB_FILT_OFFSET	R/W	Selects doubled filtering of offset regulation or sets it to hold if ib_frc_offset = 1.	0x1
3	IB_FRC_HP	R/W	Selects manual control for high-pass-gain regulation if enabled.	0x1
2	IB_FRC_MID	R/W	Selects manual control for mid-pass-gain regulation if enabled.	0x1
1	IB_FRC_LP	R/W	Selects manual control for low-pass-gain regulation if enabled.	0x1
0	IB_FRC_OFFSET	R/W	Selects manual control for offset regulation if enabled.	0x1

Four different modes can be identified and selected by setting SERDES6G_IB_CFG1B (4xe61c):

- Normal Dynamic mode using 31 calibration cycles, 0x0ff0.
- Freeze the current dynamic settings, 0x0fff.
- Static mode with values given by the programmable initial values, 0x0f0f.
- Run calibration with new min/max numbers, 0x0f00 (not 0x0ff0).

For new settings to take effect, a toggle enable should be performed on configuration register SERDES6G_IB_CFG0B (4xe61a). Write the value 0x583e followed by 0x583f.

```
// Read current offset (and LP) from SerDes6G_IB_Status1B_lane - see they varies
# phy mmd read 0x4 0xe632
   1     25  0xe632   0x0025  0000.0000.0010.0101
# phy mmd read 0x4 0xe632
   1     25  0xe632   0x0024  0000.0000.0010.0100
# phy mmd read 0x4 0xe639
   1     25  0xe639   0x0022  0000.0000.0010.0010
# phy mmd read 0x4 0xe639
   1     25  0xe639   0x0020  0000.0000.0010.0000
# phy mmd read 0x4 0xe640
   1     25  0xe640   0x002f  0000.0000.0010.1111
# phy mmd read 0x4 0xe640
   1     25  0xe640   0x0030  0000.0000.0011.0000
# phy mmd read 0x4 0xe647
   1     25  0xe647   0x0034  0000.0000.0011.0100
# phy mmd read 0x4 0xe647
   1     25  0xe647   0x0035  0000.0000.0011.0101

// Freeze current dynamic settings (mode 2))
deb phy mmd read 0x4 0xe61c
   1     25  0xe61c   0x0ff0  0000.1111.1111.0000
# phy mmd write 0x4 0xe61c 0x0fff
# phy mmd read 0x4 0xe61a
   1     25  0xe61a   0x583f  0101.1000.0011.1111
# phy mmd write 0x4 0xe61a 0x583e
# phy mmd write 0x4 0xe61a 0x583f

// Read current offset (and LP) freezed settings - see they are constant value
# phy mmd read 0x4 0xe632
   1     25  0xe632   0x0023  0000.0000.0010.0011
# phy mmd read 0x4 0xe632
   1     25  0xe632   0x0023  0000.0000.0010.0011
# phy mmd read 0x4 0xe639
   1     25  0xe639   0x0020  0000.0000.0010.0000
# phy mmd read 0x4 0xe639
   1     25  0xe639   0x0020  0000.0000.0010.0000
# phy mmd read 0x4 0xe640
   1     25  0xe640   0x002f  0000.0000.0010.1111
# phy mmd read 0x4 0xe640
   1     25  0xe640   0x002f  0000.0000.0010.1111
# phy mmd read 0x4 0xe647
   1     25  0xe647   0x0034  0000.0000.0011.0100
# phy mmd read 0x4 0xe647
   1     25  0xe647   0x0034  0000.0000.0011.0100

// Send frames from Switch in Tx direction to see, if they are forwarded normally
# clear statistics *
# deb frame tx interface 10g 1/2 packet-size 1230
Transmitting 10000 frames...Done in 3.940 seconds.
# show interface 10g * statistics pac
Interface               Rx Packets          Tx Packets
----------------------  ------------------  ------------------
10GigabitEthernet 1/1   10000               0
10GigabitEthernet 1/2   0                   10000
10GigabitEthernet 1/3   0                   0
10GigabitEthernet 1/4   0                   0
#
```

```
// Test static settings (mode 3)) - Initial value HP, MP and LP = 0
// Set initial offset value (from above mean=(0x23+0x20+0x2f+0x34)/4=0x28)
# phy mmd read 0x4 0xe61f
   1     25  0xe61f   0x001f  0000.0000.0001.1111
# phy mmd write 0x4 0xe61f 0x0000
# deb phy mmd read 0x4 0xe620
   1     25  0xe620   0x011f  0000.0001.0001.1111
# phy mmd write 0x4 0xe620 0x0028
# phy mmd write 0x4 0xe61c 0x0f0f
# phy mmd write 0x4 0xe61a 0x583e
# phy mmd write 0x4 0xe61a 0x583f
#
// Read current offset (and LP) - see they have initial settings
# phy mmd read 0x4 0xe632
   1     25  0xe632   0x0028  0000.0000.0010.1000
# phy mmd read 0x4 0xe639
   1     25  0xe639   0x0028  0000.0000.0010.1000
# phy mmd read 0x4 0xe640
   1     25  0xe640   0x0028  0000.0000.0010.1000
# phy mmd read 0x4 0xe647
   1     25  0xe647   0x0028  0000.0000.0010.1000
#
// Send frames in Tx direction to see, if they are forwarded normally
# clear statistics *
# deb frame tx interface 10g 1/2 pac 1230
Transmitting 10000 frames...Done in 3.907 seconds.
# show interface 10g * statistics pac
Interface               Rx Packets          Tx Packets
----------------------  ------------------  ------------------
10GigabitEthernet 1/1   10000               0
10GigabitEthernet 1/2   0                   10000
10GigabitEthernet 1/3   0                   0
10GigabitEthernet 1/4   0                   0
#

// Re-run in dynamic Equalization (mode 1))
# phy mmd write 0x4 0xe61c 0x0ff0
# phy mmd write 0x4 0xe61a 0x583e
# phy mmd write 0x4 0xe61a 0x583f
#
// Read current offset (and LP) - see they varies
# phy mmd read 0x4 0xe632
   1     25  0xe632   0x0023  0000.0000.0010.0011
# phy mmd read 0x4 0xe632
   1     25  0xe632   0x0022  0000.0000.0010.0010
# phy mmd read 0x4 0xe639
   1     25  0xe639   0x0020  0000.0000.0010.0000
# phy mmd read 0x4 0xe639
   1     25  0xe639   0x0020  0000.0000.0010.0000
# phy mmd read 0x4 0xe640
   1     25  0xe640   0x0031  0000.0000.0011.0001
# phy mmd read 0x4 0xe640
   1     25  0xe640   0x002d  0000.0000.0010.1101
# phy mmd read 0x4 0xe647
   1     25  0xe647   0x0033  0000.0000.0011.0011
# phy mmd read 0x4 0xe647
   1     25  0xe647   0x0032  0000.0000.0011.0010
```

```
// Change min/max settings on the fly (mode 4)), offset between 0x2b-0x25
# phy mmd read 0x4 0xe622
   1     25  0xe622   0x023f  0000.0010.0011.1111
# phy mmd write 0x4 0xe622 0x022b
# phy mmd read 0x4 0xe624
   1     25  0xe624   0x0000  0000.0000.0000.0000
# phy mmd write 0x4 0xe624 0x0025
# phy mmd write 0x4 0xe61c 0x0f00
# phy mmd write 0x4 0xe61a 0x583e
# phy mmd write 0x4 0xe61a 0x583f

// Read current offset (and LP) - see they are at either max or min value
# phy mmd read 0x4 0xe632
   1     25  0xe632   0x0025  0000.0000.0010.0101
# phy mmd read 0x4 0xe632
   1     25  0xe632   0x0025  0000.0000.0010.0101
# phy mmd read 0x4 0xe639
   1     25  0xe639   0x0025  0000.0000.0010.0101
# phy mmd read 0x4 0xe639
   1     25  0xe639   0x0025  0000.0000.0010.0101
# phy mmd read 0x4 0xe640
   1     25  0xe640   0x002b  0000.0000.0010.1011
# phy mmd read 0x4 0xe640
   1     25  0xe640   0x002b  0000.0000.0010.1011
# phy mmd read 0x4 0xe647
   1     25  0xe647   0x002b  0000.0000.0010.1011
# phy mmd read 0x4 0xe647
   1     25  0xe647   0x002b  0000.0000.0010.1011

// Send frames in Tx direction to see, if they are forwarded normally
# clear statistics *
# deb frame tx interface 10g 1/2 pac 1230
Transmitting 10000 frames...Done in 3.934 seconds.
# show interface 10g * statistics pac
Interface               Rx Packets          Tx Packets
----------------------  ------------------  ------------------
10GigabitEthernet 1/1   10000               0
10GigabitEthernet 1/2   0                   10000
10GigabitEthernet 1/3   0                   0
10GigabitEthernet 1/4   0                   0
#
```

7.2.10 INSERTION LOSS

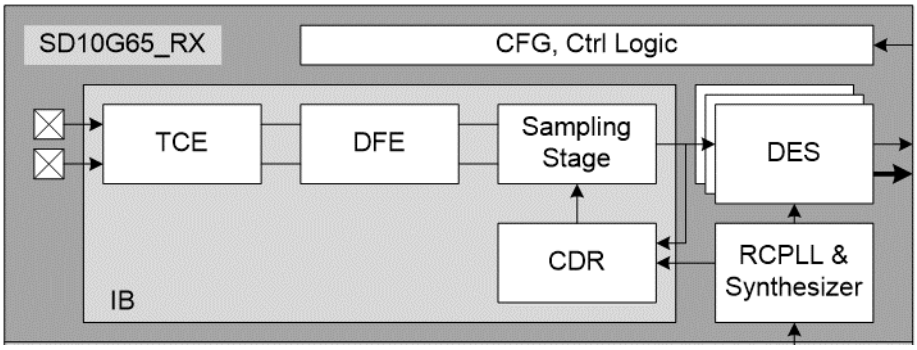
Insertion-loss is a measure for the damping of a signal by the channel. The 1G Serdes equalizing capabilities can handle up to 10-11 dB insertion loss, whereas the 6G SerDes is designed to equalize more than 27 db loss at 3 GHz.

Reflections must be minimized, so return-loss should be high, whereas the damping of the channel (insertion-loss) should be minimized (signal is not damped, so the receiver does not need to deal with small and distorted eyes).

7.3 10G SerDes Input Buffer

The high-speed input is terminated inside a termination stage. The equalization of the signal is done by a Continuous-Time-Linear-Equalizer (CTLE) followed by a Decision-Feedback-Equalizer (DFE). After sampling the rehashed signal, a Deserializer splits it into parallel digital signals of lower speed. The sampling clock is generated by an RC-PLL.

FIGURE 7-2: HIGH-LEVEL STRUCTURAL BLOCK DIAGRAM



The 10G Input Buffer features:

- Automatic data independent input voltage offset compensation
- High-precision signal detect functionality
- Time Continuous Equalization filter (TCE/CTLE)
- Four-tap Decision Feedback Equalization (DFE)
- TCE and DFE with filters that can be automatically controlled via APC and LMS
- CDR with programmable loop-bandwidth and phase regulation
- RC-PLL with configurable baud rate support
- Silicon process variation compensation

7.3.1 INPUT BUFFER TERMINATION

The high-speed input is terminated into 100Ω differential to a common-mode voltage selectable by IB_TERM_V_SEL. The termination resistance is automatically adjusted by the value determined by the common RCOMP cell, but can be corrected using IB_RIB_ADJ.

For DC coupling, IB_TERM_VDD_ENA can be set, which complies to the OIF CEI load specification. For this setting the common point of the input termination resistances is connected to Vdda and results in having load resistances for the connected transmitter. Thus the current of the transmitter's output stage can be doubled without shifting common-mode voltage. This improves bandwidth and linearity.

When AC-coupled (IB_TERM_VDD_ENA = 0), the common-mode termination voltage is internally generated and the impedance of the voltage can be lowered by setting IB_TERM_V_SEL to improve suppression of common-mode noise.

The input termination supply voltage can be 1.0V or 1.2V. This is controlled from IB_1V_ENA.

TABLE 7-7: COMMON-MODE TERMINATION SETTINGS

Register name	Description
SD10G65_IB_CFG0.IB_TERM_VDD_ENA	Enable common-mode termination 0: Termination to 0.7*Vdda for AC coupling 1: Termination to Vdda for DC coupling
SD10G65_IB_CFG0.IB_TERM_V_SEL	Selects impedance for AC coupling
SD10G65_IB_CFG0.IB_1V_ENA	Termination supply voltage 0: 1.2V 1: 1.0V mode
SD10G65_IB_CFG0.IB_RIB_ADJ	Termination resistance offset adjustment

7.3.2 TWO SIGNAL DETECTION CIRCUITRIES

The auxiliary stage contains functionality for signal detection. An alternative source for signal detection is located inside the equalizer stage and can be chosen by setting IB_SDET_SEL. They are enabled by setting IB_IA_SDET_ENA and IB_IE_SDET_ENA. The results of both circuitries are visible at IB_IA_SDET and IB_IE_SDET and can be forced high by IB_SET_SDET.

The signal detection thresholds are adjustable by IB_IA_SDET_LEVEL and IB_IE_SDET_LEVEL and are calibrated at start-up sequence automatically.

The IA signal detection circuitry is controlled by a dividable reset clock, which should always be lower than the signal activity density at longer bit sequences (<1 GHz).

TABLE 7-8: 10G SIGNAL DETECT SETTINGS

Register name	Description
SD10G65_IB_CFG0.IB_IA_ENA	Enable Auxiliary stage
SD10G65_IB_CFG0.IB_IA_SDET_ENA	Enable Auxiliary stage signal detection circuitry
SD10G65_IB_CFG0.IB_IE_SDET_ENA	Enable Equalizer stage signal detection circuitry
SD10G65_IB_CFG3.IB_SET_SDET	Force Signal Detect output high
SD10G65_IB_CFG3.IB_SDET_SEL.	Selects Signal Detect source 0: IA 1: IE
SD10G65_IB_CFG3.IB_IA_SDET_LEVEL	Threshold value for IA Signal Detect
SD10G65_IB_CFG3.IB_IE_SDET_LEVEL	Threshold value for IE Signal Detect
SD10G65_IB_CFG3.IB_SDET_CLK_DIV	Clock dividing factor for IA signal detection circuitry
SD10G65_IB_CFG3.IB_LDSD_DIVSEL	Dividing factor for IE Signal Detect and Level Detect
SD10G65_IB_CFG10.IB_IA_SDET	IA Signal Detect result
SD10G65_IB_CFG10.IB_IE_SDET	IEA Signal Detect result

7.3.3 AUTOMATIC CONTROL (APC AND LMS)

Automatic Control takes care of the CTLE settings by using the APC algorithm and the DFE settings by using the LMS algorithm. Both controls can be enabled separately or switched into Manual mode by setting APC_MODE register.

TABLE 7-9: 10G APC SETTINGS

Register name	Description
APC_COMMON_CFG0.APC_MODE	APC operation mode
APC_COMMON_CFG0.IF_WIDTH	Interface bit width

7.3.4 SAMPLING STAGE

Sampling of time-continuous data is done at the output of DFE stage by three sampling channels in parallel. Beside the main channel, there are two additional channels having a significant positive and negative offset compared to the main channel. Both are used for automatic control of the DFE and CTLE by APC or LMS algorithm and can be enabled by setting IB_VSCOPE_ENA. They can also be used for scanning data eye opening in the “VScope” mode, which is enabled by setting VSCOPE_ENA.

The APC algorithm searches for characteristic sequences in the main data stream and compares the critical bit inside the sequence with the data samples on the auxiliary channels. The results of these comparisons are used for adjusting the gain, offset, and filter coefficients of the equalizers. The regulation targets a 50% error rate on both channels.

For normal operation mode, the auxiliary threshold values should be chosen symmetrical around zero, which means that IB_VSCOPE_L_THRES should be programmed with the negative value of IB_VSCOPE_H_THRES.

Normally, the main threshold IB_MAIN_THRES should be programmed to zero, but can be adjusted by an external forward-error-correction (FER). For unsymmetrical data eyes caused by optical channels, IB_MAIN_THRES can be moved into the wider opened side of the data eye.

TABLE 7-10: 10G SAMPLER SETTINGS

Register name	Description
SD10G65_IB_CFG0.IB_SAM_ENA	Enables sampling stage
SD10G65_IB_CFG0.IB_CLKDIV_ENA	Enables clock dividers
SD10G65_IB_CFG0.IB_VSCOPE_ENA	Enables auxiliary sampling channels
SD10G65_IB_CFG4.IB_MAIN_THRES	Threshold value for main sampling path
SD10G65_IB_CFG4.IB_VSCOPE_H_THRES	Threshold value for auxiliary high sampling path
SD10G65_IB_CFG4.IB_VSCOPE_L_THRES	Threshold value for auxiliary low sampling path

7.3.5 DESERIALIZER

The Deserializer splits the high-speed signal into several parallel data signals of lower speed. The number of parallel data signals are selectable by setting the interface width in DES_IF_MODE_SEL.

TABLE 7-11: 10G DESERIALIZER SETTINGS

Register name	Description
SD10G65_DES_CFG0.DES_DIS	Disables deserializer
SD10G65_DES_CFG0.DES_VSC_DIS	Disables auxiliary channels of deserializer
SD10G65_DES_CFG0.DES_IF_MODE_SEL	Setting interface width

7.3.6 CLOCK AND DATA RECOVERY LOOP FILTER

The CDR loop filter tracks the phase and frequency offset of the input data in two separate ways. The dynamic changes are compensated by using the first and second order contribution of the regulator in a low latency loop by incorporating a phase rotator behind the RC-PLL. The static frequency offset is compensated by injecting the third order contribution of the regulator into the feedback path of the RC-PLL.

TABLE 7-12: 10G SYNTHESIZER/CDR LOOP FILTER SETTINGS

Register name	Description
SD10G65_RX_SYNTH_CFG0.SYNTH_FB_STEP	Selects step width for sync output
SD10G65_RX_SYNTH_CFG0.SYNTH_P_STEP	Selects step width for proportional part
SD10G65_RX_SYNTH_CDRLF.SYNTH_INTEG1_FSEL	Selects frequency of integrator 1
SD10G65_RX_SYNTH_CDRLF.SYNTH_INTEG2_FSEL	Selects frequency of integrator 2

The CDR loop filter is implemented as third order filter with one proportional path and two cascaded integrators. The proportional part is controlled by MOEBDIV_BW_CDR_SEL_A/B.

FIGURE 7-3: CDR LOOP FILTER STRUCTURE

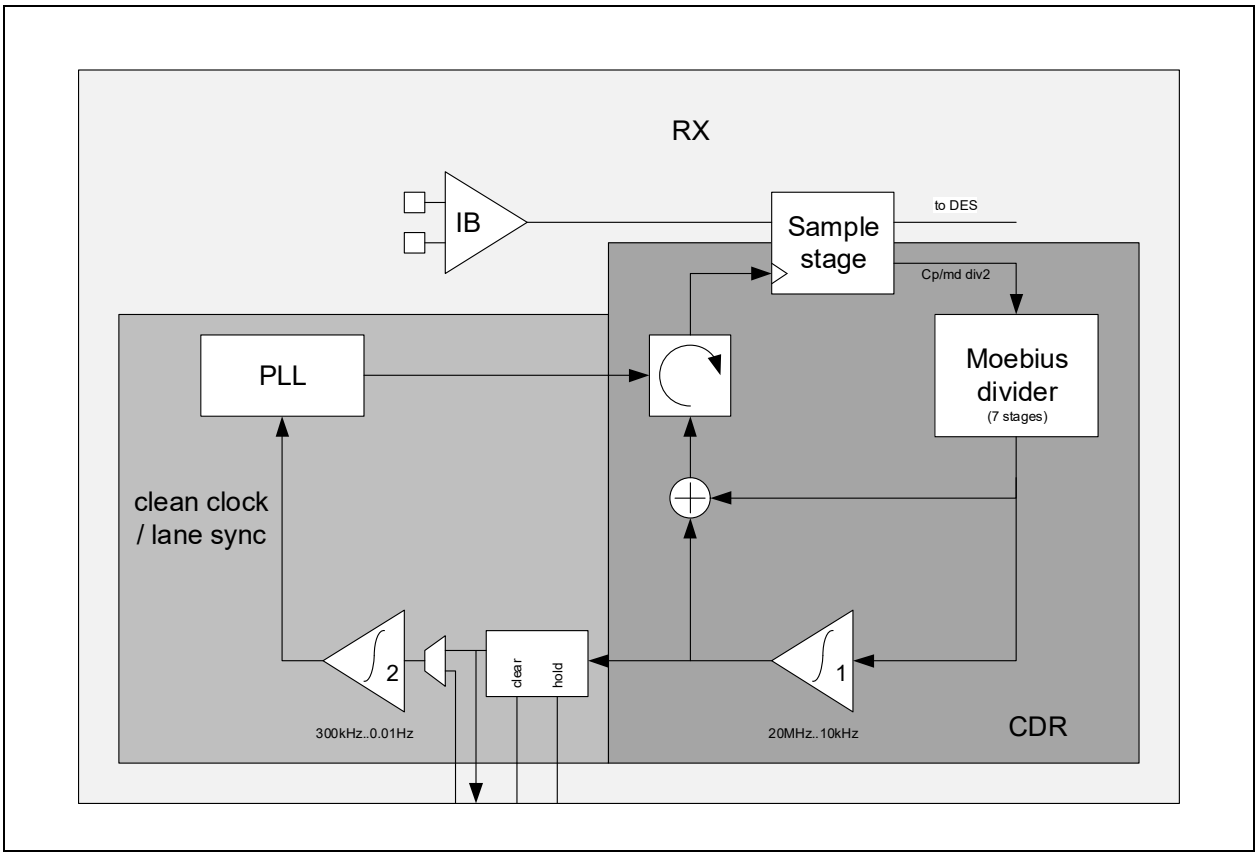


Table 7-13 gives the maximum frequency offset compensation capability in parts per million (ppm) dependent on the configuration. The values are valid for a high-speed pattern (“1010”) and an ideal signal without jitter. A good configuration is where the value in Table 7-13 is in the range of four times the expected frequency offset in the application.

TABLE 7-13: 10G FREQUENCY OFFSET COMPENSATION CAPABILITY

MOEBDIV_BW_CDR_SEL_A/B	Double rate	Full rate	Half rate
0	7812 ppm	3906 ppm	1953 ppm
1	3906 ppm	1953 ppm	977 ppm
2	1953 ppm	977 ppm	488 ppm
3	977 ppm	488 ppm	244 ppm
4	488 ppm	244 ppm	122 ppm
5	244 ppm	122 ppm	61 ppm
6	122 ppm	61 ppm	31 ppm
7	61 ppm	31 ppm	15 ppm

The values are valid for the recommended value of SYNTH_P_STEP = 1. With SYNTH_P_STEP = 0, the values are doubled for the prize of a coarser phase regulation.

7.3.7 RCOMP DISTRIBUTION

The SerDes IO buffers as well as the CML logic of the 10G macro are required to be resistor-calibrated to guarantee proper performance (that is, IO resistance, speed of CML cells) over PVT.

The calibration is done by adjusting the 10G macro internal resistor networks through a digital 4-bit value. This 4-bit calibration value itself is generated by the RCOMP cell, which compares an external 1%, 620Ω resistance to an internal resistor.

7.3.8 RETURN LOSS VS. CHANGE IN TERMINATION TEST

Return-loss is a measure for how much of the signal is reflected at the sink. Most of the reflection is caused by mismatch in impedance. The SerDes IO buffers comply to standard; however board layout typically changes from an ideal impedance and thus increases the return loss to an undesired level.

The SerDes IO buffers can be manually calibrated using an offset to the RCOMP value.

The following test changes the termination value for both Input and Output buffers. This is done by writing to the SD10G65_SBUS_RX_CFG.SBUS_RCOMP register. The following status readouts are made to identify if there are any changes in the SerDes equalizer settings. The idea is to program a new “value” into the SerDes IO buffers to change termination and thus find a way of “measuring” return-loss.

```
// See current linkup - 10G port 1/1 and 1/2 are looped together using 1m DAC cable
# show interface 10g 1/1,2 status
Interface              Mode    Speed&Duplex FlowControl MaxFrame Excessive Link
---------------------- ------- ------------ ----------- -------- --------- ------
10GigabitEthernet 1/1  enabled 10Gfdx       disabled    10240    Discard   10Gfdx
10GigabitEthernet 1/2  enabled 10Gfdx       disabled    10240    Discard   10Gfdx

// See current register setting, the manual offset value to RCOMP is not set (=0)
# debug sym read ::sd10g65_sbus_rx_cfg
Register                     Value
XGANA[0]::SD10G65_SBUS_RX_CFG 0x00000007
XGANA[1]::SD10G65_SBUS_RX_CFG 0x00000007
XGANA[2]::SD10G65_SBUS_RX_CFG 0x00000007
XGANA[3]::SD10G65_SBUS_RX_CFG 0x00000007

// See current APC values for 10G port 1
# debug api port in 10g 1/1 | begin APC
APC status:
port    gain   g.adj  ldlev   offs   agc     c    l      dfe1   dfe2   dfe3   dfe4
49      0      35     24      518    95      12   24     85     21     13     16
50      0      40     24      512    96      12   24     76     25     13     15

// Change value to +1 on 10G port 1
# debug sym write xgana[0]::sd10g65_sbus_rx_cfg 0xf
Register                     Value
XGANA[0]::SD10G65_SBUS_RX_CFG 0x0000000f

# debug api port in 10g 1/1 | begin APC
APC status:
port    gain   g.adj  ldlev   offs   agc     c    l      dfe1   dfe2   dfe3   dfe4
49      0      34     24      518    96      12   24     85     22     13     16
50      0      41     24      512    96      12   24     76     24     14     15

// Change value to +3 on 10G port 1
# debug sym write xgana[0]::sd10g65_sbus_rx_cfg 0x1f
Register                     Value
XGANA[0]::SD10G65_SBUS_RX_CFG 0x0000001f

# debug api port in 10g 1/1 | begin APC
APC status:
port    gain   g.adj  ldlev   offs   agc     c    l      dfe1   dfe2   dfe3   dfe4
49      0      36     24      518    96      12   24     85     21     13     16
50      0      42     24      513    96      12   24     78     24     13     15
```

```
// Change value to -1 on 10G port 1
# debug sym write xgana[0]::sd10g65_sbus_rx_cfg 0x7f
Register                      Value
XGANA[0]::SD10G65_SBUS_RX_CFG 0x0000007f

# debug api port in 10g 1/1 | begin APC
APC status:
port    gain   g.adj  ldlev   offs   agc     c    l      dfe1   dfe2   dfe3   dfe4
49      0      35     24      519    95      12   24     85     21     13     16
50      0      41     24      512    96      12   24     76     25     13     15

// Change value to -3 on 10G port 1
# debug sym write xgana[0]::sd10g65_sbus_rx_cfg 0x6f
Register                      Value
XGANA[0]::SD10G65_SBUS_RX_CFG 0x0000006f

# debug api port in 10g 1/1 | begin APC
APC status:
port    gain   g.adj  ldlev   offs   agc     c    l      dfe1   dfe2   dfe3   dfe4
49      0      37     24      518    96      12   24     85     22     13     16
50      0      42     24      513    96      12   24     74     26     13     15

//-------------------------------------------------------------------------------
// Collecting the data side-by-side gives a better overview
   port    gain   g.adj  ldlev   offs   agc     c    l    dfe1   dfe2   dfe3   dfe4
+3 49      0      36     24      518    96      12   24   85     21     13     16
+1 49      0      34     24      518    96      12   24   85     22     13     16
0  49      0      35     24      518    95      12   24   85     21     13     16
-1 49      0      35     24      519    95      12   24   85     21     13     16
-3 49      0      37     24      518    96      12   24   85     22     13     16

+3 50      0      42     24      513    96      12   24   78     24     13     15
+1 50      0      41     24      512    96      12   24   76     24     14     15
0  50      0      40     24      512    96      12   24   76     25     13     15
-1 50      0      41     24      512    96      12   24   76     25     13     15
-3 50      0      42     24      513    96      12   24   74     26     13     15
```

In above test, there is an increased gain adjustment when changing the termination. This could be an indication of termination mismatch, so there might be a correlation to return-loss.

NOTES:

APPENDIX A: SERDES SHADOW REGISTERS

The SerDes macros are set up indirectly using shadow registers. This indirect read and write to each SerDes macro is controlled through an address or mask register (MCB). Either all registers are read out to the shadow registers, or all shadow registers are written to the SerDes macro.

```
# deb sym read hsio:serdes*
Register                                          Value
HSIO:SERDES1G_ANA_CFG:SERDES1G_DES_CFG            0x0000c2ce
HSIO:SERDES1G_ANA_CFG:SERDES1G_IB_CFG             0x0100220b
HSIO:SERDES1G_ANA_CFG:SERDES1G_OB_CFG             0x00078841
HSIO:SERDES1G_ANA_CFG:SERDES1G_SER_CFG            0x00000000
HSIO:SERDES1G_ANA_CFG:SERDES1G_COMMON_CFG         0x80040001
HSIO:SERDES1G_ANA_CFG:SERDES1G_PLL_CFG            0x0020c880
HSIO:SERDES1G_ANA_STATUS:SERDES1G_PLL_STATUS      0x00001000
HSIO:SERDES1G_DIG_CFG:SERDES1G_DFT_CFG0           0x00000000
HSIO:SERDES1G_DIG_CFG:SERDES1G_DFT_CFG1           0x00000000
HSIO:SERDES1G_DIG_CFG:SERDES1G_DFT_CFG2           0x00000000
HSIO:SERDES1G_DIG_CFG:SERDES1G_TP_CFG             0x00000000
HSIO:SERDES1G_DIG_CFG:SERDES1G_RC_PLL_BIST_CFG    0x0002c8c8
HSIO:SERDES1G_DIG_CFG:SERDES1G_MISC_CFG           0x00000000
HSIO:SERDES1G_DIG_STATUS:SERDES1G_DFT_STATUS      0x000000c2
HSIO:SERDES1G_DIG_STATUS:SERDES1G_MISC_STATUS     0x00000000
HSIO:MCB_SERDES1G_CFG:MCB_SERDES1G_ADDR_CFG       0x00000020

HSIO:SERDES6G_DIG_CFG:SERDES6G_DIG_CFG            0x00000000
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG0           0x00000000
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG1           0x00000000
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG2           0x00000000
HSIO:SERDES6G_DIG_CFG:SERDES6G_TP_CFG0            0x00000000
HSIO:SERDES6G_DIG_CFG:SERDES6G_TP_CFG1            0x00000000
HSIO:SERDES6G_DIG_CFG:SERDES6G_RC_PLL_BIST_CFG    0x00007878
HSIO:SERDES6G_DIG_CFG:SERDES6G_MISC_CFG           0x00000000
HSIO:SERDES6G_DIG_CFG:SERDES6G_OB_ANEG_CFG        0x00000000
HSIO:SERDES6G_DIG_STATUS:SERDES6G_DFT_STATUS      0x000000c2
HSIO:SERDES6G_DIG_STATUS:SERDES6G_ERR_CNT         0x00000000
HSIO:SERDES6G_DIG_STATUS:SERDES6G_MISC_STATUS     0x00000000
HSIO:SERDES6G_ANA_CFG:SERDES6G_DES_CFG            0x000048a6
HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG             0x3d57ac3f
HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG1            0x00103ff0
HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG2            0x1fc78194
HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG3            0x0001f05f
HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG4            0x00fff0bf
HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG5            0x00000000
HSIO:SERDES6G_ANA_CFG:SERDES6G_OB_CFG             0x20800171
HSIO:SERDES6G_ANA_CFG:SERDES6G_OB_CFG1            0x000000b0
HSIO:SERDES6G_ANA_CFG:SERDES6G_SER_CFG            0x00000000
HSIO:SERDES6G_ANA_CFG:SERDES6G_COMMON_CFG         0x00024005
HSIO:SERDES6G_ANA_CFG:SERDES6G_PLL_CFG            0x00030f20
HSIO:SERDES6G_ANA_CFG:SERDES6G_ACJTAG_CFG         0x00000000
HSIO:SERDES6G_ANA_CFG:SERDES6G_GP_CFG             0x00000300
HSIO:SERDES6G_ANA_STATUS:SERDES6G_IB_STATUS0      0x000001fa
HSIO:SERDES6G_ANA_STATUS:SERDES6G_IB_STATUS1      0x00fff080
HSIO:SERDES6G_ANA_STATUS:SERDES6G_ACJTAG_STATUS   0x00000004
HSIO:SERDES6G_ANA_STATUS:SERDES6G_PLL_STATUS      0x00000400
HSIO:SERDES6G_ANA_STATUS:SERDES6G_REVID           0x2cc410a3
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG       0x00000002
#
```

The read from or write to the SerDes macro is done by a write to the MCB register. The status or progress of the last write action is found by reading the MCB register. Bit 31 and 30 should be cleared before initiating a new write action.

TABLE A-1: MCB SERDES6G ADDRESS CFG

Short Name: MACRO_CTRL::MCB_SERDES6G_ADDR_CFG
Configuration of SERDES6G MCB macros to be accessed

Bit	Name	Access	Description	Default
31	SERDES6G_WR_ONE_SHOT	One-shot	Initiate a write access to marked SerDes6G macros 0: No write operation pending 1: Initiate write to macros (kept 1 until write operation has finished)	0x0
30	SERDES6G_RD_ONE_SHOT	One-shot	Initiate a read access to marked SerDes6G macros 0: No read operation pending (read op finished after bit has been set) 1: Initiate a read access (kept 1 until read operation has finished)	0x0
24:0	SERDES6G_ADDR	R/W	Activation vector for SerDes6G macros, one-hot coded, each bit is related to one macro, for example, bit 0 enables/disables access to macro no. 0. 0: Disable macro access via MCB 1: Enable macro access via MCB	0x1FFFFFF

APPENDIX B: REGISTER ACCESS USING UNMANAGED BOARD

When testing on Managed board, the debug CLI commands are used for symbolic register read and write. On an Unmanaged board, register address is used directly because the Unmanaged CLI does not offer the symbolic naming.

```
// Finding the register addresses on a Managed Ocelot board/PCB123.
# deb sym query hsio:serdes6g_dig*
Register                                          Address
HSIO:SERDES6G_DIG_CFG:SERDES6G_DIG_CFG            0x710d008c
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG0           0x710d0090
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG1           0x710d0094
HSIO:SERDES6G_DIG_CFG:SERDES6G_DFT_CFG2           0x710d0098
HSIO:SERDES6G_DIG_CFG:SERDES6G_TP_CFG0            0x710d009c
HSIO:SERDES6G_DIG_CFG:SERDES6G_TP_CFG1            0x710d00a0
HSIO:SERDES6G_DIG_CFG:SERDES6G_RC_PLL_BIST_CFG    0x710d00a4
HSIO:SERDES6G_DIG_CFG:SERDES6G_MISC_CFG           0x710d00a8
HSIO:SERDES6G_DIG_CFG:SERDES6G_OB_ANEG_CFG        0x710d00ac
HSIO:SERDES6G_DIG_STATUS:SERDES6G_DFT_STATUS      0x710d00b0
HSIO:SERDES6G_DIG_STATUS:SERDES6G_ERR_CNT         0x710d00b4
HSIO:SERDES6G_DIG_STATUS:SERDES6G_MISC_STATUS     0x710d00b8

# deb sym query hsio::mcb_serdes6g_addr_cfg
Register                                    Address
HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG 0x710d0108
#

// How to use it on an Unmanaged Ocelot board/PCB121.:
>?
V : Show version
R <target> <offset> <addr>: Read from chip register
  --> Example: Read Chip ID register DEVCPU_GCB:CHIP_REGS:CHIP_ID
  -->                                0x71070000       0x0     0x0
  --> Command: R 0x71070000 0x0 0x0
W <target> <offset> <addr> <value>: Write switch register
I <uport> <addr> [<page>]: Read PHY register
  --> Example: Read user port 1 PHY ID from PHY register 2 page 0
  --> Command: I 1 0x2 0
O <uport> <addr> <value> [<page>]: Write PHY register
P : Show Port information
? : Show commands
T <uport>: Send test packet (uport=0xff for all ports)
K <0|1> <uport>: Flow control mode (0=Enable, 1=Disable)
M [<uport> [c]: Show/Clear MAC address entries (uport=0 for CPU port)
X : Reboot device
Z <0|1>: E-Col-Drop mode, linkup ports only (0=Disable, 1=Enable)
H <uport> [c]: Show/Clear port statistics (uport=0 for CPU port)
S <0|1>: Suspend/Resume applications (0=Resume, 1=Suspend)
CONFIG                       : Show all configurations
CONFIG MAC xx:xx:xx:xx:xx:xx : Update MAC addresses in RAM

// Read ChipID
>r 0x71070000 0 0
Hex        Decimal    31     24 23     16 15      8 7       0
---------- ---------- --------- --------- --------- ---------
0x175120e9  391201001 0001.0111.0101.0001.0100.0000.1110.1001
// Read DIG_CFG
>r 0x710d008c 0 0
Hex        Decimal    31     24 23     16 15      8 7       0
---------- ---------- --------- --------- --------- ---------
0x00000000
```

APPENDIX C: LOOPBACK REGISTER DESCRIPTION

TABLE C-1: SERDES1G COMMON CFG

Short Name:MACRO_CTRL::SERDES1G_COMMON_CFG

Bit	Name	Access	Description	Default
31	SYS_RST	R/W	System reset (low active) 0: Apply reset (not self-clearing) 1: Reset released	0x0
21	SE_AUTO_SQUELCH_ENA	R/W	Enable auto-squelching for sync. Ethernet clock output. When set, the clock output will stop toggling (keep its last value constantly) - when PCS loses link synchrony. 0: Disable 1: Enable	0x0
18	ENA_LANE	R/W	Enable lane 0: Disable lane 1: Enable line	0x0
17	PWD_RX [DBG]	R/W	Power-down RX-path 0: Normal mode 1: Power Down mode	0x0
16	PWD_TX [DBG]	R/W	Power-down TX-path 0: Normal mode 1: Power Down mode	0x0
15:13	LANE_CTRL [DBG]	R/W	Hidden spare bits (not connected internally yet)	0x0
12	ENA_DIRECT [DBG]	R/W	Enable direct line 0: Disable 1: Enable	0x0
11	ENA_ELOOP	R/W	Enable equipment loop 0: Disable 1: Enable	0x0
10	ENA_FLOOP	R/W	Enable facility loop. When enabling this loop, the phase alignment in the serializer has to be enabled and configured adequately. SERDES1G_SER_CFG.SER_ENALI must be set to 1. SERDES1G_SER_CFG.SER_ALISELmust be set to 0. 0: Disable 1: Enable	0x0
9	ENA_ILOOP [DBG]	R/W	Enable input loop 0: Disable 1: Enable	0x0
8	ENA_PLOOP [DBG]	R/W	Enable pad loop 0: Disable 1: Enable	0x0
7	HRATE [DBG]	R/W	Enable half rate 0: Disable 1: Enable	0x0
0	IF_MODE [DBG]	R/W	Interface mode 0: 8-bit mode 1: 10-bit mode	0x1

TABLE C-2: SERDES1G SERIALIZER CFG

Short Name:MACRO_CTRL::SERDES1G_SER_CFG

Bit	Name	Access	Description	Default
9	SER_IDLE	R/W	Invert output D0b for idle-mode of OB 0: Non-inverting 1: Inverting	0x0
8	SER_DEEMPH	R/W	Invert and delays (one clock cycle) output D1 for deemphasis of OB 0: Non-inverting and non-delaying 1: Inverting and delaying	0x0
7	SER_CPMD_SEL [DBG]	R/W	Select source of CP/MD signals 0: Phase alignment block 1: Core	0x0
6	SER_SWAP_CPMD [DBG]	R/W	Swap CP/MD signals of phase alignment circuit 0: Disable swapping 1: Enable swapping	0x0
5:4	SER_ALISEL [DBG]	R/W	Select reference clock source for phase alignment 0: RXCLKP 1: RefClk15MHz 2: RXCLKN 3: ext. ALICLK	0x0
3	SER_ENHYS	R/W	Enable hysteresis for phase alignment 0: Disable hysteresis 1: Enable hysteresis	0x0
2	SER_BIG_WIN	R/W	Use wider window for phase alignment 0: Use small window for low jitter (100 to 200 ps) 1: Use wide window for higher jitter (150 to 300 ps)	0x0
1	SER_EN_WIN	R/W	Enable window for phase alignment 0: Disable window 1: Enable window	0x0
0	SER_ENALI	R/W	Enable phase alignment 0: Disable phase alignment 1: Enable phase alignment	0x0

TABLE C-3: PCS1G LOOPBACK CONFIGURATION

Short Name:DEV::PCS1G_LB_CFG

Bit	Name	Access	Description	Default
4	RA_ENA [DBG]	R/W	Enable rate adaption capability in PCS receive direction explicitly (required when PHY data looped back within MAC) 1: Enable	0x0
1	GMII_PHY_LB_ENA [DBG]	R/W	Loops data in PCS (GMII side) from ingress direction to egress direction. Rate adaption is automatically performed in a FIFO within the PCS. 1: GMII Loopback Enabled	0x0
0	TBI_HOST_LB_ENA	R/W	Loops data in PCS (TBI side) from egress direction to ingress direction. The Rx clock is automatically set equal to the Tx clock. 1: TBI Loopback Enabled	0x0

TABLE C-4: SERDES6G COMMON CFG

Short Name:MACRO_CTRL::SERDES6G_COMMON_CFG

Bit	Name	Access	Description	Default
16	SYS_RST	R/W	System reset (low active). Should be set after SERDES6G_ COMMON_CFG.ENA_LANE is set to 1. 0: Apply reset (not self-clearing) 1: Reset released (Mission mode)	0x0
15	SE_AUTO_SQUELCH_ENA	R/W	Enable auto-squelching for sync. Ethernet clock output. When set, the clock output will stop toggling (keep its last value constantly) - when PCS loses link synchrony. 0: Disable 1: Enable	0x0
14	ENA_LANE	R/W	Enable lane 0: Disable lane 1: Enable line	0x0
13	PWD_RX [DBG]	R/W	Power-down RX-path 0: Normal mode 1: Power Down mode	0x0
12	PWD_TX [DBG]	R/W	Power-down TX-path 0: Normal mode 1: Power Down mode	0x0
11:9	LANE_CTRL [DBG]	R/W	Hidden spare bits (not connected internally yet)	0x0
8	ENA_DIRECT [DBG]	R/W	Enable direct line 0: Disable 1: Enable	0x0
7	ENA_ELOOP	R/W	Enable equipment loop 0: Disable 1: Enable	0x0

TABLE C-4: SERDES6G COMMON CFG (CONTINUED)

Short Name:MACRO_CTRL::SERDES6G_COMMON_CFG

Bit	Name	Access	Description	Default
6	ENA_FLOOP	R/W	Enable facility loop. When enabling this loop, the phase alignment in the serializer has to be enabled and configured adequately. SERDES6G_SER_CFG.SER_ENALI must be set to 1. SERDES6G_SER_CFG.SER_ALISELmust be set to 0. 0: Disable 1: Enable	0x0
5	ENA_ILOOP [DBG]	R/W	Enable input loop 0: Disable 1: Enable	0x0
4	ENA_PLOOP [DBG]	R/W	Enable pad loop 0: Disable 1: Enable	0x0
3	HRATE	R/W	Enable half rate 0: Disable 1: Enable	0x0
2	QRATE	R/W	Enable quarter rate 0: Disable 1: Enable	0x1
1:0	IF_MODE	R/W	Interface mode 0: 8-bit mode 1: 10-bit mode 2: 16-bit mode 3: 20-bit mode	0x1

TABLE C-5: SERDES6G SERIALIZER CFG

Short Name:MACRO_CTRL::SERDES6G_SER_CFG

Bit	Name	Access	Description	Default
8	SER_4TAP_ENA [DBG]	R/W	Enable the fourth cml output Q3 for POST1 input of OB8G 0: Disable 4th output 1: Enable 4th output	0x0
7	SER_CPMD_SEL [DBG]	R/W	Select source of cp/md signals 0: Phase alignment block 1: Core	0x0
6	SER_SWAP_CPMD [DBG]	R/W	Swap cp/md signals 0: Disable swapping 1: Enable swapping	0x0
5:4	SER_ALISEL	R/W	Select reference clock source for phase alignment 00: RXCLKP (for Facility Loop mode) 01: RefClk15MHz (for XAUI/RXAUI) 10: RXCLKN (debug) 11: ext. ALICLK (debug)	0x0
3	SER_ENHYS	R/W	Enable hysteresis for phase alignment 0: Disable hysteresis 1: Enable hysteresis	0x0

TABLE C-5: SERDES6G SERIALIZER CFG (CONTINUED)

Short Name:MACRO_CTRL::SERDES6G_SER_CFG

Bit	Name	Access	Description	Default
2	SER_BIG_WIN [DBG]	R/W	Use wider window for phase alignment 0: Use small-window 1: Use wide window	0x0
1	SER_EN_WIN	R/W	Enable window for phase alignment 0: Disable window 1: Enable window	0x0
0	SER_ENALI	R/W	Enable phase alignment 0: Disable phase alignment 1: Enable phase alignment (required for MLD-modes - XAUI/RXAUI - and Facility Loop mode)	0x0

TABLE C-6: SD10G65 OB CONFIGURATION REGISTER 0

Short Name:SD10G65::SD10G65_OB_CFG0

Bit	Name	Access	Description	Default
23	SER_INV	R/W	Invert input to serializer	0x0
22:21	CLK_BUF_CMV	R/W	Control of common-mode voltage of clock buffer between synthesizer and OB	0x0
20:19	OB_SPARE_POOL [DBG]	R/W	Pool of spare bits for use in late design changes	0x0
18	BYP_D [DBG]	R/W	Bypass data path (for example, for JTAG), allows to drive output when EN_DIRECT = 1 and EN_OB = 1	0x0
17	RST	R/W	Set digital part into pseudo reset	0x0
16	EN_PAD_LOOP	R/W	Enable pad loop	0x0
15	EN_INP_LOOP	R/W	Enable input loop	0x0
14	EN_DIRECT	R/W	Enable direct path	0x0
13	EN_OB	R/W	Enable output buffer and serializer	0x0
8	INCR_LEVN	R/W	Selects amplitude range controlled via levn. See description of levn.	0x1
7:5	SEL_IFW	R/W	Interface width 0: 8 1: 10 2: 16 3: 20 4: 32 5: 40 6-7: Reserved	0x4
4:0	LEVN	R/W	Amplitude control value. Step size is 25 mVpp, decreasing amplitude with increasing control value. Range depends on incr_levn. Coding for incr_levn = 0: 31: 500 mVpp, 30: 525 mVpp, 29: 550 mVpp, ..., 0: 1275 mVpp. Coding for incr_levn = 1: 31: 300 mVpp, 30: 325 mVpp, 29: 350 mVpp, .., 0: 1075 mVpp. **Note:** The maximum achievable amplitude depends on the supply voltage.	0x07

TABLE C-7: SD10G65 IB CONFIGURATION REGISTER 0

Short Name:SD10G65::SD10G65_IB_CFG0

Bit	Name	Access	Description	Default
30:27	IB_RCML_ADJ	R/W	Offset resistance adjustment for CML cells (two-complement) 1000: –8 1111: –1 0000: 0 0111: 7	0x0
26:23	IB_TERM_V_SEL	R/W	Select termination voltage	0x8
22	IB_TERM_VDD_ENA	R/W	Enable common-mode termination 0: No common mode termination (only AC-common-mode termination) 1: Termination to VDDI	0x0
21	IB_RIB_SHIFT	R/W	Shifts resistance adjustment value ib_rib_adj by +1	0x0
20:17	IB_RIB_ADJ	R/W	Offset resistance adjustment for termination (two-complement)	0x0
15	IB_DIRECT_ENA [DBG]	R/W	Is OR'ed to the primary input of the macro and is used to enable the direct data path.	0x0
14	IB_DFE_ENA	R/W	Enable DFE stage (gates IB_ISEL_DFE)	0x0
13:12	IB_SIG_SEL	R/W	Select input buffer input signal 0: Normal operation 1: –6 dB input 2: OB to IB data loop or test signal 3: RESERVED	0x0
11	IB_VBULK_SEL	R/W	Controls Bulk Voltage of High Speed Cells 0: High 1: Low (Mission mode)	0x1
10	IB_IA_ENA	R/W	Enable for IA including ACJtag	0x1
9	IB_IA_SDET_ENA	R/W	Enable for IA signal detect circuit (IB_SDET_SEL = 0 required)	0x0
8	IB_IE_SDET_ENA	R/W	Enable for IA signal detect circuit (IB_SDET_SEL = 1 required)	0x0
7	IB_LD_ENA	R/W	Enable for level detect circuit	0x0
6	IB_1V_ENA	R/W	Enable for 1V mode 0: VDDI = 1.2V 1: VDDI = 1.0V	0x0
5	IB_CLKDIV_ENA	R/W	Enable clock dividers in sampling stag 0: Disable (use in Double Rate mode) 1: Enable (use in Full Rate mode)	0x0
4	IB_SPARE_POOL2 [DBG]	R/W	Routed to analog macro but not used inside. Vscope clock source is selected via ib_sel_vclk.	0x0
3	IB_VSCOPE_ENA	R/W	Enable VScope Path of Sampling-Stage	0x0
2	IB_SAM_ENA	R/W	Enable Sampling stage 1: Enable (Normal Mission mode)	0x0
1	IB_EQZ_ENA	R/W	Enable Equalization stage 1: Enable (Normal Mission mode)	0x0

TABLE C-8: SD10G65 IB CONFIGURATION REGISTER 3

Short Name:SD10G65::SD10G65_IB_CFG3

Bit	Name	Access	Description	Default
31:30	IB_LDSD_DIVSEL	R/W	Dividing factor for SDET and LD circuits of IE. 0: 128 1: 32 2: 8 3: 4	0x1
29:27	IB_SDET_CLK_DIV	R/W	Clock dividing factor for Signal Detect circuit of IA 0: 2 ... 7: 256	0x5
26	IB_SET_SDET	R/W	Force Signal-Detect output to high level 0: Normal operation 1: Force sigdet high	0x0
24	IB_SDET_SEL	R/W	Selects source of signal detect (ib_X_sdet_ena must be enabled accordingly) 0: IA 1: IE	0x0
23	IB_DIRECT_SEL	R/W	Selects source of direct data path to core 0: IE 1: IA	0x0
22:17	IB_EQ_LD1_OFFSET	R/W	With APC-enabled level offset (6-bit-signed) compared to IB_EQ_LD0_LEVEL for Level-Detect circuitry 1. Saturating between 20 mV and 340 mV. See also note in register description. 0: No offset 1: +5 mV 31: +155 mV 63(= –1): –5 mV 32(= –32): –160 mV	0x00
16:11	IB_EQ_LD0_LEVEL	R/W	Level for Level-Detect circuitry 0 0: 20 mV 1: 25 mV ... 40: 220 mV ... 63: 340 mV	0x28
10:5	IB_IE_SDET_LEVEL	R/W	Threshold value for IE Signal-Detect. 0: 20mV 1: 25mV 2: 30mV ... 63: 340mV	0x02

Note 1: Configuration register 1 for SD10G65 IB. The behavior of IB_EQ_LD1_OFFSET changes when APC is disabled. In this case, IB_EQ_LD1_OFFSET directly controls the level for Level-Detect circuitry 1. Coding: 0: 20 mV, 1: 25 mV, ... 63: 340 mV.

TABLE C-8: SD10G65 IB CONFIGURATION REGISTER 3 (CONTINUED)

Short Name:SD10G65::SD10G65_IB_CFG3

Bit	Name	Access	Description	Default
4:0	IB_IA_SDET_LEVEL	R/W	Threshold value for IA Signal-Detect 0: 0 mV ...8: 80 mV ... 31: 310 mV	0x08

Note 1: Configuration register 1 for SD10G65 IB. The behavior of IB_EQ_LD1_OFFSET changes when APC is disabled. In this case, IB_EQ_LD1_OFFSET directly controls the level for Level-Detect circuitry 1. Coding: 0: 20 mV, 1: 25 mV, ... 63: 340 mV.

TABLE C-9: SD10G65 IB CONFIGURATION REGISTER 10 JTAG RELATED SETTING

Short Name:SD10G65::SD10G65_IB_CFG10

Bit	Name	Access	Description	Default
31	IB_IA_DOFFS_CAL	R/O	Data offset calibration result IA stage	0x0
30	IB_IS_DOFFS_CAL	R/O	Data offset calibration result IS stage	0x0
29	IB_IE_SDET_PEDGE	R/O	Detection of toggling signal at PADP and PADN	0x0
28	IB_IE_SDET_NEDGE	R/O	Detection of toggling signal at PADP and PADN	0x0
27	IB_IE_SDET	R/O	Result signal detect of IE stage	0x0
26	IB_IA_SDET	R/O	Result signal detect of IA stage	0x0
25	IB_EQZ_LD1_PEDGE	R/O	Result of Level-Detect1 (after ES2-stage of EQZ) 1: Input level above threshold by IB_EQ_LD_LEV	0x0
24	IB_EQZ_LD1_NEDGE	R/O	Result of Level-Detect1 (after ES2-stage of EQZ) 1: Input level above threshold by IB_EQ_LD_LEV	0x0
23	IB_EQZ_LD0_PEDGE	R/O	Result of Level-Detect0 (after IB-stage of EQZ) 1: Input level above threshold by IB_EQ_LD_LEV	0x0
22	IB_EQZ_LD0_NEDGE	R/O	Result of Level-Detect0 (after IB-stage of EQZ) 1: Input level above threshold by IB_EQ_LD_LEV	0x0
21	IB_IE_DIRECT_DATA	R/O	Direct Data output from IE block	0x0
20	IB_IA_DIRECT_DATA	R/O	Direct Data output from IA block	0x0
17	IB_LOOP_REC	R/W	Receive enable for BiDi loop (a.k.a. PAD loop o. TX to RX loop). Is OR'ed with primary input: ib_pad_loop_ena_i. Disable test generator 'ib_tstgen_ena" if input loop is used.	0x0
16	IB_LOOP_DRV	R/W	Drive enable for BiDi loop (a.k.a. Input loop o. RX to TX loop). Is OR'ed with primary input: ib_inp_loop_ena_i. Is overruled by PAD loop.	0x0
10	IB_JTAG_OUT_P	R/O	JTAG debug p-output	0x0
9	IB_JTAG_OUT_N	R/O	JTAG debug n-output	0x0

TABLE C-9: SD10G65 IB CONFIGURATION REGISTER 10 JTAG RELATED SETTING (CONTINUED)

Bit	Name	Access	Description	Default
8:4	IB_JTAG_THRES	R/W	JTAG debug threshold 0: 0 mV 1: 10 mV 31: 310 mV	0x08
3	IB_JTAG_IN_P	R/W	JTAG debug p-input	0x0
2	IB_JTAG_IN_N	R/W	JTAG debug n-input	0x0
1	IB_JTAG_CLK	R/W	JTAG debug clock	0x0
0	IB_JTAG_ENA	R/W	JTAG debug enable	0x0

APPENDIX D: PRBS REGISTER DESCRIPTION

TABLE D-1: SERDES1G DFT CONFIGURATION REGISTER 0

Short Name: MACRO_CTRL::SERDES1G_DFT_CFG0

Bit	Name	Access	Description	Default
31	LAZYBIT [DBG]	R/W	Lazy designers spare bit	0x0
23	INV_DIS [DBG]	R/W	Disable output inverter of BIST PRBS generator	0x0
21:20	PRBS_SEL [DBG]	R/W	Select PRBS pattern for BIST 0: G(x) = x^7 + x^6 + 1 1: G(x) = x^15 + x^14 + 1 2: G(x) = x^23 + x^18 + 1 3: G(x) = x^31 + x^28 + 1	0x0
18:16	TEST_MODE [DBG]	R/W	Selection of Test mode 0: Normal operation 1: BIST 2: Fixed pattern 3: Random pattern 4-7: Reserved	0x0
4	RX_PHS_CORR_DIS [DBG]	R/W	Disable influence of external phase correction on step controller 0: Enable 1: Disable	0x0
3	RX_PDSENS_ENA [DBG]	R/W	Enable sensitivity for phase detector CP/MD (RX-Path) 0: Off 1: On	0x0
2	RX_DFT_ENA [DBG]	R/W	General enable for Jitter-Injection/Frequency-Offset-Generation Block (RX-Path) 0: Off 1: On	0x0
0	TX_DFT_ENA [DBG]	R/W	General enable for Jitter-Injection/Frequency-Offset-Generation Block (TX-Path) 0: Off 1: On	0x0

TABLE D-2: SERDES1G TEST PATTERN CONFIGURATION

Short Name: MACRO_CTRL::SERDES1G_TP_CFG

Bit	Name	Access	Description	Default
19:0	STATIC_PATTERN [DBG]	R/W	Static pattern transferred in fixed pattern test mode; LSB is transferred first.	0x00000

Note 1: These bits (pattern) are used when Lane_Test_cfg. Test_mode is set to 2 (fixed pattern).

TABLE D-3: SERDES6G DFT CONFIGURATION REGISTER 0

Short Name:MACRO_CTRL::SERDES6G_DFT_CFG0

Bit	Name	Access	Description	Default
31	LAZYBIT [DBG]	R/W	Lazy designers spare bit	0x0
23	INV_DIS [DBG]	R/W	Disable output inverter of BIST PRBS generator	0x0

TABLE D-3: SERDES6G DFT CONFIGURATION REGISTER 0 (CONTINUED)

Short Name:MACRO_CTRL::SERDES6G_DFT_CFG0

Bit	Name	Access	Description	Default
21:20	PRBS_SEL [DBG]	R/W	Select PRBS pattern for BIST 0: G(x) = x^7 + x^6 + 1 1: G(x) = x^15 + x^14 + 1 2: G(x) = x^23 + x^18 + 1 3: G(x) = x^31 + x^28 + 1	0x0
18:16	TEST_MODE [DBG]	R/W	Selection of Test mode 0: Normal operation 1: BIST 2: Fixed pattern 3: Random pattern 4: Jitter injection 5-7: Reserved	0x0
4	RX_PHS_CORR_DIS [DBG]	R/W	Disable influence of external phase correction on step controller 0: Enable 1: Disable	0x0
3	RX_PDSENS_ENA [DBG]	R/W	Enable sensitivity for phase detector CP/MD (RX-Path) 0: Off 1: On	0x0
2	RX_DFT_ENA [DBG]	R/W	General enable for Jitter-Injection/Frequency-Offset-Generation Block (RX-Path) 0: Off 1: On	0x0
0	TX_DFT_ENA [DBG]	R/W	General enable for Jitter-Injection/Frequency-Offset-Generation Block (TX-Path) 0: Off 1: On	0x0

TABLE D-4: SERDES6G DFT STATUS

Short Name:MACRO_CTRL::SERDES6G_DFT_STATUS

Bit	Name	Access	Description	Default
8	PRBS_SYNC_STAT [DBG]	R/O	PRBS synchronization status 0: PRBS checker not synchronized 1: PRBS checker synchronized	0x0
7	PLL_BIST_NOT_DONE [DBG]	R/O	RC-PLL BIST not done flag 0: BIST done 1: BIST not started or active	0x0
6	PLL_BIST_FAILED [DBG]	R/O	RC-PLL BIST result 0: No error found 1: Errors during BIST found	0x0
5	PLL_BIST_TIMEOUT_ERR [DBG]	R/O	RC-PLL BIST timeout error flag 0: No timeout occurred 1: Timeout occurred	0x0
3	BIST_ACTIVE [DBG]	R/O	BIST activity 0: BIST inactive 1: BIST active	0x0
2	BIST_NOSYNC [DBG]	R/O	BIST sync result 0: Synchronization successful 1: Synchronization on BIST data failed	0x0

TABLE D-4: SERDES6G DFT STATUS (CONTINUED)

Short Name:MACRO_CTRL::SERDES6G_DFT_STATUS

Bit	Name	Access	Description	Default
1	BIST_COMPLETE_N [DBG]	R/O	BIST completion state (low-active) 0: BIST completed 1: Not completed	0x0
0	BIST_ERROR [DBG]	R/O	BIST result 0: No error found 1: Errors during BIST found	0x0

TABLE D-5: SERDES6G ERROR COUNTER

Short Name: MACRO_CTRL::SERDES6G_ERR_CNT

Bit	Name	Access	Description	Default
15:0	PRBS_ERR_CNT [DBG]	R/O	PRBS error counter	0x0000

TABLE D-6: PCS1G LOOPBACK CONFIGURATION

Short Name: DEV::PCS1G_LB_CFG

Bit	Name	Access	Description	Default
4	RA_ENA [DBG]	R/W	Enable rate adaption capability in PCS receive direction explicitly (required when PHY data looped back within MAC)	0x0
1	GMII_PHY_LB_ENA [DBG]	R/W	Loops data in PCS (GMII side) from ingress direction to egress direction. Rate adaption is automatically performed in a FIFO within the PCS.	0x0
0	TBI_HOST_LB_ENA	R/W	Loops data in PCS (TBI side) from egress direction to ingress direction. The Rx clock is automatically set equal to the Tx clock.	0x0

TABLE D-7: SD10G65 DFT TX MAIN CONFIGURATION REGISTERS

Short Name: SD10G65_DIG::DFT_TX_CFG

Bit	Name	Access	Description	Default
12	RST_ON_STUCK_AT_CFG	R/W	Enables (1) reset of PRBS generator in case of unchanged data (“stuck-at”) for at least 511 clock cycles. Can be disabled (0), for example, in Scrambler mode to avoid the very rare case that input patterns allow to keep the generator’s shift register filled with a constant value.	0x1
11:9	TX_WID_SEL_CFG	R/W	Selects SER interface width 0: 8 1: 10 2: 16 3: 20 4: 32 5: 40 (default)	0x5

TABLE D-7: SD10G65 DFT TX MAIN CONFIGURATION REGISTERS (CONTINUED)

Short Name: SD10G65_DIG::DFT_TX_CFG

Bit	Name	Access	Description	Default
8:6	TX_PRBS_SEL_CFG	R/W	Selects PRBS generator 0: prbs7 1: prbs15 2: prbs23 3: prbs11 4: prbs31 (default) 5: prbs9	0x4
5	SCRAM_INV_CFG	R/W	Inverts the scrambler output	0x0
4	IPATH_CFG	R/W	Selects PRBS generator input 0: pat-gen 1: core	0x1
3:2	OPATH_CFG	R/W	Selects DFT-TX output 0: PRBS/scrambler (default) 1: Bypass 2: Clock pattern generator	0x0
1	TX_WORD_MODE_CFG	R/W	Word width of constant pattern generator 0: Bytes mode 1: 10-bits word mode	0x0
0	DFT_TX_ENA	R/W	Enable TX DFT capability 0: Disable DFT 1: Enable DFT	0x0

TABLE D-8: SD10G65 DFT RX MAIN CONFIGURATION REGISTER

SD10G65_DIG::DFT_RX_CFG

Bit	Name	Access	Description	Default
27	STUCK_AT_PAR_MASK_CFG	R/W	Disables error generation based on stuck_at_par errors 0: stuck_at_par error generates 63 errors per clock cycle (in PRBS mode only) 1: stuck_at_par error does not generate errors	0x1
26	STUCK_AT_01_MASK_CFG	R/W	Disables error generation based on stuck_at_01 errors 0: stuck_at_01 error generates 63 errors per clock cycle (in PRBS mode only) 1: stuck_at_01 error does not generate errors	0x0
25	DIRECT_THROUGH_ENA_CFG	R/W	Enables data through from gearbox to gear-box	0x0
24	ERR_CNT_CAPT_CFG	R/W	Captures data from error counter to allow reading of stable data	0x0
23:22	RX_DATA_SRC_SEL	R/W	Data source selection **0: Main path** 1: Vscope high path 2: Vscope low path	0x0
21:20	BIST_CNT_CFG	R/W	States in which error counting is enabled 3: All but IDLE **2: check** 1: stable+check 0: wait_stable+stable+check	0x0

TABLE D-8: SD10G65 DFT RX MAIN CONFIGURATION REGISTER (CONTINUED)

SD10G65_DIG::DFT_RX_CFG

Bit	Name	Access	Description	Default
19	FREEZE_PATTERN_CFG	R/W	Disable change of stored patterns (for example, to avoid changes during read-out)	0x0
18	CHK_MODE_CFG	R/W	Selects pattern to check 0: PRBS pattern 1: Constant pattern	0x0
17:15	RX_WID_SEL_CFG	R/W	Selects DES interface width 0: 8 1: 10 2: 16 3: 20 4: 32 5: 40 (default)	0x5
14	RX_WORD_MODE_CFG	R/W	Pattern generator: 0: Bytes mode 1: 10-bits word mode	0x0
13:11	RX_PRBS_SEL_CFG	R/W	Selects PRBS check 0: prbs7 1: prbs15 2: prbs23 3: prbs11 4: prbs31 (default) 5: prbs9	0x4
10	INV_ENA_CFG	R/W	Enables PRBS checker input inversion	0x0
9	CMP_MODE_CFG	R/W	Selects Compare mode 0: Compare mode possible 1: Learn mode is forced	0x0
8:6	LRN_CNT_CFG	R/W	Number of consecutive errors/non-errors before transitioning to respective state value = num-40-bits-words + 1	0x0
5	CNT_RST	R/W	SW reset of error counter; rising edge activates reset.	0x0
4:3	CNT_CFG	R/W	Selects modes in which error counter is active 0: Learn and Compare mode 1: Transition between modes 2: Learn mode 3: Compare mode	0x0
2:1	BIST_MODE_CFG	R/W	BIST mode 0: Off 1: BIST 2: BER 3: CONT (Infinite mode)	0x0
0	DFT_RX_ENA	R/W	Enable RX DFT capability 0: Disable DFT 1: Enable DFT	0x0

TABLE D-9: DFT BIST CONFIGURATION 0

Short Name:SD10G65_DIG::DFT_BIST_CFG0
BIST configuration register for SD10G65 DFT controlling “Check and Wait-Stable” mode. The length of a “40-bit clock cycle” is defined by 40 divided by the chosen bit rate per second.

Bit	Name	Access	Description	Default
31:16	WAKEUP_DLY_CFG	R/W	BIST FSM: Threshold to leave DOZE state N: time = (N+1) 40-bit clock cycles	0x0000
15:0	MAX_BIST_FRAMES_CFG	R/W	BIST FSM: Threshold to enter FINISHED state (refer to cfg field frame_len_cfg) N: time = (N+1) * (frame_len_cfg+1) 40-bit clock cycles	0x0000

TABLE D-10: DFT BIST CONFIGURATION 1

Short Name:SD10G65_DIG::DFT_BIST_CFG1
BIST configuration register for SD10G65 DFT controlling “Stable” mode. The length of a “40-bit clock cycle” is defined by 40 divided by the chosen bit rate per second.

Bit	Name	Access	Description	Default
31:16	MAX_UNSTABLE_CYC_CFG	R/W	BIST FSM: Threshold to iterate counter for max_stable_attempts N: attempts = (N+1)	0x0000
15:0	STABLE_THRES_CFG	R/W	BIST FSM: Threshold to enter CHECK state N: time = (N+1) 40-bit clock cycles	0x0000

TABLE D-11: DFT BIST CONFIGURATION 2

Short Name:SD10G65_DIG::DFT_BIST_CFG2
BIST configuration register for SD10G65 DFT controlling frame length in “Check” mode.

Bit	Name	Access	Description	Default
31:0	FRAME_LEN_CFG	R/W	BIST FSM: Threshold to iterate counter for max_bist_frames (refer to cfg field max_bist_frames_cfg) N: multiplier = (N+1)	0x00000000

TABLE D-12: DFT BIST CONFIGURATION 3

Short Name:SD10G65_DIG::DFT_BIST_CFG3
BIST configuration register for SD10G65 DFT controlling stable attempts in “Wait-Stable” mode.

Bit	Name	Access	Description	Default
31:0	MAX_STABLE_ATTEMPTS_CFG	R/W	BIST FSM: threshold to enter SYN-C_ERR state N: attempts = (N+1)	0x00000000

D.1 DFT Status Registers

TABLE D-13: DFT ERROR STATUS REGISTER

Short Name:SD10G65_DIG::DFT_ERR_STAT

Bit	Name	Access	Description	Default
31:0	ERR_CNT	R/O	Counter output depending on cnt_cfg	0x00000000

TABLE D-14: DFT PRBS STATUS REGISTER

Short Name:SD10G65_DIG::DFT_PRBS_STAT
Status register for SD10G65 DFT containing the PRBS data related to 1st sync lost event

Bit	Name	Access	Description	Default
31:0	PRBS_DATA_STAT	R/O	PRBS data after first sync lost	0x00000000

TABLE D-15: DFT MISCELLANEOUS STATUS REGISTER

Short Name:SD10G65_DIG::DFT_MAIN_STAT

Bit	Name	Access	Description	Default
17:8	CMP_DATA_STAT	R/O	10 bits data word at address “read_addr_cfg” used for further observation by SW	0x000
5	STUCK_AT_PAR	R/O	Data input is unchanged for all 40 parallel bits for at least seven clock cycles (defined by c_STCK_CNT_THRES)	0x0
4	STUCK_AT_01	R/O	Data input is constantly 0 or constantly 1 for all 40 parallel bits for at least seven clock cycles (by c_STCK_CNT_THRES)	0x0
3	NO_SYNC	R/O	BIST: no sync found since BIST enabled	0x0
2	INSTABLE	R/O	BIST: input data not stable	0x0
1	INCOMPLETE	R/O	BIST not complete (that is, not reached stable state or following)	0x0
0	ACTIVE	R/O	BIST is active (that is, left DOZE but did not enter a final state)	0x0

TABLE D-16: PCS CONFIGURATION

Short Name:PCS_10GBASE_R::PCS_CFG
Configuration register

Bit	Name	Access	Description	Default
31	PCS_ENA	R/W	Global PCS Enable/Disable configuration bit 0 = Disable PCS 1 = Enable PCS	0x0
30	PMA_LOOPBACK_ENA	R/W	Enable PMA loopback operation. When set, Transmit PMA data is looped back to Receive PMA data 0 = Normal mode 1 = Loopback Tx PMA to Rx PMA	0x0
29:24	SH_CNT_MAX [DBG]	R/W	Number of sync headers required for block lock. The actual number used is this number plus 1. That is, entering 63 implies a value of 64. Binary number.	0x3F
18	RX_DATA_FLIP	R/W	Flip the data bus bits at the WIS/PMA interface such that bit 63 is mapped to bit 0 and bit 0 to 63. That is, the output bus (63 down to 0) is remapped to (0 to 63) and bit 63 is the first bit. 0: No flip (LSB first) 1: Flip bus (MSB first)	0x0

TABLE D-16: PCS CONFIGURATION (CONTINUED)

Short Name:PCS_10GBASE_R::PCS_CFG
Configuration register

Bit	Name	Access	Description	Default
15	RESYNC_ENA [DBG]	R/W	Force resynchronization of receive logic. When asserted, the receive sync state machine is forced into the LOCK_INIT state and block_lock is lost. 0: Normal operation 1: Reset synchronization	0x0
14	LF_GEN_DIS [DBG]	R/W	Disable RX local fault generation when no alignment has been reached. 0: Output local fault symbol at XGMII when not aligned 1: Output IDLE symbols at XGMII when not aligned	0x0
13	RX_TEST_MODE	R/W	Enable test pattern checking mode. 0: Normal operation 1: Test pattern mode	0x0
12	RX_SCR_DISABLE [DBG]	R/W	Disable the descrambler. When disabled, the data is passed through without being descrambled. 0: Descrambler active 1: Descrambler disabled	0x0
7	TX_DATA_FLIP	R/W	Flip the data bus bits at the WIS/PMA interface such that bit 63 is mapped to bit 0 and bit 0 to 63. That is, the output bus (63 down to 0) is remapped to (0 to 63) and bit 63 is the first bit. 0: No flip (LSB first) 1: Flip bus (MSB first)	0x0
6	AN_LINK_CTRL_ENA	R/W	Enable link control using backplane Ethernet ANEG (Auto-Negotiation) 0: Disable link control 1: Enable link control	0x0
4	TX_TEST_MODE	R/W	Enable test pattern generation mode 0: Normal operation 1: Test pattern mode	0x0
3	TX_SCR_DISABLE [DBG]	R/W	Disable the scrambler. When disabled, the data is passed through without being scrambled. 0: Scrambler active 1: Scrambler disabled	0x0

TABLE D-17: TEST PATTERN MODE CONFIGURATION

Short Name:PCS_10GBASE_R::TEST_CFG
Select test patterns when test mode is enabled

Bit	Name	Access	Description	Default
18	RX_DSBL_INV	R/W	Disables inversion of seeds and data in the pseudo-random test pattern 0: Inversion enabled 1: Inversion disabled	0x0

TABLE D-17: TEST PATTERN MODE CONFIGURATION (CONTINUED)

Short Name:PCS_10GBASE_R::TEST_CFG
Select test patterns when test mode is enabled

Bit	Name	Access	Description	Default
17:16	RX_TESTPAT_SEL	R/W	Selects the test pattern used by the test pattern checker. This register is only used if RX_TEST_MODE is active. 0: Unused 1: Pseudo random 2: PRBS31 3: User defined	0x0
5	TX_DSBL_INV	R/W	Disables inversion of seeds and data in the pseudo-random test pattern 0: Inversion enabled 1: Inversion disabled	0x0
4:2	TX_SQPW_4B	R/W	Period of square wave. Value in the register is (Period-4). Valid values of period are 4 to 11. Period = (TX_SQPW_4B+4)	0x0
1:0	TX_TESTPAT_SEL	R/W	Select the test pattern used by the test pattern generator. This register is only used if TX_TEST_MODE is active. 0: Square wave 1: Pseudo random 2: PRBS31 3: User defined	0x0

TABLE D-18: PCS STATUS

Short Name: PCS_10GBASE_R::PCS_STATUS
Contains status information from the PCS core

Bit	Name	Access	Description	Default
4	TESTPAT_MATCH	R/O	When in test pattern check mode, this bit will read 1 if the test pattern checker detects a match. When 0, the test pattern does not match. The test pattern error counts should still be used along with this register bit to determine proper test match status. The bit will read back 1 only when the test pattern is matching. This may happen even while test pattern errors are counted on other clock cycles. 0: Test pattern mismatch 1: Test pattern match	0x0
3	RX_BLOCK_LOCK	R/O	The block_lock status from the synchronization state machine 0: Not synchronized 1: Synchronized, lock obtained	0x0
0	RX_HI_BER	R/O	Set by the Rx BER state machine when a high bit-error-rate condition is detected 0: Normal BER 1: High BER	0x0

TABLE D-19: TEST PATTERN MODE ERROR COUNTS

Short Name:PCS_10GBASE_R::TEST_ERR_CNT
Count of the errors detected in test pattern mode

Bit	Name	Access	Description	Default
31:0	TEST_ERR_CNT	R/W	Count of detected test pattern errors in Rx test pattern checker. Write 0 to clear.	0x00000000

TABLE D-20: TX ERRORED BLOCK COUNTER

Short Name:PCS_10GBASE_R::TX_ERRBLK_CNT
Count of the Tx errored blocks

Bit	Name	Access	Description	Default
31:0	TX_ERRBLK_CNT	R/W	Count of the error Tx blocks	0x00000000

TABLE D-21: INVALID CHARACTER COUNTER

Short Name:PCS_10GBASE_R::TX_CHARERR_CNT
Counts the number of invalid control characters

Bit	Name	Access	Description	Default
31:0	TX_CHARERR_CNT	R/W	Count of the number of invalid control characters	0x00000000

TABLE D-22: BER_COUNT

Short Name:PCS_10GBASE_R::RX_BER_CNT
ber_count from IEEE802.3 section 49.2.14.2.

Bit	Name	Access	Description	Default
4:0	RX_BER_CNT	R/W	The ber_count from the BER state machine	0x00

TABLE D-23: RX ERRORED BLOCK COUNTER

Short Name:PCS_10GBASE_R::RX_ERRBLK_CNT
Count of the Rx errored blocks

Bit	Name	Access	Description	Default
31:0	RX_ERRBLK_CNT	R/W	Count of the error Rx blocks	0x00000000

TABLE D-24: INVALID CHARACTER COUNTER

Short Name:PCS_10GBASE_R::RX_CHARERR_CNT
Counts the number of invalid control characters

Bit	Name	Access	Description	Default
31:0	RX_CHARERR_CNT	R/W	Count of the number of invalid control characters	0x00000000

APPENDIX E: OUTPUT BUFFER REGISTER DESCRIPTION

TABLE E-1: SERDES1G OUTPUT BUFFER CFG

Short Name:MACRO_CTRL::SERDES1G_OB_CFG

Bit	Name	Access	Description	Default
18:17	OB_SLP	R/W	Slope/slew rate control 0: 45 ps 1: 85 ps 2: 105 ps 3: 115 ps	0x3
16:13	OB_AMP_CTRL	R/W	Amplitude control in steps of 50 mVppd 0: 0.4 Vppd 15: 1.1 Vppd	0xC
12:10	OB_CMM_BIAS_CTRL [DBG]	R/W	CMM bias control	0x2
9	OB_DIS_VCM_CTRL [DBG]	R/W	Disable VCM control	0x0
8	OB_EN_MEAS_VREG [DBG]	R/W	Enable measure Vreg	0x0
7:4	OB_VCM_CTRL	R/W	Common-mode voltage control 0: Reserved 1: 440 mV 2: 480 mV 3: 460 mV 4: 530 mV 5: 500 mV 6: 570 mV 7: 550 mV	0x4
3:0	OB_RESISTOR_CTRL [DBG]	R/W	Resistor control. Value must be taken from RCOMP_STATUS.RCOMP. (default: +1)	0x1

TABLE E-2: SERDES6G OUTPUT BUFFER CFG 0

Short Name:MACRO_CTRL::SERDES6G_OB_CFG

Bit	Name	Access	Description	Default
31	OB_IDLE	R/W	PCIe support 1: Idle - force to 0V differential 0: Normal mode	0x0
30	OB_ENA1V_MODE	R/W	Output buffer supply voltage 1: Set to nominal 1V 0: Set to higher voltage	0x1
29	OB_POL	R/W	Polarity of output signal 0: Normal 1: Inverted	0x1
28:23	OB_POST0	R/W	Coefficients for first post-cursor (MSB is sign)	0x00
22:18	OB_PREC	R/W	Coefficients for precursor (MSB is sign)	0x00
17	OB_R_ADJ_MUX [DBG]	R/W	Resistor adjust MUX, driving strength selection of MUX 1: Reduced 0: Normal	0x0
16	OB_R_ADJ_PDR [DBG]	R/W	Resistor adjust predriver, driving strength selection of predriver 1: Reduced 0: Normal	0x0

TABLE E-2: SERDES6G OUTPUT BUFFER CFG 0 (CONTINUED)

Short Name:MACRO_CTRL::SERDES6G_OB_CFG

Bit	Name	Access	Description	Default
15:11	OB_POST1	R/W	Coefficients for second post-cursor (MSB is sign)	0x00
10	OB_R_COR [DBG]	R/W	Reduce the impedance by 3% 0: Disable 1: Enable	0x0
9	OB_SEL_RCTRL [DBG]	R/W	Select resistor control 0: Automatic mode 1: Manual mode - use ob_r_adj_mux and ob_r_adj_pdr for driving strength control	0x0
8	OB_SR_H	R/W	Half the predriver speed, use for slew rate control 0: Disable - slew rate < 60 ps 1: Enable - slew rate > 60 ps	0x1
7:4	OB_SR	R/W	Driver speed, fine adjustment of slew rate 30-60 ps (if OB_SR_H = 0), 60-140 ps (if OB_SR_H = 1). LSB is not used. 000x: ~30 ps/60 ps ... 111x: ~60 ps/140 ps	0x7
3:0	OB_RESISTOR_CTRL	R/W	Resistance adjustment for termination and CML cell regulation. This configuration defines an offset (2-complement) to the RCOMP value. The effective value is limited between 0 to 15. 7: RCOMP+7 1: RCOMP+1 0: RCOMP 15: RCOMP-1 8: RCOMP-8	0x1

TABLE E-3: SERDES6G OUTPUT BUFFER CFG 1

Short Name:MACRO_CTRL::SERDES6G_OB_CFG1
Configuration register 1 for SERDES6G output buffer

Bit	Name	Access	Description	Default
8:6	OB_ENA_CAS	R/W	Output skew, used for skew adjustment in SGMII mode - 1-bit-hot-coded 000: Non-SGMII/1 Gbps modes 001: Lowest skew 010: SGMII/1 Gbps mode 100: Highest skew All other settings: Reserved	0x0
5:0	OB_LEV	R/W	Level of output amplitude for 1V mode: max: ~48, and for 1.2V mode: max: 63 0: Lowest level 63: Highest level	0x30

TABLE E-4: SD10G65 OUTPUT BUFFER CFG 0

Short Name:SD10G65::SD10G65_OB_CFG0

Bit	Name	Access	Description	Default
23	SER_INV	R/W	Invert input to serializer	0x0
22:21	CLK_BUF_CMV	R/W	Control of common-mode voltage of clock buffer between synthesizer and OB	0x0
20:19	OB_SPARE_POOL [DBG]	R/W	Pool of spare bits for use in late design changes	0x0
18	BYP_D [DBG]	R/W	Bypass data path (for example, for JTAG), allows to drive output when EN_DIRECT = 1 and EN_OB = 1	0x0
17	RST	R/W	Set digital part into pseudo reset	0x0
16	EN_PAD_LOOP	R/W	Enable pad loop	0x0
15	EN_INP_LOOP	R/W	Enable input loop	0x0
14	EN_DIRECT	R/W	Enable direct path	0x0
13	EN_OB	R/W	Enable output buffer and serializer	0x0
8	INCR_LEVN	R/W	Selects amplitude range controlled via levn. See description of levn.	0x1
7:5	SEL_IFW	R/W	Interface width 0: 8 1: 10 2: 16 3: 20 4: 32 5: 40 6-7: Reserved	0x4
4:0	LEVN	R/W	Amplitude control value. Step size is 25 mVpp, decreasing amplitude with increasing control value. Range depends on incr_levn. Coding for incr_levn = 0: 31: 500 mVpp, 30: 525 mVpp, 29: 550 mVpp, ..., 0: 1275 mVpp. Coding for incr_levn = 1: 31: 300 mVpp, 30: 325 mVpp, 29: 350 mVpp, .., 0: 1075 mVpp. **Note:** The maximum achievable amplitude depends on the supply voltage.	0x07

TABLE E-5: SD10G65 OB CONFIGURATION REGISTER 1

Short Name:SD10G65::SD10G65_OB_CFG1

Bit	Name	Access	Description	Default
26	AB_COMP_EN	R/W	Enable amplitude compensation of AB bleed current	0x1
25:23	DIODE_CUR	R/W	Bleed current for class AB operation of driver 0: 1% 1: 0.5% 2: 2% 3: Reserved	0x0

TABLE E-5: SD10G65 OB CONFIGURATION REGISTER 1 (CONTINUED)

Short Name:SD10G65::SD10G65_OB_CFG1

Bit	Name	Access	Description	Default
22:21	LEV_SHFT	R/W	Level shift ctrl of class AB bias generator 0: 50 mV 1: 100 mV 2:150 mV 3: 200 mV	0x1
19:18	PREDRV_R_CTRL	R/W	Slew rate control of OB (R), encoding see PREDRV_C_CTRL	0x3
17:16	PREDRV_C_CTRL	R/W	Slew rate control of OB (C) C = 3 R = 3: 25 ps C = 3 R = 0: 35 ps C = 0 R = 3: 55 ps C = 1 R = 0: 70 ps C = 0 R = 0: 120 ps	0x3
15:10	VTAIL	R/W	Tail voltage driver settings 0: Reserved 1: 75 mV 2: 100 mV 4: 125 mV 8: 150 mV 16: 175 mV 32: 200 mV Intermediate values possible when setting two bits	0x02
9:5	VCAS	R/W	Ctrl of cascade volt in drv stage 0: Reserved 1: 0 2: 1/12 4: 2/12 8: 3/12 16: 4/12 Intermediate values possible when setting two bits	0x01
4	R_COR	R/W	Additional resistor calibration trim	0x0
3:0	R_I	R/W	Offset resistance adjustment for CML cells (two-complement) 1000: –8 1111: –1 0000: 0 0111: 7	0x0

TABLE E-6: SD10G65 OB CONFIGURATION REGISTER 2

Short Name:SD10G65::SD10G65_OB_CFG2

D_filter contains four 6-bit precalculated DA input values. Please note the differences in programming for various interface (IF) bit widths.

Bit	Name	Access	Description	Default
23:0	D_FILTER	R/W	Transmit filter coefficients for FIR taps. Suggested start value (no emphasis, max amplitude) 0x820820: for I/F width 8/10 bits 0x7DF820: for I/F width 16/20/32/40 bits	0x7DF820

APPENDIX F: OUTPUT BUFFER REGISTER DESCRIPTION

TABLE F-1: RCOMP CONFIGURATION 0

Short Name:MACRO_CTRL::RCOMP_CFG0

Bit	Name	Access	Description	Default
13	PWD_ENA	R/W	Enable power-down after calibration done 0: Disable power-down 1: Enable power-down	0x0
12	RUN_CAL	R/W	Start calibration 0: Idle/inactive 1: Start (activate)	0x1
11:10	SPEED_SEL	R/W	Speed selection. Setting time for analog circuit after changing resistor settings. 0: Max period 1: Max period/2 2: Max period/4 3: Max period/8	0x0
9:8	MODE_SEL	R/W	RCOMP Operation mode 0: Inactive 1: Perform calibration permanently 2: Perform calibration once 3: Perform calibration once and generate alarm if necessary	0x2
4	FORCE_ENA	R/W	Overwrite measured resistor value with value programmed in rcomp_val 0: Normal mode 1: Overwrite mode	0x0
3:0	RCOMP_VAL	R/W	Resistor comparator value 0: Maximum resistance value 15: Minimum resistance value	0x0

TABLE F-2: RCOMP STATUS

Short Name:MACRO_CTRL::RCOMP_STATUS

Bit	Name	Access	Description	Default
12	BUSY	R/O	Resistor comparison activity 0: Resistor measurement finished or inactive 1: Resistor measurement in progress	0x0
7	DELTA_ALERT	R/O	Alarm signal if rcomp is no longer the best choice 0: Inactive 1: Active	0x0
3:0	RCOMP	R/O	Measured resistor value 0: Maximum resistance value 15: Minimum resistance value	0x0

TABLE F-3: SD10G65 SBUS RX CFG SERVICE-BUS RELATED SETTING

Short Name:SD10G65::SD10G65_SBUS_RX_CFG
Configuration register for Service-Bus related setting. Note that the SBUS configuration applies for RX/TX aggregates only, and any configuration applied to SBUS_TX_CFG (output buffer cfg space) will be ignored.

Bit	Name	Access	Description	Default
19:16	SBUS_SPARE_POOL [DBG]	R/W	Pool of spare bits for use in late design changes	0x0
12	SBUS_LOOPDRV_ENA	R/W	Enable BiDi loop driver for F2DF testing	0x0
11:8	SBUS_ANAOUT_SEL	R/W	Analog test output 0: l0_ctrlspeed[0] 1: vbulk 2: nref 3: vref820m 4: vddfilt 5: vddfilt 6: ie_aout 7: ib_aout 8: ob_aout2 9: pll_frange 10: pll_srange 11: pll_vreg820m_tx 12: pll_vreg820m_rx 13: ob_aout_n 14: ob_aout_p 15: vddfilt	0x0
7	SBUS_ANAOUT_EN	R/W	Enable analog test output multiplexer	0x0
6:3	SBUS_RCOMP	R/W	Offset value for BIAS resistor calibration (2-complement) 1000: –8 1001: –7 1010: –6 1011: –5 1100: –4 1101: –3 1110: –2 1111: –1 0000: 0 0001: 1 0010: 2 0011: 3 0100: 4 0101: 5 0110: 6 0111: 7	0x0
2:1	SBUS_BIAS_SPEED_SEL	R/W	Bias speed selection 0: Below 4 Gbps 1: 4 Gbps to 6 Gbps 2: 6 Gbps to 9 Gbps 3: Above 9 Gbps	0x3
0	SBUS_BIAS_EN	R/W	Bias enable 1: Enable 0: Disable	0x0

APPENDIX G: KX AND KR ANEG REGISTER DESCRIPTION

TABLE G-1: KX ANEG CONFIGURATION

Short Name:VAUI_CHANNEL::ANEG_CFG

Bit	Name	Access	Description	Default
31	ANEG_RESET_ONE_SHOT [DBG]	One-shot	Reserved for test purposes, asynchronous reset	0x0
23	TXBYP_TESTMODE [DBG]	R/W	Reserved for test purposes	0x0
22	ATE_TESTMODE [DBG]	R/W	Reserved for test purposes	0x0
21	RX_TESTMODE [DBG]	R/W	Reserved for test purposes	0x0
20	ARB_TESTMODE [DBG]	R/W	Reserved for test purposes	0x0
16	ANEG_OB_CTRL_DIS	R/W	Disable automatic ANEG OB configuration 0: Allow ANEG block to control OB during aneg 1: OB settings are not touched by ANEG block	0x0
15	ANEG_FREQSEL_DIS [DBG]	R/W	Disable automatic ANEG speed setting 0: Allow ANEG to select frequency 1: Frequency is programmed using mode2g5_ena and hr_mode_ena	0x0
14	ANEG_PWDN_DIS [DBG]	R/W	Disable automatic power down of lane controlled by ANEG 0: Allow ANEG to power down unused lane 1: Power down is not controlled by ANEG	0x0
13:12	PD_TIMER_10GKX4 [DBG]	R/W	Parallel detect wait time for 10G using four lanes 0: 0 ms 1: 10 ms 2: 20 ms 3: 40 ms	0x1
11:10	PD_TIMER_1GKX	R/W	Parallel detect wait time for 1G using single lane 0: 0 ms 1: 10 ms 2: 20 ms 3: 40 ms	0x1
9:8	PD_TIMER_2G5	R/W	Parallel detect wait time for 2.5G using single lane 0: 0 ms 1: 10 ms 2: 20 ms 3: 40 ms	0x1
7	BLTD_ENA [DBG]	R/W	Reserved	0x0
1	RESTART_ANEG_ONE_SHOT	One-shot	Restart negotiation process 1: Restart	0x0
0	ANEG_ENA	R/W	Auto-negotiation enable 1: Enable 0: Disable	0x0

Note 1: Setting one of the parallel detect wait times to 0 disables parallel detect function for that specific mode.

TABLE G-2: KX ANEG ADVERTISED ABILITY 0

Short Name:VAUI_CHANNEL::ANEG_ADV_ABILITY_0
48 bits that contain the advertised abilities link code word for auto-negotiation (here: lower 32 bit).

Bit	Name	Access	Description	Default
31:24	ADV_ABIL_LSB	R/W	Reserved for future technology as defined in IEEE 802.3ap clause 73.	0x00
23	CAP_10GKR	R/W	Technology Ability to be advertised (here, 10GBASE-KR) 0: Do not advertise 10GB-KR capability 1: Advertise 10GB-KR capability	0x0
22	CAP_10GKX4	R/W	Technology Ability to be advertised (here, 10GBASE-KX4) 0: Do not advertise 10GB-KX4 capability 1: Advertise 10GB-KX4 capability	0x0
21	CAP_1GKX	R/W	Technology Ability to be advertised (here, 1000BASE-KX) 0: Do not advertise 1GB-KX capability 1: Advertise 1GB-KX capability	0x1
20:16	TX_NONCE	R/W	Initial value for Transmit-Nonce field	0x01
15	NP	R/W	Next page exchange desired 0: Disable NP exchange 1: Enable NP exchange	0x0
14	ACKN	R/W	Acknowledge bit (this bit is automatically overwritten by ANEG)	0x0
13	RF	R/W	RF bit (initial value)	0x0
12:10	PAUSE	R/W	Pause field	0x0
9:5	ECHOED_NONCE	R/W	Reserved for echoed nonce field (must be cleared)	0x00
4:0	SEL_FIELD	R/W	Selector field (must be 0x1)	0x01

TABLE G-3: KX ANEG ADVERTISED ABILITY 1

Short Name:VAUI_CHANNEL::ANEG_ADV_ABILITY_1
48 bits that contain the advertised abilities link code word for auto-negotiation (here: upper 16 bit).

Bit	Name	Access	Description	Default
15:14	FEC	R/W	FEC capability (bit 14: FEC ability, bit 15: FEC requested) - Only used with 10GBASE-KR	0x0
13:0	ADV_ABIL_MSB	R/W	Reserved for future technology as defined in IEEE 802.3ap clause 73.	0x0000

TABLE G-4: KX ANEG NEXT PAGE 0

Short Name:VAUI_CHANNEL::ANEG_NEXT_PAGE_0
48 bits that contain the new next page to transmit during auto-negotiation (here: lower 32 bits).

Bit	Name	Access	Description	Default
31:0	NP_TX_LSB	R/W	Lower 32 bits of next page link code word	0x00000000

TABLE G-5: KX ANEG NEXT PAGE 1

Short Name:VAUI_CHANNEL::ANEG_NEXT_PAGE_1
48 bits that contain the new next page to transmit during auto-negotiation (here: upper 16 bits).

Bit	Name	Access	Description	Default
31	NEXT_PAGE_LOADED_ONE_-SHOT	One-shot	Must be set when a new next page is programmed (self-clearing)	0x0
15:0	NP_TX_MSB	R/W	Upper 16 bits of next page link code word	0x0000

TABLE G-6: KX ANEG LINK PARTNER ADVERTISED ABILITY 0

Short Name:VAUI_CHANNEL::ANEG_LP_ADV_ABILITY_0
48 bits that contain the link partner's advertised abilities or next page information (received link code word, lower 32 bits, received during auto-negotiation). The bit groups are only valid for base pages; for next page data exchange a different bit group coding must be applied.

Bit	Name	Access	Description	Default
31:24	LP_ADV_ABIL_LSB	R/O	Bits 31 down to 24 of link code word received from link partner	0x00
23	CAP_10GKR	R/O	Technology Ability advertised by LP 0: LP is not 10GB-KR capable 1: LP is 10GB-KR capable	0x0
22	CAP_10GKX4	R/O	Technology Ability advertised by LP 0: LP is not 10GB-KX4 capable 1: LP is 10GB-KX4 capable	0x0
21	CAP_1GKX	R/O	Technology Ability advertised by LP 0: LP is not 1GB-KX capable 1: LP is 1GB-KX capable	0x0
20:16	TX_NONCE	R/O	Transmit-Nonce field (received from Link-Partner)	0x00
15	NP	R/O	Next page exchange desired by LP 0: No NP exchange desired 1: NP exchange desired	0x0
14	ACKN	R/O	Acknowledge bit (this bit is automatically overwritten by ANEG)	0x0
13	RF	R/O	RF bit	0x0
12:10	PAUSE	R/O	Pause field	0x0
9:5	ECHOED_NONCE	R/O	Echoed nonce field	0x00
4:0	SEL_FIELD	R/O	Selector field	0x00

TABLE G-7: KX ANEG LINK PARTNER ADVERTISED ABILITY 1

Short Name:VAUI_CHANNEL::ANEG_LP_ADV_ABILITY_1
48 bits that contain the link partner's advertised abilities or next page information (received link code word, upper 16 bits, received during auto-negotiation). The bit groups are only valid for base pages; for next page data exchange a different bit group coding must be applied.

Bit	Name	Access	Description	Default
15:14	FEC	R/O	FEC capability (bit 14: FEC ability, bit 15: FEC requested) - Only used with 10GBASE-KR	0x0
13:0	LP_ADV_ABIL_MSB	R/O	Bits 45 down to 32 of link code word received from link partner	0x0000

TABLE G-8: KX ANEG STATUS

Short Name:VAUI_CHANNEL::ANEG_STATUS
Auto negotiation status register

Bit	Name	Access	Description	Default
29:28	LINK_CTRL_10GKX4 [DBG]	R/O	Link control information for 10G Quad Lane mode 00: Disabled 01: Enabled 11: Scan for carrier	0x0
27:26	LINK_CTRL_1GKX [DBG]	R/O	Link control information for 1G Single Lane mode 00: Disabled 01: Enabled 11: Scan for carrier	0x0
25:24	LINK_CTRL_2G5 [DBG]	R/O	Link control information for 2.5G Single Lane mode 00: Disabled 01: Enabled 11: Scan for carrier	0x0
20	ANEG_ARB_FSM_ERR_STICKY [DBG]	Sticky	Error condition indicating an Arbitration state machine error Bit is cleared by writing a 1 to this position.	0x0
19	ANEG_RX_FSM_ERR_STICKY [DBG]	Sticky	Error condition indicating a Receive state machine error Bit is cleared by writing a 1 to this position.	0x0
18	ANEG_TX_FSM_ERR_STICKY [DBG]	Sticky	Error condition indicating a Transmit state machine error Bit is cleared by writing a 1 to this position.	0x0
17	INCOMPATIBLE_LINK	R/O	Error condition indicating that no compatible link was found	0x0
16	PAR_DETECT_FAULT_STICKY	Sticky	Error condition indicating errors during parallel detection. Bit is cleared by writing a 1 to this position.	0x0
11:8	ARBITER_STATE [DBG]	R/O	Current state of Arbiter State Machine 0000: AUTO_NEG_ENA 0001: TX_DISABLE 0010: ABILITY_DETECT 0011: ACKN_DETECT 0100: COMPLETE_ACKN 0101: AN_GOOD_CHECK 0110: AN_GOOD 0111: NEXT_PAGE_WAIT 1000: LINK_STATUS_CHECK 1001: PARALLEL_DET_FAULT 1010: PD_CHECK10GKR 1011: PD_CHECK2G5 1100: PD_CHECK1GKX 1101: PD_CHECK10GKX4	0x0
3	PAGE_RX	R/O	Status indicating whether a new page has been received	0x0
1	LP_ANEG_ABLE	R/O	Status indicating whether the link partner supports auto-negotiation	0x0
0	ANEG_COMPLETE	R/O	Status indicating whether auto-negotiation has completed	0x0

TABLE G-9: KR MODE CONTROL

Short Name:XFI_SHELL::KR_CONTROL

Bit	Name	Access	Description	Default
18:17	KR_RATE	R/O	ANEG link partner rate negotiation result (link-HCD) 0: 10G 1: 1G 2: 3G	0x0
16	KR_FEC_ENABLE	R/O	KR-ANEG FEC negotiation result 0: KR_FEC shall be disabled 1: KR_FEC shall be enabled	0x0
15	KR_INT_MASK	R/W	Global Masking of KR interrupt 0: Inhibit KR interrupt propagation 1: Enable KR interrupt	0x0
14	KR_INT_POL	R/W	Polarity of KR interrupt 0: High-active (0 is inactive level) 1: Low-active (1 is inactive level)	0x0
13	KR_RATE_INT_MASK	R/W	Masking of KR RATE interrupt 0: Inhibit KR_RATE select interrupt propagation 1: Enable KR_RATE select interrupt	0x0
12	KR_FEC_INT_MASK	R/W	Masking of KR FEC interrupt 0: Inhibit KR_FEC interrupt propagation 1: Enable KR_FEC interrupt	0x0
11	KR_MODE_INT_MASK	R/W	Masking of KR MODE interrupt 0: Inhibit KR_MODE interrupt propagation 1: Enable KR_MODE interrupt	0x0
10	KR_ANEG_RATE_STICKY	Sticky	ANEG requires KR rate selection be changed (required state see KR_FEC_ENABLE) 0: No action required 1: KR rate must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0
9	KR_ANEG_FEC_STICKY	Sticky	ANEG requires KR_FEC state be changed (required state see KR_FEC_ENABLE) 0: No action required 1: KR_FEC must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0
8	KR_ANEG_10G_STICKY	Sticky	ANEG requires SD10G65-macro (RX+TX) be setup to 10.3125G mode 0: No action required 1: Macro must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0
7	KR_ANEG_TX10G_STICKY	Sticky	ANEG requires SD10G65_TX-macro be setup to 10.3125G mode 0: No action required 1: Macro must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0

TABLE G-9: KR MODE CONTROL (CONTINUED)

Short Name:XFI_SHELL::KR_CONTROL

Bit	Name	Access	Description	Default
6	KR_ANEG_RX10G_STICKY	Sticky	ANEG requires SD10G65_RX-macro be setup to 10.3125G mode 0: No action required 1: Macro must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0
5	KR_ANEG_3G_STICKY	Sticky	ANEG requires SD10G65_-macro (RX+TX) be setup to 3.125G mode 0: No action required 1: Macro must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0
4	KR_ANEG_TX3G_STICKY	Sticky	ANEG requires SD10G65_TX-macro be setup to 3.125G mode 0: No action required 1: Macro must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0
3	KR_ANEG_RX3G_STICKY	Sticky	ANEG requires SD10G65_RX-macro be setup to 3.125G mode 0: No action required 1: Macro must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0
2	KR_ANEG_1G_STICKY	Sticky	ANEG requires SD10G65-macro (RX+TX) be setup to 1.25G mode 0: No action required 1: Macro must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0
1	KR_ANEG_TX1G_STICKY	Sticky	ANEG requires SD10G65_TX-macro be setup to 1.25G mode 0: No action required 1: Macro must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0
0	KR_ANEG_RX1G_STICKY	Sticky	ANEG requires SD10G65_RX-macro be setup to 1.25G mode 0: No action required 1: Macro must be reconfigured, SW has to clear this bit after reconfiguration (by writing a 1 to this bit-group)	0x0

APPENDIX H: LC-PLL REGISTER DESCRIPTION

TABLE H-1: PLL5G CONFIGURATION 2

Short Name:MACRO_CTRL::PLL5G_CFG2

Bit	Name	Access	Description	Default
0	ENA_GAIN_TEST [DBG]	R/W	Enable static VCO frequency stepping	0x0
1	DISABLE_FSM [DBG]	R/W	Disable automatic FSM startup frequency stepping	0x0
2	EN_RESET_FRQ_DET [DBG]	R/W	Enable FSM frequency deviation detection	0x1
3	EN_RESET_LIM_DET [DBG]	R/W	Enable FSM limiter detection	0x0
4	EN_RESET_OVERRUN [DBG]	R/W	Enable FSM frequency deviation overrun	0x1
9:5	GAIN_TEST [DBG]	R/W	Setting for static VCO frequency stepping 0: Lowest frequency 31: Highest frequency	0x08
10	DISABLE_FSM_POR [DBG]	R/W	Disables the startup FSM to start ramp-up the frequency from POR 0: Normal 1: Disable	0x0
11	FRC_FSM_POR [DBG]	R/W	Forces the startup FSM to start ramp-up the frequency by POR 0: No force 1: Force	0x0
12	ENA_AMP_CTRL_FORCE [DBG]	R/W	Enable static VCO amplitude control	0x0
13	ENA_AMPCTRL [DBG]	R/W	Enable automatic VCO amplitude control	0x1
14	PWD_AMPCTRL_N [DBG]	R/W	Force VCO amplitude control output to low (no VCO current) 0: Force 1: No force	0x1
15	ENA_CLK_BYPASS [DBG]	R/W	Enable clock bypass for all output clocks to come from ref clock pad	0x0
23:16	AMPC_SEL [DBG]	R/W	Static VCO amplitude control, active w/ ena_amp_ctrl_force 0: Lowest current 255: Highest current	0x10
24	ENA_CLK_BYPASS1 [DBG]	R/W	Enable clock bypass for all output clocks to come from extra dividers (125 MHz, 250 MHz, 312.5 MHz)	0x0
25	ENA_CP2 [DBG]	R/W	Enable resistor mode charge pump, test mode	0x0
26	ENA_RCPLL [DBG]	R/W	Enable RCPLL clock buffer in LCPLL VCO (sx_ena_vco_buf_i must be set to 0)	0x0
27	ENA_FBTESTOUT [DBG]	R/W	Enable feedback divider output to test output buffer	0x0
28	ENA_VCO_NREF_TESTOUT [DBG]	R/W	Enable VCO frequency control output	0x0
29	ENA_PFD_IN_FLIP [DBG]	R/W	Enable flip of refclk and fbclk at PFD, used for second chargepump	0x0
30	ENA_TEST_MODE [DBG]	R/W	Enables test modes, for example, fbdivsel	0x0

TABLE H-2: PLL5G STATUS 0

Short Name:MACRO_CTRL::PLL5G_STATUS0

Bit	Name	Access	Description	Default
0	LOCK_STATUS	R/O	PLL lock status 0: Not locked 1: Locked	0x0
8:1	READBACK_DATA	R/O	RCPLL Interface to read back internal data of the FSM	0x00
9	CALIBRATION_DONE	R/O	RCPLL Flag that indicates that the calibration procedure has finished	0x0
10	CALIBRATION_ERR	R/O	RCPLL Flag that indicates errors that may occur during the calibration procedure	0x0
11	OUT_OF_RANGE_ERR	R/O	RCPLL Flag that indicates a out of range condition while NOT in calibration mode	0x0
12	RANGE_LIM	R/O	RCPLL Flag range limiter signaling	0x0

TABLE H-3: PLL5G STATUS 1

Short Name:MACRO_CTRL::PLL5G_STATUS1

Bit	Name	Access	Description	Default
0	FSM_LOCK	R/O	Startup FSM lock status	0x0
3:1	FSM_STAT	R/O	Startup FSM internal status	0x0
13:4	FBCNT_DIF	R/O	VCO frequency difference to refclk	0x000
18:14	GAIN_STAT	R/O	VCO frequency step stop	0x00
26:19	SIG_DEL	R/O	Sigma delta ADC output	0x00

TABLE H-4: PLL5G CONFIGURATION 2A

Short Name: H_PLL5G_CFG2A, Address:0x8104

Bit	Name	Access	Description	Default
0	ENA_GAIN_TEST	R/W	Enable static VCO frequency stepping	0x0
1	DISABLE_FSM	R/W	Disable automatic FSM startup frequency stepping	0x0
2	EN_RESET_FRQ_DET	R/W	Enable FSM frequency deviation detection	0x1
3	EN_RESET_LIM_DET	R/W	Enable FSM limiter detection	0x0
4	EN_RESET_OVERRUN	R/W	Enable FSM frequency deviation overrun	0x1
9:5	GAIN_TEST	R/W	Setting for static VCO frequency stepping 0: Lowest frequency 31: Highest frequency	0x08
10	DISABLE_FSM_POR	R/W	Disables the startup FSM to start ramp up the frequency from POR 0: Normal 1: Disable	0x0
11	FRC_FSM_POR	R/W	Forces the startup FSM to start ramp-up the frequency by POR 0: No force 1: Force	0x0
12	ENA_AMP_CTRL_FORCE	R/W	Enable static VCO amplitude control	0x0
13	ENA_AMPCTRL	R/W	Enable automatic VCO amplitude control	0x1

TABLE H-4: PLL5G CONFIGURATION 2A (CONTINUED)

Short Name: H_PLL5G_CFG2A, Address:0x8104

Bit	Name	Access	Description	Default
14	PWD_AMPCTRL_N	R/W	Force VCO amplitude control output to low (no VCO current) 0: Force 1: No force	0x1
15	ENA_CLK_BYPASS	R/W	Enable clock bypass for all output clocks to come from ref clock pad	0x0

TABLE H-5: PLL5G STATUS 0

Short Name: H_PLL5G_STATUS0, Address:0x810d

Bit	Name	Access	Description	Default
0	LOCK_STATUS	R/O	PLL lock status 0: Not locked 1: Locked	0x0
8:1	READBACK_DATA	R/O	RCPLL Interface to read back internal data of the FSM	0x00
9	CALIBRATION_DONE	R/O	RCPLL Flag that indicates that the calibration procedure has finished	0x0
10	CALIBRATION_ERR	R/O	RCPLL Flag that indicates errors that may occur during the calibration procedure	0x0
11	OUT_OF_RANGE_ERR	R/O	RCPLL Flag that indicates an out of range condition while NOT in calibration mode	0x0
12	RANGE_LIM	R/O	RCPLL Flag range limiter signaling	0x0

TABLE H-6: PLL5G STATUS 1

Short Name: H_PLL5G_STATUS1A, Address:0x0x810e

Bit	Name	Access	Description	Default
0	FSM_LOCK	R/O	Startup FSM lock status	0x0
3:1	FSM_STAT	R/O	Startup FSM internal status	0x0
13:4	FBCNT_DIF	R/O	VCO frequency difference to refclk	0x000

TABLE H-7: PLL5G STATUS 1B

Short Name: H_PLL5G_STATUS1B, Address:0x0x810f

Bit	Name	Access	Description	Default
4:0	GAIN_STAT	R/O	VCO frequency step stop	0x00
12:5	SIG_DEL	R/O	Sigma delta ADC output	0x00

APPENDIX I: INPUT BUFFER REGISTER DESCRIPTION

TABLE I-1: SERDES1G INPUT BUFFER CONFIGURATION

Short Name:MACRO_CTRL::SERDES1G_IB_CFG

Bit	Name	Access	Description	Default
27	IB_FX100_ENA	R/W	Switches signal detect circuit into low frequency mode, must be used in FX100 mode	0x0
26:24	ACJTAG_HYST [DBG]	R/W	Hysteresis level for AC-JTAG Input 0: Low 7: High	0x1
21:19	IB_DET_LEV	R/W	Detect thresholds 0: 159-189 mVppd 1: 138-164 mVppd 2: 109-124 mVppd 3: 74-89 mVppd	0x3
14	IB_HYST_LEV	R/W	Input buffer hysteresis levels 0: 59-79 mV 1: 81-124 mV	0x0
13	IB_ENA_CMV_TERM	R/W	Enable common-mode voltage termination 0: Low termination (VDD_A x 0.7) 1: High termination (VDD_A)	0x1
12	IB_ENA_DC_COUPLING	R/W	Enable dc-coupling of input signal 0: Disable 1: Enable	0x0
11	IB_ENA_DETLEV	R/W	Enable detect level circuit 0: Disable 1: Enable	0x1
10	IB_ENA_HYST	R/W	Enable hysteresis for input signal. Hystesis can only be enabled if DC offset compensation is disabled. 0: Disable 1: Enable	0x0
9	IB_ENA_OFFSET_COMP	R/W	Enable offset compensation of input stage. This bit must be disabled to enable hysteresis (IB_ENA_HYST). 0: Disable 1: Enable	0x1
8:6	IB_EQ_GAIN	R/W	Selects weighting between AC and DC input path: 0: Reserved 1: Reserved 2: 0 dB (recommended value) 3: 1.5 dB 4: 3 dB 5: 6 dB 6: 9 dB 7: 12.5 dB	0x2
5:4	IB_SEL_CORNER_FREQ	R/W	Corner frequencies of AC path: 0: 1.3 GHz 1: 1.5 GHz 2: 1.6 GHz 3: 1.8 GHz	0x0

TABLE I-1: SERDES1G INPUT BUFFER CONFIGURATION (CONTINUED)

Short Name:MACRO_CTRL::SERDES1G_IB_CFG

Bit	Name	Access	Description	Default
3:0	IB_RESISTOR_CTRL [DBG]	R/W	Resistor control. Value must be taken from RCOMP_STATUS.RCOMP. (default: –3)	0xB

TABLE I-2: SERDES1G DESERIALIZER CONFIGURATION

Short Name:MACRO_CTRL::SERDES1G_DES_CFG

Bit	Name	Access	Description	Default
16:13	DES_PHS_CTRL	R/W	Control of phase regulator logic. Bit 3 must be set to 0. 0: Disabled 1: Enabled with 99 ppm limit 2: Enabled with 202 ppm limit 3: Enabled with 485 ppm limit 4: Enabled if corresponding PCS is in sync with 50 ppm limit 5: Enabled if corresponding PCS is in syn-with 99 ppm limit 6: Enabled if corresponding PCS is in sync with 202 ppm limit 7: Enabled if corresponding PCS is in sync with 485 ppm limit	0x6
12:11	DES_CPMD_SEL	R/W	Deserializer phase control, main CP/MD select 0: Directly from DES1: Through hysteresis stage from DES 2: From core 3: Disabled	0x0
10:8	DES_MBTR_CTRL	R/W	Des phase control for 180 degrees dead-lock block mode of operation 0: Depending on density of input pattern 1: Active until PCS has synchronized 2: Depending on density of input pattern until PCS has synchronized 3: Never 4: Always 5-7: Reserved	0x2
7:5	DES_BW_ANA	R/W	Bandwidth selection for proportional path of CDR loop 0: No division 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32 6: Divide by 64 7: Divide by 128	0x6
4	DES_SWAP_ANA [DBG]	R/W	Swap non-hysteresis CP/MD signals 0: No swapping 1: Swapping	0x0

TABLE I-2: SERDES1G DESERIALIZER CONFIGURATION (CONTINUED)

Short Name:MACRO_CTRL::SERDES1G_DES_CFG

Bit	Name	Access	Description	Default
3:1	DES_BW_HYST	R/W	Selection of time constant for integrative path of CDR loop 0: Divide by 2 1: Divide by 4 2: Divide by 8 3: Divide by 16 4: Divide by 32 5: Divide by 64 6: Divide by 128 7: Divide by 256	0x7
0	DES_SWAP_HYST [DBG]	R/W	Swap hysteresis CP/MD signals 0: No swapping 1: Swapping	0x0

TABLE I-3: SERDES6G IB CONFIGURATION REGISTER 0

Short Name:MACRO_CTRL::SERDES6G_IB_CFG

Bit	Name	Access	Description	Default
30:29	IB_SOFSI	R/W	Select location of offset correction inside equalizer 0: No offset correction 1: First stage (preferred) 2: Last stage 3: First and last stage	0x1
28	IB_VBULK_SEL	R/W	Controls Bulk Voltage of High Speed Cells 0: Reserved 1: Low (Mission mode)	0x1
27:24	IB_RTRM_ADJ	R/W	Resistance adjustment for termination and CML cell regulation. This configuration defines an offset (2-complement) to the RCOMP value. The effective value is limited between 0 to 15. 7: RCOMP+7 1: RCOMP+1 0: RCOMP 15: RCOMP-1 8: RCOMP -8	0xD
23:20	IB_ICML_ADJ	R/W	Current adjustment for CML cells 0: Low current 1: High current	0x5
19:18	IB_TERM_MODE_SEL	R/W	Select common-mode termination voltage 0: Open - recommended mission mode for DC-coupling 1: VCM ref - recommended mission mode for AC-coupling 2: VDD - used to increase amplitude in certain DC-coupled modes 3: Capacitance only - Reserved for debug test purpose	0x1

TABLE I-3: SERDES6G IB CONFIGURATION REGISTER 0 (CONTINUED)

Short Name:MACRO_CTRL::SERDES6G_IB_CFG

Bit	Name	Access	Description	Default
17:15	IB_SIG_DET_CLK_SEL	R/W	Select signal detect clock: Frequency = 125 MHz / 2**n Set to 0 for ATE testing (reduces test-time) Set to 7 for optimized performance in Mission mode	0x0
14:13	IB_REG_PAT_SEL_HP	R/W	Selects pattern detection for regulation of high-pass-gain 0: Only regulation assessment if basic pattern is detected 1: Regulation assessment if basic and simplified pattern are detected 2: Regulation assessment if basic and critical pattern are detected 3: Regulation assessment if simplified basic and critical pattern are detected	0x1
12:11	IB_REG_PAT_SEL_MID	R/W	Selects pattern detection for regulation of mid-pass-gain 0: Only regulation assessment if basic pattern is detected 1: Regulation assessment if basic and simplified pattern are detected 2: Regulation assessment if basic and critical pattern are detected 3: Regulation assessment if simplified basic and critical pattern are detected	0x1
10:9	IB_REG_PAT_SEL_LP	R/W	Selects pattern detection for regulation of low-pass-gain 0: Only regulation assessment if basic pattern is detected 1: Regulation assessment if basic and simplified pattern are detected 2: Regulation assessment if basic and critical pattern are detected 3: Regulation assessment if simplified basic and critical pattern are detected	0x2
8:7	IB_REG_PAT_SEL_OFFSET	R/W	Selects pattern detection for regulation of offset 0: Only regulation assessment if basic pattern is detected 1: Regulation assessment if basic and simplified pattern are detected 2: Regulation assessment if basic and critical pattern are detected 3: Regulation assessment if simplified basic and critical pattern are detected	0x1
6	IB_ANA_TEST_ENA	R/W	Enable analog test output 0: Disable 1: Enable	0x0
5	IB_SIG_DET_ENA	R/W	Enable signal detection 0: Disable 1: Enable	0x1

TABLE I-3: SERDES6G IB CONFIGURATION REGISTER 0 (CONTINUED)

Short Name:MACRO_CTRL::SERDES6G_IB_CFG

Bit	Name	Access	Description	Default
4	IB_CONCUR	R/W	Selection between constant current and constant resistor mode for CML cells 0: Constant Resistor mode 1: Constant Current mode	0x1
3	IB_CAL_ENA	R/W	Enable calibration IB calibration should be started after SERDES6G_COMMON_CFG.ENA_LANE is set to 1. Calibration procedure takes up to 1 second depending on configuration of SERDES6G_IB_CFG0.IB_SIG_DET_ CLK_SEL. Maximum calibration time is for SERDES6G_IB_CFG0.IB_SIG_DET_ CLK_SEL set to 7. 0: Disable 1: Enable (Mission mode)	0x0
2	IB_SAM_ENA	R/W	Enable sampling stage 0: Disable 1: Enable (Mission mode)	0x1
1	IB_EQZ_ENA	R/W	Enable equalization stage 0: Disable 1: Enable (Mission mode)	0x1
0	IB_REG_ENA	R/W	Enable equalizer regulation stage 0: Disable 1: Enable (Mission mode)	0x1

TABLE I-4: SERDES6G IB CONFIGURATION REGISTER 1

Short Name:MACRO_CTRL::SERDES6G_IB_CFG1

Bit	Name	Access	Description	Default
21:17	IB_TJTAG	R/W	Selects threshold voltage for ac-jtag Voltage = (n + 1) * 20 mV	0x08
16:12	IB_TSDET	R/W	Selects threshold voltage for signal detect Voltage = (n + 1) * 20 mV	0x10
11:8	IB_SCALY	R/W	Selects number of calibration cycles for equalizer, sampling stage, signal-detect, and AC-JTAG comparator, BIAS. 0: No calibration --> neutral values are used	0xF
7	IB_FILT_HP	R/W	Selects doubled filtering of high-pass-gain regulation or set it to hold if ib_frc_hp = 1	0x1
6	IB_FILT_MID	R/W	Selects doubled filtering of mid-pass-gain regulation or set it to hold if ib_frc_mid = 1	0x1
5	IB_FILT_LP	R/W	Selects doubled filtering of low-pass-gain regulation or set it to hold if ib_frc_lp = 1	0x1
4	IB_FILT_OFFSET	R/W	Selects doubled filtering of offset regulation or set it to hold if ib_frc_offset = 1	0x1
3	IB_FRC_HP	R/W	Selects manual control for high-pass-gain regulation if enabled	0x0
2	IB_FRC_MID	R/W	Selects manual control for mid-pass-gain regulation if enabled	0x0

TABLE I-4: SERDES6G IB CONFIGURATION REGISTER 1 (CONTINUED)

Short Name:MACRO_CTRL::SERDES6G_IB_CFG1

Bit	Name	Access	Description	Default
1	IB_FRC_LP	R/W	Selects manual control for low-pass-gain regulation if enabled	0x0
0	IB_FRC_OFFSET	R/W	Selects manual control for offset regulation if enabled	0x0

TABLE I-5: SERDES6G IB CONFIGURATION REGISTER 2

Short Name:MACRO_CTRL::SERDES6G_IB_CFG2

Bit	Name	Access	Description	Default
29:27	IB_TINFV	R/W	Selects maximum threshold influence for threshold calibration of vscope samplers 0: 40 mV 1: 80 mV ...	0x3
26:22	IB_OINFI	R/W	Selects maximum offset influence for offset regulation 0: 10 mV 1: 20 mV ...	0x1F
21:19	IB_TAUX [DBG]	R/W	Reserved	0x0
18:16	IB_OINFS	R/W	Selects maximum offset influence for offset calibration of main samplers 0: 40 mV 1: 80 mV ...	0x7
15:10	IB_OCALS	R/W	Selects offset voltage for main sampler calibration 0: –70 mV ... 31: –0 mV 32: +0 mV ... 63: 70 mV	0x20
9:5	IB_TCALV	R/W	Selects threshold voltage for VScope sampler calibration 0: 10 mV 1: 20 mV ...	0x0C
4:3	IB_UMAX	R/W	Tunes common-mode voltage to adapt to maximum voltage of input signal 0: 320 mVppd 1: 480 mVppd 2: 640 mVppd (recommended for Mission mode) 3: 800 mVppd	0x2

TABLE I-5: SERDES6G IB CONFIGURATION REGISTER 2 (CONTINUED)

Short Name:MACRO_CTRL::SERDES6G_IB_CFG2

Bit	Name	Access	Description	Default
2:0	IB_UREG	R/W	0 dB regulation voltage for high-speed-cells 0: 160 mV 1: 180 mV 2: 200 mV 3: 220 mV 4: 240 mV (recommended for Mission mode) 5: 260 mV 6: 280 mV 7: 300 mV	0x4

TABLE I-6: SERDES6G IB CONFIGURATION REGISTER 3

Short Name:MACRO_CTRL::SERDES6G_IB_CFG3

Bit	Name	Access	Description	Default
23:18	IB_INI_HP	R/W	Init force value for high-pass gain regulation	0x00
17:12	IB_INI_MID	R/W	Init force value for mid-pass gain regulation	0x1F
11:6	IB_INI_LP	R/W	Init force value for low-pass gain regulation	0x01
5:0	IB_INI_OFFSET	R/W	Init force value for offset gain regulation	0x1F

TABLE I-7: SERDES6G IB CONFIGURATION REGISTER 4

Short Name:MACRO_CTRL::SERDES6G_IB_CFG4

Bit	Name	Access	Description	Default
23:18	IB_MAX_HP	R/W	Max value for high-pass gain regulation	0x3F
17:12	IB_MAX_MID	R/W	Max value for mid-pass gain regulation	0x3F
11:6	IB_MAX_LP	R/W	Max value for low-pass gain regulation	0x02
5:0	IB_MAX_OFFSET	R/W	Max value for offset gain regulation	0x3F

TABLE I-8: SERDES6G IB CONFIGURATION REGISTER 5

Short Name:MACRO_CTRL::SERDES6G_IB_CFG5

Bit	Name	Access	Description	Default
23:18	IB_MIN_HP	R/W	Min value for high-pass gain regulation	0x00
17:12	IB_MIN_MID	R/W	Min value for mid-pass gain regulation	0x00
11:6	IB_MIN_LP	R/W	Min value for low-pass gain regulation	0x00
5:0	IB_MIN_OFFSET	R/W	Min value for offset gain regulation	0x00

TABLE I-9: SD10G65 IB CONFIGURATION REGISTER 0

Short Name:SD10G65::SD10G65_IB_CFG0

Bit	Name	Access	Description	Default
30:27	IB_RCML_ADJ	R/W	Offset resistance adjustment for CML cells (two-complement) 1000: –8 1111: –1 0000: 0 0111: 7	0x0
26:23	IB_TERM_V_SEL	R/W	Select termination voltage	0x8
22	IB_TERM_VDD_ENA	R/W	Enable common-mode termination 0: No common mode termination (only AC-common-mode termination) 1: Termination to VDDI	0x0
21	IB_RIB_SHIFT	R/W	Shifts resistance adjustment value ib_rib_adj by +1	0x0
20:17	IB_RIB_ADJ	R/W	Offset resistance adjustment for termination (two-complement) 1000: –8 1111: –1 0000: 0 0111: 7	0x0
15	IB_DIRECT_ENA [DBG]	R/W	Is OR'ed to the primary input of the macro: sx_direct_data_ena_rx_i and is used to enable the direct data path	0x0
14	IB_DFE_ENA	R/W	Enable DFE stage (gates IB_ISEL_DFE) 0: Disable 1: Enable	0x0
13:12	IB_SIG_SEL	R/W	Select input buffer input signal 0: Normal operation 1: –6 dB input 2: OB to IB data loop or test signal 3: RESERVED	0x0
11	IB_VBULK_SEL	R/W	Controls Bulk Voltage of High Speed Cells 0: High 1: Low (Mission mode)	0x1
10	IB_IA_ENA	R/W	Enable for IA including ACJtag	0x1
9	IB_IA_SDET_ENA	R/W	Enable for IA signal detect circuit (IB_SDET_SEL = 0)	0x0
8	IB_IE_SDET_ENA	R/W	Enable for IE signal detect circuit (IB_SDET_SEL = 1)	0x0
7	IB_LD_ENA	R/W	Enable for level detect circuit	0x0
6	IB_1V_ENA	R/W	Enable for 1V mode 0: VDDI = 1.2V 1: VDDI = 1.0V	0x0
5	IB_CLKDIV_ENA	R/W	Enable clock dividers in sampling stage 0: Disable (use in Double Rate mode) 1: Enable (use in Full Rate mode)	0x0
4	IB_SPARE_POOL2 [DBG]	R/W	Routed to analog macro but not used inside, Vscope clock source is selected via ib_sel_vclk.	0x0
3	IB_VSCOPE_ENA	R/W	Enable Vscope Path of Sampling-Stage	0x0

TABLE I-9: SD10G65 IB CONFIGURATION REGISTER 0 (CONTINUED)

Short Name:SD10G65::SD10G65_IB_CFG0

Bit	Name	Access	Description	Default
2	IB_SAM_ENA	R/W	Enable ampling stage	0x0
1	IB_EQZ_ENA	R/W	Enable equalization stage	0x0

TABLE I-10: SD10G65 IB CONFIGURATION REGISTER 1

Short Name:SD10G65::SD10G65_IB_CFG1

Bit	Name	Access	Description	Default
31:28	IB_AMP_L	R/W	Inductor peaking of 1. stage Input buffer 0: No peaking 15: Maximum peaking maximum peaking > 3 db at 8 GHz	0x8
27:24	IB_EQZ_L0	R/W	Inductor peaking of EQ-Buffer0 (over all 2. stage) 0: No peaking 15: Maximum peaking Maximum peaking > 3 db at 8 GHz	0x8
23:20	IB_EQZ_L1	R/W	Inductor peaking of EQ-Buffer1 (over all 3. stage) 0: No peaking 15: Maximum peaking Maximum peaking > 3 db at 8 GHz	0x8
19:16	IB_EQZ_L2	R/W	Inductor peaking of EQ-Buffer2 (over all 4. stage) 0: No peaking 15: Maximum peaking Maximum peaking > 3 db at 8 GHz	0x8
15:12	IB_AGC_L	R/W	Inductor peaking of EQ-Buffer3 (over all 5. stage) 0: No peaking 15: Maximum peaking Maximum peaking > 3 db at 8 GHz	0x8
11:9	IB_AMP_C	R/W	C-gain peaking for IB-stage 0: No peaking 7: Maximum peaking Corner frequency adjustment with ib_eqz_c_adj_ib	0x4
8:6	IB_EQZ_C0	R/W	C-gain peaking for EQ-stage0 0: No peaking 7: Maximum peaking Corner frequency adjustment with ib_eqz_c_adj_es0	0x4
5:3	IB_EQZ_C1	R/W	C-gain peaking for EQ-stage1 0: No peaking 7: Maximum peaking Corner frequency adjustment with ib_eqz_c_adj_es1	0x4
2:0	IB_EQZ_C2	R/W	C-gain peaking for EQ-stage2 0: No peaking 7: Maximum peaking Corner frequency adjustment with ib_eqz_c_adj_es2	0x4

TABLE I-11: SD10G65 IB CONFIGURATION REGISTER 2

Short Name:SD10G65::SD10G65_IB_CFG2

Bit	Name	Access	Description	Default
27:18	IB_EQZ_GAIN	R/W	Gain of Input Buffer 0-511 gain adjustment only in first stage > 511 gain in first stage at max. 512-639 gain in 2.stage increased from 1 to 2 > 639 gain = 2 640-767 gain in 3.stage increased from 1 to 2 >767 gain = 2 768-895 gain in 4.stage increased from 1 to 2 >895 gain at max.	0x040
17:10	IB_EQZ_AGC	R/W	Amplification (gain) of AGC in Input Buffer (normal operation) after gain calibration 0: Gain = 0.3 255: Gain = 1.5 if disp/disn is active dac function for dfe gain calibration	0x80
9:0	IB_EQZ_OFFSET	R/W	Offset value for IB-stage of Input Buffer 512: Neutral > 512: Positive < 512: Negative range +/- 600 mV (low gain) to +/-30 mV (high gain) gain dependent offset sensitivity required for Baseline wander compensation not supported in test chip	0x200

TABLE I-12: SD10G65 IB CONFIGURATION REGISTER 3

Short Name:SD10G65::SD10G65_IB_CFG3

Bit	Name	Access	Description	Default
31:30	IB_LDSD_DIVSEL	R/W	Dividing factor for SDET and LD circuits of IE 0: 128 1: 32 2: 8 3: 4	0x1
29:27	IB_SDET_CLK_DIV	R/W	Clock dividing factor for Signal Detect circuit of IA 0: 2 ... 7: 256	0x5
26	IB_SET_SDET	R/W	Force Signal-Detect output to high level 0: Normal operation 1: Force sigdet high	0x0
24	IB_SDET_SEL	R/W	Selects source of signal detect (ib_X_sdet_ena must be enabled accordingly) 0: IA 1: IE	0x0

TABLE I-12: SD10G65 IB CONFIGURATION REGISTER 3 (CONTINUED)

Short Name:SD10G65::SD10G65_IB_CFG3

Bit	Name	Access	Description	Default
23	IB_DIRECT_SEL	R/W	Selects source of direct data path to core 0: IE 1: IA	0x0
22:17	IB_EQ_LD1_OFFSET	R/W	With APC-enabled level offset (6-bit-signed) compared to IB_EQ_LD0_LEVEL for Level-Detect circuitry 1. Saturating between 20 mV and 340 mV. See also note in register description. 0: No offset 1: +5 mV 31: +155 mV 63(= –1): –5 mV 32(= –32): –160 mV	0x00
16:11	IB_EQ_LD0_LEVEL	R/W	Level for Level-Detect circuitry 0 0: 20 mV 1: 25 mV ... 40: 220 mV ... 63: 340 mV	0x28
10:5	IB_IE_SDET_LEVEL	R/W	Threshold value for IE Signal-Detect 0: 20 mV 1: 25 mV 2: 30 mV ... 63: 340 mV	0x02
4:0	IB_IA_SDET_LEVEL	R/W	Threshold value for IA Signal-Detect 0: 0 mV ... 8: 80 mV ... 31: 310 mV	0x08

TABLE I-13: SD10G65 IB CONFIGURATION REGISTER 4

Short Name:SD10G65::SD10G65_IB_CFG4

Bit	Name	Access	Description	Default
31:30	IB_EQZ_C_ADJ_IB	R/W	Corner frequency selection for c-gain peaking 1.stage 0: Lowest corner frequency 3: Highest corner frequency	0x2
29:28	IB_EQZ_C_ADJ_ES2	R/W	Corner frequency selection for c-gain peaking 2.stage 0: Lowest corner frequency 3: Highest corner frequency	0x2
27:26	IB_EQZ_C_ADJ_ES1	R/W	Corner frequency selection for c-gain peaking 3.stage 0: Lowest corner frequency 3: Highest corner frequency	0x2

TABLE I-13: SD10G65 IB CONFIGURATION REGISTER 4 (CONTINUED)

Short Name:SD10G65::SD10G65_IB_CFG4

Bit	Name	Access	Description	Default
25:24	IB_EQZ_C_ADJ_ES0	R/W	Corner frequency selection for c-gain peaking 4.stage 0: Lowest corner frequency 3: Highest corner frequency	0x2
23:21	IB_EQZ_L_MODE	R/W	Coder mode: APC L value to IE inductance 0: Equ. distributed (double step 3 to 4) 1: Equ. distributed (no change 6+7) 2: First buffer max - 2nd buffer max - ...	0x0
20:18	IB_EQZ_C_MODE	R/W	Coder mode: APC C value to IE capacitance 0: Equ. distributed 2: First buffer max - 2nd buffer max - ...	0x0
17:12	IB_VSCOPE_H_THRES	R/W	Threshold value (offset) for vscope-high sampling path 0: –max 31: –0 32: +0 63: +max (depending on calibration)	0x30
11:6	IB_VSCOPE_L_THRES	R/W	Threshold value (offset) for vscope-low sampling path 0: –max 31: –0 32: +0 63: +max (depending on calibration)	0x0F
5:0	IB_MAIN_THRES	R/W	Threshold value (offset) for main sampling path 0: –max 31: –0 32: +0 63: +max (depending on calibration)	0x20

TABLE I-14: SD10G65 DES CONFIGURATION REGISTER 0

Short Name:SD10G65::SD10G65_DES_CFG0

Bit	Name	Access	Description	Default
7	DES_INV_H	R/W	Invert output of high auxiliary deserializer	0x0
6	DES_INV_L	R/W	Invert output of low auxiliary deserializer	0x0
5	DES_INV_M	R/W	Invert output of main deserializer	0x0
4:2	DES_IF_MODE_SEL	R/W	Interface width 0: 8 1: 10 2: 16 (energy efficient) 3: 20 (energy efficient) 4: 32 5: 40 6: 16 bit (fast) 7: 20 bit (fast)	0x4
1	DES_VSC_DIS	R/W	Auxiliary deserializer channels disable	0x1
0	DES_DIS	R/W	Deserializer disable	0x0

TABLE I-15: SD10G65 MOEBDIV CONFIGURATION REGISTER 0

Short Name:SD10G65::SD10G65_MOEBDIV_CFG0

Bit	Name	Access	Description	Default
11:9	MOEBDIV_BW_CDR_SEL_A	R/W	Bandwidth selection for cp/md of cdr loop when core NOT flags valid data detected	0x3
8:6	MOEBDIV_BW_CDR_SEL_B	R/W	Bandwidth selection for cp/md of cdr loop when core flags valid data detected	0x3
5:3	MOEBDIV_BW_CORE_SEL	R/W	Bandwidth selection for cp/md signals towards core	0x0
2	MOEBDIV_CPMD_SWAP	R/W	CP/MD swapping	0x0
1	MOEBDIV_DIV32_ENA	R/W	MD divider enable	0x0
0	MOEBDIV_DIS	R/W	Divider disable	0x0

APPENDIX J: APPLICATION NOTE REVISION HISTORY

TABLE J-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003743A (12-01-20)	Initial release	

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