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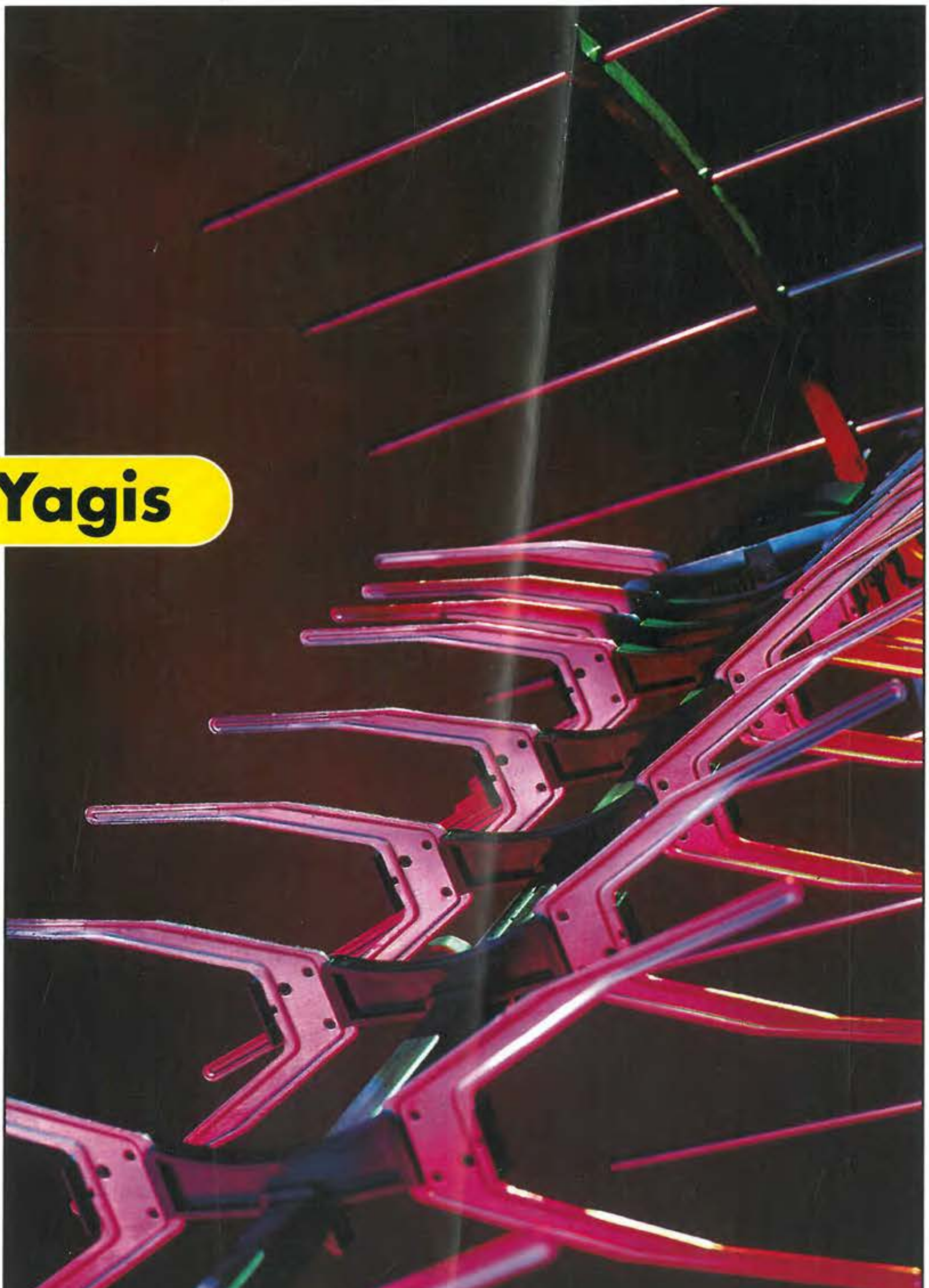

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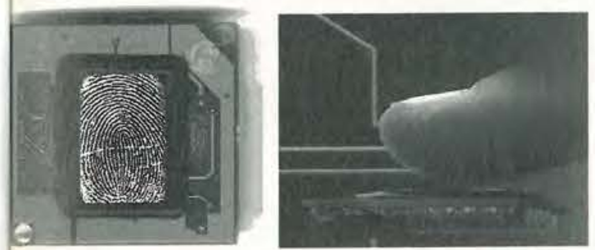
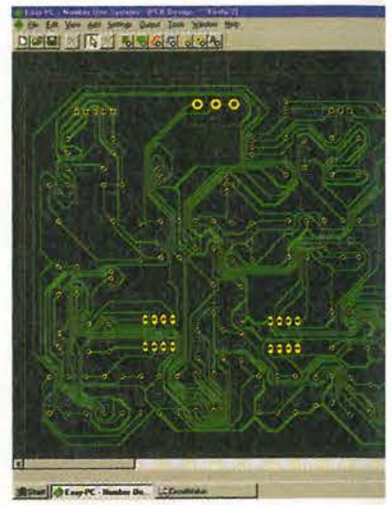


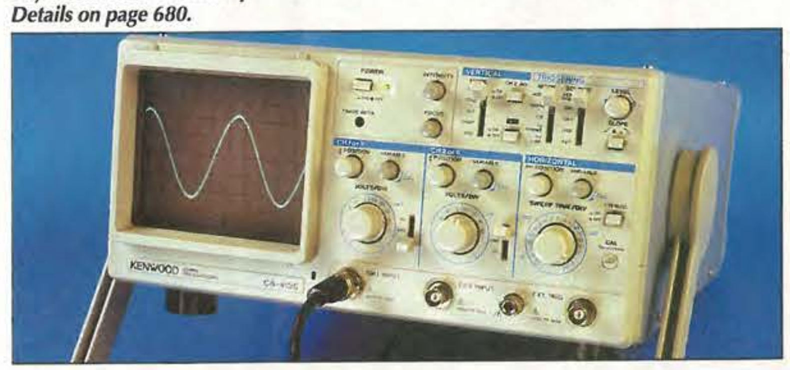
Putting a fingerprint sensor on a chip makes it not only small, but also cheap enough for high-volume applications. See page 629.



To coincide with the review in this issue, Number One Systems is offering the new Windows-based EasyPC pcb CAD tool to Electronics World readers at a discount. See page 674.

Interested in designing antennas? Electronics World is making available the new Newnes book and cd combination 'Antenna Toolkit' on page 656.

Buy a Kenwood oscilloscope with an exclusive Electronics World reader discount. Details on page 680.



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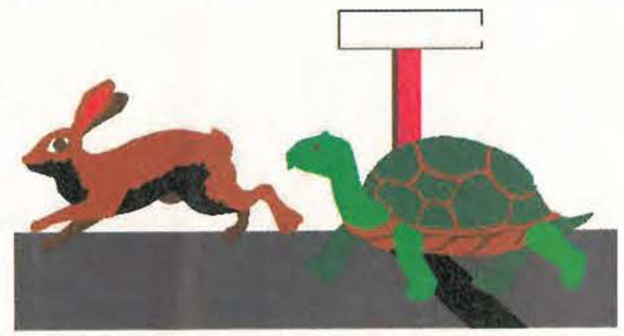
The tortoise and the hare



If you said that the capacity of mobile telecommunications networks could overtake fixed wire phones in the next five years or so, you'd risk being thought crazy. After all, terabit per second data rates for cable have been demonstrated in laboratories while the guaranteed GSM capacity is only 9.6kbit/s.

But although the potential of fixed link communications is vastly greater than wireless, commercial considerations seem to be driving the mobile people to higher capacities faster than the fixed link people.

The technology bane of the age has been the leaden pace of advance of the fixed wire telecommunications service providers. Most of us still have the 28.8kbit/s rate offered by the standard twisted pair wires running into our houses, despite the fact that technology to boost that capacity by more than ten times has been around for some fifteen years.

Of the two most suitable ways of increasing carrying capacity – ISDN and ADSL – 384kbits/s ISDN has been deployed grudgingly and expensively, costing an extra £80 or so on your quarterly bill, while 2Mbits/s ADSL remains some way off.

"We've completed year-long ADSL trials in Ipswich and Colchester. Consumer trials start in September and we're currently looking for 30 content providers to join in those trials," says a BT spokesman.

Yet the world's mobile operators have inked in 2000 as the date for having third generation mobile technologies called UMTS (universal mobile telephone systems) running. And they'll run at 384kbit/s – the same as fixed wire ISDN. Moreover, the mobile people are talking about an accelerated move to 2Mbits/s, which takes capacity into the territory of ISDN's successor technology ADSL.

A wild card in the equation is the world's first 'global wireless LAN' – the broadband, 288 satellite constellation Teledesic – backed by Bill Gates, Craig McCaw, Motorola and Prince Talal of Saudi Arabia, which is expected to begin its service in 2003. Capacity and cost of use is not yet known, but it could provide global access to a network for voice communications, datacommunications, video communications and Internet access which would make every other network redundant – if the others don't provide at least equivalent carrying capacity.

The thing is that the mobile people seem to be moulded from more entrepreneurial clay than the fixed link people with their 100 year legacy of being government-controlled monopolists.

Furthermore, as the government wises up to the benefits of promoting competition by auctioning off licences to operate mobile telephone networks, they'll probably be getting more competitive.

In May, Barbara Roche, minister of state at the Department of Trade and Industry, announced that UMTS licences would be sold off in an auction in 1999.

Roche was following the example of the Americans who raised, or thought they had raised, an amazing $16bn in auctions of mobile phone licences in 1995 and 1996.

'Thought they had raised' has to be said because a number of the buyers of American licencees subsequently withdrew, realising they had overbid.

Roche has more modest expectations, expecting only £1.5bn for the UK licences, which seems about right in view of the 5:1 population difference between the UK and US, less generous financial arrangements for bidders, and more stringent qualification provisions. In the US auctions only very modest amounts of money had to be paid up-front, and almost anyone, regardless of antecedents, could bid.

A second wild card in the equation could be the satellite systems which are to provide digital television broadcasting. Regulators permitting, these satellites can also be used to provide telecommunications services.

It looks as if the regulators are going to be permissive because the EC has agreed to allow Rupert Murdoch's BSkyB and BT to set up a joint venture called British Interactive Broadcasting to provide interactive tv and telecommunications services using the Murdoch satellite constellation.

All these people spending money on expensive mobile network licences, and on even more expensive satellite constellations, will be anxious to see returns on their investments. That's why it's possible that the aggressively profit-conscious mobile operators could out-bandwidth the fixed wire operators still hampered by their monopolist mental legacy ■

David Manners

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Mobile video phones: Japan leads Europe

Japan looks set to steal a march on Europe in the development of mobile video phones.

Since Japan's third generation mobile services (IMT-2000) – based on wideband code division access (W-CDMA) – will be compatible with Europe's UMTS services, Japanese developed video handsets will also be suitable for use in Europe.

European third generation UMTS services are due to start in 2001, a year later than Japan's, so European suppliers accept that Japanese manufacturers will be in a strong position in the market for next generation handsets.

"Whereas the US led with first generation wireless phones (AMPS) and Europe with second generation GSM, Japan is looking to lead with the third generation IMT-2000," said an industry observer. "However, Europe is fully aware of the threat."

Matsushita Electric Industrial is developing an MPEG-4 core for a mobile video handset available from 2000, once third generation mobile phone services begin in Japan. Matsushita and NEC have also been selected for an IMT-2000 handset trial being undertaken by Japanese phone operator NTT Docomo.

Texas Instruments – which claims to have its dsps in over half of all GSM handsets – is acutely aware of the importance of video and the MPEG-4 audio visual standard for mobile phones.

"Video is the next medium for cellular," said Eric Dewannain, TI's semiconductor's group European multimedia programme manager.

He admitted that the advent of IMT-2000 places Japanese firms on an equal footing with European.

This is also the view of UK consultancy The Technology Partnership (TTP). "The power base is definitely shifting East," said TTP's Dr Tony Milbourn, who added, "Don't underestimate the position of European firms."

TI's Dewannain confirmed that the company was undertaking MPEG-4 simulation work but would not be drawn on when its expects to have MPEG-4 silicon. Will it have silicon for the Japanese market by 2000? "I cannot say," he said.

Other companies in Europe undertaking r&d work on video coding algorithms for handsets include Siemens and Bosch. However neither has revealed time scales for any video coding hardware.

Roy Rubenstein, *Electronics Weekly*

Fingerprint ICs suit phones and laptops

STMicroelectronics is preparing to put its fingerprint recognition IC into production for products such as mobile phones and laptop pcs. A prototype was first shown in May last year with 390dpi resolution. This latest version ups the resolution to 508dpi.

"Our product is based on a sensor which detects capacitance between the finger and a plate. This can recognise the difference between ridges and valleys of fingerprints," said product manager Herve Martin.

All the associated electronics, including a-to-d converters, is integrated, so the sensor can easily be interfaced to a controller using an I²C bus.

Resolution and sensitivity of the sensor are high enough to detect the difference between – hold onto your breakfast – a live or dead finger.

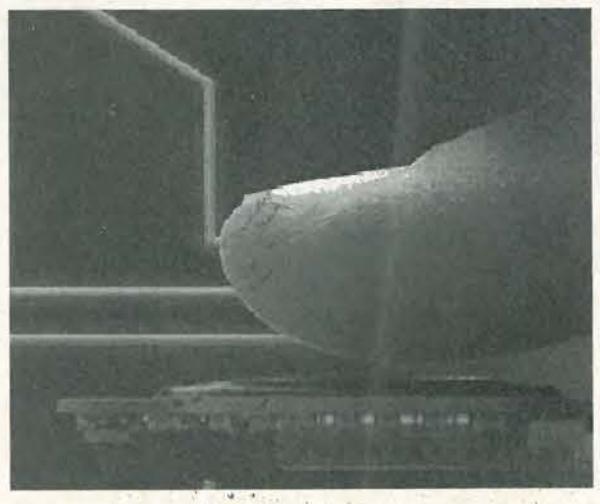
Martin expects the sensor to be integrated into phones and laptops next year. It is small enough for such applications because the entire sensor is constructed on silicon.

Low-cost radio links for inter-pc comms

A specification for low cost radio links between electronic equipment has been announced by a group of companies headed by Ericsson.

Developed with the help of IBM, Intel, Nokia and Toshiba, the technology code named Blue Tooth will provide wireless links between pcs, mobile phones, digital cameras and printers.

Data rates will be 432kbit/s full duplex between up to eight devices per network. Two simultaneous voice channels will be possible. The technology uses 2.4GHz microwave links and is estimated to cost $5 in semiconductor costs to implement in each product.



Far left, STMicroelectronics' fingerprint sensor has gone into production.

Left, resolution and sensitivity of the sensor are high enough to detect the difference between a living finger and one that has been chopped off!

ITC warns digital tv set-top makers

The government's broadcasting watchdog has issued a warning to set-top box receiver manufacturers and broadcasters as it draws up the technical guidelines for the introduction of digital television services later this year.

The Independent Television Commission (ITC) wants to ensure that viewers know what they are paying for when they buy the digital set-top boxes needed to receive digital tv services. "What the viewer plugs in must be able to do what he expects it to do," said Peter Rogers, ITC chief executive. "We don't want the consumer to be confused."

Action against a digital tv broadcaster that does not fulfil its licence conditions can be taken by the ITC, but the watchdog cannot stop set-top boxes being sold that do not conform to the document. "We are not all powerful and don't aspire to be," said Rogers.

The ITC is hoping to clarify standards for the interoperability and open access of digital television services from competing satellite and terrestrial broadcasters with the publication of a consultation document. It proposes a framework of digital transmission standards as well as a requirement for service providers to support reception of their services on open standard integrated digital televisions.

According to the ITC, satellite broadcaster British Sky Broadcasting (BSkyB) has concerns over open access creating difficulties in making receiver chips piracy proof. But, the ITC does not accept that open access makes piracy any more likely.

Last month BSkyB issued a writ against digital terrestrial TV broadcaster British Digital Broadcasting (BDB) following BDB's decision to use the SECA conditional access system which it believed was incompatible with its own and which was not part of an agreement struck when BSkyB agreed to quit the BDB consortium before it won the licence.

There has now been positive dialogue between the two on the issue of interoperability, according to the ITC.

Standards for terrestrial, satellite, cable and microwave digital televisions are all covered in the document which the ITC is inviting the industry to comment on by 10 July.

Melanie Reynolds, *Electronics Weekly*

ADSL for Web access is imminent

High-speed Internet access, based on asymmetrical digital subscriber line technology, or adsl, will start to roll out this year, claims SGS-Thomson Microelectronics (STM).

Telecoms firms in several countries – including the US and Denmark – have committed to using the technology which gives Internet access at up to 6Mbit/s.

"The volume deployment of adsl starts this year," said Pierandrea Borgato, product manager for dsl technology at STM. The company expects up to 400000 lines to be connected this year, increasing to three million by the year 2000.

Although originally developed for the tv industry, particularly video-on-demand, adsl has more recently been championed by Internet users.

"The need for more and faster Internet access is driving the development of adsl," said Borgato. "There will be 100 million people connected to the Internet in the year 2000."

Because of the switch from video-on-demand to Internet, a lower speed version called *ADSL Lite* has been specified by Intel, Microsoft and Compaq. It has a 1.5Mbit/s downstream speed and 384kbit/s upstream.

"The *Lite* version has come into favour because of its lower speed and hence simpler installation," Borgato added. The system uses all existing wiring and phone sockets. The lower data rate also enables longer runs of standard copper wiring up to several miles.

Richard Ball, *Electronics Weekly*

NHS year 2000 problems could cause deaths

Non-Year 2000 compliant microcontrollers embedded in NHS equipment threaten widespread disruption in hospitals and surgeries with potentially fatal consequences for patients, the National Audit Office (NAO) has warned.

Some 15 per cent of Trusts admitted to the NAO that they could not be confident of ensuring that their clinical equipment would continue to function normally in the year 2000 despite predicted spending on the year 2000 for the NHS as a whole of £230m.

Embedded micros are the key threat, says the report.

David Davis, chairman of the House of Commons Public Accounts committee, to which the NAO reports, underlined the warning: "Much of the equipment used in diagnosis and treatment, for example, intravenous infusion pumps used commonly in the NHS, contain embedded microprocessors. Failure of such vital pieces of equipment could have even more serious consequences for individuals than failure of major computer systems."

Many of the more sophisticated laboratory, X-ray and other diagnostic and treatment services rely on electronic equipment with embedded computer chips. "Failure of these systems could have serious consequences for patients," said the NAO.

The NAO's report concludes that "some parts of the NHS remain at risk of failing to achieve year 2000 compliance".

Electronics sector fares well

The relative strength of the electronics manufacturing sector has been emphasised in a new set of government statistics.

Further evidence that manufacturing in the electronics sector is fairing better than the rest of the UK's manufacturing industry is provided by the Office for National Statistics.

Its Index of Production report claims that while the overall engineering manufacturing output fell by 0.1 per cent in the first quarter of 1998, the output from the electrical and optical equipment industries (underpinned by electronics) increased by 2.3 per cent.

This agrees with the findings that electronic manufacturers are bucking the trend that has seen many small and medium sized enterprises suffer a fall in orders in the last four months. The gloomy findings based on a Confederation of British Industry survey does not appear to reflect the current experiences of electronic firms.

The relative strength of the electronics sector is also confirmed by the Engineering Employer's Federation. "While engineering *per se* is taking a hammering, the higher value segments of electronics and aerospace are buoyant," said an EEF spokesman.

The EEF is optimistic about the segments' longer term prospects, expecting electronics and aerospace to grow at between 2.5 and 3 per cent over the next two years. Engineering in general is expected to grow by only 0.5 per cent, a marked drop on last year's 3.5 per cent growth.

Roy Rubenstein

UK digital tv held back by politics

Chip makers are being frustrated by political delays in launching digital terrestrial tv in the UK.

Some were complaining at this week's Cable & Satellite show in London that they do not know when products would be needed despite having silicon about to go into production.

"It is frustrating to find things going on so long," said Nigel Pritchard, technical marketing and business development manager for SGS-Thomson Microelectronics (now known as STMicroelectronics).

"There are a lot of things that are taking a long time to get started. These are political rather than technical. People are looking at the Christmas period but whether we will be up and running by then remains to be seen. If not it won't be silicon preventing it," he added.

But doubts about technology were expressed by Anthony Simon, product market manager of VLSI Technology subsidiary Comatlas. "It is an extremely difficult technology," he said. "The BBC is still finding echoes that are longer than expected. It is not going to be an easy market."

Another supplier, LSI Logic, was in London to show off its single chip receiver product developed with the BBC. The chip does not include error correction circuitry which is still on a separate IC. LSI Logic plans to combine the two but because of uncertainty in the digital tv market it will not give a date.

Jean-Luc Droitcourt, LSI marketing director for digital tv said: "We want to make them into one chip. It will depend on the market. It is not difficult technology; if the market takes off we will do it quickly."

Barclays trials 'Screenphone' home banking

A UK trial involving a Screenphone that offers banking and a range of home delivery services is been launched by Barclays Bank.

The six month trial, set to start in the summer, will involve 2000 of the bank's customers in ten areas in the UK.

"We hope to glean from the pilot how much value a customer would put on a service like this," said a spokeswoman. If everything goes to plan, the service will be rolled out next year.

In addition to 24-hour access to the bank account, customers will be able to order foreign currency, CDs, videos, tickets, wine or book holidays.

The Screenphone plugs into the telephone line and communicates with the server using the analogue display services interface (ADSI) protocol which allows the phone to receive and display digital text and services.

Security for the system will include a membership number and a personal ID.

The screenphone, developed in conjunction with Matra Nortel and New North Media, is priced at £99, and will have a £5 monthly service charge.

Phone banking... The Barclays Bank Screenphone gives customers access to banking details and other services without requiring a home computer. The ADSI protocol used specifies how voice and small bursts of data can simultaneously share the one analogue telephone line. The data transfer rate is 1.2kbit/s.

Fast, clean and powerful

Giovanni Stochino has enhanced his ultra fast, low-distortion power amplifier for audio use. Delivering 100W into 8Ω, this design slews at over 300V/µs and features 0.0026% distortion at rated power. In addition, Giovanni has refined the design to make sure that this performance level can be replicated.

Since the publication of my article on the 100W into 8Ω low distortion audio amplifier, I have received a number of letters from *EW* readers interested in implementing a low thd fast amplifier.

I must stress that special care is essential when implementing this amplifier design, since all stages are capable of providing extremely high currents. Wrong connections or occasional shorts during testing can have catastrophic consequences.

Here I present a functionally optimised design, and include instructions for the implementation of a suitable powering scheme. I have also designed and fully tested a pcb, details of which appear later.

Circuit enhancements

Figure 1 shows the detailed circuit diagram of the amplifier which has been implemented. Compared with the corresponding diagram presented in my previous article, i.e. Fig. 3a, some minor changes have been introduced in order to add more flexibility to the design.

In particular, I have introduced dc decoupling into the feedback network via capacitor C_{22} and C_{23}. This is to keep low the output offset voltage even when using a relatively high value of resistor R_{12}, which both provides a return path to ground for the base currents of input transistors Tr_1 and Tr_3, and sets the level of the overall amplifier input impedance.

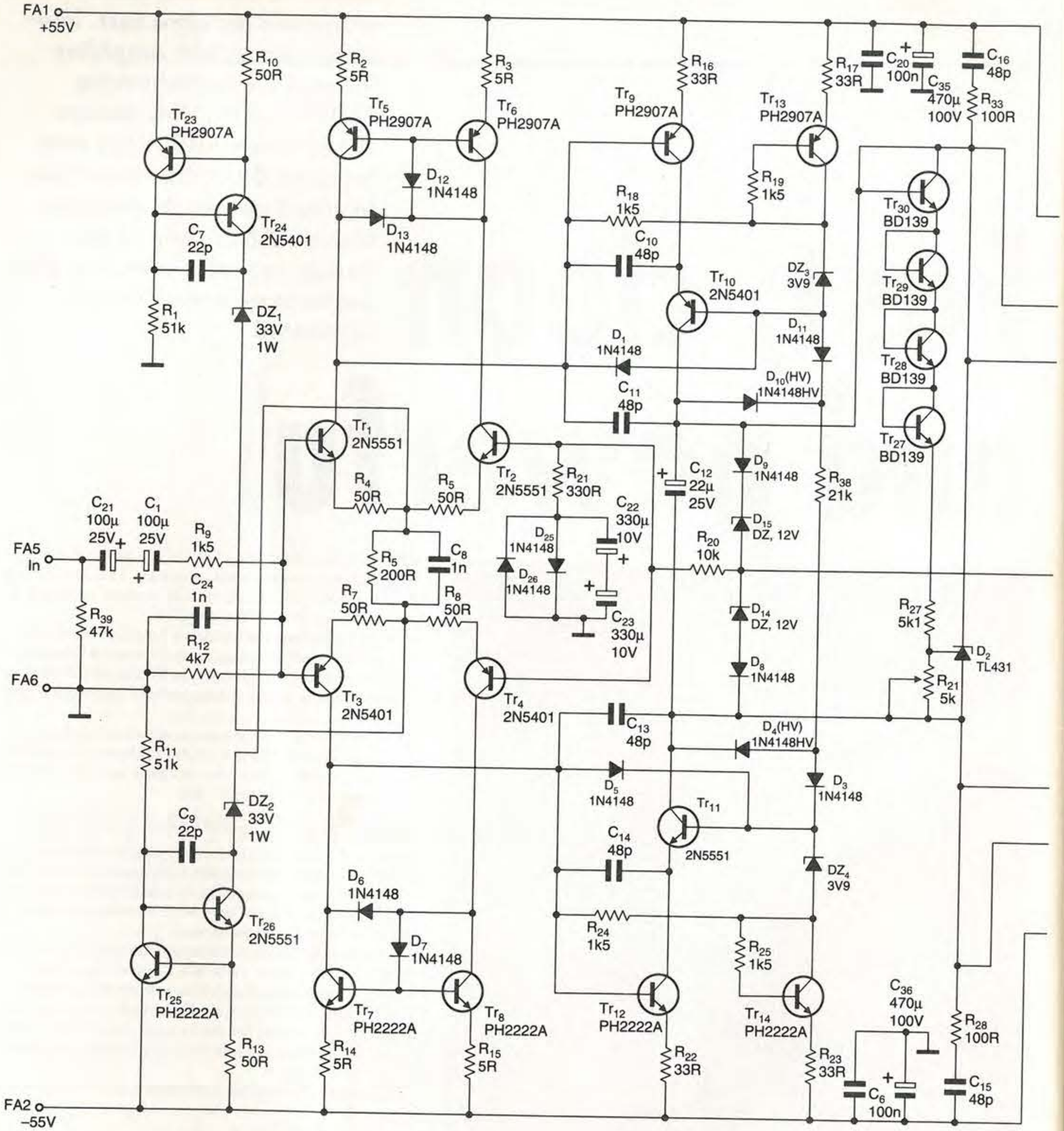
The output offset voltage contribution due to R_{12} is given by,

$$V_{os} = \frac{I_A(\beta_p - \beta_n)}{\beta_p \beta_n} R_{12} G_o \qquad (1)$$

where I_A is the bias current of the input stage transistors, $Tr_{1\text{-}4}$, β_n and β_p are the current gain of n-p-n and p-n-p bipolar input transistors, respectively. Finally, G_o is the closed-loop dc gain of the amplifier.

Typical gain figures when $I_A \approx 2$mA are $\beta_n \approx 150$ for the n-p-n 2N5551 transistor and $\beta_p \approx 70$ for the 2N5401 p-n-p device. While $G_o = 32$, with R_{21} connected to ground, equation (1) yields 2.3V for $R_{12} = 4.7$kΩ.

This offset is unacceptably high. The insertion of dc decoupling reduces G_o to almost unity, so that the worst



case V_{os} is limited to few hundred millivolt. This represents an acceptable level of output offset.

Filtering added. Another change made to increase flexibility is to allow the possibility of incorporating an input passband filter, via components C_1 and C_{21}, together with R_{12} for the high-pass section and R_9+C_{24} for the low-pass section.

In the following analysis, C_1 and C_{21} are considered equal to $2C_H$. With component value shown, the –3 dB bandwidth is 1Hz to 120kHz. Assuming that the signal source resistance, which is usually lower than 300Ω, has no influence, high-pass and low-pass frequency corners are given by

$$f_H = \frac{1}{2\pi R_H C_H}$$

and

$$f_L = \frac{1}{2\pi R_L C_{24}}$$

respectively, where R_H is the sum R_{12}+R_9, and R_L is the parallel $R_{12}//R_9$. They are easily adapted, and the low-pass section can be bypassed by omitting C_{24} and shorting R_9.

Improved temperature sensing. The temperature-sensing network *TS* incorporates an additional transistor. This adds

Fig. 1. Detailed circuit diagram of the chosen practical implementation of the 100W/8Ω audio-power amplifier, featuring a speed higher than 300V/µs and rated power thd figures of 0.002% and 0.018% at 1kHz and 20 kHz, respectively. All diodes are 1N4448 Diodes D_4 and D_{10} marked 1N4448HV are still 1N4448, but selected for a reverse voltage higher than 120V. This selection is made by applying a reverse voltage of 130V via a resistor of 10kΩ and measuring the current, which has to be less than 10mA. The yield is normally higher than 50%.

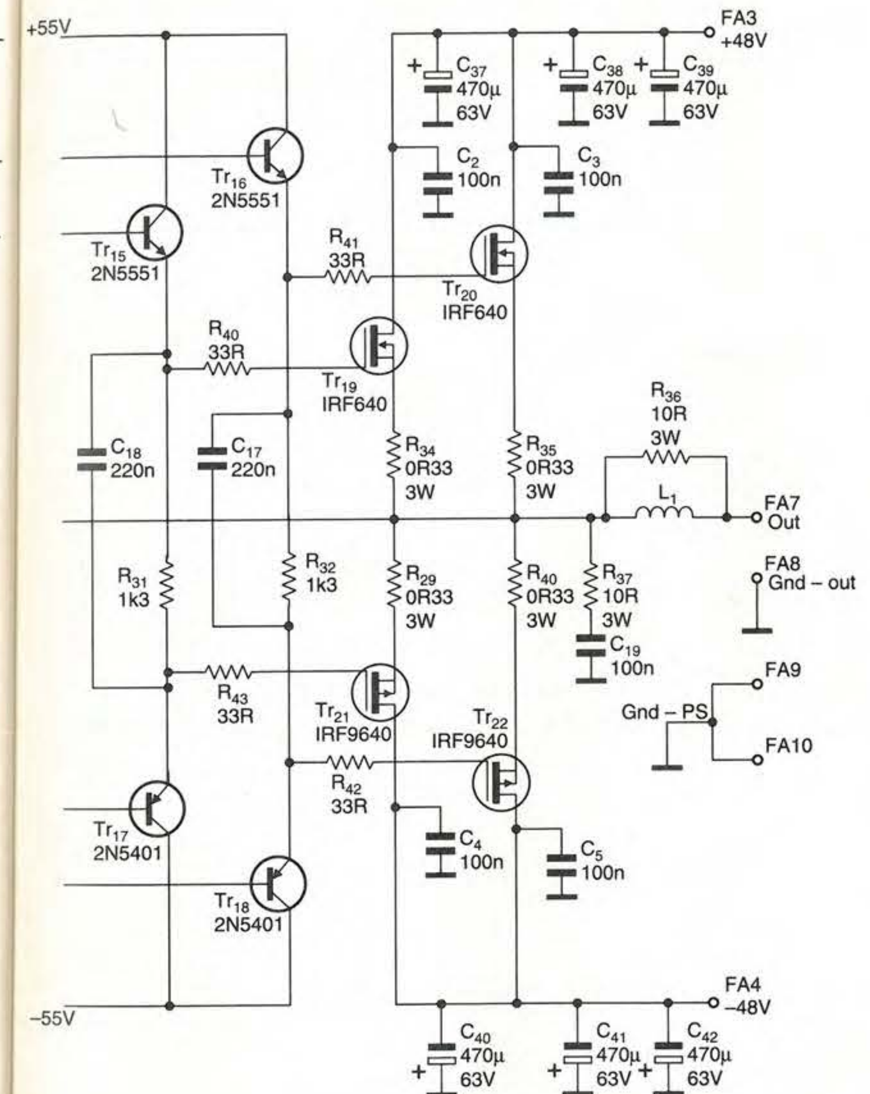


Table 2. Slewing performance of the audio power amplifier for a source resistance of 50Ω and an 8Ω load. Pulse input was 6V peak, as in Fig. 4 of my previous article.[1]

Characteristic results	Measurement
Positive slew-rate	+320V/µs
Negative slew-rate	–300V/µs

Table 3 . Total harmonic distortion figures of the final 100W/8Ω audio power amplifier for a source resistance of 50Ω and an 8Ω load. Quiescent current was 150mA and bandwidth 80kHz.

V_{out}, pk-pk	1kHz	20kHz
5	0.0030%	0.0043%
10	0.0028%	0.0047%
20	0.0023%	0.0061%
40	0.0028%	0.0110%
80	0.0026%	0.0170%

Note: Total harmonic distortion remains virtually constant when source impedance R_s varies in the range 50Ω to 5kΩ. The instrumentation limit, thd+noise, was 0.002% at 1kHz; 0.003% at 20kHz.

extra flexibility to the mounting mode of the temperature-sensing network relative to the power output devices Tr_{19-22}.

In my original prototype, the three sensing transistors were mounted very close to output power mosfets. A total $\Delta V_{TS}/\Delta T$ of –6mV/°C was adequate.

However, when a more practical scheme for mounting the temperature-sensing network on the heat sink is needed, like the one presented here, you have to allow a looser thermal coupling with power devices. Because of this, $\Delta V_{TS}/\Delta T$ will be higher and it may turn out that a greater number of temperature sensing transistors will be needed.

In the layout scheme proposed, four transistors providing a $\Delta V_{TS}/\Delta T$ of –8mV/°C were x found adequate to provide a fairly stable – within 20% – output power mosfets bias setting under a wide range of operating conditions.

The quiescent current of output devices has been set to 150mA, which further contributes to the thermal stability of the operating point of the output mosfets. The

Table 1. Main characteristics of the fast audio power amplifier for 150mA quiescent current and 80kHz bandwidth.

Characteristic	Measurement results
Measured output offset voltage	+32mV
DC open-loop gain	110dB
Low-frequency closed loop gain	32dB
Small-signal bandwidth before the output filter (–3dB)	20Hz (–0.1dB), 1.3MHz
Unity gain frequency before the output filter	22MHz
Open-loop gain at 20kHz	66dB
Closed-loop amplifier phase margin before the output filter	+76°
Output noise (BW=80kHz, input terminated with 50Ω)	42µV rms
Slew rate	See Table 2
Total harmonic distortion (thd)	See Table 3

scheme is flexible in the sense that a different $\Delta V_{TS}/\Delta T$ is easily achieved by bypassing one or more thermal sensing transistors. Remember to make sure to set trimmer R_{26}, i.e. VR_1 in Fig. 3a of my previous article,[1] to its highest value before applying power to the amplifier.

Better stability. Gate resistors $R_{40\text{-}43}$, needed to prevent high frequency oscillation of the output mosfets, are shown in Fig. 1. They were also used in my first prototype but were not reported, inadvertently, on the earlier circuit of Fig. 3a.[1] This oscillation is very likely to occur, mainly due to parasitics in the implementation, but it is not usually evident during Spice simulation.

More decoupling. Power supply decoupling capacitors, for both unregulated 48 V and regulated 55V rails, have been included in Fig. 1. Regulated supply rails can be varied up to 58V in order to increase output power to 120W/8Ω. Of course adequate heat-sink has to be assured.

Is board layout critical?

The amplifier layout was designed for compactness, ease of assembly and alignment, and, finally, to ensure the same level of performance as the prototype.

It has not been an easy task. As a matter of fact my first pcb layout had to be slightly modified, since measured total harmonic distortion was 6dB worse than the original breadboarded prototype. The reason for this poor thd performance was found in the return path for the load current, which was not well controlled.

The final design, however, has proved effective and the amplifier performances are more or less the same as those reported in my previous article.

The value of inductance L_1 should be in the region of 3-5mH. I suggested wire diameter of 1.5-1.8mm. On my pcb, the board area for this inductor, at 25 by 45mm, is enough for all practical implementation options.

Determining the value of L_1 is carried out as follows:

$$L_1(\mu H) \approx \frac{N^2 d}{1010\left(0.45 + \frac{l}{d}\right)} \qquad (2)$$

where l and d are the length and the diameter, both in mm, of the coil former – assumed to be cylindrical – respectively, and N is the number of turns.

I suggest:

l=45mm
d=16mm
ϕ(diameter of the wire)=1.5mm
N=30

In this case, equation (2) yields L_1=4μH.

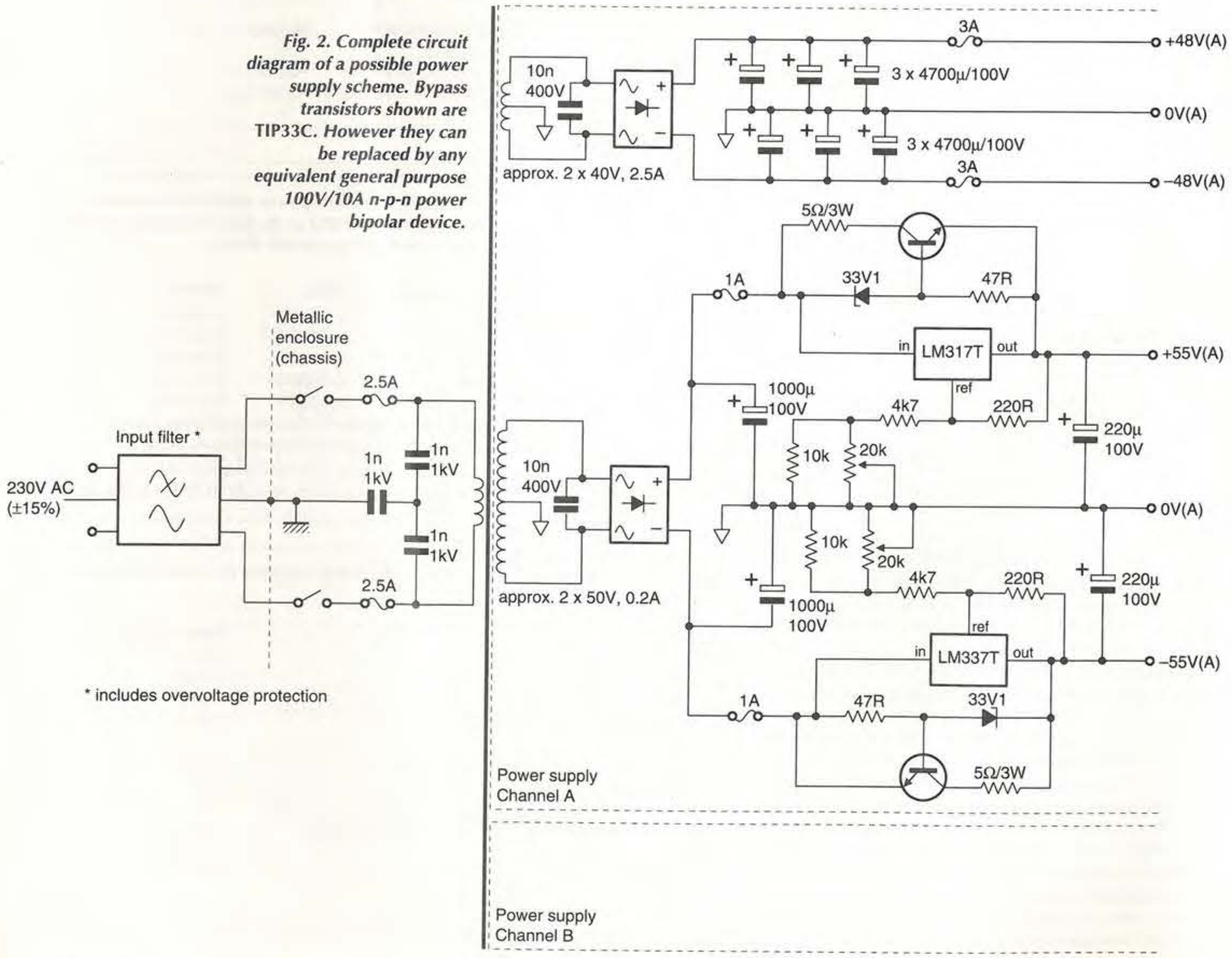


Fig. 2. Complete circuit diagram of a possible power supply scheme. Bypass transistors shown are TIP33C. However they can be replaced by any equivalent general purpose 100V/10A n-p-n power bipolar device.

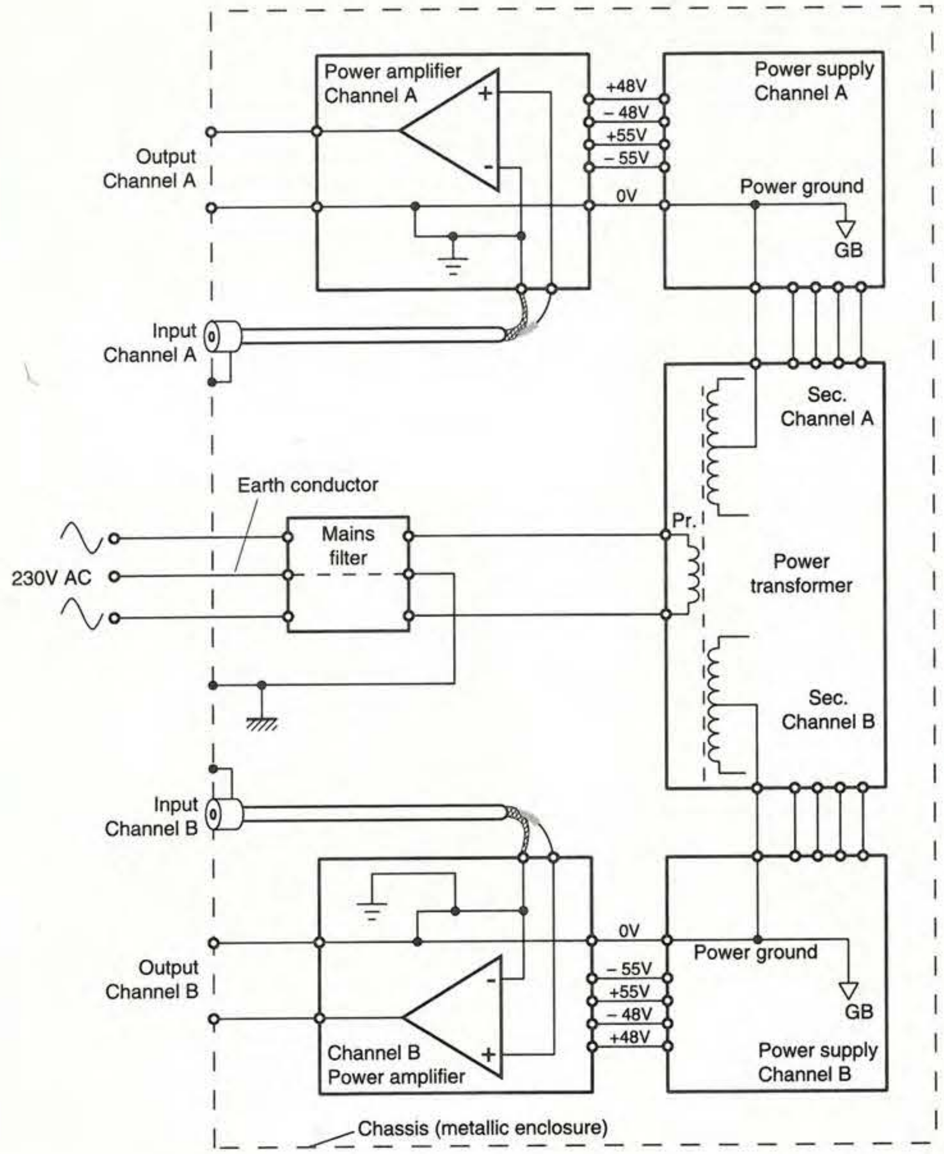


Fig. 3. A practical grounding scheme.

Fig. 4. Photograph of the amplifier printed board assembly prototype.

Power supply

Figure 2 shows a suggested power supply scheme, which is simple, effective and low cost.

Separate power supply sections are recommended in order to avoid ground loops and ensure the optimum signal to noise ratio. One section – channel A – only is shown in detail in Fig. 2.

Regulators *LM317T* and *LM337T* are bypassed by a protection-clamping circuit made up from a 33V zener diode of a few watts, a power resistor and *TIP33C* power transistors. This prevents the maximum input-output voltage difference from being exceeded, which is 40V for both regulators.

Note that, in order to avoid ground loops, the ground references of channel A and channel B have to be joined at a single point, normally at the inputs of the two A and B amplifiers. Connection to the metallic enclosure, i.e. chassis ground, is also usually made here.

Safety is assured by connecting, as usual, the chassis to the safety ground ⏚. The chassis also acts as a metallic shield.

Figure 3 shows a suggested grounding scheme, where the power ground of the power supply ⏚ is connected to the signal ground ⏚ of the corresponding power amplifier.

The outer conductor of the input signal connector of both channels is connected – the usual mechanical connection provides good electrical contact too – to the chassis ground of the mechanical enclosure.

Finally, **Fig. 4** is a photograph of the prototype of the power amplifier used for all measurements.

Verified amplifier performance

Measurements have shown that the performance of the prototype assembled on the final version of the pcb are as good as the performances of the first experimental prototype of the low thd, very fast audio power amplifier.

This fact, in conjunction with the observation that even combining n and p-channel output power mosfet coming from different vendors did not affect distortion performance, is additional proof that the chosen architecture for very fast, low distortion audio power amplification is robust and relatively insensitive to component tolerances and mismatches.

Finally, it is worth mentioning that the amplifier is stable for any value of the input signal source impedance Z_s, consisting of a resistor in parallel with a capacitor, $R_s//C_s$.

Reference

1. Stochino, G, '300V/μs Power', *Electronics World*, April 1997, pp. 278-282.

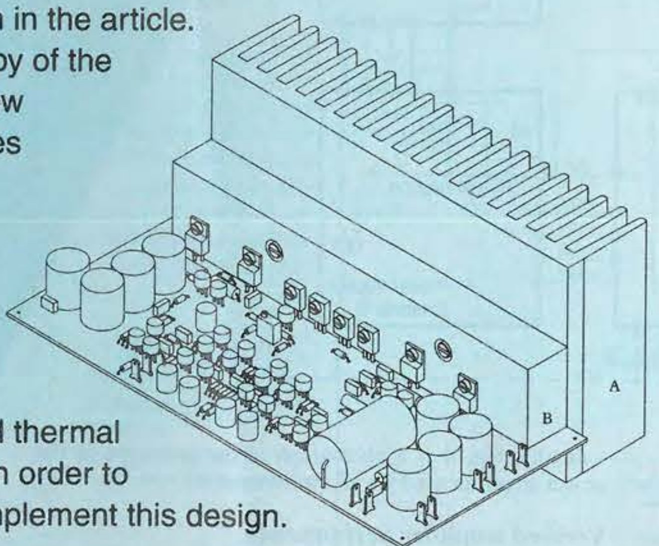
Power amplifier circuit boards

£42 per pair fully inclusive or £25 each

Professionally designed and manufactured printed circuit boards for Giovanni Stochino's no compromise 100W power amp are available to buy.

These high-quality fibre-glass reinforced circuit boards are designed for Giovanni Stochino's fast, low-distortion 100W power amplifier described in the August 1998 issue. Layout of the double-sided, silk screened and solder masked boards has been verified and approved by Giovanni.

This offer is for the pcbs only. The layout does not accommodate the power amplifier scheme shown in the article. Note that a copy of the article and a few designers' notes are included with each purchase, but you will need some knowledge of electronics and thermal management in order to successfully implement this design.



Giovanni's high-performance power amplifier mounted on its heat sink.

Please send me___ pcbs @ £25 each or £42 a pair.
I enclose my cheque for £ _____
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Address______________
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Cheques made payable to Reed Business Information.
Post to: PCB Offer, Electronics World, Quadrant House, The Quadrant, Sutton, Surrey, SM2 5AS. Please alow 28 days for delivery.

Specifications

Power into 8Ω load	100W
Small-signal bandwidth before the output filter	20Hz (–0.1dB), 1.3MHz (–3dB)
Unity gain frequency before the output filter	22MHz
Output noise (BW=80kHz, input terminated with 50Ω	42μV rms
Measured output offset voltage	+32mV

Distortion performance

V_{out}, pk-pk	1kHz	20kHz
5	0.0030%	0.0043%
10	0.0028%	0.0047%
20	0.0023%	0.0061%
40	0.0028%	0.0110%
80	0.0026%	0.0170%

Slew rate

Positive slew-rate	+320V/μs
Negative slew-rate	–300V/μs

Cyril Bateman looks at measuring capacitors at rf via the reflection bridge and discusses fault finding, handling and dielectric absorption in this final article.

Understanding capacitors

Conventional capacitor bridge measurement techniques were described in my last article. These techniques are useful to 10MHz, although there are specialised *LCR* meters capable of measuring at higher frequencies. There's more on this in the panel entitled 'Capacitor bridge.'

Measurements at higher frequencies can be made using the reflection bridge technique with a vector network analyser to measure the 'S' parameters of a capacitor. Developed in the sixties, this technique was intended for characterising high-frequency semiconductors. With suitable jigs, reflection bridge techniques can be used at up to at least 40GHz using an *HP8510* or 6GHz using the *HP8753*.

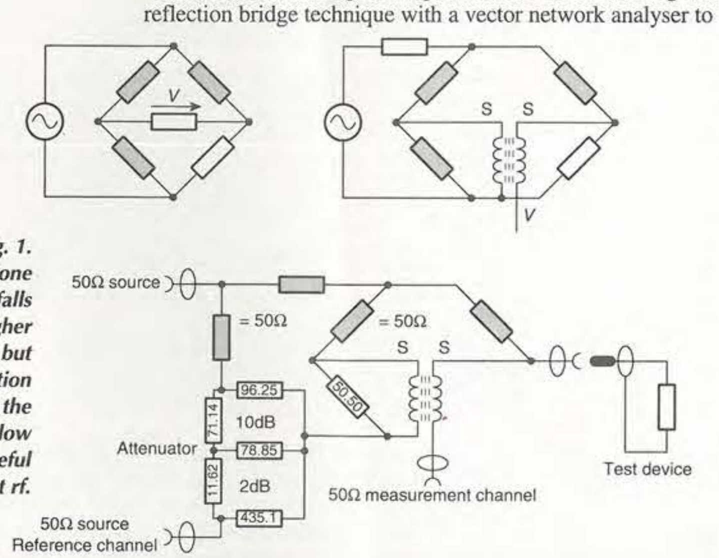
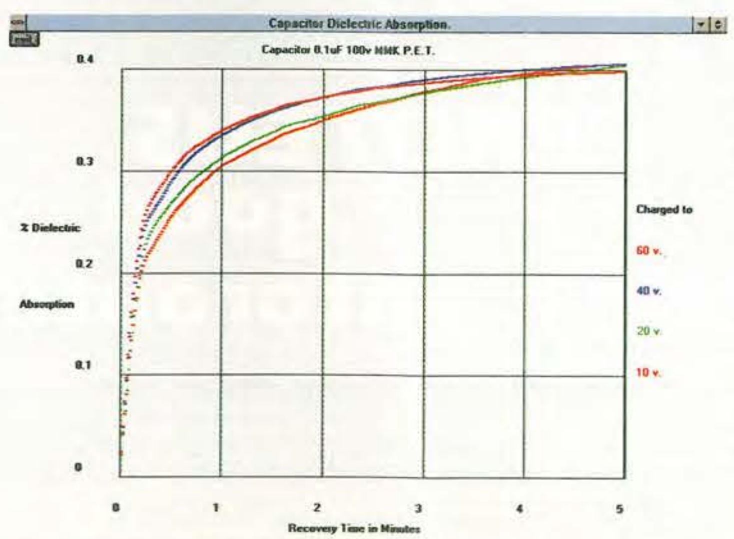


Fig. 1. Wheatstone bridge, left, falls down at higher frequencies but the reflection bridge on the right and below produces useful readings at rf.



Reflection-bridge measurement

For many years, the reflection bridge[1] was the only practical method for making precision measurements at frequencies above 30MHz.

Based on 50Ω standards, such reflection bridge measurements provided excellent accuracy for medium impedances. But accuracy suffered when measuring very high or low impedances. Since many design and measurement laboratories already had access to an *HP8753* though, this method was popular.

I have assumed use of either the *HP8510* or *HP8753* analysers, since I am familiar with them and both include 12-term accuracy enhancement as standard. Other similar instruments – provided they include 12-term accuracy enhancement, sometimes known as 'full 2-port correction' – should also be suitable.

Why this emphasis on 12-term accuracy enhancement ? The accuracy of vector network analyser measurement systems is specified assuming 'well matched' test devices. When used to measure a severely mismatched load, such as a capacitor, the source generator has to drive into effectively a short circuit, but having a mismatched phase. The 12-term accuracy enhancement method corrects for this. Analysers having less than 12-term accuracy enhancement result in increased measurement error.[2]

As frequency increases, it becomes more difficult to measure the test currents and voltages applied to the component being measured, at the exact point where the component has been inserted. Even small changes in electrical length when connecting components, cause considerable measurement phase changes – hence major errors – at high frequencies.

Reflection bridge in practice

A reflection or directional bridge, comprising three 50Ω precision resistors with a wideband 1:1 balun, has the ability to discriminate between signals passing to, and reflected from, a transmission line.[1]

Fig. 2. Dielectric absorption is not a fixed number, it varies according to measurement method. With any given capacitor, dielectric absorption also varies according to the 'volts per micron' stress applied.

A loss-free transmission line having a matched load absorbs all incident power and reflects nothing. Terminated with anything other than this matched load, a reflected signal is returned to the signal source. This reflected signal, which is separated from the incident signal in the reflection bridge, can then be measured, **Fig. 1**.

When terminated by an open circuit, the reflected signal is identical in amplitude and phase with the incident signal. Terminated in a short circuit, this reflected signal is identical in amplitude but 180° out of phase with the incident signal.

Measurements of these three 'standards,' i.e. of a known value, of a short and of an open circuit, at each frequency of interest can be used to mathematically define a 'calibration plane.' Subsequent measurements of a test component are then corrected to this exact measurement insertion point in the transmission line, ensuring accuracy.

When the line is terminated in a pure capacitive or inductive load, the phase of the reflected wave depends on the load, but the amplitude of the reflected wave will equal that of the incident wave.

When the line is terminated in a lossy capacitive or inductive load, the phase of the reflected wave depends on the phase of the load. The amplitude of the reflected wave will be dependent on the resistive losses being measured.

These measured reflection values, $\pm\Gamma x$ $\pm\Gamma y$ of a test component, can easily be converted into the conventional $R \pm jX$ format, by substitution into two standard equations,

$$R = Z_o \times \frac{1-(\Gamma x^2 + \Gamma y^2)}{1 - 2\Gamma x + \Gamma x^2 + \Gamma y^2}$$

$$jX = Z_o \times \frac{2\Gamma y}{1 - 2\Gamma x + \Gamma x^2 + \Gamma y^2}$$

Once in the $R \pm jX$ format, any other desired parameters can simply be derived.[1] There's more on this in box 'Conversions and equations' in last month's article.

In 1994, Hewlett Packard marketed the first high frequency voltage/current based impedance meter, the *HP4291A*. It offered a basic measurement accuracy of 0.8% and a wider impedance range than was possible for reflection measurements using the *HP8753*. But it had a similar price tag.

Measuring from 1MHz to 1.8GHz and having dedicated capacitor test jigs, this instrument avoided the need to design, make and calibrate, high-quality, low-loss, test jigs.

The *HP4286* meter introduced a year later was the first dedicated radio frequency *LCR* meter capable of measuring from 1MHz to 1GHz. It offered a broadly similar capacitor measurement ability but at lower cost. The panel 'Capacitor test instruments' in last month's article details this topic.

More accessible measurement methods

Experimenters' methods trade off cost for accuracy and measurement speed, but commercial *LCR* meters are able to maintain measurement accuracy even at volume production rates. Perhaps you need an intermediate approach, i.e. better accuracy than is possible with experimenters' methods cheaper than buying state-of-the-art equipment?

Good quality second-hand low frequency *LCR* meters are extremely rare, but higher frequency rf impedance measurement instruments are often available from used equipment suppliers. A typical example is the discontinued *HP4191A*, which measures from 1MHz to 1GHz. Using accuracy enhancement techniques, it is still able to provide a useful measurement capability at low cost.

The companion lower frequency *HP4193A* was equipped with an internal generator and test probe. Components could be measured *in situ* on a circuit board, from 400kHz to 110MHz.

Capacitor bridge

The conventional Wheatstone bridge used to measure the ac impedance of a capacitor involves a fixed known capacitance standard and two calibrated variable resistances, Fig. 1. It measures the unknown capacitor as a ratio of this standard by balancing out the detector voltage to near zero.[1]

This configuration has been used commercially, but it suffers from interaction of the two balance controls when measuring high tanδ capacitors. It needs repeated rebalancing, and achieving a true balance is slow.

The transformer ratio-arm bridge was a successful early attempt to eliminate this interacting balance problem, but it is best suited to values less than 10μF. Venerable examples of Wayne-Kerr bridges often appear at good prices. Replacement of every capacitor in the power supply and detector circuits, followed by routine recalibration, usually restores the bridge to its original accuracy.

One manual capacitor bridge which is most successful for all capacitance values can be easily built. It is a variation on the Wheatstone bridge, but with one balancing arm using a variable capacitor. If care is taken in choosing close tolerance and lowest-loss foil with polypropylene or polystyrene capacitor standards, good basic accuracy can be obtained.

My version is optimised for values of 10μF or above, but it can measure down to 100pF when needed. The arrangement shown in the schematics can be used to measure capacitors having a dc polarisation of up to 100V.

Assuming care is taken to minimise stray capacitances and series resistances in the bridge, good measurement results are possible from 20Hz to 20kHz. Higher frequency measurement is possible, but requires some care in arranging guards and in screening the bridge components, See Fig. 5 of last month's article.

For these reasons, and to minimise noise, the internal untuned detector shown in the schematic has been restricted to audio frequencies. I also have an excellent General Radio Corporation *1232A* tuneable high-Q external detector, measuring up to 100kHz, which can be used with this design. It can also be used with either of my two transformer ratio arm bridges. See Fig. 6 of last month's article.

These three bridges, combined with my reflection bridge/phase meter, an *HP4815* rf vector impedance meter and *HP8405* vector voltmeter, provide good accuracy measurements of an extremely wide range of capacitance values over a range of 20Hz to 1GHz.

Dielectric absorption

A degree of dielectric absorption is exhibited by all solid dielectric capacitors, but just what is dielectric absorption? My first demonstration of dielectric absorption resulted from a colleague saying 'catch' and throwing me a discharged high voltage ceramic capacitor, which gave me a nasty jolt. Between the time it was discharged and my catching it, it had recovered a most noticeable voltage.

This is the practical result of dielectric absorption. The cause is the dielectric's ability to store more charge than can be instantly released. This property is fundamental to the dielectric material and depends on the symmetry of its molecular structure.

A symmetrical-molecule dielectric has electrical characteristics effectively constant regardless of frequency and it exhibits minimal dielectric absorption effects. An asymmetrical molecular structure dielectric has a dipole moment, resulting usually in increased dielectric constant. Such an asymmetrical dielectric's electrical characteristics are frequency dependent and it exhibits notable dielectric absorption effects.[3]

Dielectric absorption obviously depends mainly on choice of dielectric materials, but is also related to the degree the dielectric material is stressed in volts per micron. The thinner the dielectric the greater effect for any one charging voltage, **Fig. 2**.

How is this effect measured? For consistency, the capacitor should be charged to a known voltage for a set time. It is discharged at a known rate using the same resistance value, for a controlled time or to a known voltage. Next it is allowed to rest for a set time with open-circuit terminals.

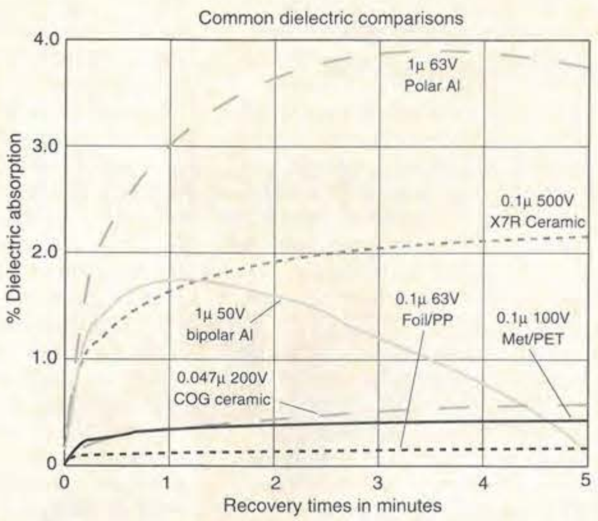


Fig. 3. Measurements using the 100MΩ impedance meter used for Fig. 2. All capacitors were charged to 10V. The effects of self discharging leakage currents can be seen on the two electrolytic capacitor curves. However this plot demonstrates how dielectric absorption varies widely with change of dielectric materials.

Finally, the recovered voltage is measured using a high impedance voltmeter.

Test circuits of various complexity have been defined in national military standards and customer specifications. However, useful comparative tests can be performed using the simplest means of a 9V battery or power supply, a 10 kΩ resistor for charging and 100Ω for discharging, a two-pole three-way rotary switch and a 10MΩ input impedance digital voltmeter.

Using a much higher input impedance meter, the recovered voltage can be observed to rise quickly initially, but continues to increase slowly for several minutes. Many digital voltmeters on their most sensitive range have an input impedance approaching 100MΩ, which is ideal for this experiment, **Fig. 3**.

Practical dielectric absorption testing is best performed in a manner matching your application – especially when choosing a sample and hold or similar capacitor. You might also need to repeat your test sequences at higher ambient temperatures. Many years ago, Bob Pease published a circuit he liked to use for this task. It provided variable charge and discharge rates and completely automated the test switching sequences for you.[4]

Capacitor fault finding

The most common failure mode is that a capacitor fails short circuit. Aluminium electrolytic types are the exception. They usually fail as a higher than normal impedance, when the available oxygen in their electrolyte has been consumed. In such a state, they are commonly referred to as 'dried'.

When measured using the low-frequency charge/discharge capacitance measurement now common in many digital multimeters, capacitance of a 'dried' capacitor may appear unchanged.

A completely open-circuit failure can be exhibited by a fuse protected tantalum. Having blown its fuse, it then becomes an open circuit.

While much less common, a metallised-film capacitor can also fail as a high esr. When subjected to excessive current pulses, the 'schoop' metal spray end connection degrades. Initially, the weakest metallic connection paths burn-out, creating local higher resistance paths. With continued application of current, these high resistance areas grow in size until eventually the capacitor has either a much increased esr, or becomes completely open circuit.

While a completely failed 'open' capacitor is easily identified, a degraded esr, incipient capacitor failure is rather more difficult. How then can a high esr capacitor be quickly identified?

Highly stressed capacitors in power supplies, and in monitor or tv eht and line-scan circuits are obvious first suspects. Another very common failure mode – albeit less well known – is in electrolytics used to block dc while coupling irregular pulse waveforms into the base of a switching transistor. These can become internally reverse polarised and so fail very quickly. Study of the circuit diagram will help you target the most likely suspects.

A dried aluminium electrolytic capacitor usually exhibits clearly visible signs of failure. The most common are deterioration of the end sealing rubber, discoloured insulation sleeve and lead out wires, or signs of leaked electrolyte on the printed circuit board.

Removing a suspect capacitor to test on a capacitance bridge capable of measuring tanδ or esr can be time consuming. Once you have removed the capacitor, it is far easier to simply replace it.

Having assessed the most obvious failure points, can a simple test be applied to check the remaining capacitors *in situ*? Most aluminium electrolytic capacitor impedance curves become a low impedance, almost flat bottomed, curve by 10 or 100kHz, being dominated by the capacitors esr. So a 10 or 100kHz impedance measurement can be used as a rough check on the capacitors high frequency esr. You need only a signal source, a known resistor for comparison and a suitable millivoltmeter or oscilloscope to measure the signal levels.

A practical measurement of this high frequency esr can be made using a 1V signal source fed to the test capacitor via a 1kΩ resistor, giving a direct reading of milliohms, 1mV equalling 1mΩ. With some organisation of leads, etc., this test can be performed while the capacitor is in circuit.

Having measured a capacitor's impedance at 10 or 100kHz, it is essential to compare this result with the maker's claims. Many electrolytic capacitor data books table a maximum 10kHz or 100kHz impedance value for each capacitor. A capacitor exhibiting double this value should certainly be replaced.

A few minutes study of such a databook proves the impossibility of applying any global rule of thumb impedances to judge whether a capacitor is good or bad. The 100kHz esr for a given capacitance value varies according to the capacitor's rated voltage, quality and physical size, **Table 1a)**.

With large-value power supply electrolytics, it is important to ensure accurate measurements down to only a few milliohms. A 10000μF 63V capacitor as used in the power supply of an audio amplifier should have a typical esr at 100Hz around 12mΩ, and at 100kHz around 10mΩ. Increase in

Table 1a). Typical impedances, in ohms, as measured at 100kHz – low capacitance values.

Capacitor	1μF	2.2μF	4.7μF	10μF	22μF	47μF	100μF
63V polycarb.	0.038Ω	0.018Ω	0.012Ω	0.01Ω			
50V bipolar Al.	2.0Ω	1.5Ω	1.0Ω	0.7Ω	0.25Ω	0.2Ω	0.12Ω
63V polar Al.	2.6Ω	1.9Ω	1.1Ω	0.95Ω	0.4Ω	0.22Ω	0.18Ω
450V polar Al.	24Ω	11Ω	5Ω	3.8Ω	1.5Ω	0.5Ω	

Table 1b). Typical impedances, in ohms, as measured at 100kHz – high capacitance values.

Capacitor	1000μF	2200μF	4700μF	10000μF
25V polar Al.	0.060Ω	0.036Ω	0.024Ω	0.022Ω
63V polar Al.	0.040Ω	0.025Ω	0.011Ω	0.010Ω

The *Capacitor Wizard* esr meter

Independence Electronics[5] has designed a low-cost 100kHz impedance meter aimed at servicing personnel. It simplifies in-circuit capacitor impedance measurements.

Test signal levels have been tailored to permit in-circuit measurement of suspect capacitors without being of sufficient voltage to turn on semiconductor junctions. A supposed 'good' capacitor sounds a beeper. While this beeping impedance level can be adjusted, the factory default sounds the beeper for impedances less than 0.5Ω. A meter scaled from 0.1Ω to 30Ω indicates the approximate impedance measured.

Claimed to be usable for capacitors of 1μF and above, I found some care was needed even with capacitors of 10μF. Many new stocks of modern miniature electrolytics have an impedance near 1Ω, and so did not sound the beeper.[6]

Similarly, some large-value capacitors known to be high esr failures, but having an impedance less than 0.5Ω, sounded the beeper, wrongly suggesting they were still good.

This of course is to be expected.

Unfortunately, the test meter and its accompanying literature incorrectly states that for most capacitors, an impedance less than 0.5Ω indicates a good capacitor.

Putting these problems to one side, does the meter work ? I performed three quite different tests. First of all I compared its readings using electrolytic capacitors previously tested for esr at 100kHz using a capacitance bridge. Capacitance values used, ranged from 1μF to 10000μF

Within the limitations of its meter scale, electrolytic capacitors larger than 1μF, displayed good agreement for both methods.

Using a low loss 1μF polypropylene capacitor in series with a variety of low value non-inductive resistors, I again found good agreement, confirming acceptable factory calibration.

By chance my son arrived with his Grundig tv, which had developed an intermittent colour decoder fault, so I took the opportunity to try this meter on his set. All but two electrolytic capacitors in this chassis caused the beeper to sound. The 'failures' were 0.47μF, 100V and a 4.7μF, 350V components, both of which were in fact good when removed for a bridge measurement.

The user needs to generate a realistic table of expected impedances by capacitor size, capacitance value and voltage rating. Armed with such a table, I consider this meter could then be most useful in a repair workshop with no better facility for measuring esr.

The impedance tabulations supplied with the meter, in my view however, are simplistic in the extreme and so are best ignored.

Intermittent failures

Most capacitors failures are identified as a permanent and very low resistance or short circuit. Exceptions are found in aluminium electrolytics which usually fail as a higher than normal impedance and high equivalent series resistance, symptomatic of a 'dried' capacitor. A completely open circuit failure can be demonstrated by a failed, fuse protected, tantalum.

A metallised film capacitor subjected to excessive current pulses can also fail as a high esr. The sprayed metal end connection degrades as the weakest metallic connection paths burn-out, creating local higher resistance paths. With continued application of excess current, these high resistance areas grow in size until eventually the capacitor has either an increased esr, or becomes completely open circuit.

A multilayer ceramic capacitor which has been cracked by handling or soldering, with change of temperature or flexing of the printed board, can sometimes exhibit an intermittent short circuit effect. There's more on this in the panel called 'Capacitor handling.'

A fault location in a metallised film capacitor used at low voltage and with such high circuit impedances that it does not receive sufficient energy to permit self-healing, might exhibit a reduced insulation resistance.

During manufacture, such capacitors are 'cleared' using overvoltage, so should not need to self-heal in normal service. However moisture or solvent ingress during washing, or surface wash residues can contribute a problem. This lower than usual insulation resistance may be intermittent in nature, or vary with temperature or humidity.

One reader who suspected he had a problem with a metallised polycarbonate capacitors possibly having an intermittent lower insulation resistance asked how this might be measured.

An extremely simple test circuit should suffice. Ideally, the test capacitor should be subject to the same voltage as seen in service. Assuming this lies within the range 3V to 15V, an *HEF4044B* set-reset latch can be used to test four capacitors simultaneously.

In **Fig. 4**, I have used 470kΩ resistors to present a high source impedance to the capacitor under test. Higher or lower values could be used, to replicate your circuit conditions.

Having installed the suspect devices, the reset switch is briefly closed to reset the circuit. Any intermittent low insulation resistance in any of the capacitors being tested turns on the respective led. This led remains lit until the reset switch is again activated.

Normally, current drain is extremely small so if necessary, batteries could be used to power the circuit continuously for several months.

It may be that your suspect low insulation resistance is not a capacitor but a track on a printed board. It could have halides remaining on its surface due to improper washing. Change of temperature or humidity can then produce an intermittent low resistance condition. The test circuit is suitable for tracking this problem too.

With suitable matrixing methods, the circuit could be easily expanded to test large numbers of capacitors simultaneously, as a form of low voltage high impedance 'burn in' having automatic indication of failure.

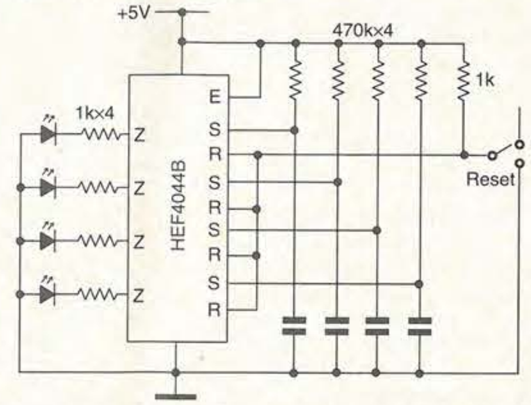


Fig. 4. Simple test circuit designed to indicate an intermittent low insulation resistance at low test voltages in high impedance circuits. While test capacitors are shown, these could in practice easily be suspect printed circuit board tracks.

Capacitor handling

Incorrect soldering methods can damage capacitors, but since most capacitor makers' catalogues specify acceptable soldering times and methods, I do not propose to cover soldering methods in detail.

Remembering that all plastic film dielectrics used to manufacture film capacitors soften and expand at temperatures below that at which solder melts, excessive time and temperature must obviously be avoided.

Ceramic capacitors are probably the most easily damaged by incorrect soldering. Almost all makers specify a pre-heat period sufficient to allow the capacitor dielectric to stabilise at a temperature intermediate between room and soldering temperature. If not observed, thermal shock can cause microscopic or larger cracks which cause the capacitor to fail, usually as a short circuit.

Note that this damage may not result in immediate capacitor failure.

Because many capacitors look mechanically solid or rugged, many users crop or form leads in such way that damage results. If the capacitor maker specifies minimum bending, cropping or soldering distances, these should be strictly observed.

Good practice is to always support the leadwires close to the capacitor body, when bending or cropping leads. Again this is most important with ceramic dielectrics, which can easily become damaged by incorrect handling – especially bare chips intended for surface mounting. Many early failures have resulted from poor handling or cropping methods.

Remember also that humidity protection of encapsulated or 'E' cased capacitors can be seriously reduced by incorrect lead bending or forming. Most lead wires are solder coated or plated with materials not easily 'wetted' by plastic resins and the moisture resisting path lengths may be quite short.

Peculiar early failures can result if handling damage allows the ingress of moisture or board washing solvent.

Should you find early failures occurring, a good rule of thumb is to assume that almost certainly, these will result from poor handling or soldering practices in your assembly.

impedance to 36mΩ at 100Hz obviously triples the power dissipated in the capacitor as heat. In such a case it should be replaced, **Table 1b**).

In summary

Accurate measurements of capacitors – especially of esr at high frequency – requires state of the art equipment and methods. However with these articles, I hope I have been able to encourage experimental measurements using more accessible equipment. ■

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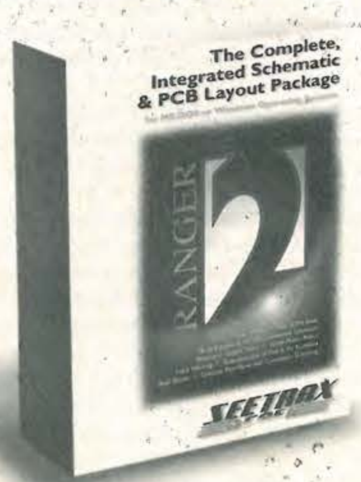
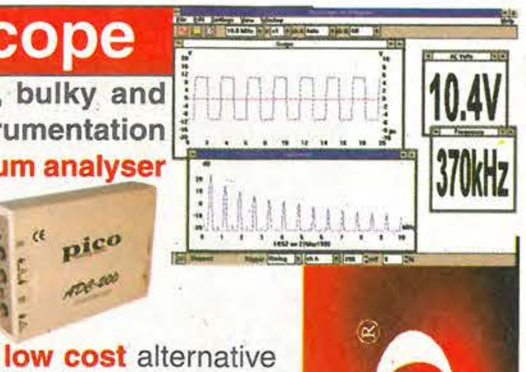




Are genetically designed Yagis worthwhile? Richard Formato investigates.

Genes and Yagis

The genetic algorithm is a powerful new antenna design and optimisation tool that is receiving progressively more attention. A natural question is "How good are genetic-algorithm-designed antennas?"

This note looks at that question by comparing four 12-element Yagis designed using genetic-algorithms. It does not examine how genetic algorithms work because there are many good references. Several are listed later.[1-6]

Here I emphasise Yagi performance, and how it changes in response to changing the parameters.

Richard A. Formato, Ph.D., WW1RF

Genetic algorithm in action

The genetic algorithm searches a 'decision space' which is defined by specifying minimum and maximum values for each antenna parameter. Only antennas falling within these limits are allowable solutions to the optimisation problem. This is a characteristic of genetic algorithms that gives the antenna designer exceptional flexibility.

Each element in a Yagi-Uda array has three design parameters: length, spacing, and radius. The minimum/maximum range of each parameter can be set on an element-by-element basis, but the usual approach is to restrict all elements in the same way – with occasional exceptions as discussed below.

For the arrays described here, the element lengths were restricted as follows. All dimensions are in wavelengths, or 'waves'.

reflector	0.35-0.65 wave
driven element	0.35-0.60 wave
directors	0.3-0.6 wave

Element spacing was 0.05-0.5 wave, thus limiting the longest boom to 5.5 wavelengths. For designs 1-3, the element radius was constant at 0.003369 wave, while design design 4 allowed driven-element radii from 0.001 to 0.0075 wave.

The standard Yagi configuration is used. Here, element 1 is the reflector, and element number 2 is the driven element.

Figure of merit

The 'goodness' a particular Yagi design is determined by a figure-of-merit which is specified by the designer. For the arrays in this note, the figure-of-merit was:

$$FoM = \frac{aG - b|Z_o - R_{in}| - c|X_{in}|}{a+b+c}$$

Variable G is the forward gain – zero degrees azimuth – in dBi, while Z_o is the feed system characteristic impedance, in this case 50Ω resistive. Variable R_{in} and X_{in} are the Yagi's input resistance and reactance, respectively.

This figure-of-merit is used in reference 1, which is why it is used here. A genetic algorithm allows the antenna designer to choose any figure-of-merit that reflects the desired balance between various antenna performance parameters. For example, front-to-back or front-to-rear ratio, or maximum sidelobe level could also be included if the designer wished to optimise against these parameters.

Weighting coefficients a, b and c determine the relative importance of each antenna performance parameter. For all designs below, the coefficient a is 40. For designs 1 and 2, b=c=1, which are the values suggested in reference 1.

In design 3, the Yagi input impedance was removed from the figure-of-merit by setting b and c equal to zero. In design number 4, the input impedance was weighted somewhat more heavily by increasing the coefficients to b=2 and c=3.

Optimised Yagis

Optimisation was done by a piece of software called *Yagi Genetic Optimiser*[7] which computes antenna performance using the *Numerical Electromagnetics Code*, Version 2, double-precision, or NEC-2D.[8]

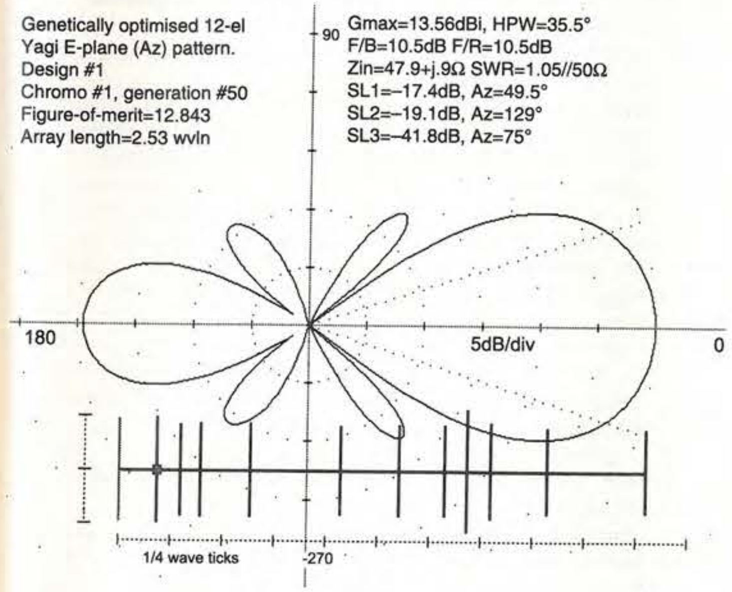
Seven segments were used for each array element in the NEC-2D model. Performance of the genetically designed arrays shown in **Table 1**. Important parameters include the boom length (wavelengths), forward gain (dBi), half-power (–3dB) beam width (degrees), input impedance (ohms), standing-wave ratio relative to 50Ω, front-to-back and front-to-rear ratios (dB//*G*), and maximum sidelobe level (dB//*G*).

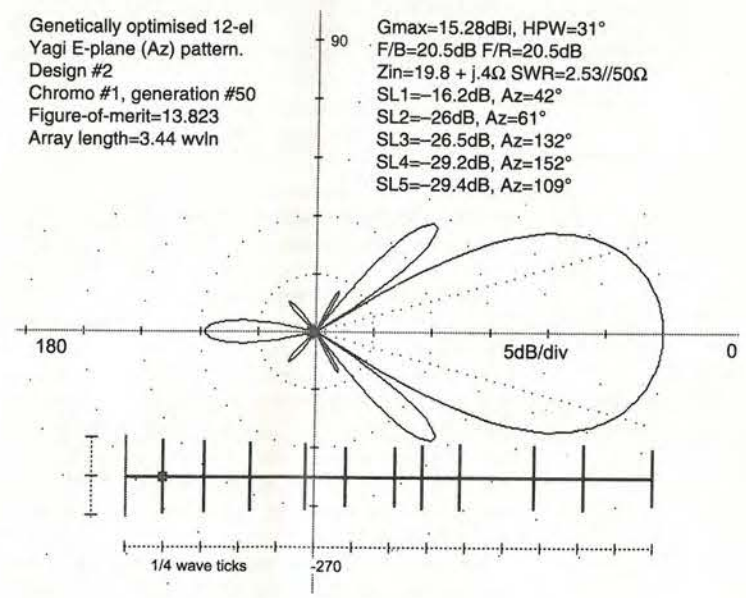
Designs 2, 3 and 4 are the optimised Yagis, corresponding to the three sets of coefficients b and c, (1,1), (0,0) and (2,3), respectively. Design number 1 is a suboptimal design that appeared in the optimisation run for design number 2. It is included to illustrate another important genetic algorithm characteristic: a genetic algorithm does not produce a single 'best' design, but instead produces a *group* of designs, with each design in the group ranked from best to worst.

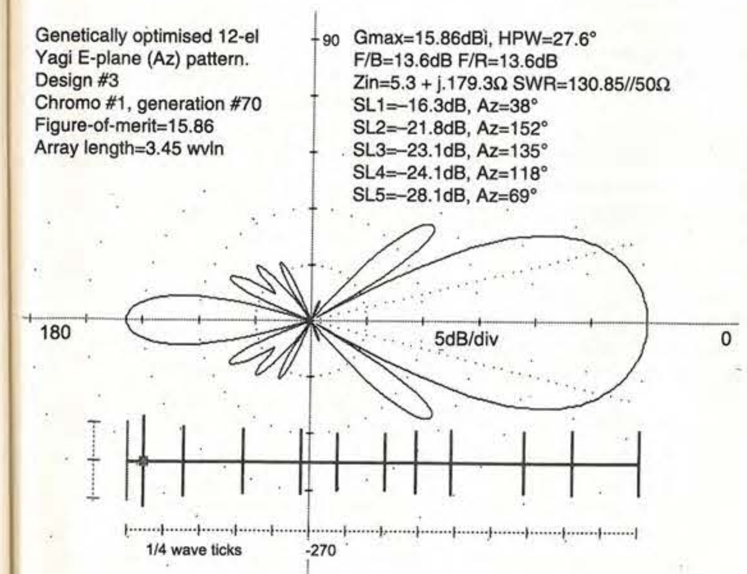
This feature can be very useful, because even suboptimal designs may be attractive. Design number 1, for example, may fill a real need because of its short boom length and excellent

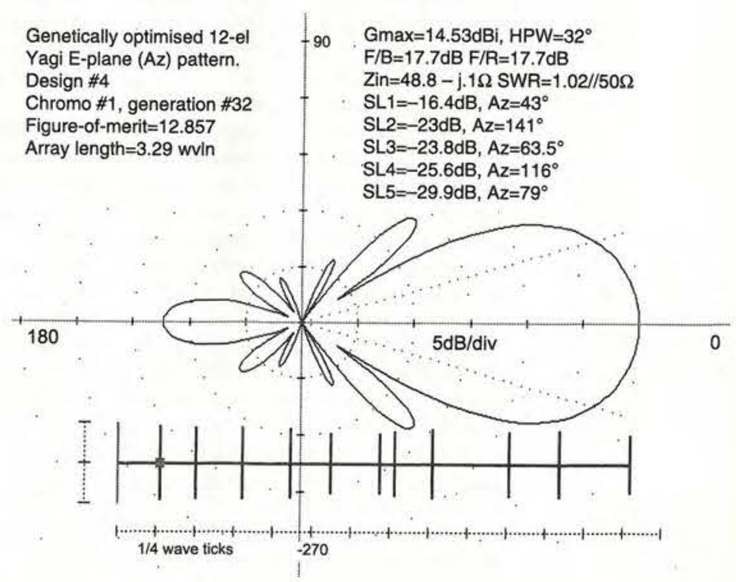
Table 1. Performance analysis of the four Yagi designs.

Ant #	*L*	*G*	HPBW	Z_{in}	SWR	F-to-B	F-to-R	MaxSLL
1	2.53	13.56	35.5	47.9+j0.9	1.05	10.5	10.5	–17.4
2	3.44	15.28	31.0	19.8+j0.4	2.53	20.5	20.5	–16.2
3	3.45	15.86	27.6	5.3+j179	131	13.6	13.6	–16.3
4	3.29	14.53	32.0	48.8-j0.1	1.02	17.7	17.7	–16.4









Performance plots of the four genetically designed Yagi antennas.

Table 2. Dimensions and spacings for the four Yagi designs.

	Design #1		Design #2		Design #3		Design #4	
Element	L	S	L	S	L	S	L	S
1(REF)	0.4794	0.0000	0.5006	0.0000	0.5006	0.0000	0.5006	0.0000
2(DE)	0.4853	0.1824	0.4549	0.2388	0.5784	0.1082	0.4588	0.2741
3	0.4165	0.1135	0.4388	0.2671	0.4400	0.2671	0.4365	0.2247
4	0.4329	0.0924	0.4318	0.3006	0.4188	0.4047	0.4341	0.3006
5	0.4341	0.2388	0.4141	0.3641	0.4188	0.3871	0.4259	0.3076
6	0.4047	0.4329	0.3624	0.2582	0.3624	0.2476	0.3647	0.2582
7	0.4224	0.2847	0.3718	0.3218	0.3718	0.3218	0.3718	0.3218
8	0.4176	0.2194	0.4012	0.1806	0.4012	0.2088	0.4012	0.0959
9	0.5671	0.1065	0.4200	0.2424	0.4200	0.2424	0.4212	0.2424
10	0.4388	0.1171	0.4035	0.4876	0.4035	0.4876	0.4035	0.4876
11	0.3906	0.2706	0.4176	0.3218	0.4176	0.3218	0.4176	0.3218
12	0.3847	0.4735	0.3471	0.4559	0.4224	0.4559	0.3482	0.4559

input impedance, even though its gain and FB/FR are worse than that of longer Yagis.

Antennas optimised using the genetic algorithm do indeed reflect different weighting in the figure-of-merit. In design number 2, for example, b and c were chosen to emphasise gain while still controlling the input impedance. The resulting antenna has a gain of 15.28dBi – a very respectable number – and it is nearly resonant with an input resistance of 19.8Ω. This moderate resistance level is easily matched, so that this antenna provides very good gain and impedance performance.

Gain above the theoretical maximum?

By contrast, design number 3 was optimised purely for gain, and nothing else. Its G of 15.86dBi is exceptionally good. In fact, this Yagi's gain appears to be slightly above the maximum theoretical gain for a 3.45-wavelength long boom as shown in the ARRL's Antenna Book.[9]

But, because the gain was maximised without any consideration of the input impedance, the Z_{in} figure for this design is a very poor match to 50Ω. Of course, it is possible to match this antenna, but it is almost certainly not worth the effort in view of designs 2 and 4.

Finally, the figure of merit coefficients for Yagi number 4 – chosen after the results of the two previous optimisation runs were analysed – were selected to improve further the balance between *G* and Z_{in}. In addition, the driven-element radius in design number 4 was allowed to vary, instead of being fixed at 0.003369 wave.

The reason for this change is that the self-impedance of a centre-fed dipole passes through a maximum as its diameter increases. This effect can be used to advantage to provide a better match to 50Ω because Yagis tend to be low-impedance antennas. The genetic algorithm confirmed this by increasing the driven-element radius to 0.005767 wave.

Best performer

Yagi number 4 exhibits very good performance. Its gain of 14.53dBi is only about 1.2dB less than the maximum theoretical gain for the boom length.[9] And, quite significantly, this array provides a near perfect 50Ω match.

Feeding this antenna with 50Ω coaxial cable requires only a balun. Completely eliminating any kind of matching network probably makes up for a good part of the 1.2dB gain reduction. The result is a Yagi that is simpler, less expensive, easier to adjust, probably has greater bandwidth, is less likely to fail than designs with matching networks, and requires little if any maintenance.

W1JR[10] makes a compelling case that Yagis should be designed to match 50Ω directly, and there are many amateur and professional antenna designers who share that view. Designs like Yagi number 4 show that achieving this objective with good overall performance is certainly possible. It is arguably the preferred approach.

The NEC-2D computed E-plane (azimuth) radiation patterns and a scale representation of the array geometry appear in the plots. It is interesting that element lengths and spacings in the genetically optimised antennas are neither uniform nor tapered as they are in deterministically optimised arrays.

Counter intuitive

Genetic-algorithm-optimised Yagis look 'different', which is another very interesting aspect of genetic algorithm antenna design. Genetically-designed antennas are often counter-intuitive and do not resemble what you would expect. This characteristic makes them intriguing, because the designer cannot predict what the next 'best' antenna might look like.

Dimensions – element length, *L*, and spacing, *S*, both in wavelengths – are shown in **Table 2**. All elements are 0.003369 wave radius, except element 2, the driven element, in design number 4, which has a radius of 0.005767 wave.

In summary

This note describes four genetically designed Yagis that illustrate how effective a genetic algorithm can be in designing complex antennas. Amateurs interested in antennas are likely to hear more about genetic algorithms, and may wish to learn more about them.

The genetic algorithm is a state-of-the-art design tool that is truly revolutionary in nature. Its potential in antenna design is just beginning to be explored, and may lead to some very interesting and unusual antennas. ■

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8. NEC-2D is available from the Applied Computational Electromagnetics Society (ACES), Attn: Dr Richard Adler, ACES Executive Officer, ECE Department, Code ECAB, Naval Postgraduate School, 833 Dyer Road, Room 437, Monterey, CA 93943-5121 USA. NEC-2 download files are also available on the web at: http://www.qsl.net/wb6tpu/swindex.html.
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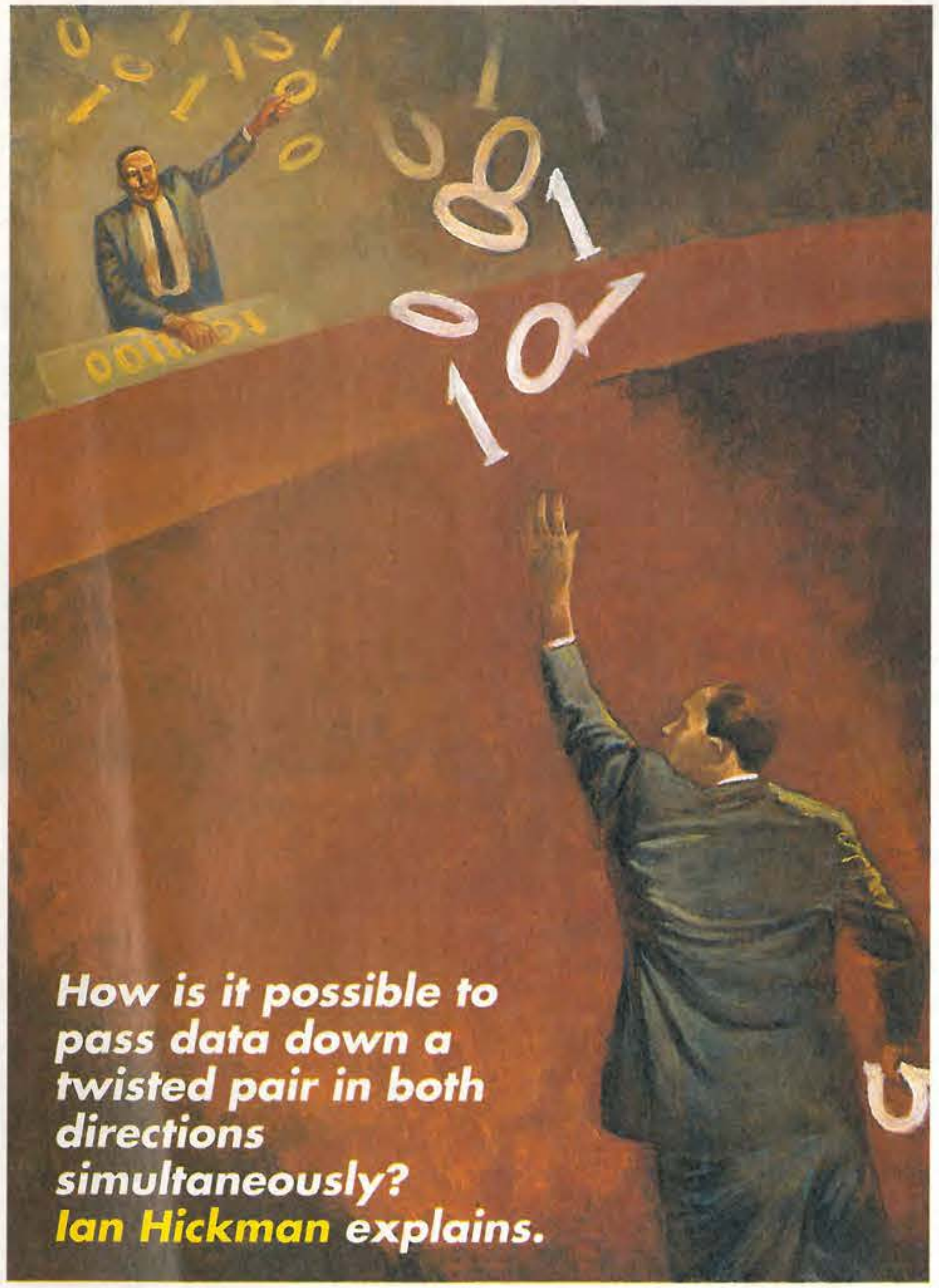


Phantom data

The prelude to this article, last month, looked at running n telephone lines over fewer than n physical pairs. I demonstrated that using phantoms – both full phantoms and an earth phantom – 2^n lines could provide 2^{n+1} circuits.

But of course, one takes it for granted that a telephone circuit is 'full duplex' – capable of carrying information in both directions simultaneously. This means that both parties to the call can speak at the same time if they so wish, and each will hear the other – except on some very long connections where echo suppressors are used. So if you count 'one way' channels, 2^n lines can provide 2^{n+2} circuits.

Data connections are often simplex; that is to say that data can be sent from A to B, and also from B to A, but not at the same time. This obviously simplifies matters, since a send/receive switching function at each end of the link, together with some protocol to control the communications, gives each sender a clear line and each receiver an input consisting solely of the desired data.

In the earliest days of telephony, the same scheme was used, the handset being provided with a 'press-to-talk', or ptt, switch. With the exception of the military 'Pressel,' this switch was rendered obsolete with the introduction of a wound hybrid. Until recently, such a hybrid could be found in the traditional black rotary-dial telephone. The Pressel ptt still survives though in military comms, both line and radio.

How the hybrid function is implemented nowadays in your nine pounds ninety five pastel coloured all-in-one handset/phone I don't know, but the traditional arrangement was with a transformer hybrid. This separates the signals on the bidirectional two wire subscriber's line – or sub's loop – to the local exchange into a four wire line. The go pair connects to the microphone and the return pair to the earpiece, **Fig. 1a)**.

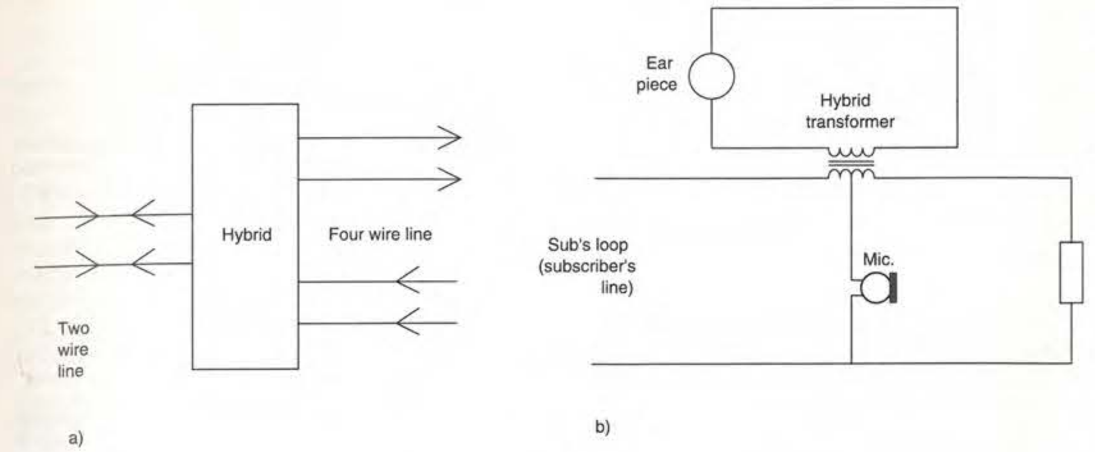


Fig. 1a). A hybrid converts a bi-directional two wire interface into a four wire interface having separate go and return paths. b). Skeleton simplified voice circuit of a telephone, omitting dialling and other features.

Two- to four-wire interface

The way it works is illustrated in **Fig. 1b)**, in highly simplified form. Direct voltage applied to the sub's line by the Central Office Battery at the local exchange causes current to flow through the microphone, traditionally of the carbon-granule type.

Sound pressure from the speaker's voice impinges on the diaphragm, varying the mic's resistance and resulting in audio frequency components of line current. Audio signal current flows into the primary centre tap of the hybrid transformer. Some flows to the left to the exchange and ultimately to the other party to the call, and some to the right, into the 'line balance'.

If these two currents are equal, there is no net resultant flux on the core of the transformer. As a result, none of the audio appears in the earpiece. Half of the audio is delivered to the line, and half wasted in the line balance.

In practice, the loss in the line balance is reduced by offsetting the tap, so that more than half of the audio goes to the line. This means that the cancellation is not complete, so a small fraction of the audio appears also in the earpiece. This is quite deliberate and is called 'sidetone'.

Too little sidetone causes the circuit to sound 'dead', encouraging the speaker to shout, while too much causes the speaker to lower his voice unduly.

In principle, the line balance could be a 600Ω or 140Ω resistor, depending on whether the sub's loop is an overhead open wire line or a pair in an underground cable. But life is not that simple.

In practice the line impedance varies with frequency, so the line balance will include some reactive components, and of course will be dc blocked by a capacitor. This avoids drawing unnecessary current from the central office battery. But the fact remains that the purpose of the hybrid is to provide the two- to four-wire interface indicated in Fig. 1a).

Sending data by wire

Data is commonly sent over a subscriber's loop, as when the Internet is accessed via a modem. But for shorter links, between buildings on a common site, or rooms within a large building, there is often a requirement for faster data transfer rates than can be accommodated on a phone line.

Various protocols are used for short links, such as RS232, RS4xx, etc, while for local area networks, protocols such as Ethernet, Token Ring, etc are used. Many of these protocols use simplex working, and I wondered whether duplex working, complete with the use of phantoms, could permit the transfer of more data over a given circuit. This could be useful in special circumstances, where it was difficult or expensive to install extra cables to cope with an increase of traffic.

Various manufacturers now produce special-purpose drivers and receivers for sending high speed data over balanced twisted pairs. A good example is the *EL214x* series from Elantec, some samples of which I recently acquired. Both *EL2140* and *EL2141* accept input data in either balanced or unbalanced format and provide a balanced output drive for lines such as twisted pairs – with or without overall screen.

The *EL2142* is a matching line receiver featuring a common mode rejection ratio, or cmrr, in excess of 60dB at 10MHz, and a frequency response extending to beyond 100MHz.

Figure 2 shows a pair of these devices being used to transmit data over a twisted pair, which is driven from – and terminated in – its characteristic impedance, to avoid reflections occurring on the line. In principle, the same line can carry another, entirely independent, data stream, using a phantom.

The arrangement is shown in the *Typical Applications* sec-

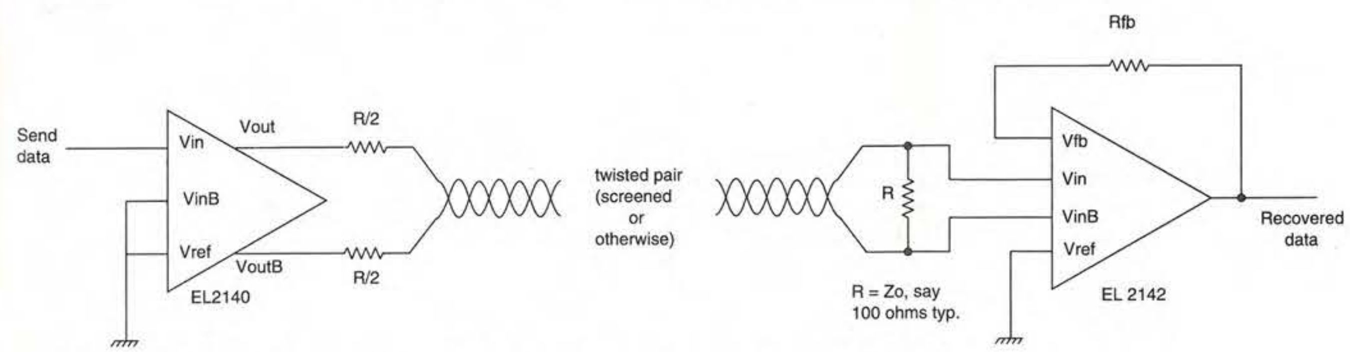


Fig. 2. Sending high speed data over a balanced line such as a twisted pair, using ICs designed for the purpose.

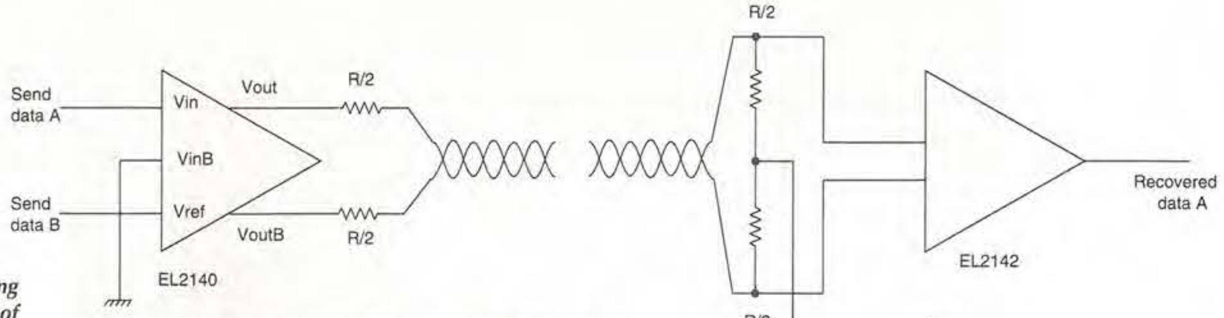
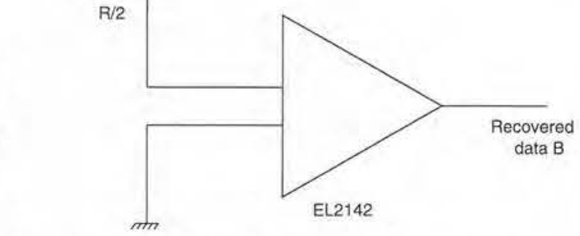



Fig. 3. Sending two streams of data over a twisted pair, using an earth phantom, as shown in the EL2140 data sheet.

tion of the *EL2140* data sheet, and is reproduced here as **Fig. 3**. In the data sheet, the characteristic impedance of the balanced line is assumed to be 100Ω. The four resistors shown as *R*/2 in Fig. 3 are therefore each 50Ω.

The scheme works because of the internal arrangement of the *EL2140*. Gain of the device is fixed at one to one from V_{in} to V_{out} and one to minus one from V_{in} to V_{outB}, assuming V_{inB} is grounded. Data A would usually be applied to V_{in} and V_{inB} as an unbalanced signal, as shown in Fig. 3, but could be applied as a balanced signal if so desired.

So, assuming V_{ref} is grounded, ±1V applied at V_{in} would give ±1V at V_{out} and ∓1V at V_{outB}. But if V_{ref} were held at +1V, then the two antiphase output signals would both be riding on a standing level of +1V. In other words, V_{ref} sets the common mode output level of the two outputs.

Now the V_{ref} input itself has a bandwidth of over 100MHz, almost as large as the bandwidth of V_{in}. So high speed data can be fed to V_{ref}, and will appear as a common mode output, simultaneously with totally independent balanced mode data, applied via V_{in}.

Two circuits, one way on one pair

In practice, certain limitations may spoil or even prevent such operation entirely.

The first point concerns the return path for common mode data carried on the phantom. The data sheet simply shows an earth symbol at each end of the link. But as I noted in my earlier article, an earth return phantom may be subject to excessive noise injected between the two ends of the link, via the earth path. That possibility could be largely negated here, by using a screened twisted pair, with the outer screen forming the earth return path.

The second point concerns the characteristic impedance of the phantom circuit. Assume for the moment that the cable is equipped with an overall screen, which is used as the return path for the earth phantom. Now, the common mode data, data B, uses a circuit consisting of the two twisted wires – considered as effectively shorted together – as the go path and the screen as the return.

This circuit will itself have some characteristic impedance: probably not the same as that of the balanced twisted pair, but probably not differing from it by a large factor.

But as shown in the data sheet, and reproduced in Fig. 3, the phantom is effectively unterminated at the receive end. Reflections will therefore be experienced on the line. This will make it unsuitable for high speed data – the longer the line the lower the data rate will have to be to allow any ringing to subside before the data is sampled.

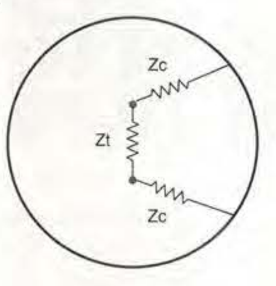
Owing to the common mode rejection afforded by the *EL2142* operating on the balanced data, this speed limitation will not apply to data A in Fig. 3 – only to data B on the phantom circuit.

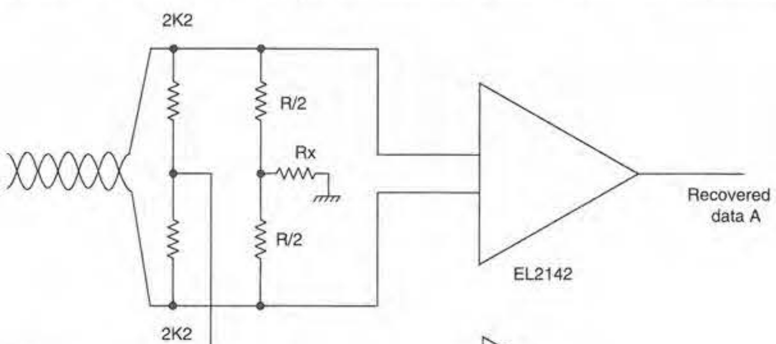
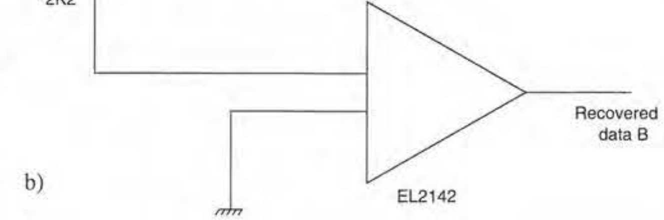
Termination issue

To avoid this speed limitation on data B, the phantom circuit needs to be properly terminated. This involves knowing the impedance of the cable in unbalanced mode, i.e. considered as a coaxial cable with a two strand inner. This will depend on the impedance from line to line Z_t, and the impedance from each line to ground Z_c, **Fig. 4a)**.

Clearly, if Z_t is very much higher than Z_c, then the balanced mode impedance Z_b is approximately $2Z_c$ and the unbalanced mode impedance Z_u *lower* than this, at $Z_c/2$. But if Z_c is very much higher than Z_t, then Z_b is approximately equal to Z_t, and Z_u $(=Z_c/2)$ could be much *higher* than Z_t.

a)



b)

Fig. 4a). Characteristic impedance of a screened twisted pair is different in balanced mode – i.e. normal mode – from in unbalanced mode, i.e. common mode.
b). This arrangement allows both the balanced line and the phantom each to be terminated in their own characteristic impedance.

In practice, Z_u is likely to be less than Z_b, but higher than $Z_b/4$. So the phantom circuit can be properly terminated as shown in Figure **4b)**, where $R_x=Z_u-Z_b/4$. The value of *R*/2 can be adjusted to allow for the parallel value 2.2kΩ, although this is so high compared with $Z_b/2$ as to be almost out of sight.

The lower *2142*, recovering data B, is effectively driven from a source resistance of a little over 1kΩ, which is low enough to support data rates well beyond 10MHz, given the device's very low input capacitance of 1pF. It is true that the phantom circuit will still be driven from a mismatched source – i.e. $Z_b/4$ instead of Z_u – but with the receive end properly terminated, there will be no problems due to reflections.

Using the phantom as above furnishes two data paths in the same direction over the one twisted pair. It is also possible to have two paths over the same pair, but in opposite directions, giving duplex working.

But before moving on to that, it is worth clearing up one obvious query: If you have two wires and an overall screen in the cable, why not send data A down one wire and data B down the other, both using the screen as a common return?

The answer is 'crosstalk'. Capacitance between the two wires, and their mutual magnetic coupling, mean that while you might apply data A to one wire and data B to the other at the send end, by the time they reach the receive end they are likely to be inextricable entangled.

Two circuits on one pair – both ways

Providing duplex working, permitting independent transmission of data in both directions simultaneously, simply requires a two wire to four wire transition, as in Fig. 1a), at each end of the link.

The hybrid-connected transformer, as used in telephones, has limited bandwidth and is unable to pass dc or low frequencies. But for data applications a wideband hybrid is needed. **Figure 5** shows just such an arrangement, implemented with ICs and resistors. The way it works is very simple.

Assume that the amplitude of send data B is ±2V. When it is at the positive level, the voltage at points P and Q will be +2V and -2V respectively, as in Fig. 5.

For the moment, assume that the other end of the link is sending no data, so that the two *R*/2 resistors there are effectively returned to ground. As the line, whose characteristic impedance *R*, is now matched at both ends, the voltages at points M and N will be +1V and –1V respectively. So, by virtue of the 2.2kΩ and 1.1kΩ resistors, the voltage at V_{in} of IC_4 will be zero, and zero likewise at V_{inB}.

Assuming that the line is well matched at the far end, IC_4 is completely 'blind' to data sent from data B. Points P and Q are therefore virtual earths, and via the 1.1kΩ and 2.2Ω resistors, IC_4 sees the arriving data A at two thirds of its received amplitude.

Incoming balanced data A sees a line termination of *R* in parallel with 6.6kΩ – in practice just slightly below the line's characteristic impedance. The position for outgoing data B is slightly different. In addition to the line current flowing from P to M via *R*/2, some antiphase current flows to M from Q via 3.3kΩ. So the two half-termination resistors *R*/2 are effectively *R*/2 in parallel with –3.3kΩ. Thus the send end termination is in practice just slightly higher than *R*.

And both ways at once?

In theory, it should be possible to combine the phantom-data scheme of Fig. 3 with the hybrid data scheme of Fig. 5, to provide two circuits over one pair in both directions simultaneously. The data on the phantom is sent by applying it to the V_{ref} input of an *EL2140*, which also transmits the balanced data, as in Fig. 3.

To receive the phantom data at the other end, a hybrid is

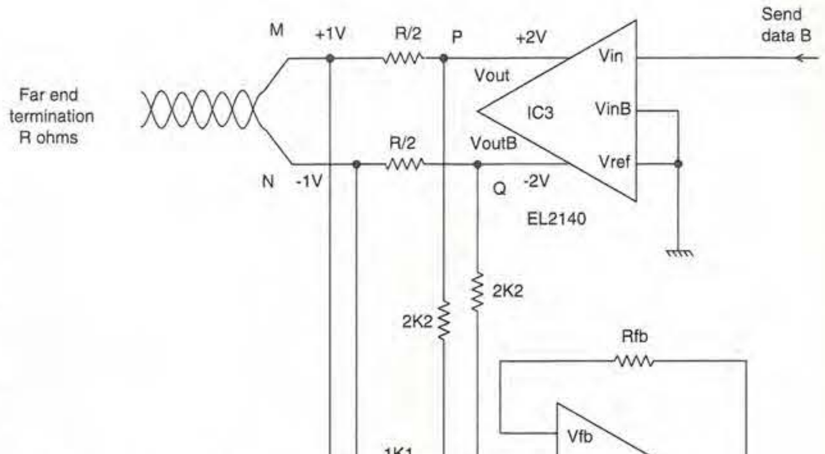
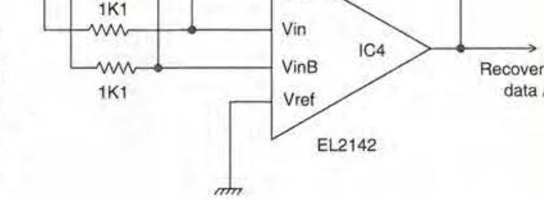



Fig. 5. A hybrid junction arrangement, interfacing between the bidirectional two wire line and the data send and data receive paths.

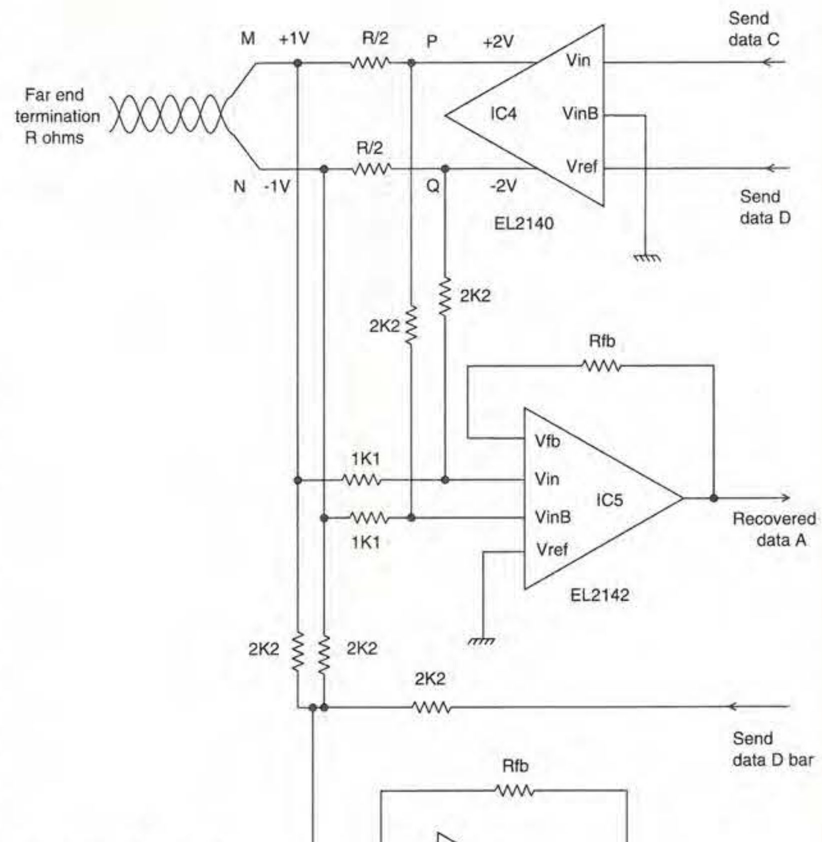
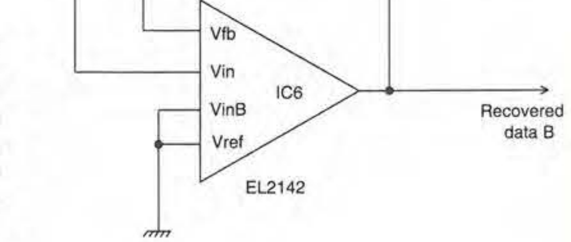



Fig. 6. In principle, the arrangements of Figs 3 and 5 can be combined to permit bidirectional data transmission on both the balanced circuit and the phantom.

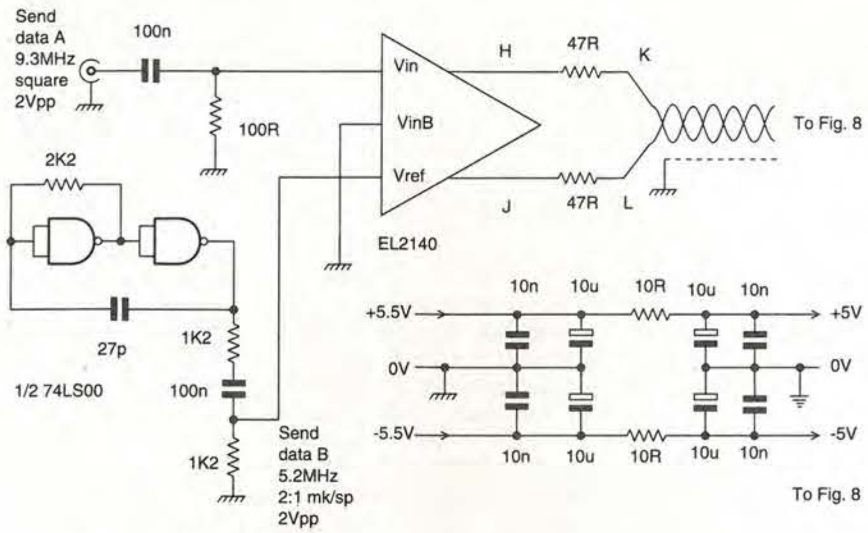


Fig. 7. One end of an experimental link designed to explore the possibility of sending and receiving two data streams in each direction simultaneously. This end is send only.

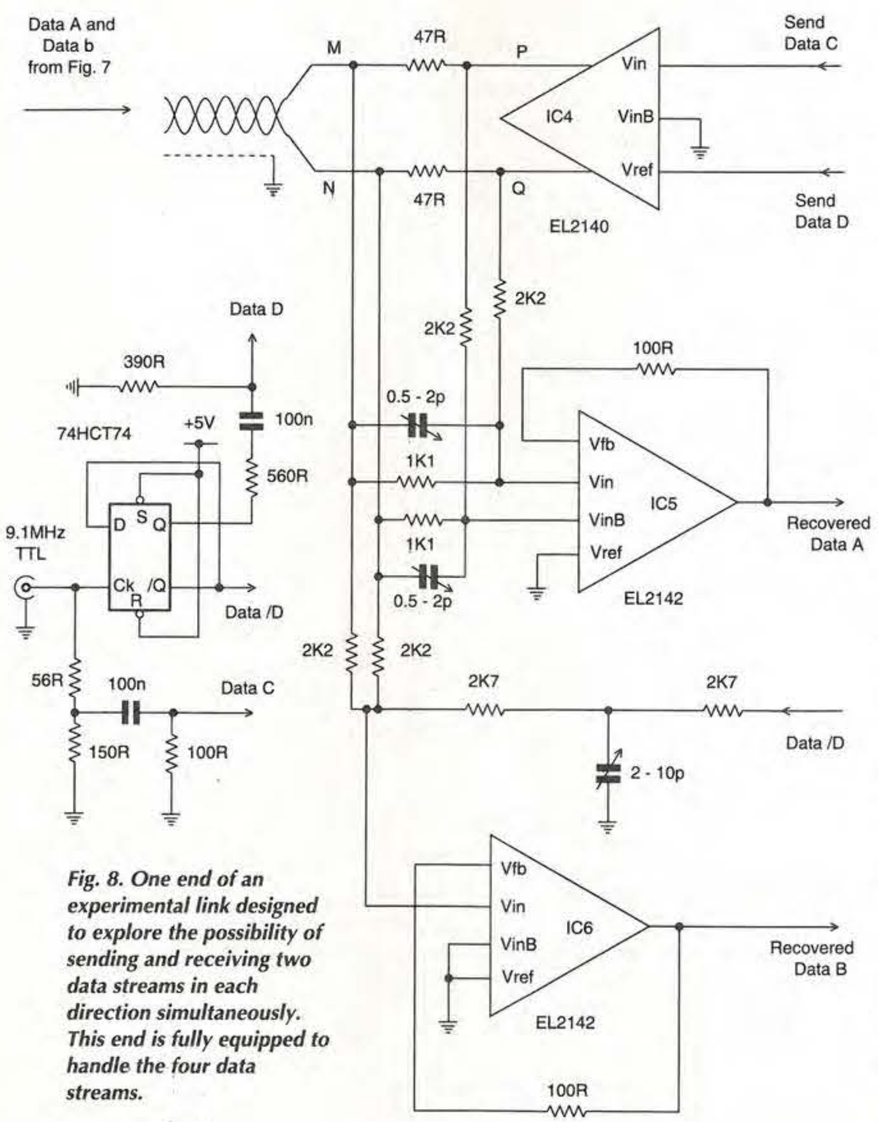


Fig. 8. One end of an experimental link designed to explore the possibility of sending and receiving two data streams in each direction simultaneously. This end is fully equipped to handle the four data streams.

needed for the phantom circuit, in addition to the hybrid for the balanced data shown in Fig. 5. This is arranged with the aid of a second *EL2142*, shown as IC_6 in **Figure 6**.

Incoming common-mode phantom signal data B, arriving from the far end, is accepted by IC_6 via the two 2.2kΩ resistors connected to its V_{in} terminal. It will also, of course, be subject to the outgoing phantom data D, but this is outphased by applying the inverse signal, data $\overline{D}$, to V_{in} of IC_6 via another 2.2kΩ resistor.

One important point to note is that here the possibility of terminating the phantom in its own characteristic impedance has been lost. In Fig. 6 the phantom circuit is terminated – and driven – by two resistors *R*/2 in parallel, or just one quarter of the impedance of the balanced pair.

Whether this would be a fatal flaw in the scheme was a matter of conjecture. Even if not, there were plenty of other potential snags and pitfalls, so the only way to be sure was to try it out for real.

Would the theoretical link work?

I managed to find a 5m length of screened twisted pair. I had no information as to its impedance, either as a balanced pair or as a two-strand-inner to screen. Nevertheless, in the absence of anything more suitable, it was pressed into service.

A full complement of transmit and receive channels, as in Fig. 6, was made up at the right hand end of the link. For speed, the other end implemented only the two transmit channels, as in the left hand side of Fig. 3. This was furnished with two independent data sources, data A and data B, with different clock rates.

At the right hand end, an *EL2140* transmitted data C and data D, at two different clock rates, both different from data A and data B. As there were no receive circuits for these at the left hand end of the link, their purpose was solely to provide outgoing signals, to test the efficacy of the hybrid arrangements.

In the absence of any data on the impedance of the cable, the correct value for the four resistors *R*/2 was determined by experiment. Using a single signal, send-data A, various values were tried to find that which resulted in a clean waveform on the line, indicating an absence of reflections. The appropriate value turned out to be 47Ω, indicating that the impedance of the balanced line was 100Ω or a shade under.

The circuits of the two ends of the link, as finally developed, are shown in **Figs 7** and **8**. In Fig. 7, two entirely independent and unrelated sources were used. Data A was a 9.3MHz squarewave from a 10Hz to 10MHz video oscillator, and can thus be taken as simulating a repeated 0101 data sequence at an 18.6MHz clock rate.

The 74LS00 oscillator generated a 5.2MHz ttl output with a two to one mark space ratio. It can therefore be taken as representing a repeated 011011 sequence clocked at 15.6MHz.

At the other end of the link, **Fig. 8**, the two transmitted data streams served solely to load the system, testing the efficacy of the hybrids. So for convenience, a single 9.1MHz data source was used, furnishing data C, and after a divide-by-two stage, also data D. These may therefore represent 0101 and 0011 sequences at an 18.2MHz clock rate.

Data $\overline{D}$ was used to cancel the transmitted data D in the phantom hybrid, circuitry associated with IC_6. Capacitive trims at IC_5 inputs were used to optimise the rejection in the balanced hybrid circuitry associated with IC_5.

What the waveforms look like

Figure 9 shows data D, top trace, and data C, middle trace. The bottom trace, taken during a second exposure, shows the line waveform at point M in Fig. 8, or point K in Fig. 7.

The upper two traces are at 2V/div., the lower at 1V/div., all at 100ns/div. For clarity, data A and data B were disabled

for these measurements. Similarly, **Fig. 10** shows data B (top trace), and data A (middle trace). Although they both appear – and indeed are – locked, this is due to the use of 'normal-mode' sync facility.

In Normal mode, the oscilloscope displays channel 1 and channel 2 alternately, each trace triggered from the appropriate channel. At the bottom is shown the combined waveform at point K in Fig. 7, with data C and data D disabled. The bottom trace was recorded with the 'scope triggered from data A.

Since there is no relation between the frequency of data A and data B – unlike in Fig. 9 – the lower trace shows predominantly data A, spread out and blurred by data B.

Figure 11, top trace, shows the line waveform with all four data streams present simultaneously, triggered from data B. Naturally, with four different frequencies present, it looks rather a mess, with only the data B component discernable.

The lower trace shows the recovered data B at the output of IC_6 in Fig. 8. **Figure 12**, top trace, shows the line waveform with all four data streams present simultaneously, triggered from data A. The lower trace shows the recovered data A at the output of IC_5 in Fig. 8.

Snags and pitfalls...

The clarity, betokening a good signal to noise ratio, of the recovered data A in **Figure 12** shows that the hybrid for the balanced signal works extremely well.

Recovered data B in Fig. 11 presents not such a good signal to noise ratio, although a fast comparator would clearly extract the data adequately. But then the test circuit only included some 5m of cable.

The poorer efficacy of the hybrid used on the phantom circuit stems from two separate causes. The first is the delay experienced by data D in IC_4 – a delay not suffered by data $\overline{D}$ fed to hybrid IC_6 and its associated components.

Adding the 2-10pF trimmer effected a useful improvement, although of course a first order lag cannot exactly compensate for a pure time delay. An improvement would result from passing data $\overline{D}$ through another *EL2142*, to provide a balancing delay.

...and a possible reprieve

The other factor is the mismatch experienced by the common-mode phantom signal, it being terminated by the two 47Ω resistors in parallel, effectively 23.5Ω.

I said earlier that with bidirectional data, the modification to provide accurate termination of the phantom shown in Fig. 4 was no longer possible.

And so I thought – until now. But it occurred to me even while writing this article, that this is not so. In Fig. 8, IC_6 extracts the phantom signal, data B found at points M, N. Suppose now the recovered data B be applied, along with send-data D, to the V_{ref} input of IC_4.

The result would be to bootstrap the two 47Ω resistors with an equal voltage at points P and Q. Thus no component of current due to data B would flow in them; their value – as far as data B only is concerned – has been effectively increased to infinity.

If instead, only an appropriate fraction of the recovered data B be fed back, the terminating resistance seen looking in at M and N can be raised to the correct value for the cable.

But, you may say, in applying a fraction of the recovered data B back to the V_{ref} input of *IC_4*, surely it will be sent back down the line, the way it came? And it will indeed, but in an amount and phase which exactly cancels the reflection which would otherwise have taken place due to the mismatch.

Delays in $IC_{6,4}$ will prevent the correct degree of bootstrapping being instantly effective. This will set an upper limit on the usable data rate over the link, as a degree of edge shaping to control rise and fall times may be advisable.

Old hat?

To engineers involved with data distribution, the foregoing may be old hat; I honestly don't know. But for me, it has been an interesting and enlightening experiment. ■

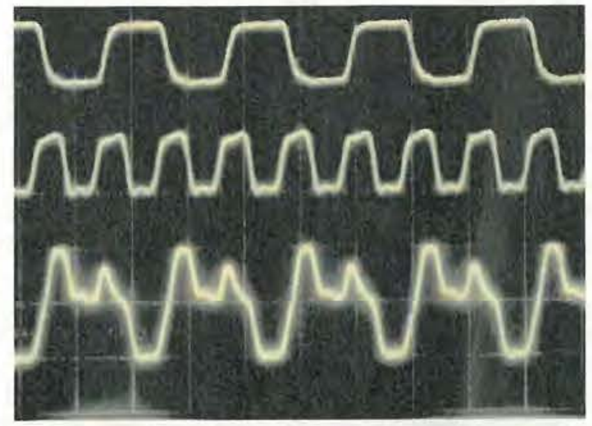


Fig. 9. Top is a), data D, 2V/div. Middle, b), is data C, 2V/div. Bottom, c), is line waveform at point M in Fig. 8, 1V/div., 0V at two divisions below centre. All traces are at 100ns/div.

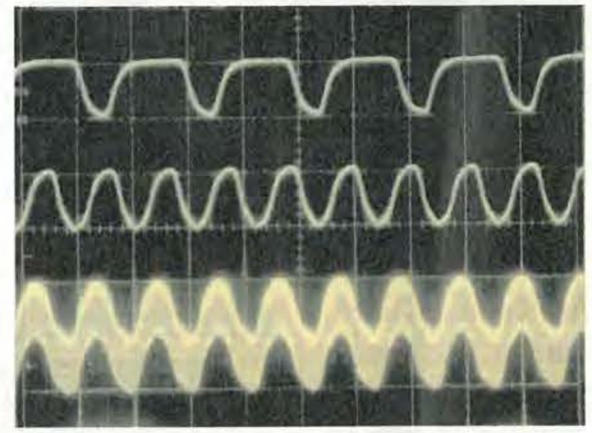


Fig. 10. Top, a) is data B, 2V/div. Middle, b) is data A, 2V/div. Bottom, c), is line waveform at point K in Fig. 7, 1V/div., 0V at two divisions below centre. All traces are at 100ns/div.

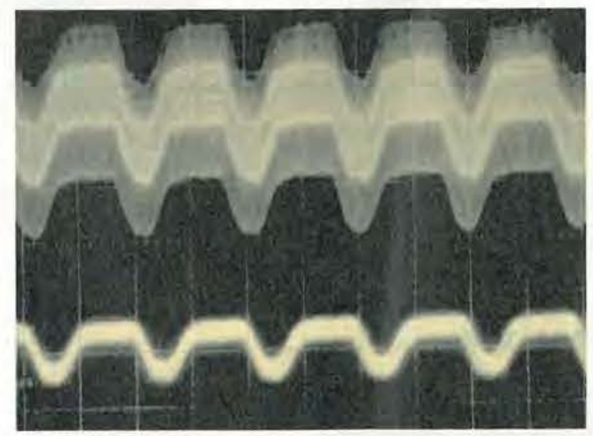


Fig. 11a). Top, a), is data A+B+C+D, 2V/div. Bottom is b), i.e. recovered data B at output of IC6, 1V/div., 0V at two divisions below centre. Both traces triggered from data B, at 100ns/div.

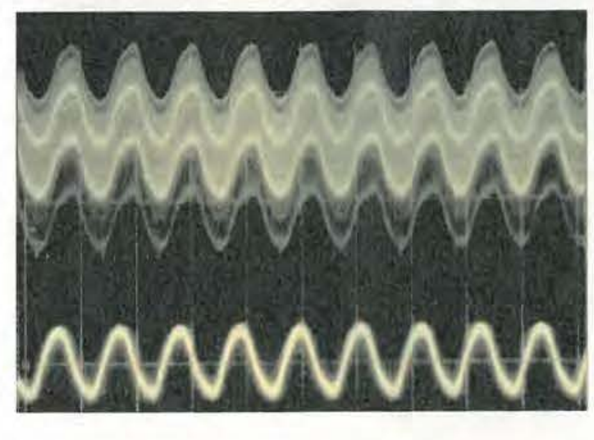


Fig. 12. Top, a), is data A+B+C+D, 2V/div. Bottom, b), recovered data A at output of IC_5, 1V/div., 0V at two divisions below centre. Both traces triggered from data A, at 100ns/div.

CIRCUIT IDEAS

Over £600 for a circuit idea?

New awards scheme for circuit ideas

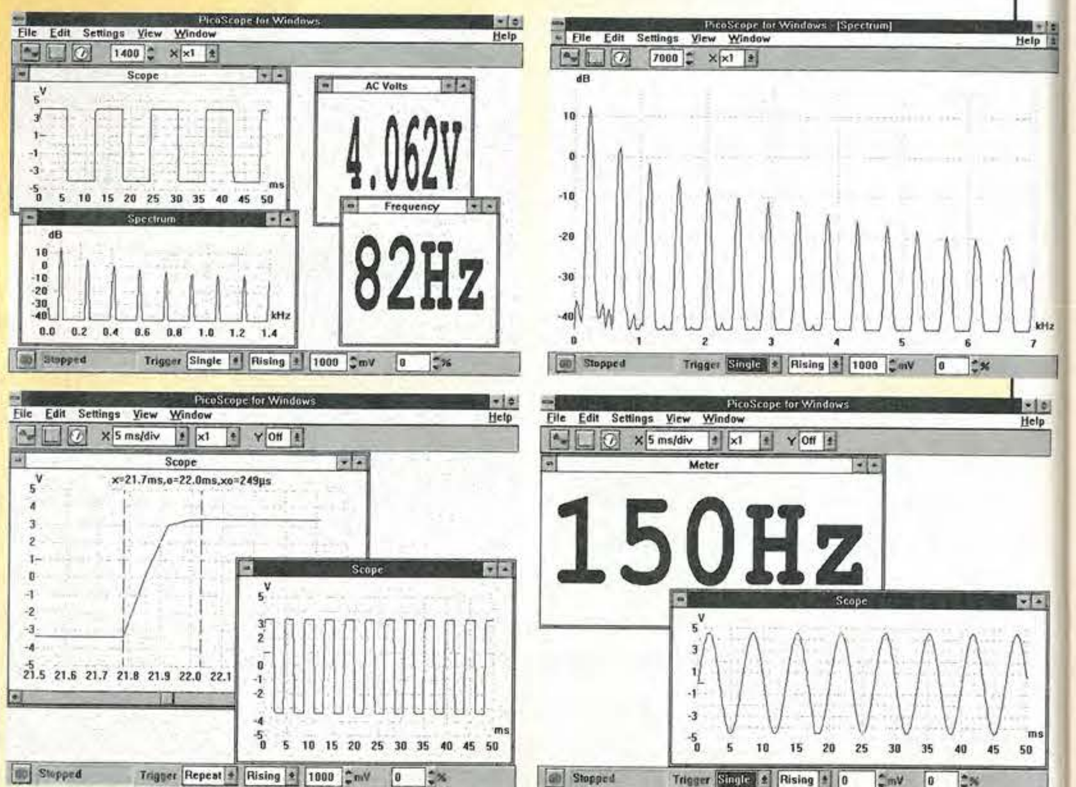
- Every circuit idea published in *Electronics World* receives £35.
- The pick of the month circuit idea receives a Pico Technology ADC42 – worth over £90 – in addition to £35.
- Once every six months, Pico Technology and *Electronics World* will select the best circuit idea published during the period and award the winner a Pico Technology ADC200-50 – worth £586.

How to submit your ideas

The best ideas are the ones that save readers time or money, or that solve a problem in a better or more elegant way than existing circuits. We will also consider the odd solution looking for a problem – if it has a degree of ingenuity.

Your submission will be judged on its originality. This means that the idea should certainly not have been published before. Useful modifications to existing circuits will be considered though – provided that they are original.

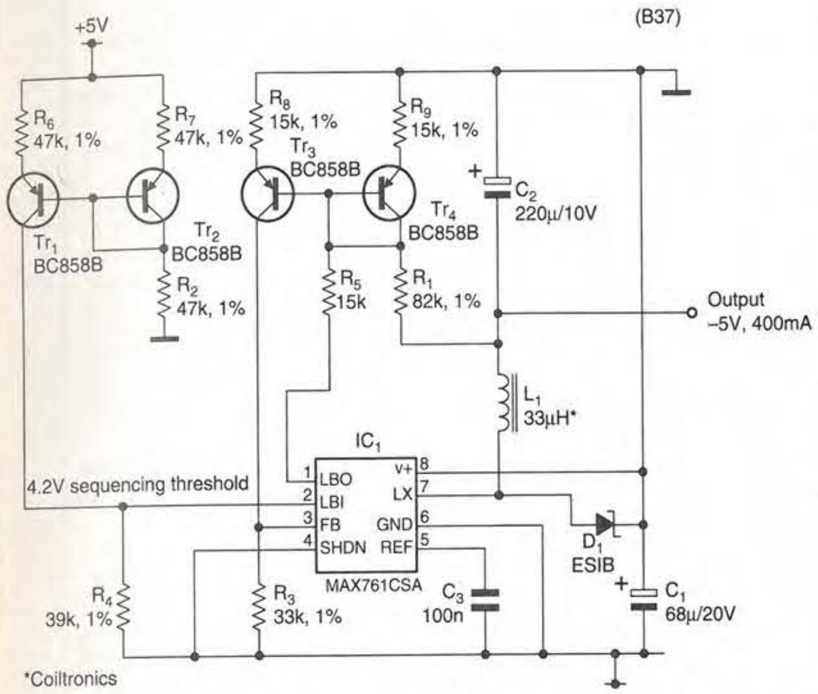
Don't forget to say why you think your idea is worthy. We can accept anything from clear hand writing and hand-drawn circuits on the back of an envelope. Type written text is better. But it helps us if the idea is on disk in a popular pc or Mac format. Include an ascii file and hard-copy drawing as a safety net and please label the disk with as much information as you can.



Turn your PC into a high-performance virtual instrument in return for a circuit idea.

The ADC200-50 is a dual-channel 50MHz digital storage oscilloscope, a 25MHz spectrum analyser and a multimeter. Interfacing to a pc via its parallel port, ADC200-50 also offers non-volatile storage and hard-copy facilities. Windows and DOS virtual instrument software is included.

ADC42 is a low-cost, high-resolution a-to-d converter sampling to 12 bits at 20ksample/s. This single-channel converter benefits from all the instrumentation features of the ADC200-50.



Maxim's MAX761CSA used as a negative buck regulator to provide –5V from a –12V supply, the –5V appearing in sequence with a separate +5V supply during switch-on and switch-off.

Sequenced step-down converter

This –12V to –5V converter only provides the –5V output when a separately regulated +5V has made its appearance, shutting down the –5V output if the +5V is not present. A-to-d and d-to-a converters often need this sequencing to avoid latch-up.

Regulator IC_1, a *MAX761CSA*, is an efficient, switching boost device used here as a negative buck regulator. The boost regulator arrangement is correct for the switching control. But the feedback, being referred to the positive rail and compared with a reference from the negative rail, needs a voltage level shift, which is provided by the current mirror $Tr_{3,4}$; emitter resistors $R_{8,9}$ reduce mismatch error.

An internal comparator and 1.5V reference in the *761*, which are intended for low-battery detection on the low-battery input and output pins, monitor the +5V rail. Current from the $Tr_{1,2}$ current mirror develops a voltage across R_4, proportional to the +5V rail, that is applied to LBI.

If this drops below a nominal 4.2V, LBO pulls R_5 to the negative rail, causing an increase in current through the diode-connected Tr_4; this is mirrored in Tr_3 and develops a voltage across R_3, applied to the feedback pin of the regulator. The action indicates that no further output is needed and the regulator shuts down, a minimum of 10kΩ load preventing D_1 leakage charging up C_2.

This buck-regulator arrangement delivers around 400mA at –5V, instead of the 150mA when used as intended as a boost converter, driven by +5V. Efficiency is 90% at 400mA, down to 85% at 100mA; ripple under 25mV at any load and accuracy dependent on the internal reference and tolerance of $R_{1,3,8,9}$.

Different V_{BE} in $Tr_{3,4}$ introduces more errors, but these can be greatly reduced and the need for $R_{6\text{-}9}$ eliminated, by substituting dual transistors such as the Rohm *UMT1N*.

Tim Herklots
Maxim Integrated Products
Reading
B37

Universal active filter

Switching a capacitor in the manner shown in **Fig. 1** simulates a resistance having the value $R_{eq}=1/f_cC_u$, f_c being the clock frequency. In this case, the simulated resistance is used to control the cut-off frequency and Q of a universal active filter.

Figure 2 shows the circuit, a low-pass filter of the second order with the possibility of interchanging the connections to pins 1 and 2 to make a band-pass filter, also of the second order.

In addition, with pin 2 grounded and pin 3 taken to pin 1 – shown by the dotted line – an all-pass filter is the outcome; adding C_2 turns the circuit into a band-stop filter. To get a high-pass filter, interchange C_1 and R_{eq}, place C_2 in parallel with R_{eq} to pin 4 and take the input to C_1.

For all versions, $f_0=f_cC_u/C_1$ and $Q=C_1/C_2$. Frequency range lies within the audio band, although the use of current-mode op-amps such as the *OPA 603* would extend the range into the megahertz region.

Kamil Kraus
Rokycany
Czech Republic

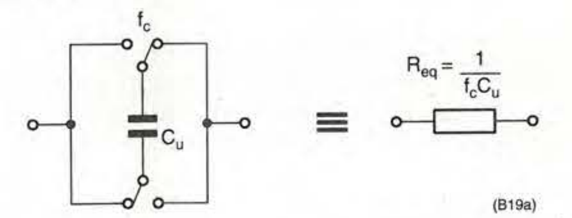


Fig. 1. Switched capacitor simulates a resistance, variable with switching frequency.

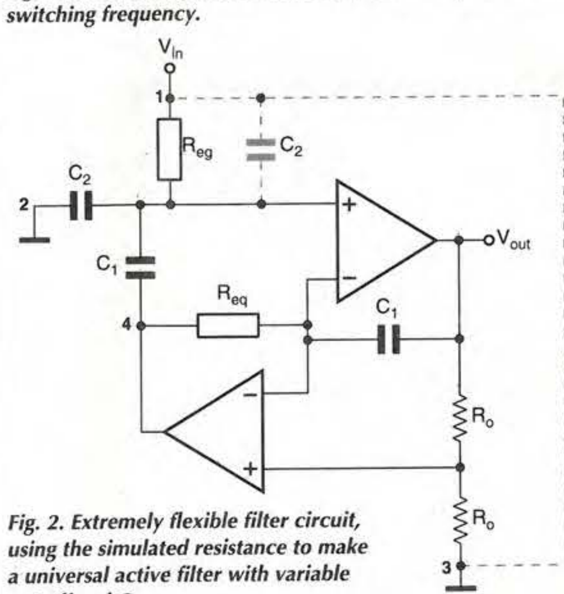


Fig. 2. Extremely flexible filter circuit, using the simulated resistance to make a universal active filter with variable cut-off and Q.

Underground radio or, "You thought you heard what?"

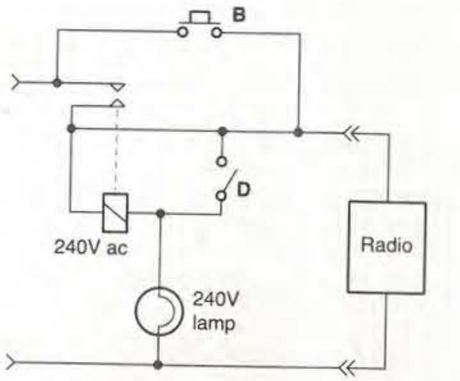
A medical friend wanted to listen to her mains-powered radio in her office between patient visits while coping with the paperwork, but didn't want it to be known – patients can be impatient. This circuit arrangement switches the radio off when the office door is opened, leaving an impression of industry and innocence.

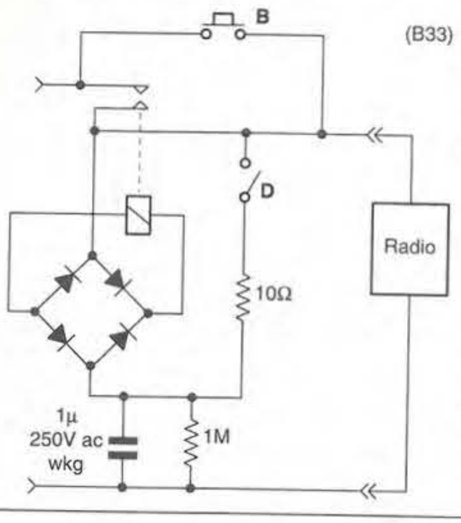
Door-mounted switch D has its contacts open when the door is closed, as in the type used for cupboard lights. As the door opens, the switch shorts the latching relay coil, opening the contacts and turning the radio off. When the coast is clear, the relay may be relatched and the Archers brought back by momentarily closing switch B, which can be anywhere convenient.

The 240V ac, 15-100W lamp acts as a current limiter to prevent damage when the coil is shorted, flashing as the door opens. A 6-48V dc relay may be used with a series 400V dc (i.e. 250V ac) 1μF capacitor with a 1MΩ bleed resistor.

Switch B will need the 10Ω series resistor to limit inrush current. Take care with the switch wiring; both are at mains potential.

Hugh T Wynne
Glasgow





(B33)

Clandestine radio switch switches off the radio as soon as the door opens, leaving a lot of very baffled people.

No-trim lf balanced mixer

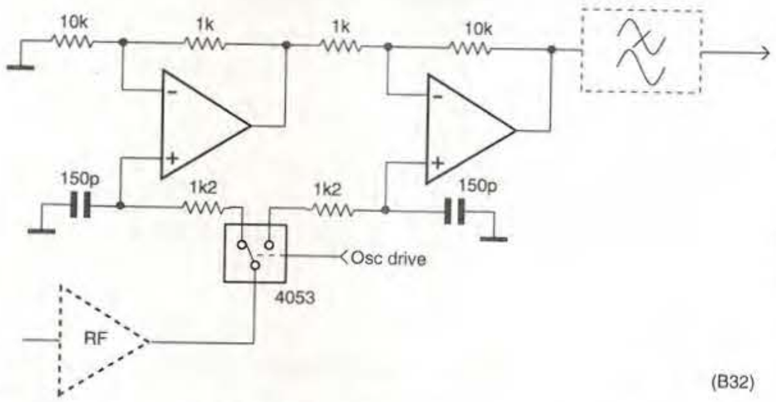
For a low-frequency ssb cave radio, I wanted to use a pair of balanced mixers that needed no balance control without resorting to multiplex ics or analogue gates, which need trimming to reduce the effect of unbalanced inputs. This circuit is probably familiar to instrument engineers, but I have not seen it used in a radio design.

The right-hand op-amp's non-inverting input gain is 11 and its inverting input sees a gain of 10; the other amplifier has a gain of 1.1, so that the overall gain is 11. With 1% resistors, balance is excellent.

Series 1.2kΩ resistors and capacitors perform the sample-and-hold at our 87kHz frequency. Oscillator drive to this circuit and its partner is at 12V digital level in phase-quadrature.

Output is very pure and the circuit is difficult to overload.

John R Hey
MIE Medical Research Ltd
Leeds



(B32)

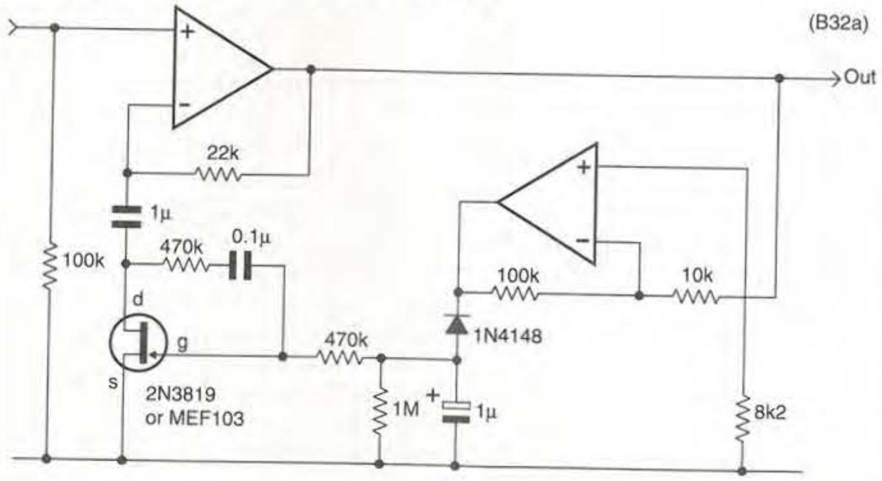
Alternative audio agc

Plessey's *6270* gain-controlled microphone preamp having been discontinued, I had to find a replacement for an audio agc system and have found other ics to be somewhat expensive. This circuit works well and is cheap.

Gain in the non-inverting op-amp is set by the 22kΩ feedback resistor and the return via the 1μF capacitor and fet, whose local feedback prevents waveform distortion. Overall feedback comes from the other op-amp with a gain of 10, its output being rectified and smoothed.

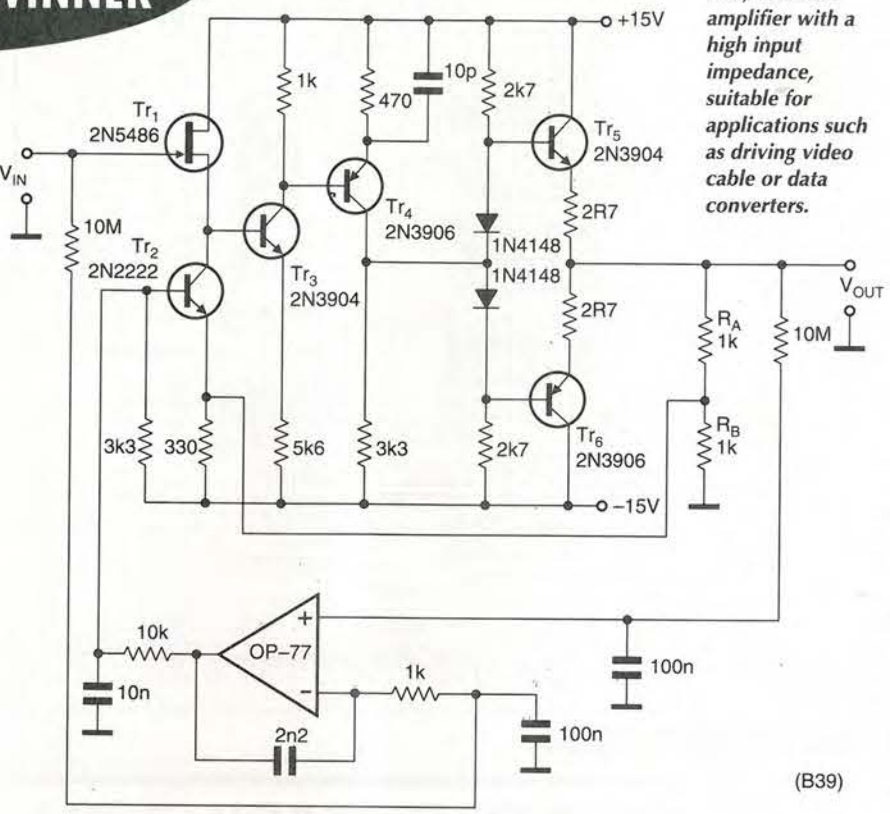
I have tried various fets, but have settled on the *3819* and *MEF103*, which work well: signal levels in the 4mV-4V range all output at about 200mV.

John R Hey
MIE Medical Research Ltd
Leeds



(B32a)

ADC42 WINNER



(B39)

Fast, dc-stable amplifier with a high input impedance, suitable for applications such as driving video cable or data converters.

Wide-band, variable-gain fet amplifier

Offering high input impedance and very good, unconditional dc stability, this fet amplifier has a –3dB bandwidth of 40-60MHz, depending on the gain setting.

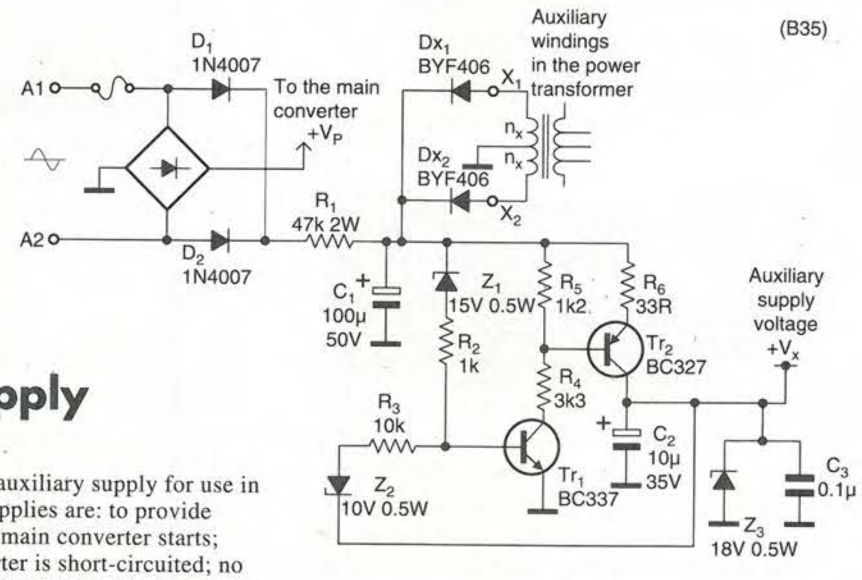
Design of the amplifier is simple, $Tr_{1,2}$ forming a high-speed input buffer, with the fet as an emitter-follower and Tr_2 as a current source to set the fet channel current. There follow simple gain and output stages with overall negative feedback, values shown giving a gain of unity.

Dc stability is the function of the *OP-77* op-amp, which compares the filtered output signal with the filtered input, the difference being used to set the bias of Tr_2 and therefore the fet channel current. Gate-source voltage of the fet must now become whatever value is needed to match input and output potentials.

The *CR* network at the *OP-77* output eliminates high-speed transients from the input signal via Tr_2 C-B junction.

Voltage gain is R_A/R_B, 1 in this case. Slewing is faster than 1000V/µs and with a gain of unity, –3dB bandwidth is 60MHz; at a gain of 10, 40MHz.

Frantisek Michele
Brno
Czech Republic



(B35)

Housekeeping supply for a switched-mode power supply provides undervoltage protection during turn-off.

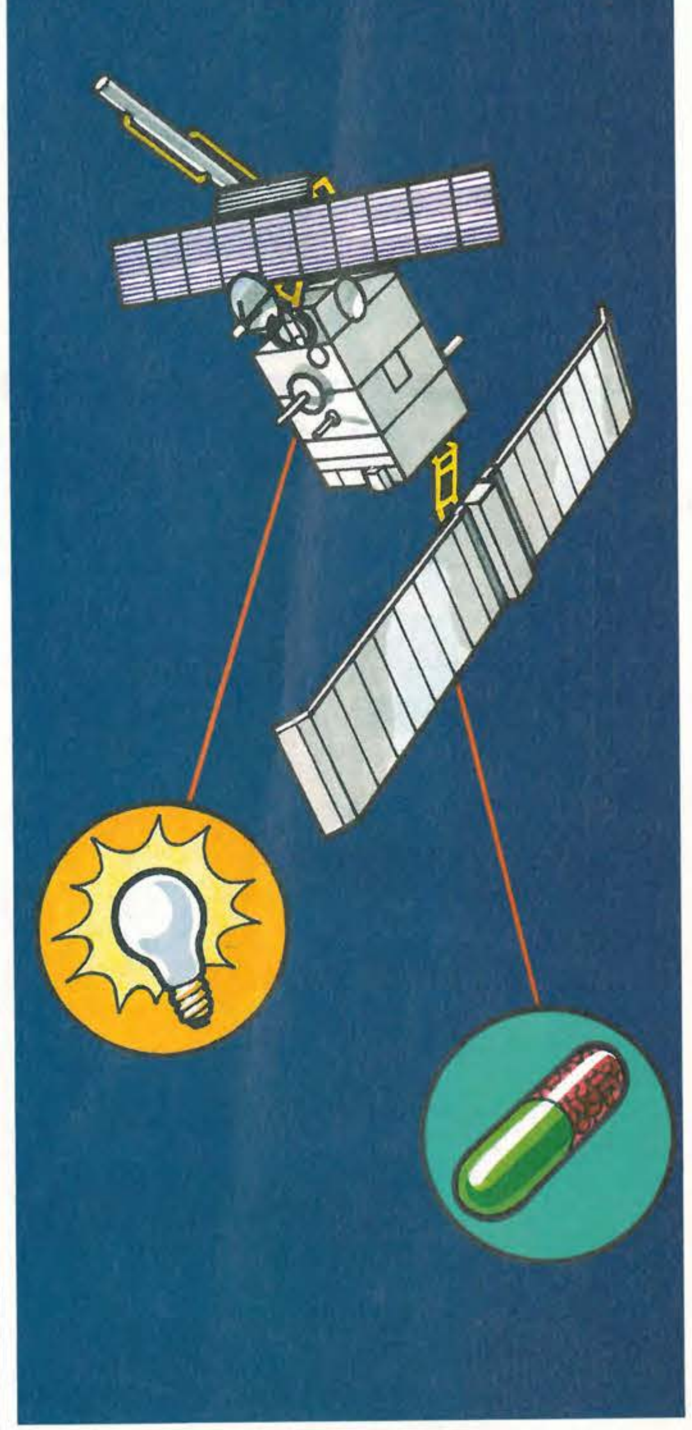
Auxiliary supply for smps

Requirements met by this auxiliary supply for use in switched-mode power supplies are: to provide auxiliary voltage before the main converter starts; operation if the main converter is short-circuited; no overvoltage; low power dissipation; and undervoltage shut-down if the frequency becomes less than an acceptable value during shutdown.

On switch-on, diodes $D_{1,2}$ rectify the mains input to charge C_1 through R_1, the main circuit starting once C_1 has enough charge to feed the control circuit.

As Z_1 turns on, Tr_1 begins to conduct, feedback around Tr_2 turning both transistors hard on and Tr_2 applying the voltage on C_1 to the output V_x. As the main converter starts, the auxiliary transformer windings supply power to the circuit. If the voltage on C_1 falls below the threshold set by Z_1, Tr_1 remains in conduction, since its base current is supplied by Tr_2 through Z_2 and R_3. However, if the C_1 voltage is less than that on Z_2, Tr_1 turns off, also turning off Tr_2 and the rest of the circuit.

H E Tacca
University of Buenos Aires
Argentina



ADC42 WINNER

Simple, linear thermoregulator

This very simple arrangement keeps small objects to within ±0.1°C in ambient-temperature variations of around ±10°C. In my case, it stabilises the temperature of pressure-meter measuring head.

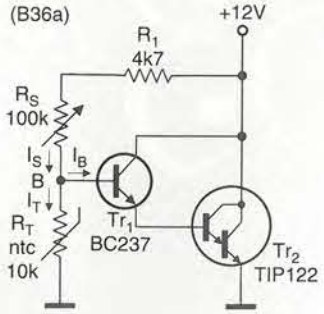


Fig. 1. A simple circuit to maintain a small object at a closely controlled temperature.

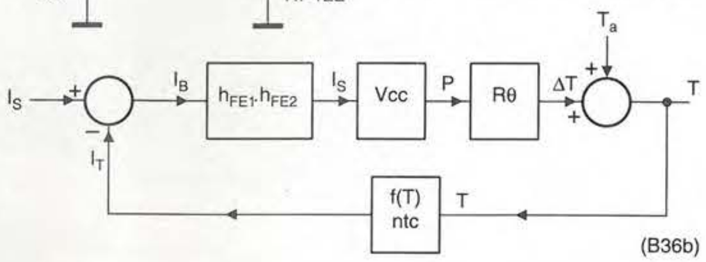


Fig. 2. Principle of the thermoregulator, in which T is the object's temperature and T_A the ambient temperature, T being fed back as control.

Sensing is done by the ntc thermistor R_T, which has a resistance of 10kΩ at 25°C. Transistor Tr_2, a *TIP122* darlington, is the heating element and is fastened to the object to maintain it at the temperature set by the bias resistors R_s and R_1. For the gain needed to achieve the regulation quoted, the transistor Tr_1 is needed; for less demanding application, it may be omitted. **Figure 2** is the block diagram.

Base current is the difference between I_S and I_T; voltage at B is approximately fixed at 1.8V or $3\times V_{BE}$, so that I_S depends solely on the value of R_S and I_T on that of R_T, which is controlled by the temperature. Power applied is $P=V_{CC}R_\theta$, R_θ being the thermal resistance between the system and its environment. An exponential response from the thermistor gives the transfer function,

$$I_T = f(T) = V_B / \{R_0 \exp[\beta(1/T + 1/T_0)]\},$$

in which V_B is the voltage at B.

As the gain is high, base current may be neglected and output temperature is approximately that determined by the inverse of f(*T*), so that setting the temperature means simply setting $I_S=I_T$ at the temperature needed.

If the thermal characteristics of the object cause instability, reduce V_{CC} and, to reduce the possibility of damage to the darlington during transients, ensure that the power supply is current-limited or has a series resistor.

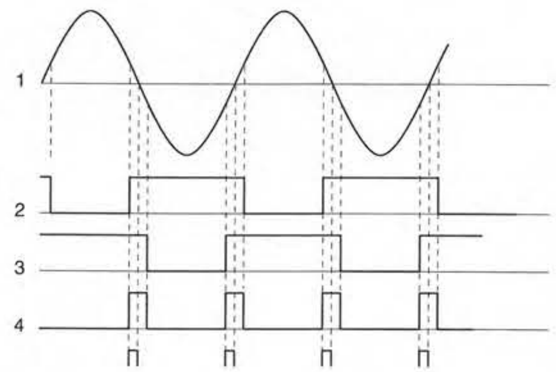
Giorgio Delfitto
University of Padova Italy

Accurate zero-crossing detector

At the output of this circuit appears a positive-going pulse, the trailing edge of which is within 8μs of the time of zero-crossing when driven by a 50Hz waveform of 190-250V ac amplitude.

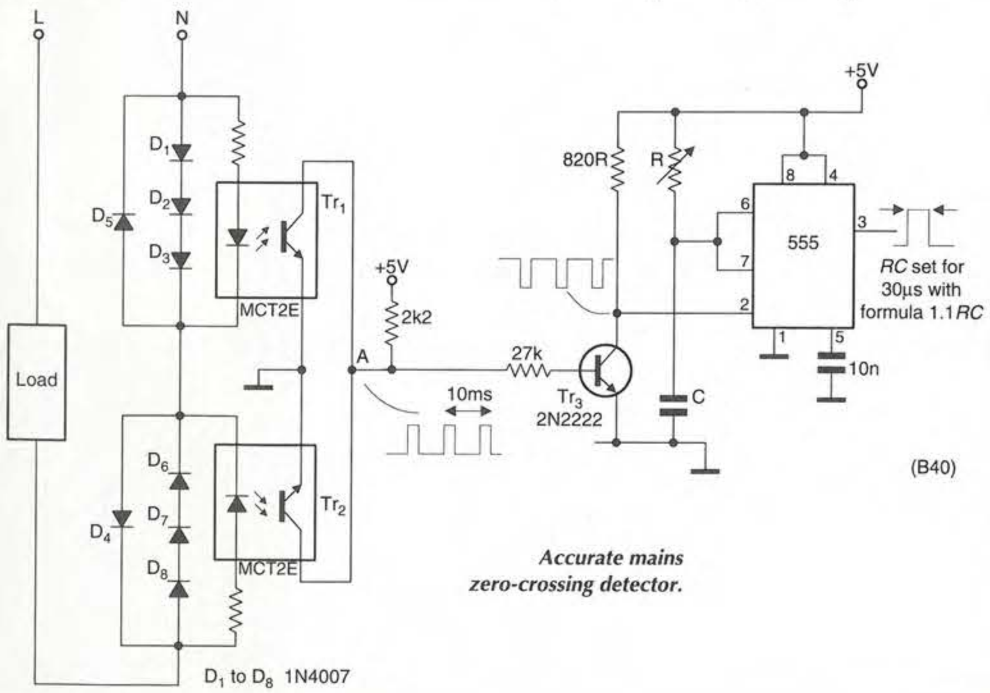
In **Fig. 1**, diodes $D_{1\text{-}3}$ conduct during most of the negative half-cycles of the input and $D_{6\text{-}8}$ during the positive half-cycles; the two sets of three diodes need about 3V across them for conduction. Diodes $D_{4,5}$ provide a path for the conducting diodes.

Figure 2 shows the waveforms, with the input at the top. Waveforms 2 and 3 would occur at point A on alternate half-cycles if each transistor were in circuit alone; at 3 is the 100Hz result of both being present.



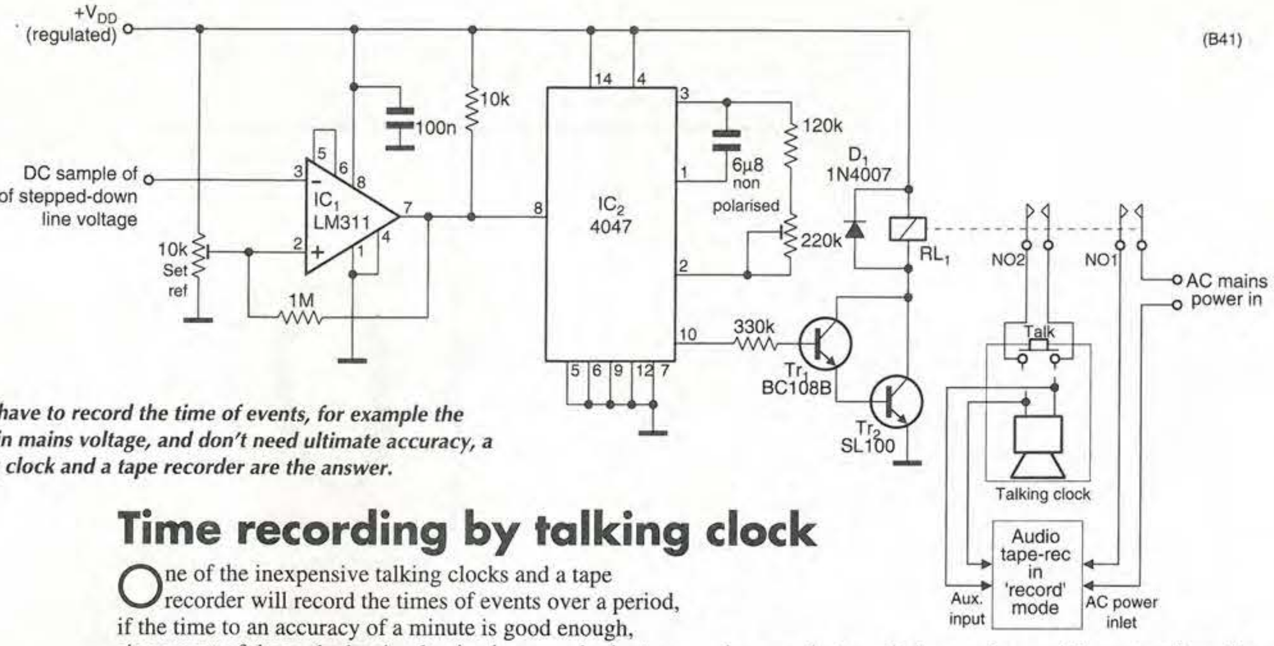
Clearly, zero crossing is more or less in the middle of the pulse at 3, so that after inversion in Tr_3 the pulse triggers the *555* monostable flip-flop, the time constant being set to give the falling edge of its output – waveform 4 – at the correct time. If the width of the 555 output pulse is set to 30μs, accuracy is within 8μs.

Jayant Kathe
Bombay
India
B40



Accurate mains zero-crossing detector.

Warning
Using an opto-isolator alone does not constitute mains safety isolation. Be conversant with the appropriate safety regulations before attempting to apply this circuit.



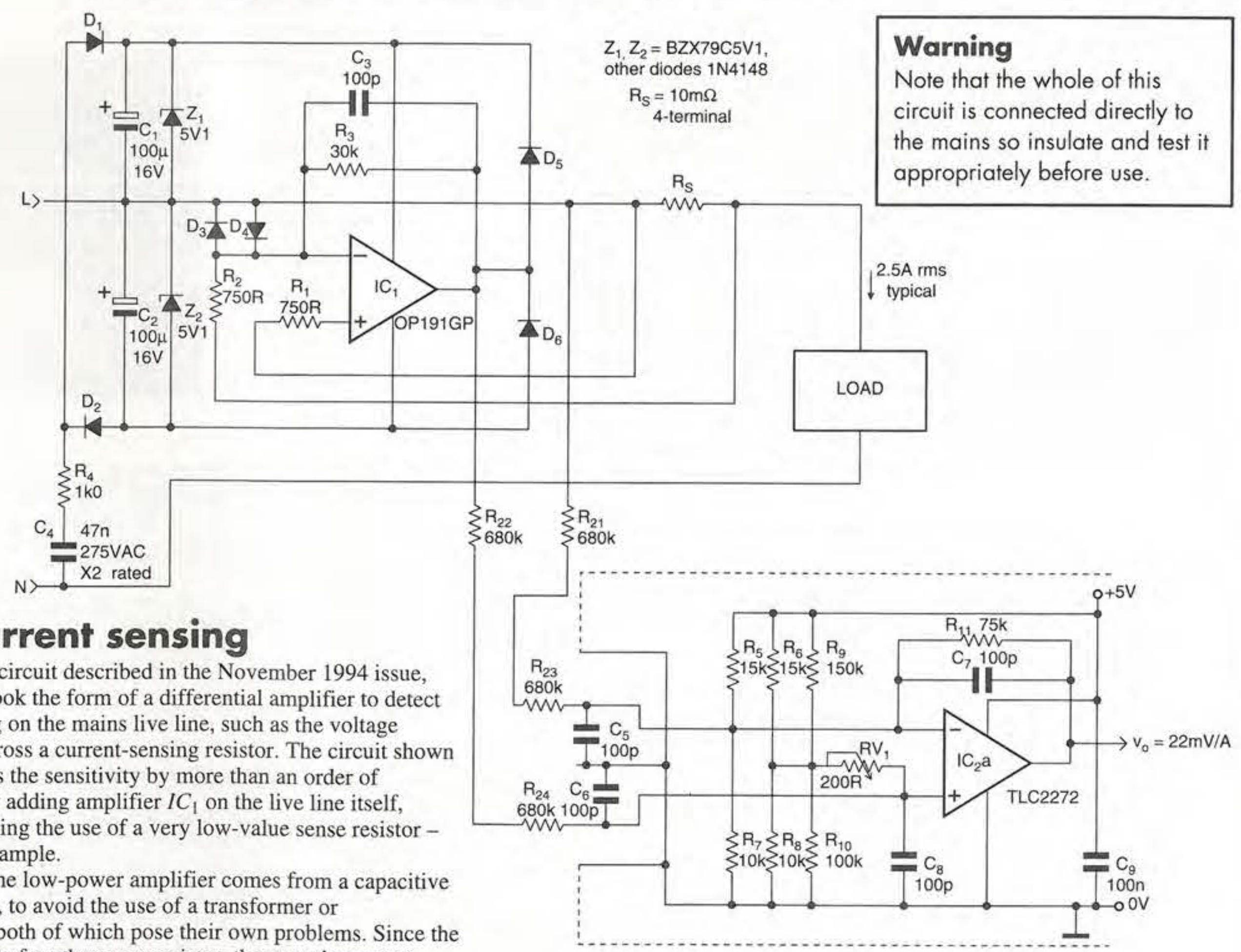
If you have to record the time of events, for example the drops in mains voltage, and don't need ultimate accuracy, a talking clock and a tape recorder are the answer.

Time recording by talking clock

One of the inexpensive talking clocks and a tape recorder will record the times of events over a period, if the time to an accuracy of a minute is good enough, since most of these clocks simply give hours and minutes. In this case, the circuit detects and records power-line drops.

A comparator looks at a rectified and smoothed sample of the line input and triggers the *4047* monostable when such a drop occurs. The time of the monostable is such that its output stays high for around 6s, long enough for the recorder to switch on and record the output from the clock, the recorder being powered, and the battery-powered clock being actuated, by the relay.

Sanjay Chendvankar
Tata Institute of Fundamental Research
Mumbai
India



Warning
Note that the whole of this circuit is connected directly to the mains so insulate and test it appropriately before use.

Live current sensing

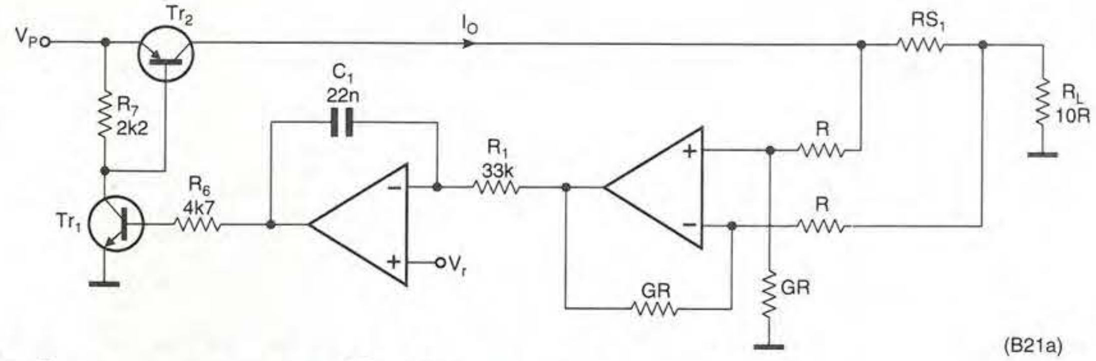
An earlier circuit described in the November 1994 issue, p. 921, took the form of a differential amplifier to detect signals sitting on the mains live line, such as the voltage developed across a current-sensing resistor. The circuit shown here increases the sensitivity by more than an order of magnitude by adding amplifier IC_1 on the live line itself, thereby allowing the use of a very low-value sense resistor – 10mΩ, for example.

Power for the low-power amplifier comes from a capacitive current pump, to avoid the use of a transformer or optocoupler, both of which pose their own problems. Since the pump comes before the sense resistor, the pump's current waveform does not add to the legitimate one being sensed.

This arrangement was used to measure the current drawn by a triac-controlled load. A further benefit is that the differential amplifier IC_2 may be grounded, as opposed to being at mains neutral, assuming that $R_{21\text{-}24}$ are of good quality. Take note that these resistors are split across the safety barrier.

CJD Catto
Cambridge

Fig. 1. Voltage-controlled current source for general-purpose use.



(B21a)

Voltage-controlled current source

Although designed to produce constant brightness from a led by maintaining a constant current through it, this is equally suitable as a general-purpose current source.

In **Fig. 1**, the action of the circuit is to equalise the voltages at the inputs of the integrator. The output of the integrator changes the bias of Q_1, changing the output current I_0 and consequently the voltage across R_s and the inputs to the op-amp, the output of which will equal the control voltage to the integrator. G being the amplifier gain, $G \times I_0 \times R_s = V_r$, so that $I_0 = V_r / G \times R_s$, output current therefore depending only on fixed quantities.

To avoid Tr_2 going into saturation and the linearity of the control being affected,

$$I_{max} \leq \frac{V_p}{R_L + R_s}$$

so that,

$$V_{r(max)} \leq \left(\frac{GR_s}{R_L + R_s} \right)$$

The relationship between the supply voltage V_p and the control voltage V_r to avoid saturation can therefore be expressed as,

$$V_{p(min)} \leq \frac{V_{r(max)}}{G} \left(1 + \frac{R_L}{R_s} \right)$$

Figure 2 shows the minimum supply voltage as a function of the required current, with $R_L = 10k\Omega$ and $R_s = 1\Omega$.

E Ahmad
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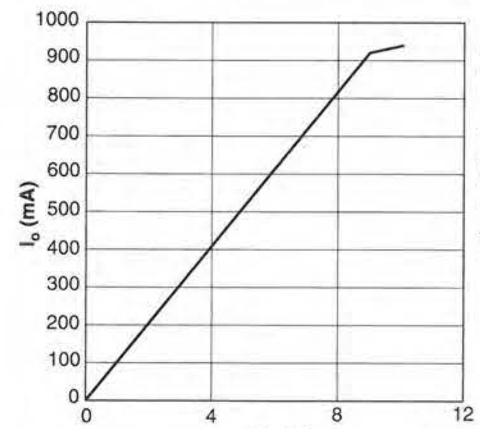
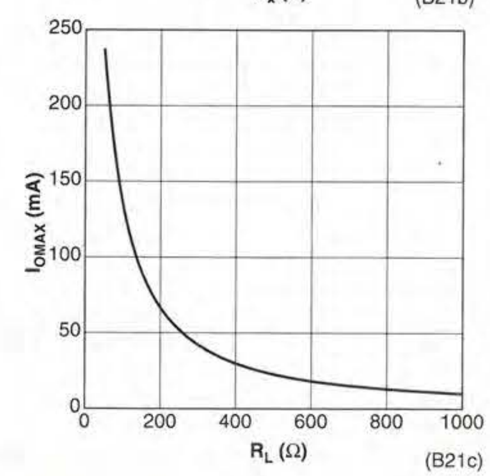


(B21b)

Fig. 2. Current variation is almost perfectly linear with supply voltage.



(B21c)

LC 'Wien-bridge' oscillator

Apropos of a comment by Linfoot in the December 1997 letters column, it may be that Wien oscillators are old-fashioned and that they may be incapable of further improvement, but replacing the *RC* network by an *LC* filter produces a sine generator with lower distortion.

It is unnecessary to use physical inductors, even at low frequencies; a gyrator is a more practical proposition. To avoid clipping at the supply rail, a diode limiter stabilises the output amplitude and the high Q of the band-pass filter removes the consequent distortion.

This generator produces a 1kHz sinewave at an amplitude of 1V rms. Frequency adjustment is by VR_1.

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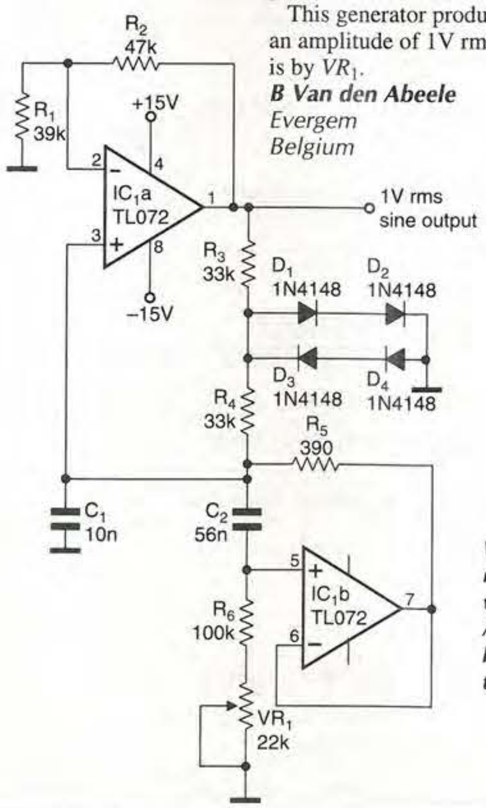
Belgium



Wien-bridge oscillator rises again, this time without its RC network. An inductor, simulated by a gyrator, improves the waveform.

EasyPC & Multirouter

Maker; Number One Systems, Ref WW, Harding Way, St Ives, Cambridgeshire PE17 4WR.
Tel; 01480 461778 fax 01480 494042.
Price; *EasyPC* £595, 2 layer *Multirouter* £295.
http://www.numberone.com,
e-mail sales@numberone.com

Rod Cooper analyses a well established Dos pcb CAD package that has recently been upgraded for Windows platforms – *Easy-PC.*

The route to pcb cad

This review investigates a new Windows version of the *Easy-PC* package, reviewed in its Dos version in *Electronics World* July 97. It has a recommended minimum hardware/software requirement of a Pentium 100 with 16Mbyte ram, and needs 20Mbyte free hard-disk space to install, plus Windows 95 or NT.

Although 32 bit, this software is not intended for use with WIN32s and Windows 3.x. The basic schematic drawing/pcb layout program comes on four floppy disks and installation is straightforward. The *MultiRouter* autorouter is on two more floppy disks. Security is by the name and number method.

Easy-PC's manual is well written and is better arranged than the Dos version. The more detailed information on the design process is kept for later in the book and, as a result, the manual is more readable. You are first given an overview, and then a more comprehensive explanation of the system.

A short chapter entitled 'Getting Started' contains most of the essential operating instructions and is laid out logically, with schematic drawing first, progressing to rat's nest and then pcb design. Operation of the autorouter is in a separate manual.

An appendix lists all the library symbols and footprints both in text and graphics, with associated function: few manuals give such comprehensive treatment for all this useful information.

MultiRouter's manual is one of the most readable instruction books on autorouter operation. The section on autorouter hints and tips is excellent and it is the only manual in this review with a dedicated chapter on single-sided routeing. Together, these two sections will be of considerable help to those new to autorouters.

Schematic capture

Number One Systems has managed to produce a good balance between icons and menus. As **Fig. 1** shows, there is just a single row of a dozen icons in the schematic drawing section. A 'tool-tips' method is used to identify them.

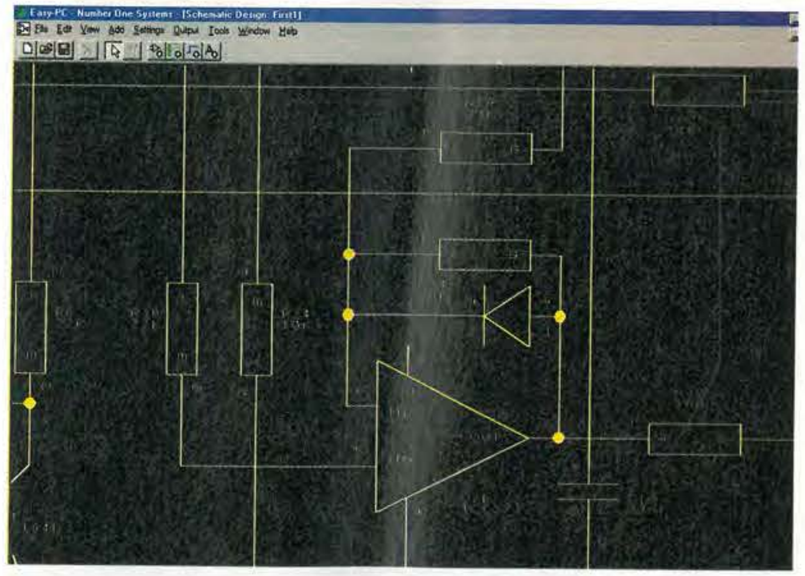


Fig. 1. Close-up view of a schematic drawing, showing the new Windows controls. Note the balance between icons and menus and how similar the symbol/drawing style is with previous versions.

Although the controls are clearly in Windows format, those familiar with the Dos version will recognise the schematic symbols and style. A glance at Fig. 1 shows these are the same as, or at least similar to, the Dos symbols. With respect to both icons and symbols, it is interesting to note that this is the same route taken by Seetrax in their approach making *Ranger2* for Windows.

Panning is done by scroll bars, but panning, zooming and un-zooming can be done with the keys P, Z, and U respectively. This is the keyboard system as used in the Dos version, and is actually quicker and more convenient than selecting these functions with the mouse. The available drawing area is good at 9in by 5.5in on a 14in monitor.

Selecting symbols is done by opening one of several libraries and picking a component in text. You don't get a

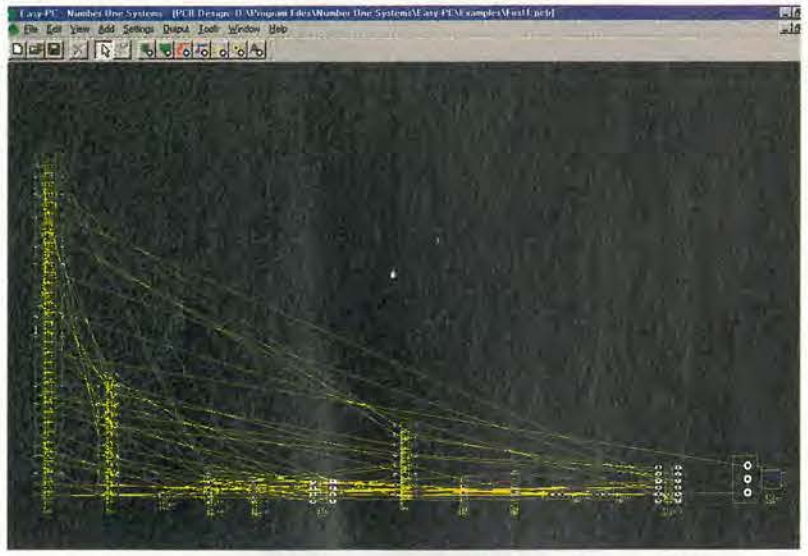


Fig. 2. Typical two-axis linear rat's nest dump from schematic capture, which has to be manually arranged.

graphical representation until the symbol is on the screen. If you want such details, you can either edit the library or refer to the manual. If you choose to edit a library component, you get presented with both the schematic symbol and its pcb footprint simultaneously, which is a good idea as you can compare symbol pins with the pcb pins.

Initially, the symbol trails the mouse to its selected position, and is placed with one click. You can place copies of the symbol with a single click at this stage. At later stages you can duplicate symbols by left-clicking on them, then right-clicking.

Any subsequent moving is done by the drag and drop method, modeless and therefore quick. Moving multiple symbols – i.e. block move – is done by pressing control and shift together on the keyboard during selection and then dragging and dropping. Connections stay intact and orthogonal while moving.

Handling parts

There is no parts bin, so to continue placing other symbols you have to return to the library. This is rather slow compared to the parts-bin method if a large number of components are involved.

Symbol annotation is done automatically as you go along. A right click on a symbol or a track brings a pop-up menu to enable editing.

Symbol text rotates if you rotate the symbol, which is done with the keyboard 'R' or from the right-click menu. The

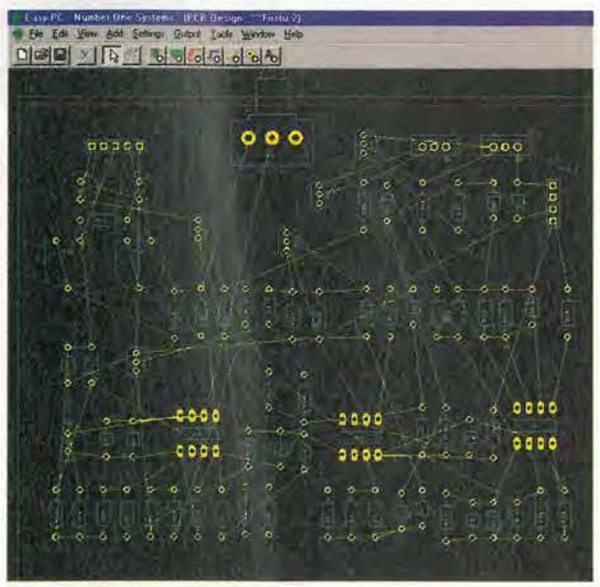


Fig. 3. Rat's nest from above screen shot after being set up manually for single-sided routeing.

rotated text can be un-rotated similarly, and is generally manoeuvrable if you wish to tidy the diagram up.

Wiring symbols up can be done by selecting the 'add, connection' menu, or by selecting the equivalent button, in which case you can start a connection line with a single click. You can also start a line by double-clicking on a symbol terminal. This enables you to draw the line with the mouse to another terminal elsewhere, double-clicking to finish.

An audible tone confirms that you have made a connection. If you want to continue the line on to another symbol terminal, a single click instead of a double will enable you to extend the line. Any corners on the way are done by single-clicking.

Click-click

Making a connection relies on getting the double-click to finish right. If you miss-fire then you have to revert to a menu, with a single right click, and terminate the line with another click in the menu.

This is a slightly more complex system compared to other programs such as *Proteus,* which uses a single click both to start a connection and finish, and has no menu entry. It assumes – this being the most common operation in CAD – that you wish to made a connection. *CircuitMaker* also uses a single click to start and finish, once you are in connection mode with a single click.

I found the *Easy-PC* method acceptable once I got used to it, but I think it will not have much appeal those who are not strong on double-clicking. How are you on double clicks? I advise those of you interested in *Easy-PC* to check this system to see how you get along with it – especially if you use a graphics tablet instead of a mouse.

There is no alternative system, such as the auto-wirer of the type found in *CircuitMaker, EDWin* and *Proteus.*

The drawing system is orthogonal with snap-to. Miss-drawn lines are not inhibited, and are not removed by refreshing the screen.

Adjustable auto-save has now been added. There is no map showing where you are on the drawing sheet, but you can retrieve lost drawings with the 'zoom-all' function.

There is support for multi-sheet schematics, which can be stored in a 'Project File' along with the pcb design. This is a system similar to the Project, Job or Database themes already discussed in other programs.

Laying out circuit boards

There are three options for making a layout. First, there is a plain manual system for starting layout from scratch, i.e. not using schematic capture. Secondly, it is possible to route a rat's nest produced from schematic capture by the interactive method. Finally there is *MultiRouter* – the Windows version of Number One's rip-up-and-retry autorouter. These options are dealt with in turn.

The manual pcb routeing system is straightforward and much like the schematic drawing section as regards component placing and putting traces in place. It is easier to use than the Dos version.

For example, compared to the dos version, interactive editing is quicker as you can swap from track editing to component moving with a mouse click i.e. no menus/buttons. When moving components, tracks stay attached and orthogonal.

As an alternative to manually composing the artwork, a pcb layout can be routed interactively from the rat's nest by the rubber-banding method. Generation of a rat's nest from the schematic is very simple – just one click in the tools menu and the components are dumped as shown in **Fig. 2.**

This rat's nest is based on a linear system much like its Dos predecessor. There is no assistance for sorting out the

components such as force vectors or autoplacement as featured in several of the other programs reviewed here. At present, users have to use their own skill at sorting, so it is a slow system needing a relatively high input of effort.

One indirect way to check if you are building the rat's nest on the right lines is to run the autorouter in 'preview' mode. It will make a single, relatively rapid pass to route the rat's nest, and the results will indicate where there are difficulties in routeing.

Autorouteing

MultiRouter was reviewed in its Dos form in the last set of reviews and like that autorouter, this Windows program is a capable rip-up-and-retry and push-and-shove shape-based autorouter without pin limits. For comments on shape-based autorouters, see the first set of reviews.

Setting up and operating of *MultiRouter* is simple. Such things as routeing layers, track widths and clearances are set up from the layout section, and the strategies set up in the autorouter menu. One point of interest here is the 'smoothing' strategy which removes any jagged edges and improves track spacing.

The autorouter is slightly unusual in that, when it has been started, the operator does not see the tracks being formed and reformed as you would in, say, *Ares IV* in *Proteus, TraxMaker* or *Ranger2.* Instead, a table shows the progress of the autorouter.

When autorouteing has finished, the table is completed and the autorouter results are then transferred back to the pcb section as a layout. Only then do you see the routed tracks.

Has this any advantage? If you see the tracks being formed, you can get some idea about which parts of the rat's nest the autorouter is finding hard to route. However, this is only useful if the run is reasonably short, because observing an autorouter at work is about as interesting as watching clothes going round in a washing machine.

In my experience, observation is only practicable for about 15 minutes. For longer runs, a tabular system may well be better. Personal choice will play a large role here.

The design rule check is run after routeing and is presented as a text report, and marks errors on the design.

The autorouter can autoneck – or track-fatten – which is a great help in finding routes. It has no gate/pin swap feature. This will hold it back, but only when swappable gates/pins are in the design.

Like its Dos counterpart, it could easily complete the test circuit, which puts it firmly in category A. To give it a more realistic trial, **Fig. 4** shows a typical result on a more complex board. Overall, this autorouter performed well.

Output

The usual Gerber and NC drill outputs are available, and artwork output can be made via Windows' printer drivers or from *Easy-PC's* own pen-plotter driver for HPGL. The set-up for both printers and plotters provides plenty of control, including the ability to mirror the output.

Some thought seems to have gone into control of the plot positioning, which is a difficult area with some programs when large boards are attempted. It was nice to see that pen-plotting has its own short chapter in the manual.

Unfortunately I was unable to verify plotter results as the driver was not compatible with my particular HPGL plotter.

In summary

This Windows version of *Easy-PC* for Windows is sure to attract attention, especially from those who have the Dos version and wish to up-grade. However, compared to other programs, the current schematic drawing and rat's nest sorting stages are labour-intensive. For example, it is one of the few programs still without a parts-bin option, and un-

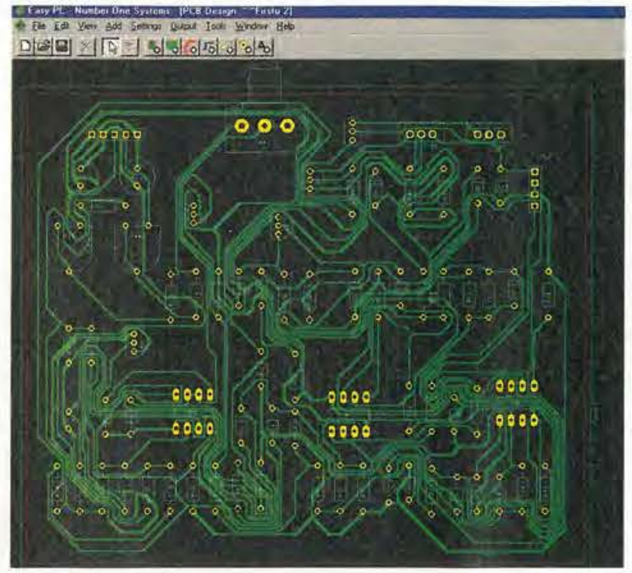


Fig. 4. Single-sided routeing of the rat's nest of Fig. 3 with Multirouter took just 15 minutes on a 133MHz Pentium with 32Mbyte of ram. Note that the amount of track mitreing is controlled from the configuration menu and this pattern is my own personal choice.

rotating symbol text is time-consuming.

Some computer assistance to sort the rat's nest – particularly one based on a linear dump – is definitely needed. I think most designers would expect to see vector forces or auto-placement, or preferably both, in a program at this price level, bearing in mind that even *EDWin* at £114 and *TraxMaker* at £200 both have autoplacement.

Several features like automatic back-annotation and gate-and-pin-swap that one takes for granted in other programs like *Proteus* and *Ranger2* are absent. However, with Number One Systems' policy of continuing improvement, it is likely these features, and others, will be added in due course.

MultiRouter is a good autorouter, easy to operate and giving reliable results. The presence of a dedicated pen-plotter driver for artwork output is a definite advantage over those programs that rely on Windows drivers.

Easy-PC with *Multirouter* is a relatively expensive package when compared to the other programs reviewed here. In fact it is slightly over the stated budget limit. Bear in mind, though, that there is no pin limit on the system. Also, as pointed out when previously reviewing the dos system, you have to look at the whole package complete with simulators to assess its worth. ■

Previous review subjects

PCB Designer: Niche Software Ltd, tel 01432 355414 – reviewed September 1996.
PIA:AW Software Ltd, Germany tel +49 89 6915352 – reviewed September 1996.
Easytrax: Protel International pty, Australia. Available from PDSL, tel 01892 663298 – reviewed September 1996.
Ranger 2: Seetrax CAE Ltd, tel. 01705 591037 – reviewed October 1996.
Electronics Workbench: Interactive Image Technologies Ltd Canada, tel. 00141 69 775 550 – reviewed October 1996.
CircuitMaker: MicroCode Engineering USA, UK agent Labvolt, tel 01480 300695 – reviewed November 1996.
Quickroute 3.5 Pro+: Quickroute Systems Ltd, tel 0161 449 7101 – reviewed December 1996.
Propak: Labcenter Electronics, tel 01756 753440 – reviewed December 1996.
Proteus: Labcenter Electronics, Schematic capture and pcb design – reviewed January 1997.
EasyPc Pro XM: Number One Systems, tel 01480 461778 – reviewed January 1997.
Challenger: Ultimate Technology, Tel 01594 810100 – reviewed June 1998.
Ranger 2: Seetrax CAE Ltd, Tel 01730 260062 – reviewed June 1998.
EDWin: Visionics, UK supplier Swift Eurotech, Tel. 01992 570006, fax 570220 – reviewed July 1998.
Traxmaker & Circuitmaker: Microcode, UK supplier Labvolt Tel. 01480 300695 – reviewed July 1998.

Grounding on a different plane

Like any conductor carrying current, a ground plane has voltages across it and these voltages can cause emc problems. Ian Darney explains how to analyse and solve such problems.

The 'equipotential ground plane' is a concept often used by system designers. As an aid to the practical problems of controlling interference, however, it owes more to mythology than science; its usefulness is about the same as a talisman brandished to ward off evil spirits.

The purpose of this article is to prove the validity of the last statement, and, in so doing, to introduce a method of analysing interference in electronic systems – a method that cannot be found in any book.[1]

Essentially, this method is a procedure for deriving the capacitive and inductive parameters of wiring assemblies, and creating circuit models.

The formulation is introduced in terms of the coupling between two wires over a ground plane, but can be developed to cater for more complex configurations. Even so, it is not complicated.

Anyone whose eyes have glazed over at the mention of div, curl, del, Maxwell equations, or boundary conditions, can relax. Most of the mathematical operations involved in the formulation are simple addition and subtraction.

Method of analysis

Traditionally, the effect of the ground plane is simulated by image conductors, and this treatment is no exception. For two wires over a plane, the number of conductors to consider must be four; two real and two image conductors.

A set of four 'primitive' equations is defined, relating voltages on the wires to the currents they carry. When this set of conductors is configured to carry signals, two loops are involved. This leads to two 'loop' equations, which can be replicated by two 'circuit' equations, derived from a circuit model.

'Primitive' parameters relate to the performance of the conductors as antennae, 'loop' parameters can be measured using test equipment, and 'circuit' parameters are those found in a circuit diagram. This distinction is important.

A circuit model is created to generate two mesh equations. Components of the circuit model are then related to the inductive, capacitive and resistive elements of the primitive equations. Acknowledgment of the fact that current varies along the length of any signal carrying conductor leads to the use of T-networks in the final circuit model.

A simple example is used to illustrate the response of a 'victim' circuit in one conductor/ground-loop to the presence of a step voltage in the other loop. No tedious calculations are involved, since mathematical and circuit analysis software is used to full advantage.

This first example demonstrates conclusively that there is no such thing as an equipotential ground plane in a functioning system.

Shielding of any signal conductor is achieved, simply by routeing a second conductor along its length, and grounding this second conductor at both ends. Characteristics of the

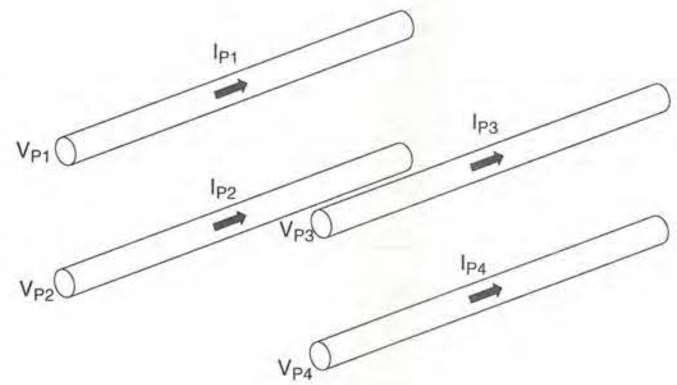


Fig. 1. Primitive – i.e. absolute – voltages and currents in four conductors

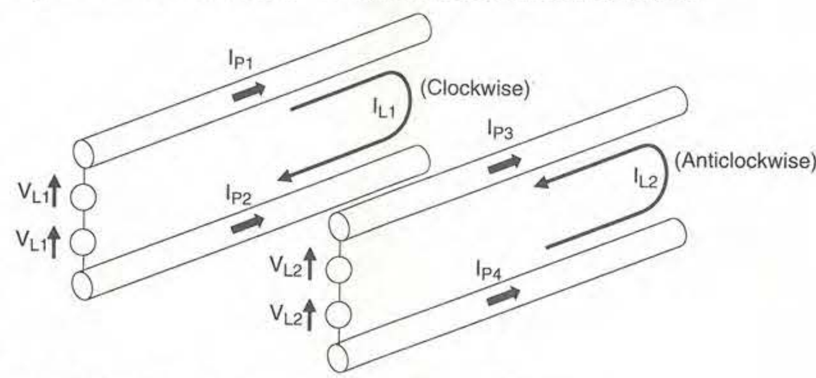


Fig. 2. Loop voltages and currents involved when two voltage sources are applied – one to the ends of conductors 1 and 2, the other to conductors 3 and 4.

Formulations

Consider the four isolated wires of **Fig. 1**. The configuration can be visualised as a section of a long structure, allowing end effects to be ignored. Assuming sinusoidal voltages and currents exist in the conductors, then,[2]

$$\begin{aligned} V_{P1} &= Z_{P11}\times i_{P1} + Z_{P12}\times i_{P2} + Z_{P13}\times i_{P3} + Z_{P14}\times i_{P4} \\ V_{P2} &= Z_{P21}\times i_{P1} + Z_{P22}\times i_{P2} + Z_{P23}\times i_{P3} + Z_{P24}\times i_{P4} \\ V_{P3} &= Z_{P31}\times i_{P1} + Z_{P32}\times i_{P2} + Z_{P33}\times i_{P3} + Z_{P34}\times i_{P4} \\ V_{P4} &= Z_{P41}\times i_{P1} + Z_{P42}\times i_{P2} + Z_{P43}\times i_{P3} + Z_{P44}\times i_{P4} \end{aligned} \quad (1)$$

where the subscript '*P*' identifies all primitives. If the integers *i* and *j* identify individual conductors, then the primitive impedances can be defined,

$$Z_{P_{ij}} = j\omega L_{P_{ij}} + R_{P_{ij}} + \frac{1}{j\omega C_{P_{ij}}} \quad (2)$$

$$L_{P_{ij}} = \frac{\mu l}{2\pi}\left(\ln\left(\frac{2l}{r_{ij}}\right) - 1\right) \quad (3)$$

$$C_{P_{ij}} = \frac{2\pi\varepsilon l}{\ln\left(\frac{l}{r_{ij}}\right)} \quad (4)$$

$$R_{P_{ij}} = \text{conductor resistance } i \quad (R_{P_{ij}} = 0 \text{ if } i \neq j) \quad (5)$$

where *j* is the complex operator, ω is the angular frequency, r_{ij} is the separation between the axes of conductors *i* and *j*, r_{ii} is the radius of conductor *i*, *l* is the length, while ε and μ are the permittivity and permeability of the insulation.

Assumptions inherent in equations (3) and (4) are that $l >> r_{ij}$, that the charge and current are evenly distributed on the surface of each wire, and that the concept of 'action at a distance' is valid.

The formulae for primitive inductors (3) and capacitors (4) may seem unusual, because these parameters are used to describe the characteristics of the conductors when the assembly is acting like an antenna. They relate the surrounding magnetic and electric field to current in the structure. Quantities defined in terms of henries or farads can have more than one interpretation!

One feature of primitive impedances is that they are symmetrical. Since $r_{ij}=r_{ji}$, it follows that $Z_{Pij}=Z_{Pji}$. Now assume that a voltage source, $2V_{L1}$, is applied between the ends of conductors 1 and 2, and that a voltage source, $2V_{L2}$, is applied between the corresponding ends of conductors 3 and 4, as shown on **Fig. 2**. Loop voltages with subscript '*L*' can be related to primitive voltages,

$$\begin{aligned} 2V_{L1} &= V_{P1} - V_{P2} \\ 2V_{L2} &= V_{P3} - V_{P4} \end{aligned} \quad (6)$$

Relationships between loop currents and primitive currents are defined in Fig. 2.

$$\begin{aligned} i_{L1} &= i_{P1} = -i_{P2} \\ i_{L2} &= -i_{P3} = i_{P4} \end{aligned} \quad (7)$$

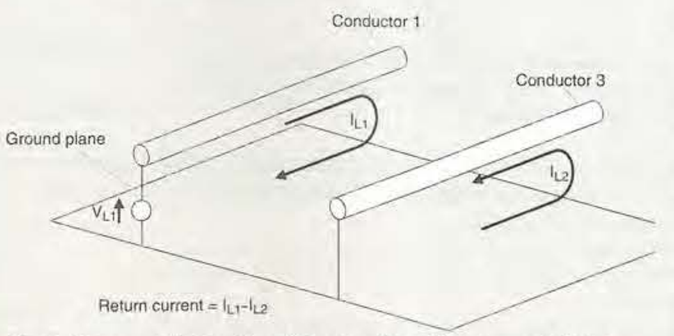


Fig. 3. Here, conductors 2 and 4 are replaced by a ground plane.

If conductors 2 and 4 are replaced by a ground plane and V_{L2} is replaced by a short circuit, the picture changes to that shown on Fig. 3. The relationships of equations (6) and (7) continue to apply. Substituting them in equation set (1) and taking account of symmetry of the image conductors leads to the loop equations,

$$\begin{aligned} V_{L1} &= Z_{L11}\times i_{L1} + Z_{L12}\times i_{L2} \\ 0 &= Z_{L21}\times i_{L1} + Z_{L22}\times i_{L2} \end{aligned} \quad (8)$$

where,

$$\begin{aligned} Z_{L11} &= Z_{P11} - Z_{P12} \\ Z_{L12} &= Z_{P14} - Z_{P13} = Z_{L21} \\ Z_{L22} &= Z_{P33} - Z_{P34} \end{aligned} \quad (9)$$

The main characteristic of loop parameters is that they can be measured with test equipment. Another characteristic is that they are symmetrical; $Z_{L12}=Z_{L21}$.

So far, the formulation has been in terms of electromagnetic theory. To create a circuit model, it is necessary to indulge in an exercise of lateral thinking and consider the question; "what configuration of components could be used to mimic the relationship between loop voltages and loop currents of equation (8)?"

Given the problem in these terms, it does not take long to sketch out **Fig. 4**, where the subscript '*C*' identifies circuit impedances. Comparing this with the equivalent circuit of a magnetic transformer identifies an earlier application of the concept.

Mesh analysis of Fig. 4 gives rise to the circuit equations,

$$\begin{aligned} V_{L1} &= (Z_{C11} + Z_{C12})\times i_{L1} - Z_{C12}\times i_{L2} \\ 0 &= -Z_{C12}\times i_{L1} + (Z_{C12} + Z_{C22})\times i_{L2} \end{aligned} \quad (10)$$

Correlating the terms of the circuit equations (10) with those of the loop equations (8) allows each circuit impedance to be defined in terms of loop impedance. Using equations (9), the circuit impedances are then related to the primitives.

$$\begin{aligned} Z_{C12} &= -Z_{L12} = Z_{P13} - Z_{P14} \\ Z_{C11} &= Z_{L11} + Z_{L12} = Z_{P11} - Z_{P12} - Z_{P13} + Z_{P14} \\ Z_{C22} &= Z_{L12} + Z_{L22} = Z_{P33} - Z_{P34} - Z_{P13} + Z_{P14} \end{aligned} \quad (11)$$

Since each primitive impedance is defined in terms of inductance, capacitance, and resistance in equation (2), each circuit impedance will also contain *L*, *C* and *R* parameters. Using equations (3), (4), and (5), the formula for each component can be derived. For resistors, the derivation is simple,

$$\begin{aligned} R_{C11} &= R_{P11} \\ R_{C12} &= 0 \\ R_{C22} &= R_{P33} \end{aligned} \quad (12)$$

It is possible to write out the formulae for reactive components merely by inspecting equation set (11). These are listed in the Appendix, under the heading "derivation of electrical parameters".

Detailing the elements of Fig. 4 leads to the initial circuit model, **Fig. 5**. This is rather crude, since it overcompensates for the fact that current in the capacitors will alter the voltages in the inductors. A better model can be formed, using the familiar T-junction. This leads to **Fig. 6**.

By invoking the star-to-delta transformation shown in the Appendix, the node at the junction of the three capacitors can be removed, giving the final circuit model of **Fig. 7**.

Using equation set (12), the resistors of Fig. 7 can be related to hardware.

With a one-to-one correlation between the conductors of Fig. 3 and the horizontal branches of the circuit, Fig. 7 can be treated as a section of a three-conductor transmission line. The simulation is surprisingly accurate[2].

new configuration are assessed without difficulty.

Using this technique with modern software, the design of equipment can be tailored to meet emc requirements.

Coupling via the ground plane

To put flesh on the bones of the dry theory in the panel entitled 'Formulations', the first action is to assign dimensions to the physical parameters of **Fig. 3** shown in the panel. One example is shown in **Fig. 8**.

At this point the value of mathematical software[3] becomes evident. When such software is accessed, the relevant equations can be typed on to the computer screen as easily as words when a word processor is used. The Appendix presents the entire calculation process, including the input data and the tabulation of results. Plugging these values into Fig. 7 gives the basic structure of **Fig. 9**.

In this example, conductor 1 is defined as the 'culprit', and fed with a 5 V step voltage, V_{in}, via a 100Ω resistor. The load at the far end is 1kΩ. Conductor 3 is nominated as the 'victim' conductor.

The victim circuit is shorted at one end and loaded with 1kΩ at the other. Voltage V_{out} across the resistor is deemed to be the signal under review. No conductor has zero resistance, so a finite value has been assigned to the ground plane.

Having created a circuit model, the next step is to analyse it, and this brings into play the processing power of circuit analysis software[4]. In this application, such software is even more impressive than the mathematical variety, because it obviates the need to check any equation.

All that is necessary is to draw the circuit on the screen and define component values. The computer program generates the necessary vectors for use in the analysis. The type of analysis, the test limits, and the signals to be examined are then selected, and at the touch of a key the output is presented on the screen.

For the circuit of Fig. 9, the transient voltage V_{out} is shown in **Fig. 10**. This should be no surprise to anyone who has monitored logic signals on an oscilloscope using a voltage probe. The spurious signal has the classical damped sinusoidal waveform, indicating an oscillatory condition.

Reflections

No need to puzzle very long to identify the reason for this: the loads at each end of the transmission line are causing reflections.

Charges are surging backwards and forward along the two metre line, mostly along the ground conductor. Energy is stored dynamically in the electric and magnetic field surrounding the conductors.

With the ground plane acting as an inductor and oscillatory current flowing in that inductor, a significant voltage is developed along the length. Since the victim loop utilises the ground plane to form its return conductor, this voltage appears in series with the expected signal in that loop.

A spurious signal, V_{out} is received by any circuit which monitors the voltage across R_{victim}. From the point of view of the victim circuit, current in the structure is emanating from an external source. Circuit theory tells us that the same effect can be achieved by a voltage generator in series with the ground conductor. The ground plane acts as a voltage source. It is anything but an equipotential surface.

However that is not the only deduction. In addition to predicting the existence of a ringing signal, Fig. 10 provides information on the frequency of oscillation (about 33MHz) and on the amplitude, peaking at about 200mV. This particular resonance correlates with the quarter wave frequency.

Further development of the circuit model to include the

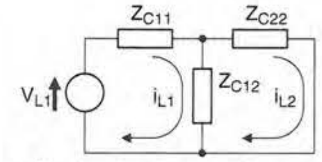


Fig. 4. This circuit gives a set of equations similar to loop equations.

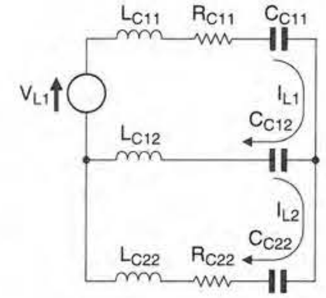


Fig. 5. Initial circuit model, identifying individual components.

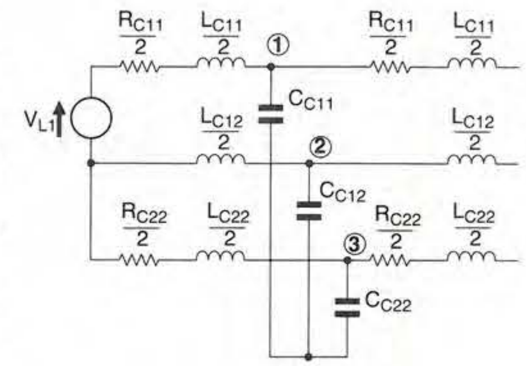
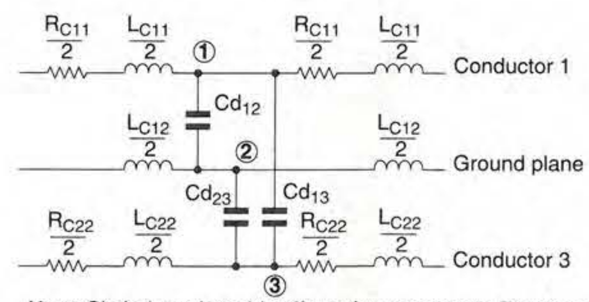


Fig. 6. The model is improved by converting each branch to a T network.



Note: Circled numbers identify nodes common to Figs 6 and 7

Fig. 7. Final circuit model after transformation from star to delta.

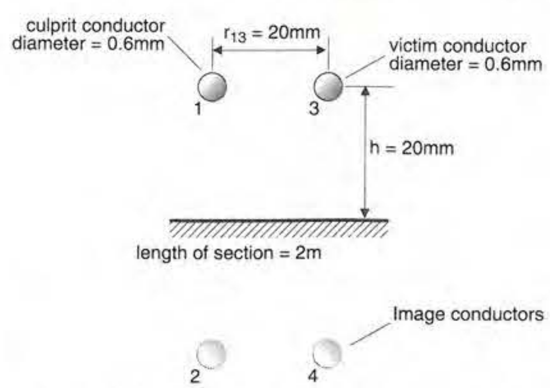


Fig. 8. Physical dimensions of the two wires over a ground plane used in the example.

active components which interface with the conductors is a simple matter. If the signal across R_{victim} is to be monitored by a logic gate, then simulation will show whether or not the device will generate a spurious pulse in response. Measures can be taken, at the initial design stage, to prevent such an occurrence.

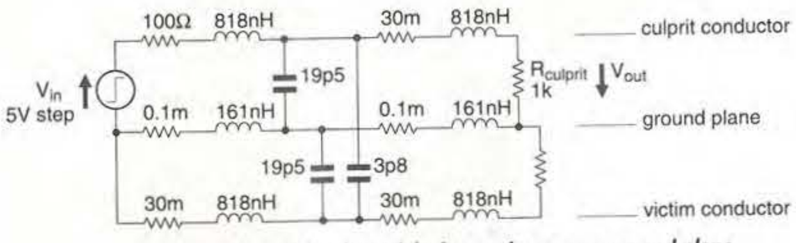


Fig. 9. Circuit model of two wires over a ground plane.

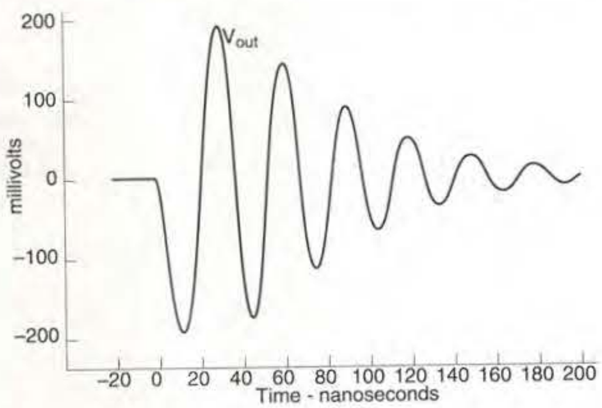


Fig. 10. Response of victim circuit to a 5V step in culprit circuit.

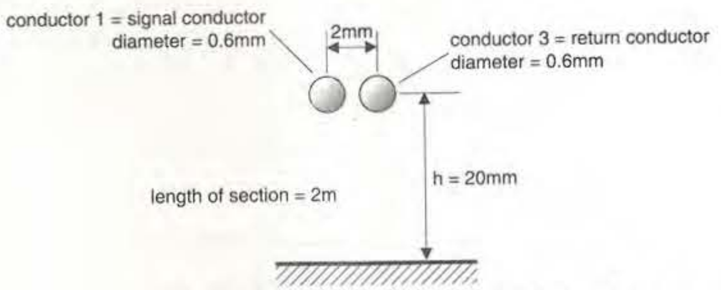


Fig. 11. One way to reduce interference is to allocate a second conductor to carry the return current. This should be mounted as close as possible to the one carrying signal current.

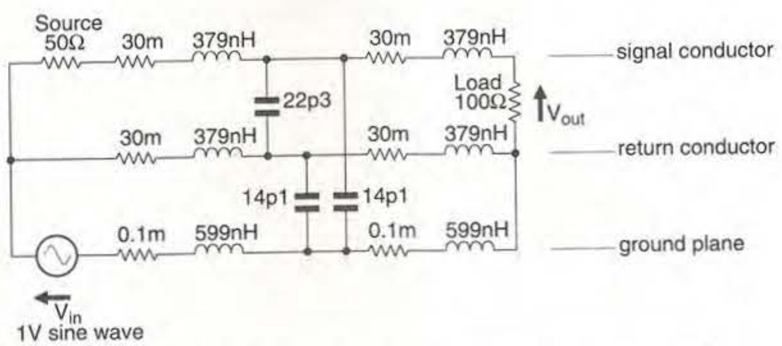


Fig. 12. Circuit model for the two wires over a ground plane configuration shown of Fig. 11.

Shielding: the first step

Perhaps the most important way of reducing interference is to allocate a conductor to carry return current, and to route that conductor as close as possible to the one carrying signal current. **Figure 11** shows the new wiring configuration.

Exploring the implications of this is quite a simple task. Going to the Appendix and altering the value of r_{13} from 20mm to 2mm will change all the reactive values in the tabulation of results.

The simplest way of ensuring that conductor 3 acts as a return conductor is to link it to local structure – the ground plane – at both ends. Values of 50Ω and 100Ω are fairly representative of the source and load resistors. **Figure 12** illustrates the effect of these changes to the model.

Inspection of this circuit reveals that the inductance of the return conductor is less than that of the ground plane, even though it presents a relatively high resistance. So this conductor is indeed the preferred return path for hf signal current.

Capacitance between signal and return conductors will enhance this effect. As the frequency increases, the performance of the wire pair approaches that of the ideal transmission line, the most efficient way of carrying electrical energy from source to load.

To determine the effect of interference, **Fig. 12** includes a sinusoidal voltage source of 1V in series with the ground. Carrying out a frequency response analysis, again using computer aided design,[4] results in **Fig. 13**. This shows that between 10kHz and 10MHz, the attenuation of any spurious signal is more than 10dB.

Above 10MHz capacitive effects cause the attenuation to increase further, but beware of resonance peaks! The model predicts one at 43MHz, pointing towards the half wave resonance. The dip in the curve correlates with quarter wave resonance. Actual tests would determine the frequency of the dip and peak more accurately.

Even in the presence of resonance, a wire pair will reduce interference.

Implications

Treating the structure as a large diameter conductor results in three primitive equations and two loop equations. Circuit model Fig. 7 remains valid, even though component formulae change. By increasing the number of conductors in the configuration, more complex circuit models can be created, allowing all the usual circuit interconnections to be analysed.[2]

Using general-purpose test equipment such as the oscilloscope, signal generator and toroidal transformer, it is possible to make practical measurements and build up circuit models of actual hardware[2]. Circuit analysis of the models will allow system performance during formal emc testing to be predicted.

Transient analysis and frequency analysis of complex circuits are simple tasks with modern software[4]. Anyone who can design electrical equipment can learn to analyse emc.

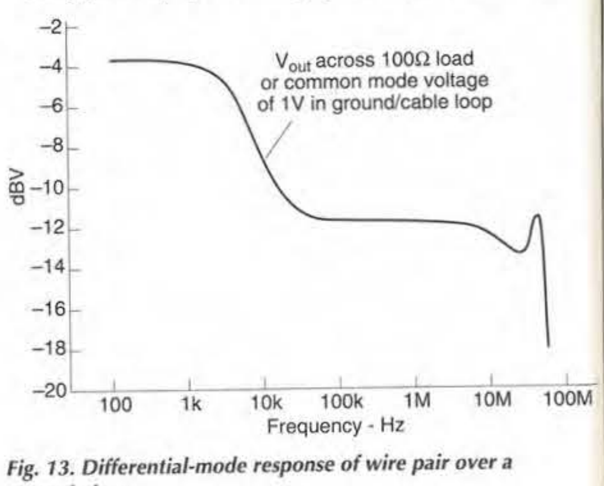


Fig. 13. Differential-mode response of wire pair over a ground plane.

In summary

Two conclusions of practical importance are,

- It is a bad mistake to assume that the ground plane is an equipotential surface, or that two points marked with the earth symbol are at the same voltage.
- A significant improvement in emc can be realised, simply by allocating two conductors to every signal and routeing those conductors together.

Of even greater importance is the fact that circuit modelling can be used to assess the merits and failings of any particular system, allowing design decisions to be based on analysis rather than on a debatable set of guidelines. ■

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3. Mathcad plus 6.0 (Adept Scientific plc, 6 Business Centre West, Avenue One, Letchworth, Hertfordshire SG6 2HB).
4. 'Geseca for Windows: Spiceage for Windows' (Those Engineers Ltd, Mill Hill, London NW7 4BP).

Appendix – coupling calculations.

These are calculations for coupling between two wires over a ground plane. Mathcad was used to compute the results.

$\mu := 4\pi 10^{-7} H/m \quad \varepsilon := 8.854\times 10^{-12} \quad \rho := 1.7\times 10^{-8}$ ohm.m (resistivity of copper)

$r_{1,1} := 0.3\times 10^{-3} \quad r_{3,3} := 0.3\times 10^{-3} \quad r_{1,3} := 20\times 10^{-3} \quad h := 20\times 10^{-3} \quad l := 2\text{m}$

Derived dimensions

$r_{1,2} := 2\times h \quad r_{1,4} := \sqrt{(r_{1,2})^2 + (r_{1,3})^2} \quad r_{3,4} := r_{1,2}$

Derivation of electrical parameters

$$Lc_{1,1} := \frac{\mu l}{2\pi}\ln\left(\frac{r_{1,2}\times r_{1,3}}{r_{1,1}\times r_{1,4}}\right) \quad Lc_{1,2} := \frac{\mu l}{2\pi}\ln\left(\frac{r_{1,4}}{r_{1,3}}\right) \quad Lc_{2,2} := \frac{\mu l}{2\pi}\ln\left(\frac{r_{1,3}\times r_{3,4}}{r_{3,3}\times r_{1,4}}\right)$$

$$Cc_{1,1} := \frac{2\pi\varepsilon l}{\ln\left(\frac{r_{1,2}\times r_{1,3}}{r_{1,1}\times r_{1,4}}\right)} \quad Cc_{1,2} := \frac{2\pi\varepsilon l}{\ln\left(\frac{r_{1,4}}{r_{1,3}}\right)} \quad Cc_{2,2} := \frac{2\pi\varepsilon l}{\ln\left(\frac{r_{1,3}\times r_{3,4}}{r_{3,3}\times r_{1,4}}\right)}$$

$$Rc_{1,1} := \frac{\rho 1}{2\pi(r_{1,1})^2} \quad Rc_{2,2} := \frac{\rho 1}{2\pi(r_{3,3})^2}$$

Star to delta transformation

$$Cd_{1,2} := \frac{Cc_{1,1}\times Cc_{1,2}}{Cc_{1,1}+Cc_{1,2}+Cc_{2,2}} \quad Cd_{1,3} := \frac{Cc_{1,1}\times Cc_{2,2}}{Cc_{1,1}+Cc_{1,2}+Cc_{2,2}}$$

$$Cd_{2,3} := \frac{Cc_{1,1}\times Cc_{2,2}}{Cc_{1,1}+Cc_{1,2}+Cc_{2,2}}$$

Results

$$\frac{\text{Lc}}{2} = \begin{pmatrix} 8.176\times 10^{-7} & 1.609\times 10^{-7} \\ 0 & 8.176\times 10^{-7} \end{pmatrix} \text{ henry}$$

$$\text{Cd} = \begin{pmatrix} 0 & 1.953\times 10^{-11} & 3.844\times 10^{-12} \\ 0 & 0 & 1.953\times 10^{-11} \end{pmatrix} \text{ farad}$$

$$\frac{\text{Rc}}{2} = \begin{pmatrix} 0.03 & 0 \\ 0 & 0.03 \end{pmatrix} \text{ ohm}$$

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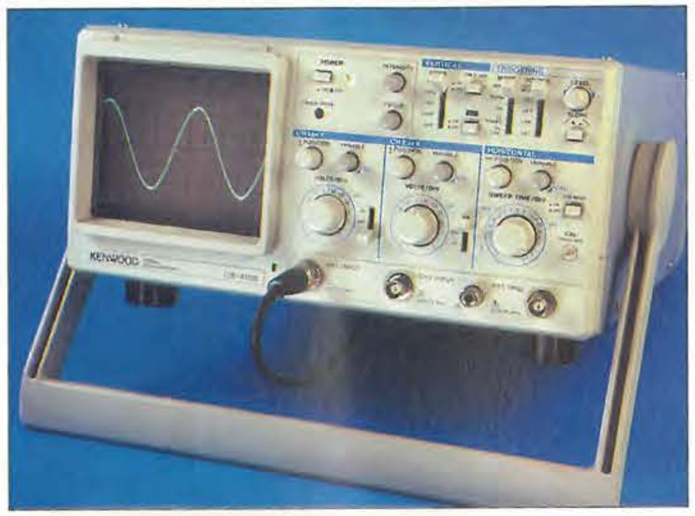

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SPEAKERS CORNER

John Watkinson asks why, now that power amplifiers are so cheap, are passive crossover networks still being used?

One of the problems with loudspeakers is that every electronic engineer thinks loudspeaker design is easy. The easiest part ought to be the crossover, because, hey, it's only electronic components.

Looking at commercially available loudspeakers reveals the truth, which is that most of them have sub-optimal crossovers because in reality it's not that easy.

The traditional approach shown in **Fig. 1** was to have one large wideband amplifier with a passive network between that amplifier and the drive units. Passive filters would be somewhat easier to design if they fed a load having a constant impedance. Unfortunately a drive unit presents anything but a constant impedance and this affects the filter response.

A further problem is that passive crossovers have to handle power. Power inductors and capacitors are physically large, and if they are to be free of distortion they will also be expensive. When power amplifiers were difficult and expensive to make, this was acceptable.

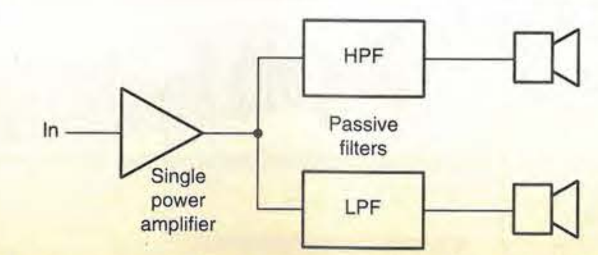


Fig. 1. In a traditional loudspeaker, a single wideband amplifier feeds two or more drive units via a passive crossover network.

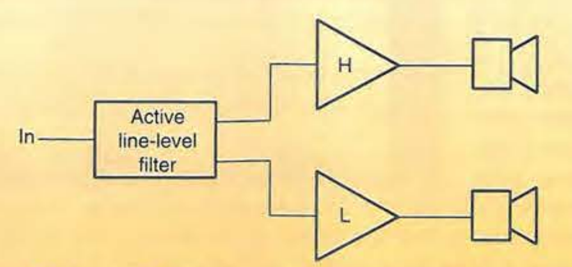


Fig. 2. Power amplifiers are now relatively cheap. An active crossover and multiple power amps allows much more precision than a single amp and passive crossovers. So why are passive crossovers still popular?

Why not have an active solution?

But times change. High-quality audio amplifiers are now extremely cheap and it makes sense to adopt the approach of **Fig. 2**, where the crossover is performed at line level and each transducer has its own power amplifier.

Now the filters drive a constant impedance and so will perform as designed. With no high power passive components, the system could actually cost less for the same quality.

Distortion is lower for two reasons: each amplifier is working over a narrower frequency range, and each handles less current. The vastly superior results obtained with active crossovers mean that, where quality is paramount, passive speakers are obsolete.

The only future for the passive speaker is in so-called high end hi-fi where enthusiasts love to mess about and replace perfectly serviceable parts with gold plated ones. Unfortunately active speakers don't lend themselves to this kind of thing and so the high-end freaks don't like them on principle. It's their loss.

An ideal crossover ought to be inaudible. For this to happen, the crossover and the drive units must form a system which is ideal in the frequency, time and spatial domains. Traditional loudspeaker designers think they are doing well if they meet the first criterion. Unfortunately the other two are just as important.

Time response is critical

As I mentioned in an earlier piece, the time response is critical if transient waveforms are not to be linearly distorted. Thus the speaker system should be phase linear. This means that the time taken for a signal to pass through the speaker should be the same at all frequencies – including the crossover frequency.

The conventional high-pass/low-pass of **Fig. 3** can never be phase linear. Irrespective of the order of the filters, if the outputs are added back together, the original waveform is not obtained and the criteria for inaudibility cannot be met.

One solution to this was the development of the filler driver. This was an additional drive unit which would add signals around the crossover frequency only, allowing a passive system to accurately reconstruct the input waveform. The extra drive unit adds to the cost and may worsen directivity problems.

The only crossover topology to meet both the frequency and time criteria without a filler driver is the so-called constant-voltage crossover. This uses subtractive techniques developed in analog computing to produce complementary outputs.

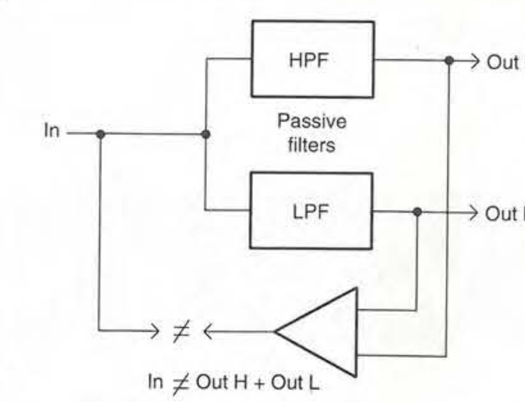


Fig. 3. The conventional high-pass/low-pass solution can never be phase linear – regardless of filter order.

Spatial response

Even if a constant-voltage crossover is created, having outputs which sum back to the original signal, there is another hurdle to overcome. This is the spatial response.

The crossover frequency will be audible if there is a change in directivity at the crossover. At the crossover frequency, each transducer is providing half of the acoustic output. Thus the acoustic size of the resulting combined transducer is roughly the distance between the two driver axes.

If this distance approaches a wavelength, the radiation at the crossover frequency becomes directional. This can be heard because even if the on-axis response remains flat, the reverberant field will be impaired.

Thus in theory – and in practice – the only way a crossover can be made inaudible is to make the crossover frequency sufficiently low that the spacing between the drivers is much less than the wavelength. In practice this means that the crossover cannot be much above a few hundred hertz.

Thus the speaker with three or four drive units each handling a different frequency range is fundamentally flawed as only the lowest crossover can be inaudible. This explains why two-way loudspeakers often score high marks for realism and stereo imaging and why dual-concentric or coaxial drive units also have a strong following.

A loudspeaker which retains linear phase through the crossover region is currently rare, but the realistic handling of percussive instruments and natural transient sounds makes it well worth the effort. ■

Windows 98

If you are using Windows 95, or you didn't upgrade to it because you were worried about its lack of polish, Windows 98 is for you. But many engineers are still happy with Windows 3.x. Should they upgrade? Rod Cooper wonders.

It is now three years since Windows 95 arrived, amid much hype, with great expectations of replacing Windows 3x entirely and establishing itself as the o/s of choice.

Despite the flaws in Windows 95, which the critics have delighted in exposing, it has enjoyed considerable success. But the really astonishing thing is that so many people have stayed with Windows 3.x – millions of them.

This phenomenon is so apparent that a major program producer – Corel – recently announced that it had produced a *new* program for Win 3.x, *Wordperfect Suite 7*, with most of the things that you would expect in the equivalent Corel Windows 95 product – including Internet connectivity. Shock horror!

To perpetrate this heresy, there must be a money incentive, implying a large, stable market for potential Windows 3.x products – a fact that will not be lost on other program makers.

Where, then, does Windows 98 fit in this scenario? If you look at Windows 95 when it first appeared and then the latest version, you will see that today's Windows 95 is a much changed and added-to program. What Windows 98 does is to rationalise the ad-hoc changes made to Windows 95 since the first release and to add a further batch of minor improvements to Windows 95 rather than introduce any big advance in technology.

> **Windows 98 – installation**
> Comes on cd only
> Needs 120MByte of hard disk space to install and occupies about 75Mbyte depending on options. Takes about an hour to up-grade from Windows 3.1.

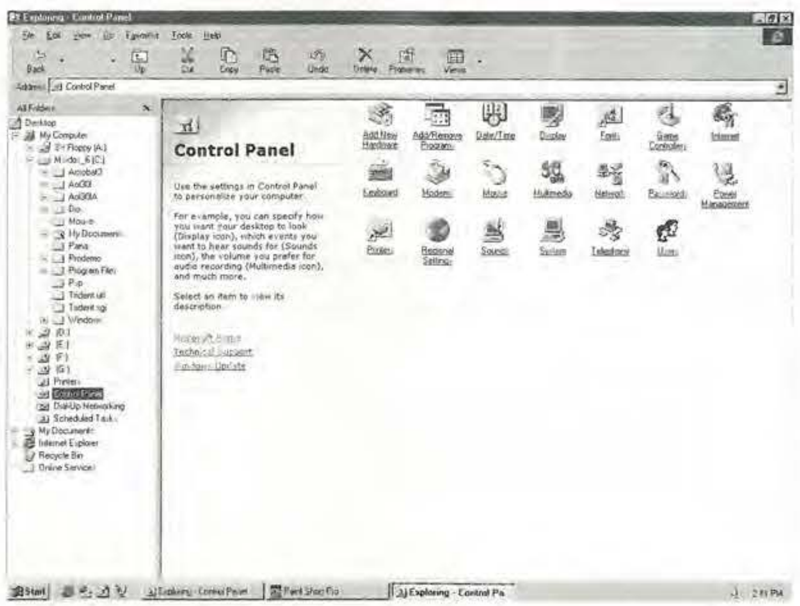


Fig. 1. View of Control Panel via Windows Explorer with the "Web-look" option turned on.

Those of you who were expecting to find integrated voice recognition in Windows 98 will be disappointed! Of course, voice recognition is available as a third-party Windows application, but the proponents of voice recognition maintain that the best method is to have it imbedded in the operating system, as with OS2/Warp for example.

Integrated browser

What *is* integrated into Windows 98 is Internet Explorer 4.0. Followers of the recent court case between the US Dept. of Justice and Microsoft will realise that this addition appears to get round the main legal objections of pc manufacturers having IE 4.0. compulsorily foisted on them, bundled with Windows 95.

So is the inclusion of Explorer 4.0 inspired by political or technical merit? Probably a bit of both.

What is interesting is that Microsoft has gone one stage further by offering a web-based desktop in Windows 98. Yet another GUI to learn, most people will cry, but fortunately this isn't compulsory and you can have the so-called "classic" Windows look if you want.

This does seem to indicate a general trend by Microsoft to make Windows less of a stand-alone operating system, but more of an Internet engine. If you are an Internet enthusiast, this approach will appeal to you. If you just use your pc as a stand-alone work-horse, this trend may ring alarm bells.

98's general features

Windows 98 maintains support for 16-bit programs just as in Windows 95, but is orientated away from the FAT16 file system and towards the new FAT32 system. More about this later.

If you choose the "classic" look as mentioned above the appearance of the desktop is very similar to Windows 95. **Figures 1** and 2 shows what you get with "Web Look".

Operation is slightly smoother and faster than Windows 95. For example you can launch programs with a single click and the forward and back buttons shown in Fig. 1. This can make life easier. System startup is said to be faster, but subjectively the saving is so small I didn't notice it. System shutdown took slightly longer.

One of the big gripes in Windows 95 was that the minimise, maximise and close buttons were so close together that accidental operation was possible, but this remains the same. Why on earth these have not been altered, considering the widespread criticism, is anyone's guess.

Those of you who were expecting an advance in reliability in multi-tasking will also have to console yourselves. Has this aspect been improved on in Windows 98? I could detect nothing in the literature or in operation to suggest this.

Better reliability?

Claims for better reliability in Windows 98 do not centre on improved multi-tasking, but on testing and automatic error-fixing the hard disk, system files and configuration. Here, there has been a significant improvement with Registry Checker and System File Checker. Windows 98 can check itself on loading with *Registry Checker* and correct itself from a set of backup files that it holds.

System File Checker, as the name implies, checks Windows system files for corruption and can restore them from the cd or from a backup set.

The most likely cause of trouble is badly-written third-party programs interfering with the system files. This used to be a problem with Windows 95. However, with both registry and system file checkers, if the system is so corrupt it won't load, then you are back to square one.

Disk enhancements

Disk Cleanup is a new tool which displays files deemed to be unnecessary and invites you to delete them. This is a big time-saver on sorting through files for removal yourself. From what I could see of Cleanup, it tended to be conservative, i.e. you are unlikely to delete anything vital.

Disk Defragmenter would be better named fragmentation control, as it not only defragments the hard disk drive in the way everyone is accustomed to, but can also do the opposite!

The defragmenter may re-arrange program files in order to start programs quicker and this may give the disk the appearance of being fragmented. In this situation, third-party defragmenters may report the hard disk to be heavily fragmented when there is actually no need to defragment. If you then run a conventional defragmentation, you will lose the optimum configuration for a faster start.

Tune-Up is another good idea. This tool runs the defragmenter, ScanDisk and Cleanup on a scheduled basis, like a tape back-up utility.

You could set it to run during the lunch-hour for example. With the huge size of current hard disks and the 'bloatware' that goes on them, Defrag and ScanDisk take a lot of time to run, so this is a welcome addition.

Task Scheduler is an easy-to-use device for starting almost any event – for example a program or file – at a set time.

Support

Support is included for the Universal Serial Bus, and for DVD-ROM as a storage device to the SFF8090 specification, including DVD movie playback.

There is a whole raft of new device drivers, including support for some scanners and cameras, and support for infra-red links. Many other small enhancements have been incorporated which cannot be included here for lack of space. But one of the most significant changes is in the FAT system, FAT32.

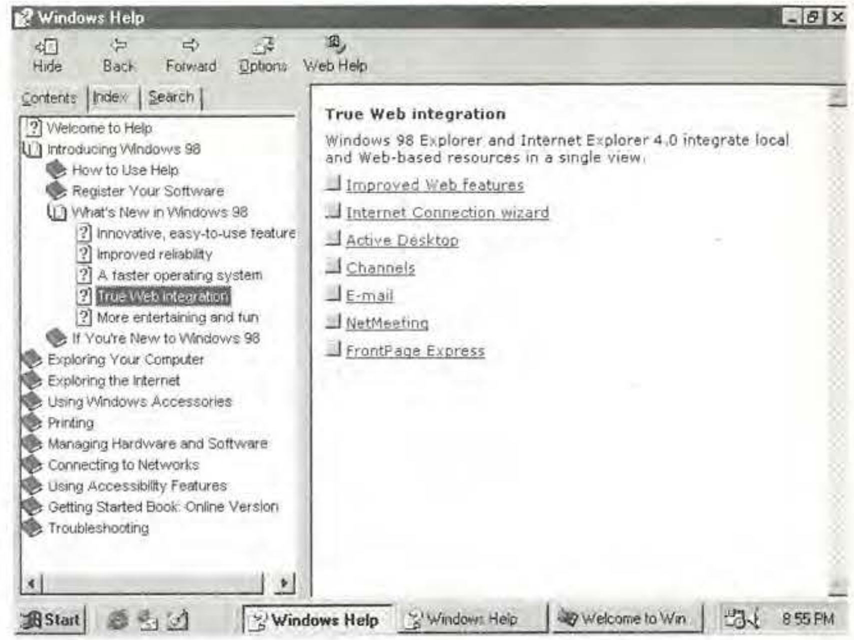


Fig. 2. A similar view to that in Fig. 1 but under the Help tool, showing just how much emphasis is being put on Web integration.

New file allocation table

Much emphasis is laid in the Windows 98 notes on the use of FAT32, the new file system for improving hard disk performance.

This is the preferred system for Windows 98, but you don't have to use it if you don't want to. There are some good reasons for sticking to the established FAT16 standard, mainly because most operating systems can recognise it and it is compatible with all the software intended for pc use to date.

FAT 32 introduces some fresh incompatibilities. Although you can dual-boot between FAT 16 Windows 98 and other operating systems, you can't dual-boot with FAT 32 Windows 98 and such o/s as Windows NT, Windows 3.1 or MS-DOS6.x or OS/2.

Drives formatted under FAT32 cannot be seen by other operating systems – even if you do manage to dual-boot from a FAT 16 drive. FAT 32 drives cannot be compressed with programs like DriveSpace. And if you do convert to FAT 32 you can't go back to FAT 16, unless you buy one of the add-on third-party converters.

Bear in mind that you cannot get a FAT 32 drive onto anything less than 514Mbyte, so if your hard disk is smaller than this, it means buying a new, larger hard drive.

The reason for creating FAT 32 is due to the cluster sizes created under FAT. The cluster size depends on how large the drive is. These are as shown in the **Table 1**.

If a file is just one byte over the size that one cluster can contain, then it occupies one whole further cluster. With the small number of files in older programs, this waste of hard disk space did not really matter. However, with the huge programs of the present day, it matters a lot because there will be a large number of these partially-filled clusters and consequent waste of disk space.

If the cluster size is large, say 32Kbyte, then you could in theory have just ten excess bytes from ten files occupying 320Kbyte, clearly a ridiculous waste of space. It pays therefore to have a small cluster size.

Better FAT means smaller clusters

In FAT 16, a cluster size of 2Kbyte, using a 128Mbyte drive, would use up only 20Kbyte in this situation. However, the downside is that you would have a large number of clusters and this imposes an extra overhead on the cpu. But this applies to FAT 16 *and* FAT 32. On today's ever-faster machines you probably would not notice this.

It pays dividends therefore to divide any hard disk into drives C:, D:, E:, etc. to get the cluster size down. Many people put their operating system on one drive, C:, with perhaps an alternative operating system on D: if they are dual-booting. Applications can go on drive E:, and data on F:.

An extra benefit of this scheme is that backing up with tape backup is easier. For example, on FAT 16 with a cluster size of 2Kbyte, drives C: D: E: and F: each of 120Mbyte or less were convenient to back up on the cheap and popular 120Mbyte QIC DC2120 cartridges.

Backing up drives individually also had other benefits. It got round the problem of the long time taken to back up a single large drive when only part of the drive needed backing up.

Note that with FAT 16 you can get the cluster size down to a lower size than with FAT 32.

Of course, the need for an improvement in file handling has been triggered by the very large size of the current crop of programs. Many would argue that more efficient programming could reduce the size and ease not just this problem but many others as well.

As Table 1 shows, FAT 16 can allocate up to only 2Gbyte for any one partition. With today's large capacity hard drives, and the trend for them to become ever larger, this limit could become an obstacle.

But do you really need partitions of more than 2Gbyte? Admittedly, at this size of drive, FAT 16 becomes less efficient at a cluster size of 64Kbyte compared to FAT 32's 4Kbyte. FAT 32 overcomes both these shortcomings with a maximum drive allocation if 2Tbyte and a maximum cluster size of 32Kbyte. But are these advantages worth the incompatibility problems?

Table 1. FAT 16 versus FAT 32.

FAT 16

Drive size in Mbyte	Cluster size in Kbyte
16 to 128	2
128 to 256	4
256 to 512	8
512 to 1024	16
1024 to 2048	64

FAT 32

Drive size in Gbyte	Cluster size in Kbyte
0.513 to 8	4
8 to 16	8
16 to 32	16
32 and above	32

Fig. 3. Windows 98 desktop showing the sub-menus. Initially looks the same as Windows 95, but note the number of Internet features and the increase in the number of system tools.

Is FAT 32 faster?

FAT 32 does not speed up the system performance when running applications. This was proved with a series of benchmark tests in the magazine *PC Direct* (Joseph Moran, May '97).

What is claimed for FAT 32 is that loading the application is faster. If you have long loading times, this could be attractive. If not, this feature is wasted.

The main advantage of FAT 32 seems to be that some hard disk space is recovered. How much is recovered will depend on exactly what is on your hard disk. And if modern hard disks are providing vast amounts of space anyway, is this important?

Windows 98 and the Internet

As you can see from **Fig. 3**, the Internet and Explorer 4 both feature prominently on the Windows 98 desk-top. Besides incorporation of a Web-based look and feel into the operating system, there are several more interesting features.

Internet Connection Wizard provides an easy step-by-step route to signing up with a service provider. This is particularly useful for first-time users who may feel a bit nervous about this.

Microsoft Outlook Express is a general-purpose e-mail and news reader, but it cannot yet be used with certain services, notably AOL and CompuServe.

Update Wizard is a web-based method of keeping abreast of developments for Windows 98 by providing access to updated system files, hardware drivers, patches etc.

Report Tool is a similar Web-based tool, but works in reverse – you use this to send details of any bugs you come across to Microsoft.

Need more screens?

For some applications, like CAD, more screen area is desirable. One way to do this is to spread the desktop over two monitors. In the past, it was not uncommon in CAD to see the drawing area and the program controls on different screens.

To do this with Windows 98, your motherboard must have a PCI or AGP chipset, and of course you need an extra video card for each monitor.

Up to nine monitors can be run like this. It is possible to use different resolutions, colour depth, etc for each monitor. The literature claims that applications need no modification to use this type of display, but that application developers can take advantage of some new APIs provided in Windows 98, presumably to optimise the application for two-screen operation.

While any PCI card can be used for the primary display, the second PCI card must comply with Windows 98 secondary drivers. Table 2 from the Windows 98 literature gives the cards are suitable;

In summary

There are some users for whom Windows 98 will have instant appeal;

- professional CAD users, for whom there are advantages in using more than one screen
- Those who regularly use the Internet and who would like to see Internet features embedded in the operating system.
- Windows 95 users whose applications or methods of operation cause problems, who will welcome the new fault checks and system tools.

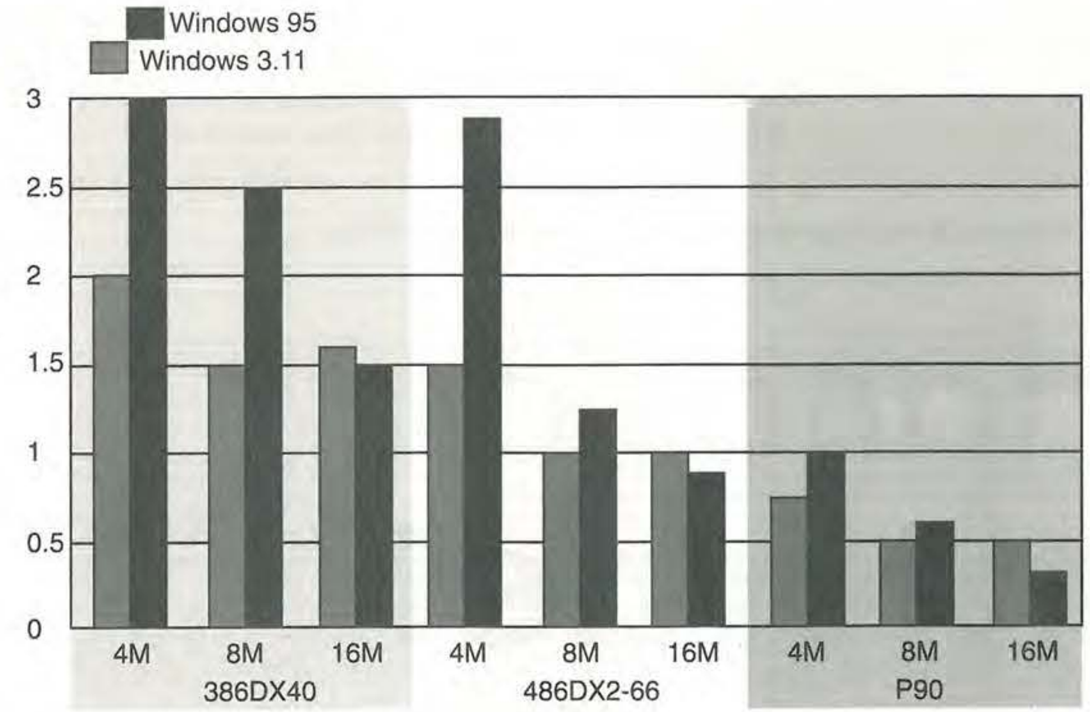


Fig. 4. Speed of Windows 3.x compared with Windows 95 on various pcs. Note that the vertical axis is relative time, so taller bars are slower.

But is Windows 98 sufficiently attractive for existing users of Windows 3x to buy it? For them, it would almost certainly mean considerable expenditure in up-grading hardware. There is of course, the irrational fear of "missing out" on something new to contend with.

Those of you who stayed with Windows 3.x have certainly been enjoying a recent and on-going bonanza of free or very cheap 16-bit programs from such sources as the front covers of magazines – particularly during the period that the program makers were shifting over to 32-bit software.

And these stick-in-the-muds haven't had to expend time and effort to re-learn the new and much-criticised Windows 95 interface or buy large amounts of new equipment.

Of course Windows 3.1 will not run as fast as the 32-bit Windows 95, will it? Well, this is not necessarily so, as Mike James proved in the November 1995 issue of *Computer Shopper* with his set of benchmark tests, **Fig. 4**.

Naturally, things have moved on since November 95, with faster pcs appearing on a regular basis. But every increase in hardware speed increases Windows 3.x's speed as well, and Windows 3.x owners know it. They also know that their existing 16-bit programs do not run as fast on a 32-bit operating system.

Recently, I went back to Windows 3.1 to compare some more recent offerings in 32-bit office suites with their older 16-bit counterparts. When it comes to word processors, spreadsheets and the like, the subjective advance in speed is not all that noticeable, all other things being equal.

In some cases, the advances in programs themselves were not all that apparent either.

To persuade people to move to a new operating system, and buy replacement software to match, the new option must offer really significant advantages – not just hype. And any advantages must be applicable to themselves in their everyday computer usage, rather than be theoretical.

As a prime example of this, one of the major features of Windows 95 was the improvement in multi-task ability. In Windows 3x, this was a difficult area, so you would think that this would be an inducement to up-grade. But comments in the pc magazines indicate that most *ordinary* people with pcs tend to do things *one at a time*. In real life, it is rare indeed for the pc in the office or home to be called on to multi-task. The only time I have noticed it in offices is during a long database search.

Table 2. PCI cards suitable for secondary monitors.

Suitable drivers:
ATI Mach64 GX
S3 764V+ (765), Trio 64V2
S3 ViRGE
S3 Aurora (S3M65)
Cirrus 5436, 7548,5446
ATI Rage 1 and 2 (VT and greater)
ATI 3D Rage Pro
Trident 9685/9680/9682/9385/9382/9385-1 PCI

These drivers have DirectDraw support:
ATI Mach64
S3 ViRGE

This driver has Direct3D support:
S3 ViRGE

The following cards cannot be used as a primary display adapter:
Permedia (Permedia NT and Permedia-2 OK)
ISA/EISA cards

For some engineers, however, it is very handy to run a lengthy CAD routine, or some number-crunching program or lengthy analysis, in the background in order to continue working – writing a technical report in a word processor for example. Windows 3x is not for them.

But if you are not one of these people, why move to Windows 95 – or Windows 98?

As for current users of Windows 95, I think many will want to change to Windows 98. They will already have most of the necessary hardware. Perhaps they will have to buy a new hard disk to accommodate FAT 32, which cannot install on anything smaller than 514Mbyte.

But apart from that, Windows 98 runs well on a Pentium with 16 to 32Mbyte of ram. The various enhancements detailed above will make life much easier for them ■

Year 2000 is not only a bios problem. Even NT users can suffer, as Cyril Bateman has been finding out. And he has news of a company searcher, a dos-based simulator for analogue plls and Motorola's field-programmable analogue chip.

Hands-on Internet

Intel's 'Katmai' processor is expected to be released early next year. Targeted for use in high-performance desktop systems, Katmai is expected to run initially at 500MHz using a 100MHz system bus.[1]

Apart from speed enhancement, Katmai introduces some 70 additional instructions for increasing performance. To enable software development using these instructions, prototype chips and development tools are scheduled this summer, **Fig. 1**.

New surfers often have difficulty locating a desired corporate Web page. It may be possible to deduce a company's web address as 'www.name.com'. When this fails, a search on the company name or trademark usually works.

Alta Vista has introduced a tool called 'Real Name'. It uses a dedicated database of company names and trademarks, which takes the user directly to the Web site having information about the company or product they are seeking.[2]

Fig. 1. Faster clock speeds, the MMX2 additional processor instructions and floating point improvements all provide improved processor power – provided that your applications are designed to take advantage of them.

Microsoft under pressure

As I write, both Microsoft and the Department of Justice are racing the Windows 98 deadline.[3] To attain a 25 June release date, Microsoft needs to ship oem software by 15 May. This puts a deadline on any plans the DoJ might have to resist the release of 98.

Eleventh-hour discussions have taken place, resulting in Microsoft agreeing to hold shipments until Monday the 18th. By the time you read this, the outcome should be resolved.

Microsoft has continued to integrate technology into Windows NT5 that was previously available as third party add-ons. Popular opinion[4] is that NT5 is soon to receive its share of anti-trust attention from the DoJ, **Fig. 2**.

Clean up your hard drive

What has been described by Microsoft as a feature is being hailed by some critics as 'the most destructive software bug in years'. *FrontPage98* users are warned by News.Com[5] that it is possible to designate their entire hard drive as a *FrontPage* file folder. Deleting this folder then wipes the hard drive.

FrontPage's default work folder is placed in the root directory as `c:my_web` making it easy to rename as `c:`. If deleted, this file wipes the disk. Microsoft now recommends users to create 'web' files in a sub-folder and not as part of the root directory of their disk.

While looking for 'Y2k' and 'operating systems' I came across an article entitled 'Auckland – Your Y2k Beta Test Site'.[6] This described the effects that the two month electrical power outages have had on the city of Auckland.

On first reading this piece, I wondered whether the text was pre-Y2k alarmist fiction. Not so. On checking the site of Mercury Energy, the utility company concerned,[7] I found it was only too true. The business centre of Auckland had been seriously affected.

Year 2000 and operating systems

Most advisors agree on the methods you should use to test bios and real-time clock year 2000 compatibility, but advice on operating system tests varies. Some writers believe that operating system Y2k date problems cannot exist, others have identified problems.

Client/Server Technologies Inc[8] has tested PCDos, Windows 3.x, Windows 95, NT 3.5 and 4.0 and several Unix platforms. It identifies six layers, from hardware to application, in which time and date failures can occur.

The company's test results suggest 5% of time and date errors result from the real time clock or bios; the remaining 95% occur at the operating system layer.

Last September IBM[9] issued tables listing year 2000 compliance for each of its operating system products, with 'fix-packs'. For IBM hardware users, this site also suggests appropriate test sequences, according to date of manufacture.

The Microsoft Year 2000 Resource Centre, established in April '98,[10] has a manager for year 2000 solutions and should help resolve your problems. Jason Matuso[11] said, "technically it's a very simple problem to deal with. Only 5% of the world's code has dates in it, but that small piece affects 85 to 95% of the rest of the code," **Fig. 3**.

Most popular operating systems require a patch or fix-pack be installed to ensure year 2000 compliance. My advice is to to download all relevant files before taking any action.

MS-Dos 6.22 is compliant. It will sort files correctly, but cannot display a four-digit year. Additionally the msbackup file does not recognise dates greater than 1999.[10]

Windows 3.1 with Dos 6.22 and an updated version of winfile.exe is compliant, but is still left with unspecified "minor issues". If not updated, file manager shows incorrect dates after 1999. Download W31filup.exe from the Microsoft Software Library to update winfile.exe.[10]

Windows for Workgroups 3.11 with Dos 6.22 and updated winfile.exe is compliant but also with "minor issues". Download WFWfilup.exe from the same library. Similarly, Windows 95 with updated winfile.exe and command.com needs the file win95y2k.exe from the library.

Windows NT 4.0 Workstation with service pack 3 and nty2k.qfe fixes is compliant but again with minor issues. If not updated, User Manager will not recognise 2000 as a leap year so 29 February will not exist. There will also be problems with 'Find File' dates and Office file custom dates. Download service pack 3 and Y2kfixes.asp.

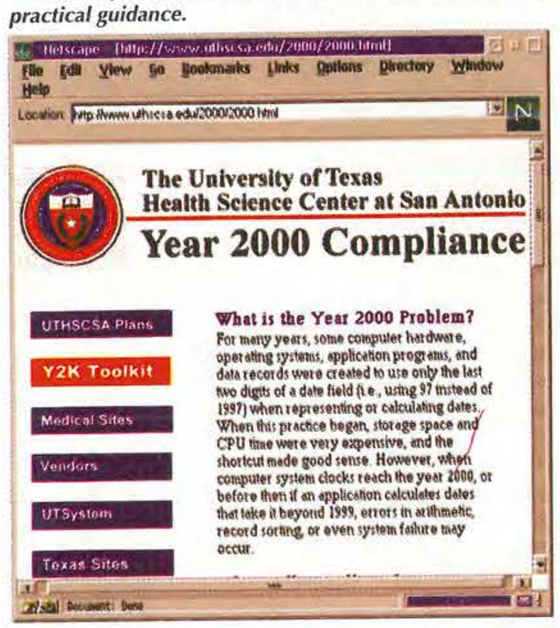


Fig. 4. This site has made good progress towards solving the Year 2000 problem for its internal systems. Visit it to obtain practical guidance.

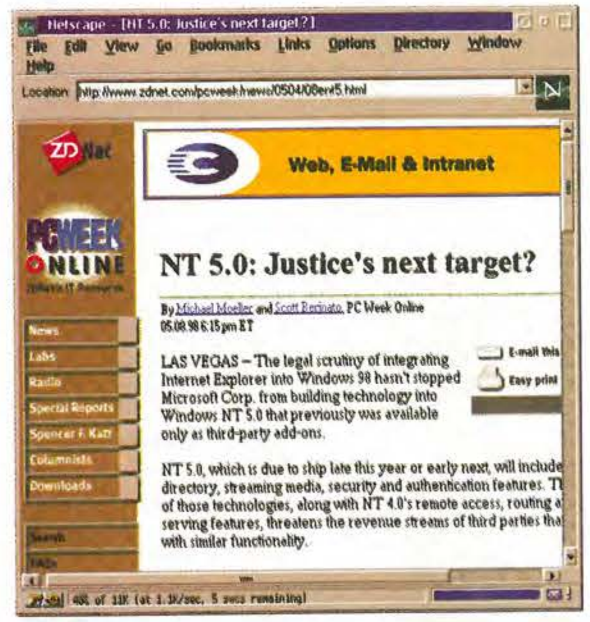


Fig. 2. Recent storms surrounding Windows 98 and Explorer could become overshadowed as Windows NT5 starts receiving attention.

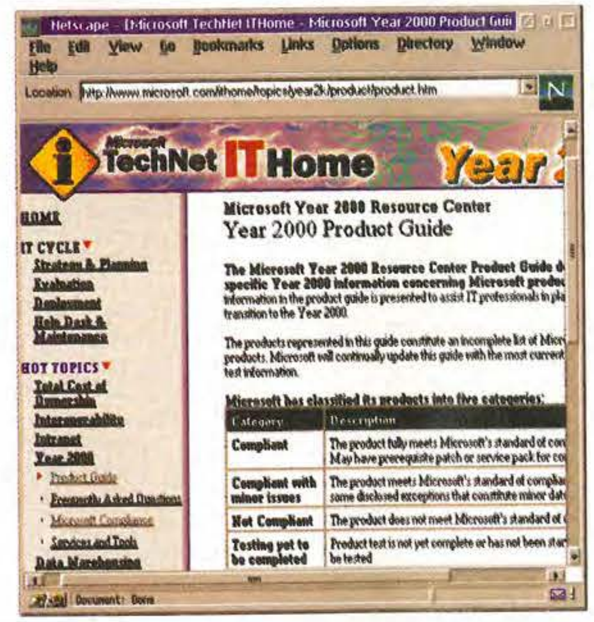


Fig. 3. Better late than never, Microsoft has now organised its Year 2000 support for users.

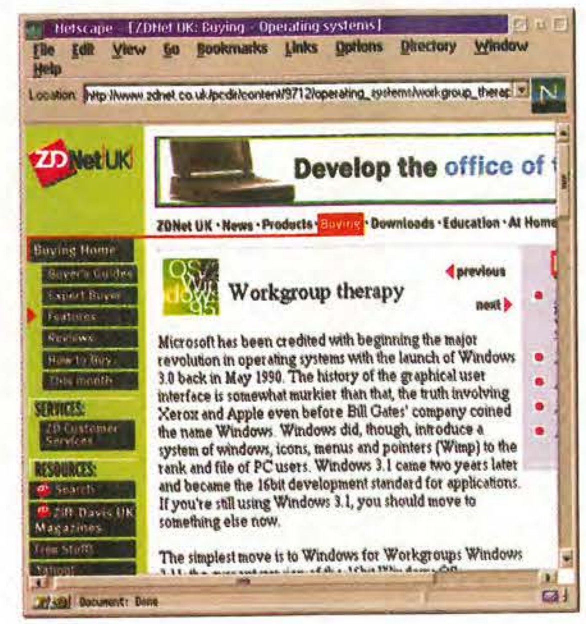


Fig. 5. This operating systems overview is worth reading, whether or not you plan to upgrade your operating system.

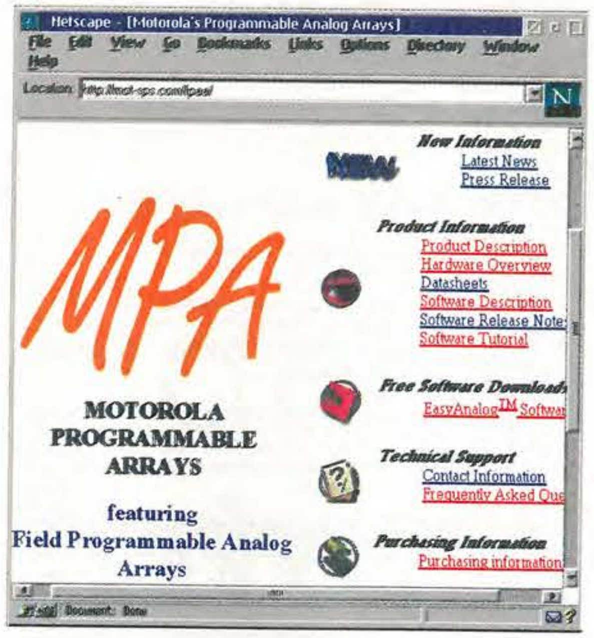


Fig. 6. Motorola's field programmable analogue array has the potential to simplify many analogue circuit designs. Download the manual and FAQ for your introduction to this system.

Microsoft's newest operating systems have a built in workaround that converts a reported year 1900 into 2000. Depending on your machine and its bios, this may not work correctly. In any case, it can only work during year 2000.[12]

According to IBM, OS/2 Warp 4 requires a fix pack,[9] but the Cinderella tests[13] found it compliant. The fix pack is available on request.

Perhaps, like me, you would prefer an independent assessment of your operating system, and be given advice as to whether to upgrade the OS with fixes, or to install a different one.

The aptly named Cinderella project's aim is to provide a simple approach to achieving Y2k compliance for desktop machines, from the very oldest to the very newest.

The Cinderella Community[13] has tested most operating systems and application software, taking care to run the tests on hardware with a bios rollover problem.

One aspect I found particularly useful is that Cinderella has tested current and older operating systems. While Microsoft's year 2000 data assumes you are using Dos 6.22 with Windows, I still use Dos 6.20, so the Cinderella tests using 6.20 were particularly interesting.

The year 2000 site at the University of Texas[14] has a sensible evaluation program and year 2000 toolkit. The site's pages are dated November '97 which may be a slight problem. Alternatively, perhaps UoT used different hardware from that used by Cinderella.

For example the UTHSCSA operating system page reports OS/2 as having no known problem and capable of correcting a bad date at rollover. In comparison, the Cinderella testing reported OS/2 as being compliant but did not correct the real time clock, **Fig. 4**.

It is essential to test all aspects of bios and operating system using your actual hardware. When resetting your real time clock manually to test for rollover, avoid re-setting it too close to 24:00 since test problems when the clock is re-set to 23:59:58 or 23:59:59 have been reported.[15]

Perhaps, like me, you have pondered whether to upgrade your present Windows 3.1 or 3.11 to '98 or NT4. A series of articles under the title "High command"[16] compares the merits of all Microsoft operating systems and OS/2 Warp 4.0 from IBM is valuable pre-reading.

While comparing the benefits of these systems, it also outlines the hardware and application software upgrade implications to be considered when choosing a new operating system, **Fig. 5**.

Before committing to a software and possible hardware upgrade to Windows NT, Windows 95 users are advised to first read a nine page Microsoft article[17]. Some Windows 95 applications used on Windows NT, may not perform as expected.

Those of you already using Windows 95 and planning to upgrade to Windows 98 might find the critique 'Don't pay for Windows 98' in *PC Magazine* by John Dvorak interesting.[18] John complains that because of the number of bugs in Windows 95 and the small number of unique enhancements in Windows 98, it should be free.

Where to surf

1	Katmai prototypes out this summer	http://www.news.com/News/Item/0,4,21917,00.html
2	Alta Vista beefing up	http://www.news.com/News/Item/0,4,21864,00.html
3	Sound and fury surround MS	http://www.zdnet.com/zdnn/content/pcwo/0508/315052.html
4	NT 5.0: Justice's next target?	http://www.zdnet.com/pcweek/news/0504/08ent5.html
5	Feature or bug in FrontPage98 ?	http://www. news.com/News/Item/0,4,21811,00.html
6	Auckland - Your Y2k Beta Test Site.	http://www.kcbbs.gen.nz/users/peterg/power.txt
7	Mercury Energy Co	http://www.mercury.co.nz/index.html
8	Client/Server Technologies Inc.	http://www.com/cst/cstos.htm
9	Network Computing Software Products Y2000	http://www.software.ibm.com/os/dos/year2000/os2cl-w4.htm
10	Microsoft Year 2000 Resource Centre	http://www.microsoft.com/ithome/topics/year2k/product/product.htm
11	The Year 2000 Problem.	http://www.microsoft.com/misc/features.htm
12	PC BIOS Year 2000 Concerns.	http://www.microsoft.com/ithome/topics/year2k/product/pcbios.htm
13	Y2k Cinderella Project.	http://www.cinderella.co.za/cinder.html
14	The University of Texas Health Science Center	http://www.uthscsa.edu/2000/2000.html
15	Robert Hilliards Y2k PC Bios Page	http://www.tyler.net/tyr7020/y2kinput.htm
16	Buying - Operating Systems	http://www.zdnet.co.uk/pcdir/content/9712/operating_systems/workgroup_therapy.html
17	Problems Encountered by Some Windows95 Applications on Windows NT	http://www.microsoft.com/win32dev/guideins/95vsnt.htm
18	Don't pay for Windows 98!	http://www.zdnet.com/zdnn/content/pcmo/0428/310887.html
19	Motorola FPAA	http://mot-sps.com/fpaa/
20	All-digital phase-locked loops	*Electronic Components & Applications* Vol.9 No2
21	Digital Phase-Locked Loop Design SDLA005B	http://www.ti.com/sc/docs/psheets/app_log.htm
22	HCMOS Phase-Locked Loop design Program	http://www-us.semiconductors.philips.com/logic/ftp/Spice/HC-T_4046A_7046A_9046A_Desi/index.htm

Applications

To complement its field-programmable gate arrays, Motorola[19] has introduced a field-programmable analogue array with design software and evaluation kit. Having some facilities in common with the Zetex *TRAC* module recently featured in *EW*, both arrays are complementary rather than competitive.

The *TRAC* module includes log and antilog functions, not available in the Motorola version. Motorola's *MPAA020* module has a 100kHz signal bandwidth and is based on switched capacitor technology. This facilitates the design of sample-and-hold or track-and-hold functions or switched integrators.

Technical information on this module, its FAQ, overview of the design software and a tutorial is available on the Web page. The *EasyAnalog* design software can be downloaded as easyal08.exe, at 2.4Mbyte, and the full design manual as the 1.3Mbyte easyal08.pdf file, **Fig. 6**.

Early phase-locked loop integrated circuits, such as the c-mos 4046 design, used mostly analogue techniques. This old chip, usable at 1MHz and lower frequencies, offered simplified design methods, but was inherently sensitive to change of supply voltage or ambient temperature.

For improved performance unaffected by supply voltage or temperature change, many recent chips use mostly digital techniques. One early all-digital design which extended operation to above 20MHz, the 74HC/HCT297, was described more than 15 years ago.[20,21]

Even faster operation is provided by the Texas *TLC2932* range which reverts to an analogue voltage-controlled oscillator. The pin compatible *TLC2933* extends operation to the 100MHz region, **Fig. 7**.

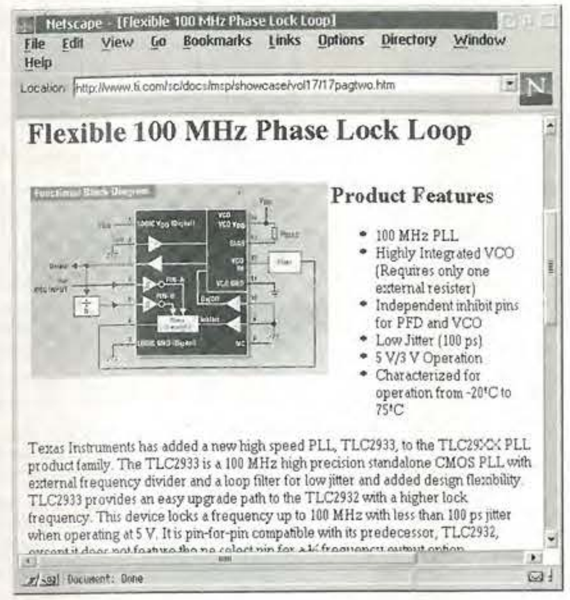


Fig. 7. This new, fast, phase-locked-loop chip uses an analogue voltage-controlled oscillator.

Simulation

One possible difficulty designing analogue phase-locked loop systems with voltage controlled oscillators is component interaction. Repetitive calculations are needed to optimise behaviour.

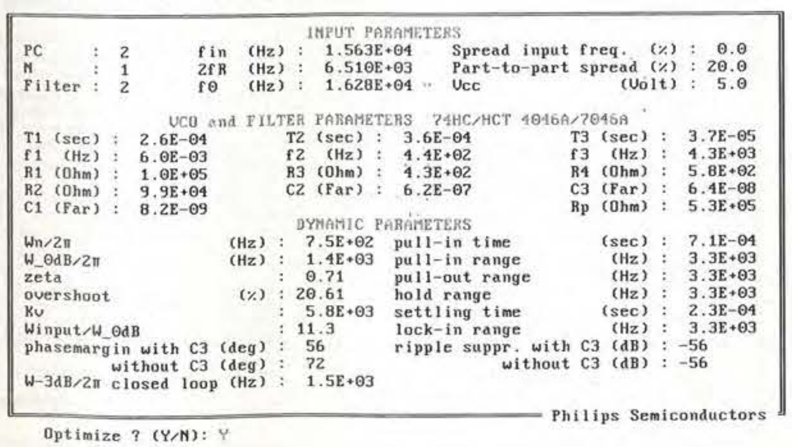
Spice simulations help little, since the required macromodels either do not exist or are elusive. Recently I spent considerable time on-line seeking such models.

To help designers use their 74HC/HCT4046A/7046A chips in 1989, Philips offered a stand alone pll design/calculation program. The original version 1.1, called pll.exe can still be found.

The updated version, 2.0, provides for the 4046A/7046A and 9046A chips and includes Lotus123 spreadsheets that can be used to calculate output frequency for any *R* and *C* combination. Version 2.0 is available by download as pll.zip.[22]

These dos based programs need few resources so run on any pc. Calculated results are quickly tabulated on screen and loop optimisation is provided. If your graphics card is compatible, a bode plot of your designed loop can be plotted to examine loop stability, **Fig. 8**. ■

Fig. 8. A quick and easy 'what if' design method dedicated to Philips phase-locked-loop chips.



LETTERS

Letters to "Electronics World" Quadrant House, The Quadrant, Sutton, Surrey, SM2 5AS

Corner response response

In response to Mr Howard's letter in the last issue, he is of course correct that the absorbent in a transmission line attenuates high frequencies. As a result the waveform shown in my article is technically incorrect and I apologise for that.

However, it is wrong to suggest that the absorbent removes the second step. Steps are used to test loudspeakers because they contain all frequencies. They reveal that the absorbent has no effect on the low frequencies and the double step I described is definitely present; my error is simply that the second step should have been shown somewhat rounded.

It is well known that transmission line, reflex, abr or bandpass speakers add their own footprint to the sound, audible as hangover on percussive material such as the tympanum or bodran, rendering these techniques obsolete for precision applications. The effect is absent on well-engineered sealed enclosures. In other words, to avoid hangover avoid the port.

Mr Howard's misgivings may simply be due to the fact that he has never heard a phase linear aperiodic woofer. The kindest interpretation of his outburst which I can conceive is that perhaps he doesn't listen to live music and so doesn't realise how unrealistic traditional ported loudspeakers sound.

It is wrong to invoke the Haas or precedence effect to suggest that a second pulse 17ms later will be inaudible. The precedence effect relates only to the localisation of a sound source, not to the assessment of its timbre. In any case localisation works best on broadband sounds and is very weak at 30 Hz.

One definition of a linear phase system is that all frequencies take the same time to pass through. When Mr. Howard calculates that some of the output takes 17ms longer than the rest, he is defining the system as phase non-linear. The only compact low-frequency technology which can ever be phase linear is one in which the rear radiation of the cone is completely contained.

It is theoretically possible to feed inverted echoes into a ported speaker so that the echo cancels the port radiation to make a phase linear system. But then, by definition, the port cannot supplant the cone radiation making this a futile exercise.

Mr Howard protests that internal and cabinet edge reflections don't merit a mention. However, I made it clear at the beginning of the section with which he has difficulty that I was considering low frequencies.

The assertion which causes me most concern is that loudspeaker units exhibit minimum phase. In all electrostatic and electrodynamic drive units, the phase response passes through an inversion around the fundamental resonant frequency. In ported speakers this is also true of the air mass at it's own resonance. Every argument he bases on this fallacy must fall down.

Mr Howard is right that the ultimate low-frequency roll-off of a simple sealed enclosure departs from phase linearity, but he accepts that this can be overcome with signal processing. This is, of course, why I stated that sealed enclosures "can be made phase linear" rather than claiming that they were automatically phase linear which would be incorrect.

I stated that large enclosures are unnecessary, but Mr Howard reads this to mean small drive units which is not what I said or meant. In a small sealed enclosure the fundamental resonant frequency of a given woofer rises. If a signal processor is used to return the system roll-off down to the free-air resonant frequency of the woofer, then it will have the same output as it did in an infinite baffle.

Following his misinterpretation, Mr Howard needs to raise the topic of providing enough of what he calls volume displacement. Loudspeaker designers and acousticians use the terms volume velocity and displacement, but these have different meanings.

It is well established that small equalised enclosures can suffer from air non-linearity, but equally there are any number of solutions to that, including feedforward predistortion, motional feedback, the isobaric principle or the simple expedient of making the woofer motor non-linear in the opposite sense.

In his penultimate paragraph there is an argument from the general to the particular which doesn't hold. I agree that some active loudspeakers are poorly engineered, not least due to poor crossover design, but this doesn't mean there is a fundamental problem. I also agree that many passive loudspeakers are designed by bright capable people. What I don't understand is why Mr Howard has neglected the possibility that bright capable people might design active speakers.

Mr Howard refers frequently to what I believe. I should make it clear that in the case of loudspeakers I don't believe anything. I either know or I don't know. If I don't know, I remain utterly silent. I think this where I differ most from Mr Howard.

In my research on loudspeakers I have read in excess of 2000 pages of learned papers. I hold a Master's Degree in sound and vibration. The quality of my loudspeaker research and design is such that I have been invited to write on the topic for this magazine and for *Studio Sound, Sound Pro, Audio Media* and *TV Technology*. I have been invited several times to speak on the subject by the Audio Engineering Society and the Institute of Acoustics and I delivered the Hayden Warren Memorial Lecture in 1996. In the circumstances many of Mr. Howard's remarks are offensive not just to me but the above organisations.

While I welcome informed debate as a way of advancing understanding, we are discussing a technology here and it is utterly inappropriate to personalise it.

John Watkinson, FAES
Burghfield Common

Remote control boost

I was interested in the circuit idea on page 206 of your March '98 issue for an infrared remote control. This is because I recently bought a cheap hifi, with a remote control, which I wanted to operate from an adjacent room.

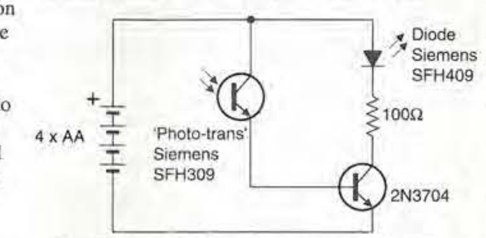
After much playing about with breadboard and oscilloscope I arrived at the circuit shown.

Unlike your contributor I did not have the advantage of an optical filter to block out ambient light, and so the opto-transistor is mounted in a cardboard mask taped to the remote control body and with the transistor directly against the IR window. Of course this does then tie the unit to a pair of wires, but in my application this doesn't matter.

The IR diode is mounted on a wall some 400mm from the sensor in the hifi unit. Note also that no switch is included, since the unit in its passive state take only a few nanoamperes.

From time to time I note that, as in the IR remote control item, your contributors mention that components are available from RS Components. For those of you who do not have access to RS, try Electromail on 01536 201 234.

John Farbrother
Walsall
West Midlands



Simple circuit for increasing the range of output from an infra-red remote control unit.

Satellite first

I've just been reading Arthur C. Clarke's 1945 article again, in which he proposed geostationary communications satellites. What I didn't spot before was this: "While this article was being written, it was announced that the Germans were considering a similar project, which they believed possible within fifty to a hundred years."

Can anyone provide more details?

Andrew Emmerson
Northampton

Please send any information you have to Andrew via Letters, Electronics World Editorial, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS.

Gain-stage investigations

I regret that there was a misprint on page 583 of my article 'Gain-stage investigations' in the July 1998 issue. The theoretical minimum value for the distortion introduced by my notional amplifier should of course, have read 0.0007% [2/2740]%.

John Linsley Hood
Taunton ■

NEW PRODUCTS CLASSIFIED

Please quote *"Electronics World"* when seeking further information

PASSIVE AND ACTIVE COMPONENTS

Connectors and cabling

Fire-resistant fibre. *Easy-Strip+* optical cable from Pinacl Communications Systems will not support a flame, even when attacked by a high-powered propane burner; it does not drip molten plastic as does polyester and will not give off chlorine gas, unlike pvc. Being easy to strip, this 900μ Low-Smoke Zero Halogen (LSZH) buffered cable reduces installation time. The cable sheath is water-resistant and needs no gel barrier. It also bends easily and will not easily kink.
Pinacl Communications Systems Ltd. Tel., 01745 584545; fax, 01745 584780.
Enq no 501

Cable adaptor kits. AMP's *M/A-COM 55009* inter-series adaptor kit for rf work contains a range of interfaces, couplers and cable assemblies in 50Ω and 75Ω impedances, 54 variants including current and obsolete types to provide more than 1300 combinations.
Aerco Ltd. Tel., 01403 260206; fax, 01403 259760
Enq no 502

50-mil pcb connector. Robinson Nugent's *PAK-50* board connector has a pin pitch of 1.27mm and uses a novel type of contact that distributes wear, confers low insertion and withdrawal forces and low contact resistance. There are four types in the range: two-piece board-to-board connectors, low-profile types, surface-mounted and input/output models. A power ground pin at each end of the *PG* units provides 2A/pin of continuous current capability and grounding for static.
Robinson Nugent (Europe) Ltd. Tel., 01256 842626; fax, 01256 842673.
Enq no 503

Discrete active devices

"Smallest" zener. Claimed to be the world's smallest, Rohm's *UDZ TE-17* zener diode series are in UMD2 packages measuring 1.7 by 1.25 by 0.7mm. There are 33 devices in the range, rated at voltages between 2V and 36V. Power dissipation is 200mW and temperature range –55°C to 150°C.
Rohm Electronics UK Ltd. Tel., 01908 282666; fax, 01908 282528.
Enq no 505

Displays

Serial lcd controller. Any liquid-crystal display up to 65ft away from the host may be controlled by Densitron's *SA-PIC* series of RS232 interface cards or stand-alone chips. All control signals for the display are provided over a three-wire line, which controls backlighting, software contrast control and rates to 9600bit/s. Each card will drive one or two displays and a local keyboard with up to 240 keys may be used and data sent along the three-wire interface.
Densitron Europe Ltd., 01959 700100; fax, 01959 700300.
Enq no 506

Large-character lcds. DM Electronics offers the *2002* liquid-crystal display module, which is a yellow-green supertwist type, backlit or reflective. Characters are 9.22mm high and come in formats from 16 by 1 to 40 by 4. All of them have an 8-bit parallel interface and are said to be readable at a distance of 10 feet.
D M Electronics. Tel., 01235 811880; fax, 01235 811889.
Enq no 507

Linear integrated circuits

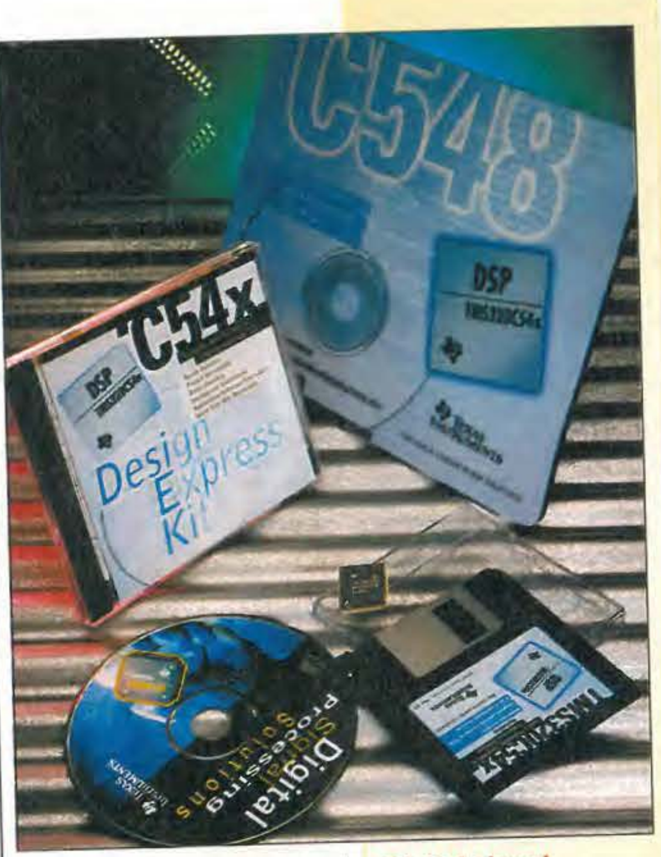
Micropower op-amps. Burr-Brown's *OPA241/251* micropower, single or dual-supply op-amps exhibit a 24μA quiescent current and rail-to-rail output. Input voltage offset is a maximum of ±250μV and common-mode voltage extends 200mV below the negative rail. Both work from 2.7 to 36V or ±1.35 to ±18V, the *241* being meant for low supply voltages and the *251* for the higher range.
Silicon Concepts Ltd. Tel., 01428 751617; fax, 01428 751603.
Enq no 508

Programmable 'trimpots'. *Epads* – electrically programmable analogue devices – are basically dual and quad mosfets, the feature of this new type being that the on resistance may be programmed. *ALD 1108E* and *ALD 1110E* are electrically programmed by the user either before insertion or in-circuit by means of a programmer and adaptor module, the programmed value being stored in the device indefinitely, even after shut-down. These devices work in the 2-10V dc region and may be programmed for a bias of 0.1μA-300μA and from 1-3V in 0.1mV increments. Positive and negative temperature coefficients are exhibited, with zero at 68μA; drift over ten years is less than 2mV.
Steatite Insulations Ltd. Tel., 0121 678 6888; fax, 0121 683 6999
Enq no 509

Silicon delay lines. Maxim has produced silicon delay lines in the *MXD1000/1005/1013* family as direct second-source components for the Dallas *DS* units. *MXD1000/1005* have five equally spaced taps to give delay from 4ns to 500ns to 3% or ±5%, while the *MXD1013* has three independent lines of equal length for delays of 10ns to 200ns, each output coping with up to ten 74LS loads. Voltage supply is 5V at around 20mA and the devices are in μMAX 8-pin packages, which are half the size of the 8-pin SO.
Maxim Integrated Products UK Ltd. Tel., 0118 9303388; fax, 0118 9305577.
Enq no 510

Logic

Low-resistance mux/demux switches. Fairchild's FST family of multiplex/demultiplex switches is extended to include the *FST16232/3* 16-32bit devices. This type of logic element enables separate signal paths to be combined into or separated from a single path, R_{on} and propagation time being critical; in this case around 4-11Ω (typical) and under 10ns, depending on conditions. The *16233* is a dual type to allow one 16-32 or two 8-16 multiplexers to be formed on two buses. Both devices are compatible with cmos ttl logic.
Fairchild Semiconductor Corporation Web site: http://www.fairchildsemi.com. E-mail: logic.europe@fairchildsemi.com
Enq no 511



Digital signal processors

C54x evaluation kit. A *Design Express Kit* is available for the Texas *TMX320LC548* digital signal processor, which runs at 100Mips. It contains application software, training and data on a cd-rom, a sample chip and applications guides. The *C548* has 32Kword of ram and 16Kword of rom, which allows the integration of functions normally performed by several dsps. There is a 4Mword address space, so that the device is able to adapt itself in operation to run a variety of software. It has a host port interface, a tdm serial port, a timer and two buffered serial ports
Arrow-Jermyn. Tel., 01234 270027; fax, 01234 214674/791501.
Enq no 504

Materials

Getters for semiconductors. Hydrogen and moisture getters by Allied-Signal Inc for hermetically sealed semiconductor packages are available in the UK from Alpha. This

material takes up moisture and the hydrogen leaching in most types of semiconductor material, which would otherwise poison the device. The getters come as cast or moulded preforms in a range of standard sizes or as paste in syringes and tubs. *Alpha Metals. Tel., 0181 6656666; fax, 0181 6654734.*
Enq no 512

Microprocessors and controllers

Extended *M16C* range. *M16C* microcontrollers by Mitsubishi are now faster and the range has two new types: the *M16C/62* and *MC16C/61A*. The 61A is an improved 61 and gives true 16MHz zero-wait performance and a 62.5ns instruction cycle time. There are now three single-channel serial i/os for usart or clock-sync.operation, one of them supporting subscriber interface module needs for smart cards and mobiles, and eight 16-bit timers. Power requirements are as little as 3V at 18mW. The *62* is a new version of the *60, 61* and *61A* with three more timers, two extra serial i/o channels and 4Mb addressing. It may be arranged to control a three-phase motor, including dead-time generation, and will generate a pwm waveform based on triangular or sawtooth modulation. Interference immunity is such that there is no malfunction in the presence of 20kV static discharge. *Mitsubishi Electric UK Ltd. Tel., 0990 134275; fax, 0171 3517633*
Enq no 513

Motors and drivers

Dc motor control. *VHFD* dc motor control modules by IXYS save space and reduce assembly cost. They are single-phase, half-thyristor bridge types with a separate free-wheeling diode and a separate diode bridge for field current. There are three members of the family to provide currents of 16A dc to 37A dc at a base-plate temperature of 85°C. Voltage ratings are 800-1600V ac, so that 240-575V mains can be accepted. *GD Rectifiers Ltd. Tel., 01444 243452; fax, 01444 870722.*
Enq no 514

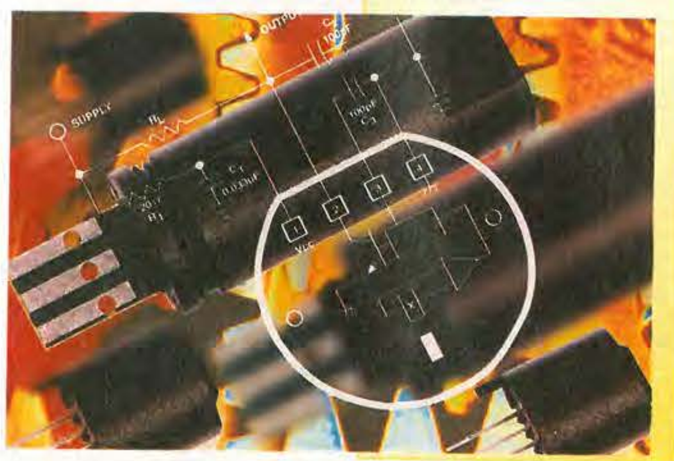
Optical devices

Uncooled laser diodes. Mitsubishi has an uncooled laser diode, which performs as a cooled design but at lower cost. The *FU-436SDF-4M1B/C*, which are distributed-feedback modules with built-in optical isolators, are meant for use in catv networks and mobile telephone systems. Both provide constant power up to temperatures of 85°C to within 0.3dB; distortion and noise are low. Central wavelength is 1290-1330nm, optical power 2.5mW, or 4mW max. The *M1B* is for front-panel mounting and the *M1C* for board use. *Mitsubishi Electric Semiconductors. Tel., 01707 276100; fax, 01707 278837.*
Enq no 515

Oscillators

Ovened crystal oscillators. Oven-controlled crystal oscillators from C-MAC maintain stability to an order of magnitude better than the Stratum III requirement should the external reference fail; *CMO5000* units also show whether the oven has failed. The whole device is contained in a 36 by 27 by 13.5mm and is stable to within 0.03ppm over the –10°C to 70°C range without the reference. Frequencies available include 33.88MHz and 51.84MHz and power requirement is 9-20V dc at 400mA during warm-up and 120mA steady at 12V. Ageing is less than 0.35ppm over 20 years and overall stability is within 0.51ppm. Tuning by voltage is ±12ppm. *C-MAC Quartz Crystals Ltd. Tel., 01279 626626; fax, 01279 454825.*
Enq no 516

Very small photosensors. Matsushita's *UZB* integrated photosensor is claimed to be the smallest available at 14.5 by 10 by 3.5mm. Light-on or dark-on through-beam types provide a 500mm range in front and side sensing versions, the slit mask provided allowing the detection of objects down to 1mm diameter. A further, fixed-focus type senses in the 2025mm range and will detect objects of 0.1mm diameter. All are independent of the colour of the object and respond in 0.5ms. Voltage needed is 12-24V dc. *Matsushita Automation Controls Ltd. Tel., 01908 231555; fax, 01908 231599.*
Enq no 525



Passive components

H-v multilayer capacitors. High-voltage, multilayer, ceramic capacitors from Semtech come in values from 100pF to 470pF at voltages to 10kV and may be mounted in chip form or as epoxy-dipped leaded types through-hole. Maximum temperature is 200°C. *Advanced Power Components Ltd. Tel., 01634 290588; fax, 01634 290591.*
Enq no 517

Disc capacitors. Dubilier's *WD2Y* high-voltage capacitors are approved to EN 132400 and IEC 384-14 (2nd). They are meant for ac work and possess limited capacitance to reduce the possibility of high current when alternating voltage is applied. Rated voltage is 250V ac and dielectric strength 4kV ac for 60s. Capacitance is in 10% and 20% values between 100pF and 10nF. Connected between phase and neutral, the capacitors are suitable to filter common-mode emi. *Dubilier Ltd. Tel., 01371 875758; fax, 01371 875075.*
Enq no 518

Common-mode chokes. A range of surface-mounted common-mode chokes for rfi suppression is offered by Vacuumschmelze. They are in the compact 5024 package and provide inductance in the 1-120mH range at up to 600mA.; the company's other family of chokes are in the 5032 package and are in values from 1 to 70mH. *Vacuumschmelze GmbH. Tel., 0049 61 81/38-26 29; fax, 0049 61 81/38-28 60.*
Enq no 519

250V ac chip capacitors. Murata's *GHM2000* series of surface-mounted ceramic capacitors are rated to 250V ac to provide mains input decoupling and suppression. Various national and international safety standards are met, including IEC384-14, and the capacitors cope with machine placing and wave soldering. They are available in forms for connection across live and live/neutral to earth and in values from 10nF to 100nF and 470pF to 4700pF respectively. Temperature range is –25°C to 85°C, but the *GHM3000* series offers –55°C to 105°C in values from 100pF to 33nF. *Surtech Distribution Ltd. Tel., 01256 840055; fax, 01256 479785*
Enq no 520

Power semiconductors

40V Schottkys. *RB060L-40* and *RB160L-40* are high-frequency Schottky barrier diodes in the epitaxial planar construction, having a forward current of 1A and maximum forward voltage drops of 0.4-0.55V; mean rectified current is 2A for the *060* and 1A in the *160*. Both show a maximum forward surge of 70A and leakage is typically 5μA at 40V/25°C. These devices are contained in a 5 by 2 by 2.6mm surface-mounted package. *Rohm Electronics UK Ltd. Tel., 01908 282666; fax, 01908 282528.*
Enq no 521

Resettable fuses. Resettable polymeric fuses in Schurter's *RA Series are* drop-in replacements in many cases and are made from a plastic material that is a mixture of carbon black and a non-conductive crystalline polymer in thin sheets. This material conducts to a given temperature and becomes a virtual insulator until the fault is cleared, whereupon it once again conducts. These devices may be tailored to requirements in resistance and tripping time and ageing is ±5% change in resistance over 1000h at 85°C and 85% relative humidity. Change after ten thermal cycles is ±10%. Various mounting options are offered for the radial-leaded devices. *Radiatron Components Ltd. Tel., 01784 439393; fax, 01784 477333.*
Enq no 522

Protection devices

Moisture indicators. Brownell's range of *moisture controller/indicators* mount on panels and enclosures. They possess a visual panel in two halves, both being blue when desiccant is active and relative humidity under 30%, blue and pink when it is partly saturated and pink when it needs replacement at 50%. The units are filled with either silica gel desiccant, which may be re-activated, for those applications where adsorption is slow, or with molecular sieves for 15/30% relative humidity. These cannot be re-used. *Brownell Ltd. Tel., 0181 9659281; fax, 0181 9653239.*
Enq no 523

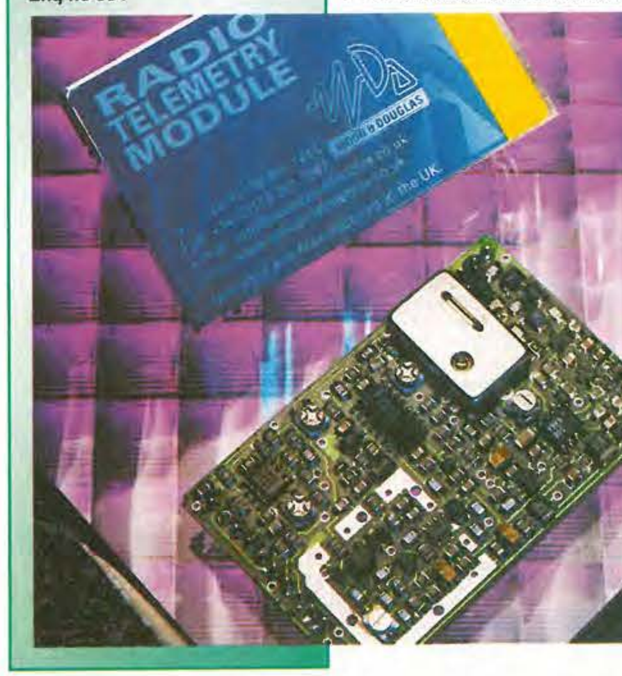
Switches and relays

Photovoltaic relay. Consisting of a two-pole, normally open solid-state relay and a ring detector in one package, the *PVO402P* photovoltaic relay by Solid State Supplies replaces a relay and ac-input opto-coupler, yet is still only 5mm thick and is suitable for use with Type II PCMCIA fax/modem cards. The relay uses a Hexfet output device, the output switch being activated by a gallium aluminium arsenide led. Input/output isolation is 3750V rms. Packaging is an 8-pin moulded dip with gull wing s-m pins. *Solid State Supplies Ltd. Tel., 01892 836836; fax, 01892 837837.*
Enq no 524

Transducers and sensors

Gear-tooth sensors. A range of Hall-effect magnetic gear-tooth sensor assemblies in Allegro's *ATS632* series provides accurate tooth-edge detection in large-pitch ferrous gears. They possess a self-calibration facility and may be installed in any plane to work with a variety of tooth forms. Signal processing includes self-calibrating, 6-bit a-to-d converters, whose thresholds adapt to the peak-to-peak signal to maintain switching accuracy. Detection at zero speed does not exhibit the jitter normally found in the digital circuitry normally used for this purpose. Sensors are available in a stand-alone cylindrical package or as board-mounted devices. *Allegro MicroSystems Inc. Tel., 01932 253355; fax, 01932 246622.*
Enq no 526

Telemetry transmitter. Wood & Douglas has a synthesised transmitter module for 430-470MHz radio telemetry, having the stability of a crystal-controlled unit but with 128-channel frequency control. The *ST500*, approved to ETSI 300 220, is meant for short-range, data transmission and telemetry in low-cost, high-volume work such as alarms, monitoring and security. It is in a board-mounted nickel-silver enclosure, frequency being programmed by a serial or parallel interface and stored in non-volatile memory to eliminate the risk of loss when the unit is turned off. Output power is adjustable from 10mW to 100mW and switching bandwidth is 5MHz and analogue or digital input. *Wood and Douglas Ltd. Tel., 0118 9811444; fax, 0118 9811567.*
Enq no 534



Position sensors. Schaevitz has a newly developed position sensor, in the shape of the *HCT 420* linear variable differential transformer, which contains all signal-conditioning circuitry in its 0.75in diameter stainless steel, hermetically sealed, tubular housing. It operates with a 4-20mA two-wire system with loop resistance to 700Ω at 28V dc. The housing withstands pressures to 70bar and temperatures from –25°C to 85°C and may be used with long cables, being designed for use in noisy areas. *Lucas Control Systems Products. Tel., 01753 537622; fax, 01753 823563.*
Enq no 527

EQUIPMENT

Cameras

Memory cards for cameras. Premier Electronics has a range of PCMCIA memory cards for digital cameras ranging in capacity from 2Mbyte to 520Mbyte. The four styles, compact and miniature Flash, Smart Media, ATA flash and pc card hard drives are available, all with high-speed buffers for rapid downloading; users without a PCMCIA socket can use an adaptor. Built-in software in adaptors interfaces the camera output to a pc. *Premier Electronics Ltd. Tel., 01922 634652; fax, 01922 634616.*
Enq no 528

Power supplies

Dc-to-dc converter evaluation. A design and evaluation kit from Newport helps development and testing of distributed power supplies using converters in the company's *NPH* family rated at 10-25W. Users are able to evaluate and modify input, output and common-mode noise performance to suit and, the sync. pin being accessible, to alter frequency and implement a shut-down feature. A potentiometer is supplied for the voltage trim pin. Kits contain a converter, noise filter components, fuse, reverse protection diode and terminals and the Newport cd-rom with application notes. *Newport Components Ltd. Tel., 01908 615232; fax, 01908 617545.*
Enq no 529

Money-saving ups. By using the *Silcon E* series of uninterruptible power supplies by Universal Power Systems, it is claimed that Lloyd's Bank is saving more than £200 000 per year. High efficiency is obtained by a patented single-conversion technique, in which power is converted only once while charging the batteries, instead of being converted to charge the battery and back again to run the equipment. A cd-rom to indicate the potential savings to be obtained is available. *Universal Power Systems Ltd. Tel., 01509 261100; fax, 01509 261148.*
Enq no 530

800W, multi-output supply. XP's *MVP* series of power supplies is now made in an 800W version, the *MP8* model having up to twelve outputs arranged to users' requirements; from over a million combinations of outputs from a standard power-factor-corrected front end, you can have a tested unit in two or three days. The standard front end drives up to six output modules in single, dual or triple form. The *MVP* series complies with standards of harmonic distortion and conducted and radiated emi; there is current sharing on outputs with 10A or more ratings, remote sensing on outputs of 2A or more, overload and overvoltage protection, short-circuit protection and auto recovery. Efficiency is 70-80% at full load and ripple 0.1% or 10mV. *XP plc. Tel., 0118 9845515; fax, 0118 9843423.*
Enq no 531

Plug-top dc power. *PWS Series* plug-in supplies by Arlec provide low-voltage dc power from 110-230V ac mains, complying with European standards, including the CE emc mark. Two models are available: the *PWS120-400* giving 2.5-12V dc at 400mA and the *PWS120-900* for 3-12V dc at 900mA. Both types are adjustable by a slide switch, which may be covered by a nameplate after setting, and the cases are double-insulated, the primary/secondary transformer isolation being 4kV. There is overload and short-circuit protection and the units have a 2m lead with a connector taking a variety of plug types. The mains plug is available in all pin configurations. *Arlec Power UK Ltd. Tel., 01582 544520; fax, 01582 544521.*
Enq no 532

250V audio mosfets. Specialist audio semiconductor distributor Profusion has samples of Exicon's new 250V, 8A power mosfets. The n-channel *ECFION25* and p-channel *ECFIOP25* are complementary, offering audio amplifier designers the ability to produce power outputs of 1750 watts into 4Ω – or more than 3000W in bridge mode. Slew rate is greater than 100V/μs and total power dissipation is 125W. Packaging is TO3 "at present." Demonstration amplifier modules are available on request, together with application notes. *Profusion, Tel., 01702 543500, fax 01702 543700.*
Enq no 551

Radio systems

SRD devices. The band for short-range devices (SRD) is now approved by most countries in Europe and RF Monolithics has a range of components and modules for this 868-870MHz band, including surface-mount resistors, resonators, *CR* filters and Tx/Rx modules. These frequencies are intended for low duty-cycle use such as garage-door openers, permitted output power being 25mW, and less interference from amateur radio and other sources is expected than was experienced in the 418MHz and 433.92MHz bands. Receiver modules on offer use the amplifier-sequenced technique, which gives a sensitivity of –100dBm without the use of heterodyne oscillators or regen. circuitry and with no use of frequency changing. *Acal Electronics Ltd. Tel., 01344 727272; fax, 01344 424263.*
Enq no 533

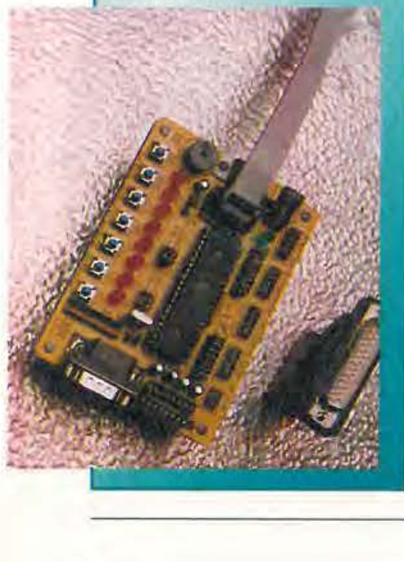
Please quote *"Electronics World"* when seeking further information

Test and measurement

Arbitrary function generators. *AFG300/310* are function and arbitrary waveform generators that will transfer waveforms straight from a digital storage oscilloscope, the *310* being a single-channel instrument and the *300* dual-channel. In this way, signals produced by electrical, mechanical or medical processes may be captured by the dso and transferred to these instruments by GPIB interface for further study and simulation. Both are for frequencies less than 16MHz, standard outputs being sine, square, triangle, pulse and the arbitrary function, which has a 16Msample/s internal clock, 8MHz output and 12-bit vertical resolution. *WaveWriter* software included is a Windows package for simple waveform creation.
Tektronix UK Ltd. Tel., 01628 403300; fax, 01628 403301.
Enq no 535

Development and evaluation

8051 development. Kanda's 8051 Workshop is a complete development system for 8051 projects and contains a restricted (2K of code, but upgradeable) IAR C compiler, an application board with ICE functions and a device programmer. Windows software supplied includes Application Builder for rapid code generation and automatic setup of on-chip peripherals; the IAR assembler, which allows unlimited source code size, is included. Also on the board are all the leds, switches and sound needed, as well as an RS 232 port. Included is the Atmel 89S53 in-system programmable flash device supporting most eprom and otp 8051 variants.
Radiatron Components Ltd. Tel., 01784 439393; fax, 01784 477333.
Enq no 542



Conductivity meter. Instead of using a forced current and measuring a very small voltage across a sample, YSI's *YSI 3200* conductivity meter compares the unknown resistance to a calibration resistor in the instrument, with a consequent increase in accuracy. The system is versatile, in that it is also able to measure salinity, temperature, resistivity and total dissolved solids. Control is by microprocessor and there are various options of linear or non-linear temperature compensation, data storage and logging. *YSI UK Ltd. Tel., 01252 514711; fax, 01252 511855.*
Enq no 536

Waveform monitor. Leader's *L1500* waveform monitor for analogue component television or hdtv signals has been reduced in price while being improved to comply with CE standards. It measures the level and phase of a component signal or the level of a composite input, the waveform of a signal, the vector of a component or the timing of an analogue component.
Thurlby Thandar Instruments Ltd. Tel., 01480 412451; fax, 01480 450409.
Enq no 537

Digital micro-ohmmeter. Having a measurement range of 600μΩ-60Ω to a resolution on the lowest range of 0.1μΩ, the *Cropico DO7* is contained in an ABS case and takes power from the mains or from an internal rechargeable battery, which lasts from 1hr to 20hr, depending on the range. A 4-digit led display has automatic point and polarity indication and protection to 415V rms at the input. RS-232 output is provided, as a socket for the connection of a remote start control such as a foot switch.
Feedback Test and Measurement. Tel., 01892 653322; fax, 01892 663719.
Enq no 538

COMPUTER AND DATA HANDLING

Computers

Twin-Pentium II board. New from Texas is the *P2000 (D) FX* series of single-board computers that comes with either one or two 266/300MHz Pentium II with 512K cache, anticipating the future needs of 32-bit image processing, process control and computer telephony. The boards contain the Intel 440FX chipset and have provision for up to 512Mbyte of dimm memory modules. There is an extensive set of i/o interfaces for floppy disk, enhanced IDE and up to 15 SCSI devices; data transfer rates on the PCIbus extend to 16.6Mbyte/s. As standard, there are two serial ports and a Centronics-compatible enhanced parallel capabilities port. A passive backplane is available.
Texas Microsystems UK Ltd. Tel., 01344 886600; fax, 01344 886650.
Enq no 539

Computer board-level products

10Msample/s a-to-d card. *CompuScope 1016* is an IBM-compatible ISAbus card that will perform 16-bit conversion at up to 10Msample/s in one channel with a 5MHz bandwidth; spurious-free dynamic range is 85dB. Digital data, up to eight million samples of it, is stored on the board itself for later reading by the pc without the need for GPIB or IEEE488 interfaces, data being transferred to a Pentium pc's extended memory using software drivers. Software supplied allows the card and pc to be used transparently as an oscilloscope with no need for any programming.
Strategic Test and Measurement Systems Ltd. Tel., 0118 9795950; fax, 0118 9795951.
Enq no 540

Data acquisition

PCI data acquisition. *PCI-DAS 1200* by ComputerBoards is a data acquisition board for the pc, having 16 single-ended or eight differential analogue inputs and two analogue outputs to 12-bit resolution and 24-bit digital i/o; gain error is within 0.02% over all input ranges. The 330kHz a-to-d uses a precision reference voltage and automatically trims input offset, calibrating itself in the field. The company's programming library supports the board and there are drivers for Hewlett-Packard HP-VEE and LabView.
Adept Scientific Micro Systems Ltd. Tel., 01462 480055; fax, 01462 480213.
Enq no 541

Interfaces

SCSI terminators. *BH9595FP-Y* and *BH9596FP-Y* by Rohm are low-power SCSI terminators to replace resistors in SCSI-I, II and the fast III standard. They contain 18 terminations in one ic and give a complete termination for V_m at 2.85V to ground and V_m to V_{DD}. Operating from 5V dc, they have a standby mode to reduce power when the devices are not in use, being controlled by an enable signal. The *9595* has active high enable and the *9596* active low.
Rohm Electronics UK Ltd. Tel., 01908 282666; fax, 01908 282528.
Enq no 543

Software

Power and control simulation. Cambridge Control, now owned by The MathWorks Inc, offers *Power System Blockset* – a software package that allows the modelling and simulation of power and control systems. When used with *Simulink*, Cambridge's modelling tool, the program provides graphical representations of power systems. It is claimed to be the first tool to predict the effect of combining electrical equipment and system designs with existing mechanical and thermal systems.
Cambridge Control Ltd. Tel., 01273 722838; fax, 01273 720550. http://www.camcontrol.co.uk
Enq no 544

PUBLICATIONS

Conductive gels. Raychem has a new brochure on its *HeatPath* range of gels for thermal management, containing application information, specifications and ordering procedure and explaining the performance of gels in comparison with pads, grease and adhesives.
Raychem Ltd. Tel., 0800 968626; fax, 0800 968627.
Enq no 545

Digital panel meters. Detailed data sheets and application notes on Datel's digital panel meters are given in a new 128-page data book.There are more than 200 general-purpose dpms in various forms, including those in dip packages and self-powered, two-wire models, and a number of new process-control monitors. Adaptors to convert the instruments for measuring high inputs and ac measurement and to adjust gain and offset plug into the back. Eighteen application notes describe various methods of using the dpms and there is advice on the practical side – avoiding ground loops and the like.
Datel (UK) Ltd. Tel., 01256 880444; fax, 01256 880706.
Enq no 546

Liquid-crystal displays. A new edition of NEC's catalogue of tft colour lcds is available on cd-rom. There is a growing range of large – up to 51cm – high-resolution 1280 by 1024 models for desk-top monitors that are said to be meant to oust the crt from such applications, particularly for mid and high-performance work.
NEC Electronics (UK) Ltd. Tel., 01908 691133; fax, 01908 670290.
Enq no 547

R & S spectrum analyser. A brochure from Rohde & Schwarz is intended to assist users to write control programs for the spectrum analysers in the *FSEx* and *ZVRx* families. It contains a section each on the IEEE 488.1 and 488.2 and SCPI, advice on the selection of IEC/IEEE-bus card, a description of controlling bus and devices from the programming language and applications of the FSE analyser.
Rohde & Schwarz UK Ltd. Tel., 01252 811377; fax, 01252 811447.
Enq no 548

Lans and wans. *Minitran's* 1988 catalogue of lan and wan equipment shows many additions to the range in the area of enclosures, trunking and associated hardware and, in particular, to the range of active networking products – hubs, switches, repeaters, routers and wireless lan equipment, including the company's own *MINI 5* range.
Minitran. Tel. and fax, 01279 757775.
Enq no 549

Programming silicon floppies

Pei An illustrates how easy it is to program Toshiba's new silicon alternative to floppy disks – SmartMedia.

The *SmartMedia* solid-state floppy disk card, or ssfdc, is a new-generation flash memory card developed and proposed as a standard by Toshiba. It is a removable storage medium best suited for use in portable information storage applications.

Applications of the technology include digital cameras, voice message recorders, musical instruments, potable digital assistants (pdas) and stand-alone data acquisition systems.

These memory cards are very small, measuring 45.0mm by 37.0mm by 0.76mm, and they weigh 2 grams, **Fig. 1**. They incorporate advanced Nand-type flash memory chips to provide 2, 4 or 8Mbyte non-volatile memory capacity. Each memory location can be written and erased over 1000000 cycles.

A single 5V or 3.3V power supply is needed. In the standby mode, the memory disks consume 100µA current. While reading, erasing and programming, current consumption is below 40mA.

There is a control set consisting of 11 commands for selecting various operations such as erasing, programming, reading data and resetting, etc. Each disk connects to external circuits via eight data/address i/o lines and five control lines. Commands, addresses and data are written into the device using a serial input/output scheme.

Available SmartMedia memory disks from Toshiba are shown in **Table 1**.

I have designed and built a programmer and reader for the *TC5832DC SmartMedia* disk. It connects to the Centronics port of a computer via a standard printer cable.

A special socket on the programmer allows the *SmartMedia* disk to be inserted. The complete system is illustrated in Fig. 2.

I have also developed a Dos Turbo Pascal 6 driver to demonstrate how the disk is erased, programmed and read.

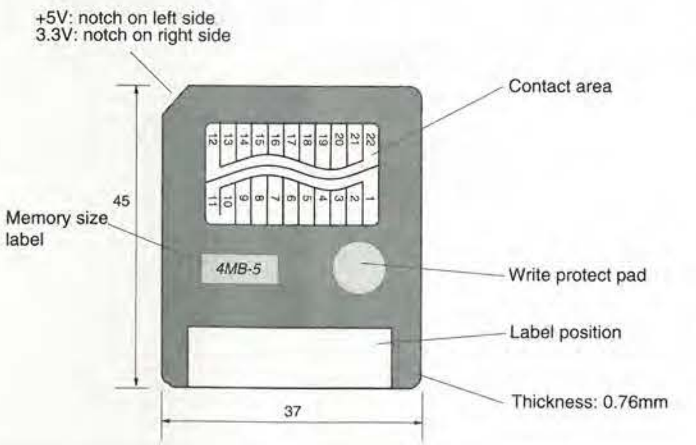


Fig. 1. The Toshiba SmartMedia solid state floppy disk card, or ssfdc, measures 37mm by 45mm by 0.76mm and weighs only 2g. Available memory sizes are 2Mbyte, 4Mbyte and 8 Mbyte. 5V and 3.3V versions are available.

Table 1. Available SmartMedia ssfdc products.

Product	Memory density (Mbyte)	Voltage (V)	Program time (µs/byte)	Erase time (ms)	Access time (ns)	Write/erase cycles
TC5816BDC	2	5.0	1.2	6	80	250000
TC5832DC	4	5.0	0.6	6	50	1000000
TC58V16BDC	2	3.3	1.2	6	80	250000
TC58V32DC	4	3.3	0.6	6	50	1000000
TC58V64DC	8	3.3	0.4	6	50	1000000

What is a *SmartMedia* silicon disk?

The *TC5832DC* is a single 5V Nand electrically erasable and programmable read only memory, or Nand eeprom. Its capacity is 33Mbit.

Pin functions of the device are shown in **Fig. 3**. The eight i/o pins and five control lines allow an external circuit to control all the operations of the memory disk. A *SmartMedia* disk socket holds the disk. Pin connections of the socket is also shown in Fig. 3.

Internal functions and memory organisation of the device are given in **Fig. 4**. The memory is organised as 528 byte by 16 pages by 512 blocks. A page consists of 528 bytes of which 512 bytes are main memories and 16 bytes are redundant memories.

One block has 16 memory pages. There are 512 blocks inside the device. To access to a particular byte in a 4Mbyte memory space, 22 address lines, $A_{0\text{-}21}$, are required. The nine bits $A_{0\text{-}8}$ determine a byte on a page. Lines $A_{9\text{-}12}$ specify the particular page in a block and $A_{13\text{-}21}$ specify the block.

Note that the erase operation of the device is carried out only in a block – 16 pages, 8Kbyte in one go – and the program operation is carried out in a page, which is 528 bytes in one go.

The device has 528 byte static registers. These act as data buffers between the external circuitry and the memories.

How it works

The *TC5832DC* responds to 11 commands for its various operations, as outlined in **Table 2** on page 705.

Now I will show how some of these commands are used in erasing, programming and read data operations.

The timing sequence for the erasing operation is shown in **Fig. 5**. To enter the erasing operation, the memory disk is enabled by taking the chip-enable pin low. Then the command-line-enable pin, CLE, is set high and address-line-enable ALE is set low. This informs the memory disk that a command is to be sent to it.

Next, the erase command byte 60_{16} is placed on the i/o lines and a high-to-low-then-high pulse is applied to the write line –WE. At the low-to-high transition of –WE, the command is latched into the memory disk. After this, a two-byte block address is written into the device.

The CLE line is set low and ALE is made high to indicate that the next data to be trans-

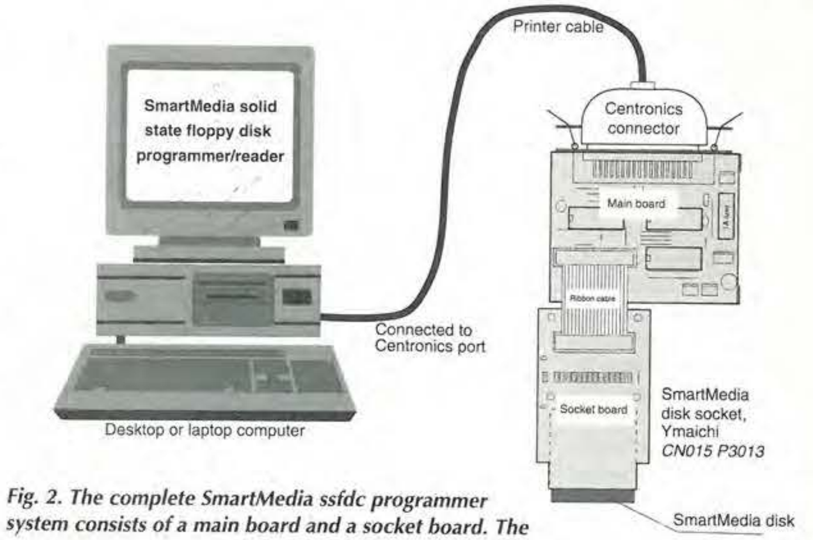


Fig. 2. The complete SmartMedia ssfdc programmer system consists of a main board and a socket board. The programmer is connected to a pc via a standard printer cable. A Dos Turbo Pascal 6 software demo driver has been developed for the programmer. Note that this programmer can only be used for 5V ssfdcs.

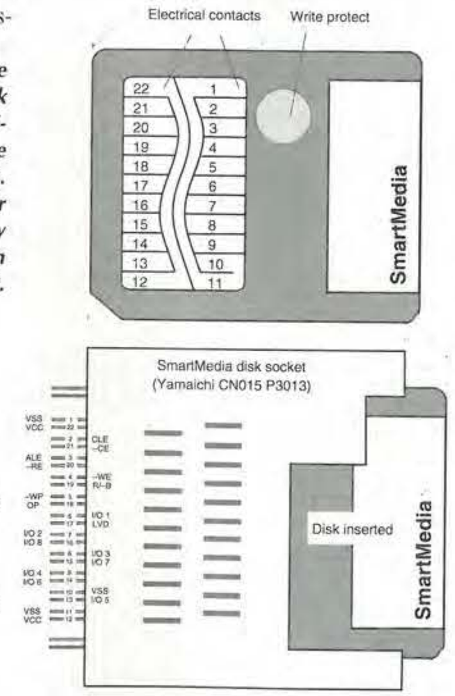


Fig. 3. Pin-out and pin functions of the TC5832DC ssfdc and its Yamaichi disk holder. The memory card has an 8-bit bi-directional data bus – $I/O_{1\text{-}8}$. There are five control lines, –WE, –WR, CLE, ALE and –CS). Line R/–B indicates if the device is busy or ready. OP selects the number of memory locations in a page. The write protection signal is –WP.

Pin functions

1	VSS	Ground
2	CLE	Command Latch Enable. High to indicate a command is on the i/o1 to i/o 8 lines
3	ALE	Address Latch Enable, high to indicate an address is on the i/o1 to i/o 8 lines
4	WE	Write Enable. Data on the i/o1 to i/o 8 written into disk at low-to-high edge
5	–WP	Write Protect activated when low
6	I/O 1	Bidirectionalal i/o port DB0
7	I/O 2	Bidirectionalal i/o port DB1
8	I/O 3	Bidirectionalal i/o port DB2
9	I/O 4	Bidirectionalal i/o port DB3
10	VSS	Ground
11	VSS	Ground
12	VCC	Power supply (+5V for +5V devices or +3.3V for +3.3V devices)
13	I/O 5	Bidirectionalal i/o port DB4
14	I/O 6	Bidirectionalal i/o port DB5
15	I/O 7	Bidirectionalal i/o port DB6
16	I/O 8	Bidirectionalal i/o port DB7
17	LVD	Low voltage detect
18	OP	Option Pin. OP=GND: 528 memories on a page, OP=VCC: 512 memories on a page
19	R/–B	Ready/busy. Open collector output
20	–RE	Read Enable. At high-to-low edge, the device outputs data
21	–CE	Chip Enable. For all operations, this pin must be low
22	VCC	Power supply same as pin 12

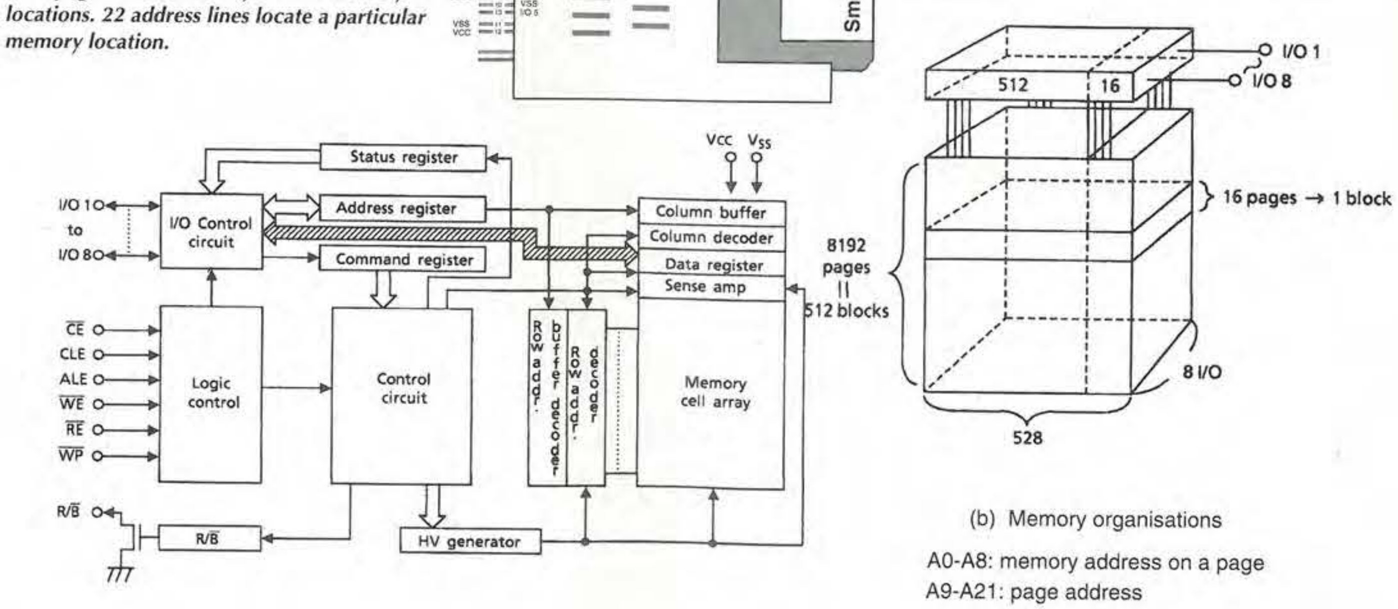


Fig. 4. Internal block diagram of the TC5832DC and its memory organisation. The 4Mbyte memory space is split into 512 blocks. Each block contains 16 pages and each page contains 528 byte-wide memory locations. 22 address lines locate a particular memory location.

(a) Internal block diagram of the TC5832DC

(b) Memory organisations

A0-A8: memory address on a page
A9-A21: page address
(A13-A21: Block address
A9-A12: NAND address in block)

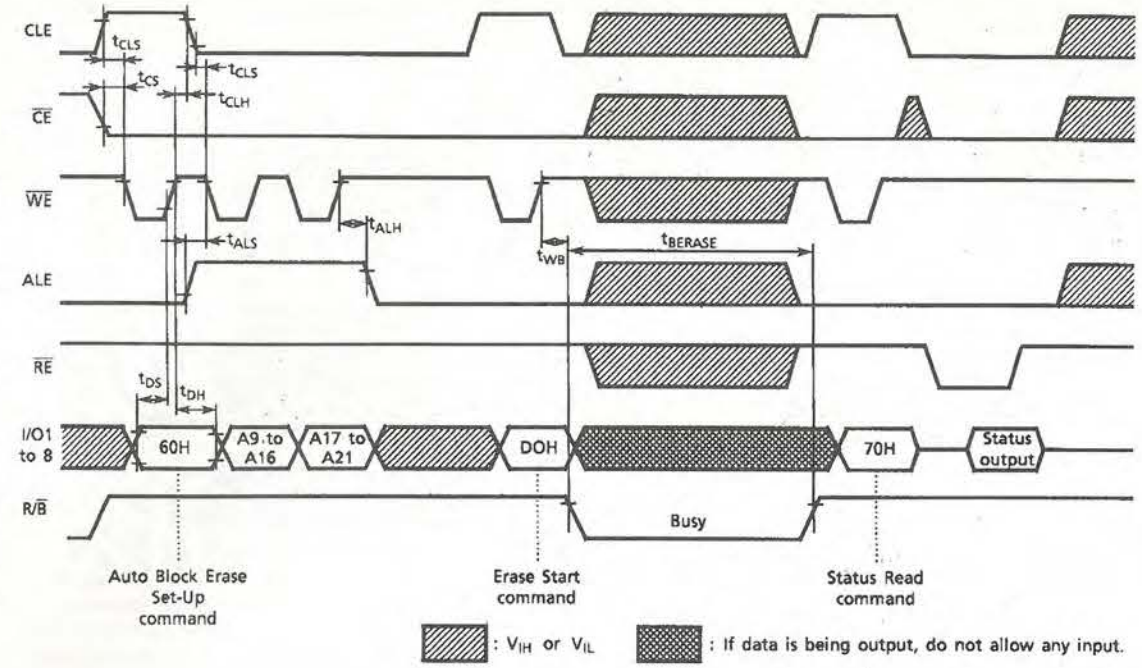


Fig. 5. Timing sequence for erasure. To start the operation, a 60_{16} command is written into the memory disk. It is followed by two addresses to specify a memory block in which memories are to be erased. Next another command, $D0_{16}$, is written into the memory. After the second command is written into the TC5832DC, it begins the erasing operation. Erasing will cause all memory locations in the block to be FF_{16}.

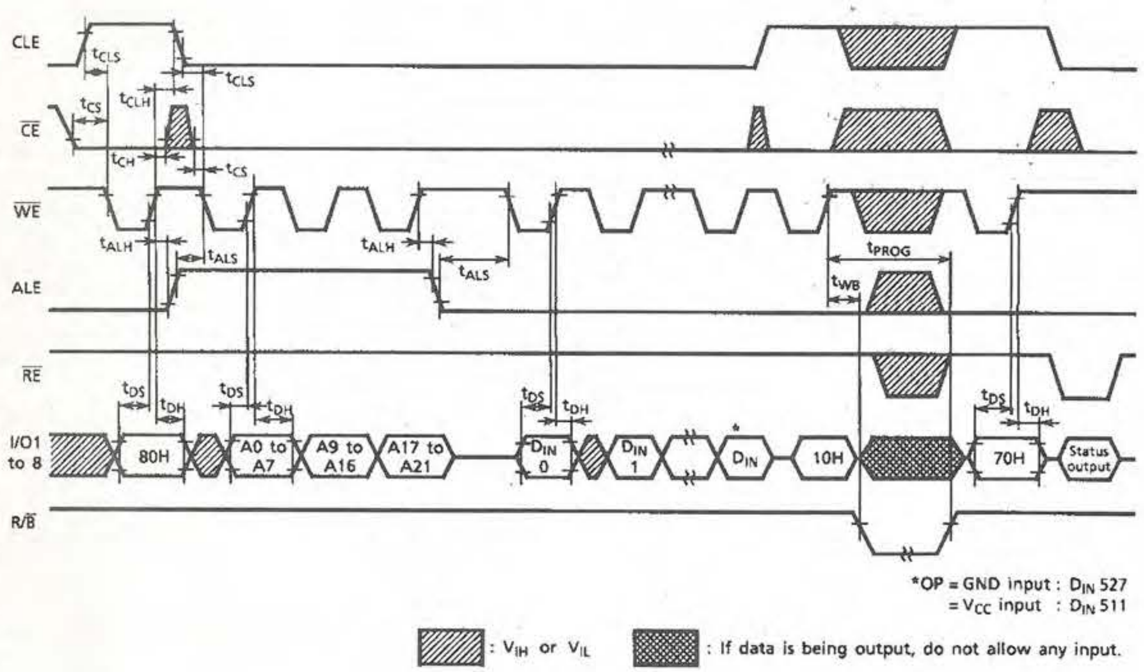


Fig. 6. Timing sequence for the programming operation. To start programming, command 80_{16} is written into the TC5832DC. It is followed by three address bytes to specify a stating point and a memory page. Next, 528 (or 512) data are written into the data buffer registers of the memory disk. The auto page program command 10_{16} is then written into the disk. After this, the TC5832 transfers the data from the data buffer registers into the memory locations in that page.

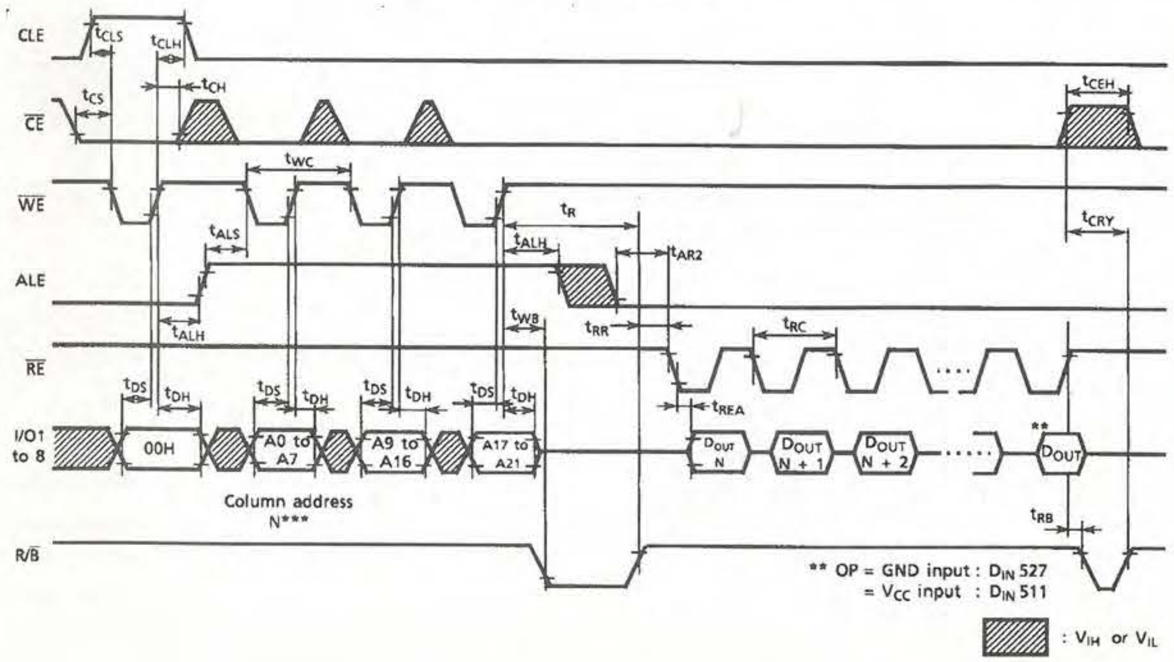


Fig. 7. Timing sequence for the reading operation. Command 00_{16} is written into the TC5832DC. It is followed by three address bytes: the starting address and the page address. Data bytes stored in the memory disk are clocked out under the control of –RE.

ferred are data rather than commands. The two bytes A_{9-16} and A_{17-21} are written into the device at the rising edges of two more pulses applied to the –WE line.

To perform the actual erasing operation, a command byte $D0_{16}$ is written into the disk. At the rising edge of the last –WE pulse, the disk begins to erase the specified memory block. To indicate that the device is busy, the ready/busy pin R/–B is set low.

During erasing, the memory disk automatically performs erasing and verification for each memory cell. Erasing is terminated if either all the memory locations are erased successfully or the maximum number of erasing loops are completed.

If the maximum number of loops is completed, some memory locations may not be erased and the block concerned should be flagged as 'bad'. Using the status read command, 70_{16}, you can check if the erase operation is successful. After erasing, all memory locations in the specified block will become FF_{16}.

Programming and reading

Timing relationships for the programming operation are shown in **Fig. 6**.

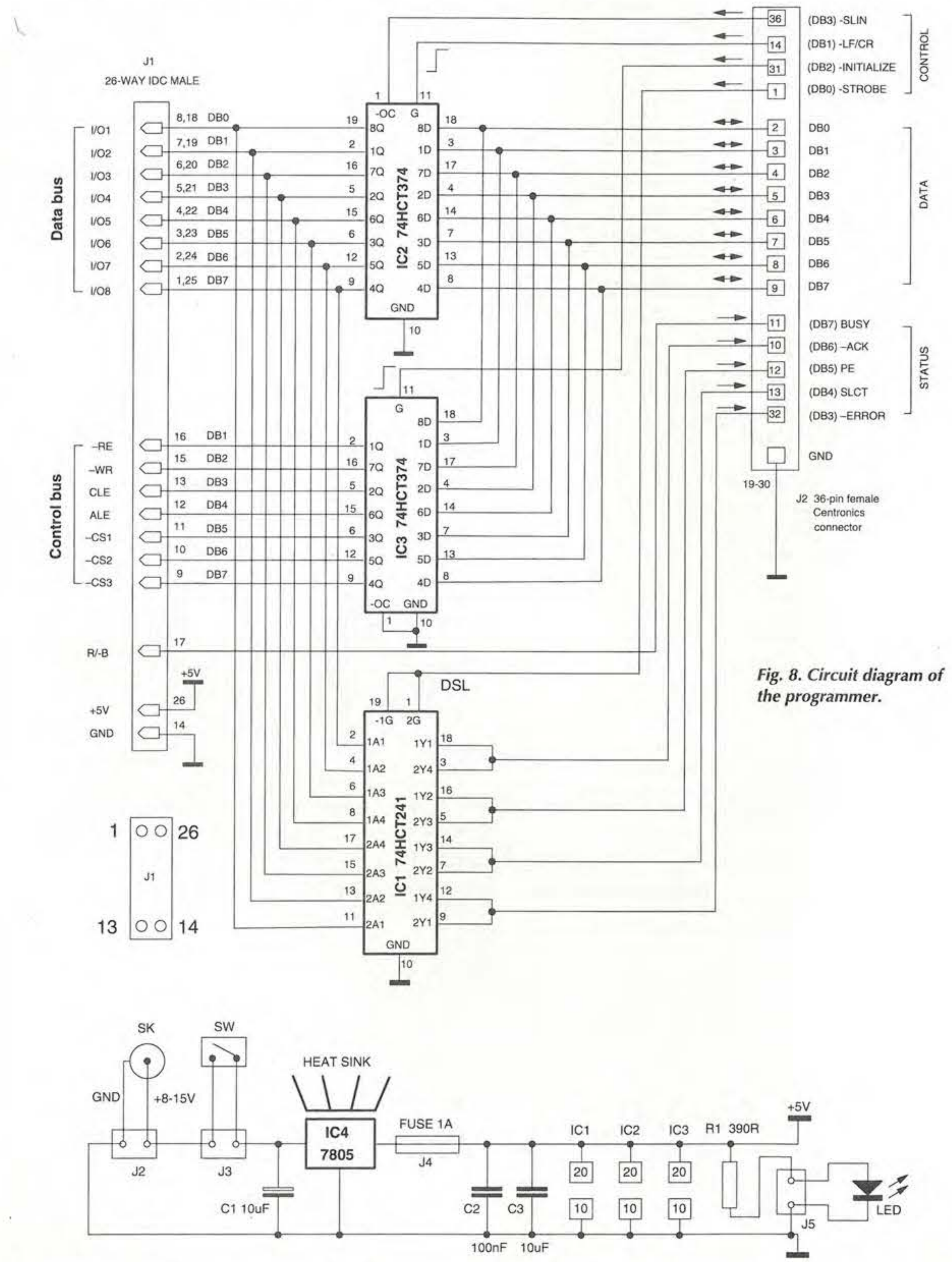


Fig. 8. Circuit diagram of the programmer.

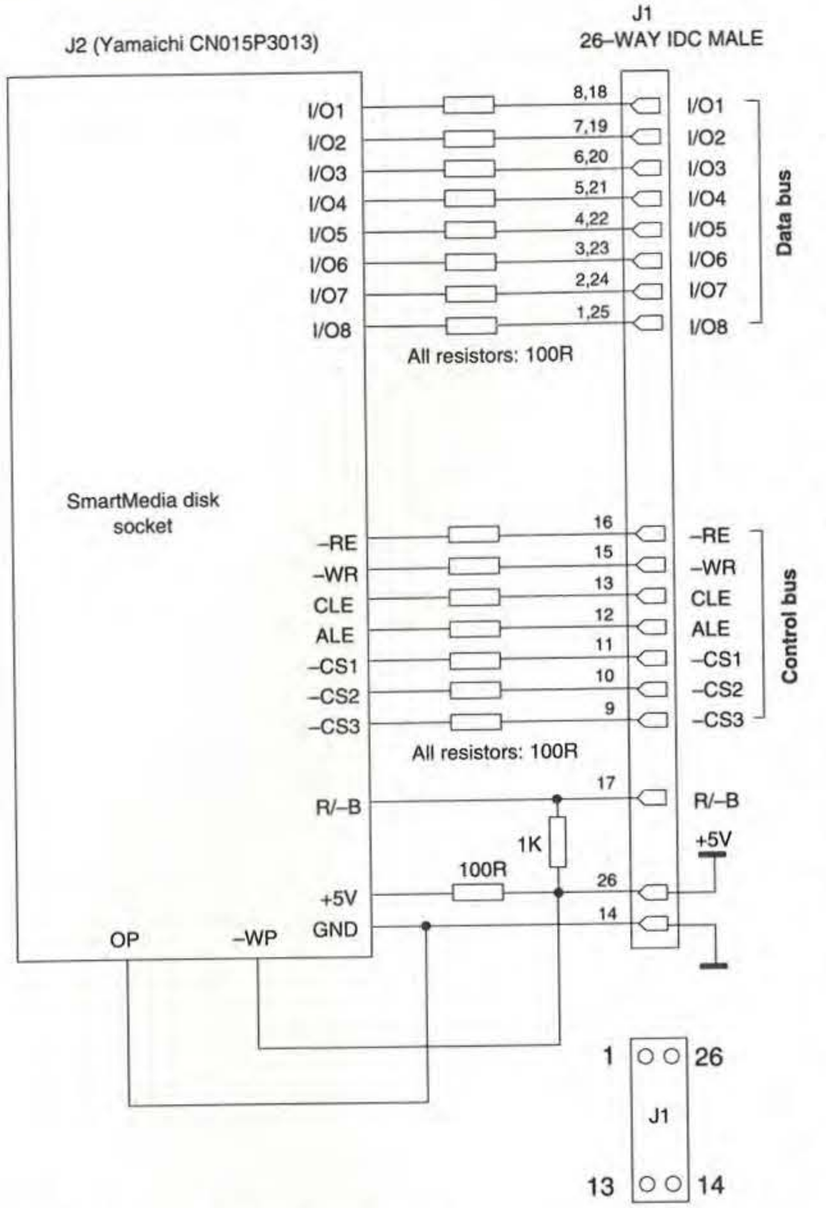


Fig. 9. Circuit diagram of the socket board

Firstly, the programming command 80_{16} is written into the device by holding CLE high, ALE low, then applying a high-to-low-then-high pulse to –WE. Then three address bytes A_{0-7}, A_{9-16} and A_{17-21} are written into the device by holding CLE low, ALE high, and sending three pulses –WE).

Next ALE is pulled to low. A group of 528 data bytes are written into the data buffer register at the rising edges of 528 pulses applied to the –WE. If OP is connected to V_{CC} however, 511 data bytes are written.

After that the auto page programming command 10_{16} is written into the device and the device begins programming. The R/–B line goes low to indicate that the device is busy.

Following page programming, the programmed data in memory is verified. If the programming is not successful, the data is programmed again until programming is successful or the maximum loop number is reached.

Using the status read command 70_{16}, you can check whether the programming operation has been successful. The programming only writes zeros into memory bits.

Timing for the read operation is shown in **Fig. 7**. For more details of the operations of the *TC5832CD*, obtain a copy of the manufacturer's data sheets. These are available from the Toshiba's web site given later.

Programming hardware

Figs 8 and **9 demonstrate how simple the** circuitry of the programmer is. It contains only three 74HCT logic chips and connects to the Centronics port via a standard printer cable.

The memory disk slots into a disk holder which, in my design, is on a separate circuit board. Assembly of the system is shown in **Fig. 10**.

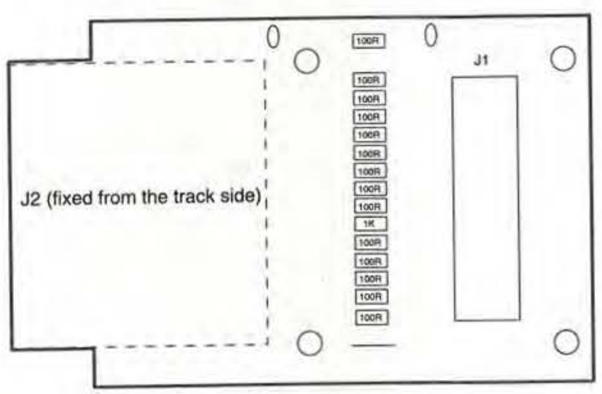
Pin designations for the PC's Centronics port are shown in **Fig. 11**. Details of the Centronics port can be found in reference 2.

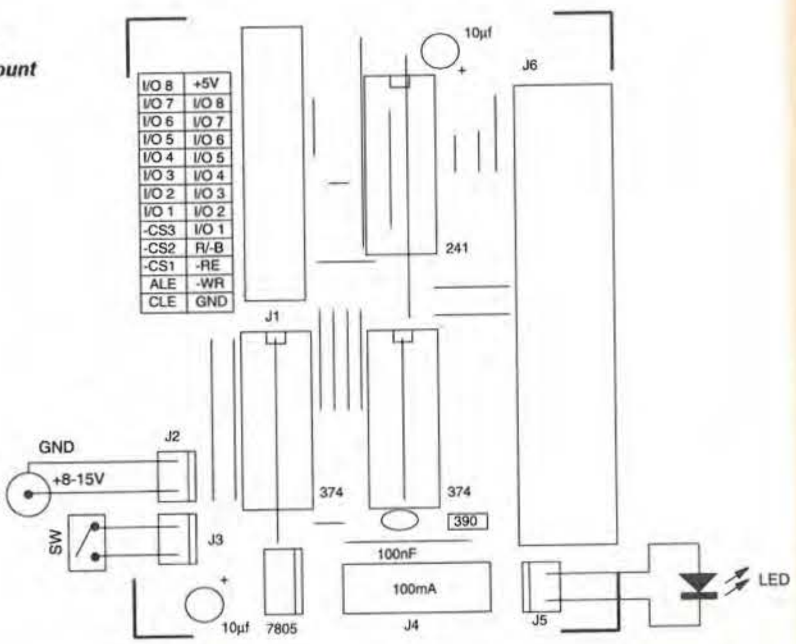
In brief, a standard Centronics port involves three i/o ports. One port is the data port comprising eight outputs, one is the control port comprising four outputs and the third is the status port which has five inputs.

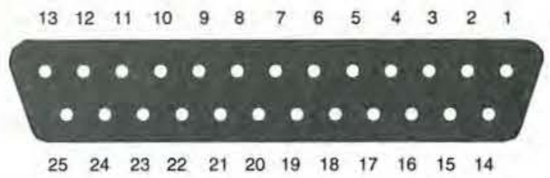
A computer uses the data and control ports to output data and the status port to input five-bit data.

Gate IC_1, a 74HCT241, is an eight-to-four line data selector which allows a byte to be read into the pc through four input lines. The eight-bit data is read into the pc in two consecutive reads, the first reading being the low four bits and the second the upper four bits.

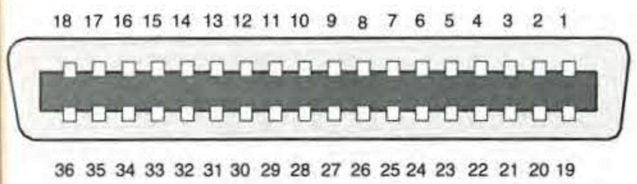
Fig. 10. Assembled SmartMedia memory card programmer on two single-sided circuit boards. The memory card socket is a surface mount device and is fixed onto the board from the track side.







(a) Pin-out of the Centronics connector on pc compatibles - viewed from the back of the pc.
Connector type: 25 pin female D-type



(b) Pin-out of the Centronics connector on printers - viewed from the back of the printer.
Connector type: 36 pin female Centronics-type

Fig. 11. Pin-out and functions of the Centronics port connectors on pcs and on printers. The Centronics connector on the programmer takes the form shown in b).

Pin functions of the Centronics port connectors

Connector on: computer	printer	Direction	Name	Explanation
1	1	C to P	STROBE	Strobe data
2	2	C to P	DB0	Data bit 0
3	3	C to P	DB1	Data bit 1
4	4	C to P	DB2	Data bit 2
5	5	C to P	DB3	Data bit 3
6	6	C to P	DB4	Data bit 4
7	7	C to P	DB5	Data bit 5
8	8	C to P	DB6	Data bit 6
9	9	C to P	DB7	Data bit 7
10	10	P to C	ACK	Indicating data received
11	11	P to C	BUSY	Indicating printer busy
12	12	P to C	PE	Indicating paper empty
13	13	P to C	SLCT	Indicating printer on line
14	14	C to P	LF/CR	Auto line feed after carriage return
15	32	P to C	ERROR	Indicating printer error
16	31	C to P	INITIALIZE	Initialise printer
17	36	C to P	SLIN	Select/deselect printer
18-25	19-30 and 33		GND	Twisted-pair return ground
	18,34		Unused	
	16		Logic GND	Logic ground
	17		Chassis GND	Chassis ground

'C' = computer 'P' = printer

The two readings are controlled by the data-select line DSL. A byte is placed on the 'D' inputs of the data buffer IC_2 and is latched to the internal output registers at the low-to-high transition of a signal applied to G on pin 11.

If the output-control pin –OC is high, the 'Q' outputs are in tri-state. If –QC is low, the latched data appears at the 'Q' outputs. Data is latched into the outputs of control buffer IC_3 in a similar fashion as for the IC_2. Output control pin –OC is permanently at logic low to enable the latched data.

The three ports of the Centronics interface are used as follows. Data port DB_{0-7} outputs data to the data buffer I/O_{1-8} or outputs data to the control buffer. Here, DB_0 is not used, DB_1 is –RE, DB_2 is –WR, DB_3 is CLE, DB_4 is ALE, DB_5 is $-CS_1$, DB_6 is $-CS_2$ and DB_7 is $-CS_3$.

The Centronics control port controls the internal operations of the programmer. Line DB_0 selects the upper or lower four bits of data connected to the data selector IC_1.

Bit DB_1 controls the data latching into the data buffer IC_2 and DB_2 controls the data latching into the control buffer IC_3. Line DB_3 enables the data buffer IC_2 to output data or to float the outputs from the buffer.

Status port DB_{3-6} reads the upper and lower four bits of data from the data bus. Bit DB_7 of the status port connects to the ready/busy pin of the memory disk. ■

Reference

1. Data sheet for TC5832DC is available from Toshiba's wet site: http://www.toshiba.com
2. PC interfacing using Centronic, RS232 and game ports, Pei An, Newnes, 1998, ISBN0 2405 1448 3

Software is described next month

Technical support

Kits including all necessary components (including the disk socket) to construct a complete programmer and the TP6 source codes are available from the authors. Please make your enquiry to Dr Pei An at 11 Sandpiper Drive, Stockport, Manchester SK3 8UL, U.K. Tel/Fax/Answer:+44-(0)161-477-9583. Pei's e-mail address is PAN@FS1.ENG.MAN.AC. UK.

Table 2. Summary of commands.

Command	Hex. value	Definition
Serial data input	80	Write 528 (or 512) data bytes into data buffer registers. 'OP' pin determines whether 528 bytes (OP=GND) or 512 bytes (OP=VCC) is written
Read mode 1	00	Read bytes from a page starting from 0 to 255 addresses
Read mode 2	01	Read bytes from a page starting from 255 to 511 addresses
Read mode 3	50	Read bytes from a page starting from 512 to 527 addresses
Reset	FF	Stop all operations and set the device in wait state
Auto page program	10	Data in buffer registers is programmed into memory
Auto block erase	60+D0	Erase a block. Verification is performed
Suspend erasing	B0	Suspend erasing
Resume	D0	Resume erasing
Status read	70	Read verification status of programming and erasing. Operation pass: I/O1=0; operation fail: I/O1=1. Write protected: I/O8=0; not write protected: I/O8=1
ID read	90	Read ID from device. Values 98_{16} and $8B_{16}$ should be read

Senior Hardware Engineer
Hants £22k to £28k

This well known company is looking to recruit a Hardware Engineer who can offer at least 2 years design experience within the electronics arena. Ideally you will have experience of low power, cost sensitive consumer products. The position involves the design and development of GSM dual mode mobile phones and hands free units, therefore you will need good digital design (80386 and H8 processors) and low level software design experience. Basic analogue knowledge will also be useful. TIME108

Graduate Hardware Engineer
Hants £20k to £25k

An opportunity for a Graduate level hardware engineer currently exists with this company who design and develop inspection equipment for the food and drugs related industries. Ideally you will be a recent graduate with some R&D experience. You should have an understanding of Digital Design, microprocessor design and high level software experience. Technology areas are varied and include analogue RF, digital and 32 bit embedded processors. TIME109

RF/Microwave Design Engineers
Kent to £35k

One of the world's leading companies involved in the design and development of vehicle antenna systems is currently looking to expand its team to keep it at the forefront of communications and intelligent transport systems technologies. You will need to be well qualified with solid experience of RF and Microwave design, LNAs, filters, diversity systems and measurement techniques. Any experience of antenna design would be very beneficial. TIME110

Hardware Design Engineer
Herts £18k to £25k

Good quality position, with a small but very successful company is currently available for an experienced hardware engineer who can offer at least 1 year's proven experience in hardware design for broad level products. A minimum HND is required along with experience of PLDs, FPGAs, TTL/CMOS logic design, analogue and digital interfacing and software design experience in C and Assembler. Any experience of Intel processors would be beneficial. This is an excellent second career move prospect. TIME111

Hardware Design Engineers
Lancs £neg

This progressive company require hardware engineers to join their R&D department involved in the design and development of electronic fire protection systems. You will possess proven skills in hardware and software design. Degree qualified with at least 2 years experience you will have hardware skills in microprocessor and microcontroller design and software skills in embedded C and Asssembler. These are good opportunities with a very stable company. TIME204

Software Engineers – Digital Broadcast
Bucks to £40k

World leader in the electronics field is currently looking to recruit Software Engineers who have at least 5 years experience in software design, with a solid background in real-time embedded software in C. You will have solid experience of working with custom hardware and have excellent experience in at least one of the following areas: DVB, MPEG, GSM. TIME205

Project Leader – Digital Broadcasting
M40 (outside M25 belt) £neg

Superb company involved in the development of digital broadcasting products are currently looking for a Project Leader who can offer at least 5 years experience of designing digital and software systems. You will be responsible for developing LSI and PCB based systems for digital audio and video broadcasting. As a project leader you will have strong team leadership skills as well as excellent man-management skills. As a senior level engineer you will need to be able to demonstrate a proven track record in hardware and software design. TIME206

Digital ASIC Design Engineers
Surrey & Hants £25k to £38k

This company releases on average 10 new technically advanced products for the telecommunications industry each year. To maintain this level of commitment they are looking to recruit top level design engineers who are able to design and develop products for the commercial market. Positions exist for graduate level engineers, through to senior/team leaders who have at least 2 years experience of ASIC design. You should have solid VHDL (or similar) tools experience. TIME100

Senior ASIC Designers
Cambs £24k to £35k

A rare opportunity to be involved in the design and development of some of the best future products is currently available with one of the UK's most respected design houses. You will be involved in the design of the latest ASIC technology for implementation into new Multimedia and Communications products. You will need a good degree (1st or 2:1) with an excellent track record in commercial product design. High gate level design experience is required coupled with excellent VHDL/Synopsys (synthesis and simulation). TIME101

Hardware Design Engineers
Surrey, Hants & Berks £20k to £38k

There is a superb array of positions available for hardware engineers who are looking for a fresh challenge. Positions currently exist in the Telecomms, TV and Video and Networking industries. You will need to be a graduate engineer with 2 years+ experience of digital and analogue design with experience gained in FPGAs, PLDs and processor design as well as having good experience of software design for embedded applications (C, C++ and Assembler). Any experience of the following would be highly beneficial: DSP, Audio, RF. TIME102

Learn RF/IC Design (superb offered prospect)
North London £20k to £36k

This well known company is involved in telecommunications and datacommunications, and has several dedicated design sites throughout the UK, Europe and the US. They are currently looking to recruit several bright engineers who are interested in the prospect of being trained as RF/IC Design Engineers. To qualify for these excellent opportunities you will need to be degree qualified and have at least 1 year's industrial experience in one of the following:
ASICs Optoelectronics Analogue ICs RF Design
You will need to be very bright and be capable of learning very complex design methods used in RF/IC designs. As part of your training, you will be required to spend several weeks abroad. TIME105

contact: Steve Riley
01844 202675
Crendon House Drake's Drive
Long Crendon Aylesbury Bucks HP18 9BB
Fax: 01844 202676
Email: Steve_time@msn.com

Time resourcing — hardware software manufacture test

Software Design
M3/M4 £20k to £40k

We are currently looking for up to 6 (six) software engineers (6 in each application area) to work on the design and development of new and existing products within the ATM, telecomms (GSM) and Multimedia markets. You should have good experience in a real-time embedded environment using C, C++ under UNIX. Any experience of the following would be beneficial: DSP, SDH, OO systems design and analysis for real-time embedded systems, VxWorks, GUI design using Visual C++, Graphics, Network Management. TIME106

DSP Design
Surrey, Hants & Cambs £25k to £45k

With good coverage across the country DSP Engineers have got it sorted. There is an impressive mixture of both large and small companies looking for DSP Engineers to work on some very complex projects including algorithm development/analysis and signal fundamentals for areas such as Telecommunications, Musical Instruments, Broadcast and Multimedia. You will need at least 2 years experience of DSP software development using C, C++ and Assembler and be very technically minded. TIME107

RF Design Engineers
M3/M4, Cambs £20k to £45k+

The market for RF Design Engineers increases rapidly due to the continuous introduction of new innovative products mainly for the telecommunications market. This demand for RF Engineers has opened the door of over twenty companies who are looking for designers who have experience of Receiver, Transmitter, Synthesiser, LNA and filter design in the RF ranges 1.8 to 2GHz. Typical technologies include GSM, wireless CDMA and UNITS for mobile and fixed communications products. Naturally you will have good HP EEsof, Touchstone and/or PSPICE experience. TIME103

RF Design Engineers
Wiltshire £24k to £45k

Having already placed several RF Engineers with this company, we now have a requirement to further expand this successful team. For over two years this company has been designing and developing the next generation of basestation products and systems for the telecomms market and is now poised to continue its already enviable reputation for designing some of the best products around. The RF team is looking for engineers who have 1 year's+ experience of RF Design gained within a very strong technically advanced company. You will work as part of a team of engineers designing Rx, Tx, LNAs, Filters. Massive resources of technical talent and financial security make this company one of the best to work for. TIME104

Principal Digital Design Engineer
Surrey £neg

Superb company involved in the design and development of complex electronics instrumentation equipment are looking to recruit an experienced digital design engineer who has at least 3 years experience of PLDs, FPGAs ADC, DAC and H8 microcontroller design and programming. You should also have real-time embedded software design experience with hands-on C. Any experience of DSP and VHDL will be of interest. JUNIOR POSITION ALSO AVAILABLE. TIME112

Hardware and Software Engineers
Cambridge £20k to £35k

Young and dynamic company based in Cambridge who are involved in the design of exciting broadcast and post-production equipment are looking to expand their team of software and hardware design engineers and are currently looking for the following engineering professionals.
DSP Engineers: Algorithm development for digital video processing using DSP, RISC and microprogrammable hardware. Minimum 3 years DSP and C coding experience is required.
Software Engineers: 3 years experience of C within an embedded environment. Development of algorithm and application software for video and audio processing systems.
Digital Designer: Hands-on design for next generation Video and Audio processing equipment. Digital design, 64 and 128 bit RICS technology. Experience of high speed digital design, FPGAs, Power PC, SPARC, DSP, PCI, VME, digital video/audio.

Senior ASIC Designers
Cambridge £24k to £35k

A rare opportunity to be involved in the design and development of some of the best future products is available with one of the UK's most respected design houses. You will be involved in the design of the latest ASIC technology for implementation into new Multimedia and Communications products. You will need a good degree (2:1 or 1st) with an excellent track record in commercial product design. High gate level design experience is required coupled with excellent VHDL/Synopsys. TIME101

Move into Digital ASIC Design
Herts to £35k

Several positions currently exist for design engineers with this very successful young company who are involved in the design and development of very complex ASICs for markets such as datacom, telecomms and wireless. The position requires a good degree with at least 2 years digital design experience. It is not essential that you have ASIC/VHDL experience as a good FPGA/PLD background will be appropriate. TIME200

RISC Design Engineer
Berkshire to £45k

You will be involved in the development of sub-micron implementation and modelling of advanced RISC architectures using design tools and methodologies. The position involves the physical realisation of RISC processor architectures, involving RTL coding in VHDL or Verilog, implementation of designs. You will need to be experienced in the design of ASICs with VHDL and/or Verilog and embedded microprocessor design. You should also be able to perform gate level simulation and verification. TIME201

RF Design Engineers
M3/M4, Cambridge £20k to £45k+

RF Design Engineers are sought by companies both large and small, to be involved in the design and development of new innovative products. This demand for RF Design Engineers has paved the way for some very exciting career opportunities. Positions exist from Graduate level through to Team Leaders with experience levels ranging from 1 year's+ experience for RF Engineers already established in the market. You will have gained experience in the design and development of Receivers, Transmitters, LNAs, Filters and Synthesisers from 1.8 to 2GHz. Technology areas include GSM, UMTS, Wireless CDMA for mobile and fixed communications systems. TIME202

DSP Design Engineer
Cambridge, Surrey, Bristol
£25k to £40k

There is an impressive mixture of companies looking for DSP Engineers to work on some excellent projects involving the Engineers from initial concepts through to finished product. You will be involved in algorithm development/analysis and signal fundamentals for areas such as Telecommunications, Musical Instruments, Broadcast and Multimedia. You will need to have a good degree with a good understanding of DSP hardware (TMS320/DSP56000) and software development using C, C++ and Assembler. Any understanding of MPEG and MPEG audio compression algorithms. TIME203

Haymill

Recruitment Consultants

Hardware

ASIC Design
Hants up to £40k Ref: 825/01/EW
Clients in the communications industry urgently seek experienced ASIC Design Engineers. You would be involved in the whole process from specification to layout. You will be offered work on complex high speed ASICs utilising VHDL and synthesis tools (e.g. Synopsis). These are critical roles and can command excellent salaries and benefits packages.

Hardware Engineer
Wilts £28k to £39k Ref: 25/03/EW
We have design and manufacturing clients who seek engineers with experience of the design and development of analogue and digital electronics in microprocessor based systems. These projects are new technology based with excellent training and career prospects.

Senior Analogue Engineer
Oxon £28k to £35k Ref: 825/05/EW
This role requires detailed Analogue expertise with an appreciation of digital design techniques particularly. You should be skilled with digital modulation techniques particularly QAM, PSK and QPSK and ideally have a knowledge of DSP technology and any transmission related problems where high speed transmission is limited by cross talk.

Hardware Support Engineer
Hants £36k Ref: 825/07/EW
Provide technical expertise to the support function and resolve problems on customer site. You should have in-depth engineer experience, ideally with a hardware development slant. ASIC's oscilloscopes, data analyzers and microprocessor based systems. As one of the main interfaces between customer input into our future and current developments.

Embedded Software Engineer
Cambs £30k Ref: 825/09/EW
Our client in the medical instruments market, urgently require software engineer; they must have the following: HND/Degree or higher in Electronic Engineering. 2 years'+ relevant post graduate experience. Real time software skills for microcontroller applications. Software development skills in C, C++ and/or Modula 2 and assembler. Experience within a safety critical environment.

RF Engineer
Surrey £28k to £35k Ref: 825/02/EW
Our client is a leading communication research and development organisation. They seek an engineer with RF Design skills to create new products and solutions for their global market place. Examples of the types of work include: passive and active RF, HW such as antennas, cables connectors, amplifiers, repeaters and indoor coverage systems.

Senior Design Engineer
Berkshire £30k Ref: 825/04/EW
Design Engineers required to join a busy expanding team with the avionics industry. HND or Degree qualified in electronic/electrical or mechanical engineering, with proven industry experience. Unigraphics design package experience preferred, but applicants with proven experience in RF or ASIC welcomed for cross training. Lead designer/team leader roles available for the right candidate.

ASIC Engineer/Designers
Hemel Hempstead £39k Ref: 825/06/EW
You'll be responsible for ASIC specification, design, coding and synthesis. With over 2 years' ASIC experience, you'll ideally have a knowledge of Verilog and Synopsis design flow tools and statistical timing analysis. Able to work as part of a multi-disciplined team, you can produce innovative solutions to challenging systems design problems. Positions exist from hands-on Engineers with 2 years' plus experience to team and project leader roles.

UNIX Systems Administrator
Oxon £28k Ref: 825/08/EW
You will provide both hardware and software support for UNIX platforms and peripherals, in addition to providing support to our PC systems. Candidates must have experience of Sun operating systems (both Sun OS and Solaris), and be familiar with networking and firewall issues.

Software Project Manager
Cambs £39k Ref: 825/10/EW
Key responsibilities include management and guidance of internal software development projects and engineers as well as developing software for real-time data acquisition and processing in a PC environment. Management of external development contractors and development of system integration and test plans. Candidates need to be degree qualified and possess 5 years' software development experience that will include Assembler, C or C++, Embedded Software.

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Hardware

RF Design Engineer
Berks up to £25k Ref: 825/11/EW
This company are searching for individuals to design and test to board level RF circuits to be used in a GSM design product. This will include detailed schematic definition and close guidance of PCB layout work. Your experience will include 2 years'+ RF design, ideally in a cellular application area, practical hands-on experience of RF board level design using appropriate test equipment (GSM experience would be highly desirable).

Hardware Design
Surrey £33k Ref: 825/13/EW
GEW into the cutting edge of PC hardware design with this innovative organisation. You will be designing single board PC's for industrial applications with cradle to grave project input. You should have at least 3 years' experience of microprocessor hardware design.

RF Designer
Berkshire £28k to £33k Ref: 825/15/EW
Your degree and RF Design experience can get you into this major electronic components manufacturer. You will be used to short project lifetimes and getting results quickly. Generous package including flexible hours, pension scheme and all the benefits of working for a large established organisation.

RF Test
Oxon £18k to £25k Ref: 25/17/EW
Our clients in the communications and related industries can offer experienced RF test engineers excellent openings within their production and R&D facilities. The ideal background would be ONC/HND qualifications plus 6 months'+ RF test experience.

Senior RF Design Engineer
Herts £36k Ref: 825/19/EW
RF Design engineer required to work on a range of radio modems, must have the ability to work at every level ie component, circuit and system level. At least 5 years' experience as a radio frequency design engineer in PMR and Data, ability to design circuitry for narrow-band hand portable and mobile data radios.

VLSI Design
Hants up to £28k Ref: 825/12/EW
You will work as a member of the VLSI Design Group developing multi-media, CD and television display and control products from systems concept to volume production. Your experience will be in the use of ideally VLSI IC design tools and methodologies, you will be qualified to at least degree level or equivalent, have a creative approach to problems solving and be willing to travel.

Hardware Designer
Surrey £35k Ref: 825/14/EW
Minimum 3 years' experience in a hands on role ideally in a low power environment. In depth digital knowledge is required as is low level software design experience. The ability to communicate effectively is also a must. Analogue experience would be a distinct advantage.

Hardware Design Engineer
Cambs £25k to £40k Ref: 825/16/EW
Experience in digital and embedded 16/32 bit microprocessor, knowledge of VHDL and high level design techniques would be advantageous. The job will entail development and support new ATM interface board.

ASIC Developer
Hants £30k Ref: 825/18/EW
Designing and developing ASICs, all candidates must be graduates with at least 3 years' experience in taking ASIC developments from specification through to completion. It is essential you have in depth knowledge of VHDL and VLSI. Previous experience of dealing with vendors would also be advantageous.

Digital Design Engineer
Berks £20k to £36k Ref: 825/20/EW
Our client is looking to recruit an experienced design engineer with at least 2 years' experience of FPGA PLD's ADC and micorcontroller design. Ideally candidates should also have real-time, embedded experience ideally developing in C.

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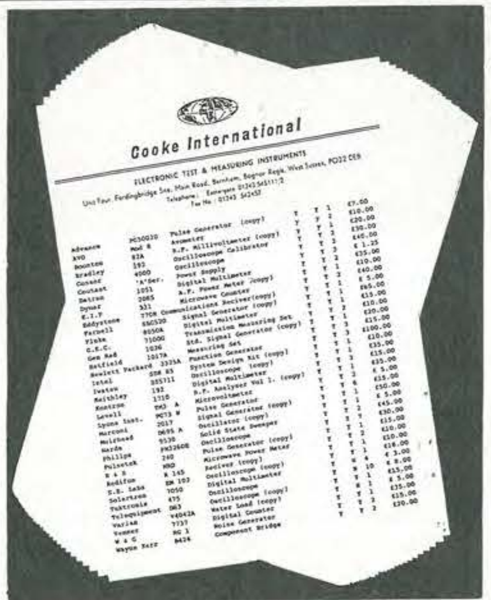

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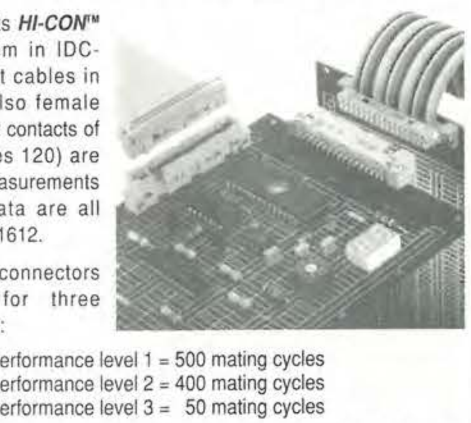

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Performance level 1 = 500 mating cycles
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Figure 1

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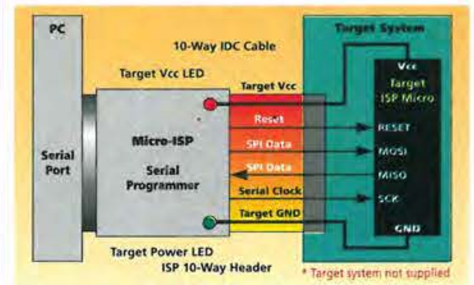

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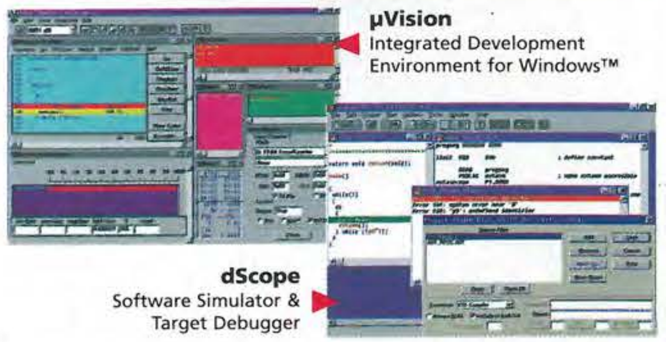

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