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NOVEMBER 1982

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# PRACTICAL ELECTRONICS

VOLUME 18

No. 11

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	1a012	12+12	1.25	
	1a013	15+15	1.00	
	1a014	18+18	0.83	
	1a015	22+22	0.68	
	1a016	25+25	0.60	
1a017	30+30	0.50		
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	2a011	9+9	2.77	
	2a012	12+12	2.08	
	2a013	15+15	1.66	
	2a014	18+18	1.38	
	2a015	22+22	1.13	
	2a016	25+25	1.00	
2a017	30+30	0.83		
2a018	110	0.45		
2a019	220	0.22		
2a030	240	0.20		
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	3a011	9+9	4.44	
	3a012	12+12	3.33	
	3a013	15+15	2.66	
	3a014	18+18	2.22	
	3a015	22+22	1.81	
	3a016	25+25	1.60	
3a017	30+30	1.33		
3a028	110	0.72		
3a029	220	0.36		
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	5a017	30+30	2.66	
5a018	35+35	2.28		
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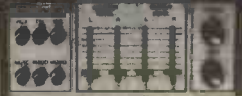
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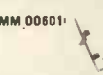
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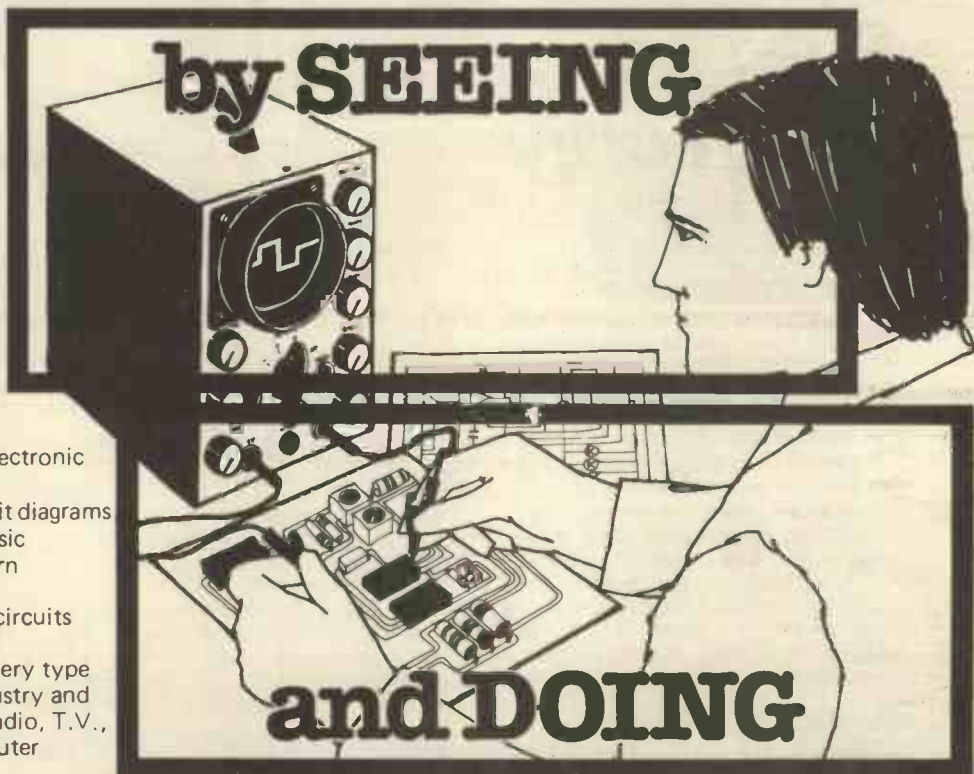
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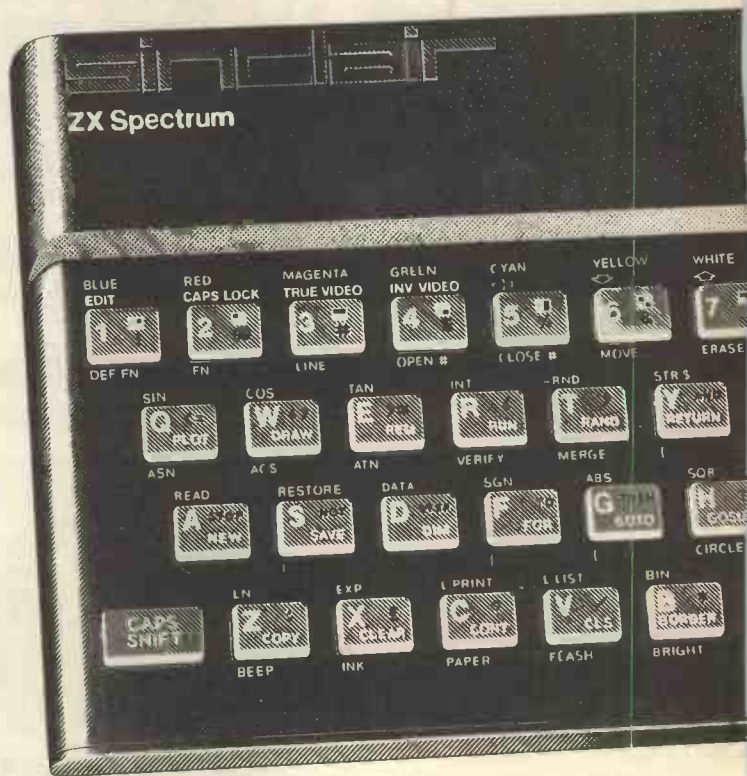
You have access to a range of 8 colours for foreground, background and border, together with a sound generator and high-resolution graphics.

You have the facility to support separate data files.

You have a choice of storage capacities (governed by the amount of RAM). 16K of RAM (which you can upgrade later to 48K of RAM) or a massive 48K of RAM.

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You may decide to begin with the 16K version. If so, you can still return it later for an upgrade. The cost? Around £60.



## Ready to use today, easy to expand tomorrow

Your ZX Spectrum comes with a mains adaptor and all the necessary leads to connect to most cassette recorders and TVs (colour or black and white).

Employing Sinclair BASIC (now used in over 500,000 computers worldwide) the ZX Spectrum comes complete with two manuals which together represent a detailed course in BASIC programming. Whether you're a beginner or a competent programmer, you'll find them both of immense help. Depending on your computer experience, you'll quickly be moving into the colourful world of ZX Spectrum professional-level computing.

There's no need to stop there. The ZX Printer—available now—is fully compatible with the ZX Spectrum. And later this year there will be Microdrives for massive amounts of extra on-line storage, plus an RS232 / network interface board.



## Key features of the Sinclair ZX Spectrum

- Full colour—8 colours each for foreground, background and border, plus flashing and brightness-intensity control.
- Sound—BEEP command with variable pitch and duration.
- Massive RAM—16K or 48K.
- Full-size moving-key keyboard—all keys at normal typewriter pitch, with repeat facility on each key.
- High-resolution—256 dots horizontally x 192 vertically, each individually addressable for true high-resolution graphics.
- ASCII character set—with upper- and lower-case characters.
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- High speed LOAD & SAVE—16K in 100 seconds via cassette, with VERIFY & MERGE for programs and separate data files.
- Sinclair 16K extended BASIC—incorporating unique 'one-touch' keyword entry, syntax check, and report codes.



# um



## The ZX Printer – available now

Designed exclusively for use with the Sinclair ZX range of computers, the printer offers ZX Spectrum owners the full ASCII character set – including lower-case characters and high-resolution graphics.

A special feature is COPY which prints out exactly what is on the whole TV screen without the need for further instructions. Printing speed is 50 characters per second, with 32 characters per line and 9 lines per vertical inch.

The ZX Printer connects to the rear of your ZX Spectrum. A roll of paper (65ft long and 4in wide) is supplied, along with full instructions. Further supplies of paper are available in packs of five rolls.



## The ZX Microdrive – coming soon

The new Microdrives, designed especially for the ZX Spectrum, are set to change the face of personal computing.

Each Microdrive is capable of holding up to 100K bytes using a single interchangeable microfloppy.

The transfer rate is 16K bytes per second, with average access time of 3.5 seconds. And you'll be able to connect up to 8 ZX Microdrives to your ZX Spectrum.

All the BASIC commands required for the Microdrives are included on the Spectrum.

A remarkable breakthrough at a remarkable price. The Microdrives are available later this year, for around £50.



## How to order your ZX Spectrum

BY PHONE – Access, Barclaycard or Trustcard holders can call 01-200 0200 for personal attention 24 hours a day, every day. BY FREEPOST – use the no-stamp needed coupon below. You can pay by cheque, postal order, Access,

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EITHER WAY – please allow up to 8 days for delivery. And there's a 14-day money-back option, of course. We want you to be satisfied beyond doubt – and we have no doubt that you will be.

## RS232/network interface board

This interface, available later this year, will enable you to connect your ZX Spectrum to a whole host of printers, terminals and other computers.

The potential is enormous. And the astonishingly low price of only £20 is possible only because the operating systems are already designed into the ROM.

## ZX Spectrum

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Component Tester: For single components and **in circuit**  
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Displays an analogue voltage on a linear 10 element LED display as a bar or single dot. Ideal for thermometers, level indicators, etc. May be stacked to obtain 20 to 100 element displays. Requires 5-20V supply. **£4.50**
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Based on the SL441 zero voltage switch, this kit may be wired to form a "burst fire" power controller, enabling the temperature of an enclosure to be maintained to within 0.5°C. Max. load 3KW **£5.55**
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Based on the ZN1034E Timer IC this kit will switch a mains load on (or off) for a preset time from 20 mins. to 35 hrs. Longer or shorter periods may be realised by minor component changes. Max. load 1KW. **£4.50**

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Based on the SAB0600 IC the kit is supplied with all components, including loudspeaker, printed circuit board, a pre-drilled box (95 x 71 x 35mm) and full instructions. Requires only a PP3 9V battery and push-switch to complete. AN IDEAL PROJECT FOR BEGINNERS. **£5.00**

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The kit comprises a mains powered receiver, a four button transmitter, complete with pre-drilled box, requiring a 9V battery and one opto-isolated solid state switch kit for interfacing the receiver to mains appliances. As with all our kits, full instructions are supplied. **Only £23.75**

Extra Solid State Switch Kits (XK104) and transmitters (XK105) can be supplied.

**XK104 £2.40 XK105 £10.50**

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## THE HOME CONTROL CENTRE

This New Remote Control Kit enables you to control up to 16 different appliances anywhere in the house from coded pulses into your armchair. The transmitter injects supply and used to switch on the appliance addressed. Receivers are addressed by means of a 16-way keyboard, followed by an on or off command. Since pushing buttons can become rather boring, the transmitter also includes a computer interface so you can program your favourite micro to switch lights, morning, electric blanket, make your coffee in the OF THE POSSIBILITIES. The KIT includes all PCBs and components for one transmitter and two receivers plus a pre-drilled box for the transmitter.

Order as XK112 **£42.00**

## DISCO LIGHTING KITS

**DL1000K**  
This value-for-money kit features a bi-directional sequence, speed of direction and frequency of direction change, being variable by means of potentiometers and incorporates a master dimming control. **Only £14.60**

**DL2100K**  
A lower cost version of the above, featuring unidirectional channel sequence with speed variable by means of a pre-set pot. Outputs switched only at mains zero crossing points to reduce radio interference to a minimum. **Only £8.00**

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## REMOTE CONTROL KITS

- MK6 SIMPLE INFRA RED TRANSMITTER**  
Pulsed infra red source complete with hand-held plastic box. Requires a 9V battery. **£4.20**
- MK7 INFRA RED RECEIVER**  
Single channel, range approx. 20ft. Mains powered with a triac output to switch loads up to 500W at 240V ac. **£8.00** (RC500K—Special Price for MK6 and MK7 together **£12.50**)
- MK8 CODED INFRA RED TRANSMITTER**  
Based on the SL490, the kit includes all components to make a coded transmitter and only requires a 9V (PP3) battery. 8 x 2 x 1.3cms **£5.90**
- MK10 16-WAY KEYBOARD**  
For use with MK8 and MK12 to generate 16 different codes for decoding by the ML928 or ML926 receiver (MK12) kit. **£5.40**
- MK11 10-Channel + 3 Analogue o/p IR Receiver**  
Based on ML922 decoder IC. Functions include onstandby output, toggle, control of volume, tone and lamp brightness. Includes its own mains supply. **£12.00**
- MK12 16-CHANNEL IR RECEIVER**  
For use with MK8 kit with 16 on/off outputs, which was further interface circuitry, such as relays or triacs, will switch up to 16 items of equipment on or off remotely. Latched or momentary outputs — please specify when ordering. Includes its own mains supply. **£11.95**
- MK13 11-WAY KEYBOARD** For use with MK8, MK18 and MK11 kits. **£4.35**
- MK18 Mains Powered IR Transmitter**  
Mains powered for continuous operation — single channel, for applications such as burglar alarms, automatic door openers, etc. Range approx. 6 ft. **£2.50**
- MK17 12V d.c. IR RECEIVER**  
For use with MK6 or MK16. Relay output with DP3 Amp change-over contacts, may be used as latched, momentary or "break beam" receiver. Operates from 6-13V d.c. **£9.50**
- MK18 HIGH POWER IR TRANSMITTER**  
Similar to MK8 but with range of approx. 60ft. **£8.20**
- Ancillary Kits:** MK2 Solid State Relay **£2.60**  
Opto-isolated with zero voltage switching. No. triac supplied.
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3N159	2.56	IC1686	10p	4644	33p	BD81	1.20	MP5A20	45p	ATI-5200	95p	LM318AN	1.40	TA6621	2.63	7424	24p	74LS66	14p	74C76	1.34	4002	10p
3N200	2.93	IC1690	10p	4645	33p	BD82	1.20	MP5A42	45p	ATI-5250	95p	LM318AN	1.80	TA6622	2.45	7425	24p	74LS68	14p	74C77	1.40	4003	10p
3N201	6.98	IC1698	10p	4646	33p	BD83	1.20	MP5A44	45p	ATI-5300	95p	LM318AN	1.20	TA6623	2.47	7426	24p	74LS70	14p	74C78	1.34	4004	10p
40251	2.95	IC1700	10p	4647	33p	BD84	1.20	MP5A45	45p	ATI-5350	95p	LM318AN	1.40	TA6624	2.47	7427	24p	74LS72	14p	74C79	1.34	4005	10p
40252	2.54	IC1702	10p	4648	33p	BD85	1.20	MP5A65	45p	ATI-5400	95p	LM318AN	1.40	TA6625	2.47	7428	24p	74LS74	14p	74C80	1.34	4006	10p
40253	2.75	IC1704	10p	4649	33p	BD86	1.20	MP5A66	45p	ATI-5450	95p	LM318AN	1.40	TA6626	2.47	7429	24p	74LS76	14p	74C81	1.34	4007	10p
40264	2.63	IC1708	10p	4650	33p	BD87	1.20	MP5A67	45p	ATI-5500	95p	LM318AN	1.40	TA6627	2.47	7430	24p	74LS78	14p	74C82	1.34	4008	10p
40280	2.60	IC1710	10p	4651	33p	BD88	1.20	MP5A68	45p	ATI-5550	95p	LM318AN	1.40	TA6628	2.47	7431	24p	74LS80	14p	74C83	1.34	4009	10p
40290	2.60	IC1712	10p	4652	33p	BD89	1.20	MP5A69	45p	ATI-5600	95p	LM318AN	1.40	TA6629	2.47	7432	24p	74LS82	14p	74C84	1.34	4010	10p
40299	1.80	IC1718	10p	4653	33p	BD90	1.20	MP5A70	45p	ATI-5650	95p	LM318AN	1.40	TA6630	2.47	7433	24p	74LS84	14p	74C85	1.34	4011	10p
40311	9.70	IC1720	10p	4654	33p	BD91	1.20	MP5A71	45p	ATI-5700	95p	LM318AN	1.40	TA6631	2.47	7434	24p	74LS86	14p	74C86	1.34	4012	10p
40312	1.64	IC1722	10p	4655	33p	BD92	1.20	MP5A72	45p	ATI-5750	95p	LM318AN	1.40	TA6632	2.47	7435	24p	74LS88	14p	74C87	1.34	4013	10p
40313	1.83	IC1724	10p	4656	33p	BD93	1.20	MP5A73	45p	ATI-5800	95p	LM318AN	1.40	TA6633	2.47	7436	24p	74LS90	14p	74C88	1.34	4014	10p
40315	1.94	IC1726	10p	4657	33p	BD94	1.20	MP5A74	45p	ATI-5850	95p	LM318AN	1.40	TA6634	2.47	7437	24p	74LS92	14p	74C89	1.34	4015	10p
40316	9.95	IC1728	10p	4658	33p	BD95	1.20	MP5A75	45p	ATI-5900	95p	LM318AN	1.40	TA6635	2.47	7438	24p	74LS94	14p	74C90	1.34	4016	10p
40317	1.80	IC1730	10p	4659	33p	BD96	1.20	MP5A76	45p	ATI-5950	95p	LM318AN	1.40	TA6636	2.47	7439	24p	74LS96	14p	74C91	1.34	4017	10p
40318	1.80	IC1732	10p	4660	33p	BD97	1.20	MP5A77	45p	ATI-6000	95p	LM318AN	1.40	TA6637	2.47	7440	24p	74LS98	14p	74C92	1.34	4018	10p
40319	1.80	IC1734	10p	4661	33p	BD98	1.20	MP5A78	45p	ATI-6050	95p	LM318AN	1.40	TA6638	2.47	7441	24p	74LS100	14p	74C93	1.34	4019	10p
40320	1.80	IC1736	10p	4662	33p	BD99	1.20	MP5A79	45p	ATI-6100	95p	LM318AN	1.40	TA6639	2.47	7442	24p	74LS102	14p	74C94	1.34	4020	10p
40321	1.80	IC1738	10p	4663	33p	BD100	1.20	MP5A80	45p	ATI-6150	95p	LM318AN	1.40	TA6640	2.47	7443	24p	74LS104	14p	74C95	1.34	4021	10p
40322	1.80	IC1740	10p	4664	33p	BD101	1.20	MP5A81	45p	ATI-6200	95p	LM318AN	1.40	TA6641	2.47	7444	24p	74LS106	14p	74C96	1.34	4022	10p
40323	1.80	IC1742	10p	4665	33p	BD102	1.20	MP5A82	45p	ATI-6250	95p	LM318AN	1.40	TA6642	2.47	7445	24p	74LS108	14p	74C97	1.34	4023	10p
40324	1.80	IC1744	10p	4666	33p	BD103	1.20	MP5A83	45p	ATI-6300	95p	LM318AN	1.40	TA6643	2.47	7446	24p	74LS110	14p	74C98	1.34	4024	10p
40325	1.80	IC1746	10p	4667	33p	BD104	1.20	MP5A84	45p	ATI-6350	95p	LM318AN	1.40	TA6644	2.47	7447	24p	74LS112	14p	74C99	1.34	4025	10p
40326	1.80	IC1748	10p	4668	33p	BD105	1.20	MP5A85	45p	ATI-6400	95p	LM318AN	1.40	TA6645	2.47	7448	24p	74LS114	14p	74C100	1.34	4026	10p
40327	1.80	IC1750	10p	4669	33p	BD106	1.20	MP5A86	45p	ATI-6450	95p	LM318AN	1.40	TA6646	2.47	7449	24p	74LS116	14p	74C101	1.34	4027	10p
40328	1.80	IC1752	10p	4670	33p	BD107	1.20	MP5A87	45p	ATI-6500	95p	LM318AN	1.40	TA6647	2.47	7450	24p	74LS118	14p	74C102	1.34	4028	10p
40329	1.80	IC1754	10p	4671	33p	BD108	1.20	MP5A88	45p	ATI-6550	95p	LM318AN	1.40	TA6648	2.47	7451	24p	74LS120	14p	74C103	1.34	4029	10p
40330	1.80	IC1756	10p	4672	33p	BD109	1.20	MP5A89	45p	ATI-6600	95p	LM318AN	1.40	TA6649	2.47	7452	24p	74LS122	14p	74C104	1.34	4030	10p
40331	1.80	IC1758	10p	4673	33p	BD110	1.20	MP5A90	45p	ATI-6650	95p	LM318AN	1.40	TA6650	2.47	7453	24p	74LS124	14p	74C105	1.34	4031	10p
40332	1.80	IC1760	10p	4674	33p	BD111	1.20	MP5A91	45p	ATI-6700	95p	LM318AN	1.40	TA6651	2.47	7454	24p	74LS126	14p	74C106	1.34	4032	10p
40333	1.80	IC1762	10p	4675	33p	BD112	1.20	MP5A92	45p	ATI-6750	95p	LM318AN	1.40	TA6652	2.47	7455	24p	74LS128	14p	74C107	1.34	4033	10p
40334	1.80	IC1764	10p	4676	33p	BD113	1.20	MP5A93	45p	ATI-6800	95p	LM318AN	1.40	TA6653	2.47	7456	24p	74LS130	14p	74C108	1.34	4034	10p
40335	1.80	IC1766	10p	4677	33p	BD114	1.20	MP5A94	45p	ATI-6850	95p	LM318AN	1.40	TA6654	2.47	7457	24p	74LS132	14p	74C109	1.34	4035	10p
40336	1.80	IC1768	10p	4678	33p	BD115	1.20	MP5A95	45p	ATI-6900	95p	LM318AN	1.40	TA6655	2.47	7458	24p	74LS134	14p	74C110	1.34	4036	10p
40337	1.80	IC1770	10p	4679	33p	BD116	1.20	MP5A96	45p	ATI-6950	95p	LM318AN	1.40	TA6656	2.47	7459	24p	74LS136	14p	74C111	1.34	4037	10p
40338	1.80	IC1772	10p	4680	33p	BD117	1.20	MP5A97	45p	ATI-7000	95p	LM318AN	1.40	TA6657	2.47	7460	24p	74LS138	14p	74C112	1.34	4038	10p
40339	1.80	IC1774	10p	4681	33p	BD118	1.20	MP5A98	45p	ATI-7050	95p	LM318AN	1.40	TA6658	2.47	7461	24p	74LS140	14p	74C113	1.34	4039	10p
40340	1.80	IC1776	10p	4682	33p	BD119	1.20	MP5A99	45p	ATI-7100	95p	LM318AN	1.40	TA6659	2.47	7462	24p	74LS142	14p	74C114	1.34	4040	10p
40341	1.80	IC1778	10p	4683	33p	BD120	1.20	MP5A100	45p	ATI-7150	95p	LM318AN	1.40	TA6660	2.47	7463	24p	74LS144	14p	74C115	1.34	4041	10p
40342	1.80	IC1780	10p	4684	33p	BD121	1.20	MP5A101	45p	ATI-7200	95p	LM318AN	1.40	TA6661	2.47	7464	24p	74LS146	14p	74C116	1.34	4042	10p
40343	1.80	IC1782	10p	4685	33p	BD122	1.20	MP5A102	45p	ATI-7250	95p	LM318AN	1.40	TA6662	2.47	7465	24p	74LS148	14p	74C117	1.34	4043	10p
40344	1.80	IC1784	10p	4686	33p	BD123	1.20	MP5A103	45p	ATI-7300	95p	LM318AN	1.40	TA6663	2.47	7466	24p	74LS150	14p	74C118	1.34	4044	10p
40345	1.80	IC1786	10p	4687	33p	BD124	1.20	MP5A104	45p	ATI-7350	95p	LM318AN	1.40	TA6664	2.47	7467	24p	74LS152	14p	74C119	1.34	4045	10p
40346	1.80	IC1788	10p	4688	33p	BD125	1.20	MP5A105	45p	ATI-7400	95p	LM318AN	1.40	TA6665	2.47	7468	24p	74LS154	14p	74C120	1.34	4046	10p
40347	1.80	IC1790	10p	4689	33p	BD126	1.20	MP5A106	45p	ATI-7450	95p	LM318AN	1.40	TA6666	2.47	7469	24p	74LS156	14p	74C121	1.34	4047	10p
40348	1.80	IC1792	10p	4690	33p	BD127	1.20	MP5A107	45p	ATI-7500	95p	LM318AN	1.40	TA6667	2.47	7470	24p	74LS158	14p	74C122	1.34	4048	10p
40349	1.80	IC1794	10p	4691	33p	BD128	1.20	MP5A108	45p	ATI-7550	95p	LM318AN	1.40	TA6668	2.47	7471	24p	74LS160	14p	74C123	1.34	4049	10p
40350	1.80	IC1796	10p	4692	33p	BD129	1.20	MP5A109	45p	ATI-7600	95p	LM318AN	1.40	TA6669	2.47	7472	24p	74LS162	14p	74C124	1.34	4050	10p
40351	1.80	IC1798	10p	4693	33p	BD130	1.20	MP5A110	45p	ATI-7650	95p	LM318AN	1.40	TA6670	2.47	7473	24p	74LS164	14p	74C125	1.34	4051	10p
40352	1.80	IC1800	10p	4694	33p	BD131	1.20	MP5A111	45p	ATI-7700	95p	LM318AN	1.40	TA6671	2.47	7474	24p	74LS166</					



# Rapid Electronics

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## FIRST STEPS

The microprocessor has now been with us for many years although few have been used in projects for the hobbyist. Perhaps this is because their use has often been a more expensive solution than smaller chips in any given project, except perhaps the "hobby computer". Well, PE did its bit for computing with the publication of the CompuKIT UK101 design back in '78 and of course we have published various projects using dedicated micros. The PE *Bandbox*, *Car Computer*, *Robots* and *Telectric* being shining examples that are going strong on the retail market. However, the big breakthrough that microprocessors promised has been slow in coming to the hobbyist, until now!

This month we take the first of a series of steps to put that right. No, we are not going to expand our computer projects (even though the amazing *Ultimum Interface* system starts in this issue). What we hope to achieve is the use of micros to expand the range and sophistication of our projects without necessarily making them more expensive or more difficult to build.

We have decided that it's high time

the micro is used as a "regular" component by the hobbyist and high time that hobbyists understand the devices more fully. With this in mind we are launching *Micro-file* in this issue. This file system will consist of a pull out section, in the centre of each issue, describing a wide range of microprocessors. The section can be extracted from the issue and filed for easy reference.

The first *Micro-file* consists of an introductory four page article, which will form the covers of the file, plus the first Datasheet and backup article on the 8080A/8085A. Each month we will present a Datasheet plus back up information on a different chip, so that over a period of about a year the sheets will form into a file packed with data on all the popular microprocessors. A file full of valuable information that will enable the hobbyist to choose and use microprocessor chips in dedicated applications.

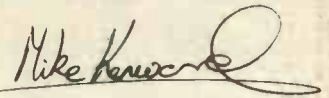
## CONTROL

In addition to *Micro-file* we are also proud to present the *Microcontroller*, which is not a project in the truest sense: the boards come ready built at

an unbelievable price! What we have done is commission Mike Tooley and David Whitfield to unravel the intricacies of the unit and write a monitor program for it, so that the hardware can be used as a "universal controller".

What we want you to do is to let us know how you have applied the unit (maybe to a robot, central heating or overall house electrical management system etc.) so that we can interest others in doing something similar. To encourage readers to do this, Display Electronics (the *Microcontroller* suppliers) are running a competition for *Microcontroller* uses and PE will publish any suitable winning entries — and pay for them of course! So here's your chance to obtain and use a micro system in a control application at a very low price and maybe reap a reward for your ideas.

We believe the time of the dedicated micro has now come for the hobbyist in a big way. We intend to provide the necessary information and more, exciting projects as the months go by.



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## Letters and Queries

We are unable to offer any advice on the use or purchase of commercial equipment or the incorporation or modification of designs published in PE. All letters requiring a reply should be accompanied by a stamped, self addressed envelope, or addressed envelope and international reply coupons, and each letter should relate to one published project only.

Components and p.c.b.s are usually available from advertisers; where we anticipate difficulties a source will be suggested.

## Back Numbers

Copies of most of our recent issues are available from: Post Sales Department (Practical Electronics), IPC Magazines Ltd., Lavington House, 25 Lavington Street, London SE1 0PF, at £1 each including Inland/Overseas p&p. Please state month and year of issue required.

## Binders

Binders for PE are available from the same address as back numbers at £4.60 each

to UK or overseas addresses, including postage and packing, and VAT where appropriate. Orders should state the year and volume required.

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Copies of PE are available by post, inland or overseas, for £13.00 per 12 issues, from: Practical Electronics, Subscription Department, Oakfield House, Perry Mount Road, Haywards Heath, West Sussex RH16 3DH. Cheques and postal orders should be made payable to IPC Magazines Limited.

Items mentioned are available through normal retail outlets unless otherwise specified. Prices correct at time of going to press.

## New Computer Systems

The Dragon 32 micro computer is just one of five new systems which have been launched this month. The others include the Micro 8 from the Japanese mainframe giant Fujitsu, the latest Colour Genie from Lowe Electronics and from two new companies, ORIC I and Jupiter Ace.

Based around the 6809E microprocessor the Dragon 32 has 32K of RAM, extended microsoft basic, eight graphic pages from 512 text points to 49,152 points, nine colours and a five octave range for both music and speech synthesis. The unit is available from Dragon Data Ltd., Queensway, Swansea Industrial Estate, Swansea (0792 580651). Price £199.50 including VAT.

The Micro 8 from Fujitsu boasts no fewer than three microprocessors; two 6809's which handle 640 x 200, 8 colour dot high resolution graphics, 8 x 8 matric block graphics and a Z80A for use with CP/M based software. Other features of the system include a real time clock, 32K of Microsoft Basic, 128K of total memory and provision for bubble memory. The Micro 8 is available from Minichip Limited, Enterprise House, Terrace Road, Walton, Surrey (09322 42777). Price £895 excluding VAT.

Lowe Electronics have added another Genie to their range of home computers the Colour Genie has 16K RAM, 16K ROM, 16K basic ROM, a maximum of 16 colours,

160 x 96 high resolution graphic characters with 128 programmable graphic characters and 64 preset characters. The Colour Genie is priced at £199 including VAT, Lowe Electronics, Mallock, Derbyshire (0629 2430).

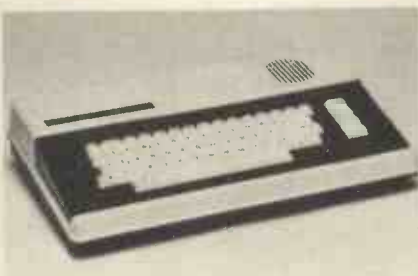
Oric I from Oric Products has been designed by Tangerine Computer Systems and is produced in two versions, both have 16 colours, one has 16K of RAM and is priced at £99 including VAT whilst the other has 48K of RAM and is priced at £169 including VAT. Oric I uses Microsoft basic, has a sound generator chip covering six octaves and a display resolution of 24 rows x 40 characters.

The Jupiter Ace which has been designed by two ex-Sinclair men uses a specially adapted version of the compiled language FORTH. The unit has 8K of ROM and 3K of RAM a memory mapped 32 x 24 character display, a programmable sound generator and a fast cassette interface.

Priced at £89.95 including VAT and p&p the Ace comes complete with a mains adapter, cassette and TV leads and a manual. Jupiter Cantab. 22 Foxhollow, Bar Hill, Cambridge.



ORIC I



The Colour Genie



The Dragon 32



Fujitsu Model 8

## POINTS ARISING . . .

### AUDIO ANALYSER (August-October '81)

1. In Fig. 13, the orientation of the diode D1 is incorrect, and this component should be reversed. The circuit diagram is correct in this respect.
2. In Fig. 17, the component layout for the backplane, the orientation of C115 and C116 is incorrect. Both components should be reversed.
3. In Fig. 17, the component layout for the backplane, C114 is shown connected between rails 1 and 3 (the +7.5V supply), rather than between rails 1 and 2 (the +5V supply), as it should be connected.
4. In Fig. 29, the component layout for the microphone preamplifier, IC1 is shown incorrectly orientated, and should be rotated so that pin 1 is adjacent to C1. Also, the capacitor shown marked C7, and positioned near to IC1, should be marked C4.
5. In the parts list for the microphone preamplifier, C7 should be shown as 47µ 16V tantalum, and C8 as 4n7 disc ceramic.

### MICROBUS (SEPT '82)

It is stated that the output of 0-255 corresponds to an analogue input of 0-5V; in this particular case this is not correct.

It can be seen from the circuit diagram that pins 7 and 8 of the ZN427 have been joined; this in effect brings into use the internal reference voltage of the chip which is 2.55V. The statement should therefore be "The output of 0-255 corresponds to an analogue input of 0-2.55V".

### COMBO AMPLIFIER (Aug.-Oct. '82)

A complete set of semiconductors is available for this project from Hart Electronic Kits Ltd., Penylan Mill, Oswestry, Shropshire SY10 9AF. Tel: 0691 2894.



Jupiter Ace



# MARKET PLACE

## BECKMAN DMM'S

Beckman Instruments has introduced two handheld digital multimeters; the 3½ digit T100 and T110 models, both of which offer five d.c. voltage ranges from 200mV to 1000V, five a.c. voltage ranges from 200mV to 750V, six d.c. and a.c. current ranges from 200µA to 10A and six resistance ranges from 200 ohm to 20 Mohm.

Of special interest is the direct 10A current range which obviates the need for external shunts. The resistance ranges can be switched to either low power for measuring in electronic circuits without turning on diodes and transistor junctions, or to high power for measuring resistances in electrical circuits or out of circuit. Both instruments also feature a special range for testing diodes and transistors which provides an accurate measure of the forward voltage drop in the diode junctions.

Diodes and transistors can also be checked in or out of circuit. The T110 also incorporates a buzzer for continuity testing and circuit tracing.

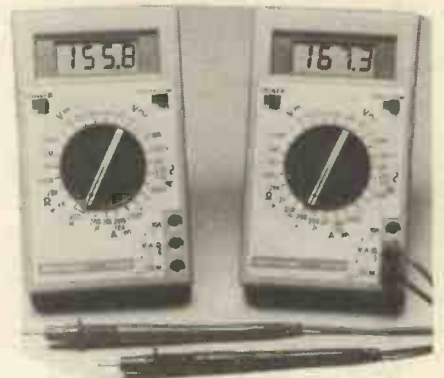
A high 10 Mohm input impedance ensures that measurements are hardly affected by circuit loading, and effective RF shielding guards against external fields. Accuracies are guaranteed for one year, and eventual recalibration is very simple, as it only requires the adjustment of two potentiometers.

All functions and ranges are selected with a single rotary switch and the 3½ digit l.c.d. features automatic decimal point positioning, polarity, overrange and low battery indication. The instruments will operate continuously for 200 hours from one standard 9V battery.

The two models T100 and T110 are priced at £49.00 and £59.00 respectively

excluding VAT and p&p.

Beckman Instruments, Mylen House, 11 Wagon Lane, Shelden, Birmingham (021 742 77611).



## Satellite TV Receiver

When you arrive at Alexandra Pavilion for the Electronic Hobbies Fair, the first thing you will see is a Luxor satellite TV receiver dish like the one shown opposite. The system with its two metre dish will be set up to receive programmes from the Russian Ghorizant-3 satellite in geostationary position 53 degrees E. The dish will be linked to a Luxor receiver system and TV inside the Pavilion so that visitors can see the results; this is just one of the special exhibits that is being arranged.

The other photo below was taken during the third International Road Racing Show. It gives a good impression of the inside of the hall. What is not apparent from this photo are the facilities available; these include three bars, two buffets, comprehensive toilet facilities—including a disabled toilet, first aid room and a baby changing room. Of course all these are purpose built and virtually brand new. In addition there will be extra cafeteria facilities with an additional area of tables and chairs, so no one should want for anything.

The largest supplier of components to the hobbyist—Maplin Electronic Supplies Ltd.—had this to say about the Fair: "The show coming in November is the one we are all excited about, here at Maplin. It's the Electronic Hobbies Fair, a brand new show, that is going to be very different from anything you've ever seen before. As well as the usual electronic stands, there will be computers, model control, amateur radio, CB and practical hi-fi.

"But the big plus about this show is that the organisers have really gone to town to provide you with dozens of extra exciting things to see and do."

Maplin will be devoting part of their stand to a bank of Atari computers, each running a different piece of software, so visitors will be able to play with them or just stand and watch.

Electronic Hobbies Fair, Alexandra Pavilion, November 18th to 21st. For more details and a 50p off voucher, see page 75. Keep watching PE for more details of the Fair; it will be the liveliest and most professionally organised event ever to be staged in this field.



Above: The Luxor satellite TV receiver dish

Below: Inside view of the new Alexandra Pavilion



## ZON X-81 SOUND UNIT

A wide range of sound effects can be added to your ZX-81 with the ZON X-81 Sound Unit, now available from BI-PAK.

The unit is based on a three-channel-plus-noise sound chip and is so designed that the pitches and volumes of the three channels and the overall attack/decay



envelope can be controlled by simple BASIC statements. By this means, piano, organ, bells, helicopters, lasers, explosions etc., can be simulated and easily added to existing programmes.

ZON X-81 is housed in a neat black plastic case with loudspeaker and manual volume control (in addition to programmed volume) and simply plugs in between the rear of the ZX-81 and its RAM pack and/or

printer (if fitted). No dismantling, wiring, soldering, batteries, power supplies or leads are required.

An instruction booklet explains the operation of the unit and a number of example programs of useful sounds is also included.

The ZON X-81 is available from: BI-PAK Semiconductors, P.O. Box 6, Ware, Herts. 0902 3442 and is priced at £25.95 including postage and VAT.

## Briefly...

Namal Electronics have developed a speech synthesizer which can be directly connected to the ZX81 or the Spectrum.

The synthesizer has a standard dictionary of about 600 words stored in an EPROM and the user can add to these by utilising the units 2K static RAM. The unit is programmed via the host computer, needing only two instructions per word.

Based on a phonetic speech synthesizer made by Votrax of Detroit the unit which measures 150 x 180 x 35mm comes complete with an integral loudspeaker, volume control and ribbon connector. There

is also provision for driving an external loudspeaker or amplifier.

The Super Talker is priced at £49.95 for the ZX81 and £59.95 for the Spectrum (prices excluding VAT).

Namal Electronics, 25 Gwydir Street, Cambridge (0223 355404).

Readers may be interested to know that Premier Publications are intending to do for the Dragon what they have done for the UK101. They are already supplying Dragons, writing software and generally getting inside the unit in preparation for servicing and the design of various add on kits. This back up will no doubt add to the Dragons attraction. Premier Publications, 208 Croydon Road, Anerley, London SE20 7YX.

The assets of EDA-Sparkrite Limited, which went into voluntary receivership in July 1982, have been acquired by STADIUM LTD. Sparkrite manufacture electronic ignition, car security systems and in-car computers and is based in Walsall, West Midlands.

This change of ownership is a major turning point for Sparkrite after the difficult circumstances of the last few months. Sparkrite (A Division of Stadium Ltd.), 82 Bath Street, Walsall WS1 3DE. 0922 614791.

## Countdown ...

Please check dates before setting out, as we cannot guarantee the accuracy of the information presented below. Note: some exhibitions may be trade only. If you are organising any electrical/electronics, radio or scientific event, big or small, we shall be glad to include it here.

**Science and Technology in 19th Century Germany** Oct. 15–Dec. 14 (weekdays 12–8pm and Sats. 10–1pm). Goethe Institut, 50 Princes Gate (Exhibition Road), London

**Video Show** Oct. 16–18. West Cntr. Hotel, London Z1

**Computer Graphics** Oct. 19–21. Royal Gdn. & Bloomsbury Cntr. London O

**Testmex** Oct. 26–28. Wembley Conf. Cntr. T

**BEX Southampton** Oct. 27–28. Polygon Hotel K

**ISSEC (Safety, Security, Fire)** Nov. 9–11. Royal Dublin Society Hall, Ireland V

**BEX Plymouth** Nov. 10–11. Holiday Inn K

**Compec** Nov. 16–19. Olympia Z1

**Hobby Electronics Fair** Nov. 18–21. Alexandra Pavilion, London Z1

**INTRON** Nov. 23–25. RDS Dublin, Ireland V

**BEX Bristol** Nov. 24–25. Holiday Inn K

**Northern Computer Fair** Nov. 25–27. Belle Vue, Manchester Z1

**Christmas Holography (+ items for sale)** Dec. 2–Mar. (1983) Light Fantastic Gallery, London A8

**ElectroNORTH** Dec. 7–9. Harrogate Supercentre Q

**IT82 (Information Technology Year Conf.)** Dec. 8–9. Barbican O

**Continuous events at the National Microprocessor & Electronics Cntr.** (nr. Tower of London) L1

**Peripherals** Feb. 2–4 1983. Cunard Int. Hotel, Hammersmith, London Z1

**BEX Bournemouth** Feb. 9–10 1983. The Pavilion K  
**Microsystems** Feb. 23–25 1983. West Cntr. Hotel, Fulham, London Z1

**CAD North** Mar. 1–3 1983. Belle Vue Ex. Cntr. Manchester Z1

**Mailing Efficiency** Mar. 1–3 1983. Bloomsbury Cntr. Hotel, London Z

**Local Networks** Mar. 8–10 1983. Royal Lancaster Hotel, London O

**Laboratory Edinburgh** Mar. 16–17 1983. Assembly Rooms, George St. E

**Brighton Electronics** March 1983 T

**BEX Leeds** Mar. 16–17. Dragonara Hotel K

**INSPEX** Mar. 21–25 1983. National Exhibition Cntr. Birmingham International Z1

**Sensors & Systems** Mar. 22–24 1983. The Forum, Wythenshawe T

**Compec Wales** Mar. 22–24 1983. Cardiff University Z1

**ETM (Electronic Test / Measurement)** Mar. 22–24 1983. The Forum, Wythenshawe, Manchester T

**Laboratory Manchester** Mar. 23–24 1983. New Century Hall, Corporation St. E.

**American Holography** Mar.–June inc. Light Fantastic Gallery, Covent Garden, London A8

**All Electronics Show** April 19–21 1983. Barbican Cntr. London E

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- Revolutionary microcomputer language FORTH.
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The Ace is set apart from all other personal computers on the market by its use of a revolutionary language called 'FORTH'. Some computer languages are easy for humans to understand, others are easy for computers; FORTH is most unusual in being both. Its underlying principles are so simple that it takes even a newcomer to computers only a few minutes to learn how to do calculations on the Ace, yet the very same principles are powerful enough to allow you to invent your own extensions to the language itself.

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Leading computer Designers Richard Altwasser and Steven Vickers have a reputation for pushing technology forwards. After playing the major role in creating the ZX Spectrum they formed Jupiter Cantab to develop their latest brainchild the Jupiter Ace. **JUPITER CANTAB, 22 FOXHOLLOW, BAR HILL, CAMBRIDGE CB3 8EP**

### Technical Specification

#### Hardware

##### Processor/Memory

Z80A running at 3.25 MHz.  
8K bytes ROM 3K bytes RAM.

##### Input

40 moving-key keyboard with auto-repeat on every key.

##### Output

Memory-mapped 32 x 24 character display with high resolution user graphics. Output to drive normal UHF TV set on channel 36.

##### Sound

Provided by internal loudspeaker.

##### Cassette

Load Save & Verify at 1500 baud, separate data storage.

#### Software, FORTH

##### Data Structures

Integer, Floating point and String data may be held as constants, variables or arrays with multiple dimensions and mixed data types.

##### Control Structures

IF-THEN-ELSE, DO-LOOP, BEGIN-WHILE-REPEAT, BEGIN-UNTIL, all may be mixed and nested to any depth.

##### Operators

Mathematical +, —, X, ÷.  
Logical AND, OR, NOT, XOR.  
Comparison <, >, =.

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FORTH words may be listed, edited and redefined. Comments are preserved when words are compiled.

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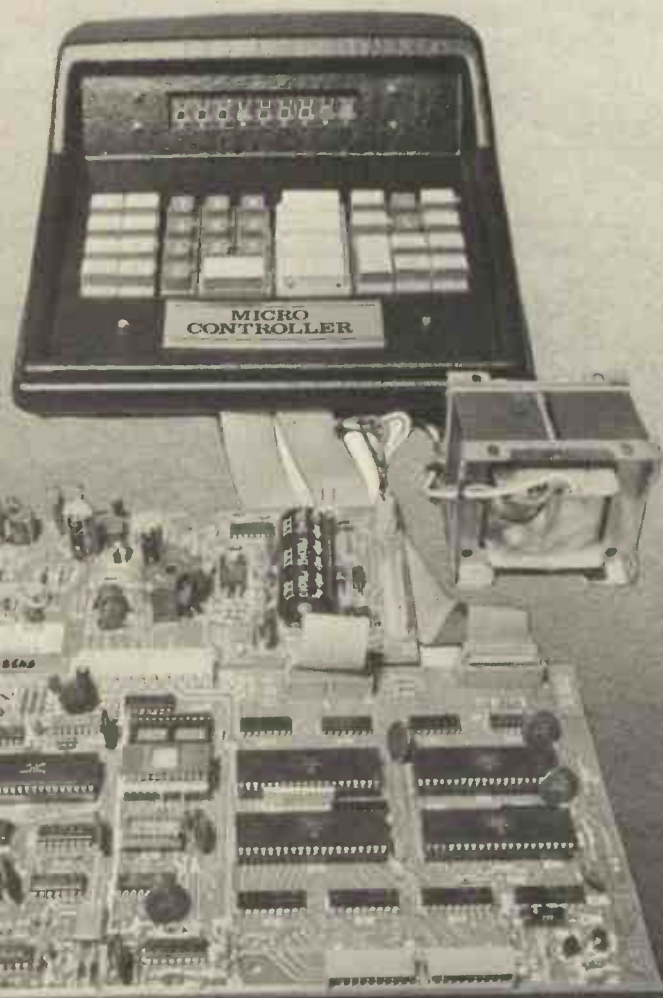
PE

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# MICRO CONTROLLER

MICHAEL TOOLEY B.A.

DAVID WHITFIELD M.A. M.Sc.



## PART ONE

**T**HE PE Microcontroller is an assembled project which is based around the 6800 micro.

Long term success for any product is usually assured if it is cost effective and if it can easily be adapted to meet any new requirements. The more adaptable the tool, the more successful and durable it is likely to be. Nature provides an example of a highly versatile tool in the human hand, which is capable of performing an extremely wide range of intricate tasks. It is, however, only with the advent of the microprocessor that the idea of the general purpose electronic controller has become a practical proposition. Such controllers still have a long way to go before they are able to rival the flexibility and ease of programming of the human hand. Programmable controllers are, nevertheless, now able to offer some significant advantages over the dedicated controllers of the last decade, and increasingly at prices which are acceptable to the home constructor.

This Microcontroller was originally designed to form the intelligent 'heart' of a mass produced commercial product. The basic design, however, followed conventional guidelines, and the final controller is a good example of a general purpose programmable controller. A wide range of control facilities are available within the basic controller, and users should have little difficulty in adapting it (often simply by writing a suitable control program) to a wide range of new applications. Practical applications will be discussed in later issues, together with details on how to program the 6800 microprocessor which is the CPU in the Microcontroller.

### MICROCONTROLLERS

A microprocessor which is used to control a system (i.e. a microcontroller) must be capable of accepting input information, responding, and outputting appropriate signals to implement the required control action. A typical microcontroller arrangement is shown in the block diagram of Fig. 1.1. It can be seen from this figure that the input/output signals may require signal conditioning so that their forms and levels become compatible with the input/output interface elements. In many cases, however, no such conditioning is necessary, and indeed it is one of the aims of any general purpose microcontroller that the amount of conditioning circuitry is kept to a minimum. In the 6800 microprocessor family, interfacing is greatly simplified by the availability of a range of versatile and programmable interface adaptors, making the 6800 well suited to controller applications. The four parallel interface adaptors in the system can each provide up to 16 separately controllable input/output lines.

An important feature of any programmable controller is that its function may be changed by modifying its control program. Thus, in many situations, the age-old call of "Back to the drawing board", becomes "Back to the keyboard". This feature also allows the function of a controller to be modified during production without the need for any changes to be made to the hardware. This is one of the reasons that the use of erasable PROMS in early production units is



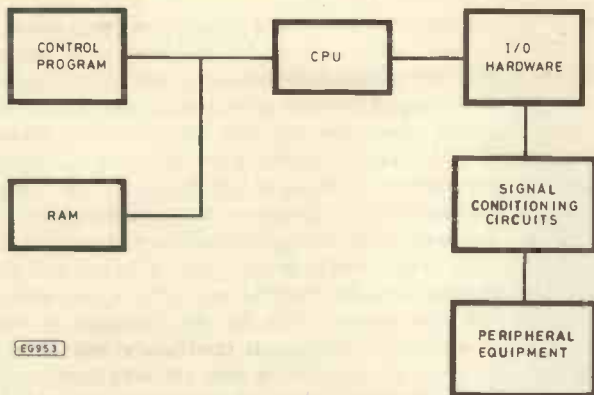


Fig. 1.1. Typical microcontroller arrangements.

so popular! Alternatively, the same hardware may be supplied to different customers, but with different control programs to enable them to perform significantly different tasks. An example of this is the way in which a manufacturer will market a range of pocket calculators all in the same case, using the same keyboard and internal hardware, but which are personalised for different applications (engineering, finance, surveying, etc.).

This system is rather more than a simple microcontroller. The keyboard and display which are provided may be used in two different ways. The first way uses them as part of the control application, with the keyboard for inputting commands, and the display for information output. The keyboard and/or display may alternatively be unplugged and different peripheral hardware substituted, in addition to that connected to the usual control ports. Such applications will have user-defined control programs to perform the necessary functions, e.g. central heating/lighting control, multi-program time switches, PROM programming, etc.

The second way in which the keyboard and display may be used is in conjunction with the DISBUG monitor program, which is supplied in permanent memory. This allows the user to develop his own applications control programs, and provides facilities to control the program execution, and to debug the program. The user program itself may then re-assign the keyboard and display for application-dependent functions. The DISBUG program cannot be overwritten by user programs, and the user can always return to DISBUG to continue debugging of an applications

program which has run out of control.

The applications for the Microcontroller are therefore limited only by the ingenuity and imagination of the user; the best application offered for the unit is the subject of a competition details of which are given at the end of this article.

### SYSTEM HARDWARE DESCRIPTION

The Microcontroller is a 6800 microprocessor-based system which is ideally suited to programmed control in a wide variety of applications. A block schematic for the 6800 configured in a conventional fashion is shown in Fig. 1.2. This diagram shows the 6800 configured in a conventional fashion with an 8-bit data bus, 16-bit address bus, and a control bus. The arrangement supports the full 64Kbyte addressing range of the 6800, while leaving scope for further expansion.

The 6800 is designed to use programmable memory-mapped peripheral devices. The system has four programmable interface adaptors (PIAs), each of which has 16 individually programmable input/output lines. One of these PIAs is dedicated to the keyboard, the second drives the gas discharge display, and the remaining two are available for user applications. The capabilities of the PIA devices are discussed in greater detail in a subsequent section, and at length in a later issue.

The Microcontroller has 1024-bytes of RAM, which is provided with integral battery back-up to safeguard against program loss in the event of power failure. The board has facility for the inclusion of a 32-byte ROM, originally intended for "personalising" units. This ROM is unused in the basic system. Permanent memory is provided for storage of the monitor program (DISBUG) by a 2048-byte EPROM. The circuit configuration does, however, allow the use of up to 8196 bytes of permanent memory.

An address map for the system is shown in Fig. 1.3. The addresses shown are all given in hexadecimal notation; areas shown with dotted line boundaries are available for use, but are not utilised in the basic unit. Users should be aware that full address decoding is not always employed, and that some address images do occur.

Two crystal controlled clocks are incorporated in the Microcontroller. The first is the master system clock which provides the basic timing for the microprocessor and the buses. In addition, it incorporates facilities for synchronising the start-up and reset sequences. The second oscillator is a real time clock, operating at 1Hz, which is connected to the display PIA. This clock may be configured under program

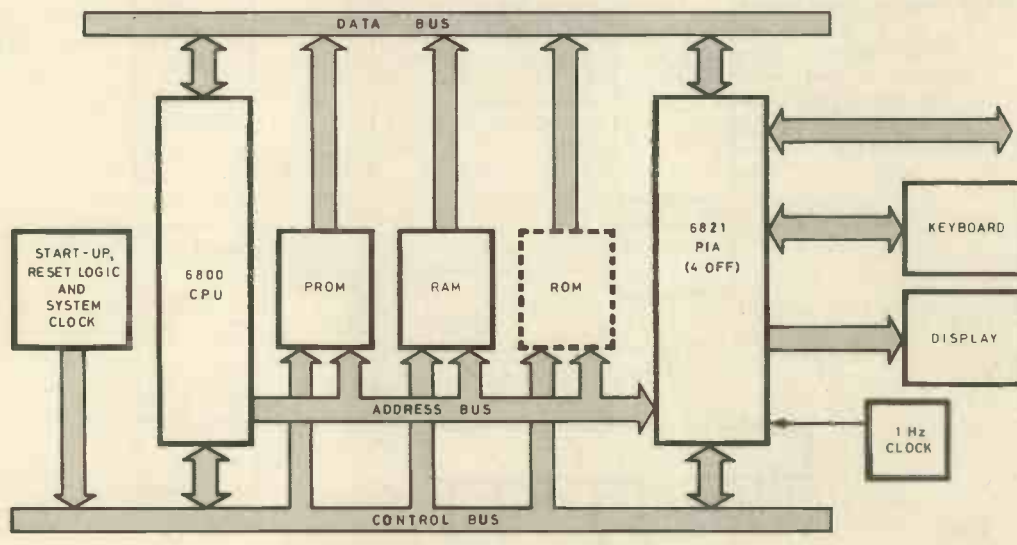
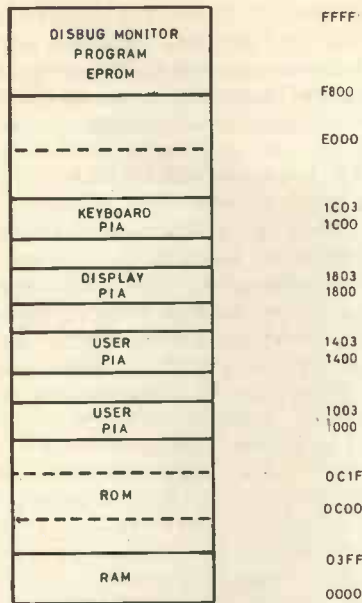


Fig. 1.2. Block schematic of the Microcontroller.



EG954

Fig. 1.3. Address map for the Microcontroller

control to provide regular interrupts, which are essential for any time dependent applications.

Separate from the main Microcontroller board are the gas discharge display, keyboard, power supply and mains transformer. Peripheral equipment to be controlled is connected to the main board by a multi-way ribbon cable.

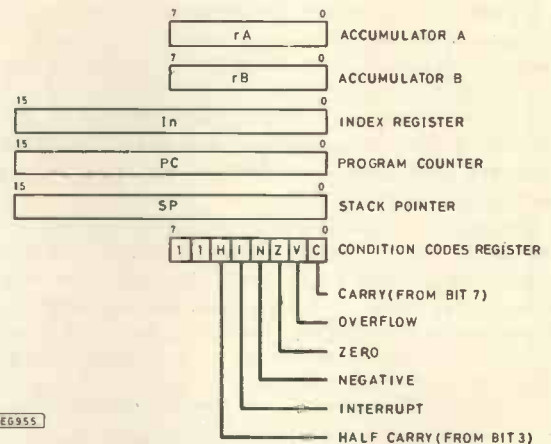
### ARCHITECTURE OF THE 6800 FAMILY

The 6800 is an 8-bit microprocessor whose internal architecture is shown in Fig. 1.4. The device is supplied in a

40-pin d.i.l. package, and requires only a single +5 volt supply. The main processor requires a 2-phase non-overlapping clock to control its operation. The basic processor cycle time is one quarter of the oscillator's crystal frequency.

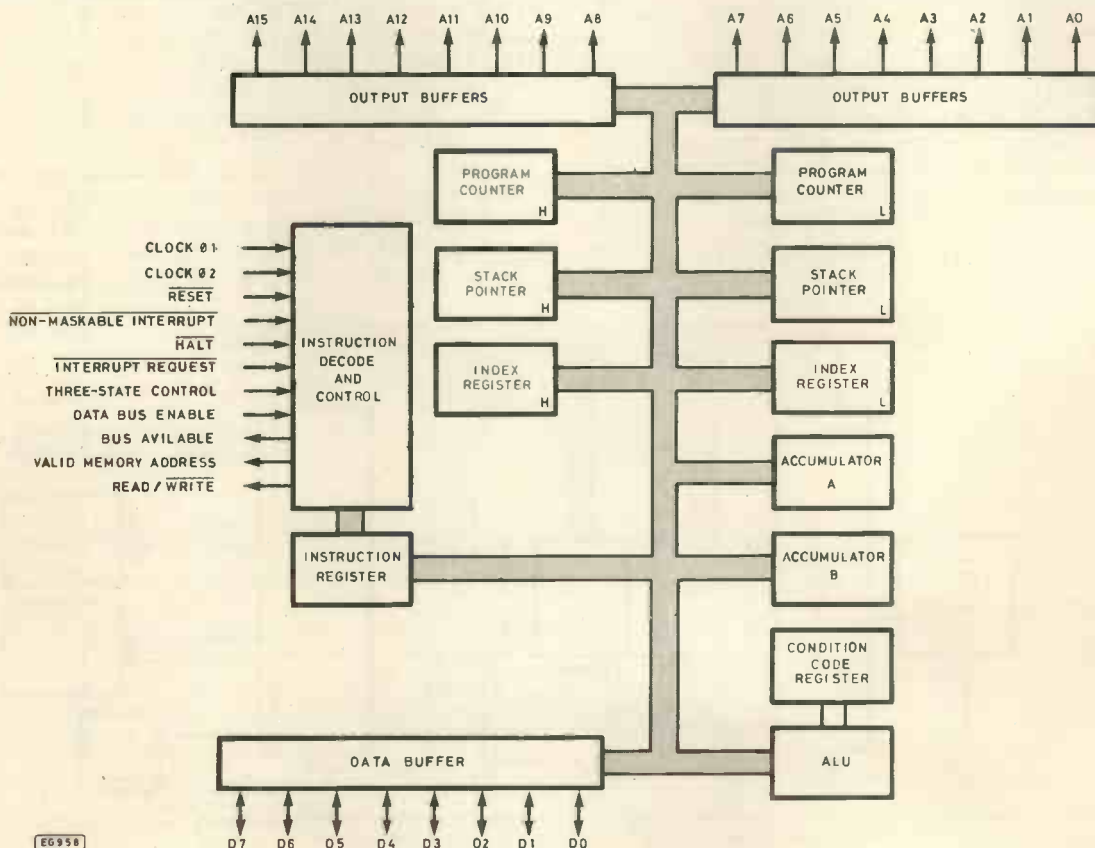
The CPU device includes an 8-bit bidirectional buffer for the data bus, and a 16-bit unidirectional address bus buffer. These buffers will each drive a single TTL load; each standard peripheral device imposes a significantly lower load.

The programming model, given in Fig. 1.5, shows the registers which are available to the user. Two general purpose 8-bit accumulator registers (rA and rB) are provided for arithmetic and logic operations. A 16-bit index register (In) is available for indexed addressing modes of many instructions. The 16-bit program counter (PC) is maintained automatically by the CPU, and holds the memory address of the next instruction to be executed. The 16-bit stack pointer (SP)



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Fig. 1.5. 6800 programming model.



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Fig. 1.4. Internal architecture of the 6800.



indicates the next free location on the push-down user stack. The stack pointer must be initialised by the user, but thereafter is maintained by the CPU. Finally, the condition code register (CCR) is used to indicate CPU and interrupt status. Only six bits of the CCR are used, the remaining two being permanently set HIGH.

Arithmetic and logic operations are performed by the arithmetic and logic unit (ALU). Operations may take one or two operands, depending on the instruction. Operands may be the contents of registers and/or memory locations. ALU operations set various bits within the CCR, depending on the instruction and the result of the operation.

The 6800 provides interrupt facilities for software interrupts, user interrupts, non-maskable interrupts and also for system reset. User interrupt requests may be masked under program control. The addresses of the interrupt service and reset service routines are defined as the top eight bytes of the 6800's memory. The instruction decode and control unit handles interrupt requests, provides bus control signals and executes instructions. Details of programming the 6800 will be given next month.

The 6821 peripheral interface adaptor (PIA) provides a universal means of parallel interfacing to peripheral equipment. The PIA interface uses two 8-bit bidirectional buses and four control/interrupt lines. Fig. 1.6, shows the internal architecture of the 6821 PIA. The CPU sets up the PIA's functional configuration under program control. The peripheral data lines, PA0 to PA7 and PB0 to PB7, can each be configured either as an input or as an output. Consequently, any combination of inputs and outputs is possible, up to

the maximum of 16 lines. The four control/interrupt lines, CA1, CA2, CB1 and CB2, may also be configured to act in one of several modes for handshaking with peripheral equipment. All PIA peripheral data lines may drive up to two TTL loads, with CMOS drive capability on PA0 to PA7.

Internally, the 6821 contains two independent sections each comprising an output register, control register, and data direction register. Separate interrupt status control is provided, together with an interface buffer, for each group of eight peripheral lines. Data is transferred to the output registers during a CPU WRITE operation via the data bus buffers and input register. Where a particular peripheral line has been programmed as an output, data will be transferred to this line. Where a particular line has been programmed as an input, data will be transferred to the system data bus from this line during a CPU READ operation. Multiple chip select lines simplify the selection of a particular PIA where several have been used. Timing is provided by an ENABLE signal derived from the 6800. Part of the address bus is externally decoded to select the required PIA, and usually the two least significant address bits are used to select the appropriate register within the PIA.

### DISBUG MONITOR FACILITIES

A program of instructions is required by the CPU in order to make any use of the hardware facilities offered by an intelligent controller. It is this feature which distinguishes between dedicated and programmable controllers. The function of a programmable controller may be changed simply by the installation of a different control program; this may be

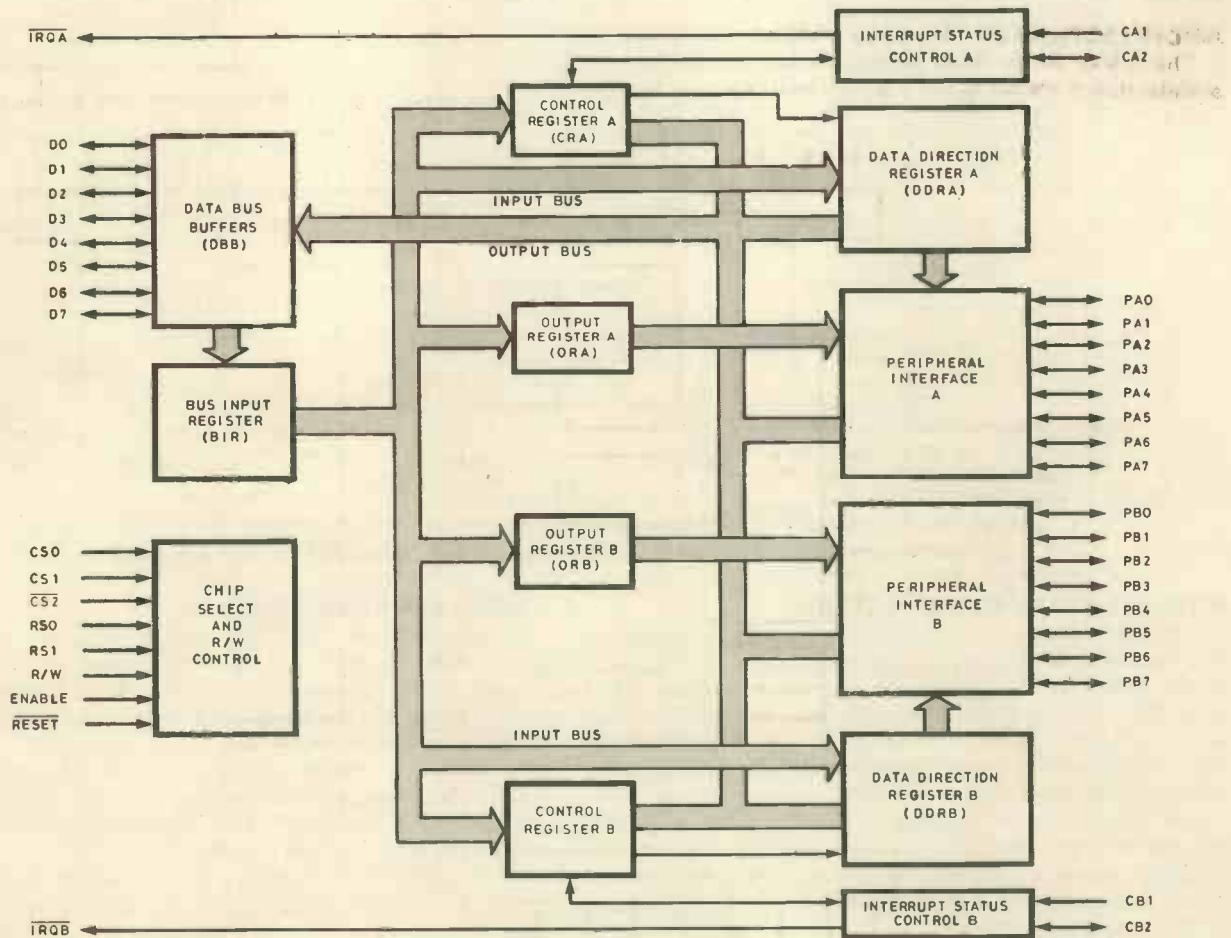


Fig. 1.6. Internal architecture of the 6821 PIA.

accomplished in a number of ways. In mass production applications, programs are written on development systems and then stored in the permanent memory of the controller. The function of the Microcontroller, however, is user-defined and therefore facilities must be provided to enable the user to develop his own control programs. These facilities are provided by the DISBUG monitor program which resides in permanent memory, and thus cannot be over-written. User programs are stored in the RAM area, allowing them to be developed in a modular fashion.

The facilities provided by a monitor program should include the following:—

1. An interface between the user and the system.
2. The means to input and modify programs.
3. The ability to control the execution of programs.
4. Debugging facilities.

The interface between the user and the system is provided by the keyboard and the display. The DISBUG monitor scans the keyboard for user commands, and uses the display to output results. The keyboard layout is shown in Fig. 1.7.

The keys are essentially divided into two major groups; numeric keys and command/control keys. The command/control keys are associated with five major groups of monitor functions:—

1. Memory examine and change.
2. Register examine and change.
3. Setting of breakpoints.
4. Memory presets.
5. User program control.

The facilities offered are outlined below and will be examined in detail in a later issue.

## REGISTER EXAMINE AND CHANGE

The user may examine the contents of any of the 6800's registers after a breakpoint has been encountered. The REGISTER key is used to invoke the register editor, and changes may then be made before the program proceeds from the current breakpoint. Registers are displayed in a cyclic fashion, as shown in Fig. 1.8. The 16-bit registers are displayed in two stages, lower and upper bytes in turn. Other editing facilities are similar to those in the memory editor.

## MEMORY PRESETTING

Areas of RAM may be present to user-defined values by using the preset editor. This facility is useful for initialising RAM to known values, e.g. all zeroes, filled with NOP instruction codes, etc. The preset editor is entered using the PRESET key, and pointers are then set up to indicate the bottom and top of the RAM area to be filled. The preset value is input, and this is then written to each location in the range specified, including the two extreme addresses.

## SETTING BREAKPOINTS

Temporary halts or breakpoints are a useful aid to debugging user programs. They enable the programmer to split the program into convenient blocks so that each block may be tested separately. Breakpoints are set and reset using the breakpoint editor, which is entered by pressing the BREAKPOINT key. Up to four breakpoints may be set in the user program and, when a breakpoint is encountered, the user may examine the register contents using the register editor.

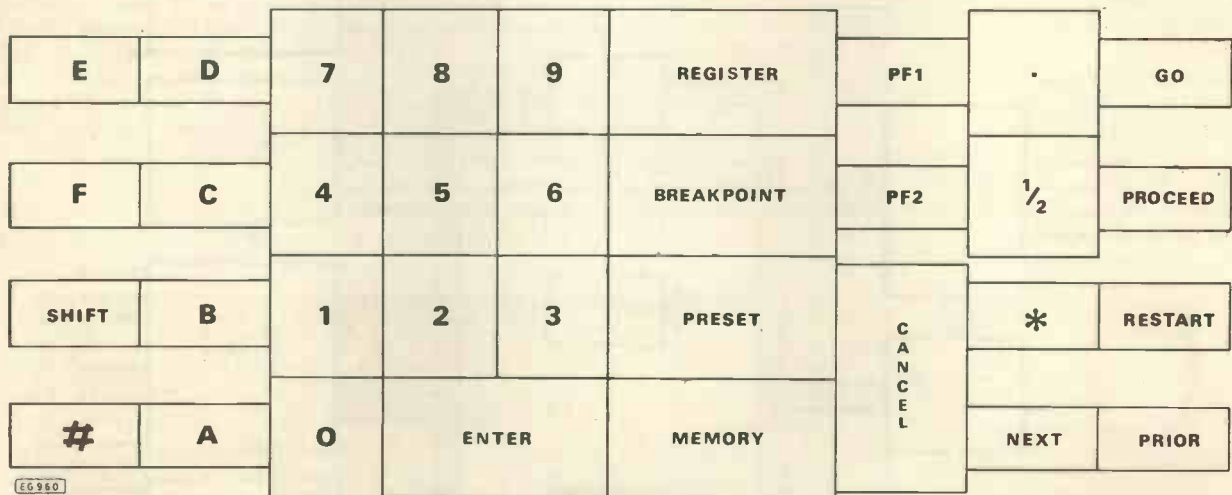


Fig. 1.7. DISBUG keyboard layout. Note this artwork can be cut out to label the user definable key tops.

## MEMORY EXAMINE AND CHANGE

The contents of any memory location may be examined and (optionally) changed using the memory editor. This function is also used for entering programs into the user RAM area. The user may specify any address in the 6800 address space, i.e. 0000 to FFFF. Over-writing the DISBUG RAM area may have unforeseen consequences, although writing to ROM addresses will have no effect.

The memory editor is invoked by pressing the MEMORY key, and the numeric keys 0 to F are then used to specify the four-digit memory address to be examined. The contents may then be changed, if required, and the editor then exited, or the next/previous memory location examined. The CANCEL key allows the user to abandon any uncompleted memory change.

## USER PROGRAM CONTROL

**GO:** The user program is started using the GO function key. After pressing GO, the user enters the start address from which program execution should commence. The ENTER key is used to initiate execution, or CANCEL may be used to abandon the function.

**PROCEED:** The user program may be caused to continue from a breakpoint using the proceed function. After PROCEED is pressed, ENTER restarts program execution, or CANCEL abandons the command.

**RESTART:** The RESTART key is used to re-initialise the DISBUG monitor program. The DISBUG RAM area is reset to its initial values, and the welcome message appears. The user RAM is unaffected by this function. A restart has the same effect as entering DISBUG at power-up, but without



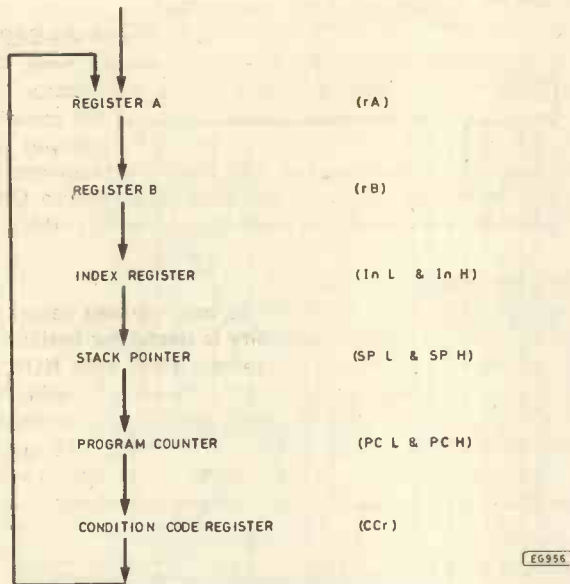


Fig. 1.8. Register display sequence.

the need to interrupt the mains supply. The CANCEL key may be used in place of the ENTER key to abandon a restart. This function is particularly useful for re-initialising the keyboard and display PIA's.

### SOFTWARE FACILITIES

Various software aids are available within the DISBUG monitor program to assist the user in developing control programs. These aids are subroutines which may be called from RAM based code. The functions and interfaces for these routines will be described in a later issue.

### CIRCUIT DESCRIPTION

The circuit diagram for the Microcontroller is shown in two parts. The CPU, clocks, memory and the CPU side of the PIAs appear in Fig. 1.9. The keyboard, display, output drivers and the peripheral side of the PIAs are shown in Fig. 1.10.

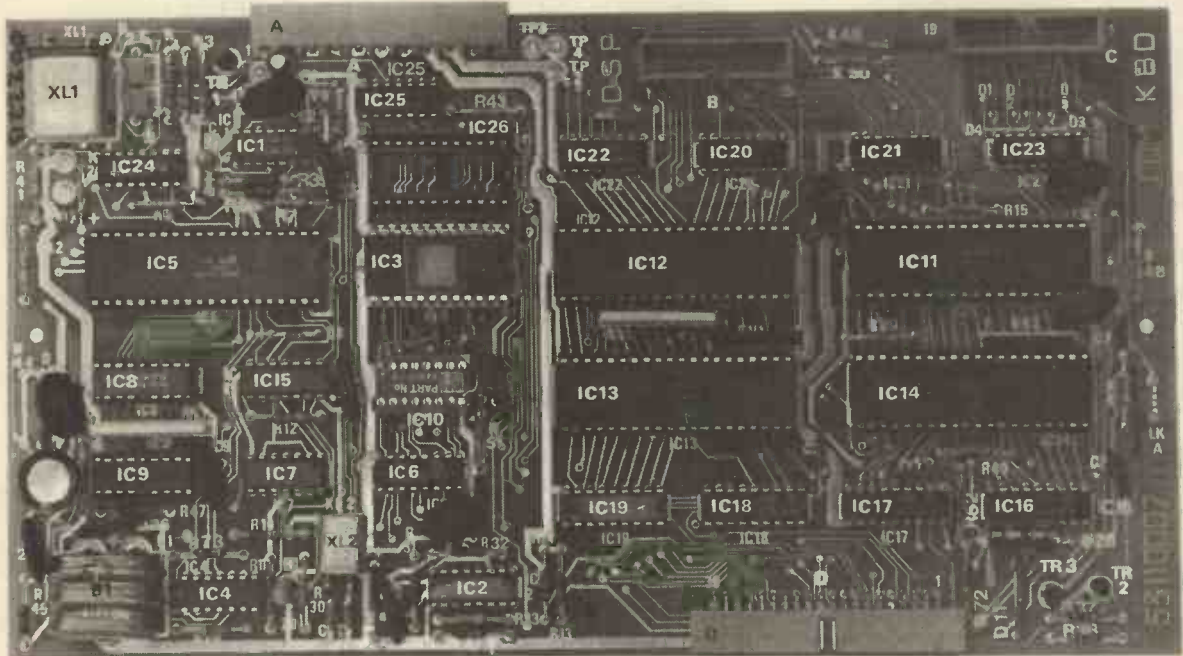
When interfacing in control applications, the primary concern is with the logic shown in the second of these drawings. Applications programs, and the monitor program used to enter and control these programs, reside in the memory and are executed by the hardware shown in the first figure.

A discrete Colpitts crystal oscillator, formed by TR1 and associated components, provides the master timing signal. The crystal operates in series resonant mode to produce a signal at 3.579MHz. The oscillator output is taken from the collector of TR1 and applied to the clock generator, IC1. The clock generator provides the necessary non-overlapping two-phase clock, producing a CPU cycle frequency of 894.75kHz, i.e. at one quarter of the frequency of the master timing signal. Outputs are also provided for memory synchronisation, and for the system reset signal.

The 6800 CPU is arranged in a conventional small system configuration, with no additional bus buffers required. Memory address decoding is provided by IC6 and IC25a. The HALT and NMI interrupt request lines are unused, and are therefore held HIGH by R7 and R5, respectively. The IRQ user interrupt request line is connected to the four PIAs, any one of which may assert this line, thereby causing a user interrupt request.

The four PIAs, IC11, IC12, IC13 and IC14, are all connected to the full width of the CPU data bus. Also connected to the PIAs are the system RESET signal from the clock generator, and the CPU R/W signal. The address decoder, IC6, provides an active low chip select (CS) to a PIA when one of its register addresses is output by the CPU. Four of these chip select outputs from IC6 are connected to the appropriate CS2 pin on the four PIAs. The CS0 and CS1 pins on all PIAs are unused, and are connected to +5 volts via R39. The two least significant lines of the address bus (A0 and A1) are connected to the register select inputs (RS1 and RS0, respectively) on the PIAs. The correspondence between the address value and the PIA register selected is shown in Table 1. A0 and A1 have no effect on the PIAs unless the CS2 in the PIA in question is held LOW by the address decoder.

The 1Hz real time clock is provided by IC2. This device is a 24-stage frequency divider which incorporates a conven-



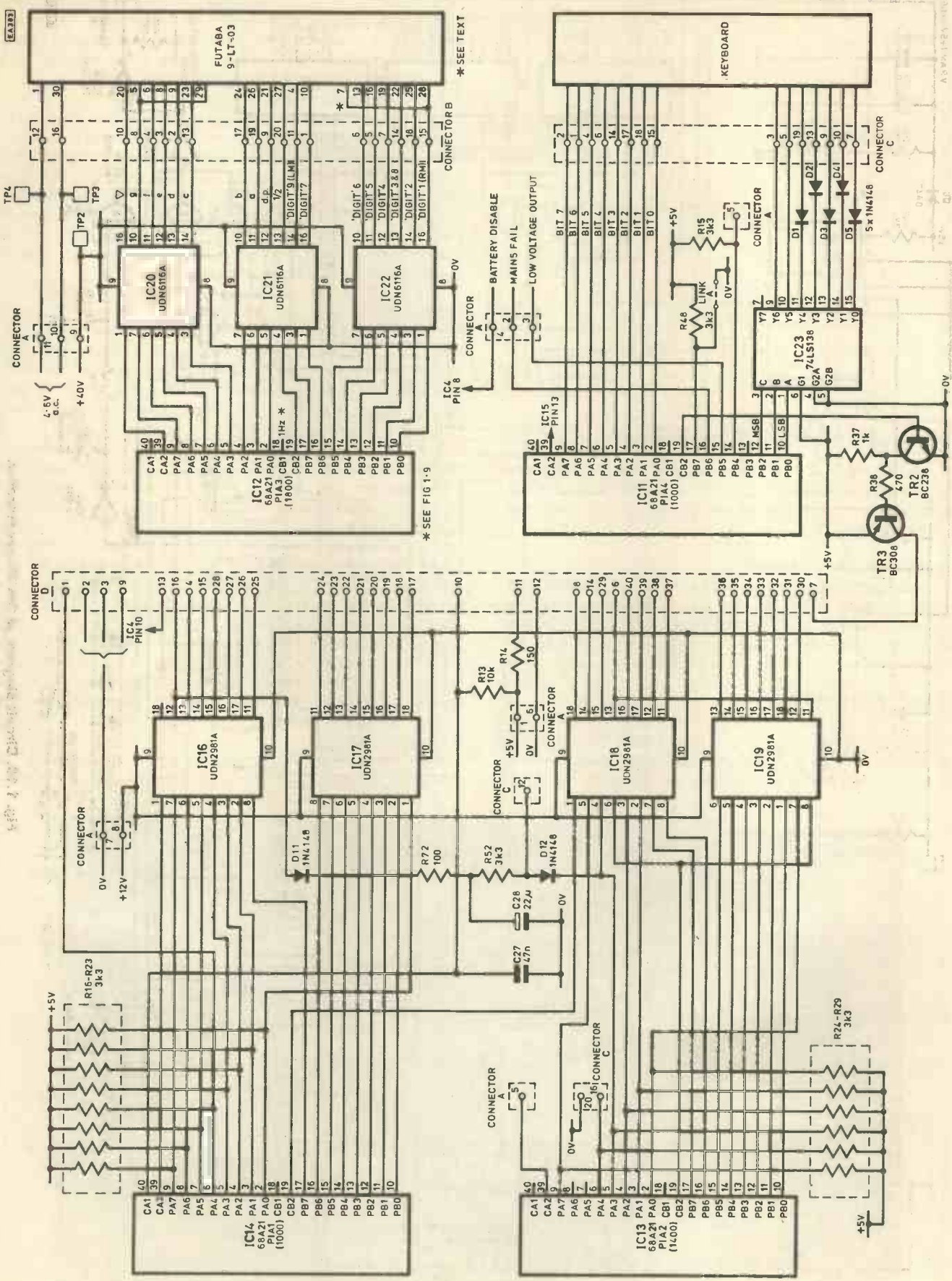


Fig. 1.9. Circuit diagram of the Microcontroller.





tional CMOS oscillator stage. A single inverting stage, biased into the linear region by R30, generates the fundamental clock at 4.194MHz. R32 reduces the crystal drive and improves the stability and accuracy of the oscillator. The oscillator output is set to standard logic levels by R33 and

A1 (RS0)	A0 (RS1)	PIA Register Selected
0	0	PIA output register A
0	1	PIA output register B
1	0	PIA control register A
1	1	PIA control register B

**TABLE 1** Correspondence between address lines and PIA registers selected.

R34. The 1Hz output is applied to the CB1 line on the display PIA, IC12.

The RAM storage in the Microcontroller is provided by two 1024x4-bit very low power memory devices, IC8 and IC9. These are arranged to provide 1024 bytes of storage. The two RAM devices are de-selected whenever the main +5V supply is absent, thus preventing inadvertent memory corruption. The memory contents are retained by the on-board Ni-Cad battery supply, B1. This battery has a capacity of 90mA/h, and during normal operation it is trickle charged at a nominal 4mA rate by means of R10. Control logic devices IC7 and IC15 are also supplied from B1 during power failure.

The gas discharge display is connected to the display PIA, IC12, via three high voltage drivers, IC20, IC21 and IC22. The display unit is multiplexed in the conventional manner under software control.

The keyboard is connected as a matrix between the A and B halves of the keyboard PIA, IC11. The three-to-eight line decoder IC23, simplifies the software scanning of the keyboard.

The user PIAs, IC12 and IC14, are available at connector "D" via four 12V high current drivers, IC16 to IC19. The function of these PIAs is, of course, user definable.

## INTERCONNECTIONS

1) Check that the thin blue and white wires on the mains transformer primary are connected together via an insulated connector block.

2) Remove the spade and tag connectors from the yellow, red, and green/yellow thin primary wires. N.B. do not remove the 4-way connector socket from the secondary wires.

3) Connect a good quality 3-core mains lead to the mains transformer, via a mains fuse (1 amp) and double pole on/off switch, as follows:

red = live  
yellow = neutral  
green/yellow = earth

The inclusion of a mains indicator neon, after the switch, is recommended.

4) Connect the mains transformer secondary lead to the power supply board by inserting the socket into the 4-pin connector labelled "C". Note that this connector will only mate correctly when properly inserted.

5) The power supply and Microcontroller boards should be linked together by mating the 11-way connectors marked "A" on the two boards.

6) Connect the 20-way ribbon cable from the display to plug "B" on the Microcontroller board, noting that the connectors are polarised.

7) Connect the 20-way ribbon cable from the keyboard to plug "C" on the Microcontroller board, again noting the polarisation of the connectors.

8) Connector "D" is utilised for interfacing the Microcontroller to the user's peripheral equipment.

## HARDWARE MODIFICATIONS

To set up the Microcontroller the following steps should be carried out.

1) Obtain a good quality 24-pin d.i.l. socket and bend pins 18 and 21 outwards at right angles. Remove any PROMs which may be supplied fitted in IC3 and, on some units only, in IC26 positions.

2) Insert the modified d.i.l. socket into the existing holder for IC3, taking care to observe correct orientation.

3) Using a short length of tinned copper wire, connect pin 18 of the new socket to the 0V rail; this is the wide p.c.b. track which runs on the top of the board between IC3 and IC5 (the 6800 CPU).

4) Using a 0.25W 1 kohm miniature carbon resistor, connect pin 21 of the new socket to the +5V rail; this is the medium width p.c.b. track which runs on the top of the board between pin 24 of IC3 and one end of C4.

5) Insert the DISBUG monitor EPROM into the new socket in the IC3 position, taking care to observe correct orientation.

6) Turn the display board over. The display unit has pins which are numbered from 1 to 30, with pin 14 missing. Pin 1 is identified on the p.c.b. Connect a short length of insulated connecting wire between pin 7 (previously unused) and pin 22.

7) Remove the key tops marked "-" and "1/2" and replace them in the positions shown in Fig. 1.8. The key top which they replace should be relocated to fill the two gaps. The keys should all be labelled as shown in the diagram.

## SWITCHING ON

1) Connect the mains supply, switch on and observe the DISBUG monitor "welcome" message on the display.

2) Should no display occur, check the voltages on connector "A" using a multimeter of 20 kohms/volt or better. Typical voltages expected are as follows:

A1	+5V	A5	+3.8V	A9	+42V
A2	+4.3V	A6	0V	A10	5V
A3	0V	A7	0V	A11	AC
A4	+4.2V	A8	+19V		

Any significant deviation from these values should be investigated. Also check that the DISBUG monitor EPROM has been correctly inserted, and that the voltage on pin 18 is 0V, and that the voltage on pin 21 is greater than +2V.

## COMPETITION

The Microcontroller competition is being run by Display Electronics to find the most practical application for the system.

The winning entry, which will be considered for publication in *PE*, will receive £300 in cash or goods from Display Electronics to the value of £400.

Full details of the competition together with an entry form and a copy of the rules are available from Display Electronics.

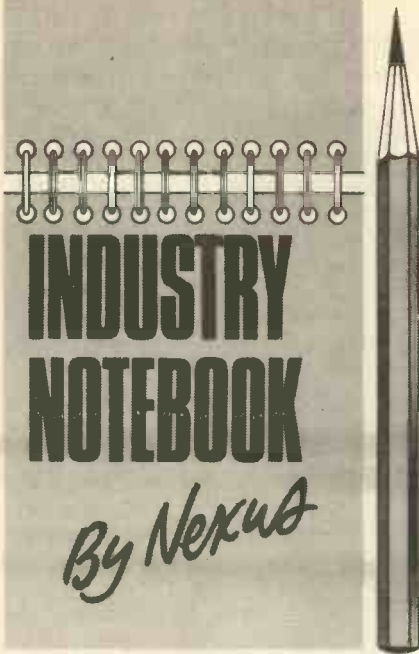
## PRICES

The complete Microcontroller system (excluding the case) is available for £32.95 plus VAT and p&p or separately at the following prices: main board £10.95, p.s.u. board £7.75, keyboard £5.50, display board £4.75, Disbug £5.25, 40 way I/O cable £1.45 and 20 way I/O cable £1.25. All prices exclude VAT and p&p.

Display Electronics, 64-66 Melfort Road, Thornton Heath, Surrey 01-689 7702. The case is available from West Hyde Developments, Unit 9, Park Street Industrial Estate, Aylesbury, Bucks.

**NEXT MONTH: P.S.U., DISBUG and 6800 programming.**





## A Year to Go

Nudges and winks of a general election within a year, perhaps sooner, added little to the theatre which passes nowadays for a political conference. The stars of their respective shows, Michael, Tony, Roy, Shirley, David, Maggie, Willie, loved, despised, hated according to party taste, all performed competently. But however clearly they argued their case it still needed a small army of media pundits to clarify and re-interpret every word. Discussion and comment seemed endless, the end result negligible.

The struggles between the parties were less interesting than the struggles within them, enlivened by new entrant, SDP, in an as yet still uneasy alliance with the Liberals. Internal squabbles can be papered over but not totally concealed. They are in every party but never more so than in Labour where all the conciliating skill of Michael Foot appears to be unavailing.

Looking back over several conference seasons and their subsequent influence on events, very few of the hopes expressed have been achieved, particularly in the economy because politicians, like the rest of us, willy-nilly are victims of fundamental shifts in other economies which, by nature of our world trade, necessarily interact with our own.

An often overlooked fact is that the supposed hard-line present government continues to pour billions of subsidy into coal, steel, shipbuilding, railways, airlines and motor manufacture in the best socialist tradition. The National Health Service cost £7.7 billion in 1978-79. Today the government is trying to contain costs within twice that figure. This is the measure of the problem that this government, or any other, has to face. Now in its fourth year it has gone some way to arrest the downhill slide, in a few areas to reverse it. Painfully slow progress but progress nevertheless with electronics shining, the rest of industry remaining dull.

## Spy Scare

The Japanese are nothing if not single-minded. For centuries theirs was an isolated nation, having no truck with foreigners. In this century they became dedicated to military conquest. Frustrated in this attempt they turned to industrial and trade war, so far with conspicuous success. No other nation has so mobilised itself to the single purpose of industrial supremacy on a world scale when military conquest has failed. The nearest parallel is equally defeated West Germany whose own 'economic miracle' is now faltering.

Every company likes to know what its competitors are doing and planning. But it still came as something of a shock that allegations are made that Hitachi and Mitsubishi have both been conspiring to obtain the trade secrets of IBM. Both companies have been indicted in US courts. Hitachi is reported to have admitted paying large sums (some £250,000) for information but denied knowing it had been stolen. Mitsubishi is reported to have denied unlawful conduct and will offer a vigorous defence against all charges.

Apparently the FBI set a trap by setting up a computer dealing company in Silicon Valley which looked genuine but was in fact bogus. Approaches were made to Japanese executives that confidential IBM documents could be provided—at a price. First contact, face-to-face, with an FBI undercover agent was, appropriately, in vice-city Las Vegas. The story, doubtless to be revealed more fully in court hearings, includes penetration of a building for photographic sessions and undercover payment in 100-dollar bills.

Whatever the outcome of these charges there is no question that they have opened another can of worms in the industry. For example it has re-opened the whole question of US technology leaking to other countries. One way of getting hold of a technology is by poaching engineering staff. A newly employed engineer should not, in theory, betray the secrets of his former employer, but even if he doesn't it is inevitable that ideas and techniques he has developed in his old job will be applied in his new employment. On a larger scale, another method is to buy a company outright or a big enough share to guarantee a place on the board. Examples are Philips buying Signetics and, more recently, Schlumberger's purchase of Fairchild. Then there are numerous cross-licensing deals which give a technology exchange between companies and also across national boundaries.

What worries the Americans is that US advanced technology can reach the Soviet Union through channels over which they have little or no control. If, say, a French company has acquired US know-how through acquisition of an American company, it can be regarded equally as French know-how and would need to be very sensitive (e.g. military security) not to be sold openly in the French manner, or indirectly through a third country acceptable to the West but having close links with the East.

So far, foreign ownership of electronics companies in the United States is mainly European and Japanese. But now, according to one report, the People's Republic of China has a half interest in a new semiconductor factory now building. It is hardly likely that the Soviet Union would be allowed equal access. But an awful thought remains. What if they have already done so through nominees? If the FBI can dupe the Japanese, why not the Soviets the USA?

## Fifth Generation

The immediate practical objective in the secrets probe at IBM was to come to the market with plug-for-plug compatible products to sell to IBM users. A longer term objective could well have been fifth generation computers which are planned to have a high order of artificial intelligence and in specialist applications are already being described as expert systems. They should be with us in the 1990s, if not earlier.

Such machines will need to be 'friendly' in the sense of being uncomplicated to use. Most of the hardware is available today but capable of further development. Voice entry, for example, rather than keyboard, and voice response with optional print-out. Assume a medical expert system. A GP may address it, describing a patient's symptoms, and get an instant diagnosis and suggested course of treatment as if the GP is in conversation with a top consultant. Which, indeed, he or she would be because massive storage would house the accumulated experience and judgement of the best medical experts. The secret, as usual, will be in very advanced programming.

The snag lies in validation of the knowledge stored. In the medical example a mistake in programming could cost lives. And, of course, 'experts' are often proved wrong. The computer, with its phenomenal calculating power, programmed with the best economic models, has hardly been a success in management of our own and other nations' economies.

Nonetheless, expert systems are on the way and the Japanese are investing a reported £200 million of government funds in a ten-year development programme plus possibly £500 million or more from Japanese industry. It all sounds very ambitious until we are reminded, as happened at a recent conference on the topic, that IBM spends as much in a year on R&D as the whole Japanese ten-year programme.

Anyway, it would be foolish to ignore progress and although it would be difficult to match the level of investment of the Japanese or the Americans, there is no doubt that British engineers and companies will be involved in expert systems. On the commercial front Racal have been first to announce an Expert Systems Division which will initially concentrate on oilfield exploration requirements and later expanded to such applications as medicine, finance, energy, industry and defence.

The new breed of super programmers generating artificial intelligence also have a new name to distinguish them from run-of-the-mill hacks. They are to be knowledge engineers.

# Ultimum Computer Interface *Part 1*

WATFORD ELECTRONICS

THE alarming rate at which personal computers have been introduced over the last couple of years *may* demonstrate a healthy growth market, but it doesn't help those who already took the plunge and are now left with a less capable machine. It matters little *when* you bought your computer, it is almost bound to be superceded by the next model in the range, and you are left with little or no support, and just like hi-fi five years ago, the only way out is to cut your losses and upgrade to one of the newer machines.

## THE ULTIMUM!

The ULTIMUM has been designed to allow *almost any* 8 bit computer to be expanded into a much more flexible system. It is modular, which makes custom systems possible, and it offers features which should whet the most megalomaniac appetite.

The ULTIMUM itself is a seven slot expansion board which connects to your computer via a 40 way ribbon cable. A purpose built case is available which will house a power supply, man enough to handle a fully expanded system.

Over the coming months, we shall be introducing several daughter cards. Below is a brief summary of the range:

- ★ A 16/64 KByte RAM card with paging.
- ★ A ROM/RAM/Battery back-up card allowing up to 20 Kbytes of RAM/ROM combinations.
- ★ A EPROM programmer with emulation facilities.
- ★ An *intelligent* floppy disk controller card, with its own processor allowing full control of disks from BASIC or M/C.
- ★ A port card with RS-232c, parallel and Centronics interfaces.
- ★ An analogue card with A>D and D>A capability.
- ★ A sound board providing up to nine voices, all independently programmable.
- ★ A speech card.
- ★ A terminal card which provides 80 column output and a keyboard interface.
- ★ A second processor card based on the 6809, for speed. This card can share the other cards on the ULTIMUM.
- ★ A prototype board, with pads and power tracks, for your own additions.

## THE MOTHERBOARD

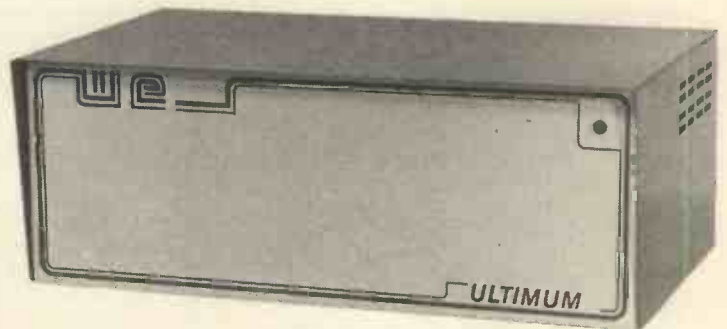
We begin with the motherboard. Fig. 1.1 gives the circuit diagram. IC1 to IC4 provide the full buffering of the data and address lines. Two basic bus standards are supported, the 65xx/68xx series and the Z80. These differ in their timing requirements and IC11 and IC12 (along with a few links) enable you to select either.

ICs 5,6,7,9 and 10 provide an on-board port, which makes paging and handshaking possible. This facility is not essential but makes the addition of large amounts of memory (256 Kbytes uses 4 slots) possible. The buffered signals are connected to each of the seven slots. IC8 is used to control the selection of the data buffer by collecting the select signals from the daughter cards. Cards can be moved around freely once set up, as all address decoding is done *off* the mother board.

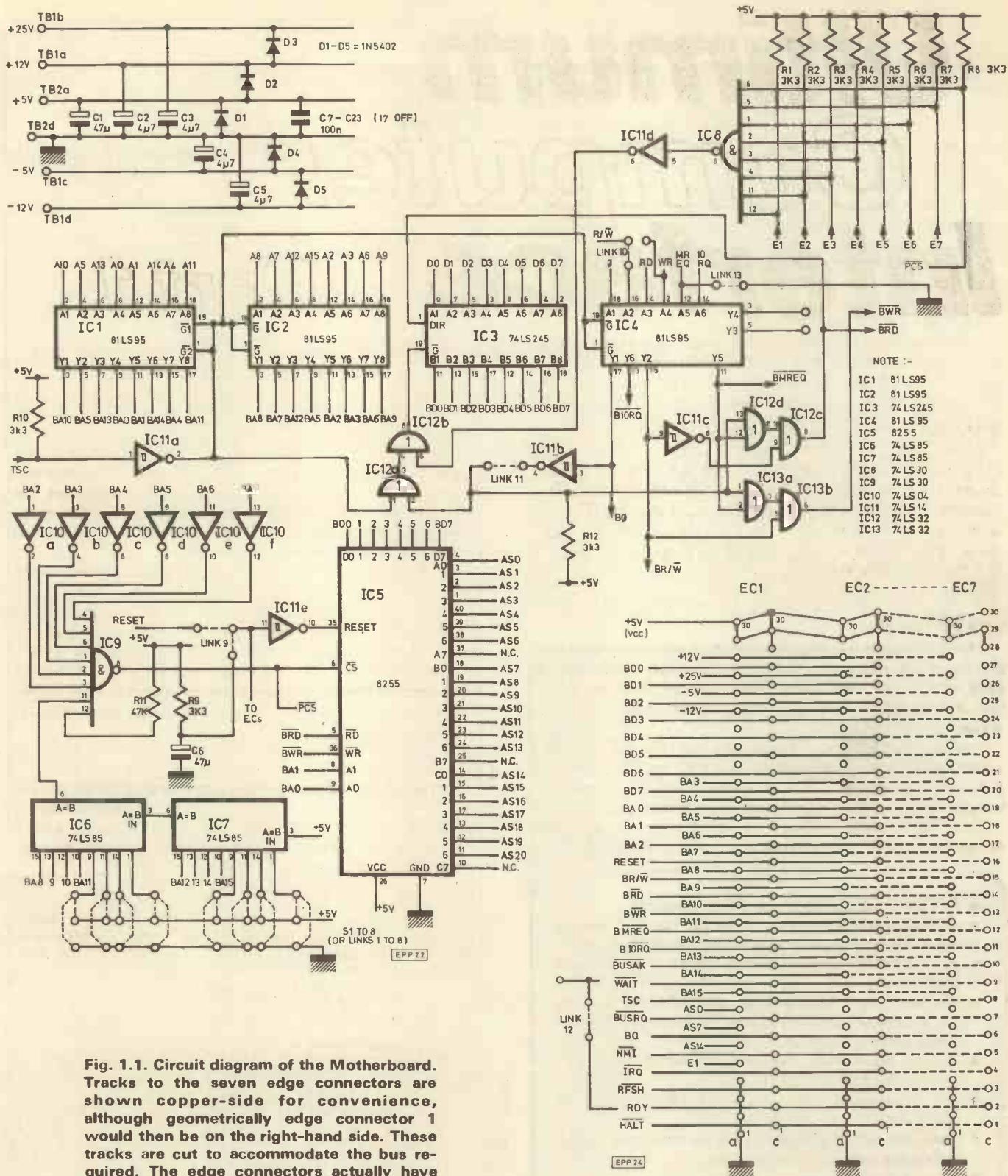
There are three 40 ways d.i.l. sockets which enable you to connect to your computer from the side or from the back.

The board is well decoupled, with diodes to prevent rails from crossing over on switch on/off. The slots themselves make use of two-part connectors, which although a little more expensive, do ensure reliable, knock resistant connection to the daughter cards.

Interfaces are in preparation for the following machines: Acorn Atom, Apple II, Atari, Commodore PET, Research Machines RML 380Z, Superboard, Spectrum, Superbrain, S100 Bus, UK101, Video Genie, ZX81.







**Fig. 1.1. Circuit diagram of the Motherboard.** Tracks to the seven edge connectors are shown copper-side for convenience, although geometrical edge connector 1 would then be on the right-hand side. These tracks are cut to accommodate the bus required. The edge connectors actually have 32 pins in each row, but the top-numbered ones are n.c. and therefore not shown

# THE UNIVERSAL INTERFACE

## ASSEMBLY

You will need a fine tipped soldering iron. Referring to the component layout of Fig. 1.3 install the i.c. sockets first, then the discrete components and finally the connectors. The backplane connections are close together and you must be careful to avoid shorting the tracks. Put the i.c.s in last, checking orientation carefully.

The connection to your computer will, of course, vary from model to model. A manual is provided with the kit of parts (see constructors' note) which tells you how to interface with most machines. As a general guide, Table 1.1. gives the standard connection to Z80 based systems and Table 1.2 is for the 6502/6800 microprocessor family. These tables also describe how to set up the various links for each type.

## TESTING THE 8255

The best way of testing that the board is wired correctly is to address the 8255 port i.c. The 8255 can be mapped to any 256 byte boundary by setting d.i.l. switches 1 to 8. Find an unused space and select it as shown in Table 1.3. The 8255 resets on power-on to its all input state. A set up routine (written in BASIC) is given in Table 1.4. which makes all the lines outputs, and then flips them from 1 to 0 approximately twice a second. You can observe this by looking on the port pins as laid out in Fig. 1.1. If nothing happens, check that you have set up the correct address and check your connections. If you use a multi-meter to check the outputs, make sure that it has an impedance of 5Kohms/volt or greater. Once the 8255 is working you can be fairly sure that any other faults are minor, and unlikely to damage the daughter cards.

## COMPONENTS . . .

### ULTIMUM MOTHERBOARD

#### Resistors

R1-R11	3k3 (11 off)
R11	47k

All resistors are  $\frac{1}{4}$ W 5%

#### Capacitors

C1, C6	47 $\mu$ /16V axial elect. (12 off)
C2-C5	4 $\mu$ 7/63V axial elect. (4 off)
C7-C24	100n disc ceramic (18 off)

#### Diodes

D1-D5	1N5402 (5 off)
-------	----------------

#### Integrated Circuits

IC1, IC2, IC4	81LS95 (3 off)
IC3	74LS245 (8T245)
IC5	8255
IC6, IC7	74LS85 (2 off)
IC8, IC9	74LS30 (2 off)
IC10	74LS04
IC11	74LS14
IC12, IC13	74LS32 (2 off)

#### Miscellaneous

14 pin d.i.l. sockets	(6 off)
16 " " "	(4 off)
20 " " "	(4 off)
40 " " "	(2 off)
S1-S4, S5-S8	4 way d.p.s.t. d.i.l. switch (2 off)
EC1, EC2	2 x 32 'A+C' DIN Euro Socket (straight pin) (2 off)
TB1, TB2	4 way p.c.b. terminal block (2 off)

#### Optional Extras

EC3-7	2 x 32 'A+C' DIN Euro Socket (straight pin) (5 off)
40 pin d.i.l. socket	(2 off)

TABLE 1.1. 40 WAY CONNECTIONS TO Z80 SYSTEMS

1 INT	40 MREQ
2 NMI	39 RESET
3 NC	38 HALT
4 D0	37 NC
5 D1	36 D4
6 D2	35 D5
7 D3	34 D6
8 IORQ	33 D7
9 GND	32 NC
10 NC	31 CLOCK
11 NC	30 RD
12 A2	29 WR
13 A1	28 RFSH
14 A0	27 A15
15 A3	26 A14
16 A4	25 A13
17 A5	24 A12
18 A6	23 A11
19 A7	22 A10
20 A8	21 A9

TABLE 1.2. 40 WAY CONNECTIONS TO 68/65xx SYSTEMS

1 IRQ	40 NC
2 NMI	39 RST
3 NC	38 NC
4 D0	37 RDY
5 D1	36 D4
6 D2	35 D5
7 D3	34 D6
8 NC	33 D7
9 GND	32 R/W
10 NC	31 Q2
11 NC	30 NC
12 A2	29 NC
13 A1	28 NC
14 A0	27 A15
15 A3	26 A14
16 A4	25 A13
17 A5	24 A12
18 A6	23 A11
19 A7	22 A10
20 A8	21 A9

NC Means No Connection  
Dn is Data bus  
An is Address bus



**TABLE 1.3.**  
**SETTING THE 8255 ADDRESS SPACE**

Link/switch	Mapped to . . . (hex)
87654321	
00000000	0000
00000001	0100
00000010	0200
00000011	0300
... in 100 hex increments	
00010000	1000
00010001	1100
00010010	1200
... in 100 hex increments	
00100000	2000
... etc.	
00110000	3000
... etc.	
11111111	FF00

Link	Switch
1 means link to Vcc	1 means ON
0 means link to GND	0 means OFF

**TABLE 1.4.**

10	P = (8255 Address in decimal)
20	POKE P + 3, 128 (Set all ports to output)
30	POKE P, 0
40	POKE P + 1, 0
50	POKE P + 2, 0
60	GOSUB 120
70	POKE P, 255
80	POKE P + 1, 255
90	POKE P + 2, 255
100	GOSUB 120
110	GOTO 30
120	FOR T = 1 TO 250 (Approx 1/2 s delay)
130	NEXT T
140	RETURN

**ULTIMUM**  
The ultimate motherboard?

Although the kit of parts will include d.i.l. switches for the setting up of address lines A8 to A15, we feel it is worthwhile pointing out the existence of an earlier option which the p.c.b. will accommodate. This is the use of prewired d.i.l. header plugs instead of switches, which can be changed quickly for different addressing. The tamper-proof nature of this option may be preferred.

The remaining links (refer to Fig. 1.3) should be wired as follows:

**LINK 9**

Link A-B for Z80 systems (allows reset from host computer)

Link B-C for 65/68 systems (gives on-board reset)

**LINK 10 (R/W, WR strapping link)**

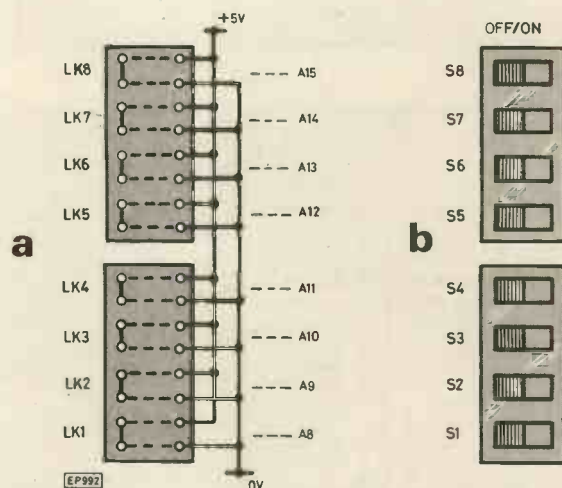
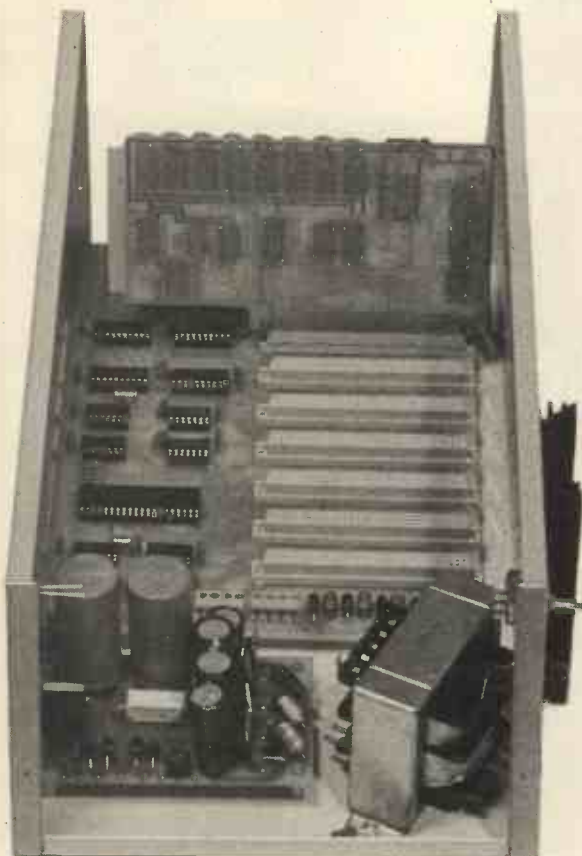
Link A-B for 65/68 systems (gives R/W to R/W)

Link A-C for Z80 systems (gives WR to R/W)

**LINK 11**

Link open for Z80 systems

Link closed for 65/68 systems



**Fig. 1.2. Ultimum links, and methods of linking. (a) Using linked header plugs which can be swapped. (b) Using d.i.l. switches**

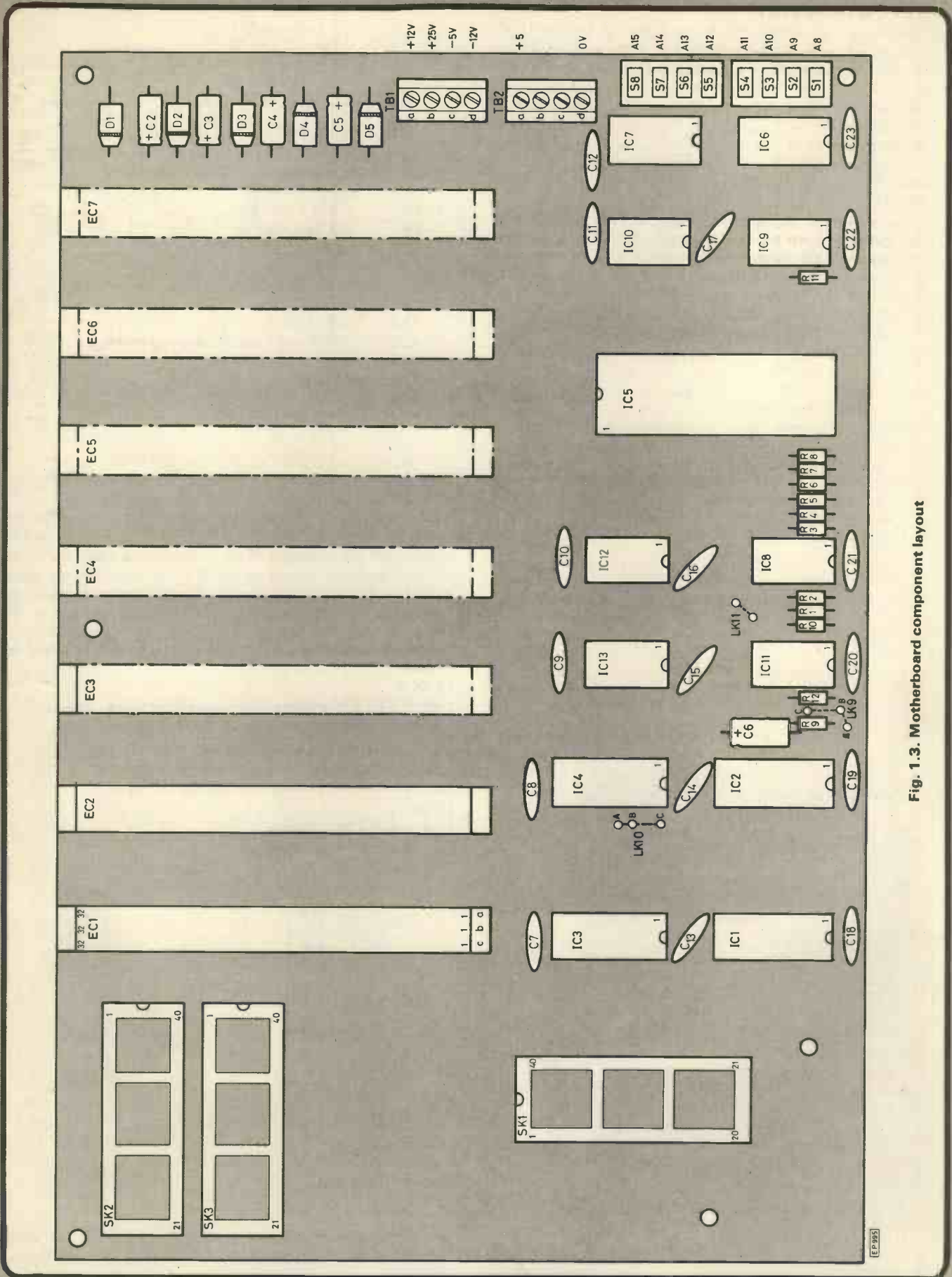


Fig. 1.3. Motherboard component layout



## THE POWER SUPPLY

A special power supply has been designed for the ULTIMUM, which provides power rails for additions such as the disk drive and the EPROM programmer. The power supply will fit inside the ULTIMUM case or may be mounted separately.

The design of the power supply is given in Fig. 1.4. This is a standard design using current limiting, thermally protected i.c. regulators. The component layout is given in Fig. 1.5. Please observe the usual precautions when wiring mains equipment. How to fit the assembled unit into its housing is covered in a comprehensive manual (see constructors' note), available with the kit of parts, but construction of the power supply p.c.b. assembly is very straightforward. Follow the overlay given (Fig. 1.5) and the instructions below, being careful to note the polarity of components where appropriate. The construction sequence is as follows:

- 1) Fit p.c.b. pins in points A-G, M, I, J, L, K, N, O, P.
- 2) Fit diodes D1-D4.
- 3) Fit REC1 and heatsink—bolt heatsink to bridge REC1 and then mount this assembly to p.c.b.
- 4) Fit bridge rectifier REC2.
- 5) Fit R1—leave 5mm clearance between resistor and p.c.b. to allow heat flow around resistor.
- 6) Fit smoothing capacitors C1 and C2. Note that the dummy tag is used only to provide greater stability.
- 7) Fit smoothing capacitors C14, C7, C11, C8.
- 8) Fit ceramic capacitors C15, C6, C13, C10.
- 9) Fit capacitors C5, C12, C3.
- 10) Fit zener diode D5.
- 11) Fit IC5, IC2, IC4, IC3—note that the metal tabs stand towards the ceramic capacitors.

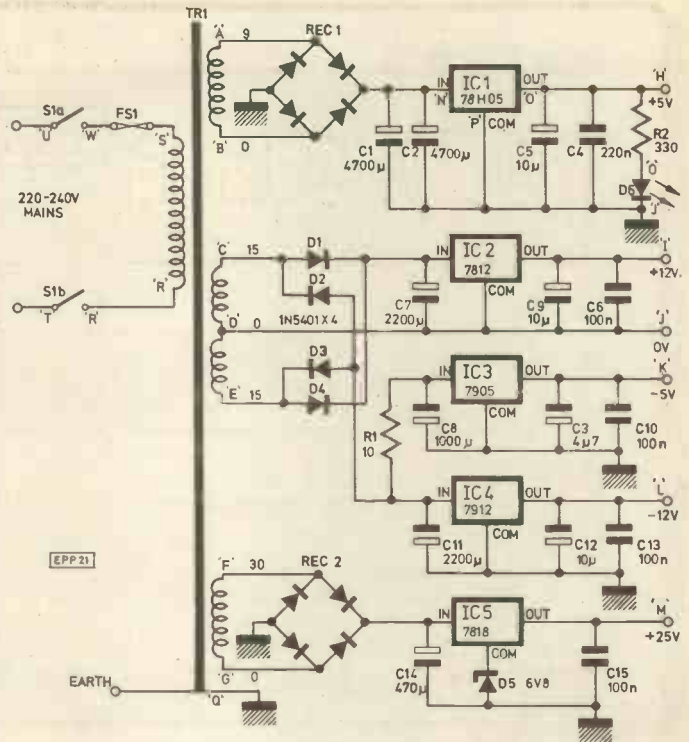
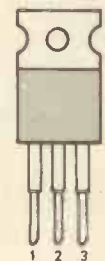
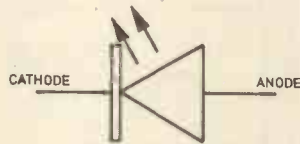
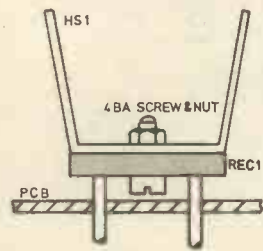
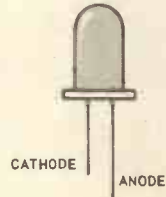
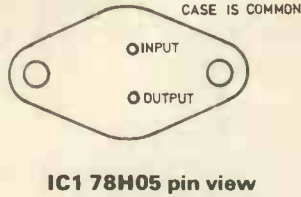
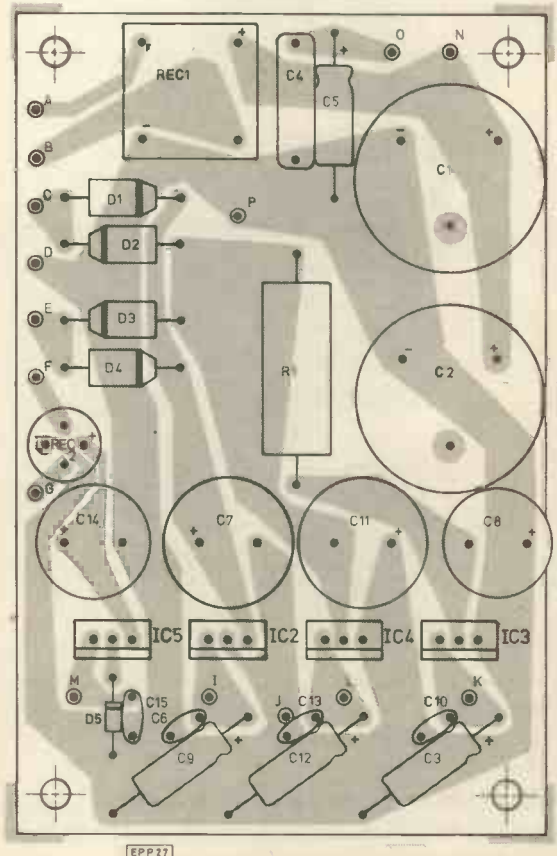


Fig. 1.4. PSU circuit diagram

Fig. 1.5. PSU component layout (copyright Watford Electronics)



IC2 7812  
IC3 7905  
IC4 7912  
IC5 7818

	1	2	3
IC2 7812	Input	Common	Output
IC3 7905	Common	Input	Output
IC4 7912	Common	Input	Output
IC5 7818	Input	Common	Output

Component pin-outs.

# COMPONENTS . . .

## MULTIRAIL POWER SUPPLY

### Resistors

R1	10 or 12Ω 5W
R2	330Ω ½W

### Capacitors

C1, C2	4700μ/25V tag elect. (2 off)
C3	4μ7/16V axial elect.
C4	220n polyester radial
C5, C9, C12	10μ/16V axial elect. (2 off)
C6, C10, C13, C15	100n disc ceramic (4 off)
C7, C11	2200μ/25V radial elect. (2 off)
C8	1000μ/16V radial elect.
C14	470μ/50V radial elect.

### Discrete Semiconductors

D1-D4	1N5401 (4 off)
D5	6V8 1W3 Zener
D6	0.2 in. l.e.d.
REC1	6A/100V bridge rect.
REC2	1A/100V bridge rect.

### Integrated Circuits

IC1	78H05 +5V/5A reg.
IC2	7812 +12V/1A reg.
IC3	7905 -5V/1A reg.
IC4	7912 -12V/1A reg.
IC5	7818 +18V/1A reg.

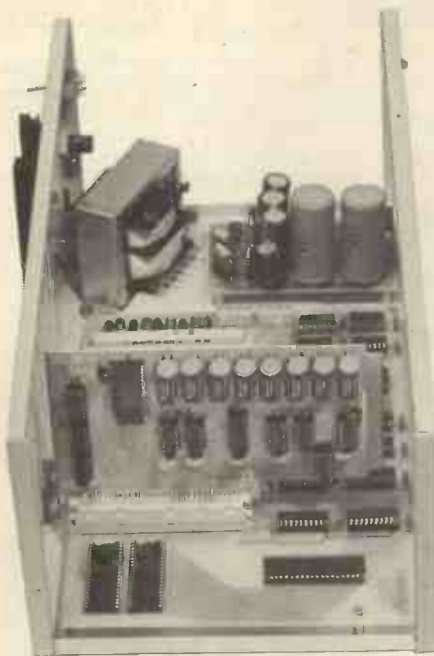
### Miscellaneous

T1	Multitap transformer (0-15, 0-15, 0-30, 0-30, 0-9, 0-9@5A)
S1	2 pole 2 way sub min. toggle (mains)
FS1	20mm 1A A/S fuse plus 20mm panel fuse holder
P.c.b.	Watford PSU board
6BA stand-offs, nuts & screws for mounting p.c.b. (4 off each)	
Heatsink	Type TV4
Insulating kit	TO3
5A 3-core mains cable	2 metres
Grommet for above	
4BA ½in. bolts, and nuts (5 off each)	
Solder tag (2 off)	

### CONSTRUCTORS' NOTE

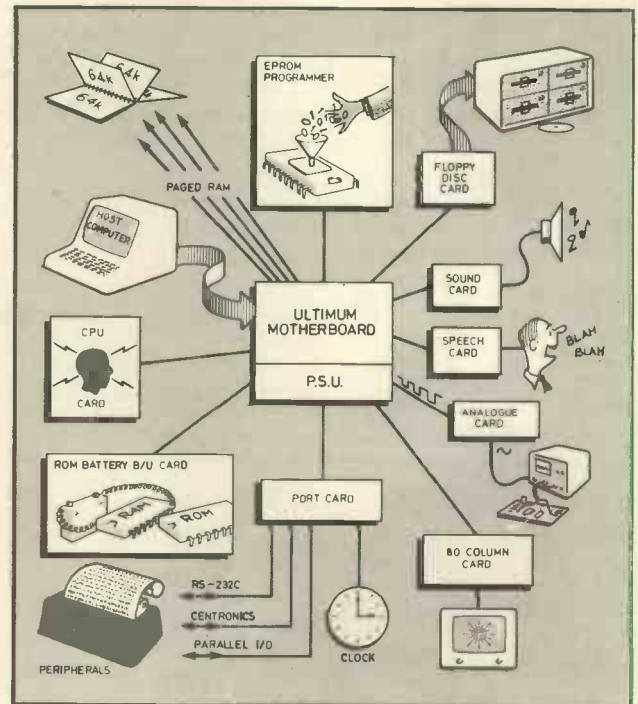
Kits for the ULTIMUM are available from Watford Electronics (see advertisers' index). A limited number of ready-built units will be available. Please send SAE for price list of boards now available.

*Because the system has so many applications, we feel sure, that people will want to exchange ideas. If this is the case, a users group will be formed to provide support for existing and future machines.*



This interface system is *totally* modular. It is therefore not only capable of rising to meet almost any specific requirement as it crops up, but may be expanded in stages as and when funds are available.

**Next Month:** Ultimium's potential will be expanded on. The 16/64K RAM board, EPROM programmer and Romulator, and ROM/RAM battery back-up.



**ULTIMUM combines economy and flexibility!**



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## MULTI ALARM WATCHES



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CA-95 (right) 2 melodies Calculator Resin £19.95

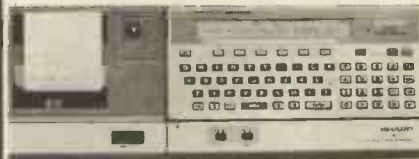
Both have 12 or 24 hour time and calendar display. Professional stopwatch; Hourly time signal; Daily alarm with pre-alarm; Daily alarm with post-alarm; Weekly alarm (or can be extra daily alarm). MM-400. In addition has monthly alarm (or extra daily alarm); Time is always on display; Dual time. CA-95 With calculator. C-951 metal version £29.95

## OTHER WATCHES

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GM-30 Battleships/submarines version £19.95  
GM-40 Pyramid building/invader version £19.95  
A656A Alarm; dual time; stopwatch. Chrome £9.95  
WS-70 S/S; W/R; C/D & alarm; D/T; S/W; slim £22.95  
SA-50 Non W/R chrome version £14.95. SA-50G £19.95

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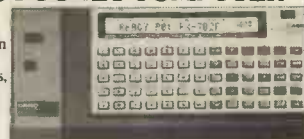


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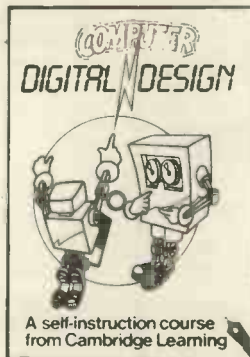
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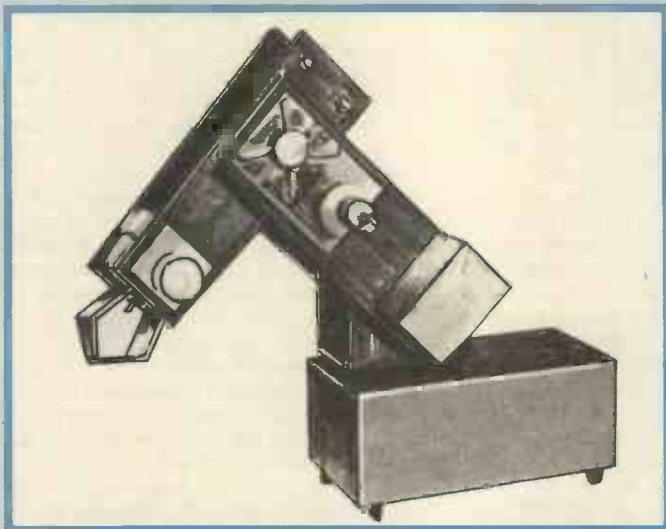
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## Space Watch...

### SALYUT 6 AND COSMOS 1,267

The Soviet Space control ended the 58 month mission of this composite unit on July the 29th, 1982. Cosmos 1,267 was docked automatically with Salyut 6 for a mission of scientific experiments and another of the Russian feasibility studies dealing with permanently manned units in orbit. Up till the time that the composite unit was commanded to destruct into the Pacific Ocean, it had logged some 676 days of manned operations. These were in short and long periods. The short duration involved 11 crews and the long durations 5 crews. The reason given for the termination of the missions was that the programme had been completed and the consumable items such as the fuel for the control systems was near the planned exhaustion level. The total number of launches of Soviet vehicles since Sputnik 1 on October the 4th, 1957, has now reached more than 1,500.

The American authorities seem to have been somewhat worried as to whether some of these manned missions were in fact concerned with anti-satellite homing vehicles as a defensive activity against American satellites. It seems out of keeping with the manner of space research that so much worthwhile work in the cause of science for the benefit of mankind should be marred by wrong attitudes and suspicious undercurrents. Nothing but benefit can come from co-operation, now especially as so many independent countries are active in space technology.

### LOOKING BELOW THE SURFACE OF THE LAND

The Shuttle imaging radar has shown that it is possible to provide adequate data of conditions and the character of sub-surface terrain. While it is, of course, possible for radar to 'see' below the surface, the imaging has always been regarded as useless. Now, after the data being analysed from the second Shuttle mission is considered, there are already plans for expeditions to the Sahara. Interest has extended to the re-examination of previous passes over arid areas. The JPL data is to be opened up for this purpose. Some of the Landsat data, like the multispectral scan over the Sahara, shows mostly sand but also a

hint of rough terrain below the sand. These, however, were over the 'hyperarid' areas where rainfall comes every 30-50 years. Here, the very fine sand allowed the radar to penetrate. Generally, however, there is no clear indication that there are reliable visual formations that could be reported. However, the radar pictures returned by the second shuttle flight provides ample evidence that very considerable detail can be seen. The varied techniques growing in experience and skill show remarkable conditions. As an example, some of the evidence points to formations which must be at least 35 million years old. Under the sand are to be seen large, wide and dry river valleys extending for hundreds of miles. Indeed, some of the valleys resemble very closely the present Nile valley. Other conclusions that have been drawn indicate that there are extensive fault lines and rugged terrain; also there can be seen alluvial valleys and terraces. The expeditions to make direct examination of these areas will be putting a new look on archaeological digs, for now they will be looking not at recent but at remote periods of time. It is not surprising that renewed interest in the planet Mars is taking place. The arid surface of Mars could yield a great deal of information if the new imaging techniques could be applied from an orbiter. It could be possible to examine the terrain of Mars beneath the polar caps. These new techniques are already regarded as a great scientific advance and new missions for the shuttle are already being planned. It should also be proper that the person who first suggested that this sub-surface imaging capability existed should be rewarded. The Geological Survey and the JPL view this a major discovery and award the credit to a guest investigator Carol S. Breed with the Astrogeologic Branch.

However, while past history is a clue to the future, there are intensive matters of interest for the present. The ebb and flow of terrestrial changes on the crust of the Earth indicates periods of wet conditions and savana growth and periods of arid conditions. Geological features now to be examined below the surface will enable assessments to be made as to the possibility of water and oil recovery. Knowledge of places where possible human habitation may have been in existence as long ago as 200,000 years, offers evidence of the conditions then. So the priorities are already being set for future shuttle missions. Two special radar missions for radar surveys will have the benefit of the new techniques from the Geological SIR-B.

SIR-B radar is an improved and upgraded version of the initial imaging system and will be flown on the shuttle in 1984. This mission will use the same aerial, that is the L-band, but with the capability of variable incidence angle ranging from 15 to 65 deg. This will facilitate the assessment of the effects on the imaging content. The shuttle 1987 to 1988 missions will use a radar system that will have the facility of variable incidence and also variable polarisation.

At the Jet Propulsion Laboratory a study is being made for a radar sounder mission to try to penetrate the polar icecaps. This will be possible because water ice is transparent to the radar energy. Studies of the surface effects

indicated that a great deal of surface information is to be obtained. Large wind patterns on the ocean surfaces were seen. In one section of the Aegean Sea it is thought that gravity waves have been detected, or at least the effect of such waves.

In enthusing about the imaging system it would be churlish not to deal with progress that is now being made with Landsat-D. The USA were intending to double the cost of the service of the distribution of data. These charges were \$5 to \$10 for a single coloured picture, and \$200 for a length of binary tape which the purchaser had to process. Some countries have set up their own land stations, paying the USA annual fees for the right to intercept the data. They were able to sell their own data as they wished. Now with the new techniques the scene becomes almost a rescue. Landsat-D, which was launched in last July, carries the new cameras with much improved data acquisition and an improvement of nearly five to one with the new Thematic mapping. This is a far more efficient system and takes pictures both in the visible spectrum and in the infra-red. Areas of 1,000 square metres can be analysed, which adds to the detail that can be 'seen'. There are particular advantages in this for small areas and plantation study. Two teams are co-operating with NASA in Britain. These are the National Environment Council in Swindon and at Reading University. They will be doing this before the Landsat-D comes into official service next year.

There is a second improvement also available for this vehicle. It will be the first to use a new communications satellite to be launched by NASA in January, 1983. It is called the Data Relay Satellite and will orbit 36,000 km above the Earth and will be in the Western Hemisphere. The signals will be received from the Landsat-D and bounced down to the Goddard Spaceflight Center. This means that it will not be necessary for them to operate a large number of base stations to receive data. This will reduce operation costs considerably.

### BRITAIN SHARES THE SPACE TELESCOPE WORK

British Aerospace will be delivering solar panels to NASA for the Space Telescope in September, 1983. The Bristol plant of British Aerospace are constructing what must be the largest solar panels so far destined for operation in space. The area of the panels are some 33 square metres. They are, in fact, so large that it is difficult to test the arrays in the Earth's gravity. Some 48,000 silicon cells will produce about 5.5 kilowatts of direct current.

The design of the panels is rather special. As the vehicle will have to be carried in the shuttle cargo bay, a compact package must be made. The solar panels will be wound around drums 20 centimetres in diameter. When the spacecraft is unloaded into orbit the two giant panels will unroll. The height at which the Telescope will orbit is comparatively low, only a few hundred kilometres.

These solar panels are likely to be the forerunners of still larger arrays. This will be necessary because power of 100kW will be required by the 1990's, and by the end of the century of the order of megawatts. The value of the contract to British Aerospace is worth some 11 million pounds.



# PE micro~file

## R.W. COLES INTRODUCTION

**WE** HAVE all been touched by the far reaching effects of the microprocessor revolution in our day to day lives, and there will soon be few households which do not have a microprocessor tucked away somewhere, in a TV game, a home computer, a washing machine or even a door bell!

Of course, as electronics enthusiasts, we have a special interest in the potential of the microprocessor, but although most of us are itching for a "piece of the action" it has *not* been easy to decide quite what we are supposed to do with this marvellous innovation. At the moment, even for electronic hobbyists, the main way "in" is to buy a basic home computer such as the Sinclair ZX81. But I suspect that for some this has been a frustrating experience. The problem is that using a home computer and programming it in BASIC is not necessarily a suitable replacement for the smell of solder flux and the burned fingers which we all enjoyed so much! Almost ten years since the first microprocessor appeared, it now seems that microprocessors are for *software* hobbyists and are much too complicated for us to use in the replacement of the transistors, gates, and pink wire with which we have been traditionally associated.

This situation cannot be allowed to continue. Microprocessors are crying out for the attentions of our soldering irons, and it is our contention that the use of these useful devices is not as difficult as it may appear at first sight. The problem we face is in the nature of an information explosion. We are surrounded by a bewildering array of microprocessor chips, support chips, memory chips and software, all apparently *very* complicated. If we want to build a simple system such as a music generator or a central heating controller, which chip do we choose? Is it powerful enough? Has it got the right features? Can we program it? Will it be obsolete next month? All questions not easy to answer, and enough to put us off the idea and return to building "traditional" projects or even turn our hand to writing a program to find all the prime numbers between 1 and 1000.

But all is not lost! The editorial team of *Practical Electronics* is determined that the electronic aspects of using microprocessors should not be delegated for ever to the professionals, and we are therefore launching the MICRO-FILE series to help reduce the confusion surrounding these powerful components. The series is an attempt to lay bare the essential characteristics of the most popular processors so that the interested may keep up to date, and the dedicated project designers can choose the correct processor for their needs. Those who already have microprocessors in personal computers or other units will also find the series useful if they wish to delve into the innards of their machine to interface with it, repair it, or even just understand it.

# the micro scene...

There are currently about 40 different available microprocessor designs, although obviously not all of these can claim to be "winners". Even this daunting figure does not tell the whole story by any means. Many of the 40 basic chip designs come in several different versions which bumps the total up considerably, and nearly all the "popular" devices are produced by several manufacturers either by second sourcing under licence, or as functional copies which may not operate like the original in all respects. Add to this the fact that most micro based systems require additional family support chips to facilitate interfacing and the seeds of confusion have sprouted to form a forest!

Because of the kaleidoscopic nature of applications for the versatile microprocessor, it is not easy to create pigeon holes into which the various chips and their uses can be slotted, but some attempt has to be made to simplify things. Perhaps the best way to start is to split the spectrum of micro applications in two, with "data processors" on the one hand and "controllers" on the other. Data processors generally operate "off-line" under human supervision and require large programs usually written in a high level language such as BASIC. These systems require large arrays of read write memory and generally have at least one operator console. Personal computers are one example of a data processor application, word processors are another.

Controllers usually operate alone to control or monitor some process automatically and generally use smaller ROM based fixed programs which are usually written in assembly language machine code. For controller applications speed is often important, and transducers are required to sense the state of the process and to generate appropriate outputs. Burglar alarms, TV games and central heating systems are examples of applications where microprocessors are used as controllers.

## CHOOSING A CHIP

Many microprocessor chips have special advantages which suit them either to data processor or to controller applications, but it is also true that many others are general purpose in nature.

Those best suited to data processing will have a word length of at least 8 bits and will have an address bus wide

enough to access at least 64K words of memory. Their instruction sets should offer a rich variety of addressing modes and a family of interface devices should also be available. There is a very definite trend towards 16 bit processors with address ranges of 1 megabyte or more for most data processing tasks. These devices are at least as powerful as the minicomputers which they will soon replace, but the design of a hardware and software system to take advantage of their power is, unfortunately, a daunting prospect for the non-professional.

Microprocessors optimised for controller applications may have any word length from 4 bits upwards and should ideally be as self-contained as possible, even to the extent of being true "single chip" devices which pack RAM ROM and interface lines into a single package. Controller instruction sets should be compact and offer fast access to I/O and timing functions. Simple, on chip interrupt prioritisation is also an advantage, as is the availability of a multifunction peripheral chip family. Generally speaking, microprocessors which are optimised for control applications are simpler to design with in both hardware and software terms.

The author's view is that if your main interest lies in the data processing or personal computer field, then it is difficult to compete with the many ready-made offerings from Sinclair, Acorn, Commodore, Tandy, Apple, and a host of other suppliers. The main problem here is that the microprocessor is really only the tip of the iceberg in D.P. applications with software being the most important factor. It has been said, for example, that to make proper use of the new data processing orientated iAPX 432 microprocessor from Intel, the typical user will need to invest as much as ten *man-years* in software creation, even using a high level language!

If you wish to use a microprocessor to *control* things however, then hardware ingenuity is still very important and the required software can usually be created in weeks even when using machine code and without the benefit of expensive development systems. The message is clear. If your ambitions lie in designing a 16 bit personal computer with twin floppies, a megabyte of RAM and a Pascal compiler, then a stony road lies ahead! If, however, you wish to control your central heating or build a fuel consumption computer for your car, then pick a suitably simple control processor and have a go; you could have a lot of fun!



## THE OBSOLESCENCE PROBLEM

One thorny problem for any budding designer is the very rapid progress in microprocessor technology which produces better, faster, and above all *cheaper* devices at a breakneck pace. There is therefore the ever present spectre of starting a project and then finding that before it is finished a new device has emerged which would do the job better and at a lower cost. This is especially true in the data processing field where development periods tend to be longer.

To avoid the worst of this problem, it is obviously necessary to choose a device which is not about to be superseded. Beware the bargain offer of a wheelbarrow full of National SC/MPs or Intel 8008s for a "Tenner!" At the same time it is necessary to choose a device which has been in play for a sufficiently long period to establish its popularity and which can therefore be expected to have good support and a long life. You can expect the manufacturers to develop their success with popular chips by bringing out improved versions, and this can be an advantage because your "learning" investment can be put to good use on future projects using the enhanced devices when they are available. It is also necessary to remember that, say, a central heating controller may be required to operate for 20 years or more while the lifetime of the majority of microprocessors can be expected to be less than ten years—so remember to buy a spare!

## SUPPORT DEVICES

If there *were* any such thing as a typical microprocessor

system then in addition to the processor device itself we could expect to find RAM and ROM memory, a parallel I/O port, a serial I/O port, and at least one "special" device such as a disc controller, a maths chip, or an analogue to digital converter. Support devices are available to fill all these requirements and many more besides, and these have to be given serious consideration since they contribute almost as much as the processor itself to the success of any project.

Support devices can be part of a particular microprocessor "family" and these often have special features to simplify their use with that family. Also available are many general purpose devices which can be interfaced to most processors with the addition of a small amount of external logic. All have their part to play. The trend in support devices is towards complex and powerful chips which give a considerable boost to the basic performance of any processor by unloading from it a lot of the system "chores" which it would otherwise have to perform for itself. Prime examples here are the maths processor chips which give systems easy access to floating point arithmetic and high level math functions such as square roots and sines which would normally have to be provided by software routines. Many support devices rival the microprocessors which they serve in chip complexity, and so it is important not to underestimate the task of learning how to initialise and program these devices to perform the required function. Some support chips even have user manuals as thick as those of their attendant microprocessor!

## MICRO-FILE FORMAT

Having set the scene, and perhaps frightened, but hopefully inspired many readers, we can now return to how the MICRO-FILE series has been designed to help!

To make any kind of objective assessment of a number of microprocessor devices it is normally necessary to purchase the relevant manuals, and these are not cheap. Having purchased the manuals, a period of intensive study is required to sort out the important characteristics and to come to any conclusion. Remember too, that the manuals are written by the manufacturer and are therefore unlikely to point out any shortcomings!

MICRO-FILE builds up month by month to provide a complete quick reference guide to the more popular microprocessors. Each MICRO-FILE entry consists of a quick reference fact sheet, designed for easy filing, and explanatory text which provides further information and application data. The sheets can be removed from the magazine and placed in a binder for filing.

This introductory article can form the binding "covers". At present there are plans to include about twelve of the most popular processors, but this may be extended later if necessary. So if you collect the whole series it will form a 48 page (or more) reference book on microprocessors plus this "cover" section.

The first FILESHEET considers the Intel 8080A and its successor the 8085A, two of the most popular processors so far, with the 8080A often considered to be the processor which really started the microprocessor revolution.

The reference fact sheet is intended to provide all the essential information about a processor or a processor family, including general background details, register arrangement, instruction set and software, system schematics, performance data, pin connections and basic support chip information. Using these sheets it will be possible to compare processors and to choose the best one for a particular application. Readers not interested in go-it-alone projects can use the sheets to assess the potential power of readily built systems using a particular processor, to help with system trouble shooting and interfacing, or simply to improve their knowledge of the subject.

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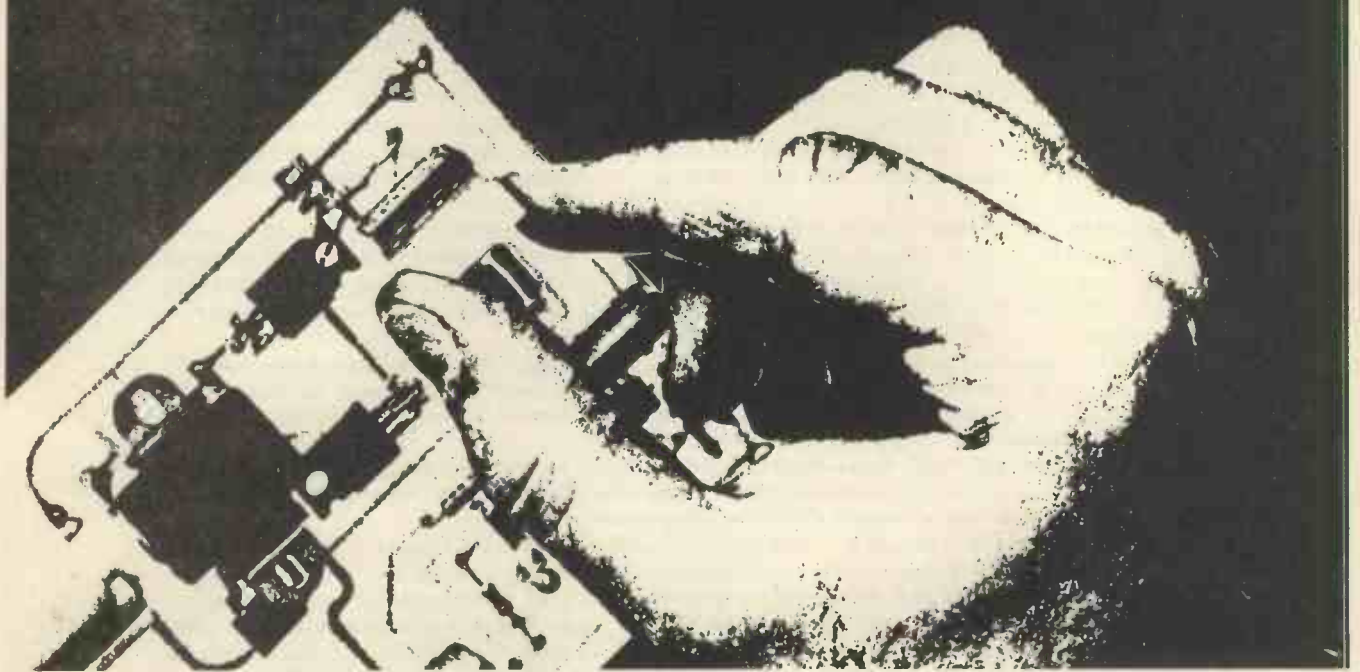
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# PE micro~file

R.W.Coles

## FILESHEET 1 8080A • 8085A

THE Intel 8080 8 bit NMOS microprocessor first appeared in 1973 as a successor to the more limited 8008 PMOS device. The 8080A was the first microprocessor to capture the imagination of designers and was a fundamental cog in the microprocessor revolution generating annual sales of over 2 million devices per year in its heyday. The success of this chip resulted in the spawning of two, more powerful successors, the Z80 from Zilog which had an enhanced instruction set but basically the same bus configuration, and the 8085A from Intel which had basically the same instruction set but a new multiplexed bus structure. Both of the newcomers appeared in 1977 and have now replaced the 8080A for all new applications with the Z80 being most popular for data processing and the 8085 being more successful as a controller.

In order to squeeze the maximum performance from the NMOS technology available in the early 1970s the 8080A was designed to use three supply rails of +5, -5 and +12 volts and had to have two additional support chips to provide clock generation and bus interface. The main competition to the 8080A in the early days was the Motorola 6800 which despite using only two chips and a single supply voltage was never as popular due to its lower overall performance.

The 8080A has a common instruction and data memory space of 64 kilobytes and a separate I/O space of 256 ports which, together with a good general purpose instruction set, made it useful for a wide range of applications in control and data processing.

The 8085 was an attempt by Intel to maintain the sales momentum created by the 8080A, although it could be argued that the competing Z80 from Zilog did a better job. The 8085 needs no support chips except for memory and I/O, and will run faster than the 8080A from a single 5V supply. To free extra interface pins the 8085A has a multiplexed data and address bus with the new connections being used for extra interrupts and serial I/O in addition to the necessary control and clock lines. Introduced at the same time as the 8085A were two special peripheral devices also in 40 pin packages. The 8155 provides 256 bytes of RAM, 22 parallel I/O lines and a 14 bit timer while the 8355 provides 2K bytes of ROM and 16 parallel I/O lines. Using the 8085A with these two peripherals it is possible to build a powerful processor system with RAM, ROM and comprehensive I/O using just three chips.

### REGISTERS

The 8080A and the 8085A have an identical data register arrangement although the 8085A does have an additional register which is used in the control of its extra serial I/O and Interrupt lines. Both devices have eight addressable 8 bit registers which can be used as four 16 bit register pairs for many operations. Perhaps most important of these is the 8 bit Accumulator register which is the implied focus of many instructions including the memory reference, arithmetic, and I/O groups. For some operations this register is paired with the flag register which itself provides single bit status information about data in the accumulator after arithmetic and logical operations. Flag bits are provided to report on five possible status conditions as shown on the file sheet, with the remaining 3 bits being unused. The BC, DE and HL registers are essentially general purpose in nature and can be used as temporary storage for 8 and 16 bit data values, as 8 and 16 bit counters, or as 16 bit memory address pointers. The HL register is particularly important as a memory pointer since it is used by a number of memory reference instructions. It is also used as an "accumulator" for 16 bit arithmetic. A smaller number of instructions use the BC and DE pairs as pointers, and either of these register pairs can be added to the HL pair to give a limited 16 bit arithmetic capability.

In addition to the four register pairs already discussed there are two other 16 bit registers which have dedicated functions. The Program Counter register always points to the next instruction to be executed and therefore contains a 16 bit address. The Stack Pointer always points to the top of the last-in-first-out stack area maintained in read/write memory for the storage of subroutine return addresses and register values saved during interrupts or for other purposes. The Stack Pointer is decremented each time data is "pushed" on to the stack and is incremented each time data is "popped" off the stack.

The generous register set of the 8080 was one of the reasons for its success over the Motorola 6800, but the specialised uses of the BC, DE and HL pairs also had the effect of producing a less regular and "messy" instruction set making it necessary for the programmer to remember just what particular pairs can and cannot be used for. The more modern 16 bit processors overcome this problem by making their registers completely general purpose and non-specialised wherever possible. Lacking in the 8080/8085 is the useful feature of an index register such as that provided by the 6800, although this job can be performed by the register pairs at the cost of using extra instructions.

### INSTRUCTION SET

As mentioned above, the 8080/8085 instruction set is rather "messy" due to the somewhat specialised nature of the large register array, but this does make these devices very powerful considering their small chip areas. The 78 basic instructions of the 8080 are used to move data between registers, between a register and memory, between a register and an I/O port, and to carry out arithmetic and logical operations. Instructions are also included to perform conditional and unconditional jumps and to control processor operation. Two additional 8085A instructions, RIM and SIM, are ingeniously used to provide access to, and control over, the extra serial I/O and interrupt features not present on the 8080.

A comprehensive array of arithmetic and logical operations are provided including 8 and 16 bit binary addition, 8 bit binary subtraction, binary coded decimal (BCD) arithmetic on packed BCD values, logical operations such as AND, OR, XOR and Compare, and a range of accumulator shifts and carry flag modifiers. One item missing from this group is the ability to set, test, and reset, individual accumulator bits which is a very useful feature for control applications. These operations can be performed by shifting the relevant bit into the carry flip-flop or by using logic instructions, however.

Four addressing modes are used as follows:—Direct, in which a memory address is specified as part of the instruction; Register, in which a register or register pair is specified; Register Indirect, in which the instruction specifies a register pair which itself contains a memory address; and Immediate, in which the instruction contains not a reference to a data area but the actual data itself. One particularly useful feature of the instruction set is the provision of a group of eight Restart instructions which cause an immediate jump to fixed vectors in low memory. These instructions use only a single byte and are used for hardware interrupt service or as software interrupts. Access to the separate I/O address space of 256 input and 256 output ports is provided by means of the instructions IN and OUT which are fast because they are only 2 bytes long. The separate I/O address space is useful because it does not encroach on main memory, but it is still possible to use memory mapping for I/O ports if required for a simple system not needing the full 64K memory address range.

# 8080A/8085A REFERENCE FILE SHEET

## GENERAL

The 8080A was the first of the mid-range NMOS 8 bit processors and is certainly the most widely used. It has a good general purpose architecture and is very well supported with both hardware and software. The 8085A has essentially the same instruction set as the 8080A but needs only a 5V supply and has many additional features such as on-chip clock, serial I/O and four new interrupt lines. Extra pins for these functions have been made available by multiplexing the low order address bits with the data bus. A complete 8085A system with 2K bytes of ROM, 256 bytes of RAM, a timer and 38 I/O lines can be built with just three 40 pin chips by utilizing the 8355 (ROM I/O) and the 8155 (RAM I/O TIMER) combination devices.

**REGISTERS:** The 8080/8085 has seven 8 bit general purpose registers. Six of these can be addressed as the three 16 bit pairs BC, DE, HL.

### Notes

- 1) PSW = Processor Status Word
- 2) HL is used as memory pointer for register indirect addressing.

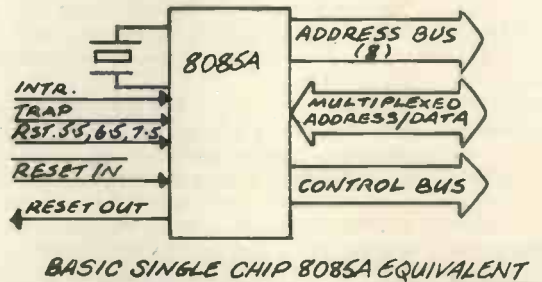
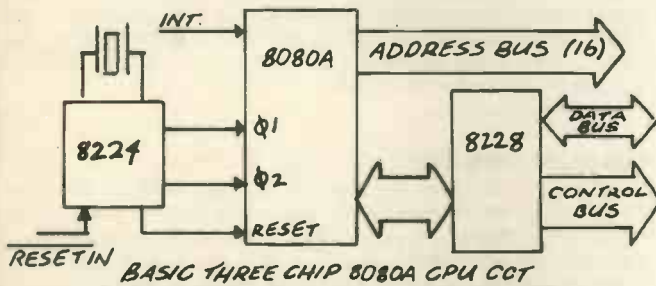
REGISTER	SIZE	REGISTER	SIZE
ACCUM	8	FLAGS	8
B	8	C	8
D	8	E	8
H	8	L	8
STACK POINTER		16	
PROGRAM COUNTER		16	

### FLAGS:

DF	D6	D5	D4	D3	D2	D1	D0
SIGN	ZERO		AUX. CARRY		PARITY		CARRY

## INSTRUCTION SET AND SOFTWARE

The 8080 has 78 basic instructions and the 8085 has two more, RIM and SIM which support the additional interrupts and serial I/O. One, two and three byte instructions are used and Direct, Register, Register Indirect and Immediate addressing modes are available. Full binary and BCD arithmetic is possible on 8 bit bytes, and some 16 bit arithmetic is possible using the HL pair as an accumulator. A separate address space is available for I/O using the IN and OUT instructions. Very well supported with software including Tiny Basics and the CPM operating system.



## PERFORMANCE DATA

	8080A	8085A
MEMORY ADDRESS RANGE:	64K	64K
I/O ADDRESS RANGE:	256	256
CLOCK FREQUENCY:*	2MHz	3-12.5
POWER SUPPLIES:	+5, -5, +12V	+5V
INTERRUPTS:	INT.	INTR. TRAP RST 5.5 RST 6.5 RST 7.5

\* NOTE: HIGH SPEED VERSIONS OF 8080A (3MHz) AND 8085A (5MHz) ALSO AVAILABLE

## BENCHMARKS

	8080A	8085A
ADD REGISTER TO ACCUM:	2µS	1.28µS
OUTPUT ACCUMULATOR TO PORT:	5µS	3.2µS
MOVE FROM MEMORY TO MEMORY:	8µS	5.12µS

A10	40	A11	X1	1	40	VCC
GND	2	39	A14	X2	2	39
D4	3	38	A13	RESET OUT	3	38
D5	4	37	A12	SOD	4	37
D6	5	36	A15	S10	5	36
D7	6	35	A9	TRAP	6	35
D3	7	34	A8	RST 7.5	7	34
D2	8	33	A7	RST 6.5	8	33
D1	9	32	A6	RST 5.5	9	32
D0	10	8080A 31	A5	INTR.	10	8085A 31
-5V	11	30	A4	INTA	11	30
RESET	12	29	A3	AD0	12	29
HOLD	13	28	+12V	AD1	13	28
INT	14	27	A2	AD2	14	27
Q2	15	26	A1	AD3	15	26
INTE	16	25	A0	AD4	16	25
DBIN	17	24	WAIT	AD5	17	24
WR	18	23	READY	AD6	18	23
SYNC	19	22	Q1	AD7	19	22
+5V	20	21	HLDA	VSS	20	21

## PIN DIAGRAMS

## MANUFACTURERS

ORIGINATOR — INTEL  
 2nd Sources } SIEMENS, AMD, NEC.  
 8080A } NATIONAL, SIENETICS, HITACHI  
 2nd Sources } AMD, SIEMENS, NEC  
 8085A

## SUPPORT CHIPS

8080A Needs 8224 and 8228 and has a large family of support devices including: 8251 (USART), 8255 (Parallel I/O), 8253 (Timer), 8259 (Interrupt Control), 8257 (DMA).  
 8085A has two special combination I/O memory chips 8355 and 8155 in addition to above devices.



TABLE 8. INSTRUCTION SET SUMMARY

Mnemonic	Description	Instruction Code[1]							Clock[2] Cycles	Mnemonic	Description	Instruction Code[1]							Clock[2] Cycles		
		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>				D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>		D <sub>1</sub>	D <sub>0</sub>
<b>MOVE, LOAD, AND STORE</b>																					
MOV r1 r2	Move register to register	0	1	D	D	S	S	S	4	CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18	
MOV M r	Move register to memory	0	1	1	1	0	S	S	S	7	CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
MOV r M	Move memory to register	0	1	D	D	D	1	1	0	7	<b>RETURN</b>										
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7	RET	Return	1	1	0	0	1	0	0	1	10
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10	RC	Return on carry	1	1	0	1	1	0	0	0	6/12
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10	RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10	RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10	RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10	RP	Return on positive	1	1	1	0	0	0	0	0	6/12
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7	RM	Return on minus	1	1	1	1	0	0	0	0	6/12
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7	RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7	RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7	<b>RESTART</b>										
STA	Store A direct	0	0	1	1	0	0	1	0	13	RST	Restart	1	1	A	A	A	1	1	1	12
LDA	Load A direct	0	0	1	1	1	0	1	0	13	<b>INPUT/OUTPUT</b>										
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16	IN	Input	1	1	0	1	1	0	1	1	10
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16	OUT	Output	1	1	0	1	0	0	1	1	10
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4	<b>INCREMENT AND DECREMENT</b>										
<b>STACK OPS</b>																					
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12	INR r	Increment register	0	0	D	D	0	1	0	0	4
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12	DCR r	Decrement register	0	0	D	D	0	1	0	1	4
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12	INR M	Increment memory	0	0	1	1	0	1	0	0	10
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12	DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10	INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10	INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10	INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10	INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	16	DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6	DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
<b>JUMP</b>																					
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10	DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10	DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10	<b>ADD</b>										
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10	ADD r	Add register to A	1	0	0	0	0	S	S	S	4
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10	ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10	ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10	ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10	ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10	ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6	DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
<b>CALL</b>																					
CALL	Call unconditional	1	1	0	0	1	1	0	1	18	DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
CC	Call on carry	1	1	0	1	1	1	0	0	9/18	DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18	DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18	<b>SUBTRACT</b>										
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18	SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
CP	Call on positive	1	1	1	1	0	1	0	0	9/18	SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
CM	Call on minus	1	1	1	1	1	1	0	0	9/18	SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
<b>SBB M</b>																					
Subtract memory from A with borrow																					
SUI																					
Subtract immediate from A																					
SBI																					
Subtract immediate from A with borrow																					

TABLE 8. INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Description	Instruction Code[1]						Clock[2] Cycles	Mnemonic	Description	Instruction Code[1]						Clock[2] Cycles				
		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>				D <sub>1</sub>	D <sub>0</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>		D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
<b>LOGICAL</b>																					
ANA r	And register with A	1	0	1	0	0	S	S	S	4	RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4	RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4	<b>SPECIALS</b>										
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4	CMA	Complement A	0	0	1	0	1	1	1	1	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7	STC	Set carry	0	0	1	1	0	1	1	1	4
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7	CMC	Complement carry	0	0	1	1	1	1	1	1	4
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7	DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	<b>CONTROL</b>										
ANI	And immediate with A	1	1	1	0	0	1	1	0	7	EI	Enable interrupts	1	1	1	1	1	0	1	1	4
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7	DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7	NOP	No-operation	0	0	0	0	0	0	0	0	4
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7	HLT	Halt	0	1	1	1	0	1	1	0	5
<b>ROTATE</b>																					
RLC	Rotate A left	0	0	0	0	0	1	1	1	4	<b>EXTRA 8085A INSTRUCTIONS</b>										
RRC	Rotate A right	0	0	0	0	1	1	1	1	4	RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
											SIM	Set Interrupt Mask	0	0	1	1	0	0	0	4	

NOTES: 1. DDD or SSS; B=D00. C 001. D 010. E 011. H 100. L 101. Memory 110. A 111.

2. Two possible cycle times. (6/12) indicate instruction cycles dependent on condition flags.

\*All mnemonics copyright ©Intel Corporation 1977

## SOFTWARE

The 8080/8085 family is probably better supported in software than any of the other microprocessors. There is so much software available that it would be quite impossible to list it all. The key to 8080/8085 software is the CP/M disc operating system produced by Digital Research of Pacific Grove, California. Since its introduction, CP/M has become the standard microprocessor operating system and has therefore encouraged large numbers of software writers to produce Interpreters, Compilers, Word processors, games, and utilities. CP/M itself is quite basic but is written in 8080 code so that it is directly compatible with 8080, 8085 and Z80 based systems. So popular is it, that personal computers based on other processors, such as the Apple which uses a 6502, are often upgraded to CP/M compatibility by the addition of an extra 8080 or Z80 processor card so that access to CP/M compatible software is possible.

Of course, not all systems can use discs, and in this case stand-alone software is desirable. Software distribution is more difficult in this case, but a number of 8080/8085 Tiny Basic Interpreters have been published and there are several books with software listings available. I can recommend the inexpensive Scelbi books which give listings for an 8080 Monitor, Editor, and Assembler.

## INTERFACING

The 8080A and 8085A interface to both memory and I/O devices by means of READ and WRITE machine cycles which each have an associated control line output ( $\overline{RD}$  and  $\overline{WR}$  respectively). An additional control line  $\overline{IO/\overline{M}}$  informs bus users whether the cycle applies to a memory or an I/O device. The main difference between the two processors is the multiplexed bus structure of the 8085A where the eight low order address bits (A0-A7) share the same pins as the data bus and are therefore labelled ADO-AD7. The special purpose 8085A interface chips, the 8155 RAM/IO/TIMER and the 8355 ROM/IO, have internal demultiplexing circuitry so that they can work directly from the 8085 bus. Other devices including general purpose ROM and RAM chips, and interface chips such as the UART, need a non-multiplexed bus and this can be easily achieved by using an external 8 bit latch such as the 74LS373. The 8085A provides a special signal, ALE, to cause the low address data to be latched. With this latch in use, the bus structures of the 8080A and 8085A are virtually identical.

The most versatile interrupt line, INT on the 8080A and INTR on the 8085A can cause a vector to any location in memory with the use of external hardware to force a CALL (Jump to subroutine) instruction on to the bus. This three byte instruction is best generated by the 8259A interrupt controller which will provide separate interrupt vectors for up to eight interrupts. A much simpler scheme can also be used to generate single byte RESTART instructions instead, but of course these vector to fixed locations in low memory. In addition to this general purpose interrupt, the 8085A has four additional fixed vector interrupt lines which do not need any external hardware support. These inputs, RST 5.5, RST 6.5, RST 7.5 and TRAP, cause the processor to vector to locations in low memory positioned between the RESTART vectors which remain available. The TRAP interrupt puts right one criticism of the 8080A by providing a non-maskable interrupt which cannot be ignored. This is useful for important occurrences such as power failure.

One major strength of the 8080A/8085A family is the very wide range of directly compatible interface devices available. In addition to the 8259A Interrupt controller there is the 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART), the 8255A Programmable Parallel Interface (PPI), the 8271 Floppy Disc Controller, the 8278 Programmable Keyboard Interface and many, many more, including devices made for this family by other manufacturers such as N.E.C. Both processors are compatible with a wide range of standard memory components including static and dynamic RAM, ROM, EPROM, and EEPROM.

## APPLICATIONS

Unless you are an existing 8080A fan, there would seem to be little point in using this processor for new applications since both the Z80 and the 8085A are actually cheaper and, of course, more powerful. The 8085A still has a part to play in controller applications which can make good use of its extra Interrupts, Serial I/O lines, and the useful 8155A peripheral device, but it is really best suited to applications which are too "big" for one of the single chip processors like the 8748, but not so big that they need one of the newer 16 bit devices. For data processing applications the Zilog Z80 is probably a better choice. Perhaps the main obstacle to using the 8085A in home projects is the inability to use the 8355A masked ROM and I/O device and the consequent need to use a standard EPROM such as the 2716 which therefore makes the use of a bus demultiplexer latch necessary.



# Using Your 6 FREE CABLE TIES

**B**y now you will no doubt have found the 6 Ty-It cable ties attached to the front of this issue. Just in case you don't know what to do with them (!) here are a few suggestions, some buying information and details of other related products. Even if you don't build any of our projects the ties will be useful in a number of other applications.

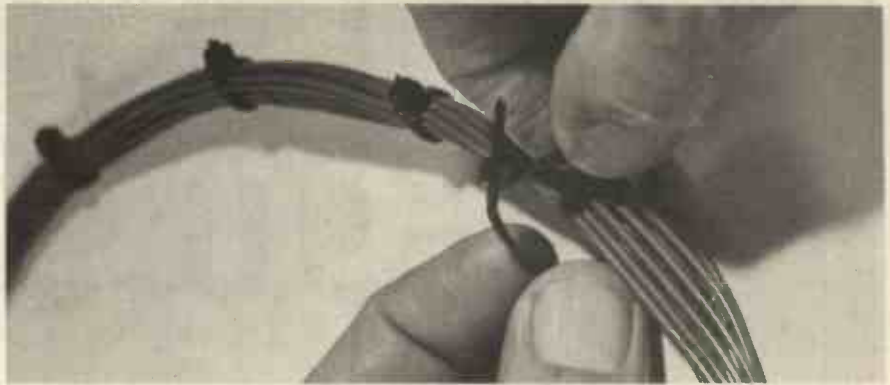
Many of the devices in current use which have been designed for the specific purpose of securing electrical cables employ plastics, either wholly, or as a covering for stronger materials such as stainless steel or aluminium. Our free Ty-It ties are made of nylon and are from the Hellermann Insuloid range.

Broadly, the range can be divided into harnessing ties, with the cables only tied to one another, and fixing ties which hold single cables or bundles of wires to chassis, cabinet, machine or cable tray. A third class provides a solid anchorage for a flexible lead—say into a domestic appliance—sometimes with the added feature of a block terminal.

Ties and fastenings which were once pieces of string and insulated staples, are now almost exclusively produced as plastic mouldings. Some flat metal types are made in stainless steel or aluminium, but these are normally plastic covered. Nylon 66 is a commonly used standard material with a high tensile strength. For outside use where weather resistance is needed there is a special 2 per cent carbon black grade and there is also a heat stabilised grade which extends the life at 150 degrees C.

## STANDARD TIES

The Ty-It ties are made in tough, flexible nylon 66. They are offered in various lengths and with alternative types of fixing heads. The size range covers 2.5mm to



7.6mm strap width with lengths from 120 to 540mm. Note that the length can be extended in an emergency by joining ties.

It is in the field of flexible ties that the greatest variety of designs is found, simply because of the infinite variety of applications such as TV receivers, business machines, motor cars, commercial vehicles, machine tools, switchgear and telecommunications, each of which can present different problems of accessibility, the concealment of fastenings and the panel material or chassis wall.

There is a variety of mounting bases or cradles designed for fixing to panels and walls before anchoring down the loom, these being arranged to accept standard nylon ties. Rivet fixing is possible for releasable and permanent ties where corrosion-proof anchorage and a sealed hole are sought. A bolted-on version is available for restricted spaces and there is a further version which lifts the loom clear of the panel surface and is recommended for tropical and high humidity conditions.

Quickly installed and often very convenient is an adhesive base cradle, which also takes a standard tie. The adhesive should be checked in the case of high temperature installations.

## CLIPS

Successor to the insulated staple perhaps and useful for domestic appliances, radio and automotive work are moulded PVC clips. Screwed down or self-adhesive (Stiki-Clips) versions are made for single

**Ty-It Releasable Ties, available in 140mm and 250mm sizes; Ty-It Non-Releasable Ties, available in 100mm, 150mm and 200mm sizes; Stiki-Clips for 6mm, 13mm and 18mm maximum overall diameter**



core cables, pairs or flat twin cables. These clips save time in securing cables and harnesses particularly where fixing holes are impractical.

## APPLICATIONS

For every cable and every situation there is a potential tying and fixing problem, but one that has probably been solved before and its solution entered into the standard repertoire of the tie maker. Sometimes cable routing has to be chosen to suit available fixing methods—for instance to avoid having to drill holes that will appear on external surfaces—but even this problem is now disappearing with the adoption of self-adhesive devices.

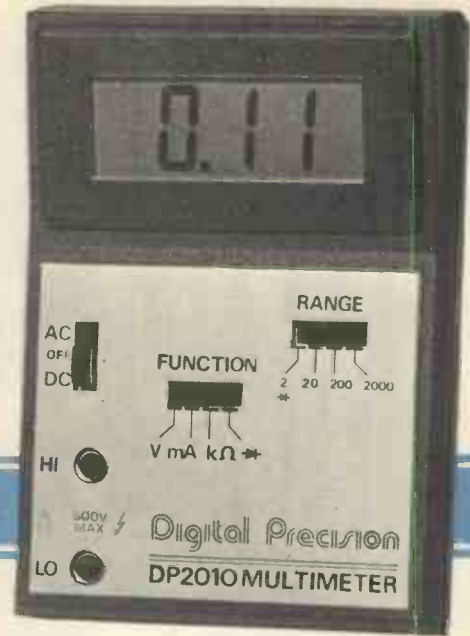
Cable ties have many other uses outside the original field of electrical wiring. The securing of large or heavy components to a p.c.b. and the fixing of light pneumatic or fluidic tubing are obvious ones, but in virtually any application where a piece of tape or string can be used a cable tie will probably do it better. With this wide range of fasteners the only limitation is the ingenuity of the designer in choosing and applying the right one.

**Ty-It ties and Stiki-Clips are available from stores throughout the country. For further details contact Hellermann Insuloid, Sharston Works, Leestone Road, Wythenshawe, Manchester M22 4RH. Tel 061-998 5415-8.**

# DMM

## MARTIN KENT

### A compact multimeter with digital read-out



THIS compact multimeter features twenty-one ranges with six functions. L.c.d. read-out gives excellent readability with extended battery life. The complete instrument calibration is by one multi-turn trimming potentiometer.

#### BOARD DESCRIPTIONS

The instrument comprises of two printed circuit boards. The display unit is a self-contained panel meter with l.c.d. read-out, which measures voltages within the range 0–200mV. It displays the magnitude and polarity of the applied voltage. The other board contains the conditioning circuitry to change all inputs into a voltage output in range 0–200mV.

#### PANEL METER MODULE

The heart of the meter is the 7126 i.c. which is a complete dual-slope integration analogue to digital converter. It consumes typically only 50µA and drives the l.c.d. directly. Components R25 and C6 determine the Integrator time constant, and C7 reduces the susceptibility to noise of the auto-zero circuit. The l.c.d. has an auto-zero feature which gives a zero reading when the analogue input is zero volts.

An input filter is formed by R27 and C8 and assists with overload protection. The frequency of the internal oscillator is determined by C10 and R28 and provides typically three samples per second. The module has a full scale reading of 199.9mV. IC3 is a high stability reference and a potential divider is formed across this so that VR1 can be adjusted to produce a  $V_{ref}$  of 100mV. A low-battery detection circuit is included to provide advance warning of battery failure directly on the display.

A potential divider is formed across the supply by R31 and R33 and when the supply voltage falls below a threshold level, the collector of TR1 goes high. EX-OR gate IC4a then acts as an inverter to provide the required drive signal for the LO BAT warning. EX-OR gate IC4b output may be used to drive the decimal points.

#### CONDITIONING BOARD

The circuit diagram of the multimeter is shown in Fig. 1. Switch S3 selects d.c. or a.c. functions whilst connecting the battery to the appropriate circuitry via S3c and S3d. When the switch is in the centre 'off' position, S3a and S3b isolate the input to the module to prevent damage. Switch sections

S1a and S1b route the input to voltage, current, resistance or diode check stages.

For the measurement of the d.c. voltage an input attenuator is formed by resistors R1 to R5 which are high stability metal film types. The attenuator settings ensure that each input range is reduced to 200mV full scale for input to the module. The input impedance of the multimeter is the standard value of 10 megohms and ensures that negligible current is drawn from the voltage source.

When a current range is selected, S2b selects one of four shunt resistors R6 to R9, each of which should develop 200mV with full scale current input. The value of R9 is chosen to allow for the effect of switch resistance. A series chain configuration could have been used for current sensing but the low value resistors required could be difficult to obtain.

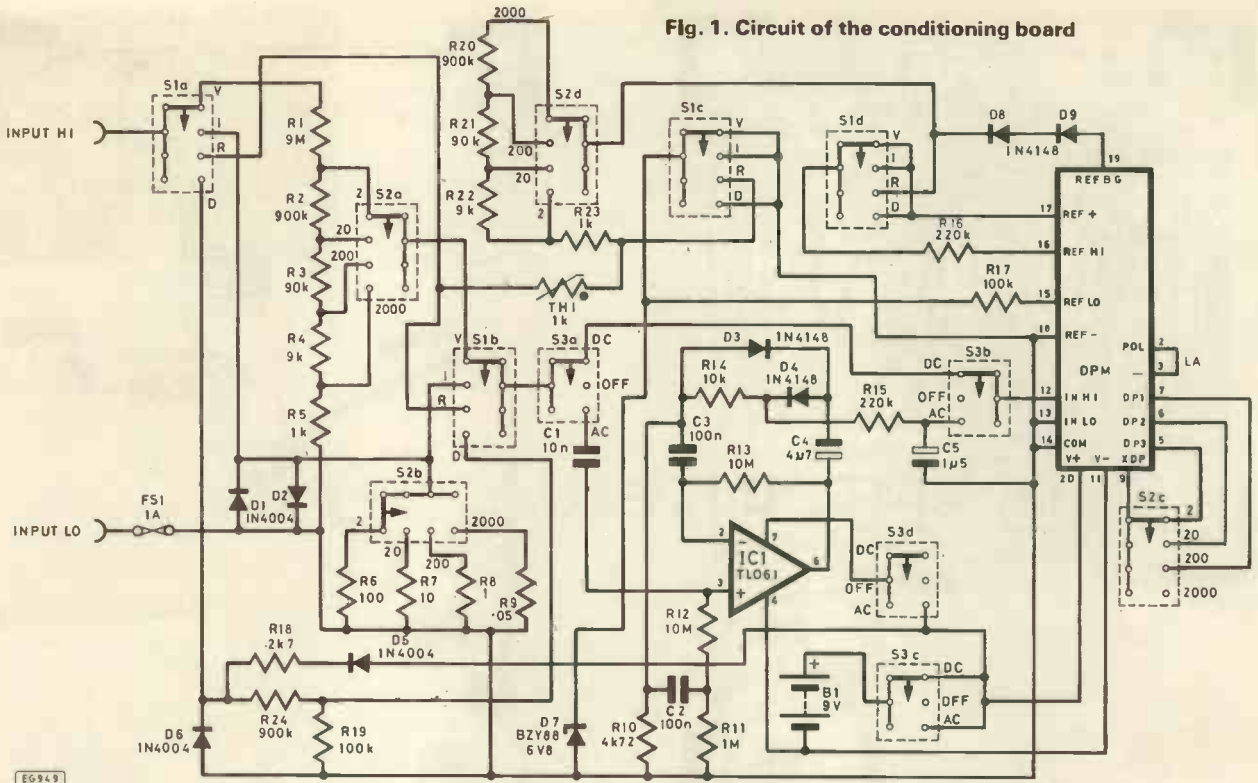
A fuse protects against excessive input currents and diodes D1 and D2 protect the instrument from the application of high input voltages.

### SPECIFICATION

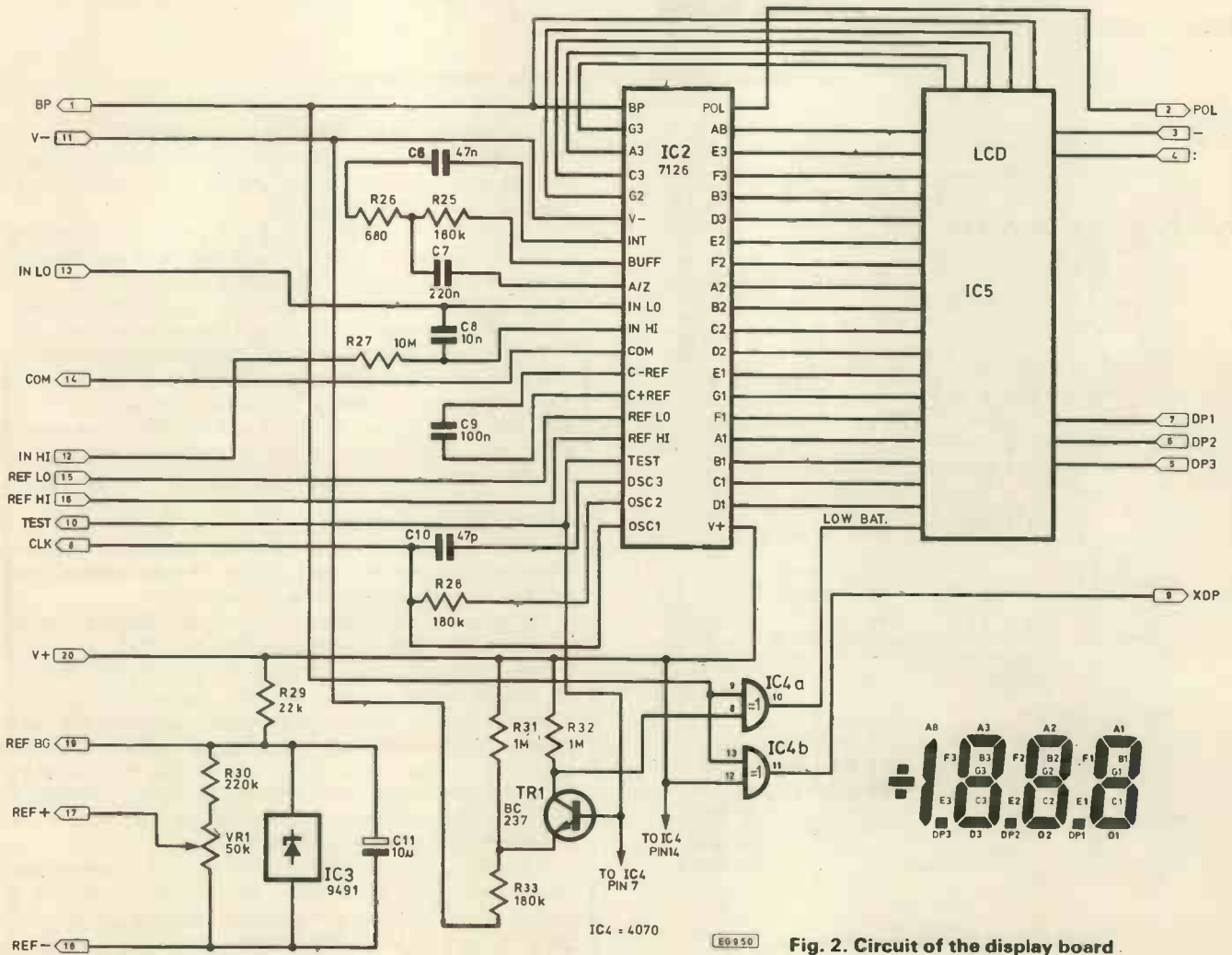
Function	F.s.d.	Resolution	Accuracy	Protection
Volts (d.c.)	2V	1mV	1% ± 1 digit	500V for one minute
	20V	10mV	1% ± 1 digit	
	200V	100mV	1% ± 1 digit	
	500V	1V	1% ± 1 digit	
Current (d.c.)	2mA	1µA	1% ± 1 digit	1A/250V
	20mA	10µA	1% ± 1 digit	
	200mA	100µA	3% ± 1 digit	
	2A	1mA	5% ± 1 digit	
Volts (d.c.)	2V	1mV	2% ± 5 digit	500V for one minute
	20V	10mV	2% ± 5 digit	
	200V	100mV	2% ± 5 digit	
	500V	1V	2% ± 5 digit	
Current (d.c.)	2mA	1µA	2% ± 5 digit	1A/250V
	20mA	10µA	2% ± 5 digit	
	200mA	100µA	4% ± 5 digit	
	2A	1mA	7% ± 5 digit	
Resistance	2k	1	1% ± 1 digit	260V r.m.s.
	20k	10	1% ± 1 digit	
	200k	100	1% ± 1 digit	
	2M	1k	1% ± 1 digit	
Diode Test	2V	1mV	1% ± 1 digit	260V r.m.s.



Fig. 1. Circuit of the conditioning board



EG949



EG950

Fig. 2. Circuit of the display board

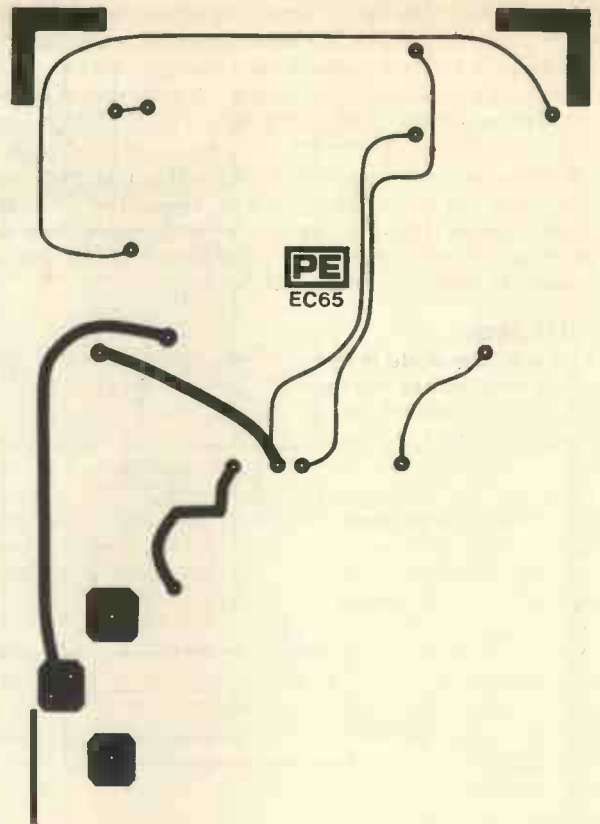
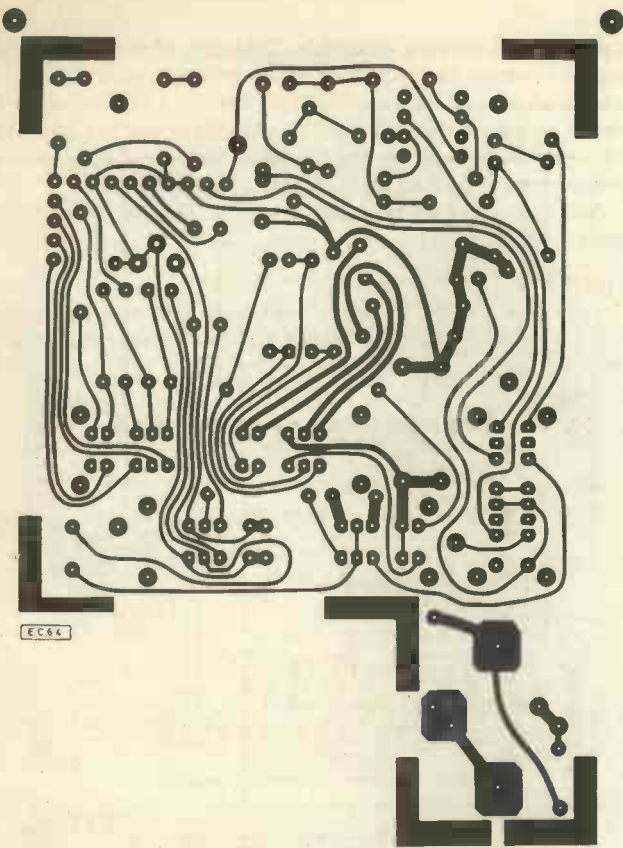


Fig. 3. Double sided p.c.b. design for the Multimeter

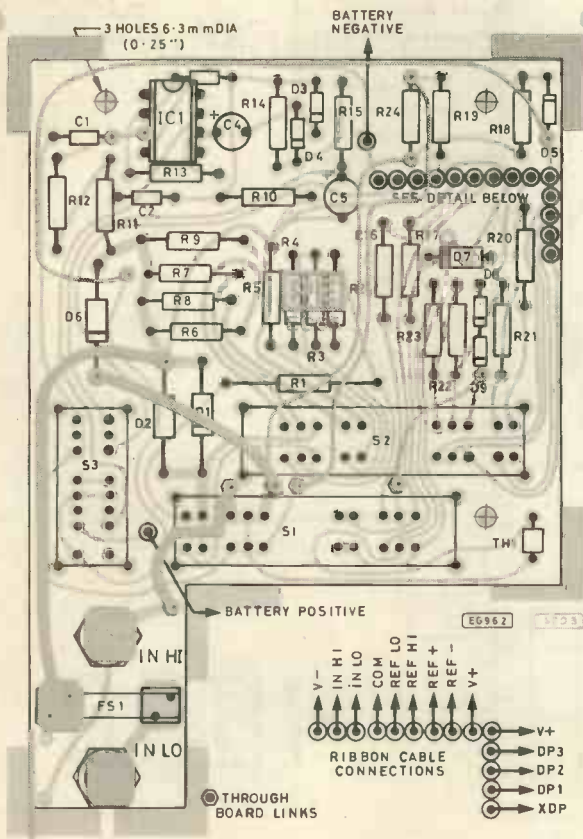


Fig. 4. Component layout for the p.c.b.

### A.C. VOLTAGE AND CURRENT RANGES

When S3a selects a.c. functions, the output from either the voltage attenuator or current shunts is fed through C1 to remove any d.c. component.

The operational amplifier IC1 is a TL061 connected as a precision rectifier. The j.f.e.t. input results in high input impedance and the supply consumption is only 250µA. Diodes D3 and D4 rectify the alternating input and the positive component is sampled by R13 and filtered by R15 and C5.

The circuit is mean sensing and calibrated to indicate the r.m.s. value of sine wave inputs by establishing the correct gain of the amplifier stage. The gain is set by R14 and R10 and use of the values indicated will eliminate the need for calibration. Alternatively, a 10k potentiometer could be substituted for R10.

### RESISTANCE RANGES

In order to minimise the components required for resistance measurement and eliminate the need for calibration adjustment, a ratiometric method is employed.

For all other multimeter functions, the voltage reference within the module is employed and the 100mV output is connected to the module reference inputs via S1c and S1d. All inputs to the module are thus compared against the reference voltage. For resistance measurement the supply voltage is applied across the reference resistor R<sub>r</sub> and the unknown resistor R<sub>x</sub>. The voltage developed across each resistor is dependent upon the ratio of the two resistors and the value of the unknown resistor may be read directly using the equation  $Reading = 1000 R_x/R_r$ .

Metal film resistors R20 to R23 are used as references. It would have been possible to use the resistors from the voltage attenuator but the resistors required are in reverse order to those for the voltage ranges, resulting in the decimal



points on the display being incorrectly positioned. Additional switch sections would be required to provide correct decimal point location and to isolate R5 from circuit common.

Resistance measurements should not be made on live circuits but protection against the application of high input voltage is provided. Thermistor TH1 has a nominal value of 1k at room temperature and diode D7 will turn on at approximately 6-8V to shunt the applied voltage. When D7 draws current through TH1 the thermistor temperature rises and due to the positive temperature coefficient the resistance increases so limiting the input current.

### DIODE TEST

When a silicon diode is forward-biased into conduction the voltage drop across the device is approximately 0.6V. The 200mV full scale of the module is however too low to measure this voltage drop. When S1 selects the 'Diode Test' function, biasing from the battery is available via D5 and R18. When the applied diode is forward-biased the voltage drop will be attenuated by a factor of 10 by R24 and R19 to bring it within the measurement range of the module. If the 2V range is selected the decimal point will be correctly positioned on the display for direct readout of the diode voltage.

If the applied diode is open-circuit or reverse-biased it will not conduct and the display will be over-range. If the diode is short-circuit the display will read zero. Because of the accuracy of measurement available close matching of transistor  $V_{be}$  can be carried out.

The diode test should not be made on live circuits but diode D6 will protect the instrument from the application of high negative input voltages which would otherwise be shunted onto the supply by D5. Positive input voltages are held off by D5 and safely attenuated by R24 and R19.

### CONDITIONING MODULE

Components should be checked against the component list and assembly commenced by soldering the through-board pins in place. As assembly proceeds, the solder pads on the top surface of the p.c.b. should be soldered to ensure circuit continuity.

Solder the resistors and capacitors in place, followed by the diodes and integrated circuit, carefully noting the orientation. The three slider switches should now be fitted to the p.c.b. and prior to soldering check that each switch is perpendicular to the board and pushed down as far as possible. The fuse clips and fuse may now be fitted followed by the p.c. mounting terminals, battery connector leads, and ribbon cable. The other end of the ribbon cable may now be soldered to the panel meter module.

### CONSTRUCTION

A plated-through-hole p.c.b. is used for the digital precision

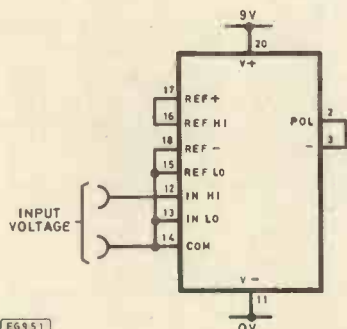


Fig. 5. Module connections for measuring a floating voltage source with 200mV full scale and autopolarity indication implemented

multimeter to simplify assembly. Soldering of components is required only on the underside of the printed circuit board.

Link LA should be inserted first. Resistors and capacitors should be positioned followed by VR1, TR1 and the i.c.s. As the i.c.d. is required to sit over IC1 and capacitors, these components should be arranged tight to the p.c.b.

The display should be carefully positioned and all components soldered in place.

### TESTING

The DPM is a self-contained instrument and may be tested and calibrated before connection to conditioning modules if required.

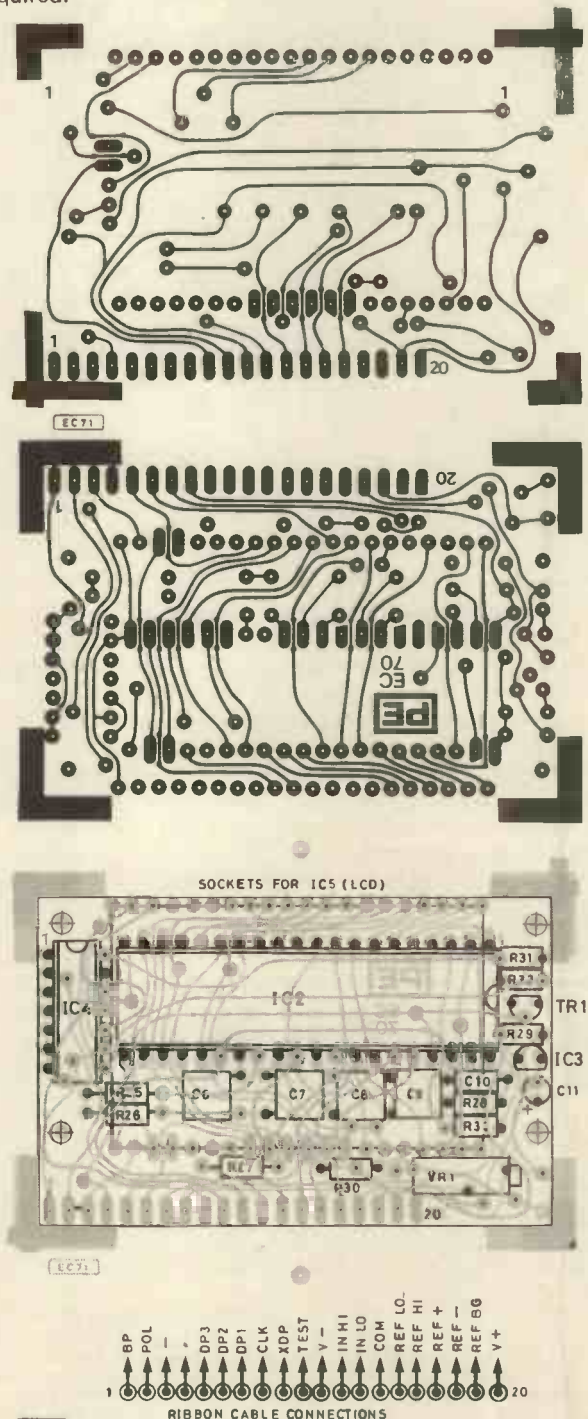


Fig. 6. Double sided p.c.b. and component layout for the display board

## COMPONENTS . . .

### Resistors

R1	9M metal film
R2, R20, R24	900k (3 off) metal film
R3, R21	90k (2 off) metal film
R4, R22	9k (2 off) metal film
R5, R23	1k (2 off) metal film
R6	100 metal film
R7	10 metal film
R8	1 metal glaze
R9	0.05 wirewound
R10	4k72 metal film
R11	1M carbon film 5%
R12, R13	10M (2 off) carbon film 5%
R14	10k metal film
R15, R16	220k (2 off) carbon film 5%
R17	100k carbon film 5%
R18	2k7 carbon film 5%
R19	100k metal film
TH1	thermistor PTC 1k 260V a.c.
R25	miniature 180k carbon film 5%
R26	680 carbon film 5%
R27	10M carbon film 5%
R28	miniature 180k carbon film 5%
R29	miniature 22k carbon film 5%
R30	miniature 220k carbon film 5%
R31, R32	miniature 1M (2 off) carbon film 5%
R33	miniature 180k

### Semiconductors

D1, D2	1N4004 (2 off)	IC2	7126
D3, D4, D8, D9	1N4148 (4 off)	IC3	9491
D5, D6	1N4004 (2 off)	IC4	4070
D7	8ZY88 6V8	IC5	3½ digit LCD
IC1	TLO61CP	TR1	BC237

### Capacitors

C1	10n polyester 100V
C2, C3	100n polyester 100V (2 off)
C4	4µ7 elect. 16V
C5	1µ5 elect. 16V
C6	47n polyester
C7	220n miniature polyester
C8	10n miniature polyester
C9	100n miniature polyester
C10	47p polystyrene
C11	10µ elect. 16V

### Switches

S1, S2	4 pole 4 way slide (2 off)
S3	4 pole 3 way

### Miscellaneous

Case
2 p.c.b.s
20mm p.c.b. fuse clips
20mm fuse 1A
PP3 battery connector
4mm terminals (2 off)
Through board pins (6 off)
Ribbon cables (10 way + 4 way)

A kit of parts is available from **Lascar Electronics Ltd., Oakland House, Reeves Way, South Woodham Ferrers, Chelmsford, Essex CM3 5XQ** at £19.95 including p/p and VAT

Fig. 5 demonstrates how the instrument may be connected to measure a floating voltage source in the 0–200mV range with the DPM powered from a 9V battery. The voltage between COM and V+ should be approximately 2.8V and battery consumption about 200µA. When the IN HI and IN LO connections are sorted together, the display should be 000. With a 100mV source connected between IN HI and IN LO the display should read 1000 when VR1 is adjusted. Calibration may also be carried out by comparison with a meter of known accuracy.

The testing of the instrument should be carried out before the case is fitted and after checking all the soldering the battery should be connected. With the input switch to 20V d.c. the display should be 0.00 and the voltage between Input

LO and battery positive should be approximately 2.8V. The voltage between pins 5 and 6 of the module should be 100mV. Apply a 10V input and adjust VR1 until the display reads 10.00. Switch to 20mA d.c. and check the reading with a 10mA source connected. Switch to 20k range and check that with the input open circuit the display shows a 1 in the most significant digit with the other three digits suppressed, which is the over-range indication. Connect a standard 10k resistor and check the reading.

With the instrument switched to 20V a.c. apply a 10V a.c. source and check the display.

The diode test function should be checked with a known diode and the reading should be approximately 600mV with a silicon diode or 300mV with a germanium diode.

## BAZAAR

**WANTED** ultrasonic cleaner, small size suitable small components, must be good condition. Reasonable price. G. A. Chappel, 'Auchenroch', Arrochar, Dunbartonshire.

**TOKUDEN** eight inch twin cone speakers. Eight ohms, seven watts max. unused £7 the pair. N. Wakelling, 8 Milton Park, Aviemore, Inverness-shire, Scotland. Tel: (0479) 810 818.

**PRE-AMP** kit. Already made with ILP transformer. No time to test. £40. Tel: Gravesend 23119. Steven Kwan, 28 Ferguson Avenue, Gravesend, Kent.

**16K NASCOM 2** with Gemini RAM card, p.s.u. graphics ROM. Fully operational mounted in 19 inch rack. £395. A. Gifford, Little Pundells, Bartley, Southampton SO4 2LN. Tel: 042 127 2392 (Evenings).

**PRACTICAL** Electronics Sep. '77 to date. E.T.I. April '78 to June '81. Everyday Electronics Feb. '75 to Aug. '77 offers. Mr. A. Pettitt, 2 Caburn View, Firle, Nr. Lewes, Sussex. Tel: Glynde 492.

**WANTED** push pull output transformer to match N78 valves for HMV car radio model 4200. Mr. G. W. Nickolds, 15 Cambridge Rd., Lee-on-Solent, Hants. Tel: 550963.

**AVO** Model 8 MKIII small crack on case but fully working £60. Phone: Tamworth 896522.

**ZX81** 16K full size keyboard leads p.s.u. User Manual, excellent value £90 o.n.o. D. Richardson, 26 Kelvin Road, Bellshill, Lanarkshire ML4 1LN.

**UK101 8K** CEGMON, numeric keypad, P.S.G., 300/600 Baud, R.T.S. output, cased, fan. Lots software £165 o.n.o. Brian Andrews, 77 Valiant Hse., Valley Grove, Charlton S.E.7. Phone after 6p.m. 853 4171.

**WANTED** coil winder, hand or motor driven for transformer winding. H. E. Enfield. Phone 412058. "Springtime", Withies Lane, Midsomer Norton, Avon, BA3 2JE.

**P.E. STRING ENSEMBLE**, only needs wiring up. Complete £90 ono. Pair of 38 radio sets—offers. L. Fletcher, 21 Shakespeare Avenue, Andover, Hants SP10 3DR. Tel: Andover 65368.

**WILL PERSON** from Aylesbury, who sent cash for book, my recent advert send name and address. G. A. Noble, 50 Croft Hill Road, Slough, Berks SL2 1HF.

**UK101, 8K**, cased, 300/600 Baud, lots s/ware, computer mags. £120 o.n.o. Tel: (0384) 75168 (after 4.00 p.m.). Ian Lavender, 288 Stourbridge Road, Holly Hall, Dudley, West Midlands.

**WANTED** ZX80 with manual and circuit diagram. 94 The Straits, Dudley, West Midlands DY3 3BH.

**UK101 8K 2MHz**. Four premier cassettes. Malik invaders and fruit machine. Many programs from magazines £110. T. C. Smith, c/o T. M. Craig, 129 High St., Dumbarton, Strathclyde (Mornings).

**WANTED** service manual or circuit diagram for Tektronix type 561A Oscilloscope. Mr. J. Bowen, 41 Lower Gardiner Street, Dublin 1, Ireland. Tel: 01-74 52 00.



# CB Synthesiser

## DUNCAN HEAD

B.Sc. (Hons)

**A**T LAST after a five month long wait the Sanyo LC7137 PLL synthesiser has become generally available in the UK. (No explanation by Sanyo or their distributors for this delay, although one may hazard a guess.)

This device has been utilised in the following circuitry and is capable of producing the required frequencies for receiving and transmitting 27MHz FM CB signals. The circuitry is very versatile indeed and has a multiplicity of inputs/outputs that may be combined with crystal controlled portables (such as the *PE* Ranger), FM communications receivers and FM transceivers operating in the 26MHz to 28MHz band.

The solution is a great deal more straightforward than employing the synthesiser techniques adopted by some companies which may use up to three separate i.c.s plus two or three different crystals.

The LC7137 is a 20-pin CMOS i.c. that forms a single crystal PLL system. It may be programmed via a 6-bit BCD input using an encoded switch or BCD logic. The receive local oscillator is generated directly with a 10.695MHz (low) IF offset; however, this may be mixed with the 10.24MHz crystal frequency to produce the local oscillator output with a 455kHz (low) IF offset. The transmit frequency is generated at half the output frequency. This is because the maximum input frequency of the programmable divider is 20MHz and at this lower frequency the modulation characteristics are more linear.

### HAVE YOU HAD YOUR PLL?

Phase-Lock-Loop frequency synthesisers have become standard in all 40 channel CBs and communications receivers. These techniques have eliminated the use of separate crystals for every channel. The actual concept stems from as early as the 1930s but until it became available in an i.c. its use was not generally cost effective. Many of the earlier PLL devices were of the analog type, but the advanced types such as the LC7137 and its hierarchy are digital in operation. We must thank the American CB market for the development of the PLL over the last ten years. The first generation synthesisers employed as many as nine i.c.s; however, the availability of LSI (Large Scale Integration) devices over the last few years has reduced the number to not more than two.

### IT'S ALL DONE WITH FREQUENCY

Fig. 1 shows the equivalent block diagram and external components. The important features are an on-board crystal oscillator, reference divider, programmable divider with associated ROM decoding logic and phase detector.

The reference frequency of 5kHz (5.000226kHz) is derived from the 10.2405MHz crystal frequency by dividing down by 2048. In practice a standard 10.24MHz crystal may be trimmed to this frequency. The reference frequency

is not exactly 5kHz since the programmable divider uses only 4 decades to achieve the UK 27MHz CB specifications with the 1.25kHz "offset"; however, the final frequencies are well within the tolerances and this error will not affect the transceiver performance.

A BCD signal is applied via the channel data inputs, D1-D6, to the internal ROM. Table 1 shows the program data against the channel number and internal divisor ratio. Data lines D1-D4 form the "units" digit of the channel code (D1 = LSB) and D5 and D6 form the "tens" digit of the code (D6 = MSB), the next two bits of the "tens" code being unnecessary.

The internal memory decodes this data and changes the divisor ratio depending on the channel and if RX or TX is required. The ratio of the RX to TX divisor values is due to the RX frequencies being generated with the 10.695MHz IF offset and the TX frequencies being generated at half the output frequency.

For example, channel 20, RX frequency = 27.79125MHz -  
10.695MHz  
TX frequency = 27.79125MHz/2  
thus RX/TX = 1.23033  
Ratio of actual divisor ratio = 3419/2779  
= 1.23029

These ratios are not exactly correct as described earlier; however, this error is very small indeed and does not significantly change the receive frequency.

The programmable divider thus divides down the input frequency to approximately 5kHz. This is then compared with the 5kHz reference signal in the phase detector. This, as with most of the other internal circuitry, is achieved digitally. In this application the phase detector has three possible conditions of its output circuit, i.e. it provides three states to the following circuit, the loop filter. These are, an off state, a negative going state and a positive going state. When the loop is locked, i.e. the VCO is running at the correct frequency and the divided down input frequency and reference frequency are exactly in phase, the detector is in the off state and no error signals are generated. When the divided down input frequency lags behind the reference frequency the detector's output pulses are negative going, and when it leads the reference frequency the output pulses are positive going. These output pulses are inverted and amplified in an active integrator stage between the detector and VCO to provide the proper direction of bias change on the varicap diode controlling the VCO.

## 40 CHANNELS FOR ALL

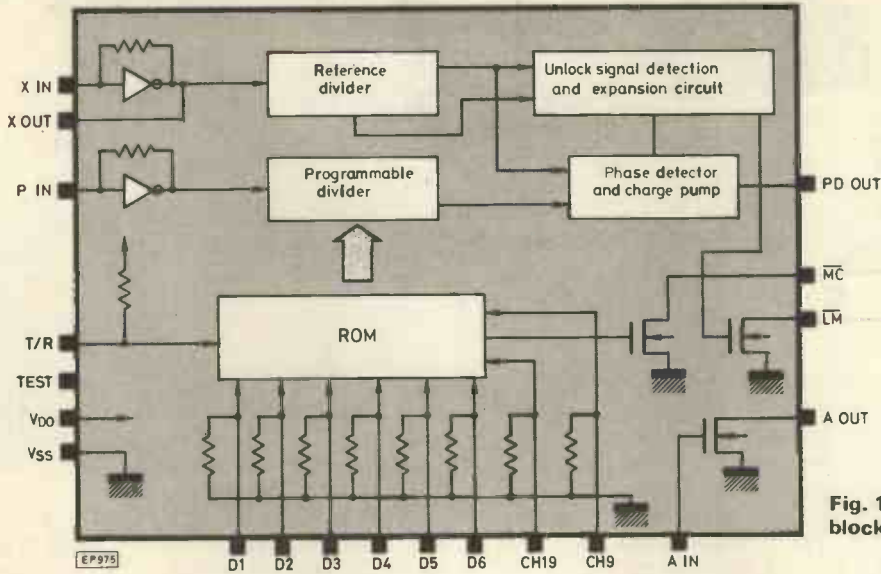
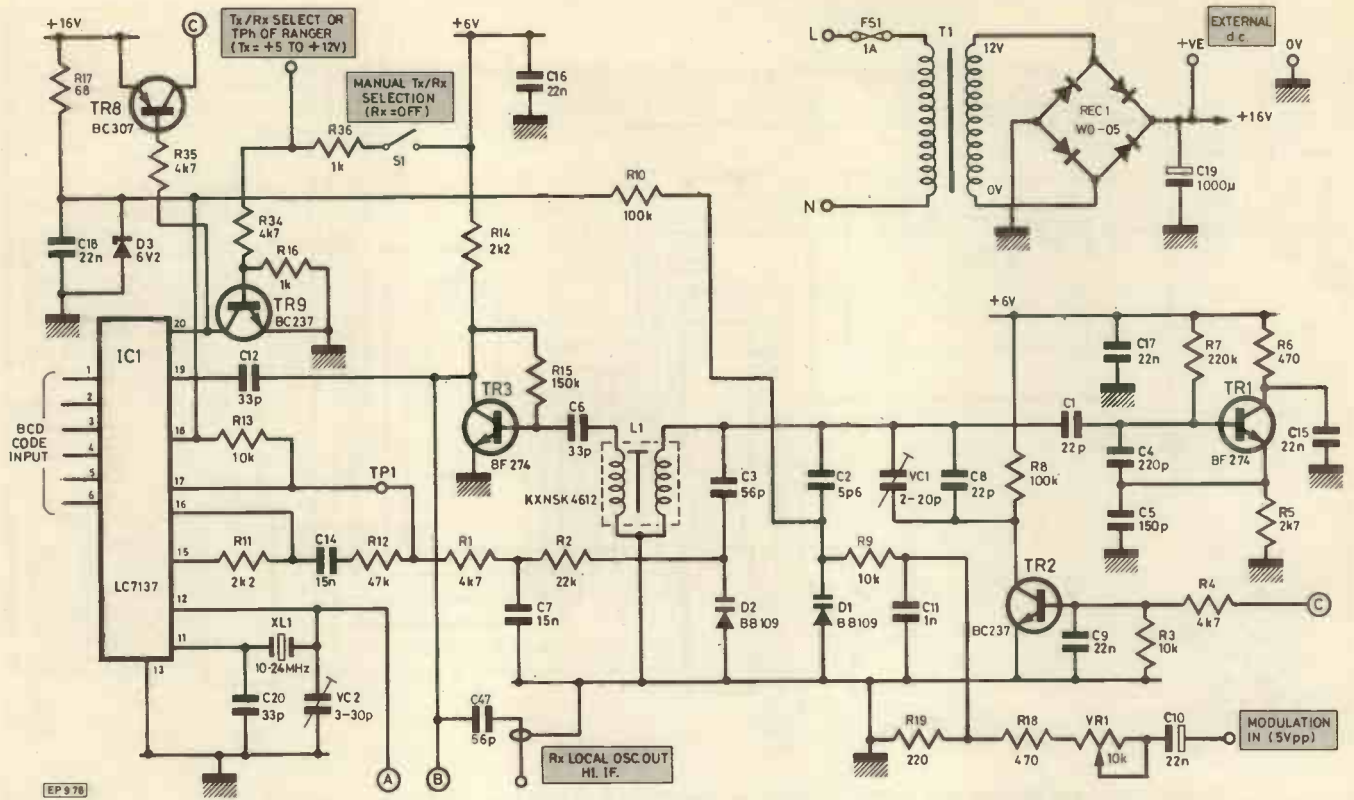


Fig. 1. Equivalent circuit block diagram

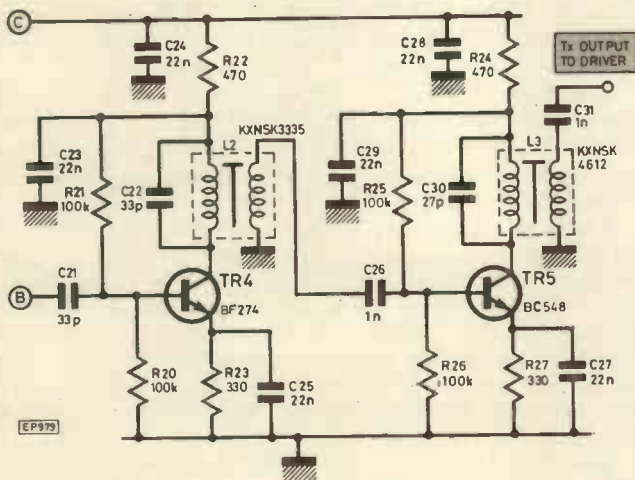
CH	Channel Frequency	Program Code						RX (T/R = 1)		TX (T/R = 0)	
		D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	Divisor	VCO Freq.	Divisor	VCO Freq.
1	27.60125	1	0	0	0	0	0	3381	16.9057	2760	13.8006
2	27.61125	0	1	0	0	0	0	3383	16.9157	2761	13.8056
3	27.62125	1	1	0	0	0	0	3385	16.9257	2762	13.8106
4	27.63125	0	0	1	0	0	0	3387	16.9357	2763	13.8156
5	27.64125	1	0	1	0	0	0	3389	16.9457	2764	13.8206
6	27.65125	0	1	1	0	0	0	3391	16.9557	2565	13.8256
7	27.66125	1	1	1	0	0	0	3393	16.9657	2766	13.8306
8	27.67125	0	0	0	1	0	0	3395	16.9757	2767	13.8356
9	27.68125	1	0	0	1	0	0	3397	16.9857	2768	13.8406
10	27.69125	0	0	0	0	1	0	3399	16.9957	2769	13.8456
11	27.70125	1	0	0	0	0	1	3401	17.0057	2770	13.8506
12	27.71125	0	1	0	0	1	0	3403	17.0157	2771	13.8556
13	27.72125	1	1	0	0	1	0	3405	17.0257	2772	13.8606
14	27.73125	0	0	1	0	1	0	3407	17.0357	2773	13.8656
15	27.74125	1	0	1	0	1	0	3409	17.0457	2774	13.8706
16	27.75125	0	1	1	0	1	0	3411	17.0557	2775	13.8756
17	27.76125	1	1	1	0	1	0	3413	17.0657	2776	13.8806
18	27.77125	0	0	0	1	1	0	3415	17.0757	2777	13.8856
19	27.78125	1	0	0	1	1	0	3417	17.0857	2778	13.8906
20	27.79125	0	0	0	0	0	1	3419	17.0957	2779	13.8956
21	27.80125	1	0	0	0	0	1	3421	17.1057	2780	13.9006
22	27.81125	0	1	0	0	0	1	3423	17.1157	2781	13.9056
23	27.82125	1	1	0	0	0	1	3425	17.1257	2782	13.9106
24	27.83125	0	0	1	0	0	1	3427	17.1357	2783	13.9156
25	27.84125	1	0	1	0	0	1	3429	17.1457	2784	13.9206
26	27.85125	0	1	1	0	0	1	3431	17.1557	2785	13.9256
27	27.86125	1	1	1	0	0	1	3433	17.1657	2786	13.9306
28	27.87125	0	0	0	1	0	1	3435	17.1757	2787	13.9356
29	27.88125	1	0	0	1	0	1	3437	17.1857	2788	13.9406
30	27.89125	0	0	0	0	1	1	3439	17.1957	2789	13.9456
31	27.90125	1	0	0	0	1	1	3441	17.2057	2790	13.9506
32	27.91125	0	1	0	0	1	1	3443	17.2157	2791	13.9556
33	27.92125	1	1	0	0	1	1	3445	17.2257	2792	13.9606
34	27.93125	0	0	1	0	1	1	3447	17.2357	2793	13.9656
35	27.94125	1	0	1	0	1	1	3449	17.2457	2794	13.9706
36	27.95125	0	1	1	0	1	1	3451	17.2557	2795	13.9756
37	27.96125	1	1	1	0	1	1	3453	17.2657	2796	13.9806
38	27.97125	0	0	0	1	1	1	3455	17.2757	2797	13.9856
39	27.98125	1	0	0	1	1	1	3457	17.2857	2798	13.9906
40	27.99125	0	0	0	0	0	0	3459	17.2957	2799	13.9956

Table 1. Program data versus divisor ratio and frequency



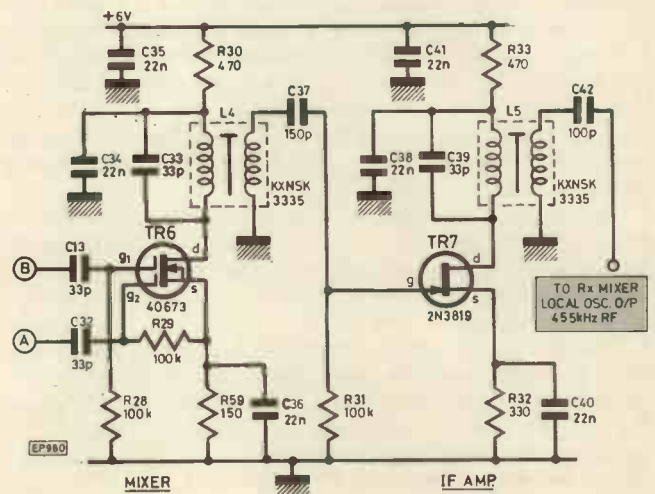


**Fig. 2a. 40 Channel CB Synthesiser circuit diagram. Diode D6 should be shown directly in the output from pin 20 of IC1 (anode towards pin 20, cathode towards R35/TR9). C20 may need to be 47pF**



**Fig. 2b. Tx x 2 multiplier (TR4) and r.f. amplifier (TR5)**

**Fig. 2c. Mixer (TR6) and i.f. amplifier (TR7)**



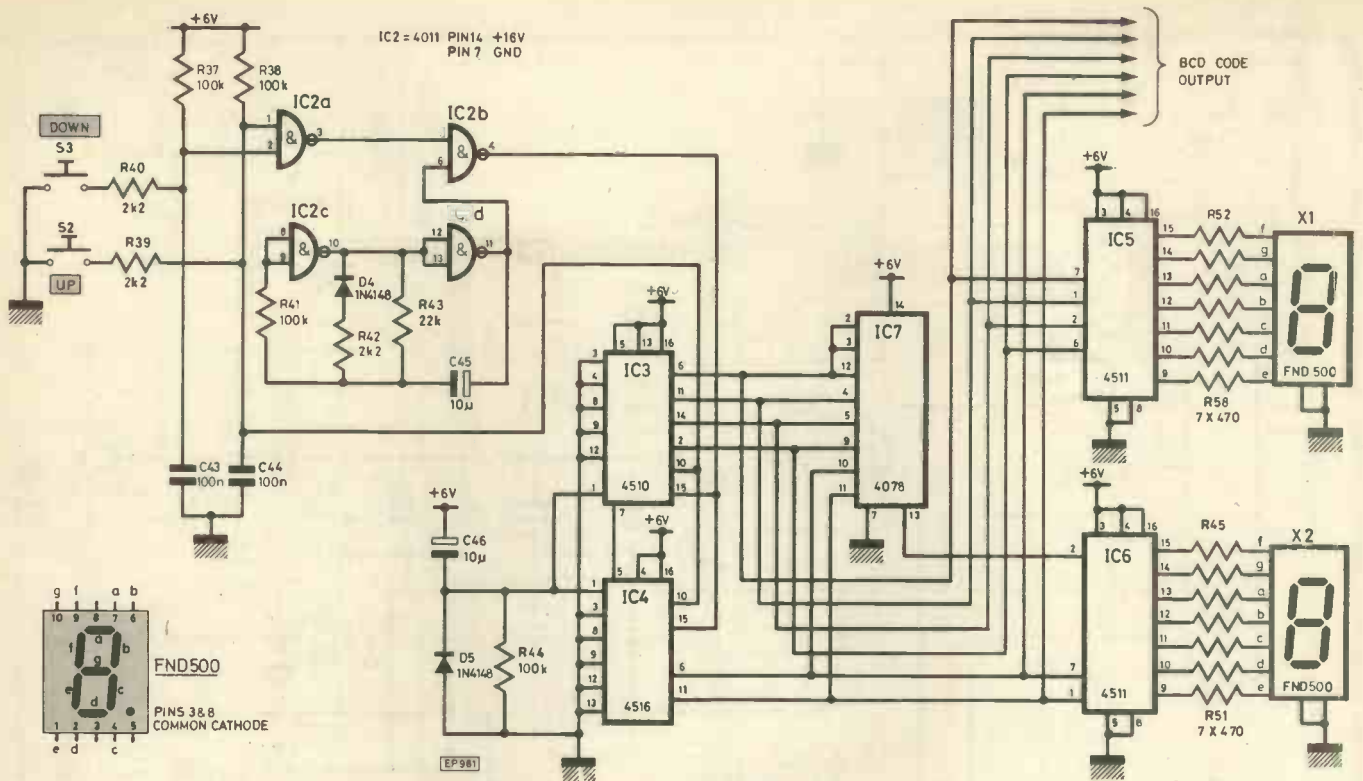


Fig. 2d. Display and BCD generator section. Pins 6 of IC3 and IC6 are connected to 0V

A loop filter follows this stage in order to smooth the phase detector output so that a d.c. voltage can be fed to the varicap diode. Thus, as the VCO frequency drifts slightly, the phase detector will sense this and will counteract this change by subsequently changing the bias on the varicap diode.

### OPERATION

The VCO comprises TR1 (see Fig. 2) which is biased in such a way as to oscillate at a frequency determined by the equivalent series load inductance and capacitance present between the base and emitter connections. This comprises C1, L1 and the series loading of C3 and C2 with D1 and D2. The frequency is changed by altering the bias on D2, the varicap diode. This semiconductor device exhibits the property of changing capacitance when the reverse bias voltage is altered. The varicap diode is chosen to have a high Q, low reverse leakage and linear characteristics. The series capacitors C2 and C3 alter the relative effects of the varicap on the oscillator frequency. The output of the VCO is fed from L1 via C6 to a buffer amplifier TR3, and then into the PLL i.c. The loop output of the i.c. is amplified and then fed via R1 to a final filter comprising R2 and C7. The d.c. bias is then fed to D2.

On TX the VCO changes from approximately 17MHz to 13.5MHz, half the final TX output frequency. To achieve optimum linearity and keep the VCO and PLL locked the VCO frequency is pulled down to this range by switching in VC1 and C8 by turning on TR2.

The modulation input, which only requires to deviate the VCO frequency by a few kHz, is fed via C10 and R9 to D1. Note the different value of series capacitance, C2 compared to that of C3, required to tune the VCO over the complete band. The buffered output of the VCO is fed via C13 or C21 to the RX mixer section and TX RF driver section. To prevent

any interference the TX circuitry is only powered up during transmit. TR8 and TR9 are used to switch the supply to the TX circuitry and change the logic on pin 20 of IC1, the RX/TX select. This input is TTL and CMOS compatible.

Transistor TR4 forms a frequency doubler circuit where the collector is tuned to 27MHz by L2 and C22. The output, rich in harmonics, is fed to a further amplifier stage consisting of TR5. The output of this stage is also tuned to 27MHz by L3 and C30.

TR6, a dual gate f.e.t., is employed in the receive circuitry to mix the VCO output with the 10.24MHz reference signal to produce the local oscillator output with a 455kHz IF offset. This section of the circuit may be omitted if an IF frequency of 10.695MHz is to be used. Again, as with the previous circuitry, the loads are tuned to remove as many harmonics and unwanted mixer products as possible. TR7 forms a buffer amplifier producing roughly 0.5V to 0.8V of RF signal.

The BCD channel coding is formed by two up-down counters, IC3, a BCD type and IC4 a binary type. The reason that IC4 is binary and not BCD coded is that as only the two LSBs of the counter are utilised no special reset lines are necessary to reset the counters from 39 to 00 on the up count and vice-versa on the down count. IC7 converts the BCD signal, 0000 0000 to 0100 0000 so that channel 40 is displayed corresponding to the BCD code 0000 0000. Refer to Table 1 for coding. The up-down select and clock pulses are produced by IC2, a quad two input NAND gate. Two gates form a pulse generator with a duty cycle determined by R42, R43 and D5. The other two gates form an enabling circuit which allows the pulses to clock the counters and select up or down. On power-up the counters are preset with the BCD number corresponding to channel 14. IC5 and IC6 decode the BCD signals and drive the 7-segment displays.



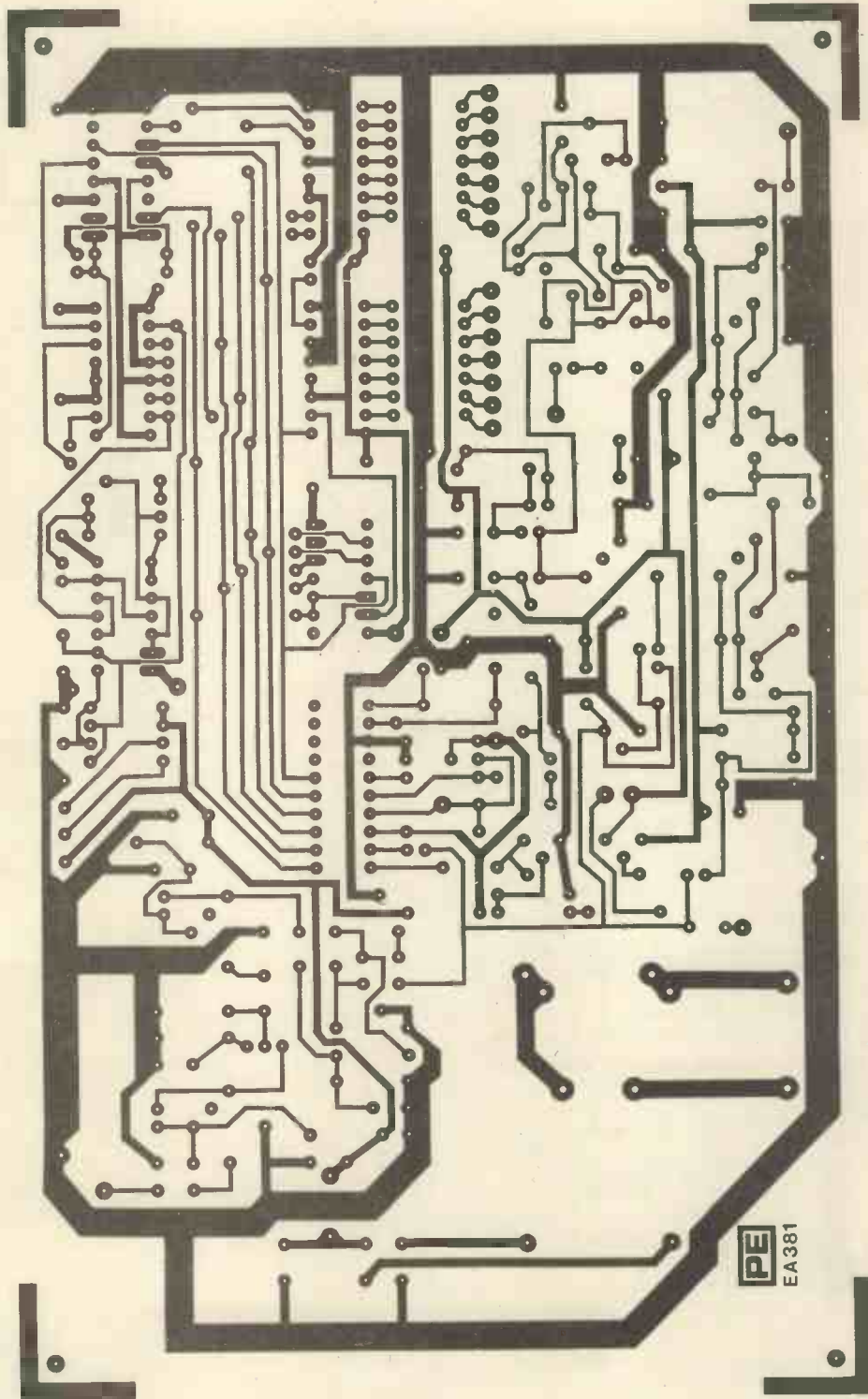


Fig. 3a. Printed circuit layout (actual size)

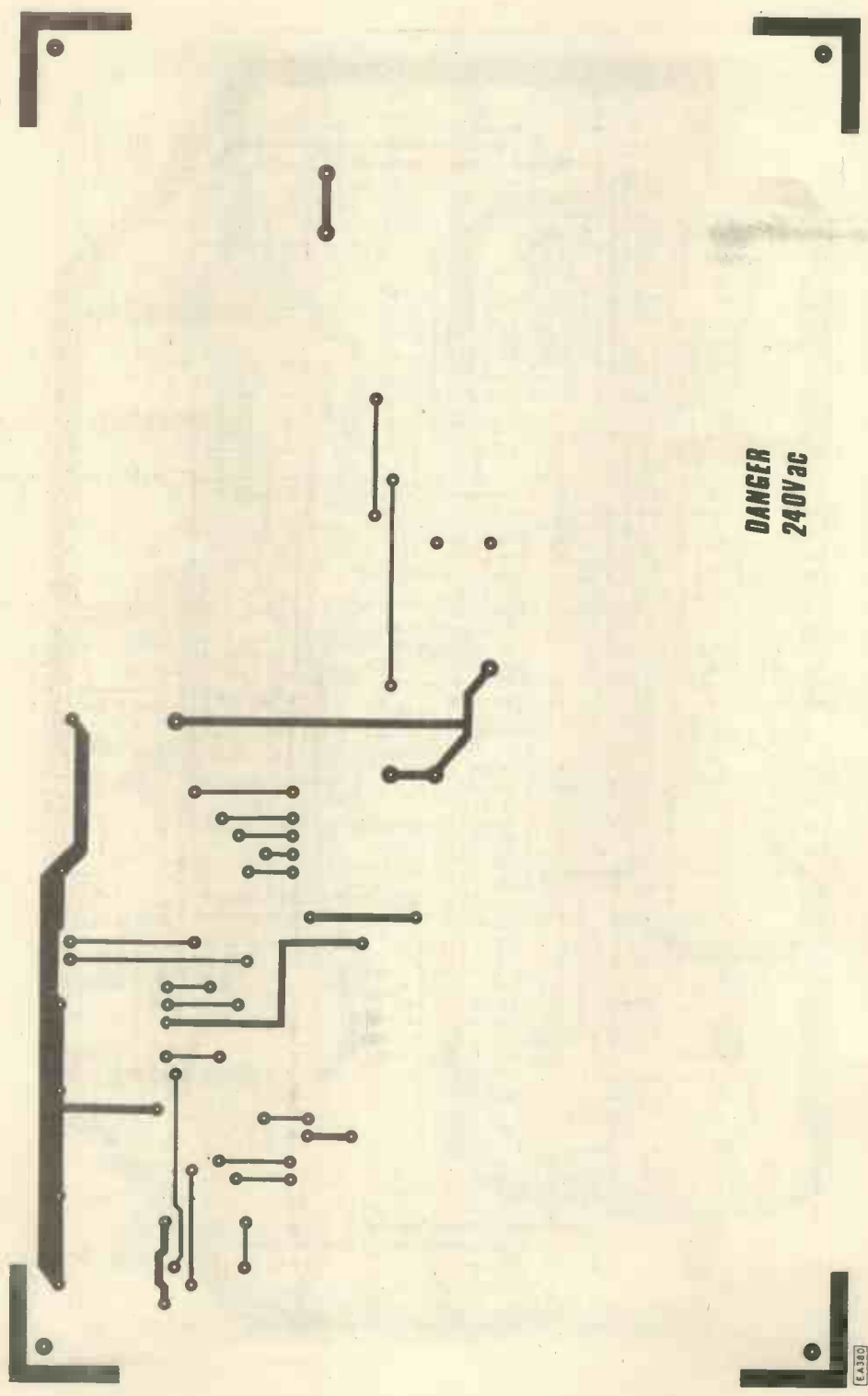


Fig. 3b. Printed circuit layout (actual size)



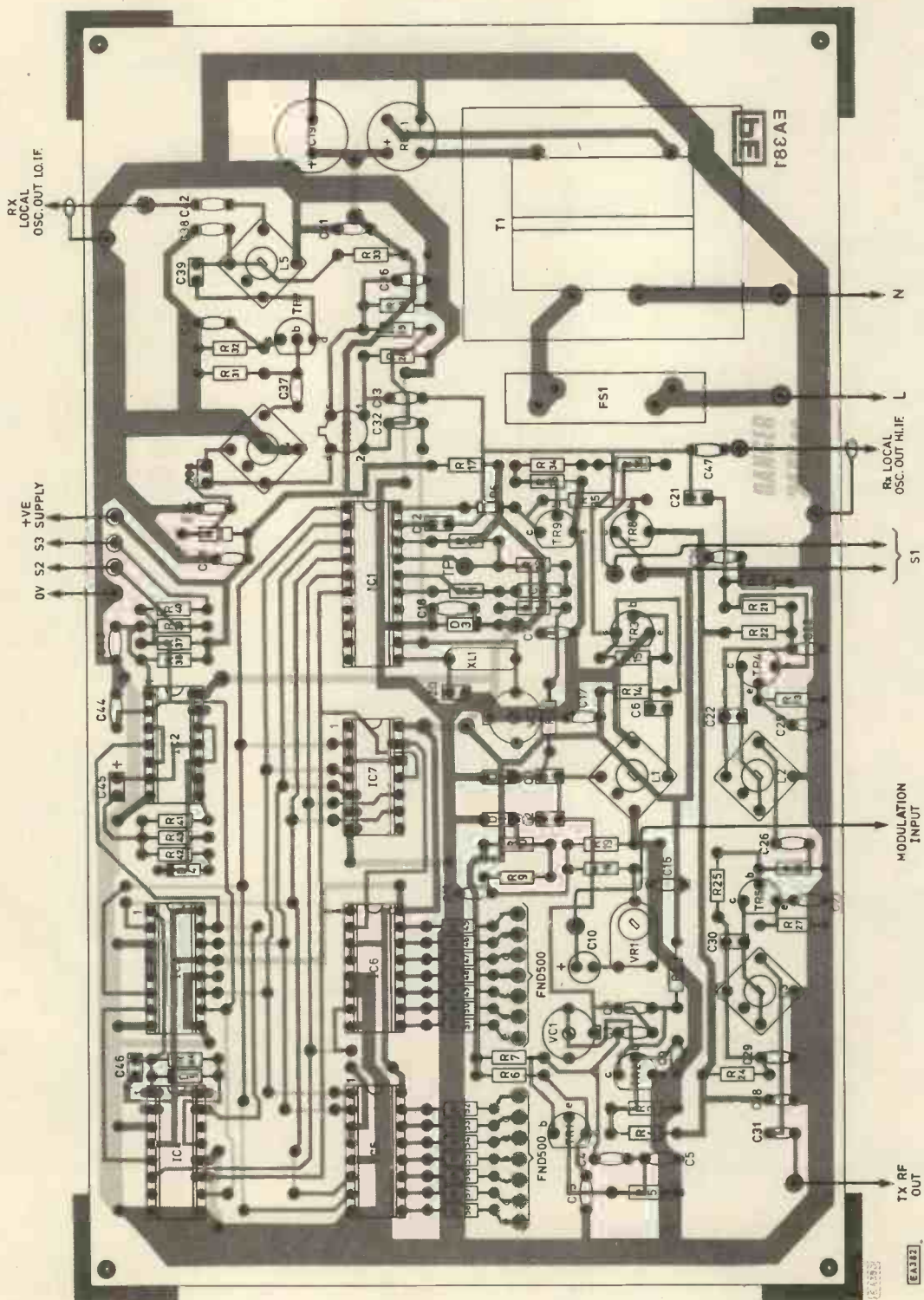


Fig. 4. Component layout

# COMPONENTS . . .

## Integrated Circuits

IC1	LC7137
IC2	4011
IC3	4510
IC4	4516
IC5,IC6	4511 (2 off)
IC7	4078

## Crystal

XL1	10.24MHz
-----	----------

## Variable Capacitors

VC1	2-20p
VC2	3-30p

## Potentiometers

VR1	10k
-----	-----

## Inductors

L1	KXNSK4612
L2-L5	KXNSK3335 (4 off)

## Transistors & Diodes

D1,D2	BB109 (2 off)
D3	6V2 400mW
REC1	W005
D4-D6	1N4148 (3 off)
TR1,TR3,TR4	BF274 (3 off)
TR2	BC237
TR5	BC548
TR6	40673
TR7	2N3819
TR8	BC307
TR9	BC237

## Resistors

R1,R4,R34,R35	4.7k (4 off)
R2,R43	22k (2 off)
R3,R9,R13	10k (3 off)
R5	2.7k
R6,R18,R22,R24,R30,R33	470 (6 off)
R7	220k
R8,R10,R20,R21,R25, R26,R28,R29,R31,R37, R38,R41,R44	100k (13 off)
R11,R14,R39,R40,R42	2.2k (5 off)
R12	47k
R15	150k
R16,R36	1k (2 off)
R17	68
R19	220
R23,R27,R32	330 (3 off)
R45-R58	470 (14 off)
R59	150

## Capacitors

C1,C8	22p (2 off)
C2	5.6p
C3,C47	56p (2 off)
C4	220p
C5,C37	150p (2 off)
C6,C12,C13,C20,C21,C22, C32,C33,C39	33p (9 off)
C7,C14	15n (2 off)
C9,C15-C18,C23-25, C27-29,C34-36,C38, C40,C41	22n (17 off)
C10	22µf
C11,C26,C31	1n (3 off)
C19	1000µf
C30	27p
C42	100p
C43,C44	100n (2 off)
C45,C46	10µf (2 off)

## Miscellaneous

T1	12V 3VA p.c.b. mounting transformer
S1	Toggle switch spst
S2	Push button switch
S3	Push button switch
LED display FND 500 (2 off)	X1, X2
P.c.b.	
Case	
Mains socket	
Mains lead	
Fuse 20mm 1A	
Fuse holders	
50 ohm coax	
BNC sockets (2 off)	

## Constructor's Note

LC7137 may be purchased from **Anglia Components Ltd**, Burdett Road, Wisbech, Cambs PE13 2PS (Tel 0945 63281) for the sum of £8.74 inc VAT and p/p.

T1, the case and the mains connector/lead may be purchased from **Modus Systems Ltd**, Park Drive, Baldock, Herts SG7 6EW (Tel 0462 894848) for the sum of £0.79, £1.99 and £1.35 respectively. VAT and 35p p/p should be added to each order.

## ADAPTION

The circuitry shown may be used in conjunction with several different types of equipment as discussed in the introduction. IF frequencies should be injected into the appropriate mixer section of the receiver. The higher 10.695 MHz IF frequency should always be used if possible to give the highest value of image rejection. Note that any existing inputs to the receiver's mixer should be inhibited or spurious outputs will cause serious interference.

On TX the input waveform should preferably be from a speech processor, i.e. amplitude and band limited to prevent over modulation and non-linearity distortion. The TX output should be connected to the pre-amplifier stage of the transmitter, which should be tunable to 27MHz.

The circuitry may also be connected to the *PE Ranger*. The modulating input should be connected to test point j, the output of the speech processor. To facilitate 40 channels,



one of the 6 channel selections in the Ranger must be inhibited, i.e. the TX and RX crystals shorted or switched out of circuit to prevent interference. The two RF connections to the synthesiser board from TR3 (base) and IC101 (pin 1) should be via 50 ohm screened coax. terminated with BNC or other suitable miniature RF connectors at the cases. The TX/RX sense is connected to test point h.

### TESTING AND ALIGNMENT

The unit is fairly simple to align. After it has been constructed and fully checked it should be powered up with a 9V to 12V supply. The channel display should indicate channel 14. If not, the load inputs to IC3 and IC4 (pins 3, 4, 12, 13) and the preset enable lines (pins 1) should be checked. On depressing the up or down switch the display should toggle at a reasonable rate. If not check IC2 and associated components. Assuming this is all correct check with the aid of an oscilloscope that the VCO and reference oscillators are working (TR3 collector and IC1 pin 12). With S1 in the off position, i.e. RX selected, measure the d.c. voltage at TP1 and adjust the core of L1 to produce a range of approximately 2V to 3V from channel 1 to 40. If the voltage at TP1 is either high or low continuously then check the BCD code input to IC1 and the associated components of IC1 and the VCO. Switch S1 on, i.e. TX selected, and adjust VC1 to produce the same voltage range at TP1 from channel 1 to 40. Repeat the alignment again and re-adjust L1 if necessary. With S1 off tune L4 and L5 for maximum local oscillator output. Re-tune when connected to a receiver for maximum receiver sensitivity. With S1 selected and a 50 ohm dummy load on the output socket

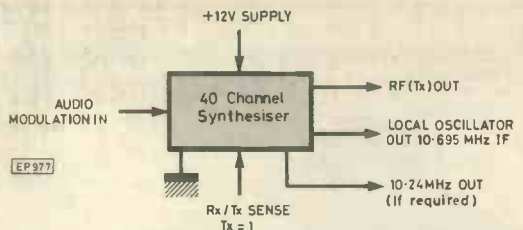


Fig. 5. Connection to a communications receiver/transceiver

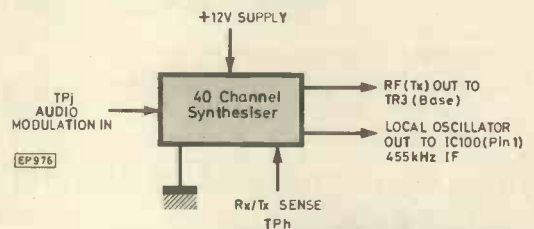
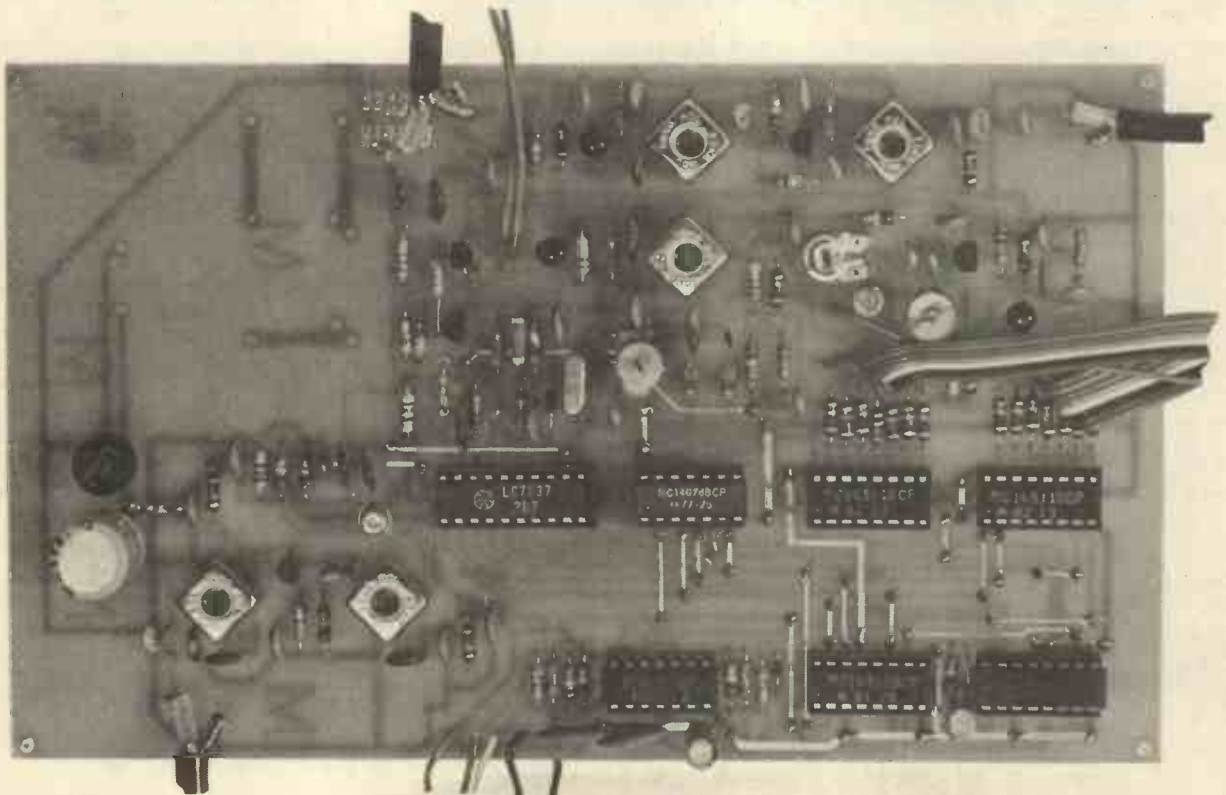


Fig. 6. Connection to a PE Ranger

tune L2 and L3 for maximum RF output, with least visible harmonic content. With a frequency counter connected to the Tx RF output, and with Tx selected, adjust VC2 to give the correct channel frequency (as shown in Table 1) to five places over the whole range. VR1 should now be adjusted to give adequate audio modulation. This is best checked with the use of a FM CB monitor or CB rig. Remember that over-modulation ( $< \pm 2.5\text{kHz}$ ) will not only cause distortion on some FM receivers and/or cross channel interference, but is a contravention of the Home Office regulations. ★

Due to the nature of this circuitry, the author cannot accept any responsibility whatsoever for the specifications of any system that may be used in conjunction with the described article.



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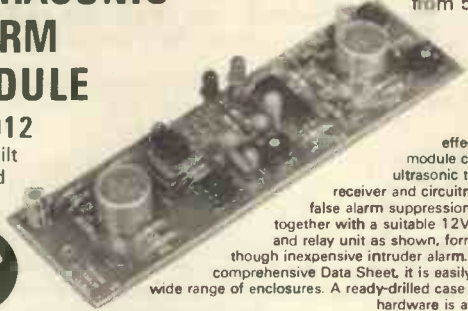
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# SEMICONDUCTOR UPDATE

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FEATURING IMS26000 X2816A X2804A S3610 S3620

## INMOS WINNER

Inmos, the world-class semiconductor memory manufacturer set up and largely funded by the British Government, is continuing to expand its share of the memory market by introducing new devices which are, quite simply, *better* than those produced by either the American or the Japanese competition. This is a deliberate policy designed to allow Inmos to join the memory race as a market leader without the need to make vast quantities of the common-or-garden memory components already supplied by all the longer established manufacturers such as Texas, Motorola, Intel, N.E.C. and others. One day Inmos expect to compete directly in those markets too, and already they have a new production facility in South Wales to add to their design centre in Bristol and their first production unit in Colorado, but for the moment Inmos are concentrating on the premium memory market where profits are higher and quantities lower. After success with their high speed 16K static parts, Inmos have now released their long awaited 64K dynamic, and it does seem to have been worth the wait! Their brand new IMS26000, organised as 64Kx1-bit, is the fastest dynamic RAM available anywhere, and it offers features which show it to be a second generation approach to the 64K DRAM design problem.

Most important in the long run may be the CAS before RAS refresh feature which has the effect of releasing a package pin so that upwards compatibility with the next generation 256K devices is possible. To get a 64K memory into a 16 pin package the 16-bit address is multiplexed as two 8-bit bytes strobed by the Row Address Strobe RAS, and the Column Address Strobe CAS. Normally CAS follows RAS and these signals are produced by an external dynamic RAM controller chip which also has the job of issuing a sequence of refresh cycles which interleave with normal memory cycles to prevent the capacitor storage cells from "forgetting." The refresh addresses are generated by an on-chip counter activated via pin 1 which unfortunately will be needed for A8 in the 256K chip when it appears. To keep pin 1 spare, Inmos detect the use of CAS before RAS to signify a refresh cycle, since this sequence is not used during a normal read or write access. The result is that circuit boards can be laid out now for 64K chips with a drop-in upgrade to 256K possible later.

Another IMS26000 innovation is "nibble mode" which allows the already fast 100 nanosecond access time of the chip to be reduced to only 55 nanoseconds for sequential four bit "nibbles". This feature is made possible by the internal memory

organisation which actually gains access to four bits at a time even though only one of the four available is selected for output. With the IMS26000 a sequence of four CAS pulses will allow all four bits to be shifted out at high speed if required.

## ROM THAT THINKS IT'S A RAM

After the EPROM, which had to be erased with U.V. light, came the EEPROM which can be erased and reprogrammed electrically by the application of high voltage pulses. EPROMs are still cheaper than EEPROMS; also, having to have high voltages and programming components on the circuit board can be a nuisance, and so the apparently more convenient EEPROM devices are nowhere near as popular as their EPROM predecessors. If, as is likely, the cost advantage of the EPROM is maintained in the future, the EEPROM will never replace it for normal program memory use and will be restricted only to those applications where the rewriting of non-volatile memory data is an especially desirable feature in itself.

Even if the price advantage of EPROMs cannot be removed, it is at least possible to overcome the *technical* disadvantages of the EEPROM technology as Xicor have demonstrated with a pair of new devices coded X2816A and X2804A. The great advantage of these two devices is that they do not require either the high voltages or the special programming circuitry needed by previous EEPROMs, and this makes them especially easy to use. In fact, these new chips appear to the rest of the system like RAM chips, and are actually pin compatible with byte-wide RAMs such as the Mostek 4802, with the main difference being that you can remove the power supply from the EEPROM without disturbing the stored data!

The X2816A and the X2804A can be read just like RAM chips, in 300 nanoseconds. Writing new data takes much longer at 10 milliseconds, but the "spanner" which this might otherwise throw into the works of RAM compatibility is avoided by having address and data latches within the package. The system carries out a normal (fast) write cycle, but this is stretched internally by the EEPROMs to provide the required 10 milliseconds. The only restriction placed on the system is that the software should not try to program another location until at least 10 milliseconds has elapsed, although during the pause other system activities can take place if required.

Now if you lay out your microprocessor board to take 24 or 28 pin memory sockets

it is possible to decide later whether you plug in a static RAM (for short term data storage), an EPROM (to contain the program) or an EEPROM (to store long term but alterable data). All three options will work from a single 5 volt supply and will not require special programming or refresh circuitry.

The Xicor X2816A has a 2Kx8 format and the X2804A provides 512x8.

## NATURAL VOICE

According to information theory, you need to take at least two samples during the period of the highest frequency when attempting to encode analogue signals digitally. For speech, this means a sampling rate of about 8kHz, so if we assume 8 bits per sample to give a reasonable quality we can predict the need for a 64K bit ROM to store just *one second* of speech.

ROM devices are getting cheaper all the time of course, but they will have to get a good deal cheaper *and* bigger to make simple sampling a viable method of digital speech encoding. Fortunately, ways have been found to encode speech with fewer bits by the elimination of the redundant information which speech signals contain. By this means, the size of the store required can be reduced by a factor of about one hundred. Linear Predictive Coding (LPC) is one such encoding technique which was championed by Texas Instruments and used, for example, in their "Speak and Spell" learning aid. If you have used the "Speak and Spell" you will be rightly impressed by the great benefits that digitised speech can bring, but you may also be less than happy about the clarity of the speech.

A new device from AMI Microsystems which uses a modified LPC technique, is claimed to provide a higher quality speech signal than has hitherto been possible with ordinary LPC. The manufacturers call their new speech technique "Natural Voice" and are currently making it available on two chips, the S3610 which has an internal 20K ROM for 17 seconds of speech, and the S3620 which can use an external 128K ROM (the S3630) to give up to 110 seconds. Apart from the promised advantages of the "Natural Voice" technique which I haven't been able to sample yet, the thing which appeals to me is AMI's "one-chip" approach to speech synthesis. The S3610 for example has an internal 30 milliwatt audio amplifier and needs only two capacitors and a cheap crystal to add speech to any instrument or toy. No doubt these chips will soon be available with a standard vocabulary so that we can all have a go. The chips are made in CMOS, run from a single 5 to 8 volt supply, and have a great ability to say for themselves!

# SEMI-PROFESSIONAL MIXING DESK

## Part Two

### Tim Orr



**T**HE p.c.b. designs for the input, output and auxiliary channels are shown in Figs. 1, 2 and 3 respectively with their component layouts shown in Figs. 4, 5 and 6. Note that the p.c.b.s are shown in two sections and should be joined along the X-X axis making sure that the tracks are aligned properly. Each p.c.b. should be assembled by first fitting the wire licks then the resistors, i.e. sockets, semiconductors and capacitors.

Take care that the jack sockets and potentiometers fit flush with the p.c.b. as these parts have to mate up with the metal work. The push switches can now be inserted but they should not be soldered. After the module panel has been fitted to the p.c.b. and the potentiometer retaining nuts tightened the push switches should be adjusted so that they do not interfere with the metal work. When the switches have been adjusted they can be soldered into position.

The slider switches should be mounted last on the input and output channels along with the mounting socket SK1. On the auxiliary channel the microphone and pre-fade listen jack socket wires should be twisted before being soldered to the p.c.b. Tinned copper wire can be used for wiring the talk back switch.

After all the channel boards have been soldered carefully check each one for any solder splashes or incorrectly placed components.

The p.c.b. design for the bus board is shown in Fig. 7, the thick tracks are for power supplies and the thin tracks for signals. The number of bus boards required depends upon the number of channels incorporated into the mixer, one bus board is required for every six channels used. Ten way pin blocks are used to connect the power supplies and signals to and from the bus board to each channel. After the pin blocks have been soldered onto the board (Fig. 8) trim off the excess pin lengths on the underside. The bus board can now be fitted into the case using spacers to prevent the pins being shorted to the chassis.

Make certain that the 4 signal tracks are facing the front of the mixer. If more than one bus board is used they should be joined together using 24s.w.g. tinned copper wire covered with rubber sleeving. The mains supply lead should be connected to the bus board as shown in Fig. 9.

#### TESTING

The input channels are relatively simple circuits; only 4 op amps are used to perform the amplification and tone control functions. Inject a 1Vpp sinewave into the line input, select LINE operation. The output signal seen at the SEND jack can

be varied from 0.3Vpp to 18Vpp (with FLAT selected) by rotating the GAIN control pot. Now select the MIC mode and inject a 10mVpp signal into the MIC jack. The signal seen on the send jack should be variable over a range of 63mV to 6.3Vpp. In all cases the output signal should be free from distortion and clipping. Note that the LEVEL DETECTOR l.e.d. should come on and stay on when the SEND level exceeds +4dBm (3.5Vpp). The noise performance of the input amplifier can be measured, but only if you have the use of the equipment shown in Fig. 10. The procedure is as follows. Remove all inputs and select MIC operation and maximum gain. Also select FLAT operation and measure the noise voltage at the SEND jack. The theoretical input noise is 1.46 $\mu$ V r.m.s. which when multiplied by the MIC gain of 56dB results in an output noise voltage of 0.9mV r.m.s. If the input noise is significantly bigger than this then check that the gain is actually 56dB. Wrong resistor values may give you a high preamplifier gain, and hence more apparent noise. Also IC1 may be more noisy than other devices. It is not uncommon to select the input op amp for low noise operation. If noise is a problem then check for dry joints or other microphonic faults. When using the MIC input at full gain you will hear the preamplifier noise, this is not a fault. The important parameter in all audio equipment is the signal to noise ratio and not the absolute noise level. If the microphone input signal level is 1.46mV r.m.s. then the signal to noise ratio will be 60dB, which is not very much worse than most semi-professional tape recorders. A microphone signal level of 1.46mV r.m.s. is quite a small signal level. In cases like this the best advice is to move the microphone nearer to the object being recorded!

#### TONE CONTROLS

The tone controls can be tested either with test equipment or by listening to pre-recorded music through them. Inject a sinewave source into the LINE input, set S2 to EQ and monitor the signal at the SEND jack. The frequency response can be plotted out by varying the sinewave frequency and recording the gain changes. These responses should conform to those shown in Fig. 2 last month. However, no one would want laboriously to plot the frequency responses of 18 tone control units using this method! The best method for determining a circuit's frequency response is to inject a swept sinewave and to monitor the output waveform on an oscilloscope. However, if you do not have access to this equipment, then a listening test is quite adequate. Note that the TONE CONTROL section actually provides gain and so it is possible to amplify the system noise. If any of the controls



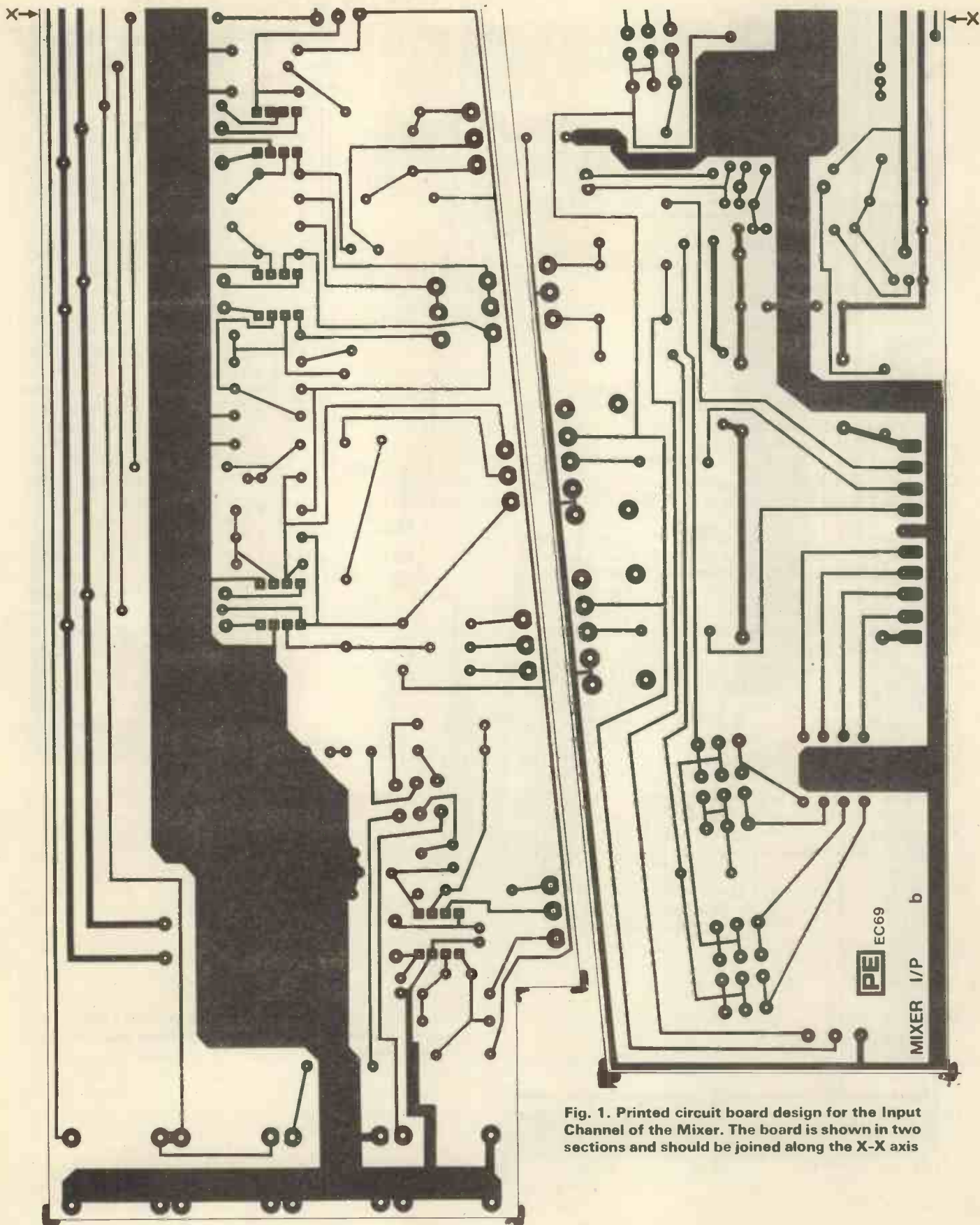


Fig. 1. Printed circuit board design for the Input Channel of the Mixer. The board is shown in two sections and should be joined along the X-X axis

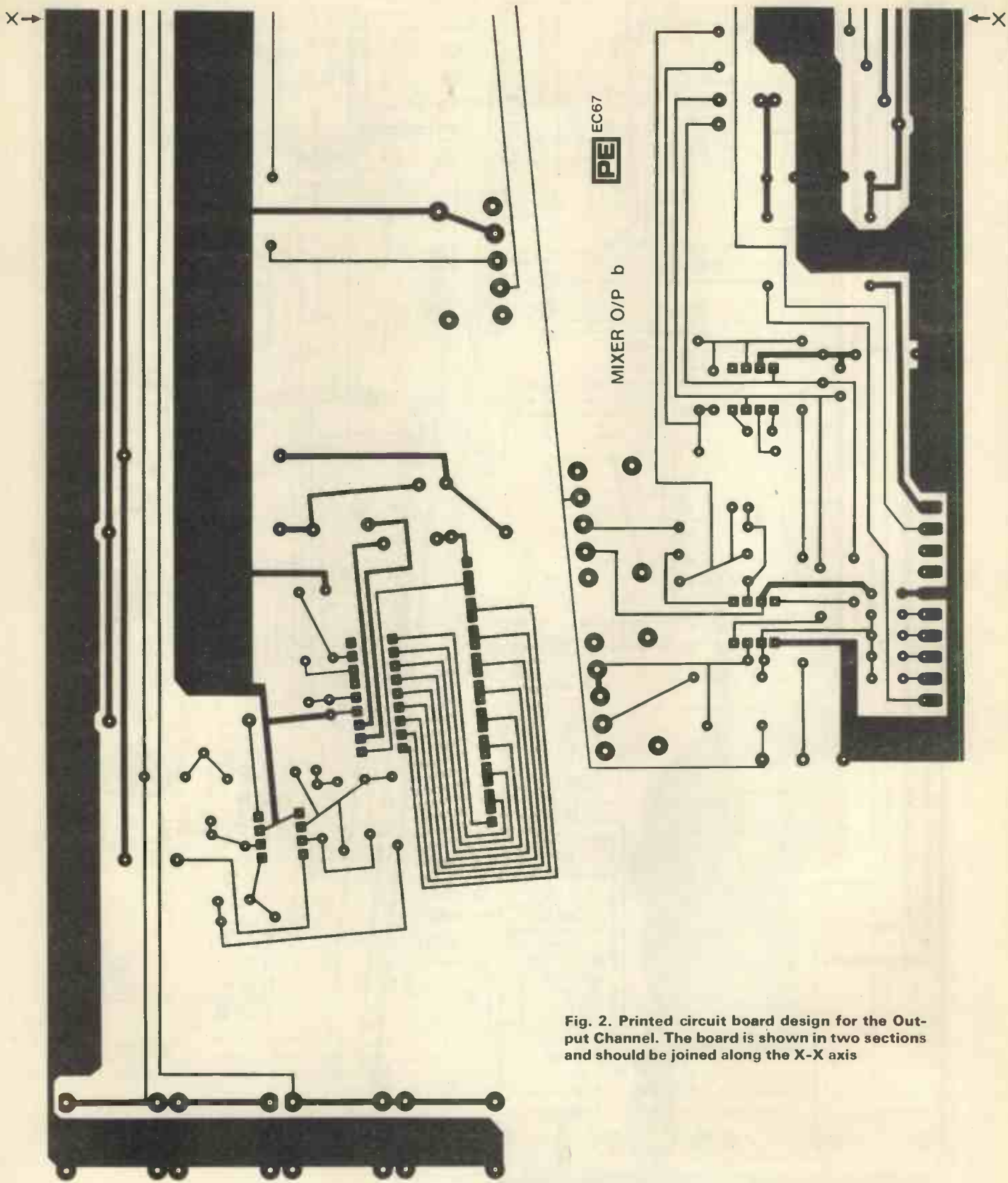


Fig. 2. Printed circuit board design for the Output Channel. The board is shown in two sections and should be joined along the X-X axis



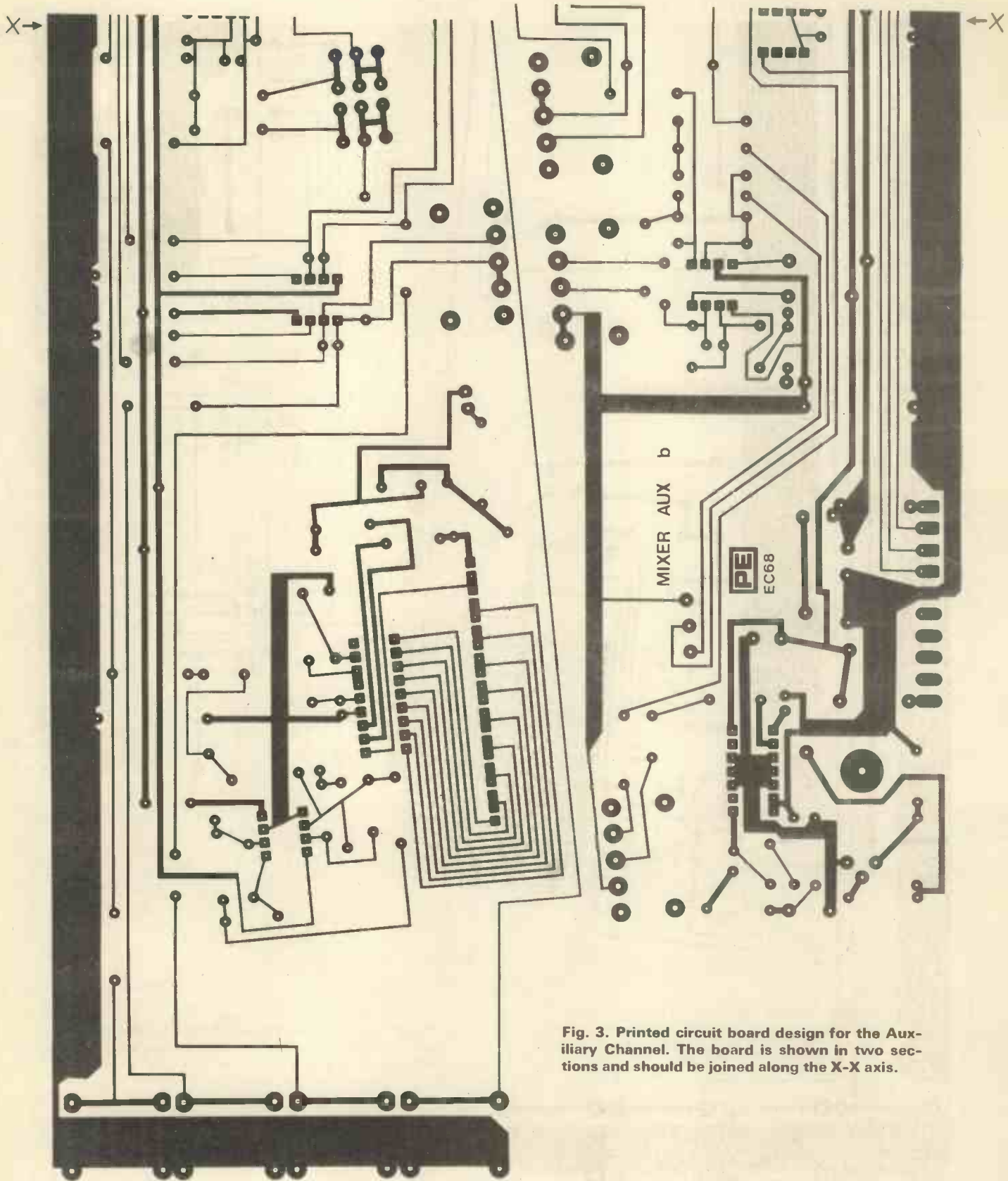


Fig. 3. Printed circuit board design for the Auxiliary Channel. The board is shown in two sections and should be joined along the X-X axis.

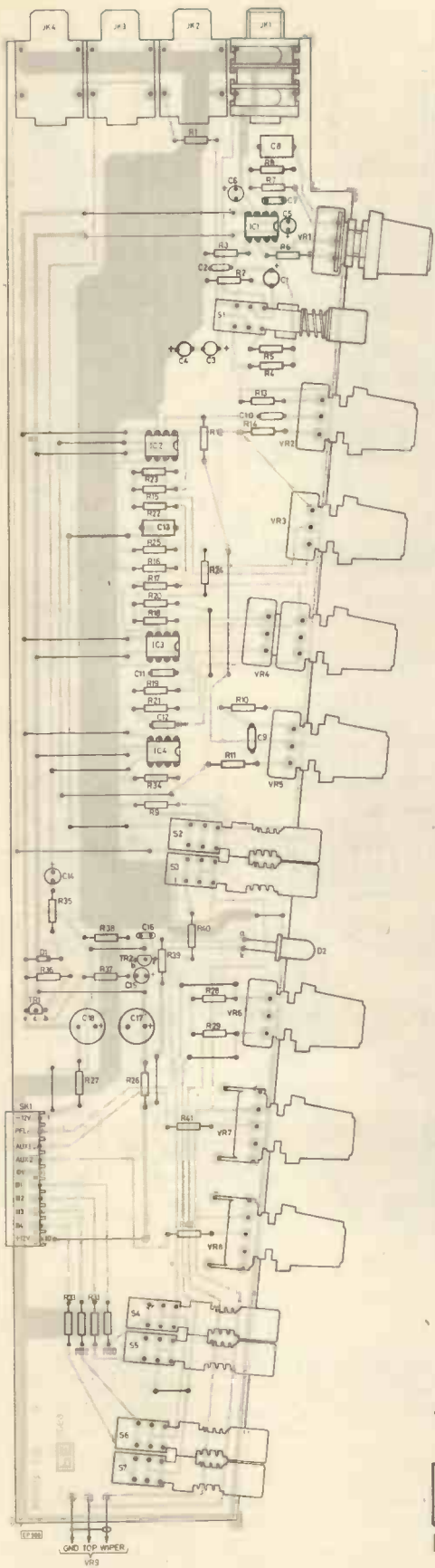


Fig. 4. Component layout for the Input Channel

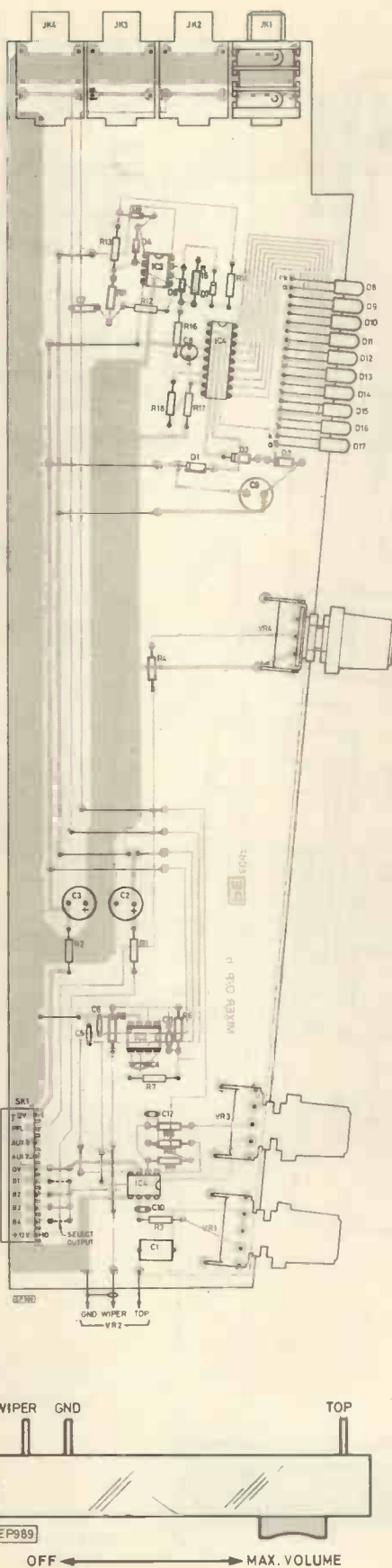


Fig. 5. Component layout for the Output Channel

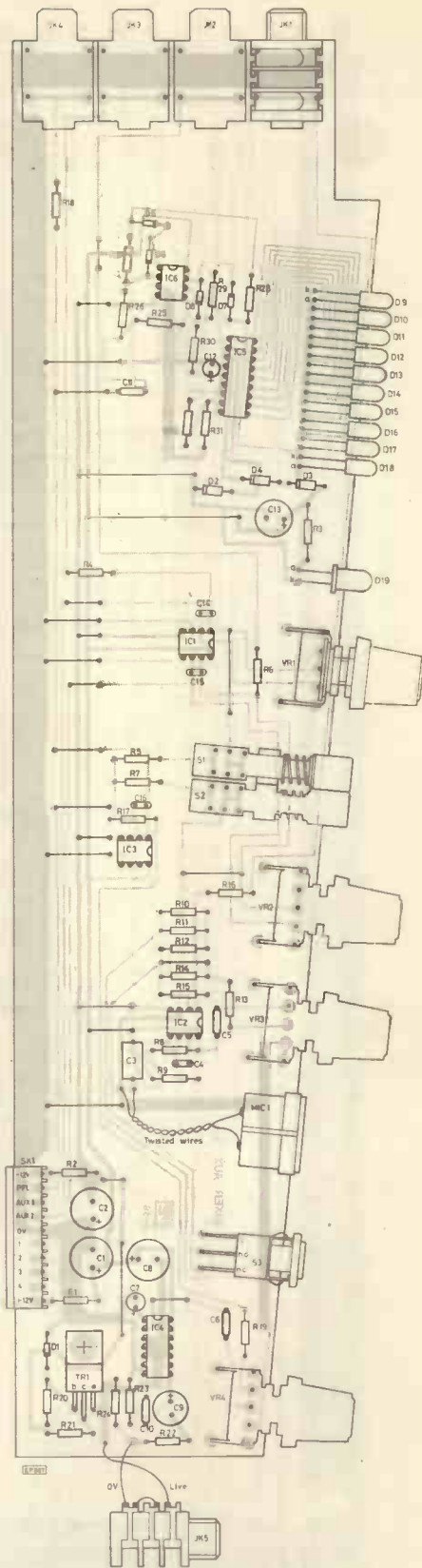
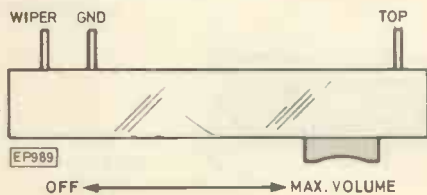


Fig. 6. Component layout for the Auxiliary Channel



OFF ← → MAX. VOLUME



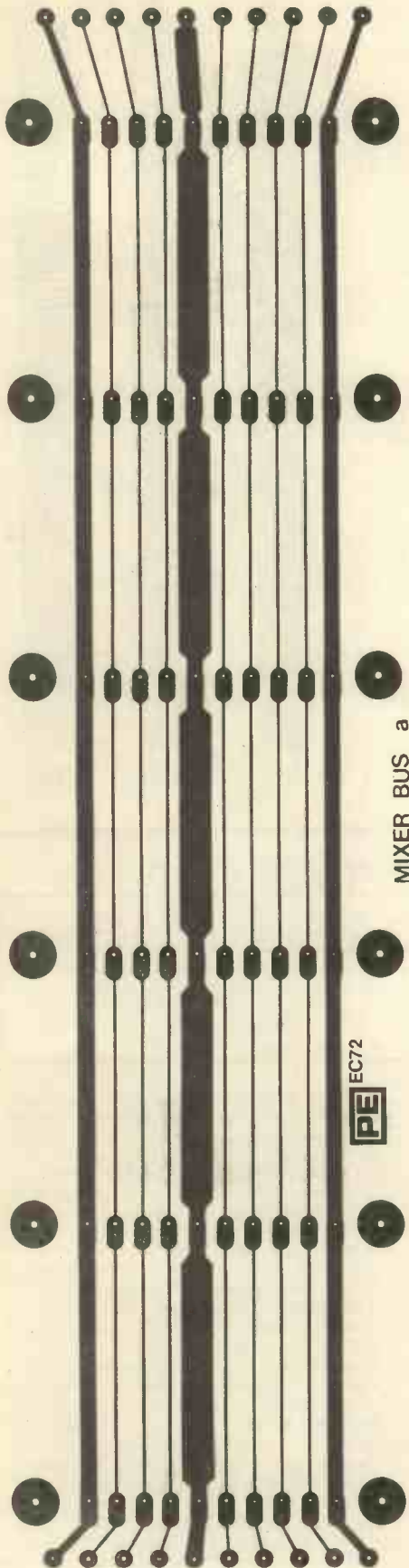


Fig. 7. Bus bar p.c.b. design

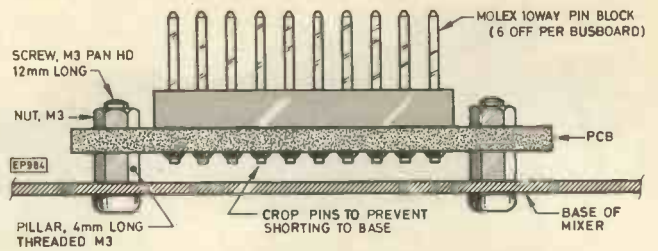


Fig. 8. Mounting details for the bus blocks

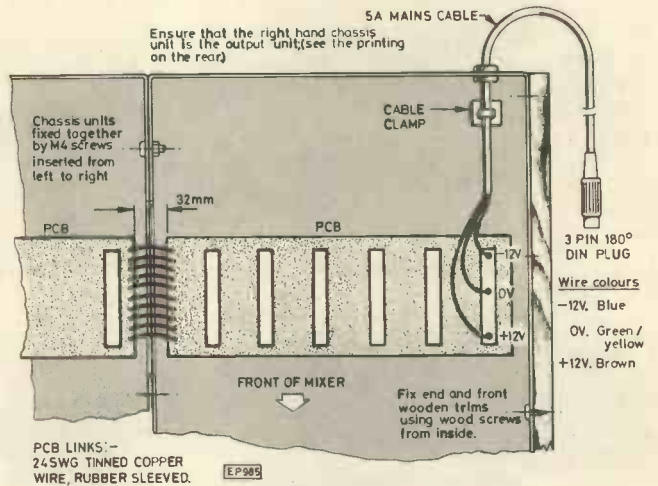
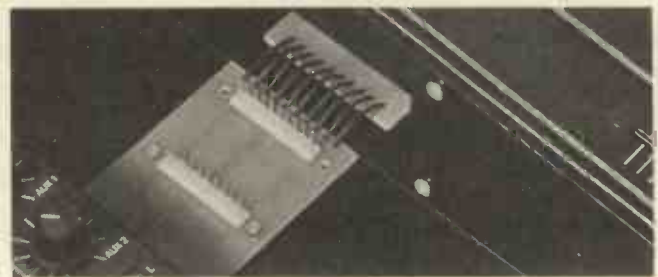


Fig. 9. Wiring and layout for the Bus boards



Bus board link wiring

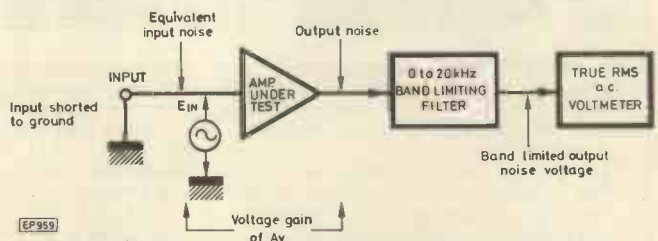
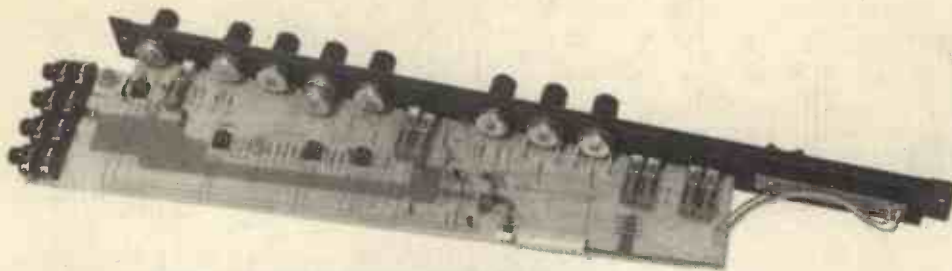


Fig. 10. Arrangement for measuring the equivalent input noise

operate at the wrong frequency or produce a wrong gain change then check the circuit for correct component values. All the pots and switches in the input channel should be almost noiseless and clickless when operated. If this is not the case then check the circuit for correct components or mechanically faulty pots.

The input channels consume about 15mA from each rail rising to nearly 30mA when the LEVEL i.e.d. comes on. All the op amps should have very little d.c. offset on their outputs. Typically the offset will be  $\pm 10\text{mV}$ . Larger offsets may well cause crackle when control pots are rotated. The two integrators in the MIDDLE tone control may have larger offsets but this will not degrade the performance.



Input Channel with the front panel layout shown in (a)

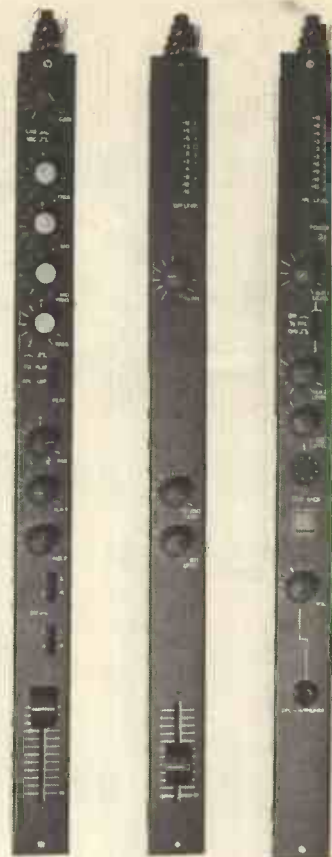


Output Channel with the front panel layout shown in (b)



Auxiliary Channel with the front panel layout shown in (c)

NEXT MONTH: P.S.U. construction and using the Mixing Desk.



(a)

(b)

(c)

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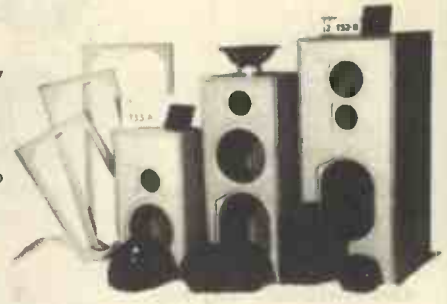
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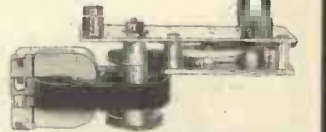
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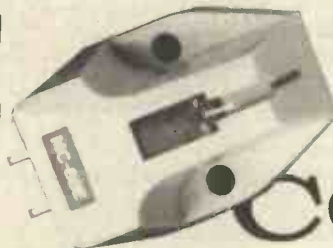
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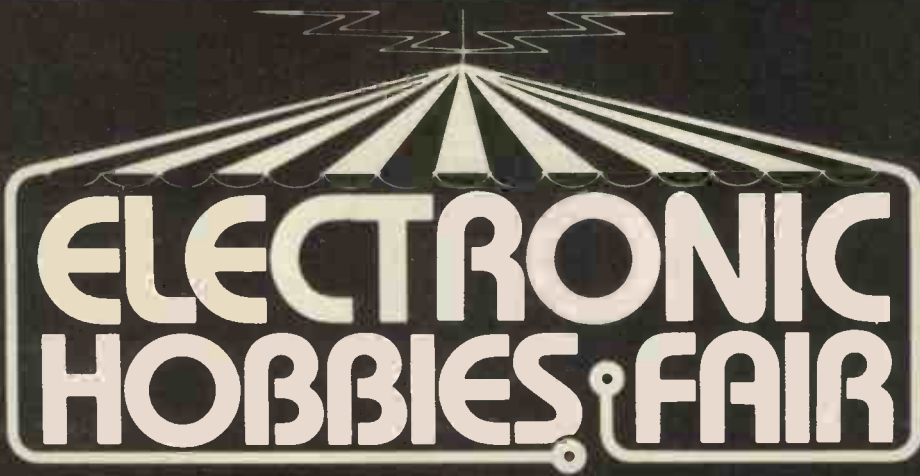
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7403	11p	74368A	30p	74LS374	55p	4011	11p	AY1-1313	668p	MC6847	£65p	AM25S2521	£32p	1.0MHz	290p
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7409	14p	74390	90p	74LS381	70p	4017	32p	AY3-8912	625p	MC6847	£65p	DS8830	225p	2.5MHz	250p
7410	14p	74390	90p	74LS382	70p	4018	32p	AY5-4007D	520p	MC6847	£65p	DS8831	140p	2.67MHz	150p
7411	18p	74390	90p	74LS383	70p	4019	32p	CA3028A	120p	MC6847	£65p	DS8832	250p	3.5795MHz	100p
7412	14p	74390	90p	74LS384	70p	4020	32p	CA3039E	200p	MC6847	£65p	DS8833	225p	3.686MHz	300p
7413	16p	74390	90p	74LS385	70p	4021	32p	CA3041	80p	MC6847	£65p	DS8834	150p	4.00MHz	150p
7414	18p	74390	90p	74LS386	70p	4022	32p	CA3042	80p	MC6847	£65p	DS8835	225p	4.194MHz	150p
7415	18p	74390	90p	74LS387	70p	4023	32p	CA3043	80p	MC6847	£65p	DS8836	225p	4.33MHz	110p
7416	18p	74390	90p	74LS388	70p	4024	32p	CA3044	80p	MC6847	£65p	DS8837	225p	4.608MHz	250p
7417	18p	74390	90p	74LS389	70p	4025	32p	CA3045	80p	MC6847	£65p	DS8838	225p	4.9152MHz	250p
7418	18p	74390	90p	74LS390	70p	4026	32p	CA3046	80p	MC6847	£65p	DS8839	225p	5.00MHz	175p
7419	18p	74390	90p	74LS391	70p	4027	32p	CA3047	80p	MC6847	£65p	DS8840	225p	6.00MHz	150p
7420	14p	74390	90p	74LS392	70p	4028	32p	CA3048	80p	MC6847	£65p	DS8841	225p	6.00MHz	150p
7421	18p	74390	90p	74LS393	70p	4029	32p	CA3049	80p	MC6847	£65p	DS8842	225p	6.00MHz	150p
7422	20p	74390	90p	74LS394	70p	4030	32p	CA3050	285p	MC6847	£65p	DS8843	225p	6.00MHz	150p
7423	18p	74390	90p	74LS395	70p	4031	32p	CA3051	285p	MC6847	£65p	DS8844	225p	6.00MHz	150p
7424	18p	74390	90p	74LS396	70p	4032	32p	CA3052	285p	MC6847	£65p	DS8845	225p	6.00MHz	150p
7425	18p	74390	90p	74LS397	70p	4033	125p	CA3053	285p	MC6847	£65p	DS8846	225p	6.00MHz	150p
7426	26p	74390	90p	74LS398	70p	4034	125p	CA3054	285p	MC6847	£65p	DS8847	225p	6.00MHz	150p
7427	26p	74390	90p	74LS399	70p	4035	125p	CA3055	285p	MC6847	£65p	DS8848	225p	6.00MHz	150p
7428	26p	74390	90p	74LS400	70p	4036	125p	CA3056	285p	MC6847	£65p	DS8849	225p	6.00MHz	150p
7429	26p	74390	90p	74LS401	70p	4037	125p	CA3057	285p	MC6847	£65p	DS8850	225p	6.00MHz	150p
7430	26p	74390	90p	74LS402	70p	4038	125p	CA3058	285p	MC6847	£65p	DS8851	225p	6.00MHz	150p
7431	26p	74390	90p	74LS403	70p	4039	125p	CA3059	285p	MC6847	£65p	DS8852	225p	6.00MHz	150p
7432	26p	74390	90p	74LS404	70p	4040	125p	CA3060	285p	MC6847	£65p	DS8853	225p	6.00MHz	150p
7433	22p	74390	90p	74LS405	70p	4041	40p	CA3061	285p	MC6847	£65p	DS8854	225p	6.00MHz	150p
7434	22p	74390	90p	74LS406	70p	4042	40p	CA3062	285p	MC6847	£65p	DS8855	225p	6.00MHz	150p
7435	22p	74390	90p	74LS407	70p	4043	40p	CA3063	285p	MC6847	£65p	DS8856	225p	6.00MHz	150p
7436	22p	74390	90p	74LS408	70p	4044	40p	CA3064	285p	MC6847	£65p	DS8857	225p	6.00MHz	150p
7437	22p	74390	90p	74LS409	70p	4045	40p	CA3065	285p	MC6847	£65p	DS8858	225p	6.00MHz	150p
7438	22p	74390	90p	74LS410	70p	4046	40p	CA3066	285p	MC6847	£65p	DS8859	225p	6.00MHz	150p
7439	22p	74390	90p	74LS411	70p	4047	40p	CA3067	285p	MC6847	£65p	DS8860	225p	6.00MHz	150p
7440	14p	74390	90p	74LS412	70p	4048	40p	CA3068	285p	MC6847	£65p	DS8861	225p	6.00MHz	150p
7441	55p	74390	90p	74LS413	70p	4049	40p	CA3069	285p	MC6847	£65p	DS8862	225p	6.00MHz	150p
7442A	30p	74390	90p	74LS414	70p	4050	40p	CA3070	285p	MC6847	£65p	DS8863	225p	6.00MHz	150p
7443A	30p	74390	90p	74LS415	70p	4051	40p	CA3071	285p	MC6847	£65p	DS8864	225p	6.00MHz	150p
7444A	30p	74390	90p	74LS416	70p	4052	40p	CA3072	285p	MC6847	£65p	DS8865	225p	6.00MHz	150p
7445A	30p	74390	90p	74LS417	70p	4053	40p	CA3073	285p	MC6847	£65p	DS8866	225p	6.00MHz	150p
7446A	30p	74390	90p	74LS418	70p	4054	40p	CA3074	285p	MC6847	£65p	DS8867	225p	6.00MHz	150p
7447A	30p	74390	90p	74LS419	70p	4055	40p	CA3075	285p	MC6847	£65p	DS8868	225p	6.00MHz	150p
7448	45p	74390	90p	74LS420	70p	4056	40p	CA3076	285p	MC6847	£65p	DS8869	225p	6.00MHz	150p
7449	45p	74390	90p	74LS421	70p	4057	40p	CA3077	285p	MC6847	£65p	DS8870	225p	6.00MHz	150p
7450	15p	74390	90p	74LS422	70p	4058	40p	CA3078	285p	MC6847	£65p	DS8871	225p	6.00MHz	150p
7451	15p	74390	90p	74LS423	70p	4059	40p	CA3079	285p	MC6847	£65p	DS8872	225p	6.00MHz	150p
7452	15p	74390	90p	74LS424	70p	4060	40p	CA3080	285p	MC6847	£65p	DS8873	225p	6.00MHz	150p
7453	15p	74390	90p	74LS425	70p	4061	40p	CA3081	285p	MC6847	£65p	DS8874	225p	6.00MHz	150p
7454	15p	74390	90p	74LS426	70p	4062	40p	CA3082	285p	MC6847	£65p	DS8875	225p	6.00MHz	150p
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7460	15p	74390	90p	74LS432	70p	4068	40p	CA3088	285p	MC6847	£65p	DS8881	225p	6.00MHz	150p
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7465	15p	74390	90p	74LS437	70p	4073	40p	CA3093	285p	MC6847	£65p	DS8886	225p	6.00MHz	150p
7466	15p	74390	90p	74LS438	70p	4074	40p	CA3094	285p	MC6847	£65p	DS8887	225p	6.00MHz	150p
7467	15p	74390	90p	74LS439	70p	4075	40p	CA3095	285p	MC6847	£65p	DS8888	225p	6.00MHz	150p
7468	15p	74390	90p	74LS440	70p	4076	40p	CA3096	285p	MC6847	£65p	DS8889	225p	6.00MHz	150p
7469	15p	74390	90p	74LS441	70p	4077	40p	CA3097	285p	MC6847	£65p	DS8890	225p	6.00MHz	150p
7470	30p	74390	90p	74LS442	70p	4078	40p	CA3098	285p	MC6847	£65p	DS8891	225p	6.00MHz	150p
7471	30p	74390	90p	74LS443	70p	4079	40p	CA3099	285p	MC6847	£65p	DS8892	225p	6.00MHz	150p
7472	30p	74390	90p	74LS444	70p	4080	40p	CA3100	285p	MC6847	£65p	DS8893	225p	6.00MHz	150p
7473	25p	74390	90p	74LS445	70p	4081	40p	CA3101	285p	MC6847	£65p	DS8894	225p	6.00MHz	150p
7474	25p	74390	90p	74LS446	70p	4082	40p	CA3102	285p	MC6847	£65p	DS8895	225p	6.00MHz	150p
7475	25p	74390	90p	74LS447	70p	4083	40p	CA3103	285p	MC6847	£65p	DS8896	225p	6.00MHz	150p
7476	25p	74390	90p	74LS448	70p	4084	40p	CA3104	285p	MC6847	£65p	DS8897	225p	6.00MHz	150p
7477	25p	74390	90p	74LS449	70p	4085	40p	CA3105	285p	MC6847	£65p	DS8898	225p	6.00MHz	150p
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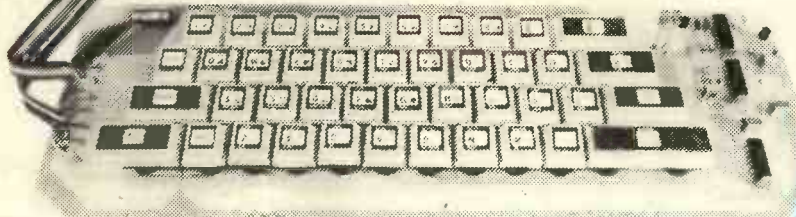


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