Technical Specification

ATLAS Level-1 Calorimeter Trigger Upgrade

FEX System Switch Module (FEX Hub) Prototype

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Contents

1 Conventions

The following conventions are used in this document:

- The term “Hub” or “FEX-Hub” is used to refer to the Phase-I L1Calo FEX system ATCA switch (hub) module in the rest of this document.
- The L1Calo FEX system Readout Driver (ROD) mezzanine is referred to as the “Hub-ROD” or just “ROD” in this document.
- FEX-Hub modules can be physically located in logical slots 1 or 2. The convention for the remainder of this document is to refer to these different modules as Hub-1 and Hub-2, respectively. Likewise the ROD modules in logical slots 1 or 2 are referred to as ROD-1 and ROD-2.
- The convention in this document will be that Hub-1 is the receiver of the TTC signal from the upstream FELIX system, and thus is responsible for distributing these signals to the FEX, ROD and Hub-2 recipients.
- A programmable parameter is defined as one that can be altered under computer control, for example between runs, not on an event-by-event basis. Changing such a parameter does not require a re-configuration of any firmware.
- Where multiple options are given for a link speed, for example, the readout links of the FEX modules are specified as running ≤6.4 Gb/s, this indicates that the link speed has not yet been fully defined. Once it is defined, that link will run at a single speed.
- In accordance with the ATCA convention, a crate of electronics is here referred to as a shelf.
- Figure 1 explains the timeline for ATLAS running and shutdowns: Phase-I upgrades will be installed before the end of long shutdown LS 2; Phase-II upgrades will be installed before the end of LS 3.
- The term “*buffer”* is used to mean electrical reception and re-transmission of signals (possibly with fan-out), but without any storage or memory function. The terms “*storage buffer*”, “*FIFO*”, “*Dual Port RAM*” et al. are used where storage is involved.

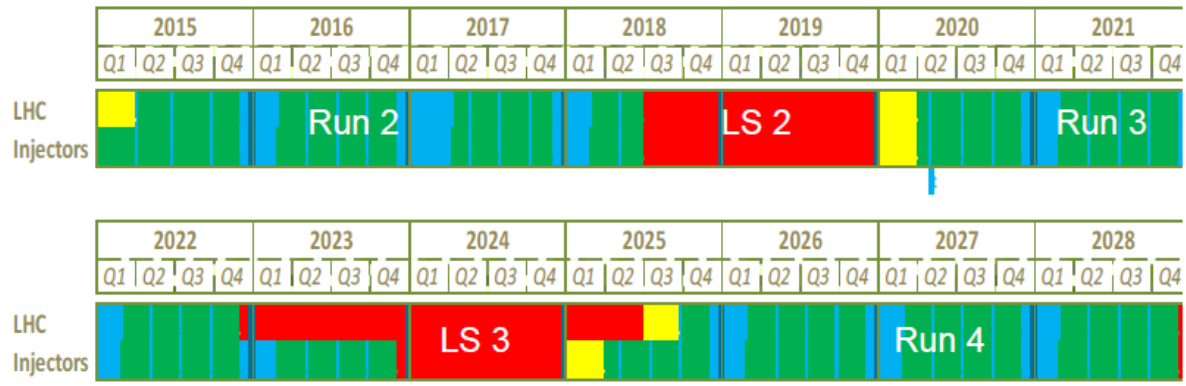


Figure 1: LHC shutdown and run schedule.

2 Related Documents

[1.1] ATLAS TDAQ System Phase-I Upgrade Technical Design Report, CERN-LHCC-2013-018, http://cds.cern.ch/record/1602235/files/ATLAS-TDR-023.pdf

[1.2] L1Calo Phase-I eFEX Specification, https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/

[1.3] L1Calo Phase-I jFEX Specification, https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/

[1.4] L1Calo gFEX Specification, https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/

[1.5] L1Calo Phase-1 ROD Specification , https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/

[1.6] L1Calo Phase-I Optical plant Specification, https://twiki.cern.ch/twiki/pub/Atlas/LevelOneCaloUpgradeModules/

[1.7] ATCA Short Form Specification, http://www.picmg.org/pdf/picmg_3_0_shortform.pdf

[1.8] PICMG 3.0 Revision 3.0 AdvancedTCA Base Specification, *access controlled*, http://www.picmg.com/

[1.9] P. Moreira, A. Marchioro, and K. Kloukinas, The GBT, a Proposed Architecture for Multi-Gb/s Data Transmission in High Energy Physics, 2007. https://espace.cern.ch/GBT-Project/Papers/paperMoreiraGBT.doc

[1.10] Development of an ATCA IPMI controller mezzanine board to be used in the ATCA developments for the ATLAS Liquid Argon upgrade, http://cds.cern.ch/record/1395495/files/ATL-LARG-PROC-2011-008.pdf

[1.11] IPbus Protocol, https://svnweb.cern.ch/trac/cactus/export/trunk/doc/ipbus_protocol_v2_0.pdf

[1.12] Front-End Link Exchange (Felix), https://edms.cern.ch/document/13111772/1

[1.13] MEG-Array Connectors, https://cdn.amphenol-icc.com/media/wysiwyg/files/documentation/datasheet/boardwiretoboard/bwb_megarray_mezzanine.pdf

[1.14] ATLAS L1Calo System-Level Specifications, https://edms.cern.ch/document/1492098/1

[1.15] Spencer Lee, Hub Gigabit Ethernet test description, https://web.pa.msu.edu/hep/atlas/l1calo/hub/specification/2_final_design_review/Hub_GbE_Test_Report_v0_1.pdf

[1.16] Hub firmware specification, https://web.pa.msu.edu/hep/atlas/l1calo/hub/specification/2_final_design_review/HUB_FW_Spec_FDR_03_12_2018.pdf

3 Introduction

This document describes the ATCA switch module (FEX-Hub) of the ATLAS Level-1 Calorimeter Trigger Processor (L1Calo) system [1.1] . The FEX-Hub is one of several modules being designed to upgrade L1Calo, providing the increased discriminatory power necessary to maintain trigger efficiency as the LHC luminosity is increased beyond that for which ATLAS was originally designed.

The function of the FEX-Hub module is to provide common communications functions for the FEX ATCA shelves including the routing of FEX readout data, network communications to and from FEX modules and distribution of clock and control signals.

The FEX-Hub modules will be installed in L1Calo during the long shutdown LS2, as part of the Phase-1 upgrade, and will operate during Run 3. They will remain in the system after the Phase-2 upgrade in LS3, and will operate during Run 4, at which time they will form part of L0Calo. The following sections provide overviews of L1Calo in Run 3 and L0Calo in Run 4.

This is a specification for the production FEX-Hub module. This final version will deliver the required functionality for the L1Calo FEX system. This specification further describes possible use cases not critical to the core Hub functionality that represent fallback options for the L1Calo (L0Calo) readout system if needed.

This document is arranged as follows. The front portion of the document introduces the L1Calo system, the plans for its upgrade and the upgrade evolutions. Next, a descriptive overview of the FEX-Hub module is provided, describing the primary specifications for its functionality within the L1Calo trigger system, including system interfaces and the implementation of the FEX-Hub itself. Finally, there are two appendices that enter into the details of how the FEX-Hub module has been designed and built, which provide an official reference on the “as built” FEX-Hub specification.

3.1 L1Calo Overview

3.1.1 Overview of the L1Calo System in Phase I (Run 3)

In Run 3, L1Calo contains three subsystems installed prior to LS2, as shown in Figure 2 (see document [1.1]):

- The Pre-processor, which receives shaped analog pulses from the ATLAS calorimeters, digitises and synchronises them, identifies the bunch-crossing from which each pulse originated, scales the digital values to yield transverse energy (E_T), and prepares and transmits the data to the following processor stages;

- The Cluster Processor (CP) subsystem (comprising Cluster Processing Modules (CPMs) and Common Merger Extended Modules (CMXs)) which identifies isolated e/γ and τ candidates;
- The Jet/Energy Processor (JEP) subsystem (comprising Jet-Energy Modules (JEMs) and Common Merger Extended Modules (CMXs)) which identifies energetic jets and computes various local energy sums.

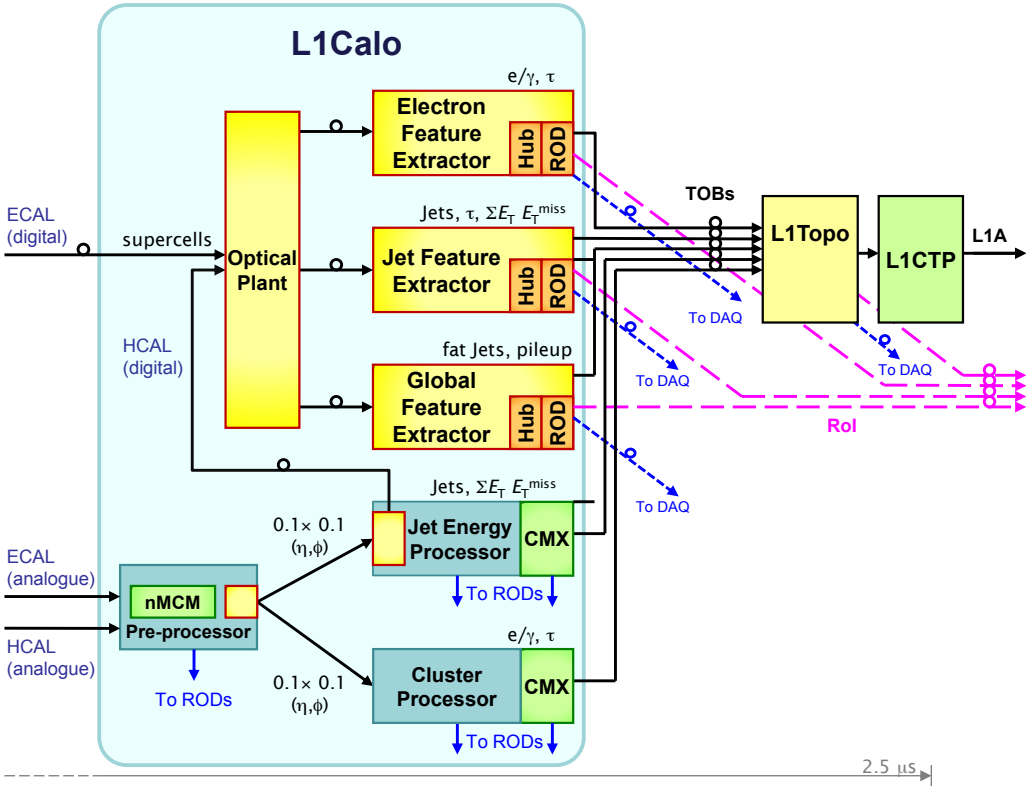


Figure 2: The L1Calo system in Run 3. *Components installed during LS2 are shown in yellow/orange*

Additionally, L1Calo contains the following three subsystems installed as part of the Phase-I upgrade in LS2:

- The electromagnetic Feature Extractor eFEX subsystem, comprising eFEX modules and FEX-Hub modules, the latter carrying Readout Driver (ROD) daughter cards. The eFEX subsystem identifies isolated e/γ and τ candidates, using data of finer granularity than is available to the CP subsystem.
- The jet Feature Extractor (jFEX) subsystem, comprising jFEX modules, and Hub modules with ROD daughter cards. The jFEX subsystem identifies energetic jets and computes various local energy sums, using data of finer granularity than that available to the JEP subsystem.
- The global Feature Extractor (gFEX) subsystem, which is a single, stand-alone module. The gFEX subsystem identifies calorimeter trigger features requiring the complete calorimeter data.

- An updated Level-1 Topological Processing subsystem (L1Topo), comprising L1Topo modules, and Hub modules with ROD daughter cards. The L1Topo subsystem applies topological selection and threshold criteria on trigger objects derived from the calorimeter and muon detector systems.

In Run 3, the Liquid Argon Calorimeter provides L1Calo both with analog signals (for the CP and JEP subsystems) and with digitized data (for the FEX subsystems). From the hadronic calorimeters, only analog signals are received. These are digitized on the Pre-processor, transmitted electrically to the JEP, and then transmitted optically to the FEX subsystems. Initially at least, the eFEX and jFEX subsystems will operate in parallel with the CP and JEP subsystems. Once the performance of the FEX subsystems has been validated, the CP sub system will be removed, and the JEP used only to provide hadronic data to the FEX subsystems.

The optical signals from the JEP and LDPS electronics are sent to the FEX subsystems via an optical plant. This performs two functions. First, it separates and reforms the fibre bundles, changing the mapping from that employed by the LDPS and JEP electronics to that required by the FEX subsystems. Second, it provides any additional fan-out of the signals necessary to map them into the FEX modules where this cannot be provided by the calorimeter electronics.

The outputs of the FEX subsystems (plus CP and JEP) comprise Trigger Objects (TOBs): data structures which describe the location and characteristics of candidate trigger objects. The TOBs are transmitted optically to the Level-1 Topological Processor (L1Topo), which merges them over the system and executes topological algorithms, the results of which are transmitted to the Level-1 Central Trigger Processor (CTP).

The eFEX, jFEX, gFEX and L1Topo subsystems comply with the ATCA standard. The eFEX subsystem comprises two shelves each of 12 eFEX modules. The jFEX subsystem comprises a single ATCA shelf holding 6 jFEX modules. The gFEX subsystem comprises a single ATCA shelf holding a single gFEX module. The L1Topo subsystem comprises a single ATCA shelf housing up to four L1Topo modules, each of which receives a copy of all data from all FEX modules. All L1Calo processing modules produce Region of Interest (RoI) and DAQ readout on receipt of a Level-1 Accept signal from the CTP. RoI information is sent both to the High-Level Trigger (HLT) and the DAQ system, while the DAQ data goes only to the DAQ system. In the FEX and L1Topo subsystems, these data are transmitted by each FEX or L1Topo module via the shelf backplane to two Hub modules (with the exception of the gFEX, which requires no Hub/ROD). Each of these buffers the data and passes a copy to their ROD daughter board. The RODs perform the processing needed to select and transmit the RoI and DAQ data in the appropriate formats; it is likely that the required tasks will be partitioned

between the two RODs. Additionally, the Hub modules provide distribution and switching of the TTC signals and control and monitoring networks.

3.1.2 Overview of the L1Calo System in Phase-II (Run 4)

The Phase-II upgrade will be installed in ATLAS during LS3. At this point, substantial changes will be made to the trigger electronics. All calorimeter input to L1Calo from the electromagnetic and hadronic calorimeters will migrate to digital format, the structure of the hardware trigger will change to consist of two levels, and a Level-1 Track Trigger (L1Track) will be introduced and will require TOB seeding. The Pre-processor, CP and JEP subsystems will be removed, and the FEX subsystems, with modified firmware, will be relabelled to form the L0Calo system in a two stage (Level-0/Level-1) real-time trigger, as shown in Figure 3. Hence, the FEX subsystems must be designed to meet both the Phase-I and Phase-II upgrade requirements. The main additional requirements are to provide real-time TOB data to L1Track, and to accept Phase-II timing and control signals including Level-0 Accept (L0A) and Level-1 Accept. Additional calorimeter trigger processing will be provided by a new L1Calo trigger stage.

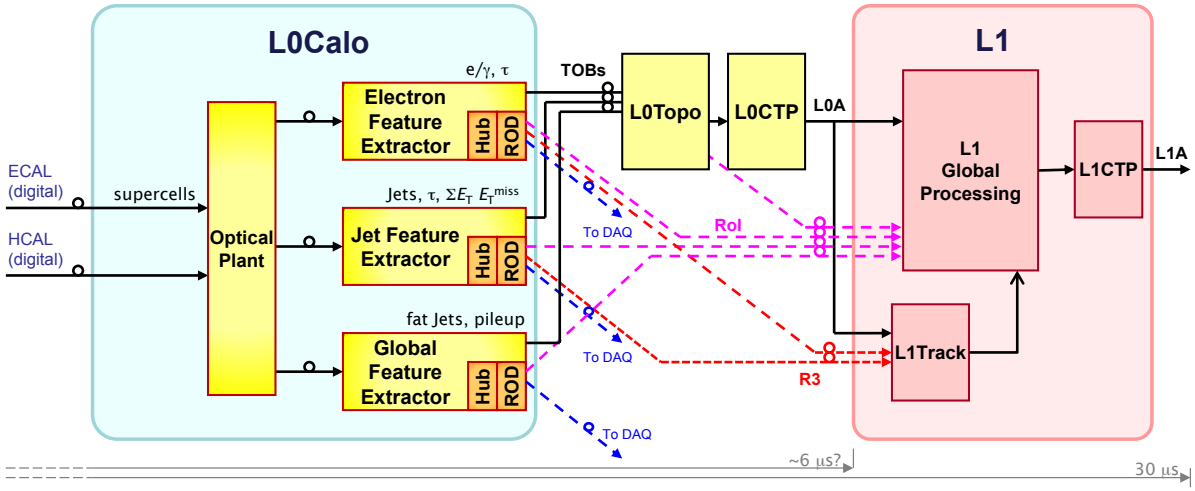


Figure 3: The L0/L1Calo system in Run 4. *The new Level-1 system is shown in red and pink. Other modules (yellow /orange) are adapted from the previous system to form the new L0Calo.*

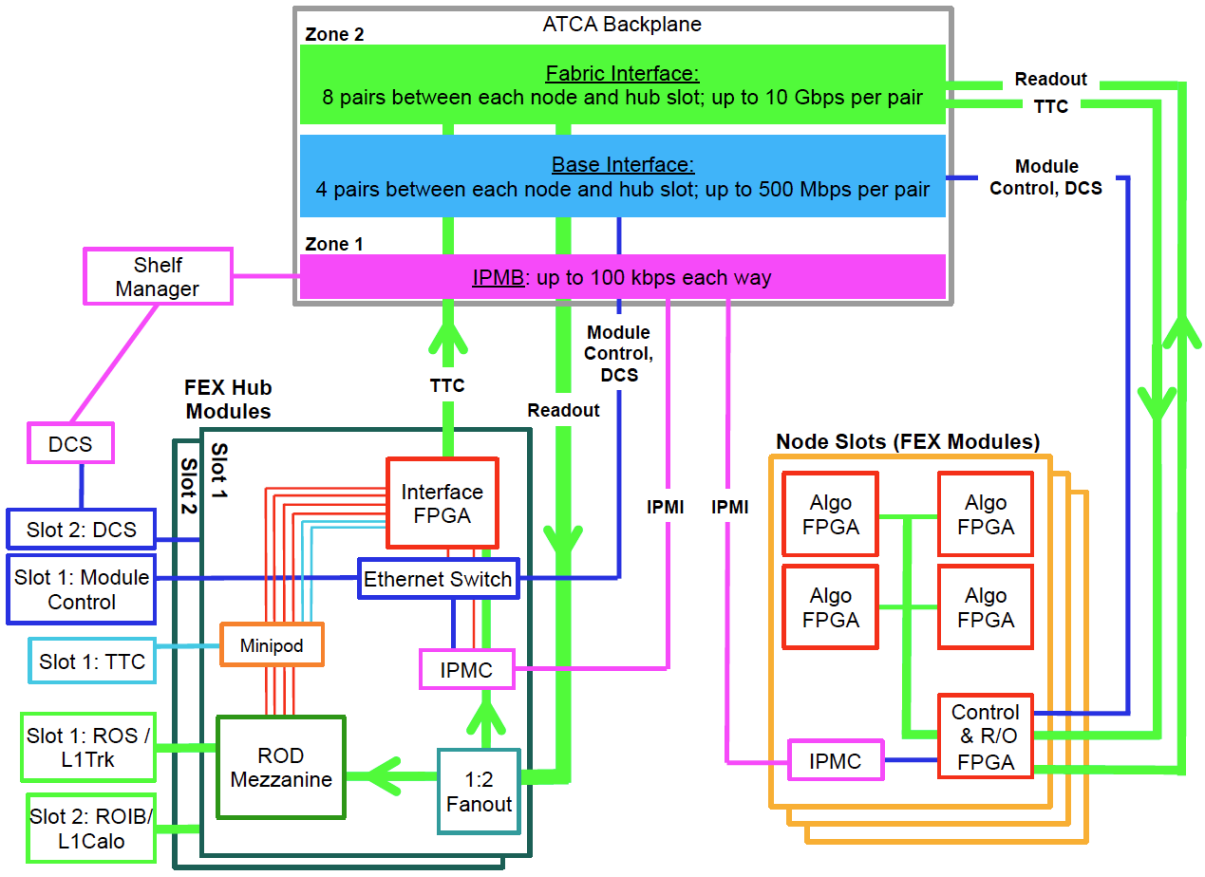
3.2 FEX-Hub Module Overview

The FEX-Hub module is an integral part of the L1Calo system. Its primary functions are to support FEX system readout, provide switching functionality for module control and DCS IPbus networks and to distribute timing and control signals to the FEX modules. **Figure 4** shows a sketch of the Hub modules within the FEX ATCA shelves. There are to be two Hub modules per shelf. Both Hub modules will receive multi-gigabit FEX data over the ATCA Fabric Interface, which will be fanned out to a ROD mezzanine on the

Hub and to the Hub's own FPGA. This high-speed data path will include two data channels from the other Hub module. The Hub module in logical slot 1 will provide switching capability for a network that routes module control signals on the base interface, while the Hub in logical slot 2 will provide switching for a network that routes DCS information. The Hub module in slot 1 will further receive TTC information from the FELIX system, and these signals will be decoded and fanned out to the FEX modules, ROD modules and also to the Hub in slot 2. The fanned-out TTC control data stream will be interleaved with ROD-to-FEX communications including, for example, back-pressure signals.

The Hub module has connections to the other slots in the ATCA shelf over three distinct electrical interfaces, as illustrated in **Figure 4**. ATCA backplane Zone-2 consists of the Fabric Interface and the Base Interface. The Fabric Interface provides 8 differential pairs (channels) from each node slot to each Hub slot (8 to Hub-1 and 8 to Hub-2). There are a total of 8 Fabric Interface channels between Hub-1 and Hub-2 (not 16 total). The Fabric Interface pairs have a nominal bandwidth specification of 10 Gbps / channel. The Base Interface provides 4 differential pairs between each node slot and each Hub slot. There are a total of 4 Base Interface channels between Hub-1 and Hub-2. The Base Interface lines have a nominal bandwidth specification of 500 Mbps / channel, suitable for Gbps Ethernet protocol. Finally, ATCA backplane Zone-1 provides each node and Hub slot with a connection to the Intelligent Platform Management Bus (IPMB) with a total bandwidth of 100 kbps. The Hub module will provide MPO connectors in the ATCA Zone-3 region, which will allow for the routing of fiber-optic cables to/from the MiniPODs on the Hub and ROD modules.

The L1Calo FEX-Hub system will consist of eight modules. There will be two eFEX shelves, one jFEX shelf and one L1Topo shelf, each hosting two Hub modules.



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446 **Figure 4:** Illustration of the functions of FEX-Hub modules within the FEX trigger
447 system, emphasizing the data paths through the ATCA backplane.

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4 FEX-Hub Module Functionality

This section describes the functionality required for the FEX-Hub module within the L1Calo FEX trigger system. Details of the implementation of these functions will be described in Section 6 of this document. **Figure 5** illustrates the overall layout of the Hub module, including the outline of the ROD mezzanine card. In this figure, all of the primary functions and features of the Hub module are annotated for reference.

4.1 Support of the ROD Mezzanine Card

The FEX-Hub physically holds the ROD Mezzanine Card and provides electrical connections to it through two 400 pin MEG-Array connectors [1.13] .

4.2 FEX and FEX-Hub Readout Data Distribution

The FEX-Hub receives over the Fabric Interface 6 serial streams of Readout Data from each FEX Module. Each FEX-Hub also receives over the Fabric Interface 2 serial streams of Readout Data from the other FEX-Hub in the ATCA shelf. These 74 high-speed serial streams pass through a 1:2 fan-out on the FEX-Hub. One copy of each stream is sent to the ROD mezzanine and one copy is sent to the Hub's own FPGA. The Hub FPGA also sends 2 serial streams with its own Readout Data to its own ROD. Each ROD thus receives a total of 76 high speed Readout Data streams: 6 streams from each FEX, 2 streams from the local Hub FPGA and 2 streams from the other Hub's Hub FPGA. The data rate per readout stream will be 10 Gbps or less.

4.3 TTC Clock and Data Stream Distribution

The FEX-Hub in Slot 1 uses a 12-channel MiniPOD optical receiver to receive TTC signals from the upstream FELIX system. The FEX-Hub receives two types of TTC signals: a copy of the LHC clock and TTC control data. These signals are fanned out to each FEX module, to the local ROD, to the local Hub FPGA and to the FEX-Hub in Slot 2 (including its ROD). The LHC clock is directly forwarded without any processing on the FEX-Hub. The TTC control data will be merged with additional control information coming from the ROD module from each FEX-Hub before being fanned out. The FEX-Hub uses two ports from the Fabric Interface Channel to each Node Slot to fan out these two signals to each FEX. These two TTC and control signals sent to the FEX plus the 6 Readout Data streams received from each FEX use all 8 signals pairs of each Fabric Channel connecting one FEX to the FEX-Hub, albeit with an unconventional port direction usage.

The FEX-Hub in Slot 2 does receive the TTC information from FELIX directly, but receives the TTC Clock and the TTC/ROD readout control stream from the FEX-Hub in

Slot 1. The FEX-Hub in Slot 2 sends any required ROD readout control data generated by its own ROD to the FEX-Hub in Slot 1 for inclusion in the combined TCC/ROD readout control data stream.

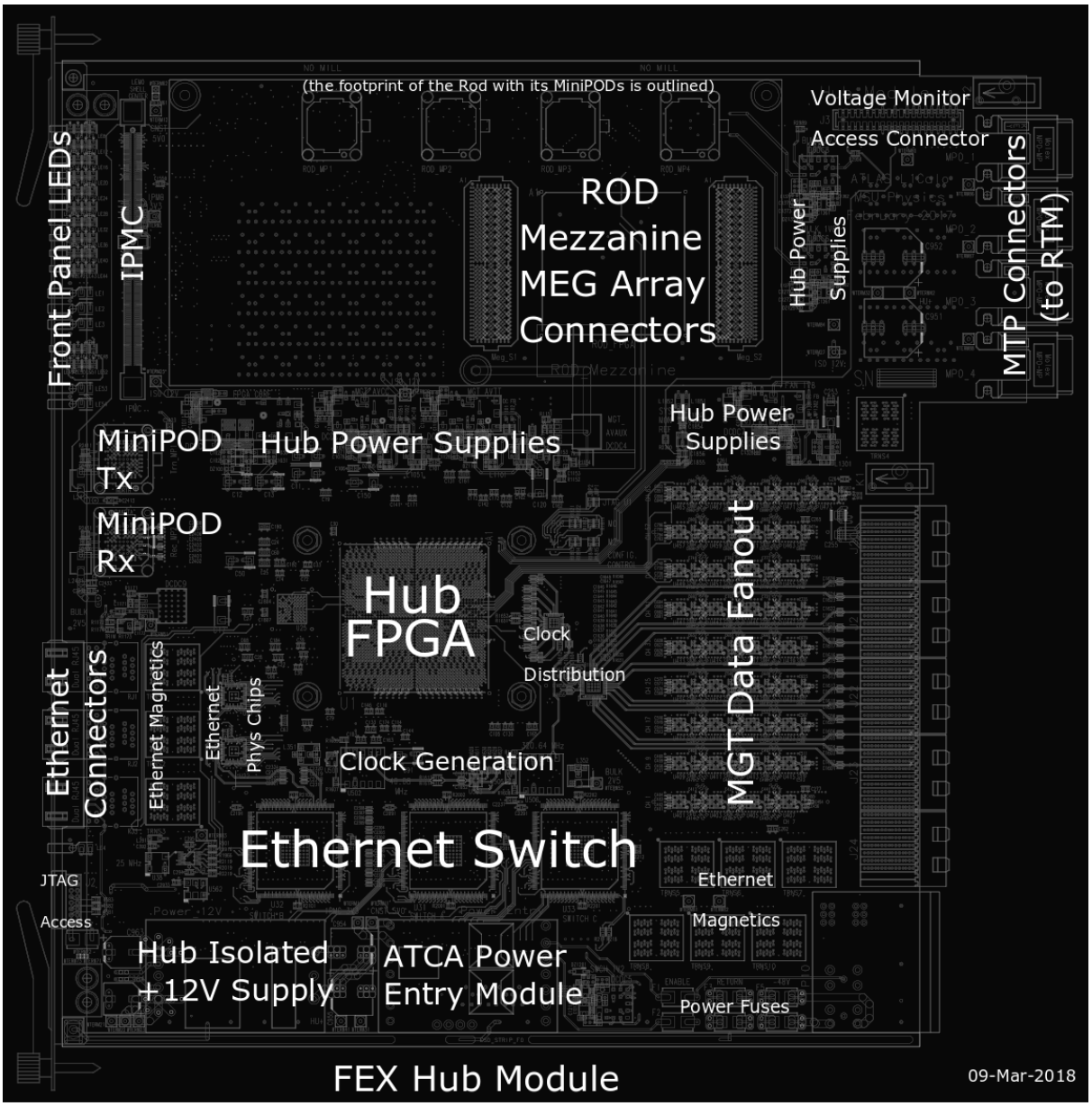


Figure 5: Annotated layout of Hub (+ROD outline) with primary functions noted.

4.4 Ethernet Network Switch

The FEX-Hub hosts an un-managed 10/100/1000 Base-T switch to provide the following 18 Gigabit Ethernet connections:

- Backplane: 12 connections to the "FEX Node" modules in this crate via the Base Channel Fabric;
- Backplane: 1 connection to the Ultrascale FPGA on the other Hub via the Update Channel Interface;
- Direct: 1 connection to the Ultrascale FPGA on this Hub;
- Front-Panel: 1 connection for an "up-link";
- Front-Panel: 1 connection for the ROD on this Hub (or IPMC on the other Hub);
- Front-Panel: 1 connection for the ROD on the other Hub (or IPMC on this Hub);
- Front-Panel: 1 spare connection;

This Ethernet switch functionality is implemented in hardware with three interconnected 8-port switch chips.
The FEX-Hub module circuit board can be modified to disconnect these three switch chips and provide a higher aggregate bandwidth capacity as described in Section 5.

4.5 Slow Control

An IPBus interface is provided for high-level, functional control of the FEX-Hub module. This allows, for example, any firmware parameters to be set, modes of operation to be controlled and monitoring data to be read.

4.6 Connections to the IPMB

The FEX-Hub maintains a connection to the Intelligent Platform Management Bus (IPMB) via an IPM Controller (IPMC) located on the Hub module. Communications between monitorable targets on the Hub, including the ROD mezzanine, are managed via an I2C Bus on the Hub module.

4.7 Power Supplies

The FEX-Hub provides all of the normal ATCA redundant power input, power isolation, and power control from the Shelf Manager via an IPMC card. Bulk +12 Volt power is provided to the ROD Mezzanine Card. Control signals are sent from the Hub to the ROD and Status signals are returned from the ROD to manage the ROD's own power up sequence. DC/DC converters are used to provide the power rails for the Hub itself.

4.8 Extended Use Cases

The FEX-Hub module is intended to be used in the L1Calo and L0Calo trigger systems through Run 4. As such, future use cases in which the Hub may need to augment the capacity of the FEX-Hub-ROD readout path have been identified. This extra functionality is being implemented on the FEX-Hub so long as it does not complicate the core Hub functions and design. These extra Hub functions are as follows:

- The Hub main FPGA receives a fanned-out copy of all high-speed FEX data being sent to the ROD mezzanine card, allowing at a minimum the monitoring of FEX data. This feature can also support Hub commissioning and diagnostics, as it further provides a Fabric Interface connection to the other Hub module.

- The Hub main FPGA provides additional MGT links to the ROD mezzanine, which will be instrumented on the ROD if sufficient input MGT links are available. Similarly, MGT links from the ROD to the Hub main FPGA are defined on the HUB-ROD interface.

- External data output paths from the Hub main FPGA are provided electrically via Ethernet and optically via one MiniPOD transmitter. The MiniPOD socket and routings are implemented by default, but the MiniPOD transmitter is only installed if required.

Together, this Hub functionality can provide supplemental trigger processing if required. However, all of this functionality could instead be ignored or disabled with no negative impact on the Hub core functions.

4.9 Commissioning and Diagnostic Facilities

The FEX-Hub module provides sufficient Hub-to-Hub electrical connections over the Fabric Interface, Base Interface and front-panel connections to commission and perform standalone diagnostic tests of the Ethernet switching functions, a subset of Fabric Interface high-speed data paths and TTC clock/data distribution using either one or two FEX-Hub modules.

Full commissioning and diagnostics will require a mated Hub+ROD, as well as a data source/sink for the node slots (eg, the FEX Test Module or Hub Test Module). The Hub testing and commissioning plan is discussed in greater detail in Section 8.

4.10 Environment Monitoring

The Hub monitors the voltage and current of every power rail on the board. It also monitors the temperatures of FPGAs, of the MiniPOD transmitters (if installed), and of other areas of dense logic. Where possible, this is done using sensors embedded in the relevant devices themselves. Where this is not possible, discrete sensors are used. The voltage and temperature data are collected by the IPMC, via an I2C bus. From there, they are transmitted via Ethernet to the ATLAS DCS system. The Hub hardware also allows these data to be transmitted to the DCS via IPMB and the ATCA Shelf Controller, but it is not foreseen that ATLAS will support this route.

4.11 ATCA Form Factor

The FEX-Hub module is an ATCA module, conforming to the PICMG® 3.0 Revision 3.0 specification. The FEX-Hub is only capable of supporting a Dual-Star 14-slot (not 16) ATCA shelf. Within the L1calo system some of the Fabric Interface and Update Interface Channel ports are not used according to their conventional ATCA manner, as described in the technical detail appendices, see Sections 15 and 17.

5 Interfaces to Other L1Calo Modules

The FEX-Hub module has mechanical and electrical connections to three other module types within the L1Calo trigger system: the Hub-ROD Mezzanine card, the eFEX/jFEX/L1Topo modules and the other Hub module when used in a shelf with two Hubs. This section describes and illustrates the electrical connections between these modules.

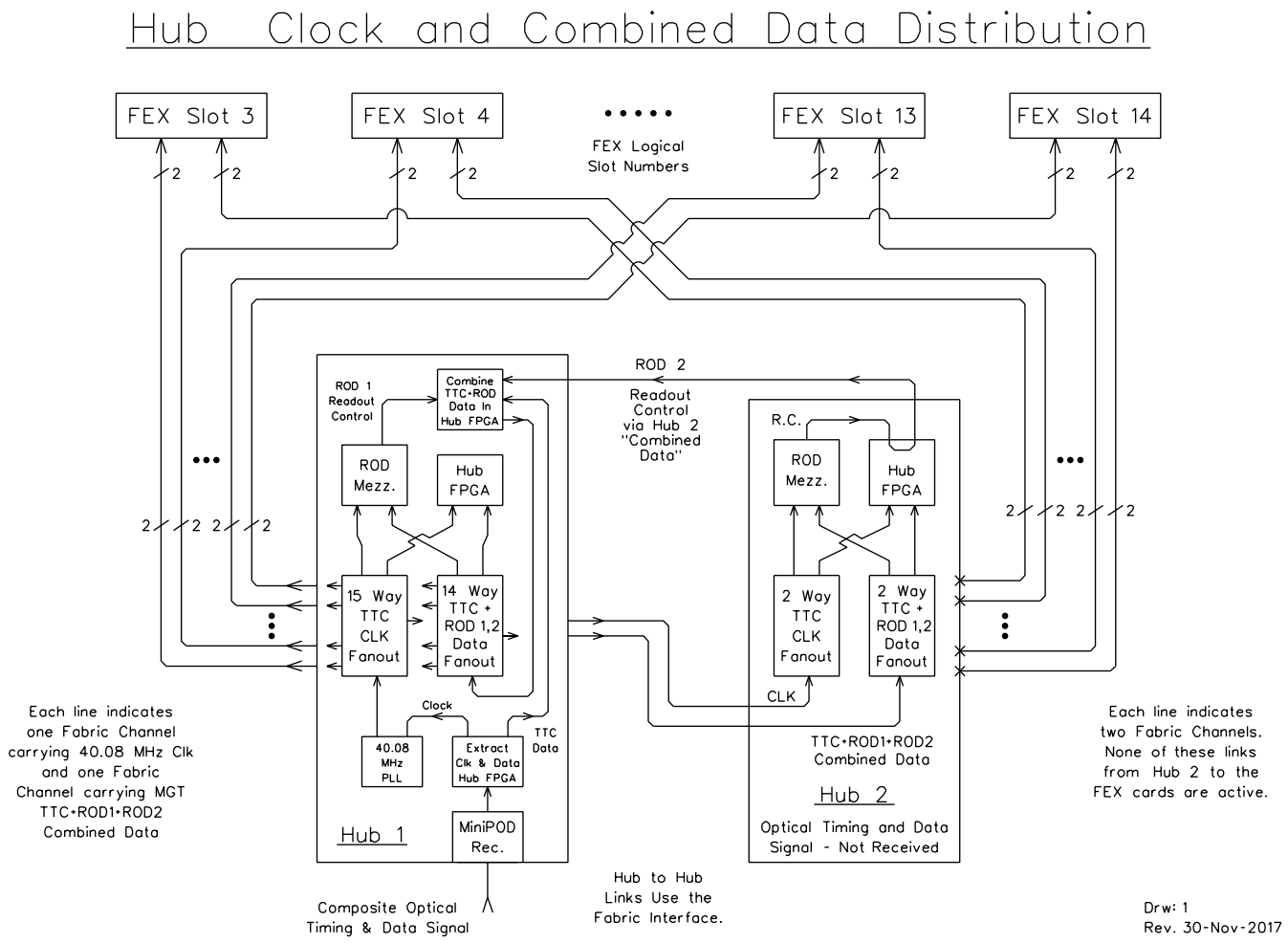
5.1 TTC Clock and Data Stream Interfaces

Figure 6 shows the Hub's distribution of the TTC Clock and Data signals in the context of the other cards in the ATCA shelf. The composite TTC signal is received by a MiniPOD receiver on the Hub-1 card. The TTC Clock is fanned out from the Hub-1 card to all other modules in the shelf (including Hub-2) over the Fabric Interface. The TTC Data is combined with the back data from both ROD-1 and ROD-2 on Hub-1 and this combined data stream is also fanned out from the Hub-1 module over the Fabric Interface. When a second Hub is used as shown in **Figure 6**, no TTC information is sent from Hub-2 to any of the Node slots, as the corresponding Fabric Interface ports are not driven on Hub-2. The Hub-1 and Hub-2 cards are identical printed circuit boards and could support independent fan-out of clock and data streams from both Hubs if that were desired in the future. Each Node slot has access to both the Hub-1 and the Hub-2 TTC clock and data streams. L1calo shelves are however currently explicitly defined to provide and use the TTC clock and data information fanned out from Hub-1 only.

5.2 High-Speed Readout Data Interfaces

Figure 7 shows the Hub's distribution of readout data in the context of the cards in the ATCA shelf. The readout data comes from the Node slots and from the FPGA on each Hub module. All of this data flows to both the ROD and to the FPGA on each Hub. The arrangement shown in **Figure 7** supports 2 independent streams of readout data. That is, the readout stream processed by the ROD and Hub FPGA on Hub-1 can be independent of the readout stream flowing into Hub-2.

The Hub’s high-speed readout data path as described at the level of the Hub board is illustrated in **Figure 19**, which can be found in the section describing the Hub PCB layout (**Section 6.11**) and in greater detail in the technical detail appendices (**Section 15**).



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597 **Figure 6:** Illustration of FEX-Hub distribution of TTC clock and control data stream
598 signals.

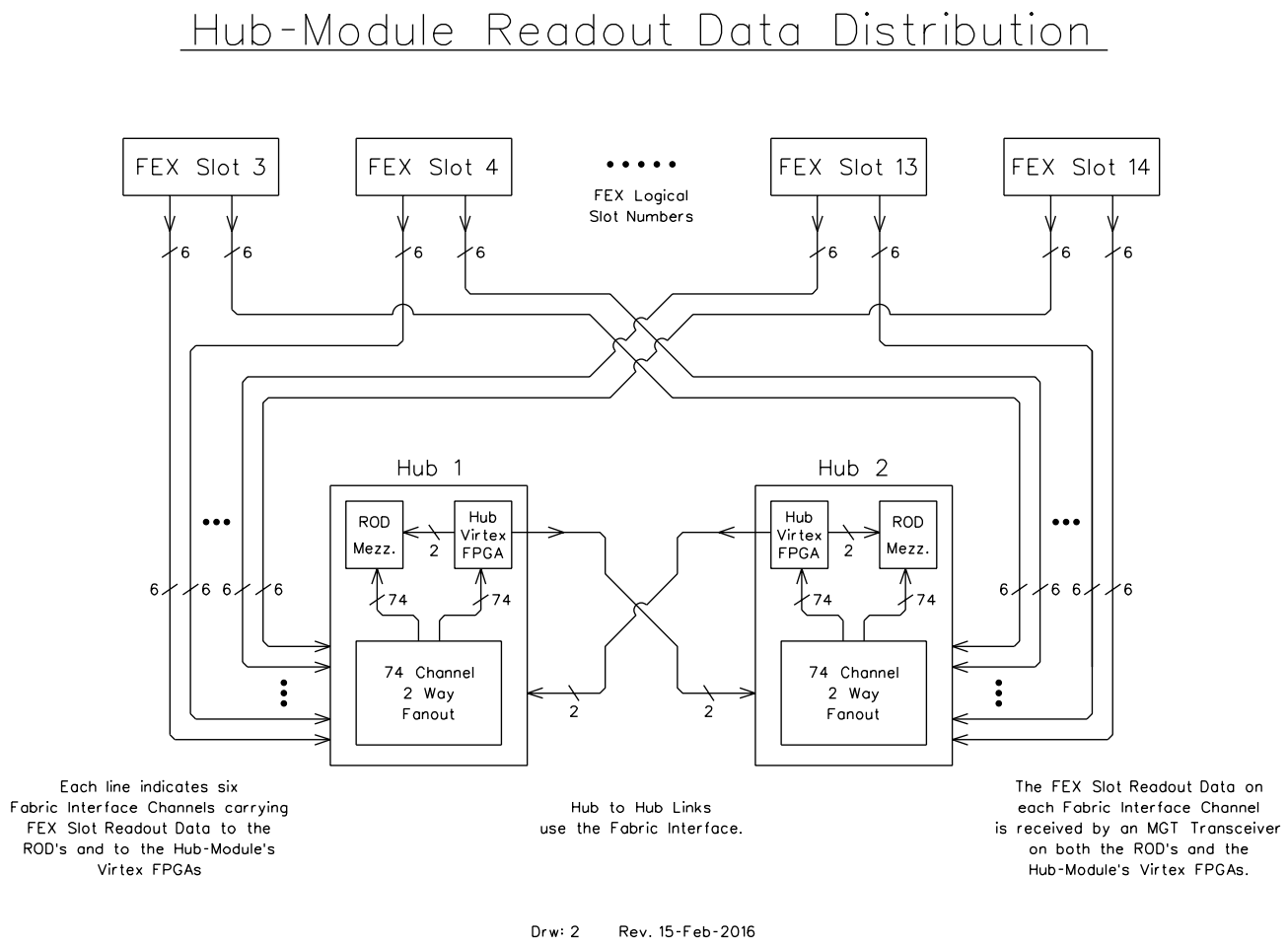


Figure 7: Illustration of FEX-Hub distribution of high-speed readout data signals.

5.3 Ethernet Network Interfaces

Figure 8 shows the Hub's Base Interface Ethernet Switch in the context of the other cards in the ATCA shelf. As shown in **Figure 8** the switch on Hub-1 is used to handle all connections to the IPbus Control network and the switch on Hub-2 is used to handle all connections to the IPMC/DCS network. Operation with only a Hub-1 in the shelf is possible but does not provide a Base Interface Ethernet connection to the IPMCs in the

Node slots. In this situation the Node slot IPMCs can use their IPMB connection to the Shelf Manager and pass monitoring data to the DCS network.

The Gigabit Ethernet switch functionality is implemented in hardware with three interconnected Broadcom BCM53128 8-port switch chips.

When these three switch Chips are left interconnected one up-link connection per Hub is used to connect the L1calo crate to the rest of the network. The available aggregate bandwidth for the whole shelf is 1 Gbps over each of the Hub1 and Hub 2 networks. The corresponding connectivity at the level of one typical L1Calo shelf is depicted in **Figure 9**.

The FEX-Hub module circuit board can be modified to severe the inter-connections between these three switch chips. This modification increases the aggregate bandwidth

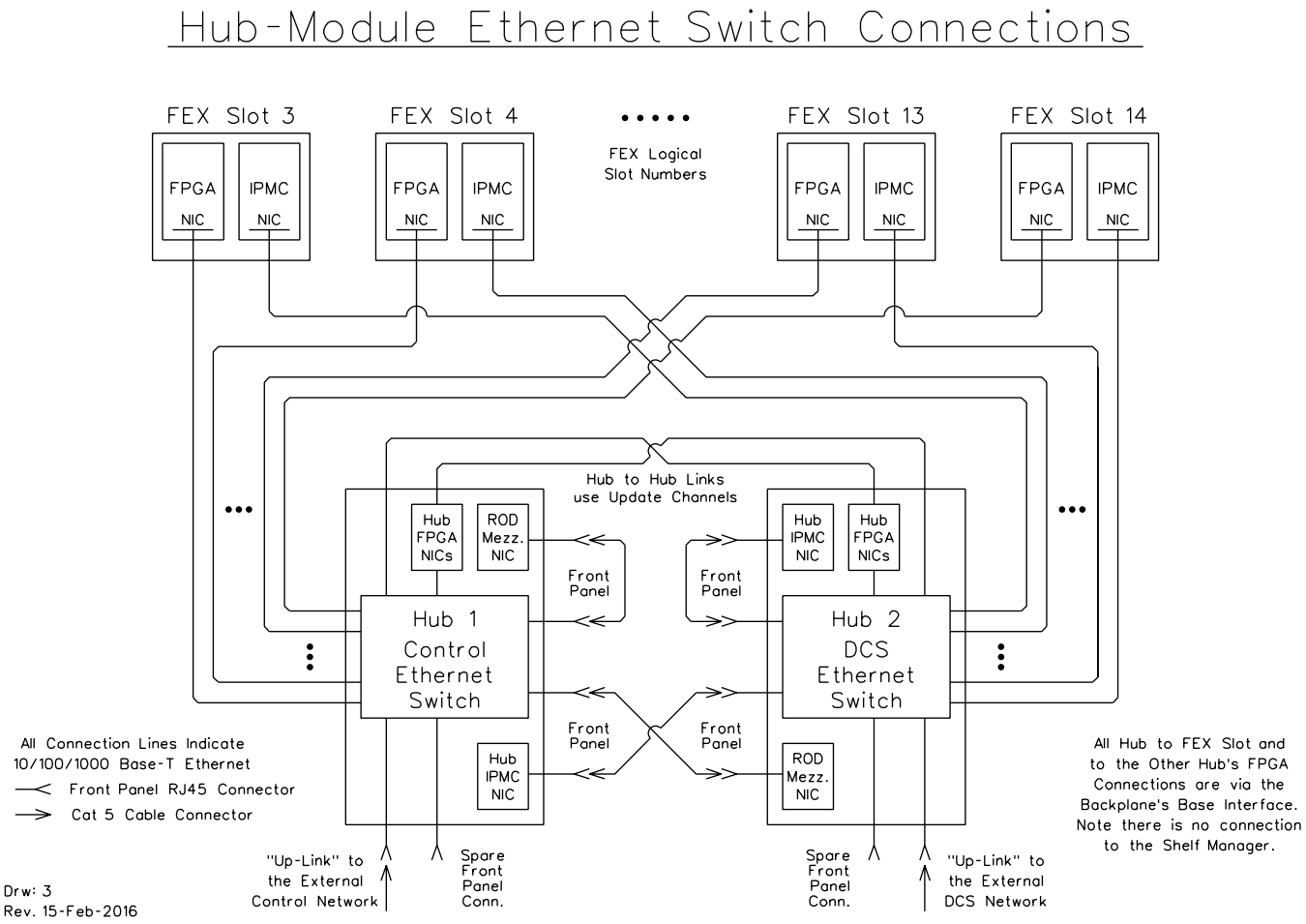


Figure 8: Circuit diagram for the Hub Ethernet switch.

capacity. In particular, the aggregate bandwidth is then doubled for the FEX node slots. Four up-link connections per Hub are then required to connect the L1calo crate to the rest of the network. The corresponding connectivity at the level of one typical l1calo crate is depicted in **Figure 10**.

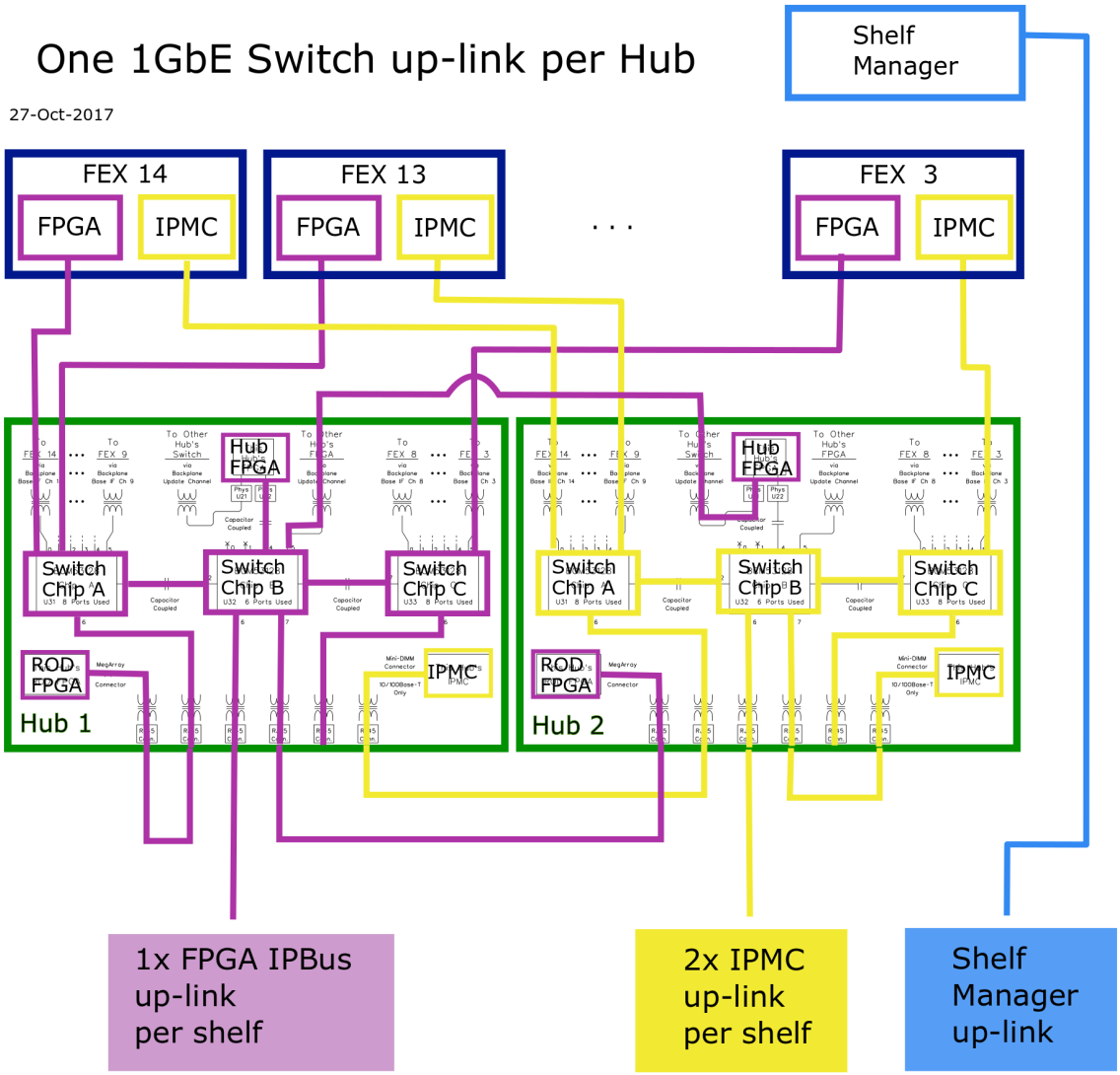


Figure 9: Hub Ethernet switch configuration with one uplink per shelf.

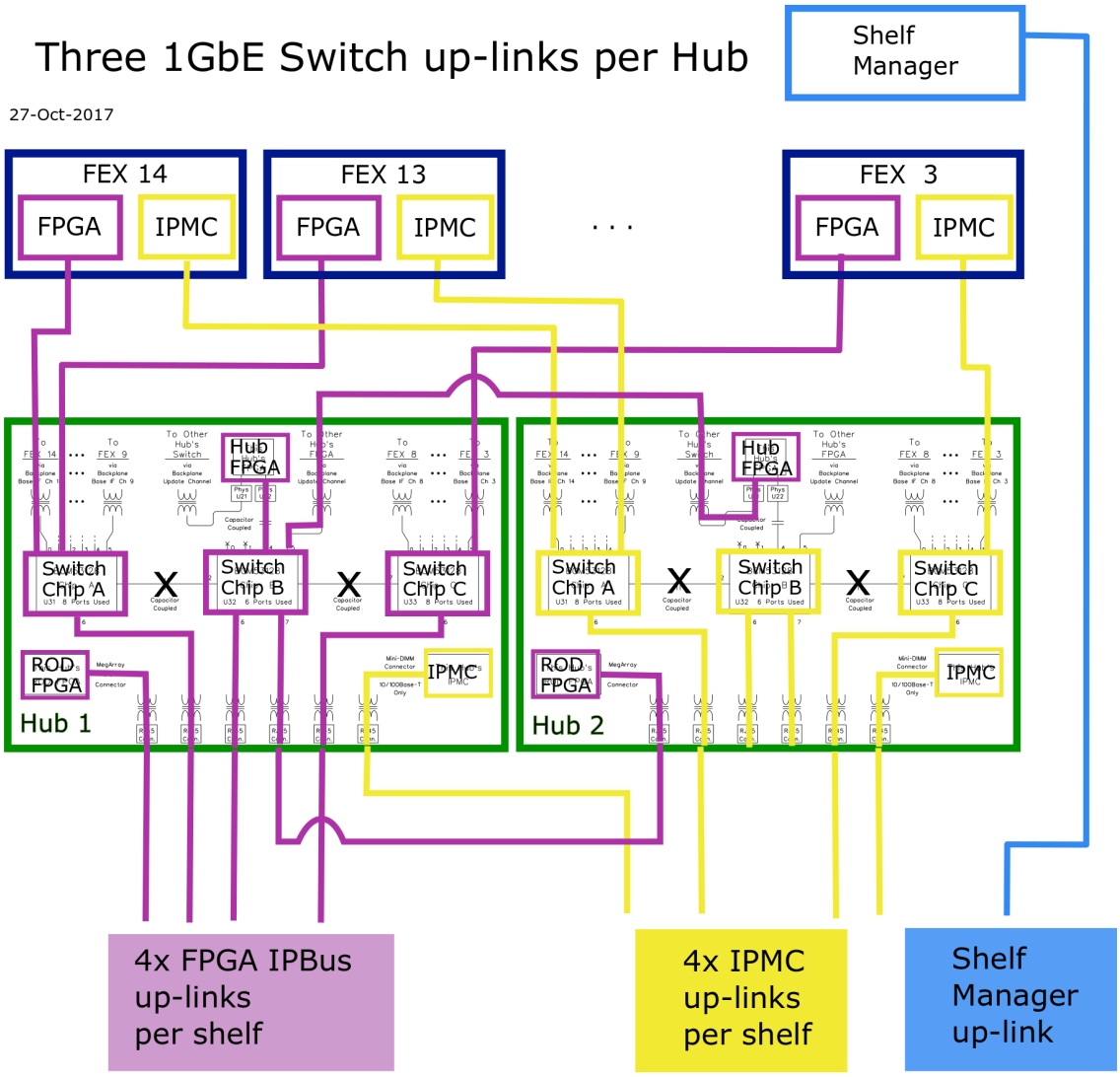


Figure 10: Hub Ethernet switch configuration with three uplinks per shelf.

5.4 Hub Interfaces to FEX Modules

This subsection summarizes the Hub electrical interfaces to the FEX modules. A more complete specification of the connector/pin assignments is illustrated in Appendix 1 (Section 14). Please refer there for more details.

5.4.1 Interface with Hub-1

Hub-1 resides in logical slot 1 and receives the TTC information from FELIX optically via MiniPOD. It thus distributes the TTC clock and control data signals. Hub-1 also hosts the slow control IPbus network.

5.4.1.1 Base Interface

The 2 ports of Base Channel 1 (4 pairs of differential signals) of the base interface are used to provide a Gigabit Ethernet connection to be used by the FEX module for its IPbus port.

The usage of the ports on this channel follows the ATCA PICMG 3.0 specification for 1000BASE-T Ethernet.

5.4.1.2 Fabric Interface

The ports of the Fabric Interface Channel 1 are not used according to the ATCA convention and notation.

The 4 ports of Fabric Channel 1 (8 pairs of differential signals) are defined by ATCA as 4 transmitting and 4 receiving pairs.

Hub-1 is instead transmitting on only 2 of these pairs and receiving readout data from the FEX on the other 6 pairs

5.4.1.3 Hub-1 Module signals as Seen from a FEX Module

The FEX modules receive the LHC clock on the receive signal pair of Fabric Interface Channel 1 port 0. (Note: this clock is received via MiniPOD on Hub-1). This signal is meant to be received as a logic clock and not as data stream. It is not driven by an FPGA MGT Transceiver on the HUB and is not meant to be received by an MGT on a FEX.

The FEX modules receive the combined TTC and ROD control data stream on the receive signal pair of Fabric Interface Channel 1 port 1. Note: the TTC control information is provided via the TTC signals sent by FELIX and received on Hub-1. The two RODs on Hub-1 and Hub-2 may need to also send control information to the FEXs. This optional ROD control is merged with the TTC control data stream according to a format to be determined.

The FEX modules send their primary readout data streams 0-3 destined to the ROD on Hub-1 on the transmit signal pair of Fabric Interface Channel 1 port 0-3. The FEX module is SENDING its secondary readout data streams 4-5 destined to the ROD on Hub-1 on the RECEIVE signal pair of Fabric Interface Channel 1 port 2-3 which means it is using these two ports in the opposite direction from their conventional usage and ATCA naming.

5.4.2 Interface with Hub-2

Hub-2 resides in logical slot 2 and hosts the IPMC network. Hub-2 does not receive the TTC signal from FELIX via its MiniPOD receiver.

5.4.2.1 Base Interface

The 2 ports of Base Channel 2 (4 pairs of differential signals) of the base interface are used to provide a Gigabit Ethernet connection to be used by the FEX module for its IPMC.

The usage of the ports on this channel follows the ATCA PICMG 3.0 specification for 1000BASE-T Ethernet.

5.4.2.2 Fabric Interface

The ports of Fabric Interface channel 2 are not used according to the ATCA convention and notation.

The 4 ports of Fabric Channel 2 (8 pairs of differential signal) are defined by ATCA as 4 transmitting and 4 receiving pairs.

Hub-2 is instead transmitting nothing on 2 of these pairs and receiving readout data from the FEX on the other 6 pairs.

5.4.2.3 Hub-2 Module Signals as Seen from a FEX Module

The receive signal pair of Fabric Interface Channel 2 port 0 is unused on FEX modules. The receive signal pair of Fabric Interface Channel 2 port 1 is also unused on FEX modules.

The FEX modules send their primary readout data streams 0-3 destined to the ROD on Hub-2 on the transmit signal pair of Fabric Interface Channel 2 port 0-3.

The FEX module is SENDING its secondary readout data streams 4-5 destined to the ROD on Hub-2 on the RECEIVE signal pair of Fabric Interface Channel 2 port 2-33 which means it is using these two ports in the opposite direction from their conventional usage and ATCA naming.

5.5 Hub Interface to the ROD Mezzanine

Two 400 pin MEG-Array connectors interface the ROD Mezzanine to the FEX-Hub. This section identifies the signals carried through these connectors. A more detailed description of these HUB-ROD connections is given in the technical appendices, **Sections 26, 19** and **18**. An illustration of how the signals are organized in the MEG-Array connectors is shown in **Figure 11**, which emphasizes the relative use of ground and signal pins for the high-speed data lines. This figure is for illustration only and the technical specification appendices should be used for the mapping.

Note: both the Ultrascale FPGA used on the FEX-Hub and the Virtex-7 FPGA used on the ROD offer a maximum of 80 MultiGigabit Transceivers (MGT) i.e. 80 Transmitter

ports and 80 MGT Receiver ports. The limit on the number of MGT Receivers has been the main limiting factor in the compromises reached in the design of both the Hub-FEX and the ROD.

5.5.1 MGT Differential Inputs to ROD from Hub

These differential signals are connected to MGT Receiver on the ROD FPGA.

- 12x6 = 72 serial streams of Readout Data from the FEX modules
- 2x serial streams of Readout Data from the local HUB FPGA
- 2x serial streams of Readout Data from the other HUB FPGA
- 1x serial stream of combined TTC and ROD control data stream

5.5.2 MGT Differential Outputs from ROD to Hub

- 1x serial stream of ROD Readout Control information

This signal needs to be merged with the TTC control data stream by the HUB FPGA of the FEX-Hub in slot 1.

A copy of this combined TTC and ROD control data stream is sent to the ROD FPGA from both FEX-Hub in Slot 1 and Slot 2.

5.5.3 Other signals between ROD and Hub

- LHC Clock
    - 1x Differential signal pair
- Geographic Address
    - 8x signals coming from the Hub FPGA

    The HUB FPGA determines this System Geographic Address by combining the J10 Hardware Address pins with the Shelf Address retrieved from the Shelf Manager by the IPMC. The shelf and slot addressing scheme for this 8-bit address needs to be defined.
- IPbus port
    - 4x Bi-directional Signal Pairs forming a 1000BASE-T Gigabit Ethernet connection.
- Sensor I2C Bi-directional Bus

- 2x I2C Signals (Clock and Data) connected to the IPMC

- JTAG access
  - 4x JTAG Signals
- Power Supply Connections
  - +12V bulk power is made available to the ROD
- Power Control signals: 4 single-ended bidirectional signals nominally used as
  - 2x Power Control Signals to the ROD
  - 2x Power Status Signals from the ROD
- Control and Status
  - 5x ROD-specified LEDs
  - 2x Phy LEDs
  - 1x Lemo
  - 4x spare bidirectional differential pairs
  - 1x ROD present

745

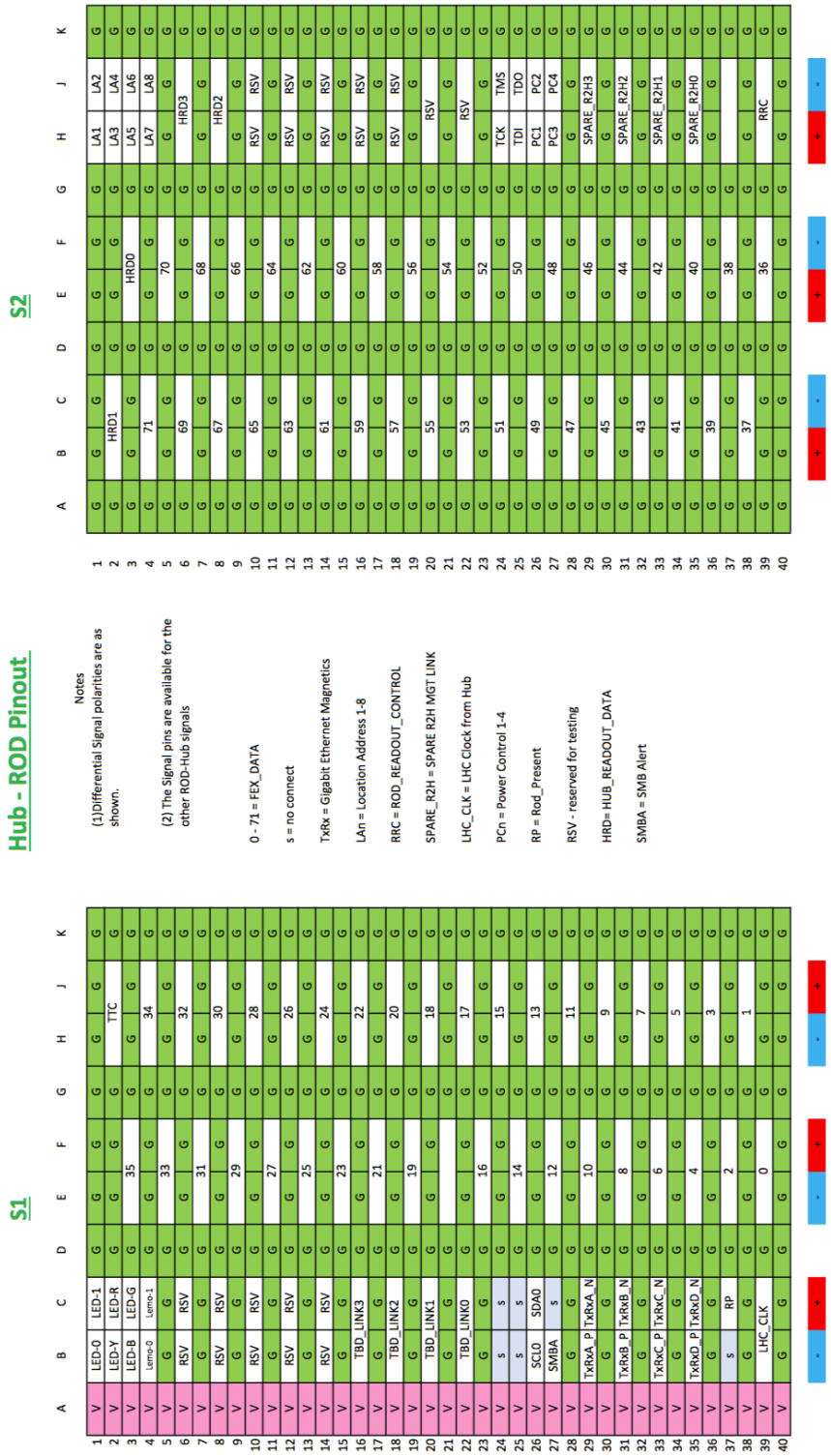


Figure 11: Illustration of the ROD/Hub MEG-Array connector pin usage, illustrating signal and ground designations. This diagram is not intended for signal mapping, and the final mapping is provided in the technical appendices.

5.6 Hub Interfaces to Second Hub Modules

5.6.1 Base Interface

The Base Channel 1 is reserved for the Shelf Manager Controller and is unused.

The Base Channel 2 port (4 pairs of differential signals) is not currently allocated.

5.6.2 Fabric Interface

The Fabric Interface channel 1 is used according to the ATCA convention and notation with one caveat for Hub-2: Hub-2 is transmitting nothing on 2 of its transmitter pairs.

5.6.3 Hub-2 usage of the Fabric Interface connection to Hub-1

Hub-2 is receiving the LHC clock on the receiving signal pair of Fabric Interface Channel 1 port 0.

Hub-2 is receiving the combined TTC and ROD control data stream on the receiving signal pair of Fabric Interface Channel 1 port 1.

Hub-2 is sending on the transmitting signal pair of Fabric Interface Channel 1 port 0-1 its readout data streams 1-2 destined to the ROD on Hub-1.

5.6.3.1 Hub-1 usage of the Fabric Interface connection to Hub-2

The receiving signal pair of Fabric Interface Channel 1 port 0 is unused on Hub-1.

Hub-1 is receiving on the receive signal pair of Fabric Interface Channel 1 port 1 the ROD Readout control information from the ROD on Hub-2.

Hub-1 is sending on the transmit signal pair of Fabric Interface Channel 1 port 0-1 its readout data streams 1-2 destined to the ROD on Hub-2.

5.6.4 Update Channel Interface

The 5 ports of the Update Channel (10 pairs of differential signal) are defined by ATCA as 5 transmitting and 5 receiving pairs. The first 4 ports of the Update Channel Interface are not used according to this ATCA convention and notation. The 5th port of the Update Channel Interface is not currently allocated.

The 4 Transmit pairs of Update Channel port 0-4 form one Gigabit Ethernet link and are connected to a Switch port of the local Hub. The 4 Receive pairs of Update Channel port 0-4 form another Gigabit Ethernet link and are connected to the Hub FPGA on the local Hub.

Note: the exact pin assignment of each port to the four 1000BASE-T signal pairs will be specified later while this assignment is internal to Hub operation only (no other L1Calo modules are affected).

This Hub-to-Hub connection allows the Hub FPGA on Hub-2 to connect to the IPbus Network serviced by the Ethernet switch on Hub-1.

The Hub FPGA on Hub-1 is directly connected to the IPbus Network switch on Hub-1 and can simply ignore this additional Ethernet port that would connect it to the IPMC Network serviced by the Ethernet switch on Hub-2.

6 Hub Implementation Details

This section describes the details of how the FEX-Hub functionality has been implemented for the prototype module, which is also the intended implementation for the final production module. The prototype FEX-Hub module is shown in **Figure 12** and **Figure 13**, wherein the ROD mezzanine card has been mounted to illustrate the anticipated final form of the Hub+ROD pairing.

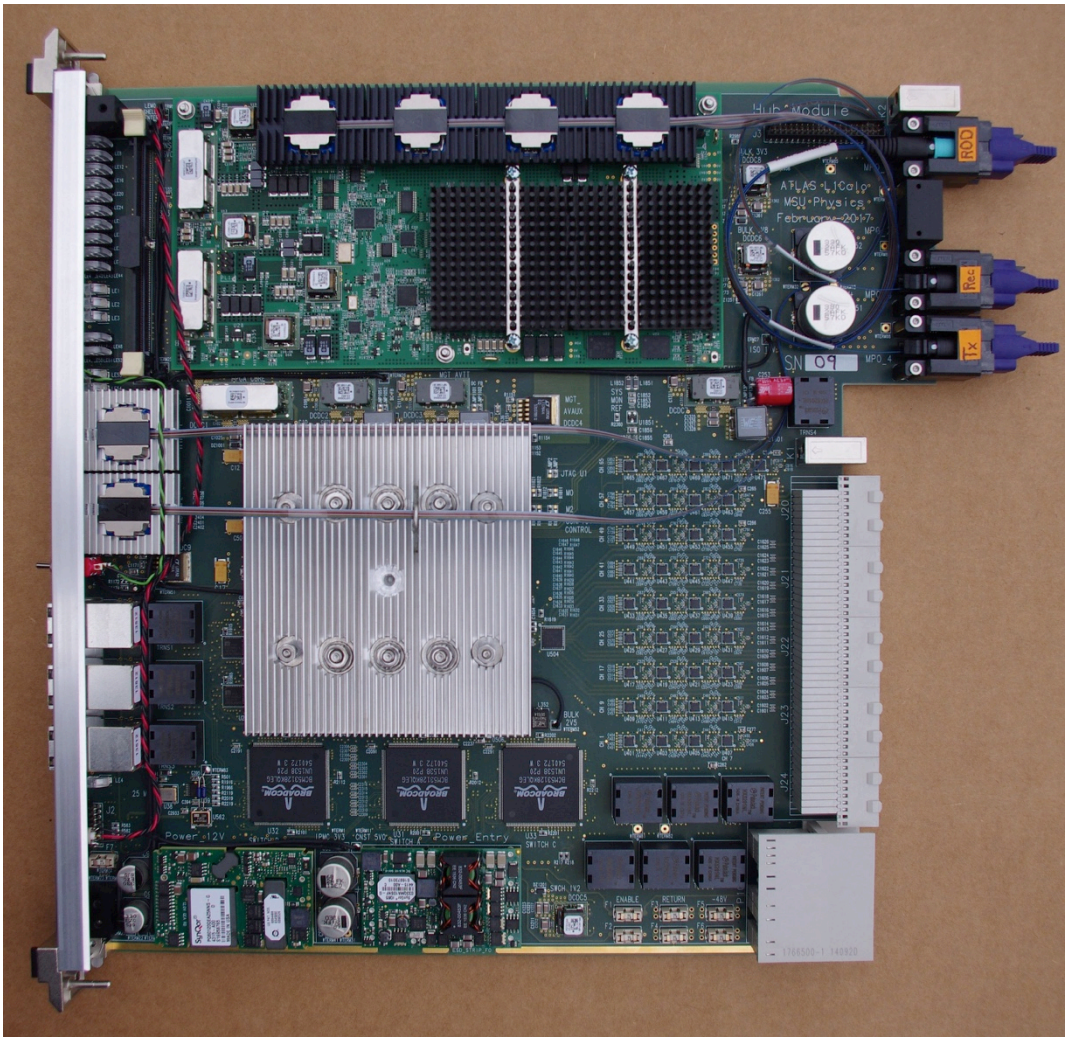


Figure 12: Prototype FEX-Hub module with ROD mezzanine mounted, as viewed from the front of the module.

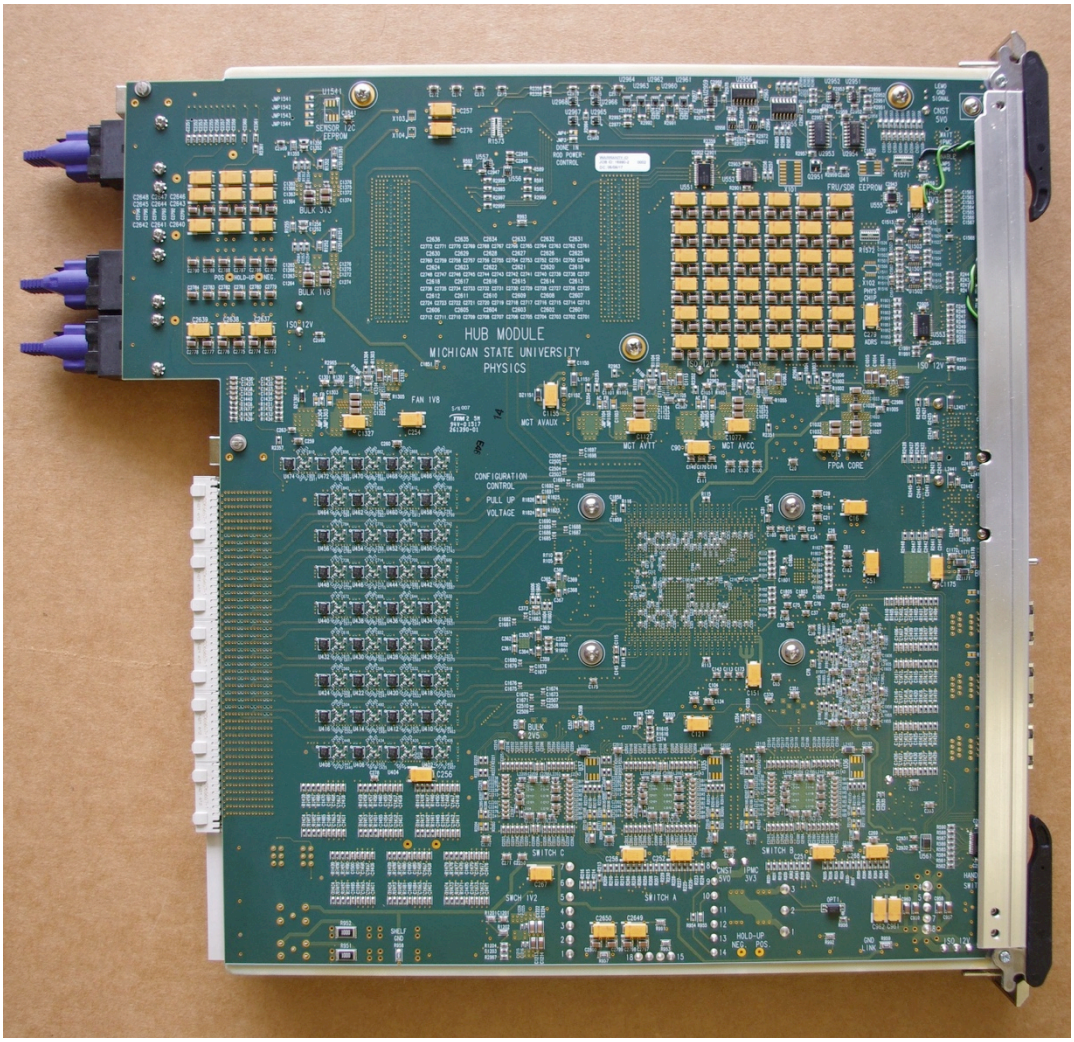


Figure 13: Prototype FEX-Hub module, as viewed from the back of the module.

6.1 Physical Layout

The FEX-Hub module is implemented as a size 6 HP ATCA card, with the L1Calo-specified bump-out in Zone 3 to accommodate the L1Calo RTM. An annotated illustration of the physical layout can be found in **Figure 5**.

The Hub holds the ROD mezzanine card. The ROD is located near the top edge of the Hub and runs from the Hub's front panel edge for 200 mm towards the Hub's backplane edge. In the direction along the front panel the ROD runs for 100 mm.

The Hub and ROD are electrically connected by two 400 pin MEG-Array connectors. A short 4mm stack height is used so that the Hub and ROD PCBs are quite close to each other. The component sides of the Hub and ROD both face in the same direction. The intent is to keep the path of the high-speed differential signals from the Hub to the ROD

as short as possible and to give the maximum available height for the MiniPODs and other components on the ROD.

The Hub and ROD are mechanically connected to each other using standoffs. The Hub holds the fiber-optic pig-tail cables and connectors that run from Zone 3 on the Hub to the MiniPOD devices on the ROD.

The primary components on the Hub card are a Xilinx Ultrascale FPGA, three Broadcom GbE switches (with associated PHY chips and RJ45 connectors), 74 ON-Semi 1:2 fanout chips.

The Hub includes heat sinks for its FPGA, and for it MiniPODs. Along its backplane edge the FEX-Hub uses the Zone 1 P10 connector, the full complement of Zone 2 connectors (J20 through J24), and 4 MPO connectors in Zone 3.

6.2 Readout Signal Distribution

The FEX-Hub receives readout data on 6 channels of the Fabric Interface from each of the 12 node slots in the shelf. This is 72 channels of high-speed readout data from the FEX node slots. In addition the Ultrascale FPGA on the other FEX-Hub provides 2 Fabric Interface channels of readout data. This makes a total of 74 channels of readout data from other slots in the shelf. The FPGA on the FEX-Hub holding the ROD also provides 2 GTH channels of readout data. Thus a total of 74 GTH receivers on the ROD are required to field the readout data from all sources in the shelf.

The readout data from the backplane is received by the Hub with On-Semi 2-way fan-out chips that have built-in termination.

One output from these fan-out chips runs to 74 MGT inputs on the FEX-Hub's Ultrascale FPGA. The other output from these fan-out chips is routed through the 2 Meg-Array connectors to the ROD mezzanine card.

The pinout of the Meg-Array connectors to the ROD has been designed to provide optimum signal fidelity for these high-speed differential signals. The intent is to provide a clean, uniform, and short route for the traces on the ROD that connect the Meg-Array pins to its GTH transceiver inputs. On the ROD the Meg-Array connectors are located adjacent to the edges of its Ultrascale FPGA that hold the MGT transceivers.

Additional details can be found in the technical appendices (Section 15).

6.3 Timing and Trigger Control Distribution

In normal operation Hub #1 uses a MiniPOD to receive an optical link from FELIX that contains the LHC Reference Clock and the TTC Data Stream. Logic in the Hub's FPGA

separates the LHC Reference Clock from this composite signal and sends it to the reference input of a 40.0787 MHz quartz crystal based Phase Locked Loop. The composite control information is combined with data flow control signals from the two ROD modules in the shelf.

The FEX-Hub distributes the TTC Clock and the TCC Data Stream to 15 different objects that use these signals. The objects that use these TTC signals are: 12 ATCA Node Slots, the ROD mezzanine card on this Hub, this Hub's own Ultrascale FPGA, and finally distribution of these TTC signals to the other Hub module.

6.3.1 Clock Distribution

Distribution of the TTC Clock by the Hub is purely by fan-out. Note that the Hub will provide a 40.08 MHz clock signal even when it is not receiving a composite TTC input signal.

The specified "pull range" of of this PLL is +- 40 ppm minimum which gives them an operating range of 40.077097 MHz to 40.080303 MHz. This operating range covers all conditions of operating temperature, supply voltage, and aging. The operating range of these PLLs is wider than the frequency range specified in FELIX Requirement 2.3.5: "The FE systems shall operate in the BC clock frequency range 40.078886 MHz to 40.078973 MHz during proton runs (at 6.5 TeV) and in the range 40.078422 MHz to 40.078970 MHz during heavy ion runs (at 6.5 TeV)".

The clean output of the Hub's 40.0787 MHz PLL is fanned out to the following loads:

- as an AC coupled LVDS reference clock to the ROD on this Hub,
- as a logic clock to the FPGA on this Hub,
- as a reference clock to the 320.6296 MHz PLL on this Hub,
- as an AC coupled LVDS reference clock over the backplane to the Hub Module #2 in this shelf,
- as an AC coupled LVDS reference clock over the backplane to the 12 FEX cards in this shelf

In normal operation Hub Module #2 receives its reference clock over the backplane just like the 12 FEX cards. Hub Module #2 does not receive an optical link from FELIX with the LHC Reference Clock. In Hub Module #2 the backplane reference clock is sent to the reference input of its 40.0787 MHz PLL. From there the clean 40 MHz clock signal is fanned out to the following loads:

- as an AC coupled LVDS reference clock to the ROD on this Hub,

- as a logic clock to the FPGA on this Hub,
- as a reference clock to the 320.6296 MHz PLL on this Hub

6.3.2 Control Signal Distribution

Distribution of the TTC Data Stream by the Hub is more complicated than what's required for the clock signal. As shown in the TTC Distribution drawing the TTC Data Stream is mixed with the "back data" coming from both the ROD on Hub-1 and the ROD on Hub-2. A small part of the logic available in the Hub-1 Virtex FPGA is used to combine these 3 data streams.

Fabric Interface Channels are used to carry the TTC Clock and the combined Data Stream from Hub-1 to the Node Slots and from Hub-1 to Hub-2. When the Hubs are used this way all Node slots receive both their TTC Clock and the combined Data Stream from the Fabric Interface channels to Hub-1. Note that the PCB traces on both Hubs are the same so that distribution of TTC Data combined with back data from the ROD on Hub-1 on one set of Fabric channels while separately distributing TTC Data combined with back data from the ROD on Hub-2 on another set of Fabric channels is possible.

We assume that extraction of the information that a given object requires from the combined TTC plus ROD Data Stream will be performed by FPGA firmware in that object. Further we assume that all objects will receive the combined Data Stream using a MGT Transceiver.

As noted the Hub module that holds receives the TTC signal will distribute the TTC Clock and combined Data Stream signals to the other Hub. This connection is necessary to supply these signals to the ROD and Ultrascale FPGA on the other Hub. The physical path to carry these signals from the Hub that receives the FELIX TTC signal to the other Hub is a pair of Fabric Interface channels that run between the Hubs.

Note that only the Fabric Interface channels from the Hub that receives the TTC signals from FELIX are actually active. The TTC Fabric Interface channels from the other Hub (Hub-2) are tied Low by that Hub.

6.4 Base Interface Switch

Each FEX-Hub provides a 10/100/1000 Base-T Ethernet switch with 19 ports that are connected to the following:

- 1 connection to the front panel i.e. the "up-link";
- 1 connection to the ROD (or IPMC) on this Hub;

- 1 connection to the ROD (or IPMC) on the other Hub;
- 1 connection to this Hub's Virtex FPGA;
- 1 connection to the other Hub's Virtex FPGA;
- 1 connection to the Shelf Manager;
- 1 spare front panel connection;
- 12 connections to the "Node" boards in this shelf.

This Hub switch is implemented using 3 Broadcom BCM53118 devices. These 8 port switches include the PHY interface to the BASE-T network connections. Besides providing the advantage of build in PHY interface the BCM53118 can be operated as either a simple unmanaged switch or if managed it can provide advanced switch features. The intent is to provide a prototype Hub switch that is easy for everyone to use but that has advanced features available via remote management if needed.

The prototype Hub module has 6 RJ45 Ethernet connectors on its front panel: 4 connectors to its switch, one to the Hub ROD and one to the Hub IPMC. The 4 switch connections are normally used for: the up-link to the external network, two ports for connections to either both Hub RODs or both Hub IPMCs (depending on whether this is Hub-1 or Hub-2), and a spare front panel Ethernet connection.

The point of having these connections accessible via front panel RJ45 connectors is to make the prototype Hub easy to uses in various test setups where either one or two Hubs may be used. The RJ45 connections to the Hub also allow the switch to be tested without any other ATCA cards in the system.

6.5 Hub FPGA

The main Hub FPGA is a large Xilinx Ultrascale device: the XCVU125-1FLVC2104I.

This is speed grade “1”, i.e. the normal common slowest speed grade and it is the “Industrial” temperature range which is the common temp range for most of these UltraScale parts.

This part has: 40 GTH Transceivers and 40 GTY Transceivers. These are spread across 2 Super Logic Regions (SLRs) with 20 of each kind of transceiver in each SLR.

This part has 7 HP Select I/O Banks with 52 I/O signals in each. 4 of the HP banks are in SLR #0 and 3 of the HP banks are in SLR #1.

This part also has 2 HR Select I/O Banks with 26 I/O signals in each. Both of the HR banks are in SLR #0. The Hub Module uses both of the HR Banks for 3V3 I/O and it uses most of the signals in these Banks.

More details are available in the technical description of the Hub FPGA implementation.

6.6 The IPM Controller

For the purposes of monitoring and controlling the power, cooling and interconnections of a module, the ATCA specification defines a low-level hardware management service based on the Intelligent Platform Management Interface standard (IPMI). The Intelligent Platform Management (IPM) Controller is that portion of a module (in this case, the FEX-Hub) that provides the local interface to the shelf manager via the IPMI bus. It is responsible for the following functions:

- interfacing to the shelf manager via dual, redundant Intelligent Platform Management Buses (IPMBs); it receives messages on all enabled IPMBs and alternates transmissions on all enabled IPMBs;
- negotiating the Hub power budget with the shelf manager and powering the Payload hardware only once this is completed;
- managing the operational state of the Hub, handling activations and deactivations, hot-swap events and failure modes;
- implementing electronic keying, enabling only those backplane interconnects that are compatible with other modules in shelf, as directed by shelf manager;
- providing to the Shelf Manager hardware information, such as the module serial number and the capabilities of each port on backplane;
- collecting, via an I2C bus, data on voltages and temperatures from sensors on the Hub, and sending these data, via IPBus, to the main Hub FPGA;
- driving the BLUE LED, LED1, LED2 and LED3.

The Hub uses the IPMC mezzanine produced by LAPP as the IPM Controller [1.9] . The form factor of this mezzanine is DDR3 VLP Mini-DIMM.

6.7 Power Supplies and Management

The power design and power management on the FEX-Hub conform to the full ATCA PICMG® specification (issue 3.0, revision 3.0). Details of the FEX-Hub power system are given in Section 28, and a summary description is provided here.

A SynQor IQ65033QMA10SNF-G (10A, 300W) power entry module provides -48V dual redundant input power distribution and 3.3V/5.0V isolated management power for IPMC and its auxiliary circuitry. From the power entry module filtered power, monitored by the IPMC, flows to the input of an Isolated +12 Volt converter. This converter makes the Isolated +12 Volt power that operates everything on the Hub Module except for the power supervision circuits and the IPMC mezzanine card. The Isolated +12 Volt power is provided by a SynQor PQ60120QEA25NNS-G 12V 25A 300 Watt quarter-brick module. Higher current modules are available if needed.

By default, on power up, the management power for the IMPC is on. The payload power is disabled by the IPMC until it has successfully negotiated power-up rights with the ATCA Shelf Manager. To enable bench-top diagnosis, a toggle switch is provided to bypass the IPMC. This switch will be disabled for the FEX-Hub modules when they are ready for installation.

Details of the Hub power configuration and management can be found in the technical appendices, Section 28.

The total power consumption of the FEX-Hub is estimated to be approximately 65W, measured using a FPGA configuration that enables all MGTs operating at their maximum anticipated line rates. Thus, this estimate does not account for any future power consumption by algorithms running in the Hub FPGA fabric.

6.8 Thermal Management

The ATLAS-standard ATCA shelf uses vertical airflow with water chillers sandwiched between shelves. The cooling capacity in ATLAS Point 1 is 400W per slot (front space), which is well above the estimated FEX-Hub power consumption. A high thermal-conductivity aluminium heat-sinks is used for the main FPGA, and heat sinks are fitted for the MiniPOD electro-optical transceivers (if fitted). Finally, the ROD mezzanine is allocated 100W of the total cooling budget, and will manage/monitor the temperature of its FPGA and MiniPODs.

6.9 Front-Panel Layout

The FEX-Hub includes an extruded aluminum ATCA front panel with an EMC gasket. The front panel insertion extraction handles actuate a PCB mounted micro-switch for the hot-swap function.

Penetrations through the front panel include those for the standard ATCA LEDs, those for the RJ45 Ethernet connections, LEDs for each of the Hub GbE links to the ROD and backplane, JTAG connection, a LEMO connection to the ROD, five that are required for the ROD mezzanine card and three spare (functions so far unspecified) Hub specific

LEDs. Further, the prototype Hub module has a front-panel toggle switch to control the power-on sequence, which will be removed for the production Hub modules.

The Hub prototype module front panel silk screen is shown in **Figure 14**.

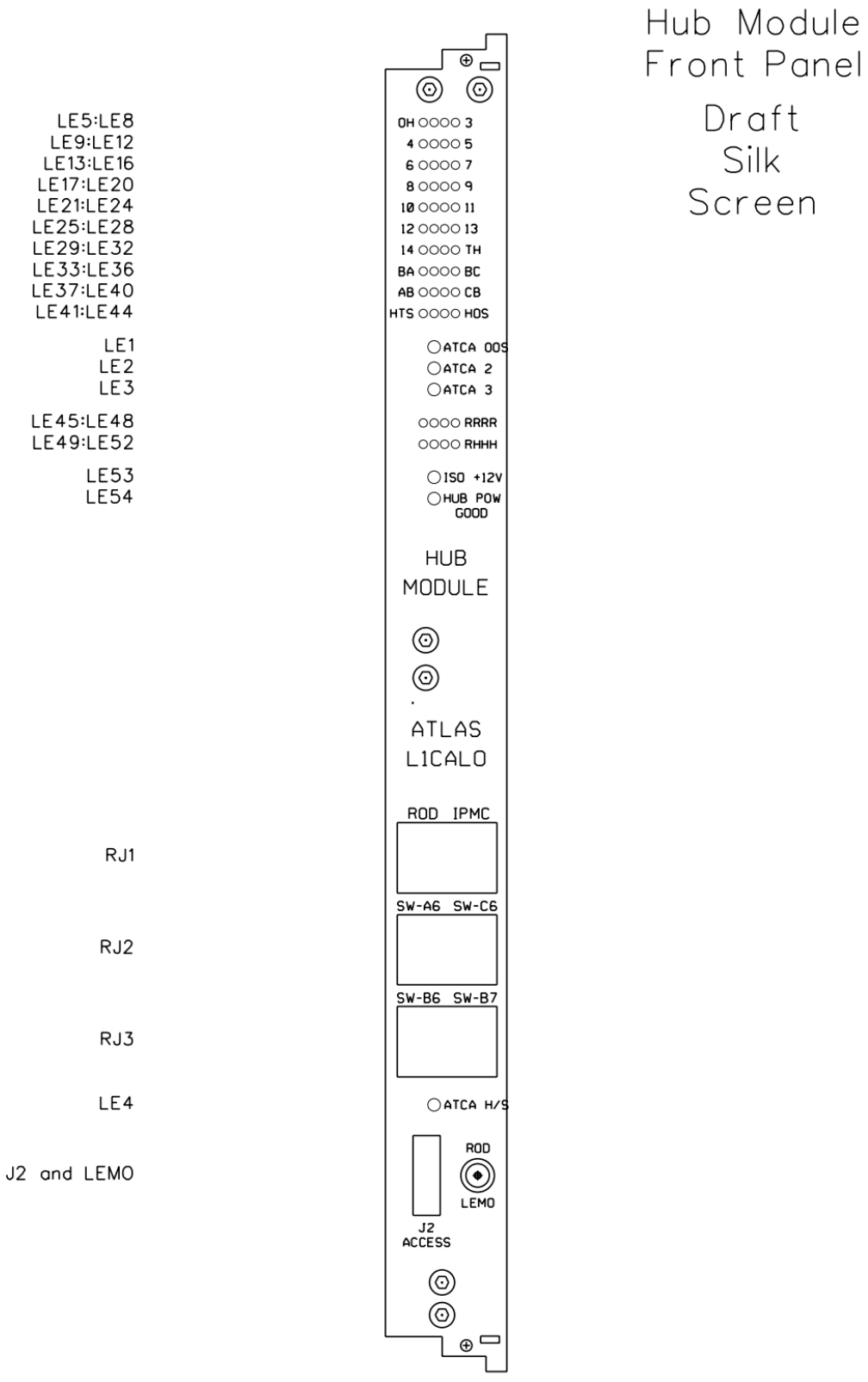


Figure 14: Hub prototype front panel silk screen.

Switch port to OtherHub		Switch port to FEX 3	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #5	LED #6	LED #7	LED #8
Switch port to FEX 4		Switch port to FEX 5	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #9	LED #10	LED #11	LED #12
Switch port to FEX 6		Switch port to FEX 7	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #13	LED #14	LED #15	LED #16
Switch port to FEX 8		Switch port to FEX 9	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #17	LED #18	LED #19	LED #20
Switch port to FEX 10		Switch port to FEX 11	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #21	LED #22	LED #23	LED #24
Switch port to FEX 12		Switch port to FEX 13	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #25	LED #26	LED #27	LED #28
Switch port to FEX 14		Switch port Hub FPGA	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #29	LED #30	LED #31	LED #32
Switch B port 2 (to A)		Switch B port 3 (to C)	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #33	LED #34	LED #35	LED #36
Switch A port 7 (to B)		Switch C port 7 (to B)	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #37	LED #38	LED #39	LED #40
Hub FPGA Phys Chip conx to this Hub's Switch		Hub FPGA Phys Chip conx to other Hub's Switch	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #41	LED #42	LED #43	LED #44

ATCA Mandatory: Failure (IPMC Socket pin #104)
Red
LED #1

ATCA Optional: TBD (IPMC Socket pin #105)
Green
LED #2

ATCA Optional: TBD (IPMC Socket pin #106)
Red
LED #3

Driven by ROD FPGA			
ConfigDone	PowerGood	SMB_Alert	GP
Green	Green	Red	Blue
LED #45	LED #46	LED #47	LED #48
From ROD	Driven by Hub FPGA		
Run	TBD	TBD	TBD
Blue	Green	Yellow	Red
LED #49	LED #50	LED #51	LED #52

Hub Module Isolated +12V present
green
LED #53

Hub Module Power Good
green
LED #54

RJ1 left/lower ROD Mezzanine		RJ1 right/upper IPMC, but no LED signal from PHY made available	
Link	Activity	green	yellow
green	yellow	LED #55	LED #56
LED #57	LED #58		
RJ2 left/lower Switch A Port 6		RJ2 right/upper Switch C Port 6	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #61	LED #62	LED #59	LED #60
RJ3 left/lower Switch B Port 6		RJ3 right/upper Switch B Port 7	
Link	Activity	Link	Activity
green	yellow	green	yellow
LED #65	LED #66	LED #63	LED #64

ATCA Mandatory: Hot Swap (IPMC Socket pin #103)
Blue
LED #4

Figure 15: Description of Hub front panel LED definitions.

6.9.1 Front Panel LEDs

A description of the LED definitions is given in **Figure 15**. Further details of the Hub LEDs are given in the technical specification Appendix, **Section 24**.

6.10 Rear Inputs and Outputs

6.10.1 ATCA Zone 1

This interface is configured according to the ATCA standard. The connections include

- dual, redundant -48V power supplies,
- hardware address,
- IPMB ports A and B (to the ATCA Shelf Manager),
- shelf ground,
- logic ground.

See the ATCA specification for further details [1.7] .

6.10.2 ATCA Zone 2

All Zone 2 connections are described in detail in Section 5 and the technical appendices (Sections 15, 0 and 17). These include:

- Eight Fabric Interface channels to each node slot:
  - One copy of the 40.08 MHz LHC clock (Hub Tx),
  - One copy of the combined TTC/Hub-ROD1_CTRL high-speed serial link (Hub Tx),
  - Six lanes of high-speed FEX readout data serial links (Hub Rx)
- Gigabit Ethernet links in the Base Interface to/from each node slot.

6.10.3 ATCA Zone 3

The ATCA Zone 3 houses four Molex MTP backplane connectors, which will connect directly to the L1Calo Rear Transition Module (RTM). Note that, here the FEX-Hub violates the standard ATCA form factor, in that the front board protrudes through Zone 3 into the rear space of the ATCA shelf. All L1Calo ATCA modules conform to this modified standard [1.14] .

6.11 FEX-Hub PCB

Figure 5 illustrates the layout of the main components on the FEX-Hub. **Figure 17**, **Figure 18** and **Figure 19** illustrate the Gigabit Ethernet switch implementation, the core TTC distribution and high-speed data distribution on the Hub module, respectively. The remainder of this section describes the PCB layout of the Hub module.

The Hub printed circuit board is a standard size ATCA card with the RAL specified "bump out" in the Zone 3 area to accommodate up to 4 MPT optical connectors for use with a Rear Transition Module.

There are 22 copper are in the Hub PCB, used in the following way:

PCB Layer	Layer Type Function	Controlled Impedance
1	Signal Traces	100 Ohm Diff
2	Ground Plane Upper Type	
3	Signal Traces	100 Ohm Diff
4	Ground Plane Upper Type	
5	Signal Traces	100 Ohm Diff
6	Ground Plane Upper Type	
7	Signal Traces	100 Ohm Diff
8	Ground Plane Middle Type	
9	Power Fills and Signals	100 Ohm Diff
10	Ground Plane	Middle Type
11	Power Fills	
12	Power Fills	
13	Ground Plane	Middle Type
14	Power Fills and Signals	100 Ohm Diff
15	Ground Plane Middle Type	
16	Signal Traces	100 Ohm Diff
17	Ground Plane	Lower Type
18	Signal Traces	100 Ohm Diff
19	Ground Plane Lower Type	
20	Signal Traces	100 Ohm Diff
21	Ground Plane Lower Type	
22	Signal Traces	100 Ohm Diff

The stack-up of the Hub card is shown in **Figure 16**.

Layer	Calc Thickness	Primary Stack	Description	Dk / Df
	0.0127		Taiyo 4000-BN	3.90 / 0.0330
Layer - 1	0.0508		**1/2oz Sig (Std Plt)**	
	0.0965	1080HRC	FR408HR	3.42 / 0.0098
Layer - 2	0.0152		**1/2oz P/G**	
	0.1270	0.0050 (1-2116)	FR408HR	3.77 / 0.0089
Layer - 3	0.0152		**1/2oz Sig**	
	0.1422	1080 1080	FR408HR	3.44 / 0.0098
Layer - 4	0.0152		**1/2oz P/G**	
	0.1270	0.0050 (1-2116)	FR408HR	3.77 / 0.0089
Layer - 5	0.0152		**1/2oz Sig**	
	0.1422	1080 1080	FR408HR	3.44 / 0.0098
Layer - 6	0.0152		**1/2oz P/G**	
	0.1270	0.0050 (1-2116)	FR408HR	3.77 / 0.0089
Layer - 7	0.0152		**1/2oz Sig**	
	0.1422	1080 1080	FR408HR	3.44 / 0.0098
Layer - 8	0.0152		**1/2oz P/G**	
	0.1270	0.0050 (1-2116)	FR408HR	3.77 / 0.0089
Layer - 9	0.0305		**1oz Mix**	
	0.1397	1080 1080	FR408HR	3.44 / 0.0098
Layer - 10	0.0152		**1/2oz P/G**	
	0.0762	0.0030 (1-1080)	FR408HR	3.48 / 0.0096
Layer - 11	0.0305		**1oz Mix**	
	0.0813	106 106	FR408HR	3.24 / 0.0106
Layer - 12	0.0305		**1oz Mix**	
	0.0762	0.0030 (1-1080)	FR408HR	3.48 / 0.0096
Layer - 13	0.0152		**1/2oz P/G**	
	0.1397	1080 1080	FR408HR	3.44 / 0.0098
Layer - 14	0.0305		**1oz Mix**	
	0.1270	0.0050 (1-2116)	FR408HR	3.77 / 0.0089
Layer - 15	0.0152		**1/2oz P/G**	
	0.1422	1080 1080	FR408HR	3.44 / 0.0098
Layer - 16	0.0152		**1/2oz Sig**	
	0.1270	0.0050 (1-2116)	FR408HR	3.77 / 0.0089
Layer - 17	0.0152		**1/2oz P/G**	
	0.1422	1080 1080	FR408HR	3.44 / 0.0098
Layer - 18	0.0152		**1/2oz Sig**	
	0.1270	0.0050 (1-2116)	FR408HR	3.77 / 0.0089
Layer - 19	0.0152		**1/2oz P/G**	
	0.1422	1080 1080	FR408HR	3.44 / 0.0098

Figure 16: Hub PCB stackup details.

The Hub PCB includes 10 ground planes that are needed to facilitate routing of the high-speed differential signals. The 3 different ground plane patterns are needed to allow relief of the ground plane layers that are immediately under the AC coupling capacitors that are used in most of these high-speed differential signals. These 0201 size AC coupling capacitors are needed on both sides of the PCB and relief of the ground planes immediately under their pads minimizes the transmission line impedance bump caused by these capacitors.

In the layers with high speed differential traces the dielectric layers are kept thick enough so that the 100 Ohm traces do not become so narrow that their losses are too high. This results in card with an overall thickness of 3.0 mm. From the backside of the card, in a narrow strip along the top and bottom edges, the thickness of the card is milled down to 2.4 mm so that it fits into standard ATCA card guides.

The layout of the Hub PCB requires routing of 384 high-speed differential pairs. The main complication in this high speed routing is at the output of the 74 Channel FEX Readout Data MGT Fanout where all of the signals routing up to the ROD must cross over those routing to the Hub FPGA. This crossover is done without any layer changes by having all MGT differential pairs running to the ROD located in layers 14, 16, 18, 20 and all MGT differential pairs routing to the Hub FPGA located in layers 3, 5, 7, 9. Layer transitions in the high speed signals are only used where these signals come to the surface to connect to a component such as the Hub FPGA or the AC coupling capacitors.

These required high speed layer transitions are implemented with a 4 via component that provides 2 ground current return vias along with the differential via pair. The ground planes are relieved in an oval pattern around the differential via pair to maintain a constant transmission line impedance All high speed trace pairs are length matched to 0.5 mm using serpentines. All vias and Zone 2 backplane connector pin holes in the high speed traces have been back-drilled to remove the via stubs. 7 back-drill depths are used from the bottom side of the card and 4 back-drill depths are used from the top side.

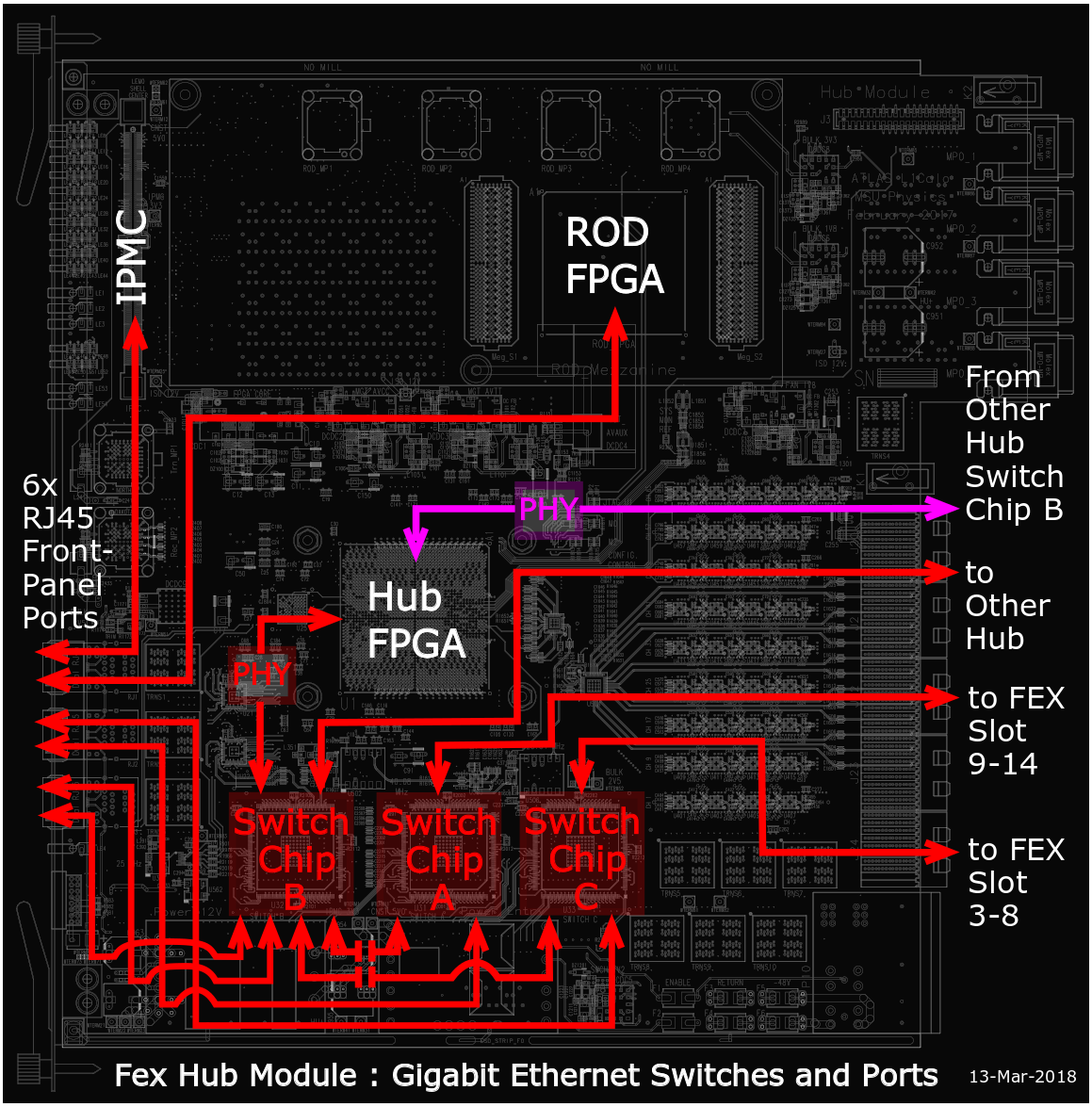
The Hub PCB is built with Isola FR408HR laminate which is a low dielectric loss laminate that is appropriate for 10 Gb/sec digital routing. This is a high transition temperature laminate to facilitate assembly of the Hub Modules with a lead free process.

The Hub design includes many components that use a center Exposed Pad that is soldered to a grounded thermal land for cooling. These thermal lands include an array of vias that connect them to the internal ground planes to help carry heat away from the associated component. To prevent wicking of solder into these vias (which would cause a poor solder connection to the associated component) hole plugs have been used in all thermal land via arrays on both the top and bottom sides of the Hub PCB.

The Hub design uses 10 main power buses. There are not enough layers available to route each power bus on its own PCB layer. Instead 58 power area fills on 5 different layers are used to route the power buses on the Hub card.

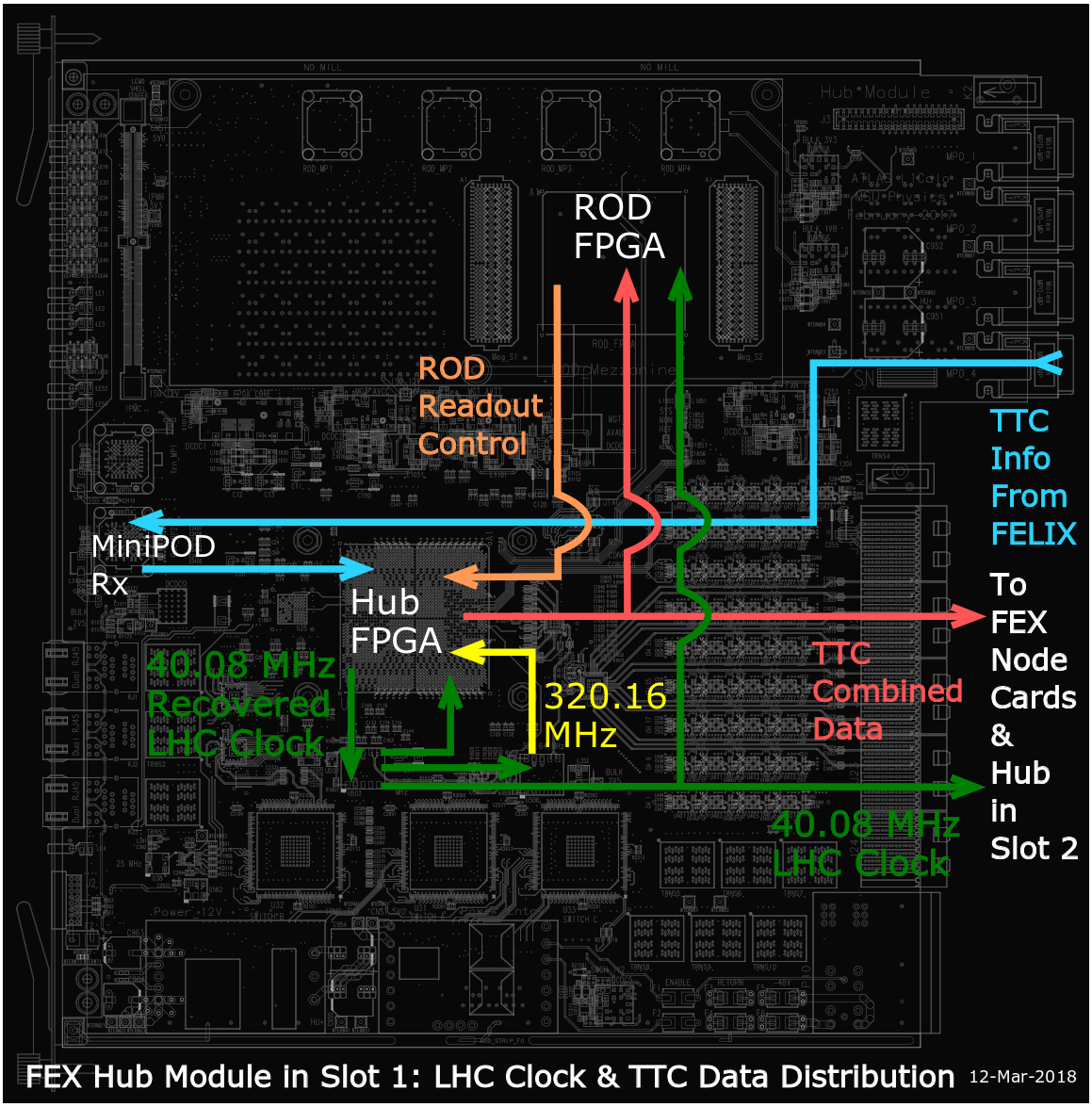
The Hub PCB has 9162 drill through holes of 20 different hole types. All drills are through all layers. Blind vias are not used.

The bare Hub PCB is manufactured with a gold surface finish to provide an optimum solder re-flow process during assembly.



1089

1090 **Figure 17:** Board-level illustration of the Hub's Gigabit Ethernet switch connections.



1091

1092 **Figure 18:** Board-level illustration of the Hub's LHC clock and TTC data distribution.

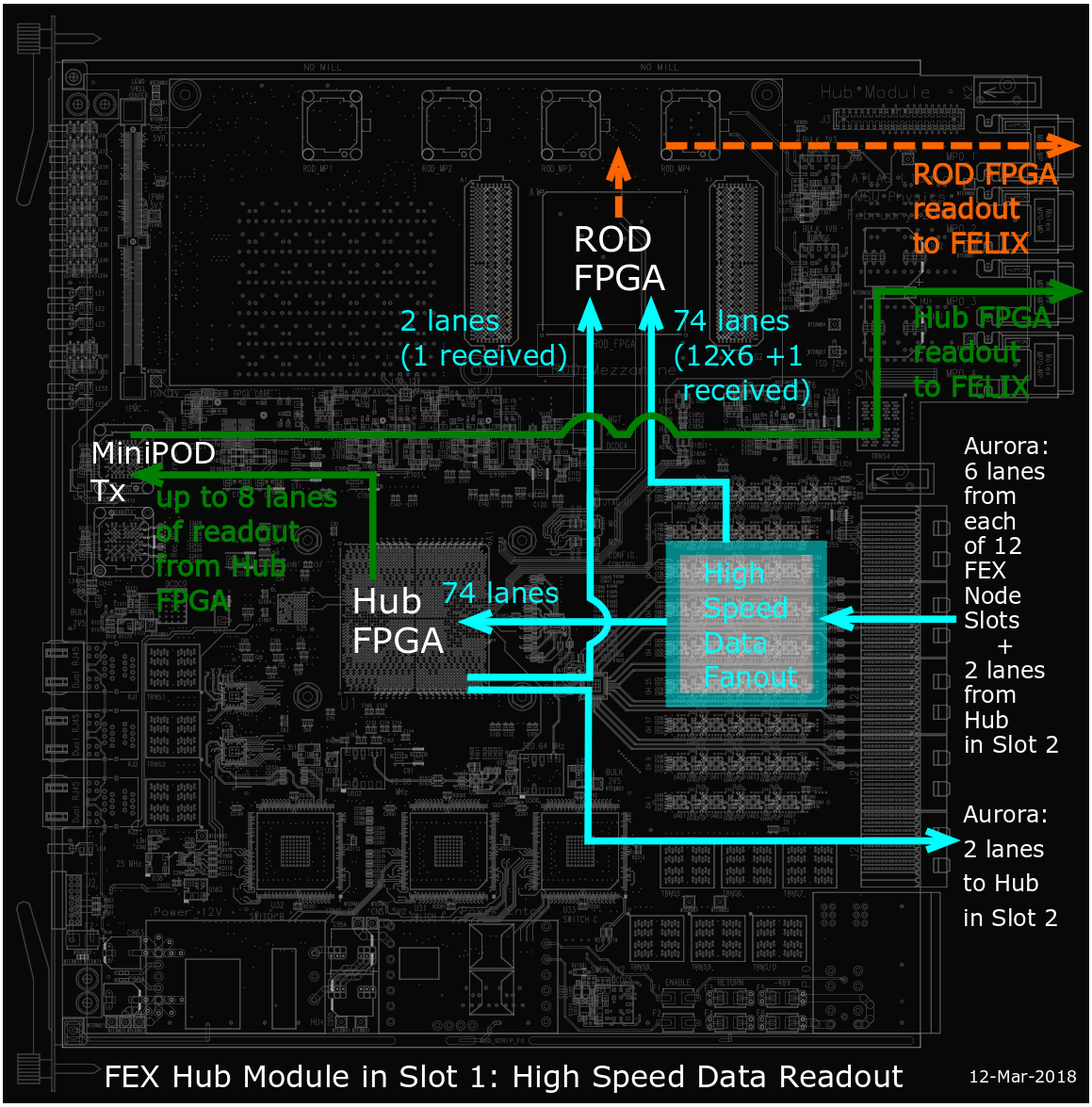


Figure 19: Board-level illustration of the high-speed data interfaces for the Hub.

7 Programming Model

The Programming model is preliminary, and is expected to change significantly during detailed design.

7.1 Guidelines

The slow-control interface of the FEX-Hub obeys the following rules.

- The system controller can read all registers; there are no ‘write only’ registers.
- Three types of register are defined: Status Registers, Control Registers and Pulse Registers.
- All Status Registers are read-only registers. Their contents can be modified only by the Hub hardware.
- All Control Registers are read/write registers. Their contents can be modified only by system controller. Reading a Control Register returns the last value written to that register.
- All Pulse Registers are read/write registers. Writing to them generates a pulse for those bits asserted. Reading them returns all bits as zero.
- Attempts to write to read-only registers, or undefined portions of registers, result in the non-modifiable fields being left unchanged.
- If the computer reads a register (e.g. a counter) which the Hub is modifying, a well-defined value is returned.
- The power-up condition of all registers bits is zero, unless otherwise stated.

7.2 Register Map & Controllable Functions

The register map and the controllable functions are described in the Hub firmware specification [1.16] .

8 Testing and Commissioning

The testing and commissioning of the FEX-Hub module will be performed in two modes: (1) standalone as a single module in an ATCA shelf, (2) together with FEX (or test module) and ROD modules to test core FEX system functionality. Both of these testing phases can be performed with either one or two Hubs per shelf.

There insufficient test modules capable of sourcing data in the ATCA backplane available in the L1Calo prototype phase to fully populate all 12 node slots, thus the current FEX-Hub design has not been tested with a full shelf of source nodes. Thus, a bandwidth test following the Final Design review will be performed prior to the Production Readiness Review.

A detailed list of commissioning tests for the production FEX-Hub module is presented in Appendix **Section 32**. While this list may grow to cover more in-depth testing of Hub interfaces, it is already covering all Hub functionality.

8.1 Standalone and FEX System Tests

Standalone Hub tests will be performed to verify power distribution, FPGA configuration and basic functionality of the GbE network. To facilitate the requirement of Hub-to-Hub testing, the Hub module:

- allows testing and validation of the DCS and control networks via direct connections to a second Hub module;
- allows testing and validation of the DCS and control networks via front-panel connections to external computers, allowing thorough scanning of all IPbus targets;
- allows the sending and receiving of high-speed signals from one Hub to another, providing a path to study Fabric Interface bandwidth limitations;
- allows testing and validation of the fanout of clock and TTC control data information over the Fabric Interface.

To facilitate the requirement of FEX-Hub-ROD testing, the Hub module:

- provides Fabric Interface connections to the ROD with no Hub configuration required;
- provides network switching functions with no Hub configuration required;
- provides a clock to all node slots with no Hub configuration required;
- functions as a single module without a second Hub module in the ATCA shelf;
- sees a copy of the same data delivered to the ROD module.

8.2 Full Bandwidth Tests

To facilitate testing of the FEX-HUB and ROD with a full shelf of data sources, Michigan State University has designed a Hub Test Module (HTM) for this purpose. The HTM is an ATCA carrier card hosting a commercial mezzanine with a Kinex-7 FPGA. Thus, the HTM is capable of emulating FEX modules by

- sourcing 6 lanes of multi-gigabit serial transmission lines to both Hub slots;
- receiving the Hub-sourced clock;
- receiving the combined TTC info signal from the Hub;
- connecting to both GbE networks provided via Hub slots 1 and 2.

Using a full shelf of HTM cards, the bandwidth conditions of a full FEX shelf will be tested. These tests will include a simultaneous test of:

- 6 lanes of data traffic to both Hub slots from all 12 node slots, with a goal of testing up to the maximum anticipated L1Calo bandwidth of 9.6 Gbps;
- distribution of the Hub clock to all 12 node slots;
- distribution of the Hub TTC combined info to all 12 node slots;
- full-bandwidth GbE traffic on both Hub Ethernet networks;
- full-bandwidth ROD-Hub links, including the backplane links between Hub slots;

While all of these tests can be performed individually with a single test module, this test will emulate the expected rigors of L1Calo operations over Run 3 and Run 4.

9 FEX-Hub Prototype Tests

9.1 Overview

Eight FEX-Hub prototype modules were manufactured in 2017. All of these modules have been tested, though some tests were only performed on a subset of Hub cards. Two of the prototype cards have been shipped to Cambridge, and are now part of the ROD test module bench. This section describes the test results for these prototype modules. While this section summarizes the salient details of the Hub tests, a full description of the Hub commissioning tests can be found in Section 32, which forms the production Hub commissioning plan as well.

9.2 Power and Cooling Tests

To perform power and cooling tests, all Hub MGTs were activated and running in the anticipated normal Hub configuration (Tx and Rx together). The FPGA fabric is primarily allocated to IBERT logic, but this is estimated to be a relatively small fraction of the FPGA fabric capacity.

9.2.1 Power Consumption

The two primary power draws on the Hub are the Hub FPGA, which consumes 33.4W in the configuration anticipated for L1Calo operations. The high-speed data fanout chips consume 21.8W in total. The MiniPODs, switch chips and IPMC all together consume less than 10W. The total power consumption for the Hub is found to be 67W in normal L1Calo operating conditions, which increases to 72W when operating all unconnected MGTs. The Hub supply capacity is 300W, of which 100W is reserved for the ROD.

9.2.2 MGT Rail Power Supply Capacity

The capacity of the Hub MGT rail power supplies were a significant concern for the prototype design, as a safety margin of 40% in DCDC supply capacity was desired for the all MGT rail supplies. This concern was driven by an apparent discrepancy between the predictions by the Xilinx Power Estimator (XPE) and measurements on Xilinx development boards, also observed by other ATLAS Xilinx users.

The current draw measurements are given in the following table. The smallest margin observed is for MGT_AVTT at 36.5%, which is a satisfactory safety margin as the design is already using all MGTs supplied by that converter.

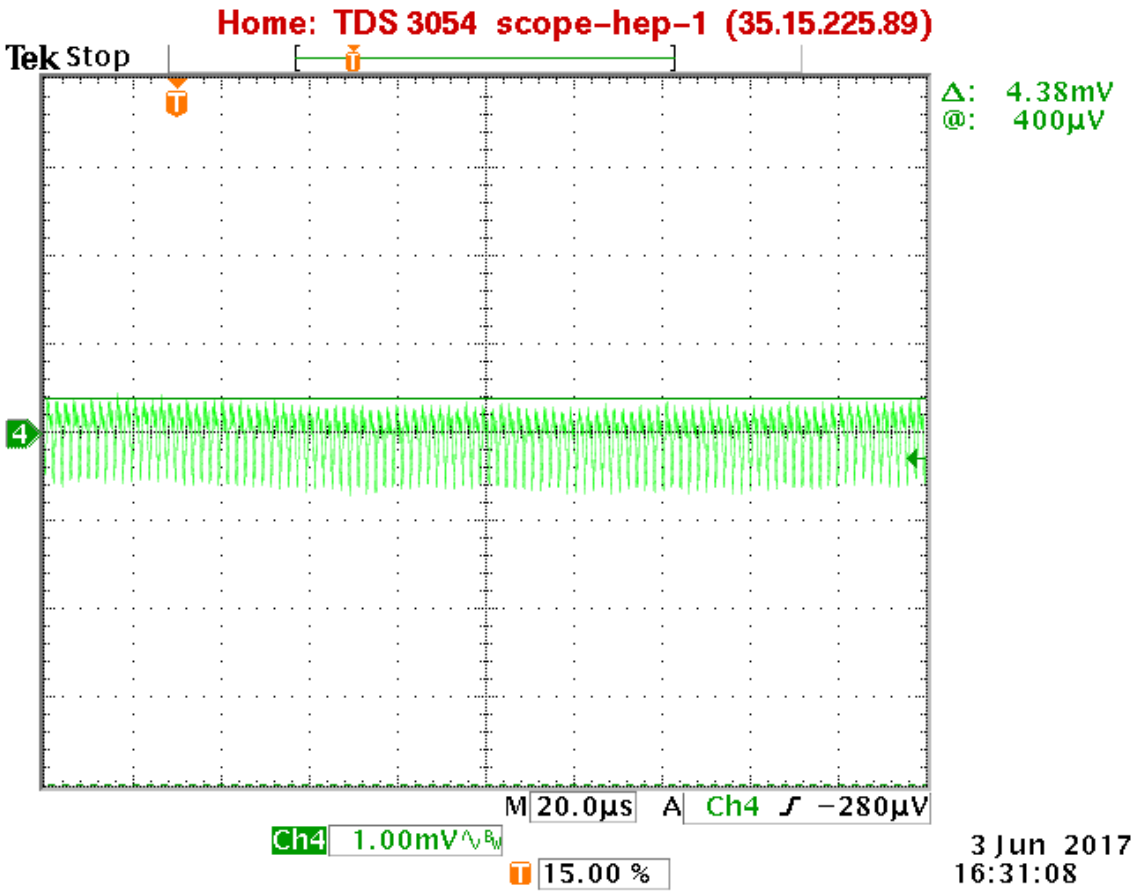
Converter	FPGA_ CORE	MGT_ AVCC	MGT_ AVTT	SWCH _1V2	BULK _1V8	FAN_ 1V8	BULK_ 3V3
Voltage	0.95 V	1.00 V	1.20 V	1.20 V	1.80 V	1.80 V	3.3 V
Draw	8.04 A	9.38 A	12.7 A	1.94 A	0.62 A	12.1 A	2.25 A
Capacity	40 A	20 A	20 A	12 A	12 A	20 A	12 A

In this configuration the FPGA is consuming 33.4W. It should be noted that we do not have direct access to the 1V8 MGT_AVAUX and 1V3 BULK_2V5 buses, but these are included in the BULK_3V3 current.

9.2.3 MGT Rail Supply Noise

The Xilinx FPGAs and ON-Semi fanout chips specify a noise tolerance for the MGT rail supplies, typically smaller than 10 mV pk-pk. Both GE (Lineage Power) D-Lynx series and TI (Power Trends) PTH08Txyz series converters were evaluated for use on the Hub Module, which both advertise noise characteristics compatible with the Hub requirements. The D-Lynx converters were selected, primarily for the PMbus connections offered on their control chips.

All supplies on the Hub prototype have been tested and fall well within the noise tolerance required. An example measurement is shown in **Figure 20** for the fanout 1.8V supply, obtained with all DCDC supplies running.



1218

1219 **Figure 20:** Noise measurement for the 1.8V fanout DCDC power supply.

1220 Tests of the Hub DCDC supply stability have also been performed, and their performance
1221 has been found to be satisfactory. An example is given in **Figure 21** wherein the
1222 MGT_AVTT 1.2V supply load is pulsed from 7.2A to 12A at 500 Hz.

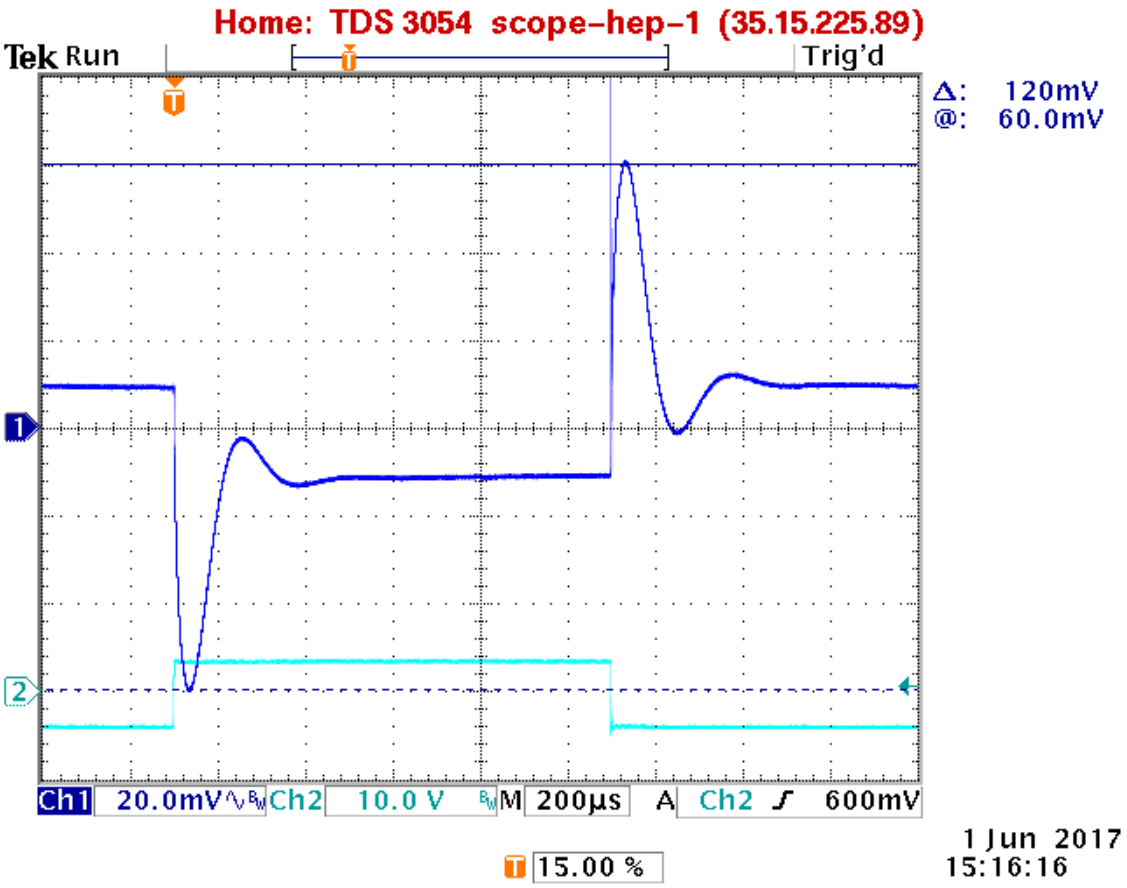


Figure 21: Stability test of the MGT_AVTT DCDC supply, obtained while pulsing the supply load from 7.2A to 12A at a 500 Hz rate.

9.2.4 FPGA Silicon Temp

The Hub FPGA silicon temperature has been measured using a full load, as described above, and with normal shelf cooling fan speeds. Measurements of FPGA silicon temperature across the Hub prototypes are typically 45C with small variance. It should be noted that the usage of the FPGA fabric is minimal in this test, but it is not anticipated that the Hub FPGA usage will be significant. In tests that activate all unused Hub FPGA MGTs, the power draw increases by 5W to 38W and the silicon temperature increases by 1C to 46C.

9.3 Clock Tests

9.3.1 Clock Generation and Distribution

The Hub module produces a 40.0787 MHz LHC reference clock with jitter characteristic that is OC-192 compliant (optical carrier standard for 10 Gbps transmission).

All clock distribution links have been verified at the recipient endpoint: this Hub's ROD, other Hub and all node slots using the FEX Test Module.

9.3.2 Hub PLL Relock

During testing of the Hub Modules these PLLs are checked to verify their "re-lock" frequency range, i.e. the reference frequency is initially set outside the PLL's operating range and then slowly brought within the operating range and the frequency where re-lock occurs is recorded. The re-lock test is done with the initial reference frequency set both below and above the operating range. The re-lock range of the 40.0787 MHz PLLs is typically a little over 2x the +- 40 ppm minimum specified by their manufacturer. Note that this test also verifies that the Hub Modules will automatically re-lock to the LHC Reference Clock as soon as it becomes available again after an interruption. A signal indicating the state of the 40.0787 MHz PLL (i.e. locked or not locked) is sent to the Hub's FPGA where it can be made visible in an IPBus register.

When the LHC Reference Clock frequency is slewing the phase of the output of the Hub's 40.0787 MHz PLL will shift from its normal position with respect to its reference input. When the LHC is slewing up in frequency the output phase of the PLL will fall behind its normal position. At the maximum LHC slew rate of 220 Hz/sec there is a phase shift of about 3.2 degrees in the output of the PLL. Such a shift in phase is not something special to the PLLs used on the Hub Module rather it is an inherent characteristic of the PLL architecture. Increasing the "loop bandwidth" of the PLL will reduce this phase shift and reduce the ability of the PLL to reject the jitter in its input reference clock.

9.4 High-Speed Link Tests

Tests of the electrical connectivity and stability of the Hub high-speed links have been performed. This includes:

- 4x MiniPOD receiver MGT links to the Hub FPGA (9.6 Gbps);
- 8x MiniPOD transmitter MGT links from the Hub FPGA (9.6 Gbps);
- 72x MGT links from the FEX data fanout to the Hub and ROD FPGAs (6.4 Gbps and 10.26 Gbps);
- 2x (1x) MGT links from the other Hub slot to the Hub (ROD) FPGA (9.6 Gbps);
- 2x (1x) MGT links from this Hub to the other Hub (ROD) FPGA (9.6 Gbps);
- 14x MGT links from the Hub FPGA to the FEX slots (12x), the ROD on this Hub (1x) and the other Hub (1x) (6.4 Gbps);
- 1x MGT link for ROD/Combined data from the other Hub (9.6 Gbps);
- 1x MGT link from the ROD on this Hub (9.6 Gbps);

All high-speed links were tested using the Xilinx IBERT test firmware using SRBS7 test patterns. The data source was a FEX Test Module (FTM). All tests were performed at the line rates expected to be used for L1Calo operations. However due to limitations of the FTM, some tests were not able to be performed at 9.6 Gbps and in such instances a line rate of 10.26 Gbps was used. And due to the availability of only one FTM, only a subset of links corresponding to a single node slot could be tested simultaneously.

The duration of the tests was limited by the number of Hub modules required to be tested and the availability of the FTM. Thus, all links were tested to at least a bit error rate (BER) of less than 1E-12 and a subset was tested to 1E-16. In all tests of all Hub prototype cards, zero errors were observed.

As noted in the test plan, these tests are planned to be repeated using Hub Test Modules (HTMs) in a configuration that allows all links to be tested simultaneously.

9.5 Gigabit Ethernet Tests

This is a summary of the FEX-Hub Gigabit Ethernet tests, described in more detail in [1.15] . The FEX-Hub has three interconnected 8-port Broadcom GbE switch chips (denoted A, B, C here). Switch chip B has ports connected to both the other chips, A and C. The scope of the tests performed was to evaluate that all 22 GbE switch ports maintain reliable GbE links and that the bandwidth characteristics of the FEX-Hub GbE network are desirable.

Regarding the first test aspect, verifying connectivity of the FEX-Hub GbE switch ports, all 8 of the Hub prototypes and one Hub prototype without a Ultrascale FPGA mounted were fully qualified in this test. No links were found to have connection or transmission issues.

Regarding the second test aspect, it was found that using the FEX Hub Module connections between a single client and a single server maintain a bandwidth of 935 Mbps, which is the same as that of the commercial switch. It is further found that when sending data from multiple clients to a single server, an overall bandwidth of 940 Mbps per switch is maintained. When using a single source of data into chip A and sinking via chips B or C, we further find bandwidth reliability. When multiple sources are sent into a multiple chips and sinked via a single chip, we observe that the bandwidth is split between sources, reflecting the maximum bandwidth for the single source chip. For example, when sourcing from chips A and C via a sink on chip B, we find a maximum bandwidth of 470 Mbps for chips A and B. This pattern continues as more sources are added. This behaviour is as expected for the design, and reflects what one would expect from a commercial GbE switch.

9.6 IPMC, Slow Control and Monitoring Tests

A LAPP IPMC has been used on the FEX-Hub prototypes. The basic functions such as power negotiation; Ethernet connection, LED management and hot swap have been tested successfully. For the final FEX-Hub, the LAPP IPMC may be replaced by the pin-compatible CERN IPMC.

9.7 Miscellaneous tests

All physical aspects of the Hub card have been verified: dimensions, insertion/extraction forces, ground points, control signals, I2C bus and feasibility of heat sinks. Furthermore, all front-panel features are verified: LEDs, JTAG, RJ45 jacks, and LEMO. The communication and control of all components on the card has been verified.

9.8 Conclusions

The FEX-Hub prototype modules have been systematically tested, yielding successful outcomes for all tests. Based on the results of these tests, there is no indication for changes to the Hub PCB or implementation of core functions. No tests thus far suggest that current Hub design will not satisfy the L1Calo operational requirements.

10 Planned Hub Module Production Yields

The construction of FEX-Hub modules will occur in two phases, prototype and production. The Hub modules were fabricated spring 2017. A total of eight prototype modules were produced, with delivery as follows:

- Two prototype modules for function testing at MSU;
- Two prototype modules for an integration test rig at CERN;
- One prototype module each for Rutherford and Cambridge, for eFEX and ROD testing;
- One prototype module for Argonne National Lab, for FELIX integration tests.
- One spare prototype Hub module.

A total of nineteen production Hub modules will be produced by April 2019, with delivery anticipated as:

- Eight production modules to support the L1Calo system eFEX, jFEX and L1Topo shelves at CERN (note, there are two eFEX shelves and two Hubs per shelf);
- Three spare production modules at CERN, dedicated for the L1Calo system;
- Two production modules for function testing at MSU;
- Two production modules the CERN test facility;
- Two production modules for Rutherford and Cambridge (one per institute), for eFEX and ROD testing;
- Two spare production module to be used as needed.

11 Special Notes

- The FEX-Hub module is not providing Fabric or Base Interface connections to the 2 slots that do not exist in 14-slot shelves, i.e. shelves with 2 Hub slots and only 12 Node slots.
- As shown the FEX-Hub's Base Interface switch provides a connection to only one Shelf Manager.

12 Glossary

ATCA	Advanced Telecommunications Computing Architecture (industry standard).
BC	Bunch Crossing: the period of bunch crossings in the LHC and of the clock provided to ATLAS by the TTC, 24.95 ns.
BCMUX	Bunch-crossing multiplexing: used at the input to the CPM, JEM (from Phase I) and eFEX, this is a method of time-multiplexing calorimeter data, doubling the number of trigger towers per serial link.
CMX	Common Merger Extended Module.
CP	Cluster Processor: the L1Calo subsystem comprising the CPMs.
CPM	Cluster Processor Module.
CTP	Central Trigger Processor
DAQ	Data Acquisition
DCS	Detector Control System: the ATLAS system that monitors and controls physical parameters of the sub-systems of the experiment, such as gas pressure, flow-rate, high voltage settings, low-voltage power supplies, temperatures, leakage currents, etc.
ECAL	The electromagnetic calorimeters of ATLAS, considered as a single system.
ECR	Event Counter Reset signal from the TTC, used to initiate clearing of ROD memories
eFEX	Electron Feature Extractor.
FEX	Feature Extractor, referring to either an eFEX or jFEX module or subsystem.
FIFO	A first-in, first-out memory buffer.
FPGA	Field-Programmable Gate Array.
HTM	Hub Test Module
HCAL	The hadronic calorimeters of ATLAS, considered as a single system.
IPbus	An IP-based protocol implementing register-level access over Ethernet for module control and monitoring.
IPMB	Intelligent Platform Management Bus: a standard protocol used in ATCA shelves to implement the lowest-level hardware management bus.
IPM Controller	Intelligent Platform Management Controller: in ATCA systems, that portion of a module (or other intelligent component of the system) that interfaces to the IPMB.
IPMI	Intelligent Platform Management Interface: a specification and mechanism for providing inventory management, monitoring, logging,

	and control for elements of a computer system. A component of, but not exclusive to, the ATCA standard.
JEM	Jet-Energy Module.
JEP	Jet-Energy Processor: the L1Calo subsystem comprising the JEMs.
jFEX	Jet Feature Extractor.
JTAG	A technique, defined by IEEE 1149.1, for transferring data to/from a device using a serial line that connects all relevant registers sequentially. JTAG stands for Joint Technology Assessment Group.
L0A	In Run 4, the Level-0 trigger accept signal.
L0Calo	In Run 4, the ATLAS Level-0 Calorimeter Trigger.
L1A	The Level-1 trigger accept signal.
L1Calo	The ATLAS Level-1 Calorimeter Trigger.
LHC	Large Hadron Collider.
MGT	As defined by Xilinx, this acronym stands for Multi-Gigabit Transceiver. However, it should be noted that it denotes a multi-gigabit transmitter–receiver pair.
MiniPOD	An embedded, 12-channel optical transmitter or receiver.
MPO	Multi-fibre Push-On/Pull-Off: a connector for mating two optical fibres.
PMA	Physical Media Attachment: a sub-layer of the physical layer of a network protocol.
ROD	Readout Driver.
RoI	Region of Interest: a geographical region of the experiment, limited in η and ϕ, identified by the Level-1 trigger (during Run 3) as containing candidates for Level-2 trigger objects requiring further information. In Run 4, RoIs are used in the same between the Level-0 and Level-1 triggers.
Shelf	A crate of ATCA modules.
SMA	Sub-Miniature version A: a small, coaxial RF connector.
Supercell	LAr calorimeter region formed by combining E_T from a number of cells adjacent in η and ϕ.
SLR	Super Logic Region. A single silicon die in a Xilinx Ultrascale FPGA, connected by a silicon interposer.
TOB	Trigger Object. A Compact data structure describing a trigger feature detected by a FEX module.
TTC	The LHC Timing, Trigger and Control system.
XTOB	Extended Trigger Object. A data packet passed to the readout path, contained more information about a TOB than can be accommodated on

the real-time path.

13 Document Revision History

Version	Date	Comments
0.01	16-09-14	Preliminary Draft
0.02	19-09-14	Language & grammar edits.
0.03	1-10-14	Final version for Preliminary Design Review
1.1	13-03-18	Updated version for Final Design Review

14 Appendix 1: Backplane Connector/Pin Tables

This Appendix enumerates the connector and pin connections intended for the Hub-FEX and Hub-Hub backplane links in the Fabric Interface, Base Interface and Update Interface.

In the convention presented here, the FEX numbering below presumes that the module called “FEX 01” is located in Logical Slot 3, FEX 02 in Slot 4,... and FEX 12 in Slot 14.

14.1 Connector and Signal Usage for a HUB Slot

Rev: 23-Oct-2015 same as table from PDR after updating from FEX 01..12 to official numbering FEX 03..14
Rev: 12-Mar-2018 use name "TTC Combined Data". For FEX slot: Keep only J23. Add LHC Clock & CombData from Hub 2

Connector Usage for a HUB Slot

Connect Number	Row Num	Channel	Connector Pin Pairs a b	c d	e f	g h
J20/P20	01	Clocks	CLK1A+ CLK1A-	CLK1B+ CLK1B-	CLK2A+ CLK2A-	CLK2B+ CLK2B-
			Unused signal pair	Unused signal pair	Unused signal pair	Unused signal pair
J20/P20	02	Upd Chan & Clocks	Tx4(UP)+ Tx4(UP)-	Rx4(UP)+ Rx4(UP)-	CLK3A+ CLK3A-	CLK3B+ CLK3B-
			Unused signal pair	Unused signal pair	Unused signal pair	Unused signal pair
J20/P20	03	Update Channel	Tx2(UP)+ Tx2(UP)-	Rx2(UP)+ Rx2(UP)-	Tx3(UP)+ Tx3(UP)-	Rx3(UP)+ Rx3(UP)-
			GE Pair C HUB FPGA	GE Pair C HUB Switch	GE Pair D HUB FPGA	GE Pair D HUB Switch
J20/P20	04	Update Channel	Tx0(UP)+ Tx0(UP)-	Rx0(UP)+ Rx0(UP)-	Tx1(UP)+ Tx1(UP)-	Rx1(UP)+ Rx1(UP)-
			GE Pair A HUB FPGA	GE Pair A HUB Switch	GE Pair B HUB FPGA	GE Pair B HUB Switch
J20/P20	05	Fabric Channel 15	Tx2[15]+ Tx2[15]-	Rx2[15]+ Rx2[15]-	Tx3[15]+ Tx3[15]-	Rx3[15]+ Rx3[15]-
			Unused signal pair	Unused signal pair	Unused signal pair	Unused signal pair
	06		Tx0[15]+ Tx0[15]-	Rx0[15]+ Rx0[15]-	Tx1[15]+ Tx1[15]-	Rx1[15]+ Rx1[15]-
			Unused signal pair	Unused signal pair	Unused signal pair	Unused signal pair
J20/P20	07	Fabric Channel 14	Tx2[14]+ Tx2[14]-	Rx2[14]+ Rx2[14]-	Tx3[14]+ Tx3[14]-	Rx3[14]+ Rx3[14]-
			Unused signal pair	Unused signal pair	Unused signal pair	Unused signal pair
	08		Tx0[14]+ Tx0[14]-	Rx0[14]+ Rx0[14]-	Tx1[14]+ Tx1[14]-	Rx1[14]+ Rx1[14]-
			Unused signal pair	Unused signal pair	Unused signal pair	Unused signal pair
J20/P20	09	Fabric Channel 13	Tx2[13]+ Tx2[13]-	Rx2[13]+ Rx2[13]-	Tx3[13]+ Tx3[13]-	Rx3[13]+ Rx3[13]-
			RO Str 5 from FEX 14	RO Str 3 from FEX 14	RO Str 6 from FEX 14	RO Str 4 from FEX 14
	10		Tx0[13]+ Tx0[13]-	Rx0[13]+ Rx0[13]-	Tx1[13]+ Tx1[13]-	Rx1[13]+ Rx1[13]-
			LHC Clk to FEX 14	RO Str 1 from FEX 14	TTCCombData to FEX 14	RO Str 2 from FEX 14
J21/P21	01	Fabric Channel 12	Tx2[12]+ Tx2[12]-	Rx2[12]+ Rx2[12]-	Tx3[12]+ Tx3[12]-	Rx3[12]+ Rx3[12]-
			RO Str 5 from FEX 13	RO Str 3 from FEX 13	RO Str 6 from FEX 13	RO Str 4 from FEX 13
	02		Tx0[12]+ Tx0[12]-	Rx0[12]+ Rx0[12]-	Tx1[12]+ Tx1[12]-	Rx1[12]+ Rx1[12]-
			LHC Clk to FEX 13	RO Str 1 from FEX 13	TTCCombData to FEX 13	RO Str 2 from FEX 13
J21/P21	03	Fabric Channel 11	Tx2[11]+ Tx2[11]-	Rx2[11]+ Rx2[11]-	Tx3[11]+ Tx3[11]-	Rx3[11]+ Rx3[11]-
			RO Str 5 from FEX 12	RO Str 3 from FEX 12	RO Str 6 from FEX 12	RO Str 4 from FEX 12
	04		Tx0[11]+ Tx0[11]-	Rx0[11]+ Rx0[11]-	Tx1[11]+ Tx1[11]-	Rx1[11]+ Rx1[11]-
			LHC Clk to FEX 12	RO Str 1 from FEX 12	TTCCombData to FEX 12	RO Str 2 from FEX 12

Continued on next page…

J21/P21	05	Fabric Channel 10	Tx2[10]+ Tx2[10]- RO Str 5 from FEX 11	Rx2[10]+ Rx2[10]- RO Str 3 from FEX 11	Tx3[10]+ Tx3[10]- RO Str 6 from FEX 11	Rx3[10]+ Rx3[10]- RO Str 4 from FEX 11
	06		Tx0[10]+ Tx0[10]- LHC Clk to FEX 11	Rx0[10]+ Rx0[10]- RO Str 1 from FEX 11	Tx1[10]+ Tx1[10]- TTCCombData to FEX 11	Rx1[10]+ Rx1[10]- RO Str 2 from FEX 11
J21/P21	07	Fabric Channel 09	Tx2[09]+ Tx2[09]- RO Str 5 from FEX 10	Rx2[09]+ Rx2[09]- RO Str 3 from FEX 10	Tx3[09]+ Tx3[09]- RO Str 6 from FEX 10	Rx3[09]+ Rx3[09]- RO Str 4 from FEX 10
	08		Tx0[09]+ Tx0[09]- LHC Clk to FEX 10	Rx0[09]+ Rx0[09]- RO Str 1 from FEX 10	Tx1[09]+ Tx1[09]- TTCCombData to FEX 10	Rx1[09]+ Rx1[09]- RO Str 2 from FEX 10
J21/P21	09	Fabric Channel 08	Tx2[08]+ Tx2[08]- RO Str 5 from FEX 09	Rx2[08]+ Rx2[08]- RO Str 3 from FEX 09	Tx3[08]+ Tx3[08]- RO Str 6 from FEX 09	Rx3[08]+ Rx3[08]- RO Str 4 from FEX 09
	10		Tx0[08]+ Tx0[08]- LHC Clk to FEX 09	Rx0[08]+ Rx0[08]- RO Str 1 from FEX 09	Tx1[08]+ Tx1[08]- TTCCombData to FEX 09	Rx1[08]+ Rx1[08]- RO Str 2 from FEX 09
P22/J22	01	Fabric Channel 07	Tx2[07]+ Tx2[07]- RO Str 5 from FEX 08	Rx2[07]+ Rx2[07]- RO Str 3 from FEX 08	Tx3[07]+ Tx3[07]- RO Str 6 from FEX 08	Rx3[07]+ Rx3[07]- RO Str 4 from FEX 08
	02		Tx0[07]+ Tx0[07]- LHC Clk to FEX 08	Rx0[07]+ Rx0[07]- RO Str 1 from FEX 08	Tx1[07]+ Tx1[07]- TTCCombData to FEX 08	Rx1[07]+ Rx1[07]- RO Str 2 from FEX 08
P22/J22	03	Fabric Channel 06	Tx2[06]+ Tx2[06]- RO Str 5 from FEX 07	Rx2[06]+ Rx2[06]- RO Str 3 from FEX 07	Tx3[06]+ Tx3[06]- RO Str 6 from FEX 07	Rx3[06]+ Rx3[06]- RO Str 4 from FEX 07
	04		Tx0[06]+ Tx0[06]- LHC Clk to FEX 07	Rx0[06]+ Rx0[06]- RO Str 1 from FEX 07	Tx1[06]+ Tx1[06]- TTCCombData to FEX 07	Rx1[06]+ Rx1[06]- RO Str 2 from FEX 07
P22/J22	05	Fabric Channel 05	Tx2[05]+ Tx2[05]- RO Str 5 from FEX 06	Rx2[05]+ Rx2[05]- RO Str 3 from FEX 06	Tx3[05]+ Tx3[05]- RO Str 6 from FEX 06	Rx3[05]+ Rx3[05]- RO Str 4 from FEX 06
	06		Tx0[05]+ Tx0[05]- LHC Clk to FEX 06	Rx0[05]+ Rx0[05]- RO Str 1 from FEX 06	Tx1[05]+ Tx1[05]- TTCCombData to FEX 06	Rx1[05]+ Rx1[05]- RO Str 2 from FEX 06
P22/J22	07	Fabric Channel 04	Tx2[04]+ Tx2[04]- RO Str 5 from FEX 05	Rx2[04]+ Rx2[04]- RO Str 3 from FEX 05	Tx3[04]+ Tx3[04]- RO Str 6 from FEX 05	Rx3[04]+ Rx3[04]- RO Str 4 from FEX 05
	08		Tx0[04]+ Tx0[04]- LHC Clk to FEX 05	Rx0[04]+ Rx0[04]- RO Str 1 from FEX 05	Tx1[04]+ Tx1[04]- TTCCombData to FEX 05	Rx1[04]+ Rx1[04]- RO Str 2 from FEX 05
P22/J22	09	Fabric Channel 03	Tx2[03]+ Tx2[03]- RO Str 5 from FEX 04	Rx2[03]+ Rx2[03]- RO Str 3 from FEX 04	Tx3[03]+ Tx3[03]- RO Str 6 from FEX 04	Rx3[03]+ Rx3[03]- RO Str 4 from FEX 04
	10		Tx0[03]+ Tx0[03]- LHC Clk to FEX 04	Rx0[03]+ Rx0[03]- RO Str 1 from FEX 04	Tx1[03]+ Tx1[03]- TTCCombData to FEX 04	Rx1[03]+ Rx1[03]- RO Str 2 from FEX 04

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P23/J23	01	Fabric Channel 02	Tx2[02]+ Tx2[02]- RO Str 5 from FEX 03	Rx2[02]+ Rx2[02]- RO Str 3 from FEX 03	Tx3[02]+ Tx3[02]- RO Str 6 from FEX 03	Rx3[02]+ Rx3[02]- RO Str 4 from FEX 03
	02		Tx0[02]+ Tx0[02]- LHC Clk to FEX 03	Rx0[02]+ Rx0[02]- RO Str 1 from FEX 03	Tx1[02]+ Tx1[02]- TTCCombData to FEX 03	Rx1[02]+ Rx1[02]- RO Str 2 from FEX 03
P23/J23	03	Fabric Channel 01	Tx2[01]+ Tx2[01]- RO Str 1 to othHUB	Rx2[01]+ Rx2[01]- RO Str 1 from othHUB	Tx3[01]+ Tx3[01]- RO Str 2 to othHUB	Rx3[01]+ Rx3[01]- RO Str2 from othHUB
	04		Tx0[01]+ Tx0[01]- LHC Clk to othHUB	Rx0[01]+ Rx0[01]- LHC Clk from othHUB	Tx1[01]+ Tx1[01]- TTC/ROD Ctl to othHUB	Rx1[01]+ Rx1[01]- TTC/ROD Ctl from othHUB
P23/J23	05	ShMC	BI_ShMCA+ BI_ShMCA- Unused signal pair	BI_ShMCB+ BI_ShMCB- Unused signal pair	BI_ShMCC+ BI_ShMCC- Unused signal pair	BI_ShMCD+ BI_ShMCD- Unused signal pair
P23/J23	06	Base Chan 02	BI_DA2+ BI_DA2- Unused signal pair	BI_DB2+ BI_DB2- Unused signal pair	BI_DC2+ BI_DC2- Unused signal pair	BI_DD2+ BI_DD2- Unused signal pair
P23/J23	07	Base Chan 03	BI_DA3+ BI_DA3- GE Pair A to FEX 03	BI_DB3+ BI_DB3- GE Pair B to FEX 03	BI_DC3+ BI_DC3- GE Pair C to FEX 03	BI_DD3+ BI_DD3- GE Pair D to FEX 03
P23/J23	08	Base Chan 04	BI_DA4+ BI_DA4- GE Pair A to FEX 04	BI_DB4+ BI_DB4- GE Pair B to FEX 04	BI_DC4+ BI_DC4- GE Pair C to FEX 04	BI_DD4+ BI_DD4- GE Pair D to FEX 04
P23/J23	09	Base Chan 05	BI_DA5+ BI_DA5- GE Pair A to FEX 05	BI_DB5+ BI_DB5- GE Pair B to FEX 05	BI_DC5+ BI_DC5- GE Pair C to FEX 05	BI_DD5+ BI_DD5- GE Pair D to FEX 05
P23/J23	10	Base Chan 06	BI_DA6+ BI_DA6- GE Pair A to FEX 06	BI_DB6+ BI_DB6- GE Pair B to FEX 06	BI_DC6+ BI_DC6- GE Pair C to FEX 06	BI_DD6+ BI_DD6 GE Pair D to FEX 06
J24/P24	01	Base Chan 07	BI_DA7+ BI_DA7- GE Pair A to FEX 07	BI_DB7+ BI_DB7- GE Pair B to FEX 07	BI_DC7+ BI_DC7- GE Pair C to FEX 07	BI_DD7+ BI_DD7- GE Pair D to FEX 07
J24/P24	02	Base Chan 08	BI_DA8+ BI_DA8- GE Pair A to FEX 08	BI_DB8+ BI_DB8- GE Pair B to FEX 08	BI_DC8+ BI_DC8- GE Pair C to FEX 08	BI_DD8+ BI_DD8- GE Pair D to FEX 08
J24/P24	03	Base Chan 09	BI_DA9+ BI_DA9- GE Pair A to FEX 09	BI_DB9+ BI_DB9- GE Pair B to FEX 09	BI_DC9+ BI_DC9- GE Pair C to FEX 09	BI_DD9+ BI_DD9- GE Pair D to FEX 09
J24/P24	04	Base Chan 10	BI_DA10+ BI_DA10- GE Pair A to FEX 10	BI_DB10+ BI_DB10- GE Pair B to FEX 10	BI_DC10+ BI_DC10- GE Pair C to FEX 10	BI_DD10+ BI_DD10- GE Pair D to FEX 10
J24/P24	05	Base Chan 11	BI_DA11+ BI_DA11- GE Pair A to FEX 11	BI_DB11+ BI_DB11- GE Pair B to FEX 11	BI_DC11+ BI_DC11- GE Pair C to FEX 11	BI_DD11+ BI_DD11- GE Pair D to FEX 11
J24/P24	06	Base Chan 12	BI_DA12+ BI_DA12- GE Pair A to FEX 12	BI_DB12+ BI_DB12- GE Pair B to FEX 12	BI_DC12+ BI_DC12- GE Pair C to FEX 12	BI_DD12+ BI_DD12- GE Pair D to FEX 12

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J24/P24	07	Base Chan 13	BI_DA13+ BI_DA13- GE Pair A to FEX 13	BI_DB13+ BI_DB13- GE Pair B to FEX 13	BI_DC13+ BI_DC13- GE Pair C to FEX 13	BI_DD13+ BI_DD13- GE Pair D to FEX 13
J24/P24	08	Base Chan 14	BI_DA14+ BI_DA14- GE Pair A to FEX 14	BI_DB14+ BI_DB14- GE Pair B to FEX 14	BI_DC14+ BI_DC14- GE Pair C to FEX 14	BI_DD14+ BI_DD14- GE Pair D to FEX 14
J24/P24	09	Base Chan 15	BI_DA15+ BI_DA15- Unused signal pair	BI_DB15+ BI_DB15- Unused signal pair	BI_DC15+ BI_DC15- Unused signal pair	BI_DD15+ BI_DD15- Unused signal pair
J24/P24	10	Base Chan 16	BI_DA16+ BI_DA16- Unused signal pair	BI_DB16+ BI_DB16- Unused signal pair	BI_DC16+ BI_DC16- Unused signal pair	BI_DD16+ BI_DD16- Unused signal pair

Note: the FEX numbering above follows the L1Calo convention to call
"FEX 03" the module in ATCA Slot 3,
"FEX 04" the module in ATCA Slot 4,

...

"FEX 14" the module in ATCA Slot 14.

Note: the name "othHUB" above stands for "the other HUB in the same ATCA crate"

14.2 Connector and Signal Usage for a FEX Slot

Connector Usage for a FEX Slot

Connect Number	Row Num	Name	Connector Pin Pairs a b	c d	e f	g h
P23/J23	01	Fabric Channel 02	Tx2[02]+ Tx2[02]- RO Stream 3 to HUB 2	Rx2[02]+ Rx2[02]- RO Stream 5 to HUB 2	Tx3[02]+ Tx3[02]- RO Stream 4 to HUB 2	Rx3[02]+ Rx3[02]- RO Stream 6 to HUB 2
	02		Tx0[02]+ Tx0[02]- RO Stream 1 to HUB 2	Rx0[02]+ Rx0[02]- LHC Clock from Hub2	Tx1[02]+ Tx1[02]- RO Stream 2 to HUB 2	Rx1[02]+ Rx1[02]- TTCCombData from Hub2
P23/J23	03	Fabric Channel 01	Tx2[01]+ Tx2[01]- RO Stream 3 to HUB 1	Rx2[01]+ Rx2[01]- RO Stream 5 to HUB 1	Tx3[01]+ Tx3[01]- RO Stream 4 to HUB 1	Rx3[01]+ Rx3[01]- RO Stream 6 to HUB 1
	04		Tx0[01]+ Tx0[01]- RO Stream 1 to HUB 1	Rx0[01]+ Rx0[01]- LHC Clock from Hub1	Tx1[01]+ Tx1[01]- RO Stream 2 to HUB 1	Rx1[01]+ Rx1[01]- TTCCombData from Hub1
P23/J23	05	Base Chan 01	BI_DA1+ BI_DA1- GE Pair A IPbus Net	BI_DB1+ BI_DB1- GE Pair B IPbus Net	BI_DC1+ BI_DC1- GE Pair C IPbus Net	BI_DD1+ BI_DD1- GE Pair D IPbus Net
P23/J23	06	Base Chan 02	BI_DA2+ BI_DA2- GE Pair A IPMC Net	BI_DB2+ BI_DB2- GE Pair B IPMC Net	BI_DC2+ BI_DC2- GE Pair C IPMC Net	BI_DD2+ BI_DD2- GE Pair D IPMC Net
P23/J23	07	Base Chan 03	BI_DA3+ BI_DA3- Unused signal pair	BI_DB3+ BI_DB3- Unused signal pair	BI_DC3+ BI_DC3- Unused signal pair	BI_DD3+ BI_DD3- Unused signal pair
P23/J23	08	Base Chan 04	BI_DA4+ BI_DA4- Unused signal pair	BI_DB4+ BI_DB4- Unused signal pair	BI_DC4+ BI_DC4- Unused signal pair	BI_DD4+ BI_DD4- Unused signal pair
P23/J23	09	Base Chan 05	BI_DA5+ BI_DA5- Unused signal pair	BI_DB5+ BI_DB5- Unused signal pair	BI_DC5+ BI_DC5- Unused signal pair	BI_DD5+ BI_DD5- Unused signal pair
P23/J23	10	Base Chan 06	BI_DA6+ BI_DA6- Unused signal pair	BI_DB6+ BI_DB6- Unused signal pair	BI_DC6+ BI_DC6- Unused signal pair	BI_DD6+ BI_DD6 Unused signal pair

15 Appendix 2: Hub Module FEX MGT Data Fanout

This section describes the 74 channel MGT Fanout on the Hub Module. This fanout receives FEX readout data from the Hub's ATCA Zone 2 connectors and sends this data to MGT transceiver inputs on both the ROD mezzanine card and to the Hub's own UltraScale Virtex FPGA. This fanout is based on the NB7VQ14M chip from On-Semi. Illustrations of the circuit diagrams can be found in **Figure 22** and **Figure 23**.

15.1 AC Coupling

The outputs from the NB7VQ14M fanout chips are AC coupled. 100 nFd 0201 size DC Blocking capacitors are used for this AC coupling. These capacitors are located very close the output pins on the NB7VQ14M fanout chips.

15.2 Input Common Mode Reference

The signals send to the Hub's MGT Fanout are all AC coupled at the sending end. Thus the input common mode voltage to NB7VQ14M fanout chips can and must be set with circuits on the Hub Module.

The fanout chips internal VRef generator is used to set their common mode input voltage. When powered with a Vcc of 1.800 Volts this reference generator provides a 1.300 V +- 150 mV common mode input voltage to the fanout chips. This makes sense as the input circuit of these fanout chips is the bases of a long-tail NPN pair the emitters of which are feed by a current source.

15.3 Input Termination

The NB7VQ14M fanout chips contain their own input termination resistors. From a center tap there is a 50 Ohm resistor to each input. This center tap is tied to the common mode reference supply and bypassed to ground with a 47 nFd capacitor. In this way the common mode input voltage to the receiver is set, the 100 Ohm differential termination is realized, and a common mode termination is implemented.

15.4 Equalizer Enable

The NB7VQ14M fanout chips contain an equalizer that can reduce inter symbol interference on long copper PCB traces. This equalizer is enabled or removed from the fanout circuit by means of a logic level control pin.

Because it is not yet clear if this equalizer will improve the MGT readout signals in the ATCA backplane application we will make the Equalizer Enable pin accessible on the Hub Module on a per slot basis. The assumption is that for the backplane losses from a

given slot that either all 6 of the MGT readout signals from that slot will be improved by the equalizer or else none of them will.

Thus from the point of view of the Equalizer Enables, the MGT fanout it is divided into 13 section (12 FEXs and the Other Hub) with the equalizer enables individually programmable to each of these sections.

The equalizer enable input pin has a 75k Ohm pull-down resistor. 6 of these in parallel is 12.5k Ohm. When this logic input is at its default Low the equalizer is bypassed. The equalizer enable logic levels are:

- Low is < 0.35 Vcc High is > 0.65 Vcc.
- With 1.8 Volt Vcc Low is < 0.630 and High is > 1.170 Volts
- Current is under +- 150 uAmp.

The fanout equalizer enable pins are driven by a 1V8 HP Select I/O Bank on the Hub FPGA. In the Hi state, these control signals from the Hub FPGA are guaranteed to reach 1.35 Volts (in LVCMOS_1V8 mode) or 1.400 Volts (in HSTL mode). So we are guaranteed to be able to remain in control of these equalizer enable inputs with the fanout chips operating from a Vcc as high as 2.154 Volts.

15.5 Reference Designators

The Hub Module uses an overall scheme to organize the reference designators of its many components. The fanout chips themselves run from U401 through U475 with an increment of 1 between channels. The various capacitors in these circuits (DC blocking, Vcc bypass, VRef bypass) run from C401 through C919 with an increment of 7 between channels.

15.6 Fanout Vcc Supply

The NB7VQ14M fanout chips can be powered with anything from 1.8 V to 3.3V. The lower supply voltages are attractive because of the reduced heat dissipation. From the data sheet I see no advantage in powering the fanout circuits from a 3.3 Volt supply. Ed Flaherty's ROD work indicates that 1V8 works as well or better than 2V5.

There may be some advantage in using a fanout Vcc supply somewhat higher than the 1V8 minimum listed in the NB7VQ14M data sheet. In any case this supply must be quiet as any noise that it puts onto these high speed MGT signals is likely to interfere with reception of these signals from across the ATCA backplane.

Thus the Hub Module provides a private supply just for powering these fanout chips. This supply, FAN_1V8, is nominally set for 1.8 Volts. Because it does not power

anything besides the fanout chips it could be adjusted up to at least 2.150 Volts if that is necessary.

The expected current draw for the 74 fanout chips is 13 Amps. At maximum the fanout Vcc current draw should be less than 15 Amps. The heat from the 74 fanout chips is expected to be about 23 Watts.

The Vcc pins on each fanout chip are bypassed with a 4.7 nFd and 100 nFd 0402 size ceramic capacitors as close as possible to the Vcc pins.

15.7 Routing Challenges

All of the differential pair traces associated with the FEX MGT data fanout circuits must be able to cleanly support 10 Gb/sec data rates. Interference and cross-talk must be kept to a minimum.

This is especially true on the traces that run from the Zone 2 connectors to the inputs of the fanout chips. These MGT signals may be in poor condition after their travel across the backplane and through two ADFplus connectors.

The 74 outputs running to the ROD must route out and separate from the 74 pairs that run to the Hub's FPGA. There is little space available on the Hub Module to hold the MGT fanout. Fanout chips are located on both sides of the card and the design of the side 2 cover needs to take the height and heat dissipation from these parts into consideration.

15.8 Fanout Name

In a few places the documentation for the Hub Module may still call its FEX MGT data fanout by the name "GTH Fanout". This old name came from the original design of the Hub Module that used a Virtex-7 FPGA with only GTH type MGT transceivers. The old name has been replaced in most of the Hub's documentation but I know that it is still used in the net names.

15.9 Hub-Module FEX MGT Data Fanout Map

This FEX MGT Data Fanout Map is presented in two sections. The first section shows the map from the Zone 2 inputs through to the ROD MegArray connectors. The second section shows the map from the Zone 2 inputs through to the Hub's FPGA MGT inputs. Details of the design understandings:

- The FEX cards are numbered 3:14 by their ATCA Logical Slot Number.
- The 6 Aurora Lanes carrying FEX readout data are assigned to the ATCA Fabric Interface Channel Ports in the following way:

Aurora Lane	0	1	2	3	4	5
FEX End ATCA	Tx0	Tx1	Tx2	Tx3	Rx2	Rx3
Hub End ATCA	Rx0	Rx1	Rx2	Rx3	Tx2	Tx3
Hub Zone 2 Pins	c,d	g,h	c,d	g,h	a,b	e,f
Hub Zone 2 Row	lower	lower	upper	upper	upper	upper

- All FEX Aurora data on the ATCA backplane is "right side up". That is, if for high speed routing considerations, a given FEX card criss-crosses some of its MGT Transmitter direct and complement output pins with the ATCA backplane direct and complement pins then it will also setup these MGT Transmitters to invert their output data.
- The MegArray connector pinout is defined by the V1p4 document from 6-May-2015 written by Ed.
- With these understandings, all readout data delivered to the ROD will be "right side up" with the map that follows.

Description of the Columns in this Map Table:

- MGT Fanout Channel Number, this table is listed in order of the MGT Fanout Channels on the Hub circuit board. The Hub Module netlist is in terms of MGT Fanout Channel Number.
- FEX, this is the FEX card number 3:14, i.e. the ATCA Logical Slot Number of the FEX card.
- Aurora Lane, this is the Aurora protocol Lane number of the readout data from this source, 0:5.
- Zone 2 Input Pins, this column shows the ATCA Fabric Interface connector and pin numbers where this data source arrives on the Hub Module, e.g. J23-C/D2 means connector J23 pins C2 and D2. The pin carrying the direct signal (aka non-inverted signal) is always listed first, the pin carrying the complement signal (aka inverted signal) is listed second.
- Layer, the signal layer (not physical layer) in the Hub PCB on which this differential pair is routed to the MGT Fanout Array.
- Inverted, indicates whether or not the trace routing inverts this differential signal on its way from the Zone 2 connector to the MGT Fanout input.
- MegAry Con, shows whether this signal is routed to the S1 or S2 MegArray connector.
- MegArry Pins, lists the pins used in the MegArray connector for this readout signal, e.g. F/E39 means pins F39 and E39 are used for this differential signal. The pin carrying the direct signal is always listed first and the pin carrying the complement signal is listed second.
- ROD FEX Input, this is the input to the ROD in Ed's notation from his version V1p4 MegArray Pinout from 6-May-2015.

- Layer, the signal layer (not physical layer) in the Hub PCB on which this differential pair is routed from the MGT Fanout output to the MegArray connector.
- Inverted, indicates whether or not the trace routing inverts this differential signal on its way from the MGT Fanout to the MegArray connector.

The map table for the connections between the backplane Zone 2 pins and the Hub's FPGA is similar but instead of the MegArray connections it shows the connections to the FPGA MTG Receivers in terms of Quad and channel within the Quad. Again the index to this table is MGT Fanout Channel Number.

Although the readout data from the FPGA on This Hub does not pass through the MGT Fanout it is listed at the end of this table for completeness.

Map from Zone 2 Fabric Interface Inputs to ROD MEG-Array Connectors

MGT Fanout Channel	FEX	Aurora Lane	Zone 2 Input Pins	Layer	Inv	MEG-Array Con	MEG-Array Pins	ROD FEX Input	FEX Layer	Inv
1	3	0	J23-C/D2	7	N	S1	F/E39	0	7	N
2	3	1	J23-G/H2	8	Y	S1	J/H38	1	8	Y
3	3	2	J23-C/D1	9	N	S1	F/E37	2	9	N
4	3	3	J23-G/H1	6	Y	S1	J/H36	3	6	Y
5	3	4	J23-A/B1	7	N	S1	F/E35	4	7	N
6	3	5	J23-E/F1	8	Y	S1	J/H34	5	8	Y
7	4	0	J22-C/D10	9	N	S1	F/E33	6	9	N
8	4	1	J22-G/H10	6	Y	S1	J/H32	7	6	Y
9	4	2	J22-C/D9	7	N	S1	F/E31	8	7	N
10	4	3	J22-G/H9	8	Y	S1	J/H30	9	8	Y
11	4	4	J22-A/B9	9	N	S1	F/E29	10	9	N
12	4	5	J22-E/F9	6	Y	S1	J/H28	11	6	Y
13	5	0	J22-C/D8	7	N	S1	F/E27	12	7	N
14	5	1	J22-G/H8	8	Y	S1	J/H26	13	8	Y
15	5	2	J22-C/D7	9	N	S1	F/E25	14	9	N
16	5	3	J22-G/H7	6	Y	S1	J/H24	15	6	Y
17	5	4	J22-A/B7	7	N	S1	F/E23	16	7	N
18	5	5	J22-E/F7	8	Y	S1	J/H22	17	8	Y
19	6	0	J22-C/D6	9	N	S1	J/H20	18	9	N
20	6	1	J22-G/H6	6	Y	S1	F/E19	19	6	Y
21	6	2	J22-C/D5	7	N	S1	J/H18	20	7	N
22	6	3	J22-G/H5	8	Y	S1	F/E17	21	8	Y
23	6	4	J22-A/B5	9	N	S1	J/H16	22	9	N
24	6	5	J22-E/F5	6	Y	S1	F/E15	23	6	Y
25	7	0	J22-C/D4	7	N	S1	J/H14	24	7	N
26	7	1	J22-G/H4	8	Y	S1	F/E13	25	8	Y
27	7	2	J22-C/D3	9	N	S1	J/H12	26	9	N
28	7	3	J22-G/H3	6	Y	S1	F/E11	27	6	Y
29	7	4	J22-A/B3	7	N	S1	J/H10	28	7	N
30	7	5	J22-E/F3	8	Y	S1	F/E9	29	8	Y
31	8	0	J22-C/D2	9	N	S1	J/H8	30	9	N
32	8	1	J22-G/H2	6	Y	S1	F/E7	31	6	Y
33	8	2	J22-C/D1	7	N	S1	J/H6	32	7	N
34	8	3	J22-G/H1	8	Y	S1	F/E5	33	8	Y
35	8	4	J22-A/B1	9	N	S1	J/H4	34	9	N
36	8	5	J22-E/F1	6	Y	S1	F/E3	35	6	Y
MGT	FEX	Aurora	Zone 2			MEG-	MEG-	ROD	FEX	

Fanout Channel		Lane	Input Pins	Layer	Inv	Array Con	Array Pins	FEX Input	Layer	Inv
37	Other Hub	0	J23-C/D3	7	Y	S2	E/F3	HRD0	7	Y
38	Other Hub	1	J23-G/H3	8	N	S2	H/J8	HRD2	8	N
39	9	0	J21-C/D10	9	Y	S2	B/C4	71	9	Y
40	9	1	J21-G/H10	6	N	S2	E/F5	70	6	N
41	9	2	J21-C/D9	7	Y	S2	B/C6	69	7	Y
42	9	3	J21-G/H9	8	N	S2	E/F7	68	8	N
43	9	4	J21-A/B9	9	Y	S2	B/C8	67	9	Y
44	9	5	J21-E/F9	6	N	S2	E/F9	66	6	N
45	10	0	J21-C/D8	7	Y	S2	B/C10	65	7	Y
46	10	1	J21-G/H8	8	N	S2	E/F11	64	8	N
47	10	2	J21-C/D7	9	Y	S2	B/C12	63	9	Y
48	10	3	J21-G/H7	6	N	S2	E/F13	62	6	N
49	10	4	J21-A/B7	7	Y	S2	B/C14	61	7	Y
50	10	5	J21-E/F7	8	N	S2	E/F15	60	8	N
51	11	0	J21-C/D6	9	Y	S2	B/C16	59	9	Y
52	11	1	J21-G/H6	6	N	S2	E/F17	58	6	N
53	11	2	J21-C/D5	7	Y	S2	B/C18	57	7	Y
54	11	3	J21-G/H5	8	N	S2	E/F19	56	8	N
55	11	4	J21-A/B5	9	Y	S2	B/C20	55	9	Y
56	11	5	J21-E/F5	6	N	S2	E/F21	54	6	N
57	12	0	J21-C/D4	7	Y	S2	B/C22	53	7	Y
58	12	1	J21-G/H4	8	N	S2	E/F23	52	8	N
59	12	2	J21-C/D3	9	Y	S2	B/C24	51	9	Y
60	12	3	J21-G/H3	6	N	S2	E/F25	50	6	N
61	12	4	J21- A/B3	7	Y	S2	B/C26	49	7	Y
62	12	5	J21-E/F3	8	N	S2	E/F27	48	8	N
63	13	0	J21-C/D2	9	Y	S2	B/C28	47	9	Y
64	13	1	J21-G/H2	6	N	S2	E/F29	46	6	N
65	13	2	J21-C/D1	7	Y	S2	B/C30	45	7	Y
66	13	3	J21-G/H1	8	N	S2	E/F31	44	8	N
67	13	4	J21-A/B1	9	Y	S2	B/C32	43	9	Y
68	13	5	J21-E/F1	6	N	S2	E/F33	42	6	N
69	14	0	J20-C/D10	7	Y	S2	B/C34	41	7	Y
70	14	1	J20-G/H10	8	N	S2	E/F35	40	8	N
71	14	2	J20-C/D9	9	Y	S2	B/C36	39	9	Y
72	14	3	J20-G/H9	6	Y	S2	E/F37	38	6	Y
73	14	4	J20-A/B9	7	Y	S2	B/C38	37	7	Y
74	14	5	J20-E/F9	6	N	S2	E/F39	36	8	N
--	This Hub	0	--	-	-	S2	B/C2	HRD1	-	-
--	This Hub	1	--	-	-	S2	H/J6	HRD3	-	-

Map from Zone 2 Fabric Interface Inputs to This Hub's FPGA MGT Inputs:

MGT Fanout Channel	FEX	Aurora Lane	Zone 2 Input Pins	Layer	Inv	Hub FPGA MGT Receiver Chan-Quad	Type	Pins	Layer	Inv
1	3	0	J23-C/D2	7	N	Rx1-126	GTY	AF43/4	2	Y
2	3	1	J23-G/H2	8	Y	Rx0-126	GTY	AG45/6	3	N
3	3	2	J23-C/D1	9	N	Rx3-125	GTY	AH43/4	4	Y
4	3	3	J23-G/H1	6	Y	Rx2-125	GTY	AJ45/6	5	N
5	3	4	J23-A/B1	7	N	Rx1-125	GTY	AK43/4	2	Y
6	3	5	J23-E/F1	8	Y	Rx0-125	GTY	AL45/6	3	N
7	4	0	J22-C/D10	9	N	Rx3-124	GTY	AM43/4	4	Y
8	4	1	J22-G/H10	6	Y	Rx2-124	GTY	AN45/6	5	N
9	4	2	J22-C/D9	7	N	Rx1-128	GTY	V43/4	2	Y
10	4	3	J22-G/H9	8	Y	Rx0-128	GTY	W45/6	3	N
11	4	4	J22-A/B9	9	N	Rx3-127	GTY	Y43/4	4	Y
12	4	5	J22-E/F9	6	Y	Rx2-127	GTY	AA45/6	5	N
13	5	0	J22-C/D8	7	N	Rx1-127	GTY	AB43/4	2	Y
14	5	1	J22-G/H8	8	Y	Rx0-127	GTY	AC45/6	3	N
15	5	2	J22-C/D7	9	N	Rx3-126	GTY	AD43/4	4	Y
16	5	3	J22-G/H7	6	Y	Rx2-126	GTY	AE45/6	5	N
17	5	4	J22-A/B7	7	N	Rx1-130	GTY	K43/4	2	Y
18	5	5	J22-E/F7	8	Y	Rx0-130	GTY	L45/6	3	N
19	6	0	J22-C/D6	9	N	Rx3-129	GTY	M43/4	4	Y
20	6	1	J22-G/H6	6	Y	Rx2-129	GTY	N45/6	5	N
21	6	2	J22-C/D5	7	N	Rx1-129	GTY	P43/4	2	Y
22	6	3	J22-G/H5	8	Y	Rx0-129	GTY	R45/6	3	N
23	6	4	J22-A/B5	9	N	Rx3-128	GTY	T43/4	4	Y
24	6	5	J22-E/F5	6	Y	Rx2-128	GTY	U45/6	5	N
25	7	0	J22-C/D4	7	N	Rx3-132	GTY	B43/4	2	Y
26	7	1	J22-G/H4	8	Y	Rx2-132	GTY	C45/6	3	N
27	7	2	J22-C/D3	9	N	Rx1-132	GTY	D43/4	4	Y
28	7	3	J22-G/H3	6	Y	Rx0-132	GTY	E45/6	5	N
29	7	4	J22-A/B3	7	N	Rx1-131	GTY	F43/4	2	Y
30	7	5	J22-E/F3	8	Y	Rx0-131	GTY	G45/6	3	N
31	8	0	J22-C/D2	9	N	Rx3-130	GTY	H43/4	4	Y
32	8	1	J22-G/H2	6	Y	Rx2-130	GTY	J45/6	5	N
33	8	2	J22-C/D1	7	N	Rx2-231	GTH	G16/5	2	N
34	8	3	J22-G/H1	8	Y	Rx3-231	GTH	E16/5	3	Y
35	8	4	J22-A/B1	9	N	Rx3-131	GTY	E31/2	4	Y
36	8	5	J22-E/F1	6	Y	Rx2-131	GTY	G31/2	5	N
37	Other Hub	0	J23-C/D3	7	Y	Rx3-133	GTY	A31/2	2	N
38	Other Hub	1	J23-G/H3	8	N	Rx2-133	GTY	B33/4	3	N
39	9	0	J21-C/D10	9	Y	Rx1-133	GTY	C31/2	4	Y
40	9	1	J21-G/H10	6	N	Rx0-133	GTY	D33/4	5	N
41	9	2	J21-C/D9	7	Y	Rx0-232	GTH	E 2/1	2	N
42	9	3	J21-G/H9	8	N	Rx1-232	GTH	D 4/3	3	Y
43	9	4	J21-A/B9	9	Y	Rx2-232	GTH	C 2/1	4	N
44	9	5	J21-E/F9	6	N	Rx3-232	GTH	B 4/3	5	Y
45	10	0	J21-C/D8	7	Y	Rx0-233	GTH	D14/3	2	N
46	10	1	J21-G/H8	8	N	Rx1-233	GTH	C16/5	3	Y
47	10	2	J21-C/D7	9	Y	Rx2-233	GTH	B14/3	4	N
48	10	3	J21-G/H7	6	N	Rx3-233	GTH	A16/5	5	N
49	10	4	J21-A/B7	7	Y	Rx2-229	GTH	N 2/1	2	N
50	10	5	J21-E/F7	8	N	Rx3-229	GTH	M 4/3	3	Y
51	11	0	J21-C/D6	9	Y	Rx0-230	GTH	L 2/1	4	N
52	11	1	J21-G/H6	6	N	Rx1-230	GTH	K 4/3	5	Y
53	11	2	J21-C/D5	7	Y	Rx2-230	GTH	J 2/1	2	N
54	11	3	J21-G/H5	8	N	Rx3-230	GTH	H 4/3	3	Y

55	11	4	J21-A/B5	9	Y	Rx0-231	GTH	G 2/1	4	N
56	11	5	J21-E/F5	6	N	Rx1-231	GTH	F 4/3	5	Y
57	12	0	J21-C/D4	7	Y	Rx2-227	GTH	AA2/1	2	N
58	12	1	J21-G/H4	8	N	Rx3-227	GTH	Y 4/3	3	Y
59	12	2	J21-C/D3	9	Y	Rx0-228	GTH	W 2/1	4	N
60	12	3	J21-G/H3	6	N	Rx1-228	GTH	V 4/3	5	Y
61	12	4	J21-A/B3	7	Y	Rx2-228	GTH	U 2/1	2	N
62	12	5	J21-E/F3	8	N	Rx3-228	GTH	T 4/3	3	Y
63	13	0	J21-C/D2	9	Y	RX0-229	GTH	R 2/1	4	N
64	13	1	J21-G/H2	6	N	Rx1-229	GTH	P 4/3	5	Y
65	13	2	J21-C/D1	7	Y	Rx0-225	GTH	AL 2/1	2	N
66	13	3	J21-G/H1	8	N	Rx1-225	GTH	AK 4/3	3	Y
67	13	4	J21-A/B1	9	Y	Rx2-225	GTH	AJ 2/1	4	N
68	13	5	J21-E/F1	6	N	Rx3-225	GTH	AH 4/3	5	Y
69	14	0	J20-C/D10	7	Y	Rx0-226	GTH	AG 2/1	2	N
70	14	1	J20-G/H10	8	N	Rx1-226	GTH	AF 4/3	3	Y
71	14	2	J20-C/D9	9	Y	Rx2-226	GTH	AE 2/1	4	N
72	14	3	J20-G/H9	6	Y	Rx3-226	GTH	AD 4/3	5	Y
73	14	4	J20-A/B9	7	Y	Rx0-227	GTH	AC 2/1	2	N
74	14	5	J20-E/F9	6	N	Rx1-227	GTH	AB 4/3	3	Y

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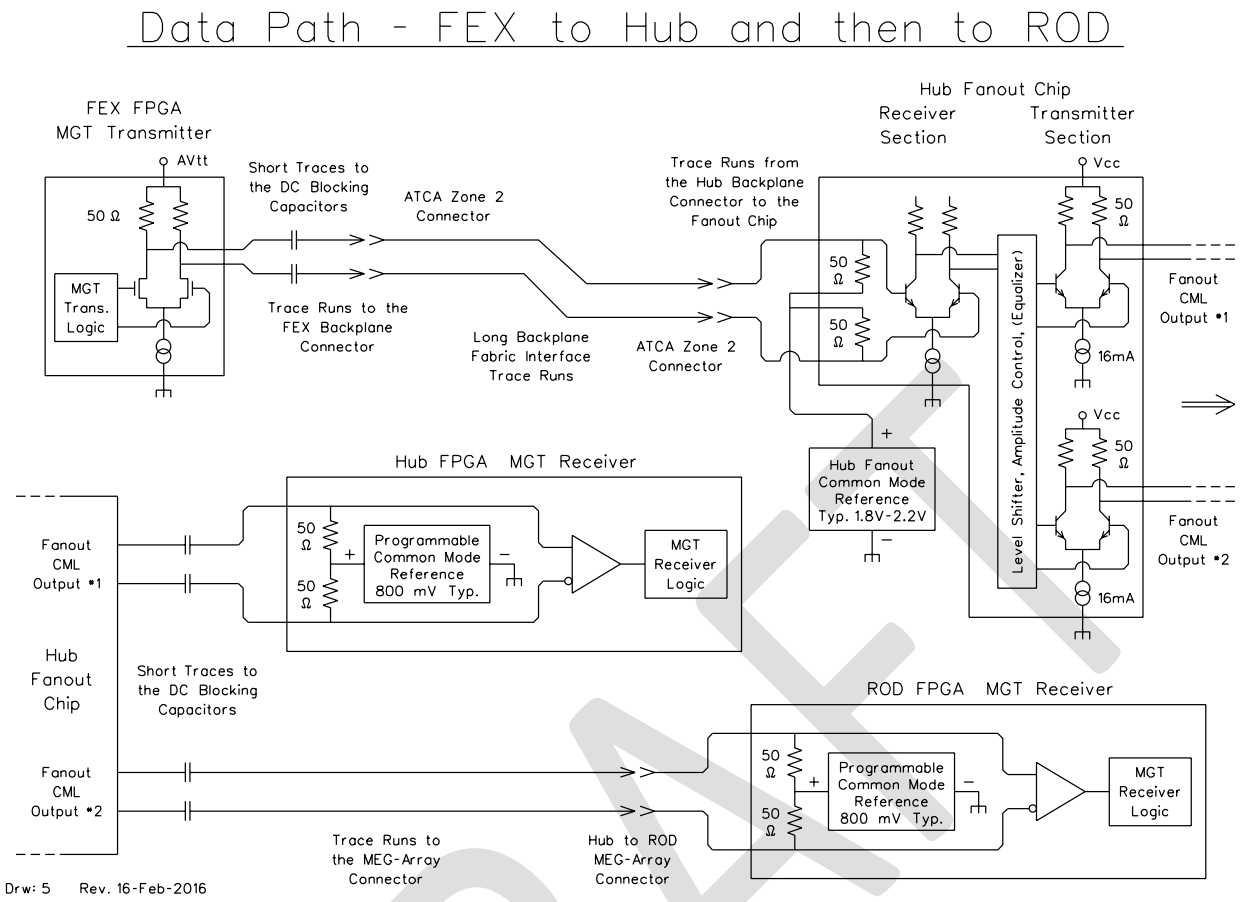

Figure 22: Circuit diagram of FEX/Hub/ROD high-speed data paths.

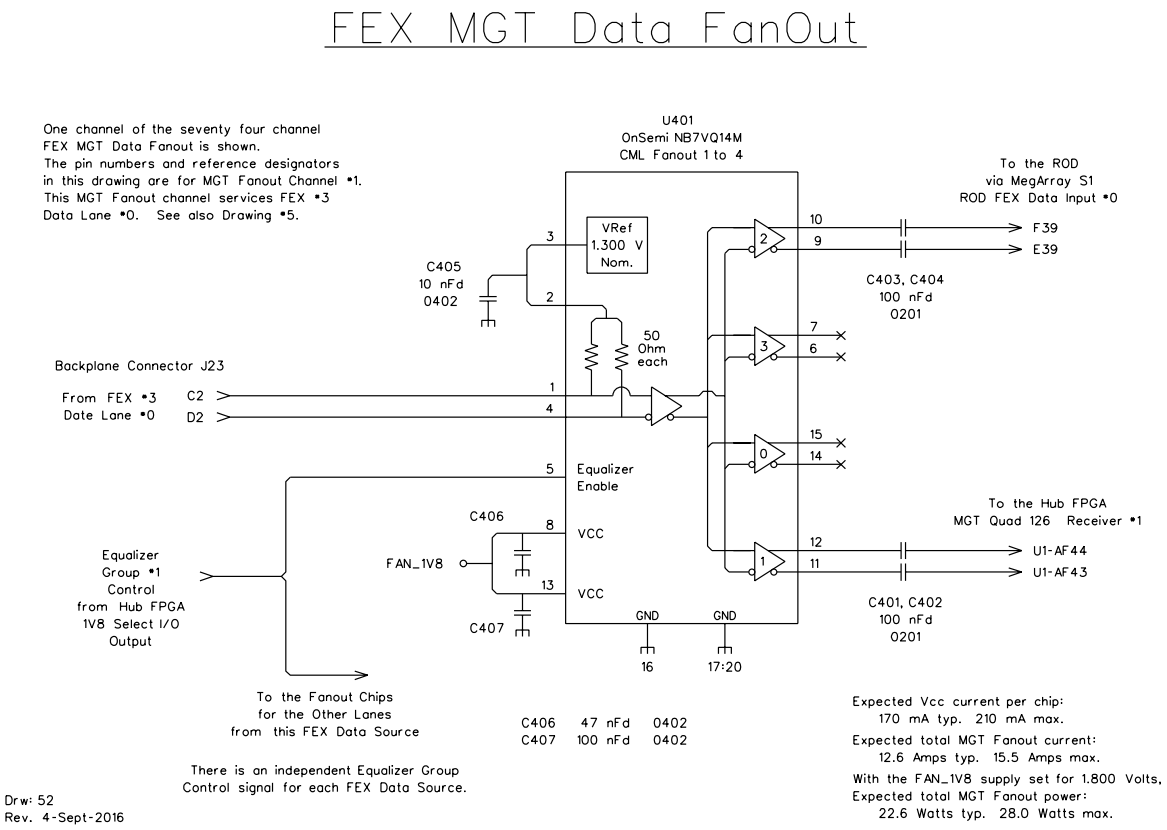

Figure 23: Hub MGT FanOut circuit diagram.

16 Appendix 3: Hub-Module Clock Generation and Distribution

The Hub-Module uses 3 different clocks:

- Ethernet 25.000 MHz Clock crystal controlled
- 40.08 MHz LHC locked clock for FPGA logic
- 320.64 MHz LHC locked clock for MGT Reference and FPGA logic

16.1 Ethernet 25.000 MHz Clock

The 25 MHz clock generation and distribution are shown in **Figure 24**. This clock is generated by a local crystal and thus is not LHC locked. All other clocks on the Hub Module are LHC locked. The main purpose of the 25.000 MHz clock is to run the Ethernet Switches and the Phys chips.

The crystal that is used to generate this clock has better frequency tolerance and jitter specification than are required by either the Switch or Phys chips. The output of this crystal oscillator is fanned out 6 ways by a low jitter TI clock fanout chip. The 25 MHz clock signals from this fanout are all single ended back terminated 3V3 CMOS level. There are separate clock feeds to each of the 3 Switch chips and to both of the Phys chips. There is also a 25.000 MHz clock feed to a Global Clock input in Select I/O Bank 94 of the FPGA. This is in SLR #0 of the UltraScale FPGA.

The clock input on the Switch chips requires a high level of 1.7 V min and 3.8 V max (XtalVdd + 0.5V max). The clock input on the Phys chips requires a high level of 2.5 V min and 3.3 V max. So a 3V3 clock is fine for both the Switch and Phys chips.

Each of the Phys chips multiplies the 25.000 MHz clock that it receives up to 125 MHz. These Phys chips make their 125 MHz clocks available on output pins in case they are needed by the associated MACs. The 125 MHz clock outputs from the 2 Phys chips have been routed to Global Clock inputs in Select I/O Bank 68 of the FPGA. This is the same I/O Bank that handles all of the RGMII MAC interface connections between the FPGA and the Phys chips. This I/O Bank is in SLR #0 of the UltraScale FPGA.

16.2 40.08 MHz LHC Locked Clock

The Hub's 40.08 MHz clock generation is shown in **Figure 26**. This 40.08 MHz clock is designed to be locked to the LHC.

To make this lock an LHC reference clock is received either as an FELIX Optical TTC signal using one of the Hub's MiniPOD Receivers or it is received from the Other Hub as a differential pair over the ATCA fabric interface backplane.

Both the decoding of the optical LHC reference clock and the selection between using the optical reference or using the reference from the Other Hub are implemented in the Hub's FPGA. This is shown in the left-hand side of **Figure 26**.

In either case, the selected LHC reference clock leaves Bank 68 of the FPGA as an LVDS signal and is routed to an LVDS to single ended receiver U501 that is located right next to the 40.08 MHz crystal controlled PLL U502. This crystal controlled PLL has a low loop frequency so that it removes jitter from the selected LHC reference. When no LHC reference is available the PLL will hold within 50 ppm of the nominal LHC frequency. A signal indicating whether or not this PLL is locked to its reference is sent to a Select I/O input on the Hub's FPGA where it can be monitored in an IPBus visible status register.

The 40.08 MHz LVPECL output from this PLL is routed to a set of clock fanouts that are shown in **Figure 26**. The First Fanout U503 drives 4 loads and then a Second Fanout U504 drives the 12 FEX cards plus the Other Hub over the Backplane. This two step fanout is necessary because of the two Hub cards in a Shelf only the Hub that receives the FELIX Optical TTC signal will drive its backplane clock lines. Thus the Second Fanout U504 can be controlled from the Hub's FPGA so that it either operates normally or else it holds its output pins static. Only on the Hub that receives the FELIX Optical TTC signal will this Second Fanout be enabled and thus provide a backplane clock to the 12 FEX cards and to the Other Hub.

First Fanout U503 a TI CDCLVD1204 drives:

- the ROD Mezzanine on This Hub
- a Select I/O Global Clock input pair in Bank 71 of This Hub's FPGA for use as a logic clock
- a reference to the 320.64 MHz Clock on This Hub
- the Second 40.08 MHz Fanout on This Hub

Second 40.08 MHz Fanout U504 a TI CDCLVD1216 drives:

- the 12 FEX cards over the backplane
- the Other Hub over the backplane

The 2V5 and 3V3 power for the 40.08 MHz clock generation and distribution components is LC filtered from the bulk supplies and distributed to these components on separate isolated PCB area fills. The ground plane under these components has been partially separated from the rest of the Hub's ground plane with a moat.

Figure 25 includes a note about FPGA differential pin pairs that receive this AC coupled LVDS clock signals.

16.3 320.64 MHz LHC Locked Clock for MGT Reference and FPGA Logic

The Hub's 320.64 MHz clock is shown in **Figure 27**. This is also an LHC locked clock. It uses a fanout copy of the Hub's 40.08 MHz clock as its reference.

This 40.08 MHz LVDS reference signal is received by U505 and converted to a single ended CMOS reference signal for U506, the 320.64 MHz PLL. This crystal controlled PLL has a loop frequency that allows it to track changes in the output of the Hub's 40.08 MHz PLL. A signal indicating whether or not this PLL is locked to its reference is sent to a Select I/O input on the Hub's FPGA where it can be monitored in an IPBus visible status register.

The LVPECL output from the 320.64 MHz PLL is delivered to U507 which is a MC100LVEP111 10 way LVPECL fanout.

- 8 copies of the 320.64 MHz clock from this fanout are delivered to MGT Reference Clock inputs on This Hub's FPGA. These are delivered as AC coupled LVPECL signals. The MGT Reference Clock inputs that receive this clock are listed near the end of Section 18.

- A copy of the 320.64 MHz clock from this fanout is delivered to a Select I/O Global Clock input pair in Bank 71 of This Hub's FPGA for use as a logic clock. Note that the correct options need to be set in this I/O Block to allow it to receive this AC coupled clock signal. See the note on **Figure 27**.

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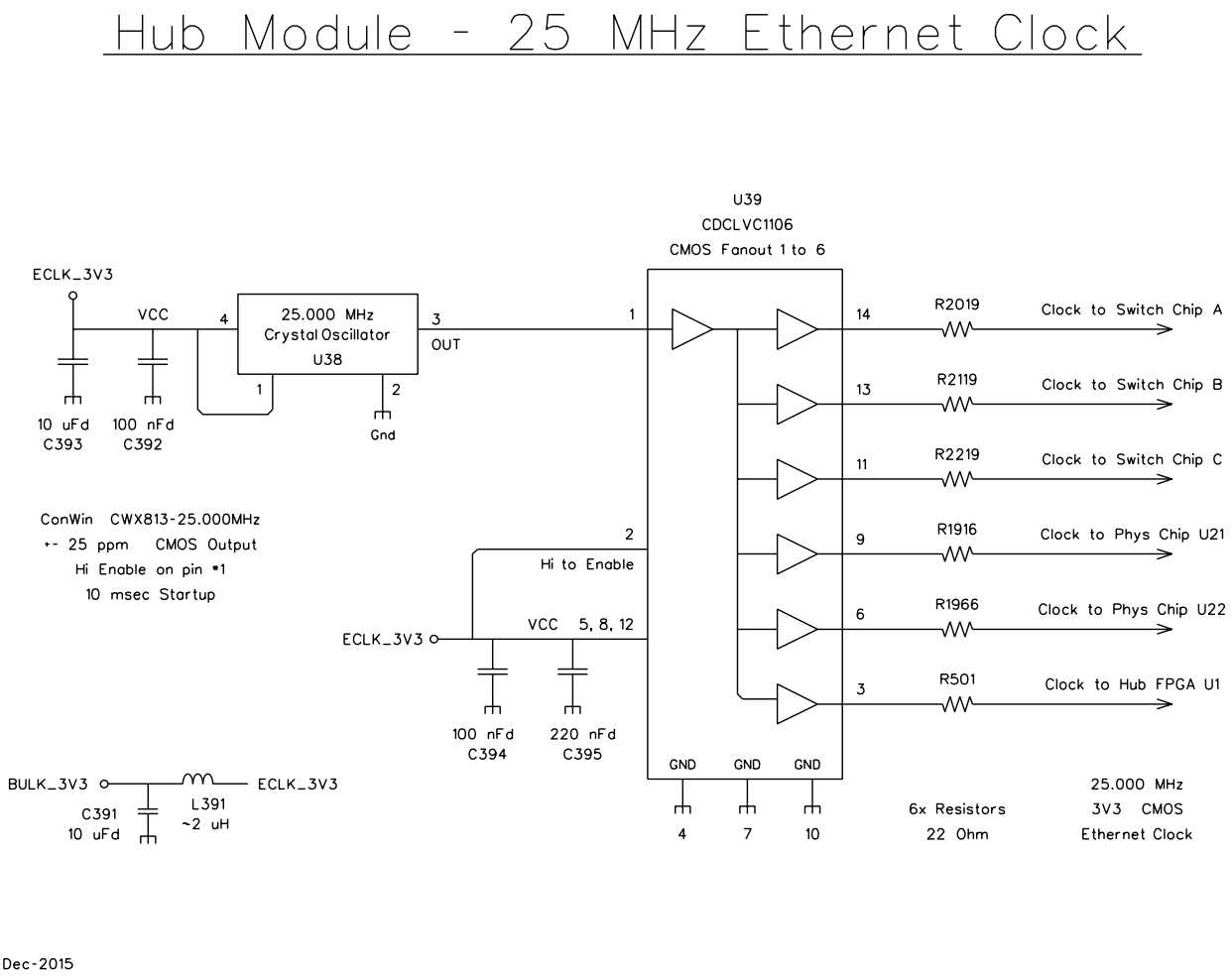

Figure 24: Circuit diagram of Hub 25 MHz Ethernet clock.

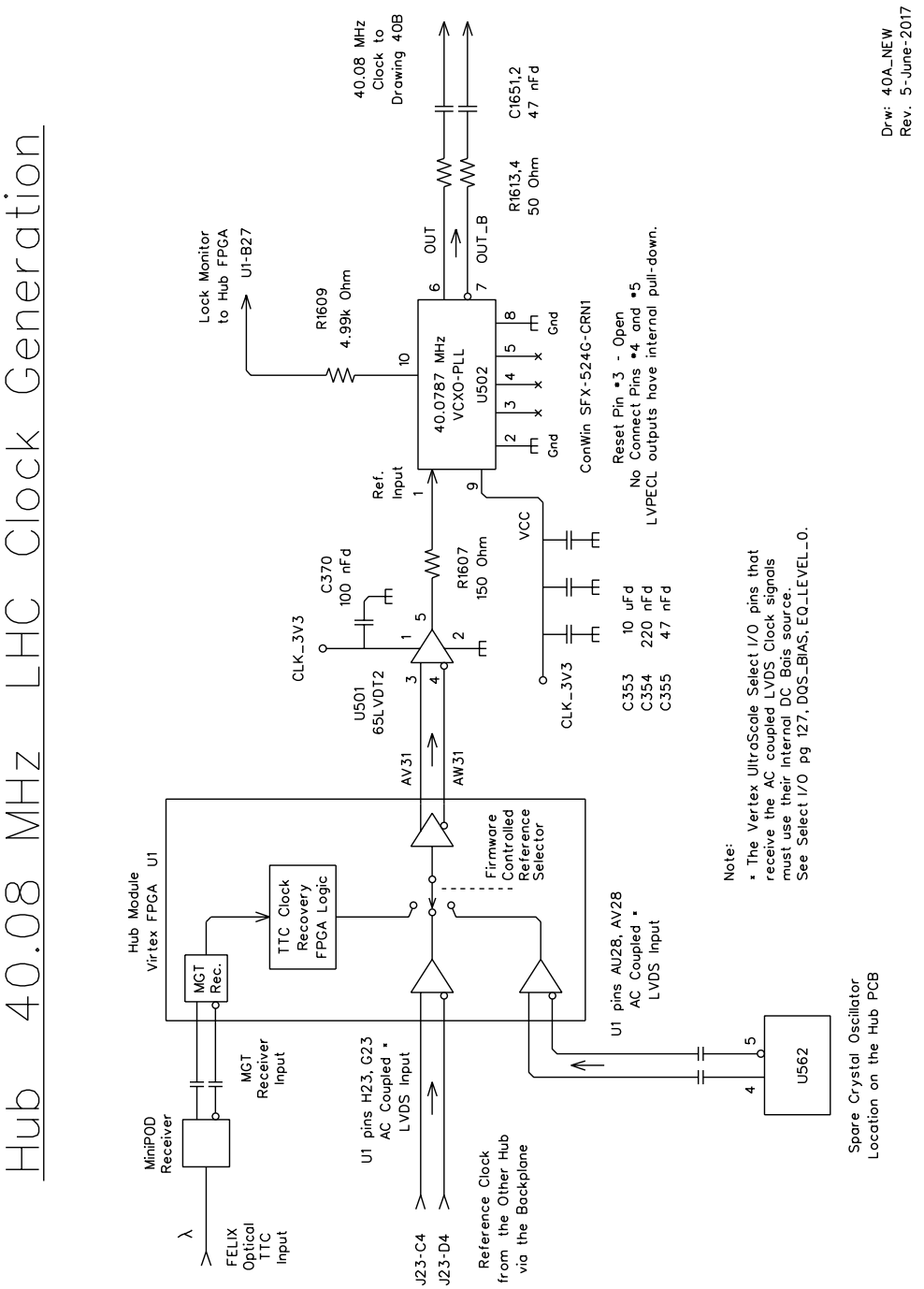

Figure 25: Circuit diagram for Hub 40.08 MHz clock distribution (1/2)

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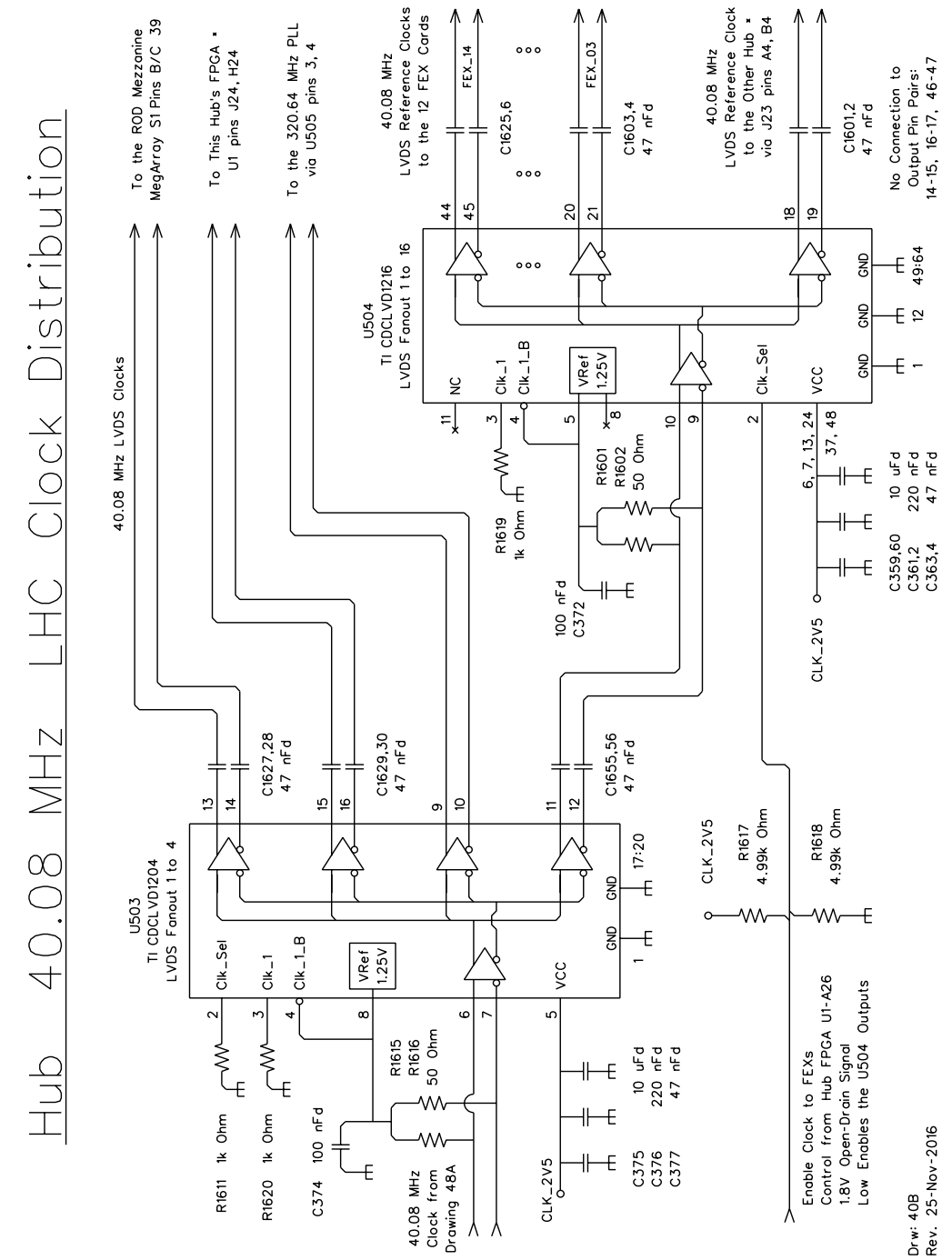

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1651 **Figure 26**: Circuit diagram for Hub 40.08 MHz clock distribution (2/2)

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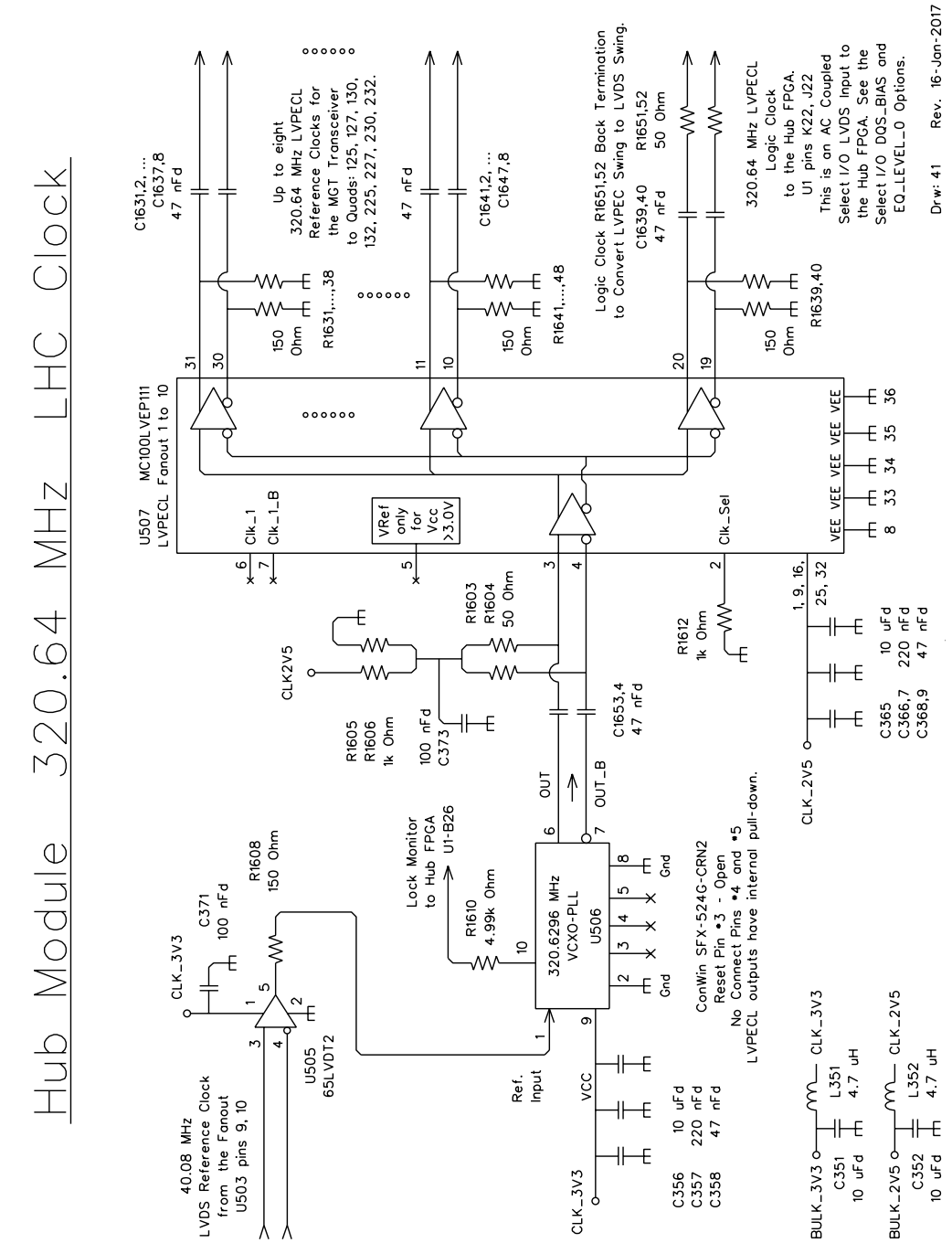

Figure 27: Circuit diagram for Hub 320 MHz clock generation.

17 Appendix 4: Hub-Module Ethernet Line Circuits

This note describes the "line circuits" on the Hub Module that connect its various Ethernet components to the twisted pair lines that run from the card. Here I used "twisted pair" to mean both the ATCA Base Interface Ethernet links and the front panel RJ-45 unshielded twisted pair cable (UTP cable) Ethernet links. The standard transformer coupled Ethernet line circuits are often referred to in engineering slang as "Ethernet magnetics". A circuit diagram is shown in **Figure 28**.

The very end of this note describes the capacitor coupled Ethernet line circuits that are used for the Ethernet connections that have both ends on the same Hub Module.

17.1 Transformer Coupled Ethernet Line Circuits

At the Ethernet physical layer the Hub Module has three different types of devices that must connect to standard transformer coupled Ethernet line circuits:

- 17 line circuits to Broadcom BCM53128 Switch ports.
- 13 of these run to the backplane Zone 2 Base Interface.
- 4 of these run to the front panel RJ-45s.
- 1 line circuit to the Micrel KSZ9031RNX Phys Chip for this Hub's Virtex FPGA. This circuit runs to the backplane Zone 2 Base Interface.
- 1 line circuit to the Micrel KSZ9031RNX Phys Chip for the ROD Virtex FPGA on this Hub card. This circuit runs to a front panel RJ-45 connector.
- 1 line circuit to the TI DP83848C Phys Chip on the IPMC mezzanine module. This circuit runs to a front panel RJ-45 connector.

Both modern voltage mode and older current mode connections to the Ethernet line circuits are used on the Hub Module. The Broadcom BCM53128 and the Micrel KSZ9031RNX are voltage mode devices. The TI DP83848C Phys Chip in the IPMC is a current mode device.

The Ethernet line circuit for the IPMC has the added complication that currently it is a 10/100 Base-T only connection but in the future the IPMC may be supplied as a 10/100/1000 Base-T device that will use 2 additional circuits and will presumable be a voltage mode device.

The "magnetics" used on the Hub Module is a SMD device that holds 8 circuits per device, i.e. 2 complete 10/100/1000 Base-T connections per device. It is a Pulse Engineering HX5201NL part that can operate over the -40 to +85 deg. C temperature range. The HX5201NL is of the recommended topology with its isolation transformer next to the Phys port and its common mode choke next to its line port. This is a so called "8 core" per Ethernet connection device and has a 3 wire common mode choke that can be used with Power Over Ethernet.

17.2 Phys Side Connections

The connection to the Phys side of the magnetics is different for voltage mode and current mode devices.

- The voltage mode Phys devices connect to the two outer primary side transformer terminals on each circuit and the primary center tap is tied to logic ground through a 100 nFd capacitor.
- The current mode Phys device connects to the two outer primary side transformer terminals as above. In addition each terminal on the Phys has a 50 Ohm resistor that runs to Vcc which is 3.3 Volts for the the DP83848C device on the IPMC. These 50 Ohm resistors are located on the IPMC mezzanine. The Vcc side of these resistors must be bypassed to ground. In addition the center tap of the transformer primary must be bypassed to ground with a 100 nFd cap and tied to Vcc, i.e. 3.3 Volts for the DP83848C device.
- So the difference in these circuits on the Hub Module needs to be the inclusion of a jumper from the transformer primary center tap to the 3.3 Volt plane for any circuits that may need to operate in current mode, i.e. the IPMC A/Tx B/Rx circuits.

17.3 Line Side Connections

In the Hub application (which does not have Power Over Ethernet) the line side of the magnetics is tied to a front panel RJ-45 connector or to a Zone 2 Base Interface connection paying attention to the required strange pinout of the B and "C" circuits in the RJ-45 connector. The center tap of the line side common mode choke is tied to ground through a Bob Smith termination (patented by Robert W. Smith).

The intent of this termination of to absorb common mode energy in the line side circuit and thus to help reduce the radiation of this energy. This termination consists of a 75 Ohm series resistor from the common mode choke choke center tap in each of the 4 circuits in a given Ethernet connection. The far side of these 4 resistors are tied together and then tied to ground through a 1 nFd capacitor.

For the Base Interface Ethernet connections the ground that this 1 nFd cap is tied to should clearly be the Logic Ground. For the front panel RJ-45 links one could argue that the 1 nFd cap should be tied to the Shelf ground or to the Logic Ground. Being an ATCA card the Hub Module has only a single pin Zone 1 connection to the Shelf Ground and thus this ground connection is likely to be noisy and not a very stiff ground point. Thus for the Hub's front panel RJ-45 Ethernet connections the 1 nFd Bob Smith capacitor is tied to Logic Ground.

17.4 Ethernet Magnetics Connection Summary

In summary, each Ethernet connection (4 circuits) requires the following passive components:

- 4x 100 nFd caps from the trans pri center tap to gnd
- 2x zero Ohm jumpers to 3V3 for current mode Tx,Rx only
- 4x 75 Ohm from common mode choke sec side center tap

- 1x 1 nFd from the 75 Ohm resistors to ground

17.5 Front Panel RJ-45s

The front panel RJ-45 connectors used on the Hub Module are TE Connectivity 1888653-x 1x2 condo connectors. These are special condo connectors for ATCA because the standard height RJ-45 condo connector is too tall to fit within the ATCA side 1 component height limitation.

The TE 1888653-x connector requires a notch in the front edge of the PCB or else it will stick out to far. On the Hub Module this notch is a minimum of 16.00 mm wide (i.e the connector itself requires a 16.00 mm wide notch and to this one needs to add some clearance and router tool radius). The notch, in theory, needs to be 10.55mm deep. Using a 7.00 mm deep cutout makes a better match to how far the other components (e.g. SFP+) stick out in front of the Hub's front panel.

The Hub Module uses the 1888653-4 RJ-45 connector. This connector has the following setup of its LEDs: LEDs 1,4 are in the lower, i.e. PCB level, RJ45; LEDs 2,3 are in the upper RJ45.

As installed on our Hub card and with the long axis of the front panel vertical:

LEDs 1,2 are above their RJ45s
LEDs 3,4 are below their RJ45s.

TE Part No.	LED_1	LED_2	LED_3	LED_4
1888653-4	Green	Green	Yellow	Yellow

There are alternative versions of this connector available with different LED arrangements. The 1888653-4 version has the common Green/Yellow LEDs and is available from stock.

For the Hub's Ethernet links that do not run through front panel RJ-45 connectors, green and yellow LEDs are provided in a separate front panel LED array.

The metal cover shell around the RJ-45 connectors, which makes no electrical connection to the twisted pair cable, is tied to the Shelf Ground via its fingers that touch the front panel. In addition the Shelf Ground net is run to the pins on this connector that attach to its metal cover shell.

17.6 Capacitor Coupled Ethernet Line Circuits

There are two types of Ethernet connections on the Hub Module were both ends of the connection are on the same module. These are:

- The connections between the Broadcom BCM53128 Switch Chips: Chip A <--> Chip B <--> Chip C.
- The connection from the Micrel KSZ9031RNX Phys Chip for this Hub's Virtex FPGA to Switch Chip C on the same Hub Module.

In these cases both ends of the Ethernet connection are on the same Hub Module and operate with the same ground planes. Thus we do not have a large concern about common mode signals on these links.

To save circuit board space capacitor coupling can be used on these links. Both of these devices have modern voltage mode physical layer transmitters which makes it much easier to use capacitor coupling.

Specific information about using capacitor coupling with the Broadcom BCM53128 Switch Chip is given on page 29 of the BCM53128 "Layout and Design Guide" including an example of capacitor coupling it to a different LDAC Phys device. Also see the Broadcom note CAP-AN102 "Capacitive Coupling 10/100/1000 Base-T Ethernet Chip-to-Chip and Backplane Applications".

Information from Micrel about using capacitor coupling is given in their application note AN-120.

17.7 Assignment of Ethernet "Magnetics"

The Pulse Engineering HX5201NL "magnetics" that are used on the Hub have 2 full Ethernet port (i.e. 8 circuits) per module. They are assigned to the various Line Circuits in the following way:

Ref. Desig.	Mag Sect	Usage
TRNS1	Left	RJ1 Lower This Hub's ROD
	Right	RJ1 Upper This Hub's IPMC
TRNS2	Left	RJ2 Lower Switch Chip "A" Port 6
	Right	RJ2 Upper Switch Chip "C" Port 6
TRNS3	Left	RJ3 Lower Switch Chip "B" Port 6
	Right	RJ3 Upper Switch Chip "B" Port 7
TRNS4	Left	This Hub's FPGA Phy U21 J20 Rw 3&4 to Other Hub Sw
	Right	Chip B Port 5 BI Ch 2 J20 Rw 3&4 to Other Hub FPGA
TRNS5	Left	Chip C Port 5 BI Ch 3 J23 Rw 7 to Slot 3 FEX
	Right	Chip C Port 4 BI Ch 4 J23 Rw 8 to Slot 4 FEX
TRNS6	Left	Chip C Port 3 BI Ch 5 J23 Rw 9 to Slot 5 FEX
	Right	Chip C Port 2 BI Ch 6 J23 Rw 10 to Slot 6 FEX

TRNS7	Left Right	Chip C Port 1 BI Ch 7 J24 Rw 1 to Slot 7 FEX Chip C Port 0 BI Ch 8 J24 Rw 2 to Slot 8 FEX
TRNS8	Left Right	Chip A Port 5 BI Ch 9 J24 Rw 3 to Slot 9 FEX Chip A Port 4 BI Ch 10 J24 Rw 4 to Slot 10 FEX
TRNS9	Left Right	Chip A Port 3 BI Ch 11 J24 Rw 5 to Slot 11 FEX Chip A Port 2 BI Ch 12 J24 Rw 6 to Slot 12 FEX
TRNS10	Left Right	Chip A Port 1 BI Ch 13 J24 Rw 7 to Slot 13 FEX Chip A Port 0 BI Ch 14 J24 Rw 8 to Slot 14 FEX

17.8 Assignment of Front Panel RJ-45 Connectors

The TE 1888653-x condo RJ-45 connector that are used on the front panel of the Hub Module are assigned in the following way:

Ref Desig	Connector	Usage
RJ1	Lower or Left Upper or Right	This Hub's ROD This Hub's IPMC
RJ2	Lower or Left Upper or Right	Switch Chip "A" Port 6 Switch Chip "C" Port 6
RJ3	Lower or Left Upper or Right	Switch Chip "B" Port 6 Switch Chip "B" Port 7

When viewed from the front with the card plugged into a crate and the long axis of its front panel vertical,then RJ1 is nearest the top of the Hub and RJ3 is nearest the bottom edge of the card.

17.9 Document / Verify the ROD's RJ45 Ethernet Connection

The ethernet connections on the ROD mezzanine card shown below come from pages 3 and 20 of the 4-Sept-2015 ROD print set.

ROD's Ethernet			Hub Magnetics and RJ45 for the ROD			
				TRNS1 Magnetics		Front Panel
ROD Net Name	U11 KSZ9031 Pin No.	MegArray S1 Pin No.	MegArray S1 Pin No.	Primary Pin No.	Secondary Pin No.	RJ45 Pin No.
TxRxA_P	2	S1-B29	S1-B29	L3	L9	2
TxRxA_N	3	S1-C29	S1-C29	L1	L7	1
TxRxB_P	5	S1-B31	S1-B31	L6	L12	6
TxRxB_N	6	S1-C31	S1-C31	L4	L10	3
TxRxC_P	7	S1-B33	S1-B33	L22	L16	5

TxRxC_N	8	S1-C33	S1-C33	L24	L18	4
TxRxD_P	10	S1-B35	S1-B35	L19	L13	8
TxRxD_N	11	S1-C35	S1-C35	L21	L15	7

For the ROD application (which is a Voltage Mode Phys Chip) the magnetics primary center tap has a 100 nFd capacitor to ground and the secondary center tap has a "Bob Jones" 50 Ohm 1 nFd in series to ground. Note as currently layed out it looks like all 4 pairs are inverted.

17.10 Document / Verify the IPMC's RJ45 Ethernet Connection

The current IPMC mezzanine supports 10/100 Mbits/sec Ethernet using a National/Texas DP83848C 10/100 Base-T Phys chip. This Phys chip has an old type Current Mode transmitter connection to the magnetics. The Hub must include jumpers so that it can support either the current IPMC or a future version of the IPMC with a 1000 Base-T Phys chip that would use a Voltage Mode connection the magnetics primary. The IPMC pinout includes pins for all 4 pairs in the standard contemporary Base-T Ethernet.

IPMC Mezzanine		Hub Magnetics and RJ45 for the IPMC			
			TRNS1 Magnetics		
IPMC Net Name	IPMC Pin No.	Hub IPMC Socket Pin No.	Primary Pin No.	Secondary Pin No.	Front Panel RJ45 Pin No.
Gb_A+ / Eth_Tx+	171	171	R1	R7	1
Gb_A- / Eth_Tx-	172	172	R3	R9	2
Gb_B+ / Eth_Rx+	174	174	R4	R10	3
Gb_B- / Eth_Rx-	175	175	R6	R12	6
Gb_C+	177	177	R24	R18	4
Gb_C-	178	178	R22	R16	5
Gb_D+	180	180	R21	R15	7
Gb_D-	181	181	R19	R13	8

For the IPMC application (which is currently a Current Mode Phys Chip but could be a Voltage Mode Phys Chip in the future) the magnetics primary center tap has a 100 nFd capacitor to ground and the primary center tap for circuits A (Tx) and B (Rx) also have a 0603 jumpers to the BULK_3V3 supply. All of the secondary center taps have a "Bob Jones" 50 Ohm 1 nFd in series to ground.

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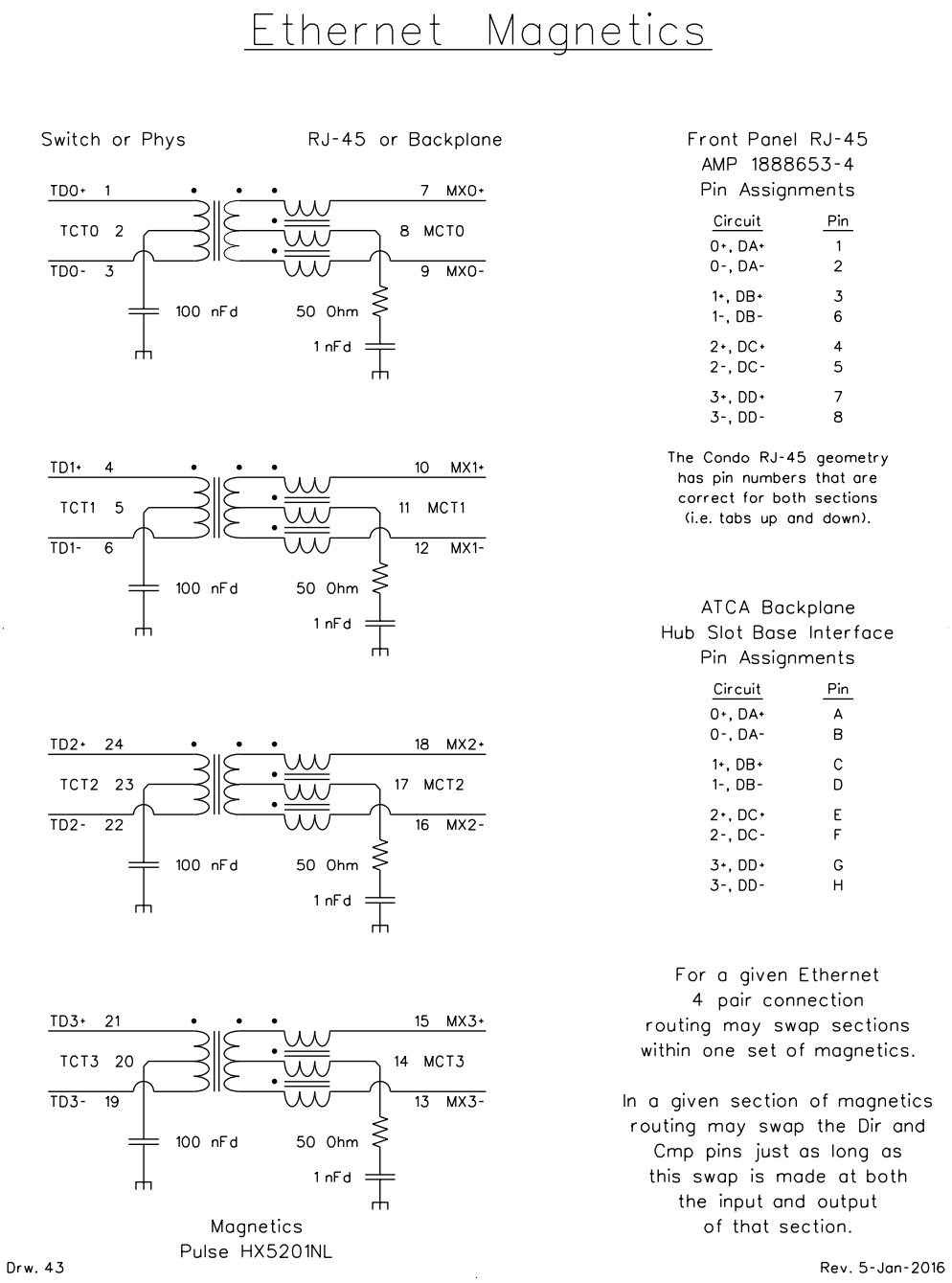

Figure 28: Circuit diagram for Hub Ethernet magnetics design.

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18 Appendix 5: Hub Virtex FPGA MGT Transceiver Usage

A significant number of MGT Transceivers are used on the Hub Module's Virtex FPGA. The intent of this document is to describe in a single place all of the MGT Transceiver connections to this FPGA. These connections are described in the text of this section, the associated tables, and in **Figure 29**, **Figure 30**, and **Figure 31**. Notes:

- The xcvu125_flvc2104 FPGA on the Hub Module contains 80 MGT Transceivers. 40 of these are GTY type transceivers and 40 of them are GTH type transceivers.
- Both the GTY and GTH type transceivers are split across the two Super-Logic-Region pieces of silcon in the xcvu125_flvc2104 FPGA. Half of each transceiver type is in each of the two Super-Logic-Regions.
- Note that MGT Reference Clocks can NOT be shared across Super-Logic-Regions.
- All 80 of the MGT Receivers are used in the Hub Module design.
  - The specific MGT Receiver used for a given application has been selected on the bases of providing the best PCB trace routing.
- Only 30 of the MGT Transmitters are used in the Hub design.
  - Again PCB trace routing was the bases for selecting a given MGT Transmitter for a specific application. In general this means that the MGT Transmitters with pins nearer the perimeter were selected for use.
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The following tables liss only the MGT Transceiver inputs and outputs. The Reference Clock inputs and the MGTAVTTRCAL_LC and MGTRREF_LC pins are listed in a separate table at the end of this section.

Pin/Quad	Pin Name	I/O Type	Super Logic Reg.	Hub Module Net Connection
GTY Quad 133:				
A36	MGTYTXP3_133	GTY	1	'Comb_Data_to_Cap_to_FEX_08_Dir'
A37	MGTYTXN3_133	GTY	1	'Comb_Data_to_Cap_to_FEX_08_Cmp'
B38	MGTYTXP2_133	GTY	1	'Comb_Data_to_Cap_to_FEX_07_Dir'
B39	MGTYTXN2_133	GTY	1	'Comb_Data_to_Cap_to_FEX_07_Cmp'
C36	MGTYTXP1_133	GTY	1	
C37	MGTYTXN1_133	GTY	1	
D38	MGTYTXP0_133	GTY	1	
D39	MGTYTXN0_133	GTY	1	
A31	MGTYRXP3_133	GTY	1	'MGT_FO_CH_37_OUT_Hub_DIR'
A32	MGTYRXN3_133	GTY	1	'MGT_FO_CH_37_OUT_Hub_CMP'
B33	MGTYRXP2_133	GTY	1	'MGT_FO_CH_38_OUT_Hub_DIR'
B34	MGTYRXN2_133	GTY	1	'MGT_FO_CH_38_OUT_Hub_CMP'
C31	MGTYRXP1_133	GTY	1	'MGT_FO_CH_39_OUT_Hub_CMP'
C32	MGTYRXN1_133	GTY	1	'MGT_FO_CH_39_OUT_Hub_DIR'
D33	MGTYRXP0_133	GTY	1	'MGT_FO_CH_40_OUT_Hub_DIR'
D34	MGTYRXN0_133	GTY	1	'MGT_FO_CH_40_OUT_Hub_CMP'
GTY Quad 132:				

A40	MGTYTXP3_132	GTY	1	'Comb_Data_to_Cap_to_FEX_06_Dir'
A41	MGTYTXN3_132	GTY	1	'Comb_Data_to_Cap_to_FEX_06_Cmp'
C40	MGTYTXP2_132	GTY	1	
C41	MGTYTXN2_132	GTY	1	
E36	MGTYTXP1_132	GTY	1	
E37	MGTYTXN1_132	GTY	1	
E40	MGTYTXP0_132	GTY	1	
E41	MGTYTXN0_132	GTY	1	
B43	MGTYRXP3_132	GTY	1	'MGT_FO_CH_25_OUT_Hub_CMP'
B44	MGTYRXN3_132	GTY	1	'MGT_FO_CH_25_OUT_Hub_DIR'
C45	MGTYRXP2_132	GTY	1	'MGT_FO_CH_26_OUT_Hub_DIR'
C46	MGTYRXN2_132	GTY	1	'MGT_FO_CH_26_OUT_Hub_CMP'
D43	MGTYRXP1_132	GTY	1	'MGT_FO_CH_27_OUT_Hub_CMP'
D44	MGTYRXN1_132	GTY	1	'MGT_FO_CH_27_OUT_Hub_DIR'
E45	MGTYRXP0_132	GTY	1	'MGT_FO_CH_28_OUT_Hub_DIR'
E46	MGTYRXN0_132	GTY	1	'MGT_FO_CH_28_OUT_Hub_CMP'
GTY Quad 131:				
F34	MGTYTXP3_131	GTY	1	
F35	MGTYTXN3_131	GTY	1	
G36	MGTYTXP2_131	GTY	1	
G37	MGTYTXN2_131	GTY	1	
F38	MGTYTXP1_131	GTY	1	
F39	MGTYTXN1_131	GTY	1	
G40	MGTYTXP0_131	GTY	1	
G41	MGTYTXN0_131	GTY	1	
E31	MGTYRXP3_131	GTY	1	'MGT_FO_CH_35_OUT_Hub_CMP'
E32	MGTYRXN3_131	GTY	1	'MGT_FO_CH_35_OUT_Hub_DIR'
G31	MGTYRXP2_131	GTY	1	'MGT_FO_CH_36_OUT_Hub_DIR'
G32	MGTYRXN2_131	GTY	1	'MGT_FO_CH_36_OUT_Hub_CMP'
F43	MGTYRXP1_131	GTY	1	'MGT_FO_CH_29_OUT_Hub_CMP'
F44	MGTYRXN1_131	GTY	1	'MGT_FO_CH_29_OUT_Hub_DIR'
G45	MGTYRXP0_131	GTY	1	'MGT_FO_CH_30_OUT_Hub_DIR'
G46	MGTYRXN0_131	GTY	1	'MGT_FO_CH_30_OUT_Hub_CMP'
GTY Quad 130:				
H38	MGTYTXP3_130	GTY	1	
H39	MGTYTXN3_130	GTY	1	
J40	MGTYTXP2_130	GTY	1	'Comb_Data_to_Cap_to_FEX_05_Dir'
J41	MGTYTXN2_130	GTY	1	'Comb_Data_to_Cap_to_FEX_05_Cmp'
K38	MGTYTXP1_130	GTY	1	
K39	MGTYTXN1_130	GTY	1	
L40	MGTYTXP0_130	GTY	1	'Comb_Data_to_Cap_to_FEX_04_Dir'
L41	MGTYTXN0_130	GTY	1	'Comb_Data_to_Cap_to_FEX_04_Cmp'
H43	MGTYRXP3_130	GTY	1	'MGT_FO_CH_31_OUT_Hub_CMP'
H44	MGTYRXN3_130	GTY	1	'MGT_FO_CH_31_OUT_Hub_DIR'
J45	MGTYRXP2_130	GTY	1	'MGT_FO_CH_32_OUT_Hub_DIR'
J46	MGTYRXN2_130	GTY	1	'MGT_FO_CH_32_OUT_Hub_CMP'
K43	MGTYRXP1_130	GTY	1	'MGT_FO_CH_17_OUT_Hub_CMP'
K44	MGTYRXN1_130	GTY	1	'MGT_FO_CH_17_OUT_Hub_DIR'
L45	MGTYRXP0_130	GTY	1	'MGT_FO_CH_18_OUT_Hub_DIR'
L46	MGTYRXN0_130	GTY	1	'MGT_FO_CH_18_OUT_Hub_CMP'
GTY Quad 129:				

M38	MGTYTXP3_129	GTY	1	
M39	MGTYTXN3_129	GTY	1	
N40	MGTYTXP2_129	GTY	1	'Comb_Data_to_Cap_to_FEX_03_Dir'
N41	MGTYTXN2_129	GTY	1	'Comb_Data_to_Cap_to_FEX_03_Cmp'
P38	MGTYTXP1_129	GTY	1	
P39	MGTYTXN1_129	GTY	1	
R40	MGTYTXP0_129	GTY	1	'Comb_Data_to_Cap_to_Other_Hub_Dir'
R41	MGTYTXN0_129	GTY	1	'Comb_Data_to_Cap_to_Other_Hub_Cmp'
M43	MGTYRXP3_129	GTY	1	'MGT_FO_CH_19_OUT_Hub_CMP'
M44	MGTYRXN3_129	GTY	1	'MGT_FO_CH_19_OUT_Hub_DIR'
N45	MGTYRXP2_129	GTY	1	'MGT_FO_CH_20_OUT_Hub_DIR'
N46	MGTYRXN2_129	GTY	1	'MGT_FO_CH_20_OUT_Hub_CMP'
P43	MGTYRXP1_129	GTY	1	'MGT_FO_CH_21_OUT_Hub_CMP'
P44	MGTYRXN1_129	GTY	1	'MGT_FO_CH_21_OUT_Hub_DIR'
R45	MGTYRXP0_129	GTY	1	'MGT_FO_CH_22_OUT_Hub_DIR'
R46	MGTYRXN0_129	GTY	1	'MGT_FO_CH_22_OUT_Hub_CMP'
GTY Quad 128:				
T38	MGTYTXP3_128	GTY	0	
T39	MGTYTXN3_128	GTY	0	
U40	MGTYTXP2_128	GTY	0	
U41	MGTYTXN2_128	GTY	0	
V38	MGTYTXP1_128	GTY	0	
V39	MGTYTXN1_128	GTY	0	
W40	MGTYTXP0_128	GTY	0	
W41	MGTYTXN0_128	GTY	0	
T43	MGTYRXP3_128	GTY	0	'MGT_FO_CH_23_OUT_Hub_CMP'
T44	MGTYRXN3_128	GTY	0	'MGT_FO_CH_23_OUT_Hub_DIR'
U45	MGTYRXP2_128	GTY	0	'MGT_FO_CH_24_OUT_Hub_DIR'
U46	MGTYRXN2_128	GTY	0	'MGT_FO_CH_24_OUT_Hub_CMP'
V43	MGTYRXP1_128	GTY	0	'MGT_FO_CH_09_OUT_Hub_CMP'
V44	MGTYRXN1_128	GTY	0	'MGT_FO_CH_09_OUT_Hub_DIR'
W45	MGTYRXP0_128	GTY	0	'MGT_FO_CH_10_OUT_Hub_DIR'
W46	MGTYRXN0_128	GTY	0	'MGT_FO_CH_10_OUT_Hub_CMP'
GTY Quad 127:				
Y38	MGTYTXP3_127	GTY	0	
Y39	MGTYTXN3_127	GTY	0	
AA40	MGTYTXP2_127	GTY	0	'This_Hubs_RO_0_to_Cap_Other_ROD_Dir'
AA41	MGTYTXN2_127	GTY	0	'This_Hubs_RO_0_to_Cap_Other_ROD_Cmp'
AB38	MGTYTXP1_127	GTY	0	
AB39	MGTYTXN1_127	GTY	0	
AC40	MGTYTXP0_127	GTY	0	'This_Hubs_RO_1_to_Cap_Other_ROD_Cmp'
AC41	MGTYTXN0_127	GTY	0	'This_Hubs_RO_1_to_Cap_Other_ROD_Dir'
Y43	MGTYRXP3_127	GTY	0	'MGT_FO_CH_11_OUT_Hub_CMP'
Y44	MGTYRXN3_127	GTY	0	'MGT_FO_CH_11_OUT_Hub_DIR'
AA45	MGTYRXP2_127	GTY	0	'MGT_FO_CH_12_OUT_Hub_DIR'
AA46	MGTYRXN2_127	GTY	0	'MGT_FO_CH_12_OUT_Hub_CMP'
AB43	MGTYRXP1_127	GTY	0	'MGT_FO_CH_13_OUT_Hub_CMP'
AB44	MGTYRXN1_127	GTY	0	'MGT_FO_CH_13_OUT_Hub_DIR'
AC45	MGTYRXP0_127	GTY	0	'MGT_FO_CH_14_OUT_Hub_DIR'
AC46	MGTYRXN0_127	GTY	0	'MGT_FO_CH_14_OUT_Hub_CMP'
GTY Quad 126:				

AD38	MGTYTXP3_126	GTY	0	
AD39	MGTYTXN3_126	GTY	0	
AE40	MGTYTXP2_126	GTY	0	
AE41	MGTYTXN2_126	GTY	0	
AF38	MGTYTXP1_126	GTY	0	
AF39	MGTYTXN1_126	GTY	0	
AG40	MGTYTXP0_126	GTY	0	
AG41	MGTYTXN0_126	GTY	0	
AD43	MGTYRXP3_126	GTY	0	'MGT_FO_CH_15_OUT_Hub_CMP'
AD44	MGTYRXN3_126	GTY	0	'MGT_FO_CH_15_OUT_Hub_DIR'
AE45	MGTYRXP2_126	GTY	0	'MGT_FO_CH_16_OUT_Hub_DIR'
AE46	MGTYRXN2_126	GTY	0	'MGT_FO_CH_16_OUT_Hub_CMP'
AF43	MGTYRXP1_126	GTY	0	'MGT_FO_CH_01_OUT_Hub_CMP'
AF44	MGTYRXN1_126	GTY	0	'MGT_FO_CH_01_OUT_Hub_DIR'
AG45	MGTYRXP0_126	GTY	0	'MGT_FO_CH_02_OUT_Hub_DIR'
AG46	MGTYRXN0_126	GTY	0	'MGT_FO_CH_02_OUT_Hub_CMP'
GTY Quad 125:				
AH38	MGTYTXP3_125	GTY	0	
AH39	MGTYTXN3_125	GTY	0	
AJ40	MGTYTXP2_125	GTY	0	
AJ41	MGTYTXN2_125	GTY	0	
AK38	MGTYTXP1_125	GTY	0	
AK39	MGTYTXN1_125	GTY	0	
AL40	MGTYTXP0_125	GTY	0	
AL41	MGTYTXN0_125	GTY	0	
AH43	MGTYRXP3_125	GTY	0	'MGT_FO_CH_03_OUT_Hub_CMP'
AH44	MGTYRXN3_125	GTY	0	'MGT_FO_CH_03_OUT_Hub_DIR'
AJ45	MGTYRXP2_125	GTY	0	'MGT_FO_CH_04_OUT_Hub_DIR'
AJ46	MGTYRXN2_125	GTY	0	'MGT_FO_CH_04_OUT_Hub_CMP'
AK43	MGTYRXP1_125	GTY	0	'MGT_FO_CH_05_OUT_Hub_CMP'
AK44	MGTYRXN1_125	GTY	0	'MGT_FO_CH_05_OUT_Hub_DIR'
AL45	MGTYRXP0_125	GTY	0	'MGT_FO_CH_06_OUT_Hub_DIR'
AL46	MGTYRXN0_125	GTY	0	'MGT_FO_CH_06_OUT_Hub_CMP'
GTY Quad 124:				
AM38	MGTYTXP3_124	GTY	0	
AM39	MGTYTXN3_124	GTY	0	
AN40	MGTYTXP2_124	GTY	0	
AN41	MGTYTXN2_124	GTY	0	
AP38	MGTYTXP1_124	GTY	0	
AP39	MGTYTXN1_124	GTY	0	
AR40	MGTYTXP0_124	GTY	0	
AR41	MGTYTXN0_124	GTY	0	
AM43	MGTYRXP3_124	GTY	0	'MGT_FO_CH_07_OUT_Hub_CMP'
AM44	MGTYRXN3_124	GTY	0	'MGT_FO_CH_07_OUT_Hub_DIR'
AN45	MGTYRXP2_124	GTY	0	'MGT_FO_CH_08_OUT_Hub_DIR'
AN46	MGTYRXN2_124	GTY	0	'MGT_FO_CH_08_OUT_Hub_CMP'
AP43	MGTYRXP1_124	GTY	0	'Combined_Data_from_OTHER_Hub_Cmp'
AP44	MGTYRXN1_124	GTY	0	'Combined_Data_from_OTHER_Hub_Dir'
AR45	MGTYRXP0_124	GTY	0	'Rec_MP_Fiber_8_to_FPGA_Dir'
AR46	MGTYRXN0_124	GTY	0	'Rec_MP_Fiber_8_to_FPGA_Cmp'

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Pin/Quad	Pin Name	I/O Type	Super Logic Reg.	Hub Module Net Connection
GTH Quad 233:				
A11	MGTHTXP3_233	GTH	1	'Comb_Data_to_Cap_to_FEX_09_Cmp'
A10	MGTHTXN3_233	GTH	1	'Comb_Data_to_Cap_to_FEX_09_Dir'
B9	MGTHTXP2_233	GTH	1	'Comb_Data_to_Cap_to_FEX_10_Cmp'
B8	MGTHTXN2_233	GTH	1	'Comb_Data_to_Cap_to_FEX_10_Dir'
C11	MGTHTXP1_233	GTH	1	
C10	MGTHTXN1_233	GTH	1	
D9	MGTHTXP0_233	GTH	1	
D8	MGTHTXN0_233	GTH	1	
A16	MGTHRXP3_233	GTH	1	'MGT_FO_CH_48_OUT_Hub_DIR'
A15	MGTHRXN3_233	GTH	1	'MGT_FO_CH_48_OUT_Hub_CMP'
B14	MGTHRXP2_233	GTH	1	'MGT_FO_CH_47_OUT_Hub_DIR'
B13	MGTHRXN2_233	GTH	1	'MGT_FO_CH_47_OUT_Hub_CMP'
C16	MGTHRXP1_233	GTH	1	'MGT_FO_CH_46_OUT_Hub_CMP'
C15	MGTHRXN1_233	GTH	1	'MGT_FO_CH_46_OUT_Hub_DIR'
D14	MGTHRXP0_233	GTH	1	'MGT_FO_CH_45_OUT_Hub_DIR'
D13	MGTHRXN0_233	GTH	1	'MGT_FO_CH_45_OUT_Hub_CMP'
GTH Quad 232:				
A7	MGTHTXP3_232	GTH	1	'Comb_Data_to_Cap_to_FEX_11_Cmp'
A6	MGTHTXN3_232	GTH	1	'Comb_Data_to_Cap_to_FEX_11_Dir'
C7	MGTHTXP2_232	GTH	1	
C6	MGTHTXN2_232	GTH	1	
E11	MGTHTXP1_232	GTH	1	
E10	MGTHTXN1_232	GTH	1	
E7	MGTHTXP0_232	GTH	1	
E6	MGTHTXN0_232	GTH	1	
B4	MGTHRXP3_232	GTH	1	'MGT_FO_CH_44_OUT_Hub_CMP'
B3	MGTHRXN3_232	GTH	1	'MGT_FO_CH_44_OUT_Hub_DIR'
C2	MGTHRXP2_232	GTH	1	'MGT_FO_CH_43_OUT_Hub_DIR'
C1	MGTHRXN2_232	GTH	1	'MGT_FO_CH_43_OUT_Hub_CMP'
D4	MGTHRXP1_232	GTH	1	'MGT_FO_CH_42_OUT_Hub_CMP'
D3	MGTHRXN1_232	GTH	1	'MGT_FO_CH_42_OUT_Hub_DIR'
E2	MGTHRXP0_232	GTH	1	'MGT_FO_CH_41_OUT_Hub_DIR'
E1	MGTHRXN0_232	GTH	1	'MGT_FO_CH_41_OUT_Hub_CMP'
GTH Quad 231:				
F13	MGTHTXP3_231	GTH	1	
F12	MGTHTXN3_231	GTH	1	
G11	MGTHTXP2_231	GTH	1	
G10	MGTHTXN2_231	GTH	1	
F9	MGTHTXP1_231	GTH	1	
F8	MGTHTXN1_231	GTH	1	
G7	MGTHTXP0_231	GTH	1	
G6	MGTHTXN0_231	GTH	1	
E16	MGTHRXP3_231	GTH	1	'MGT_FO_CH_34_OUT_Hub_CMP'

E15	MGTHRXN3_231	GTH	1	'MGT_FO_CH_34_OUT_Hub_DIR'
G16	MGTHRXP2_231	GTH	1	'MGT_FO_CH_33_OUT_Hub_DIR'
G15	MGTHRXN2_231	GTH	1	'MGT_FO_CH_33_OUT_Hub_CMP'
F4	MGTHRXP1_231	GTH	1	'MGT_FO_CH_56_OUT_Hub_CMP'
F3	MGTHRXN1_231	GTH	1	'MGT_FO_CH_56_OUT_Hub_DIR'
G2	MGTHRXP0_231	GTH	1	'MGT_FO_CH_55_OUT_Hub_DIR'
G1	MGTHRXN0_231	GTH	1	'MGT_FO_CH_55_OUT_Hub_CMP'
GTH Quad 230:				
H9	MGTHTXP3_230	GTH	1	
H8	MGTHTXN3_230	GTH	1	
J7	MGTHTXP2_230	GTH	1	'Comb_Data_to_Cap_to_FEX_12_Cmp'
J6	MGTHTXN2_230	GTH	1	'Comb_Data_to_Cap_to_FEX_12_Dir'
K9	MGTHTXP1_230	GTH	1	
K8	MGTHTXN1_230	GTH	1	
L7	MGTHTXP0_230	GTH	1	'Comb_Data_to_Cap_to_FEX_13_Cmp'
L6	MGTHTXN0_230	GTH	1	'Comb_Data_to_Cap_to_FEX_13_Dir'
H4	MGTHRXP3_230	GTH	1	'MGT_FO_CH_54_OUT_Hub_CMP'
H3	MGTHRXN3_230	GTH	1	'MGT_FO_CH_54_OUT_Hub_DIR'
J2	MGTHRXP2_230	GTH	1	'MGT_FO_CH_53_OUT_Hub_DIR'
J1	MGTHRXN2_230	GTH	1	'MGT_FO_CH_53_OUT_Hub_CMP'
K4	MGTHRXP1_230	GTH	1	'MGT_FO_CH_52_OUT_Hub_CMP'
K3	MGTHRXN1_230	GTH	1	'MGT_FO_CH_52_OUT_Hub_DIR'
L2	MGTHRXP0_230	GTH	1	'MGT_FO_CH_51_OUT_Hub_DIR'
L1	MGTHRXN0_230	GTH	1	'MGT_FO_CH_51_OUT_Hub_CMP'
GTH Quad 229:				
M9	MGTHTXP3_229	GTH	1	
M8	MGTHTXN3_229	GTH	1	
N7	MGTHTXP2_229	GTH	1	'Comb_Data_to_Cap_to_FEX_14_Cmp'
N6	MGTHTXN2_229	GTH	1	'Comb_Data_to_Cap_to_FEX_14_Dir'
P9	MGTHTXP1_229	GTH	1	
P8	MGTHTXN1_229	GTH	1	
R7	MGTHTXP0_229	GTH	1	'This_Hubs_RO_0_to_Cap_Its_ROD_Dir'
R6	MGTHTXN0_229	GTH	1	'This_Hubs_RO_0_to_Cap_Its_ROD_Cmp'
M4	MGTHRXP3_229	GTH	1	'MGT_FO_CH_50_OUT_Hub_CMP'
M3	MGTHRXN3_229	GTH	1	'MGT_FO_CH_50_OUT_Hub_DIR'
N2	MGTHRXP2_229	GTH	1	'MGT_FO_CH_49_OUT_Hub_DIR'
N1	MGTHRXN2_229	GTH	1	'MGT_FO_CH_49_OUT_Hub_CMP'
P4	MGTHRXP1_229	GTH	1	'MGT_FO_CH_64_OUT_Hub_CMP'
P3	MGTHRXN1_229	GTH	1	'MGT_FO_CH_64_OUT_Hub_DIR'
R2	MGTHRXP0_229	GTH	1	'MGT_FO_CH_63_OUT_Hub_DIR'
R1	MGTHRXN0_229	GTH	1	'MGT_FO_CH_63_OUT_Hub_CMP'
GTH Quad 228:				
T9	MGTHTXP3_228	GTH	0	
T8	MGTHTXN3_228	GTH	0	
U7	MGTHTXP2_228	GTH	0	'This_Hubs_RO_1_to_Cap_Its_ROD_Dir'
U6	MGTHTXN2_228	GTH	0	'This_Hubs_RO_1_to_Cap_Its_ROD_Cmp'
V9	MGTHTXP1_228	GTH	0	
V8	MGTHTXN1_228	GTH	0	
W7	MGTHTXP0_228	GTH	0	'Comb_Data_to_Cap_to_ROD_Dir'
W6	MGTHTXN0_228	GTH	0	'Comb_Data_to_Cap_to_ROD_Cmp'
T4	MGTHRXP3_228	GTH	0	'MGT_FO_CH_62_OUT_Hub_CMP'

T3	MGTHRXN3_228	GTH	0	'MGT_FO_CH_62_OUT_Hub_DIR'
U2	MGTHRXP2_228	GTH	0	'MGT_FO_CH_61_OUT_Hub_DIR'
U1	MGTHRXN2_228	GTH	0	'MGT_FO_CH_61_OUT_Hub_CMP'
V4	MGTHRXP1_228	GTH	0	'MGT_FO_CH_60_OUT_Hub_CMP'
V3	MGTHRXN1_228	GTH	0	'MGT_FO_CH_60_OUT_Hub_DIR'
W2	MGTHRXP0_228	GTH	0	'MGT_FO_CH_59_OUT_Hub_DIR'
W1	MGTHRXN0_228	GTH	0	'MGT_FO_CH_59_OUT_Hub_CMP'
GTH Quad 227:				
Y9	MGTHTXP3_227	GTH	0	
Y8	MGTHTXN3_227	GTH	0	
AA7	MGTHTXP2_227	GTH	0	'MiniPOD_Trans_Fiber_0_Data_Cmp'
AA6	MGTHTXN2_227	GTH	0	'MiniPOD_Trans_Fiber_0_Data_Dir'
AB9	MGTHTXP1_227	GTH	0	
AB8	MGTHTXN1_227	GTH	0	
AC7	MGTHTXP0_227	GTH	0	'MiniPOD_Trans_Fiber_1_Data_Cmp'
AC6	MGTHTXN0_227	GTH	0	'MiniPOD_Trans_Fiber_1_Data_Dir'
Y4	MGTHRXP3_227	GTH	0	'MGT_FO_CH_58_OUT_Hub_CMP'
Y3	MGTHRXN3_227	GTH	0	'MGT_FO_CH_58_OUT_Hub_DIR'
AA2	MGTHRXP2_227	GTH	0	'MGT_FO_CH_57_OUT_Hub_DIR'
AA1	MGTHRXN2_227	GTH	0	'MGT_FO_CH_57_OUT_Hub_CMP'
AB4	MGTHRXP1_227	GTH	0	'MGT_FO_CH_74_OUT_Hub_CMP'
AB3	MGTHRXN1_227	GTH	0	'MGT_FO_CH_74_OUT_Hub_DIR'
AC2	MGTHRXP0_227	GTH	0	'MGT_FO_CH_73_OUT_Hub_DIR'
AC1	MGTHRXN0_227	GTH	0	'MGT_FO_CH_73_OUT_Hub_CMP'
GTH Quad 226:				
AD9	MGTHTXP3_226	GTH	0	
AD8	MGTHTXN3_226	GTH	0	
AE7	MGTHTXP2_226	GTH	0	'MiniPOD_Trans_Fiber_2_Data_Cmp'
AE6	MGTHTXN2_226	GTH	0	'MiniPOD_Trans_Fiber_2_Data_Dir'
AF9	MGTHTXP1_226	GTH	0	
AF8	MGTHTXN1_226	GTH	0	
AG7	MGTHTXP0_226	GTH	0	'MiniPOD_Trans_Fiber_4_Data_Cmp'
AG6	MGTHTXN0_226	GTH	0	'MiniPOD_Trans_Fiber_4_Data_Dir'
AD4	MGTHRXP3_226	GTH	0	'MGT_FO_CH_72_OUT_Hub_CMP'
AD3	MGTHRXN3_226	GTH	0	'MGT_FO_CH_72_OUT_Hub_DIR'
AE2	MGTHRXP2_226	GTH	0	'MGT_FO_CH_71_OUT_Hub_DIR'
AE1	MGTHRXN2_226	GTH	0	'MGT_FO_CH_71_OUT_Hub_CMP'
AF4	MGTHRXP1_226	GTH	0	'MGT_FO_CH_70_OUT_Hub_CMP'
AF3	MGTHRXN1_226	GTH	0	'MGT_FO_CH_70_OUT_Hub_DIR'
AG2	MGTHRXP0_226	GTH	0	'MGT_FO_CH_69_OUT_Hub_DIR'
AG1	MGTHRXN0_226	GTH	0	'MGT_FO_CH_69_OUT_Hub_CMP'
GTH Quad 225:				
AH9	MGTHTXP3_225	GTH	0	
AH8	MGTHTXN3_225	GTH	0	
AJ7	MGTHTXP2_225	GTH	0	'MiniPOD_Trans_Fiber_6_Data_Cmp'
AJ6	MGTHTXN2_225	GTH	0	'MiniPOD_Trans_Fiber_6_Data_Dir'
AK9	MGTHTXP1_225	GTH	0	
AK8	MGTHTXN1_225	GTH	0	
AL7	MGTHTXP0_225	GTH	0	'MiniPOD_Trans_Fiber_8_Data_Cmp'
AL6	MGTHTXN0_225	GTH	0	'MiniPOD_Trans_Fiber_8_Data_Dir'
AH4	MGTHRXP3_225	GTH	0	'MGT_FO_CH_68_OUT_Hub_CMP'

AH3	MGTHRXN3_225	GTH	0	'MGT_FO_CH_68_OUT_Hub_DIR'
AJ2	MGTHRXP2_225	GTH	0	'MGT_FO_CH_67_OUT_Hub_DIR'
AJ1	MGTHRXN2_225	GTH	0	'MGT_FO_CH_67_OUT_Hub_CMP'
AK4	MGTHRXP1_225	GTH	0	'MGT_FO_CH_66_OUT_Hub_CMP'
AK3	MGTHRXN1_225	GTH	0	'MGT_FO_CH_66_OUT_Hub_DIR'
AL2	MGTHRXP0_225	GTH	0	'MGT_FO_CH_65_OUT_Hub_DIR'
AL1	MGTHRXN0_225	GTH	0	'MGT_FO_CH_65_OUT_Hub_CMP'
GTH Quad 224:				
AM9	MGTHTXP3_224	GTH	0	
AM8	MGTHTXN3_224	GTH	0	
AN7	MGTHTXP2_224	GTH	0	'MiniPOD_Trans_Fiber_10_Data_Cmp'
AN6	MGTHTXN2_224	GTH	0	'MiniPOD_Trans_Fiber_10_Data_Dir'
AP9	MGTHTXP1_224	GTH	0	
AP8	MGTHTXN1_224	GTH	0	
AR7	MGTHTXP0_224	GTH	0	'MiniPOD_Trans_Fiber_11_Data_Cmp'
AR6	MGTHTXN0_224	GTH	0	'MiniPOD_Trans_Fiber_11_Data_Dir'
AM4	MGTHRXP3_224	GTH	0	'This_RODs_Readout_Ctrl_to_GTH_Input_Cmp'
AM3	MGTHRXN3_224	GTH	0	'This_RODs_Readout_Ctrl_to_GTH_Input_Dir'
AN2	MGTHRXP2_224	GTH	0	'Rec_MP_Fiber_2_to_FPGA_Dir'
AN1	MGTHRXN2_224	GTH	0	'Rec_MP_Fiber_2_to_FPGA_Cmp'
AP4	MGTHRXP1_224	GTH	0	'Rec_MP_Fiber_4_to_FPGA_Dir'
AP3	MGTHRXN1_224	GTH	0	'Rec_MP_Fiber_4_to_FPGA_Cmp'
AR2	MGTHRXP0_224	GTH	0	'Rec_MP_Fiber_6_to_FPGA_Dir'
AR1	MGTHRXN0_224	GTH	0	'Rec_MP_Fiber_6_to_FPGA_Cmp'

Now we list the Reference Clock inputs and the MGTAVTTRCAL_LC and MGTRREF_LC pin connections. All Quads that have MGTAVTTRCAL_LC and MGTRREF_LC pins have the appropriate resistors and supplies connected to them. In this file I'm just listing the reference designators of the MGT Termination Calibration Resistors.

Pin/Quad	Pin Name	I/O Type	Super Logic Reg.	Hub Module Net Connection
GTY Quad 133:				
H34	MGTREFCLK1P_133	GTY	1	
H35	MGTREFCLK1N_133	GTY	1	
J36	MGTREFCLK0P_133	GTY	1	
J37	MGTREFCLK0N_133	GTY	1	
GTY Quad 132:				
K34	MGTREFCLK1P_132	GTY	1	'MHZ_320.64_COPY_2_DIR'
K35	MGTREFCLK1N_132	GTY	1	'MHZ_320.64_COPY_2_CMP'
L36	MGTREFCLK0P_132	GTY	1	
L37	MGTREFCLK0N_132	GTY	1	
GTY Quad 131:				
M34	MGTREFCLK1P_131	GTY	1	
M35	MGTREFCLK1N_131	GTY	1	
N36	MGTREFCLK0P_131	GTY	1	

N37	MGTREFCLK0N_131	GTY	1	
GTY Quad 130:				
P34	MGTREFCLK1P_130	GTY	1	
P35	MGTREFCLK1N_130	GTY	1	
R36	MGTREFCLK0P_130	GTY	1	'MHZ_320.64_COPY_1_DIR'
R37	MGTREFCLK0N_130	GTY	1	'MHZ_320.64_COPY_1_CMP'
D40	MGTAVTTRCAL_LN	NA	NA	R114
D41	MGTRREF_LN	NA	NA	R114
GTY Quad 129:				
T34	MGTREFCLK1P_129	GTY	1	
T35	MGTREFCLK1N_129	GTY	1	
U36	MGTREFCLK0P_129	GTY	1	
U37	MGTREFCLK0N_129	GTY	1	
GTY Quad 128:				
V34	MGTREFCLK1P_128	GTY	0	
V35	MGTREFCLK1N_128	GTY	0	
W36	MGTREFCLK0P_128	GTY	0	
W37	MGTREFCLK0N_128	GTY	0	
GTY Quad 127:				
Y34	MGTREFCLK1P_127	GTY	0	'MHZ_320.64_COPY_3_DIR'
Y35	MGTREFCLK1N_127	GTY	0	'MHZ_320.64_COPY_3_CMP'
AA36	MGTREFCLK0P_127	GTY	0	
AA37	MGTREFCLK0N_127	GTY	0	
GTY Quad 126:				
AB34	MGTREFCLK1P_126	GTY	0	
AB35	MGTREFCLK1N_126	GTY	0	
AC36	MGTREFCLK0P_126	GTY	0	
AC37	MGTREFCLK0N_126	GTY	0	
GTY Quad 125:				
AE36	MGTREFCLK0P_125	GTY	0	'MHZ_320.64_COPY_0_DIR'
AE37	MGTREFCLK0N_125	GTY	0	'MHZ_320.64_COPY_0_CMP'
AD34	MGTREFCLK1P_125	GTY	0	
AD35	MGTREFCLK1N_125	GTY	0	
AH40	MGTAVTTRCAL_LC	NA	NA	R113
AH41	MGTRREF_LC	NA	NA	R113
GTY Quad 124:				
AF34	MGTREFCLK1P_124	GTY	0	
AF35	MGTREFCLK1N_124	GTY	0	
AG36	MGTREFCLK0P_124	GTY	0	
AG37	MGTREFCLK0N_124	GTY	0	

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Pin/Quad	Pin Name	I/O Type	Super Logic Reg.	Hub Module Net Connection
GTH Quad 233:				
H13	MGTREFCLK1P_233	GTH	1	
H12	MGTREFCLK1N_233	GTH	1	
J11	MGTREFCLK0P_233	GTH	1	
J10	MGTREFCLK0N_233	GTH	1	
GTH Quad 232:				
K13	MGTREFCLK1P_232	GTH	1	'MHZ_320.64_COPY_7_DIR'
K12	MGTREFCLK1N_232	GTH	1	'MHZ_320.64_COPY_7_CMP'
L11	MGTREFCLK0P_232	GTH	1	
L10	MGTREFCLK0N_232	GTH	1	
GTH Quad 231:				
M13	MGTREFCLK1P_231	GTH	1	
M12	MGTREFCLK1N_231	GTH	1	
N11	MGTREFCLK0P_231	GTH	1	
N10	MGTREFCLK0N_231	GTH	1	
D6	MGTRREF_RN	NA	NA	R116
D7	MGTAVTTRCAL_RN	NA	NA	R116
GTH Quad 230:				
P13	MGTREFCLK1P_230	GTH	1	
P12	MGTREFCLK1N_230	GTH	1	
R11	MGTREFCLK0P_230	GTH	1	'MHZ_320.64_COPY_8_DIR'
R10	MGTREFCLK0N_230	GTH	1	'MHZ_320.64_COPY_8_CMP'
GTH Quad 229:				
T13	MGTREFCLK1P_229	GTH	1	
T12	MGTREFCLK1N_229	GTH	1	
U11	MGTREFCLK0P_229	GTH	1	
U10	MGTREFCLK0N_229	GTH	1	
GTH Quad 228:				
V13	MGTREFCLK1P_228	GTH	0	
V12	MGTREFCLK1N_228	GTH	0	
W11	MGTREFCLK0P_228	GTH	0	
W10	MGTREFCLK0N_228	GTH	0	
GTH Quad 227:				
Y13	MGTREFCLK1P_227	GTH	0	'MHZ_320.64_COPY_6_DIR'
Y12	MGTREFCLK1N_227	GTH	0	'MHZ_320.64_COPY_6_CMP'
AA11	MGTREFCLK0P_227	GTH	0	
AA10	MGTREFCLK0N_227	GTH	0	
GTH Quad 226:				
AB13	MGTREFCLK1P_226	GTH	0	
AB12	MGTREFCLK1N_226	GTH	0	
AC11	MGTREFCLK0P_226	GTH	0	
AC10	MGTREFCLK0N_226	GTH	0	
AH6	MGTRREF_RC	NA	NA	R115

AH7	MGTAVTTRCAL_RC	NA	NA	R115
GTH Quad 225:				
AD13	MGTREFCLK1P_225	GTH	0	
AD12	MGTREFCLK1N_225	GTH	0	
AE11	MGTREFCLK0P_225	GTH	0	'MHZ_320.64_COPY_9_DIR'
AE10	MGTREFCLK0N_225	GTH	0	'MHZ_320.64_COPY_9_CMP'
GTH Quad 224:				
AF13	MGTREFCLK1P_224	GTH	0	
AF12	MGTREFCLK1N_224	GTH	0	
AG11	MGTREFCLK0P_224	GTH	0	
AG10	MGTREFCLK0N_224	GTH	0	

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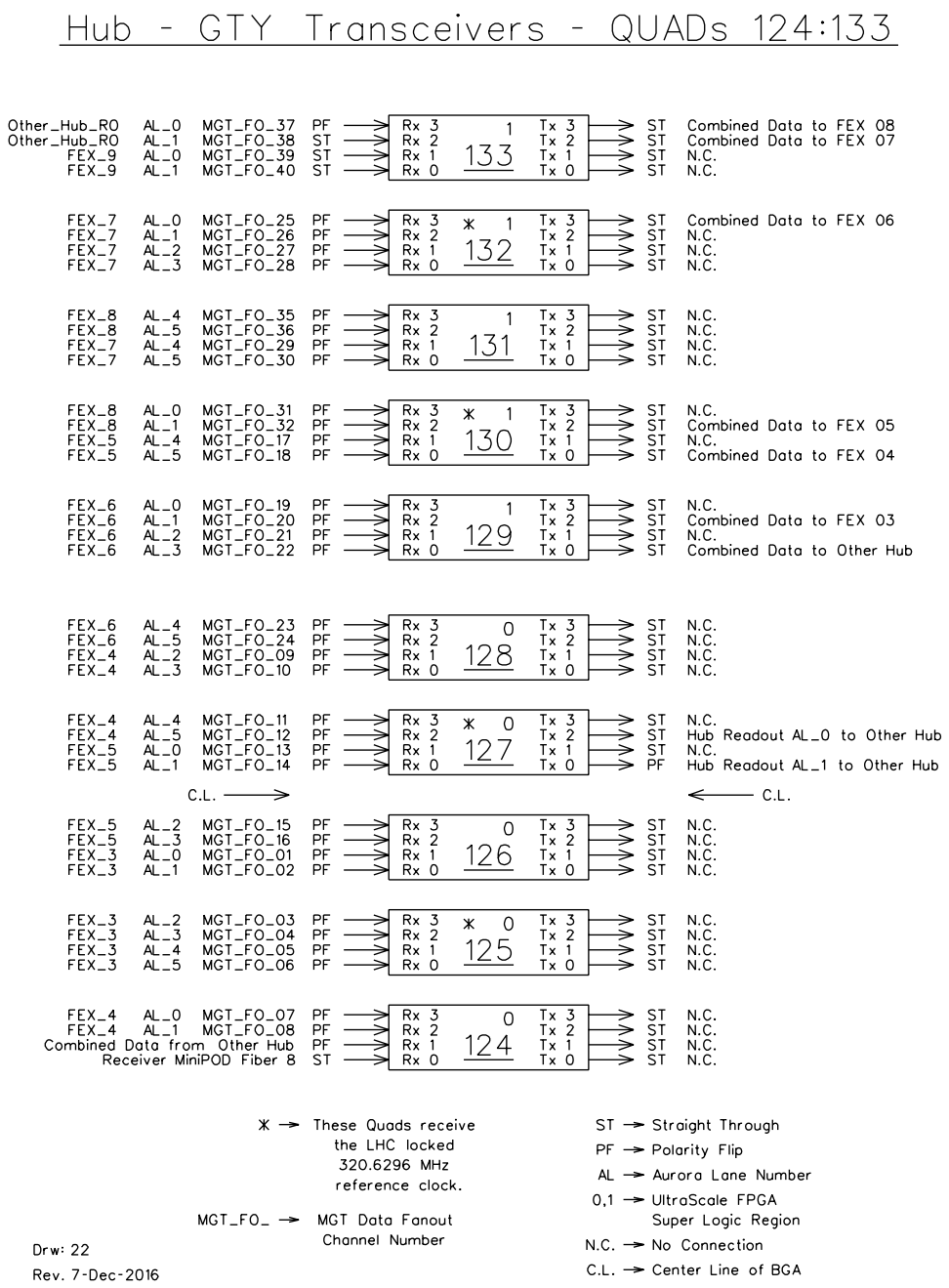

Figure 29: Hub GTY Transceiver Quad Assignments

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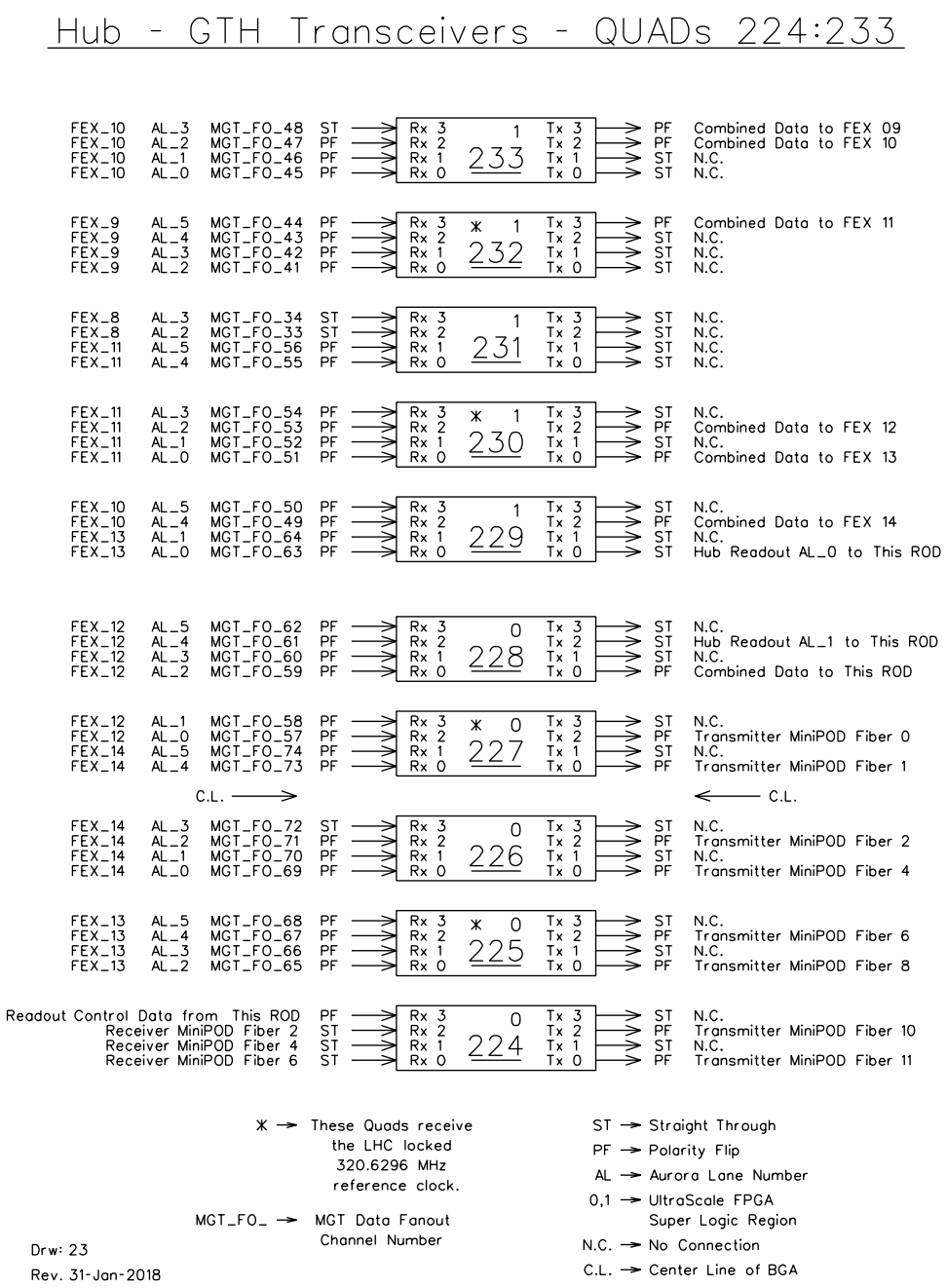

Figure 30: Hub GTH Transceiver Quad assignments.

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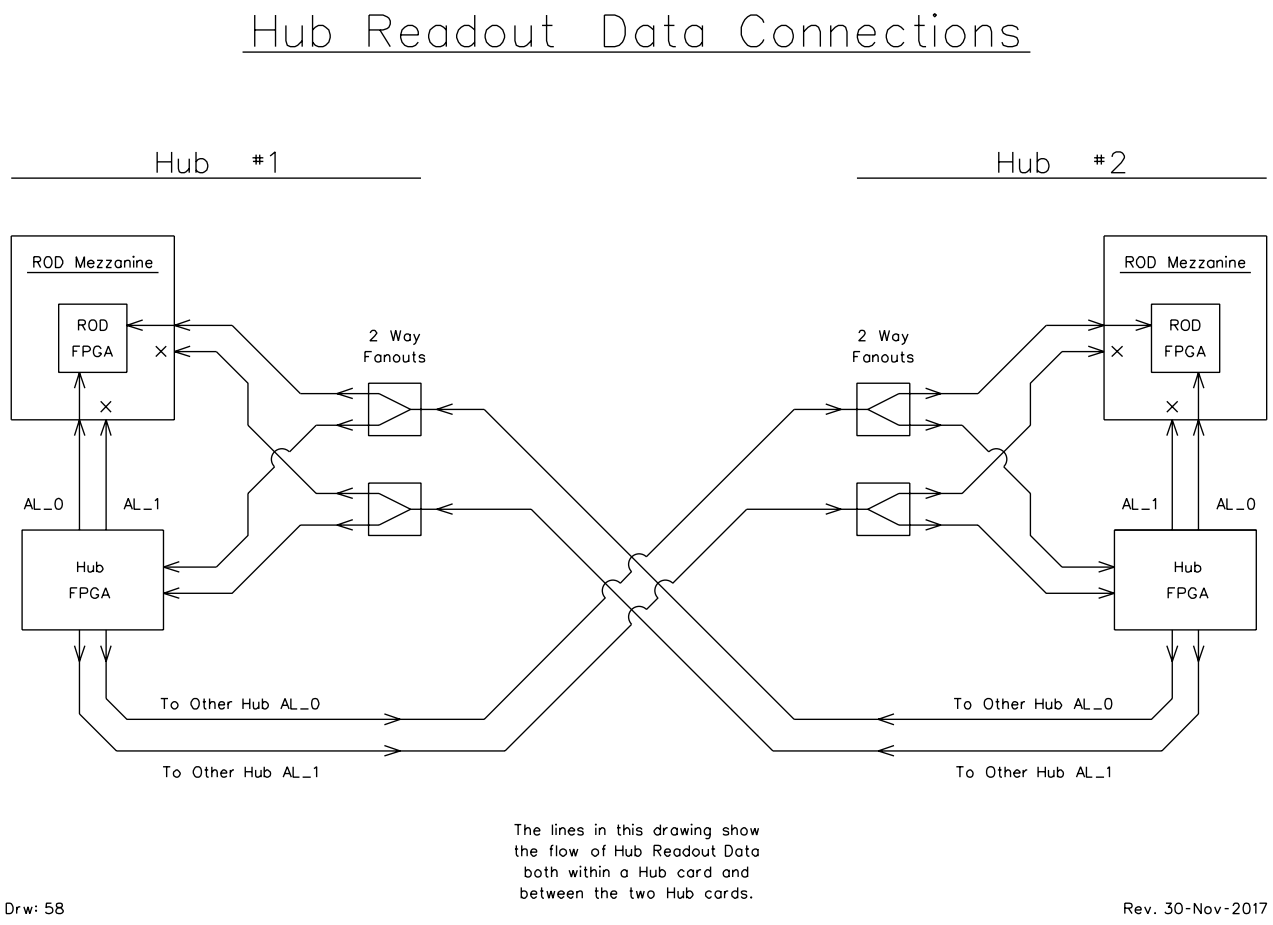

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Figure 31: Hub Readout Data Connections.

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19 Appendix 6: Hub Virtex FPGA Select I/O Usage

A significant number of Select I/O signals are used on the Hub Module's UltraScale Virtex FPGA. The intent of this document is to list in a single place all of the Select I/O lines that are used on the Hub FPGA. About 183 Select I/O pins are connected in the Hub design.
Notes:

- Currently all Select I/O connections to the Hub FPGA are made to Banks: 65, 67, 68, 70, 71, 72, 84, and 94.
- Bank 65 is used for Configuration of the FPGA from FLASH memory - Master BPI mode Configuration. Currently none of the Bank 65 Select I/O pins are used after Configuration except for the two pins that allow I2C slave access to the FPGA's System Monitor.
- Banks 84 and 94 are operated with a Vcco of 3V3. The Select I/O lines from Banks 84 and 94 are used for all of the 3V3 logic connections to the Hub Virtex FPGA.
- The only signals that are routed to Select I/O Banks 70, 71, 72 are:
  - the 13 Equalizer Enable signals that control the MGT Fanout equalizers (these are static low current output lines with non-critical routing),
  - the 2 PLL Lock-Detect inputs to the FPGA which should be static durning normal operation,
  - the 1 "clock select" signal that controls whether or not the 40.08 MHz reference clock outputs in Zone 2 are active or not. This is a static low current output,
  - and 3 differential clock signals inputs that use Bank 71 because it is adjacent to the clock generation chips. Bank 71 is of the HP type and is on SLR #1. These clock signals are the 40.08 MHz Logic Clock, the 320.64 MHz Logic Clock, and the 40.08 MHz Reference Clock from the Other Hub Module.
- Currently there are no connections to Bank 66. The reason for this is to facilitate routing access for required configuration signals to the very deep rings on Bank 65. These configuration signals need to go 14 or 15 rings in. Except for this - Bank 66 is perfectly usable HP type Select I/O signals. Bank 66 does have Vcco power.
- All banks that must handle high speed Select I/O signals have their VRP and VREF pins connected to the appripriate resistors. I have listed the reference designators of the resistors associated with these pins (instead of listing a not interesting net name).
- All of the Select I/O Banks that we are using in the Hub design come from Super Logic Region #0 in the XCVU125 stacked silicon FPGA, except for Banks 70, 71, and 72 which are part of Super Logic Region #1.

Bank 65:	1V8 I/O HP SLR #0	44 Hub Connections
BE20	IO_L24P_T3U_N10_EMCCLK_65	'NO_CONN_FPGA_BANK_65_BE20'
BF20	IO_L24N_T3U_N11_DOUT_CSO_B_65	'NO_CONN_FPGA_BANK_65_BF20'
BD20	IO_T3U_N12_PERSTN0_65	'NO_CONN_FPGA_BANK_65_BD20'
BE16	IO_L23P_T3U_N8_I2C_SCLK_65	'HUB_I2C_TO_FPGA_SCL'
BF16	IO_L23N_T3U_N9_I2C_SDA_65	'HUB_I2C_TO_FPGA_SDA'
BE19	IO_L22P_T3U_N6_DBC_AD0P_D04_65	'FLASH_D04'
BF19	IO_L22N_T3U_N7_DBC_AD0N_D05_65	'FLASH_D05'
BD18	IO_L21P_T3L_N4_AD8P_D06_65	'FLASH_D06'
BE18	IO_L21N_T3L_N5_AD8N_D07_65	'FLASH_D07'
BE17	IO_L20P_T3L_N2_AD1P_D08_65	'FLASH_D08'
BF17	IO_L20N_T3L_N3_AD1N_D09_65	'FLASH_D09'

BD17	IO_L19P_T3L_N0_DBC_AD9P_D10_65	'FLASH_D10'
BD16	IO_L19N_T3L_N1_DBC_AD9N_D11_65	'FLASH_D11'
BC20	IO_L18P_T2U_N10_AD2P_D12_65	'FLASH_D12'
BC19	IO_L18N_T2U_N11_AD2N_D13_65	'FLASH_D13'
BA19	IO_L17P_T2U_N8_AD10P_D14_65	'FLASH_D14'
BB19	IO_L17N_T2U_N9_AD10N_D15_65	'FLASH_D15'
BA21	IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65	'FLASH_A00'
BB21	IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65	'FLASH_A01'
BB18	IO_L15P_T2L_N4_AD11P_A02_D18_65	'FLASH_A02'
BC18	IO_L15N_T2L_N5_AD11N_A03_D19_65	'FLASH_A03'
AY20	IO_L14P_T2L_N2_GC_A04_D20_65	'FLASH_A04'
BA20	IO_L14N_T2L_N3_GC_A05_D21_65	'FLASH_A05'
BC21	IO_T2U_N12_CSI_ADV_B_65	'NO_CONN_FPGA_BANK_65_BC21'
AY19	IO_L13P_T2L_N0_GC_QBC_A06_D22_65	'FLASH_A06'
AY18	IO_L13N_T2L_N1_GC_QBC_A07_D23_65	'FLASH_A07'
AV20	IO_L12P_T1U_N10_GC_A08_D24_65	'FLASH_A08'
AW20	IO_L12N_T1U_N11_GC_A09_D25_65	'FLASH_A09'
AV19	IO_T1U_N12_PERSTN1_65	'NO_CONN_FPGA_BANK_65_AV19'
AW18	IO_L11P_T1U_N8_GC_A10_D26_65	'FLASH_A10'
AW17	IO_L11N_T1U_N9_GC_A11_D27_65	'FLASH_A11'
AV21	IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65	'FLASH_A12'
AW21	IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65	'FLASH_A13'
AU18	IO_L9P_T1L_N4_AD12P_A14_D30_65	'FLASH_A14'
AV18	IO_L9N_T1L_N5_AD12N_A15_D31_65	'FLASH_A15'
AT21	IO_L8P_T1L_N2_AD5P_A16_65	'FLASH_A16'
AU21	IO_L8N_T1L_N3_AD5N_A17_65	'FLASH_A17'
AT19	IO_L7P_T1L_N0_QBC_AD13P_A18_65	'FLASH_A18'
AU19	IO_L7N_T1L_N1_QBC_AD13N_A19_65	'FLASH_A19'
AR20	IO_L6P_T0U_N10_AD6P_A20_65	'FLASH_A20'
AT20	IO_L6N_T0U_N11_AD6N_A21_65	'FLASH_A21'
AR19	IO_L5P_T0U_N8_AD14P_A22_65	'FLASH_A22'
AR18	IO_L5N_T0U_N9_AD14N_A23_65	'FLASH_A23'
AM21	IO_L4P_T0U_N6_DBC_AD7P_A24_65	'FLASH_A24'
AN21	IO_L4N_T0U_N7_DBC_AD7N_A25_65	'FLASH_A25'
AM19	IO_L3P_T0L_N4_AD15P_A26_65	'NO_CONN_FPGA_BANK_65_AM19'
AN19	IO_L3N_T0L_N5_AD15N_A27_65	'NO_CONN_FPGA_BANK_65_AN19'
AN20	IO_L2P_T0L_N2_FOE_B_65	'FLASH_OUTPUT_ENB_B'
AP20	IO_L2N_T0L_N3_FWE_FCS2_B_65	'FLASH_WRITE_ENB_B'
AP21	IO_T0U_N12_VRP_A28_65	R101
AN18	IO_L1P_T0L_N0_DBC_RS0_65	'NO_CONN_FPGA_BANK_65_AN18'
AP18	IO_L1N_T0L_N1_DBC_RS1_65	'NO_CONN_FPGA_BANK_65_AP18'
AM18	VREF_65	R106
This is a complete list of all pins in Bank 65 including 9 No_Conn_ spare unused pins.		
Bank 66:	1V8 I/O HP SLR #0	2 Hub Connections
Except for the resistor pins no pins in Bank 66 are currently in use - all are "No_COnn_" spare not connected pins.		
AM27	IO_T0U_N12_VRP_66	R102
AM22	VREF_66	R107
Bank 67:	1V8 I/O HP SLR #0	27 Hub Connections

BE25	IO_L23P_T3U_N8_67	'OVERALL_ADRS_1_TO_RES_NET'
BF25	IO_L23N_T3U_N9_67	'OVERALL_ADRS_0_TO_RES_NET'
BE27	IO_L22P_T3U_N6_DBC_AD0P_67	'OVERALL_ADRS_3_TO_RES_NET'
BE28	IO_L22N_T3U_N7_DBC_AD0N_67	'OVERALL_ADRS_5_TO_RES_NET'
BF26	IO_L20P_T3L_N2_AD1P_67	'OVERALL_ADRS_2_TO_RES_NET'
BF27	IO_L20N_T3L_N3_AD1N_67	'OVERALL_ADRS_4_TO_RES_NET'
BA29	IO_L18P_T2U_N10_AD2P_67	'Hub_I2C_to_FPGA_SCL'
BB29	IO_L18N_T2U_N11_AD2N_67	'Hub_I2C_to_FPGA_SDA'
AW27	IO_L14P_T2L_N2_GC_67	'ROD_PRESENT_B_TO_FPGA'
AW28	IO_L14N_T2L_N3_GC_67	'ROD_Power_Control_2_FPGA'
BB28	IO_T2U_N12_67	'FPGA_RODs_SMBALERT_B'
AY27	IO_L13P_T2L_N0_GC_QBC_67	'TBD_SPARE_LINK_2_DIR'
AY28	IO_L13N_T2L_N1_GC_QBC_67	'TBD_SPARE_LINK_2_CMP'
AV29	IO_L12P_T1U_N10_GC_67	'ROD_Power_Control_4_FPGA'
AV30	IO_L12N_T1U_N11_GC_67	'ROD_Power_Control_3_FPGA'
AU28	IO_L11P_T1U_N8_GC_67	'SPARE_OSC_TO_FPGA_DIR'
AV28	IO_L11N_T1U_N9_GC_67	'SPARE_OSC_TO_FPGA_CMP'
AT30	IO_L10P_T1U_N6_QBC_AD4P_67	'ACCESS_SIGNAL_1_FROM_FPGA'
AT31	IO_L10N_T1U_N7_QBC_AD4N_67	'ACCESS_SIGNAL_2_FROM_FPGA'
AT29	IO_L9P_T1L_N4_AD12P_67	'TBD_SPARE_LINK_3_DIR'
AU29	IO_L9N_T1L_N5_AD12N_67	'TBD_SPARE_LINK_3_CMP'
AT27	IO_L8P_T1L_N2_AD5P_67	'TBD_SPARE_LINK_1_DIR'
AU27	IO_L8N_T1L_N3_AD5N_67	'TBD_SPARE_LINK_1_CMP'
AV26	IO_L7P_T1L_N0_QBC_AD13P_67	'TBD_SPARE_LINK_0_DIR'
AW26	IO_L7N_T1L_N1_QBC_AD13N_67	'TBD_SPARE_LINK_0_CMP'
AP31	IO_T0U_N12_VRP_67	R103
AM28	VREF_67	R108
The remaining Bank 67 pins are not connected and are not listed here.		
Bank 68:	1V8 I/O HP SLR #0	41 Hub Connections
BF30	IO_L24P_T3U_N10_68	'HUB_FPGA_LED51_DRV'
BF31	IO_L24N_T3U_N11_68	'HUB_FPGA_LED52_DRV'
BA30	IO_T3U_N12_68	'Phys_U21_MDIO'
BC31	IO_L23P_T3U_N8_68	'Phys_U21_RXD0__MODE0'
BD31	IO_L23N_T3U_N9_68	'No_Conn_FPGA_BD31'
BE29	IO_L22P_T3U_N6_DBC_AD0P_68	'OVERALL_ADRS_6_TO_RES_NET'
BF29	IO_L22N_T3U_N7_DBC_AD0N_68	'HUB_FPGA_LED50_DRV'
BA31	IO_L21P_T3L_N4_AD8P_68	'Phys_U22_INT_B'
BB31	IO_L21N_T3L_N5_AD8N_68	'Phys_U21_RX_DV__CLK125_EN'
BD30	IO_L20P_T3L_N2_AD1P_68	'No_Conn_FPGA_BD30'
BE30	IO_L20N_T3L_N3_AD1N_68	'OVERALL_ADRS_7_TO_RES_NET'
BC29	IO_L19P_T3L_N0_DBC_AD9P_68	'No_Conn_FPGA_BC29'
BC30	IO_L19N_T3L_N1_DBC_AD9N_68	'Phys_U21_INT_B'
BA36	IO_L18P_T2U_N10_AD2P_68	'Phys_U21_TXD0'
BB36	IO_L18N_T2U_N11_AD2N_68	'Phys_U21_TXD2'
BB32	IO_L17P_T2U_N8_AD10P_68	'Phys_U21_MDC'
BB33	IO_L17N_T2U_N9_AD10N_68	'Phys_U21_RXD2__MODE2'
BA34	IO_L16P_T2U_N6_QBC_AD3P_68	'Phys_U21_GTX_CLK'
BB34	IO_L16N_T2U_N7_QBC_AD3N_68	'Phys_U21_TX_EN'
AY32	IO_L15P_T2L_N4_AD11P_68	'Phys_U21_RXD1__MODE1'
BA32	IO_L15N_T2L_N5_AD11N_68	'No_Conn_FPGA_BA32'

AW33	IO_L14P_T2L_N2_GC_68	'Phys_U22_RX_CLK__PHYAD2'
AY33	IO_L14N_T2L_N3_GC_68	'Phys_U21_RXD3__MODE3'
BA35	IO_T2U_N12_68	'Phys_U21_TXD3'
AY34	IO_L13P_T2L_N0_GC_QBC_68	'Phys_U22_CLK125__LED_MODE'
AY35	IO_L13N_T2L_N1_GC_QBC_68	'Phys_U21_TXD1'
AU33	IO_L12P_T1U_N10_GC_68	'Phys_U21_CLK125__LED_MODE'
AU34	IO_L12N_T1U_N11_GC_68	'Phys_U22_TX_EN'
AW32	IO_T1U_N12_68	'Phys_U22_RX_DV__CLK125_EN'
AV33	IO_L11P_T1U_N8_GC_68	'Phys_U21_RX_CLK__PHYAD2'
AV34	IO_L11N_T1U_N9_GC_68	'Phys_U22_RXD2__MODE2'
AV36	IO_L10P_T1U_N6_QBC_AD4P_68	'Phys_U22_RXD1__MODE1'
AW36	IO_L10N_T1U_N7_QBC_AD4N_68	'Phys_U22_MDC'
AV35	IO_L9P_T1L_N4_AD12P_68	'Phys_U22_RXD0__MODE0'
AW35	IO_L9N_T1L_N5_AD12N_68	'Phys_U22_MDIO'
AU31	IO_L8P_T1L_N2_AD5P_68	'No_Conn_FPGA_AU31'
AU32	IO_L8N_T1L_N3_AD5N_68	'Phys_U22_RXD3__MODE3'
AV31	IO_L7P_T1L_N0_QBC_AD13P_68	'Ref_40.08_MHz_from_FPGA_to_Rec_Dir'
AW31	IO_L7N_T1L_N1_QBC_AD13N_68	'Ref_40.08_MHz_from_FPGA_to_Rec_Cmp'
AR36	IO_L6P_T0U_N10_AD6P_68	'Phys_U22_TXD0'
AT36	IO_L6N_T0U_N11_AD6N_68	'Phys_U22_TXD1'
AP33	IO_L5P_T0U_N8_AD14P_68	'No_Conn_FPGA_AP33'
AR33	IO_L5N_T0U_N9_AD14N_68	'No_Conn_FPGA_AR33'
AR35	IO_L4P_T0U_N6_DBC_AD7P_68	'Phys_U22_TXD2'
AT35	IO_L4N_T0U_N7_DBC_AD7N_68	'Phys_U22_TXD3'
AR32	IO_L3P_T0L_N4_AD15P_68	'No_Conn_FPGA_AR32'
AT32	IO_L3N_T0L_N5_AD15N_68	'No_Conn_FPGA_AT32'
AR34	IO_L2P_T0L_N2_68	'No_Conn_FPGA_AR34'
AT34	IO_L2N_T0L_N3_68	'Phys_U22_GTX_CLK'
AU36	IO_T0U_N12_VRP_68	R104
AN32	IO_L1P_T0L_N0_DBC_68	'No_Conn_FPGA_AN32'
AP32	IO_L1N_T0L_N1_DBC_68	'No_Conn_FPGA_AP32'
AM32	VREF_68	R109
This is a complete list of all pins in Bank 68 including 12 No_Conn_ spare unused pins.		
Bank 84:	3V3 I/O_HR_SLR #0	24 Hub Connections
AP17	IO_L24P_T3U_N10_84	'ROD_Power_Enable_B'
AR17	IO_L24N_T3U_N11_84	'ROD_Power_Enable'
AM16	IO_T3U_N12_84	'ALL_HUB_POWER_GOOD_TO_FPGA'
AN15	IO_L23P_T3U_N8_84	'Trans_MiniPOD_SCL'
AP15	IO_L23N_T3U_N9_84	'Trans_MiniPOD_SDA'
AV16	IO_L22P_T3U_N6_DBC_AD0P_84	'FPGA_SW_C_LOOP_DETECTED'
AV15	IO_L22N_T3U_N7_DBC_AD0N_84	'FPGA_SW_C_ATC_LOOP_DET'
AN16	IO_L21P_T3L_N4_AD8P_84	'Trans_MiniPOD_INTR_B'
AP16	IO_L21N_T3L_N5_AD8N_84	'Hubs_SMB_Alert_B'
AT17	IO_L20P_T3L_N2_AD1P_84	'No_Conn_FPGA_AT17'
AU17	IO_L20N_T3L_N3_AD1N_84	'No_Conn_FPGA_AU17'
AT16	IO_L19P_T3L_N0_DBC_AD9P_84	'FPGA_SW_B_MDC'
AU16	IO_L19N_T3L_N1_DBC_AD9N_84	'FPGA_SW_B_MDIO'
AP13	IO_L18P_T2U_N10_AD2P_84	'Trans_MiniPOD_RESET_B'
AR13	IO_L18N_T2U_N11_AD2N_84	'Recvr_MiniPOD_SDA'
AU12	IO_L17P_T2U_N8_AD10P_84	'ISO_SLOT_HW_ADRS_2'
AU11	IO_L17N_T2U_N9_AD10N_84	'ISO_SLOT_HW_ADRS_3'

AR15	IO_L16P_T2U_N6_QBC_AD3P_84	'Recvr_MiniPOD_INTR_B'
AR14	IO_L16N_T2U_N7_QBC_AD3N_84	'Recvr_MiniPOD_RESET_B'
AR12	IO_L15P_T2L_N4_AD11P_84	'Recvr_MiniPOD_SCL'
AT12	IO_L15N_T2L_N5_AD11N_84	'ISO_SLOT_HW_ADRS_0'
AT15	IO_L14P_T2L_N2_GC_84	'CLOCK_25_MHz_FPGA'
AT14	IO_L14N_T2L_N3_GC_84	'FPGA_SW_B_ATC_LOOP_DET'
AT11	IO_T2U_N12_84	'ISO_SLOT_HW_ADRS_1'
AU14	IO_L13P_T2L_N0_GC_QBC_84	'No_Conn_FPGA_AU14'
AU13	IO_L13N_T2L_N1_GC_QBC_84	'FPGA_SW_B_LOOP_DETECTED'
AM17	VREF_84	R111
This is a complete list of all pins in Bank 84 including 3 No_Conn_ spare unused pins.		
Bank 94:	3V3 I/O HR SLR #0	22 Hub Connections
AW13	IO_L12P_T1U_N10_GC_94	'FPGA_SW_A_MDC'
AW12	IO_L12N_T1U_N11_GC_94	'ISO_SLOT_HW_ADRS_5'
AY13	IO_T1U_N12_94	'FPGA_SW_C_MDC'
AV14	IO_L11P_T1U_N8_GC_94	'No_Conn_FPGA_AV14'
AV13	IO_L11N_T1U_N9_GC_94	'FPGA_SW_A_ATC_LOOP_DET'
BA11	IO_L10P_T1U_N6_QBC_AD4P_94	'SHELF_ADRS_7_TO_FPGA'
BB11	IO_L10N_T1U_N7_QBC_AD4N_94	'SHELF_ADRS_5_TO_FPGA'
AY12	IO_L9P_T1L_N4_AD12P_94	'ISO_SLOT_HW_ADRS_7'
BA12	IO_L9N_T1L_N5_AD12N_94	'SHELF_ADRS_6_TO_FPGA'
BB13	IO_L8P_T1L_N2_AD5P_94	'SHELF_ADRS_3_TO_FPGA'
BB12	IO_L8N_T1L_N3_AD5N_94	'SHELF_ADRS_4_TO_FPGA'
AV11	IO_L7P_T1L_N0_QBC_AD13P_94	'ISO_SLOT_HW_ADRS_4'
AW11	IO_L7N_T1L_N1_QBC_AD13N_94	'ISO_SLOT_HW_ADRS_6'
AY17	IO_L6P_T0U_N10_AD6P_94	'No_Conn_FPGA_AY17'
BA17	IO_L6N_T0U_N11_AD6N_94	'No_Conn_FPGA_BA17'
BA14	IO_L5P_T0U_N8_AD14P_94	'SHELF_ADRS_2_TO_FPGA'
BB14	IO_L5N_T0U_N9_AD14N_94	'SHELF_ADRS_1_TO_FPGA'
BB17	IO_L4P_T0U_N6_DBC_AD7P_94	'No_Conn_FPGA_BB17'
BB16	IO_L4N_T0U_N7_DBC_AD7N_94	'I2C_Buf_1503_ENABLE'
BA16	IO_L3P_T0L_N4_AD15P_94	'I2C_Buf_1501_ENABLE'
BB15	IO_L3N_T0L_N5_AD15N_94	'SHELF_ADRS_0_TO_FPGA'
AW15	IO_L2P_T0L_N2_94	'FPGA_SW_A_MDIO'
AY14	IO_L2N_T0L_N3_94	'FPGA_SW_C_MDIO'
BC16	IO_T0U_N12_94	'No_Conn_FPGA_BC16'
AY15	IO_L1P_T0L_N0_DBC_94	'FPGA_SW_A_LOOP_DETECTED'
BA15	IO_L1N_T0L_N1_DBC_94	'I2C_Buf_1502_ENABLE'
AW16	VREF_94	R112
This is a complete list of all pins in Bank 94 including 5 No_Conn_ spare unused pins.		
Bank 70:	1V8 I/O HP SLR #1	3 Connections PLL-Det FEX Ref Clk Enb
B26	IO_L24P_T3U_N10_70	'PLL_320.64_MHz_Lock_Detect_to_FPGA'
B27	IO_L22P_T3U_N6_DBC_AD0P_70	'PLL_40.08_MHz_Lock_Detect_to_FPGA'
A26	IO_L24N_T3U_N11_70	'Select_Input_Second_40_Fanout'
Only the Bank 70 signals used in the Hub design are listed.		
Bank 71:	1V8 I/O HP SLR #1	15 Connections Clocks and Equalizer Enb
B22	IO_L24N_T3U_N11_71	'MGT_FO_EQU_ENB_GRP_6'

B25	IO_L23P_T3U_N8_71	'MGT_FO_EQU_ENB_GRP_3'
A25	IO_L23N_T3U_N9_71	'MGT_FO_EQU_ENB_GRP_2'
C25	IO_L21N_T3L_N5_AD8N_71	'MGT_FO_EQU_ENB_GRP_1'
A24	IO_L20P_T3L_N2_AD1P_71	'MGT_FO_EQU_ENB_GRP_4'
A23	IO_L20N_T3L_N3_AD1N_71	'MGT_FO_EQU_ENB_GRP_9'
C24	IO_L19N_T3L_N1_DBC_AD9N_71	'MGT_FO_EQU_ENB_GRP_5'
H23	IO_L14P_T2L_N2_GC_71	'Ref_40.08_MHz_from_Other_Hub_Dir'
G23	IO_L14N_T2L_N3_GC_71	'Ref_40.08_MHz_from_Other_Hub_Cmp'
J24	IO_L12P_T1U_N10_GC_71	'Logic_Clk_40.08_MHz_to_FPGA_Dir'
H24	IO_L12N_T1U_N11_GC_71	'"Logic_Clk_40.08_MHz_to_FPGA_Cmp'
K22	IO_L11P_T1U_N8_GC_71	'Logic_Clk_320.64_MHz_to_FPGA_Dir'
J22	IO_L11N_T1U_N9_GC_71	'Logic_Clk_320.64_MHz_to_FPGA_Cmp'
P22	IO_T0U_N12_VRP_71	R105
P21	VREF_71	R110
The remaining 39 pins in Bank 71 are not used in the Hub design and are not listed here.		
Bank 72:	1V8 I/O HP SLR #1	6 Connections Equalizer Enables
A18	IO_L24N_T3U_N11_72	'MGT_FO_EQU_ENB_GRP_13'
A20	IO_L23P_T3U_N8_72	'MGT_FO_EQU_ENB_GRP_11'
A19	IO_L23N_T3U_N9_72	'MGT_FO_EQU_ENB_GRP_12'
A21	IO_L21N_T3L_N5_AD8N_72	'MGT_FO_EQU_ENB_GRP_10'
D20	IO_L20P_T3L_N2_AD1P_72	'MGT_FO_EQU_ENB_GRP_7'
C20	IO_L19P_T3L_N0_DBC_AD9P_72	'MGT_FO_EQU_ENB_GRP_8'
Only the Bank 72 signals used in the Hub design are listed.		

20 Appendix 7: Hub FPGA Signal Types

For each signal "type" that connects to the Hub's FPGA this file provides:

- A short description of the function of that signal type.
- A description of how the I/O Block that handles that signal type should be setup.
- A description of the FPGA logic that is necessary to properly handle that signal type in a minimal safe Hub firmware implementation.
- Where applicable a reference is given to the Hub Circuit Diagram(s) where that signal type is shown so that you can see how it is used on the Hub circuit board.

20.1 Select I/O Signals:

20.1.1 Clock and Clock Management Signals

This sections lists the various Select I/O clock signals and clock management signals in the Hub design. See **Figure 24**, **Figure 25**, **Figure 26** and **Figure 27**.

CLOCK_25_MHz_FPGA

This is a single ended clock input to the FPGA. This clock is used in the Ethernet circuits. This is not an LHC locked clock. This is a 3.3V CMOS clock signal that is always running. The FPGA needs to always provide a 3.3V CMOS receiver for it. No special internal FPGA termination should be necessary to correctly receive this clock signal.

Logic_Clk_320.64_MHz_to_FPGA_ Dir/Cmp, Logic_Clk_40.08_MHz_to_FPGA_ Dir/Cmp

These are the main Logic Clock signals for the Hub FPGA. These are AC coupled LHC locked clocks. The FPGA must receive them as differential signals, 100 Ohm terminate them, and DC Bias these FPGA inputs by including the proper combination of DQS_Bias and EQ_Level0 attributes in the setup of these I/O Blocks. Even if these clocks are not used in a minimal safe FPGA design they must still be properly received.

Ref_40.08_MHz_from_Other_Hub_ Dir/Cmp

This is an AC coupled LVDS input to the Hub FPGA. In a shelf with two Hub Modules this clock path is used on the Hub that does not receive an Optical Felix TTC signal. Because this is AC coupled the I/O Block that receives this signal must be setup with the correct combination of the DQS_Bias and EQ_Level0 attributes. This FPGA input should include a 100 Ohm differential terminator. This input needs to be setup and instantiated in all versions of the Hub FPGA firmware.

Ref_40.08_MHz_from_FPGA_to_Rec_ Dir/Cmp

This is an LVDS output from the Hub FPGA that runs to an LVDS receiver and then connects to the reference input on the 40.08 MHz PLL. I believe that we should include this output even in a minimal safe FPGA design even if we only tie the input to the LVDS driver Low.

PLL_40.08_MHz_Lock_Detect_to_FPGA, PLL_320.64_MHz_Lock_Detect_to_FPGA

These are two Lock Detect signals from the PLL Clock circuits on the Hub Module. When Hi they indicate that the associated PLL has locked onto its reference input. The FPGA needs to always provide 1.8V CMOS receivers for these two signals.

Select_Input_Second_40_Fanout

This signal is an output from the Hub FPGA. It is used to enable or disable the Hub circuit board from sending out 40.08 MHz Reference Clocks on Zone-2 of the Backplane. Recall that in a shelf with 2 Hub Modules, that only the primary Hub that receives the Optical Felix TTC signal will send out its 40.08 MHz Reference Clocks to the FEX modules. The secondary Hub (the Hub that does not receive an Optical Felix TTC signal) must not send out its Zone-2 Reference Clocks. This is a 1.8V CMOS open-drain output from the Hub Module. When Low it enables the Hub Module to send out its Zone-2 Reference Clocks. When the open-drain output transistor in the FPGA I/O Block is Off then its backplane Reference Clock output drives will be shutdown. In a minimal safe design I think that we want this open-drain output to pull this signal Low so that we can see these Reference Clock outputs.

SPARE_OSC_TO_FPGA_ Dir/Cmp

This is a spare differential clock input to the Hub FPGA. As long as we are not installing this part (U562) then nothing special needs to be done with these input pins to the FPGA even in a minimal safe FW design.

20.1.2 Ethernet Switch Chip Management Signals

Each of the 3 Broadcom Ethernet Switch chips has its own set of 4 management signals with the Hub FPGA. See Hub Circuit Diagram 17.

FPGA_SW_?_ATC_LOOP_DET

This is a control signal from the Hub FPGA to the Ethernet Switch chips. I assume that this signal will eventually be controlled from a bit in an IPBus visible register. A minimal Hub FPGA design could just tie this signal Low. A Slow Slew and 4 mA Drive level is fine for this 3.3V CMOS static level output signal.

FPGA_SW_?_LOOP_DETECTED

This is a status signal from the Broadcom Switch chips to the Hub FPGA. I assume that this status bit will eventually be visible in an IPBus register. The FPGA needs to at least always provide a receiver for this 3.3V CMOS input signal.

FPGA_SW_?_MDC

Because the MDC/MDIO interface on the Broadcom Switch chips is in Slave mode, this clock signal runs from the Hub FPGA to the Switch chip. Eventually I assume that these pins on the Hub FPGA will be controlled by firmware that implements the MDC/MDIO part of a MAC. For minimal safe firmware this line could just be driven Low by a Slow Slew 4 mA 3.3V CMOS output driver.

FPGA_SW_?_MDIO

This is a bi-directional data line between the Hub FPGA and the MDC/MDIO interface in the Broadcom Switch chips. Eventually I assume that these pins on the Hub FPGA will be handled by firmware that implements the MDC/MDIO part of a MAC. In a minimal safe Hub FPGA design I would provide a 3.3V CMOS receiver for this signal with a weak pull-up resistor at its input.

20.1.3 Hardware Address Signals

ISO_SLOT_HW_ADRS_?

These 8 signals bring the backplane Hardware Slot Address to the Hub FPGA. The IPMC module also receives these signals. Even if the Hub FPGA is not going to use this Hardware Slot number information it must still receive these 8 lines with 3.3V CMOS receivers. See Hub Circuit Diagram 13.

SHELF_ADRS_?_TO_FPGA

These are 8 signals that bring the Shelf Address information from the IPMC to the Hub's FPGA. These lines connect to "User I/O" pins on one of the ARM CPUs in the IPMC module. The Hub Firmware needs to at least always provide 3.3V CMOS receives for these signals.

OVERALL_ADRS_?_TO_RES_NET

These are 8 outputs from the Hub FPGA that provide an Overall Hardware Address to the ROD mezzanine. This Overall Hardware Address is made up of the Slot Hardware Address that comes from the Backplane and the Shelf Hardware Address that comes from the IPMC. In a minimal safe FPGA implementation I would just tie all 8 of these Overall Hardware Address lines Low. These can be 1.8V CMOS Slow Slew 4 mA Drive outputs.

20.1.4 I2C Bus Signals

Hub_I2C_to_FPGA_SCL, Hub_I2C_to_FPGA_SDA

Note that this I2C bus makes TWO connections to the Hub FPGA. See Hub Circuit Diagram 37.

It connects to pins:

BE16 IO_L23P_T3U_N8_I2C_SCLK_65

BF16 IO_L23N_T3U_N9_I2C_SDA_65

that provide for a Slave I2C interface to the FPGA System Monitor, and it connects to pins:

BA29 IO_L18P_T2U_N10_AD2P_67

BB29 IO_L18N_T2U_N11_AD2N_67

so that one can implement a Master I2C interface so that for example the Hub FPGA can talk to the Hub's DCDC Converter power supplies.

In a minimal safe design both of these I2C signals at both pin pairs should connect to 1.8V CMOS Receivers.

I2C_Buf_150?_ENABLE

These are control signals from the Hub FPGA to the Sensor I2C Bus translator/buffer chips. These translator/buffer chips allow the overall Sensor I2C Bus on the ROD-Hub cards to be divided up into sections. Eventually we may need to control dividing up the Sensor I2C bus either from bits in an IPBus visible register of from a control signal from the ROD to the Hub. For a minimal safe Hub FPGA design these 3 I2C buffer control signals can just be tied Hi which will enable these I2C translator/buffers. These control signals are 3.3V Slow Slew 4 mA Drive outputs from the Hub FPGA.

20.1.5 MiniPOD Management Signals

Each of the MiniPODs has 4 management signals associated with it. The Hub's Receiver and Transmitter MiniPODs each have their own private set of these 4 management signals. Hub Circuit Diagram 21 shows the layout of these signals. The setup of the MiniPOD management signals on the Hub is very similar to that used on the CMX card.

Recvr_MiniPOD_INTR_B, Trans_MiniPOD_INTR_B

Interrupt signals from the MiniPODs to the FPGA. Low indicates interrupt. The FPGA should always provide 3.3V CMOS receivers for these two signals.

Recvr_MiniPOD_RESET_B, Trans_MiniPOD_RESET_B

These are Reset signals from the FPGA to the MiniPODs. Low indicates Reset. A minimal safe design should at least drive these lines Hi with a Slow Slew 4 mA Drive 3.3V CMOS output. In a full firmware design I assume that these Reset signals will be controlled from bits in an IPBus visible register.

Recvr_MiniPOD_SCL, Trans_MiniPOD_SCL

These are the clock signals for the bi-directional serial data path between the FPGA and the MiniPODs. In a minimal safe design I would drive this signals Low with a Slow Slew 4 mA Drive 3.3V CMOS output.

Recvr_MiniPOD_SDA, Trans_MiniPOD_SDA

These are the bi-directional data lines for the serial data path between the FPGA and the MiniPODs. In a minimal design I would provide a 3.3V CMOS receiver for these signals.

20.1.6 Miscellaneous Select I/O Signals

ACCESS_SIGNAL_?_FROM_FPGA

These two output signals from the FPGA run to a translator/buffer chip and then to pins in the front panel J2 connector. See Hub Circuit Diagram 53. The purpose of these signals is to allow one to see with an oscilloscope some aspect of the FPGA's operation. Unless needed for something special these 1.8V CMOS output signals can be configured for a Slow Slew rate and modest 4 mA Drive. A minimal safe Hub FPGA design could just tie these 2 signals Low.

HUB_FPGA_LED5?_DRV

These three signals are outputs from the Hub FPGA that control front panel LEDs. These are 1.8V CMOS signals and using a Slow Slew and 4 mA of Drive would be fine. A minimal safe Hub FPGA design could just tie these 3 output signals Low.

Hubs_SMB_Alert_B

This is an input signal to the Hub's FPGA from the 7 DCDC Converter power supplies on the Hub Module. When Low it indicates that one or more of these Hub power supplies is in trouble (or at least wants attention). Normally this signal should be Hi. This is a 3.3V CMOS signal and the FPGA must always have a receiver for it even if it does not make use of this signal.

ALL_HUB_POWER_GOOD_TO_FPGA

This is an input signal to the Hub's FPGA from the Power Control circuits on the Hub Module. This is a 3.3V Select I/O signal in Bank 84. When Low this signal indicates that there is some kind of power supply problem on the Hub Module. When Hi this signal indicates: that all 7 DCDC Converters report that they are operating correctly, and that the Isolated +12V supply is Enabled, and that the output from the Linear MGT_AVAUX and BULK_2V5 supplies is good. The Hub FPGA must always instance a 3.3V CMOS receiver for this signal even if it does not make use of this signal. This signal comes through a 2.7k Ohm isolation resistor from a 5V source.

MGT_FO_EQU_ENB_GRP_?

These 13 control signals are outputs from the Hub FPGA that enable or disable the equalization in the MGT Fanout chips. All fanout chips that service a given data source either have their equalization enabled or disabled. I assume that eventually these 13 equalization enable signals will be separately controllable from bits in an IPBus visible register. In a minimal safe Hub FPGA design all of the Equalization Enable signals can just be tied HI. I would drive them as 1.8V CMOS outputs with Slow Slew and 8 mA of Drive. The loading on these signals will only be about 150 uA but the high Drive level may help if we need to ramp up the FAN_1V8 rail voltage.

TBD_SPARE_LINK_?_ Dir/Cmp

These are 8 To Be Determined spare lines between the Hub and ROD FPGAs. Currently none of them have an assigned function. If needed they can be operated as either 8 separate 1.8V CMOS signals or as 4 separate LVDS signals. As with all CMOS signals we can not just leave them floating. As unassigned spare signals the agreement with ROD is that we will run them as 8 separate CMOS signals and that the Hub will drive them and the ROD will receive them. Further the agreement with ROD is that the Hub will keep these signals tri-stated until the ROD asserts it Power Control #2 signal HI to the Hub. See Hub Circuit Diagram 42. Even in a minimal safe firmware design the Hub needs to implement this functionality. These 8 lines should be driven with Slow Slew 4 mA Drive 1.8V CMOS output blocks. See also Section 26.

20.1.7 Phys_U21 and Phys_U22 signals

Each Phys Chip makes 16 connections with the Hub's FPGA. These Phys Chip <--> FPGA connections are shown in **Figure 43** and make up a RGMII interface bus.

In the real Hub operation these 16 signals will be managed by MAC IP firmware. This RGMII connection between the FPGA and the Phys Chips includes signals that may require fast slew rates, higher drive current, and DCI back (series) termination. These RGMII signals have been laid out carefully on the Hub circuit to minimize cross-talk, reflections, and signal loss. Careful consideration must be given to how the RMGII signals are handled in the FPGA I/O Blocks to provide both a good RGMII interface and to minimize interference with other parts of the Hub Module.

For a minimal safe Hub FPGA design we still should handle these CMOS signals in a defined rational way.

I would provide Low current Drive Slow Slew 1.8V CMOS outputs tied Low for the following signals:

Phys_U2?_TXD0

Phys_U2?_TXD1
Phys_U2?_TXD2
Phys_U2?_TXD3
Phys_U2?_TX_EN
Phys_U2?_GTX_CLK
Phys_U2?_MDC

I would provide 1.8V CMOS receivers for the following signals:

Phys_U2?_RXD0__MODE0
Phys_U2?_RXD1__MODE1
Phys_U2?_RXD2__MODE2
Phys_U2?_RXD3__MODE3
Phys_U2?_RX_CLK__PHYAD2
Phys_U2?_RX_DV__CLK125_EN
Phys_U2?_CLK125__LED_MODE
Phys_U2?_MDIO
Phys_U2?_INT_B

20.1.8 ROD Present and ROD Power Control Signals

These 7 signals have to do with letting the Hub know whether or not a ROD is installed on it, Controlling (i.e. enabling) the power on the ROD, and letting the Hub know whether or not all ROD power is good and that the ROD is ready for normal trigger system operation. See also Section 26 for further discussion.

ROD_PRESENT_B_TO_FPGA

This signal is a pull-down resistor on the ROD. When the ROD is NOT present this signal goes HI on the Hub. The Hub must always provide a 1.8V CMOS receiver for this signal even if it does not use it.

ROD_Power_Control_2_FPGA

This is an input to the Hub's FPGA. When HI this signal indicates that all power supplies on the ROD are operating correctly. The Hub must always provide a 1.8V CMOS receiver for this signal even if it does not use it.

ROD_Power_Control_3_FPGA

This is an input to the Hub's FPGA. When HI this signal indicates that the ROD is Configured and fully ready for normal L1Calo operation. The Hub must always provide a 1.8V CMOS receiver for this signal even if it does not use it.

ROD_Power_Control_4_FPGA

This is a spare power control signal. In a minimal safe firmware design the Hub should provide a 1.8V CMOS receiver for this signal with a weak pull-up resistor at its input.

ROD_Power_Enable, ROD_Power_Enable_B

These two signal are outputs from the Hub FPGA that through some hardwired logic on the Hub tell the ROD when it may turn ON its power supplies. The hardwired logic associated with these signals is shown in Hub Circuit Diagram 32. These are 3.3V Slow Slew 4 mA Drive CMOS outputs. A minimal safe design (that just locks OFF the ROD power) should set ROD_Power_Enable Low and set ROD_Power_Enable_B Hi.

FPGA_RODs_SMBALERT_B

This is an input to the Hub's FPGA that when LOW indicates a power supply problem on the ROD. During normal operation this signal should always be HI. Pull up current to 1V8 is provided by a 1k Ohm resistor on page 25 of the ROD schematics. A normal 1.8V CMOS receiver should be used. The FPGA needs to always provide a receiver for this signal.

20.2 MGT Transceiver Signals

Comb_Data_to_Cap_to_FEX_*_Dir/Cmp, Comb_Data_to_Cap_to_Other_Hub_Dir/Cmp, Comb_Data_to_Cap_to_ROD_Dir/Cmp

These 14 Combined Data signals are MGT Outputs from the FPGA. Hub Circuit Diagrams 22 and 23 indicate which of the Combined Data signals needed to be inverted in their MGT Transmitter in order to provide standard right-side-up polarity over the Backplane and at the Receiver.

This_Hubs_RO_?_to_Cap_Its_ROD_Dir/Cmp, This_Hubs_RO_?_to_Cap_Other_ROD_Dir/Cmp

These 4 MGT outputs are the readout data from the Hub FPGA. One of these links goes to the ROD on This Hub (where it can only receive the Lane 0 signal) and the second pair goes to the MGT Fanout on the Other Hub from which it is routed to both the Other Hub's FPGA and to the Other Hub's ROD. Hub Circuit Diagrams 22 and 23 indicate the MGT Transmitter logic inversions that should be included in the firmware setup.

MiniPOD_Trans_Fiber_??_Data_ Dir/Cmp

These are 8 MGT Transmitter outputs that run to the Transmitter MiniPOD. Hub Circuit Diagram 23 indicates which of these MGT Transmitters needs to include a logic inversion so that all 8 of these Transmitter MiniPOD fibers provide a right-side-up light signal.

Rec_MP_Fiber_?_to_FPGA_ Dir/Cmp

These 4 MGT inputs come from the Receiver MiniPOD. Hub Circuit Diagrams 22 and 23 indicate which of these links need to be inverted in the MGT receiver in order to compensate in a polarity flip in the trace routing.

MGT_FO_CH_??_OUT_Hub_ Dir/Cmp

These are the 74 MGT inputs to the Hub FPGA that carry the FEX readout data and the readout data from the Other Hub. Hub Circuit Diagrams 22 and 23 indicate which of these MGT Receivers need to invert their input signal. These 74 signals are specified by their MGT_Fanout_Channel number.

Combined_Data_from_OTHER_Hub_ Dir/Cmp

This signal is an MGT Input to the Hub FPGA. As indicated in Hub Circuit Diagram 22 the MGT receiver for this signal needs to invert it to compensate for the polarity flip in the Hub circuit board traces.

This_RODs_Readout_Ctrl_to_GTH_Input_ Dir/Cmp

This is the MGT input for the Readout Control data from the ROD on This Hub. Hub Circuit Diagram 23 indicates that this MGT Receiver should be setup to provide a logic inversion to properly receive this data.

Note that this high bandwidth link from the ROD to the Hub FPGA was provided so that if the ROD ever needs to send a lot Readout Control information to the FEX data sources that we can provide such a data path (i.e. to match the bandwidth of the Combined Data links to the FEX cards).

On the other hand if the ROD only needs to send one bit On/Off Readout Control to the Hub FPGA then one of the ROD-Hub TBD spare links could be used to transport that simple type of Readout Control.

MHz_320.64_COPY_?_ Dir/Cmp

These 8 clocks are the MGT Reference clock inputs to the Hub FPGA. They have been spread through out the 20 MGT Quads so that no MGT Transceiver needs to go further than the adjacent Quad to get its reference clock signal. These are AC coupled LHC locked clock signals. All clock polarities have been kept right-side-up to keep clock duty factor uncertainty from turning into clock jitter. See Hub Circuit Diagram 41.

21 Appendix 8: Hub-Module IPMC Connections

The Hub Module design includes a large number of connections to the IPMC mezzanine card. These connections are described in following sections of this document and are shown in **Figure 33**, **Figure 34** and **Figure 35** as well as **Figure 36**.

21.1 Connections Shown in Figure 33

Backplane IPMB A and B:

The IPMC is connected to the Shelf Manager by the two IPMB buses. The A and B IPMB Buses enter the Hub Module on the Zone 1 connector and have a rather long path up to near the top of the IPMC socket. These two I2C buses are routed to keep them away from noise sources as much as possible.

Slot Hardware Address:

The 8 Slot Hardware Address signals allow the Hub Module to know what slot it is in but not what Shelf it is in in the overall L1Calo system it is in. The Slot Hardware Address enters the Hub Module on its Zone 1 connector and is routed up to near the top of the IPMC socket. Hear next to the IPMC socket are located the 4.99k Ohm pull-up resistors to IPMC_3V3 and the 100 nFd noise bypass capacitors.

A point to note is that both the IPMC and the Hub's FPGA need to know the Slot Hardware Address. This is accomplished by also running these 8 signals to a 3V3 Select I/O Bank in the Hub's FPGA. These 8 connections to the Hub's FPGA include 470 Ohm isolation resistors.

A potential issue involves IPMC trying to read the Slot Hardware Address lines before the FPGA has powered up. In that situation these lines may be held low by the input protection diodes on the FPGA. If that is the case then stronger pull-ups will be used along with higher value isolation resistors. These are static signals so rather high value isolation resistors should be OK. In any case I don't think that this should require a full buffer for these signals.

Front Panel Switch:

The Hub Module uses a front panel switch that is permanently mounted to the back side of the PCB. The required sense of this switch is not well explained in the IPMC documentation. I believe that it should be "open" when the front panel handle is fully closed and latched. The switch wiring is up-side-down from common rational practice, i.e. the switch connects to 3V3 and uses a pull-down resistor) but it is connected as the IPMC document recommends.

21.2 Connections Shown in Figure 34

Front Panel LEDs:

The IPMC directly drives the 4 ATCA front panel LEDs. The required setup of these LEDs is not explained in the IPMC documentation. I believe that they use normal GPIO pins their ARM uProcessor to drive these LEDs. I believe that the user needs to supply the LED series resistor but this is never explained. I believe that they are trying to drive the anode of the LED (backwards from rational practice) but this is not explained in their document. On the Hub I have connected the LED cathode pin to Ground and put the series resistor between the LED anode and the LED pin on the IPMC.

Pay Load Enable Signal:

I believe that the Pay Load Enable signal goes Hi when it wants to turn ON the card. Opto-Coupler isolation is used between the IPMC and the Control pin on the Isolated +12V power supply. The cathode of this LED is Grounded and its anode is tied to the IPMC's 12V_Enable pin through a 330 Ohm LED series resistor.

The Opto-Coupler's LED will illuminate when the IPMC's 12V_Enable pin goes HI, and will turn ON the Opto-Coupler's transistor and will turn ON the Isolated +12V supply.

To allow power up the Hub Module in the absence of an IPMC or on the bench in the absence of a Shelf Manager for the IPMC to talk to, I have included two jumper locations JMP5 and JMP6. Install JMP5 and remove JMP6 for normal operation controlled by the IPMC. Install JMP6 and remove JMP5 to turn on the Hub's Isolated +12V supply all of the time.

Note that the 12V_Enable signal is also routed to the Hub's power supply supervisor circuits. This signal is used both as part of the startup sequence for the Hub Module's DCDC converters and also during the shutdown sequence. This 12V_Enable signal falling is the first indication that the Hub is going to power down. Using this signal to shutdown the Hub's DCDC converters allows then time to ramp down before the Isolated +12V power bus falls below threshold.

Power Entry Module Alarm:

The single Alarm pin signal from the ATCA Power Entry Module is connected to the ALARM_A pin on the IPMC. This connections includes a 4.99k Ohm pull-up to IPMC_3V3. The Hub Module makes no connection to the IPMC's ALARM_B pin.

Management I2C Bus:

The IPMC's Management I2C bus is connected to both the ATCA Power Entry Module and to the FRU-SDR EEPROM. The I2C bus address of the Power Entry Module is set by resistor R955 connected between its pin #10 and Ground. The IPMC documentation does not say what I2C address it expects the Power Entry Module to appear at. The FRU-SDR EEPROM is a ST Micro M24256 that is configured by its Ex pins to appear as 32k words of

8 bits at I2C address 1010000. The EEPROM's WC pin is tied Low to allow write operations.

21.3 Connections Shown in Figure 35

Power for the IPMC:

3.3 Volt power for the IPMC is supplied by the ATCA Power Entry Module. This power bus is called IPMC_3V3 and is used only by the IPMC and the components immediately associated with it. The IPMC_3V3 bus is energized any time that the Power Entry Module receives backplane 48 Volt power.

IPMC Ethernet Port:

The Hub Module provide the Ethernet Magnetics and RJ45 connector for the IPMC. The current IPMC is a 10/100 speed only device that uses only 2 of the 4 pairs in the standard Ethernet connection. This device requires an old "current" mode type of connection to its magnetics. The Hub Module provides the required environment the existing IPMC and can also be setup via jumpers for a 10/100/1000 speed voltage mode operation that a future IPMC would most likely require.

The Ethernet connection to the IPMC is via a front panel RJ45 connector on the Hub Module. In this way the IPMC can be connected to the DCS Ethernet in a 2 Hub Shelf or operated with a single Ethernet up-link in a one Hub test setup.

Shelf Address:

The IPMC needs to obtain the Shelf Address of the shelf that it finds itself in from the Shelf Manager. Then the IPMC needs to make the Shelf Address available on 8 of its User I/O output pins. These IPMC User I/O pins are connected to pins on the Hub's FPGA through isolation resistors. The point of this is to send the Shelf Address to the Hub FPGA. The Hub FPGA will use a combination of this Self Address and the Slot Hardware Address to generate the Ethernet Address that it will use for IPBus communication.

A combination of the Shelf Address and the Slot Hardware Address is also sent to the ROD so that it can also generate the Ethernet Address that its FPGA will use for IPBus communication.

Sensor I2C Bus

The IPMC Senor I2C Bus is used to collect monitoring data about power supply voltages and currents and device temperatures on the ROD and Hub. The IPMC will forward this hardware monitoring information over Ethernet to the Atlas DCS system. The layout of the Sensor I2C Bus is shown in **Figure 36**.

As shown in this drawing, three I2C bus buffer/translators are used both to drive the large number of devices on this bus, a combination of ROD and Hub devices, and also to translate between the sections of the Sensor I2C Bus that are 3V3 and the sections that are 1V8 level

I2C bus. The buffer/translator part that is used on the Hub is the Linear Technology LTC4315. If necessary these buffer/ translators can also be used to separate the various sections of overall Sensor I2C bus under control of the Hub FPGA.

At times other devices will need to initiate and master cycles on the Sensor I2C Bus, e.g. to setup parameters in the GE DCDC power converters on both the ROD and Hub modules. A User I/O input pin on the IPMC to disable its collection sweeps of monitoring data might be useful during the short and infrequent periods when other devices need to initiate and master cycles on this bus.

I2C Addresses on the Sensor I2C Bus

ROD	Binary	Decimal	TI-GE Octal
FPGA Master	0100 000	32	--
LM82 Temp Monitor	0011 001	25	--
MDT040 1V0	0011 010	26	32
MDT040 1V05	0011 011	26	33
PDT012 1V2	0011 100	28	34
PDT006 1V8	0011 101	29	35
PDT006 2V5	0011 110	30	36
PDT006 3V3	0011 111	31	37
SI5338 Clk Gen	1110 000	112	--
Hub	Binary	Decimal	TI-GE Octal
FPGA Master	0101 001	41	--
FPGA Sys Mon Slv	0101 010	42	--
MDT040 FPGA_CORE	0110 000	48	50
UDT020 MGT_AVCC	0110 001	49	51
UDT020 MGT_AVTT	0110 010	50	52
PDT012 SWCH_1V2	0110 011	51	53
PDT012 BULK_1V8	0110 100	52	54
UDT020 FAN_1V8	0110 101	53	55
PDT020 BULK_3V3	0110 110	54	56

Note that a number of addresses are reserved:

0:12, 40, 44, 45, 55, 64:68, 72:75, 99, 120:127 all in decimal.

The MSB of the address of the GE/TI converters must be zero.

Decimal means take the whole 7 bit I2C address and represent it as a decimal number.

TI-GE Octal means take the 6 least significant address binary bits and represent them as 2 octal digits, i.e. the setup of the address programming resistors on the TPS40400.

2362 *JTAG Master and Slave Ports*

2363 The Hub Module make no connection to the IPMC's master or slave JTAG ports.

2364

2365

2366

2367

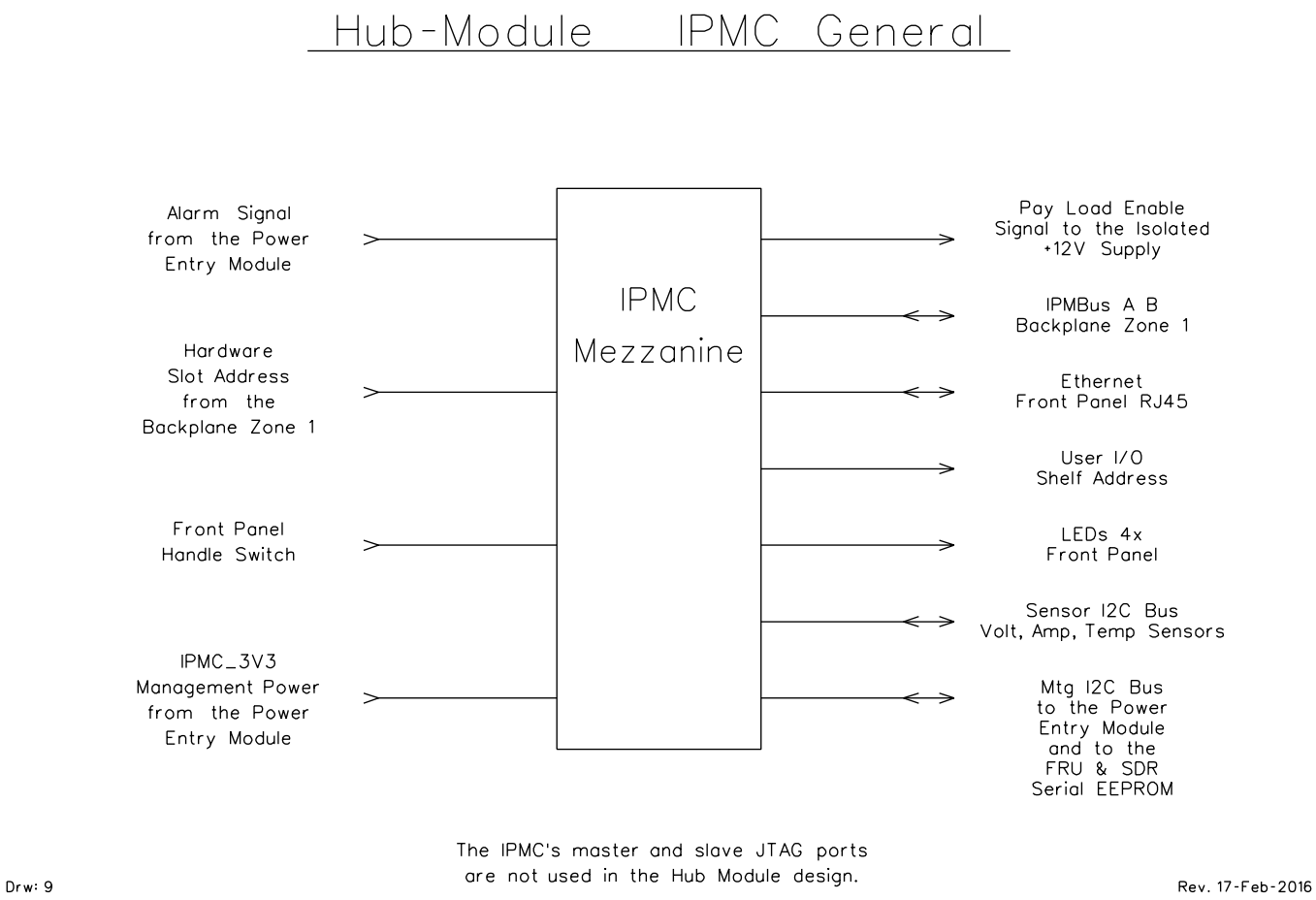


Figure 32: General circuit diagram for Hub IPMC connections.

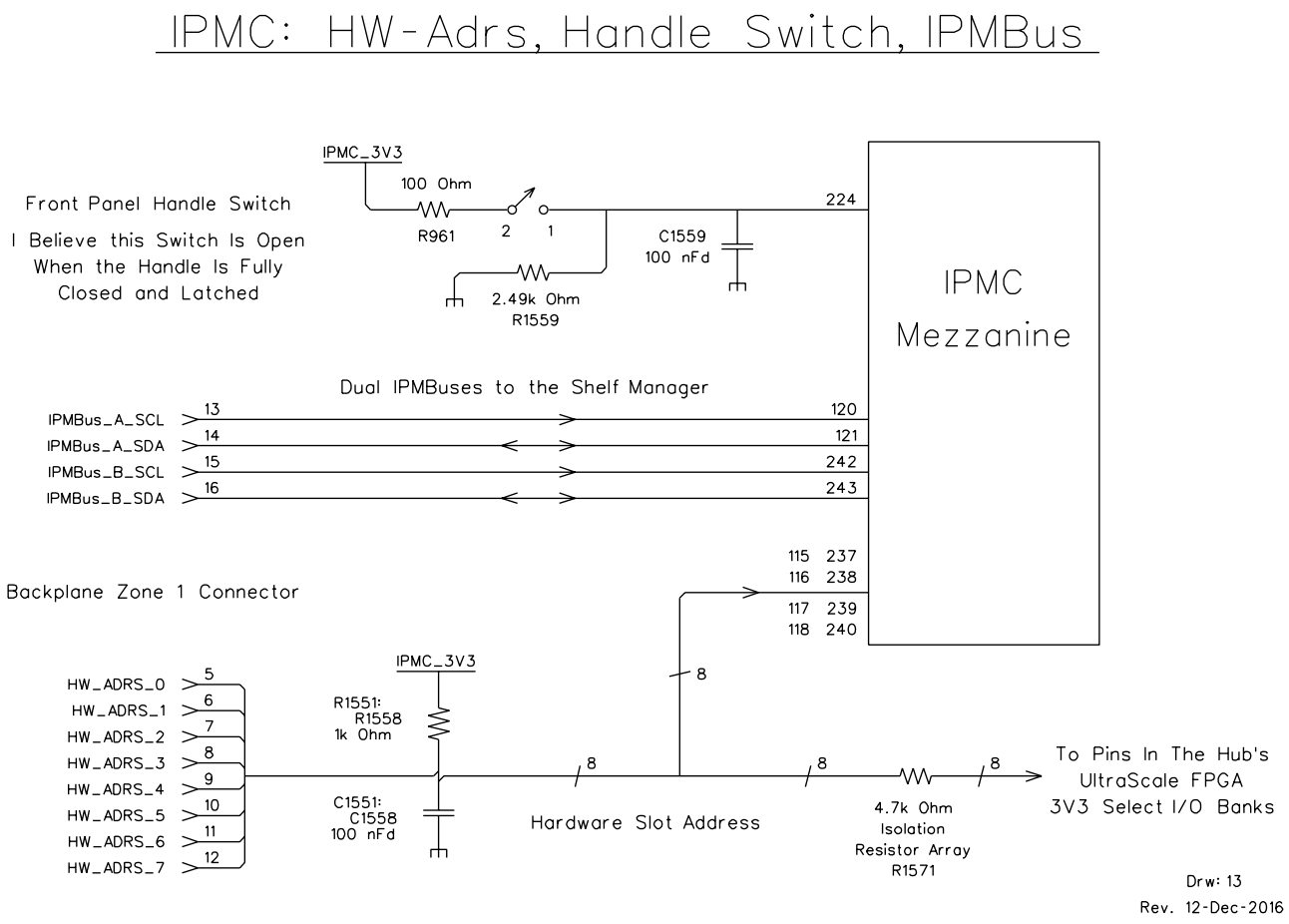


Figure 33: Hub IPMC circuit diagram (1/3)

2368

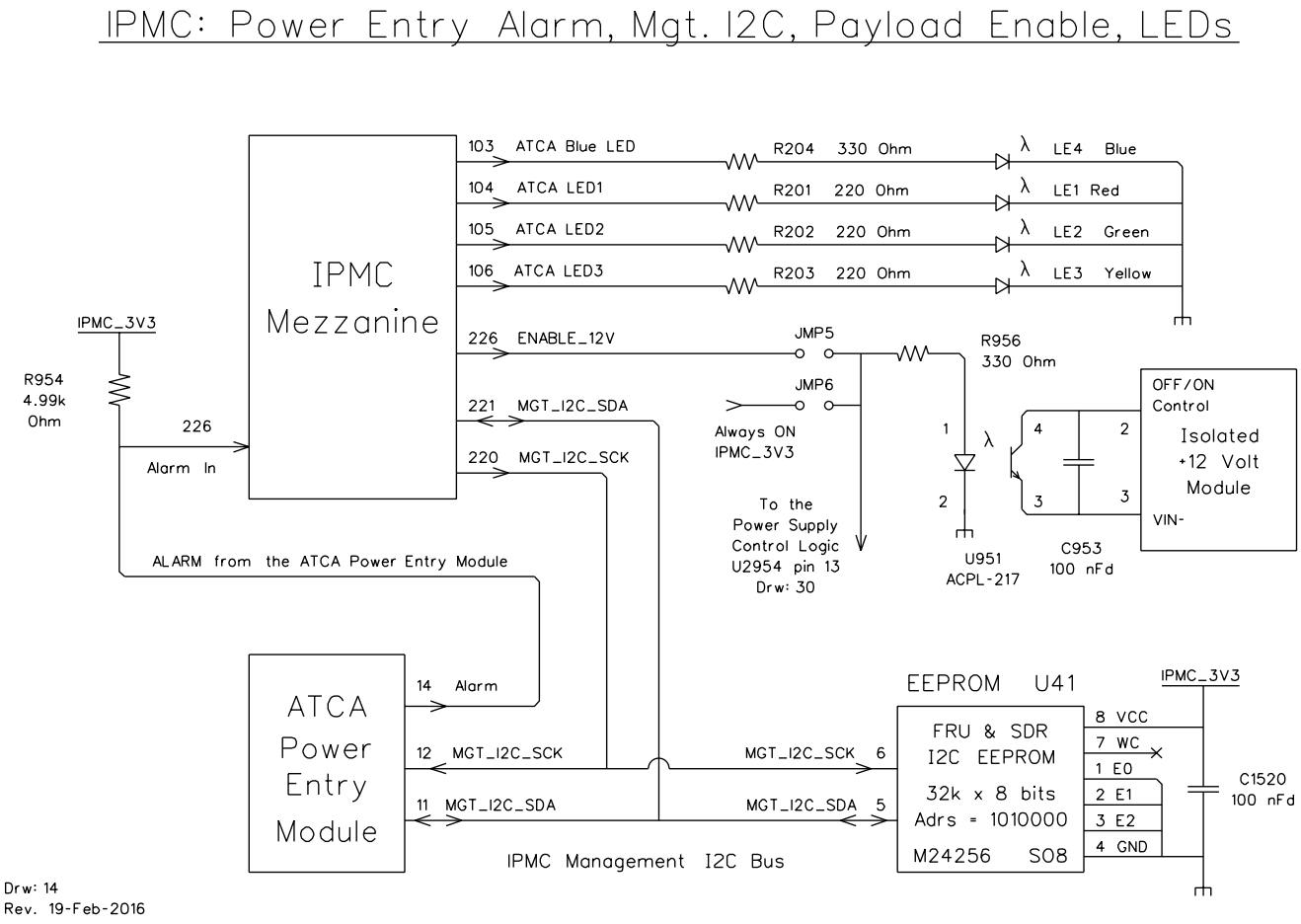


Figure 34: Hub IPMC circuit diagram (2/3)

2369

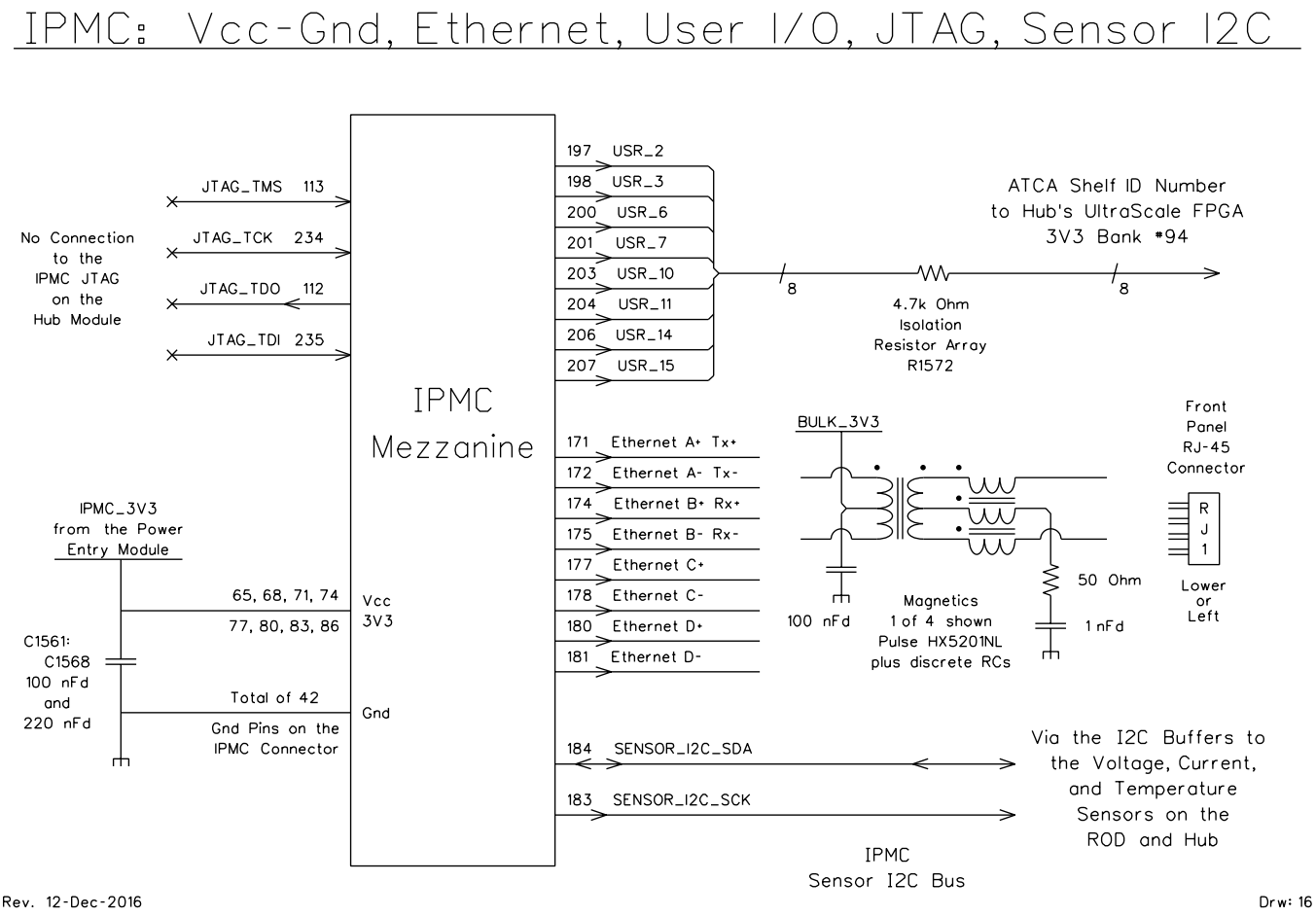


Figure 35: Hub IPMC circuit diagram (3/3)

2370

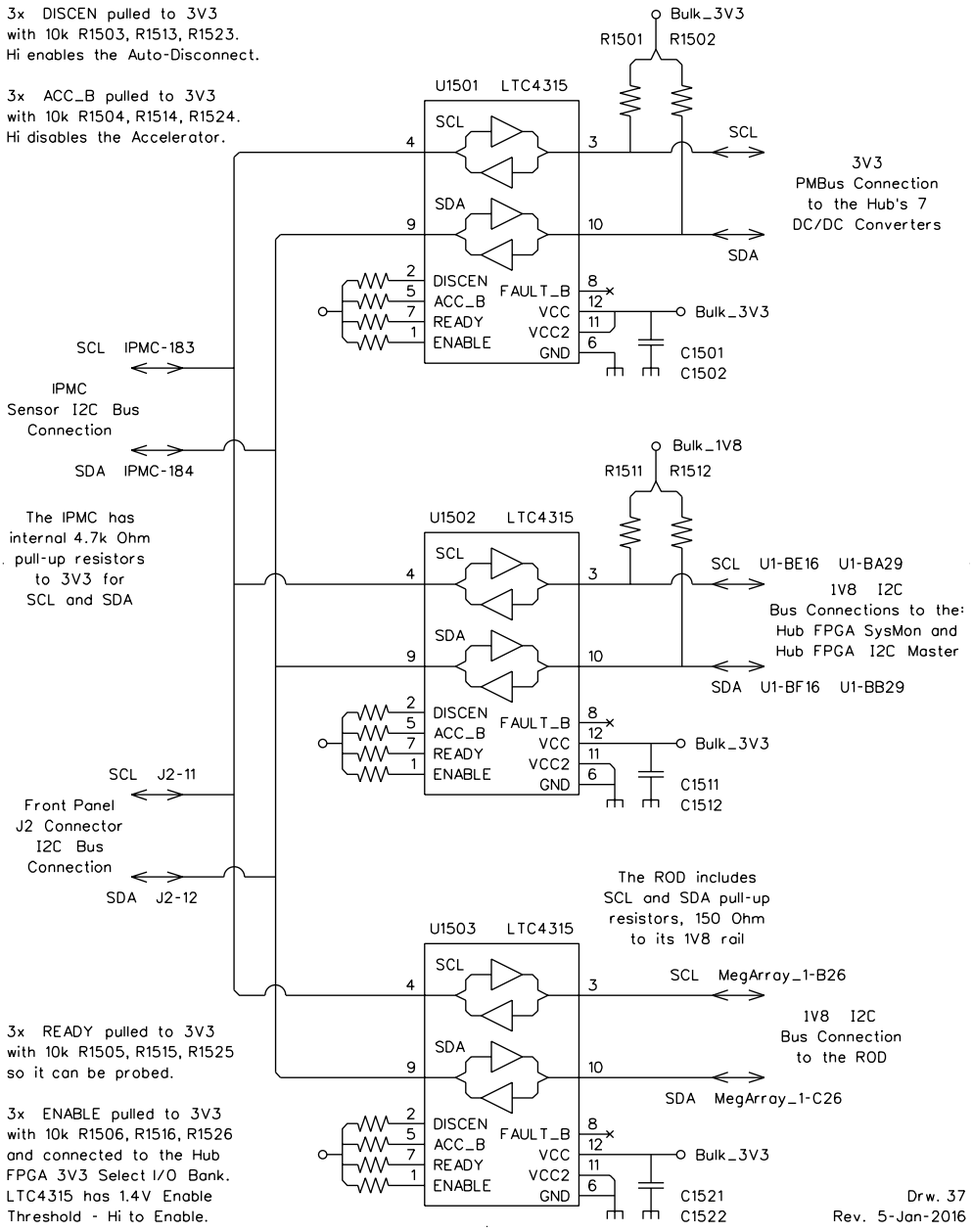


Figure 36: Hub I2C sensor bus circuit diagram.

22 Appendix 9: Hub-Module JTAG String

The Hub Module provides a front panel JTAG connection via its J2 "Access Connector". The layout of the Hub Module's JTAG string is shown in **Figure 37**.

This JTAG string runs to components on both the ROD and Hub:

- On the ROD this JTAG string connects only to the ROD's FPGA.
- On the Hub this JTAG string connects only to the Hub's FPGA.

This JTAG string is not connected to either the IPMC's "master" or "slave" JTAG ports.

Jumpers locations are provided so that the JTAG string can be jumpered around the Hub's FPGA if necessary.

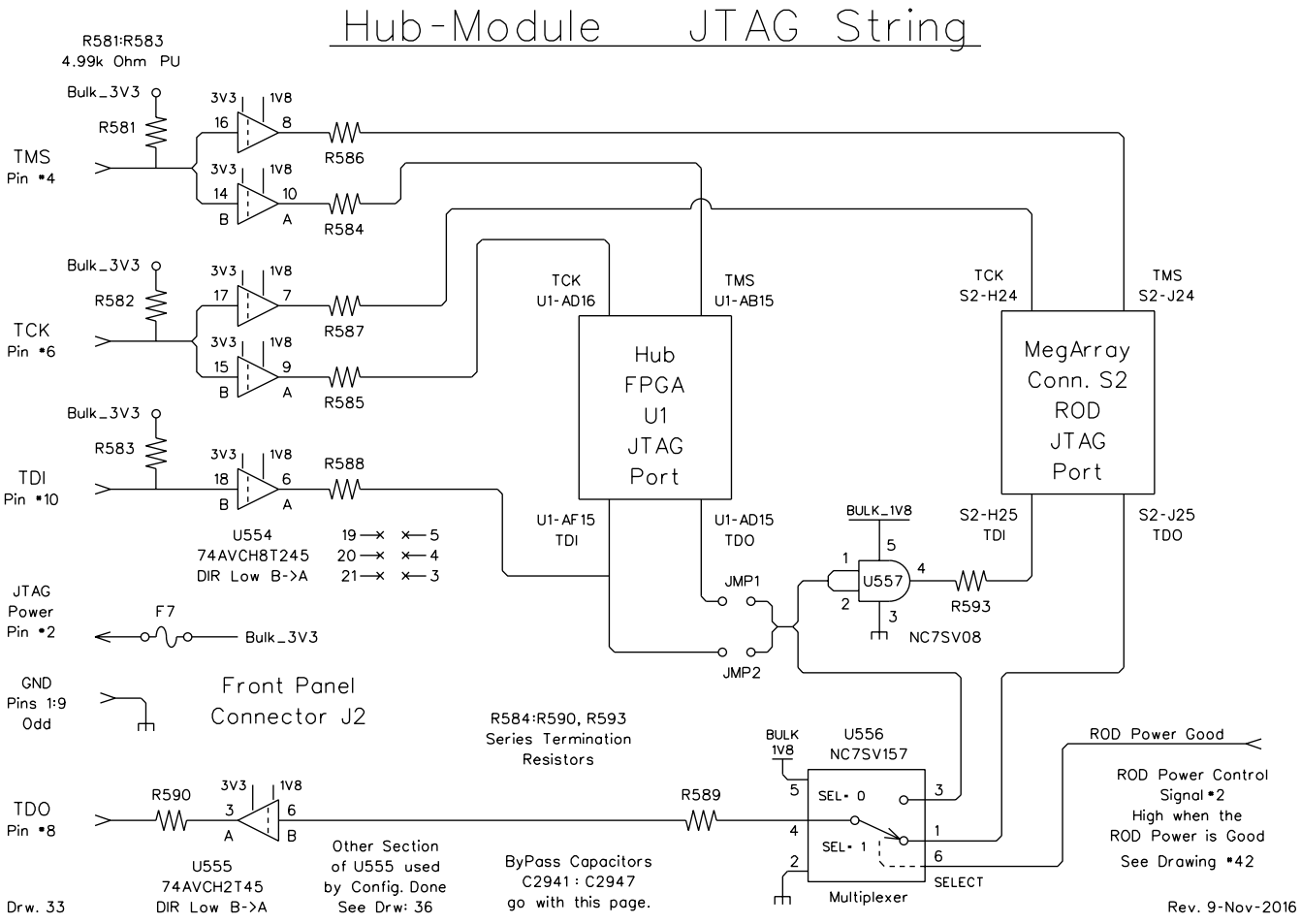
An automatic jumper is provided so that this JTAG string jumpers around the ROD when the ROD Power Control signal #2 is not asserted. Power Control #2 is the ROD's "Power Good" signal.

Note that even though the Hub provides this automatic jumper around the ROD for cases when the ROD is either not installed or is installed but not yet powered up, one will probably still need to reset the JTAG string when a new device appears on it or a device drops out.

The JTAG signal level at the Hub's from panel is 3V3 CMOS. The pinout of the Hub front panel JTAG connection is standard for Xilinx signal/ground pair type of JTAG wiring and includes a fused 3V3 reference pin.

The front panel pin-out and a typical JTAG cable setup to plug a JTAG "pod" into the Hub's front panel access connector is shown in **Figure 38**.

On the Hub Module the JTAG signals are buffered and translated to 1V8 levels. The JTAG signal level to the ROD is 1.8 Volt.



2408

2409

Figure 37: Hub circuit diagram for JTAG string.

2410

23 Appendix 10: Hub-Module Jumpers

This note collects in one place a description of all of the jumpers on the Hub Module except for the jumpers associated with the 3 Switch Chips. The Switch Chip jumper are described in Section 30.

All of these jumpers are typically used to control various functions on the Hub Module that need to be defined during the power up process or that can not be controlled through IPBus registers.

23.1 IPMC Ethernet A/Tx, B/Rx, Mag CT to 3V3, R1405 & R1410

IPMC Ethernet A/Tx B/Rx circuits magnetics primary side center tap connection to the 3.3V bus. The issue is that all of the connections to the Hub's Ethernet Magnetics use modern "voltage mode" connections except for the IPMC. The IPMC uses an old "current mode" National/TI DP83848 Phys chip. This current mode connection to the Magnetics requires that the center taps on the primary side be connected to the 3V3 bus. The normal 100 nFd capacitor from the primary center taps to ground is used for either voltage mode or current mode connections to the Magnetics.

The two jumpers that make these connections are R1405 and R1410.

Default setup:

For the current version of the IPMC with a current mode Phys chip we need to install both of these jumpers to tie the center taps to 3V3. These are Zero_Ohm jumpers. If a newer version of the IPMC is ever made then we may need to remove these jumpers.

- R1405 R1410 Installed

23.2 Virtex FPGA Configuration Mode R1811 through R1816

These 6 jumpers control the M2, M1, and M0 Configuration Mode pins on the Virtex FPGA. Normally this FPGA is Configured via Master BPI mode from its dedicated Parallel NOR Flash Memory device U25. The Master BPI mode requires the three M lines to be set: 0,1,0.

Never install both the HI and LOW jumpers for a given signal. Installed jumpers are to be 100 Ohm resistors.

Install R1816 to pull M2 LOW R1815 to pull M2 HI

Install R1814 to pull M1 LOW R1813 to pull M1 HI

Install R1812 to pull M0 LOW R1811 to pull M0 HI

Default setup:

Select Master BPI Configuration Mode.

Set M2, M1, M0 to: 0, 1, 0.

- R1812, R1813, R1816 Installed

- R1811, R1814, R1815 NOT installed

23.3 Power On Reset Delay Override R1821 and R1822

These two jumpers control how long the FPGA waits after it has powered up until it begins its Configuration process. This delay allows time for the Parallel NOR Flash Configuration Memory to wake up and get itself organized. The options are Standard Delay or Shorter Delay. These two jumpers control the state of the FPGA's POR_OVERRIDE pin.

Never install both the Standard and Short Delay jumpers at the same time. These are Zero Ohm jumpers.

Install R1821 for a Shorter Delay
Install R1822 for a Standard Delay

Default Setup:

We want the Standard Delay.

- R1822 Installed
- R1821 NOT Installed

23.4 Configuration Bank Voltage Select R1823 and R1824

These two jumpers are used to VCCO voltage range of BANK 0 and of the Configuration part of Bank 65 during Configuration. The two ranges are: 3V3/2V5 and 1V8 and under. These jumpers control the state of the FPGA's CFGBVS_0 pin.

Never install both jumpers at the same time.

These are Zero Ohm jumpers.

Install R1823 for 3V3/2V5 voltage range Configuration
Install R1824 for 1V8 and under voltage range Config

Default Setup:

We need the 1V8 and under voltage range Configuration.

- R1824 Installed
- R1823 NOT Installed

23.5 Pull-Ups During Configuration R1825 and R1826

These two jumpers are used to control whether or not the FPGA turns on weak pull-ups during its Configuration process. The weak pull-ups are on all of its Select I/O pins and can be used to define a fixed state of these CMOS signals during the Configuration process, i.e. no floating receiver inputs. These two jumpers control the state of the FPGA's PUDC_B_0 pin.

Never install both jumpers at the same time.

These are 100 Ohm jumpers.

1. Install R1825 to turn OFF the weak pull-ups
2. Install R1826 to turn ON the weak pull-ups

during Configuration
Default Setup:

We select to turn on weak pull-ups during Configuration.

- R1826 Installed
- R1825 NOT Installed

23.6 VBATT R1827

Jumper R1827 connects the FPGA's VBATT pin to ground.

Default Setup:

We are not using VBATT so we want to connect this FPGA pin to Ground. This is a Zero Ohm jumper.

- R1827 Installed

23.7 JTAG Skip the Hub FPGA JMP1 and JMP2

Jumpers JMP1 and JMP2 control whether or not the JTAG string on the Hub Module includes the Hub's Virtex FPGA. Normally we want to include the Hub's FPGA in the JTAG string. Install either JMP1 or JMP2 - never install both at once.

Install JMP1 (and remove JMP2) to include the

Hub's FPGA in the JTAG string

Install JMP2 (and remove JMP1) to skip over the

Hub's FPGA in the JTAG string

Default Setup:

We want to include the Hub's FPGA in the JTAG string.

- JMP1 Installed
- JMP2 NOT Installed

23.8 DONE Included in ROD Power Control JMP3 and JMP4

Jumpers JMP3 and JMP4 control whether or not the Hub FPGA Configuration DONE signal is included in the "AND" gate that generates the power enable signal to the ROD mezzanine card.

Install JMP3 (and remove JMP4) to INCLUDE the Hub FPGA Configuration DONE signal when generating the power enable signal to the ROD mezzanine.

Install JMP4 (and remove JMP3) to IGNORE the Hub FPGA Configuration DONE signal when generating the power enable signal to the ROD mezzanine. Note that if used JMP4 can be a 1k Ohm resistor.

Default Setup:

We want to include the Hub FPGA Config DONE signal.

- JMP3 Installed
- JMP4 NOT Installed

23.9 Wait for IPMC Payload Enable Signal JMP5 and JMP6

Jumpers JMP5 and JMP6 control whether or not the Hub card waits for the IPMC Payload Enable signal before starting up its Isolated +12V power supply. JMP5 JMP6 are Zero Ohm jumpers.

Install either JMP5 or JMP6 - never install both at once.

With JMP5 installed the Payload Enable signal from the IPMC is connected to the LED in the opto-coupler that turns on the Isolated +12V power supply.

With JMP6 installed the IPMC's Payload Enable signal is disconnected. Instead the constant auxiliary 3V3 supply from the ATCA Power Entry module is used to always enable the Isolated +12V power supply and to provide the power enable signal to the Hub power supply control logic via U2954.

Default Setup:

We want to use the IPMC to Enable the Isolated +12V power supply and thus control the startup of the Hub Module.

- JMP5 Installed
- JMP6 NOT Installed

23.10 Hub Phys Chip Jumpers R1901:R1914, R1951:R1964

The Hub Module has two KSZ9031RNX Phys chips. There are 14 jumpers associated with each of these Phys chips. These jumpers are resistors that bias a pin in one direction or the other and this value is read when the Phys chip first powers up or is reset.

The KSZ9031RNX has 9 pins (called "Strapping Options") that are read in this way at power up. Because of space limitations and because there is an obvious why that the Hub Module wants some of these Strapping Options set, 4 of them have only one jumper to pull that pin in the direction that is obviously needed for rational operation of the Hub Module.

The following is a list of all of the jumpers that are associated with each Phys chip on the Hub Module.

Option	Pull-Up	Pull-Down
PHYAD0	R1901	R1902
PHYAD1	R1903	R1904
PHYAD2	R1905	R1906
Mode_0	R1911	R1912
Mode_1	R1909	R1910
Mode_2	R1908	---
Mode_3	R1907	---
CLK125_EN	R1913	---
LED_Mode	R1914	---

This table shows the Reference Designators for Phys chip U21. Phys chips U22 has the same setup but its Reference Designators are higher by 50.

In all cases, if installed, the pull-up resistor should be 10k Ohms and the pull-down resistor should be 1k Ohm.

The PHYADx jumpers set the address of the Management Interface Port on the KSZ9031RNX. The Management Port PHYAD bits 3 and 4 are internally always set to 0,0. To set one of these three PHYAD bits HI install the associated pull-up resistor. To set one low install the pull-down resistor.

The Hub Module provides easy control of only the Mode_0 and Mode_1 lines. This provides the following 4 options for the Phys chip (Mode bits listed Mode_3, ..., Mode_0).

1100 RGMII 1000 Base-T fullduplex only
1101 RGMII 1000 Base-T full or half duplex
1110 RGMII 10/100/100 all but 1000 half duplex
1111 RGMII 10/100/1000 full or half duplex

CLK125_EN is pulled up by R1913 thus enabling the Phys chip to send its 125 MHz clock back to the MAC in the Hub's FPGA.

LED_Mode is pulled up by R1914 thus setting up the Phys chip for Single LED mode.

Default Setup:

Note that Phys chips U21 and U22 are setup with the same Management Port PHYAD which is OK because they each have their own private Management Power connection in the Hub's FPGA.

- PHYADx:
  - Set the 3 controllable PHYAD lines Low.
  - Install 1k Ohm in R1902, R1904, R1906.
  - Leave R1901, R1903, R1905 open.
- Mode:
  - Set all Mode lines Hi.
  - Install 10k Ohm in R1907 R1908 R1909 and R1911.
  - Leave R1910 and R1912 open.

- *CLK125_EN:*
  - *Enable the 125 MHz Clock*.
  - Install a 10k Ohm resistor in R1913.
- *LED_Mode:*
  - *Enable Single LED Mode*.
  - Install a 10k Ohm resistor in R1914.

23.11 DCDC Converter with LC Output Filter Feedback Jumpers

3 of the DCDC Converters on the Hub Module include an LC Output Filter to reduce the switching noise that is present in their output voltage. These 3 converters include jumpers to provide some options in how their control loop feedback is setup. These 3 converters and their jumpers are:

DCDC-2 MGT_AVCC	JMP1051	JMP1052	JMP1053	JMP1054
DCDC-3 MGT_AVTT	JMP1101	JMP1102	JMP1103	JMP1104
DCDC-7 FAN_1V8	JMP1301	JMP1302	JMP1303	JMP1304

Jumpers JMP1051, JMP1052 (and JMP1101, JMP1102 and JMP1301, JMP1302) control whether the the V_SENSE_+ feedback is taken before or after the output filter inductor. JMP1051 selects before the output inductor and JMP1052 selects after the inductor.

Jumpers JMP1053, JMP1054 (and JMP1103, JMP1104 and JMP1303, JMP1304) control whether the the RC coupled feedback is taken before or after the output filter inductor. JMP1053 selects before the output inductor and JMP1054 selects after the inductor.

During initial pro-type manufacturing none of these 4 jumpers will be installed by the assembly company.

23.12 ATCA "Shelf Ground" to "Logic Ground" Connection R959

ATCA Specification 4.96 requires a jumper that can optionally macke a connection between the ATCA Shelf Ground and the ATCA Logic Ground. On the Hub Module this optional link between these ground systems is made by R959.

Install a zero Ohm jumper at R959 to connect the Shelf and Logic Grounds.

Note that one could also use a high value resistor so that there are not significant currents or loops between these two ground systems will still providing a path to remove static charge from the card.

Default Setup:

A 1 Meg Ohm resistor will be installed in location R959.

23.13 Jumper on the Sensor I2C Bus EEPROM

U1541 is a soic_8 location that can hold a M24256 EEPROM that appears on the Hub's Sensor I2C bus. There are 4 jumpers associated with the operation of the EEPROM.

3. JMP1541 controls the chip's E0 Enable pin (aka Address Select)
4. JMP1542 controls the chip's E1 Enable pin (aka Address Select)
5. JMP1543 controls the chip's E2 Enable pin (aka Address Select)

Zero Ohm jumper install --> Enable pin is Hi

Open --> Enable pin is Low

JMP1544 controls the chip's WC_B pin

Zero Ohm jumper install --> WC_B pin is Hi

--> Write operations are Disabled

Open --> WC_B pin is Low

--> Write operations are Enabled

Default Setup: Neither U1541 or any of the jumpers JMP1541:JMP1544 are installed.

24 Appendix 11: Hub-Module Front Panel LEDs

This note collects the information about the LED displays that are used on the front panel of the Hub Module. The Hub Module includes front panel LEDs to indicate the following:

- Four that are required by the ATCA format and are managed by the IPMC mezzanine
  - Mandatory LED_1
  - Optional LED_2
  - Optional LED_3
  - Mandatory Blue
- Two general health/rationality LEDs
  - Has the IPMC Enabled the Pay Load Power ?
  - Are all of the Hub's DCDC Converters running OK ?
- Five LEDs for the ROD Mezzanine
- Three LEDs for the Hub Module that are managed by the Hub's Virtex FPGA.
- Six RJ-45 Ethernet connectors with 2 LEDs each
  - RJ1 Upper/Right for This Hub's IPMC
  - *RJ1 Lower/Left for This Hub;s ROD Mezzanine FPGA*
  - *RJ2 Upper/Right for This Hub's Switch Chip "C"*
  - *RJ2 Lower/Left for This Hub's Switch Chip "A"*
  - *RJ3 Upper/Right for This Hub's Switch Chip "B"*
  - *RJ3 Lower/Left for This Hub's Switch Chip "B"*
- Two LEDs each for 20 other Ethernet connections
  - Switch Ports to the FEXs
  - *1 This Hub's Switch Port to the Other Hub's FPGA*
  - *1 This Hub's Switch Port to This Hub's FPGA*
  - 1 This Hub's FPGA Phys to the Other Hub's Switch
  - 1 This Hub's FPGA Phys to This Hub's Switch
  - *1 Switch Chip "A" side of A <--> B connection*
  - *1 Switch Chip "B" side of A <--> B connection*
  - *1 Switch Chip "B" side of B <--> C connection*
  - *1 Switch Chip "C" side of B <--> C connection*

This is a total of 66 front panel LEDs. An illustration of the layout of these LEDs on the front panel is shown in **Figure 38**, **Figure 39** and **Figure 40**.

The 4 ATCA LEDs use the 3mm Mentor 1271.100x "single column" light pipes to reach the front panel.

The 2 General Health LEDs also use the same 3mm Mentor 1271.100x light pipes.

The 5 ROD LEDs, and the 3 Hub LEDs, and the 40 "Other Ethernet Connections" LEDs use the 2mm Mentor 1296.10x4 light pipe array. This is a 4 column light pipe array. They are layed out in a 4x2 array and a 4x10 array.

The Hub Module uses SMD LEDs on side 1 of the PCB and light pipe assemblies to route them to the front panel. This design is driven by the need to place the required ATCA LEDs in specific locations and to use very little space along the West edge of the card for these LEDs.

The LEDs are in two categories: single column and 4 column. Note that in this document the words row and column refer to viewing the Hub Module from the front as it normally looks when plugged into a crate, i.e. columns are vertical along the long axis of the front panel.

The single column setup has a 3.0 mm diameter light pipe that is centered 5.08 mm to the right of the side 1 surface of the PCB. This uses a Mentor 1271.100x light pipe and an Osram LED:

LxT673 P-LLC-2 3.0x3.4 package Vf Blue typ 2.9/3.1 at 5/10 mA

Hyper TOPLED Blue, Green Vf Grn typ 2.8/3.0 at 5/10 mA

2006

LxT676 P-LLC-2 3.0x3.4 package Vf Red typ 1.9/1.95 at 5/10 mA

Hyper TOPLED Red, Yellow Vf Yel typ 1.9/1.95 at 5/10 mA

2007

Many other Osram parts in the 2-PLCC Advanced Power TOPLEDs are available.

The 4 column setup has 1.95 mm Mentor 1296.10x4 light pipes. The first light pipe is centered 2.54 mm to the right of the side 1 surface of the PCB. The next light pipe is centered 2.54 mm to the right of the first one and so on. Center to Center the rows are spaced by 5.08 mm. This provides some limited space for labels. This 4 column setup with the Mentor 1296.10x4 light pipe array uses an Osram LED in the 0805 case size package:

LG R971 green Vf about 2.0 to 2.1 at 5 to 10 mA

LS R976 super red Vf about 1.9 at 5 to 10 mA

LY R976 yellow Vf about 1.9 at 5 to 10 mA

Many other 0805 case size types are available from Osram for example: LH R974 hyper red.

Ed needs a blue LEDs in this 4 column setup for the ROD display. Osram does not seem to make one in the correct package to work with the Mentor 1296.10x4 light pipes. The problem is to find a quality blue LED in the 0805 package size with the right optics to put light into the light pipe and the same suggested PCB layout pattern. So far the Avago HSMR-C170 looks OK except for the PCB layout pattern.

24.1 LEDs Driven by the IPMC Mezzanine

These are the 4 ATCA Status LEDs that are driven by the IPMC mezzanine card. I believe that the IPMC mezzanine directly drives the anodes of these LEDs through series resistors and that the cathodes of these LEDs are just tied to ground. See also the 2 IPMC Ethernet LEDs that are listed below under "not driven".

LED Ref Desgntr	Display	Source -Pin
LE1	ATCA Mandatory Red LED_1	IPMC Mezz Socket 104
LE2	ATCA Optional Green LED_2	IPMC Mezz Socket 105
LE3	ATCA Optional Red LED_3	IPMC Mezz Socket 106
LE4	ATCA Mandatory Blue	IPMC Mezz Socket 103

24.2 LEDs Driven by the Switch Chips

The switch chips used in the Hub module can drive up to 4 LEDs per ethernet port. Control registers in these chips allow you to select what types of information about a given ethernet port are displayed on its LEDs.

The Hub module provides 2 LEDs per switch chip ethernet port. By default one of these LEDs shows if the port is operating at 10/100 vs 1000 speed and the other LED shows if a connection exists on that port and when a connection exists whether or not it is currently moving data.

In the following table for LE5:LE40, the Speed LED is Green and the Link Activity LED is Yellow.

In the section of the table that describes the front panel RJ-45 connectors recall that these are TE Connectivity part number 1888653-4 "condo" connectors. The -4 indicates the LED colors for each socket:

TE Part No.	LED_1	LED_2	LED_3	LED_4
1888653-4	Green	Green	Yellow	Yellow

Note, if we change which switch port is connected to which Base Interface target then we should also change the connections to these LEDs to keep them in rational BI Channel order.

Recall which 53128 Switch Chip LED Pin is used to indicate what information about a given 53128 Switch Chip Port:

Link Speed			Link Active		
Port	Pin Num	Pin Name	Port	Pin Num	Pin Name

7	168	LEDP0	7	170	LEDP1
6	174	LEDP4	6	175	LEDP5
5	178	LEDP8	5	179	LEDP9
4	184	LEDP12	4	185	LEDP13
3	189	LEDP16	3	190	LEDP17
2	194	LEDP20	2	195	LEDP21
1	198	LEDP24	1	199	LEDP25
0	256	LEDP28	0	1	LEDP29

These are the switch chip port numbers as defined in the 53128 documentation.

The switch chip LEDs are arranged on the Hub module front panel in the following way:

LED Ref Desgntr	Display	Source	Pin
LE5	BI “Channel 2” Speed Grn	Sw Chip B Port 5	LED8-178
LE6	BI “Channel 2” Lnk-Act Yel	Sw Chip B Port 5	LED9-179
LE7	BI Channel 3 Speed Grn	Sw Chip C Port 5	LED8-178
LE8	BI Channel 3 Lnk-Act Yel	Sw Chip C Port 5	LED9-179
LE9	BI Channel 4 Speed Grm	Sw Chip C Port 4	LED12-184
LE10	BI Channel 4 Lnk-Act Yel	Sw Chip C Port 4	LED13-185
LE11	BI Channel 5 Speed Grn	Sw Chip C Port 3	LED16-189
LE12	BI Channel 5 Lnk-Act Yel	Sw Chip C Port 3	LED17-190
LE13	BI Channel 6 Speed Grn	Sw Chip C Port 2	LED20-194
LE14	BI Channel 6 Lnk-Act Yel	Sw Chip C Port 2	LED21-195
LE15	BI Channel 7 Speed Grn	Sw Chip C Port 1	LED24-198
LE16	BI Channel 7 Lnk-Act Yel	Sw Chip C Port 1	LED25-199
LE17	BI Channel 8 Speed Grn	Sw Chip C Port 0	LED28-256
LE18	BI Channel 8 Lnk-Act Yel	Sw Chip C Port 0	LED29-1
LE19	BI Channel 9 Speed Grn	Sw Chip A Port 5	LED8-178
LE20	BI Channel 9 Lnk-Act Yel	Sw Chip A Port 5	LED9-179
LE21	BI Channel 10 Speed Grn	Sw Chip A Port 4	LED12-184
LE22	BI Channel 10 Lnk-Act Yel	Sw Chip A Port 4	LED13-185
LE23	BI Channel 11 Speed Grn	Sw Chip A Port 3	LED16-189
LE24	BI Channel 11 Lnk-Act Yel	Sw Chip A Port 3	LED17-190
LE25	BI Channel 12 Speed Grn	Sw Chip A Port 2	LED20-194
LE26	BI Channel 12 Lnk-Act Yel	Sw Chip A Port 2	LED21-195
LE27	BI Channel 13 Speed Grn	Sw Chip A Port 1	LED24-198
LE28	BI Channel 13 Lnk-Act Yel	Sw Chip A Port 1	LED25-199
LE29	BI Channel 14 Speed Grn	Sw Chip A Port 0	LED28-256
LE30	BI Channel 14 Lnk-Act Yel	Sw Chip A Port 0	LED29-1
LE31	SW to Hub FPGA Speed Grn	Sw Chip B Port 4	LED12-184
LE32	Sw to Hub FPGA Lnk-Act Yel	Sw Chip B Port 4	LED13-185
LE33	Sw B to Sw A Speed Grn	Sw Chip B Port 2	LED20-194
LE34	Sw B to Sw A Lnk-Act Yel	Sw Chip B Port 2	LED21-195
LE35	Sw B to Sw C Speed Grn	Sw Chip B Port 3	LED16-189
LE36	Sw B to Sw C Lnk-Act Yel	Sw Chip B Port 3	LED17-190
LE37	Sw A to Sw B Speed Grn	Sw Chip A Port 7	LED0-168
LE38	Sw A to Sw B Lnk-Act Yel	Sw Chip A Port 7	LED1-170
LE39	Sw C to Sw B Speed Grn	Sw Chip C Port 7	LED0-168
LE40	Sw C to Sw B Lnk-Act Yel	Sw Chip C Port 7	LED1-170

And now the RJ-45 LEDs driven by the Switch Chips			
LED Ref Desgntr	Display	Source	Pin
LED_59	RJ2-LED2 Grn	RJ2 Upper or Right Sw Chip C Port 6	LED4-174
LED_60	RJ2-LED3 Yel	Sw Chip C Port 6	LED5-175
LED_61	RJ2-LED1 Grn	RJ2 Lower or Left Sw Chip A Port 6	LED4-174
LED_62	RJ2-LED4 Yel	Sw Chip A Port 6	LED5-175
LED_63	RJ3-LED2 Grn	RJ3 Upper or Right Sw Chip B Port 7	LED0-168
LED_64	RJ3-LED3 Yel	Sw Chip B Port 7	LED1-170
LED_65	RJ3-LED1 Grn	RJ3 Lower or Left Sw Chip B Port 6	LED4-174
LED_66	RJ3-LED4 Yel	Sw Chip B Port 6	LED5-175

24.3 LEDs Driven by the Phys Chips on the Hub Module

The two KSZ9031RNX Phys chips on the Hub Module each drive two LEDs. These LEDs are not directly driven by the Phys chips but rather they are driven through a buffer. The Hub's Phys chip LEDs are arranged on the front panel in the following way:

LED Ref Desgntr	Display	Source	Pin
LE41	Hub FPGA to Sw Link Grn	Phys U22	LED2-15
LE42	Hub FPGA to Sw Active Yel	Phys U22	LED1-17
LE43	Hub FPGA to BI Ch 2 Link Grn	Phys U21	LED2-15
LE44	Hub FPGA to BI Ch 2 Active Yel	Phys U21	LED1-17

24.4 LEDs Driven by the ROD Mezzanine Card

The ROD mezzanine controls two types of LEDs on the Hub Module. It controls 5 LEDs that indicate the "Status" of the ROD and it controls two LEDs that indicate the operation of the ROD's Ethernet Phys chip which is also a KSZ9031RNX.

In all 7 cases the Hub module provides buffering for the 1V8 logic control signals that come from the ROD for these LEDs. In all 7 cases the LED is illuminated when the control signal from the ROD is Low.

Note that an 8th control signal from the ROD is used to set the state of the front panel Lemo connector on the Hub. The Hub provides an open collector driver for this Lemo. When this control signal from the ROD is Hi then this open collector Lemo driver pulls down.

LED Ref Desgntr	Display	Source	Pin
LED_57	RJ1-LED1 RJ1 Lower or Left Lnk Grn	MegArray S1	B1
LED_58	RJ1-LED4 RJ1 Lower or Left Act Yel	MegArray S1	B2
LED_45	Prog_Done_LED_B Green	MegArray S1	B3

J1	LEMO not an LED	MegArray S1	B4
LED_46	Pwr_Good_LED_B Green	MegArray S1	C1
LED_47	SMB_Alert_LED_B RED	MegArray S1	C2
LED_48	GP_LED_B Blue	MegArray S1	C3
LED_49	Run_LED_B Blue	MegArray S1	C4

ROD MegArray Conn Specification			
MegArray S1 Pin#	Old Name	New Current Name	LED Color
B1	LED-0	Phy_LED2_B	Green
B2	LED-Y	Phy_LED1_B	Yellow
B3	LED-B	Prog_Done_LED_B	Green
B4	LEMO-0	LEMO not an LED	--
C1	LED-1	Pwr_Good_LED_B	Green
C2	LED-R	SMB_Alert_LED_B	RED
C3	LED-G	GP_LED_B	Blue
C4	LEMO-1	Run_LED_B	Blue

24.5 LEDs Driven by the Hub Module's FPGA

The Hub Module's FPGA directly controls 3 Front Panel LEDs using 3 of its Select I/O signals. The Hub provides buffers between its FPGA pins and these LEDs. The Select I/O signals that are used to control these 3 LEDs are listed in Section 19.

LED Ref Desgntr	Display	Source	Pin
LE50	Hub FPGA LED Grn	Hub FPGA Select I/O	--
LE51	Hub FPGA LED Yel	Hub FPGA Select I/O	--
LE52	Hub FPGA LED Red	Hub FPGA Select I/O	--

24.6 LEDs NOT Driven by the IPMC Card's Ethernet Connection

Besides the 4 "ATCA Status" LEDs listed above, the IPMC also could have driven LEDs to indicate the operation of its Ethernet circuit. The IPMC uses a National/TI DP83848 Phys chip which does directly drive LED but these pins were not routed out out on the IPMC to its edge connector. So as far as I know we cannot directly see the status of the ethernet connection to the IPMC mezzanine card. There is still the issue of what to do with these LEDs in the Hub's RJ-45 Ethernet connector for the IPMC.

LED Ref Desgntr	Display	Source	Pin
LED_55	RJ1-LED2 RJ1 Upper or Right Green	---	
LED_56	RJ1-LED3 RJ1 Upper or Right Yellow	---	

24.7 Two Rationality LEDs

There are two front panel LEDs that show the general health of the Hub Module. These two LEDs indicate to the user whether or not it is "rational" to consult the other LEDs on the card.

- One of these LEDs (LED 53) shows whether or not the Isolated +12V supply is running.
- The other LED (LED 54) shows whether or not all of the power buses on the Hub Module are operating within tolerance.

The cathode of the Iso +12V LED is connected to ground. The anode of this LED is connected through a series resistor to the Iso_12V bus. This is LED 53.

The anode of the All Power OK LED is tied through a series resistor to the BULK_3V3 bus. The cathode of this LED is tied to the source of the low active All Power Is OK signal, i.e. U2961 pin 4. This is LED 54.

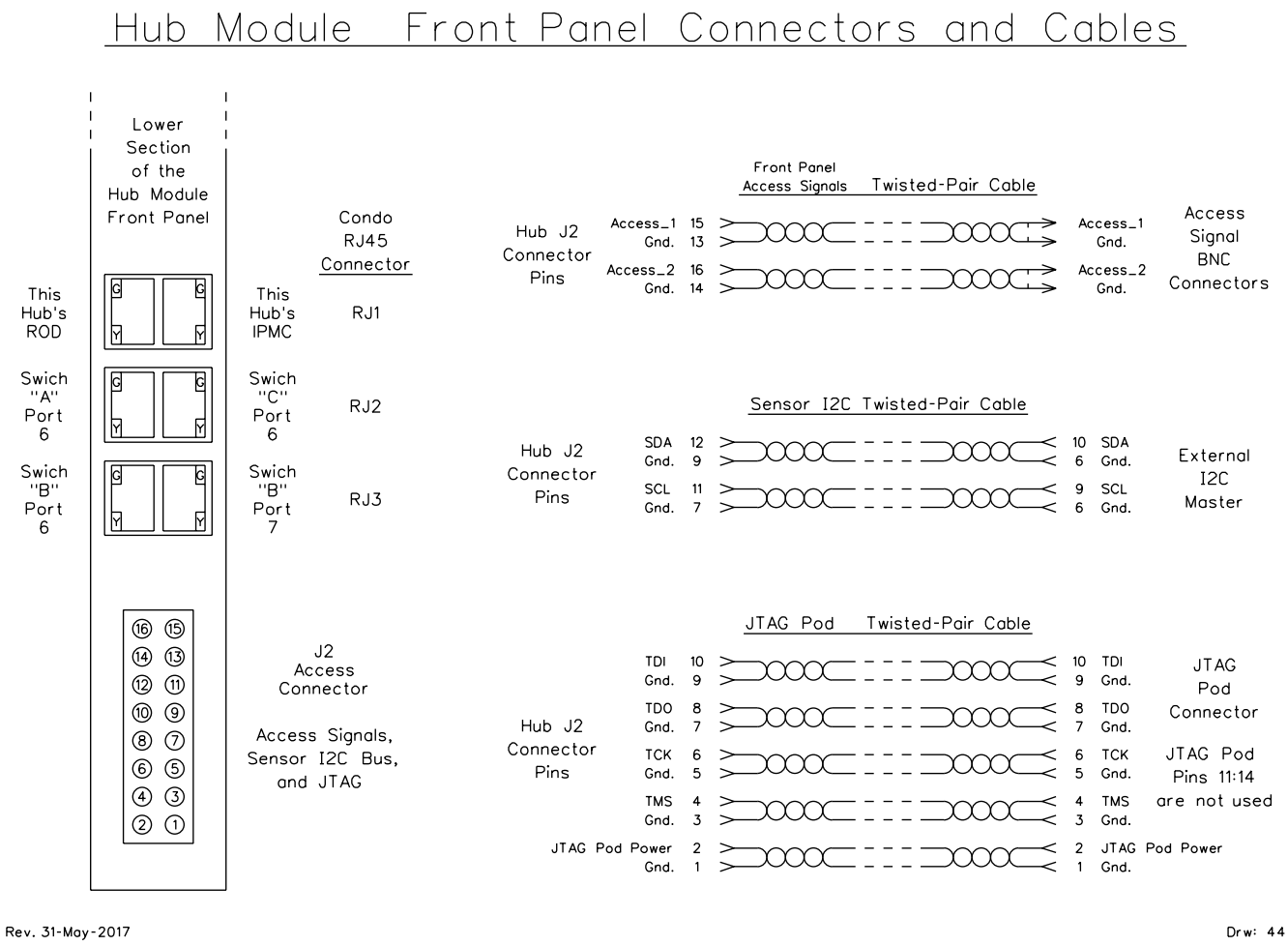


Figure 38: Illustration of Hub front-panel connections.

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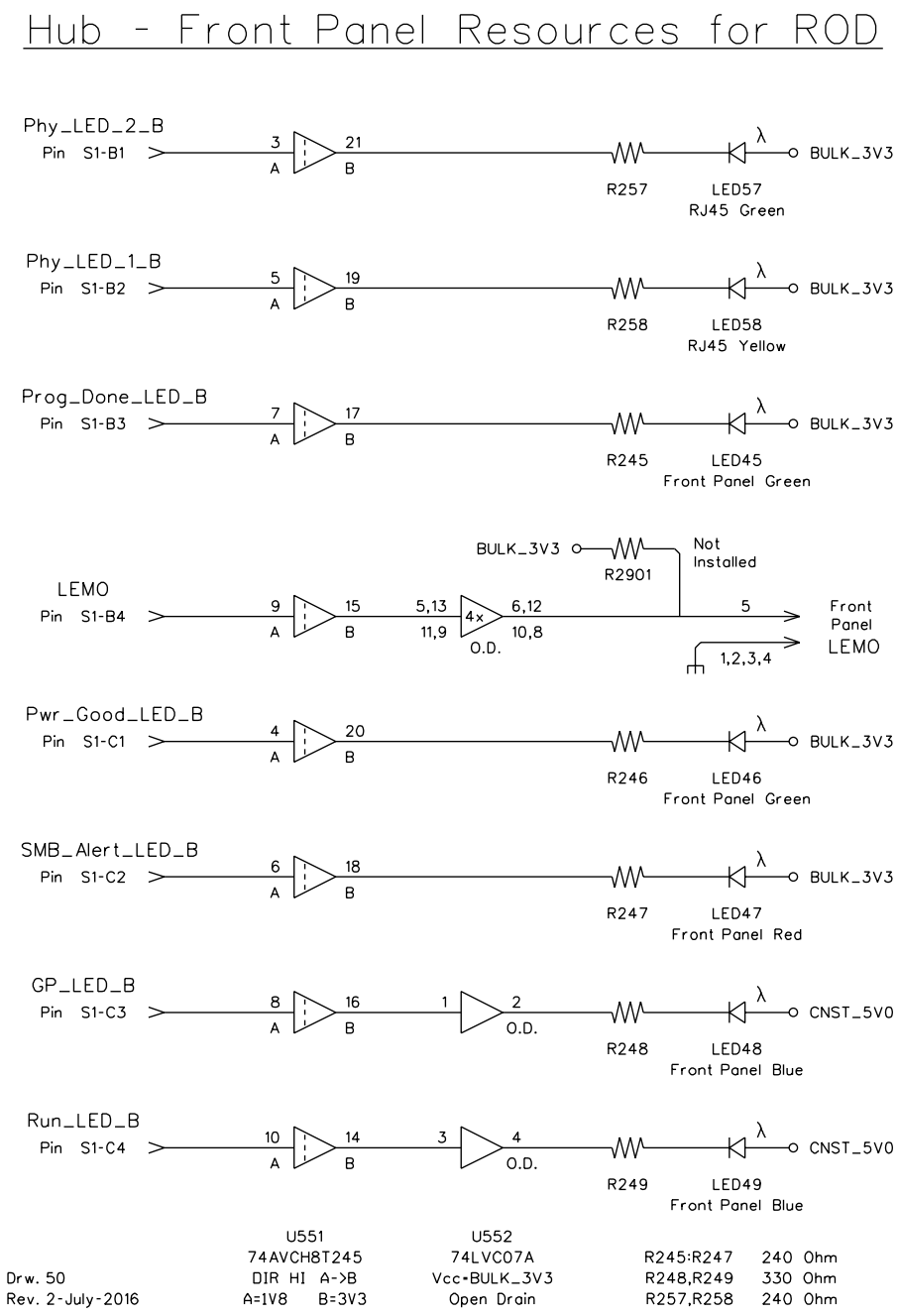

Figure 39: Hub front-panel resources for the ROD mezzanine.

2777

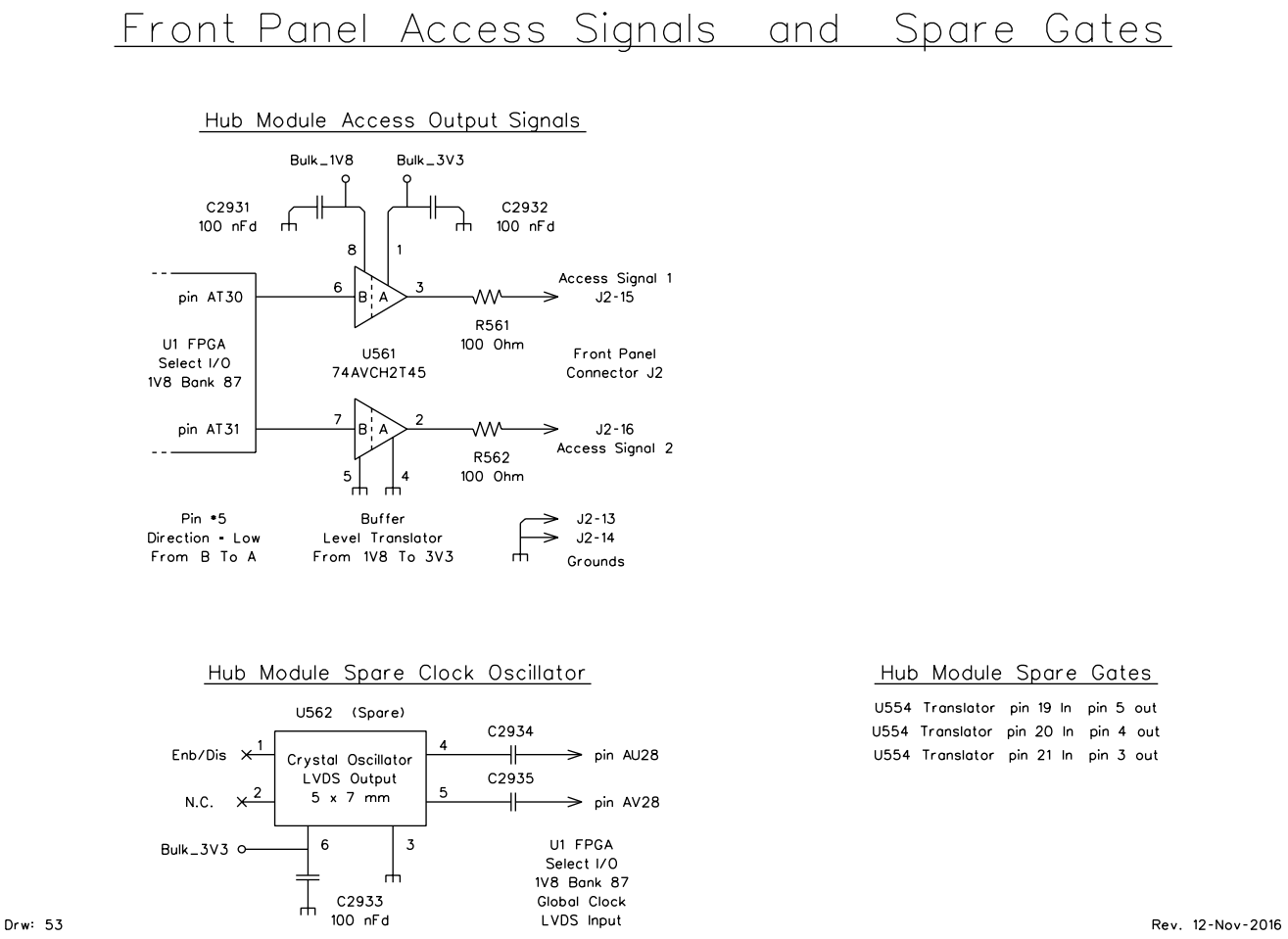

Figure 40: Hub front-panel access signals and spare gates.

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25 Appendix 12: Hub-Module MiniPOD Connections

The Hub Module includes 2 MiniPODs: 1 Transmitter MiniPOD and 1 Receiver MiniPOD. Details about the connections to a Hub Module MiniPOD are shown in **Figure 41**.

Only 8 of the 12 channels in the Transmitter MiniPOD are connected to MGT transmitter outputs on the Hub's FPGA. MiniPOD fibers: 3, 5, 7, 9 are not connected to the FPGA.

The 8 attached MiniPOD fibers are connected to MGT outpu ports in the following order:

Transmitter MiniPOD Fiber	MGT Quad and Port
0	227 Tx2
1	227 Tx0
2	226 Tx2
4	226 Tx0
6	225 Tx2
8	225 Tx0
10	224 Tx2
11	224 Tx0

These Quads are GTH type MGT transceivers in SLR 0 of the FPGA. These connections are listed in Section 18 and are shown in **Figure 30**.

Only 4 channels from the Receiver MiniPOD are connected to MGT receivers in the Hub;s FPGA. The connected Receiver MiniPOD fibers are shown in the following table:

Receiver MiniPOD Fiber	MGT Quad and Port
2	224 Rx2
4	224 Rx1
6	224 Rx2
8	124 Rx0

Quad 224 is of the GTH type and Quad 124 is of the GTY type. Both of these Quads are in SLR 0 of the FPGA. These MiniPOD connections are capacitor coupled using 100 nFd 0201 size coupling capacitors. The trace routing from fiber 8 to Quad 124 Port Rx0 is particularly complicated and may not support high-speed operation.

The 8 remaining Receiver MiniPOD fibers have no connection on the Hub's FPGA. Recall that one of these fibers is used to receiver the Optical Felix TTC clock and data signal. These connections are listed in Section 18 and are shown in **Figure 29** and **Figure 30**.

Monitoring and control of the two MiniPODs is provided by a separate "TWB" from the Hub's FPGA to each MiniPOD. Both MiniPODs have their TWB Address set at zero. Each MiniPOD has its own Interrupt_B and Reset_B lines connecting it to the Hub FPGA. Pull-up

resistors are provided for the TWB SDA and SCL lines as well as for the interrupt and reset lines so the Hub FPGA does not need to provide the pull up current.

Filtered 2.5 Volt and 3.3 Volt power is separately supplied to each MiniPOD from the bulk supplies on individual isolated power fills.

The design of the heat sinks for these MiniPODs must take into consideration: the ATCA height limitation, the ROD mezzanine air flow requirements, and the near by Hub FPGA heat sink.

The two ribbons of optical fibers for these MiniPODs will uses the backplane optical MPO connectors to exit the Hub via its Rear Transition Module. Part numbers for 50 cm single 12-fiber ribbon Prizm to MPO cables are:

Molex 106267-2011 for the male MPO connector and

Molex 106267-2001 for the female MPO connector

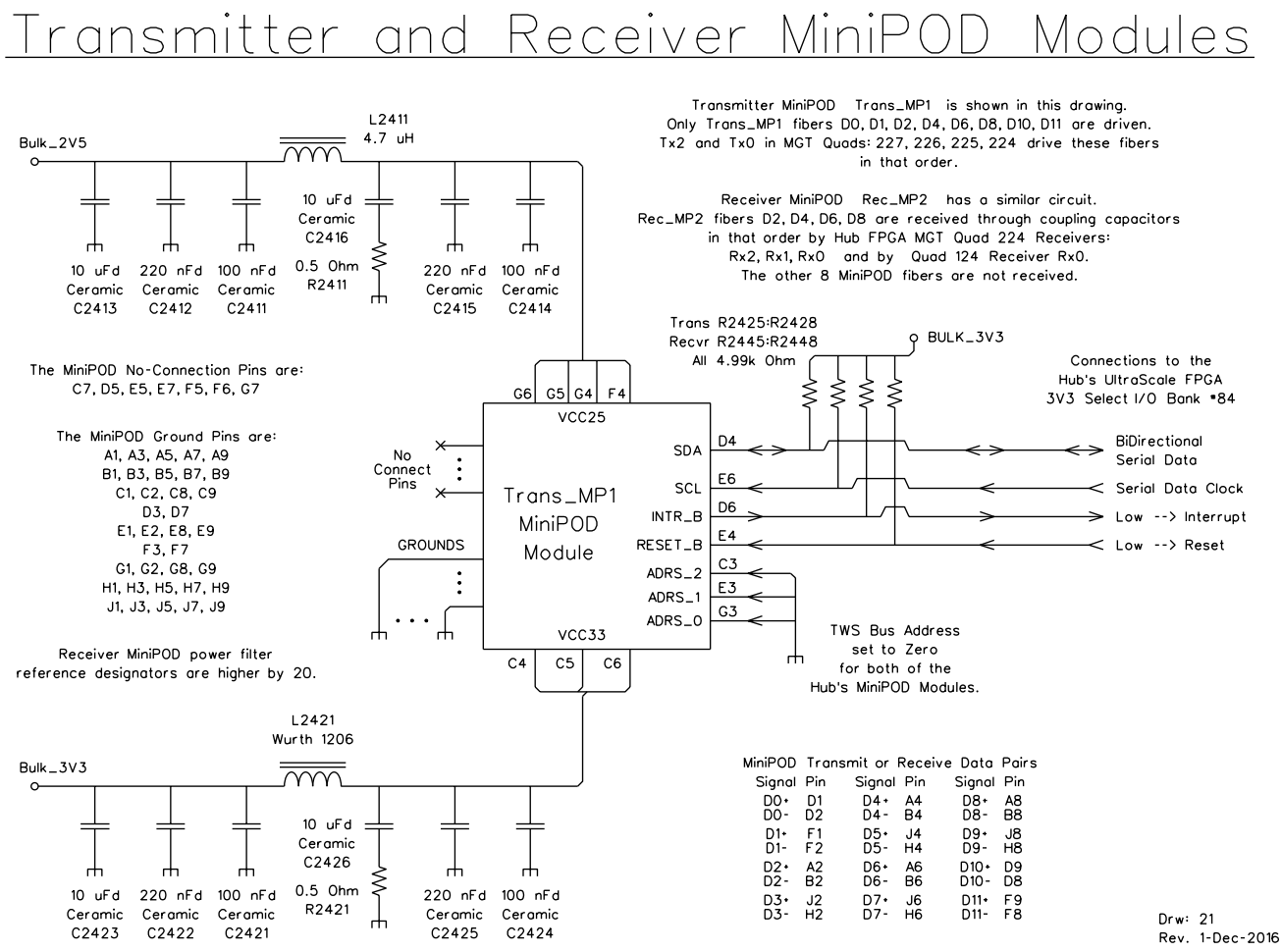

Figure 41: Hub MiniPOD module circuit digrams.

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26 Appendix 13: Non-MGT Rod-Hub Connections

The intent of this note is to describe all of the non-MGT ROD-Hub connection signals. The Meg-Array pinout of these signals is presented in Ed's document, "ROD Hub Pinout" Rev. 1.4 from 6-May-2015.

26.1 JTAG

The Hub Module provides a front panel "Access" connector". One of the functions available on this J2 access connector is a JTAG string that runs to components on both the ROD and Hub.

On the ROD this JTAG string connects only to the ROD's FPGA.

On the Hub this JTAG string connects only to the Hub's FPGA.

This JTAG string is not connected to either the IPMC's "Master" or "Slave" JTAG ports.

Manually installed jumpers are provided so that the JTAG string can be jumpered around the Hub's FPGA. An automatic jumper is provided so that this JTAG string jumpers around the ROD when the ROD Power Good signal is not asserted.

The JTAG signal level at the Hub's front panel is 3V3 CMOS. The front panel pinout is standard for Xilinx signal/ground pair type of JTAG wiring and includes a fused 3V3 reference.

On the Hub Module the JTAG signals are buffered and translated to 1V8 levels. The JTAG signal level to the ROD is 1.8 Volt.

The Hub Module JTAG String is shown in **Figure 37**.

26.2 Sensor I2C Bus

The I2C Bus connection to the ROD is normally mastered by the IPMC's Sensor I2C port. The normal function of the Sensor I2C bus is to allow collection of monitoring information (e.g. power supply voltages and currents and device temperatures). The IPMC initiates and masters the Sensor I2C Bus cycles that collect this monitoring data. The Sensor I2C bus from the IPMC is shared by the ROD and the Hub and is used to collect the Atlas DCS monitoring information from both of them.

At times either the Hub or ROD FPGA may need to initiate and master a Sensor I2C Bus cycle for example to set a parameter in one of their GE power supplies. Thus not only sensors and GE power modules are connected to the Sensor I2C Bus but also both the Hub and ROD FPGAs make a master connection to this bus. In addition the Hub's FPGA makes a second slave only connection to the Sensor I2C Bus that provides a port to the System Monitor in the Hub's FPGA.

The I2C addresses are shared between the Hub and ROD on this IPMC Sensor I2C Bus.

Some parts of the overall Sensor I2C bus are 3V3 level and some parts are 1V8 level. The Hub Module provides the required translation and uses buffered translator chips, to provide the required drive for the large number of devices that are connected to the Sensor I2C Bus. These translators can have their ports enabled or disables under control of the Hub's FPGA.

The Hub's Sensor I2C Bus is shown in **Figure 36**.

Note that the Sensor I2C Bus can also be accessed from the front panel of the Hub Module via its J2 "Access Connector".

The ROD-Hub Sensor I2C bus has the potential problem that when a section of it is either powered off or has a power supply problem, that the the ESD diodes in the devices in that section of the bus may clamp the I2C signals to ground. Comments on this potential problem:

- We really only need monitoring information when the ROD Hub are up and running so a brief lack of monitoring data at the start of a normal power up is probably OK.
- It would be very useful the IPMC could report in its monitoring data when the Sensor I2C cycles are not working vs just sending junk data or no data to the DCS monitoring system.
- The Linear Technology I2C bus translators/buffers may automatically isolate stuck sections of the Sensor I2C bus and allow good monitoring data to be read from the sections of the bus that are fully powered up.
- It may be useful to run the Ready signals from the I2C bus translators/buffers back to the Hub FPGA so that it can see if a section of the Sensor I2C bus is stuck.

26.3 ROD Front Panel Signals

The ROD provides a total of 8 front panel control signals. The net-names of these signals, both old and new netnames are shown in the table below.

- **Figure 39** shows the resources on the Hub that are connected to these 8 front panel control signals from the ROD.
- Two of these front panel signals control the two LEDs in the RJ45 connector for the ROD.
- One of these front panel signals is the input to the LEMO driver and thus controls the output of the ROD's LEMO connector on the Hub's front panel.
- Five of these front panel signals control five of the LEDs on the Hub's front panel.
- All 7 of the front panel control signals from the ROD that control LEDs are Low active 1V8 logic signals. When these signals are voltage Low the LED illuminates.
- The one front panel control signal from the ROD that controls the LEMO output is also a 1V8 logic signal. When this control signal is voltage Low the open drain LEMO output pulls Low.
- All of these front panel signals from the ROD are 1V8 CMOS level, i.e. they do not directly drive the LEDs.
- Front panel signal table:

MegArray	Old	New	LED
S1_Pin#	Name	Current Name	Color
B1	LED-0	Phy_LED2_B	Green
B2	LED-Y	Phy_LED1_B	Yellow
B3	LED-B	Prog_Done_LED_B	Green
B4	LEMO-0	LEMO	--
C1	LED-1	Pwr_Good_LED_B	Green
C2	LED-R	SMB_Alert_LED_B	RED
C3	LED-G	GP_LED_B	Blue
C4	LEMO-1	Run_LED_B	Blue

- GP_LED_B is a General Purpose LED which can be used by firmware to signal some condition (TBD)
- "The Run_LED_B is the "Up and Running" signal that you had proposed a while back. It indicates to the Hub and to the Front Panel that the ROD is running a functional firmware image. This will not be turned on if the ROD is running an initialization, error recovery, or other engineering image.

- My configuration sequence is to always boot an engineering image first. That image will check to see the board context, and will then trigger the boot of the appropriate "RUN" image. I've allowed for the ROD to carry several images for [efex, gfex, jfex * hub1, hub2] + the engineering image = 7 configuration images.
- I will turn on "Run" when the second image has booted."

26.4 Clock 40.08 MHz

This is a clock signal from the Hub to the ROD. This 40.08 MHz clock is always running - even when the Hub is not receiving an Optical Timing reference signal from the LHC. This is an LVDS signal. It is AC coupled on the Hub before being sent to the ROD. It is synchronous with the Clock signal that the Hub sends to the other 12 FEX slots in the ATCA Shelf.

26.5 Geographic Address

These 8 lines are 1V8 signals from the Hub to the ROD.

The net-names of these signals are: LOC_ADD1:LOC_ADD8.

These signals indicate a unique Geographic Address within the overall L1Calo system. That is, these lines indicate both a Slot Number and a Shelf Number within the overall L1Calo system. These lines are not just the backplane Geographic Address signals from the ATCA Zone 1 connector.

The details of how the Hub obtains the Shelf Number and encodes the Shelf Nmbr + Slot Nmbr before sending it to the ROD on these 8 lines are currently being discussed with Ian and David.

26.6 Ethernet Connection

These 8 lines come from the Micrel KSZ9031RNX Phys chip on the ROD. The net-names of these signals are: TR01_P, TR01_N, through TR04_P, TR04_N. The Hub provides the "magnetics" and the RJ45 connector for the ROD's Base Interface Ethernet connection.

The components on the Hub are specified for 10/100/1000 Base-T operation. The components currently in the Hub design are Pulse Engineering HX5201NL magnetics and TE Connectivity 1888653-x connectors. The colors of the LEDs in the RJ45 connector are Green and Yellow.

Careful attention must be paid while routing the Hub to confirm that it correctly implements the polarity of the Ethernet signals coming from the ROD.

26.7 Module_Present

This ROD_PRSNT_B signal is pulled to Ground with a 1k Ohm resistor on the ROD. The Hub has a high value pull-up resistors on this signal. The resulting logic signal goes Low when the ROD is plugged in. This signal can be used to let the Hub FPGA know if a ROD mezzanine card is installed.

26.8 ROD-Hub Power Control Signals

All 4 of the Power Control Signals are 1V8 CMOS level logic signals. These are single ended signals and the direction of each of them is given below.

OK for ROD to Power Up: --- Net PWR_CON1

This is a signal from the Hub to the ROD that tells the ROD when everything on the HUB has been brought up and is running. By using this signal the ROD can delay its power up until the Hub is fully running and presenting a stable environment to the ROD.

The ROD includes a 1k Ohm pull-down resistor on this signal.

Before telling the ROD to power up the Hub will have configured its FPGA and will have all clocks running.

It will take several (many) seconds from the time that the Shelf Manager gives the Hub the OK to power up until the Hub gives the ROD the OK to power up.

During an overall power up sequence, once the Hub asserts the PWR_CON1 signal voltage Hi it will not return this signal Low until the Shelf Manager tells the Hub to turn off or the backplane 48V goes away or a process is started to re-power-up the ROD.

ROD Power Supplies Are All Running OK: --- Net PWR_CON2

This is a signal from the ROD to the Hub.

As soon as the ROD has all of its power supplies up and running with their outputs within the required voltage range then it will assert this signal.

The Hub will not "believe or use" any other signals that it receives from the ROD until this signal is asserted.

ROD Has Completed Its Power Up: --- Net PWR_CON3

This is a signal from the ROD to the Hub.

This signal means that the ROD is fully Configured and ready for normal L1Cal Trigger operation.

The Hub will not indicate to any other cards that it is ready to operate in the overall L1Calo system until this signal from the ROD is asserted.

Spare Power Control Signal: --- Net PWR_CON4

The spare Power Control signal will be routed to Select I/O pins on both the ROD and Hub FPGAs.

PWR_CON signals 2, 3, and 4 all run directly between the ROD and Hub FPGAs. The Hub includes 470 Ohm "isolation" resistors in these line to limit current flow before both FPGAs are both powered up and configured.

26.9 Spare Unused ROD-Hub HP IO Signals

We have a number of spare currently un-assigned signals between the ROD and the Hub. All of these signals are FPGA to FPGA HP IO lines.

- There are 8 spare HP IO lines in the Meg-Array pinout list. These are nicely setup as 4 LVDS pairs so that we can use them as LVDS or as single-ended signals, which ever may be required in the future.
- The net-names of these spare signals are: TBD_LINK0_P, TBD_LINK0_N, through TBD_LINK3_P, TBD_LINK3_N.
- Both ROD and Hub have routed these 8 signals as 4 differential pairs.
- When not used for some function, these 8 spare signals are to be operated with 1.8V single ended CMOS levels with the Hub driving and the ROD receiving. The Hub is required to tri-state its output drives for these signals any time that the ROD's Power Control #2 signal is NOT asserted HI. That is, the Hub will only drive these signals when the ROD reports that it is fully powered up. In any case, in this stand by service the Hub should use a low level of Drive current on these lines.
- In firmware, these unused spare HP IO lines between the ROD and Hub will be connected to IPBus visible registers so that we may test them to prove that they are OK, i.e. prove that our lifeboat floats.

26.10 Power from the Hub to the ROD

The Hub provides bulk +12 Volt power to the ROD that is isolated from the backplane 48 Volt power feed.. This power is the same Isolated +12V bus that feeds all of the DC/DC Converters on the Hub module itself.

The ROD may draw up to 100 Watts of this bulk +12V power, i.e. 8.3 Amps. This +12V power is sent to the ROD as soon as the Shelf Manager tells the Hub that it may power up.

The current parts in the Hub design that provide the bulk Isolated +12V power are: SynQor IQ65033QMA10SNF-G power entry module and SynQor PQ60120QEA25NNS-G Isolated +12V supply.

Note that the Isolated +12V supply module has a maximum capacitive load of 12,000 uFd that it can support when fully loaded with a resistive load. The Hub itself places 3118 uFd on the output of the Isolated +12V converter or about 26% of the assumed total available budget.

26.11 ROD-Hub MGT Signals

These signals are covered in Section 18.

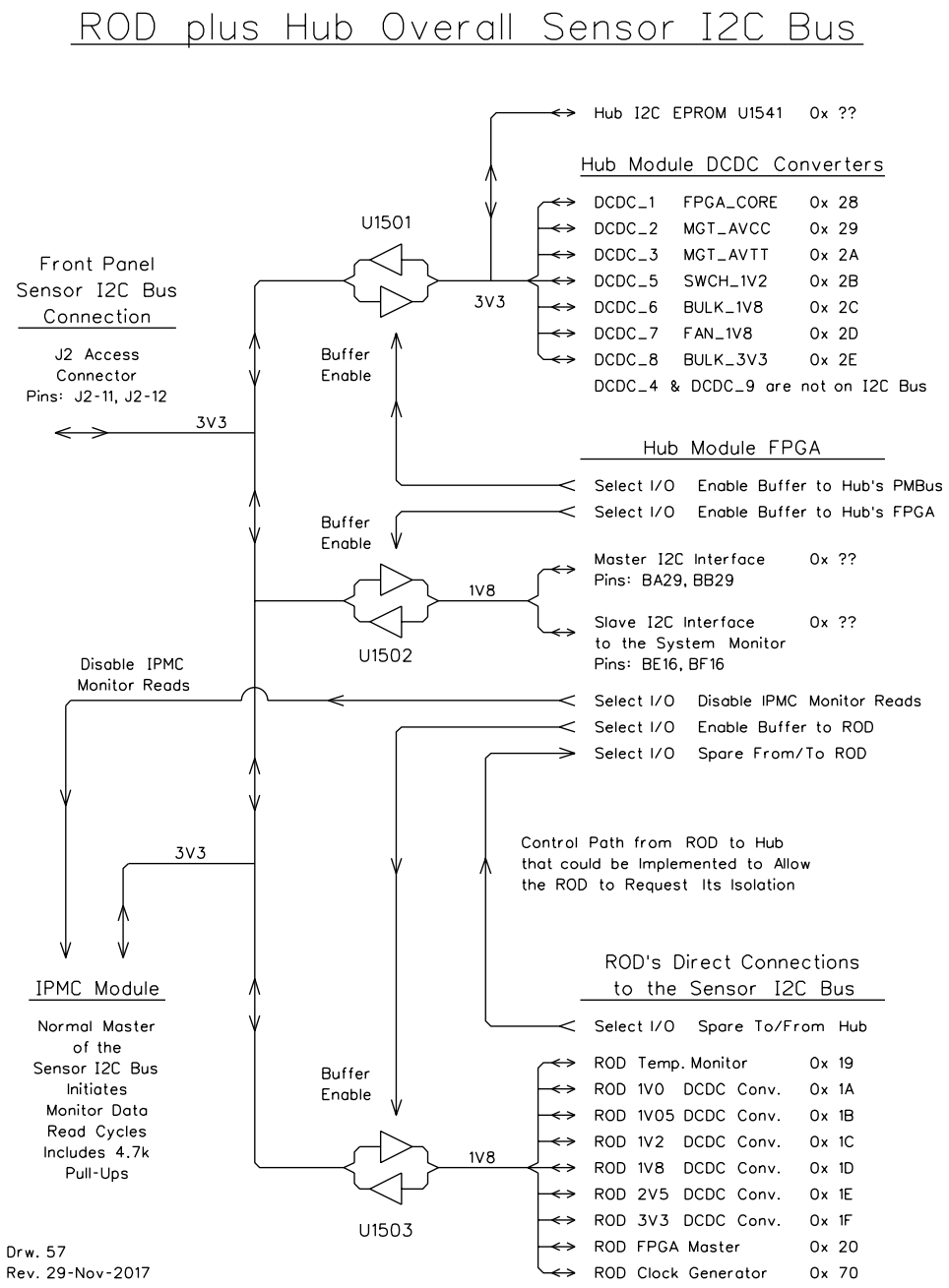

Figure 42: Joint ROD and Hub sensor I2C bus circuit diagram.

27 Appendix 14: Phys Chip Usage on the Hub Module

The Hub Module requires 2 Phys Chips for the Ethernet Base Interface connections to its UltraScale Virtex FPGA.

Two Micrel (now Microchip Technology) KSZ9031RNX Phys chips are used to implement these Ethernet connection. An advantage of this part is that it can operate with a 1.8V RGMII port and thus directly connect to the Virtex HP I/O pins. The documentation for this Micrel part looks good and its implementation looks clean.

Two drawings show the implementation of the Micrel Phys chips on the Hub Module, provided in **Figure 61** and **Figure 62**.

27.1 Power Supply, ByPass, Power Up, and Reset Requirements

In the Hub application the KSZ9031RNX Phys chip requires 3 supply buses:

- 1.2V supply for: AVDDL = the Analog Core, DVDDL = the Digital Core, AVDD_PLL = Internal PLL
- 1.8V supply for: DVDDH = the Digital I/Os, this bus can be: 1.8V, 2.5V, or 3.3V
- *3.3V supply for: AVDDH = Transceiver Analog Power*

The total load on each of these 3 power buses is expected to be the following, per chip, recall that Hub has 2 chips:

- 1.2V supply 265 mA for Cores and PLL
- 1.8V supply 65 mA for Digital I/Os
- 3.3V supply 82 mA for Transceivers

The Micrel data sheet gives a +-5% tolerance on all of this chip's supply rails.

Note that the KSZ9031RNX includes a "controller" for an external MOSFET pass transistor so that by itself it can generate the 1.2V bus from the 3.3V bus if the application requires that function. The Hub Module provide all 3 buses from external supplies.

Total Power Consumption with 1.8 V digital IO and 3.3 V Transceiver supply and 100% utilization at 1000 Base-T is expected to be about 706 mW per chip.

ByPass and Filter Components recommended for the KSZ9031RNX:

- AVDDL Bus: Next to pins 4, 9 bypass with 100 nFd on each pin. Also include one or two 10 uFd and a 1 uFd on the AVDDL bus.
- DVDDL Bus: Next to pins 14, 18, 23, 26, 30, 39 bypass with 100 nFd on each pin. Also include a 10 uFd and use a Ferrite Bead to isolate the DVDDL bus.
- AVDDL_PPL Bus: Next to pin 44 bypass with 100 nFd. Also include a 10 uFd and use a Ferrite Bead to isolate the AVDDL_PLL bus.

- DVDDH Bus: Pins 16, 34, 40
- AVDDH Bus: Pins 1, 12
- Ground: Pins 29 and the exposed thermal pad pin 49
- All capacitors are X5R or X7R ceramic.
- All ferrite beads are <0.1 Ohm DC and >60 Ohm at 100 MHz e.g. TDK MPZ1005S600C

This list of Bypass and Filter requirements for the KSZ9031RNX about matches the schematic of the Micrel Eval Brd for this chip.

The Mircel Eval Brd uses chokes (ferrite beads) on all 5 supply rails to the chip. They use: Steward HI1206N101R-00 on all rails. These are: 100 Ohm at 100 MHz, 144 Ohm at 500 MHz and 150 Ohm at 1 Ghz with 35 mOhm of DC resistance and 3 Amp max.

Because of space limitation on the Hub module I think that we can use the smaller Wurth 782633601 0603 size chokes on 4 of these 5 power rails. The Wurth 782633601 has better AC filtering characteristic, a 1 Amp max, but has 200 mOhm max DC resistance. This should be OK for the: AVDDL, AVDDL_PLL, DVDDH, and AVDDH rails.

None of these supplies can be over 100 mA and thus the maximum drop with the Wurth 782633601 choke is about 20 mV or about 1.6% on the lowest 1.2 Volt rails. I expect the current draws to be less than 100 mA, and it's possible to measure them on a running card and replace these parts if necessary so I think that this is OK.

I believe that most of the current for this chip is on its DVDDL rail, probably about 225 mA so for that I will use the lower DC resistance (60 mOhm) Wurth 742792116.

See pages 40 and 65 in the ver 2.2 datasheet for this chip for details about the expected current requirements.

Power Up Sequence:

- Basically the KSZ9031RNX wants its Cores to power up last.
- Recommended power up sequence is to have the transceiver AVDDH and the digital I/O DVDDH voltages power up before the 1.2V buses to DVDDL, AVDDL, AVDDL_PLL.
- There is no required sequence between the transceiver AVDDH and the digital I/O DVDDH.
- The power up waveforms need to be monotonic for all power buses to the KSZ9031RNX.
- After de-assertion of the RESET wait 100 usec before starting to use the part.
- At power down it is best to remove the 1.2 V supply first.
- For a power down cycle all buses must be less than 0.4V for at least 150 msec.
- All power buses must be stable for at least 10 msec before de-assertion of the Reset signal.
- All supply voltages must have a minimum of 200 usec ramp up time and have monotonic ramp.
- The recommended Reset circuit, on page 75 of the data sheet is a combination of the typical R, C, Diode to guarantee a Reset at power up and another Diode to mix in an External Reset from a CPU or FPGA.

27.2 RGMII Interface Port

The RGMII port on the KSZ9031RNX is its data connection with the Hub's UltraScale Virtex FPGA. The KSZ9031RNX RGMII connects to HP I/O pins on the FPGA.

The RGMII bus consists of 12 signals:

- Transmit Clock to the KSZ9031RNX
- Transmit Control (enable) to the KSZ9031RNX
- Transmit Data 0:3 to the KSZ9031RNX
- Receive Clock from the KSZ9031RNX
- Receive Control (enable) from the KSZ9031RNX
- Receive Data 0:3 from the KSZ9031RNX

27.3 MDC/MIIM/MDIO Interface Port

The KSZ9031RNX includes a MII Management port. This type of port is also called MDIO Management Data Input/Output. This port allows higher level devices to monitor and control the KSZ9031RNX. This port allows direct access to the IEEE defined MIIM registers, and the vendor specific registers. This port also allows indirect access to the MMD address space and registers.

This port consists of signals:

- MDC the clock
- MDIO the data line

The MAC in the FPGA provides the connections to this device management port.

27.4 Jumpers for the KSZ9031RNX (aka Strapping Pins)

The KSZ9031RNX uses a number of jumpers that are "read" during its power up process and then the state of these jumpers control its operation of the chip once power up is completed.

Most of these jumpers are the new standard type of jumper, i.e. a weak pull-up or weak pull-down on a dual purpose I/O pin. Once the jumper is "read" and the KSZ9031RNX completes its power up then the pin begins its normal function and the weak pull resistor is ignored.

For this chip the pull-up resistors connect to the DVDDH 1V8 rail.

Pin #	Strap Pin Name	Normal Function	Jumper Function - Strapping Option
17	PHYAD0	LED1	Pull-Up = 1 Pull-Down = 0 PHY Address Bits 3 and 4 are always 0, 0. This is the PHYAD of the Management Interface port on the KSZ9031RNX.
15	PHYAD1	LED2	
35	PHYAD2	RX_CLK	
32	MODE0	RXD0	Set operating Mode at Power Up

31	MODE1	RXD1	0100 NAND tree mode
28	MODE2	RXD2	1100 RGMII 1000 Base-T full duplex
27	MODE3	RXD3	1101 RGMII 1000 Base-T full or half duplex
			1110 RGMII 10/100/100 all but 1000 half duplex
			1111 RGMII 10/100/1000 full or half duplex
33	CLK125_EN	RX_DV	Pull-Up --> Enable the 125 MHz Clk Output
			Pull-Down --> Disable the 125 MHz Clk Output
41	LED_MODE	CLK125_NDO	Pull-Up --> Single LED Mode
			Pull-Down --> 3 color or dual LED Mode

KSZ9031RNX Jumpers implemented on the Hub Module:

- Pins 15, 17, 35 PHYAD Pull-Up and Pull-Down R1901:R1906
- Pins 27, 28 MODE Pull-Up Only R1907,R1908
- Pins 31, 32 MODE Pull-Up and Pull-Down R1909:R1912
- Pin 33, CLK125_EN, Pull-Up Only --> Enable the 125 MHz Clk to the MAC
- Pin 41, LED_MODE, Pull-Up Only --> Single LED Mode R1913,R1914

Note that the Pull-Down resistors are 1k Ohm and the Pull-Up resistors are 10k Ohm. Note that some of these Pull-Up / Pull-Down resistors are on high-speed RGMII lines. They must be placed and routed with minimum parasitic effect on the high-speed signals.

KSZ9031RNX LEDs:

The Hub Module runs the KSZ9031RNX LEDs in "Single LED Mode". That is it does not use tri-color or multiple LEDs per LED pin on the chip. With a 1V8 DVDDH rail I do not think that the chip can drive the LEDs directly. Rather the standard, 74AVCH8T245 non-inverting Hub circuit for controlling LEDs with 1V8 CMOS logic signals is used for the Phys chip LEDs.

KSZ9031RNX ISET Resistor:

ISET pin #48 requires a 12.1k Ohm 1% resistor to ground to set the transmitter output level. This is resistor R1915.

KSZ9031RNX RESET Circuit:

The KSZ9031RNX Phys Chips receive a reset signal from the Hub's Board Startup Reset circuits. Currently it is not understood if we want to or should provide the Phys Chips with a reset from the Hub's FPGA that would be controlled from a bit in an IPBus visible register.

KSZ9031RNX Clocks:

The KSZ9031RNX contains an internal oscillator circuit for use with a 25 MHz crystal or it can use an external clock. Be sure to use the version 2.2 or later data sheet for this Phys chip to correctly understand its clock signal requirements.

The Hub supplies the KSZ9031RNX with a quality external 25 MHz 3V3 clock signal. This external clock is sent into "X1" pin #46. Pin "X0" pin #45 is not connected.

Internally the KSZ9031RNX manipulates this 25 MHz clock as required to sequence its various functions. One step to to multiply this up to 125 MHz.

The internally generated 125 MHz clock is made available on pin CLK125 pin #41 for use by the MAC that controls the KSZ9031RNX. This 125 MHz clock is returned to the Hub FPGA as it provides the MAC for the KSZ9031RNX Ethernet circuits.

Note that this Phys chip has internal series terminator resistors in the CLK125 line and the other high-speed output lines from it in the RGMII interface. The FPGA pins in its RGMII port should incorporate the correct type of DCI termination, e.g. series termination in its output pins.

KSZ9031RNX RGMII Link to FPGA:

Reduced Gigabit Media Independent Interface between the KSZ9031RNX Phys chip and the MAC in the Hub FPGA.

KSZ9031RNX MII / MIIM Link to the FPGA:

This is the "Management Interface" between the MAC in the Hub FPGA and the KSZ9031RNX Phys chip. This separate interface allows an external entity to monitor and control the KSZ9031RNX via way of its MDC/MDIO Monitor Data Clock and I/O pins. The address of this port on the KSZ9031RNX is set by the PHYAD strapping jumpers. This Management Interface can talk to 32 bit registers both directly addressed IEEE defined registers and indirectly to vendor defined management registers.

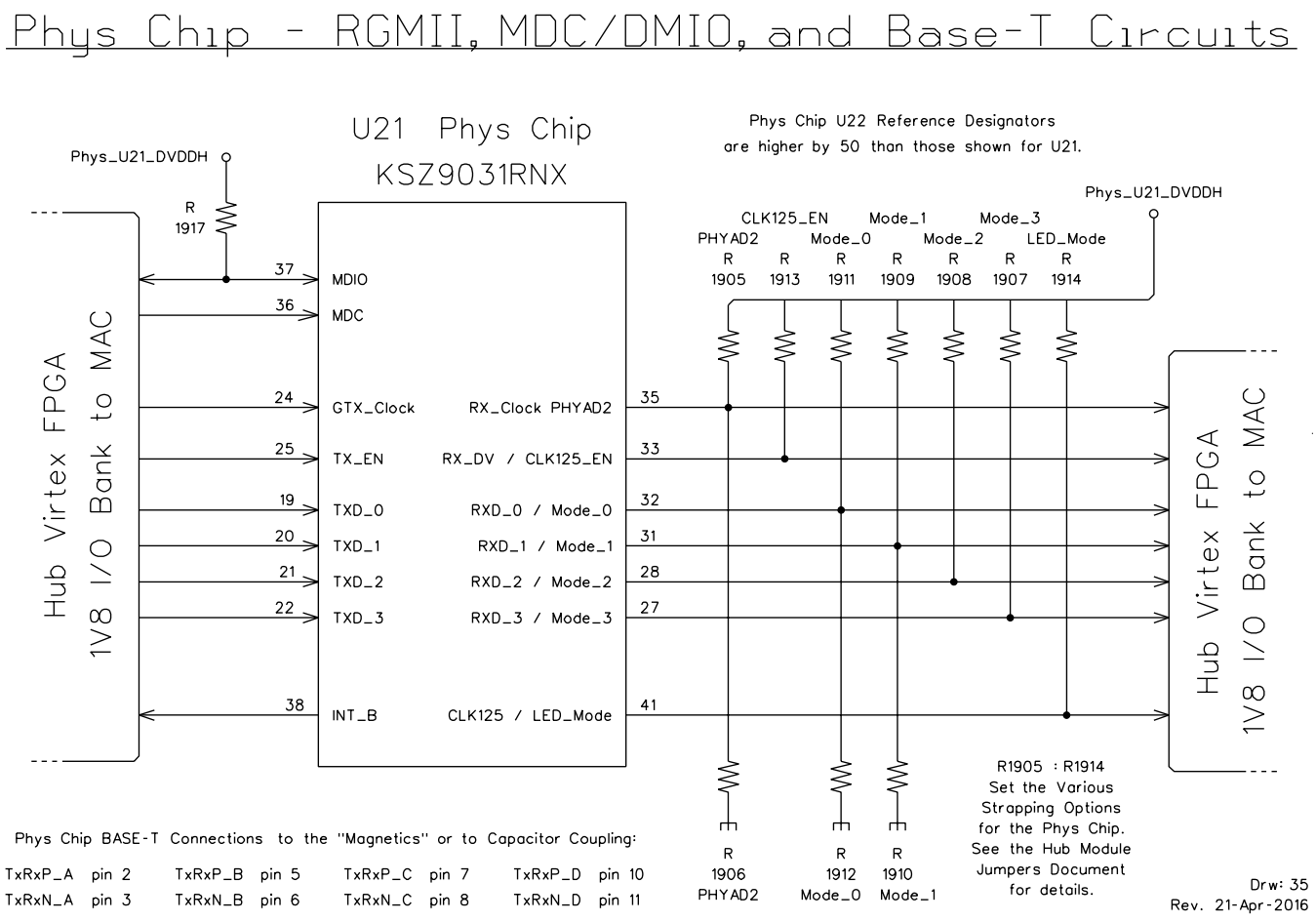

Figure 43: PHY Chip RGMII, MDC/DMIO and Base-T circuit diagrams.

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28 Appendix 15: Hub-Module Power System

The Hub-Module power system is based on the ATCA architecture. This power system supplies both the components on the Hub-Module itself and provides +12V power to the ROD mezzanine card. An overall view of the Hub Module power supplies is presented in **Figure 47**.

28.1 ATCA Power Entry and Isolated +12V Supply

Power reaches the Hub Module's zone 1 connector on redundant negative 48 Volt buses. After passing through fuses the bulk -48 Volt power from the backplane enters a SynQor "power entry module". This is either a SynQor IQ65033QMA10 10 Amp 300 Watt module or a SynQor IQ65033QGA12 12 Amp 350 Watt module. In either case these are quarter-brick size modules with the same footprint. The first prototype Hub cards are built with the SynQor IQ65033QMA10SNF-G power entry module.

From the power entry module filtered power, monitored by the IPMC, flows to the input of an Isolated +12 Volt converter. This converter makes the Isolated +12 Volt power that operates everything on the Hub Module except for the power supervision circuits and the IPMC mezzanine card. The Isolated +12 Volt power is provided by a SynQor PQ60120QEA25NNS-G 12V 25A 300 Watt quarter-brick module. Higher current modules are available if needed.

The Isolated +12 Volt power from this SynQor module is the input power to a number of non-isolated DC/DC "buck" converters that generate the actual power buses used on the Hub Module. This same Isolated +12 Volt power is provided to the ROD mezzanine card on the Hub.

The power entry module provides a separate isolated 5V0 supply that is used to operate the power supervision circuits on the Hub Module. This isolated 5V0 supply is available anytime that the Hub receives backplane 48V power.

The power entry module also provides separate isolated 3V3 power for the IPMC card. This separate 3V3 power is available anytime that the input module receives backplane 48V power.

The IPMC controls when the Isolated +12V module is allowed to operate. When the IPMC and the Shelf Manager have successfully negotiated the power up of the Hub Module then the IPMC assets the enable signal to the Isolated +12V module.

The IPMC the monitors the power entry module using its Management I2C bus which runs to both the ATCA power entry module and to the FRU & SDR EEPROM.

The power entry and Isolated +12V section of the overall Hub Module design are shown in **Figure 44** and **Figure 45**. **Figure 46** shows the various backplane ground connections that are used on the Hub Module.

28.2 Hub Module Power Bus Table

Power Bus Net Name	Bus Voltage	Principal Consumers	Anticipated Load	Supply Capacity	Supply Name
FPGA_CORE	0.950 V	FPGA INT & BRAM	20.8 Amps	40 Amps	DCDC-1
MGT_AVCC	1.000 V	FPGA MGT	10.8 Amps	20 Amps	DCDC-2
MGT_AVTT	1.200 V	FPGA MGT	10.0 Amps	20 Amps	DCDC-3
MGT_AVAUX	1.800 V	FPGA MGT	0.60 Amps	3 Amps	DCDC-4
SWCH_1V2	1.200 V	Switch & Phys	4.0 Amps	12 Amps	DCDC-5
BULK_1V8	1.800 V	FPGA & other	3.0 Amps	12 Amps	DCDC-6
FAN_1V8	1.800 V	MGT Fanout	13.0 Amps	20 Amps	DCDC-7
BULK_3V3	3.300 V	Switch & other	4.6 Amps	12 Amps	DCDC-8
BULK_2V5	2.500 V	MiniPOD & Clk FO	1.3 Amps	3 Amps	DCDC-9

Notes:

- The 40 Amp supply is a GE MDT040A0X3-SRPHZ
- The 20 Amp supplies are GE UDT020A0X3-SRZ
- The 12 Amp supplies are GE PDT012A0X3-SRZ
- The 3 Amp linear supplies are LT1764AEQ
- The low current reference supplies for the FPGA System Monitor are not included in this table.

28.3 DCDC Converters

Both GE (Lineage Power) D-Lynx series and TI (Power Trends) PTH08Txyz series converters were evaluated for use on the Hub Module. The D-Lynx converters were selected based mostly on the PMBus connection offered by their TI TPS40400 control chip. Concerns about using the D-Lynx converters remain in the areas of noise, assembly, and rework. Note that for the 2 low current supplies Linear Technology LDO linear regulators are used both to save space on the PCB and to insure a low noise supply bus. The amperage capacity of each of these DC/DC converters was sized to the load that it must drive. During this selection consideration is also given to minimizing the number of different component types used on the Hub Module.

The details of the 7 GE DCDC Converters are shown in **Figure 49 - Figure 51**. The following table and its notes summarize these designs:

Converter Name:	DCDC1	DCDC2	DCDC3
Bus NetName:	FPGA_CORE	MGT_AVCC	MGT_AVTT
Bus Voltage:	0.950 V	1.000 V	1.200 V
Max Bus Amps:	40 A	20 A	20 A
Converter Type:	MDT040A0X3	UDT020A0X3	UDT020A0X3
* Cin Local:	62 uFd	42 uFd	42 uFd
# Cout Local:	220 uFd	580 uFd	580 uFd
Cout Remote:	3822 uFd	1013 uFd	1013 uFd
R V-Set Theory:	34.29k	30.0k	20.0k
R V-Set Real :	34.00k	30.0k	20.0k
R Ramp Series:	20.0k	20.0k	20.0k
R Ramp Shunt :	34.0k	30.0k	20.0k
R Servo:	180 Ohm	180 Ohm	180 Ohm
C Servo:	10 nFd	10 nFd	10 nFd
R ADRS_0:	10k	15.4k	23.7k
R Adrs_1:	84.5k	84.5k	84.5k
I2C Adrs:	0o50	0o51	0o52
Anticipated Load in Watts:	19.8 W	10.8 W	12.0 W
@ Anticipated Input Current:	1.83 A	1.00 A	1.11 A
Design Notes:	--	External Output LC Filter	External Output LC Filter

3224

3225

Converter Name:	DCDC5	DCDC6	DCDC7	DCDC8
Bus Net Name:	SWCH_1V2	BULK_1V8	FAN_1V8	BULK_3V3
Bus Voltage:	1.200 V	1.800 V	1.800 V	3.300 V
Max Bus Amps:	12 A	12 A	20 A	12 A
Converter Type:	PDT012A0X3	PDT012A0X3	UDT020A0X3	PDT012A0X3
* Cin Local:	42 uFd	42 uFd	42 uFd	42 uFd
# Cout Local:	88 uFd	88 uFd	580 uFd	88 uFd
Cout Remote:	1530 uFd	1510 uFd	1929 uFd	1030 uFd
R V-Set Theory:	20.0k	10.0k	10.0k	4.444k
R V-Set Real :	20.0k	10.0k	10.0k	4.420k
R Ramp Series:	--	40.0k	40.0k	40.0k
R Ramp Shunt :	--	20.0k	20.0k	8.87k
R Servo:	180 Ohm	180 Ohm	- Ohm	200 Ohm
C Servo:	10 nFd	15 nFd	- nFd	10 nFd
R ADRS_0:	36.5k	54.9k	84.5k	130k
R Adrs_1:	84.5k	84.5k	84.5k	84.5k
I2C Adrs:	0o53	0o54	0o55	0o56
Anticipated Load in Watts:	4.8 W	5.4 W	23.4 W	15.2 W
@ Anticipated Input Current:	0.44 A	0.50 A	2.17 A	1.41 A
Design Notes:	Delayed Turn On & Self Ramp	--	External Output LC Filter	--

The following symbols were used in the previous table:

* --> The Cin Local capacitors are all ceramic of 3 different values and are located immediately next to the converter's input terminal.

There is an additional Bulk Cin of 2100 uFd consisting of both ceramic and Tantalum capacitors that is shared by all 7 DCDC converters. This Bulk Cin is located within a few cm of the converters and is connected to each converter by a neck of trace typically a one or two cm wide.

--> The Cout Local capacitors are all ceramic of 2 different values and are located immediately next to the converter's output terminal. Note that in the case of converters: DCDC_2, DCDC_3, and DCDC_7 (the 3 DCDC Converters that include an external LC output filter) that the Cout Local includes a 470 uFd Tantalum capacitor in addition to the multiple ceramic capacitors.

Cout Remote consists of ceramic and Tantalum capacitors of multiple values distributed around the card. In the case of the FPGA supplies these capacitors are all located near the U1 FPGA.

@ --> The anticipated Input Current in Amps for each supply assumes 90% efficiency for that converter.

Currently the total anticipated load on the Isolated +12V bus from the Hub itself is 8.46 Amps or about 101.5 Watts. About 91 Watts of this reaches components on the Hub and about 10 Watts is lost as heat in the DCDC converters.

28.4 DCDC Converter Input Filter Capacitors

There is a limit of about 12,000 uFd for the total amount of capacitance that one may have on the output of the Isolated +12V converter without upsetting its stability. Note that this 12,000 uFd is specified with the Isolated +12V supply running at capacity into a resistive load and I do not know how running it at less than full output or running it into a chopping DCDC Converter load affects its stability with the full 12,000 uFd on its output.

This 12,000 uFd must be split between the DCDC Converters on the Hub itself and the converters on the ROD mezzanine.

On the Hub Module itself, the total capacitance presented to the Isolated +12V supply is: 3118 uFd or about 26% of the assumed total available budget.

28.5 DCDC Linear Supplies

Two low current power buses on the Hub Module use linear LDO regulators. One of the linear supplies is MGT_AVAUX and the other is BULK_2V5. Both of these linear supplies are powered from the BULK_3V3 bus. Both supplies use an LC filter between the possibly noisy BULK_3V3 supply and the linear regulator's power input pin. These supplies include a trim pot with a +-5% adjustment range. These LDO regulators are enabled all of the time. Their output ramps up as the BULK_3V3 supply ramps with the regulator output typically trailing the BULK_3V3 supply by about 200 mV. These two supplies do not have PMBus monitoring and control like the 7 DCDC converters do. Details of these low current linear supplies are shown in **Figure 52**.

28.6 DCDC Converter Supervision

The IPMC supervises the Hub module power system through its control of the Isolated +12V bus. In addition the IPMC can monitor the ATCA power entry module via its Management I2C bus and it can monitor the 7 DCDC converters via its Sensor I2C bus.

The only two supplies that can not be directly monitored in this way by the IPMC are the linear regulators for the MGT_AVAUX and BULK_2V5 power buses. The voltage of these supplies can be read by the FPGA's System Monitor. The System Monitor can internally see the MGT_AVAUX supply and the BULK_2V5 is scaled and connected to an analog input to the System Monitor's ADC.

The voltage of all 9 supplies can be accurately measured with a good DVM plugged into header J3 in the NE corner of the Hub circuit board. This step is needed to calibrate the internal monitoring provided by the DCDC Converters.

A number of components on the Hub Module (FPGA, Switch chips, and Phys chips) have specific power supply sequencing requirements. These requirements are meet by ramping up together on a volt per volt bases all supplies on the Hub module except for the SWCH_1V2 supply. The SWCH_1V2 converter is not started until the other 8 supplies have ramped up and are stable.

The circuits that control the start-up of the power supplies are shown in **Figure 53, Figure 55** and **Figure 56**. The start-up process has the following steps:

- The process starts when the supervisor sees that the enable signal to the Isolated +12V supply has been asserted and that the Isolated +12V bus from this supply has reached a minimum of 8.5 Volts.
- At this point a delay of 500 msec is used to allow the Isolated +12V bus to reach its full value and to stabilise.
- Then the enable signal is sent to 6 of the DCDC converters on the Hub Module, all of the DCDC converters except for the SWCH_1V2 supply.
- At this point a delay of 120 msec is used to allow these 6 DCDC converters time to complete their internal startup routines. Note that the output of these converters does not begin to ramp during this 120 msec delay because the Ramp Sequence pins on these converters is being held low.
- After this 120 msec delay the Ramp Sequence signal to these 6 converters begins to rise. The converter outputs follow the Ramp Sequence signal on a volt per volt bases. The main supplies to the FPGA reach their full output over a 5 to 9 msec period. The BULK_3V3 supply is the last to reach its full output - taking about 3 times longer than a 1 Volt supply.
- About 100 msec after these 6 supplies have reached their full output the SWCH_1V2 converter is enabled. The ramp rate of this converter is internally controlled so that it reaches its full output in a few msec. This delayed startup of the SWCH_1V2 supply is required by the Switch chips, not just to prevent cross coupling of the power rails through the CMOS circuits but rather because the Switch does not want its core to start until its I/O has been powered up and is stable.

- The two linear regulator supplies MGT_AVAUX and BULK_2V5 receive their input power from the BULK_3V3 supply. They just ramp up about 200 mV behind the BULK_3V3 supply.
- Once all 9 supplies are up and stable, as indicated either by their Power Good signals being asserted or as measured for the two linear regulator supplies, then there is a delay of 500 msec for everything to settle down and then the Board_Startup_Reset_B signal is de-asserted. The distribution of the Board_Startup_ Reset_B signal is shown in **Figure 58**. This completes the power up of the Hub Module.

The circuits that supervise this startup process are powered by an isolated 5 Volt output on the ATCA power entry module. This 5 Volt output is active anytime that the card receives backplane 48 Volt power.

The shutdown of the Hub Module supplies is initiated when either the enable to the Isolated +12V supply is dropped (the normal shutdown situation) or when the output of the Isolated +12V supply falls below 8.5 Volts. During the shutdown sequence the SWCH_1V2 converter is immediately stopped and the other 6 converters ramp down quickly in an orderly manner for as long as their input power remains available. When the input power falls below threshold then all of the converters are immediately stopped. The shutdown sequence is shown in **Figure 54**. During shutdown the Board_Startup_ Reset_B signal is asserted as soon as the enable is removed from the Isolated +12V supply and remains asserted for as long as power is available.

28.7 DCDC Converters with an LC Output Filter

Three of the DCDC Converters on the Hub Module include an LC Output Filter to reduce the switching noise that is present in their output voltage. These 3 converters make power for the MGT Transciver circuits and these circuits specify a peak to peak noise voltage of under 10 mV on their power supply rails.

The low current MGT_AVAUX supply meets this requirement by using a linear regulator with a filter inductor before it to remove the high frequency noise. The higher current MGT_AVCC, MGT_AVTT, and FAN_1V8 supplies meet this requirement by using an LC filter after these DCDC Converters. The L for this filter is a high current low resistance 680 nH Wurth inductor. The C for the filter consists of large value tantalum capacitors and ceramic capacitors of multiple values. Most of these capacitors are located near the load point.

A potential issue with using an LC filter after these buck DCDC Converters is that their servo control loop may require special compensation for it to be stable. To provide various options for how the feedback network is setup in these 3 converters the Hub Module PCB includes a set of 4 jumpers for each of these supplies. The jumpers that are associated with each of these converters are:

DCDC-2 MGT_AVCC JMP1051, JMP1052, JMP1053, JMP1054

DCDC-3 MGT_AVTT JMP1101, JMP1102, JMP1103, JMP1104

DCDC-7 FAN_1V8 JMP1301, JMP1302, JMP1303, JMP1304

Jumpers JMP1051, JMP1052 (and JMP1101, JMP1102 and JMP1301, JMP1302) control whether the the V_SENSE_+ feedback is taken before or after the output filter inductor. JMP1051 selects before the output inductor and JMP1052 selects after the inductor.

Jumpers JMP1053, JMP1054 (and JMP1103, JMP1104 and JMP1303, JMP1304) control whether the the RC coupled feedback is taken before or after the output filter inductor. JMP1053 selects before the output inductor and JMP1054 selects after the inductor.

This jumpers information is also presented in the "as built jumpers" document. In addition to these feedback source selection jumpers, the layout for each of these 3 converters also includes the SMD pads to mount an 0805 capacitor that directly connects between the converters output and its "Trim" input pin.

28.8 Power Requirements Information for each Section of the Hub

The following are power supply requirements information about the various components on the Hub Module. This information was used to design the overall Hub Module power supply and to make the overall list of Hub Module power buses shown above. More details about the power requirements of the individual sections can be found in their "as built" documents.

Power Supply Requirements for the Hub Module UltraScale XCVU125 FPGA:

FPGA Bus	Bus Volts	Estimated Current Draw
VCCINT+VCCBRAM	0.950 V	20.8 Amps est.
VCCAUX	1.800	147 mA quiescent
VCCAUX_IO	1.800	2 mA quiescent
VCCO	1.800 / 3.300	1 mA per bank quiescent
VCCADC	1.800	few mA
VREFP	1.250	few mA
MGT_AVCC	1.000	8.8 Amps est.
MGT_AVTT	1.200	12.6 Amps est.
MGT_AVAUX	1.800	0.6 Amps est.

Note that this FPGA has power supply sequencing requirements.

See below for more details about the estimates for FPGA MGT power from the Xilinx tools.

Requirements for the Base Interface Switch Power Supplies:

A separate 12 Amp converter is used for the Switch's 1.2 Volt requirements. To meet the power supply sequencing requirements of the Switch and Phys chips, this SWCH_1V2 converter is not enabled until after the other DCDC converters on the Hub have ramped up and stable.

The total draw on the SWCH_1V2 bus from all 3 switch chips is expected to be 3.5 Amps.

The total draw on the BULK_3V3 supply from the 3 Switch chips is expected to be 1.5 Amps.

The total heat dissipation from the 3 Switch chips is expected to be 9.2 Watts.

Requirements for the GTH Fanout Power Supply:

The 74 channel FEX Data Fanout (aka GTH Fanout) has its own private power bus called FAN_1V8. The reasons to have a private converter for this Gb/s speed fanout include the requirement for low noise and the possible need to adjust this supply independent of other loads.

The expected load on the FAN_1V8 supply is 13.0 Amps which results in about 23.4 Watts of heat from the 74 fanout chips.

Requirements for the Micrel KSZ9031RNX Phys Chip Power Supplies:

In the Hub application the KSZ9031RNX requires 3 supply buses:

- 1.2V supply for: AVDDL, the Analog Core, DVDDL the Digital Core, AVDD_PLL Internal PLL
- 1.8V supply for: DVDDH, the Digital I/Os
- 3.3V supply for: AVDDH, Transceiver Analog Power

The total load on each of these power buses from the 2 Phys Chips on the Hub Module is expected to be:

- 1.2V supply 530 mA from SWCH_1V2 delayed turn on
- 1.8V supply 130 mA from BULK_1V8
- 3.3V supply 164 mA from BULK_3V3

Total Power Consumption with 1.8 V digital IO and 3.3 V Transceiver supply and 100% utilization at 1000 Base-T is expected to be about 1.5 Watts for both Phys chips.

Requirements for the Clock Generation and Fanout Power Supplies:

The 25 MHz Ethernet Clock generator and its fanout are expected to use 55 mA from the BULK_3V3 supply.

The 40.08 MHz and 320.64 MHz Clock generators and their fanouts are expected to use 160 mA from the BULK_3V3 supply and 381 mA from the BULK_2V5 supply.

6. All supplies to these clock generators and fanouts are filtered and distributed to the clock components on a separate isolated PCB area fills. A total of about 2.0 Watts is needed for Clock generation and distribution.

Requirements for the MiniPOD Power Supplies:

The MiniPODs each require: 2.5 V and 3.3 V power.

The Transmitter MiniPOD requires: from the 2V5 bus 280 mA typical 365 mA maximum, from the 3V3 bus 105 mA typical 185 mA maximum. This is a heat load of 1.2 Watts typ 1.6 Watts max.

The Receiver MiniPOD requires: from the 2V5 bus 350 mA typical 525 mA maximum, from the 3V3 bus 48 mA typical 90 mA maximum. This is a heat load of 1.1 Watts typ 1.6 Watts max.

The total maximum requirements for both MiniPODs are:

Bulk_2V5 bus 890 mA
Bulk_3V3 bus 275 mA
Heat Load 3.1 Watts

Power to both MiniPODs is filtered and distributed on separate isolated PCB area fills.

28.9 Final best Estimate on FPGA MGT Power from Xilinx Tools

Requirements for the MGT AVCC and AVTT Power Supplies

Ultrascale GTH and GTY channels each draw currents from:

1.0 V AVCC power
1.2 V AVTT power

The Xilinx Power Estimator spreadsheet (XPE) was used to evaluate the expected power usage for AVCC and AVTT. The current draw on these supplies depends highly on the line rate and very little on the user data payload. This is quite different from estimating current usage in the main logic area where user data content and most importantly the toggling ratio is the driving factor. For MGT channels the toggling ratio for the highest rate circuitry has to be 50%. XPE thus has all the information it should need to produce an accurate estimate for MGT AVCC and AVTT.

The goal was to determine a maximum expected power usage.

This requires knowing the maximum line rate considered.

The asumptions were

- 9.6 Gbps maximum line rate for backplane and all readout channels
- 4.8 Gbps maximum line rate for MiniPOD channels, i.e. all TTC, combined data and FELIX channels
- DFE used for all receiver channels (as it uses more power)
- 1.0 V differential swing on Hub FPGA readout output channels
- 0.5 V differential swing on MiniPOD output channels

The MGT channel assignment from 18-Apr-2016 provided the list of GTH and GTY channels the Hub uses only as transmitters and as full transceivers, grouped by usage and by corresponding expected line rates. This list was used to configure the XPE GTH and GTY tabs.

4.8, 6.4 and 9.6 Gbps are backplane speeds still plausible at this time for l1calo. XPE indicates that some current draws are higher at 6.4 than 9.6 Gbps, for GTY AVTT in particular. Two sets of XPE estimates were thus needed, for backplane line rates of 6.4 and 9.6 Gbps. The maximum values are summarized below.

The maximum currents from these XPE estimates are:

MGT AVCC drawing 8.8 Amps
MGT AVTT drawing 12.6 Amps

Note: The “EyeScan” feature was NOT enabled in the XPE estimation.

Adding this option to all channels increases AVCC only, by ~2 A.

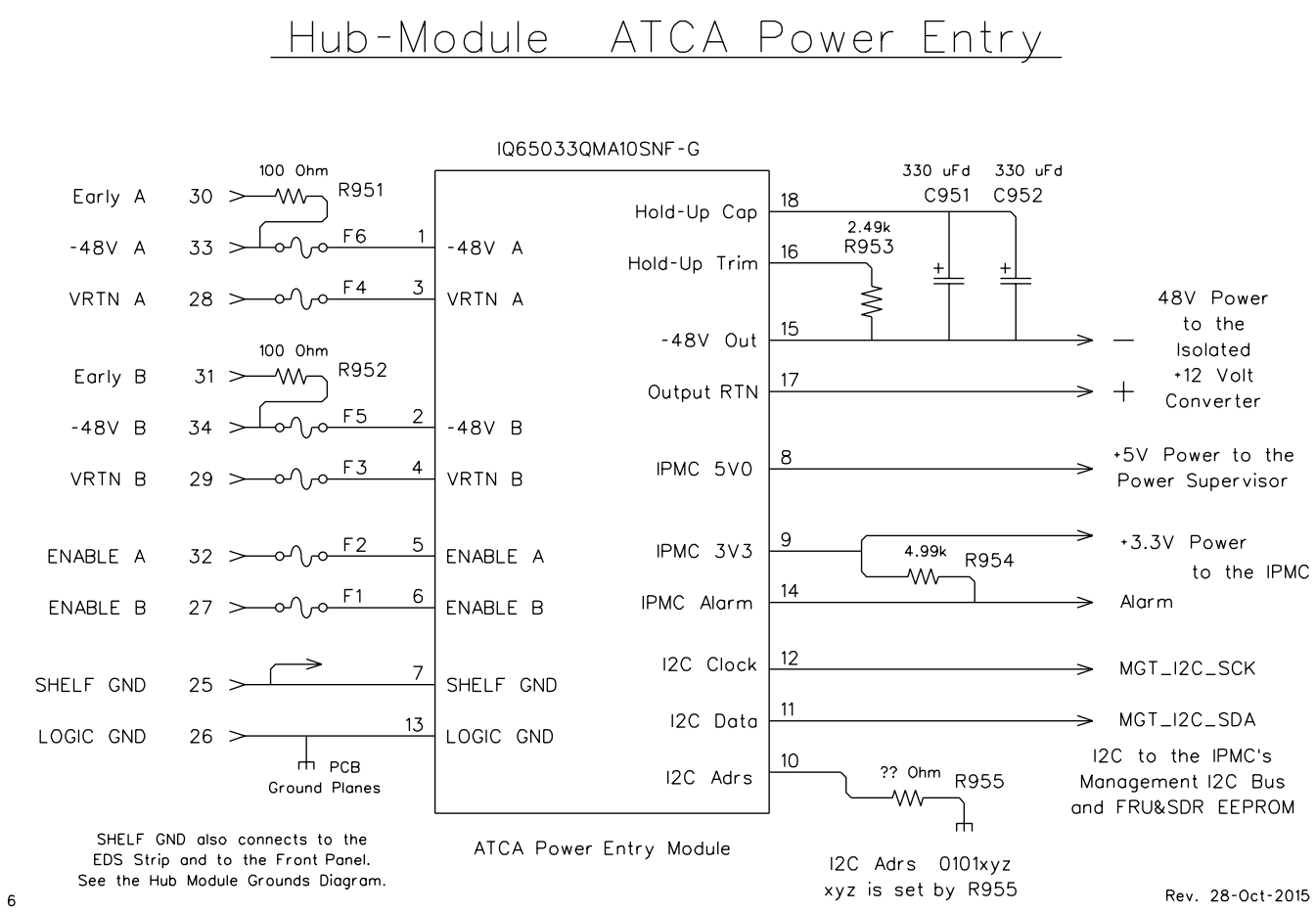

Figure 44: Circuit diagram for Hub power entry.

3479

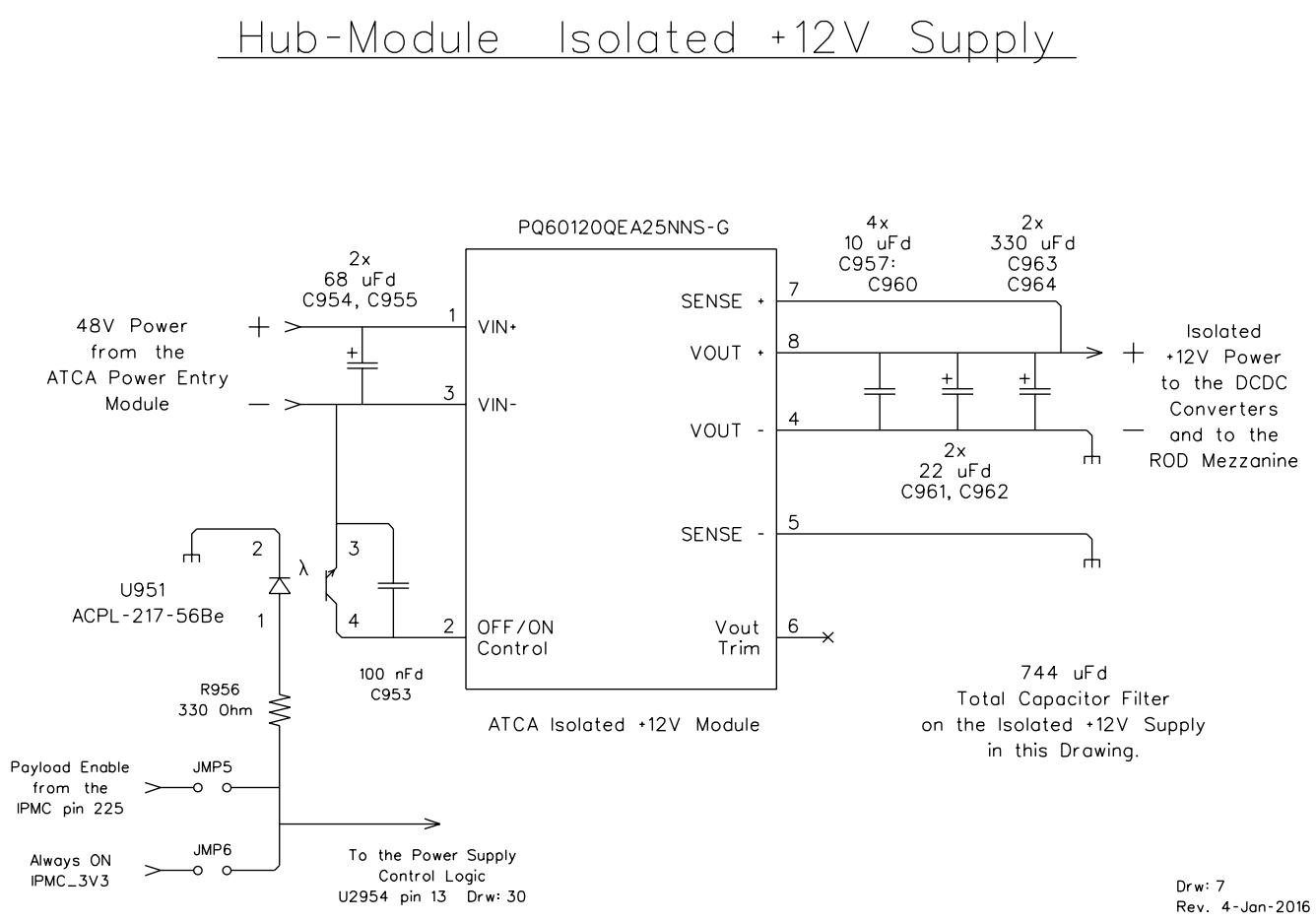

Figure 45: Circuit diagram for Hub +12V supply.

3480

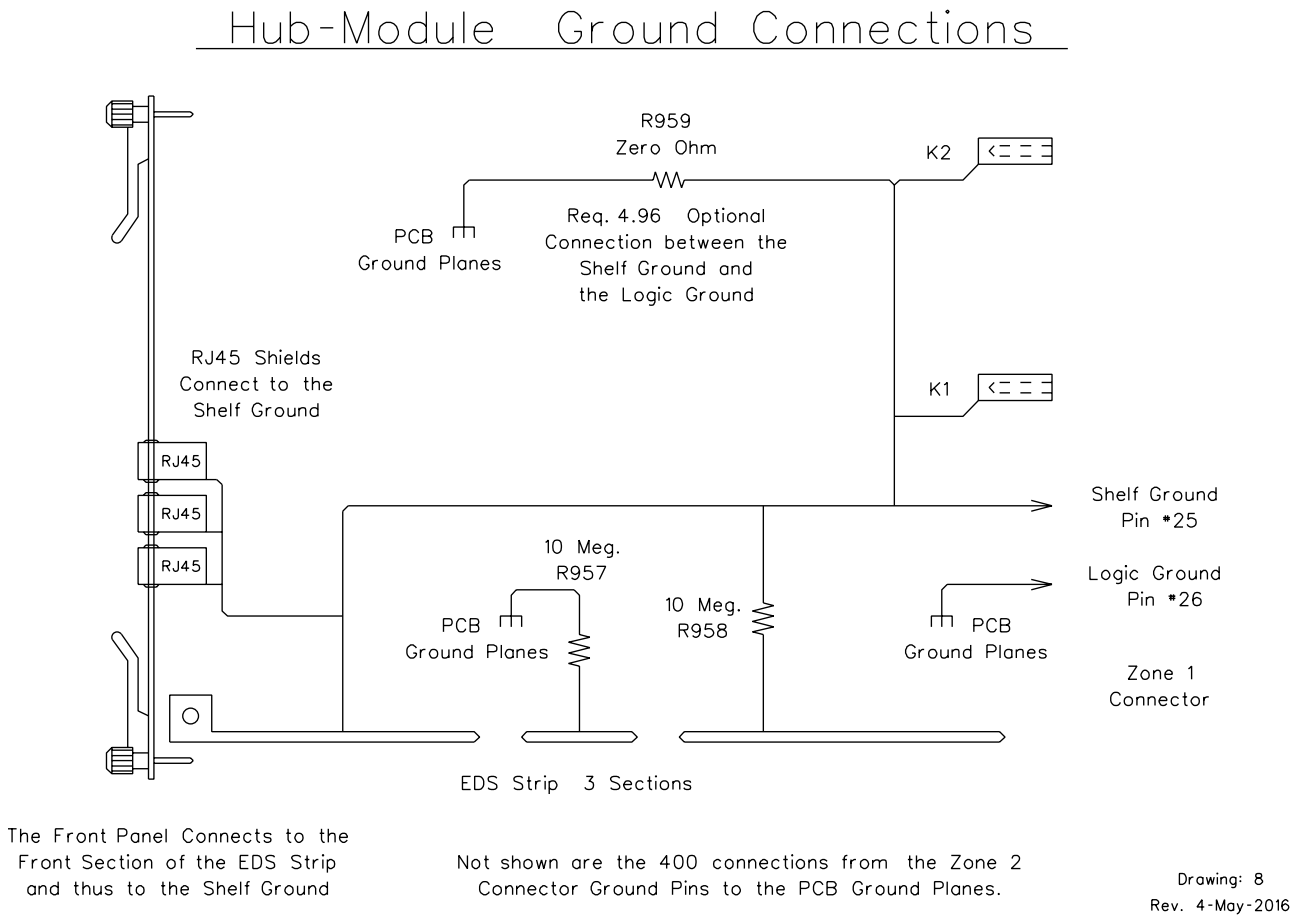

Figure 46: Circuit diagram for Hub ground connections.

3481

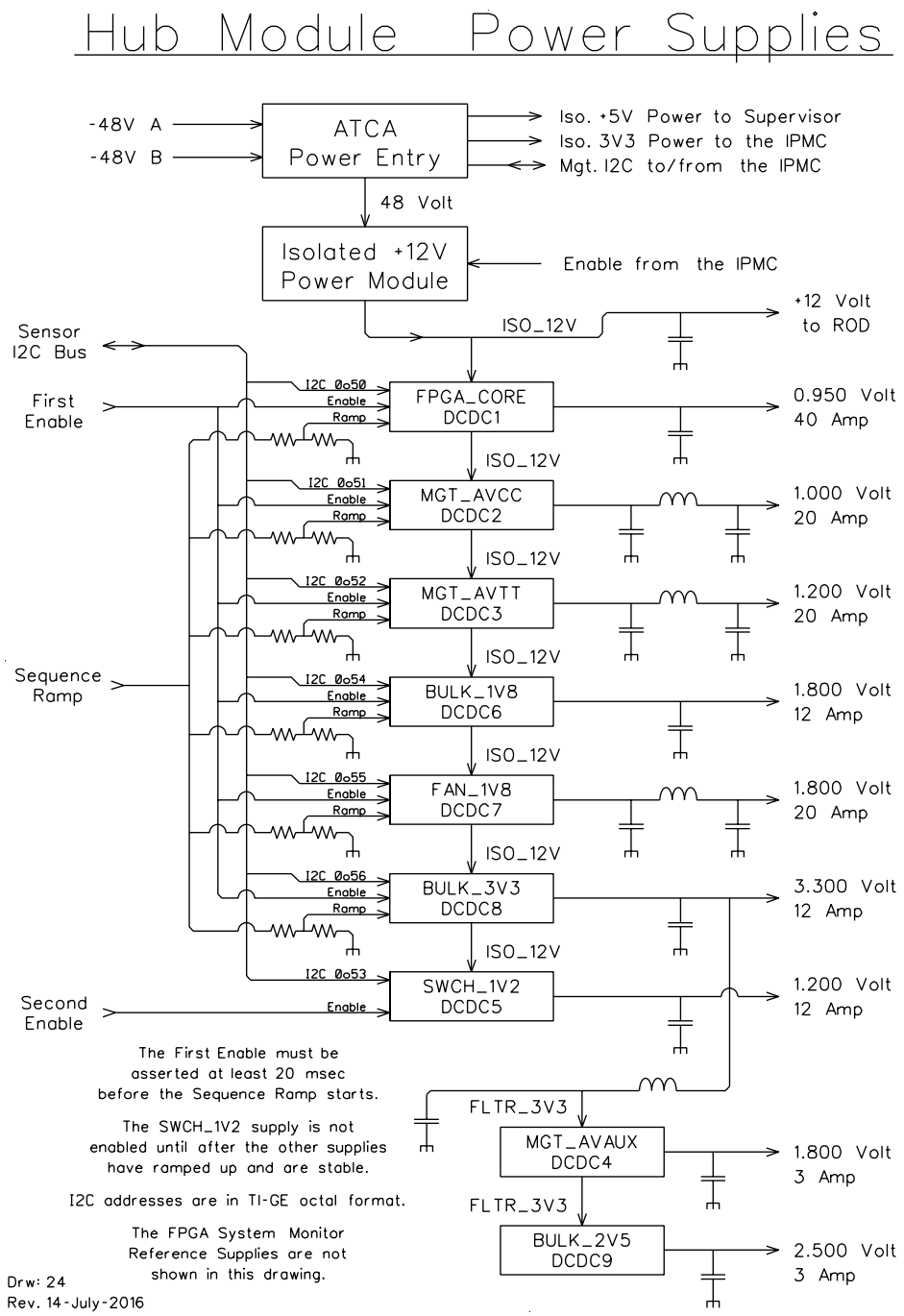

Figure 47: Circuit diagram for Hub power supplies.

3482

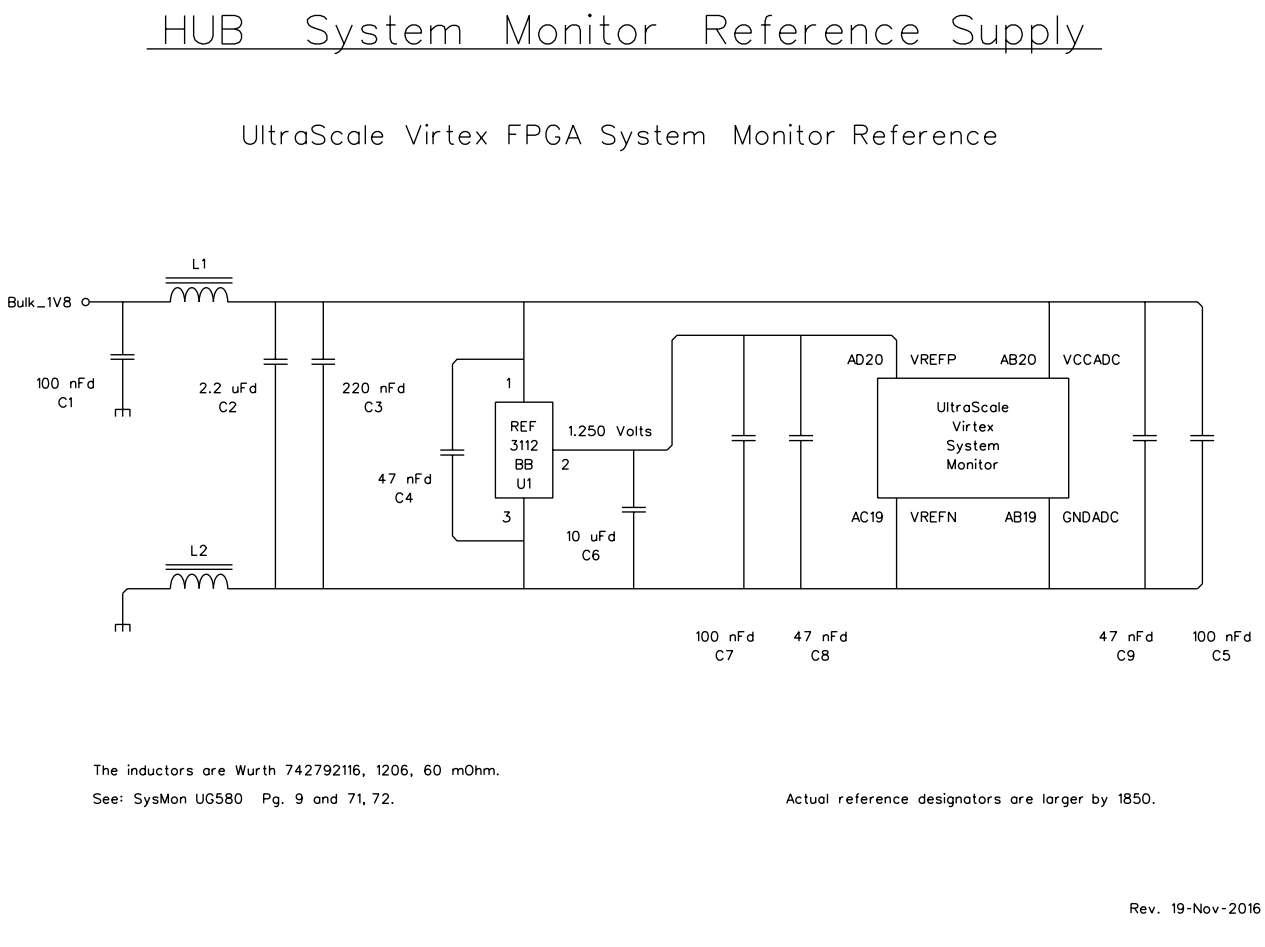

Figure 48: Circuit diagram for the Hub monitor reference supply.

3483

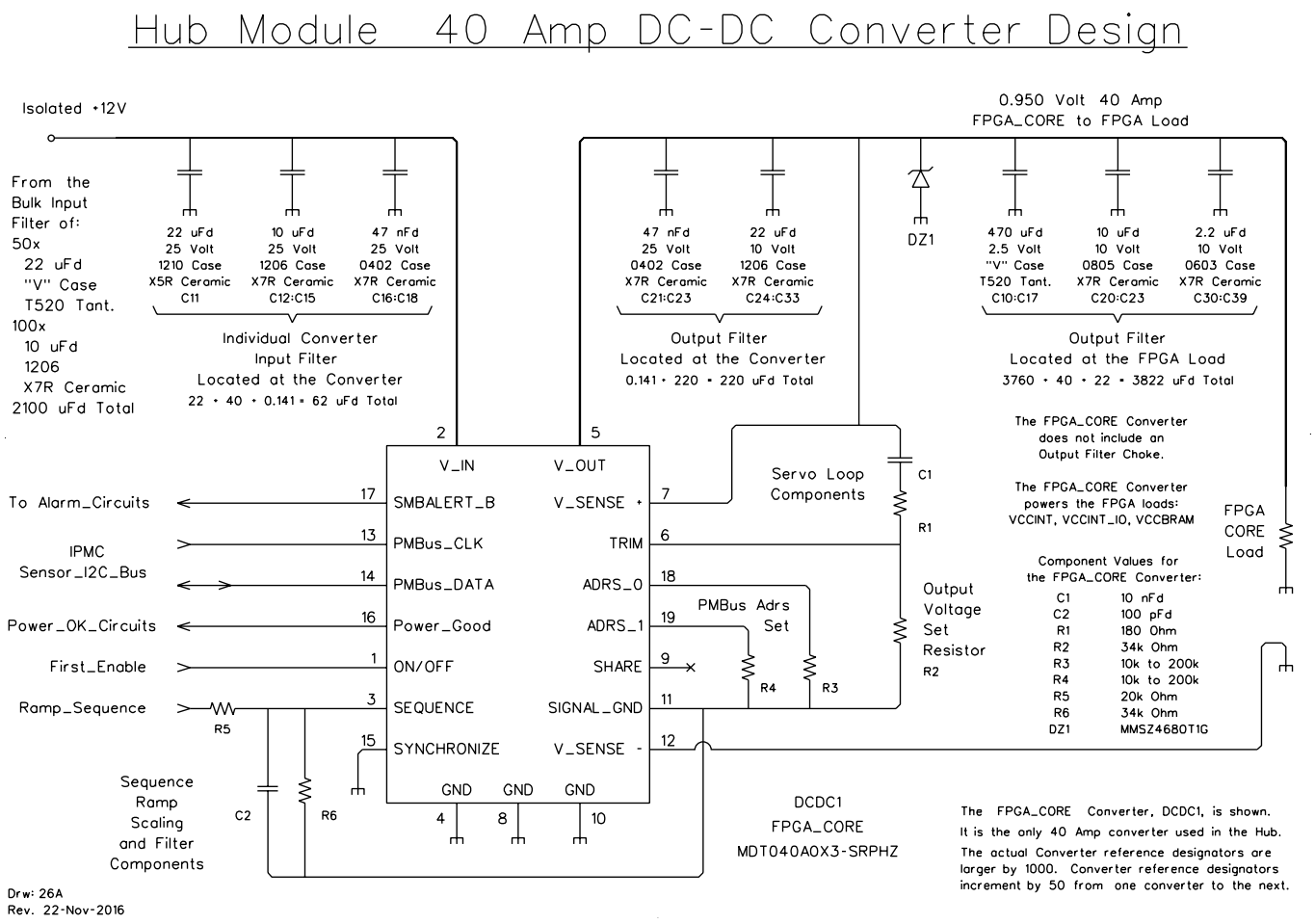

Figure 49: Circuit diagram for Hub 40A DCDC converter

3484

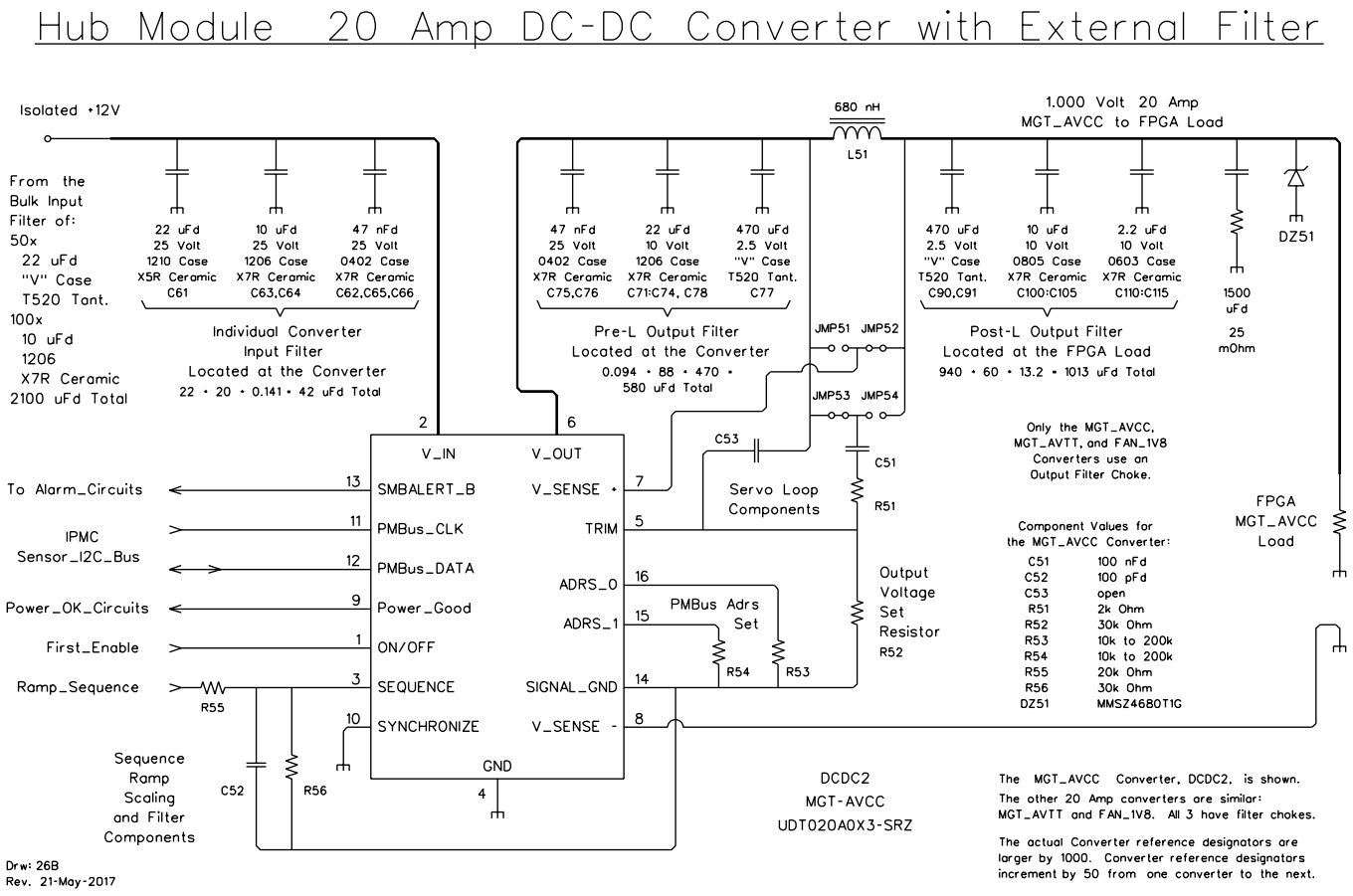

Figure 50: Circuit diagram for Hub 20A DCDC converter

3485

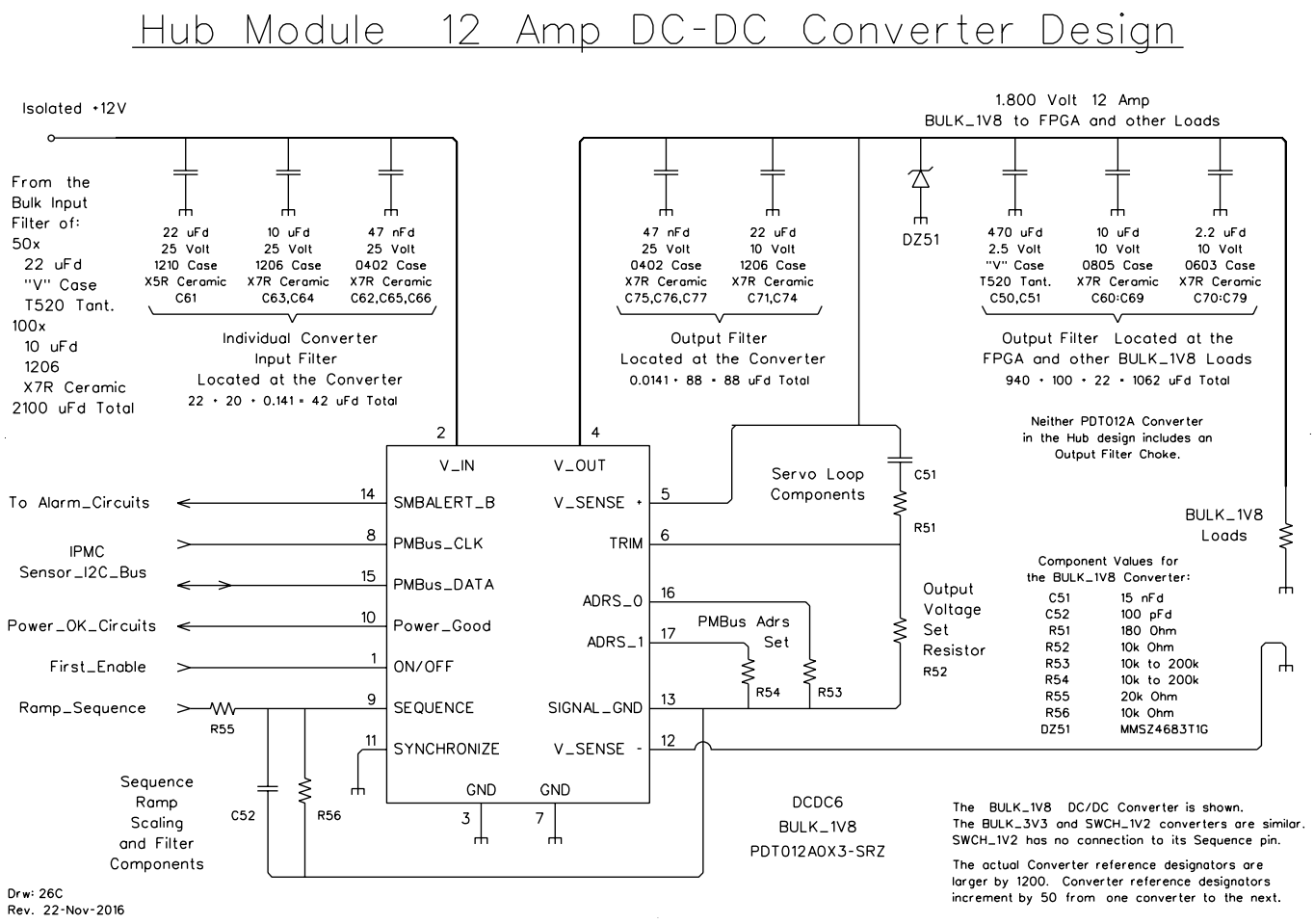

Figure 51: Circuit diagram for Hub 12A DCDC converter.

3486

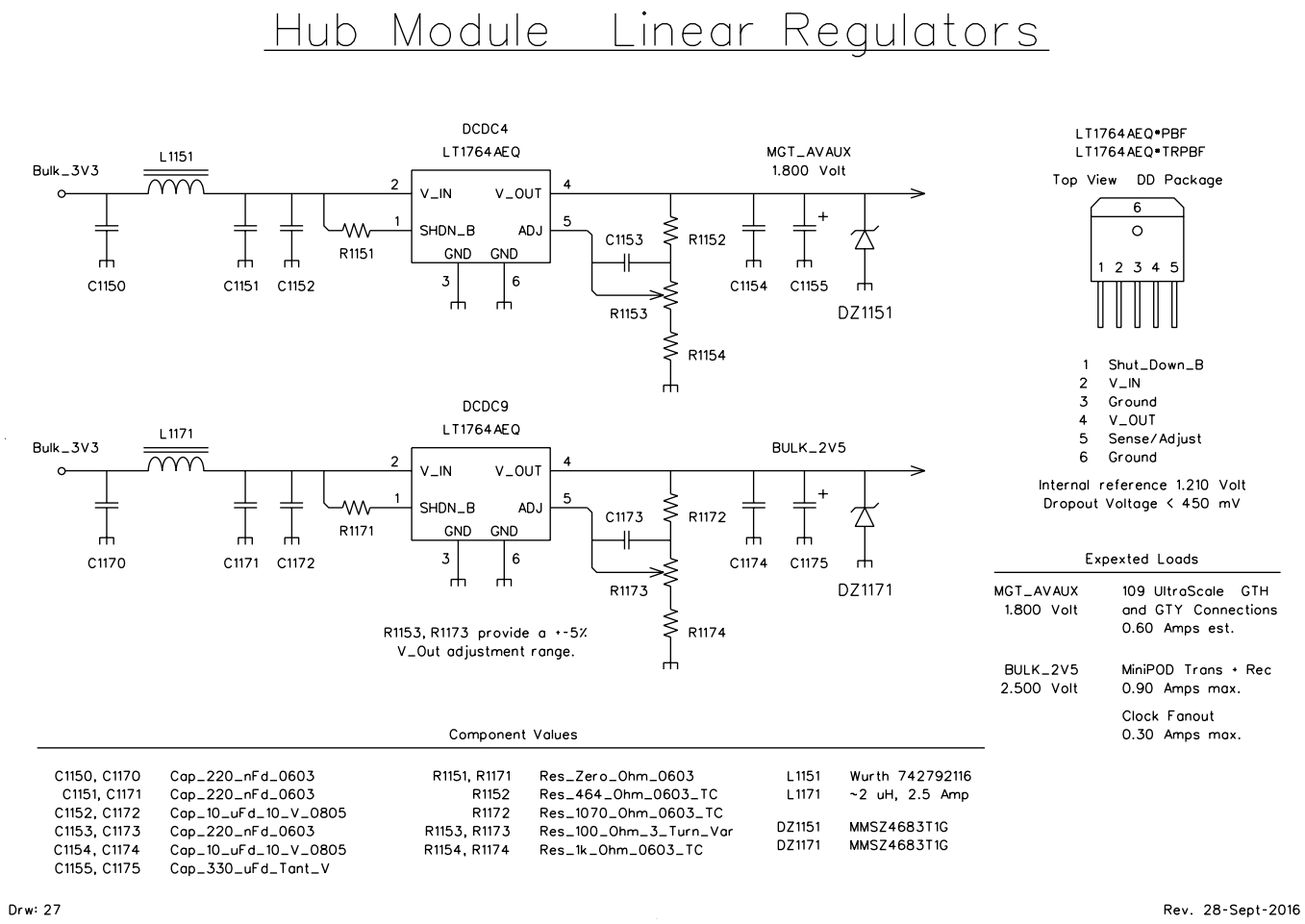

Figure 52: Circuit diagram for Hub linear regulartors.

3487

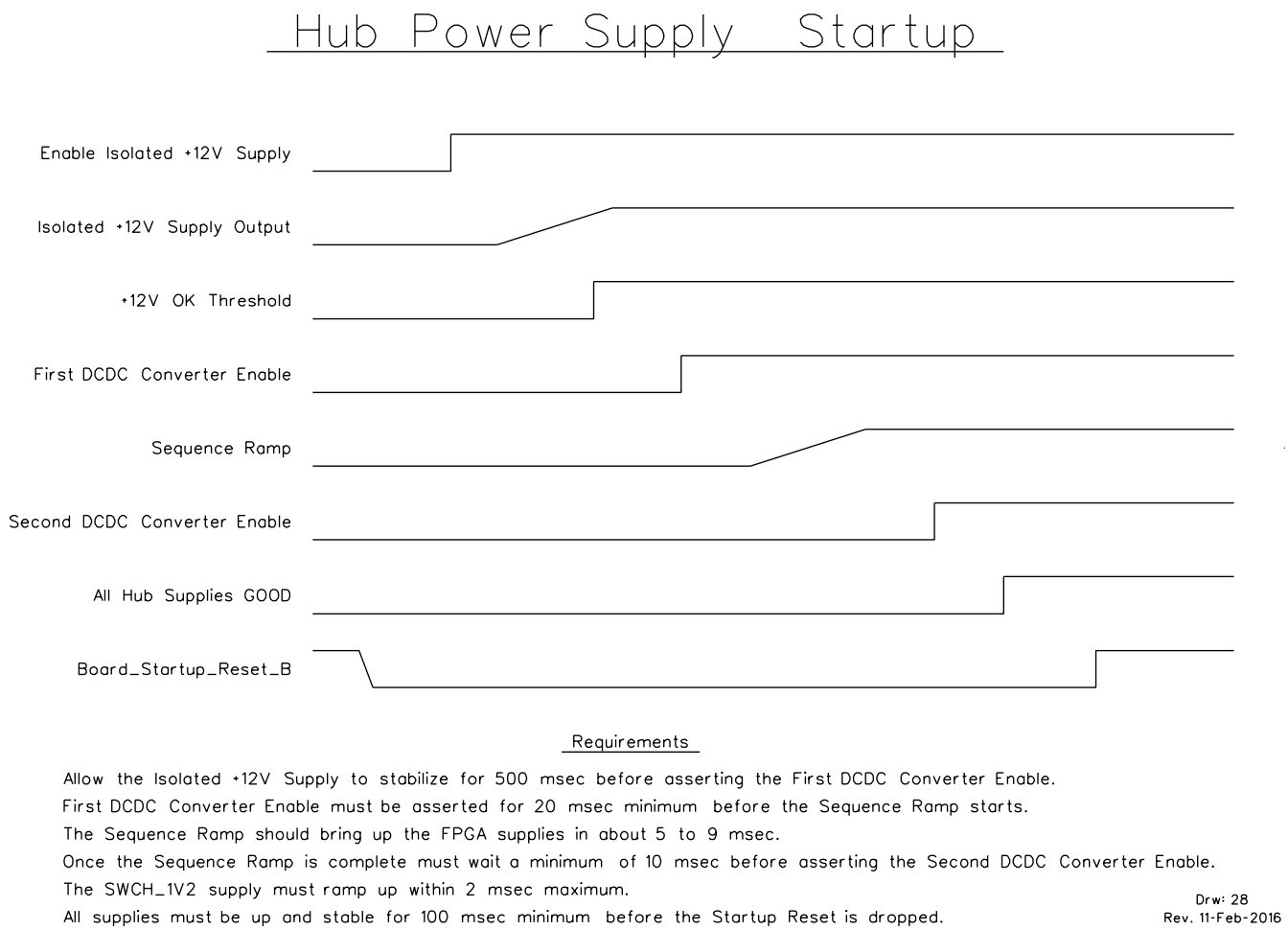

Figure 53: Hub power supply startup timing diagram.

3488

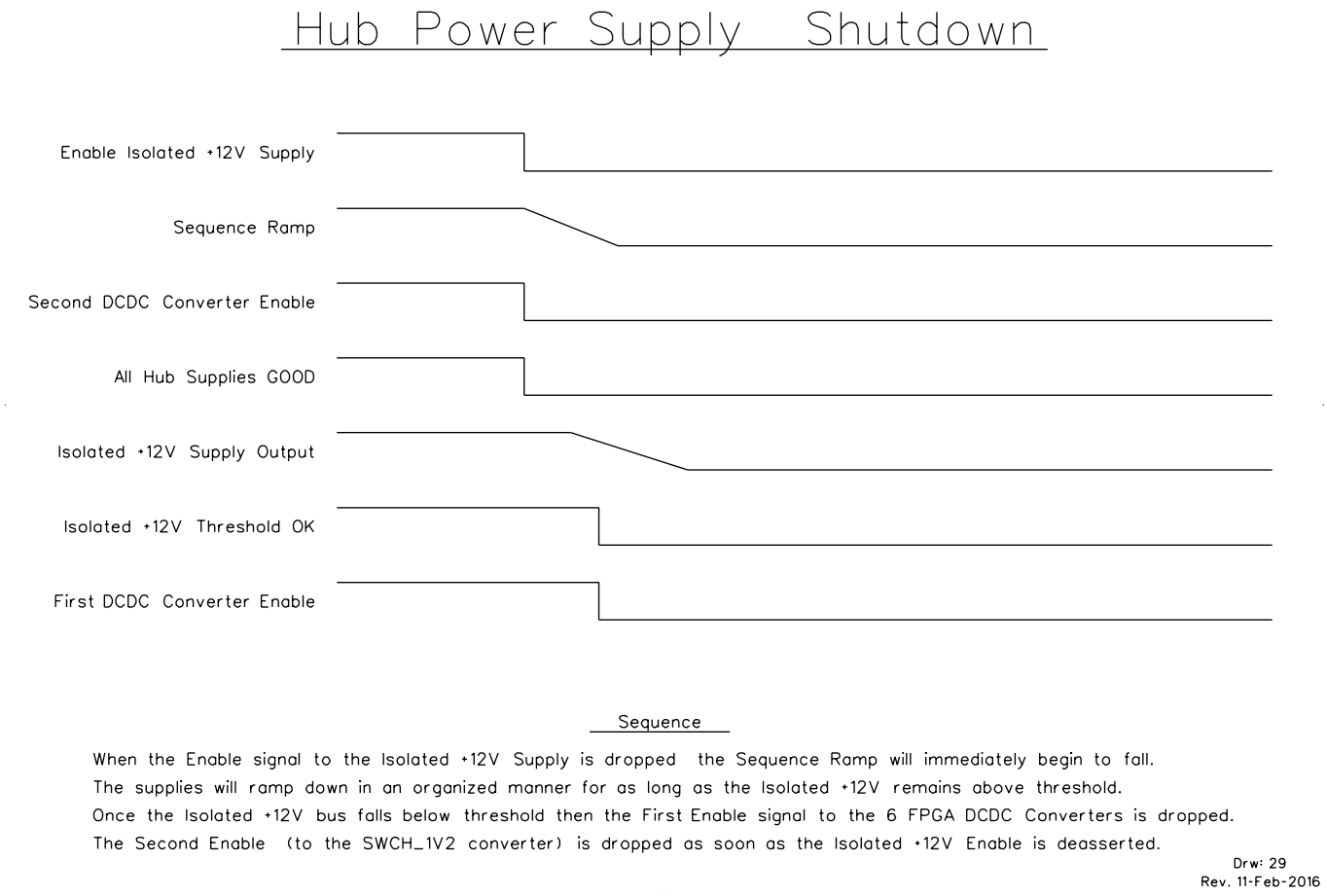

Figure 54: Hub power supply shutdown timing diagram.

3489

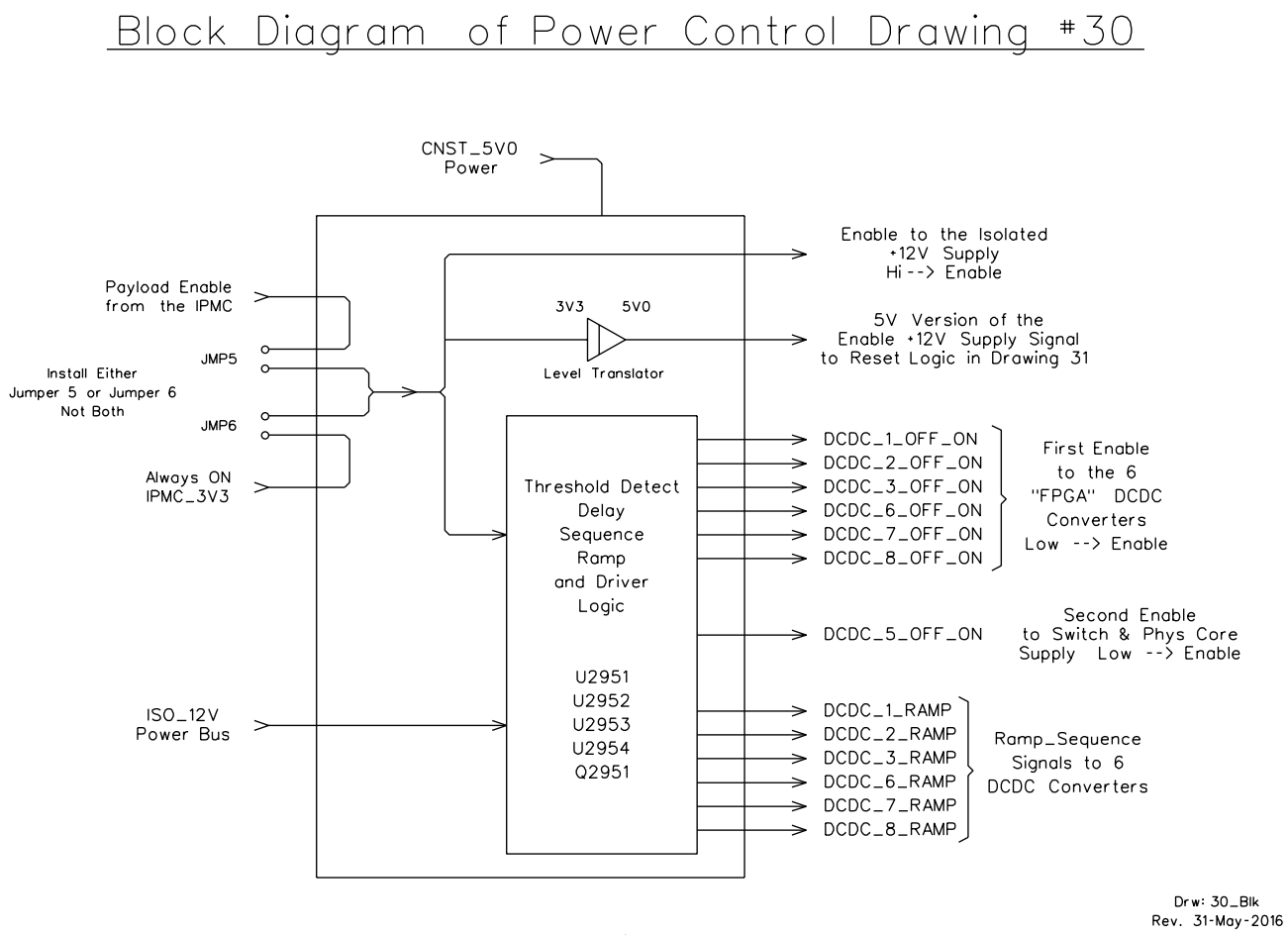

Figure 55: Block diagram of Hub power control (1/2)

3490

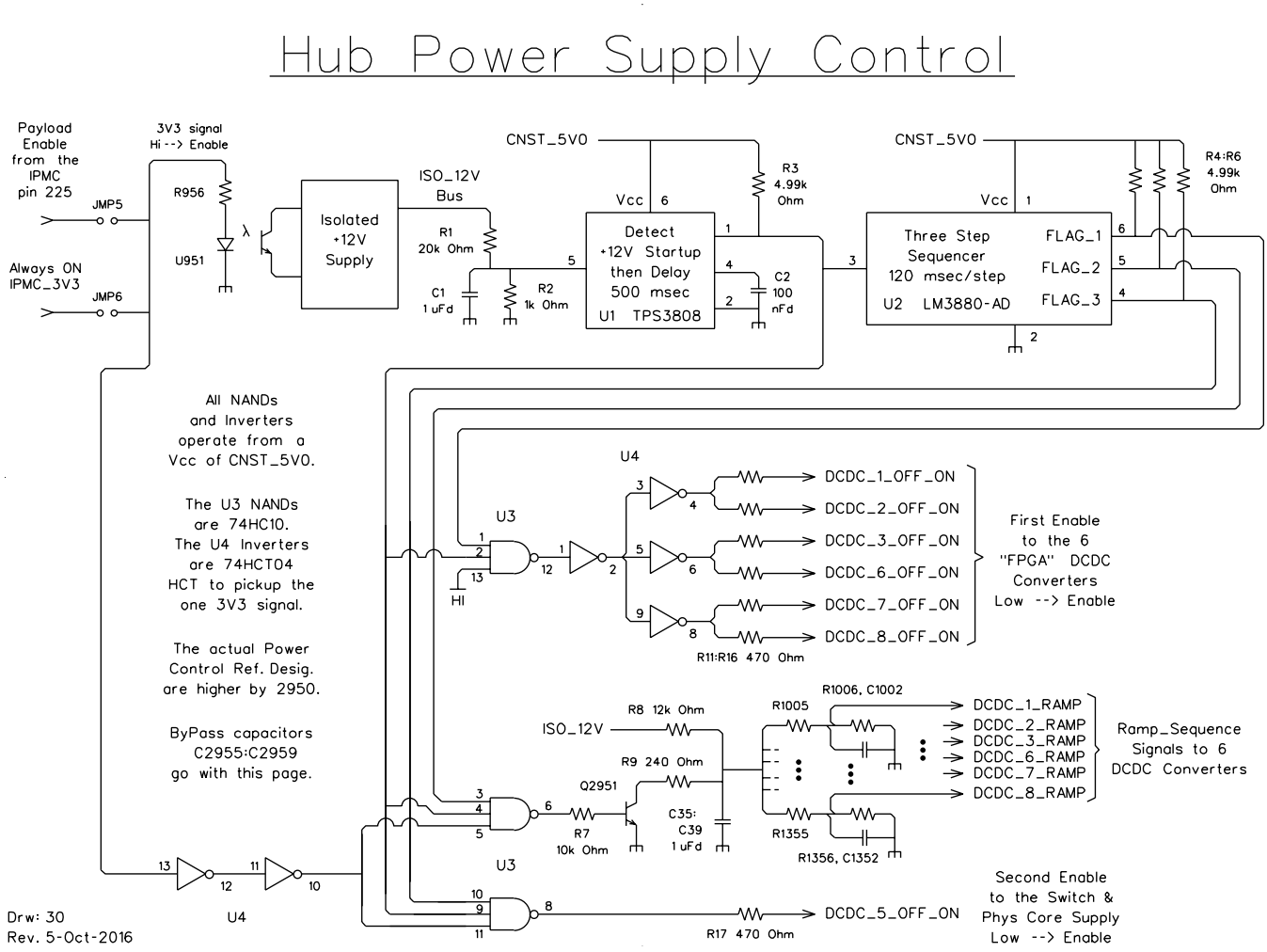

Figure 56: Circuit diagram of Hub power supply control (2/2).

3491

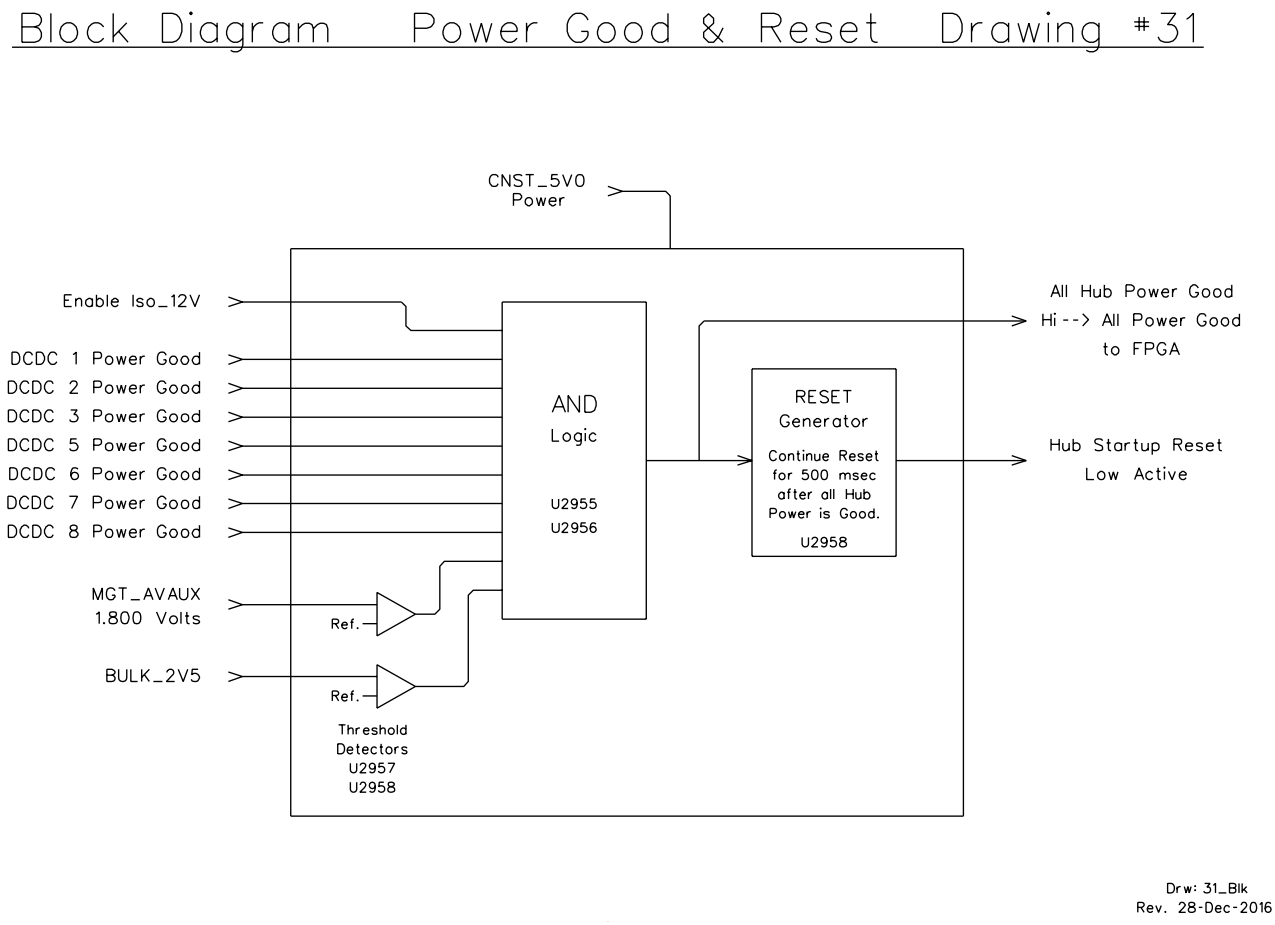

Figure 57: Block diagram of Hub power ready/reset (1/2).

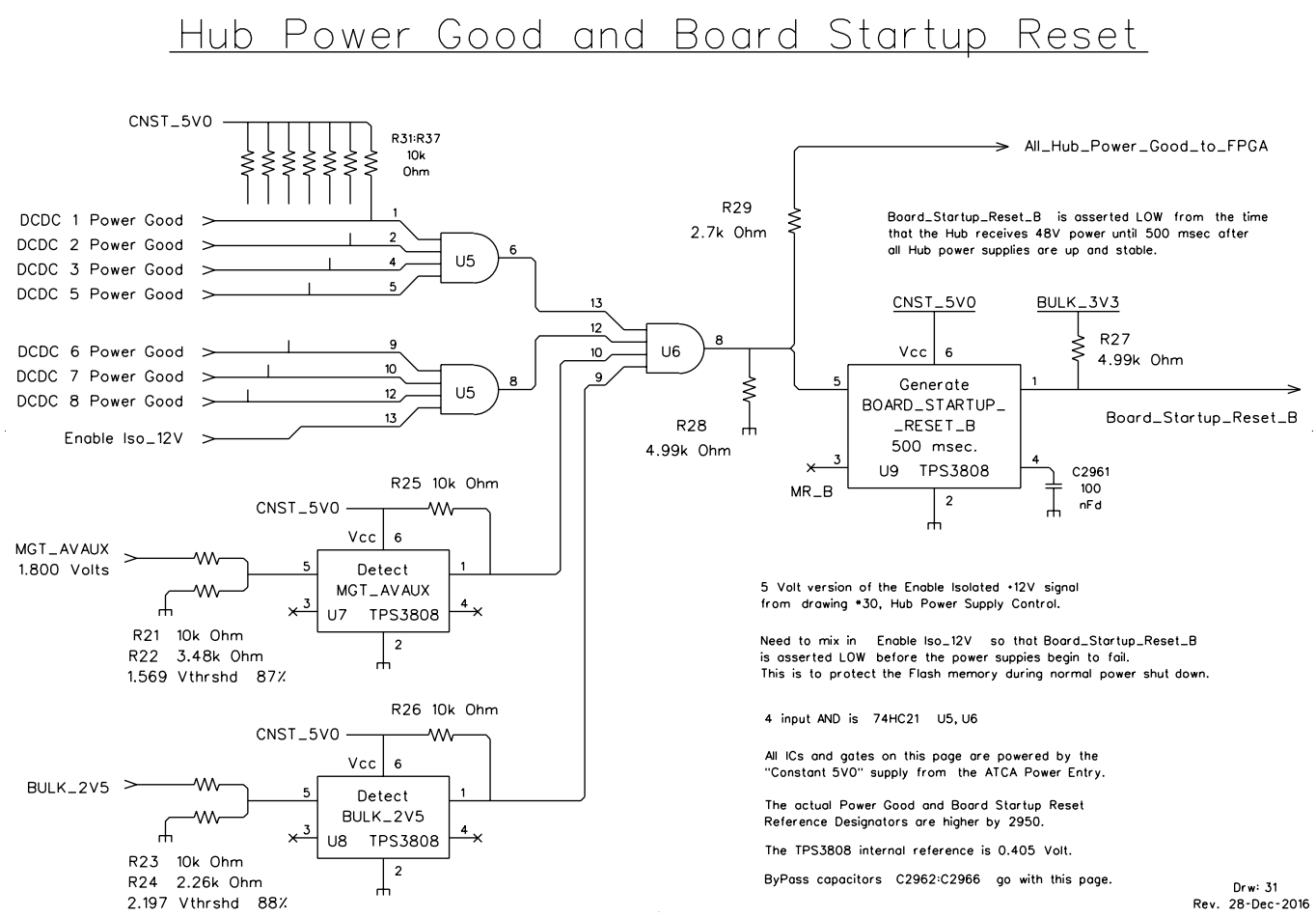

Figure 58: Circuit diagram for Hub power ready/reset (2/2).

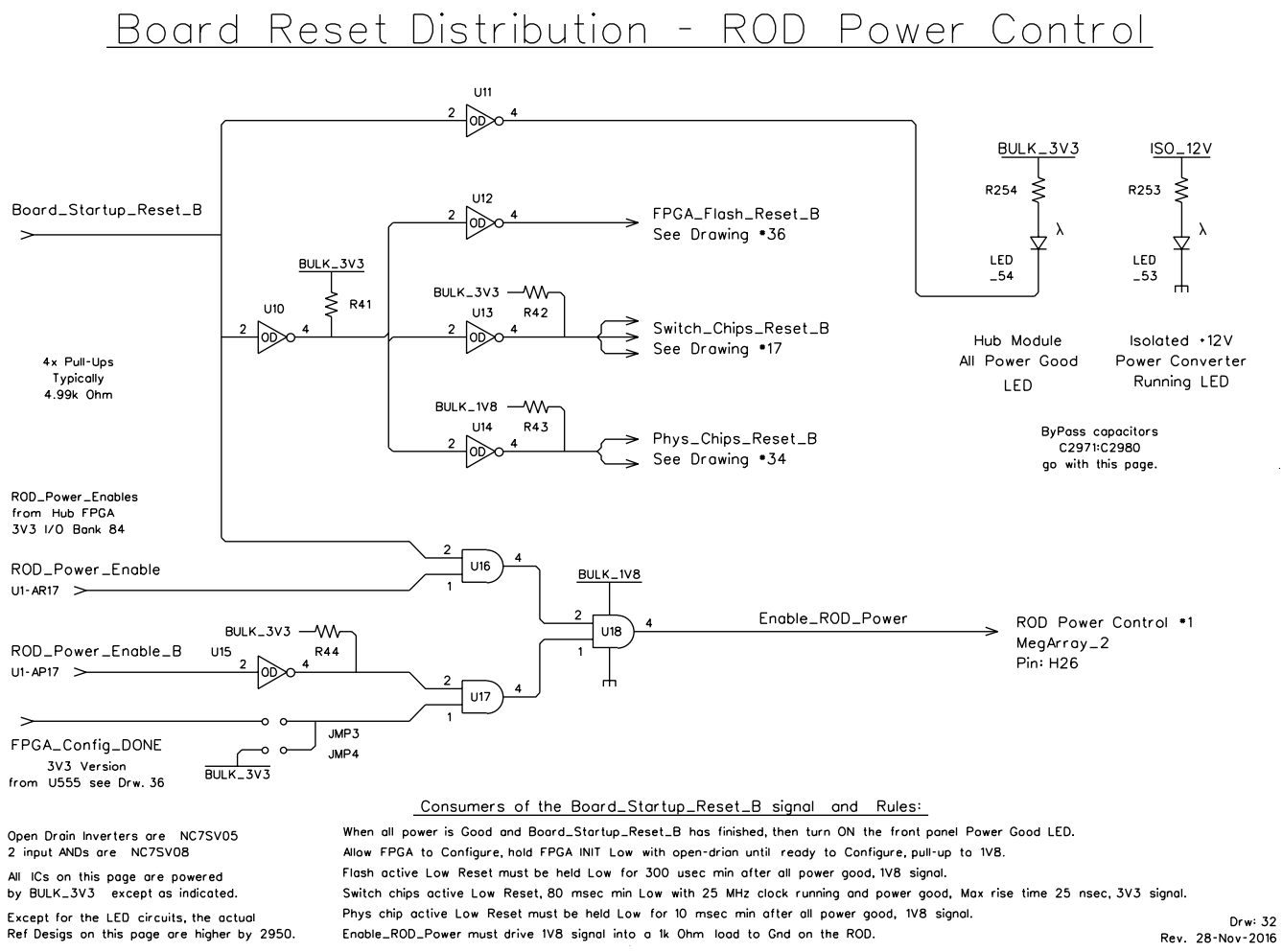

Figure 59: Circuit diagram for Hub board reset distribution.

3509

29 Appendix 16: Hub-Module Base Interface Ethernet Switch

The Hub Module contains a Base Interface Ethernet Switch that is built from 3 Broadcom BCM 53128 KQLE switch chips. The Hub Module Ethernet switch provides ATCA Base Interface Ethernet connections to the following:

- 12 to the FEX Cards via the backplane
- to the Other Hub's FPGA via the backplane
- to This Hub's FPGA via capacitor coupling
- 4 Front Panel RJ-45s 1x to Switch Chip "A",
- 2x to Switch Chip "B",
- 1x to Switch Chip "C"

During normal operation the 4 front panel RJ-45 connections to the Ethernet Switch are used in the following way:

- one is used for the "up-link" connection,
- one is used for the connection to the ROD or IPMC mezzanine on This Hub Module.
- one is used for the connection to the ROD or IPMC mezzanine on the Other Hub Module.

and there is one spare front panel RJ-45 connection to the Ethernet Switch.

Internally there are 4 switch ports used to connect the 3 BMC53128 switch chips: Chip "A" <--> Chip "B" and Chip "B" <--> Chip "C".

The Hub Module does not provide a Base Interface Ethernet connection to the Shelf Manager.

With 2 Hub Modules in an ATCA Shelf the intent is that the switch in one module will provide connection to the "Control" Ethernet and the switch in the other Hub Module will proved connection to the "DCS" Ethernet.

The FEX modules have an ethernet connection to both switches and thus to both networks.

The Hub FPGAs also have an etherent connection to both switches and thus to both networks.

The RODs have only one ethernet connection and both the ROD on This Hub and the ROD on the Other Hub are connected to the Control network switch.

The IPMCs have only one ethernet connection and both the IPMC on This Hub and the IPMC on the Other Hub are connected to the DCS network switch.

Test systems may be operated with a single Hub Module that handles the Etherent connects to both the single ROD and single Hub IPMC in the Shelf.

The Hub's ethernet switch supports 10/100/1000 Base-T operation. The switch is based on 3 Broadcom BCM53128 switch chips. These 3 chips are connected together to form one switch but can also be operated as 2 separate switches. Note that the part used is a BCM53128 not a BCM53128v.

29.1 Power Supply for the BCM53128 Switch Chip

The BCM53128 Switch chip has some rather specific power supply requirements in terms of the number of supplies, their noise level, and the order in which they are ramped up at power on.

The naming of the power buses to this switch chip does not seem to be consistent in all of the BCM53128 documentation so one must be very careful. In the Hub design I have used unambiguous versions of the BMC53128 power supply net names.

Using the power supply net-names from the Data Sheet the required power rails are:

Data Sheet Power Net	Supplies Power to	Details
AVDDH	Analog I/O	3.3V from BULK_3V3 Net-name matches in the Design Guide the Demo Brd Sch and Data Sheet tables and Pin Lists.
AVDDL	Analog Core	1.2V from SWCH_1V2 DCDC Conv. Ferrite isolated on Demo Board. Net-name matches in the Design Guide the Demo Brd Sch and Data Sheet tables and Pin Lists.
DVDD	Digital Core	1.2V from SWCH_1V2 DCDC Conv. Called DVDD in Data Sheet and Sch. Called VDDC in the Design Guide.
OVDD	GMII-RGMII Port	Can be: 1.5V or 2.5V or 3.3V from BULK_3V3 on the Hub. This port is not used on the Hub. Called OVDD in Data Sheet and Sch. Called VDDO1 in the Design Guide.
OVDD2	Digital 3V3 I/O	3.3V from BULK_3V3 Called OVDD2 in Data Sheet and Sch. Called VDDO3 in the Design Guide.
GPHY1_BAVDD	Phys Analog	3.3V from BULK_3V3 Ferrite isolated on Demo Brd. Called GPHY1_BAVDD in Data Sheet Table 32 Signal Definitions and Design Guide Pg 62. Called GPHY1_BVDD in the Schematic and the Data Sheet Pin Lists. Called QGPHY1_BVDD1 in the Design Guide Pg 61.
GPHY2_BAVDD	Phys Analog	3.3V from BULK_3V3 Ferrite isolated on Demo Brd. Called GPHY2_BAVDD in Data Sheet Table 32 Signal Definitions and Design Guide Pg 62. Called GPHY2_BVDD in the Schematic and the Data Sheet Pin Lists. Called QGPHY2_BVDD1 in the Design Guide Pg 61.
PLL_AVDD	PLL Analog	1.2V from SWCH_1V2 DCDC Conv. Ferrite isolated on Demo Brd. Called PLL_AVDD in all documents but not listed Pg 61 Design Guide.
GPHY1_PLLDVDD	Phys Analog	1.2V from SWCH_1V2 DCDC Conv. Ferrite isolated on Demo Brd. Called

		GPHY1_PLLDVDD in Data Sheet Table 32 Signal Definitions and Design Guide Pg 62. Called GPHY1_PLLVDD in the Schematic and the Data Sheet Pin Lists. Called QGPHY1_PLLVDD in the Design Guide Pg 61.
GPHY2_PLLDVDD	Phys Analog	1.2V from SWCH_1V2 DCDC Conv. Ferrite isolated on Demo Brd. Called GPHY2_PLLDVDD in Data Sheet Table 32 Signal Definitions and Design Guide Pg 62. Called GPHY2_PLLVDD in the Schematic and the Data Sheet Pin Lists. Called QGPHY2_PLLVDD in the Design Guide Pg 61.
XTAL_AVDD	Osc Analog	3.3V from BULK_3V3 Ferrite isolated on Demo Brd. Called XTAL_AVDD in all documents but not in Design Guide Pg 61 or 62.

References: see pages 61, 62 in the Design Guide, the Demo Board Schematics, and in the Data Sheet pages 136 and the pin lists starting on page 138.

This is a total of 11 supply buses to the Switch Chip. As implemented on the Demo Brd, 7 of them have Ferrite power noise filters.

There are a number of additional power supply related pins:

GPHYS1_RDAC Bias Setting Pin 1.24k Ohm to Gnd Required.

GPHYS2_RDAC Bias Setting Pin 1.24k Ohm to Gnd Required.

IMP_VOL_REF IMP Interface Voltage Reference Gnd this pin.

PLL_AVSS Gnd Tie this pin to Logic Ground.

XTAL_AVSS Gnd Tie this pin to Logic Ground.

Exposed_Pad Gnd Tie this pin to Logic Ground.

As such I do not think that there are any Gnd pins on this part. Its one and only ground connection is through its center Exposed Thermal Pad.

The power supply connections to a Switch Chip on the Hub Module are shown in **Figure 60**.

29.2 Power-Up Supply Sequencing

The required power supply ramp up sequence is discussed on page 62 and 63 of the Design Guide. They say that failure to properly sequence the supplies will not damage the device but the for "successful" power up the proper supply sequence must be followed and the Reset line used in the proper way.

The BCM53128 device requires specific power sequencing between the core and I/O supplies.

- The device power sequence requires I/O power (3.3V, 2.5V) to come up first, followed by the core power (1.2V). The requirement is that the core power (1.2V) should not be on until the I/O power (3.3V, 2.5V) reaches at least 1.0V.
- When the core power reaches nominal core voltage (1.2V +-5%), the I/O power should be stable at nominal I/O voltage (3.3V +-5% or 2.5V +-5%).
- The max ramp-up time for core power 1.2V (from 0V to nominal voltage +-5%) is 2 msec. See page 63.
- Additionally, for successful power-up, Broadcom recommends that the external hardware reset be active for at least 80 msec after both I/O and core power are stable. See page 63.

Note that the required power-up sequence rules out ramping all supplies Volt for Volt because they do not want any power on the core until the I/O is up to at least 1.0V.

Thus the Hub Module needs a separate delayed 1.2V Core supply for the Switch Chips. Having a separate 1.2V supply for the Switch Chips was kind of in the cards anyway because clearly it can not be shared with the 1.2V Virtex MGT supply.

The power supply current requirements on page 298 of the data sheet appear to be total current from the various voltage buses. I don't know if there are extra start up requirements.

1.2 Volt 1130 mA
2.5 Volt 26 mA (if used)

3.3 Volt 496 mA

29.3 Hub Module Power Supply Design for Its Switch Chips

A separate 12 Amp supply is used for the Switch's 1.2 Volt requirements. This is a GE UDT020A0X1 DCDC Converter and it is enabled after the other DCDC Converters on the Hub Module have all ramped up and specifically after the BULK_3V3 converter has ramped up.

The typical draw on this SWCH_1V2 bus for all 3 switch chips is expected to be 3.5 Amps. The typical draw on the BULK_3V3 bus for all 3 switch chips is expected to be 1.5 Amps. The expected heat load for all 3 switch chips is 9.2 Watts.

The OVDD power bus to the Switch Chips can be either 2.5 Volt or 3.3 Volt. The OVDD rail powers the GMII - RGMII port I/O pins. On the Hub Module the GMII-RGMII port is not used and for convenience the OVDD rail is powered from the BULK_3V3 supply.

The sources of the 11 supply rails to the BCM53128 Switch Chips on the Hub Module are the following:

AVDDL	1.2V	from SWCH_1V2 DC/DC Converter
DVDD	1.2V	from SWCH_1V2 DC/DC Converter
PLL_AVDD	1.2V	from SWCH_1V2 DC/DC Converter
GPHY1_PLLDVDD	1.2V	from SWCH_1V2 DC/DC Converter
GPHY2_PLLDVDD	1.2V	from SWCH_1V2 DC/DC Converter
AVDDH	3.3V	from BULK_3V3 DC/DC Converter
OVDD	3.3V	from BULK_3V3 DC/DC Converter
OVDD2	3.3V	from BULK_3V3 DC/DC Converter
GPHY1_BAVDD	3.3V	from BULK_3V3 DC/DC Converter
GPHY2_BAVDD	3.3V	from BULK_3V3 DC/DC Converter
XTAL_AVDD	3.3V	from BULK_3V3 DC/DC Converter

29.4 Switch Chip Bypass Capacitors and Filter Chokes

Recall the power supply bypass capacitors recommended by Broadcom. The following is a combination of the BCM53128 Design Guide and the Demo Board Schematic.

- PLL_AVDD pin (each one) is connected to the Analog 1.2V plane via the ferrite bead. Each pin is bypassed with 22 uFd and 100 nFd capacitors.
- AVDDL pins are connected to the Analog 1.2V plane and bypassed with a 33 uFd capacitor. Each pin is decoupled with a 1.0 uFd capacitor.
- DVDD pins are connected to the Digital 1.2V plane and bypassed with a 10 uFd capacitor. Each pin is bypassed with a 100 nFd capacitor.
- GPHY1_PLLDVDD pins are connected to the Digital 1.2V plane and bypassed with a 10 uFd capacitor. Each pin is bypassed with a 100 nFd capacitor.
- GPHY2_PLLDVDD pins are connected to the Digital 1.2V plane and bypassed with a 10 uFd capacitor. Each pin is bypassed with a 100 nFd capacitor.
- XTAL_AVDD pins are connected to the 3.3V plane and bypassed with a 100 nFd capacitor.

- AVDDH pins are connected to the 3.3V plane and bypassed with a 33 uFd capacitor. Each pin is bypassed with a 1.0 uFd capacitor.
- OVDD2 pins are connected to the 3.3V plane and bypassed with a 10 uFd capacitor. Each pin is bypassed with a 100 nFd capacitor.
- OVDD pins are connected to either the 2.5V or 3.3V plane and bypassed with a 10 uFd capacitor. Each pin is bypassed with a 100 nFd capacitor.
- GPHY1_BAVDD pins are connected to the 3.3V plane and bypassed with a 10 uFd capacitor. Each pin is bypassed with a 100 nFd capacitor.
- GPHY2_BAVDD pins are connected to the 3.3V plane and bypassed with a 10 uFd capacitor. Each pin is bypassed with a 100 nFd capacitor.

On the Hub Module the following 7 supply rails to the switch chips are isolated with a ferrite filter chokes:

AVDDL	1.2V
PLL_AVDD	1.2V
GPHY1_PLLDVDD	1.2V
GPHY2_PLLDVDD	1.2V
GPHY1_BAVDD	3.3V
GPHY2_BAVDD	3.3V
XTAL_AVDD	3.3V

From the demo board schematics I believe that ferrite chokes with a reactance of 600 Ohms at 100 MHz and a 2 Amp capacity with less than 100 mOhm resistance is adiquate for all 7 of these applications.

On the Hub Module the following 4 supply rails to the switch chips are not isolated with a filter choke:

DVDD	1.2V
AVDDH	3.3V
OVDD	3.3V
OVDD2	3.3V

29.5 The BCM53128 Switch Capacitive Coupling

Page 29 of the BCM53128 Design Guide explains that capacitive coupling can be used between pairs of BCM53128 chips for all 3 ethernet speeds. Capacitive coupling works between BMC53128 chips because the BCM53128 uses Voltage Mode Phy technology.

Capacitive coupling should also work between the BMC53128 and other parts that use Voltage Mode Phy technology.

There are termination schemes that use capacitive coupling between the BCM53128 and parts with older Current Mode Phys parts but this is probably speed dependent and is not needed on the Hub Module.

The Micrel KSZ9031 Phys has a voltage mode transmitter connection to the medium so it can probably work with capacitive coupling. The KSZ9031 data sheet talks only about connection with magnetics. Because the KSZ9031 has voltage mode transmitters, the center tap on the chip's side of the transformer should just be tied to ground with a 100 nFd capacitor (i.e. not connection to a power bus). This is just like the transformer connection to the BCM53128 switch chip.

The Hub Module design uses capacitive coupling between the 3 BCM53128 Switch chips and between the BCM53128 and the KSZ9031RNX Phys for the Hub's FPGA.

29.6 Switch Chip Orientation and Port Connections

For all 3 Switch Chips their pin #1 will be in the SE corner.

The 1:64 edge is to the East with its Clock, JTAG, 3 LED, and unused IMP connections.

The 65:128 edge is to the North. This is Ports 4:7 with Port 4 closest to the Hub's back edge.

The 129:192 edge is to the West. This is a bunch of unused IMP stuff and then the bulk of the LED connections.

The 193:256 edge is to the South. This is a few LED connections and then Ports 0:3 with Port 3 closest to the back edge of the Hub.

Based on the placement of the Switch Chips running B, A, C across the card from front to back and based on the Switch Chip's orientation the following Port assignments are the most straight forward to route.

Chip "A" U31 is in the center of the row:

Port 0 to J24 Row 8 BI Channel 14 Slot 14 FEX

Port 1 to J24 Row 7 BI Channel 13 Slot 13 FEX

Port 2 to J24 Row 6 BI Channel 12 Slot 12 FEX

Port 3 to J24 Row 5 BI Channel 11 Slot 11 FEX

Port 4 to J24 Row 4 BI Channel 10 Slot 10 FEX

Port 5 to J24 Row 3 BI Channel 9 Slot 9 FEX

Port 6 to Front Panel RJ-45 Connector RJ2 Lower/Left

Port 7 to Switch Chip “B” Capacitor Coupled

Chip “B” U32 is the “center” Switch Chip:

Port 0 not used

Port 1 not used

Port 2 to Switch Chip “A” Capacitor Coupled

Port 3 to Switch Chip “C” Capacitor Coupled

Port 4 to This Hub’s FPGA Capacitor Coupled

Port 5 to J20 Row 3 Update Channel to Other Hub

Port 6 to Front Panel RJ-45 Connector RJ3 Lower/Left

Port 7 to Front Panel RJ-45 Connector RJ3 Upper/Right

Chip “C” U33 is near the cards backplane edge:

Port 0 to J24 Row 2 BI Channel 8 Slot 8 FEX

Port 1 to J24 Row 1 BI Channel 7 Slot 7 FEX

Port 2 to J23 Row 10 BI Channel 6 Slot 6 FEX

Port 3 to J23 Row 9 BI Channel 5 Slot 5 FEX

Port 4 to J23 Row 8 BI Channel 4 Slot 4 FEX

Port 5 to J23 Row 7 BI Channel 3 Slot 3 FEX

Port 6 to Front Panel RJ-45 Connector RJ2 Upper/Right

Port 7 to Switch Chip “B” Capacitor Coupled

29.7 Assignment of Ethernet "Magnetics"

These assignments are given in Section 17.

29.8 Assignment of Front Panel RJ-45 Connectors

These assignments are given in Section 17.

29.9 Resistor Set Pin

The RDAC pins, GPHY1_RDAC pin 228 and GPHY2_RDAC pin 96 must be connected to Ground with 1.24k Ohm 1% resistors.

29.10 Unused Tie Hi, Tie Low, Float Pins

There are a number of un-used and no-connect pins on the switch chips. Some of the un-used pins must be tied Hi or Low - others must be left floating.

IMP_VOL_REF pin 146 must be tied to Ground.

CLK_FREQ0/GPIO0 pin 14 must be left floating

CLK_FREQ1/GPIO1 pin 15 must be left floating

IMP RGMII Inputs: RXCLK, RXD(3:0), RXCTL (aka RXDV)

should all be Pulled-Down These are pins:

144, 154, 152, 151, 150, 149

LOOP_DETECTED pin 58 warning buzzer if a Loop

is Detected - float

No Connect Pins from BCM Datasheet:

NC 5 this is a second MDIO aka MDIO2

NC 6 this is a second MDC aka MDC2

NC 20

NC 28

NC 37

NC 39

NC 41

NC 42

NC 45

NC 46

NC 69

NC 70

NC 99

NC 225

Other unused pins, e.g.

LEDCLK 167 HP has small cap to gnd Kit has 100 pFd to gnd

LEDDATA 166 HP has small cap to gnd Kit floats

TRST pin 36 has an internal Pull-Up but Must be pulled Low

7. for normal operation. See datasheet page 129.
8. Kit has a DNI pull-down. HP has a pull-down.

29.11 EEPROM Connection to the Switch Chip

The BCM53128 contains about 200 internal registers. The initial running state of many of these registers may be set at power up by the contents of an attached EEPROM.

Figure 61 shows the connection of this EEPROM to the BCM53128 switch. This drawing also shows the Clock, Reset, and management connections to the Swtich Chip.

The EEPROM is an AT93C66B device with 8 pins. Note that an earlier Atmel device (AT93C66A-2.7) had originally been specified for use with the BCM53128. This EEPROM is powered from the 3V3 bus and 4 of its pins connect to the switch chip:

SS slave select pin 160 Low active to the EEPROM

SCK SPI Clock pin 163 to the EEPROM

MOSI Master Out Slave In pin 164 input to the EEPROM

MISO Master In Slave Out pin 161 output from EEPROM

All 4 of these pins use series damping resistors, e.g. 22 Ohm. In addition to these 4 signal pins this EEPROM has one power pin and one ground pin and one not connected pin.

The ORG pin on the EEPROM is pulled up to set it for 16 bit words. The AT93C66B stores 256 16 bit words.

Note that this: SS, SCK, MOSI, MISO interface to the switch chip can be used for either: EEPROM or SPI bus - but not for both. It's use is set for ever more at power up by the CPU_EEPROM_SEL strapping pin, pin 18. Pull it down to enable use with the EEPROM. At power up I think it's basically an issue of setting up the switch's SPI port as a SPI master or a slave.

We still have the questions of what content to put into this EEPROM for the Hub application, can all 3 EEPROMs contain exactly the same data, how to program them, and how to change their data if there is a problem in the future.

Because of these uncertanties I want to put the EEPROMs on the back side of the Hub PCB and keep them open and easy to change. To facilitate this I will use an SOIC-8 part. This should be part number: AT93C66B-SSHM -B or -T. Both are good DK numbers. This is a normal SOIC with a 3.90 mm wide body, i.e. feet about 6.00 mm wide. Atmel says that its maximum height is 1.75 mm so it fits within the Hub's 2.00 mm side 2 comp height rule.

29.12 SPI Bus Connection

The BCM53128 switch chip includes a serial SPI bus connection. This SPI serial bus allows control and monitoring of the chip through its various registers. The problem is that the SPI serial bus and the EEPROM share the same pins on the device. At power up, a strapping option sets these pins to operate as either an SPI bus interface or as an EEPROM interface. Once this option is set it can not be changed.

In the Hub Module we need to use these pins for EEPROM setup of the switch chips. For subsequent control and monitoring of the switch chips from the Hub's FPGA we need to use the MDC MDIO management interface to the device.

29.13 MDC MDIO Connection to the Hub's Virtex FPGA

The Hub uses the Switch Chip's MDC MDIO port in slave mode so that an external entity, i.e. the Hub's FPGA, can access registers within the Switch. See the Datasheet starting at page 112 and on page 128. See the Design Guide starting on page 56.

MDIO pin 61 Data I/O pin

"In slave mode, it is used by an external entity to read/write to the switch registers via the Pseudo-PHY."

MDC pin 62 Clock pin

"In slave mode (the clock) is sourced by an external entity."

29.14 Switch Chip Reset

The BCM53128 Swtich Chip needs a Reset signal that remains asserted until 80 msec after all of its power supply rails are fully ramped up. We may also want to be able to reset one or all of the Switch Chips from a protected register in the Hub Module's Virtex FPGA. The minimum pulse width of the Reset signal is 1 msec. One must wait 50 msec after the end of the Reset signal before trying to talk to the switch chip via its SPI bus. The Reset signal is pin 17. The Reset signal is Low active.

29.15 Clock to the Switch Chip

The Hub Module uses an external 25 MHz clock source to provide the clock to all 3 of its Switch Chips. This external clock enters the chip on its XTAL1 pin 34 and the XTAL0 pin 33 is left floating. The clock source for the Switch Chips must be:

25 MHz +- 50 ppm,
50% duty cycle,
1 to 4 nsec edge speed,
3V3 CMOS level,
5 ppm per year,
10 ppm over temperature,
less then 100 psec jitter
very low jitter in the 5 kHz to 1 MHz band.

The Hub Module supplies this clock from a Connor Winfield CWX813-025.0M oscillator with a 6x fanout and series terminator resistors.

29.16 Switch Chip Functions That Are Not Used on the Hub

One must understand whether or not any pull-up / pull-downs are needed to not use these functions so that they just sit quietly as good citizens.

- Flash Memory, pins: FSO 64, FCSB 65, FSCLK 66, FSI 67 Note that the Flash Memory is for 8051 code only.
- JTAG, pins: TDO 22, TDI 23, TCK 24, TMS 25, TRST 36
- IMP Interface - this is the Inband-Management-Port, i.e. a PhysLess port that can operate as: GMII, RGMII, MII, TMII, RxMII or whatever to manage the switch chip. We do not want it at all - thus we must tie DIS_IMP strap pin Hi. The IMP pins - note that the Design Guide says to tie Low unused IMP pins: RXCLK, RXD(3:0), RXCTL but that neither the Kit or HP does this.
- List of IMP pins:

IMP_VOL_REF 146 must be tied Low

IMP_VOL_SEL1 48, IMP_VOL_SEL0 49

IMP_COL 159, IMP_CRS 143

IMP_DUPLEX 52, IMP_LINK 54

IMP_MODE0/GPIO5 7, IMP_MODE1/GPIO6 8

IMP_PAUSECAP_RX 55, IMP_PAUSECAP_TX 56

IMP_SPEED1 50, IMP_SPEED0 51

IMP_GTXCLK 132, IMP_RXCLK 144

IMP_RXD0 150, IMP_RXD1 151

IMP_RXD2 152, IMP_RXD3 154

IMP_RXD4 155, IMP_RXD5 156

IMP_RXD6 157, IMP_RXD7 158

IMP_RXDV 149, IMP_RXER 147

IMP_TXCLK 141, IMP_TXD0 137

IMP_TXD1 136, IMP_TXD2 134

IMP_TXD3 131, IMP_TXD4 130

IMP_TXD5 128, IMP_TXD6 127

IMP_TXD7 126, IMP_TXEN 139

IMP_TXER 140

29.17 Switch Chip Bypass Capacitor and Filter Update

During the tentative final placement of the 100 or so RCL comps for each Switch chips the following changes were made:

PLL_AVDD C01 C02 L01 no-change

GPHY1_PLLDVDD C03 C04 L02 no-change

GPHY2_PLLDVDD C05 C06 L03 no-change

GPHY1_BAVDD C07 C08 L04 no-change

GPHY2_BAVDD C09 C10 L05 no-change

XTAL_AVDD C11 C12 L06 no-change

DVDD SWCH_1V2 C36,C37 C38:C47 no-change

AVDDL 1V2 C13,C14 C16:C30 L07

remove from set: C15 C33,C34,C35

AVDDH \ C48, C49, C50

OVDD | BULK_3V3 C51:C62

OVDD2 / C78:C85

remove from set: C67, C68, C76, C77

C63, C64, C65, C66

C69:C75

C86:C90

The components that have been removed from the relatively positioned component set are now in their own comps file for manual positioning.

Other Changes in Switch Comps:

R2x19 the clock series terminator has been moved
out of the Switch Chip Comps files and into
the 25 MHz Enet Clock Generator comps file.

C2x91 for the Switch EEPROM has been moved to the
top side of the card.

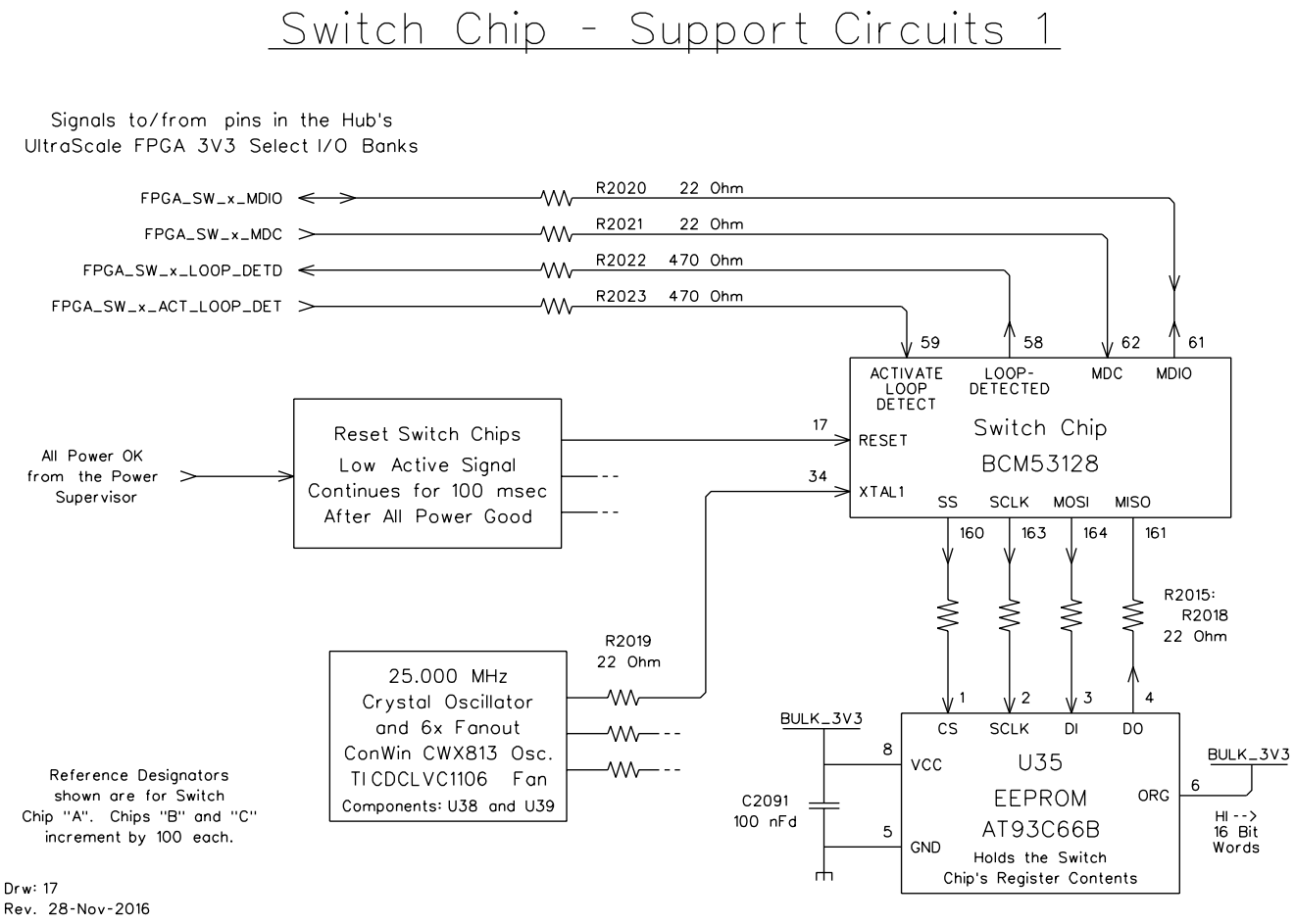

Figure 60: Hub switch chip support circuit diagram (1/3).

3919

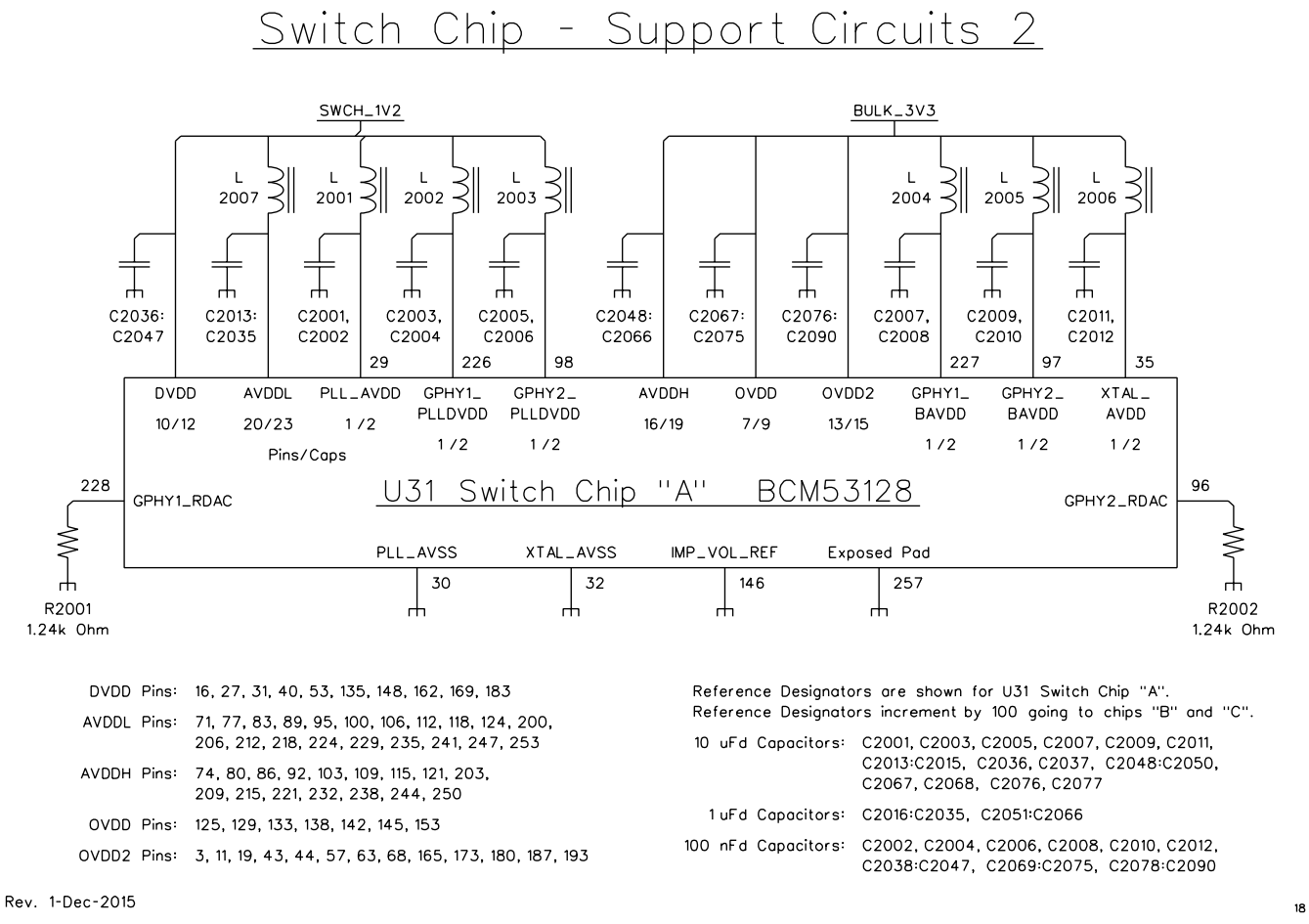

Figure 61: Hub switch chip circuit diagram (2/3).

3920

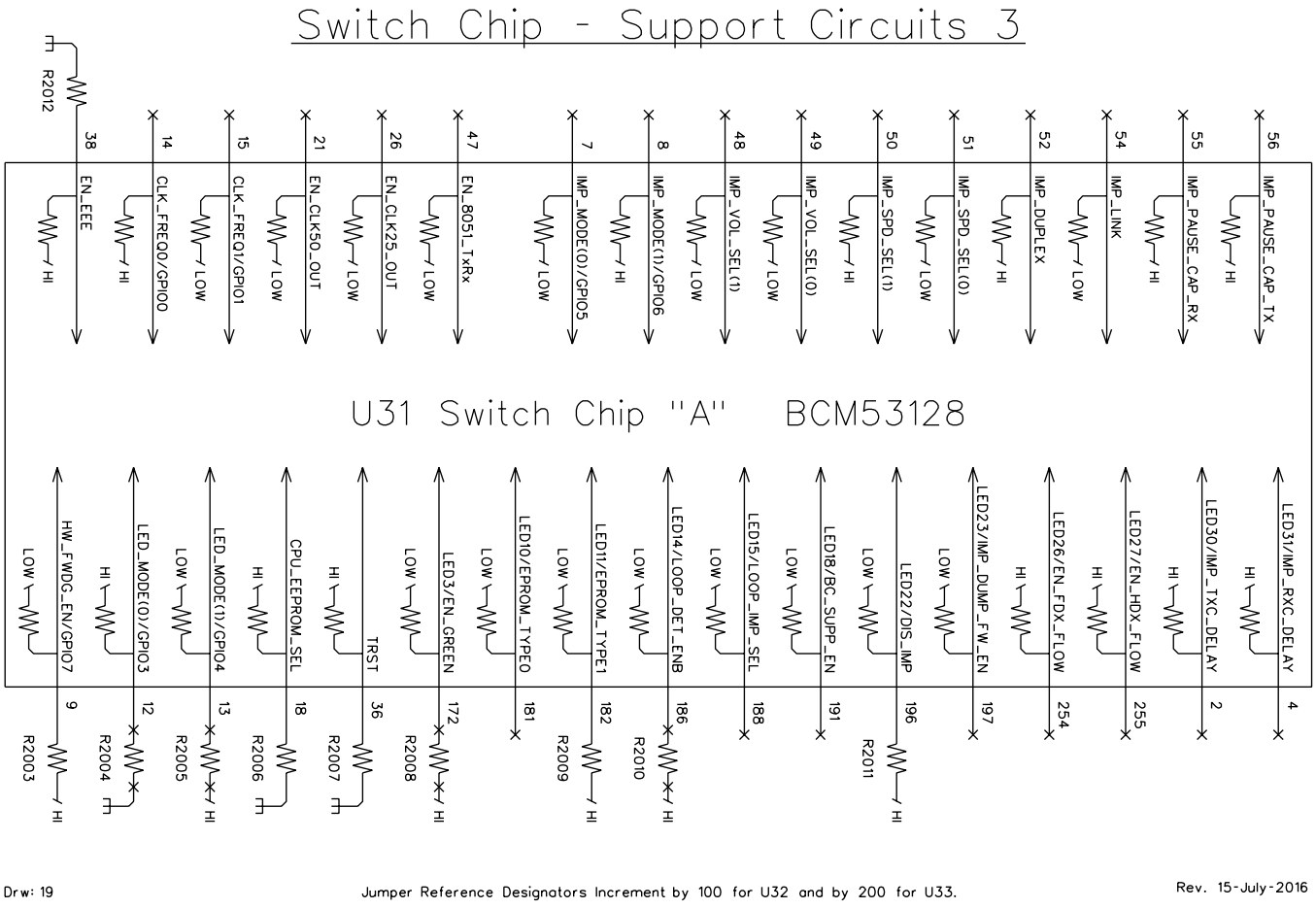

Figure 62: Hub switch chip circuit diagram (3/3).

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30 Appendix 17: Switch Chip Associated Jumpers

The BMC53128 switch chip has a large number of "straping" pins (33) to provide basic control its various functions. The use of these strapping pins is complicated because there are interactions between then and because the documentation seem incomplete and different sections of the documentation frequently call the same object by different names and frequently use slang names, e.g. green means don't use the 8051.

On the Hub Module, to the extent that space limitations allow, the approach taken (same as HP used) is to provide a 0603 jumper site for each strapping pin that is tied to the opposite rail than the default internal pull up/down resistor for that pin. This gives us a way to make post production changes if necessary.

The 0603 site has not been provided for some strapping pins where their funtions were clear and where we wanted the default provided by the internal pull up/down resistor. In these cases trace routing is such that access can be made to the signal if necessary.

The 33 strapping pins and their internal pull up/down resistors and their external 0603 jumper sites are shown in **Figure 62**.

30.1 Enumeration of All Strapping Options on the BCM53128

Signal Name	Pin #	Int'l Default	BCM Docs Say	Kit	HP	Hub
CLK_FREQ1/GPIO1	15	PD	Must Float in all designs DG pg 39	DNI PU	Float	---
CLK_FREQ0/GPIO0	14	PU		DNI PD	Float	---
EN_CLK25_OUT/CLK_25_OUT	26	PD	Low --> Disable	Float	Float	---
EN_CLK50_OUT/CLK_50_OUT	21	PD		Float	Float	---
EN_EEE	38	PU	Hi->Enable	Float	Float	YID
EN_8051_TxRx	47	PD	Hi->Enable	Float	Float	---
IMP_MODE(1)/GPIO6	8	PU	Sets IMP Mode	Float	Float	---
IMP_MODE(0)/GPIO5	7	PD		Float	Float	---
IMP_VOL_SEL(1)	48	PD	Both Low --> 3V3	Float	Float	---
IMP_VOL_SEL(0)	49	PD		Float	Float	---
IMP_SPD_SEL(1)	50	PU	Default for normal operation	Float	Float	---
IMP_SPD_SEL(0)	51	PD		Float	Float	---
IMP_DUPLEX	52	PU	Hi->Duplex	Float	Float	---
IMP_LINK	54	PD	Hi->LinkUp	Float	Float	---
IMP_PAUSE_CAP_RX	55	PU	Hi->EnbPause	Float	Float	---
IMP_PAUSE_CAP_TX	56	PU	Hi->EnbPause	Float	Float	---
HW_FWDG_EN/GPIO7	9	PD	HI to Enb Frame Fwd	has PU	has PU	YIU

LED_MODE(1)/GPIO4	13	PD	Set LED Mode	DNI PD	has PD	YBU
LED_MODE(0)/GPIO3	12	PU		DNI PU	Float	YBD
CPU_EEPROM_SEL	18	PU	Low to Enb EEPROM	has PD	has PD	YID
TRST	36	PU	Pull Low for normal operation	DNI PD	has PD	YID
LED3/EN_GREEN	172	PD	Hi->Enable Green Mode DS Pg 133 DG pg 56	has PU	Float	YBU
LEDP11/EPROM_TYPE1	182	PD	10b is PROM type 93C66	has PU	has PU	YIU
LEDP10/EPROM_TYPE0	181	PD		Float	Float	---
LEDP14/LOOP_DETECT_EN	186	PD	Hi->Enable	has PU	Float	YBU
LEDP15/LOOP_IMP_SEL	188	PD	Hi->Include	Float	Float	---
LEDP18/BC_SUPP_EN	191	PD	Hi->Enable Rate Brdcst Supp	Float	Float	---
LEDP22/DIS_IMP	196	PD	Hi->Disable	has PU	has PU	YIU
LEDP23/IMP_DUMB_FWDG_EN	197	PD	Hi->Allow Dumb Forward	Float	Float	---
LEDP26/ENFDXFLOW	254	PU	Hi->Not Clear from DS or DG	Float	Float	---
LEDP27/ENHDXFLOW	255	PU	Hi->Enable	Float	Float	---
LEDP30/IMP_TXC_DELAY	2	PU	Hi->Enable	Float	Float	---
LEDP31/IMP_RXC_DELAY	4	PU	Hi->Enable	Float	Float	---

Hub Notation Key:

- YIU -> Yes Hub has an Installed jumper and it's a Pull-Up
- YID -> Yes Hub has an Installed jumper and it's a Pull-Dowm
- YBU -> Yes Hub has a Not-Installed jumper and it's a Pull-Up
- YBD -> Yes Hub has a Not-Installed jumper and it's a Pull-Dowm
- --- -> For these, the Hub does not have a jumper for this function

31 Appendix 18: Hub-Module Xilinx FPGA

The UltraScale Virtex device on the Hub Module is a: XCVU125-1FLVC2104I

This is speed grade "1", i.e. the normal common slowest speed grade and it is the "Industrial" temperature range which is the common temp range for most of these UltraScale parts.

This part has: 40 GTH Transceivers and 40 GTY Transceivers. These are spread across 2 SLRs with 20 of each kind of transceiver in each SLR.

This part has 7 HP Select I/O Banks with 52 I/O signals in each. 4 of the HP banks are in SLR #0 and 3 of the HP banks are in SLR #1.

This part also has 2 HR Select I/O Banks with 26 I/O signals in each. Both of the HR banks are in SLR #0. The Hub Module uses both of the HR Banks for 3V3 I/O and it uses most of the signals in these Banks.

The FLVC2104 package has 2104 pins in a 1mm by 1mm square array with 46 pins on each side and 3 pins missing at each corner. This is a No-Lead package.

31.1 FPGA Configuration:

The Hub's UltraScale Virtex FPGA is configured in Master BPI mode from a Micron MT28GU01GAAA1EGC-OSIT NOR Flash memory. This method of configuration requires pins in both the special Bank #0 and most of the pins in Select I/O Bank #65.

Figure 63 shows the details of this configuration setup.

The MT28GU01GAAA1EGC-OSIT Flash memory holds 1 Gb of data. The XCVU125 FPGA requires 401,441,280 bits to configure so the Hub Module can hold 2 versions of FPGA Firmware.

31.2 FPGA JTAG Connection

The Hub Module provides a front panel JTAG connection via its J2 "Access Connector". A 1V8 version of this JTAG string is routed to the Hub's FPGA as shown in **Figure 37**.

31.3 FPGA System Monitor Reference and Connections

The hub provides an external precision reference and filtered power for the FPGA System Monitor. This is shown in **Figure 64**. The IPMC's Sensor I2C bus is routed to the slave I2C port to the System Monitor as shown in **Figure 36**.

31.4 FPGA MGT Transceivers

The Hub design uses all 80 MGT Receivers and 29 of the MGT Transmitters. Note that this FPGA's MGT transceivers are shared across both of its SLRs.

The assignment of the MGT transceivers is listed in Section 18. The connections to the GTY and GTH Banks are shown in **Figure 29** and **Figure 30**.

31.5 FPGA RGMII Ethernet Base Interface Connection

The Hub Module FPGA is connected to 2 Micrel KSZ9031RNX Phys chips. These Phys chips provide 10/100/1000 speed ethernet connection between the FPGA and the Switch on This Hub and via the backplane to the Switch on the Other Hub.

The Phys RGMII to FPGA connections are made to HP Bank #68.

Besides the MACs to run these connections the FPGA firmware may want MACs to run the MDC MDIO management links to the 3 Switch chips.

31.6 FPGA Clock Sources

The Hub's FPGA is provided with the following clocks:

- 25.000 MHz Ethernet Clock single ended 3V3 to Bank 94
- 40.08 MHz LHC Clock LVDS Logic Clock to Bank 71
- 320.64 MHz LHC Clock Cap Coupled LVPECL Logic Clk to Bank 71
- 8x 320.64 MHz LHC Clock Cap Coupled LVPECL MGT Reference Clk
- 2x 125.000 MHz Ethernet Clock single ended 1V8 level
- Each Phys Chip returns its 5x multiplied Clk to Bank 68 in the FPGA

31.7 The Select I/O Signals

The Hub design currently uses about 166 Select I/O signals. Both 1V8 and 3V3 levels are used. The 3V3 levels are from HR Select I/O Banks 84 and 94.

The Hub's use of FPGA Select I/O signals is listed in Sections 19 and 20.1.

31.8 FPGA Power Supply Requirements

The intent here is to list the full details of this FPGA's power supply and bypass capacitor requirements. Then in the Hub Power Supply Design document only a short summary of these FPGA's power requirements will be presented along with a summary of the power supply requirements of the other components on the Hub Module.

UltraScale XCVU125-FLVC2104 Recommended Operating Conditions:

- VCCINT 0.950 V +- 3.0%
- VCCINT_IO 0.950 V +- 3.0%
- VCCBRAM 0.950 V +- 3.0%
- VCCAUX 1.800 V +- 3.0%

- VCCAUX_IO 1.800 V +- 3.0%
- VCCO HR 1.140 V to 3.400 V
- VCCO HP 0.950 V to 1.890 V
- VBATT
  - MGTAVCC 1.000 V +- 3.0%
  - MGTAVTT 1.200 V +- 2.5%
  - MGTVCCAUX 1.800 V +- 2.8%

VCCINT_IO must be connected to VCCINT

VCCAUX_IO must be connected to VCCAUX

If VBATT is not used then connect VBATT to either ground or to VCCAU, then VCCO_0 must be a minimum of 1.425V during configuration.

Quiescent Supply Currents:

- VCCINT 2875 mA
- VCCINT_IO 178 mA
- VCCBRAM 162 mA
- VCCAUX 373 mA
- VCCAUX_IO 148 mA
- VCCO 1 mA (assume per Bank)

Power Supply Sequencing and Common Supplies:

At Power ON:

VCCINT / VCCINT_IO then VCCBRAM then

VCCAUX / VCCAUX_IO then VCCO

Power OFF is the reverse.

VCCINT / VCCINT_IO and VCCBRAM can all be powered from the same supply and ramped simultaneously.

VCCAUX / VCCAUX_IO and VCCO can all be powered from the same supply and ramped simultaneously.

VCCINT and MGTAVCC may be ramped simultaneously.

MGTAVCC should ramp before MGTAVTT.

No recommended sequencing for MGTVCCAUX.

Besides the Quiescent currents listed above the supplies must be able to provide the following minimum currents during power up:

- VCCINT / VCCINT_IO supply 4397 mA minimum additional current
- VCCBRAM 200 mA
- VCCAUX / VCCAUX_io supply 533 mA
- VCCO supply 54 mA

All ramp times are 200 usec minimum and 40 msec max.

3.0 msec is about in the middle 16x from either side.

From the “ultrascale PCB design guide” ug583

ByPass Capacitor Requirements for the XCVU125-FLVC2104:

- VCCINT / VCCINT_IO 2x 680 uFd, 3x 100 uFd, 5x 4.7 uFd
- VCCBRAM 1x 47 uFd, 1x 4.7 uFd
- VCCAUX / VCCAUX_IO 2x 47 uFd, 4x 4.7 uFd
- VCCO HR or HP 1x 47 uFd
- MGTAVCC, MGTAVTT, MGTVCCAUX One 4.7 uFd per Power Group

The XCVU125-FLVC2104 has a from the GTH & GTY Guides total of 6 Power Groups. Six Power Groups includes both the GTH and GTY. There is the same one 4.7 uFd capacitor requirement for both the GTH and GTY transceivers.

Notes:

- VCCINT and VCCINT_IO must be tied together on PCB.
- VCCAUX and VCCAUX_IO must be tied together on PCB.
- One 47 uFd capacitor is required for up (to) four
- HP/HR Banks when powered from the same VCCO voltage.
- 470 uFd can be used for 680 uFd in a 4 to 3 ratio

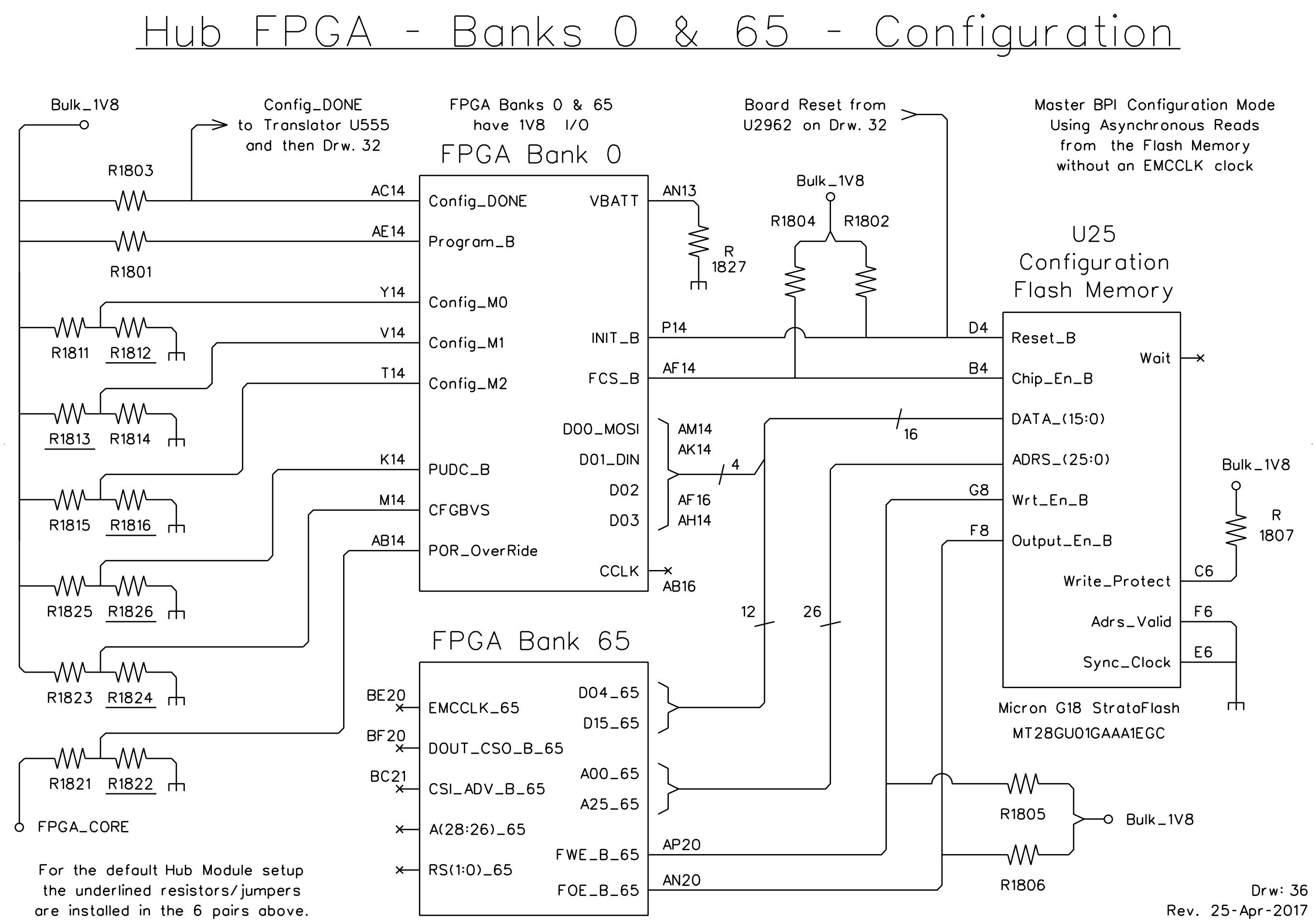

Figure 63: Hub FPGA configuration, banks 0 & 65.

4079

4080

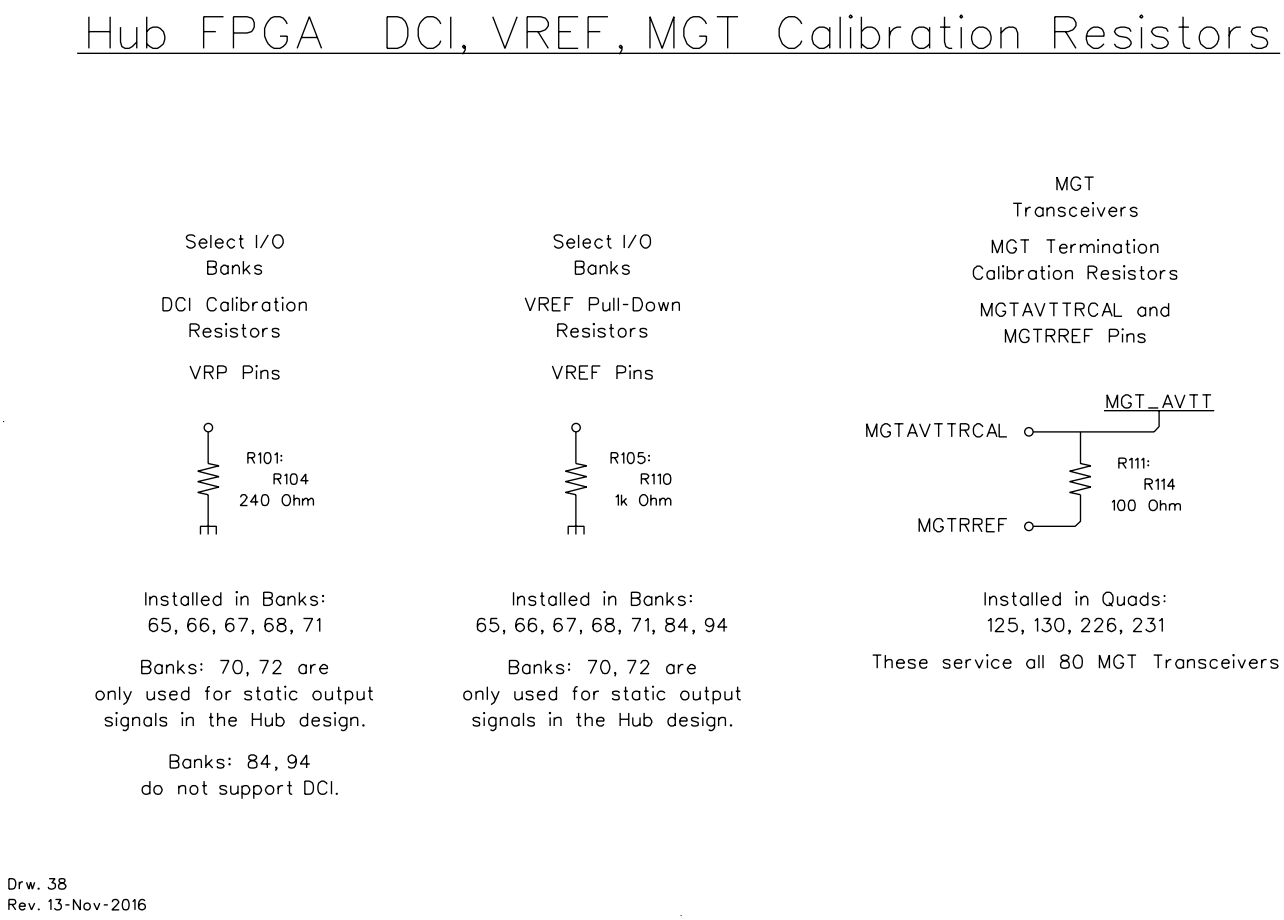

Figure 64: Hub FPGA calibration resistors.

32 Appendix 19: Hub Commissioning Test Plan

External inputs:

- Requirements from ROD, FEX and FELIX interfaces are assumed to be defined by the prior review outcomes and module specifications.
- An engineering definition should be provided for the maximum changes in LHC input reference clock (eg, "We must be able to track a slew rate of 220 Hz/sec while our recovered clock does not shift in phase by more than 30 degrees from its normal position with respect to a static center frequency reference input.")

Definitions:

- "This Hub" / "Other Hub"
  - Hub modules do not have a physical difference of whether they are in logical slot 1 or logical slot 2. The only difference is that the Hub in slot 1 transmits the master clock to the FEX, ROD and slot-2 Hub modules.
  - Thus, each Hub can view the world from its own internal reference point and must be able to achieve satisfactory operation from both logical slots.
  - "This Hub" corresponds to a Hub module in a reference slot (eg, Slot 1)
  - "Other Hub" thus corresponds to the Hub in the implied alternate slot relative to "This Hub" (eg, Slot 2 relative to Slot 1 and vice versa)
- Combined Data
  - The Hub module receives TTC information from FELIX and extracts the clock and configuration data. It then combines local control signals from the ROD(s) present and distributions this Combined Data to all modules in the ATCA shelf.
- GbE = Gigabit Ethernet

32.1 Power Supplies and Hub Component Cooling Tests

1. During MSU Final Assembly and Bench Testing
   a. Verify (measure) 11 power supply output voltages and 7 power supply output currents while the FPGA is configured with test firmware.
   b. The 7 DCDC Converters on each Hub are tested and setup for: Vin_On, Vin_Off, Vout_Margin_High, Vout_Margin_Low, and Vout_Scale_Loop.
2. Verify that the I2C PMBus monitoring of the 7 DCDC Converter output voltages and currents is working OK by reading them from the Front Panel I2C Bus connector. The intent is to verify that the IPMC has access to this data.
3. Verify that the FPGA's System Monitor reads out correct data for the Si Temperature, 1V8 Aux power, and 0V95 Core power.
4. Verify the sequencing and ramp rate for at least two of the power supply voltages, e.g. DC/DC-1 FPGA_Core, DC/DC-5 SWCH_1V2, and DC/DC-8 Bulk_3V3.
5. Verify that the board power enable circuit, the board start-up reset circuit and the two front panel board power status LEDs are all working correctly.
6. Verify the expected Hub FPGA Si Temperature with the Hub running in the Shelf with standard air flow rate and the highest wattage FPGA firmware that we have available (currently about 32 Watts).

7. Verify that the expected operating temperature is readout from the two MiniPODs via their control/monitoring serial bus connection to the Hub FPGA.

32.2 IPMC and Slow Control & Monitoring Bus Tests

1. Verify that the IPMC can negotiate via the IPMB Buses with the Shelf Manager and turn On or Off the Hub card appropriately.
2. Verify that the IPMC can detect the front panel handle switch position and correctly follow the protocol to turn the Hob module power On and Off.
3. Verify that the IPMC can correctly read the Slot Address from the backplane pins for both Hub Slots.
4. Verify that the IPMC can correctly get the Crate Address from the Shelf Manager and make this address data available on the IPMC's general purpose I/O pins.
5. Verify that the IPMC can correctly gather the Hub's voltage, current, and temperature Monitoring Data by initiating the required cycles on the Sensor I2C Bus and that it can forward this Monitoring Data to the Shelf Manager where it is made available to the DCS system.
6. Verify that by one of its general purpose I/O pins the IPMC can be told to suspend its Reads of Monitoring Data over the Sensor I2C Bus and then later to resume its normal reads of the Hub Monitoring Data.
7. Verify that the IPMC can correctly read FRU and SDR data from the PROM on the Hub card via the Management I2C bus so that a generic Hub type L1Calo IPMC can be used on any Hub card.
8. Verify that the IPMC can correctly read the Monitoring Data from the Hub's ATCA Power Entry Module via the Management I2C Bus.
9. Verify that the three I2C buffers in the overall Sensor I2C Bus are working and be enabled or disabled via their control lines that run to the Hub's FPGA.
10. Verify that the Front Panel JTAG connector has access to the Hub's FPGA and that when the ROD is installed and powered up that the ROD's FPGA also appears in this JTAG string.
11. Verify that the two MiniPOD serial control & monitoring I/O buses are working and communicating with the Hub's FPGA.

32.3 MGT Link Tests

1. Verify that the 13 Equalization Group Enable Signals are all working OK and routed to the correct sets of MGT Fanout Chips.
2. Verify that the 4 MiniPOD Receiver MGT channels and the 8 MiniPOD Transmitter MGT channels are all working OK.
3. Verify that the Hub FPGA can receive 6 lanes of MGT data from all 12 of the FEX slots.
4. Verify that the Hub can receiver 6 lanes of MGT data from all 12 of the FEX slots and correctly pass this data to the ROD.
5. Verify that the Hub FPGA can send out Combined Data to the 12 FEX slots, to the ROD on This Hub, and to the Other Hub.
6. Verify that This Hub can Receive Combined Data that was sent out by the Other Hub.
7. Verify that This Hub can Receive the Readout Control data that was sent out by the ROD on This Hub.
8. Verify that This Hub can send out two lanes of Readout data to the Other Hub.
9. Verify that This Hub can Receive two lanes of Readout data from the Other Hub.

10. Verify that This Hub can Receive and correctly pass to its ROD one lane of readout data from the Other Hub.
11. Verify that the FPGA on This Hub can send one lane of its readout data to the ROD on This Hub.

32.4 Clock Tests

1. Verify that the 25.0 MHz and 40.0787 MHz oscillators are running at the correct frequency and are stable.
2. Verify the 40.0787 and 320.6296 MHz PLLs have the correct LHC frequency tracking range.
3. Verify both sides of the First 40 MHz Fanout to the: Hub FPGA, ROD, 320 MHz PLL, and Second 40 MHz Fanout.
4. Verify both sides of the 13 outputs from the Second 40 MHz Fanout: 12 to the FEXs and 1 to Other Hub.
5. Verify both sides of the outputs from the 320 MHz Fanout: 8 connections to MGT Reference Inputs and 1 Logic Clock to the Hub FPGA.
6. Verify that when operated as the Other Hub (i.e. the Hub that does not directly receive an optical TTC signal from FELIX), that the Hub card can correctly receive its LHC Reference Clock from the backplane.

32.5 Ethernet Connection and Ethernet Switch Tests

1. Verify that both GbE links to the Hub's FPGA are working correctly (link to the GbE Switch on This Hub and link via the backplane Base Interface to the GbE Switch on the Other Hub).
2. Verify that all 22 GbE Switch Ports that are used on the Hub card carry GbE traffic OK.
3. Verify that the Hub's Front Panel GbE connection and GbE Magnetics for the ROD are all working OK.
4. Verify that the Hub's Front Panel GbE connection and GbE Magnetics for the IPMC are all working OK.
5. Verify that the current GbE Switch PROM content is OK and Final and start installing GbE Switch PROMs with this content on all Hub Modules.
6. Characterize the performance of the GbE Switch, i.e. test in isolation the data flow rate to each of the Switch's 18 external ports and test the switch when all 18 of its external ports are trying to flow data at the same time.

32.6 Miscellaneous Tests

1. Verify that all 66 Front Panel LEDs are working and are of the correct color.
2. Verify the Physical aspects of this Hub card:
    a. Dimensions look correct (e.g. none of the brackets are in backwards).
    b. The board's corners are in good shape.
    c. The Insertion and Extraction forces feel correct and are smooth.
    d. The Front Panel Labels are clear and not scratched.
    e. All of the backplane connectors line up in a straight row and are fully inserted.
    f. Nothing is loose or likely to vibrate in the air flow (e.g. the discrete power wires or fiber optic ribbons, or power supply LC filter comps).
    g. MiniPOD and FPGA heat sinks are correctly installed.

4214 h. The MiniPODs are fully seated and screwed down.
4215 i. The MiniPOD Fiber Optic Ribbon Cables are correctly routed and not
4216 blocking air flow.
4217 3. Verify that all 9 ESD ground points are correctly connected so that the card is safe to
4218 handle.
4219 4. Verify that the card auto-configures its FPGA from its Flash memory at power up.
4220 5. Verify that the ROD can control the open collector output signals from the Hub's
4221 Front Panel LEMO Connector.
4222 6. Verify the correct operation of the 4 Power Control signals and the 8 Spare TBD
4223 signals between the Hub and ROD cards.
4224 7. Verify the correct fuses are installed.
4225 8. Verify that both Front Panel FPGA output Access Signals are working OK.