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Published in:
IEEE Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2021.3074986

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

On the Equilibrium Points in Three-Phase PLL Based on d-axis Voltage Normalization

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***Abstract*— Voltage normalization is usually adopted for a phase-locked loop (PLL) to keep a constant bandwidth unaffected from the voltage magnitude at the point of synchronization. Two conventional PLL normalization methods are analyzed from a large-signal perspective in this letter. However, different from the voltage magnitude normalization method, an unexpected stable equilibrium point emerges in the three-phase PLL based on d-axis voltage normalization, the mechanism of which is revealed by the phase-plane analysis. Due to the unexpected equilibrium point, the d-axis voltage normalization will lose the phase tracking ability when the initial phase difference or phase jump exceeds π/2. Thus, it is suggested to use the magnitude normalization instead of the d-axis voltage normalization to avoid this kind of malfunction. Finally, the experimental results validate the theoretical analysis.**

***Index Terms*—Phase-locked loop (PLL), voltage normalization, equilibrium point, large-signal analysis.**

I. Introduction

Over the past decades, converter-based renewable power generation has been widely integrated into the power grids [1]. The basic requirement of these installed renewable power generations is to achieve precise power control. The accurate and stable power control of the converter is highly dependent on the synchronization block, which is applied for acquiring the grid voltage angle [2],[3]. Among all synchronization blocks, the phase-locked loop (PLL) is the most commonly used synchronization method for the power converter. Thus, it is of significant importance to study the performance of PLL.

There are a lot of research works about the PLL studies [4]-[15]. The main objective of the PLL is to track the grid voltage angle quickly and accurately [4]-[6]. From this perspective, the bandwidth of PLL should be designed high enough to maintain a good dynamic performance of phase tracking. However, under weak-grid conditions, a high bandwidth will cause instability since the PLL will introduce a negative resistance behavior to the current control [7]. Thus, between the fast phase tracking and the stability requirement, the bandwidth of the PLL should be designed carefully to make a compromise between these two performances.

In order to have a unified bandwidth design method for PLL under different voltage levels, voltage normalization is usually applied to eliminate the effect of voltage magnitude on the PLL dynamics. To this end, an amplitude normalization scheme is often included in the PLL structure to keep the dynamic and stability characteristics of the PLL decoupled from variations of voltage. Straightforwardly, the voltage normalization can be achieved by simply dividing voltage magnitude (DVM) in the stationary frame [8]. Furthermore, directly dividing *d*-axis voltage (DDV) can also be used for the voltage normalization [6],[9],[14]. In [10]-[12], an alternative approach for amplitude normalization is using the inverse tangent operation, which reduces the nonlinearity of the PLL control loop at the cost of a higher computational effort. All these methods can achieve voltage normalization to keep a constant bandwidth. However, only the small-signal response is analyzed in the prior-art research without considering the large-signal performance. In [13], an adaptive PLL structure is proposed for fast and smooth tracking of phase-angle jumps. Furthermore, the magnitude is also used for the voltage normalization in the single-phase enhanced PLL (EPLL) [14]. Even though another stable equilibrium point is shown by the phase portraits, the intrinsic reason is not revealed and a comprehensive comparison between different normalization methods is absent. Namely, what is the dynamic response difference between different normalized PLLs when there is an initial phase angle difference or a sudden phase jump? This question will be answered in this letter.

In this letter, the non-linear mathematical models of the two widely used normalized PLLs are built for a comprehensive comparison from a large-signal perspective. Surprisingly, it is discovered that the widely used d-axis voltage normalization method will have an unexpected equilibrium point, which may cause a wrong tracking phase angle. Thus, using the voltage magnitude division instead of the d-axis voltage division for the voltage normalization to avoid the unexpected wrong equilibrium point is highly suggested. Finally, the experimental results are conducted to verify the theoretical analysis.

II. Mathematical models of normalized PLLs

The topology of the grid-connected converter is illustrated in Fig. 1. $\boldsymbol{U}_{gabc}$ represents the three-phase grid voltage, $\boldsymbol{I}_{gabc}$

Manuscript received March 3, 2021; revised April 06, 2021; accepted April 19, 2021. This work is supported by THE VELUX FOUNDATIONS under the VILLUM Investigator Grant REPEPS (Award Ref. No.: 00016591) and part by the National Natural Science Foundation of China under Grant 51707065 (*Corresponding author: Xiaoling Xiong*).

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represents the three-phase current injected into the grid, L_{cf} is the converter filter that is applied for suppressing current harmonics, U_{dc} is the dc-link voltage. It should be noted that in practice a grid impedance will add another destabilizing term, which further challenges the system stability [3]. Thus, the grid impedance is not considered since the main focus of this work is to study the phase tracking ability of the normalized PLLs. The block PLL is applied to estimate the angle of grid voltage. In order to maintain a constant bandwidth and damping ratio, voltage normalization methods are always introduced into the PLL block. In this letter, the two commonly used normalized PLL structures are discussed and compared from a large-signal perspective.

The structures of two typical normalized PLLs are shown in Fig. 2. In order to do simplification, the DDV-PLL and DVM-PLL represent the normalization based on DDV and DVM, respectively. The input is the three-phase grid voltage $\boldsymbol{U}_{gabc}$, and the output is the estimated angle of grid voltage, which is denoted as θ_{pll} to distinguish it from the grid voltage angle θ_g. In the steady-state, $\theta_{pll}=\theta_g$. However, during the transient period, such as the initial start-up or phase jump of grid voltage, $\theta_{pll}\neq\theta_g$, and the PLL angle will try to track the grid voltage angle quickly to eliminate the angle error. ω_b is a constant frequency feedforward term, which is 100π rad/s in this paper, ω_{pll} is the PLL angular frequency, $f_{pll}=\omega_{pll}/(2\pi)$ is the PLL frequency. k_p and k_i are the proportional and integral parameters of the PI controller applied in the normalized PLLs.

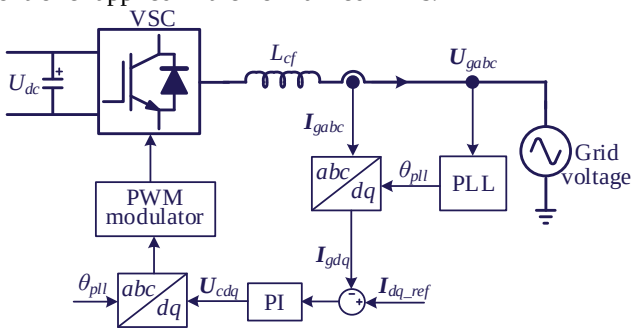
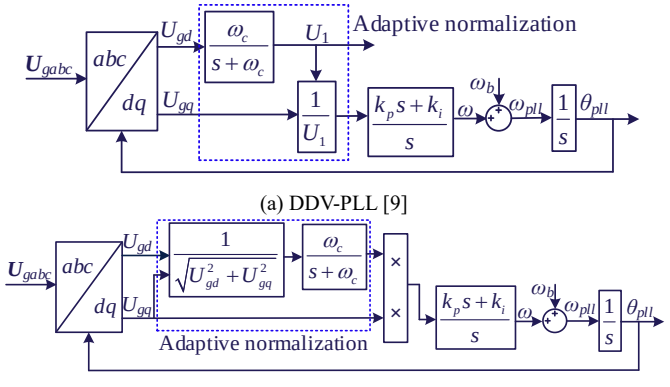


Fig. 1. General topology and control scheme of a three-phase grid-connected converter with the current vector control.



(a) DDV-PLL [9]

(b) DVM-PLL [8]

Fig. 2. Structures of two different normalized PLLs.

It should be noted that the low-pass filter is only employed for eliminating the noise caused by the division part. Thus, the cut-off frequency can be set high enough without affecting the PLL dynamics. In this letter, the bandwidth of PLL is chosen at 30 Hz, and the cut-off frequency of the LPF is set at 300 Hz. To this end, the effect of the LPF can be ignored when analyzing the dynamic performance of PLL.

Without considering the LPF, the *dq*-axes voltages in Fig. 2 can be expressed as,

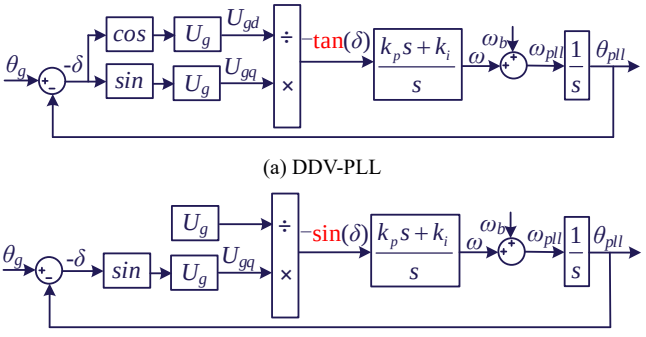
$$\begin{aligned} U_{gd} &= U_g\cos\left(\theta_g-\theta_{pll}\right)=U_g\cos\delta \\ U_{gq} &= U_g\sin\left(\theta_g-\theta_{pll}\right)=-U_g\sin\delta \end{aligned} \tag{1}$$

where U_g is the magnitude of grid voltage, and the angle difference between the PLL angle and grid voltage angle is defined as $\delta=\theta_{pll}-\theta_g$.

Thus, the simplified large-signal model of the two normalized PLL methods can be illustrated in Fig. 3, where the *q*-axis voltage can be seen as an input and the output is the angle difference δ.

According to the large-signal model in Fig. 3, it can be seen that the dynamics of the normalized PLL is a second-order nonlinear system, δ and ω are chosen as the state variables. Consequently, the state-space model of the DDV-PLL in Fig. 3(a) can be expressed as,

$$\begin{cases} \dot{\delta}=\left(\omega+\omega_b-\omega_g\right) \\ \dot{\omega}=\dfrac{-\dot{\delta}k_p}{\left(\cos\delta\right)^2}-k_i\tan\delta \end{cases} \tag{2}$$



(a) DDV-PLL

(b) DVM-PLL

Fig. 3. Simplified large-signal model of the two normalized PLLs in Fig. 2.

The state-space model of the DVM-PLL in Fig. 3(b) can be derived as,

$$\begin{cases} \dot{\delta}=\left(\omega+\omega_b-\omega_g\right) \\ \dot{\omega}=-\dot{\delta}k_p\cos\delta-k_i\sin\delta \end{cases} \tag{3}$$

As can be shown from (2) and (3), the second-order differential equations are different with different normalization schemes. In order to make a more intuitive comparison between the two normalization methods, the large-signal analysis based on phase-plane analysis is conducted in the next section.

III. Large Signal Analysis of Normalized PLLs

A. *Phase-plane analysis*

In order to analyze the large-signal stability performance, the phase-plane analysis method is used. It is well known that the

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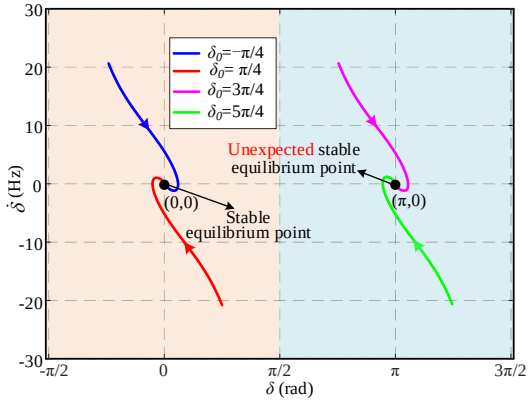
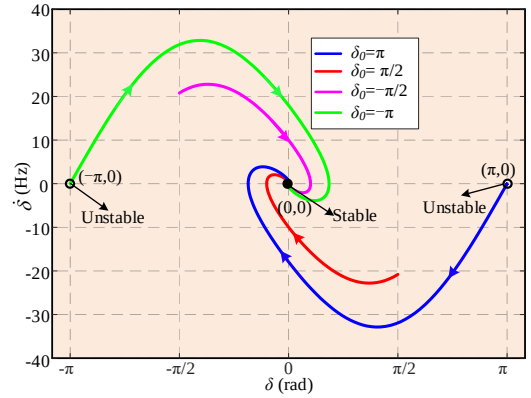
initial angle difference between the grid voltage angle and the PLL angle can be any angle in the range [-π/2, 3π/2] or [-π, π]. A phase jump can be seen as the same disturbance type as an initial angle difference. Thus, only the initial angle difference is mentioned in the following analysis. To guarantee the phase tracking ability of normalized PLL, the angle δ should come back to zero under any kind of initial angle difference. In this way, to check the angle tracking ability of the normalized PLLs, the phase portraits of the two different normalization methods with different initial angle differences are plotted in Fig. 4. It should be noted that $\dot{\delta}$ is chosen as the y-axis in Fig.4 but not the angular frequency ω. Thus, the phase portrait in Fig.4 is also correct when considering the grid frequency deviations.



(a) Phase portrait of DDV-PLL.



(b) Phase portrait of DVM-PLL

Fig. 4. Phase portraits of two normalized PLLs with different initial angle differences.

Fig. 4(a) shows the phase portrait of DDV-PLL with different initial states. Four different initial angle differences δ_0 are checked based on the differential equations in (2). From Fig. 4(a), when the initial angle differences are between [-π/2, π/2], such as -π/4 and π/4, the angle difference δ can converge to 0 in the steady-state, which means that the PLL works normally under these conditions. However, when the initial angle differences are between [π/2, 3π/2], such as 3π/4 and 5π/4, the angle difference δ will converge to π in the steady-state, which means there is a large steady-state error between the grid voltage angle and the PLL angle. Under these conditions, the DDV-PLL will lose the phase tracking ability. It should be kept in mind that the objective of PLL is to track the angle without steady-state error. What we anticipate for PLL is that the output angle can always be equal to the grid voltage angle no matter what kind of phase jump happens. However, as we can see, the steady-state angle error will be 180 degrees when the phase jumps larger than 90 degrees, this is not acceptable in the real case. Thus, this stable equilibrium point is called "unexpected". The steady-state angle error π could cause that the power flow direction of the converter will be reversed which can cause instability or damages to the dc-link. This should be avoided in real applications.

Fig. 4(b) shows the phase portrait of DVM-PLL with different initial angle differences. Four different initial angle differences δ_0 are checked based on the differential equations (4). The maximum initial angle differences are π and -π. As can be seen from Fig. 4(b), the angle δ can always come back to 0 no matter which initial angle is, which proves that this kind of normalized PLL can always track the grid voltage angle under any kind of phase jumps. Thus, the DVM-PLL has a more robust response to the variations of the grid voltage phase jumps, which is preferably recommended for real applications.

B. *Mechanism analysis*

From the above, it is desirable to answer the following questions: Why is there a significant difference between the two normalization methods, and how can this phenomenon be explained? The answers to those will be detailed in the following.

As can be seen from Fig. 4, the main difference between these two normalized PLLs is the stable equilibrium point difference. For the DVM-PLL, there is only one stable equilibrium point during 2π range. However, for the DDV-PLL, there are two equilibrium points during 2π range, which is the main reason that causes the malfunction of PLL during large initial angle difference.

To identify which operating point is stable or unstable, the simplest way is to check the slope of the equilibrium points. Based on (2) and (4), setting the differential terms in (2) and (4) to be zero, the equilibrium points can be obtained. From (2), the equilibrium point is dependent on the tangent function while the equilibrium point is dependent on the sine function in (4). Thus, the waveforms of sine and tangent function in the 2π range are plotted in Fig. 5. It can be seen the two normalized PLLs both have two equilibrium points 0 and π.

However, for the sine function in Fig. 5(a), the slope of the equilibrium point at π is negative, which means this equilibrium point is unstable. From Fig. 5(b), it is easy to find that both the two equilibrium points are stable for the tangent function. Thus, when the phase angle jumps more than π/2 from the zero point, the angle difference will converge to another equilibrium point π. Even though the PLL can operate stably at this equilibrium point, the angle acquired from the PLL is not the same as the grid voltage angle, which has a steady-state error π. To this end, the phase detector changing from sine function to tangent function is the fundamental reason that causes this unexpected stable equilibrium point in DDV-PLL.

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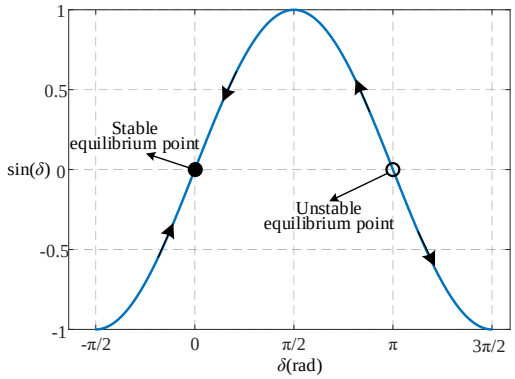
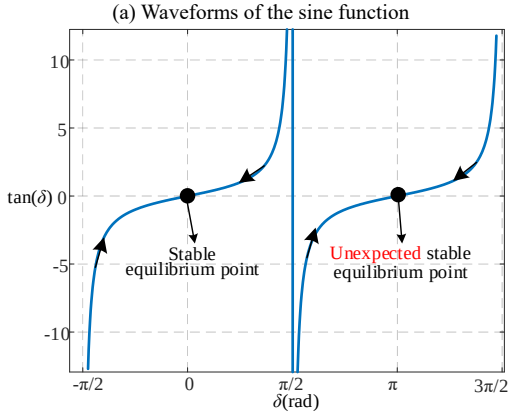


(a) Waveforms of the sine function



(b) Waveforms of the tangent function

Fig. 5. The waveforms of sine and tangent function in 2π range.

IV. Experimental Validation

To verify the theoretical analysis, the experiments for the two normalized PLLs are carried out in the lab. A 45kVA Chroma 61845 grid simulator is used for generating the three-phase grid voltage, the DS2400 A/D board is used to sample the grid voltage, which is then sent to the dSpace DS1007 where the control strategy is implemented. The DS2102 D/A board is used to output the frequency and angle of PLL, which is acquired by the Scope to display the waveforms. The peak value of the phase voltage is 325 V and the grid frequency is 50 Hz. The cut-off frequency ω_c is chosen as 1885 rad/s, k_p is 130 and k_i is 7750, which are large due to the normalization.

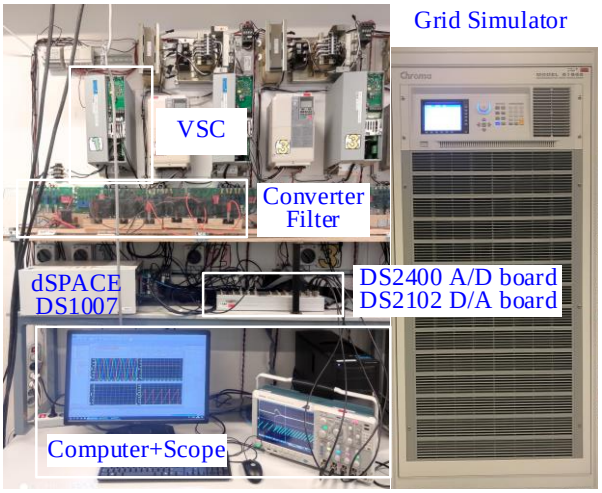


Fig. 6. Laboratory setup for the experimental verification.

Fig. 7 shows the experimental results when the phase jump is π/3. When the phase jump occurs, the frequency will have a sudden jump. However, the frequency deviation of the DDV-PLL is higher than the DVM-PLL because the tangent function is larger than the sine function when the angle is large. However, both the two normalized PLLs can track the grid voltage angle since the angle δ can come back to zero in the steady-state and the two PLL angles are completely coincident. Since the angle of the grid voltage and the normalized PLLs are both sawtooth waveforms changing from 0 to 2π, the phase error is not ideally 0 but jumping from 0 to 2π due to the digital controller. Thus, the phase error is not shown in the experimental results but directly showing the frequency and angle, which are more clear to show the dynamic process during phase jumps.

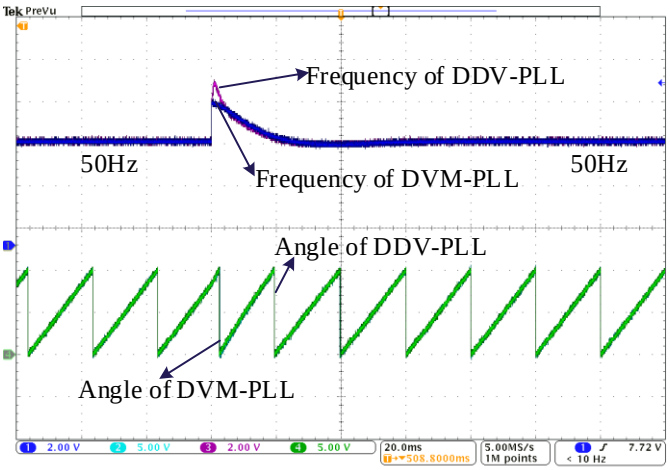


Fig. 7. Experimental results of normalized PLLs during sudden phase jump π/3.

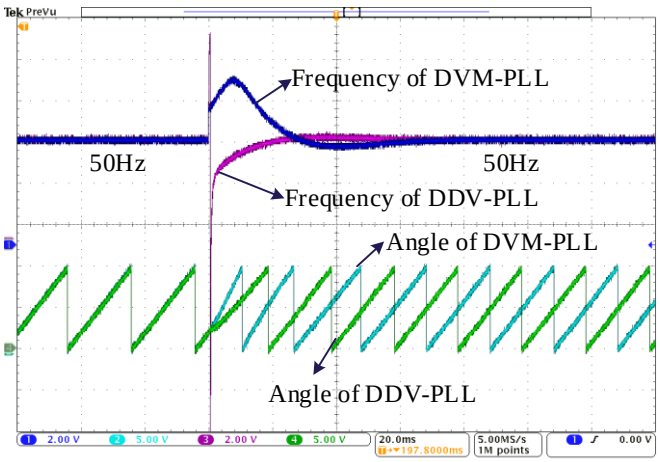


Fig. 8. Experimental results of normalized PLLs during sudden phase jump 3π/4.

Fig. 8. shows the experimental results when the phase jump is 2π/3. Due to the sudden phase change exceeds pi/2, the d-axis voltage will be negative and will cause the angle δ to converge to –π. In this way, the DDV-PLL will lose the phase tracking ability but the DVM-PLL can still be capable of tracking the phase even when the phase jump is so large. Thus, there will be a constant angle error π between the angle of DDV-PLL and DVM-PLL. These experimental results agree well with the theoretical analysis with the phase portraits depicted in Fig. 4, which further confirms the correctness of the theoretical

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findings.

In order to validate the unexpected equilibrium point also exists in other improved PLL structures, the experimental results of DDV-PLL with dq-frame delayed signal cancellation (dqDSC) under phase jump 5π/6 are shown in Fig. 9. The dqDSC block is added in the PLL for eliminating the negative effect of the dc offset and odd harmonics [15]. Since the dqDSC-PLL is still directly using the d-axis voltage for normalization, it will cause a steady phase error during a large phase jump. Thus, the conclusion obtained from the simple DDV-PLL structure shown in Fig. 2(a) is applicable for any other kinds of improved PLL structures, which are using the *d*-axis voltage for normalization without any correction to the output angle.

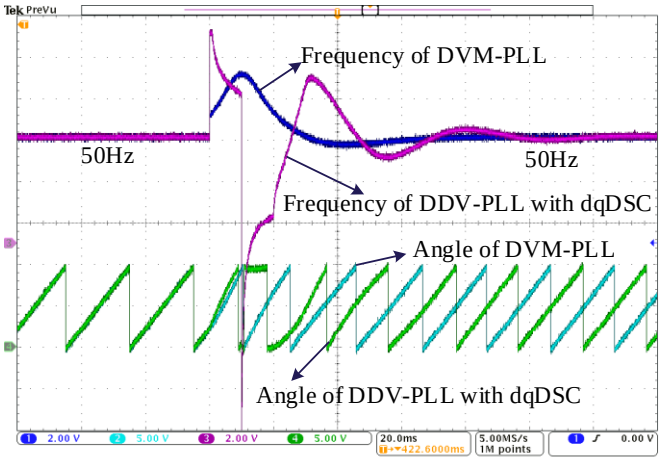

Fig. 9. Experimental results of normalized PLLs during sudden phase jump 5π/6.

V. Conclusion

In this letter, the detailed non-linear mathematical models of two widely used normalized PLLs are built for performance comparison from a large-signal perspective. It is revealed that there is an unexpected stable equilibrium point in the DDV-PLL, resulting in tracking problems when the initial angle difference or phase jump exceeds π/2. The root cause is that dividing d-axis voltage causes the phase detector to be a tangent function instead of a sinusoid function. Finally, the experimental results verified these important findings, and it is highly recommended to use the voltage magnitude instead of the *d*-axis voltage for normalization in the PLL. It should be noted that the conclusion can also be extended to single-phase PLLs. When the phase detector is mathematically equivalent to the tangent function, one should always be careful and recognize that an unexpected stable equilibrium point (π, 0) exists.

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