Anritsu

envision : ensure

Signal Quality Analyzer-R

32G/64G NRZ/PAM4 Signal Integrity Test Solution*

MP1900A

SQA-R

*: Refer to the MP1900A PCIe/USB/Thunderbolt Test Solution Catalog (MP1900A-E-A-1) for the information on MP1900A high-speed-bus test solution.

Excellent Eco Product

One Box over 400G Testing

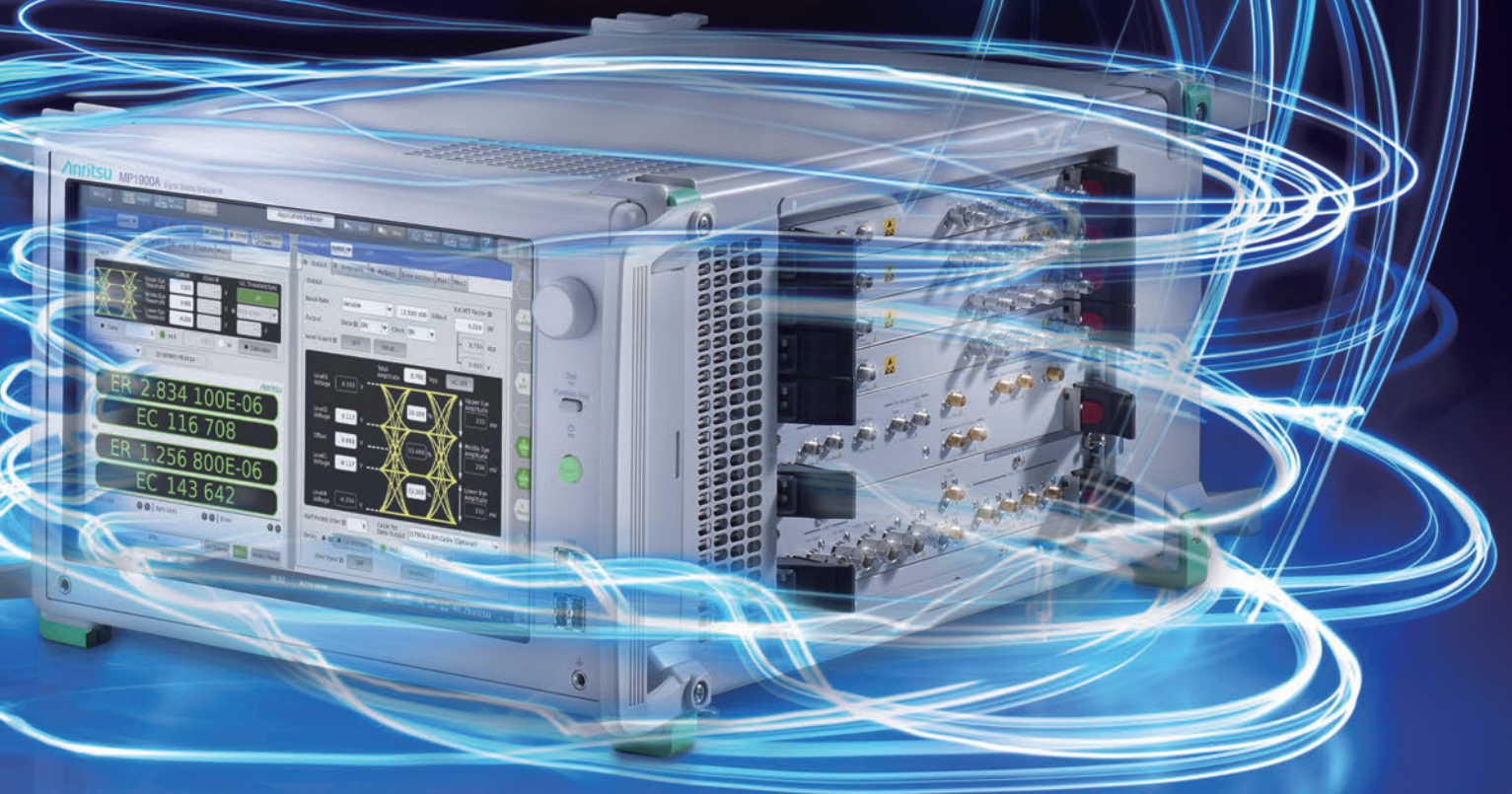## MP1900A

Signal Quality Analyzer-R

SQA-R

Automation Function PCIe Gen1-5

Data center and network traffic volumes are increasing exponentially as mobile networks start upgrading to 5G and 'Big Data' applications become popular. As a consequence, physical-layer devices are required to support faster transmission speeds, larger data capacities, and assured signal quality, in turn making signal integrity analysis ever more important. To meet these needs, Anritsu has implemented more accurate signal integrity tests, such as bit error rate (BER) measurements, crosstalk tests, Jitter Tolerance tests, etc., in its MP1900A test solution for 64 Gbaud NRZ/PAM4.

All-in-One Futureproof Measurements

The Signal Quality Analyzer-R MP1900A series is a modular 8-slot high-performance BERT. Installing multiple modules in the slots not only supports today's 400 GbE analysis requirements, but also provides futureproof support for next-generation 800G measurements.

World-Leading Highest Level Waveform Output Quality Resulting from Fast Tr/Tf and Low Intrinsic Jitter.

MP1900A PAM4 Output Waveform (53.125 Gbaud, PRBS15, Differential 1400 mV)
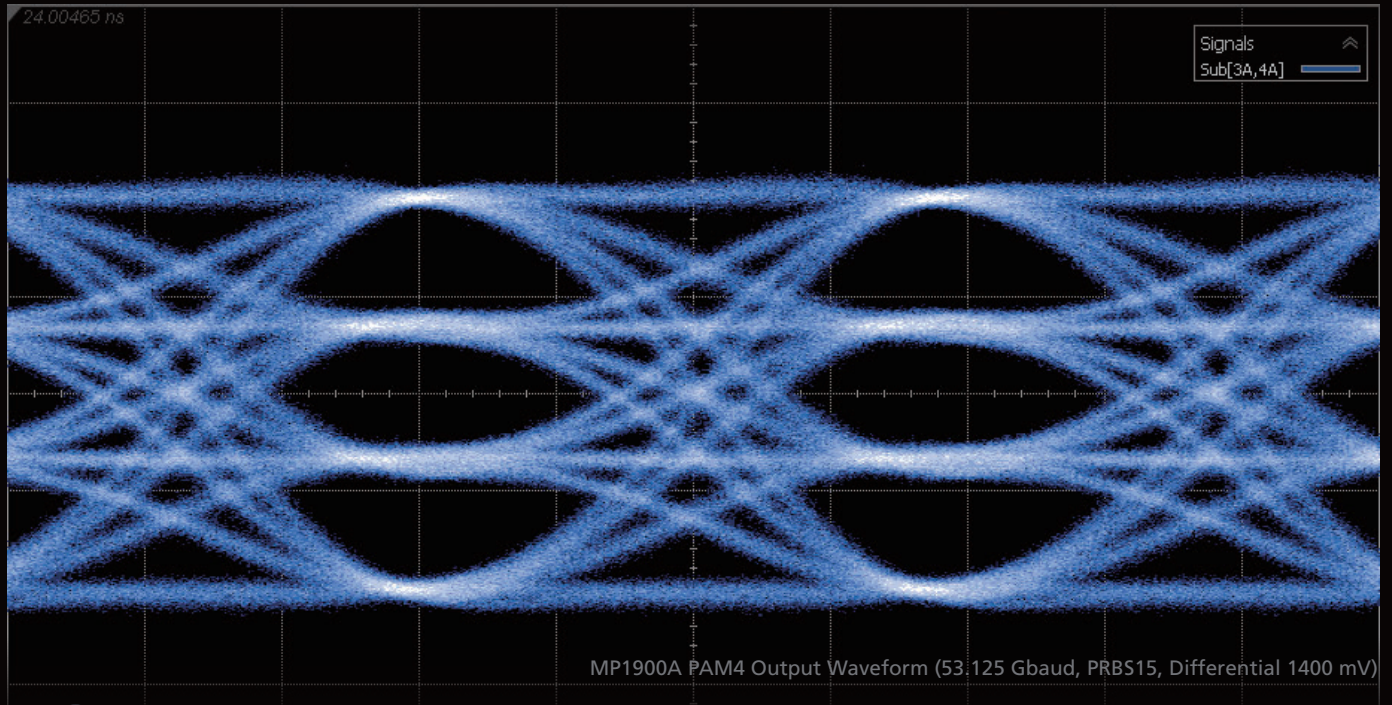
One Box over
400G Testing

MP1900A
Signal Quality Analyzer-R

SQA-R

Multichannel Signal Integrity Evaluation

Beyond 400 GbE Expectations

High-Quality Waveforms, and High-Sensitivity Input

Higher Measurement Efficiency Supported by Industry-beating Signal Quality, High Sensitivity, And Wide Bandwidth

- High-speed Tr/Tf of 8.5 ps (20 to 80%)
- Low Intrinsic Jitter of 170 fs (rms)
- Low noise and low distortion high-quality data output
- 116-Gbit/s PAM4 error-free measurements using high-sensitivity and wideband Rx performance

High Transmission Capacity and Excellent Expandability

Futureproof Multichannel Expansion for 800G R&D

- All-in-one support for 512 Gbit/s max. transmission capacity
- Multichannel expandability 4ch PAM4/NRZ
- 8 slots for module addition
- Jitter and noise module expandability
- Operation baud rates of 2.4 Gbaud to 64.2 Gbaud

World-First All-in-One PAM4 BER Test Solution

Easy-to-Setup and Operate All-in-One PAM4 Bit Error/FEC Symbol Error Measurement System

- Supports Emphasis variable dynamic range (±20 dB) and ISI simulation
- 4-level linearity control
- Built -in Clock Recovery, Equalizer
- Jitter Tolerance Test, Bathtub Jitter Analysis
- PAM4 Pattern Editor, Symbol Error Measurement
- Real-time FEC Symbol Error and FEC Based Jitter Tolerance Measurements
- FEC Pattern Generation, Error Analysis using FEC Symbol Capture Function
- Jitter Tolerance measurement using DUT BER counter function
- Automatic Margin measurement using Eye contour
- Automatic pattern mismatch detection and optimum Equalizing using Auto Search
- PCIe 1.0 to 5.0 Link training plus BER and JTOL measurements for future PCIe 6.0

| Target Standards	Target DUT
— Ethernet , 800/400/200/100/50 GbE	— Optical module (QSFP-DD, OSPF, CFP8, SFP56)
— CEI-56G, CEI-112G	— TOSA, ROSA, SERDES
— InfiniBand-HDR	— Active Optical Cable (AOC)
— 64G Fibre Channel	— PCI-Express Device, System
— PCI-Express 1.0 to 5.0	

High-Quality Waveforms PAM4 PPG

High-Quality Data Output with High-Speed Tr/Tf and Low Intrinsic Jitter

The PAM4 PPG MU196020A supports high-quality data output with low noise and low distortion over high analog band with Tr/Tf of 8.5 ms and Intrinsic Jitter of 170 fs rms. High-reproducibility measurement supported by PAM4 signals with open 3-Eye waveform. Additionally, Emphasis and Linearity control functions optimize PAM4 data output to DUT.
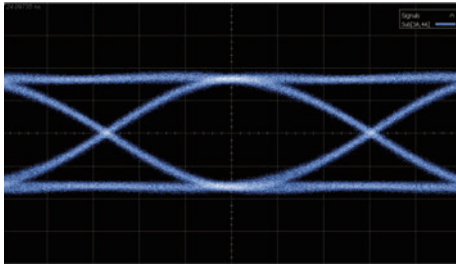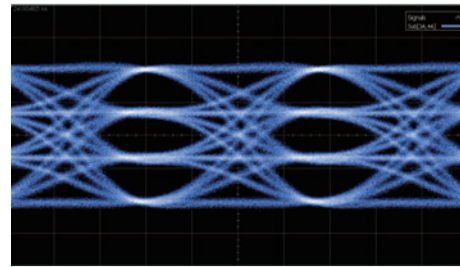
53.125 Gbaud PAM4
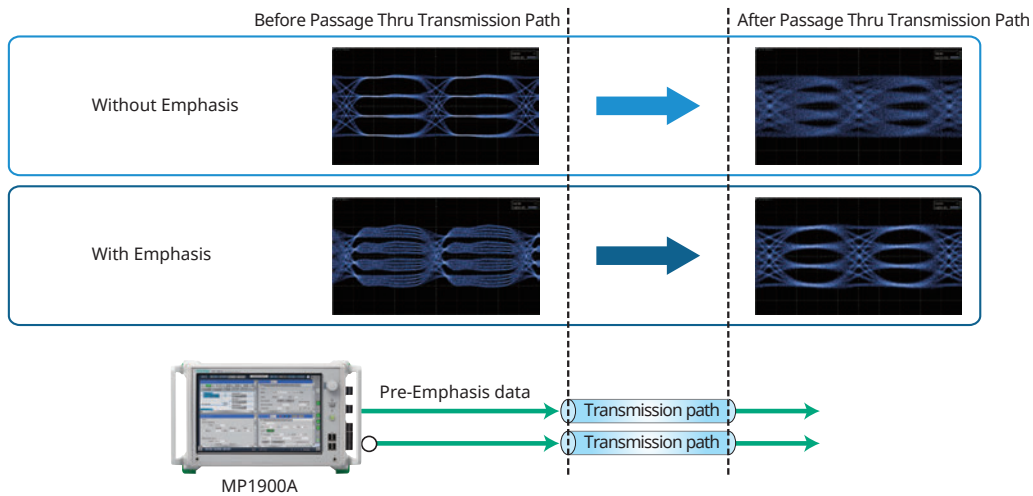

58 Gbaud NRZ
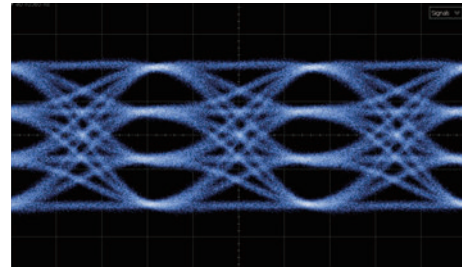
58 Gbaud PAM4

**Typical Output Waveform (J1789A 40 cm Cable, 1400 mV Differential, PRBS15)**

4Tap Emphasis Output at 20 dB max.

The 4Tap Emphasis function (MU196020A-011) can generate the Pre-Emphasis and De-Emphasis signals required by each standard for maximum rates of 64.2G. Since each tap can be changed independently up to 20 dB, corrected waveforms for various transmission paths can be output with good reproducibility.

Before Passage Thru Transmission Path | After Passage Thru Transmission Path

Without Emphasis

With Emphasis

Pre-Emphasis data — Transmission path

MP1900A

Pre-Emphasis/De-Emphasis Optimization Effects

In addition, using the Channel Emulator and ISI functions* makes it easy to output waveforms with simulated channel loss for high-speed devices, as well as waveforms corrected for loss. As a result, not only is testing of multiple channel boards unnecessary, but also high-reproducibility channel-loss-dependent tests of high-speed device performance are easy, helping shorten development times.

Channel Emulator and ISI Functions

S_{21}

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Emulates Channel Loss
or generates Loss calibration signal (MU196020A-040)
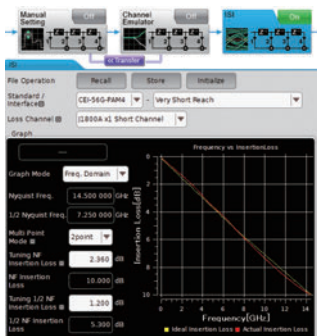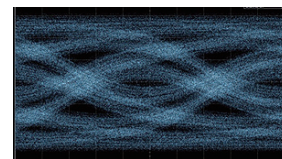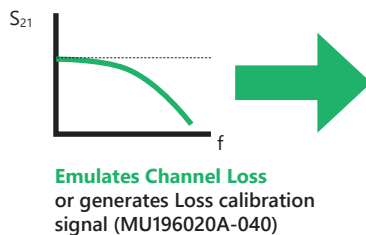
NRZ CEI-28G 14 dB loss
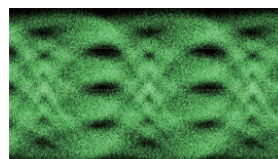
PAM4 26.6G 4 dB loss

PAM4 26.6G 6 dB loss

ISI Function Typical Waveform

High-Quality Waveforms PAM4 PPG

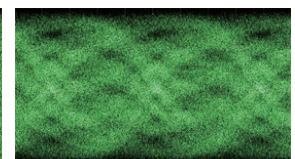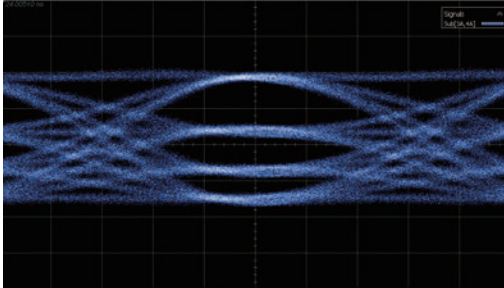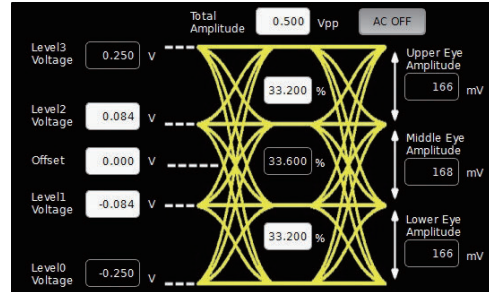## Freely Control PAM4 Output Linearity

The PAM4 PPG can freely control the PAM4 output linearity to change the output level for each Eye independently.
As well as correcting the output waveform of non-linear devices, a PAM4 waveform with variable RLM (Ratio of Level Mismatch) can be output with good reproducibility.


Waveform with Controlled Linearity

PAM4 Output Setting

PAM4 Pattern Editor

PAM4 evaluation test patterns (SSPRQ, PRBS13Q, PRBS31Q, etc.) are built-in as standard. Versatile pattern output settings, such as MSB/LSB bit inversion, Gray Coder ON/OFF, Precoder ON/OFF, and a Bit Shift function (changes MSB bit phase by ±256 bits) support combined use of various DUT internal error counters and analysis of error occurrence locations.
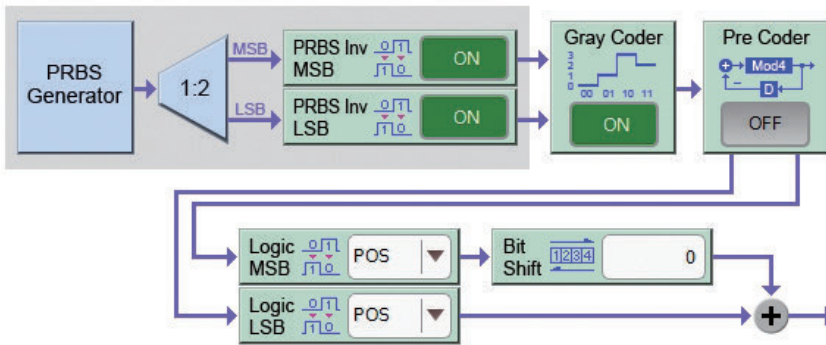
FEC Pattern Generation

The option can be used to generate FEC patterns and add FEC errors (MU196020A-042).
Supported FEC patterns are 400/200/100/25 GbE, and both NRZ and PAM4 FEC patterns can be generated at each lane. Additionally, the FEC error addition function can be used for evaluating the DUT FEC.

PAM4
• RS-FEC Scrambled Idle 50G 1 Lane (26.5625 Gbaud, 50GBASE-KR/CR/SR/FR/LR)
• RS-FEC Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-DR/KR1/CR1)
• RS-FEC-Int Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-P)
• RS-FEC Scrambled Idle 100G 2 Lanes (26.5625 Gbaud, 100GBASE-KR2/CR2/SR2)
• RS-FEC Scrambled Idle 200G 4 Lanes (26.5625 Gbaud, 200GBASE-SR4/DR4/FR4/LR4)
• RS-FEC Scrambled Idle 200G 2 Lanes (53.125 Gbaud, 200GBASE-KR2/CR2)
• RS-FEC Scrambled Idle 400G 4 Lanes (53.125 Gbaud, 400GBASE-DR4/KR4/CR4)
• RS-FEC Scrambled Idle 400G 8 Lanes (26.5625 Gbaud, 400GBASE-FR8/LR8)

NRZ
• RS-FEC Scrambled Idle 25G 1 Lane (25.78125 Gbaud, 25GBASE-KR/CR/SR/LR/ER)
• RS-FEC Scrambled Idle 100G 4 Lanes (25.78125 Gbaud, 100GBASE-KR4/CR4/SR4)

High-Sensitivity, Wideband PAM4 ED

116-Gbit/s PAM4 Signal Error-Free BER Measurement using High Input Sensitivity Function

Combining the PAM4 ED MU196040B with the PAM4 PPG supports BER measurements of 116-Gbit/s (58 Gbaud) PAM4 signals. Error-free BER measurement is achieved by the industry-best high sensitivity performance of 23 mV @26 Gbaud and 36 mV @53 Gbaud. The resulting high-accuracy BER measurements make it easy to troubleshoot previously difficult-to-analyze PAM4 devices. In addition, true DUT performance can be verified because even CEI-112G-VSR-defined worst-case stressed signals can be received at low-error rates (<E-8), exceeding the specifications.
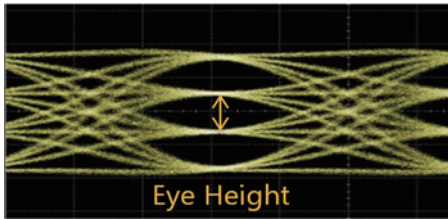
Error-Free Measurement of PAM3 Signals at 23 mV @26 Gbaud, and 36 mV @53Gbaud
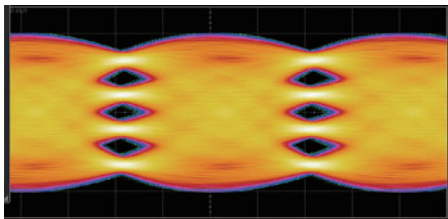
CEI-112G-VSR-defined Worst-Case Stressed PAM4 Signal
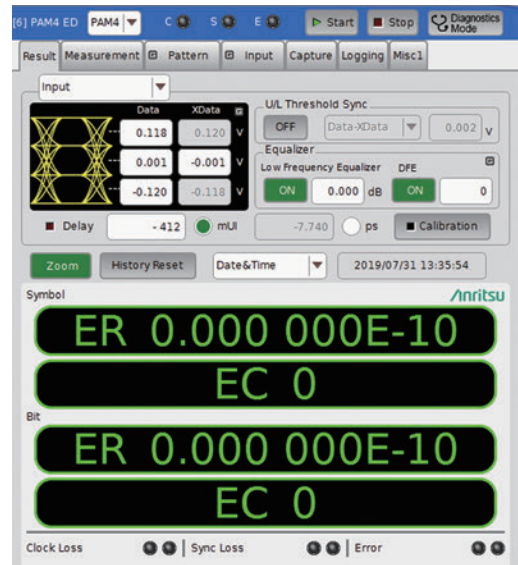
PAM4 BER Measurement Screen

Moreover, even the BER of Eye waveforms closed by ISI can be measured using the built-in Equalizer function.

Eye Waveform Closed by ISI   Low-frequency Equalizer   Decision Feedback Equalizer   BER Measurement
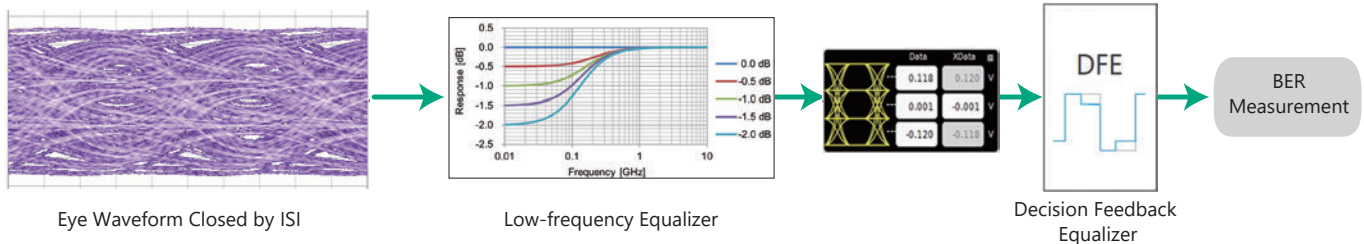
Built-in Equalizer Configuration

Built-in Clock Recovery

An optional Clock Recovery function (MU196040B-021, 022, 023) can be installed in the PAM4 ED, eliminating both the need for an external clock recovery unit, and phase adjustment of the ED Data/Clock. Jitter Tolerance tests of PHY devices, such as QSFP-DD and SERDES with different Tx and Rx signal clocks, as well as BER measurements of AOC device are supported for the ideal, high cost-performance test solution.

Symbol Error Rate (SER) Evaluation

Since the error rate at each symbol (0 to 3) of the PAM4 signal can be confirmed, error occurrence locations can be analyzed in more detail (MU196040B-041).

3

2

1

0

PAM4 Symbol Image

Error Rate Measurement Screen per Symbol Error Level

Auto-Search Function

In addition to the Upper, Middle, and Lower Eye measurement points (voltage threshold value and phase), automatic detection of the optimum Equalizer setting automatically detects the conditions required for the best BER results. Moreover, automatic detection of the PAM4 Symbol Logic and Gray Coding conditions supports automatic evaluation of pattern conditions for the input PAM4 Symbol coding, providing a more efficient measurement environment.

Diagnostics Mode Function
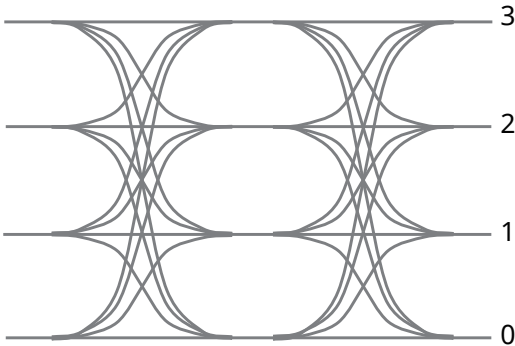
This function is for troubleshooting logic errors, such as inverted logic, and bit skew between the MSB and LSB. When these types of logic errors prevent synchronization, the cause can be specified from the MSB and LSB error results, and from the bit skew detection result.

Capture Function

Input test-pattern data can be captured in blocks of up to 8 Mbits (4 million symbols) for input and analysis of results. The captured test pattern is displayed as lines of symbol patterns with color-coded errors for easy analysis.

Color-Coded Error Capture Screen

Logging Function

Changes in DUT performance and stability over time can be evaluated by saving measurement results, such as ER/EC, periodically.

BER/SER Results Logging Screen

9

High-Sensitivity, Wideband PAM4 ED

Real-time FEC Symbol Error and FEC Based Jitter Tolerance Measurement Functions

Uncorrectable Codeword and FEC Symbol Errors can be measured and displayed on one screen in real-time simultaneously with bit error measurements. Measurement of jitter tolerance and FEC Symbol Error per codeword distribution based on correctable/uncorrectable FEC is supported (MU196040B-042). Both bit error and FEC Symbol Errors are measured at high speed.
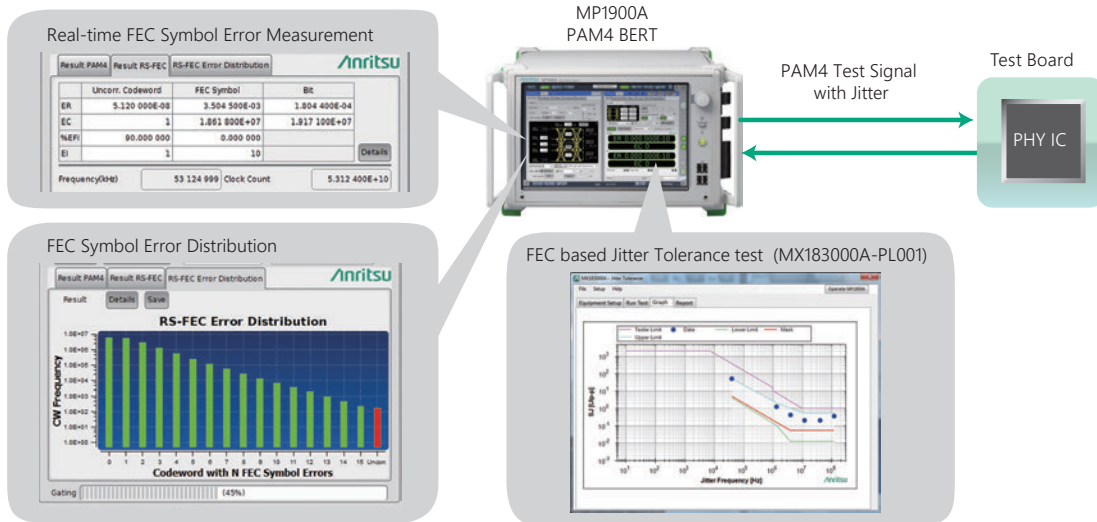
FEC Symbol Capture Function

The input data is captured when the number of FEC symbol errors exceeds the threshold setting based on the 400 GbE-defined FEC symbols and Codeword length. The causes of FEC-uncorrectable errors can be analyzed from the captured data (MU196040B-041).
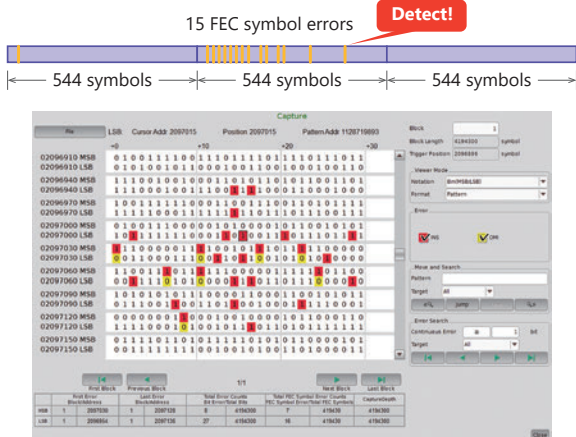
Capturing Detected FEC Symbols Errors

Eye Contour

The input signal Eye opening is measured at high speed based on the Bathtub estimate.
In addition to NRZ, the PAM4 Symbol Upper, Middle, and Lower Eye openings are measured, supporting more accurate evaluation of Eye Margin characteristics at BER estimates up to E-20.

PAM4 Bathtub Jitter Analysis

The input signal jitter and phase margin can be measured automatically using the Bathtub function.
The wideband and high-sensitivity PAM4 ED helps more accurate measurement of DUT performance.
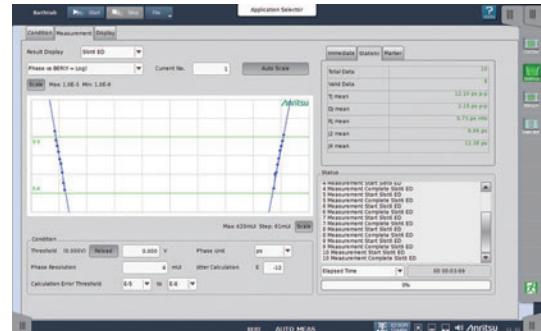
Example of PAM4 Signal Bathtub Measurement
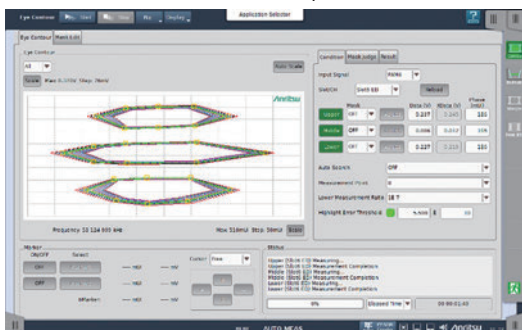
One Box PAM4 BER Test Solution

All-in-One Measurement Solution

8-slot main unit accommodates various modules, including PPG/ED, synthesizer, Jitter modulation source, and noise generator.
A compact, high cost-performance, next-generation, all-in-one measurement solution can be configured without other external instruments.

MP1900A

12.5 GHz 4 Port Synthesizer MU181000B

Jitter Modulation Source MU181500B

PAM4 ED MU196040B

PAM4 PPG MU196020A

Noise Generator MU195050A
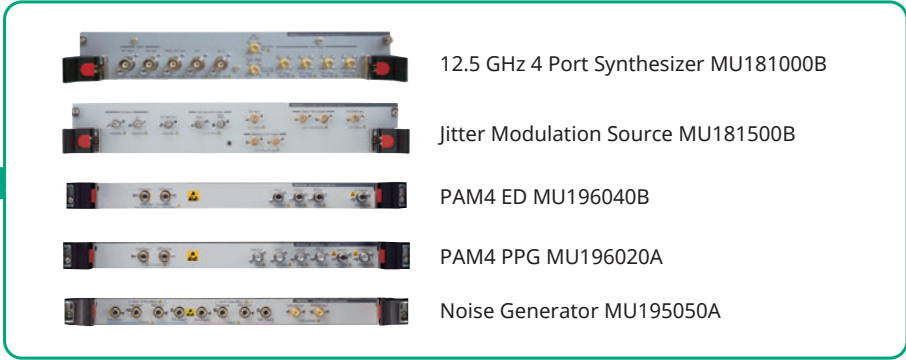
*: Refer to the MP1900A Selection Guide for details of supported multichannel configurations and module combinations.
  Consult your sales representative for module configurations not described in the MP1900A Selection Guide.

64 Gbaud All-in-One NRZ/PAM4 BER Measurement

BER can be measured in real-time without using external equipment. In addition, permits error evaluation at each symbol (MU196040B-041).

- World-first all-in-one solution without requiring external equipment
- Baud rates of 2.4 Gbaud to 58.2 Gbaud (PAM4)/64.2 Gbaud (NRZ)
- Module with built-in Clock Recovery (MU196040B-021, 022, 023), 2.4 Gbaud to 32.1 Gbaud, 51 Gbaud to 58.2 Gbaud
- Symbol BER evaluation (MU196040B-041)

Error Rate Measurement Screen for Each Symbol Level

MP1900A

PAM4 PPG MU196020A

Synthesizer MU181000B

PAM4 ED MU196040B

PAM4

DUT

PAM4
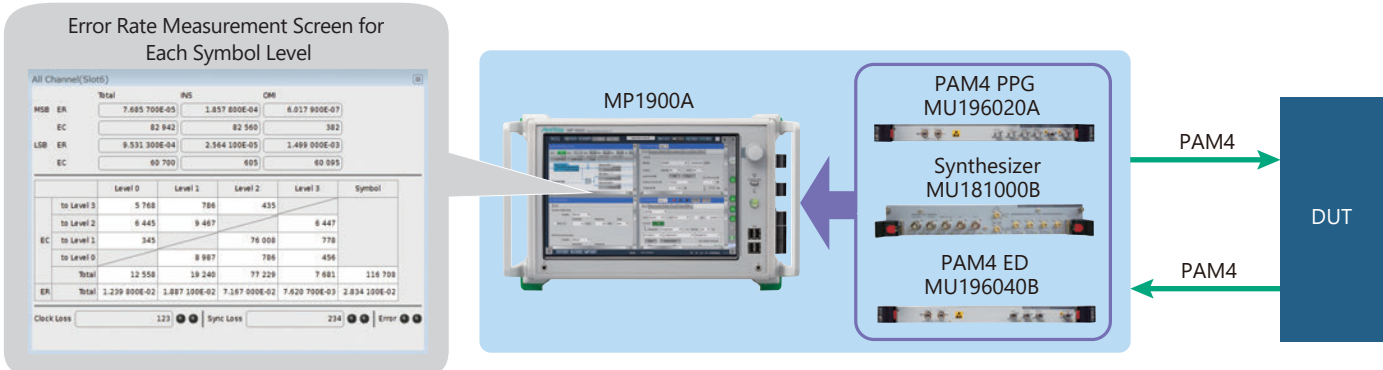
Jitter Tolerance Measurement using DUT BER Counter (MX183000A-PL031)

When the DUT has a bit error counter, combination with the MP1900A PPG makes it easy to configure a highly cost-effective Jitter Tolerance measurement environment.

JTOL Measurement Screen

DUT

PCB Trace

Measure Jitter Tolerance using captured error count

Capture error count via USB or Ethernet connection

One Box PAM4 BER Test Solution

Versatile Jitter/Noise Addition Function for Jitter Tolerance Tests without Other External Equipment (MX183000A-PL001)

The DUT receiver input stress tolerance test measures the BER under the worst conditions using a stressed signal with added jitter and voltage noise. Adding the Jitter Modulation Source MU181500B and MU195050A for adding CM/DM/White Voltage Noise to the MP1900A series supports all-in-one receiver stress tests for various interface standards. Using the MP1900A high-quality signal prior to jitter and noise addition along with the high-linearity jitter and noise addition function offers powerful support for receiver stress tolerance tests.

- Easy Jitter Tolerance measurement
- PHY device Jitter Tolerance test with impressed SJ/RJ/BUJ
- Mask measurements supporting various standards
- Shorter measurement times using low error rate (1E-12, 1E-15, etc.) estimation function
- Tolerance measurement for device characteristics using four Binary, Upward, Downward, and Binary + Linear measurement methods
- Built-in Jitter Tolerance Mask standards for 200/400G including IEEE 802.3, CEI, etc.
- Support for both user-defined masks and new standards
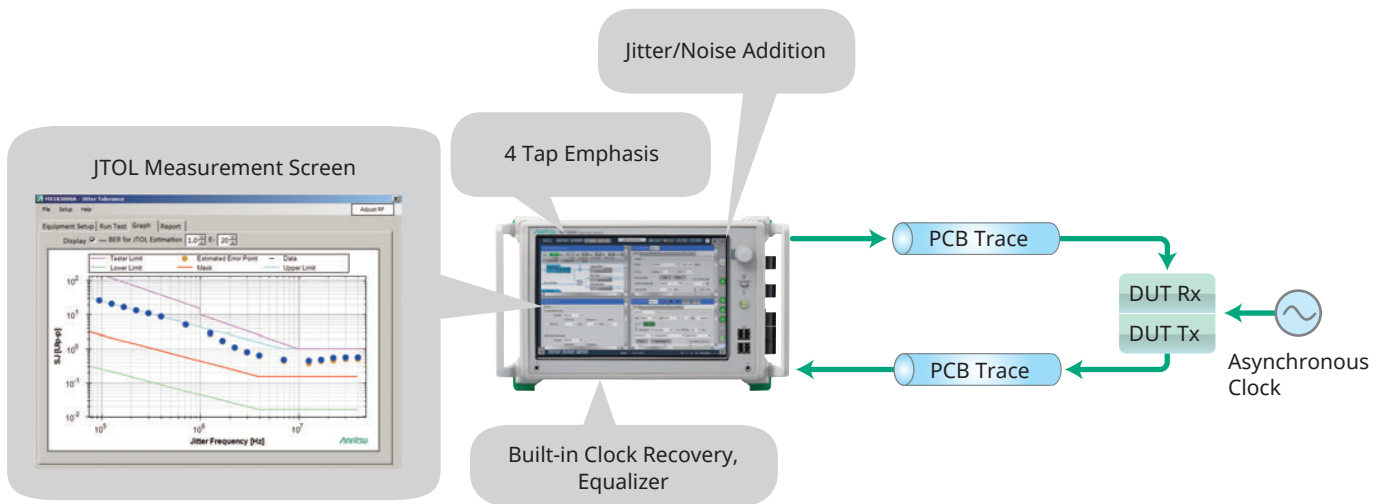
PAM4 Signal Jitter Tolerance Test using One MP1900A
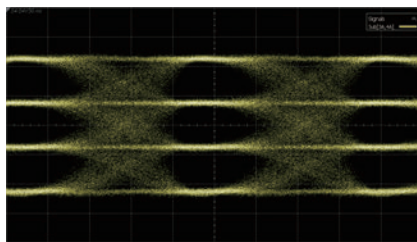
Sine Wave Jitter (SJ)
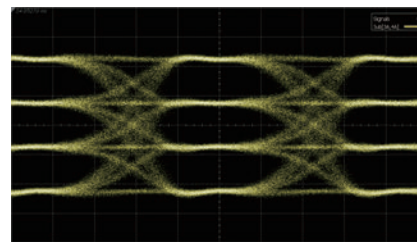
Random Jitter (RJ)
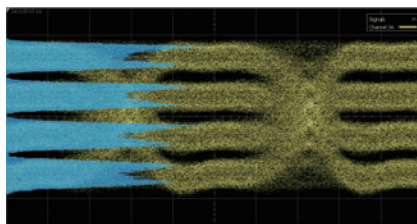
CM/DM Noise
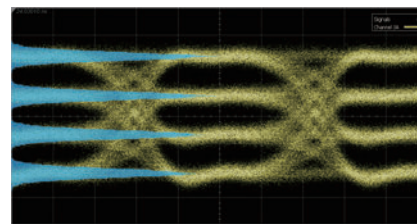
White Noise

Jitter/Noise Types*

*: The upper noise addition rate is 32.1G.

One Box PAM4 BER Test Solution

All-in-One Ethernet/PCIe Measurement

Both PAM4 and increasingly faster PCIe 1.0 to 5.0 interfaces can be measured using this all-in-one test solution. Protocol Aware Link training[1] is supported up to PCIe 5.0 along with PAM4 Symbol Error measurements defined in the next-generation PCIe 6.0 standard and Jitter Tolerance tests, helping play a key role in first-stage PCIe certification[2].

*1: For details, refer to the Selection Guide (MP1900A-E-Z-1)
*2: Contact our business section for details related to PCIe 6.0 Link training.

PCIe Receiver Test Measurement Screen

PAM4 Symbol BER Measurement Screen

MP1900A

SI ED
MU195040A

Synthesizer
MU181000B

Jitter Modulation Source
MU181500B

Noise Generator
MU195050A

PAM4 PPG
MU196020A

PAM4 ED
MU196040B

DUT
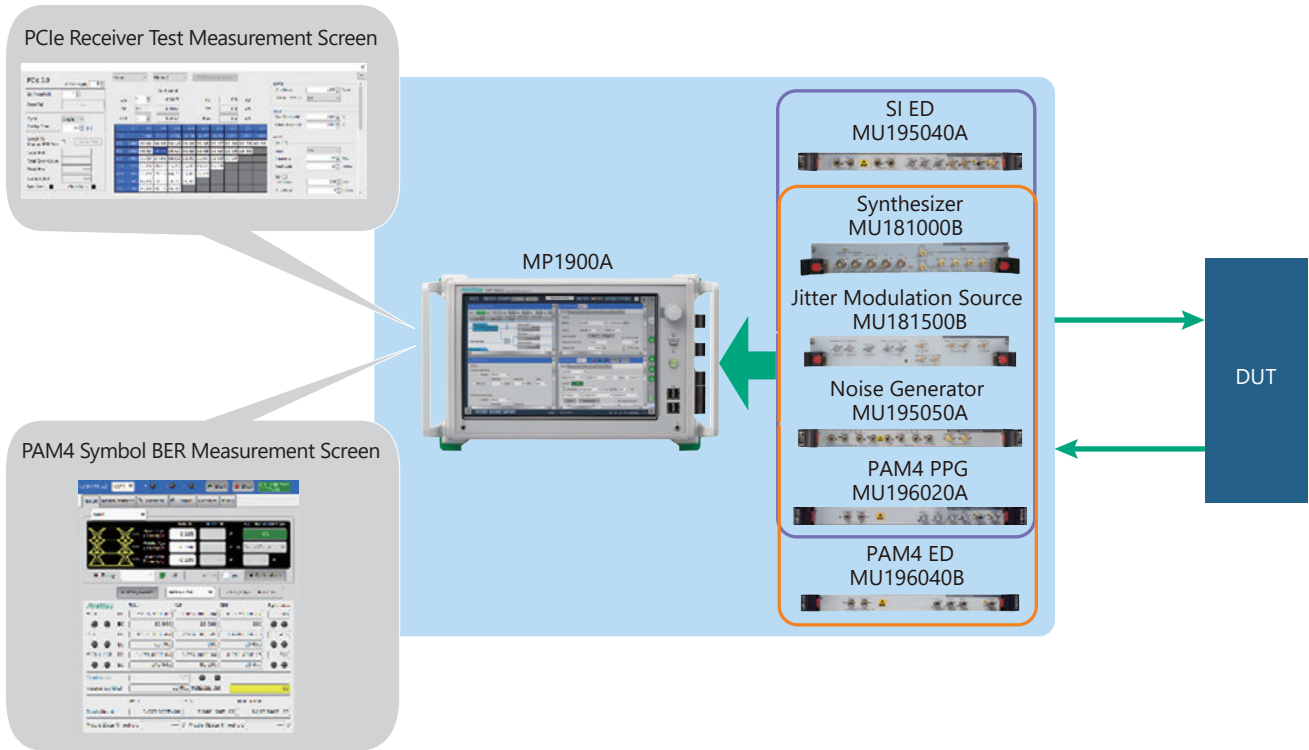
High Transmission Capacity and Excellent Expandability

Easy Multichannel Measurement Support

The MP1900A series is an 8-slot, modular, high-performance BERT.
Installing multiple 64G PAM4 PPG module boards in the slots provides the performance for measuring not only 400 GbE systems but also future 800 GbE systems as well. This flexible expandability helps customers maximize product development-cost efficiencies and bring products to market early.

NRZ Solution
Max. 64 Gbit/s at 1ch

4ch

1ch

128 Gbit/s   256 Gbit/s

PAM4 Solution
Max. 64 Gbaud at 1ch

4ch

1ch

256 Gbit/s   512 Gbit/s
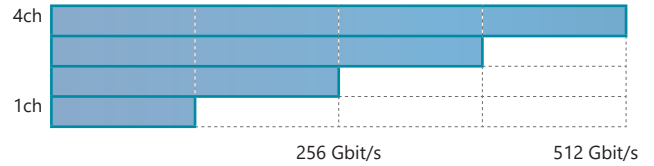
PAM3 Solution
Max. 64 Gbaud at 1ch

4ch

1ch

192 Gbit/s   384 Gbit/s
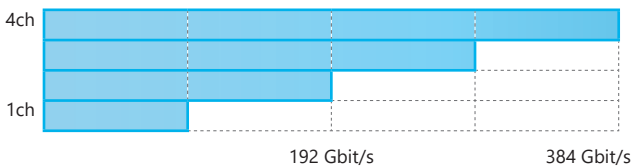
Supports 64G × 4ch Output Pattern Synchronization

Pattern synchronization for each channel ideal for all-at-once evaluation of parallel interfaces, Crosstalk and Skew tolerance evaluation, D/A converter evaluation and FEC pattern evaluation.

Differential 64G × 4ch

MP1900A

CH1	a1	a2	a3	a4	a5
CH2	a1	a2	a3	a4	a5
CH3	a1	a2	a3	a4	a5
CH4	a1	a2	a3	a4	a5

Pattern Synchronous Output

Inter-lane Skew Adjustment and Crosstalk Tests

The phase of each channel can be controlled independently using the option (MU196020A-030).
The precision control in 2-mUI steps supports high-accuracy testing of DUT crosstalk characteristics.

Input Signal

Victim Signal

Aggressor Signal

Crosstalk

Output Signal
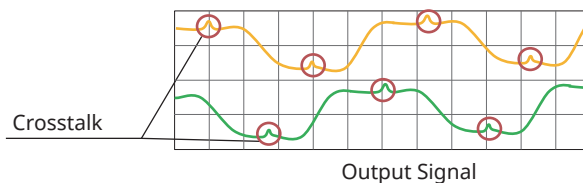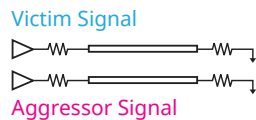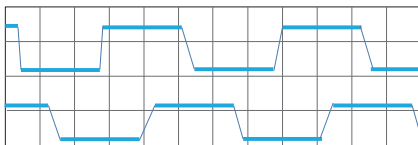
PAM4 PPG/ED Application Example

PAM4 SERDES IC, CDR IC Evaluations

PPG
- Multi-channels
- PAM4 Test Pattern
- PAM4 Level Control
- Emphasis Function
- Jitter/Noise Addition Function

Stress Function Built Into MP1900A Main Unit

Stress Addition

Stress Addition
- Transmission Path Loss (ISI)
- Noise
- Jitter
- Crosstalk

Calibrate and Confirm Test Signal at Oscilloscope

Test Board

PHY IC

ED
- Clock Recovery
- Jitter Tolerance Measurement
- High Sensitivity
- <E-12 BER Rx Performance
- FEC Analysis, Capture

Required Test Items

- Stress Test
- BER and FEC Based Jitter Tolerance Tests

All-in-One Built-in Stress Test Function

Accurate evaluation of the Rx performance of PHY layer ICs used in high-speed servers, optical transceivers, and Active Optical Cables (AOCs) requiring good compatible connectivity requires correction of the signal performance at the test board input connector. When evaluating ICs supporting various protocols, the stress signal including transmission path loss, jitter, etc., must be corrected for various cases according to the specifications. However, changing the cables, test board, and components connected to the PPG for each protocol is time consuming, lowers work efficiency, and has issues with unstable measurement results.
The MP1900A have built-in ISI, Noise, Jitter, Crosstalk, Emphasis, and Clock Recovery functions required for NRZ and PAM4 signal stress tests to support easy and high-reproducibility evaluations using the all-in-one MP1900A.

Jitter Tolerance Test

Supports addition of various jitter types (SJ1/2, RJ, BUJ, SSC) to the PAM4 PPG output (MU181500B). In addition, the PAM4 ED has a built-in Clock Recovery required for Jitter Tolerance tests as well as high sensitivity and wide analog bandwidth performance for receiving low-amplitude and closed-Eye data signals to support high-reproducibility Jitter Tolerance tests. In addition, measurement based on correctable/uncorrectable FEC is supported.

Burst Error Analysis using Real-time FEC Symbol Error Measurement and FEC Symbol Capture Functions

Uncorrectable Codeword and FEC Symbol Errors can be measured and displayed on one screen in real-time simultaneously with bit error measurements. The FEC symbol capture function captures input data when the number of FEC Symbol Errors exceeds the set threshold.
The input data is captured when the number of FEC symbol errors exceeds the threshold setting. The causes of FEC-uncorrectable errors can be analyzed from the captured data.

PAM4 PPG/ED Application Example

TOSA, Driver IC Evaluations

Since the test-signal performance affects the IC performance at evaluation of parts such as TOSA and driver ICs used by optical transceivers requiring analog high-frequency performance, a reference test signal source with fast Tr/Tf and low Intrinsic Jitter is required.

MP1900A PPG modules

Linear Driver 4 lane

TOSA 4 lane

53 Gbaud PAM4

53 Gbaud PAM4
53 Gbaud PAM4
53 Gbaud PAM4
53 Gbaud PAM4

MP2110A Sampling Oscilloscope

PPG Emphasis adjusted automatically when MP2110A oscilloscope connected
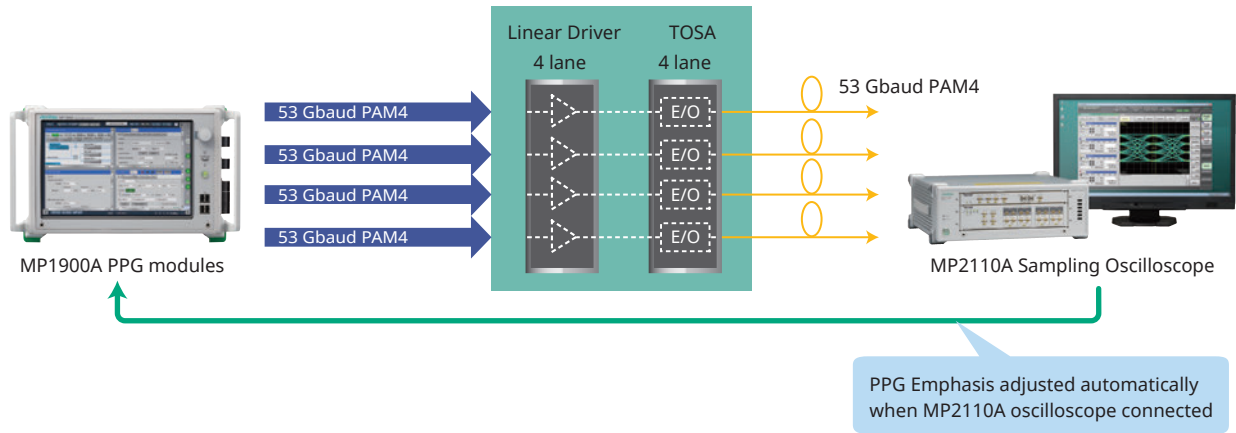
Required Test Items

- Multi-channel synchronous measurement
- Optimized TOSA TDECQ value using Emphasis and Linearity settings

Simultaneous Multichannel Measurement of 4ch max. with One MP1900A

Optical transceiver modules specified as 200 GbE/400 GbE achieve high bit rates using either a 4- or 8-lane optical interface. The MP1900A main unit can accommodate four PAM4 PPG boards and four ED boards in four slots each to perform simultaneous 4ch parallel measurement of multilane integrated optical parts and driver ICs, helping shorten measurement times.

Optimized TOSA TDECQ value using Emphasis and Linearity settings

The TDECQ value is a specific measurement item at 200 GbE/400 GbE PAM4 TOSA evaluation.
The TDECQ value is dependent not only on the signal waveform quality but also on the test signal Emphasis setting and 4-level linearity. Consequently, to examine the true ability, both a high-quality signal source and Emphasis and linearity control functions are required to evaluate the TDECQ characteristics for each setting. The PAM4 PPG MU196020A has built-in Emphasis and linearity control functions supporting high-quality data output with its high Tr/Tf speed and low Intrinsic jitter, which is sufficient for TDECQ optical output evaluation. The functions and performance required for PAM4 signal evaluation are implemented with high-quality waveforms optimized for evaluating TOSA and driver, etc., ICs. Evaluation of TOSA, driver ICs, etc., optimized by implementing functions and performance required for evaluating PAM4 signals using high-quality waveforms. In addition, connecting MP2110A oscilloscope automatically sets optimum Emphasis for TOSA optical signal TDECQ value.

PAM4 PPG/ED Application Example

Optical Module Evaluation
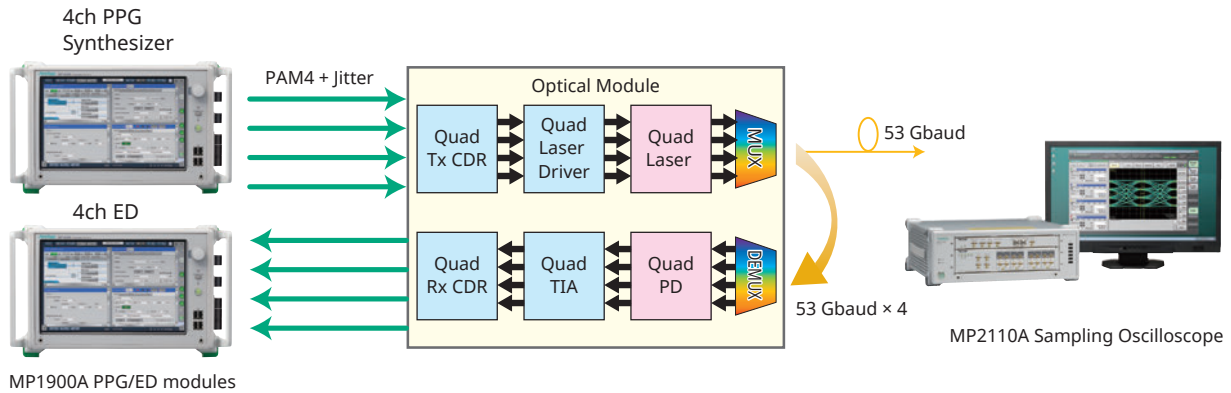
Required Test Items

- Simultaneous 4ch BER Measurement
- Optical output waveform optimized using Emphasis and Linearity Control
- Skew and Crosstalk Tests
- Jitter Tolerance Test

400-GbE (53G × 4λ) PAM4 BER Measurements

IEEE 802.3 200 GbE/400 GbE EML and optical modules can be evaluated.
Multilane evaluation of 4ch EML is supported by simultaneous and independent driving.

Optical Output Waveform Optimization using Emphasis and Linearity Control

The linearity and crosspoints of each Eye on the screen can be adjusted easily using the 4Tap Emphasis up to 20 dB and PAM4 output linearity control function for fast and high-reliability evaluation.

Skew and Crosstalk Test

Applications using 30-Gbaud class signals require testing using actual equipment as well as logic testing.
With pattern synchronization and variable phase functions, the MP1900A easily supports the tests, such as Rx device skew tolerance, crosstalk effect, etc.

Jitter Tolerance Test

With built-in Clock Recovery required for Jitter Tolerance tests, the PAM4 ED can receive low-amplitude, closed-Eye data signals using its high-sensitivity and wide analog band functions to support high-reproducibility Jitter Tolerance tests.

PAM4 PPG/ED Application Example

Multilane FEC Evaluation

FEC can be evaluated by combining the FEC pattern generation, error insertion, and reading the DUT bit error count.

Evaluating Optical FEC Signal Transmission

Jitter Tolerance Measurement
(MX183000A-PL001)

MP1900A

1 or 4 or 8 lanes

Fiber

Optical module

SERDES with FEC decoder

Capture bit error count at USB or Ethernet connection
(MX183000A-PL031)

Evaluating Electrical FEC Signal Transmission

Jitter Tolerance Measurement
(MX183000A-PL001)

MP1900A

1 or 4 or 8 lanes

PCB

SERDES with FEC decoder

Capture bit error count at USB or Ethernet connection
(MX183000A-PL031)

Required Test Items

- Generates 1, 4, 8ch FEC patterns
- Inter-lane Skew Adjustment Test and Crosstalk Test
- Executes Jitter Tolerance tests using FEC patterns
- FEC Analysis Assistance using ED Capture Function

400 GbE Evaluation

IEEE 802.3-specified 400 GbE SERDES FEC evaluation is supported by simultaneous and independent driving of 1, 4, 8ch FEC pattern data output from the all-in-one MP1900A.
And Captures uncorrectable errors from DUT using DUT error counter read function and displays results at MP1900A.

Inter-lane Skew Adjustment Test and Crosstalk Test

FEC decoding is performed after first adjusting the inter-lane skew of the received signal in SERDES.
Since the MP1900A generates signals for the number of lanes and can generate skew of ±64 UI for each lane, it is ideal for testing inter-lane skew adjustment. Additionally, the MP1900A has pattern synchronization and variable phase functions, and easily supports the tests, such as Rx device skew tolerance, crosstalk effect, etc.

Jitter Tolerance Test

Jitter is impressed on the FEC pattern generated by the MP1900A and SERDES uncorrectable errors are read to implement Jitter Tolerance tests with FEC patterns.

FEC Analysis Assistance using ED Capture Function

Generally, RS-FEC (544, 514) is used for 200 GbE/400 GbE, and RS-FEC (528, 514) is used for 25 GbE.
To understand whether errors generated in the transmission line can be corrected or not by FEC, it is important to both count the number of errors and report the error distribution. Additionally, signal analysis helps understand whether errors occur easily when each symbol transitions in some way. The MP1900A has a function for capturing and displaying received signals by using errors as a trigger. In addition to reporting the error distribution using this function, it is also easy to understand what error is generated by which symbol transition.

PAM4 PPG/ED Application Example

Active Cable Evaluation
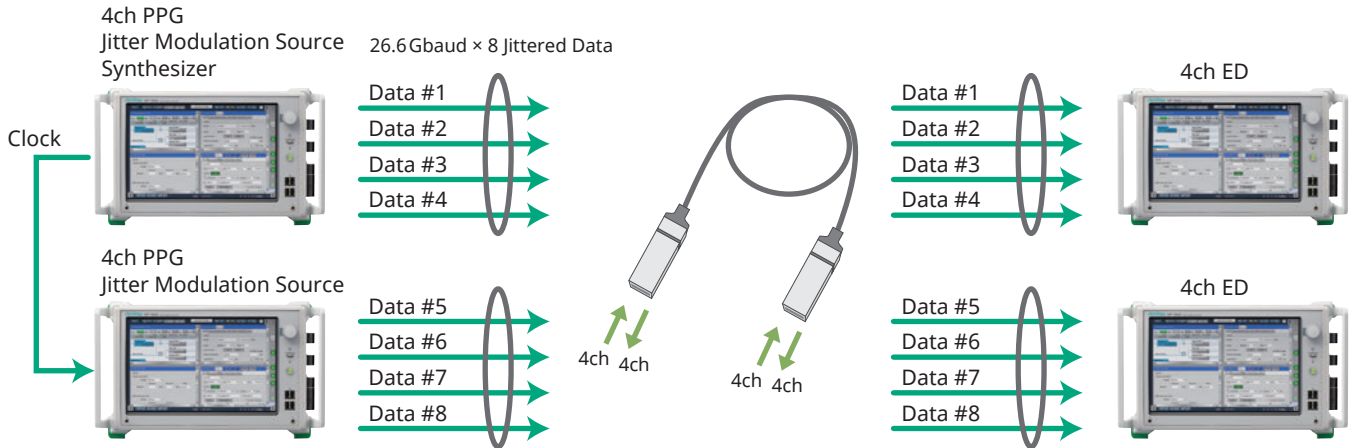
Required Test Items

- 8ch Simultaneous PAM4 BER Measurement
  (4ch both ways)
- Crosstalk Test
- Jitter Tolerance Test

8ch Simultaneous PAM4 BER Measurement (4ch both ways)

QFSP-type Active Optical Cables (AOC) used by 200 GbE, etc., use 4ch transmission in both directions to achieve simultaneous 8ch transmission. The MP1900A can measure 8ch (8ch PPG + 8ch ED) simultaneously for both excellent performance and shorter measurement time.

Crosstalk Test

Applications using 30-Gbaud class signals require testing using actual equipment as well as logic testing.
With pattern synchronization and variable phase functions for each channel, the MP1900A easily supports the tests, such as the impact of AOC crosstalk, etc.

Jitter Tolerance Test

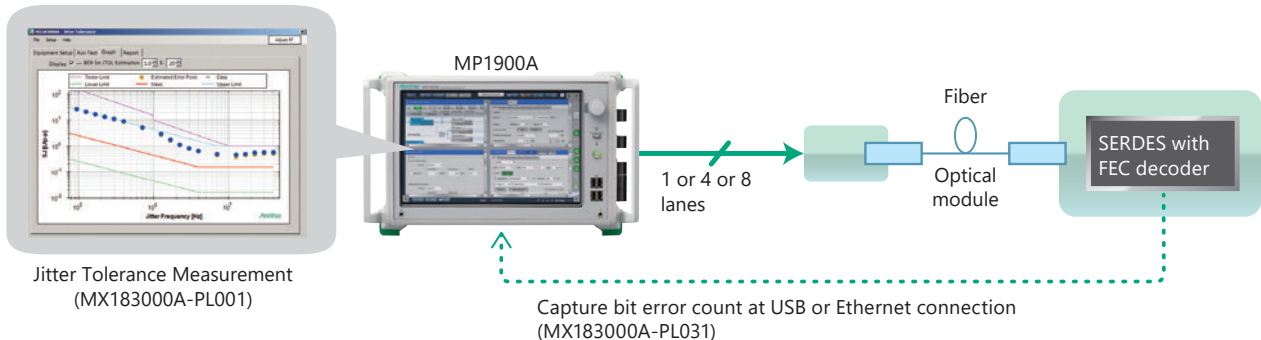AOCs in data centers are increasingly switching to low I/O amplitude levels to cut power consumption, increasing the importance of interconnectivity. With built-in Clock Recovery required for Jitter Tolerance tests, the PAM4 ED can receive low-amplitude, closed-Eye data signals using its high-sensitivity and wide analog band functions to support high-reproducibility Jitter Tolerance tests.
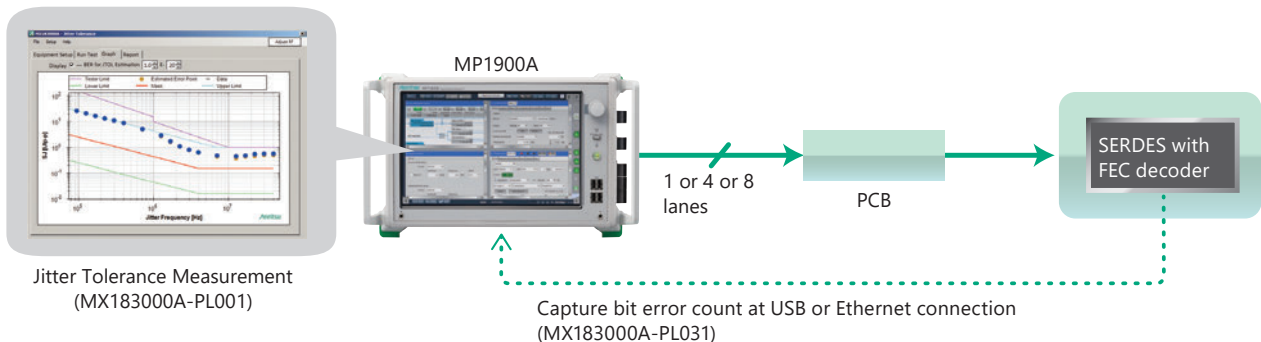
W Components

W1 (1.0 mm) 110-GHz Components

This line of components is for ultra-high-speed signals exceeding 100 GHz.
Future ultra-high-speed signal interfaces are supported by attenuators, dividers, DC blocks, cables, and Bias Tees with a W1 connector.
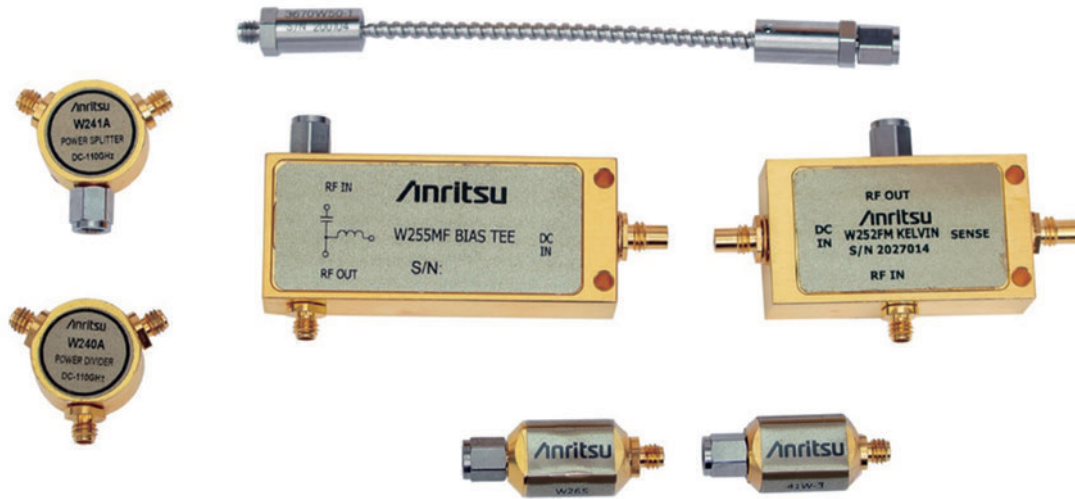
Attenuators	
41W-X* Series	Precision Fixed Attenuator, 3 dB, DC to 110 GHz, W1 (m)-W1 (f), 50Ω
	Precision Fixed Attenuator, 6 dB, DC to 110 GHz, W1 (m)-W1 (f), 50Ω
	Precision Fixed Attenuator, 10 dB, DC to 110 GHz, W1 (m)-W1 (f), 50Ω
Power Divider	
W240A	Precision Power Divider, DC to 110 GHz, W1 (f) input, W1 (f) outputs, 3 resistor, 50Ω
Power Splitter	
W241A	Precision Power Splitter, DC to 110 GHz, W1 (m) input, W1 (f) outputs, 2 resistor, 50Ω
DC Block	
W265	Precision Ultra Wide Band DC Block, 50 kHz to 110 GHz
Cables	
3670W50A-1	Test Port Cable, Armored, Semi-rigid, DC to 110 GHz, W1 (m)-W1 (f), 10 cm
3650W50A-2	Test Port Cable, Armored, Semi-rigid, DC to 110 GHz, W1 (m)-W1 (f), 16 cm
Bias Tees	
W255FM	Precision Ultra Wide Band Bias Tee, 50 kHz to 110 GHz, W1 (f), W1 (m) output, SMC (m) bias
W255MF	Precision Ultra Wide Band Bias Tee, 50 kHz to 110 GHz, W1 (m), W1 (f) output, SMC (m) bias
W252MF	Ultra Wide Band Kelvin Bias Tee, 100 MHz to 110 GHz, W1 (m) input, W1 (f) output, SMC (m) bias and sense
W252FM	Ultra Wide Band Kelvin Bias Tee, 100 MHz to 110 GHz, W1 (f) input, W1 (m) output, SMC (m) bias and sense

*: X is replaced by the attenuation level value

PAM4 PPG/ED Selection Guide

Refer to the Selection Guide (MP1900A-E-Z-1) for details on the module and option combinations.

Category	Model/Name	64G NRZ/PAM4 1ch BERT (1Box)	58G PAM4 SERDES/CPRI Evaluation (All-in-one)/Jitter Tolerance Measurement	Optical Module Evaluation 400 GbE 53G PAM4 4ch BERT	58G/64G PAM4 1ch PPG	TOSA Driver IC Evaluation 400 GbE 53G PAM4 4ch PPG	PCIe Gen1-5 Receiver Test/Gen6 PAM4 BER/JTOL Test
Main Frame	Signal Quality Analyzer-R MP1900A	1	1	2	1	1	1
Synthesizer	12.5 GHz 4 Port Synthesizer MU181000B	1	1	1	1	1	1
	SSC Extension MU181000B-002						1
Jitter Modulation	Jitter Modulation Source MU181500B		1				1
PAM4 PPG	PAM4 PPG MU196020A	1	1	4	1	4	1
	32G baud MU196020A-001						1
	58G baud MU196020A-002	1*2	1*2	4*2	1*2	4	
	64G baud MU196020A-003				1*2		
	4Tap Emphasis MU196020A-011	1	1	4	1	4	1
	Data Delay MU196020A-030			4		4	
	Adjustable ISI MU196020A-040	1	1	4	1	4	
	FEC Pattern Generation MU196020A-042	1	1	4	1	4	
	Inter-Module Synchronization MU196020A-050			4		4	
PAM4 ED	PAM4 ED MU196040B	1	1	4			1*3
	32G baud MU196040B-001	1*2	1*2	4*2			1*3
	58G baud MU196040B-002						
	Equalizer MU196040B-011	1	1	4			1*3
	29G baud Clock Recovery MU196040B-021	1*2	1*2	4*2			
	32G baud Clock Recovery MU196040B-022						1*3
	58G baud Clock Recovery Extension MU196040B-023	1	1	4			
	SER Measurement MU196040B-041	1*1	1	4			1
	FEC Analysis MU196040B-042	1	1	4			1
21G/32G ED	21G/32G bit/s SI ED MU195040A						1
	32 Gbit/s Extension MU195040A-001						1
	1ch ED MU195040A-010						1
	2ch ED MU195040A-020						
	1ch CTLE MU195040A-011						1
	2ch CTLE MU195040A-021						
	Clock Recovery MU195040A-022						1
Voltage Noise	Noise Generator MU195050A		1				1
Software	Jitter Tolerance Test MX183000A-PL001		1				1
	DUT Error Counts Import MX183000A-PL031		1				
	PCIe Link Training MX183000A-PL021						1
	PCIe 5 Link Training MX183000A-PL025						1

*1: Not required at NRZ
*2: Choose any one.
*3: The PAM4 ED is for future PCIe 6.0 BER/JTOL measurements. Please contact our business section regarding support for PCIe 6.0 receiver tests.

Panel Layout

Signal Quality Analyzer-R MP1900A

Front Panel

Rear Panel
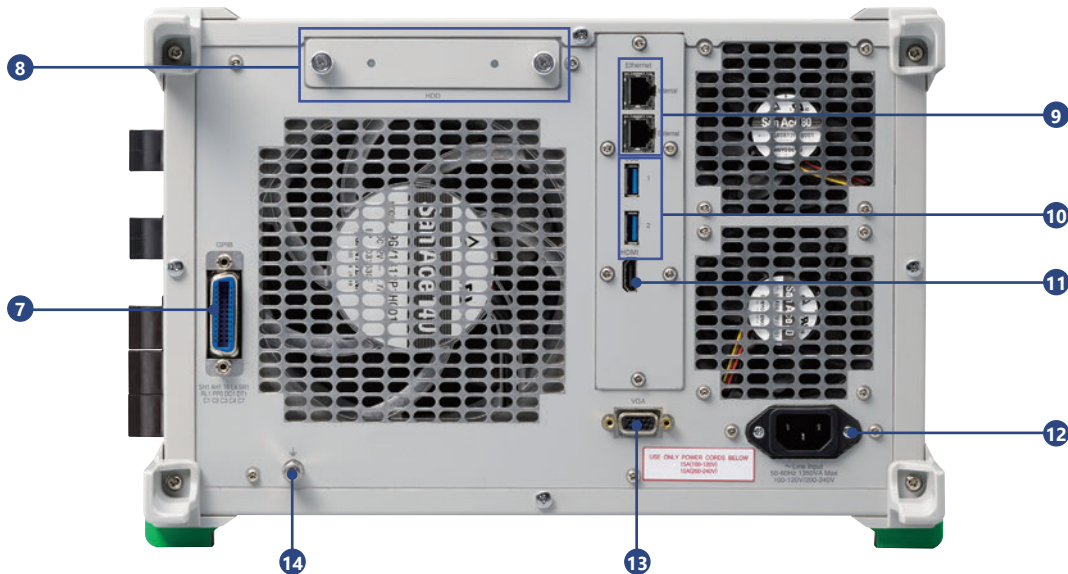
1 **Ground Jack**
Wrist strap to discharge static electricity

2 **USB Port**
Four USB2 ports for connecting peripherals

3 **Power Switch**
Switches power on and off; Standby LED over power switch lights when power cord connected and Power switch set to off

4 **Function Keys**
Keys for defining functions using software

5 **HDD Access LED**
Lamp that lights during access to built-in HDD

6 **Rotary Encoder**
Switch to increase/decrease numeric values by turning knob

7 **GPIB**
GPIB Connector

8 **HDD**
Slot for secondary 2.5" HDD

9 **Ethernet Connector**
External: For Remote Control
(Internal: Reserved for future function expansion)

10 **USB Port**
Two USB3.0 ports for peripherals

11 **HDMI**
HDMI connector for displaying screens on external screen

12 **Power Inlet**
Socket for connecting 3-pole power cord to supply 100 VAC to 12 VAC or 200 VAC to 240 VAC power

13 **VGA**
VGA connector for displaying screens on external screen

14 **Frame Ground Terminal**
Terminal for discharging electrostatic charges; connect DUT and common ground using ground strap

Panel Layout

Modules

21G/32G bit/s SI PPG MU195020A
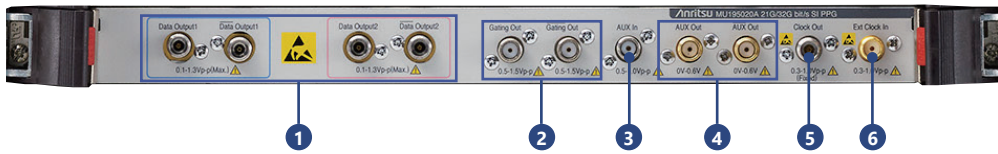
1 **Data Output, Data Output**
Connectors outputting differential Data and Data signals

2 **Gating Out, Gating Out**
Repeat: Timing signal output
Burst: Timing signal output used at Burst

3 **Aux In**
Auxiliary signal input connector
Either Error Injection or Burst can be selected.

4 **Aux Out, Aux Out**
Auxiliary signal output connectors
Output of any of 1/N Clock, Pattern Sync, and Burst2 can be selected.

5 **Clock Out**
Clock signal output connector

6 **Ext Clock In**
Clock signal input connector

21G/32G bit/s SI ED MU195040A

1 **Data Input, Data Input**
Input connectors for Data and Data signals
Supports both differential and single inputs
When the Clock Recovery MU195040A-x22 is installed, the clock is recovered from the signal input to Data Input1.

2 **Aux In**
Auxiliary signal input connector
Any of External Mask, Burst, and Capture External Trigger can be selected.

3 **Aux Out, Aux Out**
Auxiliary signal output connectors
Any of 1/N Clock, Pattern Sync, Error, Sync Gain can be output.

4 **Ext Clock In**
Clock signal input connector

Panel Layout

Modules

PAM4 PPG MU196020A
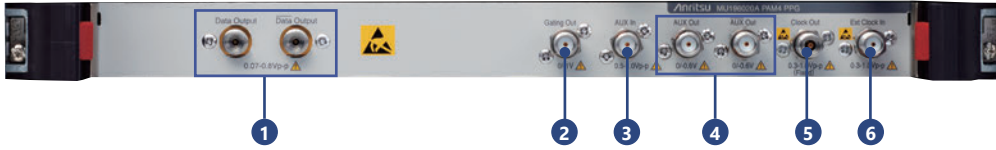
1 **Data Output, $\overline{\text{Data Output}}$**
Connectors outputting differential Data and $\overline{\text{Data}}$ signals

2 **Gating Out**
Repeat: Timing signal output
Burst: Timing signal output used at Burst

3 **Aux In**
Auxiliary signal input connector
Either Error Injection or Burst can be selected.

4 **Aux Out, $\overline{\text{Aux Out}}$**
Auxiliary signal output connectors
Output of any of 1/N Clock, Pattern Sync, and Burst2 can be selected.

5 **Clock Out**
Clock signal output connector

6 **Ext Clock In**
Clock signal input connector

PAM4 ED MU196040B
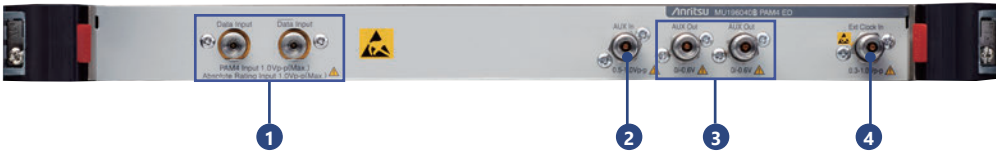
1 **Data Input, $\overline{\text{Data Input}}$**
Input connectors for Data and $\overline{\text{Data}}$ signals
Supports both differential and single inputs

2 **Aux In**
Auxiliary signal input connector
Any of External Mask, Burst, and Capture External Trigger can be selected.

3 **Aux Out, $\overline{\text{Aux Out}}$**
Auxiliary signal output connectors
Any of 1/N Clock, Pattern Sync, Error, Sync Gain can be output.

4 **Ext Clock In**
Clock signal input connector

Noise Generator MU195050A
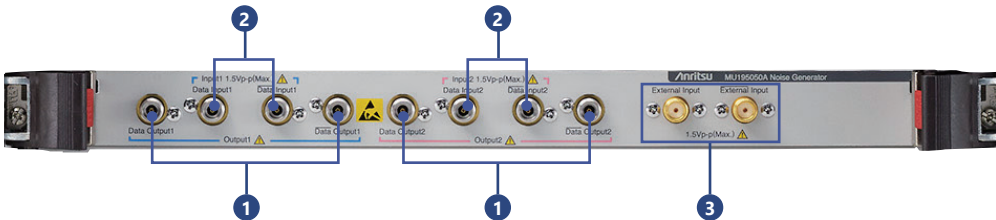
1 **Data Output, $\overline{\text{Data Output}}$**
Connector for outputting differential Data and $\overline{\text{Data}}$ Signal with added noise

2 **Data Input, $\overline{\text{Data Input}}$**
Connector for inputting Data and Data signal with added noise

3 **External Input, $\overline{\text{External Input}}$**
External noise input connectors

* Input2 and Output2 are not used by the MU196020A

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Panel Layout

Modules

12.5 GHz 4port Synthesizer MU181000B
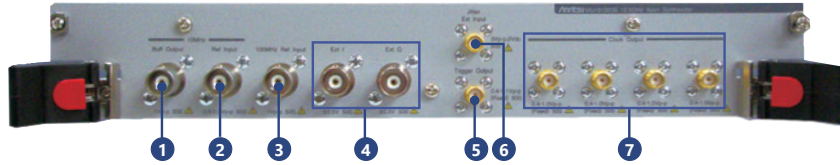
❶ **10 MHz Buff Output**
Output 10 MHz clock for reference

❷ **10 MHz Ref Input**
Inputs 10 MHz clock for reference

❸ **100 MHz Ref Input**[*1]
Inputs 100 MHz clock for reference

❹ **Ext I, Q**[*2]
Inputs I, Q signals

❺ **Trigger Output**[*2]
Outputs 1/1 or 1/64 clock frequency

❻ **Jitter Ext Input**[*2]
Inputs modulation signal source

❼ **Clock Output 1 to 4**
Outputs clocks

*1: Only when Jitter Modulation Option (MU181000B-001) or SSC Extension (MU181000B-002) installed
*2: Only when Jitter Modulation Option installed (MU181000B-001)

Jitter Modulation Source MU181500B
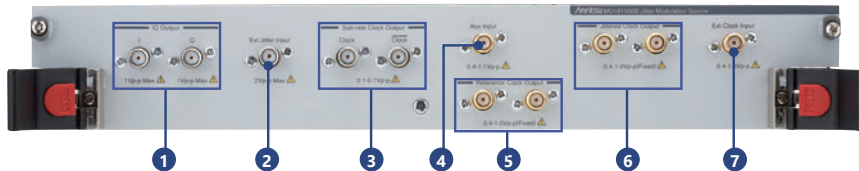
❶ **IQ Output**
Outputs IQ signal

❷ **Ext Jitter Input**
Inputs Jitter Modulation Source

❸ **Sub-rate Clock Output**
Differential Clock Output signal generated from 1/8 to 1/256-divided Clock Output based on any of following Clock inputs
• Ext Clock Input   • Aux Input

❹ **Aux Input**
Inputs clock signal

❺ **Reference Clock Output**
Dual-system Clock Output signal generated from either 1/1, 1/2, or 1/4-divided Jitter Clock Output based on any of following Clock inputs
• Ext Clock Input   • Aux Input

❻ **Jittered Clock Output**
Two outputs jitter modulated clock signal

❼ **Ext Clock Input**
Inputs external clock

28G/32G bit/s PPG (1ch or 2ch) MU183020A

❶ **Data1/Data1 Output**[*3]
Output for 1ch differential data signal

❷ **Data2/Data2 Output**[*4]
Output for 2ch differential data signal

❸ **Gating Output**
Output for burst timing signal

❹ **Aux Input**
Input for auxiliary signal

❺ **Aux/Aux Output**
Output for differential auxiliary signal

❻ **Clock Output**
Output for clock signal

❼ **Ext Clock Input**
Input for external clock signal

*3: Data/Data when 1ch option was selected.
*4: Not implemented when 1ch option was selected.

28G/32G bit/s High Sensitivity ED (1ch or 2ch) MU183040B

❶ **Data1/Data1 Input**[*5]
Input for 1ch differential data signal

❷ **Data2/Data2 Input**[*6]
Input for 2ch differential data signal

❸ **Aux Input**
Input for auxiliary signal

❹ **Aux/Aux Output**
Output for differential auxiliary signal

❺ **Ext Clock Input**
Input for external clock signal

*5: Data/Data when 1ch option was selected.
*6: Not implemented when 1ch option was selected.

Signal Quality Analyzer-R MP1900A Specifications

Refer to the MP1900A Data Sheet (MP1900A_Datasheet-E-A-1) for detailed specifications.

Signal Quality Analyzer-R MP1900A

LCD	12.1" WXGA 1280 × 800
Remote Interface	GPIB, LAN
Module Slots	8
External Equipment Interface	USB × 6, VGA × 1, HDMI × 1
OS	Window Embedded Standard 7
Power Supply	100 VAC to 120 VAC, 200 VAC to 240 VAC, 50 Hz to 60 Hz Power consumption: 1350 VA max.
Dimensions and Mass	340 (W) × 222.5 (H) × 451 (D) mm, 20 kg (excluding modules)
CE	EMC	2014/30/EU, EN61326-1, EN61000-3-2
	LVD	2014/35/EU, EN61010-1
	RoHS	2011/65/EU, EN50581

12.5 GHz 4 Port Synthesizer MU181000B

Clock Output	Number of Output: 4 Frequency Range: 0.1 GHz to 12.5 GHz, Steps: 1 kHz/1 MHz Level: 0.4 Vp-p to 1 Vp-p (AC) Connector: SMA (f), Termination: 50Ω/GND
10 MHz Input	Frequency: 10 MHz ±10 ppm Level: 0.5 Vp-p to 2.0 Vp-p Connector: BNC, Termination: 50Ω/GND
10 MHz Output	Level: 1.0 Vp-p ±30% (AC) Connector: BNC, Termination: 50Ω/GND
100 MHz Reference Signal Input (SSC Extension MU181000B-002)	Outputs either 100 MHz with phase deviation x25, x50, or x80 frequency-multiplied clock from Clock Output connector Supports PCI Express Host Reflclk input Modulation Frequency: 30 kHz to 33 kHz Level: 0.15 Vp-p to 1.3 Vp-p (AC) Connector: BNC

Jitter Modulation Source MU181500B

External Clock Input	Frequency Range: 0.800 000 GHz to 15.000 000 GHz Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA (f), Termination: 50Ω/AC Coupling
Jittered Clock Output	Number of Output: 2 Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA (f), Termination: 50Ω/AC Coupling
SJ1	Modulation Frequency: 10 Hz to 250 MHz Amplitude: 0 to 2000 UI @Modulation Frequency 10 kHz to 100 kHz 　　　　　　 0 to 1 UI @Modulation Frequency 10 MHz to 250 MHz (Different depending on the operating bit rate)
Built-in SJ2	Modulation Frequency: 33 kHz, 87 MHz, 100 MHz, 210 MHz
Spread Spectrum Clocking (SSC)	Modulation Frequency: 28 kHz to 37 kHz Deviation: 0 to 7000 ppm
Random Jitter (RJ)	Bandwidth: 10 kHz to 1 GHz Amplitude: 0 to 0.5 UI (Different depending on the operating frequency)
Bounded Uncorrelated Jitter (BUJ)	PRBS Pattern Length: $2^n - 1$ (n = 7, 9, 11, 15, 23, or 31) BUJ Rate: 0.1 Gbit/s to 3.2 Gbit/s, 4.9 Gbit/s to 6.25 Gbit/s, 9.8 Gbit/s to 12.5 Gbit/s Filter Type (LPF 3 dB Bandwidth): 50, 100, 200, 300, 500 MHz, Through Amplitude: 0 to 0.5 UI (Different depending on the operating frequency)
External Jitter	Bandwidth: 10 kHz to 1 GHz

Noise Generator MU195050A

Number of Channels	2
Insertion Loss	−3 dB
CMI: Common Mode Noise	0.1 GHz to 6 GHz: Sinusoidal wave
DMI: Differential Mode Noise	2 GHz to 10 GHz: Sinusoidal wave
White Noise	10 MHz to 10 GHz
Crest Factor	>5

Signal Quality Analyzer-R MP1900A Specifications

Refer to the MP1900A Data Sheet (MP1900A_Datasheet-E-A-1) for detailed specifications.

21G/32G bit/s SI PPG MU195020A

Operation Rate (NRZ)	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of Channels	1 or 2
Output Amplitude	0.1 Vp-p to 1.3 Vp-p (Single-end) 0.2 Vp-p to 2.6 Vp-p (Differential)
Emphasis	10Tap
Channel Emulator	Normal: Emulates Insertion Loss using S-parameter data Inverse: Performs De-Emphasis compensation for S-parameter Insertion Loss S-Parameter file: S2P,S4P
ISI	Emulates ISI output using CEI-28G/25G Nyquist frequency loss setting Supports loss control in combination with ISI Board J1758A accessory Insertion Loss setting: 1.5 to 25 dB, 0.01 dB step, Nyquist frequency 0 to 25 dB, 0.01 dB step, 1/2 Nyquist frequency
Tr/Tf (20 to 80%)	12 ps (typ.)
Random Jitter	115 fs rms (typ.)
PCIe, USB Link Training	Supported (MX183000A-PL021/PL022/PL025)
Output Connector	K (f)

21G/32G bit/s SI ED MU195040A

Operation Rate (NRZ)	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of Channels	1 or 2
Input Attitude	0.05 Vp-p to 1.0 Vp-p (Single-End) 0.1 Vp-p to 2.0 Vp-p (Differential)
Input Sensitivity (Eye Height)	15 mV (28.1 Gbit/s, NRZ) 30 mV/Eye (28.1 Gbaud, PRBS15, PAM4)
CTLE	Peak Frequency: 14, 8, 4 GHz Gain: 0 to −12 dB
Clock Recovery	Yes, supports SSC
PCIe, USB Link Training	Supported (MX183000A-PL021/PL022/PL025)
Input Connector	K (f)

PAM4 PPG MU196020A

Operation Rate (PAM4/NRZ)	2.4 Gbaud to 32.1/58.2/64.2 Gbaud (option selection)
No. of Channels	1
Output Amplitude	70 mVp-p to 800 mVp-p (Single-end) 140 mVp-p to 1600 mVp-p (Differential)
Offset	−2 V to +3.3 V
Emphasis	4 Tap, −20 to +20 dB
Channel Emulator	Generates waveform with insertion loss and simulates waveform with corrected insertion loss Set by loading S-Parameter file (S2 P, S4 P)
ISI	Simulates ISI generation waveform Set using loss (−8.00 to 8.00 dB) at CEI-specified Nyquist frequency Used in combination with channel board, such as J1800A/J1758A (optional accessories parts), or Noise Module MU195050A
Independently Variable PAM4 3 Eye	20 to 50% (PAM4 Amplitude 0/3 level = 100%)
PAM4 Pattern	SSPRQ, PRBS13Q, PRBS31Q, RS-FEC, etc.
PAM4 Pattern Error Addition	MSB Error, LSB Error, LSB&MSB Error, RS-FEC Symbol Error
Tr/Tf (20 to 80%)	8.5 ps (typ., NRZ)
Random Jitter	170 fs rms (typ., NRZ)
Output Connector	V (f)

PAM4 ED MU196040B

Operation Rates (PAM4/NRZ)	2.4 Gbaud to either 32.1 Gbaud, or 58.2 Gbaud (PAM4)/64.2 Gbaud (NRZ) (option selection)
No. of Channels	1
Input Amplitude	NRZ: ≤32.1G: 0.05 Vp-p to 1.0 Vp-p, >32.1G: 0.1 Vp-p to 1.0 Vp-p PAM4: ≤32.1G: 0.3 Vp-p to 1.0 Vp-p, >32.1G: 0.4 Vp-p to 1.0 Vp-p
Input Sensitivity (Eye Height)	NRZ: 19 mV @ 26.5625 Gbaud, 21 mV @ 53.125 Gbaud PAM4: 23 mV @ 26.5625 Gbaud, 36 mV @ 53.125 Gbaud
Clock Recovery (Option)	2.4 Gbaud to 32.1 Gbaud, 51 Gbaud to 58.2 Gbaud
Equalizer (Option)	Low-frequency Equalizer (≤1 GHz, 2 dB typ.) + DFE (1.4 dB typ.)
PAM4 Patterns	SSPRQ, PRBS13Q, PRBS31Q, etc.
PAM4 Counter	MSB, LSB, Symbol 0 to 3 (Option)
Input Connector	V (f)

Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.
The names listed in the chart below are Order Names. The actual name of the item may differ from the Order Name.

MP1900A

Model/Order No.	Name	
	Main Frame*1	
MP1900A	Signal Quality Analyzer-R	
	Standard Accessories	
G0342A	ESD DISCHARGER:	1
J1211	POWER CORD. 3M:	1
J1627A	GND connection cable:	1
P0031A	USB Memory:	1
Z0306A	Wrist Strap:	1
	Retrofit Option	
MP1900A-110	Windows10 Upgrade Retrofit*2	
	Maintenance Service	
MP1900A-ES310	Three Years Extended Warranty Service	
MP1900A-ES510	Five Years Extended Warranty Service	

*1: The Windows 10 OS will be installed in all orders from July 1, 2020.
*2: MP1900A main units running Windows Embedded Standard 7 are retrofitted
to Windows 10 using a hardware upgrade. Anritsu destroys
the unnecessary, post-upgrade Windows Embedded Standard 7 parts.
For details, contact our sales representative.

MU181000B

Model/Order No.	Name	
	Module	
MU181000B	12.5 GHz 4port Synthesizer	
	Standard Accessories	
J1624A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz):	4 pcs
	Option	
MU181000B-001	Jitter Modulation	
MU181000B-002	SSC Extension	
	Retrofit Option	
MU181000B-101	Jitter Modulation Retrofit	
MU181000B-102	SSC Extension Retrofit	
	Maintenance Service	
MU181000B-ES310	Three Years Extended Warranty Service	
MU181000B-ES510	Five Years Extended Warranty Service	

MU181500B

Model/Order No.	Name	
	Module	
MU181500B	Jitter Modulation Source	
	Standard Accessories	
J1624A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz):	1 pc
J1508A	BNC-SMA Connector Cable (30 cm):	2 pcs
J1137	Terminator:	6 pcs
J1341A	Open:	2 pcs
Z0897A	MP1800A Manual CD:	1 pc
Z0918A	MX180000A Software CD:	1 pc
	Maintenance Service	
MU181500B-ES310	Three Years Extended Warranty Service	
MU181500B-ES510	Five Years Extended Warranty Service	

MU195050A

Model/Order No.	Name	
	Module	
MU195050A	Noise Generator	
	Standard Accessories	
J1632A	Terminator:	4
J1359A	Coaxial Adapter (K-P, K-J, SMA):	4
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J):	2
J1341A	Open:	6
J1746A	Skew Match Pair Semrigid Cable	
	(K connector, Data Input1):	1 set
J1747A	Skew Match Pair Semrigid Cable	
	(K connector, Data Input2):	1 set
J1792A	Skew Match Pair Semrigid Cable	
	(V-K connector, MU196020A PPG Output to MU195050A Noise Data Input1):	1 set
	Option	
MU195050A-001	White Noise	
	Retrofit Option	
MU195050A-101	White Noise Retrofit	
	Maintenance Service	
MU195050A-ES310	Three Years Extended Warranty Service	
MU195050A-ES510	Five Years Extended Warranty Service	

Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

MU195020A

Model/Order No.	Name	
	Module	
MU195020A	21G/32G bit/s SI PPG	
	Standard Accessories	
J1632A	Terminator:	5
J1341A	Open:	2
J1359A	Coaxial Adapter (K-P, K-J, SMA):	1
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J):	6
	Option	
MU195020A-001	32G bit/s Extension	
MU195020A-010	1ch Data Output	
MU195020A-020	2ch Data Output	
MU195020A-011	1ch 10Tap Emphasis	
MU195020A-021	2ch 10Tap Emphasis	
MU195020A-030	1ch Data Delay	
MU195020A-031	2ch Data Delay	
MU195020A-040	1ch Variable ISI	
MU195020A-041	2ch Variable ISI	
	Retrofit Options	
MU195020A-101	32G bit/s Extension Retrofit	
MU195020A-120	2ch Data Output Retrofit	
MU195020A-111	1ch 10Tap Emphasis Retrofit	
MU195020A-121	2ch 10Tap Emphasis Retrofit	
MU195020A-130	1ch Data Delay Retrofit	
MU195020A-131	2ch Data Delay Retrofit	
MU195020A-140	1ch Variable ISI Retrofit	
MU195020A-141	2ch Variable ISI Retrofit	
	When Option 010/110 Installed	
J1632A	Terminator:	2
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2
	When Option 020/120 Installed	
J1632A	Terminator:	4
J1359A	Coaxial Adapter (K-P, K-J, SMA):	4
	Maintenance Service	
MU195020A-ES310	Three Years Extended Warranty Service	
MU195020A-ES510	Five Years Extended Warranty Service	

MU196020A*6

Model/Order No.	Name	
	Module	
MU196020A	PAM4 PPG	
	Standard Accessories	
J1632A	TERMINATOR:	4
V210	TERMINATOR (V):	2
J1341A	OPEN:	2
J1359A	COAXIAL ADAPTOR (K-P.K-J,SMA):	1
J1717A	COAXIAL ADAPTOR(SMA-P.SMA-J):	5
	Option	
MU196020A-001	32G baud*	
MU196020A-002	58G baud*	
MU196020A-003	64G baud*	
MU196020A-011	4Tap Emphasis	
MU196020A-030	Data Delay	
MU196020A-040	Adjustable ISI	
MU196020A-042	FEC Pattern Generation	
MU196020A-050	Inter-Module Synchronization	
	Retrofit Options	
MU196020A-112	32G to 58G baud Extension Retrofit	
MU196020A-113	32G to 64G baud Retrofit	
MU196020A-123	58G to 64G baud Retrofit	
MU196020A-111	4Tap Emphasis Retrofit	
MU196020A-130	Data Delay Retrofit	
MU196020A-140	Adjustable ISI Retrofit	
MU196020A-142	FEC Pattern Generation Retrofit	
MU196020A-150	Inter-Module Synchronization Retrofit	
	Maintenance Service	
MU196020A-ES310	Three Years Extended Warranty Service	
MU196020A-ES510	Five Years Extended Warranty Service	

*: Select any one

MU195040A

Model/Order No.	Name	
	Module	
MU195040A	21G/32G bit/s SI ED	
	Standard Accessories	
J1632A	Terminator:	2
J1341A	Open:	1
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J):	4
	Option	
MU195040A-001	32G bit/s Extension	
MU195040A-010	1ch ED	
MU195040A-020	2ch ED	
MU195040A-011	1ch CTLE	
MU195040A-021	2ch CTLE	
MU195040A-022	Clock Recovery	
	Retrofit Options	
MU195040A-101	32G bit/s Extension Retrofit	
MU195040A-120	2ch ED Retrofit	
MU195040A-111	1ch CTLE Retrofit	
MU195040A-121	2ch CTLE Retrofit	
MU195040A-122	Clock Recovery Retrofit	
	When Option 010/110 Installed	
J1341A	Open:	3
J1359A	Coaxial Adapter (K-P, K-J, SMA):	2
41KC-6	Fixed Attenuator 6 dB:	2
	When Option 020/120 Installed	
J1341A	Open:	5
J1359A	Coaxial Adapter (K-P, K-J, SMA):	4
41KC-6	Fixed Attenuator 6 dB:	4
	Maintenance Service	
MU195040A-ES310	Three Years Extended Warranty Service	
MU195040A-ES510	Five Years Extended Warranty Service	

MU196040B*6

Model/Order No.	Name	
	Module	
MU196040B	PAM4 ED	
	Standard Accessories	
J1632A	TERMINATOR:	2
V210	TERMINATOR (V):	2
J1341A	OPEN:	2
J1359A	COAXIAL ADAPTOR (K-P.K-J,SMA):	1
J1717A	COAXIAL ADAPTOR (SMA-P.SMA-J):	3
41VA-6	Fixed Attenuator 6 dB:	2
	Option	
MU196040B-001	32G baud (2.4G to 32.1G)	
MU196040B-002	58G baud (NRZ: 2.4G to 64.2G, PAM4: 2.4G to 58.2G)	
MU196040B-011	Equalizer	
MU196040B-021	29G baud Clock Recovery (2.4G to 29G)	
MU196040B-022	32G baud Clock Recovery (2.4G to 32.1G)	
MU196040B-023	58G baud Clock Recovery Extension (51G to 58.2G)	
MU196040B-041	SER Measurement	
MU196040B-042	FEC Analysis	
	Retrofit Options	
MU196040B-111	Equalizer Retrofit	
MU196040B-112	32G to 58G baud Extension Retrofit	
MU196040B-121	29G baud Clock Recovery Retrofit	
MU196040B-122	32G baud Clock Recovery Retrofit	
MU196040B-123	58G baud Clock Recovery Extension Retrofit	
MU196040B-124	32G baud Clock Recovery Extension Retrofit	
MU196040B-141	SER Measurement Retrofit	
MU196040B-342	FEC Analysis Retrofit	
	Maintenance Service	
MU196040B-ES310	Three Years Extended Warranty Service	
MU196040B-ES510	Five Years Extended Warranty Service	

Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

MU183020A

Model/Order No.	Name	
MU183020A	**Module** 28G/32G bit/s PPG	
J1137 J1359A J1341A J0541E Z0897A Z0918A	**Standard Accessories** Terminator: Coaxial Adaptor (K-P, K-J, SMA): Open: 6 dB Fixed Attenuator: MP1800A Manual CD: MX180000A Software CD:	3 pcs 1 pc 1 pc 1 pc 1 pc 1 pc
MU183020A-001 MU183020A-012 MU183020A-013 MU183020A-022 MU183020A-023 MU183020A-030 MU183020A-031	**Options** 32G bit/s Extension 1ch 2 V Data Output 1ch 3.5 V Data Output 2ch 2 V Data Output 2ch 3.5 V Data Output 1ch Data Delay 2ch Data Delay	
MU183020A-101 MU183020A-112 MU183020A-113 MU183020A-122 MU183020A-123 MU183020A-130 MU183020A-131	**Retrofit Options** 32G bit/s Extension Retrofit 1ch 2 V Data Output Retrofit 1ch 3.5 V Data Output Retrofit 2ch 2 V Data Output Retrofit 2ch 3.5 V Data Output Retrofit 1ch Data Delay Retrofit 2ch Data Delay Retrofit	
J1137 J1359A	**Standard Accessories for MU183020A-x12, x13** Terminator: Coaxial Adaptor (K-P, K-J, SMA):	2 pcs 2 pcs
J1137 J1359A	**Standard Accessories for MU183020A-x22, x23** Terminator: Coaxial Adaptor (K-P, K-J, SMA):	4 pcs 4 pcs
MU183020A-ES310 MU183020A-ES510	**Maintenance Service** Three Years Extended Warranty Service Five Years Extended Warranty Service	

MU183040B

Model/Order No.	Name	
MU183040B	**Module** 28G/32G bit/s High Sensitivity ED	
J1137 J1341A Z0897A Z0918A	**Standard Accessories** Terminator: Open: MP1800A Manual CD: MX180000A Software CD:	2 pcs 1 pc 1 pc 1 pc
MU183040B-001 MU183040B-010 MU183040B-020 MU183040B-022 MU183040B-023	**Options** 32 Gbit/s Extension 1ch ED 2ch ED 2.4G to 28.1G bit/s Clock Recovery 25.5G to 32.1G bit/s Clock Recovery	
MU183040B-101 MU183040B-110 MU183040B-120 MU183040B-122 MU183040B-123	**Retrofit Options** 32 Gbit/s Extension Retrofit 1ch ED Retrofit 2ch ED Retrofit 2.4G to 28.1G bit/s Clock Recover Retrofit 25.5G to 32.1G bit/s Clock Recovery Retrofit	
J1341A J1359A 41KC-6	**Standard Accessories for MU183040B-x10** Open: Coaxial Adaptor (K-P, K-J, SMA): Precision Fixed Attenuator 6 dB:	2 pcs 2 pcs 2 pcs
J1341A J1359A 41KC-6	**Standard Accessories for MU183040B-x20** Open: Coaxial Adaptor (K-P, K-J, SMA): Precision Fixed Attenuator 6 dB:	4 pcs 4 pcs 4 pcs
MU183040B-ES310 MU183040B-ES510	**Maintenance Service** Three Years Extended Warranty Service Five Years Extended Warranty Service	

Software

Model/Order No.	Name
MX183000A	High-Speed Serial Data Test Software
MX183000A-PL001	Jitter Tolerance Test
MX183000A-PL011	PCIe Link Sequence
MX183000A-PL021	PCIe Link Training[3]
MX183000A-PL022	USB Link Training
MX183000A-PL025	PCIe 5 Link Training[3]
MX183000A-PL031	DUT Error Counts Import

*3: The PL021 option supports PCIe Gen1 to Gen4.
　　The PL025 option supports PCIe Gen5.
　　PL021 is required to add PL025.

On Using VISA[4]

The National Instruments™ (NI hereafter) NI-VISA[5] software must be installed to use the MX183000A (this product hereafter). We recommend using NI-VISA saved on the product USB memory stick. Customers may only use NI-VISA saved on the product memory stick. NI-VISA on the memory stick may not be used for other applications with other products.
When uninstalling this product from the controller PC, etc., also uninstall NI-VISA from the USB memory.

*4: Abbreviation for Virtual Instrument Software Architecture. This is I/O software for remote control of measuring instruments via GPIB, Ethernet and USB interfaces.

*5: NI-VISA was developed by National Instruments for VXI Plug&Play Alliance standards compliant I/O interfaces.
　　National Instruments™, NI™, and NI-VISA™ are registered trademarks of National Instruments Corporation.

Ordering Information

Optional Accessories

| Model/Order No.	Name
J1632A	Terminator
V210	TERMINATOR (V)
J1678A	ESD Protection Adapter-K
J1679A	ESD Protection Adapter-V
J1359A	Coaxial Adapter (K-P, K-J, SMA)
34VFK50A	Fixed Adapter (V-F, K-M)*6
34VKF50A	Fixed Adapter (V-M. K-F)
41KC-3	Fixed Attenuator 3 dB
41KC-6	Fixed Attenuator 6 dB
41KC-10	Fixed Attenuator 10 dB
41KC-20	Fixed Attenuator 20 dB
41VA-3	Fixed Attenuator 3 dB
41VA-6	Fixed Attenuator 6 dB
41VA-10	Fixed Attenuator 10 dB
41VA-20	Fixed Attenuator 20 dB
J1758A	ISI Board
J1800A	ISI Board V
K261	DC Block
K240C	Precision Power Divider
V240C	Fixed Power divider
J1510A	Pick OFF Tee (K)
J1793A	Pick OFF Tee (V)
K241C	Power Splitter
J1748A	Power Splitter (1.5 GHz to 18 GHz, SMA, using MU195020A × 4 to MU181500B connection)
J1624A	COAXIAL CABLE 0.3 m (18 GHz and SMA)
J1342A	COAXIAL CABLE 0.8 m (APC3.5 connector)
J1439A	Coaxial cable (0.8 m, K connector)
J1625A	Coaxial Cable 1 m (18 GHz, SMA)
J1449A	Measurement kit (J1324A × 2, J1439A × 2, J1625A × 1)
J1550A	Coaxial skew match cable (0.8 m, APC3.5 connector)
J1551A	Coaxial skew match cable (0.8 m, K connector)

Model/Order No.	Name
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K connector)
J1741A	Electrical Length Specified Coaxial Cable (0.8 m, K Connector)
J1789A	Electrical Length Specified Coaxial Cable*6 (0.4 m, V connector)
J1790A	Electrical Length Specified Coaxial Cable*6 (0.8 m, V connector)
J1792A	Skew match pair semirigid cable (V-K connector, MU196020A PPG Output to MU195050A Noise Data Input1)
J1761A	PCIe Reference Clock Cable Kit
Z2025A	PCIe CBB Controller
Z2029A	PCIe Reference Clock Buffer
W3911AE	MP1900A Operation Manual
W3913AE	MX190000A Operation Manual
W3813AE	MX183000A Operation Manual
W3915AE	MU195020/40/50A Operation Manual
W3976AE	MU196020/40A OPERATION MANUAL
B0576A	Blank Panel
B0736A	Front Cover (For MP1900A)
B0737A	Carrying Case (For MP1900A, with B0736A)
B0738A	Rack Mount Kit (For MP1900A)
Z1746A	Stylus
Z0541A	USB Mouse
J0008	GPIB CABLE, 2.0 m
Z0917A	Shielded LAN Cable, 5 m
Z1953A	Gigabit Ethernet Switch (5 Port)
Z0306A	Wrist Strap
Z1964A	Torque Wrench (Right Angle)

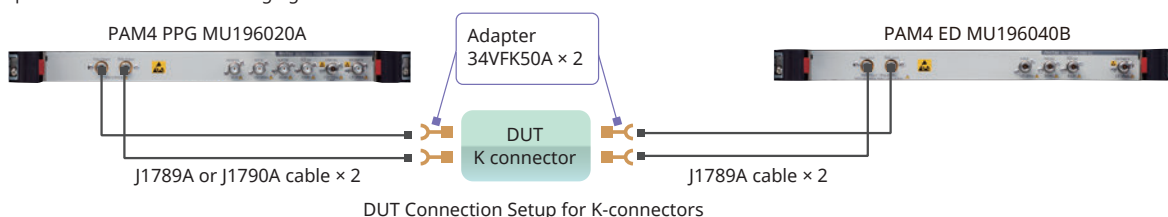## J1815A MP1900A PCIe Measurement Component Set

The following table lists the component set required by the PCIe Gen3/4/5 Tx/Rx LEQ test.

Model/Order No.	Name	Qty.	Application
J1551A	Coaxial skew match cable (0.8 m, K connector)	4	Tx LEQ, Rx LEQ
J1625A	Coaxial cable (1m, SMA connector)	2	Tx LEQ, Rx LEQ
J1510A	Pick OFF Tee	2	Tx LEQ
J1761A	PCIe Reference Clock Cable Kit	2	Tx LEQ, Rx LEQ
K261	DC Block	2	Tx LEQ
K241C	Power Splitter	2	Tx LEQ

*6: We recommend using either the J1789A or J1790A as the coaxial cable for the MU196020A data output. Recommend using coaxial cable J1789A for MU196040B Data IN. The MU196020A data output specifications are defined based on the performance observed using a 70-GHz bandwidth oscilloscope connected as shown below.
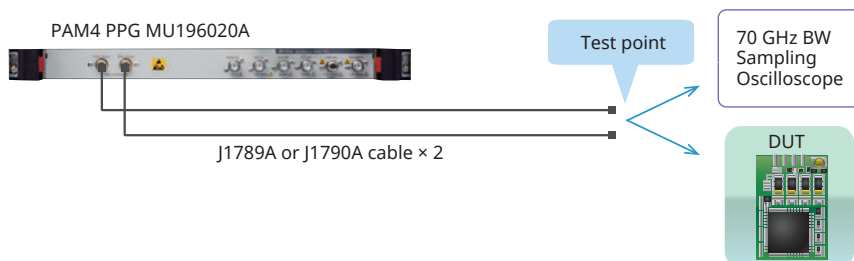
The MU196020A Data OUT and MU196040B Data IN connectors, and the J1789A/J1790A cables all use V-connectors. Consequently, for K-connectors, use 34VFK50A adapters as shown in the following figure.

DUT Connection Setup for K-connectors

Anritsu envision : ensure

Specifications are subject to change without notice.

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