Prime Computer Logic Diagrams

CONTROL PANEL
MEMORIES
MEMORY EXTENDER
LOGIC DIAG. LDS2886

Prime Computer, Incorporated, 145 Pennsylvania Avenue, Framingham, Massachusetts 01701

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CONTROL PANEL
MEMORIES
MEMORY EXTENDER
LOGIC DIAG. LDS2886

DWG NO.	DATE	REV
LDS 2886	2-18-77	A

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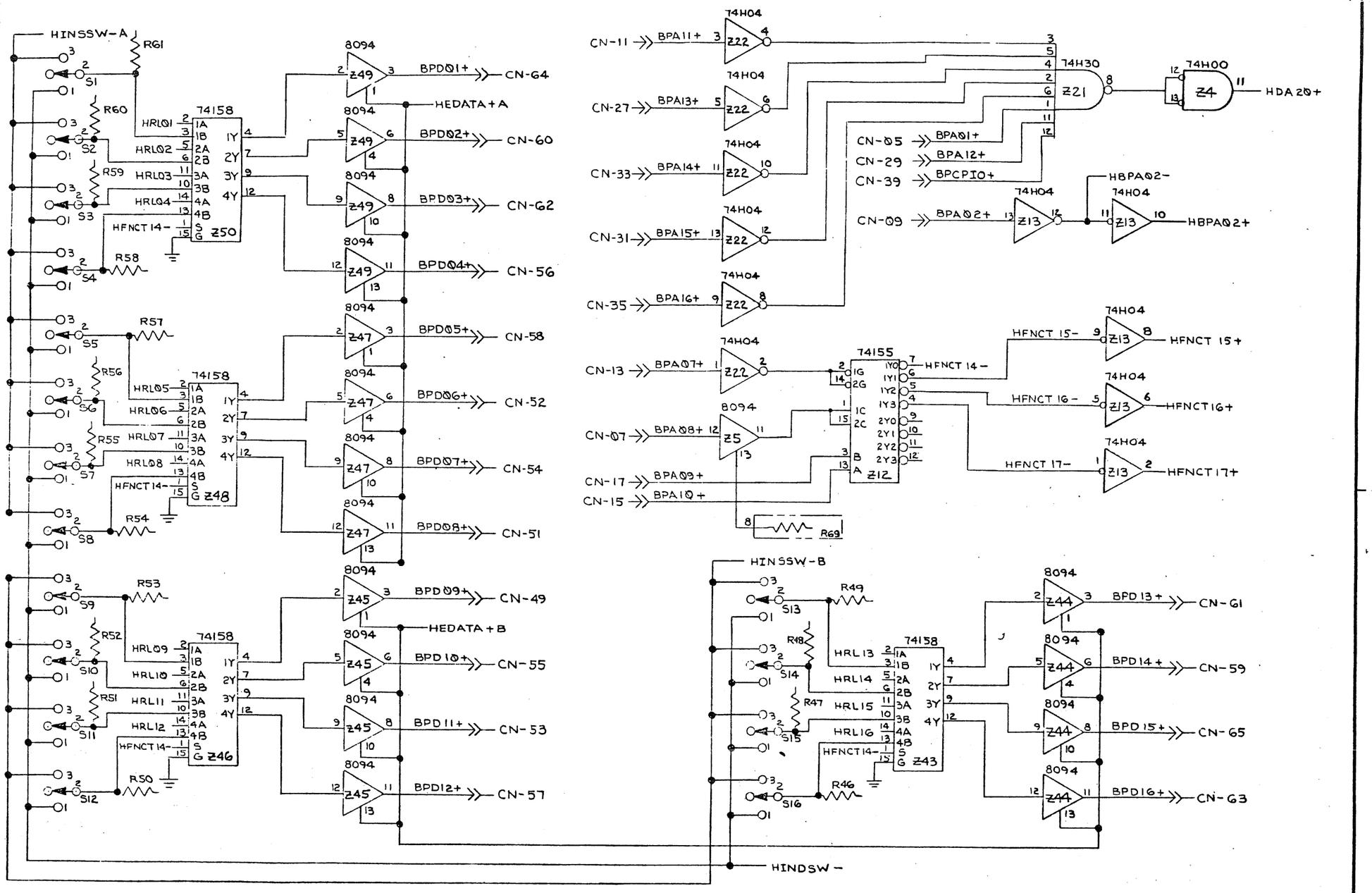
PRIME COMPUTER, INC.



REV	D	C1	C	B	A
1					1223
2					1273
3			✓	✓	1416
4			✓	✓	DOCUMENTATION
ECN					1614
LEVEL					SHEETS AFFECTED

MATERIAL

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES:
- DIMENSIONS ARE IN INCHES
- TOLERANCES

.XX ± .02 .XXX ± .005 ANGLES ± 1/2°

USED ON MECO630
NEXT ASSY PCB0628

DWN BW 4-13-73
CHK
ENG. NRP
APPRD

PRIME COMPUTER, INC.
NATICK, MASS.

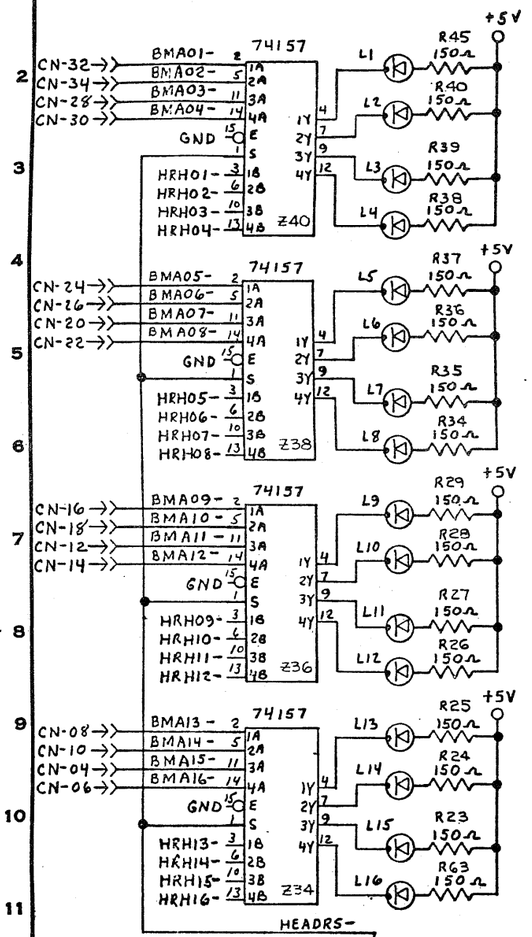
LOGIC CONTROL PANEL
ETCH VERSION

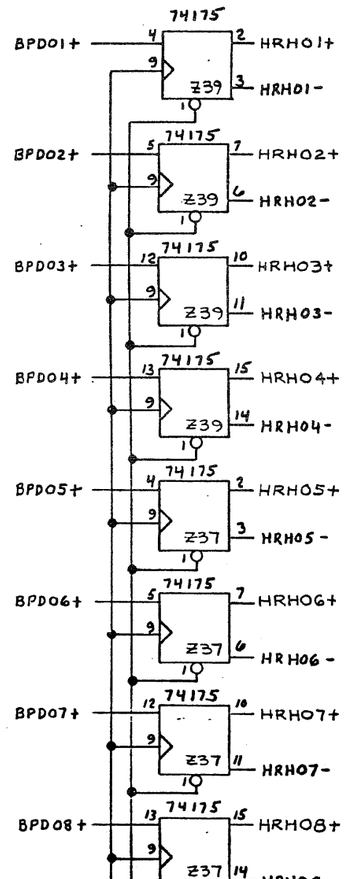
SCALE ~ SIZE C DWG. NO. LRD0620 REV. M-D
SHEET 1 OF 2

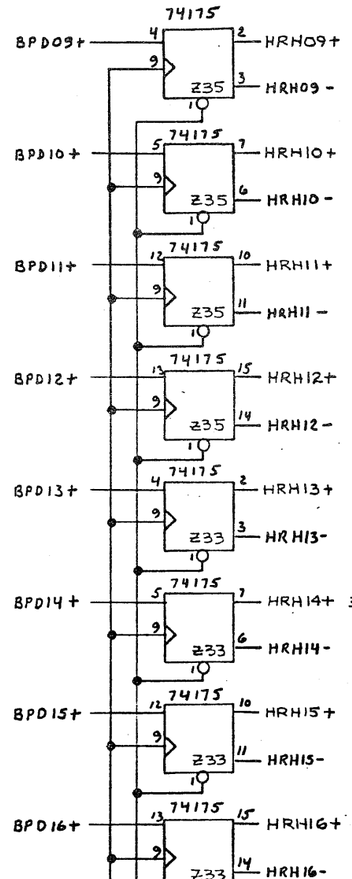
I-1

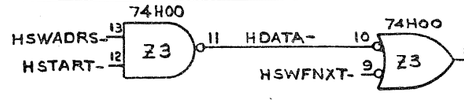
PRIME COMPUTER, INC.

DATA DISPLAY









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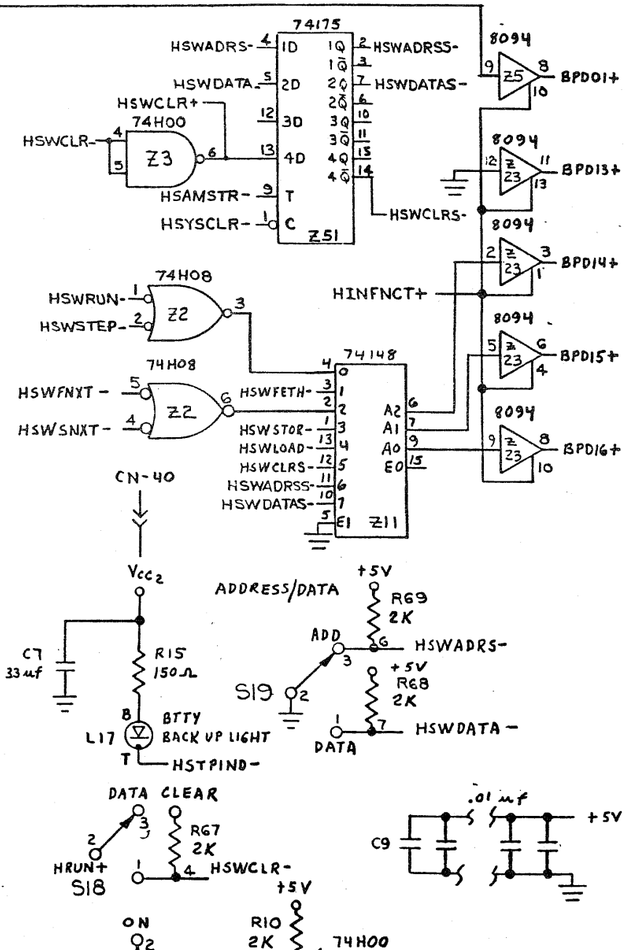
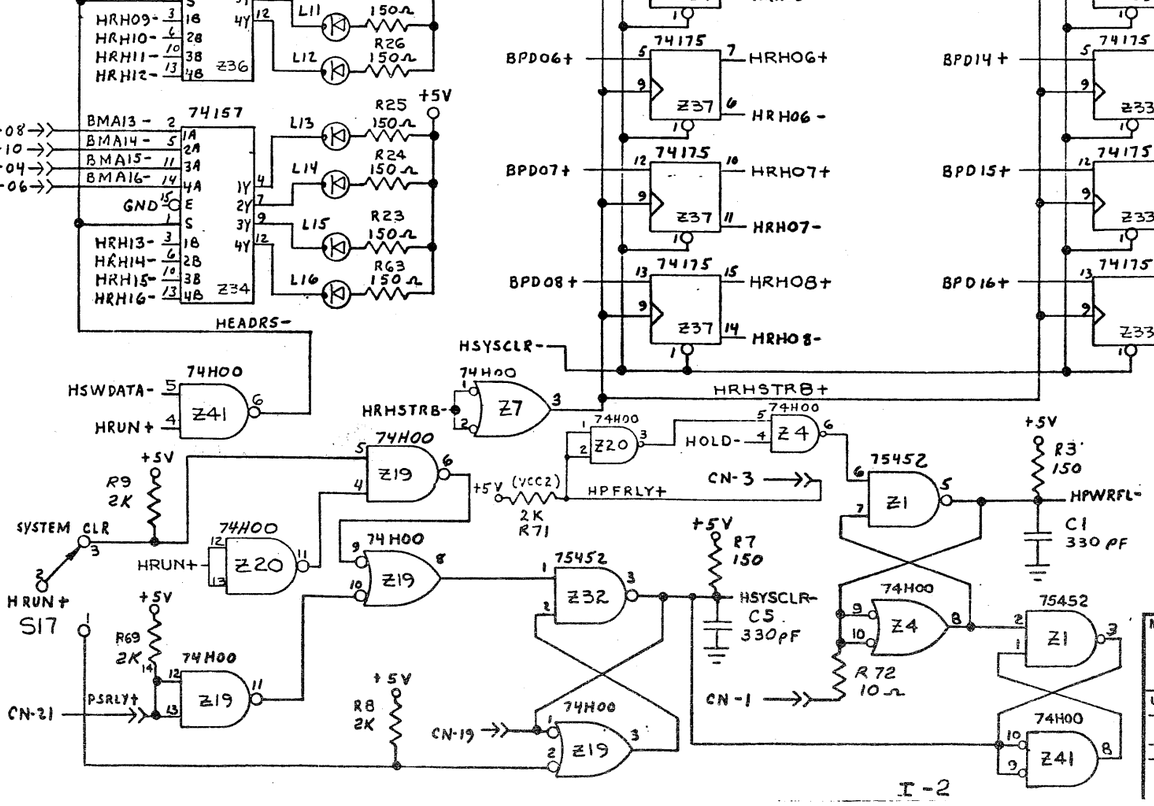
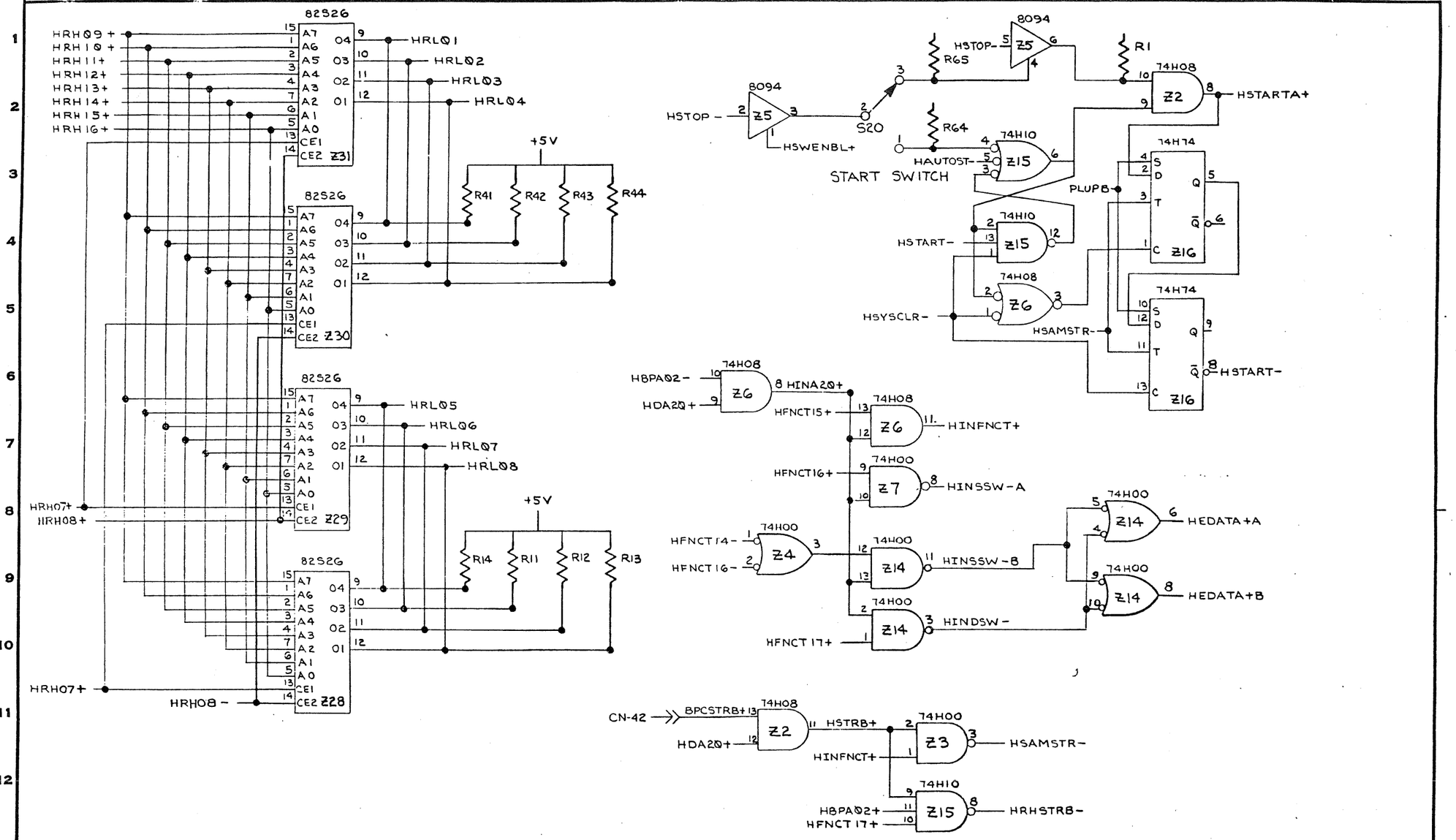




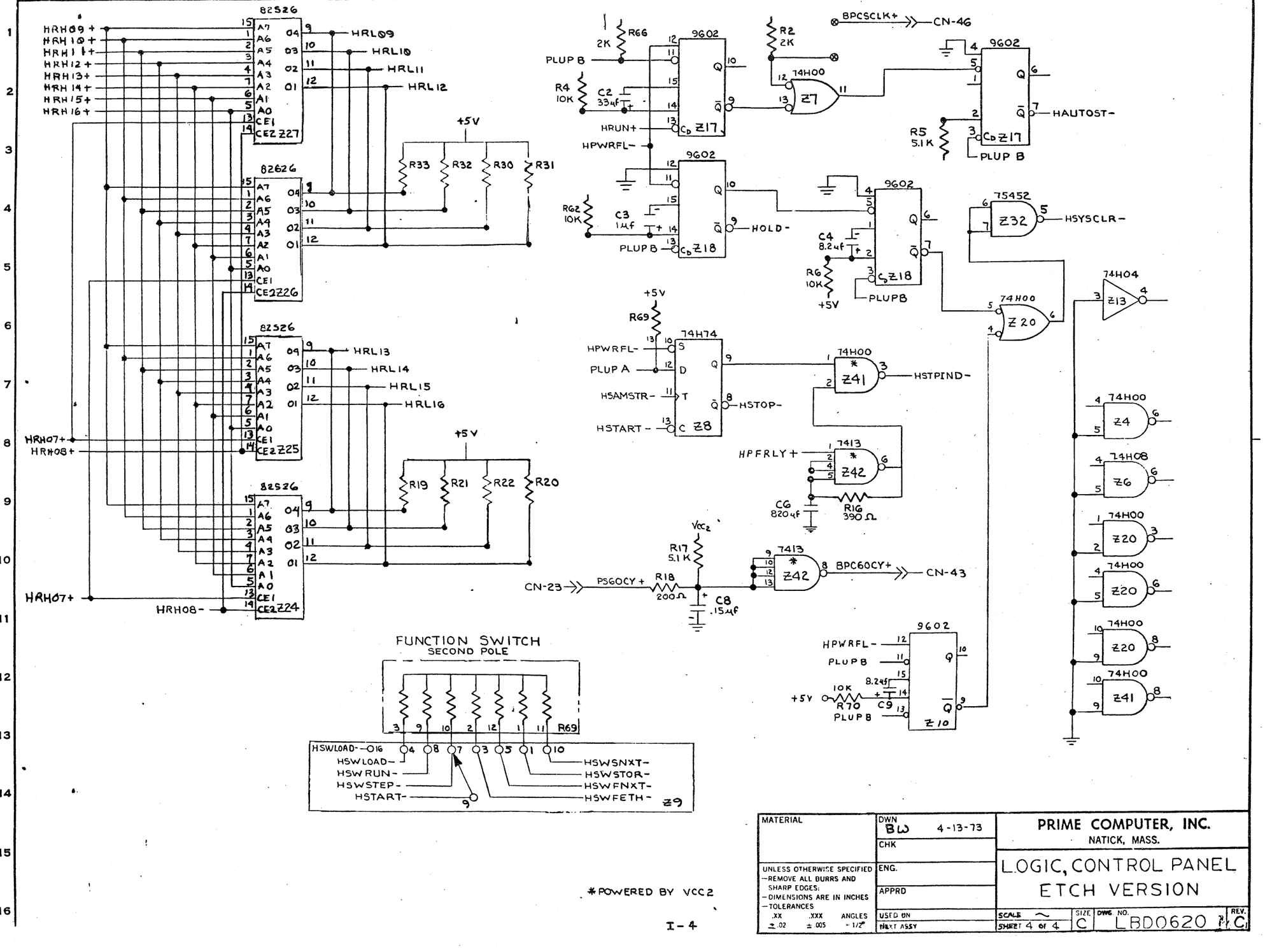
I-2

MATERIAL	DWN JCL 11/2/72	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	LOGIC CONTROL PANEL ETCH VERSION	
	APPRD		
USED ON	SCALE	SIZE C	DWG. NO. LBD0620 REV. D
NEXT ASSY	SHEET 2 OF 4		



MATERIAL	DWN Bw 4-13-73	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	LOGIC, CONTROL PANEL ETCH VERSION	
	APPRD		
	USED ON	SCALE — SIZE C DWG. NO. LBD0620 REV. 13	
	NEXT ASSY	SHEET 3 OF 4	

PRIME COMPUTER, INC.



*POWERED BY VCC2

I-4

MATERIAL	DWN BW 4-13-73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES; –DIMENSIONS ARE IN INCHES –TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	LOGIC, CONTROL PANEL ETCH VERSION
	APPRD	
	USED ON / NEXT ASSY	SCALE ~ SHEET 4 of 4 SIZE C DWG NO. LBD0620 REV. C

MIC 1656 REV D


```
(0001) *      CPBOOT(REV D), AIDS2, MHJ-REG-MHS-MLG, 13 DECEMBER 1974
(0002) *      CONTROL PANEL BOOT PROGRAM
(0003) *      PRIME COMPUTER, INC., SRC0781.003
(0004) *      COPYRIGHT 1974, PRIME COMPUTER, INC., FRAMINGHAM, MASS.
(0005) *
(0006) *
(0007) *
(0008) *
(0009) *      CONTROL PANEL BOOT SENSE SWITCH SETTINGS (X = DON'T CARE)
(0010) *      (EXCEPT FOR THE START BOOT, SS14 - SS16 = 0, SENSE SWITCHES
(0011) *      1 - 10 ARE DEFINED BY THE SECOND LEVEL BOOTS)
(0012) *
(0013) *
(0014) *      SS=11   12   13   14   15   16   ='     MEANING
(0015) *         --   --   --   --   --   --   --     -------
(0016) *          X    X    X    0    0    0   =0     START AT ADDRESS IN SS1 - SS1
(0017) *          X    X    X    0    0    1   =1     ASR PAPER TAPE
(0018) *          X    X    X    0    1    0   =2     HIGH SPEED PAPER TAPE
(0019) *                         0    1    1   =3     FHD (SEE BELOW FOR SS11 - SS1
(0020) *                         1    0    0   =4     MHD (SEE BELOW FOR SS11 - SS1
(0021) *          X         X    1    0    1   =5     MAG TAPE (SS12: 0=9 TRK, 1=7
(0022) *          X    X    X    1    1    0   =6     FLOPPY DISK (DISKETTE)
(0023) *          X    X    X    1    1    1   =7     SPARE
(0024) *
(0025) *
(0026) *      SENSE SWITCHES 11 - 13 FOR DISKS (FHD/MHD, SS14 - SS16 = 3/4)
(0027) *
(0028) *      UNLIKE SENSE SWITCHES 14 - 16 WHICH ARE TREATED AS A THREE DIGIT
(0029) *      BINARY NUMBER (0 - 7), SENSE SWITCHES 11 - 13 FOR DISKS ARE TREATED
(0030) *      AS INDEPENDENT FLAGS.  THEIR MEANINGS ARE AS FOLLOWS:
(0031) *
(0032) *            SS13 = 0: OPTION B
(0033) *                   1: OPTION B'/C
(0034) *            SS12 = 0: OPTION B'/C DEVICE ADDRESS '21
(0035) *                   1: OPTION B'/C DEVICE ADDRESS '23
(0036) *            SS11 = 0: BOOT FROM UPPER SURFACE
(0037) *                   1: BOOT FROM LOWER SURFACE
(0038) *
```



```
(0039) *      NOT ALL COMBINATIONS OF THESE SENSE SWITCHES ARE MEANINGFUL.  FOR F
(0040) *      (SS14 - SS16 = 3), SS11 IS NOT LOOKED AT.  FOR MHD (OPTION B), SS12
(0041) *      IS NOT LOOKED AT.  SPECIFIC COMBINATIONS ARE DEFINED AS FOLLOWS:
(0042) *
(0043) *      FOR FHD (SS14 - SS16 = 3) (X = DON'T CARE)
(0044) *
(0045) *      SS=  11   12   13     MEANING
(0046) *           --   --   --     -------
(0047) *            X    X    0     OPTION B
(0048) *            X    0    1     OPTION B'/C ('21)
(0049) *            X    1    1     OPTION B'/C ('23)
(0050) *
(0051) *      FOR MHD (SS14 - SS16 = 4) (X = DON'T CARE)
(0052) *
(0053) *      SS=  11   12   13     MEANING
(0054) *           --   --   --     -------
(0055) *            0    X    0     OPTION B (UPPER)
(0056) *            1    X    0     OPTION B (LOWER)
(0057) *            0    0    1     OPTION B'/C ('21) (UPPER)
(0058) *            1    0    1     OPTION B'/C ('21) (LOWER=HEAD 2 FOR 20 SUR)
(0059) *            0    1    1     OPTION B'/C ('23) (UPPER)
(0060) *            1    1    1     OPTION B'/C ('23) (LOWER=HEAD 2 FOR 20 SUR)
(0061) *
(0062) *
(0063) *      INITIALIZE LOAD SECTOR TO 0'S
(0064) *
(0065)        D16S
(0066)        ABS
      001000  (0067)        ORG    '1000
001000: 000000 (0068)        BSZ    512             CLEAR SECTOR '1000
001777: 001000 (0069)        ORG    '1000           BEGIN BOOT AT '1000
(0070)        EJCT
```



```
(0071) *      PRE-BOOTSTRAP - LOADS BOOTSTRAP PROGRAM FROM CONTROL PANEL
(0072) *
(0073) *
(0074) *
              001000  (0075) PBS    EQU    *
              177006  (0076) PBD    EQU    6-*
06 001000:    000007  (0077) PB2    DATA   7              MASK BITS
07 001001:    000022  (0078)        DATA   PB4+PBD        PRE-BOOT  STARTING LOCATION
(0079) *
(0080) *      TABLE OF INDIVIDUAL BOOT CONTROL PANEL LOCATIONS
(0081) *                                                          PROM ADDRESS
10 001002:    000051  (0082) PTLOAD DATA   START-PBS       START AT SENSE SWITCH   IN CONTROL PANEL
11 001003:    000057  (0083)        DATA   PTAS-PBS       COMBINED PTR/ASR BOOT
12 001004:    000057  (0084)        DATA   PTAS-PBS       COMBINED PTR/ASR BOOT
13 001005:    000103  (0085)        DATA   ELSES-PBS      DISK, MT, FLOPPY, AND USER BOOTS
(0086) *
(0087) *      PB1 IS A TABLE WITH ONE WORD FOR EACH DEVICE BOOT.
(0088) *      LEFT BYTE IS HSM START FOR BOOT.  RIGHT IS -NUMBER OF LOCATIONS.
(0089) *
14 001006:    121771  (0090) PB1    VFD    6,OVER+PBD,10,START-STE     START AT SENSE SWITCHES (Loc 50, 7 wds)
15 001007:    021754  (0091)        VFD    6,PTLOAD+PBD,10,PTAS-PTASE  PTR/ASR (Loc 10, 24 wds)
16 001010:    021754  (0092)        VFD    6,PTLOAD+PBD,10,PTAS-PTASE  PTR/ASR Loc 10, 24 wds
17 001011:    121524  (0093)        VFD    6,OVER+PBD,10,ELSES-ELSEE   DISK/MT/FLOPPY/USER  Loc 50, 254 wds
(0094) *
(0095) *      MT DMA CHANNEL IN '20 AND '21
(0096) *
20 001012:    004040  (0097) MTRNGE DATA   -(4096-'200-2).LS.4
21 001013:    000200  (0098) MTSTRT DATA   '200
(0099) *
(0100) *      INITIAL BOOT ROUTINE
(0101) *
22 001014: 04.000057A (0102) PB4    STA    '57             PRE-BOOT ENTRY
23 001015:    140010  (0103) KMTPON CRL                    INITIALIZE
24 001016:    131620  (0104)        INA    '1620
25 001017: 03.000006A (0105)        ANA    PB2+PBD
26 001020:    100275  (0106)        SAR    14              SKIP IF < 3
27 001021: 02.000056A (0107)        LDA    PB6+PBD         SET = 3
30 001022: 35.000001A (0108)        LDX    1
```



```
31 001023: 22.000010A (0109)        LDA    PTLOAD+PBD,1
32 001024: 04.000003A (0110)        STA    3
33 001025: 22.000014A (0111)        LDA    PB1+PBD,1
34 001026:    041272  (0112)        LLR    6
35 001027:    040572  (0113)        ARS    6
36 001030: 35.000001A (0114)        LDX    1
(0115) *
(0116) *      PRE-BOOT/BOOT LOADER
(0117) *
37 001031: 02.000003A (0118) PB3    LDA    3
40 001032:    171720  (0119)        OTA    '1720
41 001033: 12.000003A (0120)        IRS    3
42 001034:    131420  (0121)        INA    '1420
43 001035: 44.000002A (0122)        STA*   2
44 001036: 12.000002A (0123)        IRS    2
45 001037:    140114  (0124)        IRX
46 001040: 01.000037A (0125)        JMP    PB3+PBD
47 001041:    131620  (0126)        INA    '1620           INPUT SS'S FOR START AND ELSE BOOTS (NOP FOR P
(0127) *
(0128) *      START OF PAPER TAPE BOOTS
(0129) *
50 001042: 02.000025A (0130) OVER   LDA    OCP4+PTASD      GET OCP INSTRUCTION
51 001043:    101257  (0131)        SNS    16              SKIP IF ASR
52 001044: 07.000056A (0132)        SUB    PB6+PBD         =3, CHANGE TO PTR
53 001045: 04.000002A (0133)        STA    2               SAVE IN B-REG
54 001046: 04.000025A (0134)        STA    OCP4+PTASD      REPLACE INSTRUCTION
55 001047: 01.000020A (0135)        JMP    PASTRT+PTASD    CONTINUE BOOT
56 001050:    000003  (0136) PB6    OCT    3               =3 (MUST BE AT LOCATION '56)
(0137)               FIN                    SHOULD BE NO LITTERALS
(0138)               EJCT
```

```
                                (0139) *       START AT SENSE SWITCH SETTING BOOT
                                (0140) *
                     176777     (0141) STD     EQU     OVER+PBD-*
50  001051: 03.000055A (0142) START   ANA     S1+STD
51  001052:    101040  (0143)         SNZ
52  001053: 41.000056A (0144)         JMP*    STE+STD-1       START AT '1000
53  001054:    001011  (0145)         E64R
54  001055: 41.000001A (0146)         JMP*    1
55  001056:    177700  (0147) S1      DATA    '177700
                        (0148)         FIN                     SHOULD BE NO LITTERALS
                     001060     (0149) STE     EQU     *+1             INCLUDE '1000 FROM PTR/ASR BOOT
                                (0150)         EJCT
```



```
                                (0151) *       COMBINED PTR/ASR PAPER TAPE BOOT
                                (0152) *
                                (0153) *
                     176731     (0154) PTASD   EQU     PTLOAD+PBD-*    (MUST LOAD AT LOCATION '10)
                     001057     (0155) PTAS    EQU     *
(56) 10  001057:     001000     (0156) INA10   OCT     1000            USED AS MASK TO CONVERT INA 4  TO I NA '1004
     11  001060: 01.000010A (0157)         JMP     *-1+PTASD
     12  001061:    141240  (0158)         ICR
     13  001062:    130004  (0159) INA4    INA     4
     14  001063: 01.000013A (0160)         JMP     *-1+PTASD
     15  001064: 24.000000A (0161)         STA     0,1
     16  001065:    140114  (0162)         IRX
     17  001066:    100040  (0163)         SZE
                            (0164) *
                            (0165) *       CONTINUATION POINT OF PAPER TAPE BOOTS
                            (0166) *
     20  001067:    140500  (0167) PASTRT SSM
     21  001070: 04.000013A (0168)         STA     INA4+PTASD      PUT INTO BOOT
     22  001071: 05.000010A (0169)         ERA     INA10+PTASD     FORM INA '100X INSTRUCTION
     23  001072: 04.000003A (0170)         STA     3               PUT INA '100X INTO S-REG
     24  001073: 04.000010A (0171)         STA     INA10+PTASD     PUT INTO BOOT
     25  001074:    030004  (0172) OCP4    OCP     4               INITIALIZE
     26  001075: 04.000026A (0173)         STA     *+PTASD         PUT INA '100X HERE
     27  001076: 01.000026A (0174)         JMP     *-1+PTASD
     30  001077:    101040  (0175)         SNZ
     31  001100: 01.000026A (0176)         JMP     *-3+PTASD
     32  001101: 04.000000A (0177)         STA     0
     33  001102: 01.000010A (0178)         JMP     INA10+PTASD     GO TO BOOT
                            (0179)         FIN                     SHOULD BE NO LITTERALS
                     001103     (0180) PTASE   EQU     *
                            (0181)         EJCT
```



```
                                (0182) *       SELECT PROPER BOOT (DISK, MT, FLOPPY, USER)
                                (0183) *
                     176745     (0184) ELSE    EQU     OVER+PBD-*
50  001103: 03.000006A (0185) ELSES   ANA     PB2+PBD         =7
51  001104: 35.000001A (0186)         LDX     1               USE AS INDEX
52  001105: 21.000050A (0187)         JMP     ELSES+ELSE,1    JUMP INTO JUMP TABLE
53  001106: 01.000143A (0188)         JMP     DISK+ELSE       DISK (FHD)
54  001107: 01.000143A (0189)         JMP     DISK+ELSE       DISK (MHD)
55  001110: 01.000066A (0190)         JMP     MGT10+ELSE      MT
56  001111: 01.000257A (0191)         JMP     FD+ELSE         FLOPPY
                            (0192) *
                            (0193) *       HALT FOR ILLEGAL BOOT AND SUBROUTINE FOR DMA SETUP
                            (0194) *
57  001112:    000000  (0195) SETUP   HLT                     HALT FOR ILLEGAL BOOT
60  001113: 35.000320A (0196)         LDX     C2+ELSE         DMA RANGE ='162000
                            (0197) *
                            (0198) *       ENTRY FOR FLOPPY ALTERNATE RANGE
                            (0199) *
61  001114: 15.000020A (0200) ALTRNG  STX     '20
62  001115: 02.000321A (0201)         LDA     C4+ELSE         DMA START = '770
63  001116: 04.000021A (0202)         STA     '21
64  001117: 02.000245A (0203)         LDA     K20+ELSE        DMA CHANNEL ADDRESS
65  001120: 41.000057A (0204)         JMP*    SETUP+ELSE      RETURN
                            (0205) *
                            (0206)         FIN                     SHOULD BE NO LITTERALS
                            (0207)         EJCT
```



```
                                (0208) *       MAG TAPE BOOTSTRAP
                                (0209) *
66  001121:    031714  (0210) MGT10   OCP     '1714           INITIALIZE
67  001122: 02.000023A (0211)         LDA     KMTPON+PBD      ='10 (LEFT BYTE IGNORED)
70  001123:    170314  (0212)         OTA     '314            POWER ON
71  001124: 01.000070A (0213)         JMP     *-1+ELSE
72  001125: 02.000137A (0214)         LDA     MGT7+ELSE
73  001126:    170114  (0215)         OTA     '114            SPACE FORWARD BETWEEN 3.5 AND 10 INCHES
74  001127: 01.000073A (0216)         JMP     *-1+ELSE
75  001130:    040200  (0217)         LRR     0               DELAY ABOUT 3.5 SEC
76  001131: 12.000254A (0218)         IRS     K0+ELSE
77  001132: 01.000075A (0219)         JMP     *-2+ELSE
100 001133:    031714  (0220)         OCP     '1714           ABORT TRANSFER IF NOT ALREADY STOPPED
101 001134: 02.000245A (0221)         LDA     K20+ELSE        DMA CHANNEL ADDRESS
102 001135:    171414  (0222)         OTA     '1414           CHANNEL
103 001136: 01.000102A (0223)         JMP     *-1+ELSE
104 001137: 02.000141A (0224)         LDA     MGT73+ELSE
105 001140:    170114  (0225)         OTA     '114            REWIND TO LOAD POINT
106 001141: 01.000105A (0226)         JMP     *-1+ELSE
107 001142: 02.000142A (0227)         LDA     MGT74+ELSE
110 001143:    101253  (0228)         SNS     12
111 001144: 02.000140A (0229)         LDA     MGT71+ELSE
112 001145:    170114  (0230)         OTA     '114            READ A RECORD
113 001146: 01.000112A (0231)         JMP     *-1+ELSE
114 001147:    070114  (0232)         SKS     '114
115 001150: 01.000114A (0233)         JMP     *-1+ELSE
116 001151:    101253  (0234)         SNS     12
117 001152: 10.000777A (0235)         JST     '777
120 001153: 35.000136A (0236)         LDX     MGT41+ELSE      COUNT
121 001154: 42.000135A (0237) MGT6    LDA*    MGT4+ELSE
122 001155:    140114  (0238)         IRX
123 001156:    041572  (0239)         ALS     6
124 001157: 45.000135A (0240)         ERA*    MGT4+ELSE
125 001160:    140114  (0241)         IRX
126 001161:    041574  (0242)         ALS     4
127 001162: 45.000135A (0243)         ERA*    MGT4+ELSE
130 001163: 44.000317A (0244)         STA*    C1+ELSE
131 001164: 12.000317A (0245)         IRS     C1+ELSE
```

```
001165:   140114   (0246)        IRX
001166: 01.000121A (0247)        JMP     MGT6+ELSE
001167: 10.000777A (0248)        JST     '777
001170:   047776   (0249) MGT4   DATA    (4096-2).OR.'40000
001171:   170202   (0250) MGT41  DATA    -(4096-'200-2)
001172:   020210   (0251) MGT7   DATA    $2088
001173:   042610   (0252) MGT71  DATA    $4588
001174:   000050   (0253) MGT73  DATA    $28
001175:   040210   (0254) MGT74  DATA    $4088
                   (0255)        FIN                          SHOULD BE NO LITTERALS
                   (0256)        EJCT
```



```
                   (0257) *      DISK BOOTSTRAPS (OPTION B/B'/C MHD/FHD)
                   (0258) *
                   (0259) *
                   (0260) *      SELECT OPTION B VS. OPTION B'/C
                   (0261) *
001176:   100254   (0262) DISK   SNR     13              SKIP FOR OPTION B
001177: 01.000205A (0263)        JMP     BPRIME+ELSE
                   (0264) *
                   (0265) *      STATUS BITS CHECKED:
                   (0266) *          BIT01...END OF CHAIN
                   (0267) *              02...END OF MEDIUM
                   (0268) *              06...WRITE PROTECT VIOLATION
                   (0269) *              07...DEVICE NOT READY
                   (0270) *              08...COMMAND ERROR
                   (0271) *              09...DATA ERROR
                   (0272) *              10...DATA RATE ERROR
                   (0273) *              11...STATUS STACK OVERFLOW
                   (0274) *
001200:   031725   (0275) STRT   OCP     '1725           INITIALIZE
001201:   140040   (0276)        CRA                     MHD UPPER SURFACE SETUP WORD
001202:   100252   (0277)        SNR     11              SKIP FOR UPPER SURFACE
001203: 02.000253A (0278)        LDA     K40+ELSE        HEAD OFFSET = '40
001204:   101255   (0279)        SNS     14              SKIP FOR MHD
001205: 02.000247A (0280)        LDA     K100K+ELSE      ='100000, SELECT FHD
001206:   170025   (0281)        OTA     '25             SLOW SPEED SEEK TO ZERO
001207: 01.000153A (0282)        JMP     *-1+ELSE
                   (0283) *
001210:   140104   (0284)        XCA                     SAVE SETUP WORD
001211:   040640   (0285) DELAY  ARR     32              DELAY AS LONG AS NEEDED FOR SEEK COMPLETE
001212:   141206   (0286)        A1A
001213:   101040   (0287)        SNZ
001214: 01.000145A (0288)        JMP     STRT+ELSE       DISK CYCLING UP
001215:   071025   (0289)        SKS     '1025           IS SEEK COMPLETE
001216: 01.000156A (0290)        JMP     DELAY+ELSE
001217: 10.000057A (0291)        JST     SETUP+ELSE      SETUP DMA CHANNELS
001220:   171425   (0292)        OTA     '1425           DMA CHANNEL ADDRESS
001221: 01.000165A (0293)        JMP     *-1+ELSE        RESTART
001222:   140204   (0294)        XCB                     RETREIVE SETUP WORD
```



```
001223:   170325   (0295)        OTA     '325            READ RCD ZERO
001224: 01.000170A (0296)        JMP     *-1+ELSE
                   (0297) *
001225:   070125   (0298)        SKS     '125            WAIT FOR TRNANSFER TO COMPLETE
001226: 01.000172A (0299)        JMP     *-1+ELSE
                   (0300) *
001227:   130725   (0301)        INA     '725            INPUT STATUS WORD
001230: 01.000174A (0302)        JMP     *-1+ELSE
001231: 03.000204A (0303)        ANA     BMASK+ELSE      ISOLATE ERROR STATUS ='143740
001232:   140024   (0304)        CHS
001233:   100040   (0305) ERRCHK SZE                     IS STATUS OK?
001234: 01.000047A (0306)        JMP     ELSES-1+ELSE    NO - RETRY
                   (0307) *
001235: 10.000777A (0308)        JST     '777            YES - START ***BOOT PROGRAM ***
                   (0309) *
001236:   000004   (0310) K4     OCT     4               =4
001237:   143740   (0311) BMASK  OCT     143740          STATUS ERROR MASK
                   (0312) *
                   (0313)        FIN                     SHOULD BE NO LITTERALS
                   (0314)        EJCT
```



```
                   (0315) *      OPTION B'/C BOOT
                   (0316) *
001240:   101255   (0317) BPRIME SNS     14              SKIP FOR MHD
001241: 01.000217A (0318)        JMP     OP23+ELSE       FHD ALL SET UP
001242: 02.000203A (0319)        LDA     K4+ELSE
001243: 05.000250A (0320)        ERA     READ+ELSE       RESET 7 SECTORS TO 3 SECTORS
001244: 04.000250A (0321)        STA     READ+ELSE       REPLACE
001245:   140417   (0322)        LT                      SELECT MHD (=1)
001246: 04.000241A (0323)        STA     SCODE+ELSE      PUT INTO CHANNEL PROGRAM
001247:   141206   (0324)        A1A                     LOWER HEAD OFFSET (=2)
001250:   100252   (0325)        SNR     11              SKIP FOR UPPER
001251: 04.000251A (0326)        STA     DADDR+ELSE      PUT INTO CHANNEL PROGRAM
001252: 02.000256A (0327) OP23   LDA     OTA21+ELSE      OTA START CHANNEL PROGRAM PROTOTYPE
001253:   100253   (0328)        SNR     12              SKIP FOR DEVICE ADDRESS '21
001254:   140304   (0329)        A2A                     MODIFY FOR ADDRESS '23
001255: 04.000230A (0330)        STA     OTA17+ELSE      PUT IN LINE
                   (0331) *
001256:   031721   (0332)        OCP     '1721           INITIALIZE OPTION B'
001257:   031723   (0333)        OCP     '1723           INITIALIZE OPTION C
001260: 10.000057A (0334)        JST     SETUP+ELSE      SETUP DMA CHANNELS
001261: 04.000040A (0335)        STA     '40             CLEAR STATUS
001262: 02.000237A (0336)        LDA     PSEL+ELSE
001263:   170000   (0337) OTA17  OTA     **              START CHANNEL PROGRAM
001264: 01.000230A (0338)        JMP     *-1+ELSE
001265: 02.000040A (0339)        LDA     '40             GET STATUS
001266:   101400   (0340)        SMI                     SKIP IF DONE
001267: 01.000232A (0341)        JMP     *-2+ELSE        KEEP TRYING
001270: 03.000255A (0342)        ANA     BPMASK+ELSE     ISOLATE ERRORS
001271: 01.000200A (0343)        JMP     ERRCHK+ELSE     CHECK STATUS
                   (0344) *
                   (0345) *      CHANNEL PROGRAM
                   (0346) *
001272: 00.000240A (0347) PSEL   DAC     SELECT+ELSE             POINT TO CHANNEL PROGRAM
                   (0348) *
001273:   040000   (0349) SELECT VFD     4,4,1,0,4,0,7,0         SELECT: UNCONDITIONAL
001274:   000400   (0350) SCODE  OCT     400                     FHD SELECT
001275:   174600   (0351)        VFD     4,15,1,1,4,3,7,0        TRANSFER: IF - SEEKING, ERROR
001276: 00.000252A (0352)        DAC     INSTAT+ELSE             TRANSFER ADDRESS
```

```
244 001277:   150600  (0353)        VFD   4,13,1,0,4,3,3,0,4,0  DMA: NOT IF = SEEKING, ERROR
245 001300:   000020  (0354) K20    OCT   '20                   USE CHANNEL '20
246 001301:   030600  (0355)        VFD   4,3,1,0,4,3,7,0       SEEK (0): NOT IF = SEEKING, ERROR
247 001302:   100000  (0356) K100K OCT   100000                SLOW SEEK TO ZERO
250 001303:   050207  (0357) READ   VFD   4,5,5,1,3,0,4,7       READ: NOT IF = ERROR
251 001304:   000000  (0358) DADDR  OCT   0                     DISK ADDRESS
252 001305:   110000  (0359) INSTAT VFD   4,9,1,0,4,0,7,0       STATUS: UNCONDITIONAL
253 001306: 00.000040A (0360) K40    DAC   '40                   STATUS WORD LOCATION
254 001307:   000000  (0361) K0     VFD   4,0,1,0,4,0,7,0       HALT: UNCONDITIONAL
255 001310:   057777  (0362) BPMASK OCT   57777                 STATUS ERROR MASK (NOT USED BY HALT)
                      (0363) *
256 001311:   171721  (0364) OTA21  OTA   '1721          OTA START CHANNEL PROGRAM PROTOTYPE
                      (0365) *
                      (0366)        FIN                 SHOULD BE NO LITTERALS
                      (0367)        EJCT
```



```
                      (0368) *      DISKETTE BOOT
                      (0369) *
                      (0370) *
257 001312:   031712  (0371) FD     OCP   '1712           INITIALIZE
260 001313: 02.000317A (0372)       LDA   C1+ELSE
261 001314:   170212  (0373)       OTA   '212            SELECT UNIT #1
262 001315: 01.000261A (0374)       JMP   *-1+ELSE
                      (0375) *
263 001316:   070112  (0376) LOOP   SKS   '112
264 001317: 01.000263A (0377)       JMP   *-1+ELSE
265 001320:   170012  (0378)       OTA   '12             STEP NEGATIVE TO TK ZERO
266 001321: 01.000265A (0379)       JMP   *-1+ELSE
267 001322:   140110  (0380)       S1A
270 001323:   100040  (0381)       SZE
271 001324: 01.000263A (0382)       JMP   LOOP+ELSE       REPEAT 128 TIMES
                      (0383) *
                      (0384) *    TRACK = ZERO
                      (0385) *
272 001325:   170112  (0386)       OTA   '112            STEP POSITIVE TO TK ONE
273 001326: 01.000272A (0387)       JMP   *-1+ELSE
                      (0388) *
274 001327: 12.000255A (0389)       IRS   BPMASK+ELSE     PULSE RANDOM FLAG (MUST START ODD)
275 001330: 02.000255A (0390)       LDA   BPMASK+ELSE     GET RANDOM FLAG
276 001331: 35.000322A (0391)       LDX   C5+ELSE         ALTERNATE RANGE (IBM COMPATIBLE FORMAT)
277 001332:   100277  (0392)       SAR   16              SKIP ON FLAG EVEN (PRIME FORMAT)
300 001333: 01.000061A (0393)       JMP   ALTRNG+ELSE     SETUP DMA WITH ALTERNATE (IBM) R ANGE
301 001334: 10.000057A (0394)       JST   SETUP+ELSE      SETUP DMA (PRIME) RANGE
302 001335:   171412  (0395)       OTA   '1412           DMA CHANNEL
303 001336: 01.000302A (0396)       JMP   *-1+ELSE
                      (0397) *
304 001337: 02.000323A (0398)       LDA   C6+ELSE         TK=1, RCD=1
305 001340:   170312  (0399)       OTA   '312            READ ONE RECORD
306 001341: 01.000305A (0400)       JMP   *-1+ELSE
                      (0401) *
307 001342:   040471  (0402)       LGR   7               REG FILE 2 = STATUS ('401 => 2)
310 001343:   170612  (0403)       OTA   '612            SETUP FOR INA
311 001344: 01.000310A (0404)       JMP   *-1+ELSE
312 001345:   130012  (0405)       INA   '12             INPUT STATUS WORD
```



```
313 001346: 01.000312A (0406)       JMP   *-1+ELSE
314 001347: 05.000317A (0407)       ERA   C1+ELSE         REMOVE NORMAL COMPLETE BIT
315 001350:   141050  (0408)       CAL                   CLEAR EXTRANEOUS STUFF
316 001351: 01.000200A (0409)       JMP   ERRCHK+ELSE     STATUS CHECK
                      (0410) *
317 001352:   000200  (0411) C1     DATA  '200
320 001353:   162000  (0412) C2     DATA  -448 .LS.4
321 001354:   000770  (0413) C4     DATA  '770
322 001355:   176000  (0414) C5     DATA  -64 .LS.4
323 001356:   000401  (0415) C6     DATA  '401            FLOPPY DISK ADDRESS (TK=1, RCD=1)
                      (0416)        FIN                 SHOULD BE NO LITTERALS
                001357 (0417) ELSEE  EQU   *
                001357 (0418)        END
```



```
ALTRNG   001114A 0200 0393
BMASK    001237A 0303 0311
BPMASK   001310A 0342 0362 0389 0390
BPRIME   001240A 0263 0317
C1       001352A 0244 0245 0372 0407 0411
C2       001353A 0196 0412
C4       001354A 0201 0413
C5       001355A 0391 0414
C6       001356A 0398 0415
DADDR    001304A 0326 0358
DELAY    001211A 0285 0290
DISK     001176A 0188 0189 0262
ELSE     176745A 0184 0187 0188 0189 0190 0191 0196 0201 0203
                 0204 0213 0214 0216 0218 0219 0221 0223 0224
                 0226 0227 0229 0231 0233 0236 0237 0240 0243
                 0244 0245 0247 0263 0278 0280 0282 0288 0290
                 0291 0293 0296 0299 0302 0303 0306 0318 0319
                 0320 0321 0323 0326 0327 0330 0334 0336 0338
                 0341 0342 0343 0347 0352 0372 0374 0377 0379
                 0382 0387 0389 0390 0391 0393 0394 0396 0398
                 0400 0404 0406 0407 0409
ELSEE    001357A 0093 0417
ELSES    001103A 0085 0093 0185 0187 0306
ERRCHK   001233A 0305 0343 0409
FD       001312A 0191 0371
INA10    001057A 0156 0169 0171 0178
INA4     001062A 0159 0168
INSTAT   001305A 0352 0359
K0       001307A 0218 0361
K100K    001302A 0280 0356
K20      001300A 0203 0221 0354
K4       001236A 0310 0319
K40      001306A 0278 0360
KMTPON   001015A 0103 0211
LOOP     001316A 0376 0382
MGT10    001121A 0190 0210
MGT4     001170A 0237 0240 0243 0249
MGT41    001171A 0236 0250
```

```
MGT6    001154A 0237  0247
MGT7    001172A 0214  0251
MGT71   001173A 0229  0252
MGT73   001174A 0224  0253
MGT74   001175A 0227  0254
MTRNGE  001012A 0097
MTSTRT  001013A 0098
OCP4    001074A 0130  0134  0172
OP23    001252A 0318  0327
OTA17   001263A 0330  0337
OTA21   001311A 0327  0364
OVER    001042A 0090  0093  0130  0141  0184
PASTRT  001067A 0135  0167
PB1     001006A 0090  0111
PB2     001000A 0077  0105  0185
PB3     001031A 0118  0125
PB4     001014A 0078  0102
PB5     001000A 0075  0082  0083  0084  0085
PB6     001050A 0107  0132  0136
PBD     177006A 0076  0078  0090  0091  0092  0093  0105  0107  0109
                0111  0125  0132  0141  0154  0184  0185  0211
PSEL    001272A 0336  0347
PTAS    001057A 0083  0084  0091  0092  0155
PTASD   176731A 0130  0134  0135  0154  0157  0160  0168  0169  0171
                0173  0174  0176  0178
PTASE   001103A 0091  0092  0180
PTLOAD  001002A 0082  0091  0092  0109  0154
READ    001303A 0320  0321  0357
S1      001056A 0142  0147
SCODE   001274A 0323  0350
SELECT  001273A 0347  0349
SETUP   001112A 0195  0204  0291  0334  0394
START   001051A 0082  0090  0142
STD     176777A 0141  0142  0144
STE     001060A 0090  0144  0149
STRT    001200A 0275  0288
```


0000 ERRORS (PMA-1080.015)

REV H

```
(0001) *      CPBOOT(REV H), AIDS2, MHJ-REG-MHS-JRW-MLG, 7 SEPTEMBER 1976
(0002) *      CONTROL PANEL BOOT PROGRAM
(0003) *      PRIME COMPUTER, INC., SRC0781-005
(0004) *      COPYRIGHT 1974, PRIME COMPUTER, INC., FRAMINGHAM, MASS.
(0005) *
(0006) *
(0007) *
(0008) *      CONTROL PANEL BOOT SENSE SWITCH SETTINGS (X = DON'T CARE)
(0009) *      (EXCEPT FOR THE START BOOT, SS14 - SS16 = 0, SENSE SWITCHES
(0010) *      1 - 10 ARE DEFINED BY THE SECOND LEVEL BOOTS)
(0011) *
(0012) *
(0013) *   SS=10   11   12   13   14   15   16   =*    MEANING
(0014) *     --   --   --   --   --   --   --   --    -------
(0015) *           X    X    X    0    0    0   =0    START AT ADDRESS IN SS1 - S
(0016) *      X    X    X    X    0    0    1   =1    ASR PAPER TAPE
(0017) *      X    X    X    X    0    1    0   =2    HIGH SPEED PAPER TAPE
(0018) *      X                   0    1    1   =3    FHD (SEE BELOW FOR SS11 - S
(0019) *                          1    0    0   =4    MHD (SEE BELOW FOR SS11 - S
(0020) *      X    X         X    1    0    1   =5    MAG TAPE (SS12: 0=9 TRK, 1=
(0021) *      X    X    X    X    1    1    0   =6    FLOPPY DISK (DISKETTE)
(0022) *      X    X    X    X    1    1    1   =7    SPARE
(0023) *
(0024) *
(0025) *      SENSE SWITCHES 11 - 13 FOR DISKS (FHD/MHD, SS14 - SS16 = 3/4)
(0026) *
(0027) *      UNLIKE SENSE SWITCHES 14 - 16 WHICH ARE TREATED AS A THREE DIGIT
(0028) *      BINARY NUMBER (0 - 7), SENSE SWITCHES 11 - 13 FOR DISKS ARE TREATED
(0029) *      AS INDEPENDENT FLAGS.  THEIR MEANINGS ARE AS FOLLOWS:
(0030) *
(0031) *            SS13 = 0: OPTION B
(0032) *                   1: OPTION B* OR STORAGE MODULE
(0033) *            SS12 = 0: OPTION B* DA= *21, STORAGE MODULE DA= *26
(0034) *                   1: OPTION B* DA= *23, STORAGE MODULE DA= *27
(0035) *            SS11 = 0: BOOT FROM UPPER SURFACE
(0036) *                   1: BOOT FROM LOWER SURFACE
(0037) *            SS10 = 0: OPTION B OR B*
(0038) *                   1: STORAGE MODULE
```



```
(0039) *      NOT ALL COMBINATIONS OF THESE SENSE SWITCHES ARE MEANINGFUL.  FOR FH
(0040) *      (SS14 - SS16 = 3), SS11 IS NOT LOOKED AT.  FOR MHD (OPTION B), SS12
(0041) *      IS NOT LOOKED AT.  SPECIFIC COMBINATIONS ARE DEFINED AS FOLLOWS:
(0042) *
(0043) *      FOR FHD (SS14 - SS16 = 3) (X = DON'T CARE)
(0044) *
(0045) *      SS=  11   12   13      MEANING
(0046) *           --   --   --      -------
(0047) *            X    X    0      OPTION B
(0048) *            X    0    1      OPTION B* (*21)
(0049) *            X    1    1      OPTION B* (*23)
(0050) *
(0051) *      FOR MHD (SS14 - SS16 = 4) (X = DON'T CARE)
(0052) *
(0053) *      SS=  10   11   12   13      MEANING
(0054) *           --   --   --   --      -------
(0055) *            X    0    X    0      OPTION B (UPPER)
(0056) *            X    1    X    0      OPTION B (LOWER)
(0057) *            0    0    0    1      OPTION B* (*21) (UPPER)
(0058) *            0    1    0    1      OPTION B* (*21) (LOWER=HEAD 2 FOR 20 SUR)
(0059) *            0    0    1    1      OPTION B* (*23) (UPPER)
(0060) *            0    1    1    1      OPTION B* (*23) (LOWER=HEAD 2 FOR 20 SUR)
(0061) *            1    X    0    1      STORAGE MODULE (*26)
(0062) *            1    X    1    1      STORAGE MODULE (*27)
(0063)        EJCT
```



```
(0064) *      IDNT MACROS FOR PROM GENERATION PROGRAM
(0065) *
(0066) *
(0067) *
(0068) IDNT   MAC
(0069) T$I    XSET *
(0070)        (ORG)  *7000
(0071)        NLSM
(0072)        (DATA) %34003
(0073)        (DATA) 511(C*  *)
(0074)        (ORG)  *7001
(0075)        BCI *<1> <2> <3> <4> <5> <6> <7> <8>*
(0076)        LSMD
(0077)        (ORG) T$I
(0078)        ENDM
(0079) *
(0080) *
(0081) *      IDNT FOR THIS REVISION OF THE MICRO-CODE
(0082) *
(0083)        IDNT  (PROM SET BA CONTROL PANEL),(REV H 09-07-76)
(0084)        EJCT
```



```
(0085) *      INITIALIZE LOAD SECTOR TO 0'S
(0086) *
(0087) *
(0088)        D16S
(0089)        ABS
001000C (0090)        ORG   *1000
001000: 000000 (0091)        BSZ   512             CLEAR SECTOR *1000
001777: 001000 (0092)        ORG   *1000           BEGIN BOOT AT *1000
(0093)        EJCT
```

```
                        (0094) *       PRE-BOOTSTRAP - LOADS BOOTSTRAP PROGRAM FROM CONTROL PANEL
                        (0095) *
                        (0096) *
                        (0097) *
            001000      (0098) PB5     EQU    *
            177006      (0099) PBD     EQU    6-*
001000: 06  000007      (0100) PB2     DATA   7              MASK BITS
001001: 07  000022      (0101)         DATA   PB4+PBD        PRE-BOOT  STARTING LOCATION
                        (0102) *
                        (0103) *       TABLE OF INDIVIDUAL BOOT CONTROL PANEL LOCATIONS
                        (0104) *
001002: 10  000051      (0105) PTLOAD  DATA   START-PB5      START AT SENSE SWITCH
001003: 11  000057      (0106)         DATA   PTAS-PB5       COMBINED PTR/ASR BOOT
001004: 12  000057      (0107)         DATA   PTAS-PB5       COMBINED PTR/ASR BOOT
001005: 13  000103      (0108)         DATA   ELSES-PB5      DISK, MT, FLOPPY, AND USER BOOTS
                        (0109) *
                        (0110) *       PB1 IS A TABLE WITH ONE WORD FOR EACH DEVICE BOOT.
                        (0111) *       LEFT BYTE IS HSM START FOR BOOT.  RIGHT IS -NUMBER OF LOCATIONS.
                        (0112) *
001006: 14  121771      (0113) PB1     VFD    6,OVER+PBD,10,START-STE      START AT SENSE SWITCHES
001007: 15  021754      (0114)         VFD    6,PTLOAD+PBD,10,PTAS-PTASE   PTR/ASR
001010: 16  021754      (0115)         VFD    6,PTLOAD+PBD,10,PTAS-PTASE   PTR/ASR
001011: 17  121503      (0116)         VFD    6,OVER+PBD,10,ELSES-ELSEE    DISK/MT/FLOPPY/USER
                        (0117) *
                        (0118) *       MT DMA CHANNEL IN '20 AND '21
                        (0119) *
001012: 20  004040      (0120) MTRNGE  DATA   -(4096-'200-2).LS.4
001013: 21  000200      (0121) MTSTRT  DATA   '200
                        (0122) *
                        (0123) *       INITIAL BOOT ROUTINE
                        (0124) *
001014: 22  04.000057A  (0125) PB4     STA    '57            PRE-BOOT ENTRY
001015: 23  140010      (0126) KMTPON  CRL                   INITIALIZE
001016: 24  131620      (0127)         INA    '1620
001017: 25  03.000006A  (0128)         ANA    PB2+PBD
001020: 26  100275      (0129)         SAR    14             SKIP IF < 3
001021: 27  02.000056A  (0130)         LDA    PB6+PBD        SET = 3
001022: 30  35.000001A  (0131)         LDX    1
```



```
001023: 31  22.000010A  (0132)         LDA    PTLOAD+PBD,1
001024: 32  04.000003A  (0133)         STA    3
001025: 33  22.000014A  (0134)         LDA    PB1+PBD,1
001026: 34    041272    (0135)         LLR    6
001027: 35    040572    (0136)         ARS    6
001030: 36  35.000001A  (0137)         LDX    1
                        (0138) *
                        (0139) *       PRE-BOOT/BOOT LOADER
                        (0140) *
001031: 37  02.000003A  (0141) PB3     LDA    3
001032: 40    171720    (0142)         OTA    '1720
001033: 41  12.000003A  (0143)         IRS    3
001034: 42    131420    (0144)         INA    '1420
001035: 43  44.000002A  (0145)         STA*   2
001036: 44  12.000002A  (0146)         IRS    2
001037: 45    140114    (0147)         IRX
001040: 46  01.000037A  (0148)         JMP    PB3+PBD
001041: 47    131620    (0149)         INA    '1620          INPUT SS'S FOR START AND ELSE BOOTS (NOP FOR P
                        (0150) *
                        (0151) *       START OF PAPER TAPE BOOTS
                        (0152) *
001042: 50  02.000025A  (0153) OVER    LDA    OCP4+PTASD     GET OCP INSTRUCTION
001043: 51    101257    (0154)         SNS    16             SKIP IF ASR
001044: 52  07.000056A  (0155)         SUB    PB6+PBD        =3, CHANGE TO PTR
001045: 53  04.000002A  (0156)         STA    2              SAVE IN B-REG
001046: 54  04.000025A  (0157)         STA    OCP4+PTASD     REPLACE INSTRUCTION
001047: 55  01.000020A  (0158)         JMP    PASTRT+PTASD   CONTINUE BOOT
001050: 56    000003    (0159) PB6     OCT    3              =3 (MUST BE AT LOCATION '56)
                        (0160)         FIN                   SHOULD BE NO LITTERALS
                        (0161)         EJCT
```



```
                        (0162) *       START AT SENSE SWITCH SETTING BOOT
                        (0163) *
            176777      (0164) STD     EQU    OVER+PBD-*
001051: 50  03.000055A  (0165) START   ANA    S1+STD
001052: 51    101040    (0166)         SNZ
001053: 52  41.000056A  (0167)         JMP*   STE+STD-1      START AT '1000
001054: 53    001011    (0168)         E64R
001055: 54  41.000001A  (0169)         JMP*   1
001056: 55    177700    (0170) S1      DATA   '177700
                        (0171)         FIN                   SHOULD BE NO LITTERALS
            001060      (0172) STE     EQU    **1            INCLUDE '1000 FROM PTR/ASR BOOT
                        (0173)         EJCT
```



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                        (0174) *       COMBINED PTR/ASR PAPER TAPE BOOT
                        (0175) *
                        (0176) *
            176731      (0177) PTASD   EQU    PTLOAD+PBD-*   (MUST LOAD AT LOCATION '10)
            001057      (0178) PTAS    EQU    *
001057: 57  001000      (0179) INA10   OCT    1000           USED AS MASK TO CONVERT INA 4  TO INA '1004
001060: 10  01.000010A  (0180)         JMP    *-1+PTASD
001061: 11    141240    (0181)         ICR
001062: 12    130004    (0182) INA4    INA    4
001063: 13  01.000013A  (0183)         JMP    *-1+PTASD
001064: 14  24.000000A  (0184)         STA    0,1
001065: 15    140114    (0185)         IRX
001066: 16    100040    (0186)         SZE
                        (0187) *
                        (0188) *       CONTINUATION POINT OF PAPER TAPE BOOTS
                        (0189) *
001067: 17    140500    (0190) PASTRT  SSM                    CONVERT TO INA
001070: 20  04.000013A  (0191)         STA    INA4+PTASD     PUT INTO BOOT
001071: 21  05.000010A  (0192)         ERA    INA10+PTASD    FORM INA '100X INSTRUCTION
001072: 22  04.000003A  (0193)         STA    3              PUT INA '100X INTO S-REG
001073: 23  04.000010A  (0194)         STA    INA10+PTASD    PUT INTO BOOT
001074: 24    030004    (0195) OCP4    OCP    4              INITIALIZE
001075: 25  04.000026A  (0196)         STA    *+PTASD        PUT INA '100X HERE
001076: 26  01.000026A  (0197)         JMP    *-1+PTASD
001077: 27    101040    (0198)         SNZ
001100: 30  01.000026A  (0199)         JMP    *-3+PTASD
001101: 31  04.000000A  (0200)         STA    0
001102: 32  01.000010A  (0201)         JMP    INA10+PTASD    GO TO BOOT
                        (0202)         FIN                   SHOULD BE NO LITTERALS
            001103      (0203) PTASE   EQU    *
                        (0204)         EJCT
```

First information on paper tape must be

'20 '004 '010

```
                        (0205) *       SELECT PROPER BOOT (DISK, MT, FLOPPY, USER)
                        (0206) *
              176745    (0207) ELSE    EQU     OVER+PBD-*
001103: 50  03.000006A  (0208) ELSES   ANA     PB2+PBD          =7
001104: 51  35.000001A  (0209)         LDX     1                USE AS INDEX
001105: 52  21.000050A  (0210)         JMP     ELSES+ELSE,1     JUMP INTO JUMP TABLE
001106: 53  01.000144A  (0211)         JMP     DISK+ELSE        DISK (FHD)
001107: 54  01.000144A  (0212)         JMP     DISK+ELSE        DISK (MHD)
001110: 55  01.000066A  (0213)         JMP     MGT10+ELSE       MT
001111: 56  01.000307A  (0214)         JMP     FD+ELSE          FLOPPY
                        (0215) *
                        (0216) *       HALT FOR ILLEGAL BOOT AND SUBROUTINE FOR DMA SETUP
                        (0217) *
001112: 57    000000    (0218) SETUP   HLT                      HALT FOR ILLEGAL BOOT
001113: 60  35.000342A  (0219)         LDX     C2+ELSE          DMA RANGE ='162000
001114: 61  15.000020A  (0220)         STX     '20
001115: 62  02.000343A  (0221)         LDA     C4+ELSE          DMA START = '770
001116: 63  04.000021A  (0222)         STA     '21
001117: 64  02.000247A  (0223)         LDA     K20+ELSE         DMA CHANNEL ADDRESS
001120: 65  41.000057A  (0224)         JMP*    SETUP+ELSE       RETURN
                        (0225) *
                        (0226)         FIN                      SHOULD BE NO LITTERALS
                        (0227)         EJCT
```



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                        (0228) *       MAG TAPE BOOTSTRAP
                        (0229) *
001121: 66    031714    (0230) MGT10   OCP     '1714            INITIALIZE
001122: 67  02.000023A  (0231)         LDA     KMTPON+PBD       ='10 (LEFT BYTE IGNORED)
001123: 70    170314    (0232)         OTA     '314             POWER ON
001124: 71  01.000070A  (0233)         JMP     *-1+ELSE
001125: 72  02.000137A  (0234)         LDA     MGT7+ELSE
001126: 73    170114    (0235)         OTA     '114             SPACE FORWARD BETWEEN 3.5 AND 10 INCHES
001127: 74  01.000073A  (0236)         JMP     *-1+ELSE
001130: 75    040200    (0237)         LRR     0                DELAY ABOUT 3.5 SEC
001131: 76  12.000260A  (0238)         IRS     K0+ELSE
001132: 77  01.000075A  (0239)         JMP     *-2+ELSE
001133:100    031714    (0240)         OCP     '1714            ABORT TRANSFER IF NOT ALREADY STOPPED
001134:101  02.000247A  (0241)         LDA     K20+ELSE         DMA CHANNEL ADDRESS
001135:102    171414    (0242)         OTA     '1414            CHANNEL
001136:103  01.000102A  (0243)         JMP     *-1+ELSE
001137:104  02.000141A  (0244)         LDA     MGT73+ELSE
001140:105    170114    (0245)         OTA     '114             REWIND TO LOAD POINT
001141:106  01.000105A  (0246)         JMP     *-1+ELSE
001142:107  02.000142A  (0247)         LDA     MGT74+ELSE
001143:110    101253    (0248)         SNS     12
001144:111  02.000140A  (0249)         LDA     MGT71+ELSE
001145:112    170114    (0250)         OTA     '114             READ A RECORD
001146:113  01.000112A  (0251)         JMP     *-1+ELSE
001147:114    070114    (0252)         SKS     '114
001150:115  01.000114A  (0253)         JMP     *-1+ELSE
001151:116    101253    (0254)         SNS     12
001152:117  10.000777A  (0255)         JST     '777
001153:120  35.000136A  (0256)         LDX     MGT41+ELSE       COUNT
001154:121  42.000135A  (0257) MGT6    LDA*    MGT4+ELSE
001155:122    140114    (0258)         IRX
001156:123    041572    (0259)         ALS     6
001157:124  45.000135A  (0260)         ERA*    MGT4+ELSE
001160:125    140114    (0261)         IRX
001161:126    041574    (0262)         ALS     4
001162:127  45.000135A  (0263)         ERA*    MGT4+ELSE
001163:130  44.000143A  (0264)         STA*    C1+ELSE
001164:131  12.000143A  (0265)         IRS.    C1+ELSE
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001165: 132   140114    (0266)         IRX
001166: 133 01.000121A  (0267)         JMP     MGT6+ELSE
001167: 134 10.000777A  (0268)         JST     '777
001170: 135   047776    (0269) MGT4    DATA    (4096-2).OR.'40000
001171: 136   170202    (0270) MGT41   DATA    -(4096-'200-2)
001172: 137   020210    (0271) MGT7    DATA    $2088
001173: 140   042610    (0272) MGT71   DATA    $4588
001174: 141   000050    (0273) MGT73   DATA    $28
001175: 142   040210    (0274) MGT74   DATA    $4088
001176: 143   000200    (0275) C1      DATA    '200
                        (0276)         FIN                      SHOULD BE NO LITTERALS
                        (0277)         EJCT
```



```
                        (0278) *       DISK BOOTSTRAPS (OPTION B/B*/C MHD/FHD)
                        (0279) *
                        (0280) *
                        (0281) *       SELECT OPTION B VS. OPTION B*/C
                        (0282) *
001177: 144   100254    (0283) DISK    SNR     13               SKIP FOR OPTION B
001200: 145 01.000205A  (0284)         JMP     BPRIME+ELSE
                        (0285) *
                        (0286) *       STATUS BITS CHECKED:
                        (0287) *           BIT01...END OF CHAIN
                        (0288) *                02...END OF MEDIUM
                        (0289) *                06...WRITE PROTECT VIOLATION
                        (0290) *                07...DEVICE NOT READY
                        (0291) *                08...COMMAND ERROR
                        (0292) *                09...DATA ERROR
                        (0293) *                10...DATA RATE ERROR
                        (0294) *                11...STATUS STACK OVERFLOW
                        (0295) *
001201: 146   031725    (0296) STRT    OCP     '1725            INITIALIZE
001202: 147   140040    (0297)         CRA                      MHD UPPER SURFACE SETUP WORD
001203: 150   100252    (0298)         SNR     11               SKIP FOR UPPER SURFACE
001204: 151 02.000257A  (0299)         LDA     K40+ELSE         HEAD OFFSET = '40
001205: 152   101255    (0300)         SNS     14               SKIP FOR MHD
001206: 153 02.000251A  (0301)         LDA     K100K+ELSE       ='100000, SELECT FHD
001207: 154   170025    (0302)         OTA     '25              SLOW SPEED SEEK TO ZERO
001210: 155 01.000154A  (0303)         JMP     *-1+ELSE
                        (0304) *
001211: 156   140104    (0305)         XCA                      SAVE SETUP WORD
001212: 157   040640    (0306) DELAY   ARR     32               DELAY AS LONG AS NEEDED FOR SEEK COMPLETE
001213: 160   141206    (0307)         A1A
001214: 161   101040    (0308)         SNZ
001215: 162 01.000146A  (0309)         JMP     STRT+ELSE        DISK CYCLING UP
001216: 163   071025    (0310)         SKS     '1025            IS SEEK COMPLETE
001217: 164 01.000157A  (0311)         JMP     DELAY+ELSE
001220: 165 10.000057A  (0312)         JST     SETUP+ELSE       SETUP DMA CHANNELS
001221: 166   171425    (0313)         OTA     '1425            DMA CHANNEL ADDRESS
001222: 167 01.000166A  (0314)         JMP     *-1+ELSE         RESTART
001223: 170   140204    (0315)         XCB                      RETREIVE SETUP WORD
```

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001224: 171   170325   (0316)         OTA     *325            READ RECORD ZERO
001225: 172   01.000171A (0317)       JMP     *-1+ELSE
                       (0318) *
001226: 173    070125  (0319)         SKS     *125            WAIT FOR TRANSFER TO COMPLETE
001227: 174   01.000173A (0320)       JMP     *-1+ELSE
                       (0321) *
001230: 175    130725  (0322)         INA     *725            INPUT STATUS WORD
001231: 176   01.000175A (0323)       JMP     *-1+ELSE
001232: 177   03.000204A (0324)       ANA     BMASK+ELSE      ISOLATE ERROR STATUS =*143740
001233: 200    140024  (0325)         CHS
001234: 201    100040  (0326) ERRCHK  SZE                     IS STATUS OK?
001235: 202   01.000047A (0327)       JMP     ELSES-1+ELSE    NO - RETRY
                       (0328) *
001236: 203   10.000777A (0329)       JST     *777            YES - START ***BOOT PROGRAM ***
                       (0330) *
001237: 204    143740  (0331) BMASK   OCT     143740          STATUS ERROR MASK
                       (0332) *
                       (0333)         FIN                     SHOULD BE NO LITTERALS
                       (0334)         EJCT
```



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                       (0335) *       OPTION B*/C BOOT
                       (0336) *
001240: 205    101255  (0337) BPRIME  SNS     14              SKIP FOR MHD
001241: 206   01.000217A (0338)       JMP     OP23+ELSE       FHD ALL SET UP
001242: 207    140401  (0339)         CMA                     A-REG = 4 FOR MHD ENTRY
001243: 210   03.000254A (0340)       ANA     READ+ELSE       RESET 7 SECTORS TO 3 SECTORS
001244: 211   04.000254A (0341)       STA     READ+ELSE       REPLACE
001245: 212    140417  (0342)         LT                      SELECT MHD (=1)
001246: 213   04.000245A (0343)       STA     SCODE+ELSE      PUT INTO CHANNEL PROGRAM
001247: 214    141206  (0344)         A1A                     LOWER HEAD OFFSET (=2)
001250: 215    100252  (0345)         SNR     11              SKIP FOR UPPER
001251: 216   04.000255A (0346)       STA     DADDR+ELSE      PUT INTO CHANNEL PROGRAM
001252: 217   02.000271A (0347) OP23   LDA     OTA23+ELSE      OTA START CHANNEL PROGRAM PROTOTYPE
001253: 220    100251  (0348)         SNR     10              SKIP FOR OPTION B*
001254: 221   01.000274A (0349)       JMP     SMOD+ELSE       STORAGE MODULE
001255: 222    101253  (0350)         SNS     12              SKIP FOR DEVICE ADDRESS *23
001256: 223    140310  (0351)         S2A                     MODIFY FOR ADDRESS *21
001257: 224   04.000234A (0352)       STA     OTA17+ELSE      PUT IN LINE
                       (0353) *
001260: 225   10.000057A (0354)       JST     SETUP+ELSE      SETUP DMA CHANNELS
001261: 226   04.000040A (0355) BPCON  STA     *40             CLEAR STATUS
001262: 227    031721  (0356)         OCP     *1721           INITIALIZE OPTION B*
001263: 230    031723  (0357)         OCP     *1723
001264: 231    031726  (0358)         OCP     *1726           INITIALIZE STORAGE MODULE
001265: 232    031727  (0359)         OCP     *1727
001266: 233   02.000243A (0360)       LDA     PSEL+ELSE
001267: 234    170000  (0361) OTA17   OTA     **              START CHANNEL PROGRAM
001270: 235   01.000234A (0362)       JMP     *-1+ELSE
001271: 236   02.000040A (0363)       LDA     *40             GET STATUS
001272: 237    101400  (0364)         SMI                     SKIP IF DONE
001273: 240   01.000236A (0365)       JMP     *-2+ELSE        KEEP TRYING
001274: 241   03.000261A (0366)       ANA     BPMASK+ELSE     ISOLATE ERRORS
001275: 242   01.000201A (0367)       JMP     ERRCHK+ELSE     CHECK STATUS
                       (0368) *
                       (0369) *       CHANNEL PROGRAM
                       (0370) *
001276: 243  00.000244A (0371) PSEL    DAC     SELECT+ELSE             POINT TO CHANNEL PROGRAM
                       (0372) *
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001277: 244   040000  (0373) SELECT  VFD     4,4,1,0,4,0,7,0         SELECT: UNCONDITIONAL
001300: 245   000400  (0374) SCODE   OCT     400                     FHD SELECT
001301: 246   150000  (0375)         VFD     4,13,1,0,4,0,3,0,4,0    DMA: UNCONDITIONAL
001302: 247   000020  (0376) K20     OCT     *20                     USE CHANNEL *20
001303: 250   030000  (0377)         VFD     4,3,1,0,4,0,7,0         SEEK (0): NOT IF - UNCONDITIONAL
001304: 251   100000  (0378) K100K   OCT     100000                  SLOW SEEK TO ZERO
001305: 252   074000  (0379) STALL   VFD     4,7,1,1,4,0,7,0         STALL: IF -  (NEVER STALLS)
001306: 253  00.000262A (0380)       DAC     SMODCP+ELSE             TRANSFER ADDRESS (SM READ ORDER)
001307: 254   050207  (0381) READ    VFD     4,5,5,1,3,0,4,7         READ: NOT IF - ERROR
001310: 255   000000  (0382) DADDR   OCT     0                       DISK ADDRESS
001311: 256   110000  (0383) INSTAT  VFD     4,9,1,0,4,0,7,0         STATUS: UNCONDITIONAL
001312: 257  00.000040A (0384) K40    DAC     *40                     STATUS WORD LOCATION
001313: 260   000000  (0385) K0      VFD     4,0,1,0,4,0,7,0         HALT: UNCONDITIONAL
001314: 261   057777  (0386) BPMASK  OCT     57777                   STATUS ERROR MASK (NOT USED BY HALT)
001315: 262   150000  (0387) SMODCP  VFD     4,13,1,0,4,0,3,0,4,0    DMA: UNCONDITIONAL (DESTROYED BY TRANSF
001316: 263   000020  (0388)         OCT     *20                     USE CHANNEL *20
001317: 264   050200  (0389)         VFD     4,5,5,1,7,0             READ: NOT IF - ERROR
001320: 265   000000  (0390)         OCT     0                       OFFSET=TRACK=0
001321: 266   000000  (0391)         OCT     0                       DISK ADDRESS = 0
001322: 267   170000  (0392) TRANS   VFD     4,15,1,0,4,0,7,0        TRANSFER: UNCONDITIONAL
001323: 270  00.000256A (0393)       DAC     INSTAT+ELSE             TRANSFER ADDRESS
                       (0394) *
001324: 271   171723  (0395) OTA23   OTA     *1723           OTA START CHANNEL PROGRAM PROTOTYPE
001325: 272   137400  (0396) SMRNG   OCT     137400          =(-1040_LS_4)
001326: 273   000760  (0397) SMST    OCT     760
                       (0398) *
                       (0399) *       STORAGE MODULE
                       (0400) *
001327: 274  06.000000A (0401) SMOD    ADD     0               X-REG=4 FOR MHD ENTRY (*23 -> *27)
001330: 275   101253  (0402)         SNS     12              SKIP FOR *27
001331: 276   140110  (0403)         S1A                     MODIFY FOR *26
001332: 277  04.000234A (0404)       STA     OTA17+ELSE      STORE IN-LINE
001333: 300  02.000267A (0405)       LDA     TRANS+ELSE      TRANSFER INSTRUCTION
001334: 301  04.000252A (0406)       STA     STALL+ELSE      USE STORAGE MODULE READ ORDER
001335: 302  02.000272A (0407)       LDA     SMRNG+ELSE      STORAGE MODULE RANGE (1040)
001336: 303  04.000020A (0408)       STA     *20             SET UP DMA CHANNEL
001337: 304  02.000273A (0409)       LDA     SMST+ELSE       LARGE RECORD START (*760)
001340: 305  04.000021A (0410)       STA     *21
```



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001341: 306 01.000226A (0411)        JMP     BPCON+ELSE      CONTINUE
                       (0412) *
                       (0413)        FIN                     SHOULD BE NO LITTERALS
                       (0414)        EJCT
```

```
                          (0415) *       DISKETTE BOOT
                          (0416) *
                          (0417) *
001342: 307    031712     (0418) FD      OCP     '1712           INITIALIZE
001343: 310    02.000143A (0419)         LDA     C1+ELSE
001344: 311    170212     (0420)         OTA     '212            SELECT UNIT #1
001345: 312    01.000311A (0421)         JMP     *-1+ELSE
                          (0422) *
001346: 313    070112     (0423) LOOP    SKS     '112
001347: 314    01.000313A (0424)         JMP     *-1+ELSE
001350: 315    170012     (0425)         OTA     '12             STEP NEGATIVE TO TK ZERO
001351: 316    01.000315A (0426)         JMP     *-1+ELSE
001352: 317    140110     (0427)         S1A
001353: 320    100040     (0428)         SZE
001354: 321    01.000313A (0429)         JMP     LOOP+ELSE       REPEAT 128 TIMES
                          (0430) *
                          (0431) *     TRACK = ZERO
                          (0432) *
001355: 322    170112     (0433)         OTA     '112            STEP POSITIVE TO TK ONE
001356: 323    01.000322A (0434)         JMP     *-1+ELSE
                          (0435) *
001357: 324    1C.000057A (0436)         JST     SETUP+ELSE      SETUP DMA (PRIME) RANGE
001360: 325    171412     (0437)         OTA     '1412           DMA CHANNEL
001361: 326    01.000325A (0438)         JMP     *-1+ELSE
                          (0439) *
001362: 327    02.000344A (0440)         LDA     C6+ELSE         TK=1, RCD=1
001363: 330    170312     (0441)         OTA     '312            READ ONE RECORD
001364: 331    01.000330A (0442)         JMP     *-1+ELSE
                          (0443) *
001365: 332    040471     (0444)         LGR     7               REG FILE 2 = STATUS ('401 -> 2)
001366: 333    170612     (0445)         OTA     '612            SETUP FOR INA
001367: 334    01.000333A (0446)         JMP     *-1+ELSE
001370: 335    130012     (0447)         INA     '12             INPUT STATUS WORD
001371: 336    01.000335A (0448)         JMP     *-1+ELSE
001372: 337    05.000143A (0449)         ERA     C1+ELSE         REMOVE NORMAL COMPLETE BIT
001373: 340    141050     (0450)         CAL                     CLEAR EXTRANEOUS STUFF
001374: 341    01.000201A (0451)         JMP     ERRCHK+ELSE     STATUS CHECK
                          (0452) *
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001375: 342    162000     (0453) C2      DATA    -448 -LS-4
001376: 343    000770     (0454) C4      DATA    '770
001377: 344    000401     (0455) C6      DATA    '401            FLOPPY DISK ADDRESS (TK=1, RCD=1)
                          (0456)         FIN                     SHOULD BE NO LITTERALS
               001400     (0457) ELSEE   EQU     *
             0C1400       (0458)         END
```

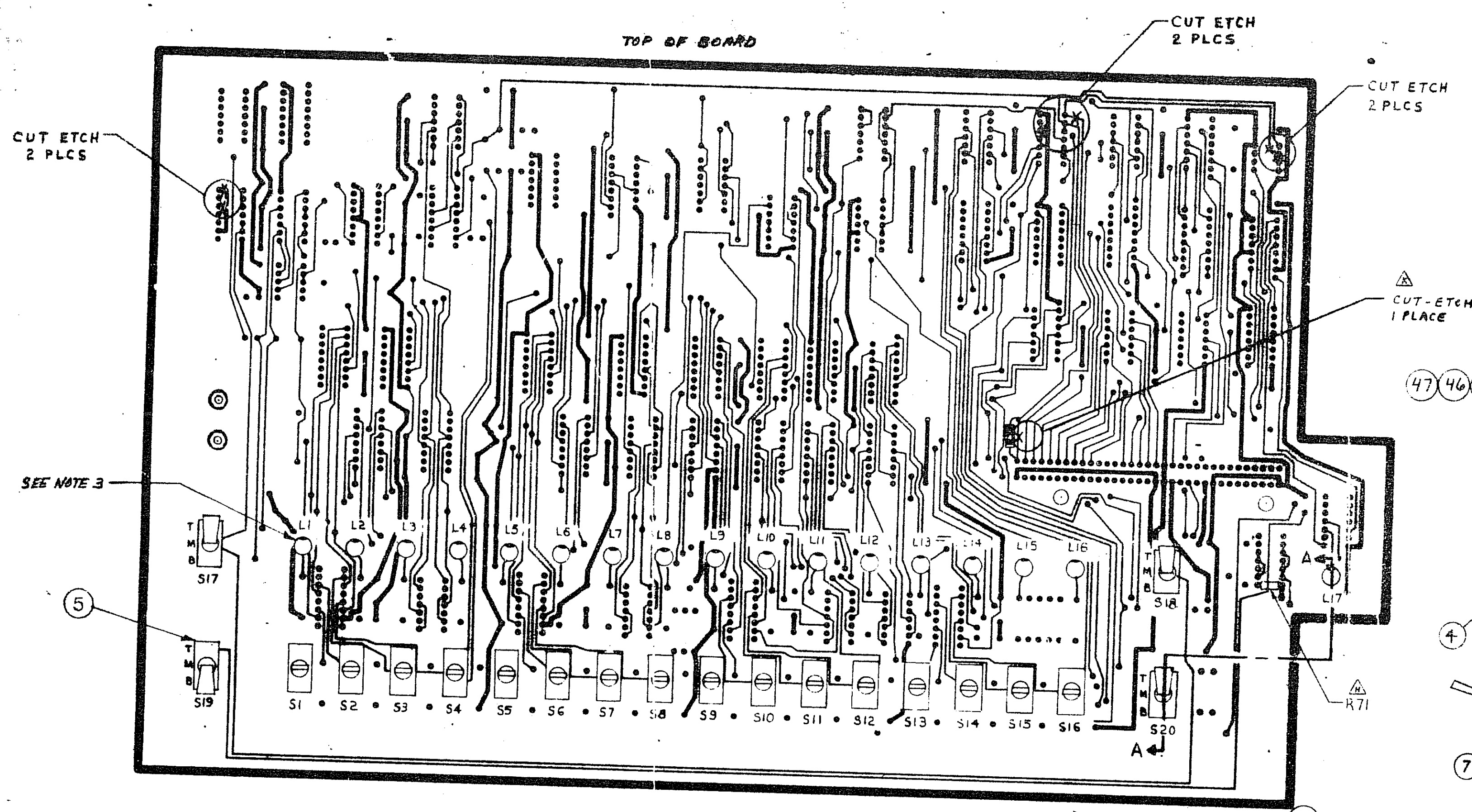


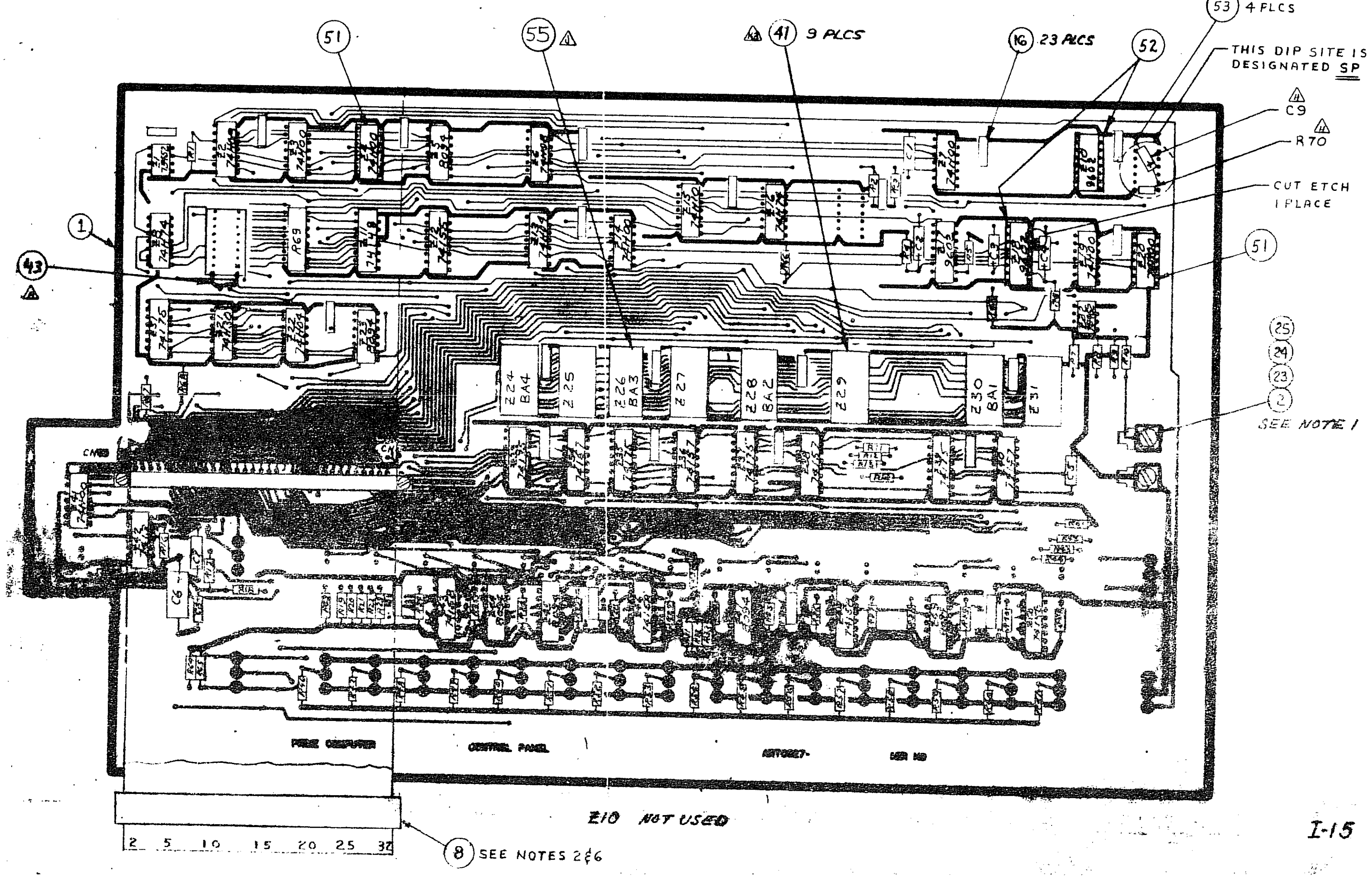
```
BMASK     0C1237A 0324  0331
BPCON     0C1261A 0355  0411
BPMASK    0C1314A 0366  0386
BPRIME    0C1240A 0284  0337
C1        0C1176A 0264  0265  0275  0419  0449
C2        0C1375A 0219  0453
C4        0C1376A 0221  0454
C6        0C1377A 0440  0455
DADDR     0C1310A 0346  0382
DELAY     0C1212A 0306  0311
DISK      0C1177A 0211  0212  0283
ELSE      176745A 0207  0210  0211  0212  0213  0214  0219  0221  0223
                  0224  0233  0234  0236  0238  0239  0241  0243  0244
                  0246  0247  0249  0251  0253  0256  0257  0260  0263
                  0264  0265  0267  0284  0299  0301  0303  0309  0311
                  0312  0314  0317  0320  0323  0324  0327  0338  0340
                  0341  0343  0346  0347  0349  0352  0354  0360  0362
                  0365  0366  0367  0371  0380  0393  0404  0405  0406
                  0407  0409  0411  0419  0421  0424  0426  0429  0434
                  0436  0438  0440  0442  0446  0448  0449  0451
ELSEE     0C1400A 0116  0457
ELSES     0C1103A 0108  0116  0208  0210  0327
ERRCHK    0C1234A 0326  0367  0451
FD        0C1342A 0214  0418
INA10     0C1C57A 0179  0192  0194  0201
INA4      0C1C62A 0182  0191
INSTAT    0C1311A 0383  0393
K0        0C1313A 0238  0385
K100K     0C1304A 0301  0378
K20       0C1302A 0223  0241  0376
K40       0C1312A 0299  0384
KMTPON    0C1015A 0126  0231
LOOP      0C1346A 0423  0429
MGT10     0C1121A 0213  0230
MGT4      0C1170A 0257  0260  0263  0269
MGT41     0C1171A 0256  0270
MGT6      0C1154A 0257  0267
MGT7      0C1172A 0234  0271
```



```
MGT71     0C1173A 0249  0272
MGT73     0C1174A 0244  0273
MGT74     0C1175A 0247  0274
MTRNGE    0C1C12A 0120
MTSTRT    0C1C13A 0121
OCP4      0C1C74A 0153  0157  0195
OP23      0C1252A 0338  0347
OTA17     0C1267A 0352  0361  0404
OTA23     0C1324A 0347  0395
OVER      0C1042A 0113  0116  0153  0164  0207
PASTRT    0C1C67A 0158  0190
PB1       0C1C86A 0113  0134
PB2       0C1C0CA 0100  0128  0208
PB3       0C1C31A 0141  0148
PB4       0C1014A 0101  0125
PB5       0C1C0CA 0096  0105  0106  0107  0108
PB6       0C1C50A 0130  0155  0159
PBD       177006A 0099  0101  0113  0114  0115  0116  0128  0130  0132
                  0134  0148  0155  0164  0177  0207  0208  0231
PSEL      0C1276A 0360  0371
PTAS      0C1C57A 0106  0107  0114  0115  0178
PTASD     176731A 0153  0157  0158  0177  0180  0183  0191  0192  0194
                  0196  0197  0199  0201
PTASE     0C1103A 0114  0115  0203
PTLOAD    0C1C02A 0105  0114  0115  0132  0177
READ      0C1307A 0340  0341  0381
S1        0C1056A 0165  0170
SCODE     0C1300A 0343  0374
SELECT    0C1277A 0371  0373
SETUP     0C1112A 0218  0224  0312  0354  0436
SMOD      0C1327A 0349  0401
SMODCP    0C1315A 0380  0387
SMRNG     0C1325A 0396  0407
SMST      0C1326A 0397  0409
STALL     0C1305A 0379  0406
START     0C1C51A 0105  0113  0165
STD       176777A 0164  0165  0167
STE       0C1C60A 0113  0167  0172
```

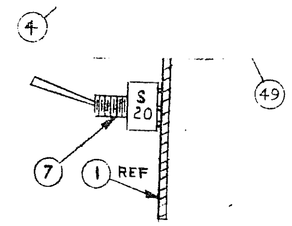
LTR	DATE	REVISION	DR.	CK.
A		RELEASED		
B	8/1/73	ITEM 43 ADDED PER ECN 1187	[illegible]	[illegible]
C	10/2/73	BOM PER ECR 1212	[illegible]	[illegible]
D	10/12/73	BOM PER ECR 1199	[illegible]	[illegible]
E	11/30/73	Z11 FROM 9318 TO 74148 ECN 1223	[illegible]	[illegible]
F	12/15/73	BOM PER ECN 1243	[illegible]	[illegible]
G	4/11/73	PER ECR 1334, 1338, 1362	[illegible]	[illegible]
H	10/16/73	PER ECR 1446, 1465	[illegible]	[illegible]
J	1/23/75	ADD ITEM 55 - ECN 1540 & 1528	PB	[illegible]
K	[illegible]	CUT ETCH & ADD R72 PER ECN 1614	[illegible]	[illegible]
K1	[illegible]	PER ECR 1685	[illegible]	[illegible]
K2	12/31/75	POLARITY DELETED FROM C1 & C5	[illegible]	[illegible]
K3	10-12-76	DELETED ITEM 50 PER ECR 1872	[illegible]	[illegible]





Pin#	Signal	Pin#	Signal	Pin#	Signal
1	HPWRFL-	23	PS60CY+	45	SPARE
2	GND	24	BMA05-	46	BPCSCLK+
3	HPWRFL+	25	SPARE	47	SPARE
4	BMA15-	26	BMA06-	48	-12V
5	BPAØ1+	27	BPA13+	49	BPD09+
6	BMA16-	28	BMA03-	50	GND
7	BPA08+	29	BPA12+	51	BPD08+
8	BMA13-	30	BMA04-	52	BPD06+
9	BPA02+	31	BPA15+	53	BPD11+
10	BMA14-	32	BMAØ1-	54	BPD07+
11	BPA11+	33	BPA14+	55	BPD1Ø+
12	BMA11-	34	BMA02-	56	BPDØ4+
13	BPA07+	35	BPA16+	57	BPD12+
14	BMA12-	36	GND	58	BPDØ5+
15	BPA10+	37	VCC1	59	BPD14+
16	BMA09-	38	VCC1	60	BPD02+
17	BPA09+	39	BPCPIO+	61	BPD13+
18	BMA10-	40	VCC2	62	BPDØ3+
19	HSYSCLR-	41	SPARE	63	BPD16+
20	BMAØ7-	42	BPCSTRB+	64	BPDØ1+
21	PSRLY+	43	BPC60CY+	65	BPD15+
22	BMAØ8-	44	HRUN-	66	GND

Control Panel Connector List



SECTION A-A

JUMPER LIST		
FROM	TO	AWG
CN-3	Z20-1	#30
Z20-1	Z20-2	
Z20-3	Z4-5	
Z4-6	Z1-6	
Z4-4	Z18-9	
Z1-2	Z4-8	
Z18-7	Z20-5	
Z10-9	Z20-4	
Z20-6	Z32-6	
Z10-11	Z10-13	
Z18-3	Z10-11	
Z10-12	Z18-11	
SP-1	SP-2	
SP-8	Z10-15	
SP-1	Z10-14	#30

NOTES:

1. POSITION ITEM 2 AS SHOWN & SOLDER TO PADS.
2. COPPER SHIELD IN ITEM 8, (FLEX CABLE) IS TO BE TOWARDS BOTTOM OF ITEM 1.
3. MOUNT L1-L17 SO THAT DOT (CATHODE) IS TOWARD TOP OF BOARD AS SHOWN.
4. ▭ INDICATES CERAMIC DISC CAPACITOR.
5. ONE JUMPER (ITEM #43) REQUIRED.
6. ITEMS 44, & 49 MUST BE ASSEMBLED TO ITEM 1 BEFORE INSTALLATION OF ITEM 8 TO ITEM 1.

-002	NO PROM
-001	AS SHOWN
-XXX	DESCRIPTION

DWN	[illegible] 5/22/73
CHK	[illegible] 11/19/73
ENG.	[illegible]
APPRD	[illegible]
USED ON	1001-XXX
NEXT ASSY	1001-XXX
SCALE	1/1
SHEET	1 OF 1
SIZE	D
DWG. NO.	MEC0630-XXX
REV.	K3

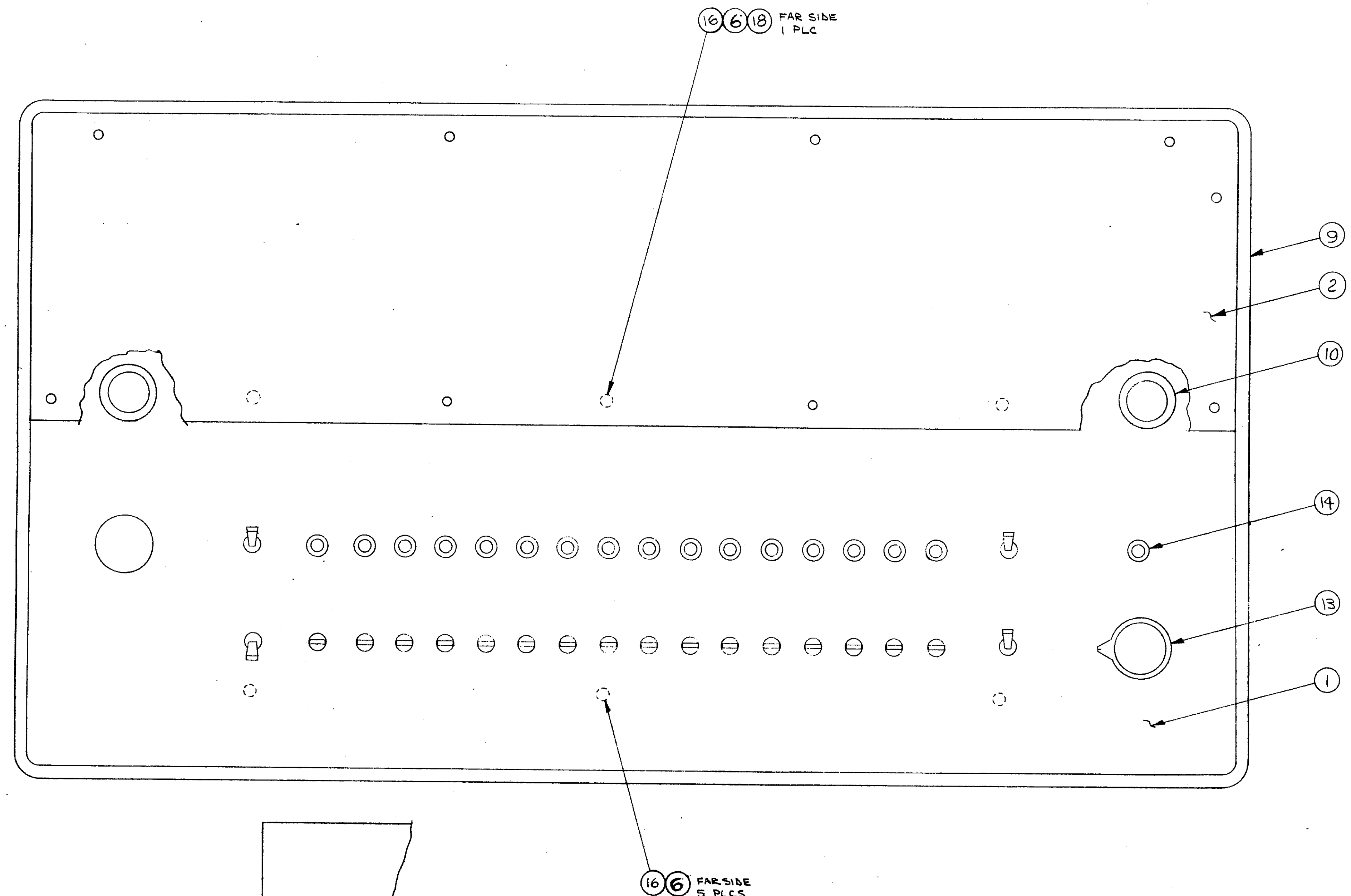
PRIME COMPUTER INC.
NATICK, MASS.

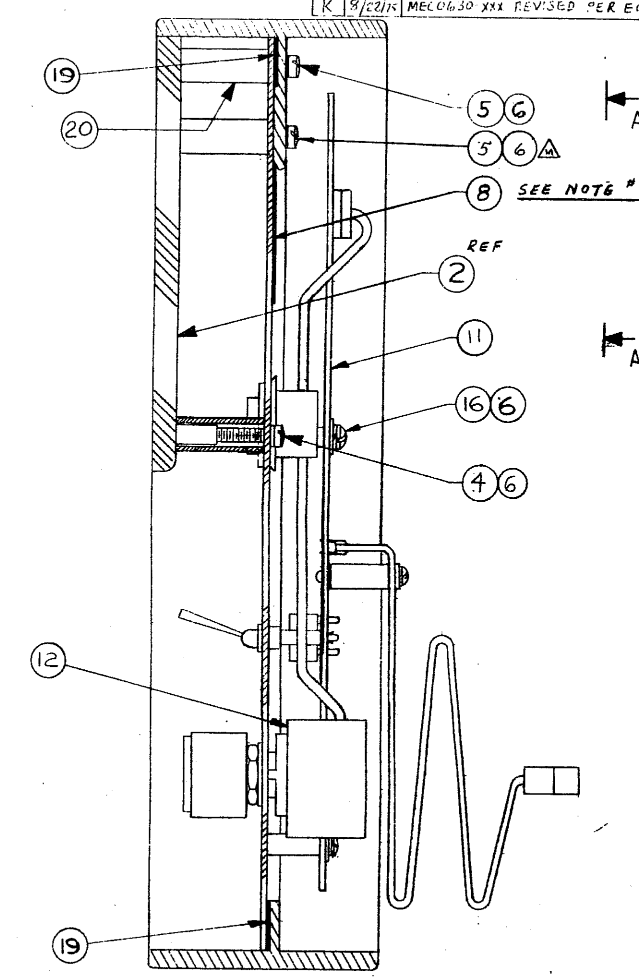
P. C. BOARD SUB-ASSY
CONTROL PANEL

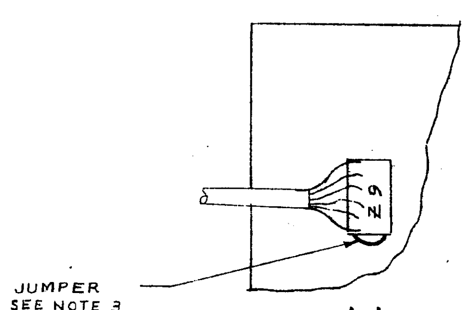
BL

EV.

LTR	DATE	REVISION	DR.	CK.
A	10/11/72	ITEMS #7 & #10 ADDED		
B	11/14/72	ITEM #9, NOTES 1 & 2 ADDED, ITEM #8 DELETED		
C	1/8/73	NO OVERLAY VERSION INC. PER ECN 1071		
D	8/30/73	REVISED PER ECN 1199		
E	12/15/73	BOM PER ECN 1243		
F	[illegible]	[illegible]		
G	[illegible]	[illegible]		
H	[illegible]	PER ECN [illegible], 1482		
J	4/23/75	ADD ITEMS 9-19 PER ECN 1540	PB	
K	8/22/75	MEC0630-XXX REVISED PER ECN 1614		AHP
L	5/5/76	PER ECR 1775	J.T.S.	AHP
M	1-28-77	PER ECR 2030, 2053, 2061		
M1	2/9/77	ADDED -907		







VIEW A-A

NOTES:

1. ATTACH ITEM #8 (NAME PLATE) TO REAR INNER PANEL AS SHOWN. CENTER OVER P.B. CATCH ON THE RIGHT SIDE LOOKING FROM THE REAR.
2. INSTALL ITEMS # 2, 3, 4, 5, 6 & 7 JUST PRIOR TO SHIPMENT TO PREVENT SCRATCHING ETC.
3. REMOVE JUMPER INDICATED ON ALL PRIMES WITHOUT AUTOLOAD.

-XXX	DESCRIPTION	ECN	REV
-907	L/P W/O LOGO		M1
-245	STC	1775	D
-006	L/P W/LOGO	1775	M
-001	STANDARD	1775	M
-000	NO PROM	1775	M

MATERIAL: SEE BOM

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES:
- DIMENSIONS ARE IN INCHES
- TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°

DWN 8-8-72
CHK 10/11/72
ENG.
APPRD
USED ON
NEXT ASSY

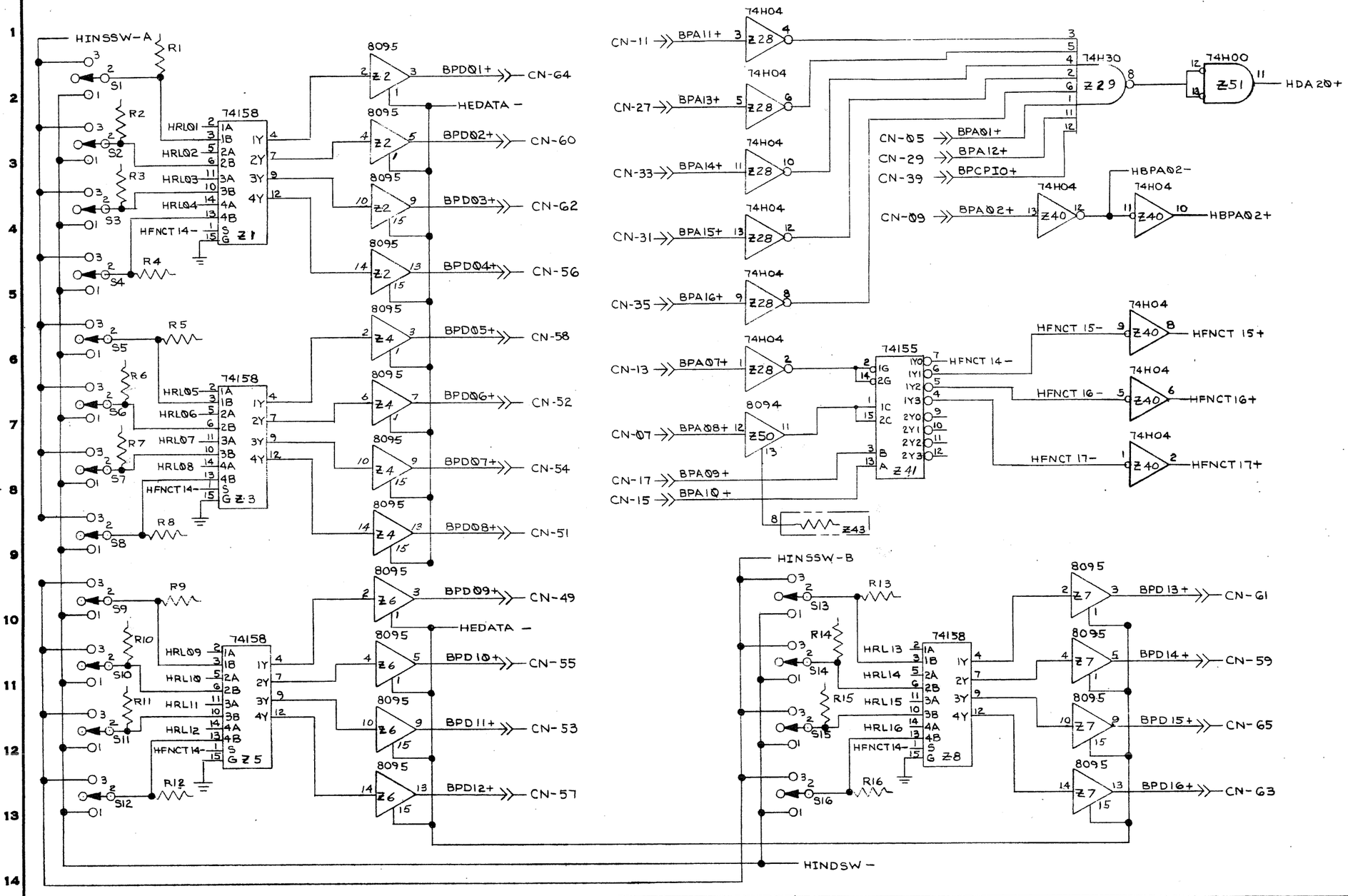
PRIME COMPUTER, INC.
NATICK, MASS.

CONTROL PANEL ASSY

SCALE 1/1 SHEET 1 OF 1 SIZE D DWG. NO. 1001-XXX REV. SEE CHART

16

PRIME COMPUTER, INC.



DWP	A	A	A	A	A	1775	
CK.	REV LEVEL	1	2	3	4	SHEETS AFFECTED	ECN

I-17

MATERIAL

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02 .XXX ±.005 ANGLES ±1/2°

DWN Leslie 5/5/76
CHK 5/18/76
ENG. DWP
APPRD
USED ON
NEXT ASSY

PRIME COMPUTER, INC.
NATICK, MASS.

LOGIC CONTROL PANEL
ETCH VERSION

SCALE ~ SIZE C DWG. NO. LBD2582 REV. A
SHEET 1 OF 4

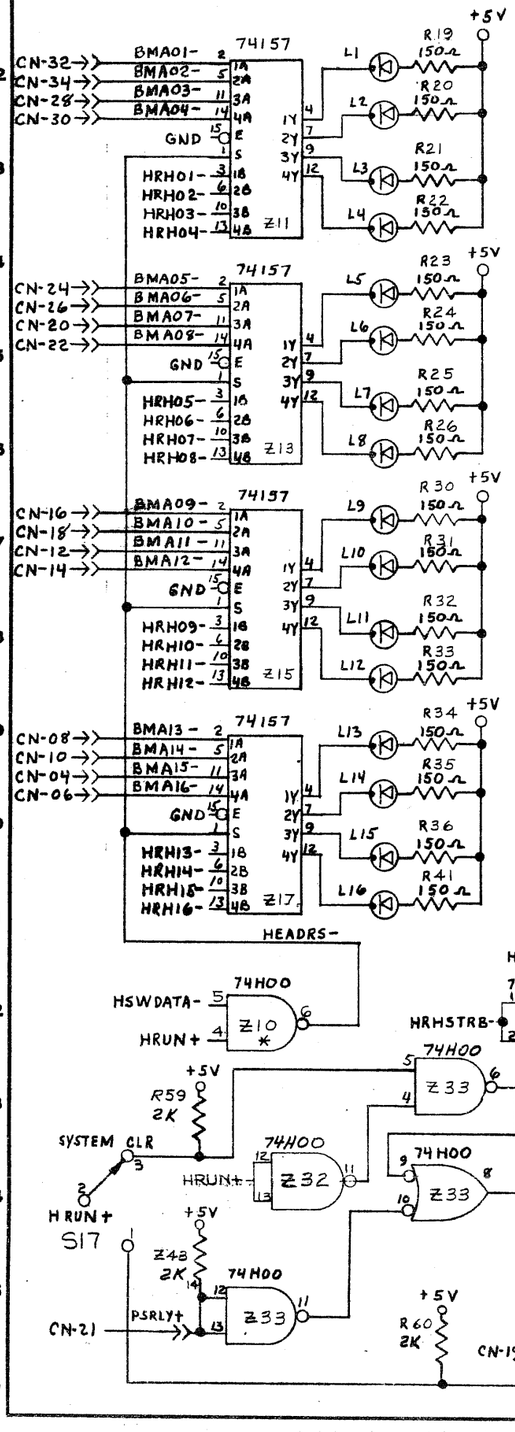
PDF-003

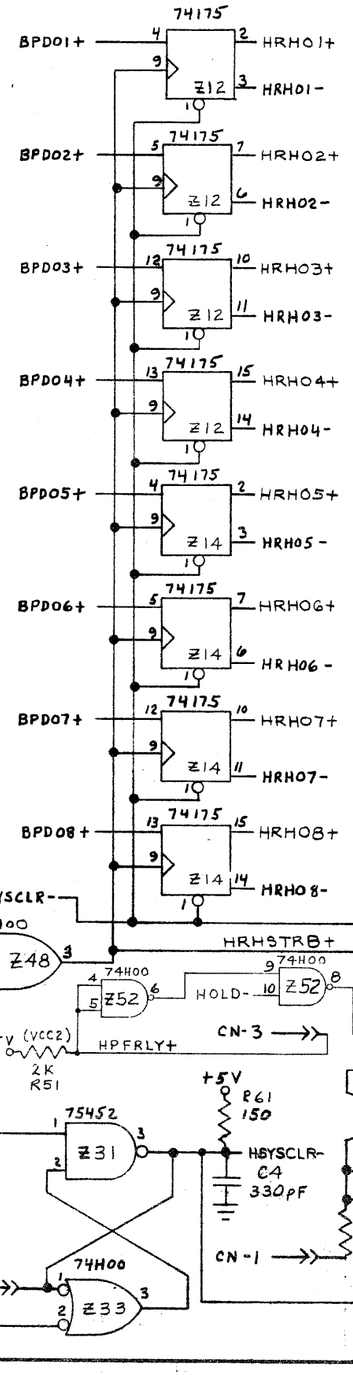
PRIME COMPUTER, INC.

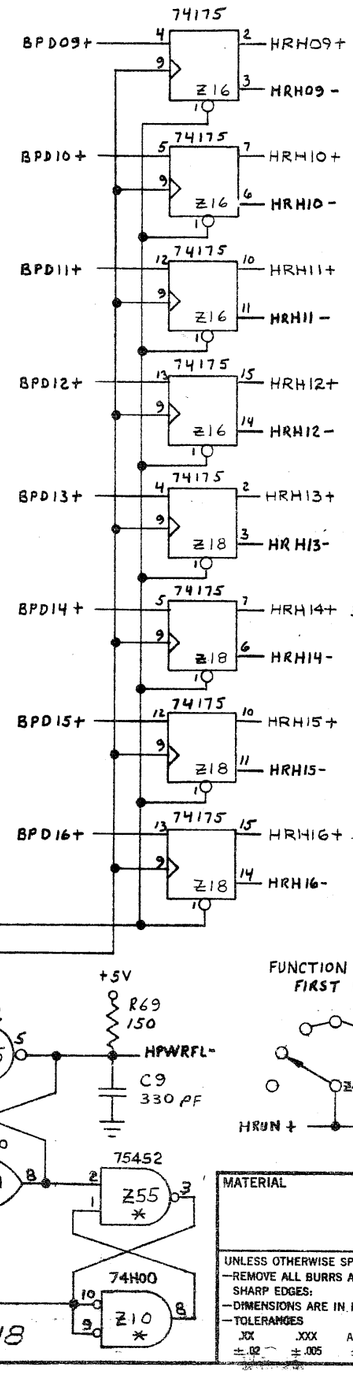
A B C D E F G H J K L M N P R S T V W X Y

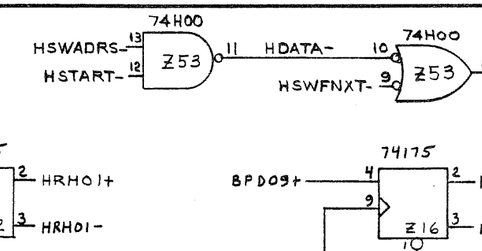
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

DATA DISPLAY

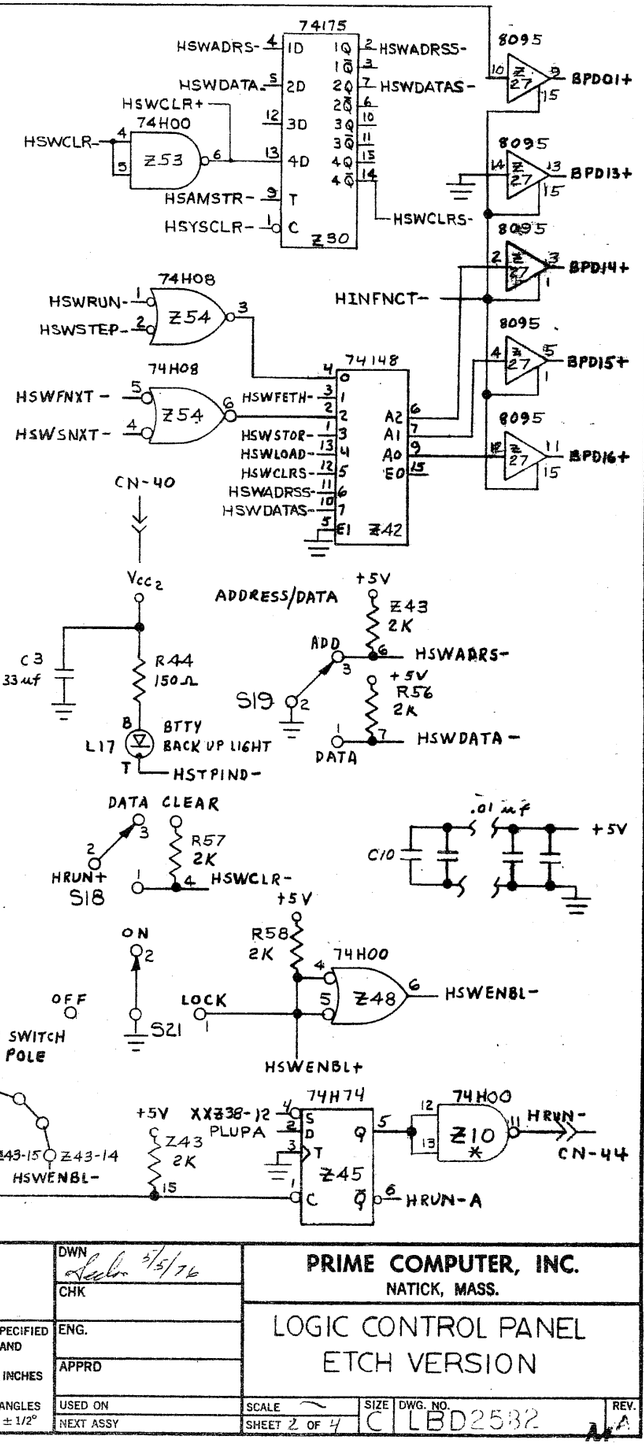




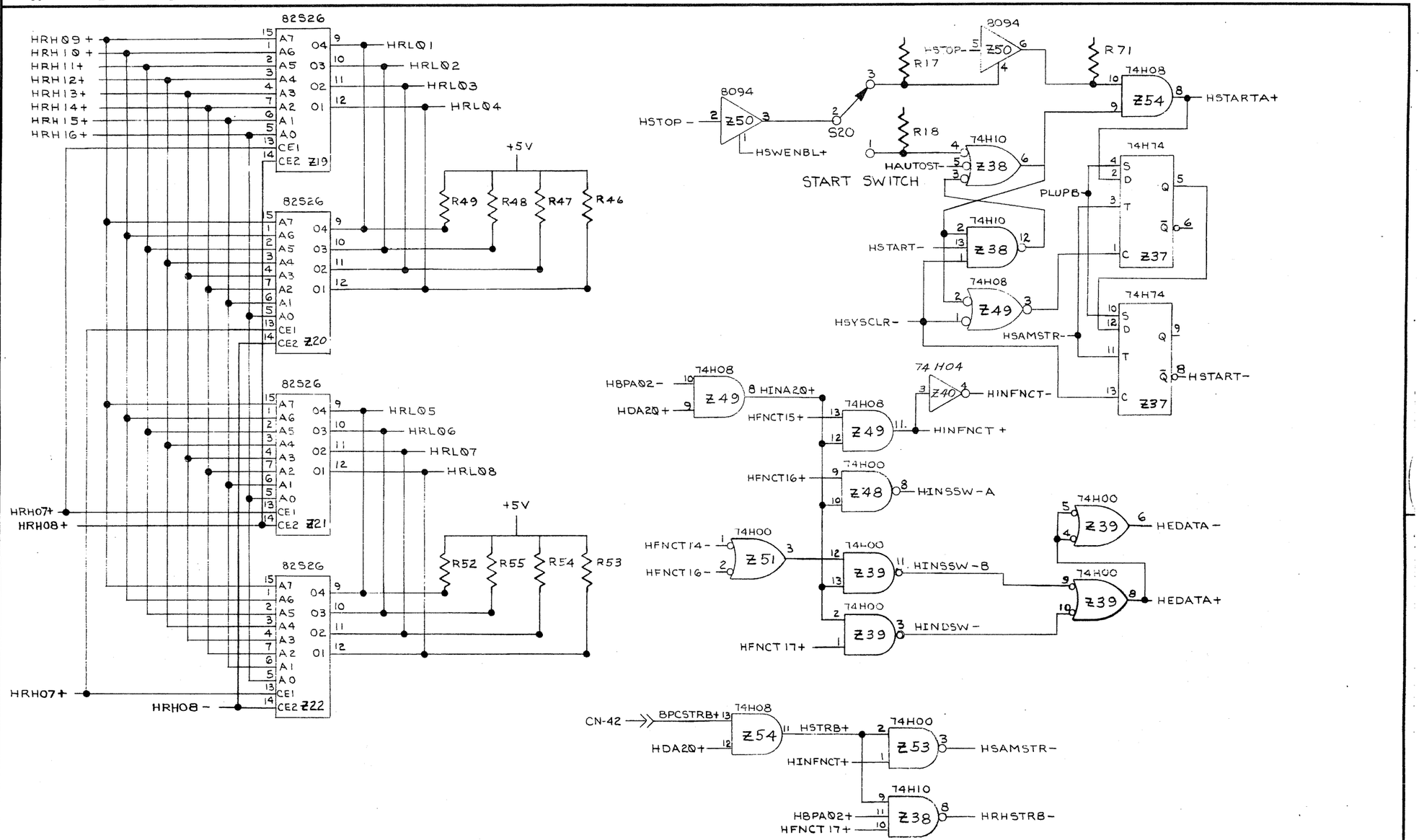




FUNCTION INPUT



MATERIAL	DWN Avelin 5/5/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	LOGIC CONTROL PANEL ETCH VERSION	
	APPRD		
	USED ON	SCALE ~	SIZE C
	NEXT ASSY	SHEET 2 OF 4	DWG. NO. LBD2532 REV. A

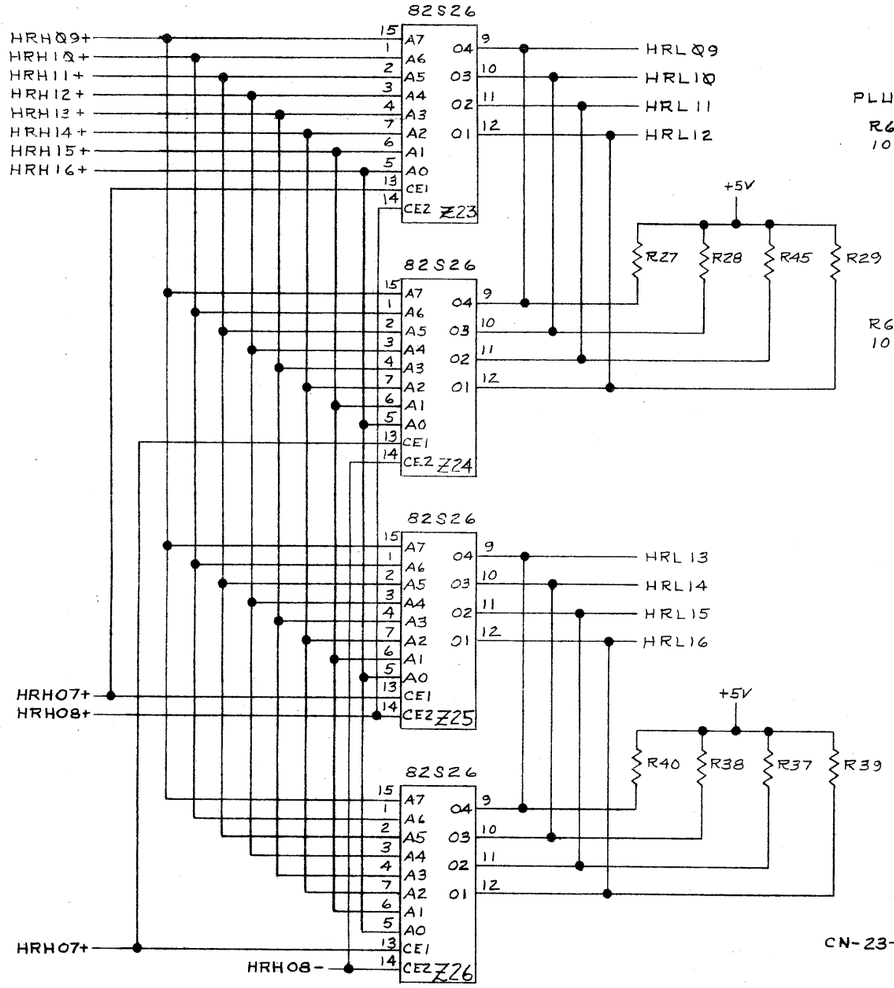


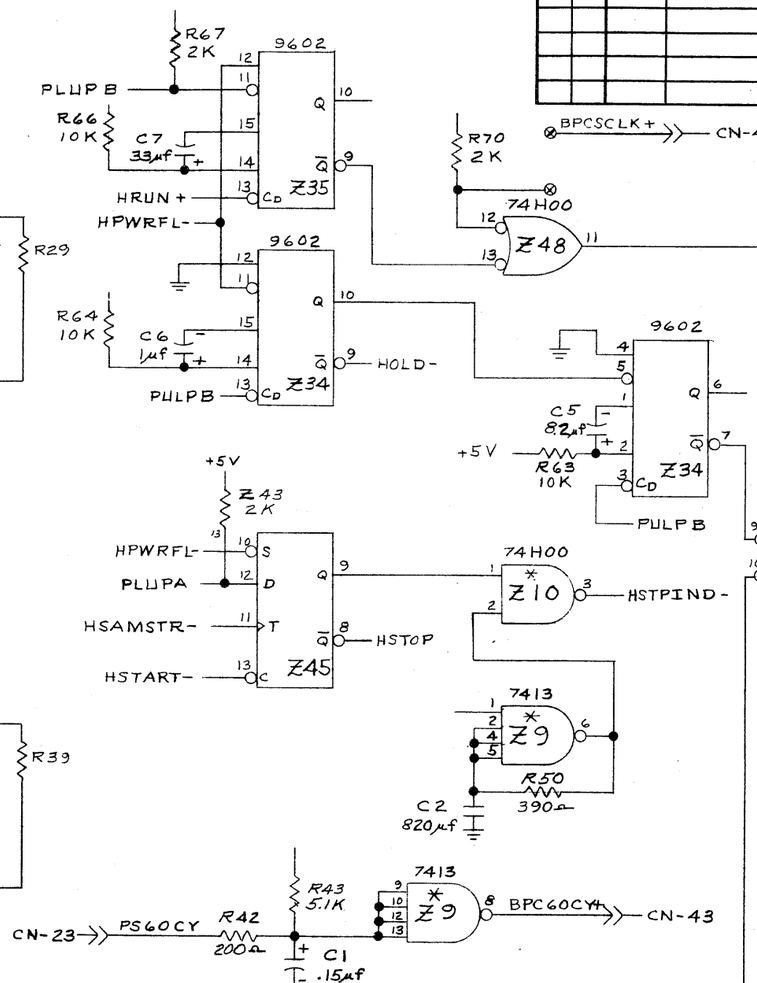
I-19

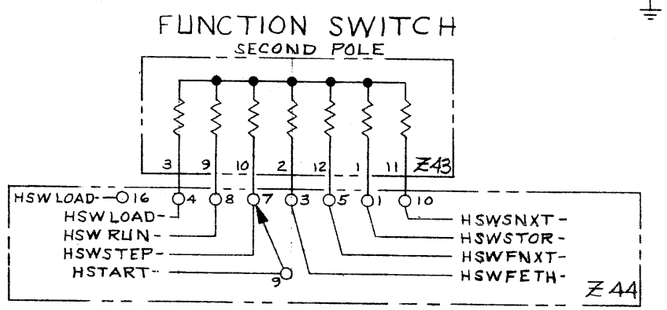
MATERIAL	DWN Heder 5/5/76	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	LOGIC, CONTROL PANEL ETCH VERSION
	APPRD	
	USED ON	SCALE — SIZE C DWG. NO. LBD2582 REV. A
	NEXT ASSY	SHEET 3 OF 4

PDF-003

M	LTR	DATE	REVISION	DR.	CK.





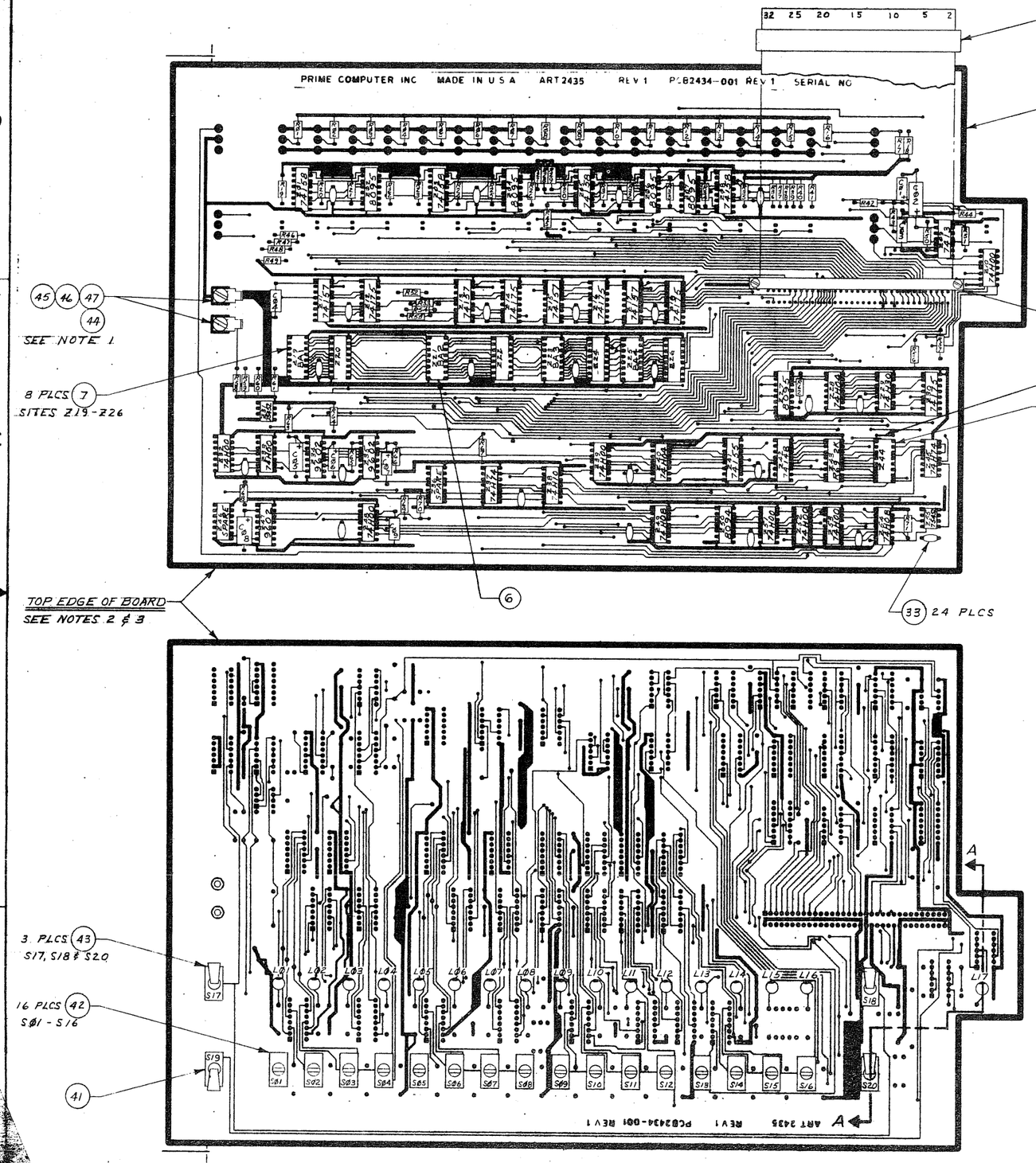


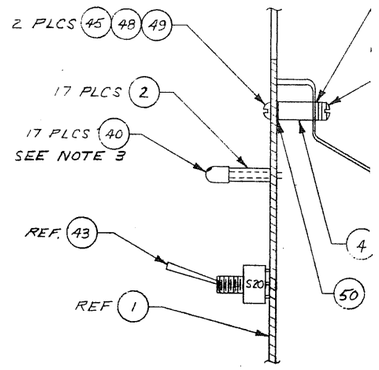
* POWERED BY VCC 2

I-20

MATERIAL	DWN Taylor 1/26/76	PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
	CHK	LOGIC, CONTROL PANEL ETCH VERSION	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.		
	APPRD		
	USED ON	SCALE ~	SIZE C
	NEXT ASSY	SHEET 4 OF 4	DWG. NO. LBD2582 REV. A

M	LTR	DATE	REVISION	DR.	CK.
	A	5/1/74	RELEASED PER ECR 1775	J.T.S.	AMP
	B	11/8/77	REVISED PER ECR 2061	[illegible]	AMP





SECTION A-A

Pin#	Signal	Pin#	Signal	Pin#	Signal
1	HPWRFL-	23	PS60CY+	45	SPARE
2	GND	24	BMA05-	46	BPCSCLK+
3	HPWRFL+	25	SPARE	47	SPARE
4	BMA15-	26	BMA06-	48	-12V
5	BPAØ1+	27	BPA13+	49	BPDØ9+
6	BMA16-	28	BMAØ3-	50	GND
7	BPAØ8+	29	BPA12+	51	BPDØ8+
8	BMA13-	30	BMA04-	52	BPDØ6+
9	BPAØ2+	31	BPA15+	53	BPDI1+
10	BMA14-	32	BMAØ1-	54	BPDØ7+
11	BPA11+	33	BPA14+	55	BPDIØ+
12	BMA11-	34	BMAØ2-	56	BPDØ4+
13	BPAØ7+	35	BPA16+	57	BPD12+
14	BMA12-	36	GND	58	BPDØ5+
15	BPA10+	37	VCC1	59	BPD14+
16	BMAØ9-	38	VCC1	60	BPDØ2+
17	BPAØ9+	39	BPCPIO+	61	BPD13+
18	BMA10-	40	VCC2	62	BPDØ3+
19	HSYSCLR-	41	SPARE	63	BPD16+
20	BMAØ7-	42	BPCSTRB+	64	BPDØ1+
21	PSRLY+	43	BPC60CY+	65	BPD15+
22	BMAØ8-	44	HRUN-	66	GND

Control Panel Connector List

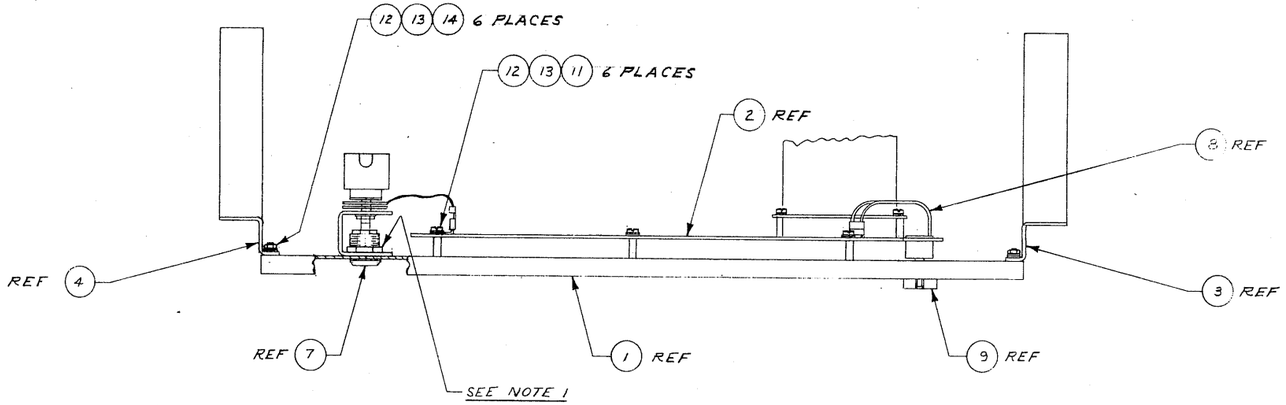
NOTES:
1. POSITION ITEM 44 AS SHOWN & SOLDER TO PADS.
2. COPPER SHIELD IN ITEM 3,(FLEX CABLE) IS TO BE TOWARDS BOTTOM OF ITEM 1 AS SHOWN
3. MOUNT LØ1 - L17 SO THAT DOT (CATHODE) IS TOWARD TOP OF BOARD AS SHOWN.
4. ITEMS 4 & 50 MUST BE ASSEMBLED TO ITEM 1 BEFORE INSTALLATION OF ITEM 3 TO ITEM 1.
5. JUMPER WIRE REQ'D. ITEM# 51

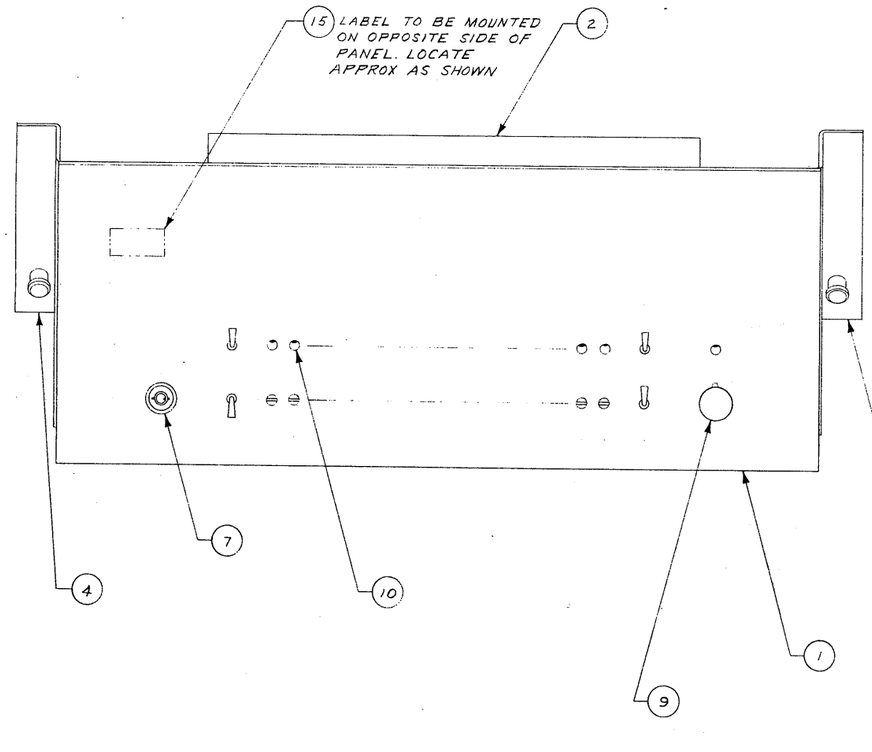
-902	NO PROM
-901	AS SHOWN
-XXX	DESCRIPTION

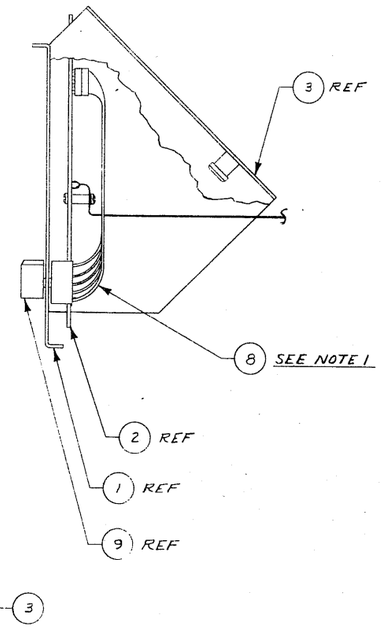
MATERIAL: SEE BOM	DWN: [illegible]	PRIME COMPUTER, INC. FRAMINGHAM, MASS.
UNLESS OTHERWISE SPECIFIED: -REMOVE ALL BURRS AND SHARP EDGES -DIMENSIONS ARE IN INCHES -TOLERANCES XX ± .01, XXX ± .005, ANGLES ± 0°	CHK: [illegible] 11/8/77 ENG: NAP APPRO:	P.C. BOARD SUB ASSY CONTROL PANEL
	USED IN: 1001-XXX NEXT ASSY: 1001-XXX	SCALE: 1/1 SHEET: 1 OF 1 SIZE: D DWG NO: ECAC630-XXX REV: B

BL E.V

M	LTR	DATE	REVISION	DR.	CK.
	A	8-20-76	RELEASED	RP	TCM
	B	11-3-76	REVISED PAINT SCHEME ECR 1933	RP	TCM
	C	1/26/77	BD. ASSY. PER ECR 2061	RP	TCM





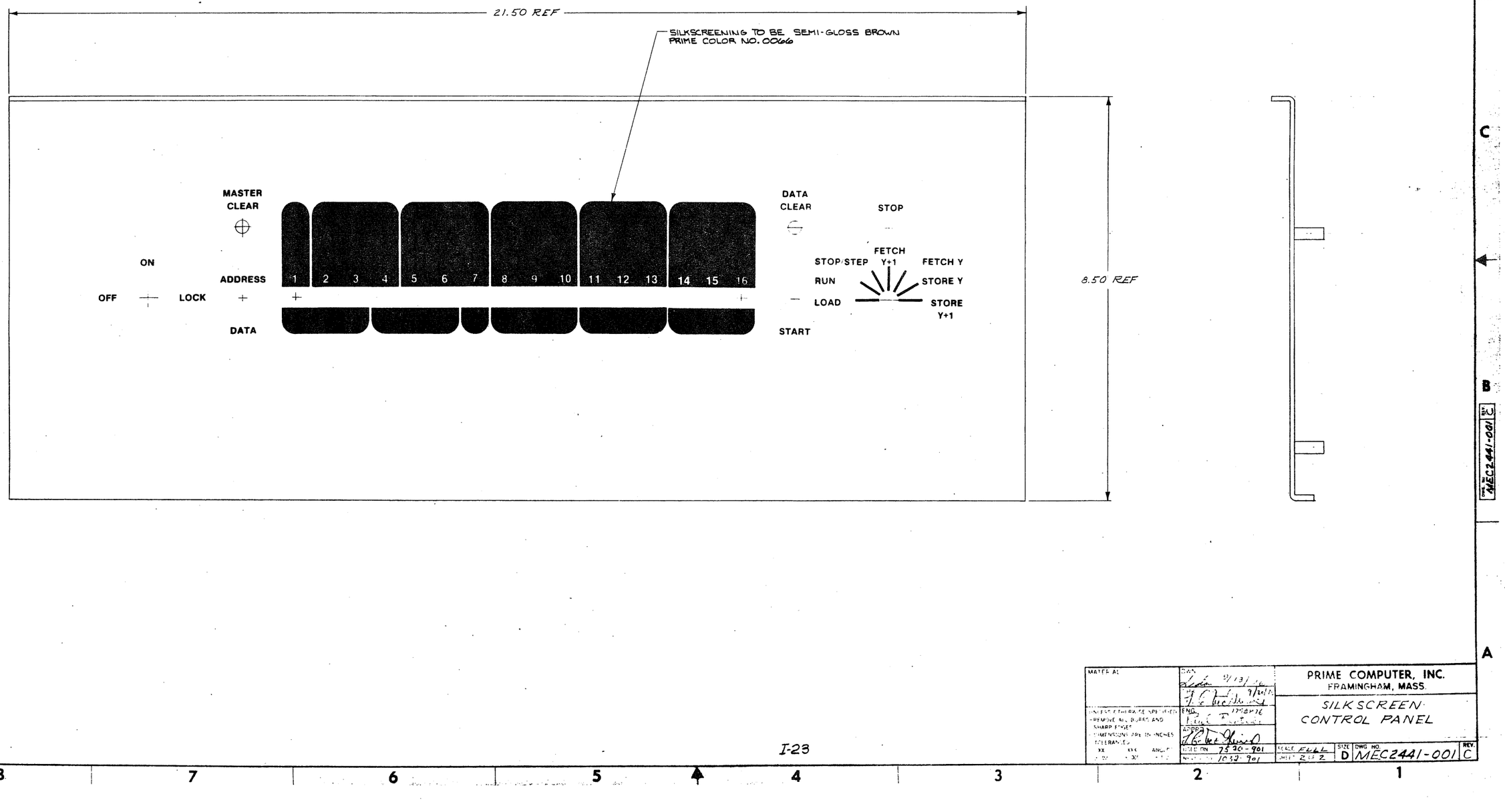


-902	WITH OUT PROM SET
-901	WITH PROM SET
-XXX	DESCRIPTION

NOTES:
1. MOUNTING HEX NUT IS PART OF ITEM 7 & ITEM 8

MATERIAL: SEE BOM	DWN	PRIME COMPUTER, INC. FRAMINGHAM, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK T. C. McDermott 1/27/77	CONTROL PANEL ASSY 7520
	ENG Paul C Beatrice 23 AUG 76	
	APPRD T. C. McDermott 1/27/77	
	USED ON 7520-901	SCALE 1/2 SIZE D DWG. NO. 1032-XXX REV. C
	NEXT ASSY	SHEET 1 OF 1

M	LTR	DATE	REVISION	DR.	CK.



MATERIAL	DAN 9/13/76	PRIME COMPUTER, INC. FRAMINGHAM, MASS.
UNLESS OTHERWISE SPECIFIED REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES TOLERANCES XX ±.01 XXX ±.005 ANGLES ±1°	ENG. [illegible] 9/20/76	SILK SCREEN CONTROL PANEL
	APPD. [illegible]	
	USED ON 7530-901	SCALE FULL SIZE D DWG NO. MEC2441-001 REV. C
	NEXT ASSY 1032-901	SHEET 2 OF 2

DWG NO. MEC2441-001 REV. C

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lein 1/29/76 | CHK. [illegible] 8/18/76 | ENG. [illegible] | APPRD.

STANDARD COST ______ DATE ______

TITLE: P.C. BOARD SUB-ASSY CONTROL PANEL

BL E.V.

BOM ESA0630-XXX REV. B

NHA: 1001-XXX SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
A	1775	[illegible]			
B	2061	[illegible]			

ITEM	SIZE	PART NUMBER	-901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1		PCB2434-001	1	1							P.C BOARD	
2	A	MEC0297	17	17							STAND-OFF LED	
3	C	CBL0572	1	1							CABLE, FLAT FLEXIBLE (FOLDING)	
4	B	MEC1530-001	1	1							STRAIN RELIEF MOUNT	
5	B	MEC1530-002	1	1							STRAIN RELIEF, CLAMP	
6	A	MEC1901-015	1	—							PROM SET EA	
7		CON0650-001	9	9							SOCKET, DIP Z19-Z26	
8		ICD0025	8	8							74H00 Z10, Z32, Z33, Z39, Z48, Z51-Z53	
9		ICD0028	2	2							74H04 Z28, Z40	
10		ICD0029	2	2							74H08 Z49, Z54	
11		ICD0030	1	1							74H10 Z38	
12		ICD0032	1	1							7413 Z09	
13		ICD0035	1	1							74H30 Z29	
14		ICD0043	2	2							74H74 Z37, Z45	
15		ICD0050	1	1							74155 Z41	
16		ICD0051	4	4							74157 Z11, Z13, Z15, Z17	
17		ICD0083	4	4							74158 Z01, Z03, Z05, Z08	
18		ICD0054	5	5							74175 Z12, Z14, Z16, Z18, Z30	
19		ICD0065	2	2							75452 Z31, Z55	
20		ICD0165	1	1							74148 Z42	
21		ICD0059	1	1							8094 Z50	
22		ICD0112	5	5							8095 Z02, Z04, Z06, Z07, Z27	

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PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lein 1/29/76 | CHK. | ENG. | APPRD.

STANDARD COST ______ DATE ______

TITLE: P.C. BOARD SUB-ASSY CONTROL PANEL

BL E.V.

BOM ESA0630-XXX REV. B

NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	-901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	*STANDARD COST
23												
24		ICD0062	3	3							9602 Z34, Z35, Z47	
25		RES0250-202	1	1							RESISTOR NETWORK 2K (R69) Z43	
26		RES1582-100	1	1							RESISTOR, 10Ω, 1/4W, 5% R62	
27		RES0221-226	19	19							RESISTOR, 150Ω, 1/4W, 2% R19,	
											R20-26, R30-36, R41, R44, R61, R69	
28		RES0221-243	1	1							RESISTOR 200Ω, 1/4W, 2% R42	
29		RES0221-289	1	1							RESISTOR, 390Ω, 1/4W, 2% R50	
30		RES0221-400	43	43							RESISTOR, 2K, 1/4W, 2% R01-18,	
											R27-29, R37-40, R45-49, R51-60	
											R67, R70, R71	
31		RES0221-467	2	2							RESISTOR, 5.1K, 1/4W, 2% R43, R65	
32		RES0221-522	4	4							RESISTOR, 10K, 1/4W, 2% R63, R64, R66,	R68
33		CAP0129	24	24							CAPACITOR, CERAMIC DISK, .01μf, 25V	
34		CAP2290-031	2	2							CAPACITOR, MONOGLASS, 330 PF, 50V C04, C09	
35		CAP0552-519	1	1							CAPACITOR, TANTALUM .15μf, 35V C01	
36		CAP0552-529	1	1							CAPACITOR, TANTALUM 1μf, 35V C06	
37		CAP0130-407	2	2							CAPACITOR, TANTALUM 8.2μf, 20V C05, C08	
38		CAP0130-210	2	2							CAPACITOR, TANTALUM 33μf, 10V ±10% C03, C07	
39		CAP0255	1	1							CAPACITOR, TANTALUM 820μf +20% -15% C02	
40		DIO0012	17	17							DIODE, LIGHT EMITTING L01-L17	
41		SWT0009	1	1							SWITCH, LEVER, ON-NONE-ON S19	

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PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lein 1/29/76 | CHK. | ENG. | APPRD.

STANDARD COST ______ DATE ______

TITLE: P.C. BOARD SUB-ASSY CONTROL PANEL

BL E.V.

BOM ESA0630-XXX REV. B

NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	-901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
42		SWT0010	16	16							SWITCH, LEVER, ON-OFF-MOM ON S01-S16	
43		SWT0011	3	3							SWITCH, LEVER, ON-NONE-MOM ON S17, S18, S20	
44		CON0166	2	2							CONN. Q.D. (TAB)	
45		MEC0303-005	6	6							SCREW, BINDER HD # 4-40 x 5/16 LG.	
46		MEC0355	2	2							WASHER, LOCK #4	
47		MEC0387	2	2							NUT, HEX # 4-40	
48		MEC0353	4	4							WASHER, FLAT METAL #4	
49		MEC0388-002	4	4							NUT, HEX SELF LOCKING # 4-40	
50		MEC0550	A/R	A/R							TAPE, INSULATING	
51		WIR0616-004	A/R	A/R							WIRE, SINGLE CONDUCTOR # 30AWG, YELLOW	
	C	LBD2582	REF	REF							LOGIC BLOCK DIAGRAM	

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PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lede 7/20/76 | CHK. [illegible] 8/26/76 | ENG. P. Beatrice 23 AUG 76 | APPRD. [illegible]

STANDARD COST ______ DATE ______

TITLE: CONTROL PANEL ASSY (7520)

BOM 1032 -XXX REV. C

NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	[illegible]			
B	1933-A	[illegible]			
C	2061	[illegible]			

ITEM	SIZE	PART NUMBER	-901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	MEC2441-001	1	1							CONTROL PANEL, CABINET	
2	D	ESA0630-901	1	—							P.C. BOARD SUB-ASSY, WITH PROM	
2	D	ESA0630-902	—	1							P.C BOARD SUB-ASSY, W/O PROM	
3	C	MEC2427-001	1	1							CONTROL PANEL SUPPORT (RH)	
4	C	MEC2427-002	1	1							CONTROL PANEL SUPPORT (LH)	
5												
6												
7	C	MSA0168-902	1	1							KEYLOCK SWITCH ASSY	
8	C	CBL1232-901	1	1							CABLE, FUNCTION SWITCH	
9		MEC0015-001	1	1							KNOB	
10		MEC0111	17	17							CLIP, PANEL MOUNT ADAPTER (LED)	
11		MEC0313-005	6	6							SCREW, BD. HD., SSTL, 6-32 x 5/16 LG	
12		MEC0359	12	12							WASHER, FLT., SSTL #6	
13		MEC0361	12	12							WASHER, LCK., INT. TOOTH #6	
14		MEC0391	6	6							NUT, HEX, SSTL #6-32	
15	A	MEC0292	1	1							LABEL, MODEL & SERIAL NO.	
16		MEC0361	1	1							WASHER, FLAT NYLON #6	

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PRIME COMPUTER INC. — NATICK MASS.

DWN. [illegible] 10/19/73 | CHK. [illegible] 10/17/77 | ENG. AHP | APPRD.

STANDARD COST ______ DATE ______

TITLE: CONTROL PANEL ASSY

BOM 1001 -XXX — REV. M1

NHA: MEC 0282 — SHT. 1 OF 2

REV.	ECN	CK	REV.	ECN	CK
F	441	[illegible]	K	1614	AHP
G	1442	[illegible]	L	1775	AHP
H	1445-1452	[illegible]	M	2030, 2053, 2061	[illegible]
J	1540	PB	M1	ADDED -907	

ITEM	SIZE	PART NUMBER	QTY -000	QTY -001	QTY -245	QTY -006	QTY -907	DESCRIPTION	STANDARD COST
1	D	MEC0264-100	1	1		1	1	PANEL, FRONT (STANDARD)	△J
2	D	MEC0285-001	1	1		—	—	FASCIA, PRIME	
2	D	MEC0285-002	—	—		1	—	FASCIA, L/P LINOTRON 303	
4	D	MEC0285-003				—	1	FASCIA, L/P PAINTED W/O LOGO	△M
5		MEC0313-014	2	2		2	2	SCREW, PH. HD. #6-32 x 7/8 LG	
6		MEC0313-016	7	7		7	7	SCREW FH HD #6-32 x 1" LG	△M
7		MEC0361	15	15		15	15	WASHER, LOCK INT TOOTH #6	△M
8	A	MEC0292	1	1	N	1	1	LABEL, MODEL & SERIAL NO.	△M
9	D	MEC0283-001	1	1		1	1	EXTRUSION BEZEL	△H △J
10		MEC0145-001	2	2	T	2	2	PUSH BUTTON CATCH (BUTTON ASSY)	△J
11	D	ESA0630-901	—	1	E	1	1	PC BD ASSY (W. PROM)	△E △J △L
11	D	ESA0630-902	1	—	E	—	—	PC BD ASSY (NO PROM)	△F △J △L
12	C	CBL1232-901	1	1	H	1	1	CABLE, FUNCTION SWITCH	△J
13		MEC0015-001	1	1	S	1	1	KNOB	△J
14		MEC0111	17	17		17	17	CLIP, PANEL MTG (DIODE)	△J
15					E				△J △M
16		MEC0313-005	6	6	E	6	6	SCREW, PAN HD #6-32 x 5/16 LG	△J
17					S				
18		MEC0363	1	1		1	1	WASHER, FLAT NYLON #6	△J
19		MEC0420-0[illegible]	A/R	A/R		A/R	A/R	TAPE, DOUBLE COATED, 1/2" W	△J
20	A	MEC0[illegible]	9	9		9	9	SPACER, PANEL (FASCIA)	

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L/P — L/P W/O LOGO

PRIME COMPUTER INC. — NATICK MASS.

DWN. DFC 6/15/73 | CHK. W. BOYAN 7/19/73 | ENG. [illegible] | APPRD. [illegible]

STANDARD COST ______ DATE ______

TITLE: P.C. BOARD SUB-ASSY CONTROL PANEL — BL — E.V.

BOM MEC0630-XXX — REV. K3

NHA: 1001-XXX — SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
D	1159		H	1446, 1425	[illegible]
E	1223		J	1540/1528	[illegible]
F	1243	[illegible]	J2	1604	[illegible]
G	1338	CHF	K	1614	AHP

ITEM	SIZE	PART NUMBER	QTY -001	QTY -002	DESCRIPTION	STANDARD COST
1	D	PCB0628	1	1	P.C. BOARD	
2		CON0166	2	2	CONN. Q.D. (TAB)	
3	A	MEC0297	17	17	STAND-OFF, LED	
4		DIC 0012	17	17	DIODES, LIGHT EMITTING L1-L17	
5		SWT0009	1	1	SWITCH, LEVER ON-NONE-ON S19	
6		SWT0010	16	16	SWITCH, LEVER, ON-OFF-MOM ON S1-S16	
7		SWT0011	3	3	SWITCH, LEVER, ON-NONE-MOM ON S17, S18, S20	
8	C	CBL 0572	1	1	CABLE, FLAT FLEXIBLE (FOLDING)	
8		RES1582-100	1	1	RESISTOR, 10Ω 1/4W 5% R72	△K
9		RES0250-202	1	1	RESISTOR NETWORK 2K R69	
10		RES0221-226	19	19	RESISTOR 150Ω 1/4W 2% R3, R7, R15, R23-R27, R34-R40, R45, R63	
11		RES0221-243	1	1	RESISTOR 200Ω 1/4W 2% R18	
12		RES0221-289	1	1	RESISTOR 390Ω 1/4W 2% R16	
13		RES0221-400	43	43	RESISTOR 2KΩ 1/4W 2% R1, R2, R8-R14, R19-R22, R30-R33, R41-R44, R46-R61, R64-R68, R71	△H
14		RES0221-467	2	2	RESISTOR 5.1K 1/4W 2% R5, R17	
15		RES0221-522	4	4	RESISTOR 10KΩ 1/4W 2% R4, R6, R62, R70	△H
16		CAP0129	23	23	CAPACITOR, CERAMIC DISK .01μf 25V	
17		CAP0130-210	2	2	CAPACITOR, TANTALUM 33μf 10V 10% C2, C7	
18		CAP0552-519	1	1	CAPACITOR, TANTALUM .15μf 35V C8	△K
19		CAP2290-031	2	2	CAPACITOR, MONOGLASS 330PF 50V C1, C5	△H △K

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PRIME COMPUTER INC. — NATICK MASS.

DWN. | CHK. | ENG. | APPRD.

STANDARD COST ______ DATE ______

TITLE: P.C. BOARD SUB-ASSY CONTROL PANEL — BL — EV.

BOM MEC0630-XXX — REV. K3

NHA: — SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK
K1	1685	[illegible]			
K2	1872	[illegible]			

ITEM	SIZE	PART NUMBER	QTY -001	QTY -002	DESCRIPTION	STANDARD COST
20		CAP0552-529	1	1	CAPACITOR, TANTALUM 1μf 35V C3	△K
21		CAP0130-407	2	2	CAPACITOR, TANTALUM 8.2μf 20V C4, C9	△H △K
22		CAP0255	1	1	CAPACITOR, TANTALUM 820μf +20% -15% C6	△E
23		MEC0303-005	4	4	SCREW, BINDER HD #4-40 x 5/16 LG.	△G △H △J
24		MEC0355	2	2	WASHER, LOCK #4	
25		MEC0387	2	2	NUT, HEX #4-40	
26		ICD0025	7	7	74H00 Z3, Z4, Z7, Z14, Z19, Z20, Z41	
27		ICD0028	2	2	74H04 Z13, Z22	
28		ICD0029	2	2	74H08 Z2, Z6	
29		ICD0030	1	1	74H10 Z15	
30		ICD0032	1	1	7413 Z42	
31		ICD0035	1	1	74H30 Z21	
32		ICD0043	2	2	74H74 Z8, Z16	
33		ICD0050	1	1	74155 Z12	
34		ICD0051	4	4	74157 Z34, Z36, Z38, Z40	
35		ICD0083	4	4	74158 Z43, Z46, Z48, Z50	
36		ICD0054	5	5	74175 Z51, Z33, Z35, Z37, Z39	
37		ICD0065	2	2	75452 Z1, Z32	
38		ICD0059	6	6	8094 Z5, Z23, Z44, Z45, Z47, Z49	
39		ICD0185	1	1	74148 Z11	△E
40		ICD0062	3	3	9602 Z17, Z18, Z10	△H
4[illegible]		CON0650-001	9	9	SOCKET, DIP Z24-Z31, Z9	△J2

PDF-004

PRIME COMPUTER INC. — NATICK MASS.

DWN. | CHK. | ENG. | APPRD.

STANDARD COST ______ DATE ______

TITLE: P.C. BOARD SUB-ASSY CONTROL PANEL

BOM MEC0630-XXX — REV. K3

NHA: — SHT. 3 OF 3

ITEM	SIZE	PART NUMBER	QTY -001	QTY -002	DESCRIPTION	STANDARD COST
43		WIR0633-000	1/2"	1/2"	WIRE, SINGLE COND (SOLID) #24 AWG BLK	
44	B	MEC1530-001	1	1	STRAIN RELIEF, MOUNT	△G
45	B	MEC1530-002	1	1	STRAIN RELIEF, CLAMP	△G
46		MEC0353	4	4	WASHER, FLAT METAL NO. 4	△G △H △J
47		MEC0388-002	4	4	NUT, HEX SELF LOCKING #4-40	△G △H △J
	C	LBD0620	REF	REF	LOGIC BLOCK DIAGRAM	
48						△G △H
49		MEC0550	A/R	A/R	TAPE, INSULATING	△G
50						△G △K3
51		CON0237	2	2	SOCKET, 14 PIN DIP	△H
52		CON0022	2	2	SOCKET, 16 PIN DIP	△H
53		CON0217	4	4	TERMINAL, SPLIT FEED THRU	△H
54		WIR0616-006	A/R	A/R	WIRE, SINGLE COND #30 AWG.	△H
55	A	MEC1301-015	1	—	PROM SET BA	△J

PDF-004

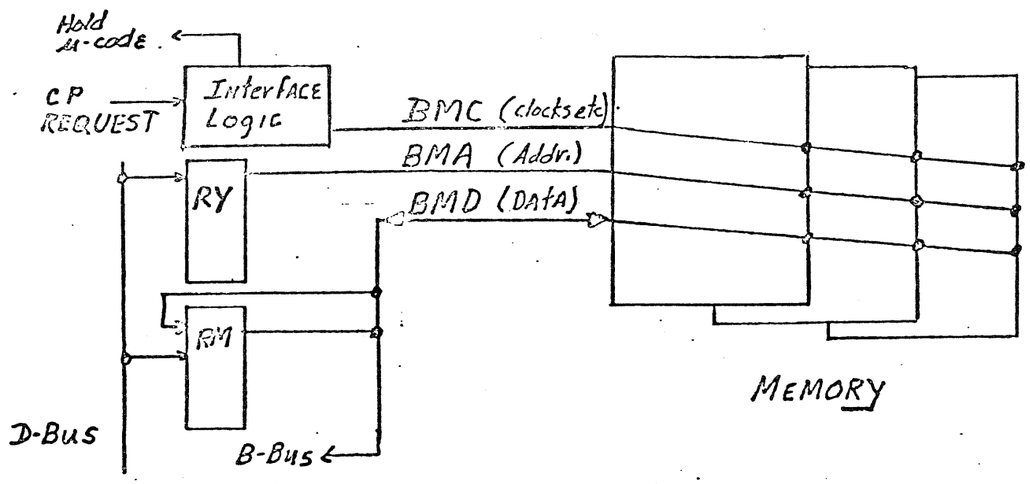
DATE: September 7, 1973

TO: List

FROM: J. E. Sheahan

SUBJECT: MEMORY INTERFACE DESCRIPTION

In all PRIME models, the CPU contains the hardware for memory cycle timing and data refresh operations. The memory modules merely respond to CPU stimulus. Two hardware registers, independent of the register file, support memory operations. The M register handles read and write data, the Y register handles memory address. Figure 1 is a primitive block diagram of the interface, buses, and memory modules.



The diagrams attached presume all positive true logic; they are not a gate for gate representation of the LBD's but are true to the functions performed. Alpha numeric designations in various blocks are the same as those on the LBD's.

Y Register

The Y register (Fig. 2A) receives data from the D bus of the μ-processor and is clocked by TRYL. The content of this register is gated onto the memory address bus, BMA, for normal memory references. There are two exceptions to the above. First, for refresh operations BMA (11-16) are not gated from RY but from refresh timing hardware designated FC (11-16). Also, BMA (8-10) are simply gated as high levels and the remaining BMA bits hold the previous states of RY since they are "don't care" conditions for refresh. If a system is in the "data save" mode, BMA always receives FC (11-16) since only refresh operations are taking place. The second exception is for Paging mode. Here the high order bits BMA 99, 00 (1-7) are gated from a register file containing a portion of the memory page map. Low order bits are not affected by paging since the map references are made on a sector basis.

M Register

Figure 2B shows the M register, its data sources and destinations. The memory data bus, BMD, is an eighteen wire bilateral bus which transmits write data to memory and transmits read data to RM.

The M register has two data sources, the D bus of the μ-processor and BMD. Its destinations are the B bus of the μ-processor for read data and BMD for data to be written into memory. MRDY is conditioned by the μ-code, and gates BMD to the RM data inputs. The data is then clocked by TRML. For memory write cycles, Register A is transferred to the D Bus and clocked into RM. The data in RM is gated to BMD by ERMEMD (basically a decoded write command).

Interface Logic

The memory interface logic contains two digital timers and four major control flip flops.

Timer 1 of Figure 3 generates a refresh request every 32 μ-second. It also divides the request by 32 and thereby generates 32 address states (FC 12-16) which are used as refresh addresses to the MOS memory devices. This results in a repetition of refresh address every one millisecond (32 μ-second x 32 states) satisfying the device specification.

Timer 2 is a 12 bit shift register gated on by requests for a memory cycle. A logic ONE is shifted for nine clocks, then a ZERO is started down the register. Memory clocks and interface time outs are generated by gating combinations of register bit outputs and polarities.

FMCPRQ

This control flop is used to store memory cycle requests from the CP. It is set as a result of RCC bits 25 and 26 indicating a request, and timed by TRCMT to form MSTCPRQ. The flop is set at TRCML time (new μ-cycle) thereby initiating Timer 2. The timer is coded to reset FMCPRQ after 600 ns into a read cycle and 720 ns into a write cycle.

The request flop cannot be reset if a refresh cycle is in progress. Therefore, if a CP request is made while a refresh cycle is active, the request will be stored but not cleared when refresh expires. The stored request will be honored as soon as refresh is complete.

MBSY

This control flop is also set by MSTCPRQ. When set, it indicates that the memory is busy processing a CP request and also prevents a refresh request from being honored. MBSY is gated with a write condition to form ERMBMD enabling RM onto BMD. It is reset at 760 ns if another CP request is not present. If requests come repeatedly at 760 ns, it is clear that refresh would be locked out and memory would crash. Therefore, μ-processor timing is structured to avoid this potential problem.

MDATAV

This third control flop is also set by MSTCPRQ and is reset at 520 ns if a refresh cycle is not being processed. When reset, it releases TPCL and permits read data to be clocked into RM at 600 ns by TRML.

FMRFRQ

This flop stores the Timer 1 request for a refresh cycle and initiates Timer 2. It cannot be set if MBSY is active, so an auxiliary flop is used to store the request until memory goes not busy. At this time, FMRFRQ is set, the auxiliary is cleared, and Timer 2 is started. FMRFRQ is reset by the timer at 840 ns and the memory is then available to the CP.

Memory Clocks

There are three clocks sent to memory for various functions. These are:

1. BMCPRCH - Precharges all nodes in the MOS memory devices in preparation for an active cycle. Starts at 40 ns after Timer 2 has been gated on and lasts for 360 ns.

2. BMCCNBL - This clock activates the selected memory devices and permits data to be read or written. It starts at 240 ns after Timer 2 has been activated and lasts until 600 ns for Read and Refresh cycles and until 720 ns for write cycles.

3. BMCWSTB - This clock causes data to be written into the MOS devices. It starts 520 ns after Timer 2 is initialized and lasts until 720 ns.

Aborted Cycles

There are two trap conditions which cause FMCPRQ to be cleared and Timer 2 to be reset. These are register file references and page traps. In each case, the memory has been started before a change in plan becomes apparent. The abort signal becomes active 120 ns after FMCPRQ and although BMCPRCH has gone to memory, no data has been altered.

Memory Reference Timing

Figure 4 shows the CP timing for two memory cycles and the associated μ-processor cycles. The first cycle is a fetch and decode of a store register A instruction; the second is the execution of the STA. The first μ-program step in the fetch is the transfer of the program counter to the Y (address) register. The second is a memory read; the third is the decode of the instruction and formation of address for the instruction execution. To execute the STA, register A is first transferred to RM, then the last μ-program step forces a memory write cycle.

The following is a definition of the timing clocks shown.

TPCL - Timing Pulse Clear - Resets μ-processor timer
TRCMT - Trigger ROM control memory, trailing edge
TRCML - Trigger ROM control memory, leading edge
TRY - Trigger register Y leading edge
TRML - Trigger register M leading edge

The end of each μ-processor cycle is characterized by TPCL making a high to low transition followed by TRCMT and TRCML pulses. TRCML clocks new ROM data (RCC) into the ROM Data Register and the μ-cycle begins to execute. In the case of memory reference cycles, TPCL is held high waiting for MDATAV during read cycles and the reset of FMCPRQ during write cycles.

Fetch

CLY 200

During this step, Register P is transferred to Register Y and clocked by TRYL at TRCML time. This action causes BMA to change after some delay. During TRCMT the data for the next ROM step has settled at the ROM outputs but is not clocked into the ROM register until TRCML. Bits 25 and 26 are gated with TRCMT and MSTCPRQ becomes true on the input to three of the control flops, FMCPRQ, MBSY, and MDATAV. At TRCML time, all three flops set and Timer 2 is enabled.

The data on BMD will change just after BMA has switched if the new memory address references a different module than was previously addressed. This is because each module has its own output data latch gated by module address. Therefore, BMD will reflect the data latch contents of the newly addressed module.

HSM Read

At 200 ns into the cycle TPCL will set and cause a write clock to go to the register file. P + 1 will be written into the file in preparation for the next fetch. However, TPCL cannot reset because it is gated by MDATAV which is in turn waiting for the memory timer. Therefore, no more μ-processor action will take place. BMD will go to all ONE's shortly after the CENABLE clock is sent to memory because of a memory chip peculiarity. However, the correct memory read data will typically appear about 500 ns into the cycle. MDATAV will time out at 520 ns permitting TPCL to reset at 560 and allowing TRCML and TRML to occur at 600 ns.

The data read from memory is now in RM, memory clocks have terminated and the next μ-processor step is clocked into RCM.

Decode and Bld. Address

During this step the instruction is decoded and a new address formed as a result of the data in RM. During this cycle, MBSY resets 800 ns from the time it was set and TRYL occurs at 280 ns. A new address is placed on BMA, and BMD may change as described previously. The next μ-step begins at TRCML-280 ns.

STA

RA→RM

Register A is transferred to Register M. Register M is clocked by TRML at 200 ns.

HSM Write

During TRCMT a memory reference is detected and MSTCPRQ becomes active. At 200 ns the three control flops will be set and the memory timer activated. Shortly after MBSY is set, ERMBMD will enable tri-state drivers and place RM on the BMD. The memory modules will have their output data latches disabled by the Byte Enable signals leaving the bus to RM. Some bus instability can be observed at this time. At 200 ns into the cycle, TPCL will set and permit TRCMT and TRCML to be generated. Since the HSM Write μ-code has a jam F condition the μ-processor goes to the first step of the fetch cycle, namely CLY 200 as previously shown. The CLY is conditioned by YBSY so TPCL will again set at 200 ns but will be prevented from resetting by FMCPRQ.

MDATAV times out at 520 ns but causes no action. At 720 ns, FMCPRQ is reset by the timer and TPCL resets at 760 ns. TRCML completes the CLY at 800 ns and begins the HSM Read step of the fetch cycle. Although FMCPRQ will accept a request at this time, the memory timer will not restart until 840 ns. This delay is required due to duty cycle requirements in the memory and memory and μ-code relationship.

Paging

PRIME has published a brochure describing the functional aspects of virtual memory and PRIME's paging system. This reading is considered a prerequisite to the following hardware description.

A functional diagram of the hardware associated with paging is shown in Figure 5. The execution of the instruction EPMJ will set FPAM and allow F4 to indicate MPAGREF. When set, this signal delays memory requests (MSTCPRQ) by 80 ns while the mapped address RPF is being obtained from the RAM.

The basic function of the hardware is to map a memory reference of a given virtual sector to a physical sector. For example, sector 7 may

be mapped to sector 24 so that a virtual reference to 7 will actually become a reference to physical memory 24. The RAM contains the sector being mapped to; the CAM contains the sector being mapped from.

If a reference is made to sector 7, RY presents a 7 to the CAM data inputs. Assuming the CAM contains a 7, one of the four match outputs will become true. This output addresses the RAM word containing a 24. RPF then becomes a 24 and is gated via the RY multiplexer onto BMA.

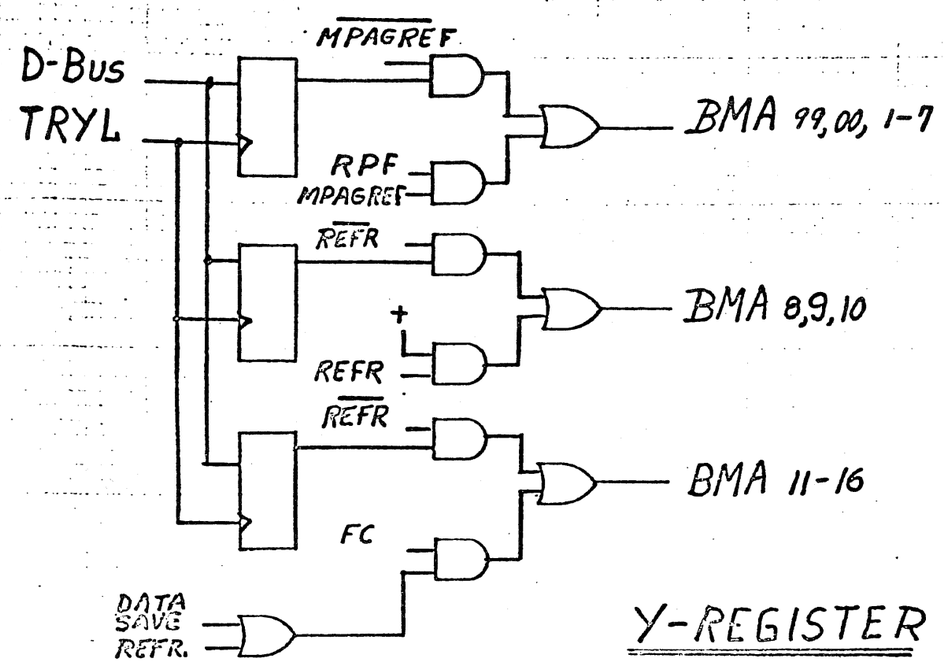
If none of the four CAM words contained a 7 the no match condition would set GPGTR a page trap. This trap signifies that the required portion of the memory map is not in RAM. The μ-code will jump to a special routine to fetch the desired map portion from main memory. A forced memory read is initiated by an independent action code IACFRD and F3 becomes set. If the trapped memory reference had been a HSM Write the byte enables BMCWLB and BMCWRB would have been active. FIAFMRD will disable these signals during the forced read. In addition, IACFRD- will prevent F1 and F2 from being changed.

The information from the memory map is written into the RAM and the associated address is loaded into the CAM. The CAM address to be used is determined by a priority network, the algorithm being that the least most recently accessed location will be the one chosen for new information. A HSM resume is issued from μ-code permitting the paged HSM Write to be executed. IACRHSM- again prevents F1 and F2 from being altered until the instruction has been completed.

James E. Sheahan

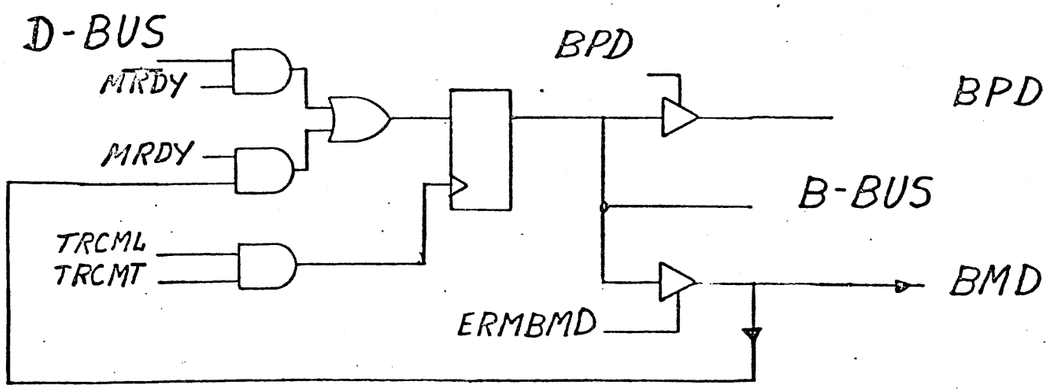
/dmf

Attachments



Y-REGISTER

Fig. 2A



M-REGISTER

Fig. 2B

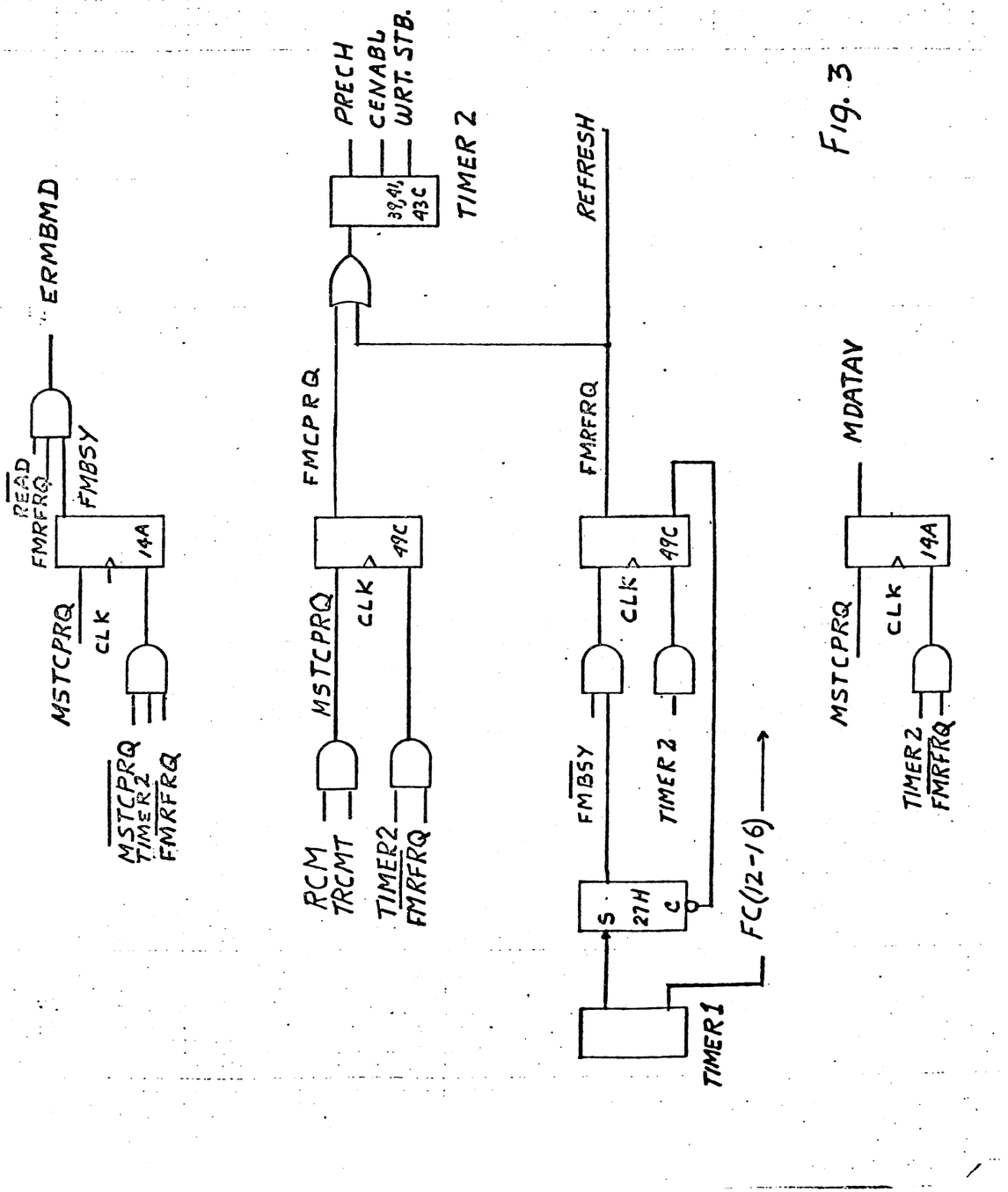


Fig. 3

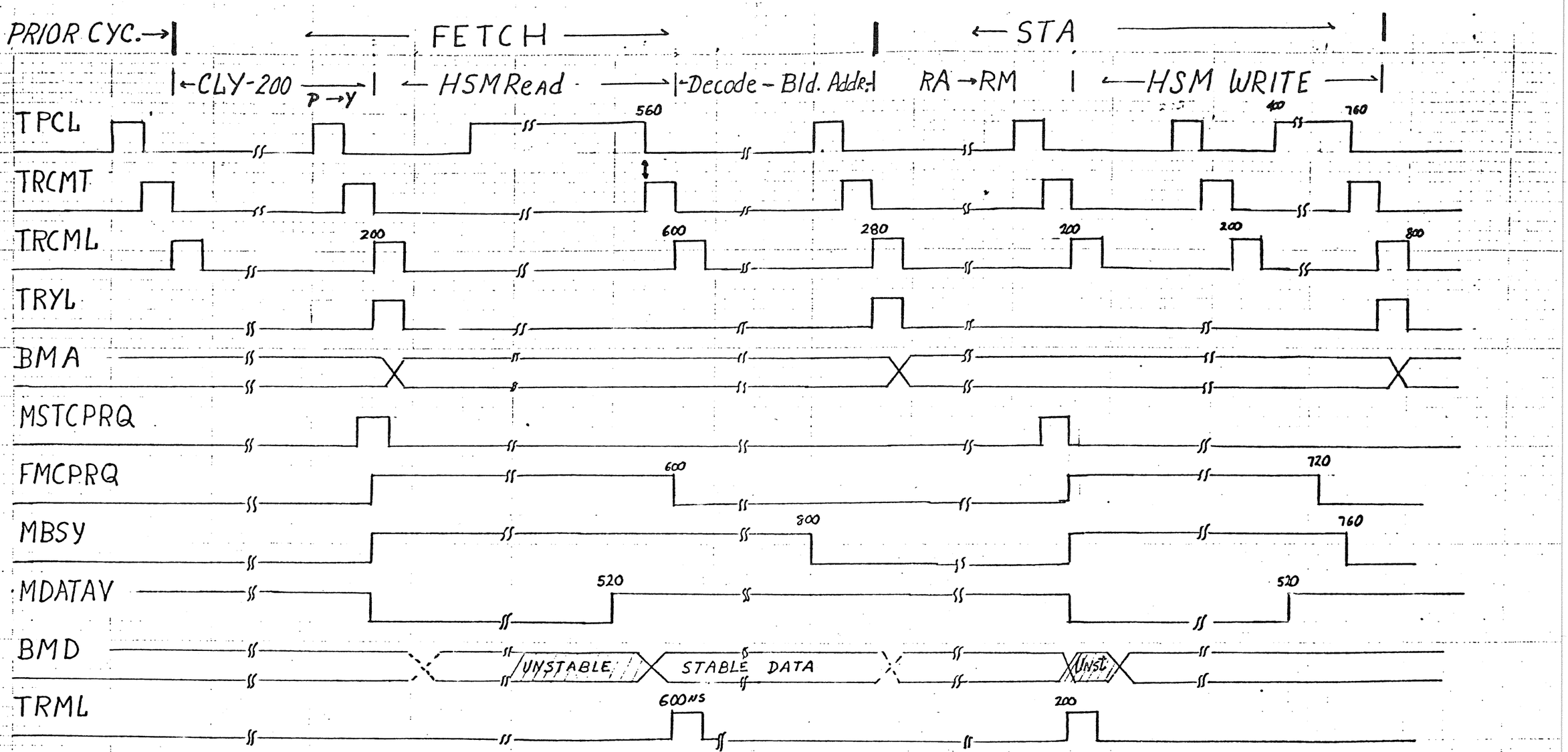

PRIOR CYC.→
FETCH
←STA
←CLY-200
P→Y
←HSM Read
←Decode-Bld. Addr.
RA→RM
←HSM WRITE
TPCL
560
400
760
TRCMT
TRCML
200
600
280
200
200
800
TRYL
BMA
MSTCPRQ
FMCPRQ
600
720
MBSY
800
760
MDATAV
520
520
BMD
UNSTABLE
STABLE DATA
UNST
TRML
600NS
200

Fig 4

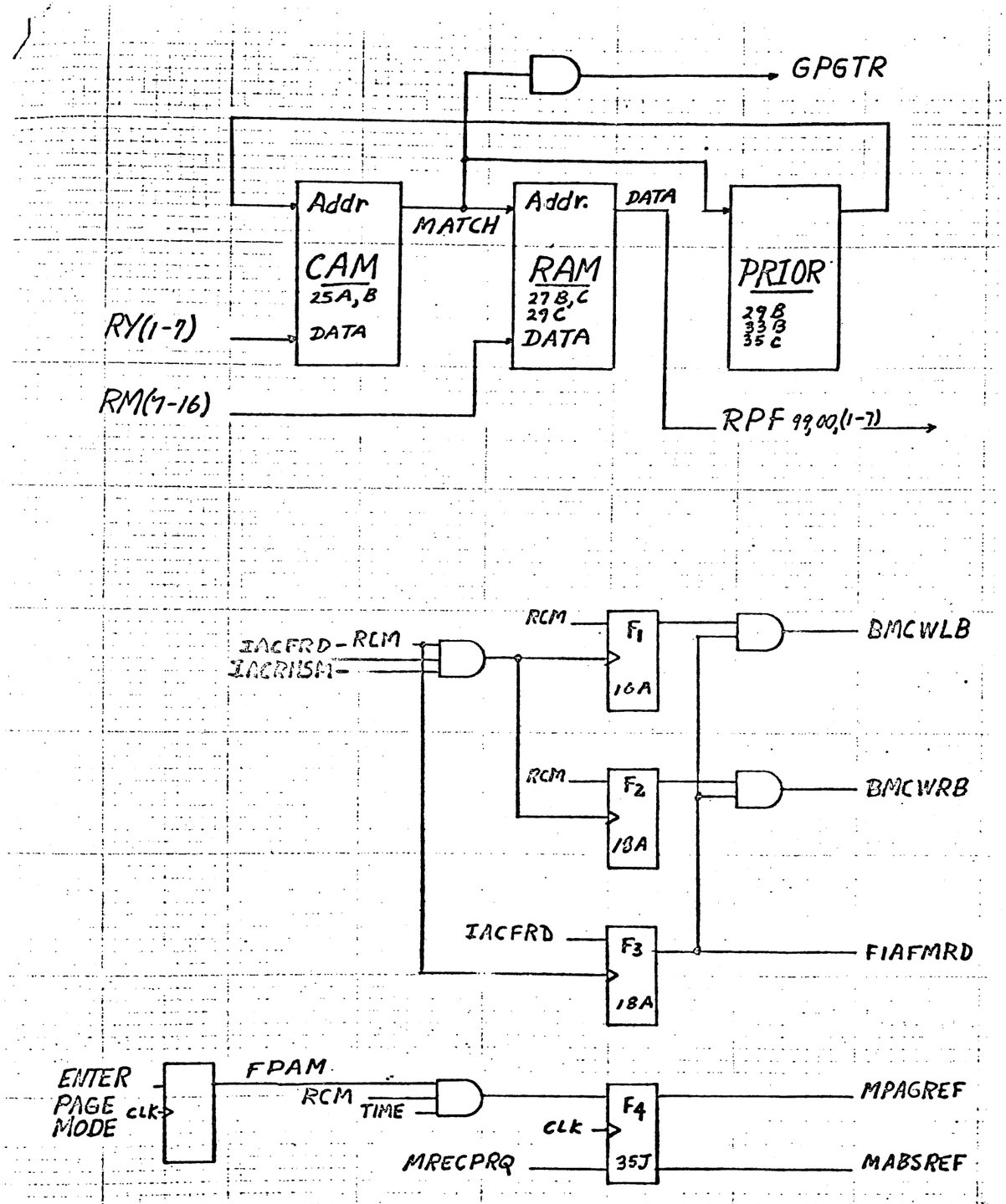

GPGTR
Addr
CAM
25A, B
DATA
MATCH
Addr.
RAM
27B, C
29C
DATA
DATA
PRIOR
29B
33B
35C
RY(1-7)
RM(7-16)
RPF 99,00,(1-7)
IACFRD-RCM
IACRISM-
RCM
F1
16A
BMCWLB
RCM
F2
18A
BMCWRB
IACFRD
F3
18A
FIAFMRD
ENTER
PAGE
MODE
clk
FPAM
RCM
TIME
clk
F4
35J
MRECPRQ
MPAGREF
MABSREF

Fig. 5

DATE: July 25, 1973

TO: List

FROM: J. E. Sheahan

SUBJECT: MEMORY MODULE DESCRIPTION

Each memory module contains module selection logic, data bus interface, MOS storage devices, MOS driver circuits and sense amps. Parity checkers for address and write data are also included. The module presents a completely TTL interface to the memory bus and receives all its timing and control for the CPU via this bus. The module is designed to operate with up to seven other similar modules sharing a common bus (backplane). The following configurations are available:

	Model No.
8192 words x 18 bits	271
8192 words x 16 bits	171
4096 words x 18 bits	270
4096 words x 16 bits	170

Figure 1 is a block diagram of an 8K memory module. The storage matrix is made up of 1103 memory devices which are organized as 1024 words by one bit. A total of 144 1103's gives a capacity of 8K words by 18 bits.

Data Bus (Positive True, ONE = +5 V)

The eighteen bit data word is comprised of two eight bit bytes with a parity bit for each byte. The 18 read-data lines (memory output) and the 18 write-data lines (memory input) are duplexed onto one 18 wire bus designated BMD. Tri-state drivers are used exclusively for this function. Data is stored and retrieved without polarity inversion.

The parity checker associated with the data bus is always active and indicates the state of bus parity during read or write cycles; however, it is only tested by the CP during write cycles.

Address Bus (Negative True, ONE = 0 volts)

The three high order bits of memory address are used to determine which module is to be selected. The selected module generates a select back signal that is tested by the CP. The absence of this signal results in a missing module trap. The select line on the active memory module enables clock drivers, address drivers, and enables the modules tri-state drivers on the data bus.

Address bits BMA(04-06) select a 1K block of the 8K storage matrix and steer clocks to this one row of 1103 devices. Therefore during normal read write cycles only 18 1103's in the entire memory are active; all others are in a low power state.

The least significant ten address bits BMA(07-16) directly address the 1103 and are decoded within the devices. Therefore, these addresses uniquely determine the word address within a 1K block.

Address parity is checked by byte (nine bits) and errors are indicated as to left or right byte. Again an error will cause a logic low (0 volts) on the error lines.

Figure 2 shows the fields and connector pins for the address and data fields.

Refresh

The 1103 storage device stores data on parasitic junction capacitors. Since these gradually lose charge through junction leakage it is necessary to rewrite or refresh the data periodically. The refresh operation is accomplished by processing a read cycle on each of the 1024 bits and must be repeated each millisecond.

The 1103 is organized as 32 rows and 32 columns. Refreshing a single row will automatically refresh all 32 columns associated with that row. Therefore on an individual 1103 device the 32 rows can be sequentially refreshed one cycle each 32 μ-sec completing the entire process in one ms.

During refresh operations the module select logic and the chip row select logic are overridden and every 1103 device in the system is selected. Therefore, Row N(1-32) of all 1103 devices sees a refresh cycle simultaneously. The entire memory system is thus refreshed with the value of N incrementing each 32 μ-sec.

Detailed Discussion

Figures 3 and 4 are more detailed diagrams of the blocks presented in figure 1. All signals are treated as positive true for ease of discussion but the reader should be aware that all 1103 clocks are active low. Address and data latches are present on the module but the latch clocks are grounded for the PRIME 100 and 200 causing the latch to act as a simple inverter.

Re: Figure 3 - Each module slot in a PRIME backplane has five lines statically coded as gnd or +5 volts. The uppermost slot is coded all ZEROS (+5V-negative true). This slot represents the least significant module address, namely the first 8K of memory. The variable addresses (BMA) are compared against the fixed slot code to determine if the CP is attempting to select a specific module. As stated previously a select signal is returned to the CP and also gates signals called X,Y enable. These in turn permit the chip address drivers to leave their normal low power state (+16 volts)

and present BMA07-16 to the 1103 device. The X enable function is an OR of select and the refresh command. This permits the X addresses to be active during refresh independent of the state of module select. Therefore, every module in the system is effectively active during refresh. System Clear holds the five Y address drivers in the low power state during battery back-up operations.

Device Clocks

Prech, Cenable, and Write are clocks which control operations within the 1103. Prech is a conditioning signal used to reset internal mode voltages prior to an active cycle. Cenable activates a chip cycle, connects the data in and data out lines and selects a specific internal cell (1 of 1024). If a Write pulse is present, data is written into the selected cell; in the absence of Write, the cell contents will be displayed on the data out line.

Prech and Cenable are gated with X-enable so that only a selected module will have active clocks. Write is gated with Select, Cenable, and the absence of refresh.

Re: Figure 4 - Figure 4 shows a further breakdown of clock decoding and address drivers. The right byte for an 8K module is shown; the left byte is identical and independent except for the common row decoder. This 1 of 8 decoder determines which of the 1K blocks is to be selected and therefore to be activated by the clocks. There are separate drivers for each 1K block and each byte; therefore a single driver circuit (4 per DIP) services nine 1103 devices. Write drivers are additionally gated by the Byte enable controls. Address drivers for BMA 7-16 are broken down by byte and 4K blocks. Therefore each driver services 4 x 9 or 36 devices.

The output of the 1103 is an open drain (like open collector gates) which sources 800 μa for a ONE and appears open for a ZERO. All 1103 outputs for a given bit are wire ORed and terminated to ground through 200-Ω's at the sense amplifier input. The sense amp is a three-stage device containing a linear amplifier, gated latch and tri-state buffer. The output of the sense amp is staticized in the latch by the trailing edge of CENBL during normal read and write cycles. The contents are not modified during deselect or refresh cycles. The tri-state drivers are active on the data bus whenever the module is selected except during Byte Enable (write cycle) periods.

During a write cycle, Byte Cenables become active, the tri-state drivers of the sense amps disconnect, and the bus information is gated through the Write Data Latch to the data drivers. There is one data driver per bit meaning each circuit services eight 1103 devices.

System Timing

All memory system timing is generated by the CP interface logic and sent to all memories via the backplane bus. Figure 5 shows the major signals on the backplane and internal to the memory module. A write cycle followed by

a read cycle is depicted. All times are typical. The scale of the drawing does not allow accurate interpretation of internal signals but is sufficient for determination of normal operation.

The arrows between various signals indicate that one signal is gated by the other, the tail of the arrow is the gator, the head is the gatee.

Unique Characteristics

Fuses

Each module has a fuse in series with the V_{ss} (16.2v) and the V_{bb} (19.7v) lines. Sensing circuitry will cause the V_{ss} fuse to blow if V_{ss} is shorted or otherwise becomes negative relative to V_{bb}. Without these fuses such a short could destroy the 1103 devices. Removal or insertion of a module when power is on will usually cause a fuse to open.

During the PRECH active period the selected 1103 devices may draw in excess of 50 ma each or (50 x 18) 900 ma per board. During Refresh this could become (50 x 18 x 8) 7.2 amps per 8K board. In normal operation, duty cycle and bypass capacitors will prevent a fuse from blowing. However, if PRECH or Refresh become stuck active (low) due to a fault, the fuse may open.

When a V_{ss} fuse opens it may be possible that one or two bits will still appear to operate properly. This is a normal state since there is some V_{ss} current available through V_{bb} to V_{ss} paths in the 16 volt drivers.

Signal Levels

All signals to the 1103 devices are 0 to +16v; data out is about 200 mv. All other signals on the module and at the interface are TTL.

Bus Latches

There are latches on the module for Address and Write Data. For the PRIME 200 the clock lines are grounded on the CP board making the latch look like a simple logic inverter.

Refresh

A refresh cycle will cause a memory busy every 32 μ-sec for the length of a normal write cycle. The address during refresh cycles will repeat every 32 refresh cycles. Missing refresh cycles may cause the memory to drop ONE's, but will not cause ONE's to be picked.

Byte Enables

Byte Enable must be active to process a write cycle. One byte may be written while the other is read by proper manipulation of Byte Enables.

July 25, 1973

Data Inhibit

An active data inhibit will force all signals from memory to a tri-state disconnect.

J. E. Sheahan

/dmf

Attachments

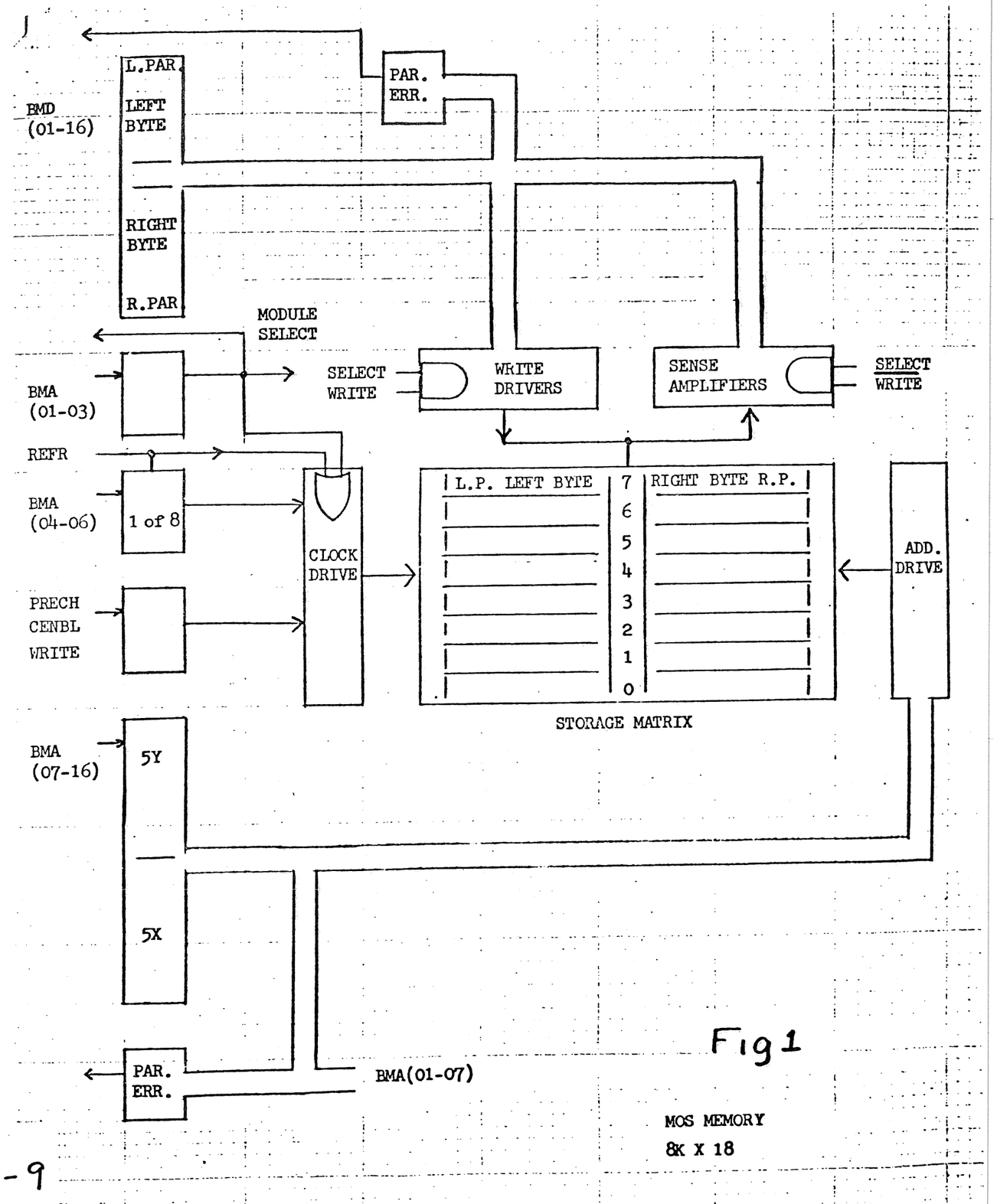


Fig 1

MOS MEMORY
8K X 18

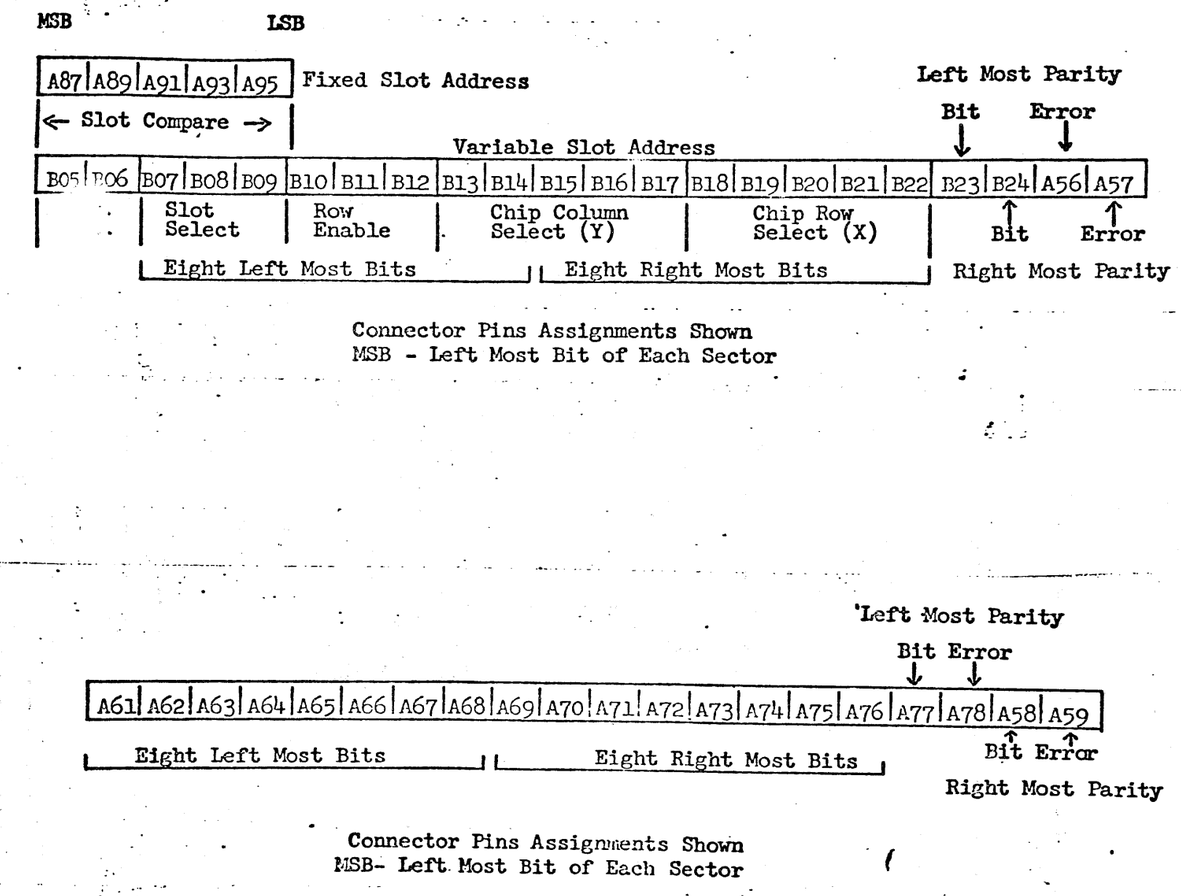

MSB
LSB
A87 A89 A91 A93 A95
Fixed Slot Address
← Slot Compare →
Left Most Parity
Bit
Error
Variable Slot Address
B05 B06 B07 B08 B09 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 B21 B22 B23 B24 A56 A57
Slot Select
Row Enable
Chip Column Select (Y)
Chip Row Select (X)
Bit
Error
Eight Left Most Bits
Eight Right Most Bits
Right Most Parity
Connector Pins Assignments Shown
MSB - Left Most Bit of Each Sector
Left Most Parity
Bit Error
A61 A62 A63 A64 A65 A66 A67 A68 A69 A70 A71 A72 A73 A74 A75 A76 A77 A78 A58 A59
Eight Left Most Bits
Eight Right Most Bits
Bit Error
Right Most Parity
Connector Pins Assignments Shown
MSB- Left Most Bit of Each Sector

Fig. 2

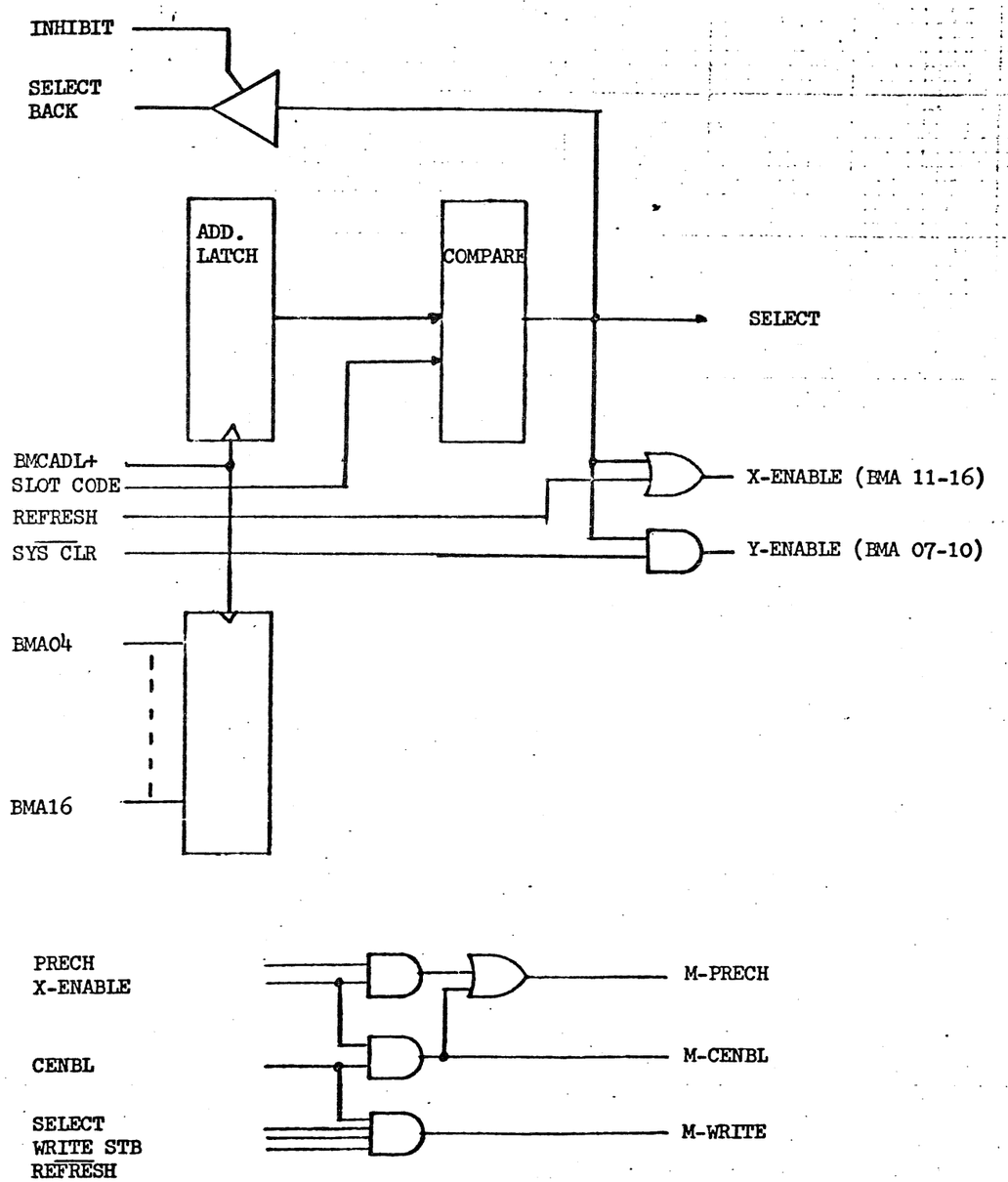

INHIBIT
SELECT BACK
ADD. LATCH
COMPARE
SELECT
BMCADL+
SLOT CODE
REFRESH
SYS CLR
X-ENABLE (BMA 11-16)
Y-ENABLE (BMA 07-10)
BMA04
BMA16
PRECH
X-ENABLE
CENBL
SELECT
WRITE STB
REFRESH
M-PRECH
M-CENBL
M-WRITE

Fig 3

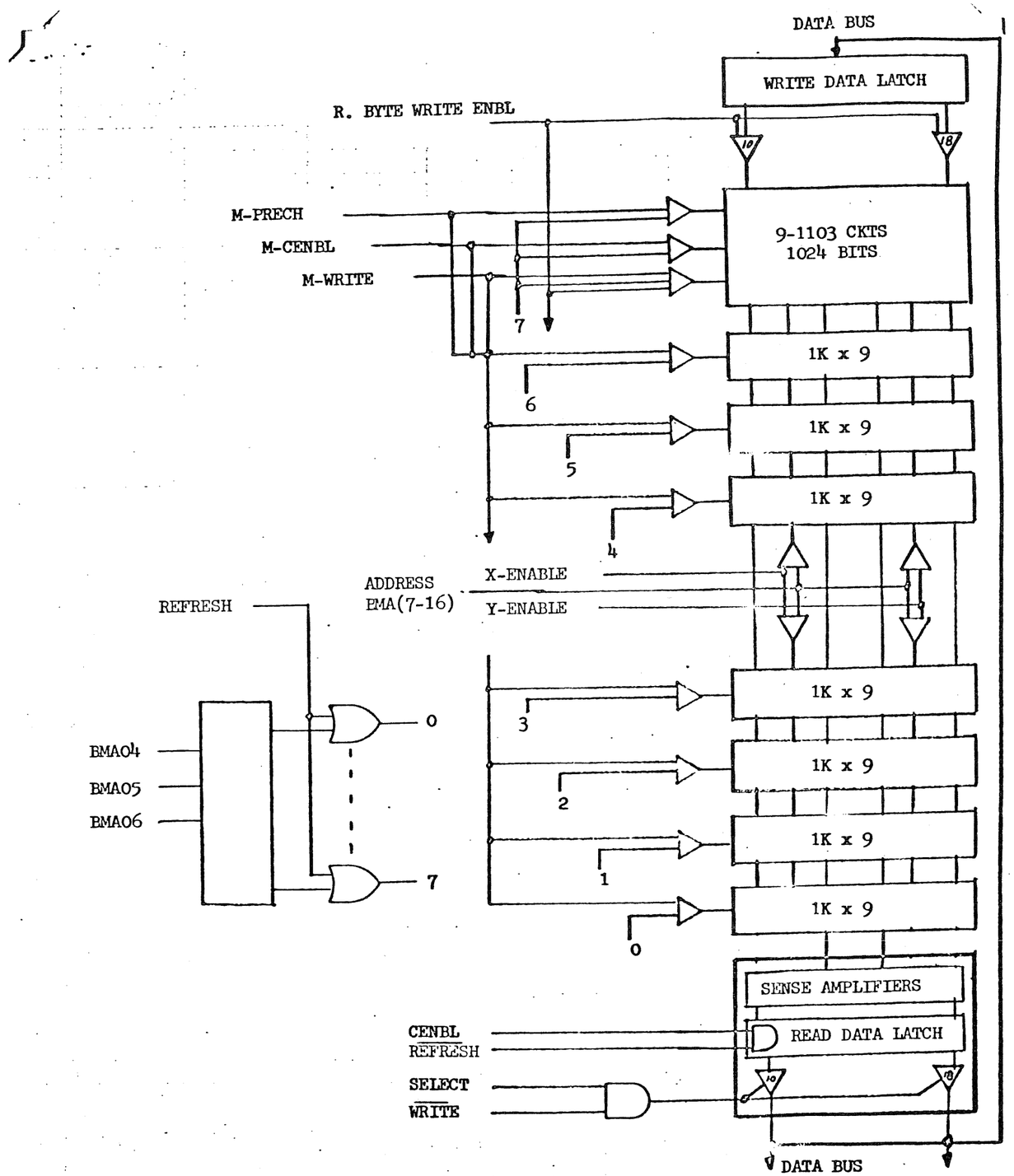

DATA BUS
WRITE DATA LATCH
R. BYTE WRITE ENBL
M-PRECH
M-CENBL
M-WRITE
9-1103 CKTS
1024 BITS
1K x 9
1K x 9
1K x 9
1K x 9
1K x 9
1K x 9
1K x 9
1K x 9
ADDRESS
PMA(7-16)
X-ENABLE
Y-ENABLE
REFRESH
BMA04
BMA05
BMA06
SENSE AMPLIFIERS
READ DATA LATCH
CENBL
REFRESH
SELECT
WRITE
DATA BUS

Fig 4

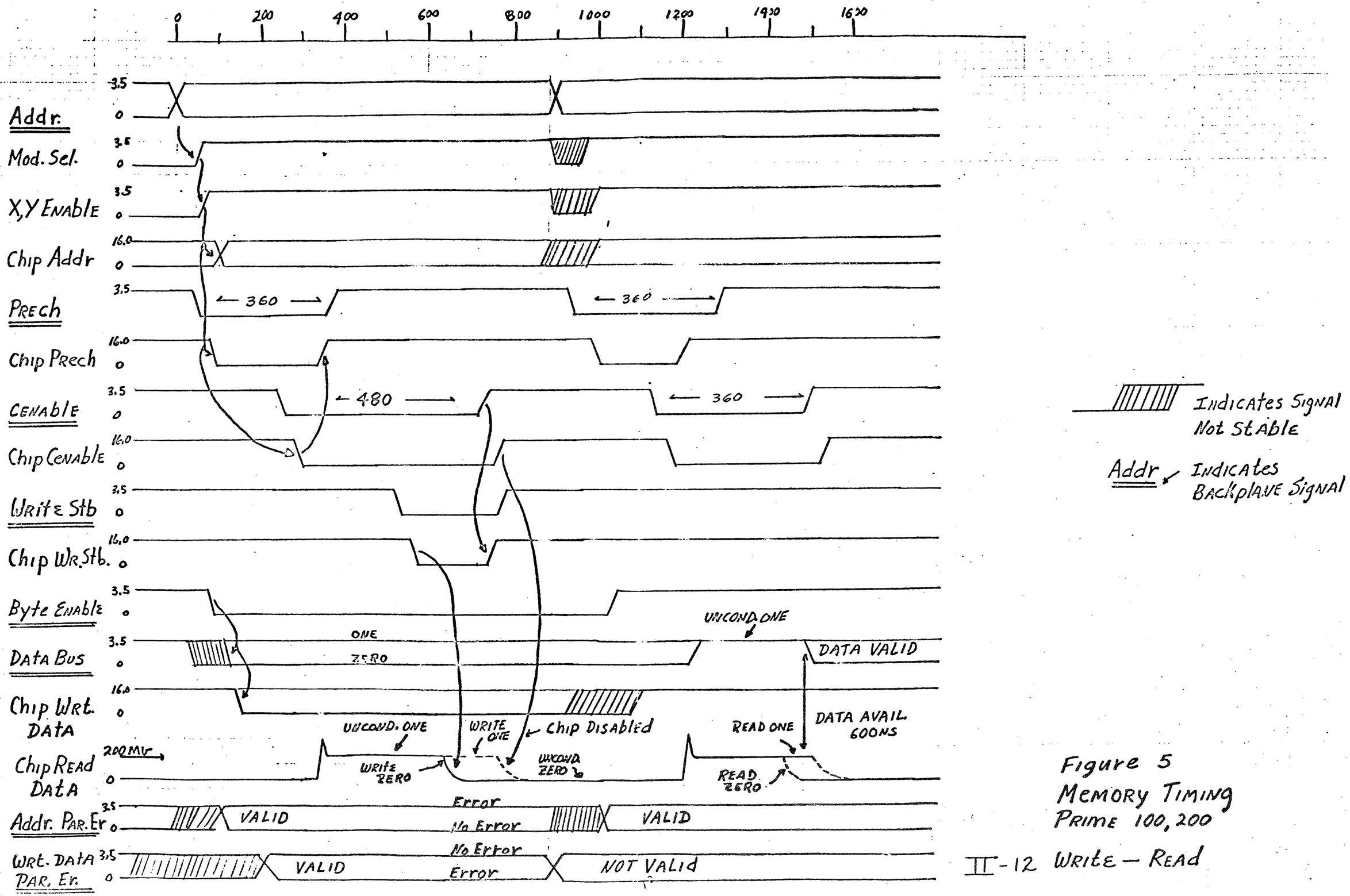


Figure 5
Memory Timing
Prime 100, 200

SCHOTTKY BIPOLAR 3208A, 3408A

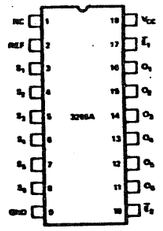
The Intel 3208A is a high speed hex sense amplifier designed to sense the output signals of the 1103 memory. The device features two separate enable inputs each controlling the output state of three sense amplifiers, and a common voltage reference input. OR-tie capability is available with the 3208A open collector TTL compatible output.

The 3408A is a hex sense amplifier with a latch circuit connected to each amplifier. The sensed data may be stored in the latches through application of a write pulse. The 3408A has three-state TTL outputs, hence in the non-enabled state the outputs float allowing wire-OR memory expansion. The latches may be bypassed by grounding the write input pin. Under this condition, the 3403A functions as a hex sense amplifier.

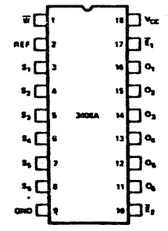
The 3208A and 3408A operate from a single +5 volt power supply. Device performance is specified over the complete ambient temperature range of 0°C to 70°C and over a V_{CC} supply voltage range of 5 volts ±5%. The 3208A and 3408A are packaged in an 18 pin plastic dual in-line package.

PIN CONFIGURATIONS

3208A



3408A

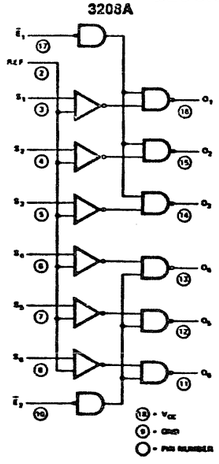


PIN NAMES

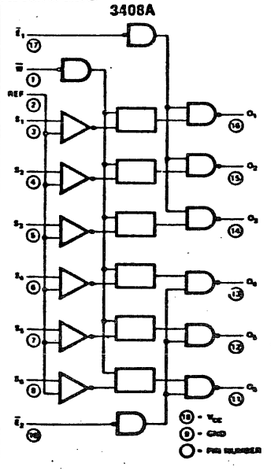
$S_1, S_2, S_3, S_4, S_5, S_6$	SENSE AMP INPUTS
$\overline{E}_1, \overline{E}_2$	ENABLE INPUTS
REF	REFERENCE INPUT
$O_1, O_2, O_3, O_4, O_5, O_6$	OUTPUTS (Non-inverting)
$\overline{W}$	WRITE INPUT (3408A only)

BLOCK DIAGRAMS

3208A



3408A



SCHOTTKY BIPOLAR 3205, 3404

3205

The 3205 decoder can be used for expansion of systems which utilize memory components with active low chip select input. When the 3205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 3205 allow easy memory expansion. For very large memory systems, 3205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

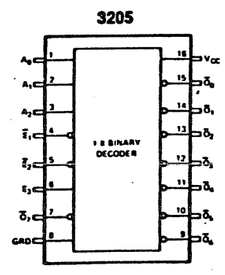
3404

The Intel 3404 contains six high speed latches organized as independent 4-bit and 2-bit latches. They are designed for use as memory data registers, address registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low".

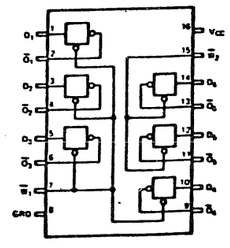
The Intel 3404 is packaged in a standard 16-pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION

3205



3404



MOS 1103 (RAMs)

The Intel 1103 is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

It is a 1024 word by 1 bit random access memory element using normally off *P*-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18 pin dual in-line package. It uses dynamic circuitry and primarily dissipates power only during precharge.

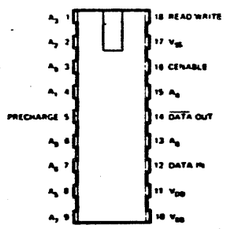
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds.

A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied.

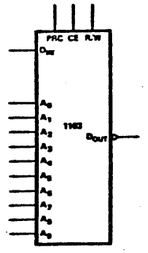
The Intel 1103 is fabricated with **silicon gate technology.** This **low threshold** technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



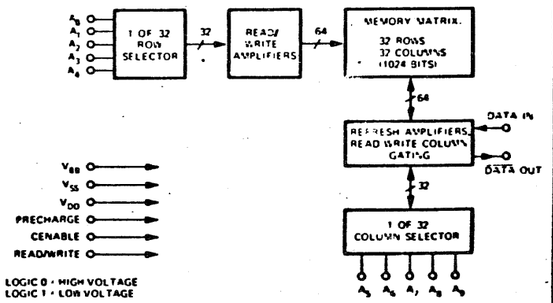
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	PRC	PRECHARGE INPUT
A_0–A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	D_{OUT}	DATA OUTPUT

BLOCK DIAGRAM

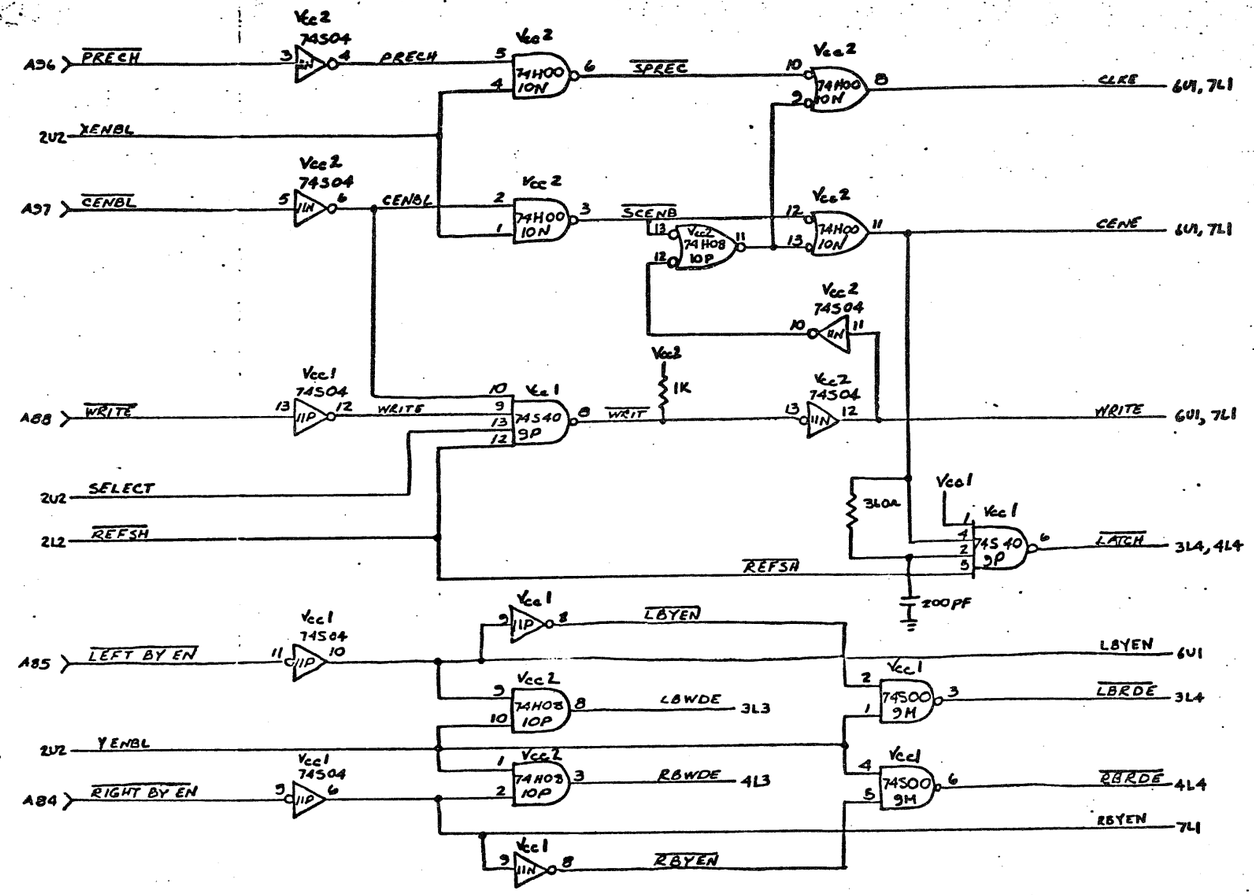


MEMORY SIGNAL NAME CROSS REFERENCE LIST

CPU	MEMORY	DESCRIPTION
BMC PRCH-	PRECH-	Pre-charge
BMCCENBL-	CENBL-	Chip Enable
BMCWSTRB-	WRITE-	Write Strobe
BMCWLB-	LEFT BY EN-	Write Left Byte
BMCWRB-	RIGHT BY EN-	Write Right Byte
BMCDINH-	DATA INHIBIT-	Data Inhibit
BMA 99-	MAD 99-	
BMA 00-	MAD 00-	
BMA 01-	MAD 01-	
BMA 02-	MAD 02-	
BMA 03-	MAD 03-	
BMA 04-	MAD 04-	
BMA 05-	MAD 05-	
BMA 06-	MAD 06-	
BMA 07-	MAD 07-	"Y" Enable
BMA 08-	MAD 08-	"Y" Enable
BMA 09-	MAD 09-	"Y" Enable
BMA 10-	MAD 10-	"Y" Enable
BMA 11-	MAD 11-	"Y" Enable
BMA 12-	MAD 12-	"X" Enable
BMA 13-	MAD 13-	"X" Enable
BMA 14-	MAD 14-	"X" Enable
BMA 15-	MAD 15-	"X" Enable
BMA 16-	MAD 16-	"X" Enable
BMCRFSH-	RFSH-	
BMCSELV-	SELB-	Missing Memory Module Trap
BMALP-	MADLP-	
BMAPELA	ERLAP-	

CPU	MEMORY	DESCRIPTION
BMAPER+	ERRAP-	
BMDLP+	MDATLP-	
BMD01+	MDAT01-	
BMD02+	MDAT02-	
BMD03+	MDAT03-	
BMD04+	MDAT04-	
BMD05+	MDAT05-	
BMD06+	MDAT06-	
BMD07+	MDAT07-	
BMD08+	MDAT08-	
BMDPEL-	ERROR DATA LEFT-	Parity Error Left Byte
BMDPER-	ERROR DATA RIGHT-	Parity Error Right Byte
BMD09+	MDAT09-	
BMD10+	MDAT10-	
BMD11+	MDAT11-	
BMD12+	MDAT12-	
BMD13+	MDAT13-	
BMD14+	MDAT14-	
BMD15+	MDAT15-	
BMD16+	MDAT16-	
BMDRP+	MDAT17-	

ZONE	ISS. C	DESCRIPTION	DATE	APPROVAL
	C6	RELEASED TO MFG "BRIDGE" EC. 51	3-29-76	



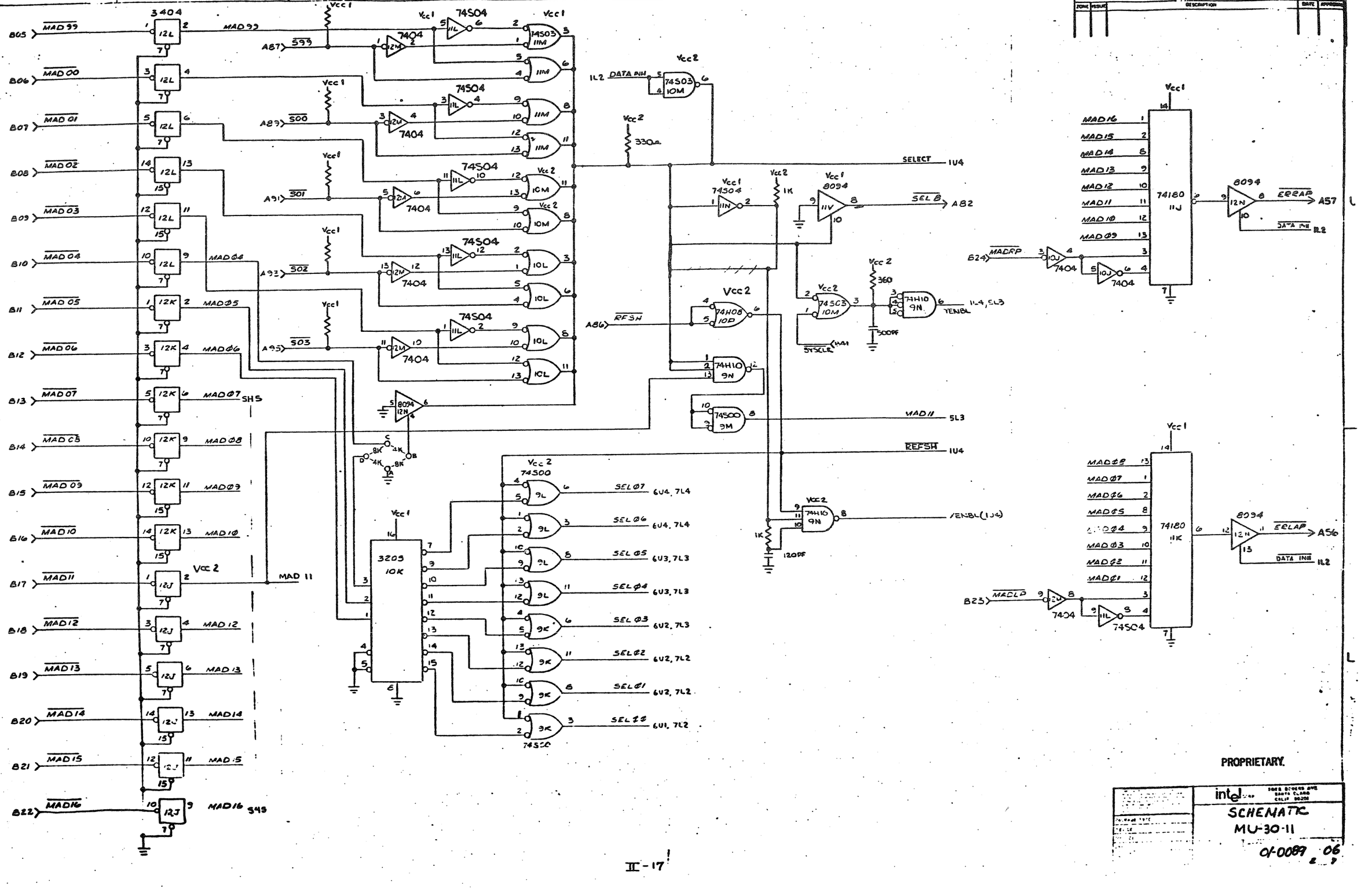
POWER PROTECT

ECN 51

PROPRIETARY

intel 3065 BOWERS AVE. SANTA CLARA CAL. P. 95051

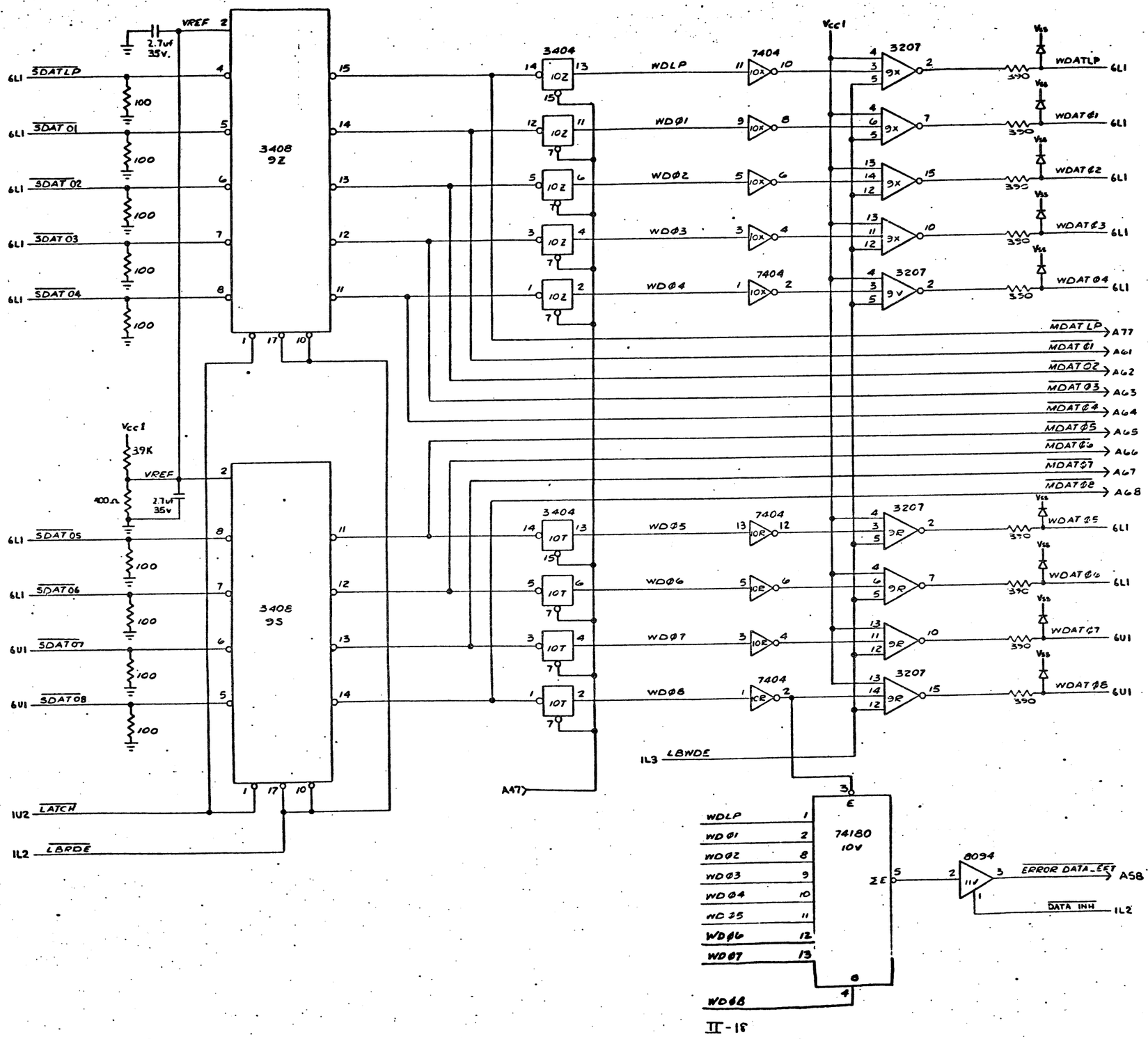
SCHEMATIC .
MU-30 11
01-0089 06



PROPRIETARY.

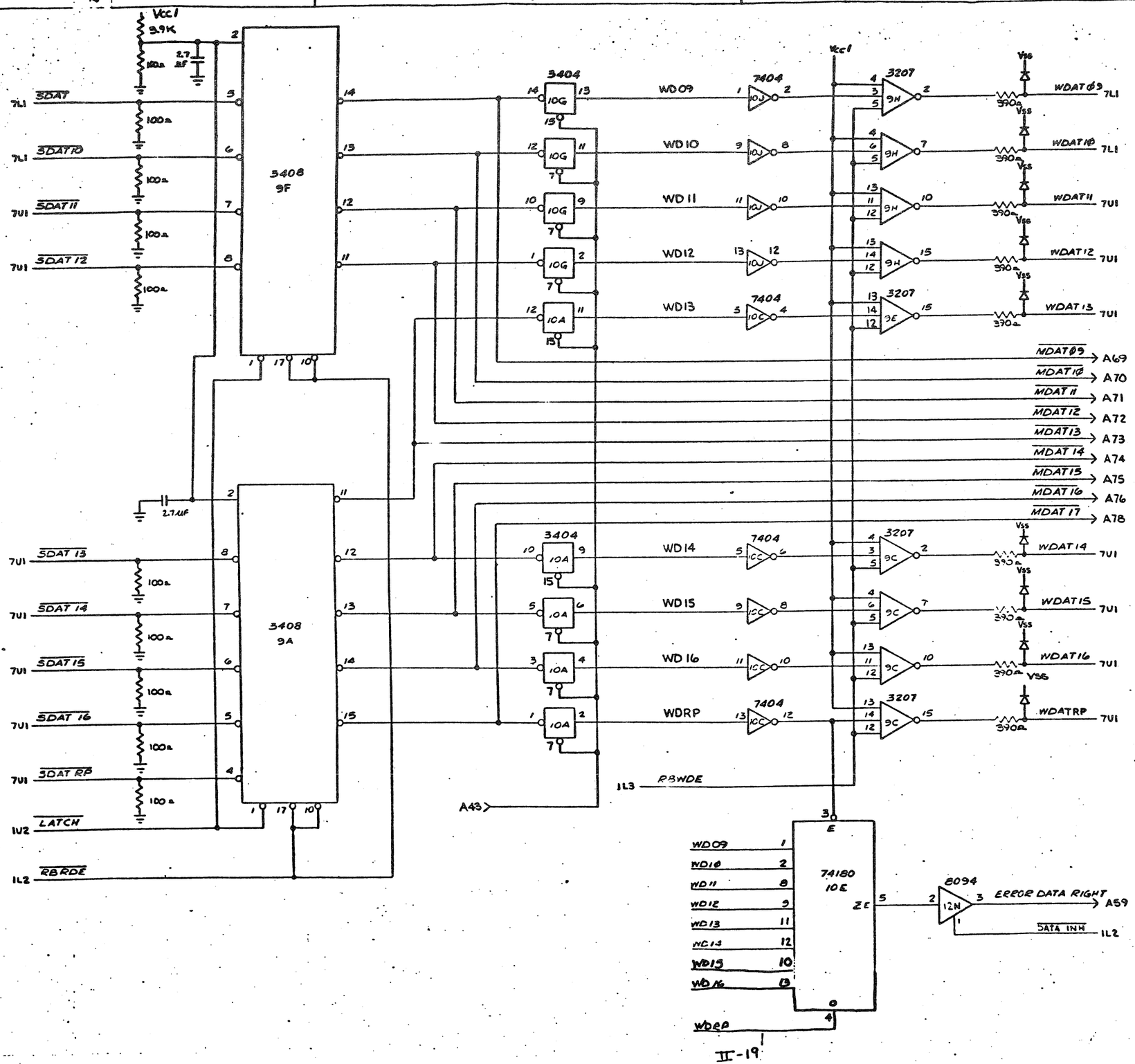
intel SCHEMATIC MU-30-11

01-0089-06



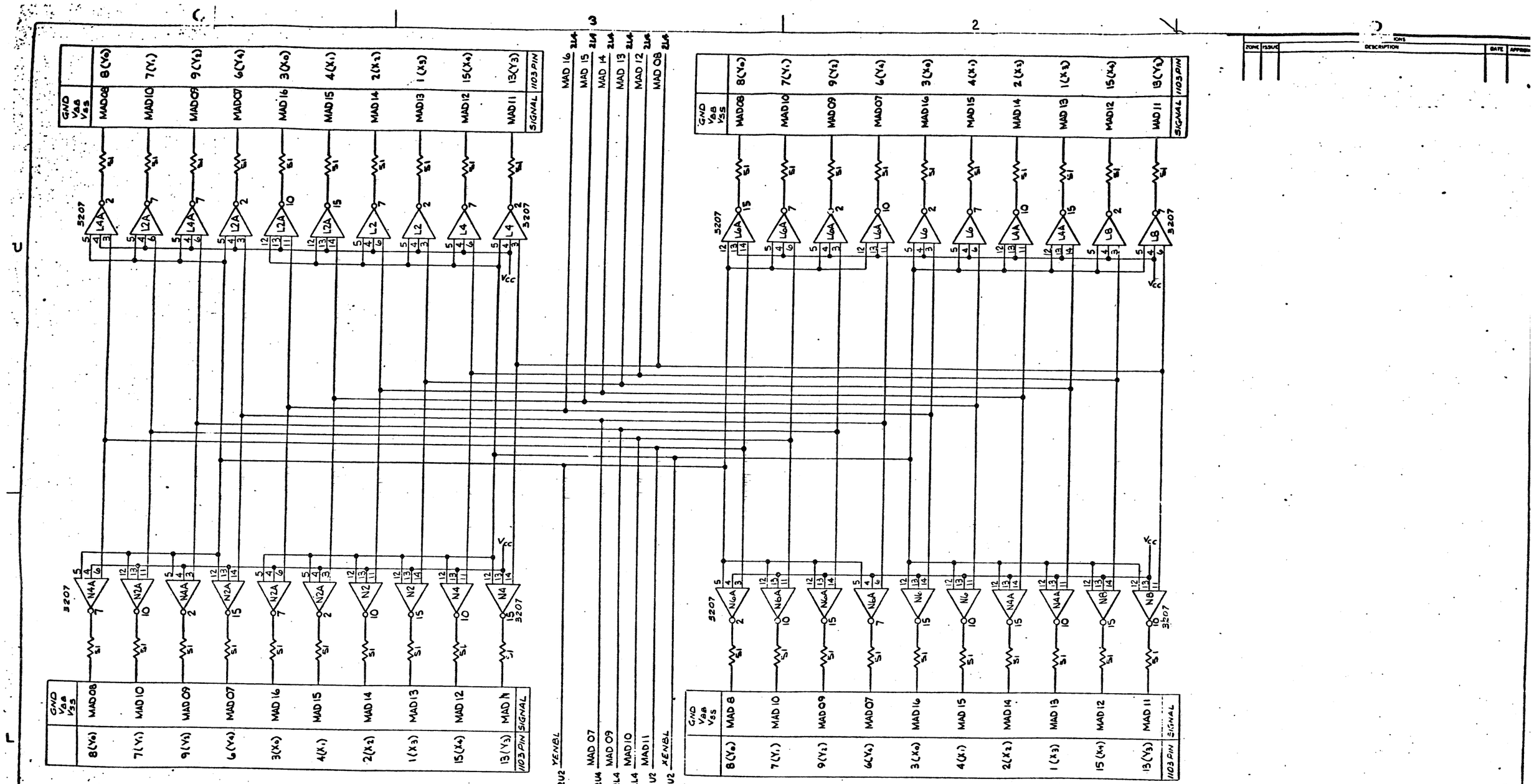
PROPRIETARY.

intel	3065 BOWERS AVE SANTA CLARA CALIF. 95051
PACKAGE TYPE:	SCHEMATIC
DEVICE	MU-3011
DIE INST	
SIZE	DRAWING NO. 01-0089



PROPRIETARY

	intel corp. 3065 BOWERS AVE SANTA CLARA CALIF. 95051
PACKAGE TYPE	SCHEMATIC
DEVICE	MU-3011
DWG. SIZE	DRAWING 01-0089 REV 06

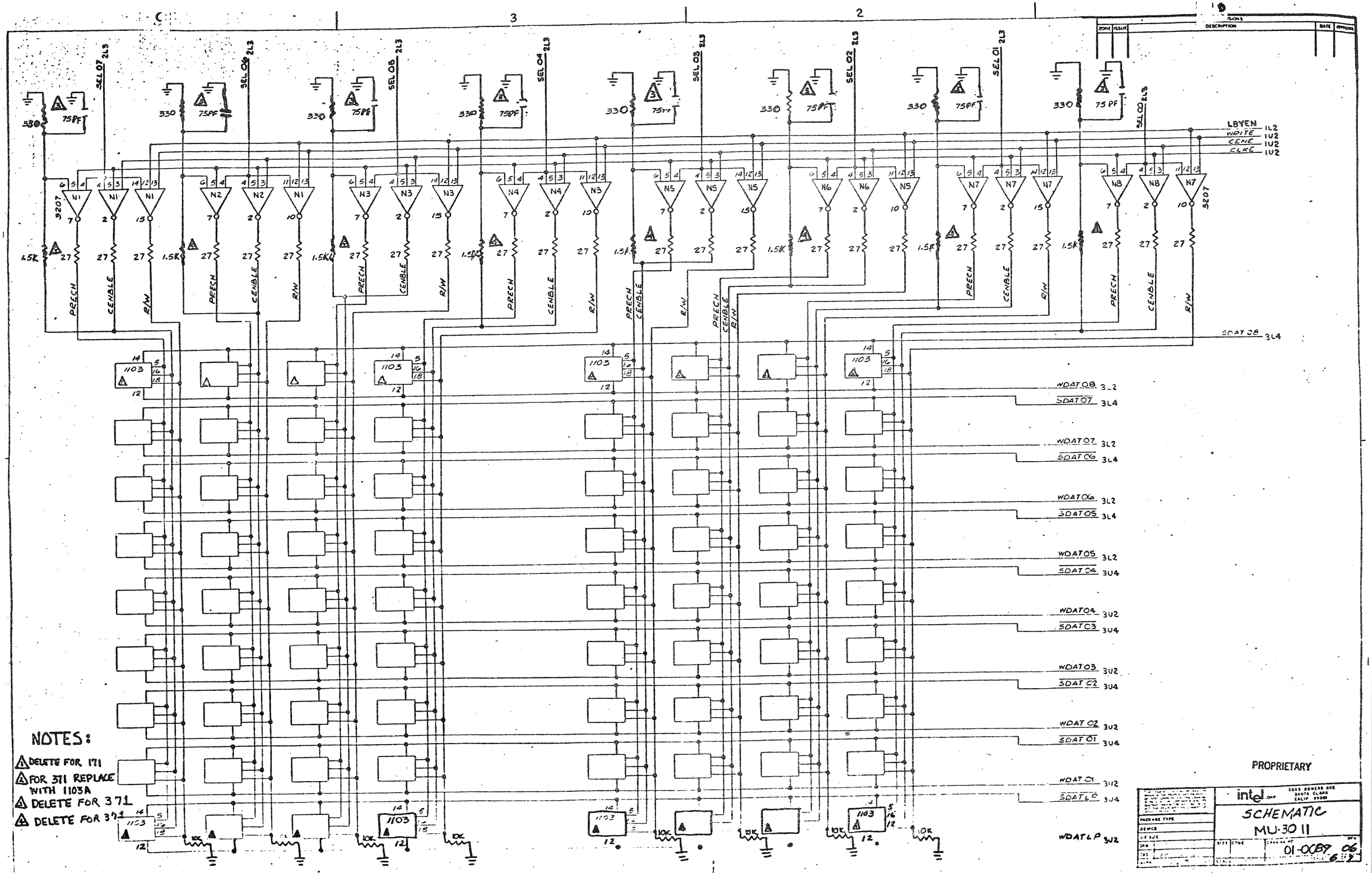


PROPRIETARY

intel 3065 BOWERS AVE SANTA CLARA CALIF. 95051

SCHEMATIC
MU-3011

01-0089 06



NOTES:

1. DELETE FOR 171
2. FOR 371 REPLACE WITH 1103A
3. DELETE FOR 371
4. DELETE FOR 371

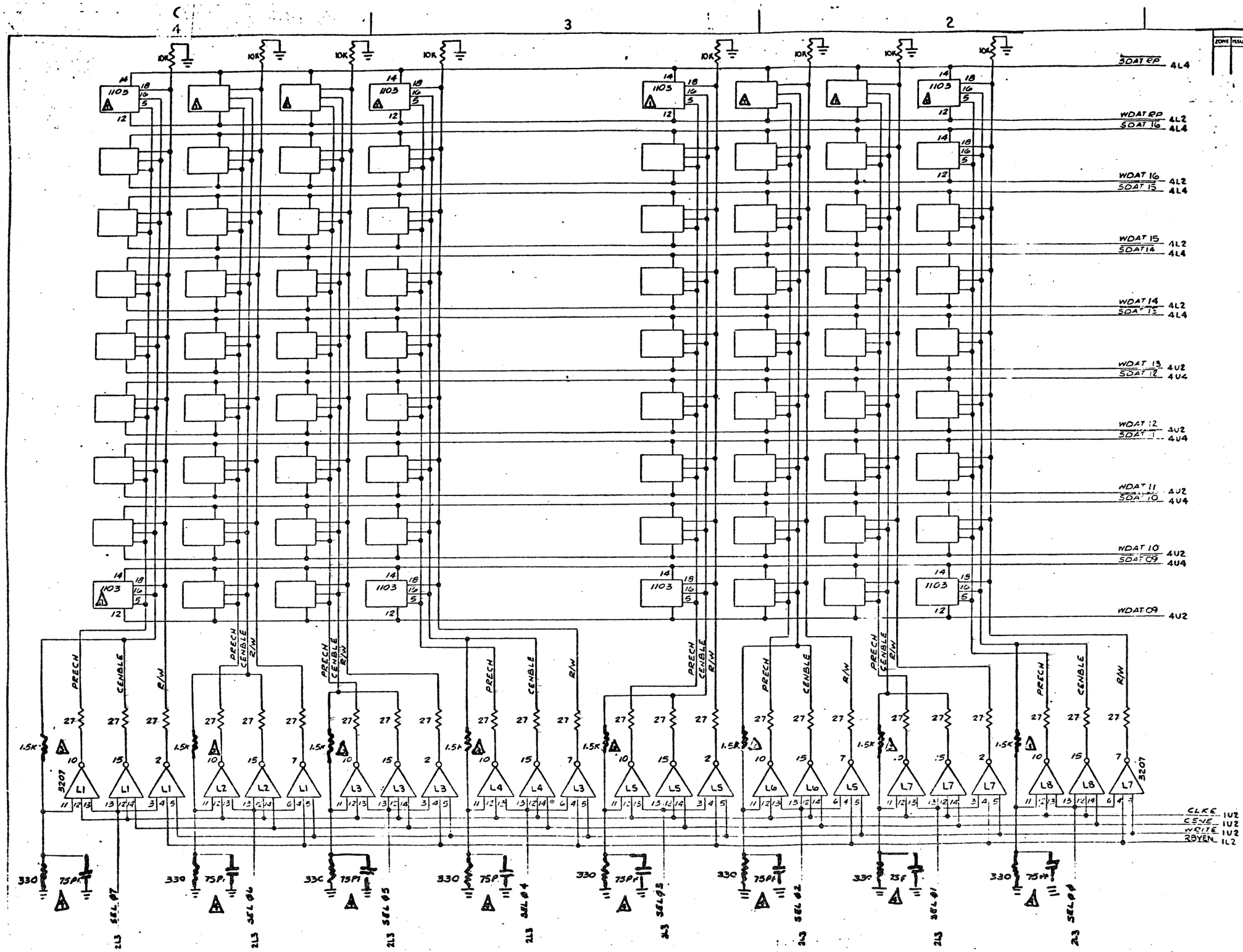
PROPRIETARY

intel corp 3065 BOWERS AVE SANTA CLARA CALIF 95051

SCHEMATIC MU-3011

SIZE C CODE 01-0089 REV 06

SHEET 6 OF 7



NOTES:

1. DELETE FOR 171
2. FOR 371 REPLACE WITH 1103A
3. DELETE FOR 371
4. DELETE FOR 371

PROPRIETARY

intel

SCHEMATIC

MU-3011

01-0089-06

PRIME COMPUTER INC.
NATICK MASS.

DWN. | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: MEMORY - MOS 8K x 18 - 211

BOM REV.

CHNG: SHT. 1 OF __

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
		ICD90017	7								3404 - Latch Inital	
		ICD90018	4								3405A - Sense Amp Inital	
		ICD90015	1								3205 - 1 of 0 Decode Inital	
		ICD90016	28								3209 - Quad Driver Inital	
		ICD00059	2								7404 - Hex Inverter Gate	
		ICD90030	6								7170 - Parity Checker	
		ICD00085	3								74S00 - Gate	
		ICD00086	3								74S04	
		ICD90007	3								74S03	
		ICD90034	1								74S40	
		ICD00009	1								74H08	
		ICD00030	1								74H10	
		ICD00195	5								7404	
		ICD00025	1								74H00	
		ICD90014	144								1103 Memory Device	
			1								Fuse - 1.5Amp Littlefs.	
			1								Fuse - 0.75Amp Littlefs.	
			18								Diode - IN914	
			2								Diode -	
			16								Capacitor - Mica 75pf 500V	
			132								Capacitor - Tantalum 2.7uf 30V	
			22								Capacitor - Tantalum 47uf 6.0V	

PBP

H-23

PRIME COMPUTER INC.
NATICK MASS.

DWN. | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: Memory - MOS 8K x 18

BOM REV.

NHA: SHT. 2 OF __

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
			4								Capacitor Tantalum 47uf @ 35V	
			3								Capacitor Tantalum 6.0uf @ 35V	
			43								Resistor 1/4 Carbon 5% 27-Ω	
			40								51-Ω	
			2								100-Ω	
			18								200-Ω	
			19								330-Ω	
			18								3.0-Ω	
			4								1.0K	
			16								1.5K	
			2								3.9K	
			16								10.0K	
			5								300K	
			1								CAPACITOR, MICA 1000pf ±5% 15V	
			1								200pf	
			1								500pf	
			1								PC BOARD	
			1								HANDLE ASSEMBLY	

PBP-004

DATE: September 19, 1975

TO: Engineering & Programming Staff

FROM: Ross E. Roberts

SUBJECT: 32K Memory Module Description

Each memory module contains module selection logic, data bus interface, MOS storage devices, MOS driver circuits and sense amps. Parity checkers for address and write data are also included. The module presents a completely TTL interface to the memory bus and receives all its timing and control for the CPU via this bus. The module is designed to operate with up to seven other similar modules sharing a common bus (backplane). The following configurations are available:

	Model No.
8,192 words x 18 bits	1208-B85
8,192 words x 16 bits	1208-B65
16,384 words x 18 bits	1216-B85
16,384 words x 16 bits	1216-B65
32,768 words x 18 bits	1232-B85
32,768 words x 16 bits	1232-B65

Figure 1 is a block diagram of a 32K memory module. The storage matrix is made up of solid state memory devices each of which are organized as 4096 words by one bit. A total of 144 devices yields a capacity of 32K words by 18 bits. The additional configurations tabulated above are achieved by depopulating the module.

Data Bus (Positive True, ONE = +5 V)

The eighteen bit data word is comprised of two eight bit bytes with a parity bit for each byte. The 18 read-data lines (memory output), and the 18 write-data lines (memory input) are duplexed onto one 18 wire bus designated BMD. Tri-state drivers are used exclusively for this function. Data is stored and retrieved without polarity inversion.

The parity checker associated with the data bus is always active and indicates the state of bus parity during read or write cycles; however, it is only tested by the CP during write cycles.

Address Bus (Negative True, ONE = 0 V)

The three high order bits of memory address are used to determine which module is to be selected. The selected module

generates a select back signal that is tested by the CP. The absence of this signal results in a missing module trap. The select line on the active memory module enables clock drivers, address drivers, and enables the modules tri-state drivers on the data bus.

Address bits BMA02, 03 and 04 select a 4K block of the 32K storage matrix and direct the appropriate clocks to this row of devices. Consequently, during normal read and write cycles, only 18 devices out of 144 are active; the remainder are in a low power state.

The 12 least significant addresses (BMA05 through BMA16) directly address the storage elements and are internally decoded. These addresses, then, uniquely determine the word address within a 4K block.

Address parity is checked by byte (nine bits) and errors are indicated as to left or right byte. An error will cause a logic low (0 volts) on the error lines.

Figure 2 shows the fields and connector pins for the address and data fields.

Refresh

The storage device stores data on parasitic junction capacitors. Since these gradually lose charge through junction leakage, it is necessary to rewrite or refresh the data periodically. The refresh operation is accomplished by processing a read cycle on each of the 4096 bits and must be repeated every two milliseconds.

The storage device is organized as 64 rows and 64 columns. Refreshing a single row will automatically refresh all 64 columns associated with that row. Therefore, on an individual device the 64 rows can be sequentially refreshed one cycle each 32 u-sec completing the entire process in two milliseconds.

During refresh operations the module select logic and the row select logic are overridden and every storage device in the system is selected. Therefore, Row N(1-64) of all devices sees a refresh cycle simultaneously. The entire memory system is thus refreshed with the value of N incrementing each 32 u-sec.

Detailed Discussion

Figures 3 and 4 are more detailed diagrams of the blocks presented in Figure 1. All signals are treated as positive true for ease of discussion. Note here that in actual practice the opposite

may be true. The actual implementation of these blocks may be found on the LBD noted in the figures. Address and data latches are provided on the module. Their use, however, is optional by virtue of a jumper which, when installed, causes the latch to behave as a simple inverter. (The jumper is present for use in the PRIME 100, 200 and 300.)

Re: Figure 3 -- Each module slot in a PRIME backplane has five lines statically coded as gnd or +5 volts. (Ref: PE-T-169, 1/8/75, J. Sheahan, System Configurations with 32K Memory Boards.) The uppermost slot is coded all ZEROS (+5V negative true). This slot represents the least significant module address, namely the first 32K of memory. The variable addresses (BMA) are compared against the fixed slot code to determine if the CP is attempting to select a specific module. As stated previously, a select signal is returned to the CP and also gates signals called X and Y enable. These in turn permit the chip address drivers to present the addresses existing at the module inputs to the storage devices. The function denoted X enable is an "OR" of select and refresh in order to allow the necessary refresh addresses to be available to the storage devices. It can be seen then that all modules in the system are active during the execution of a "REFRESH" command.

Device Clocks

Each 4096x1 storage device requires the following signals to cause it to function as a memory. Chip Enable (CENBL), Read/Write (WRITE), Chip Select (CS), Addresses (MAD00-MAD11), and Data In (WDATXX). The proper application of these signals results in the storage and/or retrieval of information via the Data Out pin (SDATXX).

The storage devices require that CENBL be a positive true signal with an amplitude of 12 volts. (Note that this is the only signal with an amplitude which is dramatically different from the TTL levels normally encountered in digital systems.) CENBL begins a chip cycle and executes the necessary preconditioning of internal busses characteristic of dynamic RAMS. CENBL, in the devices being discussed, performs the function of PRECH as well as those performed by CENBL in the 1103. (Ref: Memory Module Description, J. E. Sheahan, July 25, 1973, p.3.) The WRITE signal, when active, causes the data presented as WDAT to be stored in a unique location defined by MAD00-MAD11. The absence of WRITE causes the data previously stored or the data existing in the unique location defined by MAD00-MAD11 to be presented at the data output pin as SDATXX. (More detailed information on the operation of these devices may be obtained from the TI Semiconductor Memory Data Book or from the Intel Application Note AP-10 "Memory System Design with the Intel 2107B 4K RAM".)

Each module is sent a signal (BMCPRCH-) which starts a cycle. The memory module determines from the addresses presented on the

bus whether or not it is the selected module. This results in the gating of CENBL and WRITE and Addresses and data to the chips for the selected module, depending on the type (i.e., READ or WRITE) of cycle to be executed. The CENBL and WRITE signals are generated by a delay line timing chain which is triggered into activity by the receipt of BMCPRCH-. CENBL is then steered by virtue of the row decode to one row of storage elements. The WRITE signal is gated by the CENBL signal and the absence of REFRESH.

There exists one active CENBL driver for each row of 18 storage devices and one WRITE driver for each two columns of 16 storage devices. The WRITE drivers are gated by, in addition to CENBL, a byte enable signal which permits the storage of nine bits in a word. Note that both bytes will receive a CENBL but only one byte will receive the necessary WRITE command.

Data Output from the devices is a TTL level with a tertiary state (i.e., tri-state output). This output is applied to a latch where it is retained until the next READ cycle on that module. The latch outputs are isolated by a non-inverting tri-state buffer from the backplane bus. These tri-state buffers are maintained in a high impedance state during both WRITE cycles and REFRESH cycles.

System Timing

All memory module timing is controlled on the module by the previously mentioned delay line except of course those input signals at the interface. The diagram of Figure 5 is illustrative of a typical READ cycle followed by a WRITE cycle.

UNIQUE CHARACTERISTICS

Power

The storage devices and their attendant drivers require voltage levels not normally associated with the system power. The requirement for the storage devices is as follows. VSS (gnd), VDD (+12V), and VBB (-5V). Gnd is, of course, no problem. +12V, however, is not available in sufficient wattage to power all the storage. There is a 16 volt supply which was used for the 8K modules. (Ref: LDS 1624 "P100/200/300 Control Panel, Memories and Power Supplies Logic Diagrams.") This is taken onto the 32K module and regulated to +12V on the module by two series pass type voltage regulators. A simple regulator of similar type provides a clamping voltage of +13V for the CENBL drivers. The CENBL drivers also utilize +16V from the system for a pull-up voltage. The address drivers use the system +5V for a clamp voltage and the locally supplied +12V for a pull-up voltage.

The negative potential required by VBB is also generated on the board by a voltage inverter circuit whose output is zener regulated to the required level. The 16 volt bus is protected by a fuse in order to prevent the destruction of the drivers in the event that +5V is not present to the drivers. The condition where the high voltage is present and the +5V is not, is a destructive condition for the drivers.

Signal Levels

All signals to the storage devices are 0 to +5V with the one exception of CENBL as previously discussed. All outputs and inputs to the module are TTL compatible.

Bus Latches

There are latches on the module for Address and Write Data. For the PRIME 200 the clock lines are grounded on the CP board making the latch look like a simple logic inverter.

Refresh

A refresh cycle will cause a memory busy every 32 u-sec for the length of a normal write cycle. The address during refresh cycles will repeat every 64 refresh cycles. Missing refresh cycles may cause the memory to drop ONE's, but will not cause ONE's to be picked.

Byte Enables

Byte Enable must be active to process a write cycle. One byte may be written while the other is read by proper manipulation of Byte Enables.

Data Inhibit

An active data inhibit will force all signals from memory to a tri-state disconnect.

Ross E. Roberts

Attachments: Figure 1,2,3,4&5

/nf

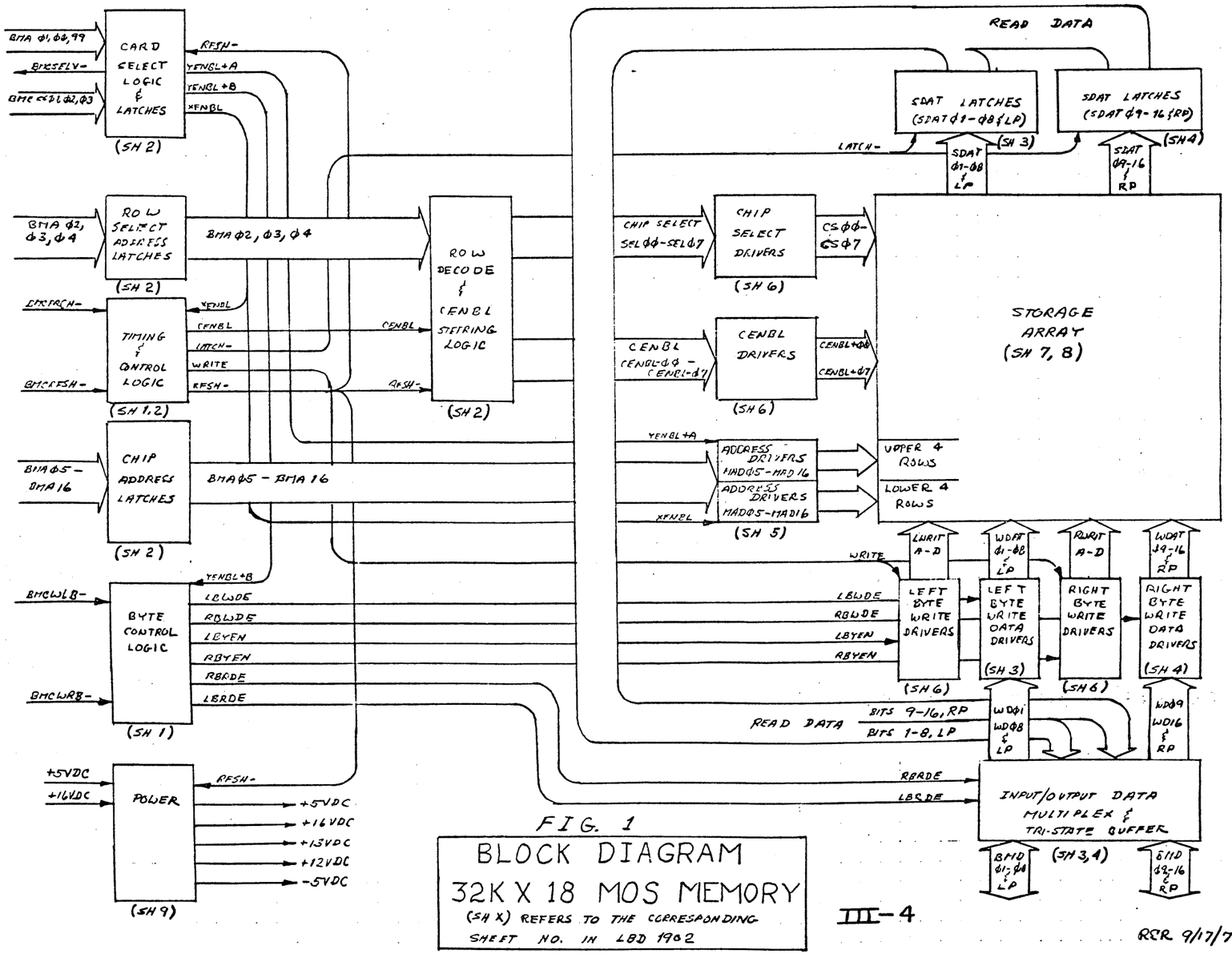


FIG. 1

BLOCK DIAGRAM

32K X 18 MOS MEMORY

(SH X) REFERS TO THE CORRESPONDING SHEET NO. IN LBD 1902

RER 9/17/75

MSB = Left most bit of each sector

	MSB		LEFT MOST BITS									RIGHT MOST BITS										
VARIABLE SLOT ADDRESS	BΦ5	BΦ6	BΦ7	BΦ8	BΦ9	B1Φ	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	A56	A57
	BMA 99	BMA ΦΦ	BMA Φ1	BMA Φ2	BMA Φ3	BMA Φ4	BMA Φ5	BMA Φ6	BMA Φ7	BMA Φ8	BMA Φ9	BMA 1Φ	BMA 11	BMA 12	BMA 13	BMA 14	BMA 15	BMA 16	BMA PL-	BMA PR-	BMA PEL+	BMA PER+
FIXED SLOT ADDRESS	A87	A89	A91	A93	A95																	
	BMC SS01-	BMC SS02-	BMC SS03-																			
8K MODULE USAGE	MEM EXT.	SLOT SELECT	ROW SELECT	CHIP COLUMN (Y) SELECT	CHIP ROW (X) SELECT (Active for Refresh)														ADDRESS PARITY BITS		ADDRESS PARITY ERROR	
	SLOT COMPARE																					
32K MODULE USAGE	SLOT COMPARE		ROW SELECT		CHIP COLUMN (Y) SELECT						CHIP ROW (X) SELECT (Active for Refresh)								ADDRESS PARITY BITS		ADDRESS PARITY ERROR	

ADDRESS BIT MNEMONIC, PIN ASSIGNMENT, and USAGE TABLE

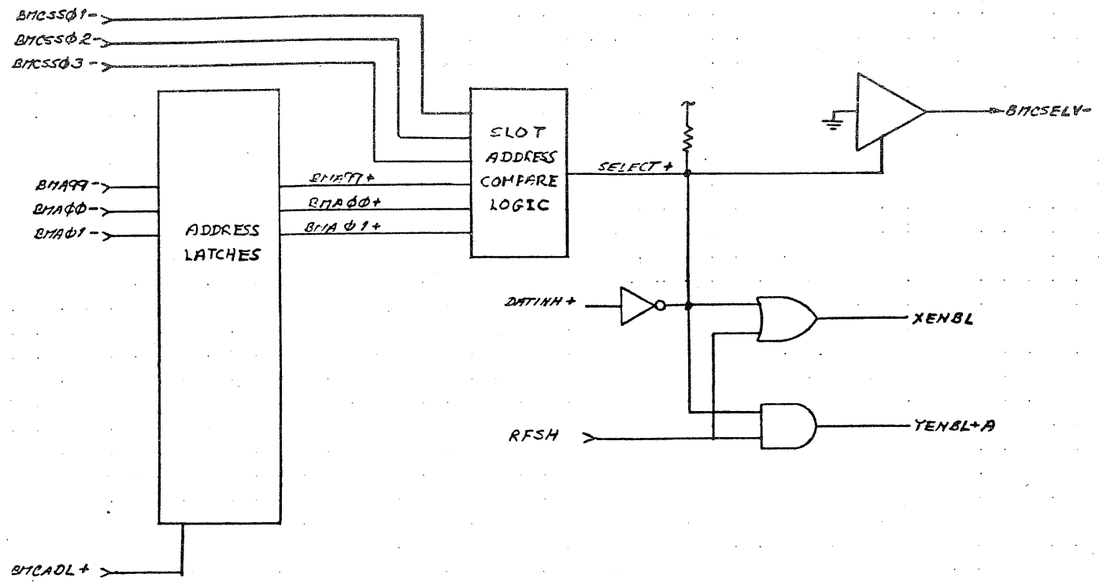
A61	A62	A63	A64	A65	A66	A67	A68	A69	A7Φ	A71	A72	A73	A74	A75	A76	A77	A78	A58	A59
BMD Φ1	BMD Φ2	BMD Φ3	BMD Φ4	BMD Φ5	BMD Φ6	BMD Φ7	BMD Φ8	BMD Φ9	BMD 1Φ	BMD 11	BMD 12	BMD 13	BMD 14	BMD 15	BMD 16	BMD LP	BMD RP	BMD PEL-	BMD PER-

LEFT MOST DATA BITS	RIGHT MOST DATA BITS	DATA PARITY BITS	DATA PARITY ERROR

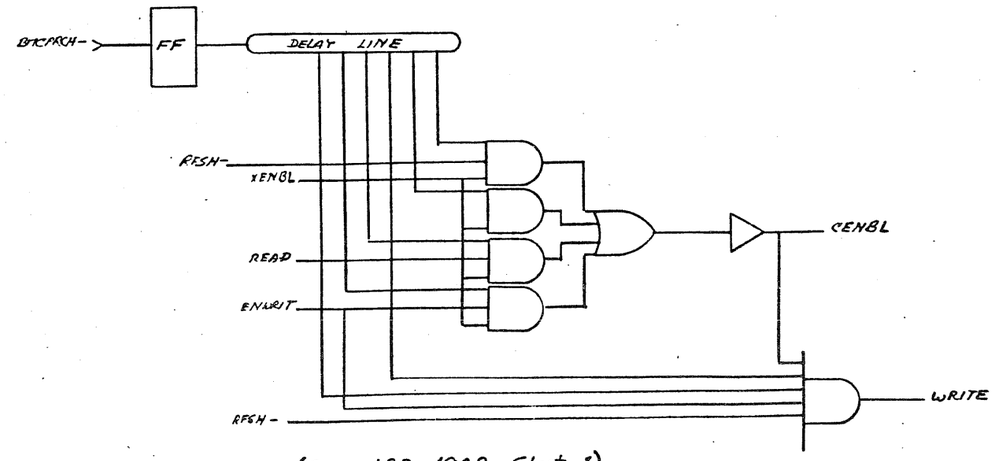
MSB = Left most bit of each sector

DATA BIT MNEMONIC, PIN ASSIGNMENT, and USAGE TABLE

FIG. 2



(See LBD 1902 Sheet 2)



(See LBD 1902 Sheet 1)

FIG. 3

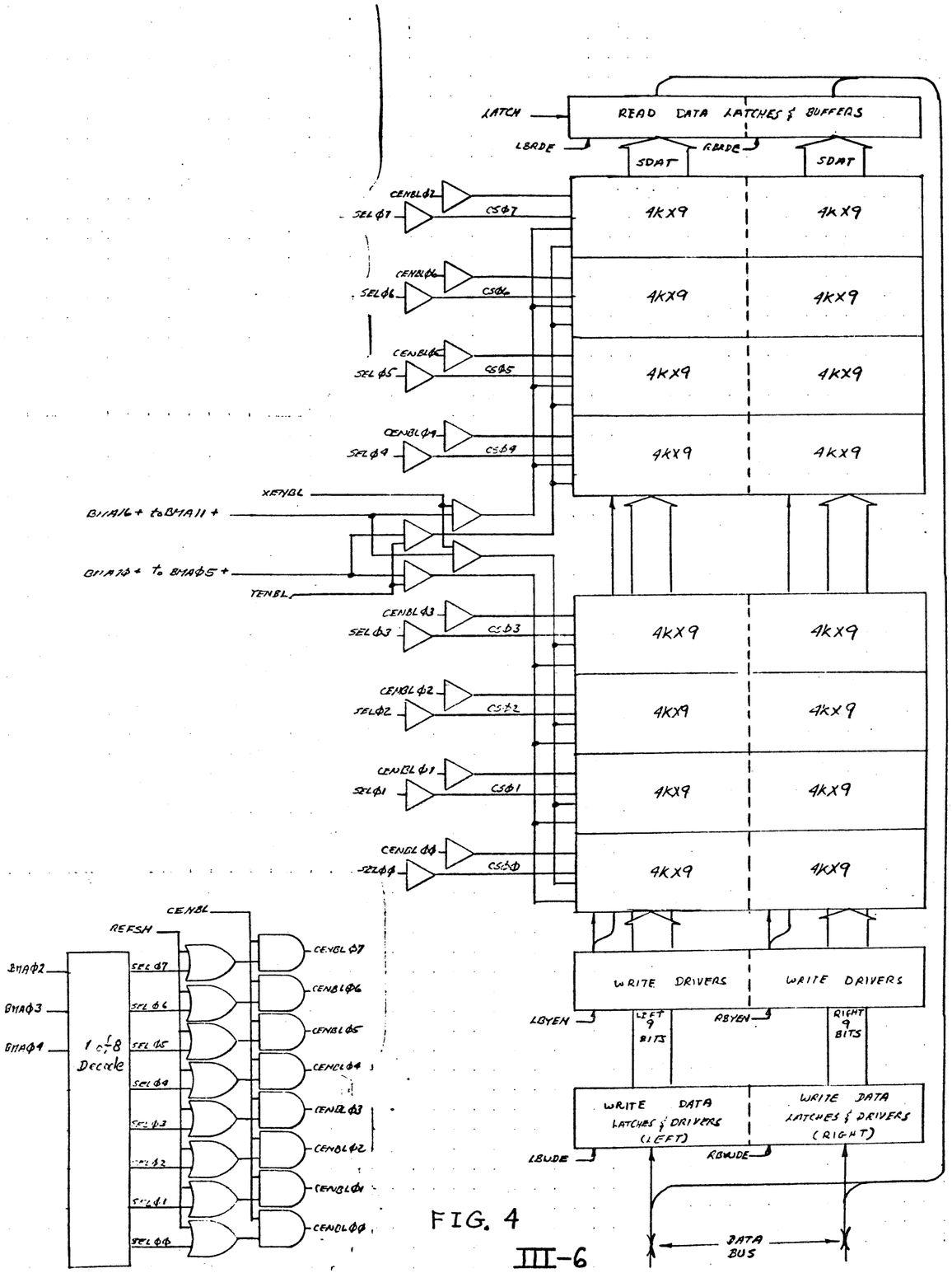
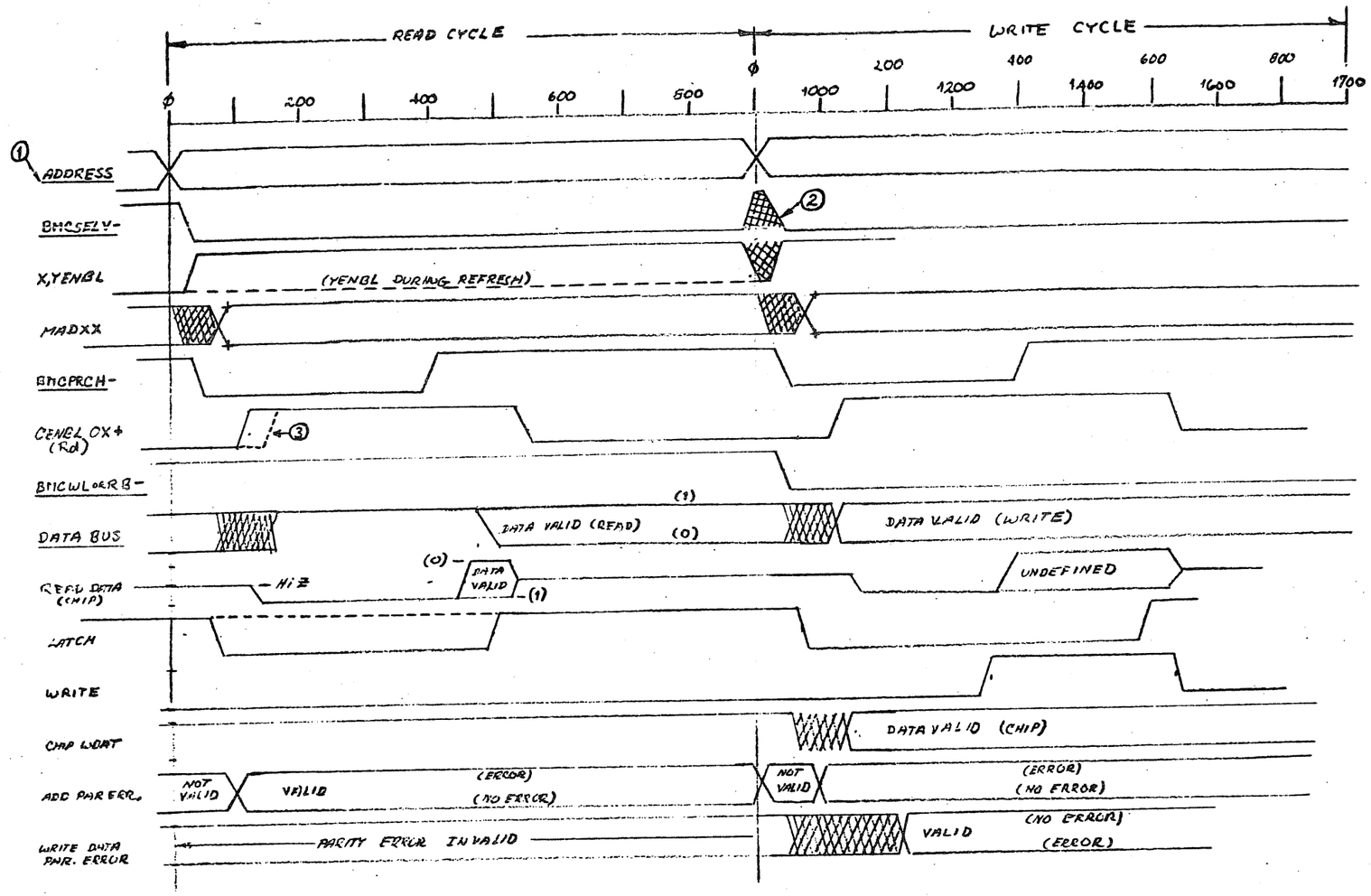

LATCH
READ DATA LATCHES & BUFFERS
LBRDE
RBRDE
SDAT
SDAT
CENBL Ø2
SEL Ø7
CS Ø7
4KX9
4KX9
CENBL Ø6
SEL Ø6
CS Ø6
4KX9
4KX9
CENBL Ø5
SEL Ø5
CS Ø5
4KX9
4KX9
CENBL Ø4
SEL Ø4
CS Ø4
4KX9
4KX9
XENBL
BIIA16+ to BIIA11+
BIIA10+ To BIIA05+
YENBL
CENBL Ø3
SEL Ø3
CS Ø3
4KX9
4KX9
CENBL Ø2
SEL Ø2
CS Ø2
4KX9
4KX9
CENBL Ø1
SEL Ø1
CS Ø1
4KX9
4KX9
CENBL Ø0
SEL Ø0
CS Ø0
4KX9
4KX9
WRITE DRIVERS
WRITE DRIVERS
LBYEN
LEFT 9 BITS
RBYEN
RIGHT 9 BITS
WRITE DATA LATCHES & DRIVERS (LEFT)
WRITE DATA LATCHES & DRIVERS (RIGHT)
LBWDE
RBWDE
DATA BUS
CENBL
REFSH
BIIA Ø2
BIIA Ø3
BIIA Ø4
1 of 8 Decode
SEL Ø7
SEL Ø6
SEL Ø5
SEL Ø4
SEL Ø3
SEL Ø2
SEL Ø1
SEL Ø0
CENBL Ø7
CENBL Ø6
CENBL Ø5
CENBL Ø4
CENBL Ø3
CENBL Ø2
CENBL Ø1
CENBL Ø0

FIG. 4

LTR	DATE	REVISION	DR.	CK.



① ADDRESS designates Backplane Signal

② Cross hatched areas indicate times where signal should not be considered stable.

③ Dashed lines indicate CENBL start for Refresh Cycle

FIG. 5

MATERIAL	DWN	PRIME COMPUTER, INC. FRAMINGHAM, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET OF
	SIZE B	DWG. NO. / REV.

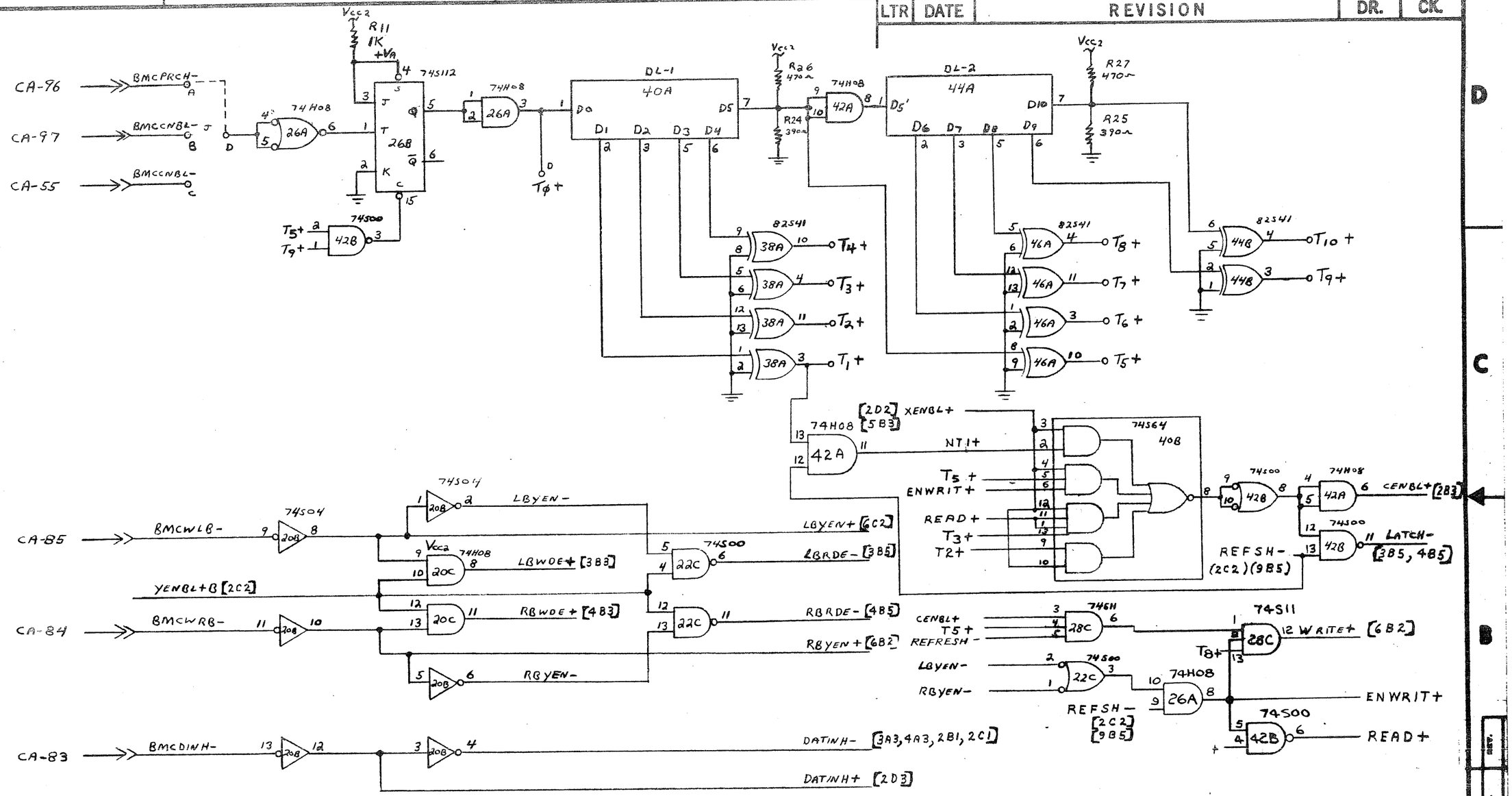
LTR	DATE	REVISION	DR.	CK.

OPTION	1	2	3	4	5	6	7	8	9
32K X18 MOS MEMORY	X	X	X	X	X	X	X	X	X
NCC P400	X	ZA	X	X	X	X	X	X	X

MATERIAL	DWN J.F.TRAVALINI 6-23-76	PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	DIRECTORY 32K MEMORY III-7A	
	APPRD		
	USED ON	SCALE	SIZE B / DWG. NO. LBD1902 / REV.
	NEXT ASSY	SHEET OF	

DWG. NO.

LTR	DATE	REVISION	DR.	CK.



F1											C1
F	1674	R&R	E						D	D	C
E	1655		D	E	C	C	C	B	C	C	B
D	1624		C	D	B	B	B		B	B	
C	1619			C							
B	1580		B	B							
A	REL		A	A	A	A	A	A	A	A	A
LBD REV	ECN	CK	1	2	3	4	5	6	7	8	9

SHEETS

MATERIAL

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES

.XX	.XXX	ANGLES
± .02	± .005	± 1/2°

DWN A.K. 1-11-74
CHK
ENG E. Sheehan 7/14/75
APPRD
USED ON
NEXT ASSY

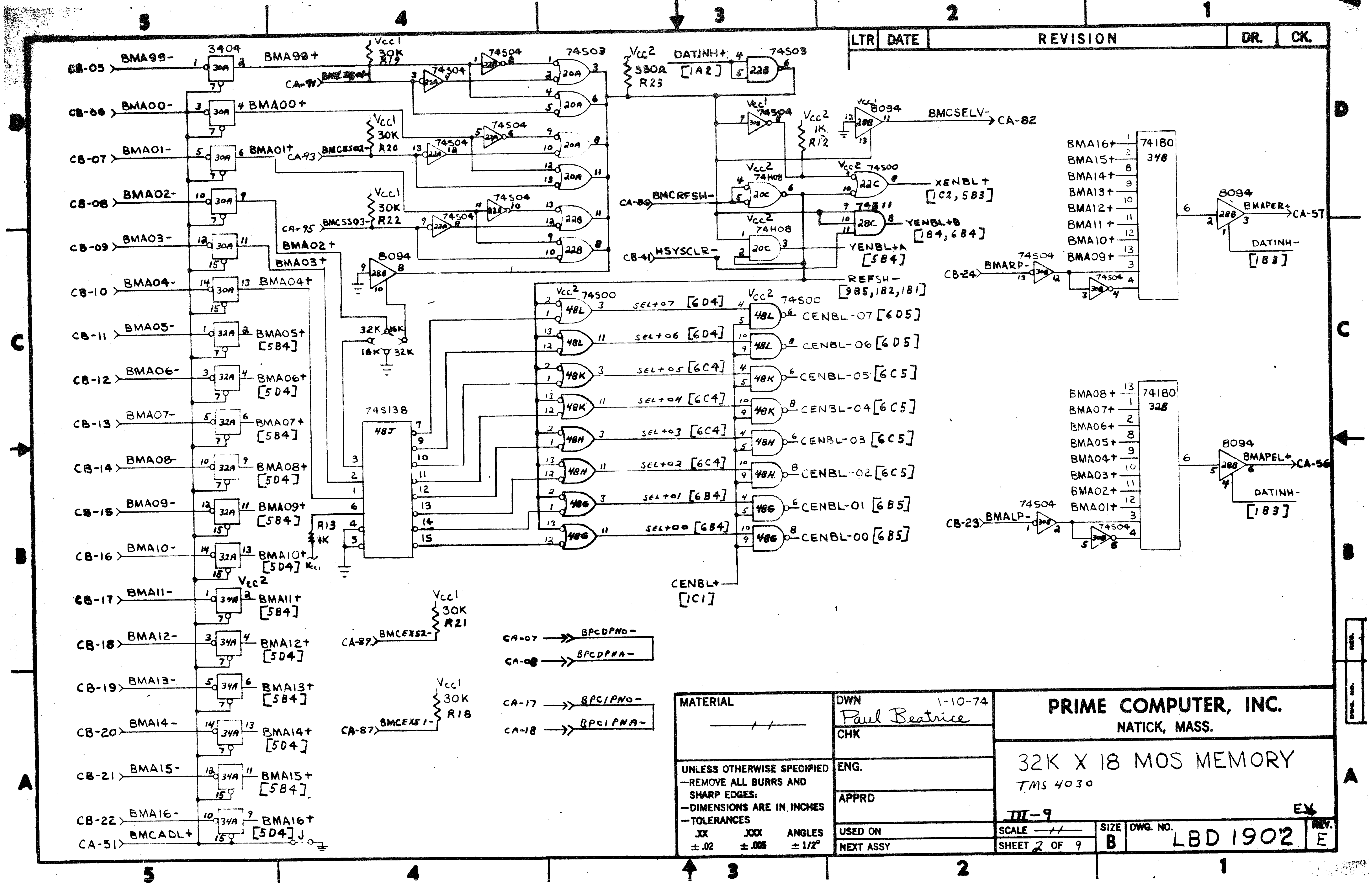
PRIME COMPUTER, INC.
NATICK, MASS.

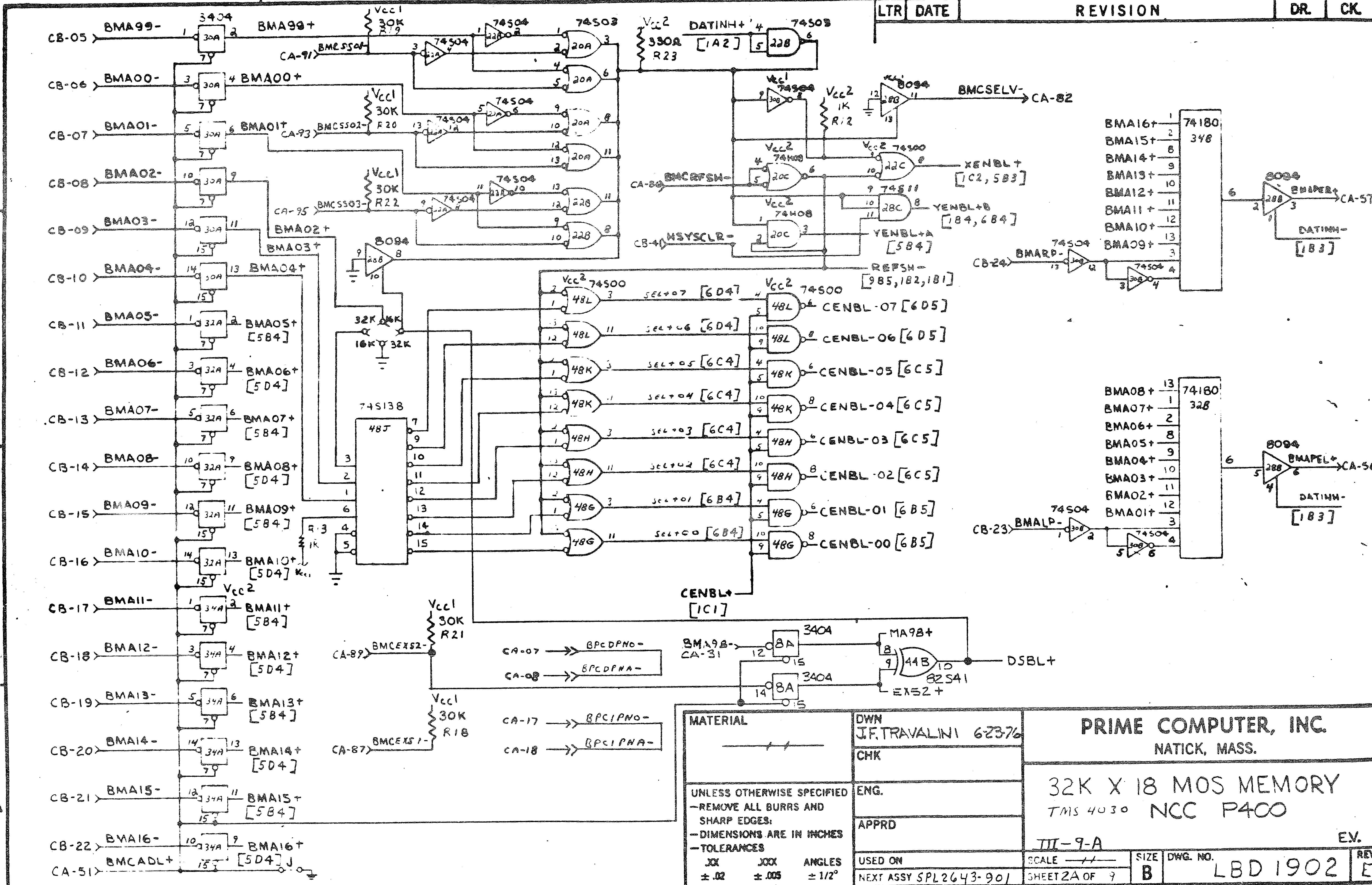
32K X 18 MOS MEMORY
TMS 4030

III-8

ETCH VERSION

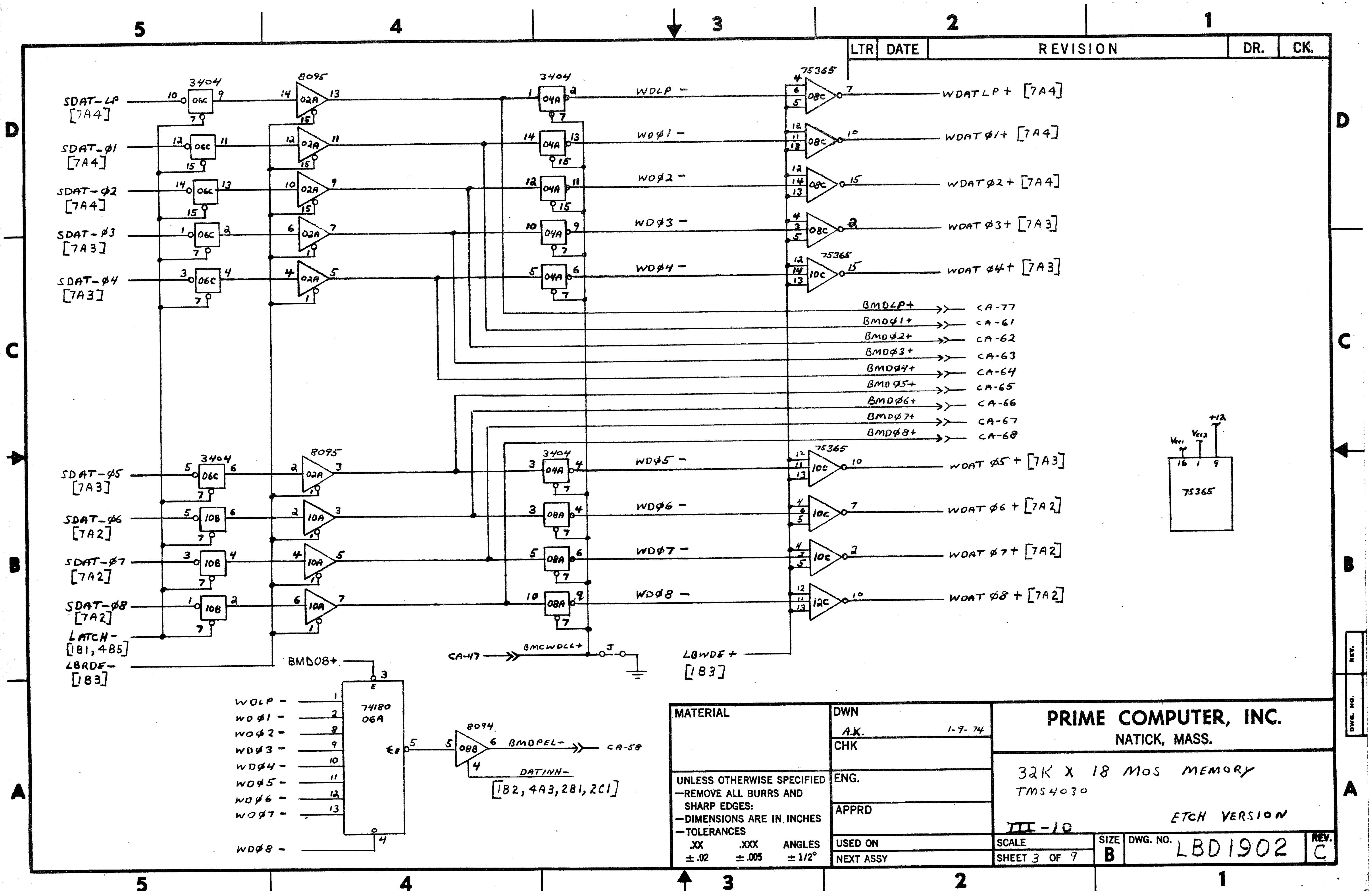
SCALE
SHEET 1 OF 9
SIZE B
DWG. NO. LBD1902
REV. E


LTR
DATE
REVISION
DR.
CK.
MATERIAL
DWN Paul Beatrice 1-10-74
CHK
ENG.
APPRD
USED ON
NEXT ASSY
UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02
.XXX ±.005
ANGLES ±1/2°
PRIME COMPUTER, INC.
NATICK, MASS.
32K X 18 MOS MEMORY
TMS 4030
III-9
SCALE
SHEET 2 OF 9
SIZE B
DWG. NO. LBD 1902
REV. E



LTR | DATE | REVISION | DR. | CK.
CB-05 BMA99- 3404 30A BMA99+
CB-06 BMA00- 30A BMA00+
CB-07 BMA01- 30A BMA01+
CB-08 BMA02- 30A
CB-09 BMA03- 30A
CB-10 BMA04- 30A BMA04+
CB-11 BMA05- 32A BMA05+ [5B4]
CB-12 BMA06- 32A BMA06+ [5D4]
CB-13 BMA07- 32A BMA07+ [5B4]
CB-14 BMA08- 32A BMA08+ [5D4]
CB-15 BMA09- 32A BMA09+ [5B4]
CB-16 BMA10- 32A BMA10+ [5D4]
CB-17 BMA11- 34A BMA11+ [5B4]
CB-18 BMA12- 34A BMA12+ [5D4]
CB-19 BMA13- 34A BMA13+ [5B4]
CB-20 BMA14- 34A BMA14+ [5D4]
CB-21 BMA15- 34A BMA15+ [5B4]
CB-22 BMA16- 34A BMA16+ [5D4]
CA-51 BMCADL+
CA-91 BMCSS01
CA-93 BMCSS02
CA-95 BMCSS03
Vcc1 30K R19
Vcc1 30K R20
Vcc1 30K R22
74S04 74S03
Vcc2 330Ω R23
DATINH+ [1A2] 74S03 22B
BMA02+ BMA03+
8094 28B
BMCSELV- CA-82
Vcc2 1K R12
CA-86 BMCRFSH-
74H08 20C
74S00 22C XENBL+ [1C2, 5B3]
74S11 28C YENBL+B [1B4, 6B4]
CB-40 HSYSCLR-
YENBL+A [5B4]
REFSH- [9B5, 1B2, 1B1]
32K 16K 16K 32K
74S138 48J
R-3 1K
Vcc2 74S00
SEL+07 [6D4] CENBL-07 [6D5]
SEL+06 [6D4] CENBL-06 [6D5]
SEL+05 [6C4] CENBL-05 [6C5]
SEL+04 [6C4] CENBL-04 [6C5]
SEL+03 [6C4] CENBL-03 [6C5]
SEL+02 [6C4] CENBL-02 [6C5]
SEL+01 [6B4] CENBL-01 [6B5]
SEL+00 [6B4] CENBL-00 [6B5]
48L 48K 48H 48G
CENBL+ [1C1]
BMA16+ BMA15+ BMA14+ BMA13+ BMA12+ BMA11+ BMA10+ BMA09+
74180 34B
8094 28B BMAPER+ CA-57
DATINH- [1B3]
CB-24 BMARP- 74S04
BMA08+ BMA07+ BMA06+ BMA05+ BMA04+ BMA03+ BMA02+ BMA01+
74180 32B
8094 28B BMAPEL+ CA-56
DATINH- [1B3]
CB-23 BMALP- 74S04
CA-89 BMCEXS2- Vcc1 30K R21
CA-87 BMCEXS1- Vcc1 30K R18
CA-07 BPCDPNO-
CA-08 BPCDPNA-
CA-17 BPC1PNO-
CA-18 BPC1PNA-
BMA98- CA-31 3404 8A
MA98+ 44B 82S41 DSBL+
EX52+

MATERIAL	DWN J.F. TRAVALINI 6-23-76	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES: — DIMENSIONS ARE IN INCHES — TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	32K X 18 MOS MEMORY TMS 4030 NCC P400
	APPRD	III-9-A E.V.
	USED ON	SCALE — SIZE B DWG. NO. LBD 1902 REV. E
	NEXT ASSY SPL2643-901	SHEET 2A OF 9



MATERIAL	DWN A.K. 1-9-74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	32K X 18 MOS MEMORY TMS4030
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	III-10 ETCH VERSION
	APPRD	
	USED ON	SCALE · SIZE B · DWG. NO. LBD1902 · REV. C
	NEXT ASSY	SHEET 3 OF 9

LTR	DATE	REVISION	DR.	CK.

SDAT-Ø9 [8A4]
SDAT-1Ø [8A4]
SDAT-11 [8A3]
SDAT-12 [8A3]
SDAT-13 [8A3]
SDAT-14 [8A3]
SDAT-15 [8A2]
SDAT-16 [8A2]
SDAT-RP [8A2]
LATCH- [1B1, 3B5]
RBRDE- [1B2]

3404 10B, 14B
8095 12B, 16B
3404 12A, 16A

WDØ9 -
WD1Ø -
WD11 -
WD12 -
WD13 -
WD14 -
WD15 -
WD16 -
WDRP -

75365 12C, 14C, 16C

WDAT Ø9 + [8A4]
WDAT 1Ø + [8A4]
WDAT 11 + [8A3]
WDAT 12 + [8A3]
WDAT 13 + [8A3]
WDAT 14 + [8A3]
WDAT 15 + [8A2]
WDAT 16 + [8A2]
WDAT RP + [8A2]

BMDØ9 + → CA-69
BMD1Ø + → CA-7Ø
BMD11 + → CA-71
BMD12 + → CA-72
BMD13 + → CA-73
BMD14 + → CA-74
BMD15 + → CA-75
BMD16 + → CA-76
BMDRP + → CA-78

CA-43 → BMCWDLR + → J

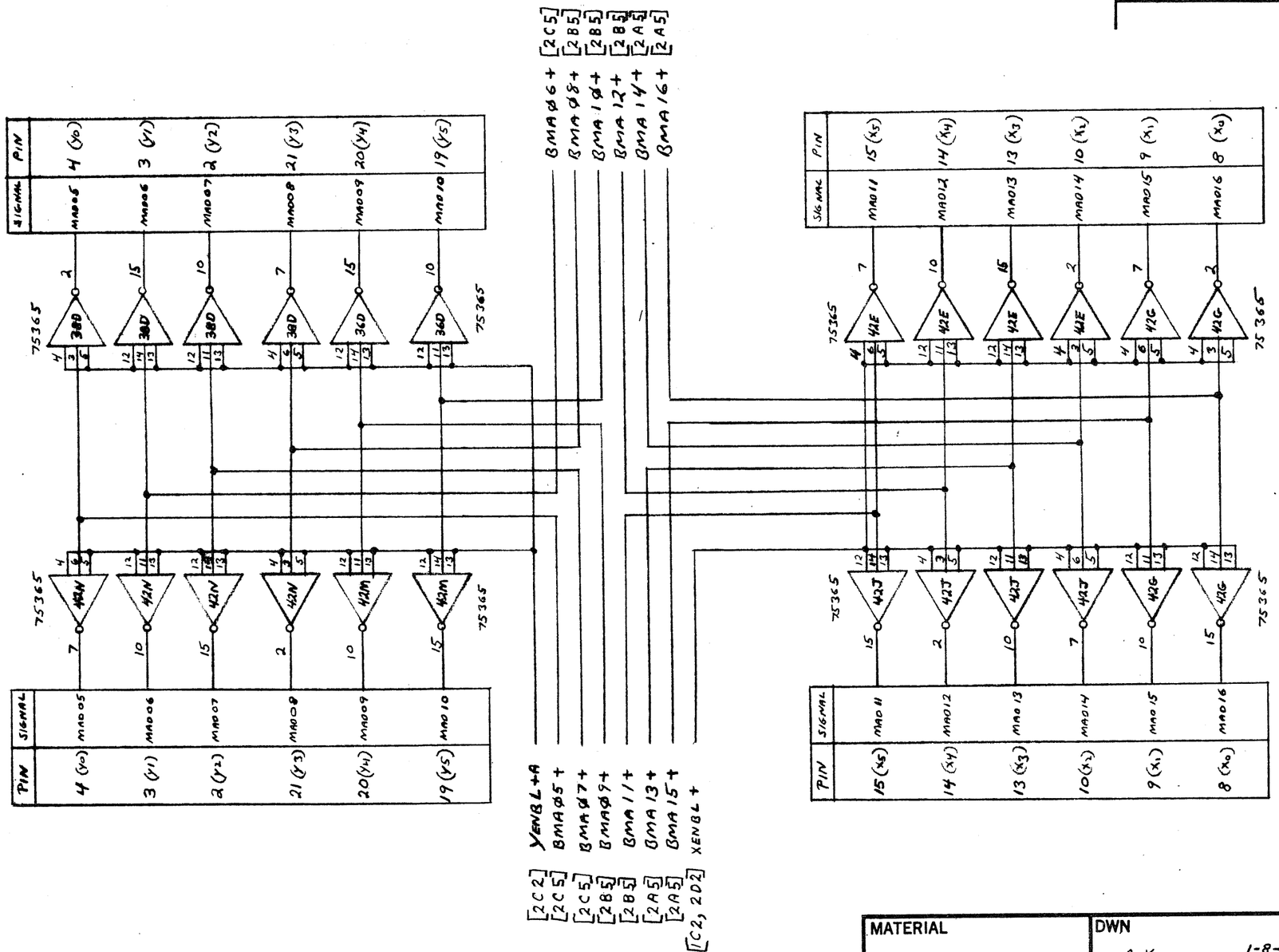
RBWDE + [1B3]

+12, V_{cc1}, V_{cc2}, 16, 1, 9 — 75365

BMDRP + → 74180 14A pin 3
WDØ9 - pin 1
WD1Ø - pin 2
WD11 - pin 8
WD12 - pin 9
WD13 - pin 10
WD14 - pin 11
WD15 - pin 12
WD16 - pin 13
WDRP - pin 4
74180 14A pin 5 → 8094 08B pin 9
8094 08B pin 8 → BMDPER- → CA-59
8094 08B pin 10 → DATINH- [1B1, 2B1, 2C1, 3A3]

MATERIAL	DWN AK 1-Y-74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK	32K X 18 MOS MEMORY TMS 4030	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	III-11 ETCH VERSION	
	APPRD		
	USED ON	SCALE	SIZE B / DWG. NO. LBD1902 / REV. C
	NEXT ASSY	SHEET 4 OF 9	

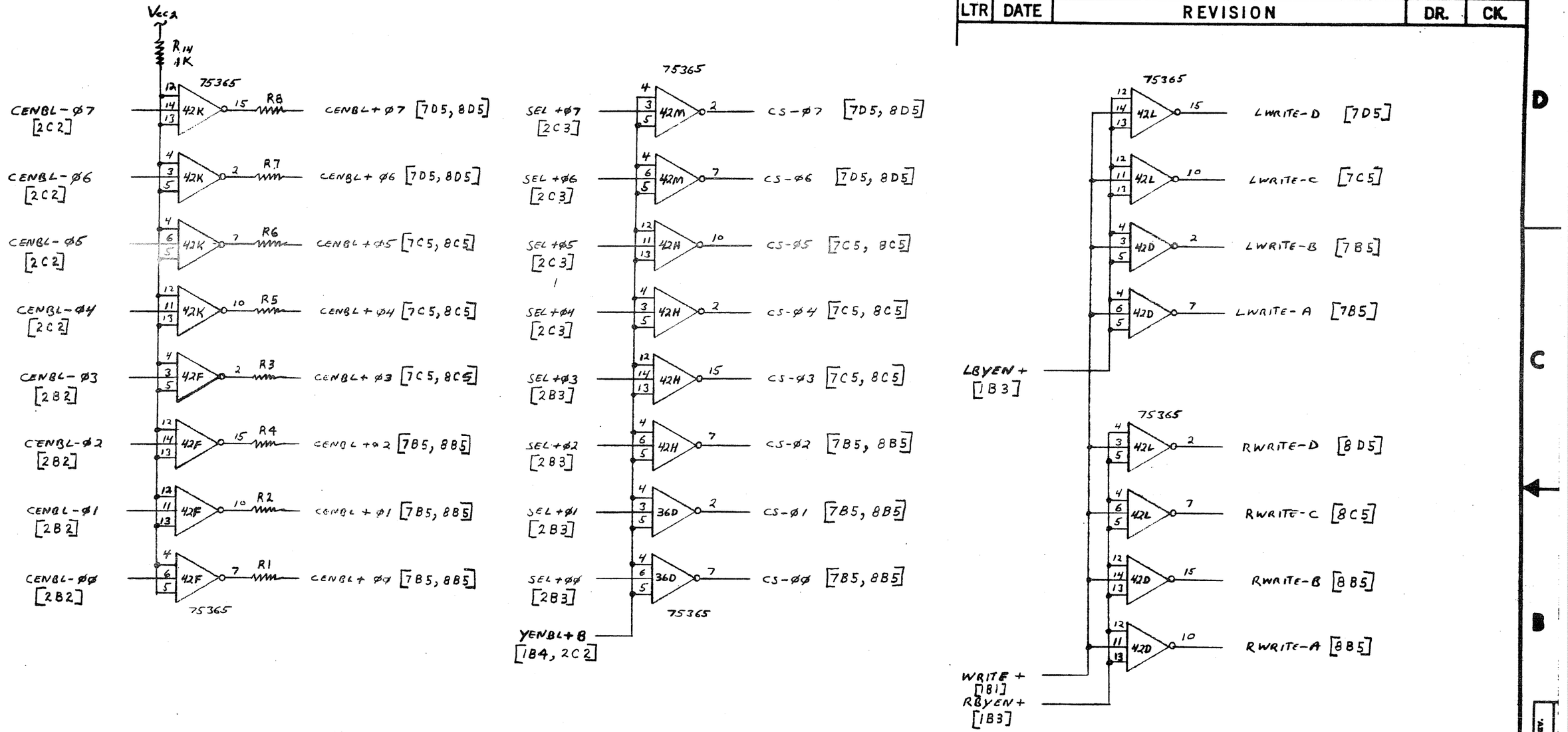
LTR	DATE	REVISION	DR.	CK.

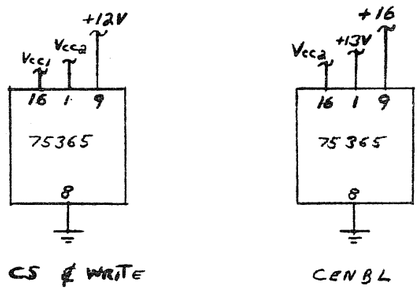


MATERIAL	DWN A K 1-8-74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	32K X 18 MOS MEMORY TMS 4030 ETCH VERSION III-12	
	ENG.		
	APPRD		
	USED ON	SCALE	SIZE B
	NEXT ASSY	SHEET 5 OF 9	DWG. NO. LBD 1902 REV. C

REV. | DWG. NO.

LTR	DATE	REVISION	DR.	CK.



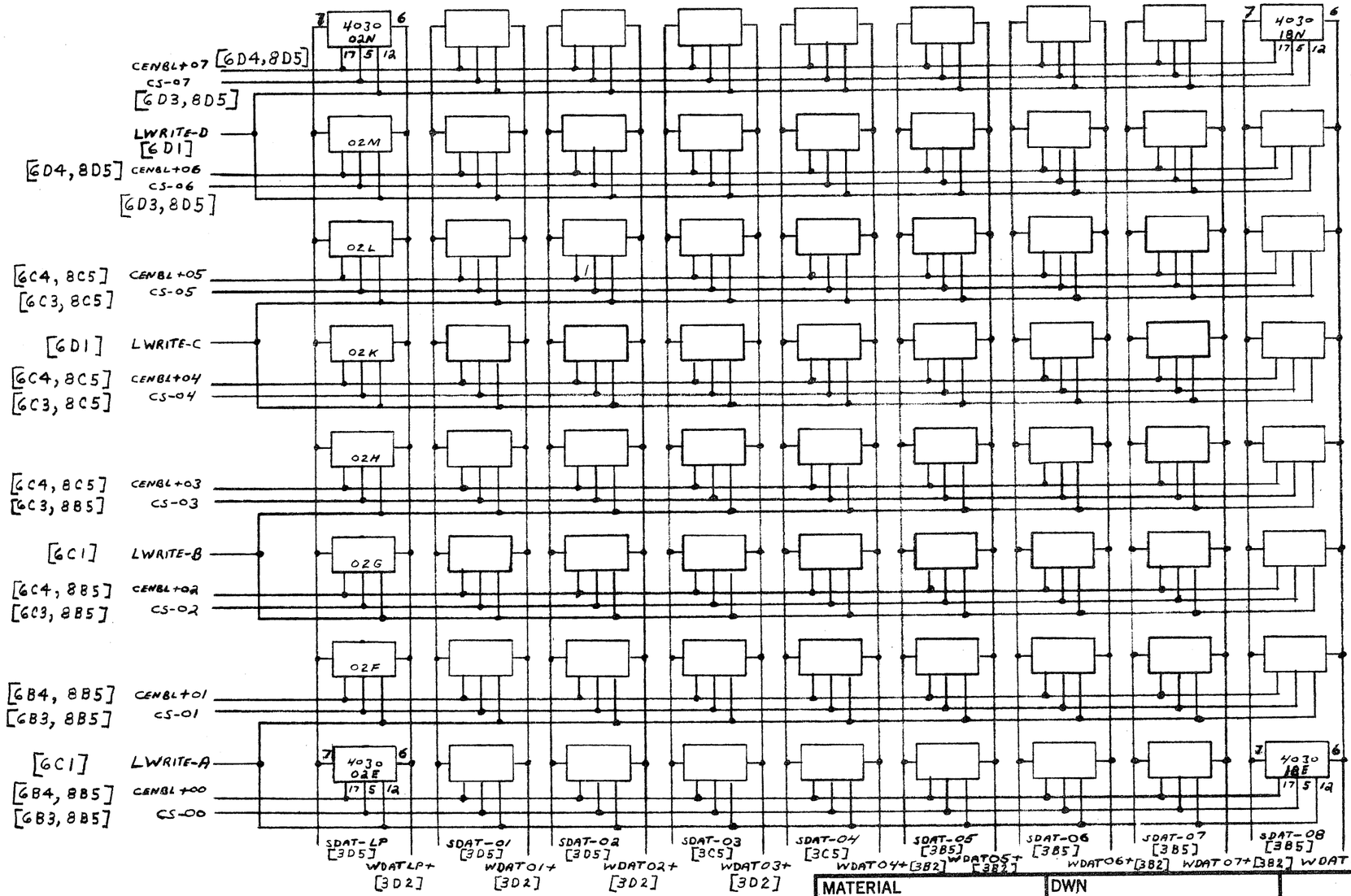


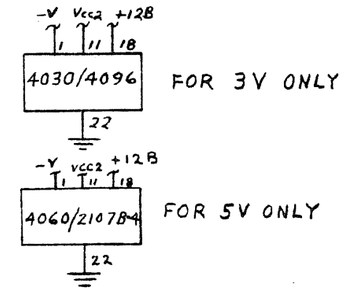
MATERIAL	DWN A.K. 1-8-74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	32K X18 MOS MEMORY TMS 4030
	ENG.	
	APPRD	III-13 ETCH VERSION
USED ON	SCALE	SIZE B DWG. NO. LBD1902 B
NEXT ASSY	SHEET 6 OF 9	

REV.

DWG. NO.

LTR	DATE	REVISION	DR.	CK.

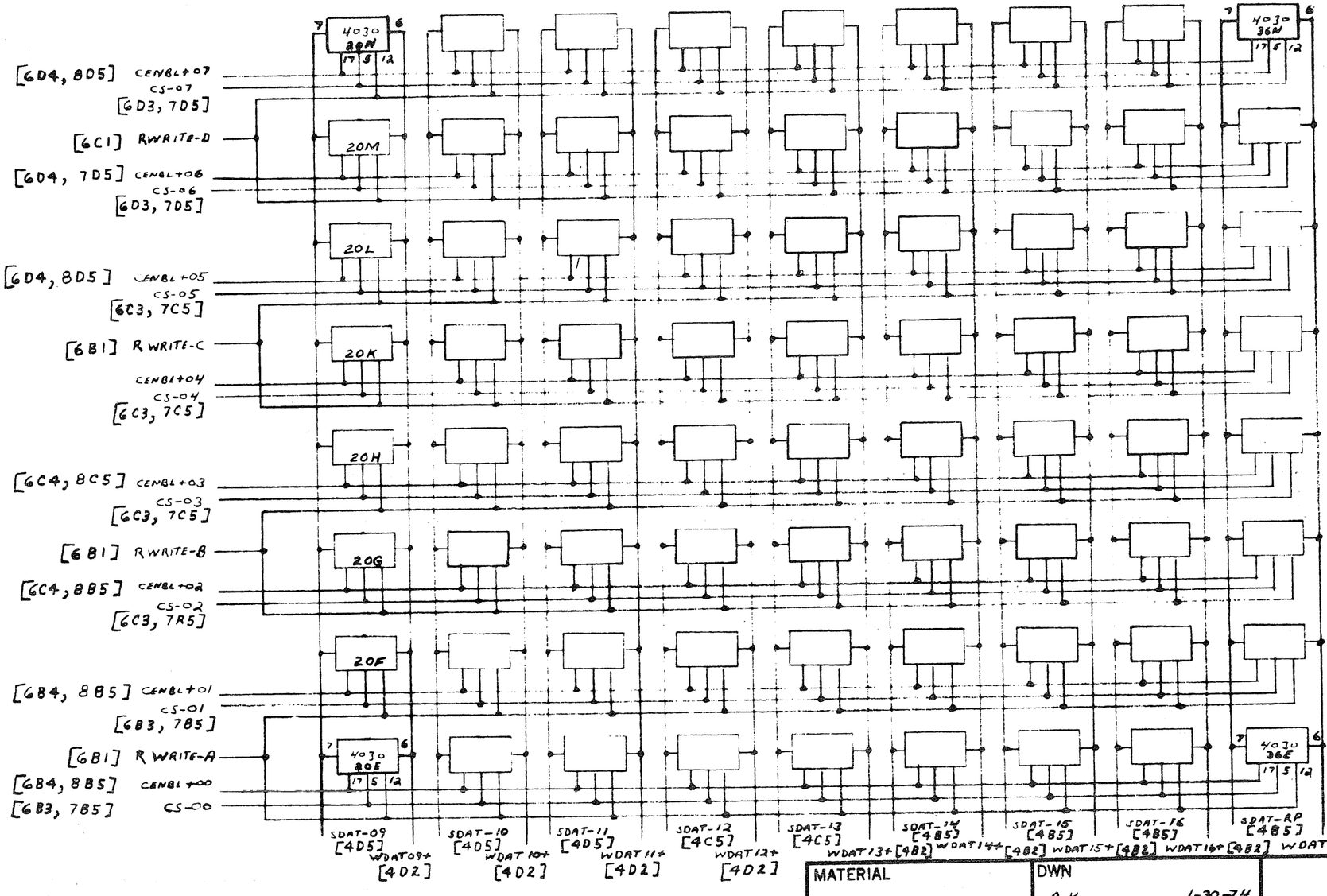




MATERIAL	DWN A.K. 1-30-74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	32K X 18 MOS MEMORY TMS 4030
	ENG.	III-14 ETCH VERSION
	APPRD	
	USED ON	SCALE NONE SIZE B DWG. NO. LBD1902 REV. D
	NEXT ASSY	SHEET 7 OF 9

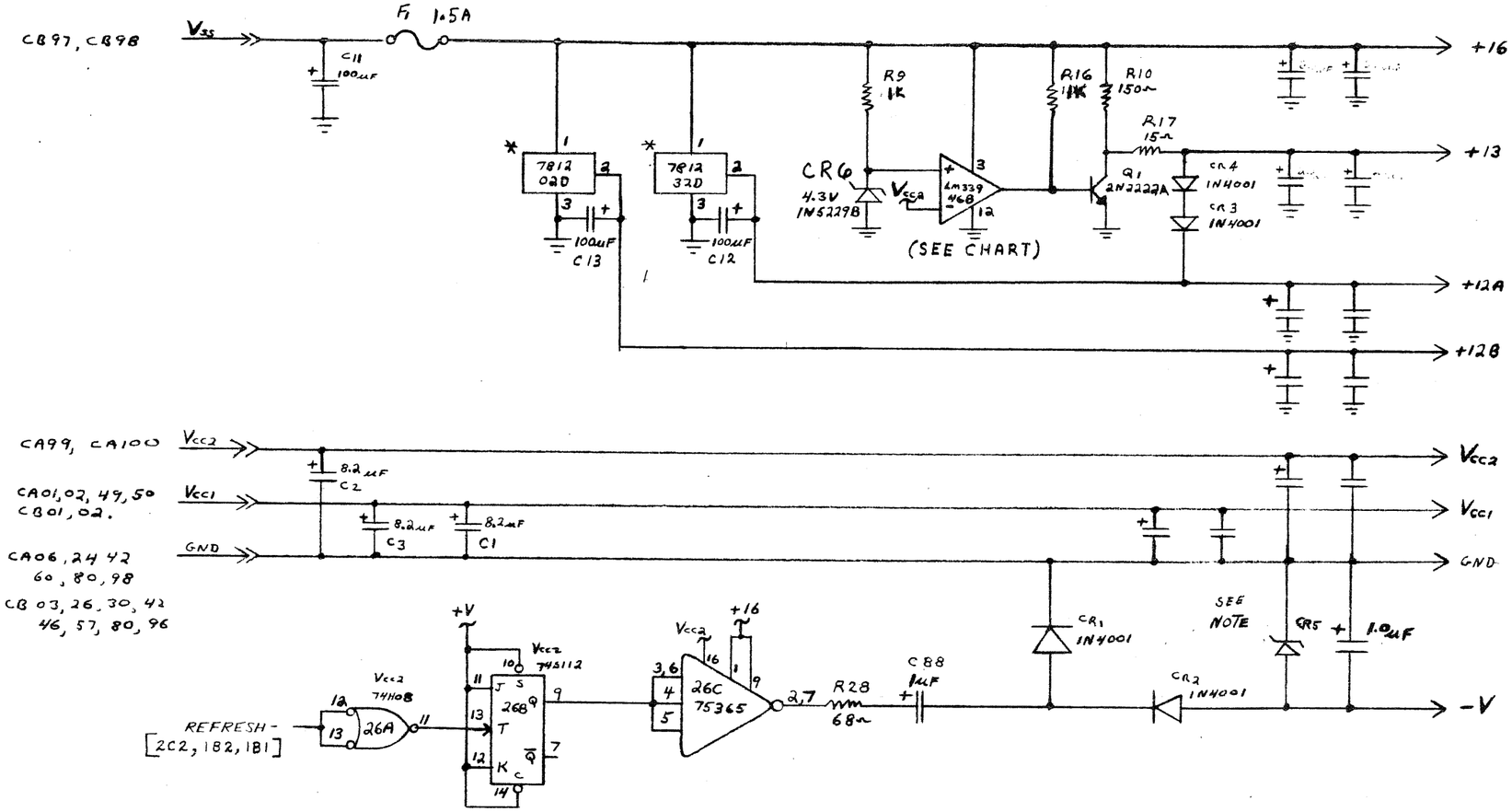
REV. DWG. NO.

LTR	DATE	REVISION	DR.	CK.



MATERIAL	DWN A.K. 1-30-74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	32K X 18 MOS MEMORY TMS 4030
	ENG.	III-15 ETCH VERSION
	APPRD	
	USED ON	SCALE NONE
	NEXT ASSY	SIZE B DWG. NO. LBD 1902 REV. D
		SHEET 8 OF 9

LTR	DATE	REVISION	DR.	CK.



NOTE:—

IN5225B (CR5) 3.0V ±5% WITH 4K CHIP (ICD1532)

IN5231B (CR5) 5.1V ±5% WITH 4K CHIP (ICD 2307)

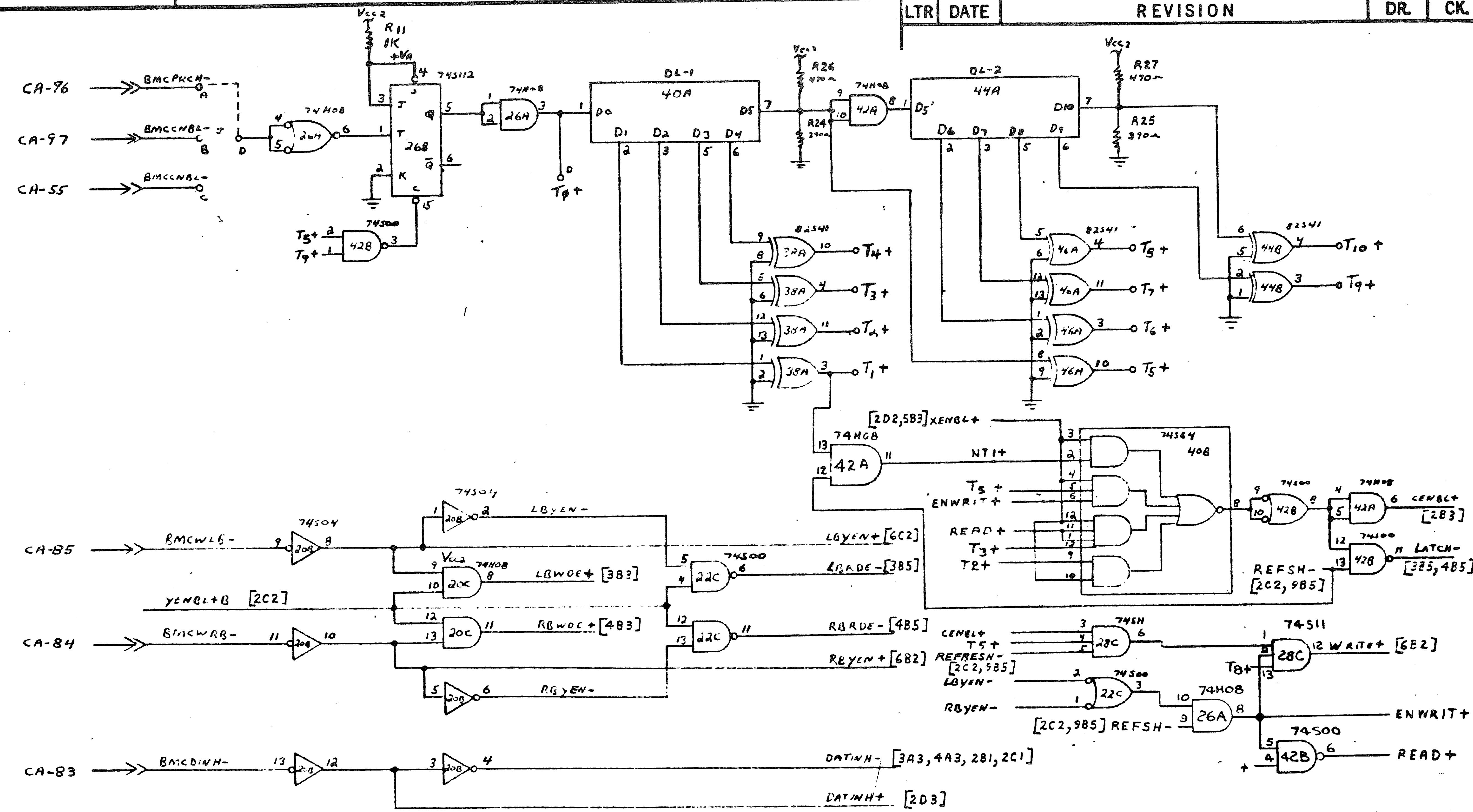
* MOUNTED ON HEAT SINK

CAPACITORS WITH NO VALUE DESIGNATION ARE CAP. TANT 1.0μF, 20V

LM339 COMMON	PINS
+ INPUT	5 7 9 11
− INPUT	4 6 8 10
OUTPUT	2 1 14 13

MATERIAL	DWN A.K. 1-30-74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	32K X 18 MOS MEMORY TMS 4030 III - 16 ETCH VERSION
	APPRD	
	USED ON	SCALE — SIZE B DWG. NO. LBD 1902 REV. C1
	NEXT ASSY	SHEET 9 OF 9

REV. DWG. NO.



LTR	DATE	REVISION	DR.	CK.

LBD REV	ECN	CK	1	2	3	4	5	6	7	8	9
C1											C1
C	1674	F2K	C						C	C	C
B	1655		B	B	B	B	B	B	B	B	B
A	REL		A	A	A	A	A	A	A	A	A
			SHEETS								

MATERIAL

UNLESS OTHERWISE SPECIFIED
- REMOVE ALL BURRS AND SHARP EDGES:
- DIMENSIONS ARE IN INCHES
- TOLERANCES

.XX	.XXX	ANGLES
± .02	± .005	± 1/2°

DWN A.K. 1-11-74
CHK
ENG. [illegible] 7/1/75
APPRD
USED ON
NEXT ASSY

PRIME COMPUTER, INC.
NATICK, MASS.

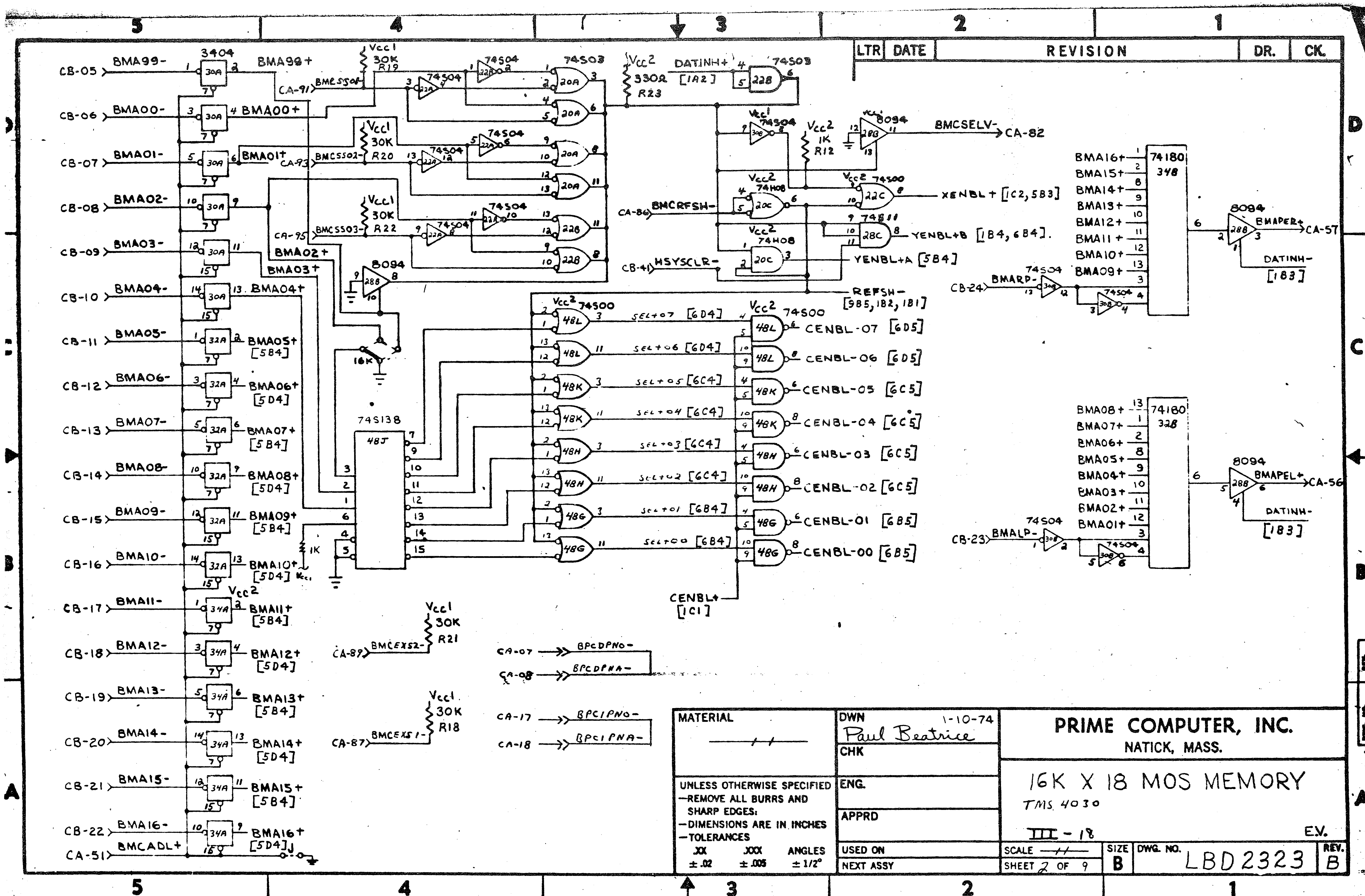
16K x 18 MOS MEMORY
TMS 4030

III-17

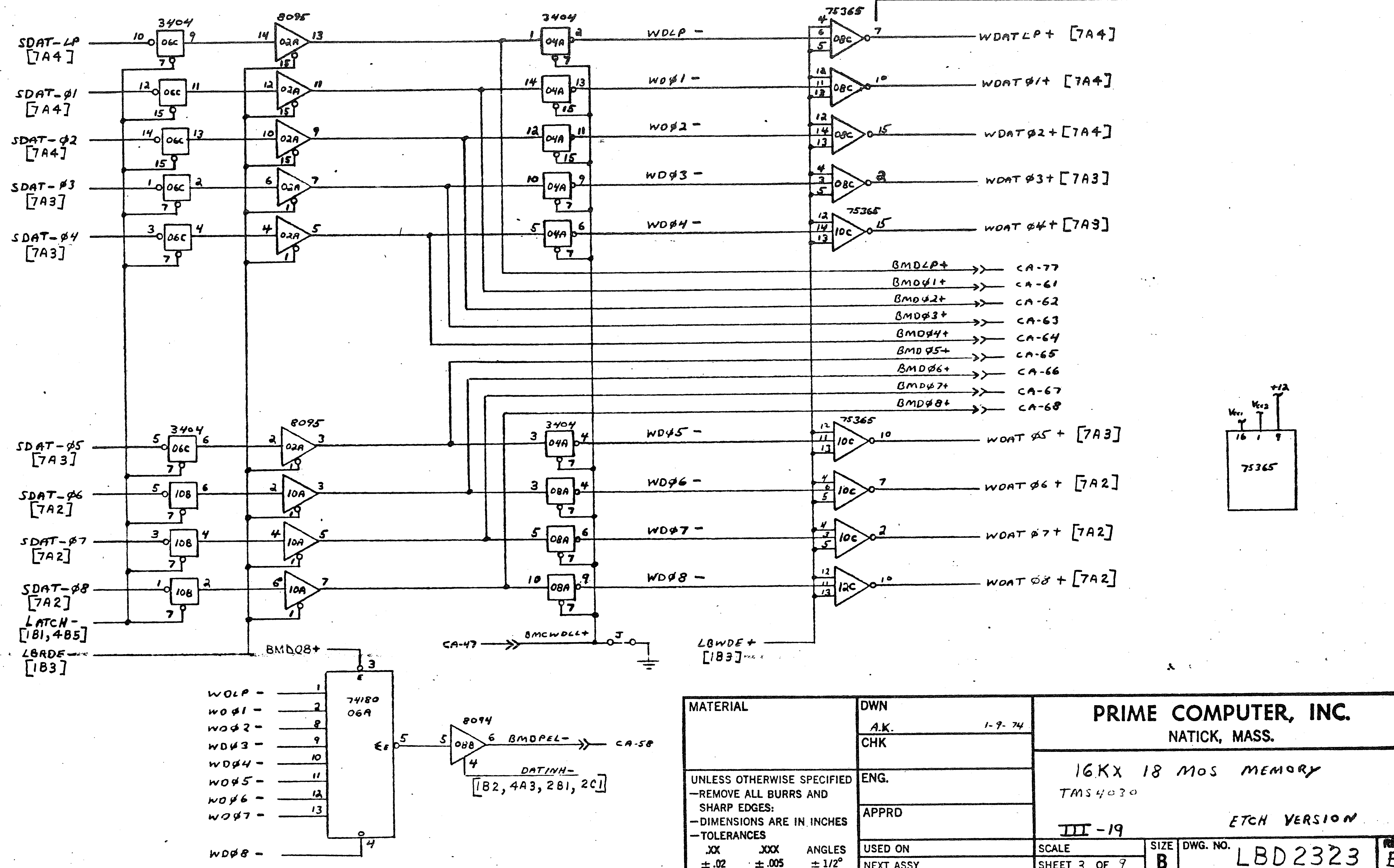
ETCH VERSION

SCALE
SHEET 1 OF 9

SIZE B | DWG. NO. LBD 2323 | REV. C



REVISION
LTR DATE DR. CK.
CB-05 BMA99- 3404 30A BMA99+
CB-06 BMA00- 30A BMA00+
CB-07 BMA01- 30A BMA01+
CB-08 BMA02- 30A
CB-09 BMA03- 30A
CB-10 BMA04- 30A BMA04+
CB-11 BMA05- 32A BMA05+ [5B4]
CB-12 BMA06- 32A BMA06+ [5D4]
CB-13 BMA07- 32A BMA07+ [5B4]
CB-14 BMA08- 32A BMA08+ [5D4]
CB-15 BMA09- 32A BMA09+ [5B4]
CB-16 BMA10- 32A BMA10+ [5D4]
CB-17 BMA11- 34A BMA11+ [5B4]
CB-18 BMA12- 34A BMA12+ [5D4]
CB-19 BMA13- 34A BMA13+ [5B4]
CB-20 BMA14- 34A BMA14+ [5D4]
CB-21 BMA15- 34A BMA15+ [5B4]
CB-22 BMA16- 34A BMA16+ [5D4]
CA-51 BMCADL+
CA-91 BMCSS01- Vcc1 30K R19
CA-93 BMCSS02- Vcc1 30K R20
CA-95 BMCSS03- Vcc1 30K R22
74S04 74S03 74S00 74H08 74S11 8094 74S138 74180
BMA02+ BMA03+
16K 1K
Vcc2 330Ω R23 DATINH+ [1A2]
BMCSELV- CA-82
Vcc2 1K R12
CA-86 BMCRFSH-
XENBL+ [1C2,5B3]
YENBL+B [1B4,6B4]
CB-41 HSYSCLR- YENBL+A [5B4]
REFSH- [9B5,1B2,1B1]
SEL+07 [6D4] CENBL-07 [6D5]
SEL+06 [6D4] CENBL-06 [6D5]
SEL+05 [6C4] CENBL-05 [6C5]
SEL+04 [6C4] CENBL-04 [6C5]
SEL+03 [6C4] CENBL-03 [6C5]
SEL+02 [6C4] CENBL-02 [6C5]
SEL+01 [6B4] CENBL-01 [6B5]
SEL+00 [6B4] CENBL-00 [6B5]
CENBL+ [1C1]
BMA16+ BMA15+ BMA14+ BMA13+ BMA12+ BMA11+ BMA10+ BMA09+ 74180 34B
CB-24 BMARP-
BMAPER+ CA-57 DATINH- [1B3]
BMA08+ BMA07+ BMA06+ BMA05+ BMA04+ BMA03+ BMA02+ BMA01+ 74180 32B
CB-23 BMALP-
BMAPEL+ CA-56 DATINH- [1B3]
CA-89 BMCEXS2- Vcc1 30K R21
CA-87 BMCEXS1- Vcc1 30K R18
CA-07 BPCDPNO-
CA-08 BPCDPNA-
CA-17 BPCIPNO-
CA-18 BPCIPNA-
MATERIAL
UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02 .XXX ±.005 ANGLES ±1/2°
DWN Paul Beatrice 1-10-74
CHK
ENG.
APPRD
USED ON
NEXT ASSY
PRIME COMPUTER, INC.
NATICK, MASS.
16K X 18 MOS MEMORY
TMS 4030
III - 18
E.V.
SCALE
SHEET 2 OF 9
SIZE B
DWG. NO. LBD2323
REV. B



LTR	DATE	REVISION	DR.	CK.

MATERIAL

DWN A.K. 1-9-74
CHK
ENG.
APPRD

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES

.XX	.XXX	ANGLES
± .02	± .005	± 1/2°

USED ON
NEXT ASSY

PRIME COMPUTER, INC.
NATICK, MASS.

16KX 18 MOS MEMORY
TMS 4030
III - 19
ETCH VERSION

SCALE
SHEET 3 OF 9
SIZE B
DWG. NO. LBD2323
REV. B

LTR	DATE	REVISION	DR.	CK.

SDAT-Ø9 [8A4]
SDAT-1Ø [8A4]
SDAT-11 [8A3]
SDAT-12 [8A3]
SDAT-13 [8A3]
SDAT-14 [8A3]
SDAT-15 [8A2]
SDAT-16 [8A2]
SDAT-RP [8A2]
LATCH- [1B1, 3B5]
RBRDE- [1B2]

WDØ9 -
WD1Ø -
WD11 -
WD12 -
WD13 -
WD14 -
WD15 -
WD16 -
WDRP -

WDAT Ø9 + [8A4]
WDAT 1Ø + [8A4]
WDAT 11 + [8A3]
WDAT 12 + [8A3]
WDAT 13 + [8A3]
WDAT 14 + [8A3]
WDAT 15 + [8A2]
WDAT 16 + [8A2]
WDAT RP + [8A2]

BMDØ9 + → CA-69
BMD1Ø + → CA-7Ø
BMD11 + → CA-71
BMD12 + → CA-72
BMD13 + → CA-73
BMD14 + → CA-74
BMD15 + → CA-75
BMD16 + → CA-76
BMDRP + → CA-78

CA-43 → BMCWDLR+

RBWDE+ [1B3]

BMDRP+

WDØ9 -
WD1Ø -
WD11 -
WD12 -
WD13 -
WD14 -
WD15 -
WD16 -
WDRP -

14180 14A

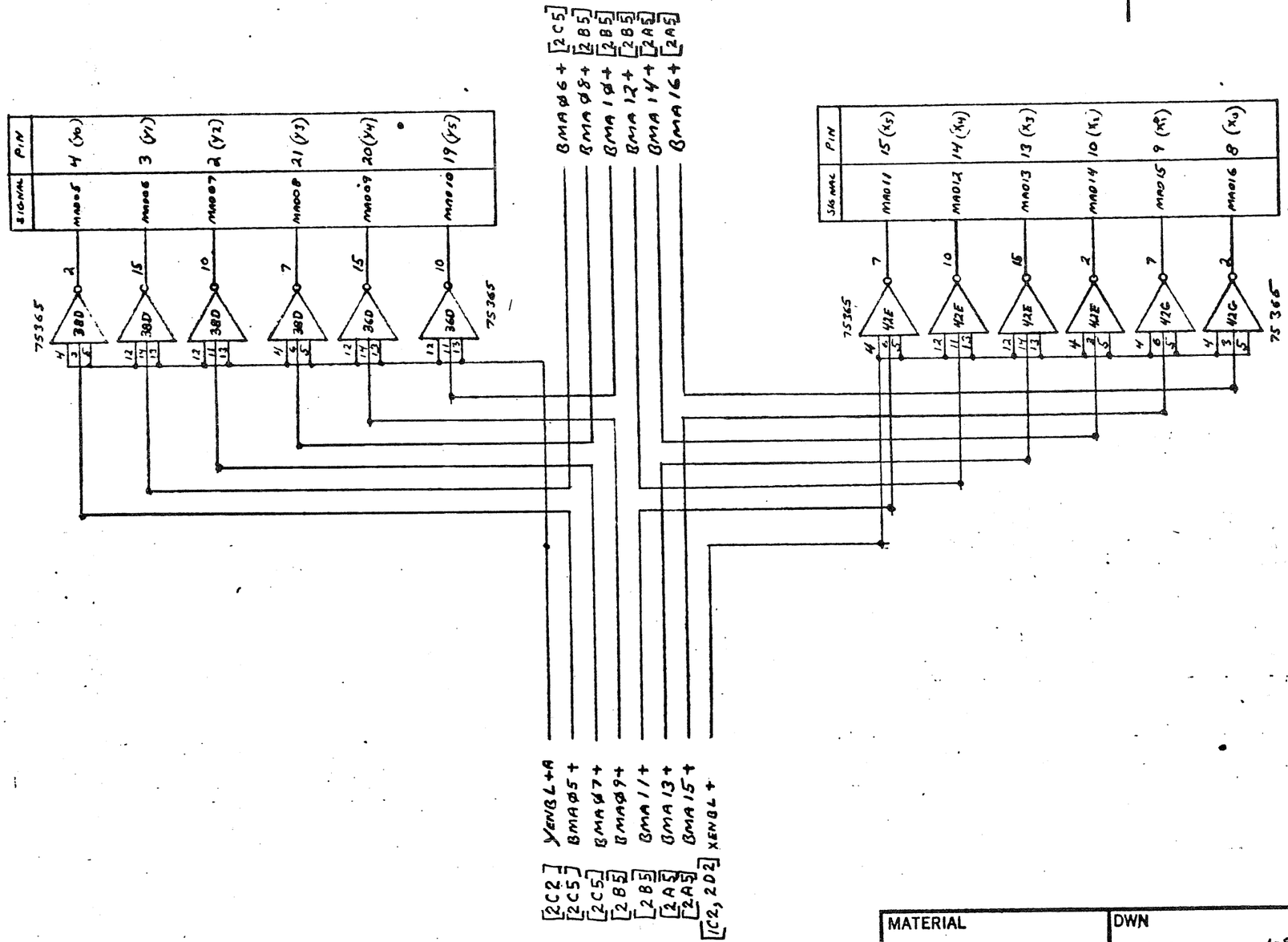
8094 08B → BMDPER- → CA-59

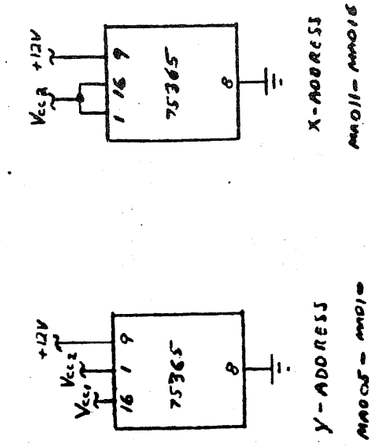
DATINH- [1B1, 2B1, 2C1, 3A3]

+12 Vcc1 Vcc2 16 1 9 75365

MATERIAL	DWN AK 1-7-76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	16KX 18 MOS MEMORY TMS4030 III-20 ETCH VERSION	
	APPRD		
	USED ON	SCALE	SIZE B
	NEXT ASSY	SHEET 4 OF 9	DWG. NO. LBD2323 REV. B

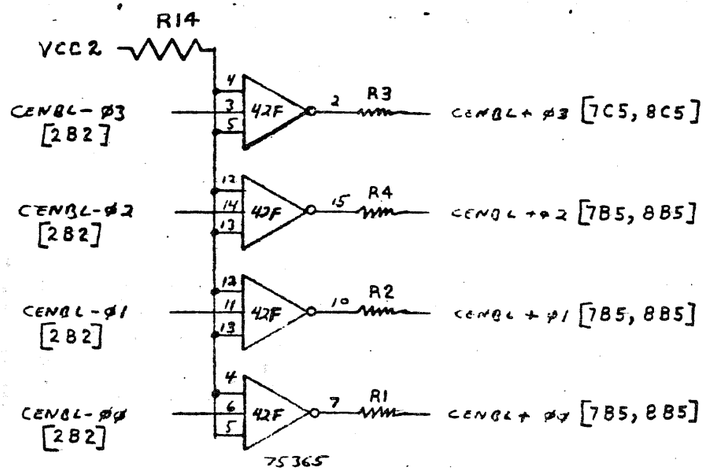
LTR	DATE	REVISION	DR.	CK.

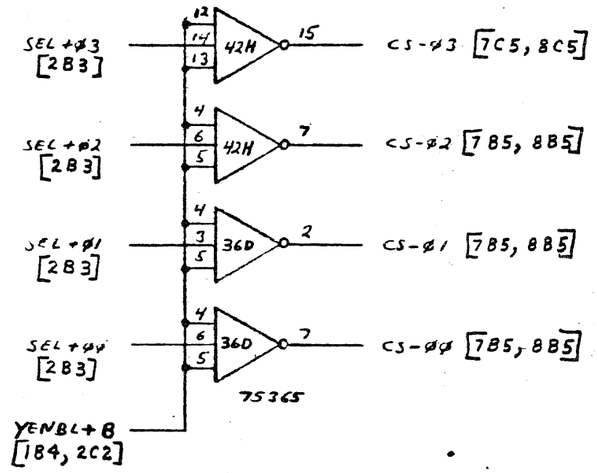


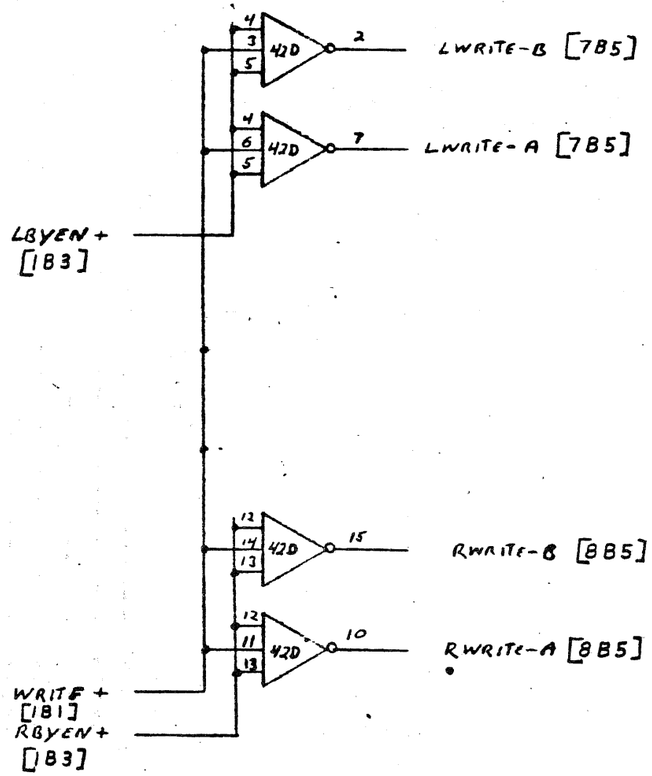


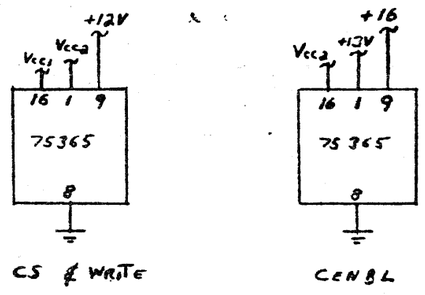
MATERIAL	DWN A K 1-8-74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK	16Kx 18 MOS MEMORY TMS 4030 ETCH VERSION III-21	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.		
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 5 OF 9	SIZE D / DWG. NO. LBD2323 / REV. B

LTR	DATE	REVISION	DR.	CK.



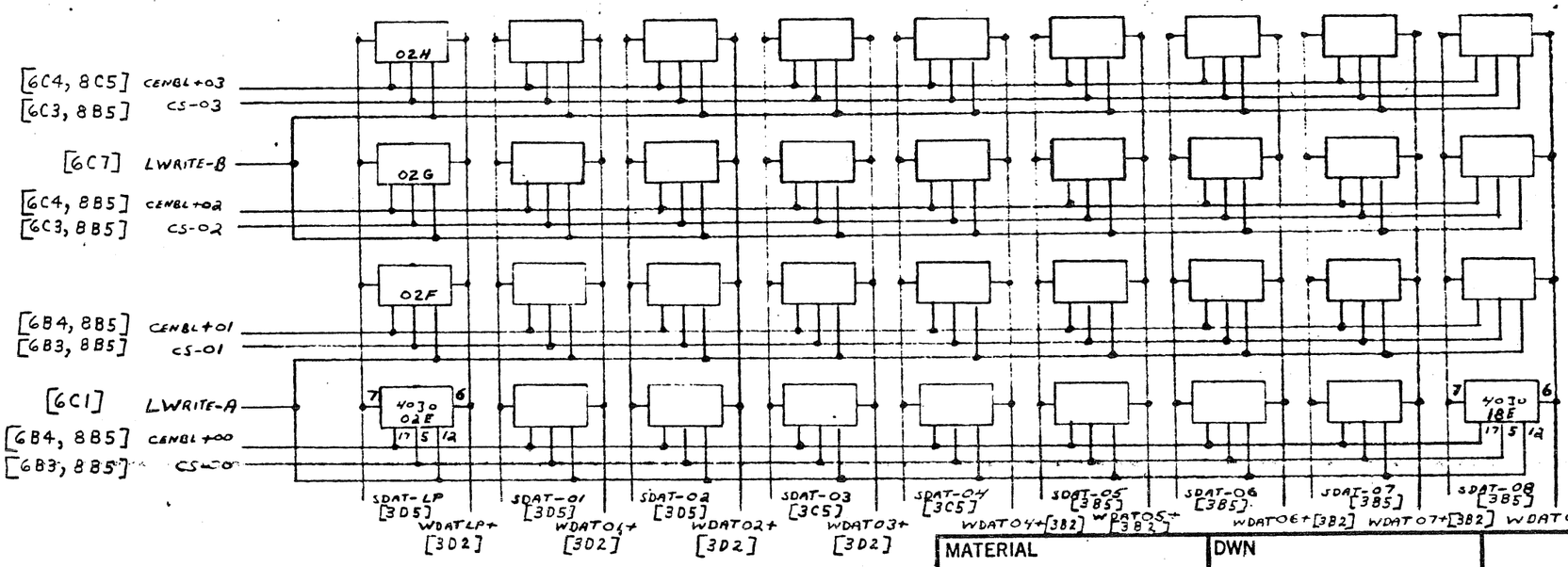


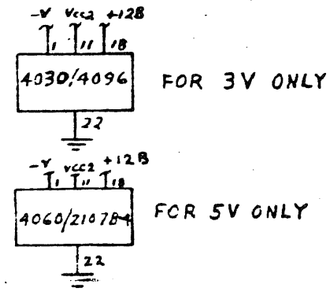




MATERIAL	DWN A.K. 1-8-74	PRIME COMPUTER, INC. NATICK, MASS.		
	CHK			
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	16KX18 MOS MEMORY TMS 4030		
	APPRD	III-22	ETCH VERSION	
	USED ON	SCALE	SIZE B	DWG. NO. LBD2323 REV. B
	NEXT ASSY	SHEET 6 OF 9		

LTR	DATE	REVISION	DR.	CK.

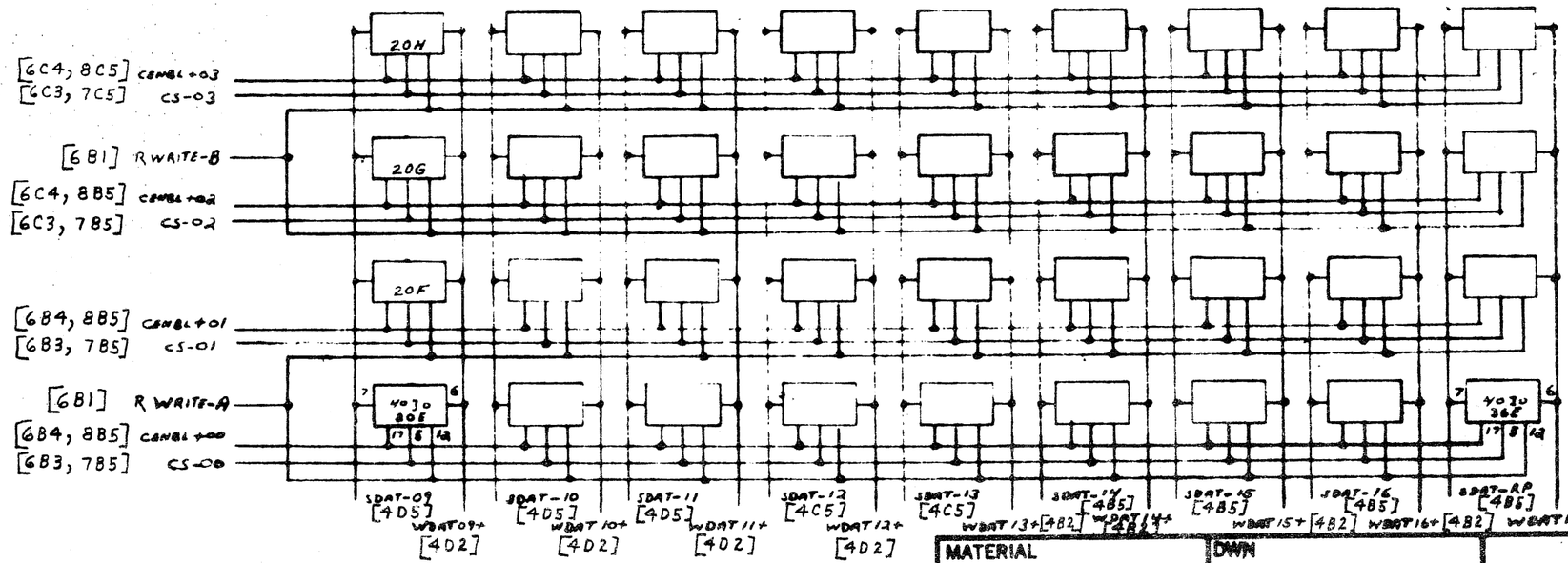


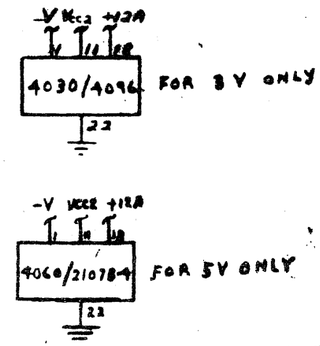


MATERIAL	DWN A.K. 1-30-74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	16K X 18 MOS MEMORY TMS 4030 III-23 ETCH VERSION
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE NONE / SHEET 7 OF 9
		SIZE B / DWG. NO. LBD2323 / REV. C

REV. | DWG. NO.

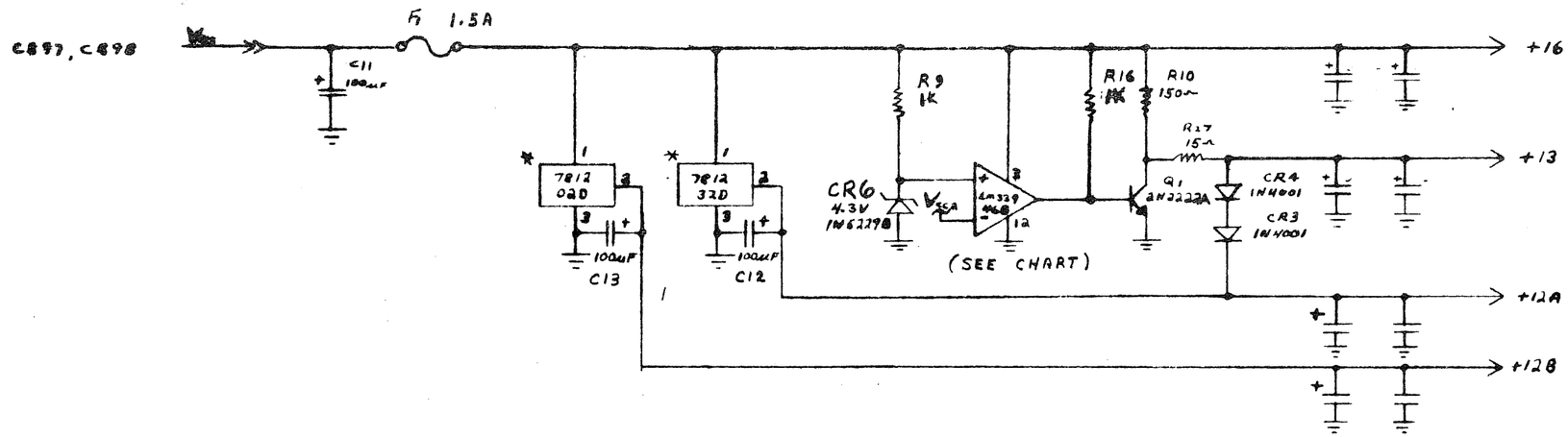
LTR	DATE	REVISION	DR.	CK.

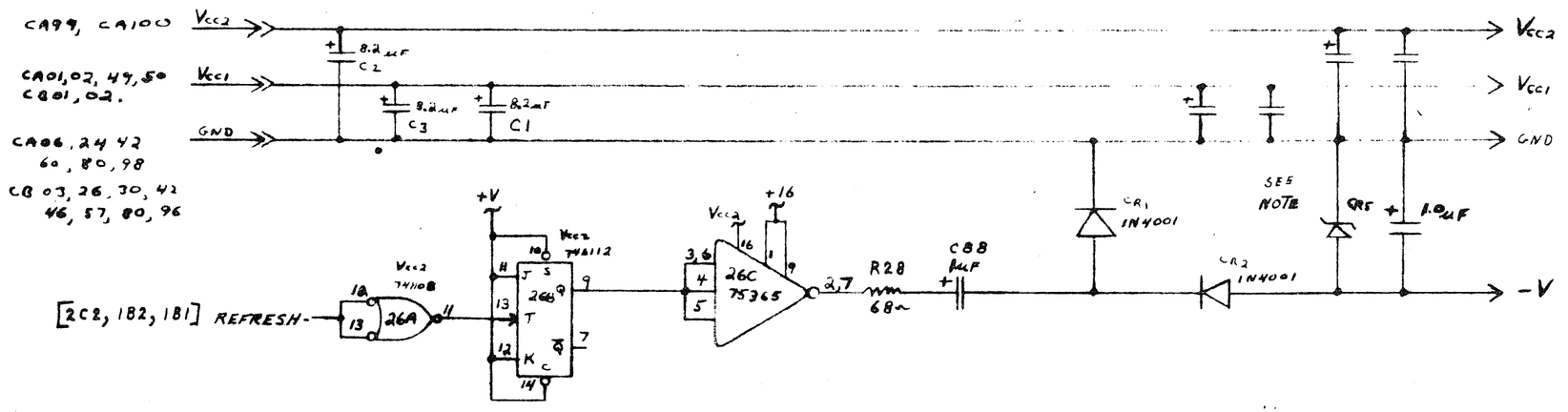




MATERIAL	DWN A.K. 1-30-74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	16K X 18 MOS MEMORY TMS 4030
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ± .02 XXX ± .005 ANGLES ± 1/2°	ENG.	III-24
	APPRD	
	USED ON	SCALE None SHEET 8 OF 9
	NEXT ASSY	SIZE D DWG. NO. LBD 2323 C

LTR	DATE	REVISION	DR.	CK.





NOTE:-

IN5225B(CR5)3.0V ± 5% WITH 4K CHIP (ICD1532)

IN5231B(CR5)5.1V ± 5% WITH 4K CHIP (ICD2307)

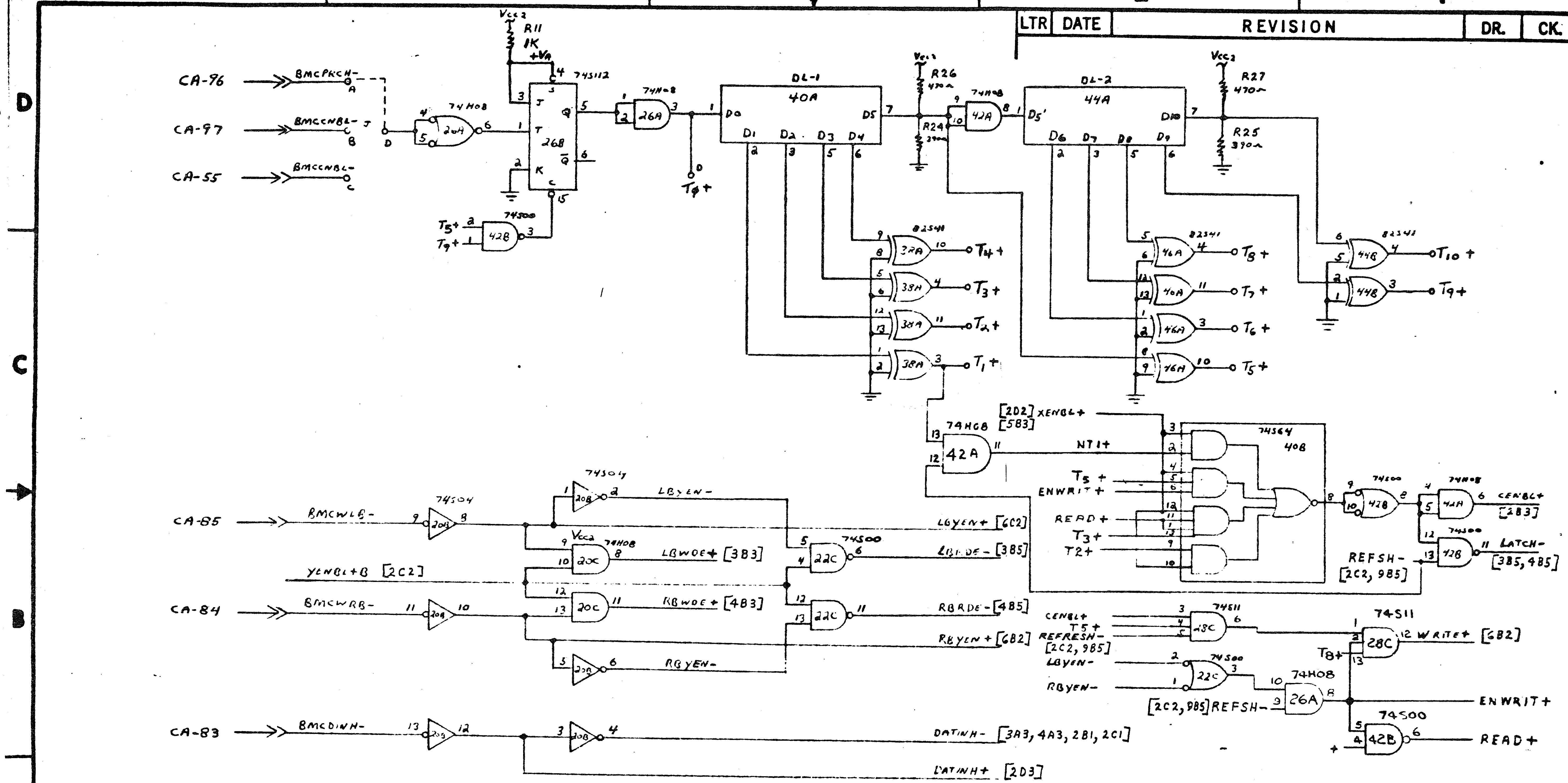
* MOUNTED ON HEAT SINK

CAPACITORS WITH NO VALUE DESIGNATION ARE CAP. TANT 1.0µF, 20V

LM339 COMMON	PINS
+ INPUT	5 7 9 11
- INPUT	4 6 8 10
OUTPUT	2 1 14 13

MATERIAL	DWN A.K. 1-30-74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	16K x 18 MOS MEMORY TMS 4030 III-25 ETCH VERSION
	APPRD	
	USED ON	SCALE
	NEXT ASSY	SHEET 9 OF 9

SIZE B | DWG. NO. LBD2323 | REV. C1



LTR	DATE	REVISION	DR.	CK.

C1										C1
C	1674	RER	C							C
B	1655		B	B	B	B	B	B	B	B
A	REL		A	A	A	A	A	A	A	A
LBD REV	ECN	CK	1	2	3	4	5	6	7	8
			SHEETS							

MATERIAL

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES

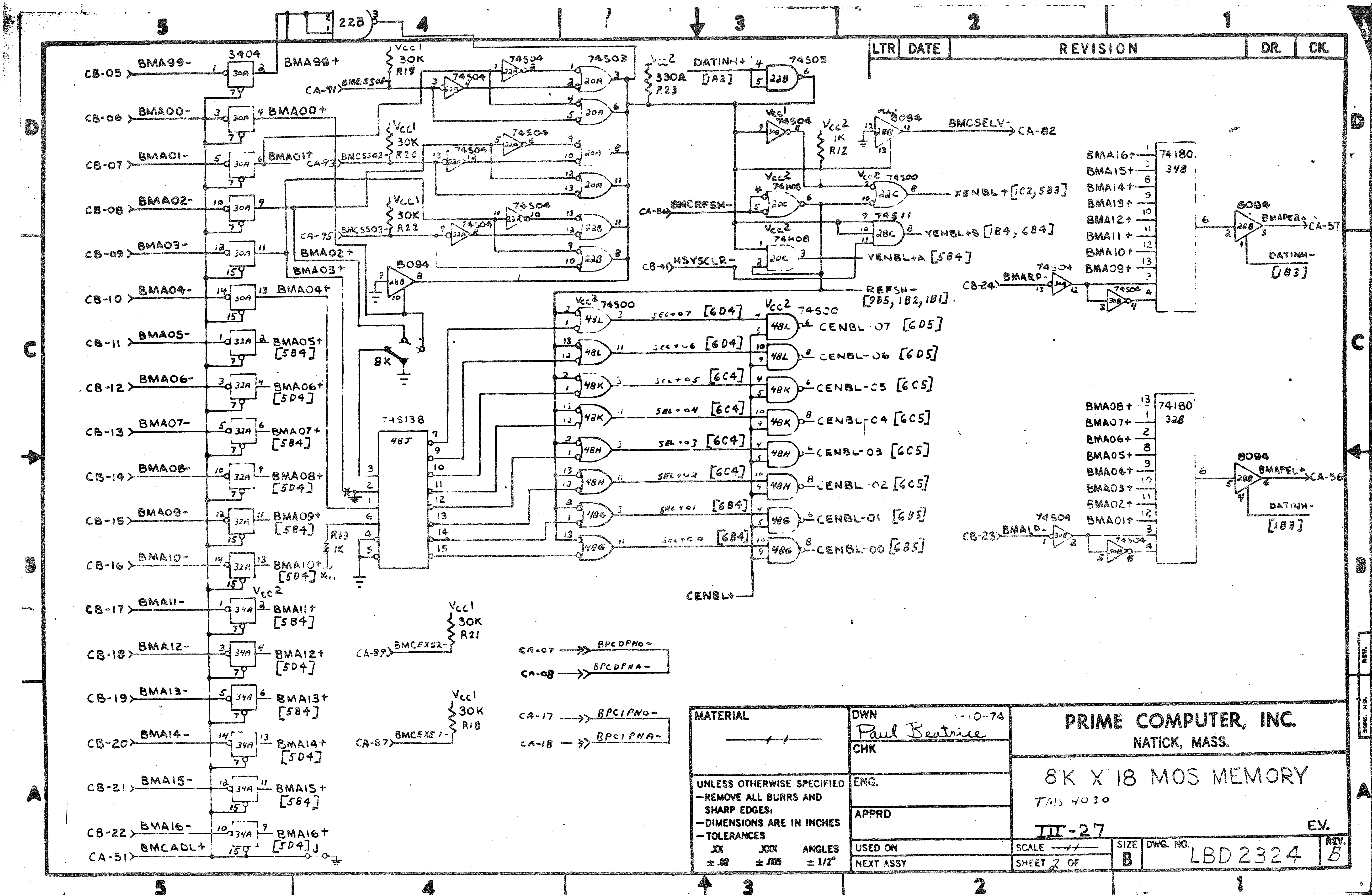
.XX	.XXX	ANGLES
± .02	± .005	± 1/2°

DWN A.K. 1-11-74
CHK
ENG. 7/1/75
APPRD
USED ON
NEXT ASSY

PRIME COMPUTER, INC.
NATICK, MASS.

8K x 18 MOS MEMORY
TMS 4030
III-26
ETCH VERSION

SCALE
SHEET 1 OF 8
SIZE B
DWG. NO. LBD2324
REV. C



CB-05 BMA99- 30A BMA99+
CB-06 BMA00- 30A BMA00+
CB-07 BMA01- 30A BMA01+
CB-08 BMA02- 30A
CB-09 BMA03- 30A
BMA02+
BMA03+
CB-10 BMA04- 30A BMA04+
CB-11 BMA05- 32A BMA05+ [5B4]
CB-12 BMA06- 32A BMA06+ [5D4]
CB-13 BMA07- 32A BMA07+ [5B4]
CB-14 BMA08- 32A BMA08+ [5D4]
CB-15 BMA09- 32A BMA09+ [5B4]
CB-16 BMA10- 32A BMA10+ [5D4]
CB-17 BMA11- 34A BMA11+ [5B4]
CB-18 BMA12- 34A BMA12+ [5D4]
CB-19 BMA13- 34A BMA13+ [5B4]
CB-20 BMA14- 34A BMA14+ [5D4]
CB-21 BMA15- 34A BMA15+ [5B4]
CB-22 BMA16- 34A BMA16+ [5D4]
CA-51 BMCADL+
CA-91 BMCSS0
CA-93 BMCSS02
CA-95 BMCSS03
Vcc1 30K R18
Vcc1 30K R20
Vcc1 30K R22
74S04
74S03
8094
8K
74S138
48J
R13 1K
Vcc2 330Ω R23
DATINH+ [1A2]
BMCSELV- CA-82
Vcc2 1K R12
CA-84 BMCRFSH-
CA-41 HSYSCLR-
74H08
74S00
74S11
XENBL+ [1C2, 5B3]
YENBL+B [1B4, 6B4]
YENBL+A [5B4]
REFSH- [9B5, 1B2, 1B1]
SEL+07 [6D4]
SEL+06 [6D4]
SEL+05 [6C4]
SEL+04 [6C4]
SEL+03 [6C4]
SEL+02 [6C4]
SEL+01 [6B4]
SEL+00 [6B4]
CENBL-07 [6D5]
CENBL-06 [6D5]
CENBL-05 [6C5]
CENBL-04 [6C5]
CENBL-03 [6C5]
CENBL-02 [6C5]
CENBL-01 [6B5]
CENBL-00 [6B5]
CENBL+
74180 34B
BMA16+ BMA15+ BMA14+ BMA13+ BMA12+ BMA11+ BMA10+ BMA09+
BMAPER+ CA-57
DATINH- [1B3]
CB-24 BMARP-
74180 32B
BMA08+ BMA07+ BMA06+ BMA05+ BMA04+ BMA03+ BMA02+ BMA01+
BMAPEL+ CA-56
DATINH- [1B3]
CB-23 BMALP-
CA-89 BMCEXS2-
Vcc1 30K R21
CA-87 BMCEXS1-
Vcc1 30K R18
CA-07 BPCDPNO-
CA-08 BPCDPNA-
CA-17 BPCIPNO-
CA-18 BPCIPNA-
LTR DATE REVISION DR. CK.

MATERIAL	DWN Paul Beatrice 1-10-74	PRIME COMPUTER, INC. NATICK, MASS.
—//—	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	8K X 18 MOS MEMORY TAIS 4030
	APPRD	III-27 E.V.
	USED ON	SCALE —//— SIZE B DWG. NO. LBD 2324 REV. B
	NEXT ASSY	SHEET 2 OF

LTR	DATE	REVISION	DR.	CK.

SDAT-LP [7A4]
SDAT-Ø1 [7A4]
SDAT-Ø2 [7A4]
SDAT-Ø3 [7A3]
SDAT-Ø4 [7A3]
SDAT-Ø5 [7A3]
SDAT-Ø6 [7A2]
SDAT-Ø7 [7A2]
SDAT-Ø8 [7A2]
LATCH- [181, 485]
LBRDE- [183]

3404 06C · 8095 02A · 3404 04A · 75365 08C

WDLP - → WDATLP+ [7A4]
WDØ1 - → WDATØ1+ [7A4]
WDØ2 - → WDATØ2+ [7A4]
WDØ3 - → WDATØ3+ [7A3]
WDØ4 - → WDATØ4+ [7A3]

75365 10C

WDATØ4+ [7A3]
WDATØ5+ [7A3]
WDATØ6+ [7A2]
WDATØ7+ [7A2]
WDATØ8+ [7A2]

BMDØLP+ → CA-77
BMDØ1+ → CA-61
BMDØ2+ → CA-62
BMDØ3+ → CA-63
BMDØ4+ → CA-64
BMDØ5+ → CA-65
BMDØ6+ → CA-66
BMDØ7+ → CA-67
BMDØ8+ → CA-68

3404 06C · 8095 02A · 3404 04A · 75365 10C

WDØ5 - → WDATØ5+ [7A3]
WDØ6 - → WDATØ6+ [7A2]
WDØ7 - → WDATØ7+ [7A2]
WDØ8 - → WDATØ8+ [7A2]

3404 10B · 8095 10A · 3404 08A · 75365 12C

CA-47 → BMCWDLL+ → J

LBWDE+ [183]

+12 → Vcc1, Vcc2 → 75365 (16, 1, 9)

BMDØ8+ → 74180 06A (E)

WDLP -
WDØ1 -
WDØ2 -
WDØ3 -
WDØ4 -
WDØ5 -
WDØ6 -
WDØ7 -
WDØ8 -

74180 06A (Σ) → 8094 08B → BMDPEL- → CA-58

DATINH- [182, 4A3, 2B1, 2C1]

MATERIAL	DWN A.K. 1-9-74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	8K X 18 MOS MEMORY TMS4030 III-28 ETCH VERSION	
	ENG.		
	APPRD		
	USED ON	SCALE	SIZE B
	NEXT ASSY	SHEET 3 OF	DWG. NO. LBD2324 B

LTR	DATE	REVISION	DR.	CK.

SDAT-09 [8A4]
SDAT-10 [8A4]
SDAT-11 [8A3]
SDAT-12 [8A3]
SDAT-13 [8A3]
SDAT-14 [8A3]
SDAT-15 [8A2]
SDAT-16 [8A2]
SDAT-RP [8A2]
LATCH- [181, 385]
RBRDE- [182]

WD09-
WD10-
WD11-
WD12-
WD13-
WD14-
WD15-
WD16-
WDRP-

WDAT 09+ [8A4]
WDAT 10+ [8A4]
WDAT 11+ [8A3]
WDAT 12+ [8A3]
WDAT 13+ [8A3]
WDAT 14+ [8A3]
WDAT 15+ [8A2]
WDAT 16+ [8A2]
WDAT RP+ [8A2]

BMD09+ → CA-69
BMD10+ → CA-70
BMD11+ → CA-71
BMD12+ → CA-72
BMD13+ → CA-73
BMD14+ → CA-74
BMD15+ → CA-75
BMD16+ → CA-76
BMDRP+ → CA-78

CA-43 → BMCWDLR+

RBWDE+ [183]

BMDRP+

WD09-
WD10-
WD11-
WD12-
WD13-
WD14-
WD15-
WD16-
WDRP-

74180 14A

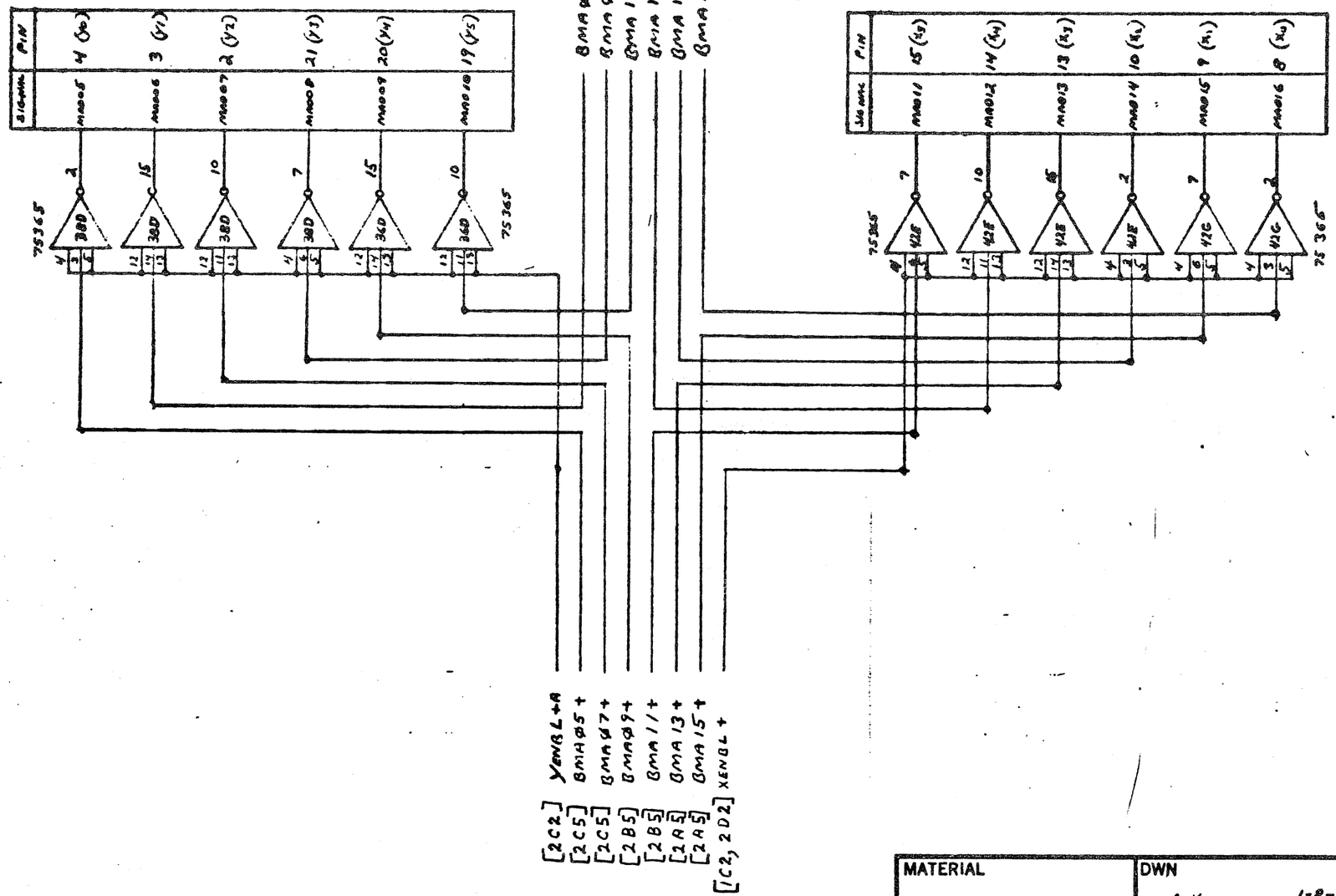
8094 088 → BMDPER- → CA-59

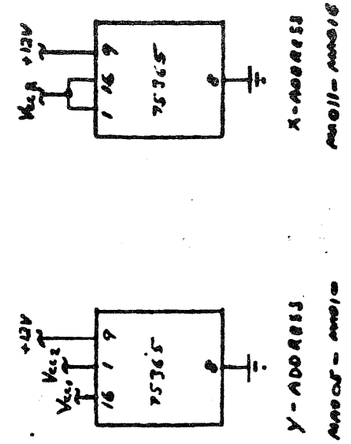
DATINH- [181, 281, 201, 383]

+12 → 75365

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	DWN JK 1-7-74	
	CHK	8K X 18 MOS MEMORY TMS4030
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	III-29 ETCH VERSION
	APPRD	
	USED ON	SCALE — SIZE B — DWG. NO. LBD 2324 — REV. B
	NEXT ASSY	SHEET 4 OF

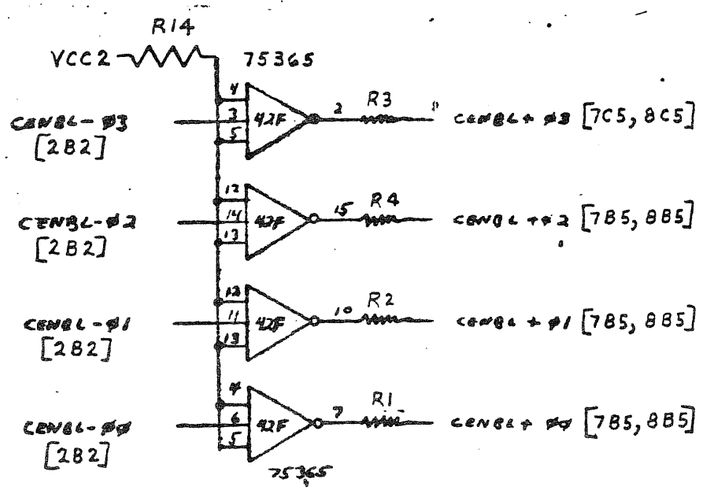
LTR	DATE	REVISION	DR.	CK.

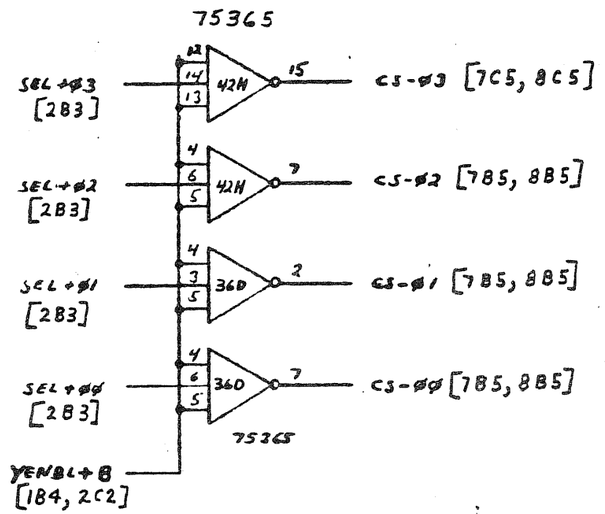


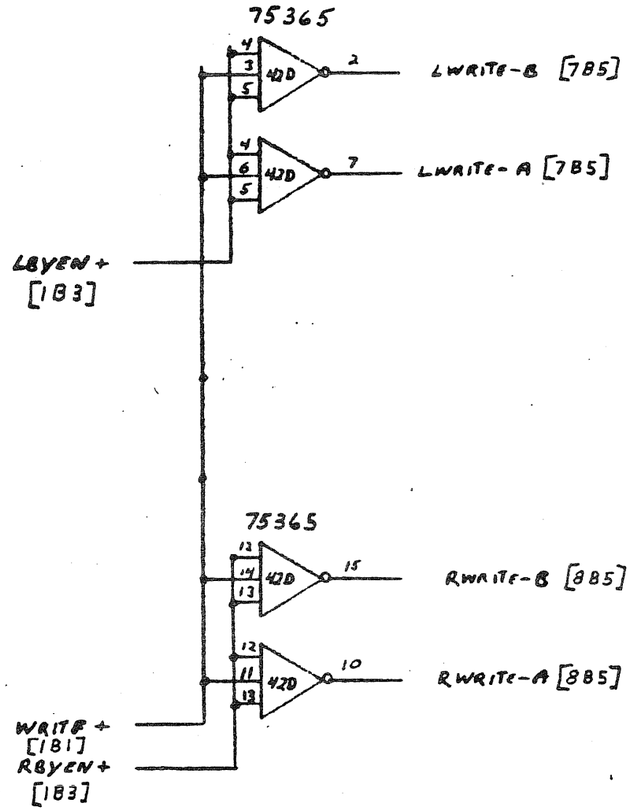


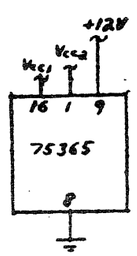
MATERIAL	DWN AK 1-8-74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	8K X 18 MOS MEMORY TMS 4030 ETCH VERSION III-30	
	ENG.		
	APPRD.		
USED ON	SCALE	SIZE B	DWG. NO. LBD2324 REV. B
NEXT ASSY	SHEET 5 OF		

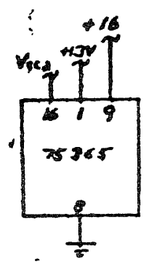
LTR	DATE	REVISION	DR.	CK.





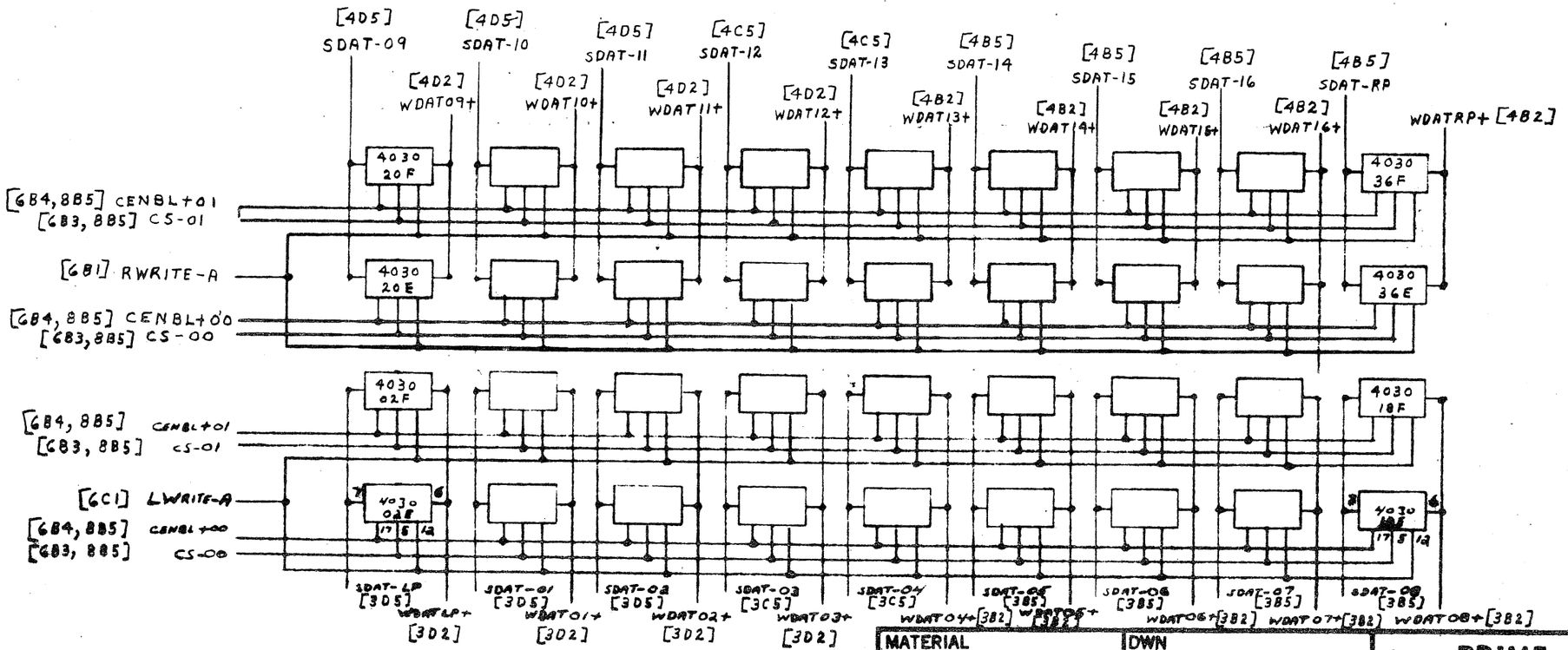






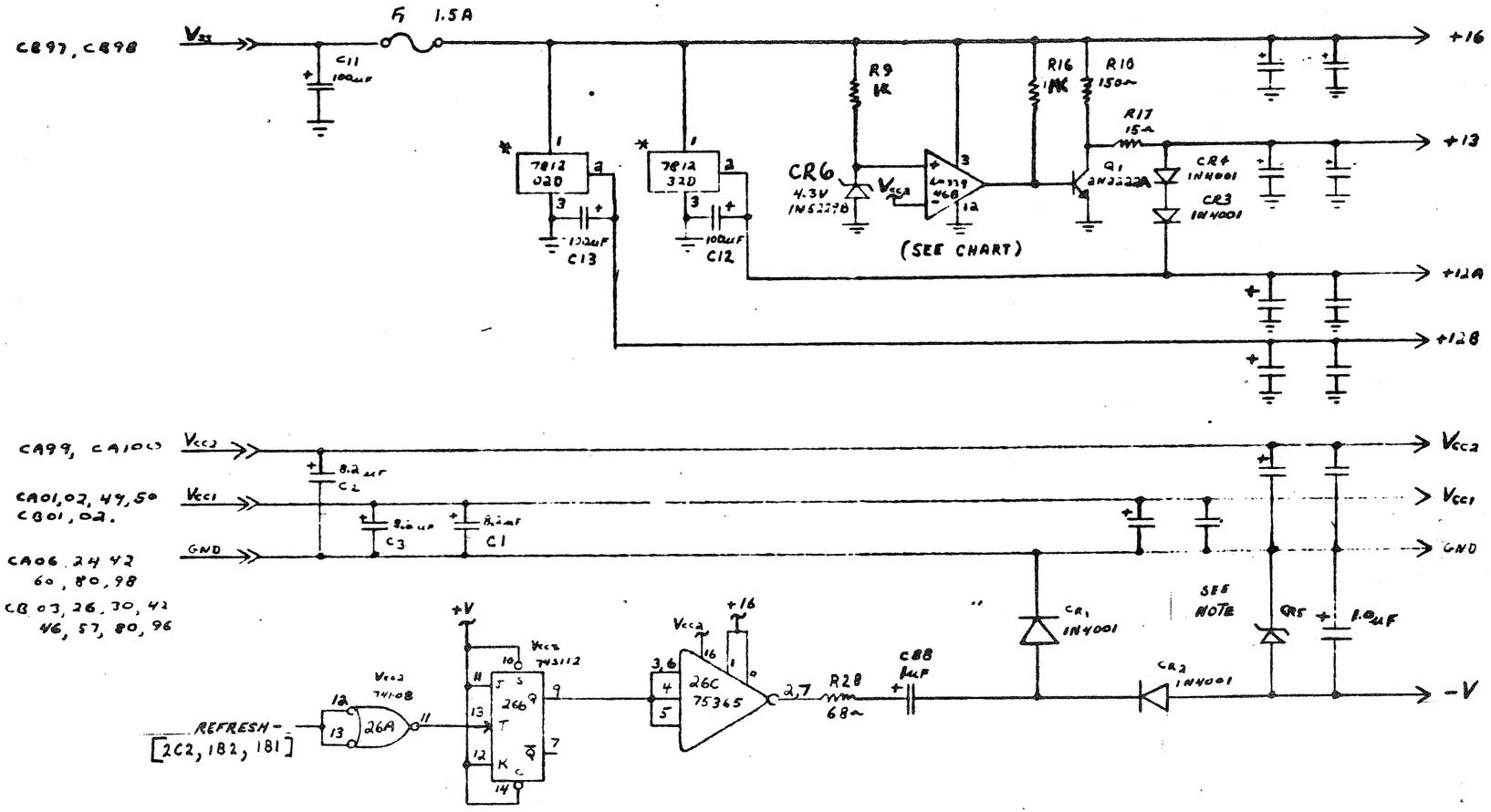
MATERIAL	DWN A.K. 1-8-74	PRIME COMPUTER, INC. NATICK, MASS.			
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK	8K X 18 MOS MEMORY TMS 4030 III-31 ETCH VERSION			
	ENG.				
	APPRD				
	USED ON	SCALE	SIZE B	DWG. NO. LBD2324	REV. 5
	NEXT ASSY	SHEET 6 OF			

LTR	DATE	REVISION	DR.	CK.



MATERIAL	DWN A.K. 1-30-74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	8K X 18 MOS MEMORY TMS 4030	
	ENG.	IT-32	ETCH VERSION
	APPRO		
	USED ON	SCALE None	SIZE B
	NEXT ASSY	SHEET 7 OF	DWG. NO. LBD2324 REV. B

LTR	DATE	REVISION	DR.	CK.



NOTE:-

IN5225B(CR5)3.0V±5% WITH 4K CHIP(ICD1532)

IN5231B(CR5)5.1V±5% WITH 4K CHIP(ICD 2307)

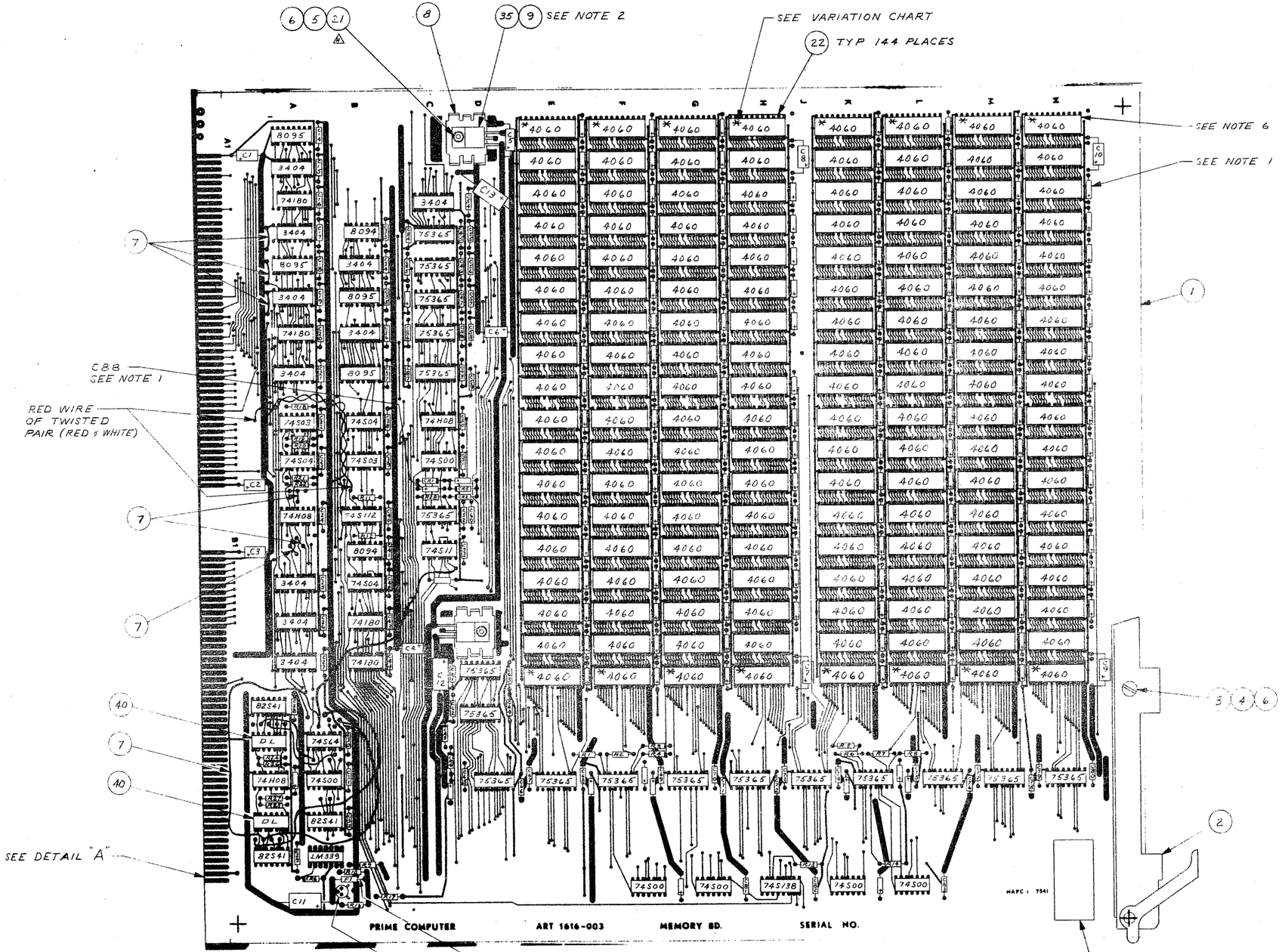
* MOUNTED ON HEAT SINK

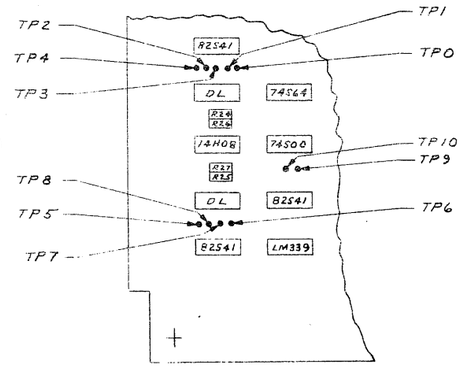
CAPACITORS WITH NO VALUE DESIGNATION ARE CAP. TANT 1.0μf, 20V

LM339 COMMON	PINS
+ INPUT	5 7 9 11
- INPUT	4 6 8 10
OUTPUT	2 1 14 13

MATERIAL	DWN A.K. 1-30-74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	8K x 18 MOS MEMORY TMS 4030
	ENG.	III - 33
	APPRD	8TCH VERSION
	USED ON	SIZE B
	NEXT ASSY	DWG. NO. LBD2324 REV. C1
	SCALE	SHEET 8 OF

M	LTR	DATE	REVISION	DR.	CK.





DETAIL "A"
TEST POINT LOCATIONS

NOTES:
1. UNMARKED DISCRETE COMPONENTS & C88 ARE ITEM 16 (CAP, TANT 1.0 μF, 20V 148 REQ'D).
2. APPLY ITEM 9 (THERMAL COMPOUND) BETWEEN ITEMS 8 AND 35.
3. JUMPER ROUTES SHOWN ARE FOR DWG CLARITY ONLY. SHORTEST ROUTES BETWEEN POINTS WILL BE DETERMINED BY MANUFACTURING.
4. ⚠
5. ALL JUMPERS ARE TO BE YELLOW.
6. Z107B-4 MAY BE USED AS ALTERNATE DIP.

VARIATION CHART

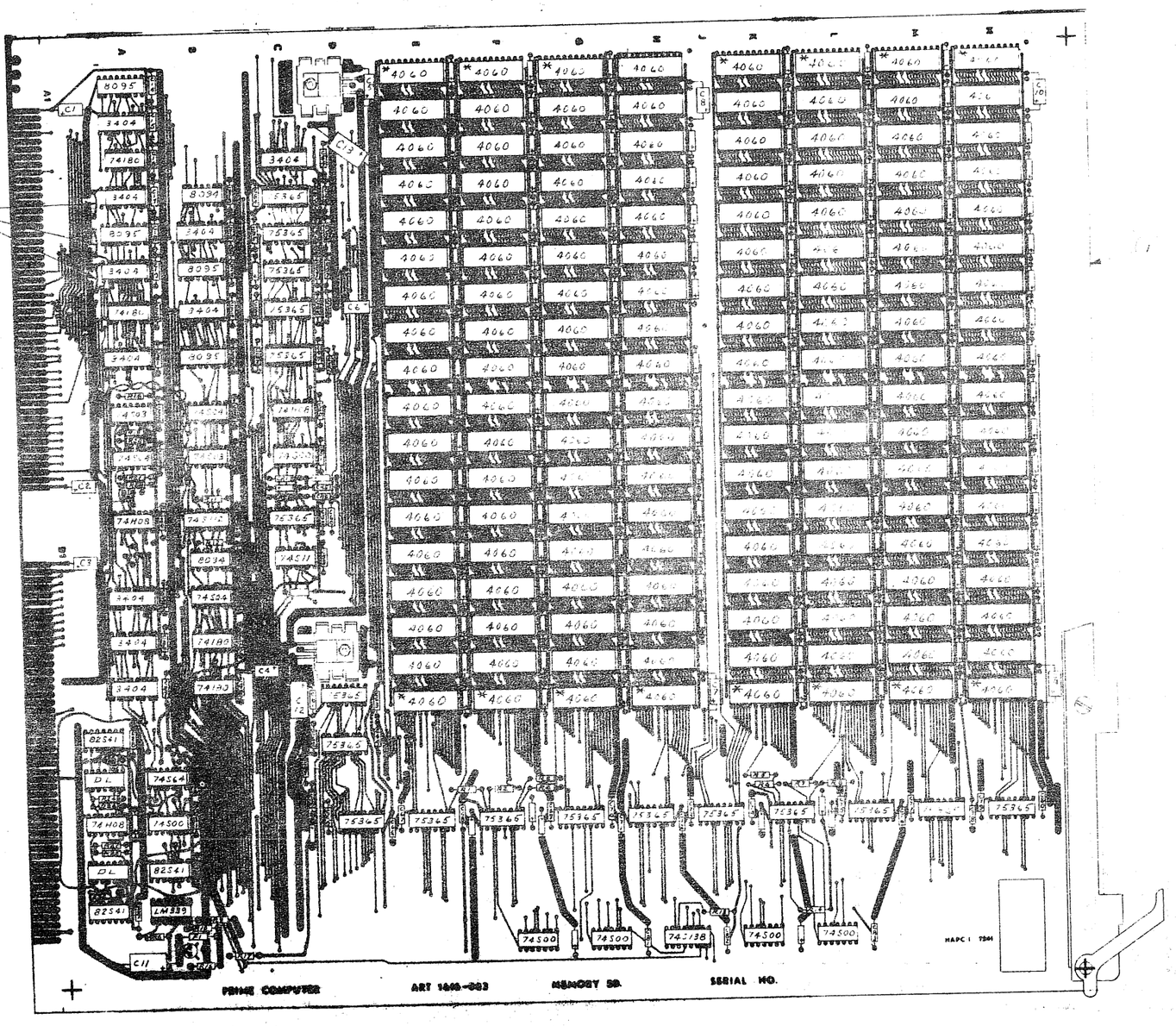
-XXX	DESCRIPTION	VARIATION
-A65	32K x 16 @ 1μS	OMIT DIPS INDICATED WITH ASTERIK
-B85	32K x 18 @ 750NS	AS SHOWN

III-34

MATERIAL	DWN	PRIME COMPUTER, INC. FRAMINGHAM, MASS
UNLESS OTHERWISE SPECIFIED - REMOVE ALL BURRS AND SHARP EDGES - DIMENSIONS ARE IN INCHES - TOLERANCES XX ± .02 XXX ± .005 ANGLES ± 1/2°	CHK APPRD USED ON NEXT ASSY	MEMORY BOARD ASSY 32K @ 5V 4L
	SCALE 1/1	SIZE D DWG NO. 1232-XXX REV J

M	LTR	DATE	REVISION	DR.	CK.
	J	5/6/76	RELEASED FOR 1752	JTS	RKR

REMOVE THESE JUMPER WIRES

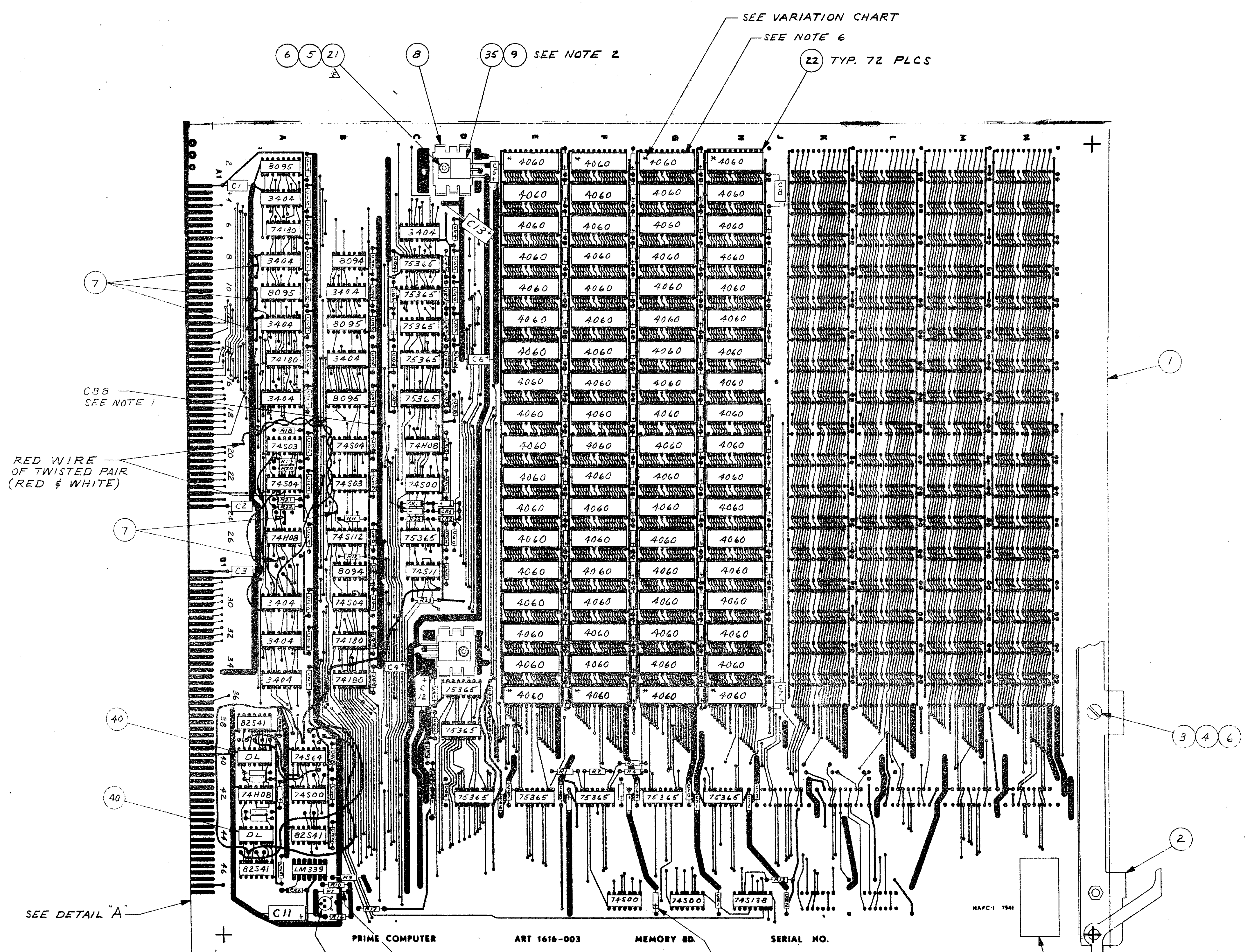


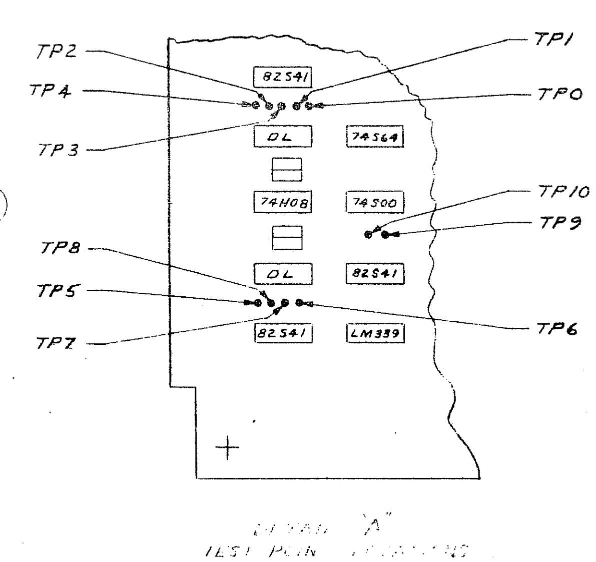
III-35

MATERIAL	DWN Leder 5/5/76	PRIME COMPUTER, INC. FRAMINGHAM, MASS.
UNLESS OTHERWISE SPECIFIED -REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES TOLERANCES XX ±.01 XXX ±.005 ANGLES ±1°	CHK J. Gate Stamp 5/6/76	32K MEMORY WITH P400 MOD
	ENG RRR 5/6/76	44
	APPRD	
	USED ON	SCALE 1/1 SIZE D DWG NO 1232-885X REV J
	NEXT ASSY	SHEET OF

1232-885X

M	LTR	DATE	REVISION	DR.	CK.
	D	11/12/75	PER ECR 1674 (4L)	J.T.S.	RER
	D1	[illegible]	PER ECR 1635 (DOCUMENTATION)	[illegible]	[illegible]
	E	[illegible]	[illegible]	J.T.S.	RK
	F	3/23/76	PER ECR 1743	JTS	RK





NOTES:

1. UNMARKED DISCRETE COMPONENTS & C88 ARE ITEM 16 (CAP, TANT 1.0 µf, 20V. 80 REQ'D)
2. APPLY ITEM 9 (THERMAL COMPOUND) BETWEEN ITEM 8 AND 35.
3. JUMPER ROUTES SHOWN ARE FOR DWG CLARITY ONLY. SHORTEST ROUTES BETWEEN POINTS WILL BE DETERMINED BY MANUFACTURING.

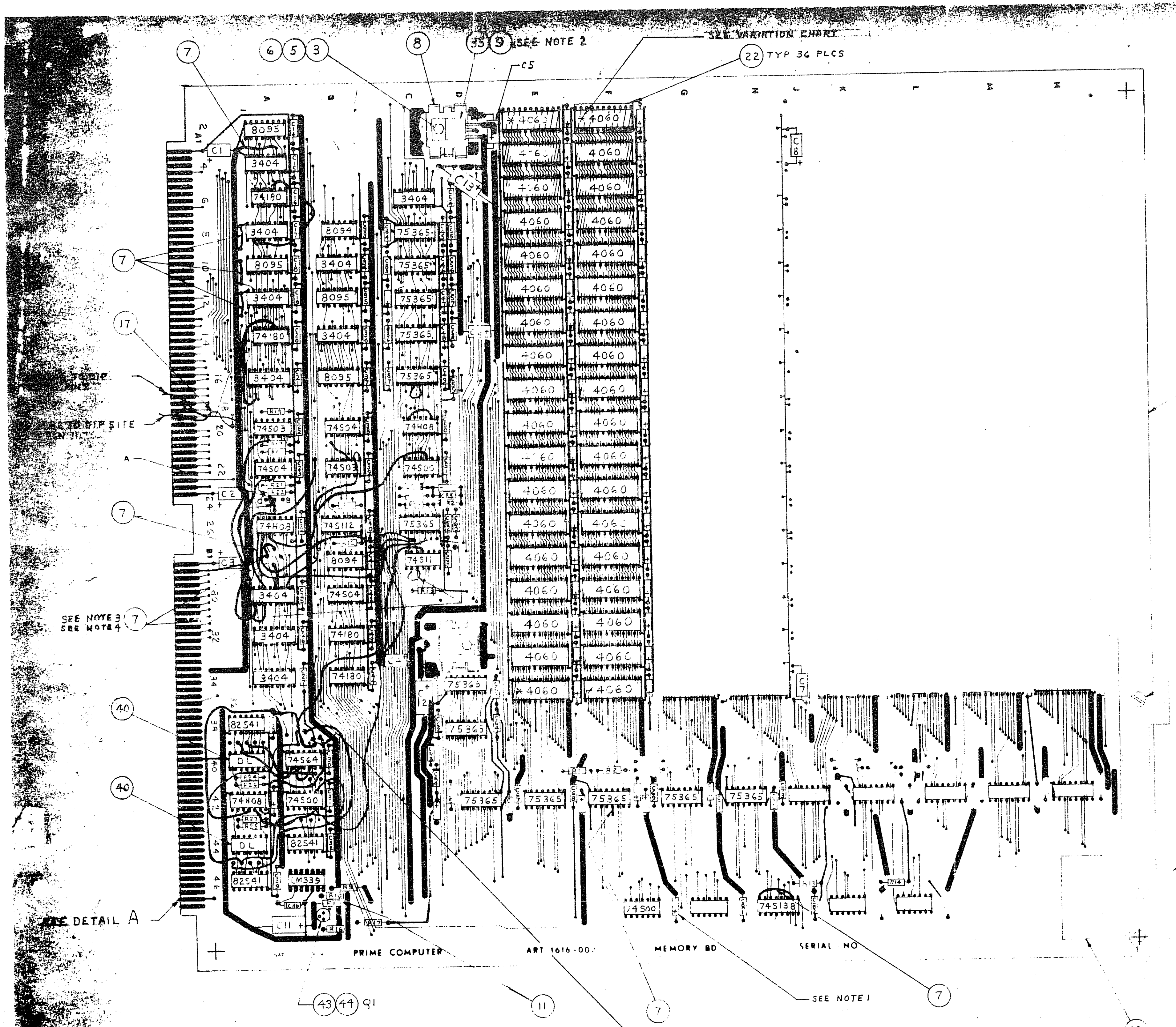
E 4.

5. ALL JUMPERS ARE TO BE YELLOW.
6. 2107B-4 MAY BE USED AS ALTERNATE DIP.
7. FOR ETCH CUTS SEE ECB 2223-004

VARIATION CHART		
-XXX	DESCRIPTION	VARIATION
-A65	16K x 16 @ 1 µS	OMIT DIPS INDICATED WITH ASTERIK
-B85	16K x 18 @ 750NS	AS SHOWN

III-36

MATERIAL	DWN [illegible] 11/10/75	PRIME COMPUTER, INC. FRAMINGHAM, MASS.		
	CHK [illegible]	MEMORY BOARD ASSY 16K - 5V 4L		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG. [illegible]			
	APPRD			
	USED ON	SCALE 1/1	SIZE D	DWG. NO. 1216-XXX
	NEXT ASSY	SHEET 1 OF 1		REV. F1



NOTES:-
1. UNMARKED DISCRETE COMPONENTS ARE ITEM 12 (CAP, TANT 1.0 uf, 20V 45 REQ'D.
2. APPLY ITEM 9 (THERMAL COMPOUND) BETWEEN ITEMS 8 AND 35.
3. JUMPER ROUTES SHOWN ARE FOR DWG CLARITY ONLY. SHORTEST ROUTES BETWEEN POINTS WILL BE DETERMINED BY MANUFACTURING.
4. CUT PIN TO FREE FROM BOARD AT DIP SITE 28C.
5. ALL JUMPERS ARE TO BE YELLOW EXCEPT JUMPER, ITEM 21, THIS IS TO BE BLUE.
6. 2107B-4 MAY BE USED AS ALTERNATE DIP.
7. FOR ETCH CUTS SEE ECB 2223-00?.

LTR	DATE	REVISION	DR.	
C				
D		PER ECN 1671	J.T.S.	RK
		PER ECN 1719		
E	4/1/76	PER ECN 1743	J.T.S.	RK
F	4/21/76	PER ECN 1770	J.T.S.	

VARIATION CHART

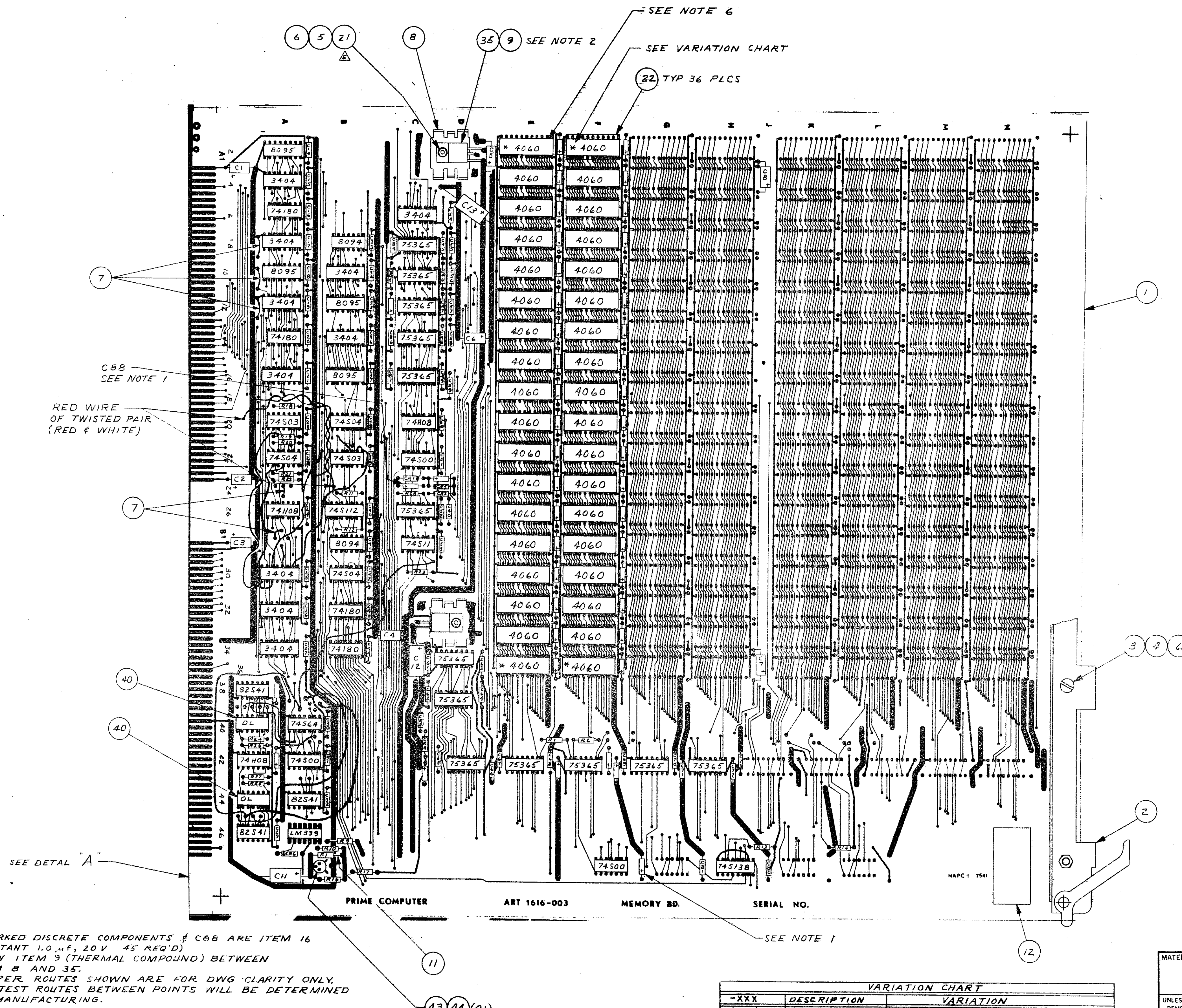
-XXX	DESCRIPTION	
-A65	8K X 16 & 1uS	UNIT TO BE ... AS SHOWN
-B85	8K X 18 & 750nS	

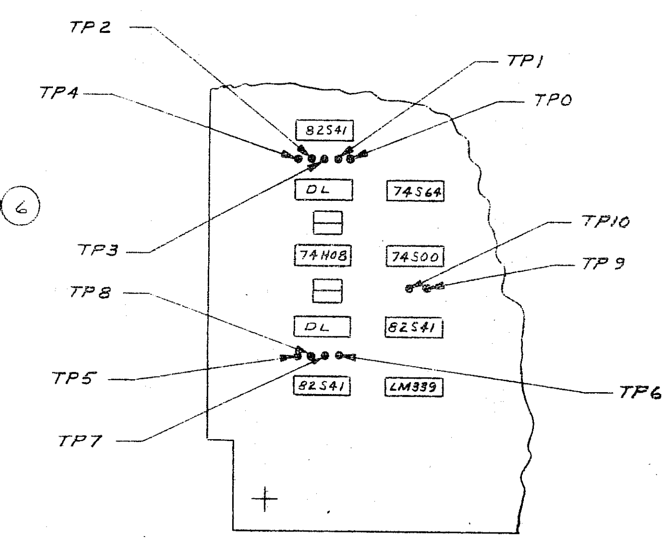
PRIME COMPUTER INC.
NATICK, MASS.

8K W/ PARITY 5V
(2 LAYER BD)

DWG NO 1208-XXX REV F

M	LTR	DATE	REVISION	DR.	CK.
	[illegible]	[illegible]	[illegible] 1674 (41)	J.T.S.	[illegible]
	[illegible]	[illegible]	[illegible] (DOCUMENTATION)	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	RK
	F	3/23/76	PER ECR 1743	JTS	RK
	G	4/23/76	PER ECR 1790	J.T.S.	[illegible]





DETAIL "A"
TEST POINT LOCATION

NOTES:

1. UNMARKED DISCRETE COMPONENTS & C88 ARE ITEM 16 (CAP, TANT 1.0 µf, 20 V 45 REQ'D)
2. APPLY ITEM 9 (THERMAL COMPOUND) BETWEEN ITEM 8 AND 35.
3. JUMPER ROUTES SHOWN ARE FOR DWG CLARITY ONLY. SHORTEST ROUTES BETWEEN POINTS WILL BE DETERMINED BY MANUFACTURING.
4. (E)
5. ALL JUMPERS ARE TO BE YELLOW
6. 2107B-4 MAY BE USED AS ALTERNATE DIP.
7. FOR ETCH CUTS SEE ECB 2223-004

VARIATION CHART

-XXX	DESCRIPTION	VARIATION
-A654L	8K x 16 @ 1µs	OMIT DIPS INDICATED WITH ASTERIK
-B854L	8K x 18 @ 750 NS	AS SHOWN

III-38

MATERIAL	
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES: — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	
DWN	[illegible]
CHK	[illegible]
ENG.	[illegible]
APPRD	
USED ON	
NEXT ASSY	

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY BOARD ASSY
8K W/PARITY 5V
4L

SCALE 1/1 | SHEET 1 OF 1 | SIZE D | DWG. NO. [illegible]08-XXX | REV. G

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. [illegible] 11/12/75
CHK.
ENG. RJR 11/24/75
APPRD.
STANDARD COST _____ DATE _____

TITLE:
MEMORY BD ASSY
32K – 5V
-A65 = 32K x 16 @ 1 µs
-B85 = 32K x 18 @ 750 NS

BOM 1232 -XXX REV. J1

NHA: SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
G	1674	KR	J	1743	RK
G1	1685	RK	J1	1796 1808	RK
G2	00C	RK			
H	1774/1119	RK			

ITEM	SIZE	PART NUMBER	QUANTITY -A65	QUANTITY -B85	DESCRIPTION	STANDARD COST
1	D	PCB1617-003	1	1	P.C. BOARD 32K MEM	G
2	C	MEC 0587	1	1	STIFFENER ASSY, P.C. BD.	
3		MEC0303-005	5	5	SCREW, BD. HD. #4-40 x 5/16 LG.	A
4		MEC 0356	5	5	WASHER, FIBER #4	
5		MEC 0353	2	2	WASHER, FLAT METAL #4	
6		MEC0388-002	7	7	NUT, SELF LOCKING #4-40	
7		WIR1365-004	A/R	A/R	WIRE, 30 AWG (YEL)	
8		MEC 1836-001	2	2	HEATSINK	
9		MEC8068-001	A/R	A/R	THERMAL JOINT COMPOUND	
10		FUS0254-1M2	1	1	FUSE, SUB-MINIATURE 1.5A (F1)	
11		CON 1693-001	2	2	CONNECTOR JACK P.C. BOARD	A1
12	A	MEC 0292	1	1	LABEL, SERIAL & MODEL NO.	
13		CAP0130-407	10	10	CAP, TANT 20V, 8.2 µf ± 10% (C1-C10)	
14		CAP0130-420	3	3	CAP, TANT 20V, 100 µf ± 10% (C11-C13)	
15		CAP0546-001	74	74	CAP, GLASS 50V +80-20% .01 µf (C14-C87)	
16		CAP0552-529	148	148	CAP, TANT 35V 1.0 µf ± 20% (INCLUDING C88)	G A1
17		WIR0616-129	A/R	A/R	WIRE, #30 AWG TWISTED PAIR	
18		DIO154A-001	4	4	DIODE, L.C. RECT IN4001 (CR1-CR4)	
19		DIO1759-211	1	1	DIODE, ZENER ± 5% IN5231B (CR5)	
20		DIO1759-209	1	1	DIODE, ZENER ± 5% IN5229B (CR6)	
21		MEC 0303-006	2	2	SCREW, BD. HD. #4-40 - 3/8 LG	G A
22		CON0650-003	144	144	SOCKET, DIP-22 PINS	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. [illegible] 11/12/75
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE:
MEMORY BD ASSY
32K – 5V
-A65 = 32K x 16 @ 1 µs
-B85 = 32K x 18 @ 750 NS

BOM 1232 -XXX REV. J1

NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -A65	QUANTITY -B85	DESCRIPTION	STANDARD COST
23		ICD 0029	3	3	74H08	
24		ICD 0059	2	2	8094	
25		ICD 0070	1	1	74S64	
26		ICD 0072	1	1	74S112	
27		ICD 0085	6	6	74S00	
28		ICD 0086	3	3	74S04	
29		ICD 0089	1	1	74S11	
30		ICD 0095	1	1	74S138	
31		ICD 0112	4	4	8095	
32		ICD 0183	3	3	82S41	
33		ICD 2306	128	144	4060 / 2107B-4	
34		ICD 1533	18	18	75365	
35		ICD 1547	2	2	7812 UC OR LM340T-12	
36		ICD 90007	2	2	74S03	
37		ICD 90017	10	10	3404	
38		ICD 90030	4	4	74180	
39		ICD 1835	1	1	LM339	
40		MEC 1546-001	2	2	DELAY LINE, 200 - 200 NS	
41						
42						
43		MEC 8260-003	1	1	TRANSISTOR MOUNTING PAD TO18	A
44		TRN 1833-010	1	1	TRANSISTOR, NPN H.S. 2N2222A(QI)	A1

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. [illegible] 11/12/75
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE:
MEMORY BD ASSY
32K – 5V
-A65 = 32K x 16 @ 1 µs
-B85 = 32K x 18 @ 750 NS

BOM 1232 -XXX REV. J1

NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -A65	QUANTITY -B85	DESCRIPTION	STANDARD COST
45		RES 1582-390	8	8	RES., CARBON 1/4 W ± 5% 39 Ω (R1-R8)	
46		RES1582-102	6	6	RES., CARBON 1/4 W ± 5% 1K	
47					(R9, R11 THRU R14, R16)	
48		RES 1582-150	1	1	RES., CARBON 1/4 W ± 5% 15 Ω (R17)	
49		RES1582-151	1	1	RES., CARBON 1/4 W ± 5% 150 Ω (R10)	
50		RES 1582-303	5	5	RES., CARBON 1/4 W ± 5% 30K (R18-R22)	
51		RES1582-331	1	1	RES., CARBON 1/4 W ± 5% 330 Ω (R23)	
52		RES1582-391	2	2	RES., CARBON 1/4 W ± 5% 390 Ω (R24, R25)	
53		RES 1582-471	2	2	RES., CARBON 1/4 W ± 5% 470 Ω (R26, R27)	
54		RES1582-680	1	1	RES., CARBON 1/4 W ± 5% 68 Ω (R28)	
55						
	B	LBD 1902	REF.	REF.	LOGIC BLOCK DIAGRAM, 32K MEM	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Labor 11/12/75
CHK.
ENG. RZR 11/12/75
APPRD.
STANDARD COST _____ DATE _____

TITLE: MEMORY BD ASSY
16K -5V
-A65 = 16K x 16 @ 1μs
-B85 = 16K x 18 @ 750 NS

BOM 1216 **-XXX** REV. F2
NHA: SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
D	1674	RSR	F1	1796/1808	JCL
D1	1685	JCL			
E	1719/1729	RK			
F	1743	RK			

ITEM	SIZE	PART NUMBER	QUANTITY -A65	QUANTITY -B85	DESCRIPTION	STANDARD COST
1	D	PCB1617-003	1	1	P.C. BOARD 32K MEM	A
2	C	MEC0587	1	1	STIFFENER ASSY, P.C. BD.	
3		MEC0303-005	5	5	SCREW, BD. HD. #4-40 x 5/16 LG.	E
4		MEC0356	5	5	WASHER, FIBER #4	
5		MEC0353	2	2	WASHER, FLAT METAL #4	
6		MEC0388-002	7	7	NUT, SELF LOCKING #4-40	
7		WIR1365-004	A/R	A/R	WIRE, 30 AWG (YEL)	
8		MEC1836-001	2	2	HEATSINK	
9		MEC8068-001	A/R	A/R	THERMAL JOINT COMPOUND	
10		FUS0254-002	1	1	FUSE, SUB-MINIATURE 1.5 A (F1)	
11		CON1693-001	2	2	CONNECTOR JACK P.C. BOARD	E
12	A	MEC0292	1	1	LABEL, SERIAL & MODEL NO.	
13		CAP0130-407	8	8	CAP, TANT 20V. 8.2μf ± 10% (C1-C8)	
14		CAP0130-420	3	3	CAP, TANT 20V. 100μf ± 10% (C11-C13)	
15		CAP0546-001	71	71	CAP, GLASS 50V +80-20% .01μf (C14-C75) (C78-C82) (C84-C87)	
16		CAP0552-529	80	80	CAP, TANT 35V. 1.0μf ± 20% (INCLUDING C88)	A A1
17		WIR0616-129	A/R	A/R	WIRE, #30 AWG TWISTED PAIR	
18		DIO1544-001	4	4	DIODE, L.C. RECT IN4001 (CR1-CR4)	
19		DIO1759-211	1	1	DIODE, ZENER ± 5% IN5231B (CR5)	
20		DIO1759-209	1	1	DIODE, ZENER ± 5% IN5229B (CR6)	
21		MEC0303-006	2	2	SCREW, BD. HD #4-40 3/8 LG	A E
22		CON0650-003	72	72	SOCKET, DIP - 22 PINS	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Labor 11/12/75
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: MEMORY BD ASSY
16K -5V
-A65 = 16K x 16 @ 1μs
-B85 = 16K x 18 @ 750 NS

BOM 1216 **-XXX** REV. F2
NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -A65	QUANTITY -B85	DESCRIPTION	STANDARD COST
23		ICD0029	3	3	74H08	
24		ICD0059	2	2	8094	
25		ICD0070	1	1	74S64	
26		ICD0072	1	1	74S112	
27		ICD0085	4	4	74S00	
28		ICD0086	3	3	74S04	
29		ICD0089	1	1	74S11	
30		ICD0095	1	1	74S138	
31		ICD0112	4	4	8095	
32		ICD0183	3	3	82S41	
33		ICD2306	64	72	4060/2107B-4	
34		ICD1533	13	13	75365	
35		ICD1547	2	2	7812UC OR LM340T-12	
36		ICD90007	2	2	74S03	
37		ICD90017	10	10	3404	
38		ICD90030	4	4	74180	
39		ICD1835	1	1	LM339	
40		MEC1546-001	2	2	DELAY LINE, 200Ω - 200 NS	
41						
42						
43		MEC8260-003	1	1	TRANSISTOR MOUNTING PAD TO 18	A
44		TRN1833-010	1	1	TRANSISTOR, NPN H.S. 2N2222A(Q1)	A

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Labor 11/12/75
CHK.
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: MEMORY BD ASSY
16K -5V
-A65 = 16K x 16 @ 1μs
-B85 = 16K x 18 @ 750 NS

BOM 1216 **-XXX** REV. F2
NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -A65	QUANTITY -B85	DESCRIPTION	STANDARD COST
45		RES1582-390	4	4	RES., CARBON 1/4 W ± 5% 39Ω (R1-R4)	
46		RES1582-102	6	6	RES, CARBON, 1/4 W ± 5% 1K	
47					(R9, R11 THRU R14, R16)	
48		RES1582-150	1	1	RES, CARBON 1/4 W ± 5% 15Ω (R17)	
49		RES1582-151	1	1	RES., CARBON 1/4 W ± 5% 150Ω (R10	
50		RES1582-303	5	5	RES., CARBON 1/4 W ± 5% 30K (R18-R22)	
51		RES1582-331	1	1	RES., CARBON 1/4 W ± 5% 330Ω (R23)	
52		RES1582-391	2	2	RES., CARBON 1/4 W ± 5% 390Ω (R24, R25)	
53		RES1582-471	2	2	RES., CARBON 1/4 W ± 5% 470Ω (R26, R27)	
54		RES1582-680	1	1	RES., CARBON 1/4 W ± 5% 68Ω (R28)	
	D	ECB2223-004	REF.	REF.	P.C. BOARD 16K MEM W/ETCH CUTS	A
	B	LBD2323	REF.	REF.	LOGIC BLOCK DIAGRAM, 16K MEM	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Ledo 11/12/75
CHK.
ENG. [illegible] 11/12/75
APPRD.

STANDARD COST _____ DATE _____

TITLE: MEMORY BD ASSY
8K – 5V
-A65 = 8K × 16 @ 1μs
-B85 = 8K × 18 @ 750 NS

BOM 1208 **-XXX** REV. F
NHA: SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
B	REL	[illegible]	E	1743	[illegible]
C	1637 1639	[illegible]	F	1790	[illegible]
C1	1671	RK			
D	1719	RK			

ITEM	SIZE	PART NUMBER	QUANTITY -A65	QUANTITY -B85	DESCRIPTION	STANDARD COST
1	D	PCB1617-001	1	1	P.C. BOARD 32K MEM	
2	C	MEC0587	1	1	STIFFENER ASSY, P.C. BD	
3		MEC0303-005	5	5	SCREW, BD. HD. # 4-40 × 5/16 LG.	
4		MEC0356	5	5	WASHER, FIBER # 4	
5		MEC0353	2	2	WASHER, FLAT METAL # 4	
6		MEC0388-002	7	7	NUT, SELF LOCKING # 4-40	
7		WIR1365-004	A/R	A/R	WIRE, 30 AWG (YEL)	
8		MEC1836-001	2	2	HEATSINK	
9		MEC8068-001	A/R	A/R	THERMAL JOINT COMPOUND	
10		FUS0254-002	1	1	FUSE, SUB-MINIATURE 1.5A (F1)	
11		CON1693-001	2	2	CONNECTOR JACK P.C. BOARD	
12	A	MEC0292	1	1	LABEL, SERIAL & MODEL NO.	
13		CAP0130-407	8	8	CAP, TANT 20V, 8.2 mf ± 10% (C1-C8)	
14		CAP0130-420	3	3	CAP, TANT 20V. 100 mf ± 10% (C11-C13)	
15		CAP0546-001	69	69	CAP, GLASS 50V +80-20% .01 mf (C14-C73)	(C81, C82) (C84-C87)
16		CAP0552-529	45	45	CAP, TANT 35V. 1.0 mf ± 20% (INCLUDING C88)	
17		WIR0616-129	A/R	A/R	WIRE, #30 AWG TWISTED PAIR	
18		DIO1544-001	4	4	DIODE, L.C. RECT IN4001 (CR1-CR4)	
19		DIO1759-211	1	1	DIODE, ZENER ± 5% IN5231B (CR-5)	
20		DIO1759-209	1	1	DIODE, ZENER ± 5% IN5229B (CR-6	
21		MEC0303-006	2	2	SCREW, BD. HD. # 4-40 × 3/16 LG	
22		CON0650-003	36	36	SOCKET, DIP-22 PINS	

PBF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Ledo 11/12/75
CHK.
ENG.
APPRD.

STANDARD COST _____ DATE _____

TITLE: MEMORY BD. ASSY
8K – 5V
-A65 = 8K × 16 @ 1μs
-B85 = 8K × 18 @ 750 NS

BOM 1208 **-XXX** REV. F
NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -A65	QUANTITY -B85	DESCRIPTION	STANDARD COST
23		ICD0029	3	3	74H08	
24		ICD0059	2	2	8094	
25		ICD0070	1	1	74S64	
26		ICD0072	1	1	74S112	
27		ICD0085	3	3	74S00	
28		ICD0086	3	3	74S04	
29		ICD0089	1	1	74S11	
30		ICD0095	1	1	74S138	
31		ICD0112	4	4	8095	
32		ICD0183	3	3	82S41	
33		ICD2306	32	36	4060/21078-4	
34		ICD1533	13	13	75365	
35		ICD1547	2	2	7812UC OR LM340T-12	
36		ICD90007	2	2	74S03	
37		ICD90017	10	10	3404	
38		ICD90030	4	4	74180	
39		ICD1835	1	1	LM339	
40		MEC1546-001	2	2	DELAY LINE, 200 Ω – 200 NS	
41						
42						
43		MEC8260-003	1	1	TRANSISTOR MOUNTING PAD TO18	
44		TRN1833-010	1	1	TRANSISTOR, NPN H.S. 2N2222A(J)	

PBF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Ledo 11/12/75
CHK.
ENG.
APPRD.

STANDARD COST _____ DATE _____

TITLE: MEMORY BD ASSY
8K – 5V
-A65 = 8K × 16 @ 1μs
-B85 = 8K × 18 @ 750 NS

BOM 1208 **-XXX** REV. F
NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -A65	QUANTITY -B85	DESCRIPTION	STANDARD COST
45		RES1582-390	2	2	RES., CARBON 1/4 W ± 5% 39Ω (R1-R2)	
46		RES1582-102	6	6	RES., CARBON 1/4 W ± 5% 1K	
47					(R9, R11 THRU R14, R16)	
48		RES1582-150	1	1	RES., CARBON 1/4 W ± 5% 15Ω (R17)	
49		RES1582-151	1	1	RES., CARBON 1/4 W ± 5% 150Ω (R10)	
50		RES1582-303	5	5	RES., CARBON 1/4 W ± 5% 30K (R18-R22)	
51		RES1582-331	1	1	RES., CARBON 1/4 W ± 5% 330Ω (R23)	
52		RES1582-391	2	2	RES., CARBON 1/4 W ± 5% 390Ω (R24-R25)	
53		RES1582-471	2	2	RES., CARBON 1/4 W ± 5% 470Ω (R26-R27)	
54		RES1582-680	1	1	RES., CARBON 1/4 W ± 5% 68Ω (R28)	
	D	ECB2223-002	REF.	REF.	P.C. BOARD 8K MEM W/ETCH CUTS	
	B	LBD2324	REF.	REF.	LOGIC BLOCK DIAGRAM, 8K MEM	

PBF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Anderson 11/12/75
CHK.
ENG. R.C.R 11/12/75
APPRD.
STANDARD COST_____ DATE_____

TITLE: MEMORY BD ASSY
8K – 5V
-A65 = 8K x 16 @ 1μs
-B85 = 8K x 18 @ 750 NS

BOM 1208 **-XXX** REV. G_2
NHA: SHT. 1 OF 3

REV.	ECN	CK	REV.	ECN	CK
D	1674	PCK	G	1790	RK
D1	1695	RK	G1	1908/1796	JRL
E	1714/1719	RK			
F	1743	RK			

ITEM	SIZE	PART NUMBER	QUANTITY -A65 4L	QUANTITY -B85 4L	DESCRIPTION	STANDARD COST
1	D	PCB1617-003	1	1	P.C. BOARD 32K MEM	(1)
2	C	MEC0587	1	1	STIFFENER ASSY, P.C. BD	
3		MEC0303-005	5	5	SCREW, BD. HD. #4-40 x 5/16 LG.	(2)
4		MEC0356	5	5	WASHER, FIBER #4	
5		MEC0353	2	2	WASHER, FLAT METAL #4	
6		MEC0388-002	7	7	NUT, SELF LOCKING #4-40	
7		WIR1365-004	A/R	A/R	WIRE, 30 AWG (YEL)	
8		MEC1836-001	2	2	HEATSINK	
9		MEC8068-001	A/R	A/R	THERMAL JOINT COMPOUND	
10		FUS0254-002	1	1	FUSE, SUB-MINIATURE 1.5A (F1)	
11		CON1693-001	2	2	CONNECTOR JACK P.C. BOARD	(3)
12	A	MEC0292	1	1	LABEL, SERIAL & MODEL NO.	
13		CAP0130-407	8	8	CAP. TANT 20V, 8.2 mf ± 10% (C1-C8)	
14		CAP0130-420	3	3	CAP. TANT 20V. 100 mf ± 10% (C11-C13)	
15		CAP0546	69	69	CAP. GLASS 25V. .01 mf ± 20% (C14-C73)	(C81, C82) (-B4 - C87)
16		CAP0552-5Z9	45	45	CAP. TANT 35V 1.0 mf ± 20% (INCLUDING C88)	(2) (3)
17		WIR0616-129	A/R	A/R	WIRE, #30 AWG TWISTED PAIR	
18		DIO1544-001	4	4	DIODE, L.C. RECT 1N4001 (CR1-CR4)	
19		DIO1759-211	1	1	DIODE, ZENER ± 5% 1N5231B (CR-5)	
20		DIO1753-209	1	1	DIODE, ZENER ± 5% 1N52298 (CR-6	
21		MEC0303-006	2	2	SCREW, BD. HD. #4-40 x 3/4 LG	(4)
22		CON0650-003	36	36	SOCKET, DIP-22 PINS	

PDP-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Anderson 11/12/75
CHK.
ENG.
APPRD.
STANDARD COST_____ DATE_____

TITLE: MEMORY BD. ASSY
8K – 5V
-A65 = 8K x 16 @ 1μs
-B85 = 8K x 18 @ 750 NS

BOM 1208 **-XXX** REV. G_2
NHA: SHT. 2 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -A65 4L	QUANTITY -B85 4L	DESCRIPTION	STANDARD COST
23		ICD0029	3	3	74H08	
24		ICD0059	2	2	8094	
25		ICD0070	1	1	74S64	
26		ICD0072	1	1	74S112	
27		ICD0085	3	3	74S00	
28		ICD0086	3	3	74S04	
29		ICD0089	1	1	74S11	
30		ICD0095	1	1	74S138	
31		ICD0112	4	4	8095	
32		ICD0183	3	3	82S41	
33		ICD2306	32	36	4060/21078-4	
34		ICD1533	13	13	75365	
35		ICD1547	2	2	7812UC OR LM340T-12	
36		ICD90007	2	2	74S03	
37		ICD90017	10	10	3404	
38		ICD90030	4	4	74180	
39		ICD1835	1	1	LM339	
40		MEC1546-001	2	2	DELAY LINE, 200 Ω - 200 NS	
41						
42						
43		MEC8260-003	1	1	TRANSISTOR MOUNTING PAD TO18	(5)
44		TRN1833-010	1	1	TRANSISTOR, NPN H.S. 2N2222A	(6)

PDP-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Anderson 11/12/75
CHK.
ENG.
APPRD.
STANDARD COST_____ DATE_____

TITLE: MEMORY BD ASSY
8K – 5V
-A65 = 8K x 16 @ 1μs
-B85 = 8K x 18 @ 750 NS

BOM 1208 **-XXX** REV. G_2
NHA: SHT. 3 OF 3

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -A65 4L	QUANTITY -B85 4L	DESCRIPTION	STANDARD COST
45		RES1582-390	2	2	RES., CARBON 1/4 W ± 5% 39Ω (R1-R2)	
46		RES1582-102	6	6	RES., CARBON 1/4 W ± 5% 1K	(7)
47					(R9, R11 THRU R14, R16)	
48		RES1582-150	1	1	RES., CARBON 1/4 W ± 5% 15Ω (R17)	
49		RES1582-151	1	1	RES., CARBON 1/4 W ± 5% 150Ω (R10)	
50		RES1582-303	5	5	RES., CARBON 1/4 W ± 5% 30K (R18-R22)	
51		RES1582-331	1	1	RES., CARBON 1/4 W ± 5% 330Ω (R23)	
52		RES1582-391	2	2	RES., CARBON 1/4 W ± 5% 390Ω (R24-R25)	
53		RES1582-471	2	2	RES., CARBON 1/4 W ± 5% 470Ω (R26-R27)	
54		RES1582-680	1	1	RES., CARBON 1/4 W ± 5% 68Ω (R28)	
	D	ECB2223-004	REF	REF	P.C. BOARD 8K MEM W/ETCH CUTS	(8)
	B	LBD2324	REF	REF	LOGIC BLOCK DIAGRAM, 8K MEM	

PDP-004A

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DWN. M.B 3/8/76
CHK. R.C.L 3/8/76
ENG. R.C.R 3/8/76
APPRD.
STANDARD COST_____ DATE_____

TITLE: 32K MEMORY WITH P400 MOD

BOM 1232-B85X REV. J
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
J	RELEASED 1757	JR			

ITEM	SIZE	PART NUMBER	QUANTITY	DESCRIPTION	STANDARD COST
1	D	1232-885	1	MEMORY, 750 NS, 32K/18 -5V	
				NOTE:	
				SEE ECR 1757	

DATE: January 31, 1977 PE-T-303

TO: Programming and Engineering

FROM: Ross E. Roberts

SUBJECT: 32K Interleavable Memory Module

INTRODUCTION:

The intent of this document is to describe the 32K memory module intended to operate in conjunction with the existing PRIME processors and with the P400 in interleaved mode. A general discussion will include the modules' functions, capacity, variations and interface. An in-depth discussion will include detailed descriptions of the major functional blocks of the module and the operations they execute within the context of the modules' function.

GENERAL DESCRIPTION

FUNCTION/CAPACITY:

Each module contains module selection logic, self contained clock generation logic, address interface, MOS driver circuits, and the MOS storage elements. The interface is TTL compatible and operates on a common bus (backplane) from which is received the address, data and control signals required for operation. Each module is capable of functioning with up to 15 additional modules. Storage capacity of a single fully populated module is 32KX18. The storage array is comprised of 144 4KX1 N-channel MOS dynamic RAMS arranged in eight rows, 18 wide. Additional capacities are obtained by depopulating the module.

DEVICES:

Each storage device requires twelve address inputs, a high level (12V) CENBL clock, a chip select, read/write control data in and data out. The twelve addresses are divided equally into column address (high order adresses) and row address (low order address) resulting in a chip organization of 64 rows x 64 columns.

Dynamic RAM'S store data as a charge or no charge condition on parasitic junction capacitors and, as in any capacitor, charge is lost through leakage and it is necessary to restore or refresh that charge periodically. These devices are constructed such that refreshing a single row will refresh all columns intersecting that row. Thus, if a refresh cycle is executed every 32 microseconds and the refresh address counter is sequentially advanced through the 64, states the entire device will be refreshed within the required 2 Ms. A refresh cycle at the chip is essentially a read cycle. The device requires that a CENBL

be applied for all operations. The condition of the read/write line defines the type of cycle and chip select enables the data output buffer. All signals to the device excepting CENBL, are TTL compatible. Further details may be obtained by referencing the Texas Instrument Memory Data Book or the Intel Application note AD-10, "Memory System Design with the Intel 2107B 4K RAM.

VARIATIONS:

The module is capable of being provided in several variations. The basic module is compatible with its predecessors in that it can be operated in the P200 and P300 as well as in the P400 in either a 32KX18 capacity or 16KX18 capacity. In addition to this compatible operation, the module can be modified such that it's performance can take advantage of some of the P400's unique characteristics. The modification renders the board incompatible with P200 and 300 machines (not permanently). The module is also provided with logic which, in the P400 only, allows it to interleave with a second module. This feature permits the storing and retrieval of two data words in less than two normal (non-interleaved) memory cycles. The interleave feature is activated by DIP switches on the board. Interleave must always entail a pair or pairs of modules (i.e. a single module cannot interleave with itself) and the modules must be 32K capacity.

The following table indicates the models available:

Capacity	Model No.	Usage
16,384 X 18	1216-B85Y	P200,300,400 (Compatible Timing)
16,384 X 16	1216-A65Y	P100
32,768 X 16	1232-A65Y	P100
32,768 X 18	1232-B85Y	P200,300,400 (Compatible Timing)
32,768 X 18	2132-D85	P400 (only)

INTERFACE:

The module interface is entirely TTL compatible. The interface consists of three general functions.

The data is 16 data bits and two parity bits wide and is carried ona bidirectional tri-state bus. The address bus carries 22 addresses and three address parity bits. The balance of the interface is comprised of control signals to and from the processor.

DATA:

Data is transmitted to or from the memory as a positive true (1=+5V). There are two 8 bit bytes with an odd parity bit associated with each byte. The memory read-data lines, and the memory write data lines are duplexed onto the bus using tri-state drivers exclusively. The memory

data bus is designated "BMD". Data is stored and retrieved with no polarity inversion. The module parity checkers associated with the data bus are always active and indicate the state of bus parity during both read and write cycles. These outputs are, however, only examined by the processor during write cycles.

ADDRESS:

The address bus is negative true (1=0V). There are 22 addresses which are designated "BMA". Address bits BMA16 through BMA3X which are the refresh addresses.

Addresses BMA04, 03 and 02 are used to select one of the eight rows of devices to receive chip enable. All other rows remain inactive. BMA01, 00, 99 and 98 select one module from the possible 16. The remaining addresses, BMA 97, 96 and 95 will cause an unconditional deselect of modules in the backplane. Three parity bits are odd parity on their respective fields (see Fig. 2).

CONTROL:

Input: There are nine control functions used by the module. All memory control lines are designated "BMC". The following tabulation indicates the signal and its function.

BMCPRCH - Initiates the timing generator on each module and is required for all cycles including refresh.

BMCWRB - Indicates to the memory the type of cycle to be executed (read or write).

BMCADL+ - Latches address into all modules (P400 only).

BMCWDL+ - Latches write data into all modules (P400 only).

BMCRFSH - Signals all modules that the next cycle will be a refresh cycle.

BMCDINH - Disables all modules.

BMCI - It is transmitted if an interleave cycle is to be executed.

BMCEBL - Selects which board of an interleaved pair will receive or transmit data.

HSYSCLR - System clear forces certain addresses to a low power state during back-up operation.

Output: The module issues control and status signals to the processor as outlined below.

BMCSELV - Is issued from the selected module indicating to the processor that memory is present.

BMCSELB - In the P400 only signals to the processor that 400 timing is available from the module.

BMCSELC - Not active.

BMCSELD - Not active.

BMCINLV - Indicates to the processor that the modules can interleave.

BMCPEL - Indicates a write data parity error on the left byte (See Fig. 2).

BMCPER - Indicates a write data parity error on the right byte (See Fig. 2).

BMAPER+ - Indicates an address parity error on the low order address bits (See Fig. 2).

BMAPEL+ - Indicates an address parity error in the high order address bits (See Figure 2).

DETAILED DESCRIPTION:

Address, Normal

The 22 bit address field is transmitted to the modules at the beginning of each cycle. All addresses are received by individual modules via latches as are the pertinent parity bits. The latches are used as buffers in P200 & 1300 and no latching occurs at the modules. The P400 does transmit BMCADL and latches the addresses into each module for the duration of the cycle. The 7 high order addresses perform a module select function. Addresses BMA97, BMA96 and BMA95 are OR'D and cause SEL- to be unconditionally invalid. BMA01 through BMA98 are compared to the fixed slot select field (BMCSS03, BMCSS02-, BMCSS01- and BMCEXS2-) by means of exclusive OR's. If the variable address matches the fixed slot selects the board is selected and BMCSELV- is issued to the processor. At this time, the additional information concerning timing and interleave capability are also transmitted to the processor. The select condition on a module also generates XENBL and YENBL on the module. These signals, when valid, permit address and timing clocks to reach the storage devices.

The next three addresses (BMA04, BMA03 and BMA02) are supplied to a 1 of 8 decoder. The resulting output enables CENBL, CSEL, and R/W to be supplied to one of the eight rows of storage devices.

The remaining addresses are supplied to all of the storage elements and serve to select one location in a 4k block. This single location is then written into or read from the selected row.

Interleave:

Interleave operation requires some relatively minor modifications to the addressing scheme. Since, when interleaving, it is necessary to have two modules simultaneously selected the low order slot select must be disabled. This comparison of BMA01+ and BMCSS03- is the term which distinguishes between two adjcent boards. The result of this compare is disconnected via a DIP switch from the AND function which generates SEL-. The input to AND is pulled high thereby causing SEL- to be independent ofthe state of BMA01-.

BMA01 is swapped with BMA16 upon entering the module (This condition is restored to normal during refresh). The effect at the chip of swapping these addresses is to hold the least significant bit in one state until BMA01 goes active which selects the second 32k. Referring to Figure 4, it can be seen that every other physical location on each module will be accessed until the second 32k is requested. This condition will cause the location not accessible in the previous condition to be used. The distinction between module 1 and module 2 is determined by BMCEBL. The operation of BMCEBL will be explored in more detail when interleaved operation is explained. (Additional information on interleaved addressing may be obtained from 'Addressing Interleaved Memories', Ken Roy, PE-T-273.)

Timing Generation:

All clocks and timing signals for operating the storage devices are generated on the module. The timing generator is started by the occurrence of BMCPRCH- at the interface. Fig. 5 illustrates the logic employed. PRECH sets the flop which propagates a positive transition down the delay lines. Each delay line has a total delay of 200NS and is tapped at 40NS increments. A flop reset pulse is generated and is used to generate the second half of the cycle by causing a negative edge to be propagated. Combinational logic is used in conjunction with the delays available to generate the CENBL clock, strobe R/W and latch read data. The storage devices require that CENBL be a positive true signal with an amplitude of 12V. This level is achieved using an appropriate MOS driver. CENBL begins a chip cycle and executes the necessary preconditioning of the internal busses characteristic of dynamic RAM's. CENBL, in the 4K device, performs the function of PRECH as well as those performed by CENBL in the 1103 (Ref: Memory Module Description, J. E. Sheahan, July 25, 1973 p.3.). The WRITE signal, when active, causes the data presented as WDAT to be stored in a unique location defined by the chip addresses. The absence of WRITE causes the data previously stored or the data existing in the addressed location to be presented at the output pin as "SDAT". The data thus read from memory is applied to a latch where the data is retained until the next non- refresh cycle.

There are certain parameters unique to the P400 interface which permit performance enhancements on the memory module. These enhancements require that the timing on the module be altered slightly. This alteration may be accomplished in the field by changing a pair of header DIPS at locations and Location Nos. 44B and 46B on the module. Changing to P400 timing is mandatory if interleaved operation is

desired. Note that the P300 model timing will operate in the P400 but will not permit interleaving nor take full advantage of the processor timing characteristics.

The P400 memory interface is capable of tailoring, within limits, the buss and control timing depending on the 'BMCSEL' signals received from the memory. Compatible mode timing (i.e. all 32k models) is the default conditon. The P400 timing headers cuase BMCSELB- to go active, thereby affecting the change in interface timing from the processor. All refresh cycles are executed with compaitble mode timing.

OPERATIONS:

Write:

The module is written into when BMCWRB is low. This signal enables the write pulse from the timing generator and the write data driver to the array. BMCWRB also causes the read data tri-state buffers to enter the high impedance state in preparation for the write data. The data is buffered on to all modules via latches. The latches are kept open continuously on the P200, 300 and are closed after write data is stable on the P400. Data is presented at the storage device inputs through MOS drivers.

PRECH has been issued starting the timing generator which sends CENBL to the selected row of devices in preparation for the write. The timing for CENBL duration is longer for write cycles than for read cycles, in order to allow sufficient time for the data to become stable at the chips. When data is stable, the write pulse is issued, thus storing the data at the location defined by BMA16-BMA05. The sequence of events is essentially the same for the P200, 300 as for the P400 but with some timing differences as can be seen from the diagram in Figure 6.

Read:

A read from memory is executed when BMCWRB is not active. BMCPRCH goes active generating CENBL at the selected row of devices thus starting the chip access. The data appears at the device outputs and is buffered to the tri-state bus drivers through latches. Since when CENBL terminates, the storage device outputs go to a high impedance condition, the data is captured in the latches where it remains until the next non-refresh cycle on that module.

Interleaved Write:

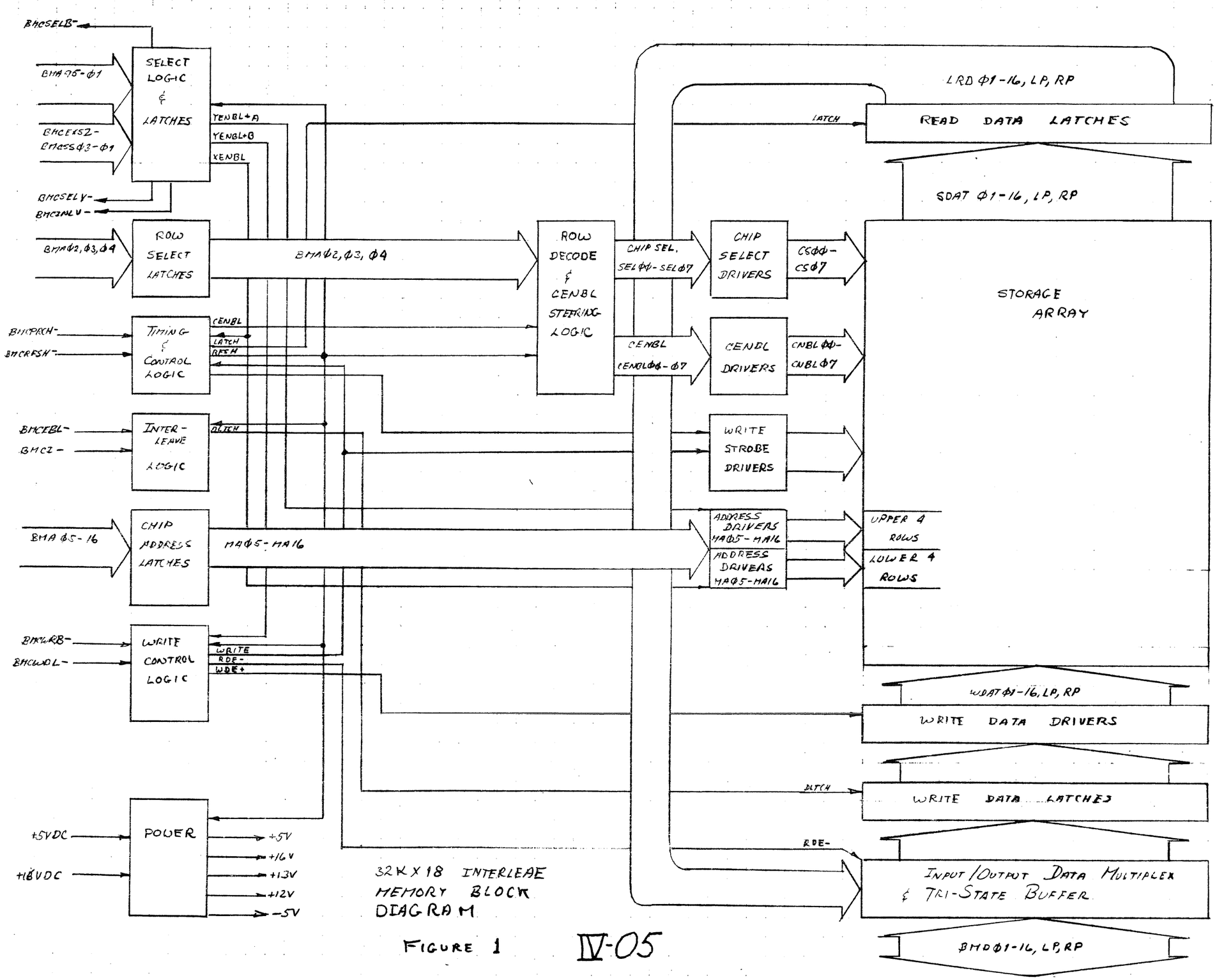
Interleaved operation is achieved in the P400 processor only by providing the module with the appropriate timing headers as previously mentioned and by setting the DIP switches at module Switch Location 28C as indicated in Table 1. Interleave operation utilizes special logic for address and data control. Address has been discussed previously and will not be reiterated here. The data manipulation logic is illustrated in Figure 7.

Data is directed to or from individual units of an interleaved pair by means of BMCEBL-. Operation is most clearly illustrated by a step by step description of the cycle. Reference to the LBD's is helpful but not mandatory.

The write cycle will be treated first. An interleaved write is to be performed on a pair of modules located in the low order slots (slot #16 and #17). The module in #17 will be referred to as module 1 and the unit in #16 as Module 2. BMCEBL- is initially a high and is XOR'd with BMCSS03-. BMCSS03- will be high for module 1 and low for module 2, thus INLVBSEL+ on module 1 will be low and high on module 2. When the data for module 1 is stable, BMCWDL+ will become high and, since DLCHNBL+ is high, DLTCH+ will become high. The signal, DLCHFB-, serves to latch this condition on module 1. Since DLCHNBL+ is low on module 2, no change in DLTCH+ has occurred. At this time, the data on the bus is permitted to become valid for module 2. After data stability is guaranteed, BMCEBL- changes state thus allowing DLTCH+ on module 2 to become active. At this time, each module has its respective data latched and the write cycle is executed in a normal manner. It should be noted that BMCI+ is high insuring that the write pulse will occur on both modules regardless of the state of BMCEBL-. When the cycle is complete, the transition of BMCWDL+ to a low causes the data latch circuitry to reset on both modules.

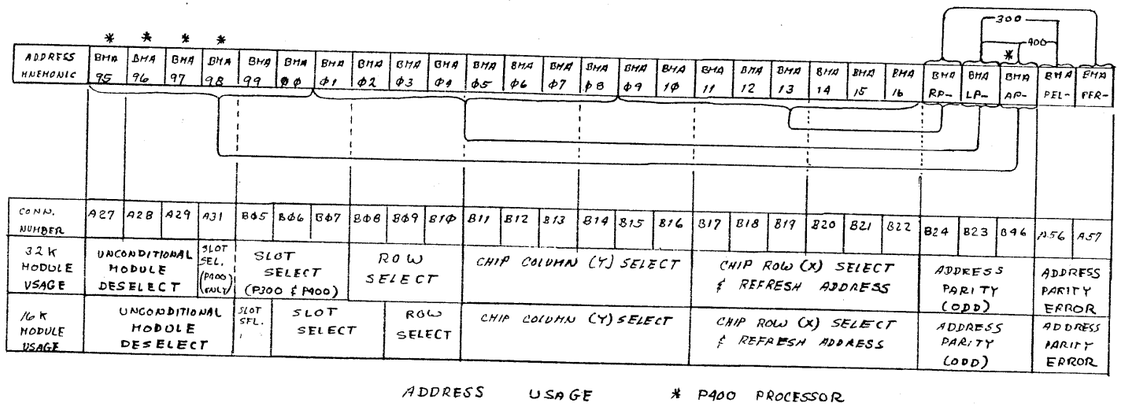
Interleaved Read:

Since both modules of an interleaved pair are selected when a read is requested, a normal read cycle as previously discussed is executed on both modules. As in the interleaved write cycle, BMCEBL- determines which board is active. Assume BMCEBL- is high and module 1 has BMCSS03- high and low on module 2. INLVBSEL+ will be low on module 1 thus causing RDE- to be low permitting module 1's data to be on the bus. When data available occurs for the first word BMCEBL- changes state causing RDE- to go high on module 1 and low on module 2 allowing the data already accessed on board 2 to be transmitted to the processor.

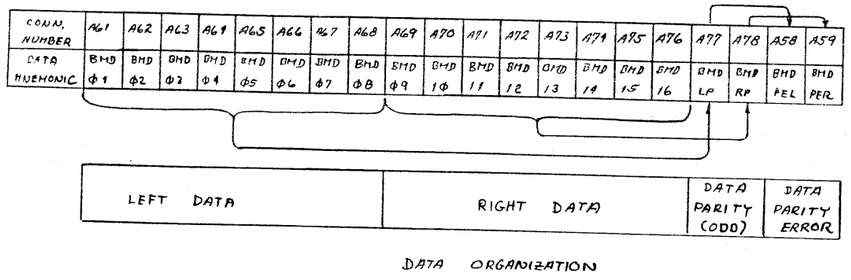


32K X 18 INTERLEAE MEMORY BLOCK DIAGRAM

FIGURE 1



ADDRESS USAGE * P400 PROCESSOR



DATA ORGANIZATION

FIGURE 2

ADDRESS & DATA ORGANIZATION and USAGE

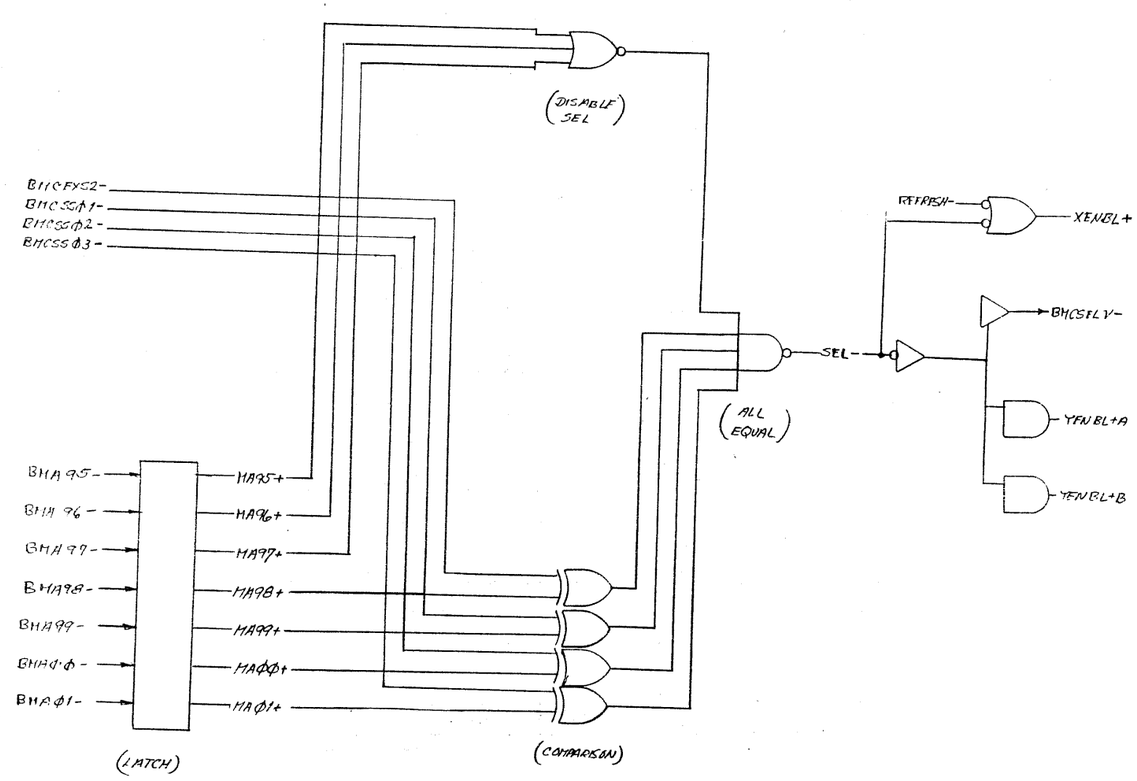


Fig. 3

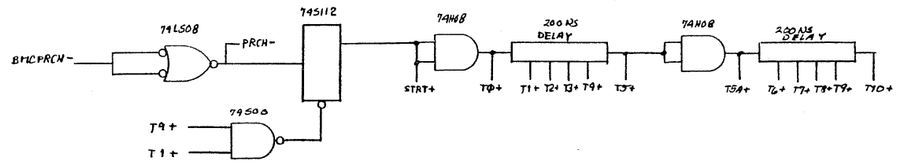
MODULE SELECTION LOGIC

CPU ADDRESS TO MODULE	ADDRESS TO CHIPS	PHYSICAL MODULE LOCATION	
		MODULE 1	MODULE 2
000000	0000	0000	
000001	0000		0000
000002	0002	0002	
000003	0002		0002
⋮			
077776	7776	7776	
077777	7776		7776
100000	0001	0001	
100001	0001		0001
100002	0003	0003	
100003	0003		0003

Note: the ROW ADDRESSES are unchanged

Figure 4

MODULE LOCATION	CPU ADD IN MODULE 1	CPU ADD IN MODULE 2
000000	000000	000001
000001	100000	100001
000002	000002	000003
000003	100002	100003
⋮		
077776	077776	077777



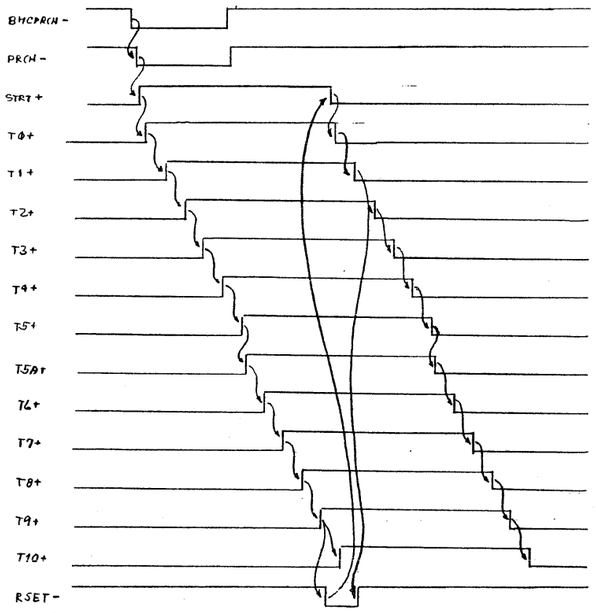
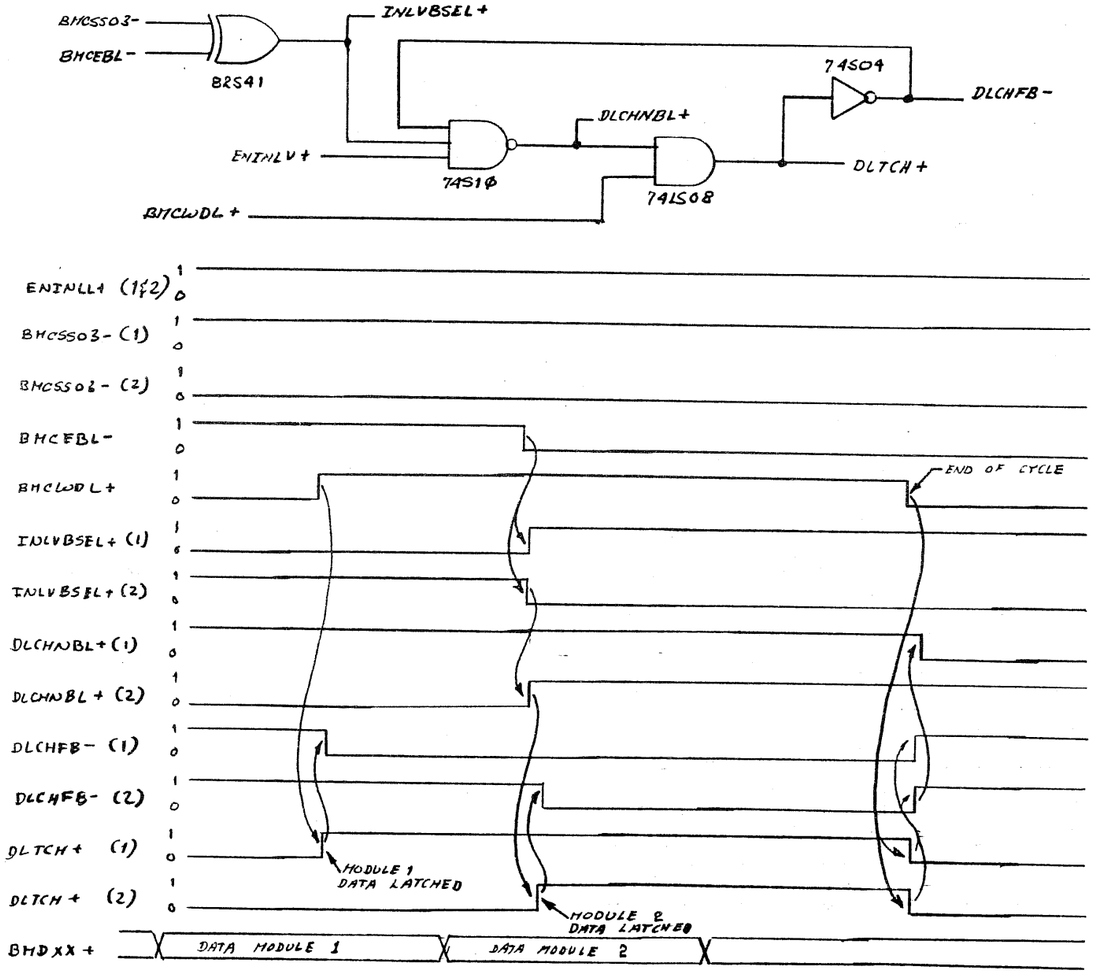


FIGURE 5

TIMING GENERATOR & SEQUENCE OF OPERATION

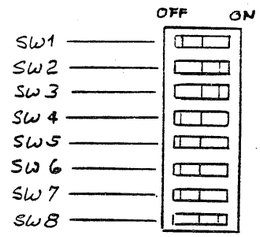


DATA LATCHING CIRCUIT FOR INTERLEAVE WRITE

FIGURE 7

TABLE 1

SWITCH SETTINGS



(ON = CLOSED)

BOARD LOCATION 28C

	UP TO 8 BDS 32K ea.			UP TO 16 BDS 32K ea.			
SWITCH	P300	P400	P400I	P300	P400	P400I	FUNCTION
1	OFF	ON	ON	OFF	ON	ON	DISABLES WRITE ON APEL-
2	OFF	ON	ON	OFF	ON	ON	DISABLES WRITE ON APER-
3	X	X	X	X	X	X	NOT USED
4	X	X	X	X	X	X	NOT USED
5	ON	ON	OFF	ON	ON	OFF	INTERLEAVE ACTIVE/NOT ACTIVE
6	ON	ON	OFF	ON	ON	OFF	INTERLEAVE ACTIVE/NOT ACTIVE
7	OFF	OFF	OFF	ON	ON	ON	MAX. NO. BDS IN BKPLN.
8	OFF	ON	ON	OFF	ON	ON	HIGH ORDER PARITY CHECK

448	W171	W174	W174	W171	W174	W174
468	W172	W173	W173	W172	W173	W173
HDR LOC.	ASSY. NO.			ASSY. NO.		

LTR	DATE	REVISION	DR.	CK.
A	7-9-76	RELEASED	[illegible]	[illegible]
B	8-25-76	PER ECR 1850	[illegible]	[illegible]
C	9-2-76	PER ECR 1878	[illegible]	[illegible]
D	9-3-76	PER ECR 1883-A	[illegible]	[illegible]
E	10/5/76	PER ECR 1910 A	[illegible]	[illegible]
F	10/18/76	PER ECR 1929	[illegible]	[illegible]

SHEET 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	A	A	A	A	A	A	A	A	A	A					
	B	B	B	-	-	-	-	-	-	-	-					
	C	C	-	C	-	-	-	-	-	-	-					
	D	D	C	-	-	-	-	-	-	-	-					
	E	F	D	C	-	-	-	-	-	-	-	B				
	F											C				

REVISION LEVEL

MATERIAL	DWN 7-7-76 J.F. TRAVALINI	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK 7/7/76 J.C. McNamee	REVISION STATUS SHEET 12K x 18 INTERLEAVED MOS MEMORY LV
	ENG. [illegible]	
	APPRD [illegible]	
	USED ON 1232 BOARD	SCALE
	NEXT ASSY 1232-BA: I	SHEET 1 OF 11
		SIZE C DWG. NO. LBD2623 REV. F

IV-08-A

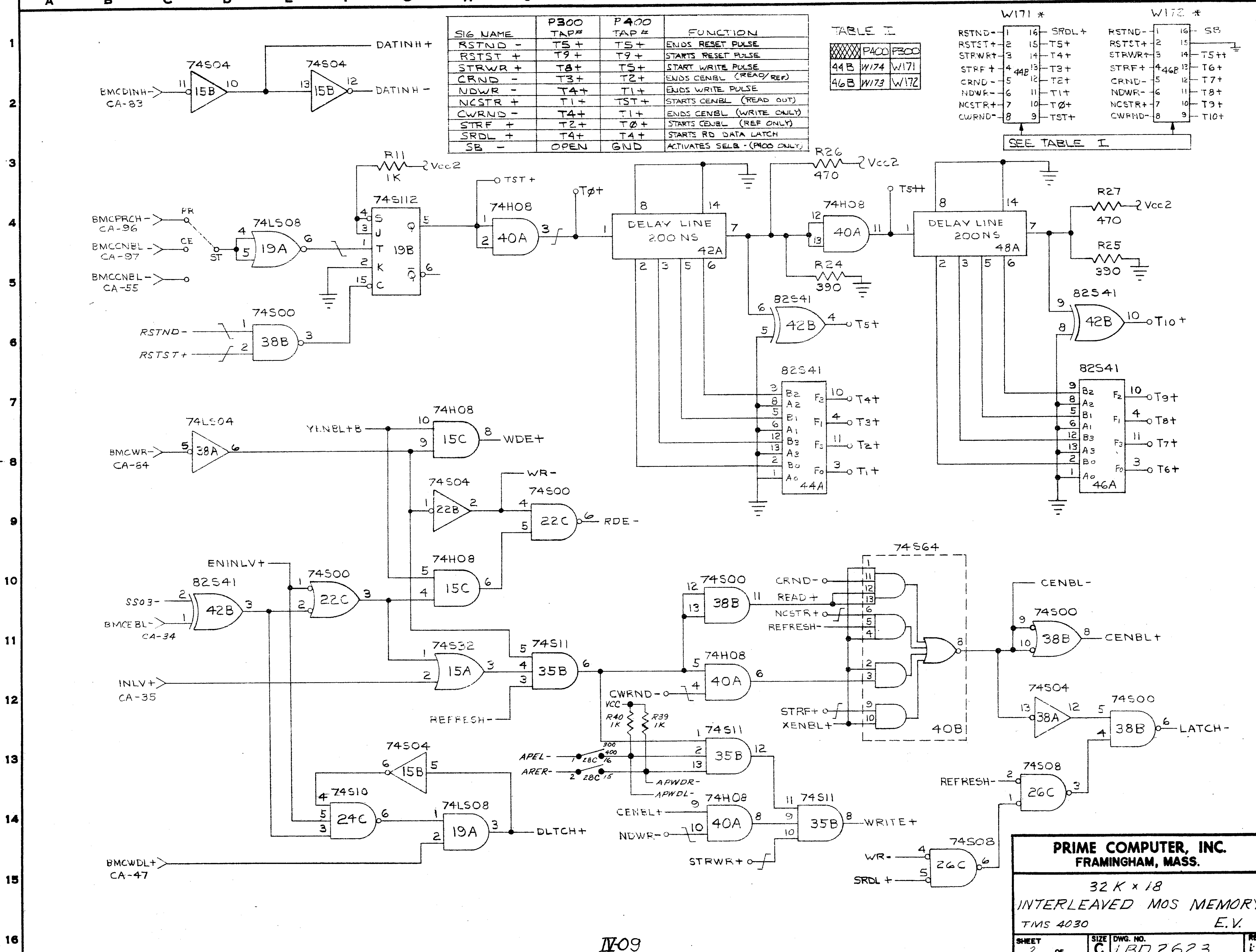
LBD2623

PRIME COMPUTER, INC.

SIG NAME	P300 TAP#	P400 TAP #	FUNCTION
RSTND -	T5 +	T5 +	ENDS RESET PULSE
RSTST +	T9 +	T9 +	STARTS RESET PULSE
STRWR +	T8+	T5+	START WRITE PULSE
CRND -	T3+	T2+	ENDS CENBL (READ/REF)
NDWR -	T4+	T1+	ENDS WRITE PULSE
NCSTR +	T1+	TST+	STARTS CENBL (READ OUT)
CWRND -	T4+	T1+	ENDS CENBL (WRITE ONLY)
STRF +	T2+	TØ+	STARTS CENBL (REF ONLY)
SRDL +	T4+	T4 +	STARTS RD DATA LATCH
SB -	OPEN	GND	ACTIVATES SELB - (P400 ONLY)

TABLE I

	P400	P300
44B	W174	W171
46B	W173	W172

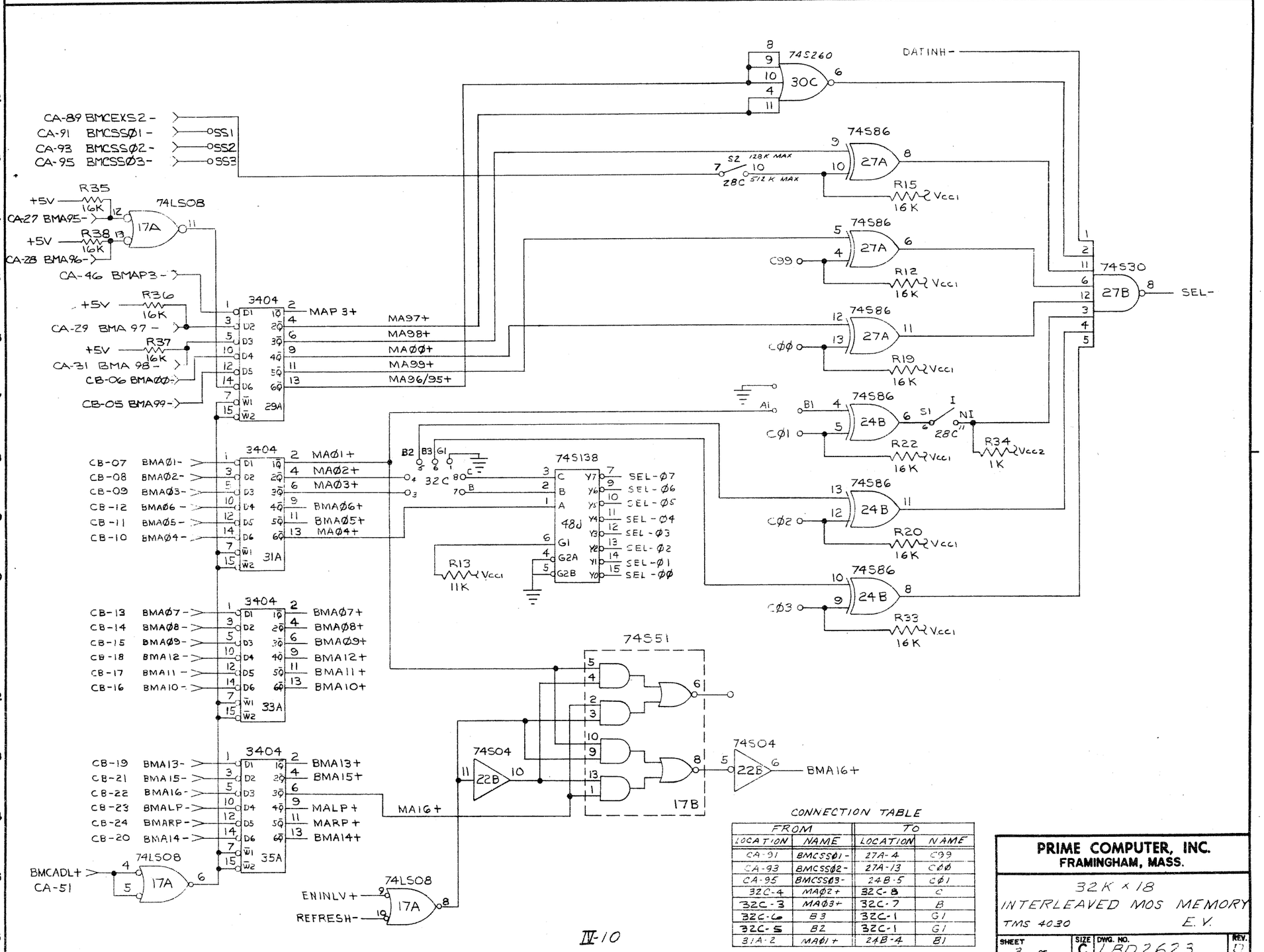


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

32 K × 18
INTERLEAVED MOS MEMORY
TMS 4030 E.V.

SHEET 2 OF | SIZE C | DWG. NO. LBD 2623 | REV.

PDF-003



CONNECTION TABLE

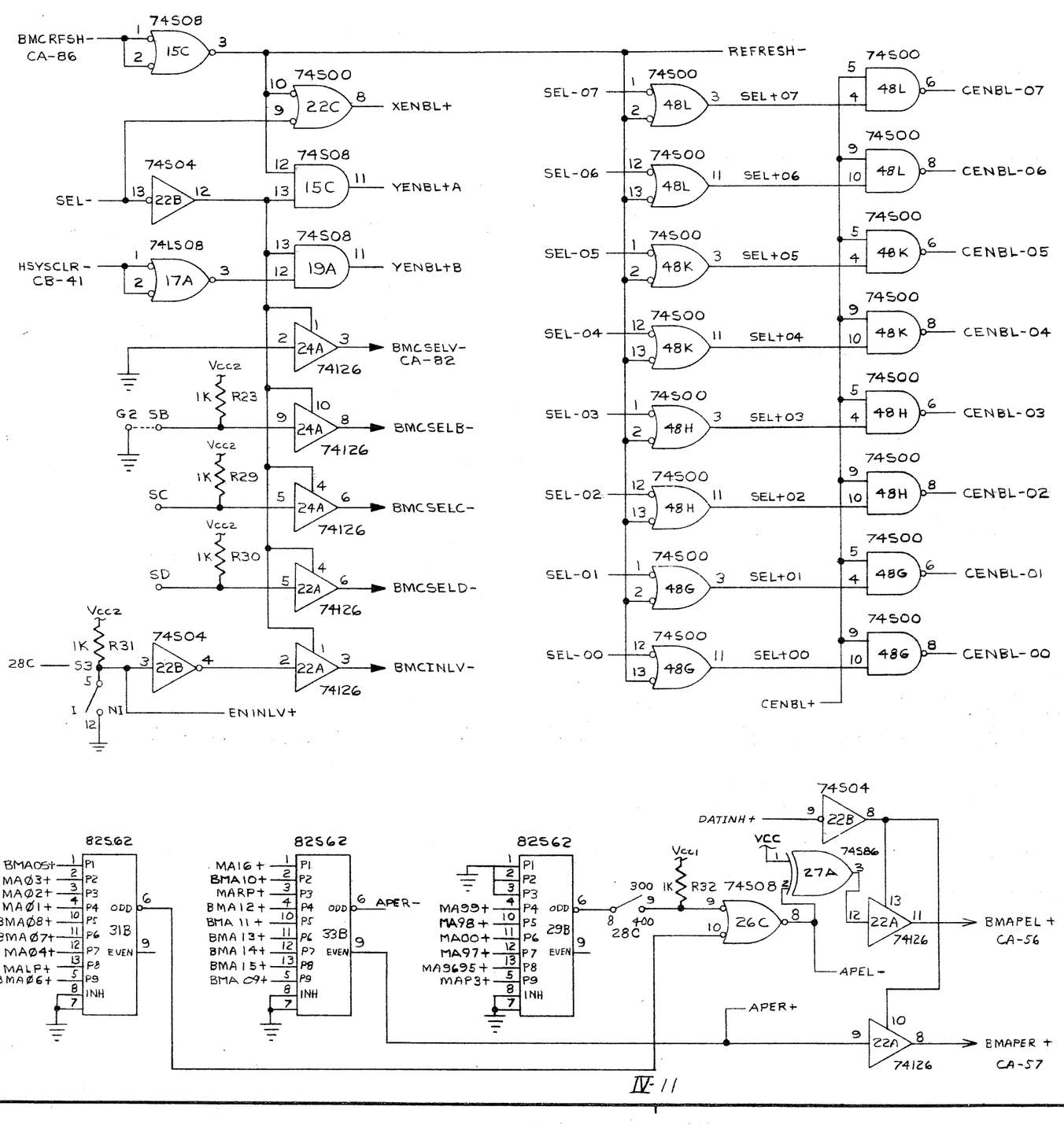
FROM		TO	
LOCATION	NAME	LOCATION	NAME
CA-91	BMCSSØ1-	27A-4	C99
CA-93	BMCSSØ2-	27A-13	CØØ
CA-95	BMCSSØ3-	24B-5	CØ1
32C-4	MAØ2+	32C-8	C
32C-3	MAØ3+	32C-7	B
32C-6	B3	32C-1	G1
32C-5	B2	32C-1	G1
31A-2	MAØ1+	24B-4	B1

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

32K x 18
INTERLEAVED MOS MEMORY
TMS 4030 E.V.

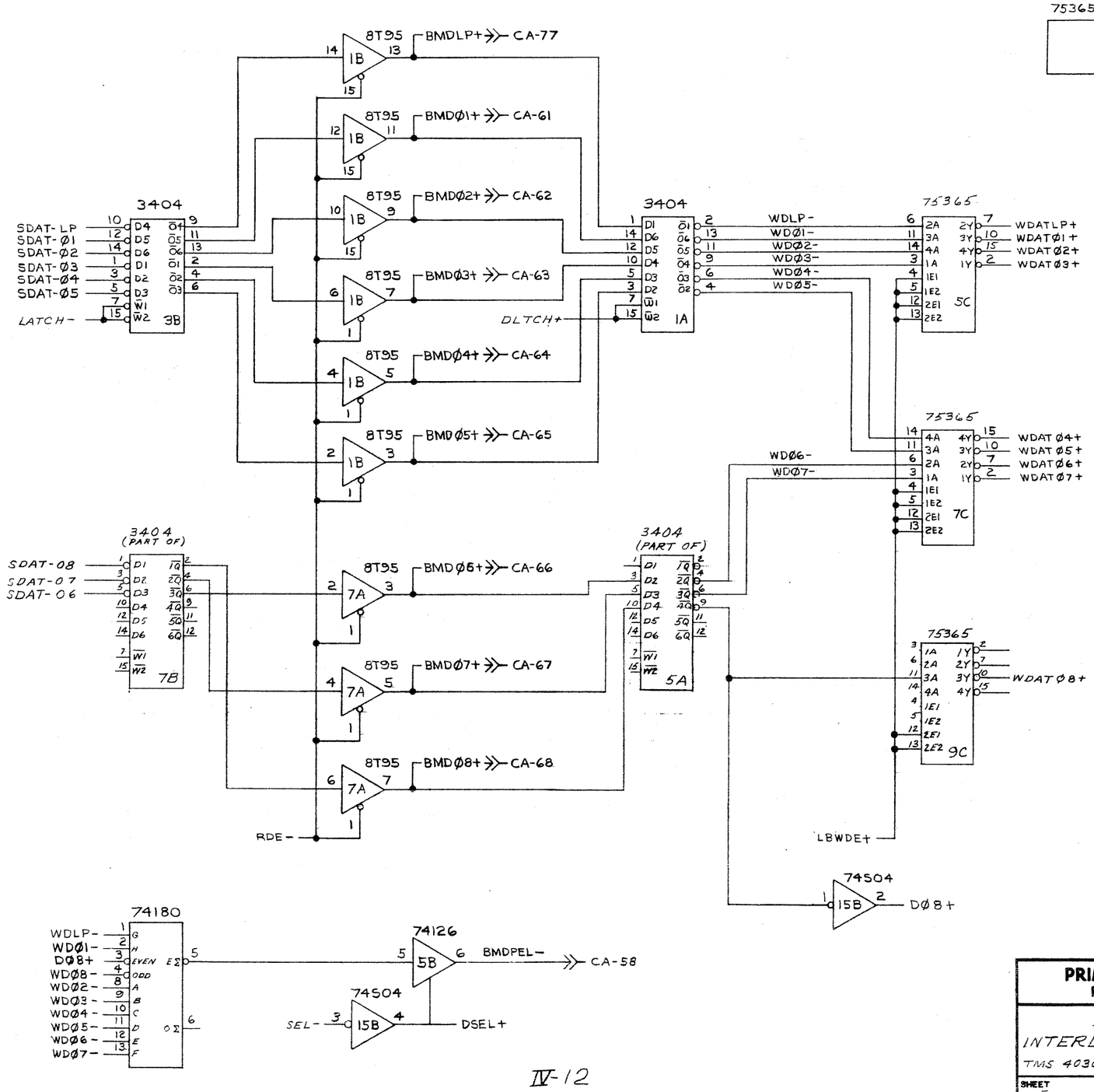
SHEET	SIZE	DWG. NO.	REV.
3 OF	C	LBD2623	D

PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
32K x 18 INTERLEAVED MOS MEMORY	
TMS 4030	E.V.
SHEET 4 OF	SIZE C / DWG. NO. LBD2623 / REV. C

PDF-003



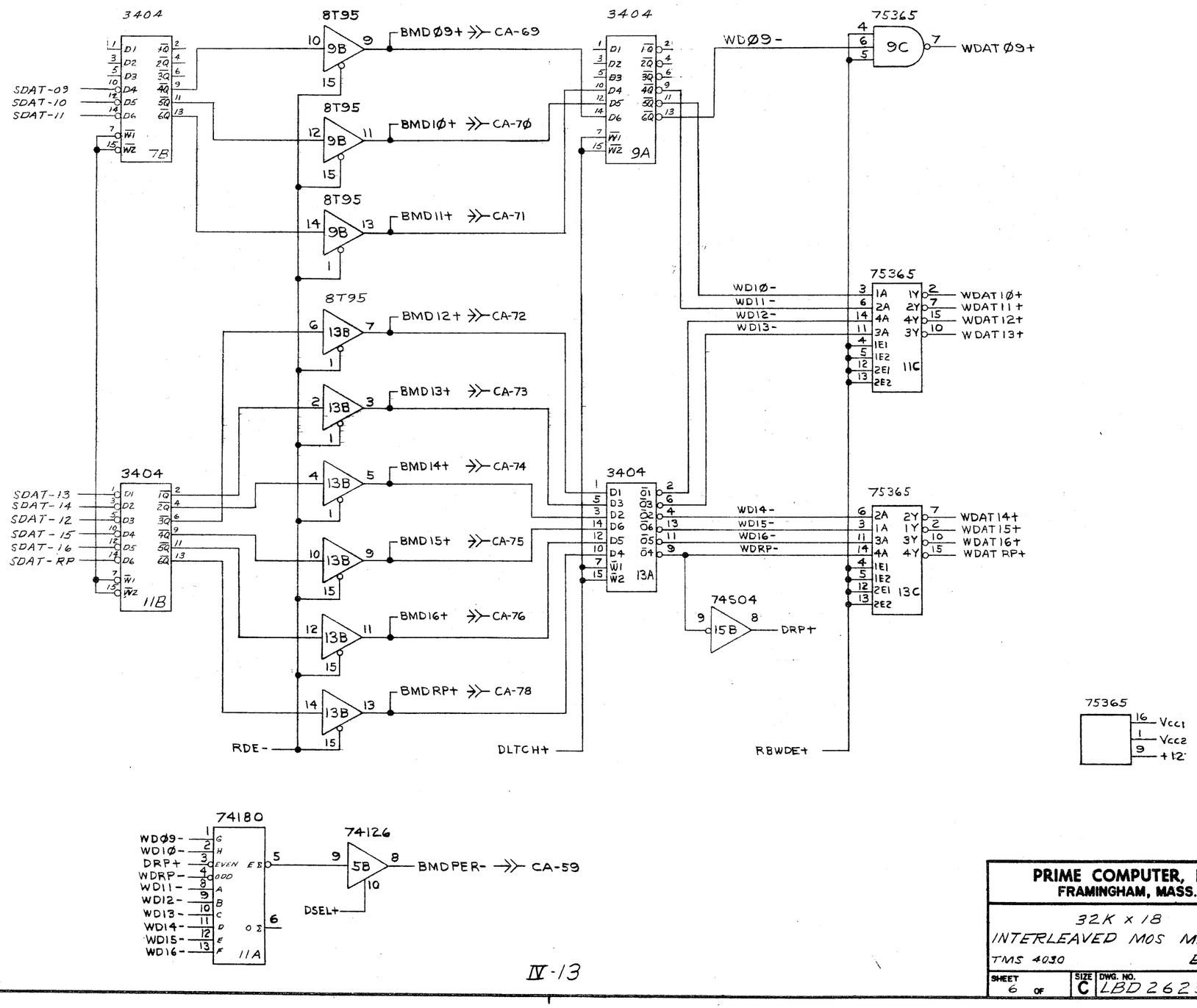
IV-12

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

32K x 18
INTERLEAVED MOS MEMORY
TMS 4030 E.V.

SHEET	SIZE	DWG. NO.	REV.
5 OF	C	LBD2623	A

PDF-003

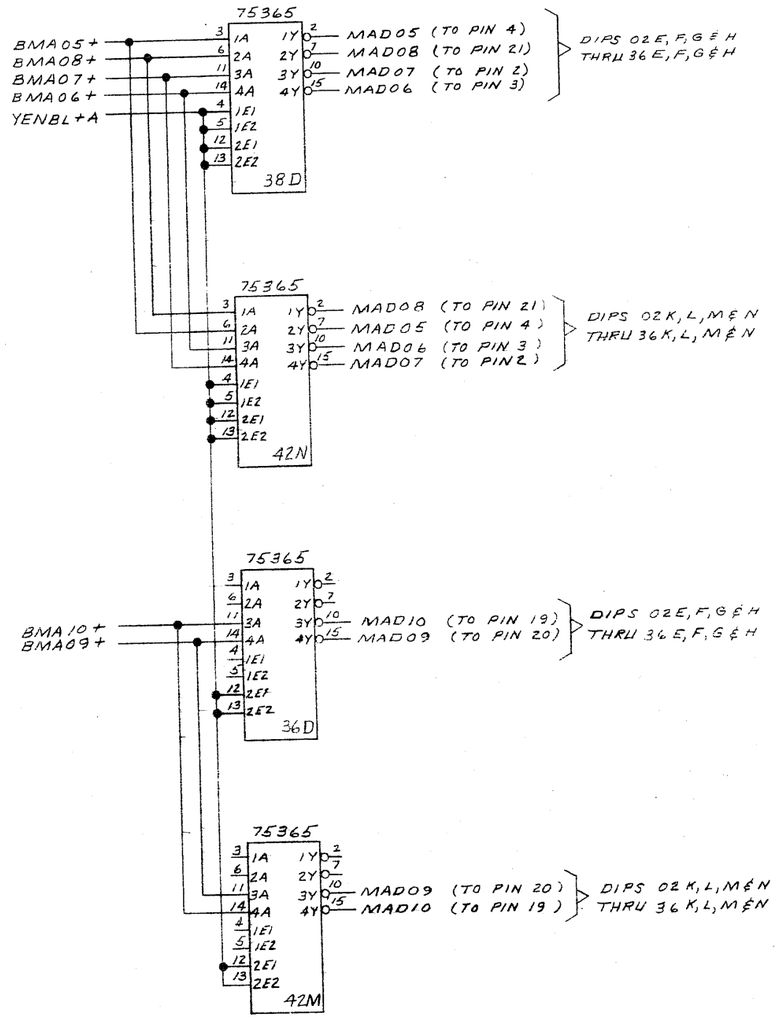


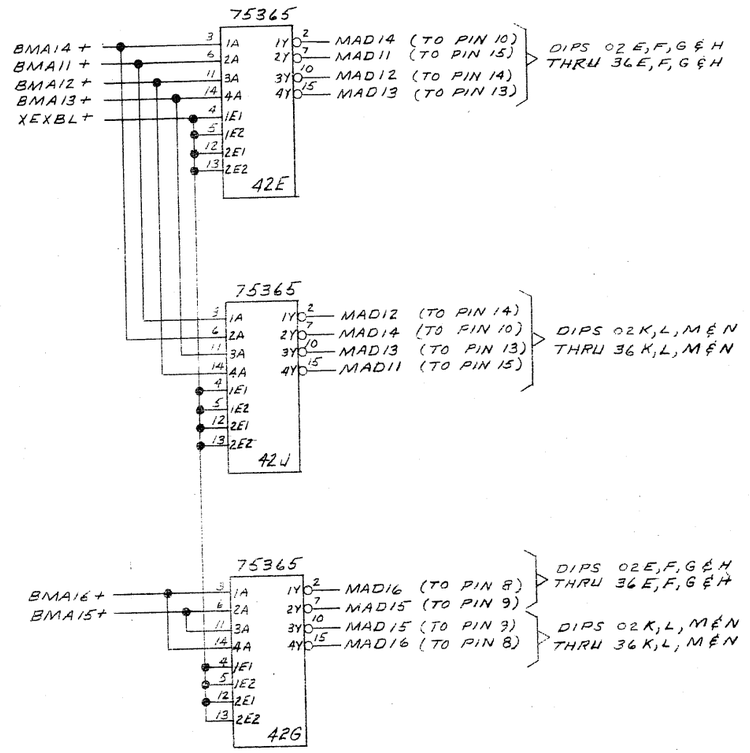
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

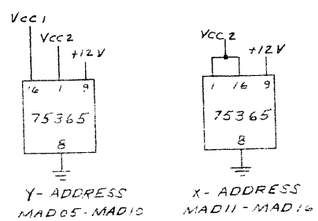
32K x 18
INTERLEAVED MOS MEMORY
TMS 4030 E.V.

SHEET 6 OF | SIZE C | DWG. NO. LBD2623 | REV. A

PDF-003





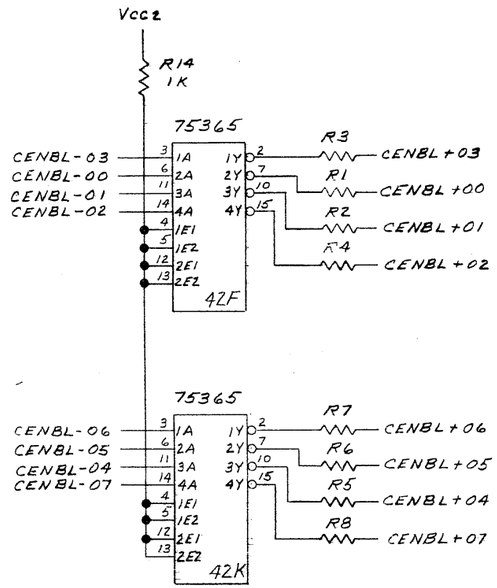


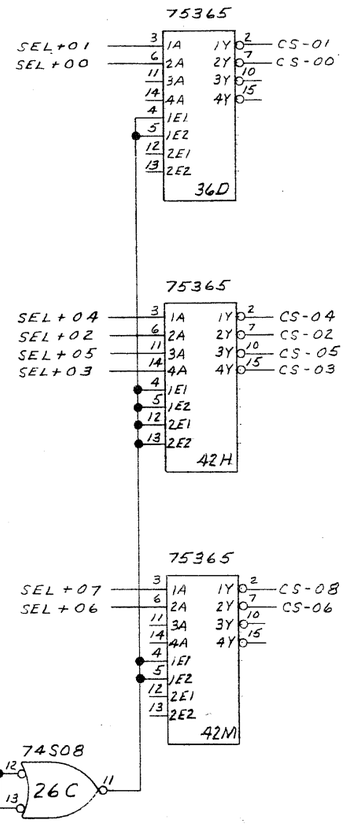
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

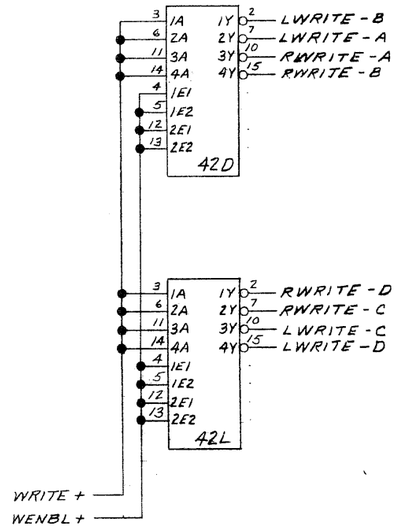
32K x 18
INTERLEAVED MOS MEMORY
TMS 4030 E.V.

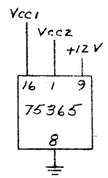
SHEET 7 OF | SIZE C | DWG. NO. LBD2623 | REV. A

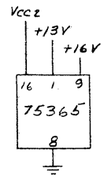
P01-003











PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

32K x 18
INTERLEAVED MOS MEMORY
TMS 4030 E.V.

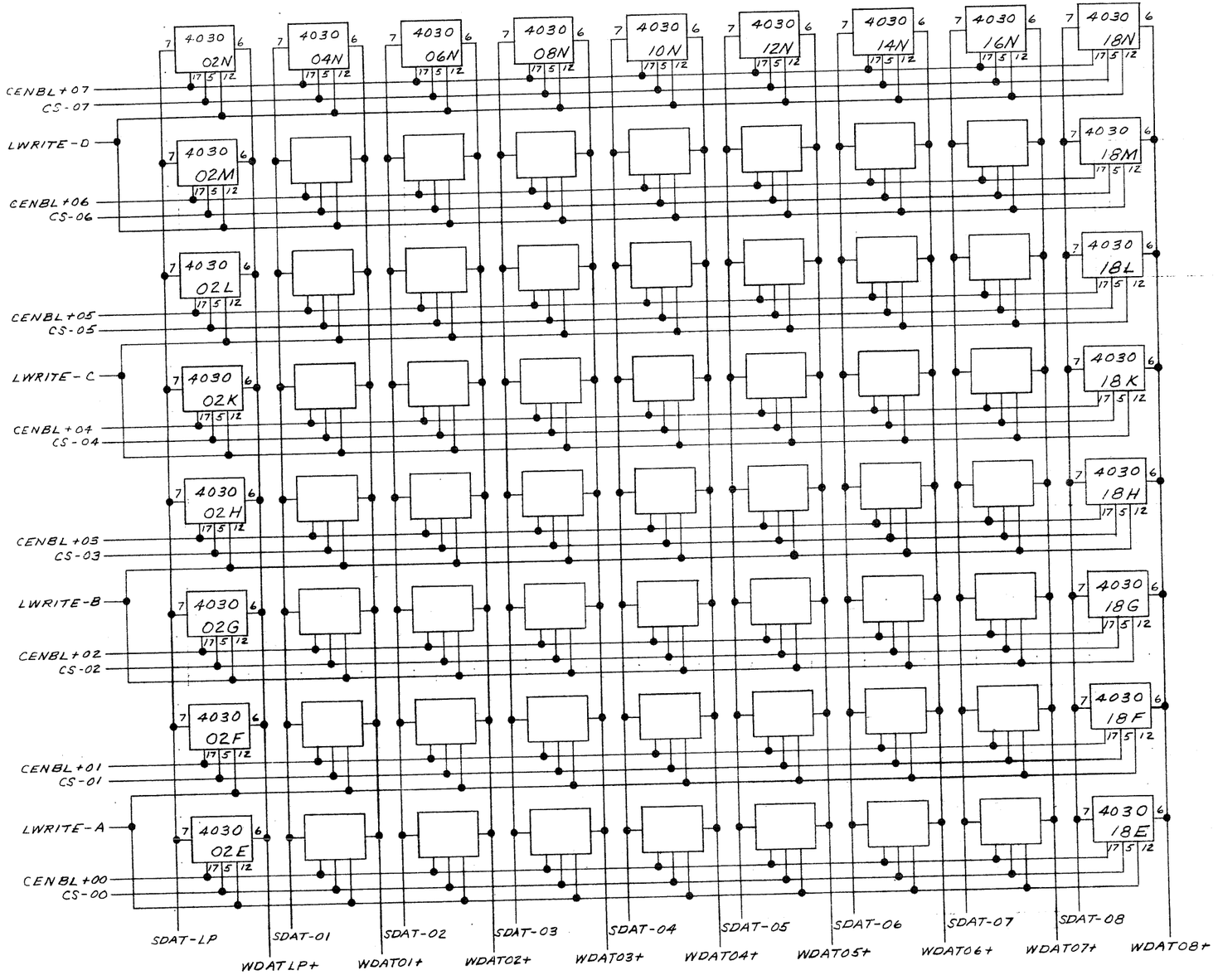
SHEET	SIZE	DWG. NO.	REV.
8 OF	C	LBD 2623	A

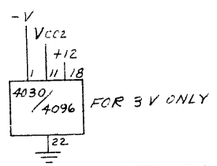
PDF-003

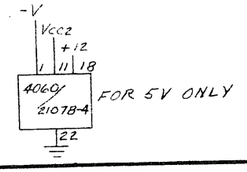
PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16





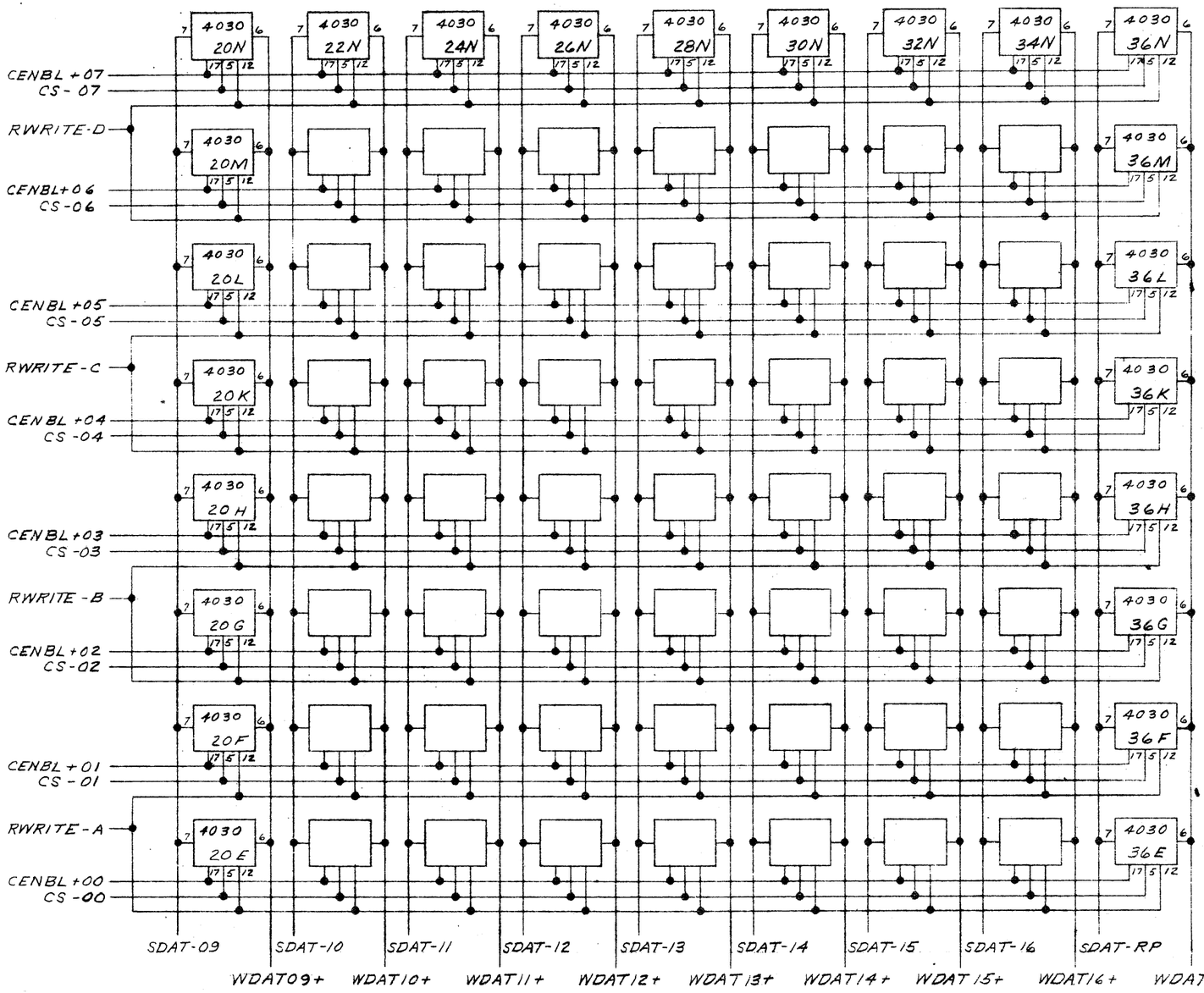


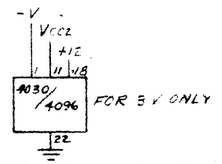
PDF-003

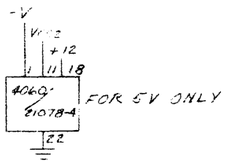
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

32K x 18
INTERLEAVED MOS MEMORY
TMS 4030 E.V.

SHEET 9 OF | SIZE C | DWG. NO. LBD2623 | REV. A







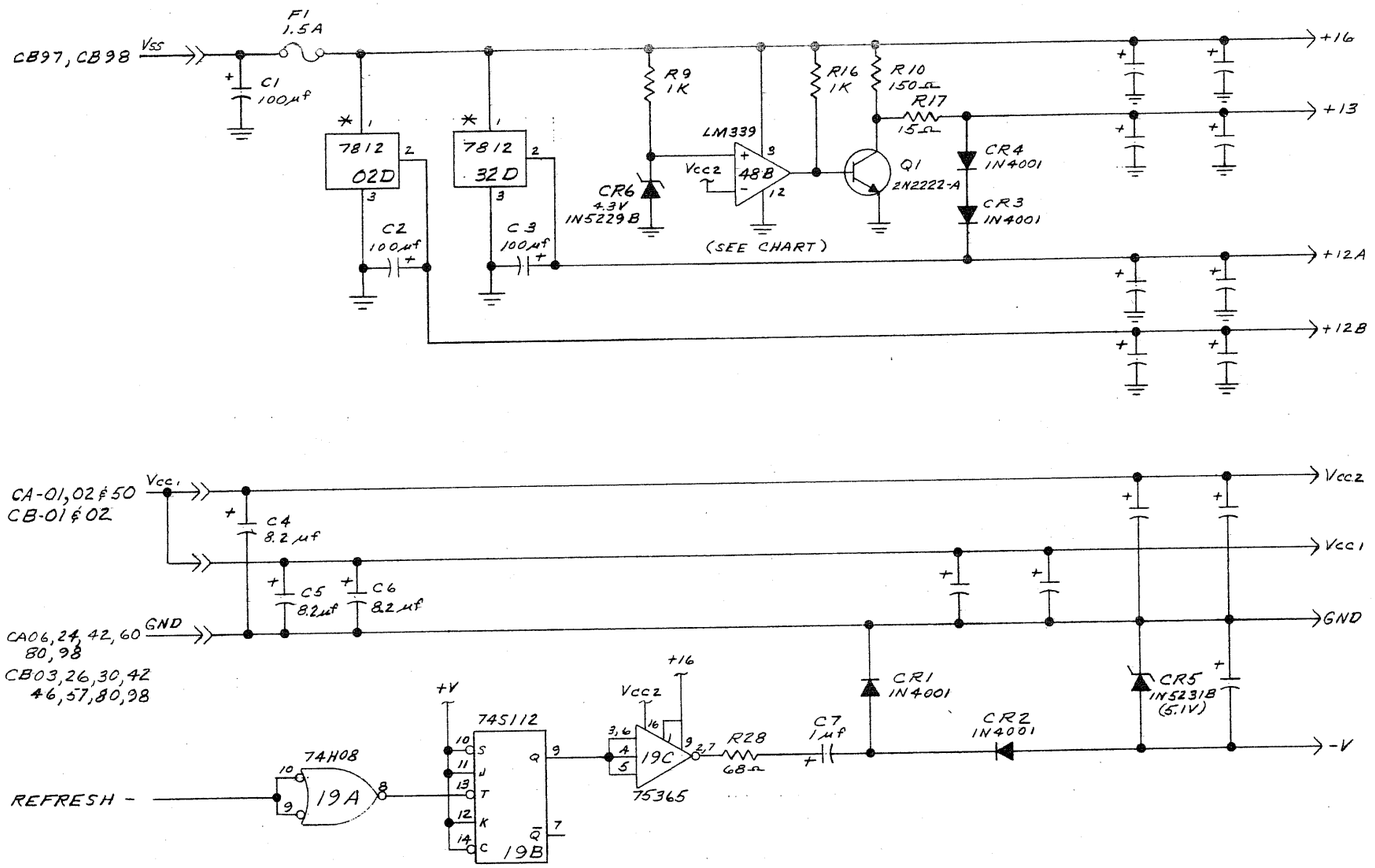
IV-17

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

32K x 18
INTERLEAVED MOS MEMORY
TMS 4030 E.V.

SHEET	SIZE	DWG. NO.	REV.
10 OF	C	LBD2623	A

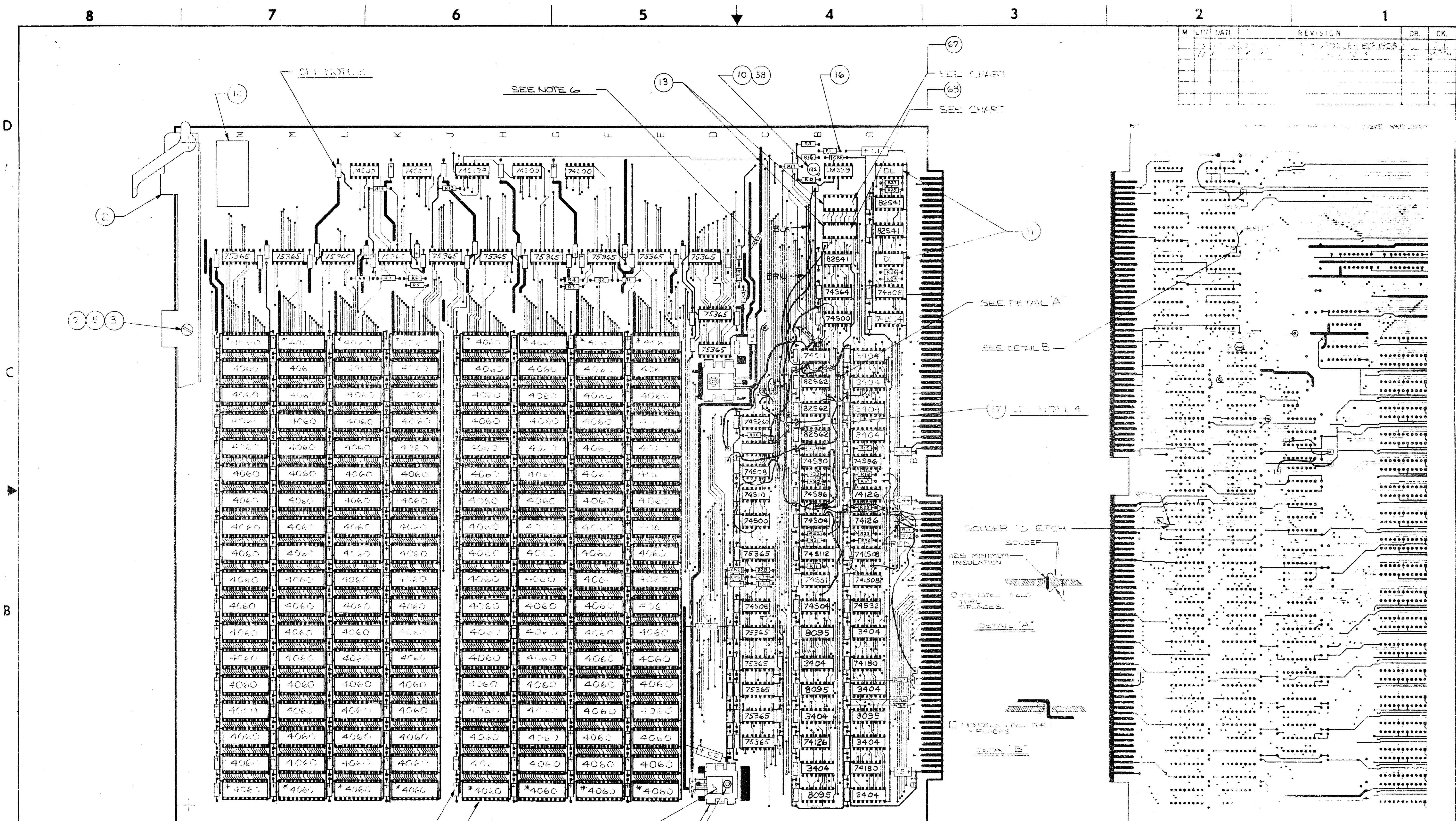
POF-003



NOTES:
1. * = MOUNT ON HEAT SINK
2. CAPACITORS WITH NO VALUE DESIGNATION ARE CAP. TANT 1.0μf, 20 V

PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
32K x 18 INTERLEAVED MOS MEMORY	
TMS 4030	E.V.
SHEET 11 OF 11	SIZE C · DWG. NO. LBD2623 · REV. C

PDF-003



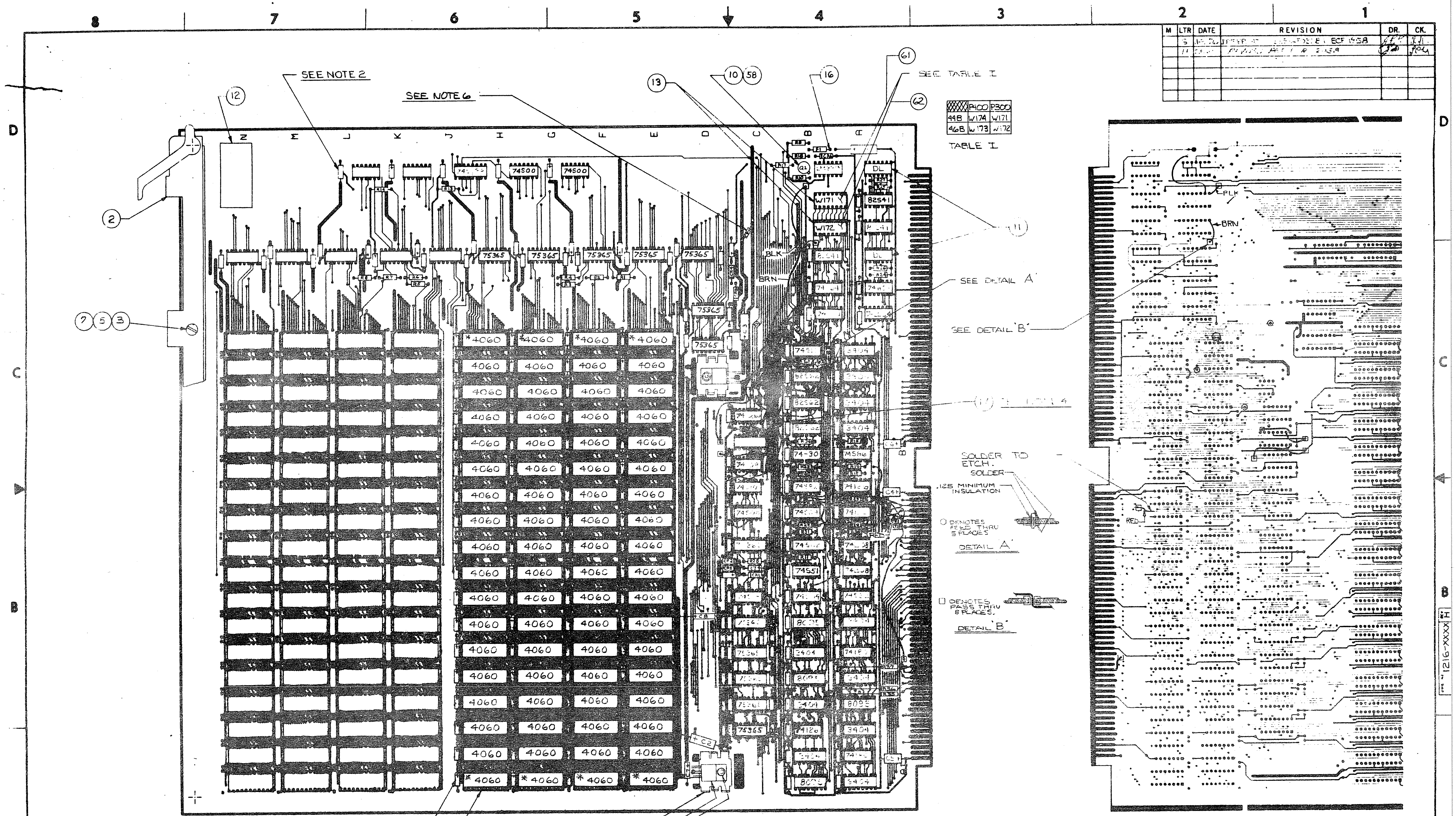
NOTES:

1. DISCRETE COMPONENTS MARKED + [illegible]
   (CAP TANT 1.0 uf 35V 15 REQUIRED.)
2. UNMARKED DISCRETE COMPONENTS [illegible]
   (CAP GLASS .01 uf 35V 82 REQUIRED.)
3. APPLY ITEM 9 (THERMAL [illegible] BETWEEN [illegible]
4. ITEM 17 TO BE INSTALLED AFTER WAVE [illegible]
5. ALL JUMPERS TO BE YELLOW EXCEPT [illegible]
6. INSTALL ITEM 69 ON LEADS R35, R36, R37 [illegible]
7. WHEN USED WITH A- DBS DELETE: 358-1 TO 358-[illegible] / 358-[illegible]
   ADD: 358-2 TO [illegible] / 358-[illegible]

IV-19

VARIATION CHART			JUMPER	DIP
-XXX	DESCRIPTION	VARIATION	44B	46B
-A ASY	32K X 16 @ [illegible]	OMIT DIPS INDICATED WITH ASTERISK	W171	W172
-B ASY	32K X 16 @ 750 NS	AS [illegible] P300	W171	W172
DBS	32K X 16 @ 750 NS	AS SHOWN P400	W171	W172

FOR ETCH CUTS SEE ECR 2658-001



FOR ETCH CUTS SEE ECB 2658-001

SEE NOTE 1

TYP 144 PLACES (14)

SEE NOTE 3 (9) (49)

VARIATION CHART		
-XXXX	DESCRIPTION	VARIATION
-A65Y	16K X16 @ 1µS	OMIT DIPS INDICATED WITH ASTERISK
-B85Y	16K X18 @ 750NS	AS SHOWN

NOTES:

1. DISCRETE COMPONENTS MARKED '+' ARE ITEM 18. (CAP TANT 1.0uf, 35V, 86 REQUIRED.)
2. UNMARKED DISCRETE COMPONENTS ARE ITEM 21 (CAP GLASS .01 uf 25V. 81 REQUIRED.)
3. APPLY ITEM 9 (THERMAL COMPOUND) BETWEEN ITEMS 49 & 9.
4. ITEM 17 TO BE INSTALLED AFTER WAVE SOLDERING.
5. ALL JUMPERS TO BE YELLOW EXCEPT WHERE NOTED
6. INSTALL ITEM 69 ON LEADS R35-R36-R37-R38 & [illegible]

IV-20

MATERIAL	DWN	PRIME COMPUTER, INC. FRAMINGHAM, MASS
UNLESS OTHERWISE SPECIFIED -REMOVE ALL BURRS AND SHARP EDGES -DIMENSIONS ARE IN INCHES -TOLERANCES	CHK / ENG / APPRD	MEMORY [illegible] INTERLEAVED 16K - 5V 4L
		SCALE 1/1 SIZE D DWG NO [illegible] -XX REV H

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. A. Napolitano
CHK. H. Logan 6/23/76
ENG. K.R.R. 6/23/76
APPRD. S.A. Lemieux 7/13/76

STANDARD COST _____ DATE _____

TITLE: 32K-SV 4L
MEMORY BD ASSY
INTERLEAVED
-D85 P400
-A65Y = 32K X16 @ 1 µs
-B85Y = 32K X18 @ 750 NS

BOM 1232-XXXX REV. H
NHA: SHT. 1 OF 4

REV.	ECN	CK	REV.	ECN	CK
A	RELEASED	KRR	E	1910-A	KRR
B	1852 1867	K.K	F	1929	KRR
C	1878	K.K	G	1958	K.K
D	1885-A	K.K	H	2038	KRR

ITEM	SIZE	PART NUMBER	QUANTITY A65Y	B85Y	-D85	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1		PCB2565-001	1	1	1					P.C. BOARD 32 K I. MEMORY	
2	C	MEC 0587	1	1	1					STIFFENER ASSY, P.C. BD.	
3		MEC0303-005	5	5	5					SCREW, BD. HD. #4-40 X 5/16 LG	
4		MEC0303-006	2	2	2					SCREW, BD. HD #4-40 X 3/8 LG	
5		MEC 0356	5	5	5					WASHER, FIBER #4	
6		MEC 0353	2	2	2					WASHER, FLAT, METAL #4	
7		MEC0388-002	7	7	7					NUT, SELF LOCKING #4-40	
8		MEC1836-001	2	2	2					HEAT SINK	
9		MEC 8068-001	A/R	A/R	A/R					THERMAL JOINT COMPOUND	
10		MEC8260-003	1	1	1					TRANSISTOR MOUNTING PAD TO18	
11		MEC1546-001	2	2	2					DELAY LINE, 200 NS	
12	A	MEC 0292	1	1	1					LABEL, SERIAL & MODEL NO.	
13		CON0650-001	2	2	2					SOCKET, 16 PIN, DIP	
14		CON0650-003	144	144	144					SOCKET, 22 PIN, DIP	
15		FUS0254-002	1	1	1					FUSE, SUB-MINIATURE 1.5A (F1)	
16		CON1693-001	2	2	2					CONN JACK P.C. BOARD	
17		SWT0601-002	1	1	1					DIP SWITCH, DUAL INLINE	A
18		CAP0552-529	158	158	158					CAP TANT 1.0 uF 35V	
19		CAP0130-407	6	6	6					CAP. TANT. 8.2 uf 20V (C4,5,6,7,8,9)	A
20		CAP0130-420	3	3	3					CAP. TANT. 100 uf 25V (C1,2,3)	
21		CAP0546-001	82	82	82					CAP, GLASS 50V +80-20% .01 uf	A
22		D101544-001	4	4	4					DIODE, L.C. RECT 1N4001 (CR1-CR4)	

PRF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. A. Napolitano
CHK.
ENG.
APPRD.

STANDARD COST _____ DATE _____

TITLE: 32K-SV 4L
MEMORY BD ASSY
INTERLEAVED
-D85 P400
-A65Y = 32K X16 @ 1 µs
-B85Y = 32K X18 @ 750 NS

BOM 1232-XXXX REV. H
NHA: SHT. 2 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY A65Y	B85Y	-D85	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
23		D101759-211	1	1	1					DIODE, ZENER ±5% 1N5231B (CR5)	
24		D101759-209	1	1	1					DIODE, ZENER ±5% 1N5229B (CR6)	
25		RES1582-150	1	1	1					RES, CARBON 15 Ω 1/4W (R17)	
26		RES1582-390	8	8	8					RES, CARBON 39 Ω 1/4W (R1-R8)	
27		RES1582-680	1	1	1					RES, CARBON 68 Ω 1/4W (R28)	
28		RES1582-151	1	1	1					RES, CARBON 150 Ω 1/4W (R10)	
29		RES1582-391	2	2	2					RES, CARBON 390 Ω 1/4W (R24,25)	
30		RES1582-471	2	2	2					RES, CARBON 470 Ω 1/4W (R26,27)	
31		RES1582-102	13	13	13					RES, CARBON 1K Ω 1/4W (R9,11,14,16,23,29,30,31,38,39,40)	A
32		RES1582-163	10	10	10					RES. CARBON 16K Ω 1/4W (R12,15,18,20,22,33,35,36,37,38)	A
33		RES1582-303	2	2	2					RES, CARBON 30K Ω 1/4W (R19,21)	
34		ICD0023	1	1	1					74H08	
35		ICD2599	1	1	1					74S30	
36		ICD0059	3	3	3					74126	
37		ICD0070	1	1	1					74S64	
38		ICD0072	1	1	1					74S112	
39		ICD0079	3	3	3					82S62	
40		ICD0085	6	6	6					74S00	
41		ICD0086	2	2	2					74S04	
42		ICD0088	1	1	1					74S10	
43		ICD0089	1	1	1					74S11	
44		ICD0095	1	1	1					74S138	

PRF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. A. Napolitano
CHK.
ENG.
APPRD.

STANDARD COST _____ DATE _____

TITLE: 32K-SV 4L
MEMORY BD ASSY
INTER LEAVED
-D85 P400
-A65Y = 32K X16 @ 1 µs
-B85Y = 32K X18 @ 750 NS

BOM 1232-XXXX REV. H
NHA: SHT. 3 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY A65Y	B85Y	-D85	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
45		ICD0097	2	2	2					74S86	
46		ICD0112	4	4	4					8095	
47		ICD0183	3	3	3					82S41	
48		ICD1533	18	18	18					75365	
49		ICD1547	2	2	2					7812	
50		ICD1835	1	1	1					LM339	
51		ICD2306	128	144	144					4060	
52		ICD2334	2	2	2					74S08	
53		ICD2338	1	1	1					74S32	
54		ICD2340	1	1	1					74S51	
55		ICD2345	1	1	1					74S260	
56		ICD90017	11	11	11					3404	
57		ICD90030	2	2	2					74180	
58		TRN1833-010	1	1	1					TRANSISTOR, NPN 2N2222A(Q1)	
59		ICD2645	1	1	1					74LS04	
60		ICD2646	2	2	2					74LS08	
61											
62											
63		WIR1365-004	A/R	A/R	A/R					WIRE 30 AWG YELLOW	
64		WIR1365-000	A/R	A/R	A/R					" " " BLACK	
65		WIR1365-001	A/R	A/R	A/R					" " " BROWN	
66		WIR1365-002	A/R	A/R	A/R					" " " RED.	

PRF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN.
CHK.
ENG.
APPRD.

STANDARD COST _____ DATE _____

TITLE: 32K-SV 4L
MEMORY BD ASSY
INTERLEAVED
-D85 P400
-A65Y = 32K X16 @ 1 µs
-B85Y = 32K X18 @ 750 NS

BOM 1232-XXX REV. H
NHA: SHT. 4 OF 4

REV	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY A65Y	B85Y	-D85	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
67	A	MEC1720-171	1	1	-					JUMPER DIP W171	
67	A	MEC1720-174	-	-	1					JUMPER DIP W174	
68	A	MEC1720-172	1	1	-					JUMPER DIP W172	
68	A	MEC1720-173	-	-	1					JUMPER DIP W173	
69		MEC0157-001	A/R	A/R	A/R					TUBING HEAT SHRINK 221-3/64	
70											A A
	D	ECB2658-001	REF	REF	REF					16K 32K ETCH CUTS	A
IV-21	C	LBD2623	REF	REF	REF					LOGIC BLOCK DIAGRAM 32K I MEM.	A

PRF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. A.Napolitano | CHK. [illegible] 6/23/76 | ENG. R&R 6/23/76 | APPRD. [illegible] 7/13/76

STANDARD COST ______ DATE ______

TITLE: MEMORY BD ASSY INTERLEAVED 16K -5V 4L
-A65Y = 16K X 16 @ 1 μs
-B85Y = 16K X 18 @ 750 NS

BOM 1216 -XXXX REV. H
NHA: SHT. 1 OF 4

REV.	ECN	CK	REV.	ECN	CK
A	RELEASED	[illegible]	E	1910A	RRC
B	1850/1862	RL	F	1929	RRC
C	1878	RL	G	1958	LC
D	1883-A	R/C	H	2038	[illegible]

ITEM	SIZE	PART NUMBER	QUANTITY A65Y	B85Y	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1		PCB2565-001	1	1							P.C.BOARD 16 K I. MEMORY	
2	C	MEC 0587	1	1							STIFFENER ASSY, P.C. BD.	
3		MEC0303-005	5	5							SCREW, BD. HD. #4-40 X 5/16 LG	
4		MEC0303-006	2	2							SCREW, BD. HD #4-40 X 3/8 LG	
5		MEC 0356	5	5							WASHER, FIBER #4	
6		MEC 0353	2	2							WASHER, FLAT, METAL #4	
7		MEC0388-002	7	7							NUT, SELF LOCKING #4-40	
8		MEC1836-001	2	2							HEAT SINK	
9		MEC 8068-001	A/R	A/R							THERMAL JOINT COMPOUND	
10		MEC8260-003	1	1							TRANSISTOR MOUNTING PAD TO18	
11		MEC1546-001	2	2							DELAY LINE, 200 NS	
12	A	MEC 0292	1	1							LABEL, SERIAL & MODEL NO.	
13		CON0650-001	2	2							SOCKET, 16 PIN, DIP	
14		CON0650-003	144	144							SOCKET, 22 PIN, DIP	
15		FUS0254-002	1	1							FUSE, SUB-MINIATURE 1.5A (F1)	
16		CON1693-001	2	2							CONN JACK P.C. BOARD	
17		SWT0601-002	1	1							DIP SWITCH, DUAL INLINE	△
18		CAP0552-529	86	86							CAP. TANT 1.0 μF 35V	
19		CAP0130-407	6	6							CAP. TANT. 8.2 μf 20V (C4,5,6,7	8,9) △B
20		CAP0130-420	3	3							CAP. TANT. 100 μf 25V (C1,2,3)	
21		CAP0546-001	81	81							CAP, GLASS 50V +80 -20% .01μf	
22		DIO1544-001	4	4							DIODE, L.C. RECT 1N4001 (CR1-CR4)	

PDP-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. A.Napolitano | CHK. | ENG. | APPRD.

STANDARD COST ______ DATE ______

TITLE: MEMORY BD ASSY INTERLEAVED 16K -5V 4L
-A65Y = 16K X 16 @ μs
-B85Y = 16K X 18 @ 750NS

BOM 1216 -XXXX REV. H
NHA: SHT. 2 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY A65Y	B85Y	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
23		DIO1759-211	1	1							DIODE, ZENER ±5% 1N5231B (CR5)	
24		DIO1759-209	1	1							DIODE, ZENER ±5% 1N5229B (CR6)	
25		RES1582-150	1	1							RES, CARBON 15Ω 1/4W (R17)	
26		RES1582-390	8	8							RES, CARBON 39Ω 1/4W (R1-R8)	
27		RES1582-680	1	1							RES, CARBON 68Ω 1/4W (R28)	
28		RES1582-151	1	1							RES, CARBON 150Ω 1/4W (R10)	
29		RES1582-391	2	2							RES, CARBON 390Ω 1/4W (R24,25)	
30		RES1582-471	2	2							RES, CARBON 470Ω 1/4W (R26,27)	
31		RES1582-102	13	13							RES, CARBON 1KΩ 1/4W (R9,11,13,14,16,23) 29,30,31,32,34,39	40) △E
32		RES1582-163	10	10							RES, CARBON 16KΩ 1/4W (R12,15,19,20,22,33,35	36,37,38) △B
33		RES1582-303	2	2							RES, CARBON 30KΩ 1/4W (R18,21)	
34		ICD0029	1	1							74HØ8	
35		ICD2599	1	1							74S3Ø	
36		ICD0059	3	3							74126	
37		ICD0070	1	1							74S64	
38		ICD0072	1	1							74S112	
39		ICD0079	3	3							82S62	
40		ICD0085	4	4							74SØØ	
41		ICD0086	2	2							74SØ4	
42		ICD0088	1	1							74S1Ø	
43		ICD0089	1	1							74S11	
44		ICD0095	1	1							74S138	

PDP-004A

PRIME COMPUTER INC.
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STANDARD COST ______ DATE ______

TITLE: MEMORY BD ASSY INTERLEAVED 16K -5V 4L
-A65Y = 16K X 16 @ 1 μs
-B85Y = 16K X 18 @ 750NS

BOM 1216 -XXXX REV. H
NHA: SHT. 3 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY A65Y	B85Y	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
45		ICD0097	2	2							74S86	
46		ICD0112	4	4							8095	
47		ICD0183	3	3							82S41	
48		ICD1533	13	13							75365	
49		ICD1547	2	2							7812	
50		ICD 1835	1	1							LM339	
51		ICD 2306	64	72							4060	
52		ICD 2334	2	2							74SØ8	
53		ICD2338	1	1							74S32	
54		ICD 2340	1	1							74S51	
55		ICD 2345	1	1							74S26Ø	
56		ICD 90017	11	11							3404	
57		ICD 90030	2	2							7418Ø	
58		TRN1833-010	1	1							TRANSISTOR, NPN 2N2222A (Q1)	
59		ICD2645	1	1							74LS04	
60		ICD2646	2	2							74LS08	
61	A	MEC1720-171	1	1							JUMPER DIP ASSY NV W171	
62	A	MEC1720-172	1	1							JUMPER DIP ASSY NV W172	
63		WIR1365-004	A/R	A/R							WIRE 30 AWG YELLOW	
64		WIR1365-000	A/R	A/R							" " " BLACK.	
65		WIR1365-001	A/R	A/R							" " " BROWN	
66		WIR1365-002	A/R	A/R							" " " RED.	

PDP-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. | CHK. | ENG. | APPRD.

STANDARD COST ______ DATE ______

TITLE: MEMORY BD ASSY INTERLEAVED 16K-5V 4L
-A65Y = 16K X16 @ 1μs
-B85Y = 16K X18 @ 750NS

BOM 1216 -XXX REV. H
NHA: SHT. 4 OF 4

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY A65Y	B85Y	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
67												△E
69		MEC0159-001	A/R	A/R							TUBING HEAT SHRINK 221-3/64	△B
?		ECB2658-001	REF	REF							16 & 32K ETCH CUTS	△E
		LBD 2623	REF	REF							LOGIC BLOCK DIAGRAM 32K I MEM.	△B △E

PDP-004A

RER:07:76

DATE: November 19, 1976

TO: List

FROM: R. E. Roberts

SUBJECT: 128KECC Memory Presentation

I. 16KRAM

The 128K memory is implemented with 16KX1 N-channel MOS dynamic RAM's. These devices are a significant departure from the 4KX1 RAM's used in existing products. The 16K RAM packs four times the storage capacity into a 16 pin DIP as opposed to the 22 pin DIP. The most significant departure from the present device is the use of multiplexed address pins. In order to address 16K locations, 14 addresses are required which in non-multiplexed schemes would demand 14 pins. The 16KX1 uses only seven pins for address input. The initial phase of the chip cycle is raw address strobe (RAS) which latches the seven least significant addresses (these are also the refresh address inputs) into the chip. The second phase of operation occurs with the advent of column address strobe (CAS). This occurs after the addresses have switched to supply the seven most significant addresses to the device. The execution of a write or read in the chip begins only after the occurrence of CAS. Refresh of this device is performed in much the same manner as in existing dynamic RAM's but with two significant differences. Due to the greater capacity, an additional refresh address must be supplied and the rate of refresh must double, that is, the 32us refresh period decreases to 16us for the 128K board in order to refresh all 16K locations within 2Ms.

Further details of operation may be obtained from device specifications available from MOSTEK, Intel, and T.I.

II. ECCL Operation Cont'd

In order to utilize any ECC scheme, it is necessary to provide additional storage to accomodate the information used to execute checking and correction. The minimum additional storage required is 5 bits of information necessary to describe, at a minimum, a no error condition and the 16 data bits or 17 unique conditions. Since the 5 bits can describe 32 unique states, a code of this size can be used to designate failing check bits as well. In order to detect all double bit errors, yet another bit is required. This sixth bit of the code is an overall parity bit generated from all of the data bits and the attandant check bits. The additional storage is therefore 6 bits for a total array width of 22 bits (16 date, 5 check, 1 overall parity).

In general, the data to be stored is presented to the memory and to the ECCL inputs where a series of interconnected parity trees generate the appropriate check bits. The check bits are stored with the data word and the overall parity bit. When the word is read from memory, it and its check bits are presented again to the ECCL where another (or the same, when multiplexed) set of interconnected parity trees generate the syndrome bits. The syndrome bits are then decoded to indicate either the bit in error or a no error condition. In the event of an error, the active line from the decoder is XOR'd with the corresponding data line resulting in the correction of the offending bit.

The overall parity bit has also been read from memory and while the syndrome generation and decode is occurring, this bit is being checked. If a no error condition has been indicated, then overall parity should also be correct; it it is not, then the overall parity bit read from storage is, itself, incorrect. A single bit error will result in incorrect overall parity and non-zero (error) syndromes. This condition indicates a correctable error. If two errors have occurred, then overall parity will be correct and non-zero syndromes will exist indicating a non-recoverable error condition.

The execution of a write to memory is initiated when write data appears at the data latch and buffer (1)*. The data is then applied to the check bit generator (2) and to the data storage (4) 5 data lines are routed to data storage via the data interchange logic (3). The check bit generator yields the resulting check bits and routes them to check bit storage (5) also via the data interchange logic. All 22 bits are then stored in memory.

*Refer to attached block diagram

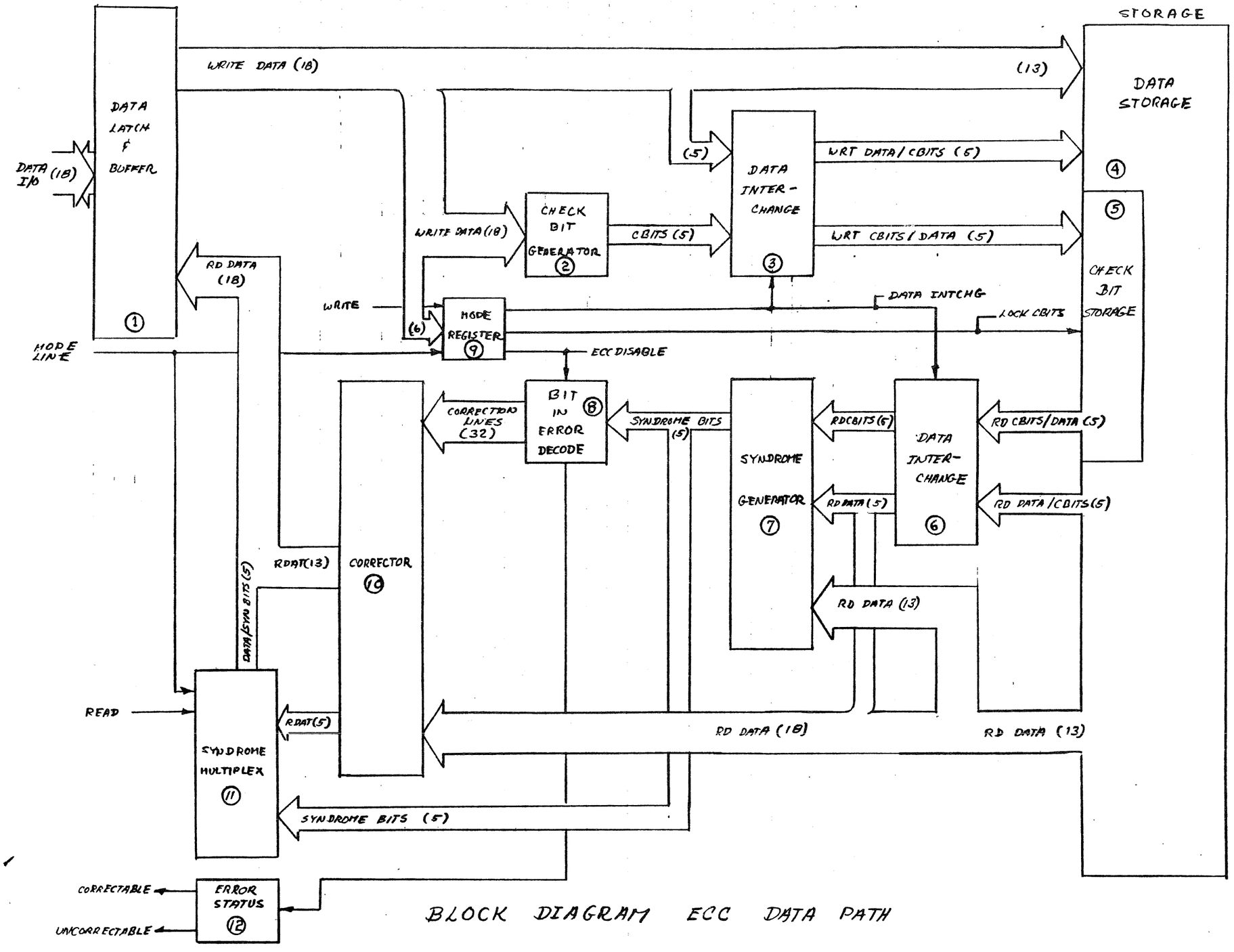
II. ECCL Operation Cont'd

When a read cycle is requested, the data and its attendant check bits are read from memory. The data is bussed to the syndrome generator (7) and to the corrector (10). Note that the same five data bits are routed to their destinations via the data interchange logic (6). The check bits are applied to data interchange (6) then to the syndrome generator. The resultant syndrome bits are applied to the bit in error decode (8). The outputs of the bit in error decoder will indicate a no-error condition or, in the event of a single bit error, cause one of the correction lines to change state. The bit in error outputs are XOR'd at the corrector (10) with the data in order to correct the offending bit.

There are four diagnostic/maintenance features incorporated in the design. These functions are activated by the memory mode line in conjunction with the mode register (9). Details of these functions are covered in the attached memo "Maintenance and Diagnostic Features for Memory with ECCL".

Ross E. Roberts

RER:jap



BLOCK DIAGRAM ECC DATA PATH

V-03

RER 2/12/76

RER:03:76

DATE: February 18, 1976

TO: List

FROM: Ross E. Roberts

SUBJECT: Maintenance ~~of~~ and Diagnostic Features for Memory with ECCL

INTRODUCTION:

Historically, memory errors have been relatively easy to detect. A known set of data was supplied to the memory and the data was retrieved to be compared with what was initially written. In this manner an error, or indeed errors, could be detected and an operator notified, thereby initiating corrective action. When error check and correction logic (ECCL) is provided, a portion of this corrective action is assumed by the memory itself. The net effect of the presence of ECCL is two-fold. Certain errors are automatically corrected, thus becoming transparent to system and operator. The source of these errors may also be recorded by the system, thereby providing a record of corrected errors which is invaluable to the field engineer in ascertaining which modules are in need of attention before they degrade system operation.

ECC is implemented by a logic structure so arranged that it provides the memory with the abilities to detect and correct single bit errors and to notify the processor in the event of certain uncorrectable errors. Further discussion concerning ECCL may be found in PE-T-163, "Error Correcting Codes", J.W. Poduska, dated December 11, 1974.

The preceding has perhaps reiterated the advantages of ECCL and as with most advantages, there are disadvantages. In the case of ECCL, the disadvantages lie in the areas of initial debug of the entire unit and later in determining the origin of a malfunction other than a storage element. It is readily evident that abnormal behavior of one or more sections of the system could lead to test results which may be confusing, misleading and potentially inconsistent. These problems may be aggravated further by the somewhat unique aspects of interleaving.

In order to minimize these anomalous interactions, three special modes of operation have been devised. These are "ECC DISABLE", "DATA INTERCHANGE", and "LOCK CHECK BITS". A fourth function, "SYNDROME INTERROGATE", is also included which provides the required data for error recording. ECC disable deactivates the ECCL and allows the memory to perform as if ECCL were not present. Data Interchange swaps check bit storage with data storage and Lock Check Bits provides a means to prevent modification to the stored check bits when new data is written.

ECC DISABLE:

The function of ECC Disable is to allow the memory to operate without intervention of the ECCL, thereby preventing the occurrence of apparent errors resulting from a malfunctioning ECCL. Activating this feature allows the data storage and its attendant support circuits to be tested and exercised in the same manner as it is presently being done.

DATA INTERCHANGE:

Data Interchange is normally used in conjunction with ECC Disable in order that the check bit storage, which is not normally accessible, may be tested in the same manner as data storage. A set of 2-1 multiplexers allows the five check bits to be stored where data bits 1-5 normally reside and the data bits 1-5 to be stored where the check bits are normally stored. The multiplexers add 14ns to read and write data paths.

The preceding two functions provide the ability to test, independent of ECCL, the entire storage array and its peripheral circuits.

LOCK CHECK BITS:

Lock Check Bits provides the means through which the ECCL may be tested. Lock Check Bits permits a predetermined set of check bits and data bits to be linked such that where both are read from memory they will yield a known syndrome and data pattern either of which may be examined by the processor for correctness. The sequence of operation is illustrated by the following example.

A word containing all zeroes is stored in the memory with its resultant check bits. Lock Check Bits is activated and a word containing a single one is written. The content of memory is now a data word having a single one and check bits describing an all zeroes word. When these are read from memory, the ECCL should take the necessary actions to correct the "error" and present an all zeroes word to the processor.

Applying in this manner a sufficient number of patterns will force single bit corrections, non-corrections, and uncorrectable errors as well as exercising each path through the check bit generators, the syndrome generators, and the bit in error decoders.

SYNDROME INTERROGATE:

The syndrome bits must be examined by the processor for diagnostic and/or recording purposes. The means of performing this action is provided by "Syndrome Interrogate". The five syndrome bits are multiplexed onto five data lines (tentatively bits 9-13). This feature must be capable of operating during diagnostic execution as well as during normal machine operation.

There are two constraints on this operation and are as follows. The execution of a syndrome interrogation must occur on the next subsequent cycle (excepting refresh cycles) after the cycle in which the error was detected. The operation must also be carried out at the same address as where the error was detected.

CONTROL:

The mechanism by which these functions are activated is comprised of a single control line designated "memory mode line" (MML) and a mode register on each memory board. The control line will be provided by BMCCNBL which is used only on the Intel 8K memory. The register will receive from data bits 1-6 a mode code which defines which function or functions are to be activated. Loading the register is accomplished by commanding the memory to execute a write cycle with the mode line active. All subsequent cycles will be executed in a normal manner (mode line not active) and the memory will respond as dictated by the mode code. Normal operation may be restored by either repeating the register load with the appropriate code or by activating master clear. A tabular description is presented on Attachment I.

Executing a read cycle with the mode line active will cause the syndromes to be presented on the data lines. A block diagram is shown on Attachment IV which illustrates the preceding functions and their positions in the data path.

INTERLEAVING:

Interleaving the memories presents a unique problem in determining which of the accessed memory cards was in error if an error should occur. This determination may be made by the error status signals which are presented to the processor two gate delays after data. These can be used to determine which block of data was in error and therefore which board was in error. Further, an instruction will be created which will cause the memory interface control to treat the memories as if they were not interleaved. They will, however, not behave exactly as if they were not interleaved. One

board will continue to retain even locations and the other odd. The significant difference is that one cycle will retrieve data from each board in succession rather than simultaneously. This enables the system to examine each board uniquely for abnormal operation.

SUMMARY:

Several features (ECC DISABLE, DATA INTERCHANGE, LOCK CHECK BITS and SYNDROME INTERROGATE) have been devised which will facilitate test and maintenance of a memory board with ECCL. In addition, a means of activating them under dynamic control has been provided utilizing minimum logic. The unique requirements of interleaved operation have been presented and dealt with.

Ross E. Roberts

/nf

Attachment I

MODE LINE/MEMORY COMMAND TABLE

Case	Memory Command	Mode Line	Action
A	Read	Not Active	Execute a normal Read Cycle
B	Write	Not Active	Execute a normal Write Cycle
C*	Read	Active	Interrogate syndrome bits and present to data bus
D	Write	Active	Enter Memory Mode Code into Memory Mode Register

Subordinate actions:

Case-

A. 1. Perform read cycle at chips
   2. Perform ECC
   3. Present data and error status to C.P.

B. 1. Accept data from C.P.
   2. Generate check bits
   3. Perform write cycle at chips

C. 1. Permit read cycle at chips
   2. Prevent entry of new data into read data latches
   3. Multiplex 5 syndromes onto 5 data lines (tentatively bits 9-13)

D. 1. Force read cycle at chips (prevent write pulse)
   2. Prevent entry of new data into read data latches
   3. Clock memory mode register at write pulse start time from data bits 1-6

* The interrogate syndrome function must be executed on the first cycle following the detection of a correctable error at the same address where the error was detected.

Attachment II

MODE CODES

Bit	1	2	3	4	5	6	Function
	0	0	0	0	0	0	Normal Operation
	1	0	0	0	0	0	Interchange Data
	0	1	0	0	0	0	Disable ECC
	0	0	1	0	0	0	Lock Check Bits

The remaining codes are undefined and will cause no modification of memory operation.

GLOSSARY

Check bits: Those bits generated by a specifically interconnected set of parity trees which are stored in conjunction with the word from which they were generated.

Syndrome bits: Those bits resulting from the application of the stored data and its attendant check bits to a specifically interconnected set of parity trees. These bits contain encoded information which when applied to the bit in error decoder indicates the error condition of the word.

BIE	Pointer**					BIE	Row Address†								
octal	1	2	3	4	5		Ø	1	2	3	4	5	6	7	
00	0	0	0	0	0	MB	*	*	*	*	*	*	*	*	00
01	0	0	0	0	1	MB	*	*	*	*	*	*	*	*	01
02	0	0	0	1	0	MB	*	*	*	*	*	*	*	*	02
03	0	0	0	1	1	15	53G	53H	53J	53K	53L	53M	53N	53P	03
04	0	0	1	0	0	MB	*	*	*	*	*	*	*	*	04
05	0	0	1	0	1	14	51G	51H	51J	51K	51L	51M	51N	51P	05
06	0	0	1	1	0	13	49G	49H	49J	49K	49L	49M	49N	49P	06
07	0	0	1	1	1	9	41G	41H	41J	41K	41L	41M	41N	41P	07
10	0	1	0	0	0	MB	*	*	*	*	*	*	*	*	10
11	0	1	0	0	1	MB	*	*	*	*	*	*	*	*	11
12	0	1	0	1	0	MB	*	*	*	*	*	*	*	*	12
13	0	1	0	1	1	12	47G	47H	47J	47K	47L	47M	47N	47P	13
14	0	1	1	0	0	16	55G	55H	55J	55K	55L	55M	55N	55P	14
15	0	1	1	0	1	11	45G	45H	45J	45K	45L	45M	45N	45P	15
16	0	1	1	1	0	10	43G	43H	43J	43K	43L	43M	43N	43P	16
17	0	1	1	1	1	RP / CB1	39G	39H	39J	39K	39L	39M	39N	39P	17
20	1	0	0	0	0	MB	*	*	*	*	*	*	*	*	20
21	1	0	0	0	1	7	9G	9H	9J	9K	9L	9M	9N	9P	21
22	1	0	0	1	0	LP	5G	5H	5J	5K	5L	5M	5N	5P	22
23	1	0	0	1	1	3	17G	17H	17J	17K	17L	17M	17N	17P	23
24	1	0	1	0	0	MB	*	*	*	*	*	*	*	*	24
25	1	0	1	0	1	2	19G	19H	19J	19K	19L	19M	19N	19P	25
26	1	0	1	1	0	1	21G	21H	21J	21K	21L	21M	21N	21P	26
27	1	0	1	1	1	CB 2	37G	37H	37J	37K	37L	37M	37N	37P	27
30	1	1	0	0	0	8	7G	7H	7J	7K	7L	7M	7N	7P	30
31	1	1	0	0	1	6	11G	11H	11J	11K	11L	11M	11N	11P	31
32	1	1	0	1	0	5	13G	13H	13J	13K	13L	13M	13N	13P	32
33	1	1	0	1	1	CB 5	3G	3H	3J	3K	3L	3M	3N	3P	33
34	1	1	1	0	0	4	15G	15H	15J	15K	15L	15M	15N	15P	34
35	1	1	1	0	1	CB4	1G	1H	1J	1K	1L	1M	1N	1P	35
36	1	1	1	1	0	CB 3	35G	35H	25J	35K	25L	35M	25N	25P	36
37	1	1	1	1	1	No Error	NA	NA	NA	NA	NA	NA	NA	NA	37
Octal	1	2	3	4	5	BIE	Ø	1	2	3	4	5	6	7	
BIE	Pointer**						Row Address†								

* = More than one (1) error at this address
NA = Not Applicable

† Row address is determined from the following chart:

	DISPLAY															
BMA	95	96	97	98	99	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	MODULE SELECT					ROW ADD.	CHIP ADDRESS															
							CHIP COLUMN							CHIP ROW								

** BIE (Bit in Error) is determined from the DSWSTATL

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BIE Pointer					LP										

1 = Syndrome bit 1 ≠ Right Parity bit (Bits 9-16)
2 = Syndrome bit 2
3 = Syndrome bit 3
4 = Syndrome bit 4
5 = Syndrome bit 5
6 = Left Parity (Bits 1-8)

128 KECC ERROR LOCATION TABLE

LTR	DATE	REVISION	DR.	CK.

SHEETS

SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
	A	A	A	A	A	A	A	A	A	A	A	A																													
	B	E	E	F	E	E	E	E	A	B	B	B																													

	DATE	DR.	CK.
RELEASED	1/11/77	JTS	JB
REVISED/ECR 2059	1 FEB 77		

MATERIAL	
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES. — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	
DWN 15 NOV 76 J. F. TRAVALINI	
CHK JB	
ENG.	
APPRD	
USED ON	
NEXT ASSY 12128-54	

PRIME COMPUTER, INC.
NATICK, MASS.

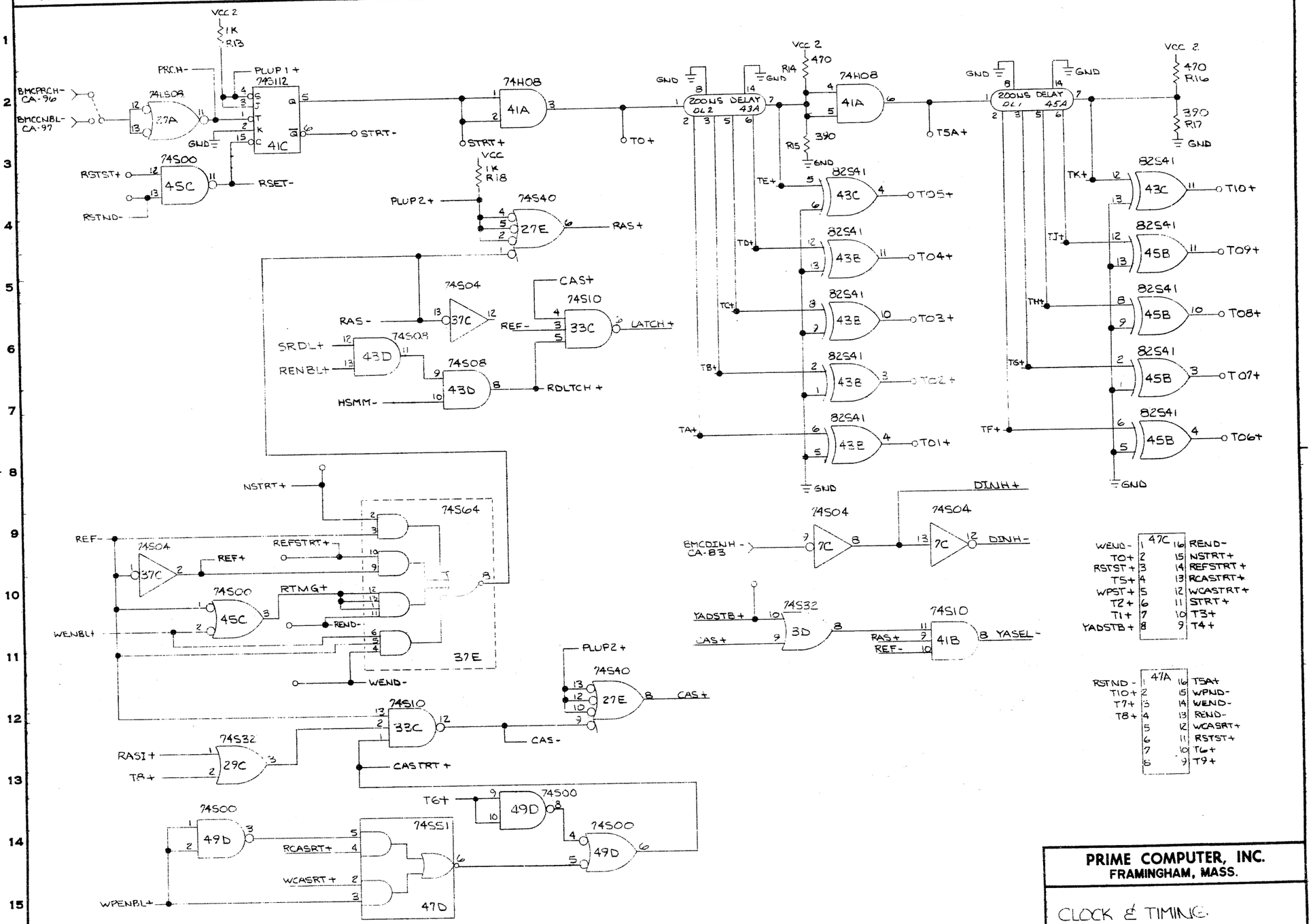
REVISION STATUS SHEET
256 KB MEMORY

SCALE | SHEET 1 OF 12 | SIZE C | DWG. NO. LB0002893 | REV. B

LBO 2893 B

7R-4

V-08

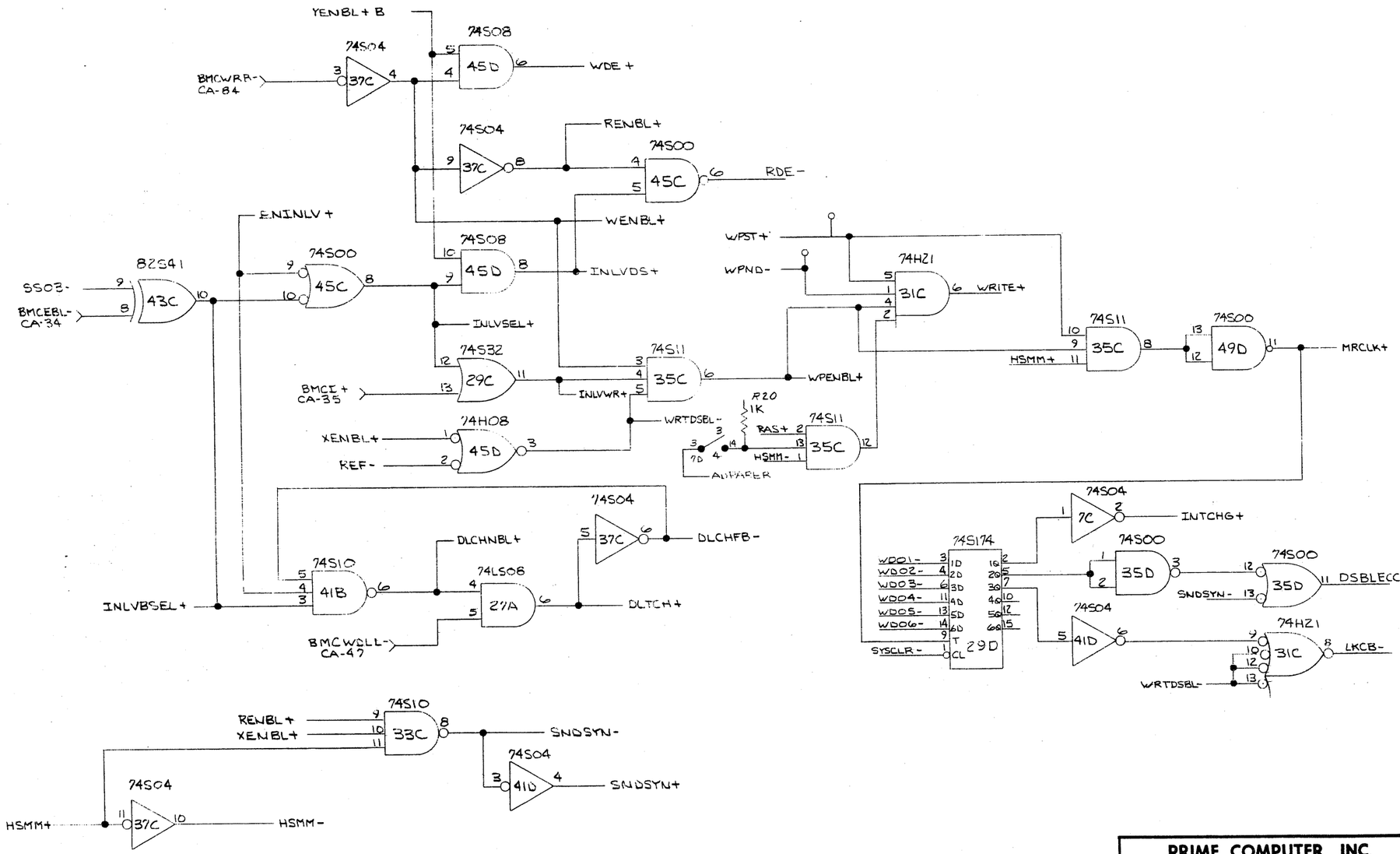


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

CLOCK & TIMING

SHEET 2 OF 12 | SIZE C | DWG. NO. [illegible] | REV.

PDF-003

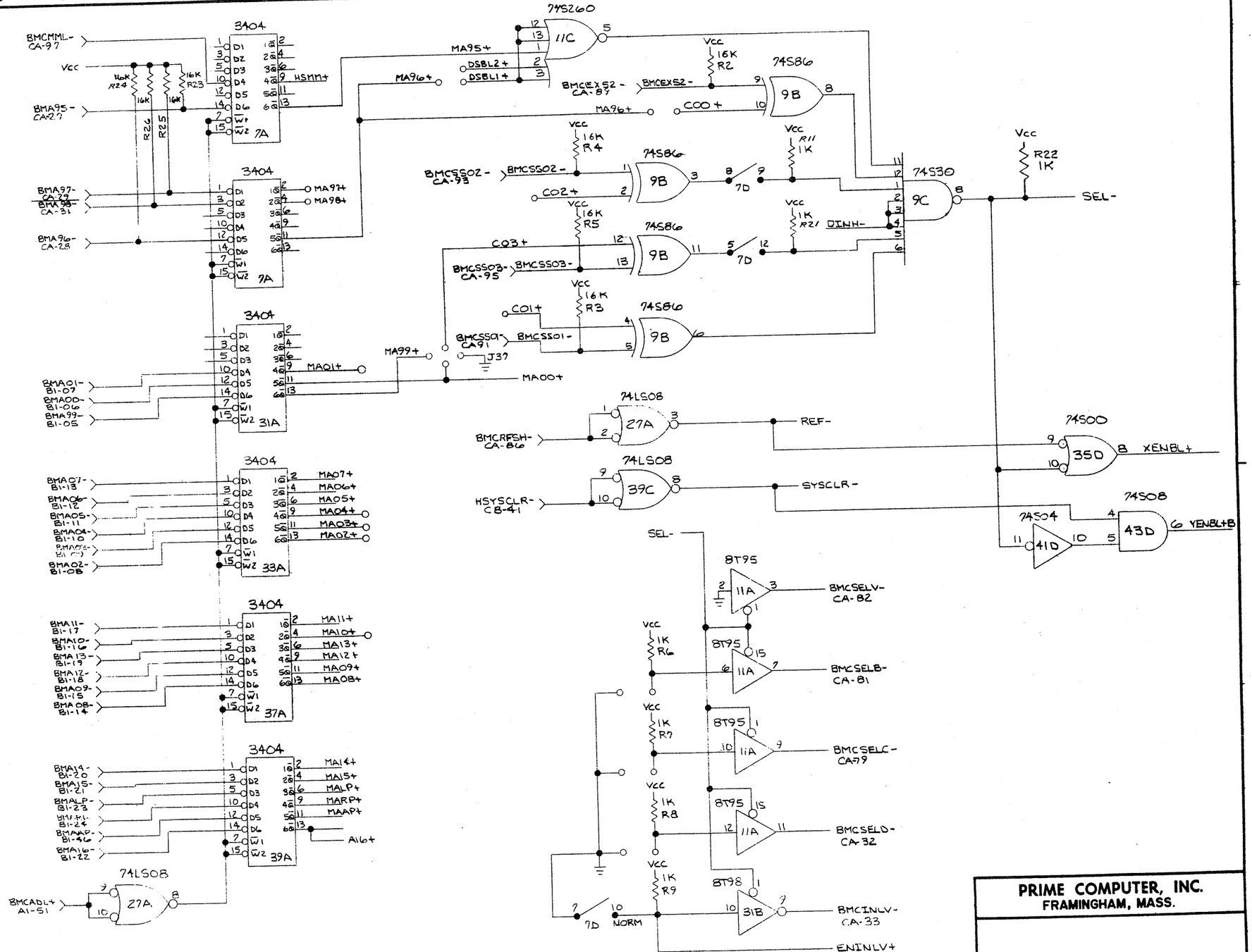


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

WRITE & INTERLEAVE CONTROL & MODE REGISTER

SHEET	SIZE	DWG. NO.	REV.
3 OF 12	C	LBD2893	E

PDF-003

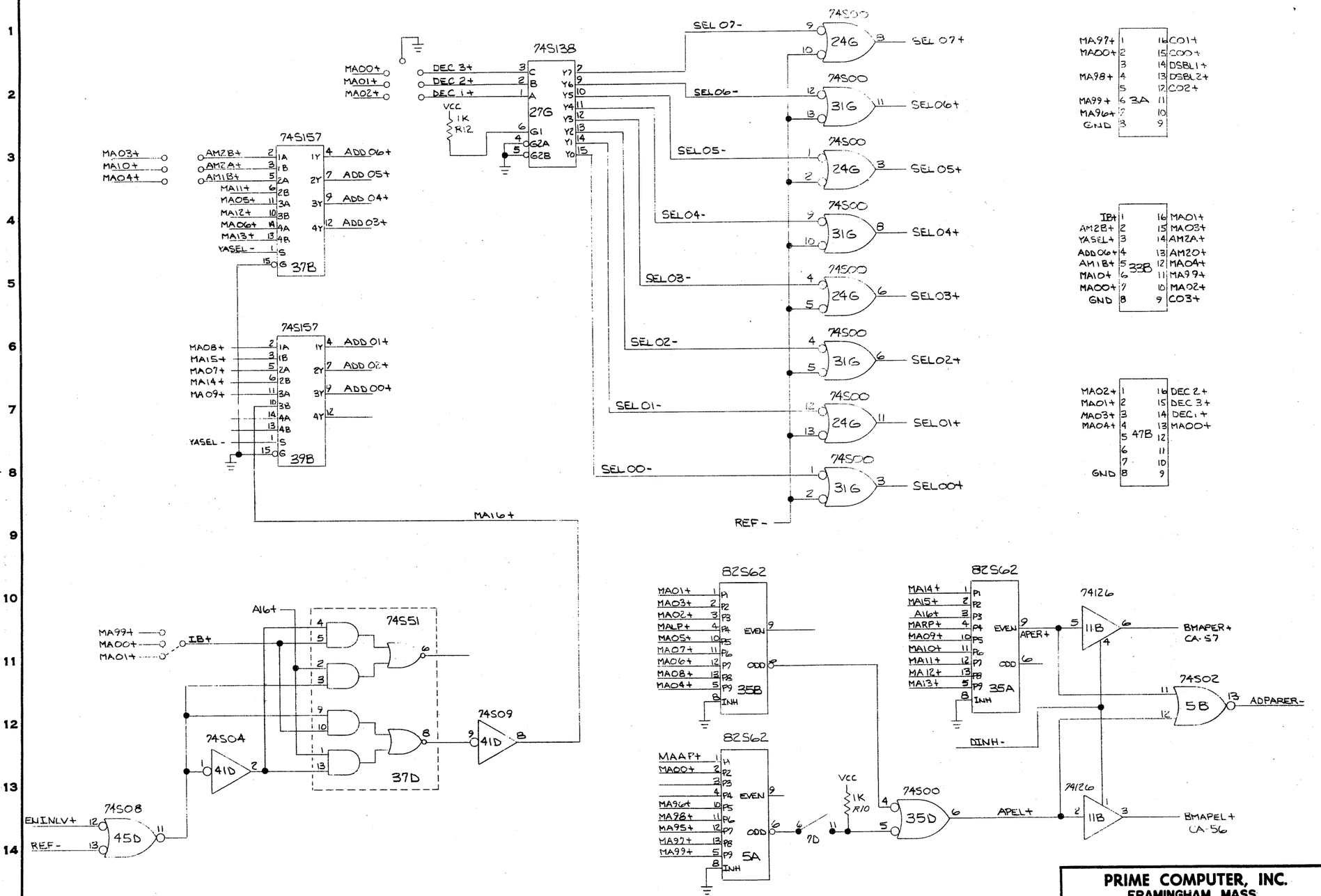


V-11

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

SHEET 4 OF 12 | SIZE C | DWG. NO. 4BD2293 | REV. F

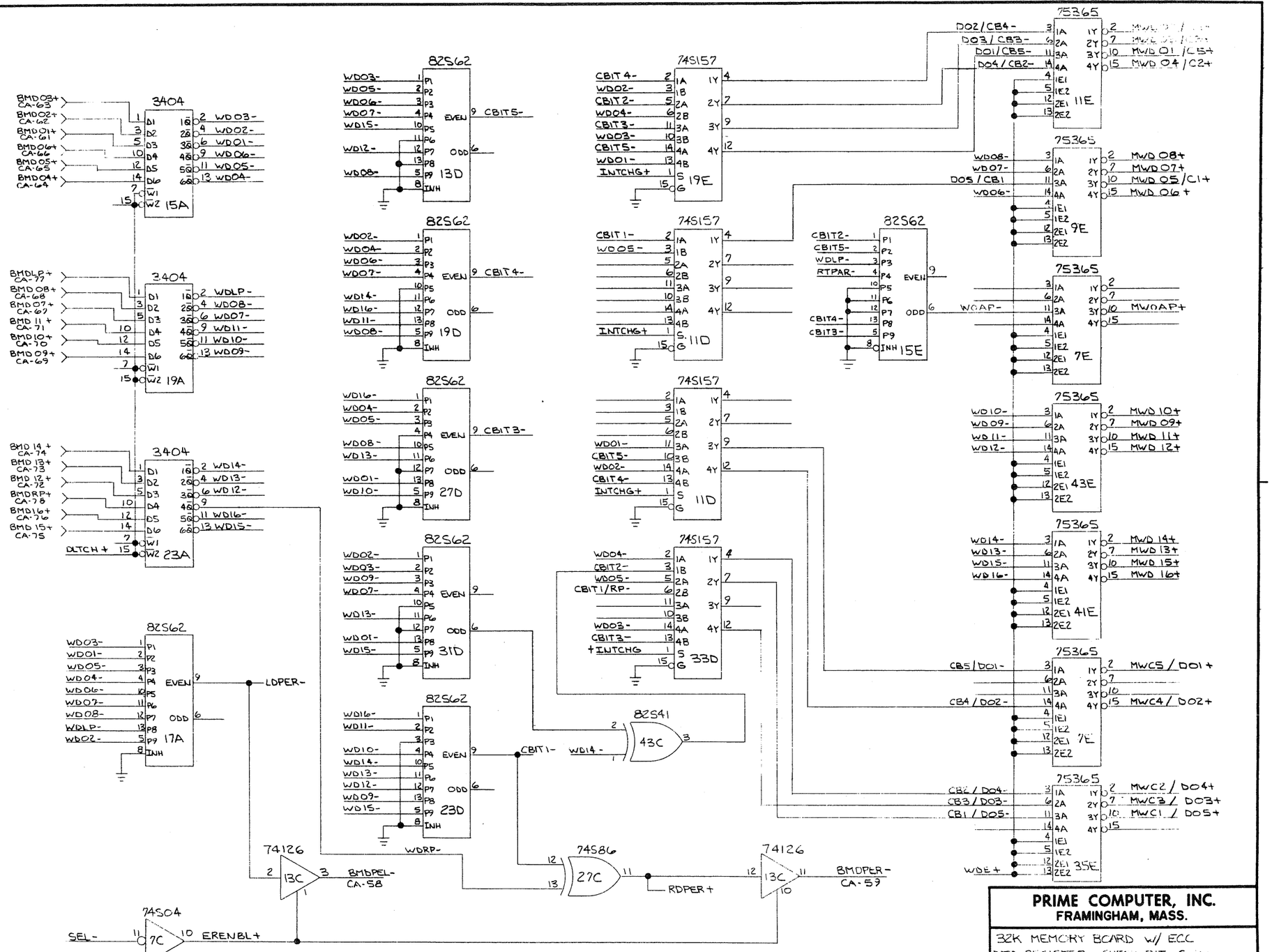
PDF-003



PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

SHEET 5 OF 12 | SIZE C | DWG. NO. LA02893 | REV. B

PDF-003

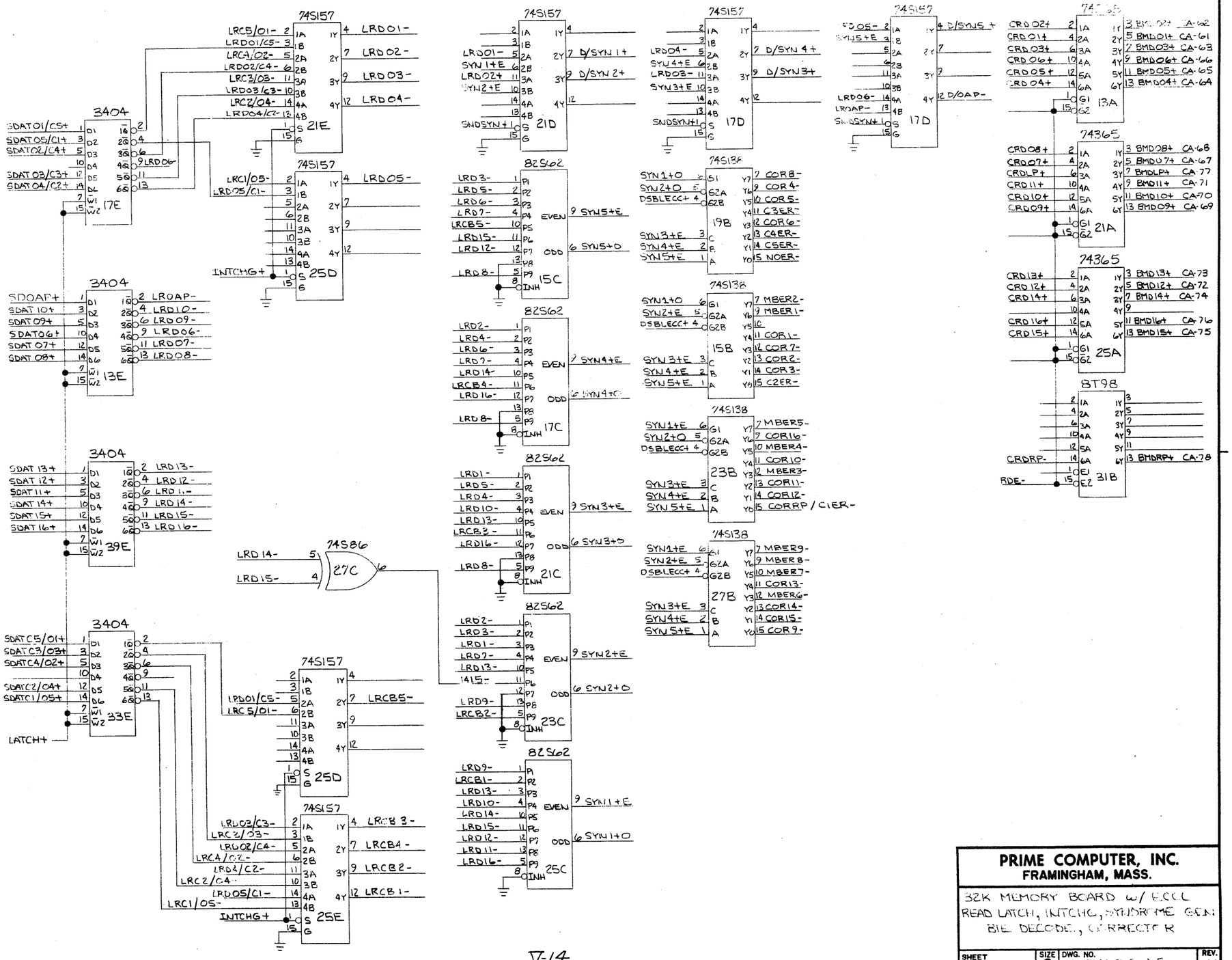


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

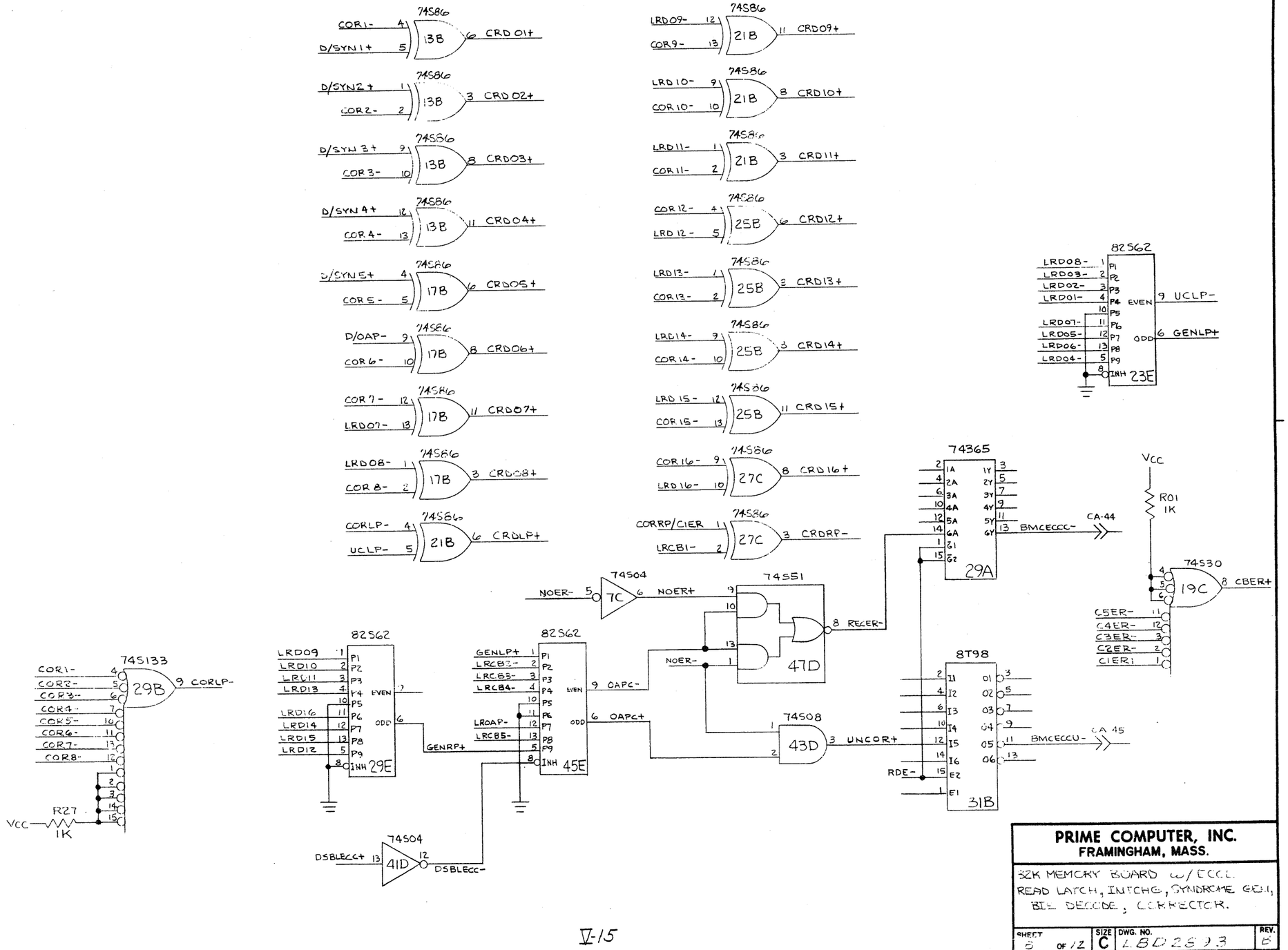
32K MEMORY BOARD W/ ECC
DATA REGISTER, CHECK BIT, GEN
INLV LOGIC & W/DATA DRIVERS

SHEET	SIZE	DWG. NO.	REV.
6 OF 12	C	L 6 6 2 5 0 3	E

PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
32K MEMORY BOARD W/ ECCC READ LATCH, INTCHG, SYNDROME GEN BIE DECODE., CORRECTOR			
SHEET 1 OF 12	SIZE C	DWG. NO. LBD2695	REV. B

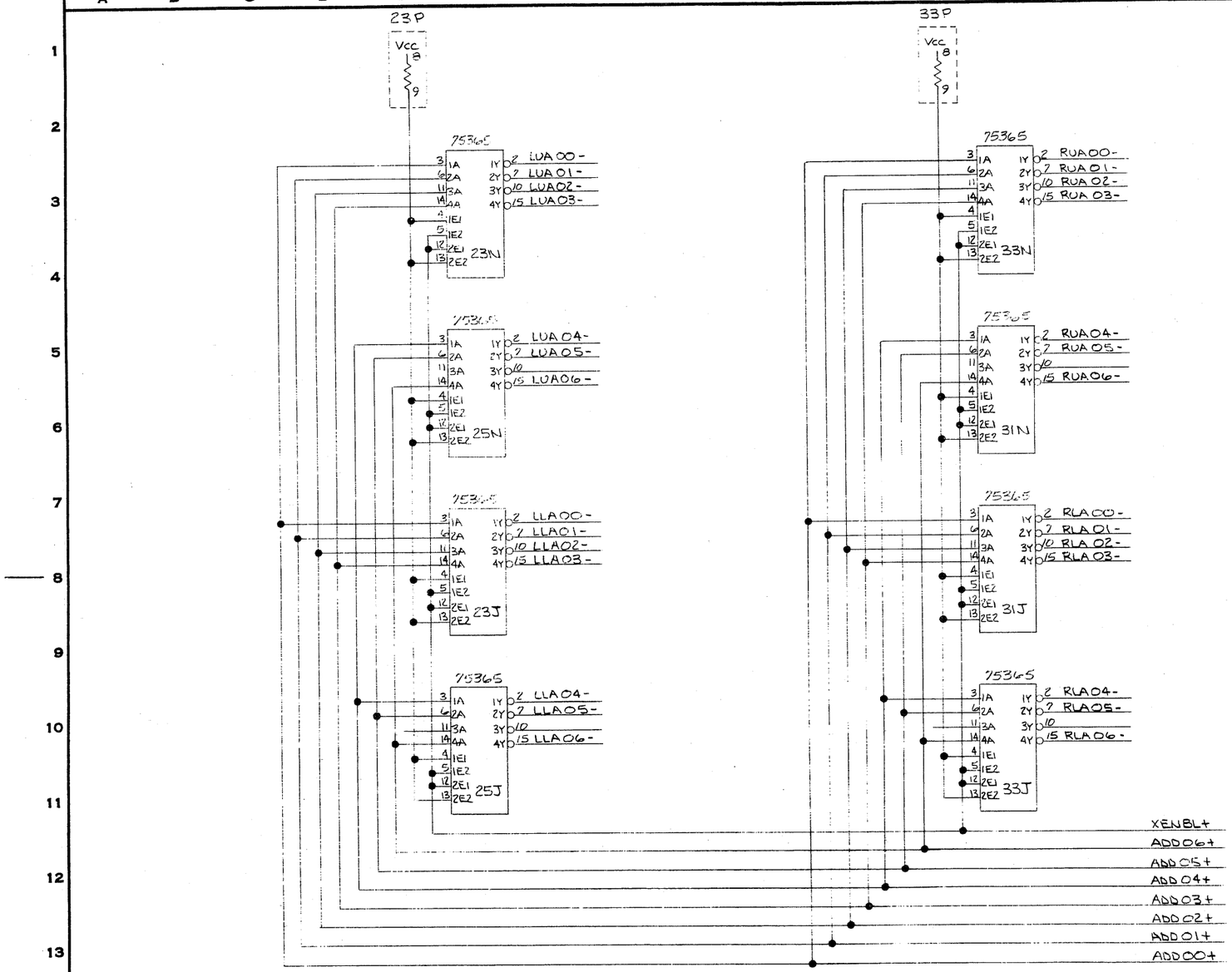


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

32K MEMORY BOARD W/ECCL
READ LATCH, INTCHG, SYNDROME GEN,
BIT DECODE, CONNECTOR.

SHEET	SIZE	DWG. NO.	REV.
5 OF 12	C	1802293	E

PDF-003



PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

ADDRESS DRIVERS

SHEET	SIZE	DWG. NO.	REV.
1 OF 12	C	LBO2893	A

PDF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

75365 VOLTAGES

VDD (12V)

VCC (5V)

1 16 8 9

LETTER PAIRS INDICATE GATES WHICH UTILISE INTERNAL CONNECTIONS OF THE 75365'S

R= 10Ω ¼W CC RES.

16K RAM VOLTAGE CONTROL LINES

VBB(-5V)	1	16	CAS-
DATA IN	2	15	DATA OUT
WRITE-	3	14	
RAS-	4		
VDD (12V)	8	9	VCC (5V)

UNMENTIONED PINS ARE ADDRESS

75365

SEL07+	3	1A	1Y 2
SEL06+	6	2A	2Y 7
LKCB-	11	3A	3Y 10
XENBL+	14	4A	4Y 15
RAS+	4	1E1	
XENBL+	5	1E2	
SEL07+	12	2E1	25P
WRITE+	13	2E2	

75365

CAS+	3	1A	1Y 2
	6	2A	2Y 7
LKCB-	11	3A	3Y 10
XENBL+	14	4A	4Y 15
XENBL+	4	1E1	
XENBL+	5	1E2	
WRITE+	12	2E1	27P
SEL06+	13	2E2	

75365

SEL05+	3	1A	1Y 2
SEL04+	6	2A	2Y 7
LKC	11	3A	3Y 10
XENBL+	14	4A	4Y 15
RAS+	4	1E1	
XENBL+	5	1E2	
SEL05+	12	2E1	25M
WRITE+	13	2E2	

75365

CAS+	3	1A	1Y 2
	6	2A	2Y 7
LKCB-	11	3A	3Y 10
XENBL+	14	4A	4Y 15
XENBL+	4	1E1	
XENBL+	5	1E2	
WRITE+	12	2E1	27M
SEL04+	13	2E2	

75365

SEL03+	3	1A	1Y 2
SEL02+	6	2A	2Y 7
LKCB-	11	3A	3Y 10
XENBL+	14	4A	4Y 15
RAS+	4	1E1	
XENBL+	5	1E2	
SEL03+	12	2E1	25K
WRITE+	13	2E2	

75365

CAS+	3	1A	1Y 2
	6	2A	2Y 7
LKCB-	11	3A	3Y 10
XENBL+	14	4A	4Y 15
XENBL+	4	1E1	
XENBL+	5	1E2	
WRITE+	12	2E1	27K
SEL02+	13	2E2	

75365

SEL01+	3	1A	1Y 2
SEL00+	6	2A	2Y 7
LKCB-	11	3A	3Y 10
XENBL+	14	4A	4Y 15
RAS+	4	1E1	
XENBL+	5	1E2	
SEL01+	12	2E1	25H
WRITE+	13	2E2	

75365

CAS+	3	1A	1Y 2
	6	2A	2Y 7
LKCB-	11	3A	3Y 10
XENBL+	14	4A	4Y 15
XENBL+	4	1E1	
XENBL+	5	1E2	
WRITE+	12	2E1	27H
SEL00+	13	2E2	

23P: 14 3 LRAS7-; 10 7 LRAS6-; 12 5 LWCB7-; 15 2 LWP7-

23M: 14 3 LRAS5-; 10 7 LRAS4-; 12 5 LWCB5-; 15 2 LWP5-

23K: 14 3 LRAS3-; 10 7 LRAS2-; 12 5 LWCB3-; 15 2 LWP3-

23H: 14 3 LRAS1-; 10 7 LRAS0-; 12 5 LWCB1-; 15 2 LWP1-

27P: 16 1 LCASD-; 11 6 LWCB6-; 13 4 LWP6-

27M: 16 1 LCASC-; 11 6 LWCB4-; 13 4 LWP4-

27K: 16 1 LCASB-; 11 6 LWCB2-; 13 4 LWP2-

27H: 16 1 LCASA-; 11 6 LWCB0-; 13 4 LWP0-

1P 3P 5P 7P 9P 11P 13P 15P 17P 19P 21P

1J 3J 5J 7J 9J 11J 13J 15J 17J 19J 21J

1N 3N 5N 7N 9N 11N 13N 15N 17N 19N 21N

1M 3M 5M 7M 9M 11M 13M 15M 17M 19M 21M

1L 3L 5L 7L 9L 11L 13L 15L 17L 19L 21L

1K 3K 5K 7K 9K 11K 13K 15K 17K 19K 21K

1H 3H 5H 7H 9H 11H 13H 15H 17H 19H 21H

16K RAM 4 15 3

1G 3G 5G 7G 9G 11G 13G 15G 17G 19G 21G

16K RAM 16 2 14 4 15 3

MWD04/C2+ SDAT04/C2+ MWDC3/C3+ SDAT03/C3+ MWDC2/C4+ SDAT02/C4+ MWD01/C4+ SDAT01/C4+

MWC4/002+ SDATC4/02+ MWC5/D01+ SDATC5/01+ MWDLP+ SDATLP+ MWD008+ SDATC6+ MWD007+ SDAT07+ MWD006+ SDAT06+ MWD05/C1+ SDAT05/C1+

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

STORAGE ARRAY & CONTROL DRIVERS (LEFT SIDE)

SHEET 10 OF 12 | SIZE C | DWG. NO. LAB028 93 | REV. B

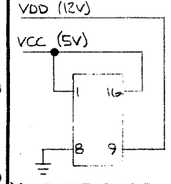
PDF-003

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

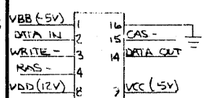
75365
VOLTAGES

VDD (12V)
VCC (5V)

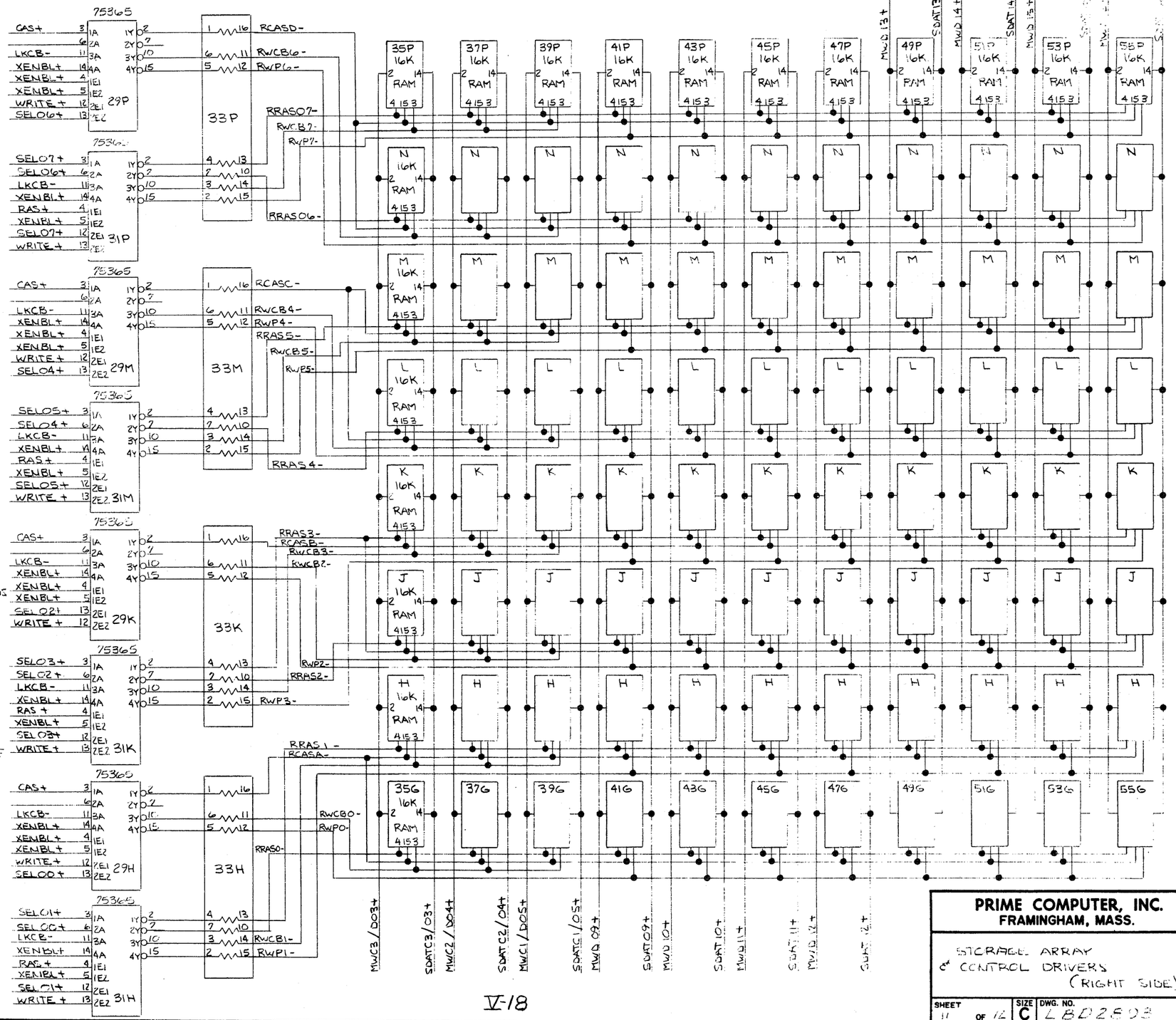


* LETTER PAIRS INDICATE GATES WHICH UTILISE INTERNAL CONNECTIONS OF THE 75365'S

16K RAM
VOLTAGE & ** CONTROL LINES



** UNMENTIONED PINS ARE ADDRESS.

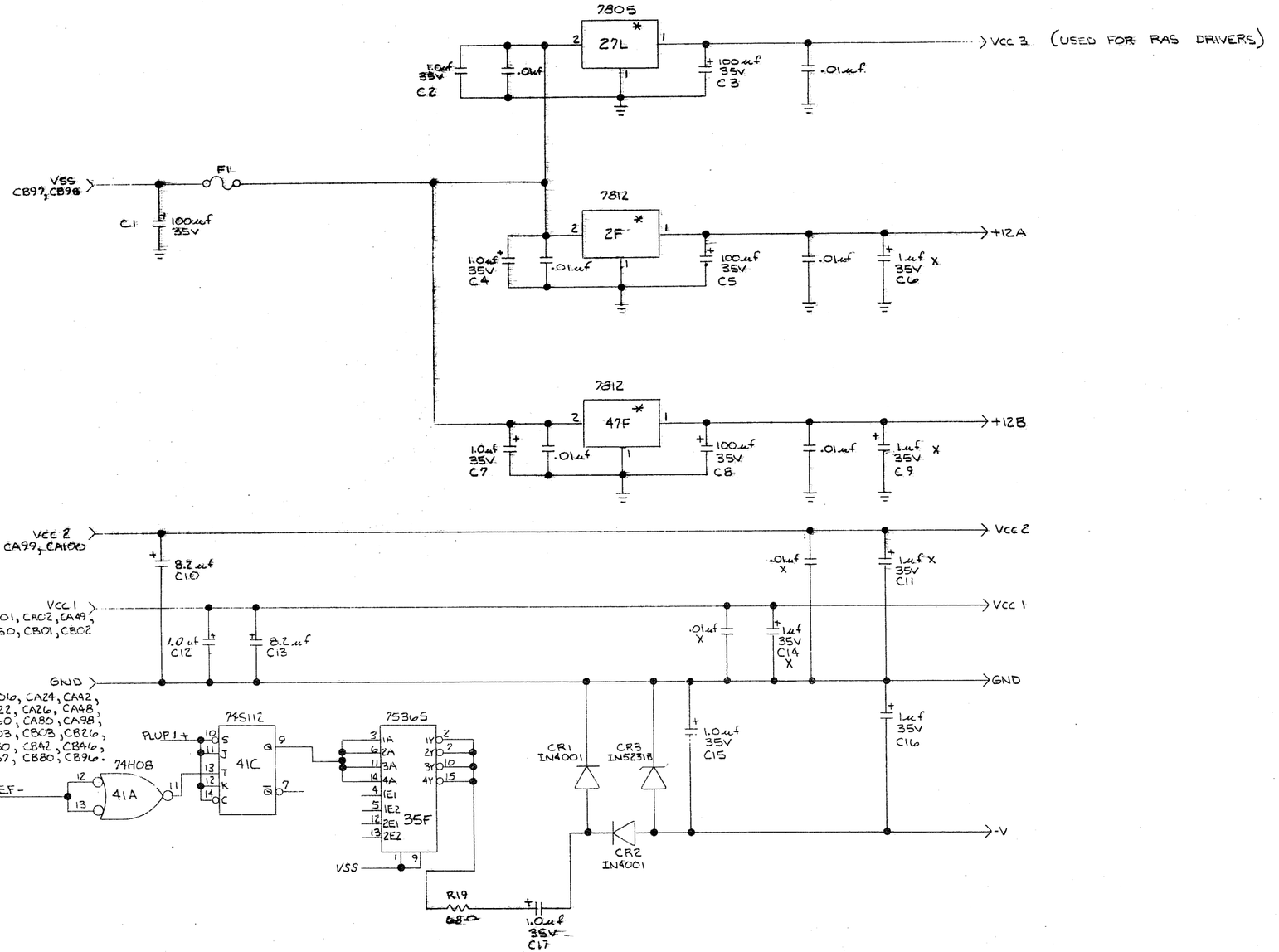


PDF-003

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

STORAGE ARRAY & CONTROL DRIVERS (RIGHT SIDE)

SHEET	SIZE	DWG. NO.	REV.
11 OF 12	C	LB02503	B



* THESE MUST BE MOUNTED ON HEATSINK.

PDF-003

PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
128K ECC POWER SECTION			
SHEET 12 OF 12	SIZE C	DWG. NO. 4B02893	REV. B

M	LTR	DATE	REVISION	DR.	CK.
	A	1-11-77	RELEASED	JFS	[illegible]
	B	1-31-77	REDRAWN & REVISED/ECR 2059	JFS	[illegible]

(18)

(57) (MK 4116 P-53) 176 PLACES SHOWN WITH *

(9) (10) SEE NOTE 1

(38)

(6) (4) (7)

(11)

(12)

(1)

(13)

(2)

(6) (4) (7)

SEE NOTE 1 (9) (10)

(14)

(7)

(8) JUMPERS 8 PLACES

R9

NOTE
1. APPLY ITEM 10 (THERMAL COMPOUND) BETWEEN ITEM 1 (PC BOARD) & ITEM 9 (HEATSINK)

REF (7) (5)
REF (2)
(5) (3) (1) REF

(17) ALL UNMARKED CAPACITORS WITH POLARITY MARKING

(6) (4) (7)
(38)
(9) (10) SEE NOTE 1

(16) ALL UNMARKED CAPACITOR WITHOUT POLARITY MARKING

MATERIAL SEE BOM	DWN [illegible]	PRIME COMPUTER, INC. FRAMINGHAM, MASS.
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES –DIMENSIONS ARE IN INCHES –TOLERANCES XX ± .02 XXX ± .005 ANGLES ± 1/2°	CHK	MEMORY BOARD ASSY 256 KB W/ECC P300X & P400
	ENG [illegible] 1/11/77	
	APPRD [illegible] 1/10/77	
	USED ON NEXT ASSY P401ZBE-XX	SCALE FULL SHEET 1 OF 1 SIZE D DWG NO. 12128-E4 REV. B

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. [signature] 11/15/76 | CHK. [signature] | ENG. [signature] 1/5/77 | APPRD. [signature] 1/6/77

STANDARD COST ______ DATE ______

TITLE: MEMORY BD ASSY 256 KB W/ ECC — P300X & P400 (EV)

BOM 12128-E4 — REV. B — NHA: P40128 E-XX — SHT. 1 OF 3

REV.	ECN	CK
A	REL	[signature]
B	2059/2038	[signature]

ITEM	SIZE	PART NUMBER	QUANTITY	DESCRIPTION	STANDARD COST
1		PCB2625-001	1	P.C. BOARD, 128 K MEMORY	
2	C	MEC0587	1	STIFFENER ASSY, P.C. BD.	
3		MEC0303-005	5	SCREW, PAN HD. # 4-40 x 5/16 LG.	
4		MEC0303-006	3	SCREW, PAN HD # 4-40 x 3/8 LG.	
5		MEC0356	10	WASHER, FIBER #4	
6		MEC0353	3	WASHER, FLAT METAL #4	
7		MEC0388-002	8	NUT, SELF LOCKING # 4-40	
8		WIR1365-004	A/R	WIRE, 30 AWG (YEL)	
9		MEC1836-001	3	HEAT SINK	
10		MEC8068-001	A/R	THERMAL JOINT COMPOUND	
11		FUS0254-002	1	FUSE, SUB MINIATURE 1.5A (F1)	
12		CON1693-001	2	CONNECTOR JACK P.C. BOARD	
13	B	MEC1590-003	1	LABEL, I/O CONN IDENT BLANK	
14		CAP0130-407	2	CAP, TANT 20V, 10%, 8.2 µf C10 C13	
15		CAP0130-420	4	CAP, TANT 20V, 10%, 100.0 µf C1, C3 C5, C8	
16		CAP0546-001	97	CAP, GLASS 50V +80 -20% .01 µf	C2, 4, 6, 7, 9, 12 C15, 16, 17
17		CAP0552-529	166	CAP, TANT 35V, 10% 1.0 µf	C2, 4, 6, 7, 9, 12 C15, 16, 17
18		CON0650-001	181	SOCKET, DIP, SOLDER TYPE 16 PIN	
19		DIO1544-001	2	DIODE, LC RECT 50V, IN4001 CR1 CR2	
20		DIO1759-211	1	DIODE, ZENER 5% IN5231B CR3	
21		ICD0034	1	74H21	
22		ICD0059	2	74126 OR 8094	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. [signature] 11/15/76 | CHK. [signature] | ENG. [signature] 1/5/77 | APPRD. [signature] 1/6/77

STANDARD COST ______ DATE ______

TITLE: MEMORY BD ASSY 256 KB W/ ECC — P300X & P400 (EV)

BOM 12128-E4 — REV. B — NHA: — SHT. 2 OF 3

ITEM	SIZE	PART NUMBER	QUANTITY	DESCRIPTION	STANDARD COST
23		ICD0070	1	74S64	
24		ICD0072	1	74S112	
25		ICD0075	10	74S157	
26		ICD0076	1	74S174	
27		ICD0079	18	82S62	
28		ICD0085	5	74S00	
29		ICD0086	3	74S04	
30		ICD0088	2	74S10	
31		ICD0089	1	74S11	
32		ICD0095	5	74S138	
33		ICD0096	1	74S133	
34		ICD0097	6	74S86	
35		ICD0112	5	8T95 / 8095 / 74365A	
36		ICD0183	3	82S41	
37		ICD1533	31	75365	
38		ICD1547	2	7812 UC OR LM340T-12	
39		ICD2333	1	74S02	
40		ICD2334	2	74S08	
41		ICD2338	2	74S32	
42		ICD2340	2	74S51	
43		ICD2345	1	74S260	
44		ICD2450	1	7805KM / LM340K-5	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. [signature] 11/15/76 | CHK. [signature] | ENG. [signature] 1/5/77 | APPRD. [signature] 1/6/77

STANDARD COST ______ DATE ______

TITLE: MEMORY BD ASSY 256 KB W/ ECC — P300X & P400 (EV)

BOM 12128-E4 — REV. B — NHA: — SHT. 3 OF 3

ITEM	SIZE	PART NUMBER	QUANTITY	DESCRIPTION	STANDARD COST
45		ICD2581	1	8T98	
46		ICD2599	2	74S30	
47		ICD2646	2	74LS08	
48		ICD1397	12	3404	
49		ICD0091	1	74S40	
50		MEC1546-001	2	DL 200 OHMS, 200 NS AT 40NS	
51		RES1582-102	12	RES, CARBON 1/4 W, 5%, 1K R1, 6-13, 18 20-22, 27, 28	
52		RES1582-163	8	RES, CARBON 1/4 W, 5%, 16K R2-5 R23-R26	
53		RES1582-391	2	RES, CARBON 1/4 W, 5%, 390 Ω R15 R17	
54		RES1582-471	2	RES, CARBON 1/4 W, 5% 470 Ω R14 R16	
55		RES1582-680	1	RES, CARBON 1/4 W, 5% 68 Ω R19	
56		SWT0601-002	1	SWITCH, DUAL INLINE	B
57		ICD2794	176	MK4116P-53	
58		ICD0029	1	74H08	
59		JDA2769-923	1	JUMPER DIP ASSY W923	
60		JDA2769-924	1	JUMPER DIP ASSY W924	
61		JDA2769-925	1	JUMPER DIP ASSY W925	
62		JDA2769-926	1	JUMPER DIP ASSY W926	
63		JDA2769-927	1	JUMPER DIP ASSY W927	
64		RDA2820-904	8	RESISTOR DIP ASSY RD4	
65					
	C	LBD2893	REF	LOGIC BLOCK DIAGRAM	

PDF-004A

DATE: November 16, 1976

PE-T-243
Rev 3

TO: Programming and Engineering Staff

FROM: Jon Sjostedt

SUBJECT: MEMORY EXTENDER SPECIFICATION (SPC 2819)

The Memory Extender Specification is now available from Drafting under SPC 2819.

I. FUNCTION

The Memory Extender is a means of expanding the P400 Memory Bus. The bus is not changed physically, but the Memory Extender Boards that plug into it provide a greater capacity. The Memory Extender Boards can be thought of as either a 256K memory board (physically representing up to 8-32K memory boards) or a 1024K memory board (physically representing up to 8-128K memory boards).

The P400's main memory addressing capability is 2**22 or 4,194,304 words! The maximum main memory in a system using only 32K memory boards is with 10 Memory Extenders, each representing 256K, for a system total of 2,621,440 words. The maximum P400 addressing capability can only be met using 128K memory boards. A total of 32-128K memory boards are needed. Four Memory Extenders each with 8 memory boards or 3 Memory Extenders and 8 memory boards in the Main Backplane will accommodate this configuration.

Combining 32K and 128K memory boards in one system is described in section 3 of this specification.

Memory address parity and memory data parity are checked twice (only address parity on a read cycle); once in the main backplane, just as any other memory board does, and once as the address and data get to the real memory boards. This second check is done in the extended backplane and any errors detected (address and/or data on write, address on read) are sent to the C.P.U. and there causes a memory address parity error trap.

II. HARDWARE REQUIREMENTS

The Memory Extender is supported only by the P400 C.P.U.

The Memory Extender consists of a 10 slot chassis, a power supply, 2 Memory Extender Boards, and a Memory Extender Cable Set (15 feet long). There are approximately 60 signals involved in passing the Memory Bus to an Extended Backplane.

The basic configuration is: one Memory Extender board plugs into the Main Backplane Memory Bus and is connected by 3 cables to another Memory Extender board plugged into the 10 slot chassis which contains the extended memories.

The Extended Backplane requires one modification, one jumper wire. (Slot 5 CB-45 to Slot 1 CB-64.) This jumper wire sends to the backplane a system clear signal (HSYSCLR+), generated in the power supply that is etched exclusively to a control panel connector on the Extended Backplane. The Memory Extender board plugged into this Extended Backplane has logic on it (normally found on a control panel) that generates a valid (debounced) system clear signal (HSYSCLR-).

VI-01

The memory select valid signal (BMCSELV-) signifies to the C.P.U. that the memory access is directed to a valid memory location. On extended cycles, this signal is generated by the extended memory boards and transferred, over the cables, to the C.P.U. If power were to be off in the extended backplane, any access to this backplane will not generate BMCSELV- and thus would cause a missing memory module trap.

The 44 amp. power supply which powers the extended 10 slot chassis has a minimum loading requirement of 8 amps. for all voltages to stabilize. The Memory Extender board in the extended backplane has loading resistors on it which will sufficiently load the power supply to handle a minimum configuration of 1 memory board and 1 Memory Extender board.

III. FIRMWARE REQUIREMENTS

The Memory Extender board in the Main Backplane activates a signal (BMCSELC-) upon proper decoding of the Memory Address Bus (BMA's). This signal indicates to the C.P.U. memory interface that an extended cycle is to take place. Read cycle timing to extended memory boards is approximately 28% longer. Write cycle timing is approximately 17%. Read and Write cycle timing to non-extended memory boards is not affected.

There is the option (by means of a switch) of activating a signal (BMCSELB-) that will indicate timing for 32k interleavable memory boards (1232-B85). This switch represents up to 8 memory boards, all of which must be of a like mode.

There is the option (by means of a switch) of activating a signal (BMCSELD-) that will indicate timing for 128k memory boards (12126-E4). This switch represents up to 8 memory boards, all of which must be of a like mode.

There is also the option (by means of a switch) of activating the interleave signal (BMCINLV-). This can only be done if all of the memory boards represented by this Memory Extender board can interleave and are paired up. Extended, interleave, read access time for 2 words is 40% longer than non-extended, interleave, read access. Extended interleave, write cycles are 29% longer than non-extended interleave, write cycles.

On extended write cycles of any type, the C.P.U. micro-code is overlapped with the write cycle. Once the address and data are on the memory bus and the cycle is started, the C.P.U. can then execute further micro-code instructions. If these micro-code instructions do not call for a memory cycle, the C.P.U. is not affected by these extended write times. If a DMX cycle is in progress, the transfer time is dependent on the memory cycle time. The increase in DMX input cycle time is 15% (non-interleaved, memory write). The increase in DMX output cycle time is 20% (non-interleaved, memory read).

P400 PROM set ML rev H or later is required to support a Memory Extender. Rev. A supports extended, compatable memory cycles. In addition, Rev. C supports extended, 32k interleaved, non-interleaved cycles. In addition, Rev. D supports extended 128k interleaved, non-interleaved cycles.

IV. SOFTWARE REQUIREMENTS

As a product, the Memory Extender requires no special software. If, however, a system configuration has more than 256K of main memory, the operating system must be capable of utilizing this extra memory.

V. CONFIGURATIONS

When using a Memory Extender, the memory boards in the Main Backplane must decode an address space at least as large as the amount of memory in the entire system. That is to say, if there is a Memory Extender set to respond to the second 256K address block (BMA98-active), then the individual memory boards in the Main Backplane must shut off on BMA98 going active. If multiple Memory Extenders are in use, then the individual memory boards in the Main Backplane must not respond to addresses other than their own, low order, address space. This is true only of the memory boards in the Main Backplane. The Memory Extender will deactivate high order address bits so that the extended memory boards will see an address on the Extended Backplane of a low order (0-256K using 32K memory boards or 0-1024K using 128K memory boards). This allows P400, 32K memory boards (model 1232-B85X)(This memory board is the standard 32K board (1232-B85) with ECO 1757) to work in a system with more than 256K of memory. These boards are put into an extended chassis.

The placement of a Memory Extender in the Main Backplane is highly flexible. The address decode is done either against hard wired slot coding on the Main Backplane or, selectively, against a switch setting.

If address decoding is done against the hard wired code, then placement of a Memory Extender follows similar constraints as placement of a memory board; the difference being the size of the responding address space. A Memory Extender is either a 256K or a 1024K memory board.

If address decoding is done against a switch setting, then the Memory Extender placement is independent of the responding address space.

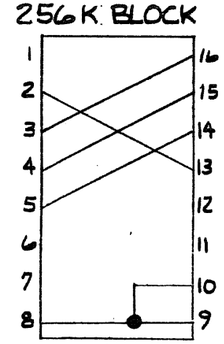
DIP SWITCH: LOCATION 06B (MAIN BOARD)

SWITCH #	FUNCTION
7	Slot code in inverted binary (same as hardwired
1	backplane code) with SW3 as the least significant
2	bit, SW7 is most significant bit Off=1 On=0
3	Example: OFF,OFF,OFF,ON=Slot 1
4	Select switch to choose above code (=OFF) or hardwired backplane code (=ON)
5	BMCINLV+ select - OFF=Interleave Enable, ON=Interleave Disable
6	BMCSELB+ select - OFF=BMCSELB Enable, ON=BMCSELB Disable
8	BMCSELD+ Select - Off=BMCSELD Enable ON=BMCSELD Disable

Memory boards in the Extended Backplane can be mixed (i.e., 32K and 128K memory boards). If the total memory in an Extended Backplane is less than or equal to 256K (i.e., 8-32K memory boards or 2-128K memory boards or 1-128K and 4-32K, etc.) then the Memory Extender board in the Main Backplane will be set up to respond to a 256K block. If the memory in the Extended Backplane is greater than 256K, then the Memory Extender board in the Main Backplane will be set up to respond to a 1024K block. Placement rules in an Extended Backplane for a mixture of memory boards are the same as present memory configuration rules.

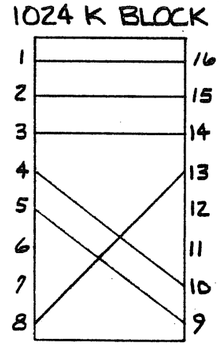
CONFIGURATION DIP: LOCATION 06C

256K BLOCK



MEC1720-175

1024 K BLOCK



JDA2769-912

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
A	A	A	A	A	A	A	A	A																																	
B	B	B	B	B	-	B	-	B																																
C	C	C	C	C																																				
D	D							C																																
E	E							D																																
F		D			C			E																																
G		E	D	B				F																																
H	F	F																																						

DATE	ENGINEERING CHANGE NOTICES
06-25-76	RELEASED
9-8-76	REVISED PER ECR 1892 W.L. TO REV 1
12/10/76	WIRE LIST TO REV 2 PER ECR 1965 & REVISED PER ECR 1980-A
12/10/76	WIRE LIST TO REV 3 & AT LOCATION C12, DIP CHANGED FROM 74510 TO 74520 & ADDED 74586 AT C29 PER ECR 1989
12/14/76	WIRE LIST TO REV 4 & ADDED GND TO PINS 7 & 8 AT DIP SITE B06 PER ECR 1990-A ADDED NOTE TO SHEETS 2 & 8 ECN 6011
1-28-77	REVISED PER ECR 2019
1-31-77	WIRE LIST TO REV 5. REVISED PER ECR 2027-A
3FEB-77	WIRE LIST TO REV 6. REVISED PER ECR 2070-A

LTR	DATE	REVISION	DR.	CK.
			[illegible]	[illegible]
			[illegible]	JS
			[illegible]	JS
			[illegible]	JS
			[illegible]	JS
			[illegible]	JS
			[illegible]	JS

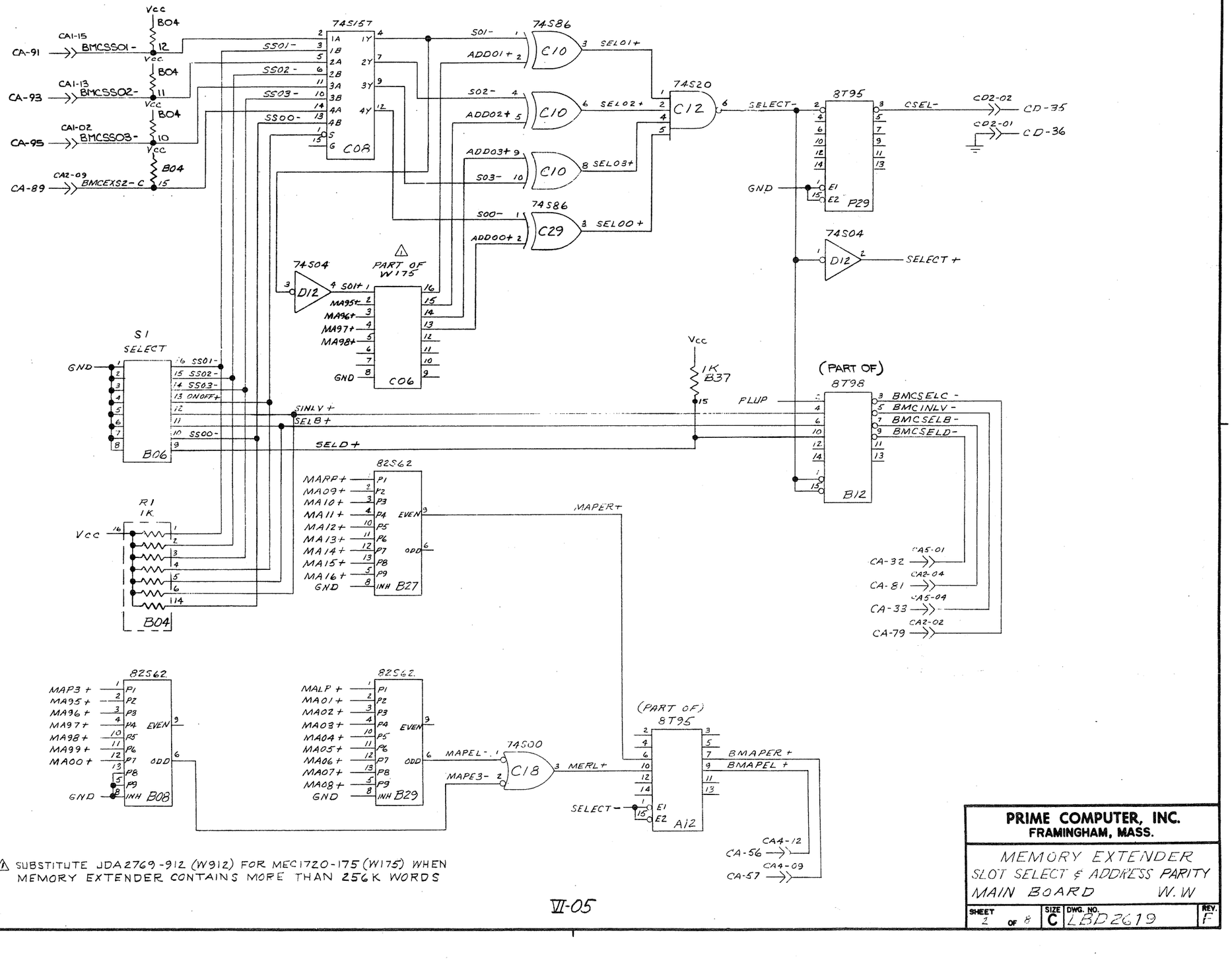
REVISION LEVEL

MATERIAL	DWN. Leslie 1/26/76	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK J. P. McManus 4/25/76	REVISION STATUS SHEET MEMORY EXTENDER MAIN BOARD W.W	
	ENG. Jon Gosselin 6/25/76		
	APPRD Bob McSweeney 6/30/76		
	USED ON 7050-901	SCALE	SIZE C DWG. NO. LBD2619 REV. H
	NEXT ASSY ESA2062-901	SHEET 1 OF 8	

LBD2619 H

VI-04

1-74



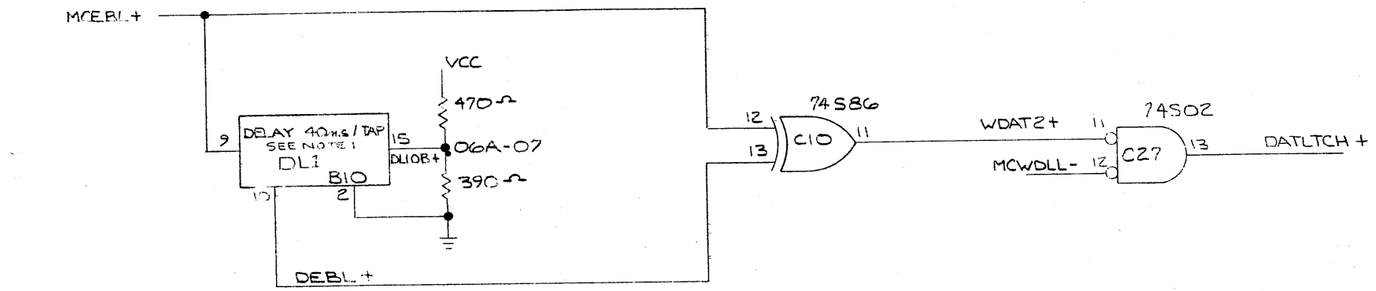
⚠ SUBSTITUTE JDA2769-912 (W912) FOR MEC1720-175 (W175) WHEN MEMORY EXTENDER CONTAINS MORE THAN 256K WORDS

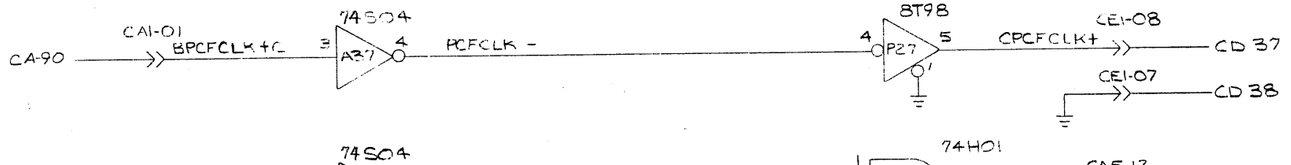
PDF-003

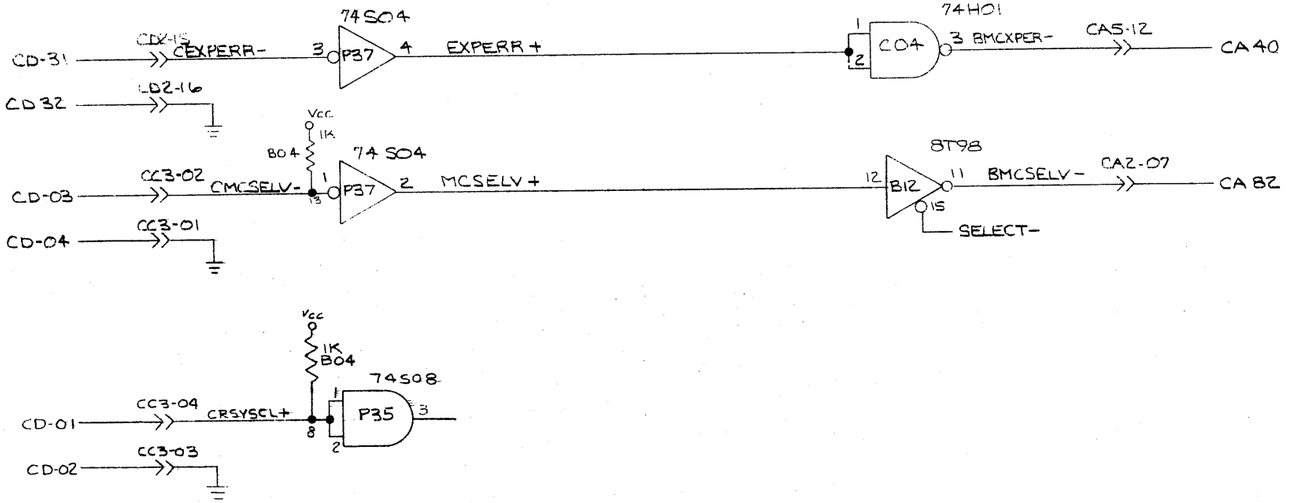
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY EXTENDER
SLOT SELECT & ADDRESS PARITY
MAIN BOARD W.W

SHEET	SIZE	DWG. NO.	REV.
2 OF 8	C	LBD2619	F







NOTES:
1. PIN 1 OF DELAY LINES GOES INTO PIN 9 OF SOCKET.

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

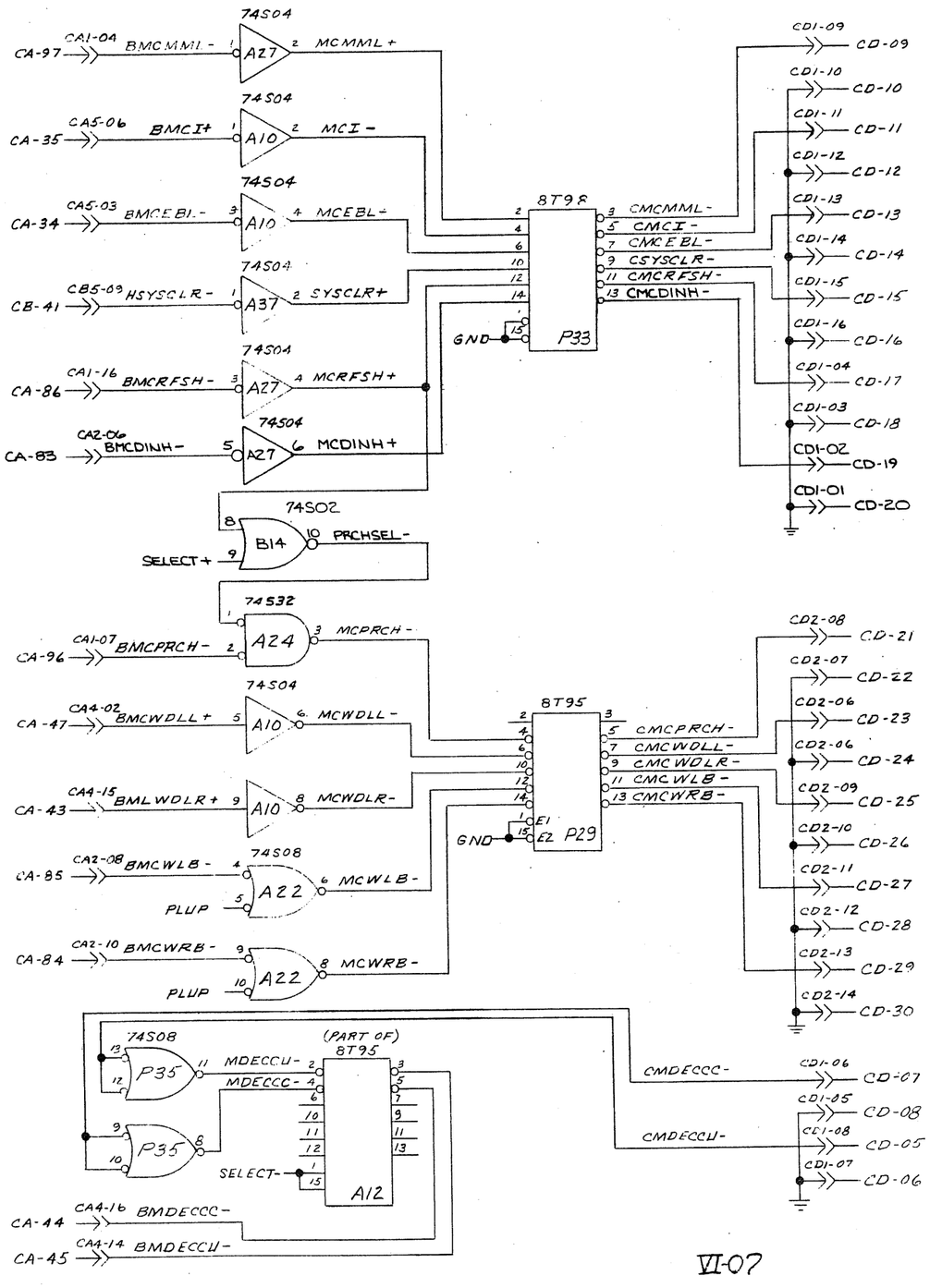
DATA LATCH & BMCSELV-

MAIN BOARD W.W.

SHEET 3 OF -
SIZE C
DWG. NO. LBD2611
REV. 1

PDF-003

PRIME COMPUTER, INC.



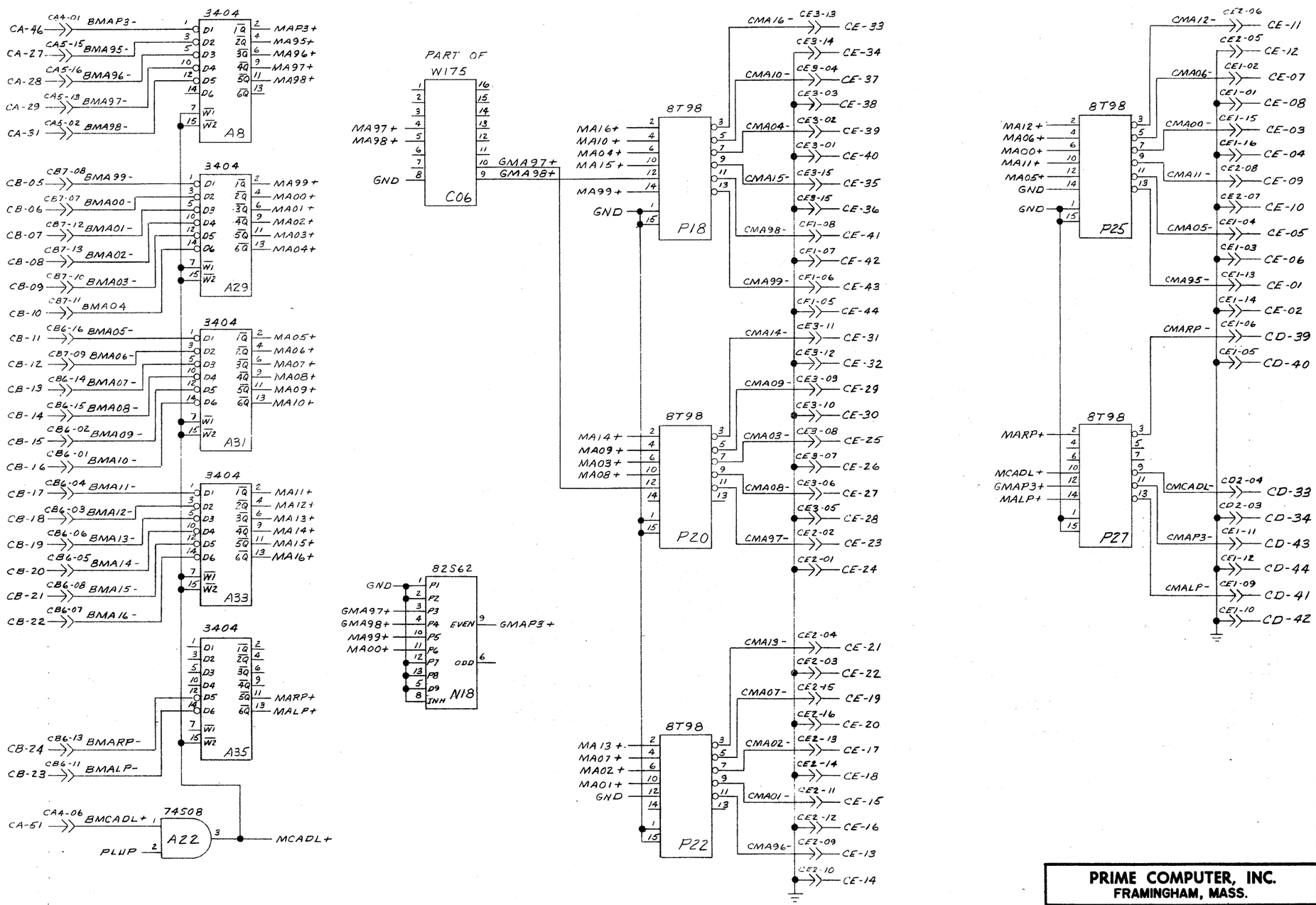
VI-07

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY EXTENDER
CONTROL LINES
MAIN BOARD W. W.

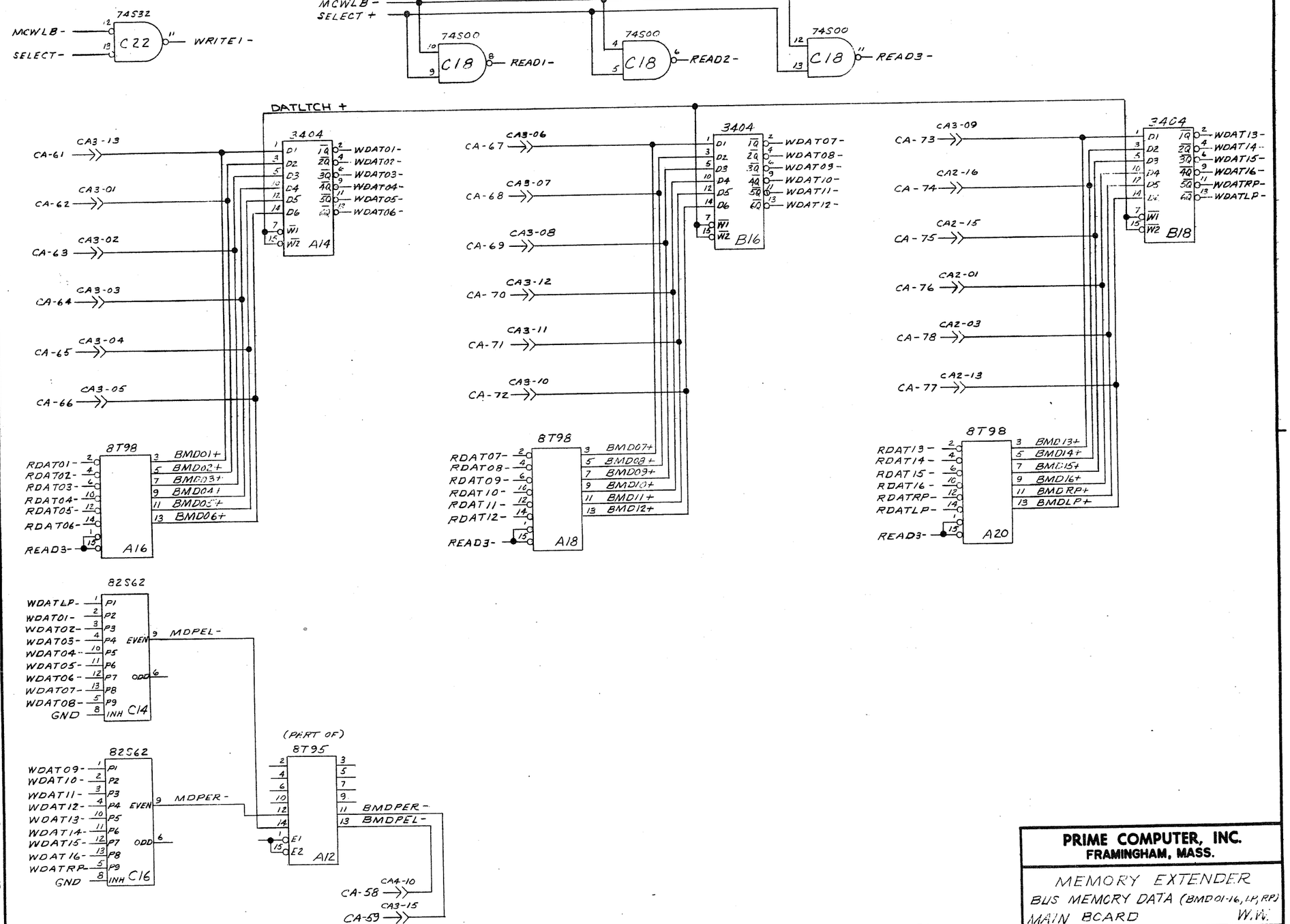
SHEET 4 OF 8 | SIZE C | DWG. NO. LBD2619 | REV. D

PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
MEMORY EXTENDER ADDRESS MAIN BOARD W.W			
SHEET 5 OF 8	SIZE C	DWG. NO. 1.BD2619	REV. E

PDF-003



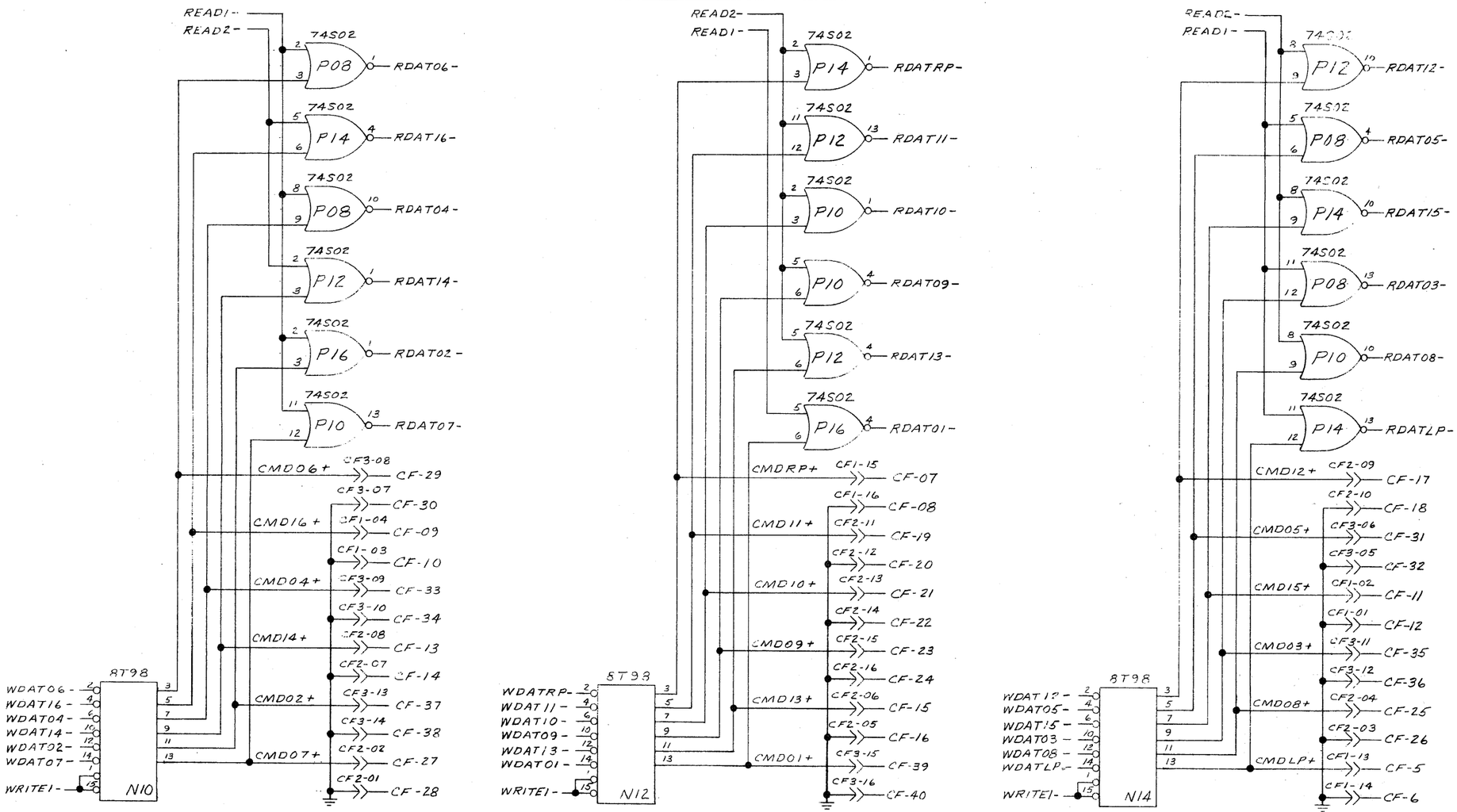
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY EXTENDER
BUS MEMORY DATA (BMD01-16, LP, RP)
MAIN BOARD W.W.

SHEET 6 OF 8 | SIZE C | DWG. NO. L.E. 2619 | REV. C

PDF-003

PRIME COMPUTER, INC.

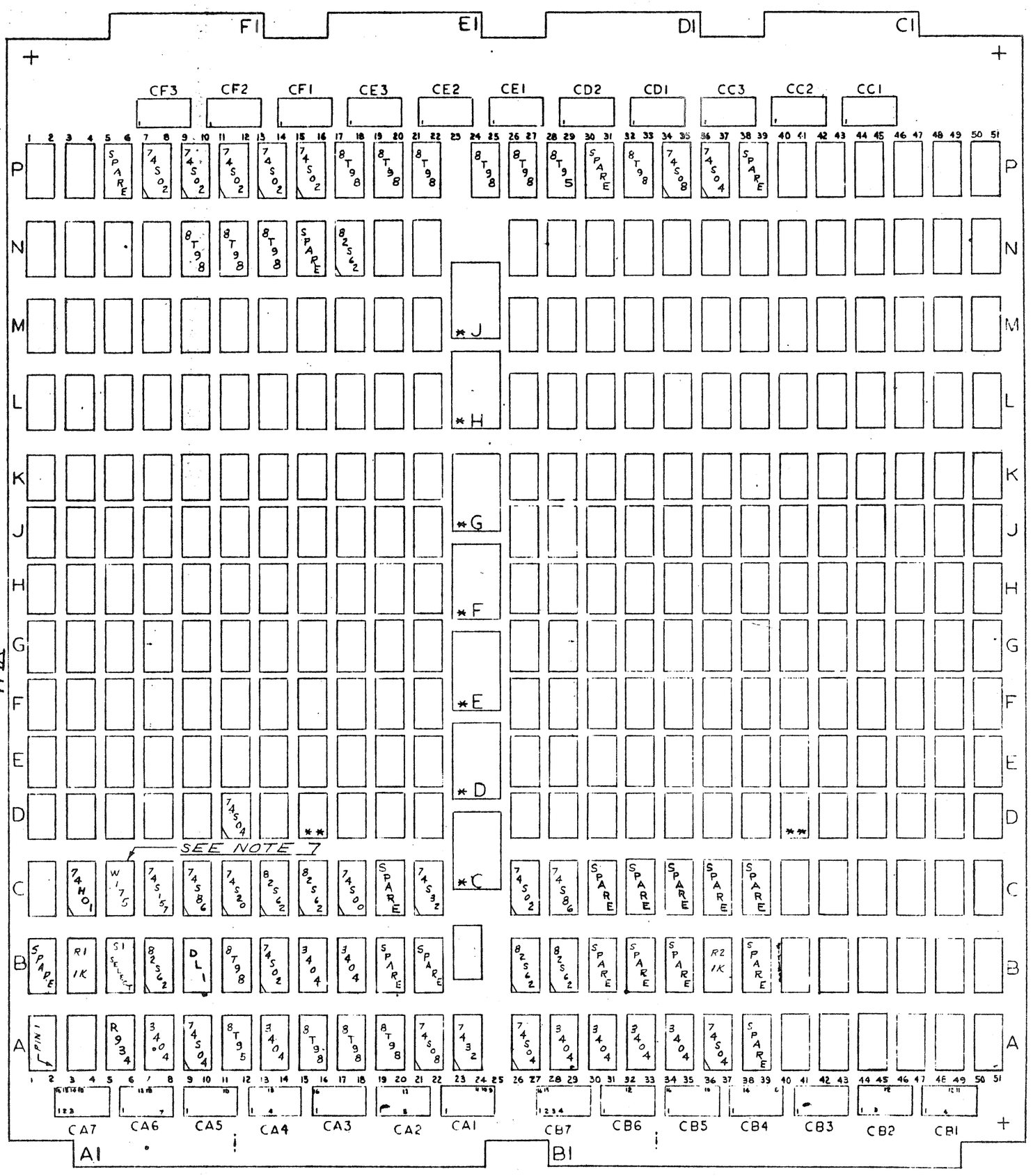


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY EXTENDER
CABLE MEMCRY DATA
MAIN BOARD W,W

SHEET 7 OF 8 | SIZE C | DWG. NO. LBD2619 | REV. A

PDF-003



COMPONENT SIDE

NOTES:

1. STANDARD I/D DIP SITES HAVE PROPER GND & VCC ETCH (ROW A & B)
2. ROW D & K HAVE GND & VCC ETCHED FOR 14 PIN DIPS (ie 7 IS GND & 14 IS VCC)
3. ALL OTHER ROWS (EXCEPT DIP SITES WITH *) HAVE GND & VCC ETCH FOR 16 PIN DIPS (ie 8 IS GND & 16 IS VCC)
4. ** MOUNTING HOLE AT DIP SITES 16 D & 41 D
5. PIN 1 IS LOCATED AT LOWER RIGHT
6. ⌊ = 14 PIN DIP
7. SUBSTITUTE JDA 2769-912 (W912) FOR MEC 1720-175 (W175) WHEN MEMORY EXTENDER CONTAINS MORE THAN 256K WORDS

DWN Luter 6/3/76	PRIME COMPUTER INC. NATICK, MASS.	
CHK		
ENG.	MEMORY EXTENDER	
APPRD	DIP ALLOCATION UNIVERSAL BOARD	
	MAIN BOARD WW	
USED ON 7050-901	SCALE NONE	SIZE C — DWG. NO. LBD 2619 — REV. F
NEXT ASSY	SHEET 8 OF 8	

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
	A	A	-	A	A	A	A	A																																	
	B	B	A	F	B	B	B	B																																	
	C		C																																					
	D	C																																						
	E	D	D						C																															
	F		E																																					

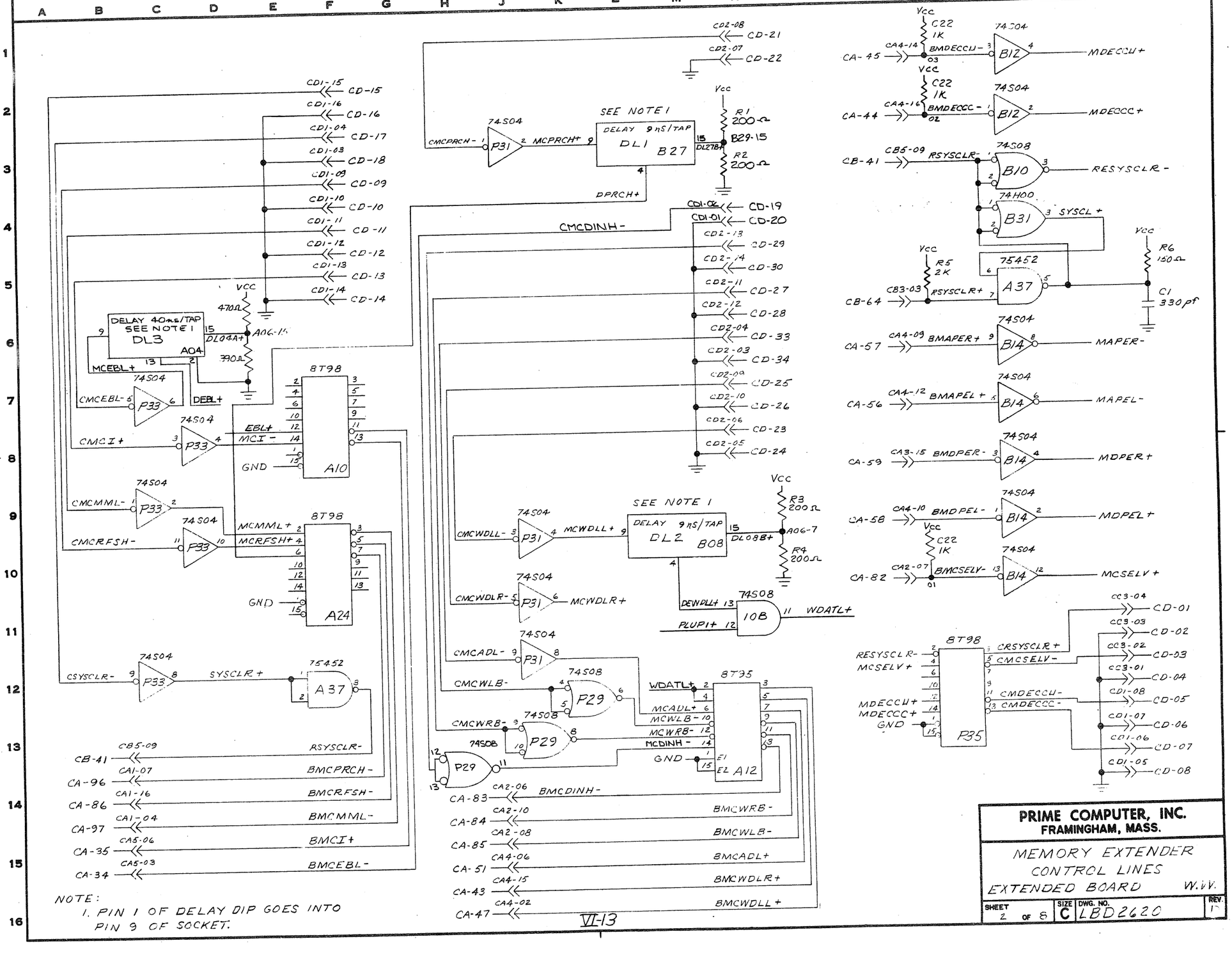
DATE	ENGINEERING CHANGE NOTICES
06-25-76	RELEASED
9-7-76	REVISED PER ECR 1892 W.L. TO REV 1. ADDED SHEET #3
12/10/76	WIRE LIST TO REV 2 REVISED PER ECR 1965
12/14/76	WIRE LIST TO REV 3 SHEET 2 ZONE 2-5 ADDED 2 RESISTORS (1K, M27) PER ECR 1990-A
1-28-77	WIRE LIST TO REV 4 REVISED PER ECR 2019
1-31-77	REVISED PER ECR 2027-A

LTR	DATE	REVISION	DR.	CK.
			J.T.S.	J.S.
			J.E.P.	J.S.
			J.T.S.	J.S.
			J.T.S.	J.S.
				J.S.
				J.S.

REVISION LEVEL

DWG. NO. LBD2620 REV. F

MATERIAL	DWN Leslie 5/26/76	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK J. E. P. James 6/25/76	REVISION STATUS SHEET MEMORY EXTENDER EXTENDED BOARD W.W.
	ENG. Jon Hoobler 6/25/76	
	APPRD John MacQuarrie 6/30/76	
	USED ON 7050-901	SCALE
	NEXT ASSY ESA 2063-901	SHEET 1 OF 8
		SIZE C DWG. NO. LBD2620 REV. F



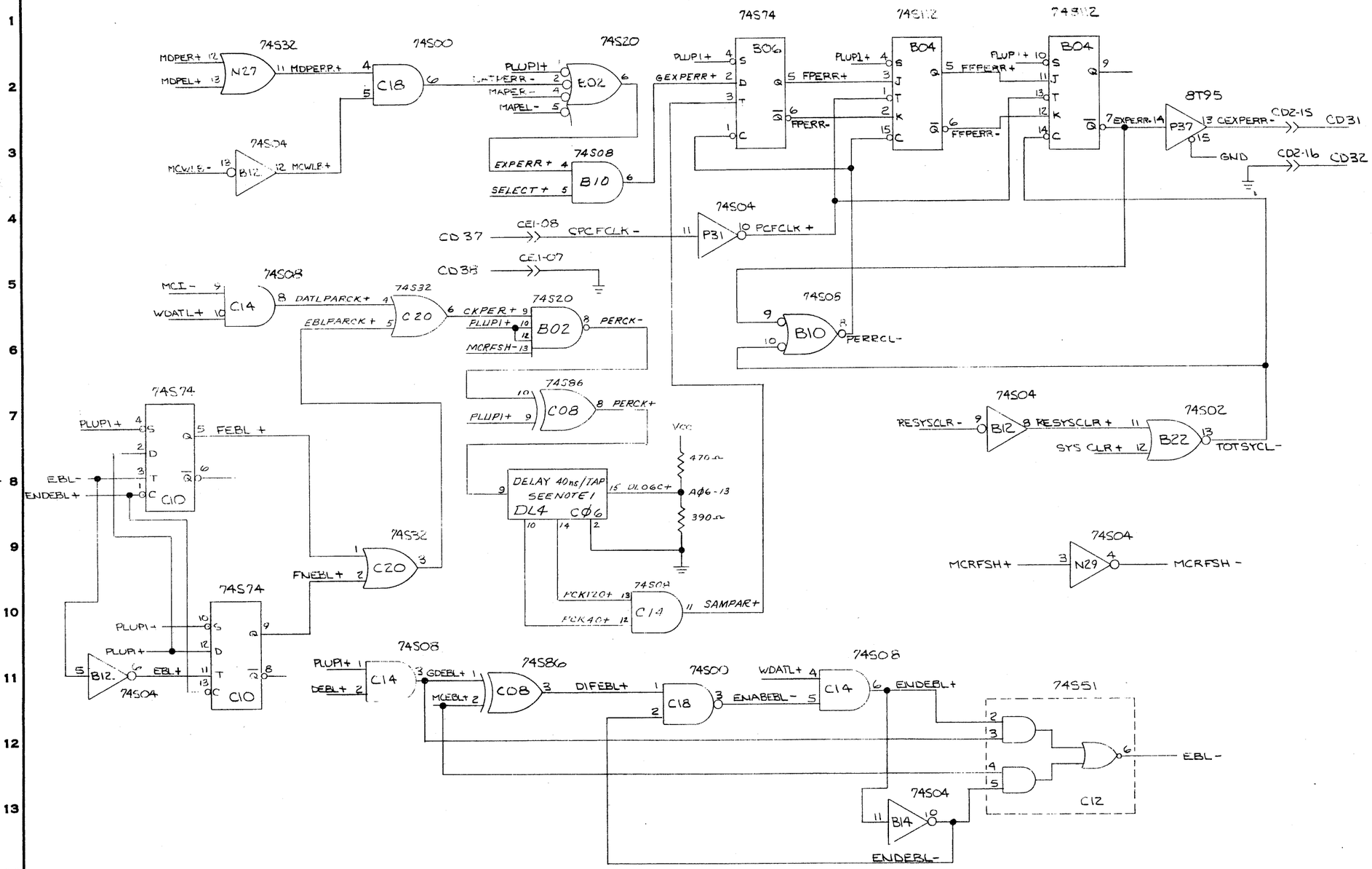
NOTE:
1. PIN 1 OF DELAY DIP GOES INTO PIN 9 OF SOCKET.

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY EXTENDER
CONTROL LINES
EXTENDED BOARD W.V.V.

SHEET 2 OF 8 | SIZE C | DWG. NO. LBD2620 | REV. 1

PDF-003



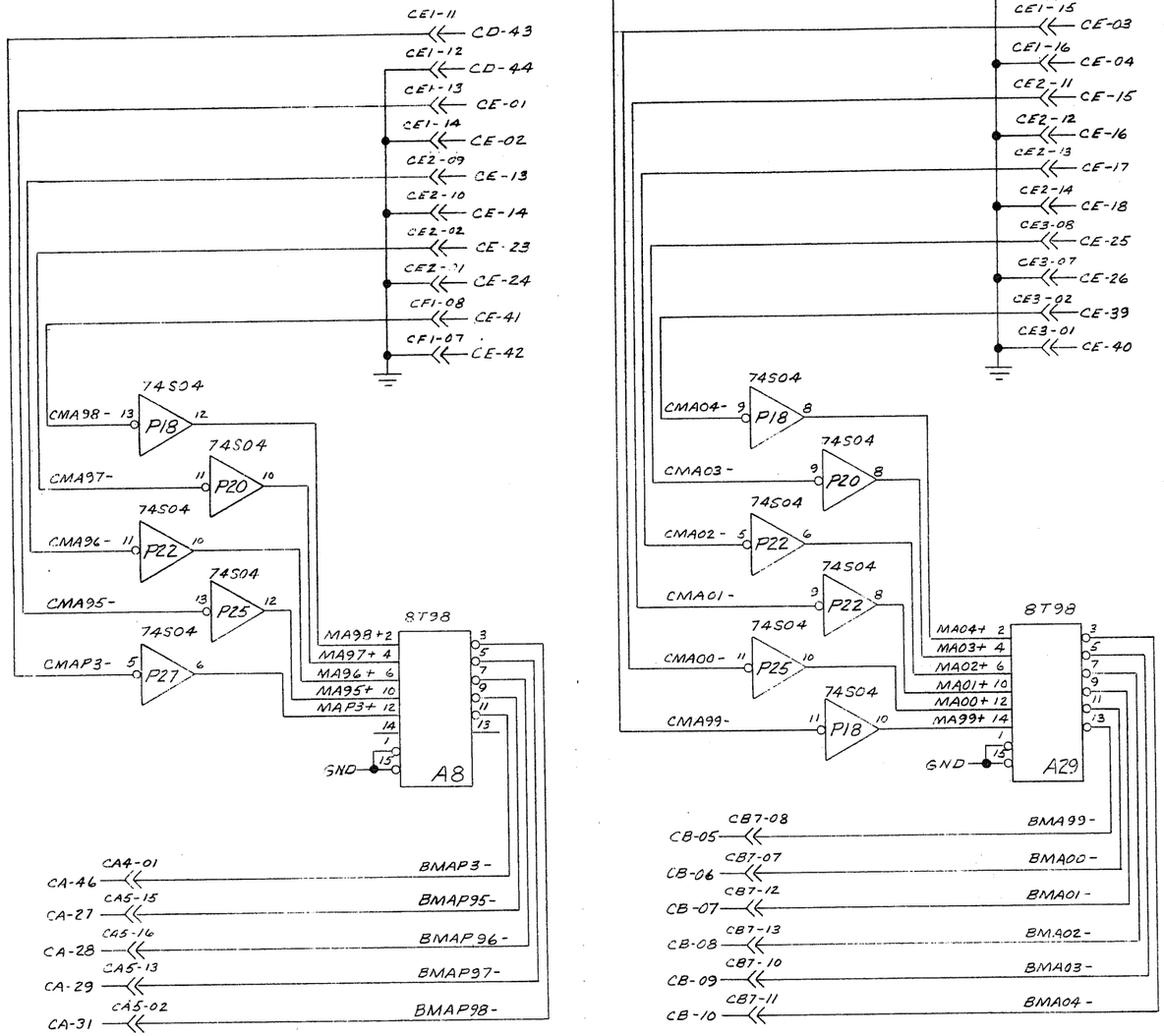
NOTE:
1. PIN 1 OF DELAY DIP GOES INTO PIN 9 OF SOCKET

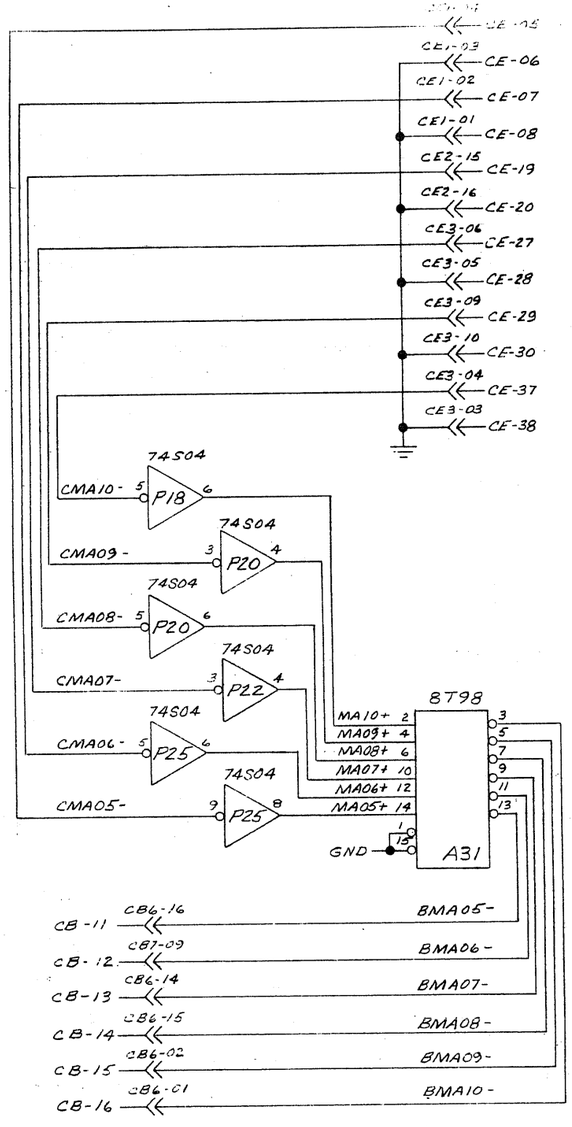
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

EXTENDED PARITY & INTERLEAVING
EXTENDED BOARD

SHEET	SIZE	DWG. NO.	REV.
3 OF 8	C	LBD2620	E

PDF-003



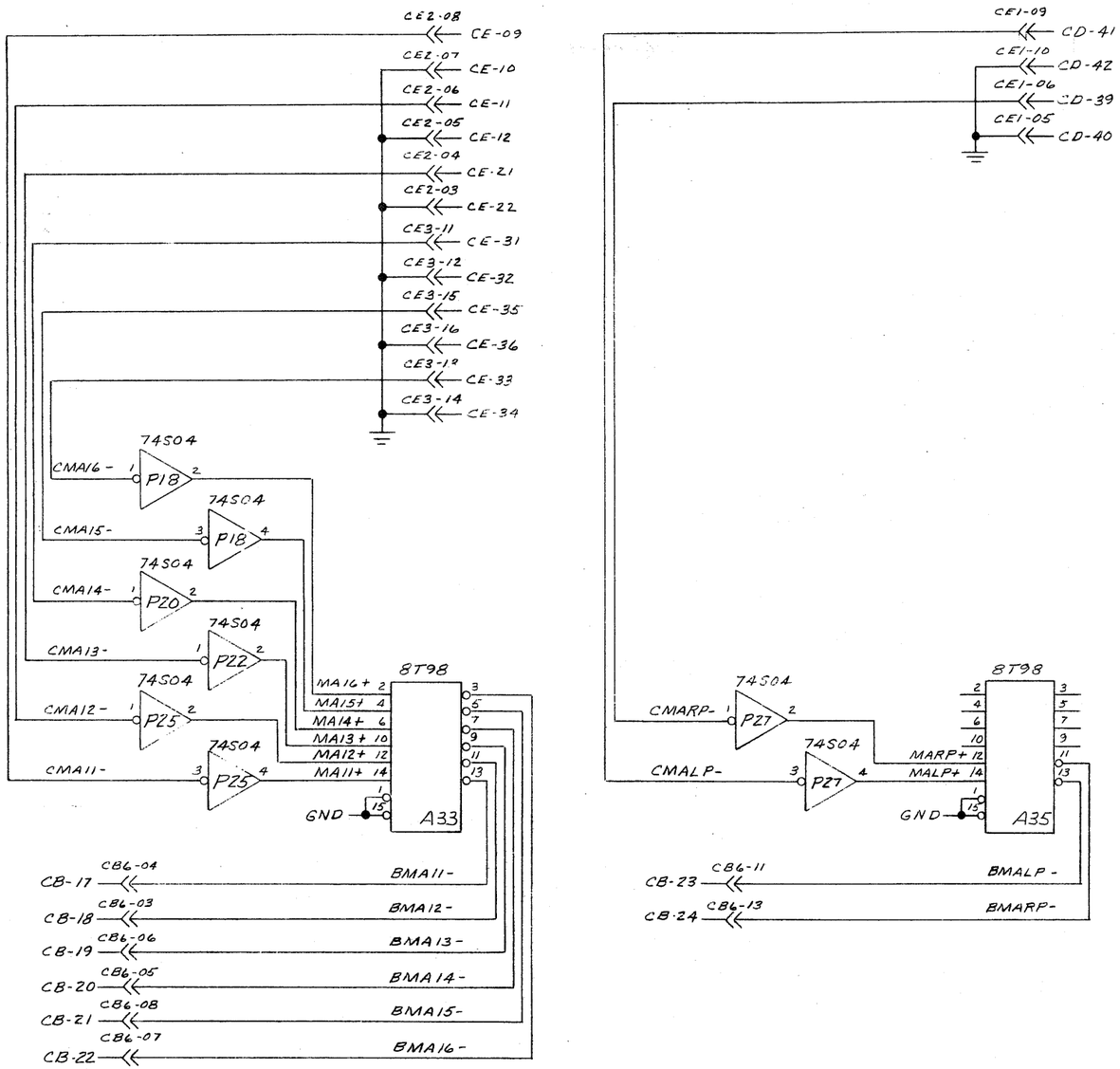


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY EXTENDER
ADDRESS (BMA 95-10, P3)
EXTENDED BOARD W.W.

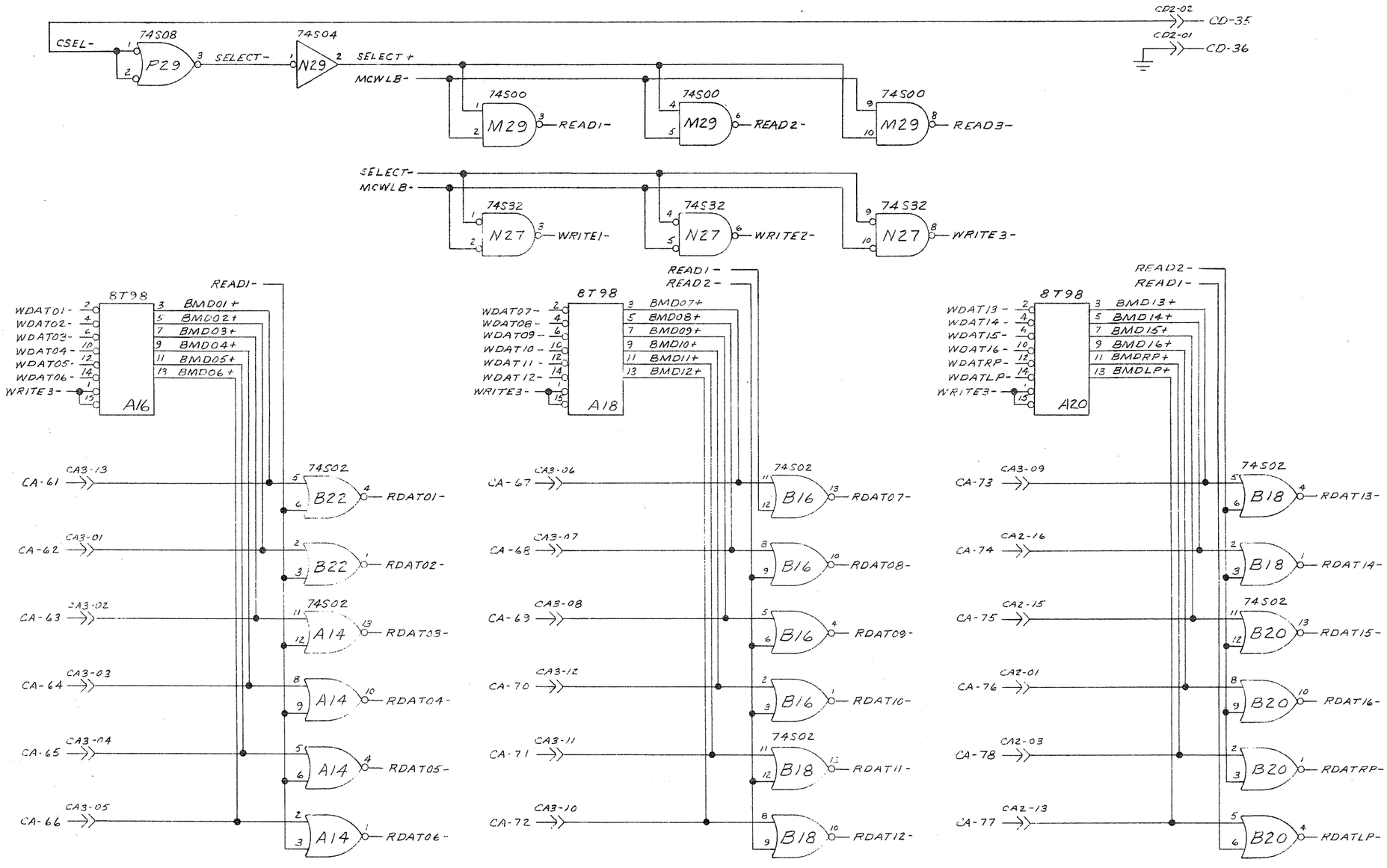
SHEET	SIZE	DWG. NO.	REV.
7 OF 8	C	LBD2620	7

PDF-003



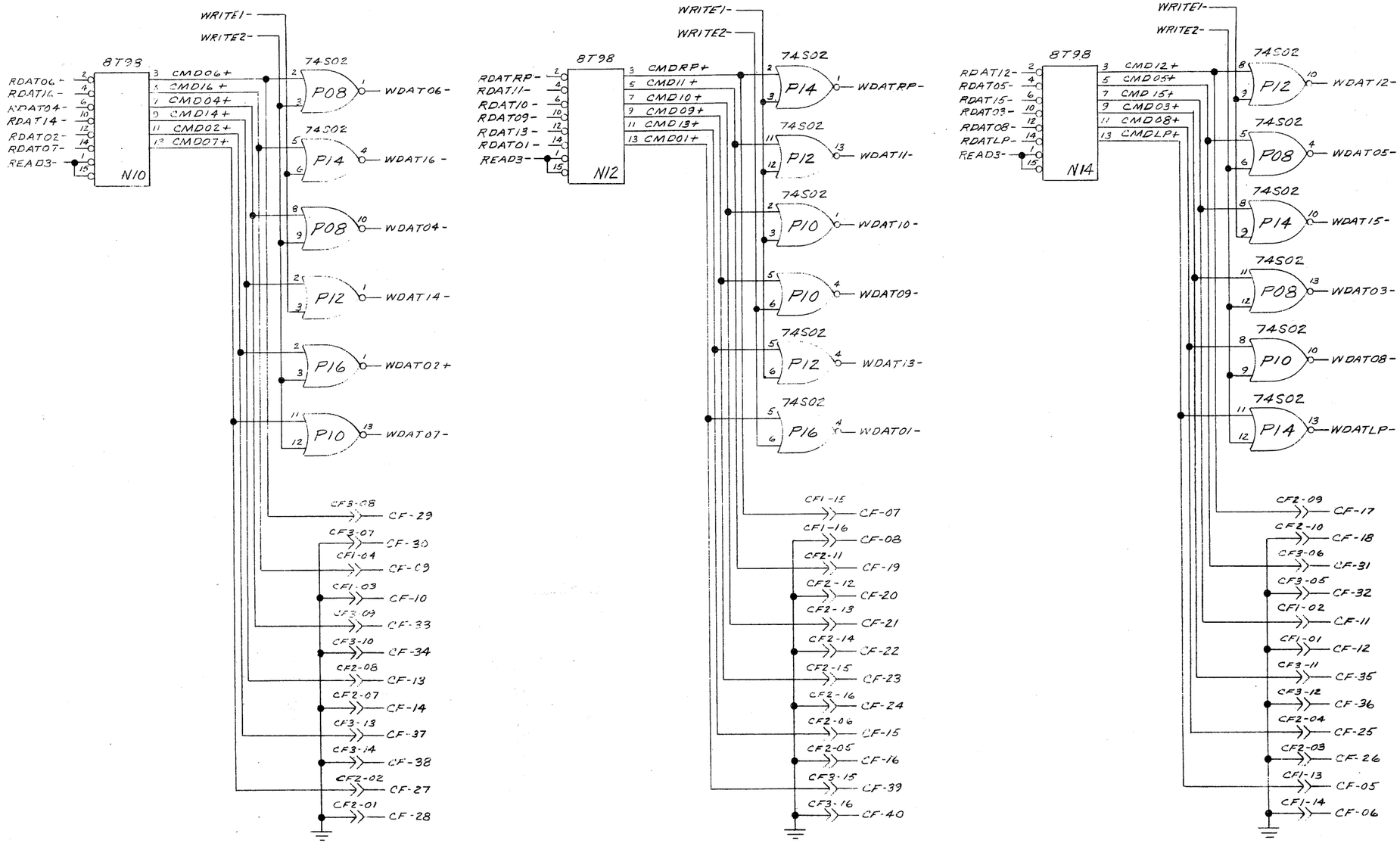
PDF-003

PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
MEMORY EXTENDER ADDRESS (BMA11-16,LA,RP) EXTENDED BOARD W.W.			
SHEET 5 OF 8	SIZE C	DWG. NO. LBD2620	REV. P



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
MEMORY EXTENDER BUS MEMORY DATA EXTENDED BOARD W.W.			
SHEET 2 OF 6	SIZE C	DWG. NO. LBD2620	REV.

PDF-003

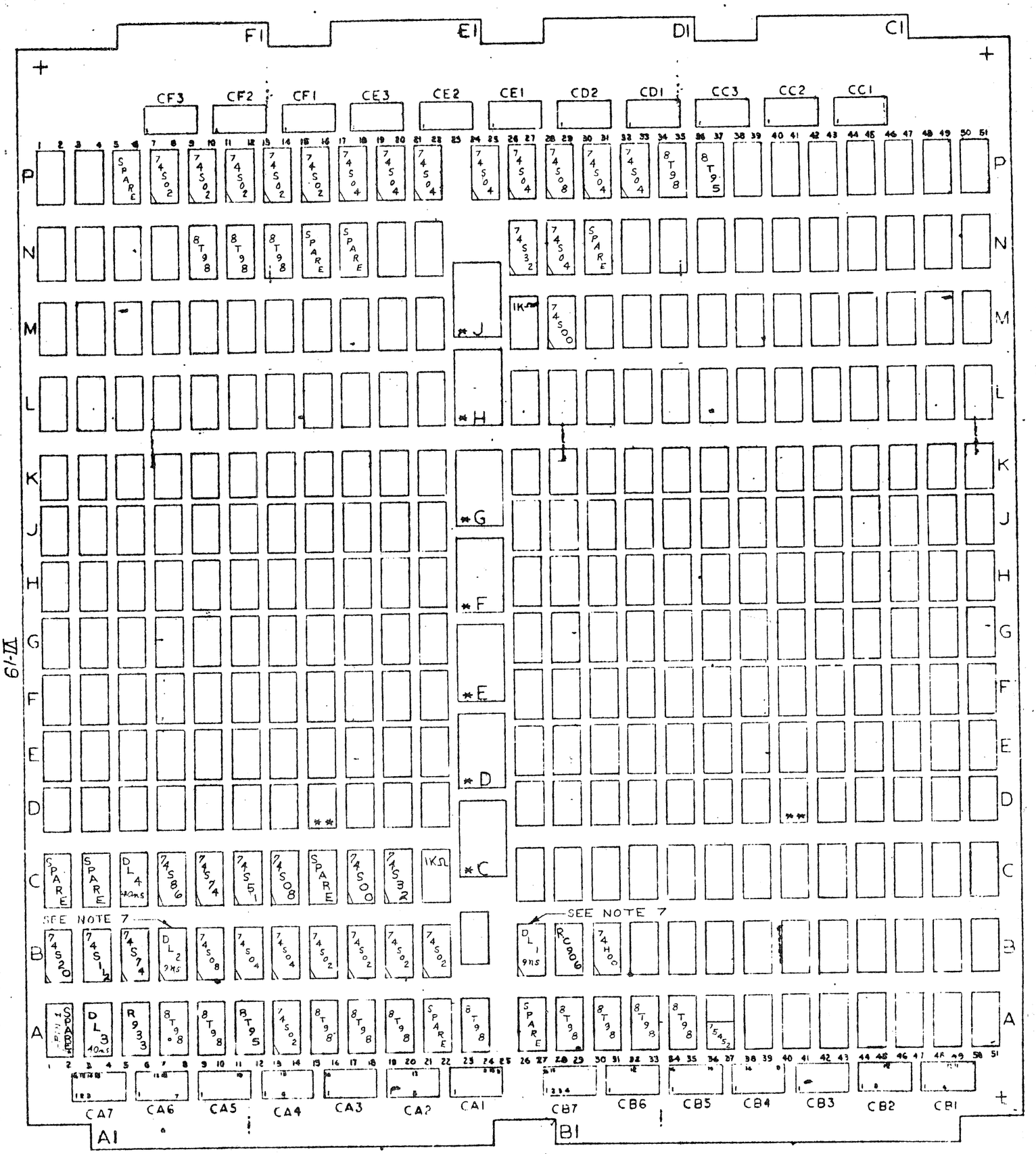


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY EXTENDER
CABLE MEMORY DATA (CMP01-16,P,RP)
EXTENDED BOARD W.W.

SHEET 1 OF 1 | SIZE C | DWG. NO. LBD2620 | REV. A

PDF-003



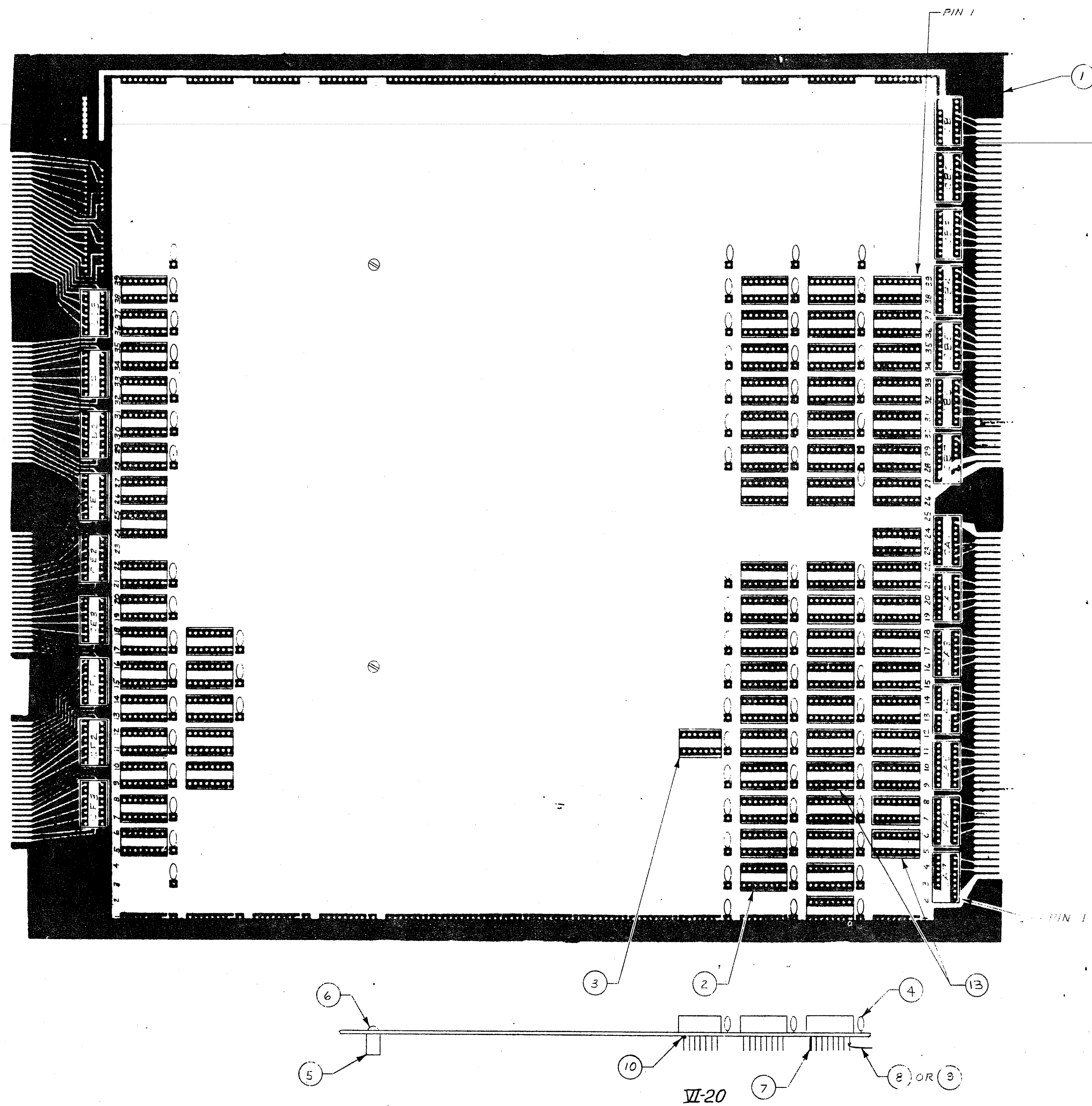
VI-19

COMPONENT SIDE

NOTES:

1. STANDARD I/O DIP SITES HAVE PROPER GND & VCC ETCH (ROW A & B)
2. ROW D & K HAVE GND & VCC ETCHED FOR 14 PIN DIPS (ie 7 IS GND & 14 IS VCC)
3. ALL OTHER ROWS (EXCEPT DIP SITES WITH *) HAVE GND & VCC ETCH FOR 16 PIN DIPS (ie 8 IS GND & 16 IS VCC)
4. ** MOUNTING HOLE AT DIP SITES 16 D & 41 D
5. PIN 1 IS LOCATED AT LOWER RIGHT
6. L = 14 PIN DIP
7. PIN 1 OF DELAY DIP GOES INTO PIN 9 OF SOCKET.

DRAWN Lester 9/3/76	PRIME COMPUTER INC. NATICK, MASS.
CHK'D	MEMORY EXTENDER
APVD	DIP ALLOCATION UNIVERSAL BOARD
MFG APVL	EXTENDED BOARD W.W.
LAYOUT BY 7650-701	SIZE C LBD2620 REV C
ASSY DWG	SHT 1 OF 3



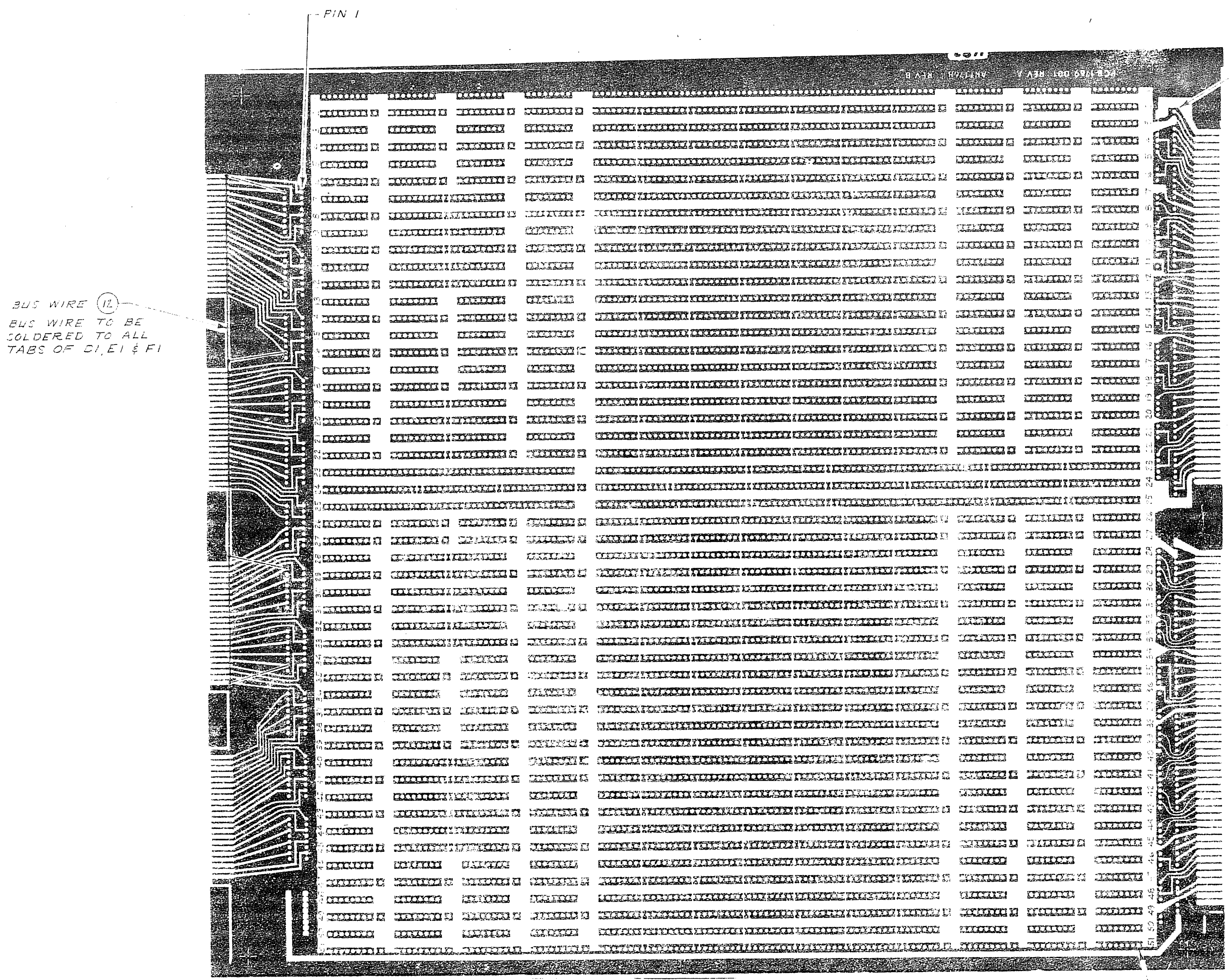
M	LTR	DATE	REVISION	DR.	CK.
	A	[illegible]	[illegible]	[illegible]	[illegible]
	B	[illegible]	[illegible]	[illegible]	JS
	C	[illegible]	[illegible]	VTS	JS
	D	[illegible]	[illegible]	VTS	JS
	E	[illegible]	WIRE [illegible] REV A PER ECR 1990	VTS	JS
	F	[illegible]	WIRE [illegible] TO REV B PER ECR 2027A	[illegible]	JS
	G	3/19/77	WIRE LIST [illegible] REV G PER ECR 2070A	[illegible]	JS

NOTES:
1. SEE SHEET 2 FOR JUMPERS
2. SEE ECB2631-001 FOR ETCH CUTS

MATERIAL: SEE BOM	DWN [illegible]	PRIME COMPUTER, INC. FRAMINGHAM, MASS.
UNLESS OTHERWISE SPECIFIED: REMOVE ALL BURRS AND SHARP EDGES; DIMENSIONS ARE IN INCHES; TOLERANCES: .XX .XXX ANGLES	CHK [illegible] 6/[illegible]/76	P.C. BOARD SOCKET ASSY MAIN BOARD MEMORY EXTENDER (W.W)
	ENG. [illegible]	
	APPRD [illegible]	SIZE D, DWG NO. ESA2042-901, REV G

ESA2042-901 G

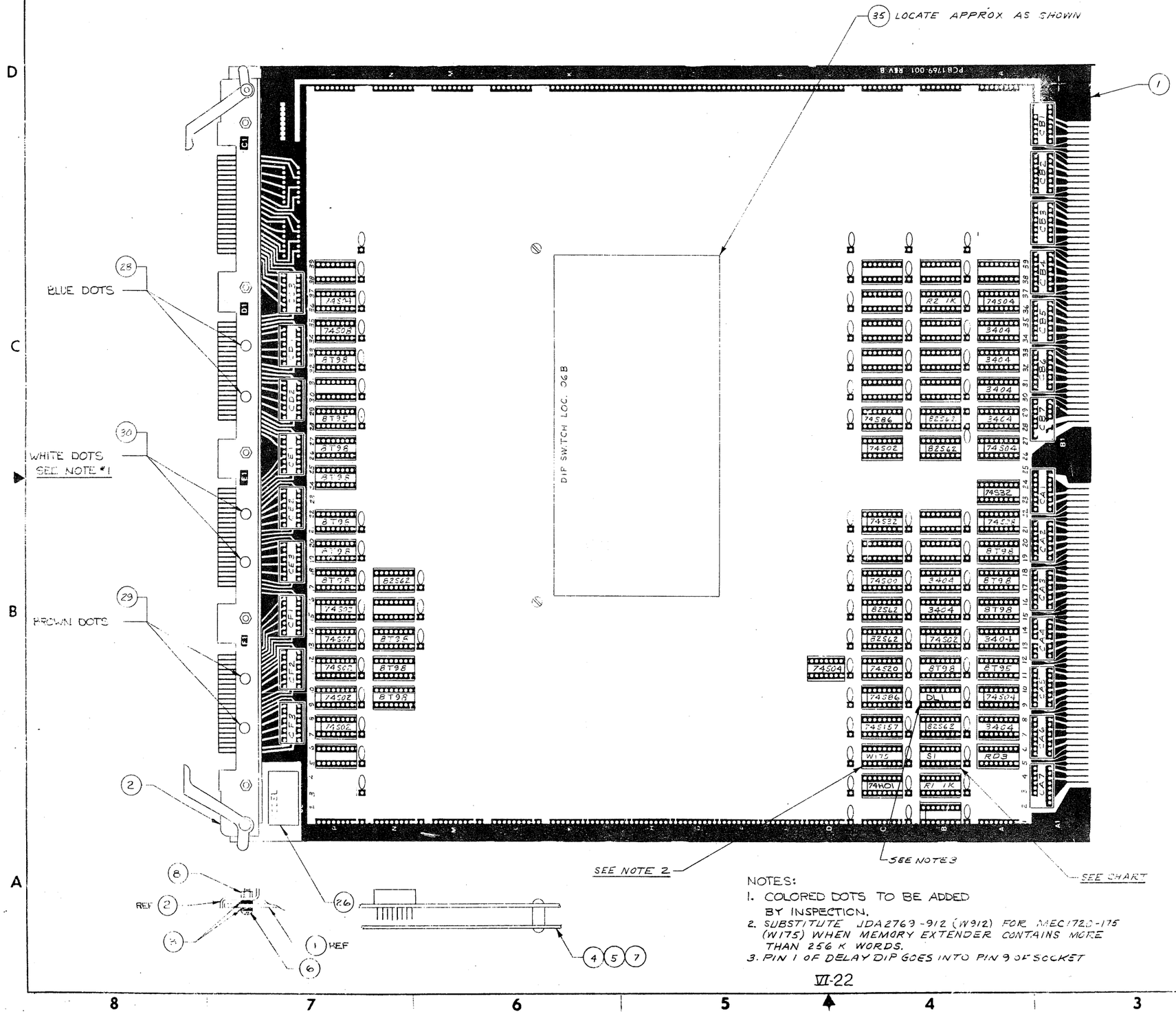
M	LTR	DATE	REVISION	DR.	CK.



SOLDER SIDE

MATERIAL: SEE BOM	DWN	COMPUTER, INC. MASS
REMOVE ALL ... AND SHARP EDGES. DIMENSIONS ARE IN INCHES. TOLERANCES: .XX .XXX	CHK	MAIN BOARD MEMORY EXTENDER
	ENG	
	APPRD	SIZE D · DWG NO. · REV G

M	LTR	DATE	REVISION	DR.	CK.



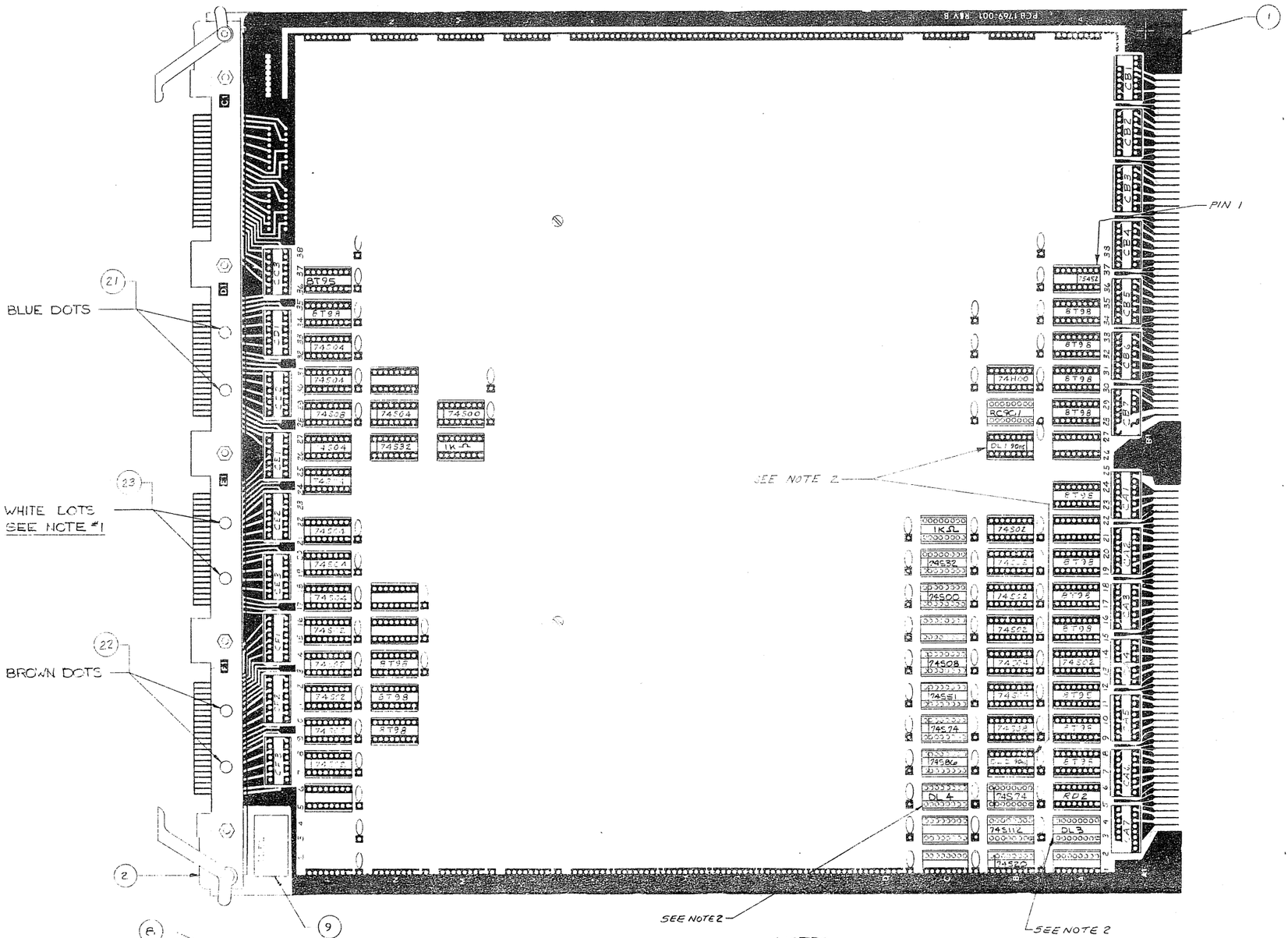
SWITCH	FUNCTION
S1	SLOT SELECT, BMCINLV, BMCSELB SELECT.

NOTES:

1. COLORED DOTS TO BE ADDED BY INSPECTION.
2. SUBSTITUTE JDA2763-912 (W912) FOR MEC1720-175 (W175) WHEN MEMORY EXTENDER CONTAINS MORE THAN 256 K WORDS.
3. PIN 1 OF DELAY DIP GOES INTO PIN 9 OF SOCKET

MATERIAL: SEE BOM	DWN: [illegible] 4/11	COMPUTER INC.
	CHK: [illegible] 4/11	MAIN BOARD ASSY
	APVD: [illegible] 4/11	MEMORY EXTENDER (WW)
	SIZE: D	DWG NO: 2082-901 REV: [illegible]

M	LTR	DATE	REVISION	DR.	CK

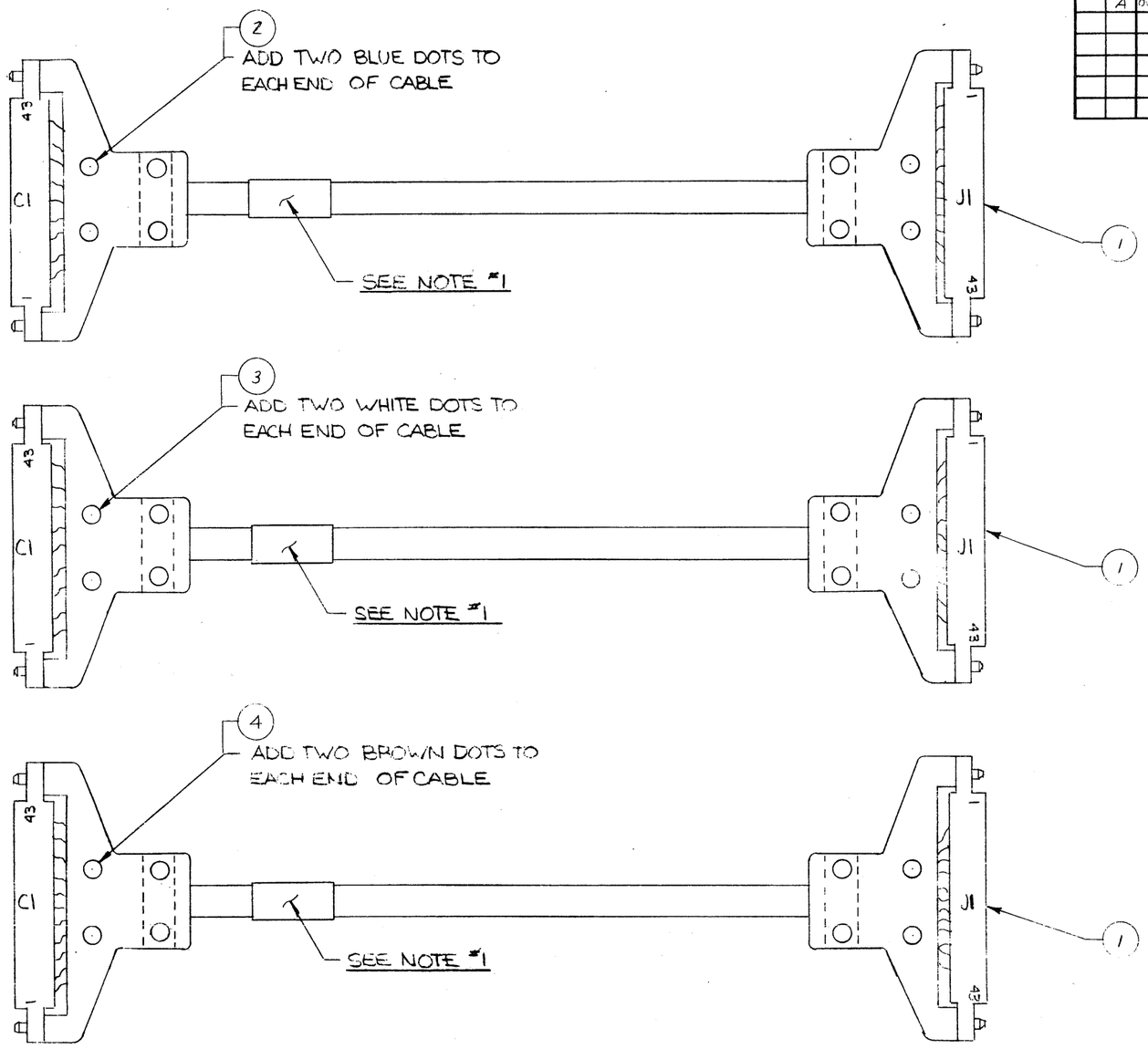


NOTES:
1. COLORED DOTS TO BE ADDED BY INSPECTION.
2. PIN 1 OF DELAY DIP GOES INTO PIN 9 OF SOCKET.

MATERIAL

		COMPUTER, INC.
		MASS
		EXTENDED BOARD ASSY
		MEMORY EXTENDER (M.W.)
		D 1769 001 F

M	LTR	DATE	REVISION	DR.	CK.
	A	10 25 76	RELEASED	G.	



NOTES:
1. INSPECTION IS TO REMOVE PART NUMBER LABEL & INSERT THREE CABLES IN A BAG AND LABEL CBL2642-901

VI-24

MATERIAL	DWN J.F.TRAVALINI 6-21-76	PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK J.F.Travalini 6/25/76 ENG. for Spitalli 6/29/76 APPRD R.F. McCarthy 6/28/76	CABLE SET MEMORY EXTENDER	
	USED ON NEXT ASSY 7050-901	SCALE — SHEET 1 OF 1	SIZE C DWG. NO. CBL2642-901 REV. A

DWG. NO. CBL2642-901 REV. A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lebo 6/9/76
CHK. J.B. 6/25/76
ENG. J.S. 6/25/76
APPRD. JAM 6/30/76
STANDARD COST _____ DATE _____

TITLE: EXTENDED BD ASSY
MEMORY EXTENDER (W.W.)

BOM 2083 **-XXX** REV. F
NHA: 7050-901 SHT. 1 OF 2

REV.	ECN	CK	REV.	ECN	CK
A	REL	J.S.	E	1990	JS
B	1892	J.S.	F	2019	JS
C	1965	JS			
D	1989-A	JS			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	ESA2043-901	1								P.C. BOARD SOCKET ASSY	(A) (D) (E)
2	C	MEC0587	1								STIFFENER ASSY	
3		MEC0356	10								WASHER, FLAT FIBER #4	(B)
4	A	MEC0412	4								STANDOFF, PIN FIELD GUARD	
5	C	MEC0270	1								PIN FIELD GUARD	
6		MEC0303-005	5								SCREW, PAN HD #4-40 x 5/16 LG	
7		MEC0309-004	10								SCREW, RD HD NYLON #4-40 x 5/16 LG	
8		MEC0388-002	5								NUT, SELF LOCKING	
9	A	MEC0292	1								LABEL, MODEL & SERIAL NO.	
10	B	MEC2370-001	1								LABEL, ECN LOG	
11		ICD0025	1								74H00	
12		ICD0065	1								75452	
13		ICD0085	2								74S00	(B)
14		ICD0086	10								74S04	
15		ICD0112	2								8T95	(B)
16		ICD2333	10								74S02	
17		ICD2334	3								74S08	(B)
18		ICD2338	2								74S32	(B)
19		ICD2581	14								8T98	
20		MEC1546-001	2								DELAY LINE 200Ω, 200NS AT 40NS	DL3, DL4 (B)
21		MFC2648-003	A/R								QUICK-DOTS, COLOR CODING (BLU)	
22		MEC2648-004	A/R								QUICK-DOTS, COLOR CODING (BR)	

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PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lebo 6/9/76
CHK. J.B. 6/25/76
ENG. J.S. 6/25/76
APPRD. JAM 6/30/76
STANDARD COST _____ DATE _____

TITLE: EXTENDED BD ASSY
MEMORY EXTENDER (WW)

BOM 2083 **-XXX** REV. F
NHA: SHT. 2 OF 2

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
23		MEC2648-011	A/R								QUICK-DOTS, COLOR CODING (WHT)	
24		MEC1546-004	2								DELAY LINE 100Ω 90ns @ 9 ns / TAP	DL1-DL2 (B)
25		ICD0071	2								74S74	(B)
26		ICD0072	1								74S112	(B)
27		ICD2336	1								74S20	(B)
28		ICD2340-	1								74S51	(B)
29		ICD0097	1								74S86	(B)
30		RESC0250-102	2								RESISTOR 16PIN 2% 1KΩ	(B) (E)
31		RCA2827-901	1								RESISTOR/CAP ASSY RC901	(B)
32		RDA2820-902	1								RESISTOR DIP ASSY RD2	(B)

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lebo 6/4/76
CHK. J.B. 6/25/76
ENG. J.S. 6/25/76
APPRD. JAM 6/30/76
STANDARD COST _____ DATE _____

TITLE: MAIN BOARD ASSY
MEMORY EXTENDER (WW)

BOM 2082 **-XXX** REV. H
NHA: 7050-901 SHT. 1 OF 2

REV.	ECN	CK	REV.	ECN	CK
A	REL	J.S.	D	1989-A	JS
B	1892	JS	E	1990/2019	JS
B1	1955	J.S.	F	2019	JS
C	1965/1980	JS	G	2027-A	JS

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	ESA2062-901	1								P.C. BOARD SOCKET ASSY	(A) (D) (E)
2	C	MEC0587	1								STIFFENER ASSY	
3		MEC0356	10								WASHER, FLAT FIBER #4	(B)
4	A	MEC0412	4								STANDOFF, PIN FIELD GUARD	
5	C	MEC0270	1								PIN FIELD GUARD	
6		MEC0303-005	5								SCREW, PAN HD #4-40 x 5/16 LG	
7		MEC0309-004	10								SCREW, RD HD NYLON #4-40 x 5/16 LG	
8		MEC0388-002	5								NUT, SELF LOCKING	
9												(B)
10		ICD0075	1								74S157	
11		ICD0079	6								82S62	
12		ICD0085	1								74S00	
13		ICD0086	5								74S04	
14		ICD2336	1								74S20	(A)
15		ICD0097	2								74S86	(A)
16		ICD0112	2								8T95	(A)
17		ICD2333	7								74S02	
18		ICD2334	2								74S08	
19		ICD2338	2								74S32	(B)
20		ICD2581	13								8T98	
21		ICD90017	8								3404	
22												(B1)

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PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Lebo 6/4/76
CHK. J.B. 6/25/76
ENG. J.S. 6/25/76
APPRD. JAM 6/30/76
STANDARD COST _____ DATE _____

TITLE: MAIN BOARD ASSY
MEMORY EXTENDER (W.W.)

BOM 2082 **-XXX** REV. H
NHA: 7050-901 SHT. 2 OF 2

REV.	ECN	CK	REV.	ECN	CK
H	2070-A	J.S.			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
23	A	MEC1720-175	1								JUMPER DIP, W175	(A)
24		RESC0250-102	2								RESISTOR NW 16 PIN 2% 1KΩ	
25		SWT2238-001	1								SWITCH, 8 POLES 16P DIP	(B1)
26	A	MEC0292	1								LABEL, MODEL & SERIAL NO.	
27	B	MEC2370-001	1								LABEL, ECN LOG	
28		MEC2648-003	A/R								QUICK-DOTS, COLOR CODING (BLU)	
29		MEC2648-004	A/R								QUICK-DOTS, COLOR CODING (BR)	
30		MEC2648-011	A/R								QUICK-DOTS, COLOR CODING (WHT)	
31		ICD0026	1								74H01	(B)
32												(B) (F)
33		MEC1546-001	1								DELAY LINE 200Ω 200ns @ 40ns TAP	DL1 (B)
34		RDA2820-903	1								RESISTOR DIP ASSY RD3	(B)
35		MEC2869-001	1								LABEL, MEMORY EXTENDER SWITCHS	(D)
36		JDA2769-912	1								JUMPER DIP ASSY W912	(E)

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PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Leslie 5/28/76
CHK. W. Lyon 5/25/76
ENG. J.S. 6/25/76
APPRD. JHM 6/30/76

TITLE: MEMORY EXTENDER 115V, 60HZ

STANDARD COST _____ DATE _____

BOM 7050 -XXX REV. H
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	JS.	E	1992/2011	JS
B	1892	JS	F	2019	JS
C	1965/1980	JS	G	2327-H	JS
D	1989	JS	H	2070-A	JS

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	2082-901	1								P.C. BOARD (W.W.) MAIN BOARD	A C D E G H
2	D	2083-901	1								P.C. BOARD (W.W.) EXTENDER BOARD	A C D E F
3	C	CBL2642-901	1								CABLE SET MEMORY EXTENDER	
4	D	1025-903	1								CHASSIS ASSY NCC P400	
5	D	1044-001	1								POWER SUPPLY, 40A, 115VAC	
	A	SPC2819	REF								SPECIFICATION MEMORY EXTENDER	E

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PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Leslie 5/28/76
CHK. W. Lyon 5/25/76
ENG. J.S. 6/25/76
APPRD. JHM 6/30/76

TITLE: MEMORY EXTENDER 230V, 50 HZ

STANDARD COST _____ DATE _____

BOM 7050-A -XXX REV. H
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	JS.	E	1992/2011	JS
B	1892	JS	F	2019	JS
C	1965/1980	JS	G	2327-A	JS
D	1989	JS	H	2070-A	JS

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	2082-901	1								P.C. BOARD (W.W.) MAIN BOARD	A C D E G H
2	D	2083-901	1								P.C. BOARD (W.W) EXTENDER BOARD	B C D E F
3	C	CBL2642-901	1								CABLE SET MEMORY EXTENDER	
4	D	1025-903	1								CHASSIS ASSY, NCC P400	
5	D	1044-A-001	1								POWER SUPPLY, 40A, 230VAC	
	A	SPC2819	REF								SPECIFICATION, MEMORY EXTENDER	E

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PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Leslie 6-21-76
CHK. J.P. 6/25/76
ENG. J.S. 6/25/76
APPRD. JHM 6/30/76

TITLE: CABLE SET MEMORY EXTENDER

STANDARD COST _____ DATE _____

BOM CBL2692 -XXX REV. A
NHA: 7050-901 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	JS.			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	C	CBL1241-005	3								CABLE UNIVERSAL	
2		MEC2648-003	A/R								QUICK-DOTS, COLOR CODING (BLU)	
3		MEC2648-011	A/R								QUICK-DOTS, COLOR CODING (WHT)	
4		MEC2648-004	A/R								QUICK-DOTS, COLOR CODING (BR)	

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PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Leslie 4/9/76
CHK. J.P. 4/9/76
ENG. J.S. 6/25/76
APPRD. 6/30/76

TITLE: P.C. BD SOCKET ASSY MAIN BOARD MEMORY EXTENDER (W.W.)

STANDARD COST _____ DATE _____

BOM ESA2062 -XXX REV. G
NHA: 2082-901 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	JS.	E	1990	JS
B	1892	JS.	F	2027-A	JS.
C	1965/1990	JS.	G	2070-A	JS.
D	1989	JS			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	PCB1769-001	1								P.C. BOARD UNIVERSAL	
2		CON0022	95								SOCKET, 16 PIN DIP	A B
3		CON0237	1								SOCKET, 14 PIN DIP	
4		CAP0546-001	74								CAP, GLASS 50V +80-20% .01 uF.	
5	A	MEC0412	2								STANDOFF, PIN FIELD GUARD	
6		MEC0309-004	2								SCREW, RD HD NYLON #4-40 x 1/4 LG	
7		MEC0159-002	1.5FT								TUBING, H.S. 1/16 I.D.	
8		WIR0616-006	A/R								WIRE, SINGLE COND #30 AWG (BLUE)	
9		WIR0616-009	A/R								WIRE, SINGLE COND #30 AWG (WHT)	
10		CON0293	24								GROUND CLIPS	E B
11		WIR0616-129	12.5'								WIRE, 30 AWG MYLNE SC TP R/W	
12		WIR1221-003	1.5'								WIRE, BUS #22 AWG	
13		CON0650-011	2								SOCKET LOW PROFILE 16 PIN	B D
		WRL2637	REF								WIRE LIST REV. 6	A E A E A B
	A	GCL2633	REF								GROUND CLIP LIST	B C
	A	MKL2632	REF								MARKER LIST	B
	D	ECB2631-001	REF								ETCH CUTS	
	C	LBD2619	REF								LOGIC BLOCK DIAGRAM	C

PDF-004A

DATE: October 27, 1976

TO: Field Engineering

FROM: John Bowne

SUBJECT: MEMORY PARITY

To answer some of the questions on the memory parity scanners for all the different revisions of software, the following charts and comments should help you find most of the parity problems:

First, a chart of all the common halts in the operating system. This chart contains the actual location of the halt instruction.

REV.	6	7	8.15	9.15	10.15	11.15	10	11
CPU						P-300	P-400	P-400
POWER FAILURE	14321	14345	15072	15226	15241	15635	31561	32451
MEMORY PARITY	14324	14350	15075	15231	15244	15640	31564	32462
MACHINE CHECK	14326	14352	15077	15233	15246	15642	31566	32464
MISSING MEMEORY MODULE	14331	14355	15102	15236	15251	15645	31571	32467
INIT PARITY		17105	65104	64040	63643	47347	54100	56115

In the process of bringing up DOSVM or PRIMOS memory parity is sometimes discovered by the routine INITO. The central processor will then halt at the location specified in the chart above according to revision of software. At this time two (2) different approaches can be taken.

1) Regardless of software revision or type of C.P. (300 or 400), by depressing the START SWITCH the BAD PAGE will be locked out by INITO and the operating system will continue to come up. If there is more than one (1) BAD PAGE, they will also be locked out.

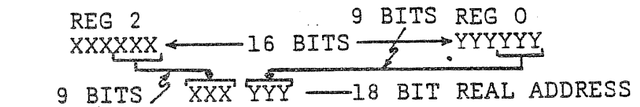
(continued)

VII-01

2) P-300 ONLY....

After the C.P. halts, fetch locations 0, 1, and 2 from the register file and record. DO NOT MASTER CLEAR.

REG 0 VIRTUAL ADDRESS
REG 1 BAD BITS
REG 2 PAGE NUMBER

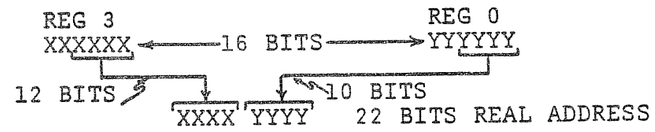


REAL ADDRESS can be formulated as shown above. Then, REG 1 should identify the BAD BIT.

2a) P-400 ONLY ....

After the C.P. halts, fetch location 0 and 3; but, make sure that all SSW are down so that you are in 300 mode.

REG 0 VIRTUAL ADDRESS
REG 3 PAGE NUMBER



(continued)

Unfortunately the P-400 INITO routine does not isolate it down to a BAD BIT, so, at this point, the memory diagnostic could be run or the page should be locked out.

MEMORY SCANNER

While running DOSVM or PRIMOS and a memory parity error is detected by the operating system, the C.P. will halt at the location specified by the chart. To try and find the offending location, run the memory scanner as follows:

Revision 7, 8, and 9 (P-300) and 10,11 (P-400).

1. MASTER CLEAR
2. Put 777 in the P counter, (location 7).
3. All SSW down.
4. Rotary switch to RUN, hit start.
5. Address DATA switch to DATA.

At this point the scanner is cycling through memory looking for the location that is bad. Wait a few minutes for the scanner to either find a bad location and cycle on it or not fine any locations and halt.

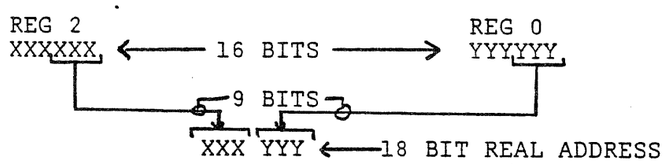
P-300	HALT	P-400	HALT
Rev. 7	16100	Rev. 10	33044
Rev. 8	16655	Rev. 11	34057
Rev. 9	17054		

If the C.P. doesn't stop it means that the scanner has detected a parity error and the address and data can now be recorded by manipulating the SSW and recording the contents of three (3) registers: 0, 2, and 4.

Revision 7, 8, and 9
P-300

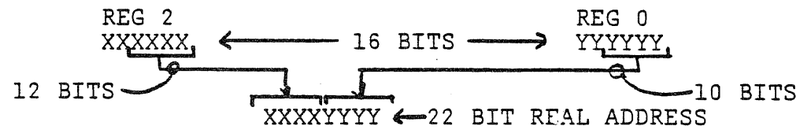
	SSW UP	CONTENTS
REG. 0	NONE	Displacement
REG. 2	15	Page Number
REG. 4	14	DATA

Revision 7, 8, and 9 (P-300)



(continued)

Revision 10 and 11 - P-400 (4-row PROM only)



Once the address has been formulated, the scanner can now be instructed to go ahead and continue to scan higher memory and try to detect more possible parity errors or halt.

Revision 7 is instructed to continue the scan by raising and lowering SSW 1. Revision 8 and 9 (P-300) and Revision 10 and 11 (P-400) can be instructed to continue by depressing a key on the system terminal.

Revision 10 and 11 - P-300*

This scanner is is slightly different from the other revisions.

1. MASTER CLEAR
2. Rotary Switch to Run, Hit Start.

At this point the scanner is running and will print out the bad pages in octal on the system terminal.

Also, printed on the system terminal is the message "STOP" FIXMMAP and PAGMAPS, WARM START".

Example of how to lock out a memory page.

Lets assume while running Revision 10.15 software, a parity error is detected and the C.P. halts at 15245 (halt instruction +1). Rotary switch to stop step, master clear, rotary switch to RUN, hit start switch twice. The system terminal prints out:

147
PARITY ERROR AT ABOVE PAGES
STOP, FIX MMAP AND PAGMPAS, WARM START

1. At this point stop the machine and fetch MMAP location:

   12000 + BAD PAGE 12000 + 147 = 12147

*See attached sheet for patch to Rev. 10 to allow scanner to work.

(continued)

Lets say location 12147 (MMAP) contains 6076.

2. Modify 12147 to 177777 (page unavailable).
3. Fetch 6076 (it should contain 10x147).
4. Modify 6076 to 0 (page not in memory).
5. Warm start (stop step, master clear, run, hit start switch twice).

The system is now operating minus the pages(s) that were locked out.

If you have any question on the scanners or memory parity, please call. Comments are also welcome.

John Bowne
Technical Support

JB/ak

MEMORY PARITY FINDER REVISION 10

SYMPTOM: THE MEMORY PARITY FINDER INDICATES MORE BAD MEMORY THAN IS ACTUALLY BAD.

PATCH:

MEMORY IMAGE (PRIMOS 3 31 USER VERSION)

LOC	CONTENTS	INST
30115	2765	JMP 765
765	104771	LDA* 771
766	201	IAB
767	102770	JMP* 770
770	30122	DAC MEM45
771	30153	DAC BADPAG

*****NOTE: THE ABOVE PATCH IS NOT FOR SMLC 31 USER VERSION*****

MEMORY IMAGE (PRIMOS 3 15 USER VERSION)

LOC	CONTENTS	INST
17055	2765	JMP 765
765	104771	LDA* 771
766	201	IAB
767	102770	JMP* 770
770	10762	DAC MEM45
771	17113	DAC BADPAG

SOURCE PATCH:

AT MEM4-2 (RMC)

```
INSERT AFTER RMC
             LDA BADPAG
             IAB
```

TO: Jim Van Beek

FR: George Dumas

DT: February 17, 1977

SJ: MEMORY UPDATES AND SPARES

Updating memories for P400 updates and/or interchanging memories for spares has become a lot more confusing than most people realize. Though still relatively simple, there are some restrictions that, although documented, are not very well known. This memo is to try to explain these restrictions.

1. P400 Updates

To update a system to a P400 and use the existing memories, the memories must be model numbers 1232-B85 (old 32K boards), 1232-B85X (old 32K boards previously modified for P400), (and/or 1232-B85Y, new 32K boards).

1232-B85 - These memories must have ECO #1757 (attached) installed. This ECO is shipped with all P400 shipments. The purpose of the ECO is to remove the grounds from the address and data latch strobes and allow the P400 to do the strobing. Once the ECO (1757) is installed, the model number should have an "X" appended to it. These memories will not size correctly in the main backplane (no upper addresses, i.e. BMA 95-98). If used in main backplane, software having size routines must be preset to only size to 256K of memory (such as PRIMOS). These memories may be used in memory extenders with no sizing problems, if the extender is configured as 256K Block. 1232-B85X memories cannot run interleaved nor do they take advantage of the P400 faster timing features.

1232-B85X - These memories are modified 1232-B85 memories and the same restrictions apply as indicated above.

1232-B85Y - These memories will run with a P400 in main memory or in extenders with no sizing restrictions. However, these memories cannot run interleaved nor do they take advantage of the P400 faster timing features. These memories may be converted to 1232-D85 (P400 memories) by changing two timing dips and setting the configuration switches per Table 1.

Location	Remove	Install
B44	MEC1720-171	MEC1720-174
B46	MEC1720-172	MEC1720-173

Table 2 shows the jumper dip wiring to rewire the dips if new dips are not available. Model numbers should be changed to 1232-D85 on these memories.

2. P400 Additional Memory

To add memory to a P400, either 1232-D85 or 12128-E4 memories should be used. Memories modified per Section I may also be used with the restrictions as specified in Section I. When mixing 32K and 128K memories in the same system (only possible in main backplane), extreme care must be taken as to where memory boards are plugged in (i.e. from an addressing standpoint, 128K boards assume all boards are 128K and 32K boards assume all boards are 32K). (See Table 6 for Configurations).

1232-D85 - These memories run with all P400's, with no restrictions, and can be interleaved or non-interleaved.

12128-E4 - These memories are 128K with error correcting code. They will run in P400's that have Rev. D (or later) memory timing Prom (Prom Set ML) and ECO 2094 (changes refresh rate for 16K chips). These memories will run in either main memory, or extenders with no sizing restrictions (See Memory Extender for Configuration).

3. Interleaved Rules (1232-D85 and 12128-E4 only)

P400 systems may run with a mix of interleaved and non-interleaved memories in the system (see memory extenders for special rules). However, the number of memories switch-configured for interleave in a system must be even and run in odd even contiguous pairs (i.e. slots 17 and 16 - but not 16 and 15). (See Table 1 for interleaved switch configuration).

4. Memory Extenders

Memory extenders may use 1232-B85X and/or 1232-B85Y memories, 1232-D85 memories with interleaving on, 1232-D85 memories with interleaving off, 12128-E4 memories with interleaving on, or 12128-E4 memories with interleaving off. However, the five types (1232-B85X and 1232-B85Y being considered one type) may not be mixed within a memory extender. When using memory extenders, 1232-B85X memories must not be used in the main backplane.

The memory extenders may be jumper-dip configured to respond to either a 256K Block, or a 1024K Block of addresses (see Table 5 for dips and jumper list). Extenders configured for 256K may use one or two 128K memories, but they must be in the top two slots of the extender. Extenders configured for 1024K Blocks may not use 1232-B85X memories.

The memory extender switches must be set to define the starting 256K/1024K Block address of the extender and the type of memory in the extender (see Table 3 and 4). Switch #4 of the extender switches disables the address select switches and uses the backplane decoding. If using the backplane decoding, the extender decodes the slot select lines as if all memories and extenders in the main backplane are the same block size as it is (i.e. an extender configured as 1024K in the third slot will decode as the third 1024K, but an extender configured as 256K in the third slot will decode as the third 256K).

5. P100,P200 and P300 Memories

When installing memory boards in P100, P200 and P300 systems, the following rules must be remembered:

A. 1232-D85 memories will not run. The timing jumper dips must be changed and the switches must be reset (see Table 1).

B. 1232-B85Y memories will not run unless ECO #1756 is installed in the CPU. This ECO grounds the memory address and data latch signals at the CPU. This ECO should be installed in all CPU's NEEDED OR NOT!

C. 1232-B85 memories have no special restrictions.

D. 1232-B85X has same restrictions as 1232-B85Y above.

E. 1232-B85Y memories do not support battery backup.

F. 12128-E4 memories will not run.

Table 1

Memory Switch Positions

	B85Y	D85	Interleaved D85	E4	Interleaved E4
SW 1	Off	On	On		
SW 2	Off	On	On		
SW 3				On	On
SW 4					
SW 5	On	On	Off	On	Off
SW 6	On	On	Off	On	On
SW 7	Off	Off	Off	On	Off
SW 8	Off	On	On	On	On

*Switches not indicated are Don't Care.

TABLE 2

Pin Connection for Timing Dips

MEC 1720-	171	172	173	174
1232-	B85Y	B85Y	D85	D85
Dip Loc.	B44	B46	B46	B44
Jumpers	1-15	2-10	2-10	1-15
	4-12	3-11	15-16	3-15
	5-13			4-10
	6-14			5-12
	7-11			6-11
	8-6			7-9
	14-16			8-11
				14-16

TABLE 3

Memory Extender Address Switches
(On board in main backplane)

Memory 1024K	Block 256K	SW3	SW2	SW1	SW7	Starting 1024K	Address 256K
1	1	Off	Off	Off	Off	'00000000	'0000000
2	2	On	Off	Off	Off	'04000000	'1000000
3	3	Off	On	Off	Off	'10000000	'2000000
4	4	On	On	Off	Off	'14000000	'3000000
	5	Off	Off	On	Off		'4000000
	6	On	Off	On	Off		'5000000
	7	Off	On	On	Off		'6000000
	8	On	On	On	Off		'7000000

TABLE 4

Memory Extender Timing Switches
(On board in main backplane)

	SW5	SW6	SW8
1232-B85X/B85Y	On	On	On
1232-D85 Interleaved	Off	Off	On
1232-D85 Non-Interleaved	On	Off	On
12128-E4 Interleaved	Off	On	Off
12128-E4 Non-Interleaved	On	On	Off

TABLE 5

Pin Connections for Extender Block Configuration

MEC 1720-175	JDA 2769-912
256K	1024K
2-13	1-16
3-16	2-15
4-15	3-14
5-14	4-10
8-9	5-9
9-10	8-13

TABLE 6A

Main Backplane Memory Configuration

Slot		Memory Starting/Ending Addresses				
		8K	16K	32K	64K	128K
17	SA.	'000000	'000000	'000000	'0000000	'0000000
	EA.	'017777	'037777	'077777	'0177777	'0377777
16	SA	'020000	'040000	'100000	'0200000	'0400000
	EA	'037777	'077777	'177777	'0377777	'0777777
15	SA	'040000	'100000	'200000	'0400000	'1000000
	EA	'057777	'137777	'277777	'0577777	'1377777
14	SA	'060000	'140000	'300000	'0600000	'1400000
	EA	'077777	'177777	'377777	'0777777	'1777777
13	SA	'100000	'200000	'400000	'1000000	'2000000
	EA	'117777	'237777	'477777	'1177777	'2377777
12	SA	'120000	'240000	'500000	'1200000	'2400000
	EA	'137777	'277777	'577777	'1377777	'2777777
11	SA	'140000	'300000	'600000	'1400000	'3000000
	EA	'157777	'337777	'677777	'1577777	'3377777
10	SA	'160000	'340000	'700000	'1600000	'3400000
	EA	'177777	'377777	'777777	'1777777	'3777777

* ALL ADDRESS REPEAT, EXCEPT 8K.

TABLE 6B

17 Slot

Slot Number	Slot Address Bits	Memory Increment 8K Bd	16K	32K	128K
17	11111	8	16	32	128
16	11110	16	32	64	256
15	11101	24	48	96	384
14	11100	32	64	128	512
13	11011	40	80	150	640
12	11010	48	96	192	768
11	11001	56	112	224	896
10	11000	64	128	256	1,024
9	10111	72	16	32	128
8	10110	80	32	64	256
7	10101	88	48	96	384
6	10100	96	64	128	512
5	10011	104	80	160	640
4	10010	112	96	192	768
3	10001	120	112	224	896
2	10000	128	128	256	1,024
1	01111	136	16	32	128

* 128K Memory board will only operate on 400 and 500 CPU.

MEMORY MODEL NUMBERS

Model	Description	Comments
170	4K, 1US, no parity	Obsolete
171	8K, 1US, no parity	Obsolete
271	8K, 750NS, parity	Obsolete
371	8K, 650NS, parity	Obsolete
1027-001	32K, 750NS, parity	Obsolete
1027-006	8K, IUS, no parity	Obsolete
1208-A65	8K, IUS, no parity	
1208-A654L	8K, IUS, no parity	Different artwork
1208-B85	8K, 750NS, parity	
1208-B854L	8K, 750NS, parity	Different artwork
1216-A65	16K, IUS, no parity	
1216-B85	16K, 750NS, parity	
1232-A65	32K, IUS, no parity	
1232-B85	32K, 750NS, parity	
1232-B85X	32K, 750NS, parity	Usable on P400*
1232-B85Y	32K, 750NS, parity	Usable on P400*
1232-D85	32K, P400	
12128-E4	128K, P400/P500	

*See Paragraph 1 and 2 for description.

DATE: January 8, 1975 PE-T-169

TO: Engineering & Programming Staff

FROM: J. E. Sheahan

SUBJECT: SYSTEM CONFIGURATIONS WITH 32K MEMORY BOARDS

This memo discusses the system characteristics of the 32K board relative to power, physical slot location, and mixing with 8K boards.

Characteristics:

1. The 32K board has approximately the same power requirements as the 8K board.

2. The PRIME power supplies will support eight boards maximum. Therefore, no combination of the two board types may exceed this maximum.

3. The present 32K board operates at 750 ns read cycle and 600 ns access. It is therefore compatible with the P100, P300 and the P300 with P200 memory interface timing. ECO #1511, 1512 must be installed in a CPU to make it compatible with this memory.

4. It is anticipated that a faster version of this board will be available in 2Q75 and will operate at the standard P300 speeds of 600 ns cycle and 440 ns access.

5. Timing adjustments are made on the board with the cycle being initiated by PRECH. No adjustments are necessary or permitted.

6. The attached charts (A and B) show the response of the 8K and 32K modules to address stimulus for the various physical slots. Referring to these charts, one can see that multiple configurations are permitted.

   For a 10 slot backplane:

   1. 8K modules are addressed sequentially from slot 10 to slot 1 permitting addressing up to 80K. The 32K modules are addressed sequentially from slot 10 through slot 3 permitting addressing up to 256K. Slots 2 and 1 repeat the selection of up to 32K and up to 64K. Therefore, for a machine having 128K, it is possible to configure four 32K boards in the following ways:

      1. 10, 9, 8, 7
      2. 2, 9, 8, 7
      3. 10, 1, 8, 7
      4. 2, 1, 8, 7

For a 17 slot backplane:

1. 8K modules are addressed sequentially from slot 17 through slot 1 permitting addressing up to 136K. The 32K modules are addressed sequentially from slot 17 to slot 10 permitting up to 256K. Slots 9 to 2 repeat the sequence of up to 256K and slot 1 becomes the third slot addressing the first 32K of memory. Again for a 128K system there are numerous combinations of slot assignments:

   1. 17, 16, 15, 14
   2. 9, 8, 7, 6
   3. 17, 16, 7, 6
   4. 9, 8, 15, 14
   5. etc., etc.

Mixing Modules:

The 8K and 32K boards may be mixed in a system provided that there is no overlap in address space per charts A and B. If contiguous memory addressing is required, it is generally easier to use the 32K boards in the lower addressing space.

Example 1 - Upgrade 32K of 8K modules (4) to 96K.

Solution I - 1. 32K board slot 17
2. 32K board slot 16
3. 8K board slot 9
   8K board slot 8
   8K board slot 7
   8K board slot 6

Solution II - 1. 8K board slot 17
   8K board slot 16
   8K board slot 15
   8K board slot 14
2. 43K board slot 8
3. 32K board slot 7

Example 2 - Upgrade 48K of 8K modules (6) by adding two 32K modules and obtaining 112K.

Solution I - 1. 32K board slot 17
2. 32K board slot 16
3. 8K board slot 9
4. 8K board slot 8
5. 8K board slot 7
6. 8K board slot 6
7. 8K board slot 5
8. 8K board slot 4

Solution II - 1. 8K board slot 17
2. 8K board slot 16
3. 8K board slot 15
4. 8K board slot 14
5. 32K board slot 8
6. 32K board slot 7
7. 8K board slot 5
8. 8K board slot 4

DOS/VM:

The above examples illustrated means of obtaining contiguous memory with mixed boards. DOS/VM requires that the first 32K be contiguous, but the remaining memory may have "holes" in the addressing scheme. Therefore, there is some added flexibility in configuring this type of system.

J. E. Sheahan

Attachments
as

/ja

Chart A

10 Slot

Slot Number	Slot Address Bits	Memory Increment 8K Bd	Memory Increment 32K Bd
10	11111	8	32
9	11110	16	64
8	11101	24	96
7	11100	32	128
6	11011	40	160
5	11010	48	192
4	11001	56	224
3	11000	64	256
2	10111	72	32
1	10110	80	64

Chart B

17 Slot

Slot Number	Slot Address Bits	Memory Increment 8K Bd	32K Bd
17	11111	8	32
16	11110	16	64
15	11101	24	96
14	11100	32	128
13	11011	40	150
12	11010	48	192
11	11001	56	224
10	11000	64	256
9	10111	72	32
8	10110	80	64
7	10101	88	96
6	10100	96	128
5	10011	104	160
4	10010	112	192
3	10001	120	224
2	10000	128	256
1	01111	136	32

```
(0001) *     HSMT2,MEMORY TEST AND VERIFICATION,GFD,MAR 75
(0002) *     TEST HIGH SPEED MOS MEMORY
(0003) *     PRIME COMPUTER INC.,SRC0723.010  (85)
(0004) *     COPYRIGHT 1974,PRIME COMPUTER INC.,FRAMINGHAM MASS.
(0005) *
(0006) *
(0007) *
(0008) *     PURPOSE:
(0009) *      TEST HIGH SPEED MOS MEMORY UP TO 256K. CHECK FOR
(0010) *      MISSING MEMORY AND MEMORIES ANSWERING TO THE
(0011) *      WRONG ADDRESS.
(0012) *
(0013) *     USE:
(0014) *      LOAD TEST PROGRAM
(0015) *      MASTER CLEAR
(0016) *      THE PROGRAM AUTOMATICLY SIZES MEMORY. TO BYPASS
(0017) *         AUTO SIZING, ENTER THE HIGHEST SECTOR ADDRESS DESIRED
(0018) *         IN BITS 8-16 OF THE A REGISTER.
(0019) *      SET SENSE SWITCHES AS DESIRED
(0020) *      START PROGRAM
(0021) *      PROGRAM TYPES END OF PASS AFTER EACH PASS OF PROGRAM
(0022) *
(0023) *     **************NOTE*****************
(0024) *     DO NOT HALT PROGRAM AFTER STARTING
(0025) *     IF SYSTEM IS RUNNING IN PAGING.
(0026) *     REVERSE PAGE MAP MAY CAUSE A MISSING
(0027) *     MEMORY VECTOR IN THE CONTROL PANEL
(0028) *     ROUTINE.
(0029) *
(0030) *     ***********************************
(0031) *
(0032) *
(0033) *
(0034) *     SENSE SWITCH:
(0035) *      1 HALT AT END OF PASS
(0036) *      2 BYPASS RELOCATION  (MUST BE SET AT START OF PROGRAM )
(0037) *      3 NO ASR-HALT ON ERRORS
(0038) *      4 BYPASS MACHINE CHECK MODE
```



```
(0039) *      5 BYPASS PAGE TEST  (MUST BE SET AT START OF PROGRAM)
(0040) *      6 TEST IN PAGING ONLY  (MUST BE SET AT START OF PROGRAM)
(0041) *      8 BYPASS ZEROS & ONES TEST
(0042) *      9 BYPASS RANDOM ADDRESS TEST
(0043) *     10 BYPASS RANDOM DATA TEST
(0044) *     11 BYPASS WORST CASE ADDRESS TEST
(0045) *     12 BYPASS WORST CASE PARITY TEST
(0046) *     13 BYPASS ADDRESS CROSSOVER TEST
(0047) *     14-16 NOT USED
(0048) *
(0049) *
(0050) *     ERRORS:
(0051) *      DATA ERRORS PRINT: IS,SB,FAILING ADDRESS,SECTOR MAP IF
(0052) *      PAGED,ADDRESS ERROR ROUTINE ENTERED FROM,AND TEST NUMBER.
(0053) *      PARITY ERRORS PRINT: FAILING ADDRESS,SECTOR MAP IF
(0054) *      PAGED,ADDRESS ERROR ROUTINE ENTERED FROM,AND TEST NUMBER.
(0055) *      ALL PARITY ERRORS CAUSED BY THE RUNNING OF THE PROGRAM
(0056) *       AND NOT THE TESTING OF THE MEMORY BLOCK CAUSE VECTOR
(0057) *       HALTS IF IN MACHINE CHECK MODE
(0058) *      ALL OTHER ERRORS HALT--SEE LISTING FOR REASON
(0059) *
(0060) *     TEST NUMBERS
(0061) *
(0062) *      T1  ZEROS & ONES TEST
(0063) *      T2  RANDOM ADDRESS TEST
(0064) *      T3  RANDOM DATA TEST
(0065) *      T4  WORST CASE ADDRESS TEST
(0066) *      T5  WORST CASE PARITY TEST
(0067) *      T6  ADDRESS CROSSOVER TEST
(0068) *
(0069) *
(0070) *
(0071) *     METHOD:
(0072) *      ON ENTRY THE PROGRAM SAVES THE A REG. FOR MEMORY AUTO
(0073) *      SIZE STATUS. NEXT, PAGING IS TESTED FOR
(0074) *      AVAILABILITY AND THE PAGE FLAG (PFLG) IS SET TO NON
(0075) *      ZERO IF PAGING IS AVAILABLE. IF THE SIZE STATUS IS ZERO
(0076) *      THE MEMORY IS SIZED AND THE SIZE MAP STORED IN THE
```



```
(0077) *      SIZE BUFFER (SIZE). THE SIZE ROUTINE CHECKS UP TO
(0078) *      THE HIGHEST POSSIBLE ADDRESS (64K NO PAGING & 256K PAGING)
(0079) *      FOR MEMORY AVAILABILITY SO THE MEMORY MAY BE CONFIGURED
(0080) *      WITH MISSING MEMORY BOARDS (HOLES) AND THE SIZE
(0081) *      ROUTINE WILL CONFIGURE AND TYPE THE SIZE MAP. THE MAP
(0082) *      SHOWS THE SIZE OF BASE MEMORY (STARTING AT SECTOR 0), THE
(0083) *      SIZE OF THE MEMORY HOLE (ONLY IF MEMORY EXISTS
(0084) *      AFTER THE HOLE), THE SIZE OF THE NEXT MEMORY BLOCK
(0085) *      ETC.,ETC.(ALWAYS ENDING WITH THE LAST MEMORY BLOCK).
(0086) *      IF THE SIZE STATUS WAS NON ZERO THEN IT IS BUMPED ONCE
(0087) *      AND SAVE AS THE MEMORY SIZE (THIS MUST BE CONTINUOUS
(0088) *      MEMORY, NO HOLES).
(0089) *
(0090) *      THE PROGRAM EXCANGES THE BASE SECTOR WITH SECTOR TWO
(0091) *      THEN TESTS THE BASE SECTOR. MACHINE CHECK MODE
(0092) *      IS TURNED OFF DURING BASE SECTOR TEST BECAUSE THE
(0093) *      VECTOR LOCATIONS ARE TESTED, HOWEVER THE MACHINE
(0094) *      CHECK FLOP IS TESTED. THE BASE SECTOR IS
(0095) *      RESTORED AFTER IT IS TESTED.
(0096) *
(0097) *
(0098) *      THE PROGRAM NOW TESTS EACH BLOCK OF MEMORY ONE
(0099) *      BLOCK AT A TIME (THE FIRST BLOCK STARTS AT SECTOR ONE, NOT ZERO).
(0100) *      THE PROGRAM TESTS FROM THE FIRST SECTOR ABOVE THE PROGRAM
(0101) *      TO THE LAST SECTOR IN THE BLOCK (OR THE TOP OF SECTOR '177
(0102) *      WHICHEVER IS THE LOWEST). THE PROGRAM IS THEN RELOCATED TO
(0103) *      THE NEXT SECTOR UP AND TESTING IS AGAIN STARTED FROM THE
(0104) *      FIRST SECTOR ABOVE THE PROGRAM.THE PROGRAM KEEPS RELOCATING
(0105) *      AFTER EACH PASS OF THE TESTS UNTIL IT RESIDES IN THE TOP
(0106) *      SECTOR OF THE BLOCK (OR SECTOR '177 ). THE TEST IS NOW RUN
(0107) *      FROM THE FIRST SECTOR OF THE BLOCK TO THE SECTOR BELOW THE
(0108) *      PROGRAM. THE PROGRAM IS THEN RELOCATED TO THE NEXT SECTOR
(0109) *      DOWN AND TESTING IS AGAIN STARTED ENDING AT THE SECTOR BELOW
(0110) *      THE PROGRAM. THE PROGRAM KEEPS RELOCATING DOWN UNTIL IT IS BACK
(0111) *      IN THE FIRST SECTOR OF THE BLOCK.
(0112) *
(0113) *
(0114) *
```

HSMT2, SAMPLE ERROR PRINTOUT

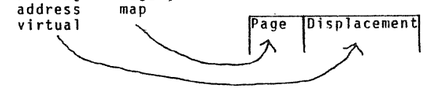
Parity Errors

1.

xxxxxx	xxxxxx	tx
Failing address	Error routine address	Test#

2.

xxxxxx	xxxxxx	xxxxxx	tx
Failing address virtual	Page map		

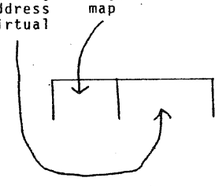


3. Data Errors:

xxxxxx	xxxxxx	xxxxxx	xxxxxx	tx	
Is	Should be	Failing address real	Error routine	Test#	

4.

xxxxxx	xxxxxx	xxxxxx	xxxxxx	xxxxxx	tx
		Failing address virtual	Page map		



```
(0001) *  HSMT3, T&MSRC, GFD, 02-04-77
(0002) *  HIGH SPEED MEMORY TEST 3
(0003) *  PRIME COMPUTER INC., SRC0791-000
(0004) *  COPYRIGHT 1977, PRIME COMPUTER COMPANY INC.
(0005) *
(0006) *
(0007) *       PURPOSE:
(0008) *               TO TEST ALL MEMORY CONFIGURATIONS FOR ALL
(0009) *               PRIME CPU'S.
(0010) *
(0011) *
(0012) *
(0013) *       USE:
(0014) *               1) LOAD TEST PROGRAM
(0015) *
(0016) *               2) MASTER CLEAR
(0017) *
(0018) *               3) ENTER SIZE IN OCTAL K (32K = 40) IN A REGISTER IF
(0019) *                  SIZE ROUTINE IS NOT WANTED
(0020) *
(0021) *               4) SET DESIRED SENSE SWITCHES
(0022) *
(0023) *               5) PRESS START
(0024) *
(0025) *               6) THE PROGRAM HEADING, CPU TYPE, AND MEMORY
(0026) *                  MAP WILL BE TYPED (MAP SHOWS PHYSICAL MEMORY
(0027) *                  BLOCKS AND MISSING MEMORY BLOCKS, ONLY MEMORY
(0028) *                  BLOCK IF NO HOLES IN MEMORY ADDRESSING).
(0029) *
(0030) *               7) THE PROGRAM WILL TYPE END-OF-PASS AFTER
(0031) *                  EACH COMPLETE PASS OF THE TEST.
(0032) *
(0033) *
(0034) *
(0035) *       SENSE SWITCHES:
(0036) *
(0037) *               1 -TERMINET CONSOLE (300 BAUD)
(0038) *
```



```
(0039) *               2 -NO PAGING (RUN AS P200)
(0040) *                  NOTE: THIS WILL ENABLE CACHE ON P4/500
(0041) *               3 - NO PARITY (NOT IN MACHINE CHECK MODE)
(0042) *               4 -ENTER DEBUG MODE AT END OF PRESENT TEST
(0043) *                  OR ERROR TYPEOUT, RESET AFTER DEBUG REQUEST
(0044) *                     SEE DEBUG MODE
(0045) *               5 -HALT ON ERROR
(0046) *               6 -DISPLAY ERROR COUNT ON ERROR
(0047) *               7 -EXECUTE FROM CACHE (P4/500 ONLY)
(0048) *               8 -CONFIGURE CHIP TESTS FOR 16K CHIP
(0049) *
(0050) *
(0051) *
(0052) *       METHOD:
(0053) *
(0054) *               THE PROGRAM DETERMINES AND TYPES THE CPU TYPE.
(0055) *               MEMORY IS SIZED AND PARITY FIXED THROUGHOUT MEMORY.
(0056) *               THE MEMORY SIZE MAP IS THEN PRINTED.
(0057) *
(0058) *               THE PROGRAM THEN EXECUTES THE SIX (6) MEMORY
(0059) *               TESTS STARTING WITH THE FIRST ADDRESS ABOVE THE
(0060) *               PROGRAM AND ENDING AT THE HIGHEST ADDRESS IN
(0061) *               MEMORY. THE PROGRAM IS THEN MOVED UP '10000 LOCATIONS
(0062) *               AND TEST 3 IS RUN. THIS IS REPEATED UNTIL THE
(0063) *               PROGRAM RESIDES IN THE LAST 4K OF MEMORY.
(0064) *
(0065) *               THE PROGRAM THEN EXECUTES THE SIX (6) MEMORY TESTS
(0066) *               STARTING WITH THE FIRST ADDRESS BELOW THE
(0067) *               PROGRAM AND ENDING AT ADDRESS '100 (ON P300'S WITH
(0068) *               MORE THAN 64K THE BOTTOM ADDRESS AT THIS POINT IS
(0069) *               '400). THE PROGRAM IS THEN RELOCATED DOWN AND TEST 3
(0070) *               IS AGAIN RUN. THIS IS REPEATED UNTIL THE PROGRAM IS
(0071) *               AGAIN LOCATED IN THE FIRST 4K OF MEMORY (FOR P300'S,
(0072) *               ONCE THE PROGRAM IS WITHIN THE FIRST 64K THE BOTTOM
(0073) *               ADDRESS IS CHANGED TO '100).
(0074) *
(0075) *               P400 & P500 ARE RUN IN SEGMENTATION MODE WITH CACHE
(0076) *               TURNED OFF. THE SDW & MAP ARE IN THE '400 LOCATIONS
```



```
(0077) *               BELOW THE PROGRAM STARTING ADDRESS (MAP STARTS AT '400)
(0078) *               WHILE THE PROGRAM IS MOVING UP AND AT '740C OF THE 4K
(0079) *               THAT THE PROGRAM IS IN WHILE MOVING DOWN. THE PROGRAM
(0080) *               ALWAYS IS VIRTUAL FIRST 4K OF MEMORY AND THE AREA
(0081) *               OF MEMORY BEING TESTED IS ALWAYS THE SECOND VIRTUAL
(0082) *               16K ('40000).
(0083) *
(0084) *               P300 RUNS IN PAGING MODE.THE MAP IS ALWAYS AT PHYSICAL
(0085) *               ADDRESSS '400 WHILE THE PROGRAM IS MOVING UP AND UNTIL
(0086) *               THE PROGRAM IS WITHIN THE FIRST 64K MOVING DOWN. ONCE
(0087) *               THE PROGRAM IS WITHIN THE FIRST 64K, THE MAP IS MOVED
(0088) *               TO THE LAST '400 LOCATIONS IN THE FIRST 64K (PAGE MAP
(0089) *               ON A P300 MUST BE IN FIRST 64K). AS WITH THE
(0090) *               P400, THE PROGRAM IS ALWAYS VIRTUAL FIRST 4K AND THE ARE
(0091) *               OF MEMORY BEING TESTED IS ALWAYS VIRTUAL SECOND 16K ('40(
(0092) *
(0093) *               PROGRAM LOCATION PMAP WILL ALWAYS POINT TO VIRTUAL LOCAT
(0094) *               OF THE PAGE MAP.
(0095) *
(0096) *               THE P100/200 WILL ALWAYS BE PHYSICAL MEMORY WITH THE
(0097) *               PROGRAM MOVING AND TEST AREA MOVING.
(0098) *
(0099) *
(0100) *       TESTS:
(0101) *
(0102) *       1       ADDRESS UNIQUENESS TEST FOR DATA
(0103) *
(0104) *               TESTS THE ADDRESS UNIQUENESS OF MEMORY ADDRESS'S BY
(0105) *               WRITING COMPLEMENTING PATTERNS IN INCREASING BLOCKS
(0106) *               UNTIL HALF THE MEMORY IS ONE PATTERN AND THE OTHER
(0107) *               HALF IS THE COMPLEMENT.
(0108) *
(0109) *       2       ADDRESS UNIQUENESS TEST FOR PARITY
(0110) *
(0111) *               SAME AS TEST 1 BUT SHIFTS THE DATA PATTERN RATHER
(0112) *               THAN COMPLEMENTING TO CHECK PARITY BITS.
(0113) *
(0114) *       3       MEMORY HIT TEST
```



```
(0115) *
(0116) *               TESTS EACH MEMORY LOCATION BY PERFORMING 512 HIGH
(0117) *               HIT RATE READ/WRITE OPERATIONS. THE FIRST 128 HITS
(0118) *               ARE PERFORMED WITH ONE DATA PATTERN, THE SECOND
(0119) *               128 WITH THE COMPLEMENT, AND THE LAST 256
(0120) *               ALTERNATING BETWEEN BOTH PATTERNS.
(0121) *
(0122) *       4       SENSE AMP TEST
(0123) *
(0124) *               TESTS WITHIN A CHIP FOR NOISE ACROSS THE SENSE
(0125) *               AMPLIFIER. PERFORMS HIGH HIT RATE WRITES/READS
(0126) *               ALTERNATING BACK AND FORTH ACROSS THE SENSE AMPLIFIER.
(0127) *               ALL BITS WITHIN A ROW IN THE ROW/COLUMN STRUCTURE ARE
(0128) *               TESTED AND THEN ALL LOCATIONS ARE CHECK FOR CHANGES
(0129) *               IN DATA WRITTEN. THIS IS REPEATED FOR ALL COLUMNS.
(0130) *
(0131) *       5       SENSE AMP COMPLEMENT TEST
(0132) *
(0133) *               SAME AS 4 BUT WITH COMPLEMENTIG DATA WHEN PERFORMING
(0134) *               HIGH HIT RATE READ/WRITE ACROSS SENSE AMP.
(0135) *
(0136) *       6       CHIP HIT TEST
(0137) *
(0138) *               TESTS FOR NOISE WITHIN A CHIP. PERFORMS A HIGH HIT RATE
(0139) *               READ/WRITE ON ALL ROW LOCATIONS AND CHECKS FOR NOISE
(0140) *               IN ALL BITS IN THE CHIP. THIS IS REPEATED FOR ALL
(0141) *               COLUMNS.
(0142) *
(0143) *
(0144) *
(0145) *       DEBUG MODE
(0146) *
(0147) *               SENSE SWITCH 4 REQUESTS DEBUG MODE. DEBUG MODE MAY BE REQUES
(0148) *               THE START OF THE PROGRAM, DURING A TEST, OR DURING AN ERROR
(0149) *               IF DEBUG IS REQUESTED AT THE START OF THE PROGRAM, DEBUG IS
(0150) *               ENTERED AFTER THE MEMORY IS SIZED. IF REQUEST DURING TEST OR
(0151) *               ERROR PRINTOUT, DEBUG IS ENTERED AT COMPLETION OF EITHER
(0152) *               PRESENT TEST OR PRINTOUT. WHEN DEBUG IS ENTERED, THE PROGRAM
```

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(0153) *
(0154) *          WILL REQUEST A DEBUG ENTRY, SENSE SWITCH 4 MUST BE RESET AT
(0155) *          THIS TIME. ONE LINE OF COMMANDS MAY BE ENTERED,
(0156) *          EXECUTION STARTS WITH C/R. LEADING ZERO'S NEED NOT BE
(0157) *          ENTERED UNLESS NUMBER ENTERED IS TO BE ZERO. DEBUG MAY BE
(0158) *          RE-ENTERED AT THE END OF ANY COMMAND. THE COMMANDS
(0159) *          ARE AS FOLLOWS WITH X'S REPRESENTING THE OCTAL NUMBER
(0160) *          ASSOCIATED WITH THE COMMAND:
(0161) *
(0162) *
(0163) *          NOTE: TO RETURN TO THE STANDARD TEST AFTER DEBUG,
(0164) *                THE PROGRAM SHOULD BE RELOADED.
(0165) *
(0166) *
(0167) *  COMMAND
(0168) *
(0169) *  SD XXXXXX       CHANGE THE STANDARD DATA PATTERNS TO THE INPUT
(0170) *                  PATTERN (STANDARD = 0 FOR 1,3-67777 FOR 2)
(0171) *
(0172) *
(0173) *  SL XXXXXXXX     SET LAST TEST ADDRESS TO ADDRESS ENTERED
(0174) *                  **SEE NOTE
(0175) *
(0176) *
(0177) *  SF XXXXXXXX     SET FIRST TEST ADDRESS TO ADDRESS ENTERED
(0178) *                  **SEE NOTE
(0179) *
(0180) *
(0181) *  MM   N/A        MOVE THE PAGE MAP. THE MAP IS MOVED FROM
(0182) *                  PRESENT LOCATION TO OTHER POSSIBLE LOCATION.
(0183) *                  EXAMPLE: MAP IS AT VERTUAL '400, MOVE TO VERTUAL
(0184) *                           '7400 OR VISE VERSER (SEE METHOD FOR
(0185) *                           PHYSICAL LOCATIONS)
(0186) *
(0187) *
(0188) *  MP XXXXXXXX     MOVE PROGRAM TO ADDRESS SPECIFIED (PROGRAM
(0189) *                  MUST BE ON 4K BOUNDRY SO RIGHT 4 NUMBERS ARE
(0190) *                  MASKED TO ZERO. EXAMPLE 167777 = 160000
```



```
(0191) *
(0192) *          RC XXXXXX     RUN THE STRING ENTERED THIS NUMBER
(0193) *                        OF TIMES BEFORE GOING ON TO NEXT COMMAND.
(0194) *                        IF THIS COMMAND IS NOT USED IT IS ASSUMED TO BE
(0195) *                        ONE. THIS COMMAND MAY BE USED TWICE PER LINE BUT
(0196) *                        WILL NEVER EXIT THE SECOND USE. THIS
(0197) *                        COMMAND DOES NOT HAVE TO BE THE LAST COMMAND.
(0198) *
(0199) *          NOTE: IF FIRST ADDRESS IS LOWER THAN LAST ADDRESS, THE
(0200) *                TEST IS PERFORMED WITH INCREMENTING ADDRESS. IF LAST IS
(0201) *                LOWER THEN FIRST ADDRESS, THE TEST IS PERFORMED WITH
(0202) *                DECREMENTIG ADDRESS. CARE SHOUL BE TAKEN NOT
(0203) *                TO TEST OVER PAGE MAP.
(0204) *
(0205) *
(0206) *          DEBUG EXAMPLE:
(0207) *          DEBUG ENTRY
(0208) *          MP 70000 SF 67777 SL 1000 RT 3 6 MP 0 SF 10000 SL 77777 RT 3 RC 5 C/R
(0209) *
(0210) *
(0211) *          ERRORS:
(0212) *
(0213) *                AN ERROR MESSAGE HEADING WILL BE TYPED ON THE FIRST
(0214) *                ERROR PRINTOUT ONLY. THE ERROR MESSAGE WILL PRINT
(0215) *                THE TEST NUMBER, AN ASTERISK IF A PARITY ERROR WAS
(0216) *                DETECTED, THE SHOULD BE DATA IF KNOWN (NOT KNOWN
(0217) *                IF MEMORY PARITY VECTOR FROM IMA ROUTINE), THE IS
(0218) *                DATA, AND THE ADDRESS THE ERROR OCCURED AT ( FOR
(0219) *                INTEPLEAVED MEMORIES CARE MUST BE TAKEN !!!!!!!!
(0220) *
(0221) *                PARITY ERRORS WITHIN THE PROGRAM OR FATAL ERRORS
(0222) *                WILL CAUSE A HALT, CHECK LISTING FOR CAUSE.
(0223) *
(0224) *
(0225) *
(0226) *
000440  (0227) SDWS   EQU     '440
000023  (0228) DTARG  EQU     '23
```