Application Note

Akademie věd České republiky
Ústav teorie informace a automatizace AV ČR, v.v.i.

# SDSoC 2015.4 Standalone BSP with Full HD HDMI In-Out with SW and HW Demos for Zynq System-on-Module TE0715-03-30 and Sundance EMC2-DP-V2 Platform

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Revision history:

| Rev. | Date | Author | Description |
|---|---|---|---|
| 1 | 12.08.2016 | Jiří Kadlec | BSP for SDSoC 2015.4 on Sundance EMC2-DP-V2 with TE0715-03-30 Zynq SoM.<br>Description of installation and use of the BSP. |
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Acknowledgements:

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# 1. Summary

## *1.1 Introduction*

This application note describes installation and use of a stand-alone board support package (BSP) for the Xilinx SDSoC 2015.4 for the Sundance EMC2-DP-V2 platform [3] with commercial or industrial grade Zynq XC7Z030-1C or XC7Z030-1I device on System on Module TE0715-03-30-1C or TE0715-03-30-1I [1].

This stand-alone BSP package also includes three motion detection and three edge detection video processing demos.

This application note and the BSP can be downloaded for free from the UTIA public www server.

**Main objectives of this application note**

- To demonstrate how to install, compile, modify and use the BSP and SW projects in the Xilinx SDSoC 2015.4 [5] for the Sundance EMC2-DP-V2 platform [3].
- To demonstrate on the EMC2-DP-V2 platform the HW accelerated video processing algorithms and the speedup against the initial SW versions running on the ARM.

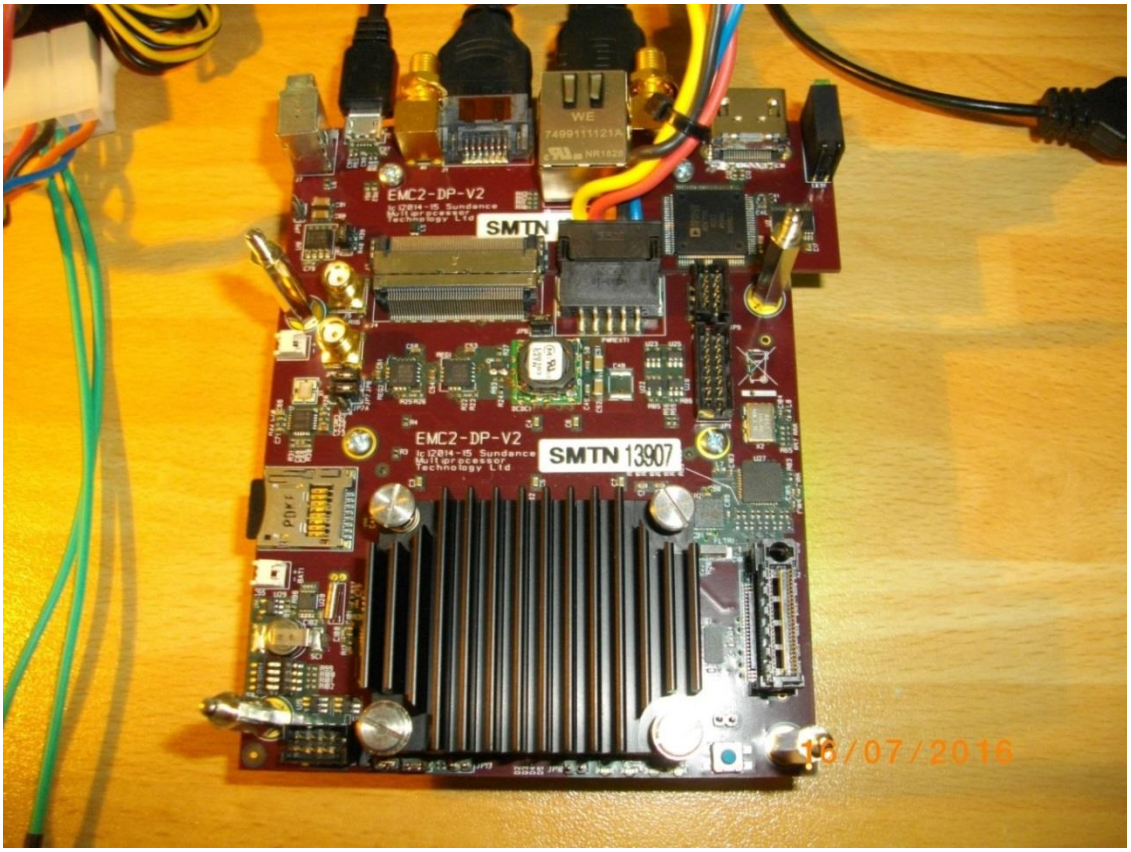



*Figure 1: Sundance EMC2-DP-V2 platform with Zynq XC7Z030-1I device and HDMII-HDMIO support.*

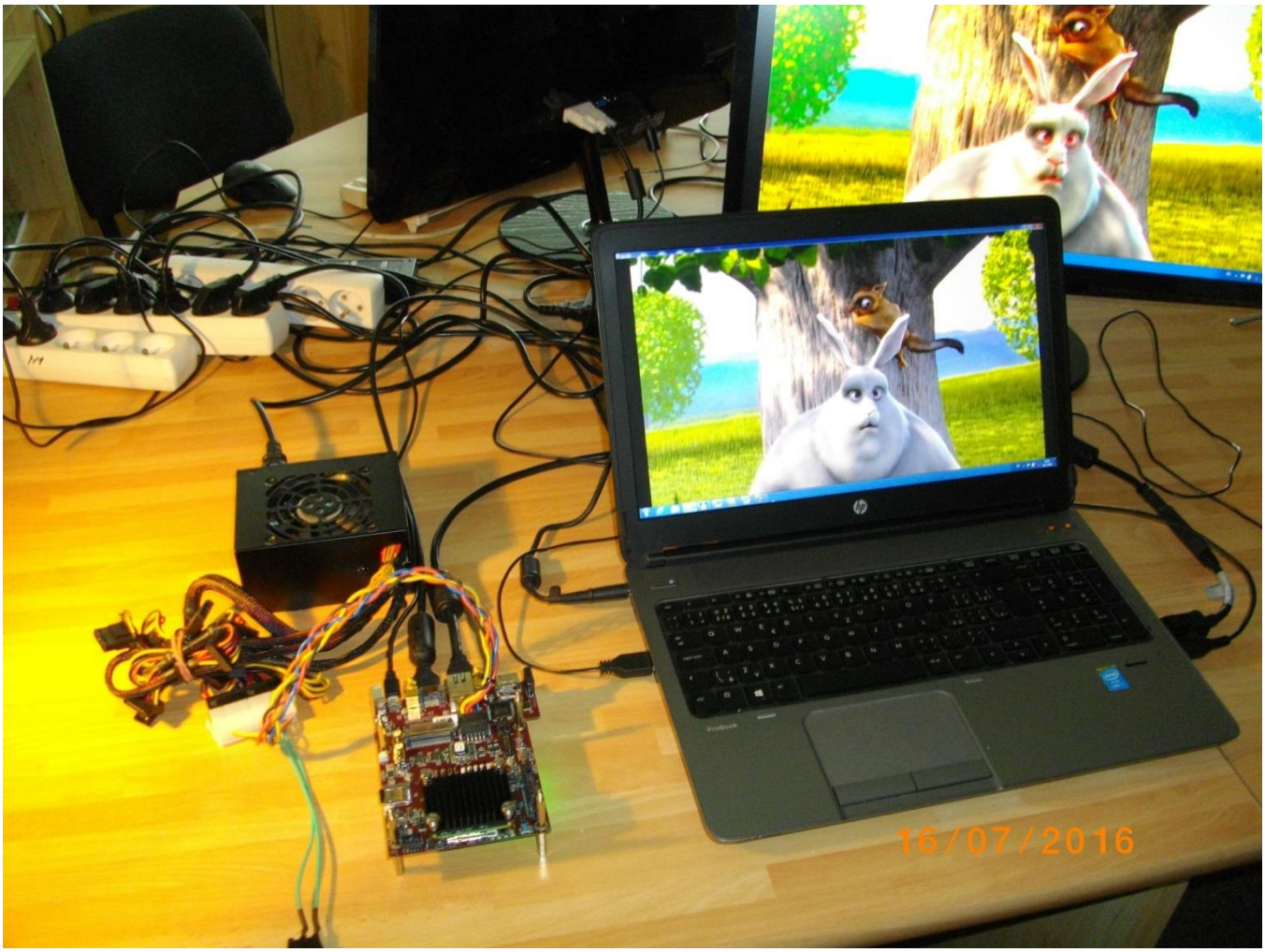



*Figure 2: HW accelerated motion detection in Full HD with 60 FPS video processing speed.*

Notice the fast moving edges in the face of the rabbit. Edges are marked by red pixels in the output display.

**Common setup for all included demos**

- ARM Cortex A9 processor of Xilinx Zynq device XC7Z030-1I executes standalone C application programs performing initialisation and synchronisation of the HW video processing chain.
- Enclosed SW projects can be modified by the user and recompiled in Xilinx SDSoC 2015.4 for SW execution on ARM or for the HW accelerated execution under control of ARM processor.
- Compiled demos (SW versions or accelerated HW versions) boot from the micro SD card directly after the power ON of the Sundance EMC2-DP-V2 board.
- Raw video data are provided by a Full HD HDMI source with resolution 1920x1080p60 (laptop).
- Data are processed in HW into the YCrCb 16 bit per pixel format and stored by video DMA (VDMA) controller to input video frame buffers (VFBs) reserved in the DDR3.
- HW DMA controller(s) send data from the input VFBs to the processing accelerators in the programmable logic (PL) part of Zynq.
- Another HW DMA controller(s) send processed data from HW to output VFBs in DDR3.
- Second part of the HW VDMA IP core is sending data to the Full HD display (1920x1080p60).

## 1.2 Introduction to the demos

### Edge detection

The edge detection algorithm is producing B/W Full HD video stream. Edges in each frame are marked as white and remaining part of the figure is set as black.

The edges are detected by a Sobel filter. Each pixel is filtered by a 3x3 2D FIR filter. A nonlinear decision on the output of the filter provides decision if the pixel is part of an edge or not. All computation is performed in fixed point. Input to the Sobel filter is the video signal with each pixel converted to the monochrome 8bit format.

Demos **sh01**, **sh02** and **sh03** provide accelerated HW computation of edge detection with 1, 2 or 3 parallel HW data paths. HW demos are using 1, 2 or 3 DMA HW channels as input from DDR3 to 1, 2 or 3 Sobel filters. Another 1, 2 or 3 DMA HW channels support output from Sobel filters to the DDR3. Zynq PL resources and the accelerations reached for these HW designs are summarised in sections 1.3, 1.4 and 1.5.

### Motion detection

The motion detection algorithm detects and performs visualisation of **moving edges**. The moving edges are identified by two Sobel filters performing FIR filtering (similar to the above described edge detection) on pixels with identical coordinates but from two subsequent video frames. A difference of these filtered results is computed a noise in that signal is filtered by a Median filter.

Resulting signal is used for the nonlinear binary decision if the analysed pixel is part of a moving edge or not. If the pixel is part of a moving edge, it is assigned red colour and merged with the original colour video signal. Resulting output Full HD video signal is unchanged, with the exception of red colour marked moving edges. See *Figure 2*. The fast moving edges in the face of the rabbit are marked by red pixels.

Demos **md01**, **md02** and **md03** provide accelerated HW computation with 1, 2 or 3 parallel HW data paths. HW demos are using 2, 4 or 6 DMA HW channels for reading from two sub sequent video frame buffers located both in the DDR3 to 1, 2 or 3 video processing chains of accelerators performing the motion detection. Another 1, 2 or 3 DMA HW channels perform parallel write of results to the DDR3. Zynq PL resources and accelerations reached for these HW designs are summarised in sections 1.6, 1.7 and 1.8.

### Measurements of acceleration

The acceleration results have been measured as a ratio of the frame per second (FPS) reached by the HW accelerators generated by the SDSoC 2015.4 and the FPS reached by the SW implementation on ARM in the SDSoC 2015.4.

## 1.3 Project sh01: Edge detection with single HW accelerator

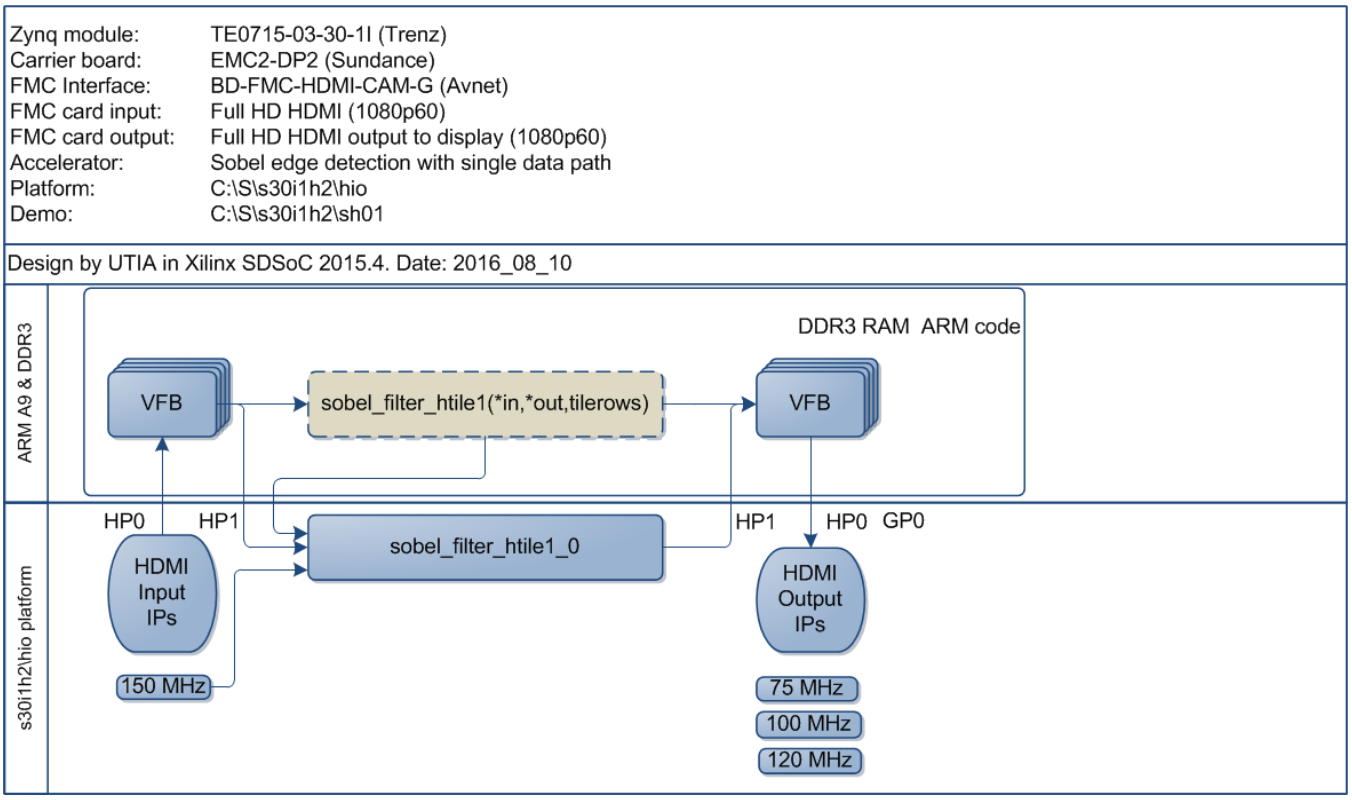



*Figure 3: Project sh01 - Edge detection with single HW accelerator.*

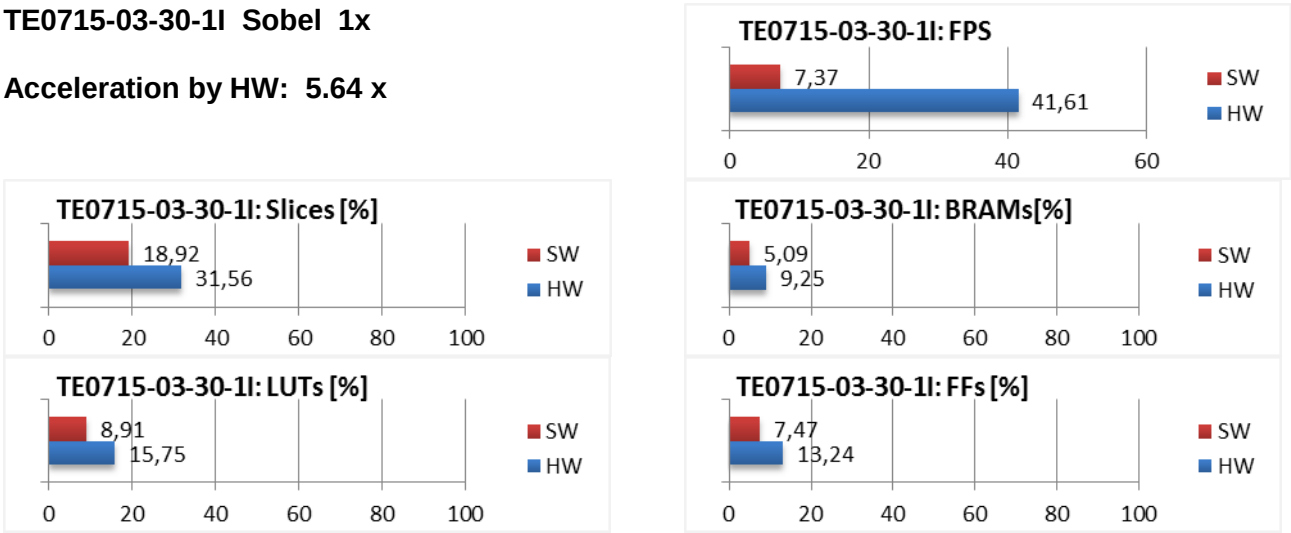



*Figure 4: Project sh01 - Acceleration and HW resources used.*

## 1.4 Project sh02: Edge detection with two HW accelerators

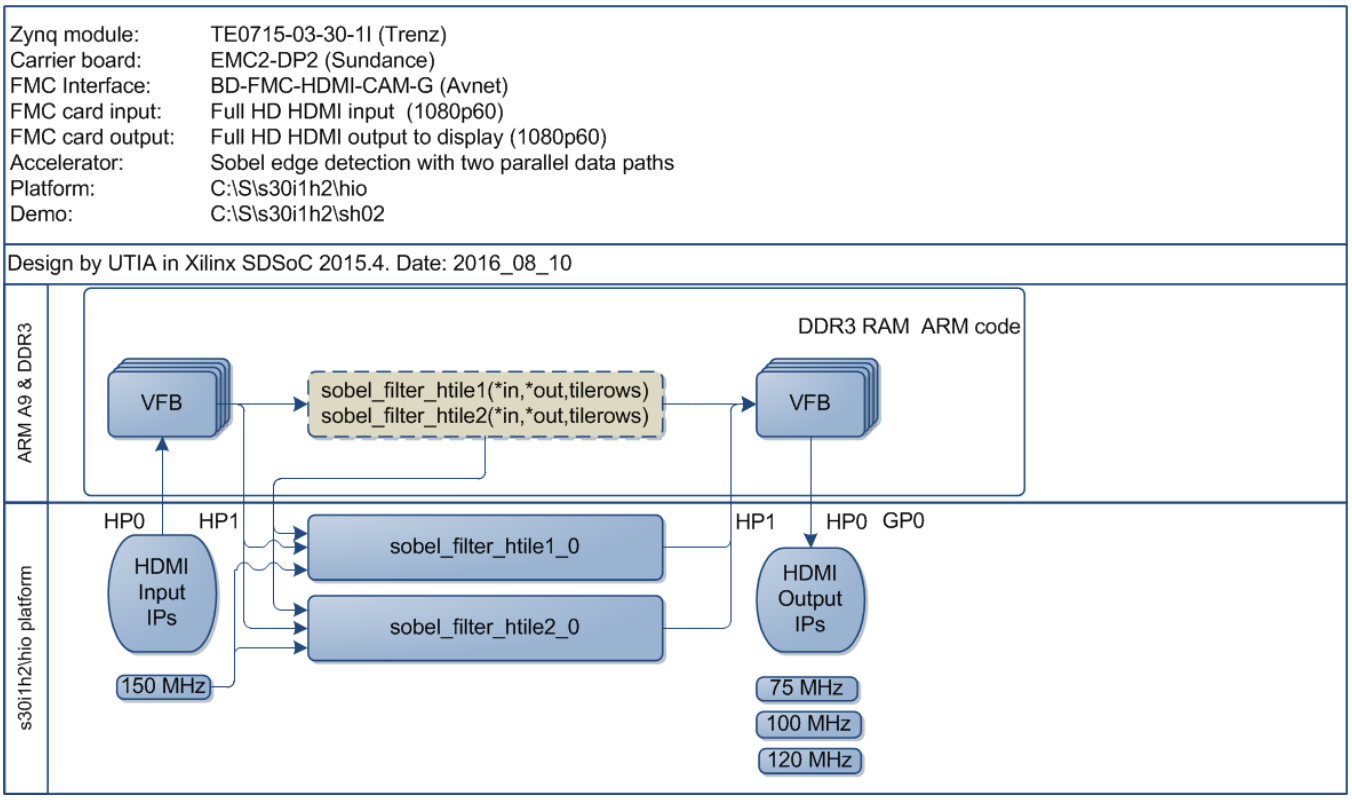



*Figure 5: Project sh02 - Edge detection with two HW accelerators.*

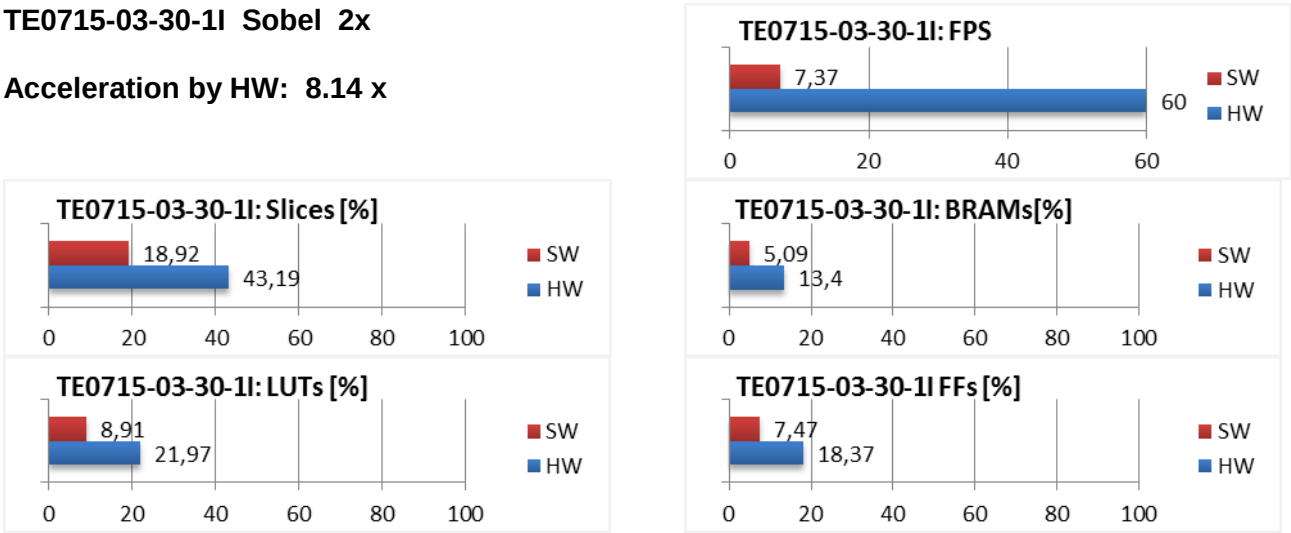



*Figure 6: Project sh02 – Acceleration and HW resources used.*

## 1.5 Project sh03: Edge detection with three HW accelerators

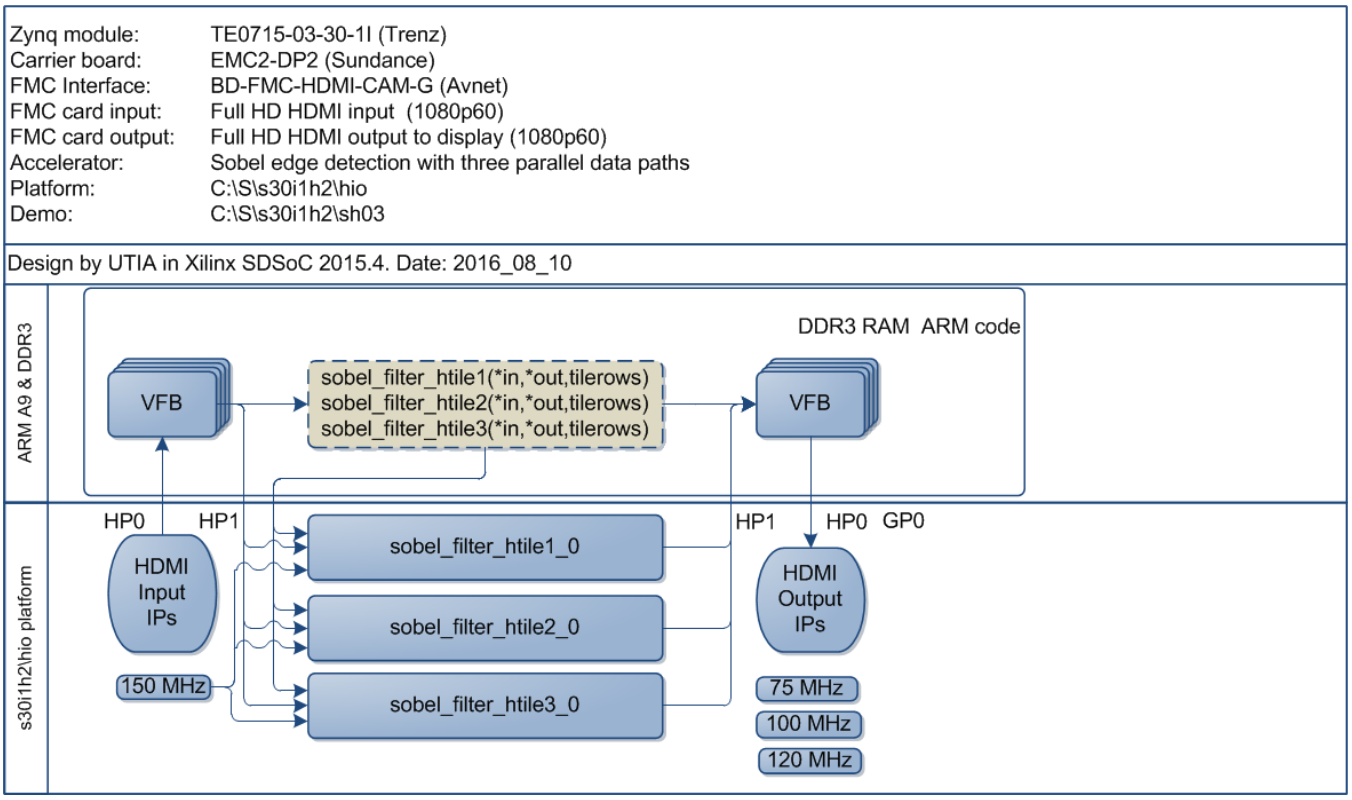
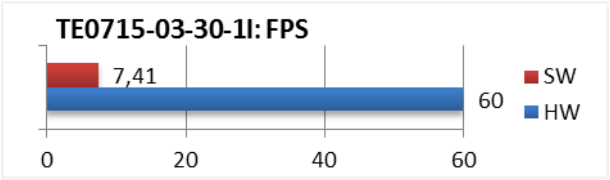
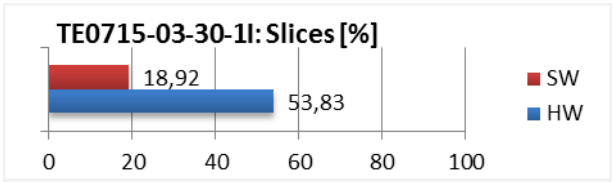


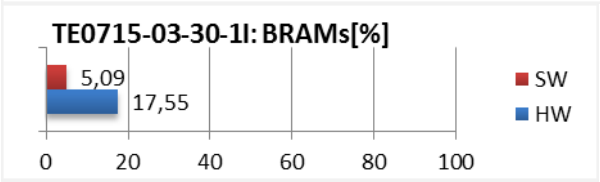

*Figure 7: Project sh03 - Edge detection with three HW accelerators.*

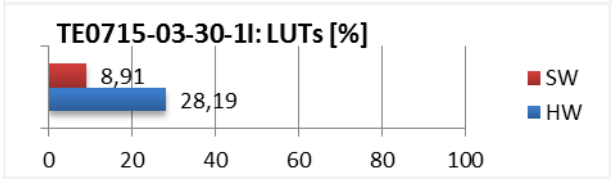
**TE0715-03-30-1I Sobel 3x**

**Acceleration by HW: 8.09 x**



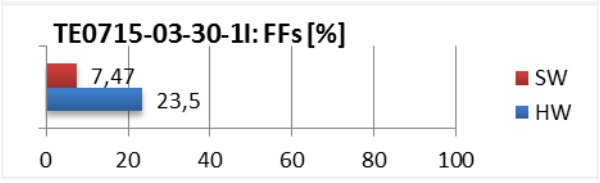




*Figure 8: Project sh03 - Acceleration and HW resources used.*

## 1.6 Project md01: Motion detection with single chain of HW accelerators

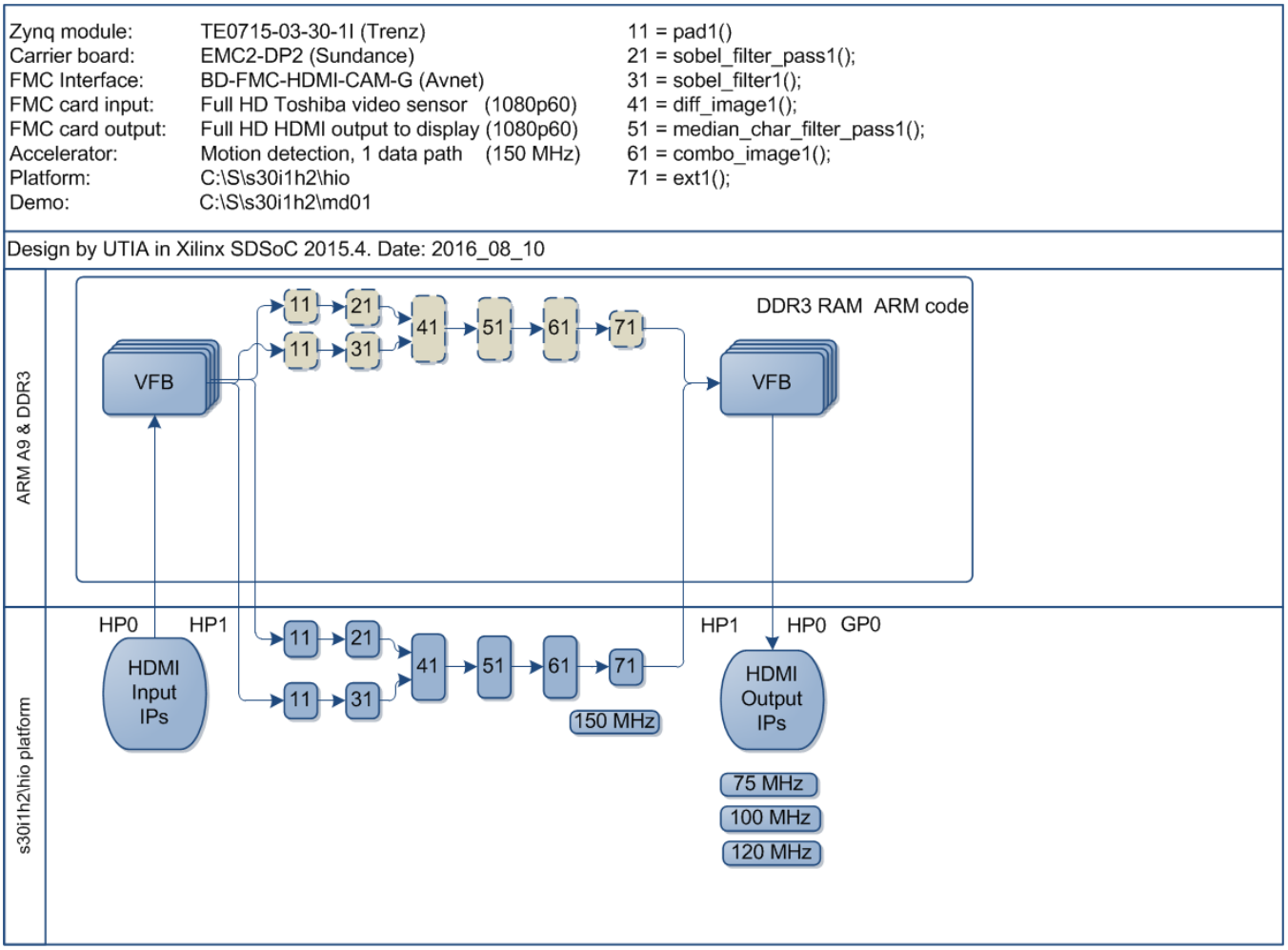
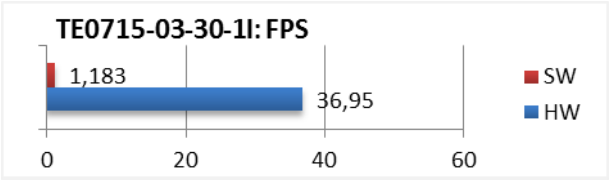
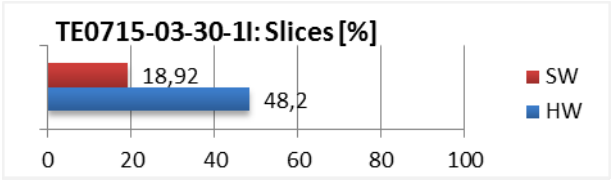


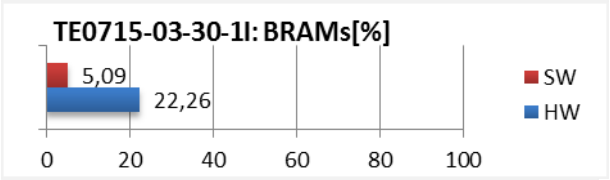

*Figure 9: Project md01 - Motion detection with single HW accelerator data path.*

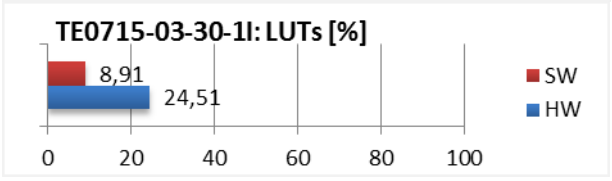
**TE0715-03-30-1I Motion Detection 1x**

**Acceleration by HW: 31.2 x**



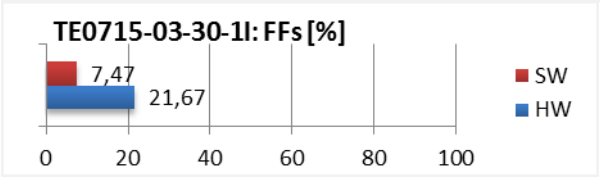




*Figure 10: Project md01 - Acceleration and HW resources used.*

## 1.7 Project md02: Motion detection with two chains of HW accelerators

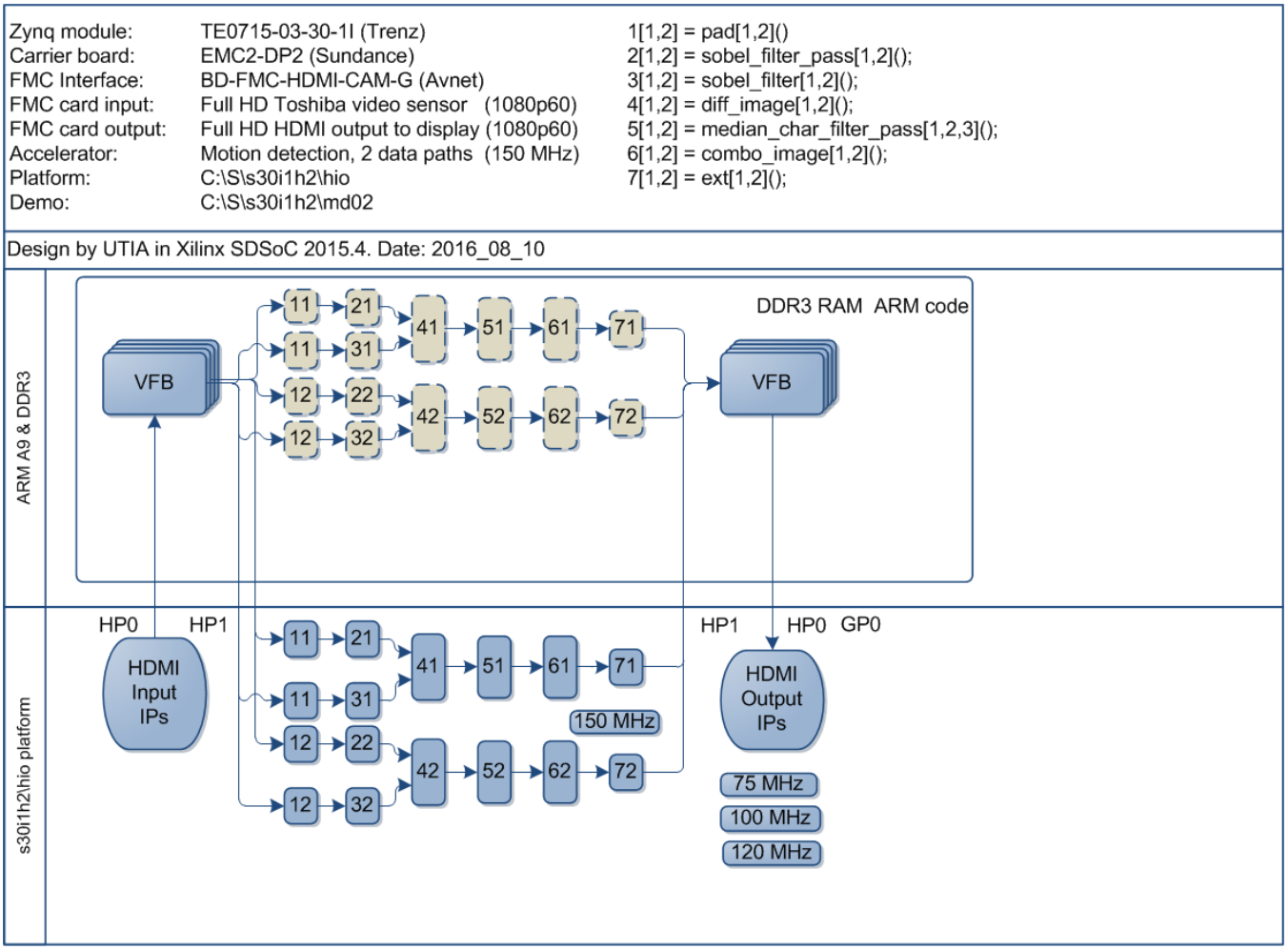
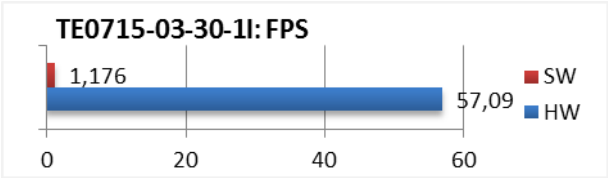
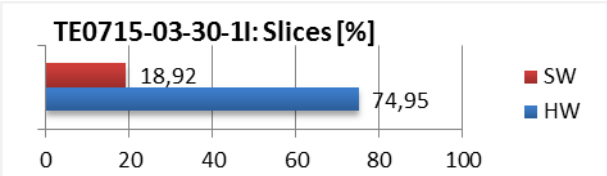


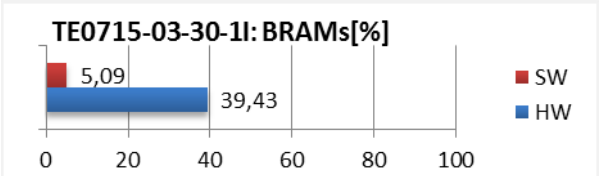

*Figure 11: Project md02 - Motion detection with two HW accelerator data paths.*

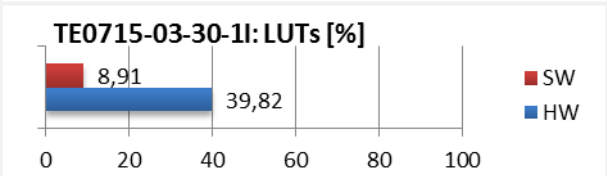
**TE0715-03-30-1I Motion Detection 2x**

**Acceleration by HW: 48.5 x**



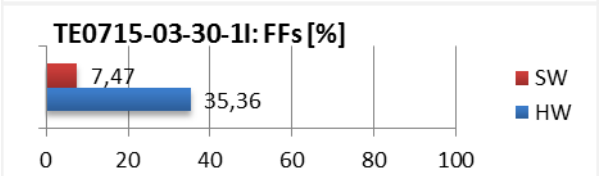




*Figure 12: Project md02 - Acceleration and HW resources used.*

## 1.8 Project md03: Motion detection with three chains of HW accelerators

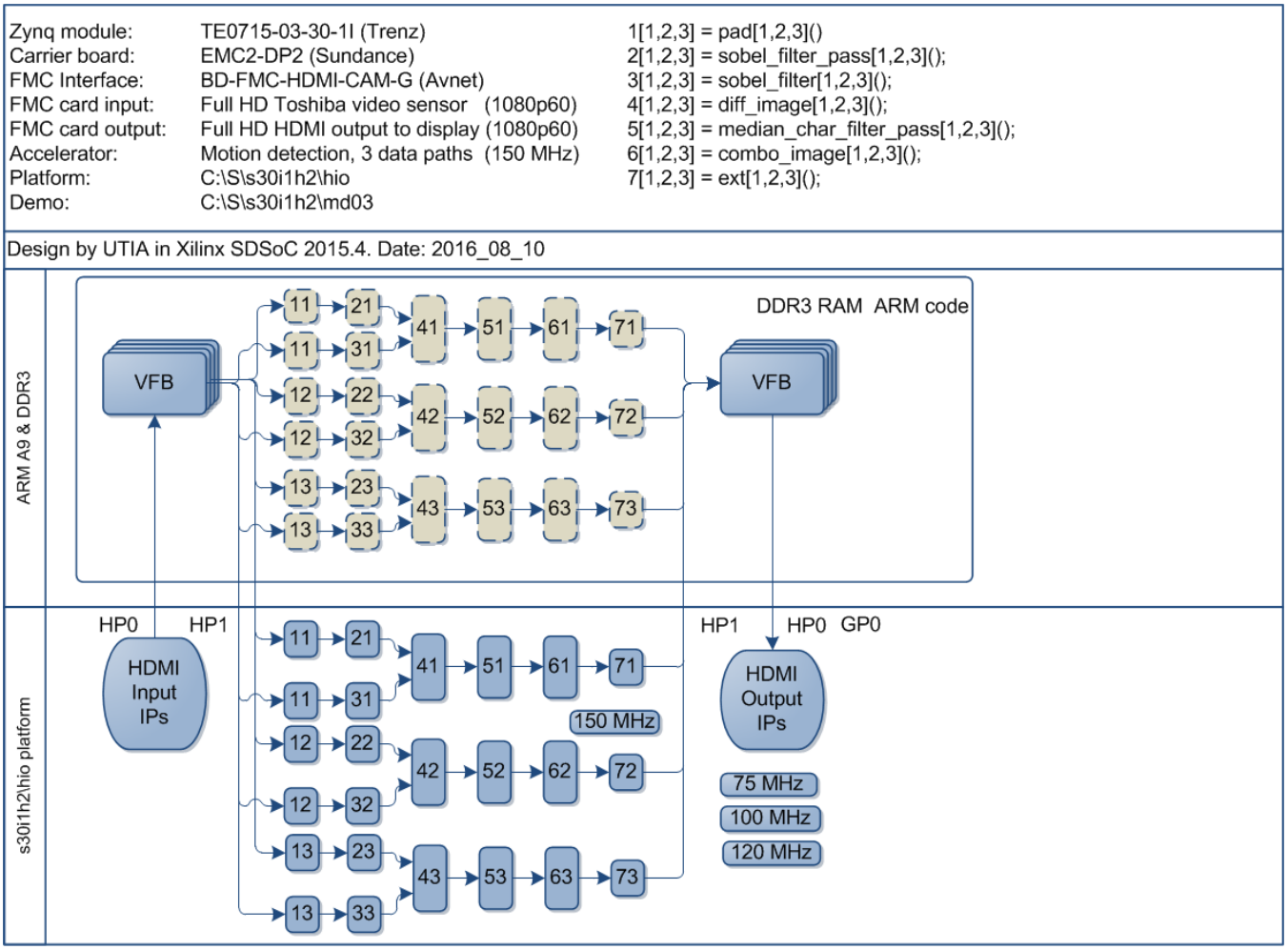



*Figure 13: Project md03 - Motion detection with tree HW accelerator data paths.*

**TE0715-03-30-1I Motion Detection 3x**

**Acceleration by HW: 51.06 x**

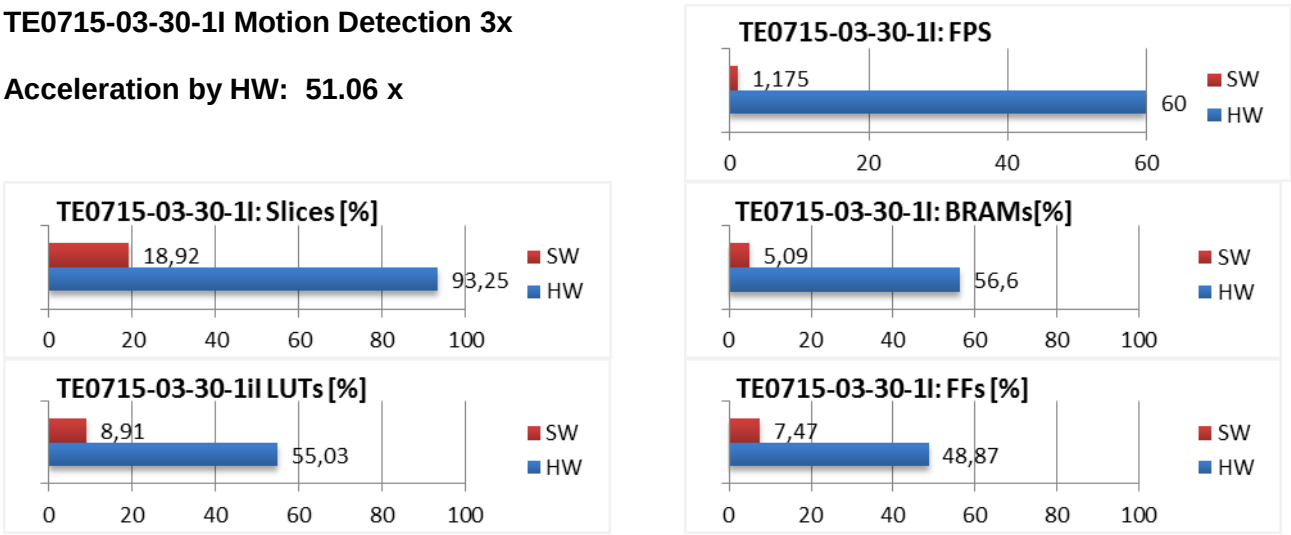



*Figure 14: Project md03 - Acceleration and HW resources used.*

# 2. Installation

## 2.1 Download the BSP for SDSoC 2015.4 and Demos

This application note can be downloaded as file [7]:
http://sp.utia.cz/results/s30i1h2/s30i1h2_2015_4.pdf
from UTIA public www server page [8]:
http://sp.utia.cz/index.php?ids=results&id=s30i1h2

The UTIA BSP package and demos can be downloaded from this page after registration. Fill your name and your e-mail). UTIA server will send to you the download link to the e-mail you have provided. It is link to your temporary copy of the package created for your download. You will download the zip file:
**s30i1h2.zip**

Unzip the **s30i1h2.zip** content to the directory **C:\S** to get this file structure on your PC:
**C:\S\s30i1h2_S54_IMPORT**
**C:\S\s30i1h2**
**C:\S\s30i1h2_S54_boot_files**

The first directory includes SDSoC 2015.4 demos to be imported into new SDSoC 2015.4 project.
The second directory includes the SDSoC 2015.4 board support package **"hio"** for the Sundance EMC2-DP-V2 platform [3] with industrial grade Zynq XC7Z030-1I device on System on Module TE0715-03-30-1C or TE0715-03-30-1I [1] with the Full HD HDMII-HDMIO support.
The third directory includes precompiled BOOT.bin files for SW and HW versions of included demos.

## 2.2 Installation of Avnet HDMI In and HDMI Out IP Cores

The board support package for the Sundance EMC2-DP-V2 platform works with Full HD HDMI input and Full HD HDMI output implemented on the Avnet FMC AES-FMC-HDMI-CAM-G board.
Avnet provides documentation for the AES-FMC-HDMI-CAM-G board in the www page [4]:

http://products.avnet.com/shop/en/ema/3074457345623664802

The Avnet IP cores for Vivado 2015.4 **avnet_hdmi_in** and **avnet_hdmi_out** have to be downloaded. Please, follow these steps:

1. Registration: If you are new you have to register on the Avnet server to be able to download files. Click on the green button: [SIGN IN/REGISTER]
2. After sign-in or registration, you can immediately download the file:
   **AES-FMC-HDMI-CAM-G-FMCHC_PYTHON1300C_Tutorial_2015_4_01.zip**
   from the Avnet AES-FMC-HDMI-CAM-G board www page [4].
3. Unzip the downloaded file and open the included pdf tutorial:
   **FMCHC_PYTHON1300C_Tutorial_2015_4_01.pdf**
4. Download the needed zip file with Avnet design files and IP cores (as described in section Experiment 2 on page 4-5) of the Avnet tutorial:
   **hdl-fmchc_python1300c_PZ7030_FMC2_20160223_221823.zip**
5. Zio file includes the needed Vivado 2015.4 IP cores for Avnet the AES-FMC-HDMI-CAM-G:
   **\IP\avnet_hdmi_in**
   **\IP\avnet_hdmi_out**
   **\IP\interfaces**

The BSP package **s30i1h2.zip** downloaded from UTIA server contains an empty directory:
**C:\s30i1h2\hio\vivado\hio.ipdefs\ip-imageon_0**

Copy the downloaded Avnet IP cores to this empty directory to get following file structure of the BSP:

**C:\s30i1h2\hio\vivado\hio.ipdefs\ip-imageon_0\avnet_hdmi_in**
**C:\s30i1h2\hio\vivado\hio.ipdefs\ip-imageon_0\avnet_hdmi_out**
**C:\s30i1h2\hio\vivado\hio.ipdefs\ip-imageon_0\interfaces**

The **"hio"** BSP for the Sundance EMC2-DP-V2 platform [3] with industrial grade Zynq XC7Z030-1I device on System on Module TE0715-03-30-1C or TE0715-03-30-1I [1] with the Full HD HDMII-HDMIO support is complete and ready for use and all needed IP cores are installed to the SDSoC 2015.4 now.

## *2.3 Download Trenz-Electronic Board Description Files for TE0715-03-30-1I*

The SDSoC 2015.4 board support package is Vivado 2015.4 project with some meta-data. It works with the Zynq xc7z030-1I part on the TE0715-03-30-1C or TE0715-03-30-1I system on module. This Vivado 2015.4 project requires actual board description files for this module named TE0715-30-1C. This set of files can be downloaded from the Trenz-Electronic server. Please, follow these steps.

1. Open www page:
   https://shop.trenz-electronic.de/en/TE0715-03-30-1I-Xilinx-Zynq-Z-7030-SoC-Micromodule-XC7Z030-1SBG485I-ind.-temp.-range

2. Switch to the sub-page Downloads and follow this selection path:
   **Reference Designs** -> **2015.4** -> **test_board**. Download the needed file:

   **te0715-test_board_noprebuilt-vivado_2015.4-build_32_20160504095525.zip**

3. This file contains the needed Vivado 2015.4 board description files **TE0715-30-1C**

   **test_board\board_files\TE0715-15-1C**
   **test_board\board_files\TE0715-30-1C**
   **test_board\board_files\TE0715-30-3E**

Copy these directories with all files to the installation directory of the SDSoC 2015.4.
You have to get this file structure:

**C:\Xilinx\SDSoC\2015.4\Vivado\2015.4\data\boards\board_files\TE0715-15-1C**
**C:\Xilinx\SDSoC\2015.4\Vivado\2015.4\data\boards\board_files\TE0715-30-1C**
**C:\Xilinx\SDSoC\2015.4\Vivado\2015.4\data\boards\board_files\TE0715-30-3E**

This path is valid for a default location of Xilinx SDSoC 2015.4 tools. If your SDSoC installation is different, use that different location.

SDSoC 2015.4 is calling its Vivado 2015.4 installation. The expected board description files will be found in TE0715-30-1C.

The board description files for the TE0715-03-30-1C or TE0715-03-30-1I module are ready for use, now.

Installation steps described in sections 2.1, 2.2 and 2.3 have to be done only once.

## 2.4 Import BSP and SW Demos to new Xilinx SDSoC 2015.4 Project

Start Xilinx SDsoC 2015.4 and select the directory **C:\S\s30i1h2** as your workspace. See Figure 15.

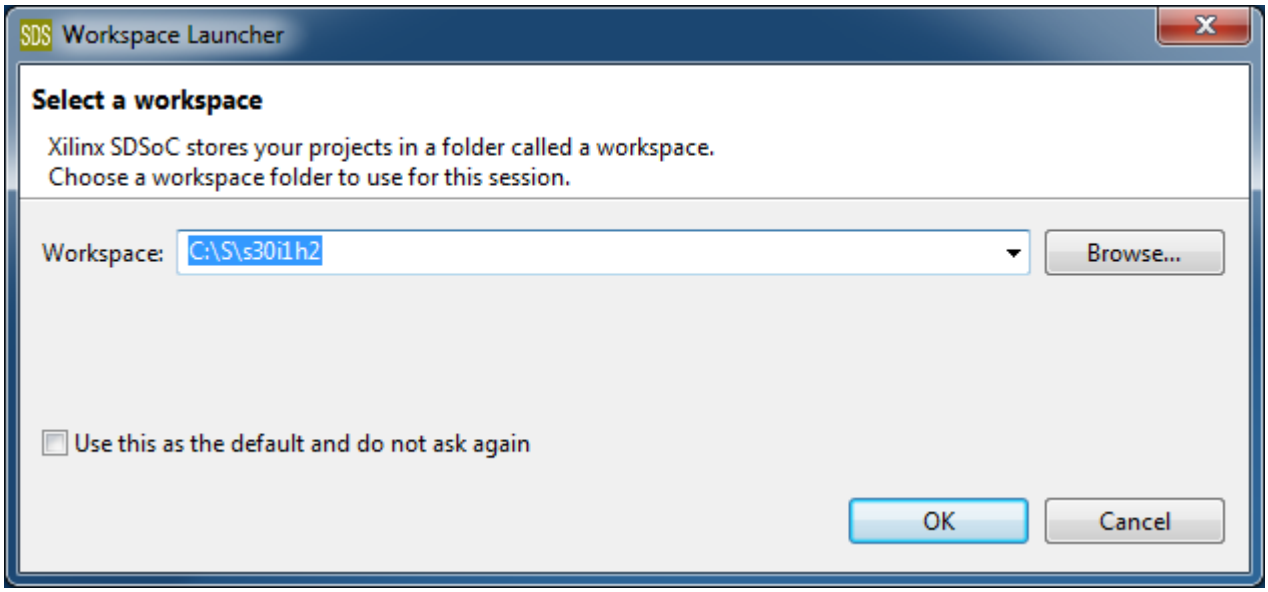



*Figure 15: Select the SDSoC 2015.4 workspace.*

Demo projects can be imported into the SDSoC 2015.4 now. Select:
**File -> Import -> General -> Existing Projects into Workspace**
Click on Next button. See Figure 16.

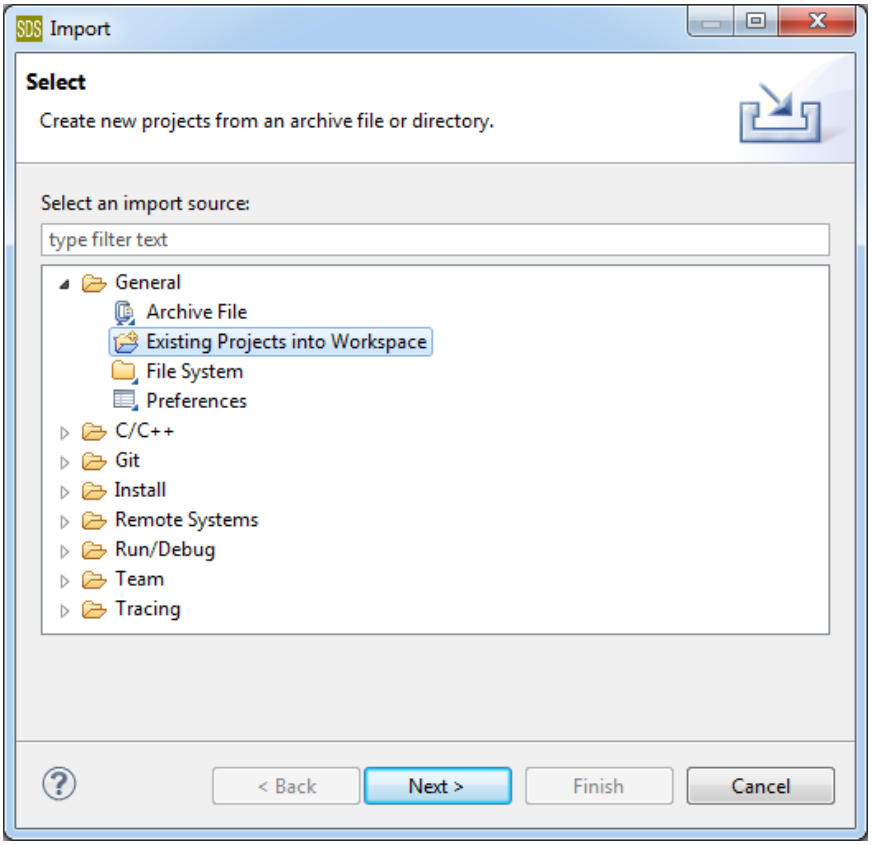



*Figure 16: Import existing demos into the SDSoC 2015.4 workspace.*

Type directory with projects to be imported. See Figure 17.

**C:\S\s30i1h2_S54_IMPORT**

Set the "**Copy projects into workspace**" check box.
Click on Finish button. See Figure 17. Click Finish and projects are imported.

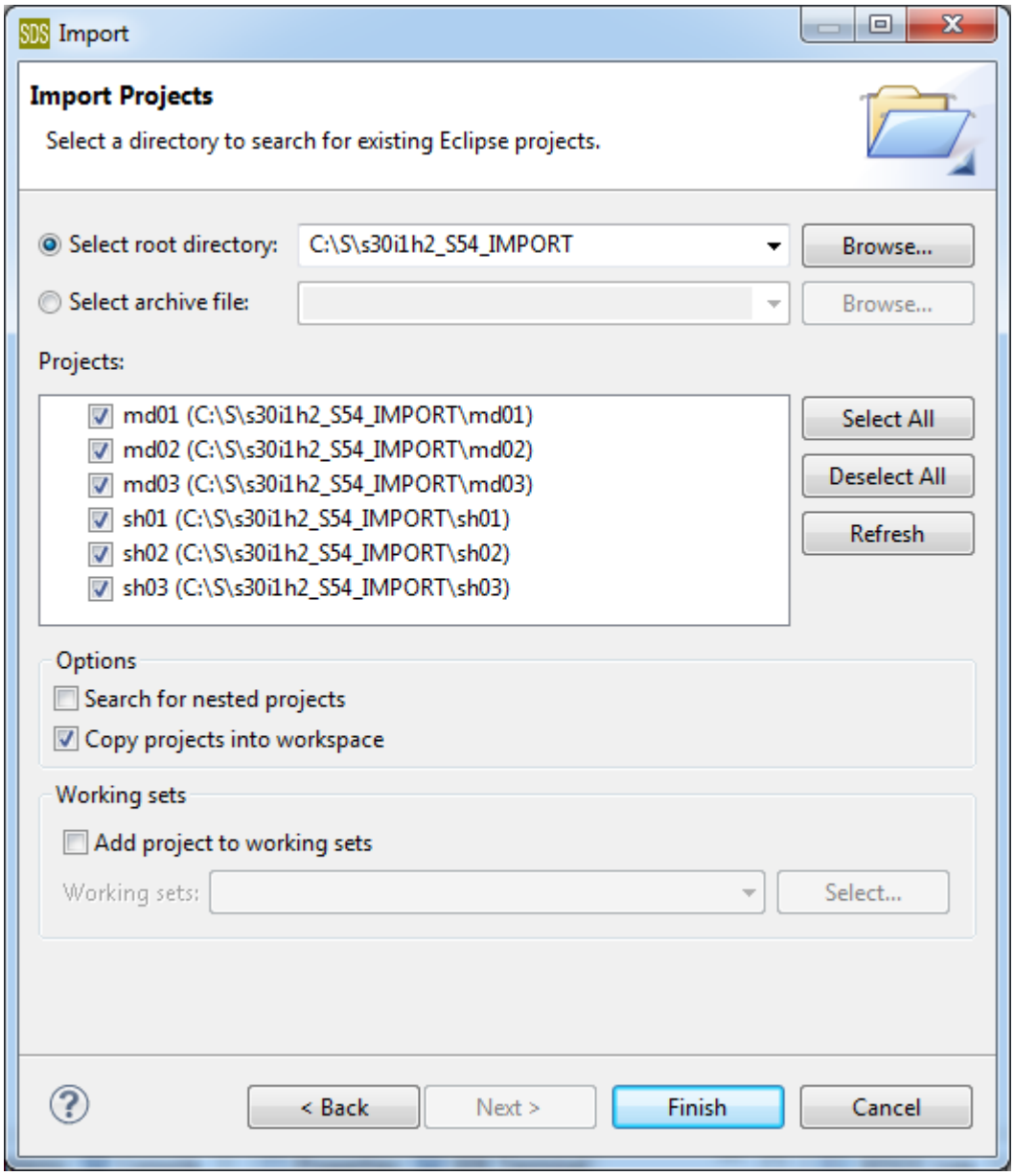



*Figure 17: Select "Copy projects into workspace" and finish the import of all projects.*

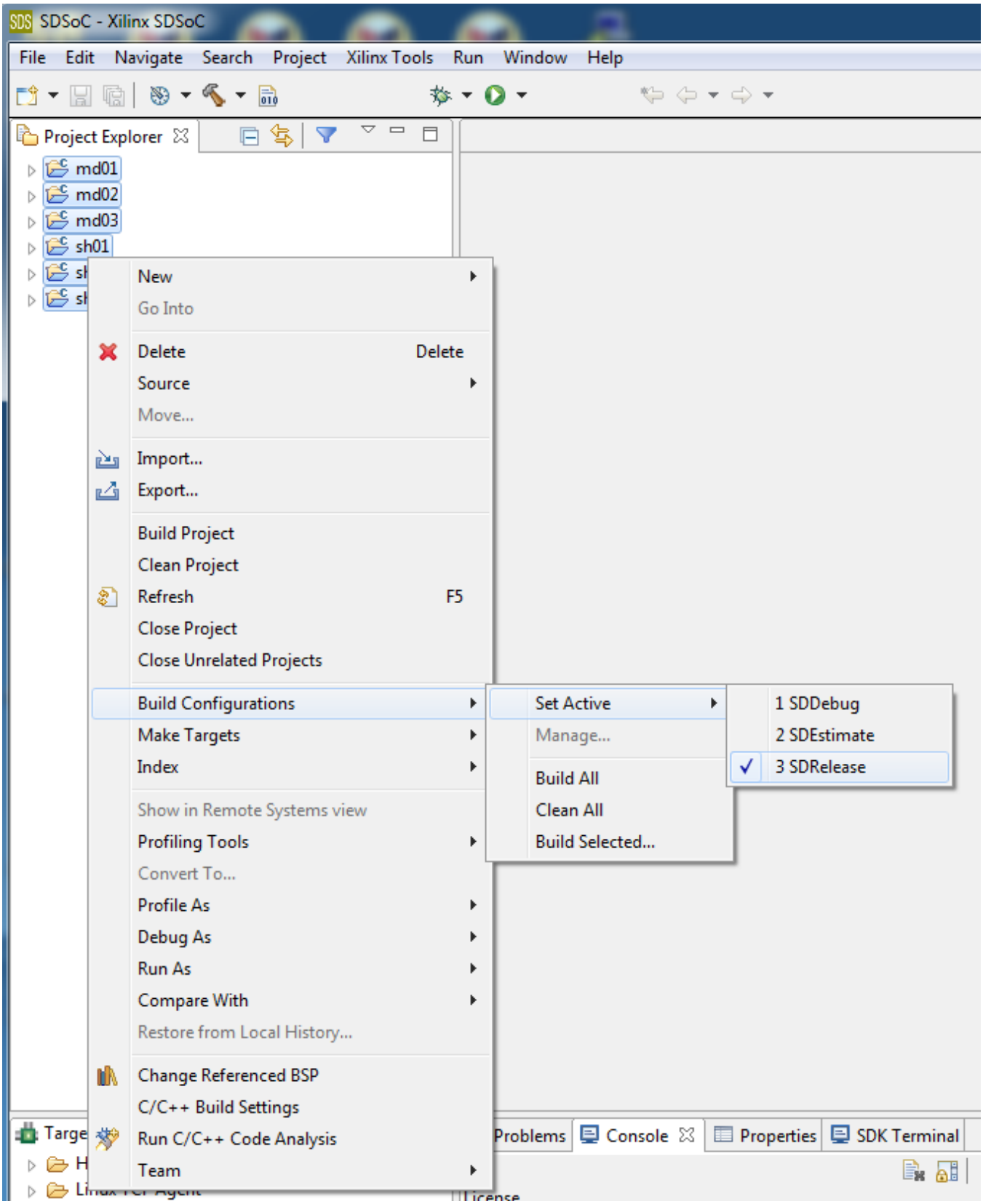



*Figure 18: Select all projects to be compiled in SDRelease mode.*

The SDSoC 2015.4 environment compiles all imported demos in SDDebug mode by default. This default helps for debugging of ARM C code, but the real-time performance is lower.

Keep all projects highlighted and select the SDRelease mode for all imported projects to get maximal performance of SW demos. Keep all projects highlighted and select “Build project”. This will compile the ARM SW version of all imported projects.

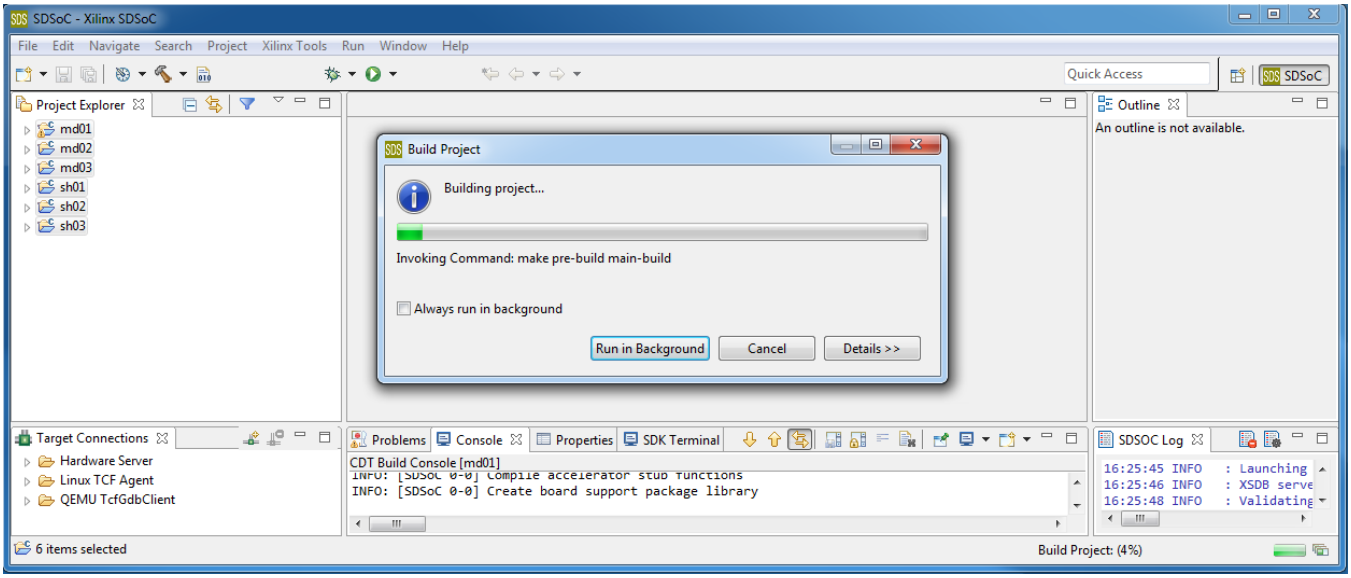



*Figure 19: All projects are compiled in SDRelease mode.*

SDSoC 2015.4 compiler compiles all imported demos. It takes approximately 1 minute for each project.

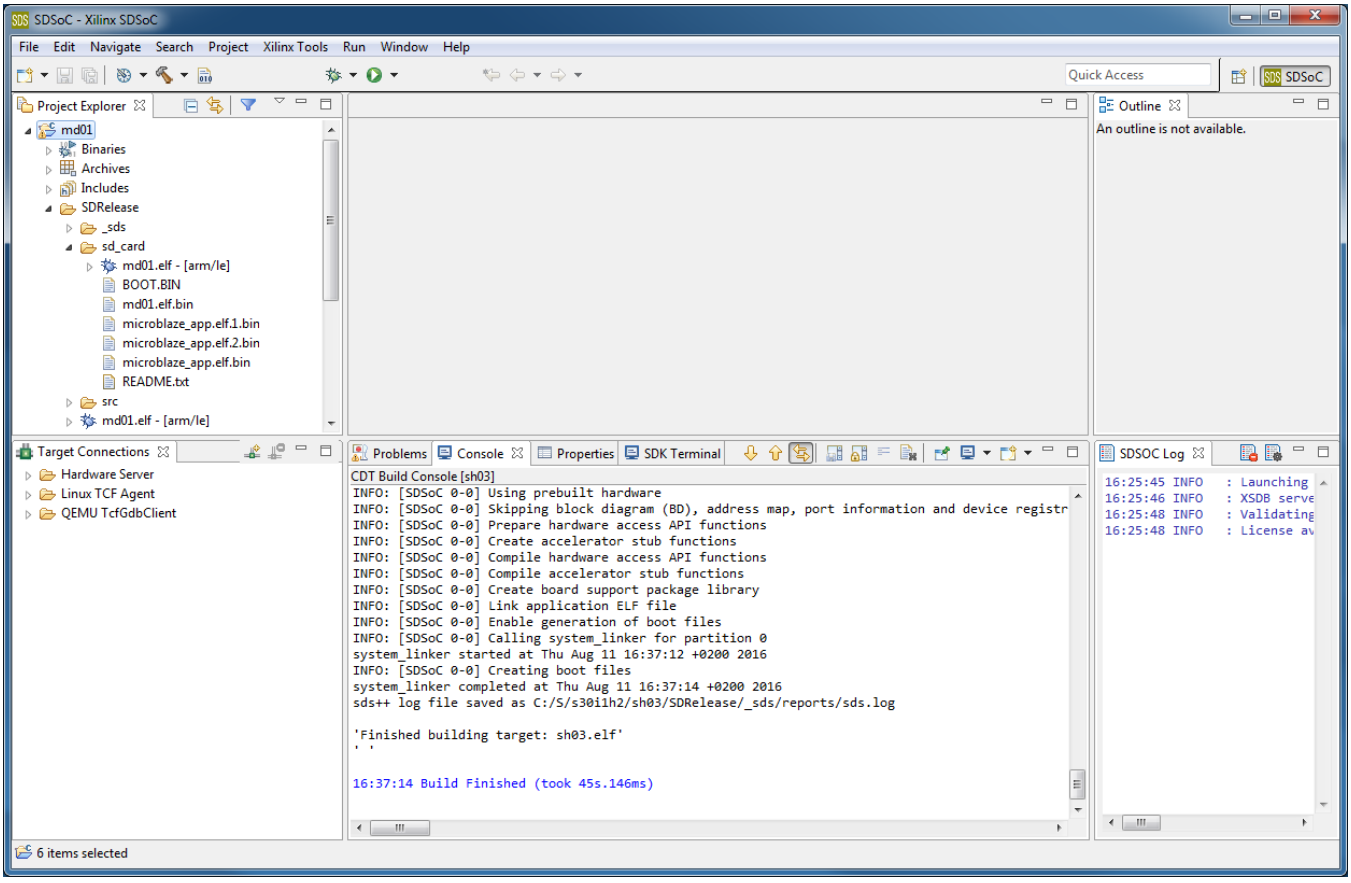



*Figure 20: All projects are compiled in debug mode.*

SDSoC 2015.4 compiled all imported projects in SDRelease mode for standalone execution on ARM processor.

Results of the compilation are the executable .elf files for ARM. These files are packed by the SDSoC 2015.4 together with the first stage boot loader executable and bitstream to the BOOT.bin files created for each project. The generated BOOT.bin files can be used for boot from the micro-SD card after the power-ON of the board.

See next Chapter for explanations how to set up the HW board and how to test the compiled HW-accelerated projects on the board.

## 2.5 Compilation to HW from SW source code in SDSOC 2015.4

Select SW functions for HW acceleration as indicated in Table 1. See Figure 21.

| Demo | Select C/C++ functions for HW acceleration |
|---|---|
| **sh01** | sobel_filter_htile1 |
| **sh02** | sobel_filter_htile1<br>sobel_filter_htile2 |
| **sh03** | sobel_filter_htile1<br>sobel_filter_htile2<br>sobel_filter_htile3 |
| **md01** | combo_image diff_image ext median_char_filter_pass pad sobel_filter sobel_filter_pass |
| **md02** | combo_image1 diff_image1 ext1 median_char_filter_pass1 pad1 sobel_filter1 sobel_filter_pass1<br>combo_image2 diff_image2 ext2 median_char_filter_pass2 pad2 sobel_filter2 sobel_filter_pass2 |
| **md03** | combo_image1 diff_image1 ext1 median_char_filter_pass1 pad1 sobel_filter1 sobel_filter_pass1<br>combo_image2 diff_image2 ext2 median_char_filter_pass2 pad2 sobel_filter2 sobel_filter_pass2<br>combo_image3 diff_image3 ext3 median_char_filter_pass3 pad3 sobel_filter3 sobel_filter_pass3 |

*Table 1: Selection of C/C++ functions for HW compilation in all demos*

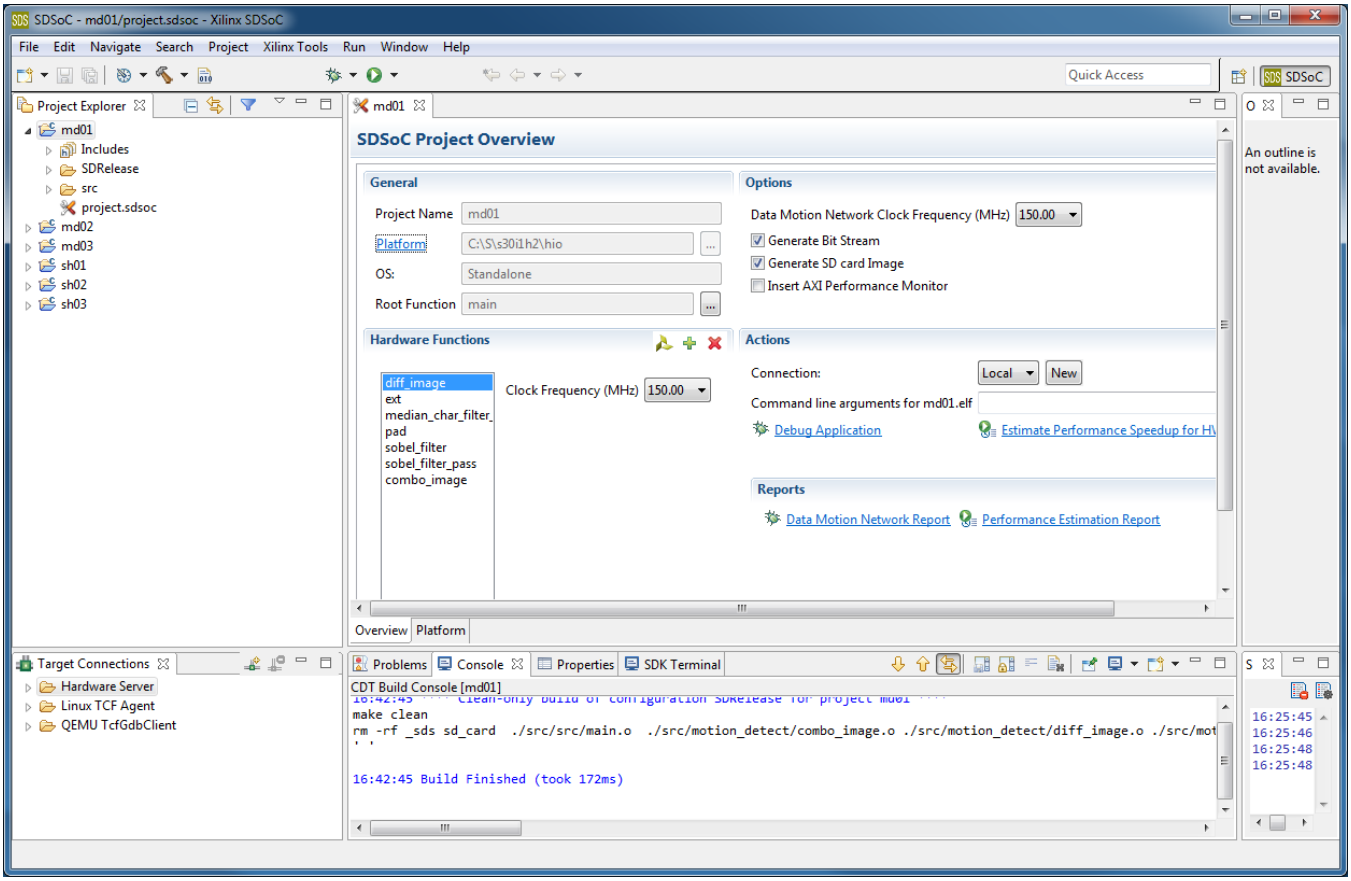



*Figure 21: Selection of C/C++ functions for HW compilation in demo md01.*

HW accelerated projects can be compiled separately or in a single batch. Results of the compilation are again standalone .elf files for ARM processor. Each .elf file is packed together with the first stage boot loader executable and the new bitstream (with the new HW) to the SDRelease BOOT.bin file.

Time needed for compilation to HW (Intel i5 processor; 64bit; 3.4 GHz; RAM 32 GB):
sh01 **29 min**; sh02 **39 min**; sh03 **47 min**; md01 **51 min**; md02 **82 min**; md03 **114 min**.

Use the generated BOOT.bin files to test the HW demos by boot of the board from the micro-SD card.

## 2.6 HW setup

HW setup is using commercially accessible components [1], [2], [3], [4]:

**TE0715-03-30-1C** or **TE0715-03-30-1I**, Part: xc7z030sbg485-1C or -1I; 1 GByte DDR3; [1]
**Heatsink for TE0715**, spring-loaded embedded; [2]
**EMC2-DP-V2 Carrier Board,** EMC²-DP PC/104 OneBank Carrier for SoC Modules [3]
**AES-FMC-HDMI-CAM-G,** FMC card with HDMI I/O and CAM interface [4]

EMC2-DP-V2 Carrier Board [3] requires one modification to run the demos on AES-FMC-HDMI-CAM-G with Zynq TE0715-03-30-1C or TE0715-03-30-1I system on module. The modification is related to the swapped polarity of the differential clock signal for the AES-FMC-HDMI-CAM-G FMC board on the Zynq TE0715-03-30-1C or TE0715-03-30-1I SoM module [1].

UTIA can implement these necessary HW modifications for the original EMC2-DP-V2 Carrier Board [3] from Sundance. This requires written e-mail request to kadlec@utia.cas.cz . Request will be first confirmed by UTIA. The interested party has to cover the cost of the shipment of the original EMC2-DP-V2 carrier board. Modification can be done in 5 working days and it is offered free of charge.

## 2.7 Test demos

To test demos follow these steps:
**Initial setup:**

- Start with EMC2-DB-V2 with switch-OFF power supply.
- Connect source of the Full HD HDMI signal (usually PC or laptop) to the HDMI IN connector on the AES-FMC-HDMI-CAM-G FMC card.
- Connect Full HD (or DVI) monitor by HDMI cable to the HDMI OUT on the AES-FMC-HDMI-CAM-G FMC card.
- Switch the HDMI monitor ON.
- Connect the carrier board by USB-to-microUSB cable to PC to support serial terminal.

**For each demo:**

- On PC, copy BOOT.bin file to the top directory of the micro SD card.
- Enter the SD card to the switched off EMC2-DB-V2.
- Switch-ON the power supply for the EMC2-DB-V2 board.
  - The first stage boot loader boots the bitstream and the application to the ARM Cotex A9 processor. The source of 1920x1080p60 video signal (PC or Laptop) connects to the EMC2-DB-V2 board like to a Full HD HDMI monitor. The EMC2-DB-V2 board connects to the Full HD HDMI output monitor. This initial process takes few seconds.
  - The processed video signal is displayed with fixed resolution 1920x1080p60 on the display.
- At this stage it is possible to open and configure the standard serial terminal client (PuTTY or similar) on your PC to see information printed from the currently running application. All applications use terminal setting: *115200 bit/sec; Data bits: 8; Stop bits: 1; Parity: None; Flow control: None.*
- On your PC, terminate the terminal client before switch-OFF the EMC2-DB-V2 board.
- Switch-OFF power supply of EMC2-DB-V2 board to stop the demo.

# 3. References


[1] Xilinx Zynq Z-7030 SoC Micromodule XC7Z030-1SBG485I (ind. temp. range)
https://shop.trenz-electronic.de/en/TE0715-03-30-1I-Xilinx-Zynq-Z-7030-SoC-Micromodule-XC7Z030-1SBG485I-ind.-temp.-range

[2] Heatsink for TE0715, spring-loaded embedded;
https://shop.trenz-electronic.de/en/26923-Heatsink-for-TE0715-spring-loaded-embedded

[3] EMC²-DP PC/104 OneBank Carrier for SoC Modules
http://www.sundance.technology/som-cariers/pc104-boards/emc2-dp/

[4] AES-FMC-HDMI-CAM-G
http://products.avnet.com/shop/en/ema/3074457345623664802

[5] Vivado HLx Web Install Client - 2015.4 Full Product Installation
http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/2015-4.html

[6] SDSoC - 2015.4 Full Product Installation - 2015.4 Full Product Installation
http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/sdx-development-environments/sdsoc/2015-4.html

[7] Jiri Kadlec, Zdenek Pohl, Lukas Kohut: SDSoC 2015.4 Standalone BSP with Full HD HDMI In-Out with SW and HW Demos for Zynq System-on-Module TE0715-03-30 and Sundance EMC2-DP-V2 Platform. UTIA application note. Released 12.8.2016 on UTIA www server.
http://sp.utia.cz/results/s30i1h2/s30i1h2_2015_4.pdf

[8] UTIA public www server page for download of the application note [7], and the BSP package with demos for the Xilinx SDSoC 2015.4 environment.
http://sp.utia.cz/index.php?ids=results&id=s30i1h2

# 4. License

This stand-alone board support package (BSP) for the Xilinx SDSoC 2015.4 [6] for Sundance EMC2-DP-V2 platform [3] contains these deliverables:

- Board support package **"hio"** for Sundance EMC2-DP-V2 platform [3] with industrial grade Zynq XC7Z030-1I device on System on Module TE0715-03-30-1I [1].
- Three edge detection video processing demos (sh01 sh02 and sh03).
- Three motion detection video processing demos (md01, md02 and md03).

The BSP package **"hio"** includes static library for ARM Cortex A9 processor (32bit) precompiled for standalone mode:

**libfmc_imageon.a**

- It is static library with interface functions for video IP cores for standalone ARM applications.
- This library has no time restrictions.
- Source code of this UTIA library is **not** part of the package.

This package can be downloaded by a customer from the public UTIA www server **free of charge.**

UTIA is granting to the customer **the time-unlimited, non-exclusive, non-transferable license** for use of this BSP on the customer site for SW and HW designs performed in the Xilinx SDSoC 2015.4 environment [6] and targeting the Sundance EMC2-DP-V2 platform [3] with industrial grade Zynq XC7Z030-1I device on the System on Module TE0715-03-30-1I [1]

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