

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Memory, CPU-PEG/Display	3,4
CPU-Control/MISC/CFG/Audio	5
CPU-Power,CPU-GND	6,7
DDR4 1/2,DDR4-POWER/GND-1/2	8,9,10,11
PCH-USB/PCIE/DMI/SATA	12
PCH-Audio/Display/Clock	13
PCH-GPIO/USBOC#/SATASTRAP	14
PCH-LPC/SPI/SMBUS/MISC	15
PCH-Power,PCH-GND,PCH-Strap	16,17,18
PCIE SLOT-CPU(X16)	19
PCIE SLOT-PCH(X1)	20
SIO-NCT5563D-M/FAN CONTROLLOR	21,22
AUDIO - ALC892/887,AUDIO - depop circuit	23,24
LAN - RTL8111H	25
DVI/HDMI/VGA	26,27,28
USB2.0/USB3.0/SATA connector	29,30,31
CUT_VBAT circuit/BIOS ROM	32,33
ACPI CONTROLLER	34
PWM-RT3606BC/VCORE 3PHASE/VGT 2PHASE	35,36,37
DDR-RT8231/DDR-MP2147-VPP25	38,39
CPU PWR_ST/PLL	40
PCH Core power	41
VCCSA - POWER/VCCIO - POWER	42,43
ATX F_Panel/TPM/MSI_LED	44
DEBUG LED/EMI CAP/Manial Part	45,46,47
Power Map/Power Sequence/GPIO MAP	48,49,50
Revision History	51

MS-7996

ATX:235*180

Ver: 10

Intel -SkyLake-S plamform

CPU:

LGA1151

CPU POWER PAK *3 Phase

GT POWER PAK *2 Phase

System Chipset:

SPT-H :B150

SPT-H :H150

Onboard Chip:

HD Audio Codec: ALC892

SIO: NCT5563D

Flash ROM: SPI 64 MB

DP to VGA: ITE6515

PWM:

VCORE - RT3606

DDR - RT8231

PCH(1.0V) - UP1540

VCCSA - RT8125C

VCCIO - NB681(Converter)

VPP25 - MP2147

Main Memory:

DDR4 * 2 (Dual Channel)

LDO:

VCCSTPLL - GS7133

ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:GS7133+PN MOS

3VDSW:GS7133

Expansion Slots:

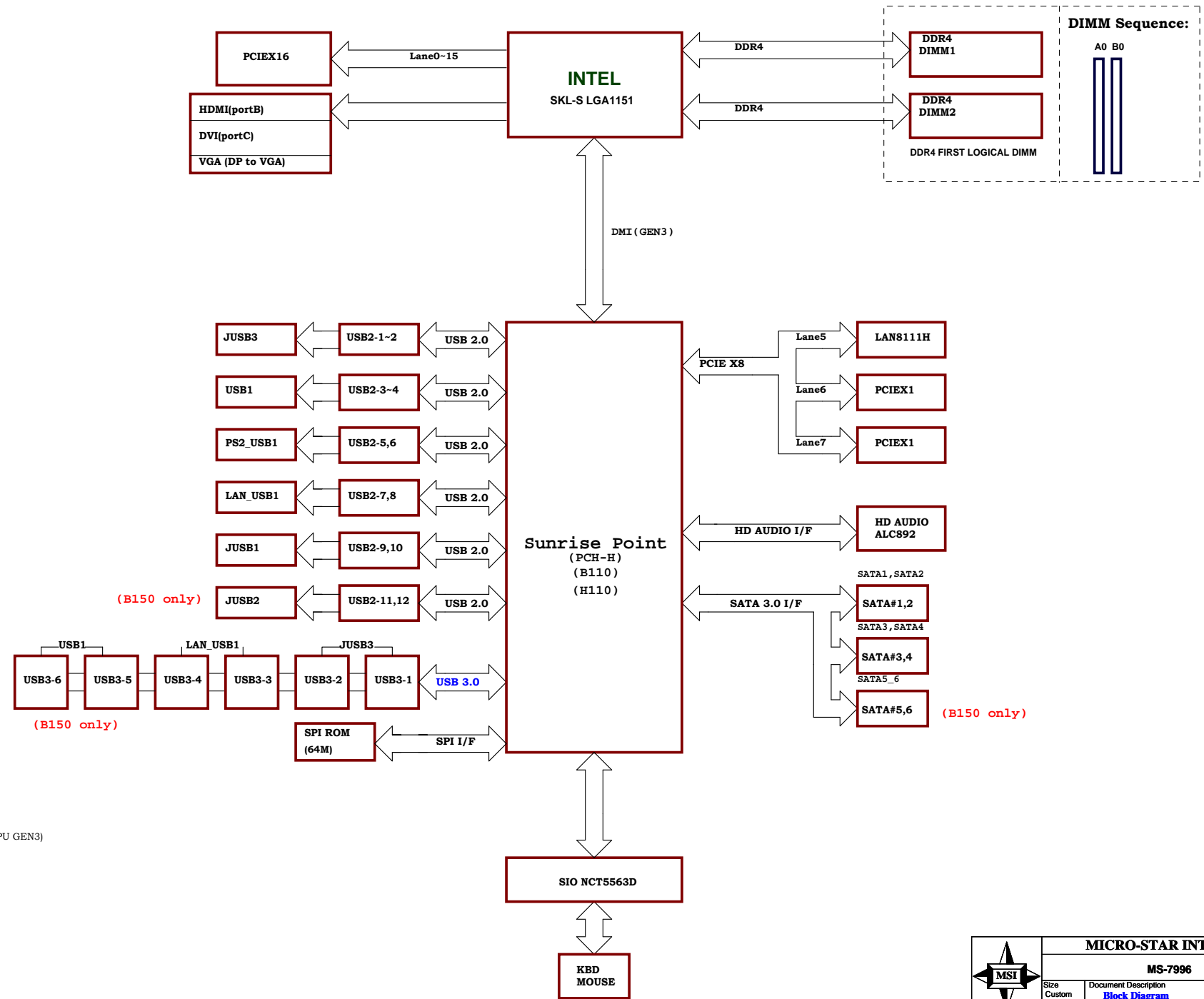
PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2



MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description Cover Sheet	Rev 10
Date: Friday, August 07, 2015	Sheet 1 of	51

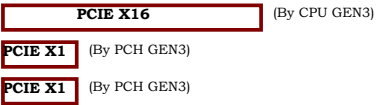
MS-7996 Block Diagram

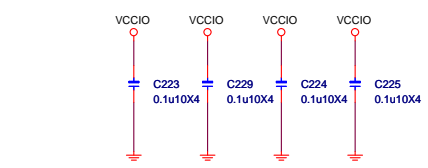
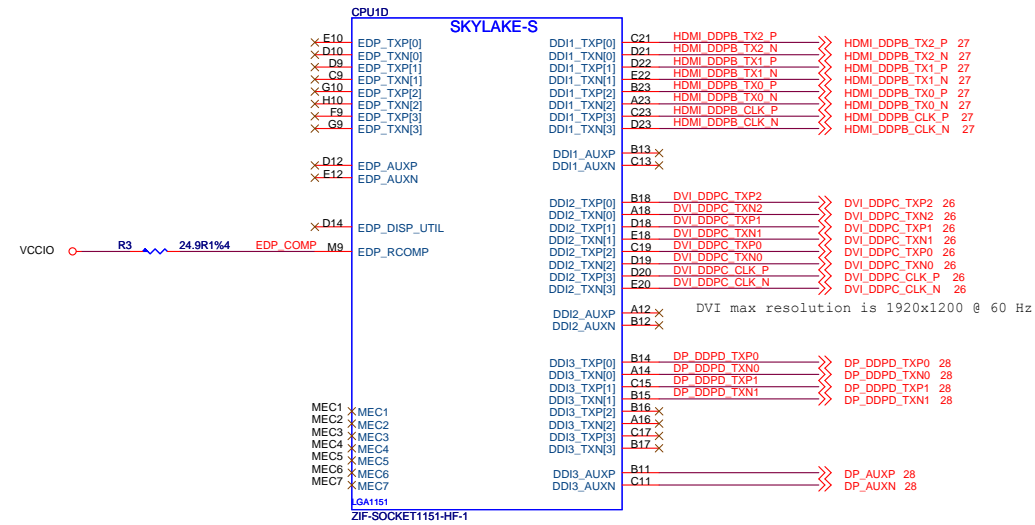
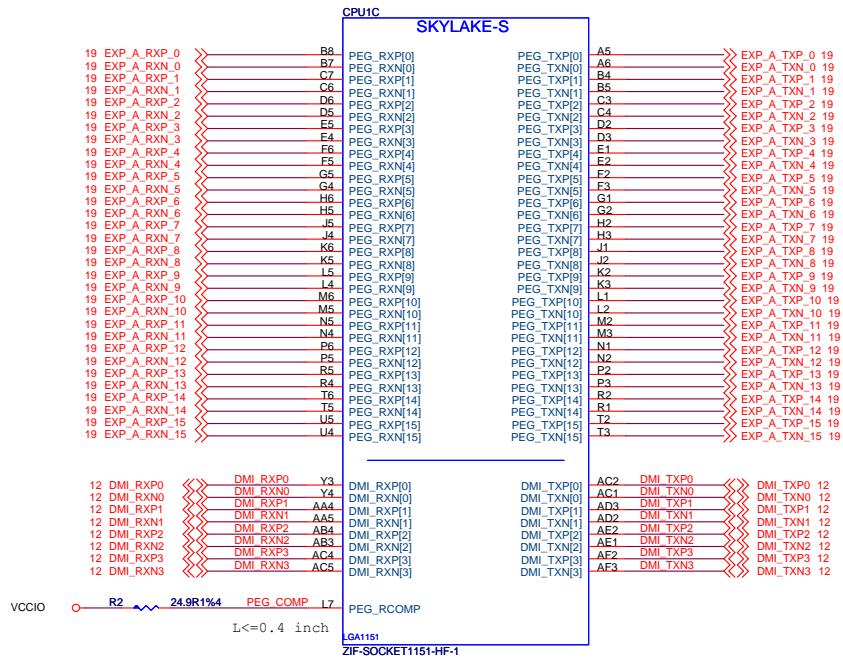


DIMM Sequence:



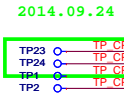
Slot Sequence:



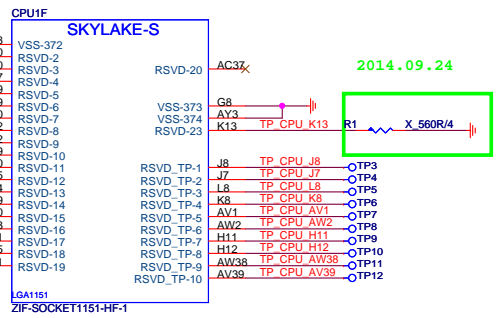
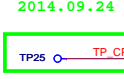


For DMI reference VCCIO USE please close to DMI via side

CRB 1.0 update
Add TP23,TP24
For Test



CRB 1.0 update
TP25
For Test



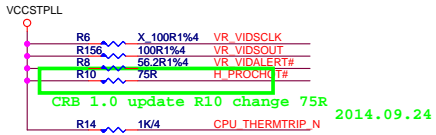
2014.09.24
CRB 1.0 update
CRB unstuff
PCB come back remove

MICRO-STAR INT'L CO.,LTD

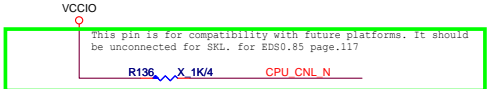
MS-7996

Size Custom Document Description CPU-PEG/Display Rev 10

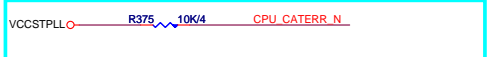
Date: Friday, August 07, 2015 Sheet 4 of 51



2014.09.24



2014.08.14

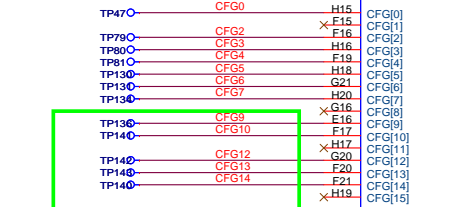
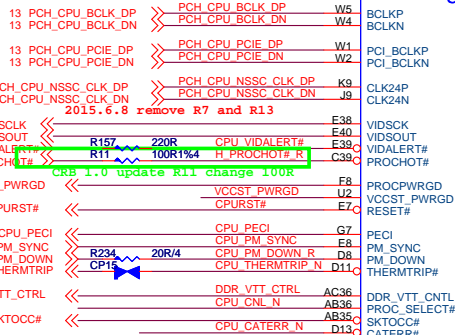


2015.04.23 for debug use

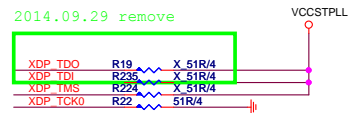
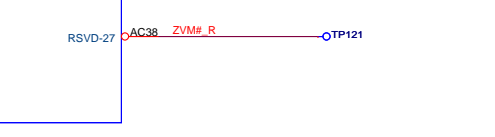
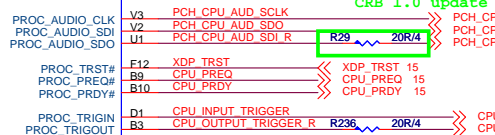
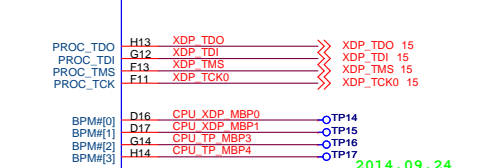
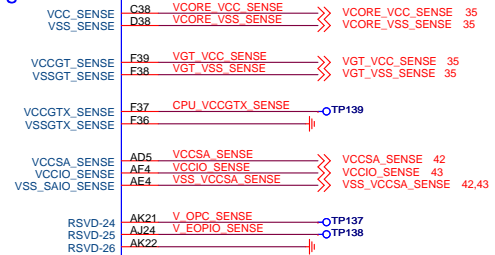
CFG Strap

CFG Table

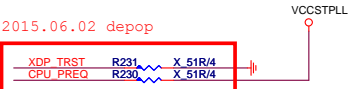
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1		RSVD	
2	NORM	REVERSE	PEG LANE REVERSAL
3		RSVD	
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIGS REQ	PEG DEFER TRAINING
8		RSVD	
9		RSVD	
10		RSVD	
11		RSVD	
12		RSVD	
13		RSVD	
14	RSVD		
15	RSVD		



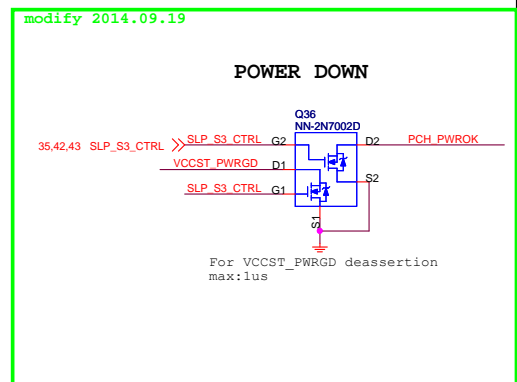
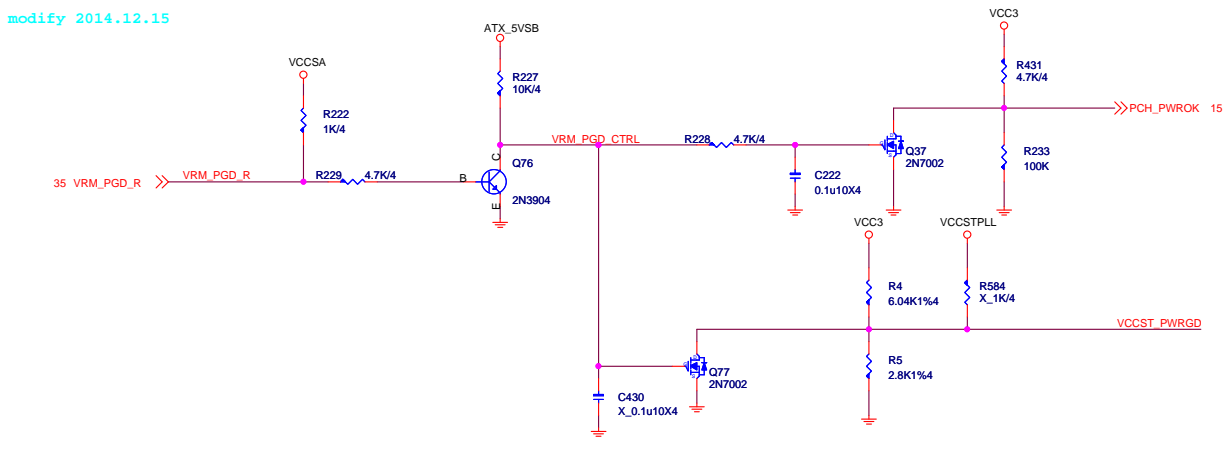
CRB 1.0 update RSVD
 Detail refer CRB 1.0
 2014.09.24



Close CPU <1100 mil
 1000 mil < CPU_XDP_MBP0~1 < 6000 mil



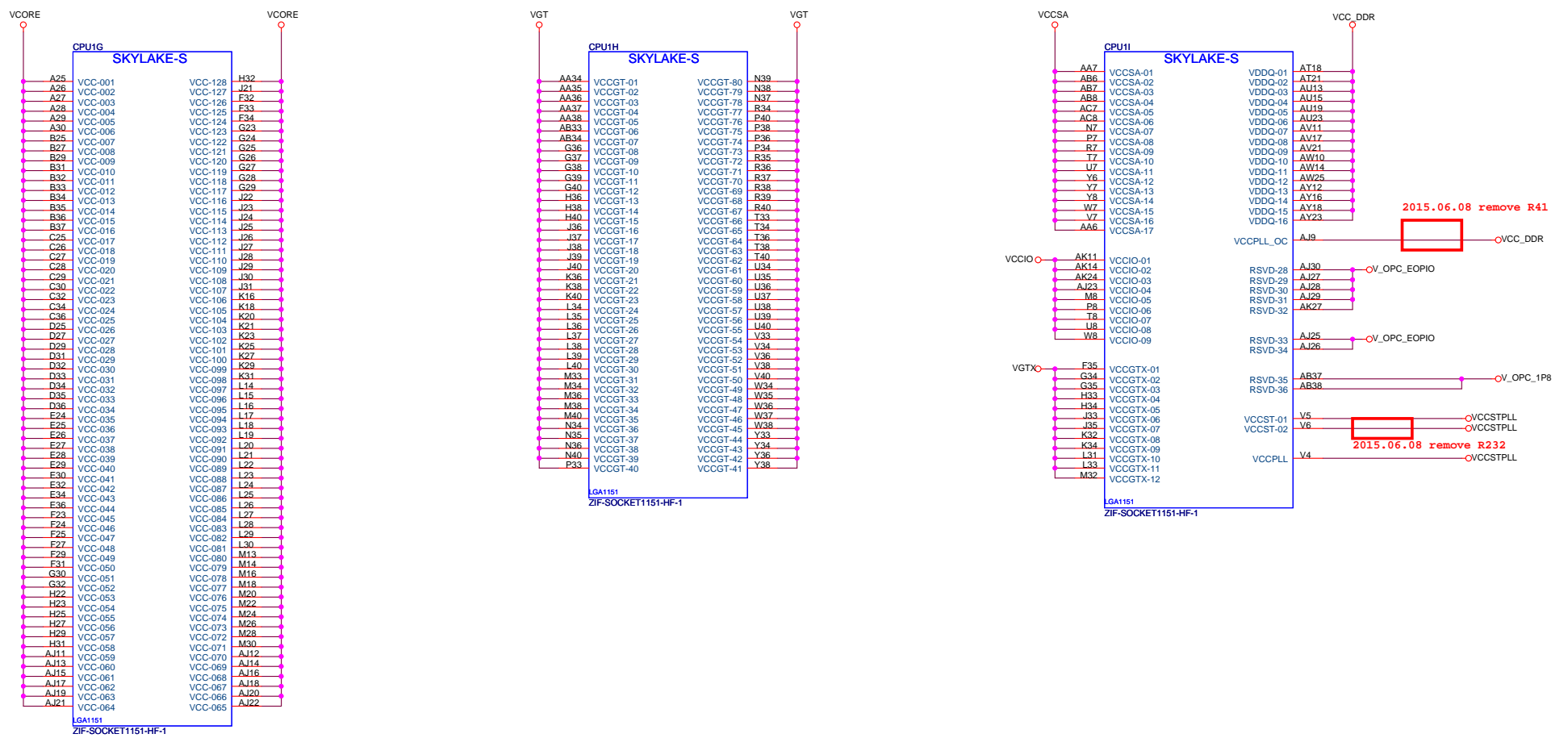
2015.06.02 depop



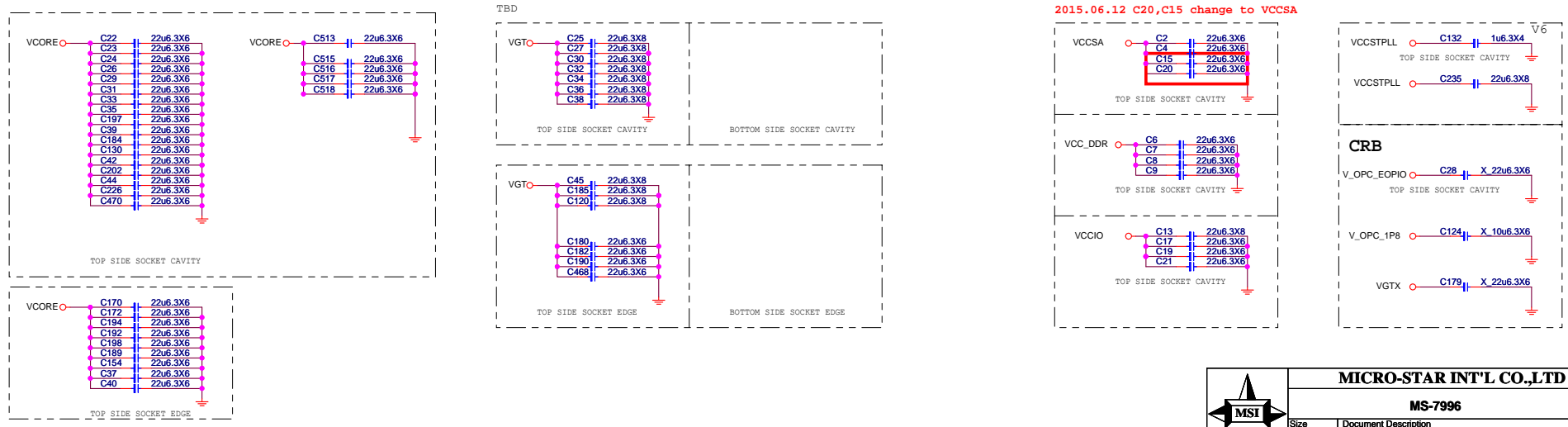
MICRO-STAR INT'L CO.,LTD

MS-7996

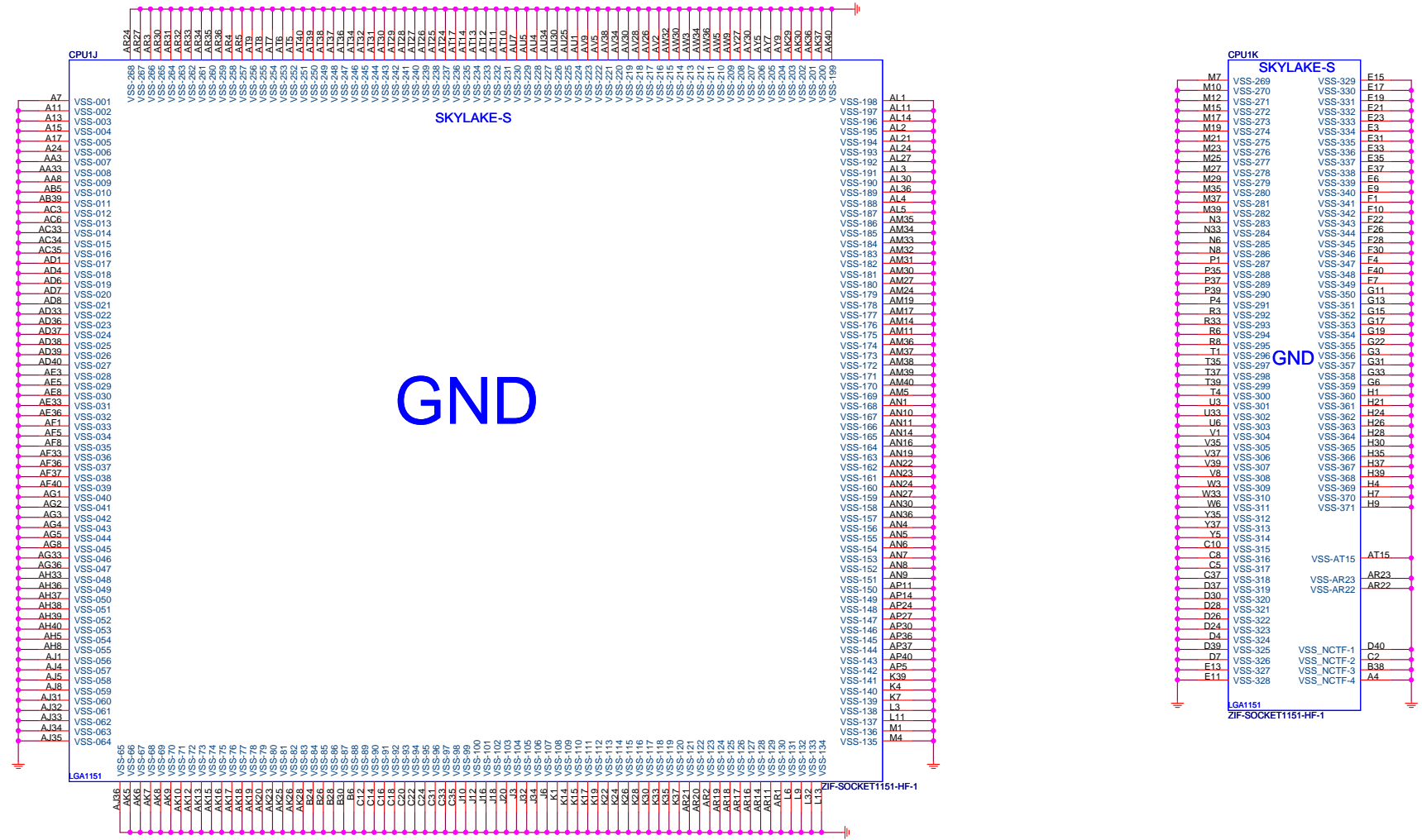
Size Custom Document Description CPU-Control/MISC/CFG/Audio Rev 10
 Date: Friday, August 07, 2015 Sheet 5 of 51

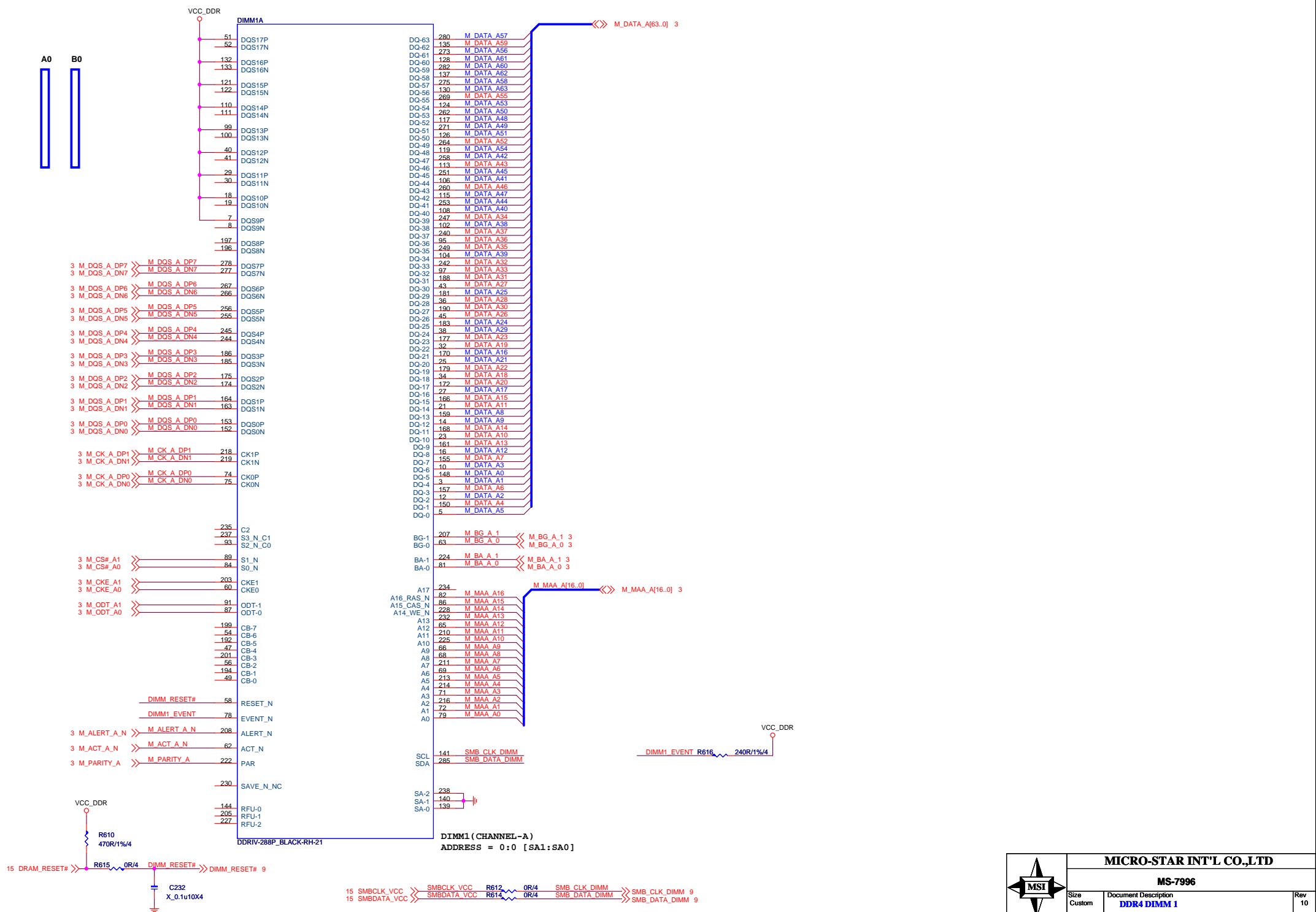


CAP

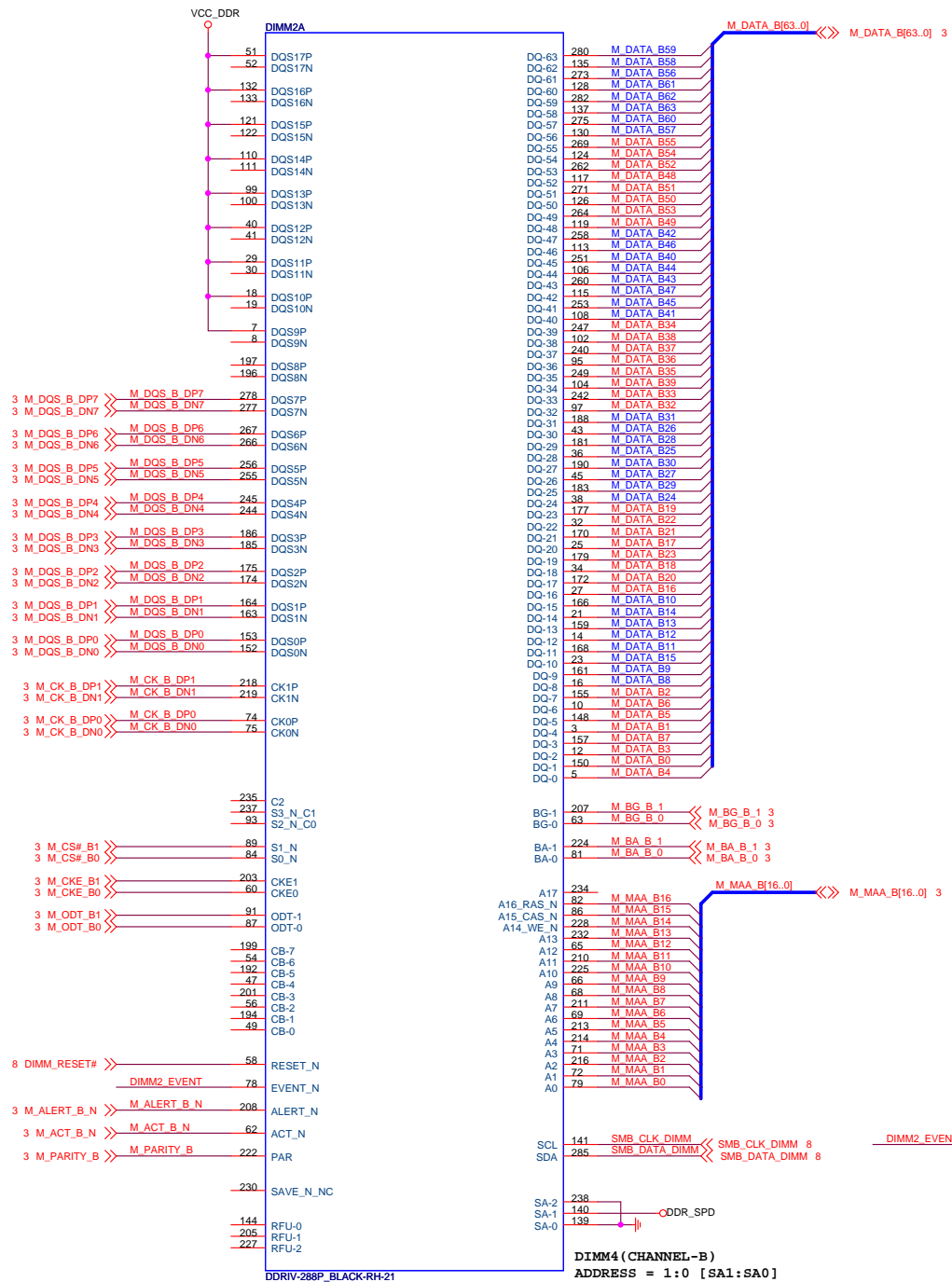


MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description CPU-Power	Rev 10
Date: Friday, August 07, 2015	Sheet 6 of 51	





MSI		
MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description DDR4 DIMM 1	Rev 10
Date: Friday, August 07, 2015		Sheet 8 of 51



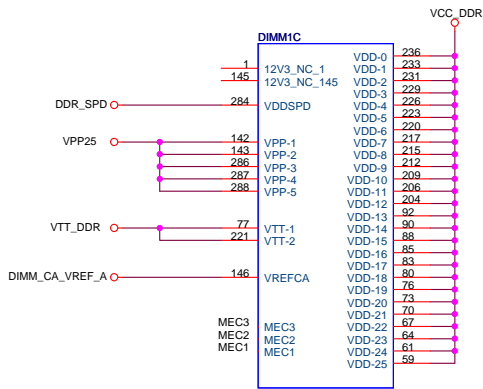
DIMM4 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]



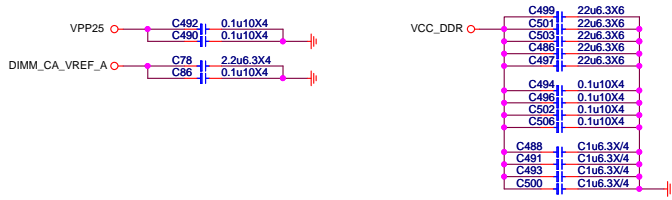
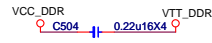
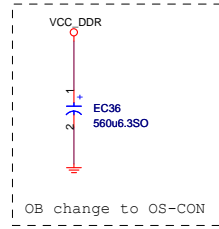
MICRO-STAR INT'L CO.,LTD

MS-7996

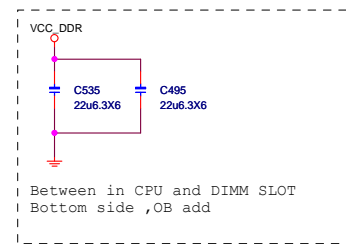
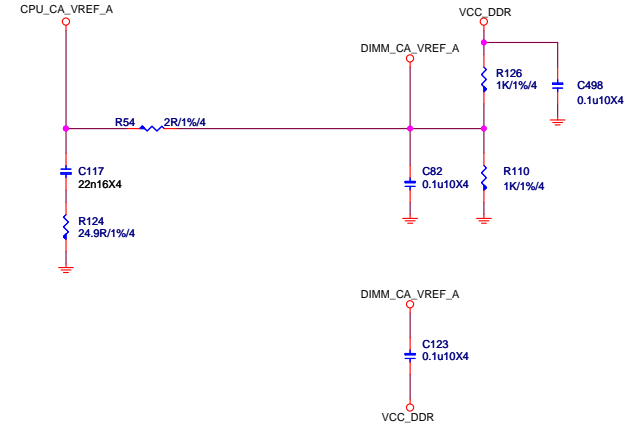
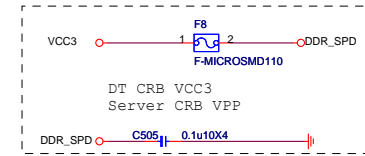
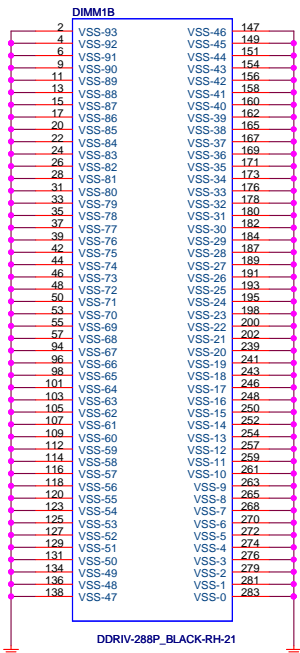
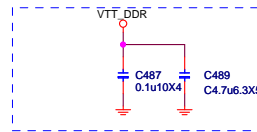
Size	Document Description	Rev
Custom	DDR4 DIMM 2	10
Date: Friday, August 07, 2015	Sheet 9 of 51	



DIMM SLOT PN BY SPEC



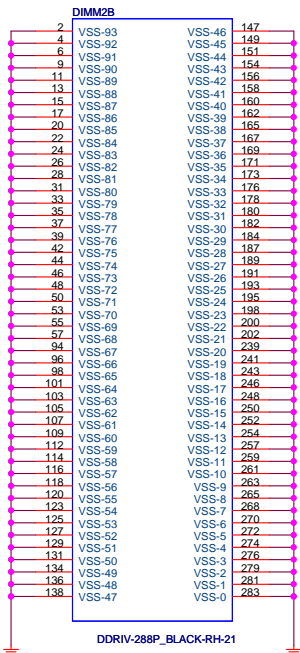
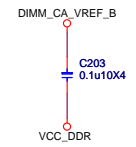
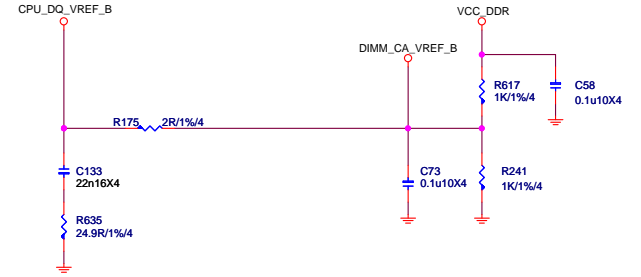
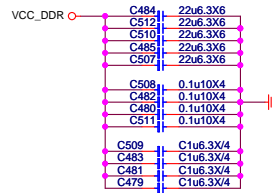
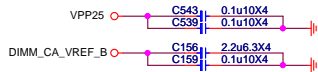
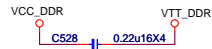
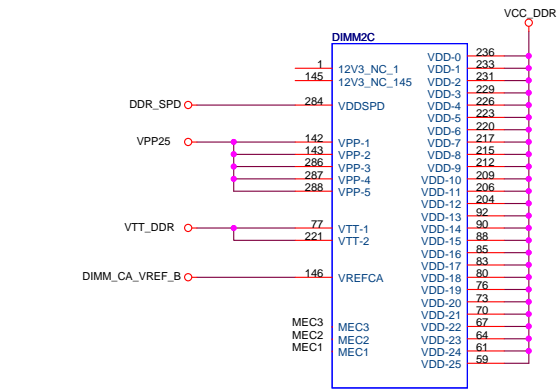
0.1uFxl per dimm



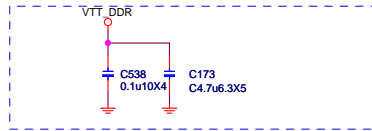
MICRO-STAR INT'L CO.,LTD

MS-7996

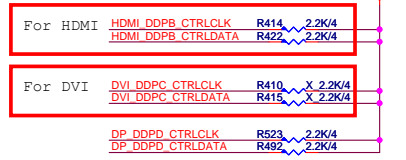
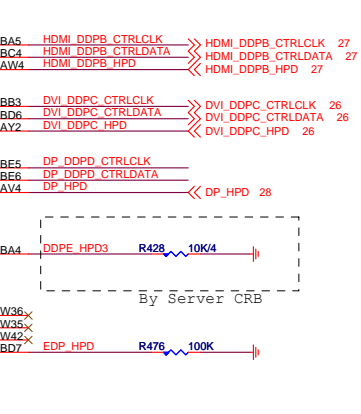
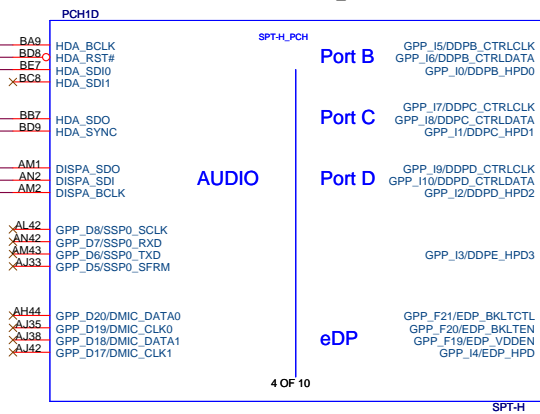
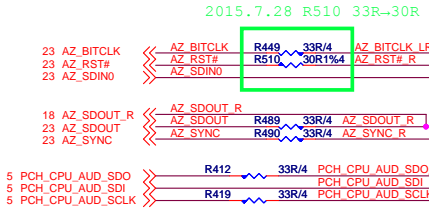
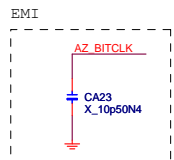
Size Custom	Document Description DDR4-POWER/GND-1	Rev 10
Date: Friday, August 07, 2015	Sheet 10 of 51	



0.1uFxl per dimm



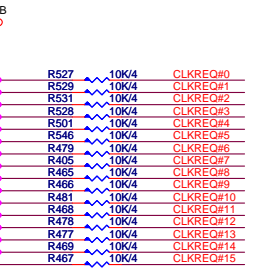
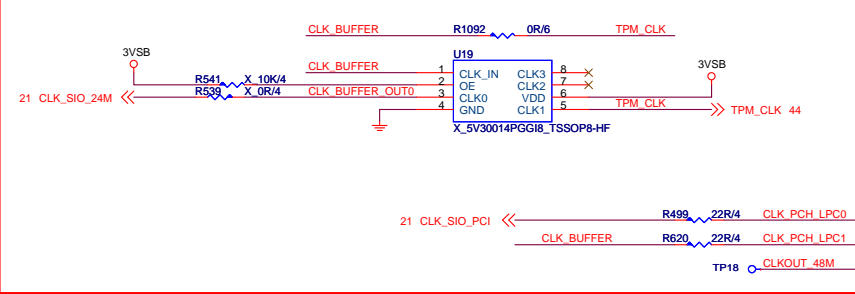
	MICRO-STAR INT'L CO.,LTD		
	MS-7996		
Size Custom	Document Description DDR4-POWER/GND-2	Rev 10	
Date: Friday, August 07, 2015		Sheet 11	of 51



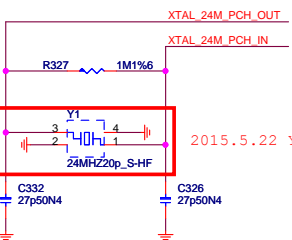
DDI interface Disable
no connect
Port B HDMI
Port C DVI, HDMI2.0 OR Others
Port D DisplayPort

2015.6.1 updata circuit

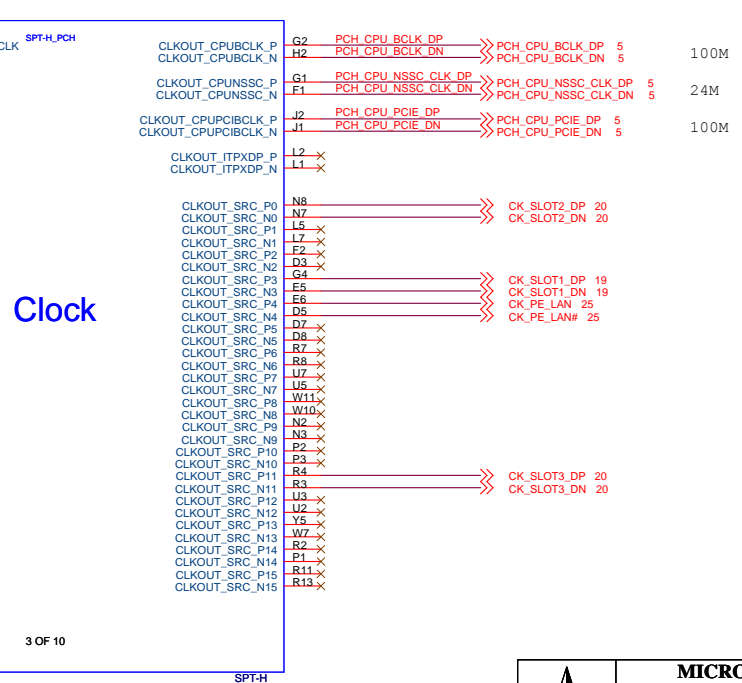
24M CLOCK BUFFER



Connct to S10T Pin B12 for support L1 PM Substates MB also can disable this funtion.



2015.5.22 Y1 change to using SMD type

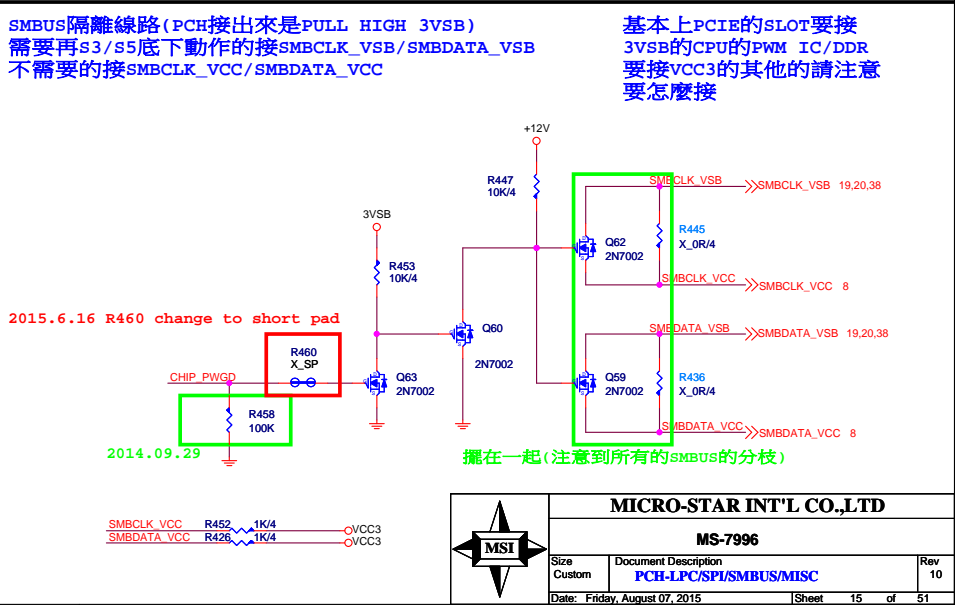
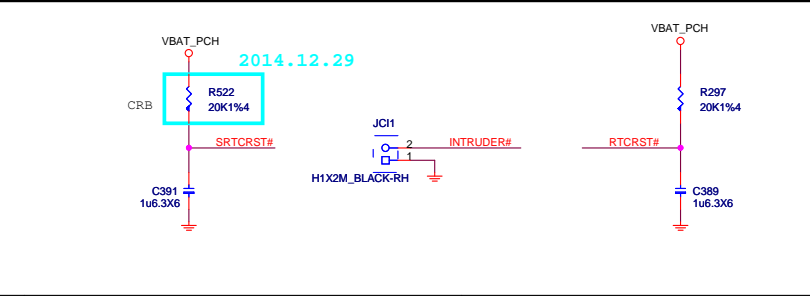
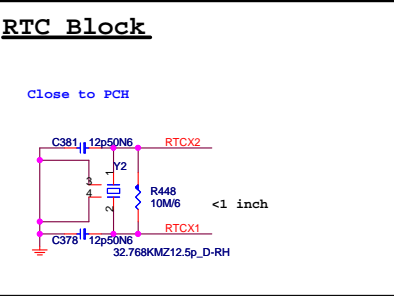
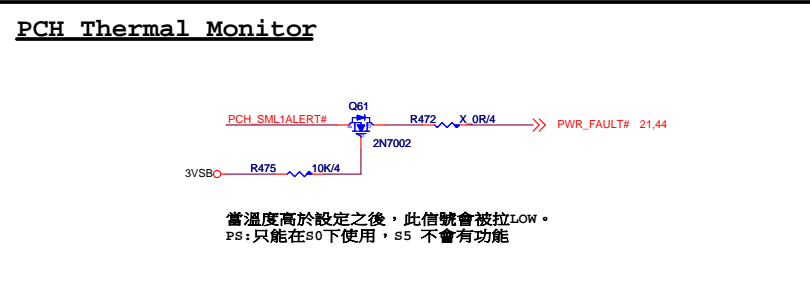
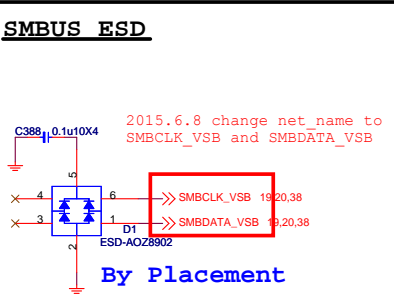
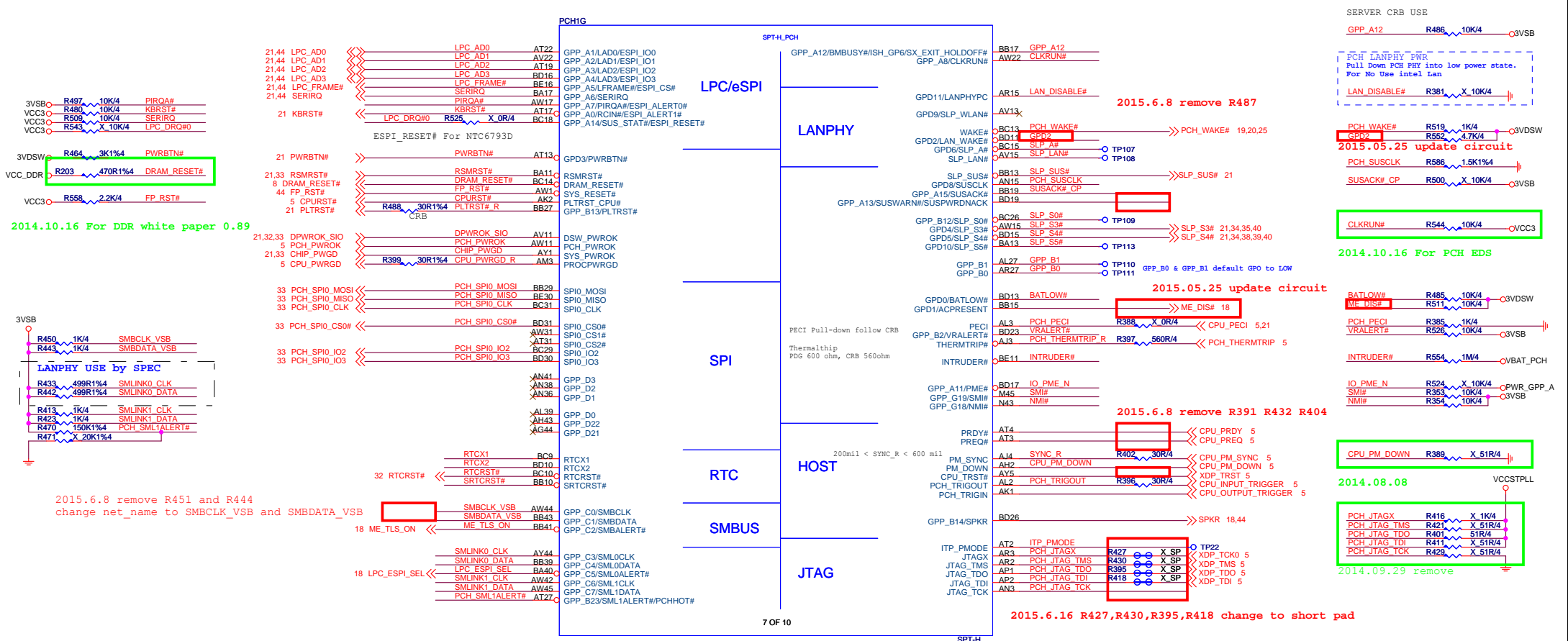


Clock

MICRO-STAR INT'L CO.,LTD

MS-7996

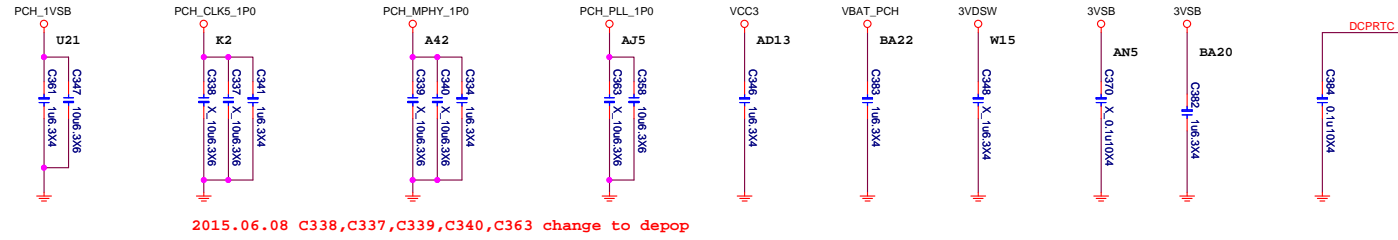
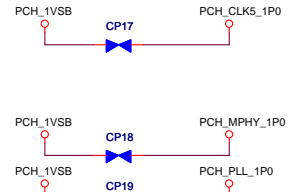
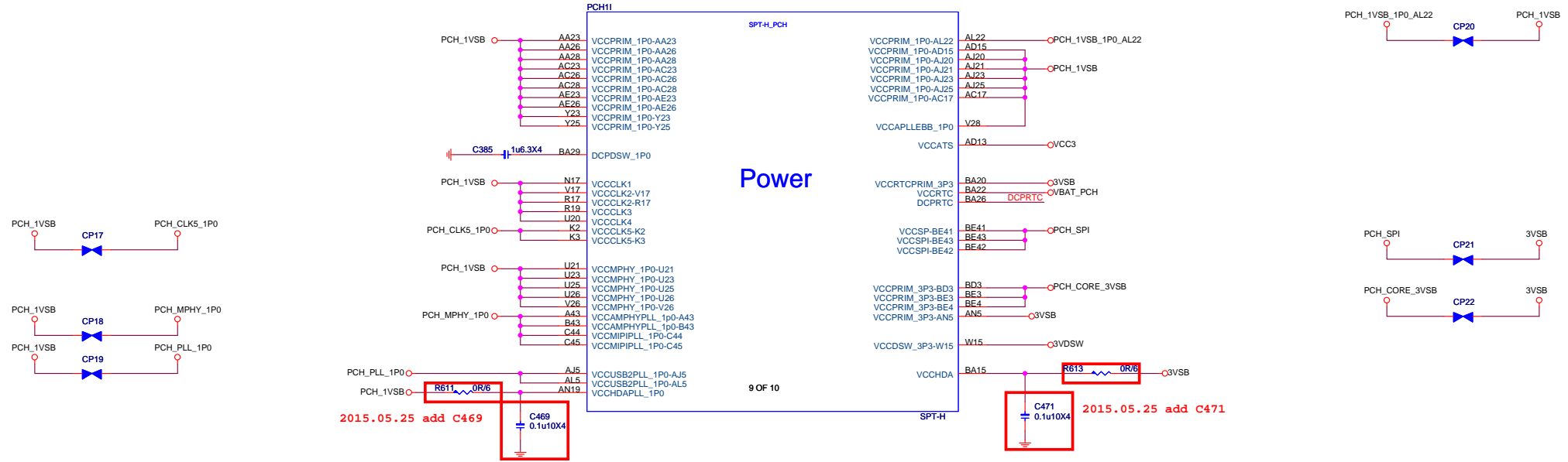
Size Custom	Document Description PCH-Audio/Display/Clock	Rev 10
Date: Friday, August 07, 2015	Sheet 13 of 51	



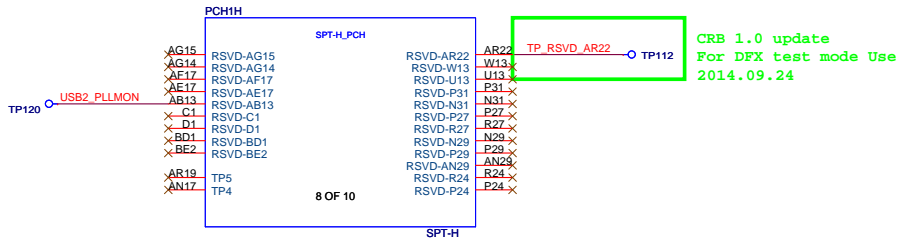
MICRO-STAR INT'L CO.,LTD

MS-7996

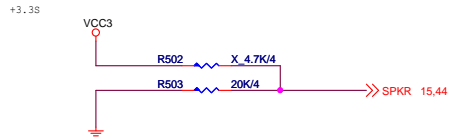
Size	Document Description	Rev
Custom	PCH-LPC/SPI/SMBUS/MISC	10
Date:	Friday, August 07, 2015	Sheet 15 of 51



2015.06.08 C338,C337,C339,C340,C363 change to depop

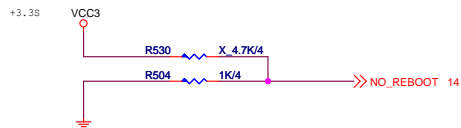


TOP Swap



Internal pull-down 20K is disabled after PLTRST#

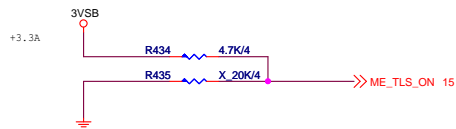
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

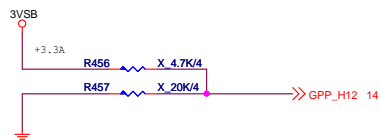
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

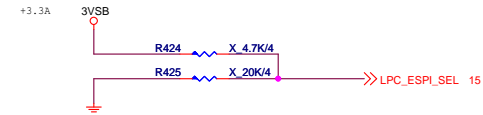
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

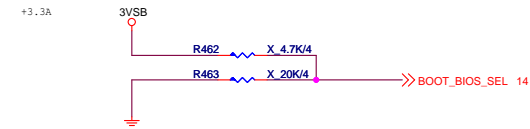
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

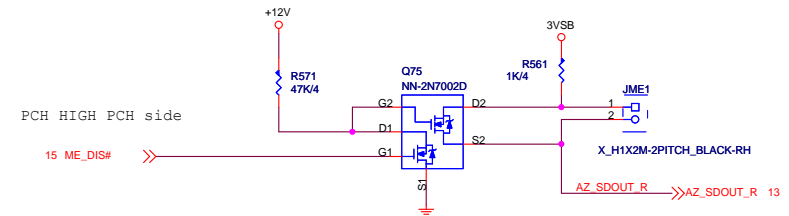
Boot BIOS



0 : SPI
1 : LPC

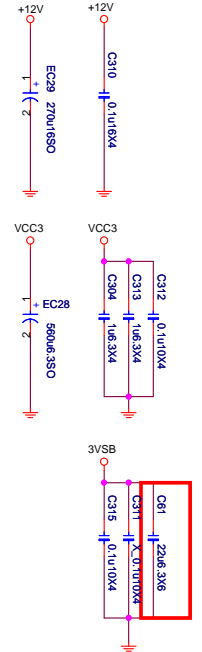
Internal pull-down 20K is disabled after PLTRST#

HDA_SDO




MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description PCH-Strap	Rev 10
Date: Friday, August 07, 2015	Sheet 18 of 51	

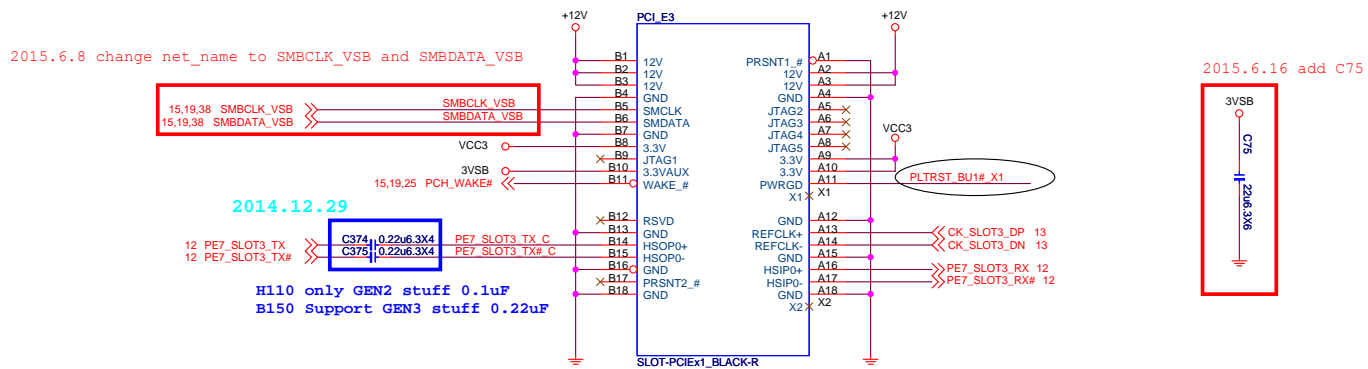
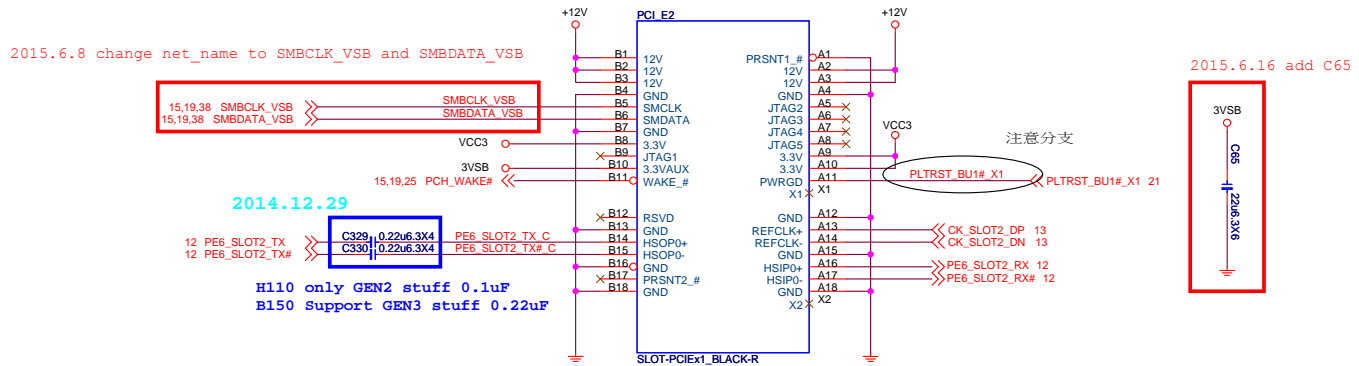
2015.6.8 change net_name to SMBCLK_VSB and SMBDATA_VSB



2015.6.16 add C61



			MICRO-STAR INT'L CO.,LTD		
			MS-7996		
Size	Document Description				Rev
Custom	PCI SLOT-CPU(X16)				10
Date:	Friday, August 07, 2015	Sheet	19	of	51

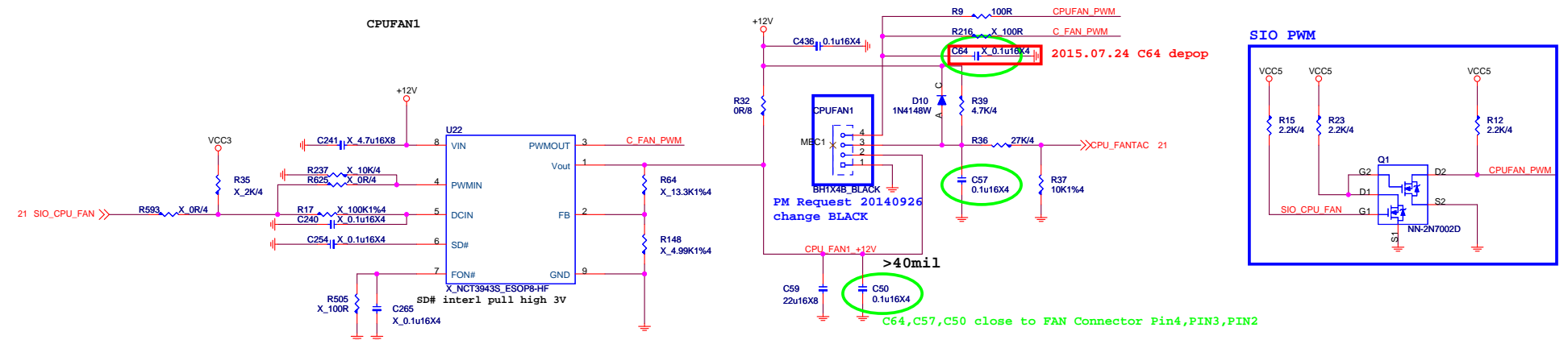


MICRO-STAR INT'L CO.,LTD

MS-7996

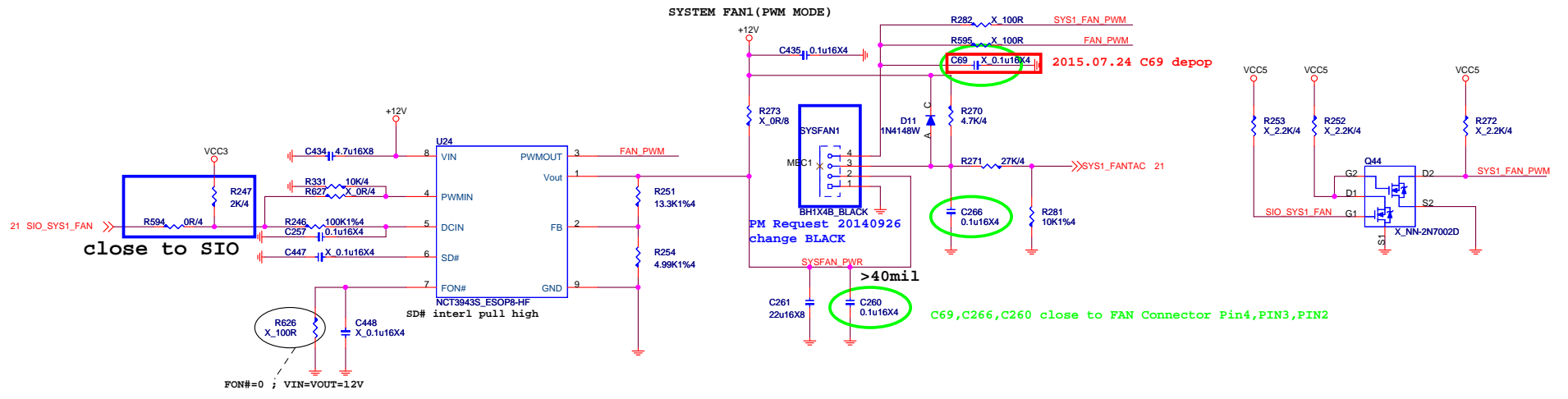
Size Custom	Document Description PCI SLOT-PCH(X1)	Rev 10
Date: Friday, August 07, 2015	Sheet 20 of 51	

Type G : 4 PIN CPU FAN FROM SIO



CPUFAN_PWR_OFF
 GPIO Control
 Deafult GPI
 If USE CUT POWER
 1.OPEN DRAIN LOW:SD# LOW Active , CPUFAN(PIN2)= 0V
 2.OPEN DRAIN : SD# Internal Pull high , CPUFAN(PIN2)=12V

Type H : 4 PIN SYS FAN FROM SIO



close to SIO

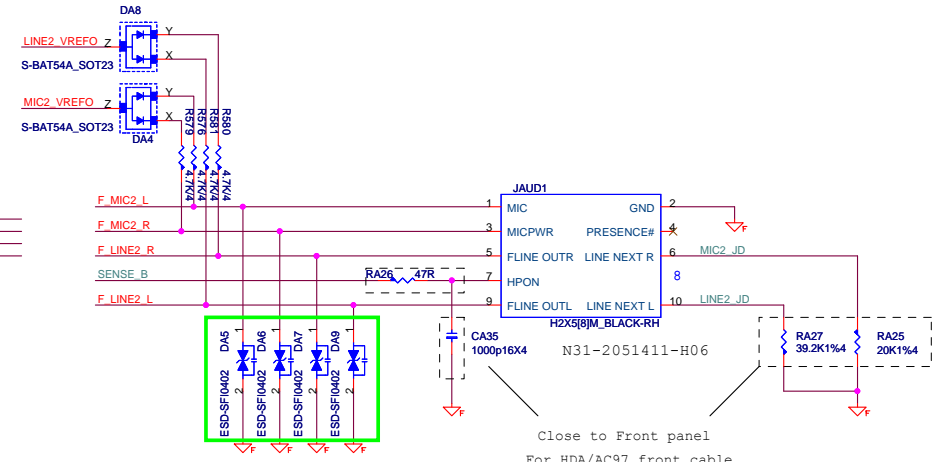
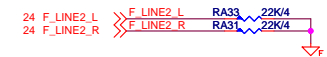
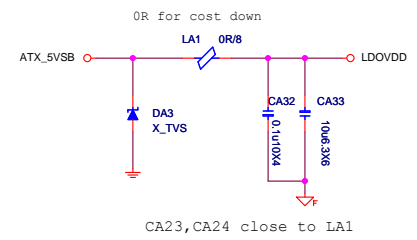
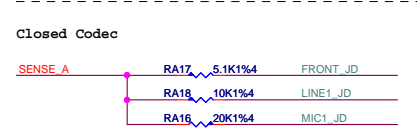
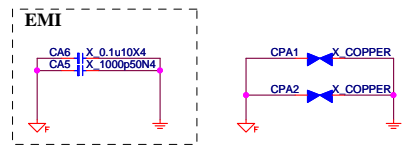
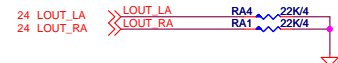
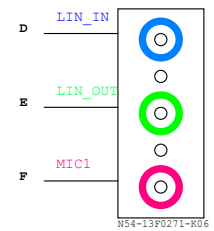
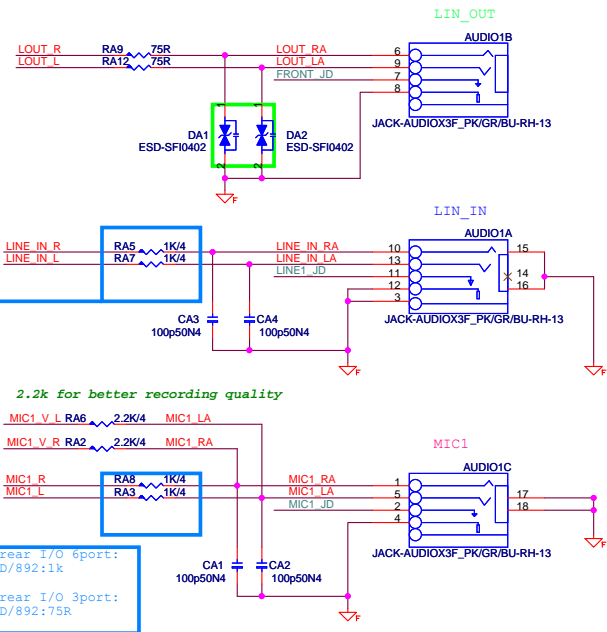
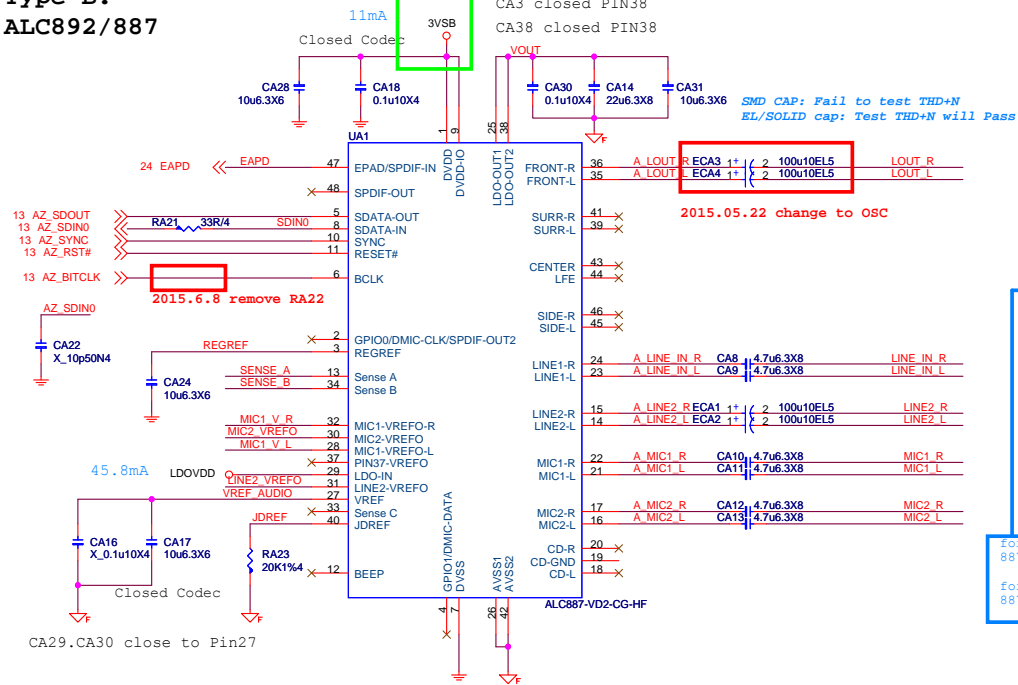
C69,C266,C260 close to FAN Connector Pin4,PIN3,PIN2

MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description FAN CONTROLLER	Rev 10
Date: Friday, August 07, 2015	Sheet 22	of 51

Type B:
ALC892/887

2014.09.15

CA4 closed PIN25
CA3 closed PIN38
CA38 closed PIN38

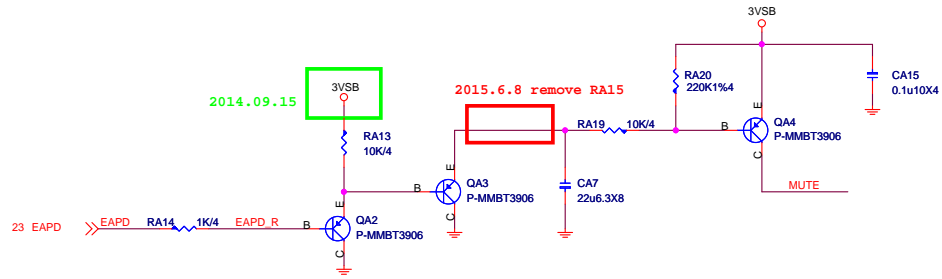


Varistor --> cap for cost down
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack

MSI		
MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description AUDIO - ALC892/887	Rev 10
Date: Friday, August 07, 2015	Sheet 23	of 51

Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



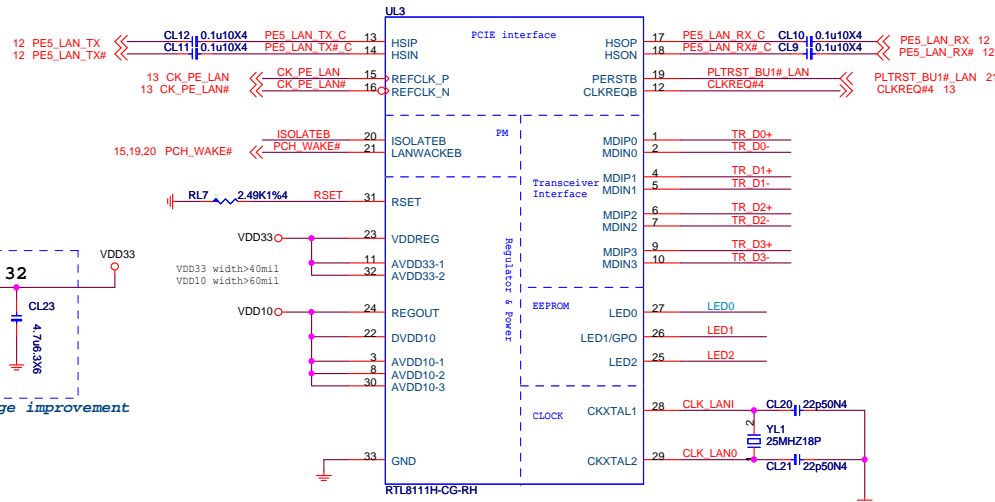
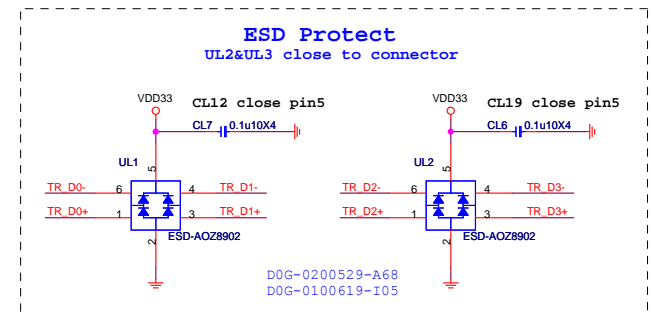
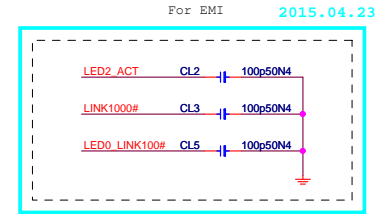
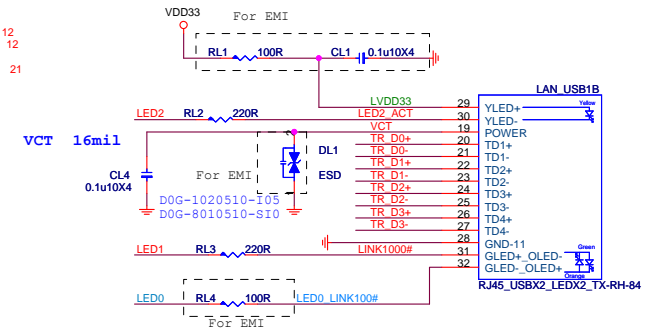
History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

LAN Connector



Pin33: 4 via from top layer to GND layer and make the via at the center of IC.

For surge improvement

For EMI 2015.04.23

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDFS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDFS	5.50	18.15



MICRO-STAR INT'L CO.,LTD

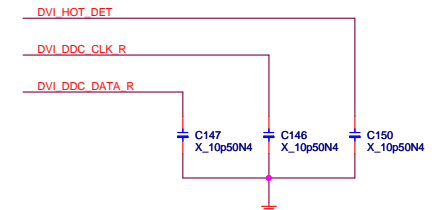
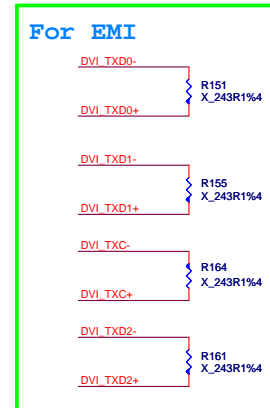
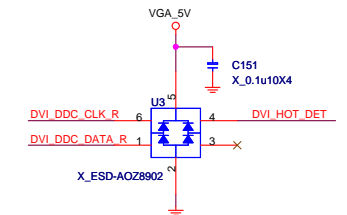
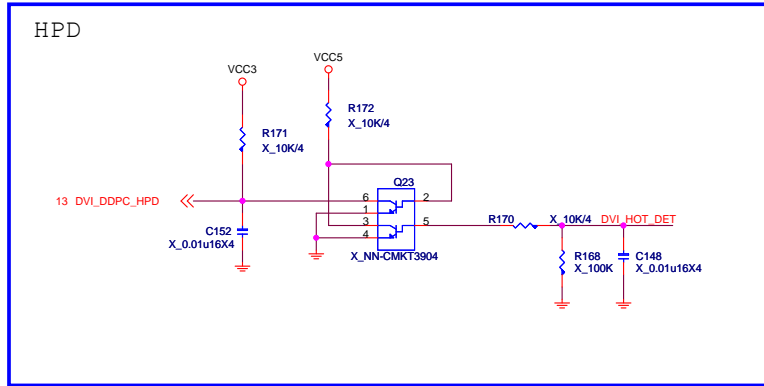
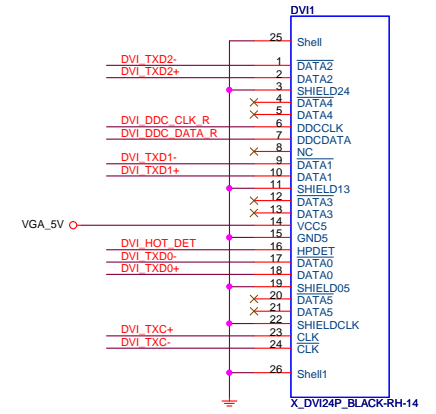
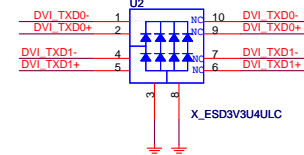
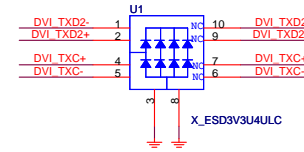
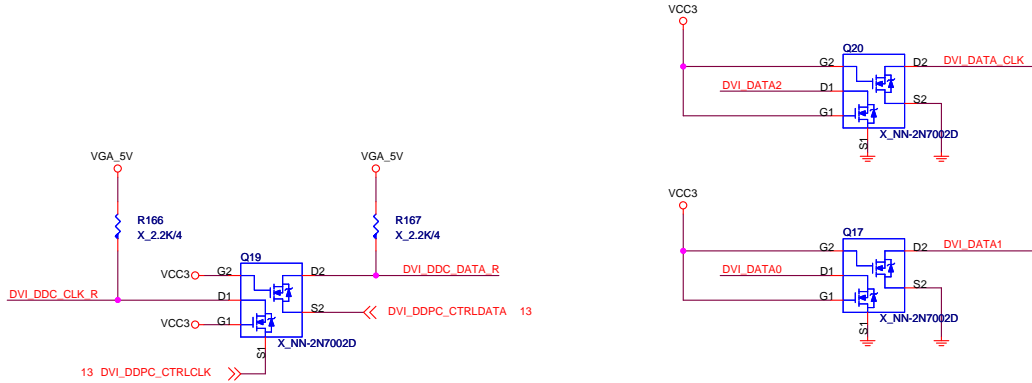
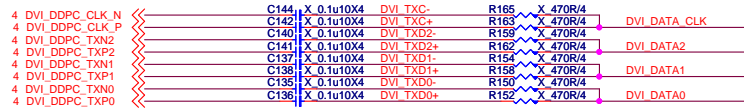
MS-7996

Size	Document Description	Rev
Custom	LAN - RTL8111H	10

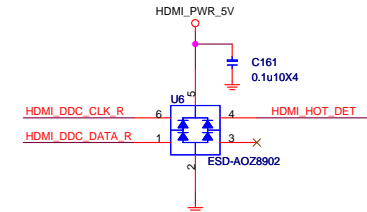
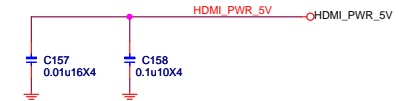
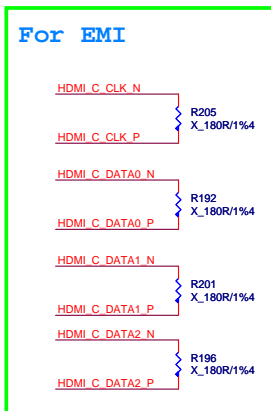
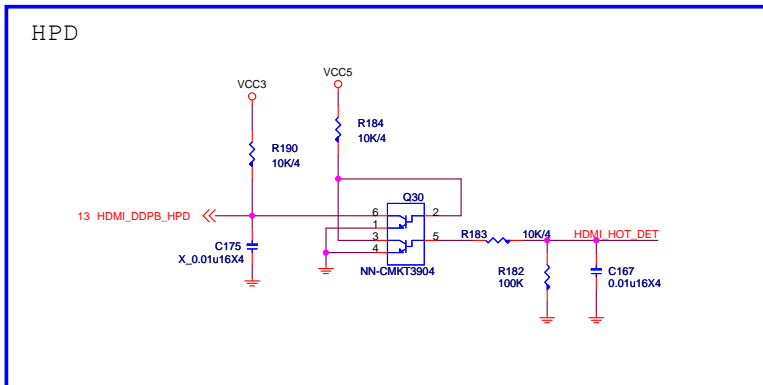
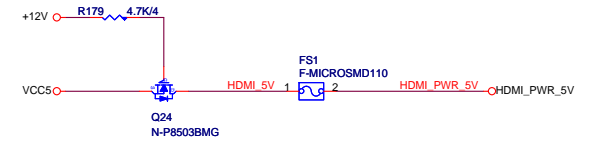
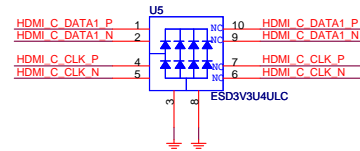
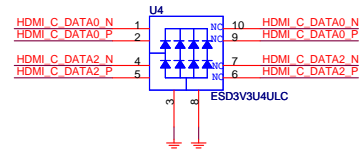
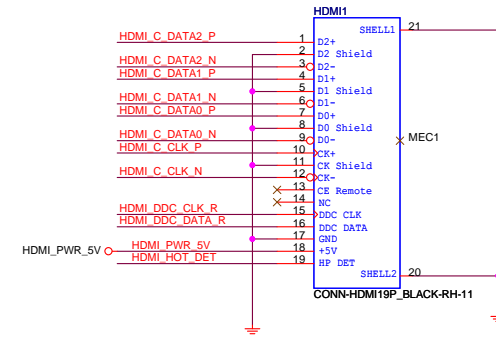
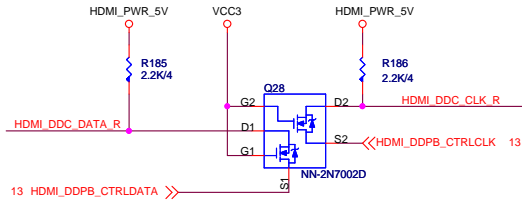
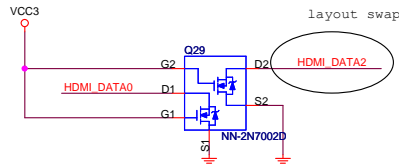
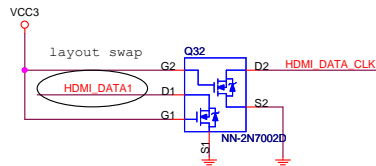
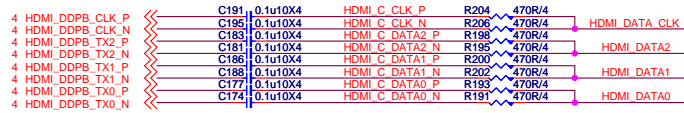
Date: Friday, August 07, 2015 | Sheet 25 of 51

DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



MICRO-STAR INT'L CO.,LTD

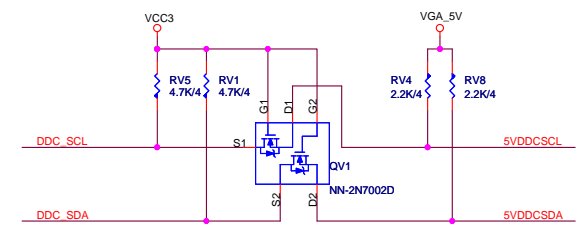
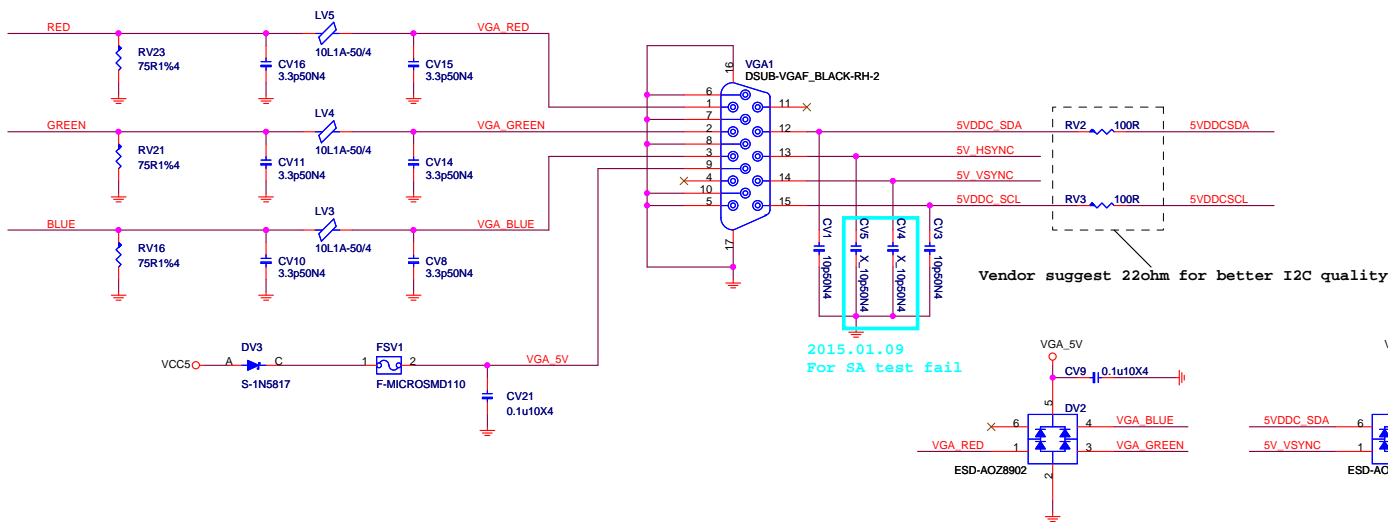
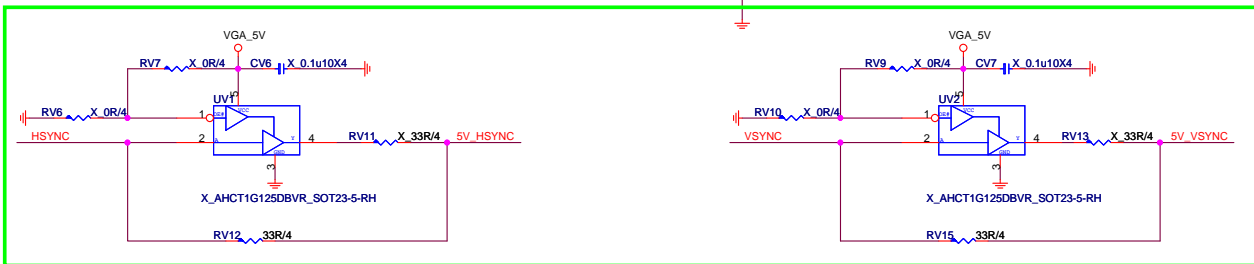
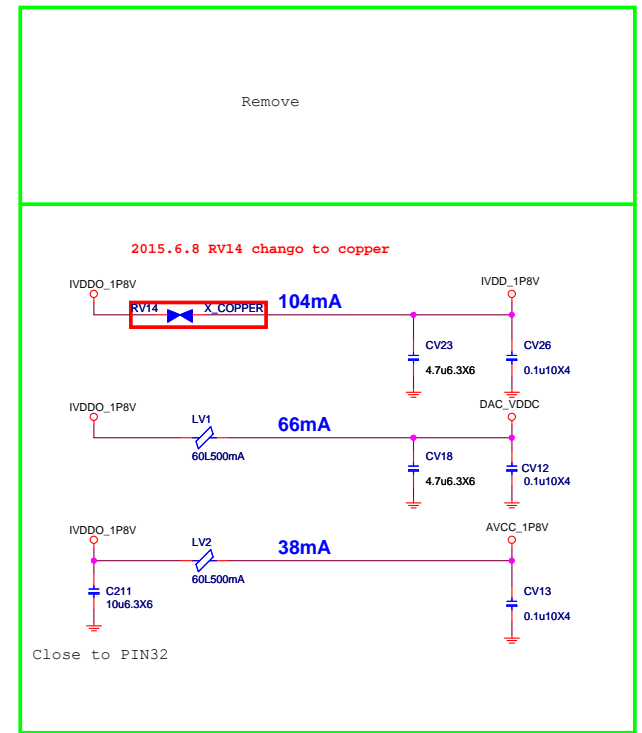
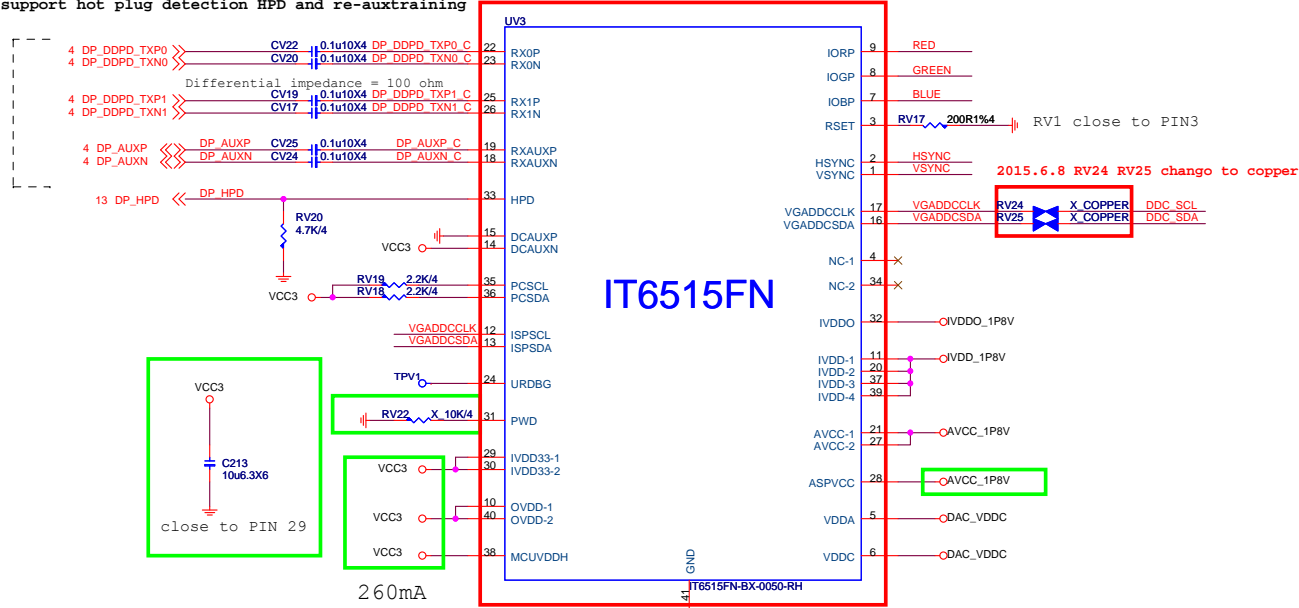
MS-7996

Size Custom	Document Description HDMI Connector	Rev 10
Date: Friday, August 07, 2015		Sheet 27 of 51

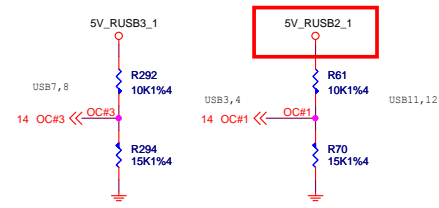
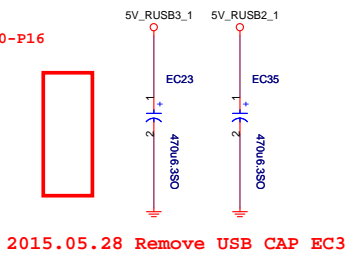
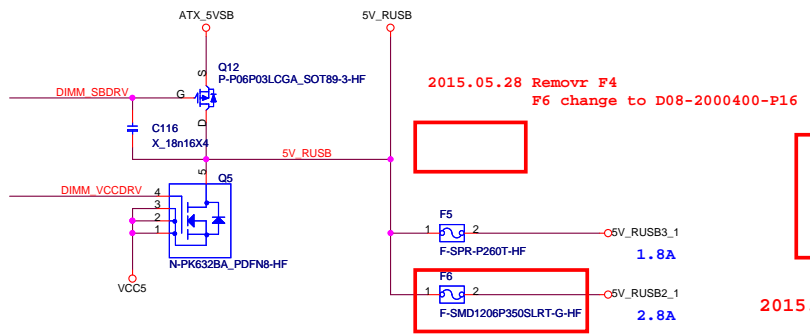
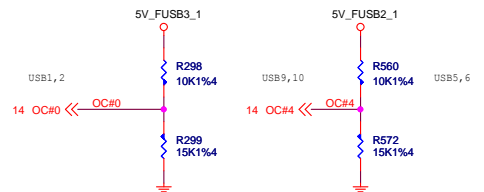
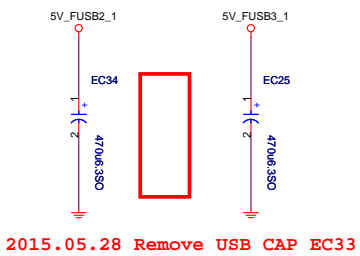
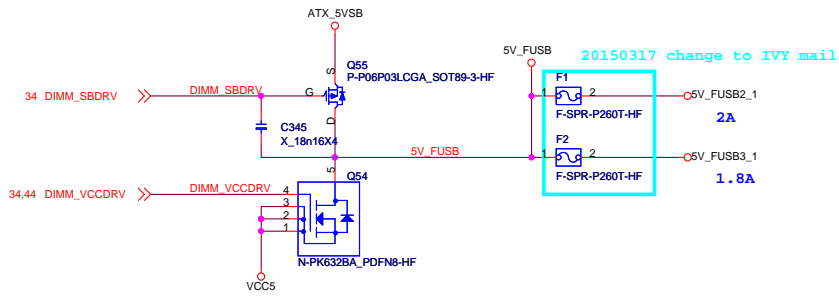
Note:

If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auxtraining

2015.05.22 UV3 change to B0B-6515F1C-II5

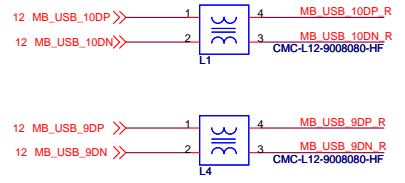


MSI		
MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description VGA - ITE6515	Rev 10
Date: Friday, August 07, 2015		Sheet 28 of 51

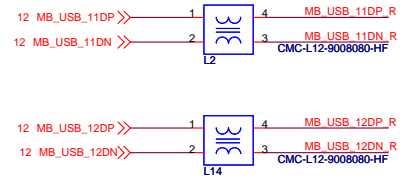


2015.05.28 change to 5V_RUSB2_1
2015.06.08 Remove R559, R575 and R605, R409

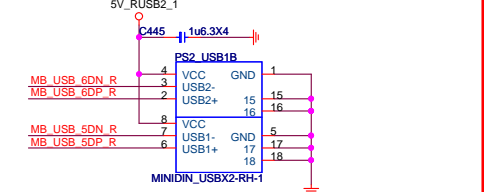
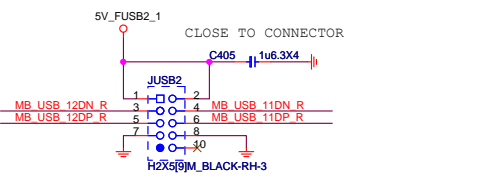
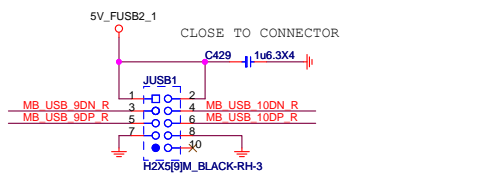
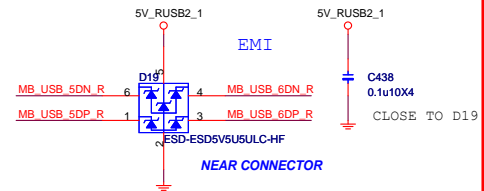
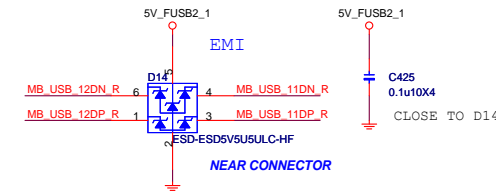
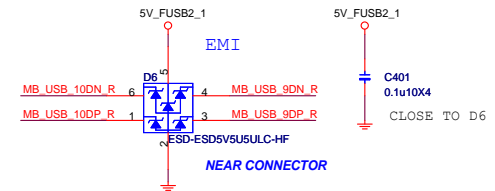
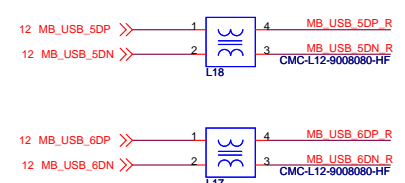
FRONT USB PORT 9,10



FRONT USB PORT 11,12

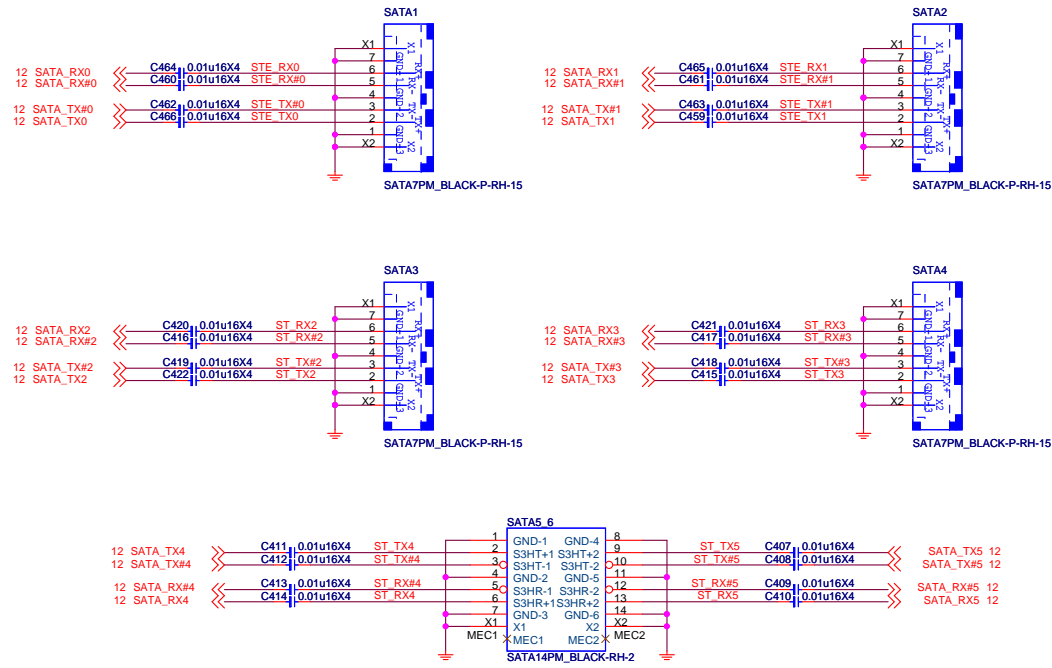


REAR USB PORT 5,6



2015.05.22 JUSB2 change to USB11,12
PS2_USB change to USB5,6

MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description USB2.0 Connector	Rev 10
Date: Friday, August 07, 2015	Sheet 29 of 51	



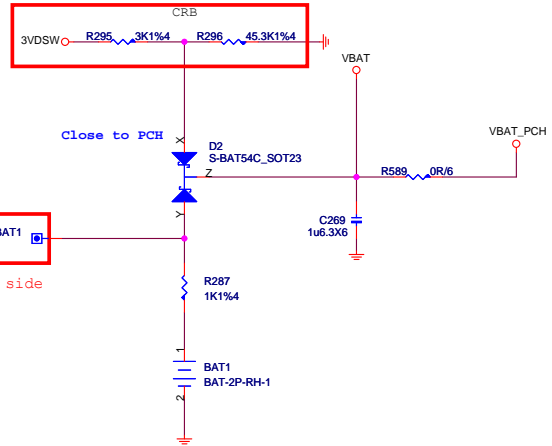
MICRO-STAR INT'L CO.,LTD

MS-7996

Size Custom	Document Description SATA connector	Rev 10
Date: Friday, August 07, 2015	Sheet 31 of 51	

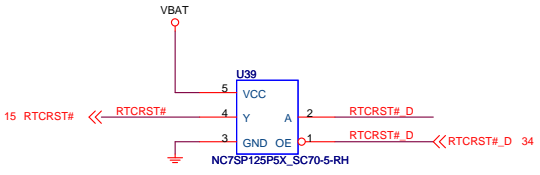
CUT_VBAT

2015.7.20 R295,R296 change to POP

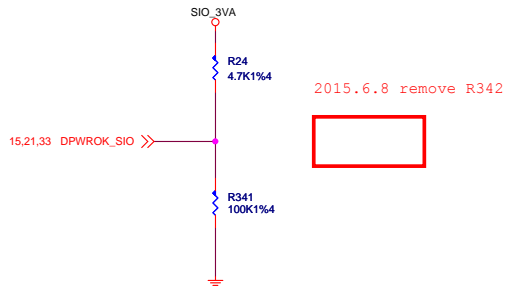
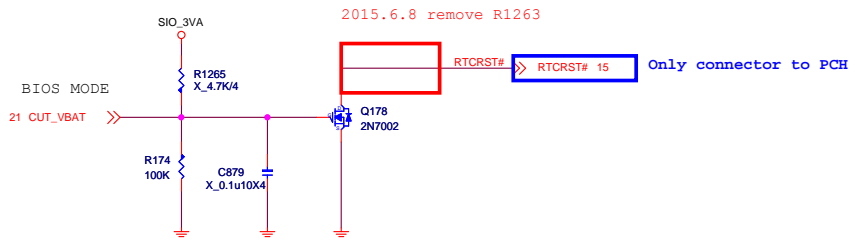
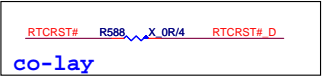
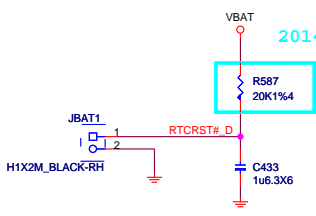


2015.6.1 add VBAT1 in bottom side

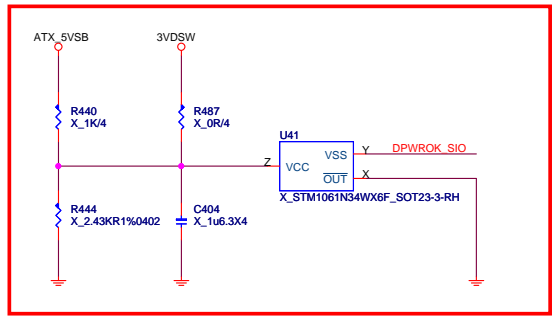
tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z



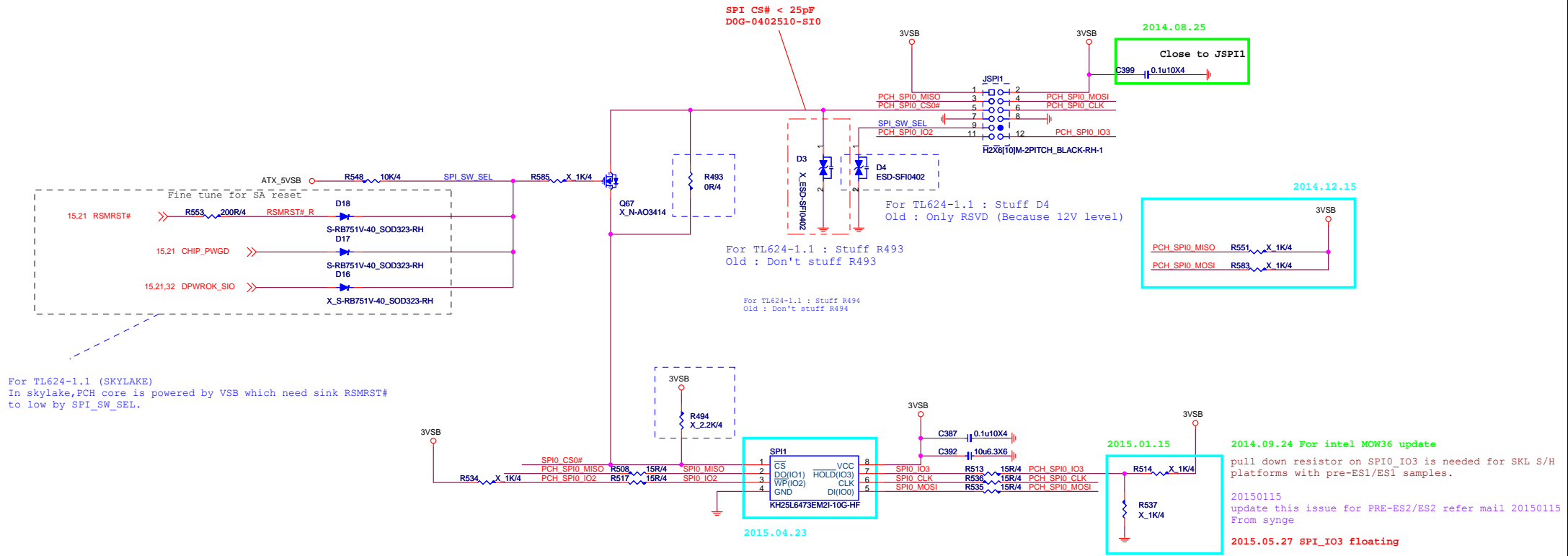
2014.12.29



2015.6.10 add circuit

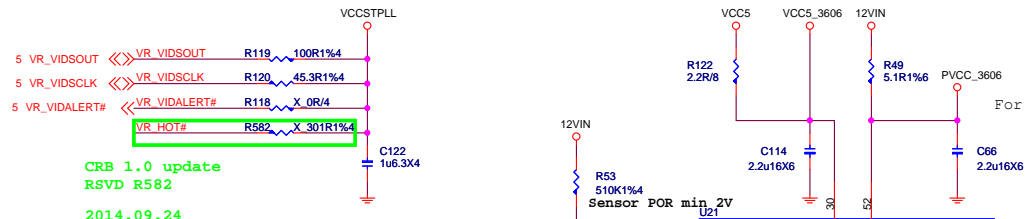


15 PCH_SPIO_MOSI << PCH_SPIO_MOSI
 15 PCH_SPIO_MISO << PCH_SPIO_MISO
 15 PCH_SPIO_CLK << PCH_SPIO_CLK
 15 PCH_SPIO_CS0# << PCH_SPIO_CS0#
 15 PCH_SPIO_IO2 << PCH_SPIO_IO2
 15 PCH_SPIO_IO3 << PCH_SPIO_IO3



* if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002
 * if you support Standby power in S5 Status(Ex; PCH is B75 Chipset), component Q14.G Pull-high to ATX_5VSB, Q14 must select "Vth" under 1V (Component Suggestion as below)
 D03-0341409-A68 / D03-0230019-A30

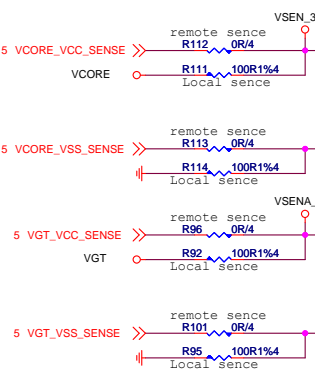
	MICRO-STAR INT'L CO.,LTD	
	MS-7996	
Size Custom	Document Description BIOS ROM	Rev 10
Date: Friday, August 07, 2015		Sheet 33 of 51



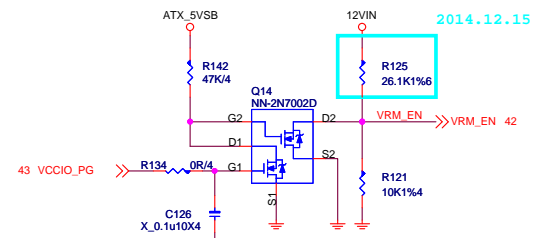
CRB 1.0 update
RSVD R582
2014.09.24

2015.7.20 R90 change to 36.5K

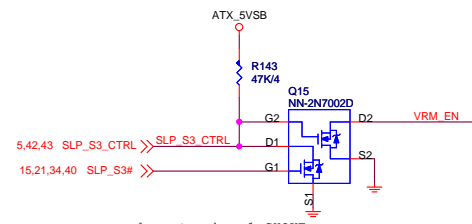
2015.08.04 change to C11-4757322-S02

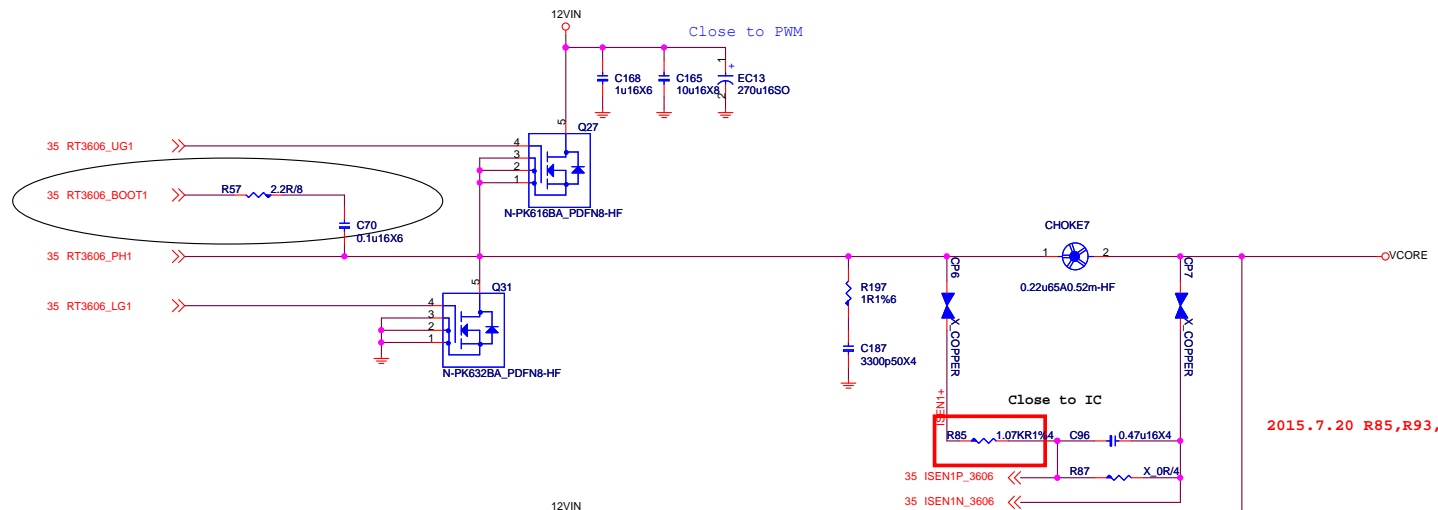


SLP_S3# assertion to IMVP VRM_EN deassertion max:1us



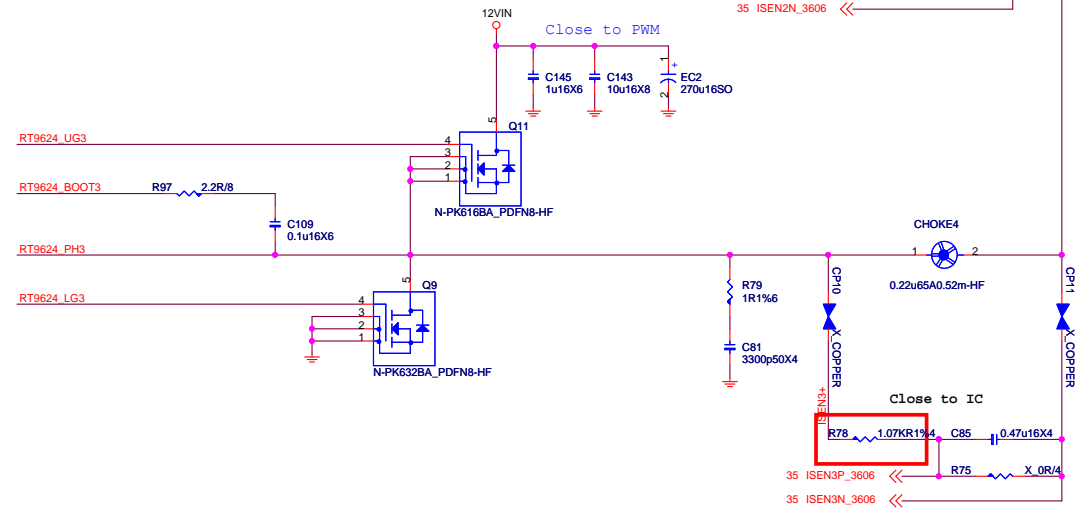
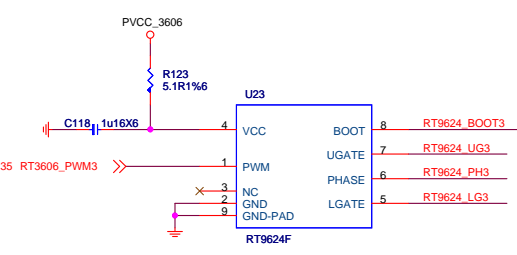
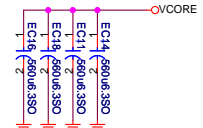
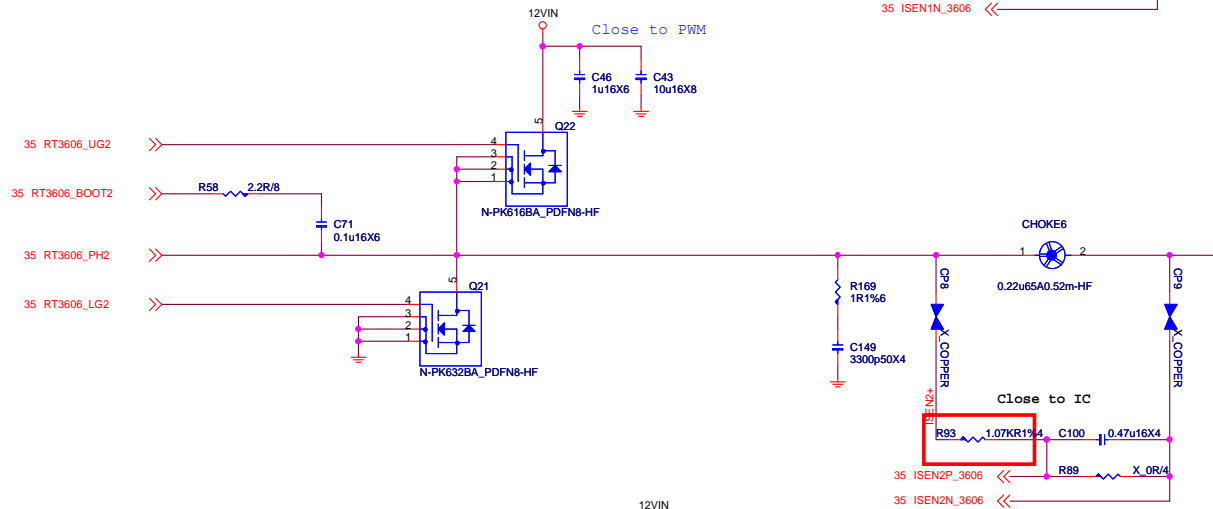
2014.12.15



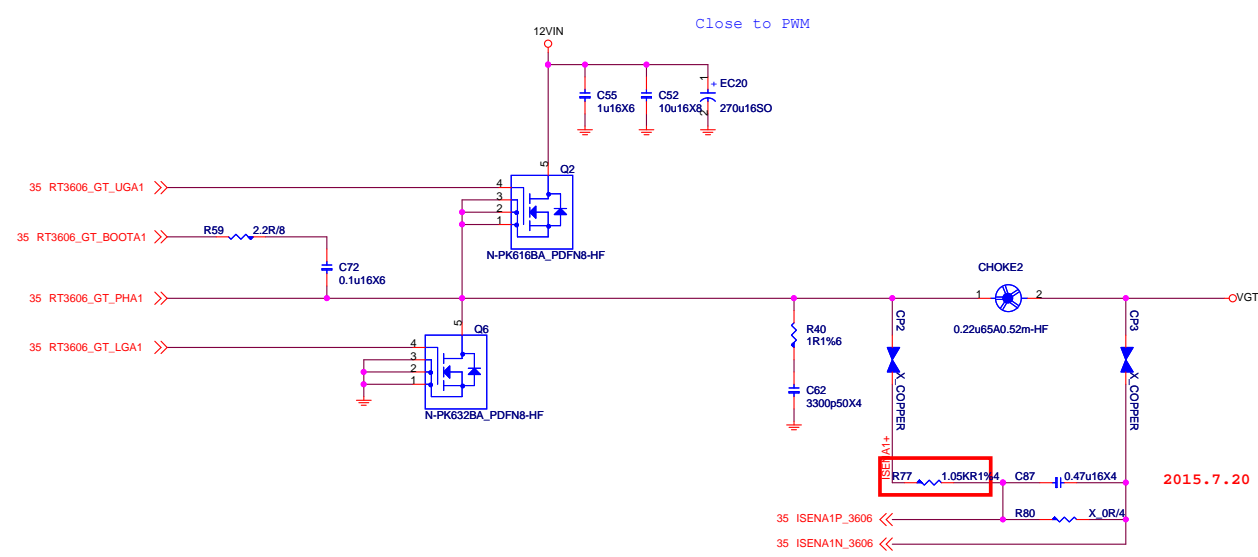
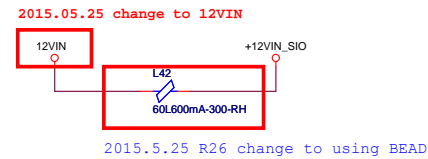
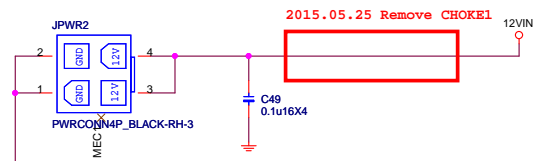


ICCMAX: 79A
 LL: 2.1m ohm

2015.7.20 R85,R93,R78 change to 1.07K

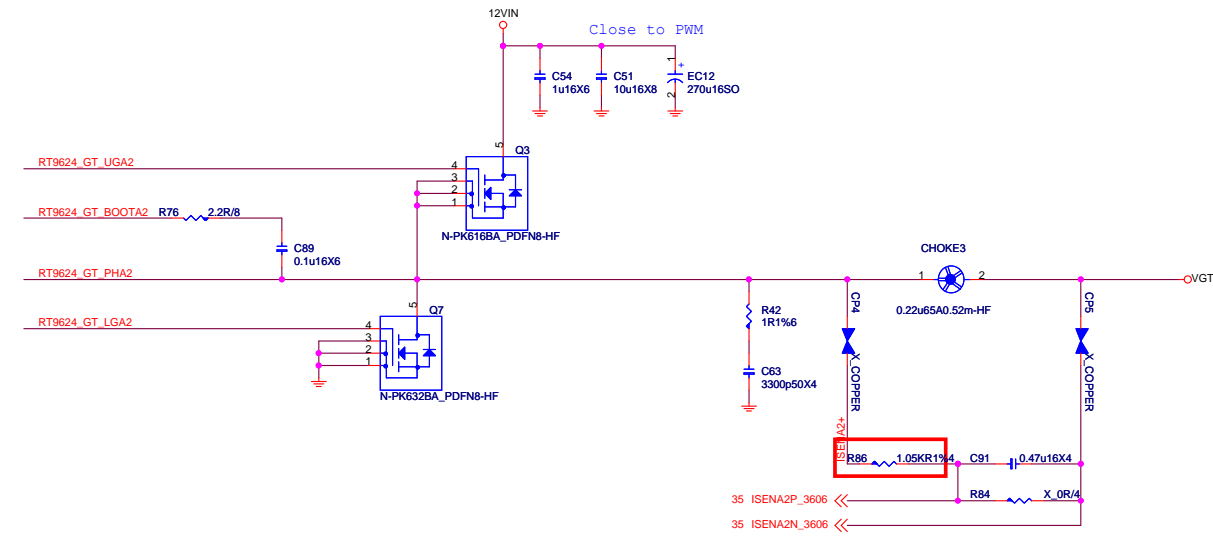
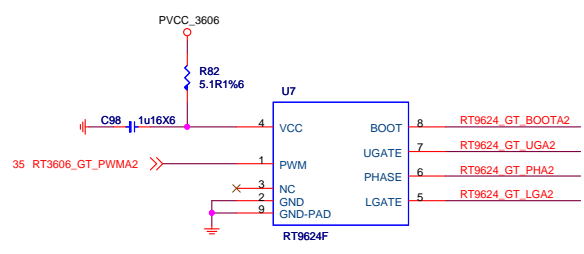
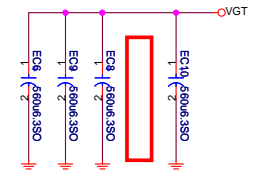


MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description VCORE(P-PAK) PHASE-3	Rev 10
Date: Friday, August 07, 2015	Sheet 36	of 51



ICCMAX:51A
LL:3.1m ohm

2015.7.20 R77,R86 change to 1.05K



MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description VGTT(P-PAK) PHASE1-2	Rev 10
Date: Friday, August 07, 2015	Sheet 37	of 51

DDR4_1.2V 2.8A+ 4.75A+0.375A=7.925

2.8A FOR CPU
4.8A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

OCF = 7.925A * 1.5 = 11.8875A
Current limit = 95.3K(R1054) * 5uA / 10 / 4mohm = 11.91A

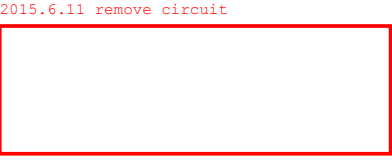
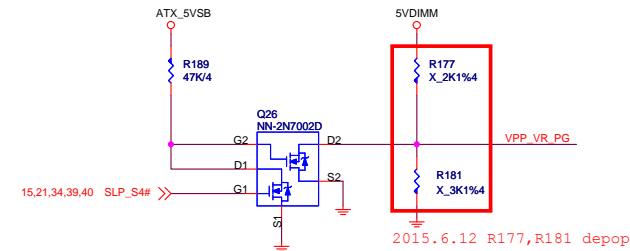
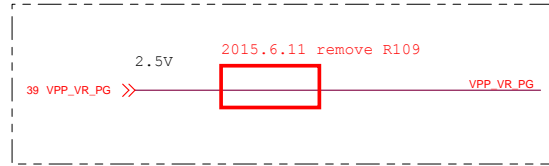
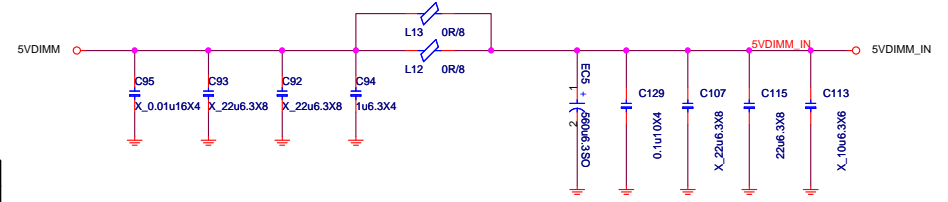
2015.05.22 change to DDR4

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 9.357 * 0.44$$

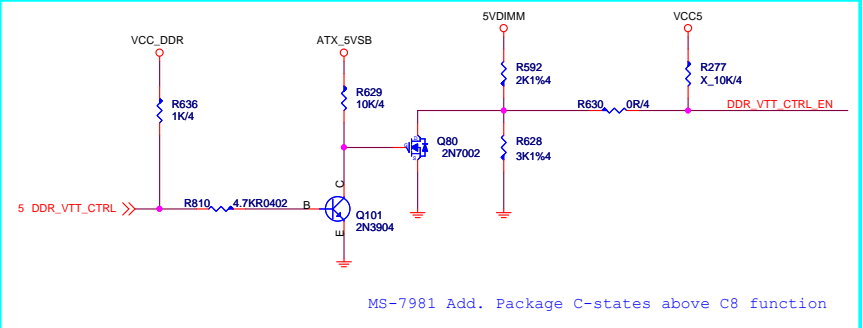
$$= 4.154A$$

VID	Reference Voltage (V)
H	0.675
L	0.75

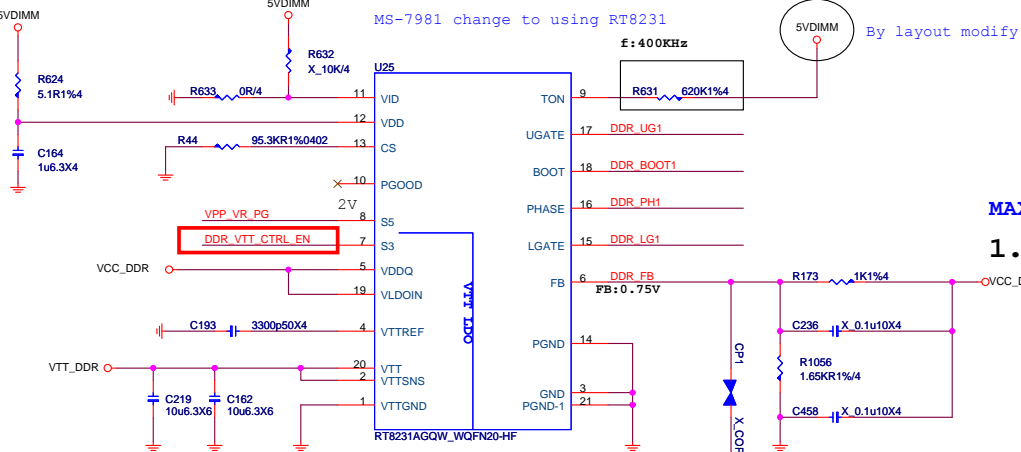


SLP_S4# de-assertion to VDDQ ramp down start

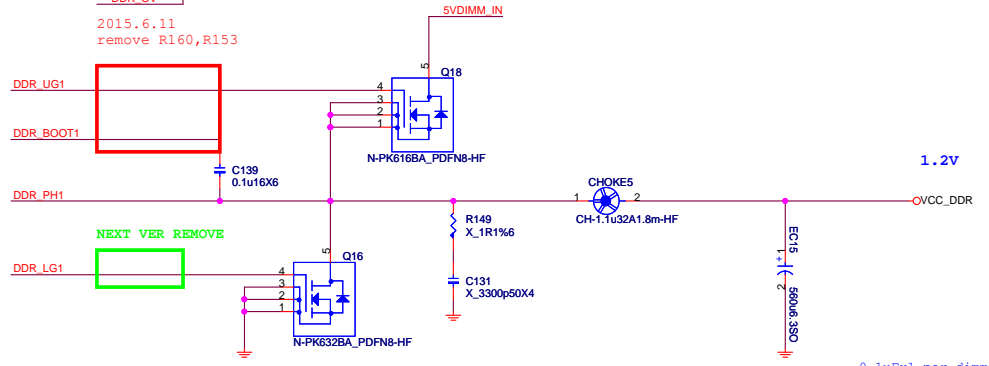
VPP ramp down after VDDQ ramp down



MS-7981 Add. Package C-states above C8 function

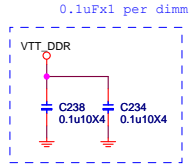
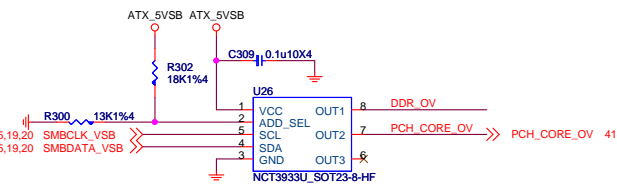


MAX: 7.925A
1.2V



UPI VOLTAGE CONSOLE

0x26 : RH=18K, RL=13K



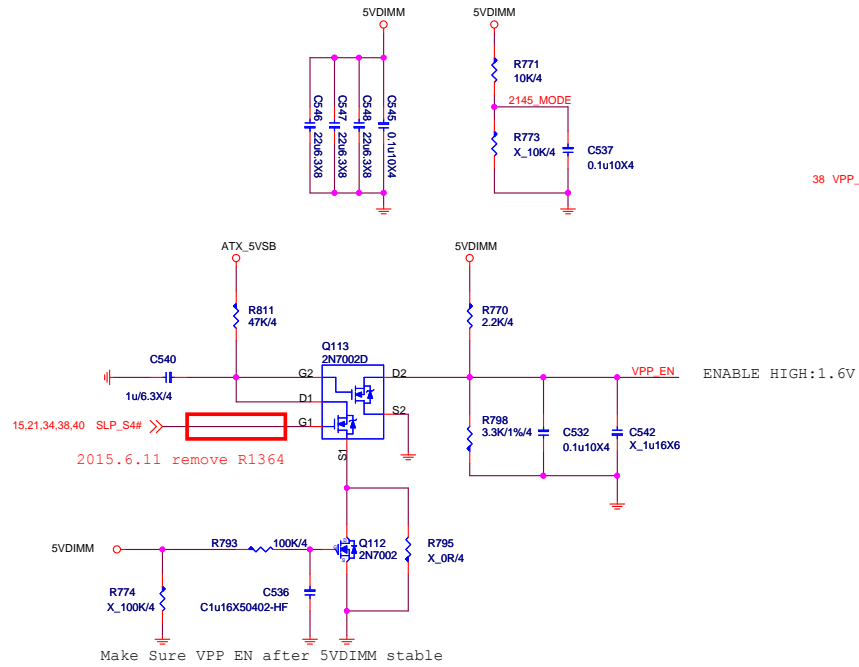
MICRO-STAR INT'L CO.,LTD

MS-7996

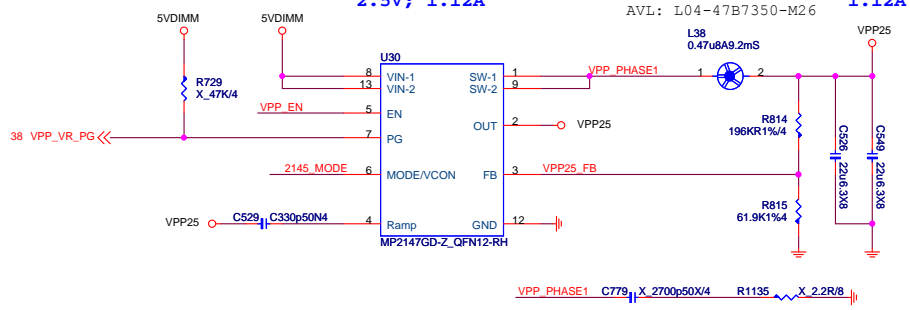
Size Custom Document Description **DDR-RT8231** Rev 10

Date: Friday, August 07, 2015 | Sheet 38 of 51

2DIMM :1.12A FOR DDR VPP2.5V



VPP25 Power
2.5V; 1.12A

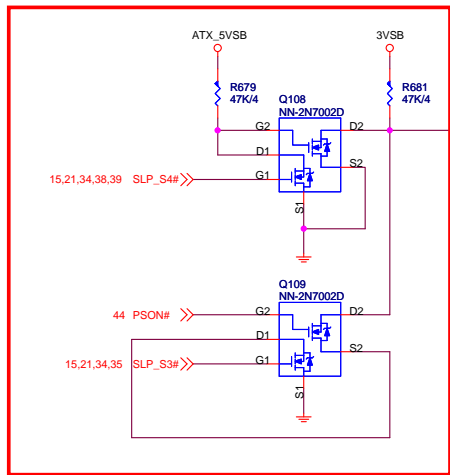


MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description DDR-MP2147-VPP25	Rev 10
Date: Friday, August 07, 2015	Sheet 39	of 51

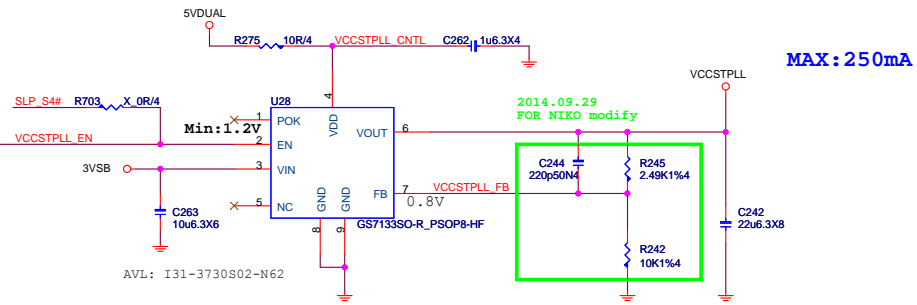
VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge



2015.05.25 add circuit



MAX: 250mA

2014.09.29
FOR NIKO modify

VCCIO ramped and stable before
beginning of VCCOPC/VCCEPIO ramp
VCCST/PLL stable 1ms before PROC_PWRGD

PCH 1VSB

1.0V; 7.858A

OCp = 11.787A

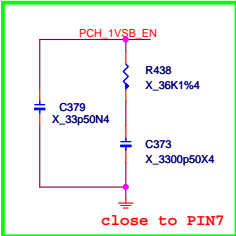
Rocset = $1.5 * I_{max} * R_{dson}(low) / I_{ocset}$
 = $1.5 * 7.858 * 5m\Omega / 10\mu A$
 = 5.8935K

RocS: 5.9K, OCP:
 D03-4C05N03-005 : 11.8A
 D03-632BA0C-N03 : 12.82A
 use UBIQ MOS need Check

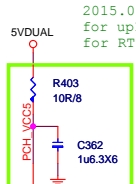
Rdson(low) 4.5V
 D03-4C05N03-005 : 5 mohm
 D03-632BA0C-N03 : 4.6mohm
 D03-3056M00-U47 : 6.2mohm

2015.04.23 change to UP1540

2014.08.22 close to U34

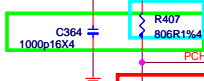


2015.01.22
 for up1540:stuff R438->36K,
 C379->NC, C373->3.3nF
 for RT8125:R438.C379.C373->NC



2015.01.22
 for up1540:R403->2.2R, C362->1uF
 for RT8125:R403->10R, C362->1uF

2014.12.25
 for up1540:C364&R407 ->NC



2015.08.06
 R407 -> 806R

2015.05.25
 For up1540:C365 is OCP set min:5Kohm
 stuff 5.9K OCP SET:11.787A
 RT8125C stuff C1000P C11-1022032-W08



2014.12.25
 for up1540:R623 ->NC

38 PCH_CORE_OV << PCH_CORE_OV
 to sink/source over voltage IC.
 pin10 sink/source current capability can't over 1mA
 So max voltage can't over 1.8V.
 from NCT3933

2014.12.25
 for up1540:stuff R622->0R

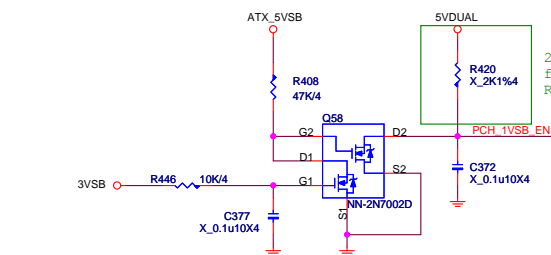


$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

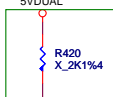
$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

$$= 1.004V$$



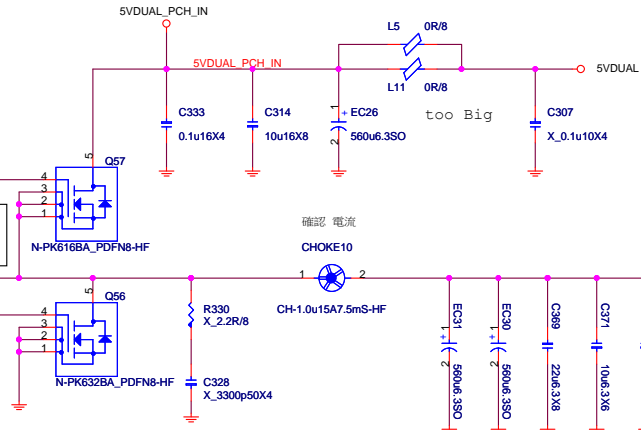
2014.12.25
 for up1540:R420 ->NC
 RT8125C:R420 ->NC



$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$



MAX:10.664A

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.8335\mu H (K = 30\%)$$

PLACE UNDER THE PCH

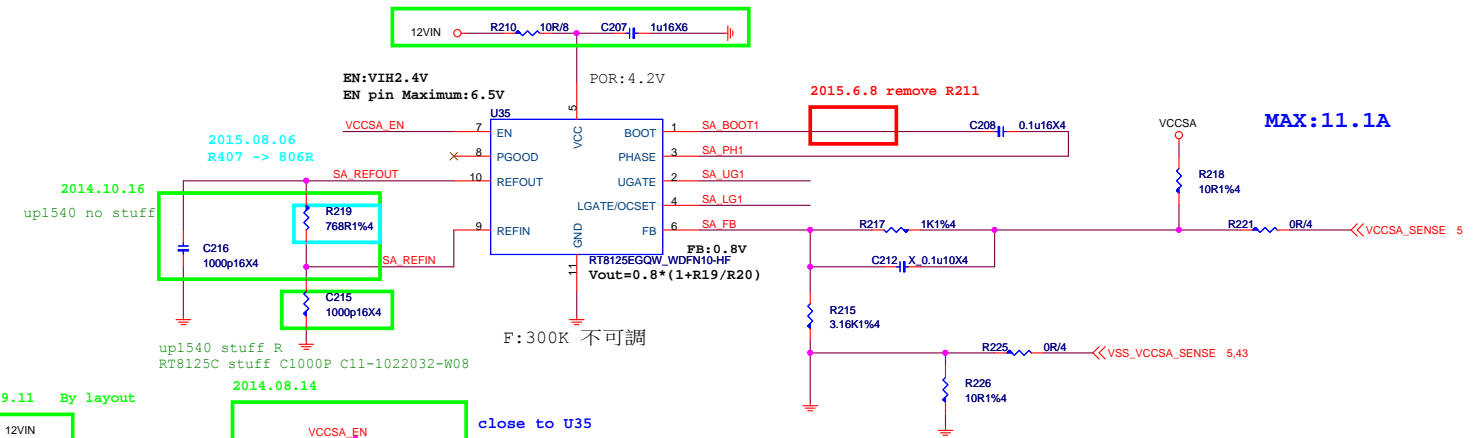
SA Power:1.05V,11.1A

OCP = 11.1A * 1.4 = 15.54A
 Rocs(R15) = OCP * Rds(on Low side) 3.4mohm / 10uA
 = 15.54 * (3.4)mohm / 10uA
 = 5.2836Kohm

Rocs: 5.2836K, OCP:
 D03-4C05N03-005 : 3.4mohm
 D03-632BA0C-N03 : 3.3mohm
 D03-3056M00-U47 : 4.2mohm

Rds(on Low) 10V
 D03-4C05N03-005 : 3.4mohm
 D03-632BA0C-N03 : 3.3mohm
 D03-3056M00-U47 : 4.2mohm

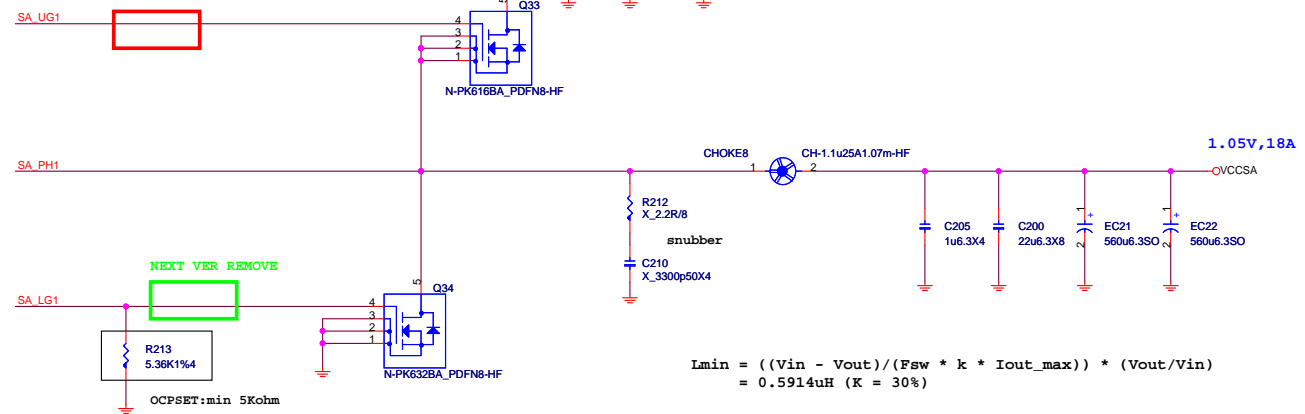
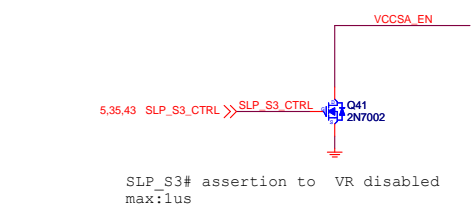
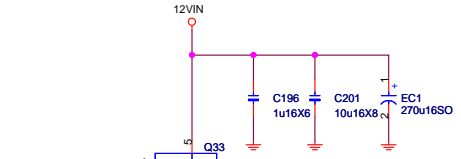
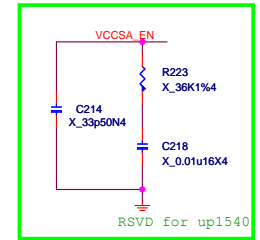
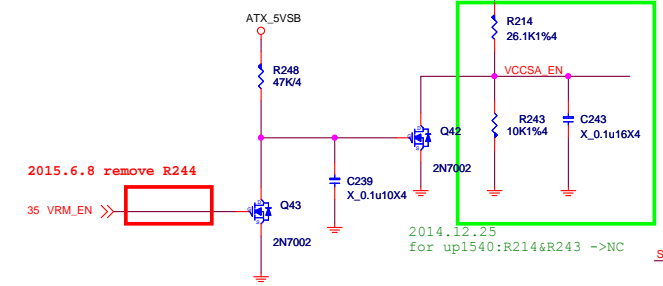
2015.01.22
 for up1540:R96->2.2R,C84->1uF
 for RT8125:R96->10R,C84->1uF



$$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$

$$= 11.1 * 0.2825$$

$$= 3.13575A$$



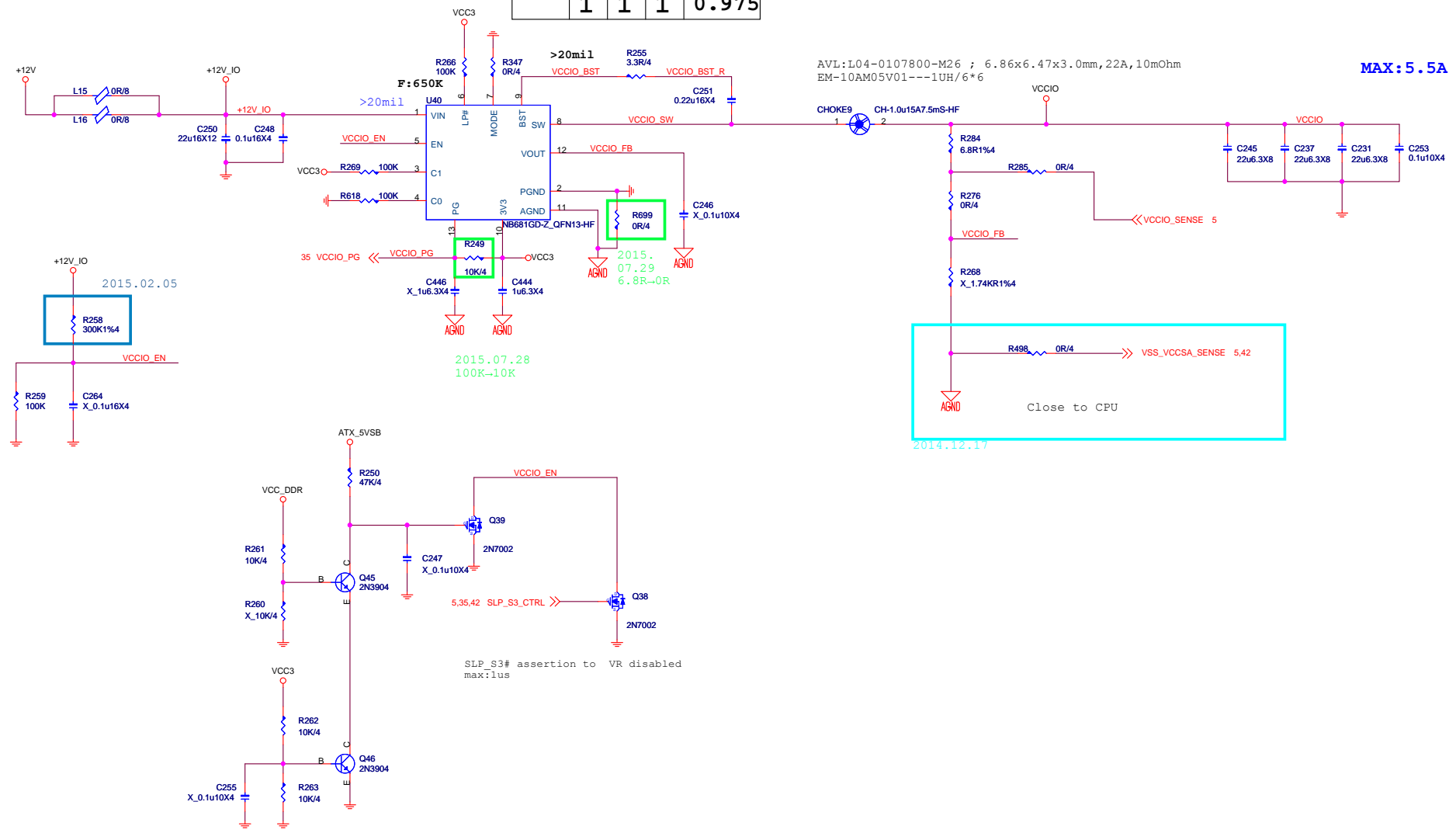
$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.5914uH (K = 30\%)$$

VCCIO

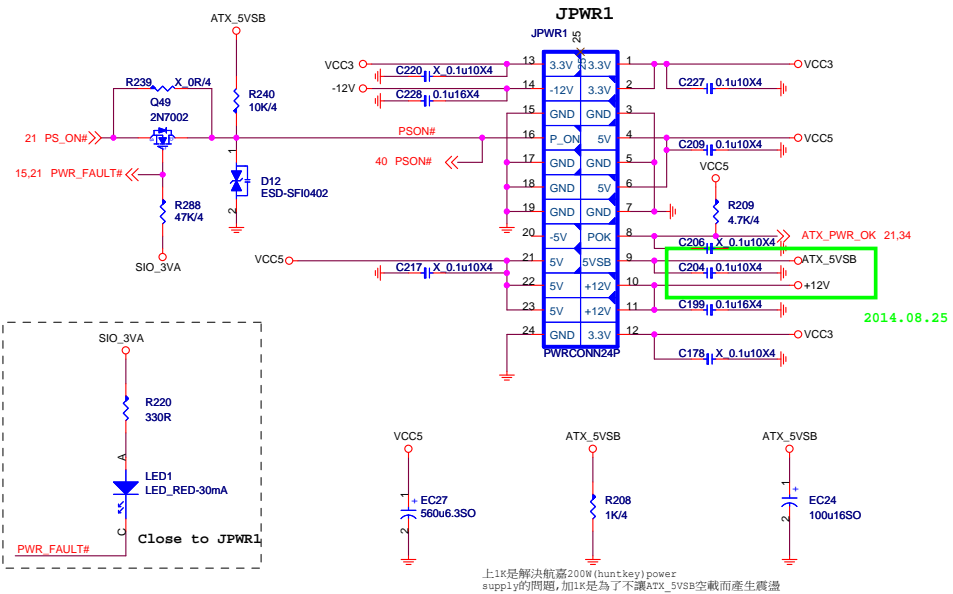
0.95V; 5.5A IMAX 6A
ILIMIT=8.5~9A

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

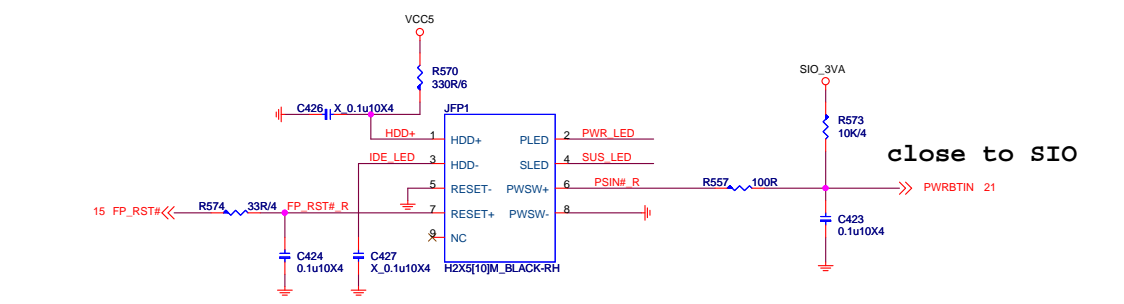


MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description VCCIO - POWER NB671	Rev 10
Date: Friday, August 07, 2015	Sheet 43 of 51	

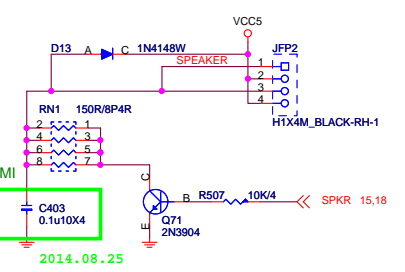
ATX POWER CONNECTOR



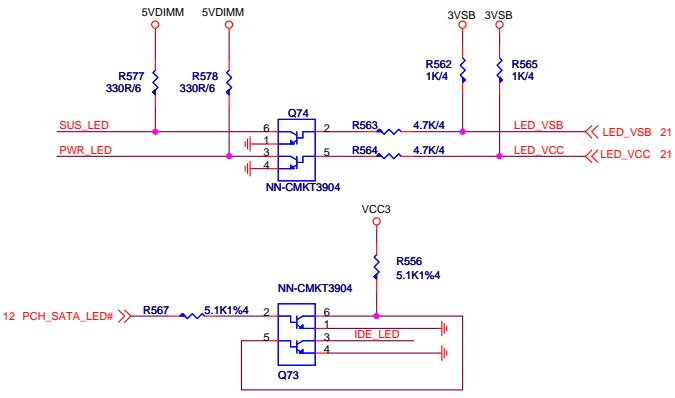
FRONT PANNEL



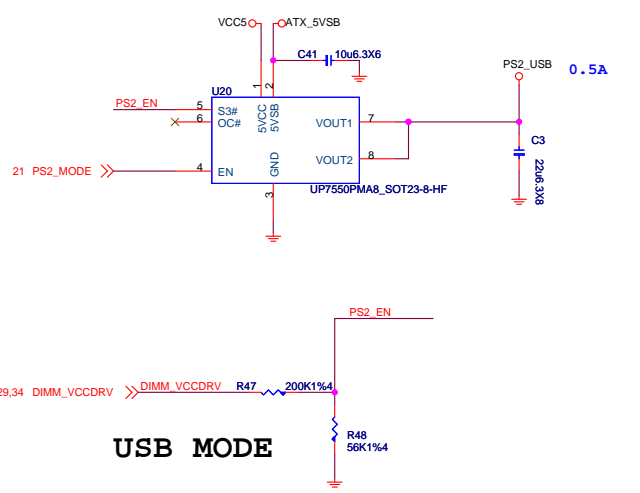
Speaker Pin Header



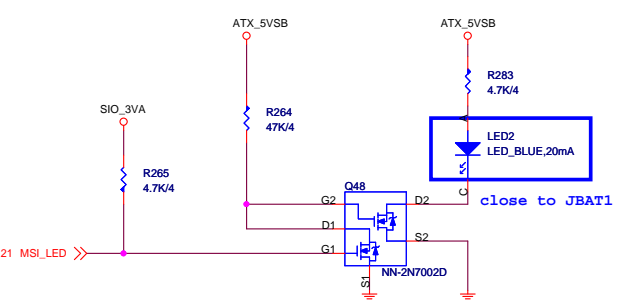
LED (for NV5533)



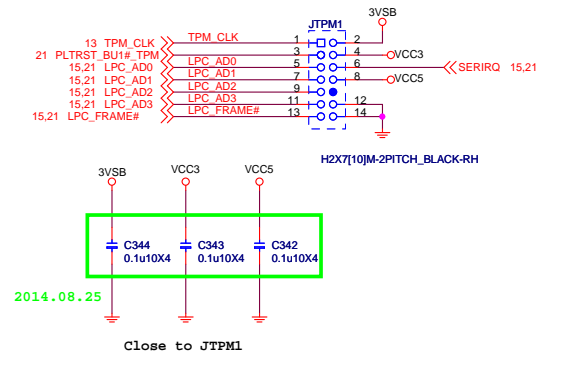
PS2 POWER



MSI LED

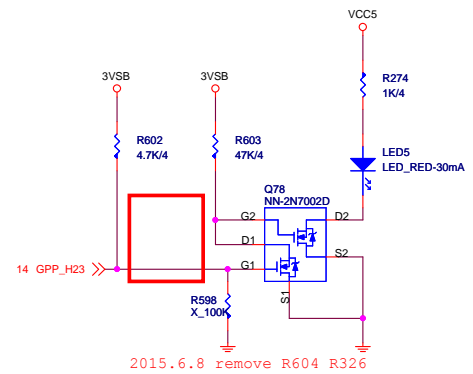
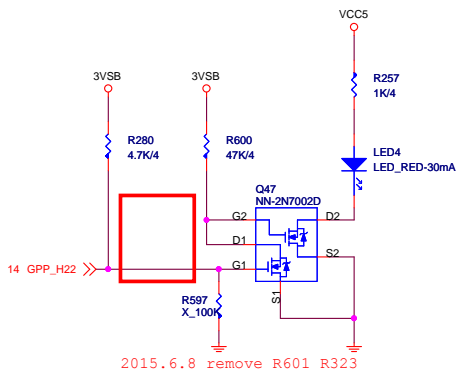
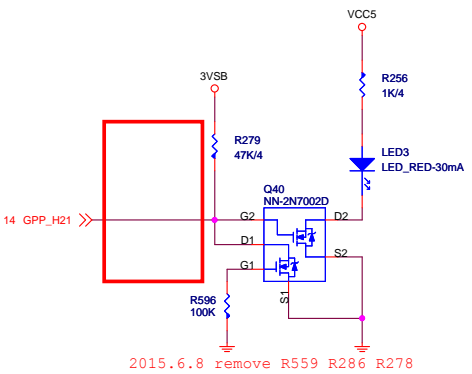


TPM



MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description ATX F_Panel/TPM/MSI_LED	Rev 10
Date: Friday, August 07, 2015 Sheet 44 of 51		

DEBUG LED

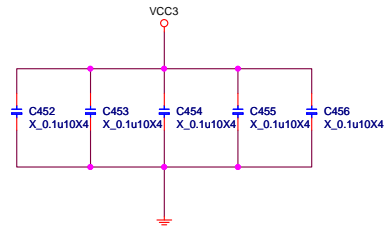
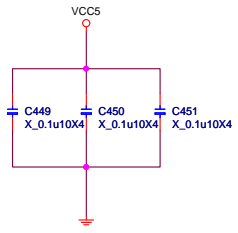



GPIO LED	GPP_H21	GPP_H21	GPP_H21
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

關機斷電狀態下，3個LED先維持default全暗，開機通電後：

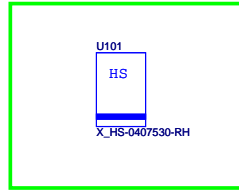
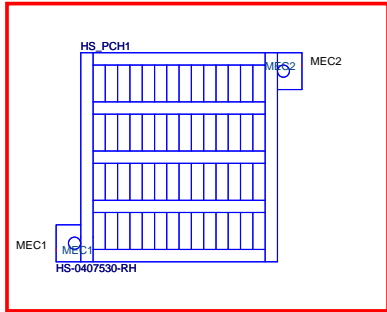
1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

EMI CAP

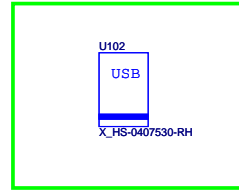


	MICRO-STAR INT'L CO.,LTD	
	MS-7996	
	Size Custom	Document Description EMI
Date: Friday, August 07, 2015	Sheet 46 of 51	Rev 10

2015.06.01 change to using E31-0407530-K08



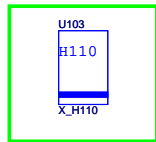
2015.08.03
colay Heatsink for H110



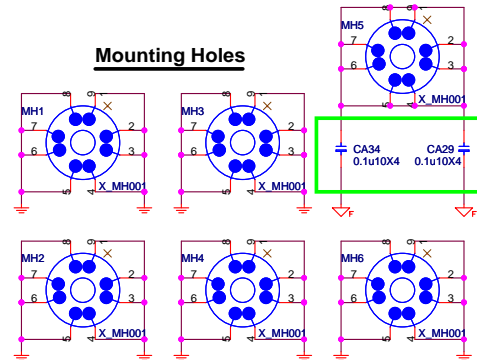
2015.08.03
USB2.0 Connector colay for H110

- VCC_DDR
- VTT_DDR
- 5VDIMM
- 3VSB
- VBAT
- 3VDSW
- PCH_1VSB
- VCORE
- VGT
- VCCSA
- VCCSTPLL
- VCCIO

2015.08.03
PCH H110 colay



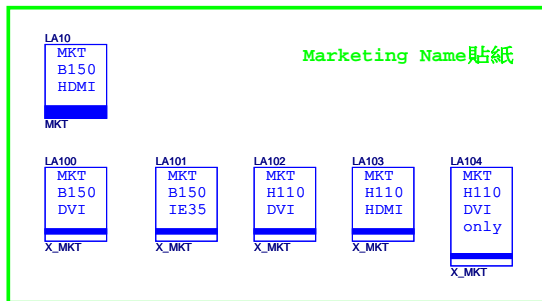
Mounting Holes



20150423 PM Request cost down



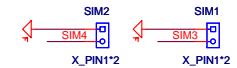
Marketing Name貼紙



Optical Fiducial Marks-120



Simulation



7996_11

- 2015/08/04 PK0-0799611-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)
- 2015/08/04 PK0-0799611-E48, 競華, 27, 寶安恩斯邁廠 (MSIS)
- 2015/08/04 PK0-0799611-G37, 精成, 23, 寶安恩斯邁廠 (MSIS)
- 2015/08/04 PK0-0799611-G37, 精成, 28, 寶安恩斯邁廠 (MSIS)

MICRO-STAR INT'L CO.,LTD		
MS-7996		
Size Custom	Document Description Manual Parts	Rev 10
Date: Friday, August 07, 2015		Sheet 47 of 51