A Low-Cost Cooperative Engagement Capability Array Antenna

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As Technical Direction Agent for the Cooperative Engagement Capability (CEC), the Air Defense Systems Department has developed a low-cost planar antenna (LCPA) concept that provides for a major reduction in acquisition and life-cycle costs over the current CEC array antenna. The new design concept also provides enhanced shipboard integration flexibility and resolves DDG 51 installation challenges associated with the preexisting CEC antenna. The concept is a four-face planar array system that uses low-cost commercial-based array techniques. Several transmit and receive modules and a small array section have been designed, fabricated, and tested to demonstrate the efficacy of the LCPA concept. The concept has been transitioned to the CEC Design Agent, Raytheon Company, which is currently developing an LCPA design that is planned to yield the first production units in 2003 to support DDG 51 Flight II/IIa installations, and subsequently become the baseline CEC shipboard antenna.

INTRODUCTION

The Navy's Cooperative Engagement Capability (CEC) provides a means by which radar measurement data from battle group radars are shared in real time to form a composite air picture and to enable cooperative engagements where different units support one another's missile operations.[1] Critical to attaining CEC objectives is a secure communications system with an unprecedented response time, high data rate, countermeasures and radio-frequency (RF) fade resistance, and terminal track accuracy to support gridlock alignment. Phased array antennas are needed to meet these system-level requirements in a directive point-to-point networking topology. These moderately high-power phased array antennas are major contributors to CEC system acquisition and life-cycle costs.

As Technical Direction Agent for CEC, APL, working in conjunction with the Navy's Design Agent, Raytheon Company, has played a leading role in developing array antenna systems for CEC. Figure 1 summarizes CEC array development, including the current AN/USG-2 shipboard cylindrical active array as well as a new-generation low-cost planar antenna (LCPA) currently under development.

Early CEC antenna/transmitter equipment, originally developed during the late 1980s and refined in the early 1990s, used a below-deck traveling wave tube–based

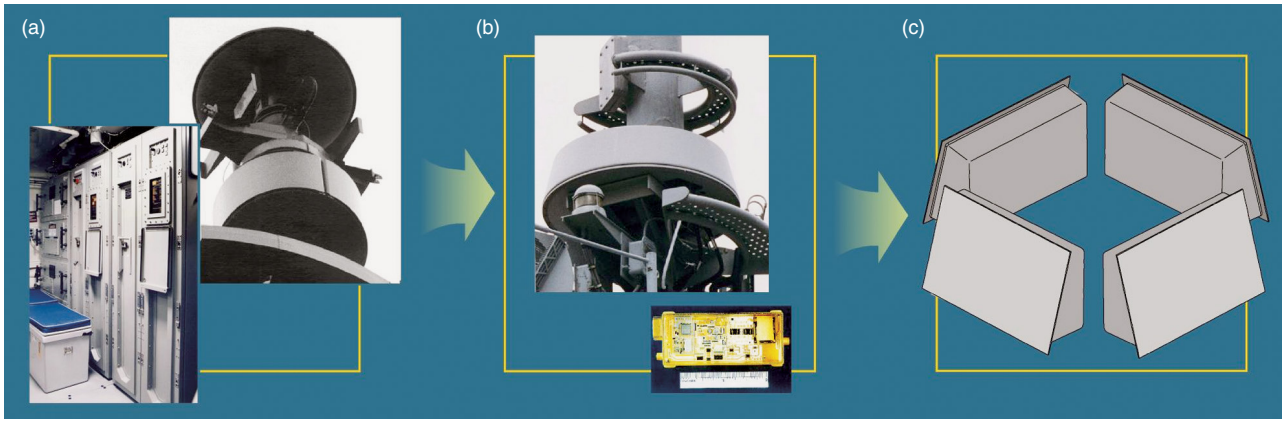

Figure 1. A historical perspective of CEC array antenna development. (a) The AN/USG-1 CEC equipment set, originally developed in the late 1980s and refined in the early 1990s, included a mast-mounted cylindrical array antenna and a below-deck tube-based transmitter. (b) The conical mast-mounted shipboard active aperture, part of the AN/USG-2 CEC equipment set, was developed in the mid-1990s and used MMIC-based transmit/receive modules (inset). (c) The four-face low-cost planar antenna is currently under development and planned for Fleet introduction in 2003.

transmitter and a mast-mounted cylindrical phased array antenna that applied "positive-intrinsic-negative" diode phase-shifter technology. This configuration, part of the AN/USG-1 CEC equipment set, was used for CEC initial operational capability in 1996. In the mid-1990s, an active cylindrical array antenna, which became known as the shipboard active aperture (SBAA), was developed. The SBAA uses gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) transmit/receive (T/R) module technology to realize the transmitter function within the antenna, thus eliminating a large amount of below-deck equipment that was associated with the previous tube-based transmitter.

Introduction of the SBAA resulted in a system weight savings of 4000 lb, reduced prime power requirements, and greatly improved system reliability. The SBAA, part of the AN/USG-2 equipment suite, was successfully demonstrated as part of CEC initial operational test and evaluation in 1997 and operational evaluation in 2001, and is currently in low-rate initial production at Raytheon. The SBAA was the first Navy active array to be fielded onboard ships and has demonstrated excellent performance and reliability at sea.

Despite the advances of the SBAA, there was a strong desire to reduce the active antenna total ownership cost (which includes acquisition, operation, and support costs) to support Fleet-wide deployment as well as new CEC applications. For example, the installation of two cylindrical SBAA antennas would be required on the USS *Arleigh Burke* class (DDG 51) Flight II/IIa destroyers. Clearly, this would be a costly approach given the large quantity of DDG 51–class II/IIa ships slated for installation. A critical need existed for a CEC array antenna system that would provide the required flexible DDG 51 installation, and significant total ownership cost avoidance relative to a single SBAA.

In 1998, APL began exploring ways to achieve total ownership cost avoidance. Also that year, the Laboratory conceived a four-face planar variant of the SBAA that could provide for the installation flexibility on the DDG 51. However, the projected acquisition and lifecycle costs for the cylindrical SBAA and its planar variant still exceeded desirable levels. A fresh approach to reducing CEC array antenna costs was needed.

One conclusion drawn from these initial concept development efforts was that the four-face planar array solution to support DDG 51 installation of CEC would also be conducive to future ship classes such as DD X, which were considered to be unlikely to support cylindrical mast-mounted antennas. It was also clear from ongoing CEC as well as other Navy shipboard antenna development efforts that solid-state active array technology was the most likely approach to address shipboard reliability, maintainability, and availability requirements and associated operational and support cost goals.

LOW-COST ARRAY DESIGN APPROACH

Anecdotal evidence from fielded phased array antenna systems, including the CEC SBAA, indicates that the T/R modules account for 30 to 50% of the production acquisition cost of such systems. T/R modules have historically cost DoD from $1,000 to $10,000 each, depending on the performance requirements, design complexity, and quantities purchased. Clearly, reducing the cost of the T/R module would be an important aspect in lowering the production acquisition cost of a phased array antenna. Noting the retail price of cellular telephones or pagers in the last few years leads one to believe that low-cost modules are feasible. The commercial market pull of the wireless revolution has

spurred the development of excellent low-cost products whose technologies should be readily adaptable to the CEC application. However, what performance differences and purchasing practices that make these consumer products low in cost would need to be adopted?

The LCPA concept was developed to address critical Navy needs for CEC antenna total ownership cost reduction and flexible shipboard integration of a single CEC antenna system.

Cellular phones operate in the ultra high frequency range, not the microwave regime of CEC. Furthermore, the transmitter in a cellular phone is limited to about 1 W of output power, rather than the significantly higher value of an SBAA CEC shipboard module. Finally, cell phone handset sales are reported to have been more than 400 million in 2000.[2] The need for CEC modules for the next 20 years would be at least 3 to 4 orders of magnitude less than that number. We examined the implications of each of these factors to a potential CEC T/R module.

The cost of a MMIC amplifier is not appreciably affected by the operating frequency. In fact, many lower-frequency cell phone power amplifiers are made through a pseudomorphic high electron mobility transistor (pHEMT) MMIC process to achieve high direct current (DC)-to-RF efficiency, and thus provide longer talk time on a single battery charge. The telephone manufacturer is unconcerned with the fact that the pHEMT process was originally developed, with DoD support, to achieve improved MMIC device performance at microwave and millimeter-wave frequencies. What does affect cost is the output power requirement of a MMIC amplifier. Higher output power requires larger transistors, which occupy more chip area. Larger chips mean fewer chips per wafer in manufacturing, and thus higher cost per chip. The cost per unit area of MMIC chips depends heavily on the number of wafers manufactured with a given process type, as well as the yield of acceptable chips from a wafer. A heavily loaded MMIC foundry process will have achieved the manufacturing efficiencies required to make and keep it competitive in the marketplace. It matters little to the foundry process that MMIC chips are being made from different design masks for different operating frequencies. Thus, a major factor in lowering the production cost of T/R modules for CEC is to use commercially viable MMIC processes at a heavily loaded foundry while using a high-yielding design that keeps the MMIC chips small (i.e., low power).

The relatively low quantities of MMIC chips needed for CEC are not an impediment to low cost if commercially successful foundry processes are employed. However, the rapid pace of change in the consumer telecommunications industry makes the issue of component obsolescence a certainty. Consumer product lifetimes are measured in months, whereas a CEC antenna system is likely to be in production for 6 or more years, with spares requirements for at least 20 years. One solution to this problem is to make a lifetime buy of MMIC chips before the foundry process is bypassed by the commercial market. Another approach is to embrace the evolution of commercial developments and plan to upgrade the MMIC design periodically to take advantage of improved performance while continuing to use commercially viable foundry processes that offer low production costs.

A commercially successful MMIC chip requires several design iterations to optimize performance against the process limits and tolerances to ensure consistent high yield. Because a design iteration can take 3 to 5 months and cost more than $100,000, it is not unusual for a new MMIC design to require 12 months and $500,000 for development. Because a T/R module contains three or more unique MMIC chips, the nonrecurring engineering and development time can be considerable. If commercial of-the-shelf (COTS) MMIC chips can be used, the development costs can be avoided. In addition, a successful COTS MMIC chip implies that it is manufactured on a highly loaded foundry process line at consistently high yield. As a corollary, a modification to COTS (MCOTS) MMIC design is likely to yield a less costly solution than a full custom design.

MMIC chip cost only addresses 30 to 50% of the T/R module cost. Other factors are the package or housing with the requisite connectors, other components in the module, assembly and test labor, and rework labor or scrap cost if yield at final test is poor. Several cost benefits accrue if the functionality of the module is kept simple:

- Both the quantity of other needed components and the size of the package are reduced.
- Assembly and test labor is more readily reduced through automation.
- High first-pass module yield at final test is more easily achieved.

There are also low-cost alternatives to conventional RF and digital control connectors, and these are heavily used in consumer electronics products.

A number of large, highly automated factories were required to produce the 400 million cell phones in 2000. Significant production outside the United States is also presumed in this endeavor. Clearly, this is outside the realm of any CEC solution to module production. The optimum production rate of a module factory depends

on the type of process for which it was designed. Some factories are designed for batch production of short production runs and are therefore adept at changing the automated equipment quickly to another product. However, the production rate of these types of factories is limited because the versatility of the automated equipment comes at the expense of production speed and attendant labor. Other factories are designed to run at high production rates for long periods with little human intervention. Downtime to reconfigure the equipment for another product can be expensive in these factories. Additionally, significant tooling charges are incurred to adapt the product to the equipment. As a rule of thumb, the minimum production rate for running three shifts per day, 7 days a week, on a small-size line of this type is 10,000 units per month (about 15 units per hour).

The current CEC shipboard antenna requires about 100 T/R modules. An order for 10 systems plus spares requires a production run of less than 1500 modules, which is appropriate for a batch-type production line but not a high rate line. If a low-cost antenna would need 1500 modules per system, an order for 10 systems plus spares might require a large enough production run to persuade a high-rate manufacturer to operate the small line for 6 to 8 weeks each year to make CEC modules. Running on this type of line should result in significant labor cost savings. The goal should be to keep the labor cost to less than 25% of the total module cost. Use of an industry standard style package and commercially viable construction technologies should reduce process development and tooling charges for module manufacture.

The argument for using COTS or MCOTS MMIC chips can be applied to other array components as well. One major item in this category is the power supply. Many choices are now available for modular supplies that meet military requirements, but are built side by side with industrial-grade units on automated assembly lines. These units have been developed in response to commercial demand for distributed DC power in computing and data communications systems. The use of commercially viable production processes is also valid for printed wiring boards, where multilayer boards containing both RF and digital control circuitry can be integrated in one process. By tailoring the array design to make use of commercial process capabilities, the economies of scale from the consumer electronics market can accrue to military programs like CEC.

Another key to achieving low production costs is to limit manual or touch labor through higher levels of integration, application of commercial electronic packaging design techniques, and design for automated high-volume assembly processes. These techniques can be implemented in an array design by combining RF beamforming, DC power, and digital control distribution manifolds into a single multilayer printed circuit board (PCB) that is manufactured with commercial high-volume production processes. This concept can potentially be extended to include the array aperture by constructing patch radiating elements and their feeds as additional laminations of the PCB. Electronic modules such as T/R modules can be attached via automated pick-and-place equipment. These techniques will dramatically reduce parts count, cabling, and interconnects and should significantly reduce material, assembly, and integration costs.

Finally, the antenna design should be modular. This allows multiples of a single line replaceable unit (LRU) to be manufactured, achieving production economies of scale, and simplifies maintenance and spares. Careful attention must be paid in partitioning functionality to optimize the reliability and cost of the LRUs, exploit the graceful degradation inherent in an array, and use additional redundancy only where needed to meet reliability requirements.

CEC LOW-COST ARRAY DESIGN CONCEPT

The argument has been made that low-cost arrays can be achieved with simple, low-power module designs using commercial processes in high-volume production and implemented in highly integrated array subassemblies. Can lower-power modules be used to achieve a full performance-compliant CEC array antenna? The principal system requirement driving the sizing of a CEC array, and thus its cost, is the effective radiated power (ERP). For an active array, there is a classic trade-off between the module power and the number of modules to achieve the required ERP. The ERP is proportional to the module power times the square of the number of radiating elements or modules.

$$\mathrm{ERP} \propto P_{\mathrm{m}} N_{\mathrm{e}}^{2} \ ,$$

where P_{m} = module power, and N_{e} = number of elements and modules.

Although with a lower-power module more modules are required to achieve a specified ERP, the relationship is not linear. As more modules are added, both gain and power increase. In parametrically investigating module power and element count for ERP-compliant CEC arrays, it was found that, assuming achievable front-end losses, reasonable CEC array sizes could be obtained with transmit modules on the order of 1 to 2 W. Low-power modules were indeed a viable alternative for CEC and provide for module quantities suitable to high-volume, low-cost production lines. (The above trade-off is application-specific. For example, a low-power module solution is attractive for a moderate-power communications link such as CEC, but not necessarily for high-power radars.)

Following the low-cost design approach outlined, a new four-face planar CEC antenna design concept was conceived. In performing design-to-cost optimization studies, cost comparison spreadsheets were used to compare the SBAA antenna architecture to alternatives with lower-power T/R modules and with separate transmit and receive modules. This study indicated that at power levels below about 1 W per module, the antenna cost started to rise owing to increased structure, higher LRU count, and more complex control and signal distribution. It was found to be advantageous to implement each array face with separate transmit and receive apertures in a common physical enclosure. This approach greatly simplified module complexity, leading to lower estimated module production costs; enabled a highly integrated implementation suitable to commercial printed wiring board fabrication techniques; and simplified implementation of independent amplitude weightings for transmit and receive sidelobe control. This new antenna concept, the LCPA, is illustrated in Fig. 2. The array primarily comprises subarray LRUs that are combined in the horizontal plane. For shipboard reliability and maintainability, the subarray LRUs are to be designed for high reliability and easy replacement. These LRUs, along with other ancillary electronics, are housed in an enclosure which is commensurate with the shipboard environment and suitable in size for installation on intended ship classes. A protective radome is used to cover the radiating apertures.

Simplified COTS-Based T/R Modules

Achieving very low module production cost is critical to meeting the LCPA cost objectives. As a communications system, the requirements that flow to the CEC T/R modules are less stringent than those typically required in military radars. As a result, these modules are functionally simple relative to conventional military T/R modules. The receive modules contain a phase-shifter MMIC, a postamplifier MMIC, and a low noise amplifier (LNA) MMIC. Similarly, the transmit module consists of a phase-shifter MMIC, a driver amplifier MMIC, and a power amplifier MMIC. In each module, a shift-and-store register, realized as a silicon IC in chip form, is included to translate serial data into a parallel data format to control the phase-shifter setting and turn the DC power on or off in the module. An attenuator MMIC is not needed in the receive modules because the amplitude taper for sidelobe control is achieved in the beamformer. The transmit modules do not need an attenuator because the modules will be operated in gain compression for all operating modes. Lower-power modes are accommodated by turning off some modules to thin the array. Furthermore, sidelobe requirements do not drive the modules to stringent amplitude and phase error levels. The phase calibration constants for each array element will be kept in the subarray-level digital control electronics rather than in individual modules. Thus, these relatively simple modules contain only 3 MMIC chips, 1 digital IC, 2 transistors for DC bias on/off, and a few resistors and capacitors, in contrast to the SBAA T/R module, which contains 8 MMICs, 3 silicon ICs, and about 80 other components.

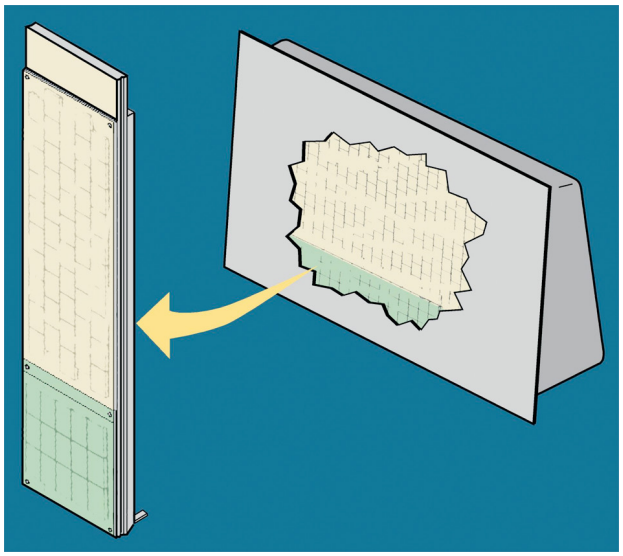

Figure 2. The low-cost planar antenna concept, showing separate transmit (yellow) and receive (green) apertures and the modular subarray implementation.

A catalog search was undertaken to identify COTS MMICs appropriate to the CEC application. It was determined that all required functions were available off the shelf. An LNA, phase-shifter, postamplifier, power amplifier, and driver amplifier were each identified as available in MMIC form.

Because T/R modules account for about a third of the antenna cost, careful attention was paid to developing production module cost estimates. For the LCPA, module cost is critically important to meeting the antenna cost objective because of the large quantity of relatively low-cost modules used in an antenna. The approach was to estimate the cost of the components in the module and the percentage of the cost in each labor category.

The MMIC cost is estimated using the total area of the MMIC chips and a value of $\$2.50/mm^2$ of chip area. The raw, unyielded chip cost at commercial foundries is generally less than $\$1.00/mm^2$ for MESFET processes on 4-in. wafers purchased in 500-wafer quantities. Factoring in typical DC, RF, and visual yields and adding the cost of wafer testing and chip dicing and packing results in typical MMIC costs of \$1.50 to $\$3.00/mm^2$. These costs will be further reduced as GaAs foundries transition to 6-in. wafers to increase production volume.

A GaAs MMIC chip area of 11.5 mm^2 was assumed for the transmit module and 8.5 mm^2 for the receive

module, resulting in MMIC cost estimates of $28.75 and $21.25, respectively. The silicon IC and control transistors in each module were estimated at $3.25 total, and the module housing (identical for transmit and receive modules) at $12.00. These estimates are based on vendor budgetary and rough order of magnitude quotes obtained when material was purchased for the concept evaluation modules discussed below. The cost of other parts in the modules was estimated at $6.00 each for the transmit module and $8.00 for the receive module.

Assembly and test labor was estimated at 25% of the cost of each module and engineering support labor at 10%. An additional category, yield contingency, was included at 10% to account for the fact that modules which fail final test are not to be reworked. This exercise resulted in a high-volume production cost estimate of $100 for the transmit modules and $89 for the receive modules. These are aggressive cost estimates that assume 200,000 transmit and 60,000 receive modules ordered at one time. Phased orders occurring over several years may increase the cost by 2 to 3 times these estimates. It should be remembered also that this is a cost estimate and not a negotiated price to the government.

Subarray Architecture Tile

The subarray LRUs, which incorporate the radiating elements, transmit and receive modules, distribution manifolds, and digital control electronics, are implemented in a highly integrated tile architecture (Fig. 3) that is critical to achieving the cost objectives.

The patch-radiating elements and their feeds are realized in a multilayer PCB assembly. This aperture board mounts onto one side of a cold plate, and the transmit and receive modules mount to the opposite side of the cold plate. The modules are packaged in COTS-derived housings that are small enough to easily fit within the lattice spacing of the radiating elements. Interconnections between the radiating elements and the transmit or receive modules are achieved by coaxial feedthroughs. The cold plate serves as a structural backbone, provides critical alignment of all components, and provides cooling for the modules. The aperture board and coaxial feedthroughs provide space to accommodate receive protectors and bandpass filters for the receive elements and ferrite isolators and low-pass filters for the transmit elements. These items are needed to protect sensitive active devices in the transmit and receive modules from the harsh shipboard electromagnetic environment.

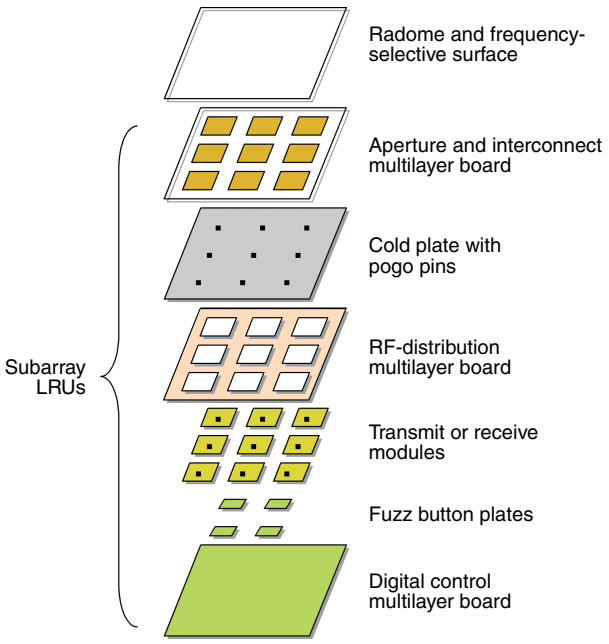

Figure 3. Conceptual view of the LCPA tile architecture.

A second multilayer PCB mounts to the module side of the cold plate. This distribution board accommodates the RF manifold (beamformer) and DC power and digital control distributions and provides RF, DC, and digital connections to the modules through conventional solder tab leads. This multilayer board has cutouts so it can mount to the cold plate without interfering with the modules. Finally, the digital control electronics are housed on a third board that overlays the modules and connects to the distribution board.

A critical aspect to achieving the low-cost subarray architecture is the use of connectorless interconnects. The modules, for example, contain no connectors. The module-to-aperture board interconnect is achieved with a pogo pin approach. A glass-sealed coaxial pin with a 50-Ω characteristic impedance is placed through the bottom of the module package to act as an RF feedthrough. A compression pin, i.e., the pogo pin, is employed as the center conductor in a length of coaxial line that passes through the cold plate.

The pogo pin consists of a pair of concentric tubes with a small internal coil spring that pushes on the inner tube to cause it to protrude from the outer tube. This assembly has the same diameter as the inner conductor of a standard semi-rigid coaxial cable (0.5 mm or 0.020 in.). A hole drilled through the cold plate is filled with the dielectric tube from a piece of semi-rigid coaxial cable, and the pogo pin is inserted in the center hole of the dielectric to form a 50-Ω coaxial feedthrough. The exposed pin on the bottom of the module presses against the pogo pin as the module is attached to the cold plate, thus making an RF connection as well as locating the module on the cold plate. The other end of the pogo pin presses onto a printed trace on the aperture multilayer board to provide a connection to the antenna element.

Pogo pins are manufactured in large quantities for use in very large PCB test fixtures. Consequently, these pins cost less than $1 apiece when purchased in quantity.

When compared with $5 to $15 per mated pair for a blind-mate RF connector, this is a low-cost innovation that has not gone unnoticed by designers for the consumer wireless market.

The connection between the modules and the distribution board can be achieved in one of two ways. In the first approach, the other RF connection, along with the bias and control signals, is made in a conventional manner. Flat leads, which protrude from one side of the module package, are soldered to the exposed traces on the edge of a cutout in the RF, DC, and control distribution board. The single RF lead is accompanied by a ground lead on each side, which forms a coplanar waveguide transmission line. In this manner, a connectorless module is realized. In the second approach, the interconnection between the modules and the RF, DC, and digital distribution board can be made with fuzz buttons. These components are made of fine, stiff wire that is gold-plated and randomly formed, like a scouring pad, into a small rod shape. Diameters as small as 0.5 mm (0.020 in.) are available commercially at low unit cost. When constrained in holes in a thin carrier plate and then sandwiched between PCBs, fuzz buttons form a planar interconnection without the need for solder, conductive epoxy, or a plug-and-socket connection. This provides a low-cost–compliant connection with relaxed tolerances in three dimensions for bias voltages and digital control signals. A current-carrying capacity up to 5 A is readily achieved. Multiple fuzz buttons have also been used successfully for RF connections.

The LCPA design concept features a minimum number of components and integrated structure, cooling, and alignment functions. Such highly integrated structures can create significant inherent stiffness, allowing the unit to survive the standard shipboard shock test without additional structural elements. From a cooling perspective, the LCPA design concept is adaptable to either liquid- or air-cooled approaches. Shipboard active aperture antennas tend to be liquid-cooled, primarily driven by the need to maintain junction temperatures to support high reliability, and thus have a very low probability of maintenance action during the ship's mission while in an operating temperature range of –25° to +55°C in a salt-laden ambient air environment. However, future land mobile applications, which are driven by different missions and environments, will likely benefit from air-cooling.

DEMONSTRATION T/R MODULES

To demonstrate the utility of COTS-based modules for CEC, transmit and receive modules were designed and a small number fabricated and tested. The demonstration modules (Fig. 4) used commercially available MMICs. About 12 modules of each type were fabricated and tested at APL.

The transmit module used a COTS power amplifier MMIC, which was 4 mm^2 in area and supplied 1.25 W of RF power at 25°C. This power level is slightly less than the performance that would be required for the intended shipboard application. An MCOTS MMIC power amplifier that supplies the required output power

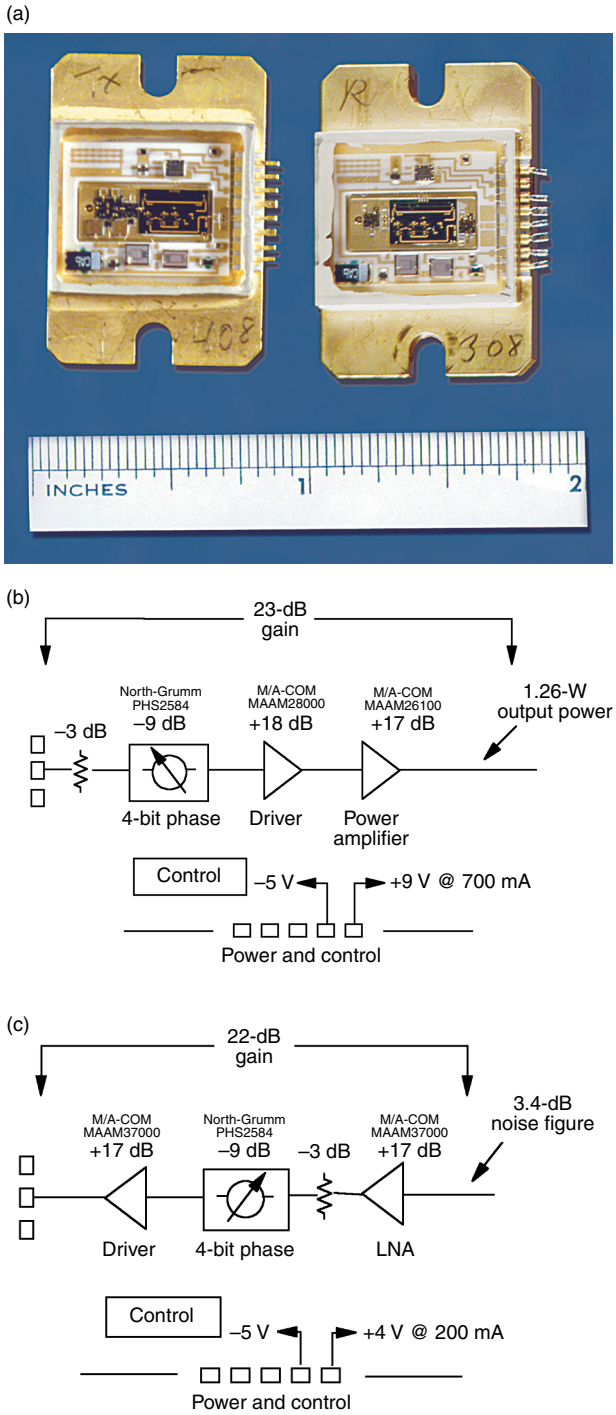

Figure 4. Transmit and receive modules fabricated at APL with COTS MMICs for the CEC LCPA concept evaluation array: (a) prototype transmit and receive modules and (b) transmit and (c) receive module block diagrams.

should occupy less than 5 mm^2. Because an MCOTS or custom design could be 10 to 15% more efficient than the 30% efficiency of the COTS unit, the actual heat dissipation of the transmit module could be less in production units. The only suitable COTS phase-shifter chip identified was a broadband 6-bit design that occupies 26 mm^2 in area. Because fewer bits of phase control are required, it is projected that a custom design could be as small as 4 mm^2, based on scaling the size of comparable units that operate at higher frequencies. Additionally, a 3-dB chip attenuator was placed next to the phase shifter in the RF path to mitigate the large voltage standing wave ratio of this device. A custom phase shifter would presumably be designed with a better impedance match, so the chip attenuator would not be needed in production units. Thus the concept evaluation modules are slightly larger and dissipate more power than the projected production units.

The receive module used a COTS LNA and postamplifier chips, each 2 mm^2 in area. This is about the minimum area projected for these MMICs, even if they are custom designed for CEC. The phase shifter is identical to that used in the transmit module. The receive demonstration module was projected to have superior performance relative to the current CEC T/R module, based on typical values for the COTS MMIC chips from manufacturers' data sheets. The noise figure should be 1 dB lower, the third-order intercept point at the input should be 5 dB higher, and the gain should be comparable. The demonstration receive module does not use a receive protector to shield the MMIC from the electromagnetic environment. A receive protector could be implemented in the aperture multilayer board or in the module. The demonstration receive module has more than enough performance margin to accommodate the insertion loss of the receiver protector and RF filter in shipboard production units.

The housing selected for the demonstration modules is similar to a commercial unit used to house RF power transistors. Kyocera America, Inc. modified its hermetic package to APL requirements by placing a glass seal feedthrough in the copper tungsten base and providing eight ribbon leads through a ceramic wall on one side. As described previously, the center pin of the glass feedthrough engages a pogo pin in the cold plate to make a coaxial connection to the radiating element through the aperture interconnect board. This engagement also locates the module on the cold plate prior to securing it with shoulder screws, which are accommodated by slots in the package base. This housing provides a large surface area to conduct heat from the power-amplifier MMIC chip to the cold plate. Both receive and transmit modules use the same housing. A production version of this housing could eliminate the screw-mounting tabs (Fig. 4) in favor of compliant conductive epoxy mounting to the cold plate. While reducing the weight of each module only slightly, it would have a significant impact on system weight because of the large number of modules in each array face.

About 12 modules of each type were assembled at APL using standard microelectronic processes and techniques. Internal details of this assembly are shown in Fig. 5. A multilayer ceramic substrate is mounted to the base of the package and surrounds a pedestal formed integral to the base. The MMIC chips are mounted on this pedestal with conductive epoxy (or eutectic solder in the case of the power amplifier). The ceramic substrate contains imbedded wiring and component mounting pads for bias and control functions that are unique to each module type. This substrate was fabricated at APL from low-temperature cofired ceramic that is patterned and routed in green tape before being stacked and fired under pressure to form an integrated multilayer ceramic unit. The top of the ceramic substrate is even in height to the top surface of the MMIC chips, thus allowing direct wirebonding

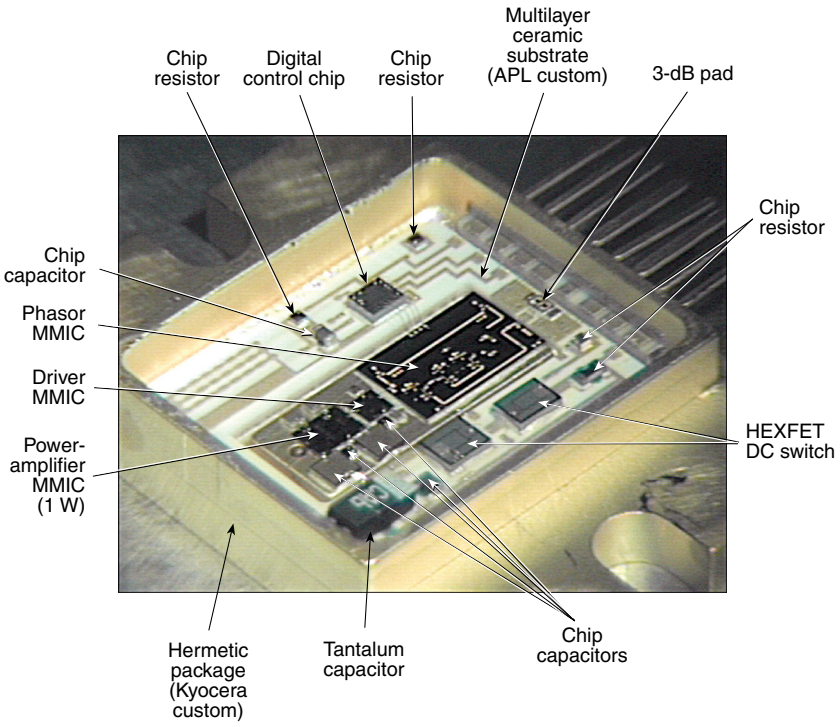

Figure 5. Details of the CEC LCPA concept evaluation module designed and fabricated at APL.

to the bias and control wiring on the substrate with minimal height change or interference to the bonding tool from component features. Chip-to-chip wirebonding was used between MMIC chips and from MMIC chips to chip capacitors mounted on the pedestal. Constant-length wirebonds[3] were used for all RF path connections. This has the effect of controlling the impedance at each interconnection, which leads to uniformity in electrical length from module to module.

Following assembly, the modules were tested for RF functionality before lids were welded in place to form a hermetic package. Of the 12 transmit modules fabricated, 9 passed the pre-seal functional test. Two of the failed modules were subsequently reworked and went on to post-seal characterization. The remaining transmit module had a failure in the ceramic substrate. Eleven, or 92%, of the transmit modules fabricated were characterized and included in the total data set. Of the 11 receive modules fabricated, 10 passed the pre-seal functional test. After rework, 11 were characterized post-seal. One receive module failed in characterization, leaving 10 units, or 91%, to be included in the data set. Both receive module failures suggest that reverse bias voltage had been applied to the digital control chip, leading to speculation of an intermittent short between the positive and negative bias lines in the module.

Typical transmit module performance at room temperature (25°C) is shown in Fig. 6. The frequency response for the four most significant bit settings of the phase shifter, shown in Figs. 6b and 6c, indicates appropriate functionality of the phase shifter. The power sweep plot (Fig. 6a) indicates an output in excess of 1.25 W (31 dBm) at the low end of the band. The second and third harmonic outputs are shown as well. All 11 transmit modules provided a mean output power of 31 dBm with a 1-σ deviation of 0.25 dBm at room temperature when averaged over the frequency range. Power-added efficiency was 23.3% with a 1-σ deviation of 1.9% under these same conditions. The 10 receive modules provided a mean noise figure at room temperature of 3 dB and a mean gain of 23.2 dB when averaged over the frequency band. It should be noted that the data were not corrected for test fixture loss or match. Thus a coaxial interface to an SMA connector (which uses a pogo pin) at the antenna port of the module is included in the data.

Figures 7 and 8 show the performance of the modules statistically. The root-mean-square (RMS) phase and gain errors for all phase states for a sample of two modules of each type indicate phase errors of less than 6° and gain errors of less than 0.5 dB over most of the measured frequency band. Similarly, the standard deviation (1 σ) of gain and insertion phase over most of the frequency band measured for the entire population is less than 1.0 dB and 15° for the transmit modules and less than 0.5 dB and 14° for the receive modules. This

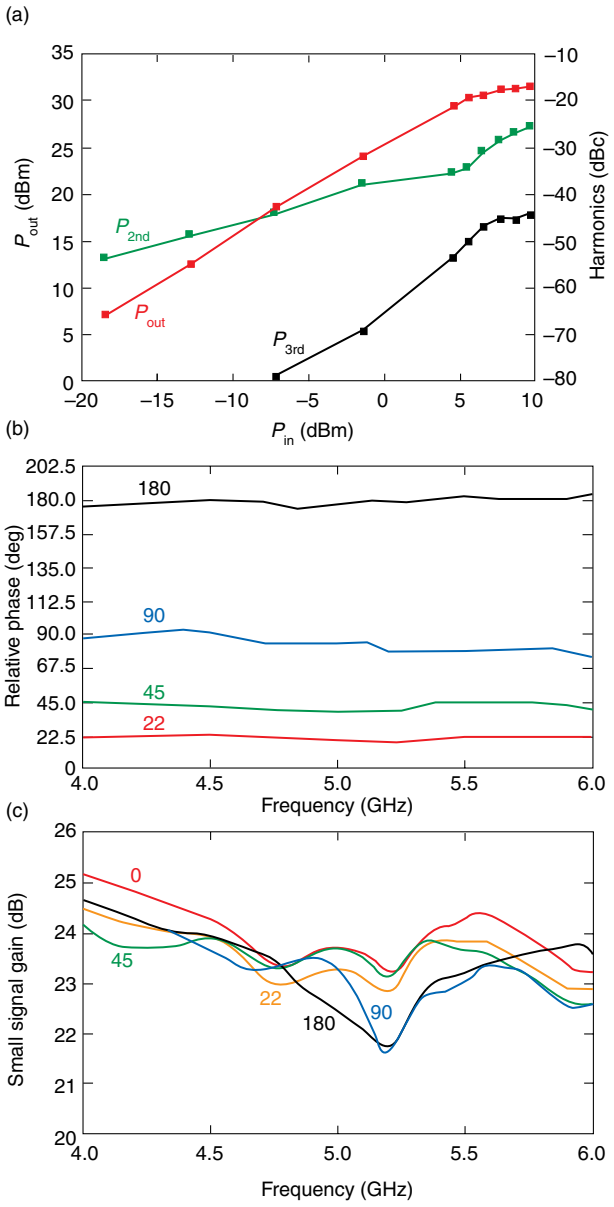

Figure 6. Measured performance of a typical transmit module fabricated by APL for the CEC LCPA concept evaluation array: (a) power sweep showing power output at the fundamental and harmonic frequencies, and (b) relative phase and (c) gain for each major phase bit.

implies that no individual calibration constants need to be applied to the modules in an array setting. Such uniformity between modules is attributed to the use of the constant-length wirebond technique in the RF path.

DEMONSTRATION ARRAY

To demonstrate the efficacy of the LCPA design concept, an array was designed to functionally replicate the key features of an LCPA subarray LRU and then fabricated and tested. To minimize costs, the array was kept small and used the 23 modules fabricated at APL. Thus, a subarray containing a 1×8 element receive aperture

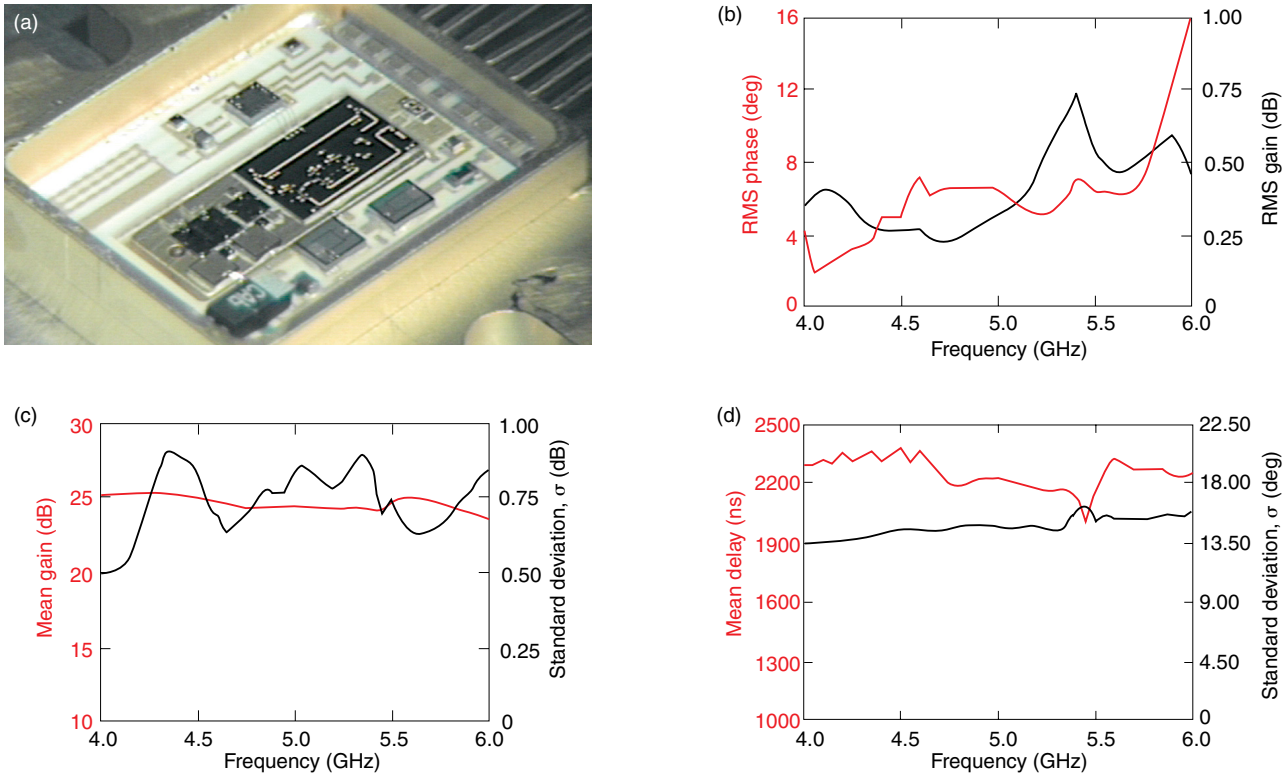

Figure 7. Measured statistical performance of the transmit modules. (a) Photograph. (b) RMS phase and gain error for all phase states of two modules at room temperature and nominal bias. Mean and standard deviation of gain (c) and phase (d) for 11 modules at room temperature and nominal bias. (Gain and phase both at 0 state.)

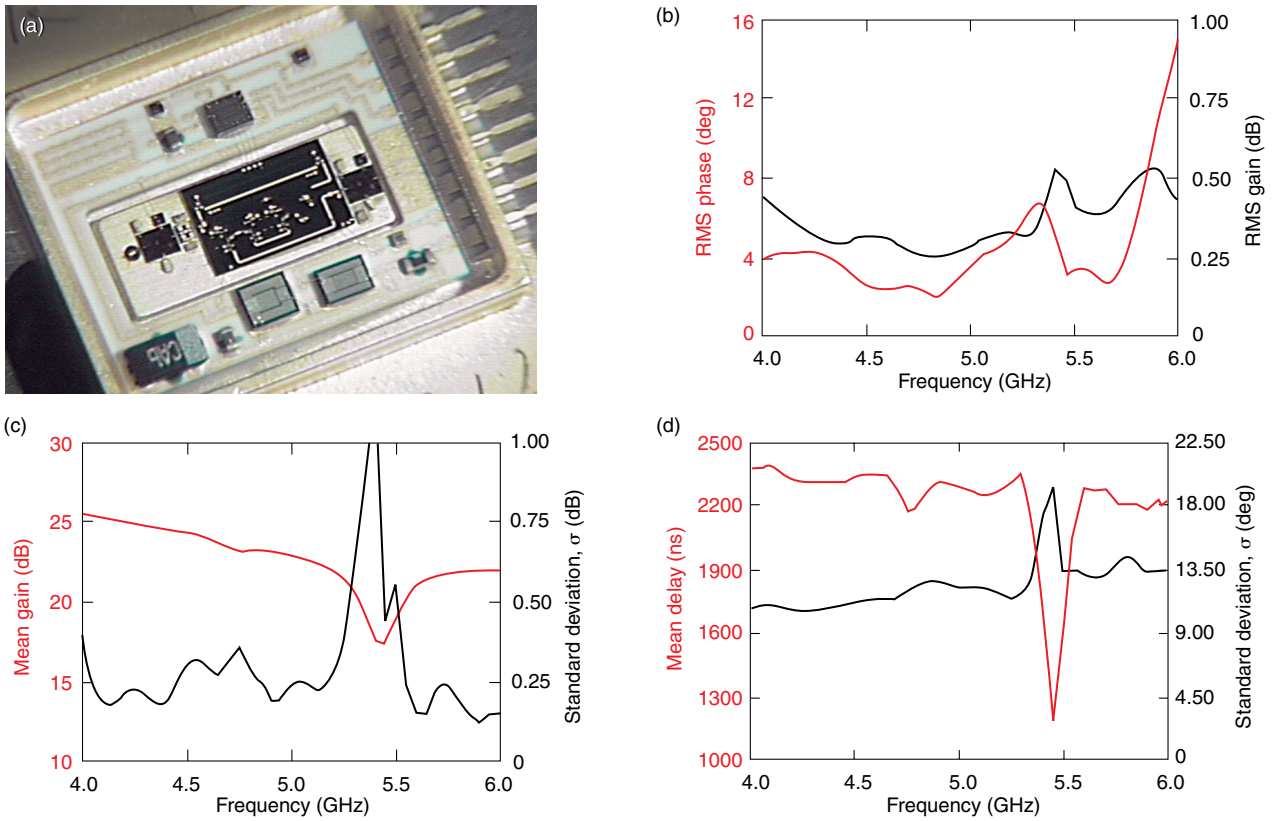

Figure 8. Same as Fig. 7 except for 10 receive modules.

and a 2×8 element transmit aperture was constructed (Fig. 9). The receive aperture was populated by eight receive modules. In the transmit aperture, the central eight elements were populated with transmit modules and the outer eight elements were populated with module packages containing matched loads. Following the LCPA design concept outlined previously, the demonstration array consists of an aperture multilayer board containing the patch radiators, a cold plate, the transmit and receive modules, and an RF, DC, and digital distribution multilayer board. To limit cost, the digital control board was made to plug into the distribution board as a connectorized daughterboard rather than using the fuzz button interconnect. The receiver protectors, isolators, and RF filters are not included in this demonstration array.

Aperture Board

The aperture board integrates the radiating elements, their feeds, and interconnects into a single-piece laminated board attached to an aluminum backing plate. The radiating elements are microstrip patch radiators, with U-shaped slots in cavities formed with plated vias (Fig. 9a). The cavity implementation mitigates scan blindness effects that could be caused by surface wave modes. The interconnections are realized with pogo pins that contact the stripline feed circuits on the aperture board. The stripline transitions to microstrip, which in turn couples to the patch radiator. The aperture board uses 0.5-oz copper-clad Duroid 3003 for the etched feed and patch layers. A thin layer of Kapton is used to protect the exposed surface.

Cold Plate

The cold plate, which serves as the structural backbone of the demonstration array, was designed to use forced-air cooling supplied by a shrouded muffin fan. Although the cold plate could be modified to use any number of cooling methods, air cooling was used to simplify testing and demonstrate feasibility with low-power modules. The cold plate provides a mounting surface and thermal path for the T/R modules, defines the spacing for each module through precise location of the mounting holes, and ensures alignment with the RF feedthroughs (pogo pins). The modules are attached to the cold plate by shoulder screws passing through the module mounting ears. In a production antenna, the modules would be bonded into position instead of screw-fastened, thus eliminating the need for mounting ears. The RF feedthroughs are located in bosses in the cold plate fin area. The feedthroughs were designed to replicate the construction of a 50-Ω semi-rigid coaxial cable, with the pogo pin serving as the center conductor held in place by a Teflon sleeve.

Distribution Board

The distribution of RF signals as well as DC bias and digital control signals is accomplished with a multilayer PCB (Fig. 3). This board mounts to the cold plate with a spacer plate under it and with cutouts to fit around the modules. The PCB is oriented with the digital and power distribution layers on top and the RF beamforming layers located against the cold plate. To maintain proper impedance match, the PCB is fabricated with an

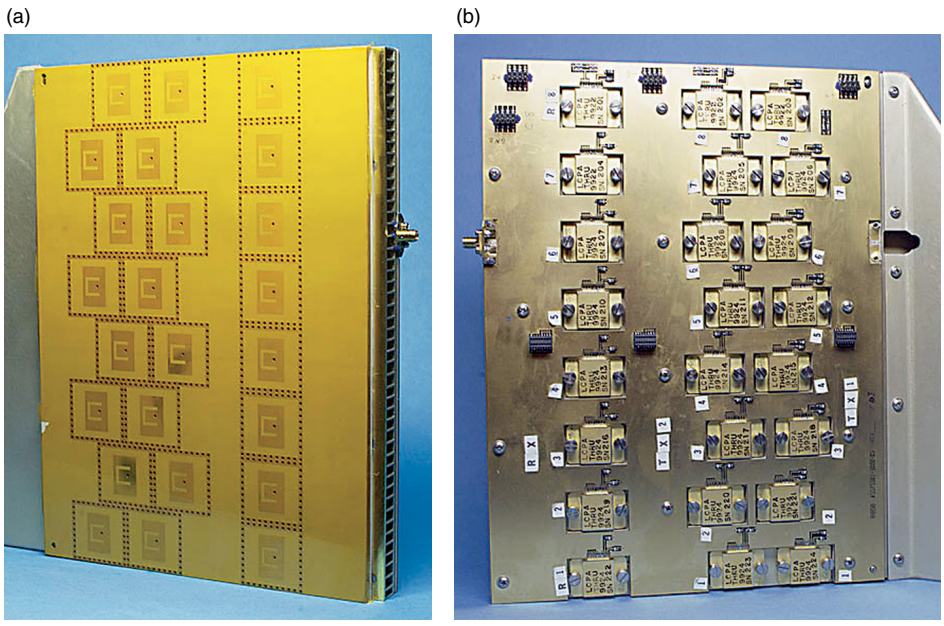

Figure 9. APL demonstration array: (a) front view showing the aperture board containing the transmit and receive microstrip patch radiating elements, and (b) back view showing the distribution board and T/R modules.

exposed ledge in the RF signal distribution layer at each cutout, allowing all module connections to take place on the imbedded RF signal layer. These module leads connect to the RF beamformer, the DC bias traces, and the data, clock, and strobe control signal traces in the distribution board. The spacer plate is used to elevate the PCB such that the ribbon connections to the modules are co-planar. The digital control signals emanate from a digital board that plugs into the three connectors in the middle of the distribution board as a daughterboard. Separate connectors, shown at the top of Fig. 9b, provide bias voltage connection for 9, 4, and −5 V, and ground return using paralleled pins to handle the current.

The 10-layer distribution board contains a bottom RF ground layer, an RF trace layer, and a top RF ground layer separated by two RF dielectric laminates. These RF laminates surround a copper trace layer and a resistive film layer, which accommodates stripline Wilkinson power dividers and combiners with imbedded RF isolation resistors. The power dividers are arranged in a 16-way equal amplitude and phase power divider to form the transmit beam. An 8-way equal amplitude and phase power combiner is used as the receive beamformer. The remaining seven copper layers are contained on conventional printed circuit laminate material (FR4). These layers consist of a top ground layer, a positive voltage plane split between 9 and 4 V on a single copper layer, a strobe buss layer, another ground layer, a data buss layer, a −5 V buss, and a clock distribution layer located above the upper RF ground layer.

PCBs are typically fabricated in their entirety prior to any routing of cutouts. For this board, the ledge that is provided inside the cutout required some routing before final bonding. It also required accurate control of resin flow to prevent resin bleed over the solder tabs during final bonding. Additionally, because the finished PCB would be unbalanced, there was some concern about achieving reasonable flatness. Since this unconventional arrangement might be difficult to manufacture, the design was fabricated at APL as well as by two commercial vendors. The vendors would only accept an order on a best-effort basis. However, all three fabrications were successful and achieved high yields, demonstrating that this design is well within the capability of current commercial PCB fabrication processes.

Digital Control Board

To control the demonstration array, digital circuitry was designed and fabricated to provide each module with a 7-bit encoded phase-shift value as well as a DC power control bit. This 8-bit word is input serially to each module on a single data pin, with timing controlled by an associated clock pin. In addition, a strobe signal gates the newly programmed value to the DC bias switch or phase-shifter MMIC. Because there is an array of modules, each module is addressed and programmed in turn from the digital beam controller. The controller consists of a laptop computer that communicates with an array controller board through a parallel printer port. A digital control board on each antenna subarray panel accepts the signals from the array controller board and directs the 8-bit data value to the appropriate module by gating the clock only to the addressed module. The array is capable of accepting data at a rate compatible with CEC beam update rate requirements, which is much faster than can be provided by the laptop computer. Therefore, the array controller acts as a rate buffer between the laptop and the higher rate of the array itself. The high-speed programming of the array with this controller can only occur in finite-length bursts owing to the much slower average speed of the laptop computer.

A program in the laptop computer calculates the phase-shift values for each module based on the requested beam-pointing position. The array controller board buffers these data and converts them from parallel to serial format using programmed logic devices operating at a 28.5-MHz clock rate. The data, clock, strobe, and module address signals are output on four RS-422 twisted-pair lines that can be up to 10 m in length. Use of differential drivers provides the mechanism to shift the reference ground level to −5 V on the subarray board, making the logic on this board suitable for directly driving the gate of depletion mode transistor switches on the MMIC phase shifter in each module. The digital control board directs data and strobe signals in parallel to each module in a row when that row is addressed. The clock signal is directed separately to each module only when that module is addressed. In this way, digital noise on the RF signal is reduced. The array controller board was fabricated on a Schottky wirewrap board and housed with a 5-V power supply in a box chassis. The digital control board was fabricated using multilayer printed circuit technology and plugs into connectors on the subarray distribution board as a daughterboard.

Measured Performance

After initial checkout in the laboratory, the array was moved to an outdoor range where receive and transmit beam patterns were recorded at several frequencies and beam positions. As shown in Fig. 10a, the receive array was populated with eight receive modules in a single row. A 4×2 transmit array was formed by populating the central eight positions of the transmit array. The outer four positions were populated with module packages containing internal RF terminations. Figure 10 also shows azimuth patterns for both arrays at several

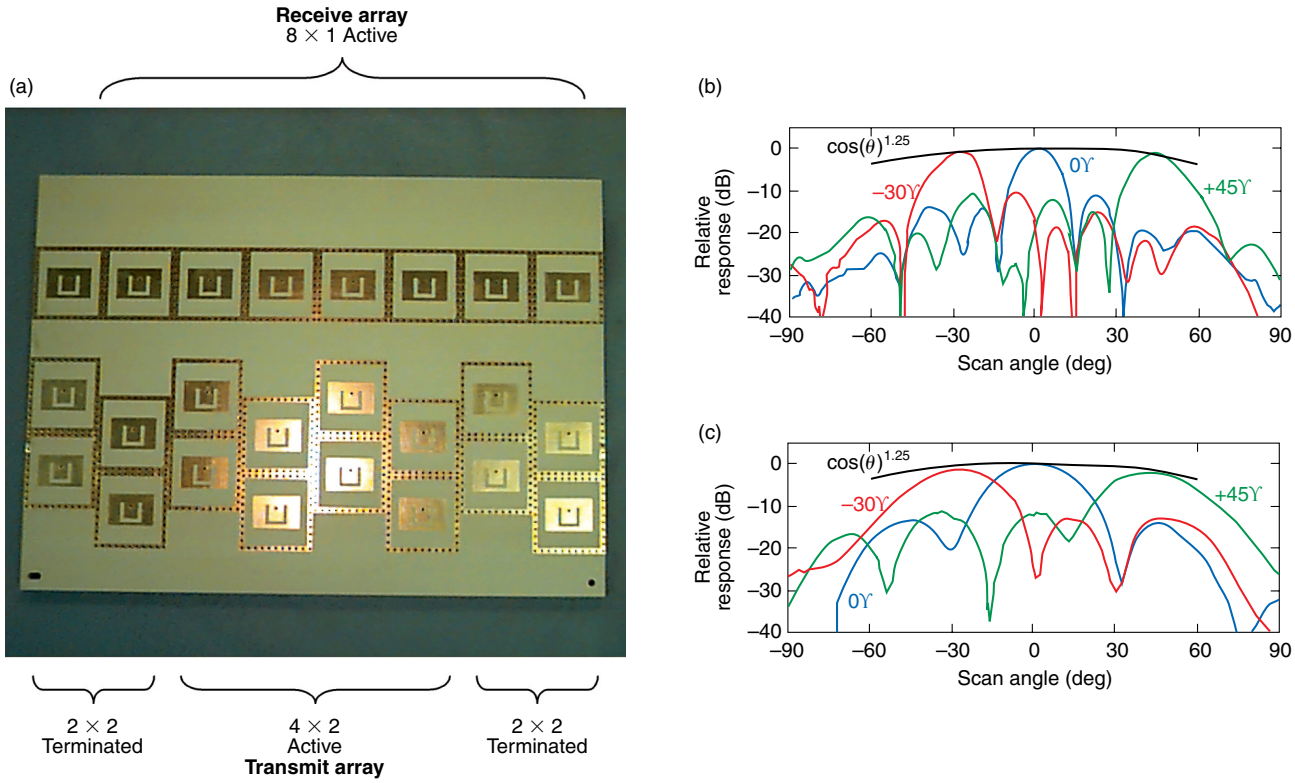

Figure 10. Performance of the CEC LCPA concept evaluation array (a) as measured on the antenna range at APL. Electronic azimuth scanning out to 45° from broadside is shown for both the receive (b) and transmit (c) arrays.

pointing angles. A $\cos(\theta)^{1.25}$ scan loss response is plotted for comparison. Because of the gain and phase uniformity of the modules, no corrections for individual modules were made to the beam-pointing commands. Similar performance was measured at other frequencies in the band.

IMPACT TO THE NAVY

At the direction of the CEC Program Office, PMS 465, the LCPA concept was transitioned to the CEC Design Agent, Raytheon Company, in the fall of 1998. Raytheon is currently developing a fully CEC-compliant LCPA design, with installation on surface combatants slated to begin in 2003. Although the Raytheon design and implementation details differ, they follow APL's LCPA concept. The critical design review stage is complete, and shipboard integration planning activities are under way. Cost analyses project that the LCPA will result in greater than $0.5 billion in total ownership cost avoidance to the Navy. As the Technical Direction Agent for CEC, APL continues to be closely involved in LCPA development and shipboard integration efforts.

In addition to addressing current CEC shipboard antenna needs, the LCPA concept was developed with a view toward future ship classes and CEC applications. For example, the planar configuration, high reliability, and low life-cycle costs are conducive to application on future ship classes such as the DD X. Also, the subarray architecture provides a high degree of modularity and scalability that is amenable to implementing the LRUs in new CEC antenna applications. For example, a lower-cost, lower-weight cylindrical array implementation concept, which uses the same LRUs as the planar LCPA configuration, has been developed to address ships that are better suited to a pole-mast installation or potential CEC land-based mobile or tower-mounted applications.

SUMMARY

The LCPA concept was developed to address critical Navy needs for CEC antenna total ownership cost reduction and flexible shipboard integration of a single CEC antenna system. Figure 11 summarizes APL's LCPA development effort. The Laboratory combined extensive CEC antenna system engineering knowledge, broad active array antenna technology expertise, insight into commercial microwave and electronics manufacturing techniques, and a disciplined focus on cost to develop the LCPA concept. A limited amount of module and array hardware was designed and fabricated to cost-effectively demonstrate the key low-cost attributes of the LCPA design concept prior to requiring a Navy commitment to a full LCPA development

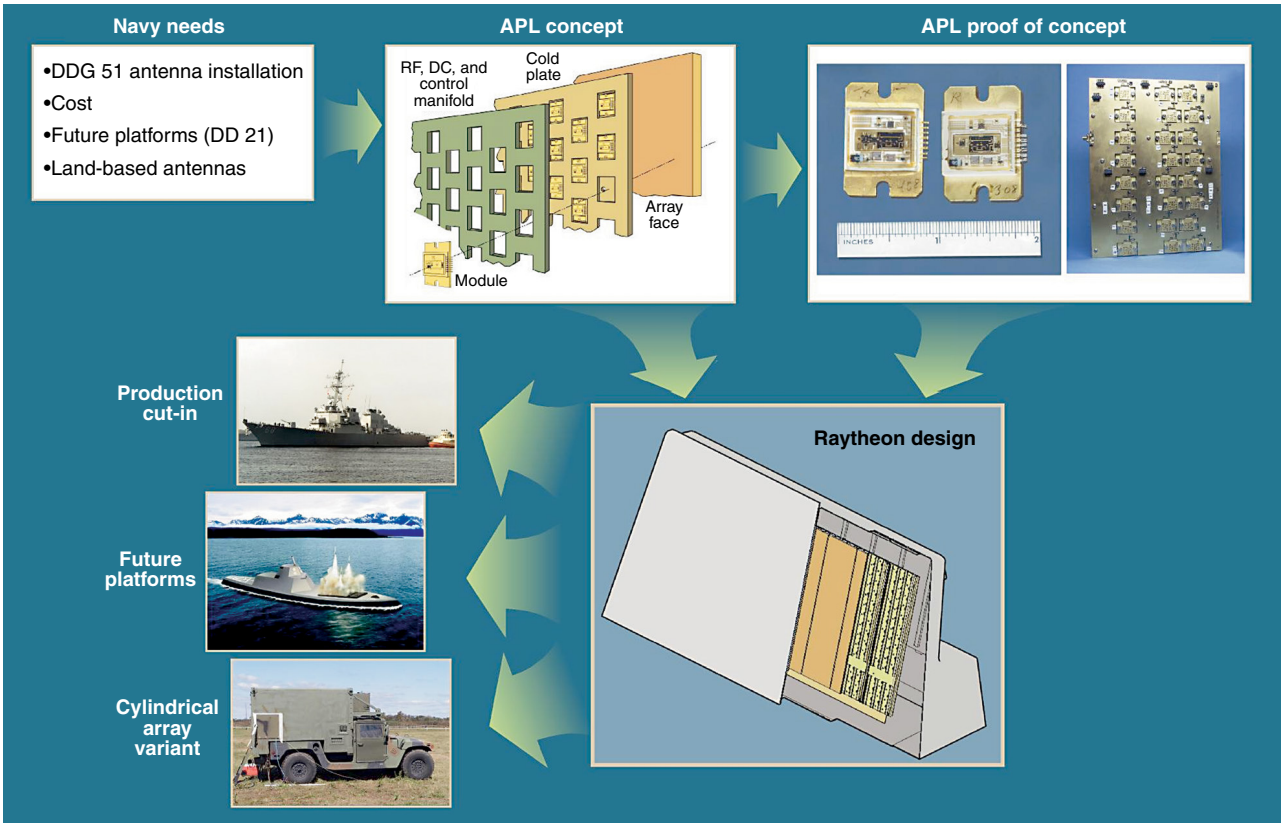

Figure 11. APL development effort for the LCPA.

program. Working with the CEC Program Office, PMS 465, the LCPA concept was then transitioned to the CEC Design Agent, Raytheon Company, where a detailed LCPA design is currently under development. APL remains fully engaged in supporting PMS 465 in the development and ship integration of the production LCPA. Raytheon's LCPA design implementation is planned for Fleet introduction in 2003, with initial installation on DDG 51 class ships. The LCPA is currently projected to provide more than $0.5 billion total ownership cost savings over the current CEC shipboard active antenna.

REFERENCES

1 "The Cooperative Engagement Capability," *Johns Hopkins APL Tech. Dig.* **16**(4), 377–396 (1995).

2 "More Growth in Communications," *Compound Semiconductor* **7**(1), 47 (Feb 2001).

3 Lehtonen, S. J., and Moore, C. R., "Constant Length Wirebonding for Microwave Multichip Modules," *Int. J. Microcircuits Electron. Packag.* **23**(1), 110–117 (2000).

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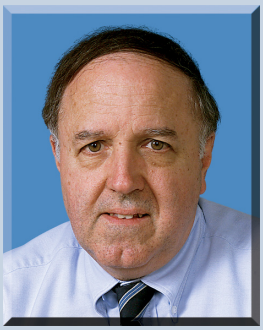
THE AUTHORS



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