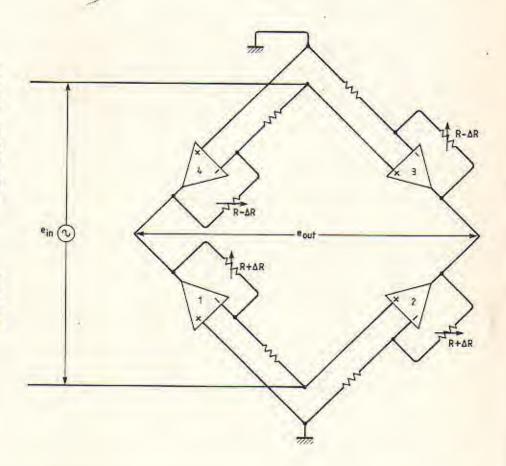
Accurate op-amp bridge

When measurements are made using resistive transducers, the sensors are often included in the arms of a balanced bridge. An improved circuit can be achieved by using an op-amp in each arm of the bridge and positive going transducers $(+\Delta R)$ in arms 1 and 2 or negative going types in arms 3 and 4. The bridge can be built around a single quad op-amp such as the LM324, and four matched sensors, and can be powered by d.c. or floating a.c. Output voltage is

$$e_{\text{out}} = \frac{4e_{\text{in}}\Delta R}{R}$$

This shows that the output is linear over a wide range and has a four-fold sensitivity compared with a single op-amp bridge. The circuit can also provide high output voltage, low output impedance and high noise immunity.

N. Balakrishnan Bangalore India



Interfacing microprocessors

Input and output functions

by J. D. Ferguson, B.Sc., M.Sc., M.Inst.P., J. Stewart, and P. Williams, B.Sc., Ph.D., M.Inst.P. Microelectronics Educational Development Centre, Paisley College of Technology

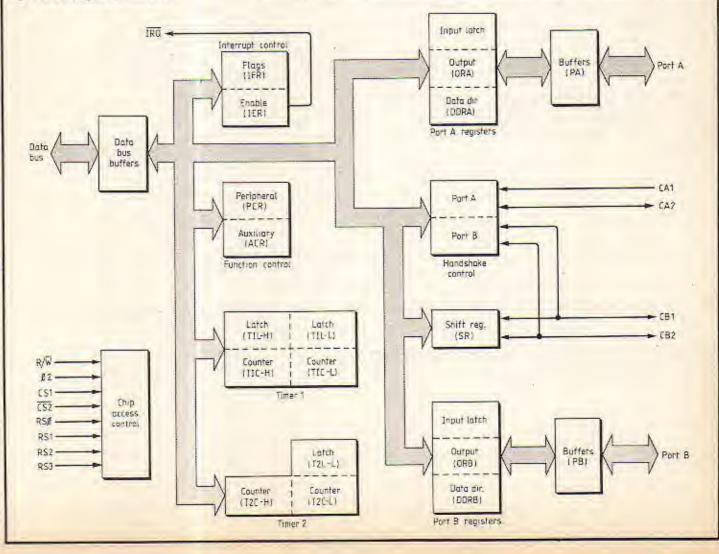
Part one of this series outlined a universal interface for 6502 microprocessor boards and microcomputers. Part two describes the operation and functions of the main i.cs and gives simple examples of driving the devices using machine code or Basic.

The 6522 v.i.a. is a very powerful device which can perform several functions simultaneously. It consists of several independent sections controlled by 16 8-bit registers which occupy 16 sequential locations in memory, the base address being selected by decoding on the microprocessor board. Some registers are directly accessible via the pins of the i.c., while others are set and monitored by the data

Fig. 2. Block diagram of the 6522.

bus. Each register is selected by the four least-significant address bits, A0 to A3, with the i.c. activated by chip-select pins. Data enters and leaves the 6522 in 8-bit bytes and two registers, called ports A and B, are reserved for this purpose. In a hardware oriented system the designer would specify one port as an input and the other as an output, but this would take no account of a common requirement for unequal numbers of pins. For example, if a dozen sensors are scanned and two or three warning indicators are driven, it would be costly to design a range of boards to cope with the large number of possible variations. An alternative scheme has a controlling register associated with each port called the data-direction register. For every bit set to 1 in the d.d.r., the corresponding pin of the port behaves as an output, while a 0 sets the pin to behave as an input. Changing the contents of the d,d,r. can, in one step, alter the status of any or all eight pins of the corresponding port. Similar control can be achieved over the functions, and Fig. 1 shows the format of the auxiliary control register. This is the eleventh register out of sixteen on the chip, and is itself selected by the address decoding at A000 to A00F. Therefore, the address of this register is A00B, Bits 0 and 1 determine whether the latches associated with the ports are latched, allowing data to be held during sections of a program.

Bits 2 to 4 control the shift register, determining whether it is used for serial to parallel or parallel to serial conversion, and also the source of the timing pulses. One of the two internal timers can be used to generate single time delays in a so-called



monostable mode or to count the numberof transitions on a particular pin of a port. The last facility is useful for event counting or as the basis of a frequency meter, while the monostable mode has wide applications in controlled time delays. The timer has an internal 16-bit register which can be reset to a prescribed value under program control, with interrupts being automatically generated at time-out. The second timer has a monostable mode

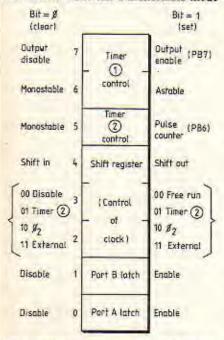


Fig. 1. Auxiliary control register of the 6522. This is the eleventh register and has the address A00B.

Fig. 3. Block diagram of the ADC 0817.

under the control of bits 6 and 7, but can also be used as a free-running generator or astable to repetitively switch an output pin from 0 to 1, with each half-cycle set by the value latched into the corresponding register. This allows the value of a given halfcycle to be continually modified until the end of the previous half-cycle is reached because the timers run independently of. the microprocessor once a sequence has commenced. However, the microprocessor can always interrupt and control the sequ-

The complete range of functions is large and a summary is shown in Table 1, which should be considered in conjunction with Fig. 2. Selected functions will be covered in future articles but full details are available in references 1 and 2.

A-to-d converter

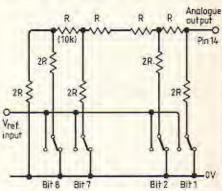
Most a-to-d converters take a single analogue input signal and produce a binarycoded output after an interval of typically tens or hundreds of microseconds. In engineering systems it is more often necessary to rapidly scan a series of inputs and collect the data for further processing. This is possible by combining an a-to-d converter with suitable analogue switching, and a suitable circuit is now available in a single low-cost i.c. The ADC 0817 covers 16channels automatically with an expansion capability for larger systems and, although the problem of signal conditioning remains, for applications with signals above 0.5V a self-contained system is possible.

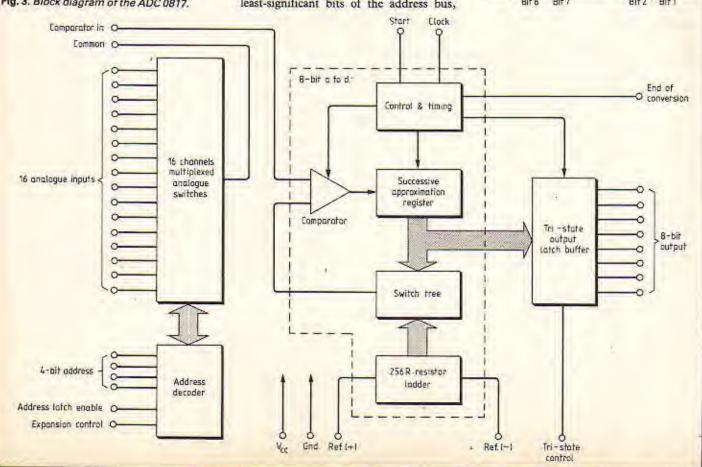
The block diagram in Fig. 3 shows the main features of the system. An address decoder, normally driven from the four least-significant bits of the address bus,

selects the analogue channel in use. The decoder can be enabled and the conversion started by the rising and falling edges of a single pulse. The appropriate analogue signal is switched through, with an intervening common stage of signal processing or filtering if required, and a chain of resistors across a reference voltage is scanned with a successive approximation register until a match is found between its output and the signal being measured. The mostsignificant bit is tested first and accepted or rejected after comparison with the unknown. Each further bit of the eight is similarly tested so that the cumulation voltage becomes closer and closer to the unknown voltage. Each conversion takes exactly eight test cycles regardless of the value of the unknown, which provides fast and precise timing relationships suitable for multi-channel systems.

On completion of the conversion, a

Fig. 4. Internal ladder network of a ZN425E. The ladder can be powered by an internal or external reference.





pulse is generated which can be used by the microprocessor to activate tri-state controls and give the a-to-d latched outputs access to the data bus. When data for one channel is collected and stored, the processor is ready to provide the address of the following channel.

Some simplification is possible with Basic programs which run sufficiently slowly for the conversion process to finish naturally before the start of the next instruction.

D-to-a converter

The ZN425 is a well established device which lacks the sophistication of some more recent devices, but is still worth using in general applications. Additional gating and latching is required for use with a microprocessor and at present only the d-to-a capability is used. The data bus is latched to the converter and an internal R-2R ladder network provides a proportional output as shown in Fig. 4. An internal or external reference may be used to drive the ladder, but the internal counter provided for a-to-d applications is not used. The reference may be a variable voltage if required, normally in the 0 to 5V range, and a small negative reference voltage (<0.5V) may be used although this is not covered by the specification. Further details of the ZN425 can be found in reference 4.

Processor interface

The 6522 was designed to interface directly with the 6500 series of microprocessors and therefore presents no difficulties when used with the systems mentioned in part one. Fig. 5 shows the lines used by the v.i.a., namely;

Data bus	Eight bidirectional wires used to transfer data be- tween the v.i.a. and c.p.u.
R/W	A control line used by the c.p.u. to define the direction of data transfer. If the R/W is low, data is transferred from the c.p.u. to the v.i.a., i.e. a write operation. If the R/W is high,
Reset	data is read by the c.p.u. The reset signal clears all internal registers except T1, T2 and the shift regis-
0 ₂ clock	ter. 02 acts as a time base for the various timers, shift re-
Register select	gisters etc. in the i.cs. The four Register select lines are normally connec- ted to the four least-signifi- cant address-bus lines to give the processor access to
Chip select	the 16 registers. The selected register can only be accessed when the chip select pin, CS2, is held low. This signal is usually derived from the address decode circuit which places the i.c. in the memory map.

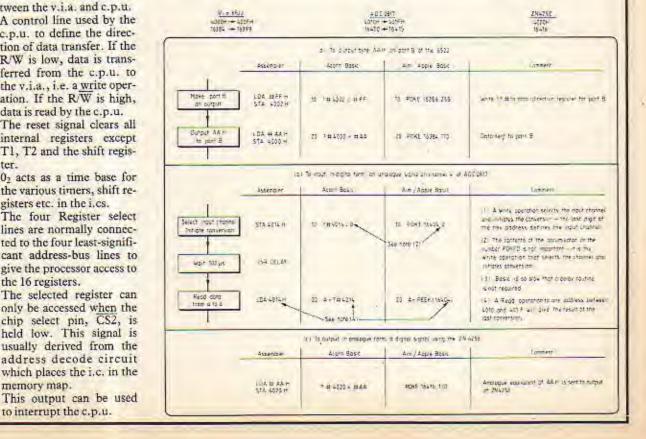
request (IRQ) to interrupt the c.p.u.

Interrupt

Table 1. V.i.a. registers and functions. L=0.4V, H=2.2V

Re	giste	rsele	ct		A 100.0000				
RS3	RS2	RS1	RSO	Address	Addressed register	R⁄W≖L	R∕W≔H	Notes	
L	L	L	t	D	posterior.	Write ORB clear CB2 and CB1 interrupt flags (IFR3 and IFR4)	Read IRB clear CB2 and CB1 interrupt flags (IFR3 and IFR4)	1=high, 0=low	
L	L	L	H	1	100	Write CRA clear CA2 and CA1 interrupt flags (IFRO and IFR1)	Read IRA clear CAZ and CA1 interrupt flags (IFR0 and IFR1)	1=high, 0=low Controls CA2 handshake	
L	i	н	I.	2	DORB	Write DDRB	Read DDRB	0=input, 1=output	
L	L	Н	H	3	DDRA	Write DDRA	Read DDRA	0=input, 1=output	
L	H	t	L	4	TI	Write T1L-L	Read T1C-L clear T1 interrupt flag (IFR6)		
L	н	L	Н	5	π	Write T1L-H & T1C-H transfer T1L-L to T1C-L clear T1 interrupt flag (IFR6) initiate T1 counting	Read T1C-H		
L	H	H	L	6	TI	Write T1L-L	Read T1L-L		
ĩ	Н	H	н	7	TI	Write T1L-H clear T1 interrupt flag (IFR6)	Read T1L-H		
н	ι	ι	L	8	T2	Write T2L-L	Read T2C-L clear T2 interrupt flag (IFR5)		
н	Ļ	t	Н	.9	T2.	Write T2C-H transfer T2L-L to T2C-L clear T2 interrupt flag (IFRS) initiate T2 counting	Read T2C-H		
H	t	н	L	A	SA	Write SR clear SR interrupt flag (IFR2)	Read SR clear SR interrupt flag (IFR2)		
H	L	н	H	8	ACR	Write ACR	Read ACR		
H	H	L	L	C	PCR	Write PCR	Read PCR		
H	Н	L	Н	D	IFR	Write IFR	Read IFR	1=detected, 0=not detected	
H	н	H	L	E	IER	Write IER	Read IER	1=enable, 0=disable	
H	Н	H	H	F	IRA/ORA	Write ORA clear CA2 and CA1 interrupt flags (IFR0 and IFR1)	Read IRA clear CA2 and CA1 interrupt flags (IFR0 and IFR1)	1 = high, 0 = low no effect on CAZ handshake	

Table 2. Driving the Interface i.cs in machine code and Basic. In these examples the address decode circuit has been adjusted so that each i.c. occupies the location shown.



OV

Table 2(a) illustrates how the v.i.a. can be used to output a byte in parallel form on port B. The v.i.a. registers are treated as memory locations by the programmer and can be read or written to in assembly language using LDA or STA instructions, or in Basic using Peek and Poke instructions.

The ADC 0817 has been designed to be compatible with a wide range of microprocessors and Fig. 6 shows that most of the signals used by the converter can be taken directly from the 6502.

Data bus

Channel select The four least-significant address lines can be used to select each of the sixteen input channels.

The R/W line is not used directly but is gated with the 02 clock to produce the Not Read Data Strobe, NRDS, and the Not

8-bit data bus R/W Reset To c.p.u. 6522 \$2 clock VID Register select A0-43 Chip select LS2 IRQ

Write Data Strobe, NWDS, NRDS and NWDS only go to zero during the positive part of 02 in a Read or Write cycle respectively as shown in Fig. 7. Fig. 6 shows how a Write operation to the i.c. activates the NWDS and creates the necessary transitions on the address-latch enable pin and initiate-conversion pin to perform the following tasks. Select the input channel from the address currently on the four least-significant address lines. Initiate an analogue-to-digital conversion. After a 100µs delay, a Read operation activates the NRDS, enabling the tri-state output and placing the digital signal on the data bus. Table 2(b) shows the programming instructions used to drive the i.c. A Write

instruction, STA or Poke, is used to define the input channel and initiate the conversion. After a delay a Read instruction, LDA or Peek, obtains the digital informa-

The ZN425E is not directly compatible with a microprocessor and must be used with the 74LS373 which latches transient data from the processor and provides the 425E converter with a continuous digital input. The latch is memory mapped and enabled by a chip-select signal from the address decode circuit, see Fig. 8. This ensures that the latch captures stable data on the bus during the positive part of the 02 clock. Table 2(c) shows how the 425E is used in Basic and assembly language.

Joutput E

port no. 13

Ref. out +5V 74LS373 ZN425E Refin d to a latch Data bus Analogue output Latch timing CS Fig. 5. V.i.a. connections to the 6502, Latch enable Fig. 6. A-to-d input/output connections and timing diagrams. Common Comparator Fig. 8. Enable signal and latch timing for out the d-to-a converter. Fig. 7. Generating NWDS and NRDS signals for the ADC 0817. TRO EOC Address bus Exp 40 +5V NRDS RIW OV Output F CS NWDS Start To ALE NWOS r pu 16 analogue ADC 0817 NWDS inputs Data bus + ref. Read cycle RIW Write cycle select input channel - initiate conversion 22 NROS NW05 NWDS Write cycle TS iarch address initiate conversion RIW ALE / Start NRDS Read cycle enable tri-state - read data NWDS NRUS References Rockwell data sheet, no. 29000D47. CS Rockwell, R6500 hardware manual, no. 29650 N. 31, p. 6-1. 2. National Semiconductor data book, Ferranti data converters, application re-Dutput enable

Accurate sine-waves

Analogue implementation of the Darwood accurate sine-wave oscillator algorithm

by D. H. Follett

In response to Mr Darwood's
'Accurate sine-wave oscillator' article
in the June'81 issue of Wireless
World, the author shows here that the
digital implementation used to
generate accurate sine and cosine
functions can be replaced by simple
analogue circuits. A prototype circuit
operated over three decades with
±1dB amplitude variation, less than 1°
error between the quadrature outputs
and around 1% or less distortion. The
circuit requires only four quad-i.cs.

The algorithm recently described by N. Darwood for generating sine and cosine functions with digital implementation may also be produced by analogue means, as will be shown. The circuit is really a form of recursive digital filter but I am unrepentant in calling it an analogue implementation since no digitization in the proper sense occurs.

The prototype operated over three decades of frequency with amplitude variations of ±1dB, distortion about 1% or less, and phase error between outputs less than 1°. Only four cheap quad i.cs are required, although Fig. 2 shows six i.cs, since the four dual op-amps can be replaced by two quad op-amps such as the LF347.

Principle

Referring to the original article for fuller explanation, each new value of sinn is computed from the previous value by adding a fraction ω of cosn;

 $\sin(n+\omega) = \sin n + \omega \cos n$

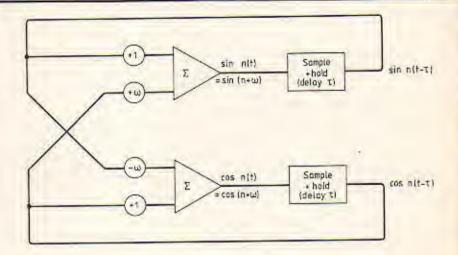
Note that ω does not have its usual significance. If we write $\sin(n+\omega)$ as $\sin n(t)$, the value of $\sin n$ at time t, and $\sin n$ as $\sin n(t-\tau)$, the value at time τ earlier, then

 $\sin n(t) = \sin n(t-\tau) + \omega \cos n(t-\tau)$

Similarly,

 $\cos n(t) = \cos n(t-\tau) - \omega \sin n(t-\tau)$

These equations are applied as shown in the block diagram, Fig. 1. The value of sinn is sampled and held so that the output of the sample and hold circuit is effectively delayed by the sampling interval τ and represents the value of $\sin n(t-\tau)$. To this is added the fraction to of the cos function to generate the new value of the sine function, $\sin(n)t$. A similar process is used for $\cos n$.



Referring again to Mr Darwood's article, the sine and cosine outputs are synthesized with $2\pi/\omega$ steps per cycle so that the output frequency is $2\pi/\omega$ times less than the sample clock frequency.

Implementation

The circuit was designed to operate in the audio-frequency range with values as shown in Fig.2. During the first half of each clock cycle (Q high) the values of sin and cos are transferred to the first pair of hold capacitors while the previous values are held on the second pair. In the second half cycle the values are transferred to the second pair of capacitors. This avoids having to use very short sample times and ensures that loops are never closed while settling. The 100kΩ resistors determine the fraction ω; the optimum fraction seems to be about one-tenth, giving about 60 steps per cycle. Although the circuit will run with 400 steps per cycle, distortion occurs because circuit errors become comparable with the step size. More accurate sample-and-hold i.cs and higher accuracy resistors will decrease circuit errors.

The diode-resistor networks around A_2 and A_6 provide a small degree of nonlinearity sufficient to stabilize the oscillation amplitude. If only one output is required and exact phase quadrature thus unimportant, one network and the associated preset can be omitted, leaving only the $10k\Omega$ feedback resistor.

Setting up

Initially, the $1k\Omega$ presets should be set to zero to prevent oscillation and the null offsets adjusted. The presets should then be advanced until oscillation occurs and then adjusted for phase quadrature. The output amplitudes should be about 4 to 5V

Fig. 1. Block diagram illustrating application of the equations for values of sin n(t) and cos n(t)

peak-to-peak. Finally, the null offsets may need readjusting. The output frequency is not critical during the adjustments, but should be between 50 and 5,000Hz.

Results

Figure 3 shows oscillograms for frequencies between 5Hz and 16kHz obtained by varying only the clock frequency. Single time-base sweeps were used for all but the 16kHz frequency as the steps are not, in general, synchronized with the output. In Fig. 4(a), the 500Hz signal is expanded to show the steps more clearly, while Figs 4(b) and (c) show Lissajous figures resulting from x-y display of the two outputs to illustrate the quadrature accuracy obtainable between 5Hz (b) and 5kHz (c).

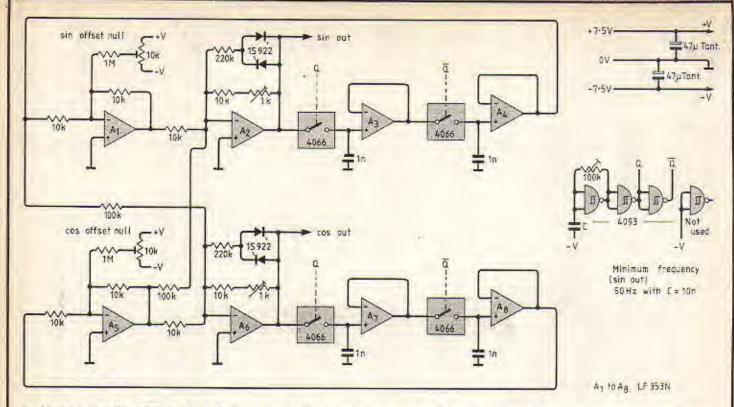
The upper frequency for constant amplitude is about 16kHz but frequencies lower than 5Hz can be obtained by increasing the 1nF hold capacitors proportionally. These capacitors must of course be polystyrene types, or similar, to minimize dielectric soaking effects.

If the clock is replaced by a voltage controlled oscillator the circuit can also be used as a sweep oscillator.

Comparisons

Out of interest, two other oscillators based on recursive filters were compared to the circuit described here using the same building blocks.

The first used direct implementation of the second-order differential for a seriestuned circuit (equivalent to the state-variable filter in band-pass mode). This circuit



used two op-amps fewer but was limited to about 30 steps per cycle, as second order terms make circuit errors more critical.

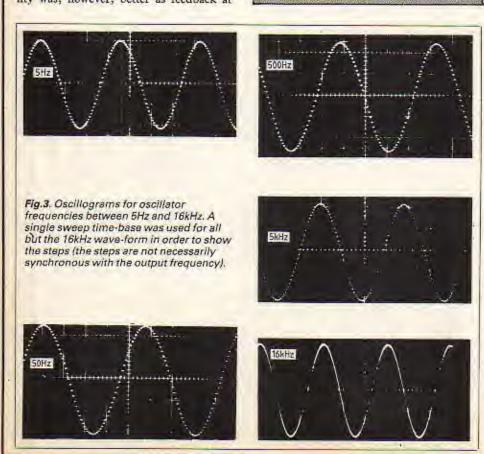
Phase-shift oscillators using three or four cascaded single-pole filters were also tried. These oscillators were more docile than those previously described, but four sections were required to obtain quadrature outputs and almost twice the component count of the circuit described here gave an inferior performance. D.c. stability was, however, better as feedback at

d.c. is negative and thus reduces offsets.

The circuit described here is sensitive to offsets because of positive feedback at d.c., so offset null adjustment is included.

Reference
1. N. Darwood, "Accurate sine-wave oscillator', Wireless World, June 1981, pp 69-78.

Fig.2. Circuit diagram of the oscillator and clock. Op-amps A₁ to A₈ were four LF353N i.cs in the prototype but they can be replaced by, say, two LF347 quad i.cs if required. These op-amps have j.f.e.t. inputs.



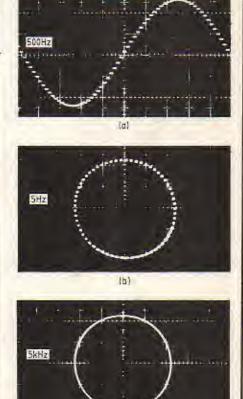


Fig.4. (a) is the 500Hz sweep expanded to show the steps more clearly. (b) shows a Lissajous figure resulting from the two oscillator outputs at 5Hz, and (c) is as (b), but at a frequency of 5kHz.

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11°C. 12°C to #50°C, 52°C swithers.

0°C to #50°C, 52°C, 80°C, 81°C to 28°C swithers.

0°C to #50°C, 52°C, 81°C swith alkaling battery), 52°C, 81°C, 81°C to #60°C (with alkaling battery), 52°C, 81°C, 81°C, 12°C to pricely ± [0.01% of reading # 0.05°C] per "C, including sole junction 50°C, 90°C, including 10°C, 10°C,

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News of the Month



Subscription tv by cable

Cables were first used for broadcast distribution in the 1920's and were extended and updated to include television, two and then three channel ty. The cables could get the broadcasts to areas where the reception was poor or non-existent. Since then, improvements and additions to the broadcasting network have made the need for cable distribution redundant and the subscribers to the cable services were reducing in numbers. However the cable networks exist, and Rediffusion, amongst others, have been pressing the Government to be allowed to institute subscription television services. Wireless World reported the granting of licences by the Home Office to a number of pilot schemes in the May issue, and the first to commence transmission, on Wednesday the 9th September, was the Rediffusion 'Starview'. Starview is being transmitted in five areas; Burnley, Hull, Pontypridd, Reading and Tunbridge Wells.

At the time of the launch, there were some 3,000 subscribers to Starview in the selected areas. Another 19,000 were subscribers to the public broadcast network and there was a potential audience of 56,000 houses which could be easily connected to the cables.

Rediffusion research has indicated that what the public really wanted was recent feature films. Sixteen films had been selected for broadcasting in September, with a further ten for October. Two films are shown each evening with an extra late-night film on Friday and Saturday and an afternoon 'matinee' performance on Sunday.

Rediffusion were surprised by the high distribution fees demanded by the Motion Picture Exporter Association of America. To break even, it is estimated that a subscription fee could be as much as £12 each month. Rediffusion have decided to charge the full rate, £11.95, only in Reading; in Burnley and Hull they are charging only £7.95.

Technical details of the Starview service are described elsewhere in this issue.

S.s.b. mobile radio still promising

The claim made two years ago by Pye Telecommunications Ltd that, to create more channels for land mobile radio, single-sideband operation at v.h.f. is the most promising technique (June 1979 issue p. 95) has now been given qualified support by some recent Home Office trials. The narrow-band system actually tested, in comparison with others, was 3,5,b, with a channel spacing of only 5kHz. The testing was a subjective evaluation of the quality of calls and it was done by operators of a typical user of private mobile redio, Bell Fruit (UK) Ltd. The other two systems compared with the 5kHz s.s.b. were 25kHz and 12.5kHz channel spacing using f.m. It was intended to use 12.5kHz a.m. for comparison as well, but this in fact will be done later.



When Racal-Decca bought some digital displays from Hewlett-Packard for use in radar equipment, the dials incorporated in the displays were manufactured by Chequers (UK) Ltd in London, some 15 miles away from the Racal-Decca Marine Radar plant in New Malden, Surrey. To cover those 15 miles they had in fact travelled 10,000 miles across the Atlantic and back. The dials have an outer ring of 100 i.e. ds to give an analogue readout with three seven-segment i.e.d. digits in the centre, Because the printed dial has to match up with the i.e.ds, the diodes are positioned and the printing registered to within 0.003in.

According to D. M. Barnes of the Home Office's Directorate of Radio Technology: "The results have shown that from a user's assessment 5kHz s.s.b. equipment could be used to provide a land mobile radio system without any loss in quality or intelligibility when compared with 12.5kHz f.m. equipment. Furthermore, in many situations the quality of the s.s.b. equipment would be better than that of existing 12.5kHz f.m. equipment. However, it has also been shown that in general 25kHz f.m. equipment would provide a higher quality service. The use of SkHz s.s.b. could theoretically provide an acceptable service with 5 times or 2.5 times as many channels in a given block of spectrum than 25 or 12.5kHz f.m. equipment respectively. However, further work is required on the frequency re-use characteristics of the different systems before a final conclusion can be reached"

This report comes from a paper delivered by Mr Barnes at the IERE's Clerk Maxwell Commemorative Conference on "Radio Receivers and Associated Systems" at Leeds in July. The tests were conducted over a six-week period on 21 mobiles - seven of each type with a base station of three transmitters in Contral London. Peak envelope powers of the three different systems were made equal: 10 watts p.e.p. for the mobiles and 25 watts e.r.p. for the transmitters. Frequencies were in the region of 160MHz for the mobiles and 165MHz for the transmitters. The f.m. transceivers were standard commercial land mobile radio equipments. The s.s.b. sets, produced by Pye Telecommunications, were of the single-sideband plus pilot carrier type (see June 1979 issue). The pilot carrier level was set at -12dB with respect to the peak envelope power. Details of these sets were presented by R. Wells of Pye in a companion paper at the above IERE conference.

Results were recorded for both stationary and moving vehicles and also using three areas of different field strengths between about 3uV/m and 100uV/m. Altogether nearly 3000 results were obtained, divided more or less equally

between the three systems. Subjective rating of call quality by the operators was given in terms of a CCIR five-point scale ranging from 5 (excellent) down to 1 (unusable). In the results the 25kHz f.m. equipment achieved a higher percentage of grade 5 ratings than the other two systems, but the s.s.b. equipment obtained a higher percentage of grade 5 ratings than the 12.5kHz f.m. equipment. However, when grade 4 and grade 5 ratings were combined the s.s.b. and 12.5kHz f.m. had the same percentage ratings. The paper comments: "This tends to imply that on an overall basis 25kHz f.m. would provide the best quality service but s.s.b. equipment would provide a similar or better quality than 12.5kHz f.m." Results obtained for stationary and moving vehicles in a given area were similar.

When the results were considered on an area basis "in the high field strength area the s.s.b. equipment achieved a greater percentage of grade 5 ratings than either of the two f.m. systems. However, in the medium and low field strength areas the 25kHz f.m. achieved the highest percentage of grade 5 results with the s.s.b. achieving more than the 12.5kHz f.m."

Further work, according to the paper, will aim to discover the distance at which a given s.s.b. channel frequency could be re-used without causing interference. There will also be tests to establish the adjacent channel performance of the different types of equipment.

• Pye Telecommunications have experimented with adapting one of their v.h.f/a.m. hand portable (walkie-talkie) sets, the P5001, for s.s.b. operation with a 5kHz channel spacing. For this a remperature-compensated crystal oscillator and i.f. crystal filters had to be specially made. According to a further paper by R. W. Wells at the IERE conference, the results did not fully meet operational requirements but they did show that "v.h.f. s.s.b. is indeed feasible with hand-portable equipment". There was a large cost penalty with the circuits used and this indicated a need for much more work before such a hand portable is a saleable reality.

BBC graphics

Viewers will have noticed the change to the titles for BBC news. What they won't realise is that the striped patterns and figures are generated electronically. ANT (animated news titles) came into service on the 7th September, only one month after it had been suggested that it may be possible. Priority was given to the graphic design for the main 9 o'clock news. BBC engineers were able to demonstrate this sequence within a week of starting the project. After the details of the other sequences had been produced it took a further three weeks to imple-

The hardware for the system was based on that used for the BBC2 electronic clock and the animated Open University logo. The equipment needed modification to cater for multiple captions, the generation of 'key' signals so that pictures may be incorporated into the sequences, and for the definition of certain

areas in the displays.

The software, which controls the commands and the sequences of the animations, uses only Ikbyte of memory for the programme. It requires another 6kbytes for the data. The data is stored in tables for each step of animation with a look-up table to arrange the actual sequence. Each data table defines only those parts which need to be changed, assuming a current state. This avoids the need to define the whole screen for each step. The microprocessor control is triggered 25 times a second by the display controller and the whole sequence can be started automatically

In a programme of work, supported by the Department of Industry, BBC research department has produced equipment to be used to study enhancements to the British teletext

One of the early uses of the equipment has been to produce a teletext decoder capable of displaying the normal pages as they are broadcast now, but with a better quality of character generation than is found at present. When the teletext specification was written, five years ago, the shape and style of characters were deliberately left undefined. This was so that as equipment improved, manufacturers could offer a choice of type style.

A photograph of a transmitted Ceefax page using the decoding equipment developed by the BBC Research department to study enhancements to teletext.

Spare signalling capacity to control a change of character set was also provided. When new character generators came into use, the decoders would still be compatible with existing transmissions, and existing decoders will continue to function normally.

The BBC equipment is being used to investigate coding methods for high-quality teletext. graphics, using the techniques known as 'redefinable characters', 'alphageometric' and 'alphaphotographic' coding. It has already been used to display high quality still pictures at the IEEE Chicago Conference, and at the Berlin Radio Show.



Computers may Dial to each other

The British Standards Institution has published the first Part of DD 75 The structure and representation of data for interchange at the application level (DIAL), a major Draft for Development describing a new system of data interchange that could lead to massive economies for users in industrial, commercial and public sectors. Entitled Part I Recommendations for syntax and basic principles, the Draft is designed to achieve direct camputer-to-computer intercommunication and provides the basis for the first 'language' in the world for general applications, regardless of differences in the equipment used.

At present, communications such as invoices and purchase orders start off on one computer and certainly end up on another in a different organization. It's the bit in between that causes problems. Take, for example, a company which uses a computer to control stocks and order their replenishment. Normally, the order is printed out, put into an envelope and mailed (via a postal service now much more expensive and slower than in pre-computer days), sorted in the recipient's mail room, part processed clerically and then, ultimately, keyed into the

organization's computer system.

Note the need for clerical pre-processing and key-entry operations! These happen to be two of the most expensive and error-prone tasks assoclated with computer systems. And at every stage of this drawn-out programme of events, the order sits waiting for attention. In the circumstances it is hardly surprising that a processing period of three days is considered to be remarkably fast, three weeks is probably typical and three months not unknown. In other words, a slow, tedious and remarkably inefficient process which stems largely from the lack of the

necessary standards that would permit more effective communication.

The major obstacle to direct inter-computer links has always been the absence of a common data language and, hence, incompatibility in the software used by the sender and the receiver, not to mention anomalies in the equipment (eg flexible discs at one end of the line - magnetic tape at the other). Where only one partner is involved, of course, it is not difficult to write programmes that will effect the necessary conversion. But there can be few suppliers with only one customer, or buyers with a single supplier. Nor is it feasible to accommodate additional organizations by writing suites of individual programmes. Quite apart from the prohibitive cost, there are just not enough analysts and programmers available to cope with interchange on this basis.

Obviously, the long-term solution is to adopt standard messages using standard software. Some industries with particularly urgent needs have, in fact, already developed their own standards, notably those now employed in banking and airline computer systems. Currently, some 16 per cent of all clearing bank transactions and probably well over 90 per cent of airline com-munications are dealt with in this way. Not every group of interests, however, has the necessary expertise to devise independent standards, especially where messages are required to cross sector boundaries.

BSI's new DIAL system aims to provide a common facility to all branches of industry, commerce and administration having access to computer services. Part 1 of the Draft describes a general-purpose language for the interchange of machine-readable data with a minimum of

negotiation or agreement. It contains:

(1) A basic grammar, suitably precise for computer processing, with extensions to meet specific applications.

General recommendations for the representation of frequently-occurring categories of

(3) Administrative arrangements for data interchange.

DIAL is intended for use with any interchange medium including:

- (a) Telecommunication networks providing simultaneous transmission
- (b) Telecommunications networks using a store-and-forward service
- The transfer of physical media such as magnetic tape

The language is independent of the applications and equipment used and has a structure that permits the necessary degree of manual processing to ensure operational integrity and flexibility. In the interests of compatibility it uses a set of characters (letter, digits and symbols) which are restricted to those available on virtually every computer, so that messages can be sent to anyone regardless of the type and make of the equipment at the receiving end.

Another important asset is that DIAL is compatible (most of it identical) with the standards produced for international trade procedures by SITPRO (the Board for the Simplification of International Trade Procedures) which are approved by the United Nations. Thus, although DIAL will become a British Standard for internal UK use it is compatible with international equivalents - an important consideration for organizations operating both at home and over-

Broadcasting "radio data"

Details of the BBC's experimental broadcasting of digital signals for programme labelling, called "radio data" (News, September issue), were revealed by Dr S. R. Ely, BBC Research Department, at a recent IERE conference on "Radio receivers and associated systems" at Leeds. (And further information became available in a BBC Research Department report, RD 1981/4 "V.h.f. radio-data: experimental BBC transmissions" June 1981.) The system, developed jointly by the BBC and Televerket of Sweden, has been used on three BBC v.h.f. sound transmitters in the London area, Radio 2, Radio 4 and Radio London, in experiments running since April this year.

The digital data is conveyed on a 57kHz subcarrier which is phase-locked to the third harmonic of the 19kHz pilot tone of the stereo transmission. Frequency tolerance of this subcarrier during stereo broadcasts is ±6Hz. It is added to the stereo multiplex signal (or a monophonic signal) at the input to the v.h.f./f.m. transmitter. Peak deviation of the main carrier due to the 57kHz subcarrier is

about ±2.25kHz.

This subcarrier is double-sideband suppressed-carrier, amplitude modulated by the digital data, which has the form of a bi-phase data signal with a bit rate of 1187.5 bit/s. (The method of modulation may be considered as a form of two-phase p.s.k. with a phase deviation of ±90°.) The bit rate is in fact, derived by dividing the transmitted subcarrier frequency by 48. But this division ratio may occasionally be altered to 50 or 46, to facilitate phasing of the transmitted code words, in such a way as to insert or delete one 57kHz cycle in each half of the bi-phase symbol corresponding to a data bit. Data is arranged in 114-bit blocks, giving 625 blocks per minute.

About 35% of the available data channel capacity is being used at present to transmit the most likely types of message required, including the network name (e.g. BBC R4 - see September News picture) in ASCII code for display purposes. The remaining 65% of the capacity is packed with dummy data from a pseudo-ran-

dom binary sequence generator.

Currently these radio data transmissions are being received by special BBC v.h.f. receivers containing circuitry for demodulating the 57kHz d.s.b.s.c. a.m. signal and decoding the bi-phase digital symbols. The first operation is to recover the 57kHz subcarrier from the suppressed carrier d.s.b. radio data signal. This is then used locally in a synchronous demodulator to recover the digital modulation at 1187.5 bit/s. Before the synchronous demodulator, though, a 57kHz bandpass filter is inserted to

C.b. legalized

November 2 is the date set by the Home Office for the start of legal c.b. operation in the UK, on the 27MHz and 934MHz bands, using frequency modulation. Licences costing £10 will allow operators to use up to three sets.

The relevant specifications are set out in Home Office publications MPT1320 (27MHz; and MPT1321 (934MHz), obtainable from

HMSO at £1.95.

Within a day of the Home Office announce-ment, Wireless World has already received a protest from the Citizens' Band Association, pointing out that the choice of frequencies means that the UK and European systems are incompatible, and claiming that the new standard will render aircraft more vulnerable to interference than the illegal system.

attenuate the comparatively large amplitude sound signal components in the multiplex sig-

The stream of bi-phase digital data is then recovered by a symbol decoder described as an integrate and dump decoder*. For decoding purposes the 1187.5 bit/s rate must be available locally as a clocksignal. This is obtained by dividing down the recovered 57kHz subcarrier by the 48 divisor mentioned above and correctly phasing the resulting 1187,5 bit/s clock relative to the zero-crossings of the recovered bi-phase coded data stream.

Last year this BBC/Televerket system, together with three other similar ones, from France, Holland and Finland, were field tested in the Bern region of Switzerland, using a Swiss PTT broadcast transmitter in the mountains. In these conditions, all four systems were found to suffer from a high mean bit-error-rate of 10 to 20%. The principal source of errors was thought to be multipath propagation causing programme signals to intrude into the data channels. However, with two of the systems using a high frequency subcarrier (BBC/Televerket on 57kHz and TDF (France) on 58.3314kHz), 70% of data blocks were received without error, as against two systems using lower subcarriers (NOS (Holland) on 16.625kHz and YLE (Finland) on 19.6kHz) which gave only 10% and 27% respectively of data blocks received error-

A firm specification for a Western European standardized radio data system will eventually be decided by the EBU.

* French, R.C. "Error performance of p.s.k. and f.f.s.k. subcarrier data demodulators," The Radio and Electronic Engineer 46, 11, pp. 543-548, 1976. Also Norton, J.J. "Drop your costs but not your bits with a Manchester-data decoder", Electronic Design, 27, 15, pp. 110-116, 1979.

Two-way wrist radio by year 2000

A two-way wrist radio will become a reality by the year 2000 as a result of communications satellite developments, according to the Lock-

heed Missiles & Space Company.

Lockheed engineers in California are developing a 180-foot demonstration version of a communications satellite antenna suitable for transport on the Space Shuttle. Once in space, such an antenna would be unfurled and look much like a huge umbrella. It would act as a highly sensitive receiver of low-power signals from Earth which it would re-broadcast at high levels to designated areas. Thus, a small, lowpower radio - even worn on the wrist - using a simple antenna, could transmit voice using the satellite as a signal booster and switchboard that would beam transmissions to selected parts of the earth, such as remote areas without telephone lines.

Other potential uses for the advanced antenna are radiometry - the measuring of tempera-tures, snowpack, moisture content on Earth observations of great value to agriculture; radio astronomy, and radio telescope applications.

The antenna with its communication satellite could be launched by the Space Shuttle into a geosynchronous orbit 22,300 miles above the Earth's equator. On site, the antenna would be deployed automatically.

Present communications satellites used in

Engineers study social implications of technology

Electrical and electronics engineers in the USA are to investigate "the impact of technology on society, including both positive and negative effects, the impact of society on the engineering profession, the history of the societal aspects of electro-technology, and professional, social and economic responsibility in the practice of engineering and its related technology"

These are the stated interests of a new group, the Society on the Social Implications of Technology, now being set up by the IEEE in New York. It will publish a journal, the IEEE Technology and Society Magazine, the first Issue of which will appear in early 1982. The Society's administrative committee will consist of representatives from each of the IEEE's seven technical divisions together with its own officers and elected representatives. Although it will be interested in ethics and will publish articles on the subject, the new society will not have sole responsibility for developing ethical standards within the IEEE. Further information can be obtained from Robert J. Bogumil, 530 W. 112th St., New York, N.Y. 10025, USA.

Two UK organizations recently set up to study this field are the Technical Change Centre. (News, April issue) and the New Technology Research Group at Southampton University (May issue, p.53).

commercial communications, including television, require elaborate antenna systems on Earth. The antenna/satellite system envisaged by Lockheed - because of its great sensitivity and beam-aiming ability - would enable users to communicate nationwide using simple transmitter-receiver units.

Simulator aids reactor safety

An Advanced Gas-cooled Reactor (AGR) training simulator has been ordered from Marconi Space and Defence Systems (MSDS) to assist in training operators at Hunterston 'B' nuclear power station in Scotland.

The order, which comes from the South of Scotland Electricity Board, is valued at approximately £3 million and results from feasibility studies carried out by MSDS since 1973 for both the SSEB and the Central Electricity Gen-

erating Board.

The simulator, which will be the first in the world to provide total realism in terms of accuracy and speed in a nuclear power station control room, is to be installed at the Hunterston 'B' site by mid-1983.

The principles used in the design of the AGR simulator can be used equally for a pressurized water reactor (PWR). The PWR is based on American technology and is similar to that involved in the accident at the Three Mile Island power station, Harrisburg, Pennsylvania two years ago. Marconi hopes to gain significant export orders as well as further orders from the UK in support of the universal drive to maintain high training standards for operators in nuclear

LaserVision delayed

When video disc systems were first introduced into the United States, the suppliers were swamped with demands for more and more discs and could not produce them quickly enough. This led to disappointments and disillusion amongst the customers. This is the principal reason why Philips have decided to delay the launch of their LaserVision system in the UK. Originally planned for Autumn 1981, Philips now say that they will "launch in the UK when we have sufficient numbers of discs to support our initial catalogue of titles"

Jimmy Dunkley, the divisional director of LaserVision, admitted that they had some production difficulties at their Blackburn disc pressing plant which he described, rather coyly, as "progressing up the learning curve". In order to meet the higher level of demand for discs which predictions indicate, additional plant is being installed to increase the pressing capacity. Player production has commenced in two factories in Europe to supply the needs of the UK

launch.

Philips have also revealed some of their plans for uses of the disc system. Of course it is highly suitable for feature films, but it may also be used, for example to store the contents of a reference book. A large illustrated encyclopacdia can be stored on the 54,000 frames available on each side of a disc and any particular frame can be found and then displayed on the tv screen. Philips are directing their attention to users of instructional, educational and business communication programmes.

Technical details of LaserVision and other disc systems were published in our September

Microcomputers in schools—free

An enterprising businessman in Berkshire, Mr Len Lewis of Audio Systems Components Ltd. in Theale, has come to an arrangement with the local school whereby he will provide ten Commodore Pet microcomputers for the free use of the school. He gets in exchange the classroom space to hold evening classes for courses in computing for adults.

Mr Lewis told us that his project was not entirely philanthropic since he hoped to break even on the basis of well-attended classes, "but I like to think that any profit will be all the better for knowing that the school children are benefit-



A LaserVision disc at a visual inspection station at the Blackburn disc-pressing plant. Discs are produced under 'clean room' conditions like those needed for integrated circuit production.

ing too". He plans to plough back some of the profits from the evening classes by purchasing peripherals, to finance a users' group and to organise a project team to develop educational software. He also told us that he thought of the scheme after reading our report of the Government's Microcomputers in Schools scheme in the June 1981 issue of Wireless World.

Engineering Council chairman

Electronics engineers will note the fact that the chairman of the new Engineering Council is to be Sir Kenneth Corfield, for, although Sir Kenneth is by training a mechanical engineer, he is of course chairman and chief executive of Standard Telephones and Cables Ltd, the ITT subsidiary. The Engineering Council, which at the time of writing is about to receive a Royal Char-

ter, is the Government's response to the proposals of the much debated Finniston report on the engineering profession. It is widely seen as a watered-down, and cheaper, version of what Finniston wanted (for example, the chairman will be unpaid and part-time) with little real power to make much needed changes, Finniston called for an Engineering Authority that would be a statutory body, funded by the government and with members appointed by the Secretary of State for Industry; it would have been accountable to the government for the use of its statutory powers and for money voted to it by Parliament.

The objects of the new Council will be "to advance education in, and to promote the science and practice of, engineering for the public benefit and thereby to promote industry and commerce" in the UK. Apart from this and other similarly vaguely stated duties, the Council will have the more specific task of forming a register of professional engineers, technician engineers and engineering technicians. Since the existing Engineers' Registration Board is run by the Council of Engineering Institutions, it would appear that the CEI will have to hand over this register - and also its power to award the title "Chartered Engineer" to the new body. But these transfers will depend on the agreement of the CEI, in the form of a two-thirds majority at an extraordinary general meeting.

High street battle of personal computers

Two items of news which affect the microcomputer came out at about the same time. One was that the mainframe computer manufacturer, IBM, is to market a micro. There have been many analyses of the impact this will have. The Venture Development Corporation in America, who produce many market analyses, have published a study which indicates that by "placing its seal of approval on low end computers, IBM will spark growth in the market for both personal and small business computers. It will be some time, though, before IBM captures a significant share of the personal computer market. IBM will have to strengthen its position with regard to distribution channels and applications software before Radio Shack [Tandy] and Apple will have anything to worry about". VDC also points out that the [American] home user

thinks that games are of the first importance and that users would not buy a home computer that didn't have Space Invaders. IBM are selling their computer through the Sears Roebuck mail order catalogue and through the US Computerland chain of retail stores.

Another analysis from Gnostics Concept gives a different answer. They suggest that the basic version of the IBM personal computer has a higher specification and a lower price than the Apple II and the full system is also better and cheaper than the Apple III. So the battle has started but at present IBM have no plans to market outside North America.

The UK domestic market is also hotting up, however, with the news that the Sinclair ZX81 is to be sold in selected High Street branches of

W. H. Smith & Son. Boots, Argos and Rumbelows are all planning to test-market the Texas Instruments' TI 99/4. Boots and Smiths are also planning to sell the Commodore VIC 20 computer, but at present there are enough to go round and Commodore will be selling only through computer shops. The VIC 20 has been beset by delays in production and by a lack of software packages to go with it. It is thought that the machine will be launched towards the end of the year.

Another 'dark horse' waiting on the sidelines is the BBC microcomputer which has not been released at the time of writing but offers a high specification at a low price. The BBC plans are to sell through mail order only, but the proliferation of high street outlets might get them to change their minds.

Display aid for microprocessors

Oscilloscope interface for alphanumeric information

by Dr K. Padmanabhan, Ph.D., M.I.E.E., and A. P. Senthilnathan

When developing, testing or repairing complex digital circuits, particularly microprocessor based systems, a means of displaying information is helpful and often essential. A convenient method of displaying data is on an oscilloscope, and this interface enables up to four lines of information to be displayed simultaneously.

The circuit is connected to the address and data lines of a microprocessor system and provides X and Y inputs suitable for a 5MHz oscilloscope. The design is based on a simple ASCII character generator which uses a dot matrix display. A surplus MK2002 is shown in Fig. 1, but any character generator which gives column outputs can be used. The display comprises four rows of 16 characters, each formed from a 5 × 7 dot matrix. Three dot spaces are used between characters and three line spaces between rows. The display does not use Z-modulation to produce the characters, instead character information is achieved by switching the Y-axis for each dot on a line. This by the simulated display produces a positive and negative image as shown in Fig. 2, and either or both can be viewed by adjusting the Y-shift control.

The circuit uses a 555 clock running at 100kHz for the dot timing, and a 4011 time-base generator operating at around 600Hz for the X-axis line generation. The character generator is provided with AS-CII data from a 128 × 8 static r.a.m. and, as the MK2002 is a m.o.s. device, a t.t.l. to m.o.s. interface is provided by two 7426 high-voltage NAND gate i.cs and a 74141

one-of-ten decoder-driver.

Clock pulses are gated to a 4024 7-stage column counter which drives the column decoder through eight steps and changes the column selected for each character. At the end of every 8th count, the r.a.m. address is incremented by the address selector to present the next character on the same row. After accessing and displaying 16 characters on the first line of the first row, the clock gate is disabled by a flip-flop which detects the 128th count from the 4024.

On the next line the clock gate is enabled by the rising edge of the time-base signal and the row counter advances by one. In this way the 4158 advances for ten successive lines, out of which seven provide the display and three provide line spacing. After line 10, the remaining three

DATA LOGGING
APPLICATION
CHANNEL 1 *3.73V
CHANNEL 2 *150MA

CHANNEL 1 *3.73V
CHANNEL 1 *3.73V
CHANNEL 2 *150MA

rows (10 lines each) follow in the same manner except that the memory address count continues from 16 to 64 because address lines A4 and A5 are connected to the second stage of the 4518. This stage counts up to five because only four rows of characters are used.

Column output information from the MK 2002 is selected during each of the seven lines by a 74151 1-out-of-8 switch which is addressed by the 4518. The lines are shifted below each other by adding weighted outputs from the 4518 and driving the Y-amplifier of the oscilloscope. Video shift information from the 74151 output is also combined by the CA3130.

Data from a microprocessor is fed to the memory by a 74365 unidirectional buffer. Six data lines are used as only six lines are needed for the capital letters in ASCII code. The 64 characters stored in r.a.m. are continuously displayed on the c.r.t. until the data is changed by switching the r.a.m. address to the microprocessor via the 74157 address selector, and enabling the 74365 with the latch output. For storing data, the 7475 is loaded with a 1 and software instructions load the r.a.m. Software then resets the latch by loading a 0 into it which also switches the r.a.m. addresses back to the counters.

The address decoder selects the display r.a.m., which here is given the addresses 0800 to 087F. However, in many microprocessor systems full address decoding is not necessary. Fig. 3 gives an example of the software necessary for

Fig. 2. Dot matrix display format. Because the Y-axis is switched to produce dots on a line, positive and negative displays are shown simultaneously.

displaying data and a legend on four lines in locations 0180 to 01C0 using an 8085 processor.

Part two describes hardware modifications for 8-line operation and programming details for a 2716 character generator.

Fig. 3. Software example for an 8085 processor.

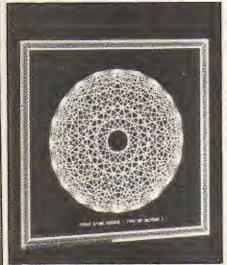
	-	
PUSH	D	
PUSH	В	
PUSH	H	
SUB	A	AND THE RESERVE AND THE
INC	A	Make Accumulator = 1
LXI	H 00 18	Point to latch address
MOV	M,A	Sets selecting latch
LXI	D 00 08	Point to display r.a.m.
MVI	B 40	
LXI	H 80 01	
MOV	A,M	Store the character in
		r.a.m. address
STAX	D	
INX	D	
INX	H	Increment memory
		address
DCR	В	Count for 64
JNZ	LOC	OP.
SUB	A	
LXI	H 00 18	
MOV	M,A	Resets the selecting
		latch for counter access
		to r.a.m.
POP	H	
POP	В	
POP	D	
HLT		

Electronic Displays '81

With the continued success of Electronic Displays, this year's show was held in the more spacious Kensington Exhibition Centre, and attracted 55 exhibitors. Unlike some other areas of electronics, the display market does not seem to be seriously affected by the economic troubles. Several exhibitors were showing new products which had just been "unpacked" and they could not yet give prices or delivery.

L.c.ds - the fastest growing technology

Because the traditional weaknesses of liquid crystal displays are steadily being overcome, they are now receiving a great deal of attention from many equipment makers. This trend was reflected by the large number of exhibitors, nearly a third, who were offering custom or ready-made displays. Most development effort at present is aimed at increasing the step-response and temperature range of the fluids, and increasing the size of displays which is



A 235mm square plasma panel from Thomson-CSF which offers a resolution of 512 lines x 512 points.

limited by the sealing process on the glass

Most manufacturers are improving their hermetic sealing technique and consequently are offering much larger display sizes. Several exhibitors were demonstrating 7-segment and dot-matrix displays with character heights above 80mm. Lucid displays announced a new range of devices with an extended temperature range of -30 to +85 deg. C.

More distributors want a piece of the action

New names in the l.c.d. business include Bulgin, ITT and Racal. Bulgin are now marketing the Data Images (a splinter company from LXD) range of displays

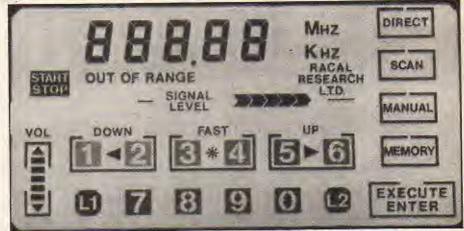
which includes two and four-inch character sizes. These displays are supported with electroluminescent backlights and Bulgin's own range of bezel assemblies.

ITT Meridian have recently signed an agreement with the Japanese manufacturer Epson who claim to have produced the first range of long-life l.c.ds. These devices offer an expected lifetime of 100,000 hrs instead of the usual 50,000 hrs. Racal's stand generated a lot of interest following their announcement of a new l.c.d. division which can offer a custom design and manufacturing service for colour and large area displays.

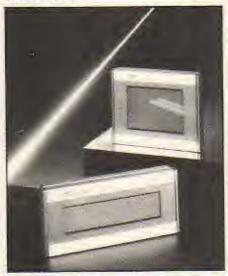
Two innovations from this division are a display electronic module (d.e.m.) and a reconfiguring display/keyboard. D.e.m. new set of prompts in a similar way to the "menu" on a computer v.d.u.

Flat-panel displays are replacing c.r.ts

Flat-panel displays using liquid crystal, electroluminescent and plasma technology were all demonstrated as alternatives to the conventional bulky c.r.t. display. Hitachi, a newcomer to the show, claim to manufacture over 50% of the world l.c.d. output, including flat-panel types. One disappointment, however, was the "non-arrival" of Hitachi's prototype l.c.d. colour television. Exhibits which did arrive included a new range of colour 7-seg-



from Sharp. \



combines a l.c.d. and thick-film technology to produce a single display driver module. The l.c.d. backplane forms a thick-film substrate which carries the necessary circuits to produce, for example, a complete frequency counter and display module. This system allows the display to be used in the transmissive mode without the obstruction of a p.c.b. Racal's reconfiguring display/keyboard combines a l.c.d. with a touch-sensitive switch, when pressed, reconfigures the display to show a

Flat screen electroluminescent displays An example of Racal's reconfigurable key-

ment displays and a 64×200 dot-matrix display for larger characters. To support their range of displays, Hitachi have also developed a 4-bit c.m.o.s. microprocessor which will directly drive l.c.ds.

G.E.C. have produced an 80-character d.c. electroluminescent display panel which only requires 8 and ±60V supplies. Each of the 80 characters is formed by a 5×7 dot matrix and they are arranged in four rows. The display panel is supplied with two circuit boards which provide supply regulation, data organization, character generation and display drive. A 128character set is standard, but special character sets can be provided.

A 235mm square a.c. plasma panel from Thomson-CSF comprises 512 lines of 512 points. This panel can be used for displaying graphics where each point is individually addressed. Alternatively, for alphanumeric operation, 64 lines of 85 5×7 characters or 32 lines of 64 7×9 characters can be produced.

The three-day exhibition was supported by a conference which presented 24 papers covering display device technology, teletext, display systems, and display applications. Reprints from these sessions and those presented at the 78, 79 and 80 exhibitions are available from Network, Printers Mews, Market Hill, Buckingham, Rucke

C.b. frequency synthesis

Generating 40 channels for 27MHz

by E. F. da Silva, M.Sc., Ph.D.

This article reviews the digital frequency synthesizer systems which can be used to generate the crystal-controlled frequencies required for 40-channel British citizens' band operating at 27 MHz. A practical design is also described which provides 40 channel operation.

The lower and upper frequency limits of c.b. are 27.601250 and 27.991250MHz, with a channel spacing of 10kHz and a frequency tolerance of 1.5kHz per channel. The carrier is frequency modulated with voice transmission and the maximum frequency deviation is 2.5kHz. In addition to the frequencies shown in Table 1, another set of forty frequencies (transmit frequencies and receiver intermediate frequency) must be supplied for the local oscillation in the superheterodyne receiver. In view of the requirements for frequency stability, manually controlled variable-tuning oscillators are not practical and, if direct crystal-controlled oscillators are used, frequency multiplication and/or mixing will generally be necessary to produce the required frequency deviation. Unfortunately, frequency multiplication and mixing produce harmonics and increase the cost, so a cheaper and more practical method is desirable. The availability of high-frequency low-power c.m.o.s. i.cs now makes frequency synthesis a practical alternative. An ideal synthesizer for c.b. would comprise one or two i.es but, as there are no dedicated devices available at present, standard components must be used.

The basic frequency synthesizer as shown in Fig. 1. comprises a voltagecontrolled oscillator operating at frequency fo. This frequency is divided by a programmable divider-counter N, to produce a frequency f_n which is compared with a reference frequency fr. The difference between these two frequencies is translated into a d.c. voltage which controls the v.c.o. so that $f_n = f_r$. Because $f_0 =$ $Nf_0 = Nf_r$, f_0 is locked to the reference frequency by the programmable divider. In practice f_r is normally chosen to be the frequency channel step or spacing, i.e. 10kHz for 27MHz c.b., or a sub-multiple of the channel spacing so that integer changes in N will step the output frequency to the required operating fre-

Direct synthesis for c.b.

The block diagram of a direct synthesis system, shown in Fig. 2., is similar to Fig. 1. except that a prescaler, K, is connected between the programmable divider and

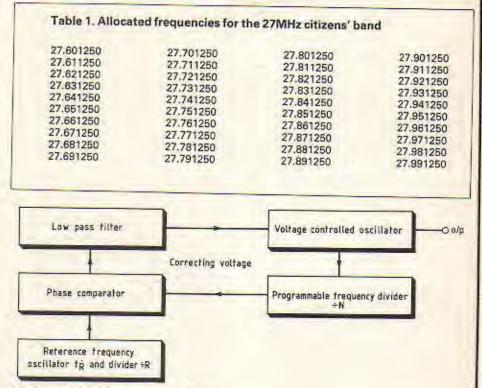


Fig. 1. Basic frequency synthesizer system.

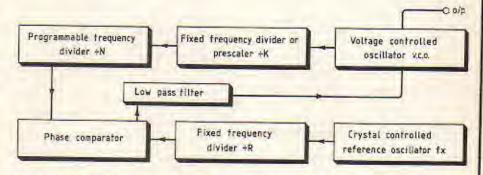
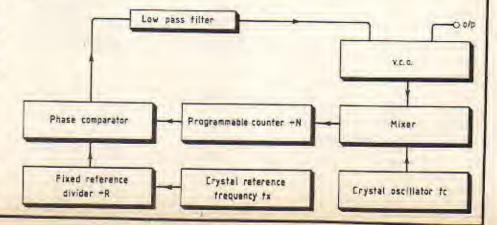


Fig. 2. Direct frequency synthesizer which uses a prescaler between the programmable divider and v.c.o.

Fig. 3. Mixing type of frequency synthesizer. The output frequency is mixed with a crystal

oscillator signal to produce an intermediate frequency.



v.c.o. The prescaler is necessary because c.m.o.s. programmable counters are not readily available for direct operation at 27MHz. Also, crystal oscillators operating at a reference frequency of 10kHz are generally bulky and expensive, so it is more

of 22081-22393 to cover the band of transmitting frequencies, and the reference frequency would then be 125Hz. However, this low reference frequency will limit the capture range of the phase com-

is mixed with a 26.591250MHz crystal oscillator, fc, to produce an i.f. of 1.4MHz which can be fed directly to the programmable divider-counter. The advantages of such a system are, the reference frequency can be made equal to the channel spacing, parator, present difficulty in low-pass fila prescaler need not be used for c.m.o.s. programmable counters, the total division factor is greatly reduced which increases the loop bandwidth, more easily divisible frequencies can be chosen and the frequencies are lower, which eases production techniques. A disadvantage is the additional cost of a mixer and crystal oscillator. However, this cost is greatly offset by the saving in logic circuits which would nor-

lator signal.

Division number Two binary switches Vdd +5V DpA₂ Dp82 Dp81 DDAL DDA3 ОрВз Dp Dp YHER ETL B A 15 ME14569 ME14568 PE out Dp B4 Perout Pein 0 PE Pout Ein >330 Vdd out of Lock Indicator 10k **≥4**47 22k 2M2 202 BFX 89 \$470 in Tx: 26-591250 MHz Rx: 27-051250 MHz 200000 TEX.22 2474 of Horx 2N3819 820 BFX89 220 BFX89 2N3B19 8205 111 22k 680n 100n Joseph ment input - Output

Fig. 4. Practical design for a mixing synthesizer, L₁ is 13 turns of 0.25mm wire on a Neosid A7 assembly.

convenient to use a higher crystal frequency and divide it for the reference frequency.

As mentioned earlier, the channel spacing is 10kHz, the lowest transmit frequency is 27.601250MHz and the highest transmit frequency is 27.991250MHz. The factors of these frequencies are $2 \times 5 \times 5$ \times 5 \times 5 \times 22081Hz, and 2 \times 5 \times 5 \times 5 \times 5 × 2239Hz respectively. With c.m.o.s. programmable counters restricted to around 10MHz at 5V, a +10 prescaler would give programmable-counter ratios tering and also cause a large change in N because $N = (f_{\text{channel}} + K + f_{\text{r}})$. Therefore, eight steps in N will be required for each channel change. A similar system has been described by RCA for American citizens' band transceivers.

Synthesizer mixing methods

A block diagram of a frequency synthesizer using mixing is shown in Fig.3. The output frequency fo high, 27.991250MHz,

Local oscillator frequencies

mally be needed to generate the local oscil-

The set of forty local-oscillator frequencies for the transceiver when receiving can be obtained in several ways. The programmable counter can be made to perform an additional count when the transceiver is operating in the receive mode. For example, with fo at 27.991250MHz, fr at 10kHz, a division ratio of 140, and a receiver i.f. of 460kHz, the local-oscillator frequency must be 27.991250 + 0.460, i.e. 28.451250MHz.

This frequency can be generated by letting N count initially to 140 (the figure set by the operator), inhibiting its output and then setting N to count an additional 46 steps (460kHz + 10kHz), i.e. a total of 140 + 46. At the end of this count an output pulse is fed to the phase comparator. The additional 46 steps can be produced automatically by using multiplexing devices such as the 4019. This system produces local-oscillator frequencies greater than the transmit frequency by the chosen i.f., but it can be more costly with the additional i.cs.

An alternative scheme uses early zero detection where, instead of letting the programmable counter reach its full count of 140, the count is stopped at 140 -46, i.e. the 94th step. Therefore, the frequency for will initially be greater than the reference frequency and it will cause the phase comparator to decreases the v.c.o. frequency until it is 460kHz below its initial frequency of 27.991250MHz.

A third scheme, only applicable to frequency mixing systems, is simply to switch in an alternative crystal which is offset from the transmit frequency by the receiver i.f. This method permits either high or low injection of the receiver local oscillator and is relatively easy to implement.

Practical circuit

A frequency synthesizer using the mixing method described above is shown in Fig. 4. The crystal reference-oscillator frequency f_x is produced by a 1MHz crystal. No tuning controls are needed, and the frequency divider chain + R is incorporated within the 14568 phase comparator i.c.

The division ratio has been programmed to 100 and the reference frequency is therefore 10kHz. The programmable divider-counter divides over the range 101 to 140. The units and tenth part of the division ratio is incorporated in the 14569 and is controlled externally by binary switches connected to the DpA and DpB inputs respectively. The hundredth part of the progammable counter in incorporated in the 14568 in conjunction with the phase comparator. This part of the counter is hard-wired to divide by 1, so no switch is necessary. The local oscillator frequencies are obtained by switching in the 27.051250 MHz crystal in place of the 26.591250MHz transmit crystal.

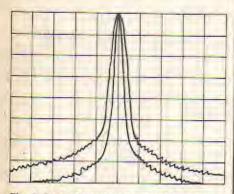


Fig. 5. Typical spectrum around the carrier for the circuit in Fig. 4.

To adjust the synthesizer, set the thumbwheel switches to 20, i.e. a frequency-division ratio of 120 and check that the transmit crystal is being used. Adjust L1 in the v.c.o. until the l.e.d. turns off and then set the voltage at point A to 2.6V. If a counter is available, check that the output frequency is 27.791250MHz. Set the programmable counter switches through positions 1 to 40 and check that the frequencies agree with Table 1. Switch in the receive crystal, step the programmable counter switches from 1 to 40 and check that the output frequencies are 460kHz above the corresponding values in Table 1. The synthesizer is now adjusted and should produce a spectrum similar to that shown in Fig. 5.

Further reading

- Home Office Publications, "Open Channel Radio", citizens' band radio, HMSO, July, 1981.
- 2. Dance, B., "Digital Tuning Systems", Electronic Industry, p.41-46, June, 1981.
- RCA application note ICAN 6374, "Applications of the COS/MOS CD4059 programmable divide by N counter", Digital frequency synthesis for FM tuners and CB transceivers.
- RCA application note ICAN 6716, "Low Power Digital Frequency Synthesizer utilizing COS/MOS ICs".

Books

Semiconductor Data Book.

Book, compiler A. M. Ball 184 pp., paperback

Newnes Technical Books, £5.50

Those familiar with the Radio Valve and Semiconductor Data Book, last published in 1975, will be pleased to know that a new edition – the eleventh – is now published. Valves have finally taken their leave and left the field open for a full range of discrete semiconductor devices.

In format, the book is very similar to its predecessors, giving a number of the most important characteristics against each type number, the main listing being followed by a section on pinout details and list of devices comparable to each type – though this is not cross-indexed.

Electric Circuit Theory, by R. Yorke

331pp., hard and paper backs Pergamon Press Ltd, £13.00 (£6.50)

Dr Yorke's intention was to provide first-year university students with a course of reading on circuit theory "of modest complexity and length". The mathematics needed for an appreciation of the text do not, therefore, extend beyond A-level.

Chapters on a.c. and d.c. circuits by the steady-state and transient analysis of linear circuits in the time and frequency domains by means of exponential and Laplace transforms. Chapters on network analysis include introductions to Kirchhoff, Thevenin and Norton, topology, the superposition theorem and the frequency response of networks with attention to poles and zeros and the Bode plot. The final chapter deals with the transmission of power in polyphase lines.

Throughout the book, the author is careful to include a large number of problems (answers given) and a short bibliography is provided.

Radio and Television

Servicing, Ed: R. N. Wainwright, 815pp., hardback Macdonald, £17.50

This is the latest in a long series of books well known to those engaged in repairing domestic receivers. It consists of manufacturers' servicing information—circuit diagrams and alignment details at least and, in some cases, a more detailed description—of several hundred 1980/81 models of radio and television receiver, clocks, tape recorders and music centres from most of the manufacturers, with a supplement containing information which has appeared since the data sheets were published.

Computer Consciousness,

by H. D. Covvey and N. H. McAlister 212 pp., paperback Addison-Wesley, \$4.95

Computers are complicated devices; and people are lealous of status. The two together have established a new social class of computer pundit, in whose interest it is to baffle the public with computerspeak. In turn, this has led to the appearance of a great number of bgoks which set out to dispel the fog and explain computers

in simple terms. This is one such book.

Unfortunately, since computers are indeed complicated, it is barely possible to explain them simply. No amount of weird cartoons or whimsteal headings will make the subject easier to understand. This is a tentative book: in common with far too many of its kind, it spends much of its time looking at computers from a distance without ever coming into contact with them, and gives the feeling of listening to an endless overture when one would really like the opera to begin.

Faced with a computer, most lay people (to whom this book is directly addressed) will ask "What will it do?" They will not find the answer here – there is much vague generalization and background, but not much to help a businessman decide whether a computer would assist him or not. There is a need for a text which will debunk the subject in a helpful and concrete manner. This is not it.

Linear Integrated Circuits

by Sol D. Prensky and Arthur H. Seidman. 336 pp., hardback Prentice/Hall International, £14.95

This is a practical book on the applications of linear i.cs for the engineer or technician written at about the same level as Wireless World. It covers op-amps, including testing and breadboard work, power amplifiers, consumer and communications circuits, regulators, digital interfacing, phase-locked loops, and a-d and d-a conversion. An appendix lists commercial devices by type number and gives one-line descriptions and cross-references with the text. Much of the material appears to have been obtained from manufacturers' application notes. Seidman is a professor of electrical engineering and the book is an expansion of an earlier manual by Prensky, now deceased.

Analog I/O Design by Patrick H. Garrett. 272 pp., hardback Prentice/Hall International, £16.45

With the increasing use of digital computers to process information in electronic systems, there is a new field of technology growing up concerned with making analogue devices and circuits work in conjunction with them. This book is on the design of analogue systems primarily for computer input and output applications. It is written to provide both a one-term course on analogue application and computer interfacing for students and a reference work on detailed design for practising engineers. Most chapters end with a set of problems. The book covers instrumentation amplifiers, active filter design, transducers, analogue signal processing, data conversion devices including a-d and d-a, and reconstructing the original signals from digital outputs. Three experiments are given in appen-

High-frequency Application of Semiconductor Devices by Ferenc Kovacs. 391 pp., hardback Elsevier, 78 US dollars

Written by a Hungarian author from a research institute in Budapest, this expensive book is a fairly deep and rather academic treatment of the operation of discrete and integrated semiconductor devices at high frequencies. Basic design principles of many practical circuits are discussed in the 24 chapters. The bulk of the space is given to amplification, and the remainder to oscillators, frequency convertors, multipliers etc. The book is well illustrated and has numerous tables and mathematical analysis. It has an extensive, 15-page list of references.

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Diode function generation

Simple strategy for choosing break-points

by Muhammad Taher Abuelma 'atti, B.Sc., Ph.D., University of Riyadh

This strategy for picking the necessary break-points in designing a diode-resistor networks avoids negative resistance values in the result which saves computational time. This simplifies diode-resistor network design and makes it more systematic than previously.

Resistor-diode networks are often designed to meet a given non-linear inputoutput specification. While modelling diodes with the diode equation gives a solution which is both accurate and general^{1,2}, the choice of break-points becomes a problem where the input is limited1 (Vin≤10V), especially for highly non-linear functions. Contrary to the ideal diode model3 where any two points on a curve such as Fig. 1 can be connected by a straight line, it becomes obvious using the diode equation that if two points are chosen too close together they cannot be realised. If two points are realised close together this sets up a condition whereby the next points cannot be realised1. This is mainly due to the need for negative resistance values which are not practically feasible. To avoid this difficulty a simple strategy for picking the break-points is needed.

Convex non-linearities

The non-linear input-output characteristic of Fig. 1(a) can be met by the diode-resistor network shown in Fig. 2(a). Design equations, rewritten from Bello¹, are

$$R_{2i} = R_{1i} \left[\frac{V_{DC}}{V_{2i}} - 1 \right], \ i = 1 \rightarrow N$$
 (1)

 $I_{\text{Di}} = I_0 [\exp(V_{\text{Di}}/\eta V_{\text{T}}) - 1], i = 1 \rightarrow N$

$$\frac{V_{1i+1} - V_{2i+1}}{R_{A}} = \sum_{j=1}^{i} I_{Dj} + \frac{V_{2i+1}}{R_{B}}, \quad i = 1 \rightarrow N$$

$$\frac{V_{2i+1} - V_{DC} - V_{Dj}}{R_{2j}} + \frac{V_{2i+1} - V_{Dj}}{R_{1j}} = I_{Dj}$$

$$j = 1 \rightarrow i, \ i = 1 \rightarrow N. \tag{2}$$

For the *i*th diode initial conditions in equation are taken from the (i-1)th calculation (i>2). Combining equation (2) written for j=I and with equation (1) solving for R_{1i} in terms of known quantities gives

$$R_{1i} = \frac{V_{DC}}{I_{Di}} = \frac{V_{2i+1} - V_{2i} - V_{Di}}{V_{DC} - V_{2i}}, i = 1 \rightarrow N.$$
 (3)

For R_{1i} and R_{2i} to be positive, equations (1) and (3) show that the following two conditions must be satisfied:

 $V_{DC} > V_{2i}$ and $V_{2i+1} - V_{2i} > V_{Di}$, $i = 1 \rightarrow N$.

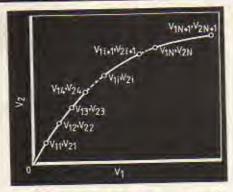
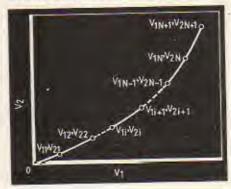


Fig. 1, Monotonically increasing non-linear characterisites, with N+1 break-points, synthesized by diode-resistor networks.



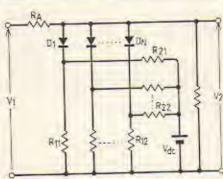
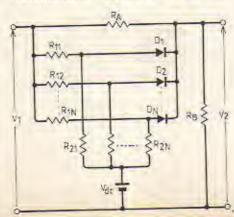


Fig. 2(a) Diode-resistor network for realising monotonically increasing convex characteristic of the type shown in Fig. 1(a). (b) Diode-resistor network for realising monotonically increasing concave characteristic of the type shown in Fig. 1(b).



This means that the supply voltage must be greater than the maximum output voltage. Also the break points must be chosen so that the difference between output voltages at two successive break-points will be greater than the voltage drop across the conducting diode (about 0.2V for Ge and 0.6V for Si diodes).

This strategy was extensively used to design diode-resistor networks to meet given monotonically increasing convex characteristics. Fig. 3(a) shows a typical example for meeting the non-linear function

$$V_0 = V_1 - 0.04V_1^3 + 0.001V_1^5$$

with maximum input voltage of 4V.

Concave non-linearities

The non-linear input-output characteristic of Fig. 1(b) can be met by the diode-resistor network of Fig. 2(b). Design equations, rewritten in a generalized form from Abuelma'atti², are

$$R_{2i} = R_{1i} \frac{V_{2i} + V_{DC}}{V_{1i} - V_{2i}}, \quad i = 1 \rightarrow N$$
 (4)

$$\frac{V_{2i+1}}{R_B} = \frac{V_{1i+1} - V_{2i+1}}{R_A} + \sum_{j=1}^{i} I_{D_j}, i = 1 \rightarrow N$$

$$I_{\text{Di}} = I_0 [\exp(V_{\text{Di}}/\eta V_{\text{T}}) - 1], \quad i = 1 \rightarrow N$$

$$=\frac{V_{1i+1}-V_{2i+1}-V_{Di}}{R_{1i}},$$

$$i=1 \rightarrow i, i=1 \rightarrow N.$$
 (5)

$$\frac{V_{2i+1} + V_{Di} + V_{DC}}{R_{2i}} + I_{Di}$$

For the ith diode, initial conditions in equation (5) are taken from the (i-1)th calculation. Combining equation (5) written for j=i with equation (4) for R_1 , in terms of known quantities gives

$$R_{1i}I_{Di} = V_{1i+1} - V_{2i+1} - V_{Di} - \frac{(V_{2i+1} + V_{Di} + V_{DC})(V_{1i} - V_{2i})}{V_{2i} + V_{DC}}.$$

If the supply voltage VDC is chosen so that

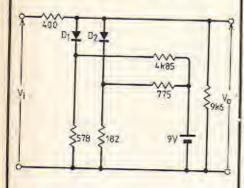
$$V_{DC} \gg V_{2i+1} + V_{Di}$$
 (6)

ther

$$R_{1i}I_{Di} \approx V_{1i+1} - V_{2i+1} - V_{Di} - V_{1i} + V_{2i}$$
 (7)

For R_{1i} and R_{2i} to be positive equations (4), (6) and (7) show that the supply voltage must be sufficiently larger than the

maximum output voltage, and the breakpoints must be so chosen that the difference between input voltages of two successive points is greater than the difference



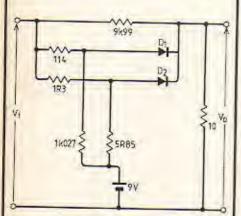


Fig. 3(a) Diode-resistor network for realising function with maximum input voltage of 4V. (b) Diode-resistor network for realising the function $V_o = V_i - 0.04V_i^0 + 0.001 V_i^0$ with maximum input 3.5V. Diodes are type 1N5404.

between the corresponding output voltages by an amount at least equal to the voltage drop across the conducting diode.

This strategy was extensively used to design diode-resistor networks to meet given monotonically increasing concave characteristics. Fig. 3(b) shows a typical example where the non-linear characteristic was expressed by

$V_0 = 0.001 V_1^5$

with maximum input voltage of 3.5V.

The means of selecting break points for diode-resistor networks presented here is intended to simplify the design of function generators. Networks for monotonically increasing concave and convex functions illustrate the validity of the selection procedure.

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2. M. T. Abuelma'atti. Synthesis of a

concave monotonically increasing function using the diode equation model, International Journal of Electronics, In press.

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3. A. E. Crump. Diode function generators, Wireless World, vol. 73, December 1967, pp. 594-8.

IN OUR NEXT ISSUE

Millimetre-wave lens aerials. An easier way of constructing metal plate refractor aerials, which hitherto have not been popular because of manufacturing difficulties. Dr Ken Smith gives design and construction details for aerials in the 20-30GHz region.

Understanding light units. Electronics engineers are having to use optical devices and techniques more and more but have difficulty in understanding the various units for measuring light. This interpretive guide is written specially to help them.

Direct digital frequency synthesizer

generates sine waves in numerical steps, a 1MHz output, for example, being produced by stepping through the sine table at a rate of 45° every 125ns and feeding the result into a d-a converter. Range: 0-3MHz.

On sale November 18

continued from page 49

Having first set the overhang, the cartridge is then twisted round slightly until the two sighting holes at 110 and 49 mm radii both align with the centre of the turntable spindle as the arm is swung inwards. Due to the offset of the overhangsetting slot, this twisting round of the cartridge may slightly alter the overhang, but the appropriate correction is easily made in a second shot if necessary.

The amount of overhang provided by the dimensions shown is in accordance with the rule proposed in the above article: h=2600/C where C is from arm pivot to turntable axis, in mm. Needless to say, the basic design can be used for any required overhang rule, the position of the slotted hole and setting marks being changed accordingly. The 2 mm holes are only intended to act as setting marks, and could be omitted in favour of short cross lines.

The author has made up a gauge in accordance with Fig. 2, and finds it a major improvement. He can now be certain, for the first time, that the required cartridge position and offset angle are correct to something within 1° of error, whereas previously an error of several degrees would have been possible.

 Cartridge alignment problem. A misunderstanding over whether author's corrections had been incorporated into proofs led to errors which must have made understanding R. J. Gilson's October article difficult. Figure numbers were omitted and although the diagrams were in the right order some of the text references were incorrect. On page 60 column 1, read Fig. 2 in line 5 for Fig. 1, Fig. 2 for Fig. 3, and in column 3, Fig. 2 for the lower reference to Fig. 3. Take the multiplication signs for addition signs in the Appendix on page 61, formulae 4 a, b and c, and also prior to 2 & 2.5° on page 60, column 1. Also in the Appendix, for the upper formula 1, read $(L^2+R^2-C^2)/2LR$, whilst in formula 4c βin should have been βi. Just below the Appendix in column 3, insert a stop after 13mm to end that sentence, Apologies to Mr Gilson for this marring of his constructive review of the tracking problem.

Aultichannel digital tape recorder

Design requirements of the digital circuitry

by A. J. Ewins, B. Tech., Research Laboratories, London Transport

In the first part of this article, the author described the aims and design concept of this economical instrumentation recorder, which employs a modified audio cassette deck with added digital electronics. In this second part, the additional circuitry is outlined.

Having determined the number of channels per track of the tape-recorder, the number of bits per data word, the length of the sync. word, and the data and tapeclock frequencies, the digital circuitry could now be designed. Figure 2 shows the main body of the recording circuitry in block form, the heart of which is the block marked 'control circuitry'. Starting with a crystal-controlled oscillator of 3.2768 MHz, this circuitry generates the two clock frequencies, DC and TC, which are divided down and operated on by various logic elements to generate the numerous pulse trains that control the flow and direction of the serial data. The inverse clocks outputs, DC and TC, clock the serial data through the various shift registers. In this way, all gates and switches are opened or closed on negative transitions of DC or TC, whilst the serial data advances on positive transitions. A reset pulse is generated every 72 cycles of DC (or 80 cycles of TC) and serves to synchronize the various logic elements of the control circuitry,

An example of some of the pulse sequences produced by the control circuitry is shown in Fig 3. This illustrates the control of the clock pulses as seen by the two 72stage temporary buffers (store 1 and store 2) and the sync, word buffer. Store 1 is shown being filled with serial data under the control of DC, up to the moment of reset, and then being emptied under the control of TC. Store 2 is shown being emptied under the control of TC up to the moment of the 72nd pulse. Having emptied store 2, the remaining eight pulses of TC, up to the moment of reset, are used to empty the sync. word buffer. After reset, store 2 is then filled with data under the control of DC. In this way, the sync. word is inserted into the data stream every 72 bits or six data words. A frame of data thus consists of one sync, word followed by six data words, one for each channel sampled. The eight bits of the sync. word are permanently present at the parallel inputs of the 8 bit shift register, and the control circuitry controls the re-entry of these 8 bits into the register once the sync.

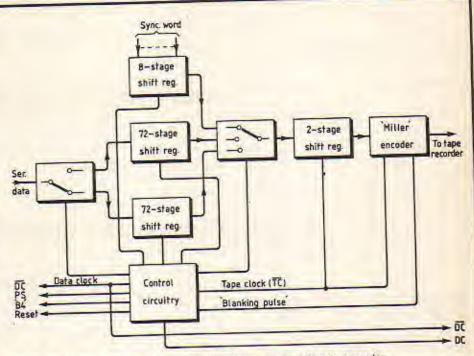


Fig. 2. Main part of recording circuitry, which controls data flow to recorder.

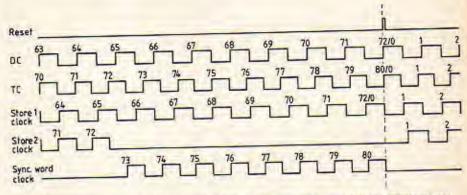


Fig. 3. Pulse trains generated by system in Fig. 2, showing sync. word being inserted into data after 72 bits in store 2.

word has been serially inserted into the data stream.

The control circuitry also generates four sequences of logic pulses, DC, PS, 'B4' and RESET, which go to the preceding stage (Fig 4) to control the multiplexing of the six analogue channels, the digitization of the selected channel and its conversion from parallel to serial form. Figure 5 shows the logical sequence of control pulses, RESET, PS, 'B4' and DC, together with the DATA READY pulse, DR, generated by the analogue-to-digital converter. The RESET pulse is the same as that referred to earlier and occurs every six data words. Having initially synchronized the analogue multiplexer, its continuing presence checks that the multiplexer is always in its original state at the start of each data frame. PS is the parallel/serial control pulse to the 12 bit shift register. When at the logic I level, a positive transition at the clock input transfers the data present on the parallel inputs into the re-

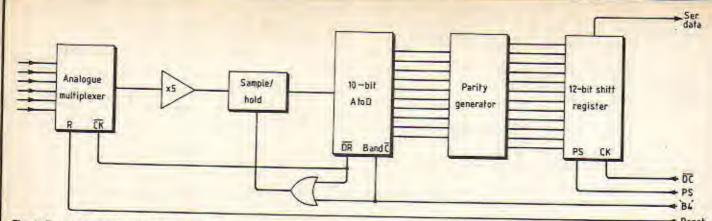


Fig. 4. Four outputs from 'control circuitry' block in Fig. 2 are used to multiplex, digitize and serialize data in six input channels.

gister. When at the logic 0 level, positive transitions of DC transfer the data serially through and out of the shift register. The control pulse B4 is derived from the control circuitry in a similar fashion to PS and occurs, as PS does, once every data word. When B4 goes to logic I, the sample/hold circuit is put into its 'hold' mode via the OR gate. At the same time, it initiates the conversion process of the a-to-d converter and blanks its output. At the start of the conversion and until it is complete the DR pulse of the a-to-d converter goes to logic '1' to keep the sample/hold circuit in the 'hold' mode via the OR gate. Only when the data is ready and DR goes negative to logic '0' does the sample/hold circuit revert to the sample mode. As it does so, the analogue multiplexer is clocked to sample the next analogue channel.

Because of the sequencing of the RE-SET and PS pulses, the data that is being scrially shifted out of the 12 bit shift register immediately after a RESET pulse (and during the conversion of the analogue data from channel 1) is the last data word, from channel six, of the previous data frame. The resulting sequence of data words between RESET pulses is thus in the order of channels 6,1,2,3,4 and 5. This may be resequenced to the desired arrangement of channels 1,2,3,4,5 and 6 by connecting the analogue output from channel 1 to input 6 of the multiplexer, channel 2 to input 1, channel 3 to input 2, and so on.

Referring back to Fig 2, it will be seen that a small 2-stage shift register is placed immediately after the switch gating the output from the two storage buffers and the sync, word buffer. This register is included to remove the undesirable changes in logic level that might otherwise occur as the outputs from these buffers are switched. Remember, the serial data is clocked out of the buffers on the positive transitions of TC and therefore changes in the logic level should only occur at these instances. The switch selects the appropriate buffer on the negative transition of TC, producing possible logic level changes at the wrong moment. Without the 2-stage shift register in between the gate and the

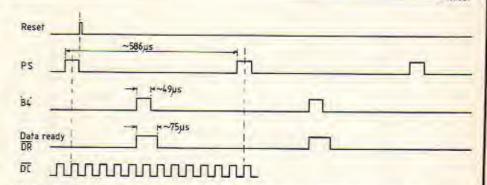


Fig. 5. Timing of control pulses from Fig. 2 system, used to control circuit in Fig. 4.

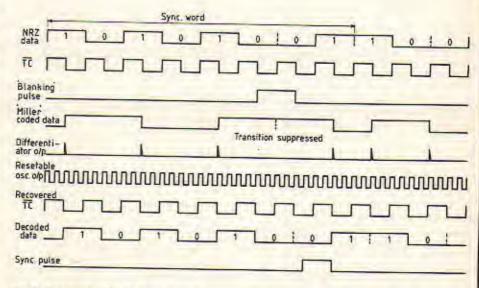


Fig. 6. Sequence 1001 must be used in sync. word to generate sync. pulse on replay. Blanking pulse suppresses a transition, causing a 'gap' which is used to generate pulse. Rest of waveforms are used by Miller decoder, which produces recovered data, recovered tape clock and a sync. pulse at its output.

Miller encoder, the Miller encoder would incorrectly interpret these logic level changes.

As mentioned earlier, it was decided that the sync, word should be 8 bits long and include the sequence 1,0,1. In order that the sync, word may be recognized on playback and decoding of the serial stream (it is quite possible for the sync, word sequence to occur within the normal data

stream) it is also essential that it includes the sequence 1,0,0,1. The need for the 1,0,1 and 1,0,0,1 sequences could be satisfied by a six-bit sync, word consisting of 1,0,1,0,0,1. However, since it was necessary for it to be 8 bits long it was chosen to be 1,0,1,0,1,0,0,1.

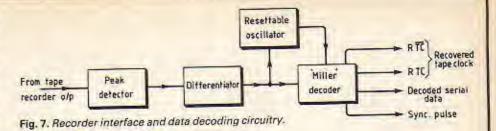
The need for the sequence 1,0,0,1 can be best explained by examination of the various pulse trains shown in Fig. 6. These are generated during the encoding and decoding of the NRZ serial data and are shown in their correct time sequence. The first row is an example of the NRZ serial data that emerges from the 2-stage shift register of Fig. 2 immediately before encoding. The third row shows a blanking pulse that is generated once every complete data frame (i.e. 80 cycles of TC) and

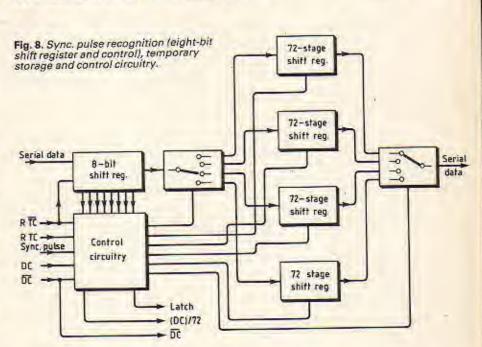
coincides with the centre of the 1,0,0,1 sequence in the sync, word. The blanking pulse is fed to the Miller encoder and suppresses the transition that would normally take place at the centre of the two zero bit cells of the 1,0,0,1 sequence. The suppression of this transition creates a unique gap in the Miller coded transitions, as shown in row four, and is used on replay to generate a synchronizing pulse. This sync. pulse is shown in correct relation to the decoded data stream in the last row of Fig. 6.

The remaining pulse trains of Fig. 6 are associated with the block-circuit diagram of Fig. 7, which shows the tape-recorder interface circuit (the peak detector), a differentiator, resettable oscillator and Miller decoder. During recording, the Millercoded data stream is presented to the recording electronics of the tape-recorder without any attempt at reshaping. However, upon replay the Miller-coded data looks like a series of positive and negative peaks (associated with the original positive and negative transitions) due to the frequency-response characteristics of the tape-recorder circuits. The peak detector detects these peaks and reconstructs the data to look exactly like the original Miller-coded data. The recovered Millercoded data is then differentiated to produce a series of short-duration, positive pulses, associated with every positive or negative transition (see row 5, Fig. 6). These pulses synchronize a resettable oscillator running at four times the frequency of the recovered tape clock. The outputs from both the differentiator and the resettable oscillator are fed to the Miller decoder. Apart from the decoded serial data, the outputs from the Miller decoder are the recovered tape clock, RTC, and a sync, pulse.

The three pulse trains, shown in the last three rows of Fig. 6, together with the crystal-controlled data clock, DC and DC from the recording stages, are fed to the circuit shown in Fig. 8, which is the block diagram of the four temporary storage buffers (72-stage shift registers), an 8-stage shift register and the associated control circuitry. As directed by the control circuitry, the temporary storage buffers receive the serial data under the control of the recovered tape clock. Both the serial data and RTC contain wow and flutter from the tape recorder, but will remain in sync, with each other provided the wow and flutter content does not rise above about 6%. The serial data first passes through the 8-stage shift register, which has parallel outputs so that as the 8 bit sync, word passes through it may be recognised by the control circuitry. Providing this recognition coincides with the recovered sync. pulse produced by the Miller decoder, an overall sync, pulse is produced that aligns the logic elements of the control circuitry in their correct sequence of operation.

The four temporary storage buffers are filled with data in sequence. Eighty RTC clock pulses clock a complete data frame into a buffer, and as each buffer is only 72 bits long, the leading sync. word passes all





the way through and out and is thus removed. When the first two storage buffers are full of data, the control circuitry allows the first buffer to be emptied under the control of DC. A time difference of (2×72)/20,480, or about 7ms, is thus created between the filling and emptying of the buffers. This time gap has proved to be more than sufficient to absorb the small timing errors produced by the wow and flutter of the tape cassette deck.

Three control pulses, DC, LATCH and (DC)/72, are passed from the control circuitry of Fig. 8 to the succeeding circuit of Fig. 9, which controls the reconversion of the serial data stream into the 12 bit data words, their conversion from digital to analogue form and their final demultiplexing via sample/hold circuits. The serial data first passes through a 12 bit serial-in, parallel-out shift register. At the correct moment, the 12 bits present at the parallel outputs are clocked across to a 12 bit latch. A 10 bit parity checker recalculates the two parity bits, compares them with the two recorded parity bits and passes the two resultant GO/NO-GO answers to the DE-MUX control circuitry. At the same time, the 10 bit data word is converted to an analogue output, via the digital-to-analogue converter, which is presented to the inputs of the six sample/hold circuits.

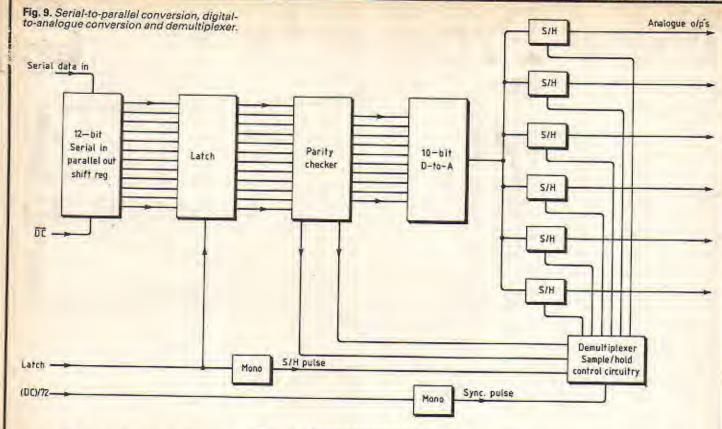
Synchronized by the (DC)/72 pulse and clocked by the LATCH pulse, the DE-MUX control circuit switches the correct sample/hold circuit into its sample mode. If, however, the parity checker gives a NO-GO answer on one of its two outputs,

the sample/hold circuit is inhibited and remains in its hold mode. Figure 10 shows the sequence of a number of pulse trains controlling the operation of the circuit of Fig. 9. The synchronizing pulse is produced by a monostable triggered by the positive transition of the (DC)/72 pulse, Sample hold pulse, SH, is produced by another monostable triggered by the negative transition of the LATCH pulse. Both monostables have pulse lengths of approximately five DC pulses.

Because the 12 bit serial-in/parallel-out shift register introduces a delay of exactly one data word with respect to the synchronizing pulse, the data from channel six appears at the expected output of channel 1; channel 1 appears at the expected output of channel 2; channel 2 appears at the expected output of channel 3; and so on. This is of no consequence whatsoever and it is a simple matter to re-label the output channels accordingly.

Speed control circuitry

The principle of operation of the speedcontrol circuitry is shown in the block diagram of Fig. 11. Ignoring, for the moment, the input to the reference frequency selector from the record/playback electronics of the digital circuitry, it will be seen that accurate speed control is achieved by means of a phase-locked loop. The frequency produced by the tachogenerator is compared with a reference frequency from the voltage-controlled oscillator (v.c.o.) of a p.l.l. integrated circuit, using the phasesensitive detector (p.s.d.) in the i.c. The



output from the p.s.d. is fed to the motor drive circuit where it is filtered and amplified to provide the required drive for the motor.

The purpose of the frequency selector circuit was to enable the cassette tape-recorder to stand alone whilst at the same time providing an input for an external reference.

Very conveniently, the frequency produced by the tachogenerator when the recorder is running at a tape speed of 17/sin/s is around 456Hz, which is very close to the 455.1Hz produced by dividing the tape clock of 22,755.5Hz by 50. During the recording process this crystal-derived frequency of 455Hz is therefore used as the reference frequency for the motor speed control. To obtain perfect long-term speed stability on playback, it is necessary to lock the recovered tape clock, from the recorded data, to the crystal-controlled tape clock. It might be thought that all that is necessary to achieve this is to substitute the output from the tachogenerator with that of the recovered tape clock divided by 50. However, this proved not to be the case; due to an increased amount of wow and flutter in the actual transport of the tape, with a slightly different frequency content, a satisfactory lock of the p.l.l. could not be obtained, except by altering its natural frequency (i.e. by changing the filter components). Even when this was tried, the p.l.l. was not as stable as that in the recording process.

A very satisfactory solution was found, even if it was a little unorthodox, by creating a second p.l.l. with a very much lower natural frequency. In this second p.l.l., the crystal-controlled tape clock is compared with the recovered tape clock, after dividing both clocks by 50, via a

TUNNUMUM :

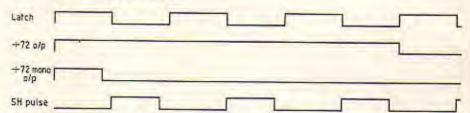


Fig. 10. Pulse train in Fig. 9.

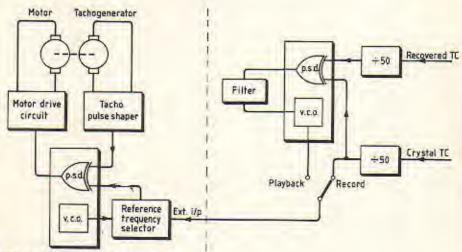


Fig. 11. Speed control circuitry.

p.s.d. The output from the p.s.d. is filtered (determining the loop's natural frequency) and used to control a v.c.o., the frequency output from which is used to provide the required reference for the motor speed control circuit. The lower natural frequency of the second p.l.l. completely removes the influence of wow and

flutter from the recovered tape clock, whilst the higher natural frequency of the first p.l.l. allows the motor speed control circuit to operate under optimum conditions. Visual and audible signals are provided by both p.l.ls to inform the operator that they are 'in-lock'.

To be continued

New Products



Single-board computer

Not so long ago, electronics engineers strove to design systems with numerous readily replacable printed-circuit boards to speed up repairs. But according to Dicoll Electronics there has been a trend towards single-board computers and they have responded by producing the DE530SBC 16-bit computer board, using Western Digital's WD9000 i.c. set. The board, costing around £2,600, includes colour graphics, analogue and parallel/serial i/o, disc controller and p.r.o.m. programming facility, and runs Pascal 'P' code. Up to 128K-bytes of memory can be accommodated (64K r.a.m., and 64K r.o.m.) and a 24-row×80-column display produced using up to eight colours. Power supply requirements are 5V, ±15V and 25V. Dicoll claim that a system incorporating their board would run 10 times faster than a DEC LSI-11/2. Dicoll Electronics Ltd, Bond Close, Kingsland Estate, Basingstoke, Hants RG24 0QB.



Two-channel waveform store

An addition to Datalab's 900 series, the DL912, has two channels and a 20MHz sampling rate a-to-d converter for recording signal frequencies up to 5MHz. Each channel has a 4096-word×8-bit memory providing a resolution of 1 in 250 vertical and 1 in 4000 horizontal. Both channels can be loaded simultaneously with waveforms from separate sources through two input amplifiers and stored information can then be displayed on an oscilloscope or chart recorder. Stored waveforms can be presented alternately with d.c. offset, so only a single-channel oscilloscope is required. The two memories can be combined for long waveforms or divided for short waveforms and the time-base frequency may be altered at a predetermined point on the sweep. Delay and pre-trigger recording are among other facilities of this unit. A digital interface is standard but may be replaced by options including RS232 and



IEEE488 (GPIB) compatible types. Data Laboratories Ltd, 28 Wates Way, Mitcham, Surrey CR4 4HR. WW302

Computer

Up to four analogue signals in the range 0 to ±2V can be accom-modated by WPA's WDC232 laboratory instrument interface. Data is transferred to the computer through an RS232 link in 7-bit AS-CII form from a 31/2-digit b.c.d. ato-d converted with a resolution of one part in 4000. Data from the converter is collated and formatted by a microprocessor which also controls input-channel selection. Up to four of these units can be used together for processing sixteen analogue inputs. Serial data to the computer is automatically adjusted to any rate within 1200 baud. When the WDC232 is fed directly into a printer the transmit rate is fixed at 110 baud. Walden Precision Apparatus Ltd, Shire Hill, Saffron Walden, Essex CB11 3BD.

U.h.f. transistors

Transistors for u.h.f. applications, namely the HXTR-3101 with a 1.8dB noise figure and maximum gain of 19.5dB at 1GHz, and the HXTR-3102 with a 1dB compressed gain of 11.5dB at 21dBm output power and 1GHz, are available from Hewlett-Packard at around £3.88 and £4.85 respectively in one-off quantities. Both n-pn devices are supplied in HPAC-100X metal-ceramic packages. Application notes are also available. Enquiries Section, Hewlett-Packard Ltd, King Street Lane, Winnersh, Wokingham, Berks RG115AR.

WW304

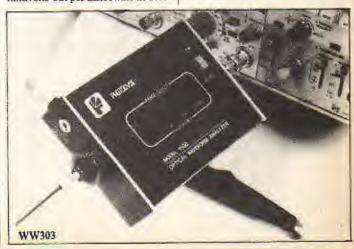


Optical/electrical signal converter

A unit for converting signals from fibre-optic cables, l.e.ds or lasers into electrical signals for displaying on an oscilloscope, spectrum analyser, etc. is manufactured by Photodyne Inc. and distributed in the UK by Lambda Photometrics Ltd. The 1500XP has a frequency response of 0 to 200MHz with 2ns rise and fall time, and is calibrated in millivolts-out per microwatt-in over

four push-button-selectable ranges of 1, 10, 100 and 1000mV/µW. Applications include waveform and loss analyses in optical fibres, and l.e.d. output rise and fall-time measurement. The distributors also announce availability of a calibrated optical attenuator (0 to 90dB) with flat response in the range 800nm to 1300nm from the same manufacturer. Lambda Photometrics Ltd, Lambda House, Batford Mill, Harpenden, Herts AL5 5BZ.

WW305



Housings for terminals

Injection-moulded keyboard and v.d.u. housings with panels for mounting disc-drives can be obtained from West Hyde De-velopments Ltd. The distributors of these German manufactured foam-plastic enclosures have options available for mounting 12in c.r.ts with panels for floppy-disc drives and with plain front mouldings for hard-discs, power supplies, etc. Keyboard enclosures have the same widths and styling as the terminal housings. West Hyde Developments Ltd, Unit 9, Park Street Industrial Estate, Aylesbury, Bucks HP20 1ET. WW306

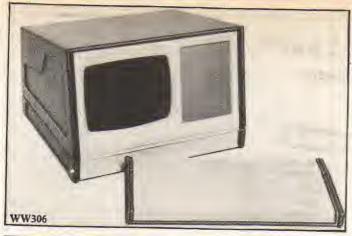
Disc-data separator

Pulses from a floppy-disc consist of clock and data information which must be separated before it enters the controller. Thame Components now market an i.e. from SMC which carries out this function and replaces they say, up to 10 t.t.l. i.es. The 8-pin d.i.l. FDC9216 operates from a 5V supply and is t.t.l.-compatible and programmable for use with either 8in or 5½in drives with single or double density. An 8MHz crystal clock is required by the i.e.Thame Components Ltd, Thame Park Rd, Thame, Oxon OX9 3XD.

Accelerometer

The A-23SI accelerometer from D. J. Birchall Ltd is a case-isolated version of the A-23 series of transducers originally designed for use on aircraft engines. Low basestrain/cross-axial sensitivities and long-term repeatability are claimed to be inherent features of the patented Konic element used in the device and specifications include 7pC/g charge sensitivity, 4.5g weight, 50kHz resonant frequency and -55 to +300°C temperature range. The stainless-steel housing is welded and stud-mounting (10-32 UNF stud), and the price is £190. D. J. Birchall Ltd, 102 Bath Rd, Cheltenham, Gloucestershire GL53 7JX. WW308





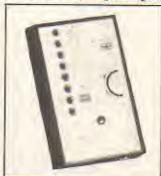


Cable assemblies

Various lengths of cable with U.H.F. or B.N.C. connector terminations and colour-coded strain relievers (10 colours) are available from Greenpar Connectors Ltd in 50 and 70 ohm versions. All components used to make up these cables are also available as separate items. Greenpar Connectors Ltd, P.O. Box 15, Harlow, Essex CM20 2ER. WW309

Small generator for colour tv

A pattern generator for servicing PAL-system colour sets is available through House of Instruments. The Sadelta MC101 generates colour-bar, grey-scale, red-raster, white-raster, cross-hatch, dot, central-cross, central-spot and vertical-line patterns on any carrier between channels 21 and 41. Each generator measures around 131×81×23mm, weighs 250g and



is supplied with rechargeable battery, charger, connecting lead and carrying case for £149.50 inclusive of packaging and delivery, but excluding v.a.t. (quantity discounts are available). House of Instruments, 34/36 High St, Saffron Walden, Essex CB10 1EP. WW310

Encoder discs

Rotation-encoding discs from the electro-forming and photo-etching company Veco are now available off-the-shelf for prototypes, etc. Four versions - one of 30mm diameter with 120 slots and three of 60mm diameter with 120, 240 or 360 slots - are immediately available and the range is to be extended. Some specifications of the 0.8 to 0.9mm-thick discs are ±20µm on the 10mm centre hole, 1:1 mark/space ratio, ±7µm on the slot width and ±20 seconds angular tolerance on the slots. Veco Electroforming/photo-etching Ltd, 36 Essendene Rd, Cater-ham, Surrey CR3 5PA.

High-speed Schottky t.t.l.

A further six 74F series devices have been added to Fairchild's Advanced Schottky t.t.l. range available from Celdis. Among the six are the F109 dual flip-flop for up to 125MHz operation and the F189 64-bit r.a.m. with 20ns access time. The others are the F182, F243, F258 and F399. These devices are claimed to have on average around 75% better frequency response and 25% lower power consumption than standard Schottky types. An evaluation kit for F74 series containing 68 parts, 14 types (not those mentioned above), is available for £30. Celdis, 37 Loverock Rd, Reading, Berkshire RG3 1ED. WW312

P.c.b. measuring

Folding lens/graticule assemblies for measuring p.c.b. track dimensions, hole diameters, etc, can be obtained from Opsec Ltd. Versions for ×5, ×8 and ×10 magnification and either Imperial or metric graticule scales are available. These units, with glass lenses, cost under £10. Opsec Ltd, Holywell Hill, St Albans, Herts AL1 1BR. WW313

A magnifier for examining the insides of plated-through holes (see photo) is manufactured by Graticules Ltd. The Borescope gives a complete picture of the inside of the hole with adjustable magnification from ×40 to ×80. Hunter Equipment Ltd, High St. Bordon, Hants GU35 0AY.

WW314



Frequencymeasurement module

An I.c.d. frequency meter module is available from Thurlby for £19.95 excluding v.a.t. The FM77T, with five, 9mm-high digits, can be used to measure frequencies up to 3999.9kHz directly: external pre-scalers can be used to extend the range. A crystal timebase is used and drift is said to be less than ±1 digit from 10° to30°C. Decimal point position, kHz/MHz legends and 23 pre-programmed i.f. offset frequencies (for use in radio-receiver applications) are selectable. Supply requirements are 4.5 to 7V, 1mA and overall dimen-sions, 70 by 38 by 11mm. Thurlby Electronics Ltd, Office suite 1, Coach Mews, The Broadway, St Ives, Huntingdon, Cambs PE17 4BN. WW315



In the July issue we published details of a range of Germanmade power supplies that were then available through a distributor called 'Big Fars'. If you tried to contact said outlet you probably think we were pulling your leg. This is not so, EA Produktion power supplies are now available through E. A. Electronics, St. Albans House, 577-579 Harehills Lane, Leeds LS9 6NQ.

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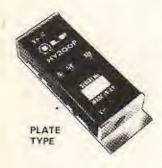
AMPLIFIER WITH HEAT SINK

	LAR Sta	ondard, with heats		iiinə		-	-	-	Without heatsinks					
MODEL NUMBER	DUTPUT POWER Watts fres	T.H.D. Typ eq 18kHz	1.M.D. 80H2/7xH2 4:1	SUPPLY VOLTAGE TYP MAX	SIZE	WT	PRICE	V45	MODEL	SIZE in mm	WT	PRICE	VAT	
HY30 -	15w 4.8t7	0.015%	<0.006%	=18±20	75×68×40	240	€7.28	£1.09	Homoca	A. 1940	line.		-	
HY60	30w 4-811	0.015%	<0.0084	+25±30	76158440	240	f8.33	£1.25					1	
HY120	60w-48Ω	0.01%	<0.005%	±35±40	120±78±40	410	£17.48	12 62	HY120P	120x25x40	715	£15.50	82.30	
HY 200	120w 4-85?	0.01%	<0.0065	#45#50	120x78x50	615	£21.21	13.18		120x26x40	215	£18.46	1000	
HY400	240w411	0.01%	<0.008%	±45±50	120×78×100	1025	COLUMN TO A	14.11	HY400P	120126170	375	128.33	14.25	

Protection Load line, momentary short circuit (typically 10 sec) Slew rate: TEV us Rise rime: 5µs S.W.retia 100db Frequency response (- 3dB) 15Hz - 50kHz Input sensitivity 500mV rms Input impedance, 100kΩ D Damping factor: (852/100Hzt)>400

_			with heatsinks							Without heatsinks			
HD120	60wi4 812	0.01%	<0.006%	±35=40	120 # 78 # 50	516	F72.09	27.27	HD1200	170±26±50	000	*****	
HD200	120w/4-8Ω	0.01%	<0.006%	±45±50	120x78x60	620	£27.38	64.11	HD200P	120,26,50	net	F22 F2	10 E
HD400	240w/4Ω	0.01%	<0.006%	±45±50	120x78x100	1025	£38.63	E5.79	HD400P	120×26×70	375	£34.28	15.14

Protection: load line, PERMANENT SHORT CIRCUIT (deat for discolarup use should evidence of short circuit not be immediately apparent). The Heavy Buty range can claim additional autgut power devices and complementary protection circuitry with performance specs, as for standard types



MOSFET Ultra-Fi, with heatsinks								Without heatsinks					
MOS120	60wi4-80	<0.005%	<0.006%	±45±50	120±78±40	420	£25.88	£3.88	MOS120P	120x26x40	215	£23.32	(350
M05200	120wi4-8Ω	<0.005%	<0.006%	±55±60	120478x80	850	£33.46	€5.02	MOSZODP	120v26vA0	820	P29 67	T # 20
M0S400	240w/452	< 0.005%	<0.008%	±55±60	120×78×100	1025	€45.39	18.81	MOS400P	120×26×100	525	138.91	F5.84

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Siew rate: 20V/µs Rise time: 3µs SiN ratio: 100ab Input sensitivity: 500mV rms boot impediate: 100kg Prequency response (- 3dB): 15Hz 100kHz Damping factor: (8Ω 100Hz)>400

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MODELNO, FOR USE WITH		PRICE	313-		
PSU30	15V combinations of HY5/66 series to a maximum of 100mA or one HY67 The following will also drive the HY6/66	E4.50	£0.68		
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HY7	MONO MIXER	To mix eight signals into one	10mA	£5.15	E0.73
нүв	STEREO MIXER	Two channels, each mixing five signals into one	10mA	£6.25	£0.94
нуэ	STEREO PRE AMP	Two channels mag. Cartridge/ Mic+Volume	10mA	£6.70	£1.0
HY11	MONO MIXER	To mix five signals into one + Bass/Treble controls	10mA	£7.05	£1.0
*HY12	MONO PRE AMP	To mix four signals into one - Bass/Mid-range/Treble	10mA	£6.70	£1.0
*HY13	MONO VU METER	Programmable gain/LED overload driver	10mA	£5.95	£0,8
НҮ66	STEREO PRE AMP	Mic/Mag. Cartridge/Tape/Tunet/Aux + Volume/Bass/Treble/Balance	20 mA	£12.19	£1.8
HY67	STEREO HEADPHONE	Will drive headphones in the range of 4Ω = 2ΚΩ	80mA	£12.35	£1.8
HY68	STEREO MIXER	Two channels, each mixing ten signals into one	20mA	£7.95	£1.1
HY69	MONO PRE AMP	Two input channels of mag. Cartridge/ Mic + Mixing/Volume/Treble/Bass	20 mA	E10.45	£1.8
HY71	DUAL STEREO PRE AMP	Four channels of mag. Cartridge/Mic + Volume	20 mA	£10.75	£1.6
*HY72	VOICE OPERATED STEREO FADER	Depth/Delay	20 mA	£13,10	£1.5
*HY73	GUITAR PRE AMP	Two Guitar (Bass/Lead) and Mic + separate Volume/Bass/Treble + Mix	20 mA	£12.25	£1.8
+HY74	STEREO MIXER	Two channels, each mixing five signals into one + Treble/Bass	20 mA	£11,45	£1.
†HY75	STEREO PRE AMP	Two channels, each mixing four signals into one – Bass/Mid-range/Treble	20 mA	£10.75	£1.
+HY76	STEREO SWITCH MATRIX	Two channels, each switching one of four signals into one	20mA	7ohe.	дісполіті е
+HY77	STEREO VU METER DRIVER	Programmable gain/LED	20mA	£9,25	E1.

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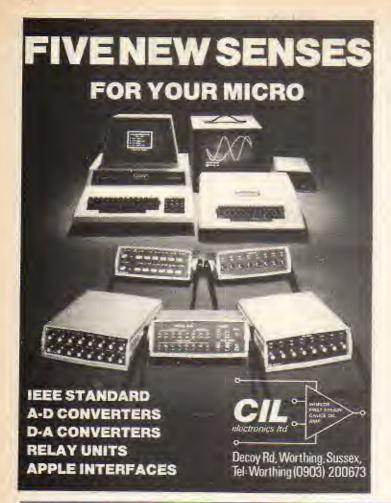
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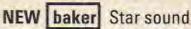
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EC52 EC91	3.40	PARC80 0.60 PC85 0.75	ULS4 0.95 6F6GB	2.80 20E1 1.30 epecial V
ECC81 ECC82	0.85 0.65 0.60	PC95 0.95 PC98 0.95 PC97 1.50 PC900 1.15	UY82 0.70 6F12 UY80 0.85 6F14	1.50 20P3 0.75 4CX 1000A 1.15 20P4 1.25 4CX 5000A
ECC83 ECC84 ECC85	0.65 0.60 0.60	PCC89 0.86	VR105/30 SF15 1.25 GF17 VR150/30 1.35 SF21 X65 0.96 SF24	1.30 20P5 1.35 BM 25L 1.15 28LeGT 0.95 BW 153 0.75 2624G 0.76 DM 26LB
ECC98 ECC189	0.80 0.95	PCC189 1.05 PCF80 0.80 PCF82 0.70	X61M 1.76 6F33 XR1.64Y0A 0FHS	1.75 30C15 0.50 11 1420 10.50 30C17 0.50 YL1430 4.20 30C18 2.45 YL 1440
ECC804 ECF80 ECF82	0.90 0.85 0.65	PCF84 0.75 PCF86 1.50 PCF87 0.50	82.90 6GA8 2759 19.00 6GH8A 2749 0.75 6H6	0.90 30F5 1.16 GXU 6 0.95 30FL2 1.40 CV1597
ECH34 ECH35	1.05 2.25 1.70	PCF200 1.60 PCF201 1.65 PCF800 0.50	2800J 3.45 GJ4 2801U 3.75 GJ4WA 2803U 16.00 6J5	200 30L15 1.10 BR 179 230 30L15 1.10 CV 5131
ECH42 ECH81 ECH84	1.20 0.70 0.80	PCF801 1.75 PCF802 0.85 PCF805 2.45	2900T 2.45 6.5GT 1A3 0.85 6.6	0.90 30P12 1.16 GMU 2 0.65 30P1 13 126 TY4-500
ECLBO ECLB2 FCLB3	0.70 0.75 1.40	PCF805 1.20 PCF808 2.76 PCH200 1.35	195 0.60 6JESC 154 0.45 6JSCC	0.90 30FL14 2.46 BK445/5052A 2.95 35L0GT 1.40 Mt 5948/1754 2.95 35W4 0.80 IC
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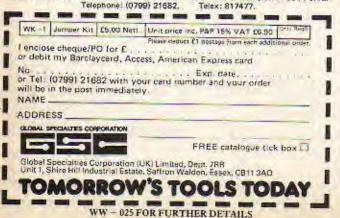
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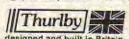
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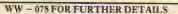
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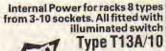


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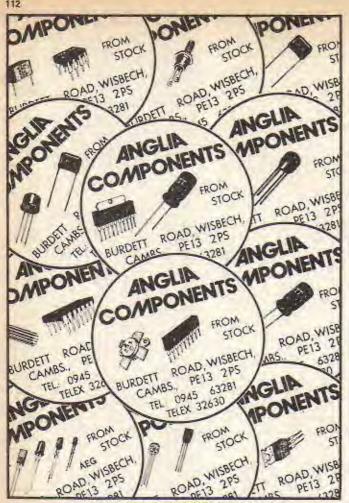
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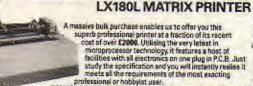
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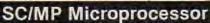


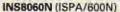
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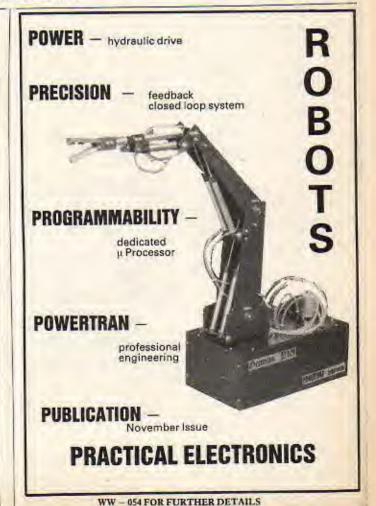
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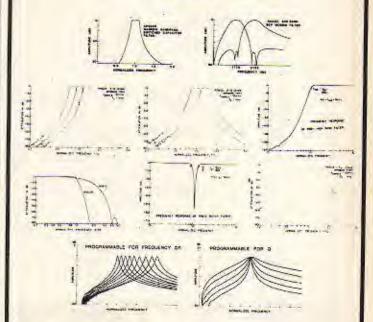


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