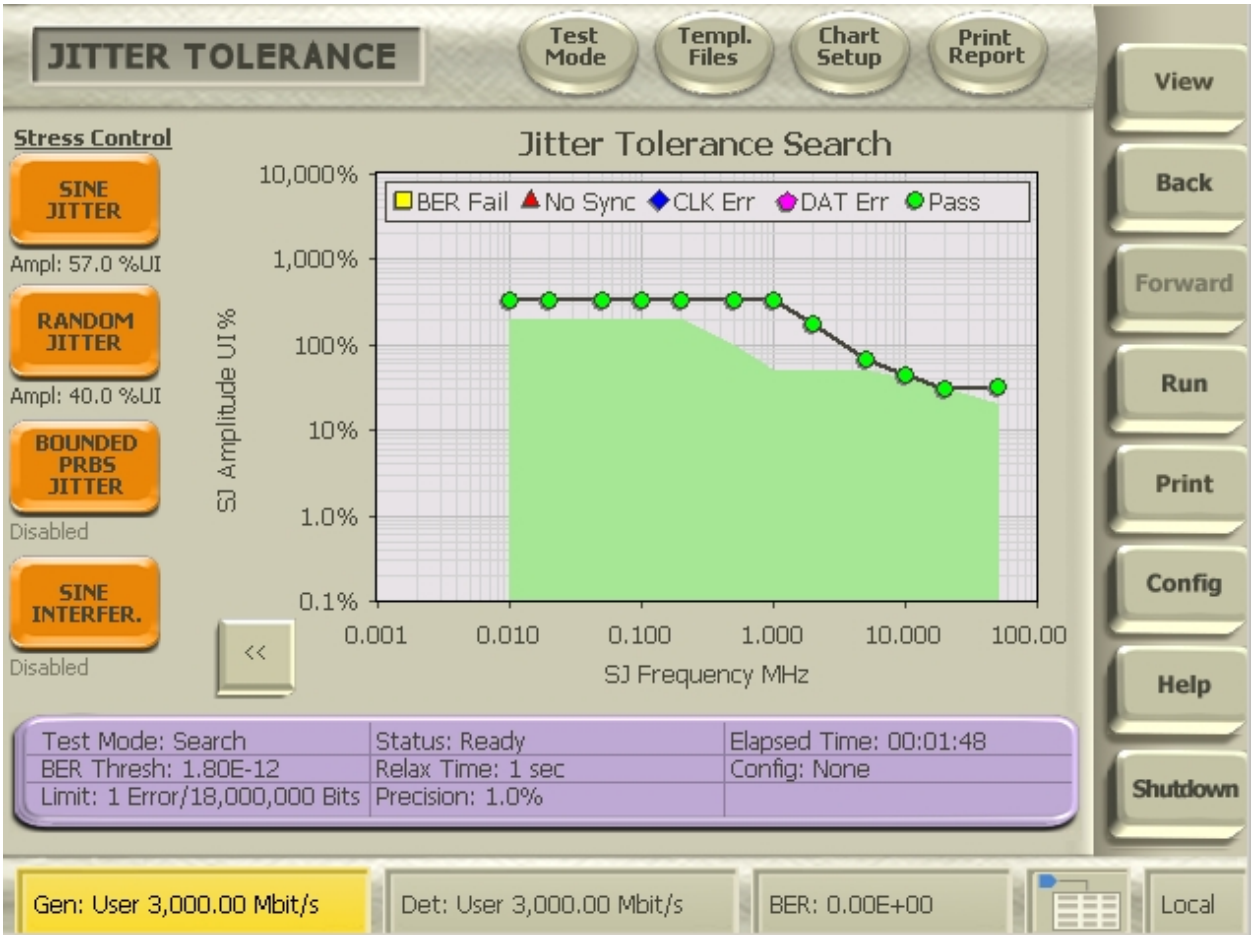
SyntheSys Research, Inc.

Serial ATA International Organization

Version 1.0
June 4, 2009

Serial ATA Interoperability Program Revision 1.4 SyntheSys Research, Inc. MOI for RSG Tests (using BERTScope 7500B with SSC option and CR)



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MODIFICATION RECORD

Revision 1.2, Version 0.8, April 11, 2007
Revision 1.2, Version 0.9, April 26, 2007; Added Grab mode to track disparity and count re-synchronizations to the pattern to get FER; Added "While the Interop testing require the use of the Pretest_MOI_Framed_COMP" and "informatively" to the last paragraph on page 10; Moved Host Worst Port Identification to Appendix with the addition of the following text: "The "worst port" identified during a Pre-test should be used. If pre-test has not yet been run then the following method, which follows and complies with the pre-test "worst port" identification procedure, is applied prior to execution of any testing on a host."
Revision 1.2, Version 0.91, July 23, 2007; Added the words "with an initial amplitude of 1 Vpp" and "determined during calibration" to respectively steps 4 and 9 and changed "desired data rate" to "maximum claimed data rate" in steps 2 and 3 of the test procedure.
Revision 1.2, Version 0.92, August 2, 2007; deleted "Testing results gathered for 33 MHz are informative."
Revision 1.2, Version 1.0RC, August 2, 2007.
Revision 1.2, Version 1.0, September 2, 2007; removed "RC" after workgroup approval and end of 30 day review.
Revision 1.3, Version 0.9, October 23, 2008; SATA Gen 1m and Gen 2m (eSATA) updates
Revision 1.3, Version 0.91, December 4, 2008; Added +350 ppm test to RSG01 and RSG02, step 4 to the Calibration procedure and changed to LBP for the Calibration of Total Jitter and amplitude.
Revision 1.3, Version 0.92, December 4, 2008; Changed +350 ppm to 0 ppm, removed wavier statement and added 62 MHz SJ to the receiver tolerance with frequency offset test.
Revision 1.3, Version 1.0RC, December 18, 2008. Updated to 1.0RC as MOI was approved to release candidate status.
Revision 1.3, Version 1.0RC, February 13, 2009. Moved from RC to fully approved after completion of 30 days all members review.
Revision 1.4, Version 0.8, March 25, 2009. Updated with references to Serial ATA Revision 3.0 including new sections RSG-03 and RSG-06
Revision 1.4, Version 0.9, March 26, 2009. Updated picture on page 7 and typos on page 11 per workgroup review.
Revision 1.4, Version 0.91, May 19, 2009. Updated per latest draft of UTD1.4 including adjustment of 1.5 Gb/s and 3.0 Gb/s SJ values, updated BIST tools for 6 Gb/s support, and inclusion of verification of retimed versus analog loopback.
Revision 1.4, Version 0.92, May 25, 2009. Increased number of frames tested from 6 to at least 18 during frequency offset and SSC tests and inserted Appendix D – Validation of Lab Source Return Loss.
Revision 1.4, Version 0.93, June 2, 2009 Removed Appendix D – Validation of Lab Source Return Loss.
Revision 1.0RC, June 4, 2009. Removed Serialtek as BIST Stimulus Tool and change "protocol analyzer" to "protocol generator" in Appendix A. After vote by the LOGO Interop work group.

INTRODUCTION

These Methods of Implementations describe the step by step procedures to perform the RSG-01 through RSG-06 tests of the Serial ATA Interoperability Program using the BERTScope by SyntheSys Research, Inc. to qualify a product, host or device, for listing on the SATA Integrators List. Described methods can test products which support disconnect as well as products without support of disconnect.

The test setup is illustrated in Appendix C.

The Framed COMP pattern used for Interoperability Testing is the pattern defined in the Unified Test Document revision 1.4 which can be found at http://www.serialata.org/testing.asp

The tests can be performed in automated fashion using Jitter Tolerance software available on the BERTScope. Please contact SyntheSys Research, Inc. at +1 (650) 364-1853 or info@bertscope.com for the latest information on such software.

REFERENCES

The following documents are referenced in this text:

[1] Serial ATA Revision 3.0
[2] Serial ATA Interoperability Program Unified Test Document, Interop_UnifiedTest_Rev1.4
[3] Serial ATA Interoperability Program Policy Document, Interop_Policy_Rev1_4
[4] SATA_PHY_MOI_BERTScope_PHY_TSG_OOB_r14

The most current versions of above documents may be found at the Serial ATA document repository:
http://www.serialata.org/testing.asp

ACKNOWLEDGEMENTS

The SATA-IO would like to acknowledge the efforts of the following individuals in the development of:

The content, tests, software and hardware implementation of this test suite:

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The **Pre-test document and procedures:**

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Test Title: RSG-01 Gen1 (1.5Gb/s): Receiver Jitter Tolerance Test
Test Title: RSG-02 Gen2 (3Gb/s): Receiver Jitter Tolerance Test
Test Title: RSG-03 Gen3 (6Gb/s): Receiver Jitter Tolerance Test
Test Title: RSG-05 Receiver Stress Test at +350ppm
Test Title: RSG-06 Receiver Stress Test with SSC

Purpose: Verify that the Product Under Test, PUT, meets the receiver tolerance specification of sections 7.2.2.5.7 and 7.3 of Serial ATA Revision 3.0 at 1.5 Gb/s and 3 Gb/s plus sections 7.2.2.5.8 and 7.3 of Serial ATA Revision 3.0 at 6 Gb/s if the PUT claims to support both rates.

Resource Requirements:

- See Appendix E

Signal Calibration:

- The setup shall be calibrated using the Calibration section of this document prior to start of the test as the calibrated settings are used throughout the test.

Last Modification: May 25, 2009

Discussion: This requirement is tested at all the interface rates which the PUT claims to support, i.e. at 6 Gb/s and 3 Gb/s and 1.5 Gb/s. The BERTScope automatically steps the jitter frequency and verify compliance according to section 7.2.2.1.2 of the Serial ATA Revision 3.0. Described methods can test product which support as well as products without support of disconnect.

Prior to execution of any testing on a host, a "worst port" must be identified. The "worst port" identified during a Pre-test should be used. If pre-test has not yet been run then the method in Appendix B, which follows and complies with the pre-test "worst port" identification procedure, is applied prior to execution of any testing on a host.

During the testing execution for all RSG test requirements, it is essential that the product under test be allowed to complete an initial OOB sequence through the device COMWAKE prior to transmission of a BIST FIS or initiation of the BIST mode sequence. This is to allow product calibration to occur prior to and/or during the initial power on and detect sequences. Several different patterns are defined within the specification to verify the receiver tolerance. In order to ensure efficient test time of products within the Interoperability Testing, testing will be limited to the Framed Long COMP. For consistent transmission of the Framed Long COMP pattern, it is required that 2 ALIGNs are transmitted prior to SOF of the frame, and then subsequently every 256 Dwords. Pretest_MOI_Framed_COMP, pattern in the SATA directory on the BERTScope, contain these features.

Four tests are run. Steps 1 through 10 of the test procedure detail the Receiver Data Detection Tolerance portion of the test. Steps 11 through 13 describe the Receiver Tolerance at +350 ppm Frequency Offset portion of the test. Step 14 repeats the test at with SSC. All tests shall be met.

Connect Test Setup as shown in Appendix C:

Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the CR 12500A full rate clock output to the BERTScope external clock input using the medium length SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables.

Connect the CR 12500A Data Input + and – ports to the respective Instrument RX + and - ports of the SATA Tee via one of the pairs of matched of SMA Male to Male Cables.

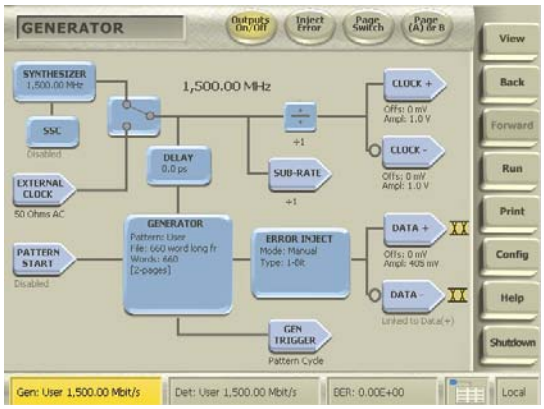
Connect the Instrument TX + and – ports of the SATA Tee via the BERTScope ISI board (17" lines of the for 6 Gb/s, lines found during calibration per Appendix A for 1.5 Gb/s and 3.0 Gb/s) and the rise time filters to the respective BERTScope Data Output + and – ports via one of the pairs of matched of SMA Male to Male Cables.

Connect the iSATA receptacle-to-SMA-adapter via the four SMA Male to SMA Male adapters to the PUT side of the SATA Tee. The A+ and A- ports of the iSATA receptacle, these are the pins marked 2 and 3 respectively, would be connected to the respective PUT RX Input + and - ports of SATA Tee for drive testing (to PUT TX for host testing). The B+ and B- ports of the iSATA receptacle, these are the pins marked 6 and 5 respectively, would be connected to the respective PUT TX Input + and - ports of SATA Tee for drive testing (to PUT RX for host testing).

Test Procedure:

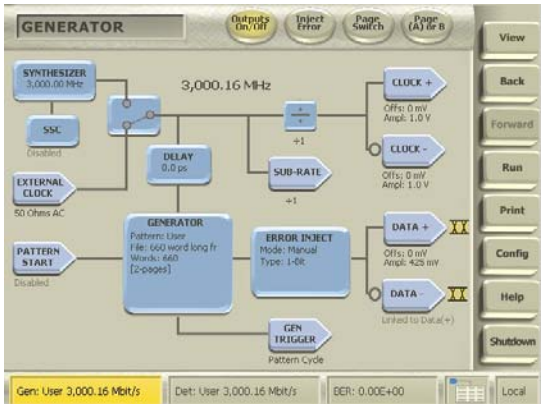
Receiver Data Detection Tolerance Test:

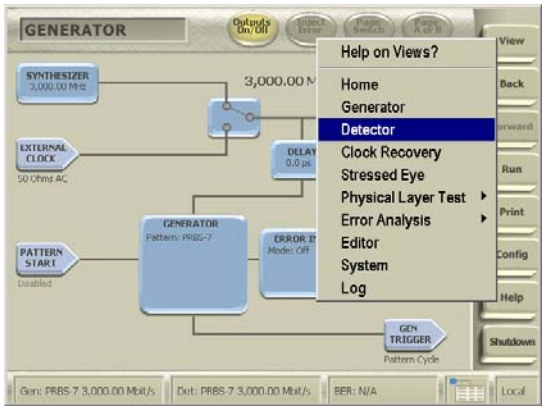
1. Connect the PUT to the setup via the iSATA receptacle
2. Initiate the PUT in the BIST L mode at the maximum claimed data rate as described in Appendix A. Note: In most cases the BERTScope with the SATA Tee can do this as per Appendix A.
3. On the BERTScope, select "View" then "Generator". Click on the "Generator" box then "User Pattern" and "Load User Pattern" and select the "Pretest_MOI_Framed_COMP" pattern from the "SATA_II" folder. Set the "Synthesizer" frequency to match the claimed data rate being tested. Enable the data outputs at or above the desired amplitude, which was determined during calibration. In the "Stressed Eye" view enable the SJ at 0%.



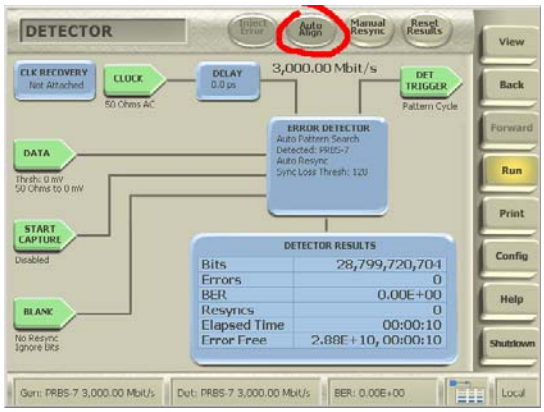
4. Once the BERTScope data output ports have been enabled with the initial amplitude of 1 Vpp then move the switch on the SATA Tee to the BERTScope position (this can be done either manually or via the electronic input on the SATA Tee).

5. On CR 12500A, choose the appropriate pre-stored selection: "SATA1 (1.98)" for 1.5 Gb/s or "SATA2 (1.98)" for 3 Gb/s or "SATA3 (1.98)" for 6 Gb/s; by pressing "Enter", scroll to the desired setting and press "Enter" again. These settings should be 1.98 MHz of closed loop bandwidth with 2.09 dB of peaking and phase error limit set to 90%. On the CR 12500A also set the sub-rate clock divider to 1 by scrolling to "SubDiv: 4" press "Enter" select "1" and press "Enter" again.
6. Once the CR 12500A is locked then click the switch in the BERTScope "Generator View" to select "External Clock Input" The PUT input data rate will now be identical to the PUT data output rate.





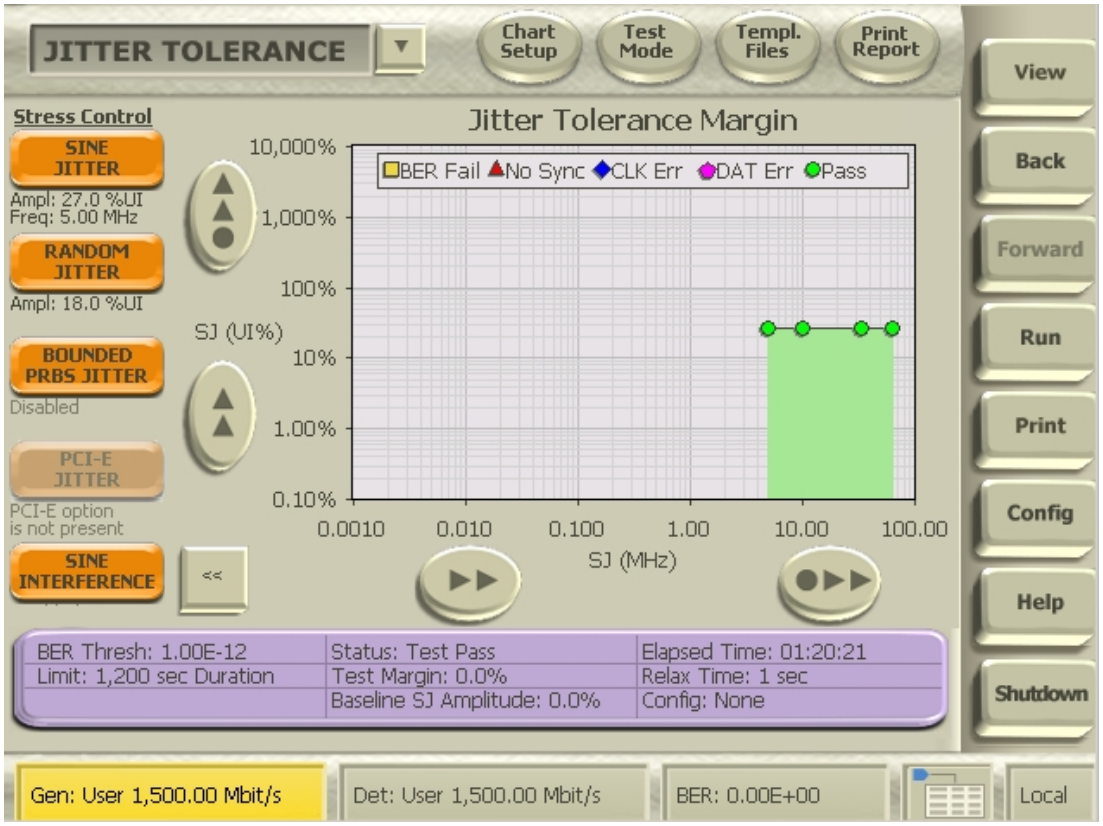
7. On the BERTScope, select “View” then “Detector” and click on “Auto Align”.



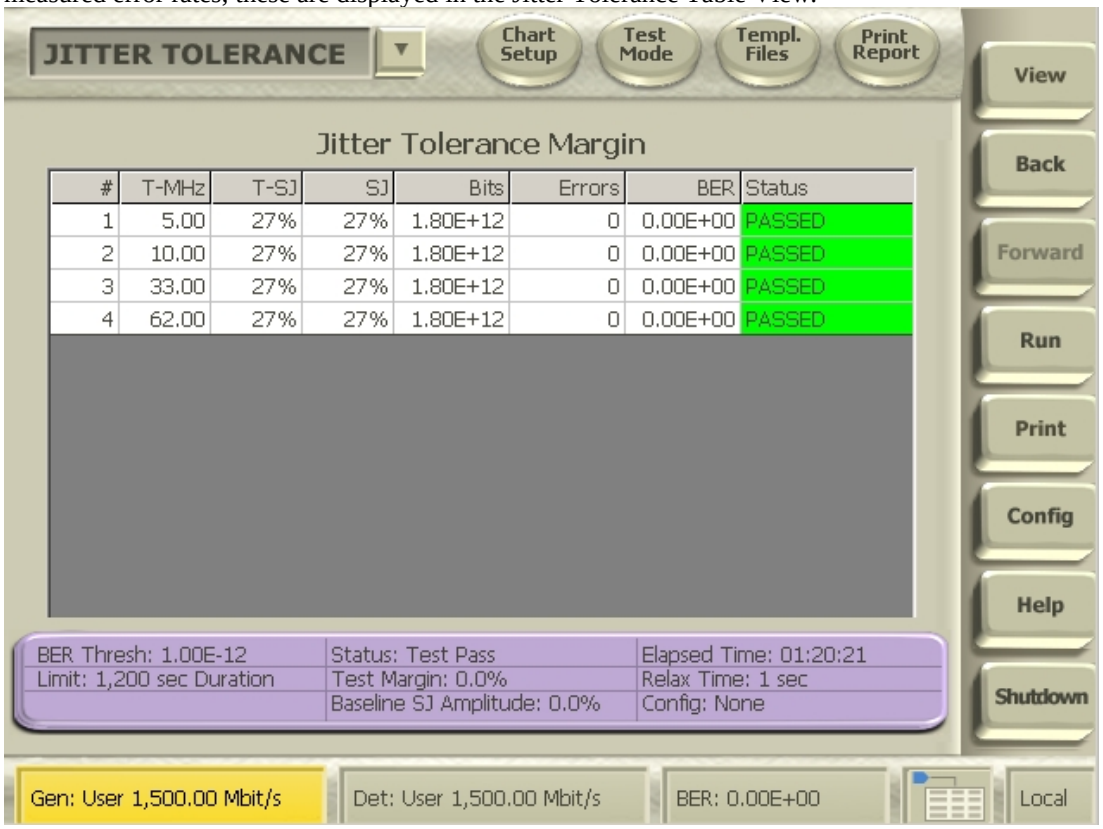
A pop-up window will appear with the Unit Interval measurement result. Click OK to close the pop-up window.

8. The detector should be running at zero bit error rate when 0% jitter is presented. Set the “Detector” “Pattern” to “Grab” (it will by default grab the length of the Pretest_Framed_COMP pattern while now tracking the disparity of the pattern returned by the PUT. The number of Resyncs will be recorded as frame error rate, FER). Verify that the PUT is in loopback mode by injecting a single error from either the “Generator” or “Detector” view and detect that one or more errors occur..
9. Select to have the “Stress” show as a side bar in the “Eye Diagram” view. Set the SJ frequency to 62 MHz. To verify that the PUT is in retimed and not in analog loop back mode; briefly increase the SJ level to 27% and see that the jitter level does not increase.
10. Decrease the generator amplitude to the desired level determined during calibration and start the “Jitter Tolerance” configuration, which was saved during calibration, associated with the data rate being tested. The Jitter Tolerance software will automatically step through and make the jitter tolerance tests for the prescribed time at each of the 4 jitter frequencies per the following Table:

	1.5 Gb/s	3.0 Gb/s	6.0 Gb/s (informative)
5 MHz	10 Minutes (RSG-01d)	5 Minutes (RSG-02d)	2.5 Minutes (RSG-03d)
10 MHz	10 Minutes (RSG-01a)	5 Minutes (RSG-02a)	2.5 Minutes (RSG-03a)
33 MHz	10 Minutes (RSG-01b)	5 Minutes (RSG-02b)	2.5 Minutes (RSG-03b)
62 MHz	10 Minutes (RSG-01c)	5 Minutes (RSG-02c)	2.5 Minutes (RSG-03c)

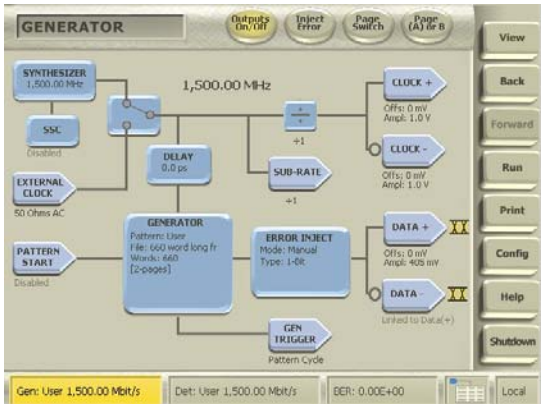


11. The Receiver Data Detection Tolerance Test takes approximately 1 hour 10 minutes. Record the measured error rates; these are displayed in the Jitter Tolerance Table View.



Receiver Tolerance at Frequency Offset Tests:

12. Leave the 62MHz SJ on set at its calibrated value. Set the "Synthesizer" frequency in the BERTScope "Generator View" to the nominal interface rates +350 ppm offset. Now change the switch to select using the built-in synthesizer instead of "External Clock Input".



13. Go to "View" then "Editor" and "Capture by Length". Set the capture "Length" to 65,536 words of 128 bits (8,388,608 bits total). These lengths correspond to at least 18 full frames of the compliance pattern .
14. Analyze the captured data and record the number of frame errors.
15. Repeat steps 11 through 13 with 30 kHz triangular SSC at -350 ppm to -5350 ppm downspread, i.e set at -350 ppm offset with -5000 ppm downspread.
16. Repeat steps 2 through 14 at each of the interface rates which the DUT claims to support, respectively 6.0 Gb/s, 3.0 Gb/s and 1.5 Gb/s. The values recorded at 1.5 Gb/s from steps 11 through 14 are also the test results for respectively RSG-05 and RSG06.

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Observable Results: The pass/fail criteria are:

- The Receiver Data Detection Tolerance Test is run for respectively 4 times 10 minutes at 1.5 Gb/s, 4 times 5 minutes at 3.0 Gb/s and 4 times 2.5 minutes at 6 Gb/s (informative) and verified to exhibit no more than zero frame errors at each of the 5 MHz, 10 MHz, 33 MHz and 62 MHz frequencies above and
- The Receiver Tolerance at Frequency Offset Tests are run at +350 ppm frequency offset and with 30 kHz triangular SSC at -350 ppm to -5350 ppm downspread from all the nominal interface rates which the PUT claims to support, respectively 6 Gb/s (informative), 3 Gb/s or 1.5 Gb/s, for at least 18 consecutive frames and the returned data sets have been verified to exhibit no more than zero frame errors.
- The RSG-05 (informative) Test is run at +350 ppm frequency offset from nominal 1.5 Gb/s interface rate for at least 18 consecutive frames and returned data has been verified to exhibit no more than zero frame errors.
- The RSG-06 (informative) Test is run with 30 kHz SSC at -350 ppm to -5350 ppm downspread from nominal 1.5 Gb/s interface rate for at least 18 consecutive frames and returned data has been verified to exhibit no more than zero frame errors.

Accuracy: FER confidence depending on the total test time, 10 minutes test without error at each setting was selected for Serial ATA LOGO testing at 1.5 Gb/s and proportionally less time at the higher data rates to achieve the required confidence. Optionally a FER counter can be directly connected to the BERTScope SATA Tee to count in parallel with the BERTScope.

Possible Issues: While the Interop testing require the use of the Pretest_MOI_Framed_COMP if the device does not support the Pretest_MOI_Framed_COMP then the Pretest_MOI_Framed_COMP_with_4_ALIGNs version or the Long version of the COMP pattern per section 7.2.4.3.6 of Serial ATA Revision 3.0, may be used to informatively verify the receiver tolerance level of the PUT. Location of bit errors within the frame may be monitored in the "Pattern Sensitivity" view.

Calibration

Purpose: Calibrate the test setup before making any RSG-01 through RSG-06 tests.

Resource Requirements:
- See Appendix E

Last Modification: May 19, 2009

Discussion: This calibration must be done prior to running any RSG-01 through RSG-06 tests.

Tester must save all the calibration data (i.e. screen shot) that is done daily at a minimum, if not for every device evaluation. Valid calibration data must be available per product for review, even if the same calibration data (i.e. daily) is used for multiple products. It is required that calibration be completed for this area of testing to ensure consistent measurements and environment impacts.

The reference plane is the end of the 50 ohm SMA cables that will be connected to the SATA-SMA test fixture.

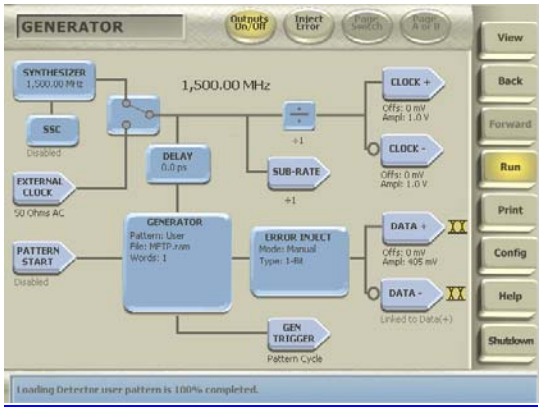
The following parameters are to be used for creating the appropriate input source involved in the RSG tests (see Table 33 in Section 7.2.1 of SATA Revision 3.0 for specification requirements):
- No SSC
- Pre-emphasis: 0 dB
- No CDR (Clock Data Recover unit) to be used for jitter calibration. The BERT detector uses a 1.5 or 3 GHz square wave direct from the clock output dependent on the data rate.
- Rise/Fall Time: 100 ps (20/80%) for Gen1 and Gen2 or between 62 ps and 75 ps (20/80%) for Gen3.

Test Setup: as shown in Appendix C and further described in Test Titles RSG-01 through RSG-06 with the exception that the SATA Tee Output + and – ports (which usually are connected to the Comax adaptor) will be connected directly to the BERTScope Data Input + and – ports and the BERTScope Clock Output + will be connected to the BERTScope Clock Input port to provide the direct clock as required for Interop calibration.

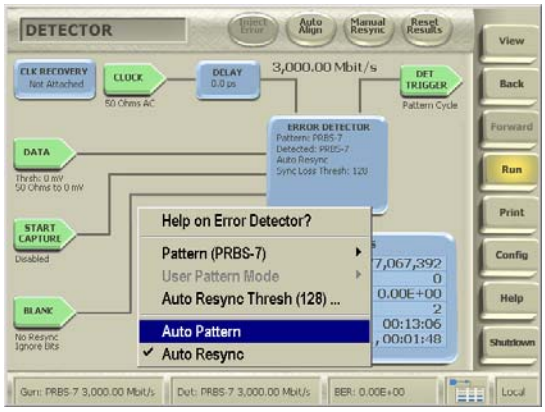
Calibration Procedure:

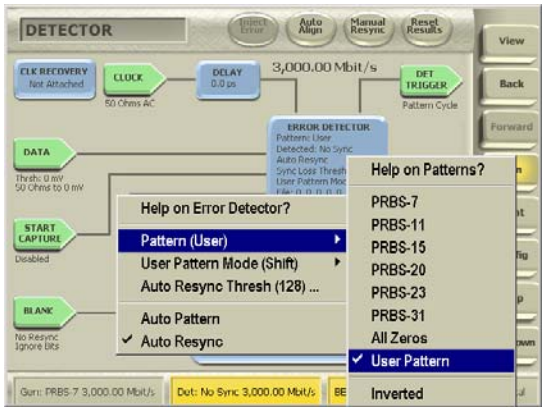
The following high level procedure is used to implement the defined Receiver Tolerance test:

1. Turn the BERTScope clock on at 1 V nominal amplitude and the desirable data rate 1.5 GHz or 3 GHz.

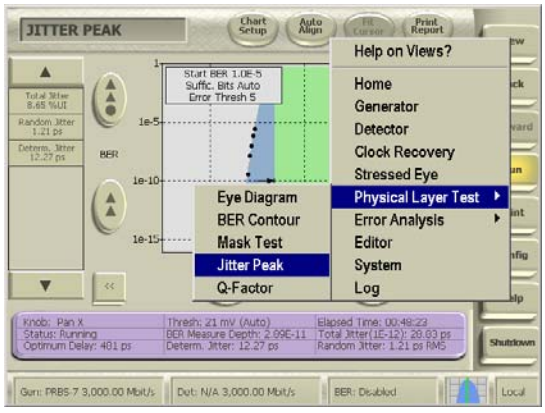


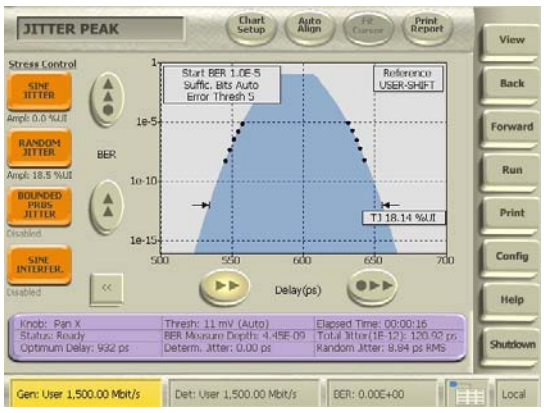
2. Select the Mid Frequency Test Pattern (MFTP) from the “Generator” view with an approximate differential voltage of 325 mV for Gen1i (1.5 Gb/s iSATA) or 275 mV for Gen2i (3.0 Gb/s iSATA) or 240 mV for Gen3 (6.0 Gb/s iSATA), Gen1m and Gen2m (eSATA) for the SJ and RJ calibrations. The MFTP is stored as a “User Pattern” in the “SATA II” directory.



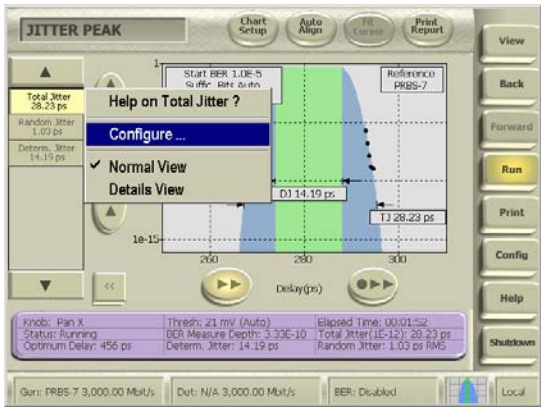


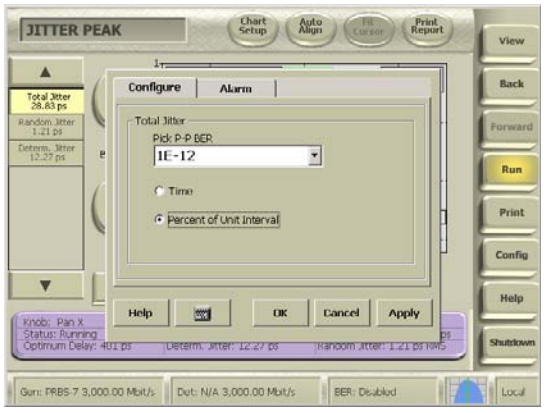
3. Use the LFTP pattern to verify that the rise and fall times are approximately 100 ps 20%/80% for Gen1 and Gen2 or between 62 ps and 75 ps 20%/80% for Gen3.
4. Set the starting BER to 1E-6 by clicking on the "<<" icon, selecting "Advanced" and "Starting BER"
5. Select to have the "Stress" show as a side bar in the "Jitter Peak" view. Enable the sinusoidal jitter (SJ) source. Set the SJ frequency to 62 MHz, but set the level to 0% to obtain the 0% stress reference level.
6. On the BERTScope, select "View" then "Physical Layer Test" and "Jitter Peak" and click on "Auto Align". Click "Yes" to perform delay line calibrations if prompted by a pop-up window. Wait until at least three points has been measured on each side of the Jitter Peak and record the TJ value in UI.





The measurement units can be altered from pico seconds to UI by right click on "Total Jitter" on the left side bar; then click on "Configure", select "Percentage Unit Interval", click "OK".

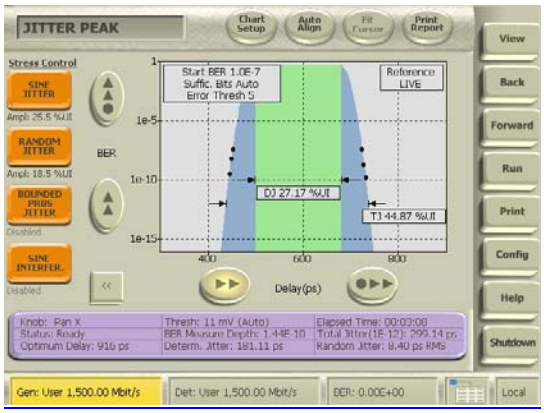




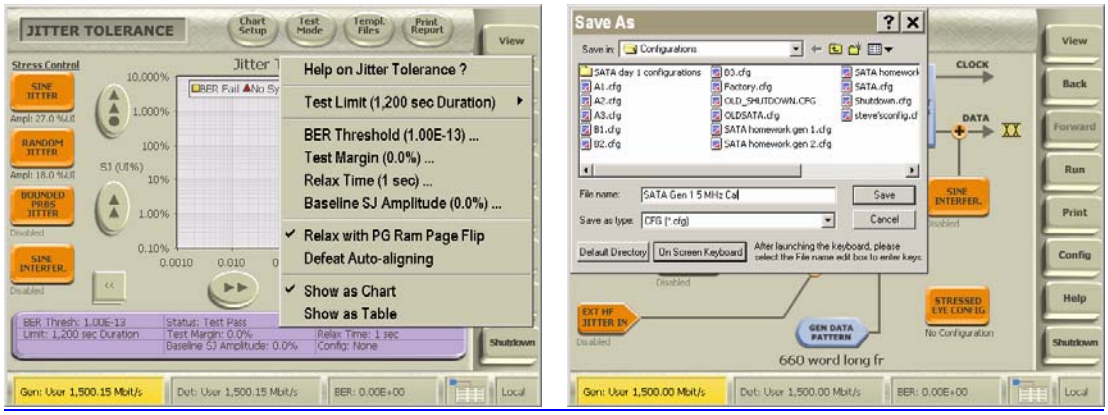
7. All calibration screen shots need to be saved. This is done by clicking on “Print” and select “Print to file” then create a unique file name for each calibration data including the serial number of the equipment.
8. Increase the SJ and repeat the TJ measurement of steps 6 and 7 until the TJ has increased by the desired SJ value, either 27% UI or 16.1% UI per the following table:

	Test point	Pattern	Gen1i/Gen1m	Gen2i/Gen2m	Gen3
Rise/fall time	TP1	LFTP	100 ps (20/80%)	100 ps (20/80%)	62 ps to 75 ps (20/80%)
RJ	TP1	MFTP	18% UI	18% UI	18% UI
SJ	TP1	MFTP	27% UI	27% UI	16.1% UI
TJ	TP2	LBP	50.1 to 51.9% UI	55.2 to 58.8% UI	49.8 to 57.0% UI
Amplitude	TP2	LBP	240 mV (Gen1m) 325 mV (Gen1i)	240 mV (Gen2m) 275 mV (Gen2i)	240 mV (Gen3)
Max. Voltage	TP2	LBP	600 mV	750 mV	1 V

9. Record the instrument setting of the SJ level and repeat step 8 and 9 while adjusting the SJ frequency to respectively 62 MHz, 33 MHz, 10 MHz and 5 MHz and setting amplitude to get the desired value.
10. Adjust the Random Jitter (RJ) still using (MFTP) pattern until the TJ measured has increased by another 18% UI due to the random jitter.
    i. NOTE: Gen1 : 8.57 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)
    ii. NOTE: Gen2 : 4.285 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)
    iii. NOTE: Gen3: 2.14 ps RMS (1 sigma for a 7 sigma 0.18 UI projection)
11. Connect the BERTScope ISI Board (17” lines for 6 Gb/s and lines or combinations, normally the 24” lines for 3.0 Gb/s and the 31” lines for 1.5 Gb/s, that generated close to 40 ps ISI for 1.5 Gb/s or 3.0 Gb/s) after the rise time filters. The 40 ps ISI with the Lone Bit Pattern (LBP) for the 1.5 Gb/s and 3.0 Gb/s interface rates can be measured using Jitter Map if available or the Jitter Measurement of the Eye Diagram (preferably CleanEye).
12. Verify that the Total Jitter (TJ) meets the value of above table using the Pretest_MOI_Framed_COMP pattern, 51% UI nominal for Gen1 or 57% UI nominal for Gen2 and Gen3. Adjust the ISI if needed.



13. Finally using “Q-Factor” view with the “Data Generator” sidebar enabled adjust the amplitude so that the Differential Voltage of the smallest bit of the Lone Bit Pattern (LBP) pattern (LBP portion of TSG-01 method) is respectively: 325 mV for Gen1i (1.5Gb/s iSATA), or 275 mV for Gen2i (3 Gb/s iSATA) or 240 mV for Gen3i (6 Gb/s iSATA), Gen1m and Gen2m (eSATA). Confirm that the maximum differential voltage does not exceed 600 mV for 1.5 Gb/s or 750 mV for 3.0 Gb/s or 1000 mV for 6.0 Gb/s respectively. The resulting signal must meet the required parameters outlined in Table 13 of the Unified Test Document Revision 1.4 (namely Rise/Fall Time, Voltage etc.).
14. Record the jitter settings and enter these in the Jitter Tolerance Template Builder. Set the “Jitter Tolerance” “Test Limit” to respectively 600 seconds (10 minutes) for 1.5 Gb/s or 300 seconds for 3.0 Gb/s or 150 seconds for 6 Gb/s set pattern to the Pretest_MOI_Framed_COMP and save the calibrated configuration.



Above steps are repeated for calibration of the signal at each interface rate. The stored Jitter Tolerance Template configuration will run the RSG test automatically at the 4 jitter frequencies for the respectively 10, 5 or 2.5 minutes each following the interface rate.

Appendix A: BIST

Initiation of PUT using BIST L mode.

Purpose: Place the PUT in the BIST L mode as an initiation before the BERTScope measurements.

References:
1. Serial ATA Revision 3.0, section 10.3.9 BIST Active
2. U-Link Operating Help Files
3. Catalyst BIST MOI

Resource Requirements:
- SATA Tee for testing of PUTs without support of disconnects.
- Stimulus Tool: Any device or system capable of :
  i. Generating SATA OOB, negotiate speed and bringing the PUT to a state where it can receive a BIST Activate FIS.
  ii. Generating the required BIST Activate FIS for BIST L mode.

Examples of Stimulus Tools:
- BERTScope.
- AMD SB800 or equivalent 6 Gb/s capable host controller with U-Link DriveMaster 2008 software version 4.0.390 or above.
- Intel 6 Gb/s SATA enabled computer with NazBIST
- SCT-BIST Drive
- Serial ATA Protocol Generator
  a. Finisar Xgig

Last Modification: June 4, 2009

Discussion: The BERTScope acts as a monitoring tool fully capable of verifying the patterns transmitted by the PUT and as a stimulus tool to generate SATA OOB, negotiate speed and issue the BIST Activate FIS in according to section 10.3.9 of the Serial ATA revision 3.0. When the BERTScope is used then there is no need for the SATA Tee as there will not be any disconnects.

The advantage of using a ULink BIST Initiation tool is that the combination of BERTScope and ULink provides a complete Digital and PHY/TSG/OOB and RSG test solution.

Test Setup: Stimulus Tool with an iSATA cable.

Test Procedure:
1. Connect PUT to the Stimulus Tool using the SATA cable (via the SATA Tee if the PUT is without support of disconnect).
2. Make sure that the Stimulus Tool is turned on and ready.
3. Allow the PUT to power up and go through OOB.
4. Initiate speed negotiation using the Stimulus Tool if change of speed is required.
5. Generate a BIST Active FIS with the appropriate bits set for BIST L as required using the Stimulus Tool. This might be done using a BERTScope.

10.3.9 BIST Activate - Bidirectional

0	Reserved (0)								Pattern Definition T	A	S	L	F	P	R	V	R	R	R	R	PM Port				FIS Type (58h)							
1	Data1 [31:24]								Data1 [23:16]								Data1 [15:8]								Data1 [7:0]							
2	Data2 [31:24]								Data2 [23:16]								Data2 [15:8]								Data2 [7:0]							

Figure 197 – BIST Activate - Bidirectional

Field Definitions

FIS Type - Set to a value of 58h. Defines the rest of the FIS fields.

PM Port – When an endpoint device is attached via a Port Multiplier, specifies the device port address that the FIS should be delivered to or is received from. This field is set by the host for Host to Device transmission and this field is set by the Port Multiplier for Device to Host transmission. Endpoint devices shall set this field to 0h for Device to Host transmissions.

R - Reserved – shall be cleared to zero.

Pattern Definition

F – Far End Analog (AFE) Loopback (Optional)

L - Far End Retimed Loopback* Transmitter shall insert additional $ALIGN_P$ primitives

T - Far end transmit only mode

A - $ALIGN_P$ Bypass (Do not Transmit $ALIGN_P$ primitives) (valid only in combination with T Bit)

S - Bypass Scrambling (valid only in combination with T Bit)

P - Primitive bit. (valid only in combination with the T Bit) (Optional)

V - Vendor Specific Test Mode. Causes all other bits to be ignored

Data1 – Dword #1 of data information used to determine what pattern is transmitted as a result of the BIST Activate FIS. Applicable only when the T bit is set to one.

Data2 - Dword #2 of data information used to determine what pattern is transmitted as a result of the BIST Activate FIS. Applicable only when the T bit is set to one.

Example Using the U-Link Stimulus Tool:

1. Start the U-Link program
2. Click “Power Up” and observe the power supply spin up. Leave it on.
3. Click “CtlSATA”
4. Click COMRESET and observe that COMRESET was received on the log on the right side of the DriveMaster window..
5. Select the appropriate data rate “1” or “2” or “3” and observe that the “RDSTATUS” displays “00000113” or “00000123” or “00000133” for 1.5 Gb/s; 3 Gb/s and 6 Gb/s respectively.
6. Select the “BIST mode L” for RSG Testing
7. Click “BIST” and observe that “BIST FIS SUCEEDED” is displayed in the lower left corner of the SATA Control Panel.
8. PUT should now be ready for test.

Possible Issues: Some PUTs may require sequences of ALIGN words to be transmitted when switched from the U-Link initiation to the BERTScope set-up when doing RTL tests. This can be accomplished by using the pattern sequencing on the BERTScope having the A pattern be ALIGNs followed by the B pattern being the desirable test pattern. AB patterns are pre-stored on the BERTScope for this purpose.

Appendix B: Host Worst Port Identification

Purpose: Prior to execution of any testing on a host, a "worst port" must be identified. The "worst port" identified during a Pre-test should be used. If pre-test has not yet been run then the following method, which follows and complies with the pre-test "worst port" identification procedure, is applied prior to execution of any testing on a host.

Resource Requirements:

- One BERTScope 7500 or BERTScope 12500 with software version 10.0 or later
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8 or later
- One iSATA receptacle to SMA Female Adapter, ICT Solutions TF-1R21 or equivalent
- One short SMA Male to SMA Male Cable less than or equal to 12" length, Sucoflex 104 or equivalent
- A pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent.

Last Modification: March 25, 2009

Discussion: The intent of identifying a worst port is not to validate each port to the specification, but to simply identify the worst port based on a single relative jitter measurement across all ports within a host. The Interoperability Tests must then be executed on the worst port identified per the procedure below.

Test Setup as shown in Appendix B: Connect the CR 12500A sub-rate clock output to the BERTScope clock input using the short SMA Male to SMA Male Cable. Connect the Data Output + and - ports of the CR 12500A to the Data Input + and – ports of the BERTScope using the matched pair of cables. Connect both of the B+ and B- ports of iSATA receptacle, these are the pins marked 6 and 5 respectively, to SMA Adapter via the short matched pair of SMA Male to Male Cables to the respective CR 12500A Data Input + and - ports.

Test Procedure:

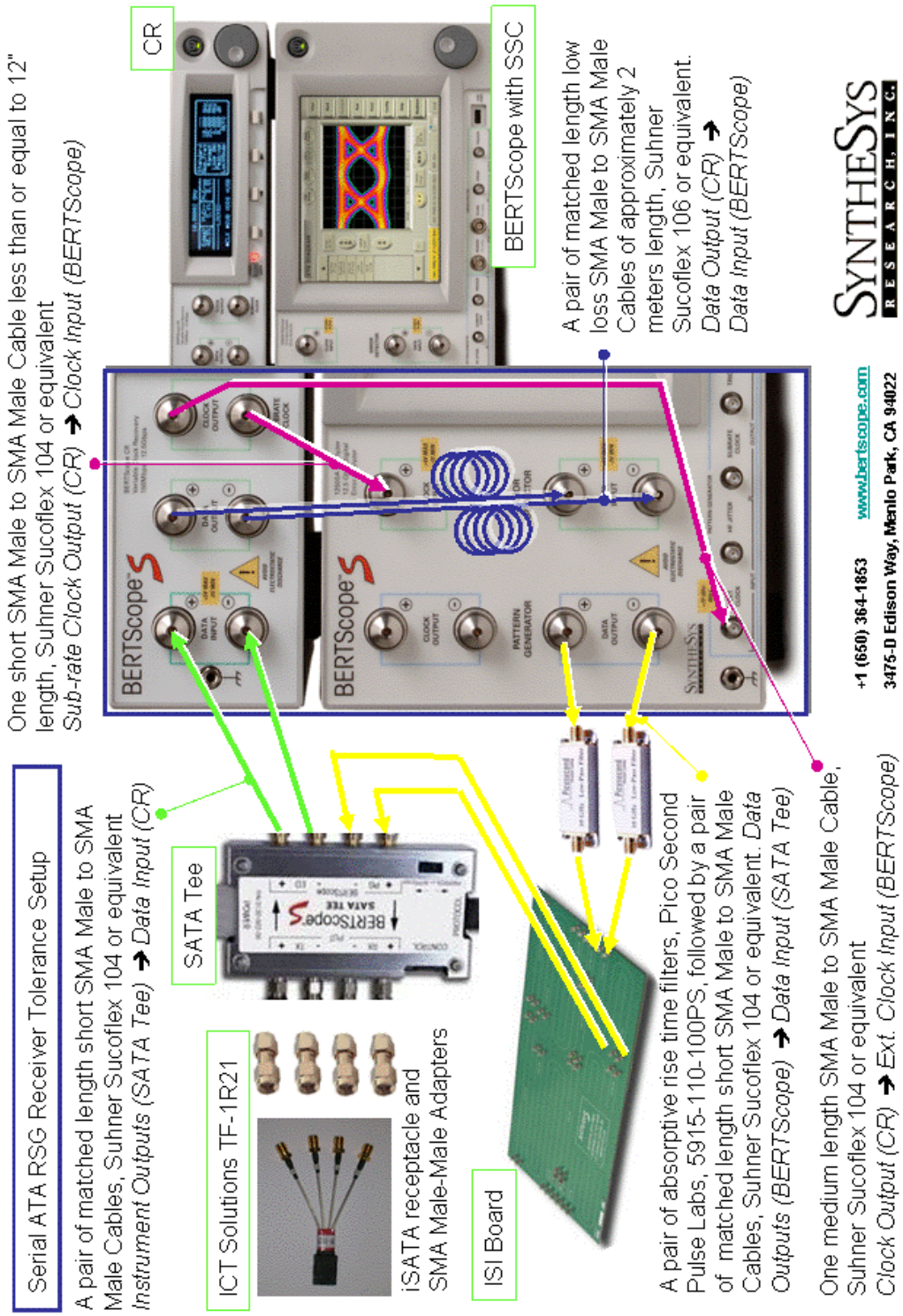
1. Power-on host and ensure test ports are enabled & functional. Run the following on each individual port.
2. Connect a 3.0 Gb/s device, i.e. HDD or ODD or device emulator, and complete OOB sequence
3. Connect the host to the iSATA receptacle
4. Execute TSG-09 per SATA_MOI_BERTScope_PHY_TSG_OOB_r14_v0_8 if the PUT is transmitting at 1.5 Gb/s or TSG-11 per SATA_MOI_BERTScope_PHY_TSG_OOB_r14_v0_8 if the PUT is transmitting at 3.0 Gb/s while the host is in NRZ idle following OOB and record results for the Total Jitter (TJ) for each port

Observable Results:

- The "worst port" is identified as that which has the highest TJ value recorded on the measurement above

Appendix C: Setup

Serial ATA Interoperability Program Unified Test RSG Setup using BERTScope[1].



[1]Setup including cables and adaptors to have 20 dB return loss per SATA specifications.

Appendix D: Resource Requirements

Resource Requirements Summary for all RSG tests as covered by this MOI:

- One BERTScope 7500B S or BERTScope 12500B S with SSC, SSC+ or XSSC option and software version 10.0 or later
- A BERTScope SATA-Tee
- One clock recovery instrument BERTScope CR 12500A with software version SW 0.9.6 FPGA 2.8or later
- One iSATA receptacle to SMA Female Adapter, ICT Solutions TF-1R21 (available from BERTScope) or equivalent
- One cable set, BERTScope CR Cables or equivalent consisting of:
    i. One short SMA Male to SMA Male Cable less than or equal to 8" length, Sucoflex 104 or equivalent
    ii. A pair of matched length low loss SMA Male to SMA Male Cables of approximately 2 meters length, Suhner Sucoflex 106 or equivalent
    iii. One pair of matched length short SMA Male to SMA Male Cables, Suhner Sucoflex 104 or equivalent
- Two pairs of matched length short SMA Male to SMA Male Cables, BERTScope P/N 0130-314-00, Suhner Sucoflex 104 or equivalent
- One SMA Male to SMA Male Cable approximately 16" length, AstroLab Minibend or equivalent
- Four SMA Male to SMA Male Adapters, SUHNER 32SMA-50-0-1 or equivalent
- A pair of absorptive rise time filters, Pico Second Pulse Labs 5915-110-100PS (available from BERTScope) or equivalent
- A BERTScope ISI Board
- One BIST initiation tool, for example the BERTScope, as per Appendix A

Last Modification: March 26, 2009