# Phase Locked Loop Ku Band Frequency Synthesizer Based on a Tuned YIG Oscillator

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***Abstract*—This paper presents design and realization of Ku band frequency synthesizer based on a YIG oscillator employed as a high frequency signal source. The key aspect of this design is ADC sampling of a phase locked loop filter voltage to compensate an output frequency drift caused by temperature changes. A dedicated circuit model was created and used to determine loop filter component values. The synthesizer was built and its measured performance was compared to calculated values.**

***Keywords—Phase locked loops, Phase noise, K-band, Microwave devices, Microwave oscillators***

## I. Introduction

One of the available high frequency signal sources is Ytterbium Iron Garnet (YIG) based oscillator. It consists of a transistor-based oscillator with a small (approx. 1mm in diameter) YIG sphere coupled into its feedback circuit with small wire/ribbon loops [1][2]. The circuit forms a narrow-band filter with a single pole located at a frequency which is linearly dependent on the applied magnetic field usually generated with an electromagnet. Thus, the frequency of the oscillations can be adjusted with a current that feeds the electromagnet. In a typical YIG oscillator the total magnetic field is obtained with two separate electromagnet coils [3]. The first coil – the TUNE coil – forms a strong electromagnet, which enables tuning YIG oscillator in its entire frequency range and requires large tuning currents reaching up to 1.5A. The second coil – the FINE coil (or the FM coil) – forms a smaller electromagnet, enabling fine-tuning of generated frequency in range of tens of MHz. Its currents are significantly smaller than the TUNE coil currents and its inductance is also significantly smaller resulting in much faster response times.

Although the YIG frequency response is highly linear in relation to magnetic field (and therefore to the current applied to driving coils) it is also temperature dependent. As the current driving the main coil changes significantly with frequency, so changes the power dissipated there. This affects the temperature of the YIG oscillator, causing a frequency drift. It often happens that the drift is larger than the frequency tuning range of the FINE coil. In order to stabilize the output frequency and compensate for the temperature drift a YIG controller must properly adjust the TUNE current.

In this paper a YIG-based frequency synthesizer operating in the Ku band (i.e. 12-18 GHz) and based on a phase-locked loop (PLL) is presented. In the described circuit the frequency drift compensation is achieved by repeated measurements of a voltage on the PLL filter that drives the FINE coil and adjusting the TUNE current accordingly. It seems that no similar approach has been described before in the literature.

## II. Design Considerations

With two tuning coils available one has to choose the one to be driven by the PLL. As the FINE coil reacts faster to current changes and enables precise control over generated frequency we have decided to control it with the PLL while drive the TUNE coil directly with a Digital to Analog Converter (DAC) output of a microcontroller and a voltage-to-current (V/I) converter following the approach employed in [4].

Our synthesizer uses Micro Lambda MLOS-1167 YIG oscillator as a controlled frequency source. The YIG oscillator is, thus, driven by two independent V/I converters, one for each coil. Its electrical design is based on [5].

The PLL is based on an integrated circuit ADF41020 from Analog Devices [6]. It is an integer division ratio (*N*) PLL, which was chosen in order to avoid increased phase noise levels typically associated with fractional-N PLLs and also to simplify the noise analysis [7].

The PLL filter was designed to minimize the phase noise of the control signal. Typical models (e.g. those incorporated in a popular PLL simulation software – ADIsim PLL [8]) – calculate phase noise of PLL synthesizer using Voltage Controlled Oscillator (VCO) as an oscillator. In our simplified model the YIG oscillator together with its driver including the V/I converter can be treated as a VCO. Then the total synthesizer noise *TOTALnoise* would be calculated using analytical equations [9]. This approach, however, ignores noise added by the driver as well as its frequency characteristics. In order to improve the accuracy of the model the equations in [9] were modified to so that they account for the presence of the driver and its impact on loop filter and phase noise. To this end the PLL filter and the V/I converter characteristics were simulated in Spice environment (Fig. 1) and the results were post-processed in Matlab to form the PLL noise model. The model calculates noise added by each synthesizer component (i.e. *PLLnoise* added by the PLL integrated circuit, *OSCnoise* added by the oscillator, *REFnoise* added by reference frequency generator and *RESnoise* added by resistors and the

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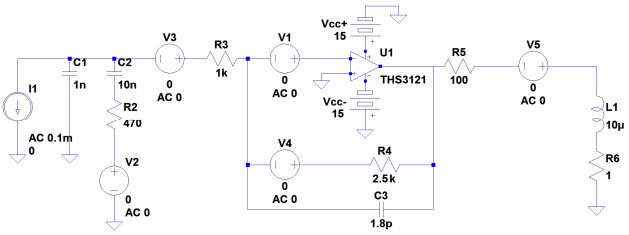


**Figure 1.** PLL filter and YIG driver simulation schematic for *RESnoise* and loop filter calculations.

amplifier). The *REFnoise* component was calculated based on the phase noise measured for the Rohde und Schwarz SML 03 signal generator employed in our experiments as a reference frequency source. The *PLLnoise* component is modeled as a sum of two components: the noise floor $PLLnoise_{flat}$ and the 1/f component $PLLnoise_{1/f}$. The $PLLnoise_{flat}$ component of the *PLLnoise* decreases with increase of reference frequency $f_{ref}$, as defined in (1) after [6][9], where the PLL division ratio $N$ is given with (2) and $PN_{1Hz}$ is the PLL figure of merit parameter.

$$PLLnoise_{flat}=PN_{1Hz}+10\times\log\left(\frac{f_{ref}}{1\text{Hz}}\right)+20\times\log(N) \quad (1)$$

$$N=\frac{f_{out}}{f_{ref}} \quad (2)$$

The *OSCnoise* is calculated using measured YIG oscillator phase noise characteristics. Every noise contribution is shaped by the low pass loop filter. Thus, the *TOTALnoise* is calculated as a sum of all noise contributions [9]:

$$TOTALnoise=PLLnoise+OSCnoise+REFnoise+\text{RESnoise} \quad (3)$$

The model let to choose component values to be used in loop filter so that the phase noise is minimal. The results of phase noise calculation are shown in Fig. 2.

The integer PLL can only generate frequencies equal to multiples of reference frequency. This means that achieving small frequency steps sacrifices the noise performance, as decreasing $f_{ref}$ leads to the increase of the $PLLnoise_{flat}$ noise

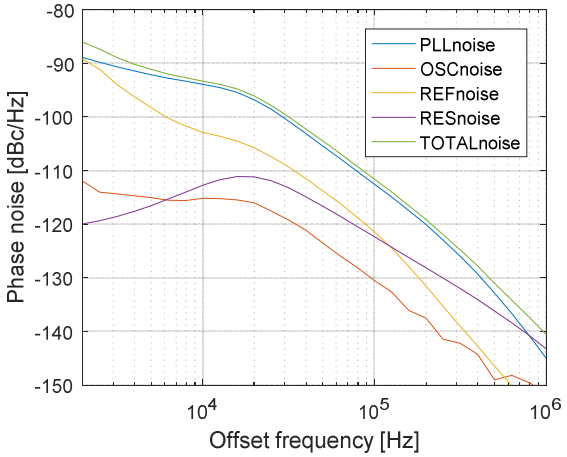


**Figure 2.** Calculated total synthesizer phase noise (green curve) and individual noise contributions from different noise sources.

component. To overcome this issue, in our design the synthesizer tuning will be achieved by changing the reference frequency. The synthesizer frequency tuning step is equal to the reference frequency tuning step multiplied by $N$. The reference frequency tuning with small tuning steps is achievable by using Direct Digital Synthesizer (DDS) as a reference frequency source.

The output frequency of a YIG generator is known to be temperature dependent and is prone to changes during synthesizer operation. Therefore care must be taken to precisely control the coarse frequency setting so that the output frequency remains stable and close to the desired frequency. If the difference between them is greater than the span of the FINE coil the PLL will fail to generate the desired frequency.

Detecting the temperature drift by measuring the output frequency would require a costly frequency counter. It would also sacrifice some of the output power. Although typical integrated PLL controllers can generate an alarm when they fall out of synchronism, there is no information provided whether the output frequency is too high or too low. Therefore in our approach the frequency mismatch is detected by measuring the voltage $V_f$ set on the PLL loop filter, as shown in Fig. 3. For the positive polarity of the phase detector the lowest possible loop filter voltage indicates that the frequency is too high (i.e. the PLL attempts to set a lower frequency than currently generated) and, similarly, the highest possible voltage indicates that the generated frequency is too low. Upon detecting any of these states the coarse frequency setting needs to be corrected accordingly.

The user sets desired frequency value in a PC-based application. The application calculates synthesizer parameters needed to achieve calculated frequency and sends them to the microcontroller. Microcontroller programs PLL chip frequency division ratio and other parameters, sets appropriate reference frequency to be generated by DDS synthesizer and sets its DAC voltage to drive the TUNE coil according to its measured tuning characteristics. Then microcontroller measures loop filter voltage $V_f$ using its ADC and adjusts coarse frequency setting accordingly to measured voltage. After the desired frequency is reached the microcontroller keeps measuring the $V_f$ voltage to accommodate for possible frequency drift due to temperature changes. Each ADC conversion result is also sent to control application running on the PC.

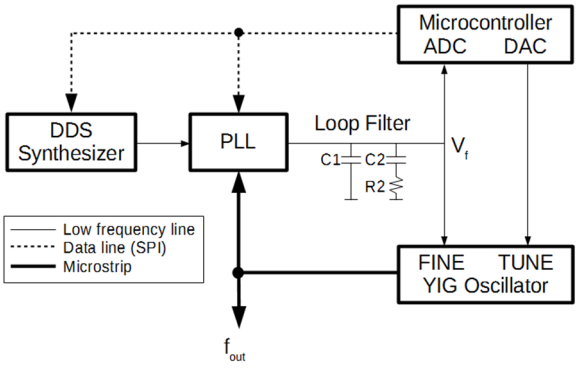


**Figure 3.** Simplified synthesizer schematic with loop filter voltage monitoring

## III. PHYSICAL REALIZATION AND MEASUREMENTS

All printed circuits boards (PCBs) used in the synthesizer were designed in the Altium Designer software and fabricated on either the standard FR4 or high frequency Rogers RT/Duroid 5880 laminate.

The synthesizer was built modularly to enable quick changes without creating a new PCB for entire synthesizer, especially in loop filter area. The first module consists of two PCBs: a simple connector board soldered to the output pins of the YIG oscillator (Fig. 4a) and a second PCB with coil drivers circuitry (Fig 4b). The driver consists of two V/I converters feeding the control coils with high current needed to create magnetic field for the YIG sphere. The coarse coil draws current from n-p-n bipolar transistor, mounted to the metal synthesizer case for cooling purposes. The driver board connects with the other PCBs using gold pin headers.

The second module is a DDS board shown in Fig. 5. This synthesizer is based on AD9957 chip by Analog Devices [10]. It is controlled by the microcontroller using Serial Peripheral Interface (SPI). The board is equipped with an output low-pass filter to suppress high frequency spurious emissions generated by DDS. The synthesizer works at clock speed ($f_{sysclk}$) of up to 1 GHz and generates analog output up to 400 MHz set with a 32-bit *FTW* (Frequency Tuning Word). The generated frequency $f_{out}$ is calculated using

$$f_{out} = \left(\frac{FTW}{2^{32}}\right) \times f_{sysclk} \qquad (4)$$

At $f_{sysclk}$ = 990 MHz the minimal frequency step of DDS synthesizer equals 0.23 Hz. This translates to 29.5 Hz step achieved by the PLL synthesizer with the division ratio *N* set to 128.

The third module (Fig. 6) hosts the microcontroller, the PLL chip and the loop filter. It was divided into sections consisting of separate PCBs: the microcontroller section, the PLL chip section, the power splitter section and the loop filter section. Both high frequency sections (i.e. the PLL chip and the power divider sections) are manufactured on the Rogers RT/duroid 5880 high frequency laminate, while the microcontroller and the loop filter boards use standard FR4. All the PCBs are mounted to the brass post with hex screws. The post provides common ground for all the PCBs and helps to cool all the active components. Splitting the module into sections has several advantages. It lowers costs as the high frequency laminate is used only for the selected PCBs. It makes the design robust as RT 5880 is soft and prone to damage especially during soldering work. Using the stiff FR4

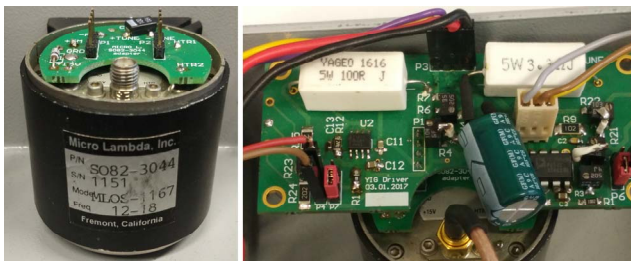


**Figure 4.** Micro Lambda Inc. Ku band YIG oscillator (a) with a voltage-to-current converter/driver (b)

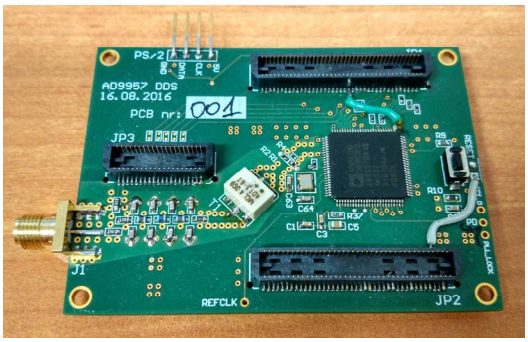


**Figure 5.** DDS Module

laminate for often modified loop filter PCB is also advantageous. The modular construction makes the design flexible, by making it possible to readily replace selected modules (e.g. in order to replace a VCO oscillator instead of YIG oscillator, change the loop filter layout or change the microcontroller without affecting rest of the synthesizer).

The microcontroller section consists Analog Devices ADuC814 microcontroller [11] with built-in ADC and DAC peripherals and an external USB-to-UART bridge chip (FTDI232) responsible for communication with a PC. The microcontroller board is also equipped with headers for external power supply and it routes power supply voltages to the other PCBs. The PLL chip section contains Analog Devices ADF41020 PLL [6] and voltage regulators to power it up. The high frequency signal is brought to the PLL by a 50Ω microstrip line. The reference frequency is either generated by an on-board crystal oscillator or provided from outside through a dedicated SMA connector. The PCB is connected to the microcontroller and the loop filter boards using gold pin jumpers and to the power splitter board using a thin copper foil soldered to microstrips on both PCBs. The current version of the system uses resistive power splitter, which inserts a power loss of ca. 6 dB. The loop filter PCB incorporates a two-pole low-pass filter with component values chosen using our circuit simulation tool. Additionally, the PCB holds also an operational amplifier, acting as voltage follower, needed to separate the loop filter from the ADC input. The loop filter PCB connects to the YIG driver module and to the PLL board. The output voltage of the voltage follower is routed to the microcontroller PCB through the PLL PCB.

The assembled synthesizer works as designed and is able to generate a stable output signal of frequency in range from 10 GHz to 18.5 GHz, covering the entire Ku band. The setting time depends on the frequency change. It varies from several milliseconds up to 200 ms, when the DAC voltage change is

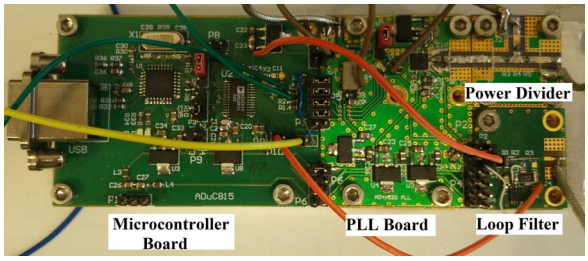


**Figure 6.** Microcontroller and PLL module

required for large steps with varying temperature. The setting time can be improved by replacing the loop filter with a circuit of higher bandwidth. However, this approach would raise the noise at larger offsets and was not adopted.

The phase noise measurement of the complete system was done using Rohde und Schwarz FSV spectrum analyzer. The measured phase noise level is −84 dBm/Hz or -90 dBm/Hz at 10 kHz offset when the reference signal $f_{ref}$ is generated with the DDS or the Rohde und Schwarz SML 03 signal generator, respectively. The noise measured when the DDS is employed is higher due to the higher DDS phase noise compared to the SML 03 generator. The phase noise level of the realized system is very close (within 5 dB) to the value calculated using our circuit-based simulation tool and the reference noise level obtained for the SML 03 generator (the DDS noise level has not been measured, yet). The measured and simulated noise levels are presented in Fig. 7.

The parameters of our synthesizer are compared to other solutions reported in the literature, including one commercially available YIG based synthesizer [14] in Table 1. The most notable advantage of our synthesizer is achieving low step size while maintaining comparable phase noise level and wide tuning range covering the full Ku band.

TABLE I. SYNTHESIZER COMPARISON

| Parameter | Synthesizer | | | |
|---|---|---|---|---|
| | ***This Work*** | ***[12]*** | ***[13]*** | ***[14]*** |
| Frequency Range [GHz] | 12-18 | 10.2-12.8 | 10.6-11.8<br>12.3-13.0 | 6-13 |
| Output Power | +5 | +10 | N/A | +16 |
| Step Size [Hz] | 29.5 | $10^6$ | $10^7$ | $10^6$ |
| SSB noise @10kHz [dBc/Hz] | −90 | −86 | −102.6 | −95 |
| Oscillator | YIG | VCO | VCO | YIG |
| Chip | ADF41020 | ADF4107 | ADF4112 | N/A |

## IV. CONCLUSIONS

The low phase noise tuned frequency synthesizer based on a YIG oscillator was successfully designed, built and tested. The proposed approach of output frequency drift tracking by measuring the loop filter voltage has proven to be working and enabled synthesizer tuning in wide band without precise temperature stabilisation. The measured phase noise level is consistent with simulation results and suggests that the model created is correct and can shorten the development time of other synthesizers to be built in future.

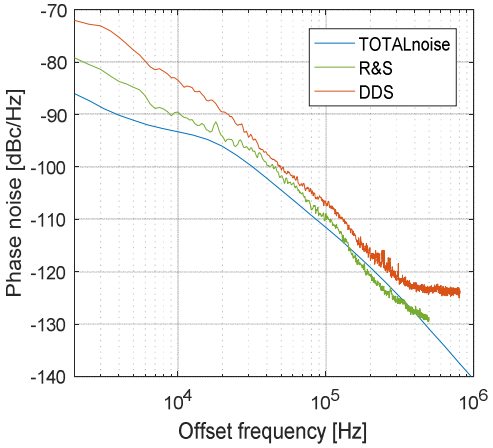


**Figure 7.** Phase noise measured using Rohde und Schwarz SML 03 signal generator as $f_{ref}$ source (green curve), using AD9957 DDS as $f_{ref}$ source (orange curve) and calculated phase noise (blue curve)

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