OpenVPX

Reference Sheet

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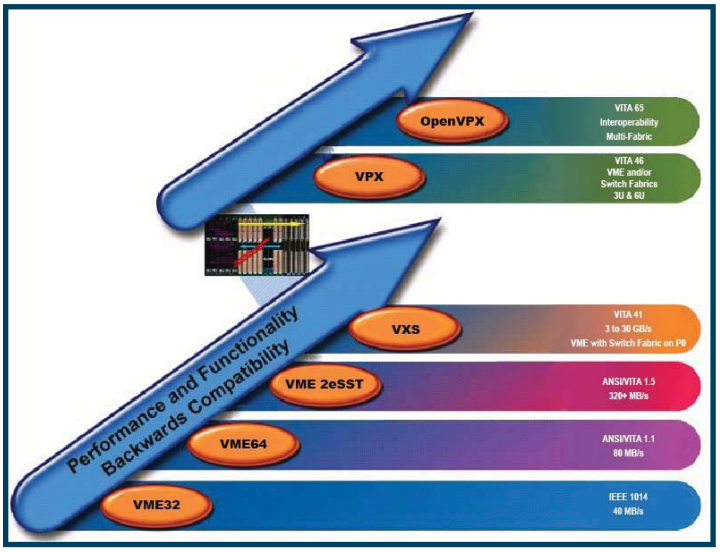
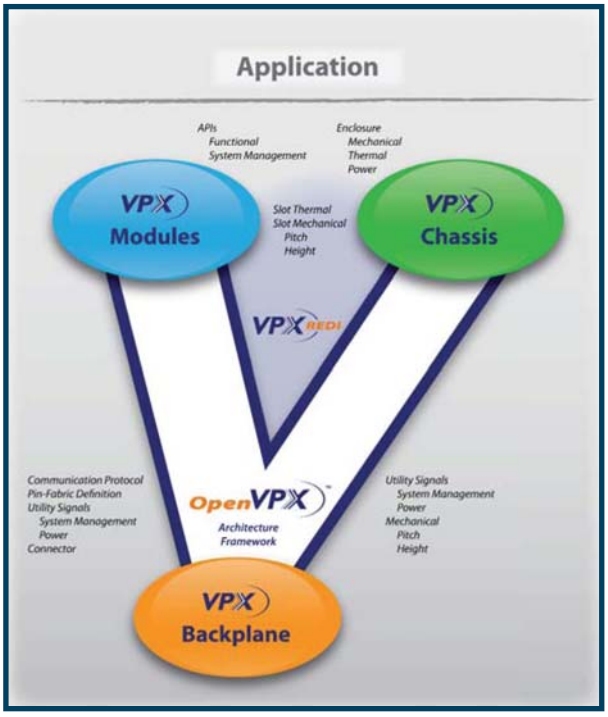
OpenVPX Reference Sheet

VME Technology Migration





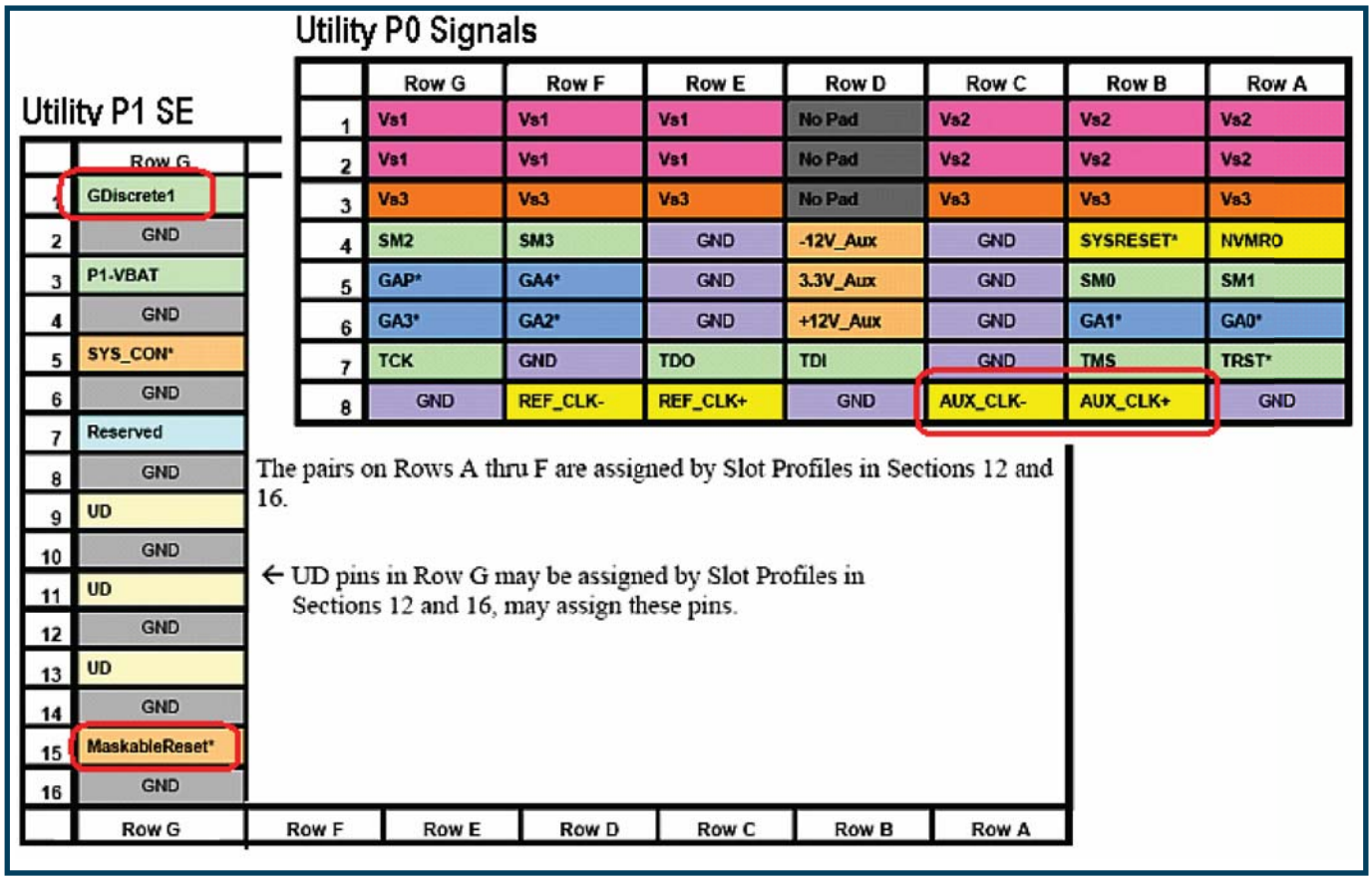
OpenVPX defines clear interoperability points necessary for integration between Module to Module, Module to Backplane and Chassis. The OpenVPX V1.0 Specification, developed by VITA members, has been turned over to the VSO in October 2009 as VITA 65 for final comment, ballot, and ratification as a standard.

The OpenVPX charter is to:

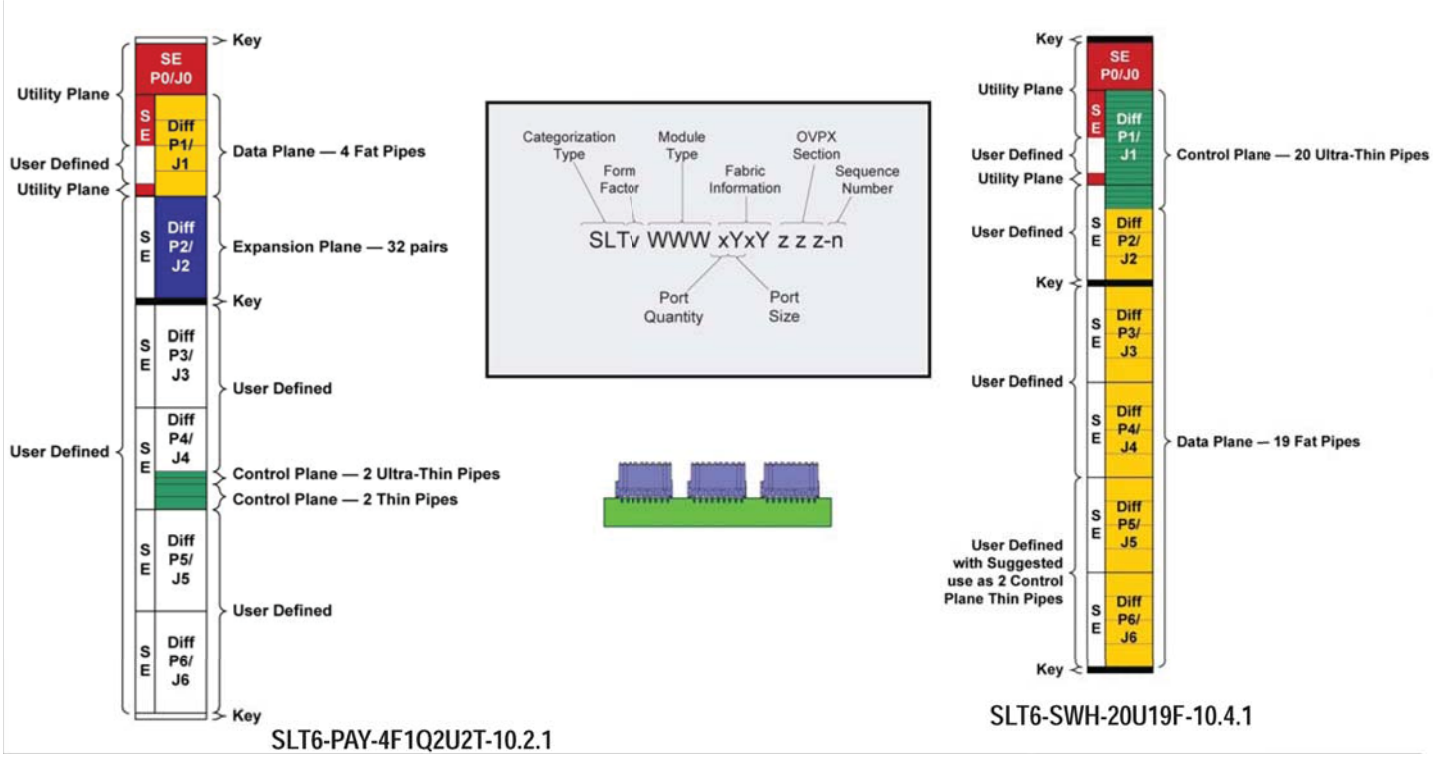
- Control and manage the assignment of VPX pins to functional planes in an interoperable architecture
- To get a high-degree of interoperability, while leaving room for sensor- / application-specific augmentation
- To make the process of developing VPX-based solutions from the lab to the field much more efficient in cost, time, quality, and repeatability

Utility Signal Additions

OpenVPX redefined two reserved P0/J0 signals Aux_Clk (+/-) and added one P1/J1 single ended Utility signal of Maskable Reset and redefined the Res_Bus signal to GDiscrete. The SysCon signal is also configurable.



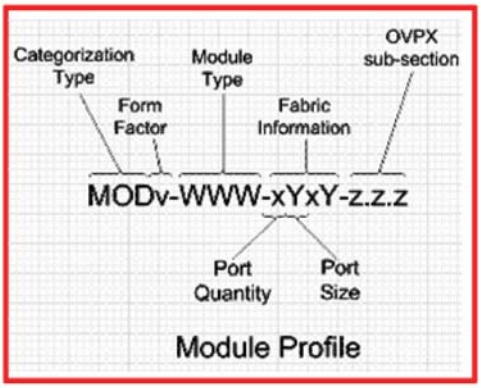
Slot Profile Examples



Examples of Slot Profile configurations

The Slot Profile shows the configuration of a backplane slot. A module that fits the slot profile may be plugged into this slot, ensuring interoperability.

Module Profile Examples



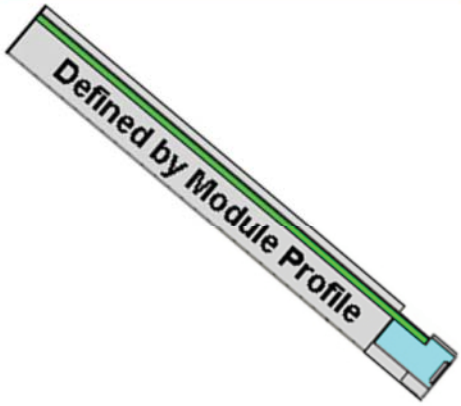


Table 12.2.2-1 Module Profiles MOD6-PAY-4F2T-12.2.2-n

Profile name	Data Plane 4 FP				Control Plane 2 TPs	
	DP01	DP02	DP03	DP04	CPtp01	CPtp02
MOD6-PAY-4F2T-12.2.2-1	SRIO 1.3 at 3.125 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-2	PCIe Gen 1 per Section 5.3				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-3	PCIe Gen 2 per Section 5.3				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-4	10GBASE-BX4 per Section 5.1.3				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-5	10GBASE-KX4 per Section 5.1.4				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-6	SRIO 2.0 at 5.0 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-7	SRIO 2.0 at 6.25 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-8	SRIO 2.1 at 5.0 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	
MOD6-PAY-4F2T-12.2.2-9	SRIO 2.1 at 6.25 Gbaud per Section 5.2				1000BASE-T per Section 5.1.2	

Example of Module Profile

Backplane Topology Example

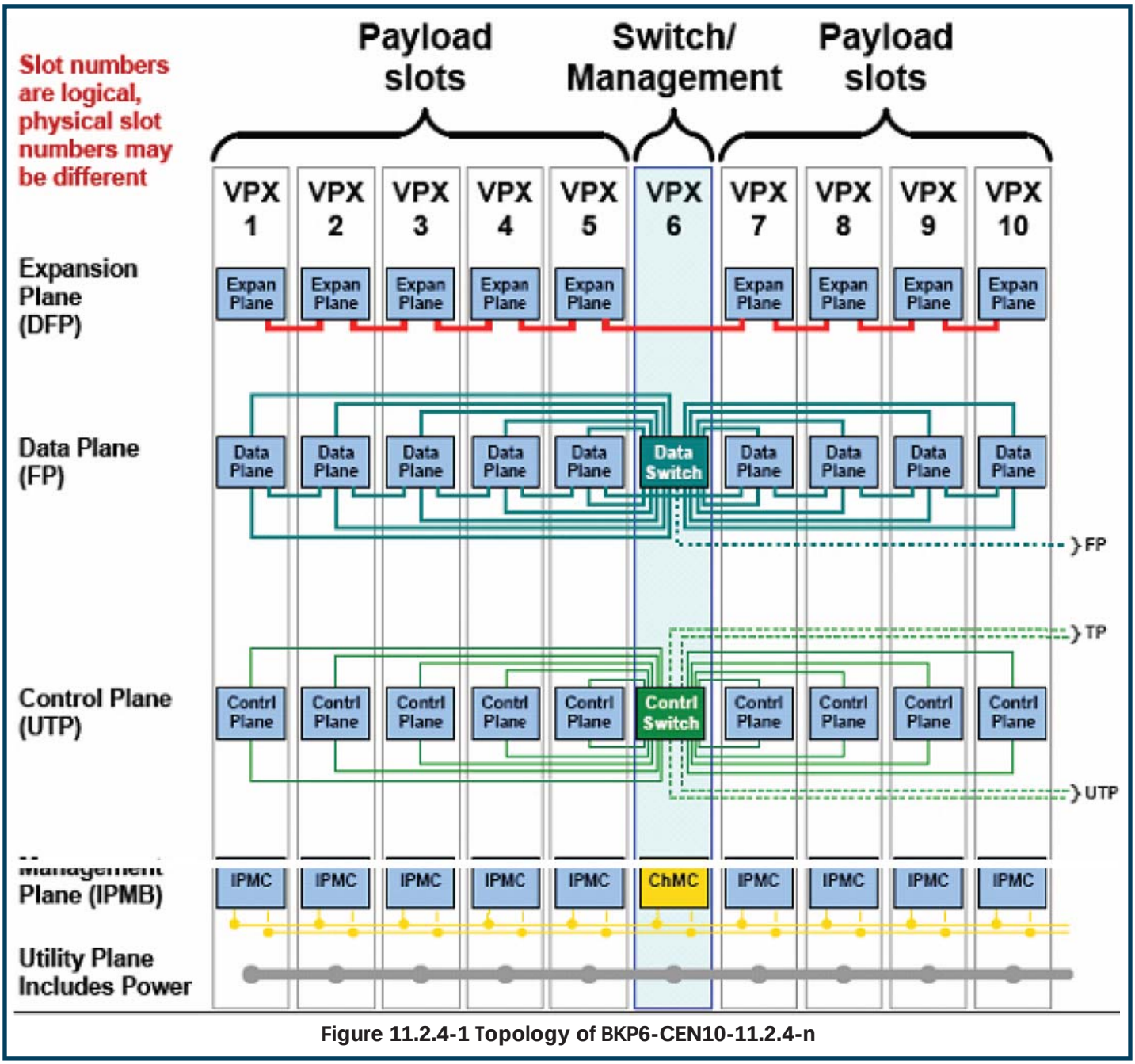


Figure 11.2.4-1 Topology of BKP6-CEN10-11.2.4-n

Backplane Profile Example

The Backplane Profile shows the various signal planes that may be used across the OpenVPX backplane. This includes the routing topology across the data plane and the connections across the expansion, control, management and utility planes. They also provide an illustration of the slot types, whether payload, switch or legacy bus slots.

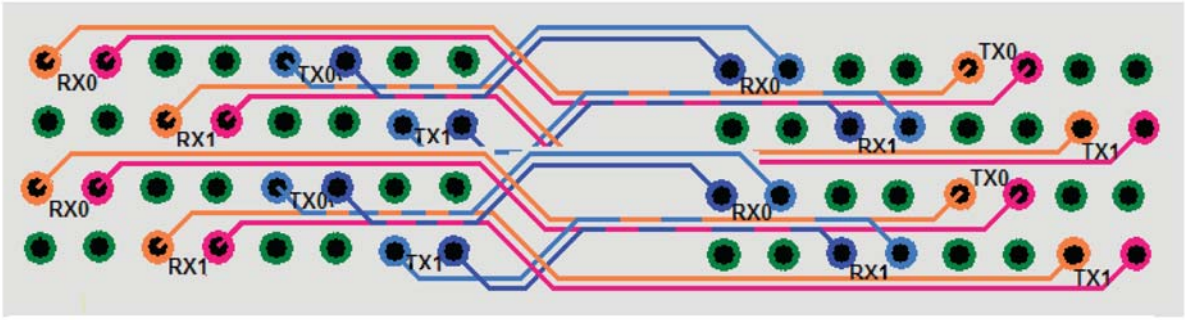
Higher Data Rates

Profile name	Mechanical		Slot Profiles and Section		Channel Gbaud Rate		
	Pitch (in)	RTM Conn	Payload	Switch	Control Plane	Data Plane	Expan-sion Plane
BKP6-CEN10-11.2.4-1	1.0	VITA 46.10	SLT6-PAY-4F1Q2U2T-10.2.1	SLT6-SWH-20U19F-10.4.1	1.25	3.125	5.0
BKP6-CEN10-11.2.4-2	1.0	VITA 46.10	SLT6-PAY-4F1Q2U2T-10.2.1	SLT6-SWH-20U19F-10.4.1	1.25	5.0	5.0
BKP6-CEN10-11.2.4-3	1.0	VITA 46.10	SLT6-PAY-4F1Q2U2T-10.2.1	SLT6-SWH-20U19F-10.4.1	1.25	6.25	5.0

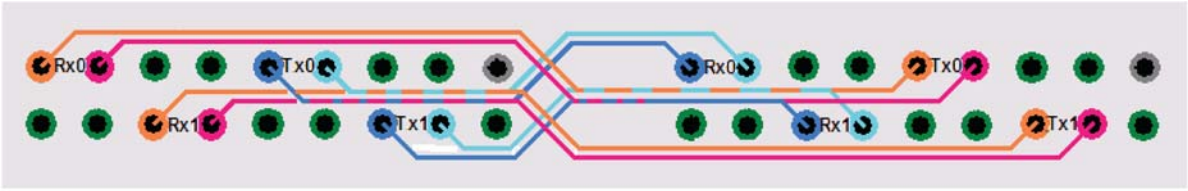
Backplane configuration chart showing the data rate options, slot profiles used, pitch and backplane profile name.

Channels: Fat, Thin, Ultra Thin

Fat Pipe: A channel comprised of four links (4 Tx pairs + 4 Rx pairs). 10Gbps capable 10GBase-KX4, 10GBase-BX4, 10GBase-T, PCIe-x4, sRIO-x4, Infiniband-x4



Thin Pipe: A channel comprised of two links (2 Tx pairs + 2 Rx pairs). 5Gbps capable 10/100/1000Base-T, 1000Base-BX, PCIe-x2, sRIO-x2, Infiniband-x2



Ultra-thin Pipe: A channel comprised of one link (1 Tx pair + 1 Rx pair). 10GBase-KR, IGBase-KX, PCIe-x1, sRIO-x1, Infiniband-x1a

Connectors

MultiGig RT-2

Ratings

Operating Voltage:	50 Volts AC peak or DC
Current:	1 ampere at <30/C (single circuit, free air)
Temperature:	-55° to 105° C
Low level contact resistance, circuit:	80 milliohms maximum initial 5 milliohms maximum average increase 10 milliohms maximum individual increase
Low level contact resistance, compliant pin:	1 milliohm maximum intital 1 milliohm maximum change
Insulation resistance:	1000 megohms minimum
Withstanding voltage:	1 minute hold with no breakdown or flashover
Temperature rise vs. current:	30° C maximum temperature at 1 ampere load, single circuit in free air using thermography

Mechanical	***Vibration, sinusodial:***
Mechanical Vibration:	No discontunuities of 1 microsecond or longer duration
Mechanical Shock:	No discontunuities of 1 microsecond or longer duration
Mating Force:	0.75 N [2.7 ozf] maximum per contact. Average for entire connector.
Unmating Force:	0.15 N [.57 ozf] minimum per contact. Average for entire connector.
Compliant pin inserton:	31 N [7 lbf] maximum per pin average
Compliant pin retention:	13.35 N [3 lbf] minimum

VME64x (160-pin DIN) - for Hybrid Backplanes

Power Stud 8-32

Current Rating:	Up to 40 A @ 30° C rise
Surface Treatment:	Tin overall
Style Designator:	86 knurled shank
Head Diameter:	0.230 inches nomial
Overall length:	0.615 inches minimum and 0.635 inches maximum
Thread Length:	0.545 inches maximum nut thread
Locking Feature:	Knurled shank