30.8 A 0.65V 12-to-16GHz Sub-Sampling PLL with 56.4fs$_{rms}$ Integrated Jitter and -256.4dB FoM

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Lowering supply voltage is an effective way to reduce circuit power consumption, especially in digital-centric system-on-chips (SoC). For low-jitter phase-locked loops (PLL) required in high-speed serial links and data converters, operation under low voltage is highly desirable such that the PLL can be readily integrated in a low-voltage (LV) SoC without a dedicated high-voltage supply. Among the various PLL architectures, the sub-sampling PLL (SSPLL) [1-3] offers low jitter with a superior jitter-power product figure-of-merit (FoM) because of its inherent rejection of N^2 amplification of in-band phase noise induced by the charge pump (CP) and phase detector (PD), as reported in [1]. However, the design of an LV SSPLL (LVSSPLL) must overcome several daunting issues. First, the CP design suffers from limited voltage headroom, degraded current noise, and limited output voltage range. Although the type-I SSPLL [3] can avoid this issue by eliminating the CP, it suffers from limited phase-noise suppression of the voltage-controlled oscillator (VCO). Second, the high on-resistance of the sub-sampling PD (SSPD) under low voltage causes attenuation of the sampled clock swing and thus degrades the in-band phase noise of the SSPLL induced by the SSPD.

This paper presents a 0.65V LVSSPLL with 56.4fs$_{rms}$ jitter and -256.4dB FoM. It mitigates the issue of limited CP output voltage range by adopting a hybrid dual-path loop architecture. By employing a combination of LV circuit techniques in designing the sub-sampling CP (SSCP), the SSPD, and a digitally controlled capacitor array (DCCA) for the class-C VCO, the LVSSPLL jitter and voltage headroom requirement are reduced simultaneously.

Figure 30.8.1 shows the block diagram of the LVSSPLL. The hybrid dual-path topology includes a proportional path (P-path) with a discrete-time switched capacitor low-pass filter (DTSCF) and an integral path (I-path) with a continuous-time passive RC low-pass filter (CTRCF). The P-path is responsible for phase tracking and thus must have high linearity and low noise. The I-path is for frequency acquisition and needs to produce a wide control voltage (V_I) tuning range to cover the desirable frequency locking range, but its nonlinearity can be tolerated. The P-path gain $G_p(s)$ dictates the loop bandwidth if it is much larger than the I-path gain $G_I(s)$. So, the overall loop stability is not sensitive to the nonlinearity in $G_I(s)$, which is caused by the variation of transconductance $g_{m,I}$ over V_I variation due to the limited output voltage range of the I-path SSCP (I-SSCP). With $G_p(s)$ set to be much higher than $G_I(s)$, the in-band phase noise of the PLL is dominated by the noise of the P-path SSCP (P-SSCP), which is suppressed by using the structure of the P-SSCP with the DTSCF. When the PLL is in lock, the P-path control voltages, V_{P+} and V_{P-}, are kept nearly constant regardless of the output frequency. Therefore, the P-SSCP only requires a small output voltage range, which in turn improves its linearity. The issue of limited CP output voltage range is relaxed by the hybrid dual-path loop structure.

Figure 30.8.1 also shows the frequency-locked loop (FLL) that is needed for the initial frequency acquisition [1]. Two current-mode logic (CML) based divide-by-2 dividers (DIV2) are used as the prescaler to operate at up to 16GHz under only 0.65V. This limits the SSPLL output frequency resolution to $4F_{REF\_FLL}$. To improve the output frequency resolution from $4F_{REF}$ to F_{REF}, we set the FLL reference frequency F_{REF_FLL} to $0.25F_{REF}$ by using a divide-by-4 divider (DIVIN/4).

Figure 30.8.2 shows the P-SSCP. Compared with the conventional SSCP [1], the P-SSCP only has two stacked MOSFETs (M1/M2 and the current source) that operate in the saturation region. Only M1 and M2 contribute noise to the P-SSCP output because the output is differential. So, not only is the voltage headroom relaxed, but also the noise is reduced. Since the P-SSCP only has a current discharge path, its output is reset and pre-charged to V_{DD} every clock cycle. Hence the DTSCF, instead of a CTRCF, is required in the P-path. The key waveforms in the P-path are presented in Fig. 30.8.2. First, C_S is pre-charged to V_{DD} when RESET is high. Next, the voltage difference as well as the phase of the sampled differential clock is converted to a voltage (V_{CP+}-V_{CP-}) by discharging C_S when PUL is high. Finally, when HOLD is high, the voltage of C_S is transferred to C_H to create the P-path VCO control voltage (V_{P+}-V_{P-}). The I-SSCP utilizes a folded input stage to relax voltage headroom requirements. When the PLL is in lock, the output current of the I-SSCP is zero, which means the sampled input differential voltage (V_{SAM+}-V_{SAM-}) is around 0V. At the same time, (V_{P+}-V_{P-}) is also around 0V, and both V_{P+} and V_{P-} are kept almost constant regardless of the output frequency.

To solve the issue of the conventional SSPD mentioned above, the LV SSPD (Fig. 30.8.3) is adopted. It adopts two high-level boosted inverters (HBINV) to enhance the turn-on voltage of the gate of M1 and M2 in the SSPD. The HBINV is modified based on the delay cell in [5]. The working principle of the HBINV is shown in Fig. 30.8.3. The post-layout simulation results of the HBINV (Fig. 30.8.3) verify that the output of the HBINV is boosted to around 1V with a 0.65V supply. As a result, the on-resistance of M1/M2 is significantly reduced even using a 0.65V supply. This prevents the attenuation of the sampled clock swing and lowers the in-band phase noise of the SSPLL induced by SSPD. M3 and M4 are inserted to compensate for the clock feedthrough from M1 and M2, respectively. Simulation results show that the sampled clock swing has a weak dependency on the SSPD input common-mode voltage V_{CM} (from 0.1 to 0.5V). This helps to reduce the design complexity of the clock isolation buffer (ISOBUF) between the SSPD input and the VCO output (Fig. 30.8.1).

A class-C VCO is used due to its low phase noise and high power efficiency [2] (Fig. 30.8.4). A differential varactor bank is used for P-path tuning whereas a single-ended varactor bank is used for I-path tuning. A 6b DCCA is adopted for coarse tuning. At 0.65V supply, the high on-resistance of the switches in the DCCA degrades the VCO Q and thus worsens the phase noise. To relax this issue, we adopt an LV DCCA. The control logic of the DCCA is supplied by the peak detector output V_{PkD} [4]. The level shifter (LS) converts the low-swing input control signals to high-swing output signals. So, the switches of the DCCA (M_{SW}) can be turned on with higher gate voltage ($>V_{DD}$), and thus suppress the Q degradation. Two thick-oxide PMOS devices are used in the LS to make the static current of LS negligible when the input P[i] is at V_{DD} (0.65V), and thus avoid degrading V_{PkD}. When M_{SW} turns off, its drain and source are biased to V_{DD} instead of V_{PkD} to increase the off-state Q while reducing voltage stress on M_{SW}. Figure 30.8.4 also shows the cascode stage adopted for the ISOBUF to improve the isolation between the VCO and the SSPD. Thanks to the large-swing VCO output, the ISOBUF can generate a buffered clock with improved swing, and the first-stage CML DIV2 (Fig. 30.8.4) in the FLL can operate at up to 16GHz under a 0.65V supply.

Figure 30.8.5 shows the measurement results of the 0.65V SSPLL with the output F_{PLL} at 14GHz using a 200MHz F_{REF}. The measured rms jitter integrated from 1kHz to 100MHz is 56.4fs, the reference spur is -64.6dBc and the FoM is -256.4dB. The measured phase noise curve and spectrum are performed on the divide-by-2 signal of the VCO output, as shown in Fig. 30.8.1. The integrated rms jitter, reference spur, and FoM remains <61fs, <-63dBc, and <-256dB, respectively, across the frequency range from 12 to 16GHz with resolution of 200MHz. Thanks to the P-SSCP with reduced noise, the LV SSPD and the LV DCCA, low-jitter performance can be achieved under a 0.65V supply.

Figure 30.8.6 shows that among the state-of-the-art low-jitter PLLs, this work achieves the best FoM and FoM_T under the lowest supply voltage reported to date. The 40nm CMOS LVSSPLL occupies 0.234mm^2 and consumes 7.2mW, as shown in Fig. 30.8.7.

Acknowledgements:
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References:

[1] X. Gao, et al., "Sub-sampling PLL Techniques", *IEEE CICC*, pp. 1-8, Sept. 2015.
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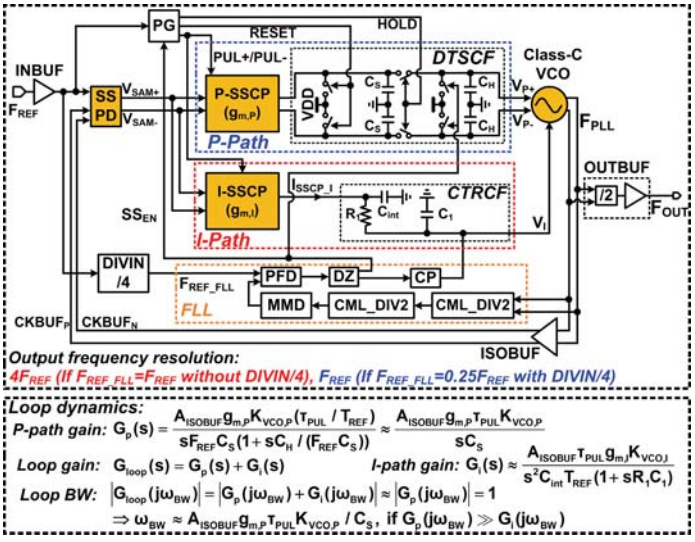


Figure 30.8.1: Block diagram of the proposed LVSSPLL.

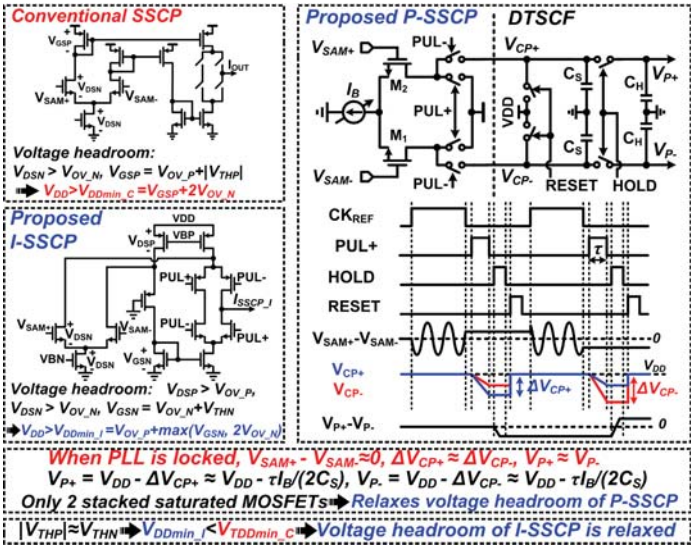


Figure 30.8.2: The P-SSCP, I-SSCP, and waveforms of the P-path.

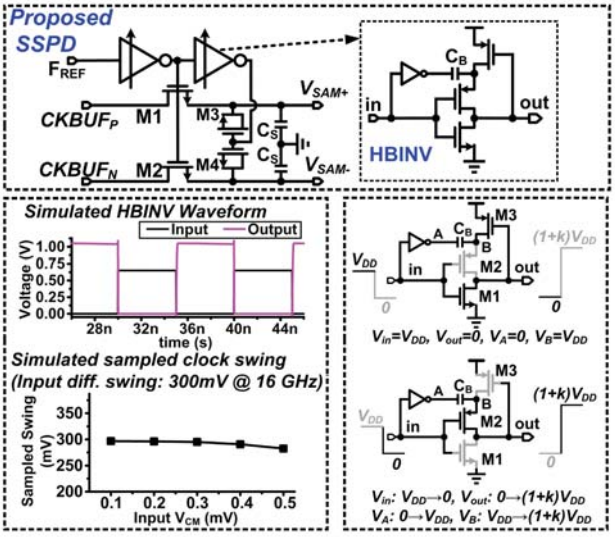


Figure 30.8.3: The SSPD and HBINV with its operation principle and simulation results.

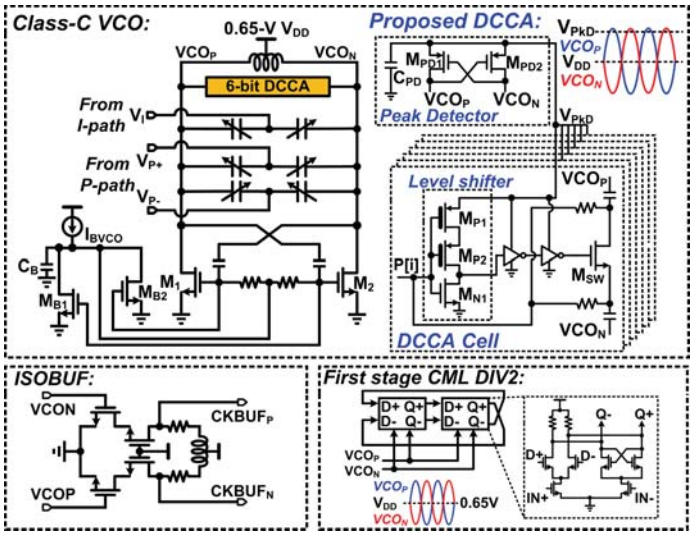


Figure 30.8.4: The Class-C VCO, DCCA, ISOBUF, and first-stage CML DIV2.

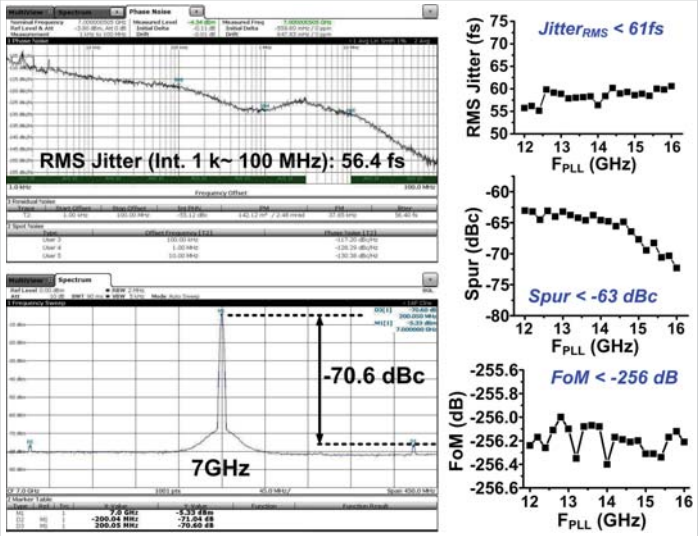


Figure 30.8.5: Measured phase noise, spectrum, rms jitter, spur level, and FoM.

	This work	A. Sharkia ISSCC'18 [3]	D. Turker ISSCC'18	M. Raj VLSI'17	A. Elkholy JSSC'18	K. H. Zeng TCAS-II'15	A. T. Narayanan JSSC'16 [2]
Architecture	SSPLL	SSPLL	CPPLL	SSPLL	ILCM (Integer-N)	ILPLL	SSPLL (Integer-N)
Process	40nm	65nm	16nm	16nm	65nm	40nm	65nm
Supply (V)	0.65	0.8	NA	0.9/1.8	0.9	1.1	1
Osc. Type	LC	LC	LC	LC	LC	LC	LC
Osc. Number	1	1	2	2	1	1	1
Out. Freq (GHz) /FTR (GHz)	14 /12-16	5 /4.6-5.6	12.5 /7.4-14	18 /9-18	7.36 /6.75-8.25	4.8 /NA	NA /4.34-4.94
Ref. Freq (MHz)	200	100	500	450	105-129	400	40
RMS jitter (fs) /Int. range	56.4 (1k~100MHz)	185.3 (10k~50MHz)	53.6 (10k~10MHz)	164 (1k~10MHz)	109 (10k~30MHz)	109.6 (1k~100M)	116 (10k~10MHz)
Ref. Spur (dBc)	-64.6	-64.1	-75.5	NA	-52	-61.59	-70.8
Power (mW)	7.2	1.1	45	29.2	2.65	3.04	2.82
FoM (dB)	-256.4	-254	-248.9	-241	-255	-254.4	-254
FoMT (dB)	-251	-247.2	-246.8	-239.3	-248	NA	-245.3
Core Area (mm²)	0.234	0.01	0.35	0.39	0.27	0.105	0.2

$FoM = 10\log((\frac{\sigma_{RMS}}{1s})^2 \times (\frac{P_{DC}}{1mW}))$ $FoM_T = FoM + 10\log(\frac{f_{Mid}}{f_{Max} - f_{Min}})$

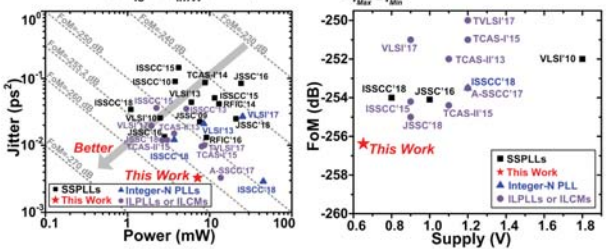
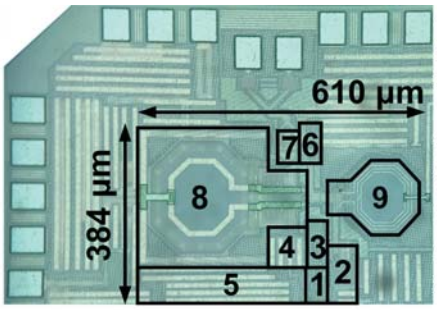


Figure 30.8.6: Performance summary and comparison.



Power Consumption						
Class-C VCO	SSPD, PG	ISOBUF	INBUF	SSCP	FLL	*Total*
3.05 mW	0.11 mW	1.4 mW	0.8 mW	0.29 mW	1.55 mW	*7.2 mW*

Figure 30.8.7: Chip photograph and power consumption breakdown.

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