ADVANCE PROGRAMME

www.date-conference.com

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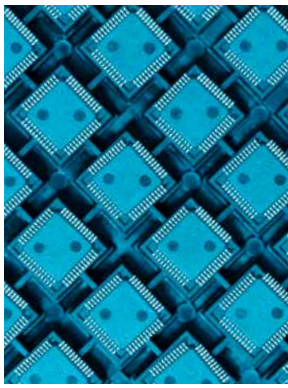

DATE 16

Design, Automation and Test in Europe

March 14—18, 2016, Dresden, Germany

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Chip Design Magazine

Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today's complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. The System Level Design and Low Power Engineering Portals offer focused editorial content you won't want to miss. And, be sure to visit www.eecatalog.com for valuable information about all of Extension Media's outstanding technology resources.

chipdesignmag.com

EDA Confidential

EDA is a commercial-free publication providing a quiet place for conversation about the Electronic Design Automation industry and its companion technologies. The coverage does not intend to be comprehensive, but does intend to provide some food for thought. To that end, EDA Confidential includes "Recipes", Freddy Santamaria's "Gourmet Corner", as well as "Voices" of other contributing authors, "Off the Record" op-ed pieces, and "Conference" coverage.

www.aycinena.com

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EDACafe.Com is the #1 EDA web portal. Thousands of IC, FPGA and System designers visit EDACafé.com to learn the latest news and research design tools and services. The sites attract more than 75,000 unique visitors each month and leverages TechJobsCafé.com to bring you job opportunities targeted to engineering and design. And daily e-newsletters reach more than 40,000 engineering professionals. For more details visitwww.EDACafe.com and www.TechJobsCafe.com.

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www.eetimes.com

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www.elinor.se

Engineering & Technology Magazine – Published by The IET

Engineering & Technology is packed with articles on the latest technology covering the areas of communications, control, consumer technology, electronics, IT, manufacturing & power engineering. It is Europe's largest circulation engineering magazine, published monthly & offers a global circulation of over 140,000 copies to more than 100 countries & a high pass-on readership. Each member of the Institution of Engineering & Technology (IET) receives a copy as part of their membership package. Readers include design & development engineers, system designers & integrators, solutions providers & installers, engineering distributors, consultants, planners, facilities managers & end-users. With its HQ in London & regional offices in Europe, North America & Asia-Pacific, the Institution of Engineering & Technology provides a global knowledge network to facilitate the exchange of ideas & promote the positive role of technology around the World. The Institution of Electrical Engineers, dating from 1889, became the Institution of Engineering & Technology in 2006. It now organises more than 120 conferences & other events each year whilst providing professional advice & briefings to industry, education & governments.

www.eandtmagazine.com

WELCOME TO DATE 2016

Dear Colleague,

We proudly present to you the Advance Programme of **DATE 2016.** DATE combines the world's favorite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design.
Out of a total of 829 paper submissions received, a large share (42%) is coming from authors in Europe, 29% of submissions are from Asia, 25% from North America, and 4% from the rest of the world. This clearly demonstrates DATE's international character, its global reach and impact.
For the 19th successive year, DATE has prepared an exciting technical programme. With the help of 327 members of the Technical Program Committee, who carried out more than 3000 reviews (about four per submission), finally 199 papers (24%) were selected for regular presentation and 81 additional ones (10%) for interactive presentation.
The DATE conference will be held at the International Congress Centre Dresden, Germany, from March 14 to 18, 2016.
As in the previous years, the conference will start on Monday, with 10 in-depth technical tutorials offered from experts of the industrial and academic worlds on innovative as well as foundational topics related to design solutions, power efficiency, the internet of things, secure systems and testing and diagnosis.
The **plenary keynote speakers** on **Tuesday** are Luc Van den hove, President and Chief Executive Officer imec, who will present a talk on **"From the happy few to the happy many: towards an intuitive internet of things.",** and Antun Domic, Executive Vice President and General Manager, Design Group, Synopsys, to talk about **"Design will make everything different".** On the same day, the **Executive Track** offers a series of business panels discussing hot topics. Executive speakers from companies leading the design and automation industry will address some of the complexity issues in electronics design and discuss about the advanced technology challenges and opportunities.

The main conference programme from Tuesday to Thursday includes 77 technical sessions organized in parallel tracks from the four areas
D – Design Methods and Tools
A – Application Design
T – Test and Robustness
E – Embedded Systems Software
and several special sessions on Hot Topics such as 3D ICs, In-Memory Computing, Heterogeneous Computing, New Transistor for Hardware Security, Embedded Tutorials on Analog-/Mixed Signal Verification Methods and on the Dark Silicon Problem as well as two sessions on selected EU Projects. In addition, the exciting programme of DATE 2016 will include a panel on past and future challenges in EDA.

Two Special Days in the programme will focus on areas bringing new challenges to the system design community: **Automotive Systems** and **Secure Systems.** Each of the Special Days will have a full programme of keynotes, panels, tutorials and technical presentations by leading experts from academia and industry.
During the Special Day on **Wednesday** on Automotive Systems, **a keynote** is given by Patrick Leteinturier, Fellow Automotive Systems, Infineon Technologies to talk about **"The Car of the future will reinvent personal mobility".** In addition, the Automotive Special Day will feature a number of technical talks covering areas such as advanced driver assistance systems, formal methods for automotive software, and various aspects of in-vehicle

WELCOME TO DATE 2016

Luca Fanucci

Jürgen Teich

as well as long-range automotive communications. Furthermore, a panel with speakers from Infineon, Bosch, Mentor, Yogitech and ETAS will discuss various EDA solutions for the automotive domain and ways to go forward.
On **Thursday,** a **keynote** in the frame of the Special Day on Secure Systems will be given by Walden C. Rhines, Chief Executive Officer and Chairman of the Board of Directors, Mentor Graphics on **"Secure silicon: enabler for the internet of things".** The Secure Systems day starts with an embedded tutorial focusing on low level software attacks, followed by technical papers addressing HW/SW embedded platform modifications for security, and technical papers discussing novel metrics and methods to support design for security and trust. The industrial relevance is illustrated with a special session addressing security challenges from Smart Grid, Industry4.0 and automotive.
Additionally, there are numerous **Interactive Presentations** which are organized into five IP sessions.
The conference is complemented by an **exhibition** which runs for three days (Tuesday – Thursday), offering a comprehensive overview of commercial design and verification tools including vendor seminars and abundant networking possibilities with fringe meetings. This year, there are dedicated campus booths with focus on major trends shaping the future of microelectronics such as **IoT and secure systems, Ultra-Low power technologies (FDSOI), 5G wireless networks, 3D-IC integration and automotive systems.** On the campus booths major international industrial players and research institutions will jointly share their vision on those trends. With this setup the exhibition provides a unique networking opportunity and states the perfect venue for industries to meet University Professors to foster University Programme and especially for PhD Students to meet future employees.
On Friday, the last day of the DATE week, **8 full-day workshops** cover a large number of hot topics related to the design and test of electronic systems. This year, DATE will present a new edition of the successful workshops targeting the manufacturing and utilization of secure devices, the techniques for model implementation fidelity, and the optical/photonic interconnects for computing systems. Additionally, some brand new workshops will take place on advanced MPSoC architectures and resource-awareness, emerging memory solutions, novel paradigms in heterogeneous computing, and modeling techniques for aging and variability.
We wish you a successful and exciting DATE 2016, fruitful discussions in the accompanying exhibition and a memorable DATE Party on Wednesday evening.

DATE 2016 General Chair
Luca Fanucci
University of Pisa, IT

DATE 2016 Programme Chair
Jürgen Teich
Friedrich-Alexander-Universität
Erlangen-Nürnberg, DE

Luc Van den hove

0915 — 0945 Großer Saal

1.1.1 From the happy few to the happy many - Towards an intuitive internet of things

Luc Van den hove, President and CEO, imec, BE

The last year every high-tech company was talking about the Internet of Things. The coming decade, we will indeed see a rise in smart connected systems. Machines, buildings, vehicles, personal appliances will all be equipped with more intelligence that will be interconnected. Smart systems will be unobtrusive, ultra-small, cheap, intelligent, and ultra–low power. They will include sensors, actuators, and processing and communication abilities, often in a one-chip wireless solution.

Imec aims at bringing the Internet of Things to the next level. Imec develops the building blocks to create an easy-to-use Internet of Things that surrounds us, that interacts with us as individuals, that learns our habits, our preferences, our health... An Internet of Things that will connect diverse unconnected systems. That will turn the massive amount of measured data in information to make the right decisions, to take the right actions exactly as we need or want. Of course taking into account our privacy preferences.

This Intuitive Internet of Things will help manage the sustainability, complexity and safety of our world. It will increase our comfort and wellbeing. Not only of the happy few. Imec will bring the Intuitive Internet of Things to the happy many.

TUESDAY OPENING CEREMONY

DATE 16
March 14 – 18, 2016, Dresden, Germany

Antun Domic

0945 — 1015 Großer Saal

1.1.2 Design Will Make Everything Different

Antun Domic, Executive Vice President and General Manager, Design Group, Synopsys, Inc., US

How many different silicon manufacturing process technologies will there be at 10, 7, or 5 nanometers? Probably only three. How many design starts will there be at 10, 7, or 5 nanometers? According to IBS[1], in 2025 there will be less than 250 design starts at 10 nanometers and below, about 3% of the total number of design starts that year, and only about five of those design starts, i.e. 2% of the 3% (0.05% of the total) will take place in Europe. But this is not the end! This is not even the beginning of the end. There is a great deal of opportunity beyond the relentless progression of Moore's law. Design innovation can be the enabler, and the differentiator, regardless of the process technology node. Automotive is a great example: according to Bosch[2], electronics represents 80% of the innovation in cars, and 40% of its cost; the car is a computer – actually, over one hundred computers – on four wheels already, and it will get smarter and smarter, with new layers of services and players just around the corner. Design, and design automation can help increase and accelerate innovation, and at the same time, improve efficiency. The "Internet of Things" is another, potentially greater example: smartness going way beyond the phone. Everything will get smarter: cars, homes, cities, agriculture, farming, factories, etc. Most of the IoT enablement and differentiation will stem from design, and design automation, which include IP, and an increasing amount of software. After performance and power consumption, systems reliability and security have already become critical design considerations at the dawn of a new era, in which design will be critical to make everything better.

[1] Design Starts by Geographic Region 2010-2025, International Business Strategies, Inc. (IBS), 2015
[2] "Can EDA Solve the Problems of Electronic Design for the Car of the Future?", Peter van Staa, Robert Bosch, ICCAD 2014 Keynote Address

WEDNESDAY KEYNOTE ADDRESS

Patrick Leteinturier

1400 — 1430 Saal 2

7.0 The Car of the Future will reinvent personal mobility

Patrick Leteinturier, Fellow Automotive Systems, Infineon Technologies AG, DE

The regulations for CO2 and pollutant reduction have pushed the automotive industry for more electrification. The internal combustion engines will continue to power our vehicles for decades but will be assisted by electric traction in various xEV architectures. The race for efficiency, environment friendly, and safety will not end here. Automated and autonomous driving cars are opening a new field of benefits, but also a new field of challenges. The engineers will have to reinvent the EE vehicle architecture for new domain control and fail operational systems. The cars will be connected to other cars and the infrastructure with software update over the air. The new vehicles will be real cyber physical systems. This keynote will explore the potential of electronic technologies to solve the new requirements in sensing, controlling, powering, energizing the car of the future.

Key items:
– Car Electronic system design & Test
– Car EE Architecture
– Car Electrification
– Connected Car
– Car Safety and Security
– Software update over the air
– Form Advance Driver Assistance System to Autonomous Driving

THURSDAY KEYNOTE ADDRESS

Walden (Wally) C. Rhines

1330 — 1400 Saal 2

11.0 Secure Silicon: Enabler for the Internet of Things

Walden C. Rhines, Chief Executive Officer and Chairman of the Board of Directors, Mentor Graphics Corporation, US

As electronic system hackers penetrate deeper—from applications to embedded software to OS to silicon—the impact of security threats is growing exponentially. Viruses and malware in the operating system, or application layer, are major concerns, but only affect a portion of users. In contrast, even small malicious modifications or compromised performance in the underlying silicon can devastate system security for all users. Growth of the Internet of Things magnifies the impact of the security problem by orders of magnitude.

Since hardware is the root of trust in an electronic product, EDA companies will be increasingly pressured to solve the silicon security problems for their customers. This requires a new paradigm in silicon design creation and verification. The traditional EDA role is to design and then verify that the silicon does what it is supposed to do. Creating secure silicon, however, requires that verification ensure that the chip does nothing that it is NOT supposed to do.

The industry is at the first stage of Secure Silicon awareness; it's going to become big business as future events unfold. Join Wally Rhines as he examines the growing threats to silicon security and EDA's possible solutions.

This printed programme is intended to provide delegates with an easy reference document during their attendance at DATE 2016. Full conference information including all technical programme details, information on awards, conference registration costs, information about accommodation, travel offers and social events is available on the conference website **www.date-conference.com**

Dates and Venue

The conference will take place from 14 to 18 March, 2016 in the MARITIM Hotel & International Congress Center Dresden (ICCD).

Maritim Hotel &
International Congress Center Dresden
Ostra-Ufer 2 / Devrientstr. 10 – 12
01067 Dresden, Germany
www.dresden-congresscenter.de

The accompanying exhibition is scheduled from 15 to 17 March, 2016 and will take place on the Terrace Level of the ICCD, which also hosts the coffee break area.

Interactive Programme Online

A fully interactive DATE 2016 programme is available on the web **www.date-conference.com** where you will be able to view the entire details of the programme and plan your attendance in advance.

Internet Access

The conference organisers will again provide free wireless internet access on-site throughout the whole congress center during the entire DATE week. The WLAN login code will be given at the registration desk upon arrival (entrance foyer of the congress center).

Proceedings

The conference proceedings are available for download on-site through the DATE-WLAN for every fully registered conference delegate at the following link: www.date-conference.com/proceedings

WHOVA Conference App

The WHOVA App can be downloaded via the following link or in the Apple / Google stores for free: **https://whova.com/download**
Microsoft users: **http://whova.com/webapp/e/date_201603/**

Please install the app and search for the conference
"DATE 2016" → Password: "DATE"

Online Conference Evaluation via the WHOVA App ("survey" button): every fully registered delegate who fills in the online conference evaluation via the app, will receive one of the exclusive DATE collector mugs at the registration desk (when showing the confirmation page).

Coffee Break in Exhibition Area

On all conference days (Tuesday to Thursday), coffee and tea will be served during the coffee breaks at the below-mentioned times in the exhibition area (Terrace Level of the ICCD).

Lunch Break — Großer Saal + Saal 1

On all conference days (Tuesday to Thursday), a seated lunch (lunch buffet) will be offered in the rooms "Großer Saal" and "Saal 1" (Saal Level of the ICCD) to fully registered conference delegates only. There will be badge control at the entrance to the lunch break area.

Tuesday, March 15, 2016	
Coffee Break	1030 – 1130
Lunch Break	1300 – 1430
Coffee Break	1600 – 1700
Wednesday, March 16, 2016	
Coffee Break	1000 – 1100
Lunch Break	1230 – 1430
Keynote Lecture in "Saal 2"	1400 – 1430
Coffee Break	1600 – 1700
Thursday, March 17, 2016	
Coffee Break	1000 – 1100
Lunch Break	1230 – 1400
Keynote Lecture in "Saal 2"	1330 – 1400
Coffee Break	1530 – 1600

Welcome Reception & PhD Forum — Mon, March 14, 2016

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2016 Welcome Reception & subsequent PhD Forum, which will take place on Monday, March 14, 2016, from 1800 - 2100 in "Saal 1" of the ICC Dresden.
The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

Exhibition Reception — Tue, March 15, 2016

The Exhibition Reception will take place on Tuesday, March 15, 2016, from 1830 – 1930 in the exhibition area (Terrace Level), where free drinks for all conference delegates and exhibition visitors will be offered. All exhibitors are welcome to also provide drinks and snacks for the attendees.

GENERAL INFORMATION

DATE Party – Networking Event — Wed, March 16, 2016

The DATE Party traditionally states one of the highlights of the DATE week. As one of the main networking opportunities during the conference, it is a perfect occasion to meet friends and colleagues in a relaxed atmosphere while enjoying local amenities. It is scheduled on March 16, 2016, from 1930 to 2300.

This year, it will take place in one of Dresden's most outstanding museum locations, the Albertinum Dresden.

This museum with its spectacular architecture has been reopened in June 2010 and houses the art gallery "Neue Meister" (New Masters Gallery) and the "Skulpturensammlung" (Sculpture Collection). You may continue the talks and discussions in a relaxed atmosphere while enjoying culinary delights. Furthermore, you will have the possibility to visit parts of the permanent collection.

Please kindly note that it is not a seated dinner.

All delegates, exhibitors and their guests are invited to attend the party. Please be aware that entrance is only possible with a valid party ticket. Each full conference registration includes a ticket for the DATE Party (which needs to be booked during the online registration process though). Additional tickets can be purchased on-site at the registration desk (subject to availability of tickets). Price for extra ticket: 60 € per person.

How to get there: A joint walk from the congress centre to the Albertinum Dresden will be organized, starting at 1900 from the main entrance of the ICC Dresden.

Interactive Presentations
(sponsored by the Cadence Academic Network)

Interactive presentations allow presenters to interactively discuss novel ideas and work in progress that may require additional research work and discussion, with other researchers working in the same area. Interested attendees can walk around freely and talk to any author they want in a vivid face-to-face format. The author may illustrate his work with a slide show on a laptop computer, a demonstration, etc. IP presentations will also be accompanied by a poster. Each IP will additionally be introduced in a relevant regular session prior to the IP Session in a one-minute presentation.

To give an overview, there will be one central projection displaying a list of all the presentations going on at the same time in the IP area. Interactive Presentation (IP) Sessions will be held in the foyer of the Conference Level in 30-minute time slots on the following days:

IP Session 1	Tuesday, March 15, 2016	Conference Level, Foyer	1600 – 1630
IP Session 2	Wednesday, March 16, 2016	Conference Level, Foyer	1000 – 1030
IP Session 3	Wednesday, March 16, 2016	Conference Level, Foyer	1600 – 1630
IP Session 4	Thursday, March 17, 2016	Conference Level, Foyer	1000 – 1030
Presentation of the Best IP Award		Saal 2	1315
IP Session 5	Thursday, March 17, 2016	Conference Level, Foyer	1530 – 1600

EXECUTIVE SESSIONS — TUESDAY

Organiser: **Yervant Zorian,** Synopsys, US

DATE 2016 will again feature an Executive Track of presentations by leading company executives representing a range of semiconductor manufacturers, EDA vendors, fables houses and IP providers. This one-day programme will be held on Tuesday 15 March, the first day of the DATE conference immediately after the Opening Session and it will be comprised of three sessions where the executives will present their technical/business vision in this nanometer technology era. Each session will feature 3-4 executives and run in parallel to the technical conference tracks.

All three executive sessions will first provide each executive with a timeslot to present his/her vision, followed by a question and answer period to provide interaction with the attendees. The Executive Track should offer prospective attendees valuable information about the vision and roadmaps of their corresponding companies from a business and technology point-of-view for Internet of Things, Automotive and Secure Systems applications.

2.1 **EXECUTIVE TRACK PANEL:**

Enabling a Connected World via Internet of Things:

See Page 41

3.1 **EXECUTIVE TRACK PANEL:**

New Opportunities in Automotive Electronics

See Page 44

4.1 **EXECUTIVE TRACK PANEL:**

Trends & Challenges to Ensure Security

See Page 50

SPECIAL DAY — WEDNESDAY

Organisers and Chairs: **Samarjit Chakraborty,** TU Munich, DE
Wolfgang Ecker, Infineon Technologies, DE

Automotive Systems

High-end cars today have up to 100 ECUs connected by various communication buses like CAN, FlexRay and Ethernet, that are used to run more than 100 millions of lines of software code spanning across safety critical, driver assistance and comfort related application domains. Designing, verifying and upgrading such a complex hardware/software system poses several challenges for EDA engineers, computer architects, and embedded systems and software designers. Further, most of the innovation in the automotive domain is now in electronics and software, as can be seen in the form of various new driver assistance systems and functionalities. Hence, there are many interesting opportunities for the EDA and the embedded systems community in the automotive domain, which the automotive special day at DATE 2016 will seek to explore in the form of various technical sessions and discussion panels.

5.1 **SPECIAL DAY Hot Topic: Building Confidence in Advanced Driver Assistance Systems**

See Page 54

6.1 **SPECIAL DAY Hot Topic: Formal Methods for Automotive Software**

See Page 59

7.1 **SPECIAL DAY Panel: Which EDA Solutions can the Automotive Domain Reuse? Very Few or All?**

See Page 63

8.1 **SPECIAL DAY Hot Topic: Connectivity in the automotive domain: From micro to macro**

See Page 69

SPECIAL DAY — THURSDAY

Organisers and Chairs: **Ingrid Verbauwhede,** KU Leuven and UCLA, BE
Matthias Schunter, Intel, DE

Secure Systems

Security is essential to create a safe and trustworthy Information and Communications Technology infrastructure. Electronics are becoming more and more integrated into the environment: the Internet of Things, CyberPhysical Systems, Smart Cities are all novel phenomena. Data is stored in and travels from implanted medical devices to the cloud over wireless links and through optical fibers. None of this revolution will be sustainable without adding security. During this special day, several aspects of making systems secure will be addressed. We plan to look at secure HW and SW platforms, address different application domains: automotive, smart grid, or smart factory. We address security versus other functional requirements as dependability and testability, and we investigate design practices for security.

On the first day of the DATE event, half-day in-depth technical tutorials are given by leading experts in their respective fields. The tutorials are well suited for researchers, tool developers and system designers.

9.1 **SPECIAL DAY Embedded Tutorial: Embedded Systems Security**

See Page 74

10.1 **SPECIAL DAY Hot Topic: Lightweight Security for Embedded Processors**

See Page 79

11.1 **SPECIAL DAY Hot Topic: Embedded Security Applications**

See Page 83

12.1 **SPECIAL DAY Hot Topic: Design Methods for Security and Trust**

See Page 89

SPECIAL SESSIONS

Special Session Chairs: **Giovanni De Micheli,** EPFL, CH
Marco Casale-Rossi, Synopsys, IT

The following eight Special Sessions have been organized, which should be of great general interest. Five Hot Topic Sessions make a technical status about emerging topics such as in-memory and embedded computing, hardware security, and 3D-IC. Two embedded tutorials offer an introduction on the latest advances in low power design, and on A&M/S verification. Finally, the Panel Session gathers experts from academia, EDA and semiconductor industry to discuss the challenges of the past and the next decade, what has been solved, and what lies ahead.

2.2 Embedded Tutorial: The Dark Silicon Problem: Technology to the Rescue?

Organisers: **Siddharth Garg,** New York University, US
Michael Niemier, University of Notre Dame, US

See Page 41

3.2 Hot Topic: 3D ICs: Leap Forward to 1,000X Performance

Organiser: **Vikas Chandra,** ARM, GB

See Page 45

4.2 Hot Topic: Nanoelectronic Design Tools Addressing Coupled Problems for 3D-IC Integration

Organisers: **Jan ter Maten,** University of Wuppertal, DE
Caren Tischendorf, Humboldt University of Berlin, DE

See Page 50

5.2 Hot Topic: In-memory Computing: Status and Trends

Organiser: **Pierre-Emmanuel Gaillardon,** University of Utah, US

See Page 54

6.2 Panel: Looking Backwards and Forwards

Organiser: **Marco Casale-Rossi,** Synopsys, US

See Page 60

SPECIAL SESSIONS

8.3 Hot Topic: Managing Heterogeneous Computing Resources at Runtime

Organisers: **Christian Plessl,** University of Paderborn, DE
David Andrews, University of Arkansas, US

See Page 70

9.8 Embedded Tutorial: Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis

Organiser: **Gregor Nitsche,** OFFIS, DE

See Page 77

12.2 Hot Topic: Exploiting New Transistor Technologies to Enhance Hardware Security (without PUFs!)

Organiser: **Michael Niemier,** University of Notre Dame, US

See Page 90

EUROPEAN PROJECTS

European Projects Chair: **Roberto Giorgi,** University of Siena, IT

New this year to DATE is a special session dedicated to European Projects. EU Project Coordinators were invited to submit a paper presenting preliminary ideas, work in progress or lessons learned. The following two special sessions have been formed for presentation based on a peer review that selected the contributions for innovation and originality.

7.2 EU Projects Special Session: Energy Efficiency drives Design

Organiser: **Roberto Giorgi,** University of Siena, IT

See Page 64

8.2 EU Projects Special Session: Towards better EU-projects - Success Stories

Organiser: **Roberto Giorgi,** University of Siena, IT

See Page 69

EVENT OVERVIEW

MONDAY
- Educational Tutorials
- Fringe Meetings & Co-Located Workshops
- Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

TUESDAY
- Opening Plenary, DATE Awards Ceremony and Keynote Addresses
- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Executive Sessions
- University Booth
- Fringe Meetings & Co-Located Workshops
- Exhibition Reception

WEDNESDAY
- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Special Day on "Automotive Systems" and Keynote
- University Booth
- Fringe Meetings & Co-Located Workshops
- DATE Party – Networking Event

THURSDAY
- Technical Conference
- Vendor Exhibition & Exhibition Theatre
- Special Day on "Secure Systems" and Keynote
- University Booth
- Fringe Meetings & Co-Located Workshops

FRIDAY
- Special Interest Workshops

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MONDAY 14 MARCH

0800 – 0930	Registration and Tutorial Welcome Refreshments at Conference Level, foyer				
Breaks	1100-1130 Morning Coffee Break 1600-1630 Afternoon Coffee Break				
	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5
0930 – 1300	M01 Design solutions: Evolutionary computing in circuit synthesis, optimization and approximation	M02 Power efficiency: Getting the Current In and the Heat Out – Power Delivery and Thermal Challenges for Mobile Computing Systems	M03 Internet-of-Things: Design Methodologies and Tools for the Internet-of-Things	M04 Secure systems: Design Automation, Test, and Error Recovery: Towards Secure, Dependable, and Adaptive Microfluidic Biochips	M05 Test and diagnosis: Hierarchical Test for Today's SOC and IoT
1300 – 1430	Lunch Break				
1330	Conference registration begins				
	Konferenz 1	Konferenz 2	Konferenz 3	Konferenz 4	Konferenz 5
1430 – 1800	M06 Design solutions: Modern clocking strategies	M07 Power efficiency: Power efficiency in the design of Smart IoT devices	M08 Internet-of-Things: Virtual Platforms in the Internet-of-Things Era – State of the art and perspectives	M09 Secure systems: Emerging Technologies and Hardware Security: Prospects and Challenges	M10 Test and diagnosis: Board-level functional fault diagnosis: industry needs and research solutions
1800 – 2100	Welcome Reception & PhD Forum in Saal 1				

TUESDAY 15 MARCH

0730	Registration, Entrance area | Speaker's Breakfast, Saal 1			
0830–1030	1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses			
1030 – 1130	Exhibition and Coffee Break			
	TRACK 1	TRACK 2	TRACK 3	TRACK 4
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1130 – 1300	2.1 Executive Track Panel: Enabling a Connected World via Internet of Things	2.2 Embedded Tutorial: The Dark Silicon Problem: Technology to the Rescue?	2.3 Automotive Systems and Smart Energy Systems	2.4 Physical Design for Cutting-edge Lithography
1300 – 1430	Lunch Break			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1430 – 1600	3.1 Executive Track Panel: New Opportunities in Automotive Electronics	3.2 Hot Topic: 3D ICs: Leap Forward to 1,000X Performance	3.3 On-Chip Security Testing	3.4 Application-specific Low-power Techniques
1600 – 1700	Coffee Break IP1 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1700 – 1830	4.1 Executive Track Panel: Trends & Challenges to Ensure Security	4.2 Hot Topic: Nanoelectronic Design Tools Addressing Coupled Problems for 3D-IC Integration	4.3 Firmware Security	4.4 System-level Energy Management
1830 – 1930	EXHIBITION RECEPTION			

TUESDAY 15 MARCH

Registration, Entrance area | Speaker's Breakfast, Saal 1					0730
1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses					0830–1030
Exhibition and Coffee Break					1030 – 1130
TRACK 5	TRACK 6	TRACK 7	TRACK 8		
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre		
2.5 Energy Efficient Systems and Architectures	2.6 Fault-Tolerant Embedded Systems	2.7 Variability Challenges in Nanoscale Designs	2.8 Revolutionising the Teaching of Computer Architecture and System on Chip Design		1130 – 1300
Lunch Break					1300 – 1430
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre		
3.5 Emerging Devices and Methodologies for Energy Efficient Systems	3.6 Timing Analysis and Measurement	3.7 Dealing with Runtime Failures	3.8 Presentations from FDSOI-Campus and from European Projects Booths: Leveraging new Semiconductor Technologies		1430 – 1600
Coffee Break IP1 Interactive Presentations					1600 – 1700
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre		
4.5 Ultra-low Energy Memory Devices	4.6 Managing Multi-Core and Flash Memory	4.7 Modeling of Devices and Mixed-Signal Circuits	4.8 Presentations from IoT-Campus (I): ASIC and Sensor Solutions		1700 – 1830
EXHIBITION RECEPTION					1830 – 1930

PLENARY SESSION
EXECUTIVE SESSION
SPECIAL SESSION
IP SESSION
EXHIBITION THEATRE
D-TRACK
A-TRACK
T-TRACK
E-TRACK

WEDNESDAY 16 MARCH

0730	Registration, Entrance area | Speaker's Breakfast, Saal 1			
	TRACK 1	TRACK 2	TRACK 3	TRACK 4
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
0830–1000	5.1 SPECIAL DAY Hot Topic: Building Confidence in Advanced Driver Assistance Systems	5.2 Hot Topic: In-memory Computing: Status and Trends	5.3 Physical Attacks and Countermeasures	5.4 Architectural-level Low-power Design
1000 – 1100	Coffee Break IP2 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1100 – 1230	6.1 SPECIAL DAY Hot Topic: Formal Methods for Automotive Software	6.2 Panel: Looking Backwards and Forwards	6.3 Anti-aging and Error protection using Checkpointing and DVFS	6.4 Power Modeling and Power Aware Synthesis
1230 – 1430	Lunch Break 7.0 SPECIAL DAY Keynote, 1400 – 1430, Saal 2			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1430 – 1600	7.1 SPECIAL DAY Panel: Which EDA Solutions can the Automotive Domain Reuse? Very Few or All?	7.2 EU Projects Special Session: Energy Efficiency drives Design	7.3 Low Power Devices and Methods for Healthcare and Assisted Living	7.4 System-Level Synthesis
1600 – 1700	Coffee Break IP3 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1700 – 1830	8.1 SPECIAL DAY Hot Topic: Connectivity in the automotive domain: From micro to macro	8.2 EU Projects Special Session: Towards better EU-projects - Success Stories	8.3 Hot Topic: Managing Heterogeneous Computing Resources at Runtime	8.4 Advanced Methods in High-Level Design
1930 – 2300	DATE Networking Event (DATE Party)			

WEDNESDAY 16 MARCH

	Registration, Entrance area | Speaker's Breakfast, Saal 1				0730
	TRACK 5	TRACK 6	TRACK 7	TRACK 8	
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
0830–1000	5.5 Alternative Computing Models	5.6 Efficient System Modeling with SystemC	5.7 RF, Power Converters, and ADC: Innovative Design and Test Solutions	5.8 Model Based Design and Verification Day - Exhibition Keynote and Application Talk	0830–1000
1000 – 1100	Coffee Break IP2 Interactive Presentations				1000 – 1100
	Konferenz 3	Konferenz 4	Konferenz 5		
1100 – 1230	6.5 Biochips	6.6 Modelling and Control of Cyber-Physical Systems	6.7 Fault tolerant systems and methods	6.8 Presentations from 5G-Campus and European Projects Booths	1100 – 1230
1230 – 1430	Lunch Break 7.0 SPECIAL DAY Keynote, 1400 – 1430, Saal 2				1230 – 1430
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
1430 – 1600	7.5 Emerging Memory Architectures	7.6 Statistical and Symbolic Techniques for the Analysis and Testing of Embedded Software	7.7 Aging mitigation to improve system robustness	7.8 Presentations from IoT-Campus (II): IoT Survival Guide and Big Data Challenges	1430 – 1600
1600 – 1700	Coffee Break IP3 Interactive Presentations				1600 – 1700
	Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
1700 – 1830	8.5 Non-volatile Memory Design Methodologies	8.6 Dataflow Modeling and Natural Language Processing	8.7 Test Methods Handling Unkowns, 2.50 Integration and Realistic Memory Defects	8.8 Model Based Design and Verification Day - Tutorial: An Industry Approach to FPGA/ARM System Development and Verification	1700 – 1830
1930 – 2300	DATE Networking Event (DATE Party)				1930 – 2300

THURSDAY 17 MARCH

0730	Registration, Entrance area | Speaker's Breakfast, Saal 1			
	TRACK 1	TRACK 2	TRACK 3	TRACK 4
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
0830–1000	9.1 SPECIAL DAY Embedded Tutorial: Embedded Systems Security	9.2 Managing the Traffic Jam in NoC	9.3 Industrial Experiences	9.4 Optimization for Logic and Physical Design
1000 – 1100	Coffee Break IP4 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1100 – 1230	10.1 SPECIAL DAY Hot Topic: Lightweight Security for Embedded Processors	10.2 Does it Work or NoC?	10.3 Design Experiences for Multimedia and Communication Applications	10.4 Stochastic Methods for Circuit Analysis & Synthesis
1230 – 1400	Lunch Break Best IP Award Presentation, 1315 – 1330, Saal 2 11.0 SPECIAL DAY Keynote, 1330 – 1400, Saal 2			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1400 – 1530	11.1 SPECIAL DAY Hot Topic: Embedded Security Applications	11.2 Beating New Technology Paths for NoC	11.3 Microarchitectures and Workload Allocation for Energy Efficiency	11.4 Automating Test Generation, Assertions and Diagnosis
1530 – 1600	Coffee Break IP5 Interactive Presentations			
	Saal 2	Konferenz 6	Konferenz 1	Konferenz 2
1600 – 1730	12.1 SPECIAL DAY Hot Topic: Design Methods for Security and Trust	12.2 Hot Topic: Exploiting New Transistor Technologies to Enhance Hardware Security (without PUFs!)	12.3 System Support for Resilience and Robustness	12.4 Simulating Everything: From Timing to Instructions

THURSDAY 17 MARCH

Registration, Entrance area | Speaker's Breakfast, Saal 1				0730
TRACK 5	TRACK 6	TRACK 7	TRACK 8	
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
9.5 Formal Bit Precise Reasoning	9.6 Real-Time Scheduling	9.7 Temperature Awareness in Computing Systems	9.8 Embedded Tutorial: Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis	0830–1000
Coffee Break IP4 Interactive Presentations				1000 – 1100
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
10.5 Enhancing Memory in Next-Generation Platforms	10.6 Compilers and Tools for GPUs and MPSoCs	10.7 Reliable System Design	10.8 Presentations from Campus 3D-IC Integration: Opportunities for SMEs and Outlook 2020+	1100 – 1230
Lunch Break Best IP Award Presentation, 1315 – 1330, Saal 2 11.0 SPECIAL DAY Keynote, 1330 – 1400, Saal 2				1230 – 1400
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
11.5 Design of Efficient Microarchitectures	11.6 Applications of Reconfigurable Computing	11.7 Naked Analog Synthesis	11.8 Launch of the Worldwide MEMS Design Contest (Part 1)	1400 – 1530
Coffee Break IP5 Interactive Presentations				1530 – 1600
Konferenz 3	Konferenz 4	Konferenz 5	Exhibition Theatre	
12.5 Accelerator Design and Heterogeneous Architectures	12.6 Reconfigurable Computing Platforms and Architectures	12.7 Formal System Level Verification	12.8 Launch of the Worldwide MEMS Design Contest (Part 2)	1600 – 1730

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SPECIAL DAY SESSION
SPECIAL SESSION
IP SESSION
EXHIBITION THEATRE
D-TRACK
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E-TRACK

FRIDAY 18 MARCH

0730 – 0830	Workshop Registration and Welcome Refreshments
Breaks	Please see individual workshop programmes for lunch and break times

0830 – 1700 Konferenz 6	0830 – 1620 Konferenz 1	0830 – 1700 Konferenz 5	0830 – 1500 Konferenz 2
W01 TRUDEVICE 2016: Workshop on Trustworthy Manufacturing and Utilization of Secure Devices	W02 3rd Workshop on Design Automation for Understanding Hardware Designs, DUHDe 2016	W03 2nd Workshop on Model-Implementation Fidelity, MiFi'16	W04 IMPAC: Getting more for less: Innovative MPSoC Architecture Paradigms for Analysability and Composability of Timing and Power
0830 – 1700 Seminar 5-6	0830 – 1715 Konferenz 3	0815 – 1700 Konferenz 4	0830 – 1630 Seminar 3-4
W05 ERMAVSS: Workshop on Early Reliability Modeling for Aging and Variability in Silicon Systems	W06 The 2nd International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS Workshop)	W07 International Workshop on Emerging Memory Solutions	W08 First Workshop on Resource Awareness and Application Autotuning in Adaptive and Heterogeneous Computing

0800 - 0930	**REGISTRATION AND TUTORIAL WELCOME REFRESHMENTS**
0930 - 1300	**TUTORIALS** (1100-1130 Coffee Break)
M01 Konferenz 1	**DESIGN SOLUTIONS: EVOLUTIONARY COMPUTING IN CIRCUIT SYNTHESIS, OPTIMIZATION AND APPROXIMATION**
M02 Konferenz 2	**POWER EFFICIENCY: GETTING THE CURRENT IN AND THE HEAT OUT - POWER DELIVERY AND THERMAL CHALLENGES FOR MOBILE COMPUTING SYSTEMS**
M03 Konferenz 3	**INTERNET-OF-THINGS: DESIGN METHODOLOGIES AND TOOLS FOR THE INTERNET-OF-THINGS**
M04 Konferenz 4	**SECURE SYSTEMS: DESIGN AUTOMATION, TEST, AND ERROR RECOVERY: TOWARDS SECURE, DEPENDABLE, AND ADAPTIVE MICROFLUIDIC BIOCHIPS**
M05 Konferenz 5	**TEST AND DIAGNOSIS: HIERARCHICAL TEST FOR TODAY'S SOC AND IOT**
1300 - 1430	**LUNCH BREAK**
1330	**CONFERENCE REGISTRATION BEGINS**
1430 - 1800	**TUTORIALS** (1600-1630 Coffee Break)
M06 Konferenz 1	**DESIGN SOLUTIONS: MODERN CLOCKING STRATEGIES**
M07 Konferenz 2	**POWER EFFICIENCY: POWER EFFICIENCY IN THE DESIGN OF SMART IOT DEVICES**
M08 Konferenz 3	**INTERNET-OF-THINGS: VIRTUAL PLATFORMS IN THE INTERNET-OF-THINGS ERA – STATE OF THE ART AND PERSPECTIVES**
M09 Konferenz 4	**SECURE SYSTEMS: EMERGING TECHNOLOGIES AND HARDWARE SECURITY: PROSPECTS AND CHALLENGES**
M10 Konferenz 5	**TEST AND DIAGNOSIS: BOARD-LEVEL FUNCTIONAL FAULT DIAGNOSIS: INDUSTRY NEEDS AND RESEARCH SOLUTIONS**
1800 - 2100	**WELCOME RECEPTION & PHD FORUM**

M01 Design solutions: Evolutionary computing in circuit synthesis, optimization and approximation

Konferenz 1 0930 - 1300

Organisers
Lukas Sekanina, Brno University of Technology, CZ
Andy M. Tyrrell, University of York, GB

Genetic and evolutionary algorithms are used in the circuit design and test community mainly as efficient optimization algorithms. Recent years have witnessed a significant development and progress in evolutionary circuit design which is now capable of delivering efficient circuit designs in terms of a multi-objective design scenario, where circuits displaying the best trade-off among key parameters are automatically sought. The goal of this tutorial is to acquaint the DATE community with the state-of-the-art evolutionary circuit design methods and demonstrate on several case studies how conventional designs can be improved by means of the evolutionary approach.

In the first part of the tutorial, we will briefly introduce the principles of evolutionary computing, evolvable hardware, and multi-objective evolutionary design. We will primarily focus on Genetic Algorithms (GA) and Cartesian Genetic Programming (CGP), as digital circuit design and optimization methods, which will be utilized in the rest of the tutorial. The first case study deals with an efficient multi-objective approach to cell libraries optimization for speed, power, yield and intrinsic variability. A second case study will consider a novel ASIC device specifically designed and fabricated to allow evolution of digital and analogue characteristics and to alleviate the post fabrication variability challenges.

The second half of the tutorial will cover gate-level circuit design, optimization and approximation. CGP will be extended to support functional equivalence checking (based on SAT solving or BDDs) in order to optimize real-world circuits, which was impossible using evolutionary algorithms in the past because of the so-called scalability problems of evolutionary design. Circuit approximation has been developed in recent years as a promising method for constructing energy efficient circuits in some application domains. We will formulate the approximate circuit design problem as a multi-objective design problem and demonstrate its solution for several key circuits (e.g. adders, multipliers, general logic, median) using CGP. Finally we will discuss hardware implementations of evolvable systems in FPGAs and compare approaches based on virtual reconfigurable circuits and dynamic partial reconfiguration.

0930 TRANSISTOR-LEVEL EVOLUTION
Chair: Lukas Sekanina, Brno University of Technology, CZ

0930 **Evolutionary computing and evolvable hardware**
Andy M. Tyrrell, University of York, GB

1000 **Evolutionary approaches to the design of variability-aware cells**
Andy M. Tyrrell, University of York, GB

1030 **Specialized hardware for evolutionary optimization and adaptation**
Andy M. Tyrrell, University of York, GB

1130 DIGITAL CIRCUIT EVOLUTION AND APPROXIMATION
Chair: Andy M. Tyrrell, University of York, GB

1130 **Evolutionary optimization of logic circuits**
Lukas Sekanina, Brno University of Technology, CZ

1200 **Evolutionary circuit approximation**
Lukas Sekanina, Brno University of Technology, CZ

1230 **FPGA-based evolvable hardware systems**
Lukas Sekanina, Brno University of Technology, CZ

M02 Power Efficiency: Getting the Current In and the Heat Out - Power Delivery and Thermal Challenges for Mobile Computing Systems

Konferenz 2 0930 - 1300

Organiser
Shidhartha Das, ARM Ltd., GB
Speakers
Saibal Mukhopadhyay, Georgia Institute of Technology, US
Visvesh Sathe, University of Washington, US

Power delivery and heat dissipation are well-known performance and reliability limiters in high-end microprocessor systems. Comparatively, mobile computing platforms typically consume order-of-magnitude lower currents, but economic and volume constraints limit impose fundamental limitations on Power Delivery Network impedance reduction and heat dissipation capability. In addition, the trend towards GHz+ operating frequencies and the ubiquity of low-power techniques such as clock-gating and power-gating, make these systems susceptible to pathological AC transients. Consequently, mobile computing systems are ultimately limited by power-delivery. Furthermore, a combination of performance demands and stringent constraints on volume, footprint, user experience and cost implies that current-generation mobile SoCs are increasingly becoming thermally limited.

In this tutorial, we address the dual challenges of power-delivery and heat dissipation in low-power mobile platforms. The tutorial is divided into 3 major sections. In the first, we motivate the pressing need for power-delivery analysis for mobile platforms. We present the system-level Power Delivery Network (PDN) modeling, analysis and measurement results on a dual-core 64bit ARM Cortex-A57 compute cluster in 28nm CMOS, as a case-study. In the second section, we examine several techniques for on-die voltage regulation and droop mitigation. We examine recent developments and challenges in the area of integrated voltage regulation across three different approaches: switching-inductor converters, switched-capacitor converters, and low-dropout (linear) regulators. We also describe architectural and circuit techniques devised to mitigate supply voltage droop and their ability to respond to various forms of supply noise events.

In the third section, we discuss approaches to alleviate thermal challenges in mobile systems. The average power of a mobile SoC is generally low and does not require additional cooling. However, occasional high-power applications can increase temperature and may incur significant performance overhead due to throttling, particularly a problem in deadline critical applications. We will discuss opportunities to enable on-demand cooling in small-form factors using two advanced cooling technologies: Thermo-electric Coolers (TEC) and in-package micro-fluidic cooling. The measurement results from test-chip will be presented to discuss the potential of TECs.

A half-day tutorial is proposed that addresses the various aspects of power and thermal challenges, particularly for mobile systems. Such systems present unique challenges due to their limited power envelopes, cost-sensitivities and form-factor considerations. To the best of our knowledge, this tutorial is the first attempt at highlighting these issues for mobile computing and presenting solutions that span a broad range of topics from on-die circuits and systems, micro-architectural techniques to packaging technology innovations. The material includes both academic and industrial perspectives that will be of high interest to both academic research community and practicing engineers.

M03 Internet-of-Things: Design Methodologies and Tools for the Internet-of-Things

Konferenz 3 0930 - 1300

Organisers

Marilyn Wolf, Georgia Institute of Technology, US
Saibal Mukhopadhyay, Georgia Institute of Technology, US
Dimitrios Serpanos, Qatar Computing Research Institute, QA

The Internet-of-Things has emerged as a key application area for semiconductors and computer systems. System-on-chip and IoT network design are key challenges for design automation and VLSI. The Internet-of-Things (IoT) interconnects an increasing number of electronic devices and systems, in order to enable the processing of their information and the control of their function. Car systems, home systems, health systems (personal or infrastructure) and industrial systems represent some of the typical application areas of the Internet-of-Things.

In the tutorial we will present a wide range of IoT technologies and applications and will classify them, so that the current differences among different IoT technologies and application areas become clear. We will follow an approach similar to the ARTEMIS embedded systems classification approach, with different but relevant application areas cross-cut by system technologies characteristics. We will survey the basic technologies for sensor architecture, processors, networking protocols, network systems, and programming environments and cloud architectures.

0930 **IOT SYSTEMS**
Organiser: Marilyn Wolf, Georgia Institute of Technology, US

1000 **IOT NETWORKING AND SECURITY**
Organiser: Dimitrios Serpanos, Qatar Computing Research Institute, QA

1100 **ULTRA-LOW POWER DEVICES FOR IOT SYSTEMS**
Organiser: Saibal Mukhopadhyay, Georgia Institute of Technology, US

1200 **IOT SYSTEM ARCHITECTURES**
Organiser: Marilyn Wolf, Georgia Institute of Technology, US

M04 Secure systems: Design Automation, Test, and Error Recovery: Towards Secure, Dependable, and Adaptive Microfluidic Biochips

Konferenz 4 0930 - 1300

Organisers

Tsung-Yi Ho, National Tsing Hua University, TW
Krishnendu Chakrabarty, Duke University, US

The tutorial offers attendees an opportunity to bridge the semiconductor ICs/system industry with the biomedical and pharmaceutical industries. The tutorial will first describe emerging applications in biology and biochemistry that can benefit from advances in electronic “biochips”. The presenters will next describe technology platforms for accomplishing “biochemistry on a chip”, and introduce the audience to both droplet-based digital and flow-based continuous microfluidics. Next, the presenters will describe reliability-aware system-level synthesis includes operation scheduling and resource binding algorithms, and physical-level synthesis includes placement and routing optimizations. In this way, the audience will see how a “biochip compiler” can translate protocol descriptions provided by an end user (e.g., a chemist or a nurse at a doctor’s clinic) to a set of optimized and executable fluidic instructions that will run on the underlying microfluidic platform.

Testing techniques will be described to detect faults after manufacture and during field operation. A classification of defects will be presented based on data for fabricated chips. Appropriately fault models will be developed and presented to the audience. Design for testability and fault diagnosis techniques will be presented. Security vulnerabilities of microfluidic biochips by identifying potential attacks will be described. The feasibility and stealthiness of possible attacks will be evaluated. Practical and fully integrated cyberphysical error-recovery system that implemented by FPGA will be demonstrated. Errors in droplet operations will be detected using capacitive sensors, the test outcome is interpreted by control hardware, and corresponding error-recovery plans are triggered in real-time for adaptive microfluidic biochips.

Finally, a number of case studies with recent applications and future challenges and several open problems in this area will also be presented.

M05 Test and diagnosis: Hierarchical Test for Today's SOC and IoT

Konferenz 5 0930 - 1300

Organiser

Yervant Zorian, Synopsys, US

Today's SoC and IoT design teams, use heterogeneous IP blocks from numerous sources, and multi-level hierarchical architecture (IPs, cores, subchips, chip). To test such SOCs and IoTs, DFT designers adopt new hierarchical test solutions across heterogeneous cores (memories, logic, AMS and interface IP), in order to support concurrent test, power reductions during test, DFT closure, isolated debug and diagnosis, pattern porting, calibration, and uniform access. This tutorial covers hierarchical test trends and solutions based on IEEE test standards, such as IEEE 1500, 1687 and 1149.1, along with intelligent infrastructure IP to help achieve the above advantages.

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M06 Design solutions: Modern clocking strategies

Konferenz 1 1430 - 1800

Organisers

Jordi Cortadella, Universitat Politecnica de Catalunya, ES
Luciano Lavagno, Politecnico di Torino, IT
Alex Yakovlev, Newcastle University, GB

Invited Speakers

Koen van Eijk, Synopsys, NL
David M. Zar, Blendics Inc., US

Clock network design and timing analysis are among the most challenging tasks in integrated circuit design. The former also exhibits the broadest range of very different solutions, ranging from "classical" zero-skew clocking, to multiple independent clock islands, each operating at a different Dynamic Voltage and Frequency Scaling (DVFS) point, and to clocks that dynamically adapt to the timing characteristics of the underlying logic. Of course, every clocking strategy must be supported by a corresponding verification method on the static timing analysis side. This can be particularly tricky when the clocks become less and less synchronous, due to power management methods or to techniques that improve robustness with respect to variability. This tutorial is aimed at covering the full range of synthesis and verification tasks for the clocks, starting from basic definitions and techniques, and then gradually expanding the horizon. Each talk will be offered by a leading industrial or academic expert, and will enable designers to choose the best synchronization technique for the problem at hand. Attendees are assumed to know about sequential logic design and basic single-phase zero-skew clocking. They will gain knowledge about the following topics: (1) clock synthesis and timing analysis, especially in conjunction with power management techniques such as clock gating, power gating and DVFS; (2) asynchronous synchronization techniques; (3) reliability analysis in the presence of meta-stability for clock domain crossing; (4) advanced adaptive clocking strategies, where the clock latency or period adapts to the operating conditions of the logic.

1430 **CLOCK SYNTHESIS AND ASYNCHRONOUS TIMING**
Chair: Luciano Lavagno, Politecnico di Torino, IT

1430 **Clock Synthesis and Chip Variability**
Koen van Eijk, Synopsys, NL

1515 **Asynchronous Timing**
Alex Yakovlev, Newcastle University, GB

1630 **CLOCK DOMAIN CROSSING AND ADAPTIVE CLOCKING**
Chair: Luciano Lavagno, Politecnico di Torino, IT

1630 **Metastability and Clock Domain Crossing**
David M. Zar, Blendics Inc., US

1715 **Adaptive clocking**
Jordi Cortadella, Universitat Politecnica de Catalunya, ES

M07 Power efficiency: Power efficiency in the design of Smart IoT devices

Konferenz 2 1430 - 1800

Organisers
Enrico Macii, Politecnico di Torino, IT
Massimo Poncino, Politecnico di Torino, IT
Michelangelo Grosso, ST-Polito s.c.ar.l., IT

In the future, objects and people will be almost permanently connected and exchanging information in the so-called Internet of Things (IoT). While the potential influence of IoT in our daily life is enormous, there are major challenges related to its energy sustainability.

The evolution of battery energy density is below the curve of Moore's law thus making power consumption the limiting factor of next-generation smart systems. Furthermore, technology allows integrating various types of energy harvesting devices, which are able to scavenge energy from the environment thus potentially compensating the increased gap between the energy demand and its availability.

The heterogeneity of domains and components involved in the design of IoT devices represents a huge challenge, but it also offers new and promising degrees of freedom in optimizing performance.

This tutorial provides IoT component and system designers with some state-of-the-art methodologies to take into account power and energy optimization during the development of a smart heterogeneous device. First, it presents an overview of the main challenges in the current IoT landscape, describing the problem setting and analyzing the performance of real-world examples. Then, the principal techniques currently used to evaluate and optimize power and energy are presented, with a special emphasis on some of the most promising novel ideas. Finally, industrial case studies are presented in further detail with some practical examples, to illustrate the possibilities that system designers can leverage to reduce system consumption, by means of a conscious selection of components and system management policies.

1430 INTRODUCTION AND MAIN CHALLENGES
Chair: Enrico Macii, Politecnico di Torino, IT

1430 **Internet of Things scenario and main challenges**
Enrico Macii, Politecnico di Torino, IT

1515 **Principles of Power Optimization: Computation, Communication and Power Delivery (I)**
Massimo Poncino, Politecnico di Torino, IT

1630 POWER AND ENERGY OPTIMIZATION FOR IOT - THEORY AND PRACTICE
Chair: Massimo Poncino, Politecnico di Torino, IT

1630 **Principles of Power Optimization: Computation, Communication and Power Delivery (II)**
Massimo Poncino, Politecnico di Torino, IT

1700 **Energy optimization & system-level modeling - case studies**
Michelangelo Grosso, ST-Polito s.c.ar.l., IT

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M08 Internet-of-Things: Virtual Platforms in the Internet-of-Things Era - State of the art and perspectives

Konferenz 3 1430 - 1800

Organisers
Kim Grüttner, OFFIS - Institute for Information Technology, DE
Davide Quaglia, EDALab s.r.l., IT

Smart embedded systems are the building blocks of the so-called Internet-of-Things (IoT). They communicate each other and interact with the physical environment. In embedded system design, it is well known that the software development effort has overtaken the hardware effort. Virtual platforms can address this mismatch by parallelizing software and hardware development. Verification and testing of applications based on IoT and smart embedded systems require a continuous evolution of virtual platform methodologies:

- the ever more powerful MPSoCs allow exploiting concurrency which must be handled in platform simulation;
- executing multiple applications on the same chip could lead to interferences and impact on extra-functional properties (e.g., time, power and temperature) which must be analyzed;
- new operating systems and hypervisors, for improved control of the system and for improved security and safety, must be ported and tested;
- smart systems are ever more connected with components or external environment with continuous-time behavior that must be simulated together with discrete-time models;
- interaction among systems is becoming a crucial aspect to be verified in a full realistic network scenario;
- integration of legacy RTL components into abstract virtual platform is desired to further reduce the time-to-market.

This tutorial will give insights into which changes to expect in new virtual platforms regarding efficient CPU simulation, analog-mixed-signal modeling, simulation of extra-functional properties and network simulation. Speakers are expert in such topics; they ported research ideas into successful tools and therefore they can provide a scientific and industrial perspective supported by real case studies. Researchers and practitioners will learn how these changes can help to design tomorrow's embedded systems more efficiently. The tutorial aims at explaining the following concepts: virtual platform concept and architecture execution and verification of embedded software by using virtual platforms simulation of extra-functional properties of embedded platforms simulation of analog-mixed-signal behavior in virtual platforms simulation of realistic network scenarios integration of legacy components in standard virtual platforms

1430 WELCOME AND OVERVIEW
Kim Grüttner[1] and Davide Quaglia[2]
[1]OFFIS - Institute for Information Technology, DE; [2]EDALab s.r.l., IT

1430 SESSION 1
Chair: Davide Quaglia, EDALab s.r.l., IT
Co-Chair: Kim Grüttner, OFFIS - Institute for Information Technology, DE

1445 **Introduction to virtual platforms: Embedded software development, debugging, analysis, and verification with virtual platforms supporting today's MPSoCs**
Simon Davidmann, Imperas Software Ltd., GB

1530 **The notion of time in virtual platforms and extraction of extra-functional properties**
Kim Grüttner, OFFIS - Institute for Information Technology, DE

1630 SESSION 2
Chair: Kim Grüttner, OFFIS - Institute for Information Technology, DE
Co-Chair: Davide Quaglia, EDALab s.r.l., IT

1630 **Modelling complex analog and digital systems: COSIDE - The design environment for heterogeneous systems**
Karsten Einwich, COSEDA Technologies GmbH, DE

1715 **Generation and integration of components into virtual platforms: RTL-to-TLM abstraction, simulation of analog components, network scenario, extra-functional properties**
Davide Quaglia, EDALab s.r.l., IT

M09 Secure systems: Emerging Technologies and Hardware Security: Prospects and Challenges

Konferenz 4 1430 - 1800

Organisers

Swaroop Ghosh, University of South Florida, US
Ramesh Karri, New York University, US
Rashmi Jha, University of Cincinnati, US

Information security has emerged as an important system and application metric. Satisfying the functionality, frequency and Thermal Design Power (TDP) in today's highly integrated circuits and systems is not adequate. Ensuring the trustworthiness and security of the design parts and overall system is the de-facto component of the design goal. This is largely due to the profit-driven business model that involves 'untrusted' third party in every step of Integrated Circuit (IC) manufacturing process ranging from design, synthesis, layout all the way to fabrication and packaging. The latest trend of integrating third party Intellectual Property (IP) blocks in the system makes the problem more intricate. Although software based security solutions are easy to implement, hardware solutions such as hardware encryption, Physically Unclonable Functions (PUFs), True Random Number Generators (TRNGs), tamper detection sensors have shown great promise to meet power/performance while uncovering and solving emerging security issues such as Trojan insertion, IC recycling, chip cloning and side channel attacks. The security primitives typically extract the spatial and temporal randomness and inherent entropy present in the system using carefully designed harvesting circuits for generating unique identification keys. The downside of CMOS based circuits are area and power overhead, sensitivity to environmental fluctuations and limited randomness and entropy offered by the Silicon substrate. The emerging technologies such as memristors, Resistive RAM (ReRAM), magnetic RAM (MRAM) and so on have shown promises to bring abundance of entropy and physical randomness while being robust, fast and orders of magnitude energy-efficient than CMOS.

This tutorial will show how one can develop hardware security primitives by exploiting the unique characteristics such as complex device and system models, chaotic dynamics, bidirectional operation, and nonvolatility of emerging nanoelectronic devices. It will explain the security capabilities of several emerging nanoelectronic devices: ReRAM devices including memristors, contact-resistive RAM, Phase Change Memories (PCM), Spin-Torque-Transfer RAM (STTRAM), Orthogonal STTRAM, graphene, carbon nanotubes, silicon nanowire field-effect transistors, and nanoelectronic mechanical switches. Next, it will focus on two particular technologies namely ReRAM and spintronics, and, dive into the prospects such as design of security primitives for authentication, key generation, data encryption, device identification, digital forensics, tamper detection, and thwarting reverse engineering. It will also cover the challenges associated with using emerging technologies such as data security and data privacy issues. Finally, the outstanding challenges in using emerging nanoelectronic devices for security will be summarized.

The first part of this tutorial will motivate the need to investigate hardware security. It will cover various forms of attacks that could be mounted on the hardware. The well-known CMOS-based hardware security primitives directed towards preventing these attacks will be introduced and their pros and cons will be highlighted. Next, the relationship between emerging technologies and hardware security will be drawn. Finally the challenges and opportunities offered by emerging nanotechnologies will be presented.

The second part of this tutorial will describe transition metal oxide (TMO) based ReRAM as a promising memory technology where the storage element is resistive in nature. The working principles, materials, and process integration approaches for ReRAM devices will be discussed in details with emphasis on device characteristics of interests for hardware security. Finally, some other contemporaries such as Conductive-Bridge RAM (CBRAM), PCM and other flavors of oxide-based memristive devices will be discuss to understand the trade-offs.

The third part of the tutorial will cover the design of security primitives by exploiting the unique feature of ReRAM devices. One popular solution to prevent hardware security attacks are physical unclonable functions (PUF) which provide a hardware specific unique signature or identification. The uniqueness of a PUF depends on intrinsic process variations within individual integrated circuits. As process variations become more prevalent due to technology scaling into the nanometer regime, novel nanoelectronic technologies such as memristors become viable options for improved security in emerging integrated circuits. An overview of the memristor based PUF structures and circuits to illustrate the potential for nanoelectronic hardware security solutions will be provided. The application of memristors for other flavors of security primitives such as tamper detection sensor, TRNGs and crypto-processors will also be discussed. Finally, the application of memristors for digital forensics will be introduced.

The last part of the tutorial will describe the basics of spintronics and some promising examples such as STTRAM and DWM. The spin-based devices have shown great promise for logic and memory applications due to superior energy-efficiency and non-volatility. However, it has been noted that the nonlinear dynamics of DWs in the physical magnetic system is an untapped source of entropy that can also be leveraged for hardware security. The inherent noise, spatial and temporal randomness in the magnetic system can be employed in conjunction with microscopic and macroscopic properties to realize novel hardware security primitives. Due to simplicity of integration the spintronic circuits can be an add-on to the Silicon substrate and complement the existing CMOS based security and trust infrastructures. This tutorial will investigate the prospects of spintronics in hardware security by exploring the security specific properties and novel security primitives realized using spintronic building blocks. As spintronic elements are entering the mainstream computing platforms they are exposed to emerging attacks that were infeasible before. This tutorial covers the security vulnerabilities, security and privacy attack models and possible countermeasures to enable safe computing environment using spintronics.

The audiences will be able to takeaway following key points from this tutorial: (a) need for hardware security, (b) emerging technologies and their security specific properties, (c) novel security primitives to exploit the unique features of emerging technologies, and, (d) security vulnerabilities, attack models and preventive solutions to protect the security and privacy attacks on circuits designed using emerging technologies.

1430 **INTRODUCTION AND MOTIVATION**
Ramesh Karri, New York University, US

1500 **OVERVIEW OF RESISTIVE RAM**
Swaroop Ghosh, University of South Florida, US

1530 **RERAM AND SECURITY**
Ramesh Karri, New York University, US

1650 **SPINTRONICS AND SECURITY**
Swaroop Ghosh, University of South Florida, US

1750 **CONCLUSIONS AND DISCUSSIONS**
Swaroop Ghosh, University of South Florida, US

M10 Test and diagnosis: Board-level functional fault diagnosis: industry needs and research solutions

Konferenz 5 1430 - 1800

Organisers

Luca Cassano, Politecnico di Milano, IT
Krishnendu Chakrabarty, Duke University, US
William Eklow, Cisco Systems, Inc., US

The objectives of this tutorial are to introduce attendees to advanced concepts in data-driven board diagnosis and repair for functional test, and how "no-trouble-founds" (NTFs) are related to board-level test and diagnosis methodologies, component testing, fault models and test escapes. Test/diagnosis engineers have to deal with large amounts of test data (for legacy boards) as well as with the lack of test data (for new products). Furthermore, given the lack of automatic diagnosis tools, the accuracy and cost of the diagnosis procedure strongly depend on the experience of the diagnosis engineers. The tutorial will be focused on diagnosis challenges that arise in the functional testing of boards and on the use of data analytics for smart diagnosis/repair. For many NTFs today, structural test solutions such as those based on boundary scan (IEEE 1149.1 and its variants) are not sufficient. The presenters will also highlight case studies, and recent research advances to reduce NTFs and increase component quality through design-for-testability solutions, decision theory, and machine-learning techniques. The presenters are from industry and academia, hence both perspectives and the interplay between basic research and industry practice will be highlighted. The presenters will highlight open problems and challenges to stimulate breakthroughs in this area.

1430 **MOTIVATION AND BACKGROUND**
Bill Eklow, Cisco Systems, Inc., US

1530 **DATA-DRIVEN DIAGNOSIS AND GUIDANCE FOR REPAIR**
Luca Cassano, Politecnico di Milano, IT

1700 **HOW TO HANDLE DATA OVERLOAD, EVALUATE DIAGNOSIS SYSTEMS, AND ACCOMPLISH DIAGNOSIS AT EARLY STAGES OF PRODUCT MANUFACTURING?**
Krishnendu Chakrabarty, Duke University, US

MAIN CONFERENCE

15 – 17 MARCH, 2016

TECHNICAL PROGRAMME

1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses

Tuesday, March 15, 2016
0830 — 1030
Großer Saal, ICCD

Chair: **Luca Fanucci,** University of Pisa, IT
Co-Chair: **Jürgen Teich,** Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

0830 **WELCOME ADDRESSES**
Luca Fanucci, DATE 2016 General Chair, University of Pisa, IT
Jürgen Teich, DATE 2016 Programme Chair
Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

0845 **PRESENTATION OF DISTINGUISHED AWARDS**

DATE 2016 BEST PAPER AWARD

2016 EDAA ACHIEVEMENT AWARD
Giovanni De Micheli, EPFL, CH

EDAA OUTSTANDING DISSERTATION AWARD

IEEE FELLOW AWARD
David Atienza Alonso, EPFL, CH

DATE FELLOW AWARDS
Robert Gardner, EDAC, US
Wolfgang Nebel, OFFIS & University of Oldenburg, DE

IEEE CEDA OUTSTANDING SERVICE CONTRIBUTION AWARD 2015
Wolfgang Nebel, OFFIS & University of Oldenburg, DE

IEEE CS TTTC OUTSTANDING CONTRIBUTION AWARD
Wolfgang Nebel, OFFIS & University of Oldenburg, DE

0915 **KEYNOTE ADDRESSES**

KEYNOTE ADDRESS: "FROM THE HAPPY FEW TO THE HAPPY MANY. TOWARDS AN INTUITIVE INTERNET OF THINGS"
Luc Van den hove, President and CEO, imec, BE

KEYNOTE ADDRESS: "DESIGN WILL MAKE EVERYTHING DIFFERENT"
Antun Domic, Executive Vice President and General Manager, Design Group, Synopsys, Inc., US

1030 **COFFEE BREAK IN THE EXHIBITION AREA**

TECHNICAL SESSIONS

2.1 Executive Track Panel: Enabling a Connected World via Internet of Things

Saal 2 1130 - 1300

Organiser: **Yervant Zorian,** Synopsys, US

Enabling a connected world through Internet of Things empower a variety of applications, including medical wearables, home automation, energy, transportation, environmental monitoring, etc. This results in several new approaches and innovative methods that work together to enable the network of smart devices. The executives in this session will discuss the impact of IoT on the semiconductor industry and their influence on the eco system players.

Executives: **Christoph Heer,** Intel, DE
Jamil Kawa, Synopsys, US
Rudy Lauwereins, IMEC, BE
Cheng-Wen Wu, Industrial Technology Research Institute, TW

1300 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

2.2 Embedded Tutorial: The Dark Silicon Problem: Technology to the Rescue?

Konferenz 6 1130 - 1300

Organisers: **Siddharth Garg,** New York University, US
Michael Niemier, University of Notre Dame, US
Chair: **Muhammad Shafique,** Karlsruhe Institute of Technology (KIT), DE
Co-Chair: **Umit Ogras,** Arizona State University, US

In 2014, Jörg Henkel organized a "hot topic" special session that provided the DATE community with a snapshot of current research activities related to the grand challenge of dark silicon (DS). A primary purpose of that session was to introduce and engage the design automation community on this important problem. The lead presentation in the 2014 session was by Prof. Michael Taylor who spoke about the "landscape of the new dark silicon design regime." He defined a taxonomy termed "the four horsemen" for addressing the DS challenge. These are:- The shrinking horseman - i.e., addressing power density and thermal challenges caused by transistor scaling- The dim horseman - i.e., mitigating the DS challenge using near-threshold voltage scaling- The "deux ex machine" horseman - i.e., leveraging emerging and/or disruptive device technologies with more appealing power, performance and power density trade-offs- The specialization horseman - i.e., provisioning chips with a large number of application-specific acceleratorsTaylor notes: "Future chips are likely to employ not just one horseman, but all of them, in interesting and unique combinations.". In this embedded tutorial, we consider how researchers are leveraging new technologies - especially 3D integration and new transistor technologies - to address the DS problem. For continuity, we frame technology-based solutions in the context of the four-horsemen identified by Taylor in 2014.

1130 **TOWARDS PERFORMANCE AND RELIABILITY-EFFICIENT COMPUTING IN THE DARK SILICON ERA**
Speaker: Jörg Henkel, Karlsruhe Institute of Technology (KIT), DE
Authors: Jörg Henkel, Santiago Pagani, Heba Khdr, Florian Kriebel, Semeen Rehman and Muhammad Shafique, Karlsruhe Institute of Technology (KIT), DE

1200 **TOWARDS NEAR-THRESHOLD SERVER PROCESSORS**
Speaker: David Atienza, École Polytechnique Fédérale de Lausanne (EPFL), CH
Authors: Ali Pahlevan[1], Javier Picorel[1], Arash Pourhabibi Zarandi[1], Davide Rossi[2], Marina Zapater[3], Andrea Bartolini[4], Pablo G. del Valle[1], David Atienza[1], Luca Benini[4] and Babak Falsafi[1]
[1]École Polytechnique Fédérale de Lausanne (EPFL), CH; [2]ETH Zurich, CH; [3]CEI Campus Moncloa, UCM-UPM, ES; [4]Università di Bologna, IT

1230 **CAN BEYOND-CMOS DEVICES ILLUMINATE DARK SILICON?**
Speaker: Michael Niemier, University of Notre Dame, US
Authors: Robert Perricone, X. Sharon Hu, Joseph Nahas and Michael Niemier, University of Notre Dame, US

1300 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

2.3 Automotive Systems and Smart Energy Systems

Konferenz 1 1130 - 1300

Chair: **David Boyle,** Imperial College London, GB
Co-Chair: **Felix Reimann,** Audi Electronics Venture, DE

This session considers the state of the art in automotive systems and smart energy systems including novel approaches for efficient embedded software in automobiles, formal analyses and fault detection, and joint optimisation approaches for lifetime and functionality improvements in electric vehicles.

1130 OTEM: OPTIMIZED THERMAL AND ENERGY MANAGEMENT FOR HYBRID ELECTRICAL ENERGY STORAGE IN ELECTRIC VEHICLES
Speaker: Mohammad Al Faruque, University of California, Irvine, US
Authors: Korosh Vatanparvar and Mohammad Abdullah Al Faruque, University of California, Irvine, US

1200 SUPERTASK: MAXIMIZING RUNNABLE-LEVEL PARALLELISM IN AUTOSAR APPLICATIONS
Speaker: Sebastian Kehr, Denso Automotive Deutschland GmbH, DE
Authors: Sebastian Kehr[1], Milos Panic[2], Eduardo Quinones[3], Bert Boeddeker[1], Jorge Becerril Sandoval[1], Jaume Abella[3], Francisco Cazorla[4] and Günter Schäfer[5]
[1]Denso Automotive Deutschland GmbH, DE; [2]Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES; [3]Barcelona Supercomputing Center, ES; [4]Barcelona Supercomputing Center and IIIA-CSIC, ES; [5]Ilmenau University of Technology, DE

1230 FORMAL ANALYSIS BASED EVALUATION OF SOFTWARE DEFINED NETWORKING FOR TIME-SENSITIVE ETHERNET
Speaker: Daniel Thiele, Technische Universität Braunschweig, DE
Authors: Daniel Thiele and Rolf Ernst, Technische Universität Braunschweig, DE

1245 ACCELERATED ARTIFICIAL NEURAL NETWORKS ON FPGA FOR FAULT DETECTION IN AUTOMOTIVE SYSTEMS
Speaker: Shreejith Shanker, Nanyang Technological University, SG
Authors: Shreejith Shanker[1], Bezborah Anshuman[1] and Suhaib A. Fahmy[2]
[1]Nanyang Technological University, SG; [2]University of Warwick, GB

IPS IP1-1, IP1-2, IP1-3

1300 LUNCH BREAK IN GROSSER SAAL + SAAL 1

2.4 Physical Design for Cutting-edge Lithography

Konferenz 2 1130 - 1300

Chair: **Jens Lienig,** Technische Universität Dresden, DE
Co-Chair: **Patrick Groeneveld,** Synopsys Inc., US

Major developments in lithography covered in this session include multiple patterning, optical proximity correction and directed self-assembly. The papers contribute numerical and graph-theoretic techniques for analysis, design and optimization. The last paper explores circuit partitioning for heterogeneous 3D integration.

1130 OPTIMIZATION FOR MULTIPLE PATTERNING LITHOGRAPHY WITH CUTTING PROCESS AND BEYOND
Speaker: Jian Kuang, The Chinese University of Hong Kong, HK
Authors: Jian Kuang and Evangeline F. Y. Young, The Chinese University of Hong Kong, HK

1200 A FAST MANUFACTURABILITY AWARE OPTICAL PROXIMITY CORRECTION (OPC) ALGORITHM WITH ADAPTIVE WAFER IMAGE ESTIMATION
Speaker: Ahmed Awad, Tokyo Institute of Technology, JP
Authors: Ahmed Awad[1], Atsushi Takahashi[1] and Chikaaki Kodama[2]
[1]Tokyo Institute of Technology, JP; [2]Toshiba Corporation, JP

1230 REDUNDANT VIA INSERTION IN DIRECTED SELF-ASSEMBLY LITHOGRAPHY
Speaker: Woohyun Chung, Korea Advanced Institute of Science and Technology, KR
Authors: Woohyun Chung, Seongbo Shim and Youngsoo Shin, Korea Advanced Institute of Science and Technology, KR

1245 IMPROVED PERFORMANCE OF 3DIC IMPLEMENTATIONS THROUGH INHERENT AWARENESS OF MIX-AND-MATCH DIE STACKING
Speaker: Andrew B. Kahng, UCSD, US
Authors: Kwangsoo Han, Andrew B. Kahng and Jiajia Li, University of California, San Diego, US

IPS IP1-4, IP1-5, IP1-6

1300 LUNCH BREAK IN GROSSER SAAL + SAAL 1

2.5 Energy Efficient Systems and Architectures

Konferenz 3 1130 - 1300

Chair: **Mladen Berekovic,** TU Braunschweig, DE
Co-Chair: **Rolf Ernst,** TU Braunschweig, DE

This session will explore novel technologies to reduce the energy and power of computing systems. The first paper explores system-level DVFS approaches that maximize performance within a fixed thermal envelope. The second paper introduces a highly introspective system that can monitor and optimize its own energy usage at run-time. The third paper explores a control algorithm design that can utilize a specialized SRAM cell design that trades performance and reliability. The fourth paper finds new ways to better utilize GPU power resources by co-scheduling synergistic kernels.

1130 A DISCRETE THERMAL CONTROLLER FOR CHIP-MULTIPROCESSORS
Speaker: Yingnan Cui, Nanyang Technological University, SG
Authors: Yingnan Cui[1], Wei Zhang[2] and Bingsheng He[1]
[1]Nanyang Technological University, SG; [2]Hong Kong University of Science and Technology, HK

1200 SWALLOW: BUILDING AN ENERGY-TRANSPARENT MANY-CORE EMBEDDED REAL-TIME SYSTEM
Speaker: Steve Kerrison, University of Bristol, GB
Authors: Steve Kerrison and Simon Hollis, University of Bristol, GB

1230 A NOVEL CACHE-UTILIZATION BASED DYNAMIC VOLTAGE FREQUENCY SCALING (DVFS) MECHANISM FOR RELIABILITY ENHANCEMENTS
Speaker: Yen-Hao Chen, National Tsing Hua University, Taiwan, TW
Authors: Yen-Hao Chen[1], Yi-Lun Tang[1], Yi-Yu Liu[2], Allen C.-H. Wu[3] and TingTing Hwang[1]
[1]National Tsing Hua University, TW; [2]Yuan Ze University, TW; [3]Jiangnan University, CN

1245 EFFICIENT KERNEL MANAGEMENT ON GPUS
Speaker: Xiuhong Li, Peking University, CN
Authors: Xiuhong Li and Yun Liang, Peking University, CN

IPS IP1-7

1300 LUNCH BREAK IN GROSSER SAAL + SAAL 1

2.6 Fault-Tolerant Embedded Systems

Konferenz 4 1130 - 1300

Chair: **Lothar Thiele,** ETH Zurich, CH
Co-Chair: **Jian-Jia Chen,** TU Dortmund, DE

This session presents new results on timing and schedulability bounds for fault-tolerant systems, covering both transient and permanent faults.

1130 **PROBABILISTIC WCET ESTIMATION IN PRESENCE OF HARDWARE FOR MITIGATING THE IMPACT OF PERMANENT FAULTS**
Speaker: Damien Hardy, University of Rennes/IRISA, FR
Authors: Damien Hardy[1], Isabelle Puaut[1] and Yiannakis Sazeides[2]
[1]University of Rennes 1/IRISA, FR; [2]University of Cyprus, CY

1200 **A FOUR-MODE MODEL FOR EFFICIENT FAULT-TOLERANT MIXED-CRITICALITY SYSTEMS**
Speaker: Zaid Al-bayati, McGill University, CA
Authors: Zaid Al-bayati[1], Jonah Caplan[1], Brett Meyer[1] and Haibo Zeng[2]
[1]McGill University, CA; [2]Virginia Tech, US

1230 **PROVIDING FORMAL LATENCY GUARANTEES FOR ARQ-BASED PROTOCOLS IN NETWORKS-ON-CHIP**
Speaker: Eberle A Rambo, Technische Universität Braunschweig, DE
Authors: Eberle A Rambo, Selma Saidi and Rolf Ernst, Technische Universität Braunschweig, DE

IPS **IP1-8**

1300 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

2.7 Variability Challenges in Nanoscale Designs

Konferenz 5 1130 - 1300

Chair: **Vikas Chandra,** ARM Research, US
Co-Chair: **Said Hamdioui,** TU Delft, NL

Process variation continues to be an important challenge across new technologies. This session explores methods for systematically designing test chips, building photonic interconnects and constructing spatial models.

1130 **ACHIEVING 100% CELL-AWARE COVERAGE BY DESIGN**
Speaker: Zeye Liu, Carnegie Mellon University, US
Authors: Zeye Liu, Benjamin Niewenhuis, Soumya Mittal and Ronald Blanton, Carnegie Mellon University, US

1200 **MODELING FABRICATION NON-UNIFORMITY IN CHIP-SCALE SILICON PHOTONIC INTERCONNECTS**
Speaker: Mahdi Nikdast, Polytechnique Montréal and McGill University, CA
Authors: Mahdi Nikdast[1], Gabriela Nicolescu[2], Jelena Trajkovic[3] and Odile Liboiron-Ladouceur[4]
[1]Polytechnique Montréal and McGill University, CA; [2]Polytechnique Montréal, CA; [3]Concordia University, CA; [4]McGill University, CA

1230 **EFFICIENT SPATIAL VARIATION MODELING VIA ROBUST DICTIONARY LEARNING**
Speaker: Changhai Liao, Fudan University, CN
Authors: Changhai Liao[1], Jun Tao[1], Xuan Zeng[1], Yangfeng Su[1], Dian Zhou[2] and Xin Li[3]
[1]Fudan University, CN; [2]Fudan University & The University of Texas at Dallas, US; [3]Carnegie Mellon University, US

IPS **IP1-9, IP1-10**

1300 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

2.8 Revolutionising the Teaching of Computer Architecture and System on Chip Design

Exhibition Theatre 1130 - 1300

Exhibition Theatre session: see Exhibition Theatre Programme for details.

3.1 Executive Track Panel: New Opportunities in Automotive Electronics

Saal 2 1430 - 1600

Organiser: **Yervant Zorian,** Synopsys, US

While the robustness requirements for automotive chips remain crucial due to their safety critical mission, the new automotive chips keep growing in functionality and complexity. The executives in this session will discuss the impact of automotive market on these semiconductor chips and the new opportunities it may bring in designing today's automotive chips.

Executives: **Martin Duncan,** STMicroelectronics, FR
Rainer Kress, Infineon Technologies, DE
Dan Kochpatcharin, TSMC Europe, NL
Frank Schirrmeister, Cadence Design Systems, US

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.2 Hot Topic: 3D ICs: Leap Forward to 1,000X Performance

Konferenz 6 1430 - 1600

Organiser: **Vikas Chandra,** ARM, US
Chair: **Vikas Chandra,** ARM, US
Co-Chair: **Norbert Wehn,** University of Kaiserslautern, DE

In this session, we will cover the entire spectrum of innovations in 3D-IC integration to applications which would give benefits of multiple orders of magnitude and everything in between. First talk focuses on discussing N3XT architecture to improve the energy efficiency of abundant-data applications significantly, thereby enabling new frontiers of applications for both mobile devices and the cloud. Second talk discusses the opportunities brought by 3D sequential integration and highlights the applications benefiting from a very small 3D contact pitch. Third talk concludes the session with the discussion of the interactions of upcoming 3D-IC technologies and the system-level interconnect hierarchy to design the next generation applications.

1430 **THE N3XT 1,000X**
Speaker: Subhasish Mitra, Stanford University, US
Author: Subhasish Mitra, Stanford University, US

1500 **3D SEQUENTIAL INTEGRATION FOR MONOLITHIC 3DIC DESIGN**
Speaker: Olivier Billoint, CEA-Leti, FR
Author: Olivier Billoint, CEA-Leti, FR

1530 **3D TECHNOLOGY DRIVEN BY 3D APPLICATION REQUIREMENTS: A 3D-LANDSCAPE FOR 3D SYSTEM DESIGN**
Speaker: Eric Beyne, IMEC, BE
Author: Eric Beyne, IMEC, BE

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.3 On-Chip Security Testing

Konferenz 1 1430 - 1600

Chair: **Giorgio Di Natale,** LIRMM, FR
Co-Chair: **Marc Witteman,** Riscure, NL

This session deals with the question whether the actual chip satisfies the design and all mechanisms work securely. This includes on-the-fly testing of the quality of a random number generator as well as methods to detect hardware trojans.

1430 **TOTAL: TRNG ON-THE-FLY TESTING FOR ATTACK DETECTION USING LIGHTWEIGHT HARDWARE**
Speaker: Bohan Yang, Katholieke Universiteit Leuven, BE
Authors: Bohan Yang[1], Vladimir Rozic[1], Nele Mentens[1], Wim Dehaene[2] and Ingrid Verbauwhede[1]
[1]Katholieke Universiteit Leuven, BE; [2]KU Leuven and IMEC, BE

1500 **ON-CHIP FINGERPRINTING OF IC TOPOLOGY FOR INTEGRITY VERIFICATION**
Speaker: Maxime Lecomte, CEA, FR
Authors: Maxime Lecomte[1], Jacques Fournier[1] and Philippe Maurine[2]
[1]CEA, FR; [2]CEA/LIRMM, FR

1530 **ACTIVATION OF LOGIC ENCRYPTED CHIPS: PRE-TEST OR POST-TEST?**
Speaker: Ozgur Sinanoglu, New York University, AE
Authors: Muhammad Yasin[1], Samah Mohamed Saeed[2], Jeyavijayan (JV) Rajendran[3] and Ozgur Sinanoglu[4]
[1]New York University, US; [2]Institute of Technology University of Washington, US; [3]The University of Texas at Dallas, US; [4]New York University, AE

IPS **IP1-12, IP1-13**

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.4 Application-specific Low-power Techniques

Konferenz 2 1430 - 1600

Chair: **Sheldon X.-D. Tan,** University of California at Riverside, US
Co-Chair: **Masaaki Kondo,** University of Tokyo, JP

This session introduces power and energy management technics that are tailed for application-specific characteristics. The first paper introduces how simplified neurons without a multiplier can perform in artificial neural networks. The second paper again demonstrates power saving of artificial neural networks with a novel hybrid SRAM cells. The third paper introduces network-aware energy management for mobile applications.

1430 **MULTIPLIER-LESS ARTIFICIAL NEURONS EXPLOITING ERROR RESILIENCY FOR ENERGY-EFFICIENT NEURAL COMPUTING**
Speaker: Syed Shakib Sarwar, Purdue University, US
Authors: Syed Shakib Sarwar, Swagath Venkataramani, Anand Raghunathan and Kaushik Roy, Purdue University, US

1500 **SIGNIFICANCE DRIVEN HYBRID 8T-6T SRAM FOR ENERGY-EFFICIENT SYNAPTIC STORAGE IN ARTIFICIAL NEURAL NETWORKS**
Speaker: Gopalakrishnan Srinivasan, Purdue University, US
Authors: Gopalakrishnan Srinivasan, Parami Wijesinghe, Syed Shakib Sarwar, Akhilesh Jaiswal and Kaushik Roy, Purdue University, US

1530 **NETWORK DELAY-AWARE ENERGY MANAGEMENT FOR MOBILE SYSTEMS**
Speaker: Soontae Kim, Korea Advanced Institute of Science and Technology, KR
Authors: Minho Ju, Hyeonggyu Kim and Soontae Kim, Korea Advanced Institute of Science and Technology, KR

IPS **IP1-14**

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.5 Emerging Devices and Methodologies for Energy Efficient Systems

Konferenz 3 1430 - 1600

Chair: **Mehdi Tahoori,** Karlsruhe Institute of Technology, DE
Co-Chair: **Aida Todri-Sanial,** LIRMM, FR

This session explores how new devices can be used to build energy efficient systems. The first paper presents a novel simultaneously bi-directional TSV technology, promising area and energy benefits. The second paper presents programmable logic circuit designs based on nanowire transistors. The last paper examines how inherent characteristics of reversible logic circuits can be exploited to check combinational equivalence in faster ways.

1430 **ENABLING SIMULTANEOUSLY BI-DIRECTIONAL TSV SIGNALING FOR ENERGY AND AREA EFFICIENT 3D-ICS**
Speaker: Sunghyun Park, Massachusetts Institute of Technology (MIT), US
Authors: Sunghyun Park[1], Alice Wang[2], Uming Ko[2], Li-Shiuan Peh[1] and Anantha Chandrakasan[1]
[1]Massachusetts Institute of Technology (MIT), US; [2]MediaTek Inc., US

1500 **RECONFIGURABLE NANOWIRE TRANSISTORS WITH MULTIPLE INDEPENDENT GATES FOR EFFICIENT AND PROGRAMMABLE COMBINATIONAL CIRCUITS**
Speaker: Jens Trommer, Namlab gGmbH, DE
Authors: Jens Trommer[1], Michael Raitza[2], André Heinzig[2], Tim Baldauf[2], Marcus Völp[2], Thomas Mikolajick[3] and Walter Weber[4]
[1]Namlab gGmbH, DE; [2]Technische Universität Dresden, DE; [3]NaMLab Gmbh / TU Dresden, DE; [4]NaMLab gGmbH and CfAED, DE

1530 **EXPLOITING INHERENT CHARACTERISTICS OF REVERSIBLE CIRCUITS FOR FASTER COMBINATIONAL EQUIVALENCE CHECKING**
Speaker: Luca Amaru, École Polytechnique Fédérale de Lausanne (EPFL), CH
Authors: Luca Amaru[1], Pierre-Emmanuel Gaillardon[2], Robert Wille[3] and Giovanni De Micheli[1]
[1]École Polytechnique Fédérale de Lausanne (EPFL), CH; [2]University of Utah, US; [3]Johannes Kepler University Linz, AT

IPS **IP1-15, IP1-16**

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.6 Timing Analysis and Measurement

Konferenz 4 1430 - 1600

Chair: **Marko Bertogna,** Università di Modena e Reggio Emilia, IT
Co-Chair: **Damien Hardy,** University of Rennes 1/IRISA, FR

The papers in this session provide timing estimation techniques for a variety of real-time systems and components, ranging from engine control to networked systems.

1430 **CONSERVATIVE MODELING OF SHARED RESOURCE CONTENTION FOR DEPENDENT TASKS IN PARTITIONED MULTI-CORE SYSTEMS**
Speaker: Junchul Choi, Seoul National University, KR
Authors: Junchul Choi, Donghyun Kang and Soonhoi Ha, Seoul National University, KR

1500 **FORMAL WORST-CASE TIMING ANALYSIS OF ETHERNET TSN'S BURST-LIMITING SHAPER**
Speaker: Daniel Thiele, Technische Universität Braunschweig, DE
Authors: Daniel Thiele and Rolf Ernst, Technische Universität Braunschweig, DE

1530 **REAL-TIME ANALYSIS OF ENGINE CONTROL APPLICATIONS WITH SPEED ESTIMATION**
Speaker: Alessandro Biondi, Scuola Superiore Sant'Anna, IT
Authors: Alessandro Biondi and Giorgio Buttazzo, Scuola Superiore Sant'Anna, IT

1545 **TRACE-BASED ANALYSIS METHODOLOGY OF PROGRAM FLASH CONTENTION IN EMBEDDED MULTICORE SYSTEMS**
Speaker: Lin Li, Infineon Technologies, DE
Authors: Lin Li and Albrecht Mayer, Infineon Technologies, DE

IPS **IP1-17**

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.7 Dealing with Runtime Failures

Konferenz 5 1430 - 1600

Chair: **Lorena Anghel,** TIMA Laboratory, FR
Co-Chair: **Michel Renovell,** LIRMM, FR

Reliability is an important consideration in modern design. Two key issues in runtime resilience are robustness against soft errors and tolerance of aging effects. The papers in this session consider both effects.

1430 **A CROSS-LAYER ANALYSIS OF SOFT ERROR, AGING AND PROCESS VARIATION IN NEAR THRESHOLD COMPUTING**
Speaker: Anteneh Gebregiorgis, Karlsruhe Institute of Technology (KIT), DE
Authors: Anteneh Gebregiorgis, Saman Kiamehr, Fabian Oboril, Rajendra Bishnoi and Mehdi B. Tahoori, Karlsruhe Institute of Technology (KIT), DE

1500 **FAST-YET-ACCURATE VARIATION-AWARE CURRENT AND VOLTAGE MODELLING OF RADIATION-INDUCED TRANSIENT FAULT**
Speaker: Yuwen Lin, National Chiao Tung University, TW
Authors: Yuwen (Dave) Lin, Yuwen Lin and Hung-Pin Wen, National Chiao Tung University, TW

1530 **A DETAILED METHODOLOGY TO COMPUTE SOFT ERROR RATES IN ADVANCED TECHNOLOGIES**
Speaker: Marc Riera, Universitat Politècnica de Catalunya (UPC), ES
Authors: Marc Riera[1], Ramon Canal[2], Jaume Abella[3] and Antonio Gonzalez[2]
[1]Universitat Politècnica de Catalunya (UPC), ES; [2]UPC-Barcelona, ES; [3]Barcelona Supercomputing Center, ES

1545 **ANALYSIS OF NBTI EFFECTS ON HIGH FREQUENCY DIGITAL CIRCUITS**
Speaker: Ahmet Unutulmaz, OFFIS Institute for Information Technology, DE
Authors: Ahmet Unutulmaz[1], Domenik Helms[1], Reef Eilers[1], Malte Metzdorf[1], Ben Kaczer[2] and Wolfgang Nebel[3]
[1]OFFIS Institute for Information Technology, DE; [2]IMEC, BE; [3]University of Oldenburg and OFFIS, DE

IPS **IP1-18**

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.8 Presentations from FDSOI-Campus and from European Projects Booths: Leveraging new Semiconductor Technologies

Exhibition Theatre 1430 - 1600

Exhibition Theatre session: see Exhibition Theatre Programme for details.

IP1 Interactive Presentations

Conference Level, Foyer 1600 - 1630

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. Moreover, one "Best Interactive Presentation Award" will be given.

IP1-1 **A SCALABLE LANE DETECTION ALGORITHM ON COTSS WITH OPENCL**
Speaker: Kai Huang, Sun Yat-Sen University, CN
Authors: Kai Huang[1], Biao Hu[2], Jan Botsch[3], Nikhil Madduri[3] and Alois Knoll[3]
[1]Sun Yat-Sen University, CN; [2]Technische Universität München (TUM), DE; [3]Technische Universität München (TUM), DE

IP1-2 **SIMULATION OF FALLING RAIN FOR ROBUSTNESS TESTING OF VIDEO-BASED SURROUND SENSING SYSTEMS**
Speaker: Dennis Hospach, Universität Tübingen, DE
Authors: Dennis Hospach[1], Stefan Mueller[1], Wolfgang Rosenstiel[1] and Oliver Bringmann[2]
[1]Universität Tübingen, DE; [2]Universität Tübingen / FZI, DE

IP1-3 **PROPOSAL FOR FAST DIRECTIONAL ENERGY INTERCHANGE USED IN MCMC-BASED AUTONOMOUS DECENTRALIZED MECHANISM TOWARD RESILIENT MICROGRID**
Speaker: Yusuke Sakumoto, Tokyo Metropolitan University, JP
Authors: Yusuke Sakumoto[1] and Ittetsu Taniguchi[2]
[1]Tokyo Metropolitan University, JP; [2]Ritsumeikan University, JP

TUESDAY 15 MARCH, 2016

DATE16
March 14–18, 2016, Dresden, Germany
TUE

IP1-4 **GRID-BASED SELF-ALIGNED QUADRUPLE PATTERNING AWARE TWO DIMENSIONAL ROUTING PATTERN**
Speaker: Atsushi Takahashi, Tokyo Institute of Technology, JP
Authors: Takeshi Ihara[1], Toshiyuki Hongo[1], Atsushi Takahashi[1] and Chikaaki Kodama[2]
[1]Tokyo Institute of Technology, JP; [2]Toshiba, JP

IP1-5 **PRACTICAL ILP-BASED ROUTING OF STANDARD CELLS**
Speaker: Rung-Bin Lin, Yuan Ze University, TW
Authors: Hsueh-Ju Lu, En-Jang Jang, Ang Lu, Yu Ting Zhang, Yu-He Chang, Chi-Hung Lin and Rung-Bin Lin, Yuan Ze University, TW

IP1-6 **A PROCEDURE FOR IMPROVING THE DISTRIBUTION OF CONGESTION IN GLOBAL ROUTING**
Speaker: Azadeh Davoodi, University of Wisconsin - Madison, US
Authors: Daohang Shi, Azadeh Davoodi and Jeffrey Linderoth, University of Wisconsin - Madison, US

IP1-7 **MACHINE LEARNED MACHINES: ADAPTIVE CO-OPTIMIZATION OF CACHES, CORES, AND ON-CHIP NETWORK**
Speaker: Rahul Jain, Indian Institute of Technology Delhi, IN
Authors: Rahul Jain[1], Preeti Ranjan Panda[1] and Sreenivas Subramoney[2]
[1]Indian Institute of Technology Delhi, IN; [2]Intel, IN

IP1-8 **IMPROVING PERFORMANCE BY MONITORING WHILE MAINTAINING WORST-CASE GUARANTEES**
Speaker: Syed Md Jakaria Abdullah, Uppsala University, SE
Authors: Syed Md Jakaria Abdullah, Kai Lampka and Wang Yi, Uppsala University, SE

IP1-9 **FAULT TOLERANT NON-VOLATILE SPINTRONIC FLIP-FLOP**
Speaker: Rajendra Bishnoi, Karlsruhe Institute of Technology (KIT), DE
Authors: Rajendra Bishnoi, Fabian Oboril and Mehdi Tahoori, Karlsruhe Institute of Technology (KIT), DE

IP1-10 **TOWARDS AUTOMATIC DIAGNOSIS OF MINORITY CARRIERS PROPAGATION PROBLEMS IN HV/HT AUTOMOTIVE SMART POWER ICS**
Speaker: Yasser Moursy, Sorbonne Universités, UPMC Univ Paris 06, UMR 7606, LIP6, F-75005, Paris, FR
Authors: Yasser Moursy[1], Hao Zou[1], Ramy Iskander[1], Pierre Tisserand[2], Dieu-My Ton[2], Giuseppe Pasetti[3], Ehrenfried Seebacher[4], Alexander Steinmair[4], Thomas Gneiting[5] and Heidrun Alius[5]
[1]Sorbonne Universités, UPMC, FR; [2]Valeo, Creteil, FR; [3]AMS, Navacchio, IT; [4]AMS AG, Unterpremstaetten, AT; [5]AdMOS, Frickenhausen, DE

IP1-12 **TOWARDS HIGHLY RELIABLE SRAM-BASED PUFS**
Speaker: Elena Ioana Vatajelu, Politecnico di Torino, IT
Authors: Elena Ioana Vatajelu[1], Giorgio Di Natale[2] and Paolo Prinetto[3]
[1]POLITO, IT; [2]LIRMM, FR; [3]Politecnico di Torino, IT

IP1-13 **CURRENT BASED PUF EXPLOITING RANDOM VARIATIONS IN SRAM CELLS**
Speaker: Fengchao Zhang, University of Florida, US
Authors: Fengchao Zhang[1], Shuo Yang[1], Jim Plusquellic[2] and Swarup Bhunia[1]
[1]University of Florida, US; [2]University of New Mexico, US

IP1-14 **BEHAVIORAL MODELING OF TIMING SLACK VARIATION IN DIGITAL CIRCUITS DUE TO POWER SUPPLY NOISE**
Speaker: Taesik Na, Georgia Institute of Technology, US
Authors: Taesik Na and Saibal Mukhopadhyay, Georgia Institute of Technology, US

IP1-15 **LOSSLESS COMPRESSION ALGORITHM BASED ON DICTIONARY CODING FOR MULTIPLE E-BEAM DIRECT WRITE SYSTEM**
Speaker: Pei-Chun Lin, National Taiwan University, TW
Authors: Pei-Chun Lin, Yu-Hsuan Pai, Yu-Hsiang Chiu, Shao-Yuan Fang and Charlie Chung-Ping Chen, National Taiwan University, TW

IP1-16 **PHONOCMAP: AN APPLICATION MAPPING TOOL FOR PHOTONIC NETWORKS-ON-CHIP**
Speaker: Edoardo Fusella, University of Naples Federico II, IT
Authors: Edoardo Fusella and Alessandro Cilardo, University of Naples Federico II, IT

IP1-17 **DESIGN OF AN EFFICIENT READY QUEUE FOR EARLIEST-DEADLINE-FIRST (EDF) SCHEDULER**
Speaker: Risat Mahmud Pathan, Chalmers University of Technology, SE
Author: Risat Mahmud Pathan, Chalmers University of Technology, SE

IP1-18 **RT LEVEL TIMING MODELING FOR AGING PREDICTION**
Speaker: Nils Koppaetzky, OFFIS Institute for Information Technology, DE
Authors: Nils Koppaetzky[1], Malte Metzdorf[1], Reef Eilers[1], Domenik Helms[1] and Wolfgang Nebel[2]
[1]OFFIS Institute for Information Technology, DE; [2]University of Oldenburg and OFFIS, DE

4.1 Executive Track Panel: Trends & Challenges to Ensure Security

Saal 2 1700 - 1830

Organiser: **Yervant Zorian,** Synopsys, US

While the new chips in the mission critical applications keep growing both in functionality and numbers, protecting the security of their content remains a major challenge. The extent of connectedness and the wealth of accessibility provided in today's chips negatively impact the security of these applications. The speakers in this executive session will address the current trends and challenges of hardware security.

Executives:
Mike Borza, Synopsys, CA
Hagai Bar-El, ARM, US
Bill Eklow, Cisco Systems, US
Serge Leef, Mentor, US

4.2 Hot Topic: Nanoelectronic Design Tools Addressing Coupled Problems for 3D-IC Integration

Konferenz 6 1700 - 1830

Organisers: **Jan ter Maten,** University of Wuppertal, DE
Caren Tischendorf, Humboldt University of Berlin, DE
Chair: **Wim Schoenmaker,** Magwel NV, BE
Co-Chair: **Caren Tischendorf,** Humboldt University of Berlin, DE

The 3D-IC integration involves strong feedback coupled problems caused by electrical proximity and heat dissipation as well as new design challenges due to immense variety and complexity. New sophisticated modeling and simulation techniques are required in order to facilitate robust designs and enable complex analyses. Within a special hot-topic session, speakers from industry (NXP, ACCO Semiconductor), CAD tool vendors (MAGWEL NV, ON Semiconductor Belgium) and research institutions (University of Wuppertal, TU Darmstadt, Humboldt University of Berlin, Max Planck Institute for Dynamics of Complex Technical Systems, University of Applied Sciences Upper Austria) shall present new jointly developed CAD tools enabling coupled electromagnetic field-circuit-heat simulations, coupled electro-thermal-stress analyses as well as aging effect predictions based on enhanced, parameterized model order reduction techniques, multirate methods, monolithic field-circuit modeling, holistic electro-thermal modeling and uncertainty quantification via adapted probability distributions.

1700 **FAST TIME DOMAIN SIMULATION FOR RELIABLE FAULT DETECTION**
Speaker: Jos J. Dohmen, NXP Semiconductors, NL
Authors: Bratislav Tasic[1], Jos J. Dohmen[1], Rick Janssen[1], E. Jan W. ter Maten[2], Theo J.G. Beelen[3] and Roland Pulch[4]
[1]NXP Semiconductors, NL; [2]Bergische Universität Wuppertal, DE; [3]Eindhoven University of Technology, NL; [4]Ernst-Moritz-Arndt-Universität Greifswald, DE

1722 **HOLISTIC COUPLED FIELD AND CIRCUIT SIMULATION**
Speaker: Christian Strohm, Humboldt University of Berlin, DE
Authors: Peter Meuris[1], Wim Schoenmaker[1], Christian Strohm[2] and Caren Tischendorf[2]
[1]Magwel NV, Leuven, BE; [2]Humboldt University of Berlin, DE

1744 **MODEL ORDER REDUCTION FOR NANOELECTRONICS COUPLED PROBLEMS WITH MANY INPUTS**
Speaker: Nicodemus Banagaaya, Max Planck Institute for Dynamics of Complex Technical Systems, DE
Authors: Nicodemus Banagaaya[1], Lihong Feng[1], Wim Schoenmaker[2], Peter Meuris[2], Aarnout Wieers[3], Renaud Gillon[3] and Peter Benner[1]
[1]Max Planck Institute for Dynamics of Complex Technical Systems, DE; [2]Magwel NV, Leuven, BE; [3]ON Semiconductor, BE

1806 **SHAPE OPTIMIZATION OF A POWER MOS DEVICE TRANSISTOR UNDER UNCERTAINTIES**
Speaker: Piotr Putek, Bergische Universität Wuppertal, DE
Authors: Piotr Putek[1], Peter Meuris[2], Roland Pulch[3], E. Jan W. ter Maten[1], Michael Günther[1], Wim Schoenmaker[2], Frederik Deleu[4] and Aarnout Wieers[4]
[1]Bergische Universität Wuppertal, DE; [2]Magwel NV, Leuven, BE; [3]Ernst-Moritz-Arndt-Universität Greifswald, DE; [4]ON Semiconductor, BE

4.3 Firmware Security

Konferenz 1 1700 - 1830

Chair: **Nele Mentens,** Katholieke Universiteit Leuven, BE
Co-Chair: **Aurelien Francillon,** EURECOM, FR

The papers in this session tackle firmware security vulnerabilities caused by threats such as software updates and code reuse. Protection against such threats include special programming approaches, symbolic execution and authenticated encryption.

1700 **PRACTICAL EVALUATION OF CODE INJECTION IN ENCRYPTED FIRMWARE UPDATES**
Speaker: Oscar Guillen, Technische Universität München (TUM), DE
Authors: Oscar Guillen[1], Dawin Schmidt[2] and Georg Sigl[1]
[1]Technische Universität München (TUM), DE; [2]LMU München, DE

1730 **INTEGRATION OF ROP/JOP MONITORING IPS IN AN ARM-BASED SOC**
Speaker: Yunheung Paek, Seoul National University, KR
Authors: Yongje Lee, Jinyong Lee, Ingoo Heo, Dongil Hwang and Yunheung Paek, Seoul National University, KR

1800 **VERIFYING INFORMATION FLOW PROPERTIES OF FIRMWARE USING SYMBOLIC EXECUTION**
Speaker: Sharad Malik, Princeton University, US
Authors: Pramod Subramanyan[1], Sharad Malik[1], Hareesh Khattri[2], Abhranil Maiti[2] and Jason Fung[2]
[1]Princeton University, US; [2]Intel Corporation, US

IPS **IP2-1, IP2-2**

4.4 System-Level Energy Management

Konferenz 2 1700 - 1830

Chair: **William Fornaciari,** Politecnico di Milano - DEIB, IT
Co-Chair: **Soontae Kim,** KAIST, KR

The goal of this session is to provide a comprehensive perspective on the design and management of power and energy, tacking the problem from several standpoints. The first paper proposes a methodology to reduce the energy consumed by OLED displays exploiting image-specific pixel-by-pixel transformations, aimed at preserving the contrast of the image as much as possible while reducing the overall power. The second paper presents an efficient Energy Management Unit (EMU) to supply generic loads when the average harvested power is much smaller than required for sustained system operation. A dynamic energy burst scaling (DEBS) technique is proposed to dynamically configure the EMU. The third paper aims at optimizing acoustic monitoring by exploiting a two-stage architecture with a low power pattern

recognition for feature extraction, combined with an optimized wakeup stage.

1700 **LOW-OVERHEAD ADAPTIVE CONSTRAST ENHANCEMENT AND POWER REDUCTION FOR OLEDS**
Speaker: Massimo Poncino, Politecnico di Torino, IT
Authors: Daniele Jahier Pagliari, Massimo Poncino and Enrico Macii, Politecnico di Torino, IT

1730 **DYNAMIC ENERGY BURST SCALING FOR TRANSIENTLY POWERED SYSTEMS**
Speaker: Andres Gomez, ETH Zurich, US
Authors: Andres Gomez, Lukas Sigrist, Michele Magno, Luca Benini and Lothar Thiele, ETH Zurich, CH

1800 **LOW-POWER MULTICHANNEL SPECTRO-TEMPORAL FEATURE EXTRACTION CIRCUIT FOR AUDIO PATTERN WAKE-UP**
Speaker: Dinko Oletic, University of Zagreb, HR
Authors: Dinko Oletic[1], Vedran Bilas[1], Michele Magno[2], Norbert Felber[2] and Luca Benini[2]
[1]University of Zagreb, HR; [2]ETH Zurich, CH

4.5 Ultra-low Energy Memory Devices

Konferenz 3 1700 - 1830

Chair: **Fabien Clermidy,** CEA-Leti, FR
Co-Chair: **Walter Weber,** Namlab, DE

This session explores the use of emerging memory devices for energy efficiency. The first paper proposes a compact SRAM design employing silicon-based tunnel FETs. A new type of tunneling device is also used in the second paper to build circuits designs of flip-flops and latches. Finally, an energy saving system integration of non-volatile ternary content addressable memory cells is presented in the third paper.

1700 **3T-TFET BITCELL BASED TFET-CMOS HYBRID SRAM DESIGN FOR ULTRA-LOW POWER APPLICATIONS**
Speaker: Costin Anghel, Institut Supérieur d'électronique de Paris (ISEP), FR
Authors: Navneet Gupta[1], Adam Makosiej[2], Andrei Vladimirescu[3], Amara Amara[3] and Costin Anghel[3]
[1]Institut Supérieur d'Électronique de Paris (ISEP) and CEA-Leti, FR; [2]CEA-Leti, FR; [3]Institut Supérieur d'Électronique de Paris (ISEP), FR

1730 **DESIGN OF LATCHES AND FLIP-FLOPS USING EMERGING TUNNELING DEVICES**
Speaker: Xunzhao Yin, University of Notre Dame, US
Authors: Xunzhao Yin, Behnam Sedighi, Michael Niemier and Xiaobo Sharon Hu, University of Notre Dame, US

1800 **MASC: ULTRA-LOW ENERGY MULTIPLE-ACCESS SIGNLE-CHARGE TCAM FOR APPROXIMATE COMPUTING**
Speaker: Tajana Rosing, UC San Diego, US
Authors: Mohsen Imani[1], Shruti Patil[1] and Tajana Rosing[2]
[1]UC San Diego, US; [2]University of California, San Diego, US

4.6 Managing Multi-Core and Flash Memory

Konferenz 4 1700 - 1830

Chair: **Akash Kumar,** Technische Universität Dresden, DE
Co-Chair: **Olivier Sentieys,** INRIA, FR

This session deals with methods to improve the management of multi- and many-core systems and flash memories. Various constraints and objectives are considered: real-time, process variation, fairness, power consumption and performance.

1700 **DISTRIBUTED FAIR SCHEDULING FOR MANY-CORES**
Speaker: Anuj Pathania, Karlsruhe Institute of Technology (KIT), DE
Authors: Anuj Pathania[1], Vanchinathan Venkataramani[2], Muhammad Shafique[1], Tulika Mitra[2] and Jörg Henkel[1]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]National University of Singapore, SG

1730 **KEEP IT SLOW AND IN TIME: ONLINE DVFS WITH HARD REAL-TIME WORKLOADS**
Speaker: Kai Lampka, Uppsala University, SE
Authors: Kai Lampka and Björn Forsberg, Uppsala University, SE

1800 **EXPLOITING PROCESS VARIATION FOR RETENTION INDUCED REFRESH MINIMIZATION ON FLASH MEMORY**
Speaker: Yejia Di, Chongqing University, CN
Authors: Yejia Di[1], Liang Shi[1], Kaijie Wu[1] and Chun Jason Xue[2]
[1]Chongqing University, CN; [2]City University of Hong Kong, HK

IPS **IP2-3, IP2-4, IP2-5**

4.7 Modeling of Devices and Mixed-Signal Circuits

Konferenz 5 1700 - 1830

Chair: **Nuno Horta,** Instituto de Telecomunicacoes, PT
Co-Chair: **Jaijeet Roychowdhury,** UC Berkeley, US

This session contains papers presenting surrogate models for RF inductors, compact models for bipolar transistor and nonlinear models for low power DC-DC converters.

1700 **ACCURATE SYNTHESIS OF INTEGRATED RF PASSIVE COMPONENTS USING SURROGATE MODELS**
Speaker: Fabio Passos, CSIC, Universidad de Sevilla, ES
Authors: F. Passos, R. González-Echeverría, E. Roca, R. Castro-López and F. V. Fernández, CSIC, Universidad de Sevilla, ES

1730 **IMPLEMENTATION AND QUALITY TESTING FOR COMPACT MODELS IMPLEMENTED IN VERILOG-A**
Speaker: Anindya Mukherjee, Technische Universität Dresden, DE
Authors: Anindya Mukherjee[1], Andreas Pawlak[1], Michael Schröter[1], Didier Celi[2] and Zoltan Huszka[3]
[1]Technische Universität Dresden, DE; [2]ST, FR; [3]AMS, AG, HU

1800 **MULTI-HARMONIC NONLINEAR MODELING OF LOW-POWER PWM DC-DC CONVERTERS OPERATING IN CCM AND DCM**
Speaker: Dani Tannir, Lebanese American University, LB
Authors: Ya Wang[1], Di Gao[1], Dani Tannir[2] and Peng Li[1]
[1]Texas A&M University, US; [2]Lebanese American University, LB

4.8 Presentations from IoT-Campus (I): ASIC and Sensor Solutions

Exhibition Theatre 1700 - 1830

Exhibition Theatre session: see Exhibition Theatre Programme for details.

Exhibition Reception

Exhibition Area (Terrace Level) 1830 - 1930

The Exhibition Reception will take place on Tuesday, March 15, 2016, from 1830 - 1930 in the exhibition area (Terrace Level), where free drinks are offered for all conference delegates and exhibition visitors.

SPECIAL DAY

5.1 SPECIAL DAY Hot Topic: Building Confidence in Advanced Driver Assistance Systems

Saal 2 0830 - 1000

Organisers: **Samarjit Chakraborty,** Technische Universität München (TUM), DE
Wolfgang Ecker, Infineon Technologies, DE
Chair: **Sebastian Steinhorst,** TUM CREATE, SG
Co-Chair: **Kai Lampka,** Uppsala University, SE

With the recent evolutions of nanometer transistor technologies, power consumption emerged as the most critical limitation. Within advanced processors and computing architectures, the processor-memory communication accounts for a significant part of the energy requirement. While alternative design approaches, such as the use of optimized accelerators or advanced power management techniques are successfully employed in contemporary designs, the trend keeps worsening due to the ever-increasing gap between on-chip and off-chip memory data rates. This trend, known as Von Neumann bottleneck, not only limits the system performance, but also acts nowadays as a limiter of the energy scaling. The quest towards more energy efficiency requires solutions that solve the Von Neumann bottleneck by tightly intertwining computing with memories. In this hot topic session, we intend to elaborate on in-memory computing by identifying its current applications and its promises in light of emerging technologies. In-memory computing is considered here in the general sense of computing information locally within large data storage. Four talks will be provided. The first talk will cover the current industrial applications of in-memory computing to achieve energy efficient acceleration. The three other talks will explore the opportunities of in-memory systems realized with emerging technologies. In particular, we will see how the memristor theory can benefit to Cellular Neural Network (CNN). We will also dig into the recently introduced concept of memcomputing that promises to speed up the execution of NP-complete problems. Finally, we will present a novel computer architecture that relies on resistive memory elements to compute and store information.

0830 **AVAILABILITY AND INTERPRETABILITY OF OPTIMAL CONTROL FOR CRITICALITY ESTIMATION IN VEHICLE ACTIVE SAFETY**
Speaker: Wolfgang Utschick, Universität München (TUM), DE
Authors: Stephan Herrmann and Wolfgang Utschick, Technische Universität München (TUM), DE

0900 **CERTIFICATION ISSUES IN AUTOMOTIVE DRIVER ASSISTANCE SYSTEMS**
Speaker: Udo Steininger, TÜV SÜD Auto Service GmbH, DE
Author: Udo Steininger, TÜV SÜD Auto Service GmbH, DE

0930 **DEEP LEARNING IN ADVANCED DRIVER ASSISTANCE SYSTEMS**
Speaker: Qing Rao, Daimler AG, DE
Author: Qing Rao, Daimler AG, DE

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.2 Hot Topic: In-memory Computing: Status and Trends

Konferenz 6 0830 - 1000

Organiser: **Pierre-Emmanuel Gaillardon,** University of Utah, US
Chair: **Ian O'Connor,** Institute des Nanotechnologies de Lyon, FR
Co-Chair: **Michael Niemier,** University of Notre Dame, US

With the recent evolutions of nanometer transistor technologies, power consumption emerged as the most critical limitation. Within advanced processors and computing architectures, the processor-memory communication accounts for a significant part of the energy requirement. While alternative design approaches, such as the use of optimized accelerators or advanced power management techniques are successfully employed in contemporary designs, the trend keeps worsening due to the ever-increasing gap between on-chip and off-chip memory data rates. This trend, known as Von Neumann bottleneck, not only limits the system performance, but also acts nowadays as a limiter of the energy scaling. The quest towards more energy-efficiency requires solutions that solve the Von Neumann bottleneck by tightly intertwining computing with memories. In this hot topic session, we intend to elaborate on in-memory computing by identifying its current applications and its promises in light of emerging technologies. In-memory computing is considered here in the general sense of computing information locally within large data storage. Four talks will be provided. The first talk will cover the current industrial applications of in-memory computing to achieve energy efficient acceleration. The three other talks will explore the opportunities of in-memory systems realized with emerging technologies. In particular, we will see how the memristor theory can benefit to Cellular Neural Network (CNN). We will also dig into the recently introduced concept of memcomputing that promises to speed up the execution of NP-complete problems. Finally, we will present a novel computer architecture that relies on resistive memory elements to compute and store information.

0830 **SOFTWARE AND SYSTEM CO-OPTIMIZATION IN THE ERA OF HETEROGENEOUS COMPUTING**
Speaker: Ruchir Puri, IBM, US
Author: Ruchir Puri, IBM, US

0852 **FADING MEMORY EFFECTS IN A MEMRISTOR FOR CELLULAR NANOSCALE NETWORK APPLICATIONS**
Speaker: Alon Ascoli, Technische Universität Dresden, DE
Authors: Alon Ascoli[1], Ronald Tetzlaff[1], Leon O. Chua[2], John Paul Strachan[3] and R. Stanley Williams[3]
[1]Technische Universität Dresden, DE; [2]University of California, US; [3]Hewlett Packard Labs, US

0914 **DIGITAL MEMCOMPUTING MACHINES**
Speaker: Fabio L. Traversa, University of California San Diego, US
Authors: Massimiliano Di Ventra and Fabio L. Traversa, UC San Diego, US

0936 **THE PROGRAMMABLE LOGIC-IN-MEMORY (PLIM) COMPUTER**
Speaker: Pierre-Emmanuel Gaillardon, University of Utah, US
Authors: Pierre-Emmanuel Gaillardon[1], Luca Amaru[2], Anne Siemon[3], Eike Linn[3], Rainer Waser[3], Anupam Chattopadhyay[4] and Giovanni De Micheli[2]
[1]University of Utah, US; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH; [3]RWTH Aachen University, DE; [4]Nanyang Technological University, SG

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.3 Physical Attacks and Countermeasures

Konferenz 1 0830 - 1000

Chair: **Assia Tria,** CEA-Leti, FR
Co-Chair: **Francesco Regazzoni,** ALaRI, CH

This session presents recent improvements on physical attacks and countermeasures. Papers discuss how to reconstruct the logic function of a camouflaged circuit, propose sensors allowing to detect injection electromagnetic pulses and countermeasures against fault attacks implemented at register transfer level.

0830 **ORACLE-GUIDED INCREMENTAL SAT SOLVING TO REVERSE ENGINEER CAMOUFLAGED LOGIC CIRCUITS**
Speaker: Daniel Holcomb, University of Massachusetts, Amherst, US
Authors: Duo Liu, Cunxi Yu, Xiangyu Zhang and Daniel Holcomb
University of Massachusetts, Amherst, US

0900 **A FULLY-DIGITAL EM PULSE DETECTOR**
Speaker: David El-baze, Mines Saint-Etienne, FR
Authors: David El-Baze[1], Jean-Baptiste Rigaud[1] and Philippe Maurine[2]
[1]Mines Saint-Etienne, FR; [2]LIRMM, FR

0930 **ON THE DEVELOPMENT OF A NEW COUNTERMEASURE BASED ON A LASER ATTACK RTL FAULT MODEL**
Speaker: Athanasios Papadimitriou, Univ. Grenoble Alpes, LCIS F-26000, Valence, FR
Authors: Charalampos Ananiadis[1], Athanasios Papadimitriou[1], David Hely[1], Vincent Beroulle[1], Regis Leveugle[2] and Paolo Maistri[3]
[1]Univ. Grenoble Alpes, LCIS, F-26000, Valence, FR; [2]Univ. Grenoble Alpes, TIMA, F-38000, Grenoble, FR; [3]CNRS, TIMA, F-38000, Grenoble, FR

IPS **IP2-6, IP2-7**

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.4 Architectural-level Low-power Design

Konferenz 2 0830 - 1000

Chair: **Alberto Macii,** Politecnico di Torino, IT
Co-Chair: **Pascal Vivet,** CEA LETI, FR

This session will demonstrate some new techniques to minimize power consumption at architectural level. The first paper will present a 2-story power distribution network applied to a GPU. The technique is extended from circuit to architecture level. The workload is evenly partitioned between the cores so that the power network is never unbalanced. The second paper demonstrate many different write-assist techniques on a 4T SRAM structure in a dual-Vt Fin-FET technology. Those techniques are efficiently evaluated and applied to the 4T structure. The third paper of this session will focus on reliability issues due to dark silicon in processors. A new physical-based EM reliability will be presented to come up with a Q-learning methods to minimize the overall power consumption. Finally, an IP presentation will present two algorithms to detect and remove redundant resets for all registers in the design in one pass, saving design effort for RTL designers. This technique is demonstrated on multiple process technologies showing the impact on power and area.

0830 **MULTI-STORY POWER DISTRIBUTION NETWORKS FOR GPUS**
Speaker: Mark Gottscho, UCLA, US
Authors: Qixiang Zhang[1], Liangzhen Lai[2], Mark Gottscho[3] and Puneet Gupta[3]
[1]Zhejiang University, CN; [2]ARM/UCLA, US; [3]UCLA, US

0900 **ENERGY-EFFICIENT CACHE MEMORIES USING A DUAL-VT 4T SRAM CELL WITH READ-ASSIST TECHNIQUES**
Speaker: Massoud Pedram, University of Southern California, US
Authors: Alireza Shafaei Bejestan and Massoud Pedram
University of Southern California, US

0930 **LEARNING-BASED DYNAMIC RELIABILITY MANAGEMENT FOR DARK SILICON PROCESSOR CONSIDERING EM EFFECTS**
Speaker: Sheldon X.-D. Tan, University of California, Riverside, US
Authors: Taeyoung Kim[1], Xin Huang[1], Hai-Bao Chen[2], Valeriy Sukharev[3] and Sheldon X.-D. Tan[1]
[1]University of California, Riverside, US; [2]Shanghai Jiao Tong University, CN; [3]Mentor Graphics Corporation, US

IPS **IP2-8**

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.5 Alternative Computing Models

Konferenz 3 0830 - 1000

Chair: **Yiyu Shi,** University of Notre Dame, US
Co-Chair: **Sébastien Le Beux,** Ecole Centrale de Lyon, FR

The approximate nature of neuromorphic / machine learning approaches is explored from several perspectives. Two works focus on modeling techniques and tools for such architectures, while the third leverages approximate metrics of classification difficulty to trade between accuracy and classification cost.

0830 **MNSIM: SIMULATION PLATFORM FOR MEMRISTOR-BASED NEUROMORPHIC COMPUTING SYSTEM**
Speaker: Lixue Xia, Tsinghua University, CN
Authors: Lixue Xia[1], Boxun Li[1], Tianqi Tang[1], Peng Gu[2], Xiling Yin[1], Wenqin Huangfu[1], Pai-Yu Chen[3], Shimeng Yu[3], Yu Cao[3], Yu Wang[1], Yuan Xie[2] and Huazhong Yang[1]
[1]Tsinghua University, CN; [2]UC Santa Barbara, US; [3]Arizona State University, US

0900 **CONDITIONAL DEEP LEARNING FOR ENERGY-EFFICIENT AND ENHANCED PATTERN RECOGNITION**
Speaker: Priyadarshini Panda, Purdue University, US
Authors: Priyadarshini Panda, Abhronil Sengupta and Kaushik Roy, Purdue University, US

0930 **PROBABILISTIC ERROR MODELS FOR MACHINE LEARNING KERNELS IMPLEMENTED ON STOCHASTIC NANOSCALE FABRICS**
Speaker: Sai Zhang, University of Illinois at Urbana-Champaign, US
Authors: Sai Zhang and Naresh Shanbhag, University of Illinois at Urbana-Champaign, US

IPS **IP2-9**

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.6 Efficient System Modeling with SystemC

Konferenz 4 0830 - 1000

Chair: **Gunar Schirner,** Northeastern University, US
Co-Chair: **Christian Haubelt,** University of Rostock, DE

SystemC has become an important tool to enable system-level modeling and simulation for early concept validation, design space exploration and virtual prototyping. However, the predominant single-threaded discrete event kernels used for its simulation limit efficiency and applicability in modeling of large systems. This session features two research papers that explore different techniques for speeding up simulation by means of parallelizing the kernel and by exploiting properties of the time-decoupled modeling approach. The third paper investigates a new modeling technique and SystemC extension to enable fast and accurate simulation of analog/mixed signal systems.

0830 **A NEW PARALLEL SYSTEMC KERNEL LEVERAGING MANYCORE ARCHITECTURES**
Speaker: Nicolas Ventroux, CEA LIST, FR
Authors: Nicolas Ventroux and Tanguy Sassolas, CEA LIST, FR

0900 **SYSTEMC-LINK: PARALLEL SYSTEMC SIMULATION USING TIME-DECOUPLED SEGMENTS**
Speaker: Jan Henrik Weinstock, RWTH Aachen University, DE
Authors: Jan Henrik Weinstock[1], Rainer Leupers[1], Gerd Ascheid[1], Dietmar Petras[2] and Andreas Hoffmann[2]
[1]RWTH Aachen University, DE; [2]Synopsys GmbH, DE

0930 **ORTHOGONAL SIGNAL MODELING AND OPERATIONAL COMPUTATION OF AMS CIRCUITS FOR FAST AND ACCURATE SYSTEM SIMULATION**
Speaker: Leandro Gil, University of Stuttgart, DE
Authors: Leandro Gil and Martin Radetzki
University of Stuttgart, DE

IPS **IP2-10**

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.7 RF, Power Converters, and ADC: Innovative Design and Test Solutions

Konferenz 5 0830 - 1000

Chair: **Marie-Minerve Louerat,** Université Pierre & Marie Curie, (UPMC - Paris 6), FR
Co-Chair: **Christoph Grimm,** University of Kaiserslautern, DE

This session presents innovative solutions for test of millimeter-wave circuits, power monitoring, and ADC optimization

0830 **BUILT-IN TEST OF MILLIMETER-WAVE CIRCUITS BASED ON NON-INTRUSIVE SENSORS**
Speaker: Athanasios Dimakos, Université Grenoble Alpes, CNRS, TIMA, FR
Authors: Athanasios Dimakos[1], Haralampos-G. Stratigopoulos[2], Alexandre Siligaris[3], Salvador Mir[1] and Emeric De Foucauld[3]
[1]Université Grenoble Alpes, CNRS, TIMA, FR; [2]Sorbonne Universités, UPMC, FR; [3]CEA-Leti, FR

0900 **ADAPTIVE DELAY MONITORING FOR WIDE VOLTAGE-RANGE OPERATION**
Speaker: Jongho Kim, Seoul National University, KR
Authors: Jongho Kim[1], Gunhee Lee[1], Kiyoung Choi[1], Yonghwan Kim[2], Wook Kim[2], Kyungtae Do[2] and Jungyun Choi[2]
[1]Seoul National University, KR; [2]Samsung Electronics, KR

0930 **ANALYTICAL DESIGN OPTIMIZATION OF SUB-RANGING ADC BASED ON STOCHASTIC COMPARATOR**
Speaker: Md. Maruf Hossain, The University of Tokyo, JP
Authors: Md. Maruf Hossain, Tetsuya Iizuka, Toru Nakura and Kunihiro Asada, The University of Tokyo, JP

IPS **IP2-11, IP2-12**

1000 **COFFEE BREAK IN EXHIBITION AREA**

5.8 Model Based Design and Verification Day - Exhibition Keynote and Application Talk

Exhibition Theatre 0830 - 1000

Exhibition Theatre session: see Exhibition Theatre Programme for details.

IP2 Interactive Presentations

Conference Level, Foyer 1000 - 1030

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. Moreover, one "Best Interactive Presentation Award" will be given.

IP2-1 **ANALYZING THE IMPACT OF INJECTED SENSOR DATA ON AN ADVANCED DRIVER ASSISTANCE SYSTEM USING THE OP2TIMUS PROTOTYPING PLATFORM**
Speaker: Alexander Stühring, University of Oldenburg, DE
Authors: Alexander Stühring[1], Günter Ehmen[1] and Sibylle Fröschle[2]
[1]University of Oldenburg, DE; [2]OFFIS Institute for Information Technology, DE

IP2-2 **HARDWARE TROJANS IN INCOMPLETELY SPECIFIED ON-CHIP BUS SYSTEMS**
Speaker: Nicole Fern, UC Santa Barbara, US
Authors: Nicole Fern, Ismail San, Cetin Kaya Koc and Kwang-Ting (Tim) Cheng, UC Santa Barbara, US

IP2-3 **WORKLOAD-AWARE POWER OPTIMIZATION STRATEGY FOR ASYMMETRIC MULTIPROCESSORS**
Speaker: Emanuele Del Sozzo, Politecnico di Milano, IT
Authors: Emanuele Del Sozzo, Gianluca Durelli, Ettore Trainiti, Antonio Miele, Marco D. Santambrogio and Cristiana Bolchini, Politecnico di Milano, IT

IP2-4 **THE SLOWDOWN OR RACE-TO-IDLE QUESTION: WORKLOAD-AWARE ENERGY OPTIMIZATION OF SMT MULTICORE PLATFORMS UNDER PROCESS VARIATION**
Speaker: Anup Das, University of Southampton, GB
Authors: Anup Das, Geoff Merrett and Bashir Al-Hashimi, University of Southampton, GB

IP2-5 **TOWARDS GENERAL PURPOSE COMPUTATIONS ON LOW-END MOBILE GPUS**
Speaker: Leonidas Kosmidis, Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES
Authors: Matina Maria Trompouki[1] and Leonidas Kosmidis[2]
[1]Universitat Politècnica de Catalunya, ES; [2]Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES

IP2-6 **ESTIMATING DELAY DIFFERENCES OF ARBITER PUFS USING SILICON DATA**
Speaker: Keshab Parhi, University of Minnesota, US
Authors: Satya Venkata Sandeep Avvaru, Chen Zhou, Saroj Satapathy, Yingjie Lao, Chris Kim and Keshab Parhi, University of Minnesota, US

IP2-7 **ON THE USE OF FORWARD BODY BIASING TO DECREASE THE REPEATABILITY OF LASER-INDUCED FAULTS**
Speaker: Marc Lacruche, Ecole Nationale Supérieure des Mines de Saint Etienne (ENSM-SE), FR
Authors: Marc Lacruche[1], Noemie Beringuier-Boher[1], Jean-Max Dutertre[1], Jean-Baptiste Rigaud[1] and Edith Kussener[2]
[1]Ecole Nationale Supérieure des Mines de Saint Etienne (ENSM-SE), FR; [2]IM2NP, FR

IP2-8 **SEQUENTIAL ANALYSIS DRIVEN RESET OPTIMIZATION TO IMPROVE POWER, AREA AND ROUTABILITY**
Speaker: Srihari Yechangunja, Mentor Graphics Corporation, IN
Authors: Srihari Yechangunja[1], Raj Shekhar[1], Mohit Kumar[1], Nikhil Tripathi[1], Abhishek Ranjan[1], Abhishek Mittal[1], Jianfeng Liu[2], Minyoung Mo[2], Kyungtae Do[2], Jung Yun Choi[2] and SungHo Park[2]
[1]Mentor Graphics Corporation, IN; [2]S.LSI, Samsung Electronics Co. Ltd, KR

IP2-9 **EFFICIENT GLOBAL OPTIMIZATION OF MEMS BASED ON SURROGATE MODEL ASSISTED EVOLUTIONARY ALGORITHM**
Speaker: Bo Liu, Glyndwr University, GB
Authors: Bo Liu[1] and Anna Nikolaeva[2]
[1]Glyndwr University, GB; [2]Bauman Moscow State Technical University, RU

IP2-10 **EFFICIENT MONITORING OF LOOSE-ORDERING PROPERTIES FOR SYSTEMC TLM**
Speaker: Yuliia Romenska, Univ. Grenoble Alpes, VERIMAG, FR
Authors: Yuliia Romenska[1] and Florence Maraninchi[2]
[1]Univ. Grenoble Alpes, VERIMAG, FR; [2]Grenoble INP & Verimag, FR

IP2-11 **TESTABLE DESIGN OF REPEATERLESS LOW SWING ON-CHIP INTERCONNECT**
Speaker: Naveen Kadayinti, Indian Institute of Technology Bombay, IN
Authors: Naveen Kadayinti and Dinesh Sharma, Indian Institute of Technology Bombay, IN

IP2-12 **ALL-DIGITAL HYBRID-CONTROL BUCK CONVERTER FOR INTEGRATED VOLTAGE REGULATOR APPLICATIONS**
Speaker: Visvesh Sathe, University of Washington, US
Authors: Ta-tung Yen, Bin Yu and Visvesh Sathe, University of Washington, US

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

6.1 SPECIAL DAY Hot Topic: Formal Methods for Automotive Software

Saal 2 1100 - 1230

Chair: **Marc Geilen,** Eindhoven University of Technology, NL
Co-Chair: **Wolfgang Ecker,** Infineon Technologies, DE

The growing complexity of automotive software has led to the increasing focus on the use of formal methods for automotive software development and validation. This session will feature three invited talks giving different perspectives on the use of formal methods for automotive software development. This will include techniques for the verification of control software code to timing analysis of automotive software.

1100 **REQUIREMENTS ENGINEERING FOR SOFTWARE-INTENSIVE AUTOMOTIVE EMBEDDED SYSTEMS**
Speaker: Manfred Broy, Technische Universität München (TUM), DE
Author: Manfred Broy, Technische Universität München (TUM), DE

1130 **FORMAL SPECIFICATION AND VERIFICATION OF AUTOMOTIVE SOFTWARE IN PRACTICE**
Speaker: Ravindra Metta, TCS Innovation Labs, IN
Author: Ravindra Metta, TCS Innovation Labs, IN

1200 **TIMING ANALYSIS OF AUTOMOTIVE ARCHITECTURES AND SOFTWARE**
Speaker: Nicolas Navet, University of Luxembourg and RealTime-at-Work, LU
Author: Nicolas Navet, University of Luxembourg and RealTime-at-Work, LU

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

6.2 Panel: Looking Backwards and Forwards

Konferenz 6 1100 - 1230

Organiser: **Marco Casale-Rossi,** Synopsys, US
Chair: **Marco Casale-Rossi,** Synopsys, US
Co-Chair: **Giovanni De Micheli,** École Polytechnique Fédérale de Lausanne (EPFL), CH

Ten years ago, at 90 nanometers EDA was challenged, and deemed inadequate in dealing with increasing complexity, power consumption, and sub-wavelength lithography, thus harming the progress of mobile phones. Today, at 10 nanometers integration capacity has increased by two orders of magnitude, power consumption has been successfully "defeated", and 193 nanometer immersion lithography is still relied uponâ ¦ *also* thanks to EDA; tools, methodologies, and flows that were originally devised for design enablement at the emerging technology nodes, have been successfully re-deployed at the established technology nodes, where they represent a critical design differentiation factor. However, the battleground is changing again: after the billions of phones, trillions of "things" lie ahead; moving forward, emerging and established technology nodes, digital and analog, hardware and software will be equally critical. What is EDA doing and, more important, what should EDA do - and is not doing - in order for the next decade to be as great as the past one? This panel session, moderated by EPFL Professor Giovanni De Micheli, gathers academia, semiconductor, and EDA industry to discuss the challenges and the requirements of the new era.

MODERATOR:
Giovanni De Micheli, École Polytechnique Fédérale de Lausanne (EPFL), CH

PANELISTS:
Antun Domic, Synopsys, US
Enrico Macii, Politecnico di Torino, IT
Domenico Rossi, STMicroelectronics, IT
Joseph Sawicki, Mentor, US

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

6.3 Anti-aging and Error Protection using Checkpointing and DVFS

Konferenz 1 1100 - 1230

Chair: **Antonio Rosario Miele,** Polimi, IT
Co-Chair: **Jose L. Ayala,** Complutense University of Madrid, ES

As reliability becomes a major concern for both designers and technologists, techniques such as error protection is needed to keep the best known state and preserve it for subsequent operations. In this session various methods of checkpointing at register level and at memory level are presented that relieve systems from aging. Various combinations of DVFS and checkpointing techniques are presented in this session including techniques that exploit application level tolerability to errors.

1100 **AGING-AWARE VOLTAGE SCALING**
Speaker: Hussam Amrouch, Karlsruhe Institute of Technology (KIT), DE
Authors: Victor M. van Santen[1], Hussam Amrouch[1], Narendra Parihar[2], Souvik Mahapatra[2] and Jörg Henkel[1]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]Indian Institute of Technology Bombay, IN

1130 **RECORD: REDUCING REGISTER TRAFFIC FOR CHECKPOINTING IN RELIABLE EMBEDDED PROCESSORS**
Speaker: Sri Parameswaran, University of New South Wales, AU
Authors: Tuo Li[1], Jude Angelo Ambrose[2] and Sri Parameswaran[1]
[1]University of New South Wales, AU; [2]Canon Information Systems Research Australia, AU

1200 **ERROR RESILIENCE AND ENERGY EFFICIENCY: AN LDPC DECODER DESIGN STUDY**
Speaker: Philipp Schläfer, University of Kaiserslautern, DE
Authors: Philipp Schläfer[1], Chu-Hsiang Huang[2], Clayton Schoeny[2], Christian Weis[1], Yao Li[3], Norbert Wehn[1] and Lara Dolecek[2]
[1]University of Kaiserslautern, DE; [2]University of California, Los Angeles, US; [3]Akamai Inc., US

1215 **RUNTIME INTERVAL OPTIMIZATION AND DEPENDABLE PERFORMANCE FOR APPLICATION-LEVEL CHECKPOINTING**
Speaker: Dimitrios Rodopoulos, ICCS/NTUA, GR
Authors: Apostolos Kokolis[1], Alexandros Mavrogiannis[1], Dimitrios Rodopoulos[2], Christos Strydis[3] and Dimitrios Soudris[1]
[1]NTUA, GR; [2]ICCS/NTUA, GR; [3]Erasmus MC, NL

IPS **IP3-1**

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

6.4 Power Modeling and Power Aware Synthesis

Konferenz 2 1100 - 1230

Chair: **Alberto Garcia Ortiz,** University of Bremen, DE
Co-Chair: **Qi Zhu,** UCR, US

Papers in this session address methods for power efficient design of digital systems. The first paper presents an FPGA emulation for design trade-offs. The second paper proposes a methodology to automatically generate power state machine models for SoCs. The third paper presents an automatic method to place isolation gates trading off precision and power dissipation. The IP paper investigates circuit verification of power grids.

1100 **A SYSTEMATIC APPROACH TO AUTOMATED CONSTRUCTION OF POWER EMULATION MODELS**
Speaker: Benjamin Andreassen Bjørnseth, Norwegian University of Science and Technology, NO
Authors: Benjamin Andreassen Bjørnseth, Asbjørn Djupdal and Lasse Natvig, Norwegian University of Science and Technology, NO

1130 **AUTOMATIC GENERATION OF POWER STATE MACHINES THROUGH DYNAMIC MINING OF TEMPORAL ASSERTIONS**
Speaker: Graziano Pravadelli, University of Verona, IT
Authors: Alessandro Danese, Ivan Zandonà and Graziano Pravadelli, University of Verona, IT

1200 **APPROXIMATION THROUGH LOGIC ISOLATION FOR THE DESIGN OF QUALITY CONFIGURABLE CIRCUITS**
Speaker: Shubham Jain, Purdue University, US
Authors: Shubham Jain, Swagath Venkataramani and Anand Raghunathan, Purdue University, US

IPS **IP3-2**

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

6.5 Biochips

Konferenz 3 1100 - 1230

Chair: **Robert Wille,** JKU, AT
Co-Chair: **Ian O'Connor,** Ecole Centrale de Lyon, FR

This session focuses on design methods for biochips. The first paper presents a methodology for synthesizing fault-tolerant biochips. The second paper proposes a synthesis method considering sieve valves, a key component in flow-based microfluidic biochips. Finally the third paper proposes a design automation framework for quantitative gene expression on cyberphysical digital microfluidic biochips.

1100 **ARCHITECTURE SYNTHESIS FOR COST-CONSTRAINED FAULT-TOLERANT FLOW-BASED BIOCHIPS**
Speaker: Seetal Potluri, Technical University of Denmark, IN
Authors: Morten Chabert Eskesen, Paul Pop and Seetal Potluri, Technical University of Denmark, DK

1130 **SIEVE-VALVE-AWARE SYNTHESIS OF FLOW-BASED MICROFLUIDIC BIOCHIPS CONSIDERING SPECIFIC BIOLOGICAL EXECUTION LIMITATIONS**
Speaker: Mengchu Li, Technische Universität München (TUM), DE
Authors: Mengchu Li[1], Tsun-Ming Tseng[1], Bing Li[1], Tsung-Yi Ho[2] and Ulf Schlichtmann[1]
[1]Technische Universität München (TUM), DE; [2]National Tsing Hua University, TW

1200 **INTEGRATED AND REAL-TIME QUANTITATIVE ANALYSIS USING CYBERPHYSICAL DIGITAL-MICROFLUIDIC BIOCHIPS**
Speaker: Mohamed Ibrahim, Duke University, US
Authors: Mohamed Ibrahim, Krishnendu Chakrabarty and Kristin Scott, Duke University, US

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

6.6 Modelling and Control of Cyber-Physical Systems

Konferenz 4 1100 - 1230

Chair: **Donatella Sciuto,** Politecnico di Milano, IT
Co-Chair: **Paul Pop,** Technical University of Denmark, DK

The session has two papers on improving the quality-of-control for cyber-physical systems, targeting the timing analysis of self-triggered controllers and the optimization of resources in a partitioned architecture. Two other papers are on modeling aspects of the human body for cyber-physical medical applications: modeling the brain-machine-body interface and a model for the electrical conduction of the human heart. One of the interactive presentations is on security aspects of vehicular systems, and the second interactive presentation is on the online control of jobs in production systems.

1100 **SELF-TRIGGERED CONTROLLERS AND HARD REAL-TIME GUARANTEES**
Speaker: Amir Aminifar, Linköping University, SE
Authors: Amir Aminifar[1], Paulo Tabuada[2], Petru Eles[1] and Zebo Peng[1]
[1]Linköping University, SE; [2]University of California at Los Angeles, US

1130 **A SPATIO-TEMPORAL FRACTAL MODEL FOR A CPS APPROACH TO BRAIN-MACHINE-BODY INTERFACES**
Speaker: Yuankun Xue, University of Southern California, US
Authors: Yuankun Xue, Saul Rodriguez and Paul Bogdan, University of Southern California, US

1200 **MODULAR CODE GENERATION FOR EMULATING THE ELECTRICAL CONDUCTION SYSTEM OF THE HUMAN HEART**
Speaker: Nathan Allen, University of Auckland, NZ
Authors: Nathan Allen[1], Sidharta Andalam[1], Partha Roop[1], Avinash Malik[1], Mark Trew[2] and Nitish Patel[1]
[1]University of Auckland, NZ; [2]Auckland Bioengineering Institute, NZ

1215 **RESOURCE UTILIZATION AND QUALITY-OF-CONTROL TRADE-OFF FOR A COMPOSABLE PLATFORM**
Speaker: Juan Valencia, Eindhoven University of Technology, NL
Authors: Juan Valencia, Eelco van Horssen, Dip Goswami, Maurice Heemels and Kees Goossens, Eindhoven University of Technology, NL

IPS **IP3-3, IP3-4**

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

6.7 Fault Tolerant Systems and Methods

Konferenz 5 1100 - 1230

Chair: **Viacheslav Izosimov,** Semcon Sweden AB, SE
Co-Chair: **Zebo Peng,** Linköping University, SE

The papers in this session present arithmetic components for approximate and fault tolerant computing, self-checking methodologies and tools for the implementation and evaluation of reliable systems

WEDNESDAY 16 MARCH, 2016

DATE16
March 14–18, 2016, Dresden, Germany
WED

1100 **INEXACT DESIGNS FOR APPROXIMATE LOW POWER ADDITION BY CELL REPLACEMENT**
Speaker: Nandha Kumar Thulasiraman, The University of Nottingham, MY
Authors: Haider A.F. Almurib[1], Nandha Kumar Thulasiraman[1] and Fabrizio Lombardi[2]
[1]The University of Nottingham, MY; [2]Northeastern University, US

1130 **A GENERAL APPROACH FOR HIGHLY DEFECT TOLERANT PARALLEL PREFIX ADDER DESIGN**
Speaker: Wenjing Rao, University of Illinois at Chicago, US
Authors: Soumya Banerjee and Wenjing Rao, University of Illinois at Chicago, US

1200 **INVERTERS' SELF-CHECKING MONITORS FOR RELIABLE PHOTOVOLTAIC SYSTEMS**
Speaker: Cecilia Metra, Università di Bologna, IT
Authors: Martin Omana, Alessandro Fiore and Cecilia Metra, Università di Bologna, IT

IPS **IP3-5, IP3-6**

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

6.8 Presentations from 5G-Campus and European Projects Booths: 5G for the Connected World, Optimizing Computing Everywhere

Exhibition Theatre 1100 - 1230

Exhibition Theatre session: see Exhibition Theatre Programme for details.

7.0 LUNCH TIME KEYNOTE SESSION

Saal 2 1400 - 1430

Chair: **Luca Fanucci,** University of Pisa, IT
Co-Chair: **Wolfgang Ecker,** Infineon Technologies, DE

The lunch keynote presentation will be given by Dr. Patrick Leteinturier, Fellow of Automotive Systems at Infineon Technologies. He will present his vision on how cars of the future will impact and dramatically change personal mobility.

1400 **THE CAR OF THE FUTURE WILL REINVENT PERSONAL MOBILITY**
Speaker: Patrick Leteinturier, Infineon Technologies, DE
Author: Patrick Leteinturier, Infineon Technologies, DE

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.1 SPECIAL DAY Panel: Which EDA Solutions can the Automotive Domain Reuse? Very Few or All?

Saal 2 1430 - 1600

Chair: **Adam Morawiec,** European Chips & Systems Design Initiative (ESCI), FR

This panel will debate on whether and how much of existing EDA solutions may extend to the automotive domain. Given the unique features of the automotive domain such as cost pressures, safety criticality, and complexity, it is not clear whether the automotive domain needs completely new and custom-made EDA techniques or whether existing techniques may be largely reused.

MODERATOR:
Oliver Bringmann, Universität Tübingen / FZI, DE

PANELISTS:
Rainer Kress, Infineon Technologies, DE
Gabriele Ernst, Robert Bosch GmbH, DE
Jean-Marie Saint-Paul, Mentor, FR
Silvano Motto, Yogitech, IT
Christoph Störmer, ETAS, DE

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.2 EU Projects Special Session: Energy Efficiency drives Design

Konferenz 6 1430 - 1600

Organiser: **Roberto Giorgi,** University of Siena, IT
Chair: **Martin Schoeberl,** Technical University of Denmark, DK
Co-Chair: **Roberto Giorgi,** University of Siena, IT

Energy efficiency is a key non-functional property that is currently a number one goal of many designs. In this session several projects focused on future datacenters are illustrated. The adopted solutions and technologies are driving the design of next energy efficient smart embedded systems too.

1430 **EUROSERVER: SHARE-ANYTHING SCALE-OUT MICRO-SERVER DESIGN**
Speaker: Manolis Marazakis, FORTH, GR
Authors: Manolis Marazakis[1], John Goodacre[2], Didier Fuin[3], Paul Carpenter[4], John Thomson[5], Emil Matus[6], Antimo Bruno[7], Per Stenström[8], Jerome Martin[9], Yves Durand[9] and Isabelle Dor[9]
[1]FORTH, GR; [2]ARM Ltd, GB; [3]STMicroelectronics, FR; [4]Barcelona Supercomputing Center, ES; [5]ONAPP Ltd, GB; [6]Technische Universität Dresden, DE; [7]NEAT Srl, IT; [8]Chalmers University of Technology, SE; [9]CEA, FR

1445 **ENERGY MINIMIZATION AT ALL LAYERS OF THE DATA CENTER: THE PARADIME PROJECT**
Speaker: Christof Fetzer, Technische Universität Dresden, DE
Authors: Oscar Palomar[1], Santhosh Kumar Rethinagiri[2], Gulay Yalcin[1], Rubén Titos-Gil[1], Pablo Prieto[1], Emma Torrella[1], Osman Unsal[1], Adrián Cristal[1], Pascal Felber[3], Anita Sobe[3], Yaroslav Hayduk[3], Mascha Kurpicz[3], Christof Fetzer[4], Thomas Knauth[4], Malte Schneegaß[5], Jens Struckmeier[5] and Dragomir Milojevic[6]
[1]Barcelona Supercomputing Center, ES; [2]BSC-Microsoft Research Center, ES; [3]University of Neuchâtel, CH; [4]Technische Universität Dresden, DE; [5]Cloud & Heat, DE; [6]IMEC, BE

1500 **RACK-SCALE DISAGGREGATED CLOUD DATA CENTERS: THE DREDBOX PROJECT VISION**
Speaker: Dimitris Syrivelis, University of Thessaly, GR
Authors: Kostas Katrinis[1], Dimitris Syrivelis[2], Dionisios Pnevmatikatos[3], Georgios Zervas[4], Dimitris Theodoropoulos[5], Iordanis Koutsopoulos[6], Kobi Hasharoni[7], Daniel Raho[8], Christian Pinto[8], Felix Espina[9], Sergio Lopez-Buedo[9], Qianqiao Chen[4], Mario Nemirovsky[10], Damian Roca[10], Hans Klos[11] and Tom Berends[11]
[1]IBM Research Ireland, IE; [2]University of Thessaly, GR; [3]ECE Department, Technical Univrsity of Crete & FORTH-ICS, GR; [4]HPN group, University of Bristol, GB; [5]Foundation for Research and Technology Hellas (FORTH), GR; [6]Athens University of Economics and Business, GR; [7]Compass-EOS, IL; [8]Virtual Open Systems, FR; [9]NAUDIT HPCN, ES; [10]Barcelona Supercomputing Center, ES; [11]SINTECS, NL

1515 **ECOSCALE: RECONFIGURABLE COMPUTING AND RUNTIME SYSTEM FOR FUTURE EXASCALE SYSTEMS**
Speaker: Iakovos Mavroidis, Telecommunication Systems Institute, GR
Authors: Iakovos Mavroidis[1], Ioannis Papaefstathiou[2], Luciano Lavagno[3], Dimitrios Nikolopoulos[4], Dirk Koch[5], John Goodacre[5], Ioannis Sourdis[6], Vassilis Papaefstathiou[6], Marcello Coppola[7] and Manuel Palomino[8]
[1]Telecommunication Systems Institute, GR; [2]Synelixis, GR; [3]Politecnico di Torino, IT; [4]Queen's University of Belfast, GB; [5]University of Manchester, GB; [6]Chalmers University of Technology, SE; [7]STMicroelectronics, FR; [8]Acciona Infraestructuras S.A., ES

1530 **ENABLING HPC FOR QOS-SENSITIVE APPLICATIONS: THE MANGO APPROACH**
Speaker: José Flich, Universitat Politècnica de València, ES
Authors: José Flich[1], Giovanni Agosta[2], Philipp Ampletzer[3], David Atienza[4], Alessandro Cilardo[5], William Fornaciari[6], Ynse Hoornengorb[7], Mario Kovac[8], Bruno Maitre[9], Giuseppe Massari[2], Ermis Papastefanakis[9], Fabrice Roudet[10], Rafael Tornero[1] and Davide Zoni[2]
[1]Universitat Politècnica de València, ES; [2]Politecnico di Milano, IT; [3]ProDesign, DE; [4]École Polytechnique Fédérale de Lausanne (EPFL), CH; [5]University of Naples Federico II, IT; [6]Politecnico di Milano - DEIB, IT; [7]Philips Medical, NL; [8]Zagreb University, HR; [9]Thales Communication, FR; [10]EATON, FR

1545 **AUTOTUNING AND ADAPTIVITY APPROACH FOR ENERGY EFFICIENT EXASCALE HPC SYSTEMS: THE ANTAREX APPROACH**
Speaker: Cristina Silvano, Politecnico di Milano, IT
Authors: Cristina Silvano[1], Giovanni Agosta[1], Andrea Bartolini[2], Andrea Beccari[3], Luca Benini[2], João Bispo[4], João M. P. Cardoso[5], Carlo Cavazzoni[6], Jan Martinovic[7], Gianluca Palermo[1], Martin Palkovic[7], Pedro Pinto[8], Erven Rohou[9], Nico Sanna[6] and Katerina Slaninova[7]
[1]Politecnico di Milano, IT; [2]Università di Bologna, IT; [3]Dompe' Farmaceutici SpA, IT; [4]Faculty of Engineering (FEUP), University of Porto, PT; [5]University of Porto, PT; [6]CINECA, IT; [7]IT4Innovation National Supercomputing Center, CZ; [8]Faculty of Engineering, University of Porto, PT; [9]INRIA Rennes, FR

IPS **IP3-7**

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.3 Low Power Devices and Methods for Healthcare and Assisted Living

Konferenz 1 1430 - 1600

Chair: **José M. Moya,** Technical University of Madrid, ES
Co-Chair: **Giovanni Ansaloni,** University of Lugano, CH

This session addresses energy efficiency for ambient intelligence and healthcare. The first part focuses on systems for fall detection and indoor localization in the context of ambient assisted living. The second part is dedicated to methods for cardiovascular monitoring, including low-power real-time diagnosis and efficient communication.

1430 **A DIGITAL PROCESSOR ARCHITECTURE FOR COMBINED EEG/EMG FALLING RISK PREDICTION**
Speaker: Daniela De Venuto, Politecnico di Bari, IT
Authors: Valerio F. Annese[1], Sabino Loconte[1], Marco Crepaldi[2], Danilo Demarchi[3] and Daniela De Venuto[1]
[1]Politecnico di Bari, IT; [2]Center for Space Human Robotics (CSHR), Istituto Italiano di Tecnologia, IT; [3]Politecnico di Torino, IT

1500 **DISTRIBUTED-NEURON-NETWORK BASED MACHINE LEARNING ON SMART-GATEWAY NETWORK TOWARDS REAL-TIME INDOOR DATA ANALYTICS**
Speaker: Hantao Huang, Nanyang Technological University, SG
Authors: Hantao Huang, Yuehua Cai and Hao Yu, Nanyang Technological University, SG

1530 **TOUCH-BASED SYSTEM FOR BEAT-TO-BEAT IMPEDANCE CARDIOGRAM ACQUISITION AND HEMODYNAMIC PARAMETERS ESTIMATION**
Speaker: Dionisije Sopic, École Polytechnique Fédérale de Lausanne (EPFL), CH
Authors: Dionisije Sopic[1], Srinivasan Murali[2], Francisco Rincón[2] and David Atienza[1]
[1]École Polytechnique Fédérale de Lausanne (EPFL), CH; [2]SmartCardia Inc., Ltd, CH

1545 **QUANTIFYING THE BENEFITS OF COMPRESSED SENSING ON A WBSN-BASED REAL-TIME BIOSIGNAL MONITOR**
Speaker: Daniele Bortolotti, Università di Bologna, IT
Authors: Daniele Bortolotti[1], Bojan Milosevic[2], Andrea Bartolini[3], Elisabetta Farella[2] and Luca Benini[3]
[1]Università di Bologna, IT; [2]Fondazione Bruno Kessler, IT; [3]ETH Zurich, CH

IPS **IP3-8, IP3-9, IP3-10**

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.4 System-Level Synthesis

Konferenz 2 1430 - 1600

Chair: **Cathal McCabe,** Xilinx, Inc. Ireland, IE
Co-Chair: **Yuichi Nakamura,** NEC Japan, JP

This session is centered around topics in System-Level Synthesis, with specific focus on hardware threads, composable templates, and evaluation of fixed-point systems. The session concludes with a short IP presentation on asynchronous circuit synthesis for cryptographic applications.

1430 **SYSTEM LEVEL SYNTHESIS FOR VIRTUAL MEMORY ENABLED HARDWARE THREADS.**
Speaker: Nicolas Estibals, IRISA, FR
Authors: Steven Derrien[1], Nicolas Estibals[2], Gaël Deest[3] and Ali Hassan El Moussawi[3]
[1]IRISA, FR; [2]University of Rennes 1/IRISA, FR; [3]University of Rennes 1, FR

1500 **COMPOSABLE, PARAMETERIZABLE TEMPLATES FOR HIGH-LEVEL SYNTHESIS**
Speaker: Dajung Lee, University of California, San Diego, US
Authors: Janarbek Matai, Dajung Lee, Alric Althoff and Ryan Kastner, University of California, San Diego, US

1530 **LEVERAGING POWER SPECTRAL DENSITY FOR SCALABLE SYSTEM-LEVEL ACCURACY EVALUATION**
Speaker: Benjamin Barrois, University of Rennes, INRIA, FR
Authors: Benjamin Barrois[1], Karthick Parashar[2] and Olivier Sentieys[3]
[1]University of Rennes, INRIA, FR; [2]IMEC, BE; [3]INRIA, FR

IPS **IP3-11**

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.5 Emerging Memory Architectures

Konferenz 3 1430 - 1600

Chair: **Amara Amara,** ISEP, FR
Co-Chair: **Fabian Oboril,** Karlsruhe Institute of Technology, DE

The first paper presents a method to utilize the variations in RRAM access latency due to IR drop in a given array. The second paper exploits the spatial and temporal locality of cache access, and proposes an ECC scheme wherein write operations with potentially different error rates are mapped to regions with different ECC strengths. The third paper proposes a write scheme for phase change memory to minimize the number of write units.

1430 **LEADER: ACCELERATING RERAM-BASED MAIN MEMORY BY LEVERAGING ACCESS LATENCY DISCREPANCY IN CROSSBAR ARRAYS**
Speaker: Hang Zhang, National University of Defense Technology, CN
Authors: Hang Zhang, Nong Xiao, Fang Liu and Zhiguang Chen, National University of Defense Technology, CN

1500 **SLIDING BASKET: AN ADAPTIVE ECC SCHEME FOR RUNTIME WRITE FAILURE SUPPRESSION OF STT-RAM CACHE**
Speaker: Yiran Chen, University of Pittsburgh, US
Authors: Xue Wang[1], Mengjie Mao[1], Wujie Wen[2], Enes Eken[1], Hai Li[1] and Yiran Chen[1]
[1]University of Pittsburgh, US; [2]Florida International University, US

1530 **EXPLOITING MORE PARALLELISM FROM WRITE OPERATIONS ON PCM**
Speaker: Zheng Li, Huazhong University of Science and Technology, CN
Authors: Zheng Li, Fang Wang, Yu Hua, Wei Tong, Jingning Liu, Yu Chen and Dan Feng, Huazhong University of Science and Technology, CN

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.6 Statistical and Symbolic Techniques for the Analysis and Testing of Embedded Software

Konferenz 4 1430 - 1600

Chair: **Jian-Jia Chen,** Technische Universität Dortmund, DE
Co-Chair: **Petru Eles,** Linköping University, SE

This session presents new approaches that enable efficient analysis and testing of embedded software. The first paper presents an interesting dynamic partitioning strategy to reduce the complexity of symbolic execution based software testing. An extension to UML activity diagrams towards stocastic modeling is proposed in the second paper; this allows for quantitative reasoning based on statistical model checking techniques. The final paper presents a new testing methodology that combines symbolic decision procedures with statistical hypothesis testing to study the correctness of intelligent embedded systems.

1430 **DYNAMIC PARTITIONING STRATEGY TO ENHANCE SYMBOLIC EXECUTION**
Speaker: Brendan Marcellino, Virginia Tech, US
Authors: Brendan Marcellino and Michael Hsiao, Virginia Tech, US

1500 **QUANTITATIVE TIMING ANALYSIS OF UML ACTIVITY DIAGRAMS USING STATISTICAL MODEL CHECKING**
Speaker: Mingsong Chen, East China Normal University, CN
Authors: Fan Gu[1], Xinqian Zhang[1], Mingsong Chen[1], Daniel Grosse[2] and Rolf Drechsler[2]
[1]East China Normal University, CN; [2]University of Bremen, DE

1530 **INTEGRATING SYMBOLIC AND STATISTICAL METHODS FOR TESTING INTELLIGENT SYSTEMS: APPLICATIONS TO MACHINE LEARNING AND COMPUTER VISION**
Speaker: Sumit Kumar Jha, University of Central Florida, US
Authors: Arvind Ramanathan[1], Laura Pullum[1], Faraz Hussain[2], Dwaipayan Chakraborty[2] and Sumit Kumar Jha[2]
[1]Oak Ridge National Laboratory, US; [2]University of Central Florida, US

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.7 Aging Mitigation to Improve System Robustness

Konferenz 5 1430 - 1600

Chair: **Maria Michael,** University of Cyprus, CY
Co-Chair: **Carles Hernandez,** Barcellona Supercomputer Center, ES

This session presents methodologies for monitoring aging effects in FPGAs and task mapping strategies for prolonging lifetime in robust multi/many-core systems

1430 **PATH SELECTION AND SENSOR INSERTION FLOW FOR AGE MONITORING IN FPGAS**
Speaker: Mohammad Ebrahimi, University of Tehran, IR
Authors: Mohammad Ebrahimi[1], Zana Ghaderi[2], Eli Bozorgzadeh[2] and Zainalabedin Navabi[1]
[1]University of Tehran, IR; [2]University of California, Irvine, US

1500 **DESIGN AND EVALUATION OF RELIABILITY-ORIENTED TASK RE-MAPPING IN MPSOCS USING TIME-SERIES ANALYSIS OF INTERMITTENT FAULTS**
Speaker: Siva Satyendra Sahoo, National University of Singapore, SG
Authors: Siva Satyendra Sahoo[1], Akash Kumar[2] and Bharadwaj Veeravalli[1]
[1]National University of Singapore, SG; [2]Technische Universität Dresden, DE

1530 **LIFETIME-AWARE LOAD DISTRIBUTION POLICIES IN MULTI-CORE SYSTEMS: AN IN-DEPTH ANALYSIS**
Speaker: Antonio Miele, Politecnico di Milano, IT
Authors: Cristiana Bolchini, Luca Cassano and Antonio Miele Politecnico di Milano, IT

IPS **IP3-12**

1600 **COFFEE BREAK IN EXHIBITION AREA**

7.8 Presentations from IoT-Campus (II): IoT Survival Guide and Big Data Challenges

Exhibition Theatre 1430 - 1600

Exhibition Theatre session: see Exhibition Theatre Programme for details.

IP3 Interactive Presentations

Conference Level, Foyer 1600 - 1630

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. Moreover, one "Best Interactive Presentation Award" will be given.

IP3-1 A FLEXIBLE INEXACT TMR TECHNIQUE FOR SRAM-BASED FPGAS

Speaker: Akash Kumar, Technische Universität Dresden, DE
Authors: Shyamsundar Venkataraman[1], Rui Santos[1] and Akash Kumar[2]
[1]National University of Singapore, SG; [2]Technische Universität Dresden, DE

IP3-2 ACCURATE VERIFICATION OF RC POWER GRIDS

Speaker: Mohammad Fawaz, University of Toronto, CA
Authors: Mohammad Fawaz and Farid N. Najm, University of Toronto, CA

IP3-3 SECURITY ANALYSIS OF CYBER-PHYSICAL SYSTEMS ILLUSTRATED WITH AUTOMOTIVE CASE STUDY

Speaker: Viacheslav Izosimov, KTH Royal Institute of Technology, SE
Authors: Viacheslav Izosimov[1], Alexandros Asvestopoulos[2], Oscar Blomkvist[2] and Martin Törngren[3]
[1]Semcon, SE; [2]Scania CV, SE; [3]KTH Royal Institute of Technology, SE

IP3-4 ONLINE HEURISTIC FOR THE MULTI-OBJECTIVE GENERALIZED TRAVELING SALESMAN PROBLEM

Speaker: Joost van Pinxten, Eindhoven University of Technology, NL
Authors: Joost van Pinxten[1], Marc Geilen[1], Twan Basten[1], Umar Waqas[1] and Lou Somers[2]
[1]Eindhoven University of Technology, NL; [2]Océ Technologies, NL

IP3-5 TOWARDS LOW OVERHEAD CONTROL FLOW CHECKING USING REGULAR STRUCTURED CONTROL

Speaker: Zhiqi Zhu, The University of Texas at Dallas, US
Authors: Zhiqi Zhu and Joseph Callenes-Sloan, The University of Texas at Dallas, US

IP3-6 EMULATION-BASED HIERARCHICAL FAULT-INJECTION FRAMEWORK FOR COARSE-TO-FINE VULNERABILITY ANALYSIS OF HARDWARE-ACCELERATED APPROXIMATE ALGORITHMS

Speaker: Theocharis Theocharides, University of Cyprus, CY
Authors: Ioannis Chadjiminas, Ioannis Savva, Christos Kyrkou, Maria K. Michael and Theocharis Theocharides, University of Cyprus, CY

IP3-7 TECHNOLOGY TRANSFER IN COMPUTING SYSTEMS: THE TETRACOM APPROACH

Speaker: Rainer Leupers, RWTH Aachen University, DE
Author: Rainer Leupers, RWTH Aachen University, DE

IP3-8 ENERGY VS. RELIABILITY TRADE-OFFS EXPLORATION IN BIOMEDICAL ULTRA-LOW POWER DEVICES

Speaker: Loris Duch, École Polytechnique Fédérale de Lausanne (EPFL), CH
Authors: Loris Duch, Pablo Garcia del Valle, David Atienza, Shrikanth Ganapathy and Andreas Burg, École Polytechnique Fédérale de Lausanne (EPFL), CH

IP3-9 A MACHINE LEARNING APPROACH FOR MEDICATION ADHERENCE MONITORING USING BODY-WORN SENSORS

Speaker: Hassan Ghasemzadeh, Washington State University, US
Authors: Niloofar Hezar Jaribi, Ramin Fallahzadeh and Hassan Ghasemzadeh Washington State University, US

IP3-10 REQUIREMENTS-CENTRIC CLOSED-LOOP VALIDATION OF IMPLANTABLE CARDIAC DEVICES

Speaker: Partha Roop, The University of Auckland, NZ
Authors: Weiwei Ai, Nitish Patel and Partha Roop, The University of Auckland, NZ

IP3-11 LOW NORMALIZED ENERGY DERIVATION ASYNCHRONOUS CIRCUIT SYNTHESIS FLOW THROUGH FORK-JOIN SLACK MATCHING FOR CRYPTOGRAPHIC APPLICATIONS

Speaker: Nan Liu, Nanyang Technological University, SG
Authors: Nan Liu, Kwen-Siong Chong, Weng-Geng Ho, Bah-Hwee Gwee and Joseph S. Chang, Nanyang Technological University, SG

IP3-12 A LIFETIME-AWARE RUNTIME MAPPING APPROACH FOR MANYCORE SYSTEMS IN THE DARK SILICON ERA

Speaker: Mohammad-Hashem Haghbayan, University of Turku, FI
Authors: Mohammad-Hashem Haghbayan[1], Antonio Miele[2], Amir-Mohammad Rahmani[3], Pasi Liljeberg[1] and Hannu Tenhunen[3]
[1]University of Turku, FI; [2]Politecnico di Milano, IT; [3]KTH Royal Institute of Technology and University of Turku, FI

8.1 SPECIAL DAY Hot Topic: Connectivity in the automotive domain: From micro to macro

Saal 2 1700 - 1830

Chair: **Henk Corporaal,** Eindhoven University of Technology, NL
Co-Chair: **Samarjit Chakraborty,** Technische Universität München (TUM), DE

The goal of this session is to discuss issues related to connectivity or communications at various scales in the automotive domain. On one hand we have in-vehicle connectivity issues like cabling, communication buses and their timing analysis, and on the other hand, vehicle-to-vehicle and vehicle-to-infrastructure communication issues are becoming increasingly important. What are the challenges, what are potential solutions, and what are emerging trends, will be discussed in this session

1700 AUTOMOTIVE V2X ON PHONES: ENABLING NEXT-GENERATION MOBILE ITS APPS

Speaker: Li-Shiuan Peh, Massachusetts Institute of Technology (MIT), US
Authors: Jason Gao and Li-Shiuan Peh, Massachusetts Institute of Technology (MIT), US

1730 EDA FOR AUTOMOTIVE CABLING

Speaker: Thomas Heurung, Mentor, DE
Author: Thomas Heurung, Mentor, DE

1800 DETERMINISTIC ETHERNET IN AUTOMOTIVE APPLICATIONS

Speaker: Astrit Ademaj, TTTech Computertechnik AG, AT
Author: Astrit Ademaj, TTTech Computertechnik AG, AT

8.2 EU Projects Special Session: Towards better EU-projects - Success Stories

Konferenz 6 1700 - 1830

Organiser: **Roberto Giorgi,** University of Siena, IT
Chair: **Cristina Silvano,** Politecnico of Milan, IT
Co-Chair: **Roberto Giorgi,** University of Siena, IT

From lessons learned to best practices and correct scientific methodologies; In this session several cases are considered showing successful strategies to solve research and industry problems in a European dimension.

1700 COLLECTIVE KNOWLEDGE: TOWARDS R&D SUSTAINABILITY

Speaker: Anton Lokhmotov, dividiti, GB
Authors: Grigori Fursin[1], Anton Lokhmotov[1] and Ed Plowman[2]
[1]dividiti, GB; [2]ARM, GB

1715 LESSONS LEARNED FROM THE EU PROJECT T-CREST

Speaker: Martin Schoeberl, Technical University of Denmark, DK
Author: Martin Schoeberl, Technical University of Denmark, DK

1730 MULTIPOS: MARIE CURIE NETWORK IN MULTI-TECHNOLOGY POSITIONING

Speaker: Jari Nurmi, Tampere University of Technology, FI
Authors: Jari Nurmi and Elena-Simona Lohan, Tampere University of Technology, FI

1745 **PROGRAM TRANSFORMATIONS IN THE POLCA PROJECT**
Speaker: Jan Kuper, University of Twente, NL
Authors: Jan Kuper[1], Lutz Schubert[2], Kilian Kempf[3], Colin Glass[4], Daniel Rubio Bonilla[4] and Manuel Carro[5]
[1]University of Twente, NL; [2]University of Ulm, DE; [3]Ulm University, DE; [4]High Performance Computing Centre Stuttgart, DE; [5]Imdea Software Institute Madrid, ES

1800 **COMPUTATION AND COMMUNICATION CHALLENGES TO DEPLOY ROBOTS IN ASSISTED LIVING ENVIRONMENTS**
Speaker: Michael Hübner, Ruhr University Bochum, DE
Authors: Georgios Keramidas[1], Christos Antonopoulos[1], Nikolaos S. Voros[1], Fynn Schwiegelshohn[2], Philipp Wehner[2], Jens Rettkowski[2], Diana Göhringer[2], Michael Hübner[2], Stasinos Konstantopoulos[3], Theodore Giannakopoulos[4], Vangelis Karkaletsis[4] and Vaggelis Mariatos[5]
[1]Technological Educational Institute of Western Greece, GR; [2]Ruhr University Bochum, DE; [3]NCSR Demokritos, GR; [4]Institute of Informatics and Telecommunications, NCSR "Demokritos", GR; [5]AVN Innovative Technology Solutions, CY

1815 **ATHENIS 3D: AUTOMOTIVE TESTED HIGH-VOLTAGE AND EMBEDDED NON-VOLATILE INTEGRATED SOC PLATFORM WITH 3D TECHNOLOGY**
Speaker: Ewald Wachmann, ams AG, AT
Authors: Ewald Wachmann[1], Sergio Saponara[2], Cristian Zambelli[3], Pierre Tisserand[4], Jean Charbonnier[5], Tobias Erlbacher[6], Saeideh Gruenler[6], Christian Hartler[1], Joerg Siegert[1], Pierre Chassard[4], Dieu-My Ton[4], Lorenzo Ferrari[2] and Luca Fanucci[2]
[1]ams AG, AT; [2]University of Pisa, IT; [3]University of Ferrara, IT; [4]Valeo Electrical System, FR; [5]CEA-Leti, FR; [6]Fraunhofer IISB, DE

8.3 Hot Topic: Managing Heterogeneous Computing Resources at Runtime

Konferenz 1 1700 - 1830

Organisers: **Christian Plessl,** University of Paderborn, DE
David Andrews, University of Arkansas, US
Chair: **Daniel Ziener,** Hamburg University of Technology, DE
Co-Chair: **José L. Ayala,** Complutense University of Madrid, ES

Embedded systems have been using different, specialized computing resources for optimizing the performance, energy consumption and/or real-time constraints of critical application parts. In recent years, we could witness an increasing trend to heterogeneous computing ranging from embedded systems to high performance computing systems. Today, a wide variety of heterogeneous computing architectures are available as off-the-shelf components, such as, heterogeneous SoCs for embedded applications or PCIe-based accelerator cards with FPGAs, GPUs, or many-cores for HPC systems. Also, the programming models, languages and design environments for creating software or hardware configurations for the heterogeneous computing resources are also maturing and increasingly standardized, e.g., OpenCL, OpenACC, and OpenMP. In contrast, the software stack for effectively managing heterogeneous computing resources at runtime is however still largely undeveloped. Hence, the decision at what time and on which computing resource a particular function is executed is explicitly managed at the application level. The constrained view of the application makes it difficult to operate a system to meet global objectives, for example, mapping tasks to available heterogeneous resources such that the performance requirements of all applications are met while minimizing energy consumption. In this hot topic session we focus on run-time systems that strive for overcoming this application-centric view and enable an automated use of heterogeneous computing by dynamically mapping computations to different resources such that global goals are optimized.

1700 **RUN TIME INTERPRETATION FOR CREATING CUSTOM ACCELERATORS**
Speaker: David Andrews, University of Arkansas, US
Authors: Sen Ma, Zeyad Aklah and David Andrews, University of Arkansas, US

1730 **A SELF-ADAPTIVE APPROACH TO EFFICIENTLY MANAGE ENERGY AND PERFORMANCE IN TOMORROW'S HETEROGENEOUS COMPUTING SYSTEMS**
Speaker: Marco Domenico Santambrogio, Politecnico di Milano, IT
Authors: Ettore Trainiti, Gianluca Durelli, Antonio Miele, Cristiana Bolchini and Marco Domenico Santambrogio, Politecnico di Milano, IT

1800 **PERFORMANCE-CENTRIC SCHEDULING WITH TASK MIGRATION FOR A HETEROGENEOUS COMPUTE NODE IN THE DATA CENTER**
Speaker: Christian Plessl, Paderborn University, DE
Authors: Achim Lösch, Tobias Beisel, Tobias Kenter, Christian Plessl and Marco Platzner, Paderborn University, DE

8.4 Advanced Methods in High-Level Design

Konferenz 2 1700 - 1830

Chair: **Fabian Oboril,** KIT Germany, DE
Co-Chair: **Luciano Lavagno,** Politecnico di Torino, IT

Techniques such as machine learning, spiking neural networks, and probabilistic analysis are being adopted in advanced high-level design methods. This session presents a sampling of these topics, and concludes with a short IP presentation on a new approach to predicting reusable hardware.

1700 **ADAPTIVE THRESHOLD NON-PARETO ELIMINATION: RE-THINKING MACHINE LEARNING FOR SYSTEM LEVEL DESIGN SPACE EXPLORATION ON FPGAS**
Speaker: Pingfan Meng, University of California, San Diego, US
Authors: Pingfan Meng, Alric Althoff, Quentin Gautier and Ryan Kastner, University of California, San Diego, US

1730 **MONITORING OF MTL SPECIFICATIONS WITH IBM'S SPIKING-NEURON MODEL**
Speaker: Konstantin Selyunin, Vienna University of Technology, AT
Authors: Konstantin Selyunin[1], Thang Nguyen[2], Ezio Bartocci[1], Dejan Nickovic[3] and Radu Grosu[1]
[1]Vienna University of Technology, AT; [2]Infineon Technologies Austria AG, AT; [3]AIT Austrian Institute of Technology, AT

1800 **FORMAL PROBABILISTIC ANALYSIS OF DISTRIBUTED RESOURCE MANAGEMENT SCHEMES IN ON-CHIP SYSTEMS**
Speaker: Osman Hasan, School of Electrical Engineering and Computer Science (SEECS), NUST, PK
Authors: Shafaq Iqtedar[1], Osman Hasan[1], Muhammad Shafique[2] and Jörg Henkel[2]
[1]National University of Sciences and Technology (NUST), PK; [2]Karlsruhe Institute of Technology (KIT), DE

IPS **IP4-1**

8.5 Non-volatile Memory Design Methodologies

Konferenz 3 1700 - 1830

Chair: **Michael Huebner,** Ruhr University Bochum, DE
Co-Chair: **Michael Niemier,** University of Notre Dame, US

The first two papers consider hybrid main memories consisting of DRAM and emerging non-volatile memories, and examine system-level optimizations. The last paper considers performance in-memory computing using properties of emerging resistive RAM.

1700 **AN OPERATING SYSTEM LEVEL DATA MIGRATION SCHEME IN HYBRID DRAM-NVM MEMORY ARCHITECTURE**
Speaker: Reza Salkhordeh, Sharif University of Technology, IR
Authors: Reza Salkhordeh and Hossein Asadi, Sharif University of Technology, IR

1730 **UNIFIED DRAM AND NVM HYBRID BUFFER CACHE ARCHITECTURE FOR REDUCING JOURNALING OVERHEAD**
Speaker: Lei Ju, Shandong University, CN
Authors: Zhiyong Zhang, Lei Ju and Zhiping Jia, Shandong University, CN

1800 **FAST LOGIC SYNTHESIS FOR RRAM-BASED IN-MEMORY COMPUTING USING MAJORITY-INVERTER GRAPHS**
Speaker: Saeideh Shirinzadeh, University of Bremen, DE
Authors: Saeideh Shirinzadeh[1], Mathias Soeken[1], Pierre-Emmanuel Gaillardon[2] and Rolf Drechsler[3]
[1]University of Bremen, DE; [2]University of Utah, US; [3]University of Bremen and DFKI, DE

IPS **IP4-2**

8.6 Dataflow Modeling and Natural Language Processing

Konferenz 4 1700 - 1830

Chair: **Dominique Borrione,** Laboratoire TIMA, FR
Co-Chair: **Marc Geilen,** Eindhoven University of Technology, NL

The first two papers present advances in modeling parallelism and dynamism in dataflow applications. The third paper presents a novel method to extract verification properties from a natural language specification.

1700 **EXPLOITING RESOURCE-CONSTRAINED PARALLELISM IN HARD REAL-TIME STREAMING APPLICATIONS**
Speaker: Jelena Spasic, Leiden University, NL
Authors: Jelena Spasic, Di Liu and Todor Stefanov, Leiden University, NL

1730 **TRANSACTION PARAMETERIZED DATAFLOW: A MODEL FOR CONTEXT-DEPENDENT STREAMING APPLICATIONS**
Speaker: Xuan Khanh Do, CEA LIST, FR
Authors: Xuan Khanh Do[1], Stéphane Louise[1] and Albert Cohen[2]
[1]CEA LIST, FR; [2]Inria, FR

1800 **GLAST: LEARNING FORMAL GRAMMARS TO TRANSLATE NATURAL LANGUAGE SPECIFICATIONS INTO HARDWARE ASSERTIONS**
Speaker: Christopher Harris, University of California, Irvine, US
Authors: Christopher Harris and Ian Harris, University of California, Irvine, US

IPS **IP4-3**

8.7 Test Methods Handling Unkowns, 2.50 Integration and Realistic Memory Defects

Konferenz 5 1700 - 1830

Chair: **Friedrich Hapke,** Mentor Graphics Hamburg, DE

Improving the quality of the test and analysis process is crucial from a technical and economical point of view. Novel methods are presented to improve ATPG in the presence of unkowns, to allow pre-bond interposer testing and to exploit the memory infrastructure to improve defect coverage. The session is complemented by an ATPG approach based on behavioral fault models, a hierarchrchical DFT methodology, and a safety analysis process combining simulation-based fault injection with graph-based guidance.

1700 **ACCURATE CEGAR-BASED ATPG IN PRESENCE OF UNKNOWN VALUES FOR LARGE INDUSTRIAL DESIGNS**
Speaker: Karsten Scheibler, University of Freiburg, DE
Authors: Karsten Scheibler, Dominik Erb and Bernd Becker, University of Freiburg, DE

1730 **PRE-BOND TESTING OF THE SILICON INTERPOSER IN 2.5D ICS**
Speaker: Ran Wang, Duke University, US
Authors: Ran Wang[1], Zipeng Li[1], Sukeshwar Kannan[2] and Krishnendu Chakrabarty[1]
[1]Duke University, US; [2]Global Foundries Inc., US

1800 **IMPROVING SRAM TEST QUALITY BY LEVERAGING SELF-TIMED CIRCUITS**
Speaker: Josef Kinseher, Intel Mobile Communications, DE
Authors: Josef Kinseher[1], Leonardo B. Zordan[2], Ilia Polian[3] and Andreas Leininger[1]
[1]Intel Mobile Communications, DE; [2]Intel Mobile Communications, FR; [3]University of Passau, DE

IPS **IP4-4, IP4-6**

8.8 Model Based Design and Verification Day - Tutorial: An Industry Approach to FPGA/ARM System Development and Verification

Exhibition Theatre 1700 - 1830

Exhibition Theatre session: see Exhibition Theatre Programme for details.

DATE Party 1930 - 2300

see page 12

9.1 SPECIAL DAY Embedded Tutorial: Embedded Systems Security

Saal 2 0830 - 1000

Chair: **Matthias Schunter,** Intel, DE
Co-Chair: **Wieland Fischer,** Infineon Technologies, DE

HW designers need to understand SW attacks. SW designers need to understand the HW platform. In this first session of the special day on secure systems, we present an embedded tutorial on low-level software attacks. This is essential to understand the HW architecture modifications that are being made to make embedded HW/SW platforms more secure.

0830 SOFTWARE SECURITY: VULNERABILITIES AND COUNTERMEASURES FOR TWO ATTACKER MODELS
Speaker: Frank Piessens, Katholieke Universiteit Leuven, BE
Authors: Frank Piessens and Ingrid Verbauwhede, Katholieke Universiteit Leuven, BE

1000 COFFEE BREAK IN EXHIBITION AREA

9.2 Managing the Traffic Jam in NoC

Konferenz 6 0830 - 1000

Chair: **Nader Bagherzadeh,** University of California Irvine, US
Co-Chair: **Massoud Daneshtalab,** KTH, SE

Multi-core systems-on-chip integrate a growing number of heterogeneous components, leading to increasingly more complex traffic patterns. This section presents three contributions to manage the growing traffic challenges in NoCs: the first paper proposes a traffic splitting model for application-specific NosCs, the second presents a MCAPI-compliant hardware buffer manager to support communication among heterogeneous components, and the third employs an overlay network and scheduling unit to provide latency guarantees for hard real-time transmissions.

0830 OLITS: AN OHM'S LAW-LIKE TRAFFIC SPLITTING MODEL BASED ON CONGESTION PREDICTION
Speaker: Gaoming Du, Hefei University of Technology, CN
Authors: Gaoming Du[1], Yanghao Ou[1], Xiangyang Li[1], Ping Song[1], Zhonghai Lu[2] and Minglun Gao[1]
[1]Hefei University of Technology, CN; [2]KTH Royal Institute of Technology, SE

0900 MCAPI-COMPLIANT HARDWARE BUFFER MANAGER MECHANISM TO SUPPORT COMMUNICATION IN MULTI-CORE ARCHITECTURES
Speaker: Romain Lemaire, CEA-Leti, FR
Authors: Thiago Raupp da Rosa, Thomas Mesquida, Romain Lemaire and Fabien Clermidy, CEA-Leti, FR

0930 SLACK-BASED RESOURCE ARBITRATION FOR REAL-TIME NETWORKS-ON-CHIP
Speaker: Adam Kostrzewa, Technische Universität Braunschweig, DE
Authors: Adam Kostrzewa, Selma Saidi and Rolf Ernst, Technische Universität Braunschweig, DE

IPS IP4-7

1000 COFFEE BREAK IN EXHIBITION AREA

9.3 Industrial Experiences

Konferenz 1 0830 - 1000

Chair: **Norbert Wehn,** University of Kaiserslautern, DE
Co-Chair: **Shidhartha Das,** ARM, US

This session presents various inrustrial relevant experiences on automotive electronics, industrial automation, sensor fusions, energy efficient design, and reliability in advanced process nodes.

0830 CHALLENGES OF USING ON-CHIP PERFORMANCE MONITORS FOR PROCESS AND ENVIRONMENTAL VARIATION COMPENSATION
Speaker: Mahroo Zandrahimi, Delft University of Technology, NL
Authors: Mahroo Zandrahimi[1], Zaid Al-Ars[1], Philippe Debaud[2] and Armand Castillejo[2]
[1]Delft University of Technology, NL; [2]STMicroelectronics, FR

0845 STUDY OF WORKLOAD IMPACT ON BTI HCI INDUCED AGING OF DIGITAL CIRCUITS
Speaker: Ajith Sivadasan, ST Microelectronics and TIMA, FR
Authors: Ajith Sivadasan[1], Florian Cacho[2], Sidi-Ahmed Benhassain[1], Vincent Huard[2] and Lorena Anghel[3]
[1]ST Microelectronics and TIMA, FR; [2]STMicroelectronics, FR; [3]TIMA, FR

0900 FAST PROTOTYPING PLATFORM FOR NAVIGATION SYSTEMS WITH SENSORS FUSION
Speaker: Karim Ben Chehida, CEA LIST, FR
Authors: Charly Bechara[1], Karim Ben Chehida[1], Mickael Guibert[1], Renaud Schmit[1], Maria Lepecq[1], Laurent Soulier[1], Thomas Dombek[1] and Yann Leclerc[2]
[1]CEA LIST, FR; [2]M3Systems, FR

0915 PRECISION TIMED INDUSTRIAL AUTOMATION SYSTEMS
Speaker: Partha Roop, University of Auckland, NZ
Authors: Matthew Kuo, Sidharta Andalam and Partha Roop, University of Auckland, NZ

0930 AUTOSAR-BASED COMMUNICATION COPROCESSOR FOR AUTOMOTIVE ECUS
Speaker: Ahmed Hamed, Mentor Graphics Corporation, EG
Authors: Ahmed Hamed[1], Mona Safar[2], M. Watheq El-Kharashi[2] and Ashraf Salem[1]
[1]Mentor Graphics Corporation, EG; [2]Ain Shams University, EG

0945 MANTISSA-MASKING FOR ENERGY-EFFICIENT FLOATING-POINT LTE UPLINK MIMO BASEBAND PROCESSING
Speaker: Tomas Henriksson, Huawei Sweden, SE
Authors: Daniel Guenther[1], Tomas Henriksson[2], Rainer Leupers[1] and Gerd Ascheid[1]
[1]RWTH Aachen University, DE; [2]Huawei, Sweden, SE

1000 COFFEE BREAK IN EXHIBITION AREA

9.4 Optimization for Logic and Physical Design

Konferenz 2 0830 - 1000

Chair: **Valeria Bertacco,** Univ. of Michigan, US
Co-Chair: **Sven Peyer,** IBM, DE

The first paper proposes minimization techniques for Majority-Inverter Graphs. The second paper presents functional rectification taking into account placement information. The third paper combines slack matching gate sizing and repeater insertion to optimize leakage power in asynchronous circuits.

0830 OPTIMIZING MAJORITY-INVERTER GRAPHS WITH FUNCTIONAL HASHING
Speaker: Mathias Soeken, École Polytechnique Fédérale de Lausanne (EPFL), CH
Authors: Mathias Soeken[1], Pierre-Emmanuel Gaillardon[2], Luca Amaru[2] and Giovanni De Micheli[2]
[1]University of Bremen, DE; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH

0900 RESOURCE-AWARE FUNCTIONAL ECO PATCH GENERATION
Speaker: Iris Hui-Ru Jiang, National Chiao Tung University, TW
Authors: An-Che Cheng[1], Iris Hui-Ru Jiang[1] and Jing-Yang Jou[2]
[1]National Chiao Tung University, TW; [2]National Central University, TW

0930 SIMULTANEOUS SLACK MATCHING, GATE SIZING AND REPEATER INSERTION FOR ASYNCHRONOUS CIRCUITS
Speaker: Gang Wu, Iowa State University, US
Authors: Gang Wu and Chris Chu, Iowa State University, US

IPS **IP4-8, IP4-9, IP4-10**

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.5 Formal Bit Precise Reasoning

Konferenz 3 0830 - 1000

Chair: **Markus Wedler,** Synopsys GmbH, DE
Co-Chair: **Julien Schmaltz,** Eindhoven University of Technology, NL

The session presents advancements in formal reasoning at the bit-level. The first paper makes significant improvements to the verification of multipliers. The second and third papers show progress in the analysis of memory-locked errors and clock domain crossing. The session closes with two IP presentations about using software analyzers for hardware verification and generating word-level models from bit-level designs.

0830 **FORMAL VERIFICATION OF INTEGER MULTIPLIERS BY COMBINING GRÖBNER BASIS WITH LOGIC REDUCTION**
Speaker: Amr Sayed-Ahmed, University of Bremen, DE
Authors: Amr Sayed Ahmed[1], Daniel Grosse[1], Ulrich Kühne[1], Mathias Soeken[1] and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]University of Bremen and DFKI, DE

0900 **ROOT-CAUSE ANALYSIS FOR MEMORY-LOCKED ERRORS**
Speaker: John Adler, University of Toronto, CA
Authors: John Adler, Djordje Maksimovic and Andreas Veneris, University of Toronto, CA

0930 **FORMAL VERIFICATION OF CLOCK DOMAIN CROSSING USING GATE-LEVEL MODELS OF METASTABLE FLIP-FLOPS**
Speaker: Ghaith Tarawneh, Newcastle University, GB
Authors: Ghaith Tarawneh, Andrey Mokhov and Alex Yakovlev, Newcastle University, GB

IPS **IP4-11, IP4-12, IP4-13**

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.6 Real-Time Scheduling

Konferenz 4 0830 - 1000

Chair: **Frank Slomka,** Universität Ulm, DE
Co-Chair: **Kai Lampka,** Uppsala University, SE

The papers in this session introduce new scheduling algorithms and schedulability analyses for modern real-time systems, including systems with parallel and self-suspending tasks, and memory-constrained systems.

0830 **RESPONSE-TIME ANALYSIS OF DAG TASKS UNDER FIXED PRIORITY SCHEDULING WITH LIMITED PREEMPTIONS**
Speaker: Maria A. Serrano, Barcelona Supercomputing Center and Technical University of Catalonia, ES
Authors: Maria A. Serrano[1], Alessandra Melani[2], Marko Bertogna[3] and Eduardo Quinones[4]
[1]Barcelona Supercomputing Center and Technical University of Catalonia, ES; [2]Scuola Superiore Sant'Anna, IT; [3]University of Modena, IT; [4]Barcelona Supercomputing Center, ES

0900 **SPEED OPTIMIZATION FOR TASKS WITH TWO RESOURCES**
Speaker: Alessandra Melani, Scuola Superiore Sant'Anna, IT
Authors: Alessandra Melani[1], Renato Mancuso[2], Daniel Cullina[2], Marco Caccamo[2] and Lothar Thiele[3]
[1]Scuola Superiore Sant'Anna, IT; [2]University of Illinois at Urbana-Champaign, US; [3]Swiss Federal Institute of Technology (ETH), CH

0930 **SELF-SUSPENSION REAL-TIME TASKS UNDER FIXED-RELATIVE-DEADLINE FIXED-PRIORITY SCHEDULING**
Speaker: Wen-Hung Huang, TU Dortmund, DE
Authors: Wen-Hung Huang and Jian-Jia Chen, TU Dortmund, DE

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.7 Temperature Awareness in Computing Systems

Konferenz 5 0830 - 1000

Chair: **Muhammad Shafique,** Karlsruhe Institute of Technology (KIT), DE
Co-Chair: **Marina Zapater,** Complutense University of Madrid, ES

This session covers different hardware and software approaches for thermal optimization in computing systems, from hybrid memory cubes, pipelined real-time systems or multiprocessors.

0830 **THERMAL-AWARE DYNAMIC PAGE ALLOCATION POLICY BY FUTURE ACCESS PATTERNS FOR HYBRID MEMORY CUBE (HMC)**
Speaker: Wei Hen Lo, National Tsing Hua University, TW
Authors: Wei-Hen Lo, Kai-zen Liang and TingTing Hwang, National Tsing Hua University, TW

0900 **MINIMIZING PEAKTEMPERATURE FOR PIPELINED HARD REAL-TIME SYSTEMS**
Speaker: Long Cheng, Technische Universität München (TUM), DE
Authors: Long Cheng[1], Kai Huang[2], Gang Chen[1], Biao Hu[1] and Alois Knoll[1]
[1]Technische Universität München (TUM), DE; [2]Sun Yat-sen University, CN

0930 **THERMAL AWARE SCHEDULING AND MAPPING OF MULTIPHASE APPLICATIONS ONTO CHIP MULTIPROCESSOR**
Speaker: Aryabartta Sahu, IIT Guwahati, IN
Author: Aryabartta Sahu, IIT Guwahati, IN

IPS **IP4-14, IP4-15**

1000 **COFFEE BREAK IN EXHIBITION AREA**

9.8 Embedded Tutorial: Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis

Exhibition Theatre 0830 - 1000

Exhibition Theatre session: see Exhibition Theatre Programme for details.

IP4 Interactive Presentations

Conference Level, Foyer 1000 - 1030

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. Moreover, one "Best Interactive Presentation Award" will be given.

IP4-1 **A Q-GRAM BIRTHMARKING APPROACH TO PREDICTING REUSABLE HARDWARE**
Speaker: Kevin Zeng, Virginia Tech, US
Authors: Kevin Zeng and Peter Athanas, Virginia Tech, US

IP4-2 **CAPTOPRIL: REDUCING THE PRESSURE OF BIT FLIPS ON HOT LOCATIONS IN NON-VOLATILE MAIN MEMORIES**
Speaker: Majid Jalili, Sharif University of Technology, IR
Authors: Majid Jalili and Hamid Sarbazi-Azad, Sharif University of Technology, IR

IP4-3 **HANDLING COMPLEX DEPENDENCIES IN SYSTEM DESIGN**
Speaker: Mischa Möstl, Technische Universität Braunschweig, DE
Authors: Mischa Möstl and Rolf Ernst, Technische Universität Braunschweig, DE

IP4-4 **A SYNTHESIS-AGNOSTIC BEHAVIORAL FAULT MODEL FOR HIGH GATE-LEVEL FAULT COVERAGE**
Speaker: Anton Karputkin, Tallinn University of Technology, EE
Authors: Anton Karputkin and Jaan Raik
Tallinn University of Technology, EE

IP4-6 **COMBINING GRAPH-BASED GUIDANCE AND ERROR EFFECT SIMULATION FOR EFFICIENT SAFETY ANALYSIS**
Speaker: Jo Laufenberg, Universität Tübingen, DE
Authors: Jo Laufenberg[1], Sebastian Reiter[2], Alexander Viehl[2], Thomas Kropf[1], Wolfgang Rosenstiel[1] and Oliver Bringmann[1]
[1]Universität Tübingen, DE; [2]FZI Forschungszentrum Informatik, DE

IP4-7 **PACKET SECURITY WITH PATH SENSITIZATION FOR NOCS**
Speaker: Travis Boraten, Ohio University, US
Authors: Travis Boraten and Avinash Kodi, Ohio University, US

IP4-8 **SYNTHESIS OF APPROXIMATE CODERS FOR ON-CHIP INTERCONNECTS USING REVERSIBLE LOGIC**
Speaker: Robert Wille, Johannes Kepler University Linz, AT
Authors: Robert Wille[1], Oliver Keszocze[2], Stefan Hillmich[2], Marcel Walter[2] and Alberto Garcia-Ortiz[3]
[1]Johannes Kepler University Linz, AT; [2]University of Bremen, DE; [3]ITEM (U.Bremen), DE

IP4-9 **DESIGN-SYNTHESIS CO-OPTIMISATION USING SKEWED AND TAPERED GATES**
Speaker: Ankur Shukla, India Systems Development Lab, IBM India, IN
Authors: Ayan Datta[1], James D. Warnock[2], Ankur Shukla[1], Saurabh Gupta[1], Yiu Hing Chan[2], Karthik Mohan[1] and Charudhattan Nagarajan[1]
[1]India Systems Development Lab, IBM India, IN; [2]IBM US, US

IP4-10 **A SYNTHESIS-PARAMETER TUNING SYSTEM FOR AUTONOMOUS DESIGN-SPACE EXPLORATION**
Speaker: Matthew Ziegler, IBM T. J. Watson Research Center, US
Authors: Matthew Ziegler[1], Hung-Yi Liu[2], George Gristede[1], Bruce Owens[3], Ricardo Nigaglioni[3] and Luca Carloni[2]
[1]IBM T. J. Watson Research Center, US; [2]Columbia University, US; [3]IBM Systems and Technology Group, US

IP4-11 **UNBOUNDED SAFETY VERIFICATION FOR HARDWARE USING SOFTWARE ANALYZERS**
Speaker: Rajdeep Mukherjee, University of Oxford, GB
Authors: Rajdeep Mukherjee, Peter Schrammel, Daniel Kroening and Tom Melham, University of Oxford, GB

IP4-12 **VERILOG2SMV: A TOOL FOR WORD-LEVEL VERIFICATION**
Speaker: Ahmed Irfan, Fondazione Bruno Kessler and University of Trento, IT
Authors: Ahmed Irfan[1], Alessandro Cimatti[2], Alberto Griggio[2], Marco Roveri[2] and Roberto Sebastiani[3]
[1]Fondazione Bruno Kessler and University of Trento, IT; [2]Fondazione Bruno Kessler, IT; [3]University of Trento, IT

IP4-13 **TOWARDS FORMAL VERIFICATION OF REAL-WORLD SYSTEMC TLM PERIPHERAL MODELS - A CASE STUDY**
Speaker: Vladimir Herdt, University of Bremen, DE
Authors: Hoang M. Le[1], Vladimir Herdt[1], Daniel Grosse[1] and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]University of Bremen and DFKI, DE

IP4-14 **FREQUENCY SCHEDULING FOR RESILIENT CHIP MULTI-PROCESSORS OPERATING AT NEAR THRESHOLD VOLTAGE**
Speaker: Huawei Li, Chinese Academy of Sciences, CN
Authors: Ying Wang, Huawei Li and Xiaowei Li, Chinese Academy of Sciences, CN

IP4-15 **A LOW OVERHEAD ERROR CONFINEMENT METHOD BASED ON APPLICATION STATISTICAL CHARACTERISTICS**
Speaker: Anupam Chattopadhyay, Nanyang Technological University, SG
Authors: Zheng Wang[1], Georgios Karakonstantis[2] and Anupam Chattopadhyay[3]
[1]RWTH-Aachen University, DE; [2]Queen's University, GB; [3]Nanyang Technological University, SG

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

10.1 SPECIAL DAY Hot Topic: Lightweight Security for Embedded Processors

Saal 2 1100 - 1230

Chair: **Tilo Müller,** Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Co-Chair: **Patrick Schaumont,** Virginia Tech, US

Past research has shown that SW-only solutions cannot provide guarantee about SW security. A minimum HW root of trust is required. In embedded context, the research challenge is to find and demonstrate the 'minimum' root-of-trust. The first two papers search for this minimum requirements: "Scaling Down: Lightweight Approaches to IoT Security" and "SOFIA: Software and Control Flow Integrity Architecture." The third paper addresses the fundamental question on how to build and verify trust in embedded devices.

1100 **SCALING DOWN: LIGHTWEIGHT APPROACHES TO IOT SECURITY**
Speaker: Patrick Koeberl, Intel Labs, DE
Author: Patrick Koeberl, Intel Labs, DE

1130 **SOFIA: SOFTWARE AND CONTROL FLOW INTEGRITY ARCHITECTURE**
Speaker: Ruan de Clercq, Katholieke Universiteit Leuven, BE
Authors: Ruan de Clercq[1], Ronald De Keulenaer[2], Bart Coppens[2], Bohan Yang[1], Pieter Maene[1], Koen De Bosschere[2], Bart Preneel[1], Bjorn De Sutter[2] and Ingrid Verbauwhede[1]
[1]Katholieke Universiteit Leuven, BE; [2]Ghent University, BE

1200 **TRUST, BUT VERIFY: WHY AND HOW TO ESTABLISH TRUST IN EMBEDDED DEVICES**
Speaker: Aurélien Francillon, EURECOM, FR
Author: Aurélien Francillon, EURECOM, FR

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

10.2 Does it Work or NoC?

Konferenz 6 1100 - 1230

Chair: **Davide Bertozzi,** University of Ferrara, IT
Co-Chair: **Kees Goossens,** Eindhoven University of Technology, NL

Reliable operation of NoCs is crucial for the correct operation of the complete system. Errors can occur at runtime coming from ill-defined clock domain crossing interfaces, partial design-time verification scenarios that did not cover all functional errors, and technology-scaling related sideffects that increase circuit's susceptibility to permanent and intermittent faults. The first paper addresses the implications of asynchronous clock domain crossing in virtual channel flow control. The second paper proposes a NoC architecture that enables the detection of functional bugs at runtime. The third paper employs dynamic link sharing for achieving fault tolerance 3D NoC designs.

1100 **CROSSOVER: CLOCK DOMAIN CROSSING UNDER VIRTUAL-CHANNEL FLOW CONTROL**
Speaker: Anastasios Psarras, Democritus University of Thrace, GR
Authors: Michalis Paschou[1], Anastasios Psarras[1], Chrysostomos Nicopoulos[2] and Giorgos Dimitrakopoulos[1]
[1]Democritus University of Thrace, GR; [2]University of Cyprus, CY

1130 **CORRECT RUNTIME OPERATION FOR NOCS THROUGH ADAPTIVE REGION PROTECTION**
Speaker: Rawan Abdel-Khalek, University of Michigan, US
Authors: Rawan Abdel-Khalek and Valeria Bertacco, University of Michigan, US

1200 **FAULT-TOLERANT 3-D NETWORK-ON-CHIP DESIGN USING DYNAMIC LINK SHARING**
Speaker: Mehdi Modarressi, University of Tehran, IR
Authors: Seyyed Hossein Seyyedaghaei Rezaei[1], Mehdi Modarressi[1], Reza Yazdani[1] and Masoud Daneshtalab[2]
[1]University of Tehran, IR; [2]KTH Royal Institute of Technology, SE

IPS **IP5-1, IP5-2**

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

10.3 Design Experiences for Multimedia and Communication Applications

Konferenz 1 1100 - 1230

Chair: **Theocharis Theocharides,** University of Cyprus, CY
Co-Chair: **Steffen Paul,** University Bremen, DE

This session presents new design experiences for multimedia and communication applications. The first presentation demonstrates the feasibility having a heterogeneous system for speeding-up computation-intensive algorithms at an ultra-low-power sub-10 mW budget. Two contributions provide new ideas on approximate computing and its application in real design cases. Novel architectures related to channel decoding are presented in two papers. One paper demonstrates the feasibility of high-performance and high-quality depth and colour sensor fusion targeting mobile devices. The session also includes an approach for designing an integrated prototype for a portable telepresence robot.

1100 **ENABLING THE HETEROGENEOUS ACCELERATOR MODEL ON ULTRA-LOW POWER MICROCONTROLLER PLATFORMS**
Speaker: Francesco Conti, Università di Bologna, IT
Authors: Francesco Conti[1], Daniele Palossi[2], Andrea Marongiu[1], Davide Rossi[1] and Luca Benini[1]
[1]Università di Bologna, IT; [2]ETH Zurich, CH

1130 **THERMAL OPTIMIZATION USING ADAPTIVE APPROXIMATE COMPUTING FOR VIDEO CODING**
Speaker: Muhammad Shafique, Karlsruhe Institute of Technology (KIT), DE
Authors: Daniel Palomino[1], Muhammad Shafique[2], Altamiro Susin[1] and Jörg Henkel[2]
[1]Universidade Federal do Rio Grande do Sul (UFRGS), BR; [2]Karlsruhe Institute of Technology (KIT), DE

1200 **HIGH PERFORMANCE TIME-OF-FLIGHT AND COLOR SENSOR FUSION WITH IMAGE-GUIDED DEPTH SUPER RESOLUTION**
Speaker: Hannes Plank, Infineon Technologies Austria AG, AT
Authors: Hannes Plank, Gerald Holweg, Thomas Herndl and Norbert Druml, Infineon Technologies Austria AG, AT

1215 **SATURATED MIN-SUM DECODING: AN "AFTERBURNER" FOR LDPC DECODER HARDWARE**
Speaker: Stefan Scholl, University of Kaiserslautern, DE
Authors: Stefan Scholl, Philipp Schläfer and Norbert Wehn, University of Kaiserslautern, DE

IPS **IP5-3, IP5-4, IP5-5**

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

10.4 Stochastic Methods for Circuit Analysis & Synthesis

Konferenz 2 1100 - 1230

Chair: **Michal Rewienski,** Technical University of Gdansk, PL
Co-Chair: **L. Miguel Silveira,** INESC-ID, IST, U Lisboa, PT

Stochastic methods are continuing to play a fundamental role in circuit analysis and synthesis in order to handle both the growing complexity of integrated circuits as well as the effects of process variations. The first paper combines a Markov Chain Monte Carlo method with a Floating Random Walk method in order to speed up capacitance extraction and handle circuits containing IP protected substructures. The second paper builds a parameterized surrogate model of node voltages in power grids which can be used for efficient evaluation of multiple variation settings. The third paper uses an iterative variation-aware circuit synthesis flow to improve performance and energy efficiency.

1100 **UTILIZING MACROMODELS IN FLOATING RANDOM WALK BASED CAPACITANCE EXTRACTION**
Speaker: Wenjian Yu, Tsinghua University, CN
Authors: Wenjian Yu[1], Bolong Zhang[1], Chao Zhang[1], Haiquan Wang[1] and Luca Daniel[2]
[1]Tsinghua University, CN; [2]Massachusetts Institute of Technology (MIT), US

1130 **VARIABILITY AND STATISTICAL ANALYSIS FLOW FOR DYNAMIC LINEAR SYSTEMS WITH LARGE NUMBER OF INPUTS**
Speaker: L. Miguel Silveira, INESC-ID, Instituto Superior Técnico, PT
Authors: António Lucas Martins[1], Jorge Fernandez Villena[2] and L. Miguel Silveira[1]
[1]INESC-ID, Instituto Superior Técnico, PT; [2]Cadence Design Systems, DE

1200 **VARIATION-AWARE NEAR THRESHOLD CIRCUIT SYNTHESIS**
Speaker: Mohammad Saber Golanbari, Karlsruhe Institute of Technology (KIT), DE
Authors: Mohammad Saber Golanbari, Saman Kiamehr, Mojtaba Ebrahimi and Mehdi Tahoori, Karlsruhe Institute of Technology (KIT), DE

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

10.5 Enhancing Memory in Next-Generation Platforms

Konferenz 3 1100 - 1230

Chair: **Fancisco Cazorla,** Barcelona Supercomputing Center, ES
Co-Chair: **Jeronimo Castrillon,** Technische Universität Dresden, DE

This session presents three interesting paper describing different approaches for enhancing the memory for obtaining significant performance and energy improvement with respect to standard processor-centric architectures. The first paper introduces a Near-Data Processing solution compatible with existing processor memory interfaces such as DDR3/4 with minimal changes. The second paper introduces the HIVE architecture, which allows performing common vector operations directly inside the HMC, avoiding contention on the interconnections as well as cache pollution. The third paper proposes a minimalistic clustered flash array which exposes a simple, stable, error-free, shared-memory flash interface that enables a flexible cross-layer flash management optimizations and a scalable distributed storage coordination.

1100 **BUFFERED COMPARES: EXCAVATING THE HIDDEN PARALLELISM INSIDE DRAM ARCHITECTURES WITH LIGHTWEIGHT LOGIC**
Speaker: Kiyoung Choi, Seoul National University, KR
Authors: Jinho Lee, Jung Ho Ahn and Kiyoung Choi, Seoul National University, KR

1130 **LARGE VECTOR OPERATIONS INSIDE HMC**
Speaker: Luigi Carro, Universidade Federal do Rio Grande do Sul (UFRGS), BR
Authors: Marco Antonio Zanata Alves, Matthias Diener, Paulo Santos and Luigi Carro, Universidade Federal do Rio Grande do Sul (UFRGS), BR

1200 **MINFLASH: A MINIMALISTIC CLUSTERED FLASH ARRAY**
Speaker: Ming Liu, Massachusetts Institute of Technology (MIT), US
Authors: Ming Liu[1], Sang-Woo Jun[1], Sungjin Lee[1], Jamey Hicks[2] and Arvind[1]
[1]Massachusetts Institute of Technology (MIT), US; [2]Quanta Research Cambridge, US

IPS **IP5-6**

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

10.6 Compilers and Tools for GPUs and MPSoCs

Konferenz 4 1100 - 1230

Chair: **Frank Hannig,** Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Co-Chair: **Lars Bauer,** Karlsruhe Institute of Technology, DE

This session covers compiler optimisations and tools for efficient execution on GPUs and MPSoCs. The first paper presents a lightweight OpenMP implementation for parallel accelerators. The next two papers in this session focus on GPU performance modelling and tuning. The final paper leverages approximation to improve the throughput of OpenCL programs on FPGAs. In addition, an interactive presentation deals with Matlab to ASIP compilation.

1100 **AN OPTIMIZED TASK-BASED RUNTIME SYSTEM FOR RESOURCE-CONSTRAINED PARALLEL ACCELERATORS**
Speaker: Daniele Cesarini, Università di Bologna, IT
Authors: Daniele Cesarini, Andrea Marongiu and Luca Benini, Università di Bologna, IT

1130 **A FINE-GRAINED PERFORMANCE MODEL FOR GPU ARCHITECTURES**
Speaker: Federico Busato, University of Verona, IT
Authors: Nicola Bombieri, Federico Busato and Franco Fummi, University of Verona, IT

1200 **CRITICAL POINTS BASED REGISTER-CONCURRENCY AUTOTUNING FOR GPUS**
Speaker: Ang Li, Eindhoven University of Technology, NL
Authors: Ang Li[1], Shuaiwen Leon Song[2], Akash Kumar[3], Eddy Z. Zhang[4], Daniel Chavarria[2] and Henk Corporaal[1]
[1]Eindhoven University of Technology, NL; [2]Pacific Northwest National Lab, US; [3]Technische Universität Dresden, DE; [4]Rutgers University, US

1215 **GRATER: AN APPROXIMATION WORKFLOW FOR EXPLOITING DATA-LEVEL PARALLELISM IN FPGA ACCELERATION**
Speaker: Abbas Rahimi, UC Berkeley, US
Authors: Atieh Lotfi[1], Abbas Rahimi[2], Amir Yazdanbakhsh[3], Hadi Esmaeilzadeh[3] and Rajesh Gupta[1]
[1]UC San Diego, US; [2]UC Berkeley, US; [3]Georgia Institute of Technology, US

IPS **IP5-7**

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

10.7 Reliable System Design

Konferenz 5 1100 - 1230

Chair: **Mohamed Sabry Aly,** Stanford University, US
Co-Chair: **Semeen Rehman,** Karlsruhe Institute of Technology (KIT), DE

This session explores several approaches for the analysis, simulation, and repair of integrated systems, from 3D ICs, to STT-RAMs.

1100 **A HOLISTIC TRI-REGION MLC STT-RAM DESIGN WITH COMBINED PERFORMANCE, ENERGY, AND RELIABILITY OPTIMIZATIONS**
Speaker: Yiran Chen, University of Pittsburgh, US
Authors: Wujie Wen[1], Mengjie Mao[2], Hai Li[2], Yiran Chen[2], Yukui Pei[3] and Ning Ge[3]
[1]Florida International University, US; [2]University of Pittsburgh, US; [3]Tsinghua University, CN

1130 **THERMAL-AWARE TSV REPAIR FOR ELECTROMIGRATION IN 3D ICS**
Speaker: Shengcheng Wang, Karlsruhe Institute of Technology (KIT), DE
Authors: Shengcheng Wang[1], Krishnendu Chakrabarty[2] and Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]Duke University, US

1200 **ELECTROTHERMAL SIMULATION OF BONDING WIRE DEGRADATION UNDER UNCERTAIN GEOMETRIES**
Speaker: Thorben Casper, Technische Universität Darmstadt, DE
Authors: Thorben Casper[1], Herbert De Gersem[1], Renaud Gillon[2], Tomas Gotthans[3], Tomáš Kratochvíl[3], Peter Meuris[4] and Sebastian Schöps[1]
[1]Technische Universität Darmstadt, DE; [2]ON Semiconductor, BE; [3]Brno University of Technology, CZ; [4]Magwel NV, Leuven, BE

IPS **IP5-8**

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

10.8 Presentations from Campus 3D-IC Integration: Opportunities for SMEs and Outlook 2020+

Exhibition Theatre 1100 - 1230

Exhibition Theatre session: see Exhibition Theatre Programme for details.

11.0 LUNCH TIME KEYNOTE SESSION

Saal 2 1330 - 1400

Chair: **Luca Fanucci,** University of Pisa, IT
Co-Chair: **Matthias Schunter,** Intel Corporation, DE

The lunch keynote presentation will be given by Dr. Rhines, recent 2015 recipient of the Phil Kaufman award. He will present a vision on design for security from EDA perspective.

1330 **SECURE SILICON: ENABLER FOR THE INTERNET OF THINGS**
Speaker: Walden C. Rhines, Mentor, US
Author: Walden C. Rhines, Mentor, US

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.1 SPECIAL DAY Hot Topic: Embedded Security Applications

Saal 2 1400 - 1530

Chair: **Tim Güneysu,** University of Bremen, DE
Co-Chair: **X. Sharon Hu,** University of Notre Dame, US

Embedded security devices end up in a wide range of applications. In this third session of the special day on secure systems, three industrial application fields are selected to illustrate the need for security and trust. The first application area is the one of smart grid and smart electricity distribution. The second application area is taken from Industry4.0, the goal of which is to develop the next generation smart factory. Automotive is a third exemplary field for which ICT security is essential: from the entertainment system to the SW controlling the engine or brakes.

1400 **SMART GRID SECURITY**
Speaker: Klaus Kursawe, European Network for Cyber Security, NL
Author: Klaus Kursawe, European Network for Cyber Security, NL

1430 **SECURITY IN INDUSTRIE 4.0 - CHALLENGES AND SOLUTIONS FOR THE FOURTH INDUSTRIAL REVOLUTION**
Speaker: Michael Waidner, Fraunhofer SIT, DE
Authors: Michael Waidner[1] and Michael Kasper[2]
[1]Technische Universität Darmstadt and Fraunhofer SIT, DE; [2]Fraunhofer SIT, DE

1500 **SECURITY FOR AUTOMOTIVE AND THE INTERNET OF THINGS**
Speaker: Hans Löhr, Robert Bosch GmbH, DE
Authors: Paul Duplys, Hans Löhr, Herve Seudie and Robert Szerwinski, Robert Bosch GmbH, DE

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.2 Beating New Technology Paths for NoC

Konferenz 6 1400 - 1530

Chair: **Partha Pande,** WSU, US
Co-Chair: **Sébastien Le Beux,** Le Beux, FR

Silicon photonics and wireless links are among the most interesting emerging technologies for on-chip communication. The first paper of this section presents a comprehensive approach for floorplanning a silicon-photonic NoC that accounts for cross-layer effects spanning the optical and electrical boundaries. The second and third papers propose new solutions for power and energy management of wireless NoCs.

1400 **CROSS-LAYER FLOORPLAN OPTIMIZATION FOR SILICON PHOTONIC NOCS IN MANY-CORE SYSTEMS**
Speaker: Andrew B. Kahng, University of California, San Diego, US
Authors: Ayse Coskun[1], Anjun Gu[2], Warren Jin[3], Ajay Jayant Joshi[1], Andrew B. Kahng[2], Jonathan Klamkin[3], Yenai Ma[1], John Recchio[2], Vaishnav Srinivas[2] and Tiansheng Zhang[1]
[1]Boston University, US; [2]University of California, San Diego, US; [3]UC Santa Barbara, US

1430 **ADAPTIVE MULTI-VOLTAGE SCALING IN WIRELESS NOC FOR HIGH PERFORMANCE LOW POWER APPLICATIONS**
Speaker: Sujay Deb, IIIT Delhi, IN
Authors: Hemanta Kumar Mondal, Sri Harsha Gade, Raghav Kishore and Sujay Deb, IIIT Delhi, IN

1500 **ENERGY EFFICIENT TRANSCEIVER IN WIRELESS NETWORK ON CHIP ARCHITECTURES**
Speaker: Salvatore Monteleone, University of Catania, IT
Authors: Vincenzo Catania[1], Andrea Mineo[1], Salvatore Monteleone[1], Maurizio Palesi[2] and Davide Patti[1]
[1]University of Catania, IT; [2]Kore University, IT

IPS **IP5-9**

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.3 Microarchitectures and Workload Allocation for Energy Efficiency

Konferenz 1 1400 - 1530

Chair: **Andrea Bartolini,** Univ. of Bologna, IT
Co-Chair: **Andreas Burg,** École Polytechnique Fédérale de Lausanne (EPFL), CH

The session discusses novel power modeling, workload allocation, and micro-architectural techniques for improving energy efficiency in data centers and processors

1400 **RESISTIVE CONFIGURABLE ASSOCIATIVE MEMORY FOR APPROXIMATE COMPUTING**
Speaker: Abbas Rahimi, University of California, Berkeley, US
Authors: Mohsen Imani[1], Abbas Rahimi[2] and Tajana Rosing[3]
[1]UC San Diego, US; [2]University of California, Berkeley, US; [3]University of California, San Diego, US

1430 **EXPLOITING CPU-LOAD AND DATA CORRELATIONS IN MULTI-OBJECTIVE VM PLACEMENT FOR GEO-DISTRIBUTED DATA CENTERS**
Speaker: Ali Pahlevan, École Polytechnique Fédérale de Lausanne (EPFL), CH
Authors: Ali Pahlevan, Pablo Garcia del Valle and David Atienza, École Polytechnique Fédérale de Lausanne (EPFL), CH

1500 **ENERGY EFFICIENCY IN CLOUD-BASED MAPREDUCE APPLICATIONS THROUGH BETTER PERFORMANCE ESTIMATION**
Speaker: Seyed Morteza Nabavinejad, Sharif University of Technology, IR
Authors: Seyed Morteza Nabavinejad and Maziar Goudarzi, Sharif University of Technology, IR

1515 **UNSUPERVISED POWER MODELING OF CO-ALLOCATED WORKLOADS FOR ENERGY EFFICIENCY IN DATA CENTERS**
Speaker: Juan Carlos Salinas-Hilburg, Universidad Politécnica de Madrid, ES
Authors: Juan Carlos Salinas-Hilburg[1], Marina Zapater[2], José L. Risco-Martín[3], Jose Manuel Moya[1] and Jose L. Ayala[3]
[1]Universidad Politécnica de Madrid, ES; [2]CEI Campus Moncloa, UCM-UPM, ES; [3]Universidad Complutense de Madrid, ES

IPS **IP5-10, IP5-11**

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.4 Automating Test Generation, Assertions and Diagnosis

Konferenz 2 1400 - 1530

Chair: **Pablo Sanchez,** University of Cantabria, ES
Co-Chair: **Ronny Morad,** IBM, IL

The session presents methodologies for automatic test generation of memory controllers and arithmetic circuits. They are complemented with techniques that improve assertion simulation and post-silicon debugging. The interactive presentations will introduce new ideas about generating properties and tests.

1400 **AUTOMATED TEST GENERATION FOR DEBUGGING ARITHMETIC CIRCUITS**
Speaker: Prabhat Mishra, University of Florida, US
Authors: Farimah Farahmandi and Prabhat Mishra, University of Florida, US

1430 **MCXPLORE: AN AUTOMATED FRAMEWORK FOR VALIDATING MEMORY CONTROLLER DESIGNS**
Speaker: Mohamed Hassan, University of Waterloo, CA
Authors: Mohamed Hassan and Hiren Patel, University of Waterloo, CA

1500 **EAST: EFFICIENT ASSERTION SIMULATION TECHNIQUES**
Speaker: Ansuman Banerjee, Indian Statistical Institute, IN
Authors: Debjyoti Bhattacharjee, Soumi Chattopadhyay and Ansuman Banerjee, Indian Statistical Institute, IN

1515 **COMBINATIONAL TRACE SIGNAL SELECTION WITH IMPROVED STATE RESTORATION FOR POST-SILICON DEBUG**
Speaker: Bijan Alizadeh, University of Tehran, IR
Authors: Siamack Beig Mohammadi and Bijan Alizadeh, University of Tehran, IR

IPS **IP5-12, IP5-13**

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.5 Design of Efficient Microarchitectures

Konferenz 3 1400 - 1530

Chair: **Dionisios Pnevmatikatos,** Technical University of Crete, GR
Co-Chair: **Todd Austin,** University of Michigan, US

The microarchitecture session presents innovative ideas for the efficient design of computing components. The first paper presents a viable prediction technique to deactivate cache ways in order to save energy without compromising performance. The second paper proposes a micro-architectural extension for approximate computing that reduces bit-error-rate while providing the power benefits of extreme voltage scaling techniques. The third paper presents a faster and accurate version of logarithmic number unit (LNU) design and implementation using a co-transformation scheme.

1400 **PRACTICAL WAY HALTING BY SPECULATIVELY ACCESSING HALT TAGS**
Speaker: Daniel Moreau, Chalmers University of Technology, SE
Authors: Daniel Moreau[1], Alen Bardizbanyan[1], Magnus Själander[2], Dave Whalley[3] and Per Larsson-Edefors[1]
[1]Chalmers University of Technology, SE; [2]Uppsala University, SE; [3]Florida State University, US

1430 **LAZY PIPELINES: ENHANCING QUALITY IN APPROXIMATE COMPUTING**
Speaker: Georgios Tziantzioulis, Northwestern University, US
Authors: Georgios Tziantzioulis[1], Ali Murat Gok[1], S M Faisal[2], Nikos Hardavellas[1], Seda Ogrenci-Memik[1] and Srinivasan Parthasarathy[2]
[1]Northwestern University, US; [2]The Ohio State University, US

1500 **HIGH-EFFICIENCY LOGARITHMIC NUMBER UNIT DESIGN BASED ON AN IMPROVED CO-TRANSFORMATION SCHEME**
Speaker: Youri Popoff, ETH Zürich, CH
Authors: Youri Popoff, Florian Scheidegger, Michael Schaffner, Michael Gautschi, Frank K. Gürkaynak and Luca Benini, ETH Zürich, CH

IPS **IP5-14, IP5-15, IP5-16, IP5-17**

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.6 Applications of Reconfigurable Computing

Konferenz 4 1400 - 1530

Chair: **Alessandro Cilardo,** University of Naples Federico II, IT
Co-Chair: **Koen Bertels,** Delft University of Technology, NL

FPGAs and other reconfigurable architectures are becoming prolific as a platform for implementing a broad domain of applications. In this session, we have three papers and an interactive presentation focused on the design of computer vision, machine learning, and video processing on reconfigurable architectures.

1400 **EFFICIENT FPGA ACCELERATION OF CONVOLUTIONAL NEURAL NETWORKS USING LOGICAL-3D COMPUTE ARRAY**
Speaker: Atul Rahman, UNIST, KR
Authors: Atul Rahman[1], Jongeun Lee[1] and Kiyoung Choi[2]
[1]UNIST, KR; [2]Seoul National University, KR

1430 **ENERGY EFFICIENT VIDEO FUSION WITH HETEROGENEOUS CPU-FPGA DEVICES**
Speaker: Peng Sun, University of Bristol, GB
Authors: Peng Sun[1], Alin Achim[1], Ian Hasler[2], Paul Hill[1] and Jose Nunez-Yanez[1]
[1]University of Bristol, GB; [2]Qioptiq LTD, GB

1500 **HIGHLY EFFICIENT RECONFIGURABLE PARALLEL GRAPH CUTS FOR EMBEDDED VISION**
Speaker: Antonis Nikitakis, Technical University of Crete, GR
Authors: Antonis Nikitakis[1] and Ioannis Papaefstathiou[2]
[1]Technical University of Crete, GR; [2]Synelixis Solutions Ltd, GR

IPS **IP5-18, IP5-19, IP5-20**

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.7 Naked Analog Synthesis

Konferenz 5 1400 - 1530

Chair: **Árpád Árpád Bürmen,** University of Ljubljana, SI
Co-Chair: **Francisco Fernandez,** IMSE-CNM, ES

The first paper introduces exciting Boolean methods into analog layout design. The second paper shows how to boost circuit optimization by data mining. The third paper presents a cocktail of model-based and simulation-based optimization. Two IPs complete the session with parallelization and learning in synthesis.

1400 **PARETO FRONT ANALOG LAYOUT PLACEMENT USING SATISFIABILITY MODULO THEORIES**
Speaker: Sherif Saif, Electronics Research Institute, EG
Authors: Sherif Saif[1], Mohamed Dessouky[2], M. Watheq El-Kharashi[3], Hazem Abbas[4] and Salwa Nassar[1]
[1]Electronics Research Institute, EG; [2]Mentor Graphics Corporation, EG; [3]Faculty of Engineering, Ain Shams University, EG; [4]Faculty of Media Engineering & Technology, GUC, EG

1430 **EFFICIENT MULTIPLE STARTING POINT OPTIMIZATION FOR AUTOMATED ANALOG CIRCUIT OPTIMIZATION VIA RECYCLING SIMULATION DATA**
Speaker: Bo Peng, Fudan University, CN
Authors: Bo Peng, Fan Yang, Changhao Yan, Xuan Zeng and Dian Zhou, Fudan University, CN

1500 **POLYGP: IMPROVING GP-BASED ANALOG OPTIMIZATION THROUGH ACCURATE HIGH-ORDER MONOMIALS AND SEMIDEFINITE RELAXATION**
Speaker: Ye Wang, The University of Texas at Austin, US
Authors: Ye Wang, Michael Orshansky and Constantine Caramanis, The University of Texas at Austin, US

IPS **IP5-21, IP5-22**

1530 **COFFEE BREAK IN EXHIBITION AREA**

11.8 Launch of the Worldwide MEMS Design Contest

Exhibition Theatre 1400 - 1730

Exhibition Theatre session: see Exhibition Theatre Programme for details.

IP5 Interactive Presentations

Conference Level, Foyer 1530 - 1600

Interactive Presentations run simultaneously during a 30-minute slot. A poster associated to the IP paper is on display throughout the afternoon. Additionally, each IP paper is briefly introduced in a one-minute presentation in a corresponding regular session, prior to the actual Interactive Presentation. Moreover, one "Best Interactive Presentation Award" will be given.

IP5-1 **RELIABILITY AND PERFORMANCE TRADE-OFFS FOR 3D NOC-ENABLED MULTICORE CHIPS**
Speaker: Partha Pande, Washington State University, US
Authors: Sourav Das[1], Janardhan Rao Doppa[1], Partha Pande[1] and Krishnendu Chakrabarty[2]
[1]Washington State University, US; [2]Duke University, US

IP5-2 **MEMORY-ACCESS AWARE DVFS FOR NETWORK-ON-CHIP IN CMPS**
Speaker: Yuan Yao, KTH Royal Institute of Technology, SE
Authors: Yuan Yao and Zhonghai Lu, KTH Royal Institute of Technology, SE

IP5-3 **A DYNAMICALLY RECONFIGURABLE ECC DECODER ARCHITECTURE**
Speaker: Philippe Coussy, Universite Bretagne Sud / Lab-STICC, FR
Authors: Awais Sani[1], Philippe Coussy[2] and Cyrille Chavet[3]
[1]Universite de Bretagne-Sud, FR; [2]Universite de Bretagne-Sud / Lab-STICC, FR; [3]Lab-STICC / Université de Bretagne Sud, FR

IP5-4 **RESISTIVE BLOOM FILTERS: FROM APPROXIMATE MEMBERSHIP TO APPROXIMATE COMPUTING WITH BOUNDED ERRORS**
Speaker: Abbas Rahimi, University of California, Berkeley, US
Authors: Vahideh Akhlaghi[1], Abbas Rahimi[2] and Rajesh K. Gupta[1]
[1]University of California, San Diego, US; [2]University of California, Berkeley, US

IP5-5 **REAL-TIME SYSTEM-LEVEL IMPLEMENTATION OF A TELEPRESENCE ROBOT USING AN EMBEDDED GPU PLATFORM**
Speaker: Swathi Gurumani, Advanced Digital Sciences Center, SG
Authors: Muhammad Teguh Satria[1], Swathi Gurumani[1], Wang Zheng[2], Keng Peng Tee[2], Augustine Koh[1], Pan Yu[2], Kyle Rupnow[1] and Deming Chen[3]
[1]Advanced Digital Sciences Center, SG; [2]Institute for Infocomm Research, SG; [3]UIUC, US

IP5-6 **EXPLORING SPECIALIZED NEAR-MEMORY PROCESSING FOR DATA INTENSIVE OPERATIONS**
Speaker: Salessawi Ferede Yitbarek, University of Michigan, US
Authors: Salessawi Ferede Yitbarek[1], Tao Yang[2], Reetuparna Das[1] and Todd Austin[1]
[1]University of Michigan, US; [2]University of California, San Diego, US

IP5-7 **MATLAB TO C COMPILATION TARGETING APPLICATION SPECIFIC INSTRUCTION SET PROCESSORS**
Speaker: Ioannis Latifis, University of Peloponnese, GR
Authors: Ioannis Latifis[1], Karthick Parashar[2], Grigoris Dimitroulakos[1], Hans Cappelle[2], Christakis Lezos[1], Konstantinos Masselos[1] and Francky Catthoor[2]
[1]University of Peloponnese, GR; [2]Interuniversity Microelectronics Centre (IMEC), BE

IP5-8 SAMPLING-BASED BUFFER INSERTION FOR POST-SILICON YIELD IMPROVEMENT UNDER PROCESS VARIABILITY

Speaker: Grace Li Zhang, Technische Universität München (TUM), DE
Authors: Grace Li Zhang, Bing Li and Ulf Schlichtmann, Technische Universität München (TUM), DE

IP5-9 PRADA: COMBATING VOLTAGE NOISE IN THE NOC POWER SUPPLY THROUGH FLOW-CONTROL AND ROUTING ALGORITHMS

Speaker: Prabal Basu, Utah State University, US
Authors: Prabal Basu, Rajesh JayashankaraShridevi, Koushik Chakraborty and Sanghamitra Roy, Utah State University, US

IP5-10 A POWER-EFFICIENT 3-D ON-CHIP INTERCONNECT FOR MULTI-CORE ACCELERATORS WITH STACKED L2 CACHE

Speaker: Kyungsu Kang, Samsung, KR
Authors: Kyungsu Kang[1], Luca Benini[2], Giovanni De Micheli[3], Sangho Park[1] and Jong-Bae Lee[1]
[1]Samsung, KR; [2]Università di Bologna, IT; [3]École Polytechnique Fédérale de Lausanne (EPFL), CH

IP5-11 POWER-EFFICIENT LOAD-BALANCING ON HETEROGENEOUS COMPUTING PLATFORMS

Speaker: Muhammad Shafique, Karlsruhe Institute of Technology (KIT), DE
Authors: Muhammad Usman Karim Khan[1], Muhammad Shafique[1], Apratim Gupta[2], Thomas Schumann[2] and Jörg Henkel[1]
[1]Karlsruhe Institute of Technology (KIT), DE; [2]University of Applied Sciences, Darmstadt, DE

IP5-12 TOPAZ: MINING HIGH-LEVEL SAFETY PROPERTIES FROM LOGIC SIMULATION TRACES

Speaker: Fadi Kurdahi, University of California, Irvine, US
Authors: Ahmed Nassar[1], Fadi Kurdahi[1] and Salam Zantout[2]
[1]University of California, Irvine, US; [2]American University of Beirut, LB

IP5-13 EXPLOITING TRANSACTION LEVEL MODELS FOR OBSERVABILITY-AWARE POST-SILICON TEST GENERATION

Speaker: Prabhat Mishra, University of Florida, US
Authors: Farimah Farahmandi[1], Prabhat Mishra[1] and Sandip Ray[2]
[1]University of Florida, US; [2]Intel Corporation, US

IP5-14 SEERAD: A HIGH SPEED YET ENERGY-EFFICIENT ROUNDING-BASED APPROXIMATE DIVIDER

Speaker: Ali Afzali-Kusha, University of Tehran, IR
Authors: Reza Zendegani[1], Mehdi Kamal[1], Arash Fayyazi[1], Ali Afzali-Kusha[1], Saeed Safari[1] and Massoud Pedram[2]
[1]University of Tehran, IR; [2]University of Southern California, US

IP5-15 IMPROVING PERFORMANCE GUARANTEES IN WORMHOLE MESH NOC DESIGNS

Speaker: Milos Panic, Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES
Authors: Milos Panic[1], Carles Hernandez[2], Jaume Abella[2], Antoni Roca Perez[3], Eduardo Quinones[2] and Francisco Cazorla[4]
[1]Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES; [2]Barcelona Supercomputing Center, ES; [3]Universitat Politècnica de Catalunya, ES; [4]Barcelona Supercomputing Center and IIIA-CSIC, ES

IP5-16 A DATA LAYOUT TRANSFORMATION (DLT) ACCELERATOR: ARCHITECTURAL SUPPORT FOR DATA MOVEMENT OPTIMIZATION IN ACCELERATED-CENTRIC HETEROGENEOUS SYSTEMS

Speaker: Tung Hoang, University of Chicago, US
Authors: Tung Hoang, Amirali Shambayati and Andrew A. Chien, University of Chicago, US

IP5-17 OUESSANT: FLEXIBLE INTEGRATION OF DEDICATED COPROCESSORS IN SYSTEMS ON CHIP

Speaker: Pierre-Henri Horrein, Lab-STICC/Télécom Bretagne, FR
Authors: Pierre-Henri Horrein, Philip-Dylan Gleonec, Erwan Libessart, André Lalevée and Matthieu Arzel, Lab-STICC/Télécom Bretagne, FR

IP5-18 A NOVEL BACKGROUND SUBTRACTION SCHEME FOR IN-CAMERA ACCELERATION IN THERMAL IMAGERY

Speaker: Konstantinos Makantasis, Institute of Communication and Computer Systems, GR
Authors: Antonis Nikitakis[1], Ioannis Papaefstathiou[2], Konstantinos Makantasis[3] and Anastasios Doulamis[4]
[1]Technical University of Crete, GR; [2]Synelixis Solutions Ltd, GR; [3]Institute of Communication and Computer Systems, GR; [4]National Technical University of Athens, GR

IP5-19 RADIATION-HARDENED DSP CONFIGURATIONS FOR IMPLEMENTING ARITHMETIC FUNCTIONS ON FPGA

Speaker: Marcos Sanchez-Elez, Universidad Complutense de Madrid, ES
Authors: Marcos Sanchez-Elez, Inmaculada Pardines, Felipe Serrano and Hortensia Mecha, Universidad Complutense de Madrid, ES

IP5-20 CONFIGURATION PREFETCHING AND REUSE FOR PREEMPTIVE HARDWARE MULTITASKING ON PARTIALLY RECONFIGURABLE FPGAS

Speaker: Ann Gordon-Ross, University of Florida, US
Authors: Aurelio Morales-Villanueva, Rohit Kumar and Ann Gordon-Ross, University of Florida, US

IP5-21 ANALOG CIRCUIT TOPOLOGICAL FEATURE EXTRACTION WITH UNSUPERVISED LEARNING OF NEW SUB-STRUCTURES

Speaker: Alex Doboli, Stony Brook University, US
Authors: Hao Li, Fanshu Jiao and Alex Doboli, Stony Brook University, US

IP5-22 DESIGN AUTOMATION TASKS SCHEDULING FOR ENHANCED PARALLEL EXECUTION OF A STATE-OF-THE-ART LAYOUT-AWARE SIZING APPROACH

Speaker: Nuno Horta, Instituto de Telecomunicações/Instituto Superior Técnico, PT
Authors: David Neves, Ricardo Martins, Nuno Lourenço and Nuno Horta, Instituto de Telecomunicações/Instituto Superior Técnico, PT

12.1 SPECIAL DAY Hot Topic: Design Methods for Security and Trust

Saal 2 1600 - 1730

Chair: **Jean-Luc Danger,** Télécom ParisTech, FR
Co-Chair: **Ilia Polian,** Universität Passau, DE

The last session of the special day on secure systems focuses on novel technologies to support the previous HW and SW architecture modifications. The first paper provides a design method for the remote integrity checking of complex PCBs based on Physically Unclonable Functions (PUFs). The second paper focuses on metrics to quantify and measure actually hardware attack resistance. The last paper focuses on design methods to support instruction set extensions on embedded micro-controllers.

1600 A DESIGN METHOD FOR REMOTE INTEGRITY CHECKING OF COMPLEX PCBS

Speaker: Patrick Schaumont, Virginia Tech, US
Authors: Aydin Aysu, Shravya Gaddam, Harsha Mandadi, Carol Pinto, Luke Wegryn and Patrick Schaumont, Virginia Tech, US

1630 QUANTIFYING HARDWARE SECURITY USING JOINT INFORMATION FLOW ANALYSIS

Speaker: Ryan Kastner, University of California, San Diego, US
Authors: Ryan Kastner, Wei Hu and Alric Althoff, University of California, San Diego, US

1700 INSTRUCTION SET EXTENSIONS FOR SECURE APPLICATIONS

Speaker: Francesco Regazzoni, ALaRI, CH
Authors: Francesco Regazzoni[1] and Paolo Ienne[2]
[1]ALaRI, CH; [2]École Polytechnique Fédérale de Lausanne (EPFL), CH

12.2 Hot Topic: Exploiting New Transistor Technologies to Enhance Hardware Security (without PUFs!)

Konferenz 6 1600 - 1730

Organiser: **Michael Niemier,** University of Notre Dame, US
Chair: **Sri Parameswaran,** The University of New South Wales, AU

Like performance, power, and reliability, security is becoming a critical design consideration. As a representative example, hardware security threats in the integrated circuit (IC) supply chain, including hardware counterfeiting, IP piracy, and reverse engineering cost the US economy more than $200 billion annually. Problems are further exacerbated by the rapid growth in the "Internet of Things" (IoT). This session will highlight how emerging transistor technologies can enhance existing hardware security primitives, and also lead to new hardware security primitives. We begin by addressing security threats that are enabled by insecure hardware. A special emphasis will be placed on the need for standards to address hardware security across all aspects of the supply chain. We then highlight how emerging transistor technologies could impact encryption engines. We consider not only how new devices could lead to more sophisticated/robust encryption ciphers in resource constrained environments, but also how new devices may make said ciphers more resilient to attacks such as differential power analysis (DPA). We conclude with a discussion of how unique I-V characteristics offered by beyond CMOS transistors can enable new hardware security primitives that could facilitate IC supply chain protection, help prevent/stop sidechannel attacks, etc.. Presently, most emerging technologies being studied in the context of hardware security are related to designing physically unclonable functions (PUFs) and random number generators (RNGs). However, most PUF and RNG designs leverage larger device-to-device variations in emerging technologies. Ironically, said variations often represent shortcomings when viewed through the lens of an original device target - i.e., reliable digital logic or memory. In contrast, we will discuss emerging transistor technologies for hardware security related applications that are not RNGs or PUFs, and do not inherently rely on device variations as a means to an end. This session will provide important insight into the following questions: Can new devices lead to more efficient hardware primitives than CMOS in countering hardware attacks? What properties should an emerging technology-based hardware infrastructure provide to better support software level protection schemes? Can such properties be reliably demonstrated by a given device? This session is especially timely as the 2015 International Technology Roadmap for Semiconductors (ITRS) chapter on Emerging Research Devices (ERD) will include the first section on how new devices might be employed to enhance hardware security. As such, the time has come to engage the design automation community in this new and important research vector.

1600 MITIGATING HARDWARE THREATS TO ENABLE THE INTERNET OF SECURE THINGS

Speaker: Yaw Obeng, National Institute of Standards and Technology, US
Authors: Yaw Obeng[1], Colm Nolan[2] and David Brown[3]
[1]National Institute of Standards and Technology, US; [2]IBM, IE; [3]Intel Corporation, US

1630 LEVERAGE EMERGING TECHNOLOGIES FOR DPA-RESILIENT BLOCK CIPHER DESIGN

Speaker: Yier Jin, University of Central Florida, US
Authors: Yu Bi[1], Kaveh Shamsi[1], Jiann-Shiun Yuan[1], Francois-Xavier Standaert[2] and Yier Jin[1]
[1]University of Central Florida, US; [2]Université Catholique de Louvain, BE

1700 USING EMERGING TECHNOLOGIES FOR HARDWARE SECURITY BEYOND PUFS

Speaker: X. Sharon Hu, University of Notre Dame, US
Authors: An Chen[1], X. Sharon Hu[2], Yier Jin[3], Michael Niemier[2] and Xunzhao Yin[2]
[1]ITRS ERD working group chair, US; [2]University of Notre Dame, US; [3]University of Central Florida, US

12.3 System Support for Resilience and Robustness

Konferenz 1 1600 - 1730

Chair: **Oliver Bringmann,** University of Tuebingen, DE
Co-Chair: **Dirk Stroobandt,** Ghent University, BE

This session discusses a wide range of innovative techniques from instruction scheduling to mobile virtualization to characterize and improve system resilience and robustness.

1600 EFFECT OF LFSR SEEDING, SCRAMBLING AND FEEDBACK POLYNOMIAL ON STOCHASTIC COMPUTING ACCURACY

Speaker: Jason H. Anderson, University of Toronto, CA
Authors: Jason H. Anderson[1], Yuko Hara-Azumi[2] and Shigeru Yamashita[3]
[1]University of Toronto, CA; [2]Tokyo Institute of Technology, JP; [3]Ritsumeikan University, JP

1630 EFFICIENT PROGRAM TRACING AND MONITORING THROUGH POWER CONSUMPTION – WITH A LITTLE HELP FROM THE COMPILER

Speaker: Carlos Moreno, University of Waterloo, CA
Authors: Carlos Moreno, Sean Kauffman and Sebastian Fischmeister, University of Waterloo, CA

1700 FLIC: FAST, LIGHTWEIGHT CHECKPOINTING FOR MOBILE VIRTUALIZATION USING NVRAM

Speaker: Kan Zhong, Chongqing University, CN
Authors: Kan Zhong[1], Duo Liu[1], Liang Liang[1], Linbo Long[1], Yi Lin[1] and Zili Shao[2]
[1]Chongqing University, CN; [2]The Hong Kong Polytechnic University, HK

1715 PAIS: PARALLELIZATION AWARE INSTRUCTION SCHEDULING FOR IMPROVING SOFT-ERROR RELIABILITY OF GPU-BASED SYSTEMS

Speaker: Mohammad Abdullah Al Faruque, University of California, Irvine, US
Authors: Haeseung Lee, Hsinchung Chen and Mohammad Abdullah Al Faruque, University of California, Irvine, US

12.4 Simulating Everything: From Timing to Instructions

Konferenz 2 1600 - 1730

Chair: **Elena Ioana Vatajelu,** Politecnico di Torino, IT
Co-Chair: **Valeria Bertacco,** University of Michigan, US

The session deals with several facets of simulation optimization, ranging from timing, circuit, and instruction decoding.

1600 ACCELERATING SOURCE-LEVEL TIMING SIMULATION

Speaker: Oliver Bringmann, Universität Tübingen, DE
Authors: Simon Schulz[1] and Oliver Bringmann[2]
[1]Universität Tübingen, DE; [2]Universität Tübingen / FZI, DE

1630 SPARSITY-ORIENTED SPARSE SOLVER DESIGN FOR CIRCUIT SIMULATION

Speaker: Xiaoming Chen, Tsinghua University, CN
Authors: Xiaoming Chen, Lixue Xia, Yu Wang and Huazhong Yang, Tsinghua University, CN

1700 INTEGRATION OF MIXED-SIGNAL COMPONENTS INTO VIRTUAL PLATFORMS FOR HOLISTIC SIMULATION OF SMART SYSTEMS

Speaker: Davide Quaglia, University of Verona, IT
Authors: Enrico Fraccaroli[1], Michele Lora[1], Sara Vinco[2], Davide Quaglia[1] and Franco Fummi[1]
[1]University of Verona, IT; [2]Politecnico di Torino, IT

1715 DECISION TREE GENERATION FOR DECODING IRREGULAR INSTRUCTIONS

Speaker: Katsumi Okuda, Mitsubishi Electric Corporation, JP
Authors: Katsumi Okuda and Haruhiko Takeyama, Mitsubishi Electric Corporation, JP

12.5 Accelerator Design and Heterogeneous Architectures

Konferenz 3 1600 - 1730

Chair: **Cristina Silvano,** Politecnico di Milano, IT
Co-Chair: **Todd Austin,** University of Michigan, US

This session presents papers on heterogenous systems with focus on hardware acceleration. The first two papers propose acceleration for general pur-

pose and domain specific computing, respectively. The third paper addresses the issue of system interconnect for many-accelerator systems. The last paper introduces a data oriented accelerator design for sparse matrix operations.

1600 **A RECONFIGURABLE HETEROGENEOUS MULTICORE WITH A HOMOGENEOUS ISA**
Speaker: Antonio Carlos Schneider Beck, Universidade Federal do Rio Grande do Sul (UFRGS), BR
Authors: Jeckson Dellagostin Souza[1], Luigi Carro[1], Mateus Beck Rutzig[2] and Antonio Carlos Schneider Beck Filho[1]
[1]Universidade Federal do Rio Grande do Sul (UFRGS), BR; [2]Universidade Federal de Santa Maria, BR

1630 **THE NEURO VECTOR ENGINE: FLEXIBILITY TO IMPROVE CONVOLUTIONAL NETWORK EFFICIENCY FOR WEARABLE VISION**
Speaker: Maurice Peemen, Eindhoven University of Technology, NL
Authors: Maurice Peemen[1], Bart Mesman[1], Henk Corporaal[1], Runbin Shi[2], Sohan Lal[3] and Ben Juurlink[3]
[1]Eindhoven University of Technology, NL; [2]Soochow University, CN; [3]TU Berlin, DE

1700 **IMPROVING SCALABILITY OF CMPS WITH DENSE ACCS COVERAGE**
Speaker: Gunar Schirner, Northeastern University, US
Authors: Nasibeh Teimouri, Hamed Tabkhi and Gunar Schirner, Northeastern University, US

1715 **HARDWARE ACCELERATOR FOR ANALYTICS OF SPARSE DATA**
Speaker: Eriko Nurvitadhi, Intel Corporation, US
Authors: Eriko Nurvitadhi, Asit Mishra, Yu Wang, Ganesh Venkatesh and Debbie Marr, Intel Corporation, US

12.6 Reconfigurable Computing Platforms and Architectures

Konferenz 4 1600 - 1730

Chair: **Dirk Stroobandt,** Ghent University, BE
Co-Chair: **Jürgen Becker,** Karlsruhe Institute of Technology (KIT), DE

In this session, we have three papers focused on design of platform and architectures for reconfigurable computing. The first paper described a dedicated hardware accelerator addressing the prohibitive computing demand of Homomorphic Encryption. The second paper develop larger, more efficient, overlays using multiple DSP blocks and then maximising their utilisation. The third paper proposes a novel scheme to dynamically optimize a reconfigurable VLIW processor by predicting and matching the number of active data-paths for each application phase.

1600 **SECURING THE CLOUD WITH RECONFIGURABLE COMPUTING: AN FPGA ACCELERATOR FOR HOMOMORPHIC ENCRYPTION**
Speaker: Alessandro Cilardo, University of Naples Federico II, IT
Authors: Alessandro Cilardo and Domenico Argenziano, University of Naples Federico II, IT

1630 **THROUGHPUT ORIENTED FPGA OVERLAYS USING DSP BLOCKS**
Speaker: Douglas L. Maskell, Nanyang Technological University, SG
Authors: Abhishek K. Jain[1], Douglas L. Maskell[1] and Suhaib A. Fahmy[2]
[1]Nanyang Technological University, SG; [2]University of Warwick, GB

1700 **RUN-TIME PHASE PREDICTION FOR A RECONFIGURABLE VLIW PROCESSOR**
Speaker: Stephan Wong, TUDelft, NL
Authors: Qi Guo[1], Anderson Sartor[2], Anthony Brandon[3], Xuehai Zhou[1] and Stephan Wong[3]
[1]University of Science and Technology of China, CN; [2]Universidade Federal do Rio Grande do Sul (UFRGS), BR; [3]TUDelft, NL

12.7 Formal System Level Verification

Konferenz 5 1600 - 1730

Chair: **Mathias Soeken,** École Polytechnique Fédérale de Lausanne (EPFL), CH
Co-Chair: **Gianpiero Cabodi,** Politecnio di Torino, IT

The session considers verification at the system level. The first paper deals with the combination of protocols and networks. The second paper refines real-time analysis from task level to the level of runnable entities within tasks. The third one focuses on the correctness of synthesis from high level models.

1600 **ADVOCAT: AUTOMATED DEADLOCK VERIFICATION FOR ON-CHIP CACHE COHERENCE AND INTERCONNECTS**
Speaker: Freek Verbeek, Open University of The Netherlands, NL
Authors: Freek Verbeek[1], Pooria Yaghini[2], Ashkan Eghbal[2] and Nader Bagherzadeh[2]
[1]Open University of The Netherlands, NL; [2]University of California, Irvine, US

1630 **GUARANTEES FOR RUNNABLE ENTITIES WITH HETEROGENEOUS REAL-TIME REQUIREMENTS**
Speaker: Leonie Ahrendts, Technische Universität Braunschweig, DE
Authors: Leonie Ahrendts, Zain A. H. Hammadeh and Rolf Ernst, Technische Universität Braunschweig, DE

1700 **VALIDATING SCHEDULING TRANSFORMATION FOR BEHAVIORAL SYNTHESIS**
Speaker: Sandip Ray, Intel Corporation, US
Authors: Zhenkun Yang[1], Kecheng Hao[2], Kai Cong[3], Li Lei[1], Sandip Ray[3] and Fei Xie[1]
[1]Portland State University, US; [2]Xilinx Inc., US; [3]Intel Corporation, US

W01 TRUDEVICE 2016: Workshop on Trustworthy Manufacturing and Utilization of Secure Devices

Konferenz 6 0830 - 1700

General Chair: **Giorgio Di Natale,** LIRMM, FR
Co-Chair: **Ilia Polian,** University of Passau, DE
Chair: **Francesco Regazzoni,** AlaRI, CH
Committee Vice-Chair: **Nicolas Sklavos,** University of Patras, GR

Security is becoming increasingly important for cyber-physical and embedded systems: secure applications such as public services, communication, control of critical infrastructure and healthcare keep growing, however devices that implement cryptography functions has become the Achille's heel in the last decade.

The TRUDEVICE Workshop will provide an environment for researchers from academia and industry who want to discuss recent findings, theories and ongoing work on all aspects of device security including design, manufacturing, testing, reliability, validation and utilization. Program will include invited talks, contributed talks and work in progress. Topics of the workshop include but are not limited to:

- Trustworthy manufacturing and testing of secure devices
- Reconfigurable devices for secure functions
- Attacks on cyber-physical and medical devices and countermeasures
- PUFs and TRNGs
- Detection of malicious components in critical infrastructure and mobile devices
- Fault attack injection, detection and protection
- Tools for secure design
- Validation, evaluation

Opening Session

0830 - 1030

0830 TRUDEVICE: TRUSTWORTHY MANUFACTURING AND UTILIZATION OF SECURE DEVICES
Speakers: Giorgio Di Natale[1], Ilia Polian[2], Francesco Regazzoni[3] and Nicolas Sklavos[4]
[1]LIRMM, FR; [2]University of Passau, DE; [3]AlaRI, CH; [4]University of Patras, GR

Keynote Talk 1

0845 - 1030

Chair: **Ilia Polian,** University of Passau, DE

0845 ON THE NEED FOR SIDE-CHANNEL PROTECTION FOR IOT DEVICES
Speaker: De Mulder Elke, Cryptography Research, Rambus, FR

Session 1

0930 - 1030

Chair: **Tim Güneysu,** University of Bremen, DE

0930 ASSESSMENT OF THE LASER-INDUCED FAULT MODEL TOWARDS CONTINUOUS CMOS TECHNOLOGY SHRINKAGE
Authors: Jean-Max Dutertre[1], Philippe Candelier[2], Clement Champeix[2], Stephan De Castro[3], Giorgio Di Natale[3], Marie-Lise Flottes[3], Marc Lacruche[1], Mathieu Lisart[2], Jean-Baptiste Rigaud[1], Cyril Roscian[4], Bruno Rouzeyre[5] and Alexandre Sarafianos[2]
[1]ENSM-SE, FR; [2]STMicroelectronics, FR; [3]LIRMM, FR; [4]École Nationale Supérieure des Mines de Saint-Étienne, FR; [5]University Montpellier, FR

0945 RELIABILITY MODEL OF TMR SYSTEM CONSIDERING TRANSIENT FAULTS
Authors: Martin Danhel, Filip Štepanek and Hana Kubatova
Faculty of Information Technology - Czech Technical University in Prague, CZ

1000 SCAN CHAIN ENCRYPTION FOR THE TEST, DIAGNOSIS AND DEBUG OF SECURE CIRCUITS
Authors: Giorgio Di Natale[1], Marie-Lise Flottes[1], Bruno Rouzeyre[2], Paolo PRINETTO[3] and Marco Restifo[3]
[1]LIRMM, FR; [2]University Montpellier, FR; [3]Politecnico di Torino, IT

1015 EVOLUTIONARY ALGORITHMS AND THE DESIGN OF S-BOXES FOR ENERGY EFFICIENT CIPHERS
Authors: Stjepan Picek[1], Bohan Yang[2], Vladimir Rožić[3], Nele Mentens[4] and Ingrid Verbauwhede[5]
[1]Faculty of Electrical Engineering and Computing, HR; [2]ESAT/COSIC, BE; [3]K.U.Leuven, BE; [4]ESAT/COSIC and iMinds, KU Leuven, BE; [5]KU Leuven and UCLA, BE

Poster Session 1

1030 - 1100

Chair: **Nicolas Sklavos,** University of Patras, GR

1030 RELAIBILITY MODEL OF TMR SYSTEM CONSIDERING TRANSIENT FAULTS
Authors: Martin Danhel, Filip Štepanek and Hana Kubatova
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A 16-BIT FPGA PROCESSOR FOR ∏ -CIPHER
Authors: Mohamed El-Hadedy[1], Hristina Mihajloska[2], Danilo Gligoroski[3] and Kevin Skadron[4]
[1]Research Associate, US; [2]University Ss Cyril and Methodius, MK; [3]NTNU, NO; [4]University of Virginia, US

ANDTROJANID? ANDROID TROJANS IDENTIFICATION USING DYNAMIC FEATURE
Authors: Jelena Milosevic[1], Alberto Ferrante[2] and Miroslaw Malek[2]
[1]ALaRI, CH; [2]ALaRI - USI, CH

CYBER ATTACK/DEFENSE ALGORITHMS BASED ON DATA HIDING IN COMPRESSED VIDEO STREAM
Authors: Yaron Amsalem and Ofer Hadar, Ben-Gurion University, IL

STT-MTJ-BASED TRUE RANDOM NUMBER GENERATOR
Authors: Elena Ioana Vatajelu, Giorgio Di Natale and Paolo Prinetto
Politecnico di Torino, IT

CHARACTERIZATION OF HIGH-SPEED Q-RNG USING CMOS PHOTON COUNTING DETECTORS
Authors: Emna Amri[1], Siddharth Sinha[2], Yacine Felk[1], Francesco Regazzoni[3], Damien Stucki[1] and Edoardo Charbon[4]
[1]IDQuantique, CH; [2]TUDelft, NL; [3]AlaRI, CH; [4]TUDelft and EPFL, CH

STUDY OF SECURITY-AWARENESS IN CYBER-PHYSICAL INTERNET OF THINGS
Authors: Viacheslav Izosimov and Martin Törngren
The Royal Institute of Technology (KTH), SE

ASSESSMENT OF THE LASER-INDUCED FAULT MODEL TOWARDS CONTINUOUS CMOS TECHNOLOGY SHRINKAGE
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PROTECTING FPGA TARGETS IN HOSTILE ENVIRONMENT: A PROPOSITION FOR KILL-SWITCH IN FPGA
Authors: Debapriya Basu Roy, Shivam Bhasin, Jean-Luc Danger, Debdeep Mukhopadhyay and Sylvain Guilley
Indian Institute of Technology, IN

Session 2

1100 - 1300

Chair: **Stjepan Picek,** Faculty of Electrical Engineering and Computing, HR

1100 UTILIZING INTRINSIC DELAY VARIABILITY IN COMPLEX DIGITAL CIRCUITS FOR DEFINING PUF BEHAVIOR
Authors: Matthias Sauer[1], Linus Feiten[1], Bernd Becker[1], Ulrich Rührmair[2] and Ilia Polian[3]
[1]University of Freiburg, DE; [2]Technische Universität München, DE; [3]University of Passau, DE

1115 **KEY RECONCILIATION PROTOCOL APPLICATION TO ERROR CORRECTION IN SILICON PUF RESPONSES**
Authors: Brice Colombier[1], Bossuet Lilian[1] and David Hely[2]
[1]University of St. Etienne, FR; [2]Univ. Grenoble Alpes, FR

1130 **ON METRICS TO QUANTIFY THE INTER-DEVICE UNIQUENESS OF PHYSICALLY UNCLONABLE FUNCTIONS**
Authors: Linus Feiten, Matthias Sauer and Bernd Becker, University of Freiburg, DE

1145 **TOTAL: TRNG ON-THE-FLY TESTING FOR ATTACK DETECTION USING LIGHTWEIGHT HARDWARE**
Authors: Bohan Yang[1], Vladimir Rožić[2], Nele Mentens[3], Wim Dehaene[4] and Ingrid Verbauwhede[5]
[1]ESAT/COSIC, BE; [2]K.U.Leuven, BE; [3]ESAT/COSIC and iMinds, KU Leuven, BE; [4]imec vzw, KU Leuven, BE; [5]KU Leuven and UCLA, BE

1200 **STT-MTJ-BASED TRUE RANDOM NUMBER GENERATOR**
Authors: Elena Ioana Vatajelu[1], Giorgio Di Natale[2] and Paolo PRINETTO[3]
[1]POLITO, IT; [2]LIRMM, FR; [3]Politecnico di Torino, IT

Keynote Talk 2

1300 - 1345

Chair: **Giorgio Di Natale,** LIRMM, FR

1300 **IMPLANT SECURITY: THE NEW DEEP END**
Speaker: Christos Strydis, Erasmus Medical Center, NL

Session 3

1345 - 1430

Chair: **Nele Mentens,** ESAT/COSIC and iMinds, KU Leuven, BE

1345 **MALICIOUS HARDWARE LOGIC DETECTION BASED ON COMBINATORIAL TESTING**
Authors: Paris Kitsos[1], Dimitris Simos[2], Kyriakos Stefanidis[3] and Artemios G. Voyiatzis[3]
[1]Technological Educational Institute of Western Greece, GR; [2]SBA Research, AT; [3]ATHENA RC-ISI, GR

1400 **DUPLICATION-BASED CONCURRENT DETECTION OF HARDWARE TROJANS IN INTEGRATED CIRCUITS**
Authors: Palanichamy Manikandan[1], Papa-Sidy Ba[2], Sophie Dupuis[2], Marie-Lise Flottes[2], Giorgio Di Natale[2] and Bruno Rouzeyre[3]
[1]LIRMM, Univ. Montpellier, Montpellier, France, FR; [2]LIRMM, FR; [3]University Montpellier, FR

1415 **LOW-OVERHEAD HARDWARE TROJAN INSERTION IN CRYPTOGRAPHIC ICS**
Authors: Ioannis Voyiatzis, P. Kyrkos, Thanos Milidonis and Costas Efstathiou
Technological Educational Institute of Athens, GR

Poster Session 2

1430 - 1500

Chair: **Nicolas Sklavos,** University of Patras, GR

1430 **RELAIBILITY MODEL OF TMR SYSTEM CONSIDERING TRANSIENT FAULTS**
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[1]Department of Computer Science and Engineering, Indian Institute of Technology Kharagpur, IN; [2]Télécom ParisTech, FR; [3]Indian Institute of Technology, IN

Session 4

1500 - 1545

Chair: **Nicolas Sklavos,** University of Patras, GR

1500 **AUTOMATIC SIDE-CHANNEL LEAKAGE MITIGATION AT THE MICRO-ARCHITECTURE LEVEL**
Author: Hermann Seuschek, Technische Universität München, DE

1515 **A WAVEFORM-MATCHING TRIGGERING SYSTEM FOR IMPLEMENTATION ATTACKS**
Authors: Arthur Beckers[1], Josep Balasch[1], Benedikt Gierlichs[1] and Ingrid Verbauwhede[2]
[1]Katholieke Universiteit Leuven, BE; [2]KU Leuven and UCLA, BE

1530 **GLIFRED: GLITCH-FREE DUPLICATION TOWARDS POWER-EQUALIZED CIRCUITS ON FPGAS**
Authors: Alexander Wild[1], Amir Moradi[2] and Tim Güneysu[3]
[1]Horst Görtz Institute for IT Security, Ruhr University Bochum, DE; [2]Ruhr University Bochum, DE; [3]University of Bremen, DE

Session 5

1545 - 1645

1545 **EXTENDING REMOTE ATTESTATION FOR HARDWARE RECONFIGURABLE TRUSTED PLATFORMS**
Authors: Domenico Amelino, Mario Barbareschi, Alessandro Cilardo and Antonino Mazzeo, University of Naples Federico II, IT

1600 **ANDTROJANID? ANDROID TROJANS IDENTIFICATION USING DYNAMIC FEATURE**
Authors: Jelena Milosevic[1], Alberto Ferrante[2] and Miroslaw Malek[2]
[1]ALaRI, CH; [2]ALaRI - USI, CH

1615 **STUDY OF SECURITY-AWARENESS IN CYBER-PHYSICAL INTERNET OF THINGS**
Authors: Viacheslav Izosimov and Martin Törngren
The Royal Institute of Technology (KTH), SE

1630 **AN FPGA BASED THIRD-PARTY INTELLECTUAL PROPERTY ISOLATION MECHANISM**
Authors: Mario Barbareschi, Salvatore Miranda and Antonino Mazzeo, University of Naples Federico II, IT

Closing Session

1645 - 1700

1645 **CLOSING REMARKS**
Speaker: Giorgio Di Natale, LIRMM, FR
Authors: Ilia Polian[1], Francesco Regazzoni[2] and Nicolas Sklavos[3]
[1]University of Passau, DE; [2]AlaRI, CH; [3]University of Patras, GR

W02 3rd Workshop on Design Automation for Understanding Hardware Designs, DUHDe 2016

Konferenz 1 0830 - 1620

Organisers: **Ian Harris,** University of Californa Irvine, US
Mathias Soeken, Universität Bremen, DE

Understanding a hardware design is tough. When entering a large team as a new member, when extending a legacy design, or when documenting a new design, a lack in understanding the details of a design is a major obstacle for productivity. In software engineering topics like software maintenance, software understanding, reverse engineering are well established in the research community and partially tackled by tools. In the hardware area the re-use of IP-blocks, the growing size of designs and design teams leads to similar problems. Understanding of hardware requires deep insight into concurrently operating units, optimizations to reduce the required area, and specially tailored functional units for a particular use.

The aim of the 3rd Workshop on Design Automation for Understanding Hardware Designs (DUHDe) is to consolidate the community for these topics in electronic design automation.

The workshop is not limited to the following topics in design understanding but includes:

- Design descriptions from the FSL (Formal Specification Level) to ESL (Electronic System Level) down to RTL (Register Transfer Level)
- Extraction of high-level properties
- Feature Localization: Localization of code implementing specialized functionality
- Synthesis and Verification from Natural Language
- Hardware design evolution: feature integration, feature interactions
- Reverse Engineering
- Innovative GUIs for design
- Analysis of interaction between hardware and software
- Formal methods for design understanding
- Scalable approaches to design understanding

Greeting Session

0830 - 0835

Organisers: **Ian Harris,** University of Californa Irvine, US
Mathias Soeken, Universität Bremen, DE

Session 1

0835 - 1000

0835 **INVITED TALK: WHERE ARE MY REQUIREMENTS? A FORGOTTEN PIECE OF THE TRUSTWORTHY DESIGN PUZZLE**
Speaker: Sandip Ray, Intel Corporation, US

0935 **VERIFICATION AND DEBUGGING OF SCIENTIFIC COMPUTATIONS WITH HARDWARE THROUGH EXTRACTION OF ARITHMETIC ASSERTIONS**
Author: Masahiro Fujita, University of Tokyo, JP

Coffee Break

1000 - 1020

Session 2

1020 - 1220

1020 **THE SUBSET PERMUTATION-INDEPENDENT CONDITIONAL EQUIVALENCE CHECKING PROBLEM**
Authors: Mathias Soeken[1], Baruch Sterin[2] and Robert Brayton[2]
[1]Universität Bremen, DE; [2]University of California Berkeley, US

1045 **TRANSPARENT LOGIC IN HARDWARE DESIGNS**
Authors: Yu-Yun Dai and Robert Brayton, University of California Berkeley, US

1110 **SIGNATURE-BASED SUB-CIRCUIT EXTRACTION**
Authors: Amir Masoud Gharehbaghi[1] and Masahiro Fujita[2]
[1]The University of Tokyo, JP; [2]University of Tokyo, JP

1135 **MATCHING ABSTRACT AND CONCRETE HARDWARE MODELS FOR DESIGN UNDERSTANDING**
Author: Tino Flenker, University of Bremen, DE

Lunch Break

1200 - 1320

Session 3

1320 - 1445

1320 **INVITED TALK: WHAT CAN ALGEBRAIC GEOMETRY TELL US ABOUT THE FUNCTION IMPLEMENTED BY A CIRCUIT?**
Speaker: Priyank Kalla, University of Utah, US

1420 **CHANGE MANAGEMENT FOR HARDWARE DESIGNERS**
Authors: Martin Ring[1], Jannis Stoppe[2], Christoph Luth[2] and Rolf Drechsler[2]
[1]Deutsches Forschungszentrum fur Kunstliche Intelligenz, DE;
[2]University of Bremen, DE

Coffee Break

1445 - 1505

Session 4

1505 - 1620

1505 **OPPORTUNITIES FOR ANALYZING HARDWARE SPECIFICATIONS WITH NLP TECHNIQUES**
Authors: Alejandro Rago, Claudia Marcos and Andrés Diaz-Pace, Instituto Superior de Ingeniería de Software (ISISTAN-UNICEN) Tandil, Buenos Aires, Argentina, AR

1530 **SYCVIEW: VISUALIZE AND PROFILE SYSTEMC SIMULATIONS**
Authors: Denis Becker[1], Matthieu Moy[2] and Jerome Cornet[1]
[1]ST Microelectronics F-38019 Grenoble, France, FR; [2]Verimag, Grenoble, FR

1555 **VISUALIZING MICROFLUIDIC BIOCHIPS INTERACTIVELY**
Authors: Oliver Keszöcze, Robert Wille and Rolf Drechsler
University of Bremen, DE

W03 2nd Workshop on Model-Implementation Fidelity, MiFi'16

Konferenz 5 0830 - 1700

Organiser: **Christian Fabre,** CEA-LETI, Grenoble, FR

In early design stages, software and platform developers work with abstractions of the hardware in the form analytical models, simulators, or estimators for, e.g., communication bandwidth, heat propagation, voltage and frequency scaling and control, etc. These abstractions are utilized to verify the correctness of software algorithms, predict their potential behavior, e.g., performance, energy, temperature, in an actual environment, and take design decisions accordingly.

A crucial issue is the difficulty in assessing the fidelity of the abstract platform model versus the real platform. The challenge when conceiving and refining such abstraction is to ensure that: (1) models are reasonably accurate with respect to the real platform, (2) the final platform is indeed an implementation of the model, and the properties verified or predicted at the model level are also satisfied by the implementation.

Opening session

0830 - 0840

Chair: **Christian Fabre,** CEA-LETI, Grenoble, FR

Session 1

0840 - 1010

0840 **TECHNOLOGY TRENDS AND THEIR IMPACT ON HPC BENCHMARKS**
Speaker: Xavier Vigouroux, Atos, FR

0930 **FIDELITY OF NATIVE-BASED PERFORMANCE MODELS FOR DESIGN SPACE EXPLORATION**
Speaker: Fernando Herrera, University of Cantabria, ES
Authors: Eugenio Villar and Fernando Herrera, University of Cantabria, ES

0950 **THOUGHTS ON THE FIDELITY OF (DATA-FLOW) MODELS FOR REAL-TIME MPSOC ARCHITECTURES**
Speaker: Kees Goossens, Eindhoven Univ. of Technology, NL

Coffee break

1010 - 1030

Session 2

1030 - 1200

Chair: **Eugenio Villar,** University of Cantabria, ES

1030 **A TIMED-AUTOMATA BASED MIDDLEWARE FOR TIME-CRITICAL MULTICORE APPLICATIONS**
Speaker: Saddek Ben Salem, Verimag, FR

1100 **MICROPROCESSOR THERMAL MODELLING AND VALIDATION**
Speaker: Giovanni Beltrame, École Polytehcnique de Montréal, CA

1130 **ACCURATE ENVIRONMENT MODEL FOR OBSTACLE DETECTION USING MULTIPLE NOISY RANGE SENSORS AND IMPLEMENTATION ON INDUSTRIAL TARGETS**
Speaker: Julien Mottin, CEA LETI, FR
Authors: Julien Mottin[1], Diego Puschini[2] and Tiana Rakotovao[1]
[1]CEA LETI, FR; [2]CEA, LETI, MINATEC, FR

W04 IMPAC: Getting more for less: Innovative MPSoC Architecture Paradigms for Analysability and Composability of Timing and Power

Konferenz 2 0830 - 1500

Organisers: **Ralph Görgen,** OFFIS, DE
Francisco J. Cazorla, Barcelona Supercomputing Center, ES
Roman Obermaisser, University of Siegen, DE

Today's MPSoCs cannot only potentially provide high performance but also the possibility of integrating more than one application. With more than one application, different workload demands need to be handled like strict timing for safety critical real-time applications or best-effort computation for, e.g., video processing. Ensuring dependable behaviour of such systems with respect to timing and power is a huge challenge for state-of-the-art analysis methods. Without support from the hardware platform, firmware and software, this analysis can become extremely cumbersome. Furthermore, the independent analysis and incremental integration of different applications on a single chip becomes infeasible.

To support the analysability of MPSoCs, predictable and composable architectures with appropriate software layer support have been proposed. This ranges from less-predictable best effort (Average Case Analysis) over cycle-level predictable (Static Timing Analysis) to predictable and randomized (Probabilistic Timing Analysis) MPSoC platforms.

This workshop aims at presenting and discussing the latest research results within this spectrum of topics, with emphasis on new on-chip architectures and analysis paradigms to enable fast, yet accurate, and dependable analysis, to support the incremental integration of heterogeneous applications in MPSoCs. The workshop, whose presentations are by invitation only, will bring together representatives of the major European projects in the field as well as academic/industrialist experts on the field. The workshop audience will be exposed to the latest developments, at hardware and software level, on predictable and composable platforms.

Welcome and Opening

0830 - 0840

Session 1a: Analysis Methods and Platform Requirements for Analysability

0840 - 1015

0840 **AVIONICS REQUIREMENTS FOR DEPENDABILITY AND COMPOSABILITY**
Speaker: Sascha Uhrig, Airbus Group Innovations, DE

0925 **STATIC CODE LEVEL TIMING ANALYSIS ON SYSTEMS WITH INTERFERENCE**
Speaker: Christian Ferdinand, AbsInt, DE

0950 **ADDRESSING THE PATH COVERAGE PROBLEM WITH MEASUREMENT-BASED TIMING ANALYSIS**
Speaker: Tullio Vardanega, University of Padua, IT

Session 1b: Analysis Methods and Platform Requirements for Analysability

1045 - 1135

1045 **ANALYSIS OF POWER - MEASUREMENT, SIMULATION, AND COMPOSABILITY**
Speaker: Kim Grüttner, OFFIS - Institute for Information Technology, DE

1110 **SHORT PANEL 1: STATIC ANALYSIS VS. MEASUREMENT-BASED ANALYSIS**
Panelists: Sascha Uhrig[1], Christian Ferdinand[2], Tullio Vardanega[3] and Kim Grüttner[4]
[1]Airbus Group Innovations, DE; [2]AbsInt, DE; [3]University of Padua, IT; [4]OFFIS - Institute for Information Technology, DE

Session 2a: Concepts for Composable Dependable Architectures

1135 - 1200

1135 **DREAMS: DEPENDABLE NOC**
Speaker: Roman Obermaisser, University of Siegen, DE

Session 2b: Concepts for Composable Dependable Architectures

1300 - 1500

1300 **MODEL-BASED CODE GENERATION FOR THE MPPA MANYCORE PROCESSOR**
Speaker: Benoit Dupont de Dinechin, Kalray, FR

1320 **SAFE AND SECURE REAL-TIME (SSRT)**
Speaker: Benjamin Gittins, Synaptic Laboratories Limited, MT

1340 **PROXIMA PROBABILISTIC ARCHITECTURE FOR FPGA AND COTS**
Speaker: Francisco J. Cazorla, Barcelona Supercomputing Center, ES

1405 **COMPSOC: A PREDICTABLE AND COMPOSABLE MULTICORE SYSTEM**
Speaker: Kees Goossens, Eindhoven Univ. of Technology, NL

1435 **SHORT PANEL 2: COSTS OF HARDWARE-SUPPORT FOR DEPENDABILITY**
Panelists: Roman Obermaisser[1], Benoit Dupont de Dinechin[2], Benjamin Gittins[3], Francisco J. Cazorla[4] and Kees Goossens[5]
[1]University of Siegen, DE; [2]Kalray, FR; [3]Synaptic Laboratories Limited, MT; [4]Barcelona Supercomputing Center, ES; [5]Eindhoven Univ. of Technology, NL

W05 ERMAVSS: Workshop on Early Reliability Modeling for Aging and Variability in Silicon Systems

Seminar 5-6 0830 - 1700

Co-Chairs: **Adrian Evans,** iRoC Technologies, FR
Praveen Raghavan, IMEC, BE
Dimitris Gizopoulos, University of Athens, GR
Stefano Di Carlo, Politecnico di Torino, IT
Publicity Chair: **Roland Jancke,** Fraunhofer IIS/EAS, DE

With the proliferation of integrated circuits implemented in the most advanced process technologies, there is a growing need to jointly analyze the effect of multiple sources of failures including variability and aging and to understand, early in the design cycle, their impact on system reliability. Today, conservative margins are required to ensure that devices operate correctly over their full lifetime, despite the impact of aging effects (BTI, HCI) and failure mechanisms such as EM. New methodologies for improved cross-layer modeling and mitigation, if planned early in the design of a product, have the potential to remove unnecessary conservatism, reduce power and cost and improve yield. This workshop is focused on sharing new research on techniques and methodologies for modeling the effects of failures due to transistor aging, variability and other mechanisms all the way from the cell level to system level. New approaches to perform early estimations of system reliability are much needed to enabling reliable, optimized and low-power designs.

Welcome and Opening

0840 - 0900

Chair: **Adrian Evans,** iRoC Technologies, FR

0840 **CLERECO PROJECT OVERVIEW**
Speaker: Stefano Di Carlo, Politecnico di Torino, IT

0850 **MORV PROJECT OVERVIEW**
Speaker: Domenik Helms, OFFIS, DE

Session I - Invited Talks

0900 - 0945

Chair: **Dimitris Gizopoulos,** University of Athens, GR

0900 **THE RESILIENCE WALL: CROSS-LAYER SOLUTIONS**
Speaker: Subhasish Mitra, Stanford University, US

0945 **RELIABILITY CHALLENGES FOR LARGE ASICS**
Speaker: Yongsheng Sun, HiSilicon, CN

Session II - Poster Session

1030 - 1100

Chair: **Domenik Helms,** OFFIS, DE

1030 **APPROXIMATING STANDARD CELL DELAY DISTRIBUTIONS USING THE MOST PROBABLE FAILURE POINT**
Authors: Dimitrios Rodopoulos[1], Philippe Roussel[2], Francky Catthoor[2], Yanos Sazeides[3] and Dimitrios Soudris[4]
[1]NTUA/ICCS, GR; [2]IMEC, BE; [3]University of Cyprus, CY; [4]National Technical Univ. of Athens and ICCS, GR

DESIGN-RELIABILITY FLOW AND ADVANCED MODELS ADDRESS IC RELIABILITY ISSUES
Authors: Mohamed Selim, Eric Jeandeau and Cyril Descleves
Mentor, FR

NBTI LIFETIME EVALUATION AND EXTENSION IN INSTRUCTION CACHES
Authors: Shengyu Duan[1], Basel Halak[1], Rick Wong[2] and Mark Zwolinski[1]
[1]University of Southampton, GB; [2]Cisco Systems Inc, US

RELIABILITY-AWARE DESIGN METHOD FOR CMOS CIRCUITS
Authors: Theodor Hillebrand[1], Nico Hellwege[2], Steffen Paul[1] and Dagmar Peters-Drolshagen[3]
[1]University of Bremen, DE; [2]ITEM, DE; [3]Institute of Electrodynamics and Microelectronics, DE

MULTI-PATH AGEING SENSOR FOR COST-EFFICIENT DELAY-FAULT PREDICTION
Authors: Gaole Sai[1], Basel Halak[1], Rick Wong[2] and Mark Zwolinski[1]
[1]University of Southampton, GB; [2]Cisco Systems Inc, US

EARLY FAILURE PREDICTION BY USING IN-SITU MONITORS: IMPLEMENTATION AND APPLICATION RESULTS
Author: Benhassain Ahmed
STMicroelectronics, FR

AGEING IMPACT ON A HIGH SPEED VOLTAGE COMPARATOR WITH HYSTERESIS
Authors: Illani Mohd Nawi, Basel Halak and Mark Zwolinski
University of Southampton, GB

OVERVIEW OF HEALTH MONITORING TECHNIQUES FOR RELIABILITY
Authors: Abhijit Deb, Bart Vermeulen and Luc van Dijk
NXP Semiconductors, NL

STATIC AGING ANALYSIS USING 3-DIMENSIONAL DELAY LIBRARY
Authors: Haider Abbas, Mark Zwolinski and Basel Halak
University of Southampton, GB

LPVM: LOW-POWER VARIATION-MITIGANT ADDER ARCHITECTURE USING CARRY EXPEDITION
Authors: Alireza Namazi and Meisam Abdollahi
Tehran University, IR

WORKLOAD IMPACT ON BTI HCI INDUCED AGING OF DIGITAL CIRCUITS: A SYSTEM LEVEL ANALYSIS
Author: Ajith Sivadasan
TIMA Laboratory, FR

Session III - Tools Demo

1100 - 1115

Chair: **Praveen Raghavan – IMEC,** BE

Session IV - Invited Talks

1115 - 1200

Chair: **Alberto Bosio,** LIRMM - University of Montpellier 2, FR

1100 **RELIABILITY AND SAFETY CHALLENGES OF AUTOMOTIVE DEVICES**
Speaker: Wu-Tung Cheng, Mentor, US

Session V - Invited Talks

1300 - 1345

Chair: **Stefano Di Carlo,** Politecnico di Torino, IT

1300 **ACCURACY VERSUS BREADTH IN CROSS-LAYER SOLUTIONS**
Speaker: Rob Aitken, ARM, US

Session VI - Embeded Tutorials

1340 - 1615

Chair: **Praveen Raghavan,** IMEC, BE

1340 **RELIABILITY AND VARIABILITY IN CMOS DEVICES**
Speaker: Ben Kaczer, IMEC, BE

1425 **AGING MODELS FOR ANALOG CIRCUIT LEVEL SIMULATIONS - INTEGRATION AND DEPLOYMENT CHALLENGES**
Speaker: Peter Rotter, Infineon Technologies, DE

1530 **AGING ON RT LEVEL - ANALYSIS AND MONITORING**
Speaker: Ulf Schlichtmann, Technische Universität München, DE

Session VII - Panel Session

1615 - 1700

Chair: **Stefano Di Carlo,** Politecnico di Torino, IT

Panelists: **Ronald Newhart,** IBM, US
Riccardo Mariani, YOGITECH SpA, IT
Tiberiu Seceleanu, ABB, SE

Wrap-Up and Closing Remarks

1700

Chair: **Adrian Evans,** iRoC Technologies, FR

W06 The 2nd International Workshop on Optical/ Photonic Interconnects for Computing Systems (OPTICS Workshop)

Konferenz 3 0830 - 1715

General Chairs: **Gabriela Nicolescu,** Polytechnique Montréal, CA
Jiang Xu, Hong Kong University of Science and Technology, CN
Sébastien Le Beux, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR

Programme Committee
Chair: **Mahdi Nikdast,** Polytechnique Montréal/McGill University, CA
Invited Speakers: **Akihiko Shinya,** NTT Basic Research Lab., JP
Alan Mickelson, University of Colorado at Boulder, US
Ayse Coskun, Boston University, US
Davide Bertozzi, University of Ferrara, IT
Ian O'Connor, Lyon Institute of Nanotechnology, FR
Jiang Xu, Hong Kong University of Science and Technology, CN
Josè Flich, Universidad Politecnica de Valencia, ES
Sebastien Rumley, University of Columbia, US
Mahdi Nikdast, Polytechnique Montréal/McGill University, CA
Marc Seifried, IBM Research Lab., Zurich, CH
Nikos Hardavellas, Northwestern University, US
Olivier Sentieys, INRIA - University of Rennes 1, FR
Isabella Cerutti, Scuola Superiore Sant'Anna, IT
Ruping Cao, Mentor Graphics Corp, FR
Sebastien Cremer, STMicroelectronics, FR
Yoan Léger, CNRS – FOTON, FR

Multiprocessor System-on-Chip (MPSoC) is becoming the standard for high-performance computing systems. The performance of an MPSoC is determined not only by the performance of its processing cores and memories, but also by how efficiently they collaborate with one another. As the technology advances and allows the integration of many processing cores, metallic interconnects in MPSoCs will consume significant power while imposing high latency and low bandwidth. Shifting to the many-core era necessitates considering an alternative interconnect technology to replace the traditional electrical interconnects. Among such technologies, photonic technology has demonstrated promising potentials to address the aforementioned issues with the metallic interconnects in MPSoCs. In this context, high-performance silicon photonic devices and circuits are necessary to construct photonic interconnect networks. Furthermore, it is required to explore the feasibility and performance of photonic interconnects as well as the guidelines and design requirements to realize such interconnects. OPTICS aims at discussing the most recent advances in photonic interconnects and silicon photonics for computing systems. Industry's and academia's views on the feasibility and recent progress of optical interconnects and silicon photonics will be discussed. The workshop is comprised of invited talks of the highest caliber in addition to refereed poster presentations. Topics to be discussed in the workshop include (but are not limited to) the following:

- Design Methodologies, Modeling and Tools: design space exploration, optimization, thermal-aware design, floor-planning, system-level modeling and simulation, etc.
- Architectures/Micro-Architectures: hybrid optical-electronic interconnects, passive/active-based optical switches networks, communication protocols, etc.
- Applications: high-performance computing, photonics interconnect for memory and many-core systems, etc.
- Silicon Photonics Devices and Circuits: circuit demonstrators, on-chip lasers, photodetectors, electro-optic modulators, optical/photonic switches and routers, athermal devices, high-bandwidth I/O, etc.

Introduction to OPTICS Workshop

0830 - 0840

Chair: **Gabriela Nicolescu,** Polytechnique Montréal, CA
Co-Chair: **Mahdi Nikdast,** Polytechnique Montréal/McGill University, CA

Morning Session I: What is New on the Technology Side?

0840 - 1030

Chair: **Sébastien Le Beux,** Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR

0840 **TOWARDS NEXT GENERATION OF SILICON PHOTONICS TECHNOLOGY**
Speaker: Sebastien Cremer, STMicroelectronics, FR

0910 **LASER INTEGRATION CHALLENGES FOR ON-CHIP OPTICAL INTERCONNECTS**
Speaker: Yoan Léger, CNRS – FOTON, FR

0930 **ELECTRO-OPTICAL INTEGRATION OF III-V-ON-SILICON FOR EFFICIENT ON-CHIP LASER SOURCES**
Speaker: Marc Seifried, IBM Research Lab., Zurich, CH

0950 **INTEGRATED NANOPHOTONICS FOR FJ/BIT ON-CHIP OPTICAL COMMUNICATIONS**
Speaker: Akihiko Shinya, NTT Basic Research Lab., JP

1010 **SELECTIVE COUPLING FUNCTIONALITIES FOR ON-CHIP MODE-DIVISION MULTIPLEXING**
Authors: Alberto Parini[1], Yann Boucher[2] and Christophe Peucheret[2]
[1]University of Ferrara, IT; [2]FOTON Laboratory, CNRS, FR

1015 **PHONOCMAP: AN APPLICATION MAPPING TOOL FOR PHOTONIC NETWORKS-ON-CHIP**
Authors: Edoardo Fusella and Alessandro Cilardo, University of Naples Federico II, IT

1020 **OPTISHARE: A DYNAMIC CHANNEL SHARING SCHEME FOR POWER EFFICIENT ON-CHIP OPTICAL ARCHITECTURES**
Authors: Eldhose Peter and Smruti R Sarangi, Indian Institute of Technology, IN

1025 **SYNTHESIS OF OPTICAL CIRCUITS WITH CONTRADICTORY OPTIMIZATION OBJECTIVES**
Authors: Arighna Deb[1], Robert Wille[2], Oliver Keszöcze[1], Stefan Hillmich[1] and Rolf Drechsler[3]
[1]University of Bremen, DE; [2]JKU, Au; [3]University of Bremen/DFKI GmbH, DE

Coffee Break and Poster Session

1030 - 1100

Morning Session II: Bringing Optical Communication into the Chip

1100 - 1200

Chair: **Mahdi Nikdast,** Polytechnique Montréal/McGill University, CA

1100 **OPTICAL INTERCONNECTIONS AND POWER CONSUMPTION IN CLOUD COMPUTING**
Speaker: Alan Mickelson, University of Colorado at Boulder, US

1120 **COMMUNICATION REQUIREMENTS INSIDE A CHIP**
Speaker: Josè Flich, Universidad Politecnica de Valencia, ES

1140 **MODELING AND ANALYSIS OF OFF-CHIP OPTICAL AND ELECTRICAL INTERCONNECTS AND INTERFACES**
Speaker: Jiang Xu, Hong Kong University of Science and Technology, HK

Lunch Break and Poster Session

1200 - 1300

Afternoon Session I: Silicon Photonic Interconnect Management

1300 - 1430

Chair: **Jiang Xu,** Hong Kong University of Science and Technology, HK

1300 **IMPACT OF HIGH-SPEED MODULATION ON THE SCALABILITY OF SILICON PHOTONIC**
Speaker: Sebastien Rumley, University of Columbia, US

1330 **TOWARDS ENERGY-PROPORTIONAL OPTICAL INTERCONNECTS**
Speaker: Nikos Hardavellas, Northwestern University, US

1350 **DESIGN SPACE EXPLORATION OF OPTICAL INTERFACES FOR SILICON PHOTONIC INTERCONNECTS**
Speaker: Olivier Sentieys, INRIA - University of Rennes 1, FR

1410 **THERMAL MANAGEMENT OF MANYCORE SYSTEMS WITH PHOTONIC NOCS**
Speaker: Ayse Coskun, Boston University, US

Coffee Break and Poster Session

1430 - 1500

Afternoon Session II: Design Methods and Challenges

1500 - 1640

Chair: **Gabriela Nicolescu,** Polytechnique Montréal, CA

1500 **NETWORK-ON-CHIP USING SILICON PHOTONICS WAVEGUIDE ARRAYS**
Speaker: Isabella Cerutti, Scuola Superiore Sant'Anna, IT

1520 **ENABLING SILICON PHOTONICS TECHNOLOGY WITH EDA**
Speaker: Ruping Cao, Mentor Graphics Corp. / Lyon Institute of Nanotechnologies, FR

1540 **FABRICATION NON-UNIFORMITY IN SILICON PHOTONIC INTERCONNECTS**
Speaker: Mahdi Nikdast, Polytechnique Montréal/McGill University, CA

1600 **LAYOUT DESIGN OF WAVELENGTH-ROUTED OPTICAL NOCS: THE GLOBAL PICTURE**
Speaker: Davide Bertozzi, University of Ferrara, IT

1620 **THERMAL AWARE DESIGN METHOD FOR ON-CHIP OPTICAL INTERCONNECT**
Speaker: Ian O'Connor, Lyon Institute of Nanotechnology, FR

Panel Discussion

1640 - 1710

Moderator: **Ian O'Connor,** Lyon Institute of Nanotechnology, FR
Panelists: **Alan Mickelson,** University of Colorado at Boulder, US
Gabriela Nicolescu, Polytechnique Montréal, CA
Sebastien Rumley, University of Columbia, US
Sebastien Cremer, STMicroelectronics, FR
Yoan Léger, CNRS – FOTON, FR

Concluding Remarks and Closing Session

1710 - 1715

Chair: **Jiang Xu,** Hong Kong University of Science and Technology, HK
Co-Chair: **Sébastien Le Beux,** Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, FR

W07 International Workshop on Emerging Memory Solutions

Konferenz 4 0815 - 1700

General Chair: **Christian Weis,** University of Kaiserslautern, DE
Panel Chair: **Robert Aitken,** ARM, US
Programme Committee Chair: **Bastien Giraud,** CEA-LETI, Minatec, FR
Steering Committee Member: **Erik Jan Marinissen,** IMEC, BE
Publication Chairs: **Pascal VIVET,** CEA-LETI, FR
Matthias Jung, University of Kaiserslautern, DE

Memory manufacturing, architectures, design and test were deeply investigated to face issues linked to technology scaling such as increasing static power, maximum operating frequency and the gap between logic and memory minimum voltages. Various emerging memories solutions have appeared in recent years to replace either partially or totally already existing memories with an aim to overcome both technology and design related limitations in order to answer the requirements of many different applications. The goal of this Workshop is to bring together researchers, practitioners, and others interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges.

Topic Areas

You are invited to participate to 1st International DATE 2016 Friday Workshop on Emerging Memory Solutions. The covered areas of interest include (but are not limited to) the following topics:

- Volatile memory design (SRAM, DRAM, CAM or TCAM, etc.)
- Non-Volatile memory design (ReRAM, Flash, PCM, STT-RAM, etc.)
- Applications of emerging devices in memories (TFETs, nanowires, etc.)
- 3D memories (volatile and non-volatile)
- Processing in Memory
- Application specific memory solutions for emerging markets

– Test, design-for-test, and debug techniques
– Application, product, or test chip case studies

Opening and 1st Keynote

0815 - 0900

Chair: **Christian Weis,** University of Kaiserslautern, DE

0815 **WELCOME ADDRESS**
Speaker: Christian Weis, University of Kaiserslautern, DE

0820 **KEYNOTE: "TOMORROW'S HIGH-BANDWIDTH, HIGH-CAPACITY, LOW-POWER MEMORY SYSTEM"**
Speaker: Bruce Jacob, University of Maryland, US

Special Session on "Memory Challenges in Emerging Applications"

0900 - 1000

Chair: **Pascal VIVET,** CEA-Leti, FR

0900 **NEW APPROACHES TO UNIFIED MEMORIES**
Speaker: Paul Franzon, North Carolina State University, US

0920 **TURNING MEMORY CHALLENGES INTO OPPORTUNITIES**
Speaker: Andreas Hansson, ARM, GB

0940 **NON-VOLATILE MCU FOR IOT APPLICATIONS**
Speaker: Fabien Clermidy, CEA-Leti, FR

0955 **MAD: NEW LETI NON-VOLATILE MEMORY MPW PROTOTYPE PLATFORM**
Speaker: Fabien Clermidy, CEA-Leti, FR

Coffee Break & Poster Session 1

1000 - 1030

Invited Talk

1030 - 1100

Chair: **Rob Aitken,** ARM, US

1030 **"CIRCUIT AND ARCHITECTURAL TECHNIQUES FOR MINIMUM-ENERGY OPERATION OF SRAM-BASED CACHE ARRAYS"**
Speaker: Borivoje Nikolic, University of California, Berkeley, US

Panel: "Will current memories be replaced by new emerging NV memories? When and which ones?"

1100 - 1200

Moderator: **Rob Aitken,** ARM, US
Panelists: **David Turgis,** STMicroelectronics, FR
Ahmed Hemani, KTH, SE
Ivan Ivanov, Micron, DE
Ian O'Connor, ECL, FR
Yervant Zorian, Synopsys, US
Jan Van Houdt, IMEC, BE

Lunch Break

1200 - 1300

2nd Keynote

1300 - 1330

Chair: **Bastien Giraud,** CEA-Leti, FR

1300 **KEYNOTE: "ABUNDANT-DATA COMPUTING: THE N3XT 1,000XT"**
Speaker: Subhasish Mitra, Stanford University, US

Special Session on "Trends in Emerging Memory Technologies"

1330 - 1430

Chair: **Gregory Di Pendina,** CNRS-Spintec, FR

1330 **EMBEDDED ECC SOLUTIONS FOR EMERGING MEMORIES (PCMS)**
Speaker: Marco Ferrari, CNR-IEIIT, IT

1350 **CAN RRAMS BE MORE THAN JUST MEMORIES?**
Speaker: Pierre-Emmanuel Gaillardon, University of Utah, US

1410 **OXRAM MEMORY: FROM TECHNOLOGY TO MACROCELL DESIGN**
Speaker: Jean-Michel Portal, IM2NP, FR

Coffee Break & Poster Session 2

1430 - 1500

Industry Short Talks

1500 - 1530

Chair: **Matthias Jung,** University of Kaiserslautern, DE

1500 **HIGH BANDWIDTH MEMORY FOR FUTURE SYSTEM ARCHITECTURES**
Speaker: Yanghan Yoon, SK Hynix, DE
Author: Jaejin Lee, SK Hynix, US

1515 **SCALABLE AND EFFICIENT PROCESSING IN MEMORY FOR BIG DATA**
Speaker: Jean-Francois Roy, UPMEM, FR

Open Call Paper Session

1530 - 1645

Chair: **Kaya Can Akyel,** CEA-Leti, FR

1530 **SPIN ORBIT TORQUE MEMORY FOR NON-VOLATILE MICROPROCESSOR CACHES**
F.Oboril[1], R.Bishnoi[1], M.Ebrahimi[1], and M.Tahoori[1] , G. Di Pendina[2], K. Jabeur[2], G.Prenat[2]
[1]Karlsruhe Institute of Technology, DE
[2]Univ. Grenoble Alpes, CNRS, CEA, INAC-SPINTEC, Grenoble, FR

1545 **A COUNTER-BASED READ CIRCUIT TOLERANT TO PROCESS VARIATION FOR LOW-VOLTAGE OPERATING STT-MRAM**
Yohei Umeki[1], Koji Yanagida[1], Hiroaki Kurotsu[1], Hiroto Kitahara[1], Haruki Mori[1], Shintaro Izumi[1], Masahiko Yoshimoto[1],Hiroshi Kawaguchi[1], Shusuke Yoshimoto[2], Koji Tsunoda[3], Toshihiro Sugii[3]
[1]Graduate School of System Informatics Kobe University, JP
[2]The Institute of Scientific and Industrial Research, Osaka University, JP;
[3]Low-Power Electronics Association and Project (LEAP), JP

1600 **ENABLING LOW LEAKAGE SRAM MEMORIES AT SYSTEM LEVEL: A CASE STUDY**
Ajay Kapoor, Nur Engin, NXP Semiconductors, NL

1615 **A CASE FOR NEAR MEMORY COMPUTATION INSIDE THE SMART MEMORY CUBE**
Erfan Azarkhish[1], Davide Rossi[1], Igor Loi[1], Luca Benini[1,2]
[1]DEI, University of Bologna, Bologna, IT
[2]ITET, Swiss Federal Institute of Technology, Zurich, CH

1630 **DESIGN CONSIDERATIONS OF DIE-STACKED DRAM CACHES**
Rou-Li Melody Wang, Yun-Chao Yu, and Jin-Fu
Department of Electrical Engineering National Central University, TW

Poster List

1645 - 1650

Chair: **Kaya Can Akyel,** CEA-Leti, FR

1645 **MEMRISTOR: THE ENABLER FOR PROCESSING-IN-MEMORY**

ARCHITECTURE EVALUATION TOOL FOR 3D CAMS

APPLICATION STUDY: RRAM FOR LOW-POWER MICROCONTROLLERS

RAPIDO TESTING OF ASSISTED WRITE AND READ OPERATIONS FOR ULTRA-LOW POWER SRAMS

A WIDE-OPERATING RANGE STANDARD-CELL BASED MEMORY IN 28NM FD-SOI

CASE STUDY: 3D MEMORY CUSTOMISATIONS FOR THREE DATA-PARALLEL SCIENTIFIC APPLICATIONS

300MM & 200MM ADVANCED MEMORIES PLATFORM AND MPW SHUTTLE AT LETI

Closing

1650 - 1700

Chair: **Christian Weis,** University of Kaiserslautern, DE
Co-Chair: **Bastien Giraud,** CEA-Leti, FR

W08 First Workshop on Resource Awareness and Application Autotuning in Adaptive and Heterogeneous Computing

Seminar 3-4 0830 - 1630

Organisers: **Walter Stechele,** Technische Universität München, DE
Cristina Silvano, Politecnico di Milano, IT
Stephan Wong, TU Delft, NL

Adaptive and heterogeneous computing platforms are gaining interest for applications spanning from embedded to high performance computing due to their promising power/performance ratio. However, sharing hardware resources creates some challenges with respect to predictable execution time and power consumption. In traditional real-time approaches, resource usage is over dimensioned to achieve worst case guarantees, whereas in best effort approaches, predictability remains a challenge. The goal of the workshop is to bring together researchers from the area of resource awareness and application autotuning, to discuss their various approaches, their commonalities and differences, to foster collaboration between them and to share their most recent research achievements with the international research community.

Opening Session

0845 - 0900

0845 **OPENING**

Morning Session 1

0900 - 1100

0900 **PROGRAMMING AND BENCHMARKING FPGAS WITH SOFTWARE-CENTRIC DESIGN ENTRIES**
Speaker: Cathal McCabe, XILINX, IE

0930 **ADAPTIVE RESTRICTION AND ISOLATION FOR PREDICTABLE MPSOC STREAM PROCESSING**
Speaker: Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

1000 **INTRODUCTION TO THE POSTER SESSION**

Morning Session 2

1100 - 1200

1100 **ENERGY EFFICIENCY IN HIGH PERFORMANCE COMPUTING. EXAMPLES FROM RSC EXPERIENCE.**
Speaker: Alexander Moskovsky, RSC Group, RU

1130 **NEW COMPUTER ARCHITECTURES FOR HIGH PERFORMANCE COMPUTING - THE DEEP-ER AND MONT-BLANC PROJECTS**
Speaker: Axel Auweter, Leibniz Supercomputing Centre, DE

Afternoon Session 1

1300 - 1500

1300 **A DSL-BASED APPROACH FOR CROSS LAYER PROGRAMMING: MONITORING, ADAPTIVITY AND TUNING**
Speaker: João M. P. Cardoso, Faculty of Engineering (FEUP), University of Porto, PT

1330 **RESOURCE MANAGEMENT IN SELF-AWARE PLATFORMS**
Speaker: Axel Jantsch, Technical University of Vienna, AT

1400 **POSTER INTERACTIVE PRESENTATIONS**

Afternoon Session 2

1500 - 1630

1500 **DRIVERS AND SOLUTIONS FOR TAILORED AUTOMOTIVE ECU ARCHITECTURES**
Speaker: Andreas Rohatschek, Robert Bosch GmbH, DE

1530 **PANEL DISCUSSION ON "MOORE'S LAW IS STILL ALIVE! SO WHY RESOURCE AWARENESS?"**
Panelists: Cathal McCabe[1], Axel Auweter[2], João M. P. Cardoso[3], Axel Jantsch[4], X. Sharon Hu[5] and Michael Hübner[6]
[1]XILINX, IE; [2]Leibniz Supercomputing Centre, DE; [3]Faculty of Engineering (FEUP), University of Porto, PT; [4]Technical University of Vienna, AT; [5]University of Notre Dame, US; [6]Ruhr-University Bochum, DE

EXHIBITION THEATRE PROGRAMME

Organiser: **Jürgen Haase,** edacentrum GmbH, DE

In addition to the conference programme during DATE 16, there will be a presentation theatre as part of the exhibition from Tuesday, March 15, to Thursday, March 17, 2016. Attendees will profit from having an industry forum in the midst of Europe's leading electronic systems design event. The theatre is located in Seminar Rooms 3+4 which is in the Seminar Level close to the exhibition hall and affords easy access for exhibition visitors as well as for conference delegates.

The sessions of DATE 2016 Exhibition Theatre are open to conference delegates as well as to exhibition visitors.

Thematic Exhibition Campuses, MEMS Design Contest and special themed session on Education

The eleven Exhibition Theatre sessions will highlight technical presentations and panel discussions from the dedicated thematic campuses in the DATE16 Exhibition on IoT and secure systems, ultra-Low power technologies (FDSOI), 5G wireless networks, 3D-IC integration and automotive systems, with contributions from Bosch Sensortec, Fraunhofer, GLOBALFOUNDRIES, IDT/ZMDI, Infineon, Nokia, T-Systems and many more. A special themed session on the education of computer architects and SoC designers will be presented by Imagination Technologies, a world-wide contest for MEMS design will be announced in a workshop and organized by Cadence together with Coventor, X-FAB and University of Reutlingen.

Model Based Design and Verification Day

With its special "Model Based Design and Verification Day" DATE 2016 for the first time combines a visionary keynote from an industrial leader, application talks of experienced users and an industrial tutorial with two sessions of the DATE conference Technical Programme on latest research results in the field. This gives attendees the opportunity to get a comprehensive overview on start-of-the-art in model based design and verification, ranging from industrial application to academic research. This day comprises the Exhibition Theatre sessions 5.8 and 8.8., including the Exhibition Keynote given by Jim Tung, MathWorks Fellow at MathWorks Inc., and MathWorks tutorials, as well as the sessions 6.6 and 7.6 from the technical conference programme.

This Exhibition Theatre programme will be completed with an embedded tutorial on Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis (session 9.8).

Please see presented below information on the Exhibition Theatre sessions. Extensions of this programme, list of contributing companies and institutes and further details of the exhibition sessions will be published on the DATE web portal. Before your DATE attendance please visit the web portal for an update.

Exhibition Theatre

2.8	Revolutionising the Teaching of Computer Architecture and System on Chip Design	TUE 1130-1300
3.8	Presentations from FDSOI-Campus and from European Projects Booths: Leveraging new Semiconductor Technologies	TUE 1430-1600
4.8	Presentations from IoT-Campus (I): ASIC and Sensor Solutions	TUE 1700-1830
5.8	Model Based Design and Verification Day - Exhibition Keynote and Application Talk	WED 0830-1000
6.8	Presentations from 5G-Campus and European Projects Booths: 5G for the Connected World, Optimizing Computing Everywhere	WED 1100-1230
7.8	Presentations from IoT-Campus (II): IoT Survival Guide and Big Data Challenges	WED 1430-1600
8.8	Model Based Design and Verification Day - Tutorial: An Industry Approach to FPGA/ARM System Development and Verification	WED 1700-1830
9.8	Embedded Tutorial: Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis	THU 0830-1000
10.8	Presentations from Campus 3D-IC Integration: Opportunities for SMEs and Outlook 2020+	THU 1100-1230
11.8 & 12.8	Launch of the Worldwide MEMS Design Contest	THU 1400-1730

EXHIBITION SESSIONS

2.8 Revolutionising the Teaching of Computer Architecture and System on Chip Design

Exhibition Theatre 1130 - 1300

Moderator: **Robert Owen,** Imagination Technologies, GB

This special themed exhibition theatre session is for academics teaching Computer Architecture, Verification or System-on-Chip design. Companies with a commercial interest are also welcome. The real 'industrial' RTL code for a MIPS processor is now freely available for academic use under the Imagination University Programme and is called 'MIPSfpga'. MIPSfpga provides the RTL source code of the MIPS microAptiv UP (microprocessor) core together with teaching materials and reference designs for implementation on an FPGA. The MIPS microAptiv UP core is a member of the same microcontroller family found in many embedded devices, including the popular PIC32MZ micro-controller from Microchip and Samsung's new Artik1. The session begins with a short overview of Imagination's Worldwide University Programme ("IUP"), and will be presented by Robert Owen, Manager: IUP. Robert is well known in Universities around the world, having specialised in this field for more than 22 years, including the establishment of Texas Instruments' very first program in 1994. Alex Wong, Technical Systems Analyst from Digilent, will talk about the Digilent educational mission and how they collaborate with Imagination's University Programme to bring the latest technology, including an introduction to the Nexys 4 DDR which can be used with MIPSfpga. Munir Hasan, Solutions Engineer, will then present and demo MIPSfpga Fundamentals. It is a complete package of teaching materials, including slides, student manual and lab exercises. This package will show how to go from digital design blocks in RTL to Microprocessor to then creating an SoC. Zubair Kakakhel, Graduate Software Engineer, will present and demo MIPSfpga SoC. Linux is one of the most popular and scalable operating systems in the world. After learning the basics in MIPSfpga Fundamentals, we will now demonstrate how system level design tools such as Vivado IP Integrator can be used to make a complex soft-SoC that is capable of running Linux. We will then switch attention to the software, and show how we port the Linux kernel and Buildroot to run on our soft-SoC based platform. MIPSfpga SoC comes with structured labs that walk through the entire process in an digestible academic format. MIPSfpga SoC gives a genuine "behind the curtain" view of how the semiconductor industry works. Vendors sell various bits of IP blocks which are stitched together by chip manufacturers to make the brains of embedded systems around you. Additional WORKSHOP For those who want to go deeper, there's a half-day hands-on workshop at DATE on Wednesday 16th March, 08:30 to 12:30, Seminar Room 1.- EARLY Registration is recommended! HERE

1130 **IMAGINATION TECHNOLOGIES WORLDWIDE UNIVERSITY PROGRAMME**
Speaker: Robert Owen, Imagination Technologies, GB

1145 **HARDWARE TOOLS FOR UNIVERSITY LABS**
Speaker: Alex Wong, Digilent Inc., GB

1150 **MIPSFPGA FUNDAMENTALS**
Speaker: Munir Hasan, Imagination Technologies, GB

1220 **MIPSFPGA SOC**
Speaker: Zubair Kakakhel, Imagination Technologies, GB

1250 **Q&A**

1300 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

1600 **COFFEE BREAK IN EXHIBITION AREA**

3.8 Presentations from FDSOI-Campus and from European Projects Booths: Leveraging new Semiconductor Technologies

Exhibition Theatre 1430 - 1600

Organiser: **Hans-Jürgen Brand,** IDT/ZMDI, DE

In this session GLOBALFOUNDRIES gives an introduction to the applications of the ultra-low-power technology FDSOI and its innovation potential. The REPARA project will show how to make better use of the advances of new semiconductor technologies for parallel computing architectures, boosting application performance and energy efficiency. Attendees are invited to also

visit the ultra-low-power technologies campus and project booths for further details and discussions.

1430 **GLOBALFOUNDRIES 22FDX INNOVATION POTENTIAL**
Speaker: Gerd Teepe, GLOBALFOUNDRIES, DE

1530 **REPARA - REENGINEERING AND ENABLING PERFORMANCE AND POWER OF APPLICATIONS**
Speaker: Imre Pechan, evopro Innovation Kft., HU

1550 **Q&A**

1600 **COFFEE BREAK IN EXHIBITION AREA**

4.8 Presentations from IoT-Campus (I): ASIC and Sensor Solutions

Exhibition Theatre 1700 - 1830

Organiser: **Hans-Jürgen Brand,** IDT/ZMDI, DE

This session features presentations given by exhibitors from the Campus on IoT and Secure Systems, with a special focus on ASIC and sensor solutions for IoT applications. A second session (7.8) will highlight how IoT will change our life and how to design IoT devices. Attendees are invited to also visit the campus booths for further details and discussions.

1700 **DESIGNING IOT DEVICES WITH X-FAB'S OPEN-PLATFORM FOUNDRY TECHNOLOGIES**
Speaker: Ulrich Bretthauer, X-FAB, DE

1730 **CHALLENGES IN ASIC DEVELOPMENT FOR IOT SENSOR NODES**
Speaker: Dirk Droste, Bosch Sensortec GmbH, DE

1800 **SENSOR-PLATFORMS FOR IOT SOLUTIONS**
Speaker: Marko Mailand, IDT/ZMDI, DE

5.8 Model Based Design and Verification Day - Exhibition Keynote and Application Talk

Exhibition Theatre 0830 - 1000

Moderator: **John Zhao,** MathWorks Inc., US

With its special "Model Based Design and Verification Day" DATE 2016 for the first time combines a visionary keynote from an industrial leader, application talks of experienced users and an industrial tutorial with two sessions of the DATE conference Technical Program on latest research results in the field. This gives attendees the opportunity to get a comprehensive overview on start-of-the-art in model based design and test, ranging from industrial application to academic research. This session starts the day with an Exhibition Keynote given by Jimm Tung, MathWorks Fellow at MathWorks Inc., followed by an application talk, given by Robert Stewart, MathWorks Professor at University of Strathclyde. Please see the abstracts of the talks for more details. It will be followed by the Technical Program sessions 6.6 and 7.6 covering research work on modelling and control of cyber-physical systems and techniques for the analysis and testing of embedded software, respectively. The day will be completed with the Exhibition Theatre session 8.8 giving an industrial tutorial on FPGA/ARM System Development and Verification.

0830 **INTRODUCTION**
Speaker: John Zhao, MathWorks Inc., US

0835 **EXHIBITION KEYNOTE: THE TRANSFORMATIVE FUSION OF SENSING, COMPUTING, COMMUNICATION & CONTROL**
Speaker: Jim Tung, MathWorks Inc., US

0920 **APPLICATION TALK: MODEL BASED DESIGN FOR 4G AND 5G WIRELESS COMMUNICATIONS SOFTWARE DEFINED RADIO USING MATLAB**
Speaker: Robert Stewart, MathWorks Professor, University of Strathclyde, GB

0950 **Q&A**

1000 **COFFEE BREAK IN EXHIBITION AREA**

6.8 Presentations from 5G-Campus and European Projects Booths: 5G for the Connected World, Optimizing Computing Everywhere

Exhibition Theatre 1100 - 1230

Organiser: **Hans-Jürgen Brand,** IDT/ZMDI, DE

This session presents how 5G technology will enable the connected world of the future. Attendees are invited to also visit the campus booths for further details and discussions.

1100 **5G FOR THE CONNECTED WORLD**
Speaker: Rainer Liebhart, Nokia Networks, DE

1145 **COLLECTING AND SHARING KNOWLEDGE TO OPTIMIZE THE EFFICIENCY AND COST OF COMPUTING EVERYWHERE**
Speaker: Anton Lokhmotov, dividiti, GB

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

KEYNOTE LECTURE IN "SAAL 2" 1400 - 1430

7.8 Presentations from IoT-Campus (II): IoT Survival Guide and Big Data Challenges

Exhibition Theatre 1430 - 1600

Organiser: **Hans-Jürgen Brand,** IDT/ZMDI, DE

This session features presentations given by exhibitors from the Campus on IoT and Secure Systems and from the projects booths, with a special focus on how IoT will change our life and how to design IoT devices. A second session (4.8) will highlight ASIC and sensor solutions for IoT applications. Attendees are invited to also visit the campus and projects booths for further details and discussions.

1430 **DIGITAL TRANSFORMATION: THE SURVIVAL GUIDE FOR THE AGE OF BIG DATA, INDUSTRY 4.0 AND THE INTERNET OF THINGS**
Speaker: Christoph Kögler, T-Systems Multimedia Solutions GmbH, DE

1500 **IOT @ INFINEON TECHNOLOGIES**
Speaker: Uwe Gäbler, Infineon Technologies, DE

1530 **BIG DATA CHALLENGES IN HIGH ENERGY PHYSICS EXPERIMENTS: THE ATLAS (CERN) FAST TRACKER APPROACH**
Speaker: Calliope-Louisa Sotiropoulou, Universita' di Pisa and INFN Pisa, IT

1600 **COFFEE BREAK IN EXHIBITION AREA**

8.8 Model Based Design and Verification Day - Tutorial: An Industry Approach to FPGA/ARM System Development and Verification

Exhibition Theatre 1700 - 1830

Moderator: **John Zhao,** MathWorks Inc., US

With its special "Model Based Design and Verification Day" DATE 2016 for the first time combines a visionary keynote from an industrial leader, application talks of experienced users and an industrial tutorial with two sessions of the DATE conference Technical Program on latest research results in the field. This gives attendees the opportunity to get a comprehensive overview on start-of-the-art in model based design and test, ranging from industrial application to academic research. This session concludes the day with an industrial tutorial on FPGA/ARM System Development and Verification. The previous sessions of this day were Exhibition Theatre session 5.8 with an Exhibition Keynote given by Jim Tung, MathWorks Fellow at MathWorks Inc., and an Application Talk given by Robert Stewart, MathWorks Professor at University of Strathclyde, followed by the Technical Program sessions 6.6 and 7.6 covering research work on modelling and control of cyber-physical systems and techniques for the analysis and testing of embedded software, respectively.

1700 **TUTORIAL: AN INDUSTRY APPROACH TO FPGA/ARM SYSTEM DEVELOPMENT AND VERIFICATION**
Speaker: John Zhao, MathWorks Inc., US

9.8 Embedded Tutorial: Analog-/Mixed-Signal Verification Methods for AMS Coverage Analysis

Exhibition Theatre 0830 - 1000

Organiser: **Gregor Nitsche,** OFFIS, DE
Chair: **Lars Hedrich,** Johann Wolfgang Goethe-Universität, DE
Co-Chair: **Christoph Grimm,** University of Kaiserslautern, DE

Analog-/Mixed-Signal (AMS) design verification is one of the most challenging and time consuming tasks of today's complex system on chip (SoC) designs. Hence, to optimize time to market while ensuring safety and quality of the design, measuring the verification quality became crucial in deciding whether the regarded system is sufficiently tested or verified. Especially in the area of safety-critical design - e.g. automotive hardware and software applications - coverage metrics are commonly used to evaluate the amount of the already invested verification effort by comparing the number of analyzed verification or test scenarios with an overall number of scenarios. Due to the finite and discrete nature of digital systems the overall number can either be obtained from the model of the design (structural coverage) or from its specification (functional coverage). In contrast to digital system design, AMS designers have to deal with a continuous state space of conservative quantities, highly nonlinear relationships, differential equations etc., impeding compositionality and enlarging the number of possible states and behaviors to infinity. In addition to these functional properties, non-functional effects like crosstalk over supply or parasitic coupling have to be investigated in industrial size designs. Moreover, several levels of abstraction have to be considered, requiring methods for system level as well as transistor level circuits. Since digital domain coverage metrics are not directly applicable for AMS circuits and systems, industrial use-cases demand for novel coverage-oriented modeling and verification strategies to be investigated to tackle this challenge, making the quality and quantity of AMS verification measurable. Within this embedded tutorial we present methods and concepts to improve the AMS verification process and to allow for the evaluation of the coverage, proposing different metrics of AMS coverage.

0830 **TOWARDS MORE DEPENDABLE VERIFICATION USING SYMBOLIC SIMULATION**
Speaker: Carna Radojicic, University of Kaiserslautern, DE
Authors: Carna Radojicic[1], Christoph Grimm[1], Fabian Speicher[2] and Stefan Heinen[2]
[1]University of Kaiserslautern, DE; [2]RWTH Aachen, DE

0900 **IDENTIFICATION OF CRITICAL SCENARIOS IN AMS VERIFICATION: METHODOLOGY FOR FINDING THE SAFE OPERATING AREA OF AMS SYSTEMS**
Speaker: Georg Gläser, IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH, DE
Authors: Georg Gläser[1], Hyun-Sek Lukas Lee[2], Markus Olbrich[2], Erich Barke[2] and Eckhard Hennig[3]
[1]IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH, DE; [2]Leibniz Universität Hannover, DE; [3]Reutlingen University, DE

0930 **AMS LEAF-COMPONENT CHARACTERIZATION WITH CONTRACTS AND SATISFACTION CHECKING VS. ELECTRONIC CIRCUIT SCHEMATICS**
Speaker: Gregor Nitsche, OFFIS - Institute for Information Technology, DE
Authors: Gregor Nitsche[1], Andreas Fürtig[2], Lars Hedrich[2] and Wolfgang Nebel[3]
[1]OFFIS Institute for Information Technology, DE; [2]Goethe University, DE; [3]University of Oldenburg and OFFIS, DE

1000 **COFFEE BREAK IN EXHIBITION AREA**

10.8 Presentations from Campus 3D-IC Integration: Opportunities for SMEs and Outlook 2020+

Exhibition Theatre 1100 - 1230

Organiser: **Hans-Jürgen Brand,** IDT/ZMDI, DE

This session features presentations given by exhibitors from the Campus on 3D-IC Integration, highlighting special opportunities for SMEs and giving an outlook to 2020 and beyond. Attendees are invited to also visit the campus booths for further details and discussions.

1100 **HIGH PERFORMANCE CENTER FUNCTIONAL INTEGRATION IN MICRO AND NANOELECTRONICS - OPPORTUNITIES FOR SMES IN PRODUCT AND TECHNOLOGY DEVELOPMENT**
Speaker: Mario Walter, Fraunhofer Institute for Photonic Microsystems IPMS, DE

1200 **SOME THOUGHTS ON IC INTEGRATION IN 2020 & BEYOND**
Speaker: Anna Fontanelli, Monozukuri S.p.A., IT

1230 **LUNCH BREAK IN GROSSER SAAL + SAAL 1**

KEYNOTE LECTURE IN "SAAL 2" 1330 - 1400

11.8 Launch of the Worldwide MEMS Design Contest

Exhibition Theatre 1400 - 1730

Organiser: **Anton Klotz,** Cadence Design Systems, DE

The presentations at DATE Exhibition Theatre sessions 11.8 and 12.8 on 17th March from 14:00-17:30 are dedicated to the worldwide MEMS Design Contest, which is organized by Cadence Design Systems, Coventor, X-FAB and Reutlingen University. The aim of the contest is to motivate design teams to start designing chips with MEMS and mixed-signal blocks using X-FAB PDK and tools from Coventor and Cadence, to spread the knowledge about the co-design of MEMS and mixed-signal and to get new ideas how MEMS can be used and what kind of MEMS can be designed using the X-FAB PDK. The winning team gets the possibility to manufacture a demonstrator in silicon in order to prove the functionality of the flow. The session will start with a motivational talk about MEMS research in academia provided by Prof. Ibrahim Elfadel from MASDAR Institute. Then Anton Klotz, University Program Manager EMEA from Cadence Design Systems, explains the rules of the contest. Jörg Doblaski, Director Design Support from X-FAB, will present the mixed-signal and MEMS PDKs, which will be used in the contest. After that, Christopher Welham, Director Applications Engineering from Coventor, will explain front-end modeling of MEMS using Coventor tools. Finally, Ahmed Osman, Principal Application Engineerfrom Cadence Design Systems, will explain the design flow, which was developed based on the research work done in the BMBF-funded MEMS2015 project and will be used for the creation of mixed-signal logic and MEMS design at the contest.

1400 **ACADEMIC MEMS GOES FABLESS: THE MASDAR INSTITUTE PERSPECTIVE**
Speaker: Ibrahim Elfadel, MASDAR Institute of Science and Technology, AE

1420 **MEMS DESIGN CONTEST RULES**
Speaker: Anton Klotz, Cadence Design Systems, DE

1500 **PDK-BASED DESIGN AUTOMATION ENABLEMENT FOR MEMS- AND CMOS PROCESSES**
Speaker: Joerg Doblaski, X-FAB, DE

EXHIBITION SESSIONS

1600 **COVENTOR TOOLS FOR MODELLING AND SIMULATION OF MEMS**
Speaker: Christopher Welham, Coventor, FR

1645 **A MEMS-ASIC CO-DESIGN FLOW: AN EDA PERSPECTIVE**
Speaker: Ahmed Hussein Osman, Cadence Design Systems, DE

UNIVERSITY BOOTH

The University Booth is organised during DATE and will be located in booth 15 of the exhibition area. All demonstrations will take place from Tuesday, March 15 to Thursday, March 17, 2016 during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of 49 demonstrations from 18 different countries, presenting software and hardware solutions. The programme is organised in 11 sessions of 2 or 2.5 h duration and will cover the topics:

- 5G wireless network Prototypes
- 3D-IC integration Prototypes
- FD-SOI Prototypes
- IoT Prototypes
- Electronic Design Automation Prototypes
- Hardware Design and Test Prototypes
- Automotive System Prototypes

Secure System Prototypes

The University Booth at DATE 2016 invites you to booth 15 to find out more about the latest trends in software and hardware from the international research community.

Several demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information can be found online at http://www.date-conference.com/exhibition/u-booth. A University Booth programme flyer will be included in the conference bags. The following demonstrators will be presented at the University Booth.

6CH-SDR-PLATFORM: 6 CHANNEL SDR PROTOTYPING PLATFORM FOR VEHICLE SELF-LOCALIZATION
Presenter: Marko Rößler, Technische Universität Chemnitz, DE
Authors: Marko Rößler[1], Ulrich Heinkel[1], Daniel Fross[1] and Ahmad El-Assaad[2]
[1]Technische Universität Chemnitz, DE; [2]Novero GmbH, DE

A CIRCUIT EXTRACTION TOOL FOR FULL CUSTOM DESIGNED MEMS SENSORS
Presenter: Axel Hald, Robert Bosch GmbH, DE
Authors: Axel Hald[1], Johannes Seelhorst[1], Mathias Reimann[1], Juergen Scheible[2] and Jens Lienig[3]
[1]Robert Bosch GmbH, DE; [2]Reutlingen University, DE; [3]Technische Universität Dresden, DE

UNIVERSITY BOOTH

A-LOOP: AMP SYSTEM WITH A DUAL-CORE ARM CORTEX A9 PROCESSOR WITH LINUX OPERATING SYSTEM AND A QUAD-CORE LEON3 PROCESSOR WITH LINUX OPERATING SYSTEM, OPENMP LIBRARY AND HARDWARE PROFILING SYSTEM
Presenter: Giacomo Valente, Università Degli Studi Dell'Aquila, IT
Authors: Giacomo Valente and Vittoriano Muttillo, Università Degli Studi Dell'Aquila, IT

AGAMID: A TLM FRAMEWORK FOR EVALUATION OF HARDWARE-ENHANCED MANY-CORE RUN-TIME MANAGEMENT
Presenter: Daniel Gregorek, University of Bremen, DE
Authors: Daniel Gregorek and Alberto Garcia-Ortiz, University of Bremen, DE

AHLS_DESYNC: DESYNCHRONIZATION TOOL FOR HIGH-LEVEL SYNTHESIS OF ASYNCHRONOUS CIRCUITS
Presenter: Jean Simatic, TIMA Laboratory, FR
Authors: Jean Simatic, Rodrigo Possamai Bastos and Laurent Fesquet, TIMA Laboratory, FR

AIPHS: ADAPTIVE PROFILING HARDWARE SUB-SYSTEM
Presenter: Luigi Pomante, Università degli Studi dell'Aquila, IT
Authors: Luigi Pomante[1], Giacomo Valente[2] and Vittoriano Muttillo[2]
[1]Università degli Studi dell'Aquila, IT; [2]Università Degli Studi Dell'Aquila, IT

ALPT: A FAST PROTOTYPING METHODOLOGY WITH CONSTRAINED FLOORPLANING ON ANALOG LAYOUT GENERATION
Presenter: Po-Cheng Pan, National Chiao Tung University, TW
Authors: Po-Cheng Pan, Hung-Wen Huang and Hung-Ming Chen, National Chiao Tung University, TW

ANALYSIS AND VERIFICATION OF COMMUNICATION FABRICS
Presenter: Frank Burns, Newcastle University, UK
Authors: Frank Burns, Danil Sokolov and Alex Yakovlev, Newcastle University, UK

AUTOMATED REFINEMENT OF ANALOG/MIXED-SIGNAL SYSTEMC MODELS BY NON-FUNCTIONAL EFFECTS
Presenter: Georg Gläser, IMMS, DE
Authors: Georg Gläser[1], Hyun-Sek Lukas Lee[2], Eckhard Hennig[3], Markus Olbrich[2] and Erich Barke[2]
[1]IMMS, DE; [2]Leibniz Universität Hannover, DE; [3]Reutlingen University, DE

BIOVIZ: AN INTERACTIVE VISUALIZATION ENGINE FOR MICROFLUIDIC BIOCHIPS
Presenter: Oliver Keszöcze, University of Bremen, DE
Authors: Oliver Keszöcze[1], Jannis Stoppe[2], Robert Wille[3] and Rolf Drechsler[2]
[1]University of Bremen, DE; [2]DFKI and University of Bremen, DE; [3]Johannes Kepler University, AT, DFKI and University of Bremen, DE

CHIMPANC: CHANGE MANAGEMENT USING CHIMPANC
Presenter: Jannis Stoppe, DFKI and University of Bremen, DE
Authors: Jannis Stoppe, Martin Ring and Rolf Drechsler, DFKI and University of Bremen, DE

CLASH: DIGITAL CIRCUITS IN CλASH
Presenter: Christiaan Baaij, University of Twente, NL
Authors: Christiaan Baaij and Jan Kuper, University of Twente, NL

COMPSOC: VIRTUALISING CONTROL APPLICATIONS ON A DISTRIBUTED COMPSOC PLATFORM
Presenter: Kees Goossens, Eindhoven University of Technology, NL
Author: Kees Goossens, Eindhoven University of Technology, NL

CONTINUOUS CHF MONITORING: AN INTEGRATED, LOW-POWER PLATFORM FOR CONTINUOUS CONGESTIVE HEART-FAILURE MONITORING
Presenter: Shahzad Muzaffar, Masdar Institute, AE
Authors: Shahzad Muzaffar, Ibrahim (Abe) M. Elfadel and Jerald Yoo, Masdar Institute, AE

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CONTREP: A SINGLE-SOURCE FRAMEWORK FOR UML-BASED MODELLING AND DESIGN OF MIXED-CRITICALITY SYSTEMS
Presenter: Fernando Herrera, University of Cantabria, ES
Authors: Fernando Herrera and Eugenio Villar, University of Cantabria, ES

COSSIM: A NOVEL, COMPREHENSIBLE, ULTRA-FAST, SECURITY-AWARE CPS SIMULATOR
Presenter: Antonios Nikitakis, Technical University of Crete, GR
Authors: Antonios Nikitakis and Andreas Brokalakis, Technical University of Crete, GR

D-VASIM: TIMING ANALYSIS OF GENETIC LOGIC CIRCUITS USING D-VASIM
Presenter: Hasan Baig, Technical University of Denmark, DK
Authors: Hasan Baig and Jan Madsen, Technical University of Denmark, DK

DAC GENERATOR: A DAC STAGE ANALOG CIRCUIT GENERATOR FOR UDSM AND FD-SOI TECHNOLOGIES
Presenter: Benjamin Prautsch, Fraunhofer Institute for Integrated Circuits IIS, Design Automation Division EAS, DE
Authors: Benjamin Prautsch, Sunil Rao, Uwe Eichler, Ajith Puppala and Torsten Reich, Fraunhofer Institute for Integrated Circuits IIS, Design Automation Division EAS, DE

DIGITALLY DRIVEN TOP-DOWN METHODOLOGY FOR MIXED SIGNAL CIRCUIT DESIGN
Presenter: Markus Mueller, University of Heidelberg, DE
Authors: Markus Mueller, Maximilian Thuermer and Ulrich Bruening, University of Heidelberg, DE

ELECTRO-, STRESS- AND THERMOMIGRATION: THREE FORCES, ONE PROBLEM
Presenter: Steve Bigalke, Technische Universität Dresden, DE
Authors: Steve Bigalke and Jens Lienig, Technische Universität Dresden, DE

ELECTRO-THERMAL SIMULATOR FOR CHIP DESIGN
Presenter: Vladyslav Ladonkin, Reutlingen University, DE
Authors: Vladyslav Ladonkin and Juergen Scheible, Reutlingen University, DE

ETEAK: ASYNCHRONOUS DATAFLOWS SYNTHESIS ONTO FPGAS USING THE ETEAK FRAMEWORK
Presenter: Mahdi Jelodari Mamaghani, The University of Manchester, UK
Authors: Mahdi Jelodari Mamaghani, Jim Garside and Steve Furber, The University of Manchester, UK

EXTRA-FUNCTIONAL PROPERTY SIMULATION WITH VIRTUAL PLATFORMS
Presenter: Ralph Görgen, OFFIS - Intitute for Information Technology, DE
Authors: Ralph Görgen, Kim Grüttner and Sören Schreiner, OFFIS - Intitute for Information Technology, DE

FORMAL VERIFICATION OF CLOCK DOMAIN CROSSING USING GATE-LEVEL MODELS OF METASTABLE FLIP-FLOPS
Presenter: Ghaith Tarawneh, Newcastle University, UK
Authors: Ghaith Tarawneh, Andrey Mokhov and Alex Yakovlev, Newcastle University, UK

GPCDS: AN INTERACTIVE TOOL FOR CREATING SCHEMATIC MODULE GENERATORS IN ANALOG IC DESIGN
Presenter: Matthias Greif, Reutlingen University, DE
Authors: Matthias Greif and Juergen Scheible, Reutlingen University, DE

GRIP: GRAPH-REWRITING-BASED IP-INTEGRATION (GRIP) - AN EDA TOOL FOR SOFTWARE DEFINED SOC DESIGN
Presenter: Munish Jassi, Technische Universität München, DE
Authors: Munish Jassi, Yong Hu, Jian Lyu, Daniel Mueller-Gritschneder and Ulf Schlichtmann, Technische Universität München, DE

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HIGH-END 122GHZ MINIATURE RADAR SENSOR FOR AUTONOMOUS AIRCRAFTS
Presenter: Federico Nava, Heinz Nixdorf Institute - Universität Paderborn, DE
Authors: Federico Nava[1] and Christoph Scheytt[2]
[1]Heinz Nixdorf Institute - Universität Paderborn, DE; [2]Heinz Nixdorf Institute - Paderborn, DE

HYPERDIMENSIONAL COMPUTING FOR TEXT CLASSIFICATION: AN EFFICIENT SOFTWARE IMPLEMENTATION
Presenter: Fateme Rasti Najafabadi, Sharif University of Technology, IR
Authors: Fateme Rasti Najafabadi[1], Abbas Rahimi[2], Pentti Kanerva[2] and Jan Rabaey[2]
[1]Sharif University of Technology, IR; [2]University of California, Berkeley, US

IDDD: AN INTERACTIVE DEPENDABILITY DRIVEN DESIGN SPACE EXPLORATION
Presenter: Stefan Scharoba, Brandenburg University of Technology Cottbus-Senftenberg, DE
Authors: Stefan Scharoba, Jacob Lorenz and Heinrich T. Vierhaus, Brandenburg University of Technology Cottbus-Senftenberg, DE

IN-NODE PROCESSING: MODELLING FRAMEWORK FOR IN-NODE PROCESSING IN INDUSTRIAL SENSOR AND ACTUATOR NETWORKS.
Presenter: Qaiser Anwar, Mid Sweden University, SE
Authors: Qaiser Anwar, Muhammad Imran and Mattias O´Nils, Mid Sweden University, SE

INVADESIM: A SIMULATOR FOR HETEROGENEOUS MULTI-PROCESSOR SYSTEMS-ON-CHIP
Presenter: Sascha Roloff, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Authors: Sascha Roloff, Frank Hannig and Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

LISA: ENABLING LAYERED INTEROPERABILITY FOR INTERNET OF THINGS THROUGH LISA
Presenter: Behailu Shiferaw Negash, University of Turku, FI
Authors: Behailu Shiferaw Negash[1], Amir-Mohammad Rahmani[1], Tomi Westerlund[1], Pasi Liljeberg[1] and Hannu Tenhunen[2]
[1]University of Turku, FI; [2]University of Turku, FI and Royal Institute of Technology (KTH), SE

LLBMC / QPR-VERIFY: HIGH-PRECISION BOUNDED MODEL CHECKING FOR AUTOMOTIVE SOFTWARE
Presenter: Carsten Sinz, Karlsruhe Institute of Technology (KIT), DE
Authors: Carsten Sinz, David Farago, Florian Merz and Reimo Schaupp, Karlsruhe Institute of Technology (KIT), DE

LOOPINVADER: A COMPILER FOR TIGHTLY COUPLED PROCESSOR ARRAYS
Presenter: Alexandru Tanase, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE
Authors: Alexandru Tanase, Michael Witterauf, Ericles Sousa, Vahid Lari, Frank Hannig and Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, DE

MCC: CONTRACT-BASED AUTOMATED INTEGRATION FOR COMPONENT-BASED CRITICAL SYSTEMS
Presenter: Johannes Schlatow, TU Braunschweig, DE
Authors: Johannes Schlatow, Marcus Nolte, Rolf Ernst and Markus Maurer, TU Braunschweig, DE

MICROTESK ARMV8 EDITION: SPECIFICATION-BASED TEST PROGRAM GENERATOR
Presenter: Andrei Tatarnikov, Russian Academy of Sciences (RAS), RU
Authors: Andrei Tatarnikov, Alexander Kamkin and Artem Kotsynyak, Russian Academy of Sciences (RAS), RU

NEURODSP: A MULTI-PURPOSE ENERGY-OPTIMIZED ACCELERATOR FOR NEURAL NETWORKS
Presenter: Jean-Marc PHILIPPE, CEA LIST, FR
Authors: Jean-Marc PHILIPPE, Alexandre CARBON and Renaud SCHMIT, CEA LIST, FR

PFPSIM: A PROGRAMMABLE FORWARDING PLANE SIMULATOR
Presenter: Gordon Bailey, Concordia University, CA
Author: Gordon Bailey, Concordia University, CA

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PSMGEN: AUTOMATIC GENERATION OF POWER STATE MACHINES
Presenter: Alessandro Danese, University of Verona, IT
Authors: Alessandro Danese[1], Graziano Pravadelli[1] and Daniel Lorenz[2]
[1]University of Verona, IT; [2]OFFIS - Institute for Information Technology, DE

Q27: PUTTING QUEENS IN CARRY CHAINS
Presenter: Thomas Preußer, Technische Universität Dresden, DE
Author: Thomas Preußer, Technische Universität Dresden, DE

RC3E: DESIGN AND TEST AUTOMATIZATION IN THE CLOUD
Presenter: Patrick Lehmann, Technische Universität Dresden, DE
Authors: Patrick Lehmann, Oliver Knodel, Martin Zabel and Rainer G. Spallek, Technische Universität Dresden, DE

RESECU_4_AMBRAMS: TOWARDS INCREASED RELIABILITY AND HARDWARE SECURITY USING AMBRAMS
Presenter: Petr Pfeifer, TU Liberec, CZ
Author: Petr Pfeifer, TU Liberec, CZ

RETRASCOPE: TOOLKIT FOR ANALYSIS AND VERIFICATION OF HDL DESIGNS
Presenter: Sergey Smolov, Russian Academy of Sciences (RAS), RU
Authors: Sergey Smolov, Alexander Kamkin and Mikhail Lebedev, Russian Academy of Sciences (RAS), RU

RT-POWMODS: RUN-TIME CPU POWER MODELS FROM REAL DATA
Presenter: Matthew Walker, University of Southampton, UK
Authors: Matthew Walker[1], Stephan Diestelhorst[2], Andreas Hansson[2], Geoff Merrett[1] and Bashir Al-Hashimi[1]
[1]University of Southampton, UK; [2]ARM Ltd., UK

SRAM-BASED PHYSICAL UNCLONABLE KEYS FOR BLE SMART LOCK SYSTEMS
Presenters: Iluminada Baturone and Miguel Ángel Prada-Delgado, University of Seville, ES
Authors: Iluminada Baturone[1], Miguel Ángel Prada-Delgado[1], Alfredo Vázquez-Reyes[1], Laurentiu Acasandrei[2], Diego Fernández-Barrera[2] and Javier Prada-Delgado[2]
[1]University of Seville, ES; [2]OCLOSE S.L., ES

T-RIDE: A MOBILE-HEALTH NEURODIAGNOSTIC SYSTEM BASED ON SPATIO-TEMPORAL P300 MONITORING: DESIGN, DEVELOPMENT AND TEST IN VIVO
Presenter: Valerio Francesco Annese, Politecnico di Bari, IT
Authors: Valerio Francesco Annese, Giovanni Mezzina and Daniela De Venuto, Politecnico di Bari, IT

UCAF TOOL: AN OPTIMIZATION-BASED DESIGN METHODOLOGY FOR ULTRA-LOW VOLTAGE ANALOG INTEGRATED CIRCUITS
Presenter: Lucas Severo, Federal University of Pampa, BR
Authors: Lucas Severo[1] and Wilhelmus Noije[2]
[1]Federal University of Pampa, BR; [2]University of São Paulo, BR

VISUALNOC: VISUALIZATION NETWORK-ON-CHIP DESIGN FRAMEWORK
Presenter: Junshi Wang, Unversity of Electronics Science and Technology of China, CN
Authors: Junshi Wang[1], Letian Huang[1], Guangjun Li[1] and Axel Jantsch[2]
[1]University of Electronics Science and Technology of China, CN; [2]Technology University of Vienna, AT

WORKCRAFT: FRAMEWORK FOR INTERPRETED GRAPHS
Presenter: Danil Sokolov, Newcastle University, UK
Author: Danil Sokolov, Newcastle University, UK

See you at the University Booth!
University Booth Co-Chairs
Jens Lienig, Dresden University of Technology, DE and
Andreas Vörg, edacentrum, DE

FRINGE TECHNICAL MEETINGS

A number of specialist interest groups will be holding their meetings at DATE 2016. The following meetings are scheduled at the moment. A complete list of fringe meetings can also be found on the DATE homepage **www.date-conference.com**

Day+Time	Meeting & Contact	Room
MON 1800-2100	**Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA** Rolf Drechsler, University of Bremen/DFKI, DE drechsle@informatik.uni-bremen.de	Saal 1
TUE 1300-1430	**eTTTC Meeting (European Group of the IEEE Test Technology Technical Council Meeting)** Giorgio Di Natale, LIRMM, FR giorgio.dinatale@lirmm.fr	Seminar 5
TUE 1600-1700	**EDAA General Assembly** Wolfgang Nebel, University of Oldenburg & OFFIS, DE wolfgang.nebel@offis.de	Seminar 2
WED 1200-1500	**Meeting of the IFIP Working Group 10.5** Masahiro Fujita, University of Tokyo, JP fujita@ee.t.u-tokyo.ac.jp	Seminar 5
THU 1400-1530	**DATE Sister-Events Meeting** Luca Fanucci, University of Pisa, IT luca.fanucci@unipi.it	MARITIM Hotel, Miniter-zimmer

MON Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

Saal 1 1800 - 2100

Organiser **Rolf Drechsler,** University of Bremen/DFKI, DE

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2016 Welcome Reception & subsequent PhD Forum, which will take place on Monday, March 14, 2016, from 1800 - 2100 in "Saal 1" of the ICC Dresden. The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

TUE eTTTC Meeting (European Group of the IEEE Test Technology Technical Council Meeting)

Seminar 5 1300 - 1430

Contact person: Giorgio Di Natale, LIRMM, FR

The European Test Technology Technical Council (eTTTC) is the European section of the TTTC. eTTTC is a volunteer professional organization sponsored by the IEEE Computer Society. TTTC's goals are to contribute to our members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the art. This meeting provides all actors involved in test technology to share information on upcoming events and projects.

TUE EDAA General Assembly

Seminar 2 1600 - 1700

General assembly meeting for the members of EDAA, open to everyone interested in Electronic Design Automation.

FRINGE TECHNICAL MEETINGS

WED Meeting of the IFIP Working Group 10.5

Seminar 5 1200 - 1500

The IFIP Working Group 10.5 is an international group of scientists working in the systems design and design automation areas.

THU DATE Sister-Events Meeting

MARITIM Hotel, Restaurant „Ministerzimmer“
1400 - 1530

Meeting of the represenatives from ASP-DAC, ICCAD, DAC and DATE

CO-LOCATED WORKSHOPS

Day+Time	Meeting & Contact	Room
MON 0800-1800	**Xilinx University Program System Design on Zynq using SDSoC** Cathal McCabe, Xilinx, IE cathal.mccabe@xilinx.com	Seminar 1
MON 0900-1700	**FDSOI IP Workshop** Gabrièle Saucier, Design and Reuse, FR gabriele.saucier@design-reuse.com	Seminar 3-5
WED 0830-1230	**MIPSfpga Workshop** Laurence Keung, Imagination Technologies, GB Laurence.Keung@imgtec.com	Seminar 1
THU 0900-1600	**OpenES Project Workshop: System-Level Power and Temperature Specification, Modelling and Analysis** Kim Grüttner, OFFIS - Institute for Information Technology, DE kim.gruettner@offis.de Adam Morawiec, ECSI, FR, Adam.Morawiec@ecsi.org	Seminar 1

MON Xilinx University Program System Design on Zynq using SDSoC

Seminar 1 0800 - 1800

Organiser **Cathal McCabe,** Xilinx, IE

This workshop provides professors with hands-on experience of creating application-specific systems on chip from C/C++ programs using the Xilinx SDSoC development environment and the Digilent Zybo board (Zynq).

The Xilinx SDSoC Development Environment provides an ASSP-like C/C++ programming experience for Zynq platform design. SDSoC includes a full-system optimizing C/C++ compiler, delivering automated software acceleration in programmable logic, automated system connectivity generation, and libraries to accelerate Zynq system designs.

For more information on SDSoC, please see the Xilinx SDSoC webpage:
http://www.xilinx.com/products/design-tools/software-zone/sdsoc.html

This workshop is a condensed 1-day version of the 2-day XUP System Design on Zynq using SDSoC workshop:
http://www.xilinx.com/support/university/vivado/vivado-workshops/Vivado-SDSoC-design-zynq.html

Pre-requisites
- Basic understanding of programmable logic
- Basic C programming experience
- Basic understanding of processor-based system

Vivado, and Zynq design experience is useful, but not essential

You will also need to bring your own laptop with the required software pre-installed. On registration, you will be sent full instructions on the software required and how to install it.

MON FDSOI IP Workshop

Seminar 3-5 0900 - 1700

Organiser **Carlos Mazure,** Soitec, FR
Gerd Teepe, GLOBALFOUNDRIES, DE
Patrick Blouet, STMicroelectronics, FR
Alexandre Valentian, CEA-Leti, FR

Programme Committee Chair **Gabrièle Saucier,** Design and Reuse, FR

The benefits of the FDSOI process have been widely claimed and the design world is eager to take profit of its benefits especially for low power applications (IoT, medical, etc.)

The availability of IP's will be the key ingredient to create a dynamic ecosystem and trigger the market penetration for this attractive innovative process.

Introductive talks will be given by gurus in the field

- Patrick Blouet (ST Microelectronics) and Carlo Mazure (Soitec)
- FD-SOI a New Era for Power Efficiency: Why and How? by Olivier Thomas (Silicon Impulse)
- 22FDX - technology update and design framework developments by Gerd Teepe (GLOBALFOUNDRIES)
- Why and How a next generation FDSOI IP shop by Gabrièle Saucier (Design & Reuse)
- Differentiated IP design in FDSOI by Bipin Malhan (INVECAS)
- "FD-SOI In the Connected World" by Andreas Vielhaber (Synopsys)

Two sessions will present the most innovative IPs on FDSOI including
- IPs in Production, Silicon Proven IPs and Pre-Silicon IPs
- A best price for the most innovative IPs will be delivered and publicized worldwide. Thus will be a good marketing opportunity for letting worldwide know your design skill and product.

WED MIPSfpga Workshop

Seminar 1 0830 - 1230

Organiser **Laurence Keung,** Imagination Technologies, GB

The Imagination University Programme is pleased to announce a deep-dive half-day workshop specifically for teachers and researchers at DATE 2016 based on the new "MIPSfpga" core.

MIPSfpga is the RTL source code of the MIPS microAptiv for implementation on an FPGA. It is a member of the same family found in many embedded devices, including the popular PIC32MZ microcontroller from Microchip and Samsung's new Artik1. MIPSfpga is the real 'industrial' RTL, non-obfuscated, and available freely for academic use. This workshop is part of a global programme of events to enable teachers of Computer Architecture and System-on-Chip design to harness this useful technology.

The Training materials and all instructions will be in English.
- Teaching Computer Architecture using MIPSfpga and the
- Digilent Nexys 4 DDR platform with a Xilinx Artix 7 FPGA

WED Seminar 1 0830 - 1230

0745 **PRE-WORKSHOP SOFTWARE CONFIGURATION CHECKS (OPTIONAL)**

0830 **SESSION 1**

A look inside the MIPS processor and how to synthesize the processor on to an FPGA

Hands-on: Running bare-metal code on MIPSfpga

1015 **COFFEE BREAK**

1035 **SESSION 2**
- Introduction to MIPSfpga SoC and Linux
- Hands-on: Run Linux kernel + Buildroot on MIPSfpga SoC
- Overview of the complete teaching package

1220 **Q&A**

Trainers: **Munir Hasan,** Solutions Engineer at Imagination Technologies
Zubair Lutfullah Kakakhel, Software Engineer at Imagination Technologies
Enrique Sedano, Hardware Design Engineer at Imagination Technologies

TUE Exhibition Theatre 1130 - 1300

1130 **ADDITIONAL SESSION**
- Special Themed Session:

"REVOLUTIONISING THE TEACHING OF COMPUTER ARCHITECTURE AND SYSTEM ON CHIP DESIGN":

This workshop is free of charge for members of academia but places are limited, so please apply for your place quickly.

These workshops are open to academic faculty members, with a priority for those involved directly in teaching.

We reserve the right to accept or refuse registrations based on our desire to enable the broadest spectrum of universities and colleges to participate.

Prior experience of Vivado or Codescape MIPS SDK is useful but not essential.

Note: Please also register as "Exhibition Visitor" for the DATE 2016 Conference for access to the exhibition and Exhibition Theatre sessions. This registration is for free and can be conducted on-site.

Find out about the Imagination University Programme

Robert Owen, Manager, Worldwide University Programme will present at both the workshop and special themed session to discuss your University's interests. For more information or enquiries, please visit our IUP page or the University Forum.

To keep in touch, please register for the Imagination University Programme here.

THU OpenES Project Workshop

Seminar 1 0900 - 1600

Organisers **Kim Grüttner,** OFFIS - Institute for Information Technology, DE
Laurent Maillet-Contoz, STMicroelectronics, FR
Adam Morawiec, ECSI, FR

With the predicted device, core and multicore scaling, a recent study revealed that regardless of chip organization and topology, multicore scaling is power limited. It has been predicted that at 22 nm, 21% of a fixed-size chip must be powered off, and at eight nm, even more than 50%. A system engineer should be able to plan the power intent and break is down to the different hardware resources. With regard to the software, a system engineer should be aware of any possible cross-application interferences with respect to timing, power and thermal properties, as soon as possible in the design flow. Power and temperature management shall be considered in conjunction with the application needs and platform capabilities. For this reason, power and temperature properties need to be modelled and analyzed at the system level, because they can strongly affect the overall quality of service (performance, battery lifetime) or even cause the system to fail meeting its real-time and safety requirements.

In this talk, we present our perspectives on the integration and usage of power and temperature models in SystemC and IP-XACT. This covers the specification of platform properties (extra-functional model) as well as the dynamic capturing, processing, and extraction of power/temperature information during the simulation. In particular, the following topics will be addressed:

Modeling of extra-functional properties (especially power and temperature) in executable system-level models (ESL models)

Estimation techniques to build/generate/annotate ESL models with extra-functional properties and extra-functional property models

Expression of Power Management techniques on ESL

Specification and monitoring of extra-functional properties

Integration with relevant standards to support future interoperability of models: SystemC, IP-XACT

Integration into industrial tools

Planned Program:

0900 **OPENING AND WORKSHOP OVERVIEW**

0915 **OPENES MODELING TOOLKIT**
Laurent Maillet-Contoz (STMicroelectronics, France)
TBA (CEA, France)

1000 **CASE STUDY: FUNCTIONAL AND EXTRA-FUNCTIONAL VERIFICATION FLOW, TEST AND TEST BENCH GENERATION**
Laurent Maillet-Contoz (STMicroelectronics, France)
TBA (NXP, Netherlands)

1030 **COFFEE BREAK & EXHIBITION**

1100 **POWER STATE MACHINES: STATE-BASED SYSTEM-LEVEL POWER ESTIMATION AND MODELLING**
Daniel Lorenz (OFFIS, Germany)

1130 **FROM RTL IP TO FUNCTIONAL SYSTEM-LEVEL MODELS WITH EXTRA-FUNCTIONAL PROPERTIES**
Davide Quaglia (EDALab, Italy)

1200 **IP-XACT EXTENSIONS FOR EXTRA-FUNCTIONAL PROPERTIES**
Emmanuel Vaumorin (Magillem, France)

1230 **LUNCH & EXHIBITION**

1330 **SYSTEM-LEVEL POWER AND TEMPERATURE ESTIMATION**
Sylvian Kaiser (Intel, France)

1400 **TIMED VALUE STREAMS: TRACING, MONITORING AND ANALYSIS OF EXTRA-FUNCTIONAL PROPERTIES IN SYSTEMC**
Kim Grüttner (OFFIS, Germany)

1430 **TIMED VALUE STREAM-BASED POWER AND TEMPERATURE MODEL**
Ralph Görgen (OFFIS, Germany)

1500 **COFFEE BREAK & EXHIBITION**

1530 **DISCUSSION: ENHANCE INTEROPERABILITY OF MODELS AND TOOLS BY UPGRADING AND EXTENDING EXISTING OPEN STANDARDS (SYSTEMC TLM, SYSTEMC-AMS, IP-XACT)**

1600 **CLOSING AND CONCLUDING REMARKS**

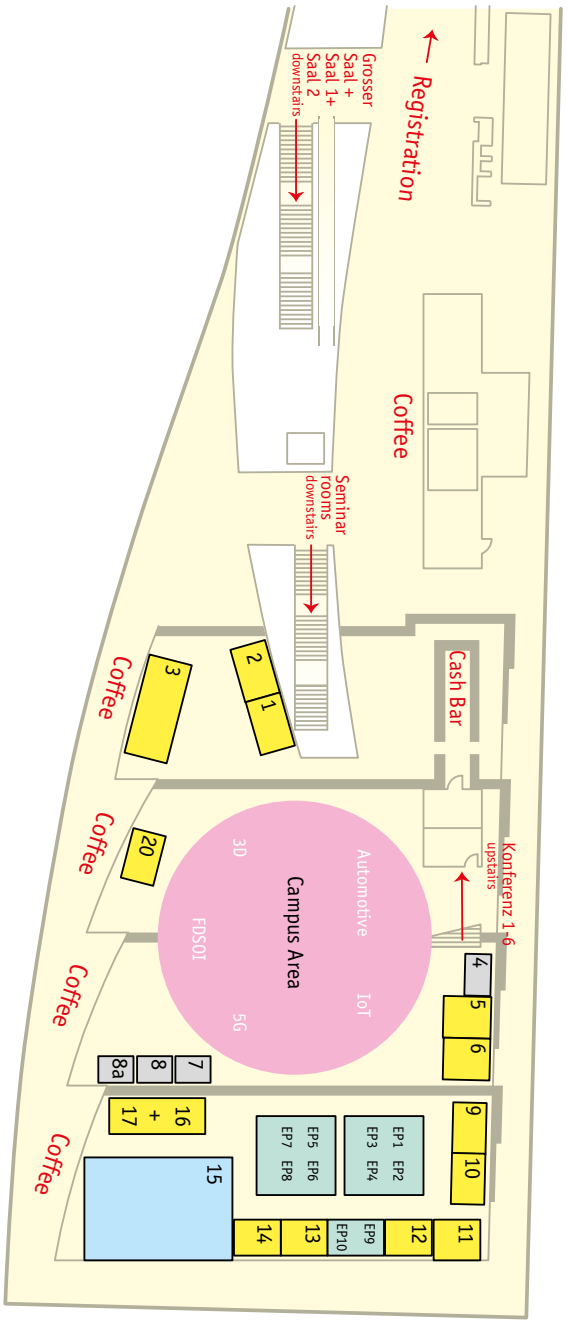
This workshop is supported by the European projects OpenES (http://www.openes-project.org) and CONTREX (https://contrex.offis.de).


EXHIBITION GUIDE

On behalf of the whole Organising Committee, we thank you very much for visiting DATE 2016 and are happy to welcoming you in the unique city of Dresden, Germany!

All commercial sponsors and participating exhibitors are listed with contact details and information about their products and services being presented at the conference. The company profiles will assist you in finding the right solution and/or person to contact.

EXHIBITION FLOOR PLAN



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5G Lab Germany

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Contact: Christian Piechnick

TU Dresden
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Within the 5G Lab Germany, more than 20 professors from TU Dresden collaborate in an interdisciplinary team with approx. 500 scientists and key industrial players to advance research and development on the key technologies for the 5th generation of mobile communications (5G) and its applications. A key feature of 5G will be a short latency that will enable Tactile Internet applications, e.g. networked automated driving, robotic-aided tele-surgery, as well as new learning and trainings methods with special tactile-to-visual feedback. To achieve this goal, the researchers in the 5G Lab Germany are addressing the whole value chain: from semiconductors design technologies and architectures across wireless data transmission, agile networking and mobile edge clouds to Tactile Internet applications.

Advantest Europe GmbH

★ Booth: 4

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A world-class technology company, Advantest is a leading producer of automatic test equipment for the semiconductor industry and a premier manufacturer of measuring instruments used in the design and production of electronic instruments and systems. Our exhibit Cloud Testing Service, Inc., a company offering an alternative to standard test hardware. CTS addresses the challenges facing major chipmakers, R&D engineers, design labs, universities and research institutes to get access to large ATE testers to debug and test their devices. It is specially set up with a flexibly, pay per use model, ideal for R&D.

The main features of CTS include:
- Small and portable personal tester with all signals, features and performance
- Multiple IPs to customize testing needs and simple EDA data migration
- Easy testing through GUI interfaces
- No capital investment in tester hardware

www.cts-advantest.com/en

Also on display is the EVA100 measurement system, enabling easy and rapid characterization, functional evaluation and mass production evaluations of low pin count analog, mixed signal and digital IC devices.

The main features of EVA100 include:
- Small and portable ATE, complete integrated desk top test system
- High performance with transparent module synchronization and high accuracy
- Intuitive GUI tool – Program-less software environment
- Expandable – Stackable testing units architecture and support external instruments

The role of the analog / mixed signal IC has become critically important not only in the smart society but also in other fields. To address these challenges EVA100 measurement system allows users to work in device design evaluation and mass production evaluations in the most efficient environment.

ALTERA Now part of Intel

★ Booth: 1

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Altera® operates as the Programmable Solutions Group (PSG) within Intel Corporation (NASDAQ: INTC), following its acquisition by Intel in 2015. Altera's programmable solutions enable designers of electronic systems to rapidly and cost effectively innovate, differentiate and win in their markets. Altera offers FPGAs, SoCs, CPLDs, and complementary technologies, such as power solutions, to provide high-value solutions to customers worldwide. For more information on Altera, visit www.altera.com. Keywords: FPGA, SOC, Quartus, Cyclone, Stratix, Arria, CPLD, CPU, ARM, A9, MAX.

Bosch Sensortec GmbH

★ Booth: Campus IoT

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Bosch Sensortec GmbH is a fully owned subsidiary of Robert Bosch GmbH dedicated to the world of consumer electronics; offering a complete portfolio of micro-electro-mechanical systems (MEMS) based sensors and solutions that enable mobile devices to feel and sense the world around them. Bosch Sensortec develops and markets a broad portfolio of MEMS sensors, solutions and systems for applications in smart phones, tablets, wearable devices, and various products within the IoT (Internet of Things).

The product portfolio includes a wide range of inertial (acceleration, yaw rate), geomagnetic and environmental sensors (barometric pressure, humidity and gas) as well as the corresponding software portfolio, which is also offered embedded within intelligent sensors. Since its foundation in 2005, Bosch Sensortec has emerged as the technology leader in the addressed markets. The Bosch Group has been the global market leader for MEMS sensors since 1998 selling more than 6 billion MEMS sensors to date.

For more information, go to www.bosch-sensortec.com

Cadence Academic Network

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Cadence Academic Network, X-FAB, Coventor and Reutlingen University teamed up to organize a worldwide MEMS Design Contest. The aim of the contest is to demonstrate a MEMS and mixed-signal design project using state-of-the-art Cadence and Coventor tools in combination with X-FAB's latest MEMS and CMOS design kits. The organizers will provide several workshops to familiarize participants with the design tools and technologies. For further information and registration please visit the website.

Center for Advancing Electronics Dresden (cfaed)

★ Booth: 16+17

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The Cluster of Excellence 'Center for Advancing Electronics Dresden' (cfaed) of Technische Universität Dresden comprises eleven research institutes in Saxony. Further members are the Technische Universität Chemnitz, two Max Planck Institutes, two Fraunhofer Institutes, two Leibniz Institutes and the Helmholtz-Research Center Dresden-Rossendorf. About 300 scientists are working in nine research paths to investigate completely new technologies for electronic information processing. These technologies are inspired by innovative materials such as silicon nanowires, carbon nanotubes or polymers or based on completely new conceptions such as circuit fabrication methods by self-assembling structures, e.g. DNA-Origami. The orchestration of these new devices into heterogeneous information processing systems with focus on their resilience and energy-efficiency is also part of cfaed's research program. To complement the Cluster, the Collaborative Research Center (CRC) 912 'Highly Adaptive Energy-Efficient Computing' (HAEC) has been integrated in cfaed. Both, cfaed and HAEC, are coordinated by Prof. Dr.-Ing. Dr. h.c. Gerhard Fettweis, who holds the Vodafone Chair Mobile Communications Systems at TU Dresden.

ASIC and SOC Design:
- Design Entry
- Behavioural Modelling & Simulation
- Power & Optimisation

System-Level Design:
- Behavioural Modelling & Analysis
- Acceleration & Emulation
- Hardware/Software Co-Design

Embedded Software Development:
- Real Time Operating Systems
- Software/Modelling

Circuits Multi-Projects (CMP)

★ Booth: 6

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Circuits Multi-Projects (CMP) is a manufacturing broker for ICs and MEMS, for prototyping and low volume production. Since 1981, more than 1000 Institutions from 70 countries have been served, more than 6700 projects have been prototyped through 800 manufacturing runs, and 60 different technologies have been interfaced. Integrated Circuits are available on CMOS, SiGe BiCMOS, HV-CMOS, CMOS-Opto from STMicroelectronics and ams down to 28 nm FDSOI, 3D-IC from TEZZARON/GLOBALFOUNDRIES. MEMS are available on various processes: specific MEMS technologies (PolyMUMPS, SOIMUMPS, PiezoMUMPS, MetalMUMPS from MEMSCAP), MIDIS from TELEDYNE DALSA and bulk micromachining from ams. Design kits for most IC CAD tools and Engineering kits for MEMS are available. Assembling is provided in a wide range of plastic and ce-

ramic packages.

ASIC and SOC Design:
– MEMS Design

Services:
– Prototyping
– Foundry & Manufacturing

City of Dresden, Office of Economic Development ★ Booth: 18

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Network Thinking - Microelectronics in Dresden
- Competencies: Research & Development, IC Design, Photomasks, Chip Manufacturing, Packaging, Equipment, Software
- The Economic Development Office of the City of Dresden is your contact and partner as enterpreneur or investor. Our service ensures that your investment in Dresden can be realized without delay.

Welcome to Dresden!

Concept Engineering GmbH ★ Booth: 8

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Concept Engineering develops and markets innovative visualization and debugging technology for commercial EDA vendors, in-house CAD tool developers, SoC and IC/FPGA designers.

Nlview Widgets™ – a family of schematic generation and visualization engines that can be easily integrated into EDA tools.

S-Engine™ - automatic system-level schematic generation capabilities combined with IP editing and SoC assembly features.

T-Engine™ - a visualization engine for transistor-level EDA tools.

StarVision® PRO - a mixed-signal and mixed-language debugger with extensive support for post-layout debugging and customizable netlist pruning.

RTLVision® PRO – a graphical debugger for SystemVerilog, Verilog and VHDL based designs.

SpiceVision® PRO – a customizable debugger for SPICE based designs.

GateVision® PRO – a customizable debugger for Verilog, LEF/DEF and EDIF based designs.

ASIC and SOC Design:
– Verification
– Analogue and Mixed-Signal Design
– MEMS Design
– RF Design

Test:
– Design for Test

CONTREX - Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties ★ Booth: EP 1

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Up to now, mission- and safety critical services of Systems of Systems have been running on dedicated and either custom designed HW/SW platforms or "legacy" COTS. In the near future, such systems will be accessible, connected with or executed on devices comprising state-of-the-art off-the-shelf MPSoCs. Significant improvements have been achieved supporting the design of mixed-critical systems by developing predictable computing platforms and mechanisms for segregation between applications of different criticalities sharing computing resources. Such platforms enable techniques for the compositional certification of applications' correctness, run-time properties and reliability.
The CONTREX project complements these important activities with an analysis and segregation along the extra-functional properties real-time, power, temperature and reliability. These properties will be major cost roadblocks when 1) scaling up the number of applications per platform and the number of cores per chip, 2) in battery-powered devices or 3) switching to smaller technology nodes.
CONTREX enables energy efficient and cost aware design through analysis and optimization of real-time, power, temperature and reliability with regard to application demands at different criticality levels.
The project focuses on extra-functional requirements derived from the automotive telematics, aeronautics and telecommunications domain.
Our economic goal is to improve energy efficiency by 20 % and to reduce cost per system by 30 % due to a more efficient use of the computing platform.

COSEDA Technologies ★ Booth: 12

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COSEDA Technologies provides software solutions in the field of system level design for complex electronic hard- & software products. We make latest modelling and simulation technologies available for our customers to enable them to master new concepts cost-effectively for innovative, completive and safety-critical products. COSEDA Technologies is a spin-off, founded in June 2015 from the Fraunhofer Institute for Integrated Circuits IIS, Design Automation Division EAS Dresden.

Our technologies have an over 15 year's history and are being used by leading European semiconductor companies, which develop circuits for automotive, communication, power, security critical (e.g. smart cards) and safety-critical applications. The founders of the company are experts, which were involved in the development and standardization (IEEE & Accellera) of the SystemC AMS modelling and simulation technology which is the basis for our main product COSIDE®.

COSIDE® is the first tool which permits the design of electronic hard- & software components in the context of the whole system. It is easy to adapt and enables a cross-domain optimization of the system concept & architecture and thus the design of next generation products. COSIDE® is intuitive to use for experienced soft- and hardware designers, while reducing the effort for modelling and simulation. We provide the reference implementation for the SystemC AMS part of the standard. On top of this standard we developed models, libraries and IP's, which are integrated within our design environment COSIDE®.

ASIC and SOC Design:
– Behavioural Modelling & Simulation
– Verification
– Analogue and Mixed-Signal Design
– RF Design

System-Level Design:
– Behavioural Modelling & Analysis
– Hardware/Software Co-Design

– Services:
– Training
– Embedded Software Development:
– Software/Modelling

Design & Reuse ★ Booth: 13

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Design & Reuse (D&R) was founded in 1997, the same year it launched its unique and renowned IP web portal, www.design-reuse.com. D&R has extended its scope with 2 new sites, one for connecting system designers with vendors of subsystems, platforms, middleware www.dr-embedded.com, and one in Mandarin language dedicated to Chinese audience www.design-reuse.cn
D&R continues to maintain its focus on streamlining IP-based design with its Enterprise IP Management System (IPMS) offering, a next generation configurable Enterprise Java based platform offering the most innovative solution for internal and external IP management from design to reuse, to IP tracing in products and Delivery etc.
It includes unique powerful procurement features for external IPs (Finance reporting, Fee and royalty calculation). Recently, the platform has been extended to software license management. It incorporates a license monitoring Front End aiming at reducing License cost and offers powerful corporate financial reporting capabilities.

DREAMS - Distributed Real-time Architecture for Mixed Criticality Systems ★ Booth: EP 1

Contact: Roman Obermaisser

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The objective of DREAMS is to develop a cross-domain architecture and design tools for networked complex systems where ap-

plication subsystems of different criticality, executing on networked multi-core chips, are supported. DREAMS will deliver architectural concepts, meta-models, virtualization technologies, model-driven development methods, tools, adaptation strategies and validation, verification and certification methods for the seamless integration of mixed-criticality to establish security, safety, real-time performance as well as data, energy and system integrity.

European Mixed-Criticality Cluster (MCC) ★ Booth: EP 1

Contact: The contact persons of the projects CONTREX, DREAMS and PROXIMA

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Website: www.mixedcriticalityforum.org

The EU FP7 projects CONTREX, DREAMS and PROXIMA collaborate in an European Mixed-Criticality Cluster (MCC) and closely work together in terms of identification of future challenges in the design and development of mixed-criticality multicore systems, join dissemination activities activities, and where possible exploring techniques to attach those challenges.

EUROPRACTICE ★ Booth: 5

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The EUROPRACTICE Service offers CAD tools for education, low cost and easy access to ASIC prototype and small volume fabrication. The service is offered by IMEC (B), STFC (UK) and Fraunhofer IIS (D). Low cost prototyping is achieved by offering fabrication through regularly scheduled MPW runs whereby many designs are merged onto the same fabrication run. These runs are fabricated in industrial CMOS, BiCMOS and SiGe processes from 0.7µ to 40nm at well-known foundries (ONSemi, austiamicrosystems, IHP, LFoundry, TSMC, UMC). A total integrated design and manufacturing flow is offered including cell library and design kit access and support, deep submicron netlist-to-layout, ASIC prototyping on MPW or dedicated single project prototype runs, volume fabrication, qualification, assembly and test. Volume fabrication starts with wafer batches as low as 12 wafers but can go up to more than 5000 wafers per year per ASIC.

Test:
- Design for Test
- Design for Manufacture and Yield
- Boundary Scan
- Silicon Validation
- Mixed-Signal Test
- System Test

Services:
- Prototyping

Semiconductor IP:
- Analogue & Mixed Signal IP
- Physical Libraries

EuroSERVER – Green Computing Node for European Micro-servers ★ Booth: EP 5

Contact: Isabelle Dor

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Data-centres form the central brains and store for the Information Society and are a key resource for innovation and leadership. The key challenge has recently moved from just delivering the required performance, to include consuming reduced energy and lowering cost of ownership. Together, these create an inflection point that provides a big opportunity for Europe, which holds a leading position in energy efficient computing and market prominent positions in embedded systems.
EUROSERVER is an ambitious and holistic project aimed to arm Europe with leading technology for conquering the new markets of cloud computing:
1. Capitalise on the European strength in embedded and low power computing to provide an innovative combined architecture-and-technology integration platform that enables the reuse of highly-integrated, high-performance, energy-efficient component subsystems in a micro-server solution suitable across both cloud data-centres and embedded application workload.
2. Perform a combined architecture-technology exploration that creates the hardware and the software for micro-server based computing in support of cloud-based and embedded applications.
3. Evidence this architecture in a data-centre grade low-power physical micro-server prototype solution utilizing advanced ARM IP, industry leading FD-SOI fabrication technology, and state of the art 2.5D device integration technologies and prove the advantages of these European technologies as the enabler of next generation,low-cost, power-efficient, high-density compute.
The EUROSERVER consortium brings together world-class leaders in their own fields and creates the critical-mass required to deliver "More than Moore" solutions. A unique differentiator of EUROSERVER is its broad access to the required industrial technologies and specialised academic support. The potential impact of EUROSERVER is therefore very high to competitively accelerate and improve the delivery of energy-efficient computing worldwide.

OBJECTIVES
EUROSERVER will design and prototype technology, architecture, and systems software for the next generation of "Micro-Servers" to be used in building datacenters. We will progress on the current state of the art in the following domains:

- Reduced Energy consumption
- Reduced Cost to build and operate each microserver,
- Better Software efficiency

ExaNoDe – European Exascale Processor Memory Node Design ★ Booth: EP 6

Contact: Denis Dutoit

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ExaNoDe is a collaborative European project within the "Horizon 2020 Framework Programme", that investigates, develops and designs a highly efficient, highly integrated, high-performance, heterogeneous compute element enabling exascale computing and demonstrated using hardware-emulated interconnect. It is addressing these important challenges through the coordinated application of several innovative solutions recently deployed by European initiatives for scalable computing: ARM-v8 low-power processors for energy efficiency, 3D interposer integration for compute density and UNIMEM advanced memory scheme for low-latency, high-bandwidth memory access, scalable to Exabyte levels.

The ExaNoDe compute element aims towards exascale compute goals through:
- Integration of low-power processors and accelerators across scalar, SIMD, GPGPU and FPGA processing elements in the deployment of associated 3D integration technologies and in the mechanical requirements to enable the development of a high-density, high-performance integrated compute element with advanced thermal characteristics and connectivity to the next generation of system interconnect and storage;
- Undertaking essential research to ensure the ExaNoDe compute element provides necessary support of HPC applications including I/O and storage virtualization techniques, operating system and semantically aware runtime capabilities and PGAS, OpenMP and MPI paradigms;
- The development of an instantiation of a hardware emulation of interconnect to enable the evaluation of UNIMEM for the deployment of multiple compute elements and the evaluation, tuning and analysis of HPC mini-apps.

Fast Tracker for Hadron Collider Experiments ★ Booth: EP 9

Contact: International coordinator: Prof. Mauro Dell'Orso, University of Pisa, IT | Contact person: Calliope-Louisa Sotiropoulou

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We develop an extremely fast but compact processor, with supercomputer performances, for pattern recognition, data reduction, and information extraction in high quality image processing.
The proposed hardware prototype features flexibility for potential applications in a wide range of fields, from triggering in high energy physics to simulating human brain functions in experimental psychology or to automating diagnosis by imaging in medical physics. In general, any artificial intelligence process based on massive pattern recognition could largely profit from our device, provided data are suitably prepared and formatted.
The first goal consists in demonstrating the system can perform online track reconstruction of full events at the highest luminosities of the LHC and SLHC) at CERN, beyond the limits of any existent or planned device and despite the overwhelming confusion due to the very high track multiplicity. We participate to the construction and the test for a high precision real-time tracker built for the ATLAS experiment: the Fast Track (FTK) processor to improve the capability of the ATLAS detector to select interesting events within the enormous LHC background. It uses FPGA and ASIC chips to implement, real-time, complex track reconstruction algorithms. The track's trajectories are reconstructed in 3D, in few dozens of microseconds and the quality of the parameters is almost offline. FTK will increase the ATLAS discovery capability.
In parallel we will pursue challenging R&D & new real time computing ideas for more complex applications.

FRACTAL TECHNOLOGIES

★ Booth: 9

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Los Gatos, California, United States
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Eindhoven, The Netherlands

Tel: +1 4089155250

E-Mail: info@fract-tech.com
Website: www.fract-tech.com

State of the art validation tools for Standard cell library, IO and hard IP.
The scope of Fractal Technologies products is to check consistency and validate all different data formats used in designs and subsequently improve the Quality of Standard Cell Libraries, IO libraries and general purpose IP blocks (Digital, Mixed Signal, Analog and Memories). Fractal Technologies offers Crossfire software as well as services and customisation.
Our mission is simple: make the Quality of your Design Formats an asset for your business.

ASIC and SOC Design:
- Design Entry
- Verification

Services:
- Design Consultancy

Fraunhofer Institute for Integrated Circuits IIS

★ Booth: Campus IoT

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The Fraunhofer Institute for Integrated Circuits IIS is one of the world's leading application-oriented research institutions for microelectronic and IT system solutions and services. With the creation of mp3 and the co-development of AAC, the institute has reached worldwide recognition.

Since more than 15 years, our scientist are working already on enabling technologies for the Internet of Things as identification mechanisms (RFID), wireless sensor systems and cyber physical systems. With this comprehensive expertise, we call upon a sophisticated platform for developing innovative and customer-specific IoT-solutions as well as for putting them into practice. Hereby, our test and application center L.I.N.K. provides the ideal combination of technological environment and true-to-life, application-oriented test conditions for the development of novel technologies and services.

Our tools and service are ranging from consulting over the development of intelligent algorithms up to the implementation of hard- and software components. Hereby, MIOTY (miniaturized wireless IoT platform), s-net® (adaptable multi-hop wireless technology), awiloc ® (positioning technology) as well as BlackFIR® (angle-of-arrival measurement) represent only a small selection of our solutions available.

ASIC and SOC Design:
- Verification
- Analogue and Mixed-Signal Design
- RF Design

System-Level Design:
- Behavioural Modelling & Analysis
- Hardware/Software Co-Design
- Package Design

Services:
- Design Consultancy
- Prototyping
- Foundry & Manufacturing
- Training

Semiconductor IP:
- Analogue & Mixed Signal IP

Application-Specific IP:
- Analogue & Mixed Signal IP
- Data Communication
- Digital Signal Processing
- Networking
- Telecommunication
- Wireless Communication

GLOBALFOUNDRIES

★ Booth: Campus FDSOI

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GLOBALFOUNDRIES is the world's first full-service semiconductor foundry with a truly global footprint. Launched in March 2009, the company has quickly achieved scale as one of the largest foundries in the world, providing a unique combination of advanced technology and manufacturing to more than 250 customers. With operations in Singapore, Germany and the United States, GLOBALFOUNDRIES is the only foundry that offers the flexibility and security of manufacturing centers spanning three continents. The company's 300mm fabs and five 200mm fabs provide the full range of process technologies from mainstream to the leading edge. This global manufacturing footprint is supported by major facilities for research, development and design enablement located near hubs of semiconductor activity in the United States, Europe and Asia. GLOBALFOUNDRIES is owned by Mubadala Development Company. For more information, visit http://www.globalfoundries.com.

High Performance Center Functional Integration in Micro- and Nanoelectronics

★ Booth: Campus 3D

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In Dresden Germany, the European hot spot of microelectronics, a new network of research organizations and the industry has been established.
Core research partners are the Technical University Dresden, the Technical University Chemnitz, the University of Applied Sciences Dresden and the Fraunhofer Institutes IPMS, ENAS, IIS-EAS and IZM-ASSID.
They started a program for development of new microelectronics components. In a cooperation network they combine system design and modelling, innovative materials for new components and processes with heterogeneous system integration and reliability characterization.
Piezo electronic materials, magnetic layer structures, nano optical layers and Li based thin on chip layers for energy storage are part of the program.
The partners offer their joint developments and capabilities for industrial partner to establish collaboration programs.

Partners:
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  Fax: +49 371 45001 101
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ASIC and SOC Design:
- Design Entry
- Behavioural Modelling & Simulation
- Physical Analysis (Timing, Themal, Signal)
- Analogue and Mixed-Signal Design
- System-Level Design:
- Behavioural Modelling & Analysis
- Physical Analysis
- Package Design

Test:
- Design for Test
- Design for Manufacture and Yield
- Silicon Validation
- Mixed-Signal Test
- System Test

Services:
- Design Consultancy
- Prototyping
- Foundry & Manufacturing

Embedded Software Development:
- Software/Modelling

Semiconductor IP:
- Analogue & Mixed Signal IP
- Embedded Software IP
- Physical Libraries
- Synthesizable Libraries

Application-Specific IP:
- Analogue & Mixed Signal IP

HiPEAC - European Network on High Performance and Embedded Architecture and Compilation

★ Booth: 10

Contact: Vicky Wandels

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HiPEAC is the largest and fastest growing membership network for High Performance

Computing (HPC) and Embedded Computing professionals in Europe. Becoming a HiPEAC industry member indicates a commitment to learning, growing and personal and business success. All our membership benefits are aimed at providing members with a wealth of exclusive resources. HiPEAC membership is also a two-way street. It's not just about consuming, but also contributing – not just to the organisation, but more importantly to other members and the HPC and Embedded Computing industry as a whole. Our members drive our work through their participation at events and sharing of best practices and more. We draw on our members' expertise and experiences to shape our services. Each and every member brings something different to the table and it's those unique characteristics that make HiPEAC strong. HiPEAC membership is invaluable. Our vendor-neutral position, coupled with our communities targeted to specific market segments, allow us to create customised services – a huge benefit to our members and organisations like your own. Joining as a HiPEAC industry member, helps you and your business grow through timely industry insight, training, recruitment and peer-to-peer interaction. Get guidance from industry experts and attend our events and discuss business opportunities and challenges. Meet EU policy makers and help to shape the HiPEAC Vision, the definitive guide for EU policy makers on future technology action areas. To join for free email membership@hipeac.net quoting "HIDATE16". For further information visit www.hipeac.net/industry and don't forget to visit our stand (booth no. 10) here at DATE 2016!

IDT/ZMDI

★ Booth: Campus IoT

Contact: Hans-Juergen Brand

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Zentrum Mikroelektronik Dresden AG (ZMDI) is a Dresden, Germany-based, automotive certified company which was recently acquired by Integrated Device Technology, Inc. (IDT), and operates today as the IDT Automotive and Industrial business unit within IDT's world-wide operations. IDT is a global supplier of analog and mixed-signal semiconductor solutions for communications, computing, consumer devices, automotive and industrial applications, including market-leading product families in timing, wireless power transfer and charging, sensors and sensor signal conditioning, high-performance serial data interconnect and switching, and memory system interfaces. ZMDI is the IDT center of excellence focused on solutions for the automotive, industrial, medical, mobile sensing markets. ZMDI develops and markets application-specific integrated circuits (ASICs) and application-specific standard products (ASSPs), which can withstand high temperatures and voltages and consume very little power. Due to its extensive experience in circuit development, ZMDI is capable to offer ICs for very demanding applications, in some cases operating at temperatures up to +160 ° C and with voltages from 0.85 to 40 volts. ZMDI has been headquartered and operating in Dresden Germany for over 50-years, and in late 2015 joined IDT which has been operating for over 35 years, headquartered in San Jose, CA. The combined company has approximately 1700 employees, and serves its customers with sales offices and design centers throughout Europe (Bulgaria, Finland, France, Germany, Italy, Netherlands, Sweden, United Kingdom), Asia (China, Japan, Korea, Malaysia, Singapore, Taiwan), and North America (United States, Canada).

ASIC and SOC Design:
- Design Entry
- Behavioural Modelling & Simulation
- Synthesis
- Power & Optimisation
- Physical Analysis (Timing, Themal, Signal)
- Verification
- Analogue and Mixed-Signal Design
- RF Design

System-Level Design:
- Behavioural Modelling & Analysis
- Physical Analysis
- Hardware/Software Co-Design
- PCB & MCM Design

Test:
- Design for Test
- Design for Manufacture and Yield
- Logic Analysis
- Test Automation (ATPG, BIST)
- Boundary Scan
- Silicon Validation
- Mixed-Signal Test
- System Test

Embedded Software Development:
- Compilers
- Real Time Operating Systems
- Debuggers
- Software/Modelling

Hardware:
- FPGA & Reconfigurable Platforms
- Development Boards

IMAGINATION TECHNOLOGIES

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About Imagination Technologies
Imagination is a global technology leader whose products touch the lives of billions of people across the globe. The company's broad range of silicon IP (intellectual property) includes the key processing blocks needed to create the SoCs (Systems on Chips) that power mobile, consumers and embedded electronics. Its unique software IP, infrastructure technologies and system solutions enable its customers to get to market quickly with complete and highly differentiated SoC platforms. Imagination's licensees include most of the world's leading semiconductor manufacturers, network operators and OEMs/ODMs who are creating some of the world's most iconic products. See: www.imgtec.com

About the Imagination University Programme
The Imagination University Programme (IUP) has commissioned excellent teaching materials from leading academics to enable our technologies to be used in university courses and student projects around the world. We are committed to produce these materials in multiple languages and support them globally. We also organise workshops, including this week at DATE, which empowers teachers to quickly put these materials to use. Teaching packages include MIPSfpga for Computer Architecture and SoC, the Connected MCU Lab for embedded control, and Mobile Graphics:

- MIPSfpga is a revolutionary project: a real MIPS RTL core, open for academics to use freely with their students, fully verified, and not obfuscated.
- The Connected MCU Lab is a starter course for under-graduates using microcontrollers for the first time. It's an ideal way to upgrade old 8051 8 bit or MSP430 16 bit labs to the new IoT-connected world that requires 32 bit processors.

More details at our intelligent website: www.community.imgtec.com/university

System-Level Design:
- Hardware/Software Co-Design

Services:
- Training

Hardware:
- FPGA & Reconfigurable Platforms

Semiconductor IP:
- CPUs & Controllers

Application-Specific IP:
- Multimedia Graphics

IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH

★ Booth: Campus IoT

Contact: Tino Hutschenreuther

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IMMS serves small and medium-sized industrial enterprises through preliminary research. It acts as their strategic partner in the development of microelectronic and mechatronic products and of systems technology. With its solutions, the institute connects information technology to the real world. For its partners, IMMS is the cutting edge, slicing through the barriers between research results and manufacturing. The institute is thus a veritable bridge between science and industry.
Our activities are driven by the need for technological contributions to help meet societal challenges like the protection of the environment, the efficient use of energy and resources, and the preservation of health and safety in public, private and industrial spheres.
As cyber-physical systems as the basis of the "Internet of Things and Services" will contain a huge number of components and will be massively distributed, energy- and resource-efficiency of those systems are of great significance. Our research therefore focuses on the development of highly energy-efficient microelectronic and embedded systems for the acquisition, processing and communication of measurement and control data. For this purpose, we investigate and create hardware and software solutions for wired and wireless sensor and actuator networks, particularly regarding aspects such as communication protocols, real-time capability, and energy-autonomous operation.
Furthermore, we focus our research activities on technology for the development and the integration of micro-electro-mechanical systems (MEMS), sensor systems for biological analysis and medical technology, and electromagnetic direct drives with nanometer precision.

ASIC and SOC Design:
- Design Entry
- Behavioural Modelling & Simulation
- Synthesis
- Verification
- Analogue and Mixed-Signal Design
- MEMS Design
- RF Design

System-Level Design:
- Behavioural Modelling & Analysis
- Acceleration & Emulation
- Hardware/Software Co-Design
- PCB & MCM Design

Test:
- Design for Test
- Design for Manufacture and Yield
- Test Automation (ATPG, BIST)
- Mixed-Signal Test
- System Test

Services:
- Design Consultancy
- Prototyping
- Training

Hardware:
- FPGA & Reconfigurable Platforms

Semiconductor IP:
- Analogue & Mixed Signal IP

INCHRON GmbH

★ Booth: Campus Automotive

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INCHRON is the worldwide leading provider of solutions for the design and test of embedded systems and networks, with a focus on performance, event chain analysis and real-time behavior. Since 2003 the company has gained a worldwide customers base in different industries and domains. In more than 12 years INCHRON has proven to be a trustworthy partner for all of its customers. In more than 150 cost and time critical development projects INCHRON has actively helped to steer them to success. The company's philosophy is to support customers with worldwide unique know-how and excellent tools to guarantee an excellent Real-Time Health of their embedded system. For details please go to www.inchron.com. To find out about the Real-Time Health of your embedded system, please visit: www.real-time-doctors.com/

System-Level Design:
- Behavioural Modelling & Analysis

Infineon Technologies AG

★ Booth: Campus IoT

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Infineon Technologies AG is a world leader in semiconductor solutions that make life easier, safer and greener. Microelectronics from Infineon is the key to a better future. In the 2015 fiscal year (ending September 30), the company reported sales of about Euro 5.8 billion with some 35,400 employees worldwide.
Infineon - Partner of choice for IoT security
The IoT is built on many different semiconductor technologies, including power management devices, sensors and microprocessors. Performance and security requirements vary considerably from one application to another. One thing is constant, however. And that is the fact that the success of smart homes, connected cars and Industrie 4.0 factories hinges on user confidence in robust, easy-to-use, fail-safe security capabilities. The greater the volume of sensitive data we transfer over the IoT, the greater the risk of data and identity theft, device manipulation, data falsification, IP theft and even server/network manipulation. Infineon has developed a broad range of easy-to-deploy semiconductor technologies to counter growing security threats in the IoT. These solutions enable system and device manufacturers as well as service providers to capitalize on growth opportunities by integrating the right level of security without compromising on the user experience. Complemented by software and supporting services, our hardware-based products create an anchor of trust for security implementations, supporting device integrity checks, authentication and secure key management.

INTENTO DESIGN

★ Booth: 14

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Intento Design provide responsive technology for analog IP. The company was born from 25 years of research aimed at developing a new analog design methodology . This research resulted in an extensive portfolio of intellectual property, including an innovative EDA tool that accelerates the design cycle by automating the sizing and migration of analog and mixed-signal circuitry used in complex SoCs for a variety of connected applications.
The Intento Design methodology solves the productivity gap inherent in the analog design process by reducing lengthy simulation iterations. Traditionally, analog and mixed-signal design requires the engineer to compute initial circuit dimensions from hand analysis using first order transistor models followed by successive simulations.
This tedious and time-consuming process can take weeks for a complex circuit. Intento accelerates this process with software that plugs into the existing design flows and standard tools, and automates the circuit sizing, thereby allowing designers to move on to layout, placement and routing in a fraction of the time.
The Intento Design methodology keeps the designer at the centre of the process, specifying the parameters that must be met by the circuit; reviewing the options based on desired power consumption, performance and surface area; and selecting the optimal solution.

MAGILLEM

★ Booth: 20

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Magillem is a Leading Provider of Complex Design Flow and Content Management Software Solutions.
Magillem has developed an easy-to-use, state of the art platform to cover electronic systems design flow challenges in a context where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SoC.
Magillem integrated design environment offers a non-disruptive framework, a backbone to the design flow, providing fluidity, flexibility, seamless execution of the entire flow and better control to designers.
Thanks to early focus on XML, the company has quickly become a specialist of design and content automation, offering a multi-industry and cross-disciplinary approach to its clients.
Magillem's innovative technology now enables the integration of specification, design and documentation into a unique process.

ASIC and SOC Design:
- Design Entry
- Analogue and Mixed-Signal Design

System-Level Design:
- Hardware/Software Co-Design

MANGO: Exploring Manycore Architectures for Next Generation HPC Systems

★ Booth: EP 10

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The performance/power efficiency wall poses the major challenge faced nowadays by HPC. Looking straight at the heart of the problem, the hurdle to the full exploitation of today computing technologies ultimately lies in the gap between the applications' demand and the underlying computing architecture: the closer the computing system matches the structure of the application, the most efficiently the available computing power is exploited. Consequently, enabling a deeper customization of architectures to applications is the main pathway towards computation power efficiency.
The MANGO project will build on this consideration and will set inherent architecture-level support for application-based customization as one of its underlying pillars. In addition to mere performanceand power-efficiency, it is of paramount importance to meet new nonfunctional requirements posed by emerging classes of applications. In particular, a growing number of HPC applications demand some form of time- predictability, or more generally Quality-of-Service (QoS), particularly in those scenarios where correctness depends on both performance and timing requirements and the failure to meet either of them is critical. Examples of such time-critical application include:

- online video transcoding
- the server-side on-the-fly conversion of video contents, which involves very computation-intensive operations on huge amounts of data to be performed within near real-time deadlines.
- medical imaging
- characterized by both stringent low-latency requirements and massive computational demand.

Time predictability and QoS, unfortunately, are a relatively unexplored area in HPC. While traditional HPC systems are based on a "the faster, the better" principle, real-timeness is a feature typically found in systems used for mission-critical applications, where timing constraints usually prevail over performance requirements. In such scenarios, the most straightforward way of ensuring isolation and time-predictability is through resource overprovisioning, which is in striking contrast to power/performance optimization.

MathWorks — Sponsor

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MathWorks is the leading developer of mathematical computing software. Engineers and scientists worldwide rely on its products to accelerate the pace of discovery, innovation, and development.
MATLAB®, the language of technical computing, is a programming environment for algorithm development, data analysis, visualization, and numeric computation. Simulink® is a graphical environment for simulation and Model-Based Design of multidomain dynamic and embedded systems. The company produces nearly 100 additional products for specialized tasks such as data analysis and image processing.
MATLAB and Simulink are used throughout the automotive, aerospace, communications, electronics, and industrial automation industries as fundamental tools for research and development. They are also used for modeling and simulation in increasingly technical fields, such as financial services and computational biology. MATLAB and Simulink enable the design and development of a wide range of advanced products, including automotive systems, aerospace flight control and avionics, telecommunications and other electronics equipment, industrial machinery, and medical devices. More than 5000 colleges and universities around the world use MATLAB and Simulink for teaching and research in a broad range of technical disciplines.

ASIC and SOC Design:
- Behavioural Modelling & Simulation
- Verification
- Analogue and Mixed-Signal Design
- RF Design

System-Level Design:
- Behavioural Modelling & Analysis
- Hardware/Software Co-Design

Test:
- System Test

Services:
- Design Consultancy
- Training

Mentor Graphics — ★ Booth: Campus FDSOI, Sponsor

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Mentor Graphics is a technology leader in electronic design automation, providing products, consulting services and award-winning support for the world's most successful electronics and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months in excess of $1.24 billion in the last fiscal year. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777. World Wide Web site: http://www.mentor.com/. We offer the broadest industry portfolio of best-in-class hardware and software design solutions focused on IC design and physical verification, functional verification, FPGA/PLD, design-for-test,PCB design embedded software and automotive EE design. Mentor Graphics innovative tools help our customers solve current and future design challenges, including scalable solutions for functional verification, cutting-edge technology for design-for-manufacturability and mixed-level IC design verification, award-winning test compression technology, embedded software development systems, and market-leading integrated system design solutions.

ASIC and SOC Design:
- Design Entry
- Functional Verification
- IC Design & Manufacturing
- Analogue and Mixed-Signal Design

System-Level Design:
- Acceleration & Emulation
- PCB & MCM Design & Manufacturing
- Automotive EE design
- Mechanical analysis

Test:
- Silicon test & yield analysis

Embedded Software Development:
- Compilers
- Real Time Operating Systems
- Multicore Framework

Microtest – Microelectronics Global Solutions — ★ Booth: 2

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Microtest, combining innovation, continuous improvement, and sustainability, is a reliable global supplier and partner for companies seeking advanced electronic and microelectronic solutions for various applications.
After its conception in 1998 strictly as a test house, Microtest began designing and manufacturing its own extensions to existing Automatic Test Equipment and solutions, increasing their performance and capability, to meet the ever-increasing testing needs of complex automotive devices.
This gave Microtest the necessary experience to begin producing its own lines of small-footprint, low-consumption, lowcost, high-parallelism ATE for bench investigation and mass production: the Hatina platform, and Hatina Workstation (WS) platform. The most versatile of these testers is the DMT (Digital Mixed-Signal Tester), particularly suited for lab environments thanks to its low weight and size. With a powerful software suite of graphical programming available (plus the traditional low-level coding option), the DMT allows one to write a full characterization test program in days, reducing time to market and cost.
Microtest's Microelectronic Design team boasts an impressive portfolio of delivered devices including analog, digital, mixed signal, high/low voltage application using BCD technology, while the company also continues its activity as test house for devices spanning the Automotive, Space, Military, Medical, Consumer, Radio Frequency, Electronic Security, and Telecommunications-sectors: with the expertise and technical knowhow accumulated over the years, Microtest now provides turn-key solutions going from the electrical specification to mass production: design, layout, assembly, test, firmware and software development phases.

ASIC and SOC Design:
- Design Entry
- Behavioural Modelling & Simulation
- Synthesis
- Power & Optimisation
- Physical Analysis (Timing, Themal, Signal)
- Verification
- Analogue and Mixed-Signal Design

System-Level Design:
- Behavioural Modelling & Analysis
- Physical Analysis
- Acceleration & Emulation
- Hardware/Software Co-Design
- Package Design
- PCB & MCM Design

Test:
- Design for Test
- Design for Manufacture and Yield
- Logic Analysis
- Test Automation (ATPG, BIST)
- Boundary Scan
- Silicon Validation
- Mixed-Signal Test
- System Test

Services:
- Design Consultancy
- Prototyping
- Data Management and Collaboration
- Training

Embedded Software Development:
- Real Time Operating Systems
- Debuggers

Hardware:
- FPGA & Reconfigurable Platforms
- Development Boards
- Workstations & IT Infrastructure

Monozukuri — ★ Booth: Campus 3D

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Monozukuri was founded in 2014 by a team of leading EDA IC and package co-design experts expressly to build new technology, from scratch, to deal with the I/O planning, and optimization phase of the physical implementation of complex 2.5D and 3D integrated circuits. The management team totals 50+ years of working experience at leading semiconductor and EDA companies, where it has given birth to multiple generation of IC and package co-design tools, methodologies, and flows. Privately held, Monozukuri is based in Rome, Italy. Monozukuri has received funding from both institutional and private investors. For further information, please, visit www.monozukuri.eu, or call +39-06-3211-0416.

MoRV - Modelling Reliability under Variability — ★ Booth: EP 3

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While feature sizes are continuously scaled towards atomic dimensions, industry is increasingly confronted with unexpected physical artefacts to be considered at each new technology node. Among these, process variation and parameter degradation lead to reliability concerns impacting integrated circuit design at all abstraction levels. As variation and degradation may become a limiting factor for future scaled technologies, there has been a tremendous research effort in understanding these artefacts. Versatile tools, allowing consideration of these artefacts and their combined impact during the design of ICs are still in their infancy.
Rather than developing yet another design support methodology, we aim to combine and refine existing reliability and variability prediction methodologies at the abstraction layers with highest industrial importance: Register transfer (RT) level - usual design entry, gate level – where most design for reliability (DfR) techniques are applied, and transistor level - where final sign-off is made.
MoRV will cover the strong relationship between variability and ageing, which are usu-

ally treated separately, fostering the idea of treating ageing as a form of time-dependent variability. Combined models from transistor, over gate, to RT level will be characterized directly from silicon measurement and all models will be able to interpret the same characterization data base from the silicon measurement.

MunEDA GmbH

★ Booth: Campus FDSOI

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MunEDA is a world leading provider of EDA tools for automated migration, analysis, modelling and optimization of custom circuits. MunEDA's WiCkeD design tool suite is the industry's most advanced solution high-sigma, low-power and high-performance verification and optimization of Custom IC Designs. Integrated into most industrial standard design and simulation environments WiCkeD delivers powerful and leading-edge tools to complement these flows and fill-up existing gaps or limitations. Additionally MunEDA offers outstanding solutions from partners for optical and display tools as well as custom layout. The tools offered by MunEDA enhance designers to speed-up their sizing and verification tasks as well achieving quality level far beyond of existing standard tools limits.
Customers of MunEDA including worldwide leading semiconductor companies such as Samsung, SKHynix, STMicroelectronics, Infineon, SMIC, Faraday, Novatek, Fraunhofer, ZMDI, HLMC and many more.
At DATE 2016 Campus MunEDA presents special low power optimization tools for IoT and RF applications in FDSOI technologies. MunEDA's solution are proven and qualified for the design in FDSOI technologies of its leading FDSOI foundry partners such as GLOBALFOUNDRIES.

ASIC and SOC Design:
- Analogue and Mixed-Signal Design
- Verification
- RF Design
- Reliability and Yield aware design
- High-Sigma Verification
- Low-Power Optimization

NANOxCOMP - Synthesis and Performance Optimization of a Switching Nano-Crossbar Computer

★ Booth: EP 4

Contact: Mustafa Altun

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The main goal of this project is developing a complete synthesis and optimization methodology for switching nano-crossbar arrays that leads to the design and construction of an emerging nanocomputer. New computing models for diode, FET, and four-terminal switch based nanoarrays are developed. The proposed methodology implements both arithmetic and memory elements, necessitated by achieving a computer, by considering performance parameters such as area, delay, power dissipation, and reliability. With combination of arithmetic and memory elements a synchronous state machine (SSM), representation of a computer, is realized. The proposed methodology targets variety of emerging technologies including nanowire/nanotube crossbar arrays, magnetic switch-based structures, and crossbar memories. The results of this project will be a foundation of nano-crossbar based circuit design techniques and greatly contribute to the construction of emerging computers beyond CMOS.
The topic of this project can be considered under the research area of "Emerging Computing Models" or "Computational Nanoelectronics", more specifically the design, modeling, and simulation of new nanoscale switches beyond CMOS. The topic is well addressed and fit in H2020 work programmes FET (Future and Emerging Technologies) and ICT-25 (Generic Micro- and Nano-electronic Technologies).

NOKIA

★ Booth: Campus 5G

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Nokia is a global leader in the technologies that connect people and things. Powered by the innovation of Bell Labs and Nokia Technologies, the company is at the forefront of creating and licensing the technologies that are increasingly at the heart of our connected lives.
With state-of-the-art software, hardware and services for any type of network, Nokia is uniquely positioned to help communication service providers, governments, and large enterprises deliver on the promise of 5G, the Cloud and the Internet of Things.

Application-Specific IP:

- Telecommunication
- Wireless Communication

Presto Engineering Inc.

★ Booth: 11

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Presto Engineering provides comprehensive semiconductor testing, product engineering and production solutions to IDM, fabless and electronics companies, contributing to improving ramp time, margins and quality of new products.
We are globally recognized experts in the development of test solutions, for component characterization, and production & logistics management of the semiconductor supply chain. This expertise, combined with our in-house "state of the art" testing equipment, ESD, reliability and failure analysis capabilities, EMS management software, and qualified personnel in key geographic location produces a competitive advantage for our customers. Presto help clients optimize end-product performance, including accelerating time to market, operating a world class IC manufacturing process, and achieving continuous improvement for quality and yield, without having to resort to large internal backend teams. We offer turn-key solutions from customer tape-out to delivery of finished goods to end-customer(s), including assembly, test, qualification, industrialization, and production sustaining activities.
Presto Engineering is headquartered in San Jose, California and has operations in Europe and Asia Additional information is available on the company's website at www.presto-eng.com.

PROXIMA - Probabilistic real-time control of mixed-criticality multicore and manycore systems

★ Booth: EP 1

Contact: Francisco J. Cazorla

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PROXIMA is a Integrated Project (IP) of the Seventh framework programme for research and technological development (FP7). The PROXIMA project provides industry ready software timing analysis using probabilistic analysis for many-core and multi-core critical real-time embedded systems and will enable cost-effective verification of software timing analysis including worst case execution time.

REPARA – Reengineering and Enabling Performance and poweR of Applications

★ Booth: EP 8

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In recent years, traditional processors have not been able to translate the advances of silicon fabrication technology into corresponding performance gain due to physical constraints and weaknesses of the sequential programming model. These difficulties have forced a shift from CPU-based homogeneous machines to heterogeneous architectures combining different kinds of computing devices, programmed in a highly parallel fashion yet poorly optimizing the available resources towards performance and low energy consumption.
The REPARA project aims to help the transformation and deployment of new and legacy applications in parallel heterogeneous computing architectures while maintaining a balance between application performance, energy efficiency and source code maintainability. The REPARA framework consists of a set of tools assisting the developer in the course of transforming and deploying the source code on heterogeneous platforms, supporting multicore CPU, GPU, DSP as well as reconfigurable FPGA devices. The framework relies on a REPARA-specific abstract representation of the source code allowing automatic code analysis and transformation. Hot spots of the code are identified and annotated as kernel candidates automatically. Selected kernels are mapped to computing devices considering performance and/or energy, relying on predictive models. Kernel code is transformed to specific programming models associated with the target device(s) automatically. The toolchain is based on a run-time system that provides means for coordination and scheduling. Initial evaluation of the framework shows that considerable performance and energy efficiency improvement can be achieved with low developer intervention for real-world industrial use case applications.

SAFURE - Safety and Security by design for interconnected mixed-critical cyberphysical systems

★ Booth: EP 7

Contact: SAFURE Coordinator Contact

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Website: www.safure.eu

The project SAFURE targets the design of cyber-physical systems by implementing a methodology that ensures safety and security "by construction". This methodology is enabled by a framework developed to extend system capabilities so as to control the concurrent effects of security threats on the system behaviour.

The goals of the SAFURE project are

- to implement a holistic approach to safety and security of embedded dependable systems, preventing and detecting potential attacks,
- to empower designers and developers with analysis methods, development tools and execution capabilities that jointly consider security and safety, and
- to set the ground for the development of SAFURE-compliant mixed-critical embedded products.

The results of SAFURE will be

- a framework with the capability to detect, prevent and protect from security threats on safety, the ability to monitor system integrity from application level down to the hardware level including time, energy, temperature and data integrity;
- a methodology that supports the joint design of safety and security of embedded systems, assisting the designers and developers with tools and modeling language extensions;
- proof of concept through 3 industrial use cases in automotive and telecommunications;
- recommendations for extensions of standards to integrate security on safety-critical systems;
- specifications to design and develop SAFURE-compliant products.

The SAFURE consortium brings together 12 partners, spread over 6 European countries and comprises basic research and service design with applied research and end-user oriented service.

SFB HAEC (TU Dresden)

★ Booth: 16+17

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The collaborative research center HAEC is a first attempt to achieve high adaptivity and energy efficiency in such an integrated approach. At the circuit level, we focus on innovative ideas for optical and wireless chip-to-chip communication. At the network level, we research secure, high performance network coding schemes for wired and wireless board-to-board communication. Innovative results at the hardware/software interface level will include energy control loops, which allow hardware to adapt to varying software requirements and vice versa. Software development in general is supported by energy-aware runtimes, energy-aware resource, stream and configuration management schemes and by an analysis framework for high performance/low energy applications. New internet applications are supported by innovations in energy-aware service execution. And, last but not least, formal methods are developed to offer a new quality of assurance in our systems of tomorrow. Demonstrating our results in a joint prototype - the HAEC Box - our goal is to become a pace setter for industry and academia on the design of future energy efficient-computing systems.

Springer Nature

★ Booth: 3

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Synopsys ★ Booth: Campus FDSOI & Automotive, Sponsor

Website: www.synopsys.com

Synopsys is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products.
Founded by Dr. Aart de Geus and a team of engineers from General Electric's Microelectronics Center in Research Triangle Park, North Carolina, Synopsys was first established as "Optimal Solutions" with a charter to develop and market ground-breaking synthesis technology developed by the team at General Electric. The company pioneered the commercial application of logic synthesis that has since been adopted by every major semiconductor design company in the world. This technology provided an exponential leap in integrated circuit (IC) design productivity by enabling engineers to specify chip functionality at a higher level of abstraction. Without this technology, the complex designs of today would not be possible.
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See more at:
http://www.synopsys.com/Company/AboutSynopsys/Pages/CompanyProfile.aspx#sthash.spf5Jb3i.dpuf

T-Systems Multimedia Solutions GmbH ★ Booth: Campus IoT

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Tata Consultancy Services (TCS) ★ Booth: Campus Automotive

Contact: Ravindra Kumar Metta

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Tata Consultancy Services (TCS) is an IT services, consulting and business solutions organization that delivers real results to global business, ensuring a level of certainty no other firm can match. TCS offers a consulting-led, integrated portfolio of IT, BPS, infrastructure, engineering and assurance services. This is delivered through its unique Global Network Delivery Model™, recognized as the benchmark of excellence in software development. A part of the Tata group, India's largest industrial conglomerate, TCS has over 319,000 of the world's best-trained consultants in 60 countries. The company generated consolidated revenues of US $15.5 billion for year ended March 31, 2015 and is listed on the National Stock Exchange and Bombay Stock Exchange in India.
Product Key Finders: Functional Requirements Specification, Functional Requirements Test Generation, Static Analysis of Embedded C Code, TCS ECA

TETRACOM ★ Booth: EP 2

Contact: Rainer Leupers

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Website: www.tetracom.eu

The mission of the TETRACOM Coordination Action is to boost European academia-to-industry technology transfer (TT) in all domains of Computing Systems. While many other European and national initiatives focus on training of entrepreneurs and support for start-up companies, the key differentiator of TETRACOM is a novel instrument called Technology Transfer Project (TTP). TTPs help to lower the barrier for researchers to make the first steps towards commercialisation of their research results. TTPs are designed to provide incentives for TT at small to medium scale via partial funding of dedicated, well-defined, and short term academia-industry collaborations that bring concrete R&D results into industrial use. This is implemented via competitive calls for TTPs, whose coordination, prioritization, evaluation, and management are the major actions of TETRACOM. The academic partner of the TTP proposals can be any public research institutions (e.g. universities, research centers, etc.) eligible for FP7 funding. TETRACOM currently runs, or has completed, 49 individual Technology Transfer Projects (TTPs). The three open calls for TTPs received 107 TTP proposals, with a total acceptance rate of 36%.
TETRACOM is co-funded by the European Commission Framework Programme 7 under the Grant Agreement No. 609491.

TUM CREATE Limited ★ Booth: Campus Automotive

Contact: Swaminathan Narayanaswamy

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TUM CREATE is a joint collaboration between Nanyang Technological University and Technische Universität München, funded by Singapore's National Research Foundation as part of the Campus for Research Excellence And Technological Enterprise (CREATE) program. We aim to improve Singapore's roadways, vehicles and public transportation network and support the integration of e-vehicles with our research.

Undo Software ★ Booth: 8a

Contact: Niamh Gallagher

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E-Mail: ngallagher@undo-software.com
Website: http://undo-software.com

Undo's products are used by thousands of developers to solve complex, real-world problems for leading technology companies from embedded to enterprise and High Performance Computing to banking. Its unique record, rewind and replay technology enables Linux and Android developers to see exactly what their program did at every step in its execution, and its reversible debugging and offline analysis capabilities allow problems to be fixed quickly and easily. Developers can now respond quickly to failures in production and test environments, increase their debugging productivity by at least 50% and improve software quality.

Undo is a privately held company headquartered in Cambridge, UK. It is one of fifteen select companies participating in Accenture's FinTech Innovation Lab in London and its technology has won numerous awards including 'Best Software Product' at the 2015 ARM Innovation Challenge and Gartner's 'Cool Vendor in Application Development'. For more information, see http://undo-software.com or follow us on Twitter at www.twitter.com/@undosoft.

University Booth ★ Booth: 15

Contact: Andreas Vörg and Jens Lienig

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ASIC and SOC Design:
- Design Entry
- Behavioural Modelling & Simulation
- Synthesis
- Power & Optimisation
- Physical Analysis (Timing, Themal, Signal)
- Verification
- Analogue and Mixed-Signal Design
- MEMS Design
- RF Design

System-Level Design:
- Behavioural Modelling & Analysis
- Physical Analysis
- Acceleration & Emulation
- Hardware/Software Co-Design
- Package Design
- PCB & MCM Design

Test:
- Design for Test
- Design for Manufacture and Yield
- Logic Analysis
- Test Automation (ATPG, BIST)
- Boundary Scan
- Silicon Validation
- Mixed-Signal Test
- System Test

Services:
- Design Consultancy
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- Data Management and Collaboration
- IP e-commerce & Exchange
- Foundry & Manufacturing
- Training

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- Real Time Operating Systems
- Debuggers
- Software/Modelling

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- Workstations & IT Infrastructure

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- Memory IP
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- On-Chip Debug
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- Synthesizable Libraries
- Test IP
- Verification IO

Application-Specific IP:
- Analogue & Mixed Signal IP
- Data Communication
- Digital Signal Processing
- Multimedia Graphics
- Networking
- Security
- Telecommunication
- Wireless Communication

X-FAB Semiconductor Foundries

★ Booth: Campus IoT

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Xilinx University Program

★ Booth: 7

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DETAILED INDEX

NOTES

DATE16
March 14–18, 2016, Dresden, Germany

HiPEAC
COMPILATION ARCHITECTURE

What industry members say about HiPEAC

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"If you're looking for skilled PhD engineers in processor design, system architecture, compilers and tools, look in HiPEAC, the best ones are there."

This project has received funding from the European Union's Horizon2020 research and innovation programme under grant agreement no. 687698.

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DATE 2017 — CALL FOR PAPERS

DATE 17

March 27–31, 2017, Lausanne, Switzerland

Scope of the Event

The 20th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website (www.date-conference.com).

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Temperature-Aware Design
- Power Estimation and Optimization
- Temperature Modeling and Management
- Emerging Technologies, Systems and Applications
- Formal Methods and Verification
- Network on Chip
- Architectural and Microarchitectural Design
- Architectural and High-Level Synthesis
- Reconfigurable Computing
- Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- Analogue and Mixed-Signal Circuits and Systems
- Interconnect, EMC, EMD and Packaging Modeling
- Multiprocessor System-on-Chip and Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical, Healthcare and Assistive Technology Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems; Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles; Software for MPSoC, Multi/many-core and GPU-based Systems

Submission of Papers

All papers have to be submitted electronically by Sunday September 11, 2016 via:
www.date-conference.com

Papers can be submitted either for standard oral presentation or for interactive presentation. **The Programme Committee also encourages proposals for Special Sessions, Tutorials, Friday Workshops, University Booth, PhD Forum and Exhibition Theatre.**

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