SLG4AX42397

OSFP Low-Speed Module Controller

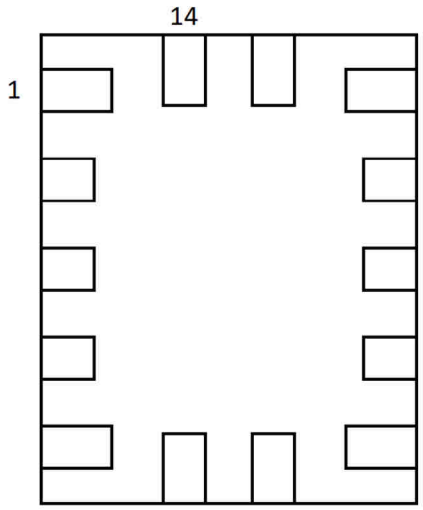
General Description

Dialog SLG4AX42397 is a low power and small form-factor bidirectional interface device for module-side low-speed OSFP standard interfaces based on a Dialog GreenPAK configurable mixed-signal IC. The device is available in a 1.6mm x 2.0mm STQFN package.

Features

- OSFP module specification V1.2 compliant low-speed module side interface support
- Integrated INT/RSTn and LPW/PRSn detection and generation
- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 14 Package

Pin Configuration



14-pin STQFN (Top View)

Table 1: Other Dialog OSFP Compatible Parts

Part Number	Description
SLG4AC42401	Dual OSFP Low-Speed Host Controller
SLG4AX42396	OSFP Low-Speed Host Controller
SLG4AX42397	OSFP Low-Speed Module Controller

Table 2: Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	GND
2	NC	9	HPW_PRSn
3	NC	10	INT_RSTn
4	M_LPW_invert	11	INT
5	M_INT_L_invert	12	M_INT_L
6	M_RSTn_invert	13	TEMP SENSOR
7	M_LPW	14	M_RSTn

Table 3: Ordering Information

Part Number	Package Type
SLG4AX42397V	14-pin STQFN
SLG4AX42397VTR	14-pin STQFN - Tape and Reel (3k units)

Block Diagram

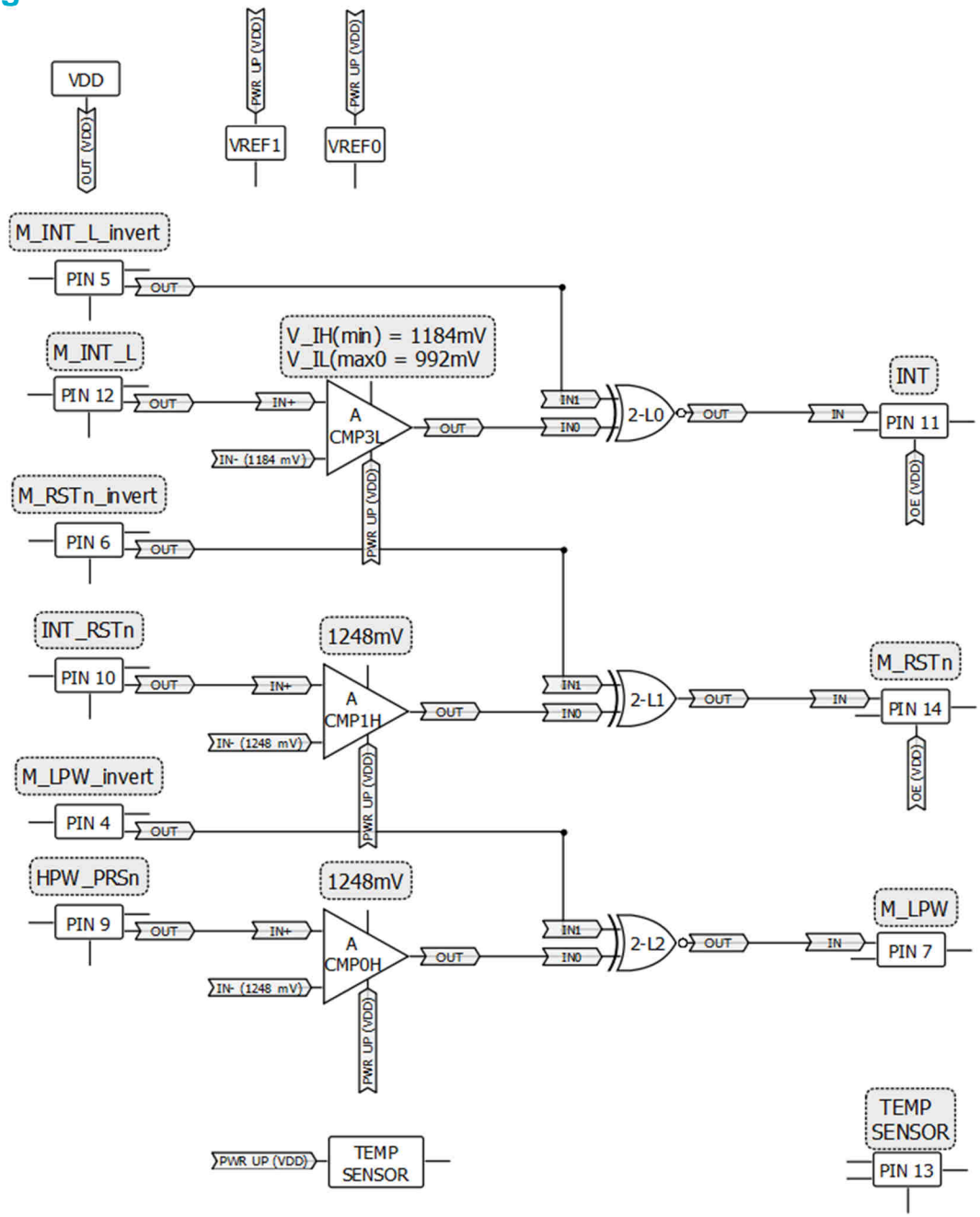


Figure 1. SLG4AX42397 internal block diagram

Table 4: Pin Configuration

Pin #	Pin Name	Type	Pin Description	Default Polarity
1	VDD	PWR	Supply Voltage	
4	M_LPW_invert	Digital Input	Input to invert M_LPW default polarity	N/A
5	M_INT_L_invert	Digital Input	Input to invert M_INT_L default polarity	N/A
6	M_RSTn_invert	Digital Input	Input to invert M_RSTn default polarity	N/A
7	M_LPW	Digital Output	Signal to Module that Host has asserted Low Power Mode	Active High
8	GND	GND		
9	HPW_PRSn	Analog Input/Output	OSFP slow speed signal	
10	INT_RSTn	Analog Input/Output	OSFP slow speed signal	
11	INT	Digital Output	Output to drive INT_RSTn to Interrupt operation	Active High
12	M_INT_L	Digital Input	Module control to GPAK to assert Interrupt	Active Low
13	TEMP SENSOR	Analog Input/Output	Temperature sensor output	
14	M_RSTn	Digital Output	Signal to Module that Host has asserted Module Reset	Active Low
2, 3	NC	--	Connect to GND	

Table 5: Absolute Maximum Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply voltage to GND	-0.3	7	V
V_I	Voltage at Input Pin	-0.3	7	V
I_{MAX}	Maximum Average or DC Current (Through V_{DD} or GND pin)	--	90	mA
I_{lkg}	Input leakage Current (Absolute Value)	--	1.0	µA
T_{STRG}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature	--	150	°C
T_{AMB}	Ambient operating temperature	-40	+85	°C
ESD	ESD Protection (Human Body Model)	±2000	--	V
	ESD Protection (Charged Device Model)	±1300	--	V
MSL	Moisture Sensitivity Level	1		

Table 6: Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	61	--	µA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=3.3V	0.7*V_{DD}	--	V_{DD}+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=3.3V	GND-0.3	--	0.3*V_{DD}	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, IOH=3mA at VDD=3.3V	2.7	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.16	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, VOH=2.4V at VDD=3.3V	5.29	--	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	4.68	--	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	12.07	--	--	mA
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 2	6	--	14	kΩ
V_{ACMP}	Analog Comparator 0 and 1 Threshold Voltage	Low to High transition, at temperature -40 +85°C (Note 3)	--	2496	--	mV
	Analog Comparator 3 Threshold Voltage	Low to High transition, at temperature -40 +85°C (Note 3)	--	1184	--	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	--	992	--	mV

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1	2	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.6	1.85	2.05	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides.
3. Guaranteed by Design.

Description

The SLG4AX42397 OSFP Low-Speed Module Controller device contains one pair of INT_RSTn and HPW_PRS signals transceivers.

INT_RSTn is a bi-directional dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The link uses multi-level signaling to provide direct signal control in both directions. The host signals a RESET to the module when M_RSTn is asserted low. The module (SLG4AX42397) signals an interrupt to the host when M_INT_L is asserted low.

HPW_PRS is another bi-directional dual function signal that allows the host to signal Low Power mode and the module (SLG4AX42397) to indicate Module Present using multi-level signaling to provide direct signal control in both directions. The host signals the module to enter the low power state when M_RSTn is asserted low.

The equation below calculates the typical analog voltage passed from the temperature sensor to Pin 13 with chip to chip variation of about ±2°C:

$$V_{TS} = -2.8 \times T + 1077.2$$

For ease of system use, three invert input pins have been added to invert the default polarity of output signals. Refer to Table 7.

Table 7: Output Polarity Control

Invert Pin Name	Status	Output Polarity
M_INTn_invert	Low	Active Low
	High	Active High
M_RSTn_invert	Low	Active Low
	High	Active High
M_LPW_invert	Low	Active High
	High	Active Low

Table 8: Other Dialog OSFP Compatible Parts

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Typical Application Circuit

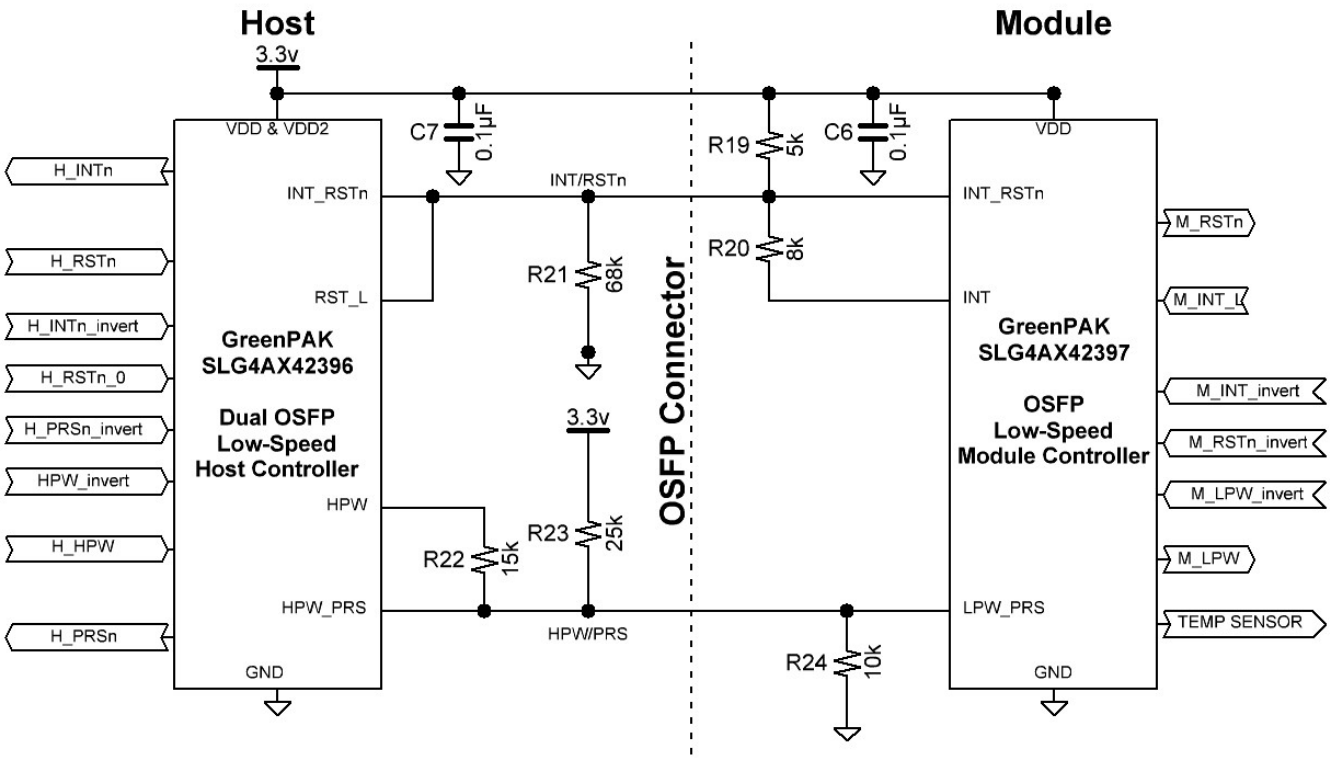


Figure 2: SLG4AX42397 Typical Application Circuit

Package Top Marking

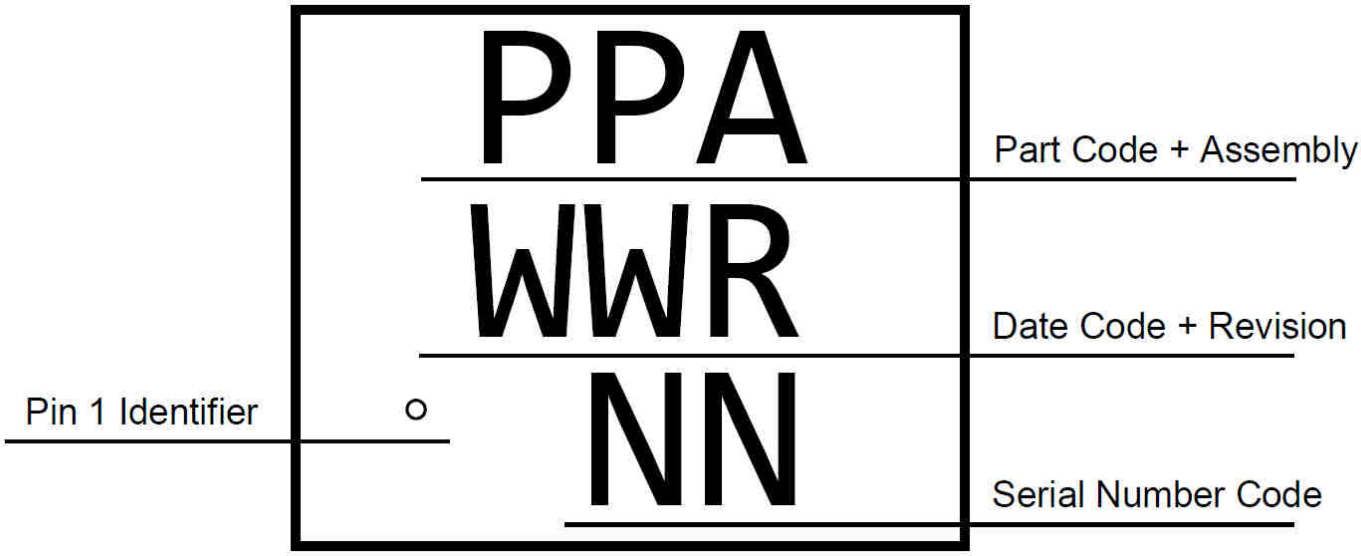


Figure 3. Package Top Marking

Table 9: Part Information

Datasheet Revision	Programming Code Number	Locked Status	Checksum	Part Code	Revision	Date
0.18	004	U	0x69AB0CAA			08/09/2018

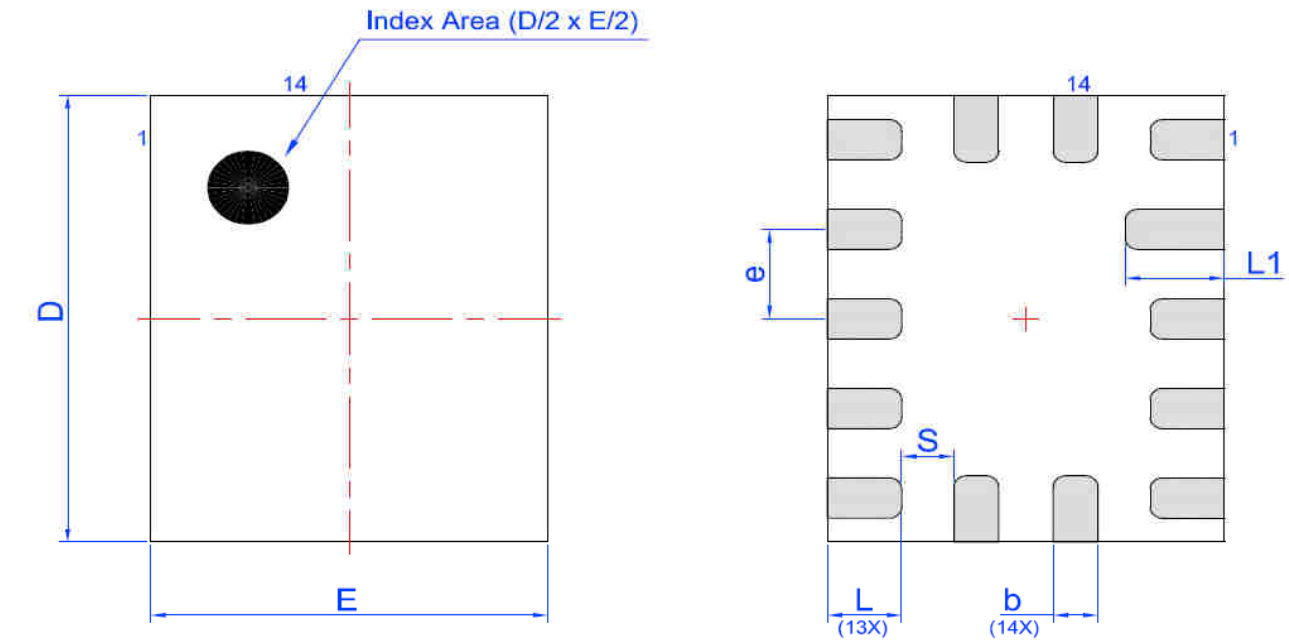
Table 10: Lock Status

Lock Status	
X	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

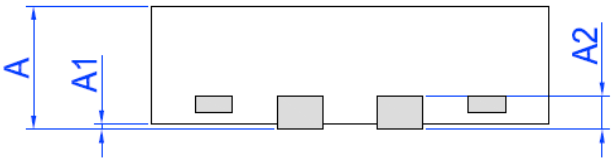
The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

STQFN 14L 1.6 x 2.0 x 0.55 mm 0.4P FC Package
IC Net Weight: TBD g



Marking View



Marking View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			S	0.21 REF		

Figure 4: SLG4AX42397 Package Drawing and Dimensions

Table 11: Tape and Reel Specification

Package Type	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
		per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 1.6x2mm 0.4P FC Green	1.6x2.0x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Table 12: Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6x2 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8

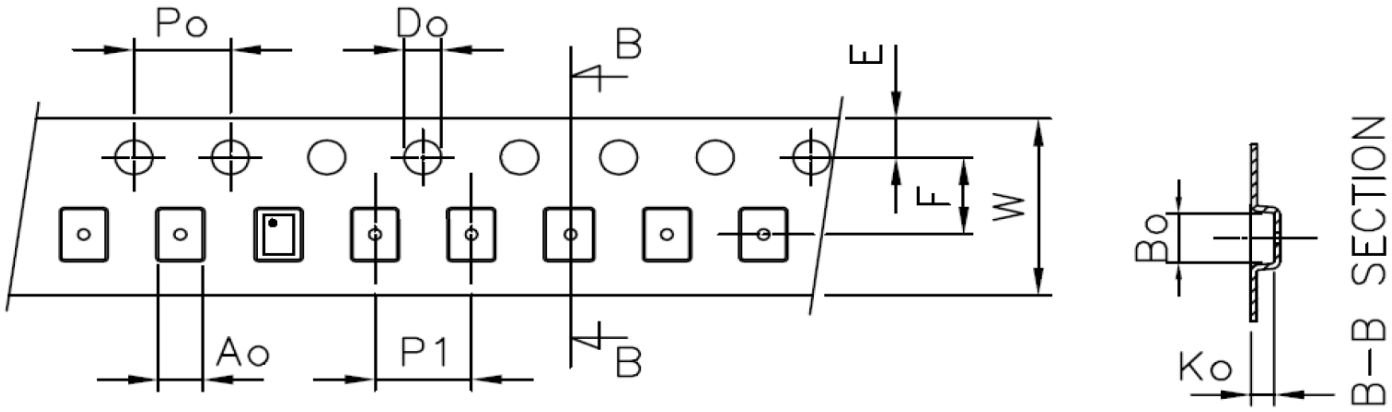


Figure 5: Tape Dimensions

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm^3 (nominal) for STQFN 14L Package. More information can be found at www.jedec.org.

Recommended Land Pattern

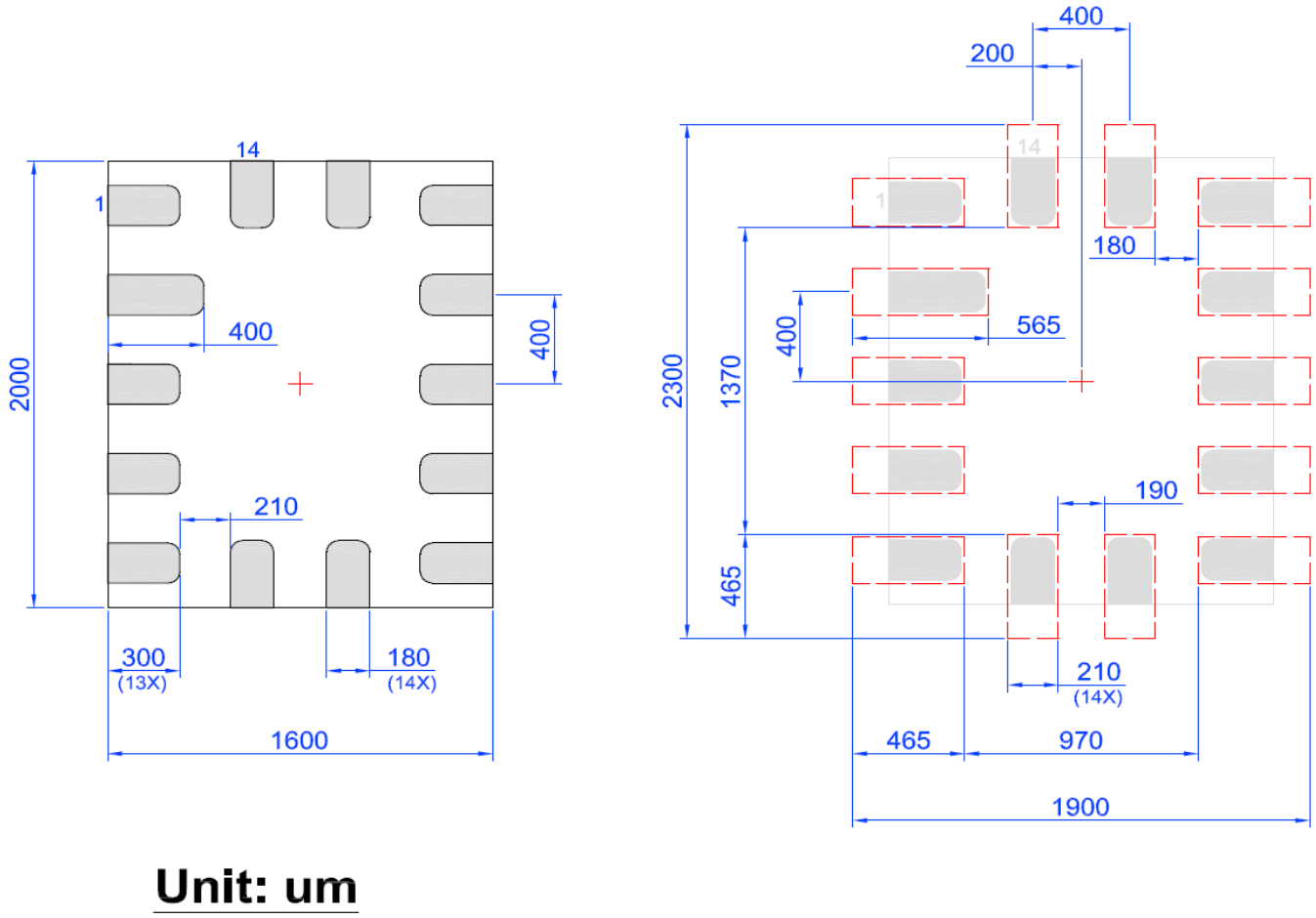


Figure 6: SLG4AX42397 Recommended Land Pattern

Table 13: Datasheet Revision History

Date	Version	Change
03/30/2018	0.10	New design for SLG46855 chip based on SLG4T42331
04/03/2018	0.11	Updated typical application circuit
04/26/2018	0.12	Updated Device Revision Table
06/14/2018	0.13	Updated with GP_r003
06/14/2018	0.14	Updated Device Revision Table
07/03/2018	0.15	Updated device functionality
07/25/2018	0.16	Updated DS formatting and updated temperature sensor
07/25/2018	0.17	Updated Programming Code Number
08/09/2018	0.18	Updated General Description with correct PN

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