HIGH PERFORMANCE CIRCUITS FOR POWER MANAGEMENT AND MILLIMETER WAVE APPLICATIONS

A Dissertation

by

AHMED MOHSEN AHMED AMER

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2012

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	Kamran Entesari
	Aniruddha Datta
	Mahmoud M. El-Halwagi
Head of Department,	Costas N. Georghiades

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ABSTRACT

High Performance Circuits for Power Management and Millimeter Wave Applications.

(May 2012)

Ahmed Mohsen Ahmed Amer, B.S.; M.S., Ain Shams University, Cairo, Egypt

Chair of Advisory Committee: Dr. Edgar Sanchez-Sinencio

The main focus of this work is to design and implement highly-efficient low-cost integrated circuits and systems for power management and millimeter wave applications. Novel system architectures and new circuit design techniques are introduced to achieve the required goals in terms of small silicon area and power consumption while at the same time achieve high performance. Four key building blocks in power management and a switchable harmonic mixer with pre-amplifier and poly-phase generator as a core part of a millimeter wave receiver are proposed, implemented and experimentally measured.

First, two externally compensated low drop-out voltage regulators (LDOs) with high power supply rejection (PSR) at high frequencies are presented. Complete PSR analysis is included together with detailed measurement results. The LDOs achieve a PSR of -56dB at 10MHz with a dropout voltage of only 0.15V. They are implemented on different CMOS processes, 0.13µm and 90nm, where they occupy small active areas of 0.049mm^2 and 0.015mm^2, respectively.

Second, an output-capacitorless LDO is presented. The LDO employs a novel topology that is adaptive to load current variations to ensure stability at light load condition and to provide fast transient response and high PSR. It is implemented in 90nm CMOS technology, and it uses a small on-chip capacitance of only 0.95pF. Measurements show that LDO achieves a fast settling time of 0.25μs and high PSR of -50dB at 1MHz while occupying an active area of 0.016mm^2. With dropout voltage of 0.15V, the LDO achieves a load regulation of 58.3μV/mA for a load current step of 120mA.

Third, a buck converter working at high switching frequency (10/20MHz) and using small on-chip and off-chip passive components is presented. The converter utilizes a novel simple controller to minimize the area (0.126mm^2) and quiescent current consumption (25 ~ 48μA), with power efficiency that is better than linear regulators.

Finally, a switchable harmonic mixer with pre-amplifier and poly-phase generator are presented as a part of a novel millimeter wave dual-band receiver (31/24 GHz) implemented in 0.18μm SiGe BiCMOS technology. Complete receiver measurements show a conversion gain higher than 18dB with a band rejection exceeding 40dB and power consumption of only 60mW.

DEDICATION

To my beloved mother, who was always behind every single achievement I had in my life and who passed away only four months before my PhD dissertation defense.

ACKNOWLEDGEMENTS

I would like to thank my committee chair, Dr. Sanchez, for his continuous guidance, encouragement, help and patience throughout the course of this research. I learned so many valuable things from him, but, above all, he taught me how to be devoted to research and how to help others.

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I would like to thank UMC and TSMC for providing the fabrication support and Texas Instruments and Microtune for funding support.

I would like to thank my parents. Their patience, care, and love are what guided me through my whole life. I pray to God that I will always be a good, faithful son to them. Last but not least, I would like to thank my lovely wife and little daughter who provided me with the perfect environment to work and achieve success.

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CHAPTER I

INTRODUCTION

1.1 Motivation and Goals

Power management systems are required in almost every integrated circuit. These include all different types of linear and switching regulators. Millimeter wave receivers on the other hand are very attractive nowadays with the advance in technology that allows integrated circuits to operate at tens of gigahertz frequencies for high-data-rate communication in addition to the congestion of the low-gigahertz frequency bands.

Recently, there has been an increasing demand for highly efficient low cost integrated circuits and systems for power management and millimeter wave applications. Thus, it has been an important requirement to design circuits of high performance while at the same time keeping the cost at minimum. The two main aspects to be reduced for minimizing the cost are the area and power consumption. The area includes both the integrated circuit silicon area as well as the area consumed by the external components required on board for the system to operate properly. Minimizing both areas results in significant reduction in the cost of the system implementation especially in small-sized widely-used portable applications. Lowering the power consumption results in better power efficiency and longer lifetime of the supplying batteries and thus the cost is significantly reduced. Reducing both area and power consumption while achieving better

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This dissertation follows the style of *IEEE Journal of Solid-State Circuits*.

performance compared to the existing state-of-the-art works is the main target of this dissertation.

In this dissertation, four key power management systems are designed and implemented on silicon. These high performance systems are two externally compensated low dropout (LDO) voltage regulators, an internally compensated output-capacitorless LDO regulator and a buck switching converter. For millimeter wave, a switchable harmonic mixer with pre-amplifier and poly-phase generator are designed and implemented as a core part of an area and power efficient dual-band (31/24GHz) millimeter wave receiver. A top level representation of the implemented systems can be demonstrated as shown in Fig. 1.1.

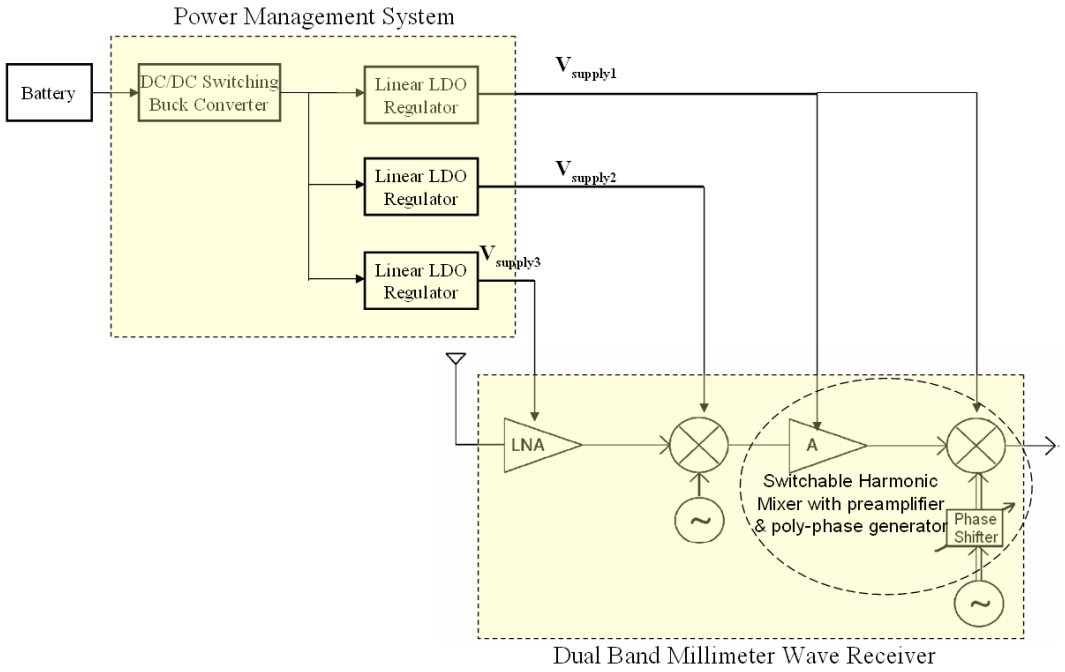


Fig. 1.1 Top level representation of the implemented systems.

The two proposed externally compensated low dropout (LDO) voltage regulators are mainly targeting the goal of achieving an improved high power supply rejection (PSR) up to mega-hertz frequency range. This is considered today as one of the challenging requirements in the power management field. This is due to the increasing switching frequencies of buck converters that are pushed towards the mega-hertz frequency range to have smaller sized external off-chip and on-chip passive components and to have smaller recovery times for the frequent load switching. This trend necessitates having a following LDO with good PSR up to these frequencies to get rid of any generated ripples.

The proposed output-capacitorless LDO (OCL-LDO) regulator is intended to have a good performance in terms of high PSR and fast transient response while eliminating the large external capacitor and minimizing the on-chip compensation capacitance for area and cost reduction.

For the buck converter, a novel implementation for the control scheme of a voltage mode synchronous buck converter is implemented. The main objective is to reduce the area and quiescent power consumption of the controller while using a high switching frequency of 10 to 20MHz.

A switchable harmonic mixer, pre-amplifier and poly-phase generator are designed and implemented as a part of a dual-band millimeter wave receiver working at 24 and 31GHz frequency bands. Through efficient frequency planning and novel wideband circuit ideas, the dual band receiver architecture reused various blocks of the front-end to minimize the complexity, area and power consumption. The dual band

receiver relies on the switchable harmonic mixer for band selection. The switchable harmonic mixer allows the local oscillator (LO) to run at a lower frequency, hence eliminating the need for a wideband voltage controlled oscillator (VCO) and reducing the power consumption.

1.2 Organization

In the following chapters, complete system and circuit analysis together with measurement results are presented for each of the proposed systems showing the performance improvement in comparison to previously published works in literature.

Chapter II presents the two different externally compensated LDO voltage regulators with high PSR up to a frequency of 10MHz. A complete PSR analysis and measurement results are discussed. A comparison with state-of-the-art designs clearly shows the improvement achieved.

In Chapter III the OCL-LDO regulator is presented. Complete stability and PSR analyses are provided for the proposed LDO. Measurement results are also included and discussed. Achieving fast transient response and high PSR at 1MHz while using an on-chip capacitance smaller than 1pF results in having the best figure-of-merit (FOM) in comparison to recently published OCL-LDOs.

The design and implementation of the area and power-efficient buck converter is included in Chapter IV. The novel controlling scheme, including both the compensator and modulator, is analyzed and complete measurement results are provided.

Chapter V presents the switchable harmonic mixer for the dual-band millimeter wave receiver working at 24 and 31GHz frequency bands. The complete system analysis

and the block level circuit analysis are presented. The mixer simulation results are included followed by the measurement results of the complete receiver.

In Chapter VI, conclusions are drawn and possible areas for future work related to the presented systems are identified.

CHAPTER II

HIGH PSR LOW-DROPOUT REGULATORS

2.1 Introduction

A typical power management system consists of a battery followed by a switching power converter (SWPC) that is followed by a low drop-out (LDO) voltage regulator as shown in Fig. 2.1(a). The voltage waveform at each node of the system is shown in Fig. 2.1(b). The LDO has a very important role to regulate the supply ripples at the SWPC output providing a clean voltage supply for the following noise-sensitive analog and RF blocks. Due to the increase in operating frequencies, high switching frequencies in SWPC are required for fast transient response in addition to allowing for the use of smaller passive components to reduce area and cost [1,2]. Ripples at these high switching frequencies appear at the output of the SWPC. The LDO has to be able to suppress these ripples and to provide a clean voltage supply at its output. In other words, the LDO should have a high power supply rejection (PSR) up to these few MHz frequencies.

Conventional LDOs have poor PSR at high frequencies due to the limited bandwidth of the error amplifier as well as the low output resistance of the pass transistor. This low output resistance problem becomes more pronounced at low feature size (sub-250nm) technologies where it provides a direct path for supply ripples to the LDO output.

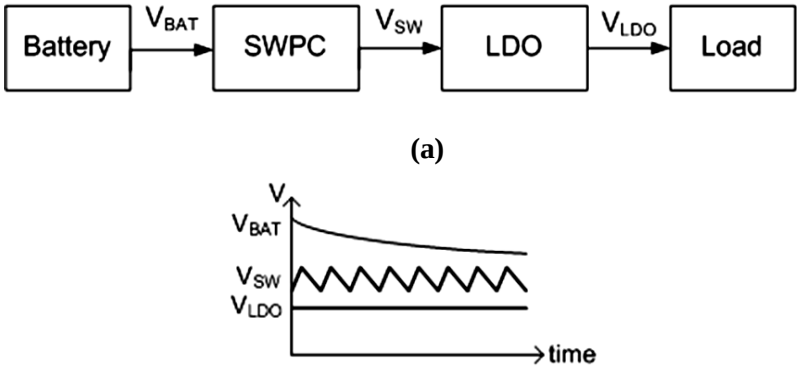


Fig. 2.1 (a) Typical power management system (b) Voltage waveforms at the different nodes.

2.1.1 Previously Reported Techniques

Different techniques have been reported to implement LDOs with high PSR at low frequencies. Straight-forward techniques include using simple RC filtering at the input of the LDO or cascading two regulators [3] as shown in Fig 2.2(a) and (b). However these techniques suffer from large area consumption and high dropout voltage.

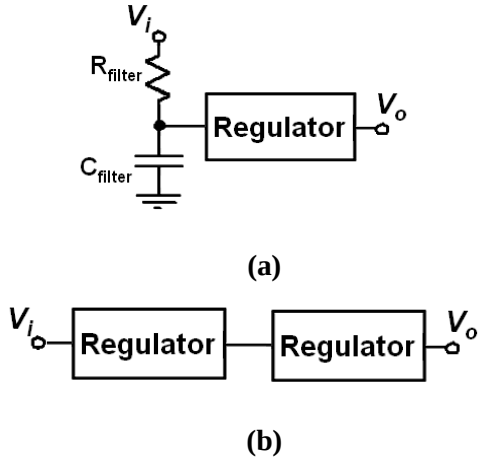


Fig. 2.2 (a) A filter preceding the LDO (b) Two LDOs in cascade.

Cascading two pass transistors using drain extended FET transistors [4] was used to improve the PSR through providing more isolation between input and output as shown in Fig. 2.3. Another technique used a voltage subtractor stage with a diode-connected transistor driving the gate of the pass transistor [5]. This technique is shown in Fig. 2.4 where the subtractor stage consists of transistors M1 and M2. The low impedence of the diode connected M2 helps replicating the supply ripples at the gate of the pass transistor so that, after subtraction, its gate-source voltage is free of ripples. However, in both cases in order to achieve high PSR at low frequencies, the gain of the error amplifier has to be increased through the use of multiple gain stages. This results in consuming large quiescent current as well as silicon area that is required for the internal compensation capacitors. Additional cost is also expected in case of using a special CMOS process with the drain extended devices.

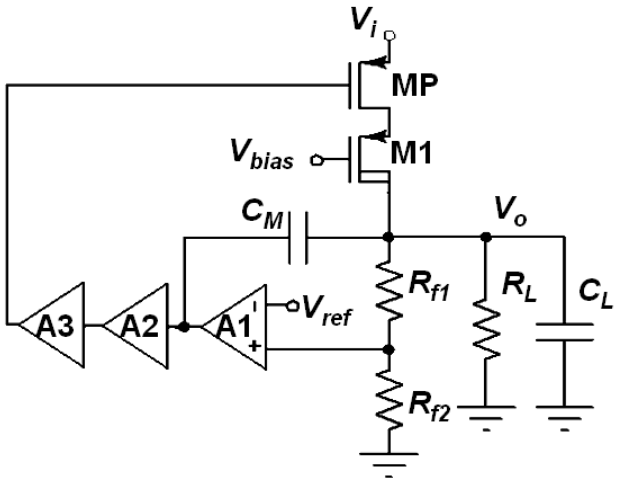


Fig. 2.3 Cascading two pass transistors using drain extended FET transistors.

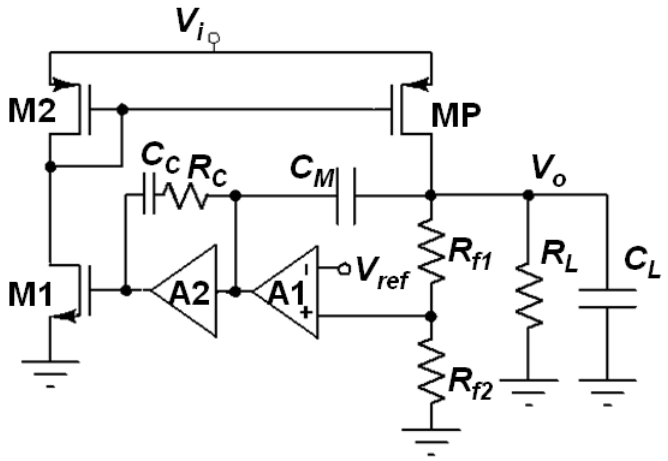


Fig. 2.4 Using a voltage subtractor stage.

Reference [6] was the first to achieve high PSR of -27dB at 10MHz frequency through using a cascade of NMOS and PMOS transistors with an RC filter at the gate of the NMOS. Thus, it provides more isolation and noise filtering. A charge pump is also required to bias the NMOS transistor as shown in Fig. 2.5. However, the circuit maximum load current (I_{Lmax}) was only 5mA with large dropout voltage (V_{DO}) of 0.6V. That is in addition to the added complexity and power consumption of the charge pump as a clock is necessary along with RC filtering to remove clock ripples.

In summary, the main idea behind most of the previously proposed techniques (except the voltage subtractor one), is to provide more isolation between the input and output along the high-current signal path. Hence, the area consumption and drop-out voltage are large, which is not suitable for low-voltage technologies. In addition, all these techniques provide high PSR at low frequencies with high quiescent power consumption, but are unable to provide sufficient PSR (better than -50dB) at frequencies up to several MHz.

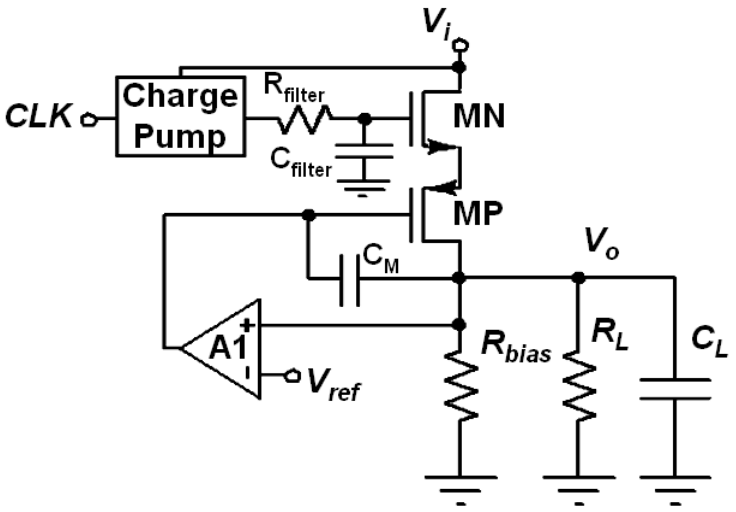


Fig. 2.5 Using a cascade of NMOS and PMOS transistors with a charge pump to bias the NMOS.

2.1.2 PSR of Conventional LDO

The finite PSR of the conventional LDO is due to several paths between the input and output of the LDO. Fig. 2.6 shows various paths that could couple input ripples to the output of the LDO. Path 1 is the main path through the transconductance of the pass transistor, Mp, regulated by the LDO loop. Path 2 is caused by the finite conductance of Mp, and it is more significant for technologies with lower feature sizes. Path 3 is as a result of the finite power-supply-rejection ratio of the error amplifier ($PSRR_{EA}$), and finally path 4 is due to the finite PSR of the bandgap circuit (PSR_{BG}).

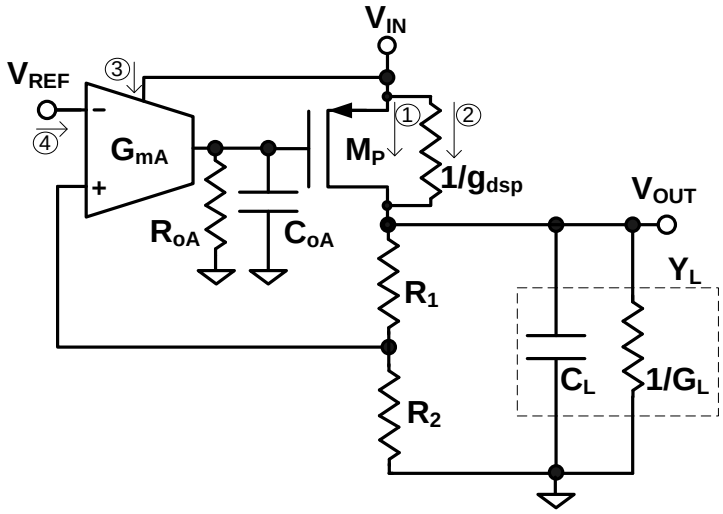


Fig. 2.6 Input to output ripple paths in a conventional LDO.

The LDO transfer function due to paths 1 and 2 is given by

$$\frac{v_{out}}{v_{in}} = \frac{g_{mp} + g_{dsp}}{Y_L + g_{dsp} + \dfrac{g_{mp}\beta G_{mA} R_{oA}}{1 + sR_a C_a}}. \qquad (2.1)$$

where g_{mp} and g_{dsp} are the transconductance and channel conductance of Mp. The error amplifier is modeled as a one pole amplifier where G_{mA}, R_{oA} and C_{oA} are its transconductance, output resistance and output capacitance, respectively. Thus, the error amplifier dc gain is given by $A_{EA} = G_{mA}R_{oA}$. β is defined as the feedback factor $R_2/(R_1+R_2)$. Y_L is the total load admittance, without the large feedback resistors R_1 and R_2. Substituting in (2.1) by $Y_L=G_L+sC_L$, where G_L and C_L are the load conductance and capacitance, respectively, then rearranging the equation we get:

$$\frac{v_{out}}{v_{in}} = \frac{(g_{mp} + g_{dsp})}{(1 + A_{ol})(G_L + g_{dsp})} \cdot \frac{(1 + sR_aC_a)}{1 + s\dfrac{\left(\dfrac{C_L}{G_L + g_{dsp}} + R_aC_a\right)}{1 + A_{ol}} + s^2 \dfrac{\left(\dfrac{C_L}{G_L + g_{dsp}} . R_aC_a\right)}{1 + A_{ol}}} \tag{2.2}$$

where A_{ol} is the dc open loop gain given by:

$$A_{ol} = \frac{\beta G_{mA} R_{oA} g_{mp}}{G_L + g_{dsp}} = \frac{\beta A_{EA} g_{mp}}{G_L + g_{dsp}} \tag{2.3}$$

Then (2.2) can be approximated to:

$$\frac{v_{out}}{v_{in}} \approx \frac{(1 + g_{dsp}/g_m)}{\beta A_{EA}} \cdot \frac{(1 + sR_aC_a)}{1 + s\dfrac{\left(\dfrac{C_L}{G_L + g_{dsp}} + R_aC_a\right)}{1 + A_{ol}} + s^2 \dfrac{\left(\dfrac{C_L}{G_L + g_{dsp}} . R_aC_a\right)}{1 + A_{ol}}} \tag{2.4}$$

Thus, if the channel conductance of Mp is neglected, i.e. path 2 is neglected; the PSR at DC will be just $1/\beta A_{EA}$ due to the main regulated path 1.

Two poles can be identified for the LDO circuit. $P_1 = 1/R_aC_a$ is located at the output of the error amplifier and $P_2 = (G_L + g_{dsp})/C_L$ is located at the LDO output. Equation (2.4) can be approximated depending on which pole is the dominant one.

A. P_1 is dominant:

Then (2.4) is approximated to (2.5):

$$\frac{v_{out}}{v_{in}} \approx \frac{1}{\beta A_{EA}} \cdot \frac{(1 + sR_aC_a)}{\left(1 + s\dfrac{C_L}{(G_L + g_{dsp})(1 + A_{ol})}\right)(1 + sR_aC_a)} \tag{2.5}$$

where there is a zero and two poles given by:

$$\omega_z = \frac{1}{R_a C_a},$$
$$\omega_{p1} = (1 + A_{ol}) \cdot \frac{(G_L + g_{dsp})}{C_L}, \tag{2.6}$$
$$\omega_{p2} = \frac{1}{R_a C_a}.$$

Thus, one pole in the transfer function is cancelled by a zero and only one pole is left at the gain-bandwidth product of the loop ($GBW|_{case1} = A_{ol}/R_aC_a$). However, the load capacitor has an effective series resistance (ESR) and an effective series inductance (ESL). Above its self resonance frequency ($f_{resonance}$), the capacitor will start to behave as an inductor and so the PSR will start to degrade as the frequency increases.

B. P_2 is dominant:

Then (2.4) is approximated to (2.7):

$$\frac{v_{out}}{v_{in}} \approx \frac{1}{\beta A_{EA}} \cdot \frac{(1 + sR_aC_a)}{\left(1 + s\frac{R_aC_a}{1 + A_{ol}}\right)\left(1 + s\frac{C_L}{G_L + g_{dsp}}\right)} \tag{2.7}$$

where the zero and poles frequencies are given by:

$$\omega_z = \frac{1}{R_a C_a},$$
$$\omega_{p1} = (1 + A_{ol}) \cdot \frac{1}{R_a C_a}, \tag{2.8}$$
$$\omega_{p2} = \frac{(G_L + g_{dsp})}{C_L}.$$

In this case, the PSR transfer function will have a zero at P_1 ($1/R_aC_a$) at which PSR will start to degrade. The zero is then followed by a pole at the gain-bandwidth product of the loop ($GBW|_{case2} = A_{ol}/R_aC_a$), and then comes the non dominant pole at the

output P_2 ($(G_L+g_{dsp})/C_L$) before finally the PSR will start degrading with frequency due to the ESL of the load capacitor.

The PSR curves for the two cases are illustrated in Fig. 2.7 showing that with the output pole P_1 being the dominant one, better PSR at high frequencies can be achieved.

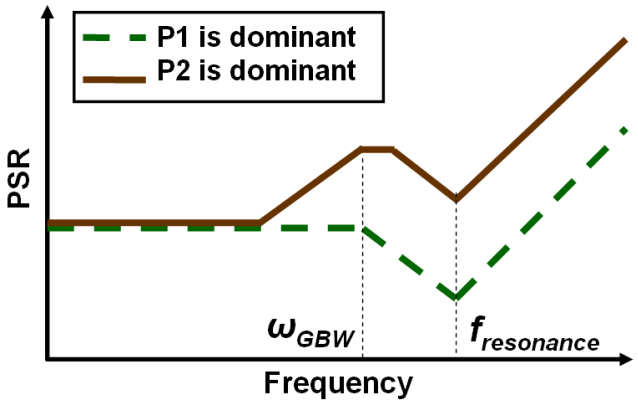


Fig. 2.7 PSR for the two different cases of dominant pole.

For paths 3 and 4, $PSRR_{EA}$ and PSR_{BG}, are defined as:

$$PSSR_{EA} = \frac{v_{oEA}/v_{sEA}}{v_{oEA}/v_{iEA}} = \frac{v_{iEA}}{v_{sEA}} \tag{2.9}$$

$$PSR_{BG} = \frac{v_{oBG}}{v_{sBG}} = \frac{v_{iEA}}{v_{sBG}} \tag{2.10}$$

where v_{sEA} and v_{sBG} represent the input supply ripples coming from the amplifier and the bandgap circuit, respectively and they are referred to the error amplifier input v_{iEA}. v_{oEA} and v_{oBG} are the outputs of the amplifier and the bandgap circuit, respectively.

Thus, the PSR transfer function (v_{out}/v_{in}) due to paths 3 and 4 can be calculated as:

$$\frac{v_{out}}{v_{in}}\Big|_{3,4} = \frac{v_{out}}{v_{sEA}} + \frac{v_{out}}{v_{sBG}}$$
$$\frac{v_{out}}{v_{in}}\Big|_{3,4} = \frac{v_{out}}{v_{iEA}}(PSSR_{EA} + PSR_{BG}) \quad (2.11)$$

where v_{out}/v_{iEA} is the closed loop transfer function. Thus (2.11) can be rewritten as:

$$\frac{v_{out}}{v_{in}} = \frac{\frac{g_{mp}}{Y_L + g_{dsp}} \cdot \frac{A_{EA}}{(1+sR_aC_a)}}{1+\beta\frac{g_{mp}}{Y_L + g_{dsp}} \cdot \frac{A_{EA}}{(1+sR_aC_a)}} \cdot (PSRR_{EA} + PSR_{BG}) \quad (2.12)$$

With high loop gain at low frequency, (2.12) can be approximated to (2.13):

$$\frac{v_{out}}{v_{in}}\Big|_{low\ frequency} = \frac{1}{\beta} \cdot (PSRR_{EA} + PSR_{BG}) \quad (2.13)$$

This means that the finite PSR due to paths 3 and 4 is an amplified quantity of $PSRR_{EA}$ and PSR_{BG} by the factor of $1/\beta$. However at high frequency the loop gain vanishes and thus the ripples leaking through the error amplifier and bandgap do not appear at the output at high frequencies. Therefore, the PSR due to paths 3 and 4 can be taken care of through good design of error amplifier and bandgap circuit with high supply rejection at low frequencies.

In summary, all four paths affect the PSR at low frequencies while only paths 1 and 2 affect the PSR at high frequencies. Several techniques could be applied to reduce the PSR at lower frequencies by decreasing $PSRR_{EA}$, PSR_{BG} and increasing gain of error amplifier. However at higher frequencies, the dominant pole of the error amplifier degrades the PSR of the LDO, and the off-chip capacitor is considered as an open circuit because of its ESL. None of the previously presented techniques have solved this problem satisfactorily. Usually, the PSR of LDO starts to degrade around 10-100 kHz [6]. In this

chapter, the fundamental limitation of the PSR due to paths 1 and 2 is analyzed and then two solutions are proposed for achieving high PSR at high frequencies are demonstrated.

2.1.3 Fundamental Condtition for Supply Ripples Cancellation

Focusing on the two main paths for input supply ripples to flow through the pass transistor, paths 1 and 2 in Fig. 2.6, the fundamental condition for canceling these ripples is driven in this section. The output small signal current i_{out} is given by:

$$i_{out} = g_{mp} v_{sg} + g_{dsp} v_{sd} \tag{2.14}$$

Thus, a simple block diagram representation of the pass transistor followed by the output load can be shown in Fig. 2.8. v_{in}, v_g are the voltages applied at the source and gate terminals of the transistor, respectively, while v_{out} is the output voltage at its drain terminal.

Now i_{out} can be rewritten as:

$$i_{out} = g_{mp}(v_{in} - v_g) + g_{dsp}(v_{in} - v_{out}) \tag{2.15}$$

and since $v_{out}=i_{out}R_L$ then $i_{out}=v_{out}G_L$.

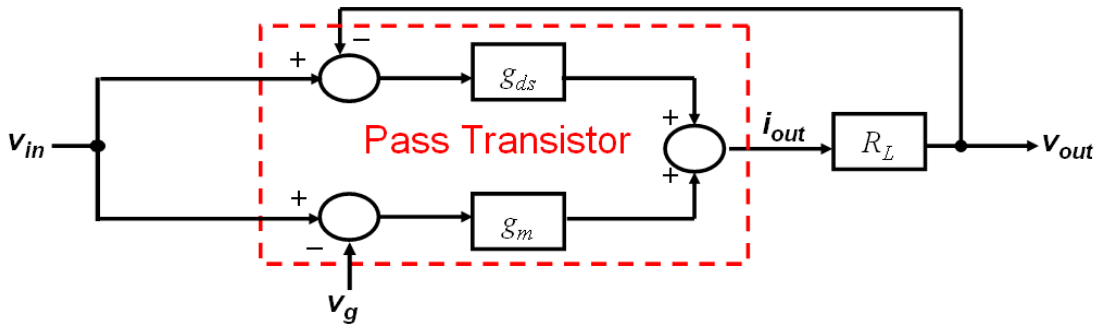


Fig. 2.8 Block diagram representation of the pass transistor.

Thus:

$$v_{out} = \frac{(g_{mp} + g_{dsp})v_{in} - g_{mp}v_g}{g_{dsp} + G_L} \tag{2.16}$$

Therefore, for v_{out} to be zero the nominator of (2.10) has to vanish:

$$v_g = \left(1 + \frac{g_{dsp}}{g_{mp}}\right)v_{in} = \left(1 + \frac{1}{g_{mp}r_{dsp}}\right)v_{in} = \left(1 + \frac{1}{A_{MP}}\right)v_{in} \tag{2.17}$$

where A_{MP} is the intrinsic gain of the pass transistor.

Thus, we need a feed-forward path from v_{in} to v_g with a gain of $(1+1/A_{MP})$ for complete ripple cancellation. This can be seen as two different paths. One of unity gain that is canceling the ripples due to g_{mp} and the other one is of gain $1/A_{MP}$ canceling the ripples leaking through g_{dsp}.

The technique in general form is shown in Fig. 2.9 illustrating how fundamentally the ripples through the two paths of the pass transistor can be cancelled.

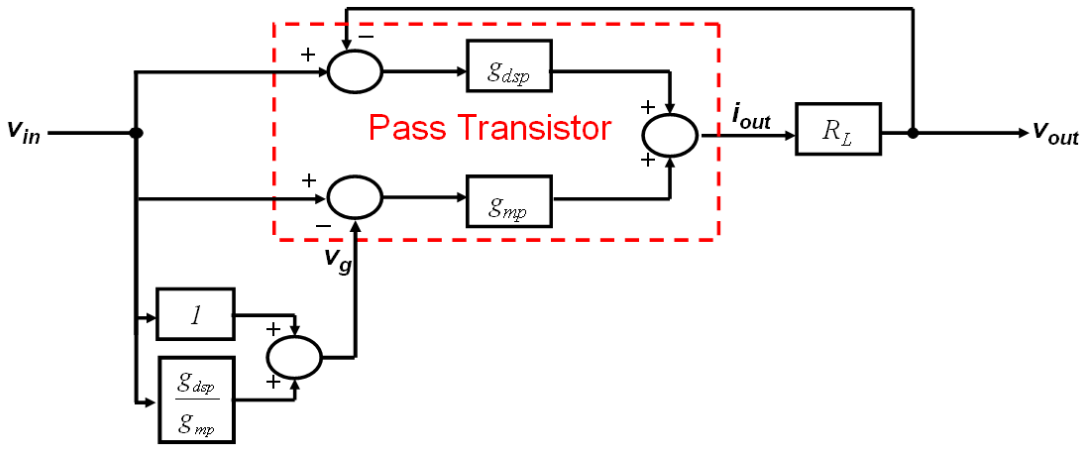


Fig. 2.9 Ripple cancellation fundamental idea.

2.1.4 Proposed Solutions

In this chapter we are presenting two different solutions to achieve a high PSR at high frequencies for an LDO. The first solution uses a feed-forward ripple cancellation (FFRC) technique [7,8] while the second one uses an adaptive technique [9] to cancel the ripples leaking along both paths 1 and 2 through the pass transistor.

2.2 Feed-forward Ripple Cancellation Technique

2.2.1 Basic Idea

As previously explained, to eliminate input ripples from appearing at the output, a zero transfer gain is necessary from the input to the output in Fig. 2.9. In the ideal case (without considering r_{dsp}), this is achieved by implementing a feed-forward path that replicates same input ripples at the gate of the pass transistor. Hence, the gate-overdrive voltage is independent of input ripples, and as a result no ripple appears across the load. In the actual case (with r_{dsp}), part of the ripples leak through the finite output resistance of Mp, and should be removed. This is done by increasing the ripple amplitude appearing at the gate of Mp by an amount of $(g_{mp} + g_{dsp})/g_{mp}$ to cancel ripples that leak through r_{dsp}

Fig. 2.10 presents a simplified block-level description of the proposed FFRC-LDO. Supply ripples, appearing at the source of pass transistor Mp, are reproduced at the gate of Mp using the feed-forward path. The generated ripples at the gate are higher in magnitude than input ripples to cancel additional ripples appearing at the output due to r_{dsp}. The feed-forward path is implemented using a feed-forward amplifier and a summing amplifier. The summing amplifier is used to merge the feedback regulating loop with feed-forward path at the gate of the transistor Mp.

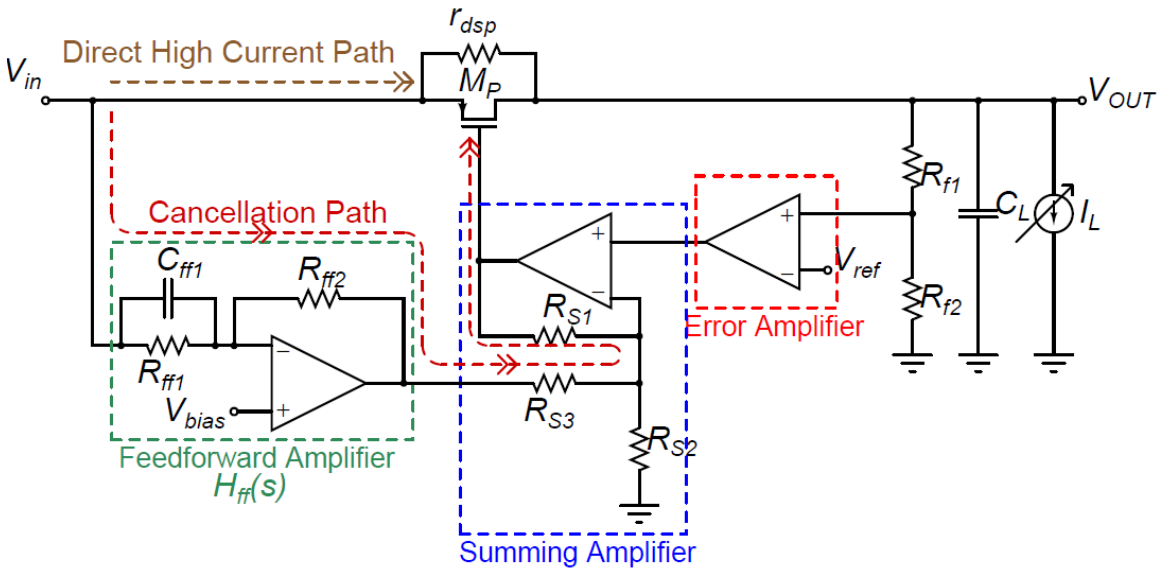


Fig. 2.10 Block-level representation of the feed-forward ripple cancellation LDO.

2.2.2 PSR Analysis

To find the Optimum value of the feed-forward gain, the block diagram representation of the LDO shown in Fig. 2.11 is used. The gains of the error amplifier and summing amplifiers are modeled by $A_{EA}/(1+s/\omega_{EA})$ and $A_S/(1+s/\omega_S)$, respectively, where A_{EA} and A_S are the DC gains while ω_{EA} and ω_S are the dominant-pole frequencies of the two amplifiers. The optimum value for the feed-forward gain $H_{FF}(s)$ is then calculated accordingly. Without the feed-forward path, $H_{FF}(s)$, the block diagram is similar to a conventional LDO. The ratio between v_{out} and v_{in} simply defines the PSR transfer function of the system.

$$v_{out} = [g_{mp}(v_{in} - v_g) + g_{dsp}(v_{in} - v_{out})] \cdot Z_L, \tag{2.18}$$

where Z_L is the total impedance seen at the output of the LDO.

v_g is obtained as follows:

$$v_g = \left[H_{FF}(s) \cdot v_{in} + \frac{\beta A_{EA}}{1 + s/\omega_{EA}} v_{out} \right] \cdot \frac{A_S}{1 + s/\omega_S}, \tag{2.19}$$

Then substituting for v_g from (2.19) in (2.18) and using $Y_L = 1/Z_L$, v_{out}/v_{in} will be given by:

$$\frac{v_{out}}{v_{in}} = \frac{g_{dsp} + g_{mp}\left(1 - H_{FF}(s)\frac{A_S}{1 + s/\omega_S}\right)}{Y_L + g_{dsp} + \left(g_{mp}\beta \cdot \frac{A_{EA}}{1 + s/\omega_{EA}} \cdot \frac{A_S}{1 + s/\omega_S}\right)}. \tag{2.20}$$

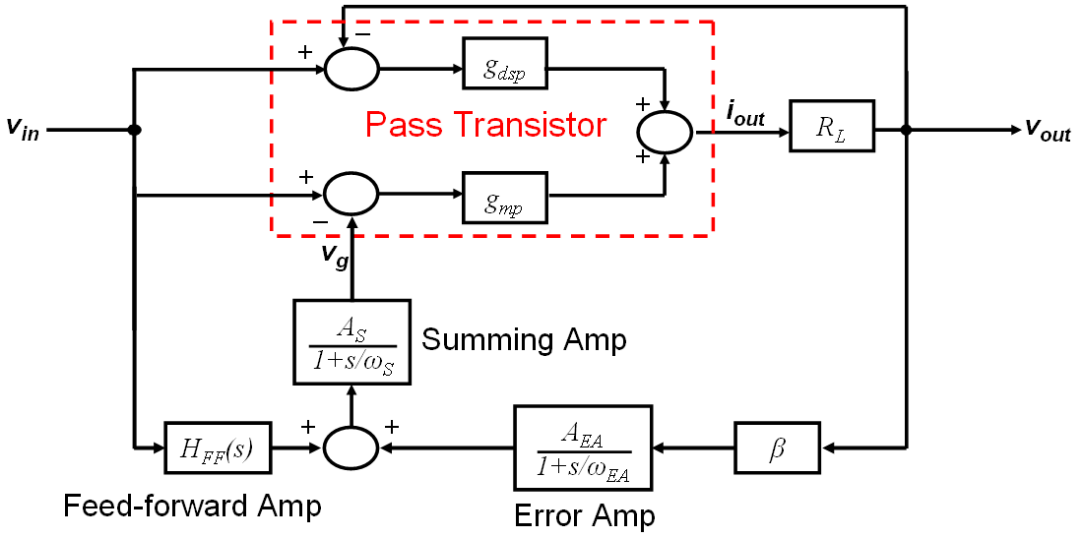


Fig. 2.11 Block diagram representation of the feed-forward ripple cancellation LDO.

To remove the ripples at the output, the numerator of (2.20) needs to be set to zero. The optimum value for $H_{FF}(s)$ is then given by:

$$H_{FF}(s)\big|_{opt} = \left(1 + \frac{g_{dsp}}{g_{mp}}\right)\frac{1 + s/\omega_S}{A_S}. \tag{2.21}$$

This agrees with (2.17) for the ripple cancellation fundamental condition where the transfer function from v_{in} to v_g through the feed-forward and summing amplifiers is optimally just $1+g_{dsp}/g_{mp}$. The optimum feed-forward amplifier gain has to contain a zero in its transfer function to cancel the effect of the pole existing at the output of the summing amplifier (at the gate of the pass transistor) in order to extend the frequency range of the ripple rejection. Then this cancellation technique is limited by internal poles of the summing and feed-forward amplifiers. The zero is implemented using the capacitor C_{ff1} in Fig. 2.10.

The simulated PSR of the LDO with and without FFRC technique is demonstrated in Fig. 2.12.

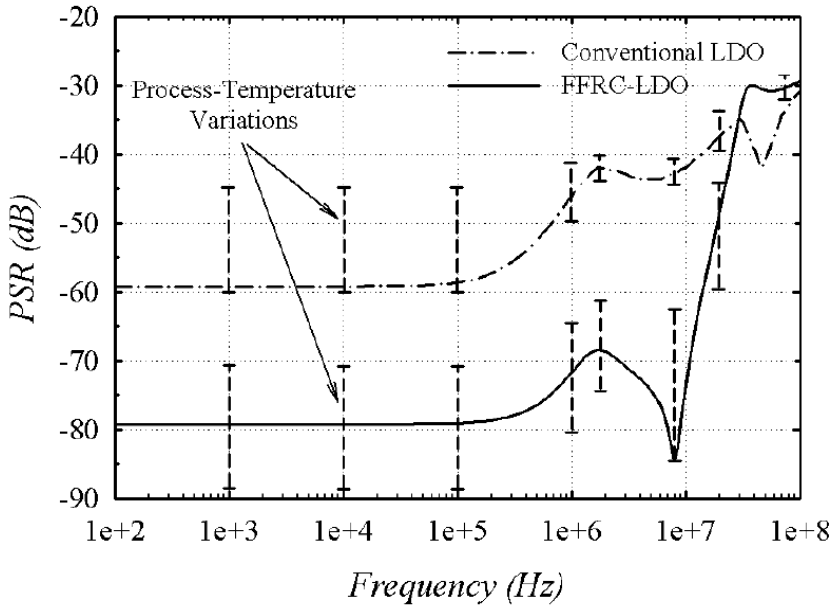


Fig. 2.12 PSR schematic simulations of conventional and FFRC-LDO (R_L = 40Ω). The effect of process and temperature variations is also demonstrated.

Using the conventional architecture, the achieved PSR is less than 60dB at DC and it starts to degrade around 330KHz. This frequency is located at the dominant pole of the error amplifier. Using the FFRC-LDO the PSR at DC is enhanced by 20dB. Besides, the additional zero increases the frequency at which the PSR starts to increase to 9MHz. This simulation shows the effectiveness of the FFRC-LDO to enhance the PSR at both DC and high frequencies. The PSR starts initially to increase around 330KHz, which is the bandwidth of the error amplifier. Then around 1MHz, the introduced zero stops the increase in the PSR. Due to the self-resonance frequency of the off-chip capacitor and finite non-dominate poles of the feed-forward and summing amplifiers, the PSR starts to degrade again at high frequencies. The main advantage of this FFRC approach is achieving a high PSR for a wide frequency range, without the need to increase the loop bandwidth and hence the quiescent power consumption. Moreover, this approach preserves the same low drop-out voltage of a conventional regulator, since supply rejection does not occur on the high-current signal path. The gain of the feed-forward and summing amplifiers is based on the ratio of resistors to reduce its dependency to process-temperature (PT) variations.

The variation of the PSR versus the load current is shown in Fig. 2.13. As depicted, the PSR has its best value for a current of 5mA at low frequencies. As the current increases, PSR is degraded due to the dependency of the DC gain of the pass transistor M_p ($g_{mp}r_{dsp}$) on the output current. For small currents, the transistor M_p is biased in deep saturation with a DC gain of 20dB. As the current increases, the transistor operating point moves near the linear region, and therefore, the DC gain is reduced to

14dB at a load current of 25mA. This example shows that $H_{FF}(s)$ has to be configurable if the LDO is designed to cover a wide range of currents.

One possible way to change $H_{FF}(s)$ gain with load current is to change the resistor R_{FF2} depending on the value of the load current. This may be done through dividing the load current range into a number of discrete ranges. Through sensing the gate voltage of the pass transistor, which varies according to load current, and comparing it to known references, the right range is determined and consequently the right R_{FF2} is selected. May be two ranges/resistors are enough then only one comparator is needed and its output is going to digitally control two switches. Thus, at any given load current only one switch is on connecting the appropriate resistor while the other switch is off.

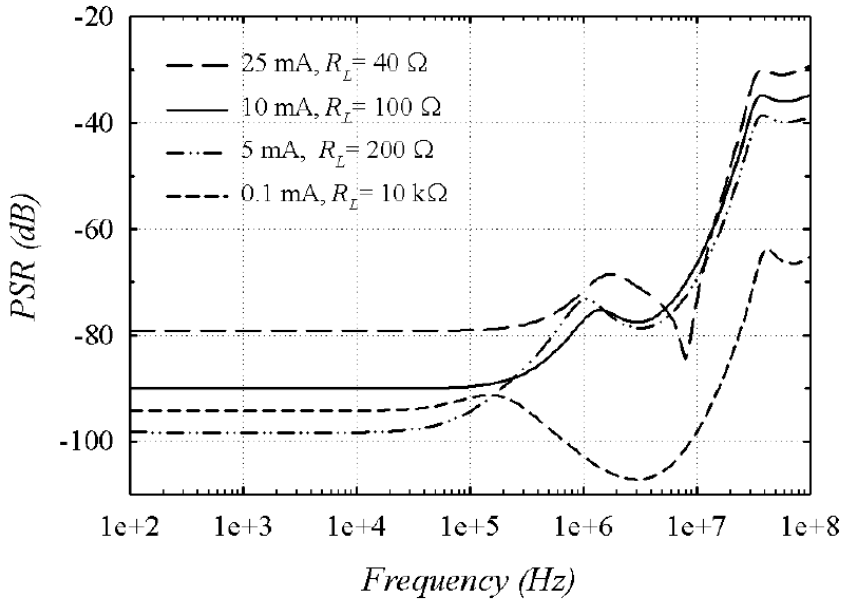


Fig. 2.13 PSR schematic simulations of FFRC-LDO for various load conditions.

The biasing voltage of the summing amplifier, V_{bias} in Fig. 2.10 has to be adjusted such that the output DC voltage of the summing amplifier is higher than zero. There is a minimum value for V_{bias} for proper operation of the FFRC-LDO. $V_{bias}|_{min}$ is given by

$$V_{bias}|_{\min} = V_{in}|_{\max} \cdot \frac{R_{ff2}}{R_{ff1} + R_{ff2}}. \tag{2.22}$$

As high PSR is only required when the output is stabilized, this system biases the positive terminal of the feed-forward amplifier directly from the output, i.e. $V_{bias} = V_{out}$. The maximum input voltage that can be applied in this case is 2V for an output voltage of 1V and $R_{ff2}/R_{ff1} =1$. Connecting the output directly to V_{bias} requires no additional voltage reference circuit, and hence, no additional power is consumed. However, in a different design, another reference voltage can be added if the output voltage of the LDO is not high enough to satisfy the condition in (2.22).

2.2.3 Circuit Implementaion

The complete transistor-level implementation of the FFRC-LDO is shown in Fig. 2.14. The error amplifier utilizes current sources with improved output impedance as active loads [10]. This implementation boosts the output impedance of the amplifier through the feedback loop formed by transistors M_{3a} and M_{2a}. The resultant gain is higher than 55dB. In addition, $PSRR_{EA}$ exceeds 90dB at DC to guarantee that the PSR of the LDO is not limited by error amplifier as depicted in the analysis in the previous section. The capacitor, C_{c1}, is added to stabilize the internal feedback loop of the error amplifier. The gain and $PSRR_{EA}$ schematic level simulations of the stand-alone error amplifier are shown in Fig. 2.15. The error amplifier achieves a 3-dB bandwidth of 180KHz, and

consumes a current of 12µA. This simulation shows that the PSR of the LDO does not depend on the bandwidth of the error amplifier when the FFRC technique is used.

The error amplifier has a limited output swing. This limited swing could be problematic for conventional LDOs when the error amplifier drives the pass transistor to accommodate a wide range of load currents. However in the proposed LDO, the summing amplifier drives the gate of the pass transistor. The summing amplifier is implemented using a two stage amplifier configuration with resistive feedback, as shown in Fig. 2.10. A wide output swing is achieved from the second stage of this amplifier. The pass transistor gate capacitance is used to create the dominant pole of the amplifier, and hence, no additional capacitor is required to stabilize the amplifier. Without summing feedback resistances, the output pole exist at 500KHz, and the internal non-dominant pole is at 28MHz resulting in an amplifier phase margin of 45°. With the summing feedback resistances, the amplifier has a pole at 28MHz, which is much higher than the GBW of the complete LDO. Therefore, the two stage topology does not affect the stability of LDO. The PSRR of the summing amplifier is not critical in this design because the PSRR is attenuated by the gain of the error amplifier. Same thing is applied to the feed-forward amplifier which is also implemented using a two stage amplifier with resistive feedback. The capacitor, C_{c2}, and resistor, R_{c2}, are used to stabilize the amplifier. In this design, each of the summing and feed-forward amplifiers consumes a current of 13µA. The total on-chip capacitance that is used to compensate the amplifiers is less than 5pF.

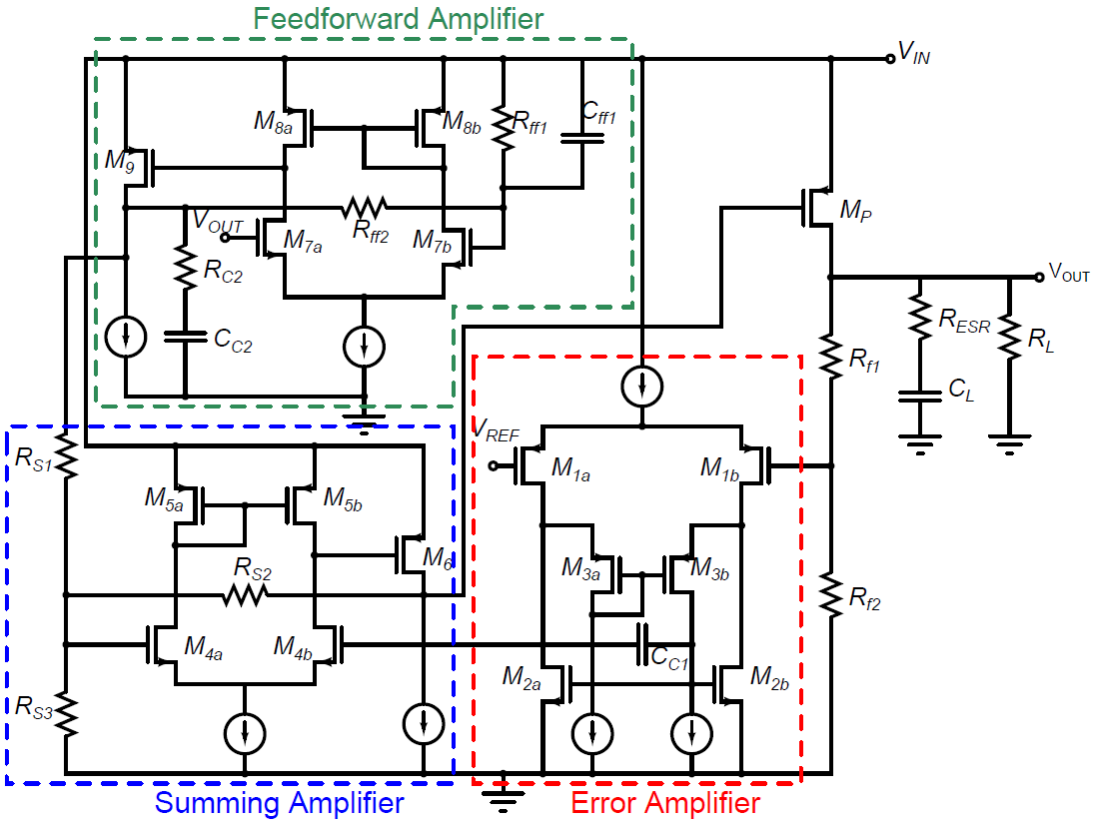


Fig. 2.14 Transistor-level implementation of the FFRC-LDO.

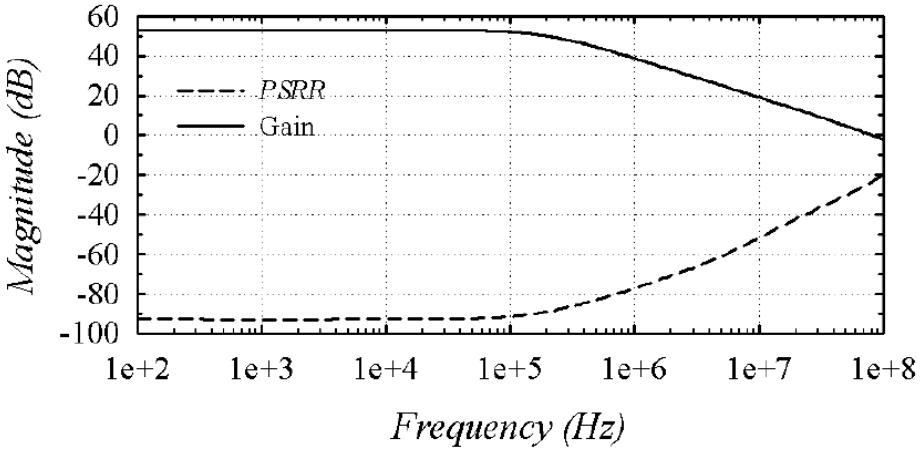


Fig. 2.15 Simulated gain and $PSRR_{EA}$ of the error amplifier.

The pass transistor is implemented using a PMOS device with minimum channel length (0.12µm) and 2.4mm width. Interdigitized and common centroid layout techniques are used to achieve high matching between the various resistors and transistors. Kelvin connection is utilized to connect the LDO to the package to reduce the dependency on the bonding inductance. Two parallel off-chip capacitors, each 2µF, are used as the capacitive load of the LDO to reduce the effective ESL with high $f_{resonance}$. During the design phase, the parasitic inductances, capacitances and resistances of the printed circuit board are also modeled to achieve simulations close to the measured performance. The inductance and resistance of the traces are assumed to be 0.5nH and 1mΩ per 1mm, respectively. Without modeling these effects, the simulated PSR at high frequencies is not close to the one measured.

2.2.4 Measurement Results

The LDO is fabricated using 0.13µm CMOS technology. The chip is encapsulated in a Quad Flat No-leads (QFN) package, and the chip micrograph is shown in Fig. 2.16. The total active area of LDO is $0.1mm^2$ including the bandgap circuitry. The bandgap circuit occupies around 50% of the total area. Two off-chip capacitors, each 2µF, are used to stabilize the LDO. The off-chip load capacitor has an ESL and ESR of 400pH and 10mΩ, respectively. However, the effective ESL and ESR are higher due to the trace parasitics. The total quiescent current of the LDO is 50µA at an input of 1.15V, where 8µA is consumed by the bandgap circuitry. The LDO operates for an input voltage ranging from 1.15 to 1.8V and the output voltage is 1V. This shows a measured minimum V_{DO} of 0.15V. The quiescent current depends on the input voltage and load current due to

the DC path formed by summing and feed-forward resistances. At 1.8V, the quiescent current increases by 6µA. It is important to note that the biasing current of the second stage of summing and feed-forward amplifiers should account for such current variations.

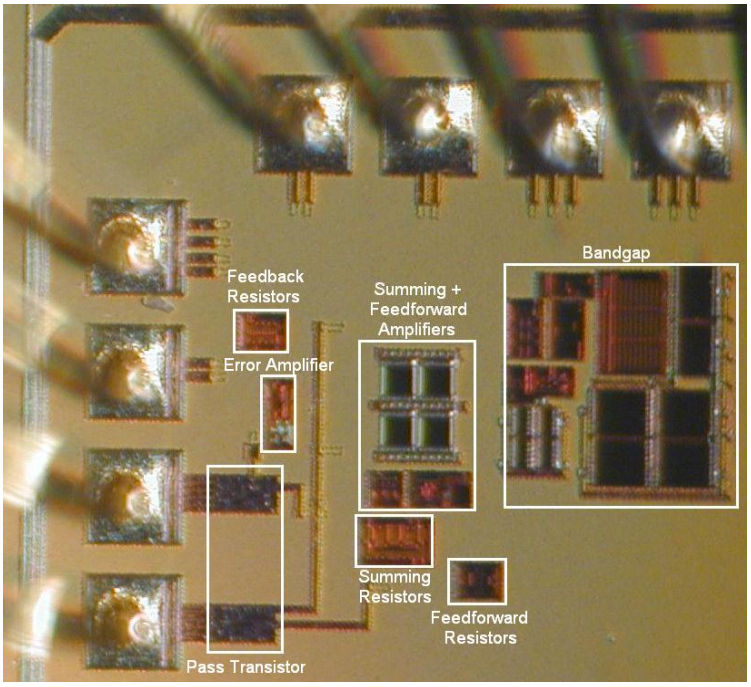


Fig. 2.16 Chip micrograph of the FFRC-LDO.

The PSR measurement setup is shown Fig. 2.17. The HP3588A spectrum analyzer with high input impedance (1MΩ) is used to measure the signal level at the input and output of the LDO. The PSR is measured by sweeping the frequency of an input sine wave across the band of interest. The sine wave at the input of LDO is adjusted to $0.1V_{pp}$ at each measurement point. The measured PSR for different load currents is shown in Fig. 2.18 for V_{DO} of 0.15V. The LDO achieves a worst PSR of -56dB at 10MHz for a load current of 25mA. For frequencies above 4MHz, the PSR starts to increase due to

internal poles of the feed-forward and summing amplifiers. The PSR at a load current of 25mA is worse than that at 5mA because the pass transistor is operating near the triode region. In this case, the channel conductance of the pass transistor is decreased, hence degrades the PSR. Increasing V_{DO} moves the operating point towards saturation, and a better PSR is achievable, as demonstrated in Fig. 2.19.

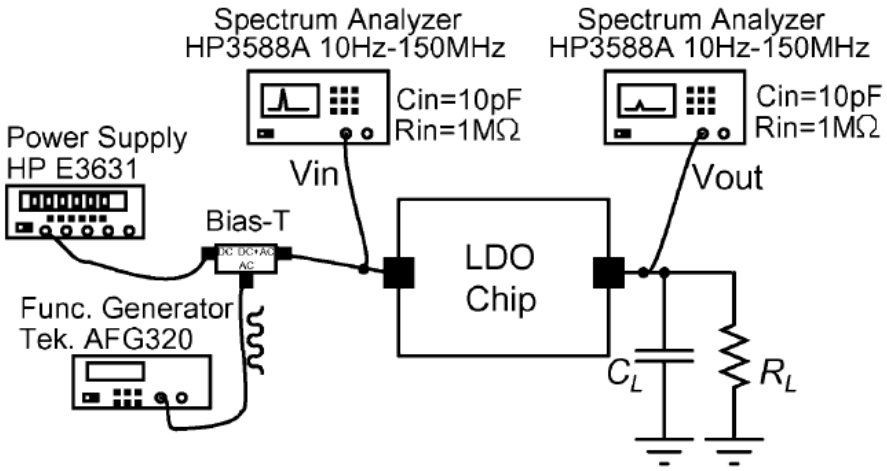


Fig. 2.17 PSR measurement setup.

For a conventional LDO with comparable performance at MHz frequencies, the open-loop gain and bandwidth should be increased, simultaneously. This increase comes at the cost of higher quiescent current as in [11], which is not the case using the FFRC technique.

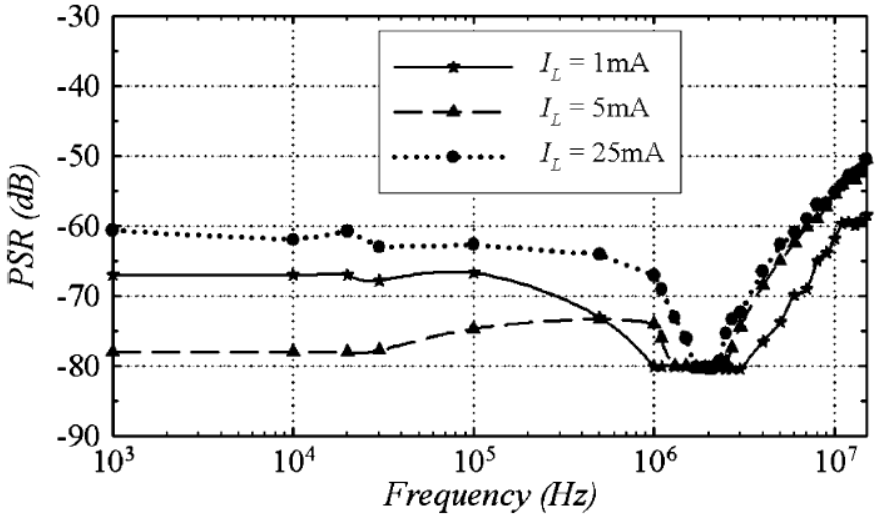


Fig. 2.18 Measured PSR for different load conditions (dropout voltage = 0.15V).

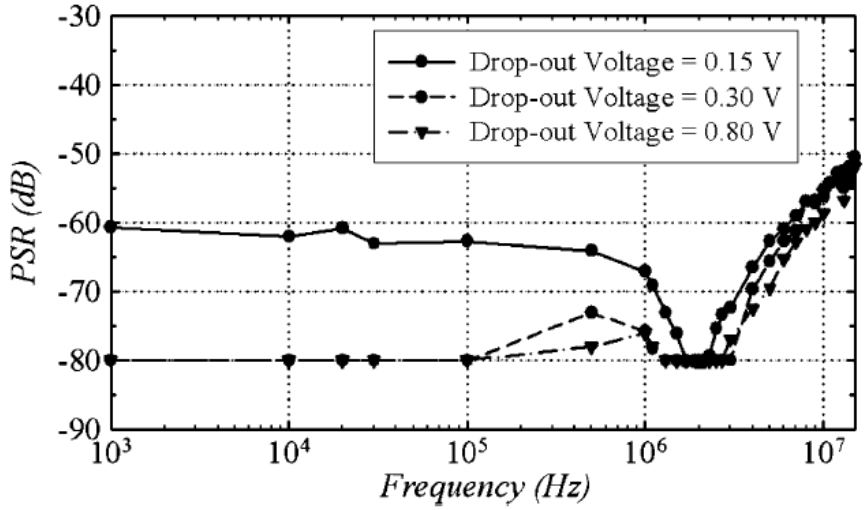


Fig. 2.19 Measured PSR for different dropout voltage (I_L = 25mA).

The load transient response is measured using the setup shown in Fig. 2.20. A switch, that is controlled by a clock, is used to switch the load current from minimum to maximum load current. Capacitor C_r is added to control the rise time of the load current.

Capacitor C_s is added to guarantee a clean ground at the input of the LDO. Also, this capacitor shorts any inductive effect due to the measurement cables. Fig. 2.21 shows the measurement results of the load transient response. A maximum overshoot of 15mV is achieved for a 25mA load current step with rise and fall times of 10ns. The FFRC technique does not degrade the load transient response, when compared to [6], because the high-current path does not include any additional device for isolation other than the main pass transistor. Finally, the line transient response for an input that varies from 1.15 to 1.8V is shown in Fig. 2.22.

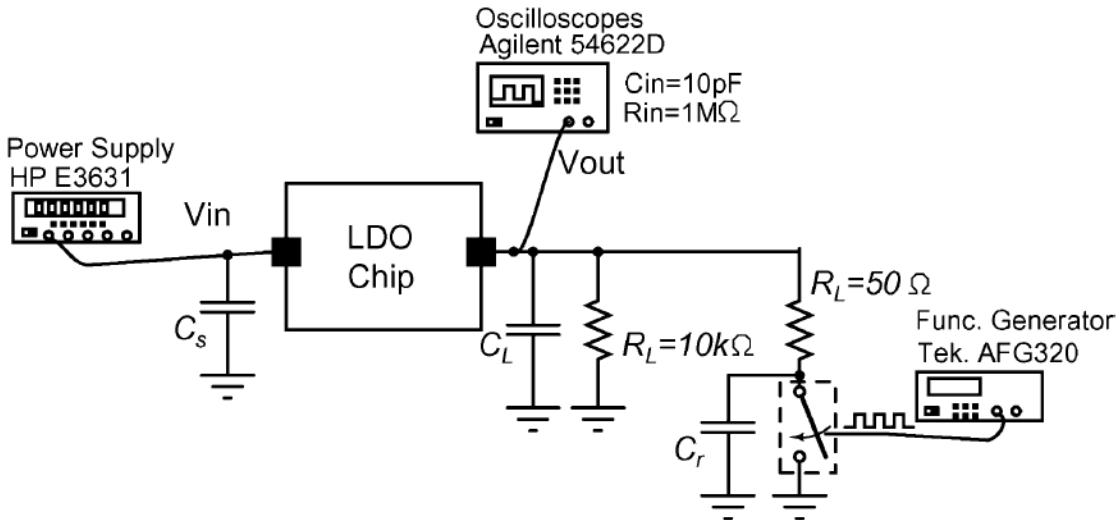


Fig. 2.20 Load transient measurement setup.

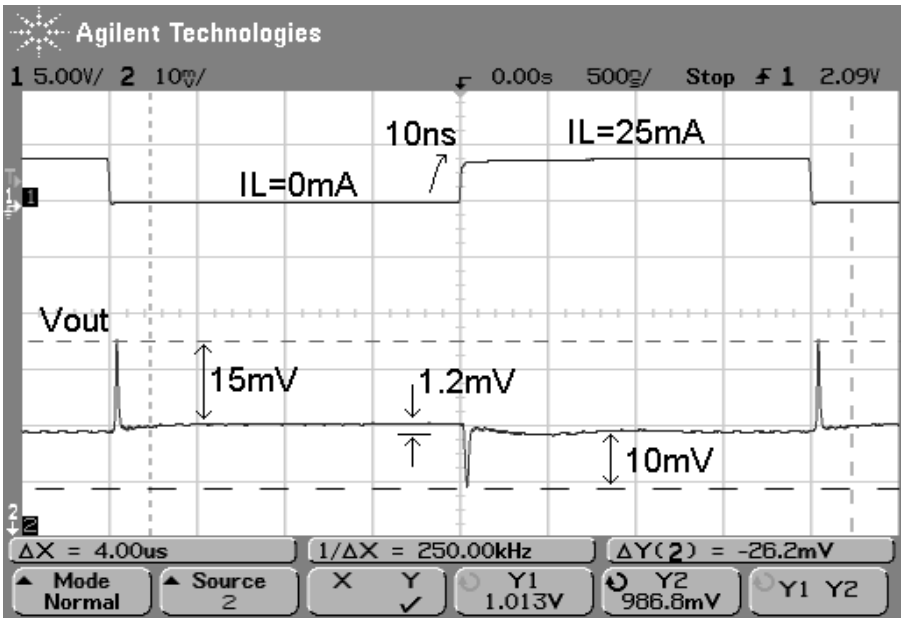


Fig. 2.21 Measured load transient response for a load current step of 25mA.

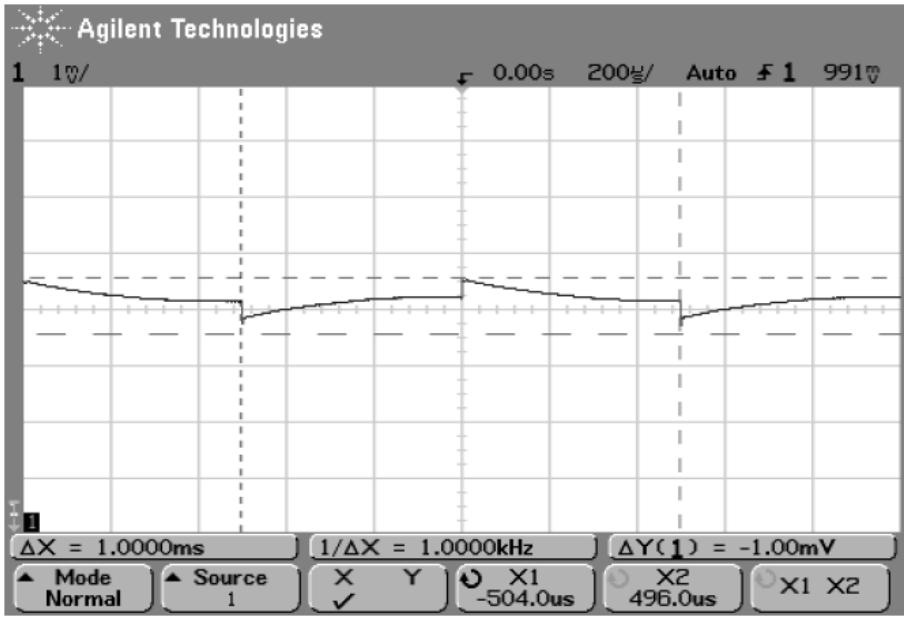


Fig. 2.22 Measured line transient response for an input voltage switching between 1.15 and 1.8V at load current of 25mA.

2.3 Adaptive Ripple Cancellation Technique

2.3.1 Basic Idea

In this technique, the input ripples flowing through both paths of transconductance and channel conductance of the pass transistor are cancelled in an adaptive way according to the load current value. This way high PSR can be achieved for a wider load current range compared to the previous technique.

The block diagram representation of the proposed LDO is shown in Fig. 2.23. As previously explained in the fundamental condition for PSR improvement, a feed-forward path with gain of $1+1/A_{MP}$ is required from the input to the pass transistor gate. This path can be divided into two paths with gains of 1 and $1/A_{MP}$ where the second is adaptively changing according to the load current.

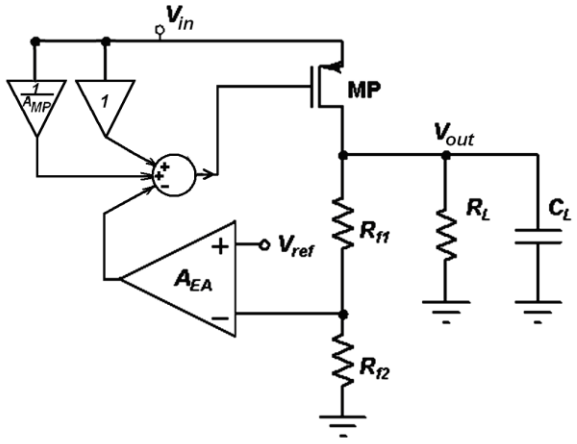


Fig. 2.23 Block diagram representation of the proposed LDO with adaptive ripple cancellation technique.

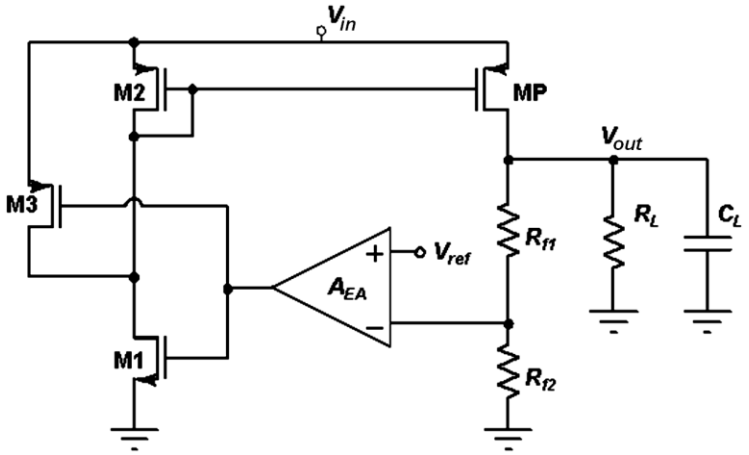


Fig. 2.24 Circuit level representation of the proposed LDO with adaptive ripple cancellation technique.

The LDO circuit level implementation is shown in Fig. 2.24. The diode-connected transistor M2 is used to provide the unity gain path as in [5] where a similar transistor is used within a voltage subtractor circuit to improve PSR. Another transistor M3 acting as an adaptive current source is introduced to provide an additional path for the input ripples to the pass transistor gate. M3 is responsible for providing the second path gain that has to be adaptive according to the gain of the pass transistor that is changing according to the value of the load current. In other words, M2 replicates the input ripples at the gate of the pass transistor, thus keeps V_{GS} free of ripples and accordingly removes the ripples due to the transconductance path of MP. On the other side, M3 provides an adaptive path from the input to the gate of MP to cancel the effect of the ripples leaking through its channel conductance which varies with load current. The following PSR analysis of the LDO is going to show the improvement gained in PSR over wide frequency range when using this technique in comparison to only using the diode-connected transistor. Also compared

to the previous technique of FFRC, this technique provides ripple cancellation through the two main paths of ripples in an adaptive way according to load current not relying on a fixed ratio between resistors to provide a fixed feed-forward gain. This allows the output load current range to be much wider. Additionally, the area required for the implementation of this technique is much smaller as no additional amplifiers are required other than the main error amplifier. Only three tiny transistors are added with no compensation capacitances needed. Moreover, the area required for implementing precise resistors is saved in this technique.

2.3.2 PSR Analysis

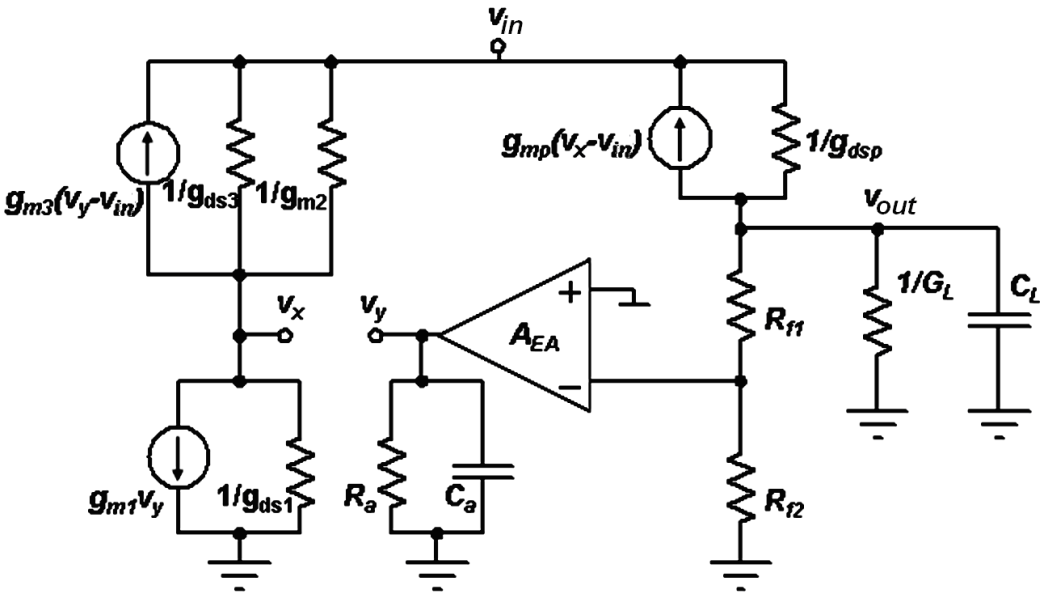


Fig. 2.25 Small signal model of the LDO using the adaptive technique.

The small signal model of the LDO is shown in Fig. 2.25. g_{m1}, g_{m2}, g_{m3}, and g_{mp} represent the transconductances of transistors M1, M2, M3, and MP (pass transistor)

respectively, while g_{ds1}, g_{ds3}, and g_{dsp} represent the channel conductances of M1, M3, and MP respectively. R_{f1} and R_{f2} are the feedback resistors while β is defined as the feedback factor $R_{f2}/(R_{f1}+R_{f2})$. The error amplifier gain is modeled as $A_{EA}/(1+sR_aC_a)$ where A_{EA} represents the DC gain while R_a and C_a represent the resistance and capacitance, respectively, of the dominant pole of amplifier located at its output node. G_L and C_L are the load conductance and capacitance, respectively. A small signal input voltage v_{in} will induce an output voltage v_{out}. The ratio between v_{out} and v_{in} simply represents the LDO PSR. v_{out} can be expressed as:

$$v_{out} = [g_{mp}(v_{in} - v_g) + g_{dsp}(v_{in} - v_{out})] \cdot Z_L, \tag{2.23}$$

where Z_L is the total impedance seen at the output of the LDO.

v_x and v_y are obtained as follows:

$$v_g = -\frac{g_{m1} + g_{m3}}{g_{m2} + g_{ds3} + g_{ds1}} v_{oEA} + \frac{g_{m2} + g_{m3} + g_{ds3}}{g_{m2} + g_{ds3} + g_{ds1}} v_{in}, \tag{2.24}$$

$$v_{oEA} = \frac{-\beta A_{EA}}{1 + sR_aC_a} v_{out}. \tag{2.25}$$

Then through neglecting g_{ds1} with respect to g_{m2} and g_{ds3} and substituting for v_{oEA} from (2.25) in (2.24), we get an approximate expression for v_g as follows:

$$v_g \cong \frac{g_{m1} + g_{m3}}{g_{m2} + g_{ds3}} \cdot \frac{\beta A_{EA}}{1 + sR_aC_a} v_{out} + \left(1 + \frac{g_{m3}}{g_{m2} + g_{ds3}}\right) v_{in}. \tag{2.26}$$

Now substituting for v_g from (2.26) in (2.23) and using $Y_L = 1/Z_L$, we rearrange (2.23) to get v_{out}/v_{in} as follows:

$$\frac{v_{out}}{v_{in}} = \frac{g_{dsp} - \dfrac{g_{mp} g_{m3}}{g_{m2} + g_{ds3}}}{Y_L + g_{dsp} + \dfrac{g_{m1} + g_{m3}}{g_{m2} + g_{ds3}} \cdot \dfrac{g_{mp} \beta A_{EA}}{1 + sR_aC_a}}. \tag{2.27}$$

Y_L can be approximated to $G_L + sC_L$ given that the feedback resistors R_{f1} and R_{f2} are large enough to be ignored. Hence, the LDO DC open loop gain A_{ol} is given by:

$$A_{ol} = \frac{g_{m1} + g_{m3}}{g_{m2} + g_{ds3}} \cdot \frac{g_{mp}}{G_L + g_{dsp}} \cdot \beta A_{EA}. \tag{2.28}$$

Now, defining A_0 as:

$$A_0 = \frac{g_{dsp} - \frac{g_{mp} g_{m3}}{g_{m2} + g_{ds3}}}{G_L + g_{dsp}}, \tag{2.29}$$

We can simplify (2.27) as follows:

$$\frac{v_{out}}{v_{in}} = \frac{A_0}{1 + \frac{sC_L}{G_L + g_{dsp}} + \frac{A_{ol}}{1 + sR_a C_a}}, \tag{2.30}$$

which is rewritten as:

$$\frac{v_{out}}{v_{in}} = \frac{A_0}{(1 + A_{ol})} \cdot \frac{(1 + sR_a C_a)}{1 + s\frac{\left(\frac{C_L}{G_L + g_{dsp}} + R_a C_a\right)}{1 + A_{ol}} + s^2 \frac{\left(\frac{C_L}{G_L + g_{dsp}} \cdot R_a C_a\right)}{1 + A_{ol}}}. \tag{2.31}$$

Now for PSR at DC:

$$\frac{v_{out}}{v_{in}}|_{DC} = \frac{A_0}{(1 + A_{ol})} = \frac{g_{dsp} - \frac{g_{mp} g_{m3}}{g_{m2} + g_{ds3}}}{(G_L + g_{dsp})(1 + A_{ol})}. \tag{2.32}$$

or in a simpler form with $R_L = 1/G_L$ and $r_{dsp} = 1/g_{dsp}$:

$$\frac{v_{out}}{v_{in}}|_{DC} = \frac{1 - \frac{g_{mp} r_{dsp} g_{m3}}{g_{m2} + g_{ds3}}}{(1 + \frac{r_{dsp}}{R_L})(1 + A_{ol})}. \tag{2.33}$$

In case of having only the diode-connected transistor M2 as in [5] without M3, the PSR at DC can be evaluated by simply setting $g_{m3} = g_{ds3} = 0$ in (2.33):

$$\frac{v_{out}}{v_{in}}|_{DC\_noM3} = \frac{1}{(1+\frac{r_{dsp}}{R_L})(1+A_{ol})}, \tag{2.34}$$

with only a slight change in A_{ol} on setting $g_{m3} = g_{ds3} = 0$ in (2.33). In this case, the PSR at DC can be enhanced only through increasing the open loop gain A_{ol} which will be at the expense of power consumption. On the contrary, for our proposed technique, the PSR at DC can be significantly enhanced if the numerator of (2.33) is set as close as possible to zero. We can simply interpret this condition as:

$$A_{MP} \cdot A_{M3} = 1, \tag{2.35}$$

where A_{MP} is the intrinsic pass transistor gain ($g_{mp}r_{dsp}$) while A_{M3} is the gain provided by M3 ($g_{m3}/(g_{m2}+g_{ds3})$). So, M3 has to provide the reciprocal of the gain provided by the pass transistor in an adaptive way with the load current variation. As the load current decreases, A_{MP} increases while the currents in M1 and M2 decreases. Thus, $|V_{GS1}|$ and $|V_{GS2}|$ decrease causing $|V_{GS3}|$ to increase and $|V_{DS3}|$ to decrease. As a result, M3 moves towards the triode region and its gain A_{M3} decreases. Thus, the multiplication of the two gains A_{MP} and A_{M3} is designed to be as close as possible to unity for a better PSR at DC and low frequencies.

Now for higher frequencies, it is noted from (2.31) that there are two poles and one zero in the PSR transfer function. We can differentiate between two different cases:

A. The output pole is the dominent one

Now with $C_L/(G_L+g_{dsp}) >> R_aC_a$, (2.31) can be rewritten as:

$$\frac{v_{out}}{v_{in}} = \frac{A_0}{(1+A_{ol})} \cdot \frac{(1+sR_aC_a)}{\left(1+s\frac{C_L}{(1+A_{ol})(G_L+g_{dsp})}\right)(1+sR_aC_a)}, \tag{2.36}$$

where the zero will cancel a pole and there will be only one pole remaining at the gain-bandwidth product of the loop (GBW = $A_{ol}(G_L+g_{dsp})/C_L$). So, ideally the PSR should be continuously improving after the GBW. However, the capacitor will start to behave as an inductor above $f_{resonance}$ and so the PSR will start to degrade as the frequency increases. The PSR variation with frequency in this case can be represented by the solid curve in Fig. 2.26.

B. The internal pole is the dominent one

Now with $R_aC_a >> C_L/(G_L+g_{dsp})$, (2.31) can be rewritten as:

$$\frac{v_{out}}{v_{in}} = \frac{A_0}{(1+A_{ol})} \cdot \frac{(1+sR_aC_a)}{\left(1+s\frac{R_aC_a}{1+A_{ol}}\right)\left(1+s\frac{C_L}{G_L+g_{dsp}}\right)}, \tag{2.37}$$

where the PSR transfer function will have a zero at the dominant pole ($1/R_aC_a$) at which PSR will start to degrade. The zero is then followed by a pole at the GBW (GBW = A_{ol}/R_aC_a), and then comes the non dominant pole at the output ($(G_L+g_{dsp})/C_L$) before finally the PSR will start degrading above $f_{resonance}$. The PSR in this case can be represented by the dotted curve in Fig. 2.26.

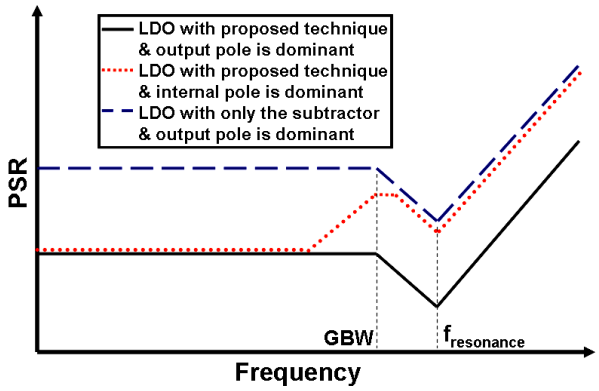


Fig. 2.26 PSR curves for comparison between three different cases.

As a conclusion from this analysis, the best PSR performance occurs when the pole at the output is the dominant one. So, the error amplifier should have a wide bandwidth. However, the amplifier does not need to have an especially large gain since the input ripples suppression can be enhanced significantly through minimizing A_0 rather than increasing A_{ol}. If same wideband error amplifier is used within an LDO with dominant pole at the output while only a diode-connected transistor is used as a subtractor for PSR improvement, then the PSR of this LDO can be represented by the dashed curve in Fig. 2.26. In this case, the PSR at DC will be equal to that in (2.34) and the whole PSR curve will be shifted upwards compared to the PSR curve using the proposed technique.

2.3.3 Circuit Implementation

The LDO is implemented using 90nm digital CMOS process. The error amplifier uses current sources with improved output impedance as active loads [10] as shown in Fig. 2.27. This is the same topology used in the error amplifier in the FFRC technique. The amplifier achieves a gain of 43dB and a -3-dB frequency of 3.3MHz while

consuming a current of 25µA with no internal compensation capacitance required. It achieves a PSRR of 100dB at DC and better than 78dB up to its -3-dB frequency. Therefore, the amplifier PSRR is not limiting the PSR of the LDO and this justifies the validity of ignoring the amplifier PSRR in the analysis in previous section.

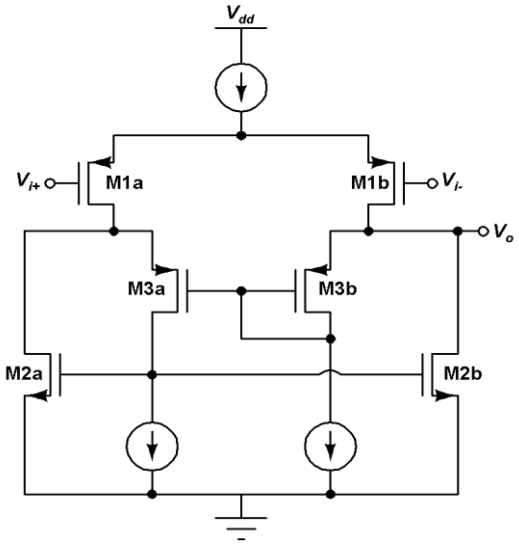


Fig. 2.27 Schematic of the error amplifier.

The LDO die photo is shown in Fig. 2.28 where it occupies an active area of only 0.015mm^2. Two off-chip load capacitors of 3µF each are used in parallel.

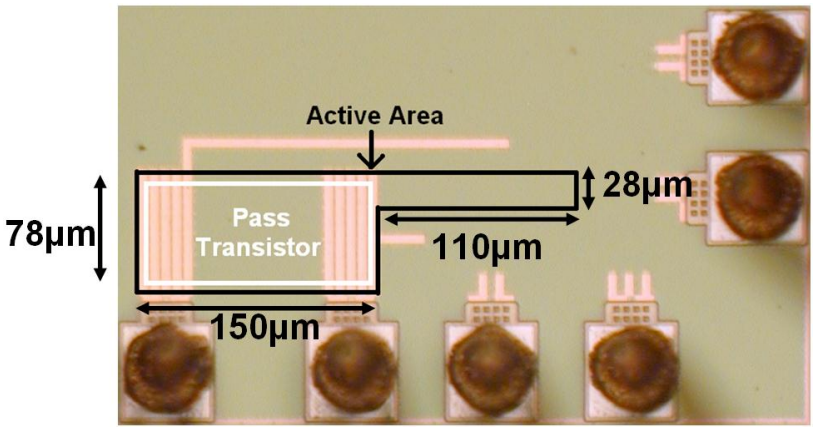


Fig. 2.28 Die photo of the LDO.

2.3.4 Measurement Results

Similar to previous FFRC-LDO, PSR is measured using the setup in Fig. 2.17 through injecting a sine wave of $0.1V_{pp}$ at the input of the LDO and sweeping its frequency across the band of interest. The measured PSR for different load currents is shown in Fig. 2.29 for a regulated output voltage of 1V with V_{DO} of 0.15V. A PSR of -56dB is achieved at 10MHz and its worst case below this frequency is -50dB across the wide load current range of 140mA. As expected, the best PSR is at $f_{resonance}$ of the load capacitor that is slightly lowered to 2.3MHz due to the trace parasitics. To get -50dB of PSR at even higher frequencies of tens of MHz it is then required to increase the loop gain so that the whole PSR curve is shifted down. This is of course needs high quiescent power consumption leading to efficiency degradation.

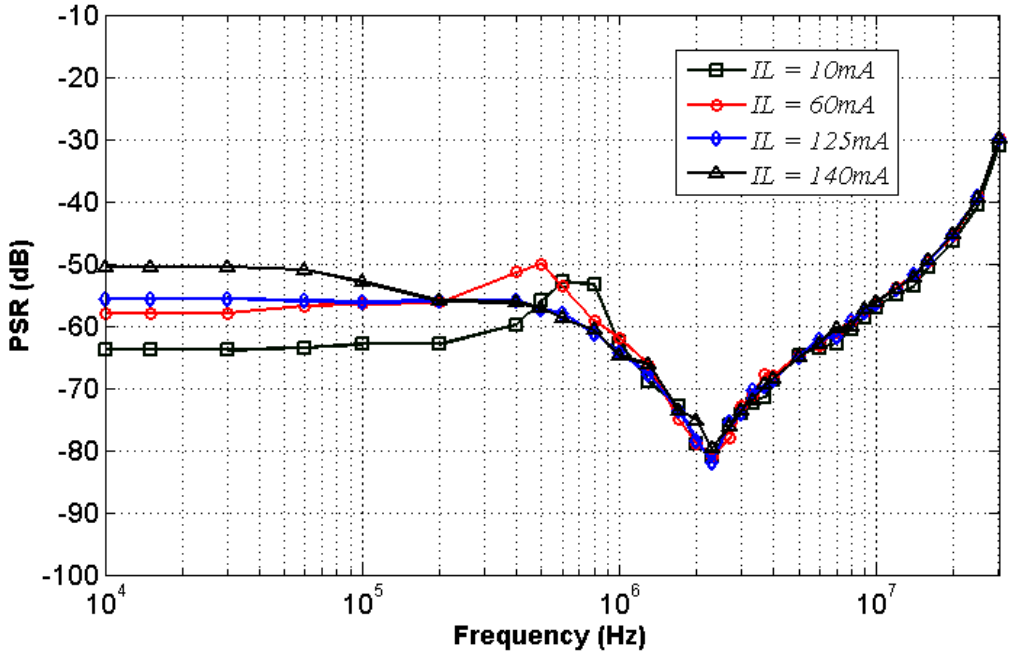


Fig. 2.29 Measured PSR for different load currents.

Load transient response is measured using setup similar to the one in Fig. 2.20 through adding a switch to ground in series with the minimum load resistance. Measurement results are shown in Fig. 2.30. The load regulation is only 0.0428mV/mA (6mV/140mA) with maximum overshoots of 24mV and undershoots of 70mV.

2.4 Comparison with Previously Reported Techniques

Table 2.1 shows a comparison between the two proposed LDOs, FFRC-LDO and Adaptive-LDO, and three relevant recently published LDOs.

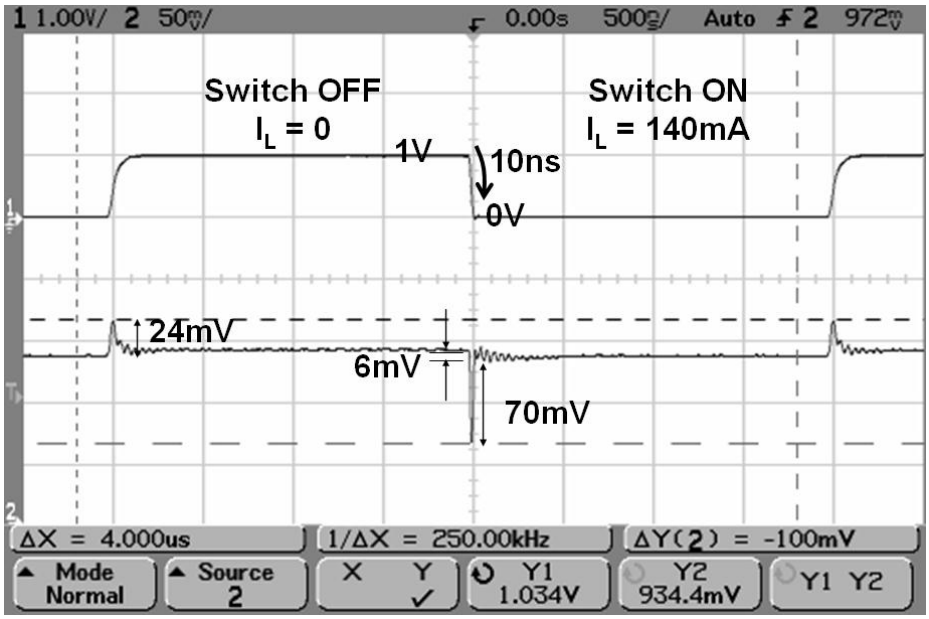


Fig. 2.30 Measured load transient response. Upper waveform is the voltage at the output of the switch connecting the minimum load to ground. Lower waveform is the load transient response for 140mA step in current.

Table 2.1 Performance summary and comparison with recently published LDO regulators.

	Unit	[5]	[6]	[11]	FFRC-LDO [7,8]	Adapt.-LDO [9]
Technology	µm	0.35	0.6	0.35	0.13	0.09
Active Area	mm^2	0.26	NA	0.053	0.049	0.015
V_{in}	V	> 3.05	> 1.8	> 1.05	> 1.15	> 1.15
V_{out}	V	2.8	1.2	0.9	1	1
Dropout Voltage	mV	> 0.25	> 0.6	> 0.15	> 0.15	> 0.15
Maximum Load	mA	100	5	50	25	140
I_Q	µA	NA*	70	4.04 to 164	42	33 to 145
Current Efficiency	%	NA	99.72	99.67	98.3	99.9
PSR @ 100KHz	dB	-56	-63	-50	-60	-53
PSR @ 1MHz	dB	NA	-40	-50	-67	-62
PSR @ 10 MHz	dB	NA	-27	NA	-56	-56
Load Regulation	mV/mA	0.06	34.2	0.0614	0.048	0.043

*I_Q is not reported but it is mentioned to be comparable to a commercial product (LP2895), which has I_Q of 75 to 850µA for I_L of 1 to 150mA [5]

Reference [5] is using only the diode-connected transistor as a subtractor replicating the input ripples at the gate of the pass-transistor. The LDO in [5] uses a two stage amplifier with internal compensation capacitors to achieve high open loop gain for better PSR. This comes at the cost of high power and area consumption. It achieves a good PSR at low frequencies and it starts degrading with frequency as the dominant pole of the LDO is at an internal node while an off-chip load capacitor of 1µF is being used. Comparing the two proposed techniques, the adaptive-LDO can achieve a slightly lower PSR at lower frequencies but for a load current range that is more than five times larger since I_{Lmax} is limited to only 25mA in FFRC-LDO. Adaptive-LDO consumes an active area that is less than one third of that in FFRC-LDO as there is no need for on-chip large resistors or compensation capacitors or extra amplifiers other than the error amplifier. In addition, adaptive-LDO achieves a slightly better load regulation and current efficiency ($I_{Lmax}/(I_{Lmax}+I_Q)$) where it consumes a quiescent current that varies adaptively from 33µA at no load to 145µA at maximum load condition.

2.5 Conclusion

In this chapter, two different high performance LDOs of high PSR at high frequencies up to 10MHz are presented. Complete PSR analysis is included together with detailed measurement results. A comparison with previously reported designs shows how the proposed designs achieve the best PSR performance with the smallest dropout voltage without sacrificing efficiency or transient response.

CHAPTER III

OUTPUT-CAPACITORLESS LDO REGULATOR USING MINIMUM ON-CHIP CAPACITANCE WITH HIGH PSR AND FAST TRANSIENT RESPONSE

3.1 Introduction

For compact System-on-Chip (SoC) solutions, the design of highly efficient LDOs without using bulky off-chip output filtering capacitors has recently gained a lot of interest [6, 12-16]. This becomes a very important requirement specifically in large systems employing tens of on-chip LDOs. Having a pin per each off-chip output capacitor is not affordable in terms of area and cost. In addition to the main LDO requirements of having good load regulation and high efficiency, with small quiescent current and low dropout voltage, additional challenges have to be specifically considered for output-capacitorless (OCL) LDOs. With a small equivalent output capacitor that is typically in the order of pF, ensuring the OCL-LDO stability at light loads becomes difficult to accomplish. That is because the dominant pole in an OCL-LDO is no longer at its output like a normal LDO with large off-chip output capacitor. The dominant pole of an OCL-LDO is at an internal node. Thus, at light loads (high output resistance) the output non-dominant pole approaches the internal dominant one causing stability problems. Another key challenge in OCL-LDOs is to minimize the on-chip compensation capacitance ($C_{on\text{-}chip}$). Using small $C_{on\text{-}chip}$ reduces the required silicon area, speeds up the transient response and improves the power supply rejection (PSR) at high frequencies. A high PSR is a vital aspect in the design of an LDO to attenuate any input supply ripples.

This becomes more pronounced at high frequencies with the continuous increase in the switching frequencies of the switching DC-DC converters which usually precede the LDOs. Using higher switching frequencies, switching converters also target higher level of integration with small passive components as well as fast transient response [14].

3.1.1. Previous Work on Capacitorless LDOs

One of the earliest works on OCL-LDOs employs damping-factor-control frequency compensation technique [12] as shown in Fig. 3.1. This technique uses three capacitors with total $C_{on\text{-}chip}$ of 12pF and it can stabilize the OCL-LDO down to a significant minimum load current (I_{Lmin}) of 10mA. Q-reduction technique shown in Fig. 3.2 is then employed in [13] to lower I_{Lmin} to 100µA using smaller $C_{on\text{-}chip}$ of 6pF. This comes on the expense of higher I_Q and worse load regulation. Another solution uses a large on-chip decoupling capacitor of 600pF to stabilize the OCL-LDO [14]. This huge capacitor consumes large silicon area and the LDO consumes high I_Q degrading its efficiency.

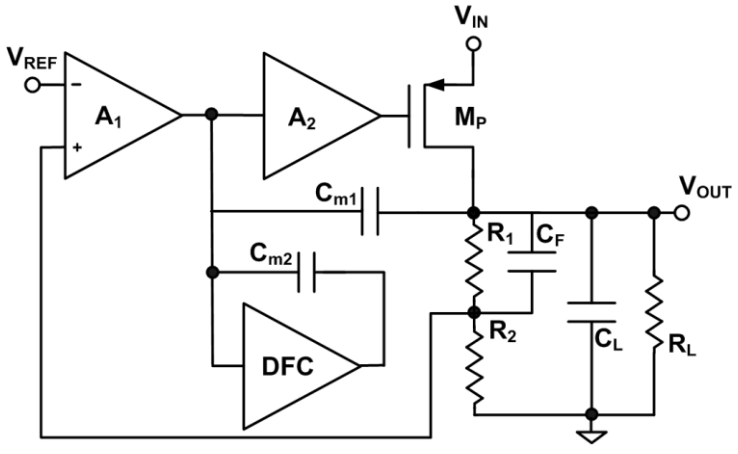


Fig. 3.1 OCL-LDO using damping-factor-control frequency compensation.

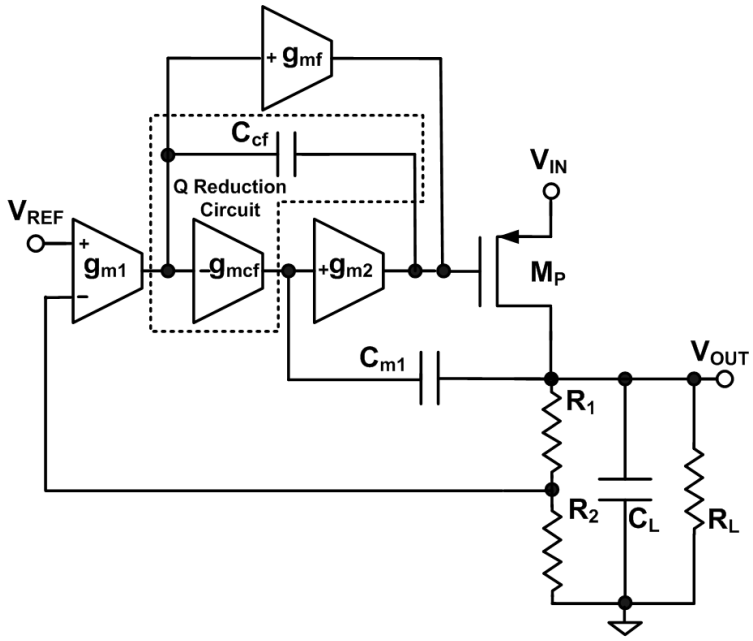


Fig. 3.2 OCL-LDO using Q-reduction circuit technique.

The first OCL-LDO targeting high PSR at MHz frequencies is proposed in [6]. This Miller-compensated OCL-LDO shown in Fig. 3.3 utilizes $C_{on\text{-}chip}$ of 60pF. Most of this capacitance (45pF) is employed in a charge pump and a filter used to bias an NMOS transistor in cascode with the main PMOS pass transistor to shield the regulator from supply noise. This technique does improve the PSR, though it suffers from large V_{DO}, degraded load regulation, and large voltage undershoots in the load transient. Additionally, the maximum load current (I_{Lmax}) for this OCL-LDO is only 5mA.

To enhance the transient response for OCL-LDOs, two different techniques were recently proposed [15,16]. In [15], a high-speed loop is used in addition to the main loop while in [16] an LDO core based on flipped voltage follower [17] is employed with low

I_Q but with slightly large I_{Lmin} of 3mA. Still both techniques [15,16] show degraded PSR and slow settling time ($T_{settling}$) while employing a relatively large $C_{on\text{-}chip}$ of 7pF.

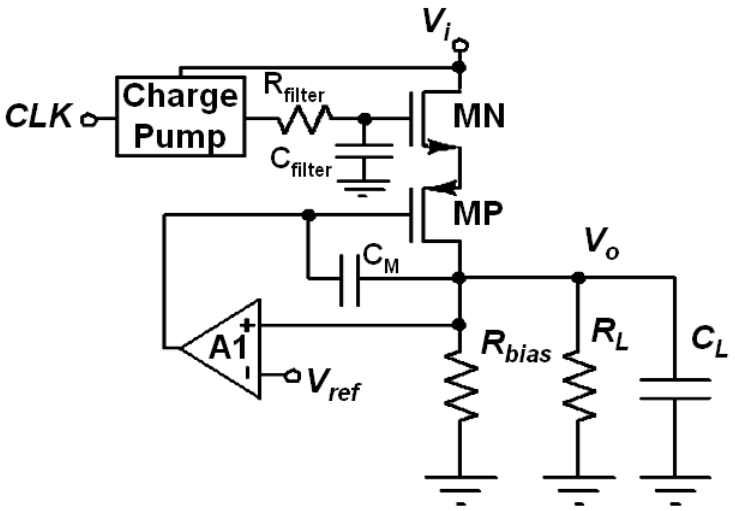


Fig. 3.3 OCL-LDO with high PSR.

Hence, all these previous works provide partial solutions to the OCL-LDO specific challenges in terms of light load stability, small $C_{on\text{-}chip}$, fast transient response and high PSR at high frequencies.

3.1.2. Proposed Solution

In this chapter, we present an OCL-LDO with a simple architecture that simultaneously ensures stability at light loads, uses small $C_{on\text{-}chip}$ (< 1pF), occupies small silicon area, achieves fast transient response, and provides PSR better than -50dB up to 1MHz. Additionally, the OCL-LDO maintains the essential features of a highly efficient LDO with low V_{DO} and low I_Q, that is adaptive to I_L, together with excellent load and line regulations.

3.2 Proposed Capacitorless LDO

3.2.1. Basic Concept

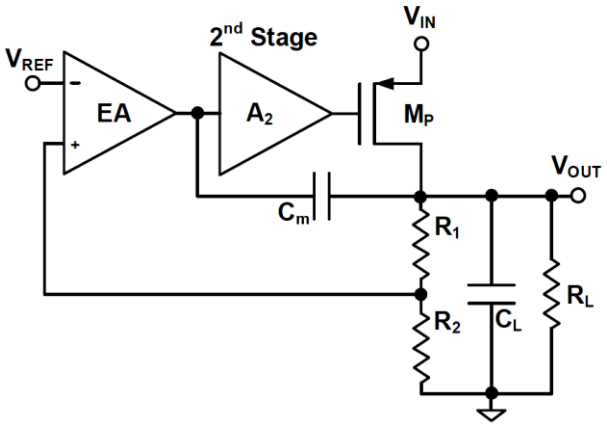


Fig. 3.4 Conceptual diagram of a conventional Miller-compensated OCL-LDO.

Fig. 3.4 shows the conceptual diagram of a conventional Miller-compensated OCL-LDO where the compensation capacitor C_m is added between the output of the high gain error amplifier (EA) and the output of the LDO for pole splitting. If the EA directly drives the pass transistor or if a second stage that is just a buffer follows the EA, this will result in a relatively small Miller multiplication factor and thus a large C_m is required for wider pole splitting. On the other hand, if the second stage following the EA is another high gain stage then the Miller multiplication factor is increased but non-dominant complex poles with large quality factor (Q) will appear close to the gain-bandwidth product frequency (ω_{GBW}) of the loop at light load condition [13]. This will cause magnitude peaking near ω_{GBW} leading to instability of the OCL-LDO at light loads. Thus, to reduce the minimum required output current of the OCL-LDO, large C_m is to be

employed again to lower ω_{GBW} of the loop sufficiently below the frequency of the complex poles (ω_o). Large C_m will result in consuming excessive area and degrading the transient response and PSR of the LDO.

In our proposed OCL-LDO shown in Fig. 3.5, C_m is differently added between the LDO output and an internal node of the EA so that a portion of the EA high gain is used in the Miller multiplication factor and is also used to push ω_o to high frequency. In addition, the second stage gain (A_2) is adaptively changed according to I_L. As I_L decreases and the pass transistor gain increases, oppositely A_2 decreases and also Q of the non-dominant complex poles is reduced. These effects on both ω_o and Q will be further explained and verified through the OCL-LDO stability analysis in the next section. Therefore, a smaller C_m can be employed for easier light load compensation and better transient response. A tiny capacitor C_c is used to place the dominant pole of the EA at its internal high impedance node and R_c is added to create a zero that cancels the pole at the EA output node.

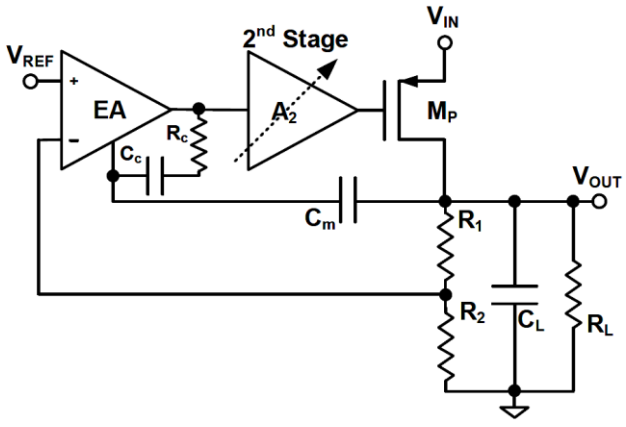


Fig. 3.5 Conceptual diagram of the proposed OCL-LDO.

3.2.2. Stability Analysis

Fig. 3.6 shows the circuit schematic of the EA employed in our OCL-LDO. The EA topology has voltage gain boost employing current sources with improved output impedance as active loads [10]. Compared to a conventional two-stage amplifier, this EA topology achieves much better power supply rejection ratio (PSRR) so as not to degrade the overall PSR of the OCL-LDO.

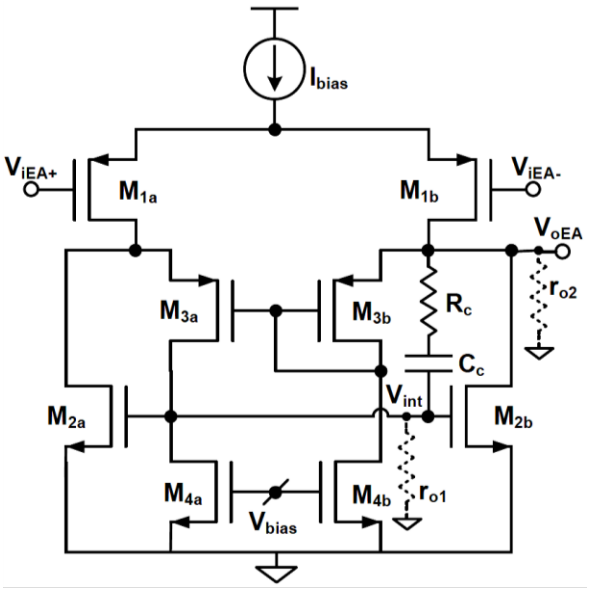


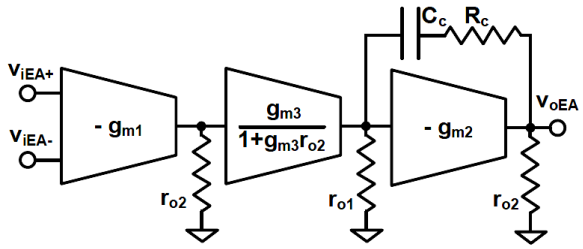
Fig. 3.6 Circuit schematic of the error amplifier.

The small signal model of the EA is shown in Fig. 3.7(a) where it can be decomposed into three stages where g_{m1}, g_{m2} and g_{m3} represent the transconductances of transistors M1, M2 and M3, respectively, while r_{o1} and r_{o2} represent the total equivalent resistances at the two high impedance nodes of the EA. The second source degenerated

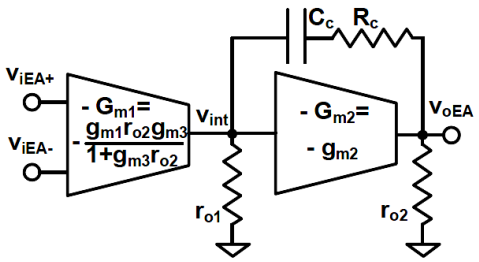
stage can be combined with the first stage for a simpler representation in Fig. 3.7(b) with only two stages of transconductances G_{m1} and G_{m2} defined as follows:

$$G_{m1} = \frac{g_{m1} r_{o2} g_{m3}}{1 + g_{m3} r_{o2}}, \qquad G_{m2} = g_{m2}. \tag{3.1}$$

Using this EA, the circuit schematic of the proposed OCL-LDO is shown in Fig. 3.8. The second stage following the EA is composed of three transistors (M5 to M7). The diode connected transistor M7 transfers the change in I_L into the second stage to bias it accordingly. r_{o3} represents the total output resistance of the second stage. C_3 represents the total parasitic capacitance to ground at the gate of the large pass transistor while C_{gd} represents its gate-drain capacitance where the parasitic capacitances at all other nodes can be neglected compared to C_m and C_c.



(a)



(b)

Fig. 3.7 (a) Small signal model of the error amplifier, (b) A simplified model.

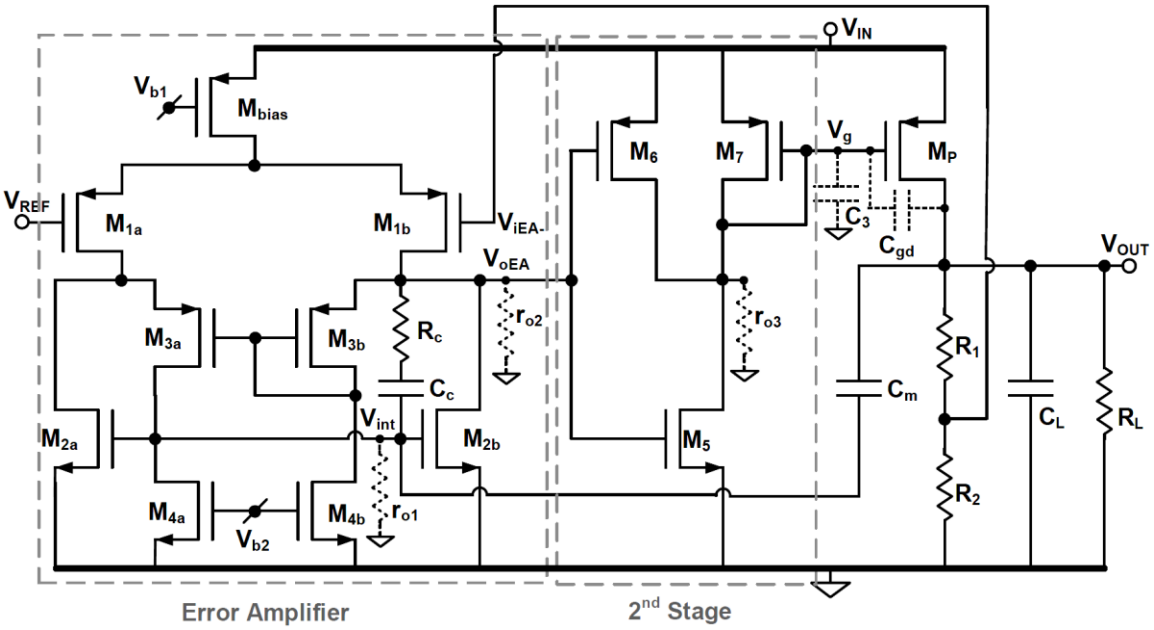


Fig. 3.8 Circuit schematic of the proposed OCL-LDO.

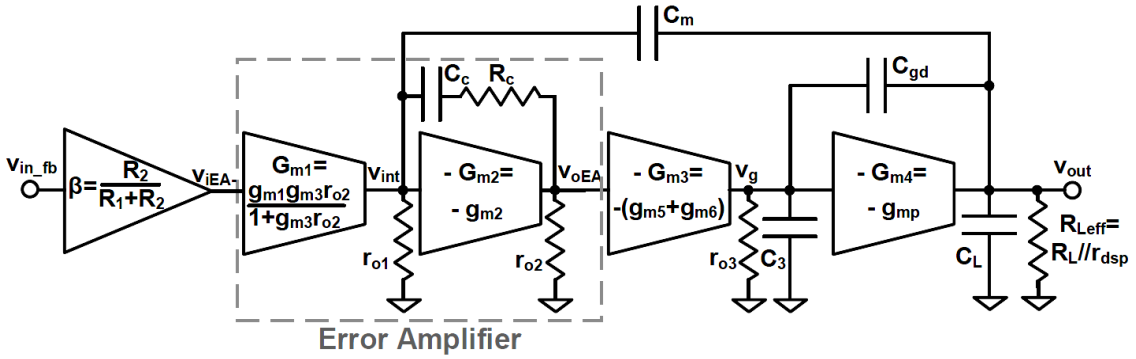


Fig. 3.9 Open-loop small signal model of the proposed OCL-LDO.

Including the simplified EA small signal model in Fig. 3.7(b), the OCL-LDO open-loop small signal model is drawn in Fig. 3.9 where g_{m5}, g_{m6}, g_{m7}, and g_{mp} represent the transconductances of transistors M5, M6, M7 and MP, respectively. $\beta = R_2/(R_1+R_2)$ is the feedback ratio. $R_{Leff} = R_L//r_{dsp}$ is the effective output resistance of the LDO neglecting

the large feedback resistors R_1 and R_2 where r_{dsp} is the output resistance of MP. To simplify the analysis, G_{m3} and G_{m4} are defined as:

$$\begin{aligned} G_{m3} &= g_{m5} + g_{m6}, \\ G_{m4} &= g_{mp}. \end{aligned} \tag{3.2}$$

The OCL-LDO open loop transfer function, from Fig. 3.9, can be approximated as:

$$\frac{v_{out}}{v_{in\_fb}} \approx \frac{-A_0\left(1-\frac{C_{gd}}{G_{m4}}s-\frac{C_m(C_{gd}+C_3)}{G_{m2}r_{o2}G_{m3}G_{m4}}s^2\right)}{\left(1+\frac{s}{\omega_{3dB}}\right)\cdot F(s)} \tag{3.3}$$

where

$$F(s)=1+\frac{(C_L+C_{gd})R_{Leff}+(C_3+C_{gd})r_{o3}+C_{gd}r_{o3}R_{Leff}(G_{m4}-G_{m3}G_{m2}r_{o2})}{G_{m2}r_{o2}G_{m3}r_{o3}G_{m4}R_{Leff}}s+\frac{C_L(C_3+C_{gd})}{G_{m2}r_{o2}G_{m3}G_{m4}}s^2 \tag{3.4}$$

while the dc loop gain (A_0) and the -3dB dominant pole frequency (ω_{3dB}) are given as:

$$A_0 = \beta G_{m1}r_{o1}G_{m2}r_{o2}G_{m3}r_{o3}G_{m4}R_{Leff}, \tag{3.5}$$

$$\omega_{3dB} = 1/r_{o1}C_mG_{m2}r_{o2}G_{m3}r_{o3}G_{m4}R_{Leff}, \tag{3.6}$$

and thus

$$\omega_{GBW} = A_0 \cdot \omega_{3dB} = \beta G_{m1}/C_m. \tag{3.7}$$

Now we can differentiate between two practical cases:

First case is at heavy load condition where G_{m4} is large while R_{Leff} is small. With small C_m and large G_{m4}, the two zeros in the transfer function are located at high frequencies and can be neglected. Thus, (3.3) can be simplified to:

$$\frac{v_{out}}{v_{in\_fb}} \approx \frac{-A_0}{\left(1+\frac{s}{\omega_{3dB}}\right)\left(1+\frac{C_{gd}}{G_{m2}r_{o2}G_{m3}}s+\frac{C_L(C_3+C_{gd})}{G_{m2}r_{o2}G_{m3}G_{m4}}s^2\right)}, \tag{3.8}$$

which can be further approximated to:

$$\frac{v_{out}}{v_{in\_fb}} \approx \frac{-A_0}{\left(1+\frac{s}{\omega_{3dB}}\right)\left(1+\frac{C_{gd}}{G_{m2}r_{o2}G_{m3}}s\right)\left(1+\frac{C_L(C_3+C_{gd})}{G_{m4}C_{gd}}s\right)}. \tag{3.9}$$

Then other than the dominant pole at ω_{3dB}, there exist two other real poles located at high frequencies compared to ω_{GBW}.

Second case is at light load condition where G_{m4} is small while R_{Leff} is large. The two zeros can still be neglected as they are located at frequencies fairly above ω_{GBW} due to having the gain term ($G_{m2}r_{o2}$) that is the gain of the last stage of the EA. This is verified by the simulated open-loop frequency response of the OCL-LDO. Now (3.3) can be approximated to:

$$\frac{v_{out}}{v_{in\_fb}} \approx \frac{-A_0}{\left(1+\frac{s}{\omega_{3dB}}\right)\left(1+\frac{C_L+C_{gd}+C_{gd}r_{o3}(G_{m4}-G_{m3}G_{m2}r_{o2})}{G_{m2}r_{o2}G_{m3}r_{o3}G_{m4}}s+\frac{C_L(C_3+C_{gd})}{G_{m2}r_{o2}G_{m3}G_{m4}}s^2\right)} \tag{3.10}$$

Other than the dominant pole, there is a pair of complex poles with ω_o and Q defined as follows:

$$\omega_o = \sqrt{\frac{G_{m2}r_{o2}G_{m3}G_{m4}}{C_L(C_3+C_{gd})}}, \tag{3.11}$$

$$Q = \frac{r_{o3}\sqrt{G_{m2}r_{o2}G_{m3}G_{m4}(C_3+C_{gd})C_L}}{C_L+C_{gd}+C_{gd}r_{o3}(G_{m4}-G_{m2}r_{o2}G_{m3})}. \tag{3.12}$$

Compared to the Q-reduction technique used in [13], ω_o is pushed to high frequency above ω_{GBW} by including the square root of the gain term ($G_{m2}r_{o2}$). Moreover, Q is proportional to r_{o3} at light loads when r_{o3} decreases significantly due to having the stage following the EA adaptively biased according to I_L. As I_L decreases, $|V_{GS5}|$ and $|V_{GS7}|$ decrease causing $|V_{GS6}|$ to increase and $|V_{DS6}|$ to decrease. Consequently, M6 moves towards the triode region; its output resistance decreases; and thus, r_{o3} and Q decrease. Therefore, the magnitude peaking is significantly suppressed. Furthermore, since both G_{m4} and G_{m3} decrease as I_L decreases and with the significant reduction in r_{o3}, the s term in the second order function in the denominator of (3.10) remains positive. This avoids having any right-half-plane poles that cause instability in the system [18]. Thus, employing this simple adaptive biasing technique is the key to stabilize the OCL-LDO at light load condition.

3.2.3. PSR Analysis

The PSR for the simplest Miller-compensated OCL-LDO shown in Fig. 3.10 is analyzed in [19] where, for frequencies below ω_{GBW} of the loop, the PSR transfer function can be given as:

$$\begin{aligned} \frac{v_{out}}{v_{in}} &= \frac{1+sg_{mp}r_{dsp}R_{oEA}(C_m+C_{gd})}{g_{mp}r_{dsp}G_{mEA}R_{oEA}} && \text{for an EA of type-A,} \\ \frac{v_{out}}{v_{in}} &= \frac{1+sR_{oEA}(C_m+C_{gd})}{G_{mEA}R_{oEA}} && \text{for an EA of type-B,} \end{aligned} \tag{3.13}$$

where G_{mEA} and R_{oEA} are the transconductance and output resistance of the EA, respectively.

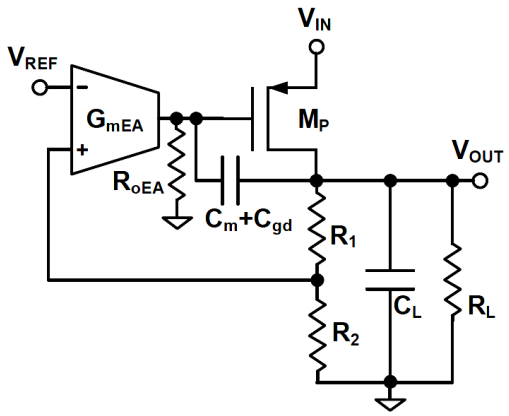


Fig. 3.10 The simplest Miller-compensated OCL-LDO.

Thus, using EA of type-A [19] good PSR at DC is achieved since it is equal to the reciprocal of the high loop gain while the PSR bandwidth (BW) is degraded since the zero frequency has (C_m+C_{gd}) multiplied by the Miller multiplication factor ($g_{mp}r_{dsp}$). On the other side, using EA of type-B the PSR BW is wider but PSR at DC is degraded.

Now we are going to analyze the PSR for our proposed OCL-LDO showing that it can simultaneously improve both PSR at DC and PSR BW. The small signal model used in our PSR analysis is shown in Fig. 3.11. g_{ds5}, g_{ds6}, and g_{dsp} represent, from Fig. 3.5, the channel conductances of M5, M6, and MP, respectively, while C_{gs} represents the gate source capacitance of MP. For the sake of simplicity, the small capacitance C_c together with R_c are not included in the analysis since they just provide local compensation for the EA, as previously explained, with insignificant effect on the PSR of the LDO.

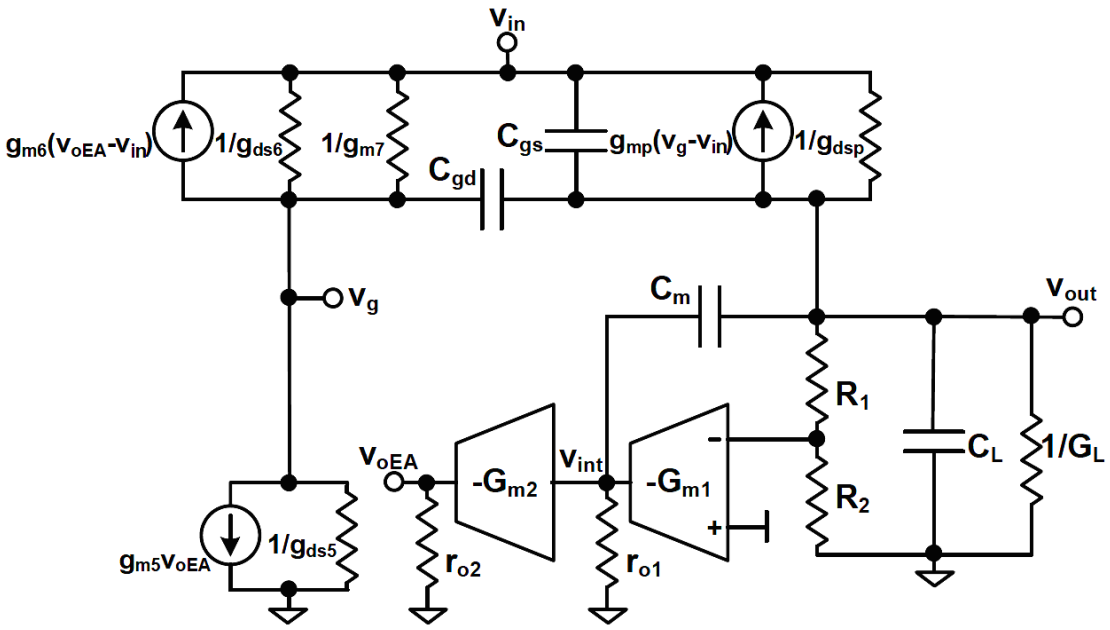


Fig. 3.11 The small signal model of the proposed OCL-LDO that is used to analyze the PSR.

The ratio between v_{out} and v_{in} in Fig. 3.11 represents the PSR transfer function of the OCL-LDO. We can express v_{out} as:

$$v_{out} = [g_{mp}(v_{in} - v_g) + g_{dsp}(v_{in} - v_{out}) + sC_m(v_{int} - v_{out}) + sC_{gd}(v_g - v_{out})] \cdot Z_L, \qquad (3.14)$$

where $Z_L = 1/(G_L + sC_L)$ is the total impedance seen at the output of the LDO ignoring the large feedback resistors R_1 and R_2.

Next we express v_g, v_{int} and v_{oEA} as follows:

$$v_g = \frac{(g_{m7} + g_{m6} + g_{ds6} + sC_{gs})v_{in} + sC_{gd}v_{out} - (g_{m5} + g_{m6})v_{oEA}}{(g_{m7} + g_{ds6} + g_{ds5} + sC_{gs} + sC_{gd})}, \qquad (3.15)$$

$$v_{int} = \beta G_{m1} r_{o1} \frac{\left(1 + s\frac{C_m}{\beta G_{m1}}\right)}{1 + C_m r_{o1}} v_{out}, \qquad (3.16)$$

$$v_{oEA} = -G_{m2} r_{o2} v_{int}. \tag{3.17}$$

Then we solve the 4 equations (3.14) through (3.17) for v_{out}/v_{in} using three basic assumptions:

1) g_{ds5} is much smaller than g_{m7} and g_{ds6} where M5 and M7 are always operating in the saturation region unlike M6 which operates in the triode region at light loads.
2) g_{mp} is much greater than g_{dsp}.
3) A_0, defined in (4), is much greater than 1.

Thus, we obtain the PSR transfer function as follows:

$$\frac{v_{out}}{v_{in}} \cong \frac{g_{dsp} - \dfrac{g_{m6} g_{mp}}{g_{m7} + g_{ds6}}}{A_0 (g_{dsp} + G_L)} \cdot \frac{(1 + sC_m r_{o1}) \left(1 + s \dfrac{g_{mp} r_{dsp} C_{gd}}{(g_{m7} + g_{ds6}) \left(1 - \dfrac{g_{m6} g_{mp} r_{dsp}}{g_{m7} + g_{ds6}}\right)}\right) \left(1 + s \dfrac{C_{gs}}{g_{mp}}\right)}{K(s)}, \tag{3.18}$$

with

$$K(s) = \left(1 + s \frac{C_m}{\beta G_{m1}}\right)\left(1 - s \frac{C_{gd}}{g_{mp}}\right) + \frac{1}{A_0}(1 + sC_m r_{o1})\left(1 + s \frac{C_{gd} + C_{gs}}{g_{m7} + g_{ds6}}\right)\left(1 + s \frac{C_{gd} + C_m + C_L}{G_L + g_{dsp}}\right) \tag{3.19}$$

Then defining the gains of M6 and MP as follows:

$$\begin{aligned} A_{M6} &= \frac{g_{m6}}{g_{m7} + g_{ds6}}, \\ A_{MP} &= g_{mp} r_{dsp}, \end{aligned} \tag{3.20}$$

and with $R_{Leff} = 1/(g_{dsp}+G_L)$, we can rewrite (3.18) as:

$$\frac{v_{out}}{v_{in}} \cong \frac{g_{dsp}(1 - A_{M6} A_{MP})}{A_0 / R_{Leff}} \cdot \frac{(1 + sC_m r_{o1}) \left(1 + s \dfrac{A_{MP} C_{gd}}{(1 - A_{M6} A_{MP})(g_{m7} + g_{ds6})}\right) \left(1 + s \dfrac{C_{gs}}{g_{mp}}\right)}{K(s)}. \tag{3.21}$$

The PSR at DC is not only improved due to having the large A_0 in the denominator but it can be further improved if the numerator is minimized. This is done through the adaptive biasing of the second stage following the EA to keep A_{M6} nearly equal to the reciprocal of A_{MP}, i.e. as I_L decreases; M6 enters the triode region with a decreasing A_{M6} to offset the increase in A_{MP}. Thus, the multiplication of A_{M6} and A_{MP} remains as close as possible to 1 and consequently the numerator of (3.21) is close to zero which means that any input supply ripples will be greatly suppressed. There are two paths for input supply ripples to flow through the pass transistor MP: the first path is through its transconductance (g_{mp}) and the second path is through its channel conductance (g_{dsp}). If the second stage following the EA has only the diode connected transistor M7 without M6 then at DC the numerator of (3.21) will be equal to just g_{dsp} (A_{M6}=0). In this case, M7 and M5 together will act as a voltage subtractor stage as in [5] and will replicate the input ripples at the gate of the pass transistor so as to get V_{GS} free of ripples and consequently the ripples due to the first path of g_{mp} are cancelled. Yet the ripples leaking through the second path of g_{dsp} will not be suppressed although they are becoming more significant in low feature size technologies with large channel conductances of MOS transistors. Therefore in the proposed OCL-LDO with M6 employed together with the adaptive biasing scheme, in addition to canceling the ripples due to g_{mp}, the ripples flowing through g_{dsp} are greatly suppressed as well through having g_{dsp} multiplied by a term that is very close to zero in the numerator of (3.21).

Regarding the PSR BW, it is observed from (3.21) that the there are three zeros in the transfer function as well as three poles. The first zero ($\omega_{Z1}=1/C_m r_{o1}$) is the only zero

depending on C_m where it is not multiplied by Miller multiplication factor. Thus, using small C_m pushes this zero to high frequency. The second zero ($\omega_{Z2}=(1-A_{M6}A_{MP})(g_{m7}+g_{ds6})/A_{MP}C_{gd}$) is close to the first one where although ($g_{m7}+g_{ds6}$) is much larger than $1/r_{o1}$ but the multiplication by $(1-A_{M6}A_{MP})/A_{MP}$ brings ω_{Z2} close to ω_{Z1}. The third zero ($\omega_{Z3}=g_{mp}/C_{gs}$) is located at much higher frequency. Regarding poles on the other hand, the dominant pole is approximately located at $\beta G_{m1}/C_m$ which equals to ω_{GBW} of the loop (defined in (3.7)).

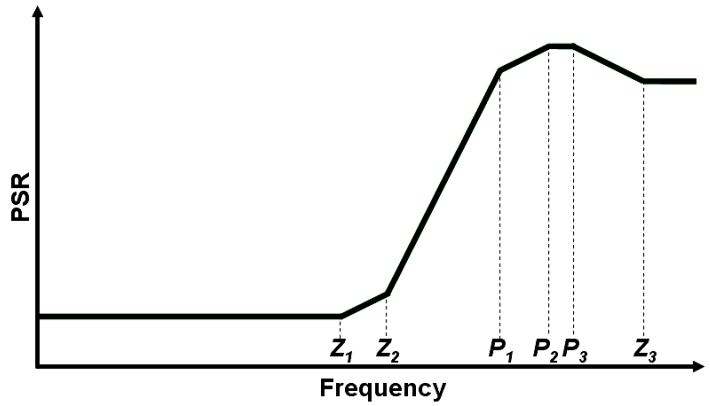


Fig. 3.12 The expected PSR based on the analysis.

Therefore, we can illustrate the expected PSR versus frequency as in Fig. 3.12. It starts with an improved PSR at DC then the wide PSR BW is defined by the high frequency ω_{Z1} that is closely followed by ω_{Z2}. The PSR then starts to degrade by 40dB/decade till $\omega_{P1}\approx\omega_{GBW}$ that is followed by two other high frequency poles and finally comes the high frequency zero ω_{Z3}. Thus, for good PSR at high frequencies it is required to raise ω_{Z1} and ω_{Z2}. This necessitates using a small C_m with the tradeoff of keeping the

loop stable with such low capacitor at light load condition. This tradeoff is greatly relaxed through the use of the adaptive technique as explained in the stability analysis in section 3.2.2.

3.3 Circuit Implementation and Simulation Results

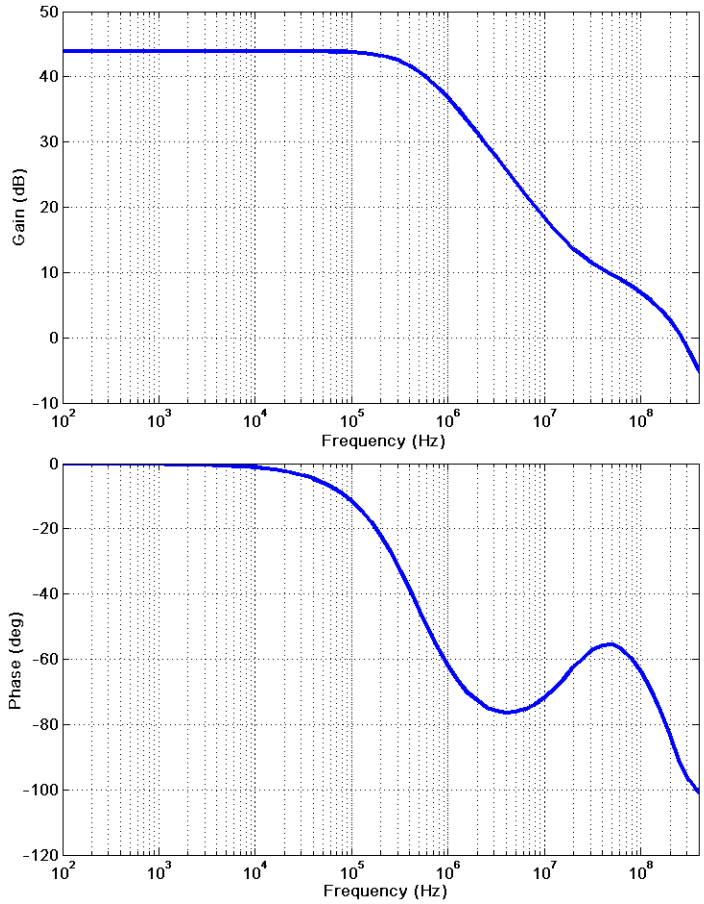


Fig. 3.13 Simulated gain and phase plots for the error amplifier.

The OCL-LDO is designed using 90nm CMOS process. C_m is set to be only 0.8pF while C_c is 0.15pF. R_c of 40KΩ is used to implement the zero required to cancel the pole

located at the EA output. The simulated small signal gain and phase plots for the compensated EA are shown in Fig. 3.13. It achieves a DC gain of 44dB and a phase margin around 90^{o} while consuming 25µA of biasing current. The simulated PSRR for the EA is shown in Fig. 3.14 indicating a PSRR of 99dB at DC and 95dB at its -3-dB frequency of 480KHz. Thus, the amplifier PSRR is not limiting the PSR of the LDO and this justifies the validity of ignoring the amplifier PSRR in the overall PSR analysis in section 3.2.3.

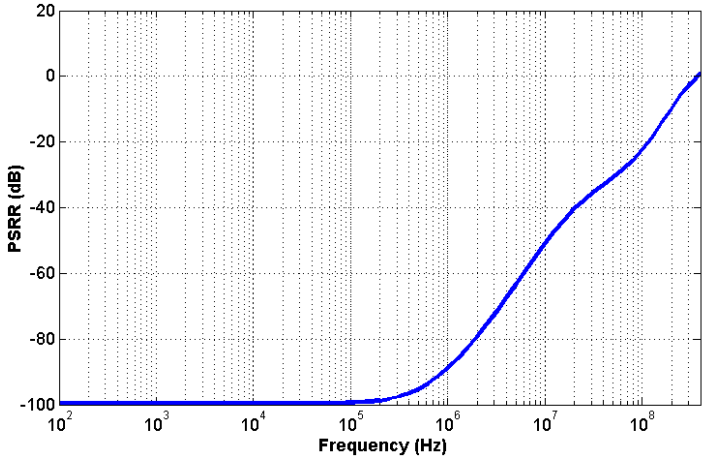


Fig. 3.14 Simulated PSRR of the error amplifier.

With 1.15V input and 1V output, the simulated OCL-LDO open-loop frequency response for different load currents is shown in Fig. 3.15 with ω_{GBW} close to 10MHz and a worst-case phase margin around 60^{o}. Verifying our previous analysis in section 3.2.2, the adaptive biasing technique efficiently pushes the non-dominant complex poles to high frequencies and suppresses the peaking in the magnitude curve to have a worst case peak of only -10dB at a frequency that is about 10 times ω_{GBW}. With process variations the

LDO may not still show good stability at zero load current but has I_{Lmin} of tens of µA for a phase margin of 45°. Also increasing C_L will have same effect of increasing I_{Lmin} for good phase margin. C_L can go up to 100pF and still have a low I_{Lmin} in tens of µA which is within the expected range of current leakage in modern technologies.

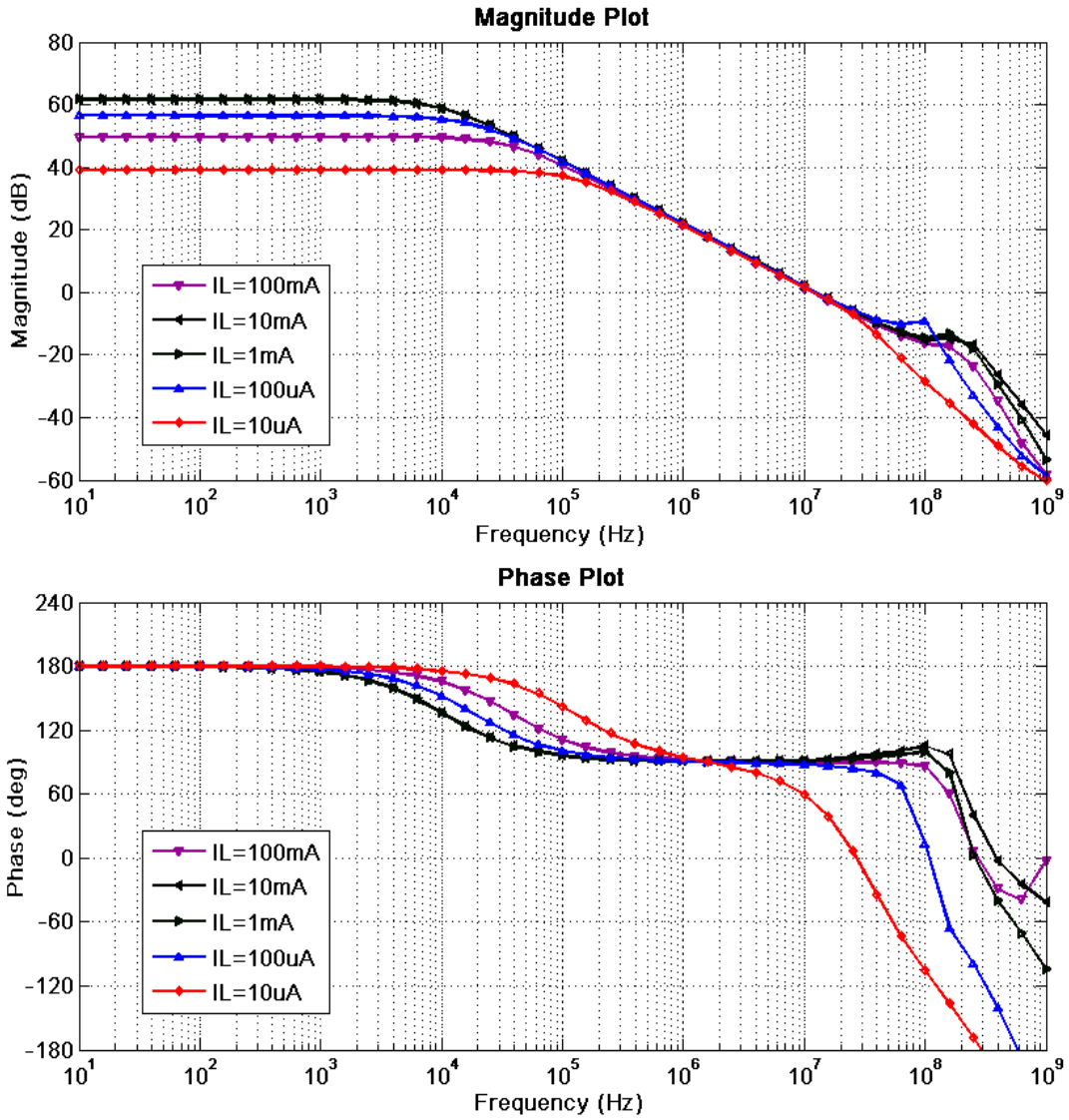


Fig. 3.15 Simulated open-loop frequency response of the OCL-LDO for different load currents.

Fig. 3.16 shows the simulated PSR for two extreme cases of having I_L =100µA and 120mA. There is good correspondence between these simulated curves and the expected one in Fig. 3.12 which verifies our PSR analysis. The first zero is located at same position in both cases around 300KHz and it is closely followed by the second zero. The first pole appears as expected around 10MHz (~ω_{GBW}) that is the same in both cases then it is followed by the remaining two poles and zero.

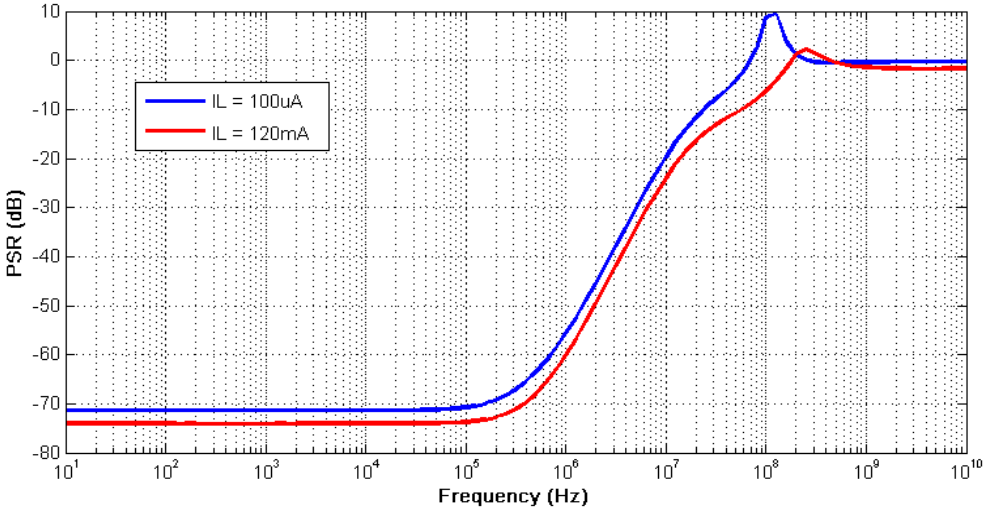


Fig. 3.16 Simulated PSR of the OCL-LDO.

3.4 Experimental Results

The OCL-LDO is implemented in 90nm digital CMOS technology and the chip micrograph is shown in Fig. 3.17. The pass transistor MP occupies around 73% of the total active area that is only 0.016mm^2. The chip is encapsulated in a Quad Flat No-Lead (QFN) package.

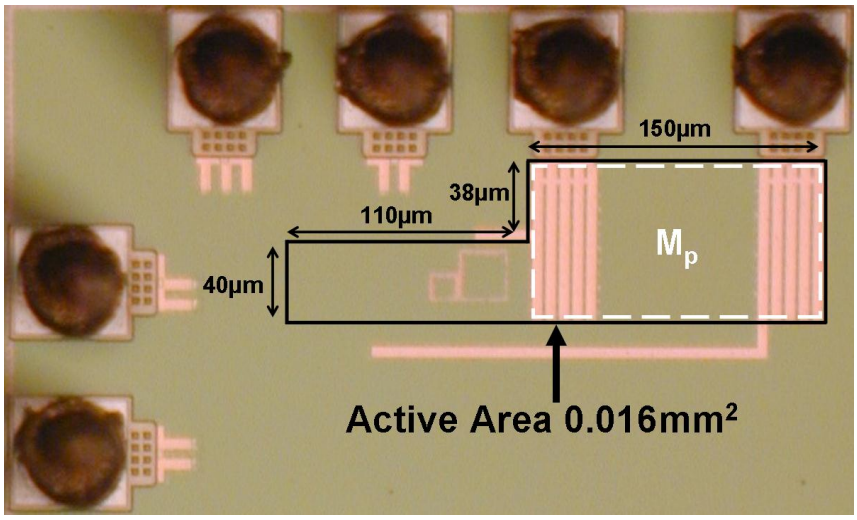


Fig. 3.17 OCL-LDO chip micrograph.

With V_{out} = 1V and V_{DO} = 0.15V, I_Q varies adaptively from 28µA at no load to 122µA at I_{Lmax} of 120mA due to the adaptive biasing of the second stage following the EA. This yields power efficiency (η) of 86.87% where:

$$\eta = \frac{V_{out}}{V_{out} + V_{DO}} \times \frac{I_{L\max}}{I_{L\max} + I_Q}. \tag{3.22}$$

The PSR is measured using the setup shown in Fig. 3.18. A bias-T is used to apply a sine-wave signal of $0.05V_{peak}$ on top of a DC voltage of 1.2V at the input of the LDO. With the output voltage set at 1V, the minimum V_{DO} is 0.15V. A spectrum analyzer with high input impedance (1MΩ in parallel with 10pF), so as not to load the LDO, is used to measure the signal level at both input and output of the LDO while the input signal frequency is swept from 10KHz to 10MHz. The measured PSR for different load currents is shown in Fig. 3.19. PSR is better than -60dB at DC while its worse case at 1MHz is -50dB. At 10MHz it can still provide 17dB of rejection at 120mA load current.

There is good agreement between these measured results and the simulated ones in Fig. 3.13 across our frequency range of interest up to 10MHz.

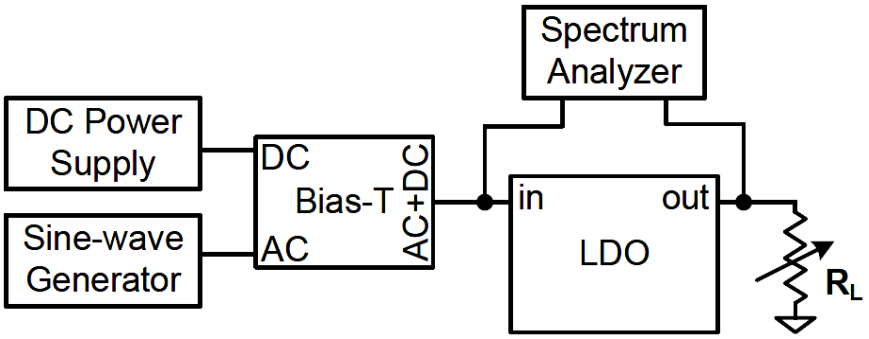


Fig. 3.18 PSR measurement setup.

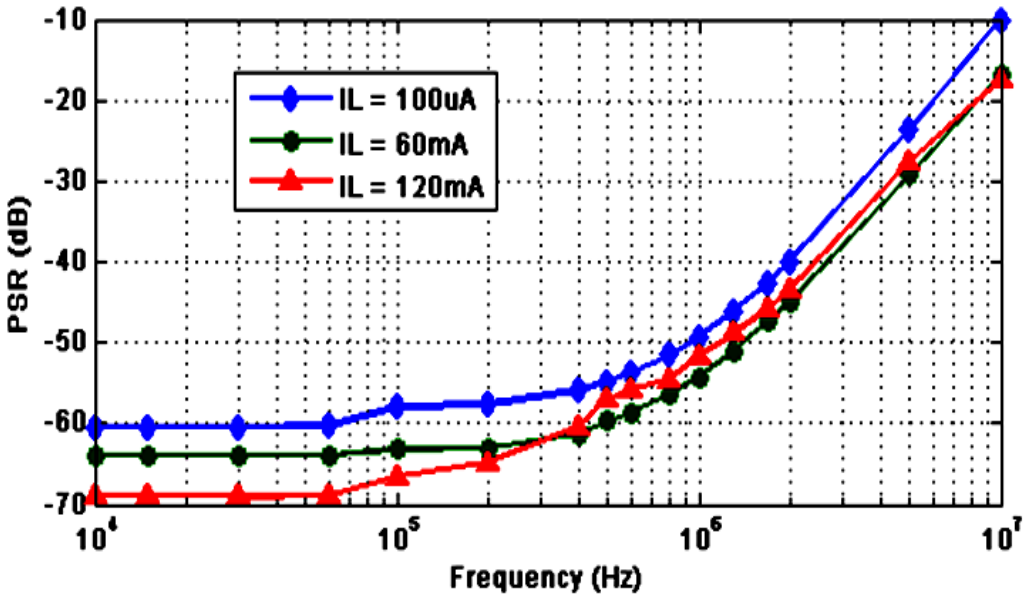


Fig. 3.19 PSR measurement results.

Load transient response is measured using the setup shown in Fig. 3.20. A square-wave generator is used to turn on and off an off-chip NMOS transistor acting as a switch

to connect and disconnect the minimum load resistance to the LDO output. Thus, I_L is switched from zero when the switch is off to I_{Lmax} of 120mA when the switch is on. The rise and fall times of the switched I_L is controlled using a variable resistor at the gate of the transistor switch to change the time constant of the input RC network. The LDO output voltage and the voltage at the output of the switch are displayed on an oscilloscope. The chosen NMOS switch transistor has a small output capacitance so that a total external equivalent C_L of 15pF is loading the LDO in this setup. The LDO also remains stable if an additional capacitance up to 100pF is added to C_L. Capacitor C_{in} is added at the LDO input to assure having a clean ground and shorting any inductive effect due to the measurement cables. Fig. 3.21 shows the load transient response measurement results for the 120mA step in I_L with rise and fall times adjusted to 100ns. The output voltage settles down within only 0.25µs. A load regulation of 58.3µV/mA (7mV/120mA) is measured with maximum overshoot of 32mV and undershoot of 122mV.

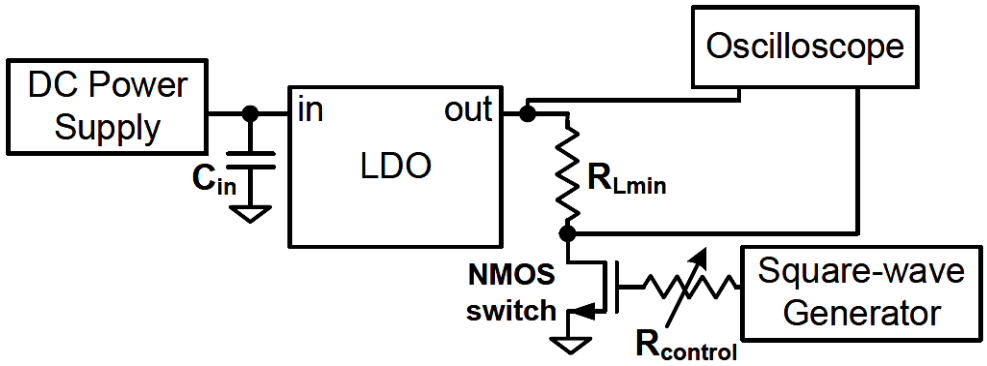
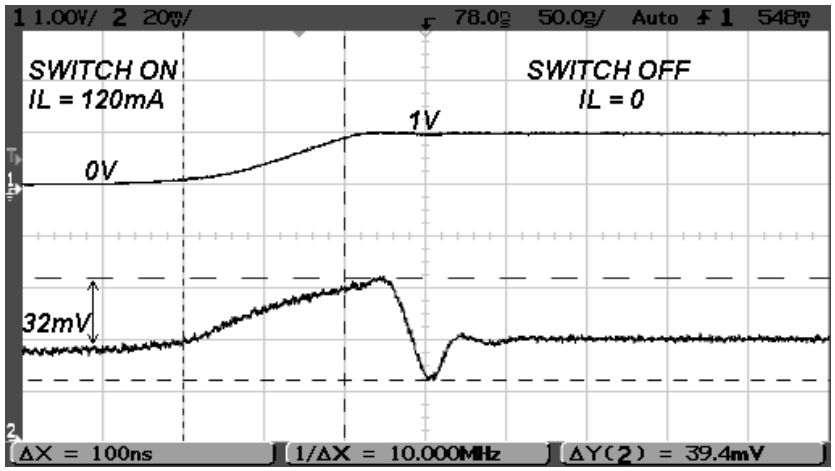
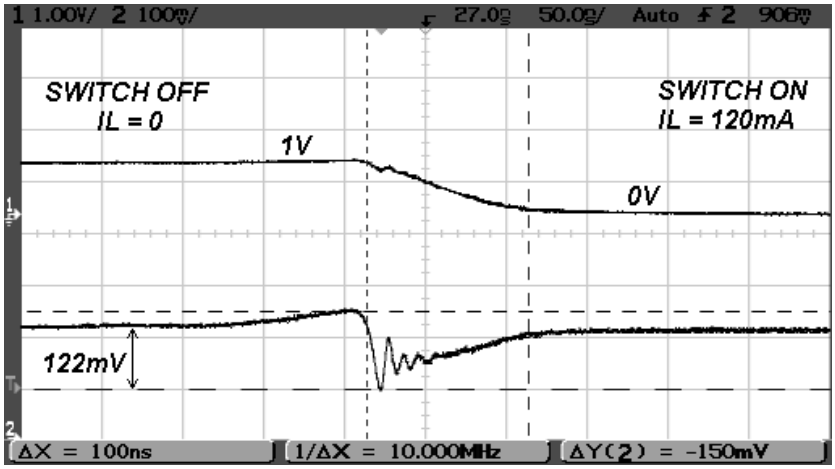


Fig. 3.20 Load transient response measurement setup.



(a)

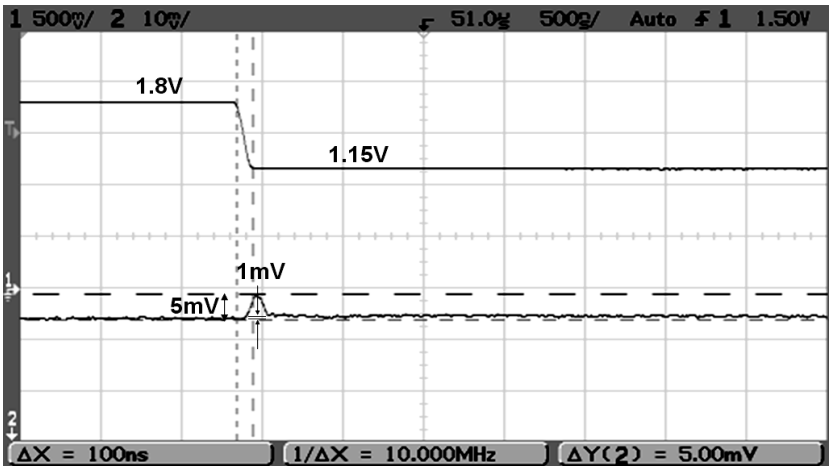


(b)

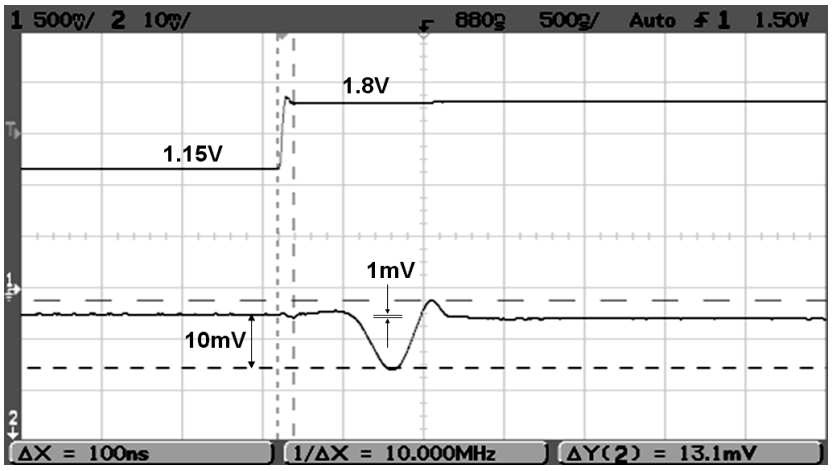
Fig. 3.21 Measured load transient response for two cases: (a) I_L is switched from full load to no load and (b) I_L is switched from no load to full load. In both cases, the upper waveform is the voltage at the drain of the NMOS switch while the lower waveform is the LDO output voltage.

Finally, line transient response is measured for an input voltage switched from 1.8 to 1.15V and vice-versa with rise and fall times of 100ns at I_L of 120mA. Fig. 3.22 shows

the measurement results where a line regulation of 1.54µV/mV (1mV/650mV) is measured with maximum overshoot of 5mV and undershoot of 10mV.



(a)



(b)

Fig. 3.22 Measured line transient response at I_L =120mA for two cases: (a) V_{IN} is switched from 1.8 to 1.15V and (b) V_{IN} is switched from 1.15 to 1.8V. In both cases, the upper waveform is V_{IN} while the lower waveform is V_{OUT}.

3.5 Performance Summary and Comparison

Table 3.1 Performance summary and comparison with recently published OCL-LDO regulators.

	Units	[12] 2003	[14] 2005	[13] 2007	[6] 2007	[15] 2010	[16] 2010	**This work**
Technology	µm	0.6	0.09	0.35	0.6	0.35	0.09	**0.09**
Active Area	mm^2	0.307	0.098	0.125	N/A	0.145	0.019	**0.016**
V_{out}	V	1.3	0.9	1	1.2	1.6	0.5 to 1	**1**
V_{DO}	V	0.2	0.3	0.2	0.6	0.2	0.2	**0.15**
I_Q	µA	38	6000	100	40***	20	8	**28 to 122**
I_{Lmax}	mA	100	100	100	5	100	100	**120**
η	%	86.63	70.75	83.25	66.14	88.87	83.33	**86.87**
ΔV_{out}	mV	100	90	50	750	97	114	**122**
Load Regulation	µV/mA	±0.25%*	1000	338	34200	109	100	**58.3**
Line Regulation	µV/mV	±0.25%*	N/A	0.344	N/A	57.40	3.78	**1.54**
$C_{on\text{-}chip}$	pF	12	600**	6	60**	7	7	**0.95**
C_L	pF	N/A	600	100	10	100	50	**15**
$T_{settling}$	µs	2	N/A	30	0.5	9	5	**0.25**
T_R	ns	N/A	0.540	0.050	1.500	0.097	0.057	**0.015**
FOM	ps	N/A	32.4	50.00m	12.0	19.40m	4.56m	**3.50m**
PSR @ 10KHz	dB	-60	N/A	N/A	-70	-40	-25	**-60**
PSR @ 1MHz	dB	-30	N/A	N/A	-40	N/A	0	**-50**

* This is error of the output voltage due to line and load changes
** This includes C_L which is implemented on-chip
*** The quiescent current for the error amplifier only

A performance summary for the proposed OCL-LDO in comparison with recently published OCL-LDOs is summarized in Table 3.1. The proposed OCL-LDO, using the smallest on-chip capacitance, has the smallest silicon area of only $0.016mm^2$. The proposed OCL-LDO has the largest I_{Lmax} and the smallest V_{DO} with small I_Q that is changing according to I_L for better efficiency and improved transient response as well. The proposed OCL-LDO has the fastest transient response in terms of both the settling

time ($T_{settling}$) and the response time ($T_R=C_L x \Delta V_{out}/I_{Lmax}$ [14]) which are at least 50% lower than in any other previously reported work. Using the figure of merit ($FOM=T_R x I_Q/I_{Lmax}$) proposed in [14] and adopted in [15] for comparing different OCL-LDOs, we can observe that our proposed OCL-LDO achieves the best FOM. Regarding PSR, the proposed OCL-LDO achieves the best PSR at 1MHz that is 10dB better than in [6] with 24 times larger I_{Lmax} and 50dB better than in the most recent 90nm CMOS OCL-LDO [16]. Load and line regulations as well as power efficiency are also among the best reported.

3.6 Conclusion

In this chapter, a simple OCL-LDO topology that is adaptive to load current variations is proposed to ensure stability of the OCL-LDO at light load condition and to provide fast transient response and high PSR. This OCL-LDO is implemented in 90nm CMOS technology and it uses a small on-chip capacitance of only 0.95pF. Up to our knowledge, the proposed OCL-LDO achieves the fastest transient response reported for OCL-LDOs in addition to the best PSR of -50dB at 1MHz and the smallest silicon area of $0.016mm^2$. With dropout voltage of just 0.15V, the OCL-LDO achieves power efficiency of 86.87%, line regulation of 1.54µV/mV and load regulation of 58.3µV/mA for a load current step of 120mA.

CHAPTER IV

POWER AND AREA EFFICIENT BUCK CONVERTER

4.1 Introduction

Switching DC-DC converters are key building blocks in any power management SoC. As operating frequencies in these integrated systems increase, load fluctuations require high switching frequencies (f_s) in the DC-DC converters for fast transient response. Additionally, high f_s allows using small sized inductor (L_o) and capacitor (C_o) in the off-chip output filter and also small sized on-chip passive components for internal compensation. This results in reducing area and cost and allows the use of larger or better battery which improves the system performance [2]. However, as f_s increases the switching losses in the power stage increase as well as the complexity of the controller where high quiescent current (I_Q) is required to be able to track this fast switching activity.

4.1.1. Previously Reported Works

In literature, two main approaches are employed to implement switching converters with high f_s. First approach is to use f_s in the range of hundreds of MHz and have the output filter integrated on chip [20,21]. This requires special expensive technologies to implement on-chip inductors of high Q. Moreover, complex control schemes are required to operate at these high frequencies. Second approach is to use an off-chip filter using L_o and C_o of tiny footprints on the printed circuit board (PCB). f_s in this case can go up to few MHz to slightly improve the transient response [1,2,22]. There

is still the challenge of the complexity of the controller. In [2] for instance, f_s is 10MHz where the straightforward pulse-width-modulation (PWM) control scheme is avoided due to limited bandwidth and large compensation capacitance. Thus, a more complicated hysteresis controller is used with a major drawback of having f_s varying widely with parameters such as the input or output voltages or the values of L_o and C_o. The variations in f_s make the output spectrum change unpredictably leading to power supply integrity issues [23,24]. Thus, an additional automatic frequency control with extra complexity and silicon area is added.

This work presents a buck converter employing a simple Pulse Width Modulation (PWM) controller working at f_s of 20MHz that can go down to 10MHz. It achieves a wide bandwidth and fast transient response while consuming very low I_Q. The proposed compensator mimics the frequency response of a conventional Type III compensator with smaller on-chip compensation capacitors and resistors to minimize the silicon area. Small sized off-chip L_o and C_o of 330nH and 2µF, respectively, are used in the output filter. The current consumed in both the compensator and the modulator is only 48µA (25µA) from 1.8V supply with f_s of 20MHz (10MHz). Working in synchronous mode with no extra special technique to reduce the switching losses in the power stage; the peak efficiency is measured to be 81% at 130mW load power.

4.1.2. Type III Compensation

As a background overview, this section presents the fundamentals of Type III compensation. The bock diagram of a typical buck converter is shown in Fig. 4.1.

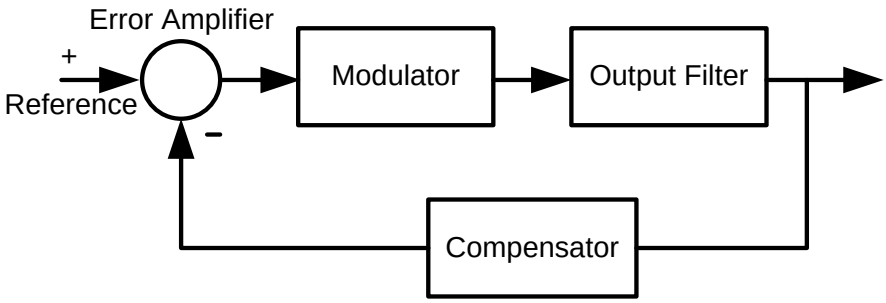


Fig. 4.1 Block diagram of a typical buck converter.

The output filter is shown in Fig. 4.2 where R_{DCR} is the DC Resistance of the output inductor L_o while R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor C_o. The transfer function of the output filter is given by:

$$\frac{v_{filter\_out}}{v_{filter\_in}} = \frac{1 + sC_oR_{ESR}}{1 + sC_o(R_{ESR} + R_{DCR}) + s^2C_oL_o} \tag{4.1}$$

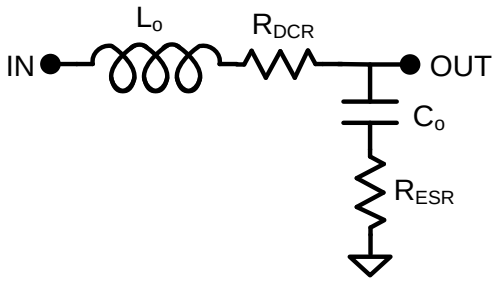


Fig. 4.2 The output filter.

Thus, the transfer function of the open loop system consisting of the modulator and the output filter can be shown in Fig. 4.3. The DC gain A_{mod} is the gain of the modulator while $f_{LC} = 1/2\pi\sqrt{L_oC_o}$ defines the frequency at which the slope starts to be

-40dB/decade before the zero due to the capacitor ESR comes into effect at f_{ESR} = $1/2\pi C_o R_{ESR}$ to make the slope -20dB/decade.

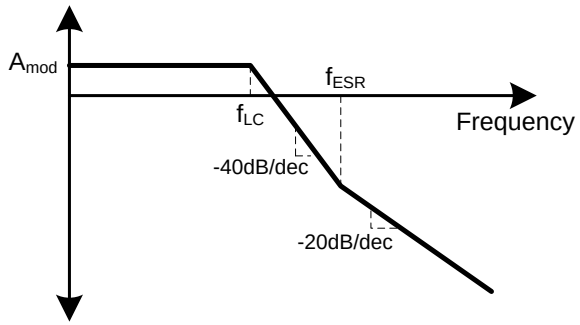


Fig. 4.3 Asymptotic Bode plot of the modulator and output filter.

Due to the double pole at f_{LC}, the system needs compensation in the feedback. In Type III compensator, two zeros are introduced to give a phase boost of 180^o to counteract the effect of the double pole of the output filter. This is preferred than Type II compensator in which only one zero is introduced relying on the ESR of the output capacitor to keep the loop stable which is not practical in many cases and sets limits on the choice of output capacitor. Fig. 4.4 shows the asymptotic Bode plot of the Type III compensator while Fig. 4.5 shows its most conventional implementation. The compensator transfer function is given by:

$$\frac{v_{out\_comp}}{v_{in\_comp}} = \frac{1}{sR_1(C_1+C_2)} \cdot \frac{(1+s/\omega_{z1})(1+s/\omega_{z2})}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \qquad (4.2)$$

where the zeros and poles frequencies are given by:

$$\omega_{z1} = \frac{1}{R_2 C_2}$$
$$\omega_{z2} = \frac{1}{(R_1 + R_3)C_3}$$
$$\omega_{p1} = \frac{C_1 + C_2}{R_2 C_1 C_2} \qquad (4.3)$$
$$\omega_{p2} = \frac{1}{R_3 C_3}$$

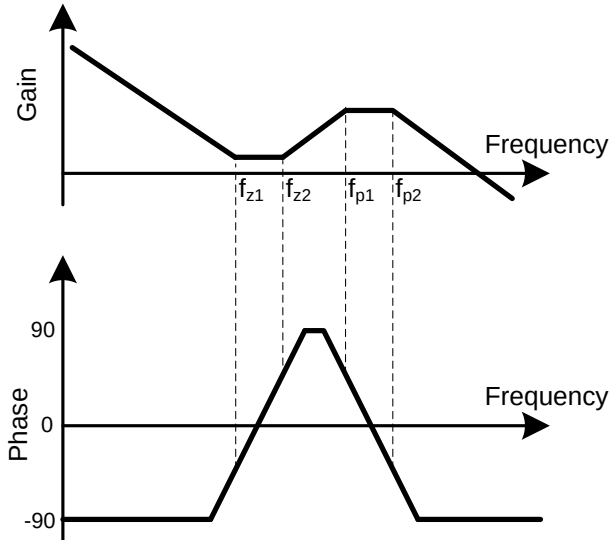


Fig. 4.4 Asymptotic Bode plot of the Type III compensator.

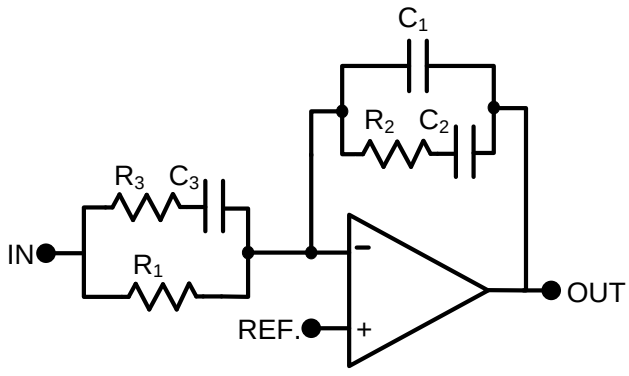


Fig. 4.5 Typical implementation of a Type III compensator.

Thus, the complete converter will be as shown in Fig. 4.6 with a PWM modulator, consisting of a sawtooth waveform generator and a comparator. Gain curves for different blocks of the converter are shown in Fig. 4.7 where the solid curve shows the resultant converter gain curve. The unity gain frequency of the error amplifier needs to be around f_s. This means that for switching at 10MHz or above, the amplifier will consume high power to achieve this wide band. The comparator as well needs to be able to respond to this high f_s which again results in high power consumption.

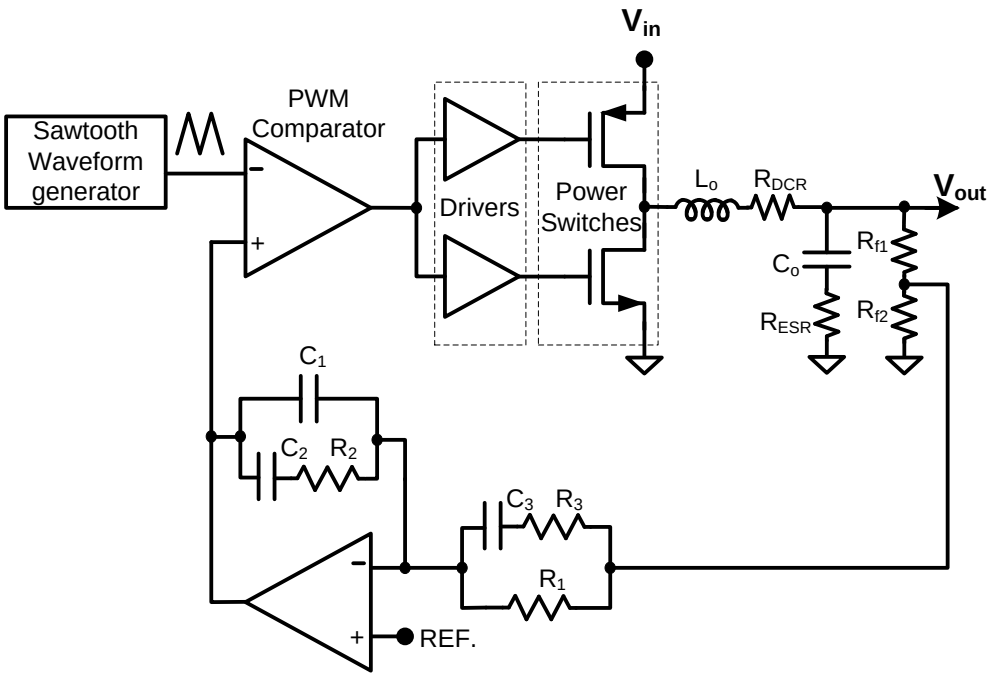


Fig. 4.6 Typical Type III buck converter.

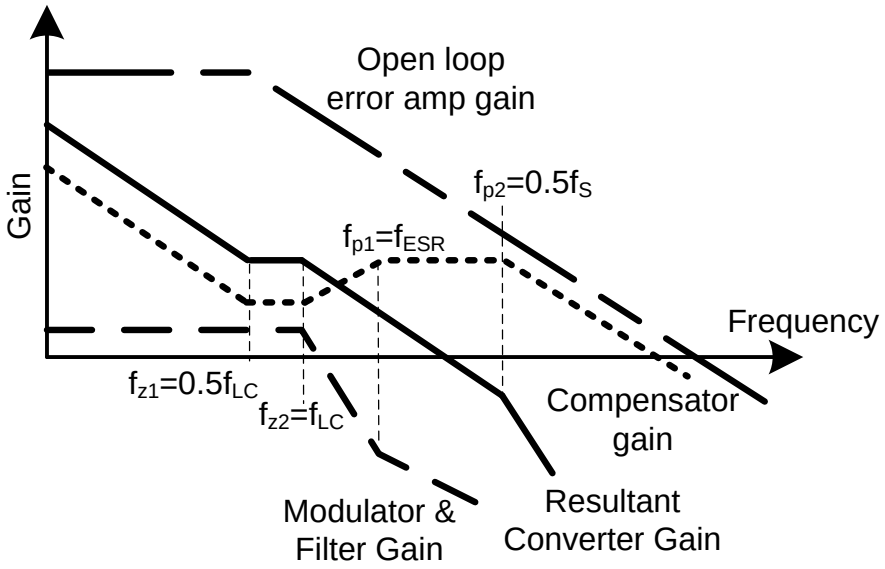


Fig. 4.7 Different gain curves for the Type III converter.

4.1.3. Proposed Solution

The proposed controller is shown in Fig. 4.8. The compensator is a Pseudo-Type III compensator where the required transfer function is achieved through a simpler architecture without the need of a power hungry error amplifier and with fewer and smaller passive components. The modulator on the other side is relying on a voltage to current converter with no need for an explicit comparator to provide the PWM signal to the drivers.

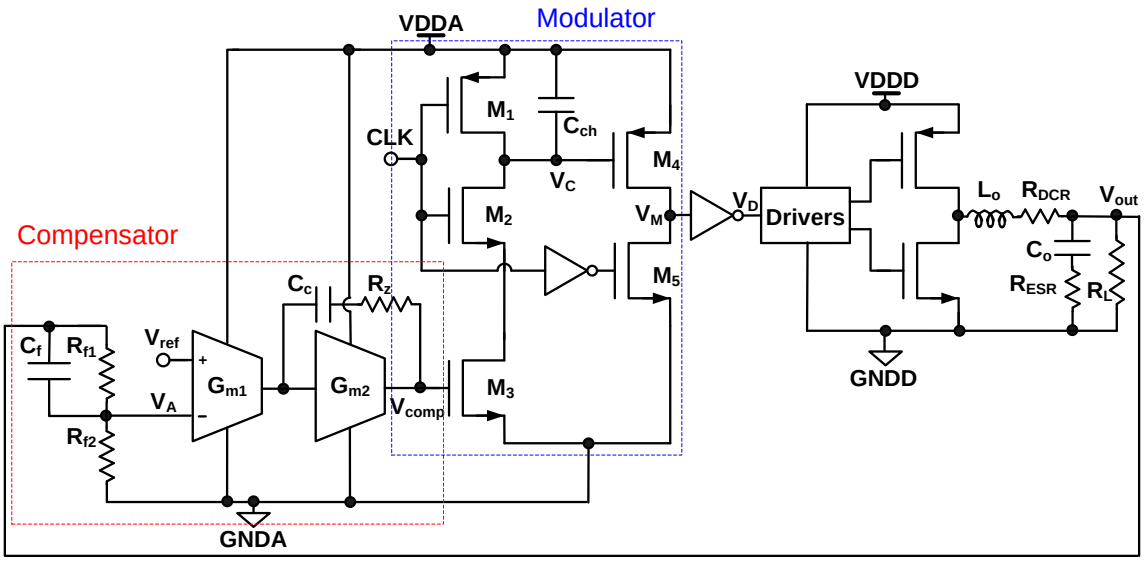


Fig. 4.8 Proposed Pseudo-Type-III buck converter.

4.2 Pseudo-Type III Compensator

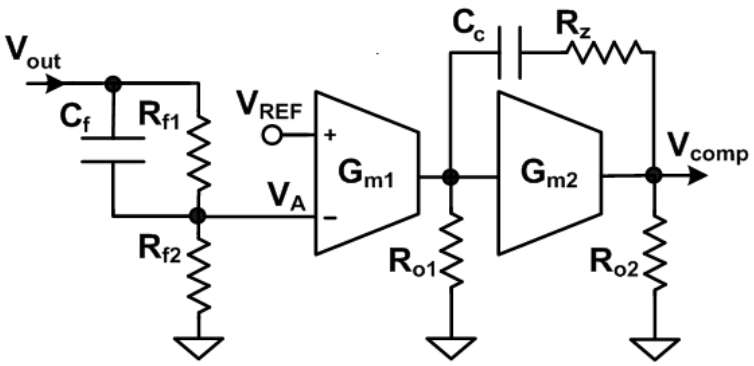


Fig. 4.9 Proposed Pseudo-Type-III compensator.

The proposed Pseudo-Type III compensator is shown in Fig. 4.9. A capacitor C_f is added in parallel to R_{f1} to have a pole-zero pair in the transfer function from v_{out} to v_A as given by:

$$\frac{v_A}{v_{out}} = \frac{R_{f2}}{R_{f1}+R_{f2}} \cdot \frac{1+sC_fR_{f1}}{1+sC_f(R_{f1}//R_{f2})} \tag{4.4}$$

There is a zero at $\omega_z=1/C_fR_{f1}$ followed by a pole at $\omega_p=1/C_f(R_{f1}//R_{f2})$. In this design R_{f1} is set three times larger than R_{f2} resulting in $\omega_p = 4\cdot\omega_z$ and V_{REF} then has to be equal $V_{out}/4$. The transfer function of (4.4) is shown in Fig. 4.10(a).

The error amplifier on the other side is a two stage amplifier with Miller compensation. C_c is the Miller capacitance while R_z is added to create a zero in the transfer function from v_A to v_{comp} that is given by:

$$\frac{v_{comp}}{v_A} = \frac{G_{m1}R_{o1}G_{m2}R_{o2}(1+sC_cR_z)}{(1+sG_{m2}R_{o2}C_cR_{o1})(1+sC_c/G_{m2})} \tag{4.5}$$

A wide separation between the two poles can be achieved with a small value of C_c <10pF making use of the gain of the second stage. R_z is then used to create a zero in between the two widely separated poles. The transfer function of (4.5) is shown in Fig. 4.10(b).

Combining the two transfer functions in (4.4) and (4.5), the compensator transfer function will be as follows:

$$\frac{v_{comp}}{v_{out}} = \frac{R_{f2}}{R_{f1}+R_{f2}} \cdot \frac{1+sC_fR_{f1}}{1+sC_f(R_{f1}//R_{f2})} \cdot \frac{G_{m1}R_{o1}G_{m2}R_{o2}(1+sC_cR_z)}{(1+sG_{m2}R_{o2}C_cR_{o1})(1+sC_c/G_{m2})} \tag{4.6}$$

This combined transfer function of the compensator is shown in Fig. 4.10(c) with three poles and two zeros given by:

$$\omega_{p0} = \frac{1}{G_{m2}R_{o2}C_cR_{o1}}$$
$$\omega_{z1} = \frac{1}{R_ZC_c}$$
$$\omega_{z2} = \frac{1}{R_{f1}C_f} \qquad (4.7)$$
$$\omega_{p1} = \frac{1}{(R_{f1} // R_{f2})C_f}$$
$$\omega_{p2} = \frac{G_{m2}}{C_3}$$

The first pole ω_{p0} needs to be at very low frequency where making use of the Miller multiplication gain $G_{m2}R_{o2}$ allows the use of C_c of no more than 10pF.

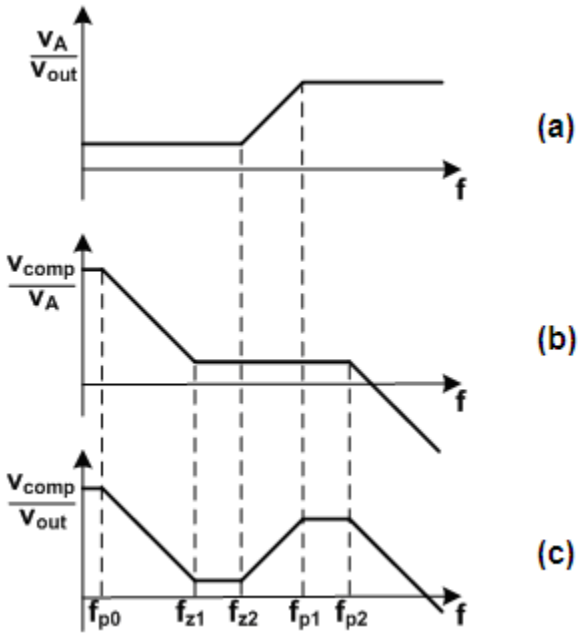


Fig. 4.10 (a) The transfer function of the feedback network. (b) The transfer function of the amplifier. (c) The combined transfer function of the compensator.

Thus the Type III transfer function is simply achieved without the need of having an error amplifier of very wide bandwidth and using smaller and fewer passive components. This leads to both power and area savings. Similar approach of mimicking the frequency response of a Type III compensator was employed in [25] for a buck converter operating at lower switching frequency of 1MHz. In [25] the transfer function was achieved as a summation of two functions implemented through two different paths. The first path had an error amplifier with very large capacitor of 100pF at its output while the second path employed a bandpass filter. However, defining the location of zeros and poles was not straight forward and it involved many approximations.

4.3 Modulator Based on Voltage to Current Conversion

The modulator circuit schematic is shown in Fig. 4.11. It consists of a voltage to current converter where the output current is used to charge a capacitor with a slope that varies according to the required duty cycle (D). The transient waveforms at different points are shown in Fig. 4.12. The clock signal has a narrow falling pulse at the beginning of each period T that turns on switches M1 and M5 to pre-discharge the capacitor C_{ch} at the supply V_{DDA} and to reset the modulator output node V_M to ground, respectively. For the rest of T, switch M2 is kept on to charge C_{ch} with a charging current I_{ch} given by:

$$I_{ch} = C_{ch} \frac{dV}{dt} \tag{4.8}$$

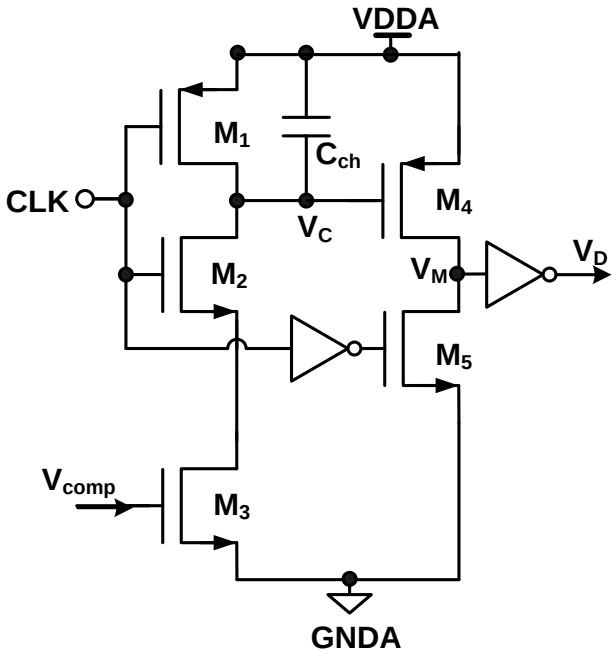


Fig. 4.11 The modulator circuit schematic.

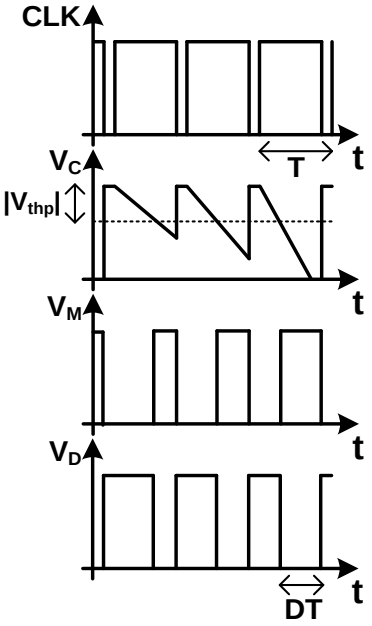


Fig. 4.12 The modulator transient waveforms.

When V_c is less than V_{DDA} by $|V_{thp}|$, which is the threshold voltage of the M4, M4 turns on and pulls up V_M to V_{DDA}. The time taken for this to happen defines D of the PWM output signal that feeds the following drivers. This time depends on the value of I_{ch} which is adjusted through the feedback loop. If the width of the negative pulse is much smaller than T then (4.8) can be approximated to:

$$I_{ch} = C_{ch} \frac{|V_{thp}|}{T(1-D)} \tag{4.9}$$

Therefore:

$$D = 1 - \frac{C_{ch}|V_{thp}|}{TI_{ch}}, \tag{4.10}$$

This indicates that for fixed f_s, if D is to be changed then I_{ch} is adjusted through the feedback loop. Similarly, for same D if f_s is changed, I_{ch} will change accordingly. In other words, if T is halved (f_s is doubled), I_{ch} will be doubled to keep same D for same input and output voltages of the buck converter.

Then the current to duty cycle transfer function can be given by:

$$\frac{\partial D}{\partial I_{ch}} = \frac{C_{ch}|V_{thp}|}{TI_{ch}^2} = \frac{(1-D)^2 T}{C_{ch}|V_{thp}|} \tag{4.11}$$

Having the transfer function of the voltage to current converter, done through transistor M3, given by:

$$\frac{\partial I_{ch}}{\partial V_{comp}} = g_{m3}, \tag{4.12}$$

then the compensator output to duty cycle transfer function will be given by:

$$\frac{\partial D}{\partial V_{comp}} = g_{m3} \cdot \frac{(1-D)^2 T}{C_{ch} |V_{thp}|}, \tag{4.13}$$

and thus including the drivers and power stage, the total gain of the modulator will be given by:

$$\frac{V_{out}}{V_{comp}} = \frac{\partial D}{\partial V_{comp}} \cdot V_{DDD} = g_{m3} \cdot \frac{(1-D)^2 T}{C_{ch} |V_{thp}|} \cdot V_{DDD} \tag{4.14}$$

Similar approach of using a modulator based on voltage to current converter was employed in [22] but with different current control scheme. In [22] the current is controlled through a bias current generator which requires two different control voltages. One of them requires a big off-chip RC filter with large time constant to minimize error. This sets limitations on the controller size and accuracy.

4.4 Circuit Implementation

The buck converter is implemented using 0.18µm CMOS process. f_s is chosen to be from 10 to 20MHz for fast transient response and to use small sized passive components both on-chip and off-chip. Thus, a surface mount inductor L_o of 0.33µH and size 2512 (1.5 mm x 2.5 mm) is used with a C_o of 2µF having R_{ESR} of 50mΩ. Therefore, f_{LC} = 200KHz and f_{ESR} = 1.6MHz.

For the compensator design, f_{p2} is set equal to f_{ESR} and thus f_{z2} has to be equal $f_{ESR}/4$ as previously explained while f_{z1} is set equal to $f_{z2}/2$. Using these values, the required on-chip compensation capacitors and resistors in the two cases of using a conventional Type III compensation and our proposed Pseudo-Type III compensation are calculated and given in Table 4.1. Notice that R_{f1} and R_{f2} are required in both converters

to provide the feedback network from the output to the input of the error amplifier, and they used to be large to minimize quiescent current. Thus, R_{f1} and R_{f2} are removed from the comparison where in our design they are set to be 300KΩ and 100KΩ, respectively.

Table 4.1 Comparison between the conventional Type III and the Pseudo-Type III compensator in terms of sizes of required passive components.

Proposed Pseudo-Type III Compensator		Conventional Type-III Compensator	
R_z	90KΩ	R_1	100KΩ
C_c	9.5pF	R_2	100KΩ
C_f	1.4pF	R_3	8KΩ
		C_1	1.2pF
		C_2	8.4pF
		C_3	4.2pF
Total C	10.9pF	Total C	13.8pF
Total R	90KΩ	Total R	208KΩ

It can be observed from Table 4.1 that the number of passive components in the proposed compensator is reduced to half. Regarding the values of components, the total resistance is reduced by more than 55% while the total capacitance is reduced by more than 20%. This results in significant silicon area reduction. This is in addition of the possibility of using a transistor in triode region to implement R_z which can be easily adjusted to set f_{z1} at the exact value accounting for any process variations. This further reduces the area required for the resistors to the minimum.

Another huge advantage is that in the proposed compensator there is no need for an amplifier of unity gain frequency exceeding 10MHz as in conventional Type III compensator with an estimated current consumption exceeding 500µA. In our proposed

compensator, the current consumed in the two Gm cells used in the error amplifier is only 7µA which means a saving of more than 98% in quiescent current consumption which is important to improve efficiency in addition to the fact that in most applications the buck converter is going to sit idle for most of the time and thus the quiescent current supplied from the battery in this case needs to be as low as possible.

For the modulator design, as previously explained no sawtooth waveform generator is required. Only a clock with large duty cycle is required as an input to the modulator. The value of the capacitor used is only 0.95pF.

The drivers of the power transistors are implemented as shown in Fig. 4.13. The two non overlapped output signals are used to drive the gates of the two power transistors. The ratio between the sizes of consecutive inverters is calculated to be 4.5 based on [26] while in each inverter the ratio between the PMOS and NMOS sizes is 3:1 to account for the mobility difference based on simulations. Thus, the last inverter has its PMOS of W/L = 972/0.18 µm/µm while its NMOS is of W/L = 324/0.18 µm/µm.

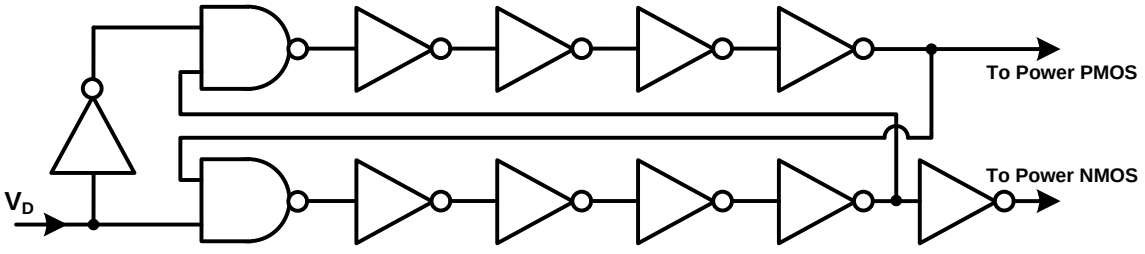


Fig. 4.13 Schematic of the drivers of the power transistors.

The PMOS power transistor has W/L = 12960/0.18 µm/µm while the NMOS transistor has W/L = 4860/0.18 µm/µm. The ratio between the sizes of the two transistors

is 3:1.125 that is slightly smaller than 3:1 because with the PMOS size designed based on achieving a reasonable low r_{dson}, the NMOS size on the other hand has to be slightly increased to have a large enough body diode to withstand the large current flowing through it in the synchronous buck converter topology during the dead zone period at which both switching transistors are off.

4.5 Simualtion Results

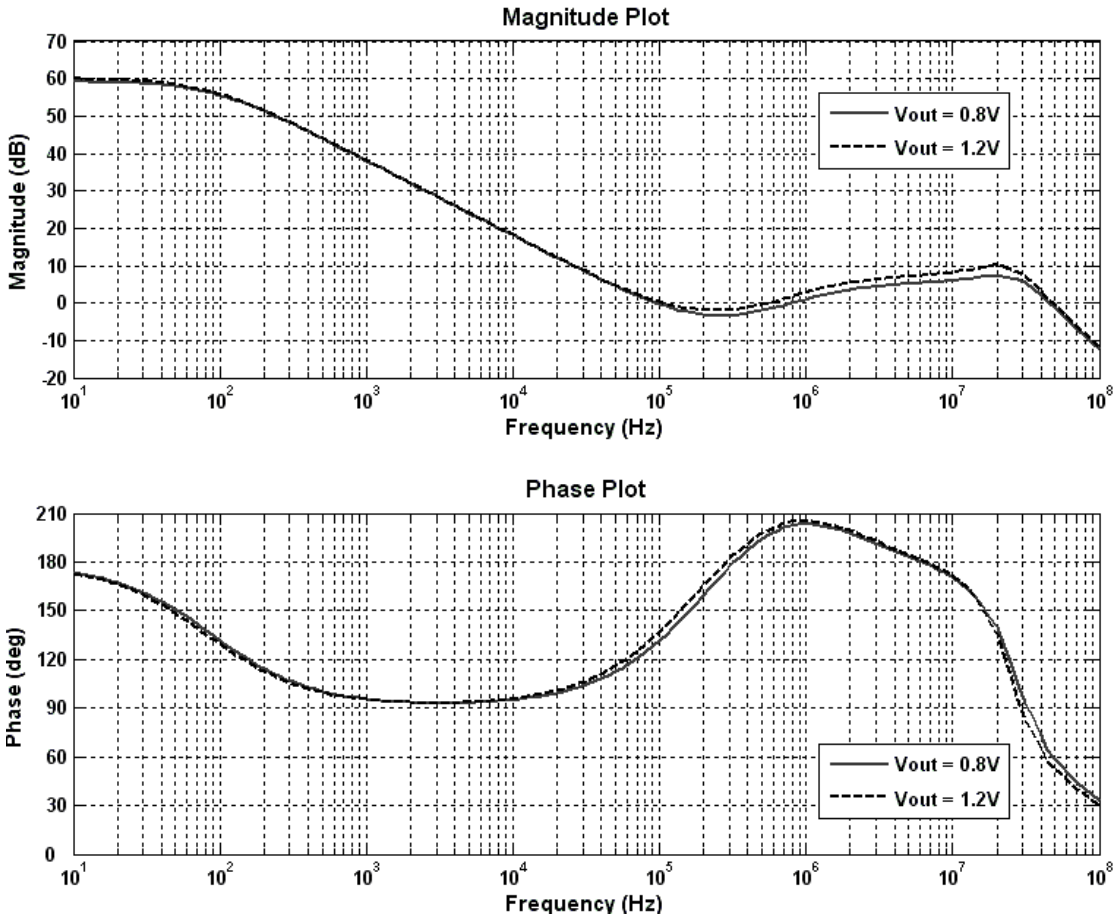


Fig. 4.14 Magnitude and phase plots of the Pseudo-Type III compensator.

Fig. 4.14 shows the simulated magnitude and phase plots of the compensator transfer function for two cases of converter output voltage V_{out} of 0.8V and 1.2V while the input is fixed at 1.8V. The required transfer function given in Fig. 4.10(c) is achieved with the two zeros boosting the phase up to around 210^o with a phase margin around 60^o to guarantee stability of the compensator. Then the open loop transfer function of the complete converter is given in Fig. 4.15 where phase margins of 53^o and 55^o are achieved for the two cases of V_{out} of 0.8V and 1.2V, respectively. High DC gain (> 70dB) as well as high gain-bandwidth product (> 400KHz) are achieved.

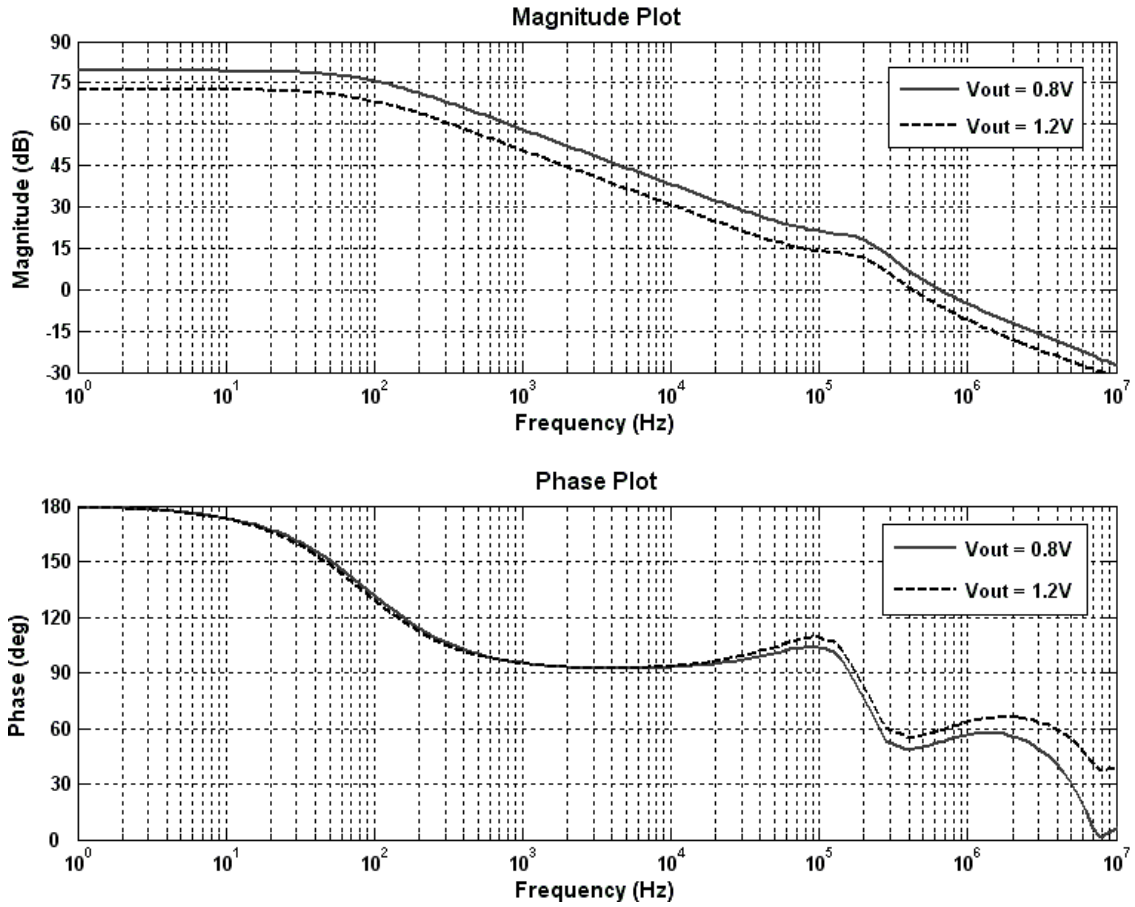


Fig. 4.15 Open loop magnitude and phase plots of the complete converter.

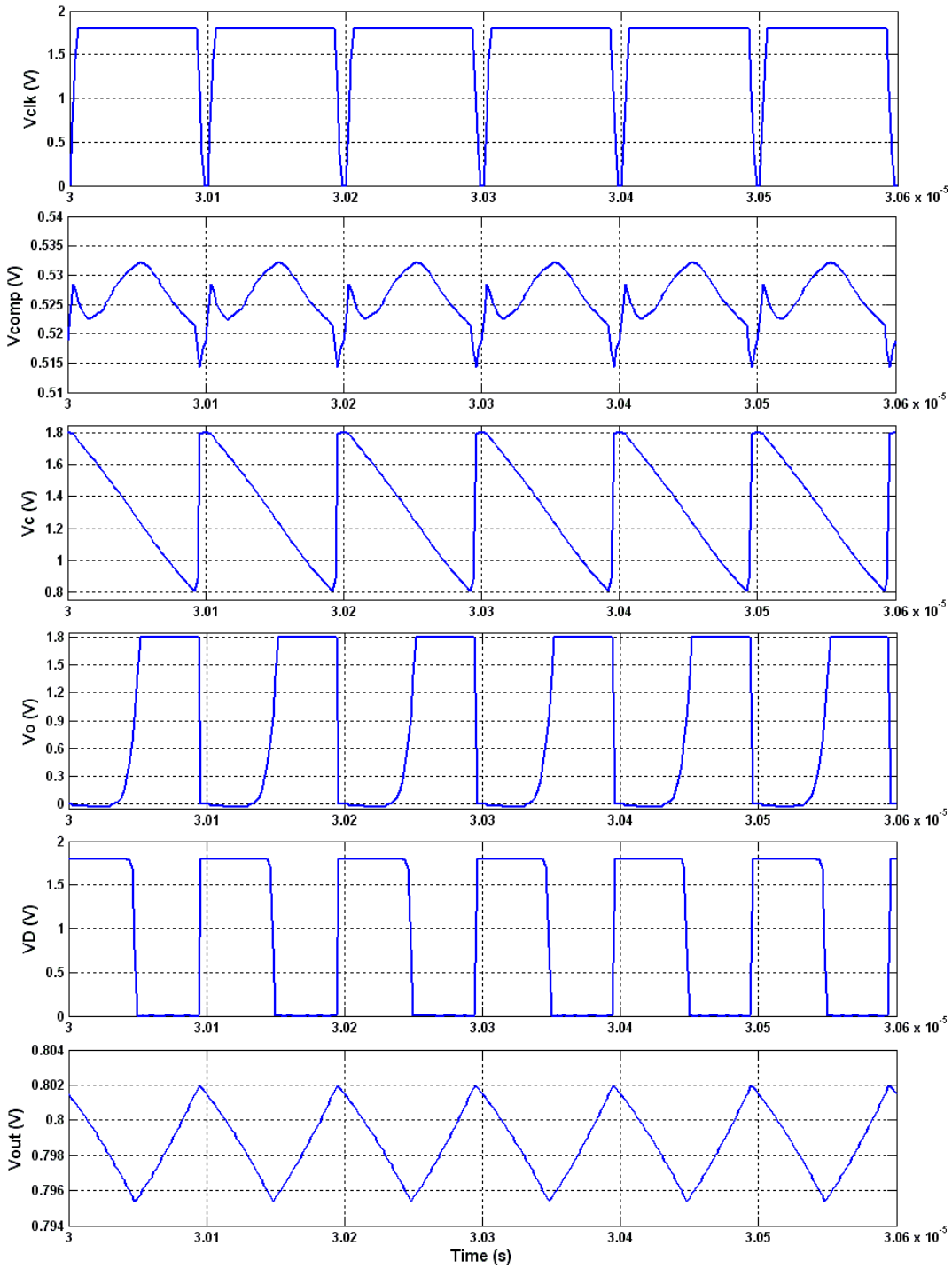


Fig. 4.16 Voltage waveforms at different nodes of the compensator in addition to the final output of the converter for V_{out}=0.8V.

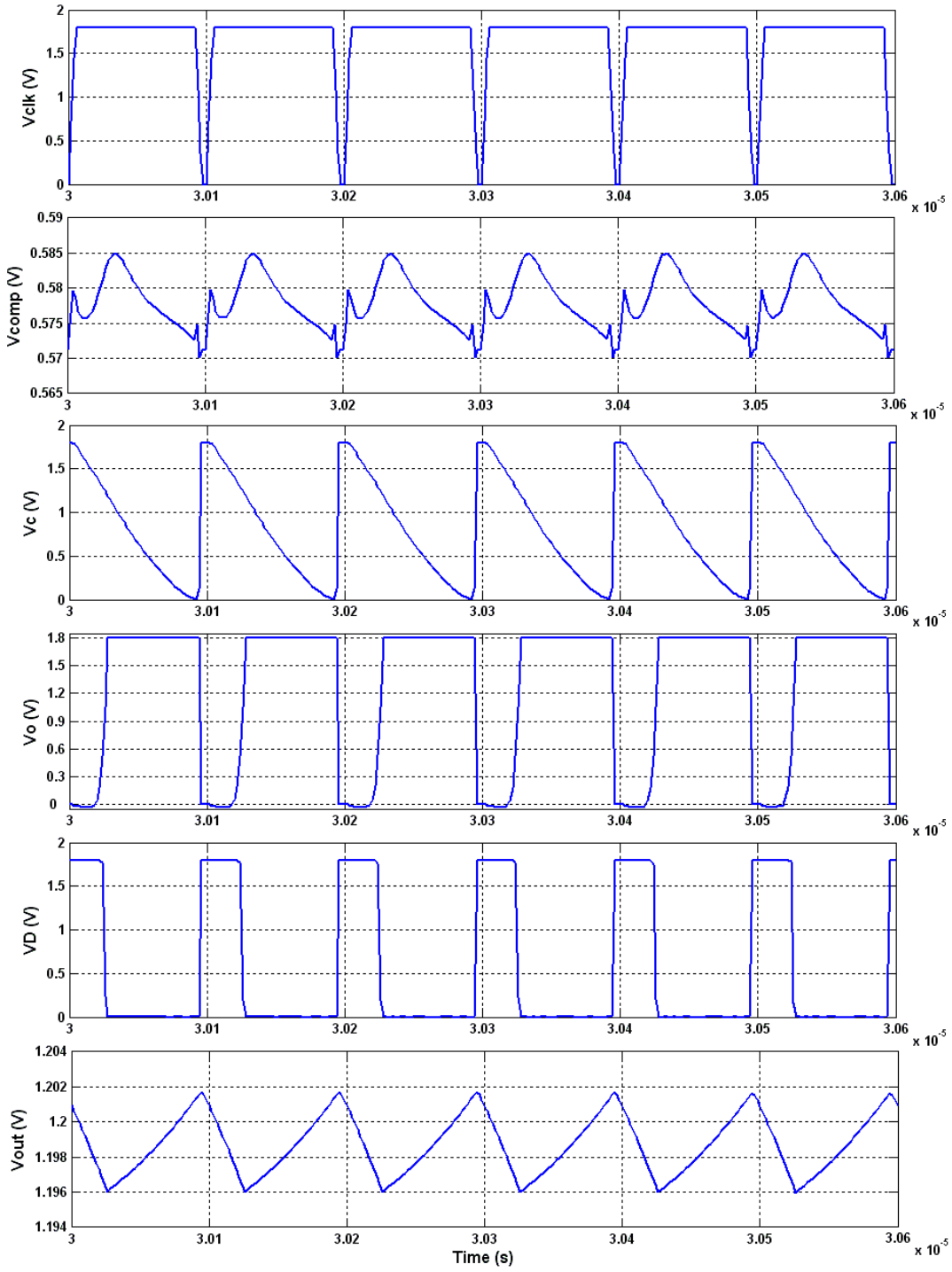


Fig. 4.17 Voltage waveforms at different nodes of the compensator in addition to the final output of the converter for V_{out}=1.2V.

Figures 4.16 and 4.17 show the voltage waveforms at different nodes of the compensator of Fig. 4.11 for the two different cases of V_{out} of 0.8 and 1.2V with load current of 150mA. The output ripples are only $6mV_{pp}$ in the two cases. Both the inductor and load currents are shown in Figures. 4.18 and 4.19 for the two cases with load current ripples in the order of $1mA_{pp}$.

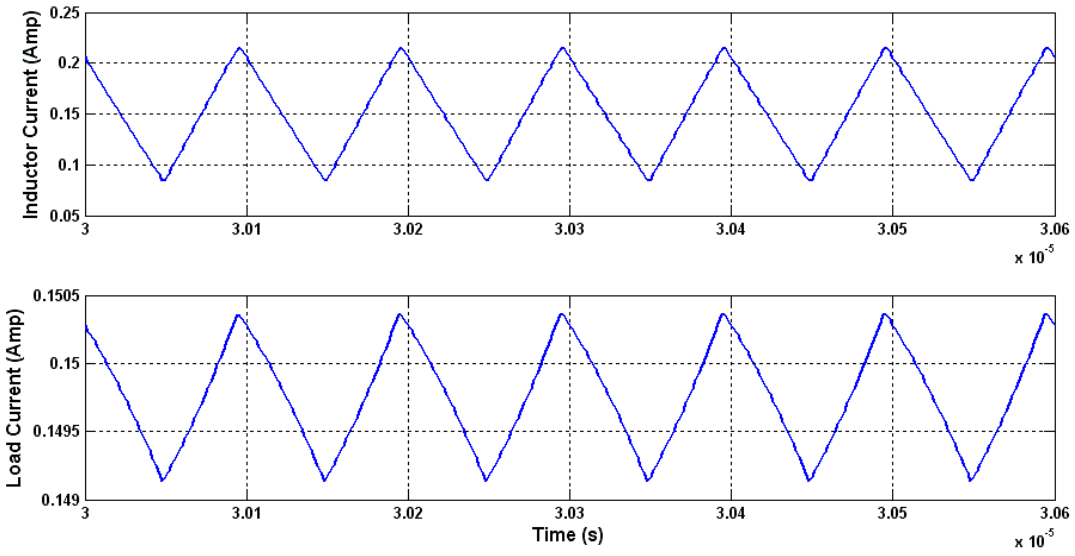


Fig. 4.18 Waveforms of inductor and load currents for 150mA load current and V_{out} of 0.8V.

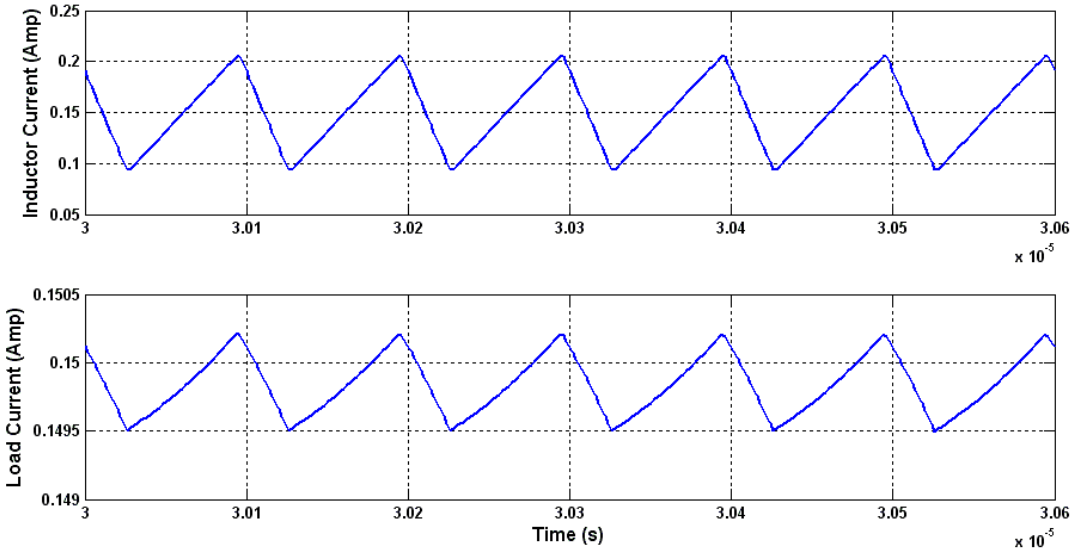


Fig. 4.19 Waveforms of inductor and load currents for 150mA load current and V_{out} of 1.2V.

The simulated power efficiency, defined as the output power divided by the input power of the converter, at f_s =10MHz is shown in Fig. 4.20 with a peak efficiency of 96% at 100mA load current and 1.8V input.

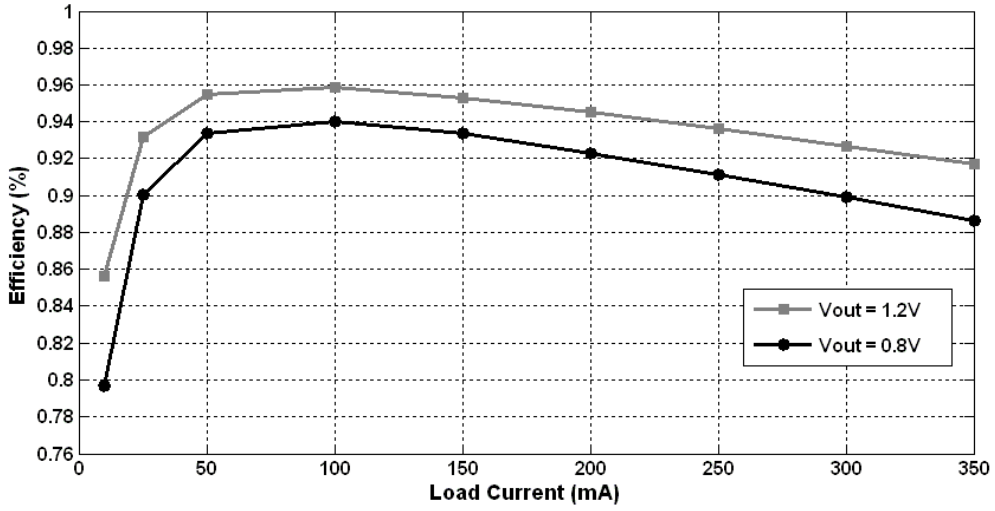


Fig. 4.20 Simulated power efficiency of the buck converter.

4.6 Measurement Results

Measurement setup is shown in Fig. 4.21. Two small sense resistors R_{s1} and R_{s2} of 100mΩ each are used to sense the input and output currents, respectively, where the voltage across the resistors are measured using two oscilloscopes. Two different supplies are used for the analog and digital supplies (V_{DDA} and V_{DDD}) and the two grounds are also separated on the PCB for better isolation.

The measured power efficiency is shown in Fig. 4.22 where a peak efficiency of 75% is achieved at f_s of 20MHz and it is increased to 81% at f_s of 10MHz at V_{in} =1.8V and V_{out} =1.2V. It is still better than using a linear regulator of 66.6% maximum efficiency (1.2/1.8) down to a load current of 80mA.

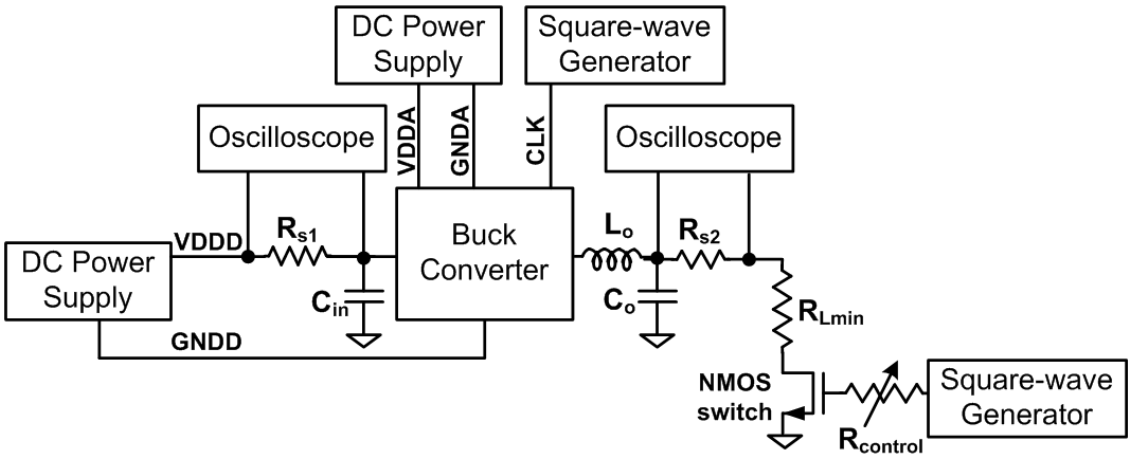


Fig. 4.21 Buck converter test setup.

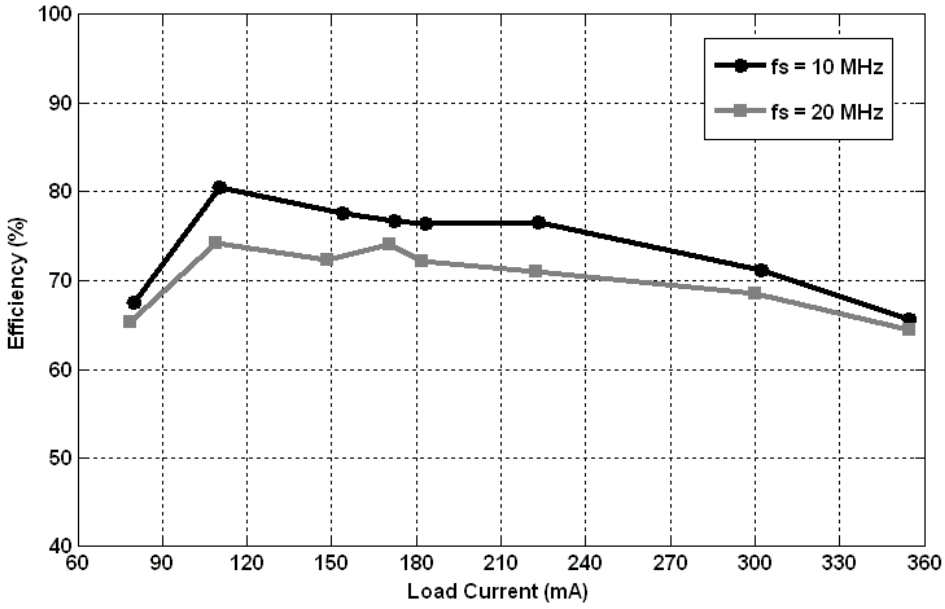


Fig. 4.22 Measured power efficiency of the buck converter at V_{in} =1.8V and V_{out} =1.2V.

The main reason of low efficiency is the high switching losses at the power drivers at high f_s. These losses were not clear in simulations because the transistors used are not modeled as power transistors in the first place. Using better power transistors would definitely reduce the discrepancy between measurements and simulations. Another issue also is the high frequency coupling between traces on the testing PCB which results in not having clean quiet grounds. This adds up to the total losses and degrades efficiency.

Load transient response is measured through switching load current between zero and 350mA using an NMOS switch as shown in Fig. 4.21. With V_{in} =1.8V and V_{out} =1.2V, Fig. 4.23 shows the load transient response at f_s =10MHz while Fig. 4.24 shows it at f_s =20MHz. As shown in both figures, maximum settling time is 22µs at f_s =10MHz while it is 15µs at f_s =20MHz on switching from on to off. Small overshoots and

undershoots with a maximum of 35mV in the 10MHz case are observed. Voltage ripples are less than $15mV_{pp}$ for f_s =10MHz and less than $10mV_{pp}$ for f_s =20MHz.

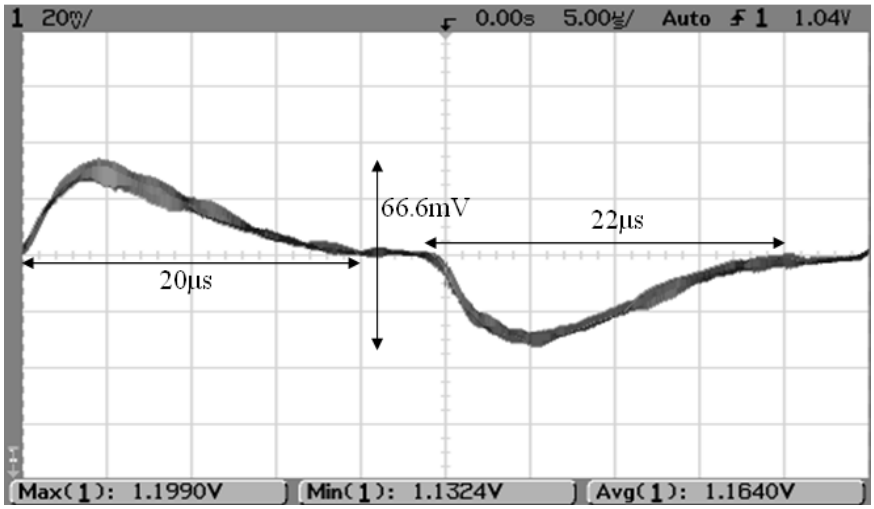


Fig. 4.23 Measured load transient response for a load current switched between zero and 350mA for f_s =10MHz.

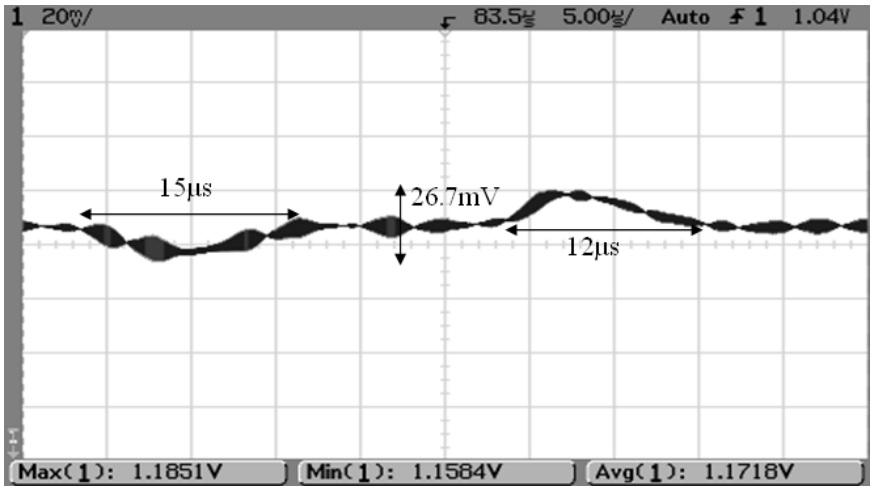


Fig. 4.24 Measured load transient response for a load current switched between zero and 350mA for fs =20MHz.

Table 4.2 shows the key performance parameters of the converter. V_{in} ranges from 1.8 to 2.6V while V_{out} ranges between 0.8 and 1.2V with maximum load current of 350mA. Total I_Q is only 25µA at f_s of 10MHz and 48µA at f_s of 20MHz.

Chip die photo is shown in Fig. 4.25 where the silicon active area is only $0.126mm^2$ that is 26% of the chip total area including pads.

In comparison to state-of-the-art buck converters with high switching frequencies (with all different values of f_s, V_{in}, V_{out}, L_o and C_o as well as different technologies), the proposed converter achieves a very good transient response in terms of fast settling time and small ripples with very small area and quiescent power consumption. On the other side the efficiency is not that high. However this degradation in efficiency is not due to the proposed architecture which is well proven to be working properly but rather due to some modeling and isolation issues which can be taken care of in future work.

Table 4.2 Buck converter chip performance summary.

Technology	0.18 µm CMOS	
Total chip area	0.48 mm^2	
Active area	0.126 mm^2	
External inductor	330 nH	
External capacitor	2 µF	
Input voltage range	1.8 – 2.6 V	
Output voltage range	0.8 – 1.2 V	
Maximum load current	350 mA	
Switching frequency	20 MHz	10 MHz
Quiescent current	48 µA	25 µA
Settling time	15 µs	22 µs
Peak efficiency	75%	81%
Voltage ripples	10 mV_{pp}	15 mV_{pp}

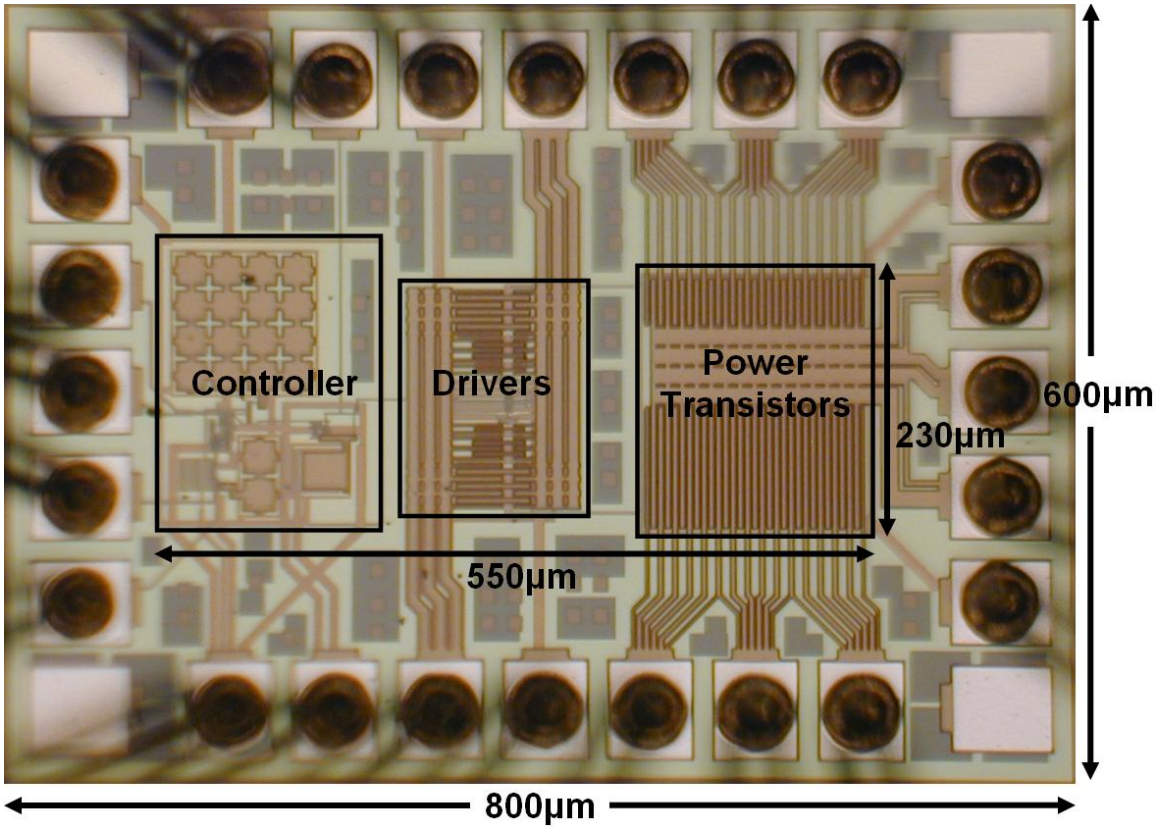


Fig. 4.25 Buck converter chip die photo.

4.7 Conclusion

In this chapter a buck converter switching at high f_s between 10 and 20MHz is presented. The converter achieves a good efficiency that is better than linear regulators with very small area and quiescent power consumption compared to conventional buck converters. There is still a space for further improvements through using additional techniques to reduce the switching losses in the power drivers and find better ways to isolate the traces with high switching activity on the testing PCB so as to minimize coupling to other traces. In conclusion, the proposed converter proves the possibility of

adopting the simple and fast PWM controller with Type III compensation to be utilized in buck converters of high f_s while consuming very low I_Q as well as small silicon area.

CHAPTER V

SWITCHABLE HARMONIC MIXER FOR DUAL BAND MILLIMETER WAVE RECEIVER

5.1 Introduction

The increasing demand for high-data-rate communications, and the congestion of the low-gigahertz frequency bands necessitate moving to the largely unused spectrum at millimeter-wave (mm-wave) frequencies for the continuously increasing wireless applications in the communication market. Some system applications include the IEEE 802.16 wireless metropolitan-area network (WiMAN) for point-point wireless communications at the 10–66 GHz frequency range, automotive short-range and long-range radars for collision avoidance at 22–29 and 77GHz, and cognitive radios. Several CMOS and BiCMOS single-band transceivers are reported in literature for mm-wave applications [27]–[37]. Combining multiple bands is very appealing for mm-wave transceivers on silicon to increase the flexibility and save the chip area.

5.1.1. Single Band Receivers

Single-band receivers at mm-wave frequencies have been the main focus of many literature until now. The first 24-GHz CMOS front end in a 0.18μm process was reported in [27]. A receiver front end that incorporated a folded microstrip geometry to create resonance at the 60-GHz band in a common-gate low-noise amplifier (LNA) and active quadrature mixers was realized in 0.13μm CMOS technology [28]. A fully integrated 8-channel phased-array heterodyne receiver at the 24-GHz industrial-scientific-medical

(ISM) band in BiCMOS technology is reported in [29]. Receiver chip sets for gigabit per second wireless communications in the 60-GHz ISM band in BiCOMS and CMOS technologies were demonstrated in [31]–[35]. A fully integrated phased-array receiver with integrated dipole antennas for long-range automotive radar applications at 77GHz was designed and fabricated in a 0.12μm BiCMOS process in [37]. As can be seen, most of the efforts have concentrated on developing the first generation of single-band commercial silicon receivers at 24, 60, and 77GHz.

5.1.2. Dual Band Receivers: Advantages and Challenges

A mm-wave dual/multiband silicon-based receiver is necessary to reduce the size and cost of the transceiver to avoid several front ends for each band. These receivers will be necessary to cover the 10–66 GHz frequency range for many applications occupying different bands, such as wireless applications. A similar requirement exists for low-gigahertz applications, such as WiFi at 2.4GHz and 5.2GHz.

Dual/multiband receivers' design poses many challenging problems at mm-wave frequencies. First: frequency synthesizers need to span over a very wide frequency range to cover the entire band of interest. As a result, they are power hungry or very hard to implement due to the wide tuning range of a voltage-controlled oscillator (VCO). Second: front-end building blocks including LNA and mm-wave mixers have to support a very wide frequency range. Hence, receiver architectures, which rely on frequency synthesizers running at lower frequencies and new front-end topologies, which support the multi-gigahertz frequency range need to be developed to overcome the aforementioned challenges.

The first dual-band 22–29/77–81 GHz transceiver for automotive radars has been recently reported using BiCMOS technology [38]. The transceiver is based on a direct conversion receiver architecture along with a dual-band LNA and frequency synthesizer. To avoid having a very wide tuning range of the VCO, this receiver architecture uses two local oscillators (LOs) for each separate band. In addition, these LOs have to run at 22 and 77GHz, which result in high power consumption. This receiver shows that direct conversion receivers are not suitable for multiband operation at mm-wave frequencies because of the limited tuning range of the LO. To the best of our knowledge, there is no other reported dual/multiband silicon-based radio at mm-wave frequencies.

5.1.3. Proposed Solution

A new dual-band receiver architecture to downconvert the ISM and local multipoint-distribution system (LMDS) bands at 24 and 31GHz, respectively, is proposed [39]. The receiver is targeted for the single carrier wireless metropolitan-area network standard (IEEE 802.16). The IEEE 802.16-SC is specified for the 10–66 GHz applications. This standard supports channel bandwidths of 20, 25, and 28MHz, with quadrature phase-shift keying (QPSK), 16-quadrature amplitude modulation (QAM) and 64-QAM modulation schemes for bit rates up to 134Mb/s [40]. In the proposed architecture, each of the 24- and 31-GHz bands has a bandwidth of 250MHz, including 9 channels with 25MHz bandwidth and QPSK modulation. The receiver relies on a switchable harmonic mixer for band selection. The switchable harmonic mixer allows the LO to run at a lower frequency, hence eliminating the need for a wideband VCO (first challenge). In addition, new circuit techniques for a wideband LNA and wideband mm-

wave mixer are employed to cover the frequency band of interest and to further reduce the power consumption (second challenge). The receiver is implemented using 0.18μm SiGe BiCMOS technology ($f_{T,BJT}/f_{max,BJT}$=70/170 GHz/GHz).

5.2 Dual Band Millimeter Wave Receiver

5.2.1. System Basic Idea

The proposed receiver architecture and its frequency planning are demonstrated in Figs. 5.1 and 5.2, respectively. Similar to the heterodyne receiver, the desired band is downconverted to baseband through an intermediate frequency f_{IF}. The two frequency bands, at 24 and 31GHz, are initially amplified using a two-stage wideband LNA. Then, a wideband mm-wave mixer and a LO(LO1) running at f_{LO1} = 10.25GHz (effective mixing frequency is 20.5GHz) is used to downconvert the 24- and 31-GHz bands to intermediate frequencies of 3.5 and 10.5GHz, respectively. The second mixing stage is a switchable harmonic mixer (SWHM) for band selection and final downconversion of signals to baseband. The second LO (LO2) operates at a frequency of f_{LO2} = 3.5GHz and the band selection is achieved by either mixing the input signal with the fundamental or third-order harmonic component of LO2. The IF amplifier is used to filter out higher unwanted frequency components, drive the high input capacitance of the switchable harmonic mixer, and provide higher gain at the upper band to compensate the 9-dB systematic gain difference between the lower and upper bands due to SWHM as discussed later.

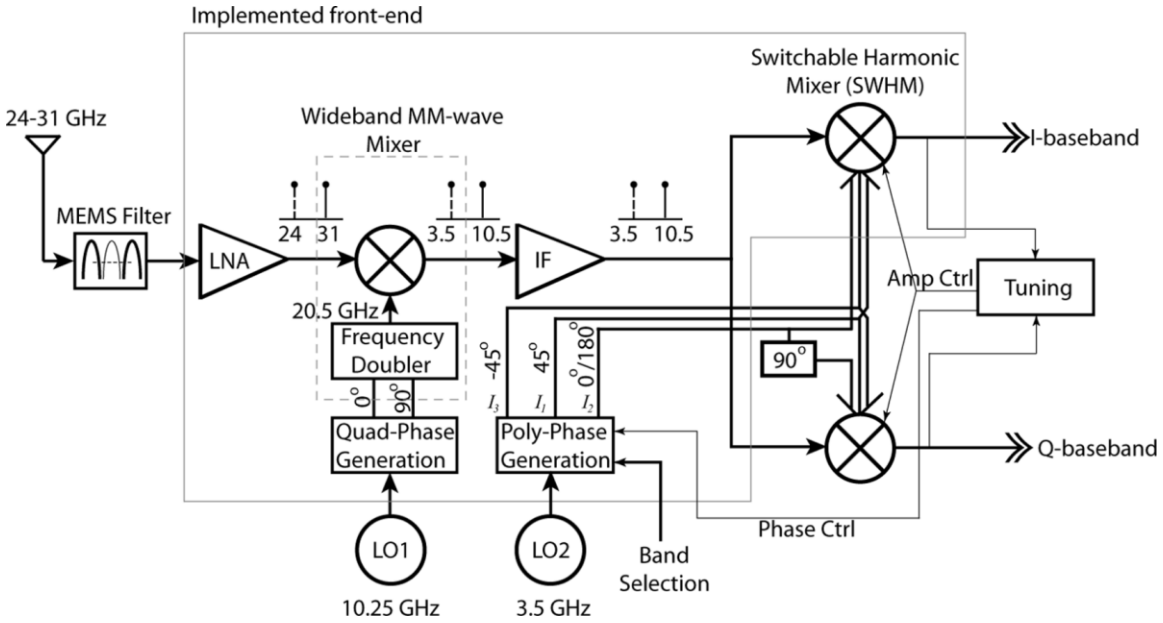


Fig. 5.1 Block diagram of the switchable harmonic receiver architecture.

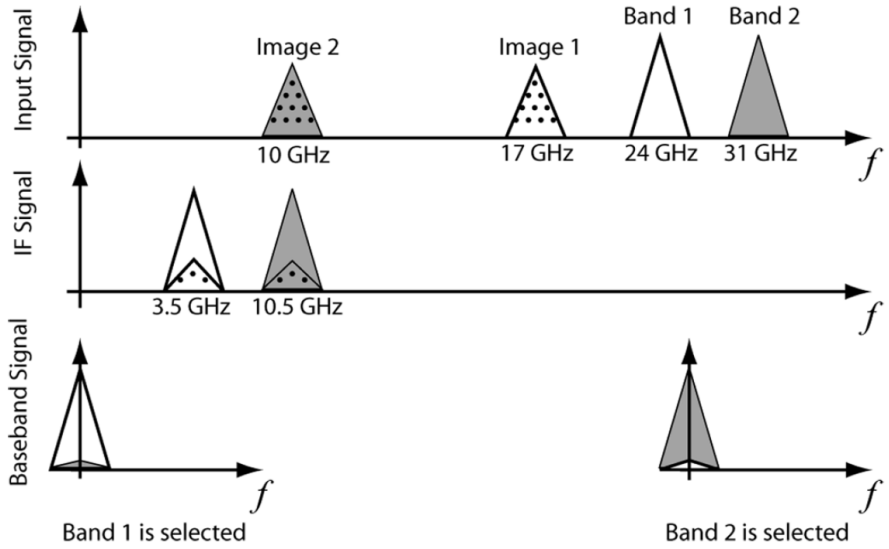


Fig. 5.2 Frequency planning of the switchable harmonic receiver (channel bandwidth = 25MHz, total RF band bandwidth = 250MHz).

The basic idea of the band selection is to adjust the harmonics of the second mixing stage. If the 24-GHz band is desired, the second mixing stage mixes the input signal with the 3.5GHz fundamental component, and the third-order harmonic component at 10.5GHz is suppressed. On the other hand, if the 31-GHz band is desired, the fundamental component of the second oscillator is suppressed and the third harmonic component, at 10.5GHz, is amplified. Since the architecture is based on a heterodyne scheme, the LNA should provide image rejection to achieve a high signal-to-noise ratio (SNR) from the received data. If the image rejection provided by the LNA is not sufficient for the necessary rejection, an external bandpass filter (such as a switchable RF micro-electro-mechanical-system (MEMS) filter at 24–31 GHz similar to the one reported in [41]) can be added in front of the receiver to remove unwanted image signals that are placed at 17 and 10GHz for the 24- and 31-GHz frequency bands, respectively.

To demonstrate the advantage of the proposed receiver architecture, it is compared to one of the existing Weaver-based dualband receivers [42]. The Weaver-based architecture requires a LO running at 27.5GHz compared to one running at 20.5GHz in the proposed architecture. Having a lower oscillating frequency reduces the power consumption while achieving better phase noise. For the second mixing stage, both architectures are using the same LO frequency. Another advantage is that the Weaver architecture requires two mixers operating at 27GHz compared to a single mixer operating at 20.5 GHz, thus reducing the power consumption as well as the complexity in the layout due to the coupling among various components. It is important to mention that both architectures require a tuning scheme, such as least mean square (LMS), to

efficiently reject one of the bands and receive the desired one [43]. In this implementation, two control lines are used for external tuning (Fig. 1). The first one adjusts the phase error, while the other one adjusts the gain error.

5.2.2. Switchable Harmonic Mixer Mathematical Analysis

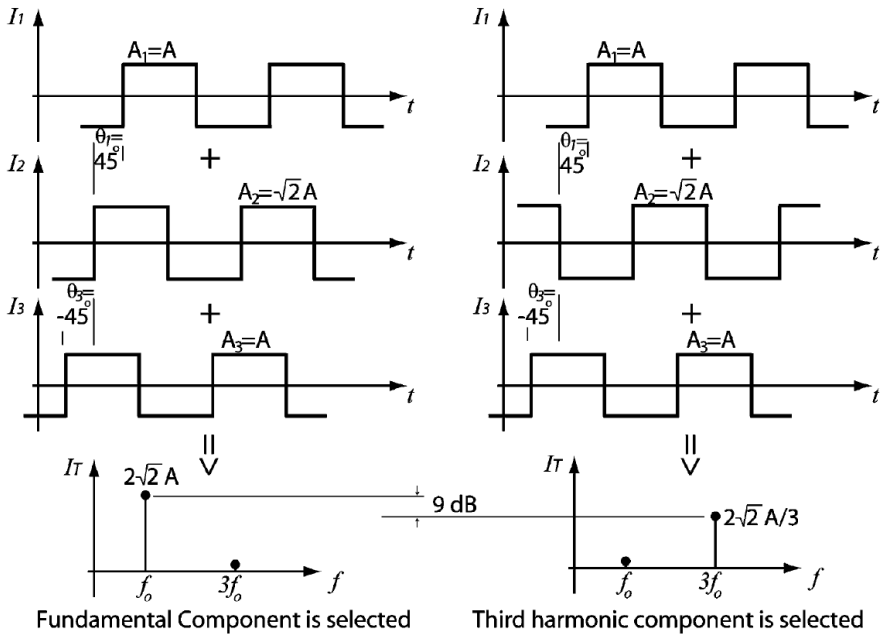


Fig. 5.3 Basic idea of the switchable harmonic mixer.

The SWHM mixes the input signal at 3.5 or 10.5GHz with either f_{LO2} or $3 \cdot f_{LO2}$, respectively. Fig. 5.3 demonstrates the basic idea of the mixer, where a single LO source with three different phases is required to mix the input signal with the fundamental or the third-order harmonic, and suppress unwanted components. The three waveforms are considered square waves because this is the effective signal seen by any Gilbert-cell-based mixer. The fundamental or third harmonic components cancellation is achieved by

summing the three LO signals I_1, I_2 and I_3, with proper phase and amplitude scaling. Using Fourier series analysis, the three waveforms are written in terms of their first five harmonics as follows:

$$\begin{aligned} I_1 &= A_1 \cdot [\cos(\omega t + \theta_1) - \frac{1}{3}\cos(3\omega t + 3\theta_1) + \frac{1}{5}\cos(5\omega t + 5\theta_1)], \\ I_2 &= A_2 \cdot [\cos(\omega t) - \frac{1}{3}\cos(3\omega t) + \frac{1}{5}\cos(5\omega t)], \\ I_3 &= A_3 \cdot [\cos(\omega t + \theta_3) - \frac{1}{3}\cos(3\omega t + 3\theta_3) + \frac{1}{5}\cos(5\omega t + 5\theta_3)]. \end{aligned} \tag{5.1}$$

where A_1, A_2, and A_3 are the amplitudes of the three different waveforms, and θ_1 and θ_3 are phase shifts. In these equations, I_2 is selected as the reference signal and, therefore, $\theta_2 = 0$. The effective mixing signal I_T is generated by summing the three waveforms as follows:

$$I_T = I_1 + I_2 + I_3. \tag{5.2}$$

With assumptions of $\theta_1 = -\theta_3$ and $A_1 = A_3$, the effective mixing signal can be written as follows:

$$\begin{aligned} I_T &= \left[(2A_1\cos(\theta_1) + A_2) \cdot \cos(\omega t)\right] \\ &- \frac{1}{3}\left[(2A_1\cos(3\theta_1) + A_2) \cdot \cos(3\omega t)\right] \\ &+ \frac{1}{5}\left[(2A_1\cos(5\theta_1) + A_2) \cdot \cos(5\omega t)\right]. \end{aligned} \tag{5.3}$$

The fundamental or the third harmonic component in (5.3) is eliminated by adjusting the values of amplitudes and phases of three waveforms I_1, I_2 and I_3. Several amplitudes and phases can perform this functionality. Fig. 5.4 shows the required amplitude ratio A_2/A_1 for each value of θ_1 to cancel either the fundamental or the third harmonic component. Among these solutions, three practical sets are selected.

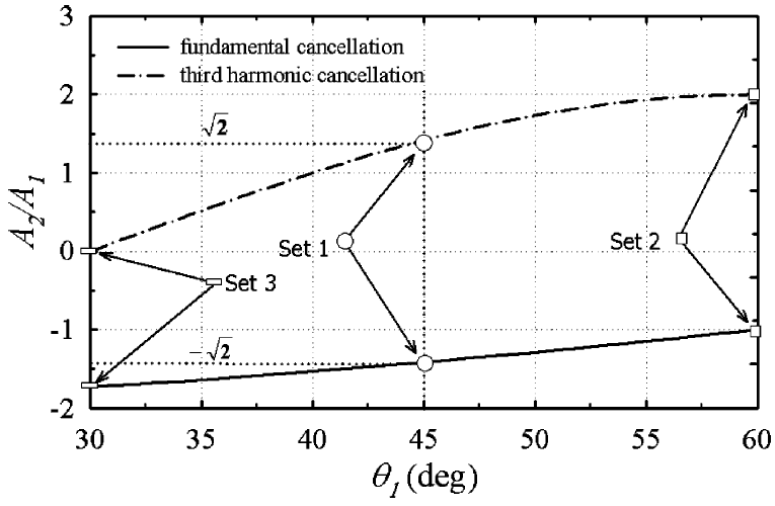


Fig. 5.4 Phase and amplitude conditions for the fundamental or third harmonic component cancellation.

Table 5.1 Coefficients values of the switchable harmonic mixer for three possible combinations ($A_1 = A_3$).

	Set 1		Set 2		Set 3	
Coefficients	$A_1 = -A_2/\sqrt{2}$ $\theta_1 = -\theta_3 = 45^o$	$A_1 = A_2/\sqrt{2}$ $\theta_1 = -\theta_3 = 45^o$	$A_1 = -A_2$ $\theta_1 = -\theta_3 = 60^o$	$A_1 = A_2/2$ $\theta_1 = -\theta_3 = 60^o$	$A_1 = -A_2/\sqrt{3}$ $\theta_1 = -\theta_3 = 30^o$	$A_1, A_2 = 0$ $\theta_1 = -\theta_3 = 30^o$
f_o component	0	$2\sqrt{2} \cdot A_1$	0	$3 \cdot A_1$	0	$\sqrt{3} \cdot A_1$
$3f_o$ component	$2\sqrt{2}/3 \cdot A_1$	0	$2 \cdot A_1$	0	$1/\sqrt{3} \cdot A_1$	0
$5f_o$ component	$2\sqrt{2}/5 \cdot A_1$	0	0	$3/5 \cdot A_1$	$2\sqrt{3}/5 \cdot A_1$	$\sqrt{3}/5 \cdot A_1$

Table 5.1 summarizes coefficients and component values for these sets. For the proposed receiver, the first set ($\theta_1 = -\theta_3 = 45^o$) is selected because it reduces the hardware complexity. For this set, only the phase of I_2 controls the band selection by changing its polarity. The lower frequency band is selected by tuning the switchable harmonic mixer for $A_1 = A_3 = A_2/\sqrt{2}$, and the upper frequency band is selected by adjusting the mixer to $A_1 = A_3 = -A_2/\sqrt{2}$. On the other hand, sets 2 and 3 require a polarity and amplitude

change of A_2 to perform the band selection, and add to the complexity of the receiver implementation. Another advantage of selecting the 45^o phase shift is in the Q-mixer implementation shown in Fig. 5.1. Only an additional 90^o phase shift is required for the I_2 signal. The 90^o is inherently generated for the I_1 and I_3 signals. This is because shifting I_1 (I_3) by 90^o provides the inverted signal of I_3 (I_1), which is already used to drive the I-mixer. This is not the case for sets 2 and 3 and, therefore, the 45^o phase shift relaxes the receiver complexity.

Table 5.1 also shows the conversion gain of the mixer for each frequency component. For set 1, there is a systematic gain difference of 9dB between the fundamental and the third harmonic component. This systematic gain difference is adjusted by using the IF amplifier, to provide a flat gain for both frequency bands. Having an almost constant gain for both bands reduces the overall power consumption by relaxing the noise figure and IIP3 requirements of the following blocks [44].

The idea of harmonic rejection/selection is verified using SIMULINK simulations and results are shown in Fig. 5.5. As depicted, the third and fundamental components are suppressed by adjusting the proper values of coefficients. Higher order harmonics are easily filtered out by using a low-pass filter in the baseband section. The proposed switchable harmonic receiver is not limited to the fundamental or the third-order harmonic components, and can be applied to higher order harmonics.

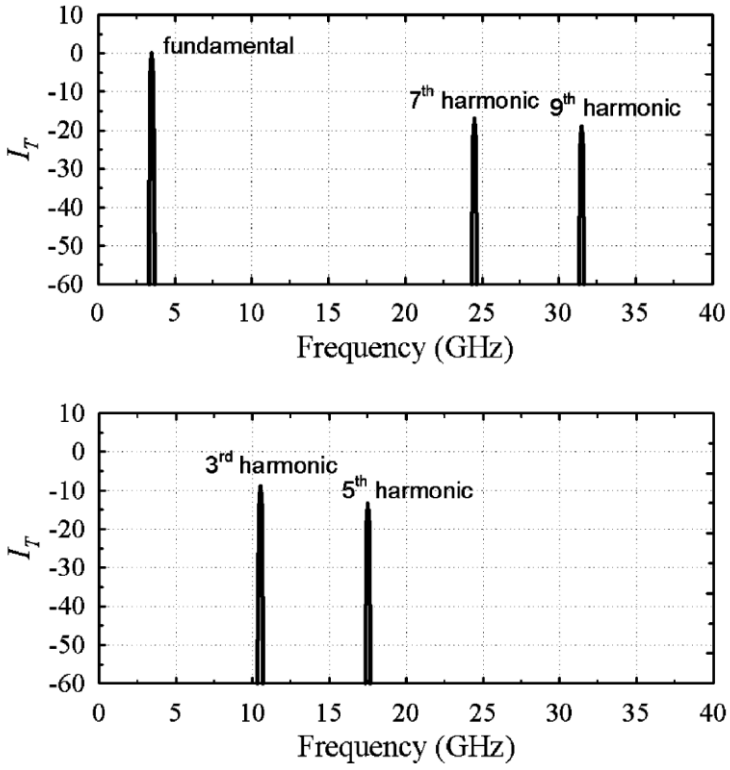


Fig. 5.5 Simulated spectrum of I_T using Simulink when the third harmonic component (top) or fundamental component (bottom) is cancelled using the information of set 1 in Table 5.1.

5.2.3. Frequency Planning

The proposed dual-band switchable harmonic receiver architecture can be employed to downconvert any arbitrary pair of frequency bands by properly selecting the frequencies of the LOs. Since the two bands are downconverted to baseband then they can be written as follows:

$$\begin{aligned} f_{band1} &= f_{LO1} + f_{LO2}, \\ f_{band2} &= f_{LO1} + 3f_{LO2}. \end{aligned} \tag{5.4}$$

where f_{LO1} and f_{LO2} are frequencies of the LOs shown in Fig. 5.1, while f_{band1} and f_{band2} are the lower and upper frequencies of the two desired bands. Thus, the equation used to calculate f_{LO1} and f_{LO2} based on the required bands are given as:

$$f_{LO1} = \frac{3f_{band1} - f_{band2}}{2}, \qquad f_{LO2} = \frac{f_{band2} - f_{band1}}{2}. \tag{5.5}$$

For the 24- and 31-GHz bands, f_{LO1} and f_{LO2} are 20.5 and 3.5GHz, respectively. In this architecture, f_{LO1} is further reduced to 10.25GHz by using a frequency doubler to reduce the power consumption of the LO generation circuitry. In this receiver, the total RF band bandwidth is less than 250MHz and, therefore, the third harmonic of LO1 at 30.75GHz is not important. However, if the targeted application bandwidth is higher than 250MHz, then the frequency doubler may not be used and, hence, f_{LO1} has to be 20.5GHz.

5.3 Circuit Implementation

5.3.1. Switchable Harmonic Mixer

Fig. 5.6 shows the implementation of the SWHM. The mixer consists of three Gilbert-cell mixers each driven with an LO signal having a different phase. According to Table 5.1, the middle mixer provides a conversion gain √2 times higher than the other two mixers. This is achieved by scaling the transconductance value of M_2 to a value of √2 times higher than the transconductance value of M_1 and M_3. This is achieved by increasing the biasing current through the transistor M_{B2} and its size. Only increasing the size of M_2 increases the parasitic capacitance at its drain and, hence, attenuates the signal close to 10.5GHz. The current of the middle mixing stage can be adjusted in an automatic

tuning scheme, which is not implemented in this receiver, to overcome the finite amount of rejection of the unwanted band due to process mismatches and variations. NMOS RF transistors are chosen for the RF input stage to minimize the loading on the preceding stage in the receiver. Also, they have the advantage of better linearity compared to bipolar junction transistors (BJTs), which need some linearization technique and make the matching between the three mixing cells a harder design problem. The biasing transistors M_{B1}, M_{B2}, and M_{B3} are designed to be large enough to reduce the overdrive voltage for higher voltage headroom, and to help increase the matching between the devices. BJTs are used for the LO input stage to minimize the flicker noise of the switches. In addition, bipolar transistors require a small LO signal amplitude (≈100mV) for switching. The number of base fingers of each bipolar transistor is increased to reduce its generated output noise.

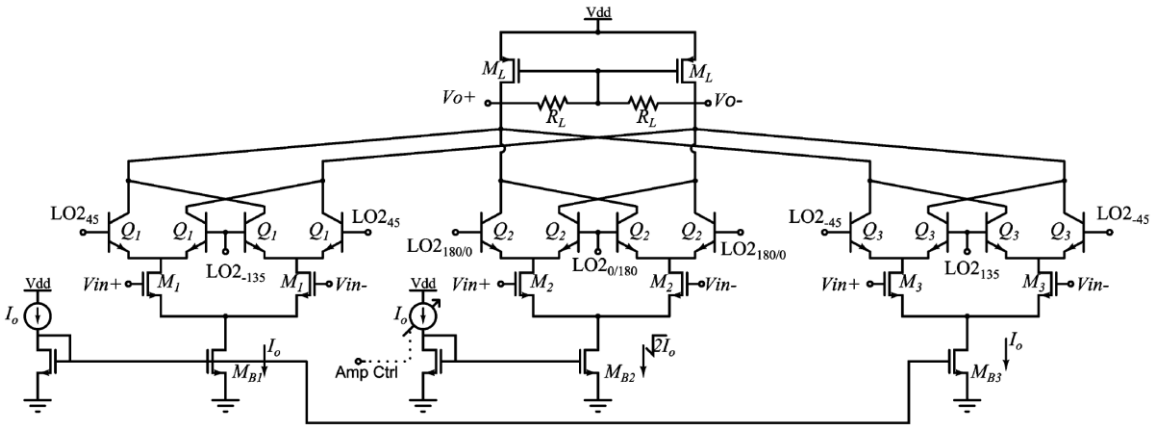


Fig. 5.6 Architecture of the switchable harmonic mixer. Selection of either the fundamental or the third-order harmonic component is achieved by changing the phase of the middle mixing stage.

The PMOS current steering technique is used to increase the conversion gain and available headroom as shown in Fig. 5.6. Current steering is implemented through the transistor M_L and resistor R_L. This is because the output dc voltage is determined by the gate overdrive voltage of PMOS devices. During ac operation, the passive resistor R_L appears and controls the conversion gain. This technique does not require a common-mode feedback circuit since R_L provides a local feedback to stabilize the output dc voltage. The area of PMOS transistors is increased to minimize their flicker noise contribution at the output. The flicker noise of M_1, M_2, and M_3 will be upconverted to f_{LO2} [44]. Slight degradation in the linearity is observed due to the nonlinear output resistance of PMOS transistors.

The LO signals are driven from the same source, and they have the same frequency of 3.5GHz but are different in phase, according to Table 5.1. This mixer provides downconversion of the signals at 3.5 and 10.5GHz, which are the IF frequencies of the 24- and 31-GHz frequency bands. The fundamental (3.5GHz)/ third-order harmonic (10.5GHz) selection is achieved by controlling the phase of the input LO signal of the middle mixer in Fig. 5.6. If the phase of LO signal is 0^o, then the fundamental component is selected while the third harmonic component is rejected. On the other hand, if the phase is 180^o, then the third harmonic component is selected and the fundamental one is rejected. This approach enables the use of a single switch to control the required band selection.

5.3.2. IF Amplifier

The proposed SWHM has a high input capacitance due to employing three mixing stages. This input capacitance can limit the performance of the previous stage (mm-wave mixer) at higher frequencies. Reducing the input capacitance comes at the cost of reducing the conversion gain and increasing the noise figure. To overcome this problem, an IF amplifier is located between the mm-wave and switchable harmonic mixers as a buffer. This amplifier, shown in Fig. 5.7, employs shunt peaking, with a differential inductor L_d of 1.1nH, to provide higher gain at the 10.5-GHz band.

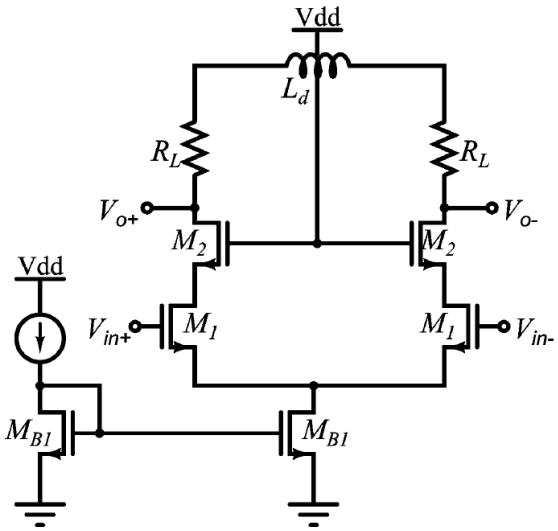


Fig. 5.7 IF amplifier with shunt peaking.

Fig. 5.8 shows the simulated gain and noise figure of the IF amplifier. The IF amplifier provides gain of -6dB and 7.7dB, and a noise figure of 12.3dB and 10.5dB at 3.5GHz and 10.5GHz, respectively. The higher gain at the 10.5-GHz band is necessary to compensate for the systematic gain difference of 9 dB between the two bands as pointed

out in Table 5.1 and the gain reduction due to the parasitic capacitances. The 6-dB loss at 3.5GHz is not problematic because the mixer has higher gain at this band. Increasing the size of the input transistor M_1 in Fig. 5.7 to avoid the 6-dB loss is not possible because it would lower the gain of the previous stage. The cascode architecture is used to ensure stability of the amplifier.

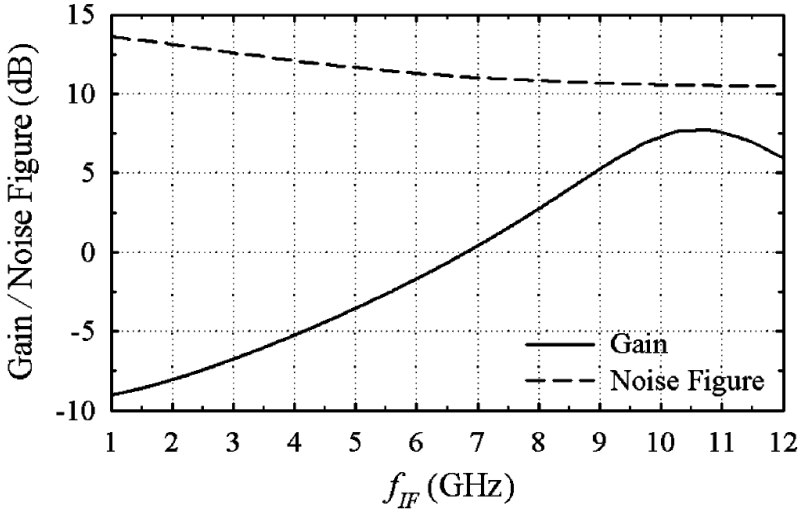


Fig. 5.8 Post-layout simulations of the conversion gain and noise figure of the IF amplifier.

5.3.3. Polyphase Generator

A two-stage polyphase shifter, shown in Fig. 5.9, is used to generate the required $\pm 45^o$ phase shifts precisely with the drawback of 3-dB loss [45]. Simulations across the process corners show a precise phase shift of 90^o between nodes $LO2_{45}$ and $LO2_{-45}$ in Fig. 5.9 as long as nodes 1 and 2 are not loaded. The $0^o/180^o$ phase shifts are taken from the main LO input signal (LO_{main+}, LO_{main-}) to reduce the loading on nodes 1 and 2, and they are injected to a multiplexer. The control line of this multiplexer determines the

desired band. Due to the additional multiplexer, the phase shift is not $0^o/180^o$, and an additional RC phase shifter, shown in Fig. 5.10, is added to reduce the amount of phase mismatch. The resistance R_o is externally controlled through the transistor M_o to account for the phase mismatch between $LO2_0$ and $LO2_{45}/LO2_{-45}$ and $LO2_{180}$ and that are generated due to process variations. In addition, this phase shifter reduces the amplitude of $LO2_0$, so that the driving amplitude of the switches is the same for the three mixers for better matching. The capacitor C_o is chosen to be double the value of the capacitor C_p of the polyphase filter to almost have the same amplitude for all LO output signals. The phase control voltage $V_{Ø,control}$ in Fig. 5.10 can be used in an automatic tuning scheme to provide the necessary phase correction and, hence, increase the amount of rejection of the unwanted band. Fig. 5.11 shows the variation of the output phase of $LO2_0$ versus $V_{Ø,control}$.

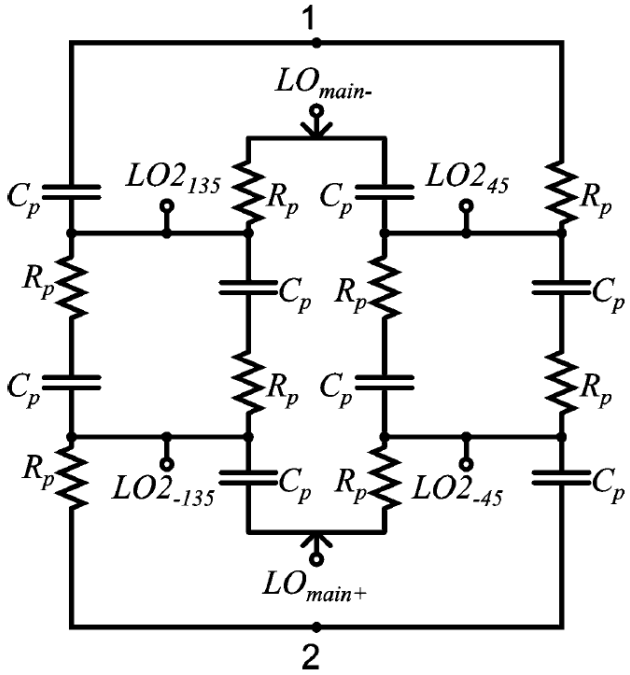


Fig. 5.9 Two-stage polyphase shifter (R_p = 200Ω, C_p = 130fF).

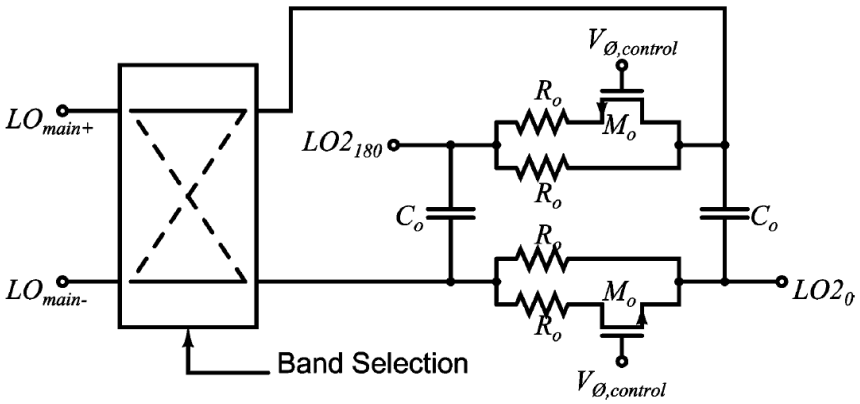


Fig. 5.10 RC phase shifter with electronic tuning (R_o = 170Ω, C_o = 260fF, including loading parasitics).

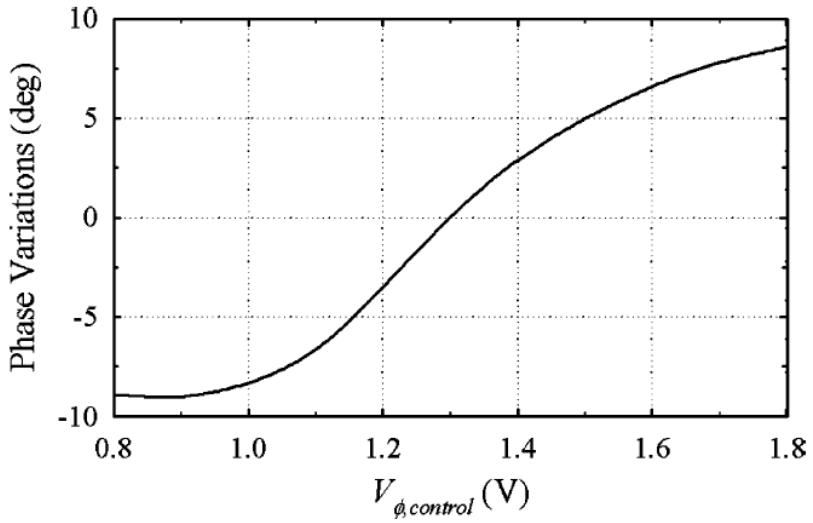


Fig. 5.11 Output phase variation of $LO2_0$ versus $V_{Ø,control}$ of the circuit in Fig. 5.10.

5.4 Simulation and Measurement Results

5.4.1. Simulation Results for the IF Amplifier and Switchable Harmonic Mixer

The post-layout simulation results for the conversion gain, noise figure, and IIP3 of the combined SWHM and IF amplifier versus the amplitude of LO2 are shown in Figs.

5.12–5.14, respectively. In this design, the amplitude of LO2 is adjusted to 100mV to provide sufficient gain and reduce the noise figure of the 10.5-GHz band. At this amplitude, there is degradation of IIP3 at the 3.5-GHz band; however, it is higher than the one at 10.5GHz. Also, simulations show LO-to-RF and 3LO-to-RF isolations of SWHM higher than 100dB, which is expected due to the differential nature of the SWHM.

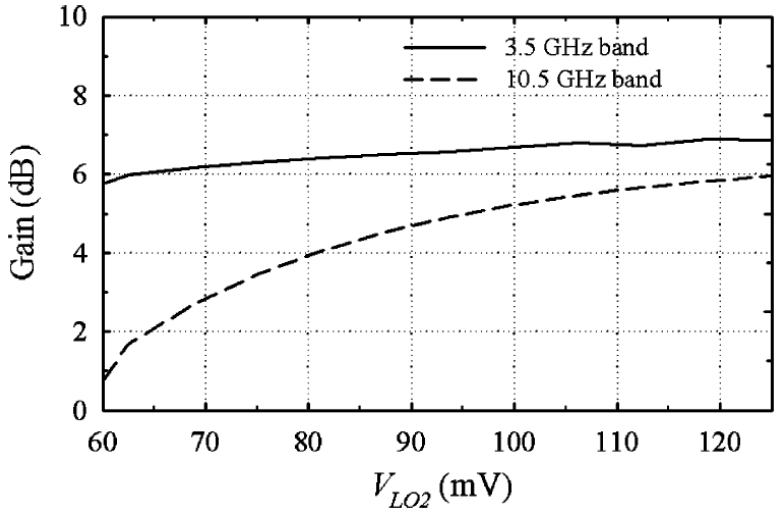


Fig. 5.12 Post-layout simulations of the switchable harmonic mixer and IF amplifier conversion gain for the 3.5- and 10.5-GHz frequency bands versus the LO2 voltage amplitude.

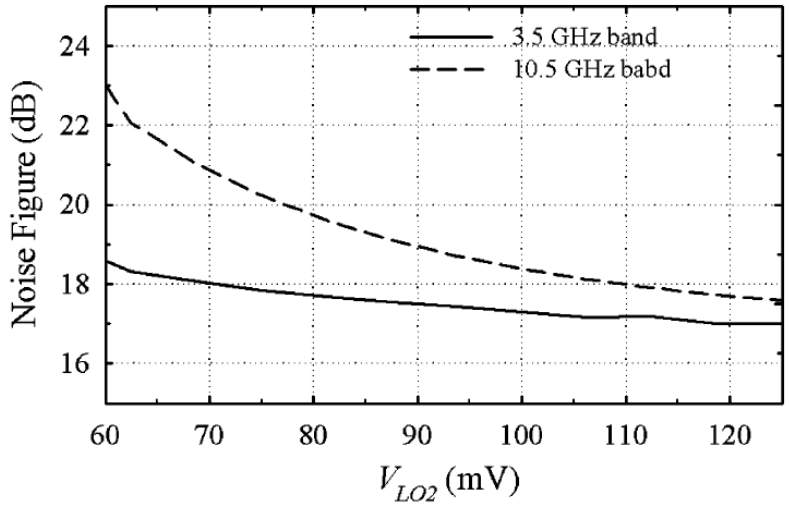


Fig. 5.13 Post-layout simulations of the switchable harmonic mixer and IF amplifier noise figure for the 3.5- and 10.5-GHz frequency bands versus the LO2 voltage amplitude.

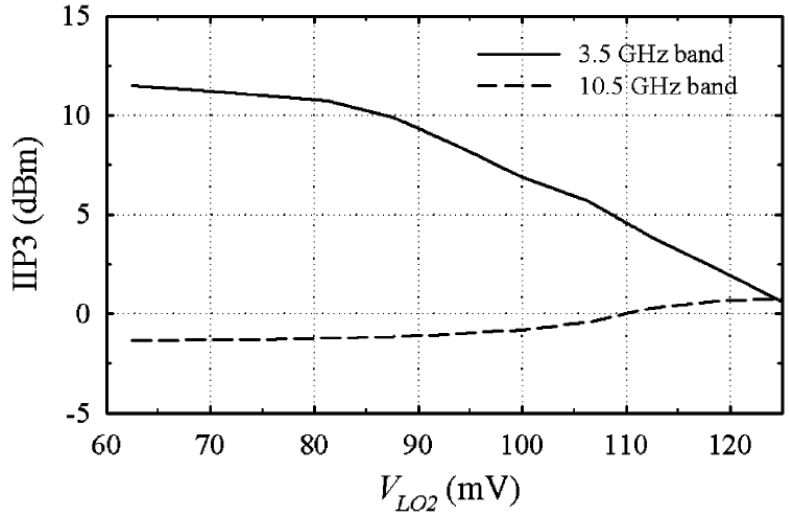


Fig. 5.14 Post-layout simulations of the switchable harmonic mixer and IF amplifier IIP3 for the 3.5- and 10.5-GHz frequency bands versus the LO2 voltage amplitude.

The conversion gain versus the baseband frequency for the 3.5- and 10.5-GHz frequency bands is shown in Fig. 5.15. The mixer has a conversion gain of 6.7 and 5.2dB

for the 3.5- and 10.5-GHz bands, respectively. Only 1.5-dB difference in gain is achieved due to the effect of the gain peaking introduced by the IF amplifier. The conversion gain varies by 1dB across the amplitude tuning range. Simulations also showed a rejection higher than 60dB. This value is hard to achieve without a tuning scheme in the measurement as mentioned previously.

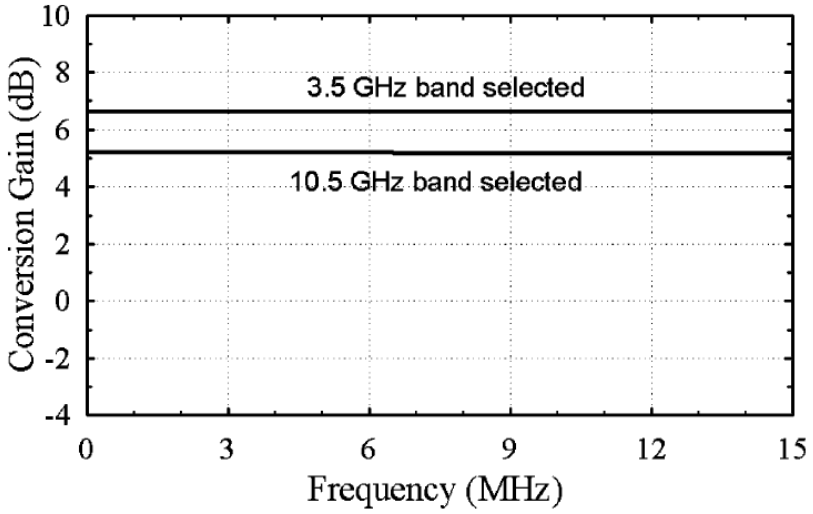


Fig. 5.15 Post-layout simulations of switchable harmonic mixer and IF amplifier conversion gain for the 3.5- and 10.5-GHz frequency bands versus the baseband frequency.

A simulated noise figure of 17.1 and 18dB at baseband are obtained for the 3.5- and 10.5-GHz frequency bands, respectively, with less than 1-dB difference between the two cases. The 10.5-GHz band has slightly higher noise figure due to the additional losses. The IIP3 of the mixer and IF amplifier are 7 and 1dBm for the 3.5- and 10.5-GHz band, respectively. Simulations are performed with a two-tone separation of 10MHz. The IIP3 at 10.5GHz is lower due to the effect of the higher gain introduced by the shunt

peaking IF amplifier. However, the 1dBm IIP3 is still within the required specification. The total current consumptions of the SWHM and IF amplifier are 8 and 7mA from a 1.8V supply, respectively.

Table 5.2 shows a summary of the post-layout simulation results of the SWHM and IF amplifier.

Table 5.2 Post-layout simulation results summary of the switchable harmonic mixer and IF amplifier.

Parameter	Value
Technology	0.18 μm SiGe BiCMOS
LO (GHz)	3.5
RF (GHz)	3.5/10.5
Conversion Gain (dB)	6.7 @ 3.5GHz 5.2 @ 10.5GHz
NF @ 1MHz (dB)	17.1 @ 3.5GHz 18 @ 10.5GHz
IIP3 (dBm)	7 @ 3.5GHz 1 @ 10.5GHz
10.5GHz Rejection (dB)	55
3.5GHz Rejection (dB)	52
Current (mA)	15

5.4.2. Measurment Results for the Complete Switchable Harmonic Receiver

The switchable harmonic receiver is fabricated using 0.18μm BiCMOS technology provided by Jazz Semiconductor. The cutoff frequencies of this technology are 70 and 50GHz for the BJT and MOS transistors, respectively. The die micrograph is

shown in Fig. 5.16, where the total area is 0.7mm^2, excluding pads. An FR-4 printed circuit board (PCB), shown in Fig. 5.17, is designed to test the dual-band receiver. The PCB is used to apply the dc signals, monitor the low-frequency output, and apply the LO signals. The chip is packaged in a quad flat-no-lead (QFN) package. The input signal is injected using a ground-signal-ground (GSG) RF probe to avoid degrading the performance of the receiver. The output of the receiver is applied to an off-chip instrumentation amplifier for the differential-to-single-ended conversion necessary for the measurements. The 3.5- and 10.25-GHz LO signals are applied externally and injected to the chip through Sub-Miniature Type-A (SMA) connectors.

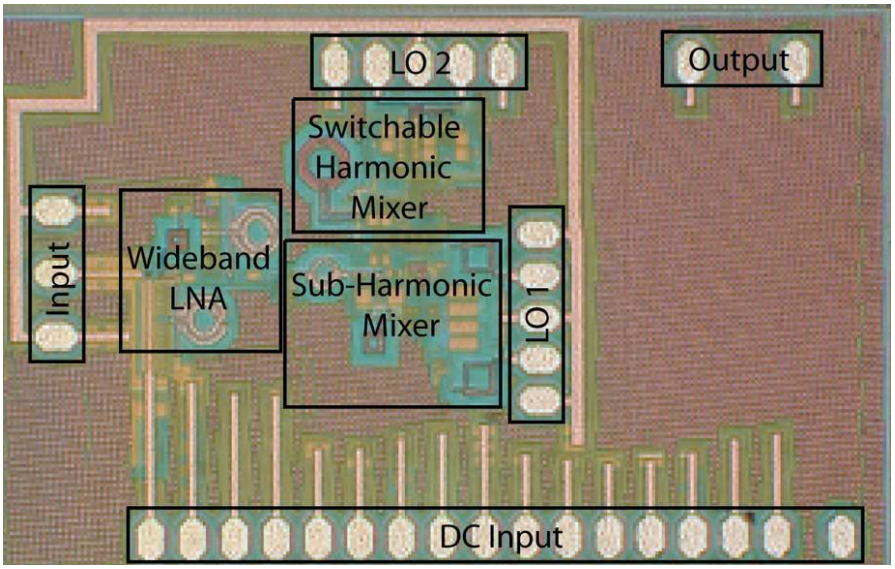


Fig. 5.16 Die photo of the switchable harmonic receiver.

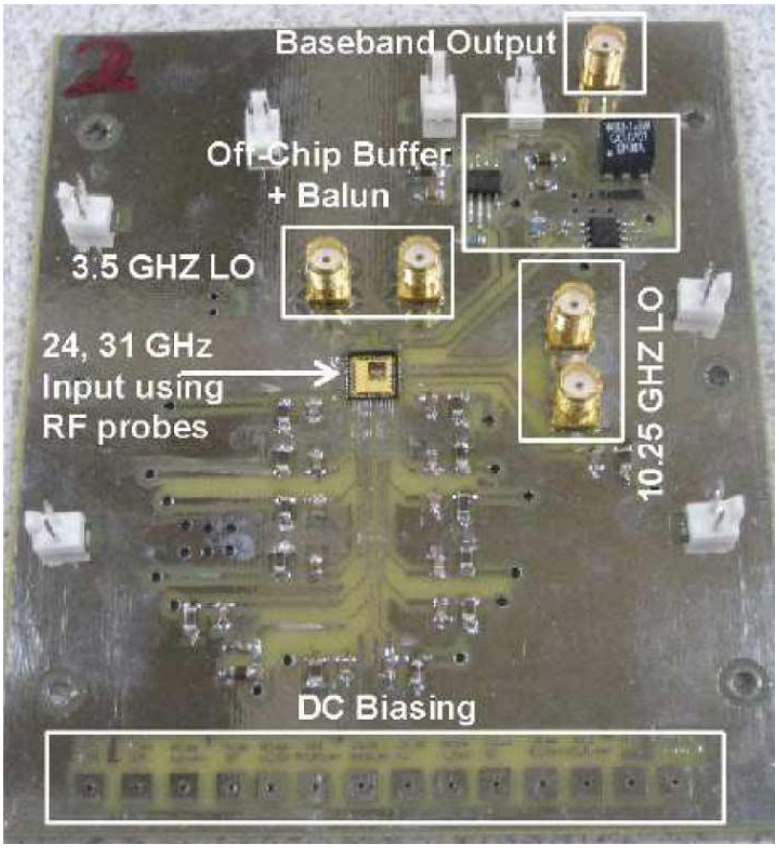


Fig. 5.17 PCB for the switchable harmonic receiver.

Test setup is shown in Fig. 5.18. An Agilent N5230A network analyzer is used to inject the mm-wave signal and to measure the reflection coefficient of the LNA. LO signals are applied using the HP-8673C signal generator and HP 8719ES network analyzer.

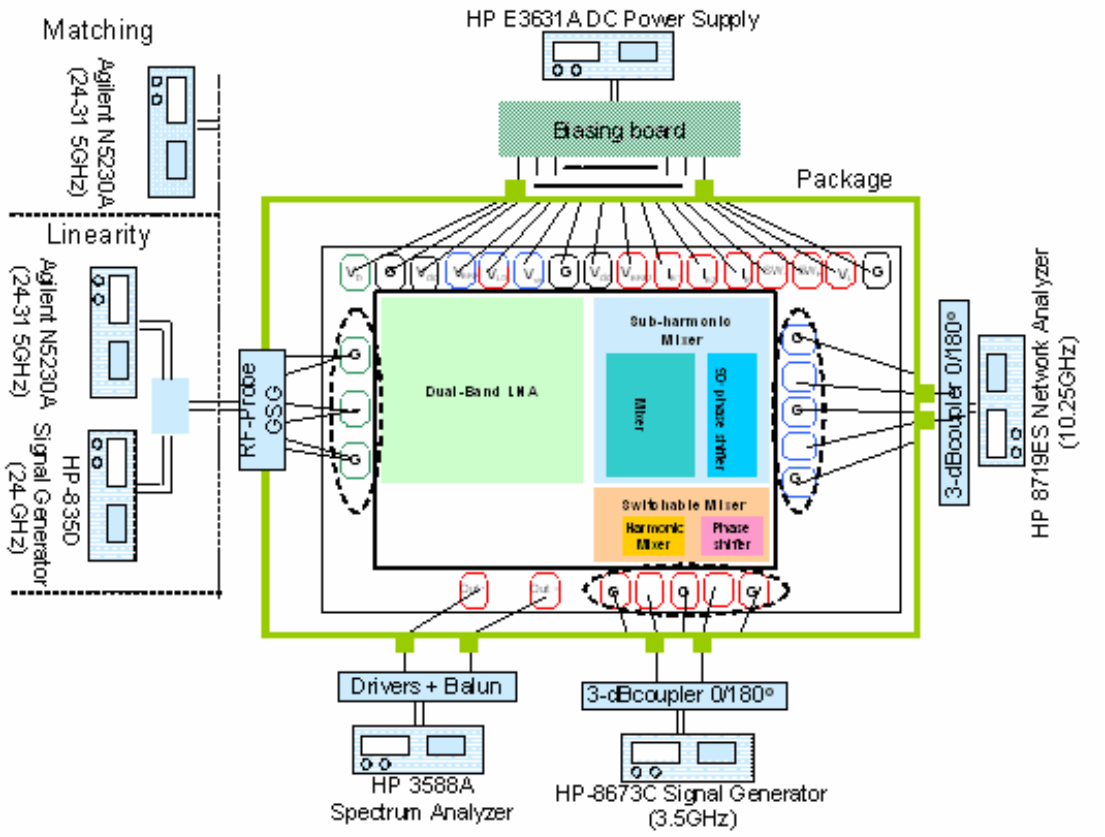


Fig. 5.18 Test setup of the switchable harmonic receiver.

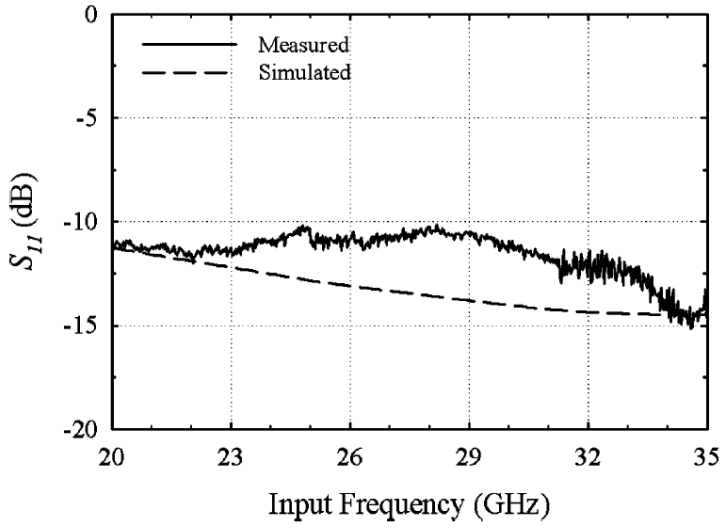


Fig. 5.19 Measured and simulated S_{11} for the dual-band receiver.

The measured reflection coefficient of the receiver is shown in Fig. 5.19. A reflection coefficient of better than 12dB is obtained for the two frequency bands. The overall measured conversion gain versus the baseband frequency (dc – 15MHz) for 24- and 31-GHz frequency bands is shown in Fig. 5.20. These plots are obtained by measuring the output signal using the HP 3588A spectrum analyzer and substracting the gain of the instrumentation amplifier. An overall conversion gain of 21 and 18dB is measured for the 24- and 31-GHz frequency bands, respectively.

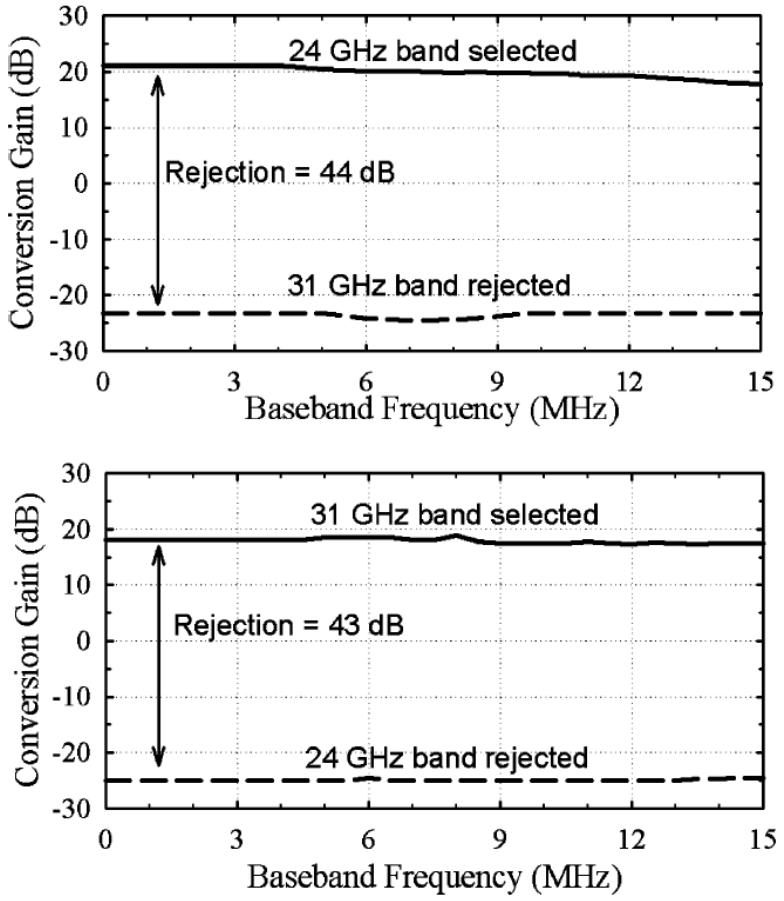


Fig. 5.20 Measured conversion gain and rejection of the proposed switchable harmonic receiver ($V_{Ø,control}$ = 0.25V).

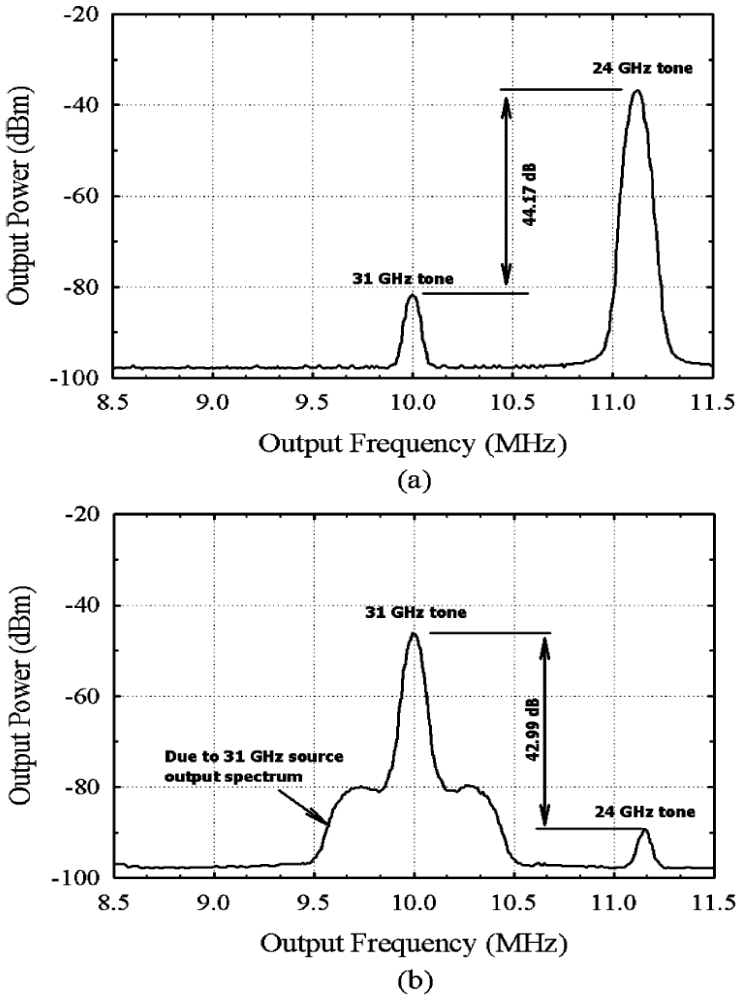


Fig. 5.21 Measured rejection in the baseband when (a) the 24-GHz band or (b) the 31-GHz band is selected.

Fig. 5.21 shows the spectrum of the output signal for various conditions. Fig. 5.21(a) demonstrates the case where the 24-GHz band is selected and the 31-GHz band is rejected, while Fig. 5.21(b) presents the opposite scenario. In this measurement, the 24- and 31-GHz input signals are adjusted to have the same amplitude. Measurements show a rejection of the unwanted signal better than 43dB for two different cases after manual tuning of the phase and amplitude mismatches ($V_{Ø,control}$ =1.26V). The widening in the

downconverted 31-GHz is due to the Agilent N5230A network analyzer that is used to generate the 31-GHz input signal. This network analyzer generates the widened spectrum shown in Fig. 5.21(b) at the input of the receiver and, therefore, the same shape appears at the output. The simulation results show a rejection of better than 60dB. The discrepancy is mainly due to mismatches, inaccurate models, and substrate coupling. Automatic tuning schemes can be applied later for this dual-band receiver to increase the amount of rejection. Fig. 5.22 shows the measured rejection versus the phase control voltage ($V_{Ø,control}$) when the amplitude control (Fig. 5.6) is kept at its default value. As depicted, optimum values of phase control voltage for maximum rejection of 24- and 31-GHz bands are 1.3 and 1.24V, respectively. Optimum values are different for the two bands because the mismatches and process variations have a different impact on the rejection for the fundamental and third-order harmonic components. This optimum value can be obtained by using an automatic tuning scheme.

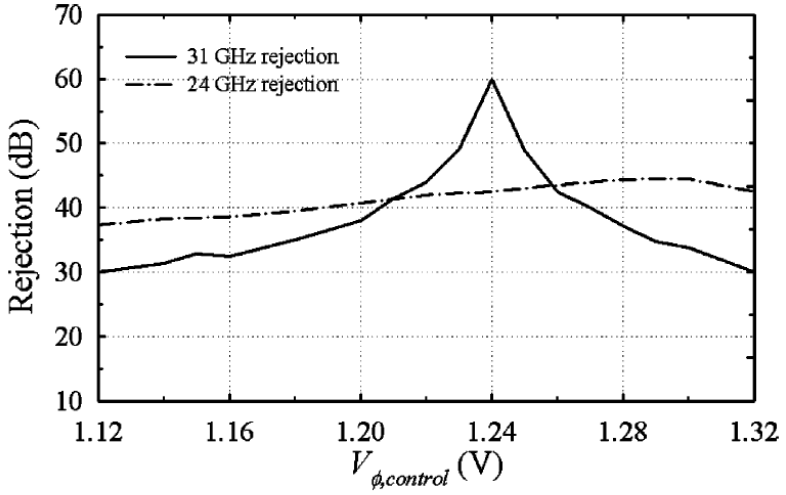


Fig. 5.22 Measured rejection versus phase control voltage $V_{Ø,control}$ when the 24- or 31-GHz band is rejected.

Nonlinearity measurements are performed for the 24- and 31-GHz frequency bands. The dc-40GHz Agilent N5230A network analyzer and 60-GHz Anritsu MG3696 signal generator are used as the input sources. The two input signal tones are applied with a separation of 1.2MHz. The main output signals tones are at 7 and 8.2MHz and the third-order intermediation signal appears at 5.8 and 9.4MHz. For the input signal at 24GHz, the measured output spectrum shows a difference between the main tones (–19-dBm output) and the third-order intermodulation tone of 44dB. This results in an output-referred third-order intercept point (OIP3) of 3dBm equivalent to an input-referred IIP3 of –18dBm. Similar steps are performed for the 31-GHz input signal, and an IIP3 of –17dBm is obtained. The noise figure of the implemented receiver front end is obtained by measuring the output noise level using a spectrum analyzer and, hence, estimating the input-referred noise. A measured noise figure of 8 and 9.5dB is obtained for the 24- and 31-GHz band, respectively. The complete dual-band receiver consumes 60mW from a 1.8V supply. Finally, the measured performance summary of the switchable harmonic receiver and its building blocks is shown in Table 5.3.

5.5 Conclusion

In this chapter, the design and implementation of a switchable harmonic mixer is presented. The mixer is a part of a new mm-wave dual-band receiver in 0.18µm SiGe BiCMOS technology. The main target of minimizing the receiver power consumption and silicon area is achieved while having good performance in terms of gain, noise and linearity as well as band rejection.

Table 5.3 Dual-band switchable harmonic receiver measured performance parameters summary.

Parameter	Simulated	Measured
Technology	0.18μm BiCMOS	
$f_{T,BJT}$/ $f_{T,MOS}$ (GHz/GHz)	70/50	
Total Core Area (mm^2)	0.7	
Supply (V)	1.8	
Total Power (mW)	60	
Conversion Gain (dB)	22.7 @24 GHz 19.2 @31 GHz	21 @24 GHz 18 @31 GHz
Overall NF (dB)	7 @24 GHz 8 @31 GHz	8 @24 GHz 9.5 @31 GHz
IIP3 (dBm)	-14.7 @24 GHz -16 @31 GHz	-18 @ 24 GHz -17 @31 GHz
S_{11} (dB)	<-12	<-12
Rejection of 24 GHz (dB)	>60	43 @ $V_{Ø,control}$= 1.26 V
Rejection of 31 GHz (dB)	>60	44 @ $V_{Ø,control}$= 1.26 V

CHAPTER VI

CONCLUSIONS

6.1 Summary

In this dissertation a number of different high performance circuits and systems are proposed for power management and mm-wave applications. Four power management systems and a core part of a dual band mm-wave receiver are designed, implemented and tested. Complete analyses, design procedures and measurement results for the different circuits and systems are included.

Measurement results for the three LDOs show better performance in terms of PSR and transient response as well as area and quiescent power reduction in comparison to state-of-the-art solutions. The OCL-LDO particularly achieves the best FOM among the recently published similar works. Measurement results for the buck switching converter show a very low quiescent current consumption with fast transient response and low ripples in addition to very small silicon area and tiny external off-chip components. Measurement results for the complete mm-wave receiver show a high band rejection exceeding 40dB with small area and power consumption compared to other existing mm-wave receivers' architectures.

6.2 Possible Areas for Future Work

There is always a great demand on designing highly-efficient low-cost power management systems. One of the possible extensions of this work is to integrate a complete higher level system with both the linear and switching regulators included and

interacted. The challenge is to improve the combined power efficiency while reduce the total cost and size.

Improving the power efficiency of the buck converter working at high switching frequency is also another interesting point to explore. This includes looking into different mechanisms to reduce the switching losses as well as optimizing the design of the PCB for better isolation.

In mm-wave area, the design of a multi-band receiver with some similar idea for band selection will be an interesting topic for future research. The trend will be always to reduce area and power while keeping the high system performance and good rejection between different bands.

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VITA

Ahmed Mohsen Ahmed Amer received the B.S. degree in electronics and communications engineering (magna sum laude), and the M.S. degree in electronic engineering, both from Ain Shams University, Cairo, Egypt, in 2002 and 2006, respectively. In the fall of 2007, he started working towards his Ph.D. degree at the Analog & Mixed Signal Center, Texas A&M University.

From 2002 to 2006, He was a teaching and research assistant in the Electronics and Communications Engineering Department at Ain Shams University. From 2004 to 2006 he was working as an RFIC Design Engineer in SysDSoft Inc., Cairo, Egypt. During the summers of 2008 and 2009, he was an intern in the medical group at Texas Instruments, Dallas, TX. He was a co-recipient of the 2009 Semiconductor Research Corporation (SRC) Design Challenge Award. He also received Fouraker/Ebensberger Fellowship in 2007 and Texas Instruments Excellence Fellowship in 2008 and 2009. His research interests include power management electronics and wideband/multiband RF receivers design.

Mr. Amer may be reached through the Department of Electrical Engineering, Texas A&M University, 3128 TAMU, College Station, TX 77843. His email is ahmed.amer@tamu.edu.