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**20 GHz SOLID STATE TRANSMITTER  
DESIGN, IMPATT DIODE DEVELOPMENT  
AND  
RELIABILITY ASSESSMENT**

**S. PICONE, Y. CHO AND J.R. ASMUS**

**JUNE, 1984**

**FINAL REPORT**

**PREPARED FOR:**

**NATIONAL AERONAUTICS AND SPACE ADMINISTRATION**

**LEWIS RESEARCH CENTER**

**CLEVELAND, OHIO**

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**LNR**  
COMMUNICATIONS

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| 16. Abstract<br>This final report highlights the results of a program encompassing the study, and design of the solid state satellite transmitter operating in the 19.7 to 20.2 frequency band, and the development of key devices and components used therein. The work was performed under contract NAS3-22491 for the NASA Lewis Research Center (LeRC) as part of the 30/20 GHz communications satellite system scheduled for demonstration in the late 1980's.<br>This contract included the development of single drift gallium arsenide (GaAs) Schottky barrier IMPATT diodes and related components, the Assessment of IMPATT Diode Reliability, a proof of concept solid state transmitter design, and a technology assessment study.<br>The transmitter design utilizes technology which, upon implementation, will demonstrate readiness for development of a POC model within the 1982 time frame and will provide an information base for flight hardware capable of deployment in a 1985-90 demonstrational 30/20 GHz satellite communication system.<br>Lifetime extrapolated from the herein described life test data are:<br>Schottky Barrier GaAs Diodes ( $\gamma_M$ ) $3 \times 10^4$ Hours<br>Grown Junction GaAs Diodes ( $\gamma_M$ ) $2 \times 10^6$ Hours<br>Furthermore, the results demonstrate the viability of GaAs IMPATTs as high performance, reliable RF power sources which, based on the recommendation made herein, will surpass device reliability requirements consistent with a ten year spaceborne solid state power amplifier mission. |  |  |                            |   |           |
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## FOREWORD

This final report covers work done under NASA/Lewis Research Center (LeRC) contract NAS3-22491, describing the tasks and efforts performed from June 1981 to September 1983. The program was managed for NASA by Mr. G.J. Chomos, Space Communications Division, LeRC.

Under the direction of Dr. H.C. Okean the LNR team consisted of J. deGruyl, E. Ng, Y. Cho, S. Picone, E. Bulan, G. Brecht and J.R. Asmus, all of LNR/Government Systems Division. The program was managed during the latter phases for LNR by J.R. Asmus.

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Extended failure and statistical analysis described in this report was performed by LNR during a four months period following program conclusion.

## ABSTRACT

This final report highlights the results of a program encompassing the study, and design of the solid state satellite transmitter operating in the 19.7 to 20.2 frequency band, and the development of key devices and components used therein. The work was performed under contract NAS3-22491 for the NASA Lewis Research Center (LeRC) as part of the 30/20 GHz communications satellite system scheduled for demonstration in the late 1980's.

This contract included the development of single drift gallium arsenide (GaAs) Schottky barrier IMPATT diodes and related components, the Assessment of IMPATT Diode Reliability, a proof of concept solid state transmitter design, and a technology assessment study.

The objectives of the 20 GHz solid state transmitter program were to foster the development of 20 GHz solid state power amplifier (SSPA) technology by:

- development and demonstration of key 20 GHz SSPA breadboard circuits;
- design of a proof of concept SSPA model;
- development of 20 GHz GaAs IMPATT material and devices;
- evaluation of the reliability of single drift GaAs IMPATT diodes;
- provision of data consistent with the definition and design of 20 GHz spaceborne communications transmitter requirements.

The transmitter design utilizes technology which, upon implementation, will demonstrate readiness for development of a POC model and will provide an information base for flight hardware capable of deployment in a 1985-90 demonstrational 30/20 GHz satellite communication system.

In order to satisfy the performance objectives on the overall 20 GHz IMPATT transmitter, the achieved design goals on the 20 GHz IMPATT diodes to be deployed therein are as follows:

- RF power output: 1.5 to 2.0W CW
- Frequency: 19.5 to 20.5 GHz
- DC-RF conversion efficiency: 16 -22 percent

The results of the initial reliability assessment defined major failure mechanisms, diode modifications, future reliability efforts, screening procedures and operating lifetimes of unscreened 20 GHz GaAs IMPATT exceeding those previously projected.

Lifetime extrapolated from the herein described life test data are:

|   |                         |
|---|-------------------------|
| Schottky Barrier GaAs Diodes ( $\gamma_M$ ) | $> 3 \times 10^4$ Hours |
| Grown Junction GaAs Diodes ( $\gamma_M$ )   | $> 2 \times 10^6$ Hours |

Furthermore, the results demonstrate the viability of GaAs IMPATTs as high performance, reliable RF power sources which, based on the recommendation made herein, will surpass device reliability requirements consistent with a ten year spaceborne solid state power amplifier mission.

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A. EXECUTIVE SUMMARY

FINAL REPORT

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## A. EXECUTIVE SUMMARY

### 1.0 Introduction

This executive summary highlights the results of a program encompassing the study and design of a solid state satellite transmitter operating in the 19.7 to 20.2 GHz frequency band, and the development of key devices and components used therein. The work was performed under contract NAS3-22491 for the NASA Lewis Research Center (NLeRC) as part of the 30/20 GHz communications satellite system scheduled for launch in the late 1980's. Period of performance was from June 1981 to Sept. 1983.

The program included the development of single drift gallium arsenide (GaAs) Schottky Barrier IMPATT diodes and related components, the assessment of IMPATT diode reliability, a Proof of concept (POC) solid state transmitter design, and a technology assessment study.

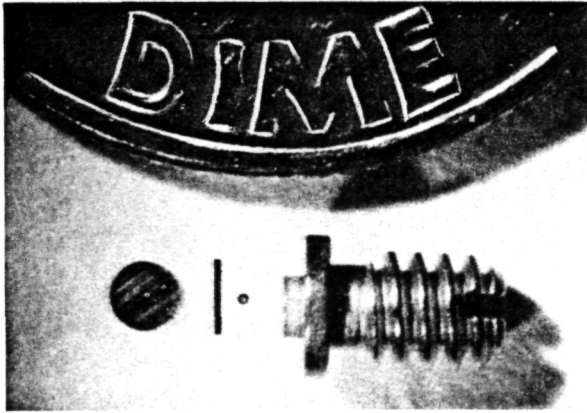
The program objectives are embodied in the following major tasks:

- 20 GHz solid state (IMPATT) transmitter preliminary design
- device/assembly development
- reliability assessment
- POC model design, test plan, and procedures
- technology assessment

Figure 1 summarizes the 20 GHz single drift GaAs IMPATT technology, including a 20 GHz solid state power amplifier (developed under a related AFSD/AFWAL Contract F33315-BOC-1182) and the level of performance achieved therein.

# 20 GHZ SINGLE DRIFT GAAS IMPATT TECHNOLOGY

## IMPATT CHIP/DIODE DEVELOPMENT



(2)

\*AFSD/NASA LeRC Contract NAS3-22493

## 20 GHZ SOLID STATE POWER AMPLIFIER

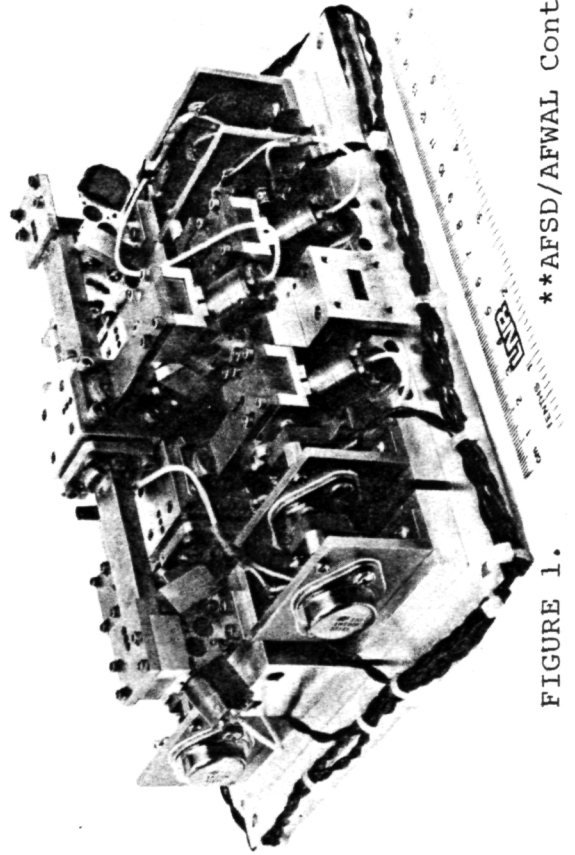
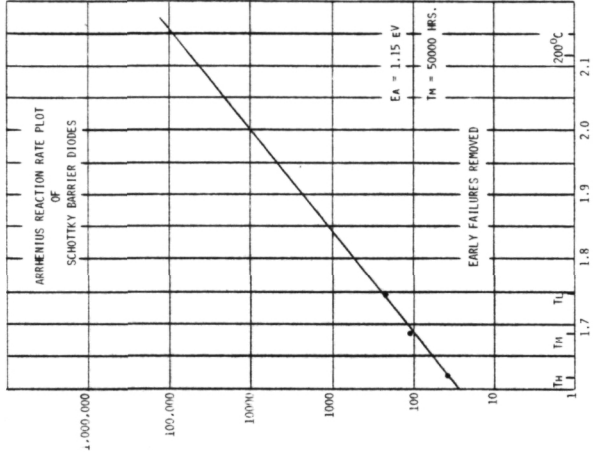
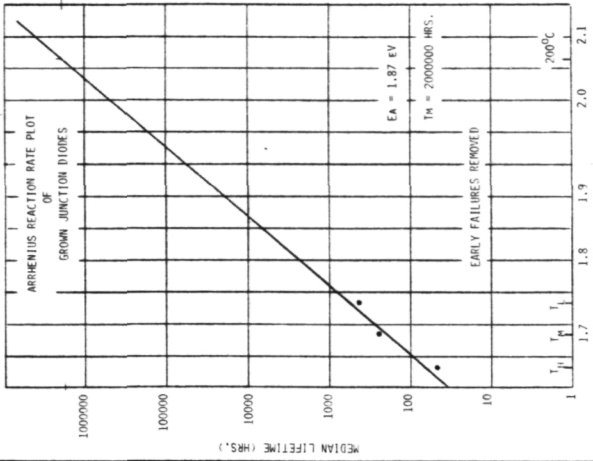


FIGURE 1.

## SCHOTTKY BARRIER DIODES

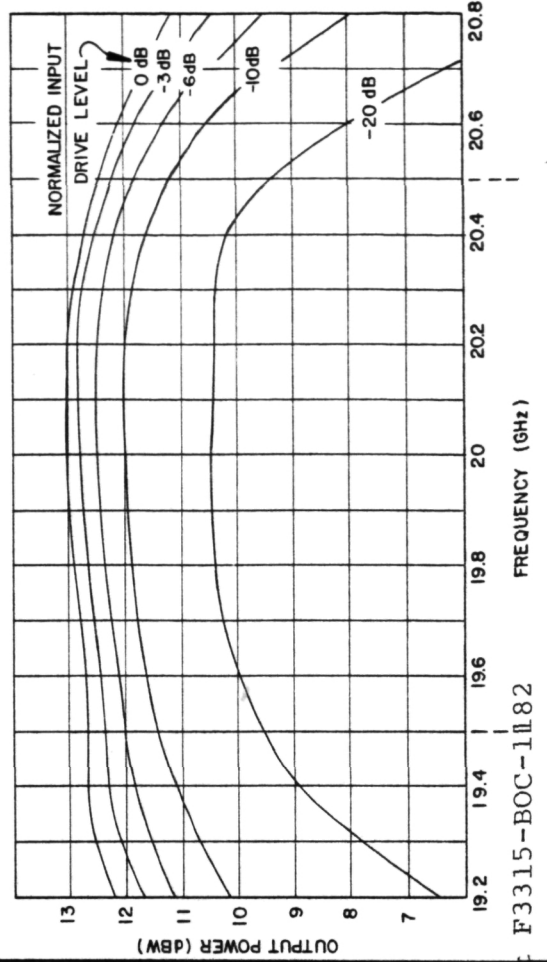


## GROWN JUNCTION DIODES



22493

## SSPA PERFORMANCE AT DIFFERENT INPUT DRIVE LEVELS \*\*



\*\*AFSD/AFWAL Contract F3315-BOC-1182

## 2.0 Program Objectives

The objectives of the 20 GHz solid state transmitter program were to foster the development of 20 GHz solid state power amplifier (SSPA) technology by:

- development and demonstration of key 20 GHz SSPA breadboard circuits
- design of a proof of concept SSPA model;
- development of 20 GHz IMPATT material and devices;
- evaluation of the reliability of single drift GaAs IMPATT diodes
- provision of data consistent with the definition and design of 20 GHz spaceborne communications transmitter requirements.

These objectives were encompassed by the program tasks, as summarized in the following paragraphs.

### 2.1 20 GHz IMPATT Transmitter for Communications Satellite

The preliminary 20 GHz IMPATT transmitter design presented in this report and characterized by the functional block diagram of Figure 2, addresses each of the general requirements enumerated in Table 1. The transmitter design utilizes technology which, upon implementation, will demonstrate readiness for development of a POC model and will provide an information base for flight hardware capable of deployment in a 1985-90 demonstrational 30/20 GHz satellite communication system.

The transmitter design utilizes those devices necessary to amplify an angle modulated, single carrier downlink signal in the band 19.7 to 20.2 GHz, to an RF output power level of 20 watts and meet all RF performance requirements specified. In so doing, size, weight and power drain requirements have been reduced to a minimum consistent with spacecraft demands.

Overall design complexity and number of parts have also been minimized, as have device junction temperature, to insure maximum transmitter reliability consistent with a 10 year oper-

TABLE I

PROJECTED CHARACTERISTICS OF  
20 GHz IMPATT TRANSMITTER DESIGN

|  |   |
|--|---|
| CENTER FREQUENCY                           | 19.95 GHz   |
| -1 dB BANDWIDTH (MIN.)                     | 500 MHz (19.7-20.2 GHz)   |
| RF POWER OUTPUT (MIN.)                     | 22W   |
| OPERATING GAIN (NOM.)                      | 34.5 dB   |
| RF/DC POWER-ADDED EFFICIENCY (MIN.)        | 20.9 PERCENT (EXCLUDING DC POWER/MONITOR CONDITIONER)                   |
| AM/PM CONVERSION (MAX.)                    | 3 deg/dB  |
| INPUT/OUTPUT VSWR (MAX.)                   | 1.25:1  |
| GAIN VARIATION VS. FREQUENCY @ FIXED DRIVE | 1.0 dB p-p  |
| PHASE LINEARITY (MAX.)                     | 10 deg p-p  |
| GAIN SLOPE (MAX.)                          | 0.1 dB/MHz  |
| PASSBAND GROUP DELAY VARIATION (MAX.)      | 0.5 nS/50 MHz   |
| SPURIOUS OUTPUTS (MAX.)                    |   |
| • HARMONIC COMPONENTS                      | -50 dBc   |
| • NON HARMONIC COMPONENTS                  | -60 dBc   |
| NOISE FIGURE (MAX.)                        | 24 dB   |
| DC PRIME INPUT POWER (MAX.)                | 105.3W EXCLUDING DC POWER/MONITOR/COMAND CONDITIONER 115W OVERALL       |
| WEIGHT                                     | 4.8 lbs.  |
| DIMENSIONS                                 | 6.75"x5.75"x2.5"  |
| BASEPLATE TEMPERATURE RANGE                | 0-75°C  |
| MAXIMUM DEVICE JUNCTION TEMPERATURE:       | 235°C (IMPATT)<br>112°C (FET)   |
| RF INPUT/OUTPUT INTERFACES (J1/J2)         | WR-42 W/G-UG595/UG 595/U COVER FLANGE +28 VDC, +15 VDC, -5 VDC, +15 VDC |
| DC INPUT POWER INTERFACE                   | -ITT CANNON DEMA TYPE CONNECTOR   |
| TELEMETRY MONITOR OUTPUT INTERFACE         | ITT CANNON DEMA TYPE CONNECTOR  |

ational life. Graceful degradation in performance under random device failure rather than complete loss of output power is an integral part of the design to further enhance transmitter reliability.

The critical areas of technology applicable to the subject 20 GHz transmitter fall into two general categories, functional circuits, and constituent devices and materials. In terms of the previously depicted (Figure 2) functional RF block diagram of a composite 20 GHz FET/IMPATT transmitter, the key circuit technologies which must be developed at 20 GHz, include IMPATT power amplifiers, FET driver amplifiers, RF power dividers/combiners and ferrite circulators. The foregoing technology development in turn depends upon the concurrent evaluation of such critical 20 GHz device and material technologies as Read-profile GaAs epitaxial wafer material, GaAs Read-IMPATT diodes and GaAs FET devices.

None of the above requires any new fundamental breakthroughs but rather represents extension of the existing state of the art in these technologies at lower frequencies to the more severe constraints associated with operation at 20 GHz.

The basic, design requirement on the subject 20 GHz transmitter is that it provides 20W (minimum) K-band RF power output over a 500 MHz bandwidth centered near 20 GHz with 20 percent DC bias/RF power added efficiency. (the latter excluding the efficiency degradation due to DC power conditioning components). Moreover, this transmitter must provide 30 dB power gain to a single, angle modulated (PM) carrier, concurrent with 25 dB maximum noise figure, and a high degree of amplitude and delay flatness ( $\pm 1$  dB and  $\pm 5$  deg. overall passband deviation from gain flatness and phase linearity and 0.15 dB/MHz and 0.5nS/50 MHz maximum gain and delay slope). For the specified single PM carrier, the transmitter output amplitude can be into saturation

provided that the requirements on such linearity-related performance parameters as AM/PM conversion ( $5 \pm 1$  deg/dB max) and harmonic/nonharmonically related spurious content ( $\sim 50/60$  dBc max) are satisfied. Finally, to accommodate representative spacecraft thermal profiles, specified performance must be achieved over a  $0-75^{\circ}\text{C}$  baseplate temperature range.

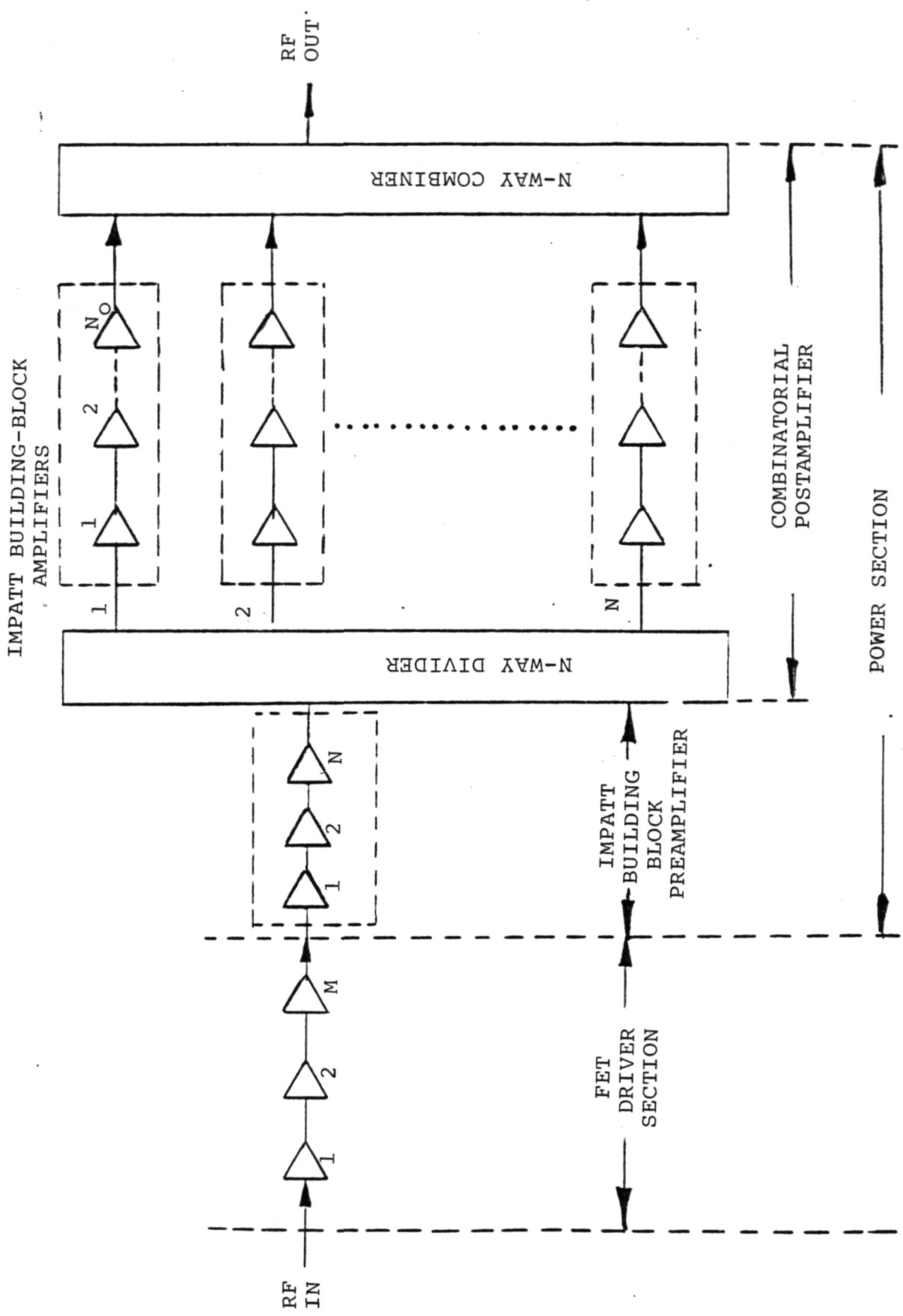
The 20 GHz IMPATT transmitter RF assembly, in its most general form, (Figure 2) consists of the cascaded combination of a FET driver section and an IMPATT power section. The FET driver section, in turn, comprises a cascade of low to medium power FET amplifier stages whereas the IMPATT power section consists of a multistage IMPATT preamplifier driving a combinatorial IMPATT postamplifier. The latter is configured as an array of identical multistage IMPATT "building blocks", paralleled between identical N-way power divider and combiner. In the most general case, the number of IMPATT amplifier stages comprising the preamplifier ( $N_i$ ) and postamplifier "building block" ( $N_o$ ) are different. The order (N) of power combination required is determined by the RF power capability of each "building block" which in turn determines how many paralleled "building blocks" are required to provide the required RF power output (20W).

In order to satisfy the performance objectives on the overall 20 GHz IMPATT transmitter, the corresponding design goals on the 20 GHz IMPATT diodes to be deployable therein are as follows:

- RF power output: 1.5 to 2.0W CW (min)
- Frequency: 20 GHz (nom.)
- DC-RF conversion efficiency: 20-25 percent (min)

Based upon the above, a dual-diode building block, 4 way combinatorial IMPATT postamplifier topology is chosen, as described in Section B.

FUNCTIONAL RF TOPOLOGY OF 20 GHz  
IMPATT TRANSMITTER



(7)

FIGURE 2.

## 2.2 Development of Device/Assembly Technology

The foregoing design objectives, referenced to measured IMPATT diode performance in a 20 GHz waveguide test oscillator, are consistent with the requirements dictated by the previously depicted preferred 20 GHz transmitter configuration. The high DC-RF conversion efficiency requirement necessitates the use of GaAs as the diode semiconductor material, as opposed to the less efficient albeit more mature Si technology.

A vital part of the overall GaAs IMPATT diode development effort was the selection, evaluation and collaboration with one or more outside suppliers of state-of-the-art epitaxial GaAs material, grown to LNR specification.

The achieved level of 20 GHz IMPATT diode performance, as measured in a K-band waveguide test oscillator, described in Section C is,:

- Frequency range 18-21 GHz
- RF power output: 1.3 to 2.7W
- DC-RF Conversion efficiency: 12 to 22 percent

In addition, a direct correlation was established between amplifier and oscillator performance measurements, wherein IMPATT diodes which exhibited  $\sim 2$ W RF power output and 18 percent conversion efficiency at 20 GHz in the test oscillator, demonstrated  $\sim 2.5$ W RF power output, 4 dB gain and 14 percent DC-RF power added efficiency over a 1 GHz bandwidth in a single stage 20 GHz test amplifier.

Other breadboard assemblies developed under this program task include 20 GHz circulators, FET driver amplifier stages and four way power divider/combiner, also described in Section C.



### 2.3 20 GHz Single Drift GaAs IMPATT Diode Reliability Assessment

A major limitation to the general acceptance of 20 GHz GaAs IMPATTs for system and spaceborne use is the question of reliability. The demonstrated performance of these devices was not in question.

Therefore, a major goal of the program was to establish the reliability of GaAs IMPATT diodes and dispel misconceptions of poor reliability identified with GaAs microwave devices operating at elevated temperatures.

The reliability assessment of Schottky barrier and grown junction IMPATT diodes consisted of several different engineering subtasks, including the fabrication and procurement of 20 GHz GaAs IMPATT diodes, design and implementation of accelerated stress test equipment, conducting actual accelerated stress testing, and performance of failure and statistical analysis.

The results of this initial reliability assessment summarized in the attached Task IIB report defined major failure mechanisms, diode modifications, future reliability efforts, screening procedures and operating lifetimes of unscreened 20 GHz GaAs IMPATT exceeding those previously projected.

Preliminary diode lifetimes, extrapolated from the measured life test data, are:

|   |                            |
|---|----------------------------|
| Schottky Barrier GaAs Diodes ( $\gamma_M$ ) | $\sim 3 \times 10^4$ Hours |
| Grown Junction GaAs Diodes ( $\gamma_M$ )   | $> 2 \times 10^6$ Hours    |

Furthermore, the results (Section D) demonstrate the viability of GaAs IMPATTs as high performance, reliable RF power sources, which, based on the recommendation made herein, will surpass device reliability requirements consistent with a ten year spaceborne solid state power amplifier mission.

## 2.4 POC Model Design

The paper design of a 20 GHz IMPATT Transmitter proof of concept described in Section E addresses major design considerations such as:

- Functional Design and Projected Performance, of minimum RF power output of 22W and a nominal operating gain of 34.5 dB at a RF/DC power added efficiency of 20.9 percent consistent with a center frequency of 19.95 GHz.
- Thermal and Mechanical Design
- Electrical Design
- Specification of key devices components and sub-assemblies.
- Detailed POC Test Plan/Procedures.

The design approach was selected to provide the best potential to achieve performance goals, minimize components, circuit and packaging complexity. Furthermore, the successful implementation of the preferred POC design is based on the following key features:

- use of LNR 2W, 20 GHz GaAs SDR Read-IMPATT diodes, which have demonstrated required capability for RF amplifier deployment;
- use of readily available modest power level GaAs MESFET chips in two-stage FET driver wherein FET's are mounted on customized pretuned LNR carriers which are in turn embedded in the microstrip circuit comprising the two stage single-ended amplifier;
- passive combination of mutually isolated, modular two stage IMPATT amplifier "building blocks" for simple manufacturability, and enhanced reliability;
- graceful degradation in RF output power under random device failure and "power down" capability, both by "turning off" individual "building blocks";

- IMPATT amplifiers, used in high gain-bandwidth product stable amplification configuration, provide wide dynamic range and small signal to full drive capability without stability problems or undesired output spuri in absence of input signal;
- compact low loss miniature multi-port high isolation stripline wye junction circulators with individual junctions serving as amplifier coupling circulators, and with appropriate resistive internal terminations, as input and interstage isolators;
- simple miniature non-critical easily aligned highly reliable and mechanically rugged TEM-line IMPATT amplifier mount design directly integrated with coupling port of circulator and incorporating optimum tradeoff between RF power output, DC/RF power added efficiently, gain-bandwidth and output flatness.

The performance specifications and budgets and physical parameters characterizing the POC model SSPA are presented in detail in Section E.

## 2.5 Technology Assessment

The purpose of this study was to define and evaluate the technology required for space qualifiable 20 GHz IMPATT transmitters. Based on the assessment of the currently available technology, projections of the technology becoming available by 1985 through 1987 were included in the study.

For the realization of the projected 1985 - 1987 performance objectives two key methodologies have been identified with the performance growth projections:

- IMPATT device technology
- power combiner technology.

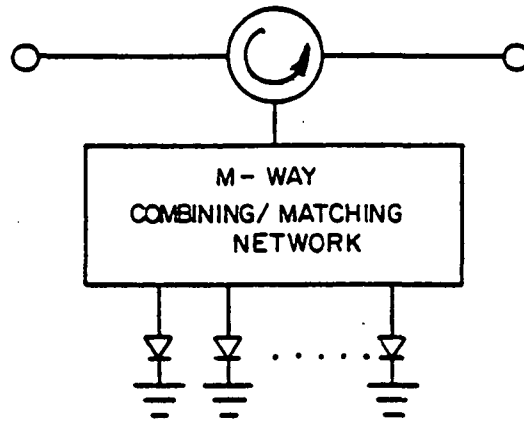
The available alternative device considerations are either single drift or double drift GaAs IMPATT diodes whereas the general forms of combinatorial configurations under consideration were active and passive intrastate divider/combiner power sections (Figure 3),

The selected approach characterized in Table 2, was based upon use of:

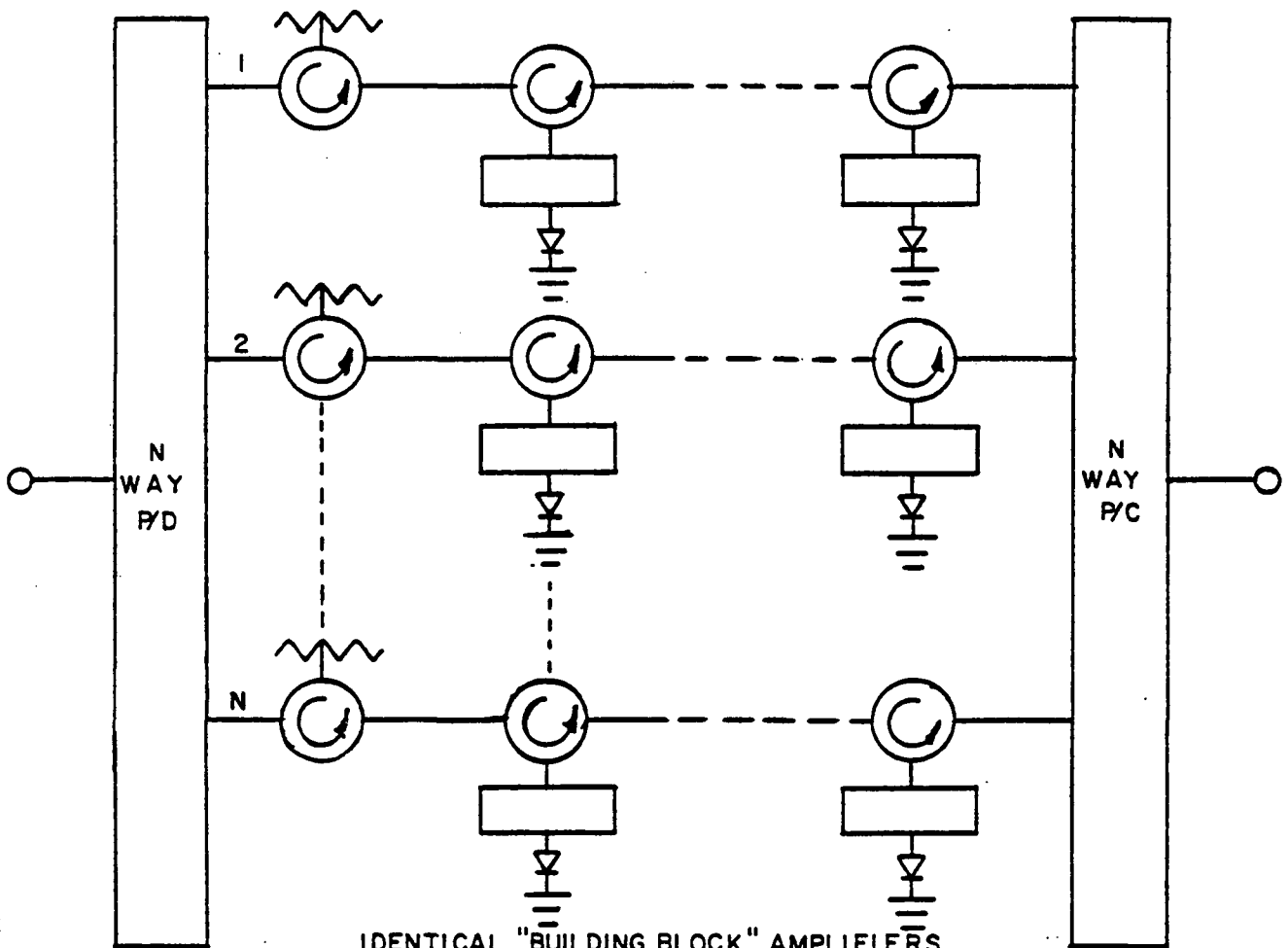
- double drift 6W IMPATT diodes
- waveguide reactive junction in the passive combinatorial configuration.

A development plan was prepared and submitted for the 1987 advanced technology IMPATT transmitter design implementation.

# IMPATT AMPLIFIER COMBINATORIAL CONFIGURATIONS



A — ACTIVE (INTRA-STAGE) COMBINING



IDENTICAL "BUILDING BLOCK" AMPLIFIERS  
B — PASSIVE (INTERSTAGE) COMBINING

FIGURE 3.

TABLE II.

ADVANCED 20 GHz IMPATT TRANSMITTER  
DESIGN USING 1987 TECHNOLOGY



| FREQUENCY RANGE                            | 17.7-20.2 GHz (Typ)  | FREQUENCY RANGES                           | 17.7-20.2 GHz (Typ)   |
|--|--|--|---|
| -1 dB BANDWIDTH (MIN)                      | 2.5 GHz  | -1 dB BANDWIDTH (MIN)                      | 2.5 GHz   |
| RF POWER OUTPUT (MIN)                      | 20W  | RF POWER OUTPUT (MIN)                      | 40W   |
| OPERATING GAIN (NOM)                       | 40 dB  | OPERATING GAIN (NOM)                       | 40 dB   |
| RF/DC POWER-ADDED EFFICIENCY (MIN)         | 22 PERCENT (EXCLUDING DC POWER MONITOR CONDITIONER)          | RF/DC POWER-ADDED EFFICIENCY (MIN)         | 21 PERCENT (EXCLUDING DC POWER MONITOR CONDITIONER)           |
| AM/PM CONVERSION (MAX)                     | 5.0 deg/dB   | AM/PM CONVERSION (MAX)                     | 6.0 deg/dB  |
| INPUT/OUTPUT VSWR (MAX)                    | 1.25:1   | INPUT/OUTPUT VSWR (MAX)                    | 1.25:1  |
| GAIN VARIATION VS. FREQUENCY @ FIXED DRIVE | 1.0 dB p-p   | GAIN VARIATION VS. FREQUENCY @ FIXED DRIVE | 1.0 dB p-p  |
| NOISE FIGURE (MAX)                         | 15 dB  | NOISE FIGURE (MAX)                         | 17 dB   |
| DC PRIME INPUT POWER-(MAX)                 | 90W - EXCLUDING DC POWER/MONITOR CONDITIONER<br>100W OVERALL | DC PRIME INPUT POWER-(MAX)                 | 190W - EXCLUDING DC POWER/MONITOR CONDITIONER<br>200W OVERALL |

AREAS OF IMPROVEMENT IN ADVANCED 20 GHz IMPATT TRANSMITTER DESIGNS

| PARAMETER                    | DEGREE OF IMPROVEMENT |                  | REASON FOR IMPROVEMENT   |
|------------------------------|-----------------------|------------------|--|
|                              | Advanced Design       | Current Baseline |  |
| RF Output Power              | 40 W                  | 20 W             | Higher power IMPATT diodes, utilizing multiple or distributed mesas and/or dual chips/package.   |
| RF/DC Power Added Efficiency | 22 percent            | 15 percent       | Higher IMPATT diode efficiency due to <ul style="list-style-type: none"> <li>• reduction in R<sub>g</sub></li> <li>• further optimization of Read profile</li> </ul> |
| Noise Figure                 | 15 dB                 | 25 dB            | Higher gain, lower noise FET preamplifier preceding IMPATT power section.  |
| Bandwidth                    | 2.5 GHz               | 1 GHz            | Lower parasitic IMPATT package and lower diode R <sub>g</sub> coupled with more extensive use of broad-banding techniques.   |

## 2.6 Summary

The 20 GHz IMPATT transmitter feasibility and design study has resulted in the development of single drift GaAs Schottky barrier IMPATT diodes and a first order reliability assessment and device modifications consistent with the paper design of a 20 GHz IMPATT Transmitter proof of concept, based on currently available (1982 - Figure 4.) and advanced (1987) technology.

The study further demonstrated, that no technological breakthroughs are required for the realization of an advanced 20 GHz IMPATT transmitter technology. Moreover, advanced performance has been defined mainly as a function of the IMPATT device and power combining topologies, rather than new and inovative technologies.

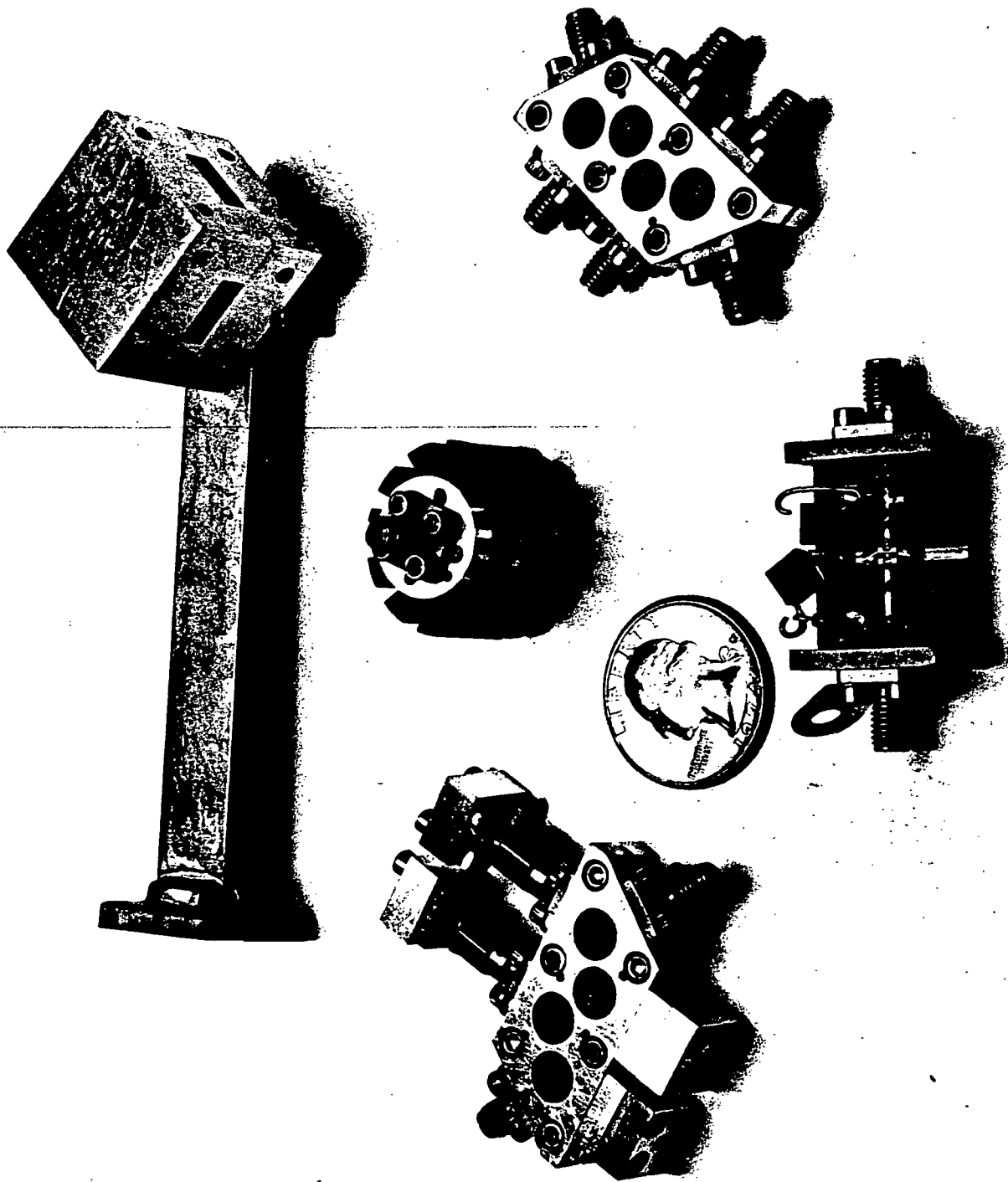


FIGURE 4. BREADBOARD 20 GHz CIRCUITS DEVELOPED FOR IMPATT TRANSMITTER DESIGN VALIDATION



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## FOREWORD

This final report covers work done under NASA/Lewis Research Center (LeRC) contract NAS3-22491, describing the tasks and efforts performed from June 1981 to September 1983. The program was managed for NASA by Mr. G.J. Chomos, Space Communications Division, LeRC, and for LNR by Mr. J.R. Asmus.

The authors gratefully acknowledge the insight and understanding provided by M.F. Millea, The Aerospace Corporation, towards the successful completion of the failure data assessment and statistical analysis. The interest and support of E.J. Calucci and E. Doyle, Jr. of the Rome Air Development Center is greatly appreciated. Pulsed RF measurements and data provided by V. Higgins and A. Paoletta of ERADCOM, Fort Monmouth, are gratefully acknowledged. The assistance received from P. Lyons and D. Sterner, Standard Microsystems, Inc., during SEM analysis is very much appreciated.

Extended failure and statistical analysis described in this report was performed by LNR during a four months period following program conclusion.



## ABSTRACT

This final report describes the work done under NASA/LeRC contract NAS3-22491, "20 GHz Single Drift GaAs IMPATT Diode Reliability Assessment". Covering a period of performance from June 1981 to September 1983.

The reliability assessment of Schottky barrier and Grown junction IMPATT diodes consisted of several different engineering tasks, including the fabrication and procurement of 20 GHz GaAs IMPATT diodes, design and implementation of accelerated stress test equipment, conducting actual accelerated stress testing, perform failure and statistical analysis.

The results of this initial reliability assessment defined major failure mechanisms, diode modifications, future reliability efforts, screening procedures and operating lifetimes of unscreened 20 GHz GaAs IMPATT exceeding those previously projected.

Lifetimes extrapolated from the herein described life test data are:

Schottky Barrier GaAs Diodes ( $\gamma_M$ )  $> 3 \times 10^4$  Hours

Grown Junction GaAs Diodes ( $\gamma_M$ )  $> 2 \times 10^6$  Hours

Furthermore, the results demonstrate the viability of GaAs IMPATTs as high performance, reliable RF power sources, which, based on the recommendation made herein, will surpass device reliability requirements consistent with a ten year spaceborne solid state power amplifier mission.

## I. INTRODUCTION

### 1.0 Summary

Solid state power amplifiers (SSPA) represent an attractive cost effective and reliable replacement for traveling-wave tubes for applications in the 30/20 GHz communications satellite technology. The 20 GHz down link SSPA may be used in applications that require up to 20 Watts of RF Power. Two solid state designs are currently under development, the field effect transistor (FET) and the impact avalanche transit time diode (IMPATT).

GaAs IMPATT diodes are well known for achieving high output powers and efficiencies. FET devices need more development to achieve the equivalent power and efficiency. Thus, the IMPATT diode appears to be the more qualified RF power generator for the next generation of EHF satellites.

A major limitation to the general acceptance of 20 GHz GaAs IMPATTs for system and spaceborne use is the question of reliability. The demonstrated performance of these devices is indeed most impressive.<sup>(1)</sup> It also appears that extensive reliability data on power FETs operating at lower frequencies (8 GHz) is used to predict a short operating lifetime for IMPATT diodes that operate at a junction temperature between 200°C and 250°C. This is a misconception since a 200°C temperature range is acceptable for IMPATT operation and not for FET due to the drastic differences in device construction. There are two major reasons for IMPATT diode reliability predictions of median failure times of  $10^7$  hours at an operating junction temperature of 240°C:

- simple device geometry and structure;
- simple device processing technology allowing greater flexibility in selecting contact metal structures including a non-ohmic substrate contact<sup>(2)</sup>.

The accelerated life testing, conducted over a period covering December 1981 through September 1983, had the following basic objectives:

- establish early and wear out failure regions;
- project preliminary operating lifetime of single drift GaAs IMPATT diodes;
- define process and assembly modifications and optimizations;

- establish screening tests to enhance the reliability of devices to be tested;
- ultimate device reliability to be consistent with a ten year spaceborne Solid State Power Amplifier (SSPA) mission.

The Phase I reliability assessment program described in this final report was directed towards the development of first order reliability information and definition of recommendations for Phase II reliability study ultimately leading to the fabrication of high-reliability IMPATT diodes. IMPATT diodes are subjected during operation to higher stresses by electric field, current density and junction temperature than other microwave and millimeter wave solid state devices with proven high reliability. The purpose of this reliability study is to define operating reliability characteristics of high frequency CW IMPATT diodes consistent with an ultimate reliability requirement of a ten year spaceborne mission. Diodes studied under the program included single drift low-high-low (L-H-L) profiled gallium arsenide (GaAs) Schottky barrier junction diodes fabricated at LNR and commercially purchased (VARIAN) devices fabricated from single drift high-low (H-L) profiled GaAs with an epitaxially grown p-layer. The low-high-low structured epitaxial GaAs was grown in a vapor phase (VPE) system, whereby molecular beam epitaxy (MBE) was used to grow the p-high-low profiled structure, thus affording a comparison of epitaxial growth systems. During the development phase, LNR fabricated Schottky barrier IMPATT diodes from both the VPE and MBE grown GaAs. The selection of the VPE grown material for this program was based on the preferred profile and not the specific technology. The devices were not subjected to a pre stress test screening in order to establish an early failure region to help design a cost-effective screening method and operational burn-in.

Considerations for cost and time schedules regarding accelerated high temperature stressing were deciding factors in selecting the constant DC stress test configuration at three predetermined high stress temperatures (three data points is the minimum data required for the construction of an Arrhenius reaction rate plot). The required correlation between RF and DC stressing as well as the RF performance degradation due to stressing was investigated and defined during the

course of the program. All devices were checked for hermeticity, and X-Rayed to determine the condition of the sealed device cavity, e.g. shape and position of ribbon and chip contact. Furthermore, the devices underwent complete DC and RF characterization, including thermal resistance measurements prior to thermal stressing.

In all, the following diodes were fabricated and in the case of the Varian diodes, procured, characterized and stress tested during the reliability assessment:

- A. Schottky Barrier (M/S) Diodes fabricated from single drift L-H-L epitaxial GaAs grown by VPE.
- |                |          |              |
|----------------|----------|--------------|
| Diode Type:    | Standard | Experimental |
| Stress tested: | 105      | 20           |
- B. Grown Junction (P/N) diodes fabricated from single drift H-L epitaxial GaAs grown by MBE.
- |                |          |              |
|----------------|----------|--------------|
| Diode Type:    | Standard | Experimental |
| Stress tested: | N/A      | 19           |
- C. Grown Junction diodes procured from Varian Associates.
- |                |          |              |
|----------------|----------|--------------|
| Diode Type:    | Standard | Experimental |
| Stress tested: | 60       | N/A          |

The reliability assessment of presently available single drift IMPATT diodes has revealed a significant failure mechanism which poses a substantial reliability problem, indicating necessary modifications to current fabrication methods. The information uncovered during the reliability study and reported herein will be of great value to the device manufacturer and end-user, ultimately leading to a high confidence level in IMPATT solid state power amplifier technology.

The statistical analysis of the accelerated stress test data, extrapolated to an operating junction temperature of two-hundred degrees centigrade, projected operating lifetimes of  $3 \times 10^4$  hours and  $2.1 \times 10^6$  hours for the 20 GHz Schottky barrier and grown junction single drift gallium arsenide IMPATT diodes respectively.

Furthermore, with the implementation of process and assembly modifications, in conjunction with newly defined screening procedures and device type recommended herein, the 20 GHz single drift GaAs IMPATT diode will be established as a highly reliable millimeter wave RF power source, more than capable of meeting a ten year space mission requirement.

## 2.0 Reliability Physics - General

The well known "bath tub" concept of three fundamental failure rates corresponds to early failures (high failure rate), the useful life region (low failure rate) and ultimate wear-out failures, is typical for all long-life semiconductor devices. For a given device lot to fall within the low failure rate region early failures need to be eliminated through effective screening and realistic burn-in, without consuming excessive operational lifetime. Therefore, one of the projected outputs of this study is the definition of a device burn-in schedule.

In general the early failure rate is identified on the typical failure rate vs. time distribution for semiconductor devices as decreasing with time and relates to faulty devices having an infant mortality rate. Screening/burn-in procedures which are utilized must raise the infant mortality rate so as to minimize the operating life failure rate by eliminating all defective devices during this early failure period.

A statistical analysis addressing the wearout failure region, where the failure rate begins to increase again is provided in Appendix 'B', The wearout region is normally investigated by accelerated aging via constant stress testing in order to shorten the useful lifetime and make this study possible within a reasonable program schedule. The average time to wearout failure is best described by the Arrhenius reaction rate law:

$$\tau_M = \tau_0 \exp. \left( \frac{E_a}{kT} \right)$$

Where,

- $\tau_M$  = median lifetime hours
- $\tau_0$  = preexponential constant, hours
- $E_a$  = activation energy, eV
- $k$  = Boltzman's constant, and
- $T$  = absolute temperature, °K

GENERALIZED FAILURE RATE VS. TIME  
CHARACTERISTICS

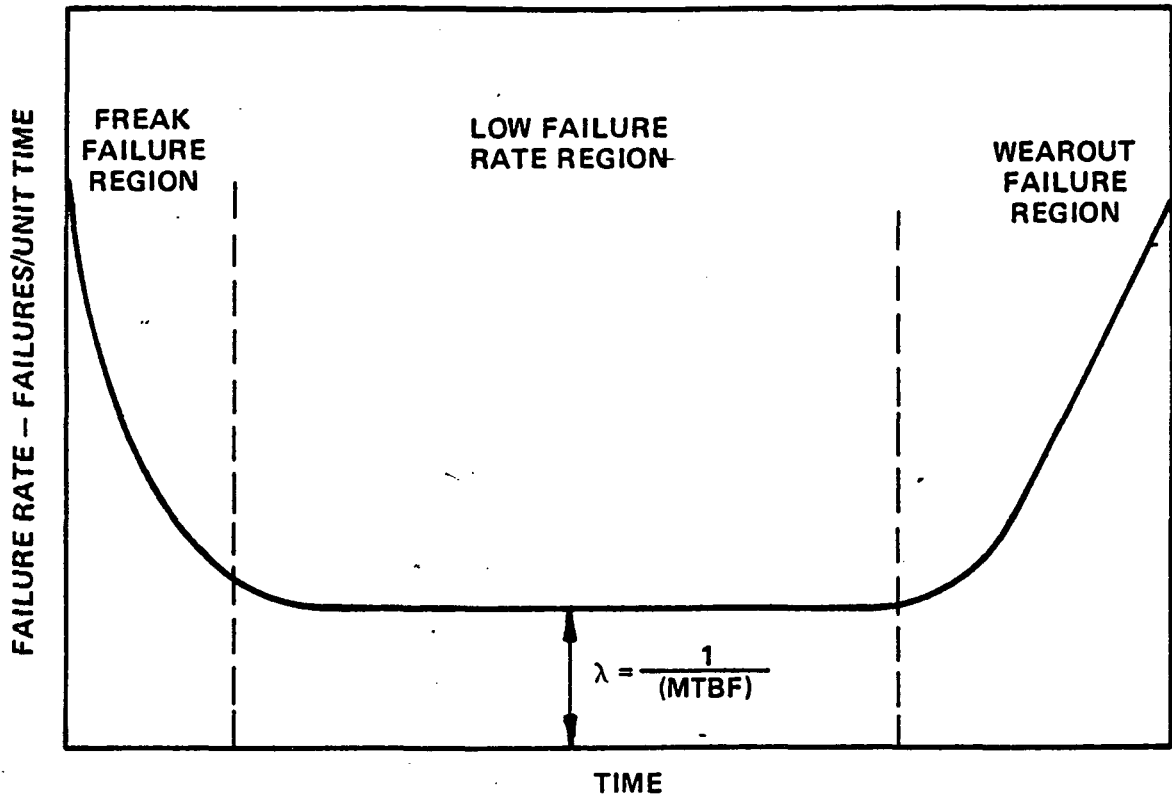


FIGURE 1.

To arrive at an Arrhenius dependence, devices are accelerated-aged at a minimum of three elevated temperatures. At each of these temperatures a normal probability graph, where the abscissa is calibrated in terms of the normal cumulative distribution function, is generated and plotted on a normal probability graph vs. the log of the time-to-failure. Any normally distributed random function will plot as a straight line versus the normal cumulative distribution function with the mean at 50% and the standard deviation,  $\sigma$ , typically between 0.5 to 2.0 for mature fabrication processes represents the slope of the line. One standard deviation will be the variation between the 50% function value and the 16% or 84% values. A normally distributed log function is indicative of a straight line, whereby an S-shaped curve would indicate an infant mortality problem.

Finally, a plot of log time-to-failure versus the reciprocal of temperature should be a straight line establishing the proportionality of log time to inverse temperature required by the Arrhenius equation.

In order to justify the assumption that the failure mechanism follows the Arrhenius reaction rate, the condition of a normally distributed log function with equal standard deviations at each temperature and a linear relationship to the reciprocal temperature must be met by the time-to-failure.<sup>(7)</sup> The resulting straight line will enable the extrapolation of a median operating life time at the projected operating junction temperature.

### 3.0 Failure Mechanism

In the past, various technical reports on IMPATT diode and/or power FET reliability have investigated and identified failure mechanisms in Schottky-barrier junction devices. The reaction of the preferred barrier metal platinum with gallium arsenide is well known by now and so are the effects of acceptor



formation and net donor density reduction in the heavily doped spike region of L-H-L IMPATTs, with optimized layer thicknesses. Keeping the platinum thickness below 200 Å the reaction with the GaAs will stop due to the exhaustion of unreacted platinum before device performance degradation becomes excessive. A layer of titanium (1500 Å to 2000 Å) is added to prevent further GaAs reaction by acting as a gold diffusion barrier, gold being the final metal used for the three metal structure selected for the IMPATT diodes studied in this program. Indeed, the post test profile reconstructions carried out on both the Schottky barrier and grown junction diodes showed practically have no change from the original pre-test profile.

Other potential failure mechanisms are identified with surface breakdown and surface states resulting in conduction and degraded current-voltage characteristics. In addition to crystalline defects and electro-migration of the ohmic or barrier contact will further effect the slow degradation of the device.

Clearly, failure mechanisms contributing to infant mortalities within the early failure region include defects due to material processing and device assembly, e.g. incomplete bonds and excessive bonding pressures.

Grown p-layer devices are much less contact metal dependent as the active n-region is isolated from the anodic metallization by the p-layer. Gradual degradation of these and Schottky barrier devices must therefore be the result of yet another failure mechanism.

In this respect, a major degradation during accelerated DC stress testing was an observed random change of the input current and voltage, resulting in a general trend of a decrease in the DC power dissipation during testing. Subsequent DC measurements of diodes with a change in dissipated DC power of more than one Watt showed however a major increase in the thermal resistance, (which after the appropriate calculations) established a much higher junction stress temperature than scheduled. A corresponding decrease in the oscillator output power was also measured. Relatively unaffected were the current-voltage and ca-

capacitance-voltage characteristics as well as the operating frequency. The above observations together with other temperature related observations made earlier in the program clearly identified a failure mechanism associated with the gold-tin bonding material used for mounting the chips to the diode packages. Various experiments substantiated this very important and unexpected observation. The results achieved with a limited number of experimental diodes with modified metal structures and bonding procedures were exceptionally good. Therefore, together with closely monitored and controlled fabrication procedures a highly reliable and stable IMPATT diode is achievable, suitable for the ultimate usage of the IMPATT SSPA technology for ground and spaceborne missions.

#### 4.0 Failure Criteria

For the purpose of obtaining a maximum post test data base, an IMPATT diode was considered to have failed, if one of the following conditions occurred:

- catastrophic Failure with the diode either electrically open or short;
- stress Test circuit trip points were set 5 volts and 200ma above the voltage and current inputs respectively;
- the actual onset of degradation in any of the monitored DC characteristics resulting in any of the above failure modes within five hours;
- termination of stress testing when none of the above criteria occurred but significant changes in leakage current and input power (DC power dissipated) were observed;

## II. TECHNICAL DISCUSSION - IMPATT DIODE

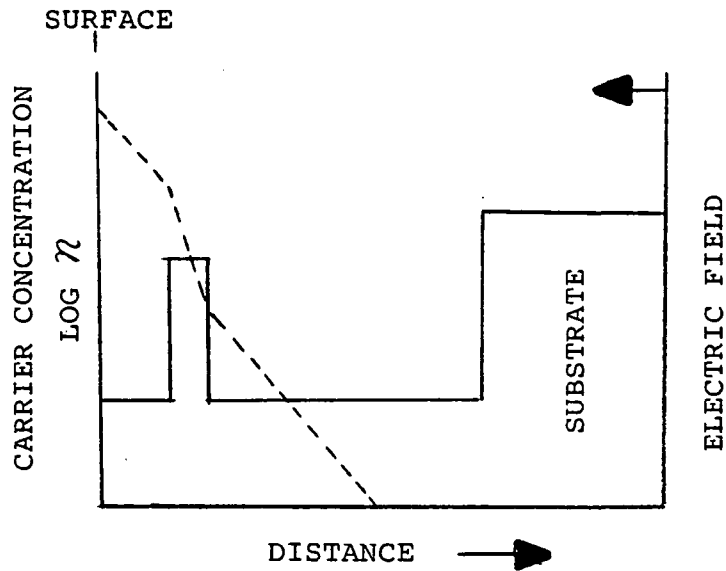
### 1.0 Introduction

The basic properties of the IMPATT diodes used for the reliability are described in this section, including specific GaAs material parameter and doping profiles. Furthermore, device design and structural configuration as well as thermal consideration are discussed.

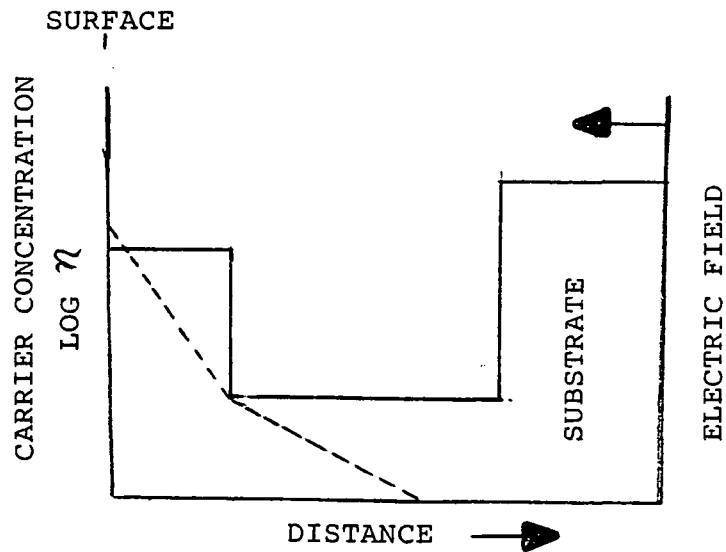
IMPATT diodes can be realized from various doping profile designs. The preferred profile structures utilized for the fabrication of devices used in this study were the single drift low-high-low (L-H-L) and high-low (H-L) profiles. Theory of operation predicted better performance specifically, higher RF output power ( $P_o$ ) and DC to RF conversion efficiency ( $\eta$ ), for the L-H-L Schottky-barrier GaAs devices as compared with the H-L grown junction GaAs devices. However, the average performance achieved did not favor one structure over the other.

Reliability data on both diode designs will assist in making recommendations for selecting the optimum design for the ultimate SSPA application.

SINGLE DRIFT GAs DOPING PROFILES  
WITH ELECTRIC FIELD



A. LHL PROFILE  
(MODIFIED READ)



B. HI-LO PROFILE  
(MODIFIED READ)

FIGURE 2.

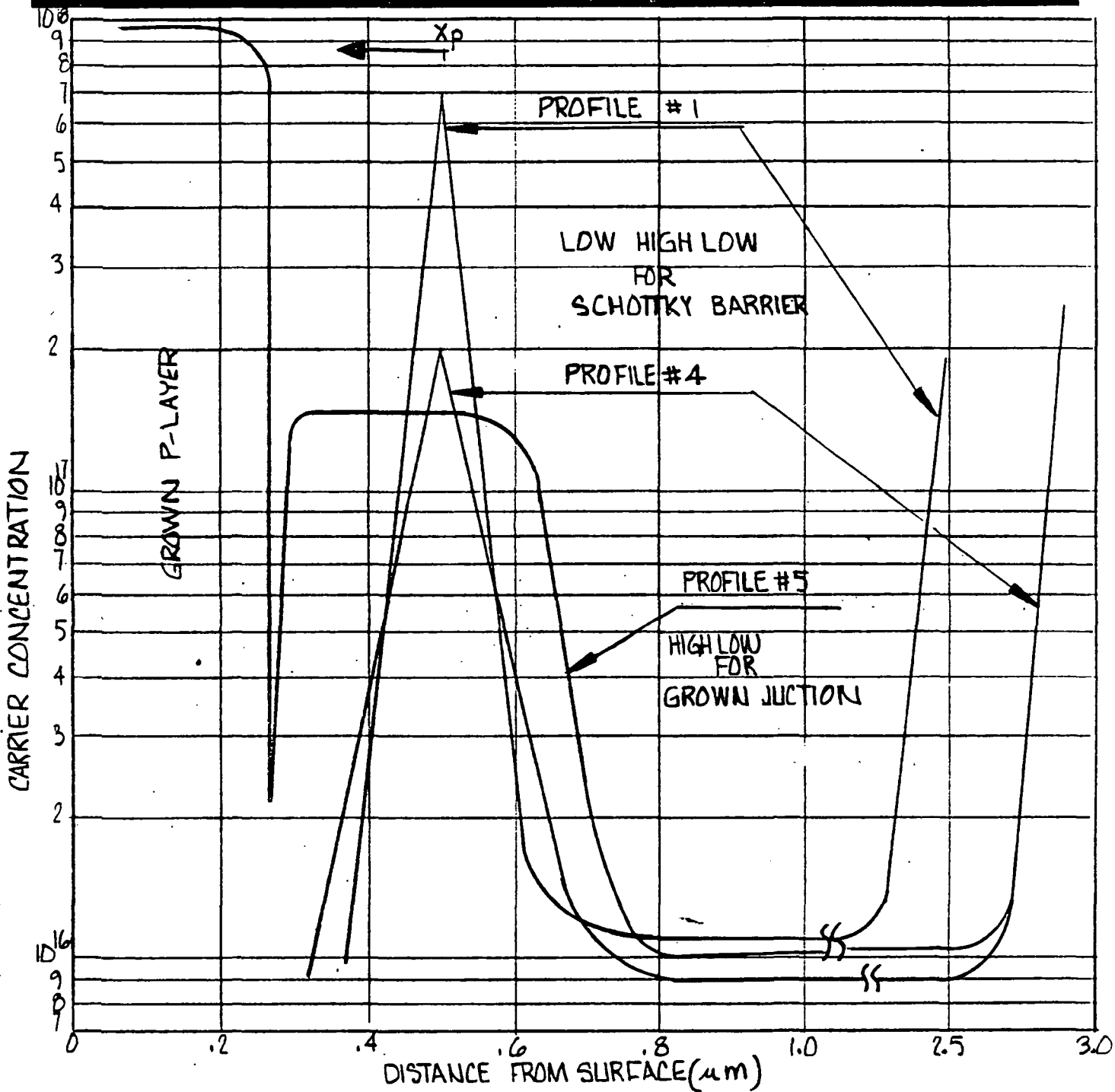
## 2.0 L-H-L Schottky-Barrier IMPATT Diodes

### 2.1 Objectives

For the purpose of obtaining first order reliability information, a relative broad data base must be established. Specifically, the question most often raised with respect to repeatability of state-of-the-art epitaxial GaAs growth needs to be satisfied first. To achieve this, LNR fabricated the diodes to be tested from various previously, performance qualified, wafers. Failure mechanisms identified during the initial reliability study, which appear to be common to the various wafer/ material lots will lead to defining process and assembly optimizations. After the device improvements have been implemented subsequent reliability studies need to address statistical requirements by stress testing devices fabricated from one epitaxial GaAs wafer (depending on the available wafer area, one wafer may yield up to several thousand chips).

The optimum design of a L-H-L GaAs IMPATT diode for sufficient RF power output and DC-RF conversion efficiency consistent with good current-voltage (I-V) characteristics having stable and sharp reverse voltage breakdowns ( $V_B$ ) and tolerable thermal resistance ( $\theta_{TH}$ ) represents the tradeoff between many competing factors. The key dimensional parameter is the distance ( $X_p$ ) of the Schottky-barrier surface to the center of the high doping spike. Diodes having a relative poor breakdown characteristics still perform satisfactorily during oscillator measurements, but generally demonstrate a short operating lifetime. Therefore, good I-V characteristics were emphasized rather than optimum RF performance, which also helped in keeping the device cost reasonable.

# EPITAXIAL GaAs PROFILE DESIGNS (LOW HIGH LOW AND HIGH LOW)



PROJECTED PERFORMANCE OF 20GHz PROFILE DESIGN

| PROFILE #  | 1   | 4   | 5   |
|------------|-----|-----|-----|
| $\eta$ (%) | 26  | 22  | 20  |
| $P_o$ (W)  | 3.5 | 7.8 | 2.5 |

$$\eta = \frac{1}{\pi} \cdot \frac{V_D}{V_A + V_D} \quad \text{WHERE } V_A = \int E(x) dx \text{ (AVALANCHE REGION)} \\ V_D = \int E(x) dx \text{ (DRIFT REGION)}$$

$$\int \alpha(x) dx = 1, \text{ WHERE } \int \text{COVERS THE ENTIRE DEPLETION REGION}$$

$$P_o = \frac{\eta}{1-\eta} \left( \frac{\Delta T_{max}}{\theta_{TH}} \right) \quad \text{WHERE } \frac{\Delta T_{max}}{\theta_{TH}} \text{ IS}$$

(13) ASSUMED TO BE 10 W

FIGURE 3.

## 2.2. IMPATT Chip Processing

Accordingly, the GaAs material was processed, taking the aforementioned criteria into consideration. The developed process flow shown enabled LNR to realize IMPATT chips with an average thickness of 10 to 12 microns and achieve stress-free chip separation.

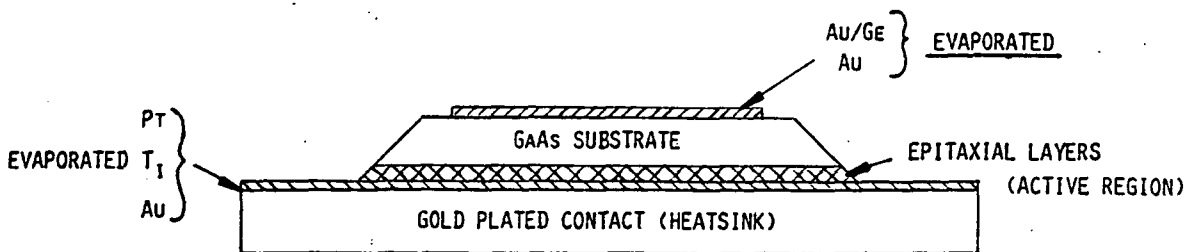


FIGURE 4.



A) SEM PHOTOGRAPH OF IMPATT DIODE MESA

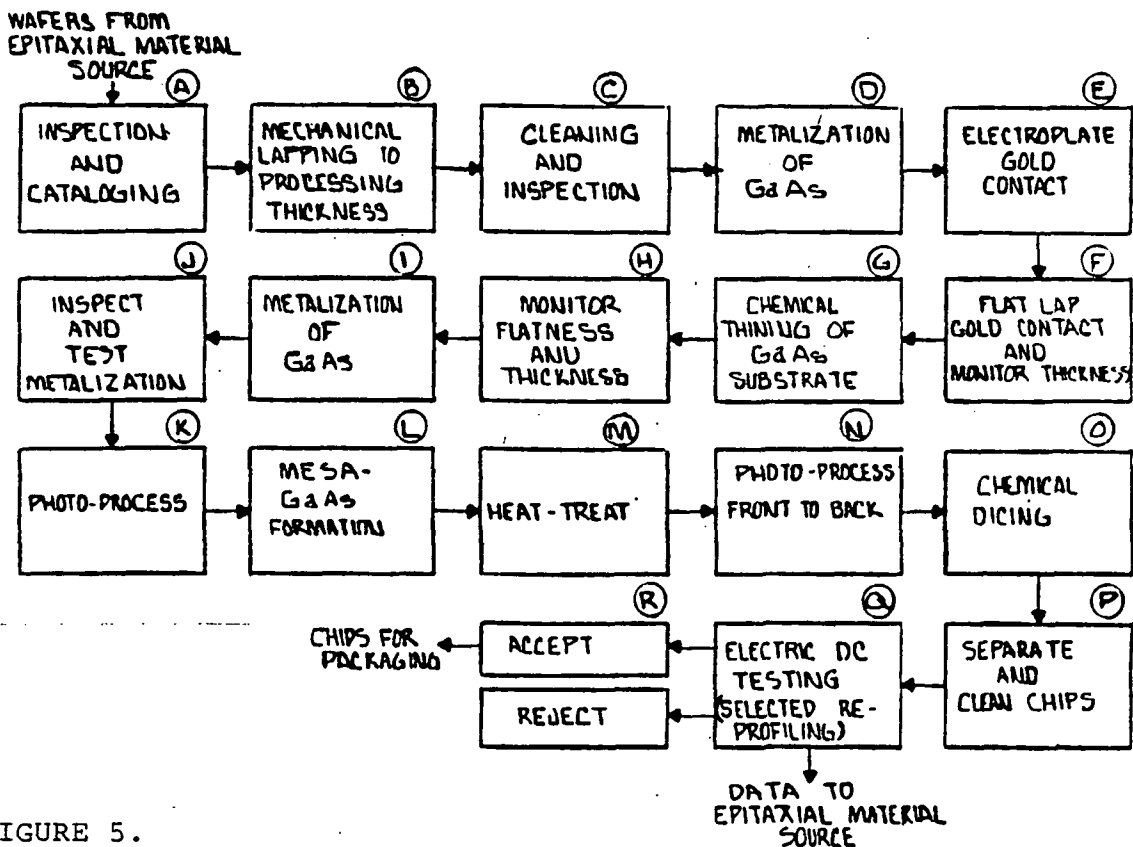


FIGURE 5.

B) PROCESS FLOW CHART FOR IMPATT CHIPS



### 2.3 IMPATT Chip Packaging

Prior to mounting the chips are examined at a magnification of 150X to 600X for potential mechanical or physical defects. This is followed by checking the forward voltage drop ( $V_f$ ), the breakdown voltage ( $V_B$ ) and the junction capacitance. At the same time a short (20 to 30 sec.) current stress (100ma) is applied to eliminate unstable or weak chips.

The chips are mounted into preselected and cleaned packages using a gold-tin (80/20) eutectic solder. The amount of solder is kept to an absolute minimum to assure flatness and maximum heat flow.

In general the contacting ribbon is first attached to the dielectric support or enclosure by means of TC-bonding or parallel gap welding. Initial contacting to the chip is again achieved by means of soldering with a minute quantity of Au/Sn solder (grow junction diodes were TC-bonded).

The junction capacitance is then reduced in discrete steps and RF tested until optimum performance is achieved.

The diodes are dried in a dry nitrogen atmosphere at 150°C for 4 to 8 hours. Without removal from the nitrogen atmosphere the diodes are then sealed in a dual step process previously developed at LNR for space borne applications.

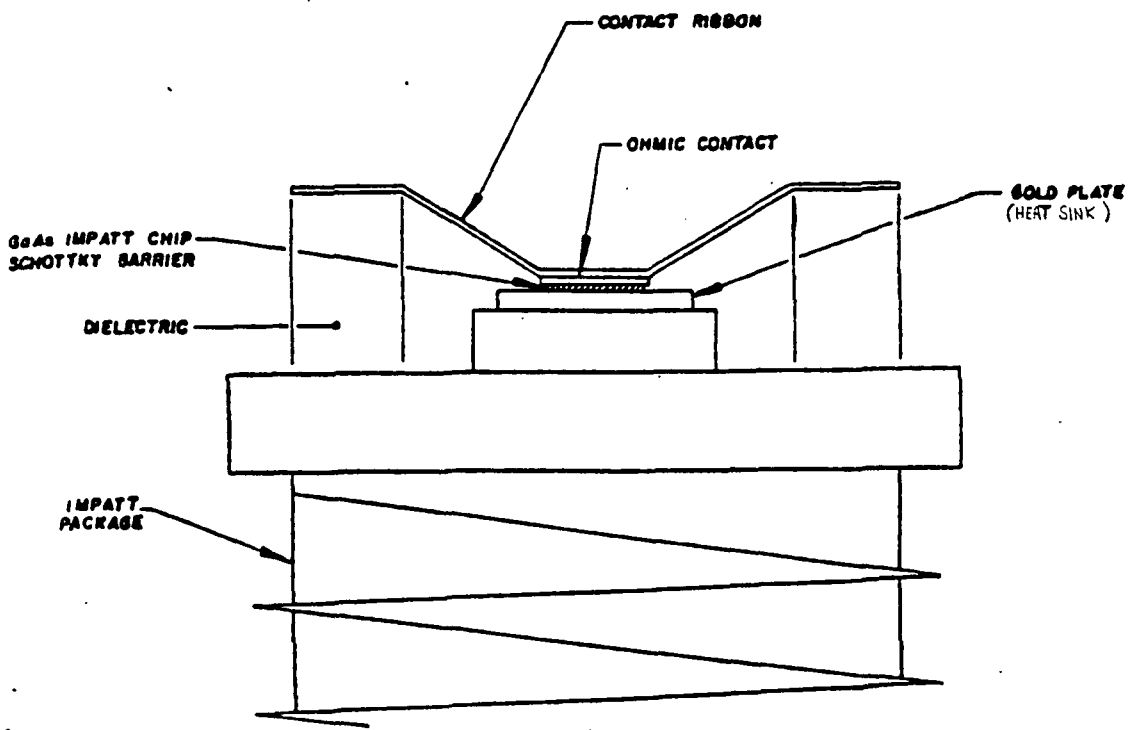
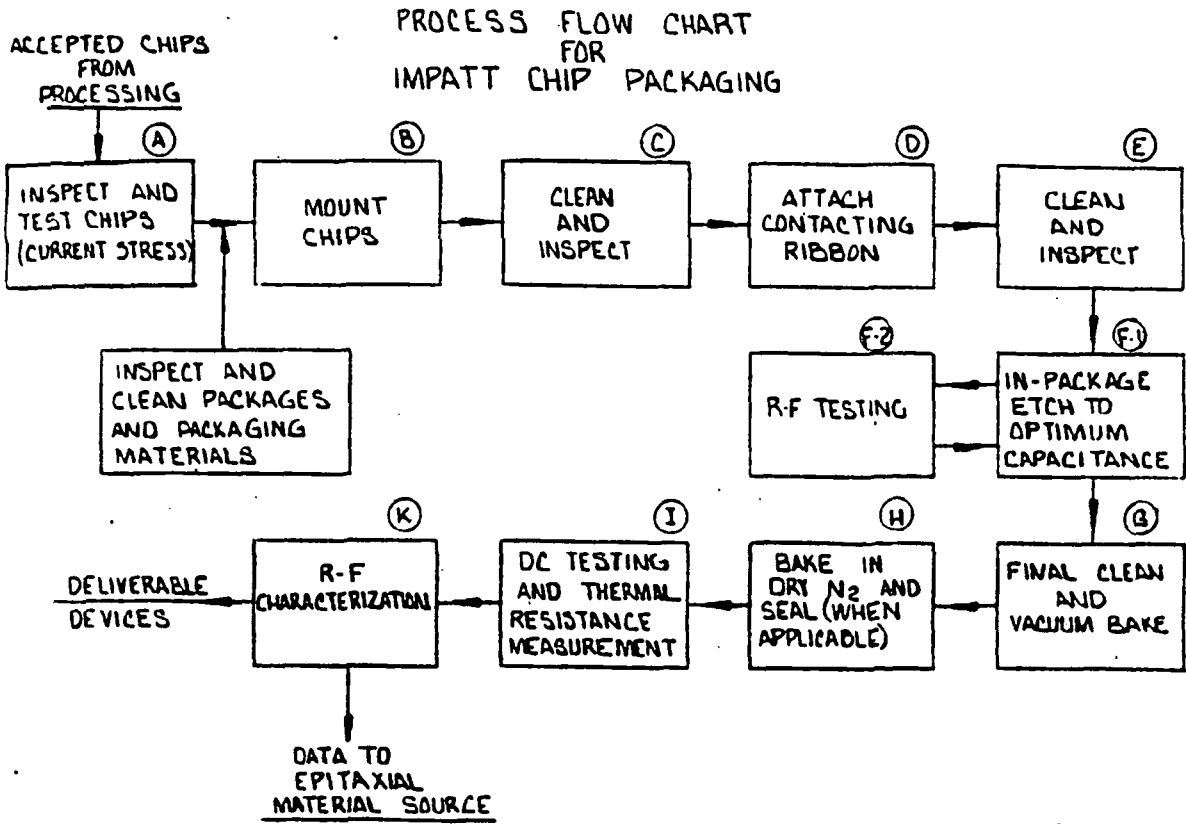


FIGURE 6.

CROSS SECTION OF PACKAGED IMPATT DIODE

### 3.0 H-L GROWN JUNCTION IMPATT DIODES

#### 3.1 Objective

Although, H-L grown junction IMPATT diodes were available at LNR, it was decided to utilize commercially available devices from a second source in the reliability study. Moreover, identical devices from the same source were evaluate at LNR during the development of a 20 GHz communications solid state power amplifier (AFWAL-TR-83-1142).

#### 3.2 Procurement

In all seventy five (75) IMPATT diodes were purchased from Varian Associates according to the following specifications:

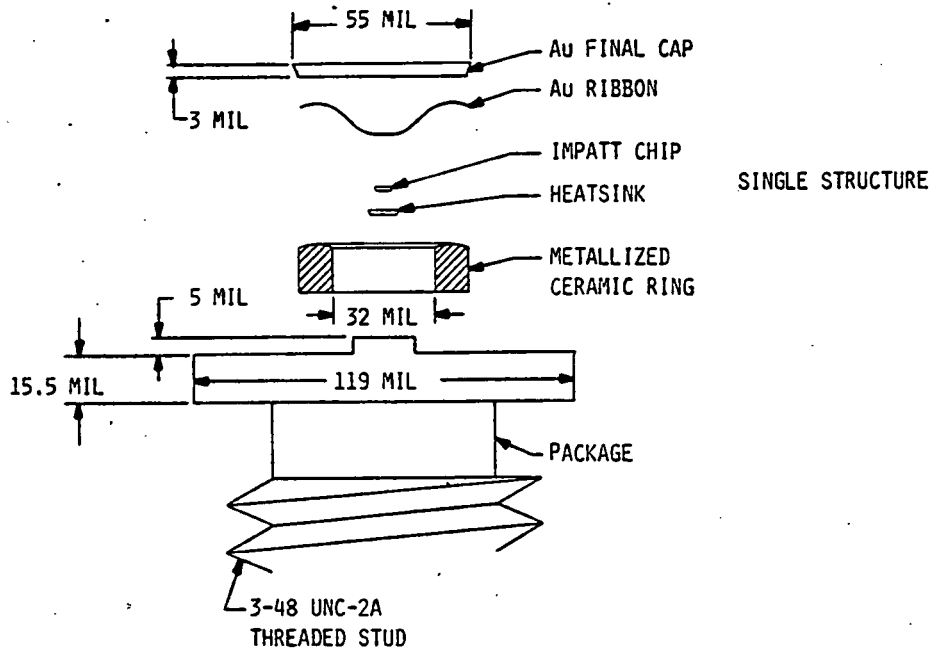
|                     |  |
|---------------------|--|
| Frequency Output:   | 20.0 GHz $\pm$ 1.0 GHz @ P <sub>o</sub> max. |
| Power Output:       | 1.5 Watts minimum                            |
| Thermal Resistance: | 30°C/Watt maximum                            |
| Efficiency:         | 16% minimum                                  |

Material processing and assembly data will be retained by Varian Associates, to be available for failure analysis if required.

#### 3.3 Device Assembly Summary

The assembly concepts employed by Varian and LNR as shown, were quite similar with the exception of minor proprietary procedures, which were determined to have no impact on the accelerated stress test data.

SINGLE DRIFT GAAS IMPATT  
DIODE ASSEMBLY



| Device Type                | Process                                 | Bonding Type     |                   |
|----------------------------|---|------------------|-------------------|
|                            |   | SCHOTTKY BARRIER | GROWN JUNCTION    |
| Standard<br>LNR/VARIAN     | IMPATT Chip/Heatsink<br>to package stud | Au/Sn            | Au/Sn             |
|                            | Ribbon to Chip                          | Au/Sn            | T.C.              |
|                            | SEALING                                 | Au/Sn            | Au/Sn             |
| <u>LNR</u><br>Experimental | Chip/Heatsink to<br>Package stud        | -                | T.C.              |
|                            | Ribbon to Chip                          | -                | Au/Sn and<br>T.C. |
|                            | Sealing                                 | -                | Au/Sn             |

Note: Experimental Devices were developed and funded by LNR in response to observations made during device fabrication and accelerated stress testing.

FIGURE 7.

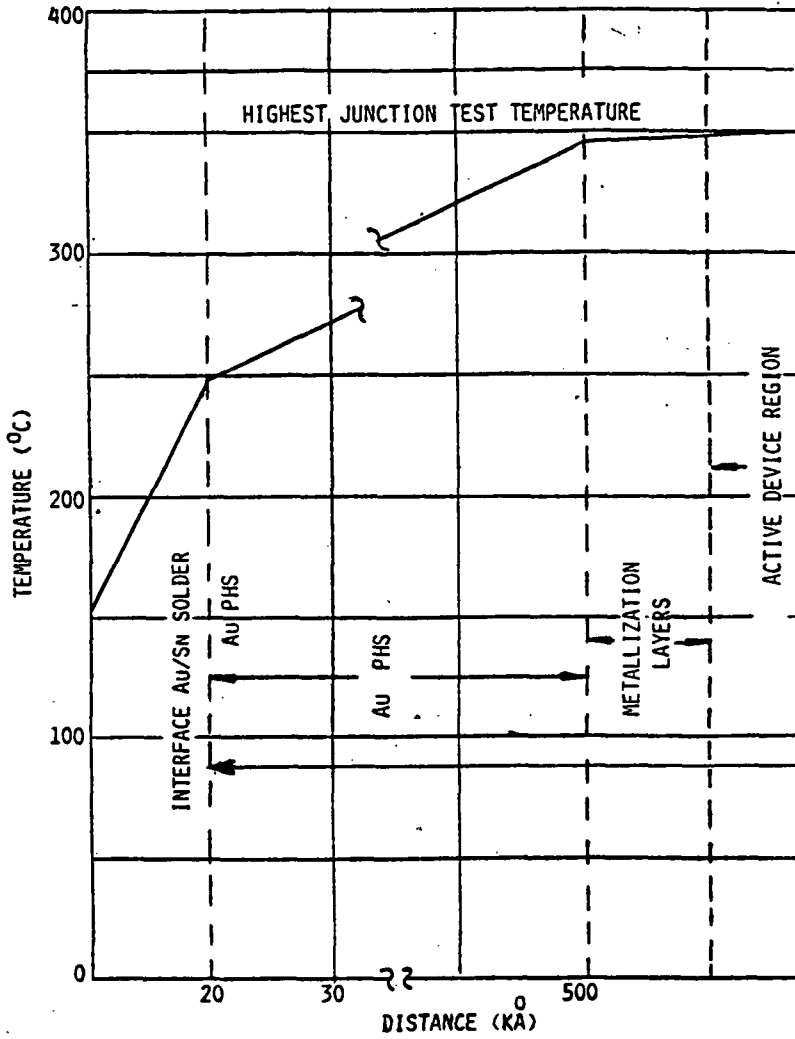
#### 4.0 THERMAL CONSIDERATIONS

The preferred bonding material used for the device assembly is the eutectic gold-tin (Au/Sn) solder. The selection was based on the results of evaluating various eutectic high temperature solders, including gold-germanium and gold silicon. The Au/Sn - compound has a strong affinity to combine with available gold, namely the package and heatsink gold plating and/or chip contact and ribbon. According to the Au/Sn phase diagram, which is extremely sharp, small compositional changes result in substantial increases in the melting or plastic temperature of the compound. This fact enabled the use of the Au/Sn solder for three different operations (chip mount, ribbon bond, sealing) during device packaging without incurring unwanted chip movement.

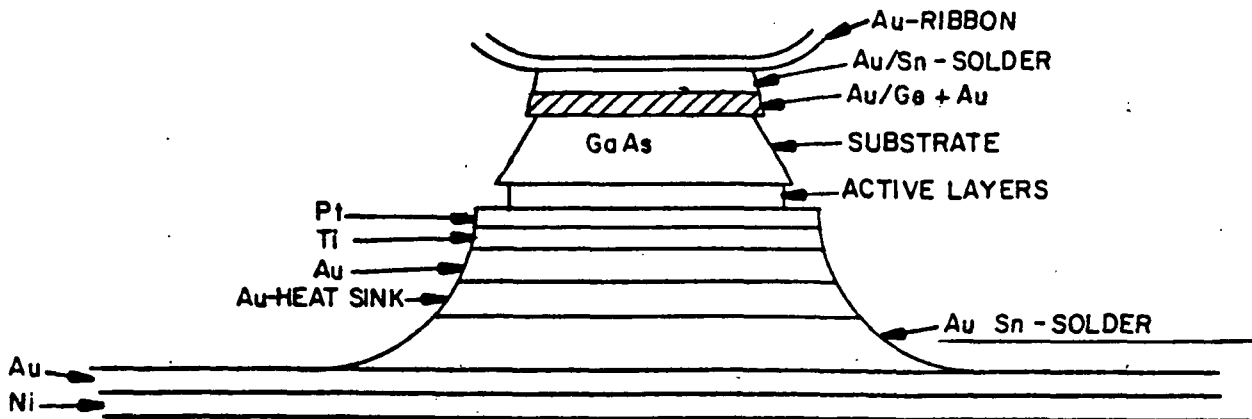
However, the affinity toward compositional change developed into a major failure mechanisms during accelerated DC stress testing. In a subsequent section this failure mechanism will be described in more detail.

Secondly, with one of the junction temperatures scheduled to be 345°C, a temperature profile was developed based on the highest junction stress test temperature and the calculated thermal impedances at the appropriate temperatures. The highest temperature, as shown on the profile, the Au/Sn would be subjected to at the chip to package interface is between 240°C and 250°C, well below the 280°C eutectic temperature.

TEMPERATURE PROFILE ACROSS 20 GHZ  
IMPATT DEVICE. (WORST CASE WITH  $\theta_{TH(AU/SN)} \approx 9^{\circ}C/W$ )



IMPATT CHIP CROSS SECTION



OFHC Cu-PACKAGE

FIGURE 8.

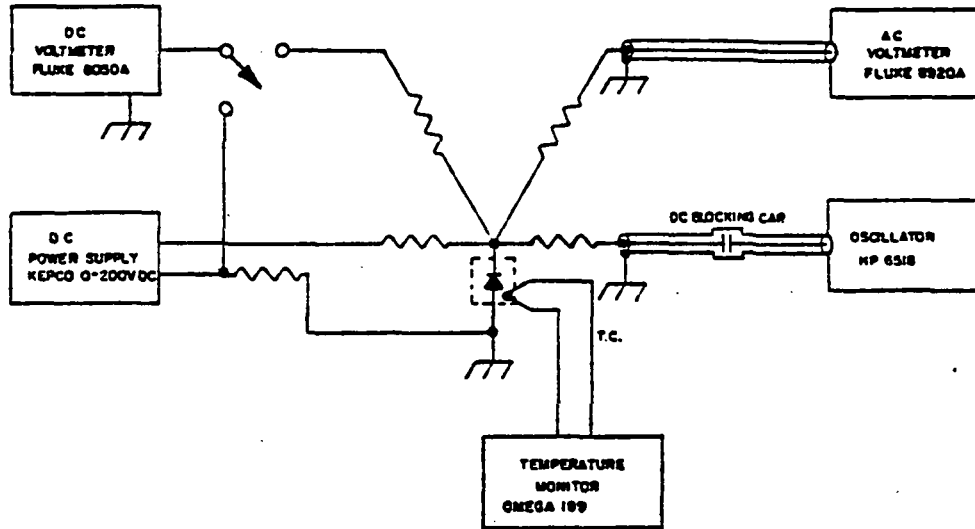
## 5.0 IMPATT DIODE CHARACTERIZATION

The evaluation of each of the IMPATT diodes fabricated as described previously included the measurement of:

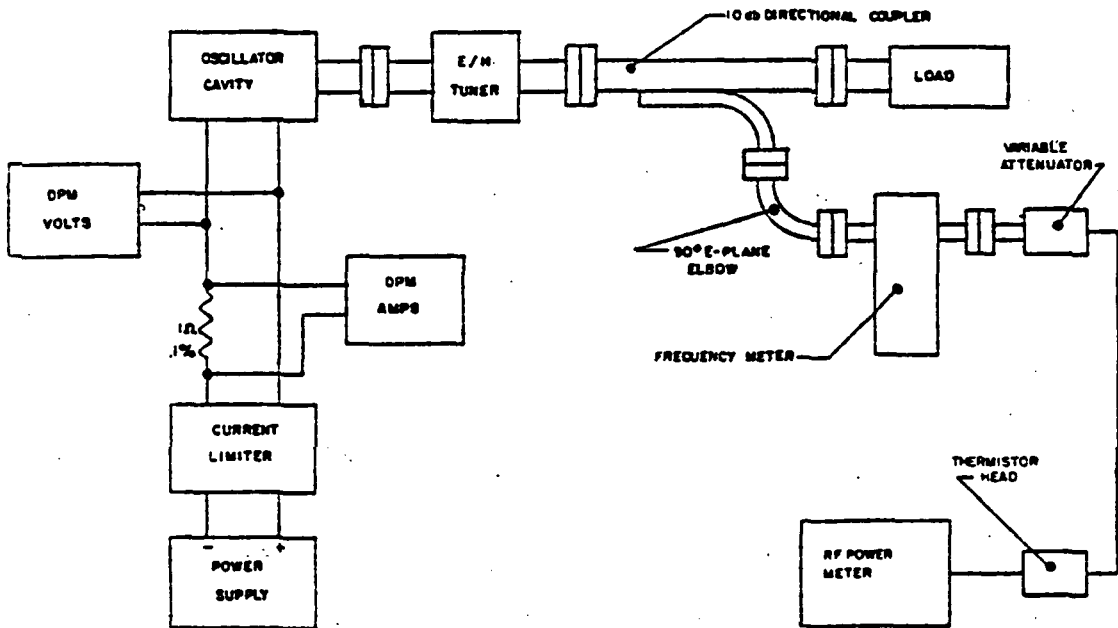
- DC current-voltage (I-V) behavior, including the diode forward ( $V_F$ ) and reverse ( $V_B$ ) breakdown voltages, and the leakage current ( $I_L$  measured at 50% of the  $10\mu\text{a}$  reverse breakdown voltage);
- Capacitance-voltage (C-V) measurements taken at zero bias, minus 3 volts and near the reverse breakdown. In addition, two diodes of each metalization lot are used for profile reconstruction (as described previously) to identify potential processing related changes and barrier interface instabilities;
- thermal resistance ( $\theta_{th}$ ) to determine diode junction temperature and to identify problems associated with the chip and/or contacting ribbon bonds;
- RF parameters, such as power output ( $P_O$ ), operating frequency, DC-RF conversion efficiency ( $\eta$ ) operating voltage and current.

The thermal resistance measurement configuration developed at LNR, utilizing a unique refinement of the Haitz\* method eliminates all frequency-dependent components, except for one blocking capacitor, permitting small signal CW measurements as opposed to the usual pulse method. The measurements are made through a high series resistance, thus protecting the device under test. A major advantage of this measuring method is a highly flat frequency response up to 20 MHz as compared to an upper limit of only  $\sim 3$  MHz on the part of other related methods. Therefore, it is possible to measure thermal response times of  $\lesssim 50$  ns. The overall accuracy of the thermal resistance measurements is typically within four percent. The one limitation of measuring thermal resistance as described is that it is breakdown voltage dependent, e.g. devices with degraded I-V characteristics can not be measured accurately.

\* R.H. Haitz, H.L. Stover and N.J. Tolar, IEEE Trans. Electron Devices ED-16, pg. 438 (1969)



A, THERMAL RESISTANCE MEASUREMENT CIRCUIT



B. BLOCK DIAGRAM OF OSCILLATOR MEASUREMENT SETUP FOR 20GHz IMPATTs

FIGURE 9.



# THERMAL RESISTANCE



LOT NO. \_\_\_\_\_

DATE: \_\_\_\_\_

DIODE NO. \_\_\_\_\_

NAME: \_\_\_\_\_

● MEASURED DATA:

|                          |                          |                           |
|--------------------------|--------------------------|---------------------------|
| T = 40°C                 | T = 50°C                 | ΔV <sub>B</sub> _____     |
| I <sub>R</sub> = 10mA    | I <sub>R</sub> = 10mA    | ΔT _____                  |
| V <sub>B</sub> = _____ V | V <sub>B</sub> = _____ V | ΔV <sub>B</sub> /ΔT _____ |
| <br>                     | <br>                     | <br>                      |
| f = 10 MHz               | f = 30 Hz                | T = 40°C                  |
| V <sub>O</sub> _____     | V <sub>O</sub> _____     | I <sub>R</sub> = 10 mA    |
| V <sub>D</sub> _____     | V <sub>D</sub> _____     | V <sub>B</sub> _____ V    |
| V <sub>R</sub> _____     | V <sub>R</sub> _____     |                           |

● CALCULATED DATA:

1. SPACE CHARGE RESISTANCE (R<sub>sc</sub> measuring frequency = 10 MHz)

$$R_{sc} = \left( \frac{V_O - V_R}{V_O - V_D} \right) \times \left( \frac{V_D}{V_R} \right) \times 95 = \boxed{\text{_____ ohms}}$$

2. TOTAL RESISTANCE (R<sub>T</sub> measuring frequency = 30 Hz)

$$R_T = \left( \frac{V_O - V_R}{V_O - V_D} \right) \times \left( \frac{V_D}{V_R} \right) \times 95 = \boxed{\text{_____ ohms}}$$

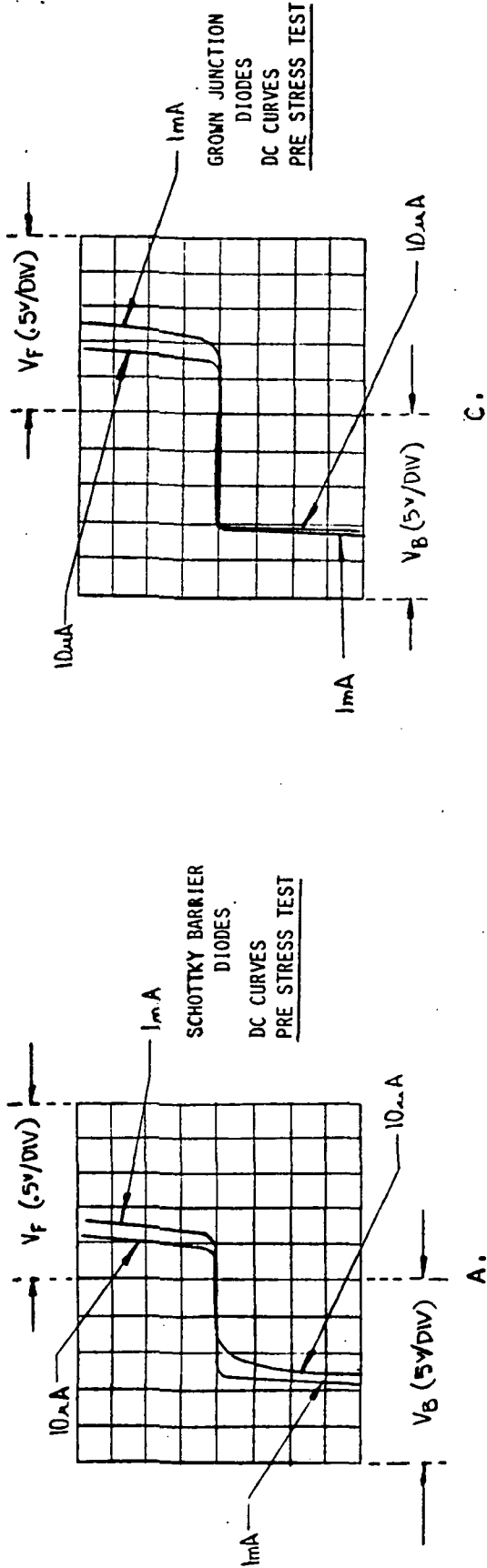
3. THERMAL RESISTANCE (θ<sub>th</sub>)

FIGURE 10.

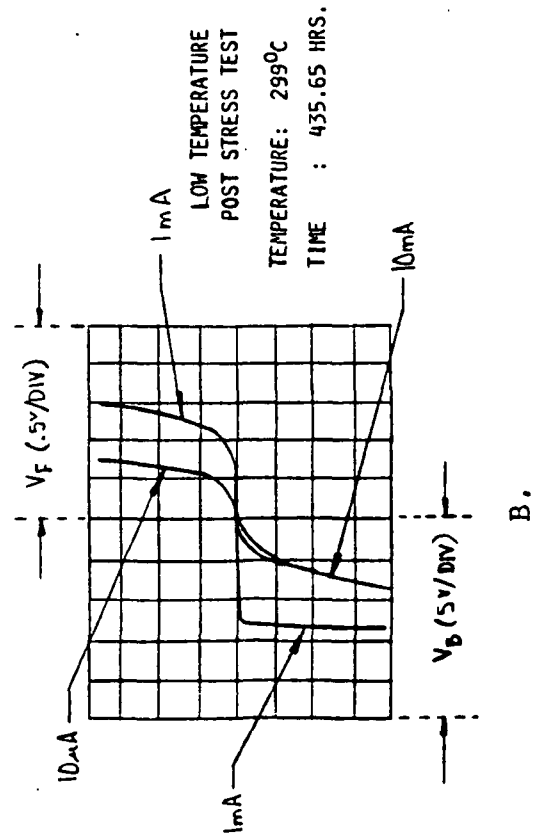
$$\theta_{TH} = \frac{R_T - R_{sc}}{\frac{\Delta V_B}{\Delta T} V_{B(40^\circ C)} + R_T I_R} = \frac{(\quad) - (\quad)}{\frac{(\quad)}{(\quad)} (\quad)_{40^\circ C} + (\quad)(\quad)}$$

$\theta_{TH} = \text{_____ } ^\circ\text{C/w}$

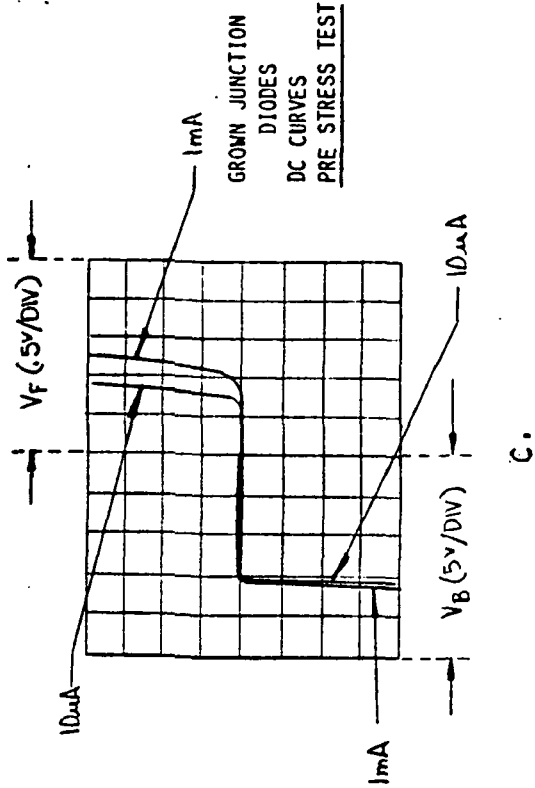
CURRENT VOLTAGE CHARACTERISTICS (I-V)  
(TYPICAL)



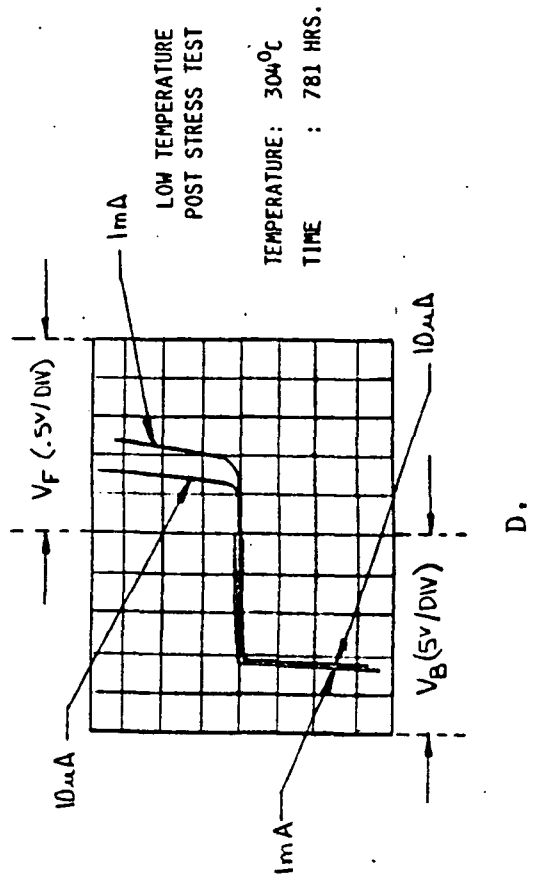
A.



B.



C.



D.

B. IS NOT SUITABLE FOR THERMAL RESISTANCE MEASUREMENT

FIGURE 11.

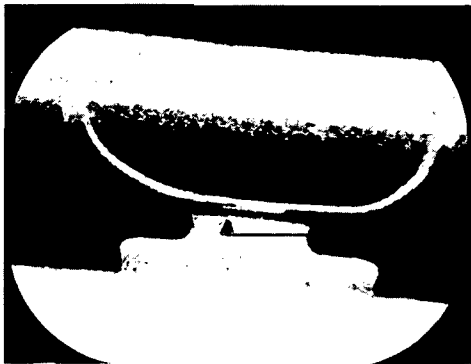
Devices accepted following the fine and gross leak measurements were evaluated via X-Ray photography to determine the internal (e.g. inside of sealed package) physical condition(s) of chip, ribbon, seal and bonds. The X-Ray examination was carried out on all devices used in this reliability study.

X-RAY PHOTOGRAPH OF A GOOD IMPATT DIODE



- GOOD SHAPE OF RIBBON
- NO EXCESS METALIZATION ALONG THE SIDES

X-RAY PHOTOGRAPH OF A marginally acceptable IMPATT DIODE



- GOOD SHAPE OF RIBBON
- NO EXCESS METALIZATION ALONG THE SIDES
- ONLY THREE FOURTHS OF THE CONTACT IS BONDED TO THE RIBBON

X-RAY PHOTOGRAPHS OF REJECTED IMPATT DIODES



- GOOD SHAPE OF RIBBON
- NO EXCESS METALIZATION ALONG SIDES
- PARTIAL BOND OF CONTACT RIBBON- CAUSE OF REJECTION

A complete history of the DC and RF characterization data of device lots ultimately used for accelerated DC stress testing is shown.

LNR Lot definition

Lot No.: (83-8) 83-16B G380-4

Where:

(83-8) = Fabrication Request

(83-16B) = YEAR - WEEK, Assembler Identification

G380-4 = Wafer # - Metallization Processing Lot

In addition each device started during fabrication is serialized, the serial number cannot be reassigned.

DC AND RF DATA



IMPATT DIODE ACCEPTANCE TEST - DC DATA

LOT # (83-8)83-16B G380-4 V= VOLTS C = pF Ir = NANOAMPS (I<sub>L</sub> @ .5V<sub>B</sub> @ 10ua)

| UNIT # | STEP 1 OF PROCESS FLOW<br>DC DATA DATE: 5/10/83 |       |                |                 |                |        |                |        | FINAL PRE STRESS TEST<br>DC DATA DATE: 6/6/83 |       |                |                 |                |        |                |        |
|--------|---|-------|----------------|-----------------|----------------|--------|----------------|--------|---|-------|----------------|-----------------|----------------|--------|----------------|--------|
|        | C <sub>o</sub>                                  | C-3   | I <sub>L</sub> | θ <sub>th</sub> | V <sub>F</sub> |        | V <sub>B</sub> |        | C <sub>o</sub>                                | C-3   | I <sub>L</sub> | θ <sub>th</sub> | V <sub>F</sub> |        | V <sub>B</sub> |        |
|        |   |       |                |                 | @ 10ua         | @ 1 ma | @10ua          | @ 1 ma |   |       |                |                 | @ 10ua         | @ 1 ma | @10ua          | @ 1 ma |
| 1555B  | 10.886  | 9.272 | 70             | 28.9            | .47            | .70    | 10.6           | 12.4   | 10.893  | 9.279 | 80             | 29.10           | .45            | .69    | 10.6           | 12.4   |
| 1559B  | 10.914  | 9.283 | 12             | 28.8            | .48            | .70    | 11.2           | 12.6   | 10.920  | 9.289 | 12             | 29.41           | .47            | .67    | 11.8           | 12.6   |

IMPATT DIODE RF - TEST DATA

LOT # (83-8)83-16B G380-4

| UNIT # | STEP F-2 PROCESS FLOW<br>RF DATA DATE 5/10/83 |                |                |                |      |                 |                | FINAL PRE STRESS TEST RF DATA DATE 6/6/83 |                 |                |                |                |      |                 |
|--------|---|----------------|----------------|----------------|------|-----------------|----------------|---|-----------------|----------------|----------------|----------------|------|-----------------|
|        | I <sub>o</sub>                                | V <sub>o</sub> | f <sub>o</sub> | P <sub>o</sub> | n(θ) | SP/PN           | I <sub>o</sub> | V <sub>o</sub>                            | P <sub>IN</sub> | P <sub>o</sub> | P <sub>D</sub> | f <sub>o</sub> | n(θ) | SP/PN           |
| 1555B  | .313  | 26.2           | 19.20          | 1.35           | 16.5 | 50<br>350<br>56 | .339           | 27.2                                      | 9.22            | 1.47           | 7.75           | 19.11          | 15.9 | 325<br>56       |
| 1559B  | .292  | 26.8           | 19.85          | 1.19           | 15.2 | 50<br>350<br>56 | .307           | 27.9                                      | 8.57            | 1.44           | 7.13           | 19.18          | 16.8 | 60<br>325<br>56 |

Note: SP/PN - denotes oscillator tuning information

FIGURE 13.

### III. TECHNICAL DISCUSSION - ACCELERATED CONSTANT DC STRESS TEST FOR 20 GHz IMPATTS

#### 1.0 Introduction

Stress tests should be designed to accelerate failure mechanisms so that a device which would fail under normal operating conditions in millions of hours will fail orders of magnitude sooner. Certain reactions are known to be temperature dependent without incurring secondary electro-migration effects. In such cases it must be determined if the reaction follows the Arrhenius equation,

$$\gamma_M = \gamma_0 \exp. \left( \frac{E_a}{kT} \right)$$

The determination of whether or not the progress follows the Arrhenius dependence is a multi-step operation and that for a single failure mechanism which has been experimentally observed (4,5) the following criteria apply:

- the probability density function (pdf) at a constant temperature and applied electrical stress is log normal;
- the logarithmic variance is independent of temperature;
- the median lifetime follows the Arrhenius dependence. (shown schematically)

Thermal stressing as a means of accelerated aging of semiconductor devices is an accepted and widely utilized form of assessing the reliability of such devices. (4,5)

The diodes tested are conventional 20 GHz single drift GaAs IMPATTs and were not subjected to any thermal or electrical stressing to remove early failures.

ARRHENIUS REACTION RATE CHART  
SAMPLE

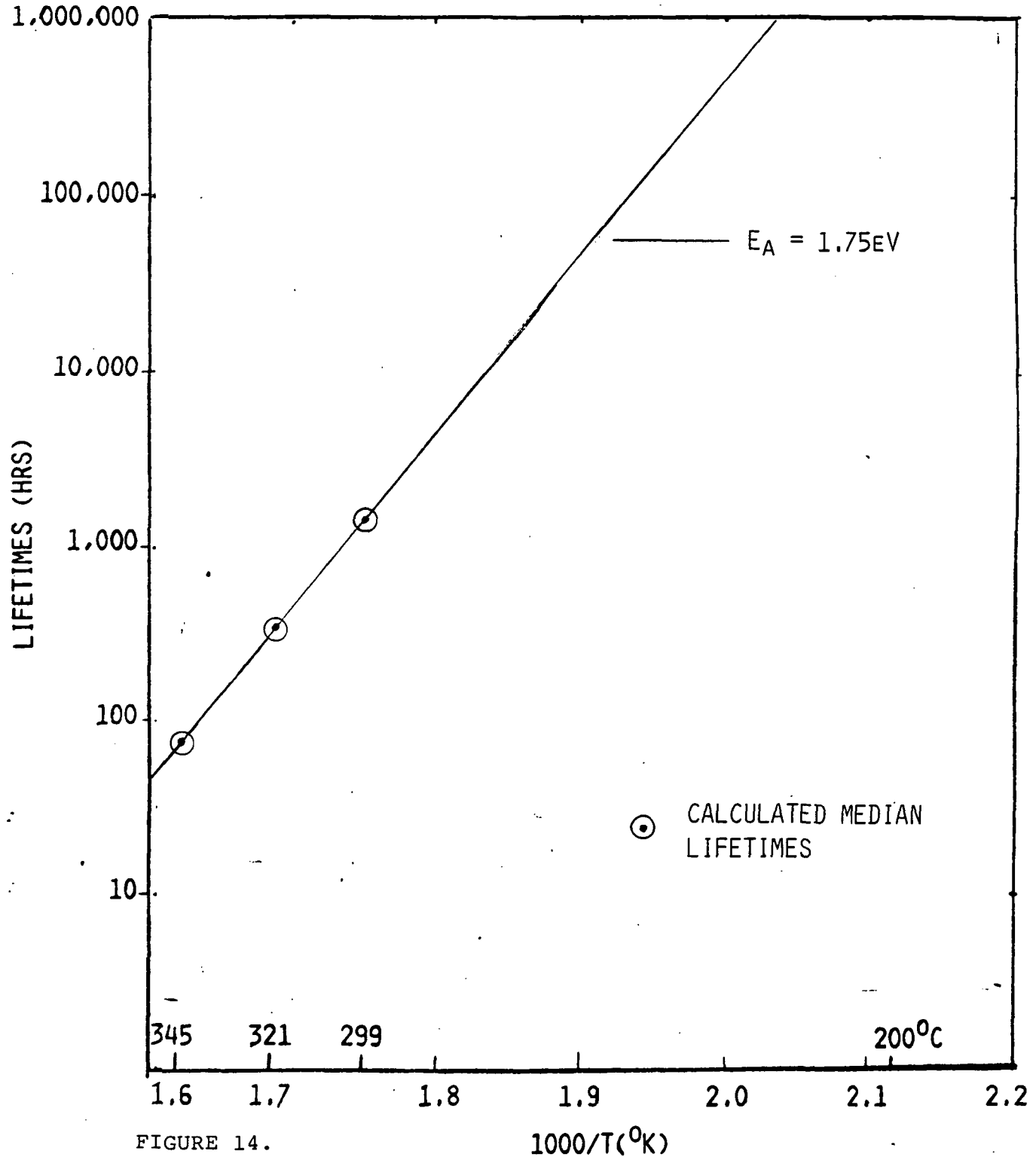


FIGURE 14.



In configuring a design for accelerated device aging, a concise work plan was developed comprised of the six major tasks.

1. Design and implement thermally accelerated stress test.
2. Design and fabricate stress test rack.
3. Conduct the required number of stress tests for each diode type.
4. Experimentally verify observations made during the diode fabrication and stress testing.
5. From the stress test data construct cumulative failure vs. time to failure and Arrhenius reaction rate plots.
6. Perform failure analysis as required.

## 2.0 Design and Implementation of Thermally Accelerated Device Aging

Taking into consideration the guidelines set forth in an "Accelerated Testing Model"<sup>6</sup> the selection of the number and choice of temperatures used to thermally accelerate device aging are a function of the following considerations. The lowest stress test temperature must be consistent with the program schedule of eighteen months. Selection of the highest test temperature is clearly a function of the diode bonding materials used and the start up system stabilization, e.g., the projected median lifetime must be sufficiently long to enable accurate monitoring and measurements following completion of start-up. Placing a number of diodes at a third temperature, midway between the two extremes will enable the construction of the required Arrhenius reaction rate plot with acceptable accuracy and indicate an earlier trend of the stress data, signified in the activation energy (Ea).

The following equations were used in determining the stress test temperatures. It must be noted, that certain assumptions and/or projections were required since actual data was not available to complete the calculations.

### Standard deviation ( $\sigma$ ) equation

$$\sigma = \ln\left(\frac{t_{50}}{t_{16}}\right) \text{ OR } \ln\left(\frac{t_{84}}{t_{16}}\right)$$

Where:

- $t_{16}$  = Time to failure of 16 percent of sample.
- $t_{50}$  = Median time to failure of 50 percent of sample.
- $t_{84}$  = Time to failure of 84 percent of sample

The standard deviation is assumed to be equal to 1.0, which is characteristic of a reasonable mature and well-controlled process (acceptable variance range is 0.5 to 2.0).<sup>(4)</sup>

Activation Energy (Ea) Equation

$$Ea = \frac{K \ln \left( \frac{t_1}{t_2} \right)}{\frac{1}{T_1} - \frac{1}{T_2}} \text{ eV}$$

Where:

- K = Boltzmann's constant (8.625x10<sup>-5</sup> eV/°K)
- T<sub>1</sub> and T<sub>2</sub> = Low and High Temperatures (°K) respectively
- t<sub>1</sub> and t<sub>2</sub> = Median life (Hrs.) at T<sub>1</sub> and T<sub>2</sub> respectively

The activation energy is assumed to be 1.75eV, furthermore projecting a median life at a given temperature will permit the calculation of a second temperature consistent with a desired median life.

Estimating a median life of 90 hours (t<sub>16</sub> = 33 hours) and using a maximum safe test temperature of 345°C based on the aforementioned thermal profile, the remaining test temperature was derived:

$$\begin{aligned} T_{\text{HIGH}} &= 345^{\circ}\text{C} \\ T_{\text{MEDIUM}} &= 321^{\circ}\text{C} \\ T_{\text{LOW}} &= 299^{\circ}\text{C} \end{aligned}$$

PROJECTED HIGH TEST TEMPERATURE (T = 345°C)  
 LOGNORMAL CUMULATIVE FAILURE DISTRIBUTION

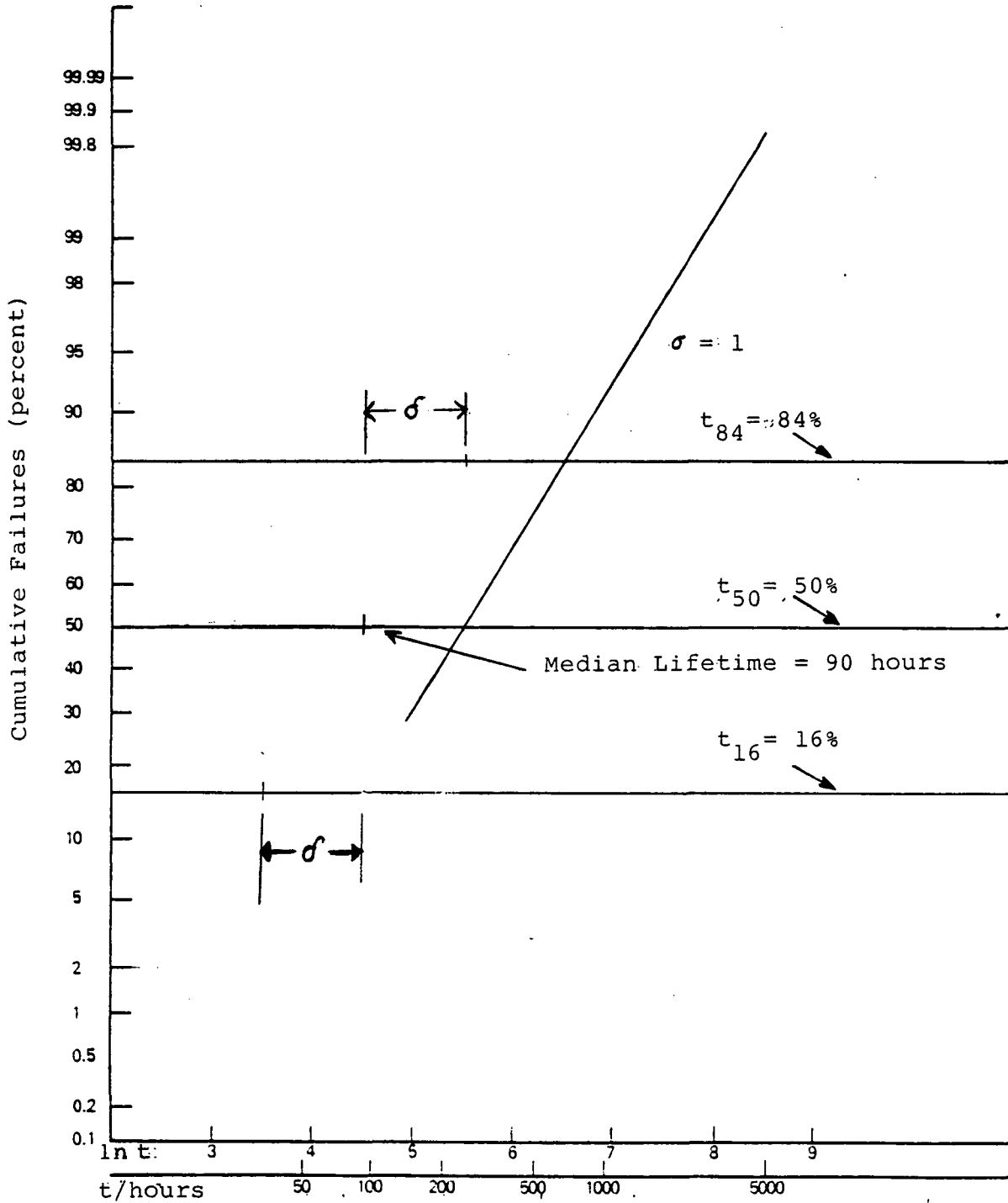


FIGURE 15.

### 3.0 Preferred Stress Test Approach

Ideally, the IMPATT diodes should be thermally aged at an accelerated rate under actual operating conditions for maximum confidence in the reliability data. However, high cost of accelerated aging under RF stress and temperature related circuit/device matching and monitoring of large number of devices make the accelerated operational aging impossible. Consequently, it was decided to employ a constant DC stress test at three predetermined elevated junction temperatures. For completeness of the reliability data and to establish correlation between RF and DC stressing, it was initially proposed to include accelerated RF stressing on a small sample of IMPATT diodes.

Subsequent experiments addressing the RF Stress testing configuration however revealed a sharp degradation of the RF performance at elevated baseplate temperatures. Unable to achieve the required stress test temperature without the collapse of the oscillation mode in spite of making the appropriate circuit adjustments, efforts to implement accelerated RF stressing were discontinued. Experimental observations are described in more detail in Appendix 'C'.

In achieving the desired DC junction stress temperature it was decided not to overstress the diodes electrically and/or thermally, since in either case unrelated failure mechanisms may be activated, which have no bearing on the actual reliability of the device under test. Thus, the accelerated constant temperature DC stress testing was carried out by first measuring the thermal resistance, the DC power input and the RF power output of each diode measured in a 20 GHz oscillator test mount. Secondly, the baseplate temperature ( $T_{BP}$ ) of the test fixture was brought to a predetermined level, which was based on the average thermal resistance of the device test lot and the stress temperature. The

baseplate temperature was held to a maximum of 150°C to minimize any potential thermal effects on fixture components and be consistent with device related constraints described in a later section. Finally, adding to the thermal resistance of the diode a correction factor resulting from a change in thermal resistance due to an increase in temperature and thermal impedance of device mounting interfaces, back biasing the diode into avalanche until the dissipated DC power raises the junction stress temperature to its required level.

The DC power dissipation was limited to 90 percent of the power dissipated during oscillator measurement and is given by:

$$T_J = \theta_{TH(TOTAL)} \cdot 0.9 (P_{DC} - P_{RT}) + T_{BP}$$

$$T_J = \theta_{TH(TOTAL)} (P_D) + T_{BP}$$

where:

$T_J$  = Diode Junction Stress Temperature (°C)

$T_{BP}$  = Baseplate Temperature (°C)

$\theta_{TH(TOTAL)}$  = Thermal Resistance of diode and correction factor (°C)

$P_D$  = Power dissipated during oscillator measurement

$P_D = (P_{DC} - P_{RF}) = I_{IN} V_{IN}$  (W)

#### 4.0 Stress Test Rack

The following design and functional concepts served as guidelines for the fabrication of the required stress test rack.

##### Design Concept

- Temperature controlled diode stress test fixture
- Series resistance controlled diode bias with constant voltage source
- Fast speed protection circuit to prevent excessive current at the time of failure (in addition to power shut down)
- Elapsed time meter (non-resettable)
- Individual diode adjustable voltage and adjustable current
- Diode "Turn-On" transient protection
- Room Temperature to 170°C operating baseplate
- 5 to 50 volt and 0 to 1 ampere operation
- Nanoampere leakage measurement capabilities

##### Functional Concept

- Capacity - 24 individually controlled diode test positions (20 required number of diodes to be tested plus 4 experimental diodes)

##### Monitoring

- Individual power input
- Individual operating time
- Individual diode over-voltage and over-current shut down
- Monitoring diode parameters during testing without disturbing the other diodes

CROSS SECTION OF DIODE STRESS TEST FIXTURE

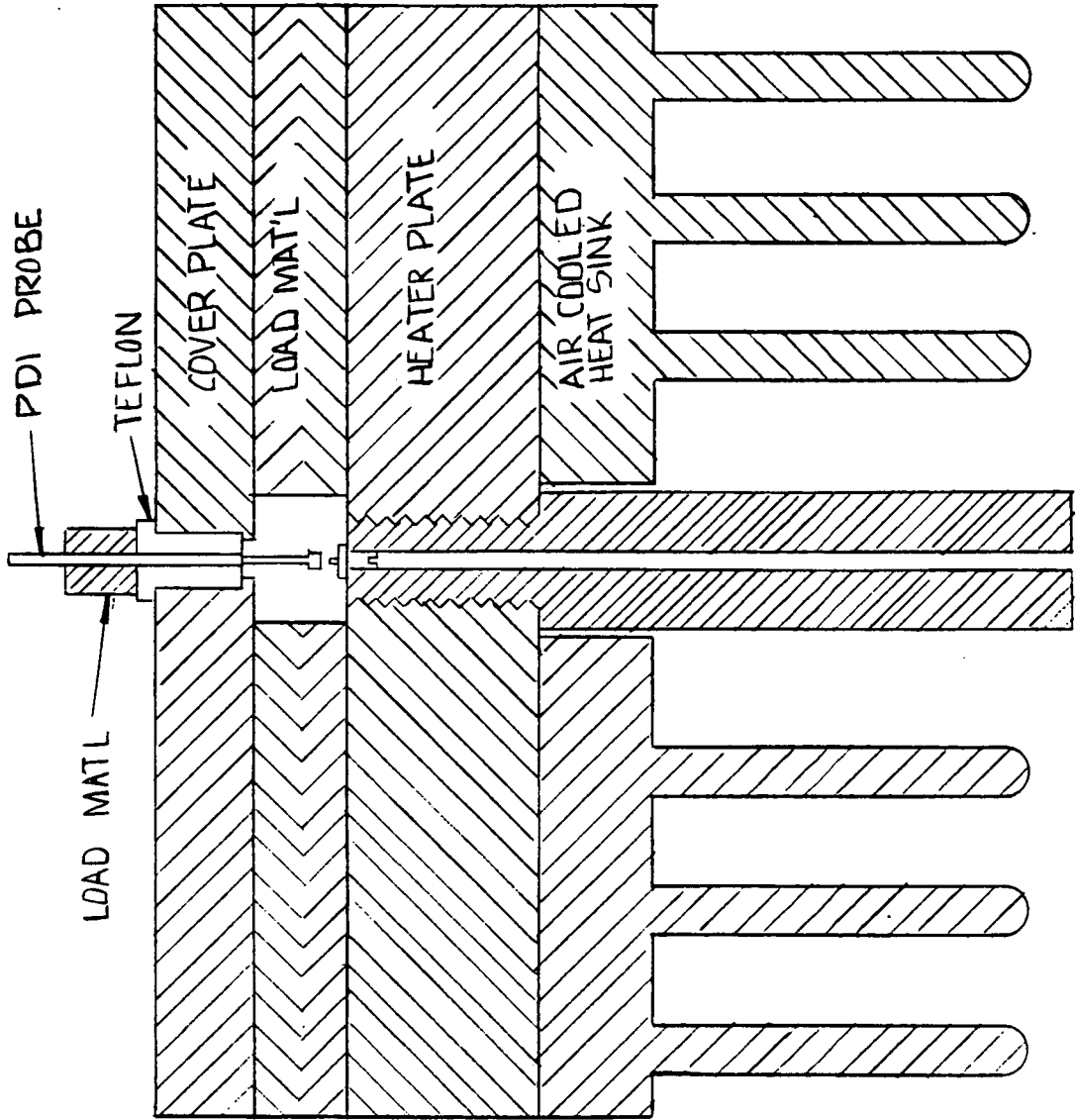
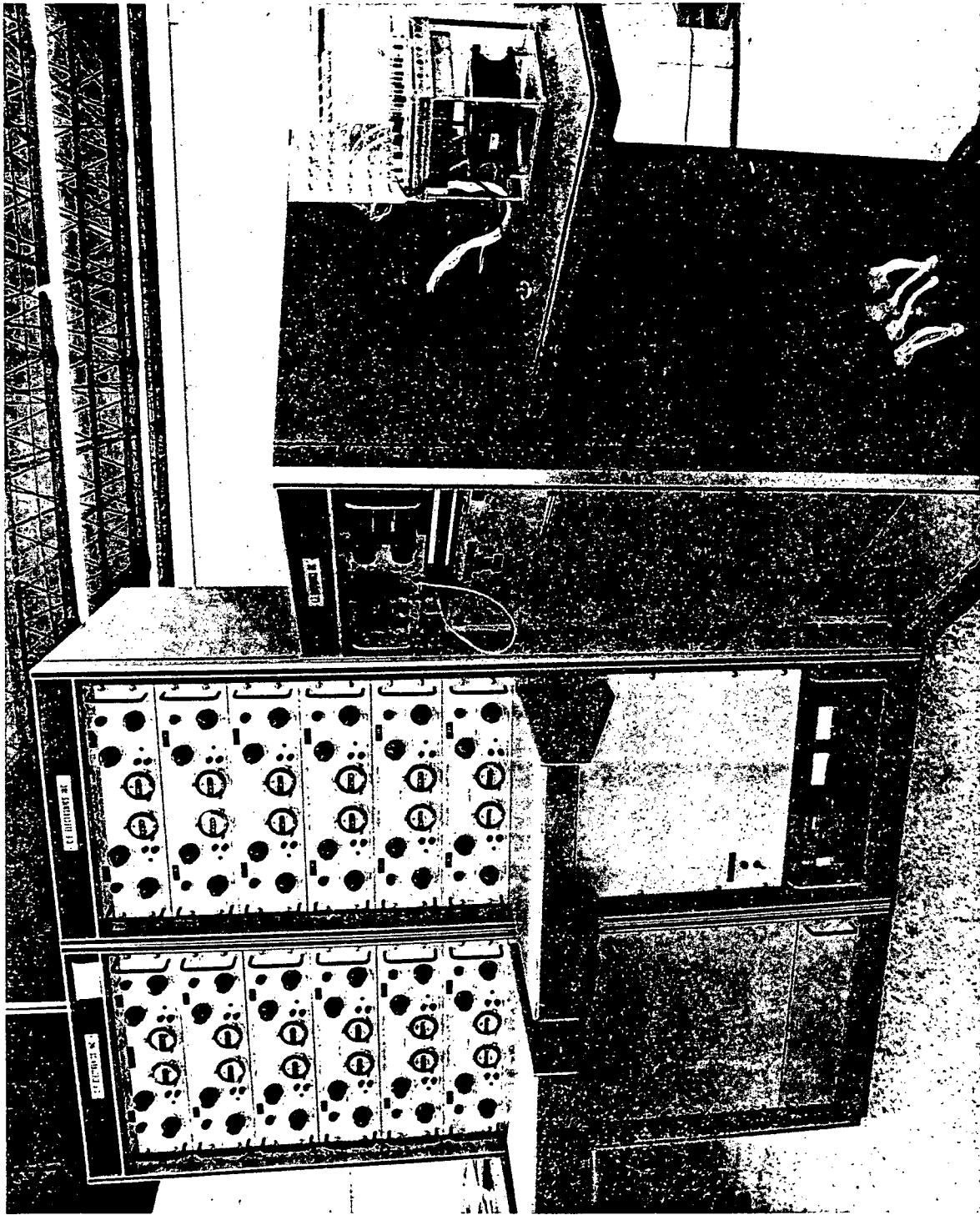


FIGURE 16.





DC STRESS TEST RACK

FIGURE 17.

## 5.0 Stress Test Procedures

For the implementation of the thermally accelerated constant DC stressing of 20 GHz IMPATT diodes an operational test procedure (LNR No.: 119012992) was developed consisting of the following major operations.

- preparations of the stress test rack prior to start-up include safety and operational functions;
- diode loading and in system measurements;
- temperature controller turn on and adjustment;
- DC-bias current adjustment for the required power dissipation;
- in-situ tests and diode measurements (as shown);
- monitoring schedule (as shown).

Monitoring of the device parameters is less than one minute per device. Measurements are made while input power is appropriately reduced on each diode individually, e.g. stressing is interrupted for less than one minute.

# TEST PROCEDURE



## TEST TEMPERATURE

HIGH

MEDIUM

LOW

## MONITOR SCHEDULE

- EVERY HOUR FOR 24 HOURS UNTIL 84% CUMULATIVE FAILURE.
- EVERY HOUR FOR THE FIRST 24 HOURS
- EVERY HOUR FOR 16 HOURS PER DAY UNTIL 168 TEST HOURS ARE ACCUMULATED
- EVERY 2 HOURS PER WORKDAY UNTIL 84% CUMULATIVE FAILURE
- EVERY 2 HOURS PER WORKDAY UNTIL 168 TEST HOURS ARE ACCUMULATED.
- EVERY 2.5 HOURS PER WORKDAY UNTIL 84% CUMULATIVE FAILURE.

## MONITORED PARAMETERS

|                       |                                       |
|-----------------------|---------------------------------------|
| FORWARD VOLTAGE       | ( $V_F$ ) AT 1Ma                      |
|                       | ( $V_F$ ) AT 10Ma                     |
| BREAKDOWN VOLTAGE     | ( $V_B$ ) AT 1Ma                      |
|                       | ( $V_B$ ) AT 10Ma                     |
|                       | ( $V_B$ ) AT 50Ma                     |
|                       | ( $V_B$ ) AT 100Ma                    |
| LEAKAGE CURRENT       | ( $I_L$ ) MEASURED AT .5 $V_B$ (10uA) |
| BASEPLATE TEMPERATURE | ( $T_{BP}$ )                          |
| INPUT CURRENT         | ( $I_{IN}$ )                          |
| INPUT VOLTAGE         | ( $V_{IN}$ )                          |
| D.C. POWER INPUT      | ( $P_{IN}$ )                          |
| TIME OF MEASUREMENT   | (HRS)                                 |

FIGURE 18.

## 6.0 Start-up Description

Device scheduled for stress testing are grouped according to the measured thermal resistance in order to accommodate previously noted thermal and electrical stress criteria.

The diodes are placed into individual diode holders and installed into the test fixture. Initial in-system measurements are taken at room temperature ( $\sim 25^{\circ}\text{C}$ ) and include the forward and reverse voltage at the noted current levels and the leakage current ( $I_L$ ). The leakage current is measured at fifty percent of the reverse breakdown voltage as measured at a 10ua current level. At this time the baseplate temperature is brought to the predetermined level and allowed to stabilize. With a maximum base plate temperature of  $150^{\circ}\text{C}$ , no operating lifetime is used up during the time period needed to finalize the start up sequence.

The above voltage and leakage current measurements are repeated once the baseplate temperature has stabilized. As anticipated, the high temperature measurements differ in that they are generally higher than the room temperature values.

Individually, the diodes are then biased in the reverse direction until the required level of DC power dissipation is reached via coarse and fine current adjustments.

Once the proper power level is set the power is turned off until all diodes have been adjusted in a like manner. Following completion of the initial bias adjustments the power to all diodes is turned on. The diodes are rechecked for the correct power level and readjusted as required.

Prior to powering up the diodes the input current and voltage trip points are set for each diode and the time on the hour meter is recorded for each diode test circuit.

The above procedure will greatly minimize temperature related increases in the thermal resistance. Data analysis at the conclusion of the accelerated stressing indicated a strong correlation between temperature, time and thermal resistance. A major deficiency of the current stress test configuration is the inability to measure the thermal resistance, which during the concluded tests seemed to change substantially. A recent paper on silicon IMPATT diode life tests<sup>(8)</sup> defined changes in the reverse bias voltage at 200 mA indicative of an increase in thermal resistance. If the change exceeded  $0.5^{\circ}$  C/W over the previous value, new bias conditions were calculated from the new value of thermal resistance. Verification of these observations with GaAs IMPATT diodes needs to be established in subsequent reliability studies.

The following example will serve as an illustration of how the correct stress test conditions were derived.

EXAMPLE:

DIODE TYPE: Varian, H-L Grown Junction

Serial No.: 25 Lot No.: 3717

RF Measurements:

$$P_{IN} = 10.93 \text{ W}$$

$$P_D = 8.74 \text{ W}$$

$$P_O = 2.19 \text{ W}$$

$$I_O = 389 \text{ mA}$$

$$V_O = 28.1 \text{ V}$$

$$\eta = 20\%$$

Thermal Resistance: 21.6 C/W

Correction Factor :  $4.0^{\circ}$  C/W

Total  $\theta_{TH}$ (total) :  $25.6^{\circ}$  C/W

Maximum DC power to be converted to heat during testing is 90% of  $P_D$ , or 7.87W, this value will serve as an upper limit for the electrical stress point.

Diode Junction Test Temperature ( $T_J$ ) : 321°C

Base Plate Temperature ( $T_{BP}$ ): 125°C

$$T_J = T_{BP} + T_{PIN}$$

$$T_{PIN} = 321^\circ\text{C} - 125^\circ\text{C} = 196^\circ\text{C}$$

$$P_{IN} = \frac{T_{PIN}}{\Theta_{TH}(\text{total})} = \frac{196^\circ\text{C}}{25.6^\circ\text{C/W}}$$

$$P_{IN} = 7.66\text{W} \text{ (this value is below the upper limit of } .9P_D = 7.87\text{W)}$$

or

$$T_{PIN} = (I_{IN} \times V_{IN}) \Theta_{TH}(\text{TOTAL})$$

Thus, the input current is adjusted until the  $P_{IN}$  value is reached at the given baseplate temperature.

# MONITORED STRESS TEST DATA (SAMPLE)



### ACCELERATED D.C. STRESS TEST DATA

TEST FIXTURE PARASITIC  $\theta_{TH} (^{\circ}C/W)$  44 PAGE 1  
 LOT # 3717 VSK9250AD DEVICE  $\theta_{TH} (^{\circ}C/W)$  21.6  
 POSITION 8 DIODE S/N 25 50% VB @ 10VA 7V TOTAL  $\theta_{TH} (^{\circ}C/W)$  25.6 VBIAS 34.1 IBIAS 224  
 BASEPLATE TEMP 125  $^{\circ}C$  P<sub>IN</sub> TEMP 196  $^{\circ}C$  REQUIRED JUNCTION TEMP. 321  $^{\circ}C$  ACTUAL P<sub>IN</sub> (W) 7.65  
 (T<sub>PIN</sub> = T<sub>J</sub> - T<sub>BP</sub>) THEORETICAL P<sub>IN</sub> (W) 7.65

|          | HOURLY METER TIME | DATE   | DATA TIME | V <sub>F</sub> 1 MA | V <sub>F</sub> 10 MA | V <sub>B</sub> 1 MA | V <sub>B</sub> 10 MA | V <sub>B</sub> 50 MA | V <sub>B</sub> 100 MA | I <sub>L</sub> @ 7V 50%VB 10VA | INITIAL | MEASURED BASEPLATE TEMP (°C) | I <sub>IN</sub> | V <sub>IN</sub> | P <sub>IN</sub> |
|----------|-------------------|--------|-----------|---------------------|----------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|---------|------------------------------|-----------------|-----------------|-----------------|
| SET UP   | 381.75            | 5/6/83 |           | 1.16                | 1.30                 | 15.94               | 16.38                | 17.48                | 19.15                 | 4NA                            | Comp    | 25                           | 0               | 0               | 0               |
| START UP | 383.6             | 5/9/83 | 10 AM     | .90                 | 1.00                 | 20.4                | 20.8                 | 22.3                 | 24.6                  | 20NA                           | Comp    | 130                          | .223            | 34.2            | 7.69            |
|          | 384.45            | 5/9/83 | 11 AM     | .89                 | 1.00                 | 20.5                | 20.8                 | 22.3                 | 24.6                  | 17NA                           | Comp    | 130                          | .223            | 34.1            | 7.61            |
|          | 385.5             |        | NOON      | .89                 | 1.01                 | 20.4                | 20.8                 | 22.3                 | 24.7                  | 20NA                           | PL      | 129                          | .225            | 34.1            | 7.68            |
|          | 386.5             |        | 1 PM      | .90                 | 1.01                 | 20.3                | 20.7                 | 22.2                 | 24.6                  | 20NA                           | Comp    | 126                          | .225            | 34.1            | 7.68            |
|          | 387.4             |        | 2 PM      | .90                 | 1.01                 | 20.4                | 20.8                 | 22.3                 | 24.8                  | 24NA                           | PL      | 130                          | .224            | 34.2            | 7.67            |
|          | 388.4             |        | 3 PM      | .90                 | 1.01                 | 20.3                | 20.7                 | 22.2                 | 24.6                  | 23NA                           | Comp    | 126                          | .225            | 34.1            | 7.68            |
|          | 389.4             |        | 4 PM      | .89                 | 1.02                 | 20.3                | 20.7                 | 22.2                 | 24.6                  | 24NA                           | PL      | 129                          | .225            | 34.2            | 7.70            |
|          | 390.4             |        | 5 PM      | .90                 | 1.02                 | 20.3                | 20.7                 | 22.2                 | 24.6                  | 26NA                           | mw      | 128                          | .224            | 34.4            | 7.69            |
|          | 391.3             |        | 6 PM      | .91                 | 1.03                 | 20.2                | 20.6                 | 22.1                 | 24.4                  | 22NA                           | mw      | 124                          | .225            | 34.4            | 7.73            |
|          | 392.3             |        | 7 PM      | .90                 | 1.02                 | 20.4                | 20.8                 | 22.3                 | 24.6                  | 24NA                           | mw      | 129                          | .224            | 34.2            | 7.67            |
|          | 393.3             |        | 8 PM      | .91                 | 1.02                 | 20.2                | 20.6                 | 22.1                 | 24.5                  | 22NA                           | mw      | 125                          | .225            | 34.2            | 7.70            |
|          | 394.35            |        | 9 PM      | .91                 | 1.02                 | 20.2                | 20.6                 | 22.2                 | 24.5                  | 31NA                           | mw      | 126                          | .223            | 34.4            | 7.66            |
|          | 395.35            |        | 10 PM     | .92                 | 1.03                 | 20.1                | 20.5                 | 22.1                 | 24.5                  | 39NA                           | mw      | 125                          | .225            | 34.2            | 7.70            |
|          | 396.35            |        | 11 PM     | .91                 | 1.02                 | 20.2                | 20.6                 | 22.2                 | 24.5                  | 23NA                           | mw      | 126                          | .224            | 34.2            | 7.67            |
|          | 397.25            |        | 12 AM     | .92                 | 1.03                 | 20.2                | 20.6                 | 22.2                 | 24.6                  | 36NA                           | PL      | 127                          | .224            | 34.2            | 7.67            |

### ACCELERATED D.C. STRESS TEST DATA

TEST FIXTURE PARASITIC  $\theta_{TH} (^{\circ}C/W)$  44 PAGE 2  
 LOT # 3717 VSK9250AD DEVICE  $\theta_{TH} (^{\circ}C/W)$  21.6  
 POSITION 8 DIODE S/N 25 50% VB @ 10VA 7V TOTAL  $\theta_{TH} (^{\circ}C/W)$  25.6 VBIAS 34.1 IBIAS 224  
 BASEPLATE TEMP 125  $^{\circ}C$  P<sub>IN</sub> TEMP 196  $^{\circ}C$  REQUIRED JUNCTION TEMP. 321  $^{\circ}C$  ACTUAL P<sub>IN</sub> (W) 7.65  
 (T<sub>PIN</sub> = T<sub>J</sub> - T<sub>BP</sub>) THEORETICAL P<sub>IN</sub> (W) 7.65

|          | HOURLY METER TIME | DATE    | DATA TIME | V <sub>F</sub> 1 MA | V <sub>F</sub> 10 MA | V <sub>B</sub> 1 MA | V <sub>B</sub> 10 MA | V <sub>B</sub> 50 MA | V <sub>B</sub> 100 MA | I <sub>L</sub> @ 7V 50%VB 10VA | INITIAL | MEASURED BASEPLATE TEMP (°C) | I <sub>IN</sub> | V <sub>IN</sub> | P <sub>IN</sub> |
|----------|-------------------|---------|-----------|---------------------|----------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|---------|------------------------------|-----------------|-----------------|-----------------|
| SET UP   | 381.75            | 5/6/83  |           | 1.16                | 1.30                 | 15.94               | 16.38                | 17.48                | 19.15                 | 4NA                            | Comp    | 25                           | 0               | 0               | 0               |
| START UP | 383.6             | 5/9/83  | 10 AM     | .90                 | 1.00                 | 20.4                | 20.8                 | 22.3                 | 24.6                  | 20NA                           | Comp    | 130                          | .223            | 34.2            | 7.69            |
|          | 398.2             | 5/10/83 | 1 AM      | .91                 | 1.02                 | 20.3                | 20.7                 | 22.3                 | 24.6                  | 33NA                           | PL      | 128                          | .224            | 34.4            | 7.69            |
|          | 399.2             |         | 2 AM      | .91                 | 1.02                 | 20.2                | 20.7                 | 22.2                 | 24.5                  | 33NA                           | PL      | 127                          | .224            | 34.4            | 7.69            |
|          | 400.15            |         | 3 AM      | .92                 | 1.03                 | 20.2                | 20.6                 | 22.0                 | 24.5                  | 33NA                           | PL      | 125                          | .225            | 34.2            | 7.70            |
|          | 401.15            |         | 4 AM      | .92                 | 1.03                 | 20.2                | 20.6                 | 22.2                 | 24.6                  | 34NA                           | PL      | 125                          | .224            | 34.2            | 7.67            |
|          | 402.15            |         | 5 AM      | .92                 | 1.02                 | 20.4                | 20.9                 | 22.4                 | 24.8                  | 34NA                           | PL      | 124                          | .225            | 34.2            | 7.70            |
|          | 403.1             |         | 6 AM      | .92                 | 1.03                 | 20.3                | 20.6                 | 22.2                 | 24.6                  | 33NA                           | PL      | 127                          | .223            | 34.4            | 7.66            |
|          | 404.1             |         | 7 AM      | .92                 | 1.01                 | 20.4                | 20.8                 | 22.4                 | 24.8                  | 44NA                           | PL      | 129                          | .222            | 34.5            | 7.65            |
|          | 405.1             |         | 8 AM      | .91                 | 1.02                 | 20.4                | 20.8                 | 22.3                 | 24.8                  | 33NA                           | Comp    | 128                          | .222            | 34.5            | 7.65            |
|          | 406.1             |         | 9 AM      | .93                 | 1.03                 | 20.4                | 20.9                 | 22.5                 | 24.8                  | 34NA                           | PL      | 125                          | .222            | 34.5            | 7.65            |
|          | 406.95            |         | 10 AM     | .92                 | 1.03                 | 20.3                | 20.8                 | 22.3                 | 24.8                  | 36NA                           | Comp    | 127                          | .222            | 34.5            | 7.65            |
|          | 408.0             |         | 11 AM     | .92                 | 1.03                 | 20.2                | 20.6                 | 22.2                 | 24.6                  | 32NA                           | PL      | 124                          | .222            | 34.5            | 7.65            |
|          | 409.0             |         | NOON      | .92                 | 1.02                 | 20.4                | 20.8                 | 22.4                 | 24.8                  | 34NA                           | PL      | 129                          | .222            | 34.5            | 7.65            |
|          | 410.0             |         | 1 PM      | .91                 | 1.02                 | 20.3                | 20.6                 | 22.2                 | 24.6                  | 31NA                           | Comp    | 125                          | .222            | 34.5            | 7.65            |
|          | 410.95            |         | 2 PM      | .91                 | 1.02                 | 20.3                | 20.7                 | 22.3                 | 24.8                  | 42NA                           | Comp    | 128                          | .222            | 34.5            | 7.65            |
|          | 411.9             |         | 3 PM      | .92                 | 1.03                 | 20.2                | 20.6                 | 22.2                 | 24.6                  | 42NA                           | PL      | 126                          | .222            | 34.5            | 7.65            |
|          | 413.0             | 5/10/83 | 4 PM      | .91                 | 1.02                 | 20.4                | 20.6                 | 22.3                 | 24.8                  | 48NA                           | PL      | 126                          | .220            | 34.6            | 7.60            |
|          | 413.9             |         | 5 PM      | .92                 | 1.02                 | 20.2                | 20.6                 | 22.2                 | 24.7                  | 41NA                           | mw      | 126                          | .221            | 34.6            | 7.64            |
|          | 414.9             |         | 6 PM      | .92                 | 1.02                 | 20.2                | 20.6                 | 22.2                 | 24.7                  | 45NA                           | mw      | 125                          | .220            | 34.6            | 7.60            |
|          | 415.9             |         | 7 PM      | .92                 | 1.02                 | 20.2                | 20.6                 | 22.2                 | 24.7                  | 43NA                           | mw      | 125                          | .221            | 34.5            | 7.62            |
|          | 416.85            |         | 8 PM      | .92                 | 1.02                 | 20.3                | 20.7                 | 22.3                 | 24.8                  | 44NA                           | mw      | 127                          | .220            | 34.6            | 7.61            |
|          | 417.85            |         | 9 PM      | .91                 | 1.02                 | 20.3                | 20.7                 | 22.3                 | 24.8                  | 42NA                           | mw      | 124                          | .220            | 34.6            | 7.61            |
|          | 418.8             |         | 10 PM     | .92                 | 1.02                 | 20.3                | 20.7                 | 22.3                 | 24.8                  | 42NA                           | mw      | 126                          | .219            | 34.7            | 7.59            |
|          | 419.8             |         | 11 PM     | .92                 | 1.02                 | 20.3                | 20.7                 | 22.3                 | 24.8                  | 42NA                           | mw      | 126                          | .219            | 34.6            | 7.57            |
|          | 427.9             | 5/11/83 | 7 AM      | .23                 | .49                  | .30                 | 2.30                 | 4.52                 | 5.04                  |                                | Comp    |                              |                 |                 |                 |

**Failure Mode:**

Test Circuit was tripped at indicated time.  
 Failure was defined as a short, as power was removed just prior to shorting.

FIGURE 19.

#### IV. THERMALLY ACCELERATED CONSTANT DC STRESS TESTS

##### 1.0 Introduction

In order to achieve the projected outputs of the combined accelerated stress tests, a minimum of three thermal stress levels are required for each device type. The obtained data is used to generate an Arrhenius reaction rate plot for both the Schottky barrier and grown junction diodes from which the activation energies can be calculated and lifetimes extrapolated to the actual operating junction temperature can be projected with reasonable accuracy.

A summary of the number of tests carried out and diodes stressed is shown. Also shown is a device fabrication and procurement history.

##### Projected Outputs

- Failure rate - early failure data
- Log-normal data and standard deviation (cumulative failure vs. time to failure)
- Validation of log-normal data
- Median time to failure for each accelerated stress test
- Definition of failure mechanism
- Activation energy and operating lifetime projection from Arrhenius reaction rate plots.
- Optimized stress test temperature recommendation
- Identification of process and packaging modifications
- Burn-in temperature and time for early failure screening





DIODE TYPES

- MODIFIED READ PROFILE (LHL) SCHOTTKY BARRIER (M/S) FABRICATED AT LNR
- HIGH LOW (HL) WITH GROWN P-LAYER (G/J) PROCURED FROM VARIAN
- A. SCHOTTKY-BARRIER (M/S) DIODES FABRICATED AT LNR FROM SINGLE DRIFT L-H-L EPITAXIAL GAAs GROWN BY VPE.

|               | STANDARD | EXPERIMENTAL |
|---------------|----------|--------------|
| FABRICATED    | 275      | 168          |
| CHARACTERIZED | 226      | 126          |
| STRESS TESTED | 105      | 20           |

- B. GROWN JUNCTION (P/N) DIODES PROCURED FROM VARIAN WERE FABRICATED FROM P<sub>+</sub>-H-L PROFILED WAFERS GROWN BY MBE.

|               |    |
|---------------|----|
| PROCURED      | 80 |
| CHARACTERIZED | 80 |
| STRESS TESTED | 79 |

C. SPECIFICATIONS:

|                           |          |
|---------------------------|----------|
| FREQUENCY (GHz):          | 19 TO 21 |
| POWER OUTPUT(W):          | ≥ 1.0    |
| EFFICIENCY (%) :          | ≥ 16     |
| THERMAL RESISTANCE(°C/W): | ≤ 30     |

NUMBER OF STRESS TESTS

- FOUR AT A HIGH TEMPERATURE ≥ 340°C (INCLUDING 2 CALIBRATION TESTS)
- TWO AT A MEDIAN TEMPERATURE OF 321°C
- TWO AT A LOW TEMPERATURE ≥ 299°C

## 2.0 Failure Criteria

In order to obtain a comprehensive data base, a certain flexibility in the failure criteria was maintained during stress testing. Thus, certain observations could be made of diode behaviors while under test, e.g. the leakage current for example, would increase substantially and then stabilize, in some case would decrease again. Previous 20 GHz oscillator measurements clearly indicated that substantial increases in leakage current did not indicate a sufficient decrease in RF performance to be considered a failure. However, if the onset of a substantial change in any of the monitored parameters ultimately resulted in a failure within five hours, the time of the onset was considered the failure time. Also, devices which showed little change as a whole, other than the level of DC power being dissipated where terminated, to enable post test thermal resistance and power measurements. The measured parameters ultimately confirmed the diode as having failed because of increases in thermal resistance and/or decreased RF performance. Thus, for any subsequent reliability studies the failure criteria can be defined more appropriately.

For the concluded reliability assessment the failure criteria used to define 20 GHz IMPATT diode failure is listed.

## FAILURE CRITERIA

- CRITERIA A: CATASTROPHIC FAILURE WITH THE DIODE EITHER ELECTRICALLY OPEN OR SHORT
- CRITERIA B: TRIPPING STRESS TEST CIRCUIT WITH POINTS SET 5 VOLTS AND 200 MA ABOVE THE VOLTAGE AND CURRENT INPUTS RESPECTIVELY.
- CRITERIA C: THE ACTUAL ONSET OF DEGRADATION IN ANY OF THE MONITORED DC CHARACTERISTICS RESULTING IN ANY OF THE ABOVE FAILURE MODES WITHIN FIVE HOURS.
- CRITERIA D: TERMINATION OF STRESS TESTING WHEN NONE OF THE ABOVE CRITERIA OCCURRED BUT SIGNIFICANT CHANGES IN LEAKAGE CURRENT AND INPUT POWER (DC POWER DISSIPATED) WERE OBSERVED.

### 3.0 High Temperature Accelerated Constant DC Stress Test

To check the operation and calibrate the burn in system, two mixed lots of Schottky barrier and grown junction diodes were used. The results of these forty six stressed diodes were not used for the statistical analysis and lifetime predictions.

Diodes were grouped according to the measured thermal resistance in order to achieve the previously described thermal and electrical stress levels. Following satisfactory calibration and operational check of the burn in rack, having made certain indicated improvements and corrections, the system was readied for the first high temperature stress test. The high temperature test was selected to provide maximum data in the shortest possible time.

#### 3.1 Test Conditions

- LNR Schottky Barrier Diodes  
Junction Stress Temperature: 345°C  
Baseplate Temperature : 140°C (constant)
- Varian Grown Junction Diodes  
Junction Stress Temperature: 340°C  
Baseplate Temperature : 150°C (constant)

#### 3.2 Test DATA Summary

The failure modes for both types of diodes have been tabulated according to the established criteria.

To generate the required Cumulative Failure (%) vs. Log Time to Failure (hrs.) plot the following calculations were used.

$$D'Agostino's \text{ Test } (D) = \frac{T_I}{\sqrt{N^3 SS}}$$

where,  $SS = \text{Sum of Squares}$   
 $= \sum X_I^2 - \frac{(\sum X_I)^2}{N}$

$$T_I = \text{Constant}$$

$$T_I = \left(I - \frac{N+1}{2}\right) X_I$$

$I = \text{Sequential Rank}$

$N = \text{Number of devices tested}$

$$X_I = L_n t_I$$

$t_I = \text{The individual failure times}$   
 $(I = 1, 2, \dots, N)$

At 90% confidence,

$$\text{IF } D_{\min} \leq D_{\text{data}} \leq D_{\max}$$

Then the assumption of lognormality is valid where:

$D_{\min}$  is taken from the table, "critical values of D'Agostino's "D" for normality testing, based on "N" and desired degree of confidence.

$D_{\max}$  is taken from the table "critical values of D'agostino's "D" for normality testing", based on "N" and desired degree of confidence.

Cumulative Failures (Percent)

$$C.F. = \frac{2P-1}{2N} \times 100$$

where,  $P$  = number of failures  
 $N$  = number in test sample

Standard Deviation

$$\sigma = L_n \left( \frac{t_{50}}{t_{16}} \right) = L_n \left( \frac{t_{84}}{t_{50}} \right)$$

where,  $t$  = time to failure in hours

Median Time to Failure (Hrs.)

$$\tilde{T}_M = \bar{X} = L_n (t_{50}) = \frac{\sum X_I}{N}$$

where,  $T_I$  = time to failure of  $I^{\text{TH}}$  diode ( $I=1,2,\dots$ )  
 $T_{CF}$  is obtained from the lognormal plot  
 $X_I = L_n T_I$   
 $N$  = Number of Diodes

### 3.3 Logarithmic - Normality Validation

To test the hypothesis of normality of the log arithmetic lifetime data the D'Agastinos test<sup>(9)</sup> is imposed. The result indicates whether or not at 10 percent significance (90 percent confidence) the hypothesis that the logarithmic lifetime data is normally distributed is to be or not to be rejected. In case the hypothesis is correct and not rejected, the logarithmic data is considered to be "normal enough" for the Student -t analysis.

### 3.4 Initial and Final DC and RF Data

The initial DC data shown is taken after the burn-in system has stabilized at the required baseplate temperature. Consequently, the data of some diodes appear to indicate defective devices, which is, however, the result of the initial impact of both thermal and electrical stressing. In some cases the combined stress levels resulted in instant failures. Furthermore, the final RF power data shown have in some cases been noted as:

- Short/open - implying that the diode shorted/  
opened during the final oscillator  
measurement.
- N/A - indicates that no oscillation could  
be observed

INITIAL AND FINAL D.C. AND RF DATA

JUNCTION STRESS TEMPERATURE  
 $T_J = T_H = 340^\circ\text{C}$   
 BASEPLATE TEMPERATURE  
 $T_{BP} = 150^\circ\text{C}$  OR AS NOTED \*

GROWN JUNCTION DIODES

| DIODE #  | INPUT CURRENT |           | INPUT VOLTAGE |           | LEAKAGE CURRENT |         | BREAKDOWN VOLTAGE |                 | INPUT POWER (W) |       | RF POWER (W) |       | ACCUMULATED TEST TIME |        |
|----------|---------------|-----------|---------------|-----------|-----------------|---------|-------------------|-----------------|-----------------|-------|--------------|-------|-----------------------|--------|
|          | INITIAL (A)   | FINAL (A) | INITIAL (V)   | FINAL (V) | PRE STRESS TEST | INITIAL | FINAL             | PRE STRESS TEST | INITIAL         | FINAL | INITIAL      | FINAL |                       |        |
| $T_{BP}$ | 150°C         | 150°C     | 150°C         | 150°C     | 25°C            | 150°C   | 150°C             | 150°C           | 150°C           | 150°C | 25°C         | 25°C  |                       |        |
| 3664/19  | .225          | NA        | 34.79         | NA        | 1NA             | NA      | NA                | .09             | NA              | 7.83  | NA           | 1.95  | NA                    | 0      |
| 3705/33  | .186          | .153      | 38.07         | 39.93     | 8NA             | 550NA   | 7.6µA             | 22.4            | 22.5            | 7.08  | 6.11         | 1.11  | NA                    | 18.4   |
| 3664/17  | .199          | .128      | 35.88         | 41.2      | 3NA             | 188NA   | 1662NA            | 21.4            | 22.1            | 7.14  | 5.27         | 1.93  | NA                    | 109.8  |
| 3664/31  | .197          | .NA       | 34.79         | NA        | 1NA             | NA      | NA                | NA              | NA              | 6.85  | NA           | 1.57  | NA                    | 0      |
| 3664/32  | .170          | .168      | 36.32         | 36.2      | 4NA             | 69NA    | 87NA              | 22.3            | 22.2            | 6.17  | 6.08         | 1.39  | NA                    | 14.05  |
| 3664/35  | .176          | NA        | 37.96         | NA        | 2NA             | NA      | NA                | 2.28            | NA              | 6.68  | NA           | 1.51  | NA                    | 0      |
| 3705/18  | .186          | .131      | 36.21         | 40.4      | 3NA             | 198NA   | 877NA             | 22.4            | 23.3            | 6.74  | 5.29         | 1.73  | NA                    | 108.7  |
| 3664/24  | .197          | .171      | 35.77         | 38.0      | 20NA            | 719NA   | 642NA             | 22.0            | 22.4            | 7.05  | 6.50         | 1.23  | NA                    | 47.6   |
| 3664/36  | NA            | NA        | NA            | NA        | 5NA             | NA      | NA                | NA              | NA              | NA    | NA           | 1.18  | NA                    | 0      |
| 3664/16  | .196          | .161      | 37.20         | 39.8      | 3NA             | 152NA   | 2.1µA             | 22.5            | 23.1            | 7.29  | 6.41         | 1.08  | NA                    | 47.4   |
| 3664/37  | .198          | NA        | 35.12         | NA        | 1NA             | 1NA     | NA                | 28.2            | NA              | 6.95  | NA           | 1.17  | NA                    | 0      |
| 3705/1   | .177          | .166      | 36.32         | 36.9      | 1NA             | 166NA   | 1.7µA             | 22.4            | 22.4            | 6.43  | 6.13         | 1.17  | NA                    | 13.4   |
| 3705/3   | .198          | .124      | 38.07         | 42.78     | 2NA             | 103NA   | 1.8µA             | 22.2            | 23.4            | 7.54  | 5.30         | 1.67  | No.050                | 46.3   |
| 3705/7   | .193          | .138      | 36.76         | 40.70     | 2NA             | 1.2µA   | 3.4µA             | 21.2            | 21.8            | 7.20  | 5.62         | 1.21  | NA                    | 33.8   |
| 3705/8   | .193          | NA        | 37.52         | NA        | 4NA             | NA      | NA                | 1.25            | NA              | 7.24  | NA           | 1.11  | NA                    | 0      |
| 3705/22  | .184          | .131      | 36.1          | 40.4      | 3NA             | 107NA   | 472NA             | 22.5            | 23.0            | 6.64  | 5.29         | 1.56  | NA                    | 200.65 |
| 3705/17  | .178          | .181      | 36.21         | 35.6      | 1NA             | 92 NA   | 89 NA             | 22.6            | 22.7            | 6.45  | 6.44         | 1.14  | No.050                | 1.0    |
| 3705/4   | .189          | .117      | 37.63         | 42.4      | 3NA             | 102NA   | 972NA             | 22.4            | 23.1            | 7.11  | 4.96         | 1.00  | No.050                | 200.5  |
| 3664/18  | .205          | .159      | 35.88         | 38.8      | 2NA             | 106NA   | 6.8NA             | 21.5            | 21.8            | 7.36  | 6.17         | 1.24  | No.050                | 25.9   |
| 3705-32  | .193          | .120      | 34.79         | 40.7      | 11NA            | 202NA   | 1119NA            | 20.4            | 21.3            | 6.71  | 4.88         | 1.47  | No.050                | 151.7  |

FIGURE 22.



INITIAL AND FINAL D.C. AND RF DATA

JUNCTION STRESS TEMPERATURE  
 $T_J = T_H = 345^{\circ}\text{C}$   
 BASEPLATE TEMPERATURE  
 $T_{BP} = 140^{\circ}\text{C}$  OR AS NOTED

SCHOTTKY BARRIER

| DIODE #  | INPUT CURRENT (A) |       | INPUT VOLTAGE (V) |       | LEAKAGE CURRENT (A) |              | PRE STRESS TEST |       | BREAKDOWN VOLTAGE (V) |       | INPUT POWER (W) |       | RF POWER (W) |       | ACCUMULATED TEST TIME |
|----------|-------------------|-------|-------------------|-------|---------------------|--------------|-----------------|-------|-----------------------|-------|-----------------|-------|--------------|-------|-----------------------|
|          | INITIAL           | FINAL | INITIAL           | FINAL | INITIAL             | FINAL        | INITIAL         | FINAL | INITIAL               | FINAL | INITIAL         | FINAL | INITIAL      | FINAL |                       |
| $T_{BP}$ | 140°C             | 140°C | 140°C             | 140°C | 25°C                | 140°C        | 25°C            | 140°C | 140°C                 | 140°C | 140°C           | 140°C | 25°C         | 25°C  |                       |
| 1254M    | .266              | .213  | 20.02             | 25.60 | 2.1µA               | 15.8µA       | 67.5µA          | 11.54 | 13.28                 | 13.56 | 5.33            | 5.45  | .53          | SHORT | 70.2                  |
| 1264M    | .184              | .146  | 29.54             | 32.93 | 1.75µA              | 6.7µA        | 16.4µA          | 13.08 | 17.05                 | 17.02 | 5.44            | 4.81  | 1.14         | NA    | 79.3                  |
| 1220G    | .178              | .167  | 34.13             | 35.01 | .65µA               | 2.2µA        | 35.8µA          | 17.38 | 22.45                 | 20.73 | 6.08            | 5.85  | 1.32         | NA    | 48.1                  |
| 1223G    | .205              | .135  | 30.30             | 35.45 | .65µA               | 1.6µA        | 10.2µA          | 15.33 | 19.58                 | 22.25 | 6.21            | 4.79  | 1.59         | .44   | 54.8                  |
| 1229G    | .206              | .206  | 31.29             | 31.29 | 770nA               | 3.8µA        | 89.6µA          | 14.82 | 19.15                 | 19.07 | 6.45            | 6.45  | 2.05         | NA    | 10.6                  |
| 1231G    | .200              | .161  | 32.38             | 35.23 | 173nA               | 0.9µA        | 15.8µA          | 15.84 | 20.54                 | 21.76 | 6.48            | 5.67  | 1.86         | SHORT | 36                    |
| 1237G    | .183              | .129  | 31.29             | 35.56 | 600nA               | 4.0µA        | 20.3µA          | 15.65 | 20.10                 | 22.77 | 5.73            | 4.59  | 1.60         | NA    | 72.8                  |
| 1238G    | .205              | NA    | 30.00             | NA    | 1.1µA               | 11.4µA       | 8.8µA           | 15.13 | 19.08                 | 18.88 | 6.15            | NA    | 1.54         | NA    | 2.8                   |
| 1188G    | .212              | NA    | 28.88             | NA    | OUT OF RANGE        | 28.0µA       | NA              | 14.69 | 18.92                 | NA    | 6.09            | NA    | 1.38         | NA    | 45.6                  |
| 1180G    | .159              | NA    | 33.15             | NA    | 338nA               | 39.4µA       | NA              | 17.30 | 22.47                 | NA    | 5.27            | NA    | 1.60         | NA    | 48.8                  |
| 1177G    | .176              | NA    | 31.18             | NA    | 1.3µA               | 6.5µA        | NA              | 16.00 | 20.69                 | NA    | 5.49            | NA    | 1.50         | NA    | 147.8                 |
| 668G     | .326              | NA    | 20.90             | NA    | .6µA                | OUT OF RANGE | 108.5µA         | 11.06 | 0.25                  | 12.46 | 6.81            | NA    | 1.29         | NA    | 21.05                 |
| 680G     | .323              | .263  | 19.69             | 24.72 | 7.65µA              | OUT OF RANGE | NA              | 10.92 | 7.76                  | NA    | 6.36            | 6.50  | 1.04         | NA    | 12.3                  |
| 685G     | .265              | .201  | 22.65             | 28.12 | 1.4µA               | 7.1µA        | 16.7µA          | 11.30 | 12.65                 | 14.15 | 6.00            | 5.65  | 1.40         | .67   | 31.5                  |
| 362D     | .246              | .194  | 19.04             | 24.83 | .45µA               | 5.6µA        | NA              | 8.97  | 10.16                 | NA    | 4.68            | 4.82  | 1.14         | SHORT | 23.2                  |
| 366D     | .245              | .194  | 20.24             | 25.93 | 1.8µA               | 36.1µA       | 52.0µA          | 9.03  | 9.92                  | 8.26  | 4.96            | 5.03  | 1.23         | SHORT | 24.5                  |
| 1106B    | .223              | .275  | 28.77             | 30.41 | .85µA               | 1.8µA        | 141.9µA         | 13.68 | 18.09                 | 16.96 | 6.42            | 8.36  | 1.63         | NA    | 47.45                 |
| 1116B    | .322              | NA    | 22.21             | NA    | .55µA               | 4.4µA        | 165.0µA         | 11.25 | 13.45                 | 14.25 | 7.15            | NA    | .93          | .75   | 14.45                 |
| 470G     | .292              | .229  | 19.80             | 25.49 | .85µA               | 2.5µA        | 27.8µA          | 11.26 | 12.39                 | 12.06 | 5.78            | 5.84  | 1.20         | .65   | 69.35                 |
| 514G     | .261              | .203  | 21.77             | 27.57 | .65µA               | 4.0µA        | NA              | 11.27 | 12.47                 | NA    | 5.68            | 5.60  | 1.33         | SHORT | 43.4                  |

FIGURE 23.

### 3.5 High Temperature Stress Test Results

#### SCHOTTKY BARRIER

|   | EARLY FAILURE | W/O EARLY FAILURE |
|---|---------------|-------------------|
| NUMBER OF DEVICES (N) :                 | 20            | 19                |
| STANDARD DEVIATION ( $\sigma$ ) :       | 0.8           | 0.7               |
| MEDIAN TIME TO FAILURE ( $\gamma_M$ ) : | 35 HRS.       | 39 HRS.           |
| D'AGOSTINO TEST (VALID/FAILED) :        | VALID         | VALID             |

#### GROWN JUNCTION

|   |                           |         |
|---|---------------------------|---------|
| NUMBER OF DEVICES (N) :                 | 20                        | 13      |
| STANDARD DEVIATION ( $\sigma$ ) :       | 3.5                       | 0.95    |
| MEDIAN TIME TO FAILURE ( $\gamma_M$ ) : | 5 HRS.                    | 47 HRS. |
| D'AGOSTINO TEST (VALID/FAILED) :        | FAILED<br>(NOT LOGNORMAL) | VALID   |

OBSERVATION: The grown junction, n = 20 sample is not lognormal due to infant mortalities, therefor, on the Arrhenius plot, the point plotted for grown-junction, high temperature, n = 20 is not valid and cannot be used to determine the activation energy.

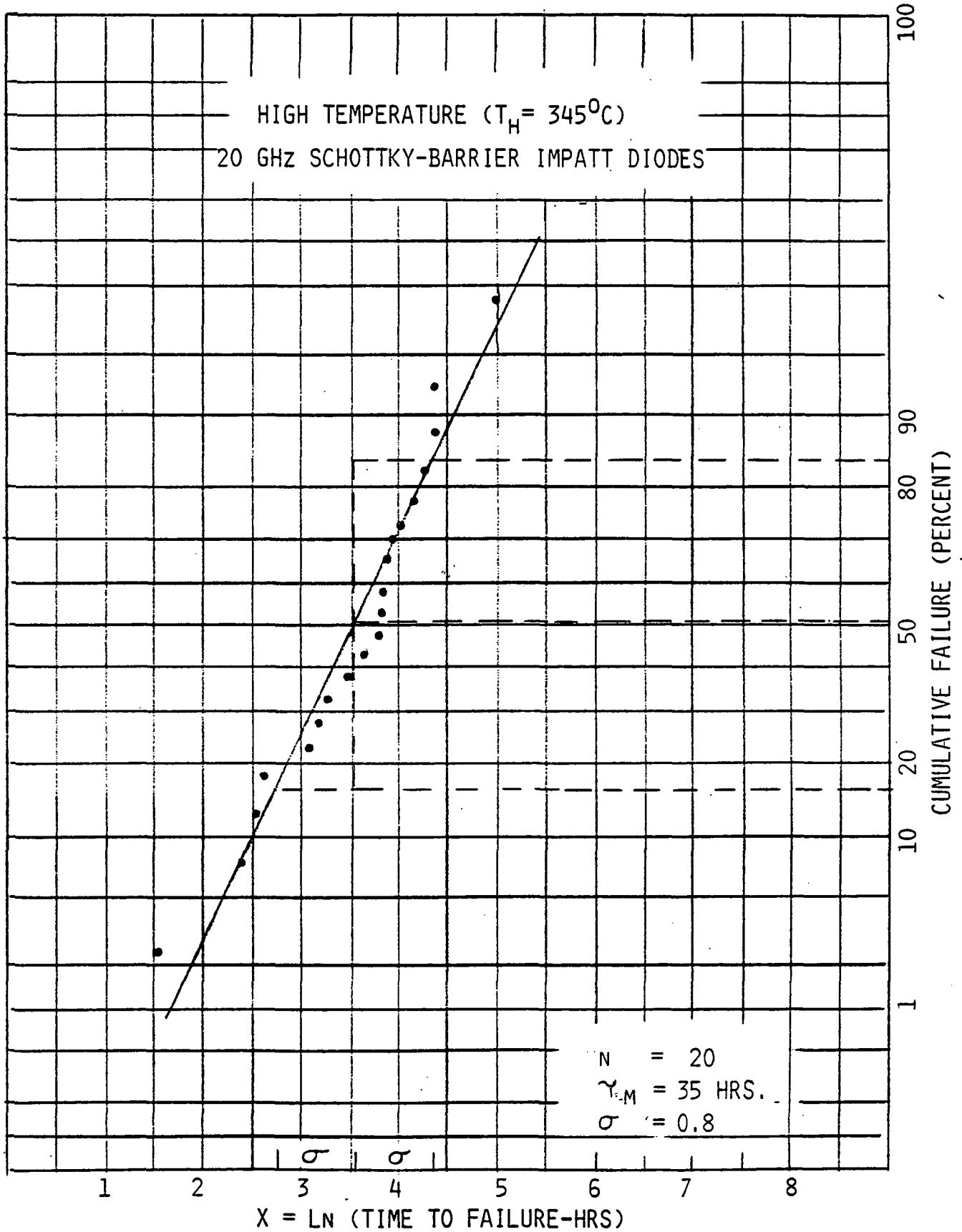


FIGURE 24.

DC ACCELERATED STRESS TEST DATA FOR  
 HIGH TEMPERATURE ( $T_H = 345^{\circ}\text{C}$ )  
 20 GHz SCHOTTKY-BARRIER IMPATT DIODES



| DEVICE S/N | $T_I$ (HRS.) | $X_I = LNT_I$ | CUMULATIVE<br>% FAILURES = $\frac{2I-1}{2N} \times 100\%$ |
|------------|--------------|---------------|---|
| 1238G      | 4.55         | 1.515         | 2.5   |
| 1229G      | 11.1         | 2.407         | 7.5   |
| 1116B      | 12.8         | 2.549         | 12.5  |
| 680G       | 13.6         | 2.610         | 17.5  |
| 668G       | 22.25        | 3.102         | 22.5  |
| 362D       | 24.5         | 3.199         | 27.5  |
| 366D       | 25.8         | 3.250         | 32.5  |
| 685G       | 32.8         | 3.490         | 37.5  |
| 1231G      | 38.5         | 3.651         | 42.5  |
| 514G       | 44.8         | 3.802         | 47.5  |
| 1188G      | 45.6         | 3.820         | 52.5  |
| 1106B      | 46.1         | 3.831         | 57.5  |
| 1180G      | 48.8         | 3.888         | 62.5  |
| 470G       | 48.8         | 3.888         | 67.5  |
| 1223G      | 55.6         | 4.018         | 72.5  |
| 1220G      | 65.8         | 4.187         | 77.5  |
| 1254M      | 70.7         | 4.258         | 82.5  |
| 1237G      | 80.2         | 4.385         | 87.5  |
| 1264M      | 80.7         | 4.391         | 92.5  |
| 1177G      | 147.8        | 4.996         | 97.5  |

N = 20

FIGURE 25.

B. 20 GHz IMPATT TRANSMITTER FOR  
COMMUNICATIONS SATELLITE

FINAL REPORT

NASA CR 174716

FEBRUARY, 1981

Prepared For:

NASA Lewis Research Center  
Cleveland, Ohio

CONTRACT NASA-NAS3-22491

## CONTENTS

- 1.0 INTRODUCTION
- 2.0 TECHNOLOGY ASSESSMENT
- 3.0 PARAMETRIC TRADEOFF ANALYSIS
- 4.0 PRELIMINARY DESIGN SPECIFICATION
- 5.0 SENSITIVITY ANALYSIS



1.0 INTRODUCTION







1.1 PROGRAM TASK/SCHEDULE OVERVIEW

The objective of the contract is to develop 20 GHz transmitter technology which will demonstrate the feasibility of providing efficient, reliable, lightweight IMPATT transmitters by the end of FY1982, (b) provide IMPATT devices and proof of concept model for breadboard amplifier circuit validation applicable for use in a flight qualified transmitter to be flown on a 20/30 GHz communication demonstration system in 1985 and, (c) provide on advanced data base for use in communications payload definitions and design studies.

In order to accomplish the above objective the contract is structured into twelve specific tasks as shown in the accompanying program task schedule.

- Task I is to generate a preliminary 20 GHz transmitter design including a technology assessment, parametric trade off analysis and sensitivity analysis.
- Task II is to develop an IMPATT device for use in the 20 GHz transmitter, and to design, fabricate and test breadboard assemblies of items required to verify task I design parameters.
- Task III is to generate a detailed development plan for implementing the transmitter design into a fully operational POC model.
- Task IV is to generate a design for the POC Model, including detailed test plan and procedures, proceeding from the task I design as updated during task II development.
- Task V is to fabricate and assemble 3 POC models\* and 100 IMPATT devices.
- Task VI is to test the POC models according to the procedures generated in task IV and conduct an analysis of test results.\*
- Task VII is to perform a reliability projection and lifetime expectancy of a flight model of the POC 20 GHz transmitter.\*
- Task VIII is to conduct a quality assurance program covering POC design, fabrication and test.\*
- Task IX is to assess the future growth prospects of IMPATT technology and combiner technology and to project capability which can be achieved in the 1987 timeframe.
- Task X is to generate and update a Work Plan identifying sub tasks to be accomplished in performing the contractual requirements.
- Task XI is to document performance under this contract effort via monthly, task and final reports.
- Task XII is to generate a Requirements Document and Development Plan for a flight demonstration transmitter system to support a 1985 launch.  
\*task performance subject to prior government authorization



SCOPE OF REPORT (TASK I)

- . 20 GHZ TRANSMITTER DESIGN
- .. TECHNOLOGY ASSESSMENT
  - IMMEDIATELY AVAILABLE
  - IN PROCESS OF DEVELOPMENT
  - CAN BE DEVELOPED
- .. PARAMETRIC TRADE OFF ANALYSIS
- .. PRELIMINARY TRANSMITTER DESIGN AND SPECIFICATION
  - PDR
- .. SENSITIVITY ANALYSIS
- .. TASK I REPORT



## 1.2 SCOPE OF REPORT (TASK I)

Task I of the contractual effort was to develop a preliminary design for a 20 GHz satellite transmitter utilizing technology which can be developed and incorporated in a proof-of-concept (POC) model. This preliminary design effort included specific subtasks which were each addressed and their outputs are included as part of this Task I Report.

The first subtask was a technology assessment whereby technology items required for the 20 GHz transmitter were identified and an assessment was made relative to current status. The outputs from this effort are included in section 2.0 of this report.

The second subtask involved a parametric trade-off analysis to determine, a) the optimum combination of IMPATT diode chip level and circuit level power combining, and resultant preferred IMPATT power amplifier configuration; b) the driver amplifier characteristics required to best meet the performance specifications of the transmitter. The outputs from this subtask are summarized in section 3.0 of the report.

Section 4.0 details the preliminary 20 GHz IMPATT transmitter design and specification, which was derived from the third subtask and subsequently presented at the Preliminary Design Review.

The last specified subtask, presented in section 5.0 of the report, consists of a sensitivity analysis, whereby assumed dispersions from nominal IMPATT diode characteristics were identified and the effect of these dispersions on transmitter performance described.



GENERAL REQUIREMENTS ON 20 GHZ IMPATT TRANSMITTER DESIGN

- . MEET ELECTRICAL/RF PROFORMANCE OF SOW
- . SPACE-QUALIFIABLE DESIGN UTILIZING 1982 TIME FRAME  
TECHNOLOGY
- . COMPATIBLE WITH SPACECRAFT DEPLOYMENT OF FULLY QUALIFIED  
FLIGHT UNIT BY 1985-90 TIME FRAME
- . MINIMUM SIZE, WEIGHT AND PRIME POWER DRAIN
- . MINIMUM COMPLEXITY AND PARTS COUNT FOR MAXIMUM RELIABILITY  
OVER 10 YEAR OPERATIONAL LIFE.
- . GRACEFUL DEGRADATION IN PERFORMANCE UNDER RANDOM DEVICE  
FAILURES
- . MINIMUM DEVICE JUNCTION TEMPERATURE FOR MAXIMUM RELIABILITY
- . COMPATIBLE WITH ANTENNA MOUNTING



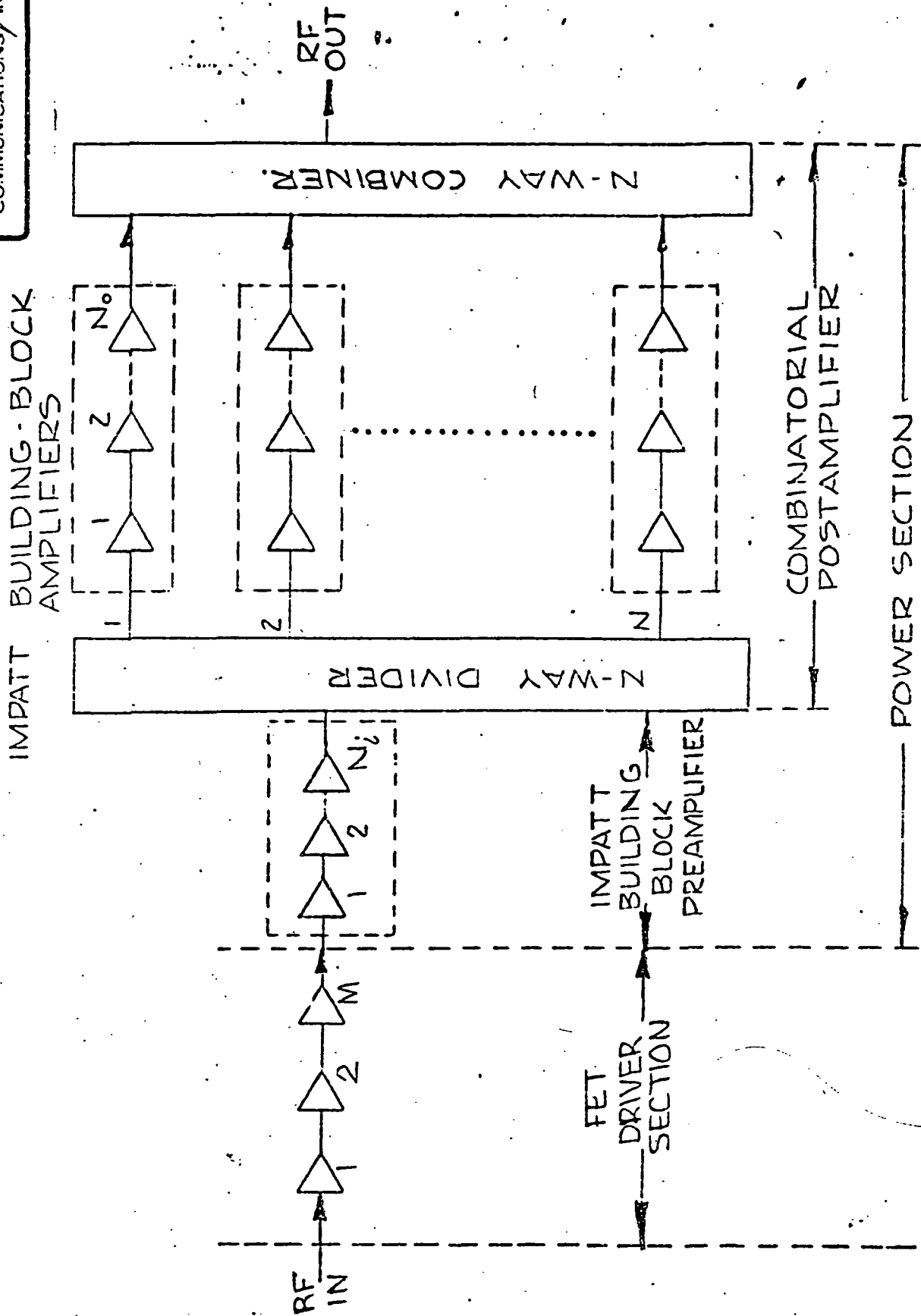
### 1.3 GENERAL REQUIREMENTS ON 20 GHz IMPATT TRANSMITTER DESIGN

The preliminary 20 GHz IMPATT Transmitter design presented in this report addresses each of the general requirements enumerated in the accompanying Table. The transmitter design utilizes technology which upon implementation, will demonstrate readiness for development of a POC model within the 1982 time frame and will provide an information base for flight hardware capable of deployment in a 1985-90 Demonstrational 30/20 GHz Satellite Communication System.

The transmitter design utilizes those devices necessary to amplify an angle modulated, single carrier downlink signal in the band 19.7 to 20.2 GHz, to a power level of  $\geq 20$  watts and meet all RF performance requirements specified. In so doing, size, weight and power drain requirements have been reduced to a minimum consistent with spacecraft demands.

Overall design complexity and number of parts have also been minimized, as has device junction temperature, to insure maximum transmitter reliability consistent with a 10 year operational life. Graceful degradation in performance under random device failure rather than complete loss of function is an integral part of the design to further enhance transmitter reliability.





FUNCTIONAL RF TOPOLOGY OF 20GHz IMPATT TRANSMITTER

#### 1.4 FUNCTIONAL RF TOPOLOGY OF 20 GHz IMPATT TRANSMITTER

The 20 GHz IMPATT transmitter RF assembly, in its most general form, consists of the cascaded combination of a FET driver section and an IMPATT power section. The FET driver section, in turn, comprises a cascade of low to medium power FET amplifier stages whereas the IMPATT power section consists of a multistage IMPATT preamplifier driving a combinatorial IMPATT postamplifier. The latter is configured as an array of identical multistage IMPATT "building blocks", paralleled between identical N-way power divider and combiner. In the most general case, the number of IMPATT amplifier stages comprising the preamplifier ( $N_i$ ) and postamplifier "building block" ( $N_o$ ) are different. The order(N) of power combination required is determined by the RF power capability of each "building block" which in turn determines how many paralleled "building blocks are required to provide the required RF power output(20W).



20 GHZ SOLID STATE TRANSMITTER-SPECIFIC DESIGN OBJECTIVES

PARAMETRIC

DESIGN OBJECTIVE (OVER PASSBAND)

|   |                                      |
|---|--------------------------------------|
| INPUT SIGNAL FORMAT                                 | ANGLE MODULATED, SINGLE CARRIER      |
| CENTER FREQUENCY                                    | 19.95 GHZ                            |
| RF PASSBAND (500 MHZ)                               | 19.7 TO 20.2 GHZ                     |
| SATURATED RF OUTPUT POWER (LOAD VSWR $\leq 1.3:1$ ) | 20 WATTS (MIN)                       |
| NOISE FIGURE  | 25 DB (MAX)                          |
| RF GAIN @ SATURATION                                | 30 DB <sup>+0</sup> <sub>-1</sub> DB |
| IN BAND OVERDRIVE SURVIVABILITY                     | 5 DB ABOVE NOMINAL INPUT LEVEL       |
| GAIN VARIATION                                      | $\pm 1$ DB (MAX)                     |
| GAIN SLOPE  | 0.15 DB/MHZ (MAX)                    |
| INPUT AND OUTPUT VSWR                               | 1.3:1 (MAX)                          |
| GROUP DELAY VARIATION                               | 0.5 NS P-P (MAX) OVER 50 MHZ SLOT    |
| AM/PM CONVERSION                                    | 5 $\pm 1^\circ$ /DB (MAX)            |
| PHASE LINEARITY                                     | 10 $^\circ$ P-P (MAX)                |
| HARMONIC RESPONSE (AT SATURATION)                   | 50 DB BELOW CARRIER                  |
| SPURIOUS RESPONSE (AT SATURATION)                   | 60 DB BELOW CARRIER                  |
| DC-RF EFFICIENCY                                    | 20% (MIN) - EXCLUDING POWER SUPPLIES |
| INTERFACE   | WR-42 WAVEGUIDE                      |
| BASEPLATE TEMPERATURE                               | 0 to 75 $^\circ$ C                   |





### 1.5 20 GHZ SOLID STATE TRANSMITTER-SPECIFIC DESIGN OBJECTIVES

The basic, gating design requirement on the subject 20 GHz transmitter is that it provides 20W (minimum) K-band RF power output over a 500 MHz bandwidth centered near 20 GHz with 20 percent DC bias/RF power added efficiency. (the latter excluding the efficiency degradation due to DC power conditioning components). Moreover, this transmitter must provide 30 dB power gain to a single, angle modulated (PM) carrier, concurrent with 25 dB maximum noise figure, and a high degree of amplitude and delay flatness ( $\pm 1$  dB and  $\pm 5$  deg. overall passband deviation from gain flatness and phase linearity and 0.15 dB/MHz and 0.5ns/50 MHz maximum gain and delay slope). For the specified single PM carrier, the transmitter output amplitude can be into saturation provided that the requirements on such linearity-related performance parameters as AM/PM conversion ( $5 \pm 1$  deg/dB max) and harmonic/nonharmonically related spurious content ( $\sim 50/60$  dBc max) are satisfied. Finally, to accommodate representative spacecraft thermal profiles, specified performance must be achieved over a 0-75°C baseplate temperature range.



2.0 RESULTS OF TECHNOLOGY ASSESSMENT



20 GHZ TRANSMITTER - CRITICAL TECHNOLOGY ITEMS

1. FUNCTIONAL CIRCUIT TECHNOLOGY
  - . IMPATT POWER AMPLIFIERS
  - . FET DRIVER AMPLIFIERS
  - . RF POWER DIVIDERS/COMBINERS
  - . FERRITE CIRCULATORS
2. CONSTITUENT DEVICE/MATERIAL TECHNOLOGY
  - . READ-PROFILE GAAS EPITAXIAL WAFER MATERIAL
  - . GAAS READ-IMPATT DIODES
  - . GAAS FET DEVICES



## 2.1 20 GHZ TRANSMITTER-CRITICAL TECHNOLOGY ITEMS

The critical areas of technology applicable to the subject 20 GHz transmitter fall into two general categories, functional circuits, and constituent devices and materials. In terms of the previously depicted functional RF block diagram of a composite 20 GHz FET/IMPATT transmitter, the key circuit technologies which must be developed at 20 GHz, include IMPATT power amplifiers, FET driver amplifiers, RF power dividers/combiners and ferrite circulators. The foregoing technology development in turn depends upon the concurrent evaluation of such critical 20 GHz device and material technologies as Read-profile GaAs epitaxial wafer material, GaAs Read-IMPATT diodes and GaAs FET devices.

None of the above requires any new fundamental breakthroughs but rather represents extension of the existing state of the art in these technologies at lower frequencies to the more severe constraints associated with operation at 20 GHz.



## 20 GHz PREFERRED TECHNOLOGY SUMMARY

| REQUIRED TECHNOLOGY         | LNR DESIGN APPROACH  | KEY PARAMETER GOALS  | SOURCE AND STATUS OF DEVELOPMENT   |
|-----------------------------|--|--|--|
| IMPATT POWER AMPLIFIER      | CIRCULATOR COUPLED TEM REFLECTION  | GAIN: 6-12 dB/STAGE<br>P <sub>o</sub> /STAGE: 0.4-6W<br>BW: 1 GHz (MIN) @ 20 GHz   | LNR-UNDER DEVELOPMENT (PRELIMINARY BREADBOARD 2 STAGE UNIT EXHIBITED 1.25W OUTPUT AND 15DB GAIN OVER A 1 GHz BW)                                       |
| FET DRIVER AMPLIFIER        | SE/BALANCED CASCADE IN DURIOD MICROSTRIP   | GAIN/STAGE: 3-5 dB<br>P <sub>o</sub> (1 dB)/STAGE: +15 to +20 dBm<br>BW: 1 GHz (MIN) @ 20 GHz  | LNR-UNDER DEVELOPMENT (PRELIMINARY BREADBOARD 2 STAGE UNIT EXHIBITED 9 dB LINEAR GAIN AND +16 dBm OUTPUT 1 dB COMPRESSION LEVEL OVER A 1 dB BANDWIDTH) |
| RF DIVIDER/COMBINER         | TEM PLANAR OR TE-MODE REACTIVE TYPE (DEPENDENT ON THERMAL/MECHANICAL DESIGN OF OVERALL TRANSMITTER.  | RESIDUAL INSERTION LOSS: 0.25 dB<br>BW: 1 GHz (MIN) @ 20 GHz   | LNR-UNDER DEVELOPMENT (PRELIMINARY BREADBOARD RESULTS VALIDATE THESE GOALS)  |
| FERRITE JUNCTION CIRCULATOR | ULTRAMINIATURE DIELECTRICALLY-LOADED STRIPLINE   | INSERTION LOSS: 0.25 dB/PASS (MAX)<br>ISOLATION/RETURN LOSS: 20 dB (MIN)<br>BW: 2 GHz (MIN) @ 20 GHz                                   | LNR-UNDER DEVELOPMENT (PRELIMINARY BREADBOARD VALIDATE THESE GOALS)  |
| IMPATT DIODES               | <ul style="list-style-type: none"> <li>GaAs READ PROFILE (LHL-SDR)</li> <li>SCHOTTKY CONTACT</li> <li>MULTIPLE MESA OR CHIP CONFIGURATION IN SEALABLE DHS PACKAGE</li> </ul> | FULL-DRIVE P <sub>out</sub> =3-6W<br>THERMAL RESISTANCE: 6-150C/W<br>POWER ADDED EFFICIENCY 25%  | LNR (USING PRECISELY PROFILED GaAs EPI MATERIAL PROCURED FROM VIABLE SUPPLIERS) (SIMILAR DDR DEVICES UNDER DEVELOPMENT BY RAYTHEON                     |
| HP FET'S                    | <ul style="list-style-type: none"> <li>GaAs READ PROFILE-(HL-SDR)</li> <li>GROWN JUNCTION</li> </ul>   | P <sub>out</sub> =1.5-2.5W<br>POWER ADDED EFFICIENCY: 20%<br>THERMAL RESISTANCE: 15-200C/W<br>P <sub>o</sub> : 0.5-1W<br>G: 4 dB (MIN) | VARIAN-AVAILABLE (USEFUL FOR CIRCUIT DEVELOPMENT   |
| MP FETS                     | PROCURED DEVICES   | P <sub>o</sub> : 0.5-1W<br>G: 4 dB (MIN)<br>P <sub>o</sub> : 0.03-0.1W<br>G: 5 dB (MIN)  | VARIAN, MSC, TI, RAYTHEON-UNDER DEVELOPMENT<br>VARIAN, DEXCEL, NEC -CURRENTLY AVAILABLE  |

LNR

## 2.2 20 GHZ PREFERRED TECHNOLOGY SUMMARY

The status of existing and projected 1982 time frame technology in the previously enumerated critical areas has been applied to the previously presented functional 20 GHz transmitter configuration, within the following preliminary guidelines which will give the LNR design:

- TEM microwave implementations wherever possible to minimize size and weight
- Use of IMPATT stages in low level high gain mode where possible to minimize demands on FET driver technology
- Optimum "mix" of IMPATT diode power accumulation within amplifier stages vis a vis externally by paralleling identical multistage "building blocks" between passive power divider and combiner.

As tabulated above, it is seen that:

- the most critical area of technology relative to the 1982 time frame 20 GHz IMPATT amplifier requirements is that encompassing the Read IMPATT diode itself.
- the preferred, approach entailing the realization of 20 GHz Read-IMPATT diodes in-house, based upon the existence of credible suppliers of precisely-profiled GaAs Read-IMPATT epitaxial material and a sophisticated proven in-house GaAs microwave diode processing facility, provides a higher degree of flexibility in diode/circuit optimization capability.

The critical aspects of K-band microwave circuit technology enumerated above are all addressed in current in-house breadboard development effort.



3.0 RESULTS OF PARAMETRIC TRADEOFF ANALYSIS



20 GHz TRANSMIT AMPLIFIER DESIGN TRADEOFFS

1. POWER SECTION "BUILDING BLOCK" IMPATT STAGE TRADEOFFS
2. POWER SECTION INTERSTAGE COMBINATORIAL TRADEOFFS
3. DRIVER SECTION TRADEOFFS





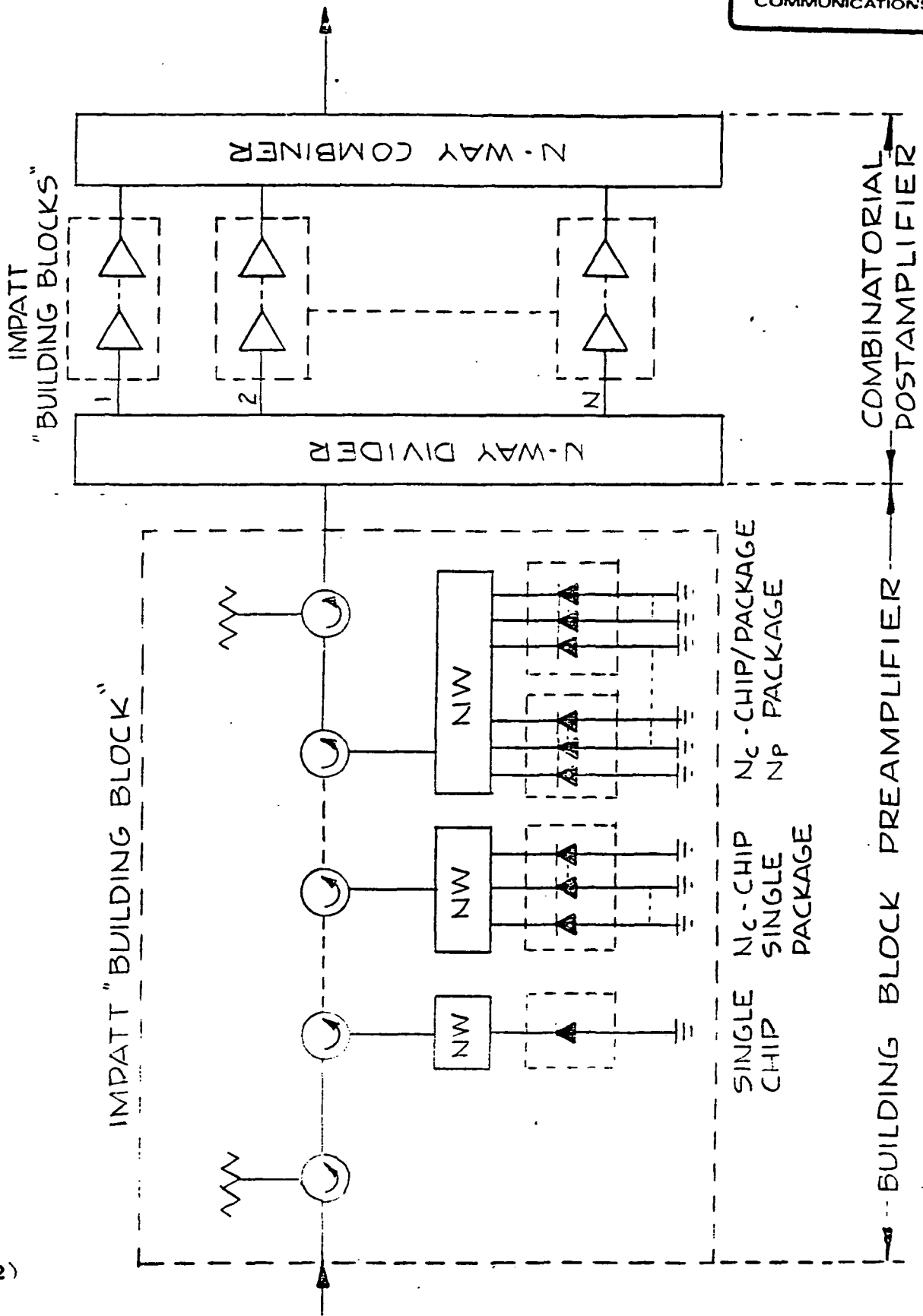
### 3.1 20 GHZ TRANSMIT AMPLIFIER DESIGN TRADEOFFS

Based upon the previously presented functional RF topological block diagram of the subject 20 GHz transmitter, the major design tradeoffs governing the optimization of this configuration fall into the following categories.

1. Power section "building block" IMPATT stage tradeoffs, including:
  - . degree of chip and/or package level intrastage IMPATT diode combining
  - . mode of IMPATT amplifier stage operation (stable amplifier vis a vis injection loaded oscillator)
  - . RF power output and DC/RF efficiency vs gain/stage, linearity and device junction temperature
  - . IMPATT diode DC bias technique (constant voltage vs constant current).
  - . capacitive tuning approach for normally inductive IMPATT diode (Parallel- vs series tuning)
2. Power section interstage combinatorial tradeoffs
  - . degree(N) of paralleled interstage power combination
  - . type of N-way K-band power divider/combiner
3. Driver section tradeoffs
  - . Type of device(s) per amplifier stage
  - . Amplifier stage topology

The resolution of these tradeoffs pursuant to evolution of an optimum design is described subsequently.





### 3.2 GENERAL COMBINATORIAL IMPATT POWER MODULE

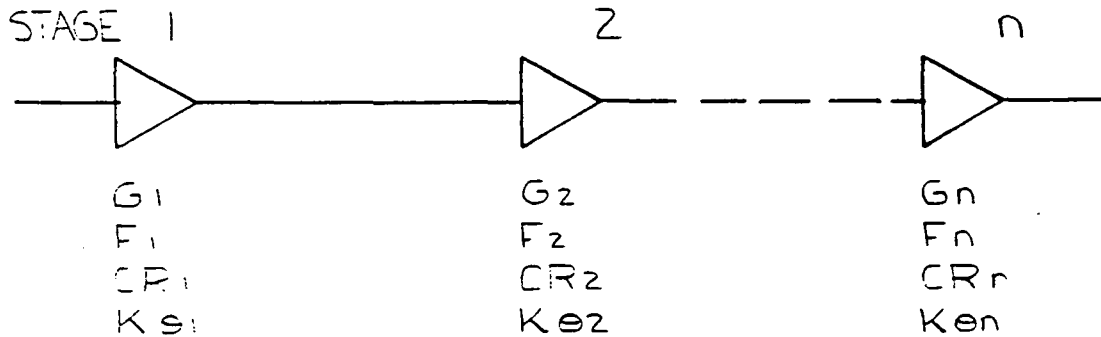
The most general combinatorial IMPATT power module configuration consists of the closely integrated combination of:

- M'-stage IMPATT preamplifier
- combinatorial postamplifier comprising N identical M-stage IMPATT "building block" amplifiers coupled between normally identical N-way power divider and combiner

In general it is not necessary that the M'-stage preamplifier be identical to each of the M-stage "building blocks". For optimum usage of amplifier stages and minimum overall parts count, it is desirable that the N "building blocks" be configured toward comparable RF power output capability representing the maximum achievable output power in a single stage under a practical degree of intrastage IMPATT device combining. In each "building block" amplifier, as in the preamplifier, the cascade is configured of stages of progressively increasing RF power output capability achieved as shown by intrastage device combining to the maximum practical degree at the chip (or mesa) level in a single package, and then at the package level.



## POWER AMPLIFIER CASCADE FORMULATIONS



$G$  = LARGE-SIGNAL GAIN  
 $F$  = NOISE FIGURE  
 $CR$  = COMPRESSION RATIO (dB/dB)  
 $K_{\theta}$  = AM/PM CONVERSION (deg/dB)  
 $CR = \Delta P_{OUT} (dB) / \Delta P_{IN} (dB)$   
 $K_{\theta} = \Delta \theta_{OUT} (deg) / \Delta F_{IN} (dB)$   
 For LINEAR AMPLIFIER  
 $CR = 1, K_{\theta} = 0$

$$10 \log_{10} G_{OV} = 10 \log_{10} G_1 + 10 \log_{10} G_2 + \dots + 10 \log_{10} G_n$$

$$F_{LV} = F_1 + \frac{F_2 - 1}{G_1 CR_1} + \frac{F_3 - 1}{G_1 G_2 CR_1 CR_2} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_n CR_1 CR_2 \dots CR_n}$$

$$CR_{OV} = CR_1 \cdot CR_2 \cdot CR_3 \dots CR_n$$

$$K_{\theta OV} = K_{\theta 1} + CR_1 \cdot K_{\theta 2} + CR_2 \cdot CR_1 K_{\theta 3} + CR_1 \dots CR_{n-1} K_{\theta n}$$

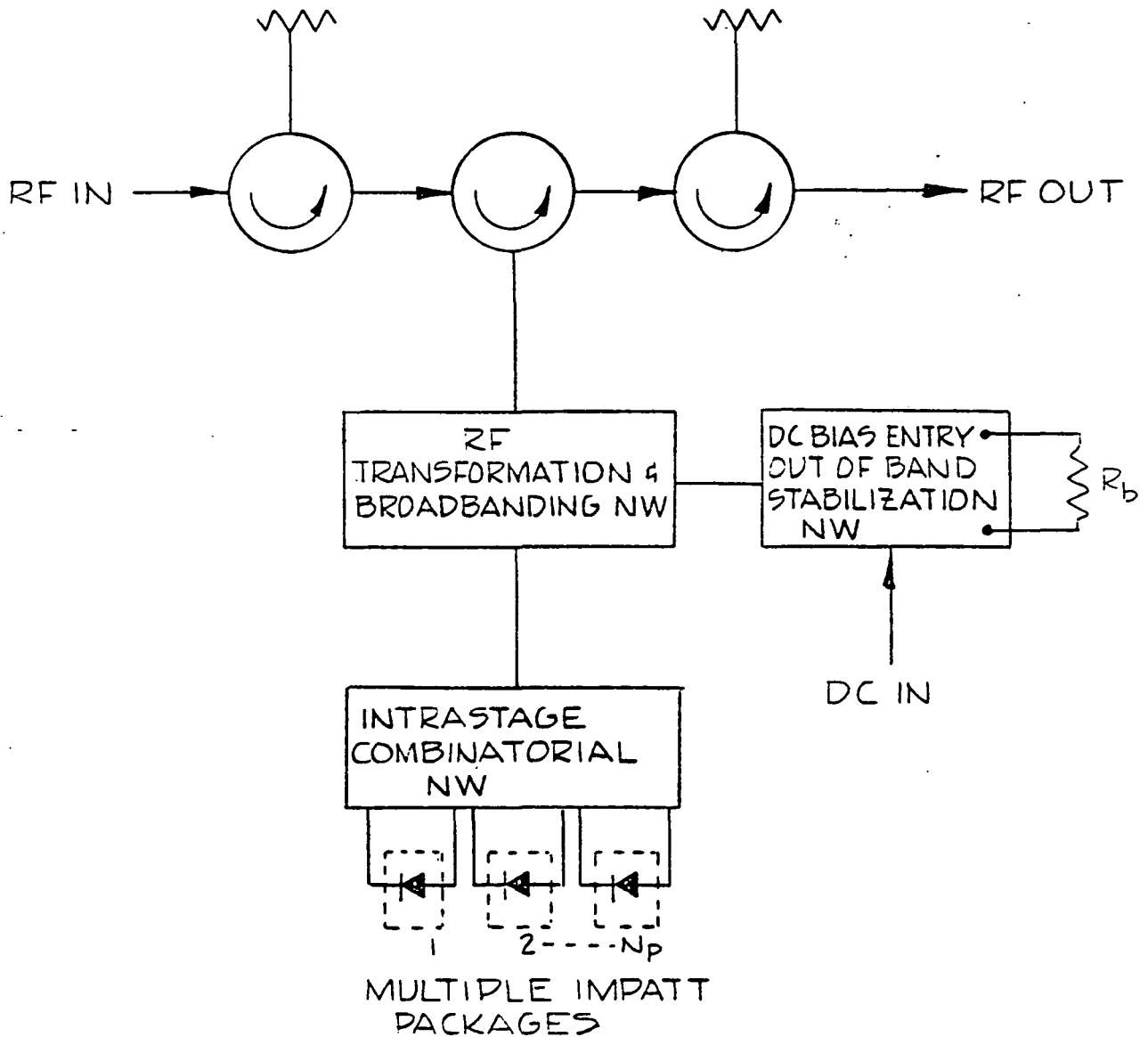
### 3.2.1 POWER AMPLIFIER CASCADE FORMULATIONS

In order to analyze the performance of the IMPATT power section, FET driver and overall 20 GHz transmitter on a stage-by-stage budgetary basis, the foregoing power amplifier cascade formulations are used. These formulations are generalizations of well-known cascaded linear amplifier analysis, wherein the following aspects of nonlinear power amplifier performance are taken into account:

- nonlinearity of input/output power transfer characteristic at operating point  $P_{in}$ ,  $P_{out}$  expressed in terms of compression ratio  $CR = (dP_{out}/dP_{in}) (P_{in}/P_{out})$ , with CR ranging between unity and zero for the extremes of a linear and completely saturated amplifier.
- variability of input/output transmission phase  $\theta$  out with input power level, expressed in terms of AM/PM conversion factor  $k_{\theta} = \Delta \theta_{out} \text{ (deg)} / \Delta P_{in} \text{ (dB)}$ , which is zero in the linear amplifier limit.
- noise figure cascade formulation is based upon incremental stage gains at respective large signal operating points, given in turn by  $G \cdot CR = dP_{out}/dP_{in}$ .

These formulations are used in all subsequent multistage amplifier performance analyses.





### 3.3 BASIC IMPATT AMPLIFIER STAGE

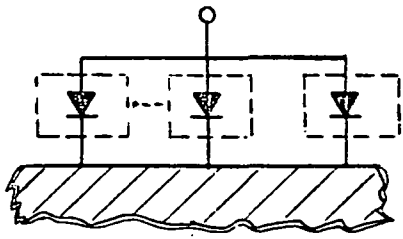
Each IMPATT amplifier stage used in the preamplifier and combinatorial "building blocks" comprising the previously described overall IMPATT power module is basically a circulator-coupled negative resistance reflection amplifier, with additional match-terminated circulator junctions deployed as input and/or output isolators. This amplifier stage incorporates  $N_p$  (one or more) IMPATT diode packages in an  $N_p$ -way combinatorial mount which is in turn coupled to the active port of the amplifier circulator through an appropriate impedance transformation and broadbanding network. The latter may also contain a band rejection type out-of-band resistive loading network for stabilization against spurious out-of-band oscillation. An RF isolated DC bias entry network may be incorporated in conjunction with this resistive loading circuit or, alternatively, may be incorporated at the match-terminated port of the input or output isolator. Each IMPATT diode package may, in turn, incorporate  $N_c$  IMPATT mesas and/or chips per package.

The major tradeoffs governing the design of this representative IMPATT amplifier stage includes degree and type of device chip or mesa level ( $N_c$ ) and package level ( $N_p$ ) intrastage IMPATT combining, mode of amplifier operation (stable vs. I.L.O.), bandwidth/power/gain and linearity and techniques for tuning and biasing.



RF INTERFACE

RF INTERFACE

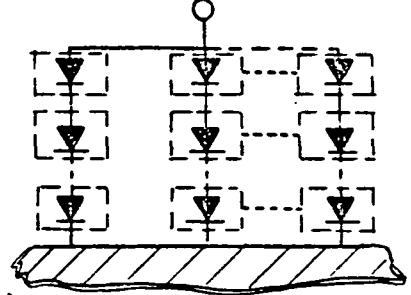


1) PARALLEL



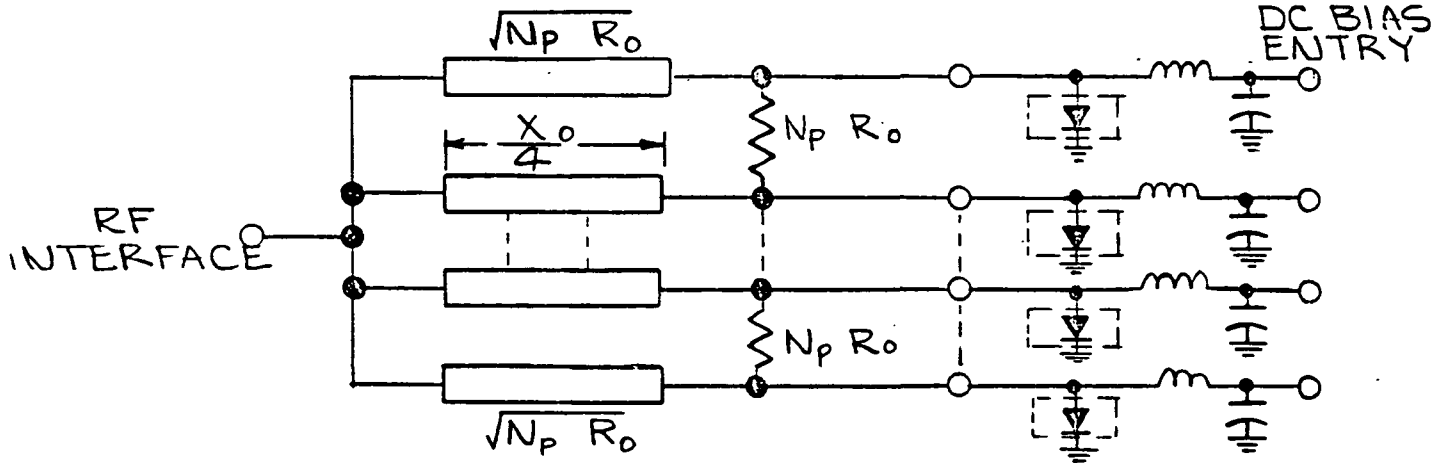
2) SERIES

RF INTERFACE

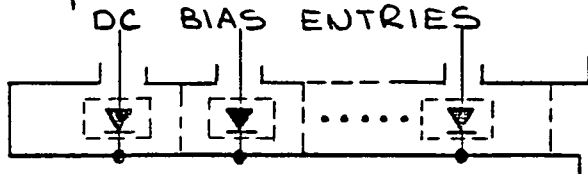


3) SERIES-PARALLEL

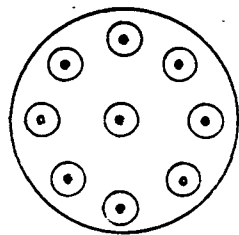
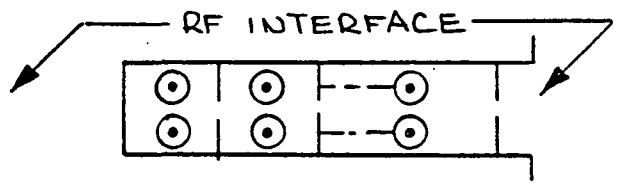
A - DIRECT INTERCONNECTION



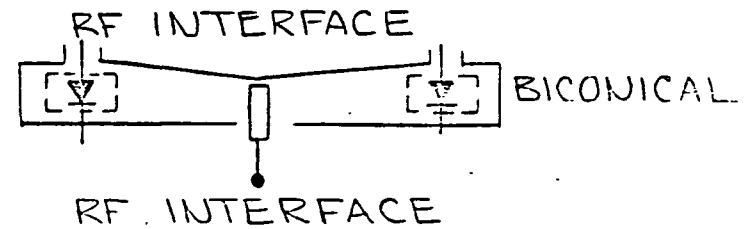
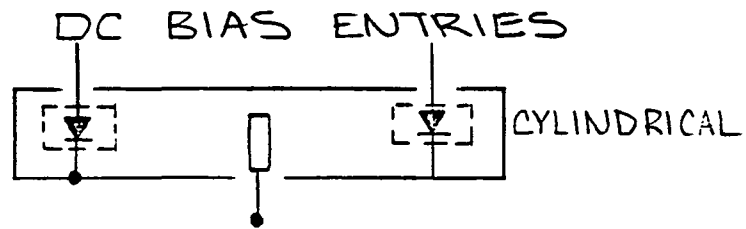
B -  $N_p$ -WAY ISOLATED-HYBRID (WILKINSON) COMBINER



1) WAVEGUIDE



2) RADIAL CAVITY



C. EXTENDED INTERACTION REACTIVE CAVITIES



### 3.3.1 INTRASTAGE IMPATT DIODE - LEVEL COMBINATORIAL ALTERNATIVES

The alternative configurations wherein more than one IMPATT diode may be combined within a single amplifier stage involve device combination at both the mesa or chip level and at the package level. The alternatives for mesa or chip level combining by direct interconnection within a single package include:

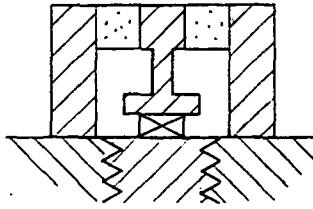
- multiple parallel connected mesas per chip
- multiple parallel, series, or series-parallel connected chips per package.

Further intrastage diode combination at the package level can be accomplished using one of the following:

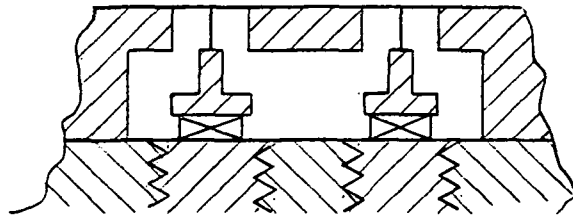
- direct paralleling (series connected packages are not viable due to inadequate thermal heat sinking as well as mechanical awkwardness)
- planar N-way Wilkinson hybrid junction (resistively isolated) coupling
- reactive N-way planar or waveguide junction
- radial, conical or waveguide reactive extended interaction cavity combining

The key factors influencing a tradeoff analysis encompassing the above intrastage combinatorial alternatives include their relative compatibility with adequate thermal heat sinking of the IMPATT devices and with graceful degradation in overall transmitter output power under random device failures.

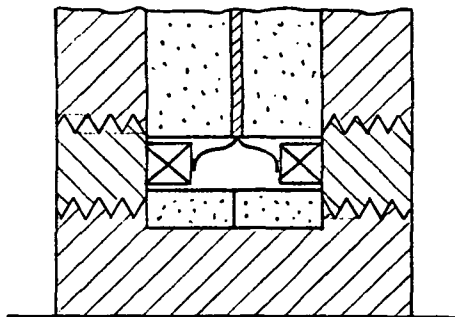




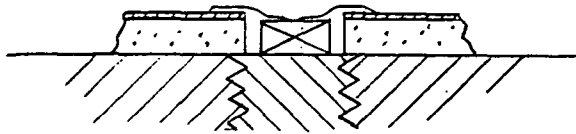
A. COAXIAL



B. WAVEGUIDE (CROSS SECTION)



C. STRIP LINE



D. MICROSTRIP

## 3.3.2

INTRASTAGE DIODE-LEVEL COMBINATORIAL TRADEOFF CONCLUSIONS

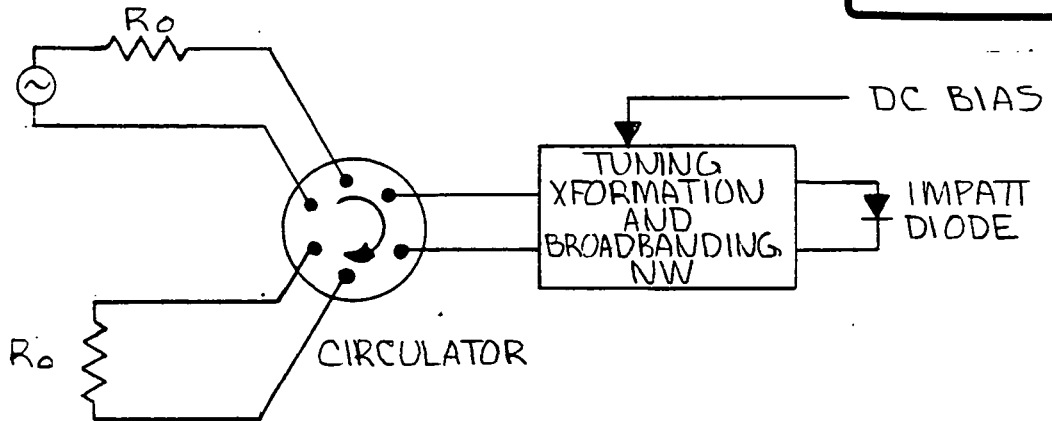
The results of a detailed tradeoff analysis relating to the optimum degree of intrastage chip and/or package level IMPATT device combining are summarized as follows:

## 1. Intra package chip level combining:

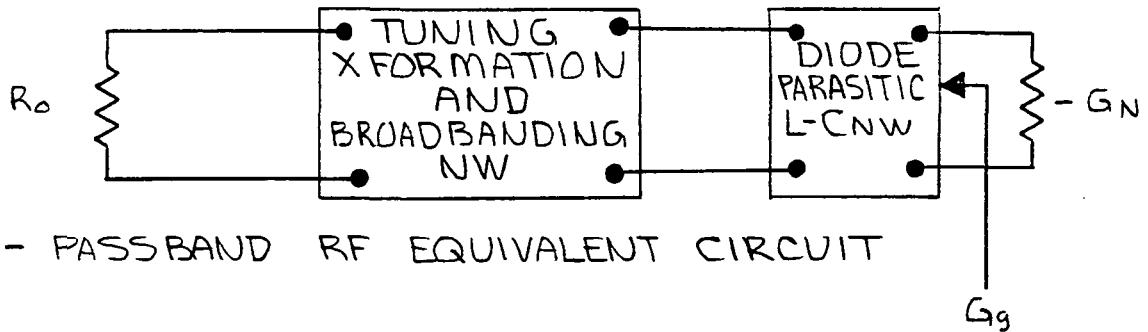
- Multiple ( $N_C$ ), paralleled mesas per chip limited to  $N_C \leq 2$  to avoid thermal "crowding" - single annular mesa a high power output alternative
- Series and parallel connected chips viable for  $N_C \leq 2$  - series connected chips are thermally in parallel in diamond heat-sunk package
- 2 X 2 series-parallel combination of dual series-connected dual-mesa chips conceptually feasible
- Optimum degree and form of chip level combining awaits breadboard evaluation-tentative assessment limits  $N_{ct} \leq 4$

## 2. Intrastage package level combining:

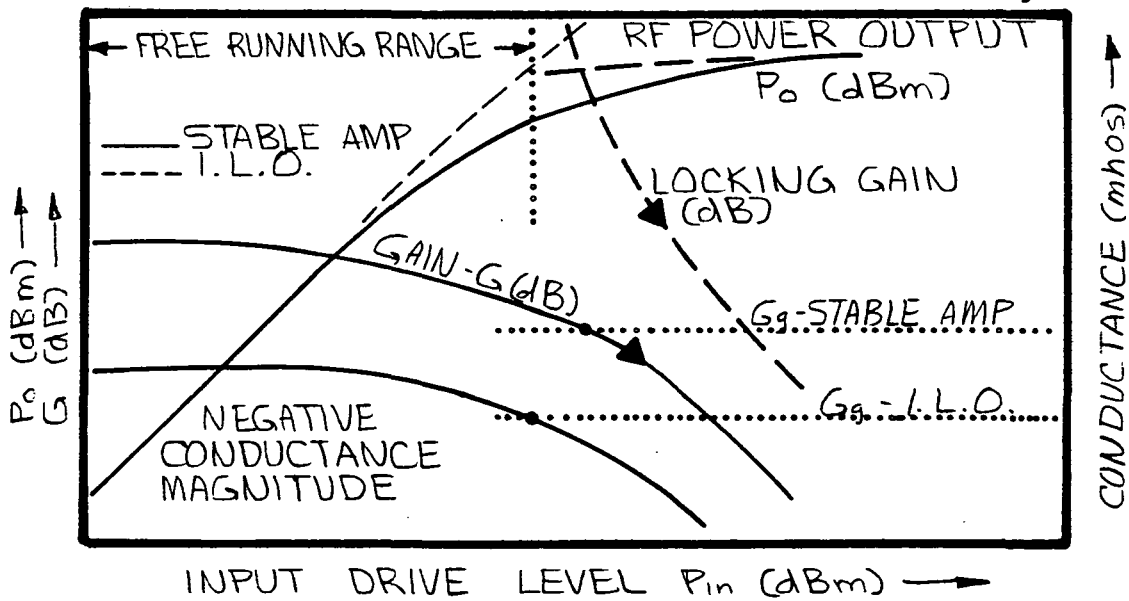
- N-th order intrastage combining of  $N_p$  IMPATT packages tends to reduce the stage bandwidth capability relative to that of a single diode stage by a factor which, in the limit of large  $N_p$ , approaches  $(1/N_p)$ , (although, for  $N_p=2$  this reduction is negligible).
- Direct interconnection of any number of packaged diodes in series or more than two diodes in parallel is impractical for thermal, electrical and physical reasons.
- Combining more than two IMPATT packages in a single amplifier stage, though possible using hybrid or extended interaction combiners, will excessively compromise the graceful degradation capability of the overall IMPATT power section (which is more easily enhanced by multiple, mutually isolated building block stages than by multiple IMPATT packages within a stage). Since a single device failure will generally detune the stage gain response sufficiently to be equivalent to a stage failure.
- The choice of embedding geometry for one of two IMPATT packages per stage (coaxial, strip-line, microstrip or waveguide) must be made as much on the basis of the thermal heat sinking provided by said configuration as of the circuit properties introduced thereby. (31)



A- SCHEMATIC OF CIRCULATOR-COUPLED IMPATT STABLE OR INJECTION-LOCKED AMPLIFIER STAGE



B- PASSBAND RF EQUIVALENT CIRCUIT



C-COMPARATIVE RF CHARACTERISTICS

COMPARISON OF STABLE AND INJECTION LOCKED IMPATT AMPLIFIER

COMPARISON OF STABLE VERSUS INJECTION  
LOCKED MODES OF IMPATT DIODE AMPLIFICATION

A detailed comparative analysis of the relative merits of the stable versus injection-locked oscillator (ILO) modes of IMPATT diode amplification has yielded the following conclusions:

The advantages of the ILO mode of amplification are:

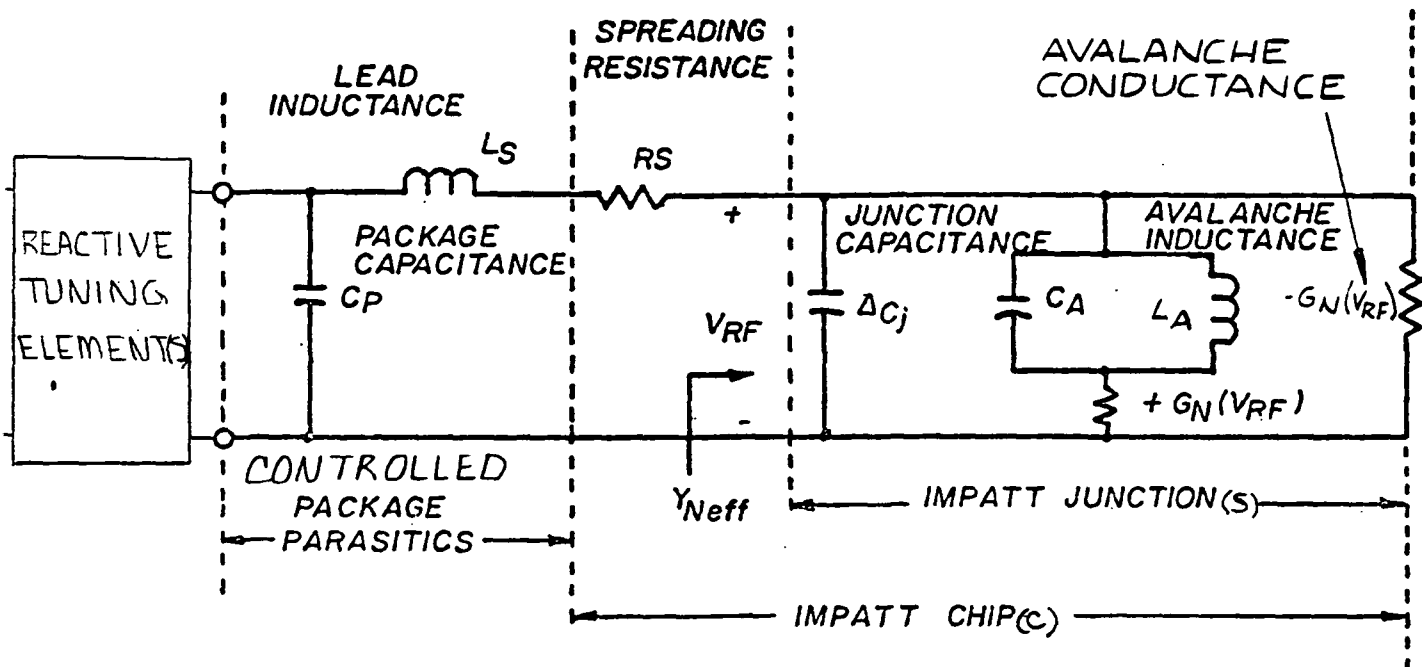
- Greater power added efficiency and higher gain at the maximum efficiency operating point.
- More saturated input-output transfer characteristic, e.g., more constant RF output versus input power for input levels exceeding the locking threshold for given bandwidth.

The disadvantages of the ILO mode of amplification are:

- Lower gain-bandwidth product (at the maximum efficiency operating point, the stable amplifier provides lower gain but considerable wider bandwidth than the ILO)- the locking bandwidth of the ILO, however, must exceed the desired bandwidth by an amount sufficient to accommodate the ILO free running frequency drift, thus reducing the advantage of the higher gain at maximum efficiency operating point.
- Somewhat greater bandedge delay distortion and AM/PM conversion.
- Noisy, free running carrier transmitted during time intervals for which drive level falls below locking threshold.
- Higher AM noise as reflected in equivalent noise figure, possibly causing degradation in phase noise due to AM/PM conversion.
- Anomalous degradation imparted to PSK signals, particularly for abrupt 0-180° phase transitions, resulting in higher BER in PSK link. Similar degradation does not occur for angle modulated waveforms with less abrupt phase discontinuities. This degradation increases with decreasing bit transition period for fixed ILO bandwidth and can only be suppressed for ILO bandwidths greater than 2 to 5 times the maximum bit rate.

Necessity to "turn-off" ILO (remove DC bias) during all transient and steady state time intervals for which drive level falls below locking threshold- hence ILO only useful for truly cw envelope, angle-modulated signals.





$$\bullet Y_{Neff} = G_{Neff}(f) + jB_{Neff}(f)$$

$$\bullet f_M = \frac{1}{2\pi\sqrt{L_A C_A}} ; Q_A = 2\pi f_0 C_A / G_N$$

$$\bullet G_{Neff}(f) \cong \frac{G_N}{1 + 4Q_A^2 y^2}$$

$$y = \frac{f}{f_M} - 1$$



TUNED IMPATT DIODE EQUIVALENT CIRCUIT MODEL

### 3.3.4 TUNED IMPATT DIODE EQUIVALENT CIRCUIT MODEL

The detailed large-signal equivalent circuit model of an externally reactively tuned, packaged single or multi chip IMPATT diode has been used as the basis for a tradeoff analysis leading to IMPATT power amplifier stage design optimization. The salient features of this circuit model are:

- band-limited, RF drive level-dependent IMPATT-mode negative conductance, characterized by maximum-conductance center frequency ( $f_m$ ) and bandwidth parameter ( $Q_A$ ).
- monotonically decreasing negative conductance magnitude  $G_N$  ( $V_{RF}$ ) with RF drive level, with rate of fall-off (typically quadratic) dependent on mode of DC bias (constant current vs. constant voltage, with the latter resulting in more moderate fall-off due to compensating effect of RF drive-derived rectified DC current)
- direct junction-area dependence of  $G_N$  and excess junction capacitance component  $\Delta C_j$ , which also vary directly with RF power added capability and DC bias current requirement.
- controllable package parasitics which, for high power (large  $\Delta C_j$ ) K-band operation, generally result in inductive untuned device impedance characteristic
- external parallel or series capacitive tuning element for resonating said inductive diode at specified amplifier band center, with the former resulting in a more tolerable negative impedance level and wider bandwidth capability than the former.

Typical normalized susceptance or reactance slopes of tuned K-band IMPATT diodes are in the range 15-30.







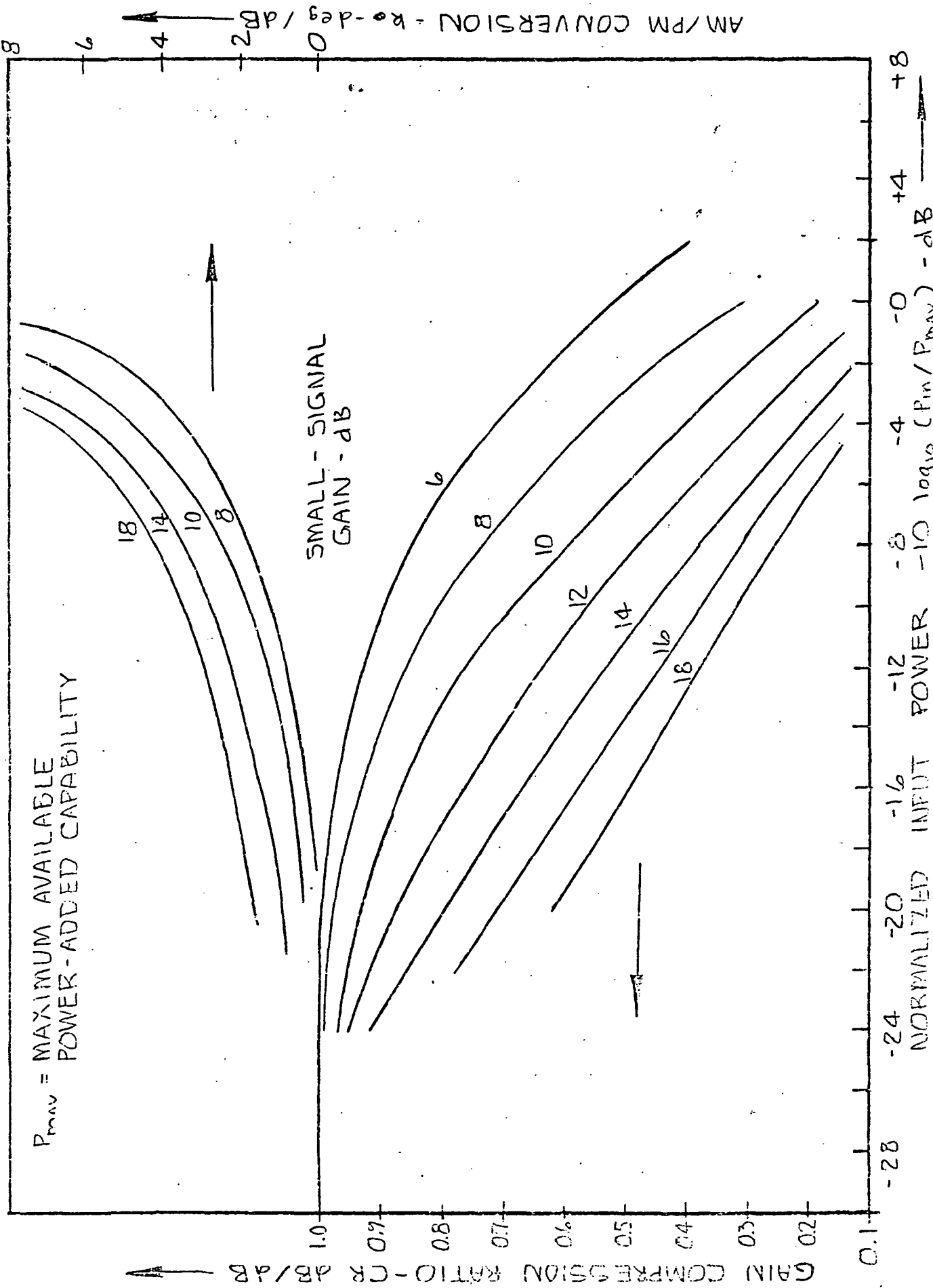
### 3.3.5 STABLE IMPATT AMPLIFIER TRADEOFFS

The key design/performance tradeoffs pertinent to the realization of an optimum IMPATT power "building block" amplifier stage are:

- large signal operating gain vs. power added efficiency
- operating gain vs. bandwidth
- operating gain vs. linearity (compression ratio, AM/PM conversion)
- RF power output vs. junction temperature.



# GENERAL LINEARITY CHARACTERISTICS OF IMPATT AMPLIFIER STAGE

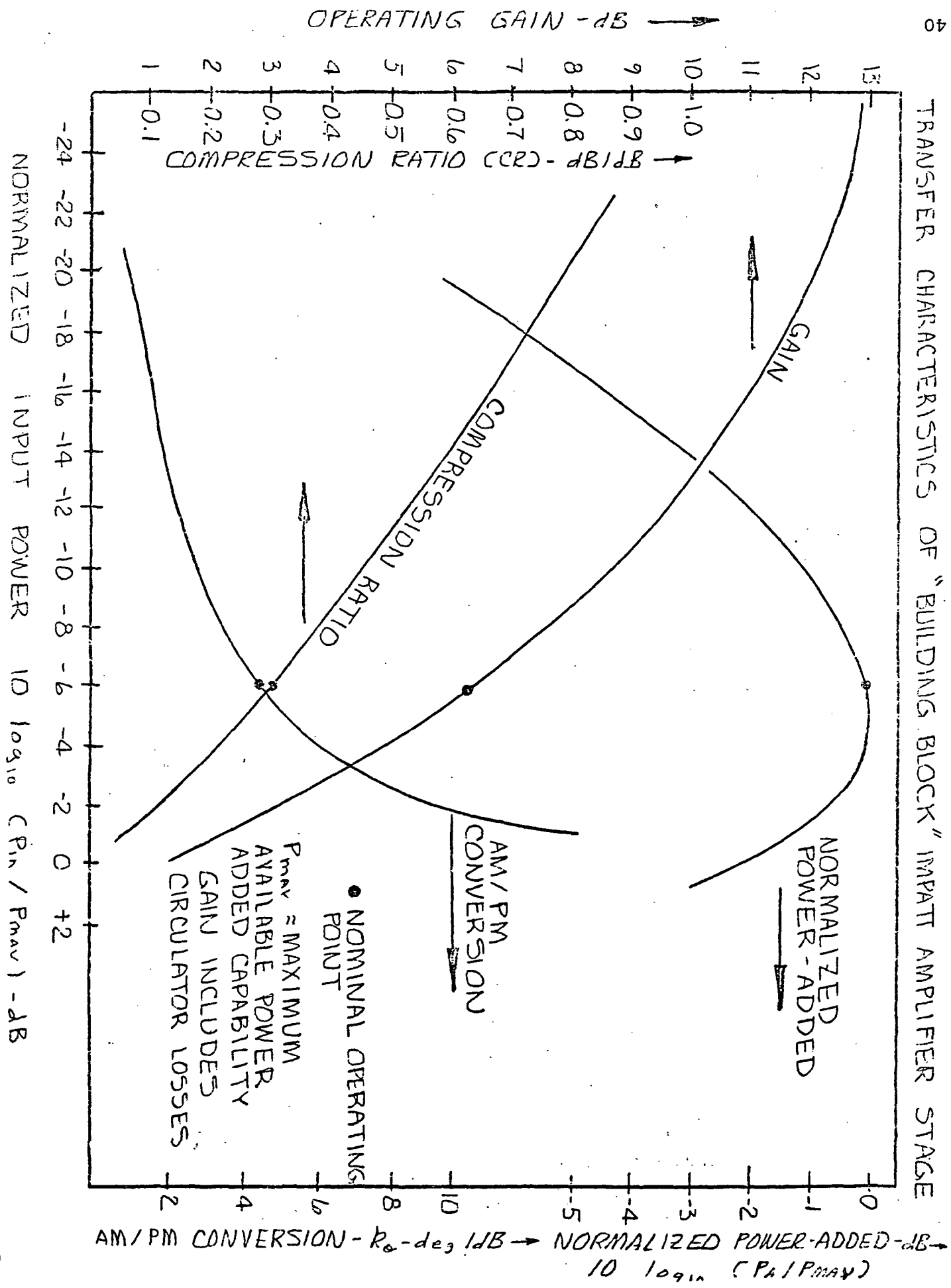


A detailed analysis encompassing the foregoing tradeoffs and based upon an established cubic-law nonlinearity of the IMPATT RF current-voltage dependence, indicates that:

- optimum large signal operating gain for maximum power added efficiency is a strong function of small signal gain, ranging between 3 and 7 dB for small signal gains of 6 to 18 dB
- the higher the operating gain, the greater the degree of amplitude saturation (desirable for single carrier angle-modulated signals) but the greater the AM/PM conversion
- the higher the operating gain, the lower the margin against small signal instability
- for limited DC bias range, backoff in DC bias power (from maximum power added point) provides one-for-one reduction in RF power output and diode junction temperature rise (above amplifier mount temperature).
- gain-bandwidth constraints for constant output power across passband indicate that for range of operating gain under consideration nominal midband (20 GHz) RF output power level can be maintained over minimum bandwidths of 0.5-1.0 GHz
- for spacecraft-compatible reliability and life expectancy, IMPATT diode junction temperature rise above amplifier housing must be maintained below 100°-150°C, corresponding to diode thermal conductance of greater than 25-50 mW/°C per watt of RF output power.



TRANSFER CHARACTERISTICS OF "BUILDING BLOCK" IMPATT AMPLIFIER STAGE



### 3.3.6

#### TYPICAL IMPATT AMPLIFIER STAGE PERFORMANCE CHARACTERISTICS

Representative IMPATT power amplifier stage performance characteristics, resulting from a design which accounts for all of the foregoing trades, includes:

- operating gain: 6.2 dB (including circulator losses)
- small signal gain: 16.25 dB (including circulator losses)
- operating bandwidth: 1 GHz
- compression ratio: 0.3 dB/dB
- AM/PM conversion: 4.2 deg/dB
- thermal resistance per IMPATT mesa: 16°C/W

Based upon the projected characteristics of the IMPATT diodes under development for use in the power amplifier "building blocks", additional amplifier characteristics are:

- |  | MP     | HP    |
|--|--------|-------|
| • composite device type:                     |        |       |
| • composite device RF power added capability | 1.25W  | 5W    |
| • amplifier RF/DC power added efficiency     | 23.6 % | 23.6% |
| • amplifier RF output power                  | 1.56W  | 6.25W |
| • composite device thermal resistance:       | 16°C/W | 6°C/W |



POWER SECTION "BUILDING BLOCK" IMPATT STAGE TRADEOFF RESULTS

| TRADEOFF  | PREFERRED APPROACH  | RATIONALE  |
|---|---|--|
| <p>1. DEGREES OF <u>INTRASTAGE</u> IMPATT DEVICE COMBINING</p> <ul style="list-style-type: none"> <li>• NUMBER OF PARALLELED IMPATT MESAS PER CHIP (Nm)</li> <li>• NUMBER OF IMPATT CHIPS PER PACKAGE (Nc)</li> <li>• NUMBER OF IMPATT PACKAGES PER AMPLIFIER STAGE (Np)</li> <li>• APPROACH TO CHIP AND PACKAGE COMBINING</li> </ul> | <p>1-2</p>  | <p>Nm <math>\leq 2</math> TO AVOID THERMAL "CROWDING" - SINGLE ANNULAR MESA A HIGH P<sub>0</sub> ALTER-NATIVE</p> <p>Nc <math>\leq 2</math> TO AVOID EXCESSIVE PACKAGE COMPLEXITY-SERIES OR PARALLEL CONNECTION VIABLE</p> <p>Np <math>\leq 2</math> TO MAINTAIN GRACEFUL DEGRADATION CAPABILITY AND AVOID BW DEGRADATION</p> <p>SERIES OR PARALLEL CHIPS-PARALLEL PACKAGES</p> <p>1.5-6W</p>  |
| <p>2. MODE OF IMPATT STAGE OPERATION (CIRCULATOR-COUPLED NEGATIVE RESISTANCE REFLECTION AMPLIFICATION) - STABLE AMPLIFIER VS. INJECTION LOCKED OSCILLATOR (I.L.O.)</p>  | <p>STABLE AMPLIFIER</p>   | <p>6W (NmNpNc <math>\leq 4</math>) FOR TOLERABLE PACKAGE/CIRCUIT COMPLEXITY AND MAINTENANCE OF GRACEFUL DEGRADATION</p> <p>I.L.O. DISADVANTAGES:</p> <ul style="list-style-type: none"> <li>• LOWER G-BW PRODUCT (DESPITE HIGHER GAIN) @ MAX-EFF. OPERATING PT.</li> <li>• BW MUST ACCOMMODATE FREE-RUNNING FREQ. DRIFT</li> <li>• MUST BE "TURNED OFF" DURING INTERVALS OF CARRIER DROPOUT</li> <li>• HIGHER AM NOISE, DELAY DISTORTION AND AM/PM CONVERSION</li> </ul> |
| <p>3. PERFORMANCE TRADEOFFS VS RF POWER OUTPUT AND POWER-ADDED EFFICIENCY</p> <ul style="list-style-type: none"> <li>• GAIN-BANDWIDTH</li> <li>• INPUT/OUTPUT LINEARITY</li> <li>• DEVICE JUNCTION TEMPERATURE</li> </ul>   | <p>GOP (dB) <math>\approx G_{SS}^2</math> (dB)</p> <p>GOP (dB) <math>\approx 3-6</math> dB</p> <p>CR <math>\approx 0.4</math> dB/dB</p> <p>PO <math>\approx 0.8</math> P<sub>OMAX</sub></p> | <ul style="list-style-type: none"> <li>• MAX. POWER ADDED OVER BAND</li> <li>• MAX. SMALL SIGNAL STABILITY</li> <li>• MAX. EFFICIENCY</li> <li>• BACKOFF IN PDC FOR LOWER T<sub>j</sub> AND TOLERABLE PERFORMANCE</li> </ul>   |
| <p>4. IMPATT DIODE DC BIAS TECHNIQUE (CONSTANT VOLTAGE VS. CURRENT)</p>   | <p>CONSTANT VOLTAGE</p>   | <ul style="list-style-type: none"> <li>• GREATER LINEARITY</li> <li>• GREATER DEGREE OF SMALL AND LARGE-SIGNAL STABILITY</li> <li>• FULL DYNAMIC RANGE (FROM SMALL-SIGNAL LIMIT TO FULL POWER OPERATION)</li> </ul>  |
| <p>5. TECHNIQUE FOR CAPACITIVE TUNING ABOVE RESONANCE (INDUCTIVE) IMPATT DIODE (SERIES VS. PARALLEL)</p>  | <p>PARALLEL</p>   | <ul style="list-style-type: none"> <li>• WIDER-BAND CAPABILITY</li> <li>• MORE TOLERABLE NEGATIVE IMPEDANCE LEVEL</li> </ul>   |

### 3.3.7: SUMMARY OF POWER SECTION "BUILDING BLOCK" TRADEOFF RESULTS

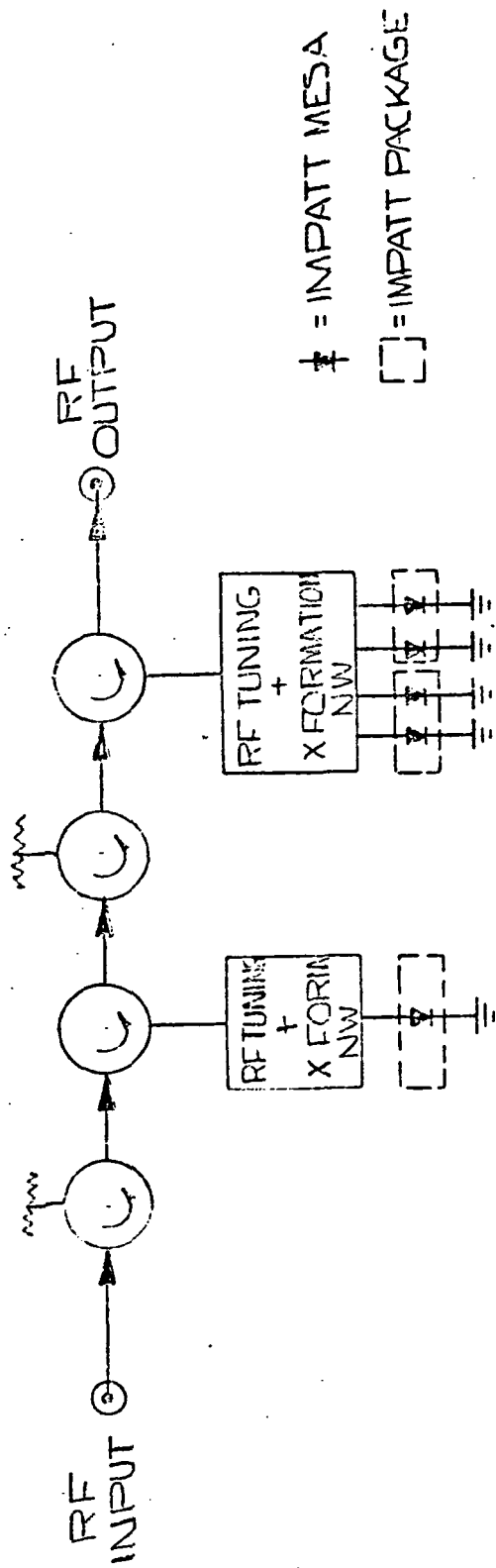
As a result of the preceding tradeoff analyses, it has been concluded that the optimum designs for the circulator coupled IMPATT amplifier stages comprising the overall transmitter power section "building blocks" will incorporate the following features:

- degree of intrastage mesa level ( $N_m \leq 2$ ), chip-level ( $N_c \leq 2$ ) and package level ( $N_p \leq 2$ ) combining:  $N_m N_c N_p \leq 4$  for tolerable package/circuit complexity and graceful degradation under random device failure.
- stable amplifier rather than injection locked oscillator mode of operation.
- parallel-tuned IMPATT packages.
- constant voltage mode of DC bias.

Based upon projected IMPATT diode parameters, key IMPATT power stage performance parameters over the specified bandwidth include:

- RF output power: 1.6, 6.4W
- Operating gain: 6 dB
- RF/DC power added efficiency: 22.5 percent for complete amplifier stage





PROJECTED PERFORMANCE

- FREQUENCY RANGE: 19.7-20.2 GHz
- RF OUTPUT LEVEL: 1.56W
- RF INPUT LEVEL: 0.02W
- OPERATING GAIN: 18.9dB
- DC POWER CONSUMPTION: 10W
- RF/DC POWER-ADDED EFFICIENCY: 15.4%
- GAIN COMPRESSION RATIO: 0.18dB/dB
- AM/PM CONVEFSION: 4.9 deg/dB
- NOISE FIGURE: 30.5dB
- GAIN FLATNESS: ±0.3dB
- PHASE LINEARITY: ±3 deg

PREAMP

- FREQUENCY RANGE: 19.7-20.2 GHz
- RF OUTPUT LEVEL: 6.25W
- RF INPUT LEVEL: 0.06W
- OPERATING GAIN: 12.3dB
- DC POWER CONSUMPTION: 25W
- RF/DC POWER-ADDED EFFICIENCY: 23.5%
- GAIN COMPRESSION RATIO: 0.09dB/dB
- AM/PM CONVEFSION: 32.5dB
- NOISE FIGURE: ±0.2dB
- GAIN FLATNESS: ±2 deg
- PHASE LINEARITY: ±2 deg

COMBINATORIAL POSTAMP



PREFERRED 20 GHz IMPATT POWER SECTION  
 "BUILDING BLOCK" AMPLIFIER DESIGN

X  
 CUT HERE  
 UNWARRANTED  
 1-82



### 3.3.8

#### PREFERRED 20 GHz IMPATT POWER SECTION "BUILDING BLOCK" AMPLIFIERS

Based upon the previously cited single stage IMPATT amplifier tradeoff results and the projected characteristics of GaAs Read IMPATT diodes currently under development, preferred two-stage IMPATT amplifier "building block" configurations have evolved for use as the IMPATT power section preamplifier as well as the combinatorial postamplifier "building blocks." In the latter case, both IMPATT stages are operated at their respected maximum power added gain/input drive levels, whereas in the former, the input stage is operated as a higher gain, lower level driver. In either case, due to the relatively low gain level (~6 dB) of the output stage, it is sufficient that the two stages be buffered with an input and interstage isolator without the necessity for an output isolator. Therefore, either "building block" can be realized in terms of a pair of one-port IMPATT mounts, connected to the appropriate ports of an integrated six port (four-junction) circulator.



OVERALL POWER SECTION COMBINATORIAL TRADEOFFS

1. DEGREE OF INTERSTAGE COMBINING (N) FOR SPECIFIED 20 W

TOTAL POWER OUTPUT, BASED UPON:

- POWER OUTPUT CAPABILITY OF INDIVIDUAL "BUILDING BLOCKS"
- DEGREE OF TOLERABLE GRACEFUL DEGRADATION UNDER RANDOM DEVICE FAILURE:
- GEOMETRIC REALIZABILITY

2. N-WAY POWER DIVIDER/COMBINER TOPOLOGY, BASED UPON:

- MINIMUM RESIDUAL INSERTION LOSS CAPABILITY
- MAXIMUM DEGREE OF SYMMETRY
- ABSENCE OF TRANSMISSION IMPAIRMENTS (PHASE IMBALANCE, EXCESSIVE MISMATCH) UNDER OPERATING CONDITIONS
- COMPATIBILITY WITH MECHANICAL CONSTRAINTS IMPOSED BY GEOMETRY AND HEAT-SINKING REQUIREMENTS OF PARALLELED IMPATT "BUILDING BLOCKS"



## 3.4

OVERALL POWER SECTION COMBINATORIAL TRADEOFFS

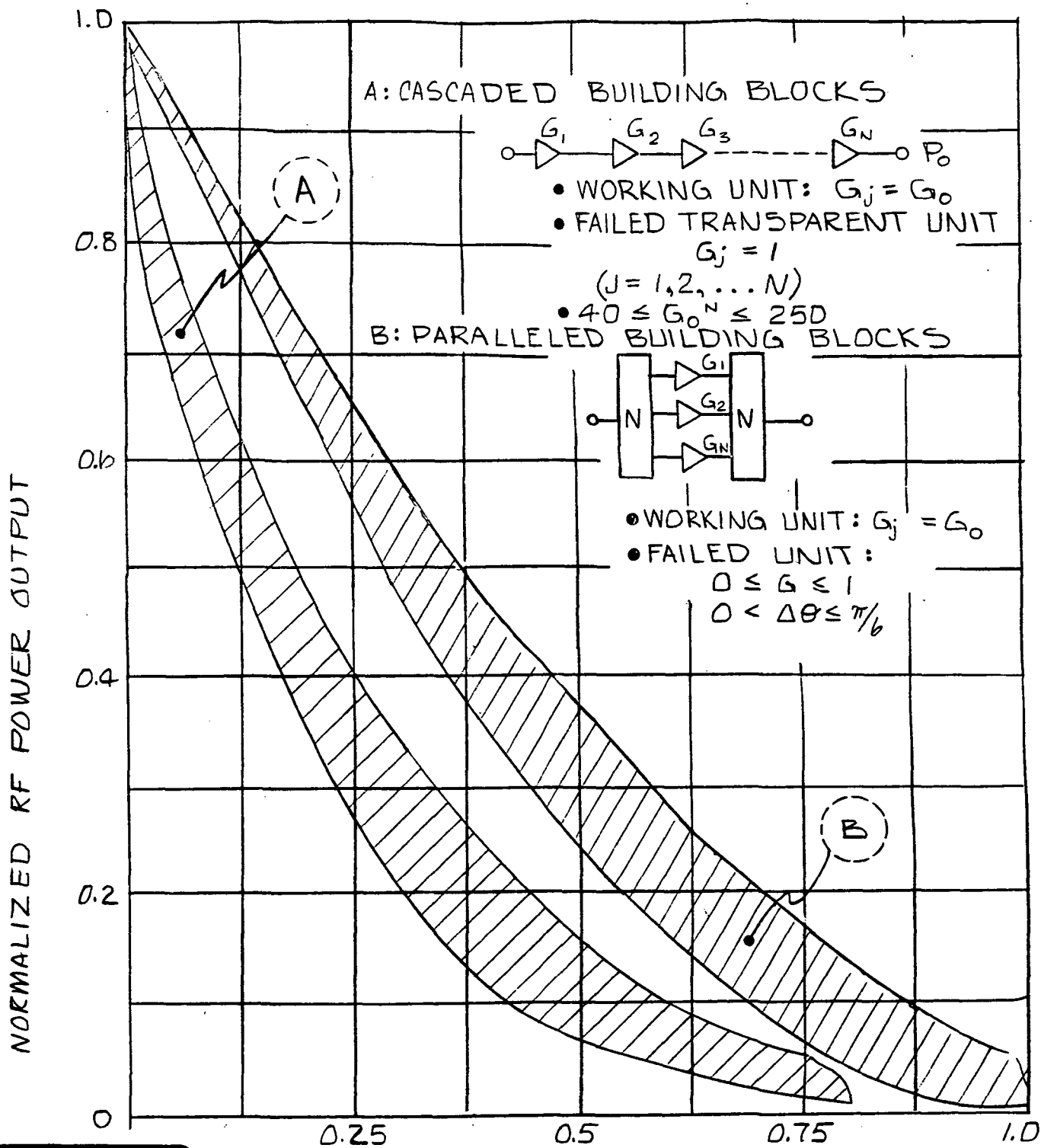
The primary tradeoffs impacting the selection of an optimum combinatorial postamplifier configuration for the IMPATT power section of the 20 GHz transmitter, involve the following alternatives:

- degree(N) of interstage combining (between N-way power divider and combiner) for specified 20W total output capability.
- type of N-way divider/combiner topology:

The major considerations entering into the foregoing tradeoffs, in turn, are:

- assessment of the maximum power output capability, (perhaps using a degree of intrastage device combining) practically achievable in each of the paralleled "building blocks"
- apportionment of the total degree of device combining required to achieve the required overall RF output power between intrastage (within each building block) and interstage (paralleled building blocks) combining for best trade between graceful degradation capability and simplicity.
- geometric realizability in an N-way combiner/divider topology that minimizes residual insertion loss, phase imbalance, mismatch, etc., while concurrently being compatible with "building block" geometry.





FRACTION OF FAILED BUILDING BLOCKS (R/N)

GRACEFUL DEGRADATION CHARACTERISTICS  
 OF ALTERNATIVE POWER SECTION COMBINATORIAL  
 POST AMPLIFIERS

3.4.1 GRACEFUL DEGRADATION CHARACTERISTICS OF ALTERNATIVE  
POWER SECTION COMBINATORIAL POST-AMPLIFIERS

Two approaches to the accumulation of sufficient IMPATT devices within a combinatorial power section post amplifier to achieve the specified 20W total RF power output capability involve:

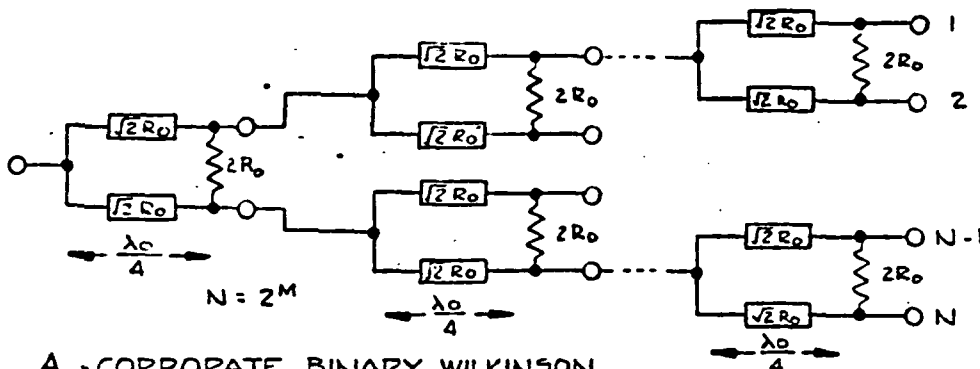
- cascading of successively higher power IMPATT stages, containing successively greater numbers of devices combined within end stages
- paralleling of identical "building blocks between N-way power divider and combiner.

The degradation in RF power output capability under random device failures occurs quite differently in each of the above configurations, e.g.:

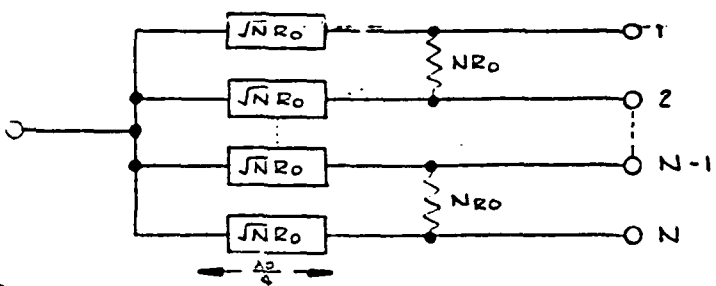
- failure of a single IMPATT device within a multiple-device, circulator-coupled IMPATT amplifier stage generally results in a sufficiently detuned and degraded gain response to require that the stage be shut down and effectively by-passed into a unity gain state by removal of DC bias current, so that failure of said device connotes failure of the amplifier stage, e.g., reduction of said stage gain to unity (less circulator loss).
- failure of an amplifier stage within a cascaded amplifier power section reduces the overall RF power output of the latter by, at worst, the nominal gain of that stage prior to failure.
- failure of an amplifier stage within one of N paralleled "building blocks" reduces the overall RF power output by at worst  $(N-1)/N^2$

Extension of the above to M failed stages shows that the paralleled power section generally exhibits about 3 dB less degradation than its completely cascaded counterpart.

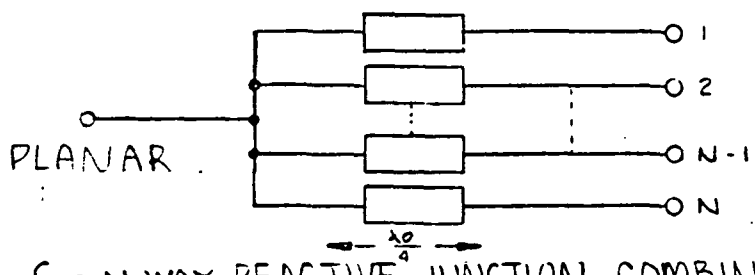




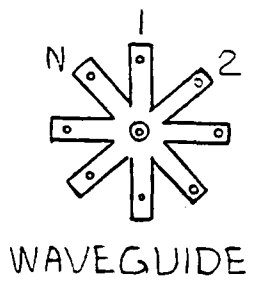
A. - CORPORATE BINARY WILKINSON COMBINING.



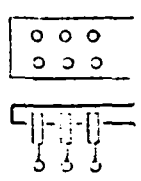
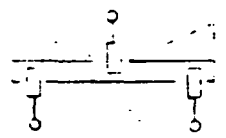
B. - N WAY WILKINSON COMBINING.



C. - N WAY REACTIVE JUNCTION COMBINING



RADIAL OR BICONICAL



WAVEGUIDE

D. REACTIVE EXTENDED INTERACTION CAVITY COMBINING



ALTERNATIVE POWER DIVIDER/COMBINER CONFIGURATIONS.

3.4.2 COMPARISON OF ALTERNATIVE 20 GHZ N-WAY POWER DIVIDER/COMBINER TOPOLOGIES

The relative merits of the various 20 GHz divider/combiner alternatives may be summarized as follows:

- . The corporate binary Wilkinson configuration, for  $N > 2$ , exhibits excessive size and residual insertion loss. Moreover the series balancing resistors are difficult to implement.
- . Generalization of the above to an N way Wilkinson configuration results in a more compact TEM transmission line implementation with moderately low residual insertion loss and port-to-port isolation. Implementation of the series balancing resistors remains difficult, however.
- . A reactive junction configuration exhibits low insertion loss but no inherent port to port isolation and hence is only useable with isolator coupled "building blocks", such as under consideration here. Within this category, the planar TEM junction is more compact and wider band but the waveguide junction exhibits the absolute minimum in insertion loss.
- . The extended interaction reactive cavity configuration exhibits low loss, and narrow (radial and waveguide) to wide (biconical) bandwidth, but may be more awkward with respect to interfacing with N "building blocks" than the above.
- . In all cases, orders of division recombination of  $N > 8$  are difficult to implement.

Based on the above, it is clear that, for accomodating circulator coupled IMPATT "building blocks", the reactive waveguide junction and biconical extended interaction cavity configurations seem most suitable.



POWER SECTION COMBINATORIAL TRADEOFF RESULTS

| <u>TRADEOFF</u>  | <u>PREFERRED APPROACH</u>   | <u>RATIONALE</u>  |
|--|---|---|
| <p>1. CASCADE VS. PARALLELED APPROACH TO RF POWER ACCUMULATION</p> <p>2. ORDER (N) OF POWER DIVIDER/COMBINER</p>   | <p>COMPOSITE:</p> <ul style="list-style-type: none"> <li>• 5-6W "BUILDING-BLOCKS"</li> <li>• 4TH ORDER PARALLELING</li> </ul> <p>N=4</p>  | <p>BEST TRADEOFF BETWEEN EFFICIENCY/SIMPLICITY AND GRACEFUL DEGRADATION</p> <ul style="list-style-type: none"> <li>• OPTIMUM DC/RF EFFICIENCY OF POWER SECTION (DEGRADED FOR <math>N &gt; 4</math>)</li> <li>• RESONABLE GRACEFUL DEGRADATION IN OUTPUT LEVEL FOR <math>m (\leq 4)</math> FAILED BUILDING-BLOCKS (<math>P_{om} = [(4-m)/4] P_o</math>)</li> <li>• POWER DIVIDER/COMBINER IMPLEMENTATION SIMPLE</li> </ul> |
| <p>3. TYPE OF RF POWER DIVIDERS/COMBINERS:</p> <ul style="list-style-type: none"> <li>• CORPORATE BINARY WILKINSON</li> <li>• N-WAY WILKINSON</li> <li>• N-WAY REACTIVE PLANAR JUNCTION</li> <li>• EXTENDED-INTERACTION CAVITY REACTIVE</li> </ul> | <p>EXTENDED-INTERACTION CAVITY REACTIVE</p> <ul style="list-style-type: none"> <li>• TEM/BICONICAL FOR WIDEBAND/LOW LOSS</li> <li>• CIRCULAR GEOMETRY MORE COMPATIBLE THAN WG WITH PREFERRED "BUILDING BLOCK" AMPLIFIER MOUNTING/HEAT SINKING GEOMETRY</li> </ul> | <ul style="list-style-type: none"> <li>• CORPORATE BINARY WILKINSON OF EXCESSIVE SIZE AND LOSS.</li> <li>• N-WAY WILKINSON USES DIFFICULT-TO-IMPLEMENT SERIES BALANCING RESISTOR.</li> <li>• EXTENDED INTERACTION CAVITY PROVIDES LOWER RESIDUAL INSERTION LOSS THAN REACTIVE JUNCTION.</li> </ul>  |





### 3.4.3 POWER SECTION COMBINATORIAL TRADEOFF RESULTS

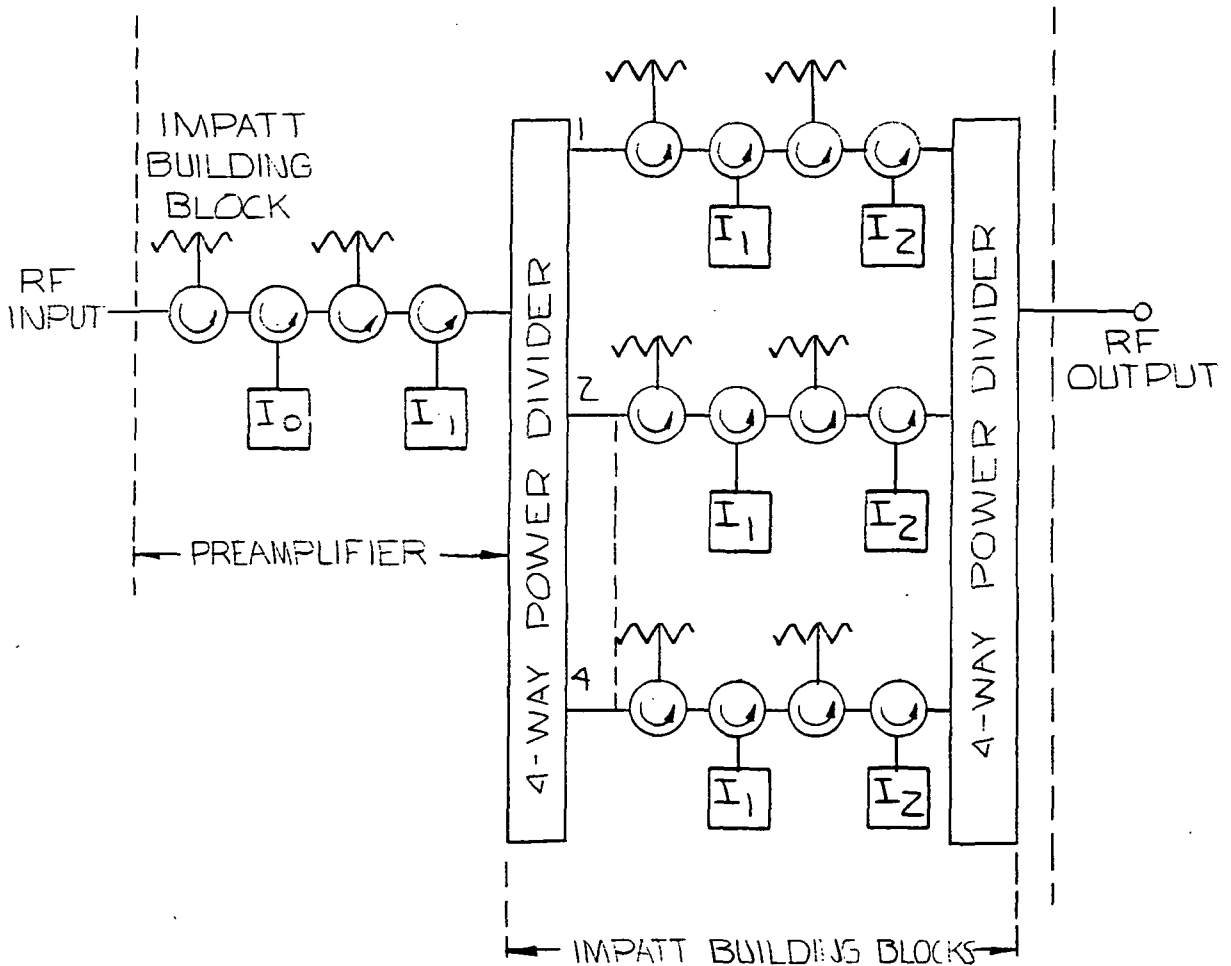
Based upon an assessment of the tradeoffs between IMPATT power section simplicity and graceful degradation capability and of the relative merits of alternative power divider/combiner configurations, it has been concluded that the preferred power section combinatorial postamplifier should utilize:

- 5 to 6W paralleled "building blocks", based upon maximum degree of practical intrastage device level combining
- N=4th order power division/recombination of paralleled "building blocks" for best trade between graceful degradation capability and size and simplicity
- waveguide junction or biconical extended interaction reactive 4-way divider/combiner, based upon low residual insertion loss, and compatibility with geometry of circulator coupled IMPATT "building blocks"

A final selection of the preferred four-way reactive divider/combiner configuration is made on the basis of the overall power section mechanical layout optimization.



# PREFERRED 20GHZ IMPATT POWER SECTION



$I_0 \approx 0.3 - 0.5 \text{ W}$  IMPATT MOUNT  
 $I_1 \approx 1.25 - 2 \text{ W}$  IMPATT MOUNT  
 $I_2 \approx 4 - 6 \text{ W}$  IMPATT MOUNT  
 IMPATT BUILDING BLOCKS  
 COMBINATORIAL POSTAMPLIFIERS  
PROJECTED CHARACTERISTICS

- RF OUTPUT LEVEL: 22.5 W (MIN)
- RF INPUT LEVEL: 20 mW (NOM)
- MODE OF OPERATION: STABLE AMPLIFIER
- OPERATING GAIN: 30.5 dB (MIN)
- DC BIAS POWER: 110 W (MAX)
- POWER-ADDED EFFICIENCY: 20.5 PERCENT (MIN)
- GAIN COMPRESSION RATIO: 0.016 dB/dB (NOM)
- AM-PM CONVERSION: 5.9 DEG/dB (MAX)
- NOISE FIGURE: 31 dB (NOM)

### 3.5 PREFERRED 20 GHz IMPATT POWER SECTION

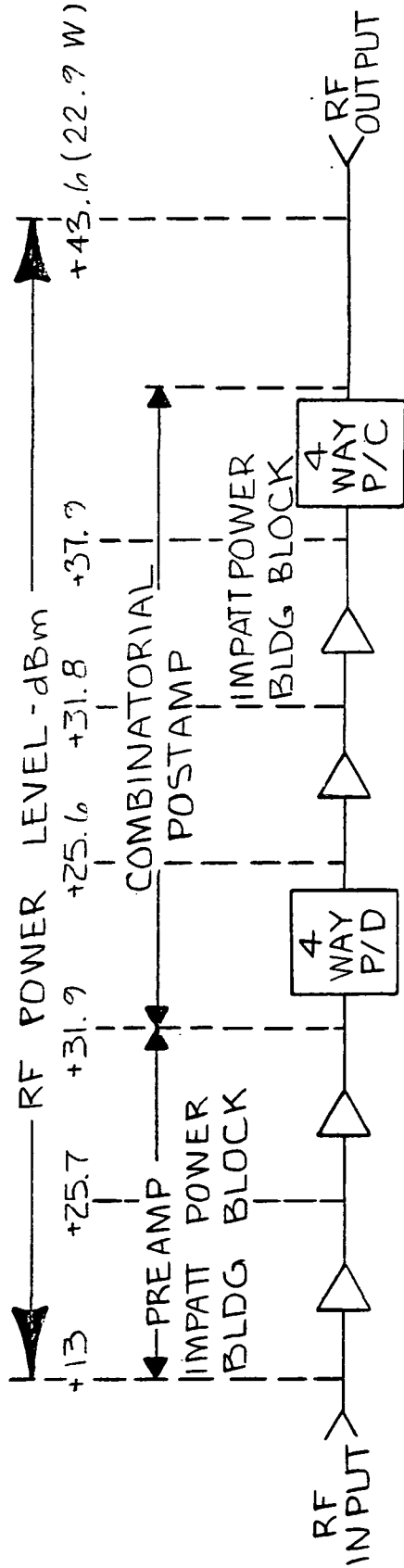
Based upon the results of the foregoing tradeoff analyses, the preferred 20 GHz IMPATT power section configuration comprises:

- . two stage circulator coupled IMPATT preamplifier utilizing single mesa 0.4W and 1.6W IMPATT devices in the stable amplifier input and output stages, respectively
- . four identical two stage circulator coupled IMPATT "building block" power amplifier, each providing 6.2W RF output capability, utilizing single mesa, 1.5W and four mesa 6.2W devices in the stable amplifier, input and output stages, respectively
- . identical four way reactive waveguide junction or biconical extended interaction RF power divider and combiner
- . all IMPATT stages operated in stable amplifier mode.

The projected performance characteristics of this IMPATT power section are, in general, consistent with the requirements on the overall 20 GHz transmitter.



PERFORMANCE BUDGET FOR PREFERRED 20GHz IMPATT POWER SECTION



| PARAMETER                                    | STAGE # |      |       |       | OVERALL ***                              |
|--|---------|------|-------|-------|--|
|  | 1       | 2    | 3     | 4     |  |
| GAIN - dB                                    | 12.7    | 6.2  | 6.2   | 6.1   | 30.6                                     |
| NOISE FIGURE dB                              | 30      | 30   | 30    | 30    | 31                                       |
| GAIN COMPRESSION RATIO - dB/dB               | 0.6     | 0.3  | 0.3   | 0.3   | 0.016                                    |
| AM/PM CONVERSION deg/dB                      | 2.4     | 4.2  | 4.2   | 4.2   | 5.9                                      |
| DC BIAS POWER - W                            | 5       | 5    | 20*** | 80*** | 110                                      |
| COMPOSITE DEVICE RF PWR ADDED CAPABILITY - W | 1.25    | 1.25 | 1.25  | 5     | —  |
| COMPOSITE DEVICE THERMAL RESISTANCE deg C/W  | 16      | 16   | 16    | 6     | —  |
| WORST CASE JUNCTION TEMPERATURE - °C         | 165     | 165  | 165   | 205   | *75°C BASE PLATE<br>*10°C (DIFFERENTIAL) |



\* INCLUDES CIRCULATOR LOSSES UNLESS OTHERWISE NOTED  
 \*\* INCLUDES LOSSES IN P/D AND P/C  
 \*\*\* TOTAL FOR 4 PARALLELED STAGES

### 3.5.1

#### PERFORMANCE BUDGET FOR PREFERRED 20 GHz IMPATT POWER SECTION

Based upon the previously presented power amplifier cascade formulations, the projected-stage-by-stage performance budget for the preferred IMPATT power section exhibits the following key features:

- Overall RF/DC power added efficiency of 20.8 percent based upon IMPATT device goal of 25 percent
- highly compressed RF power input/output transfer characteristic albeit with tolerable AM/PM conversion
- tolerable "worst case" device junction temperatures based upon reasonable IMPATT thermal resistance goals
- sufficient gain to satisfy overall 20 GHz transmitter gain requirement.

Based upon the above, it is clear that the role of the driver amplifier section preceding this power section is to provide a nominal amount of lower noise gain and thereby reduce the contribution of 31 dB power section noise figure sufficiently to satisfy the 25 dB overall transmitter noise figure requirement.



20 GHz DRIVER SECTION ALTERNATIVES

- TYPE OF DEVICE - FET VS. GaAs IMPATT DIODE
- MODE OF AMPLIFICATION - POSITIVE RESISTANCE TWO-PORT TRANSMISSION (FET) VS. CIRCULATOR COUPLED NEGATIVE RESISTANCE ONE PORT REFLECTION (IMPATT OR FET)
- TOTAL DRIVER GAIN AND LINEARITY,
- NUMBER OF CASCADED DRIVER STAGES
- APPORTIONMENT OF GAIN, NOISE FIGURE, AND LINEARITY PER STAGE TO ACHIEVE SPECIFIED 25 DB OVERALL TRANSMITTER NOISE FIGURE AT DRIVER SECTION GAIN LEVEL DICTATED BY SELECTION OF PREFERRED POWER SECTION.



### 3.6 20 GHz DRIVER SECTION ALTERNATIVES

The general 20 GHz driver section design alternatives include:

- type of device (FET vs. GaAs IMPATT)
- mode of amplification (positive resistance two-port transmission versus circulator-coupled negative resistance one-port reflection.
- total driver gain, linearity and noise figure, as dictated by characteristics of preferred power section design.
- number of driver stages and apportionment of performance among stages.

Based upon the previously presented preferred power section design, however, it is clear that the driver section need only provide a nominal ( $\sim$  8-10 dB) amount of relatively moderate noise figure ( $\leq$  20 dB) gain to meet the overall transmitter noise figure requirement. This greatly simplifies the driver section tradeoffs and makes the selection of preferred configuration less critical.



DRIVER SECTION TRADEOFF RESULTS



| TRADEOFF   | PREFERRED APPROACH  | RATIONALE   |
|--|---|---|
| <p>1. TYPE OF DEVICE</p> <ul style="list-style-type: none"> <li>. GaAs FET ONLY</li> <li>. GaAs READ/IMPATT ONLY</li> <li>. COMPOSITE FET/IMPATT</li> </ul>  | <p>ALL FET*<br/>(REQUIRED IN ORDER TO MEET NOISE PERFORMANCE REQUIREMENT)</p>                                 | <ul style="list-style-type: none"> <li>. FET PROVIDES:                             <ul style="list-style-type: none"> <li>- LOWER NOISE FIGURE</li> <li>- LOWER DC POWER DRAIN</li> <li>- LOW/MODERATE GAIN/STAGE</li> </ul> </li> <li>. IMPATT PROVIDES                             <ul style="list-style-type: none"> <li>- HIGHER GAIN/STAGE</li> <li>- TRANSPARENT OPERATION UNDER DEVICE FAILURE</li> </ul> </li> </ul>  |
| <p>2. AMPLIFIER STAGE TOPOLOGY</p> <ul style="list-style-type: none"> <li>. TWO-PORT POSITIVE RESISTANCE (+R) TRANSMISSION</li> <li>. ONE-PORT CIRCULATOR-COUPLED NEGATIVE-RESISTANCE (-R) REFLECTION</li> </ul> | <p>TWO-PORT COMMON SOURCE FET*</p>  | <ul style="list-style-type: none"> <li>. TWO-PORT +R                             <ul style="list-style-type: none"> <li>- APPLIES ONLY TO FET</li> <li>- SMALLER/LIGHTER</li> <li>- LIMITED GAIN/STAGE</li> <li>- MORE AMENABLE TO MULTIPLE DEVICES</li> </ul> </li> <li>. ONE PORT -R                             <ul style="list-style-type: none"> <li>- FET OR IMPATT</li> <li>- UNLIMITED GAIN UNDER WELL DEFINED GAIN-BW CONSTRAINTS</li> <li>- MAY EXHIBIT (USING FET) DEGRADED BW, NOISE FIGURE OR POWER OUTPUT</li> <li>- TRANSPARENT UNDER ACTIVE DEVICE FAILURE</li> </ul> </li> </ul> |
| <p>3. FET TWO PORT AMPLIFIER TOPOLOGY</p> <ul style="list-style-type: none"> <li>. SINGLE-ENDED</li> <li>. BALANCED</li> </ul>   | <ul style="list-style-type: none"> <li>. SINGLE-ENDED INPUT STAGE</li> <li>. OTHER STAGES BALANCED</li> </ul> | <ul style="list-style-type: none"> <li>. SINGLE-ENDED CONFIGURATION PROVIDES:                             <ul style="list-style-type: none"> <li>- SLIGHTLY HIGHER GAIN</li> <li>- SMALLER, LIGHTER, LOWER PARTS COUNT</li> </ul> </li> <li>. BALANCED-CONFIGURATION PROVIDES:                             <ul style="list-style-type: none"> <li>- HIGHER RF POWER INPUT/OUTPUT</li> <li>- ADDITIONAL DEGREE OF INPUT / OUTPUT MATCHING CAPABILITY</li> </ul> </li> </ul>  |



### 3.6.1 DRIVER SECTION TRADEOFF SUMMARY

A summary of the tradeoff results obtained in evolving a preferred approach to the 20 GHz driver section, in light of the relatively modest requirement on driver performance ( $\lesssim 10$  dB gain,  $\lesssim 20$  dB noise figure) is as follows:

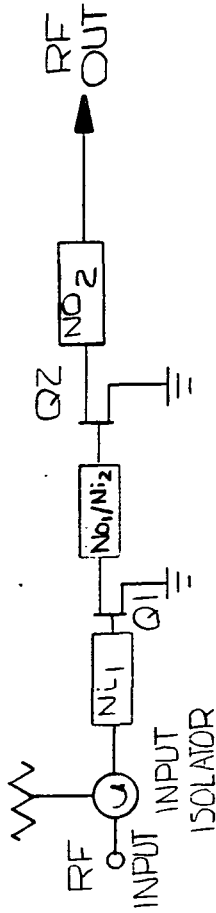
- all FET driver necessary in order to meet noise performance requirements
- two-port common-source FET stages preferred due to better noise performance and linearity
- single ended stages preferred due to their simplicity and lower parts count.

Based upon the relatively modest RF gain and power output capability imposed upon the driver section by the previously described preferred IMPATT power section design, it is concluded that a two-stage single-ended common source FET driver amplifier with integral input isolator is the simplest and most appropriate design approach.



PREFERRED 20GHz FET DRIVER SECTION

STAGE #1 STAGE #2



FET SELECTION

Q1, Q2 MP (~60mW) DEVICES

| STAGE NO. (j=1,2)                              | 1    | 2    | OV   |
|--|------|------|------|
| #FETS / STAGE                                  | MP   | MD   | -    |
| FET TYPE                                       |      |      |      |
| RF OUTPUT POWER - P <sub>o j</sub> - dBm       | 8.5  | 13   | 13   |
| RF INPUT POWER - P <sub>in j</sub> - dBm       | 4.0  | 8.5  | 4.75 |
| GAIN: 10 log <sub>10</sub> G <sub>j</sub> - dB | 4.5  | 4.5  | 8.75 |
| COMP. RATIO: CR <sub>j</sub> - dB/dB           | 1    | 1    | 1    |
| AM/PM: k <sub>o j</sub> deg/dB                 | 0    | 0    | 0    |
| NF: 10 log <sub>10</sub> F <sub>j</sub> - dB   | 6    | 6    | 8.1  |
| DC POWER DRAIN - W                             | 0.15 | 0.15 | 0.3  |
| COMPOSITE THERMAL RESISTANCE - °C/W            | 160  | 160  | -    |
| WORST CASE CHANNEL TEMPERATURE - °C *          | 109  | 109  | -    |

PROJECTED CHARACTERISTICS

- RF OUTPUT LEVEL: 20mW (MIN)
- RF INPUT LEVEL: 2.7mW (NOM)
- OPERATING GAIN: 8.75 dB (MIN)
- NOISE FIGURE: 8.1 dB (NOM)
- GAIN COMPRESSION RATIO: 1.0 dB/dB
- AM/PM CONVERSION: 0 deg/dB
- DC BIAS POWER: 0.3 W

\* 75°C BASEPLATE, 10°C CASE TO BASEPLATE DIFFERENTIAL



### 3.6.2

#### PREFERRED 20 GHz FET DRIVER SECTION

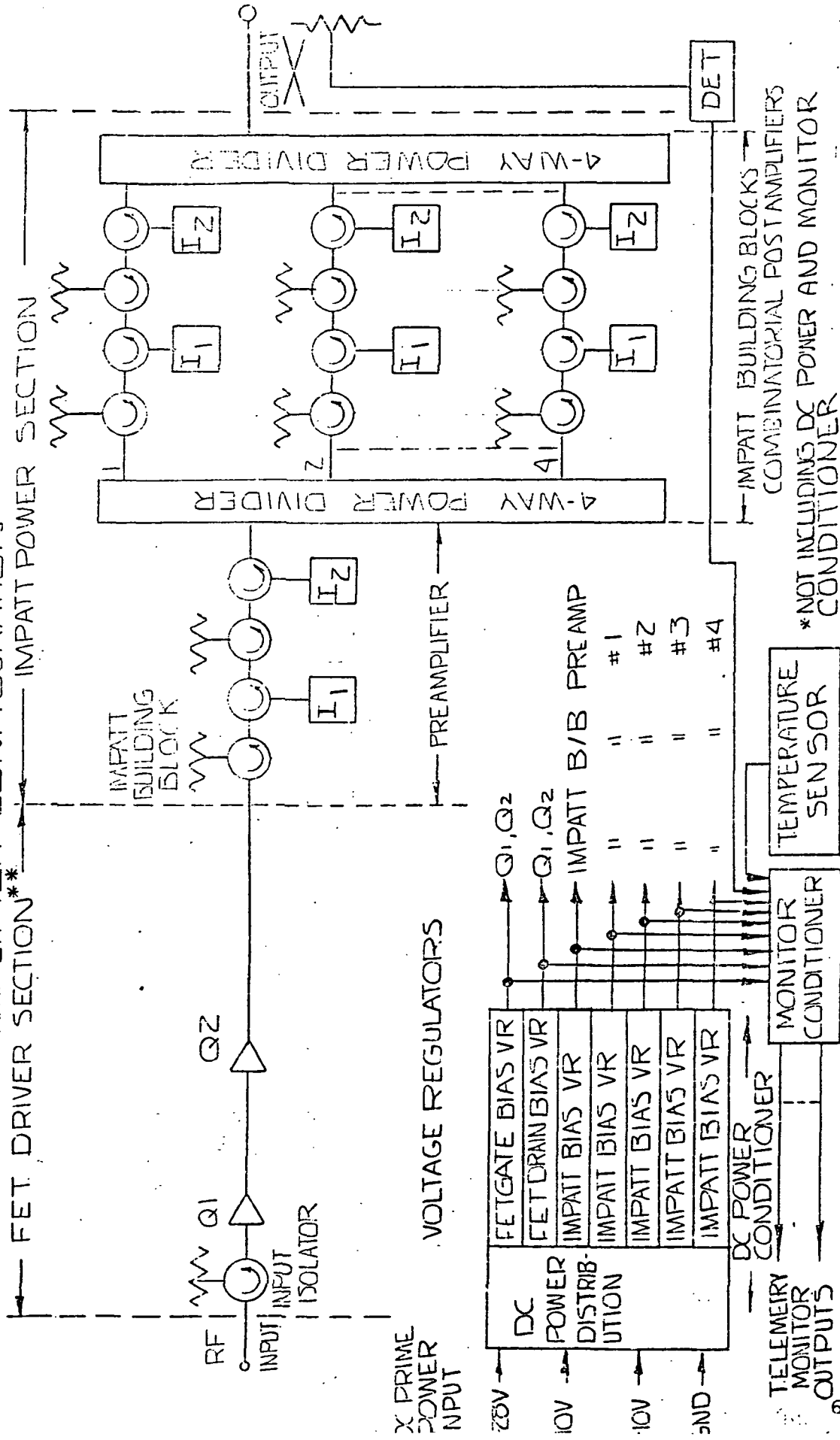
Based upon the results of the foregoing tradeoff analysis the preferred 20 GHz FET driver section comprises two cascaded single-ended common source two-port FET stages, preceded by a terminated circulator which serves as an input isolator. Each single-ended stage utilizes a medium power FET which exhibits moderately low noise figure at 20 GHz. A stage-by-stage performance budget for this driver amplifier demonstrates that it provides sufficient operating gain capability ( $\sim 9$  dB) to adequately suppress the noise figure contribution of the IMPATT power section that follows it so as to make possible the satisfaction of the overall transmitter noise figure requirement without adversely impacting the linearity of the overall transmitter.



4.0 PRELIMINARY DESIGN SPECIFICATION



PREFERRED 20 GHz TRANSMITTER  
AMPLIFIER CONFIGURATION



- PROJECTED CHARACTERISTICS
- RF OUTPUT LEVEL: 22.5 W (MIN)
  - POWER-ADDED EFFICIENCY: 20.4 PERCENT (MIN)\*
  - RF INPUT LEVEL: 2.7 W (NOM)
  - GAIN COMPRESSION: 0.016 dB/dB (MAX)
  - OPERATING GAIN: 39.3 dB (NOM)
  - AM/PM CONVERSION: 5.9 DEG/dB (MAX)
  - DC PRIME POWER: 120 W (MAX)\*
  - NOISE FIGURE: 22.5 dB (NOM)
- \* \* IF NF SPECIFICATION IS RELAXED TO 32dB, DRIVER SECTION CAN BE ELIMINATED

\* NOT INCLUDING DC POWER AND MONITOR CONDITIONER

IMPATT BUILDING BLOCKS  
COMBINATORIAL POST AMPLIFIERS

#### 4.1

##### PREFERRED 20 GHZ TRANSMITTER CONFIGURATION

Based upon the results of the foregoing tradeoff analysis, the preferred 20 GHz IMPATT transmitter configuration consists of:

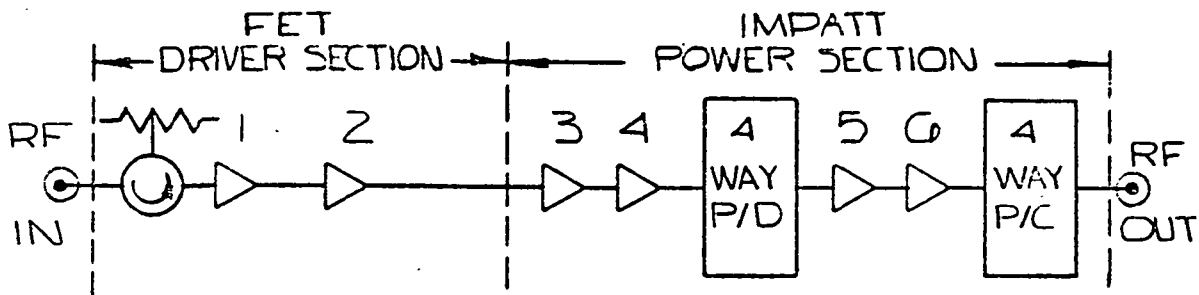
- IMPATT power section comprising two stage circulator coupled IMPATT pre-amplifier cascaded with a four-way combinatorial postamplifier formed by four paralleled two-stage IMPATT "building block" amplifiers, paralleled between identical four way reactive power divider and combiner
- two stage single-ended common source FET driven amplifier with integral input isolator
- DC power conditioner, comprising power distribution network coupled to individual DC bias voltage regulators for FET driver amplifier and for each two stage IMPATT "building block."
- monitor conditioner providing analog DC outputs which are linearly related to key transmitter operating parameters, e.g., secondary DC bias voltages and currents, RF power level, physical temperature, etc.

This design assumes that the required primary DC input voltages are provided from a central spacecraft DC/DC conversion subsystem, such as often is done for maximum efficiency, in practical spacecraft deployments. (Alternately, a dedicated DC/DC converter, operating off a single +28V prime input bus, can be incorporated in the transmitter DC power conditioning subassembly).

This design can be expanded to provide redundancy at the overall transmitter assembly level or internally by providing RF switch-coupled FET driver/IMPATT preamplifier or DC switch-coupled power conditioner pairs. The degree of redundancy required is dependent upon a detailed set of reliability predictions encompassing all of the major transmitter subassemblies as well as an assessment of the degree of transmitter performance degradation which constitutes a failure in the intended spacecraft usage.



# PERFORMANCE BUDGET FOR PREFERRED 20 GHz IMPATT TRANSMITTER CONFIGURATION



| STAGE   | 1    | 2    | 3    | 4    | 5     | 6     | OVERALL |
|---|------|------|------|------|-------|-------|---------|
| GAIN - dB *   | 4.5  | 4.5  | 12.7 | 6.2  | 6.2   | 6.1   | 39.3*   |
| RF OUTPUT POWER - dB*                               | 8.5  | 13   | 25.7 | 31.9 | 31.8  | 37.9  | 43.6*   |
| GAIN COMPRESSION RATIO - dB/dB                      | 1.0  | 1.0  | 0.6  | 0.6  | 0.6   | 0.6   | 0.016   |
| AM/PA (CONVERSION) - deg/dB                         | 0    | 0    | 2.4  | 4.2  | 4.2   | 4.2   | 5.9     |
| COMPOSITE DEVICE RF POWER ADDED CAPABILITY - W      | 0.04 | 0.04 | 1.25 | 1.25 | 1.25  | 5     | -       |
| NOISE FIGURE - dB**                                 | 6    | 6    | 30   | 30   | 30    | 30    | 22.5*   |
| DC POWER DRAIN - W ***                              | 0.15 | 0.15 | 5    | 5    | 20*** | 80*** | 103     |
| COMPOSITE THERMAL RESISTANCE - °C/W                 | 160  | 160  | 16   | 16   | 16    | 6     | -       |
| WORST CASE **** DEVICE ACTIVE REGION TEMPERATURE °C | 109  | 109  | 165  | 165  | 165   | 205   | -       |

\* INCLUDES LOSSES IN P/D P/C CIRCULATORS AND INTERCONNECTS (0.3 dB ea)

\*\* NOT INCLUDING DC VOLTAGE REGULATORS, ETC.

\*\*\* TOTAL FOR 4 PARALLELED STAGES

\*\*\*\* 75°C BASEPLATE AND 10°C BASEPLATE / CASE DIFFERENTIAL

IF NOISE FIGURE SPECIFICATION IS RELAXED TO 32 dB, DRIVER SECTION CAN BE ELIMINATED.



#### 4.2 PERFORMANCE BUDGET FOR PREFERRED 20 GHz IMPATT TRANSMITTER CONFIGURATION

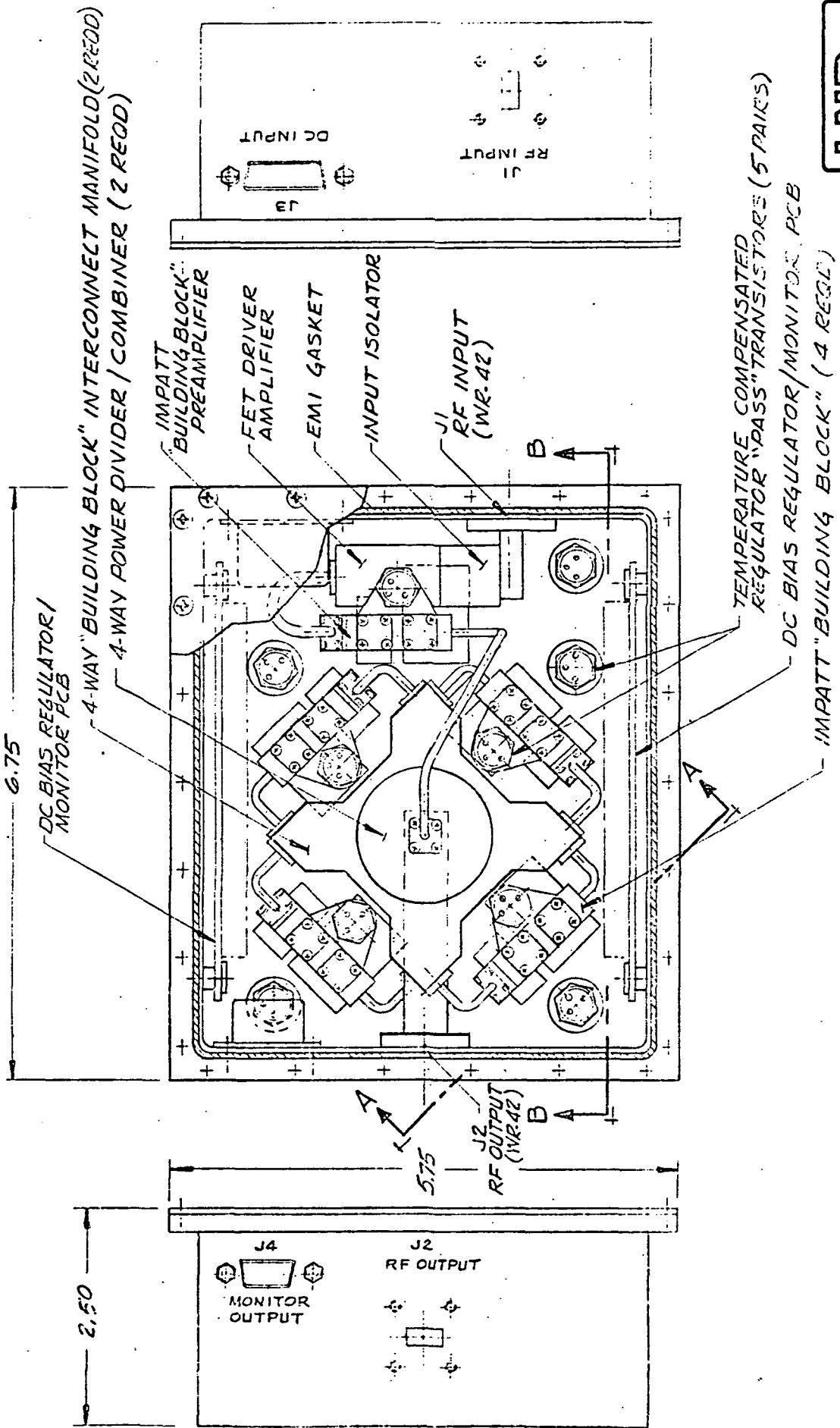
Based upon a composite of the previously presented preferred power and driver section performance budgets, that governing the overall transmitter design exhibits the following key features:

- Four-way combinatorial IMPATT power section which by itself exceeds the 30 dB gain, 20WRF power output and 20 percent DC/RF power added efficiency requirements on the overall 20 GHz transmitter.
- Simple two-stage FET driver amplifier section, providing sufficient gain (~9 dB) to adequately reduce the contribution of the 32 dB noise figure IMPATT power section to overall transmitter noise figure to maintain the latter below the specified 25 dB.
- Tolerable AM/PM conversion within specified 6 deg/dB maximum, coupled with highly saturated input/output amplitude transfer characteristic.
- Realizeable device junction (or channel)-to-housing thermal resistances, resulting in tolerable maximum junction or channel temperatures at maximum base-plate temperature.

It is clear from the above that if the overall transmitter noise figure specification is relaxed to 32 dB, the FET driver section can be eliminated from the transmitter.







CONCEPTUAL LAYOUT OF 20 GHz IMPATT TRANSMITTER



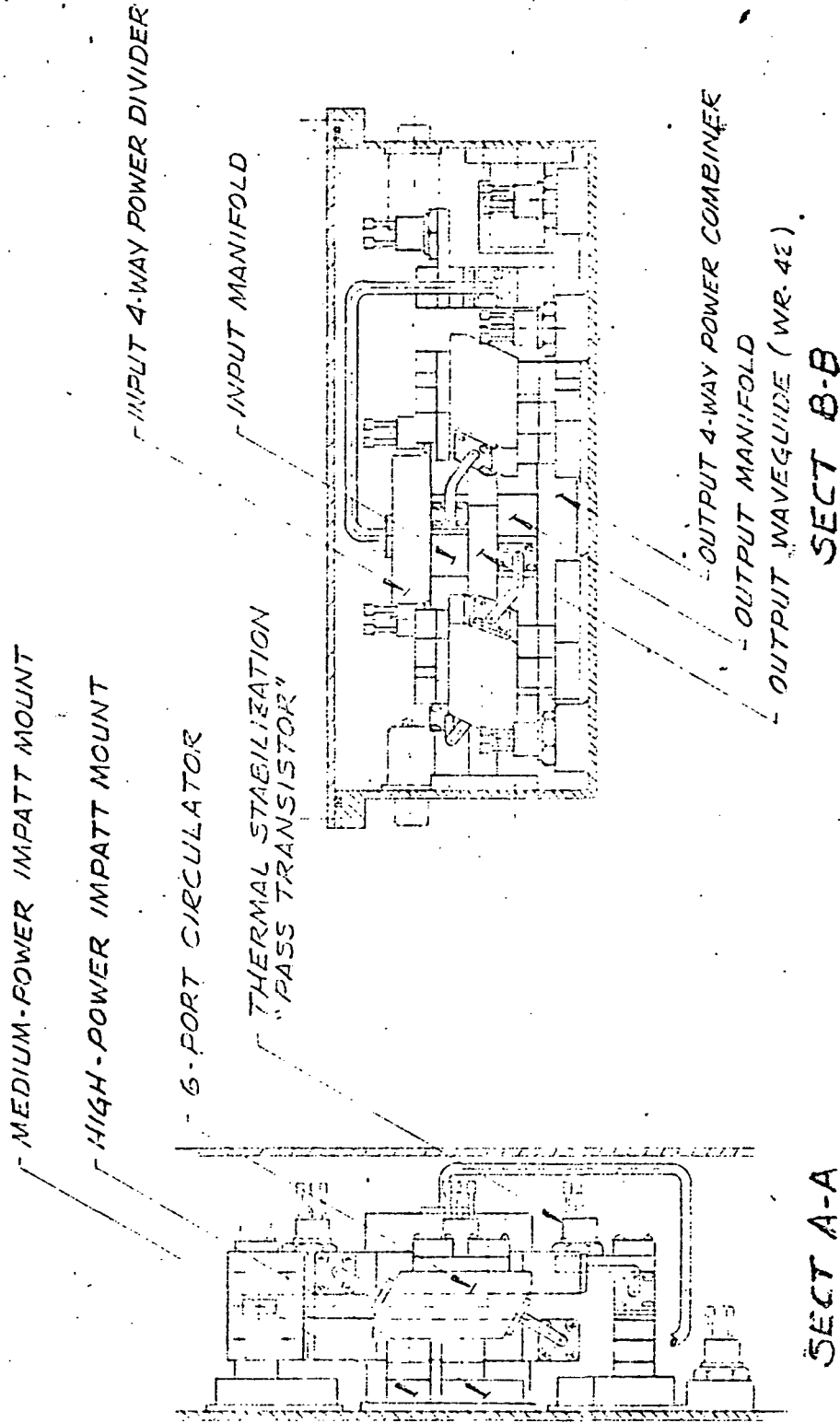
#### 4.3 CONCEPTUAL LAYOUT OF 20 GHZ IMPATT TRANSMITTER

The preferred 20 GHz IMPATT transmitter amplifier design is mechanically packaged as a compact closely integrated highly modular structure wherein the overall assembly is formed as the direct inter connection of the following self contained replaceable modules:

- Two stage power section circulator coupled IMPATT amplifiers implemented as integrated four-junction dielectrically loaded stripline circulator structures to the active ports of the second and fourth junction to which are directly coupled the TEM-line IMPATT amplifier mounts each containing a single or paralleled pair of hermetically sealed stud mounted IMPATT (diode(s)). The first and third junctions of each circulator comprise input and interstage isolators having their respective isolated ports match-terminated with directly integrated customized miniature 20 GHz terminations, configured in-house to withstand the required RF dissipation levels.
- Four paralleled two stage IMPATT amplifier "building blocks" comprising the power module combinatorial postamplifier are mounted vertically and symmetrically disposed around the periphery of parallel horizontal 4-way radial input power divider and output power combiner, the latter affixed to the transmitter baseplate and the former elevated.
- Power section input two-stage IMPATT preamplifier and combinatorial postamplifier "building blocks" are affixed to the transmitter baseplate IMPATT mount-sidedown such that the stud mounted IMPATT diodes are in intimate thermal contact with said baseplate.
- Driver section two stage FET amplifier, implemented in duroid-substrate-based microstrip transmission line with self contained, stripline terminated circulator input isolator integrated within same baseplate-mounted housing.
- Miniaturized PC card DC bias postregulators comprising DC power conditioner incorporated in close proximity to corresponding amplifier stages, each of which utilize PC card mounted, hermitically sealed "flatpack" functional IC's and discrete "pass" transistors which are affixed to the transmitter baseplate for better heat sinking.
- PC card based monitor conditioner utilizing functional IC's to derive required DC analog outputs, incorporated directly on associated voltage regulator cards where applicable.

In addition to the above, the overall transmit amplifier enclosure includes a shielded compartment containing EMI filters for the DC power inputs and telemetry monitor outputs.





CROSS SECTIONAL LAYOUT OF 20 GHZ IMPATT TRANSMITTER

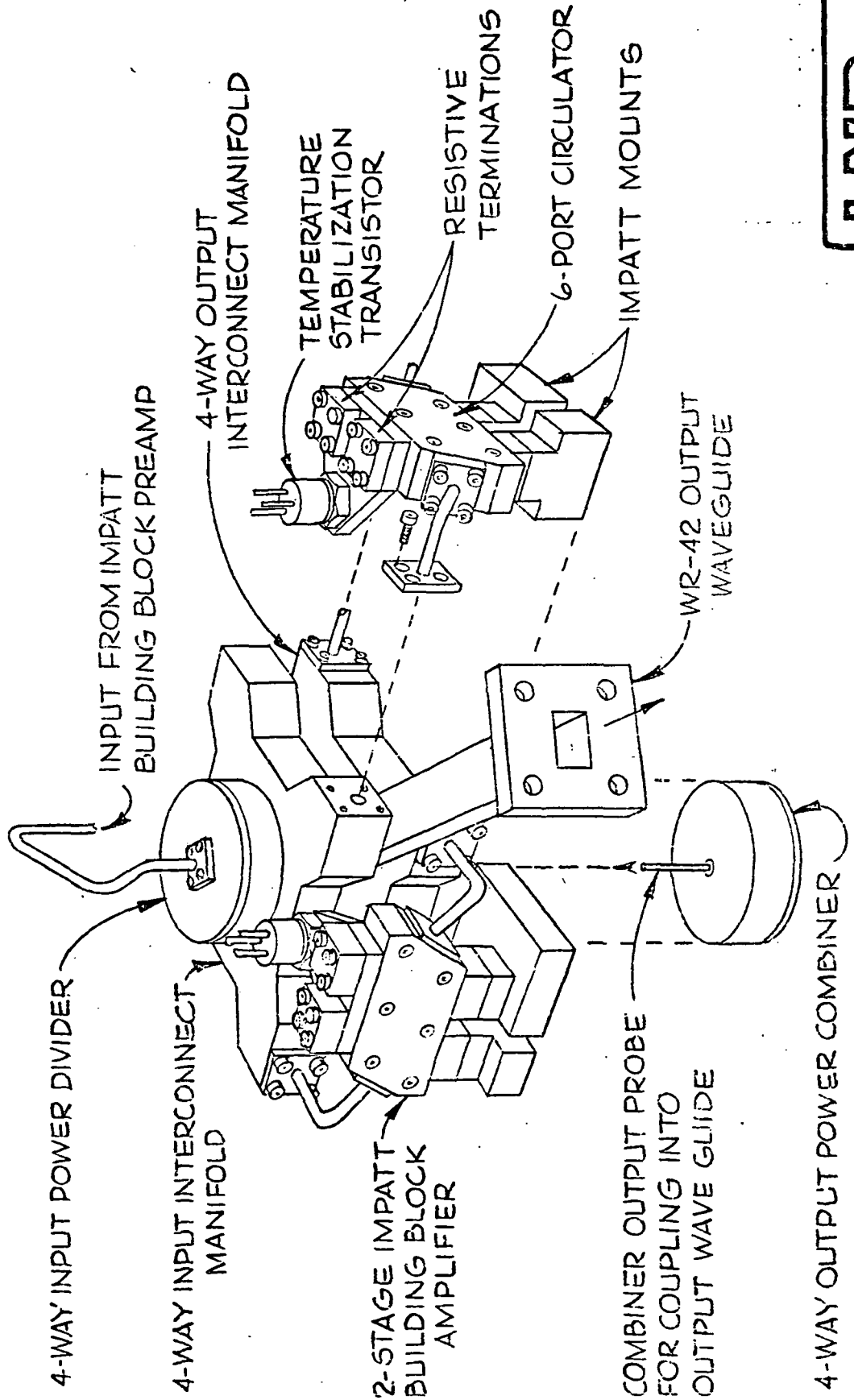


PROJECTED WEIGHT BUDGET FOR PREFERRED  
20 GHz IMPATT TRANSMITTER DESIGN

| <u>COMPONENT (QUANTITY)</u>                  | <u>WEIGHT (oz.)</u> |
|--|---------------------|
| . IMPATT POWER "BUILDING BLOCKS" (5)         | 16.8                |
| . FET DRIVER AMPLIFIER (1)                   | 1.5                 |
| . POWER DIVIDER/COMBINER (2)                 | 4.4                 |
| . INPUT ISOLATOR (1)                         | 1.2                 |
| . WG/TEM TRANSDUCERS (2)                     | 2.1                 |
| . DC POWER/MONITOR CONDITIONER PCB (2)       | 5.0                 |
| . IMPATT REGULATOR PASS TRANSISTORS (10)     | 2.0                 |
| . WIRING, ETC                                | 0.8                 |
| . DC POWER, MONITOR CONNECTORS               | 0.6                 |
| . EMI FILTERS                                | 1.8                 |
| . INTERNAL CONNECTORS, TRANSDUCERS AND CABLE | 1.8                 |
| . HOUSING AND COVER                          | 16.0                |
| . STRUCTURE AND HARDWARE                     | 5.0                 |
|  | <hr/>               |
| TOTAL  | 59.0 oz (3.7 lbs)   |



EXPLODED VIEW OF IMPATT POWER SECTION  
 COMBINATORIAL POSTAMPLIFIER



#### 4.4 PACKAGING FEATURES OF 20 GHz IMPATT TRANSMITTER

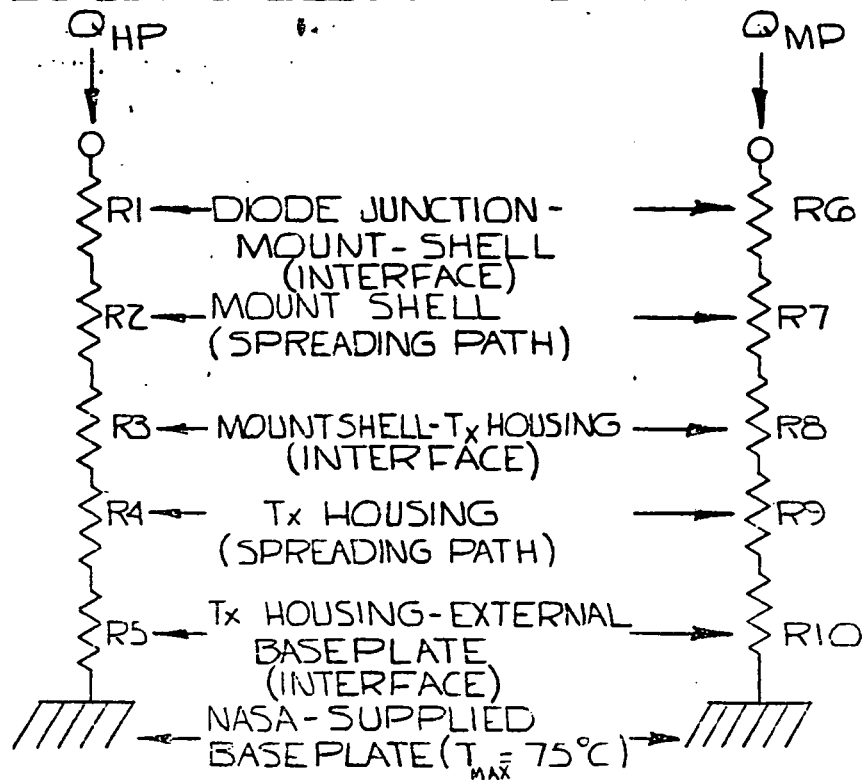
Additional features of the physical packaging concept underlying the preferred transmitter design include:

- Two identical four-way biconical reactive power divider/combiners, directly integrated with the four associated paralleled IMPATT "building blocks" through low loss strip-line interconnect manifolds.
- Directly integrated TEM/waveguide transducers coupled to input and output WR-42 waveguide RF interfaces, in driver and power modules, respectively.
- Modular construction wherein self-contained replaceable driver section and power section ("building blocks"), DC power conditioner, and monitor conditioner, are incorporated as individual prealigned modules prior to embedding in the master transmitter enclosure. This modular approach enhances RF performance, ease of assembly, integrability and reliability with negligible impact upon size and weight.
- Elimination, where possible, of internal RF connectors and superfluous transmission line lengths, thereby enhancing reliability and mechanical integrity as well as electrical performance. Direct transmission line interconnections between microwave components and hard-wired DC interfaces will be used in lieu of internal connectors.
- Partitioned housing machined from solid aluminum stock, thereby providing maximum degree of mechanical rigidity consistent with minimized weight, as best tradeoff between selective "lightening" for weight reduction and "stiffening" for immunity to severe vibrational environments.
- Hermetically sealed and passivated heat sunk semiconductor devices avoid necessity for sealing at the compartment or component level and promote greater reliability by minimizing device temperature.

The overall transmitter package design is of approximate dimensions 6.75" x 5.75" x 2.5", and will weigh about 3.7 lbs.



# "WORST CASE" THERMAL ANALYSIS OF IMPATT "BUILDING-BLOCK" AMPLIFIER



| MOUNT                         | THERMAL PATH | THERMAL RESISTANCE °C/W | TEMP. RISE ΔT ABOVE BASEPLATE °C | MAXIMUM TEMP. T(°C) |
|-------------------------------|--------------|-------------------------|----------------------------------|---------------------|
| HIGH-POWER<br>$Q_{HP} = 20W$  | R1           | 6                       | 120                              | 203 *               |
|                               | R2           | 0.14                    | 2.8                              | 83                  |
|                               | R3           | 0.1                     | 2.0                              | 80.2                |
|                               | R4           | 0.02                    | 0.4                              | 78.2                |
|                               | R5           | 0.14                    | 2.8                              | 77.8                |
| MEDIUM POWER<br>$Q_{MP} = 5W$ | R6           | 16                      | 80                               | 162.3 *             |
|                               | R7           | 0.77                    | 3.85                             | 82.3                |
|                               | R8           | 0.27                    | 1.35                             | 78.5                |
|                               | R9           | 0.06                    | 0.3                              | 77.1                |
|                               | R10          | 0.36                    | 1.8                              | 76.8                |

\* "WORST-CASE" IMPATT DIODE JUNCTION TEMPERATURE.

#### 4.5 THERMAL ASPECTS OF 20 GHZ IMPATT TRANSMITTER DESIGN

The thermal aspects of the 20 GHz IMPATT transmitter design are based upon the following general principles:

- Mounting of all high dissipation components in intimate thermal contact with overall enclosure baseplate.
- Use of high thermal conductance interfaces between individual module baseplates and overall enclosure baseplate.
- Maintenance of short length, large area thermal conductance paths of high conductance materials.
- Optimum spreading in thermal paths to minimize baseplate thermal density.

The net result of this design approach is that, in this transmitter packaging concept all dissipative component temperatures are confined to less than 10°C above the enclosure baseplate, with the exception of the 20 GHz FET's and IMPATT's. Moreover, the dissipative elements are widely distributed on the enclosure baseplate so that the average thermal density presented to the baseplate mounting interface is low,

The "worst case" transmitter device junction temperatures are those experienced by the high and medium power IMPATT diodes in the absence of RF drive, under which condition all of the IMPATT diode DC bias power is dissipated. In this case, under maximum baseplate (thermal interface) temperature of 75°C, the high and medium power IMPATT junction temperatures are 203°C and 162°C, respectively.





PROJECTED CHARACTERISTICS OF PREFERRED

20 GHz IMPATT TRANSMITTER DESIGN

|  |   |
|--|---|
| CENTER FREQUENCY                             | 19.95 GHz   |
| -1 dB BANDWIDTH (MIN.)                       | 700 MHz (19.6-20.3 GHz)   |
| RF POWER OUTPUT (MIN.)                       | 22.5W   |
| OPERATING GAIN (NOM.)                        | 39 dB   |
| RF/DC POWER-ADDED EFFICIENCY(MIN.)           | 20.4 PERCENT (EXCLUDING DC POWER/<br>MONITOR CONDITIONER)           |
| AM/PM CONVERSION (MAX.)                      | 5.9 deg/dB  |
| INPUT/OUTPUT VSWR (MAX.)                     | 1.25:1  |
| GAIN VARIATION VS FREQUENCY @<br>FIXED DRIVE | 1.0 dB p-p  |
| PHASE LINEARITY (MAX.)                       | 10 deg p-p  |
| GAIN SLOPE (MAX.)                            | 0.1 dB/MHz  |
| PASSBAND GROUP DELAY VARIATION (MAX.)        | 0.5 nS/50 MHz   |
| SPURIOUS OUTPUTS (MAX.)                      |   |
| . HARMONIC COMPONENTS                        | -50 dBc   |
| . NON HARMONIC COMPONENTS                    | -60 dBc   |
| NOISE FIGURE (MAX.)                          | 23 dB   |
| DC PRIME INPUT POWER-(MAX.)                  | 110.3W-EXCLUDING DC POWER/MONITOR<br>CONDITIONER                    |
| WEIGHT                                       | 120W - OVERALL<br>3.7 lbs.  |
| DIMENSIONS                                   | 6.75"x5.75"x2.5"  |
| BASEPLATE TEMPERATURE RANGE                  | 0-75°C  |
| MAXIMUM DEVICE JUNCTION TEMPERATURE:         | 205°C (IMPATT)<br>109°C (FET)                                       |
| RF INPUT/OUTPUT INTERFACES (J1/J2)           | WR-42 W/G- UG595/UG 595/U COVER FLANGE<br>+28 VDC, +10 VDC, -10 VDC |
| DC INPUT POWER INTERFACE                     | -ITT CANNON DEMA TYPE CONNECTOR                                     |
| TELEMETRY MONITOR OUTPUT INTERFACE           | ITT CANNON DAMA TYPE CONNECTOR                                      |



#### 4.6 PROJECTED CHARACTERISTICS OF PREFERRED 20 GHz IMPATT TRANSMITTER DESIGN

The preferred 20 GHz IMPATT transmitter design described herein meets or exceeds all of the previously enumerated specific design and performance requirements on the subject program. In particular, some of the key characteristics of this preferred design include the following:

- RF power output at nominal operating point: 22.5W (+43.5 dBm min.), as compared to 20W requirement.
- -1 dB bandwidth: 700 MHz (min.), as compared to 500 MHz requirement), by virtue of inherently wideband design.
- Operating gain: 39 dB (nom.), as compared to 30 dB requirement. Note that the latter could be satisfied by use of the IMPATT power section alone, with the 9 dB additional FET driver section gain being provided to sufficiently suppress the IMPATT noise contribution to meet the requirement on overall transmitter noise figure.
- Noise figure: 23 dB (max.), as compared to 25 dB requirement (if requirement were relaxed to 32 dB, FET driver section could be omitted).
- DC prime power: 120W (max.) including dissipation in DC power and monitor conditioner (110.3W required as DC bias for the amplifier stages themselves).
- RF/DC power added efficiency: 20.4 percent (not including DC power and monitor conditioners).

The above is based upon the use of IMPATT power devices with 25 percent DC/RF power added efficiency.



5.0 SENSITIVITY ANALYSIS



CRITICAL IMPATT PARAMETERS IMPACTING AMPLIFIER SENSITIVITY

IMPATT CHIP PARAMETERS

- AVALANCHE 1-G1
- AVALANCHE FREQUENCY
- SPREADING RESISTANCE
- MAXIMUM RF POWER GENERATION CAPABILITY
- DC/RF GENERATION EFFICIENCY

IMPATT DIODE TERMINAL CHARACTERISTICS

- 1 - G<sub>N1</sub>
- RESIDUAL UNRESONATED SUSCEPTANCE:  $w_0 \Delta c$
- PARALLEL - TUNED SUSCEPTANCE SLOPE:  $\delta_n$
- MAXIMUM RF POWER GENERATION CAPABILITY
- DC/RF GENERATION EFFICIENCY

IMPATT AMPLIFIER PASSBAND (9.7-20.2 GHz) CHARACTERISTICS

- REFLECTION GAIN
- REFLECTION PHASE
- MAXIMUM RF POWER ADDED CAPABILITY
- MAXIMUM DC/RF CONVERSION EFFICIENCY

IMPATT PACKAGE PARASITICS

- SERIES LEAD INDUCTANCE
- PARALLEL STANDOFF CAPACITANCE



## 5.1 CRITICAL IMPATT PARAMETERS IMPACTING 20 GHz TRANSMITTER SENSITIVITY

Deviations from nominal performance of the 20 GHz IMPATT transmitter arise as a consequence of deviation from nominal of one or more of the following passband characteristics of any of the IMPATT amplifier stages comprising the overall power section:

- Reflection power gain/stage.
- Reflection phase/stage.
- Maximum RF power added capability/stage.
- Maximum DC/RF conversion efficiency/stage.

These deviations, in turn, arise from dispersion in one or more of the following IMPATT diode terminal characteristics:

- Negative conductance.
- Residual unresonated susceptance.
- Susceptance slope of tuned diode.
- Maximum RF power generation capability.
- DC/RF generation efficiency.

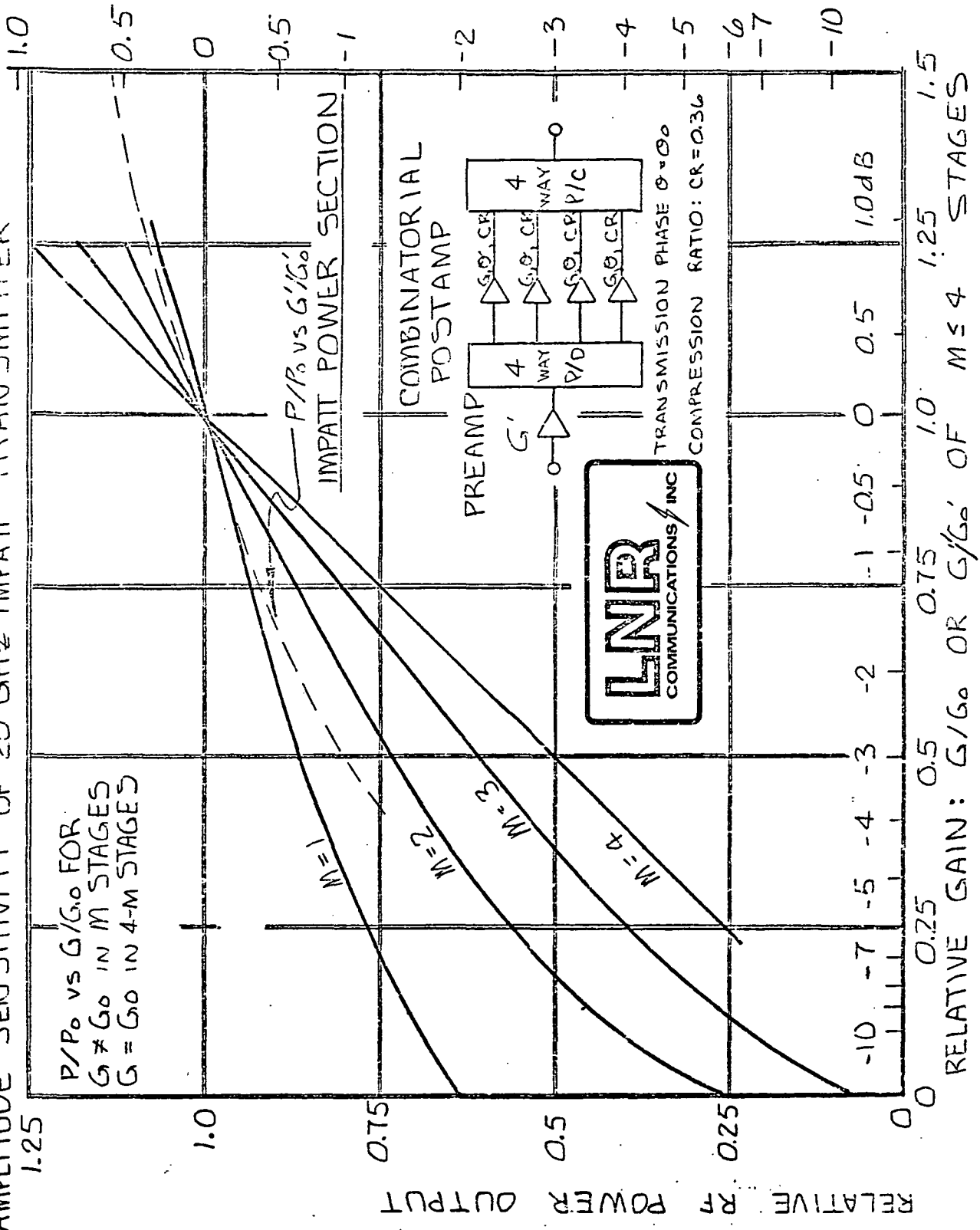
The above are brought on, for the most part, by the following IMPATT chip/package parameters:

- Chip avalanche negative conductance (and frequency).
- Chip spreading resistance.
- Package parasitics, such as series lead inductance and parallel standoff capacitance.

The major overall transmitter performance characteristics affected by the foregoing parametric dispersion are RF power output (and DC/RF efficiency) gain, bandwidth and linearity (AM/PM conversion). Emphasis in this analysis will be on the former.



AMPLITUDE SENSITIVITY OF 20 GHz IMPATT TRANSMITTER



RELATIVE RF POWER OUTPUT -dB

## 5.2 AMPLITUDE SENSITIVITY OF 20 GHz IMPATT TRANSMITTER

Within the specified overall transmitter passband, the output power of said transmitter is sensitive to deviations from nominal of the net two stage operating gain of either the IMPATT preamplifier and/or one or more of the four combinatorial IMPATT postamplifier paralleled "building blocks" comprising the overall IMPATT power section.

Due to the "single thread" connection of the preamp, the sensitivity of transmitter output power to preamp gain changes is  $\sim 0.36$  dB/dB, where the latter quantity represents the nominal composite compression ratio of each of the identical paralleled two stage "building blocks".

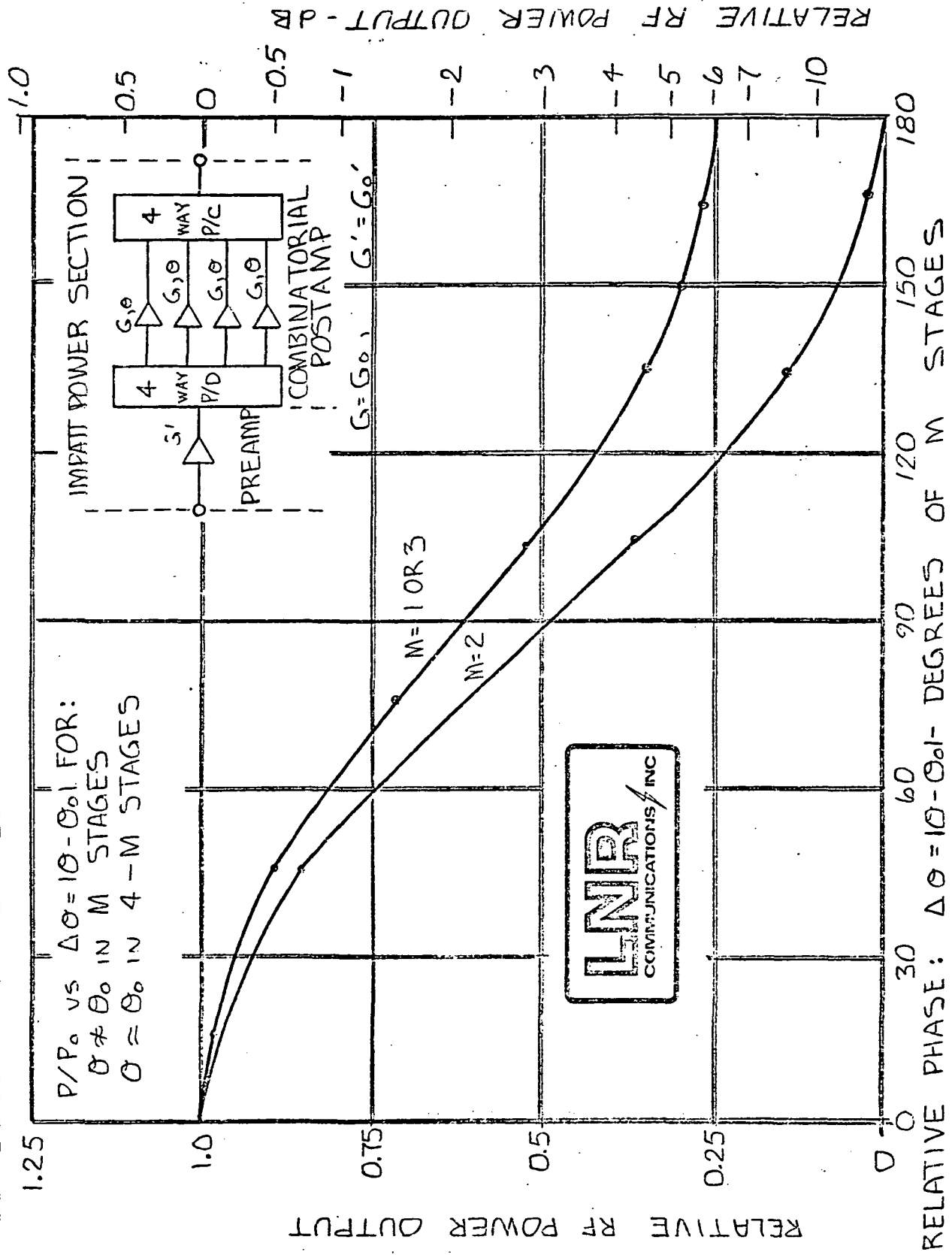
By virtue of the graceful degradation properties of the combinatorial post-amplifier, under equiphase conditions ( $\theta = \theta_0$ ) the sensitivity in transmitter RF output power to "building block" gain changes is:

- Between  $\sim 0.3$  dB/dB for identical gain changes in  $M=1, 2, \dots, 3, 4$ .
- $\sim 0.3 \sqrt{M}$  dB/dB for random gain changes in  $M$  branches.

The latter is probably a more realistic bound on amplitude sensitivity.



8) PHASE SENSITIVITY OF 20 GHz IMPATT TRANSMITTER



RELATIVE RF POWER OUTPUT

RELATIVE PHASE:  $\Delta\theta = 10 - \theta_0$  - DEGREES OF M STAGES

RELATIVE RF POWER OUTPUT - dB



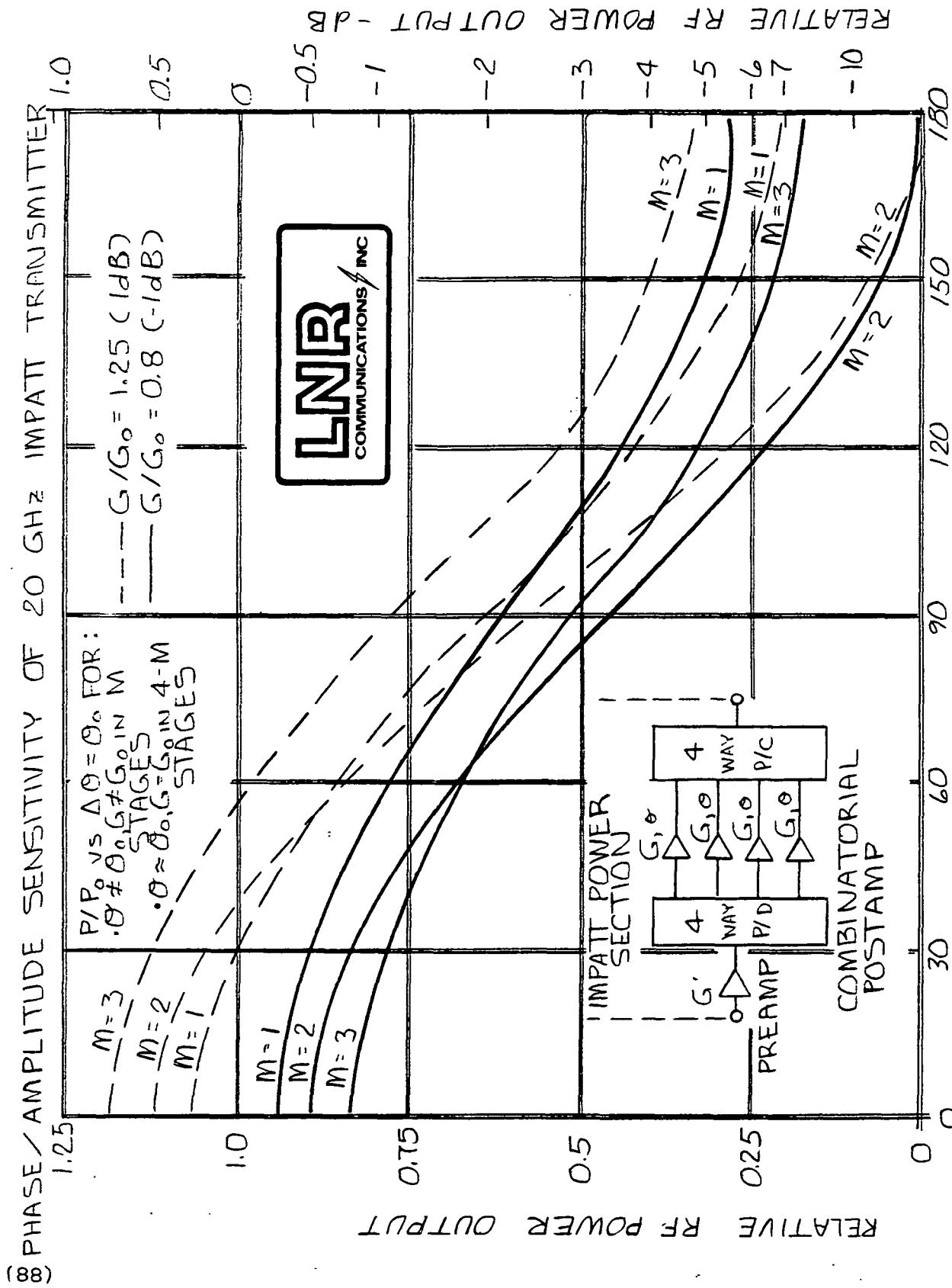
### 5.3 PHASE SENSITIVITY OF 20 GHZ IMPATT TRANSMITTER

Within the specified overall transmitter passband, the transmitter output power is sensitive to residual differences in transmission phase between the four nominally identical paralleled "building blocks" comprising the IMPATT power section combinatorial postamplifier for particular, phase deviations from nominal in one, two or three of the paralleled building blocks cause reductions in overall transmitter output power as follows (assuming that "building block" gains remain identical):

- Identical phase deviations  $\Delta \theta$  in two "building blocks" cause more severe degradation than does deviation in one.
- Identical deviations  $\Delta \theta$  in three building blocks is clearly equivalent in effect to a deviation  $\Delta \theta$  in one.
- Phase deviations of less than 45 degrees in one or two "building blocks" (as will be shown to be generally the case) result in modest degradations in transmitter output power of less than 0.75 dB, whereas severe degradation occurs only under extremely unlikely phase deviations of greater than 90 degrees.

Random phase deviating in more than one "building block" will generally result in less output power degradation than that calculated for two "building blocks" at the largest deviation.





RELATIVE PHASE:  $\Delta\theta = 0-0^\circ$  OF  $M < 4$  STAGES (DEGREES)

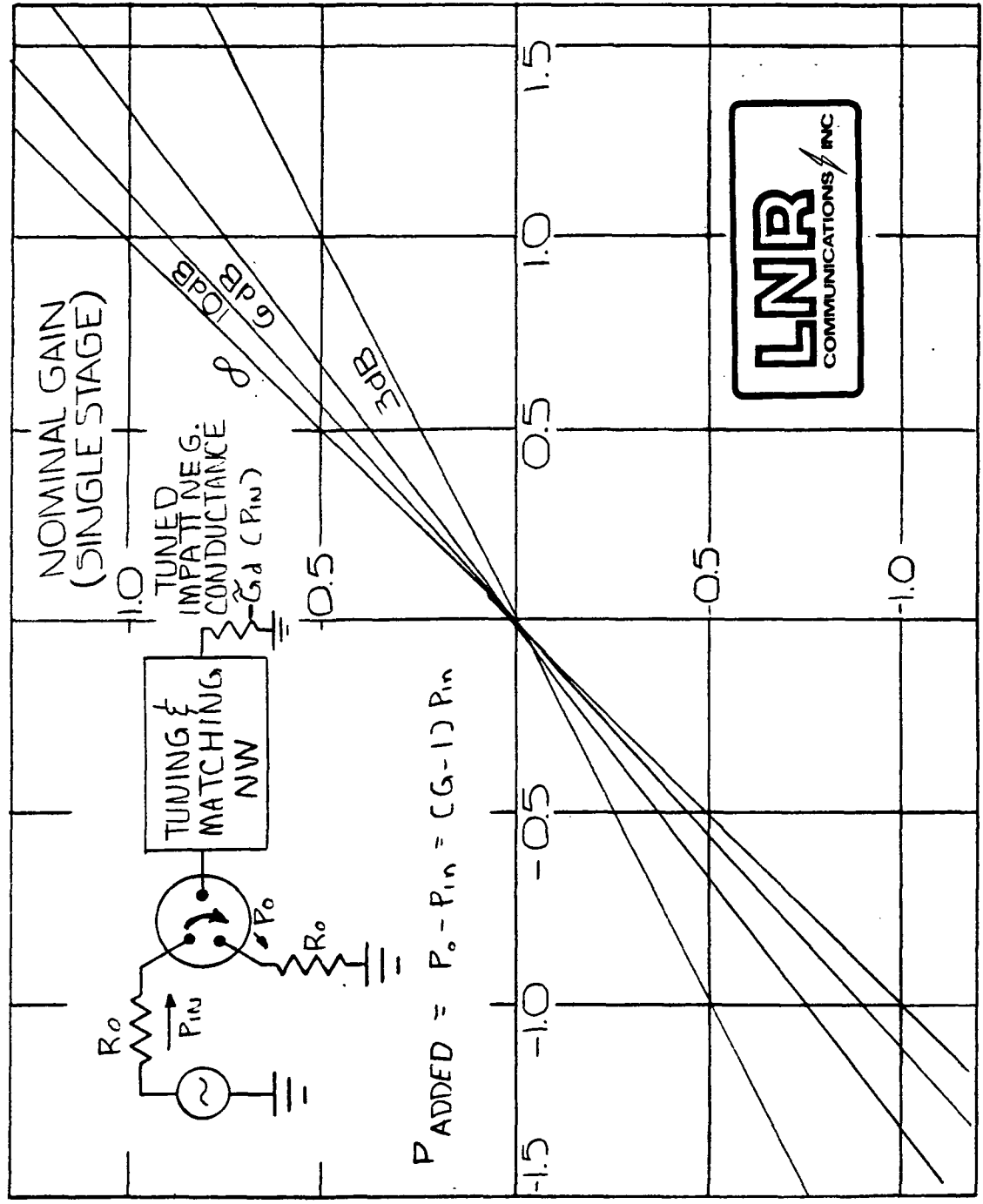
#### 5.4 COMBINED PHASE/AMPLITUDE SENSITIVITY OF 20 GHZ IMPATT TRANSMITTER

Within the specified overall transmitter passband, simultaneous deviations from nominal gain and transmission phase of  $M=1$ , 2 or 3 of the four paralleled IMPATT power section "building blocks" can result in enhancement as well as degradation from nominal of RF output power, with the latter, however, being most prevalent. Specifically, for gain deviations of within  $\pm 1.0$  dB and phase deviations of less than 45 degrees, in  $M=1$ , 2 or 3 "building blocks" variation of overall transmitter output power from nominal will be within  $\pm 0.5$  dB, whereas greater than 90 degrees phase deviations will result in more severe ( $>3$  dB) degradation in transmitter output power. Random gain and phase deviations from nominal in  $M=2$  or 3 "building blocks" will generally result in less output power degradation than uniform deviations of the "worst case" value.



SENSITIVITY OF IMPATT AMPLIFIER STAGE GAIN

VARIATIONS IN IMPATT DIODE POWER ADDED CAPABILITY



VARIATION IN AMPLIFIER STAGE GAIN  $\Delta G$  (dB)

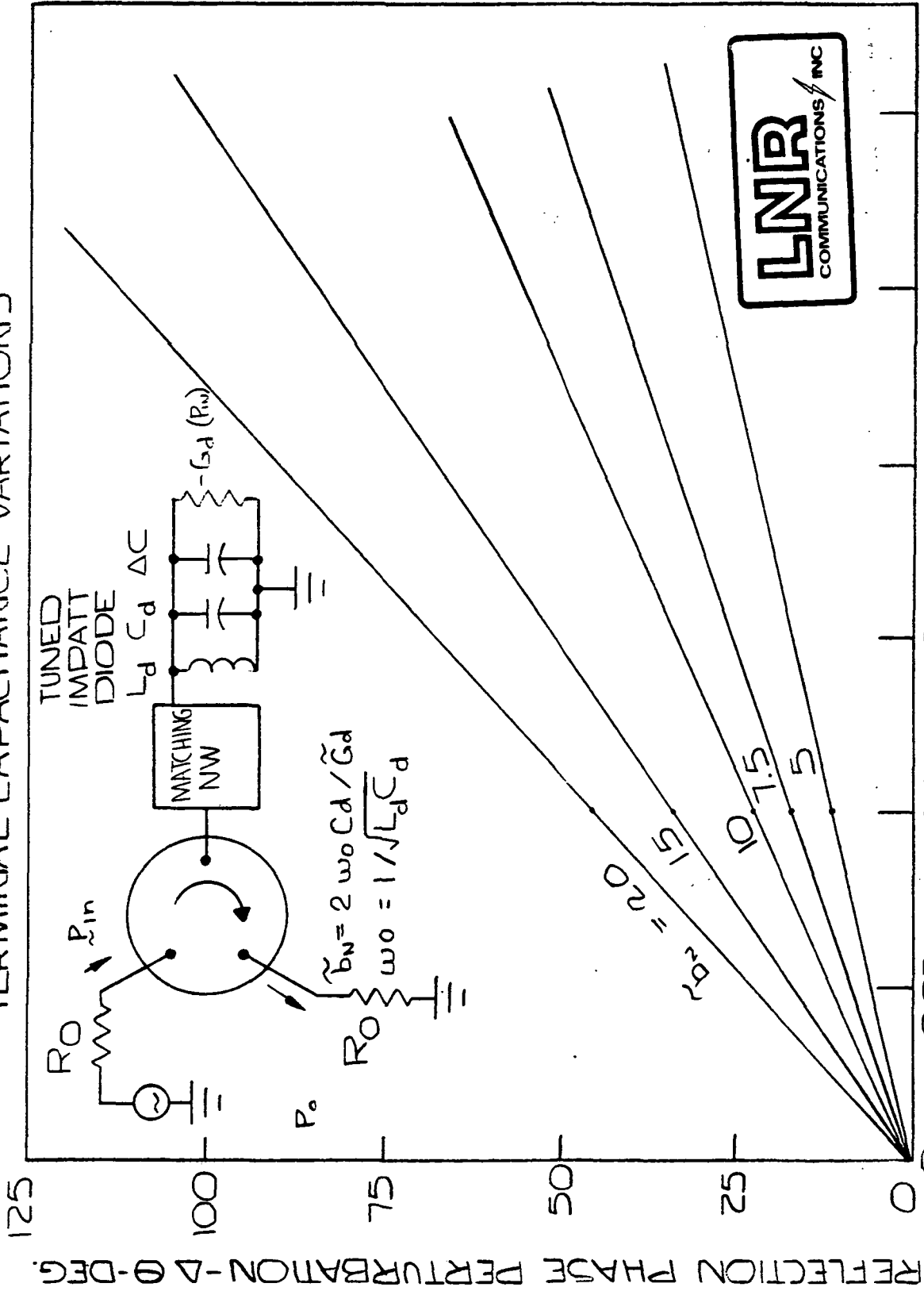
VARIATION IN IMPATT DIODE POWER ADDED CAPABILITY  $\Delta P_A$  (dB)

5.5 SENSITIVITY OF IMPATT AMPLIFIER STAGE GAIN TO VARIATIONS IN IMPATT DIODE POWER ADDED CAPABILITY

The large-signal gain of a properly tuned single stage circulator coupled IMPATT reflection amplifier operated at the optimum nominal RF drive level required for maximum nominal RF power added capability, will deviate from nominal directly but at a less than one to one rate with corresponding deviations from nominal of said maximum power added capability. The latter, in turn, results from deviations from nominal of IMPATT diode large signal terminal negative conductance, which themselves arise from variations in IMPATT diode chip and encapsulation parameters such as avalanche conductance, chip series resistance, series lead inductance. Specifically, for the nominal 6 dB operating gain level of each "building block" stage, the rate of variation of said gain with deviations from nominal in power added capability is about 0.75 dB/dB. This corresponds to a sensitivity in overall transmitter RF output power of between 0.22 to 0.75 dB per dB of deviation from nominal power added capability in one or more of the two stage IMPATT "building blocks".



"WORST CASE" IMPATT AMPLIFIER STAGE PHASE SENSITIVITY TO DIODE  
 TERMINAL CAPACITANCE VARIATIONS



REFLECTION PHASE PERTURBATION- $\Delta\theta$ -DEG. ←

RELATIVE PERTURBATION IN TERMINAL CAPACITANCE -  $\Delta C/C_d$  →

## 5.6 SENSITIVITY OF IMPATT AMPLIFIER STAGE TRANSMISSION PHASE TO VARIATIONS IN IMPATT DIODE CHARACTERISTICS

Differences in transmission phase through each of the four nominally identical IMPATT combinatorial postamplifier paralleled "building blocks" arise from corresponding differences between the "building block"

- reflection phase at each amplifier stage IMPATT mount/circulator interface
- transmission phase through circulators
- path lengths of interconnects to power divider and combiner

The former of the above, in turn, is impacted by variations of the following IMPATT diode/mount characteristics from their respective nominal values:

- residual unresonated susceptance ( $\omega_0$ ,  $\Delta C$ ) of nominal amplifier center frequency  $\omega_0 = 2\pi f_0$  (nominally zero at  $f_0 = 19.95$  GHz) a parallel tuned diode normalized susceptance slope parameter  $b_N$  - nominally  $\sim 15$  (typ.)

The above, in turn are influenced by the following IMPATT chip and encapsulation parameters

- chip junction capacitance
- avalanche inductance
- package parasitics (series lead inductance and parallel standoff capacitance).

For "worst case" values of relative residual unresonated diode susceptance ( $\Delta C/C_d \leq 0.04$ ) and typical diode susceptance slope parameter ( $b_N \approx 15$ ), the "worst case" deviation from nominal amplifier stage transmission phase is less than 30 degrees. This corresponds to degradation in overall transmitter power of less than 0.5 dB from nominal.



CONSTRUCTION/ALIGNMENT TECHNIQUES FOR MINIMIZATION  
OF AMPLIFIER SENSITIVITY TO VARIATIONS IN IMPATT  
DIODE PARAMETERS

1. MODULAR IMPATT MOUNT CONSTRUCTION
  - . EASY REPLACEMENT OF IMPATT DIODES
  - . DIRECT ACCESS TO IMPATT MOUNT TUNING AND BROADBANDING ELEMENTS FOR PRECISE ITERATIONS TOWARD NOMINAL PERFORMANCE GOALS
2. PRECISE AMPLIFIER "BUILDING BLOCK" ALIGNMENT
  - . SELECTION OF MOUNT TUNING ELEMENTS TO RESONATE DIODES AT SPECIFIED BAND CENTER
  - . SELECTION OF MOUNT TRANSFORMERS TO ACHIEVE SPECIFIED MID-BAND GAIN LEVEL.
  - . ADJUSTMENT OF DIODE BIAS VOLTAGES FOR NOMINAL VALUE OF POWER ADDED CAPABILITY.
  - . GENERAL ALIGNMENT OF "BUILDING BLOCKS" FOR NOMINALLY IDENTICAL POWER OUTPUT, GAIN AND PHASE CHARACTERISTICS PRIOR TO INTEGRATION INTO IMPATT "POWER SECTION"
3. FINAL, SECOND-ORDER PHASE EQUALIZATION OF PARALLELED "BUILDING BLOCK" AMPLIFIER PATH LENGTHS IN POWER SECTION COMBINATORIAL POSTAMPLIFIER, BY USE OF INCREMENTAL REACTIVE "PHASE ADJUST" PERTURBATIONS INCORPORATED IN POWER DIVIDER/COMBINER INTERCONNECT MANIFOLDS:
4. SELECTION OF IMPATT DIODES FOR MATCHED POWER ADDED CAPABILITY





5.7 CONSTRUCTION/ALIGNMENT TECHNIQUES FOR MINIMIZATION OF  
AMPLIFIER SENSITIVITY TO VARIATIONS IN IMPATT DIODE PARAMETERS

The impact on overall transmitter performance of dispersion in this characteristics of the IMPATT diodes used in power section "building block" amplifiers will be minimized by the use of the following dedicated constructional and alignment techniques in the implementation of said power section:

- . modular IMPATT mount construction, permitting easy replacement of IMPATT diodes and direct access to IMPATT mount tuning and broadbanding elements for precise iterations toward nominal performance goals.
- . precise alignment of combinatorial postamplifier "building blocks" for nominally identical RF power output, gain and phase characteristics prior to integration on overall IMPATT power section.
- . accomplishment of above by precise selection of mount tuning elements for diode resonance at band center, of mount transformers for specified gain level and of diode bias voltages for specified power output capability.
- . final second order phase equalization of paralleled "building blocks" path lengths by use of incremental phase adjustments in power divider/combiner interconnect manifolds
- . selection of IMPATT diodes for matched power added capability

Utilization of the above techniques should reduce any degradation of overall transmitter performance due to IMPATT diode dispersion to negligible values.



C. DEVELOPMENT OF DEVICE/ASSEMBLY  
TECHNOLOGY

FINAL REPORT

NASA CR 174716

FEBRUARY, 1983

Prepared For:

NASA Lewis Research Center  
Cleveland, Ohio

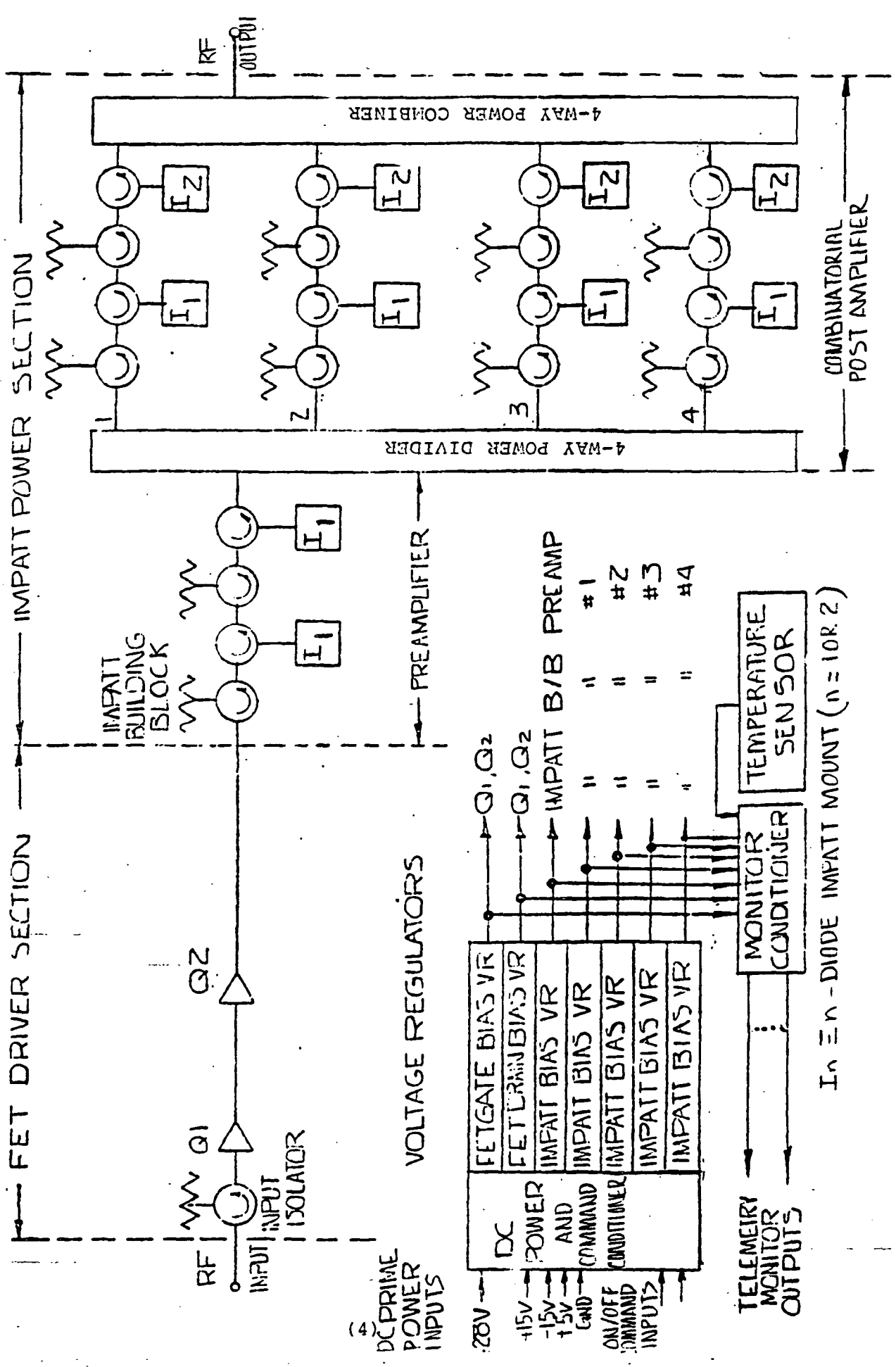
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  - 3. Electrical Design
  - 4. Key Device, Component and Subassembly Specifications
- B. DETAILED POC TEST PLAN/PROCEDURES (2.4.3/2.4.4)

A. POC MODEL DESIGN

1. Functional Design/Projected Performance



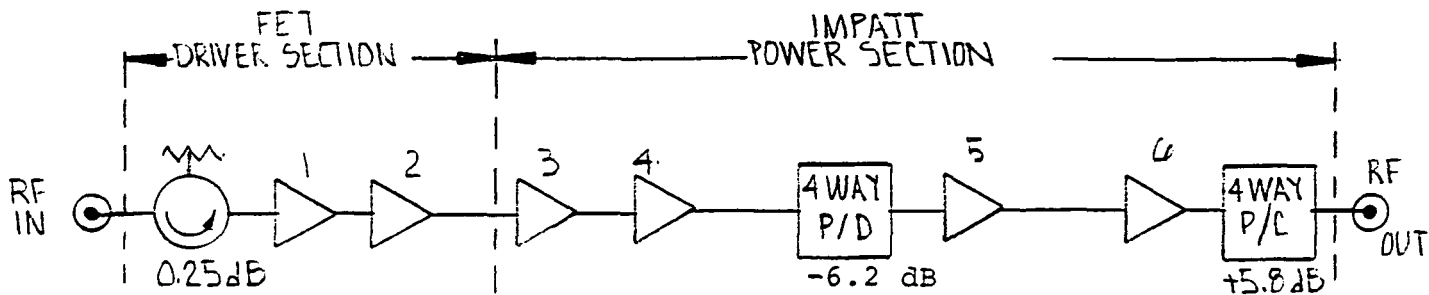
In  $n$  - DIODE IMPATT MOUNT ( $n = 10R.2$ )

BLOCK DIAGRAM OF POC MODEL 20 GHz IMPATT TRANSMITTER DESIGN

PROJECTED CHARACTERISTICS OF POC MODEL  
20 GHz IMPATT TRANSMITTER DESIGN

|   |   |
|---|---|
| CENTER FREQUENCY                          | 19.95 GHz   |
| -1 dB BANDWIDTH (MIN.)                    | 500 MHz (19.7-20.2 GHz)   |
| RF POWER OUTPUT (MIN.)                    | 22W   |
| OPERATING GAIN (NOM.)                     | 34.5 dB   |
| RF/DC POWER-ADDED EFFICIENCY (MIN.)       | 20.9 PERCENT (EXCLUDING DC POWER/MONITOR CONDITIONER)                     |
| AM/PM CONVERSION (MAX.)                   | 3 deg/dB  |
| INPUT/OUTPUT VSWR (MAX.)                  | 1.25:1  |
| GAIN VARIATION VS FREQUENCY @ FIXED DRIVE | 1.0 dB p-p  |
| PHASE LINEARITY (MAX.)                    | 10 deg p-p  |
| GAIN SLOPE (MAX.)                         | 0.1 dB/MHz  |
| PASSBAND GROUP DELAY VARIATION (MAX.)     | 0.5 nS/50 MHz   |
| SPURIOUS OUTPUTS (MAX.)                   |   |
| . HARMONIC COMPONENTS                     | -50 dBc   |
| . NON HARMONIC COMPONENTS                 | -60 dBc   |
| NOISE FIGURE (MAX.)                       | 24 dB   |
| DC PRIME INPUT POWER (MAX.)               | 105.3W EXCLUDING DC POWER/MONITOR/COMMAND CONDITIONER<br>115W OVERALL     |
| WEIGHT                                    | 4.8 lbs.  |
| DIMENSIONS                                | 6.75"x5.75"x2.5"  |
| BASEPLATE TEMPERATURE RANGE               | 0-75°C  |
| MAXIMUM DEVICE JUNCTION TEMPERATURE:      | 235°C (IMPATT)<br>112°C (FET)   |
| RF INPUT/OUTPUT INTERFACES (J1/J2)        | WR-42 W/G - UG595/UG 595/U COVER FLANGE +28 VDC, +15 VDC, -15 VDC, +5 VDC |
| DC INPUT POWER INTERFACE                  | -ITT CANNON DEMA TYPE CONNECTOR   |
| TELEMETRY MONITOR OUTPUT INTERFACE        | ITT CANNON DEMA TYPE CONNECTOR  |

# PROJECTED PERFORMANCE BUDGET FOR 20 GHz POC MODEL IMPATT TRANSMITTER



| STAGE                                  | 1    | 2    | 3   | 4     | 5     | 6     | OVERALL |
|--|------|------|-----|-------|-------|-------|---------|
| GAIN dB                                | 5.25 | 4    | 9   | 6.2   | 6.2   | 4.5   | 34.5    |
| RF OUTPUT POWER - dBm                  | +14  | +18  | +27 | +33.2 | +33.2 | +37.7 | +43.5   |
| GAIN COMPRESSION RATIO - dB/dB         | 1.0  | 1.0  | 0.7 | 0.6   | 0.6   | 0.4   | 0.1     |
| AM/PM CONVERSION - deg/dB              | 0    | 0    | 1.0 | 1.2   | 1.2   | 1.8   | 2.8     |
| NUMBER OF PARALLELED STAGES            | 1    | 1    | 1   | 1     | 4     | 4     |         |
| NOISE FIGURE - dB                      | 6    | 8    | 32  | 32    | 32    | 32    | 24      |
| DC POWER DRAIN / STAGE - W             | 0.03 | 0.27 | 7.5 | 7.5   | 7.5   | 15    | 105.3   |
| COMPOSITE THERMAL RESISTANCE - °C/W    | 300  | 100  | 20  | 20    | 20    | 10    | —       |
| "WORST CASE" DEVICE JUNCTION TEMP - °C | 95   | 112  | 235 | 235   | 235   | 235   | —       |

**NOTES:**

- PERFORMANCE CALCULATED AT +9 dBm NOMINAL INPUT DRIVE LEVEL.
- LARGE SIGNAL AM/PM CONVERSION AND NOISE FIGURE CALCULATIONS TAKE INTO ACCOUNT GAIN COMPRESSION RATIO.
- DC POWER DRAIN DOES NOT INCLUDE CONTRIBUTIONS OF DC REGULATORS, COMMAND AND MONITOR CIRCUITS.
- JUNCTION TEMP @ 75°C BASEPLATE AND, 10°C MAX STAGE HOUSING / BASEPLATE RISE.

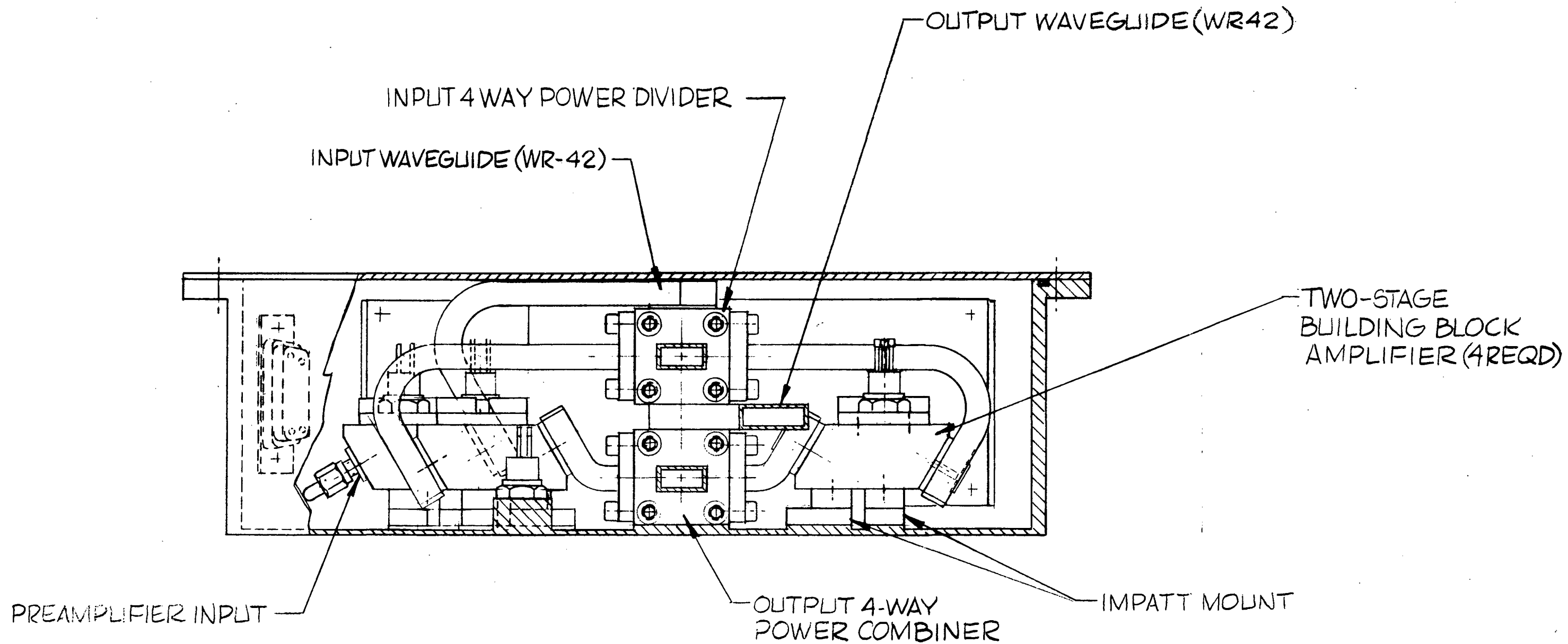




KEY FEATURES OF POC MODEL 20 GHz IMPATT  
TRANSMITTER DESIGN

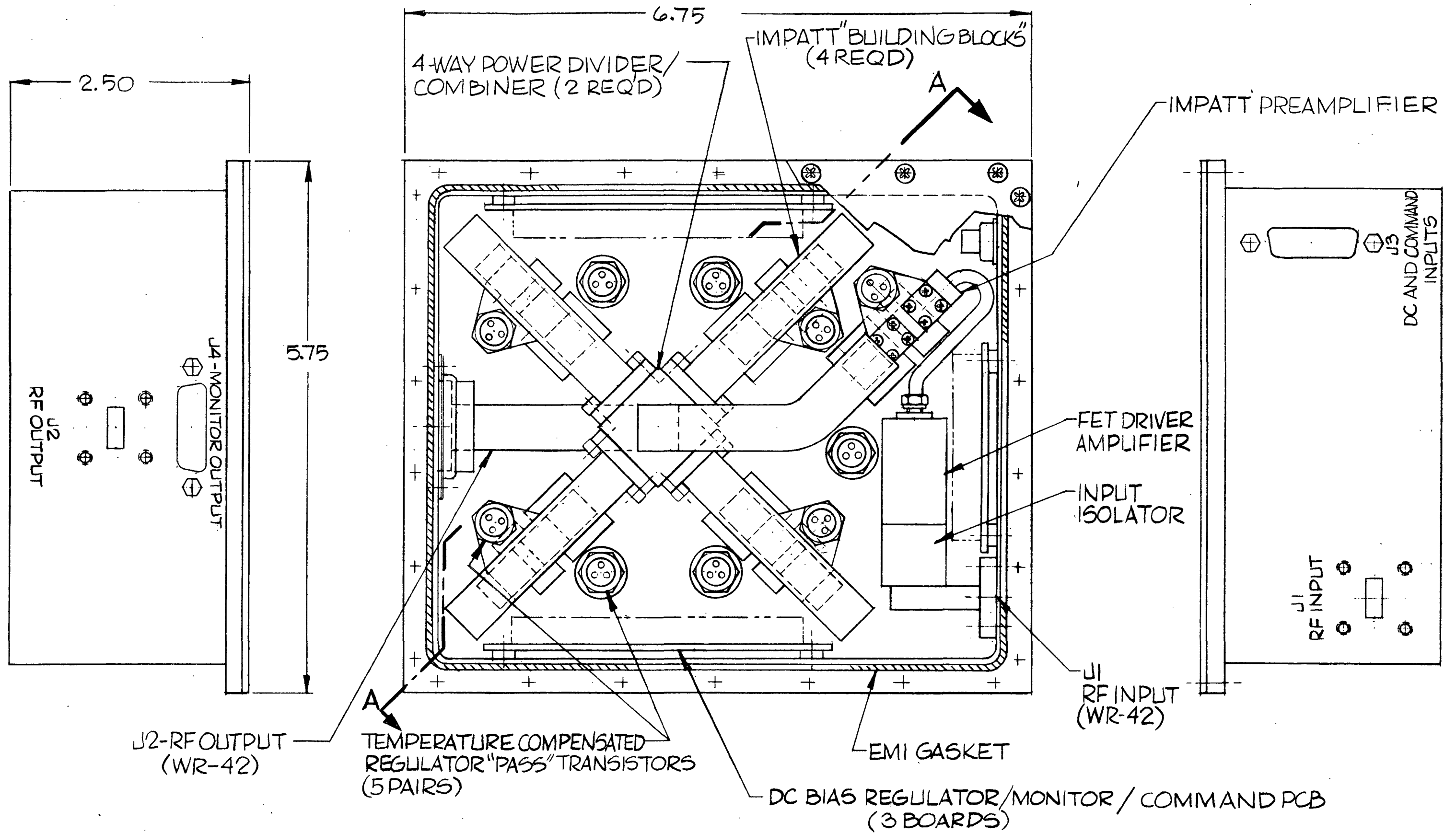
- . Use of LNR 2W, 20 GHz GaAs SDR Read-IMPATT diodes, which have demonstrated required capability for RF amplifier deployment.
- . Use of readily available modest power level GaAs MESFET chips in two-stage FET driver wherein FET's are mounted on customized pretuned LNR carriers which are in turn embedded in the microstrip circuit comprising the two stage single-ended amplifier.
- . Passive combination of mutually isolated, modular two stage IMPATT amplifier "building blocks" for simple manufacturability, and enhanced reliability.
- . Graceful degradation in RF output power under random device failure and "power down" capability, both by "turning off" individual "building blocks".
- . IMPATT amplifiers, used in high gain-bandwidth product stable amplification configuration, provide wide dynamic range and small signal to full drive capability without stability problems or undesired output spuri in absence of input signal.
- . Compact low loss miniature multi-port high isolation stripline wye junction circulators with individual junctions serving as amplifier coupling circulators, and with appropriate resistive internal terminations, as input and interstage isolators.
- . Simple miniature non-critical easily aligned highly reliable and mechanically rugged TEM-line IMPATT amplifier mount design directly integrated with coupling port of circulator and incorporating optimum tradeoff between RF power output, DC/RF power added efficiency, gain-bandwidth and output flatness.

## 2. Thermal/Mechanical Design



SECTION A-A

CONCEPTUAL LAYOUT OF 20GHZ IMPATT TRANSMITTER



CONCEPTUAL LAYOUT OF 20GHZ IMPATT TRANSMITTER

PROJECTED WEIGHT BUDGET FOR POC MODEL 20 GHz IMPATT TRANSMITTER

| <u>COMPONENT (QUANTITY)</u>                | <u>WEIGHT (OZ)</u>       |
|--|--------------------------|
| . IMPATT Power Section Building Blocks (4) | 16.0                     |
| . IMPATT Power Section Preamplifier (1)    | 3.0                      |
| . FET Driver Section                       | 2.0                      |
| . 4-Way Power Divider/Combiner (2)         | 6.0                      |
| . Input Isolator (1)                       | 0.5                      |
| . DC Postregulators (7)                    | 10.5                     |
| . Monitor Conditioner (7)                  | 3.5                      |
| . Command Conditioners (6)                 | 2.5                      |
| . Wiring, etc.                             | 1.0                      |
| . Waveguide interconnects                  | 8.0                      |
| . EMI Filter Box                           | 2.0                      |
| . Connectors and Transducers               | 1.0                      |
| . Structure and Hardware                   | 20.0                     |
| TOTAL                                      | <hr/> 76.0 oz (4.75 lb.) |

MECHANICAL ASPECTS OF POC MODEL 20 GHz IMPATT  
TRANSMITTER DESIGN

- . Identical two stage "building block" circulator-coupled IMPATT amplifiers implemented as integrated four junction dielectrically loaded stripline circulator structures to the active ports of the second and fourth junctions of which are directly coupled the TEM-line IMPATT amplifier mounts. Each IMPATT mount containing the hermetically sealed stud-mounted IMPATT diode and its associated tuning and broadbanding/transformation elements, is directly integrated with the circulator housing, and is directly heat sunk to the transmitter baseplate. The first and third junctions comprising input isolators have their isolated ports match terminated with directly integrated customized miniature 20 GHz terminations, the former of which accomodates RF-isolated, non dissipative DC bias input for the IMPATT diodes.
- . The power section two stage IMPATT pre-amplifier is implemented as a similar integrated, unitized structure.
- . The five two-stage IMPATT "building blocks" utilized in the power section are mounted vertically and coupled between a four way input power divider and output power combiner the latter affixed to the transmitter baseplate and the former elevated, thereby providing short, low resistance thermal paths from the stud-mounted IMPATT diodes, to the transmitter baseplate.
- . The four way waveguide power divider and combiner are essentially compensated reactive junctions, formed in milled-out waveguide enclosed housings.
- . Power section IMPATT preamplifier, "building blocks" and power dividers and combiner, mounted as above, are directly inter-connected through matched and phase-compensated waveguide sections, to form high packaging density power section with most efficient utilization of space.
- . Directly interconnected connectorless driver, section comprising cascade of two-stage FET amplifier of duroid based microstrip implementation.
- . Dielectrically loaded stripline terminated circulator input isolator directly integrated with FET driver input and through TEM/waveguide transducer, with transmitter RF input WR-42 waveguide interface.

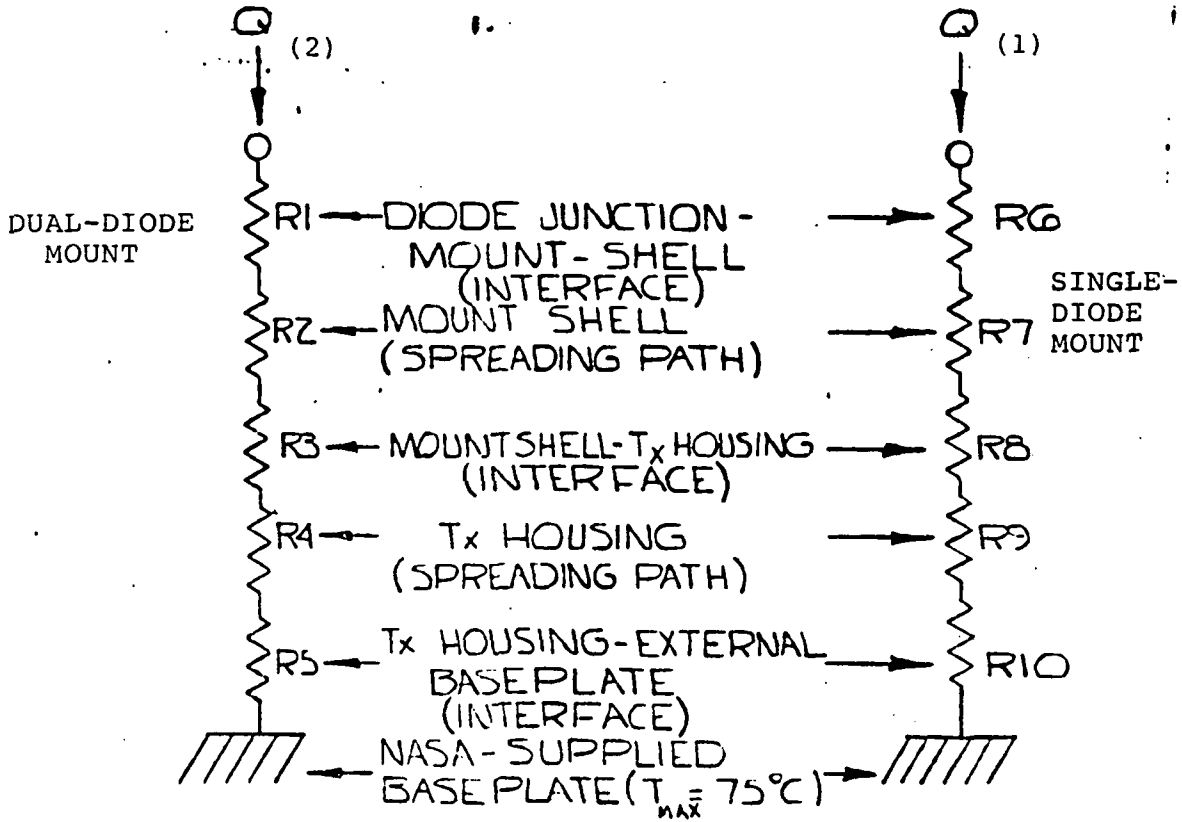
- . Miniatureized PC card DC bias postregulators each of which utilize PC card mounted, hermetically sealed "flatpack" functional IC's and discrete "pass" transistors which are affixed to the transmitter baseplate for better heat sinking.
- . PC card based monitor conditioners utilizing functional IC's to derive required DC analog outputs, and interconnected directly with associated voltage regulator cards.
- . PC card based command conditioners, providing turn off/turn on of amplifier stages on external pulse command, and interconnected directly with associated voltage regulator cards.

THERMAL ASPECTS OF 20 GHz POC MODEL  
IMPATT TRANSMITTER DESIGN

- . Mounting of all high dissipation components in intimate thermal contact with overall enclosure baseplate.
- . Use of high thermal conductance interfaces between individual module baseplates and overall enclosure baseplate.
- . Maintenance of short length, large area thermal conductance paths of high conductance materials.
- . Optimum spreading in thermal paths to minimize baseplate thermal density.
- . All dissipative component temperatures confined to less than 10°C above the enclosure baseplate, with the exception of the 20 GHz FET's and IMPATT's.
- . Dissipative elements widely distributed on enclosure baseplate so that average thermal density presented to baseplate mounting interface is low.
- . "Worst case" Transmitter device junction temperatures (those experienced by IMPATT diodes in the absence of RF drive, under which condition all of the IMPATT diode DC bias power is dissipated), at maximum baseplate temperature of 75°C, are 235 degrees C.



# WORST CASE "THERMAL ANALYSIS OF IMPATT "BUILDING-BLOCK" AMPLIFIER



| MOUNT                             | THERMAL PATH | COMPOSITE THERMAL RESISTANCE $^{\circ}C/W$ | TEMP. RISE $\Delta T$ ABOVE BASEPLATE $^{\circ}C$ | MAXIMUM TEMP. $T (^{\circ}C)$ |
|-----------------------------------|--------------|--|---|-------------------------------|
| DUAL-DIODE<br>$Q_{(2)} = 15^W$    | R1           | 10   | 150   | 234.9*                        |
|                                   | R2           | 0.36                                       | 5.4   | 84.9                          |
|                                   | R3           | 0.1  | 1.5   | 79.5                          |
|                                   | R4           | 0.02                                       | 0.3   | 78.0                          |
|                                   | R5           | 0.18                                       | 2.7   | 77.7                          |
| SINGLE-DIODE<br>$Q_{(1)} = 7.5^W$ | R6           | 20   | 150   | 234*                          |
|                                   | R7           | 0.6  | 4.5   | 84                            |
|                                   | R8           | 0.2  | 1.5   | 79.5                          |
|                                   | R9           | 0.04                                       | 0.3   | 78,0                          |
|                                   | R10          | 0.36                                       | 2.7   | 77.7                          |

\*"WORST-CASE" IMPATT DIODE JUNCTION TEMPERATURE  
(15)

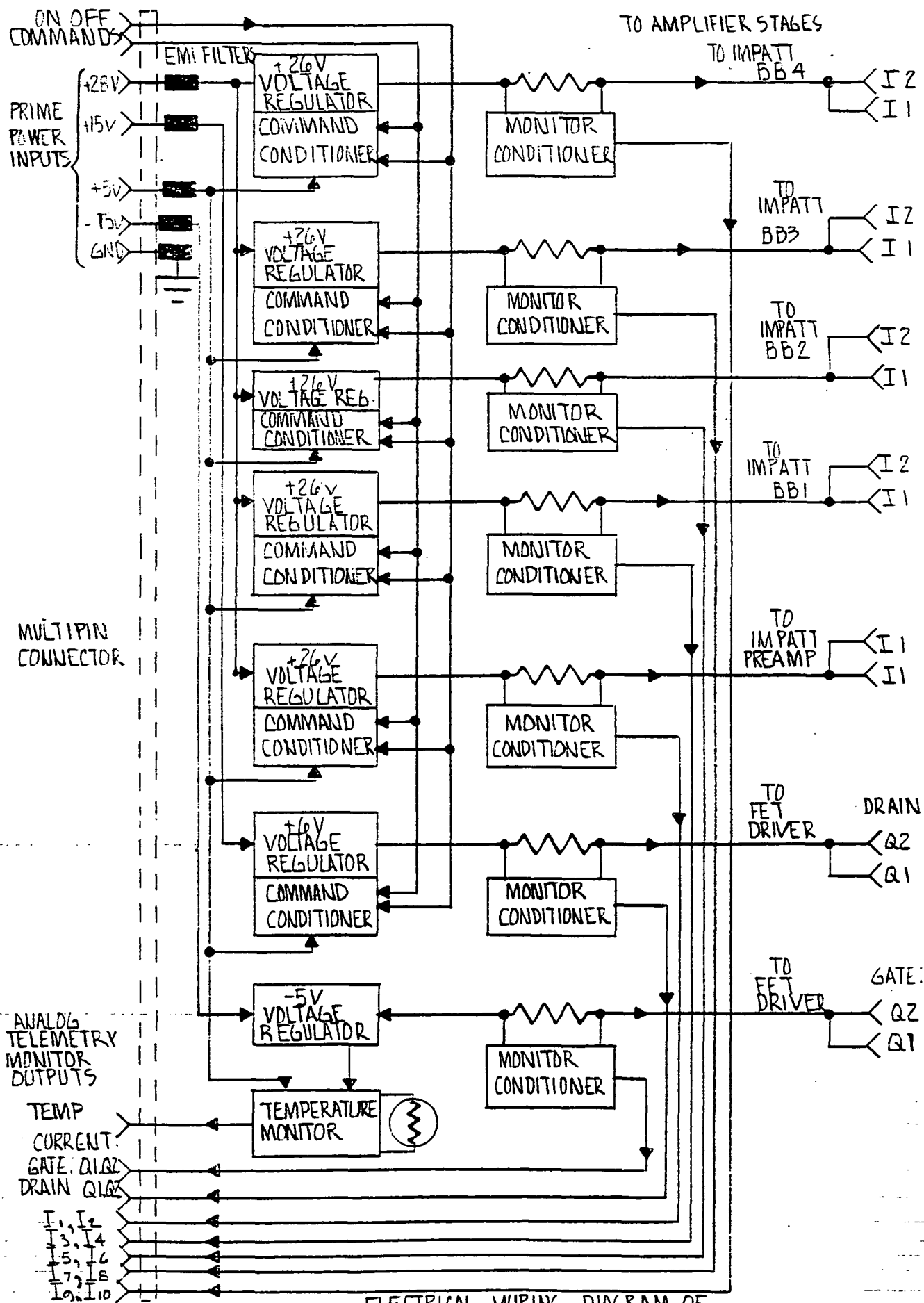
PACKAGING FEATURES OF 20 GHz POC MODEL  
IMPATT TRANSMITTER DESIGN

- . Modular construction wherein, self-contained replaceable FET driver and IMPATT power amplifier subassemblies (and their associated miniature postregulators, command conditioners, and monitor conditioners) are incorporated as individual prealigned modules prior to embedding in the transmitter master enclosure. This modular approach provides enhanced RF performance, ease of assembly, integrability and reliability with negligible impact upon size and weight.
- . Direct mounting, through minimum thermal paths, of all power dissipating modules and components, to enclosure baseplate.
- . TEM line housings milled out from solid aluminum stock All surfaces finished with silver plate and then lead-tin electroplated and heated for final lead/tin flow (similar construction used on currently manufactured high-rel amplifiers).
- . Optimum spreading in thermal paths to minimize baseplate thermal density.
- . Elimination, where passive, of internal RF connectors and superfluous transmission line lengths, thereby enhancing reliability and mechanical integrity as well as electrical performance.
- . Partitioned housing machined from solid aluminum stock thereby providing maximum degree of mechanical rigidity consistent with minimized weight, as best tradeoff between selective "lightening" for weight reduction and "stiffening" for immunity to severe vibrational environments.
- . Monel EMI gasketing used around all cover openings.
- . Strain relief at all electrical solder "bridge" interconnections thereby avoiding thermal and mechanical fatigue.

ENVIRONMENTAL ASPECTS OF 20 GHz POC  
MODEL IMPATT TRANSMITTER DESIGN

1. Operation over 0-75°C Temperature Range
  - . design optimization for peak performance at the high operating temperature extreme so as to minimize impact of inherent rolloff in transmitter RF output power, with increasing temperature.
  - . passive temperature compensation within DC bias voltage regulators to provide bias voltage versus temperature profiles which maximize performance at high temperature extreme and maintain tolerable variations in performance over the entire specified temperature range.
  - . use of temperature dependent residual heating obtainable from dissipative elements of voltage regulators to reduce temperature excursions of more critical passive RF components, such as circulators.
  
2. Constructional Techniques to Maximize Mechanical Integrity in Shock and Vibration Environment
  - . all hardware torqued and staked.
  - . all harnesses and cabling staked.
  - . all wires provided with adequate band stress relief at their termination.
  - . no teflon wiring used.
  - . all solder connections hand soldered.
  - . elimination of loose fits, with all microwave parts and assemblies under design compression fits.
  - . cantilever structures minimized.
  - . design maintains all structural resonances well above 2000 Hz.

### 3. Electrical Design



(19) ELECTRICAL WIRING DIAGRAM OF POC MODEL 20GHz IMPATT TRANSMITTER

DC POWER BUDGET FOR POC MODEL 20 GHz IMPATT TRANSMITTER

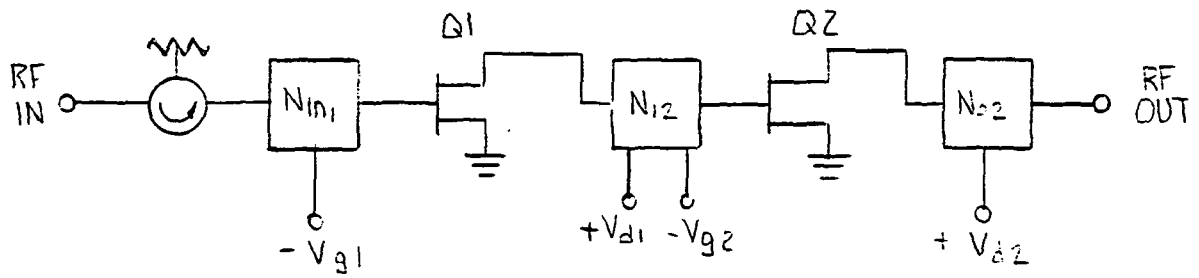
| <u>Subassembly</u>                                   | <u>Quantity</u> | <u>DC Input Voltage(s) -V</u>                       | <u>DC Power Drain-W Unit</u> | <u>Total</u> |
|--|-----------------|---|------------------------------|--------------|
| FET driver   | 1               | +3 <sup>V</sup> , +6 <sup>V</sup> , -1 <sup>V</sup> | 0.3                          | 0.3          |
| IMPATT Preamplifier                                  | 1               | +26 <sup>V</sup>                                    | 15                           | 15           |
| IMPATT "building blocks"                             | 4               | +26 <sup>V</sup>                                    | 22.5                         | 90           |
| +6 <sup>V</sup> FET drain voltage regulator          | 1               | +15 <sup>V</sup>                                    | 0.5                          | 0.5          |
| FET gate voltage regulator                           | 1               | -15 <sup>V</sup>                                    | 0.02                         | 0.02         |
| +26 <sup>V</sup> IMPATT bias voltage regulators for: |                 |   |                              |              |
| . IMPATT preamplifier                                | 1               | +28 <sup>V</sup>                                    | 1.2                          | 1.2          |
| . IMPATT "building blocks"                           | 4               | +28 <sup>V</sup>                                    | 1.73                         | 6.92         |
| Command Conditioners                                 | 6               | +5 <sup>V</sup>                                     | 0.02                         | 0.12         |
| Monitor Conditioner                                  | 7               |   | 0.02                         | 0.14         |
| TOTAL DC POWER DRAIN                                 |                 |   |                              | 114.2W       |

ELECTRICAL FEATURES OF 20 GHz POC MODEL  
IMPATT TRANSMITTER DESIGN

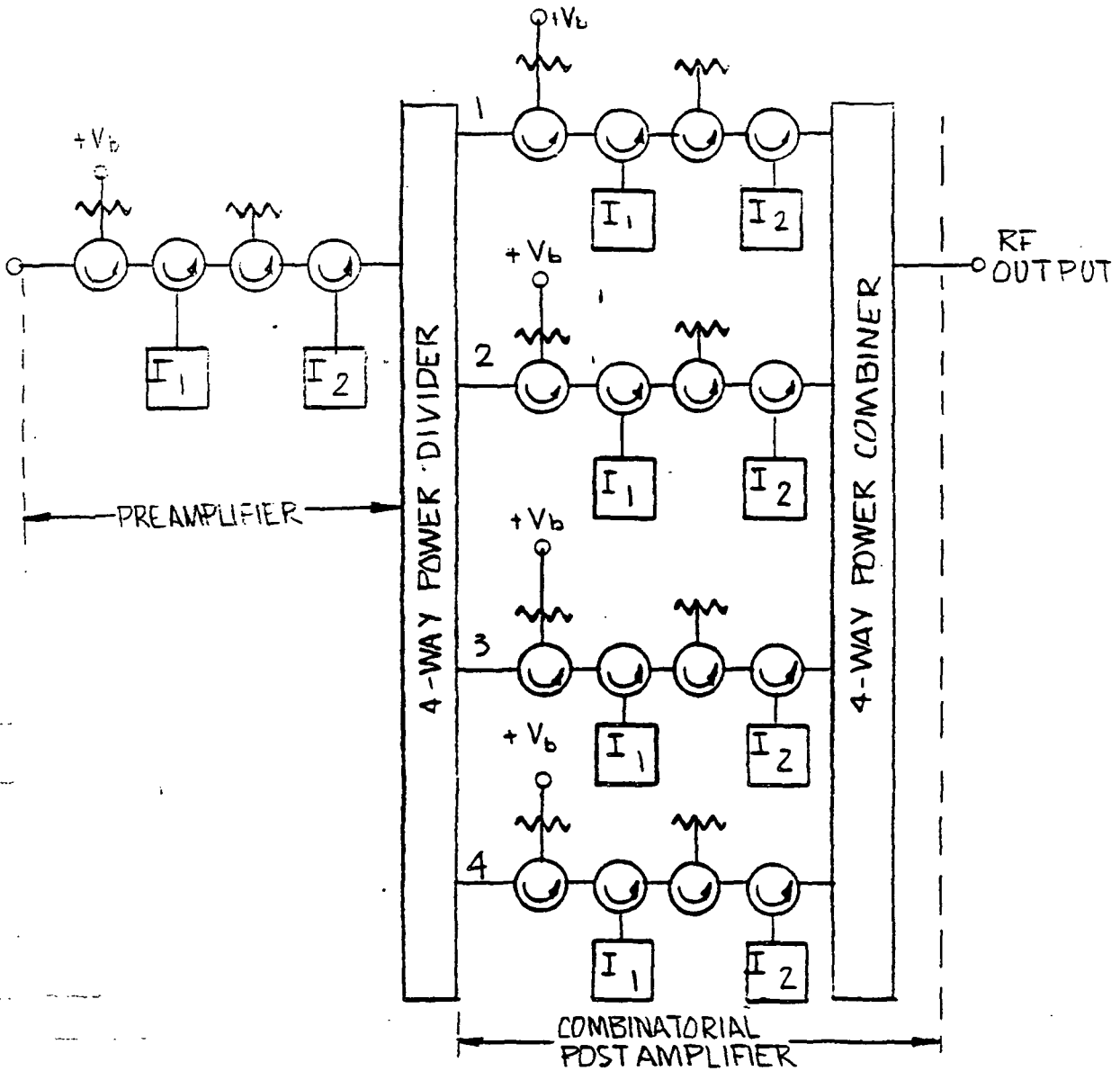
- . Co-ordinated DC bias postregulation, command and monitor conditioning for functional amplifier subassemblies.
- . Apportionment of coordinated DC bias voltage post-regulation and command and monitor conditioning among amplifier stages is as follows: FET drain (two stages), FET gate (two stages), IMPATT pre-amplifier (two stage), IMPATT "building blocks" #1, #2 and #3 and #4, (each two stage) thus resulting in a total of seven dedicated voltage regulator/command conditioner/monitor conditioner subassemblies.
- . Individual DC bias voltage postregulators, deployed as above to provide passively temperature compensated sufficiently regulated drain and gate bias voltage to both FET driver stages and to each IMPATT power section building block. Also included therein are foldback current limiting circuits to protect amplifier stages and secondary voltage input lines from excess current conditions.
- . Monitor conditioner circuits deployed in conjunction with corresponding postregulators, which provide analog telemetry outputs linearly proportional to corresponding DC bias currents, and to thermistor-derived unit temperature.
- . Command conditioner circuits, deployed in conjunction with corresponding monitor conditioners, provide "shut-off" and "turn-on" gates to the post regulators in response to input "turn-off" and "turn-on" command pulses, with a change of state occurring upon receipt of each new command pulse.
- . Individual high rel worthy connector for the DC power input and associated ground return, and analog command inputs and telemetry monitor outputs.

4. Key Device, Component and Subassembly Specifications



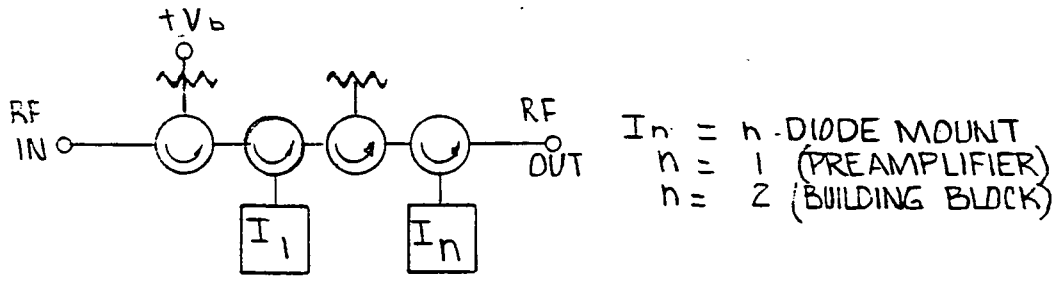


A- FET DRIVER SECTION

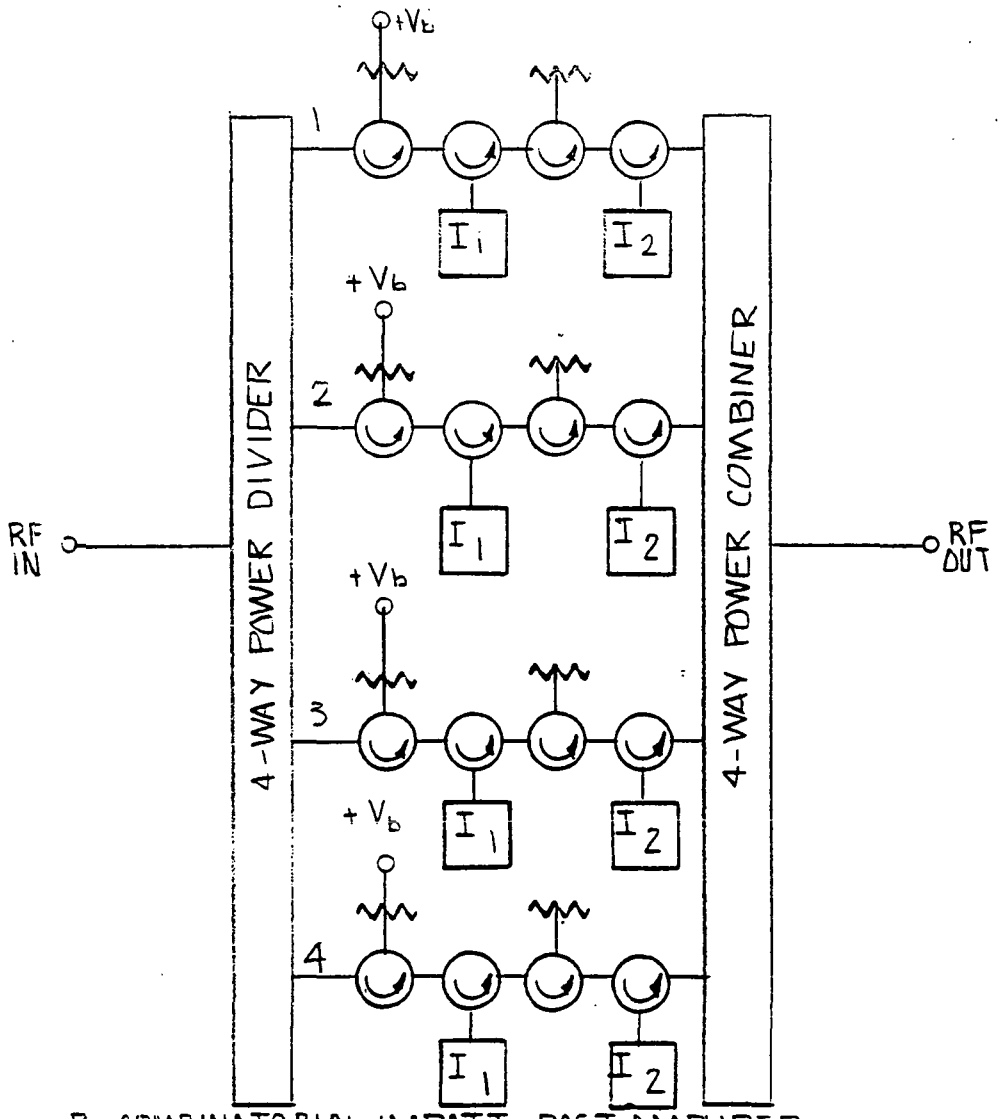


B-IMPATT POWER SECTION

MAJOR RF CONSTITUENTS OF 20GHz IMPATT TRANSMITTER



A - 2 STAGE IMPATT PREAMPLIFIER OR COMBINATORIAL "BUILDING BLOCK"



B - COMBINATORIAL IMPATT POST AMPLIFIER

MAJOR SUBASSEMBLIES COMPRISING IMPATT POWER SECTION

IMPATT Diode Specification

Supplier: LNR

Frequency range\*: 19.7-20.2 GHz

RF power output\*: 2W (min)

DC-RF conversion efficiency:\* 22 percent (min)

Thermal resistance: 20 deg C/W (max)

Package: LNR Part No. 118000119

\*measured in 20 GHz waveguide test oscillator

IMPATT Power Section "Building Block"

Frequency range: 19.7-20.2 GHz

Number of stages: 2

Number of IMPATT  
devices/stage           1. (input stage)  
                          2. (output stage)

RF power output: 6W (min)

Operating gain: 10.8 dB (min)

RF input drive level: +27 dBm (nom)

Gain compression ratio: 0.24 dB/dB (min)

AM/PM conversion: 2.3 deg/dB (max)

Noise figure: 37 dB (max)

Input/output VSWR: 1.25:1 (max)

DC power requirement: 22.5W (max) @ +26V

Construction: Composite WG/TEM

RF input/output interfaces: WR-42 WG

IMPATT Power Section Preamplifier

Frequency range: 19.7-20.2 GHz  
Number of stages: 2  
Number of IMPATT devices: 2  
RF power output: 2.0W (min)  
Operating gain: 15 dB (min)  
RF input drive level: +18 dBm (nom)  
Gain compression ratio: 0.4 dB/dB (min)  
AM/PM conversion: 1.8 deg/dB (max)  
Noise figure: 36.5 dB (max)  
Input/output VSWR: 1.25:1 (max)  
DC power requirement: 15W (max) @ +26V  
Construction: composite WG/TEM:  
RF input/output interfaces: 1.5 mm (SMA)/WR-42 WG

Four-Way Power Divider/Combiner

Frequency range: 19.7-20.2 GHz

Residual insertion loss: 0.2 dB (max)

Port to port amplitude balance:  $\pm 0.25$  dB (max)

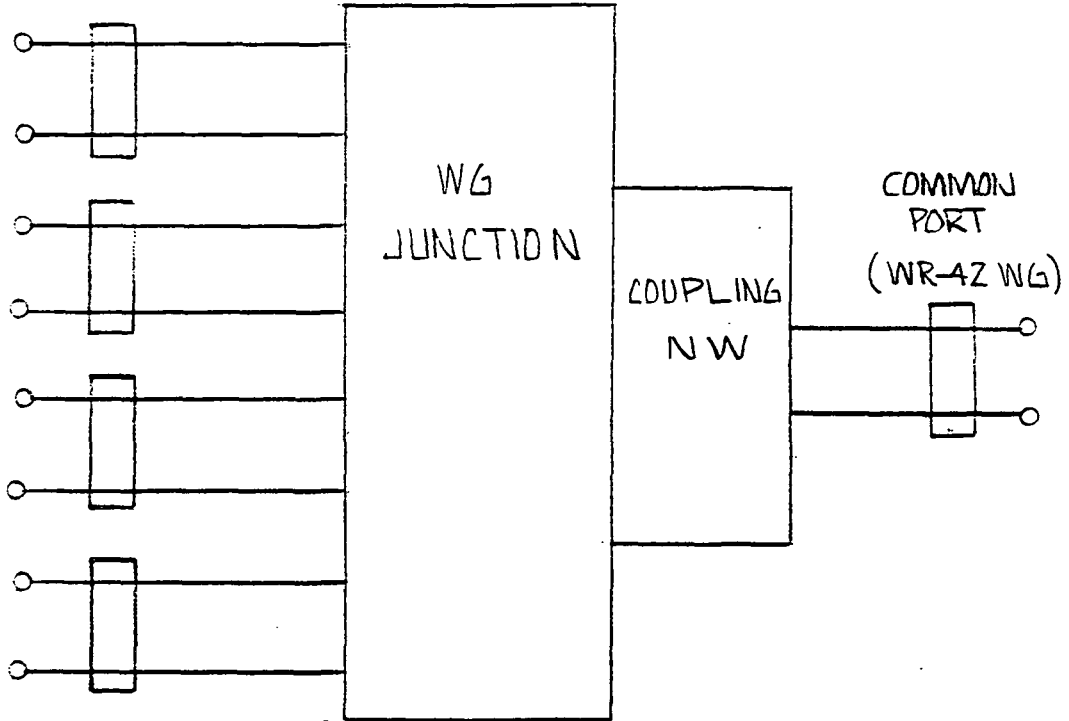
Port to port phase balance:  $\pm 5$  deg (max)

Common port VSWR: 1.25:1 (max)

Construction: composite WG/TEM

RF input/output interfaces: WR-42 WG

COMBINATORIAL  
PORTE  
(WR-42 WG)



FOUR WAY POWER DIVIDER / COMBINER

IMPATT Combinatorial Postamplifier

Frequency range: 19.7-20.2 GHz  
Number of "building blocks": 4  
Number of IMPATT devices: 12  
RF power output: 22W (min)  
Operating gain: 10.3 dB (min)  
RF input drive level: +33 dBm (min)  
Gain compression ratio: 0.24 dB/dB (min)  
AM/PM conversion: 2.3 deg/dB (max)  
Noise figure: 37.5 dB (max)  
Input/output VSWR: 1.25:1 (max)  
DC power requirement: 90W @ +26V  
Construction: Composite WG/TEM  
RF input/output interfaces: WR42-WG



IMPATT Power Section

Frequency range: 19.7-30.2 GHz  
Number of "building blocks": 5 (incl. preamplifier)  
Number of IMPATT devices: 14  
RF power output: 22W (min)  
Operating gain: 25 dB (min)  
RF input drive level: +18 dBm (nom)  
Gain compression ratio: 0.1 dB/dB (min)  
AM-PM conversion: 3 deg/dB (max)  
Noise figure: 37.5 dB (max)  
Input/output VSWR: 1.25:1 (max)  
DC Power requirement: 105W @ +26V  
Construction: Composite WG/TEM  
RF input/output interfaces: 1.5mm SMA/WR-42 WG

FET Specifications

Supplier - Varian, MSC, Dexcel

Frequency range: 19.7-20.2 GHz

| Driver stage deployment              | <u>1</u>                             | <u>2</u>                             |
|--------------------------------------|--------------------------------------|--------------------------------------|
| Small signal gain                    | 5.5 dB (min)                         | 4 dB (min)                           |
| Noise Figure                         | 6 dB (max)                           | 8 dB (max)                           |
| Output level @ 1 dB gain compression | +17 dBm(min)                         | +21 dBm(min)                         |
| DC bias requirement                  | 10 ma @ +3V<br>(drain)<br>-1V (gate) | 45 ma @ +6V<br>(drain)<br>-1V (gate) |
| Thermal resistance:                  | 300 deg C/W<br>(max)                 | 100 deg C/W<br>(max)                 |
| Configuration                        | carrier-mounted chip                 |                                      |

### FET Driver Section

Frequency range: 19.7-20.2 GHz

Number of stages: 2

Number of FET devices: 2

RF power output: 62.5 mW (nom)

Operating gain: 9 dB (min)

RF input drive level: 9 dBm (nom)

Gain compression ratio: 1 dB/dB

AM/PM conversion: 0

Noise figure: 8 dB (max)

Input VSWR: 1.25:1 (max)

Output VSWR: 2:1 (max)

DC bias requirement: 10 mA @ +3V  
45 mA @ +6V  
-1V

Construction: Composite WG/TEM

RF input/output interfaces: WR-42WG/1.5 mm SMA

B. DETAILED POC TEST PLAN/PROCEEDURES (2.4.3/2.4.4)

## TABLE OF CONTENTS

- 1.0 Introduction
- 2.0 Acceptance Tests
- 3.0 Thermal Vacuum Testing
- 4.0 Summary Tables
- 5.0 Test Descriptions
  - 5.1 Gain/Frequency/RF Power/Efficiency
  - 5.2 Noise Figure
  - 5.3 In Band Overdrive
  - 5.4 Input/Output VSWR
  - 5.5 Group Delay Variation
  - 5.6 Phase Linearity/AM to PM Conversion
  - 5.7 Harmonic/Spurious Response
  - 5.8 Thermal Vacuum Test
  - 5.9 Test Sequences
- 6.0 Test Equipment List
- 7.0 Test Discrepancies

## 1.0 INTRODUCTION

This test plan describes the test and methods which will be used to evaluate the performance of the 20 GHz IMPATT Transmitter (ITX) Proof-of-Concept Model. The formal test program will be based on the specifications and requirements outlined in contract NAS3-22491. The test plan consists of functional tests at room ambient temperature and atmospheric pressure and environmental tests to simulate space conditions. The functional tests are described in Sections 2.0, 4.0 and 5.0, whereas the thermal vacuum tests to be performed on the POC model are described in paragraph 5.8. All raw data taken during the acceptance tests will be properly recorded and analyzed for worst case performance unless otherwise noted.

## 2.0 ACCEPTANCE TESTS

Acceptance tests on three POC model IMPATT transmitter assemblies shall be conducted in a standard ambient environment to demonstrate that the POC Model design meets the RF performance specification outlined in the previously presented POC Model Design. One POC Model will be subjected to additional testing in a thermal vacuum environment. The standard ambient condition for conducting POC Model acceptance tests shall be as indicated below:

- a) Temperature, +60° to +80°F
- b) Relative humidity, 70 percent or less
- c) Barometric pressure, between 28 and 32 inches of mercury.

### 3.0 THERMAL VACUUM TESTING

Thermal vacuum testing will consist of mounting a POC model assembly on a baseplate which contains a reference temperature sensor and installing this assembly in a thermal vacuum chamber. Limited functional tests will be conducted at standard ambient conditions to establish a reference baseline. A vacuum of less than  $5 \times 10^{-5}$  torr is then established in the chamber and the limited functional tests are repeated at ambient temperature. Limited functional testing is then conducted at an elevated baseplate temperature of  $75^{\circ}\text{C}$ , and a reduced baseplate temperature of  $0^{\circ}\text{C}$ . A repeat of testing at ambient temperature in vacuum and at ambient pressure completes the thermal/vacuum test cycle.

### 4.0 SUMMARY TABLES

Table 4-1 summarizes the acceptance tests to be conducted on all three POC Model assemblies. Table 4-2 summarizes the limited functional testing and thermal/vacuum test sequence required for testing one POC Model in a thermal/vacuum environment.



TABLE 4-1

POC MODEL ACCEPTANCE TESTS  
(STANDARD AMBIENT ENVIRONMENT)

| <u>PERFORMANCE PARAMETER</u>  | <u>RANGE OF TEST PARAMETER</u>         | <u>TEST PROCEDURE</u><br><u>(PARAGRAPH)</u> |
|---|--|---|
| Frequency Range<br>RF Output Power/Gain<br>Gain Variation vs Freq.<br>Gain Slope<br>DC Power/Efficiency | RF 19.7-20.2 GHz                       | 5.1   |
| Noise Figure  | RF 19.7, 19.95, 20.2 GHz               | 5.2   |
| In-Band Overdrive   | RF 19.7, 19.95, 20.2 GHz               | 5.3   |
| Input/Output VSWR   | RF 19.7-20.2 GHz                       | 5.4   |
| Group Delay   | RF 19.7-20.2 GHz                       | 5.5   |
| AM-PM Conversion  | RF 19.7-20.2 GHz<br>(3 freq over band) | 5.6   |
| Phase Linearity   | RF 19.7-20.2 GHz                       | 5.6   |
| Harmonic/Spurious<br>Response   | RF 19.7-20.2 GHz                       | 5.7   |

TABLE 4-2

POC MODEL THERMAL/VACUUM TESTS

A. Limited Functional Testing

| <u>PERFORMANCE PARAMETER</u>                           | <u>RANGE OF TEST PARAMETER</u> | <u>TEST PROCEDURE</u> |
|--|--------------------------------|-----------------------|
| Frequency Range<br>RF Gain/<br>Gain Variation vs freq. | RF 19.7-20.2 GHz               | Gain Setup            |
| Gain Slope<br>DC Power                                 |                                |                       |

B. Test Sequence

|   | <u>Baseplate Temperature</u> | <u>Pressure</u> |
|---|------------------------------|-----------------|
| 1 | 60°-80°F                     | Ambient         |
| 2 | 60°-80°F                     | Vacuum          |
| 3 | 75°C                         | Vacuum          |
| 4 | 0°C                          | Vacuum          |
| 5 | 60°-80°F                     | Vacuum          |
| 6 | 60°-80°F                     | Ambient         |

5.0 TEST DESCRIPTIONS

5.1 Gain/Frequency Range/RF Output Power/Efficiency  
Gain Variations (3.2.2.1, 3.2.2.2, 3.2.2.4, 3.2.2.6,  
3.2.2.7, 3.2.2.15)

The power output variations and power output added efficiency will be measured using the test set-up of Figure 5-1. The unit will be mounted on a temperature controlled baseplate and will be powered with +28, +15, +5 and -15 VDC sources. D.C. voltages, currents and temperature of the unit will be continuously monitored and recorded at beginning and end of test. The test set-up will be initially calibrated for RF power and frequency range with the ITX unit removed. The power level into the ITX will be set to the nominal required level +13.0 dBm (20 mW). the frequency range will be set on a sweeper from 19.7 to 20.2 GHz. With the ITX removed, the response of the test set-up will be measured and stored in the memory of the network analyzer. The ITX will then be installed in the test set-up with power "ON" and the response of its gain displayed on the CRT of the network analyzer in "Memory Minus input" mode at 1 dB/Division sensitivity. The response will be plotted on the x-y recorder and properly annotated. All traces will be properly annotated for corresponding input power levels and analyzed for compliance to gain specifications. Output power and power added efficiency will be calculated from the gain data as follows:

- .  $P_{out} = P_{in} \times 10^G$ , where  $G = \text{Gain (dB)}/10$
- . Power added efficiency =  $\frac{P_{out} - P_{in}}{V_{DC} - I_{DC}} \times 100$

where  $V_{DC}$  AND  $I_{DC}$  are the DC voltage and current inputs, respectively, to the ITX

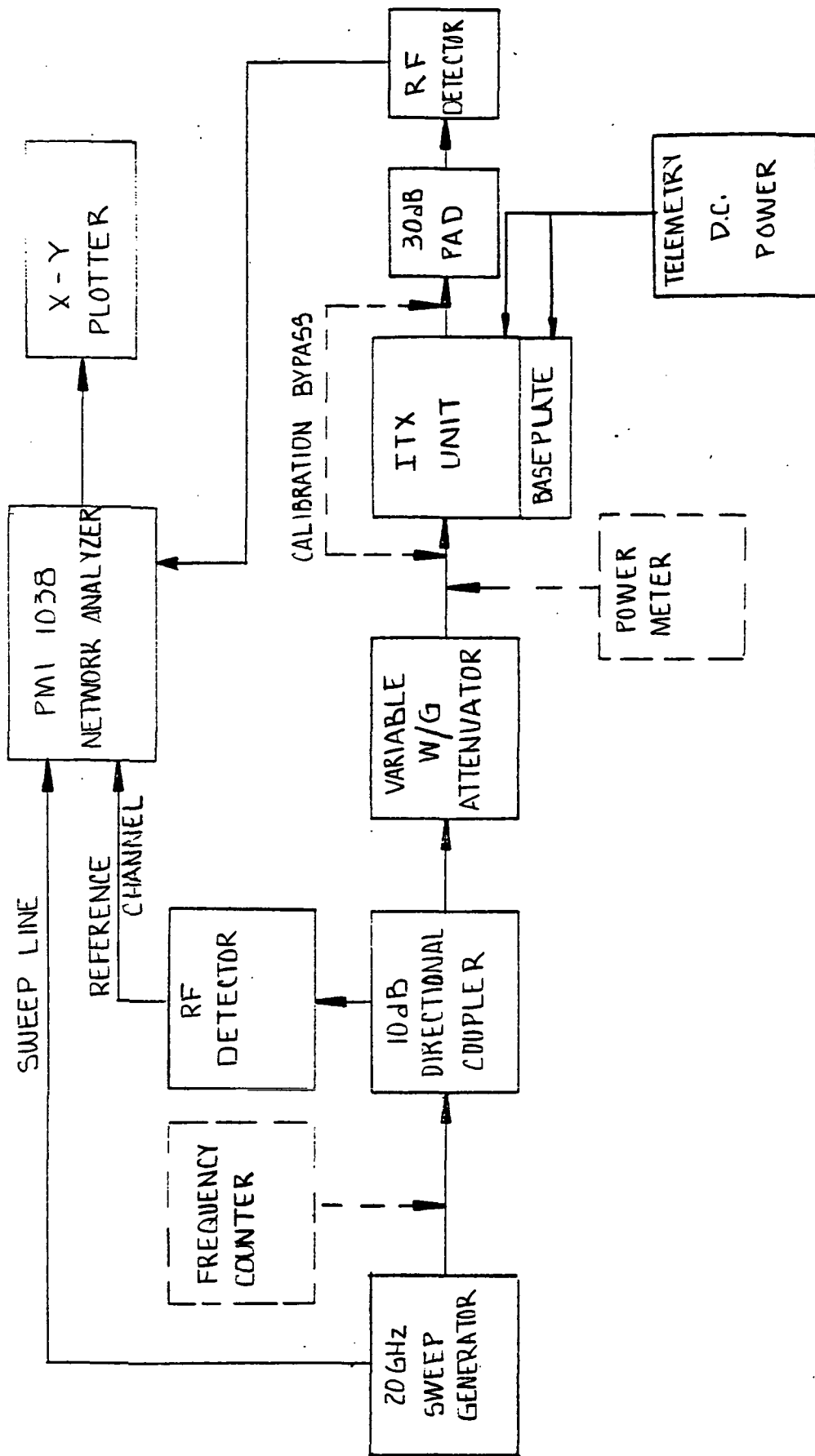


FIGURE 5.1 - GAIN, GAIN VARIATIONS, POWER OUTPUT TEST SET-UP

## 5.2 Noise Figure (3.2.2.3)

The operating noise figure of the ITX will be measured on a point by point basis at the nominal drive level +13.0 dBm using a calibrated noise diode, a mixer and automatic noise figure meter shown in Figure 5.2.

Set the signal generator to the lower band-edge frequency of 19.7 GHz. Adjust the tunable trap (T) to absorb the amplified signal at the output of ITX to a level below saturation of the mixer (M). Set the automatic noise figure meter to "CAL" and adjust the calibration to the excess noise ratio (ENR) of the calibrated noise diode at 19.7 GHz. Set the automatic noise figure meter to "AUTO" and read and record the corresponding noise figure in dB. Repeat test at mid-band (19.9 GHz) and upper band edge (20.2 GHz). Analyze results for compliance to specifications.

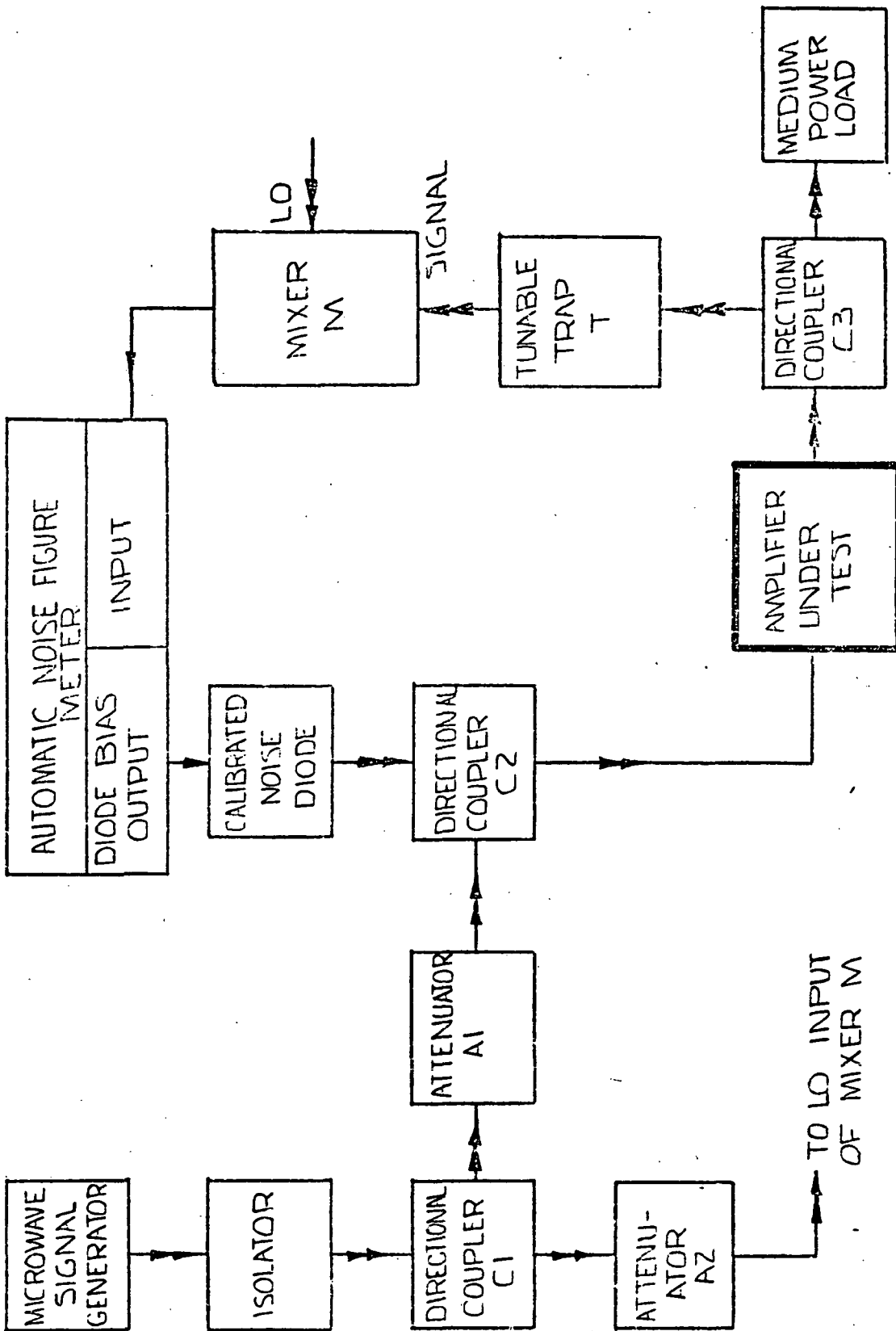


FIGURE 5.2 NOISE FIGURE MEASUREMENT SET-UP

### 5.3 In-Band Overdrive (3.2.2.5)

The in-band overdrive capability of the ITX will be measured using the test set-up of Figure 5.1. The input level into the ITX will initially be set to nominal +13.0 dBm and a swept gain response will be plotted on the x-y recorder. The input will be adjusted +5 dB and the output monitored on the CRT of the network analyzer. The above condition will be maintained for a short TBD time interval after which time the input level to the ITX will be adjusted back to nominal and a second gain trace plotted on the same graph sheet as the first trace. Data will be properly annotated and analyzed for degradation in performance of the ITX.



#### 5.4 Input/Output VSWR (3.2.2.8)

The VSWR tests will be performed using the test setup of Figure 5.3. The measurement will be made on a swept frequency basis in both operating and non-operating modes for the ITX. The nominal power level (+13.0 dBm) and frequency range (19.7-20.2 GHz) will be set at the input to the ITX. The test port will be calibrated with a matched load for the ITX port to be measured (1.30:1 Input and Output). A plot of the return loss response will be recorded on the x-y plotter via the PMI network analyzer. The matched load will then be replaced with the ITX port and a second plot recorded on the same x-y graph sheet. The data will be properly annotated and analyzed for compliance. The test will be similarly repeated with ITX in non-operating mode and for the remaining port using the appropriate matched load. All data will be analyzed for compliance to specifications.

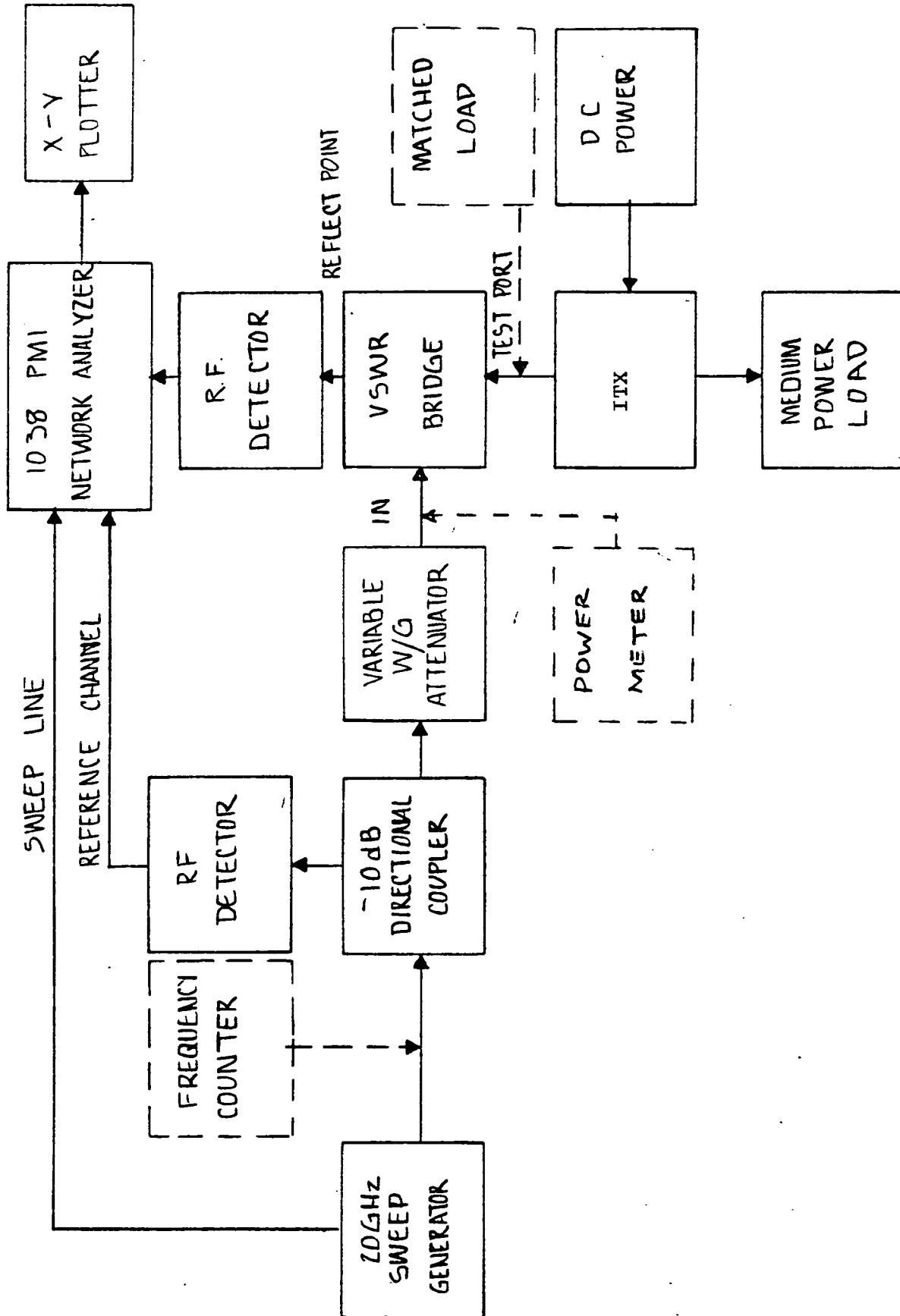
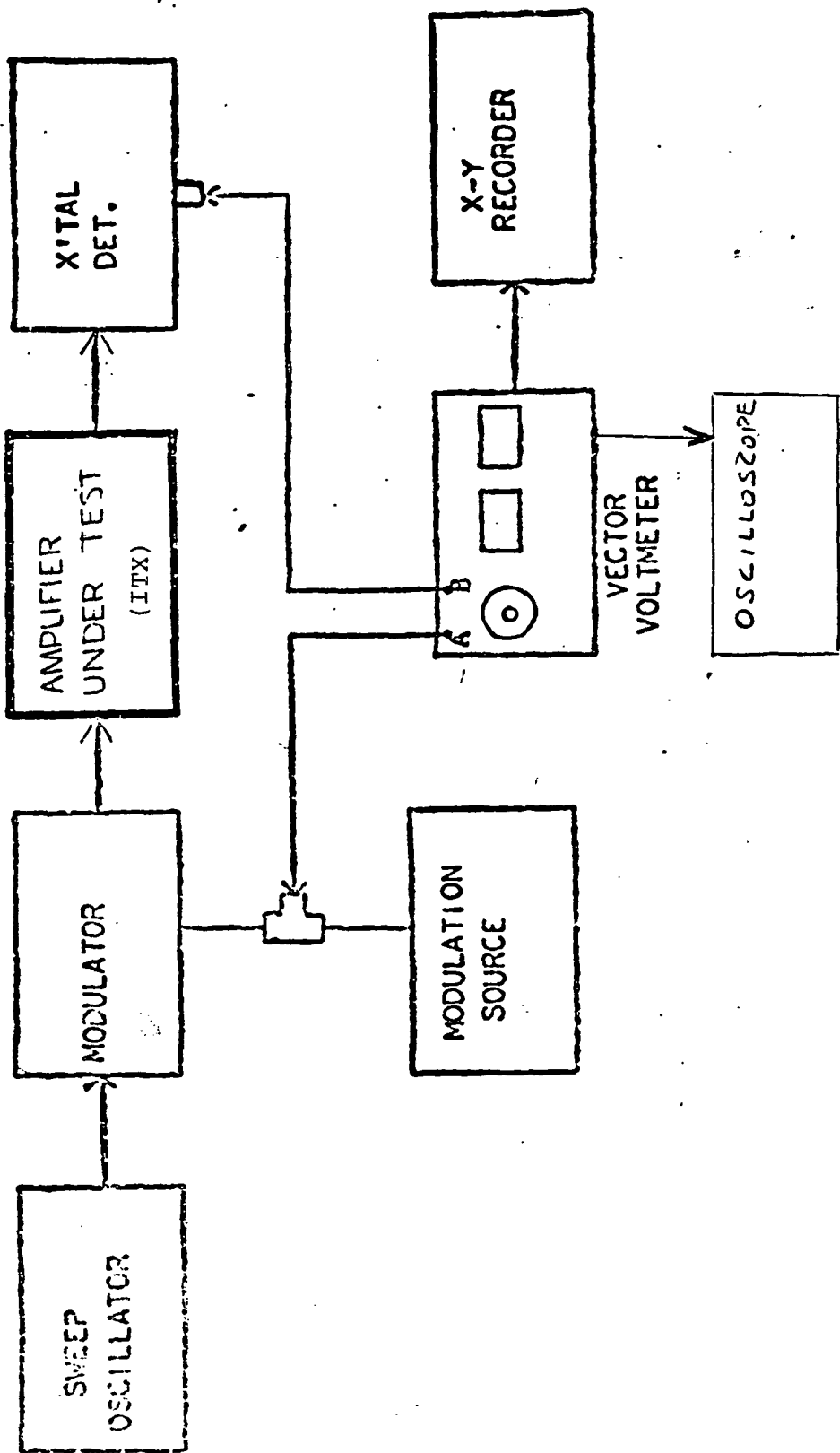


FIGURE 5.3 VSWR INPUT/OUTPUT TEST SET-UP

### 5.5 Group Delay Variation (3.2.2.10)

The group delay variation of the ITX will be measured using the test set-up of Figure 5.4. The sweep oscillator will be set to sweep a 1 GHz band centered on 20 GHz and a slow sweep time of 1 to 10 secs. A 20 GHz pin modulator will be driven with a 1 MHz to 10 MHz modulation frequency. The RF power and modulator signal amplitude will be adjusted to obtain an undistorted sinewave on channel B of the Vector Voltmeter using an oscilloscope, as shown. The signal amplitudes into channel A and B will be adjusted for equal levels using the variable attenuator. The x-y recorder will be calibrated for phase resolution with ITX removed. A group delay response plot of the ITX will be made after inserting the unit into the test setup. Data will be annotated and analyzed for compliance.



GROUP DELAY SETUP

FIGURE 5.4

## 5.6 Phase Linearity/AM To PM Conversion (3.2.2.13, 3.2.2.12)

The test set-up of Figure 5.5 will be used for these measurements. Initially, an electrical equivalent length of the ITX will be installed in the test set-up. The power level (+13.0 dBm) will be set before the 30 dB pad to obtain equal levels at the "REF" and "test" ports of the harmonic converter. The sweeper will be set to the frequency range 19.7-20.2 GHz. With the test set-up calibrated, the transmission test set unit will be adjusted to display phase response on the HP network analyzer at a sensitivity of  $45^{\circ}/\text{Div}$ . The phase output of the analyzer will be expanded from 10mv/degree to 100mw/div on the linear amplifier of the PMI Analyzer. The response will be stored in memory. The w/g electrical length will be replaced with the ITX unit in operating mode. The phase response of the ITX will then be displayed on the PMI analyzer CRT in "Input Minus Memory" condition and the trace plotted on calibrated graph sheet using the x-y recorder. Without disturbing the test set-up, the input power into the ITX will be adjusted  $\pm 2$  dB from nominal power level using the w/g variable attenuator. The resultant responses will be plotted on the same graph sheet. All data will be annotated and analyzed for compliance.

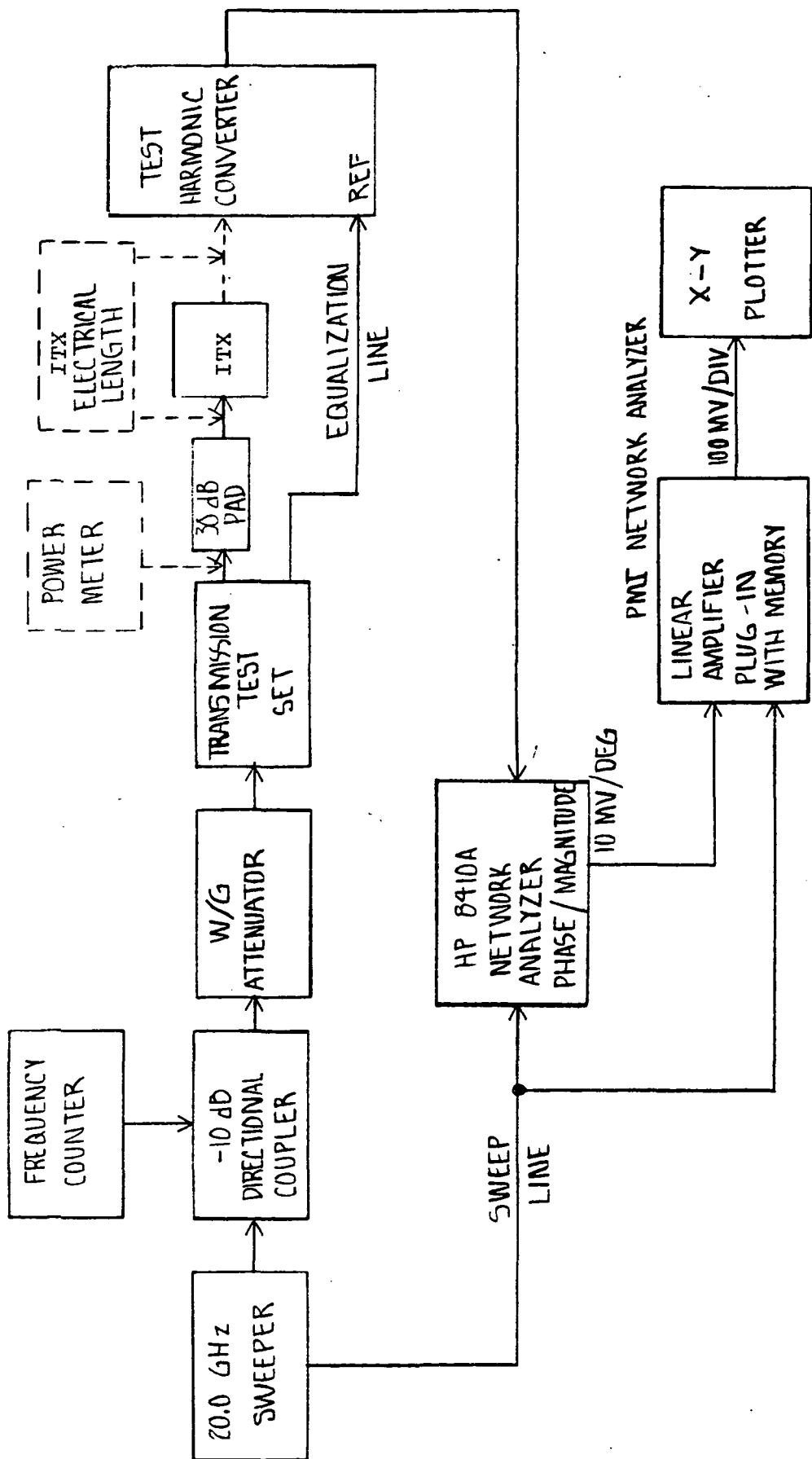


FIGURE 5.5 PHASE LINEARITY, AM-PM CONVERSION TEST SET-UP

5.7 Harmonic/Spurious Outputs (3.2.2.14)

The spurious outputs requirement will be satisfied by manually sweeping a CW signal of nominal power level (+13 dBm) into the ITX and observing the output with a spectrum analyzer. Harmonic and non-harmonic components will be observed on the calibrated display of the spectrum analyzer and signal level and frequency of each recorded on a data sheet. The sensitivity of the spectrum analyzer will be set to a minimum 60 dBc range to satisfy the requirement for non-harmonic components levels. In addition, an automatic preselector (HP8443A) will be used in conjunction with the spectrum analyzer to filter mixing and spurious responses of the L.O sources in the analyzer.

### 5.8 Thermal Vacuum Test (3.2.3)

The thermal vacuum requirements for the ITX will be satisfied upon successful completion of the initial functional tests outlined in sections 5.1 through 5.7. A thermal vacuum chamber will be used for the tests as shown in Figure 5.6. The ITX unit will be mounted on a baseplate inside the thermal vacuum chamber with a temperature sensor attached to the plate for monitoring the operating temperature inside the chamber. A limited functional test (LF) consisting of a gain response will be performed prior to evacuation of the chamber to establish a reference baseline (see timeline Figure 5.7). This will be accomplished as discussed in the gain test of paragraph 5.1 of this section. Upon evacuation to the desired level of  $1 \times 10^{-10}$  torr the baseplate temperature will be raised to 165°F and a second gain trace will be recorded after a stabilization period of TBD hours.

After a four (4) hour dwell at 165°F the baseplate temperature will be lowered to 30°F. A gain trace will be recorded at 30°F after a stabilization period of TBD hours. The baseplate temperature will be returned to room ambient after completion of a four (4) hour dwell at 30°F. A final gain trace will be recorded after venting the chamber. All data will be compared for repeatability and compliance to gain performance requirements.



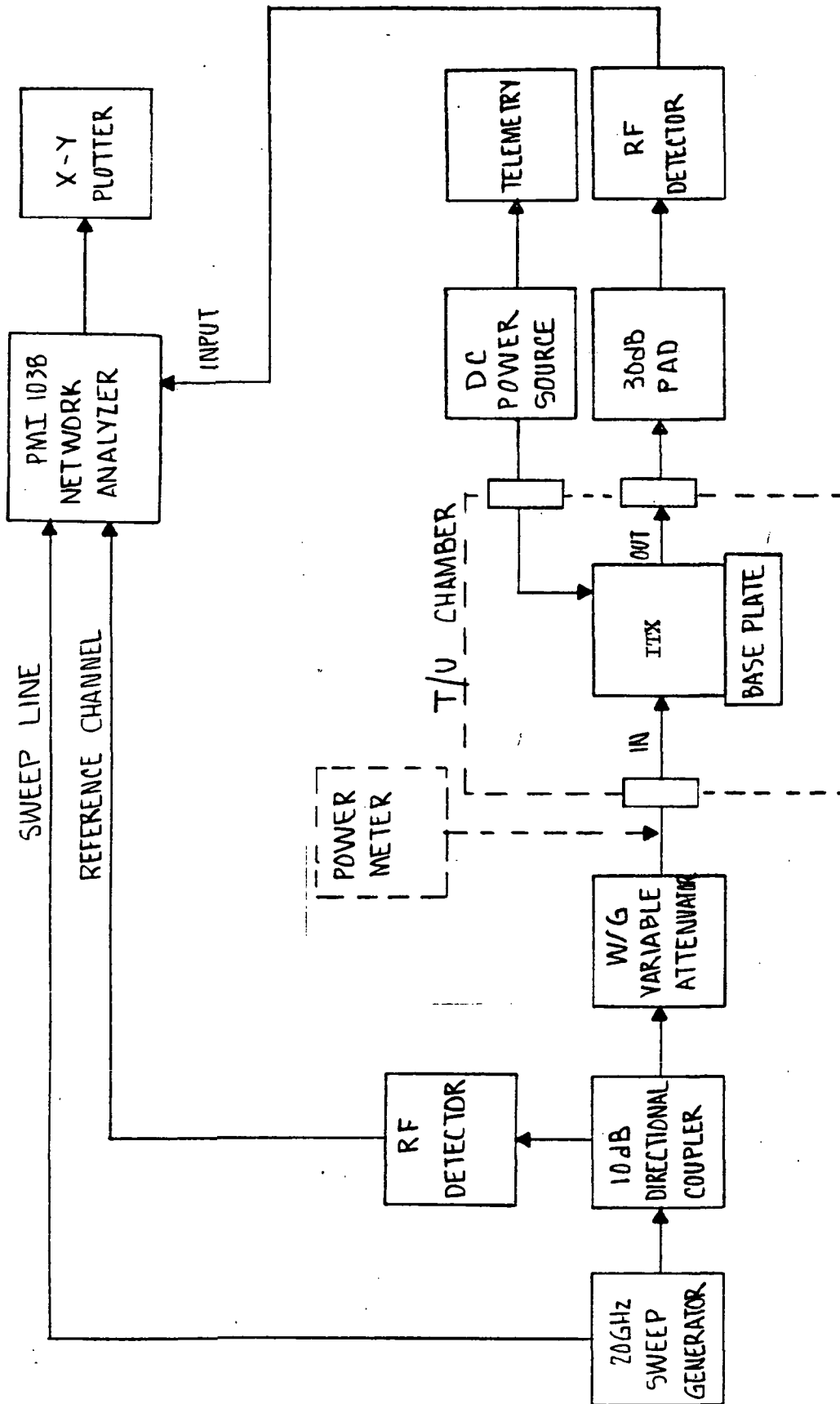


FIGURE 5.6 T/V LIMITED FUNCTIONAL TEST SET-UP

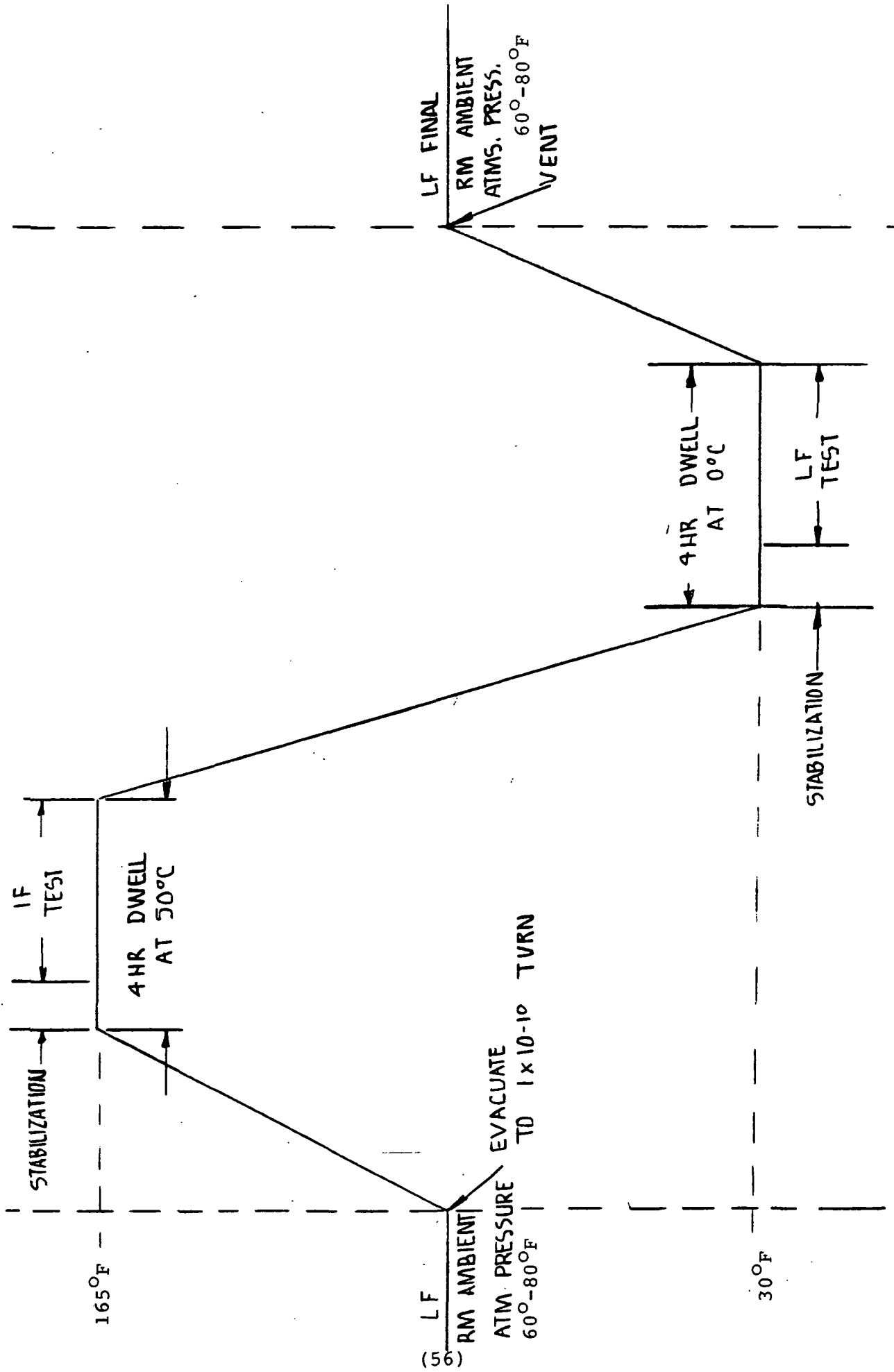


FIGURE 5.7 T/V TIME LINE

## 5.9 Test Sequence

The test sequence for the acceptance test program will be performed as follows:

- . Initial functional tests
- . Thermal vacuum tests
- . Final functional tests

All tests are described in the preceding sections. Initial and final functional tests will be performed to verify the repeatability of data and will be performed at ambient conditions.

## 6.0 TEST EQUIPMENT LIST

The following list of test equipment on its equivalent will be used to perform the tests in this plan.

| <u>DESCRIPTION</u>        | <u>MFG/MODEL</u>     |
|---------------------------|----------------------|
| CW Signal Generator       | HP628A               |
| 20 GHz Sweeper            | HP8690B              |
| Network Analyzer          | PMI1038              |
| Network Analyzer          | HP8410A              |
| Sweep Amplitude Plug-In   | PMI 1038-H13         |
| Log Amp/Memory Plug-In    | PMI 1038-V12         |
| Linear Amp/Memory Plug-In | PMI 1038-V20         |
| Phase Magnitude Plug-In   | HP8412A              |
| Spectrum Analyzer         | HP141T/8555A/8554B   |
| RF Detector (2)           | PMI 12466            |
| RF Crystal Detector       | Aertech W806FS       |
| Power Meter               | HP431B               |
| Thermistor Head           | HPK486A              |
| Waveguide Attenuator      | Flan Microwave 20/11 |
| Noise Figure Meter        | Ailtech 7514         |
| Oscilloscope              | Tektronics 465       |
| Digital Voltmeter         | Simpson 464          |
| D.C Power Supply          | Kepeco JOE 55-10M    |
| Noise Diode               | Ailtech              |
| X-Y Plotter               | PMI 1034             |
| Harmonic Converter        | HP8411A              |
| VSWR Bridge               | Narda 5082           |
| Frequency Counter         | SD 6054B             |

6.0 TEST EQUIPMENT LIST (CONT'D)

| <u>DESCRIPTION</u>    | <u>MFG/MODEL</u>   |
|-----------------------|--------------------|
| Transmission Test Set | HP8740A            |
| Directional Coupler   | HP11692D           |
| Yig Preselector       | HP8445B            |
| RF Switch (2)         | HP8761A            |
| Mixer (20 GHz)        | Honeywell SMC-1826 |
| Vector Voltmeter      | HP8405A            |
| Modulator (20 GHz)    | Narda              |

## 7.0 TEST DISCREPANCIES

Any discrepancies observed during the course of POC Model acceptance testing will be immediately flagged and brought to the attention of the cognizant quality assurance engineer. QA will convene a review board consisting of the technical program manager, director of quality assurance, the quality engineer, reliability engineering, and the director of high-rel engineering. This board will (a) document the nature of the discrepancy; (b) attempt to isolate the cause i.e. test set-up, design, component failure etc; (c) direct further failure analysis and (d) define retest requirements.

The nature of any discrepancies will be categorized into one of three possible types:

- 1) Performance Discrepancy whereby the POC model measured performance of a particular parameter is below the anticipated design goal. In this case the equipment log will be carefully reviewed and acceptance test data compared to manufacturing test data and pre-A.T. integration data. This will ascertain whether or not the discrepancy is historical to the sub-assembly involved. If so, design engineering will recommend modifications or follow-on technology development leading to improved performance for flight hardware. Acceptance testing will continue from the point where the discrepancy was noted. If the anomaly can not be explained from past performance records, category 2 applies, as described below.
- 2) A shift or change is observed in one or more parameters which affects performance relative to design goal. The unit will be removed from acceptance test and evaluated to determine the sub-assembly or component requiring adjustment/realignment. If the affected area is one previously defined as being of flight type design, extensive failure analysis will be performed and appropriate design modification recommendations made. Depending on the outcome of said failure analysis the unit may be returned to test in sequence or retest ordered from initial acceptance test.

- 3) Complete loss of performance whereby the POC model ceases to function. In this case the unit will be removed from test and submitted for failure analysis which will determine the mode of failure, recommend design modifications, if any, and define any repair action to be implemented. Depending on the outcome of said analysis the unit may be returned to test in sequence or retest ordered from initial acceptance test.

Any and all test discrepancies will be duly recorded in the POC model equipment log. The results of all failure analysis will be fully documented via a failure analysis report and said report will become a permanent part of the acceptance test data package for the POC Model as well as the acceptance test report. Design modification recommendations or recommendations for follow-on technology development which may result from any test discrepancies will be included in the formal analysis of test results.

D. 20 GHz SINGLE DRIFT GaAs IMPATT  
DIODE RELIABILITY ASSESSMENT

S. PICONE, Y. CHO AND J.R. ASMUS

FINAL REPORT

NASA CR 174716

DECEMBER, 1983

Prepared For:

NASA Lewis Research Center  
Cleveland, Ohio

CONTRACT NASA-NAS3022491



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- 4.0 SUMMARY AND CONCLUSIONS



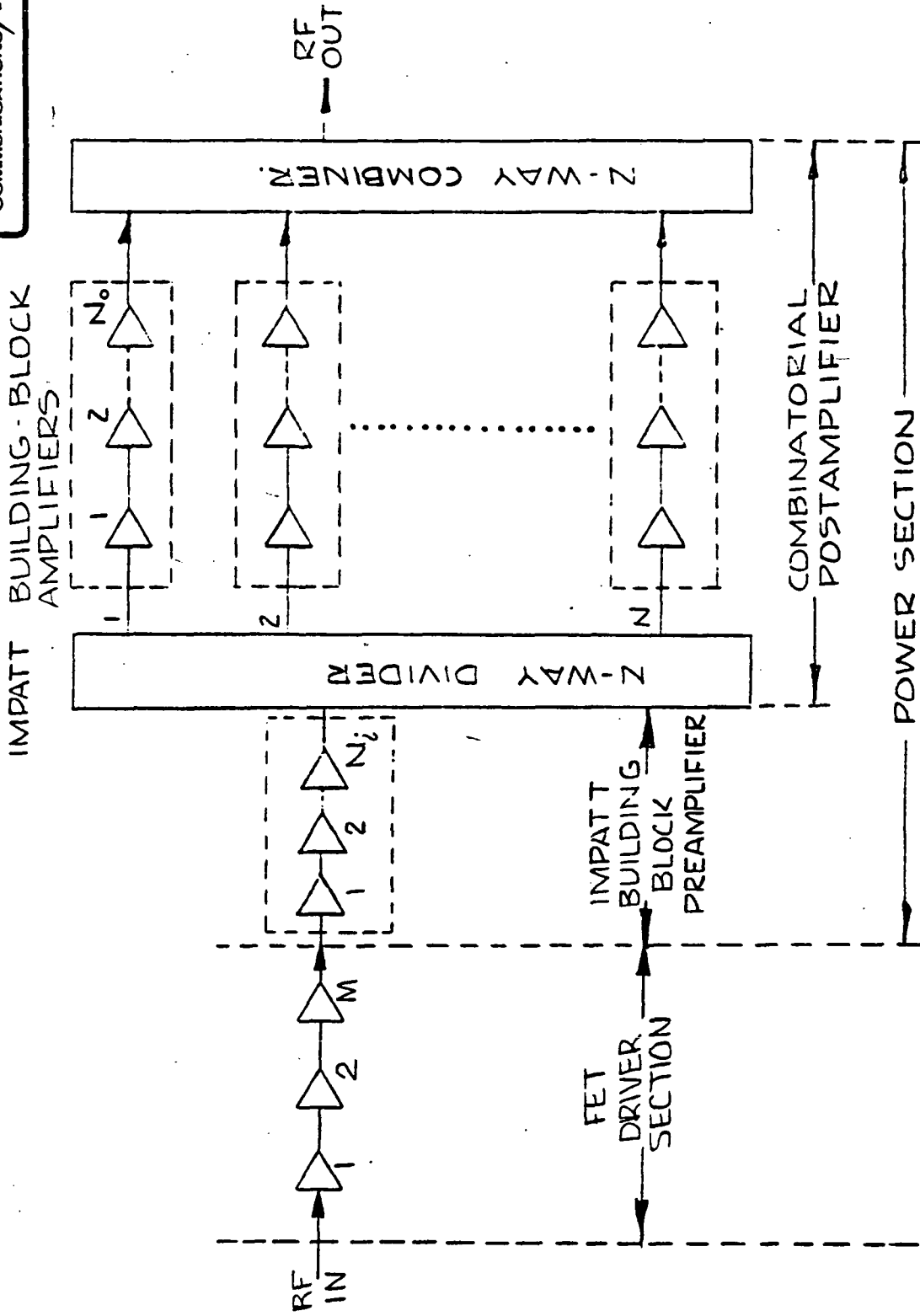
1.0 DEVICE/ASSEMBLY DEVELOPMENT - DEFINITION



### 1.1 20 GHz IMPATT TRANSMITTER FUNCTIONAL TOPOLOGY

The 20 GHz IMPATT transmitter RF assembly, in its most general form, consists of the cascaded combination of a FET driver section and an IMPATT power section. The FET driver section, in turn, comprises a cascade of low to medium power FET amplifier stages whereas the IMPATT power section consists of a multistage IMPATT preamplifier driving a combinatorial IMPATT postamplifier. The latter is configured as an array of identical multistage IMPATT "building blocks", paralleled between identical N-way power divider and combiner. In the most general case, the number of IMPATT amplifier stages comprising the preamplifier ( $N_1$ ) and postamplifier "building block" ( $N_0$ ) are different. The order (N) of power combination required is determined by the RF power capability of each "building block" which in turn determines how many paralleled "building blocks are required to provide the required RF power output (20W).





FUNCTIONAL RF TOPOLOGY OF 20GHz IMPATT TRANSMITTER

### 1.2. 20 GHz SOLID STATE TRANSMITTER-SPECIFIC DESIGN OBJECTIVES

The primary design requirement on the subject 20 GHz transmitter is that it provides 20W (minimum) K-band RF power output over a 500 MHz bandwidth centered near 20 GHz with 20 percent DC bias/RF power added efficiency. (the latter excluding the efficiency degradation due to DC power conditioning components). Moreover, this transmitter must provide 30 dB power gain to a single, angle modulated (PM) carrier, concurrent with 25 dB maximum noise figure, and a high degree of amplitude and delay flatness ( $\pm 1$  dB and  $\pm 5$  deg. overall passband deviation from gain flatness and phase linearity and 0.15 dB/MHz and 0.5nS/50 MHz maximum gain and delay slope). For the specified single PM carrier, the transmitter output amplitude can be into saturation provided that the requirements on such linearity-related performance parameters as AM/PM conversion ( $5 \pm 1$  deg/dB max) and harmonic/nonharmonically related spurious content ( $\sim 50/60$  dBc max) are satisfied. Finally, to accommodate representative spacecraft thermal profiles, specified performance must be achieved over a 0-75°C baseplate temperature range.



20 GHz SOLID STATE TRANSMITTER-SPECIFIC DESIGN OBJECTIVES

DESIGN OBJECTIVE (OVER PASSBAND)

PARAMETER

|   |   |
|---|---|
| INPUT SIGNAL FORMAT                                 | ANGLE MODULATED, SINGLE CARRIER                 |
| CENTER FREQUENCY                                    | 19.95 GHZ                                       |
| RF PASSBAND (500 MHZ)                               | 19.7 TO 20.2 GHZ                                |
| SATURATED RF OUTPUT POWER (LOAD VSWR $\leq 1.3:1$ ) | 20 WATTS (MIN)                                  |
| NOISE FIGURE  | 25 DB (MAX)                                     |
| RF GAIN @ SATURATION                                | 30 DB $\begin{matrix} +0 \\ -1 \end{matrix}$ DB |
| IN BAND OVERDRIVE SURVIVABILITY                     | 5 DB ABOVE NOMINAL INPUT LEVEL                  |
| GAIN VARIATION                                      | $\pm 1$ DB (MAX)                                |
| GAIN SLOPE  | 0.15 DB/MHZ (MAX)                               |
| INPUT AND OUTPUT VSWR                               | 1.3:1 (MAX)                                     |
| GROUP DELAY VARIATION                               | 0.5 NS P-P (MAX) OVER 50 MHZ SLOT               |
| AM/PM CONVERSION                                    | 5 $\pm 1^\circ$ /DB (MAX)                       |
| PHASE LINEARITY                                     | 10 $^\circ$ P-P (MAX)                           |
| HARMONIC RESPONSE (AT SATURATION)                   | 50 DB BELOW CARRIER                             |
| SPURIOUS RESPONSE (AT SATURATION)                   | 60 DB BELOW CARRIER                             |
| DC-RF EFFICIENCY                                    | 20% (MIN) - EXCLUDING POWER SUPPLIES            |
| INTERFACE   | WR-42 WAVEGUIDE                                 |
| BASEPLATE TEMPERATURE                               | 0 to 75 $^\circ$ C                              |



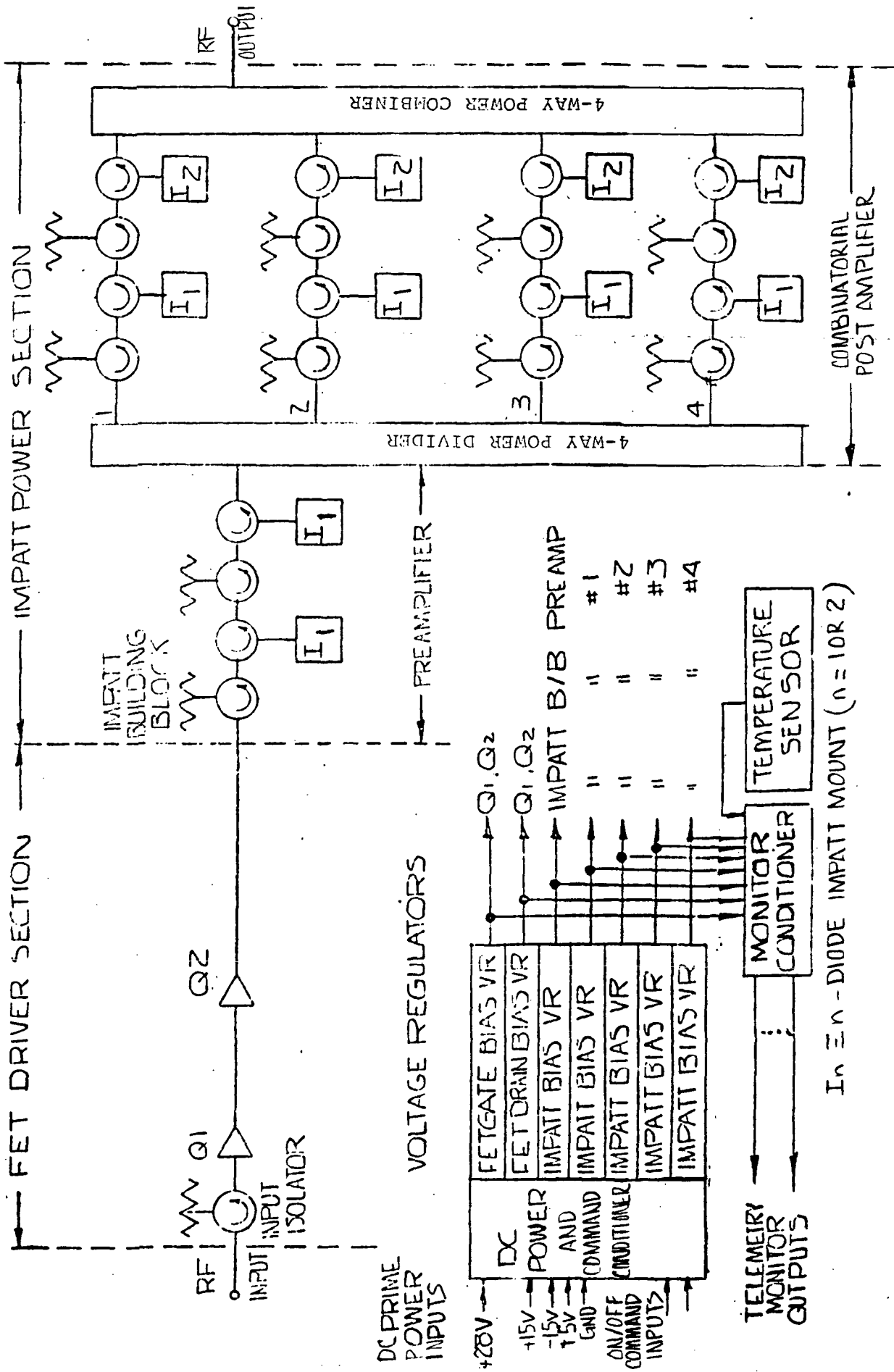
### 1.3 PREFERRED 20 GHz TRANSMITTER CONFIGURATION

Based upon the results of detailed ongoing tradeoff analyses, the preferred 20 GHz IMPATT transmitter configuration consists of:

- IMPATT power section comprising two stage circulator coupled 2W IMPATT preamplifier cascaded with a four-way combinatorial postamplifier formed by four paralleled two-stage 6W IMPATT "building block" amplifiers, paralleled between identical four way reactive power divider and combiner;
- two stage 20 mW single-ended common source FET driver amplifier with integral input isolator;
- DC power/command conditioner, comprising power distribution network coupled to individual DC bias voltage regulators for FET driver amplifier and for each two stage IMPATT "building block" and including "shutdown" and "turn-on" circuits which respond to input commands;
- monitor conditioner providing analog DC outputs which are linearly related to key transmitter operating parameters, e.g., secondary DC bias currents, physical temperature, etc.

This design assumes that the required primary DC input voltages are provided from a central spacecraft DC/DC conversion subsystem, such as often is done for maximum efficiency, in practical spacecraft deployments. (Alternately, a dedicated DC/DC converter, operating off a single +28V prime input bus, can be incorporated in the transmitter DC power conditioning subassembly).





In  $n$  - DIODE IMPATT MOUNT ( $n = 1$  OR  $2$ )



BLOCK DIAGRAM OF POC MODEL 20 GHz IMPATT TRANSMITTER DESIGN



#### 1.4 20 GHz TRANSMITTER-CRITICAL TECHNOLOGY ITEMS

The critical areas of technology applicable to the subject 20 GHz transmitter fall into two general categories, functional circuits, and constituent devices and materials. In terms of the previously depicted functional RF block diagram of a composite 20 GHz FET/IMPATT transmitter, the key circuit technologies which must be developed (and demonstrated in breadboard form) at 20 GHz, include IMPATT power amplifiers, FET driver amplifiers, RF power dividers/combiners and ferrite circulators. The foregoing technology development in turn depends upon the concurrent development and/or evaluation of such critical 20 GHz device and material technologies as Read-profile GaAs epitaxial wafer material, GaAs Read-IMPATT diodes and GaAs FET devices.

None of the above requires any new fundamental breakthroughs but rather represents an extension of the existing state of the art in these technologies at lower frequencies to the more severe constraints associated with operation at 20 GHz. Moreover, an assessment of the status of appropriate 20 GHz technology available from credible outside suppliers indicated that, with the exception of the FET devices (available from several FET vendors) and GaAs epiwafers (available from two credible GaAs epifafer suppliers), all of above will be developed and implemented in house.

D.C. power and command conditioning and monitor circuits, although required to implement the over transmitter, were not considered for technology development since such circuit designs are already well established.



20 GHZ TRANSMITTER - CRITICAL TECHNOLOGY ITEMS

1. FUNCTIONAL CIRCUIT TECHNOLOGY
  - . IMPATT POWER AMPLIFIERS
  - . FET DRIVER AMPLIFIERS
  - . RF POWER DIVIDERS/COMBINERS
  - . FERRITE CIRCULATORS
2. CONSTITUENT DEVICE/MATERIAL TECHNOLOGY
  - . READ-PROFILE GAAS EPITAXIAL WAFER MATERIAL
  - . GAAS READ-IMPATT DIODES
  - . GAAS FET DEVICES



## 1.5 SCOPE OF 20 GHz DEVICE/ASSEMBLY TECHNOLOGY DEVELOPMENT

In order to address the previously enumerated critical technology areas identified in the preferred 20 GHz transmitter design approach, the following key 20 GHz devices and circuits were developed and demonstrated in breadboard form within the device/assembly technology task:

- . SDR GaAs Schottky modified-Read-profile IMPATT diodes, in stud-mounted encapsulated structures;
- . Dual-junction (six port) stripline circulator;
- . Coaxial one-port IMPATT test mount for diode impedance measurements and single stage test amplifier experiments;
- . Two stage, circulator coupled, composite TEM line IMPATT "building block" amplifier, incorporating single IMPATT diode per stage;
- . Single-stage duroid-based microstrip FET amplifier, utilizing procured FET chip mounted on customized in-house carrier;
- . Four way waveguide reactive junction power divider/combiner.

The goals on developed device/assembly performance, enumerated in the above table, are consistent with the previously described preferred 20 GHz transmitter design, which assumed 6W dual diode IMPATT building block output stages.



SCOPE OF 20 GHz DEVICE/ASSEMBLY TECHNOLOGY DEVELOPMENT

A - IMPATT POWER SECTION

1. ELEMENTS TO BE DEVELOPED @ 20 GHz
  - . GaAs READ-IMPATT DIODES
  - . CIRCULATOR-COUPLED IMPATT TEST AMPLIFIER
  - . 4 WAY POWER DIVIDER/COMBINER
  - . TWO-STAGE IMPATT "BUILDING BLOCK" AMPLIFIER
2. OBJECTIVES OF BREADBOARD DEVELOPMENT - DEMONSTRATION OF PERFORMANCE CAPABILITIES/GOALS AND VALIDATION OF DESIGN OF 20 GHz
  - . IMPATT DIODES: 1.5-2W (MIN) RF POWER @ 20-25% (MIN) EFFICIENCY (IN TEST OSC.)
  - . CIRCULATORS: 0.25 dB (MAX) INS. LOSS/PASS AND 20 dB MIN ISOL/RET. LOSS OVER 2 GHz MIN BW
  - . BUILDING BLOCK AMPLIFIERS:  $\geq$ 2.5-3W MIN RF OUTPUT OVER 0.5 GHz MIN BW
  - . 4 WAY P/D, P/C:  $\leq$ 0.25 dB MAX RESIDUAL LOSS OVER 0.5 GHz MIN BW
3. CONSTRUCTION / IMPLEMENTATION APPROACHES
  - . ENCAPSULATED, STUD-MOUNTED IMPATT DIODES
  - . COAXIAL IMPATT TEST MOUNT
  - . STRIP-LINE CIRCULATOR FOR TEST AMPLIFIER
  - . COMPOSITE TEM-LINE TWO-STAGE IMPATT "BUILDING BLOCK"
  - . WAVEGUIDE REACTIVE-JUNCTION 4 WAY DIVIDER/COMBINER

B - FET DRIVER SECTION

1. ELEMENTS TO BE DEVELOPED @ 20 GHz
  - . TEST AMPLIFIER
2. OBJECTIVES OF BREADBOARD DEVELOPMENT
  - . SELECTION OF PREFERRED FET DEVICE
  - . DEMONSTRATION OF DRIVER AMPLIFIER PERFORMANCE CAPABILITY
  - . VALIDATION OF DRIVER AMPLIFIER DESIGN
3. CONSTRUCTION/IMPLEMENTATION APPROACHES
  - . FET DEVICES IN CHIP FORM, MOUNTED ON CUSTOMIZED IN-HOUSE CARRIERS
  - . DUROID-BASED MICROSTRIP FET AMPLIFIER STAGE W/ $>$  5 dB LINEAR GAIN,  $>$ 0.5 GHz BW AND  $>$ 50 mW OUTPUT LEVEL @ 1 dB GAIN COMPRESSION



2.0 20 GHz IMPATT DIODE DEVELOPMENT



## 2.1 PROGRAM OBJECTIVES

In order to satisfy the performance objectives on the overall 20 GHz IMPATT transmitter, the corresponding design goals on the 20 GHz IMPATT diodes to be deployed therein are as follows:

- . RF power output: 1.5 to 2.0W CW (min)
- . Frequency: 20 GHz (nom.)
- . DC-RF conversion efficiency: 20-25 percent (min)

The frequency design objectives, directed to measured IMPATT diode performance in a 20 GHz waveguide test oscillator, is consistent with the requirements dictated by the previously depicted preferred 20 GHz transmitter configuration. The high DC-RF conversion efficiency requirement necessitates the use of GaAs as the diode semiconductor material, as opposed to the less efficient albeit more mature Si technology.

A vital part of the overall GaAs IMPATT diode development effort was the selection, evaluation and collaboration with one or more outside suppliers of state-of-the-art epitaxial GaAs material, grown to LNR specification.



PROGRAM OBJECTIVES

DEVELOP ADVANCED - GaAs IMPATT DIODE TECHNOLOGY FOR 20 GHz  
20 WATT SOLID STATE SPACEBORNE TRANSMITTER

DEVICE GOALS

|                           |                   |                           |
|---------------------------|-------------------|---------------------------|
| RF POWER OUTPUT ( $P_o$ ) |                   | 1.5 to 2.0 WATTS CW (min) |
| FREQUENCY                 | ( $f_o$ )         | 20 GHz (nom)              |
| EFFICIENCY                | ( $\eta$ )        | 20-25 Percent (min)       |
| THERMAL RESISTANCE        | ( $\theta_{th}$ ) | 25 Degrees C/W (max)      |



## 2.2 DEVICE DESIGN CONSIDERATIONS

Alternatives considered during the evaluation of an optimum 20 GHz GaAs IMPATT device design encompassed:

- a) GaAs epitaxial growth technique
  - . VPE - vapor phase epitaxy
  - . MBE - molecular beam epitaxy
- b) doping profile
  - . single versus double drift (SDR vs DDR)
  - . high-low (HL) vs low-high-low (LHL)
- c) junction formation
  - . grown (p-n) vs Schottky (SDR only)
  - . single versus multiple mesa cross sections
  - . simple versus complex structure
- d) heat sinking
  - . gold plated versus metallized diamond heat sink (PHS vs DHS)
- e) packaging alternatives
  - . hermetically sealable package versus open structure
  - . single versus multiple chip embedding

The criteria utilized in enduring a preferred device design from among the above alternatives included:

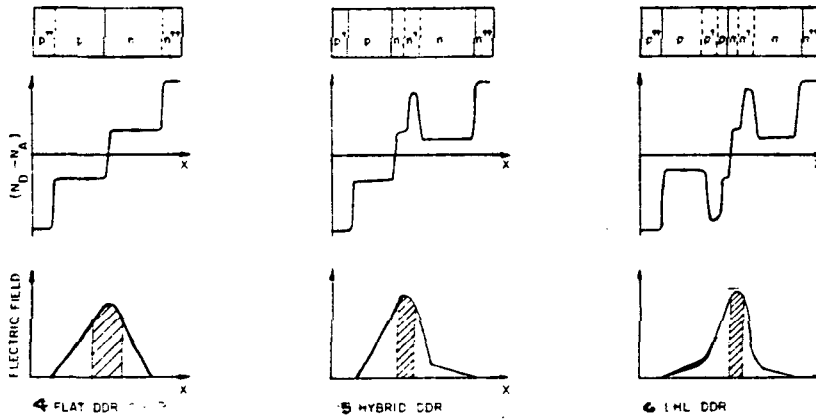
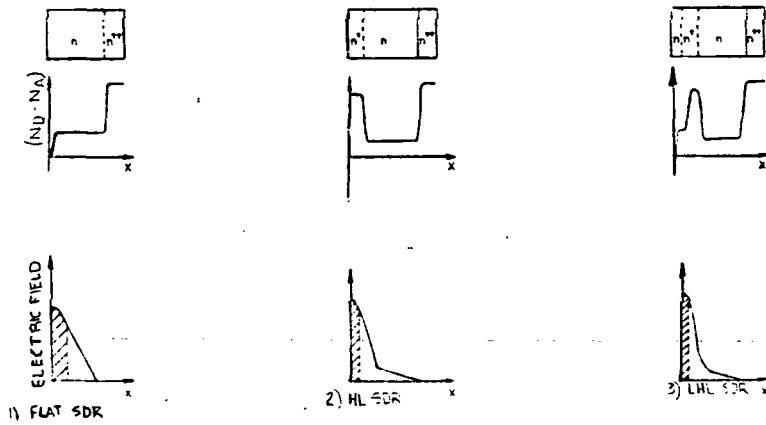
- . potential RF performance
- . realizability of epitaxially grown doping profile
- . practicality of associated processing

These criteria were also applied within the context of the capabilities of several potential outside sources of epitaxial grown GaAs wafers.

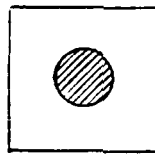




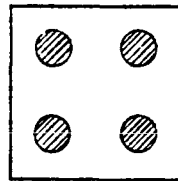
# IMPATT DEVICE DESIGN ALTERNATIVES



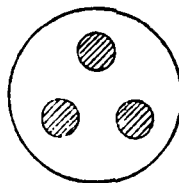
## A-ALTERNATIVE DOPING PROFILES



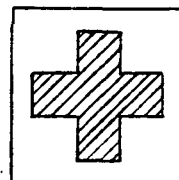
(1)



(2)



(3)



(4)

## B- ALTERNATIVE MESA CROSS SECTIONS



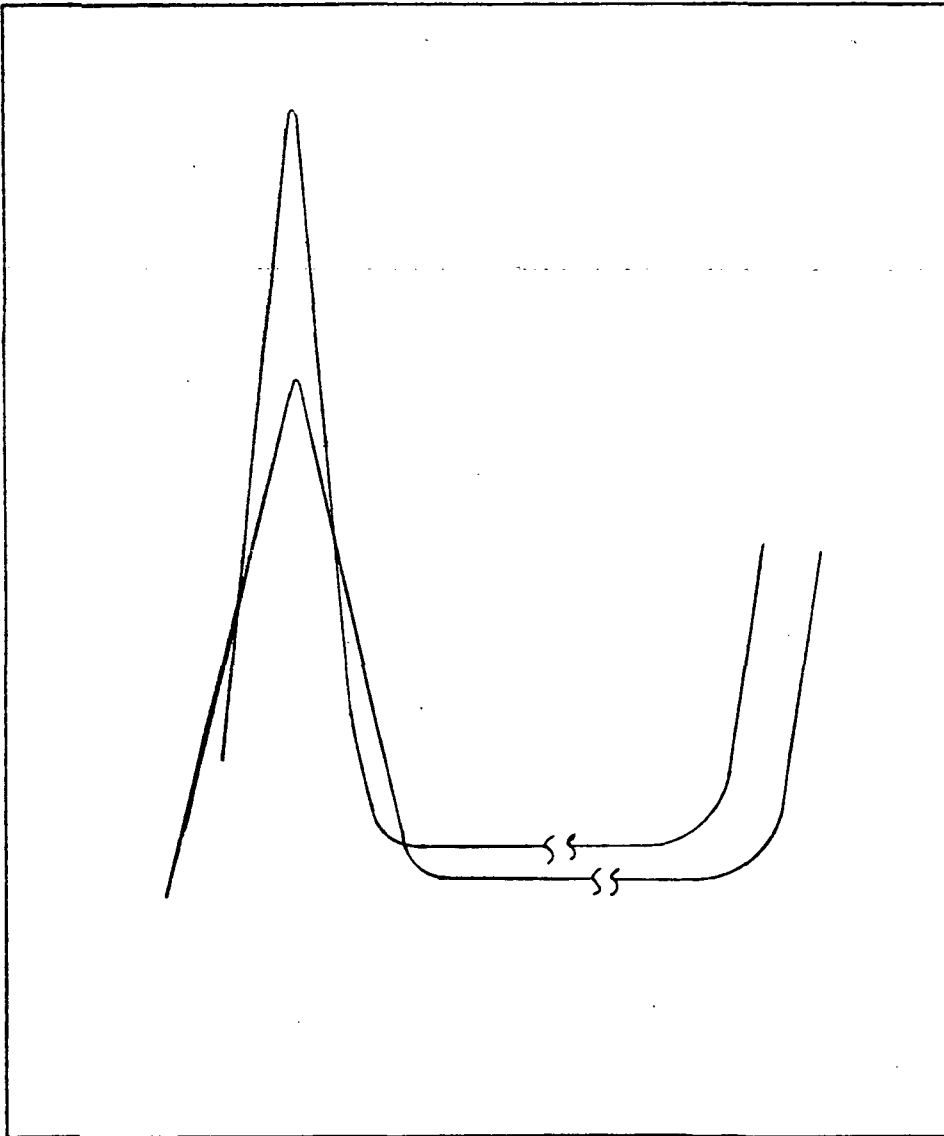
### 2.3 PREFERRED LNR IMPATT DEVICE DESIGN

Based upon imposition of the foregoing criteria to the previously presented IMPATT diode design alternatives, the preferred LNR GaAs IMPATT device design comprised the following features:

- . Based upon the availability of two independent outside sources of epitaxial GaAs material, epi-wafers grown to precise LNR specifications by both VPE and MBE were procured and processed into IMPATT chips.
- . SDR rather than DDR doping profiles were grown, based upon the comparative simplicity and lower development risk of the former, despite the potentially higher RF power output capability of the latter.
- . The modified Read (LHL) doping profile was selected rather than the simpler HL profile, due to the higher potential DC to RF conversion efficiency of the former, as well as the availability of a greater number of degrees of freedom in optimizing the LHL doping profile for realization of best performance.
- . The Schottky rather than grown (p-n) junction configuration was selected, as it not only permitted an additional iteration in remeasurement of the epitaxial layer doping profile but more significantly, permitted efficient fine grain optimization of the surface to high doping region distance. In-house processing avoided excessively time consuming and costly optimization during the epitaxial growth cycle. Once this distance has been established a p-layer could easily be grown in place of the Schottky barrier.
- . A circular cross section single mesa junction geometry was selected in preference to more complex multiple or distributed junction configurations despite the potential increase in RF power generation and decreases in thermal resistance with increasing junction area, thereby avoiding unusually low RF junction impedance levels and excessively complex and potentially unreliable device contacting requirements.



CARRIER DOPING DENSITY



DISTANCE

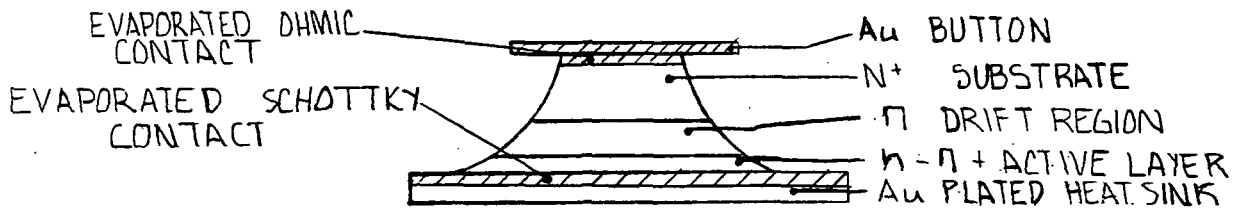
PREFERRED LHL PROFILE



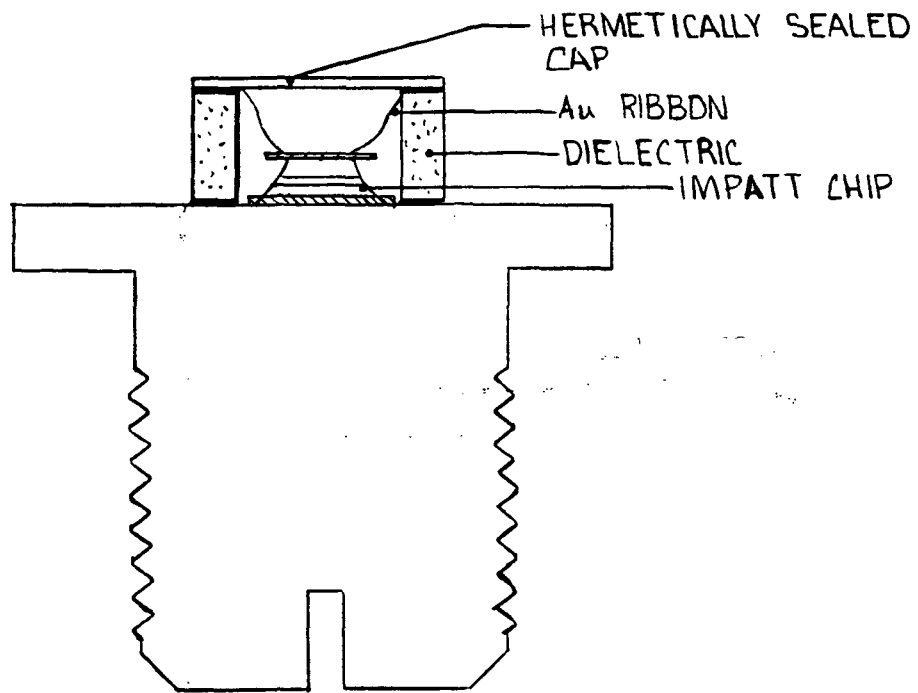
- . Gold plated (PHS) rather than diamond (DHS) heat sinking of the IMPATT chip was pursued as the primary approach (although preliminary DHS investigation was undertaken) due to its higher probability of success despite the 20 to 25 percent potential reduction in diode thermal resistance obtainable using DHS. The active or heat generating surface was bonded directly to the package stud.
- . Enclosed hermetically sealable rather than open structure packaging configuration was selected on the basis of its superior reliability and mechanical integrity for ultimate spacecraft deployments.
- . Single rather than multiple chip per package deployment was selected since, based upon preliminary experiments at LNR, the latter exhibited poor combinatorial efficiency and tended to introduce undesired modes of spurious oscillation which were not readily suppressed.

The foregoing considerations provided the basis of the preferred LNR GaAs IMPATT design, as described in the following paragraphs.





(A)



(B)

PREFERRED 20GHz GaAs IMPATT DEVICE CONFIGURATION



#### 2.4 CRITICAL STEPS IN GaAs IMPATT DIODE DEVELOPMENT & EVALUATION

The evaluation of a successful 20 GHz GaAs IMPATT diode design and implementation required the following series of critical and somewhat interactive steps:

- . design and specification of the preferred SDR LHL doping profiles for the proposed epitaxial GaAs material;
- . procurement and characterization of epitaxial GaAs wafers grown by reliable suppliers;
- . process development for ultra thin, stress free IMPATT chips;
- . assembly and characterization of packaged 20 GHz IMPATT devices.

The LNR approach to and results incurred during the performance of each of these steps in the successful 20 GHz IMPATT diode development process are described in the following paragraphs.



CRITICAL STEPS IN GaAs IMPATT DIODE  
DEVELOPMENT AND EVALUATION

1. EPITAXIAL MATERIAL DEVELOPMENT

- . Design and specification of suitable 20 GHz single drift modified Read doping profiles.
- . Identification and development of suitable outside suppliers with capability to grow specified epitaxial GaAs material.
- . Evaluation of epitaxial GaAs structure.
- . Iteration of doping profile design and epitaxial growth for optimum device characteristics.

2. IMPATT CHIP DEVELOPMENT AND IMPLEMENTATION

- . Wafer thinning and contact layer thickness optimization.
- . Surface preparation prior to forming the Schottky barrier metal structure.
- . Schottky and ohmic contact metallization.
- . Stress free chip formation.
- . Junction area etching.

3. IMPATT DIODE DEVELOPMENT AND IMPLEMENTATION

- . Implementation of void-free chip bonding techniques
- . Development of high temperature solder-and thermocompression bonding techniques
- . Development of optimum chip embedding/heat sinking configuration
- . Realization of hermetically sealable package having minimum parasitic circuit elements.

4. DEVELOPMENT OF REQUIRED CHARACTERIZATION CAPABILITY

- . Doping profile reconstruction as a function of C-V data.
- . Surface and profile characterization using SEM, ESCA, SAM EBIC.
- . Thermal resistance measurement.
- . RF characterization in suitable test oscillator structures.



## 2.5 DESIGN AND SPECIFICATION OF IMPATT DOPING PROFILE

In order to maximize the probability of success in the realization of the specified epitaxial GaAs which is within the reproducible growth capabilities of potential semiconductor material suppliers, a family of LHL doping profile designs have been generated. The realized growth "window" provides a range of values of the following critical LHL profile parameters for acceptable device performance:

- $X_P$  = active layer depth, e.g, location of highly doped (H) "spike" relative to Schottky contact interface
- $N_P$  = peak doping density of "spike"
- $\delta$  = width of "spike"
- $W_D$  = width of lightly-doped drift region
- $N_D$  = drift region doping density

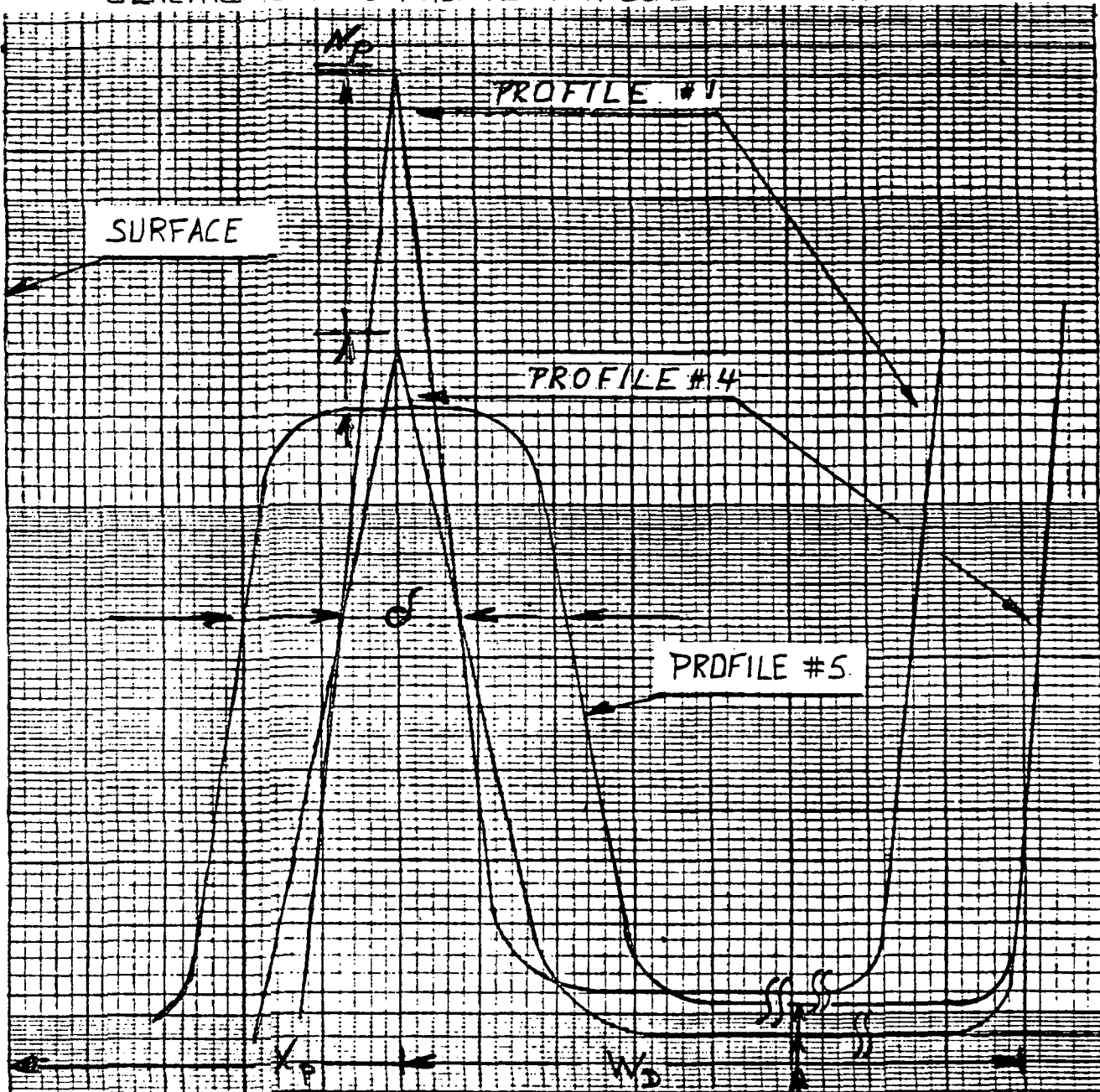
The tradeoff in potential RF performance with the degree of relaxation in specification of the foregoing critical L-H-L profile parameters relative to their optimum "modified Read" values, shows that considerable relaxation is possible without intolerable deterioration in predicted RF performance.

Accordingly, this family of LHL doping profile designs formed the basis for the specification and procurement of GaAs epiwafers as described in the following paragraphs.





# GENERIC DOPING PROFILES FOR GaAs LHL IMPATT



Projected Performance of 20 GHz Profile Design

| Profile No. | 1   | 2   | 3   | 4   | 5   |
|-------------|-----|-----|-----|-----|-----|
| $\eta$ (%)  | 26  | 24  | 22  | 20  | 18  |
| $P_0$ (W)   | 3.5 | 3.2 | 2.8 | 2.5 | 2.2 |

- $\eta = \frac{1}{\pi} \frac{V_D}{V_A + V_D}$  where  $V_A = \int E(x) dx$  (Avalanche Region)  
 $V_D = \int E(x) dx$  (Drift Region)
- $\int \alpha(x) dx = 1$ , where  $\int$  covers the entire depletion
- $P_0 = \frac{\eta}{1-\eta} \left( \frac{\Delta T_{max}}{\theta_{j-h}} \right)$  where  $\frac{\Delta T_{max}}{\theta_{j-h}}$  is assumed to be 10W



DISTANCE FROM REGION TO REGION (um)

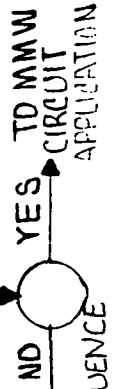
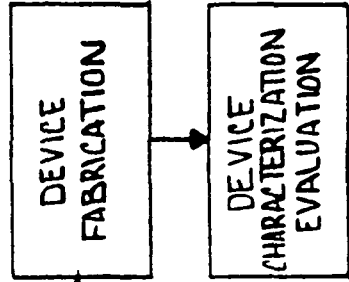
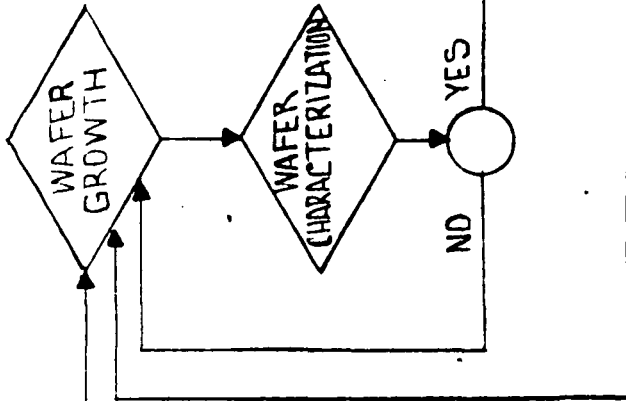
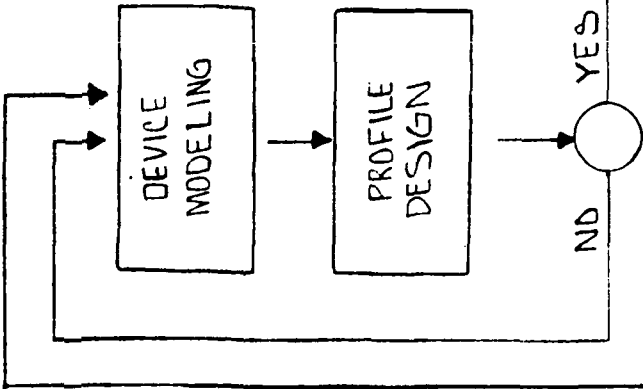
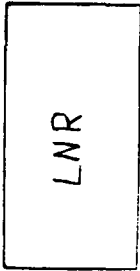
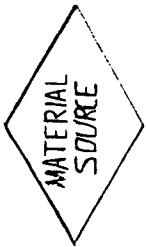
## 2.6 PROCUREMENT AND EVALUATION OF EPITAXIAL GaAs WAFERS

The success of the 20 GHz GaAs IMPATT diode development hinged upon the identification, development, and cultivation of one or more viable sources of epitaxial GaAs wafers grown to LNR specifications. A plan was evolved by LNR to govern an effective interactive collaboration process of doping profile design, epitaxial growth and material characterization. Subsequent device implementation and characterization followed by LNR and the material supplier wherein data feedback provided by LNR led to continual refinement of epiwafer growth.

Two separate industrial sources of state-of-the-art epitaxial GaAs were developed along the above lines, one utilizing VPE and the other, MBE systems. In addition, GaAs epiwafers supplied by several university and government agency sources were evaluated. Ultimately, the two industrial sources provided not only a supply of high quality GaAs epiwafers grown closely to LNR specifications, but also the basis of a comparison between similarly designed and processed IMPATT devices grown by these two competing technologies.



CODE



GENERAL GaAs IMPATT WAFER DESIGN GROWTH AND EVALUATION SEQUENCE

## 2.7 EPITAXIAL GaAs (LHL) DOPING PROFILE RECONSTRUCTION

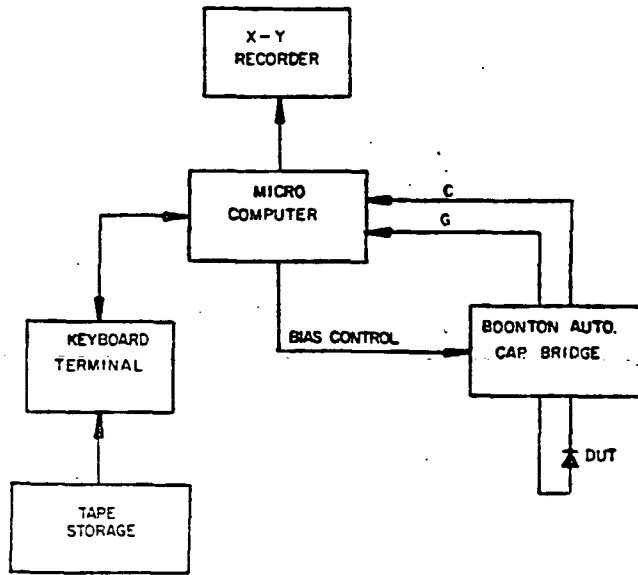
The accurate reconstruction of the GaAs epiwafer doping profile as a function of the distance from the surface of the active region is the most critical step in evaluating the grown layer structure with respect to potential IMPATT diode performance. Capacitance-voltage profiling is the technique used to characterize the grown single drift modified Read (LHL) IMPATT structure. The technique is based on the measurements of the capacitance as a function of negative applied voltage of a series of Schottky barrier diodes processed from said IMPATT wafers.

By measuring the depletion layer capacitance ( $C_{(V)}$ ) as a function of the applied reverse bias voltage ( $V$ ), the doping density ( $N$ ) can be derived as a function of the calculated distance from the surface, based upon accurate measurement of the junction area. For the complete profile reconstruction of multi-layer LHL IMPATT structure, it is necessary to step-etch wafer sections in discrete increments of active layer depth prior to forming the Schottky barrier interface. Specifically, accurately controlled step etching will move the surface on which the Schottky barrier structure is formed towards the highly doped spike and finally past the spike into the drift (Low) region.

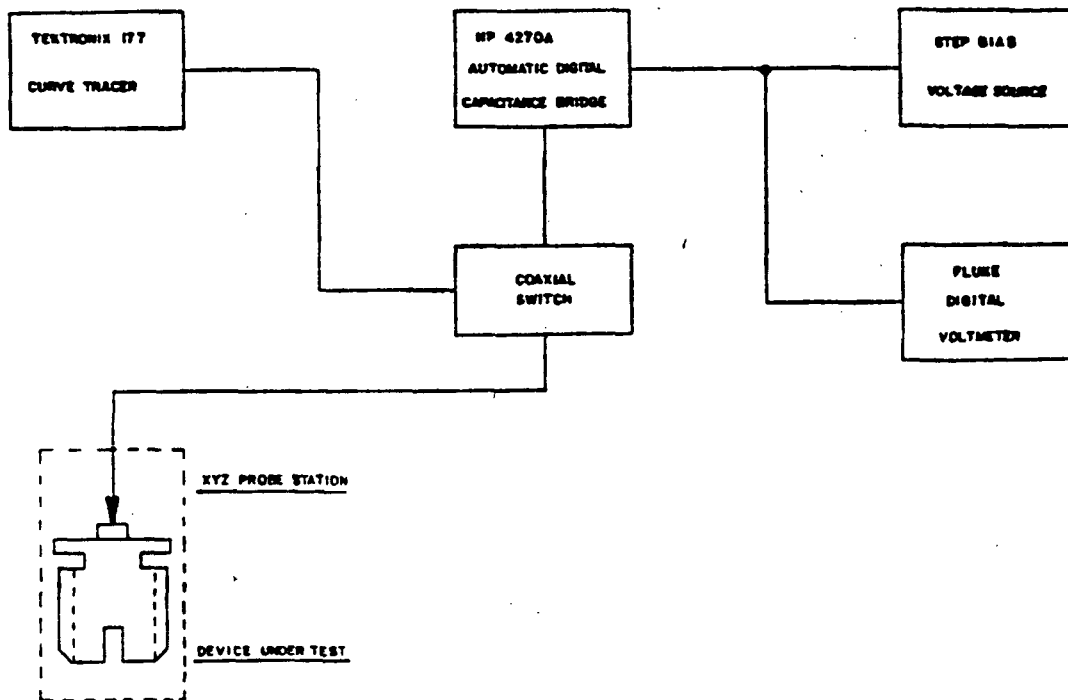
The Capacitance-voltage profiling has been performed using both manual and automatic measurement, with representative measured results from the latter as shown.



BLOCK DIAGRAMS OF C-V DATA ACQUISITION SYSTEMS



A) AUTOMATIC PROFILING BLOCK DIAGRAM



B) MANUAL PROFILING BLOCK DIAGRAM



For this purpose of verification of the doping profile of each GaAs epiwafer procured for ultimate IMPATT diode fabrication, as small section of the wafer is removed and used to fabricate a series of Schottky diodes, as described previously, per the depicted process flow chart.

For each of these Schottky diodes, corresponding to a different value of etched surface layer thickness, the data acquisition includes fine grain measurements of reverse bias capacitance versus applied voltage steps, photographic record of current-voltage (I-V) characteristic and carefully measured junction areas.

Measurements of the epitaxial wafer doping profile and the corresponding series of Schottky diode current-voltage characteristics provided the basis for an early prediction of potential IMPATT diode performance, which was verified during subsequent RF measurements on fabricated devices.

During the course of the development the following number of epitaxial GaAs wafers were characterized:

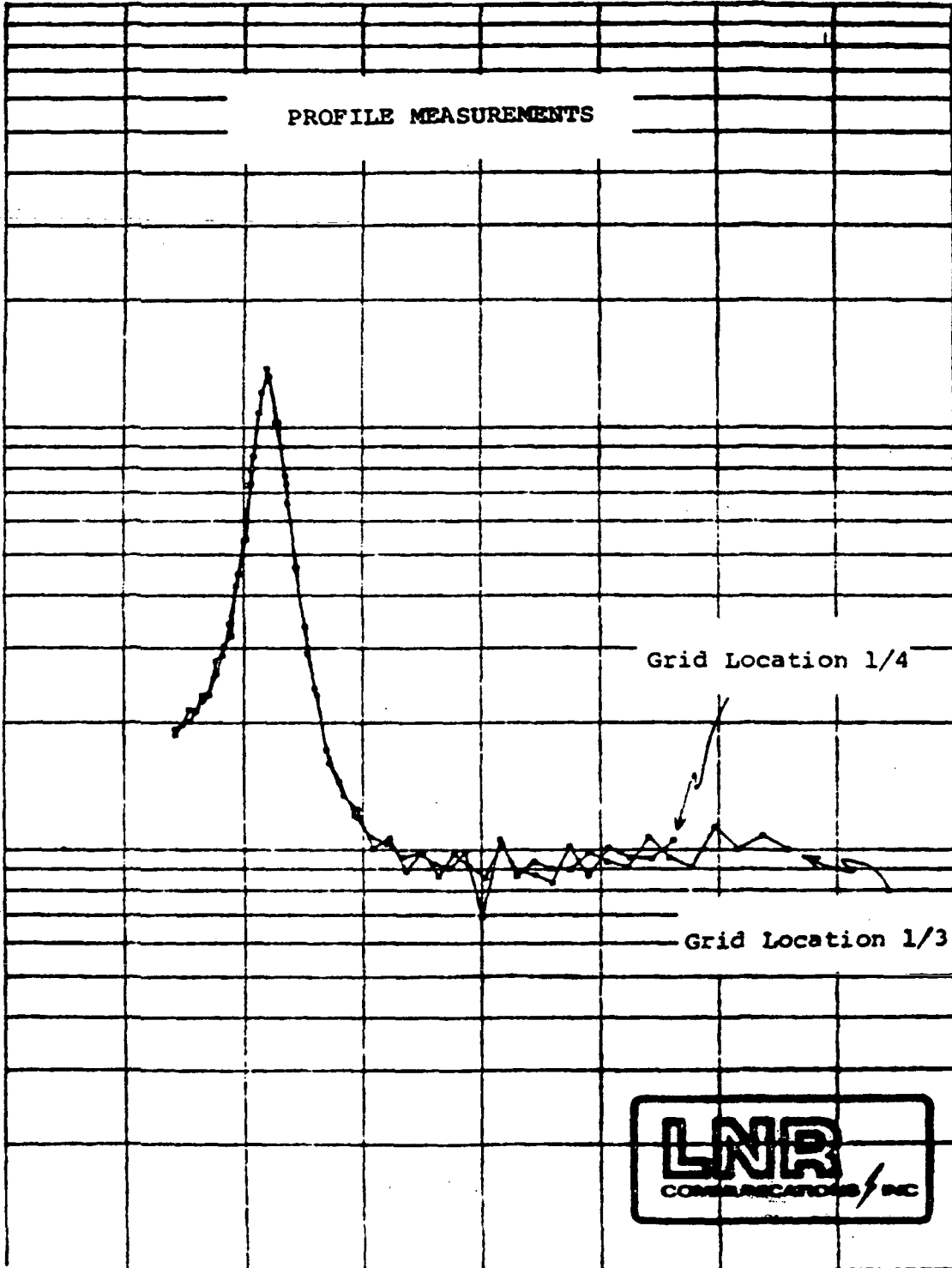
| <u>Growth System</u> | <u># of Wafers Characterized</u> | <u># of Wafers Meeting Requirements</u> |
|----------------------|----------------------------------|---|
| VPE                  | 35                               | 7                                       |
| MBE                  | 6                                | 3                                       |

Those of the foregoing wafers with measured doping profiles corresponding to the required level of potential 20 GHz IMPATT device performance, were used to process IMPATT chips as described in the following section.



RUN NUMBER 300-1B-1/3(ADD .4MICRON)

CARRIER CONCENTRATION, PER CC



DISTANCE FROM SURFACE, MICRONS  
TYPICAL MEASURED LHL DOPING PROFILE

## 2.8 IMPATT CHIP DEVELOPMENT AND IMPLEMENTATION

The optimum design of a III-V semiconductor (e.g. GaAs) IMPATT diode for maximum RF power output and DC-RF efficiency consistent with tolerable thermal resistance represents a trade-off between many competing factors. The key dimensional design parameters characterizing the physical GaAs IMPATT chip implementation include:

- . Chip thickness (N++ Substrate)
- . Effective mesa area
- . Mesa geometry
- . Ohmic and Schottky barrier metal structure
- . Void-free chip to package bond

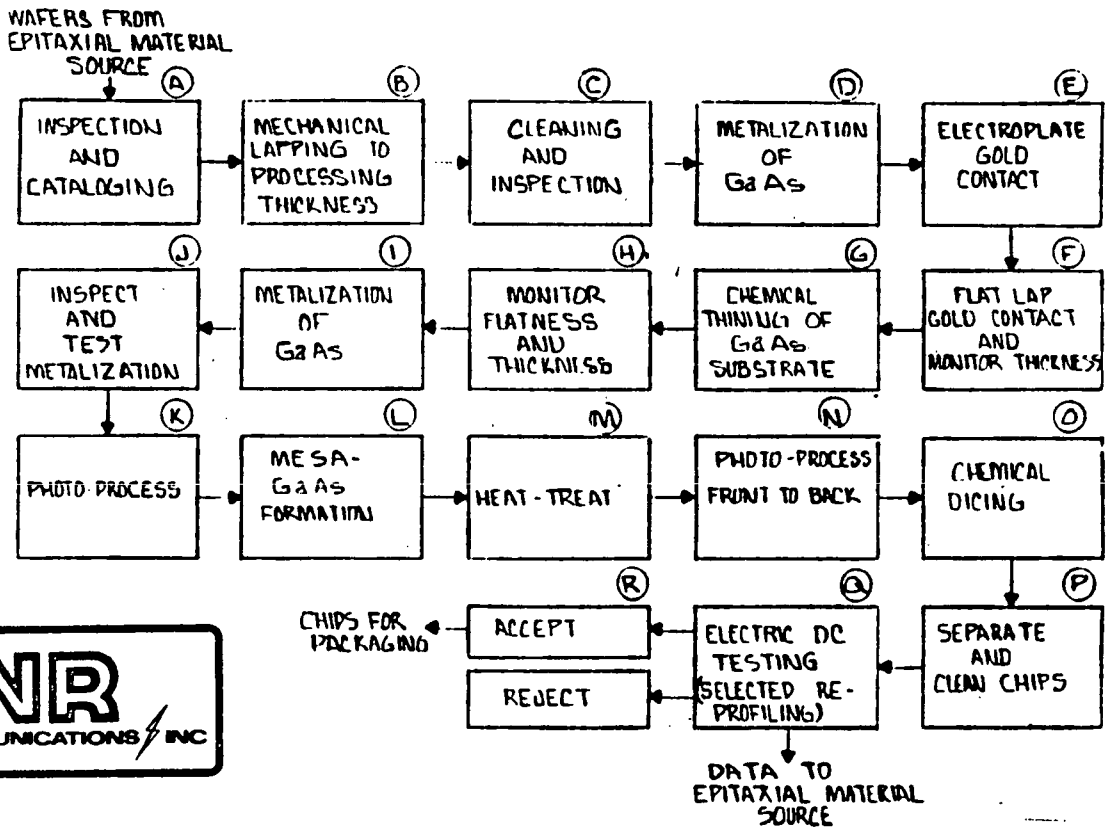
Accordingly, a GaAs material process was developed, which took the aforementioned criteria into consideration. The process flow shown enabled LNR to realize IMPATT chips with an average thickness of 10 to 12 microns and achieve stress-free chip separation. During the development phase a combined total of 3400 chips were produced for the purpose of providing a comprehensive material, process and device performance (DC and RF) evaluation.







A) SEM PHOTOGRAPH OF IMPATT DIODE MESA



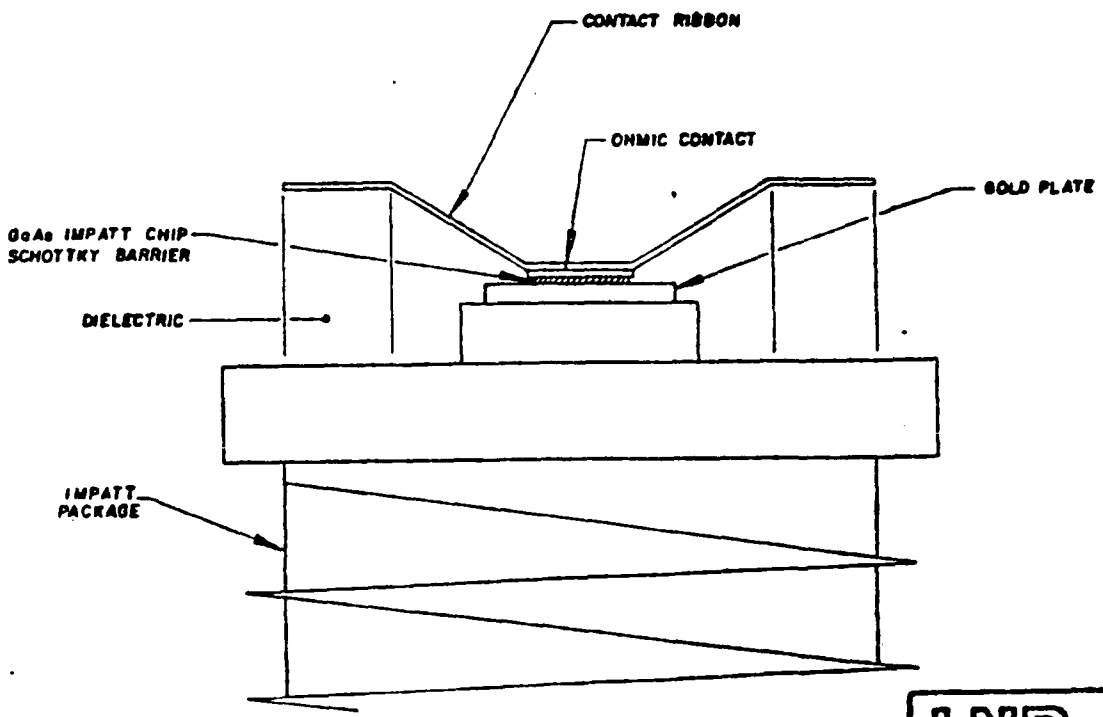
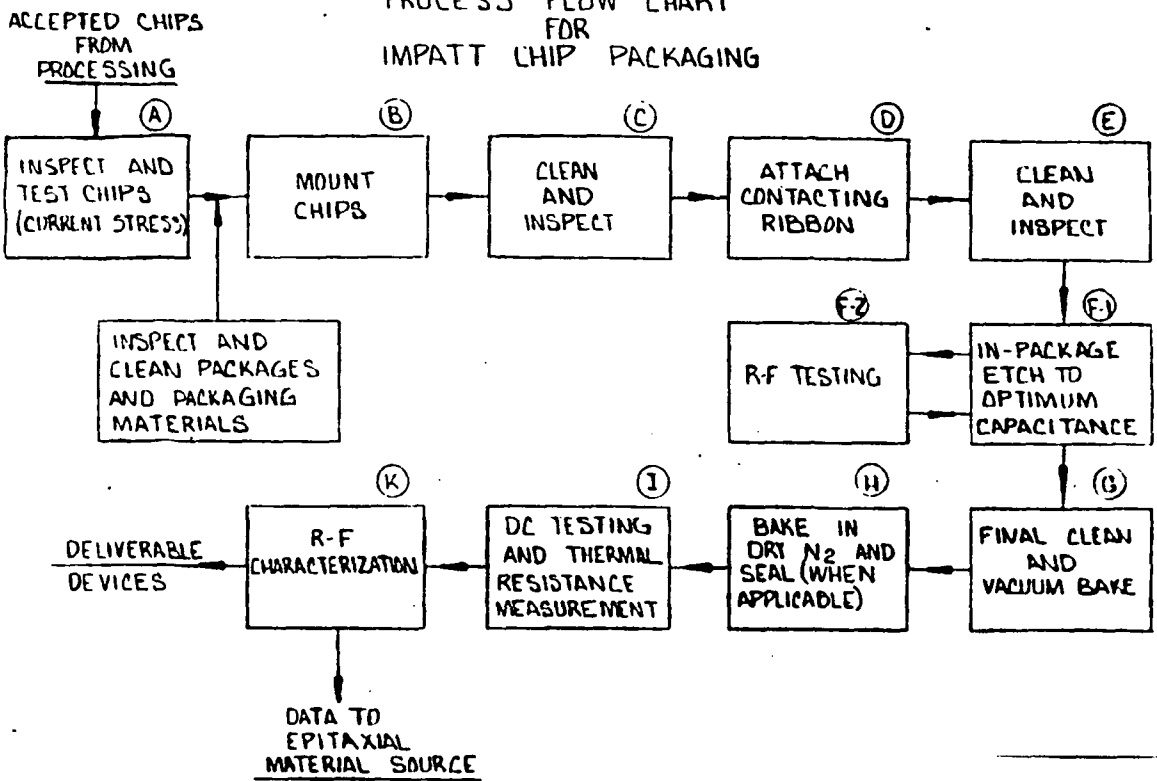
B) PROCESS FLOW CHART FOR IMPATT CHIPS

## 2.9 IMPATT DIODE PACKAGING

It is LNR's experience that the internal IMPATT diode thermal interfacial quality plays a very significant role in determining the total thermal resistance and consequently the operating junction temperature of the diode. Furthermore, it is also LNR's finding that device package parasitic inductance and capacitance have a considerable effect on performance. The packaging process developed encompassed both high temperature solder bonding and thermocompression bonding achieving excellent chip to package "foot prints" (e.g. void free interfaces). Over 500 packaged IMPATT diodes were fabricated for DC and RF evaluation.



# PROCESS FLOW CHART FOR IMPATT CHIP PACKAGING



SCALE 100:1



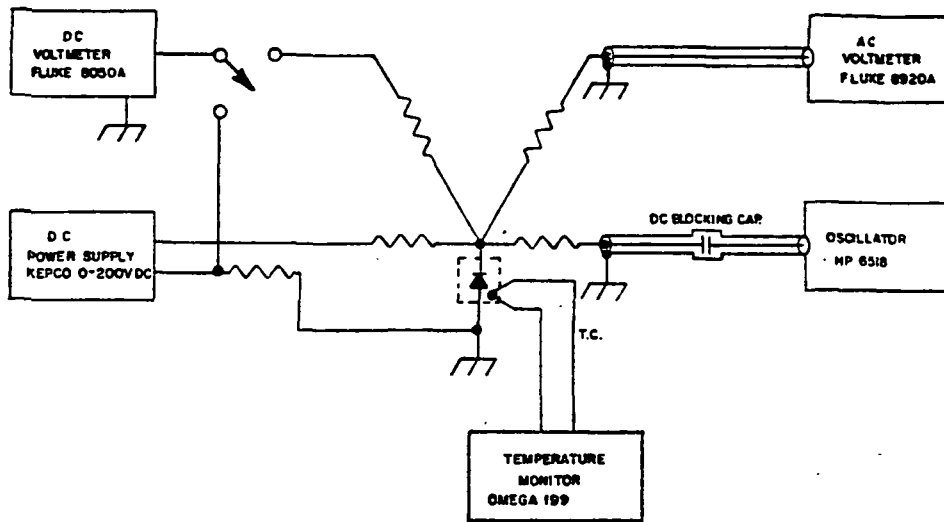
## 2.10 IMPATT DIODE CHARACTERIZATION

The evaluation of each of the IMPATT diodes fabricated as described previously included the measurement of:

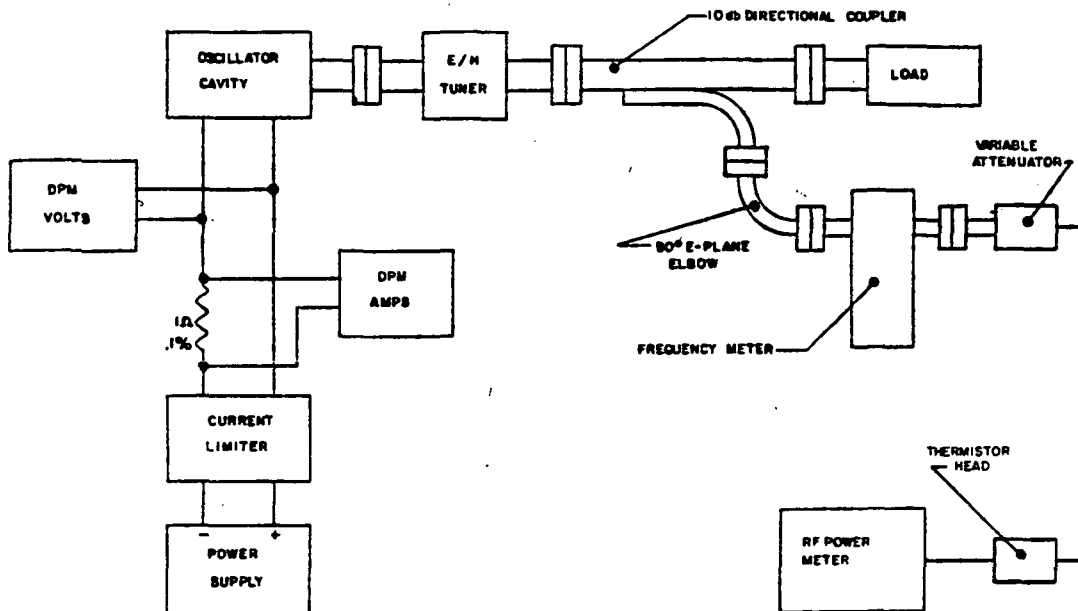
- . DC current-voltage (I-V) behavior, including the diode forward ( $V_F$ ) and reverse ( $V_B$ ) breakdown voltages, and the leakage current ( $I_L$  measured at 50% of the 10ua reverse breakdown voltage).
- . Capacitance-voltage (C-V) measurements taken at zero bias, minus 3 volts and near the reverse breakdown. In addition, two diodes of each metalization lot are used for profile reconstruction (as described previously) to identify potential processing related changes and barrier interface instabilities.
- . Thermal resistance ( $\theta_{th}$ ) to determine diode junction temperature and to identify problems associated with the chip and/or contacting ribbon bonds.
- . RF parameters, such as power output ( $P_O$ ), operating frequency, DC-RF conversion efficiency ( $\eta$ ) operating voltage and current.

The thermal resistance measurement configuration developed at LNR, utilizing a unique refinement of that due to Haitz\* eliminates all frequency-dependent components, except for one blocking capacitor, permitting small signal CW measurements as opposed to the usual pulse method. The measurements are made through a high series resistance, thus protecting the device under test. A major advantage of this measuring method is a highly flat frequency response up to 20 MHz as compared to an upper limit of only  $\sim 3$  MHz on the part of other related methods. Therefore, it is possible to measure thermal response times of  $\lesssim 50$  ns. The average thermal resistance achieved was  $24^\circ\text{C/W}$  without any specific emphasis on its optimization during the development phase.

\* R.H. Haitz, H.L. Stover and N.J. Tolar, IEEE Trans. Electron Devices ED-16, pg. 438 (1969)



A) THERMAL RESISTANCE MEASUREMENT CIRCUIT



B) BLOCK DIAGRAM OF OSCILLATOR MEASUREMENT SETUP FOR 20GHz IMPATTs



The RF measurements were conducted in a dedicated K-band waveguide oscillator test station, wherein variable tuning adjustments permitted centering of the distribution of oscillator frequencies in the vicinity of 20 GHz and simultaneous maximization of RF power output. The results of the above measurements ranging from 30 to 80 data points per diode were used extensively during the IMPATT diode development sequence, wherein observation was made of the impact on diode characteristics of fine grain iterations in such device design parameters as:

- . LHL doping profile "spike" doping level and location relative to contact interface.
- . LHL active layer depth and doping level.
- . Junction capacitance (as optimized by in-package etching).

Analysis of the fine grain measured results indicated that each of these parameters exhibited a "window" over which acceptable performance was achieved.

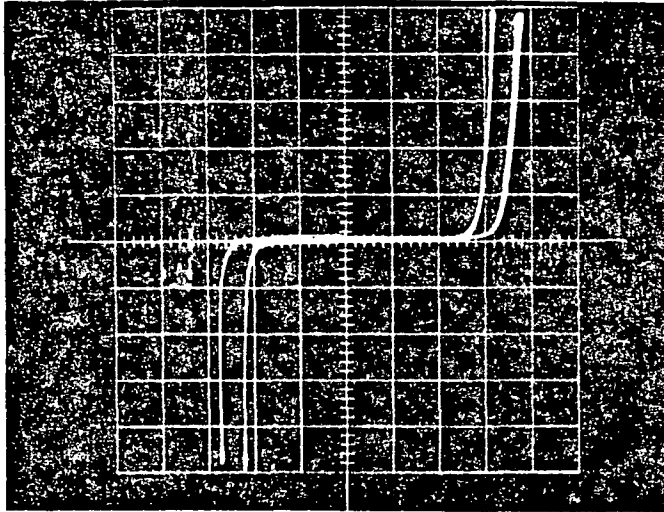
A combined total of more than 300 diodes were characterized. The distribution of RF oscillator power output and DC-RF efficiency for a quantity of 175 diodes operating in the 19-21 GHz frequency range indicates a range of 1.3 to 2.7W and 12 to 22 percent, respectively.



TYPICAL IMPATT DIODE CURRENT-VOLTAGE CHARACTERISTICS

G304-4

→  $V_F$  0.2V/Div.

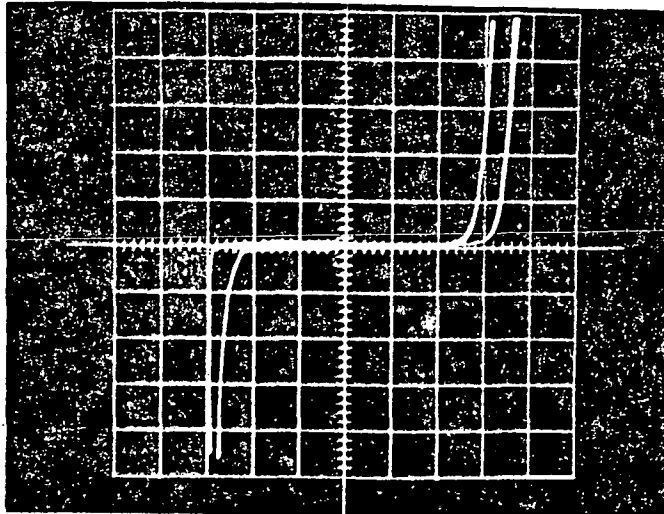


10 $\mu$ a and 1ma/Div.

$V_B$  5V/Div. ←

G301-2B

→  $V_F$  0.2V/Div.



10 $\mu$ a and 1ma/Div.

$V_B$  5V/Div. ←



## 2.11 20 GHZ IMPATT DIODE RF PERFORMANCE SUMMARY

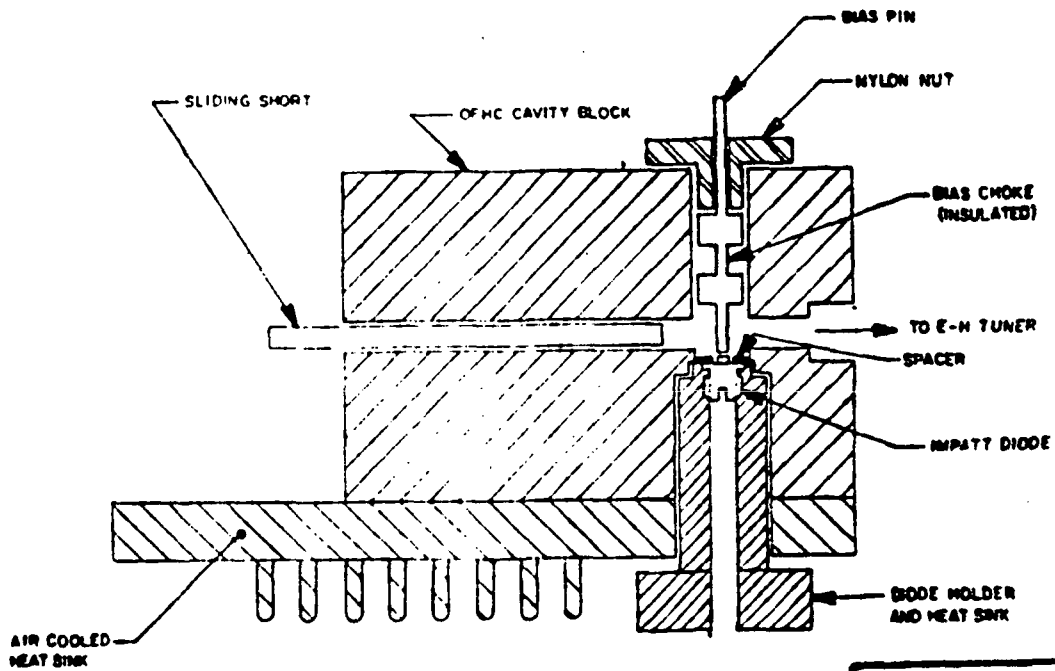
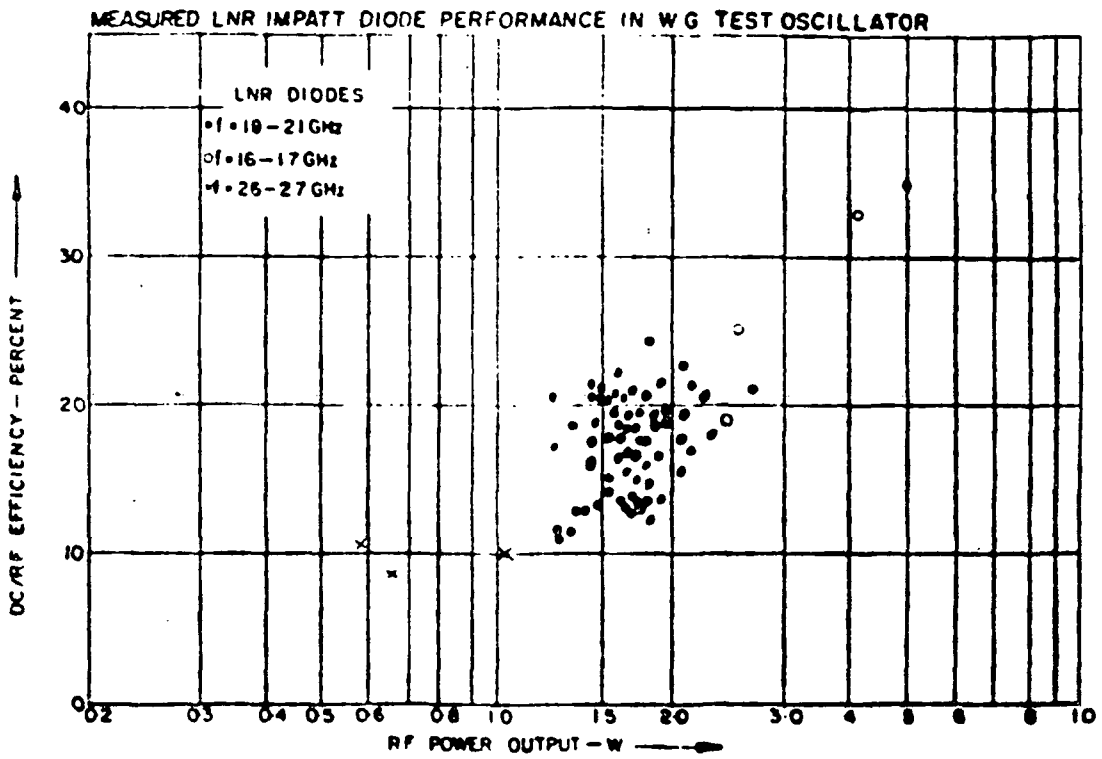
LNR achieved the following level of developmental ~20 GHz IMPATT diode performance, as measured in the aforementioned K-band waveguide test oscillator:

- . Frequency range 18-21 GHz
- . RF power output: 1.3 to 2.7W
- . DC-RF Conversion efficiency: 12 to 22 percent.

In addition, a direct correlation was established between amplifier and oscillator performance measurements, wherein IMPATT diodes which exhibited ~2W RF power output and 18 percent conversion efficiency at 20 GHz in the test oscillator, demonstrated ~2.5W RF power output, 4dB gain and 14 percent DC-RF power added efficiency over a 1 GHz bandwidth in a single stage 20 GHz test amplifier.





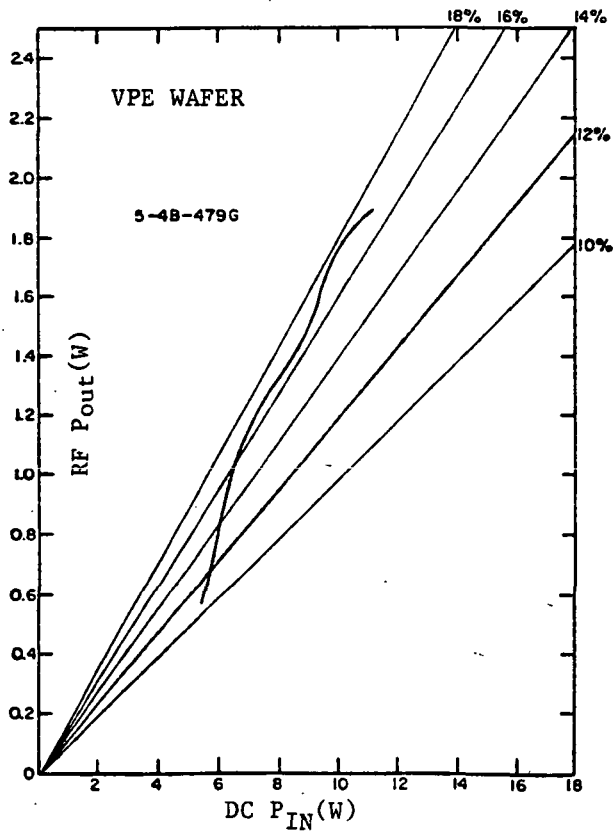
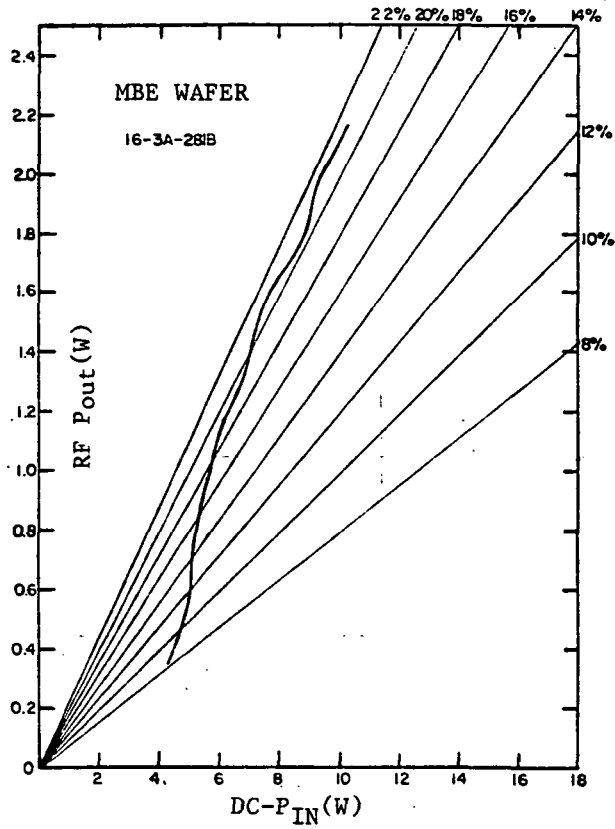


K-BAND IMPATT TEST OSCILLATOR

## 2.12 MBE vs VPE Performance

A byproduct of the 20 GHz IMPATT diode developed was a comparison of the RF performance of GaAs IMPATT diodes fabricated from MBE or VPE material as grown to precise LNR specifications by two separate epiwafer suppliers. Since this comparison was not itself the main thrust of the development effort, the available data is not a conclusive comparison of (epitaxial growth) technology but also includes the result of random sampling variations between different epitaxial GaAs wafers. In general, the results obtained with LNR IMPATT diodes processed from both types of epitaxial wafers are seen to be comparable, both on an individual and statistical (histogram) basis. However, the MBE technique for wafer growth, has, based upon wafer/diode yield data accumulated during this development effort, established itself as being more uniform and repeatable, and, consequently, capable of achieving specified state of the art doping profiles with a minimum of iterations.





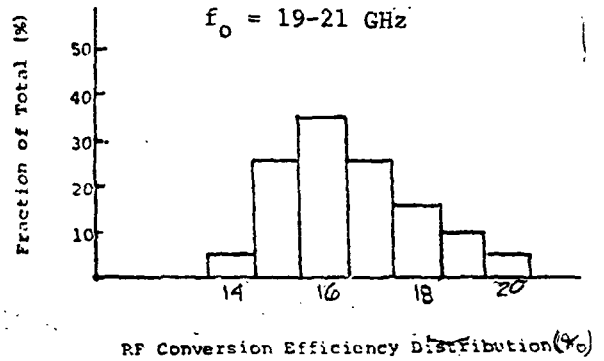
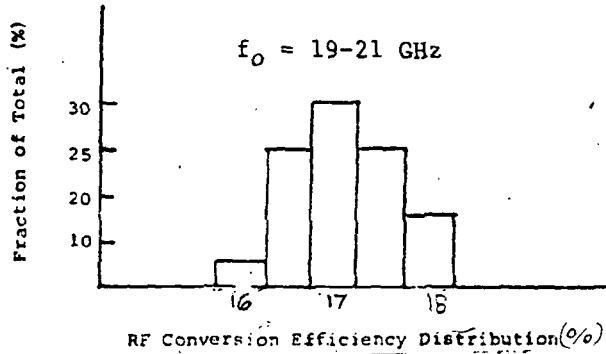
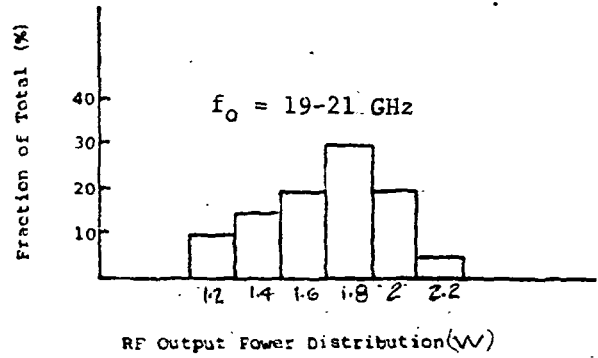
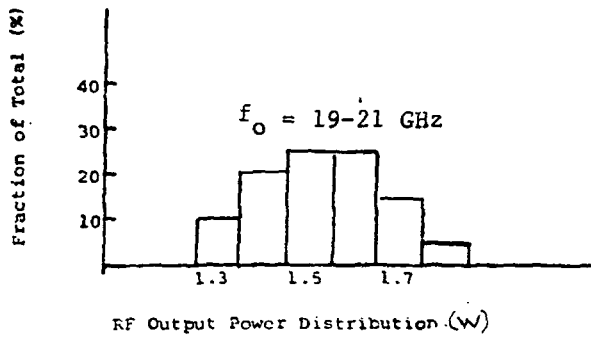
TYPICAL MEASURED RF OUTPUT/DC INPUT POWER  
PROFILES OF 20 GHz GaAs IMPATT DIODES



### 2.13 DISTRIBUTION OF RESULTS

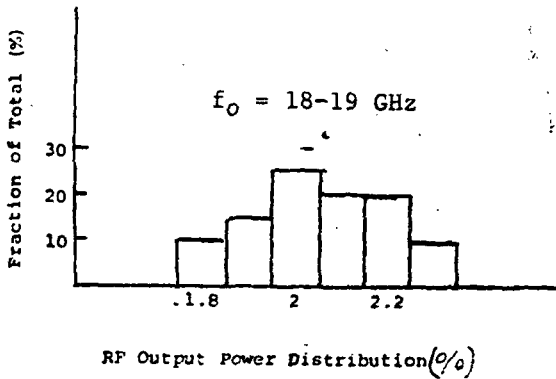
The distributions of measured IMPATT diode test oscillator RF power output, efficiency and frequency data vary as widely between wafers grown by a particular technique as between those grown by MBE versus VPE. In reality substantial performance variations are also evident from processing lot to processing lot as the result of deliberately introduced process iterations. However, as seen in histogrammic data summaries, a large fraction of the characterized diodes meet the basic RF performance objectives. Introduction of tighter specifications however, in order to achieve higher levels of RF performance reduces the yield factor, thereby introducing a cost versus performance tradeoff.



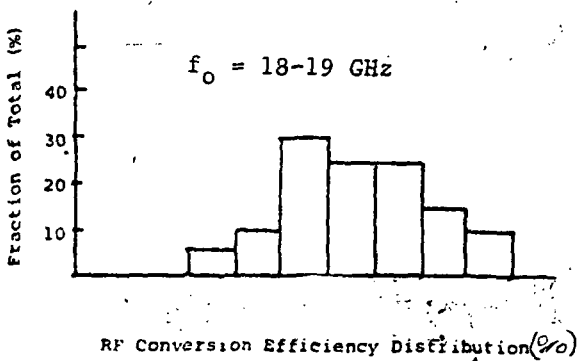
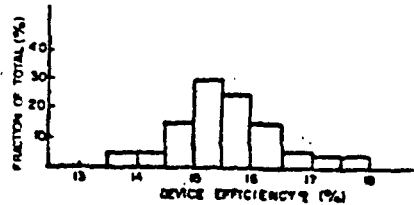
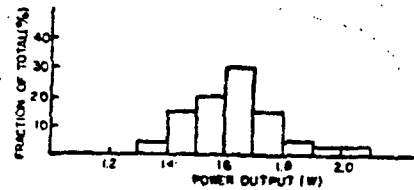


A-VPE WAFER #5

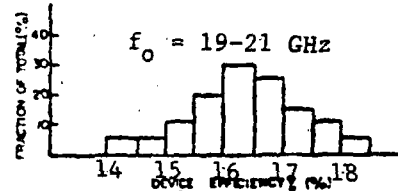
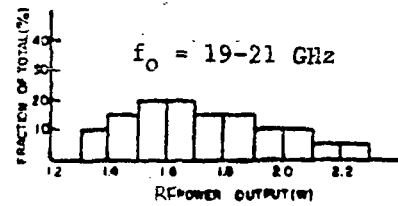
B-VPE WAFER #35



D-VPE WAFER



E-MBE WAFER



C-MBE WAFER #16

HISTOGRAMS OF MEASURED RF PERFORMANCE OF 20GHz GaAs IMPATT DIODES PROCESSED FROM TYPICAL EPI WAFERS

3.0 20 GHz RF ASSEMBLY DESIGN/DEVELOPMENT



### 3.1 BREADBOARD 20 GHz CIRCUITS DEVELOPED FOR TRANSMIT AMPLIFIER DESIGN VALIDATION

In addition to the major development effort on 20 GHz IMPATT devices described in the preceding section, the following 20 GHz functional circuits comprising key elements in the preferred transmitter design were implemented and evaluated in breadboard form to validate said design, with results as enumerated below:

#### 1. Single-stage IMPATT Test Amplifier

- . Construction: composite TEM transmission line
- . Frequency range: 19.5-20.5 GHz
- . RF power output: 2.5-2.8W
- . Operating gain: 4.0-4.5 dB
- . Operating bandwidth: 1 GHz (min)
- . DC-RF power added efficiency: 14 percent

#### 2. Four and six-port (two and four junction) circulators:

- . Construction: stripline
- . Frequency range: 19-21 GHz
- . Insertion loss/pass: 0.25 dB (max)
- . External port return loss: 20-27 dB (typ)
- . Interjunction isolation: 20-30 dB (typ)

#### 3. Integrated two-stage IMPATT driver amplifier

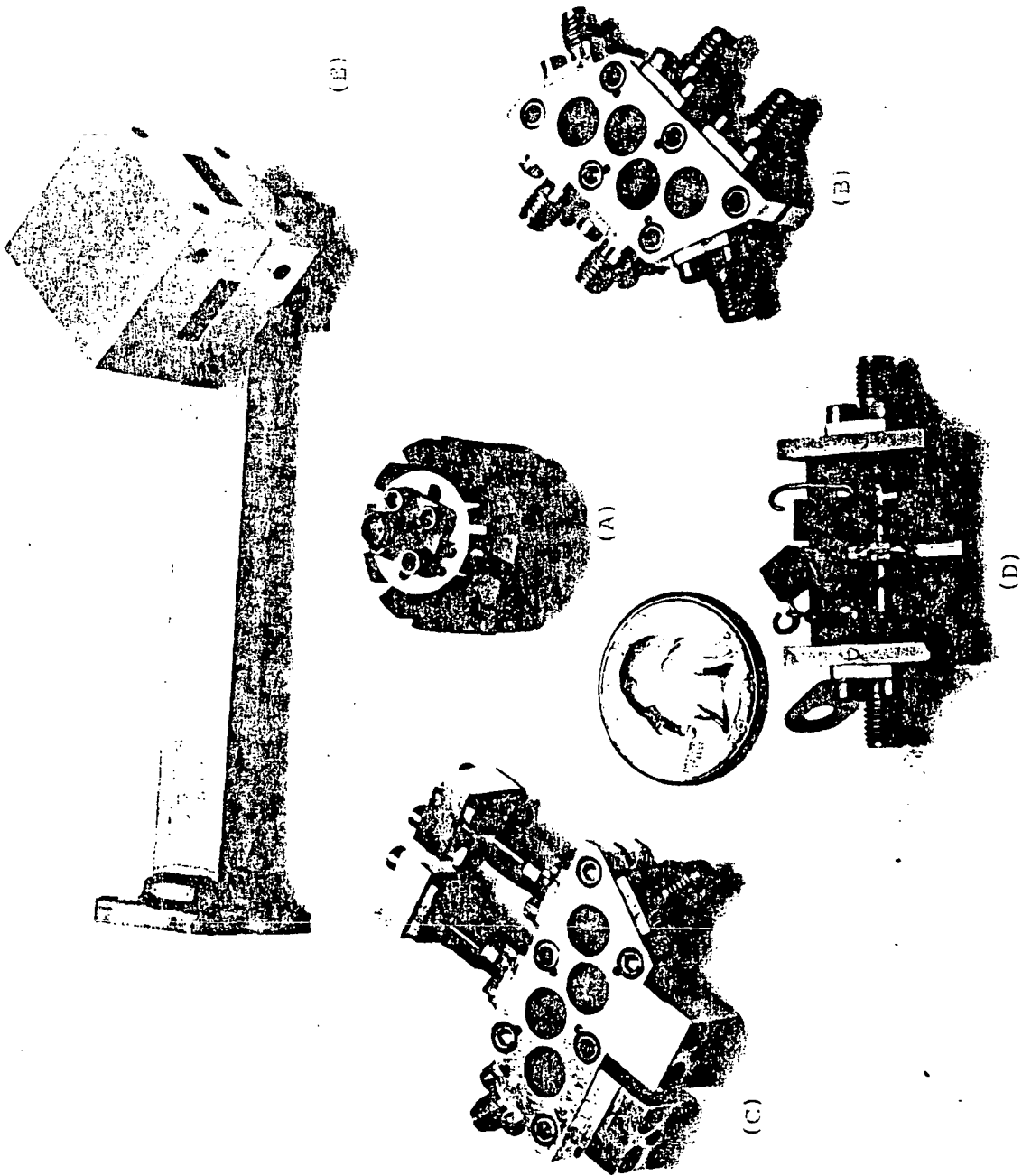
- . Construction: composite stripline/TEM
- . Frequency range: 19.5-20.5 GHz
- . RF power output: 2.5W (nom)
- . Operating gain: 7.0 dB (nom)
- . Efficiency: 12.5 percent

#### 4. FET amplifier stage

- . Construction: Duroid-based microstrip
- . Frequency range: 19.7-20.7 GHz
- . Small signal gain: 5.5 +1 dB
- . RF power out @ 1 dB compression: 45 mW
- . DC power drain: 0.3W

#### 5. Four-way power combiner

- . Construction: waveguide reactive junction
- . Frequency range: 19.5-20.5 GHz
- . Residual insertion loss: 0.2 dB (max)
- . Output port VSWR: 1.1:1 (max)



BREADBOARD 20 GHZ CIRCUITS DEVELOPED FOR IMPATT TRANSMITTER  
 DESIGN VALIDATION  
 (A) IMPATT AMPLIFIER TEST MOUNT (B) FOUR-JUNCTION (6 PORT) CIRCULATOR  
 (C) TWO-STAGE INTEGRATED IMPATT AMPLIFIER (D) FET AMPLIFIER STAGE





### 3.2 20 GHz IMPATT TEST MOUNT AND TEST AMPLIFIER STAGE

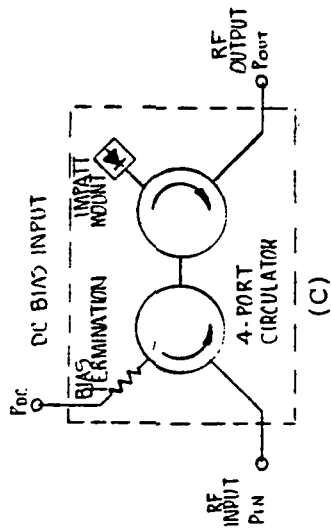
A one port coaxial IMPATT diode test mount was implemented not only as a vehicle for LNR IMPATT diode evaluation but also, when coupled to a 20 GHz four port TEM-line circulator, as a means toward evolving and demonstrating a baseline 20 GHz IMPATT "building block" amplifier stage design. The coaxial mount design was selected over its waveguide counterpart on the basis of its lower-parasitic reactance diode mounting geometry, and its wider band immunity against out of band oscillations. Accordingly, the test mount itself, incorporating an end-mounted IMPATT diode embedding geometry (for lowest diode parasitics and best heat sinking) and in-line capacitive tuning element and cascaded line transformation network, was used to accommodate small signal network analyzer IMPATT diode negative impedance measurements. When extrapolated, these measurements provided a useful large signal design characterization of the IMPATT diode as well as a means toward selecting the optimum tuning and transformation elements.

The single stage test amplifier formed by connecting this IMPATT diode mount to the output junction of a dual junction (4-port) breadboard 20 GHz TEM circulator (the resistively match-terminated input junction comprises an input isolator), demonstrates wideband high power operation of LNR IMPATT diodes developed under this device/assembly task. Typical IMPATT diode performance obtained in this 20 GHz test amplifier operated in the constant voltage mode included 2.5W RF power output, 4 dB operating gain and 14 percent DC-RF power-added efficiency over a 1.5 GHz bandwidth at a nominal 1W RF input drive level, all of which is consistent with the 2W, 18 percent RF power/efficiency performance exhibited by the same diode in a 20 GHz waveguide test oscillator.

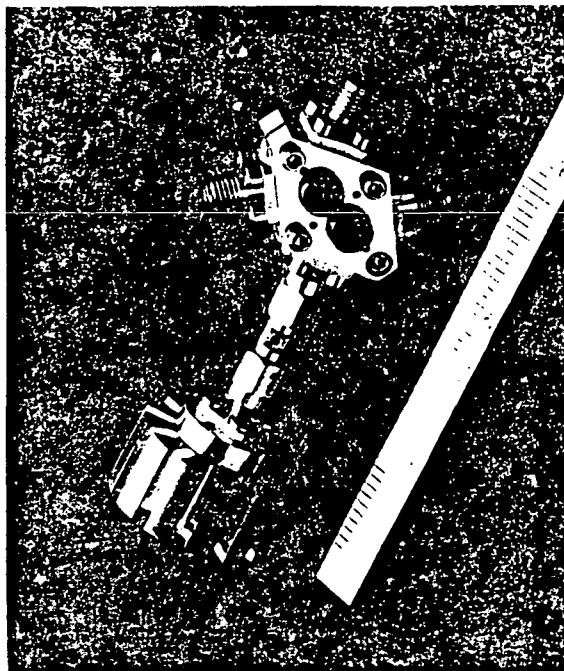




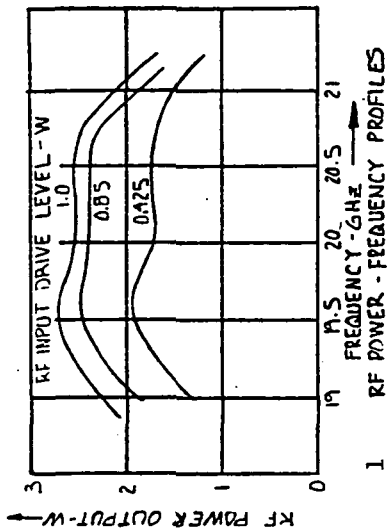
(A)



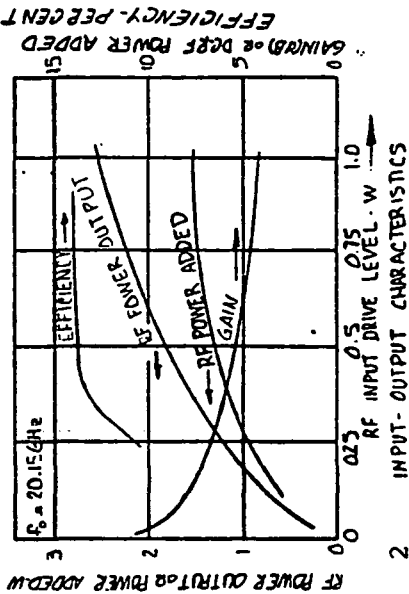
(C)



(B)



1 RF POWER - FREQUENCY PROFILES



2 INPUT-OUTPUT CHARACTERISTICS

(D)

20 GHz IMPATT TEST MOUNT AND TEST AMPLIFIER STAGE  
 (A) COAXIAL TEST MOUNT (B) CIRCULATOR-COUPLED IMPATT MOUNT (20 GHz TEST AMPLIFIER STAGE) (C) BLOCK DIAGRAM OF TEST AMPLIFIER STAGE (D) MEASURED PERFORMANCE OF TEST AMPLIFIER STAGE



### 3.3 20 GHz MULTIJUNCTION CIRCULATORS

Both two and four junction (four-and- six port) circulators were developed at 20 GHz for use as the coupling mechanisms for single stage IMPATT "test amplifier and an integrated two stage IMPATT "amplifier respectively, wherein the unused junctions are resistively match terminated for use as input and/or interstage isolators. The preferred dielectrically loaded stripline circulator configuration, though at the threshold of the state-of-the-art at 20 GHz, was selected over its more conventional (at this frequency) waveguide counterpart due to its:

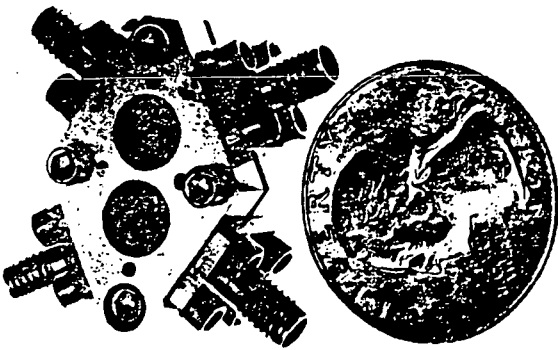
- . Significantly smaller size and lighter weight (by factor of 4:1), of particular importance since five such six-ports are utilized in the preferred transmitter design.
- . Considerably wider bandwidth capability, which is of great importance in presenting the IMPATT diode with a wideband well-matched terminating impedance over wide "guard-bands" on either side of the specified passband so as to maintain out of band stability.

Accordingly, both the four and six-port implementations exhibited the following typical level of performance at 20 GHz.

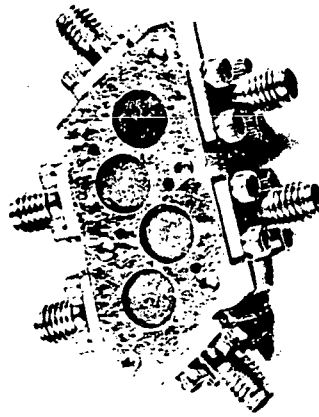
- . less than 0.25 dB/pass insertion loss over 19-21 GHz
- . greater than 25 and 20 dB external port isolation/return loss over 19.5-20.5 GHz and 19-21.5 GHz, respectively
- . greater than 24 and 20 dB interjunction isolation over 19.5-20.5 and 19-23 GHz, respectively

Relatively high power, DC insulating microwave absorbing loads were utilized at each of the internally terminated circulator ports, providing RF isolated DC bias entry networks for each of the associated IMPATT amplifier stages.





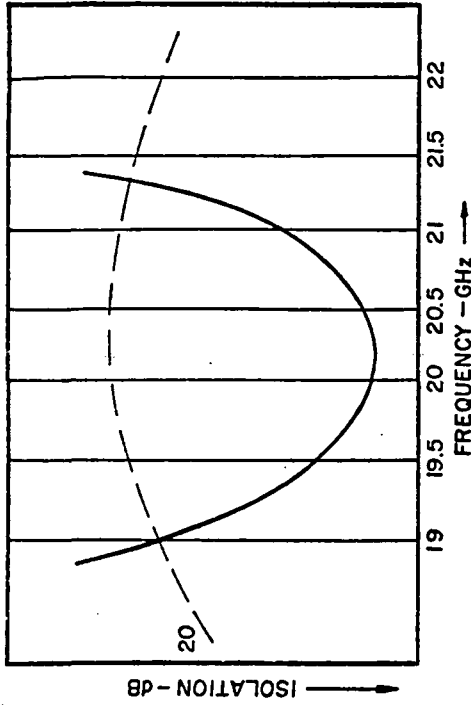
(A)



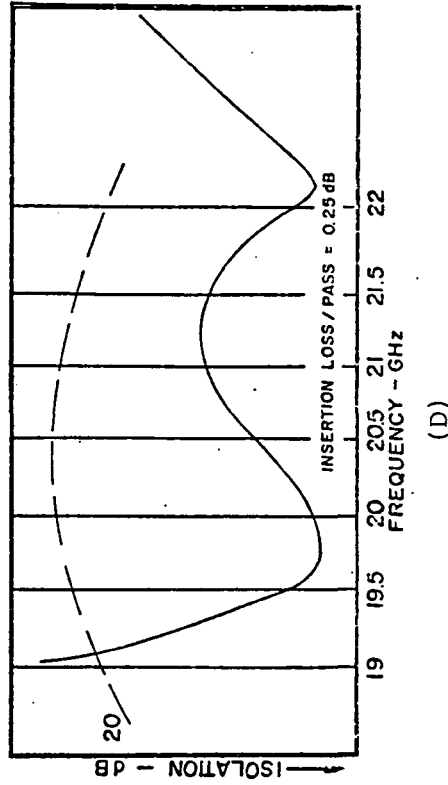
(B)

20 GHz MULTI-JUNCTION CIRCULATOR IMPLEMENTATIONS

(A) TWO JUNCTION (FOUR-PORT) CIRCULATOR, (B) FOUR JUNCTION (SIX PORT) CIRCULATOR  
 (C) MEASURED EXTERNAL PORT ISOLATION/RETURN LOSS (TYP), (D) MEASURED INTERJUNCTION ISOLATION (TYP)



TYPICAL EXTERNAL PORT ISOLATION OF BREADBOARD K-BAND 6-PORT CIRCULATOR (C)



(D)

### 3.4 INTEGRATED, TWO-STAGE 20 GHz IMPATT AMPLIFIER

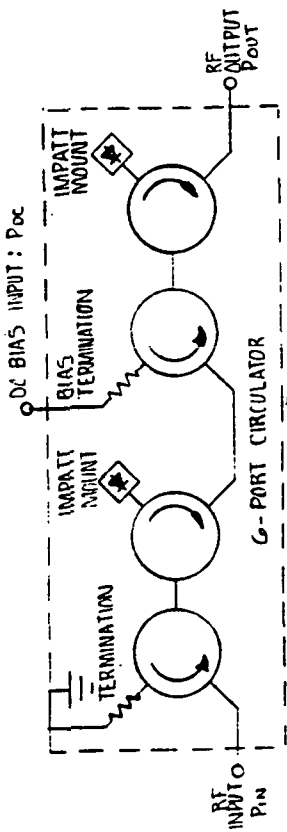
The design baseline achieved in the previously described 20 GHz IMPATT test amplifier stage was extended to the implementation of a completely integrated two stage, 20 GHz IMPATT amplifier. Constructed in a composite coaxial/stripline transmission medium, with the in-line IMPATT mounts connected to the second and fourth junction of the six port circulator, this amplifier is typically mounted diode-side down to the baseplate for best diode heat sinking. In the preferred 20 GHz transmitter design approach, this two stage amplifier may be utilized as the power section preamplifier or, if suitably modified to accommodate two 2W IMPATT diodes in the output stage, as each of the four power section combinatorial "building blocks".

Typical measured performance of this two stage, 20 GHz integrated IMPATT amplifier, over the 19.5-20.5 GHz frequency range, utilizing 1.5 to 2W GaAs IMPATT diodes operated in the constant voltage mode, includes:

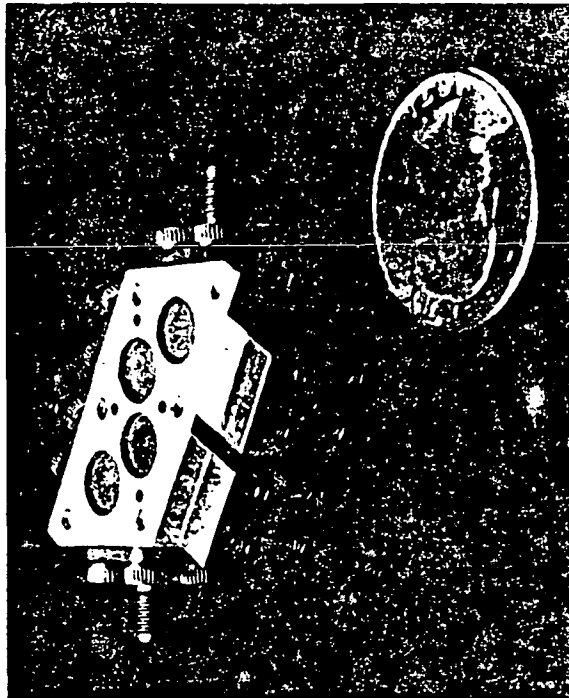
- . maximum useful RF power output of 2.5W at 7.0 dB overall gain and DC-RF efficiency of 12.5 percent at a 0.50W input drive level.
- . maximum DC-RF power added efficiency of 12.7 percent at 2W RF output power; 13 dB gain and 0.1W input drive level
- . higher gain smaller signal operation exemplified by 1.25W RF output power at 17 dB gain and 25 mW input drive level

This level of performance is useful as the 20 GHz transmitter power section preamplifier and extrapolates to 5W RF output for a dual diode output stage as required for the power section "building blocks".

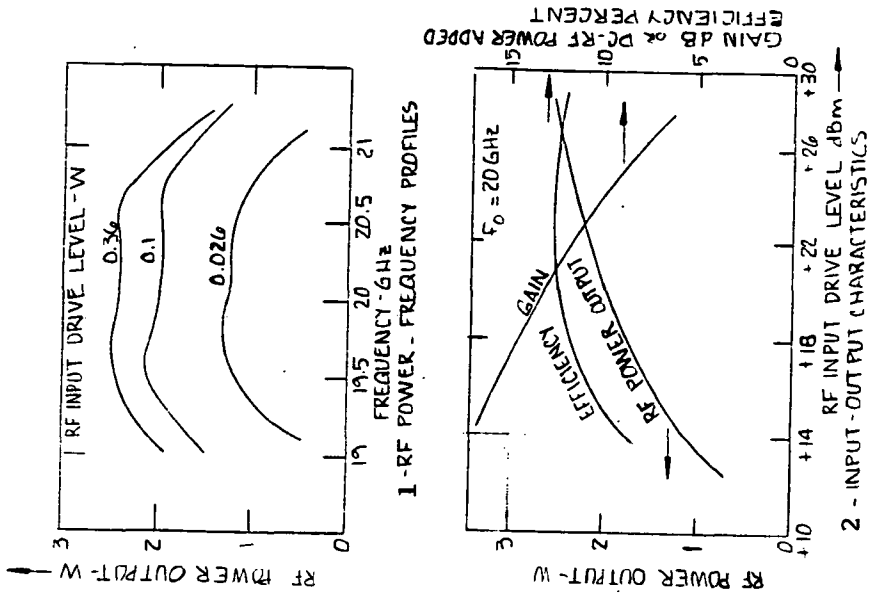




A - BLOCK DIAGRAM



B - PHOTOGRAPH



C - MEASURED PERFORMANCE

INTEGRATED, TWO-STAGE, 20 GHz IMPATT AMPLIFIER  
 A-BLOCK DIAGRAM, B-PHOTOGRAPH, C-MEASURED PERFORMANCE



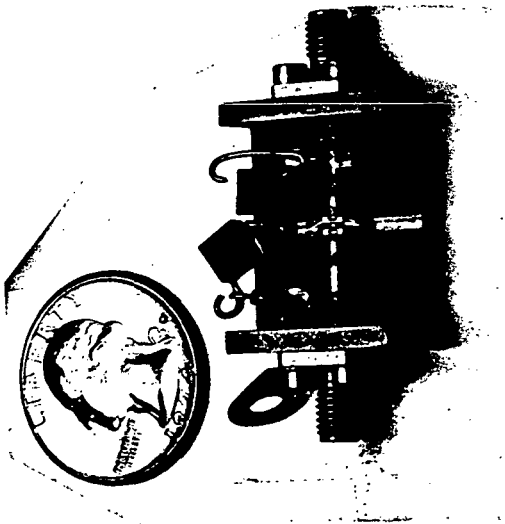
### 3.5 SINGLE-STAGE 20 GHz FET TEST AMPLIFIER

To demonstrate the validity of the use of a two-stage 10 dB gain FET driver section amplifier in the preferred 20 GHz transmitter design, a single stage 20 GHz FET test amplifier was implemented in duriod based microstrip transmission line. Utilizing a commercially available (DXL 3504A) 20 GHz FET chip, mounted on a customized LNR carrier which incorporated self contained gate input and drain output matching elements, this breadboard test amplifier exhibited:

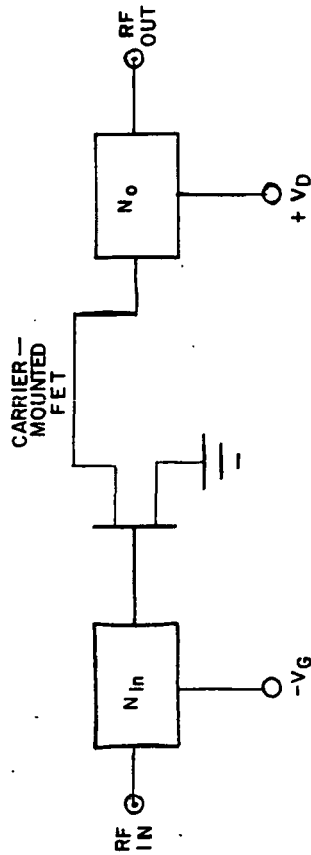
- . 5.5  $\pm$ 1.0 dB monotonic small signal gain over the 19.7-20.7 GHz frequency range.
- . +16.4 dBm (45 mW) RF output level at 1 dB gain compression
- . 10 percent DC-RF power added efficiency at the 1 dB compression point

Combining the above with a second FET amplifier stage utilizing currently available higher level (0.1 to 0.25W) 20 GHz FET's can be shown, based upon extrapolation of the above data, to yield a two-stage FET driver with the desired 10 dB operating gain and 0.1W RF output at 1 dB gain compression.

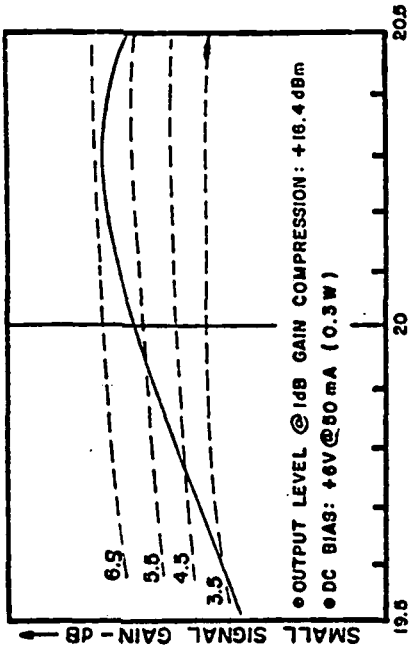




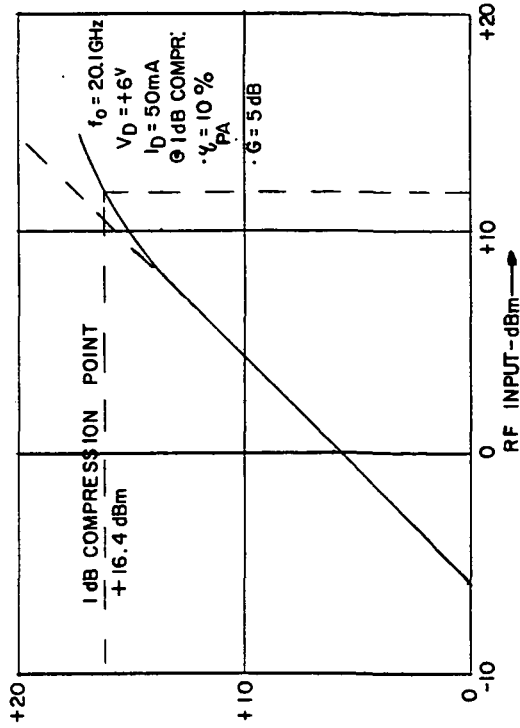
A - PHOTOGRAPH



B - BLOCK DIAGRAM



C - MEASURED - FREQUENCY RESPONSE



D - MEASURED - INPUT-OUTPUT CHARACTERISTIC

SINGLE-STAGE 20GHz FET TEST AMPLIFIER





### 3.6 20 GHz FOUR-WAY POWER DIVIDER/COMBINER

In the preferred 20 GHz transmitter design, the use of circulator-coupled IMPATT "building block" amplifiers in the four-way combinatorial power section postamplifier permits the utilization of a reactive (non-isolated) four-way power divider and power combiner, since the terminated ports of the input and interstage isolator in each "building block" provide external port-to-port isolation for the divider and combiner. Therefore, for minimum residual insertion loss and maximum compatibility with the combinatorial postamplifier topology, a four way waveguide reactive junction divider/combiner configuration was selected, and developed.

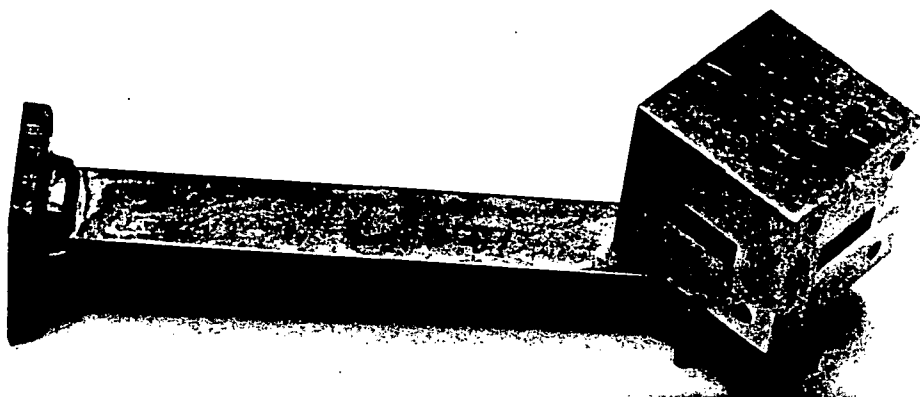
The breadboard implementation of the resulting 20 GHz four-way reactive waveguide junction divider/combiner design, representable by a symmetrical 5 x 5 scattering matrix, exhibited the following measured performance over the 19.5-20.5 GHz range:

- . Residual insertion loss:  $< 0.2$  dB (max) (combining efficiency  $> 96$  percent)
- . Common port VSWR: 1.1:1 (max)

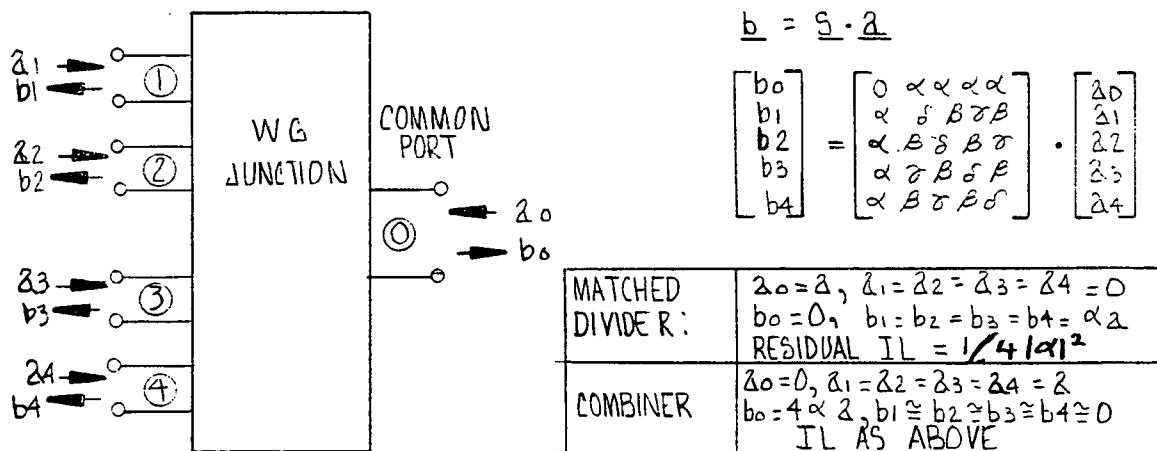
In fact, the useful bandwidth of this divider/combiner was about 2 GHz.

Based upon the above measured results, the validity of the reactive waveguide junction divider/combiner design approach was amply demonstrated and seen to yield the state of the art in 20 GHz combinatorial technology.

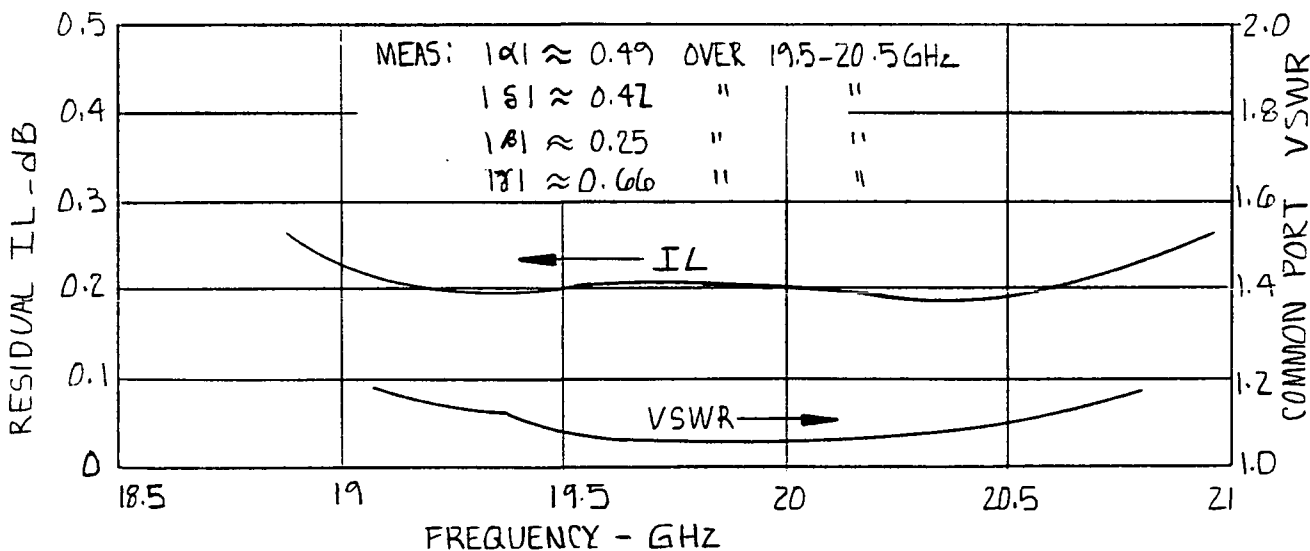




A - PHOTOGRAPH



B - BLOCK DIAGRAM / CIRCUIT MODEL



C - MEASURED PERFORMANCE

20GHz, FOUR-WAY POWER DIVIDER/COMBINER



4.0 SUMMARY AND CONCLUSIONS



#### 4.0 SUMMARY AND CONCLUSIONS

This report has summarized the accomplishments of the Device/Assembly Technology Development task wherein the key state of the art technology items requisite to the development and implementation of a POC model 20 GHz IMPATT transmitter were developed and demonstrated.

The 20 GHz POC model 20W IMPATT transmitter paper design generated on this program is configured around a two stage FET driver and an IMPATT power section. The latter, in turn, consists of a two stage, circulator coupled 2W IMPATT preamplifier cascaded with a four way combinatorial postamplifier. This IMPATT post-amplifier is formed by four identical two-stage, circulator-coupled 6W IMPATT "building block" amplifiers paralleled between identical four way reactive power divider and combiner, wherein each "building block" output stage utilizes two 2-2.5W IMPATT diodes in a dual diode mount.

The primary accomplishments of the task include the development, implementation and breadboard evaluation of:

- . 20 GHz single drift GaAs Schottky LHL Read-profile IMPATT diodes in hermetically sealed packages, which, in developmental quantities, exhibited 1.5-2.7W RF output power and 12-22 percent DC-RF power added efficiency when evaluated in K-band test oscillator. Typical diode performance in single-stage 20 GHz test amplifier includes 2.5W to 2.8W RF power output, 4 dB gain and 14 percent DC-RF power added efficiency, over a greater than 1 GHz instantaneous bandwidth;
- . critical constituent building blocks of POC IMPATT transmitter design, including 6 port circulator, two stage IMPATT amplifier, FET amplifier stage and four way reactive power divider/combiner.

The measured results of the aforementioned development effort serve to validate the POC IMPATT transmitter design.



## SUMMARY OF DEVICE/ASSEMBLY DEVELOPMENT RESULTS

1. 20 GHz GaAs Read-IMPATT Diodes:
  - . Construction: Stud-mounted, encapsulated
  - . RF power output: 1.3-2.7W
  - . Efficiency: 12-22 percent
2. Single-stage IMPATT Test Amplifier
  - . Construction: composite TEM transmission line
  - . Frequency range: 19.5-20.5 GHz
  - . RF power output: 2.5-2.8W
  - . Operating gain: 4.0-4.5 dB
  - . Operating bandwidth: 1 GHz
  - . DC-RF power added efficiency: 14 percent
3. Six-port (four junction) circulator:
  - . Construction: stripline
  - . Frequency range: 19-21 GHz
  - . Insertion loss/pass: 0.25 dB (max)
  - . External port return loss: 20-27 dB
  - . Interjunction isolation: 20-30 dB
4. Integrated two-stage IMPATT driver amplifier
  - . Construction: composite stripline/TEM
  - . Frequency range: 19.5-20.5 GHz
  - . RF power output: 2.5W (nom)
  - . Operating gain: 7.0 dB (nom)
  - . Efficiency: 12.5 percent
5. FET amplifier stage
  - . Construction: Duroid-based microstrip
  - . Frequency range: 19.7-20.7 GHz
  - . Small signal gain: 5.5  $\pm$ 1 dB
  - . RF power out @ 1 dB compression: 45 mW
  - . DC power drain: 0.3W
6. Four-way power combiner
  - . Construction: waveguide reactive junction
  - . Frequency range: 19.5-20.5 GHz
  - . Residual insertion loss: 0.2 dB (max)
  - . Output port VSWR: 1.1:1



E. POC MODEL DESIGN, TEST PLAN  
AND PROCEDURES

FINAL REPORT

NASA CR 174716

Prepared For:

NASA Lewis Research Center  
Cleveland, Ohio

CONTRACT NASA-NAS3-22491

LOGNORMAL MODEL FOR DC ACCELERATED STRESS TEST DATA  
 HIGH TEMPERATURE ( $T_H = 345^{\circ}\text{C}$ )  
 20 GHZ SCHOTTKY-BARRIER IMPATT DIODE



VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

SS=SUM OF SQUARES

$$= \sum X_I^2 - \frac{(\sum X_I)^2}{N}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK

N = NUMBER OF DEVICES

$$N = 20$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2734$$

AT 90% CONFIDENCE,  $N = 20$ :

$$D^*_{\text{MIN}} = 0.2657 \quad D^*_{\text{MAX}} = 0.2857$$

$$D^*_{\text{MIN}} \leq D_{\text{DATA}} \leq D^*_{\text{MAX}}$$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS VALID.

\*ZAR, J.H. 1974 BIOSTATISTICAL ANALYSIS.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.

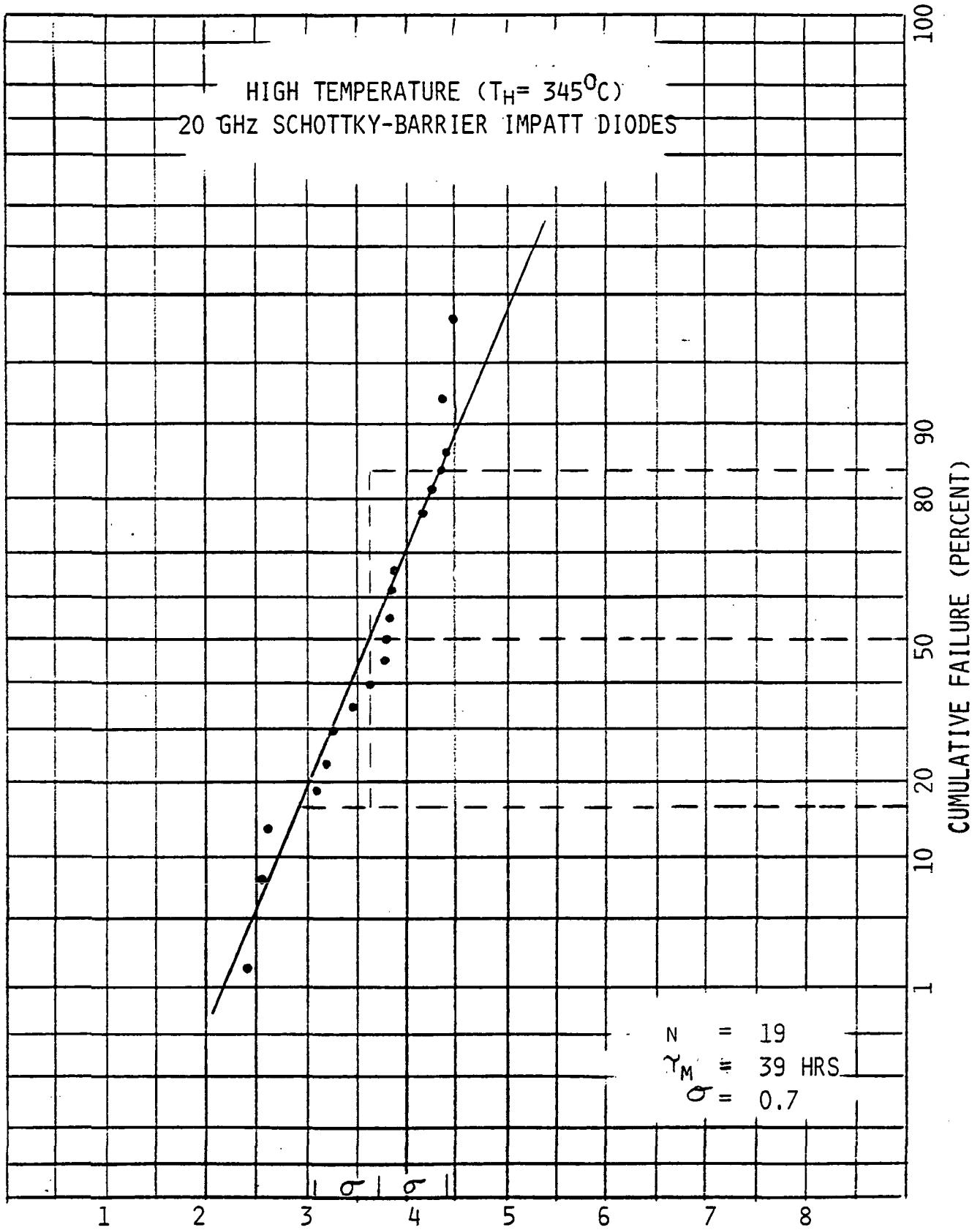


FIGURE 27.

$X = \text{LN (TIME TO FAILURE-HRS)}$   
(61)



DC ACCELERATED TEST DATA FOR  
HIGH TEMPERATURE ( $T_H = 345^{\circ}\text{C}$ )  
20 GHz SCHOTTKY-BARRIER IMPATT DIODES



| DEVICE S/N | $T_I$ (HRS.) | $X_I = LNT_I$ | CUMULATIVE<br>% FAILURES = $\frac{2^{X_I} - 1}{2^N} \times 100\%$ |
|------------|--------------|---------------|---|
| 1229G      | 11.1         | 2.407         | 2.6   |
| 1116B      | 12.8         | 2.549         | 7.9   |
| 680G       | 13.6         | 2.610         | 13.2  |
| 668G       | 22.25        | 3.102         | 18.4  |
| 362D       | 24.5         | 3.199         | 23.7  |
| 366D       | 25.8         | 3.250         | 28.9  |
| 685G       | 32.8         | 3.490         | 34.2  |
| 1231G      | 38.5         | 3.651         | 39.5  |
| 514G       | 44.8         | 3.802         | 44.7  |
| 1188G      | 45.6         | 3.820         | 50  |
| 1106B      | 46.1         | 3.831         | 55.3  |
| 1180G      | 48.8         | 3.888         | 60.5  |
| 470G       | 48.8         | 3.888         | 65.8  |
| 1223G      | 55.6         | 4.018         | 71.1  |
| 1220G      | 65.8         | 4.187         | 76.3  |
| 1254M      | 70.7         | 4.258         | 81.6  |
| 1237G      | 80.2         | 4.385         | 86.8  |
| 1264M      | 80.7         | 4.391         | 92.1  |
| 1177G      | 147.8        | 4.996         | 97.4  |

N=19

LOGNORMAL MODEL FOR DC ACCELERATED STRESS TEST DATA  
 HIGH TEMPERATURE ( $T_H = 345^{\circ}\text{C}$ )  
 20 GHZ SCHOTTKY-BARRIER IMPATT DIODE



VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

$$\begin{aligned} SS &= \text{SUM OF SQUARES} \\ &= \sum X_I^2 - \frac{(\sum X_I)^2}{N} \end{aligned}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK

N = NUMBER OF DEVICES

$$N = 19$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2793$$

AT 90% CONFIDENCE,  $N = 19$ :

$$D^*_{\text{MIN}} = 0.2646 \quad D^*_{\text{MAX}} = 0.2855$$

$$D^*_{\text{MIN}} \leq D_{\text{DATA}} \leq D^*_{\text{MAX}}$$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS VALID.

\*ZAR, J.H. 1974 BIostatistical Analysis.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.

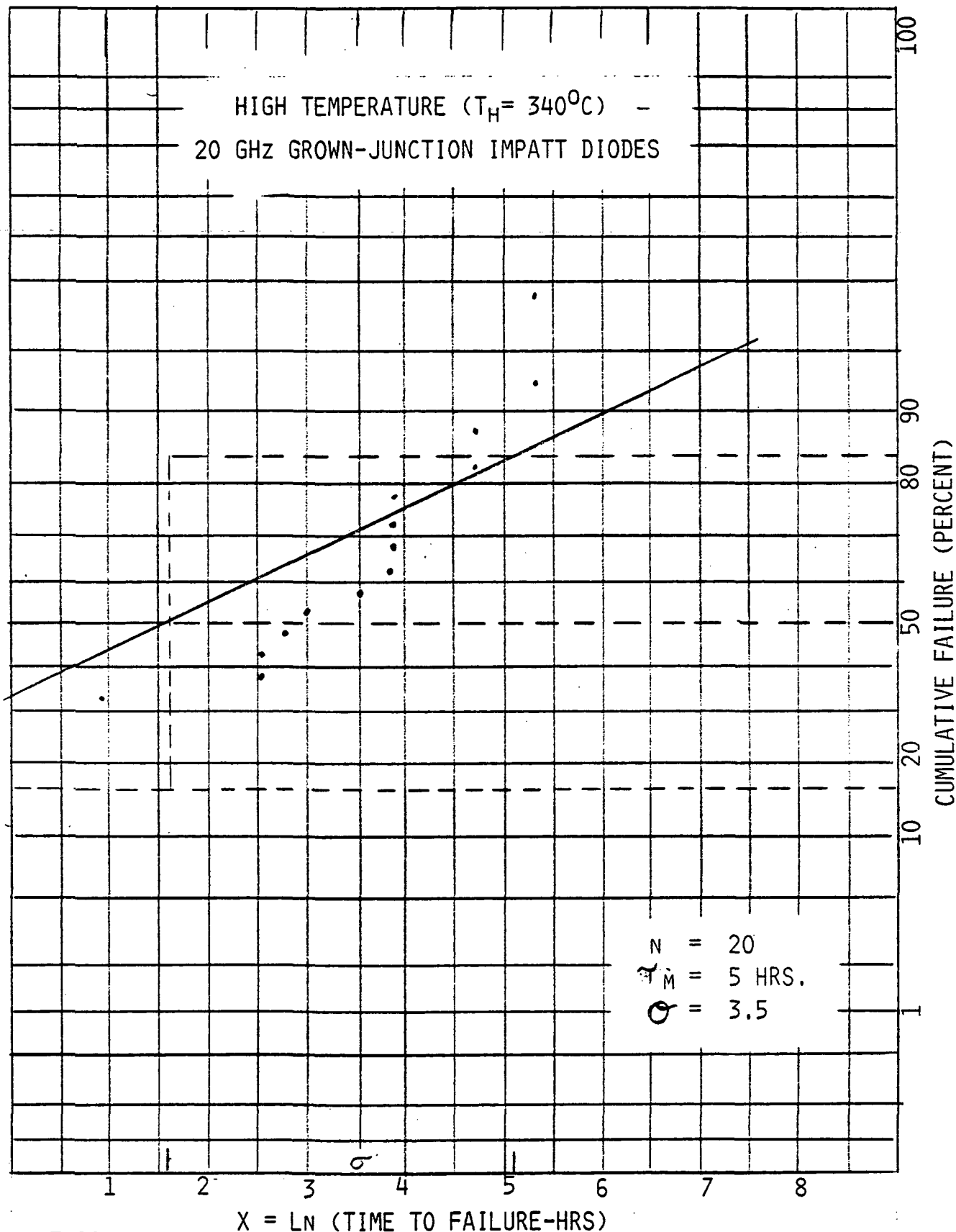


FIGURE 30.

DC ACCELERATED STRESS TEST DATA FOR  
HIGH TEMPERATURE ( $T_H=340^{\circ}\text{C}$ )  
20 GHz GROWN-JUNCTION IMPATT DIODES



| DEVICE S/N | $T_I$ (HRS.) | $X_I=LNT_I$            | CUMULATIVE<br>% FAILURES = $\frac{2I-1}{2N} \times 100\%$ |
|------------|--------------|------------------------|---|
| 19         | 0            | $\rightarrow - \infty$ | 2.5   |
| 35         | 0            | $\rightarrow - \infty$ | 7.5   |
| 36         | 0            | $\rightarrow - \infty$ | 12.5  |
| 8          | 0            | $\rightarrow - \infty$ | 17.5  |
| 31         | 0.5          | -.69315                | 22.5  |
| 37         | 1.0          | 0.0                    | 27.5  |
| 17         | 2.5          | .91629                 | 32.5  |
| 33         | 12.8         | 2.54945                | 37.5  |
| 1          | 12.9         | 2.55723                | 42.5  |
| 32         | 16.05        | 2.77571                | 47.5  |
| 18         | 20.3         | 3.01062                | 52.5  |
| 7          | 35.2         | 3.56105                | 57.5  |
| 3          | 47.75        | 3.86598                | 62.5  |
| 16         | 48.6         | 3.88362                | 67.5  |
| 24         | 48.85        | 3.88875                | 72.5  |
| 17         | 49.0         | 3.89182                | 77.5  |
| 32         | 110.2        | 4.70230                | 82.5  |
| 18         | 110.65       | 4.70637                | 87.5  |
| 4          | 201.75       | 5.30703                | 92.5  |
| 22         | 202.0        | 5.30827                | 97.5  |

$N = 20$

FIGURE 31.

LOGNORMAL MODEL FOR DC ACCELERATED STRESS TEST DATA  
 HIGH TEMPERATURE ( $T_H = 340^{\circ}\text{C}$ )  
 20 GHz SCHOTTKY-BARRIER IMPATT DIODE



VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

SS=SUM OF SQUARES

$$= \sum X_I^2 - \frac{(\sum X_I)^2}{N}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK

N = NUMBER OF DEVICES

$$N = 20$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2653$$

AT 90% CONFIDENCE,  $N = 20$ :

$$D^*_{\text{MIN}} = 0.2657 \quad D^*_{\text{MAX}} = 0.2857$$

$D_{\text{DATA}}$  IS NOT BETWEEN  $D^*_{\text{MIN}}$  AND  $D^*_{\text{MAX}}$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS NOT VALID.

NOTE: FOR THE PURPOSE OF THIS TEST, LIFETIMES OF ZERO HOURS WERE ASSIGNED  $T=0.01$  HOURS.

\*ZAR, J.H. 1974 BIostatistical Analysis.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.

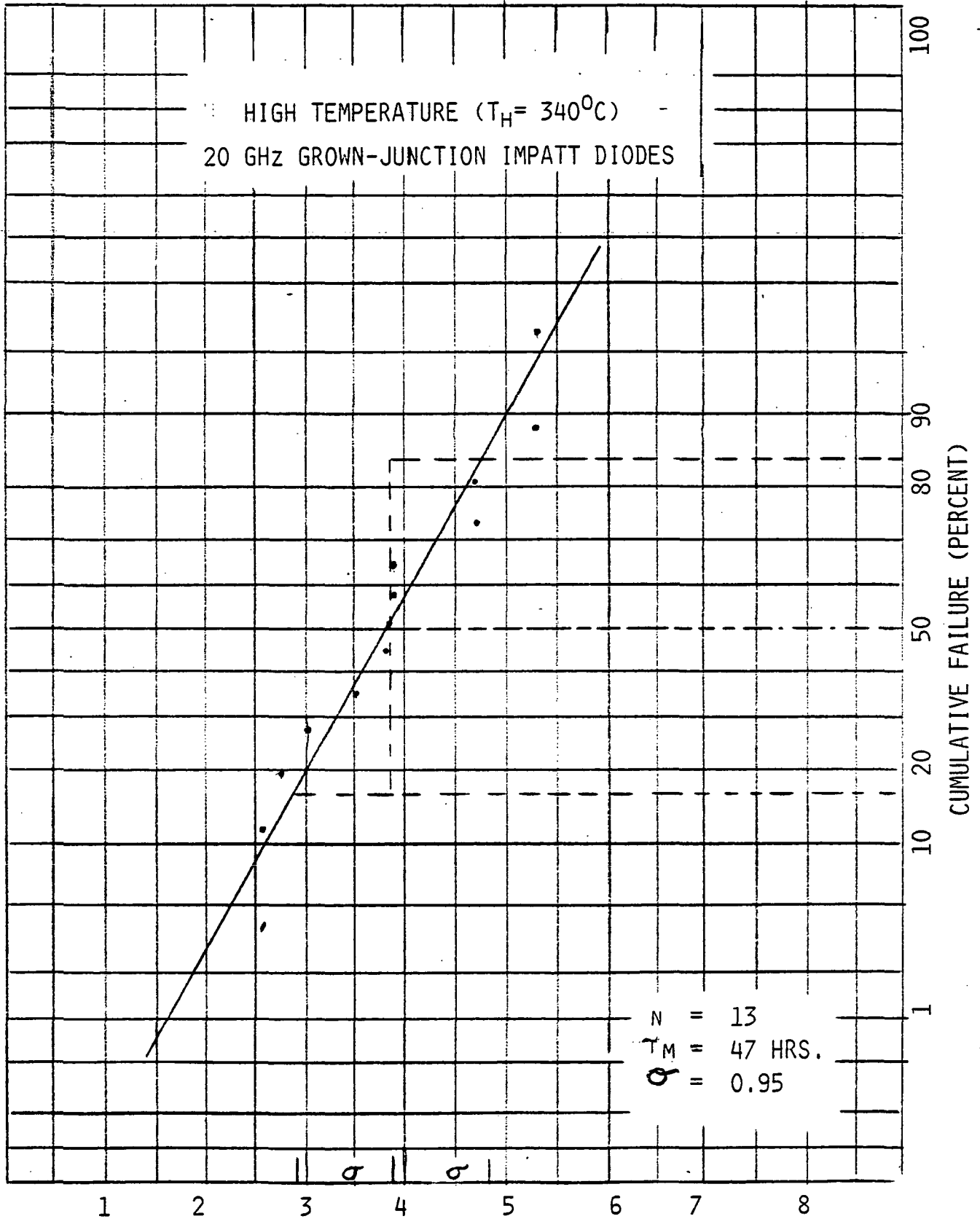


FIGURE 33.

$X = \text{LN (TIME TO FAILURE-HRS)}$

DC ACCELERATED STRESS TEST DATA FOR  
HIGH TEMPERATURE ( $T_H = 340^{\circ}\text{C}$ )  
20 GHz GROWN-JUNCTION IMPATT DIODES



| DEVICE- S/N | $T_I$ (HRS.) | $X_I = LNT_I$ | CUMULATIVE<br>% FAILURES = $\frac{2I-1}{2N} \times 100\%$ |
|-------------|--------------|---------------|---|
| 33          | 12.8         | 2.54945       | 3.8   |
| 1           | 12.9         | 2.55723       | 11.5  |
| 32          | 16.05        | 2.77571       | 19.2  |
| 18          | 20.3         | 3.01062       | 26.9  |
| 7           | 35.2         | 3.56105       | 34.6  |
| 3           | 47.75        | 3.86598       | 42.3  |
| 16          | 48.6         | 3.88362       | 50  |
| 24          | 48.85        | 3.88875       | 57.7  |
| 17          | 49.0         | 3.89182       | 65.4  |
| 32          | 110.2        | 4.70230       | 73.1  |
| 18          | 110.65       | 4.70637       | 80.8  |
| 4           | 201.75       | 5.30703       | 88.5  |
| 22          | 202.0        | 5.30827       | 96.2  |

N = 13

LOGNORMAL MODEL FOR DC ACCELERATED STRESS TEST DATA  
 HIGH TEMPERATURE ( $T_H = 340^{\circ}\text{C}$ )  
 20 GHz GROWN-JUNCTION IMPATT DIODES



VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

SS = SUM OF SQUARES

$$= \sum X_I^2 - \frac{(\sum X_I)^2}{N}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK

N = NUMBER OF DEVICES

$$N = 13$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2814$$

AT 90% CONFIDENCE,  $N = 13$ :

$$D^*_{\text{MIN}} = 0.2598 \quad D^*_{\text{MAX}} = 0.2849$$

$$D^*_{\text{MIN}} \leq D_{\text{DATA}} \leq D^*_{\text{MAX}}$$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS VALID.

\*ZAR, J.H. 1974 BIOSTATISTICAL ANALYSIS.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.



4.0 Medium Temperature Accelerated Constant DC Stress Test

4.1 Test Conditions

- LNR Schottky Barrier Diodes

$T_j$ : 321°C

$T_{BP}$ : 100°C (constant)

- Varian Grown Junction Diodes

$T_J$ : 321°C

$T_{BP}$ : 125°C (constant)

4.2 Test Data Summary

The same rationale as described in section 6.3 applies.

4.3 Logarithmic Normal Validation

(see section 6.3 for rationale)

4.4 Initial and Final DC and RF Data

(see section 6.3 for description)

4.5 Medium Temperature Test Results

SCHOTTKY BARRIER

|  | Early Failure | W/O Early Failure |
|--|---------------|-------------------|
| Number of Devices(N) :                     | 20            | 16                |
| Standard Deviation( $\sigma$ ):            | 2.95          | 0.5               |
| Median Time To Failure<br>( $\gamma_M$ ) : | 30 Hrs.       | 105 Hrs.          |
| D'Agostino Test<br>(Valid/Failed) :        | Failed        | Valid             |

GROWN JUNCTION

|   | Early Failure | W/O Early Failure |
|---|---------------|-------------------|
| Number of Devices(N) :                      | 20            | 18                |
| Standard Deviation( $\sigma$ ) :            | 0.9           | 0.8               |
| Median Time To Failure:<br>( $\gamma_M$ ) : | 210 Hrs.      | 248               |
| D'Agostino Test<br>(Valid/Failed) :         | Valid         | Valid             |

Observations: The Schottky barrier, N=20 sample is not lognormal due to infant mortalities. Therefore, on the Arrhenius plot, the point plotted for schottky barrier medium temperature N=20 is not valid and can not be used to determine activation energy.

INITIAL AND FINAL D.C. AND RF DATA

GROWN JUNCTION DIODES

JUNCTION STRESS TEMPERATURE:

$$T_J = T_M = 321^{\circ}\text{C}$$

BASEPLATE TEMPERATURE:

$$T_{BP} = 125^{\circ}\text{C OR AS NOTED}$$

| DIODE #  | INPUT CURRENT (A) |       | INPUT VOLTAGE (V) |       | LEAKAGE CURRENT (A) |       | BREAKDOWN VOLTAGE (V) |       | INPUT POWER (W) |       | RF POWER (W) |       | ACCUMULATED TEST TIME |        |
|----------|-------------------|-------|-------------------|-------|---------------------|-------|-----------------------|-------|-----------------|-------|--------------|-------|-----------------------|--------|
|          | INITIAL           | FINAL | INITIAL           | FINAL | PRE-TEST            | FINAL | INITIAL               | FINAL | INITIAL         | FINAL | INITIAL      | FINAL |                       |        |
| $T_{BP}$ | 125°C             | 125°C | 125°C             | 125°C | 25°C                | 125°C | 125°C                 | 125°C | 125°C           | 125°C | 25°C         | 25°C  |                       |        |
| 3717/55  | .239              | .209  | 33.37             | 35.56 | 6NA                 | 25NA  | 122NA                 | 19.30 | 19.34           | 7.97  | 7.43         | 1.69  | NA                    | 270.10 |
| 3717/18  | .234              | .208  | 34.13             | 35.88 | 13NA                | 274NA | 38.2µA                | 20.0  | 20.0            | 7.99  | 7.46         | 1.69  | NA                    | 50.70  |
| 3717/21  | .227              | .202  | 34.90             | 38.73 | 1NA                 | 27NA  | 7.1µA                 | 20.6  | 20.4            | 7.92  | 7.82         | 2.10  | NA                    | 102.4  |
| 3717/22  | .209              | .162  | 36.10             | 37.52 | 1NA                 | 28NA  | 407NA                 | 2.18  | 21.9            | 7.54  | 6.08         | 2.00  | NA                    | 240.25 |
| 3717/25  | .224              | .219  | 34.13             | 34.57 | 4NA                 | 20NA  | 42NA                  | 20.4  | 20.3            | 7.65  | 7.57         | 2.19  | NA                    | 38.05  |
| 3717/27  | .213              | .198  | 33.48             | 34.79 | 10NA                | 40NA  | 2.7µA                 | 20.6  | 20.4            | 7.13  | 6.89         | 2.09  | NA                    | 80.85  |
| 3717/28  | .229              | .184  | 33.69             | 36.76 | 1NA                 | 64NA  | 349NA                 | 19.66 | 19.74           | 7.72  | 6.76         | 1.93  | NA                    | 102.55 |
| 3717/30  | .202              | .170  | 34.24             | 35.99 | 2NA                 | 43NA  | 177NA                 | 21.3  | 21.4            | 6.92  | 6.12         | 2.05  | 1.20                  | 695.8  |
| 3717/31  | .192              | .170  | 34.90             | 37.41 | 2NA                 | 94NA  | 101NA                 | 21.2  | 20.9            | 6.70  | 6.36         | 1.30  | NA                    | 533.3  |
| 3717/32  | .211              | .148  | 34.46             | 39.38 | 2NA                 | 22NA  | 830NA                 | 20.5  | 21.3            | 7.27  | 5.83         | 1.80  | .31                   | 604.75 |
| 3717/33  | .220              | .162  | 33.37             | 38.29 | 3NA                 | 51NA  | 2.8µA                 | 20.3  | 20.8            | 7.34  | 6.20         | 1.99  | .58                   | 488.7  |
| 3717/34  | .211              | .191  | 33.26             | 35.01 | 21NA                | 982NA | 1.4µA                 | 20.2  | 20.1            | 7.02  | 6.69         | 1.45  | NA                    | 102.7  |
| 3717/35  | .221              | .188  | 34.79             | 35.12 | 3NA                 | 82NA  | 118NA                 | 20.9  | 21.2            | 7.69  | 6.60         | 1.39  | 1.12                  | 102.75 |
| 3717/36  | .225              | .155  | 33.04             | 38.29 | 1NA                 | 44NA  | 780NA                 | 20.2  | 20.6            | 7.43  | 6.32         | 1.75  | .58                   | 488.7  |
| 3717/37  | .213              | .165  | 33.81             | 37.85 | 12NA                | 28NA  | 503NA                 | 20.5  | 21.0            | 7.20  | 6.25         | 1.62  | .38                   | 696.8  |
| 3717/41  | .242              | .205  | 32.49             | 35.56 | 1NA                 | 137NA | 82.0µA                | 19.51 | 19.69           | 7.86  | 7.29         | 1.52  | NA                    | 365.85 |
| 3717/42  | .226              | .167  | 34.79             | 38.84 | 10NA                | 12NA  | OPEN                  | 20.8  | 21.3            | 7.86  | 6.49         | 1.94  | NA                    | 389.9  |
| 3717/47  | .191              | .164  | 35.66             | 38.07 | 67NA                | 243NA | 356NA                 | 21.5  | 21.5            | 6.81  | 6.24         | 1.60  | NA                    | 382.6  |
| 3717/48  | .203              | .155  | 36.10             | 39.49 | 62NA                | 395NA | 1688NA                | 21.8  | 22.1            | 7.33  | 6.12         | 1.58  | .58                   | 222.35 |
| 3717/50  | .226              | .199  | 34.68             | 37.09 | 2NA                 | 38NA  | 11.4µA                | 21.2  | 21.2            | 7.84  | 7.38         | 1.40  | NA                    | 102.9  |

FIGURE 36

JUNCTION STRESS TEMPERATURE:  
 $T_J = T_M = 321^{\circ}\text{C}$   
 BASEPLATE TEMPERATURE:  
 $T_{BP} = 100^{\circ}\text{C}$  OR AS NOTED

SCHOTTKY BARRIER DIODES

| DIODE #  | INPUT CURRENT |           | INPUT VOLTAGE |           | LEAKAGE CURRENT |         | BREAKDOWN VOLTAGE (1mA) |                 | INPUT POWER (W) |       | RF POWER (W) |       | ACCUMULATED TEST TIME |
|----------|---------------|-----------|---------------|-----------|-----------------|---------|-------------------------|-----------------|-----------------|-------|--------------|-------|-----------------------|
|          | INITIAL (A)   | FINAL (A) | INITIAL (V)   | FINAL (V) | PRE STRESS TEST | INITIAL | FINAL                   | PRE STRESS TEST | INITIAL         | FINAL | INITIAL      | FINAL |                       |
| $T_{BP}$ | 100°C         | 100°C     | 100°C         | 100°C     | 25°C            | 100°C   | 100°C                   | 100°C           | 100°C           | 100°C | 25°C         | 25°C  |                       |
| 1300B    | .202          | .005      | 33.59         | 00.0      | 53NA            | 652NA   | 146.7µA                 | 16.92           | 20.0            | 1.35  | 6.78         | NA    | 93.2                  |
| 1301B    | .194          | .181      | 33.69         | 34.68     | 78NA            | 986NA   | 17.6µA                  | 16.68           | 19.69           | 20.2  | 6.54         | 6.28  | 100.05                |
| 1302B    | .197          | .196      | 33.37         | 33.48     | 627NA           | NA      | NA                      | 17.16           | NA              | NA    | 6.57         | 6.56  | 2.25                  |
| 1303B    | .204          | .185      | 33.48         | 35.01     | 1416NA          | 3.3µA   | 8.4µA                   | 16.18           | 19.39           | 20.4  | 6.83         | 6.48  | 83.4                  |
| 1307B    | .205          | .194      | 32.71         | 33.81     | 214NA           | 1463NA  | 11.0µA                  | 15.19           | 18.33           | 19.76 | 6.71         | 6.56  | 60.45                 |
| 1310G    | .189          | .179      | 34.13         | 35.23     | 90NA            | 430NA   | OUT OF RANGE            | 17.52           | 20.9            | 21.0  | 6.45         | 6.31  | 120.05                |
| 1313G    | .186          | .125      | 34.90         | 40.04     | 50NA            | 1.3µA   | 36.1µA                  | 17.44           | 20.9            | 23.4  | 6.49         | 5.01  | 261.2                 |
| 1314G    | .183          | .176      | 33.37         | 34.46     | 21NA            | 500NA   | 21.0µA                  | 16.35           | 19.68           | 20.8  | 6.11         | 6.06  | 101.4                 |
| 1316G    | .208          | .143      | 30.74         | 37.09     | 98NA            | 194NA   | 36.7µA                  | 15.38           | 18.22           | 21.2  | 6.39         | 5.30  | 159.10                |
| 1317G    | .183          | .171      | 33.81         | 35.66     | 909NA           | 3.2µA   | 57.2µA                  | 16.18           | 19.82           | 20.6  | 6.19         | 6.10  | 121.25                |
| 1318G    | .198          | .189      | 33.04         | 34.13     | 650NA           | 1.9µA   | 42.1µA                  | 16.62           | 19.75           | 19.92 | 6.54         | 6.45  | 84.6                  |
| 1382B    | .219          | .188      | 30.63         | 33.69     | 36NA            | 2.0µA   | 5.9µA                   | 15.36           | 18.03           | 18.78 | 6.71         | 6.33  | 47.75                 |
| 1385B    | .214          | .153      | 31.73         | 37.4      | 17NA            | .4 µA   | 54.7µA                  | 15.84           | 18.82           | 21.2  | 6.79         | 5.72  | 194.9                 |
| 1389B    | .191          | .131      | 33.26         | 38.73     | 11NA            | 558NA   | 55.5µA                  | 16.98           | 20.2            | 22.4  | 6.35         | 5.07  | 261.35                |
| 1392B    | .184          | .170      | 35.01         | 36.32     | 365NA           | .5 µA   | 30.2µA                  | 16.24           | 20.0            | 21.4  | 6.44         | 6.17  | 84.6                  |
| 1396B    | .215          | NA        | 31.29         | NA        | 38NA            | NA      | NA                      | 15.04           | NA              | NA    | 6.73         | NA    | 0                     |
| 1397B    | .203          | .200      | 32.71         | 33.15     | 568NA           | 35.6µA  | OUT OF RANGE            | 13.65           | 16.98           | 0.63  | 6.64         | 6.63  | 15.45                 |
| 1428B    | .211          | .000      | 32.16         | 00.2      | 595NA           | 720.NA  | OUT OF RANGE            | 15.93           | 19.14           | 2.33  | 6.79         | NA    | .61.65                |
| 1429B    | .203          | NA        | 32.05         | NA        | 144NA           | NA      | NA                      | 14.98           | NA              | NA    | 6.51         | NA    | 0                     |
| 1430B    | .193          | .182      | 33.69         | 35.12     | 18NA            | 621NA   | 21.7µA                  | 16.45           | 19.85           | 20.7  | 6.50         | 6.39  | 121.1                 |

FIGURE 37.

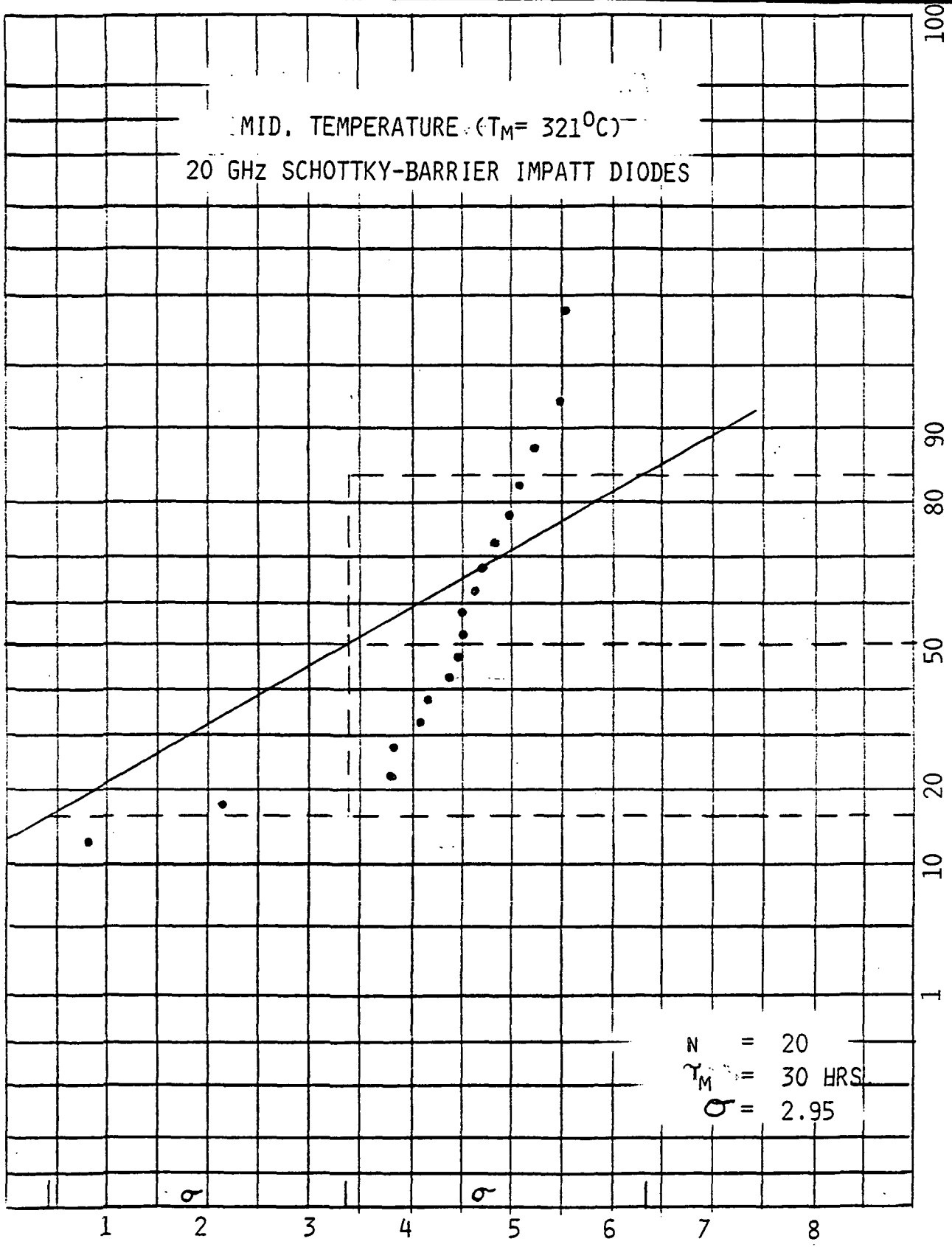


FIGURE 38.

DC ACCELERATED STRESS TEST DATA FOR  
MID. TEMPERATURE ( $T_M = 321^{\circ}\text{C}$ )  
20 GHz SCHOTTKY-BARRIER IMPATT DIODES



| DEVICE S/N | $T_I$ (HRS.) | $X_I = LNT_I$          | CUMULATIVE<br>% FAILURES = $\frac{2I-1}{2N} \times 100\%$ |
|------------|--------------|------------------------|---|
| 1396B      | 0            | $\rightarrow - \infty$ | 2.5   |
| 1429B      | 0            | $\rightarrow - \infty$ | 7.5   |
| 1302B      | 2.25         | .81093                 | 12.5  |
| 1397B      | 8.55         | 2.14593                | 17.5  |
| 1310G      | 44.75        | 3.80109                | 22.5  |
| 1382B      | 46.1         | 3.83081                | 27.5  |
| 1428B      | 60.5         | 4.10264                | 32.5  |
| 1307B      | 65.2         | 4.17746                | 37.5  |
| 1318G      | 81.6         | 4.40183                | 42.5  |
| 1303B      | 87.7         | 4.47392                | 47.5  |
| 1300B      | 93.2         | 4.53475                | 52.5  |
| 1392B      | 93.4         | 4.53689                | 57.5  |
| 1301B      | 105.2        | 4.65586                | 62.5  |
| 1314G      | 114.0        | 4.73620                | 67.5  |
| 1317G      | 122.75       | 4.81015                | 72.5  |
| 1430B      | 147.2        | 4.99180                | 77.5  |
| 1316G      | 159.15       | 5.06985                | 82.5  |
| 1385B      | 189.8        | 5.24597                | 87.5  |
| 1389B      | 243.2        | 5.49388                | 92.5  |
| 1313G      | 262.3        | 5.56949                | 97.5  |

N = 20

FIGURE 39.

VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_i}{\sqrt{N^3 SS}}$$

WHERE,

SS = SUM OF SQUARES

$$= \sum X_i^2 - \frac{(\sum X_i)^2}{N}$$

$$T = \left( i - \frac{N+1}{2} \right) X_i$$

$i$  = SEQUENTIAL RANK

$N$  = NUMBER OF DEVICES

$$N = 20$$

$$D_{\text{DATA}} = \frac{\sum T_i}{\sqrt{N^3 SS}} = 0.2165$$

AT 90% CONFIDENCE,  $N = 20$ :

$$D^*_{\text{MIN}} = 0.2657 \quad D^*_{\text{MAX}} = 0.2857$$

$D_{\text{DATA}}$  IS NOT BETWEEN  $D^*_{\text{MIN}}$  AND  $D^*_{\text{MAX}}$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS NOT VALID.

NOTE: FOR THE PURPOSE OF THIS TEST, LIFETIMES OF  
 ZERO HOURS WERE ASSIGNED  $\tau = 0.01$  HOURS.

\*ZAR, J.H. 1974 BIostatistical Analysis.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.

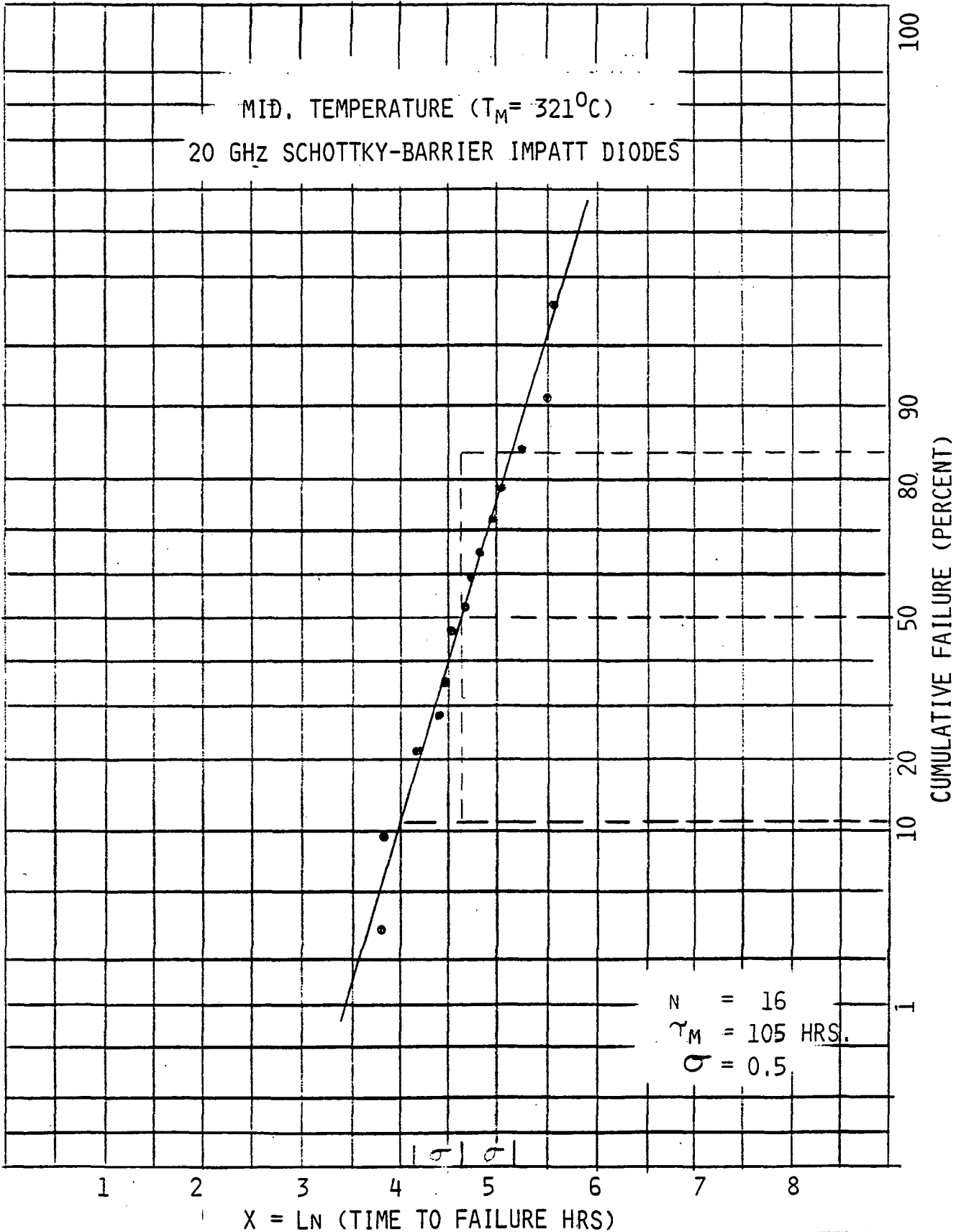


FIGURE 41.



BC ACCELERATED STRESS TEST DATA FOR  
MID. TEMPERATURE ( $T_M = 321^{\circ}\text{C}$ )  
20 GHZ SCHOTTKY-BARRIER IMPATT DIODE



| DEVICE S/N | $T_I$ (HRS.) | $X_I = LNT_I$ | CUMULATIVE<br>% FAILURES = $\frac{2i-1}{2N} \times 100\%$ |
|------------|--------------|---------------|---|
| 1310G      | 44.75        | 3.80109       | 3.1   |
| 1382B      | 46.1         | 3.83081       | 9.4   |
| 1428B      | 60.5         | 4.10264       | 15.6  |
| 1307B      | 65.2         | 4.17746       | 21.9  |
| 1318G      | 81.6         | 4.40183       | 28.1  |
| 1303B      | 87.7         | 4.47392       | 34.4  |
| 1300B      | 93.2         | 4.53475       | 40.6  |
| 1392B      | 93.4         | 4.53689       | 46.9  |
| 1301B      | 105.2        | 4.65586       | 53.1  |
| 1314G      | 114.0        | 4.73620       | 59.4  |
| 1317G      | 122.75       | 4.81015       | 65.6  |
| 1430B      | 147.2        | 4.99180       | 71.9  |
| 1316G      | 159.15       | 5.06985       | 78.1  |
| 1385B      | 189.8        | 5.24597       | 84.4  |
| 1389B      | 243.2        | 5.49388       | 90.6  |
| 1313G      | 262.3        | 5.56949       | 96.9  |

N = 16

FIGURE 42.

VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

$$\begin{aligned} & \text{SS} = \text{SUM OF SQUARES} \\ & = \sum X_I^2 - \frac{(\sum X_I)^2}{N} \end{aligned}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK

N = NUMBER OF DEVICES

$$N = 16$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2846$$

AT 90% CONFIDENCE,  $N = 16$ :

$$D^*_{\text{MIN}} = 0.2634 \quad D^*_{\text{MAX}} = 0.2855$$

$$D^*_{\text{MIN}} \leq D_{\text{DATA}} \leq D^*_{\text{MAX}}$$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS VALID.

\*ZAR, J.H. 1974 BIOSTATISTICAL ANALYSIS.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.

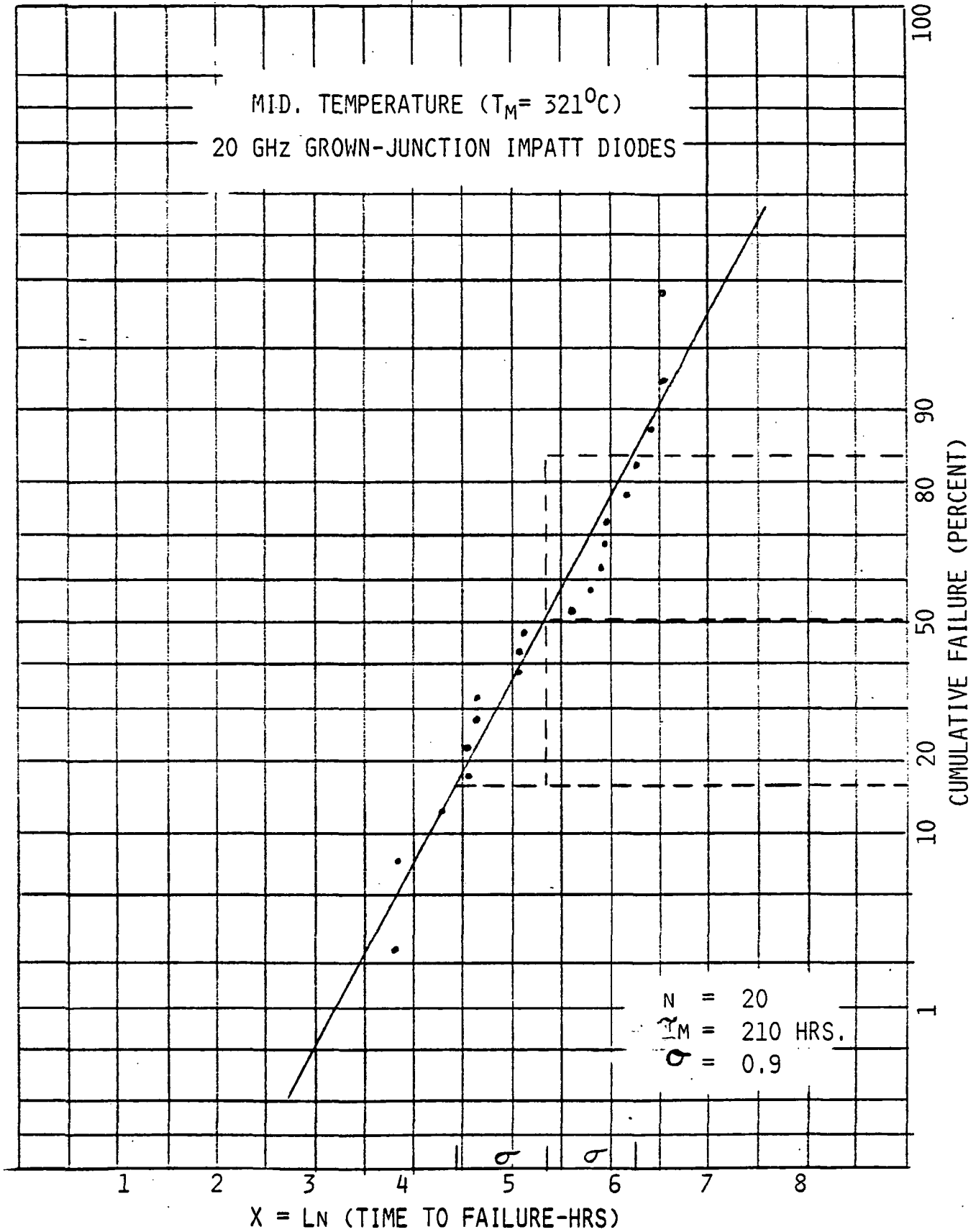


FIGURE 44.

DC ACCELERATED STRESS TEST DATA FOR  
MID. TEMPERATURE ( $T_M = 321^{\circ}\text{C}$ )  
20 GHZ GROWN-JUNCTION IMPATT DIODES



| DEVICE S/N | $T_i$ (HRS.) | $X_i = LNT_i$ | CUMULATIVE<br>% FAILURES = $\frac{2i-1}{2N} \times 100\%$ |
|------------|--------------|---------------|---|
| 25         | 46.15        | 3.832         | 2.5   |
| 18         | 46.65        | 3.843         | 7.5   |
| 27         | 72.7         | 4.286         | 12.5  |
| 21         | 94.55        | 4.549         | 17.5  |
| 22         | 94.7         | 4.551         | 22.5  |
| 35         | 103.05       | 4.635         | 27.5  |
| 34         | 106.5        | 4.668         | 32.5  |
| 28         | 158.95       | 5.069         | 37.5  |
| 50         | 161.7        | 5.086         | 42.5  |
| 48         | 167.55       | 5.121         | 47.5  |
| 55         | 275.45       | 5.618         | 52.5  |
| 33         | 334.0        | 5.811         | 57.5  |
| 41         | 369.0        | 5.911         | 62.5  |
| 47         | 384.4        | 5.952         | 67.5  |
| 42         | 389.9        | 5.966         | 72.5  |
| 36         | 488.7        | 6.192         | 77.5  |
| 31         | 533.3        | 6.279         | 82.5  |
| 32         | 623.7        | 6.436         | 87.5  |
| 30         | 695.9        | 6.545         | 92.5  |
| 37         | 696.9        | 6.547         | 97.5  |

N = 20

FIGURE 45.

VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

$$\begin{aligned} SS &= \text{SUM OF SQUARES} \\ &= \sum X_I^2 - \frac{(\sum X_I)^2}{N} \end{aligned}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK  
 N = NUMBER OF DEVICES

$$N = 20$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2849$$

AT 90% CONFIDENCE,  $N=20$ :

$$D^*_{\text{MIN}} = 0.2657 \quad D^*_{\text{MAX}} = 0.2857$$

$$D^*_{\text{MIN}} \leq D_{\text{DATA}} \leq D^*_{\text{MAX}}$$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS VALID.

\*ZAR, J.H. 1974 BIostatistical Analysis.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.

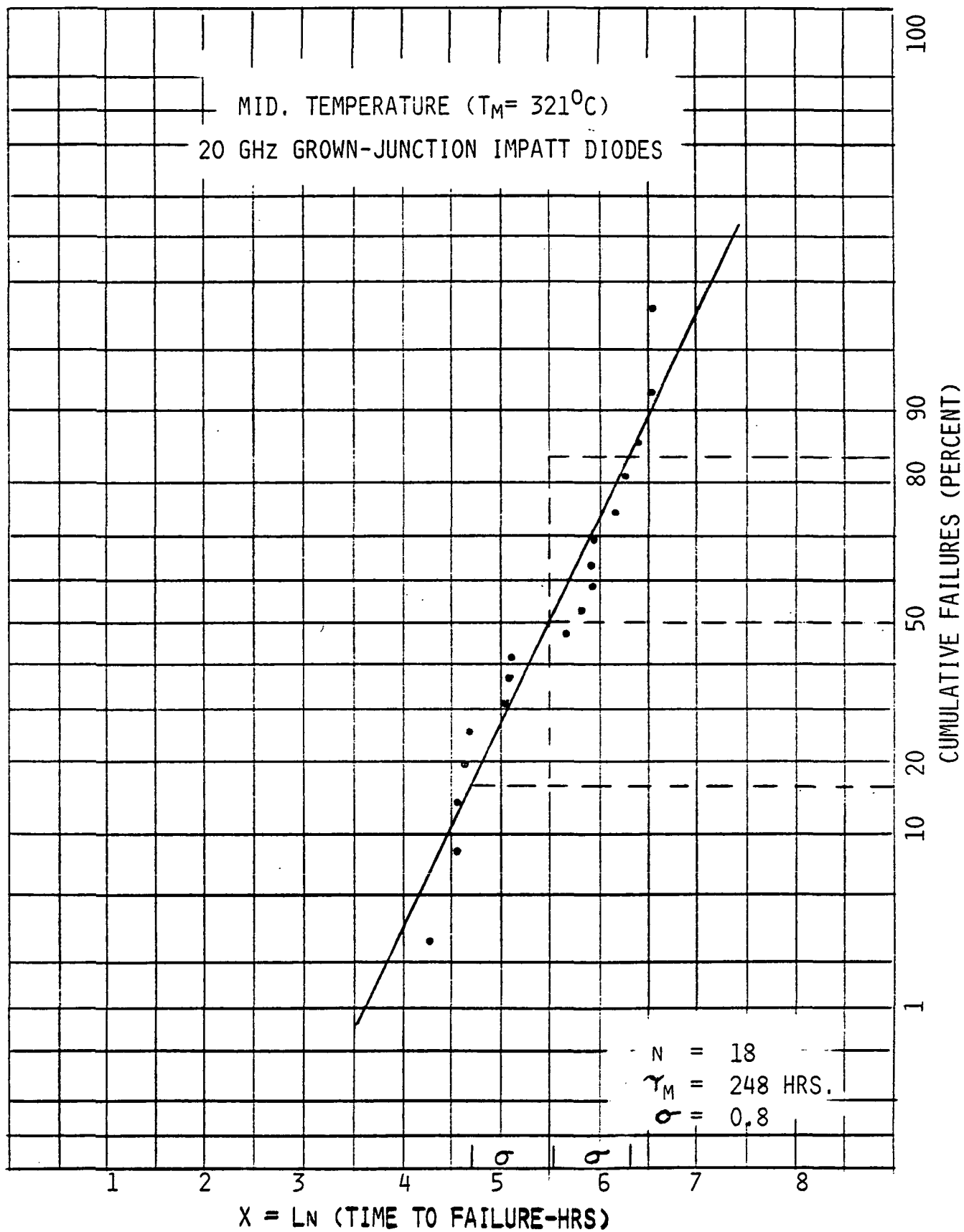


FIGURE 47.

DC ACCELERATED STRESS TEST DATA FOR  
MID. TEMPERATURE ( $T_M = 321^{\circ}\text{C}$ )  
20 GHz GROWN-JUNCTION IMPATT DIODES



| DEVICE S/N | $T_I$ (HRS.) | $X_I = LNT_I$ | CUMULATIVE<br>% FAILURES = $\frac{2I-1}{2N} \times 100\%$ |
|------------|--------------|---------------|---|
| 27         | 72.7         | 4.286         | 2.8   |
| 21         | 94.55        | 4.549         | 8.3   |
| 22         | 94.7         | 4.551         | 13.9  |
| 35         | 103.05       | 4.635         | 19.4  |
| 34         | 106.5        | 4.668         | 25.0  |
| 28         | 158.95       | 5.069         | 30.55   |
| 50         | 161.7        | 5.086         | 36.11   |
| 48         | 167.55       | 5.121         | 41.7  |
| 55         | 275.45       | 5.618         | 47.2  |
| 33         | 334.0        | 5.811         | 52.8  |
| 41         | 369.0        | 5.911         | 58.3  |
| 47         | 384.4        | 5.952         | 63.9  |
| 42         | 389.9        | 5.966         | 69.4  |
| 36         | 488.7        | 6.192         | 75.0  |
| 31         | 533.3        | 6.279         | 80.6  |
| 32         | 623.7        | 6.436         | 86.1  |
| 30         | 695.9        | 6.545         | 91.7  |
| 37         | 696.9        | 6.547         | 97.2  |

N = 18

FIGURE 48.

LOGNORMAL MODEL FOR DC ACCELERATED STRESS TEST DATA  
MID. TEMPERATURE ( $T_M = 321^{\circ}\text{C}$ )  
20 GHZ GROWN-JUNCTION IMPATT DIODES



VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

$$\begin{aligned} SS &= \text{SUM OF SQUARES} \\ &= \sum X_I^2 - \frac{(\sum X_I)^2}{N} \end{aligned}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK

N = NUMBER OF DEVICES

$$N = 18$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2844$$

AT 90% CONFIDENCE,  $N = 18$ :

$$D^*_{\text{MIN}} = 0.2646 \quad D^*_{\text{MAX}} = 0.2855$$

$$D^*_{\text{MIN}} \leq D_{\text{DATA}} \leq D^*_{\text{MAX}}$$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS VALID.

\*ZAR, J.H. 1974 BIostatistical Analysis.  
PRENTICE - HALL, INC. N.J. PP83-84, 504.



## 5.0 Low Temperature Accelerated Constant DC stress Test

### 5.1 Test Condition

- LNR Schottky Barrier Diodes

$$T_J : 299^{\circ}\text{C}$$

$$T_{BP} : 100^{\circ}\text{C (constant)}$$

- Varian Grown Junction Diodes

$$T_J : 304^{\circ}\text{C}$$

$$T_{BP} : 120^{\circ}\text{C}$$

### 5.2 Test Data Summary

The same rationale as described in section 6.3 applies.

### 5.3 Logarithmic Normal Validation

(See section 6.3 for rationale)

### 5.4 Initial and Final DC and RF Data

In addition to the description given in section 6.3, it must be noted here that Varian diodes numbers 3717/7 and 3717/40 were terminated from the testing with no apparent change in any of the monitored parameters, not satisfying the imposed failure criteria. Termination was based on meeting the requirement of 84 percent cumulative failure. Furthermore, the diode characteristics remained very stable, giving no indication of failing within a reasonable time period. However, subsequent thermal resistance and oscillator measurements indicated device failure, because the measured output power was insufficient. Thus, the difficulty associated with monitoring DC parameters without direct correlation to either thermal resistance or RF data is evident. Furthermore, the above observations also substantiate the effects of the Au/Sn solder described in a subsequent section addressing data analysis.

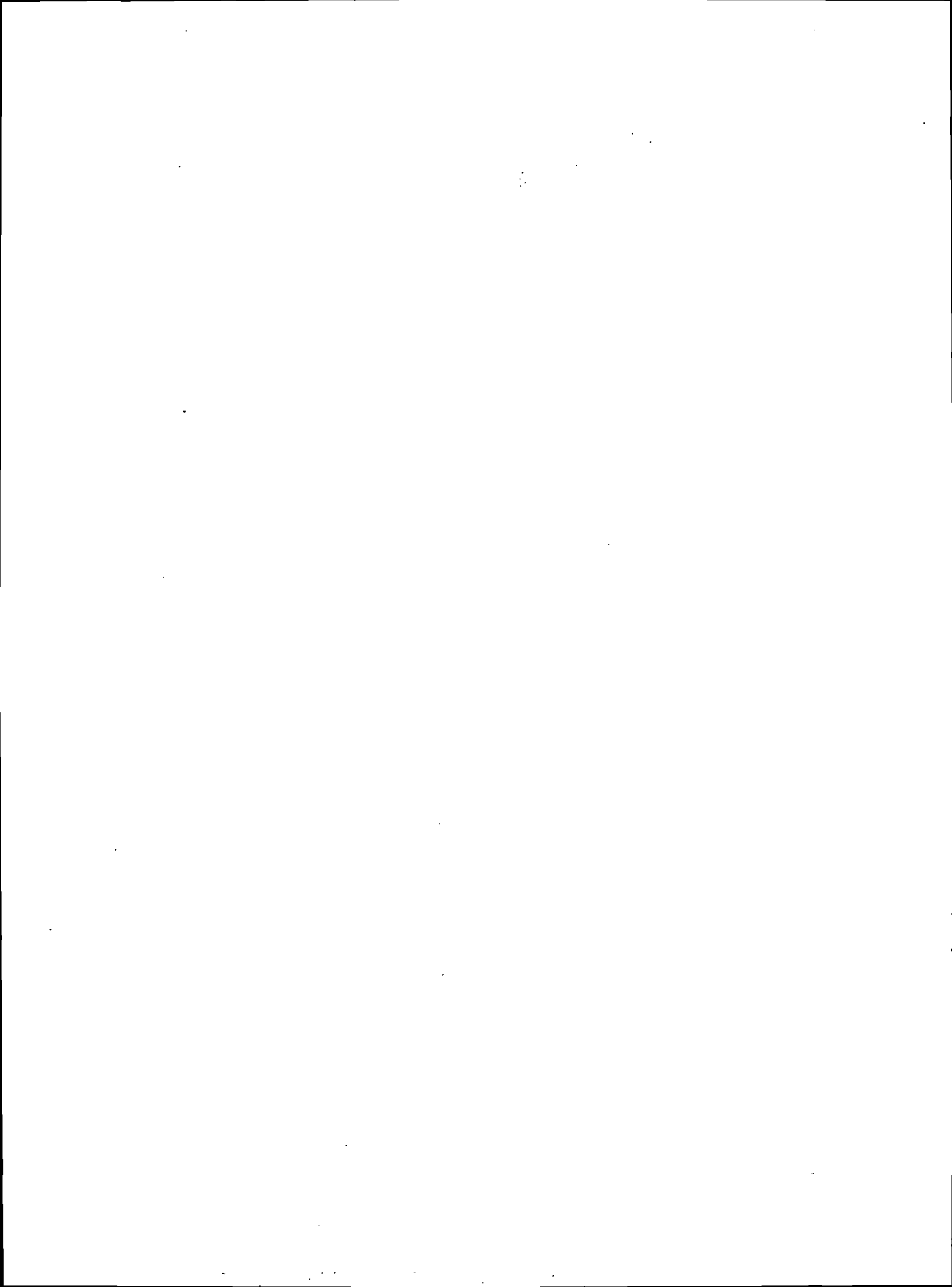
INITIAL AND FINAL D.C. AND RF DATA

JUNCTION STRESS TEMPERATURE:  
 $T_J = T_L = 299^\circ\text{C}$   
 BASEPLATE TEMPERATURE:  
 $T_{BP} = 100^\circ\text{C}$  OR AS NOTED

SCHOTTKY BARRIER DIODES

| DIODE #  | INPUT CURRENT |           | INPUT VOLTAGE |           | LEAKAGE CURRENT |         | BREAKDOWN VOLTAGE (V <sub>BR</sub> ) |                 | INPUT POWER (W) |       | RF POWER (W) | ACCUMULATED TEST TIME |         |       |        |
|----------|---------------|-----------|---------------|-----------|-----------------|---------|--------------------------------------|-----------------|-----------------|-------|--------------|-----------------------|---------|-------|--------|
|          | INITIAL (A)   | FINAL (A) | INITIAL (V)   | FINAL (V) | PRE STRESS TEST | INITIAL | FINAL                                | PRE STRESS TEST | INITIAL         | FINAL |              |                       | INITIAL | FINAL |        |
| $T_{BP}$ | 100°C         | 100°C     | 100°C         | 100°C     | 25°C            | 100°C   | 100°C                                | 100°C           | 100°C           | 100°C | 25°C         | 25°C                  |         |       |        |
| 1497B    | .220          | .211      | 27.90         | 29.54     | 217NA           | 519NA   | 73.3µA                               | 12.73           | 15.22           | 13.66 | 6.14         | 6.23                  | 1.45    | NA    | 360.95 |
| 1499B    | .203          | .192      | 28.12         | 29.54     | 50NA            | 409NA   | 4.4µA                                | 13.10           | 15.60           | 15.72 | 5.71         | 5.67                  | 1.55    | NA    | 334.2  |
| 1500G    | .214          | .204      | 28.88         | 29.87     | 19NA            | 208NA   | 32.2µA                               | 13.01           | 15.52           | 15.43 | 6.18         | 6.09                  | 1.45    | NA    | 194.15 |
| 1549B    | .192          | .183      | 29.65         | 31.18     | 73NA            | .5µA    | 12.2µA                               | 13.73           | 16.56           | 16.48 | 5.69         | 5.71                  | 1.35    | NA    | 435.65 |
| 1552B    | .204          | .198      | 25.71         | 27.24     | 138NA           | 1.4µA   | 15.8µA                               | 12.48           | 14.68           | 14.62 | 5.24         | 5.39                  | 1.17    | NA    | 363.75 |
| 1553B    | .246          | .244      | 25.93         | 25.93     | 268NA           | 976NA   | .3µA                                 | 12.09           | 14.04           | 13.85 | 6.38         | 6.33                  | 1.05    | NA    | 46.95  |
| 1555B    | .229          | .216      | 26.47         | 27.35     | 29NA            | NA      | 61.1µA                               | 12.45           | 1.88            | 12.04 | 6.06         | 5.91                  | 1.47    | NA    | 196.3  |
| 1559B    | .216          | .202      | 27.35         | 28.99     | 13NA            | 221NA   | NA                                   | 12.66           | 15.06           | 8.0   | 5.91         | 5.86                  | 1.44    | NA    | 292.2  |
| 1562B    | .311          | .279      | 24.72         | 27.35     | 594NA           | 47.8µA  | NA                                   | 11.69           | 13.20           | 11.65 | 7.69         | 7.63                  | 1.13    | NA    | 29.05  |
| 1563B    | .250          | .234      | 24.94         | 26.58     | 740NA           | 730NA   | NA                                   | 12.04           | 13.93           | 11.28 | 6.24         | 6.22                  | 1.36    | NA    | 100.9  |
| 1565B    | .229          | .225      | 27.24         | 27.46     | 485NA           | .5µA    | 35.9µA                               | 12.37           | 14.49           | 14.58 | 6.24         | 6.18                  | 1.39    | NA    | 47.05  |
| 1579G    | .242          | .227      | 25.82         | 27.24     | 1.5µA           | 58.8µA  | 41.4µA                               | 12.25           | 14.28           | 14.28 | 6.25         | 6.18                  | 1.41    | NA    | 196.95 |
| 1580G    | .204          | .195      | 28.55         | 29.43     | 1.5µA           | 1363NA  | 1.9µA                                | 13.15           | 15.85           | 15.93 | 5.82         | 5.74                  | 1.37    | NA    | 196.35 |
| 1581G    | .206          | .194      | 26.26         | 28.12     | 315NA           | 401NA   | 31.0µA                               | 12.73           | 14.95           | 14.95 | 5.41         | 5.46                  | 1.41    | NA    | 435.7  |
| 1582G    | .239          | .222      | 25.05         | 26.26     | 518NA           | 1NA     | 68.1µA                               | 12.00           | 28.5            | 13.26 | 5.99         | 5.83                  | 1.49    | NA    | 169.5  |
| 1586G    | .183          | .173      | 31.29         | 32.60     | 575NA           | 1390NA  | 110.5µA                              | 14.18           | 17.32           | 17.00 | 5.73         | 5.64                  | .95     | NA    | 292.25 |
| 1588G    | .192          | .184      | 29.10         | 29.98     | 1.0µA           | 1.0µA   | 23.4µA                               | 13.08           | 15.87           | 15.89 | 5.59         | 5.52                  | 1.23    | NA    | 196.5  |
| 1589G    | .226          | .215      | 25.49         | 26.80     | 1.031NA         | 37.3NA  | 158.2µA                              | 12.24           | 14.29           | 13.93 | 5.76         | 5.76                  | 1.36    | NA    | 292.2  |
| 1591G    | .236          | .225      | 26.15         | 27.02     | 1.026NA         | 1347NA  | NA                                   | 12.43           | 14.43           | .42   | 6.17         | 6.08                  | 1.59    | NA    | 167.3  |
| 1597G    | .266          | .262      | 26.15         | 26.37     | 2.3µA           | 1.1µA   | 35.2µA                               | 11.95           | 13.64           | 13.62 | 6.96         | 6.91                  | 1.28    | NA    | 47.3   |

FIGURE 50.



INITIAL AND FINAL D.C. AND RF DATA



JUNCTION STRESS TEMPERATURE:  
 $T_J = T_L = 304^{\circ}\text{C}$

BASEPLATE TEMPERATURE:  
 $T_{BP} = 120^{\circ}\text{C}$  OR AS NOTED

GROWN JUNCTION DIODES

| DIODE #  | INPUT CURRENT |           | INPUT VOLTAGE |           | LEAKAGE CURRENT |         | BREAKDOWN VOLTAGE (VMA) |         | INPUT POWER (W) |         | RF POWER (W) |         | ACCUMULATED TEST TIME |            |        |
|----------|---------------|-----------|---------------|-----------|-----------------|---------|-------------------------|---------|-----------------|---------|--------------|---------|-----------------------|------------|--------|
|          | INITIAL (A)   | FINAL (A) | INITIAL (V)   | FINAL (V) | PRE STRESS TEST | INITIAL | FINAL                   | INITIAL | FINAL           | INITIAL | FINAL        | INITIAL |                       | FINAL      |        |
| $T_{BP}$ | 120°C         | 120°C     | 120°C         | 120°C     | 25°C            | 120°C   | 120°C                   | 120°C   | 120°C           | 120°C   | 120°C        | 25°C    | 25°C                  |            |        |
| 3717/1   | .214          | .161      | 33.37         | 38.07     | 16NA            | 284NA   | 853NA                   | 16.48   | 20.7            | 21.2    | 7.14         | 6.13    | 2.05                  | .64        | 770.8  |
| 3717/2   | .236          | .174      | 30.74         | 35.77     | 4NA             | 177NA   | 923NA                   | 15.42   | 19.24           | 19.49   | 7.20         | 6.22    | 1.93                  | .17        | 528.7  |
| 3717/4   | .227          | .164      | 31.73         | 36.87     | 8NA             | 308NA   | 4.3µA                   | 15.72   | 19.63           | 20.0    | 7.20         | 6.05    | 1.72                  | .12        | 579    |
| 3717/5   | .220          | .170      | 30.63         | 35.45     | 3NA             | 62NA    | 468NA                   | 15.33   | 19.02           | 19.46   | 6.74         | 6.03    | 1.77                  | SHORT      | 770.5  |
| 3717/6   | .187          | .187      | 33.48         | 34.79     | 3NA             | 1583NA  | 58NA                    | 16.72   | 20.9            | 21.3    | 6.22         | 6.51    | 1.79                  | SHORT      | 196.35 |
| 3717/7   | .220          | .195      | 30.85         | 33.914    | 59NA            | 106NA   | 343NA                   | 15.44   | 19.22           | 19.46   | 6.79         | 6.61    | 2.09                  | POWER < .1 | 842.6  |
| 3717/8   | .213          | .175      | 33.80         | 36.65     | 2NA             | 373NA   | 1.7NA                   | 16.68   | 21.2            | 21.5    | 7.20         | 6.41    | 1.95                  | NA         | 411.65 |
| 3717/9   | .224          | .169      | 29.54         | 35.01     | 1NA             | 19NA    | 757µA                   | 15.44   | 19.34           | 19.83   | 6.62         | 6.08    | 2.15                  | .30        | 554.8  |
| 3717/10  | .215          | .158      | 32.71         | 37.96     | 2NA             | 1220NA  | 641NA                   | 16.02   | 20.2            | 20.4    | 7.03         | 6.00    | 1.95                  | .59        | 770.6  |
| 3717/11  | .214          | .157      | 34.13         | 39.17     | 3NA             | 37NA    | 856NA                   | 16.45   | 20.6            | 21.5    | 7.30         | 6.15    | 1.97                  | .25        | 459.45 |
| 3717/12  | .210          | .205      | 33.70         | 33.59     | 5NA             | 44NA    | 65NA                    | 16.29   | 20.7            | 20.7    | 7.08         | 6.89    | 2.07                  | NA         | 29.9   |
| 3717/13  | .213          | .148      | 31.40         | 36.98     | 18NA            | 185     | 871NA                   | 15.53   | 19.78           | 20.4    | 6.69         | 5.47    | 1.80                  | .63        | 379.1  |
| 3717/14  | .217          | .184      | 30.52         | 33.37     | 96NA            | 216NA   | 722NA                   | 15.49   | 19.35           | 19.49   | 6.62         | 6.14    | 2.13                  | NA         | 411.6  |
| 3717/15  | .202          | .148      | 32.38         | 37.20     | 8NA             | 30NA    | 646NA                   | 16.16   | 20.3            | 20.7    | 6.54         | 5.51    | 1.69                  | .12        | 579.15 |
| 3717/16  | .217          | .194      | 33.04         | 32.27     | 2NA             | 68NA    | NA                      | 16.02   | 20.5            | 20.6    | 7.17         | 6.26    | 2.07                  | NA         | 100.55 |
| 3717/44  | .221          | .212      | 33.59         | 34.24     | 1NA             | 85NA    | 808NA                   | 16.12   | 20.5            | 20.7    | 7.42         | 7.26    | 2.20                  | NA         | 100.55 |
| 3717/39  | .200          | .121      | 33.80         | 39.49     | 6NA             | 293NA   | 1006NA                  | 16.49   | 21.1            | 21.8    | 6.76         | 4.78    | 1.40                  | POWER < .1 | 220.35 |
| 3717/40  | .176          | .140      | 33.37         | 37.63     | 1NA             | 21NA    | 122NA                   | 16.85   | 21.3            | 21.4    | 5.87         | 5.27    | 1.51                  | POWER < .1 | 842.3  |
| 3717/52  | .201          | .159      | 34.13         | 39.17     | 4NA             | 160NA   | 346NA                   | 16.85   | 21.3            | 21.7    | 6.86         | 6.23    | 1.38                  | OPEN       | 770.4  |
| 3717/53  | .211          | .216      | 32.27         | 31.84     | 1NA             | 17NA    | 24NA                    | 15.96   | 19.85           | 20.0    | 6.81         | 6.88    | 1.82                  | NA         | 5.95   |

FIGURE 51.

## 5.5 Low Temperature Test Results

### SCHOTTKY BARRIER

|  | Early Failures | W/O Early Failure |
|--|----------------|-------------------|
| Number of Devices(N):                      | 20             | 18                |
| Standard Deviation( $\sigma$ ):            | 0.75           | 0.5               |
| Median Time To Failure<br>( $\gamma_M$ ) : | 185 Hrs.       | 221 Hrs.          |
| D'Agostino Test<br>(Valid/Failed) :        | Valid          | Valid             |

### GROWN JUNCTION

|  | Early Failures | W/O Early Failures |
|--|----------------|--------------------|
| Number of Devices(N) :                     | 20             | 18                 |
| Standard Deviation( $\sigma$ ):            | 1.1            | 0.65               |
| Median Time To Failure<br>( $\gamma_M$ ) : | 317 Hrs.       | 424 Hrs.           |
| D'Agostino Test<br>(Valid/Failed) :        | Failed         | Valid              |

OBSERVATIONS: The Grown-Junction, N=20 sample is not log-normal, therefore, on the arrhenius plot, the point plotted for grown-junction low temperature, N=20 is not valid and cannot be used to determine activation energy.

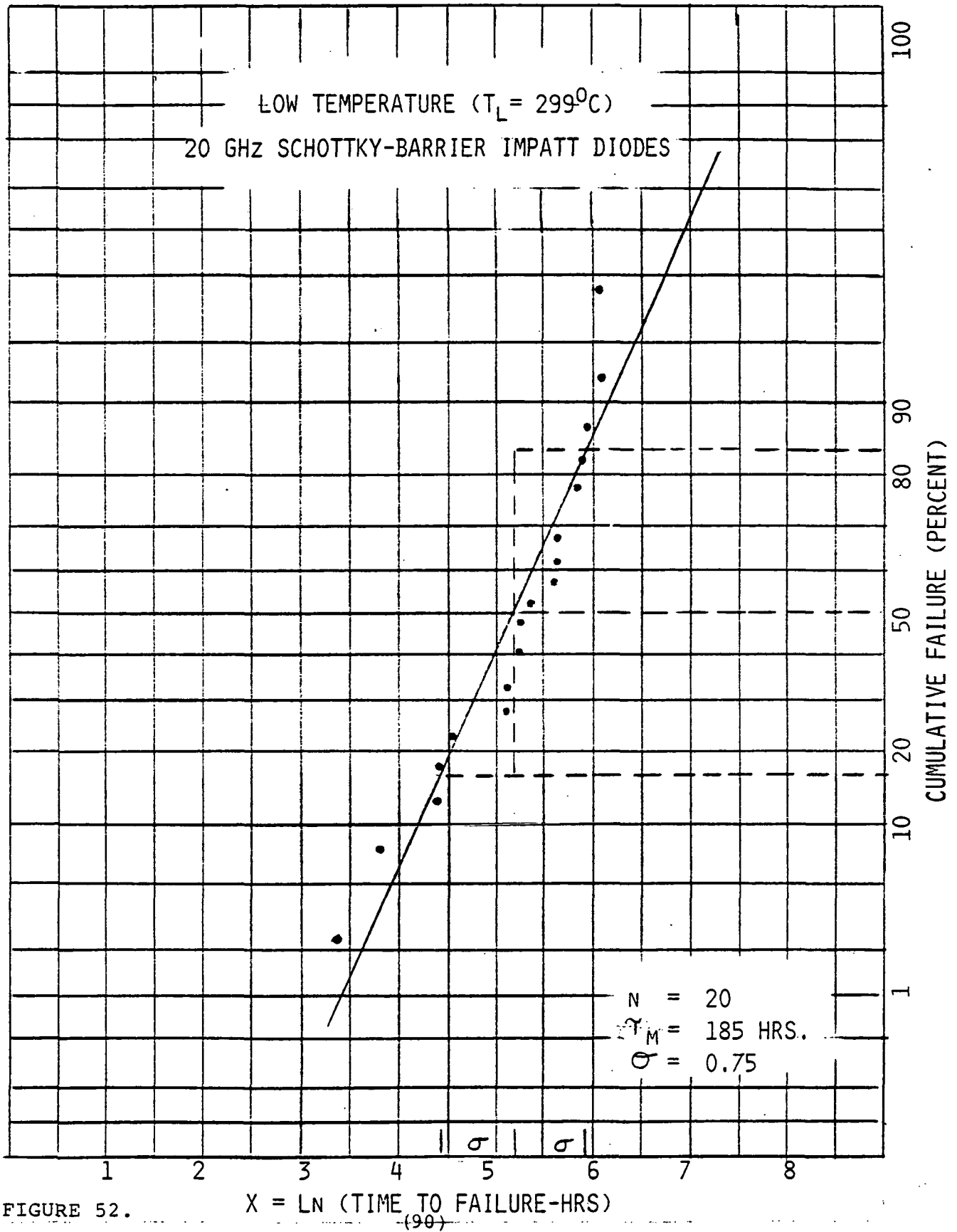


FIGURE 52.

DC ACCELERATED STRESS TEST DATA FOR  
 LOW TEMPERATURE ( $T_L = 299^{\circ}\text{C}$ )  
 20 GHz SCHOTTKY-BARRIER IMPATT DIODES



| DEVICE S/N | $T_I$ (HRS.) | $X_I = LNT_I$ | CUMULATIVE<br>% FAILURES = $\frac{2I-1}{2N} \times 100\%$ |
|------------|--------------|---------------|---|
| 1562B      | 29.05        | 3.369         | 2.5   |
| 1565B      | 45.65        | 3.821         | 7.5   |
| 1597G      | 84.2         | 4.433         | 12.5  |
| 1553B      | 84.3         | 4.434         | 17.5  |
| 1563B      | 95.6         | 4.560         | 22.5  |
| 1591G      | 165.5        | 5.109         | 27.5  |
| 1582G      | 170.5        | 5.139         | 32.5  |
| 1500B      | 191.4        | 5.254         | 37.5  |
| 1555B      | 191.4        | 5.254         | 42.5  |
| 1579G      | 191.6        | 5.255         | 47.5  |
| 1588G      | 218.8        | 5.388         | 52.5  |
| 1580G      | 273.0        | 5.609         | 57.5  |
| 1559B      | 285.0        | 5.652         | 62.5  |
| 1586G      | 287.35       | 5.661         | 67.5  |
| 1589G      | 287.4        | 5.661         | 72.5  |
| 1499B      | 336.6        | 5.819         | 77.5  |
| 1497B      | 356.05       | 5.875         | 82.5  |
| 1552B      | 373.2        | 5.922         | 87.5  |
| 1549B      | 435.65       | 6.077         | 92.5  |
| 1581G      | 435.7        | 6.077         | 97.5  |

N = 20

FIGURE 53.

LOGNORMAL MODEL FOR DC ACCELERATED STRESS TEST DATA  
 LOW TEMPERATURE ( $T_L = 299^{\circ}\text{C}$ )  
 20 GHz SCHOTTKY-BARRIER IMPATT DIODE



VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

SS = SUM OF SQUARES

$$= \sum X_I^2 - \frac{(\sum X_I)^2}{N}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK

N = NUMBER OF DEVICES

$$N = 20$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2690$$

AT 90% CONFIDENCE,  $N = 20$ :

$$D^*_{\text{MIN}} = 0.2657 \quad D^*_{\text{MAX}} = 0.2857$$

$$D^*_{\text{MIN}} \leq D_{\text{DATA}} \leq D^*_{\text{MAX}}$$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS VALID.

\*ZAR, J.H. 1974 BIostatistical Analysis.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.



ACCELERATED DC STRESS TEST DATA

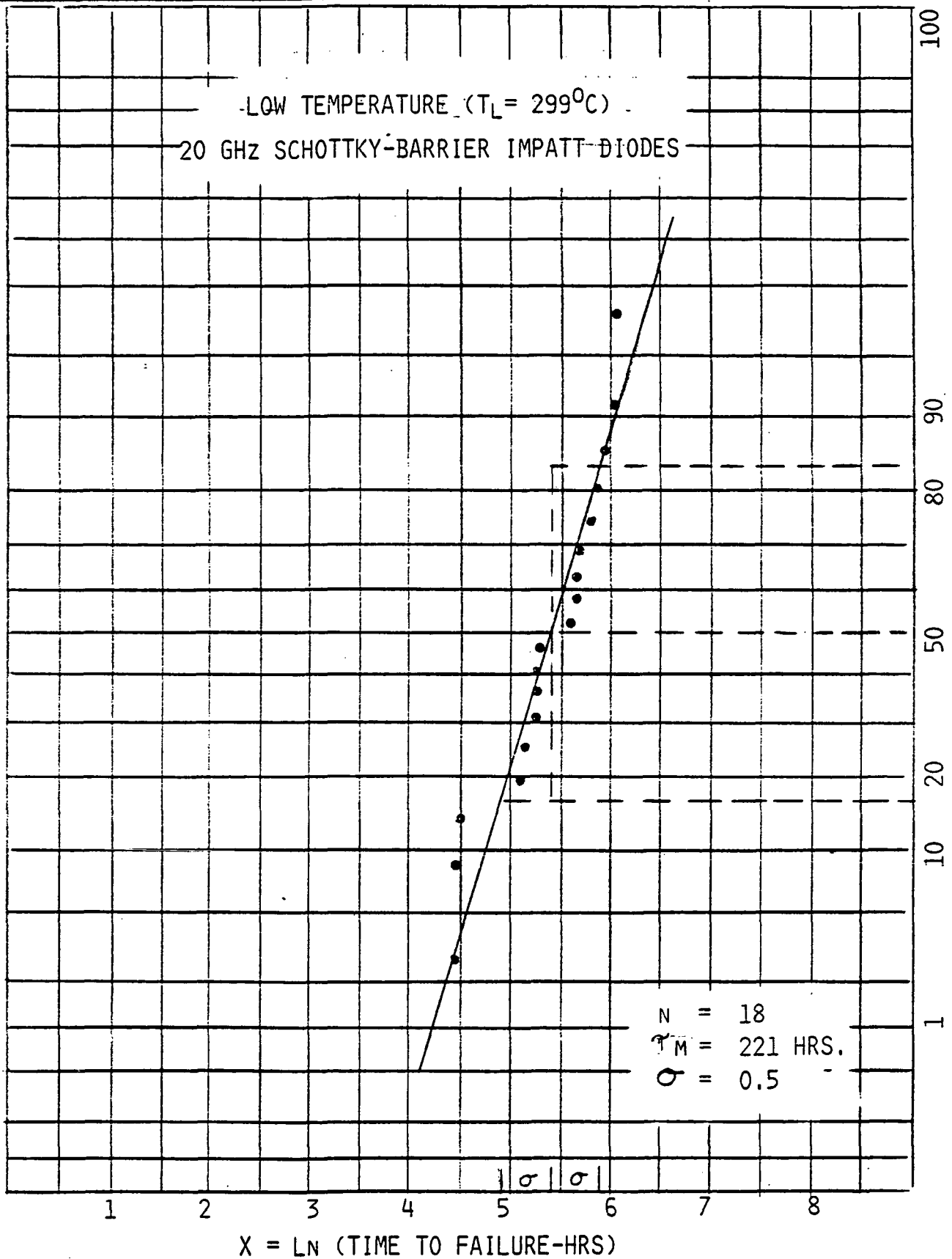


FIGURE 55.

DC ACCELERATED STRESS TEST DATA FOR  
 LOW TEMPERATURE ( $T_L = 299^{\circ}\text{C}$ )  
 20 GHZ SCHOTTKY-BARRIER IMPATT DIODES



| DEVICE S/N | $T_I$ (HRS.) | $X_I = LNT_I$ | CUMULATIVE<br>% FAILURES = $\frac{2I-1}{2N} \times 100\%$ |
|------------|--------------|---------------|---|
| 1597G      | 84.2         | 4.433         | 2.8   |
| 1553B      | 84.3         | 4.434         | 8.3   |
| 1563B      | 95.6         | 4.560         | 13.9  |
| 1591G      | 165.5        | 5.109         | 19.4  |
| 1582G      | 170.5        | 5.139         | 25.0  |
| 1500B      | 191.4        | 5.254         | 30.6  |
| 1555B      | 191.4        | 5.254         | 36.1  |
| 1579G      | 191.6        | 5.255         | 41.7  |
| 1588G      | 218.8        | 5.388         | 47.2  |
| 1580G      | 273.0        | 5.609         | 52.8  |
| 1559B      | 285.0        | 5.652         | 58.3  |
| 1586G      | 287.35       | 5.661         | 63.9  |
| 1589G      | 287.4        | 5.661         | 69.4  |
| 1499B      | 336.6        | 5.819         | 75.0  |
| 1497B      | 356.05       | 5.875         | 80.6  |
| 1552B      | 373.2        | 5.992         | 86.1  |
| 1549G      | 435.65       | 6.077         | 91.7  |
| 1581G      | 435.7        | 6.077         | 97.2  |

N = 18

FIGURE 56.

VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

SS = SUM OF SQUARES

$$= \sum X_I^2 - \frac{(\sum X_I)^2}{N}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK

N = NUMBER OF DEVICES

$$N = 18$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2775$$

AT 90% CONFIDENCE, N = 18:

$$D^*_{\text{MIN}} = 0.2646$$

$$D^*_{\text{MAX}} = 0.2855$$

$$D^*_{\text{MIN}} \leq D_{\text{DATA}} \leq D^*_{\text{MAX}}$$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS VALID.

\*ZAR, J.H. 1974 BIostatistical Analysis.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.

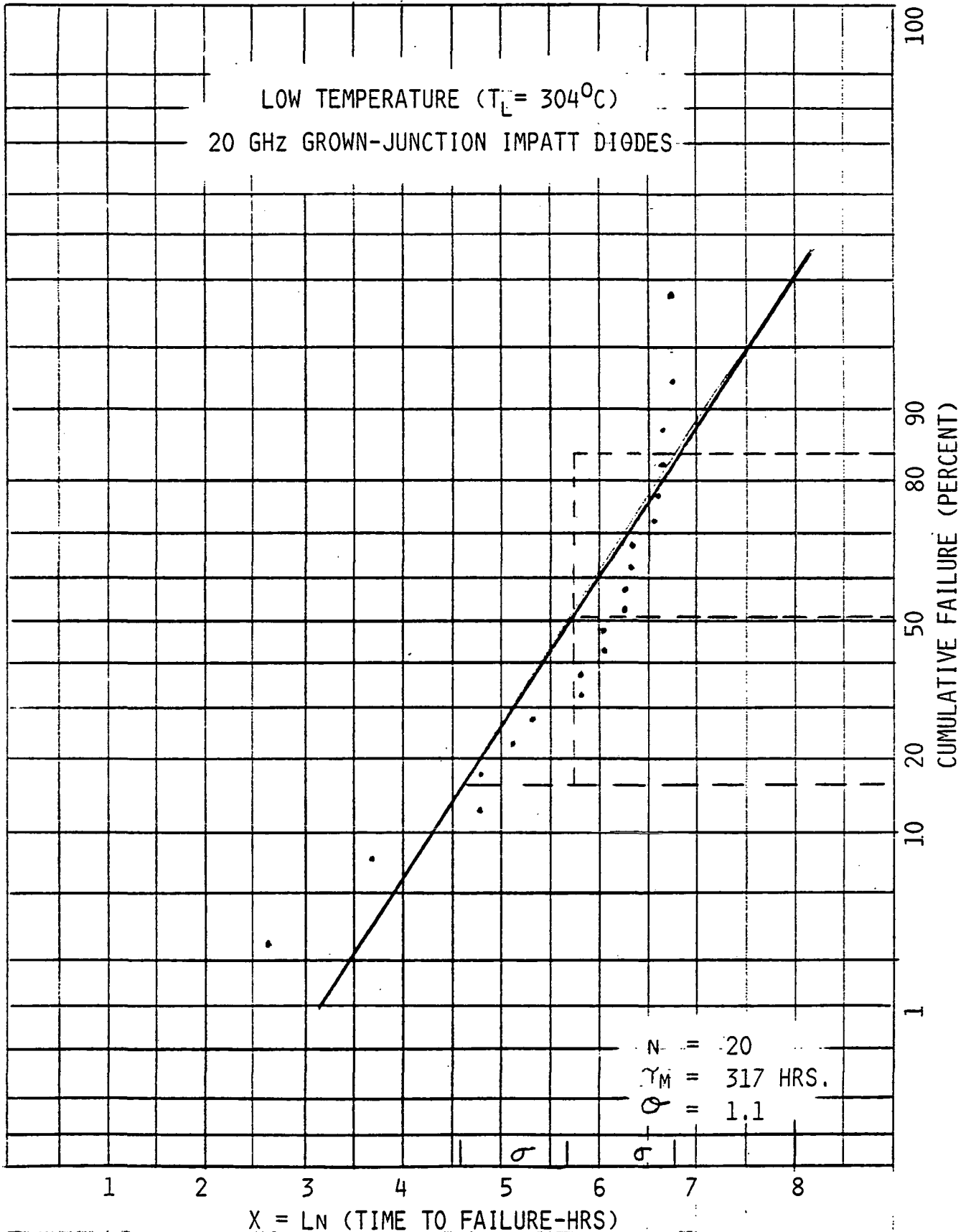


FIGURE 58.

DC ACCELERATED STRESS TEST DATA FOR  
 LOW TEMPERATURE ( $T_L = 304^{\circ}\text{C}$ )  
 20 GHz GROWN-JUNCTION IMPATT DIODES



| DEVICE S/N | $T_I$ (HRS.) | $X_I = LNT_I$ | CUMULATIVE<br>% FAILURES = $\frac{2i-1}{2N} \times 100\%$ |
|------------|--------------|---------------|---|
| 53         | 13.8         | 2.625         | 2.5   |
| 12         | 39.8         | 3.684         | 7.5   |
| 44         | 121.2        | 4.797         | 12.5  |
| 16         | 121.45       | 4.800         | 17.5  |
| 39         | 167.2        | 5.119         | 22.5  |
| 6          | 207.35       | 5.334         | 27.5  |
| 11         | 334.5        | 5.813         | 32.5  |
| 13         | 334.6        | 5.813         | 37.5  |
| 8          | 420.8        | 6.042         | 42.5  |
| 14         | 428.0        | 6.059         | 47.5  |
| 2          | 523.1        | 6.260         | 52.5  |
| 4          | 525.35       | 6.264         | 57.5  |
| 15         | 548.85       | 6.308         | 62.5  |
| 9          | 556.5        | 6.322         | 67.5  |
| 10         | 693.2        | 6.541         | 72.5  |
| 1          | 740.7        | 6.608         | 77.5  |
| 5          | 781.15       | 6.661         | 82.5  |
| 52         | 781.3        | 6.661         | 87.5  |
| 7          | 844.15       | 6.738         | 92.5  |
| 40         | 844.2        | 6.738         | 97.5  |

N = 20

FIGURE 59.

LOGNORMAL MODEL FOR DC ACCELERATED STRESS TEST DATA  
 LOW TEMPERATURE ( $T_L = 304^{\circ}\text{C}$ )  
 20 GHz GROWN-JUNCTION IMPATT DIODES



VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_i}{\sqrt{N^3 SS}}$$

WHERE,

SS = SUM OF SQUARES

$$= \sum X_i^2 - \frac{(\sum X_i)^2}{N}$$

$$T = \left( i - \frac{N+1}{2} \right) X_i$$

$i$  = SEQUENTIAL RANK

$N$  = NUMBER OF DEVICES

$$N = 20$$

$$D_{\text{DATA}} = \frac{\sum T_i}{\sqrt{N^3 SS}} = 0.2536$$

AT 90% CONFIDENCE,  $N = 20$ :

$$D^*_{\text{MIN}} = 0.2657$$

$$D^*_{\text{MAX}} = 0.2857$$

$D_{\text{DATA}}$  IS NOT BETWEEN  $D^*_{\text{MIN}}$  AND  $D^*_{\text{MAX}}$ .

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS NOT VALID.

\*ZAR, J.H. 1974 BIOSTATISTICAL ANALYSIS.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.

ACCELERATED DC STRESS TEST DATA

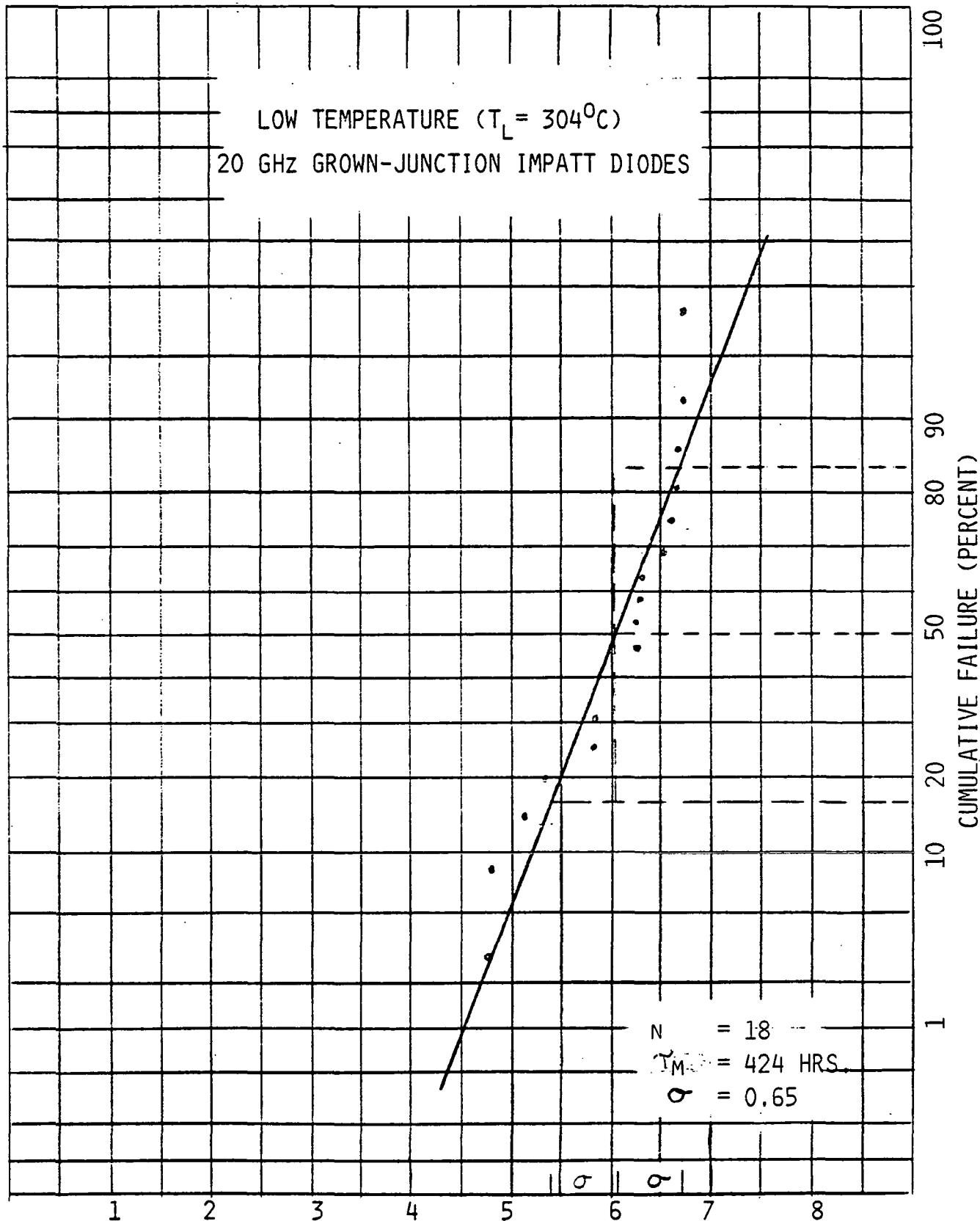


FIGURE 61.  $X = \text{LN} (\text{TIME TO FAILURE-HRS})$   
(99)

DC ACCELERATED STRESS TEST DATA FOR  
 LOW TEMPERATURE ( $T_L = 304^{\circ}\text{C}$ )  
 20 GHz GROWN-JUNCTION IMPATT DIODES



| DEVICE S/N | $T_I$ (HRS.) | $X_I = LNT_I$ | CUMULATIVE<br>% FAILURES = $\frac{2i-1}{2N} \times 100\%$ |
|------------|--------------|---------------|---|
| 44         | 121.2        | 4.797         | 2.8   |
| 16         | 121.45       | 4.800         | 8.3   |
| 39         | 167.2        | 5.119         | 13.9  |
| 6          | 207.35       | 5.334         | 19.4  |
| 11         | 334.5        | 5.813         | 25.0  |
| 13         | 334.6        | 5.813         | 30.55   |
| 8          | 420.8        | 6.042         | 36.11   |
| 14         | 428.0        | 6.059         | 41.7  |
| 2          | 523.1        | 6.260         | 47.2  |
| 4          | 525.35       | 6.264         | 52.8  |
| 15         | 548.85       | 6.308         | 58.3  |
| 9          | 556.5        | 6.322         | 63.9  |
| 10         | 693.2        | 6.541         | 69.4  |
| 1          | 740.7        | 6.608         | 75.0  |
| 5          | 781.15       | 6.661         | 80.6  |
| 52         | 781.3        | 6.661         | 86.1  |
| 7          | 844.15       | 6.738         | 91.7  |
| 19         | 844.2        | 6.738         | 97.2  |

N = 18

FIGURE 62.



VALIDATION BY D'AGOSTINO'S TEST\*

$$D = \frac{\sum T_I}{\sqrt{N^3 SS}}$$

WHERE,

SS = SUM OF SQUARES

$$= \sum X_I^2 - \frac{(\sum X_I)^2}{N}$$

$$T = \left( I - \frac{N+1}{2} \right) X_I$$

I = SEQUENTIAL RANK

N = NUMBER OF DEVICES

$$N = 18$$

$$D_{\text{DATA}} = \frac{\sum T_I}{\sqrt{N^3 SS}} = 0.2730$$

AT 90% CONFIDENCE,  $N=18$ :

$$D^*_{\text{MIN}} = 0.2646$$

$$D^*_{\text{MAX}} = 0.2855$$

$$D^*_{\text{MIN}} \leq D_{\text{DATA}} \leq D^*_{\text{MAX}}$$

THEREFORE, THE ASSUMPTION OF LOGNORMALITY IS VALID.

\*ZAR, J.H. 1974 BIostatistical Analysis.  
 PRENTICE - HALL, INC. N.J. PP83-84, 504.

## V. DATA AND FAILURE ANALYSIS

### 1.0 Arrhenius Dependence

The small number of devices tested and the rather insignificant number identified as early failures, required the development of a different approach in determining the early failure activation energy than the method used in reporting life data <sup>8</sup> when a large test population (N=357) is available. The method developed for the identification of a criteria to define early failure, resulting from a small test population, is described in Appendix 'A'.

Furthermore, a statistical analysis of the obtained life test data was performed, providing refined operational lifetime projections. The resulting data is presented in this section, whereby the analysis is shown in Appendix 'B'.

The Arrhenius dependence expression,

$$\ln \tau_M = \ln \tau_0 + E_a/KT$$

was used to analyze the life-test data in Appendix 'B'. The results of the linear regression and confidence interval determination are summarized here and the refined Arrhenius reaction rate plots are shown. The refined Arrhenius data is somewhat different from the preliminary Arrhenius reported in November, 1983, since the early failure definition was somewhat arbitrary.

The sequence of the data shown is as follows:

- A. Summary Data of both types of Diodes
- B. Schottky Barrier
  - Diode Identification and failure times for the three test temperatures.
  - Combined Lifetimes vs. the inverse of the test temperatures plot with early failures defined according to 'Appendix A', which are below the range of the main population.

- Combined Diode Identification and failure times with early failures removed.
- Combined Log-Normal Plot with early failures removed.
- Final Arrhenius (Regression) Line Plot

The above sequence is repeated for the grown junction diodes.

SUMMARY  
OF:

STATISTICAL ANALYSIS OF LIFE TEST DATA



DEVICE PARAMETERS  
EXTRAPOLATED TO 200°C

SCHOTTKY BARRIER

GROWN JUNCTION

$E_A$  (ACTIVATION ENERGY)

1.148EV

1.887EV

$\text{LN}\tau_0$  (PRE-EXPONENTIAL FACTOR)

-17.829

-31.694

ESTIMATED  $\gamma_M$

29,829 HRS.

2,111,865 HRS.

$P \{ \gamma_M > \text{LOWER BOUND} \} = 90\%$

12,929 HRS.

397,630 HRS.

ESTIMATED  $\text{LOG}_E$ -VARIANCE ( $\sigma^2$ )

0.342

0.688

$P \{ \text{LOWER BOUND} \leq \sigma^2 \leq \text{UPPER BOUND} \} = 90\%$

$0.254 \leq \sigma^2 \leq 0.490$

$0.508 \leq \sigma^2 \leq 0.994$

LIFETIME OF A SINGLE UNTESTED DEVICE

$P \{ t_{N+1} > \text{LOWER BOUND} \} = 90\%$

9,641 HRS.

289,485 HRS.

31

DC ACCELERATED STRESS TEST DATA FOR  
20 GHZ SCHOTTKY-BARRIER GAAS IMPATT DIODES



| HIGH TEMPERATURE<br>( $T_H=345^{\circ}\text{C}$ )<br>N = 20 |              | MID. TEMPERATURE<br>( $T_M=321^{\circ}\text{C}$ )<br>N = 20 |              | LOW TEMPERATURE<br>( $T_L=299^{\circ}\text{C}$ )<br>N = 20 |              |
|---|--------------|---|--------------|--|--------------|
| DEVICE S/N  | $T_I$ (HRS.) | DEVICE S/N  | $T_I$ (HRS.) | DEVICE S/N   | $T_I$ (HRS.) |
| 1238G   | 4.55         | 1396B   | 0            | 1562B  | 29.05        |
| 1229G   | 11.1         | 1429B   | 0            | 1565B  | 45.65        |
| 1116B   | 12.8         | 1302B   | 2.25         | 1597G  | 84.2         |
| 680G  | 13.6         | 1397B   | 8.55         | 1553B  | 84.3         |
| 668G  | 22.25        | 1310G   | 44.75        | 1563B  | 95.6         |
| 362D  | 24.5         | 1382B   | 46.1         | 1591G  | 165.5        |
| 366D  | 25.8         | 1428B   | 60.5         | 1582G  | 170.5        |
| 685G  | 32.8         | 1307B   | 65.2         | 1500B  | 191.4        |
| 1231G   | 38.5         | 1318G   | 81.6         | 1555B  | 191.4        |
| 514G  | 44.8         | 1303B   | 87.7         | 1579G  | 191.6        |
| 1188G   | 45.6         | 1300B   | 93.2         | 1588G  | 218.8        |
| 1106B   | 46.1         | 1392B   | 93.4         | 1580G  | 273.0        |
| 1180G   | 48.8         | 1301B   | 105.2        | 1559B  | 285.0        |
| 470G  | 48.8         | 1314G   | 114.0        | 1586G  | 287.35       |
| 1223G   | 55.6         | 1317G   | 122.75       | 1589G  | 287.4        |
| 1220G   | 65.8         | 1430B   | 147.2        | 1499B  | 336.6        |
| 1254M   | 70.7         | 1316G   | 159.15       | 1497B  | 356.05       |
| 1237G   | 80.2         | 1385B   | 189.8        | 1552B  | 373.2        |
| 1264M   | 80.7         | 1389B   | 243.2        | 1549B  | 435.65       |
| 1177G   | 147.8        | 1313G   | 262.3        | 1581G  | 435.7        |

FIGURE 65.

ILLUSTRATION OF INDIVIDUAL DEVICE LIFETIME VS.  
 ACCELERATED TEST TEMPERATURE BEFORE DETERMINATION  
 OF EARLY FAILURES. (NOTE: FAILURE TIMES LESS THAN  
 1 HOUR ARE NOT SHOWN)



SCHOTTKY-BARRIER IMPATTS : 60 DIODES TESTED

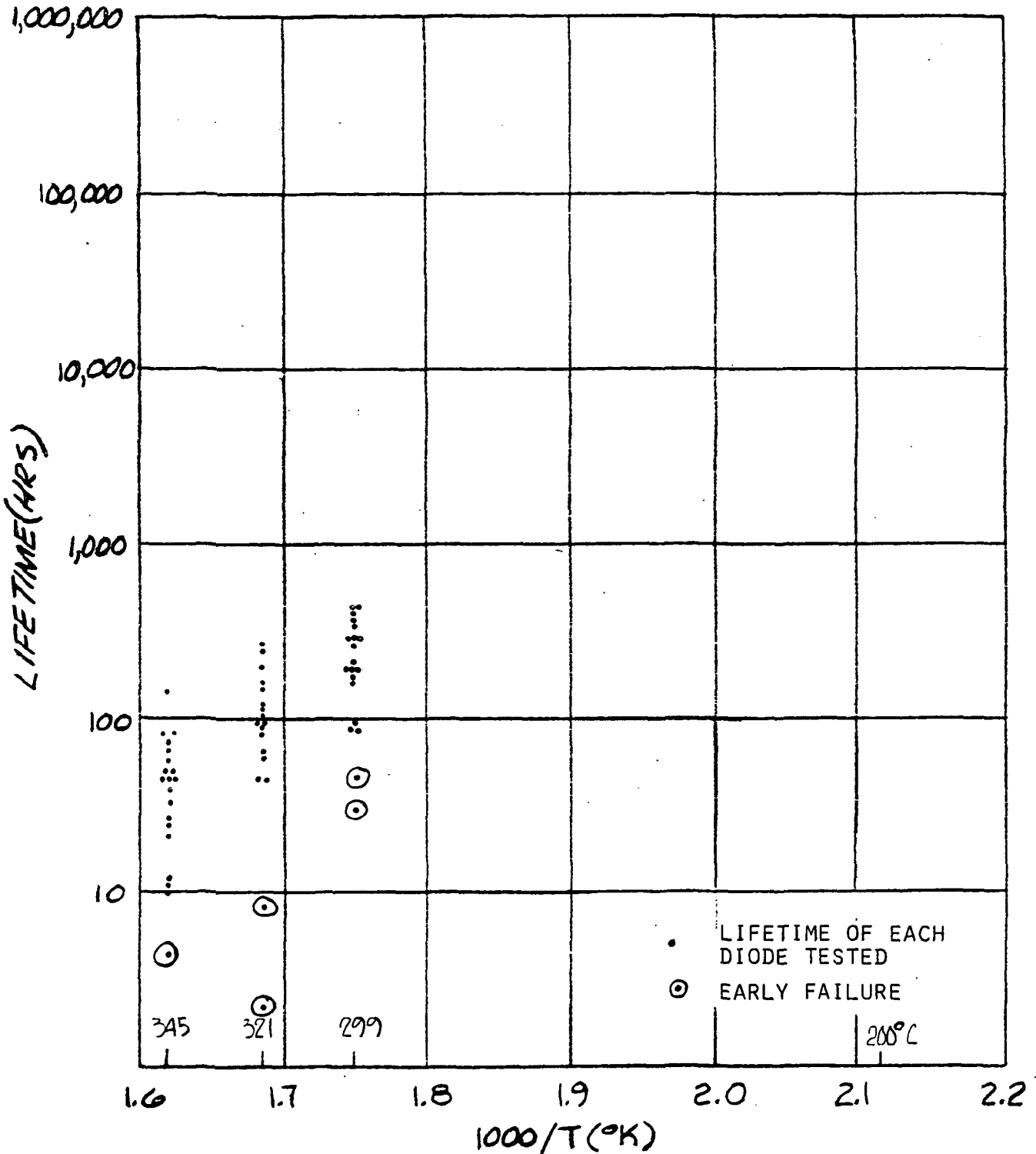


FIGURE 66.

DC ACCELERATED STRESS TEST DATA FOR  
20 GHZ SCHOTTKY-BARRIER GAAS IMPATT DIODES



EARLY FAILURES REMOVED

| HIGH TEMPERATURE<br>( $T_H = 345^{\circ}\text{C}$ )<br>N=19 |              | MID. TEMPERATURE<br>( $T_M = 321^{\circ}\text{C}$ )<br>N=16 |              | LOW TEMPERATURE<br>( $T_L = 299^{\circ}\text{C}$ )<br>N=18 |              |
|---|--------------|---|--------------|--|--------------|
| DEVICE S/N  | $T_I$ (HRS.) | DEVICE S/N  | $T_I$ (HRS.) | DEVICE S/N   | $T_I$ (HRS.) |
| 1229G   | 11.1         | 1310G   | 44.75        | 1597G  | 84.2         |
| 1116B   | 12.8         | 1382B   | 46.1         | 1553B  | 84.3         |
| 680G  | 13.6         | 1428B   | 60.5         | 1563B  | 95.6         |
| 668G  | 22.25        | 1307B   | 65.2         | 1591G  | 165.5        |
| 362D  | 24.5         | 1318G   | 81.6         | 1582G  | 170.5        |
| 366D  | 25.8         | 1303B   | 87.7         | 1500B  | 191.4        |
| 685G  | 32.8         | 1300B   | 93.2         | 1555B  | 191.4        |
| 1231G   | 38.5         | 1392B   | 93.4         | 1579G  | 191.6        |
| 514G  | 44.8         | 1301B   | 105.2        | 1588G  | 218.8        |
| 1188G   | 45.6         | 1314G   | 114.0        | 1580G  | 273.0        |
| 1106B   | 46.1         | 1317G   | 122.75       | 1559B  | 285.0        |
| 1180G   | 48.8         | 1430B   | 147.2        | 1586G  | 287.35       |
| 470G  | 48.8         | 1316G   | 159.15       | 1589G  | 287.4        |
| 1223G   | 55.6         | 1385B   | 189.8        | 1499B  | 336.6        |
| 1220G   | 65.8         | 1389B   | 243.2        | 1497B  | 356.05       |
| 1254M   | 70.7         | 1313G   | 262.3        | 1552B  | 373.2        |
| 1237G   | 80.2         |   |              | 1549B  | 435.65       |
| 1264M   | 80.7         |   |              | 1581G  | 435.7        |
| 1177G   | 147.8        |   |              |  |              |

$N_T = 53$

FIGURE 67.

# SCHOTTKY BARRIER DIODES COMBINED LOGNORMAL PLOT



EARLY FAILURES REMOVED

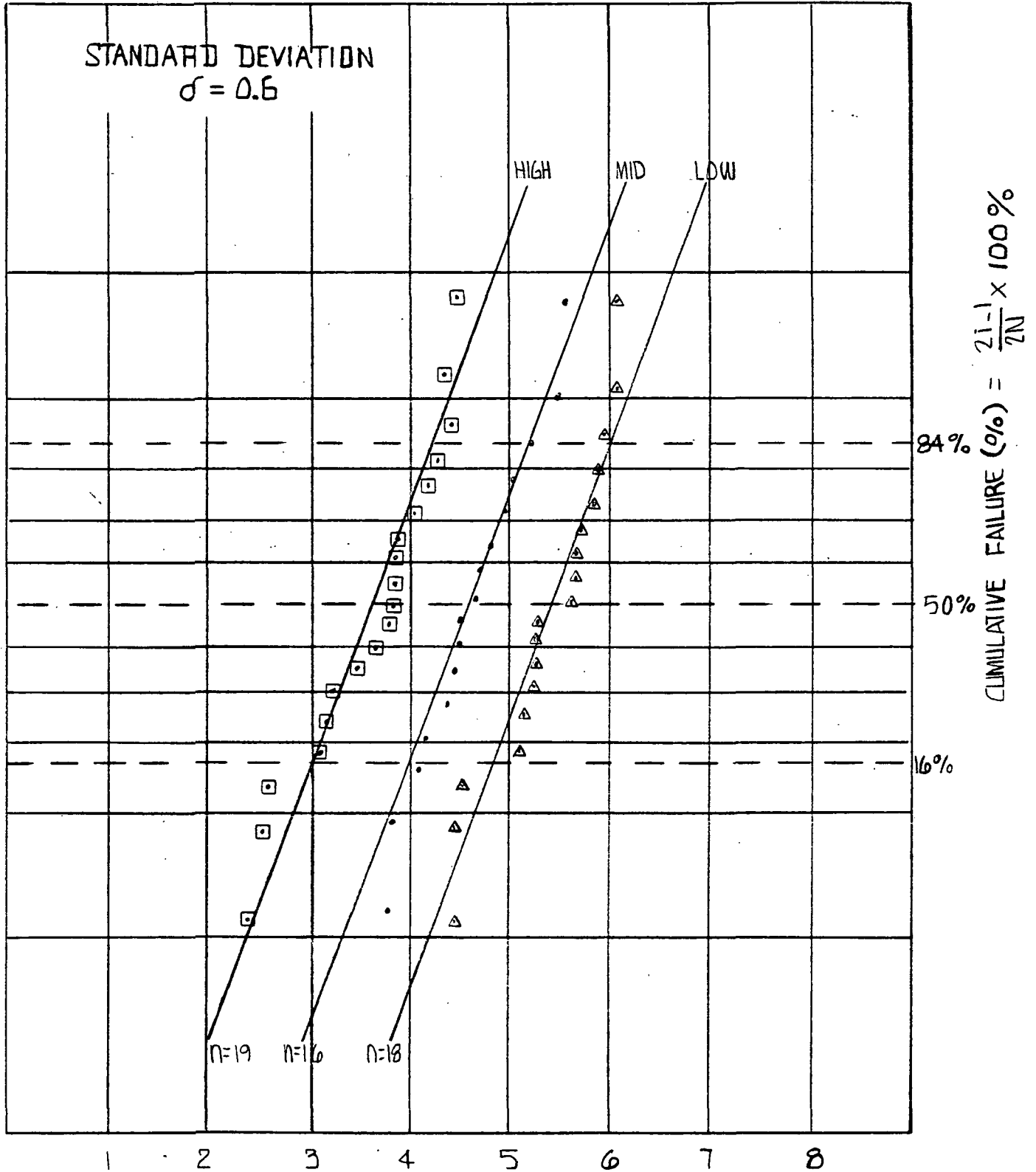


FIGURE 68.

$L_n$  (LIFETIME)  
(108)



# ARRHENIUS (REGRESSION) LINE PLOT



## SCHOTTKY-BARRIER IMPATT'S

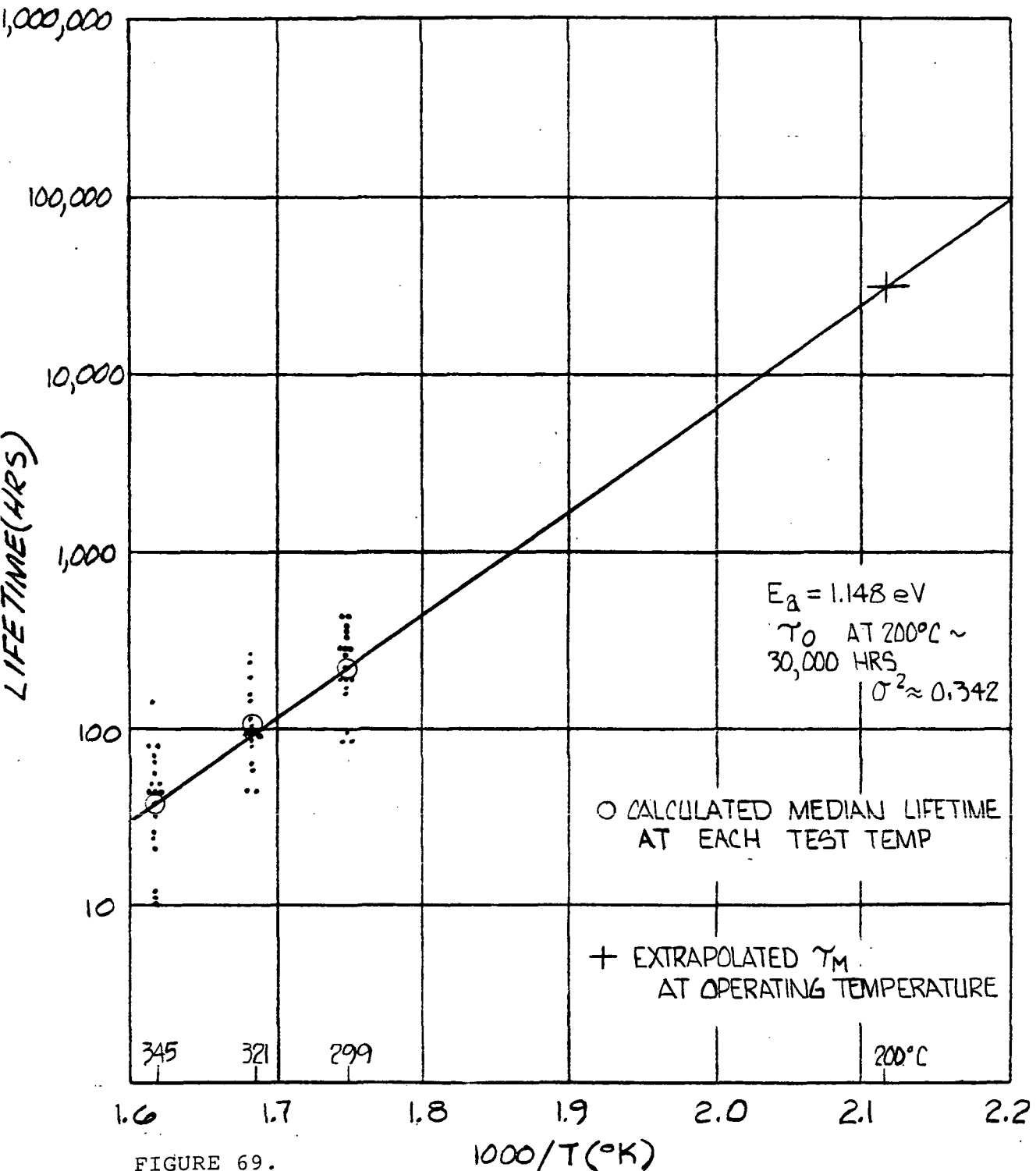


FIGURE 69.

DC ACCELERATED STRESS TEST DATA FOR  
20 GHZ GROWN-JUNCTION GAAS IMPATT DIODES



HIGH TEMPERATURE  
( $T_H = 340^{\circ}\text{C}$ )  
N = 20

MID. TEMPERATURE  
( $T_M = 321^{\circ}\text{C}$ )  
N = 20

LOW TEMPERATURE  
( $T_L = 304^{\circ}\text{C}$ )  
N = 20

| DEVICE S/N | $T_I$ (HRS.) | DEVICE S/N | $T_I$ (HRS.) | DEVICE S/N | $T_I$ (HRS.) |
|------------|--------------|------------|--------------|------------|--------------|
| 19         | 0            | 25         | 46.15        | 53         | 13.8         |
| 35         | 0            | 18         | 46.65        | 12         | 39.8         |
| 36         | 0            | 27         | 72.7         | 44         | 121.2        |
| 8          | 0            | 21         | 94.55        | 16         | 121.45       |
| 31         | 0.5          | 22         | 94.7         | 39         | 167.2        |
| 37         | 1.0          | 35         | 103.05       | 6          | 207.35       |
| 17         | 2.5          | 34         | 106.5        | 11         | 334.5        |
| 33         | 12.8         | 28         | 158.95       | 13         | 334.6        |
| 1          | 12.9         | 50         | 161.7        | 8          | 420.8        |
| 32         | 16.05        | 48         | 167.55       | 14         | 428.0        |
| 18         | 20.3         | 55         | 275.45       | 2          | 523.1        |
| 7          | 35.2         | 33         | 334.0        | 4          | 525.35       |
| 3          | 47.75        | 41         | 369.0        | 15         | 548.85       |
| 16         | 48.6         | 47         | 384.4        | 9          | 556.5        |
| 24         | 48.85        | 42         | 389.9        | 10         | 693.2        |
| 17         | 49.0         | 36         | 488.7        | 1          | 740.7        |
| 32         | 110.2        | 31         | 533.3        | 5          | 781.15       |
| 18         | 110.65       | 32         | 623.7        | 52         | 781.3        |
| 4          | 201.75       | 30         | 695.9        | 7          | 844.15       |
| 22         | 202.0        | 37         | 696.9        | 19         | 844.2        |

FIGURE 70.

ILLUSTRATION OF INDIVIDUAL DEVICE LIFETIME  
 VS. ACCELERATED TEST TEMPERATURE BEFORE  
 DETERMINATION OF EARLY FAILURES.  
 (NOTE: FAILURE TIMES LESS THAN 1 HR. ARE NOT SHOWN)



GROWN-JUNCTION IMPATTS: 60 DEVICES TESTED

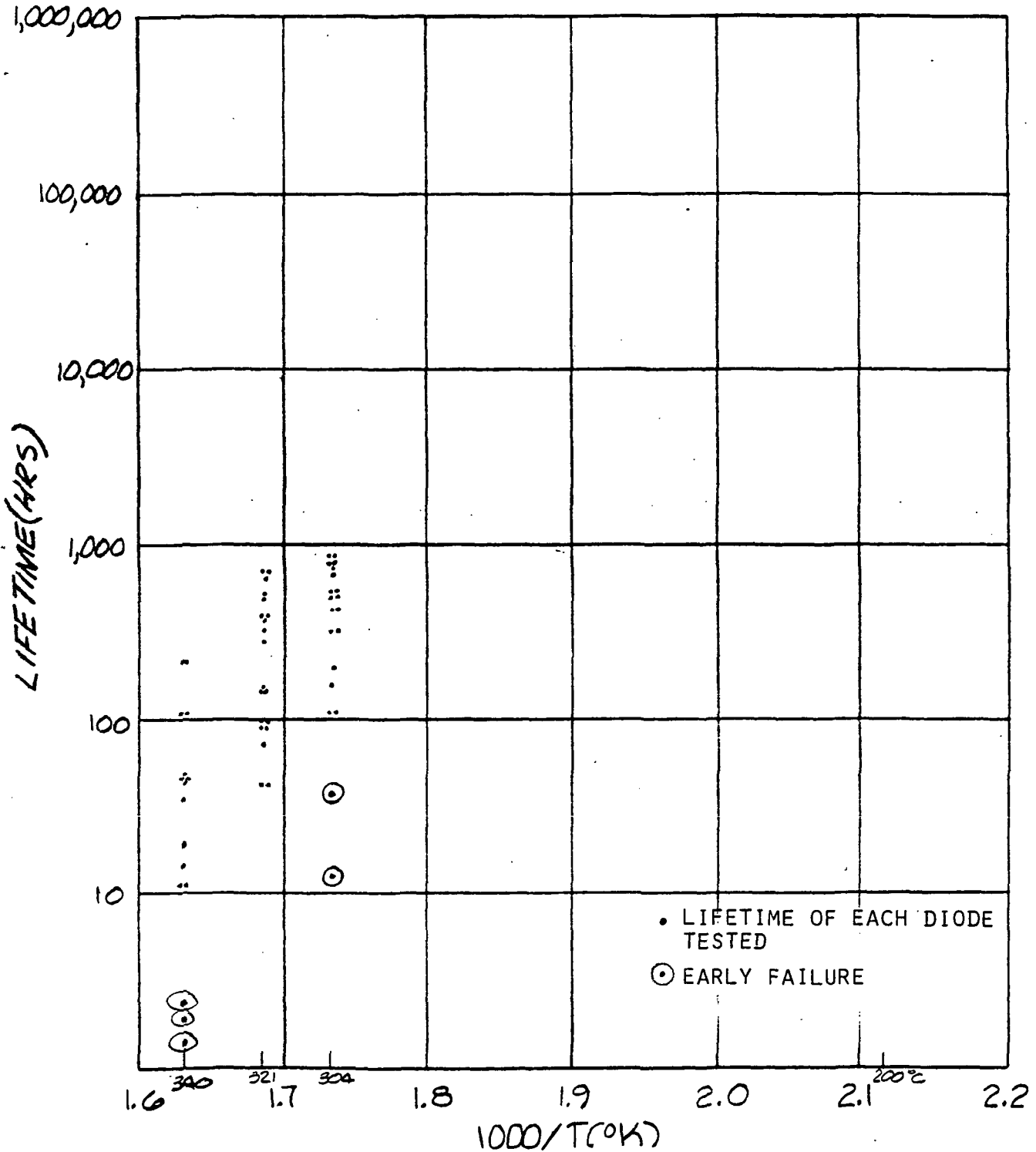


FIGURE 71.

DC ACCELERATED STRESS TEST DATA FOR  
20 GHz GROWN-JUNCTION GaAs IMPATT DIODES



EARLY FAILURES REMOVED

HIGH TEMPERATURE

( $T_H = 340^{\circ}\text{C}$ )

N=13

MID. TEMPERATURE

( $T_M = 321^{\circ}\text{C}$ )

N=20

LOW TEMPERATURE

( $T_L = 304^{\circ}\text{C}$ )

N=18

| DEVICE S/N | $T_I$ (HRS.) | DEVICE S/N | $T_I$ (HRS.) | DEVICE S/N | $T_I$ (HRS.) |
|------------|--------------|------------|--------------|------------|--------------|
| 33         | 12.8         | 25         | 46.15        | 44         | 121.2        |
| 1          | 12.9         | 18         | 46.65        | 16         | 121.45       |
| 32         | 16.05        | 27         | 72.7         | 39         | 167.2        |
| 18         | 20.3         | 21         | 94.55        | 6          | 207.35       |
| 7          | 35.2         | 22         | 94.7         | 11         | 334.5        |
| 3          | 47.75        | 35         | 103.05       | 13         | 334.6        |
| 16         | 48.6         | 34         | 106.5        | 8          | 420.8        |
| 24         | 48.85        | 28         | 158.95       | 14         | 428.0        |
| 17         | 49.0         | 50         | 161.7        | 2          | 523.1        |
| 32         | 110.2        | 48         | 167.55       | 4          | 525.35       |
| 18         | 110.65       | 55         | 275.45       | 15         | 548.85       |
| 4          | 201.75       | 33         | 334.0        | 9          | 556.5        |
| 22         | 202.0        | 41         | 369.0        | 10         | 693.2        |
|            |              | 47         | 384.4        | 1          | 740.7        |
|            |              | 42         | 389.9        | 5          | 781.15       |
|            |              | 36         | 488.7        | 52         | 781.3        |
|            |              | 31         | 533.3        | 7          | 844.15       |
|            |              | 32         | 623.7        | 19         | 844.2        |
|            |              | 30         | 695.9        |            |              |
|            |              | 37         | 696.9        |            |              |

$N_T = 51$

FIGURE 72.

# GROWN JUNCTION DIODES COMBINED LOGNORMAL PLOT



EARLY FAILURES ELIMINATED

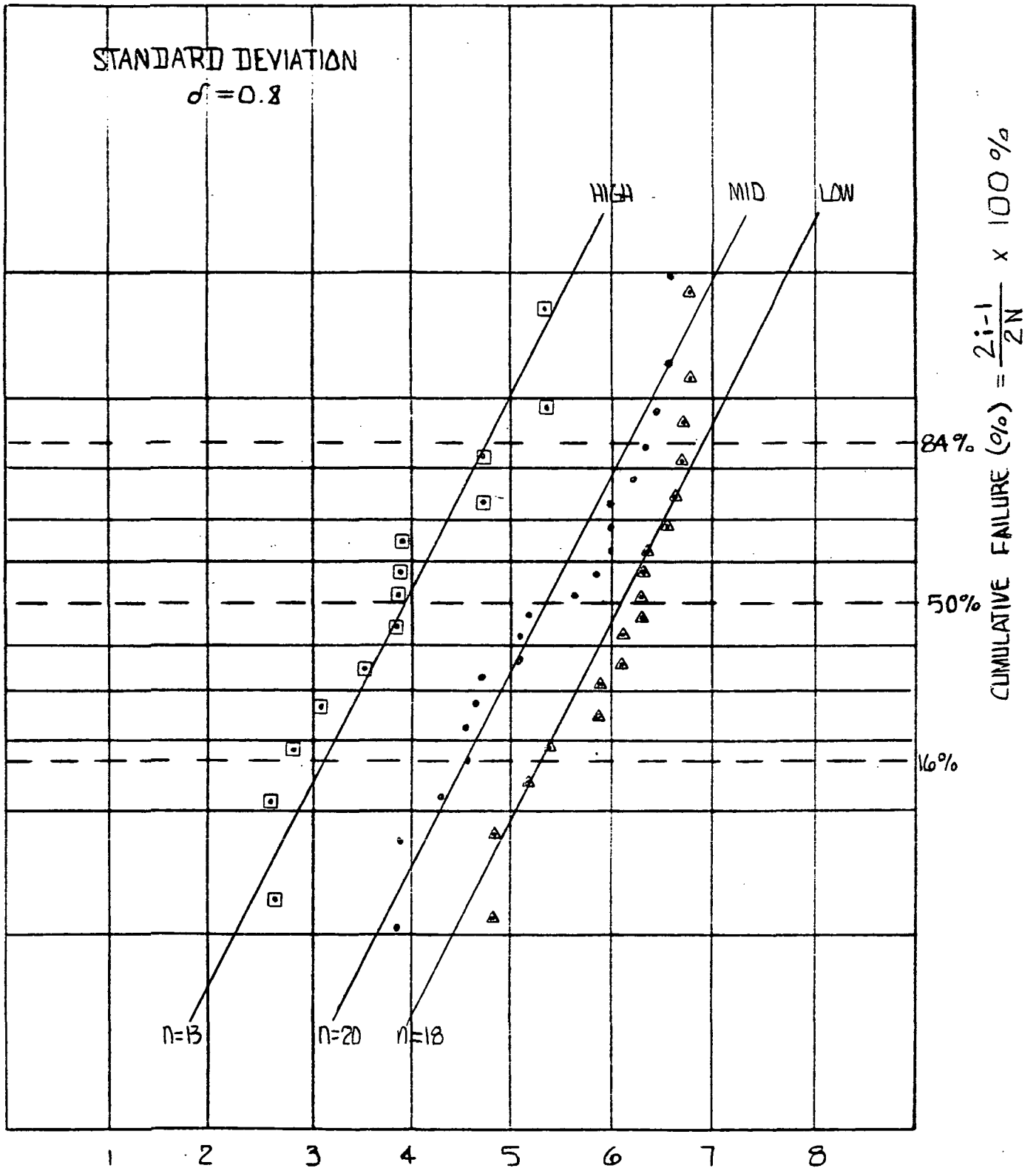


FIGURE 73.

$L_n$  (LIFETIME)

# ARRHENIUS (REGRESSION) LINE PLOT

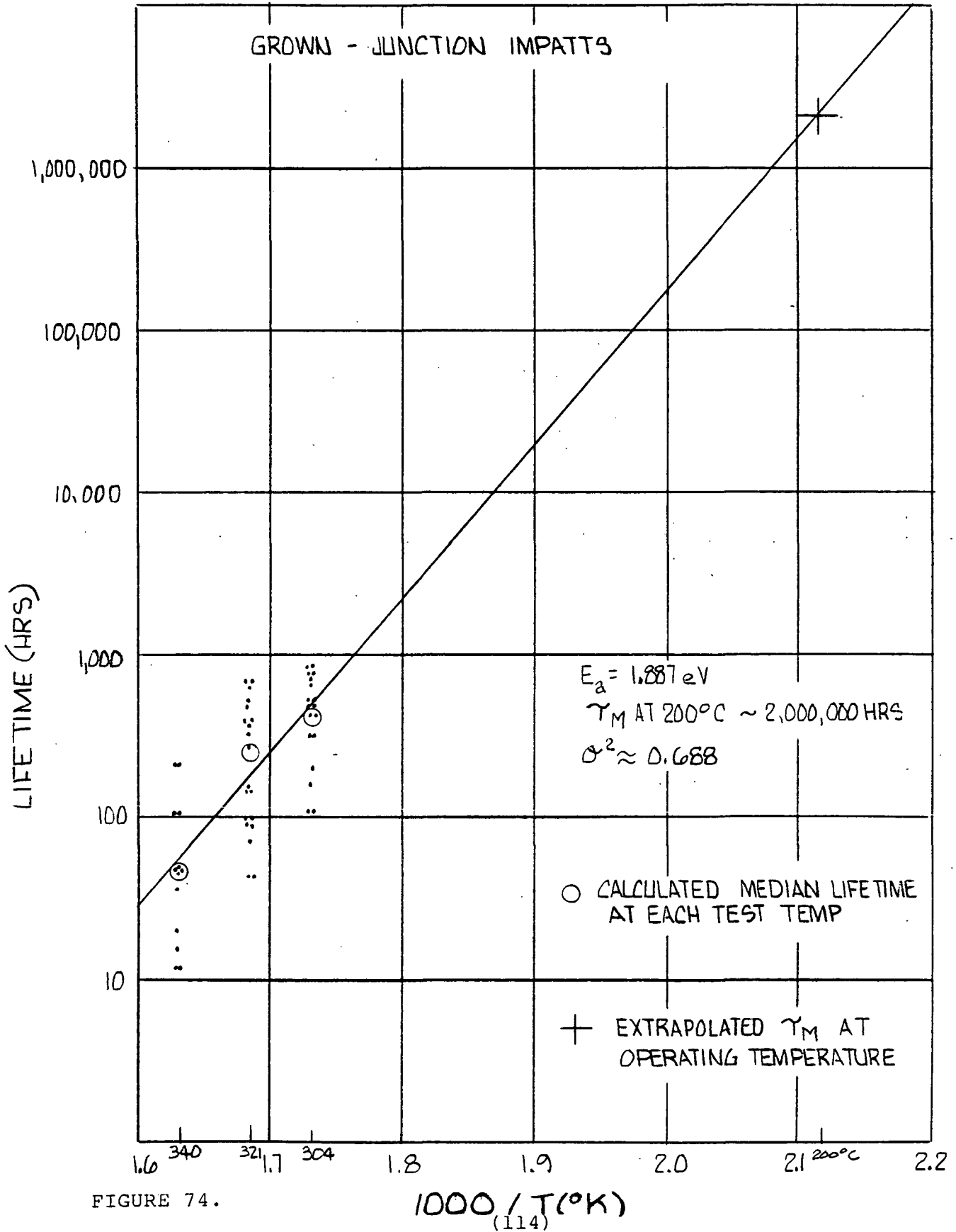


FIGURE 74.

## 2.0 Summary of Failures

A summary of failures is presented here, together with an identification of failure mode for each of the IMPATT diodes. A subsequent failure analysis will address each of the failure modes with representative illustration of the ultimate failure mechanism.

### A. High Temperature Stress Test

| <u>Failure Mode</u>   | <u>Schottky Barrier</u> | <u>Grown Junction</u> |
|-----------------------|-------------------------|-----------------------|
| Short                 | 9                       | 11                    |
| Open                  | 0                       | 1                     |
| Criteria<br>B, C or D | 11                      | 8                     |

### B. Medium Temperature Stress Test

|                      |    |    |
|----------------------|----|----|
| Short                | 6  | 5  |
| Open                 | 0  | 2  |
| Criteria<br>B,C or D | 14 | 14 |

### C. Low Temperature Stress Test

|                      |    |    |
|----------------------|----|----|
| Short                | 8  | 7  |
| Open                 | 0  | 0  |
| Criteria<br>B,C or D | 12 | 13 |

LOW TEMPERATURE STRESS TEST DATA SUMMARY



| <u>SCHOTTKY-BARRIER DIODES</u> |                             |                     | <u>GROWN JUNCTION DIODES</u> |                             |                      |
|--------------------------------|-----------------------------|---------------------|------------------------------|-----------------------------|----------------------|
| <u>DEVICE S/N</u>              | <u>T<sub>1</sub> (HRS.)</u> | <u>FAILURE MODE</u> | <u>DEVICE S/N</u>            | <u>T<sub>1</sub> (HRS.)</u> | <u>FAILURE MODE</u>  |
| 1562B                          | 29.05                       | C.                  | 3717/53                      | 13.8                        | SHORT                |
| 1565B                          | 45.65                       | D.                  | 12                           | 39.8                        | SHORT                |
| 1597G                          | 84.2                        | SHORT               | 44                           | 121.2                       | SHORT                |
| 1553B                          | 94.3                        | SHORT               | 16                           | 121.45                      | SHORT                |
| 1563B                          | 95.6                        | D.                  | 39                           | 167.2                       | D.                   |
| 1591G                          | 165.5                       | C.                  | 6                            | 207.35                      | SHORT                |
| 1582G                          | 170.5                       | SHORT               | 11                           | 334.5                       | D.                   |
| 1500B                          | 191.4                       | SHORT               | 13                           | 334.6                       | D.                   |
| 1555B                          | 191.4                       | D.                  | 8                            | 420.8                       | SHORT                |
| 1579G                          | 191.6                       | D.                  | 14                           | 428.0                       | SHORT                |
| 1588G                          | 218.8                       | SHORT               | 2                            | 523.1                       | D.                   |
| 1580G                          | 273.0                       | SHORT               | 4                            | 525.35                      | D.                   |
| 1559B                          | 285.0                       | D.                  | 15                           | 548.85                      | D.                   |
| 1586G                          | 287.35                      | D.                  | 9                            | 556.5                       | V <sub>IN</sub> TRIP |
| 1589G                          | 287.4                       | D.                  | 10                           | 693.2                       | D.                   |
| 1499B                          | 336.6                       | SHORT               | 1                            | 740.7                       | D.                   |
| 1497B                          | 356.05                      | D.                  | 5                            | 781.15                      | V <sub>IN</sub> TRIP |
| 1552B                          | 373.2                       | SHORT               | 52                           | 781.3                       | V <sub>IN</sub> TRIP |
| 1549B                          | 435.65                      | D.                  | 7                            | 844.15                      | TERMINATED*          |
| 1581G                          | 435.7                       | D.                  | 40                           | 844.2                       | TERMINATED*          |

\* POST TEST OSCILLATOR MEASUREMENTS CONFIRMED FAILURE AS THE RESULT OF LOW RF POWER OUTPUT.

FIGURE 75.



MEDIUM TEMPERATURE STRESS TEST DATA SUMMARY

| <u>SCHOTTKY BARRIER DIODES</u> |                             |                      | <u>GROMN JUNCTION DIODES</u> |                             |                      |
|--------------------------------|-----------------------------|----------------------|------------------------------|-----------------------------|----------------------|
| <u>DEVICE S/N</u>              | <u>T<sub>1</sub> (HRS.)</u> | <u>FAILURE MODE</u>  | <u>DEVICE S/N</u>            | <u>T<sub>1</sub> (HRS.)</u> | <u>FAILURE MODE</u>  |
| 1396B                          | 0                           | I <sub>IN</sub> TRIP | 3717/25                      | 46.15                       | SHORT                |
| 1429B                          | 0                           | I <sub>IN</sub> TRIP | 18                           | 46.65                       | C.                   |
| 1302B                          | 7.25                        | V <sub>IN</sub> TRIP | 27                           | 72.7                        | D.                   |
| 1397B                          | 8.55                        | D.                   | 21                           | 94.55                       | C.                   |
| 1310G                          | 44.75                       | D.                   | 22                           | 94.7                        | C.                   |
| 1382B                          | 46.1                        | C.                   | 35                           | 103.05                      | D.                   |
| 1428B                          | 60.5                        | C.                   | 34                           | 106.5                       | SHORT                |
| 1307B                          | 65.2                        | SHORT                | 28                           | 158.95                      | SHORT                |
| 1318G                          | 81.6                        | C.                   | 50                           | 161.7                       | SHORT                |
| 1303B                          | 87.7                        | SHORT                | 48                           | 167.55                      | D.                   |
| 1300B                          | 93.2                        | V <sub>IN</sub> TRIP | 55                           | 275.45                      | SHORT                |
| 1392B                          | 93.4                        | SHORT                | 33                           | 334.0                       | D.                   |
| 1301B                          | 105.2                       | SHORT                | 41                           | 369.0                       | V <sub>IN</sub> TRIP |
| 1314G                          | 114.0                       | SHORT                | 47                           | 384.4                       | OPEN                 |
| 1317G                          | 122.75                      | SHORT                | 42                           | 389.9                       | OPEN                 |
| 1430B                          | 147.2                       | V <sub>IN</sub> TRIP | 36                           | 488.7                       | D.                   |
| 1316G                          | 159.15                      | V <sub>IN</sub> TRIP | 31                           | 533.5                       | C.                   |
| 1385B                          | 189.8                       | V <sub>IN</sub> TRIP | 32                           | 623.7                       | V <sub>IN</sub> TRIP |
| 1389B                          | 243.2                       | V <sub>IN</sub> TRIP | 30                           | 695.9                       | D.                   |
| 1313G                          | 262.3                       | V <sub>IN</sub> TRIP | 37                           | 696.9                       | C.                   |

FIGURE 76.

HIGH TEMPERATURE STRESS TEST DATA SUMMARY

| SCHOTTKY BARRIER DIODES |                      |                      | GROWN JUNCTION DIODES |                      |                      |
|-------------------------|----------------------|----------------------|-----------------------|----------------------|----------------------|
| DEVICE S/N              | T <sub>1</sub> (HRS) | FAILURE MODE         | DEVICE S/N            | T <sub>1</sub> (HRS) | FAILURE MODE         |
| 1238G                   | 4.55                 | SHORT                | 3664/19               | 0                    | SHORT                |
| 1229G                   | 11.1                 | SHORT                | 3664/35               | 0                    | SHORT                |
| 1116B                   | 12.8                 | SHORT                | 3664/36               | 0                    | SHORT                |
| 680G                    | 13.6                 | SHORT                | 3705/8                | 0                    | SHORT                |
| 668G                    | 22.25                | V <sub>IN</sub> TRIP | 3664/31               | 0.5                  | SHORT                |
| 362D                    | 24.5                 | V <sub>IN</sub> TRIP | 3664/37               | 1.0                  | OPEN                 |
| 366D                    | 25.8                 | V <sub>IN</sub> TRIP | 3705/17               | 2.5                  | SHORT                |
| 685G                    | 32.8                 | V <sub>IN</sub> TRIP | 3705/33               | 12.8                 | D.                   |
| 1231G                   | 38.5                 | V <sub>IN</sub> TRIP | 3705/1                | 12.9                 | C.                   |
| 514G                    | 44.8                 | V <sub>IN</sub> TRIP | 3664/32               | 16.05                | SHORT                |
| 1188G                   | 45.6                 | SHORT                | 3664/18               | 20.3                 | D.                   |
| 1106B                   | 46.1                 | SHORT                | 3705/7                | 35.2                 | SHORT                |
| 1180G                   | 48.8                 | SHORT                | 3705/3                | 47.75                | V <sub>IN</sub> TRIP |
| 470G                    | 48.8                 | V <sub>IN</sub> TRIP | 3664/16               | 48.6                 | SHORT                |
| 1223G                   | 55.6                 | V <sub>IN</sub> TRIP | 3664/24               | 48.85                | SHORT                |
| 1220G                   | 65.8                 | SHORT                | 3664/17               | 49.0                 | V <sub>IN</sub> TRIP |
| 1254M                   | 70.7                 | V <sub>IN</sub> TRIP | 3705/32               | 110.2                | V <sub>IN</sub> TRIP |
| 1237G                   | 80.2                 | V <sub>IN</sub> TRIP | 3705/18               | 110.65               | SHORT                |
| 1264M                   | 80.7                 | V <sub>IN</sub> TRIP | 3705/4                | 201.75               | D.                   |
| 1177G                   | 147.8                | SHORT                | 3705/22               | 202.0                | D.                   |

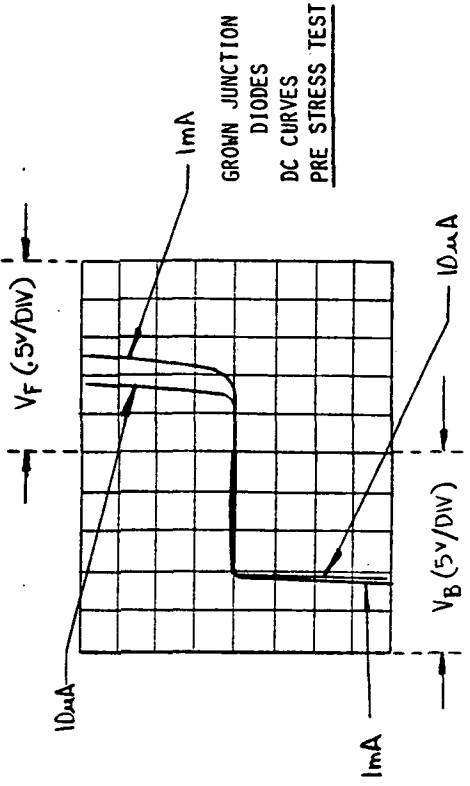
FIGURE 77.

### 3.0 Initial and Final Thermal Data

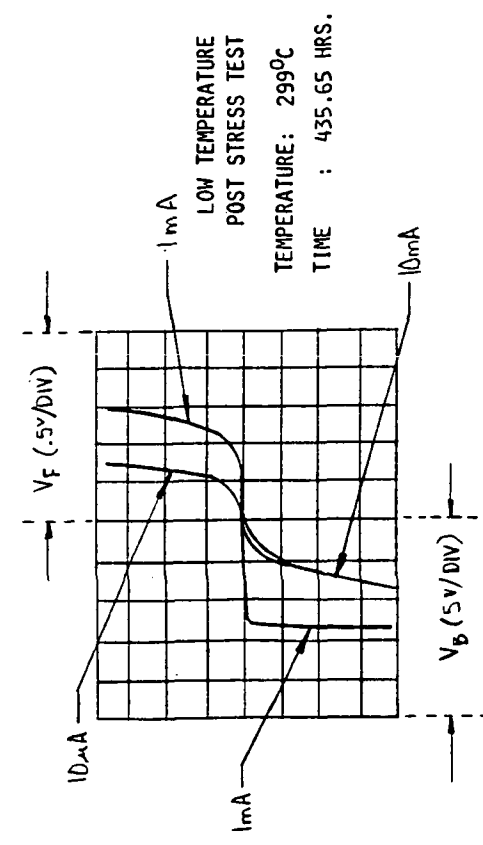
The post test thermal resistance could only be measured on diodes with good I-V characteristic, a limitation of the method used as mentioned in a previous section (II-5.0). The degradation of Schottky barrier diodes, as anticipated, is more pronounced as compared to the grown junction diodes, consequently, more post test thermal data is available.

Both types of diodes show substantial and variable increases in thermal resistance, which resulted in either very poor or no RF performance (data in section IV - 3.0, 4.0 and 5.0). Furthermore, the measured increases in thermal resistance, - and it appears safe to assume, that diodes not measured experienced identical increases in thermal resistance -, ultimately subjected the diodes to higher than scheduled junction stress temperatures. Because of limited data and randomly distributed increases in thermal resistance and junction stress temperature, these effects were not considered in the statistical analysis. The random change in thermal resistance, not measurable during stress testing, did not correlate with the random change in  $I_{in}$  and  $V_{in}$  monitored during testing.

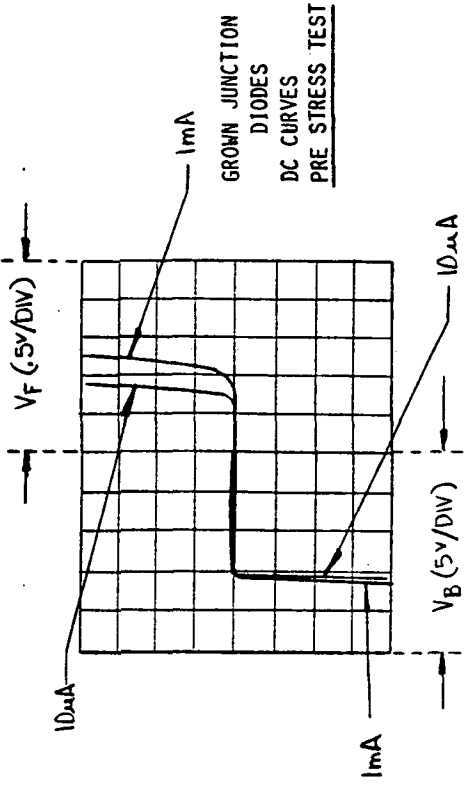
CURRENT VOLTAGE CHARACTERISTICS (I-V)  
(TYPICAL)



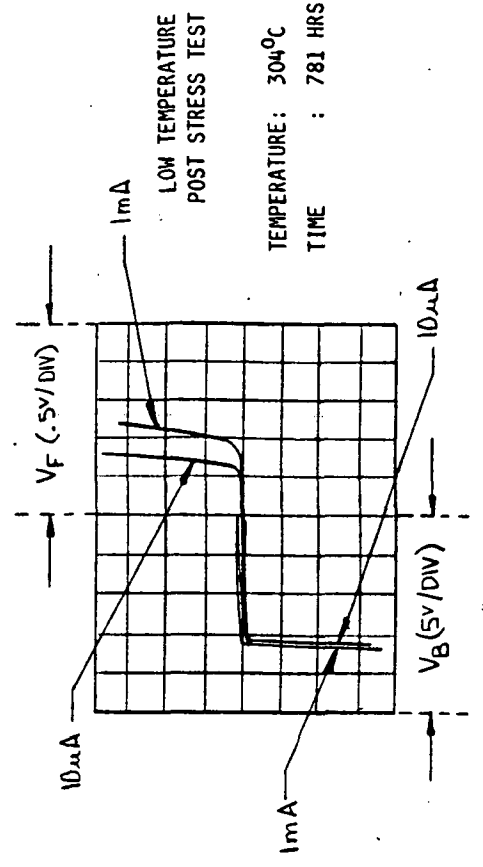
A.



B.



C.



D.

FIGURE 78 .  
D. IS NOT SUITABLE FOR THERMAL RESISTANCE MEASUREMENT

INCREASE IN JUNCTION TEST TEMPERATURE AS A  
FUNCTION OF THERMAL RESISTANCE INCREASE WITH TIME  
(GROWN JUNCTION)

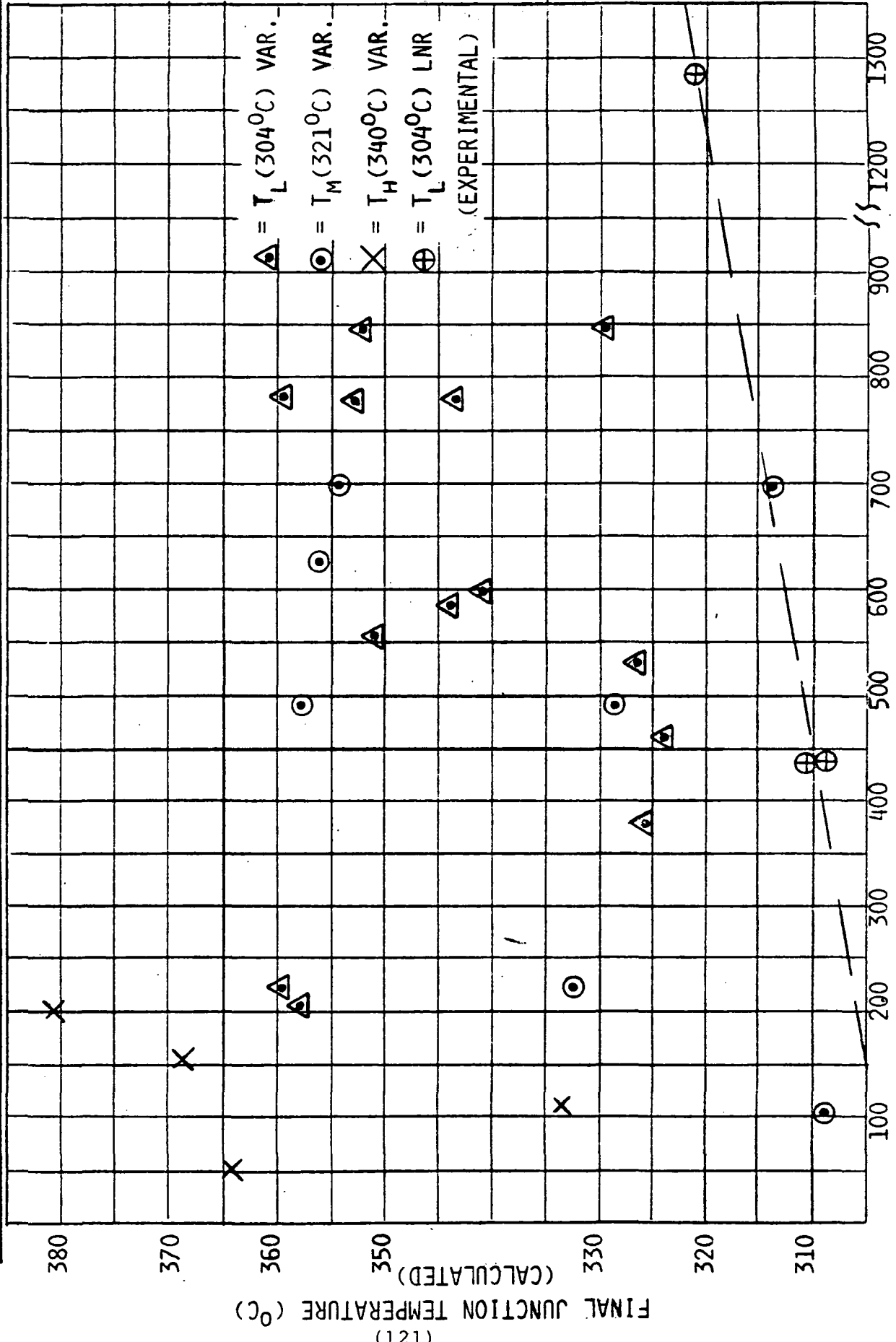
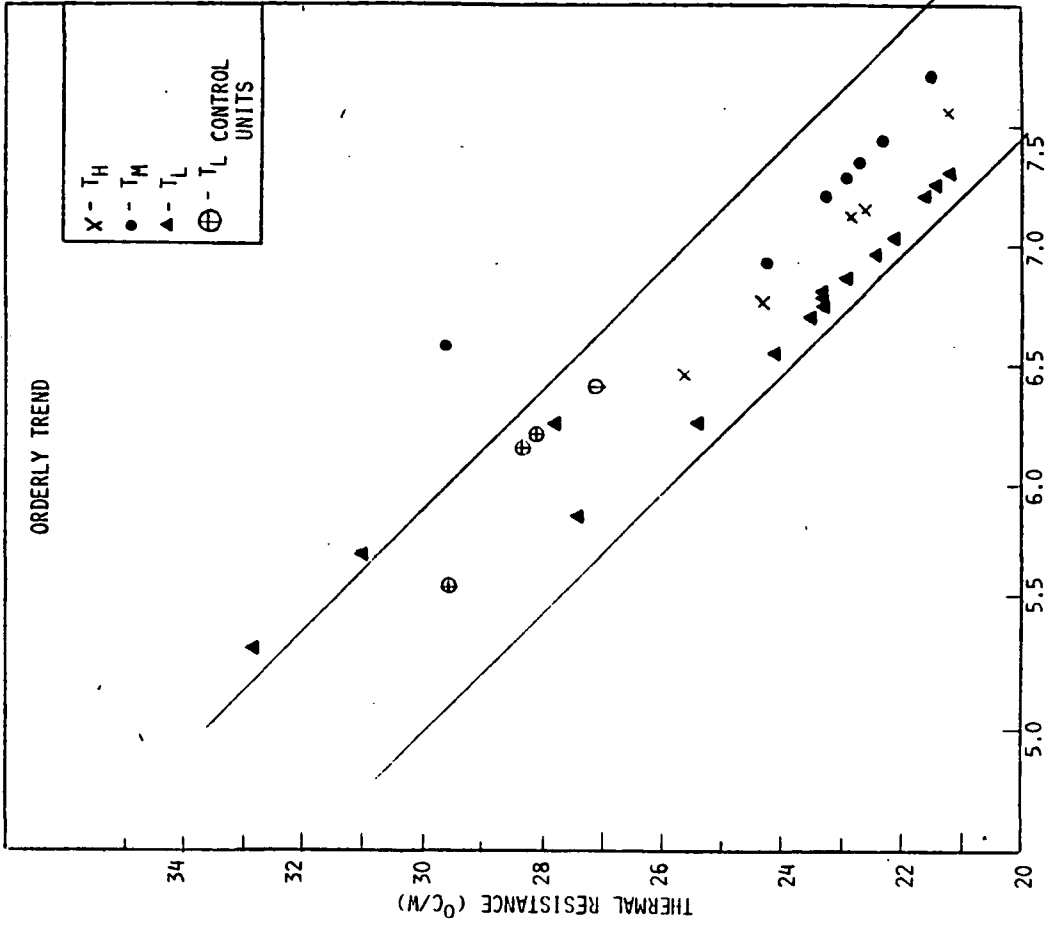
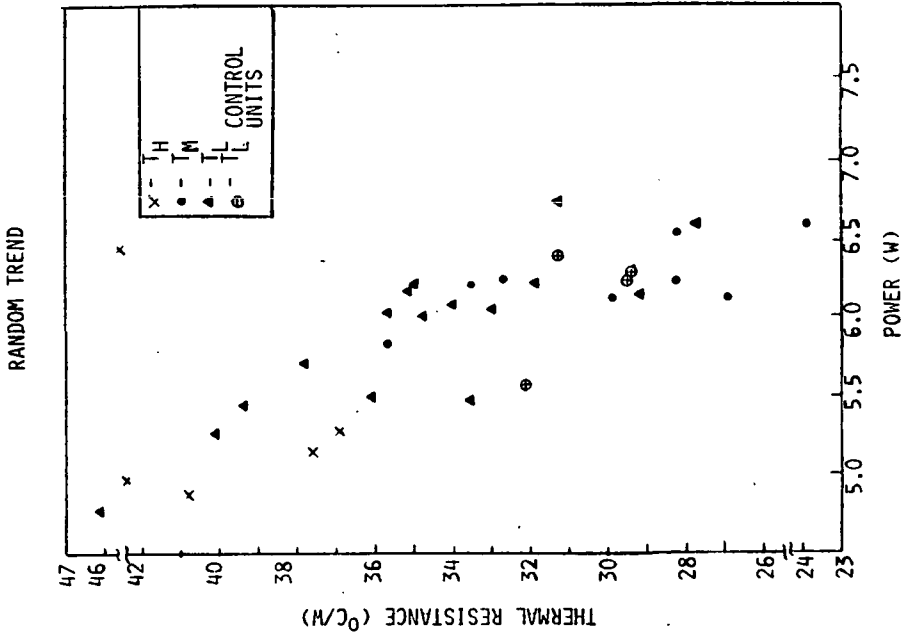


FIGURE 79.

PRE AND POST TEST RELATIONS OF  
 $\theta_{TH}$  AND  $P_{IN(DC)}$



A. PRE TEST RELATION



B. POST TEST RELATION

FIGURE 80.

SCHOTTKY BARRIER DIODES

| DIODE # | THERMAL RESISTANCE<br>( $^{\circ}\text{C/W}$ ) |       | STRESS, TEMPERATURE<br>( $^{\circ}\text{C}$ ) |       |
|---------|--|-------|---|-------|
|         | INITIAL  | FINAL | INITIAL                                       | FINAL |
| 1549B   | 31   | 37.77 | 299.2   | 338.5 |
| 1579G   | 27.8   | 35.13 | 298.8   | 341.8 |
| 1581G   | 32.8   | 39.42 | 299.1   | 336.6 |

GROWN JUNCTION DIODES

| DIODE # | THERMAL RESISTANCE<br>( $^{\circ}\text{C/W}$ ) |       | STRESS, TEMPERATURE<br>( $^{\circ}\text{C}$ ) |       |
|---------|--|-------|---|-------|
|         | INITIAL  | FINAL | INITIAL                                       | FINAL |
| 3664/17 | 22.6   | 36.9  | 339.9   | 336   |
| 3705/3  | 21.18  | 37.6  | 339.9   | 364.2 |
| 3705/17 | 25.58  | 42.5  | 340.8   | 423.4 |
| 3705/4  | 22.76  | 42.4  | 340.3   | 380.6 |
| 3705/32 | 24.26  | 40.8  | 339.6   | 368.6 |
| 3717/30 | 24.2   | 26.87 | 320.1   | 313.9 |
| 3717/32 | 22.9   | 35.66 | 320.6   | 356.2 |
| 3717/33 | 22.7   | 33.54 | 321   | 357.7 |
| 3717/35 | 21.5   | 23.9  | 321.1   | 309.1 |
| 3717/36 | 22.3   | 28.23 | 320.4   | 328.7 |
| 3717/37 | 23.2   | 32.7  | 320.8   | 354.4 |
| 3717/48 | 22.7   | 29.9  | 320.7   | 332.5 |
| 3717/2  | 21.4   | 35    | 304.2   | 362.6 |
| 3717/4  | 21.6   | 33    | 304.3   | 343.9 |
| 3717/5  | 23.3   | 35.7  | 304   | 359.4 |
| 3717/6  | 25.4   | 31.3  | 304   | 357.8 |
| 3717/7  | 23.3   | 27.7  | 305   | 329.5 |
| 3717/9  | 22.4   | 34    | 303.7   | 351   |
| 3717/10 | 22.1   | 34.8  | 303.5   | 352.8 |
| 3717/11 | 21.2   | 29.2  | 304   | 324.2 |
| 3717/13 | 23.5   | 33.6  | 304   | 325.7 |
| 3717/15 | 24.1   | 36.1  | 303.8   | 341   |
| 3717/39 | 23.3   | 46.1  | 304.5   | 359.5 |
| 3717/40 | 27.4   | 40.1  | 304.3   | 352.4 |
| 3717/52 | 22.9   | 31.9  | 304.5   | 343.7 |

FIGURE 81.

#### 4.0 Failure Mechanism and Analysis

##### 4.1 Thermal/Electrical Stress Effects on GaAs Doping Profile

Reconstruction of both the L-H-L Schottky barrier and H-L grown junction profiles before and following accelerated stress testing revealed no significant profile changes. Thus, it can be concluded that none of the observed device failures are related to the insignificant changes of the GaAs doping profiles.



SCHOTTKY BARRIER AND GROWN JUNCTION DOPING PROFILE SUMMARY  
(TYPICAL)

DATA VIA C-V MEASUREMENTS

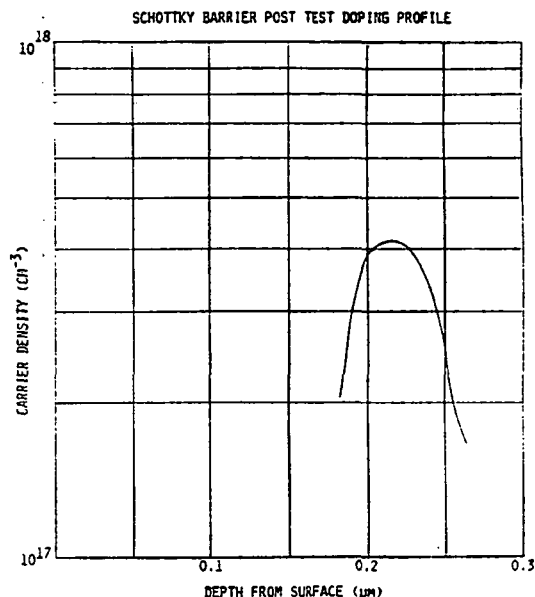
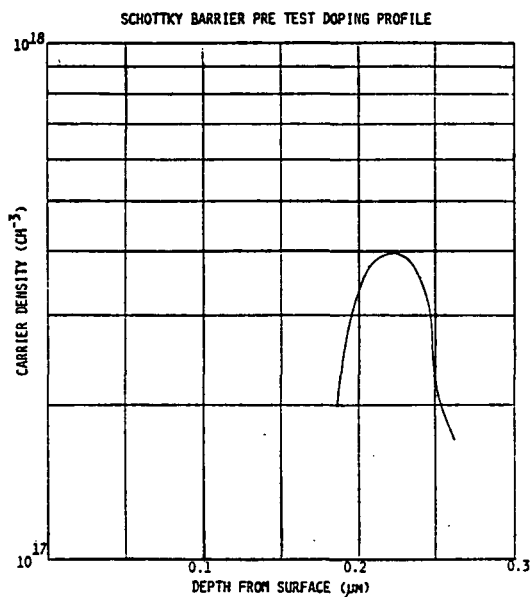
|  | SCHOTTKY BARRIER    |                         | GROWN JUNCTION     |                         |
|--|---------------------|-------------------------|--------------------|-------------------------|
|  | PRE-TEST            | POST TEST               | PRE TEST           | POST TEST               |
| ● DISTANCE OF SURFACE TO CRITICAL HIGH DOPANT REGION ( $\mu\text{M}$ ) | 0.220               | 0.215                   | 0.35               | 0.34                    |
| ● CARRIER CONCENTRATION $\text{CM}^{-3}$                               | 4E17                | 4.2E17                  | 9.2E17             | 9E17                    |
| ● NET CHANGE   | 0.005 $\mu\text{M}$ | 0.2E17 $\text{CM}^{-3}$ | 0.01 $\mu\text{M}$ | 0.2E17 $\text{CM}^{-3}$ |
| ● TEST TEMPERATURE ( $^{\circ}\text{C}$ )                              | 299                 |                         |                    | 304                     |
| ● TEST TIME (HRS)  | 436                 |                         |                    | 781                     |

● OBSERVATION: THE NOTED PROFILE CHANGES ARE NOT SIGNIFICANT IN FIGURING IN THE DEVICE FAILURES.

# DOPING PROFILE RECONSTRUCTION (USING C-V DATA)

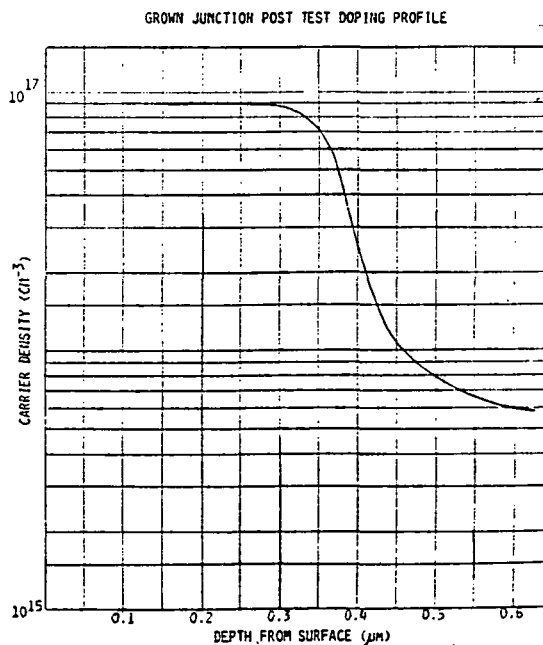
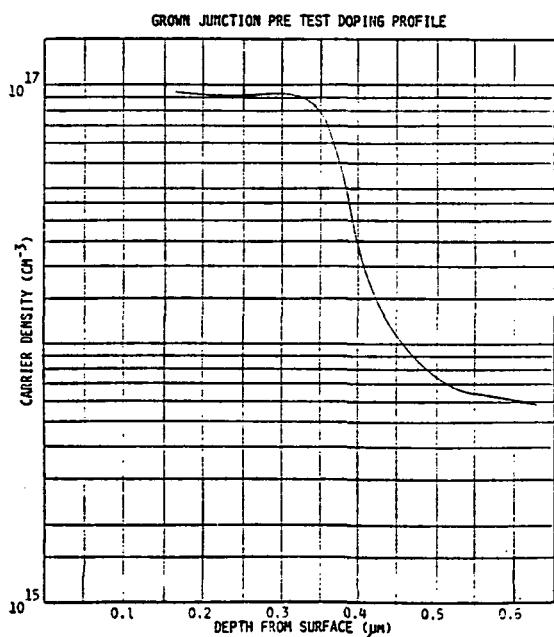


## L-H-L PROFILE



CONDITIONS:  
TEST TEMPERATURE (°C): 299  
TEST TIME (HRS): 435.65

## H-L PROFILE



CONDITIONS:  
TEST TEMPERATURE (°C): 304  
TEST TIME (HRS.): 781.05

FIGURE 83.

#### 4.2 Open Circuit Failures

Out of all the diodes stress tested only three diodes failed due to an electrically open circuit. The three failed diodes are grown junction diodes procured from Varian Associates.

After removal from the test fixture, the diodes were electrically checked to confirm the open circuit failure (standard procedure for all tested diodes). External examination did not indicate any reasons for the failure. To examine the internal cavity the devices were carefully delidded. Microscopic viewing of the ribbon bonds to the IMPATT chip showed very shallow nearly undetectable thermo compression imprints. Subsequent attempts to move the contacting ribbon were successful. The ribbons of all three diodes were not bonded to the chips, causing the open circuit conditions.

Probing of the IMPATT chips indicated good I-V characteristics, which indicates an operational IMPATT device.

Therefore, improved bonding procedures, in conjunction with precap inspection and thermal cycling as per Mil-standards can eliminate these types of failures.

The following documentation of the external and internal visual inspection is representative of the type of examination all diodes were subjected to after accelerated aging.

EXTERNAL VISUAL INSTPECTION OF FAILED IMPATT  
DIODE

DIODE NO.: VSK9250AD Lot: 3664 S/N 37

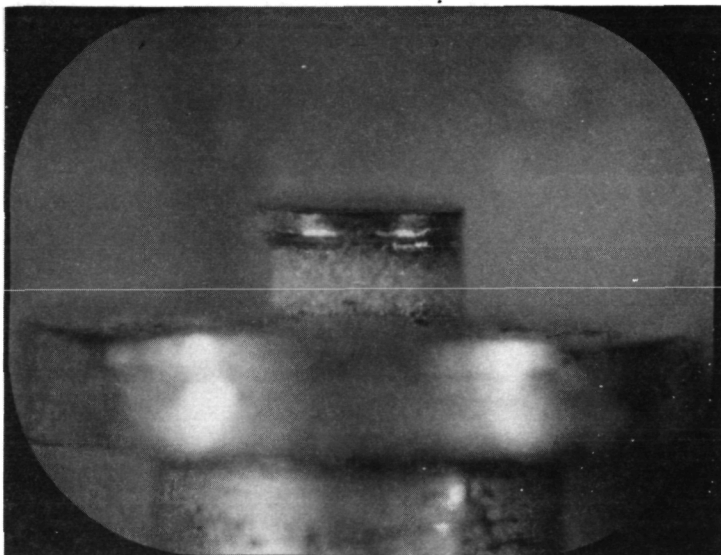
TEST TIME: One Hour

FAILURE MODE: Electrically Open

OBSERVATIONS



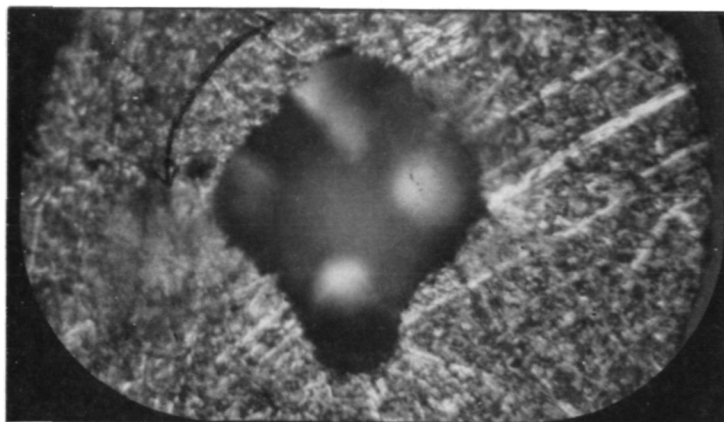
- No discolorations on package.
- Visible diode identification.
- Top of package shows impressions caused during oscillator measurement.



- Complete solder flow between cap and package.
- Cap is slightly off center.

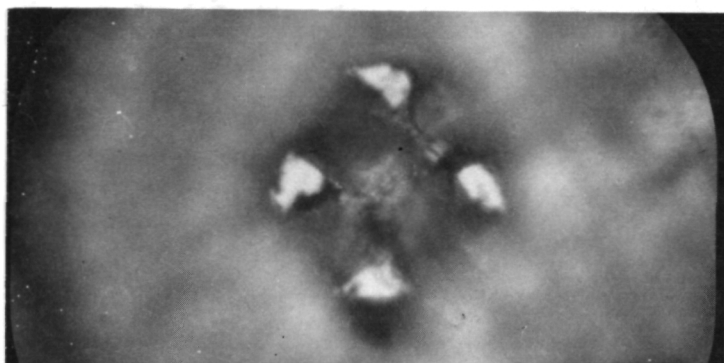
INTERNAL VISUAL INSPECTION OF FAILED  
IMPATT DIODE

DIODE NO.: VSK9250AD Lot: 3664 S/N 37  
TEST TIME: One Hour  
FAILURE MODE: Electrically Open

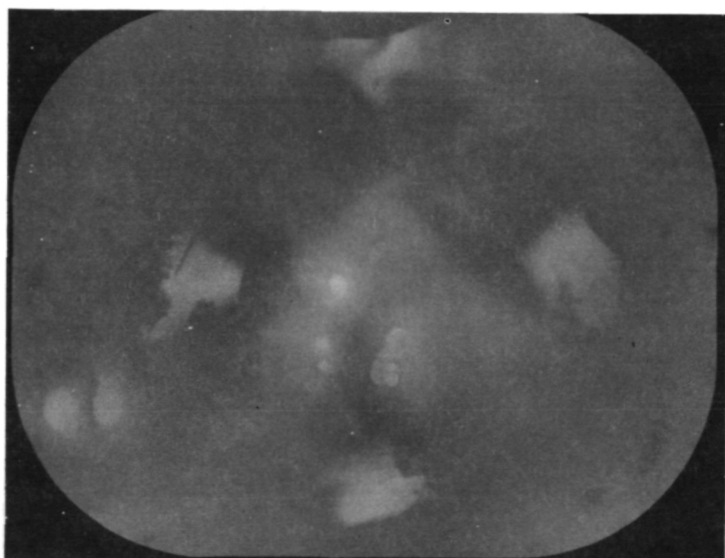


OBSERVATIONS

- Partially delidded, Au/Sn solder is shown in cavity.



- Fully delidded, top ribbon of the cross ribbon used shows centered wedge shape bond impression.

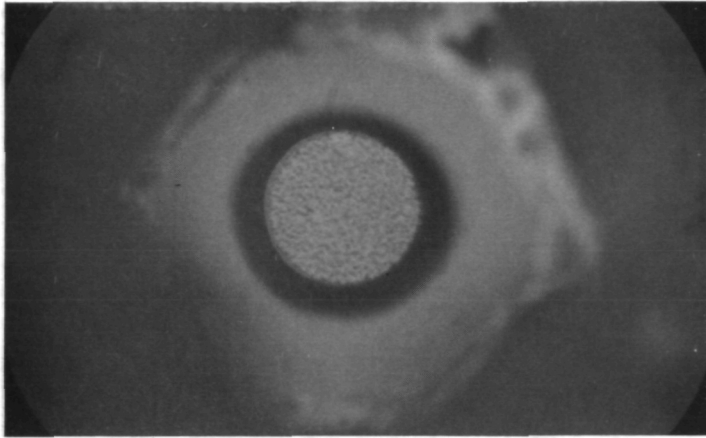


- Flaky or curled up metal visible, introduced during delidding.

INTERNAL VISUAL-INSPECTION OF FAILED  
IMPATT DIODE

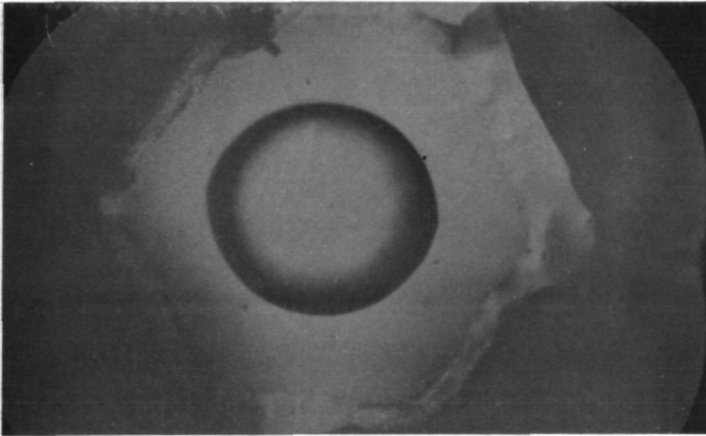
**LNR**  
COMMUNICATIONS

DIODE NO.: VSK9250AD Lot 3664 S/N 37  
TEST TIME: One Hour  
FAILURE MODE: Electrically Open

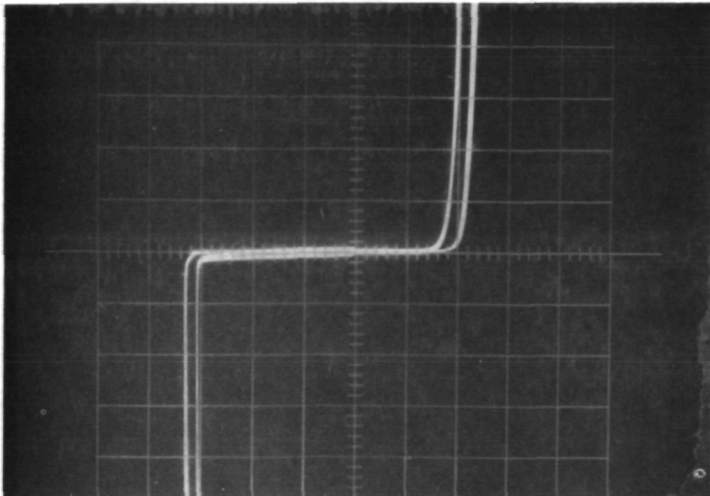


OBSERVATIONS

- With ribbons easily removed, no thermo-compression foot print is visible on Au/Ge contact pad.



- Smooth barrier metal outlines pre-etch chip area.
- GaAs is evenly etched.
- Excessive, unattached and wrinkled barrier metal extending beyond the heatsink.



- Direct contact to contact pad shows good I-V characteristic.
- Failure due to poor ribbon to chip bond.

SCALE: Vertical 10 $\mu$ A/Div.  
1mA/Div.

5V/Div.  
0.5V/Div.

FIGURE 86.

### 4.3 Short Circuit Failures

All electrically shorted device failures, twenty three Schottky barrier and twenty three grown junction diodes (revised from previously reported short circuit failures, November 1983), were physically examined externally and internally following delidding. Prior to delidding, the diodes were confirmed as electrical shorts, which did not change after the ribbons were removed and the chips checked directly.

Microscopic examination clearly grouped the two types of diodes. Specifically, the Schottky barrier diodes did not visually indicate any reason for shorting. Conversely, every grown junction diode showed a discolored burn area, the obvious location where the electrical short occurred. Further study of the failures revealed and was confirmed via SEM-analysis a singular failure mechanism of the Schottky barrier diodes and two failure mechanisms relating to the grown junction diodes.

It is apparent from the photos of the SEM-analysis, that the Schottky barrier failures are either surface and/or semiconductor material related, whereby the grown junction failures clearly indicate flaws introduced by chip processing and/or device fabrication.

#### A. SEM Analysis of Schottky Barrier Diodes

The SEM analysis of the Schottky barrier IMPATT diode shown here, is representative of all the electrically shorted Schottky barrier diodes.

Following the aforementioned external and internal inspections and with no burn marks visible, it was decided not to cross section the device. Instead, the analysis proceeded by chemically etching the GaAs chip from the substrate side towards the active

region in discrete steps allowing the detection of any potential causes of the short circuit failure relating either to the substrate active region or metal to semiconductor interface.

The first observation of a crystal defect appeared after etching for two minutes (photo a.). In addition, in the photo the partial removal of the GaAs reveals the smooth barrier metal (Pt) covered by the GaAs during stress testing. The distinct orange peel effect seen outside this area is addressed in detail in a later section. The wrinkled exposed barrier surface has been observed on every diode.

Close up examination of the suspect crystal defect via Scanning Electron Microscope (SEM) shows a highly reflective center of the obviously damaged area. (Photo b.) The high reflectivity of the area can generally be identified with high conductivity.

Continuous etching revealed a strangely shaped mesa or spike, roughly 3.75 microns high (Photo C.). The mesa height penetrated the active and drift region, causing the electrical short. The X-Ray spectrum analysis of the mesa identified only barrier surface elements, eliminating electromigration of the ohmic substrate contact.

Every shorted Schottky barrier diode indicated an identical failure mechanism.

The most probable cause, among numerous possibilities for this type of failure mechanism, is a surface or near surface crystal defect or epitaxial growth imperfection resulting in very high localized heating or 'hot spot', thus, accelerating electromigration of the barrier surface metal structure. Not to be ruled out is the development of a hot spot due to compositional reaction of the Au/Sn bonding material.

Review of the pre test DC data identified these diodes with a somewhat unstable forward and reverse breakdown voltage at high current levels ( $\geq 50\text{ma}$ ). Also, the leakage current was consistently higher than diodes which did not short during stress testing.



Consequently, this type of failure can be eliminated by limiting the range of acceptable device leakage current and observing the voltage breakdown behavior during a brief electrical stressing, which follows an effective high temperature reverse bias burn-in.

# SEM ANALYSIS OF IMPATT DIODE

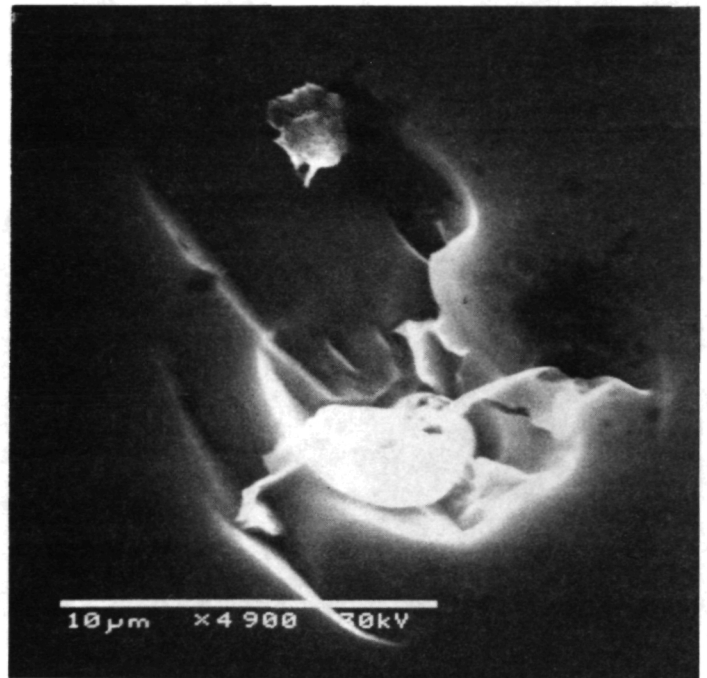
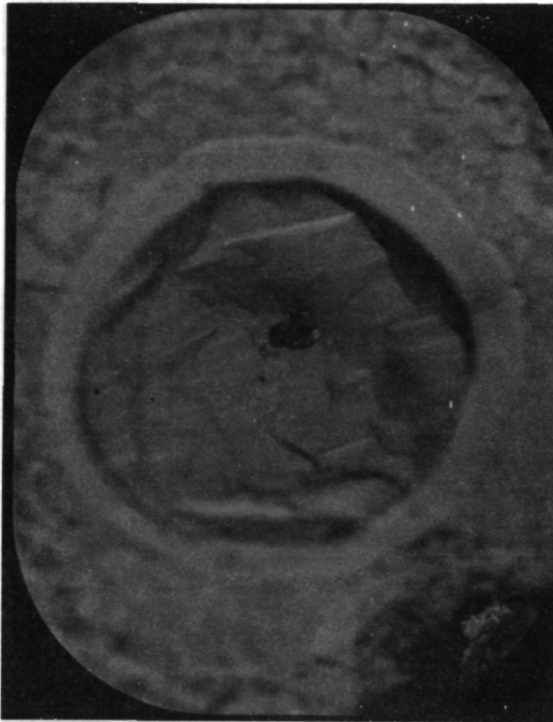
DIODE NO.: 1317G

STRESS TEST TEMPERATURE: 321°C

TEST TIME: 122.75hrs.

ASSEMBLY FABRICATION: LNR Schottky-  
Barrier Au/Sn  
Solder Bonded

FAILURE MODE: Electrical Short



a) (400X)

b)

- a) Top view of an opened IMPATT diode with the ohmic contact and ribbon removed shows suspect area of electrical short following 120 seconds of chemical etching.
- b) Close up view of suspect area clearly shows crystal damage. Light area is indicative of conductive material.

# SEM ANALYSIS OF IMPATT DIODE

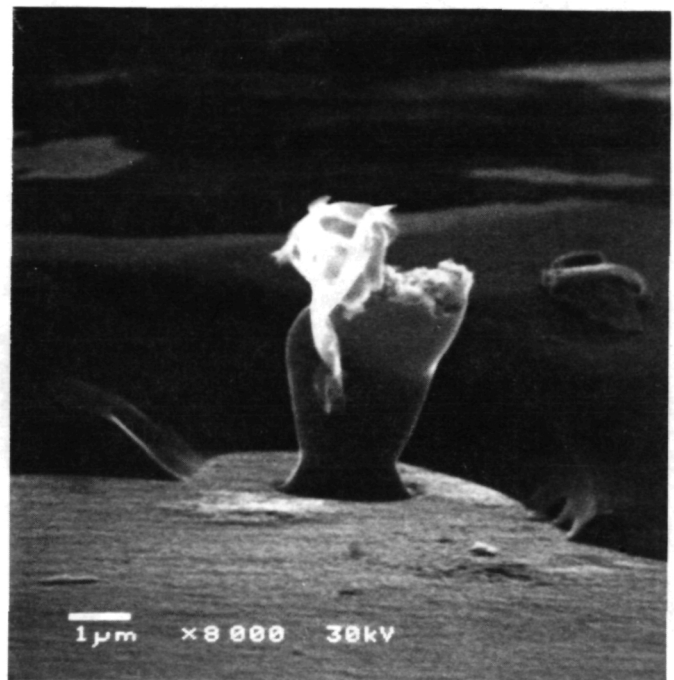
DIODE NO.: 1317G

STRESS TEST TEMPERATURE: 321°C

TEST TIME: 122.75hrs.

ASSEMBLY FABRICATION: LNR Schottky-Barrier Au/Sn Solder Bonded

FAILURE MODE: Electrical Short



- c) SEM photographs give the indication that the obstruction is possibly erupting up from the Pt. barrier metal. Continuous etching of suspect area left an  $\sim 3.75 \mu\text{m}$  high mesa. X-Ray spectrum analysis of the mesa confirms electromigration of barrier metal structure.

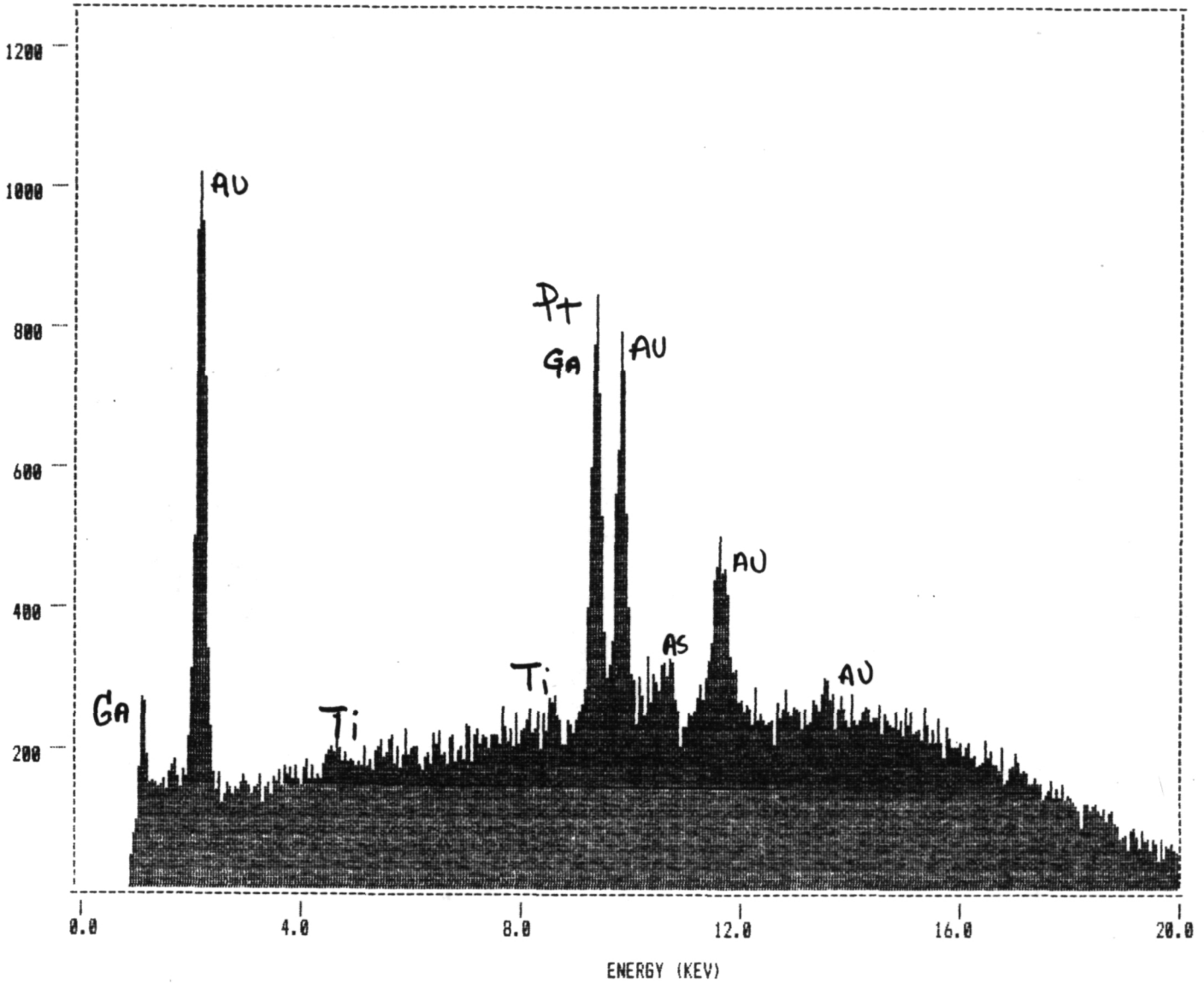
1317G

SPECTRUM LABEL



SPECTRUM FILE NAME

■ LNR1



⊗ PIGITI

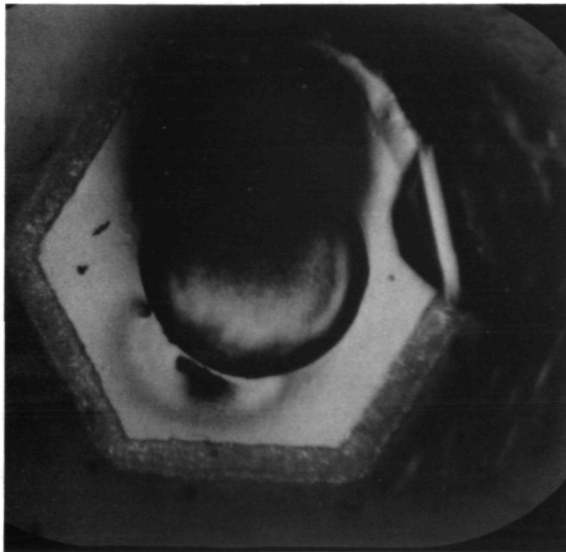
Multiple peaks are indicative of the different energy levels associated with the various elements found in the mesa like structure.

## B. SEM Analysis of Grown Junction Failures

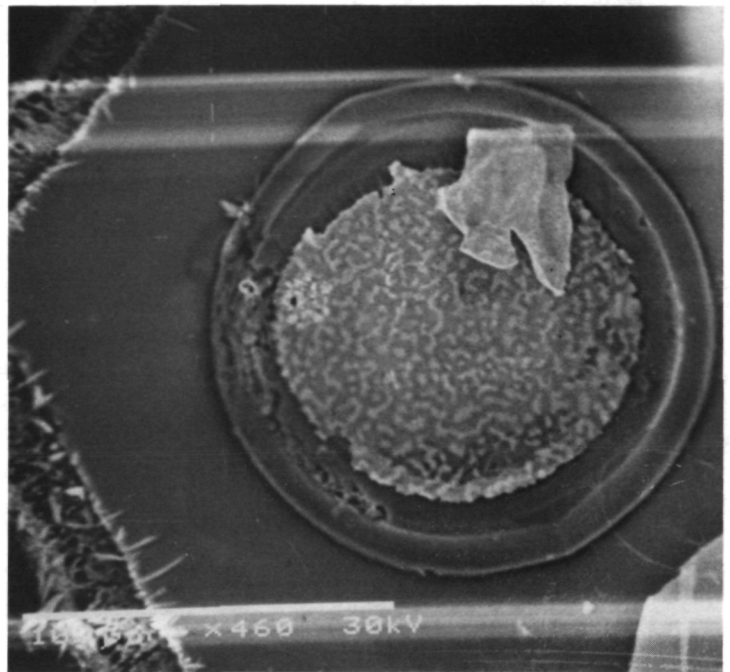
Every shorted grown junction diode was identified with one of the herein described failure mechanisms, which is related to either chip processing or device assembly. Internal visual inspection showed discoloration due to excessive heat on every diode (Photo a.) examined.

The type of failure mechanism shown in Photo C. clearly demonstrates some form of eruption of the barrier metal (Pt.) bridging the active area, causing the diode to short. Excessive and instantaneous heat melted the GaAs and ohmic metallization. It is conceivable, that entrapped gas and/or fluid during the electroplating of the heatsink was superheated, resulting in the blister formation.

Refinement of the plating process would be a first step towards eliminating this failure mechanism.

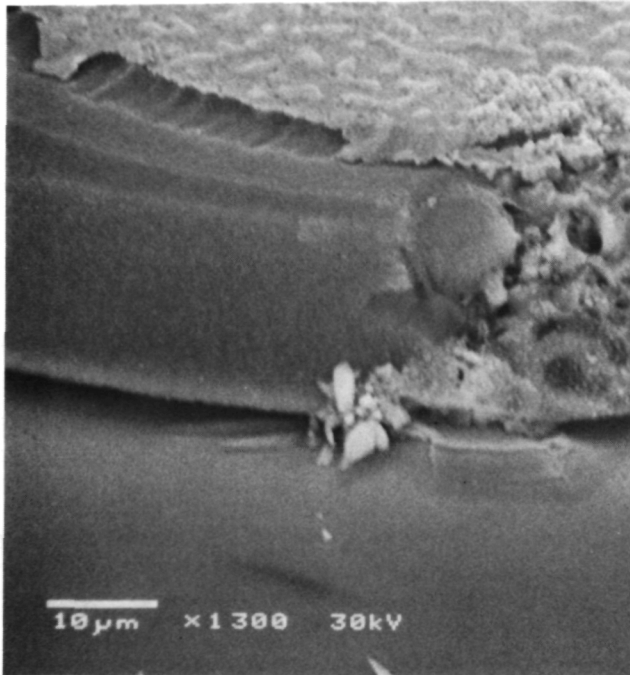
DIODE NO.: S/N 50TEST TIME: 102.9hrs.FAILURE MODE: Electrical ShortSTRESS TEST TEMPERATURE: 321°CASSEMBLY FABRICATION: Varian Grown-  
Junction Au/Sn  
Solder Bonded  
Chip T.C. Bonded  
Ribbon

a) (200X)

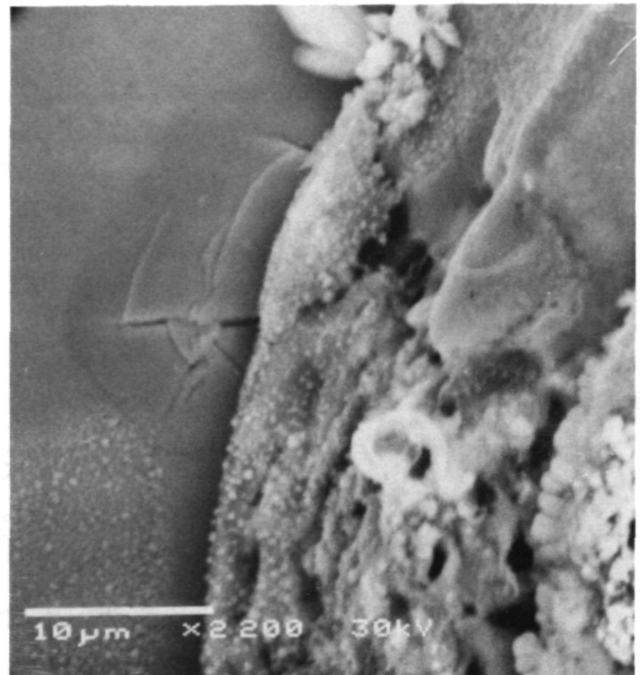


b)

- a) Shown is the hexagon heatsink with the GaAs chip centrally located. Just below the GaAs chip the discolored suspect burn area is visible.
- b) Extensive damage on the substrate surface near the ohmic contact in the upper left corner is apparently due to electric arcing.

DIODE NO.: S/N 50STRESS TEST TEMPERATURE: 321°CTEST TIME: 102.9hrs.ASSEMBLY FABRICATION: : Varian Grown  
Junction Au/Sn  
Solder Bonded  
Chip T.C. Bonded  
RibbonFAILURE MODE: Electrical Short

c)



d)

C) High magnification of the damaged area shows a mesa or blister formation of the Pt. metal bridging the active layer (dark region) causing the electrical short.

d) Close up view shows actual rupture of the platinum.

The second type of failure mechanism identified with the shorted grown junction diodes is mechanical damage to the GaAs apparently introduced while soldering the IMPATT chip into the diode package or during thermo compression bonding the ribbons to the substrate side of the chip. From photo a. it appears as if the IMPATT chip is cracked, however, further investigation and chemically etching the chip as described previously did not reveal any evidence of cracking through the center of the chip connecting the two damaged areas. However, it was established that the direction of the contact ribbon was in line with these damaged areas. The X-Ray photo of the internal cavity of the above diode does not indicate any abnormality of the ribbon shape or position.



# SEM ANALYSIS OF IMPATT DIODE

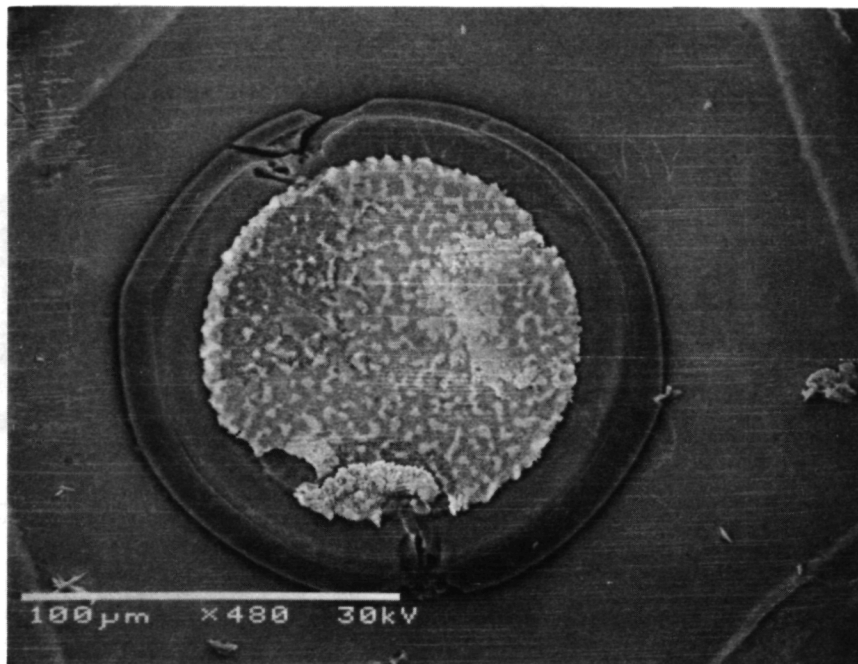
DIODE NO.: S/N 27

STRESS TEST TEMPERATURE: 321°C

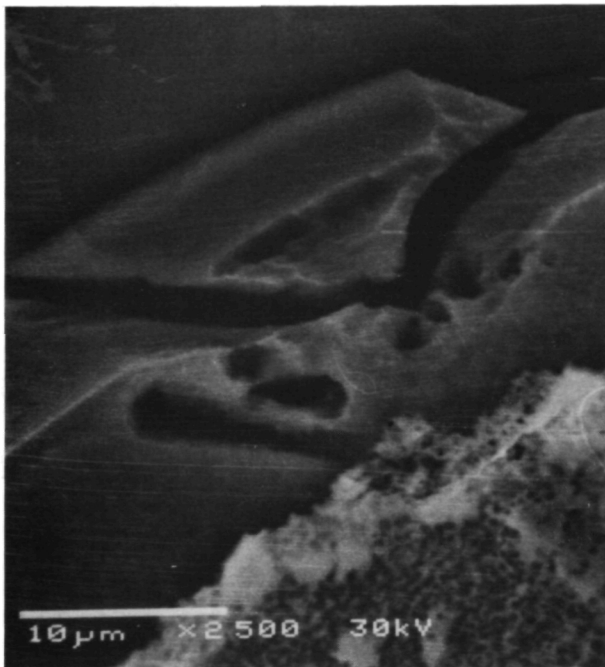
TEST TIME: 80.85hrs.

ASSEMBLY FABRICATION : Varian Grown-  
Junction Au/Sn  
Solder Bonded  
Chip T.C.  
Bonded Ribbon

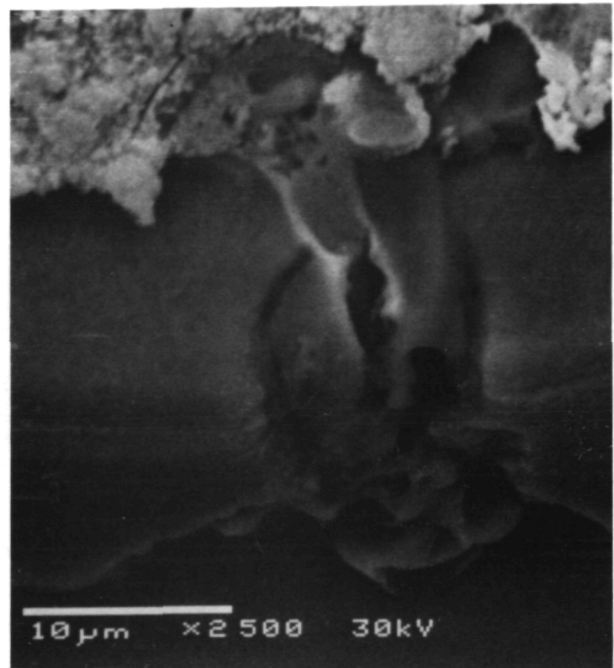
FAILURE MODE: Electrical Short



- a) Top view of the IMPATT diode shows the GaAs chip on top of the Pt and subsequent metal structure. Centered on the rounded GaAs chip is the Au/Ge ohmic contact to which the ribbon was bonded. Damaged areas on the outer edges of the GaAs are suspected to be device assembly related. Electromigration of the contact metal along the damaged area ultimately caused the device to electrically fail. Detached particles were introduced during the failure analysis.

DIODE NO.: S/N 27STRESS TEST TEMPERATURE: 321°CTEST TIME: 80.85 hrs.ASSEMBLY FABRICATION : Varian Grown-  
Junction Au/Sn  
Solder Bonded  
Chip T.C.  
Bonded RibbonFAILURE MODE: Electrical Short

b)



c)

- b) High magnification of the cracked area allows a partial view of the smooth active layer. Also very visible is the Pt. contact metal in the upper left side of the photo.
- c) High magnification of the second damaged area exhibits electromigration from the Ohmic contact, through the GaAs substrate to the Pt. metal contact. Note the extensive damage to the GaAs as the result of localized heating.

#### 4.4 Failure due to Degradation

Both types of diodes (summary of failures) exhibited the greatest percentage of failures as the result of degradation. The degradation appears to be quite random, whereby the monitored parameters did not establish a clear trend and did not reoccur as identical changes during the various stress test conditions. However, those diodes which retained good I-V characteristics to enable post stress test thermal resistance measurements clearly showed, a substantial increase in thermal resistance on nearly all diodes. Thus, the dominant changes in thermal resistnace caused substantial increases in junction temperature during stress testing (junction temperature vs time) and conceivably activated premature failure modes, obscuring lesser potential failure modes and parametric trends.

Expermental results established the Au/Sn solder bond (interface) thermally and electrically unstable. The exact physics of this thermal instability is not known at this time and requires further investigation. Experimental diodes on the other hand, with the chip to package solder bond replaced by a thermo compression bond, demonstrated substantial improvements in the thermal stability, trends and lifetimes (nearly twice that of Au/Sn bonded diodes).

In most cases, degradation of IMPATT diodes will ultimately result in electrical shorts. The slow changes observed during stress testing with this type of failure mode could be attributed to many different mechanisms. However, in general these mechanism are usually identified with reactions or diffusions between both the barrier and ohmic metals and the GaAs. Moreover, the process is well understood and new techniques developed to optimize the metallization of GaAs IMPATT material have demonstrated superior thermal and electrical stability. Experiments, carried

out at LNR have confirmed the outstanding results reported.<sup>(3)</sup>

The failure analysis of degradation failures substantiated experimental findings and observations during the reliability assessment study. Two major observations, changes on the surface of the barrier metal and substantial thermal resistance increase have been related to compositional changes of the  $\text{Au}_{80}/\text{Sn}_{20}$  solder bonds used for the assembly of the IMPATT diodes.

#### A. Experimental Results

Specific experiments addressing degradation as a function of:

- thermal
- electrical
- thermal electrical

effects on IMPATT chips and diodes fabricated in one case with the eutectic Au/Sn solder and the other case with TC-bonding, established, without any doubt, the superior thermal and electrical stability of TC bonded devices. In all experimental cases grown junction diodes were used (fabricated at LNR).

High temperature storage of IMPATT diodes at temperatures ranging from  $150^{\circ}\text{C}$  to  $270^{\circ}\text{C}$  demonstrated initial degradation of RF-power output and thermal resistance at package temperatures as low as  $180^{\circ}\text{C}$ . This information was used in limiting the maximum base plate temperature during stress testing to  $150^{\circ}\text{C}$ . Furthermore, minute changes in the surface topology of exposed Schottky barrier metallization not covered by the GaAs were observed at  $200^{\circ}\text{C}$ .

Subjecting the experimental 20 GHz GaAs IMPATT diodes to RF pulse stressing, the results again clearly established the TC bonded devices as superior devices.

| <u>BOND</u> | <u>PULSE WIDTH</u>    |
|-------------|-----------------------|
| Au/Sn       | 4 microseconds max.   |
| TC          | >10 microseconds max. |

The magnitude of the input current and voltages were identical.

Finally the results of brief RF stressing (C.W.) shown here, again verify the thermal and electrical stability of the TC bonded diodes.

By keeping the junction temperature the same, three different baseplate (storage) temperatures were selected to generate three distinct stress conditions. Three groups of devices were subjected to the following stress variations:

- high thermal - low electrical
- low thermal - high electrical
- ~medium thermal - ~medium electrical

The Au/Sn bonded IMPATTs were subjected to the high - low stress conditions, whereby the TC-bonded devices were stressed at the medium levels. The grouping of the stress conditions was utilized to define the corresponding effects on the performance of the diodes, specifically the thermal resistance.

The tabulated results shown here, clearly demonstrate the substantial degradation in RF power output and thermal resistance identified with the high thermal stress device group. Degradation is still evident with the high electrical stress diode group, however the degradation is greatly reduced.

Conversely, the TC bonded devices not only remained unchanged and stable, but the initial, pre stress thermal resistance is also about 15 percent lower.

Thus, the thermocompression bonded IMPATT diode has proven to be much superior to the gold-tin soldered device.

The above experimental results were essential to the failure analysis of degraded GaAs IMPATT diodes and supported the findings that, indeed, the Au/Sn eutectic solder is an unstable compound, not suitable for high temperature junction devices, and degrades device performance at relative low storage temperatures.

The following SEM-Analysis offers further evidence of undesirable effects arising from the continuous reaction of the gold-tin as a function of temperature.

AVERAGE RF STRESS TEST DATA SUMMARY



● HIGH THERMAL - LOW ELECTRICAL STRESS

|         | $P_{IN}(W)$ | $T_{BP}(^{\circ}C)$ | $T_J(^{\circ}C)$ | TIME(MIN) | $P_{OUT}(W)$ | $\eta \%$ | $F_0(GHz)$ | $\theta_{TH}(^{\circ}C/W)$ | BOND. |
|---------|-------------|---------------------|------------------|-----------|--------------|-----------|------------|----------------------------|-------|
| INITIAL |             |                     |                  |           | 1.29         | 14.2      | 19.76      | 23.2                       | AU/SN |
| TEST #1 | 5.17        | 135                 | 225              | 1         | 1.29         | 13.9      | 19.8       | 24.8                       | AU/SN |
| #2      | 2.62        | 250                 | 310.5            | 1         | 1.25         | 13.8      | 19.74      | 25.4                       | AU/SN |
| #3      | 2.93        | 275                 | 349              | 20        | 0.96         | 12.3      | 19.62      | 28.6                       | AU/SN |
| #4      | 2.34        | 245                 | 312              | 15        | 0.76         | 10.7      | 19.94      | 29.4                       | AU/SN |
| #5      | 1.56        | 265                 | 311              | 5         |              |           |            | 29.8                       | AU/SN |

● LOW THERMAL - HIGH ELECTRICAL STRESS

|         |       |    |       |    |      |      |       |      | AU/SN |
|---------|-------|----|-------|----|------|------|-------|------|-------|
| INITIAL |       |    |       |    | 1.63 | 14.4 | 20.02 | 24.9 | AU/SN |
| TEST #1 | 10.29 | 30 | 254.8 | 1  | 1.46 | 13.1 | 19.96 | 24.8 | AU/SN |
| #2      | 9.7   | 80 | 316.3 | 1  | 1.27 | 11.7 | 19.96 | 26.1 | AU/SN |
| #3      | 9.94  | 96 | 348   | 20 | 1.29 | 12.0 | 19.78 | 25.7 | AU/SN |
| #4      | 10.12 | 60 | 312.4 | 15 | 1.21 | 11.7 | 19.88 | 25.9 | AU/SN |
| #5      | 9.29  | 80 | 309.5 | 5  |      |      |       | 25.9 | AU/SN |

● MEDIUM THERMAL AND ELECTRICAL STRESS

|         |      |     |       |    |      |      |       |      | TC |
|---------|------|-----|-------|----|------|------|-------|------|----|
| INITIAL |      |     |       |    | 1.44 | 14.7 | 19.73 | 20.5 | TC |
| TEST #1 | 8.0  | 105 | 263   | 1  | 1.26 | 12.9 | 19.61 | 20.9 | TC |
| #2      | 7.2  | 160 | 310.5 | 1  | 1.59 | 16.1 | 19.84 | 20.1 | TC |
| #3      | 6.72 | 215 | 350.0 | 20 | 1.33 | 13.8 | 19.84 | 20.6 | TC |
| #4      | 7.20 | 162 | 310.3 | 15 | 1.46 | 14.8 | 19.78 | 20.5 | TC |
| #5      | 7.18 | 163 | 310.9 | 5  |      |      |       | 20.5 | TC |

FIGURE 94.

## B. SEM Analysis of Degradation Failures

The following series of SEM photos dramatically illustrate the profound change of the barrier surface morphology of the gold/tin bonded IMPATT diodes. The degree of surface distortion is a function of stress time and temperature. It was also determined later, that the Varian Associates diodes utilize heatsink metal other than gold and employ nickel as a diffusion barrier, which reduced the Au/Sn thermal effect at the barrier surface, but did not eliminate it.



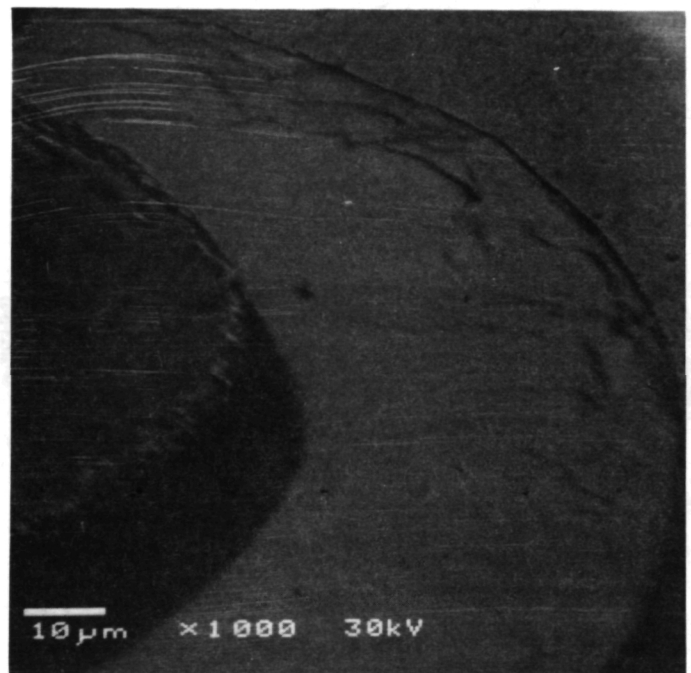
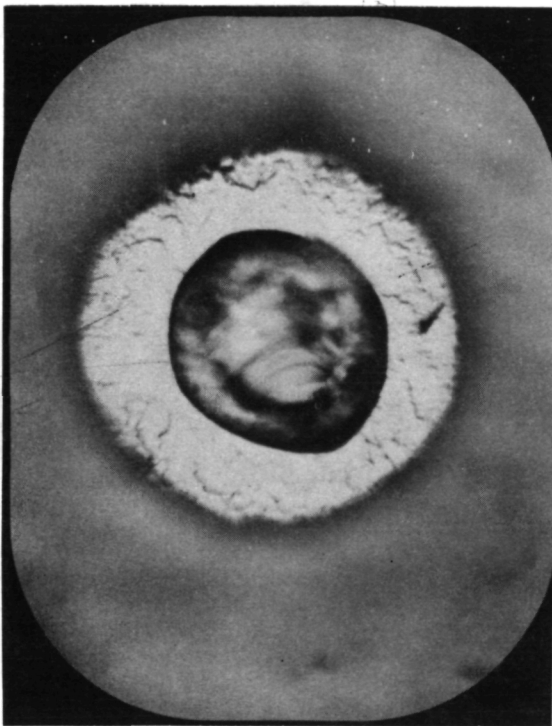
# SEM ANALYSIS OF THERMAL EFFECTS

DIODE NO.: 1237G

STRESS TEST TEMPERATURE: 345°C

TEST TIME: 72.8hrs.

ASSEMBLY FABRICATION : LNR Schottky-  
Barrier Au/Sn  
Solder Bonded



X200

Au/Sn solder bonded diodes show severe wrinkle effect on the Pt barrier metal, (this is characteristic of Au/Sn solder bonded diodes). Thermal Effect was noted after only 73 hours of accelerated aging, (Fracture of the GaAs chip resulted when the contact ribbon was removed.)

Discrete chemical etching of the GaAs IMPATT chip exposes the smooth barrier metal (Pt) surface. In contrast, the barrier metal not covered by the GaAs during the high temperature stressing appears raised and greatly distorted. Thus, the effects of the thermally activated Au/Sn compound reaction are visible, even though, the barrier surface is separated by the remaining barrier metal structure and close to 50 microns of gold plated heatsink.

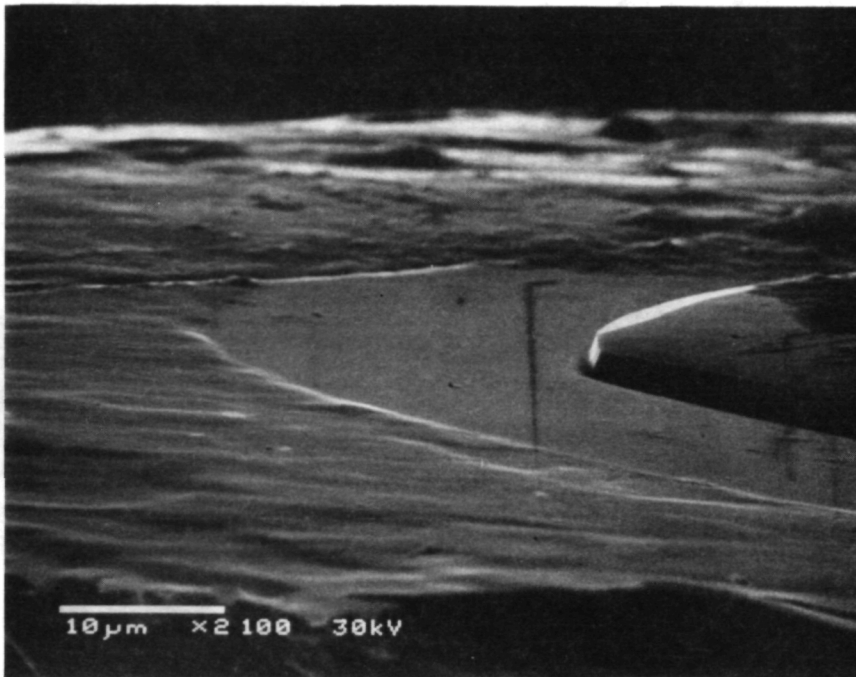
# SEM ANALYSIS OF THERMAL EFFECTS

DIODE NO.: 1317G

STRESS TEST TEMPERATURE: 321°C

TEST TIME: 122.75 hrs.

ASSEMBLY FABRICATION: LNR Schottky-  
Barrier Au/Sn  
Solder Bonded



— GaAs

— Original GaAs  
chip area

— Region not covered  
by the GaAs

Thermal effects on the barrier metal show up as a raised surface with roughened texture outside the area covered by the IMPATT chip. The GaAs was removed as part of the failure analysis.

As previously mentioned, the surface distortion is less severe on the Varian Associates grown junction diodes, however, the effects are still clearly visible. Note the terrace effect due to the undercutting of the active region during etching. Damaged area resulting from the electrical short is also visible, lifting of barrier metal in the rear area defined as the under cut active area.

SEM ANALYSIS OF THERMAL EFFECTS

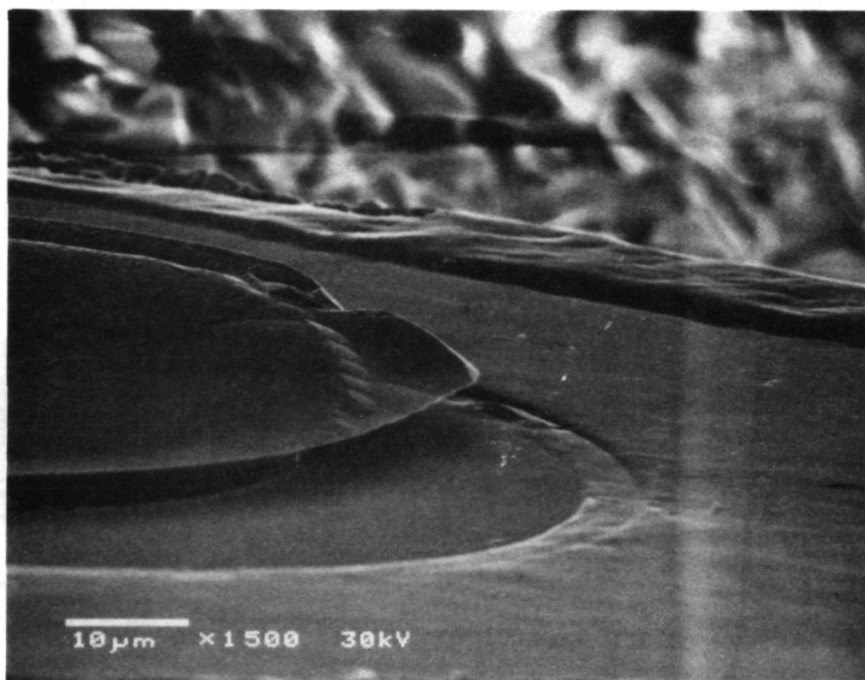
**LNR**  
COMMUNICATIONS

DIODE NO: S/N 27

STRESS TEST TEMPERATURE: 321°C

TEST TIME: 80.85 hrs.

ASSEMBLY FABRICATION: Varian Grown-  
Junction Au/Sn  
Solder Bonded  
Chip T.C.  
Bonded Ribbon



Thermal Effects on contact metal near the active region not covered by the GaAs chip is shown as a raised surface with a change in texture following removal of GaAs via chemical etching.

In contrast, no surface texture changes are noted on this experimental LNR grown junction 20 GHz IMPATT diode, different only in that the device was thermo-compression rather than solder bonded. No structural metallization modifications were implemented. The diode accumulated 1060 hours of stressing at a junction temperature of 304°C. Prior to failure analysis which was performed for the sole purpose of investigating the barrier surface condition, the diode was characterized and found to be fully operational. However, accidental detuning during oscillator measurements shorted the diode.

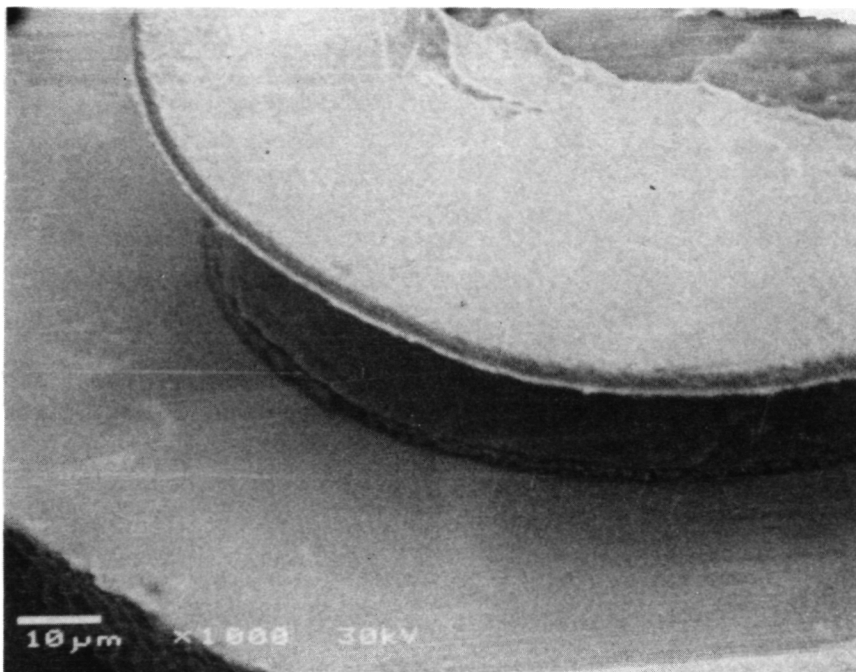
# SEM ANALYSIS OF THERMAL EFFECTS

DIODE NO.: 1632B

STRESS TEST TEMPERATURE: 304°C

TEST TIME: 1060.75hrs.

ASSEMBLY FABRICATION : LNR Grown  
Junction T.C.  
Bonded



— damaged ribbon  
bond area following  
ribbon removal

— Ohmic contact

— Substrate

— Active Layer

— Pt. Metallization

T.C. bonded diode shows no evidence of any thermal effects on the Pt. metallization following accelerated aging for 1060 hours.

## VI. CONCLUSIONS AND RECOMMENDATIONS

The completion of the Phase I reliability assessment on 20 GHz single drift GaAs IMPATT diodes has resulted in projecting the operational lifetime of Schottky barrier and grown junction IMPATT devices, defining four major failure mechanisms, recommending device modifications, addressing process and assembly improvements supported by experimental observations and failure analysis, and identifying future reliability efforts including device screening procedures.

LNR has demonstrated, that the 20GHz GaAs IMPATT diode is a viable EHF RF power source, which based on the recommendations made herein, will exceed ultimate device reliability requirements, consistent with a ten year spaceborne solid-state power amplifier mission.

### 1. Conclusions

The conclusions arising from the completed reliability assessment phase of unscreened 20 GHz GaAs IMPATTs are presented in summary.

- Measured and extrapolated medium lifetimes of GaAs IMPATT diodes far exceed previously predicted lifetimes.

Schottky Barrier:  $>3 \times 10^4$  hours

Grown Junction :  $>2.1 \times 10^6$  hours

- The failure mechanisms identified in this report can be eliminated by refining process and assembly procedures.
- A limited number of new and improved experimental IMPATT diodes fabricated as recommended clearly demonstrated significant increase in:

thermal stability

electrical stability

lifetimes

performance (Pulsed operation  $>10$   $\mu$ sec.)



- Confirmation of observed improvements via a second phase reliability program is fundamental in establishing a high level of confidence in the integrity and reliability of EHF - GaAs IMPATT diodes (single and double drift).
- The recommendations directed towards device improvement do not require a technological break through, but are readily available for implementation.
- Severe degradation of the current-voltage (I-V) characteristics has been experimentally identified with surface-states resulting from incorrect etching and rinse procedure. Schottky barrier (LHL) diode degradation is compounded by:
  - carrier concentration at barrier surface
  - critical distance of surfact to doping spike
- Incorrect sealing results in entrapment of potential contaminants causing substantial degradation.
- In general, grown junction diodes exhibit superior I-V characteristics.
- Schottky barrier diodes with excellent pre high temperature storage I-V characteristics remained nearly as stable as the grown junction diodes.
- Conversely, diodes with relative poor I-V characteristics at the 10  $\mu$ a level degraded with temperature at an accelerated rate.
- Additional changes associated with the IMPATT metallization structures and/or GaAs during the stress testing are not ruled out, as they may have been obscured by the effects of the Au/Sn degradation. However, judging by the experimental data, such changes, if any, appear minimal.

- Observed failure modes and failure mechanisms were general in nature and could not be identified with a specific wafer and/or device lot.
- Accelerated RF stress testing of the herein described IMPATT diodes was not possible because of the severe degradation of RF performance. Loss of oscillation during high temperature measurements, suggest that high temperature RF stressing would ultimately result in a form of DC stressing.
- Device performance degradation at high baseplate temperatures has been linked to the Au/Sn eutectic solder used for device assembly.

## 2.0 Recommendations

### 2.1 Preferred IMPATT Diode Design

With the average achievable RF performance being equal, it was easy to recommend the H-L profiled grown junction IMPATT device for further reliability assessments and ultimate space-borne SSAP application. Achieving the required ideal relation between perfect current voltage characteristics and reliable RF device performance is nearly impossible with the L-H-L profiled Schottky barrier IMPATTs on a high yield, cost effective basis.

### 2.2 Processing and Fabrication Modifications

The recommended changes of state-of-the art metallization structures, were developed and reported after the reliability assessment program was in progress. Experiments, with the recommended modifications in place, conducted at LNR confirmed improvements reported by Raytheon.

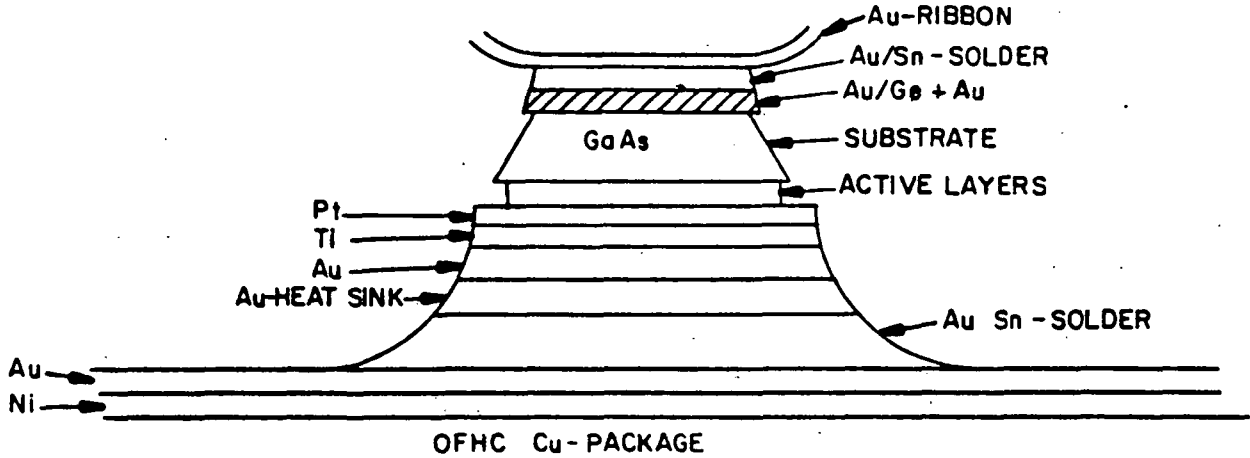
Large area thermocompression bonding developed at LNR was used for experimental devices and found to be superior to Au/Sn bonded diodes. Thus, elimination of Au/Sn in favor of thermo compression bonding in addition to the illustrated modifications in the GaAs metallization is strongly recommended.

# RECOMMENDED IMPATT DIODE PROCESSING AND FABRICATION IMPROVEMENTS

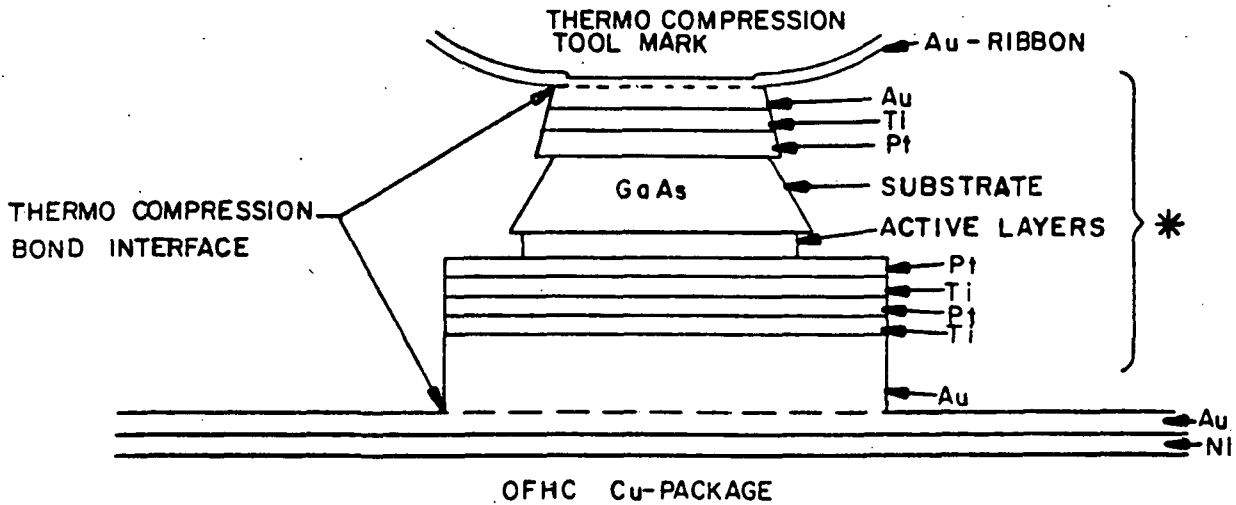


CURRENT

## IMPATT CHIP CROSS SECTION



RECOMMENDED



\* METALIZATION SYSTEM AS DEVELOPED BY RAYTHEON AND REPORTED AT "MANTECH DEBRIEFING", MAY, 1983

FIGURE 994.

### 2.3 Screening Procedure for IMPATT Diodes

Resulting from the accelerated stress test program and the determination of criteria to define early failures described in Appendix 'A', a preliminary screening procedure, as shown in the flow chart, has been developed and is recommended for implementation of a potential follow on reliability program.

The high temperature reverse bias burn in is perhaps the most important screening step in that its purpose is the elimination of "Infant Mortalities", early failures. For the statistical analysis criteria III of Appendix 'A' was used, however, with the elimination of the Au/Sn it is recommended to implement criteria II which is a slightly lower burn-in level.

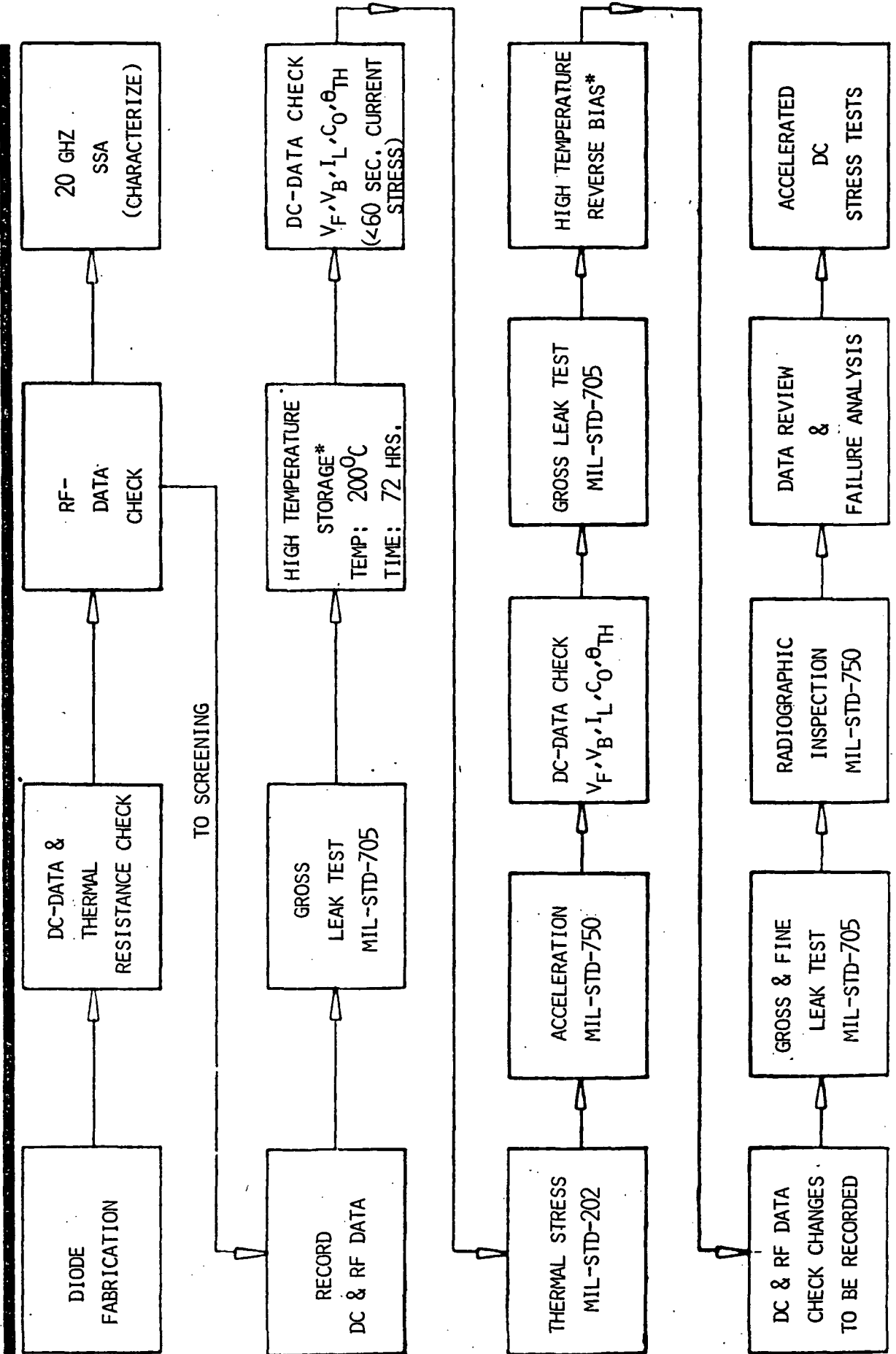
IMPATT Diode Stress Temperature: 270°C  
Burn in Time : 168 Hours

An operational DC burn in is preferred, with test conditions being identical to those of the accelerated stress test.

Specifically, the junction stress temperature is achieved via a combination of high temperature storage and applied reverse bias.

It is conceivable that the burn in schedule, which indicates a high stress level, may have to be revised following initial screening and accelerated stress testing of one device sample lot.

20 GHZ IMPATT DIODE SCREENING



\* BIASED TO REVERSE BREAKDOWN  
FIGURE 10.0.

#### 2.4 Extended Reliability Assessment

The completion of the herein reported 20 GHz IMPATT reliability assessment must be viewed as an initial assessment, with the reported results forming the basis for an extended reliability program, consistent with the reliability objectives enumerated in this final report.

An extended reliability program would consist of the major tasks and tests illustrated in the flow chart. The essential stress test configuration would again comprise high, medium and low temperature stress levels, adding the validation of the proposed screening procedure via a high temperature accelerated DC stress test, ultimately determining the actual burn in conditions to be used.

The advantages of an added temperature optimized stress test in conjunction with 20 GHz oscillator measurements are:

- provide fourth data point on Arrhenius reaction rate plot;
- perform 20 GHz oscillator measurements at pre-determined intervals by interrupting the DC stress test;
- correlate DC stress test data to actual RF performance data;
- comparison between interrupted and continuous stress testing;
- enhance confidence level.

The result of the initial accelerated stress tests are used to optimize the stress temperature.

The dominating degradation effect of the Au/Sn solder indicates the need to further investigate high temperature effects on 20 GHz oscillator measurements, providing the potential design criteria or an accelerated RF stress test configuration.

Finally, the inclusion of a fifth accelerated stress test with an assumed operational lifetime of  $10^4$  hours, would permit a relative low stress temperature, thus providing maximum confidence in the reliability data. Obtaining the activation energy from the aforementioned stress tests will permit extrapolation of the  $\gamma_M$  after the first one or two failures occurring with  $1 \times 10^3$  and  $2 \times 10^3$  hours. A major advantage of the recommended low temperature stress level would be the potential verification of the activation energy obtained at high temperature stress levels with stress data reflecting results most generically identified with operational 20 GHz GaAs IMPATT diodes.



RECOMMENDATIONS FOR A SECOND PHASE RELIABILITY  
ASSESSMENT PROGRAM

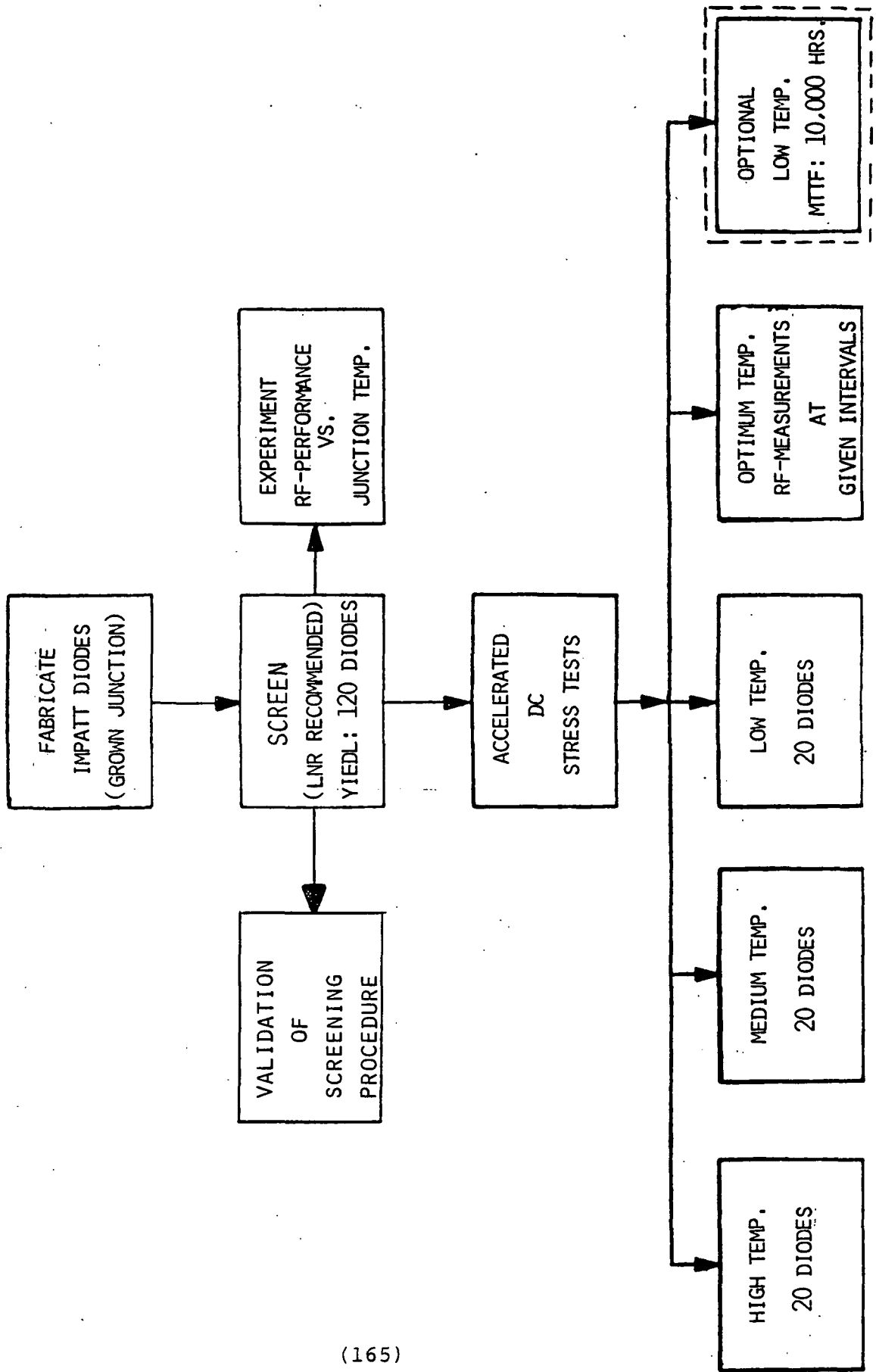


FIGURE 101.

## VII. REFERENCES

- (1) LNR, Technical Report AFWAL-TR-83-1142, September 1983.
- (2) Raytheon/AFWAL, MANTECH DEBRIEFING, May 1983.
- (3) W.A. Johnson and M.F. Millea, "Statistical Analysis of Accelerated Temperature Aging of Semiconductor Devices", Technical Report SD-TR-81-37, 15 May 1981.
- (4) D.S. Peck and C.H. Ziedt, Jr., "The Reliability of Semiconductor Devices in the Bell System," Proc. IEEE, 62, 185-211 (1974).
- (5) F.H. Reynolds, "Thermally Accelerated Aging of Semiconductor Components," Proc. IEEE, 62, 212-222 (1974).
- (6) M. Millea and R. Sahmel, "GaAs 20 GHz IMPATT and FET Reliability Assessment Technical Report", NASAID No. 1-10-A-1-T1, (1981).
- (7) IEEE Standards Committee, "IEEE Guide for the Statistical Analysis of Thermal Life Test Data," IEEE standard 101-1972 (reaffirmed 1980), IEEE Inc, NY March 17, 1972.
- (8) N.B. Kramer and M.M. Morishita, "IMPATT Diode Life Tests", Hughes Aircraft Company, November 1983.
- (9) J.H. Zar, Biostatistical Analysis, Prentice-Hall Inc., N.J. 1974.

APPENDIX 'A'

DETERMINATION OF CRITERIA  
TO DEFINE EARLY FAILURE

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## DETERMINATION OF CRITERIA TO DEFINE EARLY FAILURE

The following is a summary of the rationale used to define early failures and to derive a burn-in screening procedure for the estimation of early failures from the main device population.

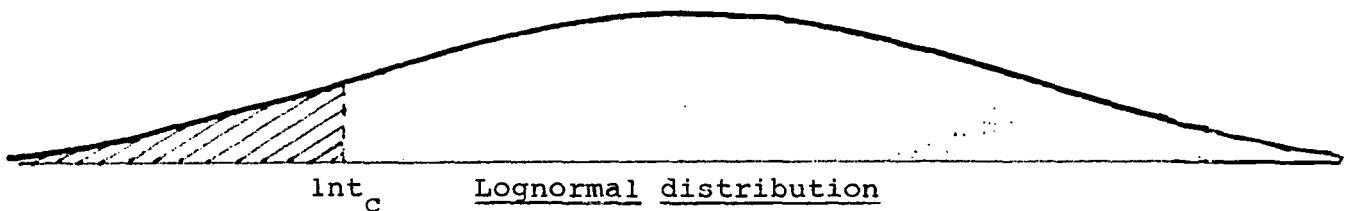
From each of the accelerated stress tests carried out, an insufficient number of infant mortalities were obtained or could be identified as such. Based on the assumption that early failures may be due to different failure modes or mechanisms, the realization of an early failure activation energy is further complicated and seems nearly impossible. In order to extrapolate an effective screening criteria from the limited stress test data, "cut off" points (denoted  $t_c$ ) between early failures and main sample failures must be clearly defined. Since precise cut off points are not obvious from the stress test data, three possible approaches are investigated.

The infant cut off time can be defined as:

- I. Approximately equal to the first main sample failure time ( $t_c = t_1$ ).
- II. Equal to  $\exp(\bar{X} - 3\sigma)$ , derived from the log normal data at each stress test level. The quantity  $(\bar{X} - 3\sigma)$  is in accordance with the concept of a normal distribution.  $(t_c = t_{\exp(\bar{X} - 3\sigma)})$   
 $\bar{X}$  = sample mean  $\ln$ (failure time)  
 $\sigma$  = approximate standard deviation
- III. Derived from the inflection point (between infant and main sample failures) on each whole-sample cumulative frequency plot ( $t_c = t_{infl.}$ )

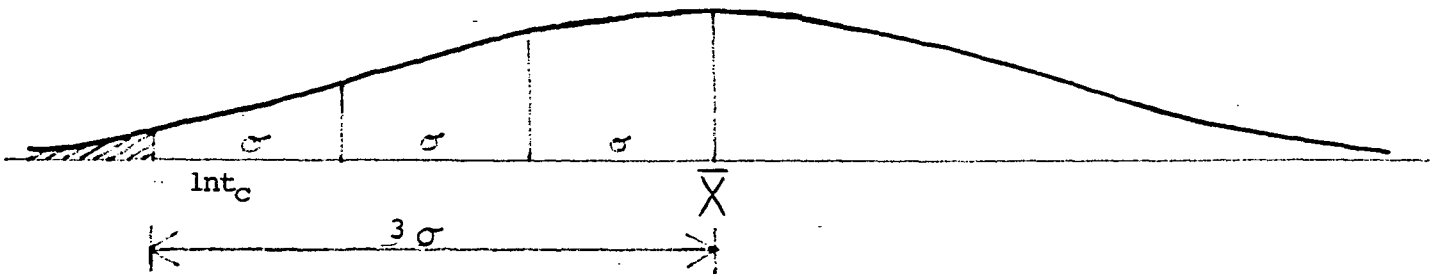
The rationale addressing the above approaches is summarized as follows:

- I. Given that the original whole population was not sufficiently large, the first main sample failure time may not be a good estimate of the first main population failure time. Therefore, this type of definition could potentially lead to a burn-in screen which may result in the removal of non-infant mortalities along with the true early failures. Furthermore, a substantial part of the operating lifetime would be consumed by this method of burn-in.



The shaded area depicts infant mortalities plus an unknown percentage of main population failures.

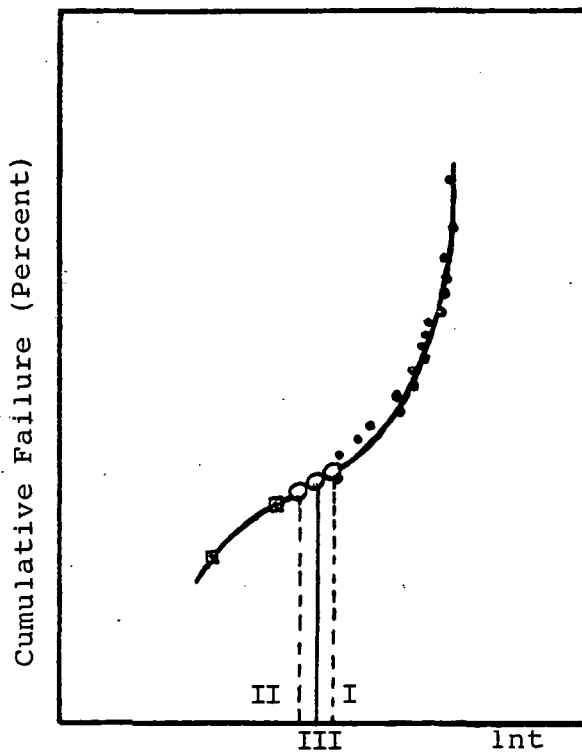
II. This method depends on first plotting each whole-sample cumulative frequency plot. Infant mortalities are determined as points which fall before the line and are then eliminated from the data set. Next, a second plot is made using the main-sample data only. Once lognormality is verified,  $\bar{X}$  and  $\sigma$  are determined. Finally, a cutoff time is calculated as  $t_c = \exp(\bar{X} - 3\sigma)$ . However, this method depends on first eliminating infant mortalities which are not yet clearly defined, and therefore could lead to ambiguities.



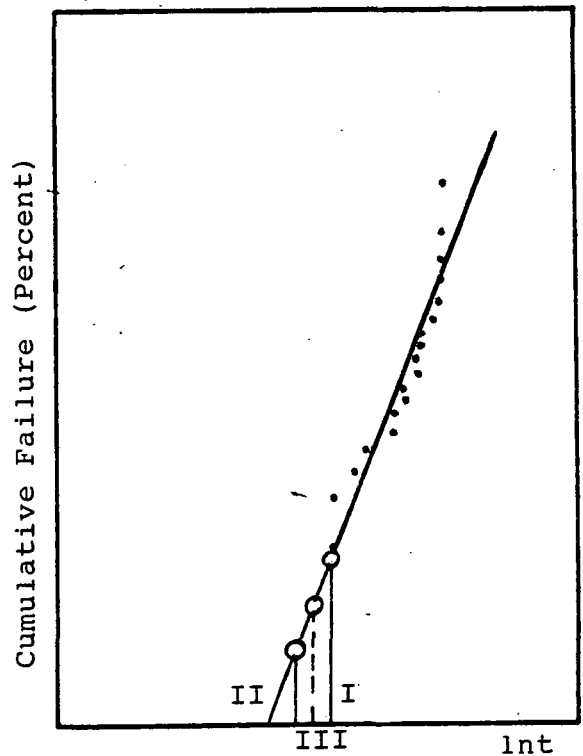
The shaded area depicts infant mortalities plus 0.135% of the main-population failures.

III. The inflection point of each whole-sample cumulative frequency plot is defined as the exact cutoff between infant failures and main-sample failures. This method is the most realistic in terms of estimating the true population cutoff point. The problem with this method is that it may not be as straight forward as it seems. Inflection points may not be clearly defined on the plots, as is the case with the Schottky barrier stress test data. However, by looking at a typical sample plot, it can be seen that the inflection point lies about half way between the points obtained by applying methods I and II as illustrated.

Example of Cumulative Frequency Plots




Whole-sample data illustrating actual inflection point (III) as well as the cut off points obtained from I and II.



Main-sample data (i.e. infant mortalities removed) illustrating the location of  $Int_{infl.}$  with respect to the other methods cited.

Graphical Representation: (Schottky Barrier IMPATTs)

- A. depicts individual life times vs. (inverse) test temperature. Infant mortalities are shown as 
- B. illustrates the Arrhenius dependence of the data. Notice the median lifetimes ( $\tau_M$ ) for main-sample data only.
- C. shows the results of each criteria. Extrapolation of screening criteria yields lines parallel to the Arrhenius line. (Note: "cutoff" implies that this is when infant failures cease and main-population failures begin).

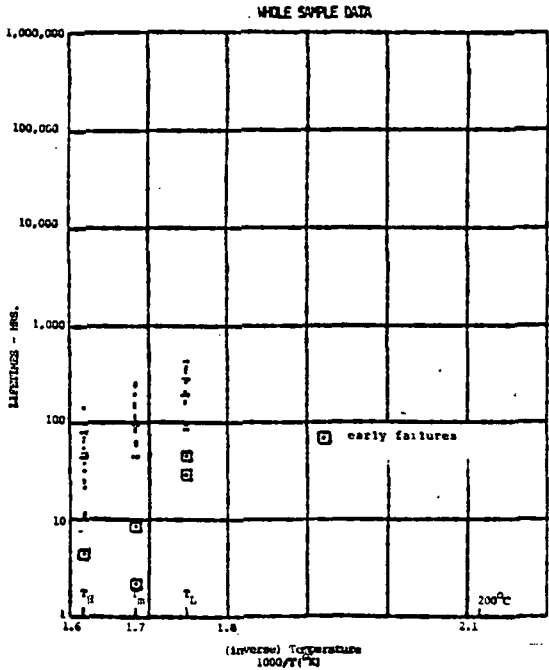
In summary, from the three methods described inflection point approach appears best suited in defining early failures of a limited device population and establishing an effective procedure for the device screening burn in.

The following observations are illustrated in

- I. Definition appears to be too arbitrary and too severe. The extrapolated line cuts through the main sample.
- II. Extrapolation appears lenient in view of the presented stress test data, since not all the early failures are eliminated. However, due to the impact the Au/Sn solder had on Criteria II was applied towards the recommended reverse bias burn in screening.
- III. Drawing a line half way between I and II eliminated all apparent early failures, without affecting the main-population. This method was used for the statistical analysis presented in Appendix B.

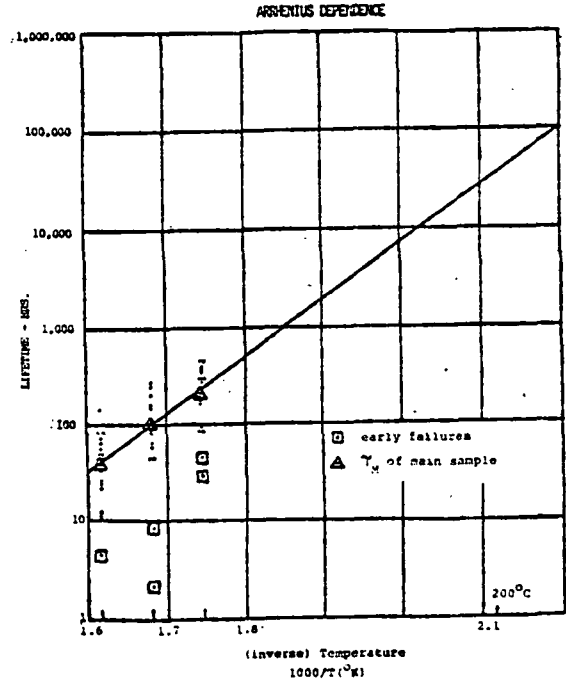


# ARRHENIUS DEPENDENCE

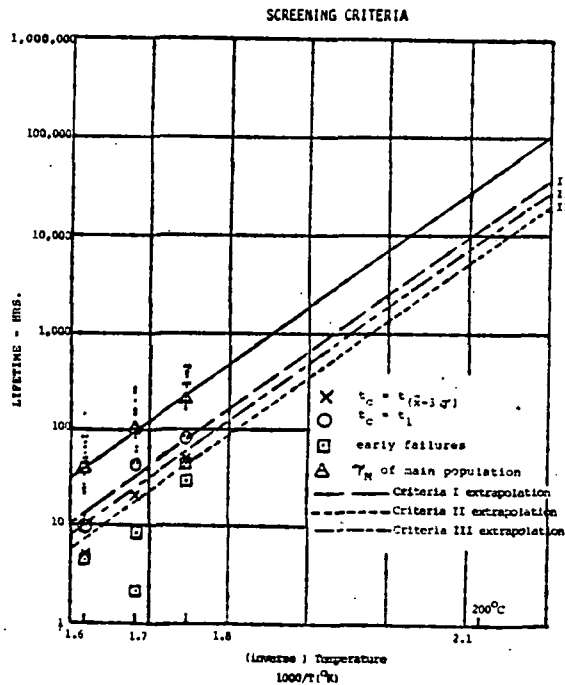


2 points off scale at  $T_m$  (not shown on other graphs).

A.



B.



C.

Definitions:

$t_c \equiv$  the cutoff time between infant mortalities and main-population failures at any given temperature.

$t_1 \approx$  the first main-sample failure time at any given test temperature.

$t_{(\bar{x}-3\sigma)} = \exp(\bar{x}-3\sigma) =$  cutoff time at three standard deviations below the logarithmic median lifetime at a given test temperature.

$t_{infl} =$  the time derived from the inflection point on each whole-sample plot.  $t_{infl.} = \exp(X_{infl})$

Where,

$x_i = \ln$  (time to failure, hrs) for each main-sample failure;

$n =$  the number of main-sample failures observed at the given test temperature.

$\sigma =$  standard deviation. (log base e)

Note: The estimates of  $\sigma$  obtained from lognormal cumulative frequency plots are used throughout.

$$\bar{x} = \text{sample mean} = \frac{\sum x_i}{n}$$

Main Sample  $\equiv$  actual test data excluding infant mortalities (i.e. the lognormal portion of the data).

Main Population  $\equiv$  all devices in the lognormal distribution. This includes the small sample of devices tested, as well as all other untested devices manufactured under the same conditions. However, it does not include infant mortalities.

## References

W.A. Johnson and M.F. Millea, "Statistical Analysis of Accelerated Temperature Aging of Semiconductor Devices" Interim Report SD-TR-81-37, May 15, 1984.

D.S. Peck and C.H. Zierdt, Jr., "The Reliability of Semiconductor Devices in the Bell System, Proc. IEEE, vol. 62 no. 2, 212-222 (1974).

APPENDIX 'B'  
STATISTICAL ANALYSIS  
OF  
LIFE TEST DATA

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## STATISTICAL ANALYSIS OF LIFE TEST DATA

### INTRODUCTION

Accelerated DC Stress Testing was used to obtain information on the lifetime distributions of 20 GHz IMPATTs. Both Grown-Junction and Schottky Barrier devices were tested, twenty of each type at each of three elevated test temperatures. To examine the mathematical relationship between device lifetime and junction temperature, the Arrhenius Model was applied. The application of statistical principles yielded extrapolated device parameters at the specified normal operating temperature of 200°C. This appendix includes a brief introduction to these statistical concepts, as well as calculated and graphical representations of the analysis results.

### OBJECTIVE:

To predict specific parameters corresponding to an actual operating temperature from the lifetime data taken at elevated device-junction temperatures.

The following parameters will be determined:

- device median lifetime ( $\gamma_M$ , which corresponds to the time at which 50% of the device will have failed) and its associated confidence interval, as explained in a later section;
- the lifetime of a single, untested device at the requested level of confidence or degree of accuracy;
- the logarithmic variance ( $\sigma^2$ ) and its associated confidence interval;
- the activation energy ( $E_a$ ) of the main failure mode.

## Fundamental Assumptions of the Analysis<sup>(1)</sup>

The mathematical rationale used to analyze life-test data is based on the following conditions, Figure 1.

- (1) The lifetime at a constant temperature and applied electrical stress is expressed by a single lognormal probability density function (pdf), where "lognormal" means that the logarithms of device lifetimes are normally distributed.
- (2) The failure mode is characterized by a single activation energy.
- (3) The logarithmic variance is independent of temperature.
- (4) The median lifetime follows an Arrhenius dependence expressed as:

$$\tau_M = \tau_0 \exp(E_a/k_B T) \quad (1)$$

$$\text{or, } \ln \tau_M = \ln \tau_0 + E_a/k_B T \quad (2)$$

These reaction-rate parameters are now simplified and converted to standard statistical regression parameters as follows:

$$Y = \alpha + \beta X \quad (\text{exact population parameters}) \quad (3)$$

$$Y = a + bX \quad (\text{estimates of population parameters obtained from sample data}) \quad (4)$$

Where:

X = reciprocal junction temperature (1/°K)

Y =  $\ln \tau_M$  = ln(Median lifetime, hrs.)

a  $\approx$   $\alpha$  =  $\ln \tau_0$  = ln(pre-exponential constant) = intercept of the regression line.

b  $\approx$   $\beta$  =  $\frac{E_a}{k_B}$  = slope of the regression line.

Analysis Approach: (1-4)

SIMPLE LINEAR REGRESSION

"Simple Linear Regression" refers to a linear functional dependence between two variables. One variable, in this case temperature, is independent, while the other, in this case lifetime, is dependent. This is a commonly employed statistical procedure. The resulting simple linear regression equation is written as:

$$Y = \alpha + \beta X, \quad (3)$$

Where:

X = the independent variable

Y = the dependent variable

$\alpha$  = the Y-intercept.

$\beta$  = the regression slope

(Figure 2)

If the actual data does not show a linear relationship, a transformation of the parameters often may be employed. Such that for the transformed parameters a linear dependence is obtained. In the case of life test data, a logarithmic transformation of the lifetime and a reciprocal transformation of the temperature are used.

The main objective of simple linear regression is to determine the "best fit" line through the X,Y data. This is accomplished by utilizing the concept of least-squares<sup>(4)</sup>. The outcomes of the least-squares regression analysis are:

- $s_{reg}^2$  Commonly referred to as the regression variance, is the best estimate of population parameter  $\sigma^2$
- a the best estimate of population parameter  $\alpha$ , the Y-intercept
- b the best estimate of the regression slope
- $\hat{Y}$  ("Y-hat") the estimated Y value corresponding to a given X.

### EXTRAPOLATION

"Extrapolation" refers to the prediction of Y for given values of X outside the sample (test) range of X. (Figure 3)

Note: The scatter, or variance, in the original X,Y data leads to an uncertainty in projected Y value(s). Therefore, the true population value,  $Y_{\text{actual}}$ , should be expressed as a range  $Y_{\text{actual}} = \hat{Y} \pm \Delta$ . (Figure 4)

(Here,  $\Delta$  is a function of the Student-t distribution and the regression variance, as well as the spread in X values. The exact relation can be inferred from the formula for the 90% Confidence Interval for  $Y_{\text{Op}}$ , equation 13).

### CONFIDENCE LEVELS/INTERVALS

Confidence determination is an extension of a concept known as statistical hypothesis testing. (Refer to statistics text for description). In short, these concepts enable us, to state a range, or confidence interval for a particular population parameter along with the degree of accuracy, or confidence level associated with this range.

A confidence interval reads as follows:

"The probability that the true Y value is within the range stated is  $(1-\delta)$  percent", and is expressed mathematically as:

$$P \{ Y = (\hat{Y} \pm \Delta) \} = (1-\delta)\% \quad (5)$$

Here,

$P \{ \}$  means "the probability that..."  
 $\delta$  is known as the statistical significance level, and  $(1-\delta)$  is the confidence level.



The above expression is known as a two-tailed confidence interval, meaning that both the upper and the lower bounds are taken into account. For lifetime predictions, only the lower bound of the range is requested and is known as a one-tailed confidence interval. It reads "The probability that the true Y value is greater than the lower bound ~~stated~~ is  $(1 - \alpha)$  percent". In life testing, the lower bound prediction for the median lifetime is of great importance, whereas the upper bound is of little interest. (See Figure 5 and equations 13 and 14.)

Confidence intervals aside from  $Y_{\text{actual}}$  are derived in the analysis of life test data using equations 13, 14 and 15. The interval for the logarithmic variance utilizes the Chi-square distribution rather than the Student-t.

FIG 1: LOGNORMAL PDF  
PLOT  $\ln(\text{LIFETIME})$   
ON PROBABILITY PAPER;  
A LOGNORMAL PDF WILL  
RESULT IN A STRAIGHT LINE

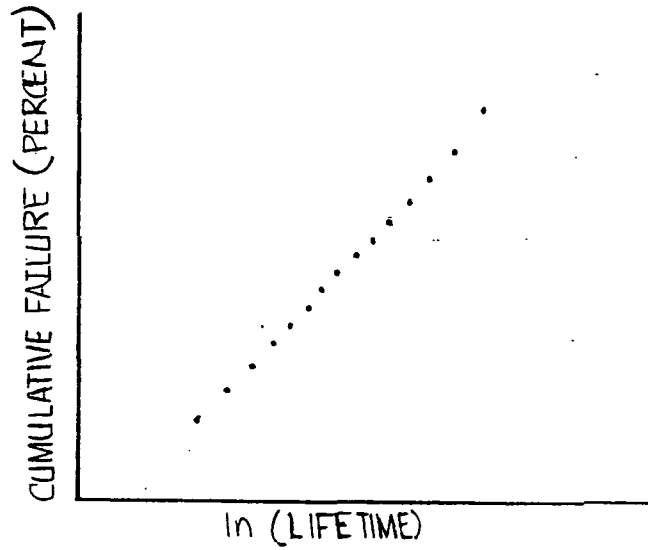


FIG 2: SIMPLE LINEAR  
REGRESSION

$$Y = \alpha + \beta X$$

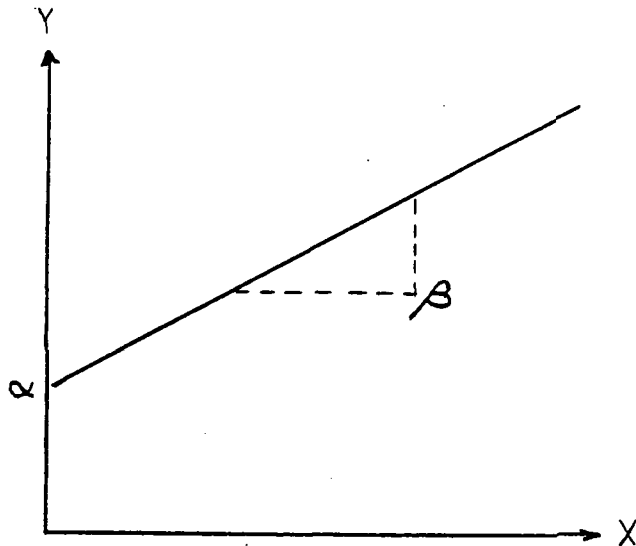


FIG 3: EXTRAPOLATION OF  $\hat{Y}$   
(AT GIVEN VALUE(S)  
OF X OUTSIDE THE  
TEST RANGE.)

$$\hat{Y} = a + bX$$

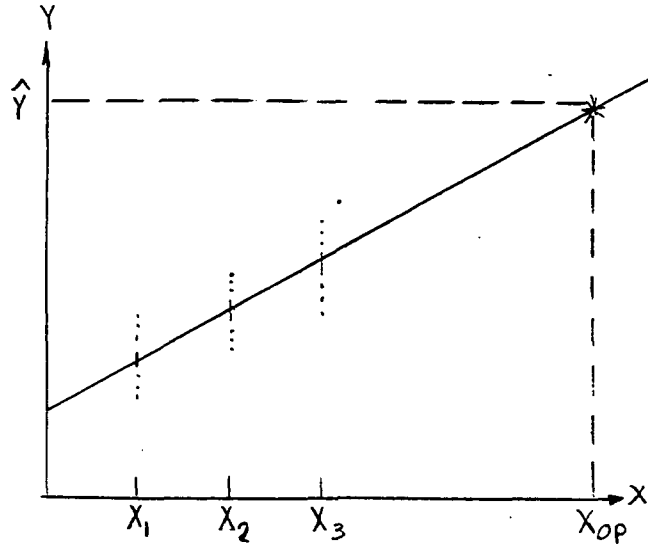
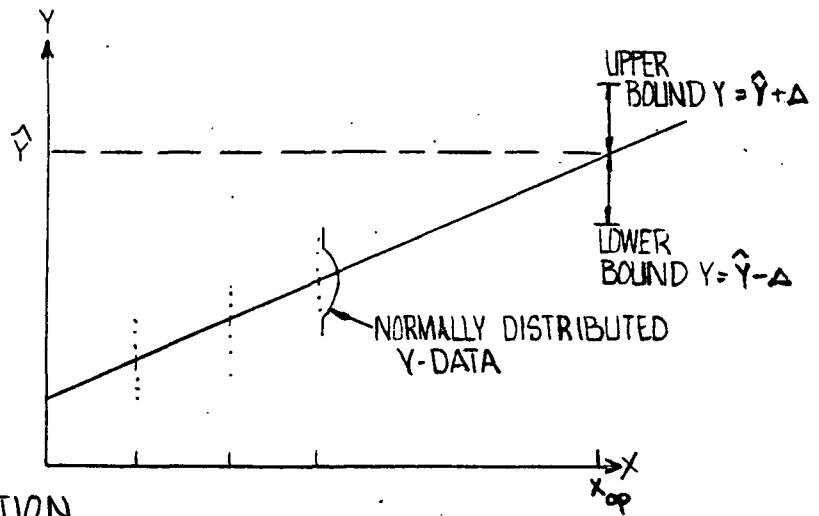
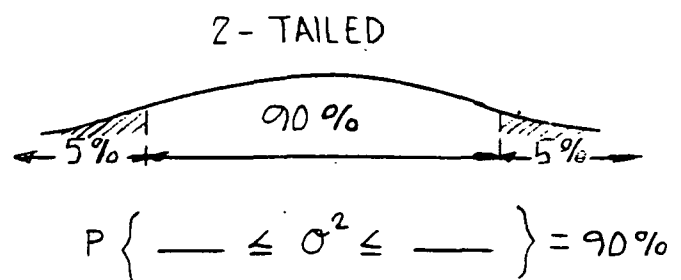
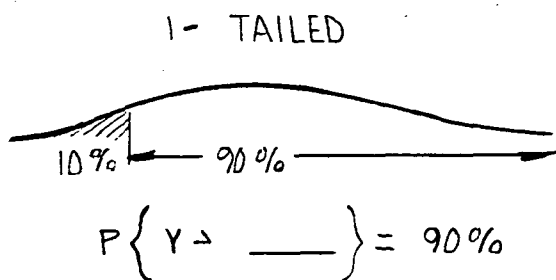


FIG.4: SCATTER IN  $\hat{Y}$   
(RELATED TO VARIANCE IN  
ORIGINAL DATA. IF  
THE VARIANCE IS SMALL,  
THE INTERVAL  $Y = \hat{Y} \pm \Delta$   
WILL BE NARROW)



IF Y DATA IS NORMALLY DISTRIBUTED AND  
THE VARIANCES OF EACH X-SAMPLE  
ARE EQUAL, THE STUDENT-T DISTRIBUTION  
MAY BE EMPLOYED TO DETERMINE THE INTERVAL (RANGE OF Y ACTUAL)

FIG 5: CONFIDENCE INTERVALS



## Analysis Equations<sup>1,4</sup>

First, we restate the Arrhenius equation and its equivalent regression or straight-line translation:

$$\ln \tau_M = \ln \tau_0 + \frac{E_a}{k_B T} \quad (2)$$

$$Y = a + bX \quad (3)$$

Where,

$$Y = \ln(\text{lifetime, hrs})$$

$$X = 1/T(^{\circ}\text{K}) = \text{reciprocal junction temperature}$$

$$a = \ln \tau_0 = Y\text{-intercept} = \ln(\text{pre-exponential constant})$$

$$b = \frac{E_a}{k_B} = \text{regression slope}$$

$$E_a = \text{activation energy, eV}$$

$$k_B = \text{Boltzmann's Constant} \\ = 8.625 \times 10^{-5} \text{ eV}/^{\circ}\text{K}$$

## Estimates of Regression Parameters

$N$  = total number of devices tested, excluding early failures

= number of  $X, Y$  pairs

$$\bar{X} = \sum X/N \text{ over entire sample} \quad (6)$$

$$\bar{Y} = \sum Y/N \text{ over entire sample} \quad (7)$$

$$b = \frac{\sum [(X-\bar{X})(Y-\bar{Y})]}{\sum (X-\bar{X})^2} \quad (8)$$

$$a = Y - bX \quad (9)$$

$$S_{\text{reg}}^2 = \frac{\sum Y^2 - a \sum Y - b \sum XY}{N-2} \quad (10)$$

$$S_{\text{reg}} = \sqrt{S_{\text{reg}}^2} \quad (11)$$

### Extrapolation

$$\hat{Y}_{op} = a + bX_{op} \quad (12)$$

given,

$$X_{op} = 1/73^{\circ}K$$

### 90% Confidence Intervals

$$P \left\{ Y_{op} > \hat{Y}_{op} - t_{10\%, N-2}^{(1-tail)} S_{reg} \sqrt{\frac{1}{N} + \frac{(X_{op} - \bar{X})^2}{\sum (X_i - \bar{X})^2}} \right\} = 90\% \quad (13)$$

$$P \left\{ Y_{N+1} > \hat{Y}_{op} - t_{10\%, N-2}^{(1-tail)} S_{reg} \sqrt{1 + \frac{1}{N} + \frac{(X_{op} - \bar{X})^2}{\sum (X_i - \bar{X})^2}} \right\} = 90\% \quad (14)$$

$$P \left\{ \frac{S_{reg}^2 (N-2)}{\chi_{5\%, N-2}^2} \leq \sigma^2 \leq \frac{S_{reg}^2 (N-2)}{\chi_{95\%, N-2}^2} \right\} = 90\% \quad (15)$$

Where,

$t_{10\%, N-2}^{(1-tail)}$  = Student-t value at 10% significance and N-2 degrees of freedom (table value)

$\chi_{\% , N-2}^2$  = Chi-Square value at the specified significance level and N-2 degrees of freedom (table value)

Translation to Arrhenius Parameters at 200°C

- Activation Energy

$$E_a \text{ (eV)} = k_B b \quad \text{(from eq. 8)}$$

- Pre-exponential Constant

$$\ln \tau_0 = a \quad \text{(from eq. 9)}$$

- Estimated median lifetime

$$\tau_M \approx \exp(\hat{Y}_{op}) \quad \text{(from eq. 12)}$$

- 90% Confidence Lower Bound for  $\tau_M$

$$P \{ \tau_M > \exp(Y_{op} \text{ lower bound}), \text{ hrs} \} = 90\% \quad \text{(from eq. 13)}$$

- Estimated Logarithmic Variance =  $S_{reg}^2$  (from eq. 10)

- Two-tailed 90% Confidence Interval for Logarithmic Variance

$$P \{ \text{lower bound} \leq \sigma^2 \leq \text{upper bound} \} = 90\% \quad \text{(from eq. 15)}$$

- 90% Confidence Lower Bound for the Lifetime of a Future Untested Device =  $\tau_{N+1}$

$$P \{ \tau_{N+1} > \exp(Y_{N+1} \text{ lower bound}), \text{ hrs} \} = 90\% \quad \text{(from eq. 14)}$$

## SUMMARY OF TERMS AND SYMBOLS

### Definitions

### Regression

$Y = \alpha + \beta X$  = linear regression equation

$X$  = independent variable =  $1/\text{junction temperature, } ^\circ\text{K}$

$Y$  = dependent variable =  $\ln(\text{lifetime, hrs.})$

$\alpha$  = Y-intercept, population parameter

$a$  = estimated Y-intercept, from sample (test) data

$\beta$  = regression line slope, population parameter

$b$  = estimated slope

also

$N$  = total number of X,Y pairs

$\bar{X}$  = sample mean of X =  $\sum X_i / N$

$\bar{Y}$  = sample mean of Y =  $\sum Y_i / N$

$\sigma^2$  = variance, population parameter

$s_{\text{reg}}^2$  = estimated variance, from regression analysis

### Extrapolation

$$\hat{Y}_{\text{op}} = a + bX_{\text{op}}$$

Where,

$\hat{Y}_{\text{op}}$  = estimated (projected) Y-value at  $X_{\text{op}}$

$X_{\text{op}}$  =  $1/\text{operating temperature, } ^\circ\text{K} = 1/473^\circ\text{K}$

### Confidence

$\delta$  = statistical significance level  $\cong 10\%$  (used to locate Student-t or Chi-Square values in table)

### Arrhenius Dependence

$\tau_M$  = device median lifetime

$E_a$  = activation energy of the main failure mode

$\tau_0$  = pre-exponential constant

$\tau_{N+1}$  = predicted lifetime of a future, untested device at normal operating temperature.



DEVICE PARAMETERS  
EXTRAPOLATED TO 200°C

SCHOTTKY BARRIER

GROWN JUNCTION

$E_A$  (ACTIVATION ENERGY)

1.148EV

1.887EV

$LN\tau_0$  (PRE-EXPONENTIAL FACTOR)

-17.829

-31.694

ESTIMATED MEDIAN LIFETIME

29,829 HRS.

2,111,865 HRS.

$P \{ \gamma_M > \underline{\text{LOWER BOUND}} \} = 90\%$

12,929 HRS.

397,630 HRS.

ESTIMATED  $\text{LOG}_E$ -VARIANCE ( $\sigma^2$ )

0.342

0.688

$P \{ \underline{\text{LOWER BOUND}} \leq \sigma^2 \leq \underline{\text{UPPER BOUND}} \} = 90\%$

$0.254 \leq \sigma^2 \leq 0.490$

$0.508 \leq \sigma^2 \leq 0.994$

LIFETIME OF A SINGLE UNTESTED DEVICE

$P \{ \gamma_{N+1} > \underline{\text{LOWER BOUND}} \} = 90\%$

9,641 HRS.

289,485 HRS.

DC ACCELERATED STRESS TEST DATA FOR  
20 GHz SCHOTTKY-BARRIER GAAS IMPATT DIODES



| HIGH TEMPERATURE<br>( $T_H = 345^\circ\text{C}$ )<br>N = 20 |              | MID. TEMPERATURE<br>( $T_M = 321^\circ\text{C}$ )<br>N = 20 |              | LOW TEMPERATURE<br>( $T_L = 299^\circ\text{C}$ )<br>N = 20 |              |
|---|--------------|---|--------------|--|--------------|
| DEVICE S/N  | $T_1$ (HRS.) | DEVICE S/N  | $T_1$ (HRS.) | DEVICE S/N   | $T_1$ (HRS.) |
| 1238G   | 4.55         | 1396B   | 0            | 1562B  | 29.05        |
| 1229G   | 11.1         | 1429B   | 0            | 1565B  | 45.65        |
| 1116B   | 12.8         | 1302B   | 2.25         | 1597G  | 84.2         |
| 680G  | 13.6         | 1397B   | 8.55         | 1553B  | 84.3         |
| 668G  | 22.25        | 1310G   | 44.75        | 1563B  | 95.6         |
| 362D  | 24.5         | 1382B   | 46.1         | 1591G  | 165.5        |
| 366D  | 25.8         | 1428B   | 60.5         | 1582G  | 170.5        |
| 685G  | 32.8         | 1307B   | 65.2         | 1500B  | 191.4        |
| 1231G   | 38.5         | 1318G   | 81.6         | 1555B  | 191.4        |
| 514G  | 44.8         | 1303B   | 87.7         | 1579G  | 191.6        |
| 1188G   | 45.6         | 1300B   | 93.2         | 1588G  | 218.8        |
| 1106B   | 46.1         | 1392B   | 93.4         | 1580G  | 273.0        |
| 1180G   | 48.8         | 1301B   | 105.2        | 1559B  | 285.0        |
| 470G  | 48.8         | 1314G   | 114.0        | 1586G  | 287.35       |
| 1223G   | 55.6         | 1317G   | 122.75       | 1589G  | 287.4        |
| 1220G   | 65.8         | 1430B   | 147.2        | 1499B  | 336.6        |
| 1254M   | 70.7         | 1316G   | 159.15       | 1497B  | 356.05       |
| 1237G   | 80.2         | 1385B   | 189.8        | 1552B  | 373.2        |
| 1264M   | 80.7         | 1389B   | 243.2        | 1549B  | 435.65       |
| 1177G   | 147.8        | 1313G   | 262.3        | 1581G  | 435.7        |

DC ACCELERATED STRESS TEST DATA FOR  
20 GHz SCHOTTKY-BARRIER GAAS IMPATT DIODES



EARLY FAILURES REMOVED

| HIGH TEMPERATURE<br>( $T_H = 345^\circ\text{C}$ )<br>N=19 |              | MID. TEMPERATURE<br>( $T_M = 321^\circ\text{C}$ )<br>N=16 |              | LOW TEMPERATURE<br>( $T_L = 299^\circ\text{C}$ )<br>N=18 |              |
|---|--------------|---|--------------|--|--------------|
| DEVICE S/N  | $T_1$ (HRS.) | DEVICE S/N  | $T_1$ (HRS.) | DEVICE S/N   | $T_1$ (HRS.) |
| 1229G   | 11.1         | 1310G   | 44.75        | 1597G  | 84.2         |
| 1116B   | 12.8         | 1382B   | 46.1         | 1553B  | 84.3         |
| 680G  | 13.6         | 1428B   | 60.5         | 1563B  | 95.6         |
| 668G  | 22.25        | 1307B   | 65.2         | 1591G  | 165.5        |
| 362D  | 24.5         | 1318G   | 81.6         | 1582G  | 170.5        |
| 366D  | 25.8         | 1303B   | 87.7         | 1500B  | 191.4        |
| 685G  | 32.8         | 1300B   | 93.2         | 1555B  | 191.4        |
| 1231G   | 38.5         | 1392B   | 93.4         | 1579G  | 191.6        |
| 514G  | 44.8         | 1301B   | 105.2        | 1588G  | 218.8        |
| 1188G   | 45.6         | 1314G   | 114.0        | 1580G  | 273.0        |
| 1106B   | 46.1         | 1317G   | 122.75       | 1559B  | 285.0        |
| 1180G   | 48.8         | 1430B   | 147.2        | 1586G  | 287.35       |
| 470G  | 48.8         | 1316G   | 159.15       | 1589G  | 287.4        |
| 1223G   | 55.6         | 1385B   | 189.8        | 1499B  | 336.6        |
| 1220G   | 65.8         | 1389B   | 243.2        | 1497B  | 356.05       |
| 1254M   | 70.7         | 1313G   | 262.3        | 1552B  | 373.2        |
| 1237G   | 80.2         |   |              | 1549B  | 435.65       |
| 1264M   | 80.7         |   |              | 1581G  | 435.7        |
| 1177G   | 147.8        |   |              |  |              |

$N_T = 53$

DC ACCELERATED STRESS TEST DATA FOR  
20 GHz GROWN-JUNCTION GAAS IMPATT DIODES



EARLY FAILURES REMOVED

| HIGH TEMPERATURE<br>( $T_H = 340^\circ\text{C}$ )<br>N=13 |              | MID. TEMPERATURE<br>( $T_M = 321^\circ\text{C}$ )<br>N=20 |              | LOW TEMPERATURE<br>( $T_L = 304^\circ\text{C}$ )<br>N=18 |              |
|---|--------------|---|--------------|--|--------------|
| DEVICE S/N  | $T_1$ (HRS.) | DEVICE S/N  | $T_1$ (HRS.) | DEVICE S/N   | $T_1$ (HRS.) |
| 33  | 12.8         | 25  | 46.15        | 44   | 121.2        |
| 1   | 12.9         | 18  | 46.65        | 16   | 121.45       |
| 32  | 16.05        | 27  | 72.7         | 39   | 167.2        |
| 18  | 20.3         | 21  | 94.55        | 6  | 207.35       |
| 7   | 35.2         | 22  | 94.7         | 11   | 334.5        |
| 3   | 47.75        | 35  | 103.05       | 13   | 334.6        |
| 16  | 48.6         | 34  | 106.5        | 8  | 420.8        |
| 24  | 48.85        | 28  | 158.95       | 14   | 428.0        |
| 17  | 49.0         | 50  | 161.7        | 2  | 523.1        |
| 32  | 110.2        | 48  | 167.55       | 4  | 525.35       |
| 18  | 110.65       | 55  | 275.45       | 15   | 548.85       |
| 4   | 201.75       | 33  | 334.0        | 9  | 556.5        |
| 22  | 202.0        | 41  | 369.0        | 10   | 693.2        |
|   |              | 47  | 384.4        | 1  | 740.7        |
|   |              | 42  | 389.9        | 5  | 781.15       |
|   |              | 36  | 488.7        | 52   | 781.3        |
|   |              | 31  | 533.3        | 7  | 844.15       |
|   |              | 32  | 623.7        | 19   | 844.2        |
|   |              | 30  | 695.9        |  |              |
|   |              | 37  | 696.9        |  |              |

$N_T = 51$

DC ACCELERATED STRESS TEST DATA FOR  
20 GHz GROWN-JUNCTION GAAS IMPATT DIODES

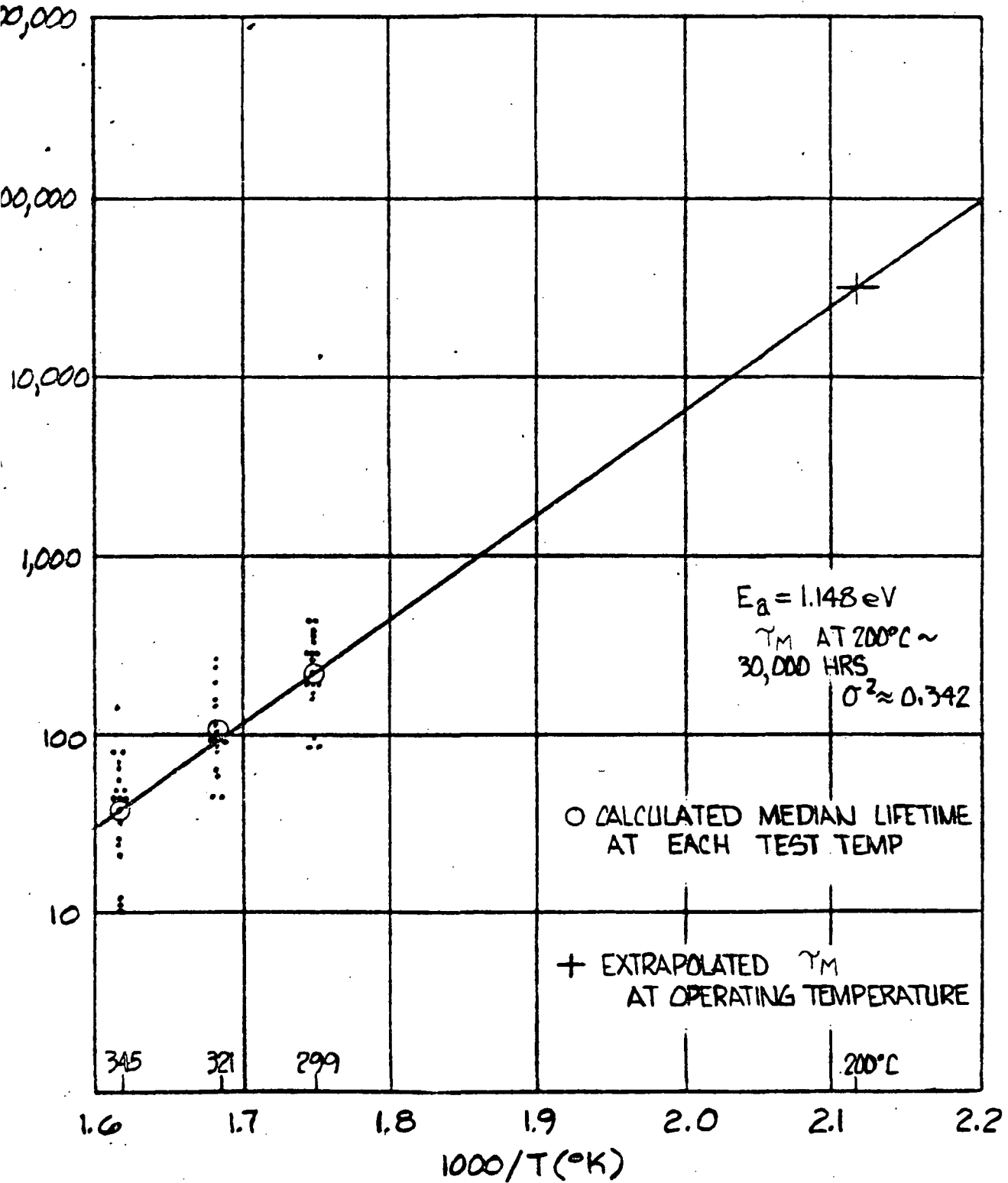


| HIGH TEMPERATURE<br>( $T_H = 340^\circ\text{C}$ )<br>N = 20 |              | MID. TEMPERATURE<br>( $T_M = 321^\circ\text{C}$ )<br>N = 20 |              | LOW TEMPERATURE<br>( $T_L = 304^\circ\text{C}$ )<br>N = 20 |              |
|---|--------------|---|--------------|--|--------------|
| DEVICE S/N  | $T_1$ (HRS.) | DEVICE S/N  | $T_1$ (HRS.) | DEVICE S/N   | $T_1$ (HRS.) |
| 19  | 0            | 25  | 46.15        | 53   | 13.8         |
| 35  | 0            | 18  | 46.65        | 12   | 39.8         |
| 36  | 0            | 27  | 72.7         | 44   | 121.2        |
| 8   | 0            | 21  | 94.55        | 16   | 121.45       |
| 31  | 0.5          | 22  | 94.7         | 39   | 167.2        |
| 37  | 1.0          | 35  | 103.05       | 6  | 207.35       |
| 17  | 2.5          | 34  | 106.5        | 11   | 334.5        |
| 33  | 12.8         | 28  | 158.95       | 13   | 334.6        |
| 1   | 12.9         | 50  | 161.7        | 8  | 420.8        |
| 32  | 16.05        | 48  | 167.55       | 14   | 428.0        |
| 18  | 20.3         | 55  | 275.45       | 2  | 523.1        |
| 7   | 35.2         | 33  | 334.0        | 4  | 525.35       |
| 3   | 47.75        | 41  | 369.0        | 15   | 548.85       |
| 16  | 48.6         | 47  | 384.4        | 9  | 556.5        |
| 24  | 48.85        | 42  | 389.9        | 10   | 693.2        |
| 17  | 49.0         | 36  | 488.7        | 1  | 740.7        |
| 32  | 110.2        | 31  | 533.3        | 5  | 781.15       |
| 18  | 110.65       | 32  | 623.7        | 52   | 781.3        |
| 4   | 201.75       | 30  | 695.9        | 7  | 844.15       |
| 22  | 202.0        | 37  | 696.9        | 19   | 844.2        |

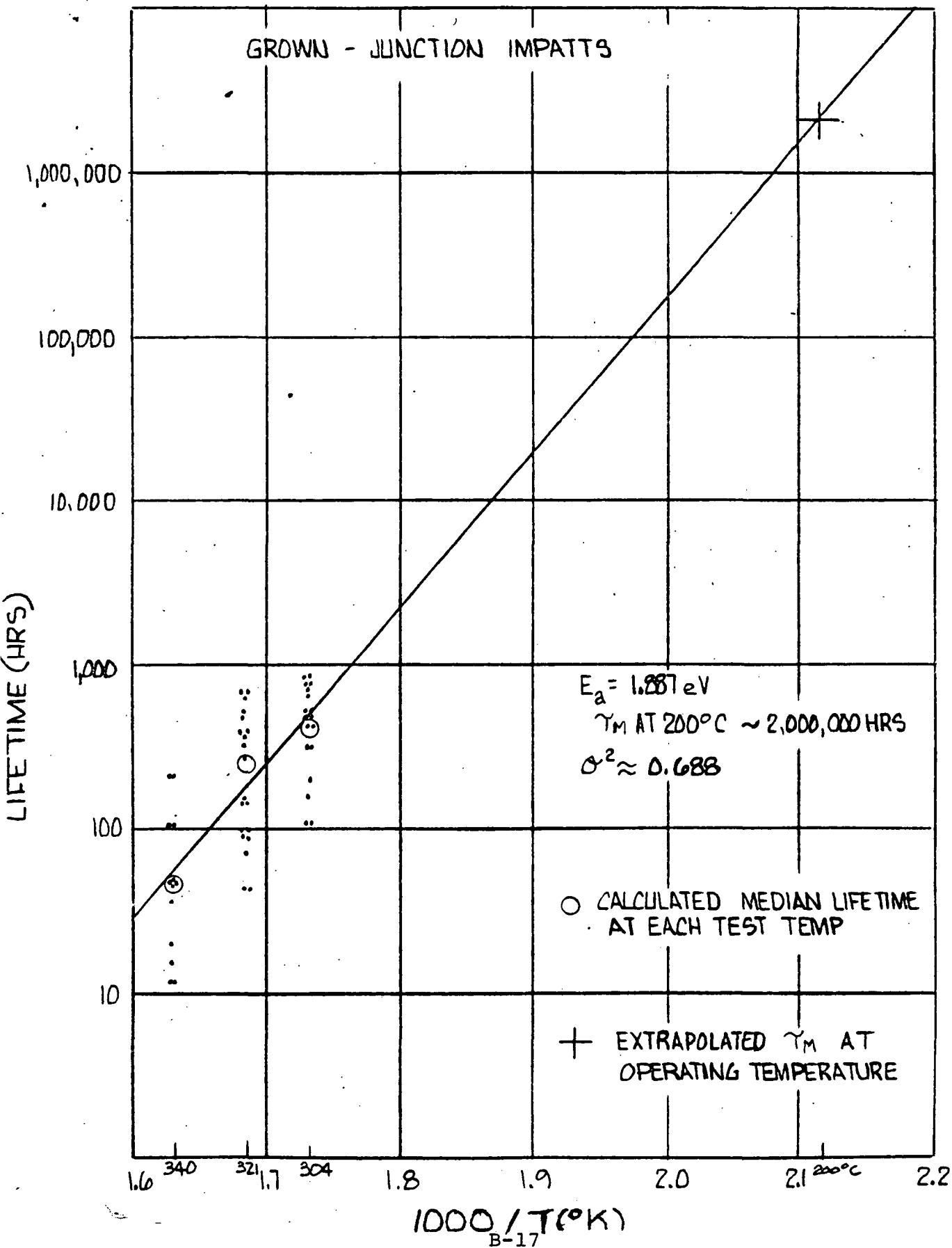
# ARRHENIUS (REGRESSION) LINE PLOT



## SCHOTTKY-BARRIER IMPATT'S



# ARRHENIUS (REGRESSION) LINE PLOT



# COMPUTER PRINTOUT FOR SCHOTTKY BARRIER ANALYSIS

LNR COMMUNICATIONS, INC.  
G.L. BRECHT JAN 1984

|             |                              |
|-------------|------------------------------|
| USER'S NAME | M. WALDMAN                   |
| DATE        | 2/28/84                      |
| PROJECT NO. | SCHOTTKY BARRIER, N=19,16,18 |

DEFINITION OF VARIABLES  
 XSUM=SUM OF ALL X VALUES  
 YSUM=SUM OF ALL Y VALUES  
 XYSUM=SUM OF PRODUCTS OF ALL X AND Y PAIRS  
 X2SUM=SUM OF ALL X VALUES SQUARED  
 Y2SUM=SUM OF ALL Y VALUES SQUARED  
 XBAR=AVERAGE OF THE X VALUES  
 YBAR=AVERAGE OF THE Y VALUES  
 S2=VARIANCE  
 S =STANDARD DEVIATION

TO CONVERT X ENTER THE NO.

- 1) NONE
- 2) TO NATURAL LOG (LN)
- 3) TO LOG BASE 10 (LOG)
- 4) TO 1/DEGK (1/273+C)
- 5) OTHER

TO CONVERT Y ENTER THE NO.

- 1) NONE
- 2) TO NATURAL LOG (LN)
- 3) TO LOG BASE 10 (LOG)
- 4) OTHER

HOW MANY PAIRS?53

ENTER DATA

ANY CORRECTIONS?NO

53 PAIRS

|  |
|--|
| XSUM=.0891488952   |
| YSUM=241.335455  |
| XYSUM=.488822817   |
| X2SUM=1.58189879E-04   |
| Y2SUM=1144.8932  |
| XBAR=1.68285463E-03  |
| YBAR=4.53349915  |
| CORRELATION=.783482387 OR X'S AND Y'S ARE 78.3482387% CORRELATED |
| REGRESSION LINE SLOPE=13306.7854 $E_a = 1.148 \text{ eV}$        |
| Y INTERCEPT=-17.8291862  |
| VARIANCE=.342141945  |
| STD DEV=.584722889   |

MEAN TIME TO FAILURE (MTTF) AND  
CONFIDENCE INTERVAL (CI)

TC=OPERATING TEMP IN DEG C  
 MTTF(M)=MEDIAN TIME TO FAILURE  
 CI=CONFIDENCE INTERVAL  
 ST=VALUE FROM STUDENT T DISTRIBUTION  
 CHI=VALUE FROM CHI-SQUARE DISTRIBUTION  
 LV=LOGARITHMIC VARIANCE  
 PRESS RETURN TO CONTINUE  
 OPER TEMP DEG C200

MTTF(M)=29828.5852 HOURS AT 200 DEG C

FOR MTTF AT OTHER CONF INTERVALS  
 ENTER ST FROM THE STUDENT T TABLE AT  
 NUMBER OF PAIRS MINUS 2 (P-2) AND CI  
 P-2=51  
 ENTER CI%=98  
 ST=1.2985

MTTF=OR)12929.4889 HOURS AT 200 DEG C  
FOR A 98% CONFIDENCE INTERVAL

LIFETIME OF A SINGLE FUTURE UNIT  
 TTF=OR)9648.76951 HOURS AT 200DEG C  
 FOR A 98% CONFIDENCE INTERVAL

FOR LOGARITHMIC VARIANCE  
 ENTER VALUES (CHI) FROM CHI-SQUARE TABLE  
 P-2=51  
 LOWER BOUND=5%  
 UPPER BOUND=95%  
 ENTER LOWER BOUND CHI68.669  
 ENTER UPPER BOUND CHI135.600

.254186499=OR) LV (OR)4.98147169  
FOR A 98% CONFIDENCE INTERVAL

# COMPUTER PRINTOUT FOR GROWN JUNCTION ANALYSIS

LNR COMMUNICATIONS, INC.  
G.L. BRECHT JAN 1984

|             |                             |
|-------------|-----------------------------|
| USER'S NAME | M. WALDMAN                  |
| DATE        | 2/23/84                     |
| PROJECT NO. | GROWN-JUNCTION, N=13,28,18. |

DEFINITION OF VARIABLES  
XSUM=SUM OF ALL X VALUES  
YSUM=SUM OF ALL Y VALUES  
XYSUM=SUM OF PRODUCTS OF ALL X AND Y PAIRS  
X2SUM=SUM OF ALL X VALUES SQUARED  
Y2SUM=SUM OF ALL Y VALUES SQUARED  
XBAR=AVERAGE OF THE X VALUES  
YBAR=AVERAGE OF THE Y VALUES  
S2=VARIANCE  
S =STANDARD DEVIATION

TO CONVERT X ENTER THE NO.

- 1) NONE
- 2) TO NATURAL LOG (LN)
- 3) TO LOG BASE 10 (LOG)
- 4) TO 1/DEGK (1/273+C)
- 5) OTHER

TO CONVERT Y ENTER THE NO.

- 1) NONE
- 2) TO NATURAL LOG (LN)
- 3) TO LOG BASE 10 (LOG)
- 4) OTHER

HOW MANY PAIRS?

ENTER DATA  
ANY CORRECTIONS?NO  
51 PAIRS

|                        |  |
|------------------------|--|
| XSUM=                  | .8868234515  |
| YSUM=                  | 265.782275   |
| XYSUM=                 | .449981964   |
| X2SUM=                 | 1.45175397E-04                                       |
| Y2SUM=                 | 1455.52344   |
| XBAR=                  | 1.68673434E-03                                       |
| YBAR=                  | 5.21141715   |
| CORRELATION=           | .722817472 OR X'S AND Y'S ARE 72.2817472% CORRELATED |
| REGRESSION LINE SLOPE= | 21879.5897 $E_a = 1.987 \text{ eV}$                  |
| Y INTERCEPT=           | -31.6936383  |
| VARIANCE=              | .687958117   |
| STD DEV=               | .829432406   |

MEAN TIME TO FAILURE (MTTF) AND  
CONFIDENCE INTERVAL (CI)

TC=OPERATING TEMP IN DEG C  
MTTF(M)=MEDIAN TIME TO FAILURE  
CI=CONFIDENCE INTERVAL  
ST=VALUE FROM STUDENT T DISTRIBUTION  
CHI=VALUE FROM CHI-SQUARE DISTRIBUTION  
LV=LOGARITHMIC VARIANCE  
PRESS RETURN TO CONTINUE  
OPER TEMP DEG C200

MTTF(M)=2111864.97 HOURS AT 200 DEG C

FOR MTTF AT OTHER CONF INTERVALS  
ENTER ST FROM THE STUDENT T TABLE AT  
NUMBER OF PAIRS MINUS 2 (P-2) AND CI  
P-2=49  
ENTER CI%=90  
ST=1.299

MTTF=OR>397638.431 HOURS AT 200 DEG C  
FOR A 90% CONFIDENCE INTERVAL

LIFETIME OF A SINGLE FUTURE UNIT  
TTF=OR>289485.351 HOURS AT 200DEG C  
FOR A 90% CONFIDENCE INTERVAL

FOR LOGARITHMIC VARIANCE  
ENTER VALUES (CHI) FROM CHI-SQUARE TABLE AT  
P-2=49  
LOWER BOUND=5%  
UPPER BOUND=95%  
ENTER LOWER BOUND CHI66.339  
ENTER UPPER BOUND CHI33.930

.508146757=OR< LV <OR=.993514522  
FOR A 90% CONFIDENCE INTERVAL

References:

- (1) W.A. Johnson and M.F. Millea, "Statistical Analysis of Accelerated Temperature Aging of Semiconductor Devices," Interim Report SD-TR-81-37, May 15, 1981.
- (2) W. Nelson, "Analysis of Accelerated Life Test Data, Methods for Complete Data - Part II; Numerical Methods and Test Planning." IEEE Trans. Elec. Insul., Vol EI-7, pp. 36-55, March 1972.
- (3) J.H. Zar, Biostatistical Analysis, Prentice-Hall Inc., NJ 1974.
- (4) IEEE Standards Committee, "IEEE Guide for the Statistical Analysis of Thermal Life Test Data," IEEE standard 101-1972 (reaffirmed 1980), IEEE Inc, NY March 17, 1972.

APPENDIX 'C'

THERMAL EFFECT AND LIMITATIONS OF  
HIGH TEMPERATURE RF STRESS TEST

December, 1983

LNR COMMUNICATIONS, INC.

180 Marcus Blvd.  
Hauppauge, NY 11788



THERMAL EFFECT AND LIMITATIONS OF HIGH TEMPERATURE  
RF STRESS TEST

While performance degradations of semiconductor devices in general are expected at elevated temperatures, the degradation is reversible in principle. The initial stress test data and subsequent experimental data indicated some significant irreversible physical changes resulting during moderate high temperature cycling of 20 GHz GaAs IMPATT diodes.

The design of an accelerated RF stress test is a function of the thermal stability of the device under test in order to maintain device oscillation with only minor adjustments in circuit tuning. In order to determine the high temperature effects on the performance of the GaAs IMPATTs as a function of the semiconductor physics, some simple calculations were made. The calculated results and predictable performance degradation formed the basis for an initial accelerated RF stress design concept. However, the actual device degradation did not follow the calculated diode performance prediction.

The ionization rate  $\alpha$  decreases with increases in temperature. A graph, showing the relation of the ionization coefficient with temperature, was generated from the expression,

$$\alpha = a \exp \left[ -(b/E)^2 \right]$$

where

$$a = 1.61 \times 10^5 \left[ 1 + 7 \times 10^{-4} (t - 25^\circ\text{C}) \right] \text{ cm}^{-1} = \text{Constant (measured)}$$

$$b = 5.41 \times 10^5 \left[ 1 + 9.7 \times 10^{-4} (t - 25^\circ\text{C}) \right] \text{ V}_{\text{cm}}^{-1} = \text{constant (measured)}$$

E = Electric field, V/cm

The decreased ionization rate results in an increase of the depletion width, causing in effect a higher breakdown voltage ( $V_B$ ) as can be seen from

$$\int \alpha(E) dx = 1$$

$$\int_0^{W_D} E(x) dx = V_B$$

where ;

x = refers to distance along the direction of avalanching.

$W_D$  = is the depletion width at breakdown.

A high-low IMPATT doping profile was used to calculate changes in DC device parameters resulting from changes in temperature.

| Temp. (°C) | $W_D$ (μm) | $E_{max}$ (kV/cm) | $V_D$ (V) | $V_B$ (V) = $V_A + V_D$ | $\left(\frac{1}{\pi}\right) \frac{V_D}{V_B}$ |
|------------|------------|-------------------|-----------|-------------------------|--|
| 200        | 1.05       | -76.8             | 11.3      | 21.3                    | 17%  |
| 250        | 1.15       | -78.2             | 12.9      | 23.3                    | 17.6%  |
| 300        | 1.27       | -79.8             | 15.1      | 25.8                    | 18.6%  |

Furthermore, the device conversion efficiency is given by

$$\eta = \left(\frac{1}{\pi}\right) \frac{V_D \sin(\pi/2W_D/W_{\pi})}{(V_A + V_D) (W_D/W_{\pi})}$$

where  $W_{\pi} = V_s/2f$  corresponds to a transit angle. The scatter-limited velocity  $V_s$  decreases from  $V_s = 4 \times 10^6$  cm/sec at 500°K to  $V_s = 3.4 \times 10^6$  cm/sec at 600°K and with corresponding increases in  $W_D$ , the efficiency decreases to a value as low as nine percent at 500°K.

Finally, calculating the output power from

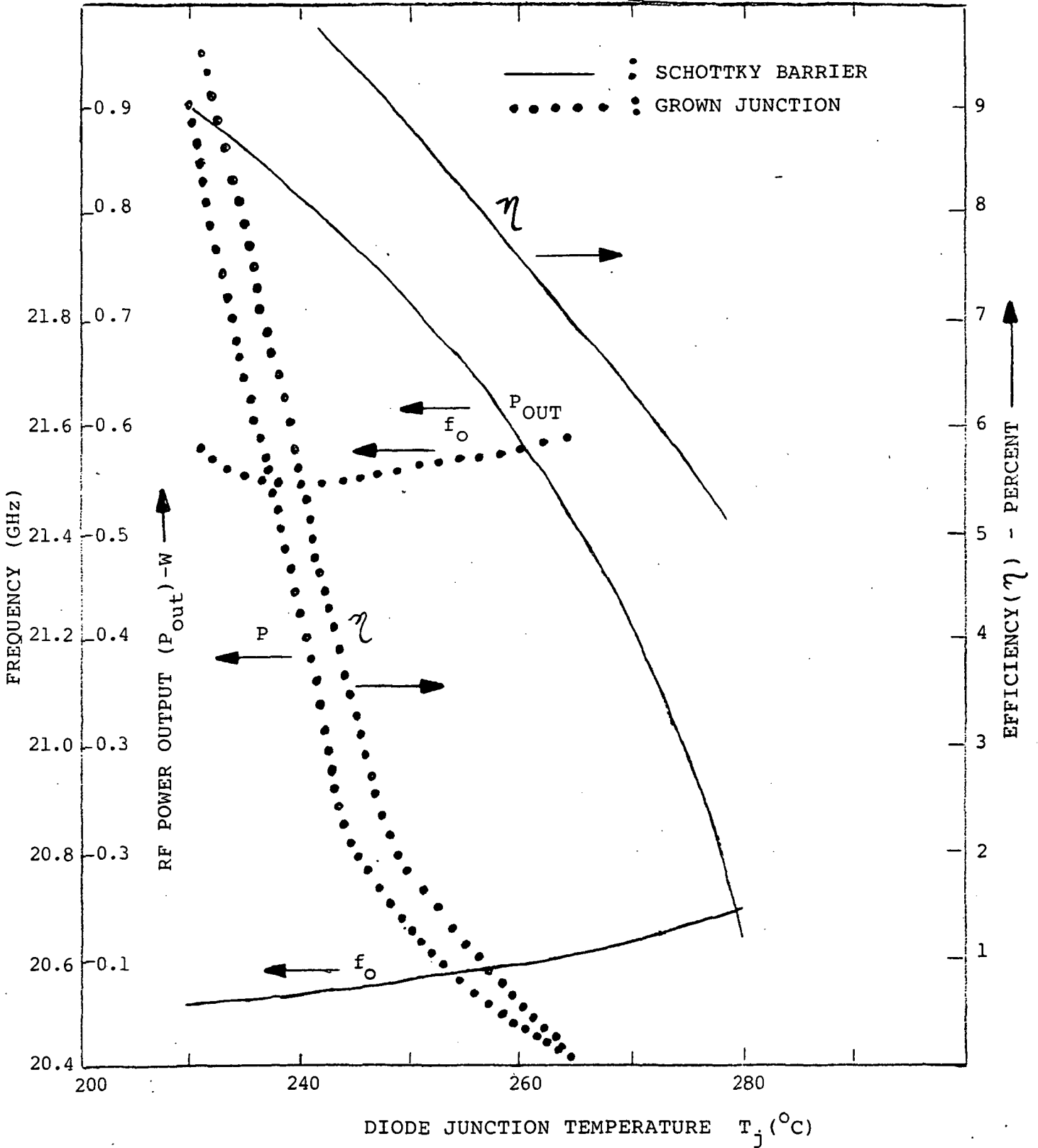
$$P_o = \frac{\eta}{1-\eta} \left( \frac{\Delta T_{max}}{\theta_{TH}} \right)$$

where values of  $\theta_{TH} = 25^{\circ}\text{C/W}$ , and  $\Delta T_{max} = T_j + 25^{\circ}\text{C}$  were assumed.

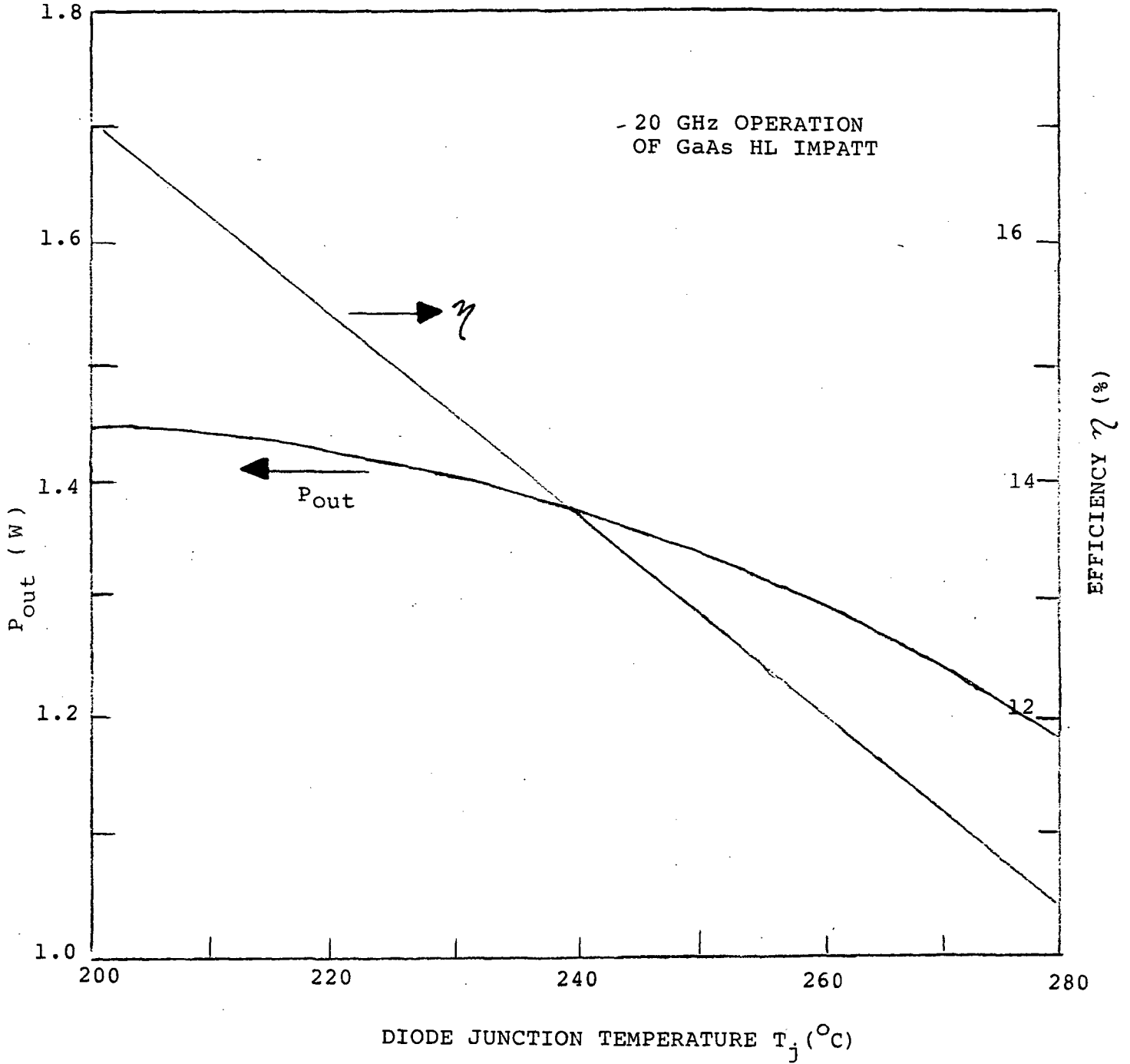
The output power and efficiency are plotted as a function of operating frequency ( $f_o$ ). Such operating assumes frequency optimized RF circuits. While a calculated degradation is evident the actual observed device degradation of both the grown junction and Schottky barrier device was much more severe. In fact the experienced degradation which resulted in the collapse of the oscillation mode inspite of careful and continuous circuit tuning, was irreversible.

Consequently, in conjunction with the stress test data, which indicated device degradation due to the compositional instability of the Au/Sn bond, a meaningful accelerated RF stress test design without implementing the recommended device modifications is not feasible.

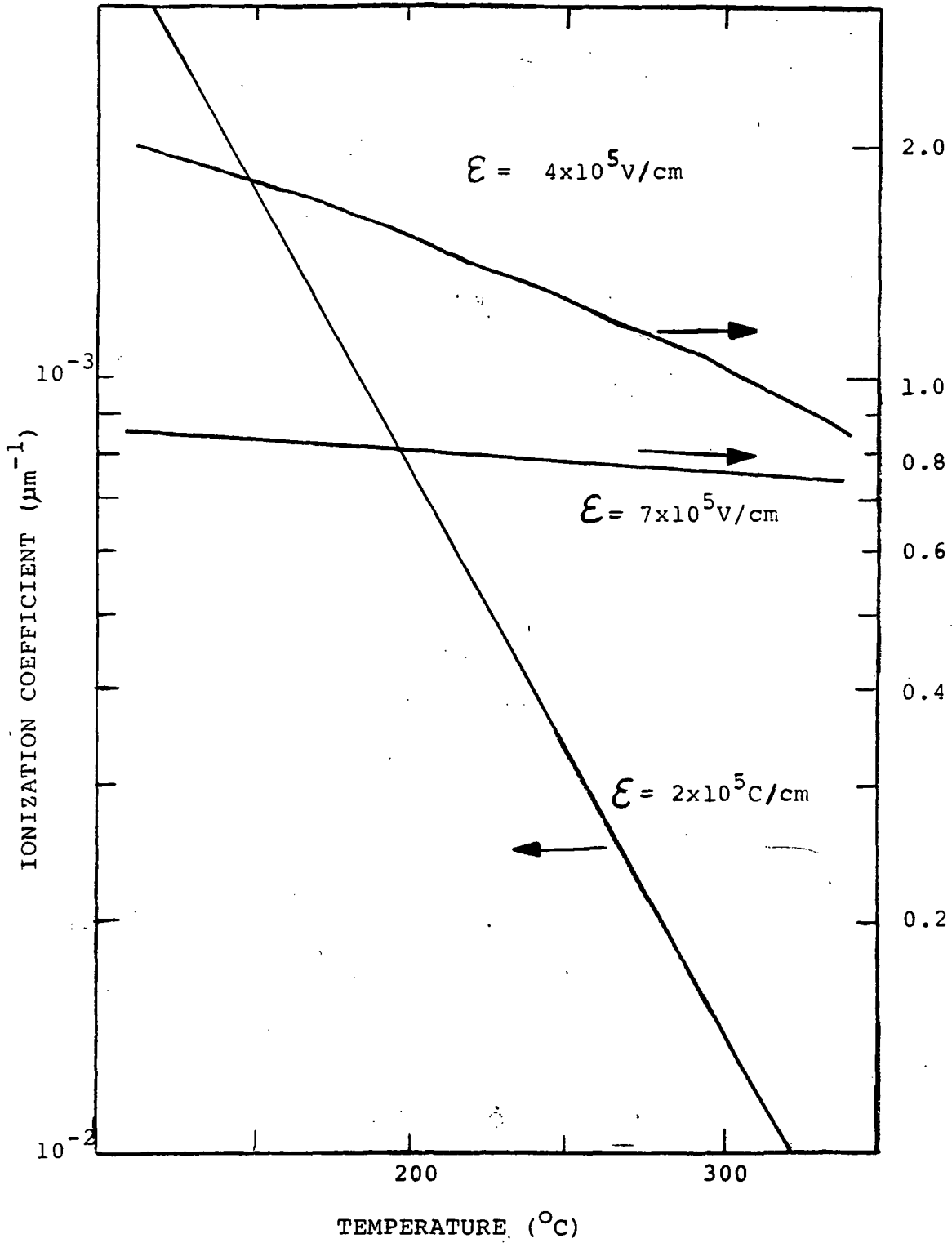
MEASURED RF PERFORMANCE AS A FUNCTION OF JUNCTION TEMPERATURE



CALCULATED RF PERFORMANCE CHARACTERISTICS OF  
20 GHz GaAs IMPATT AS A FUNCTION OF  
JUNCTION TEMPERATURE

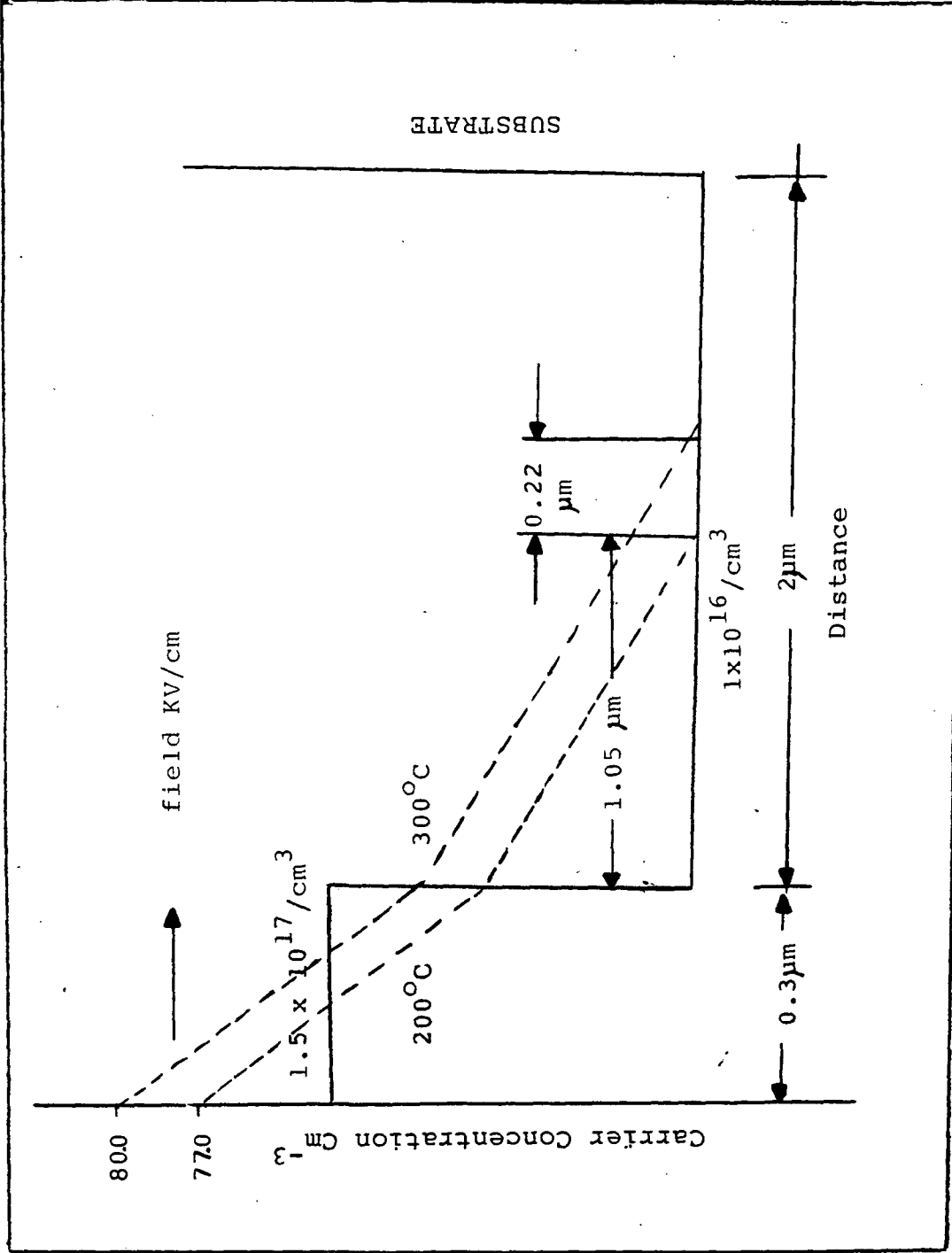


IONIZATION COEFFICIENT AS A  
FUNCTION OF TEMPERATURE FOR GAAs

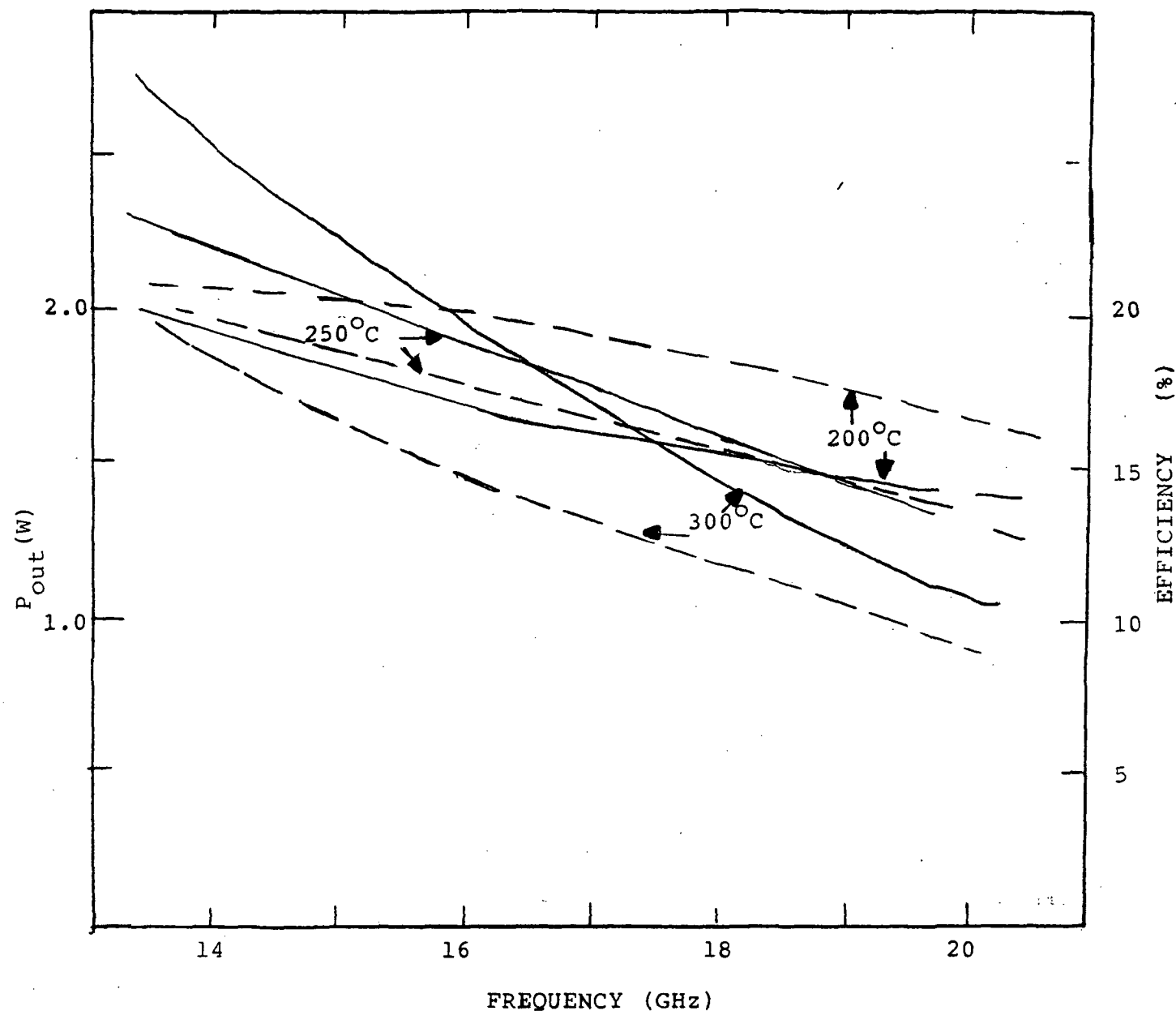


DOPING PROFILE AND ELECTRIC FIELD DISTRIBUTION  
ON HIGH LOW TYPE 20 GHZ GAAS IMPATT DEVICE

DOPING PROFILE AND ELECTRIC FIELD



CALCULATED POWER OUTPUT AND  
EFFICIENCY AS A FUNCTION OF FREQUENCY



CALCULATED  $P_{out}$  and  $\eta$  AS A  
FUNCTION OF FREQUENCY AT THREE  
DIFFERENT TEMPERATURES FOR 20  
GHz GaAs IMPATT.



F. TECHNOLOGY ASSESSMENT

FINAL REPORT

NASA CR 174716

APRIL, 1982

Prepared For:

NASA Lewis Research Center  
Cleveland, Ohio

CONTRACT NASA-NAS3-22491

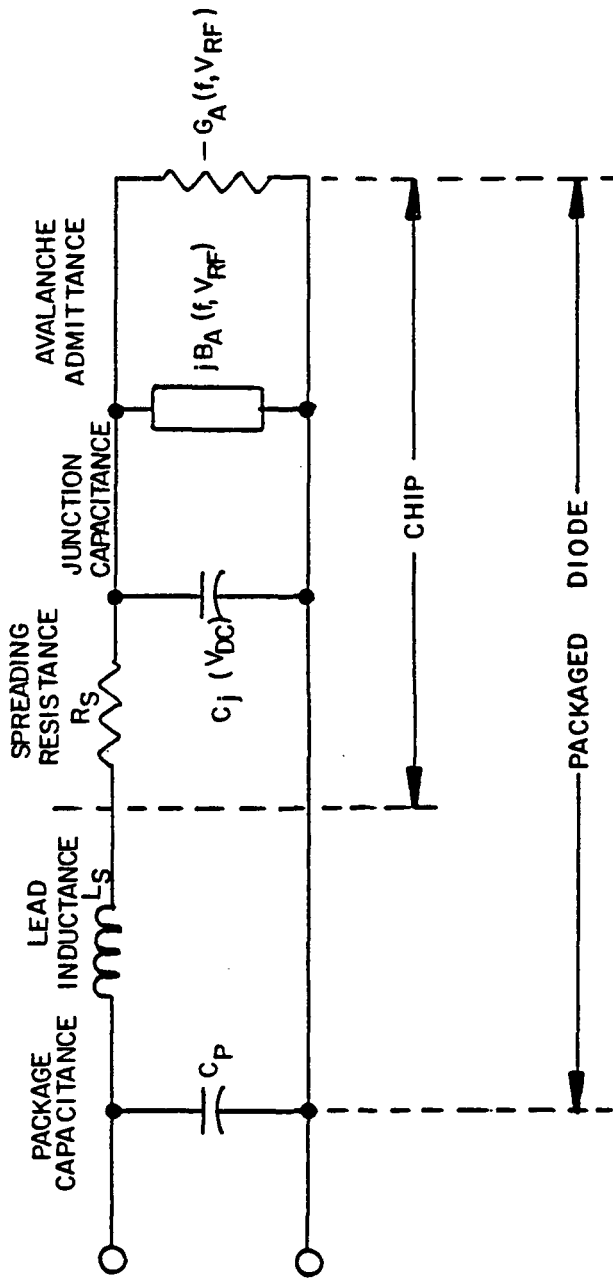
TABLE OF CONTENTS

- 1.0 Performance Assessment of POC IMPATT Technology
- 2.0 Performance Assessment of POC Combiner Technology
- 3.0 1987 IMPATT Transmitter Technology Assessment Study

## 1.0 Performance Assessment of POC IMPATT Technology

## KEY IMPATT DIODE PARAMETERS

1. GaAs Epi layer Doping Profile
2. Reverse Breakdown Voltage
3. Effective Mesa Area (Junction Capacitance)
4. Device Series Resistance
5. Thermal Resistance



GaAs READ-IMPATT DIODE EQUIVALENT CIRCUIT



METHODOLOGY FOR 20 GHZ IMPATT DIODE  
PERFORMANCE GROWTH PROJECTIONS

20 GHZ IMPATT Diode Performance Improvements  
Based Upon Optimization of:

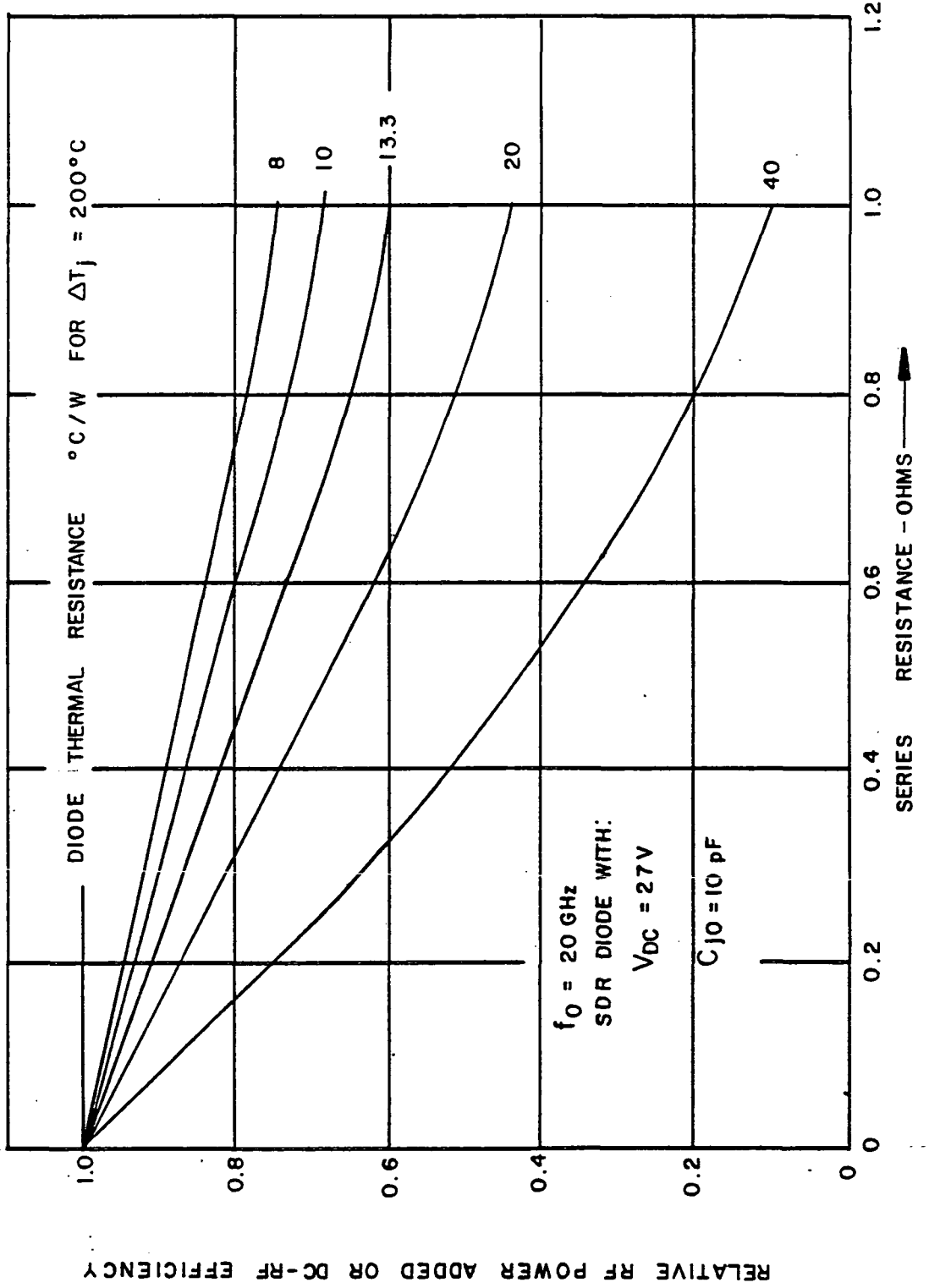
1. Read-IMPATT Doping Profile
  - . SDR vs DDR
  - . LHL vs HL
2. Junction Geometry
  - . Single vs multiple mesa
  - . Distributed mesa
3. Chip Processing
  - . Grown vs Schottky junction
  - . Contact metallization systems
  - . Etching procedure
  - . Chip thickness
4. Chip-Level Combining
  - . Series vs parallel
  - . Stabilization approach
5. Heat Sinking (Thermal Design)
  - . Minimization of thermal resistance
  - . Plated versus diamond heat sink (PHS vs DHS)

RATIONALE FOR 20 GHz IMPATT DIODE  
PERFORMANCE GROWTH PROJECTIONS

1. 1 Yr. Projections Based Upon:
  - . Short-term Read profile optimization within context of LHL, SDR configuration
  - . Single mesa
  - . Some reduction in chip  $R_s$
  - . DHS package
  - . Reduced package parasitics
2. 3 Yr. Projections Based Upon:
  - . More fundamental Read profile optimization, with possible utilization of DDR configuration
  - . Exploitation of premature collection mode
  - . Significant reduction in chip  $R_s$
  - . Multiple or distributed mesa, or,
  - . Dual chips/package
  - . Reduced package parasitics

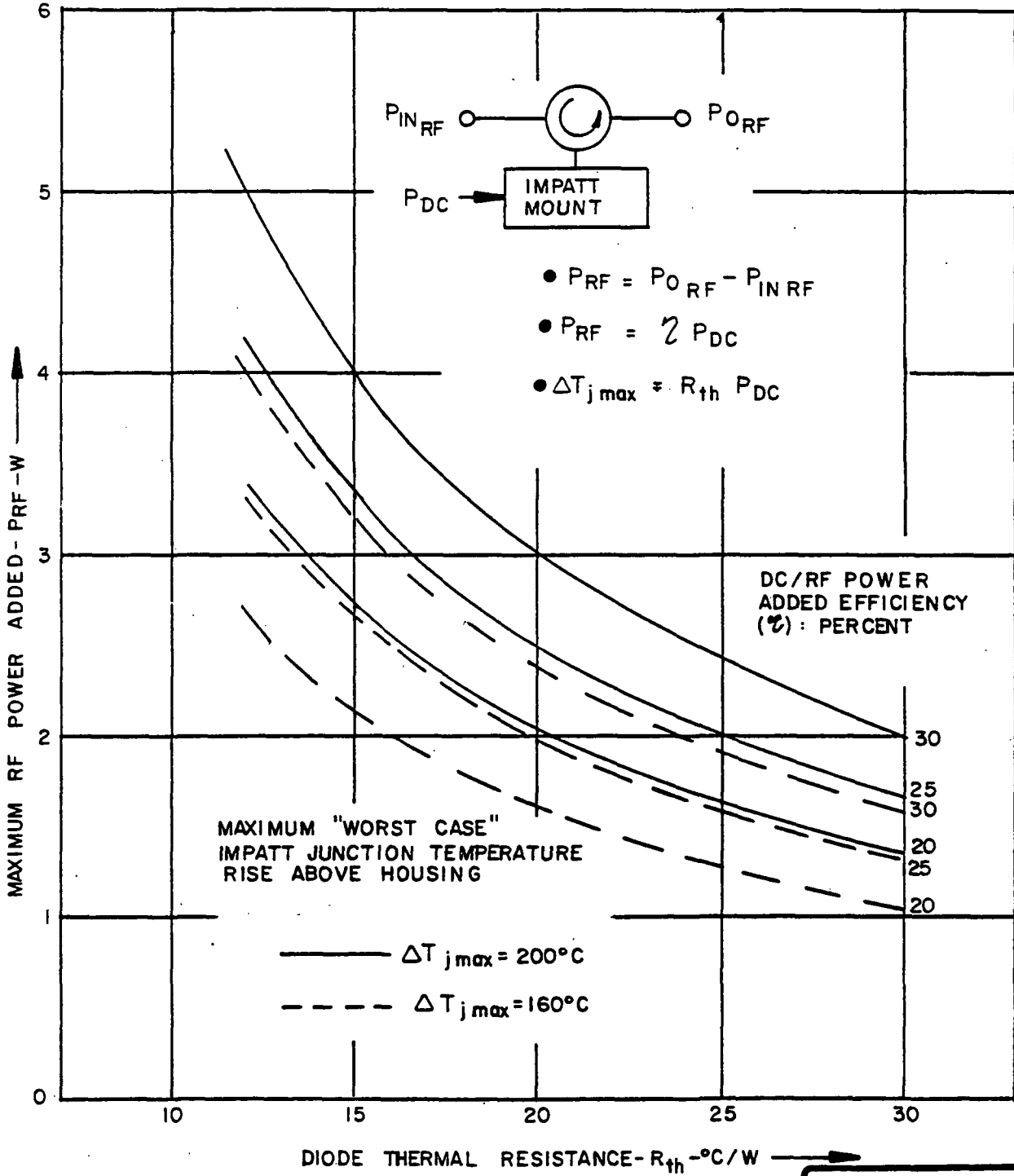


IMPACT OF DIODE SERIES RESISTANCE ON IMPATT AMPLIFIER PERFORMANCE

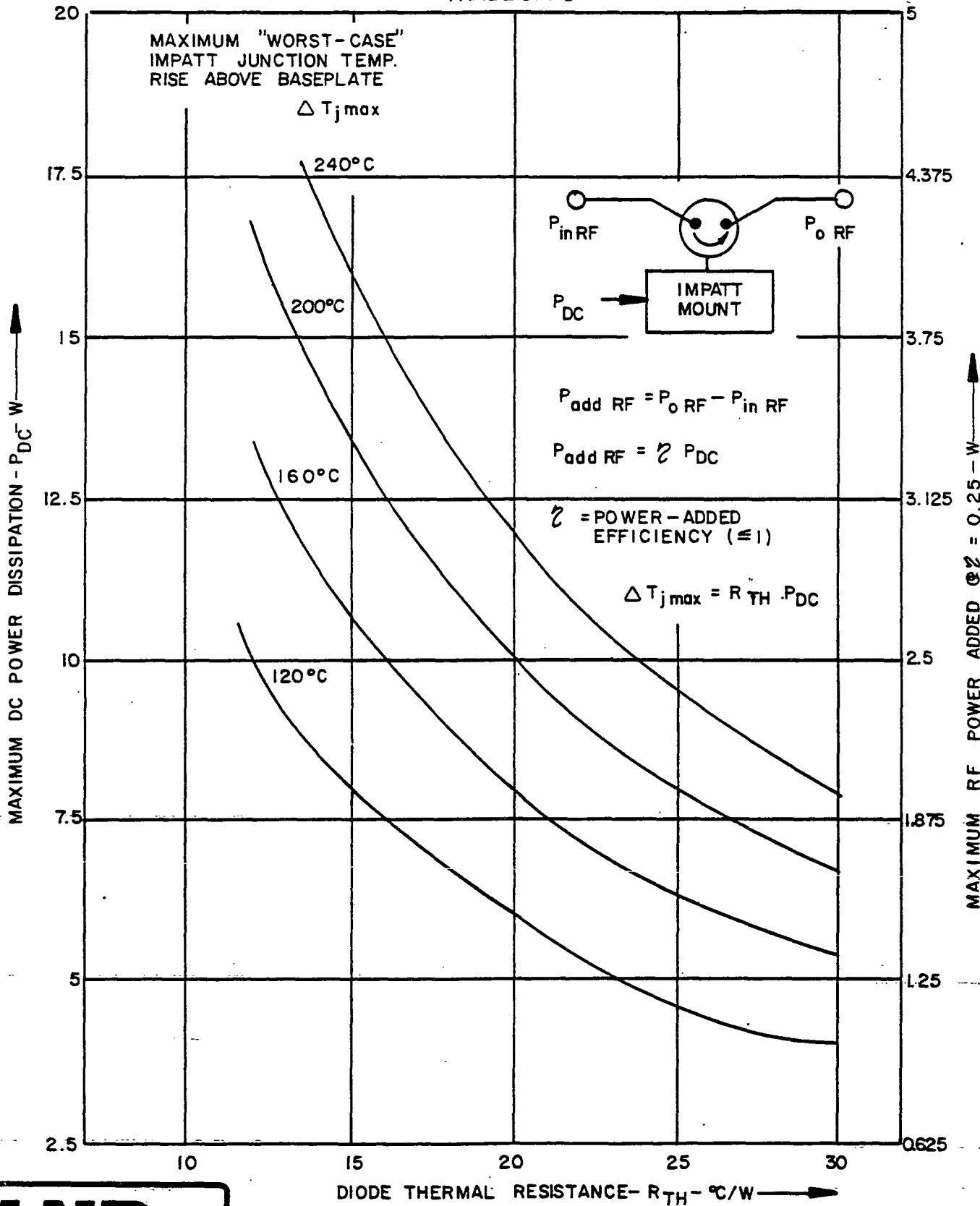




IMPATT DIODE RF POWER/EFFICIENCY VERSUS THERMAL RESISTANCE / JUNCTION TEMPERATURE



# IMPATT DIODE RF EFFICIENCY / POWER / THERMAL RESISTANCE TRADE OFFS



## 20 GHz IMPATT Diode Performance Growth Prospects

| Performance Parameters<br>(Stable Amplifier)                    | Time Period |           |           |
|---|-------------|-----------|-----------|
|   | Current     | 1 yr.     | 3 yrs.    |
| RF Power Output (W)   | 1.5 - 2.5   | 3.0 - 4.0 | 4.5 - 6.0 |
| RF Power Added (W)  | 1.0 - 1.5   | 2.0 - 2.5 | 3.5 - 4.0 |
| Operating Gain (dB)   | 3.0 - 4.0   | 4.0 - 5.0 | 4.5 - 6.0 |
| DC/RF Power Added<br>Efficiency - Percent                       | 15 - 20     | 20 - 22   | 22 - 25   |
| -1 dB Bandwidth-GHz   | 1.0 - 1.5   | 1.5 - 2.0 | 1.5 - 2.5 |
| Diode Thermal Resistance<br>°C/W                                | 20 - 30     | 16 - 20   | 8 - 12    |
| Diode Junction Temperature<br>Rise Above Baseplate (Max)<br>-°C | 150 - 200   | 150 - 210 | 150 - 220 |

CONCLUSIONS OF 20 GHz IMPATT DIODE  
PERFORMANCE GROWTH ASSESSMENT

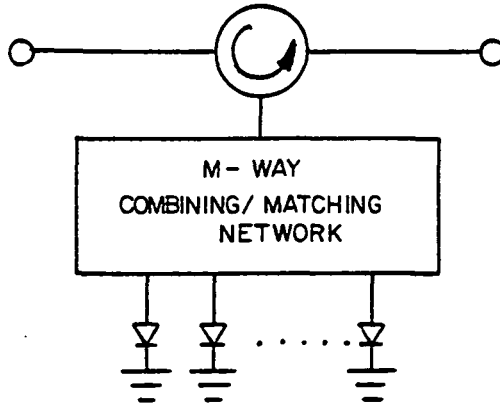
1. Near Term (1 Yr) Growth Prospects

- . Significant performance improvement within context of single-mesa, SDR, LHL-profile Read IMPATT device
- . Reduced package parasitics permit use of larger mesa with attendant decrease in  $R_s$  and increase in RF output power
- . Increase in efficiency based on reduction of  $R_s$  and further short-term Read profile optimization
- . utilization of DHS for reduction in thermal resistance

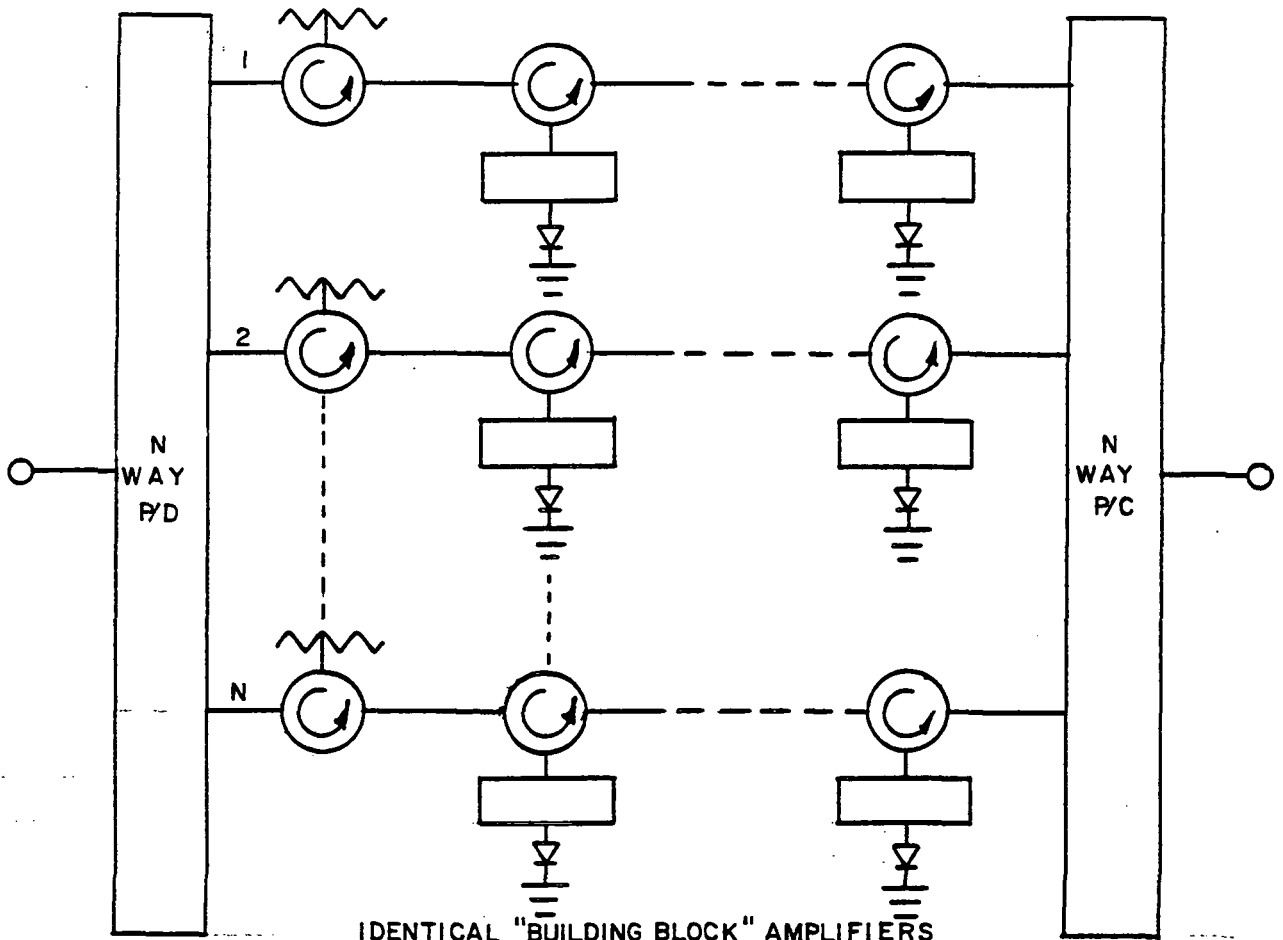
2. Long Term (3 Yr) Growth Prospects

- . Additional increase in performance capability requires more fundamental advance in IMPATT device characteristics
- . Higher RF power capability based upon use of multiple or distributed mesa chips, either singly or in dual chip per package configuration
- . Further increase in efficiency due to more fundamental Read profile optimization (including possible use of DDR) and significant reduction in  $R_s$
- . Concurrent reduction in thermal resistance due to combination of usage of DHS, larger mesa and/or multiple chip devices and chip thinning.

## 2.0 Performance Assessment of POC Combiner Technology



A - ACTIVE (INTRA STAGE) COMBINING



IDENTICAL "BUILDING BLOCK" AMPLIFIERS

B - PASSIVE (INTERSTAGE) COMBINING

IMPATT AMPLIFIER COMBINATORIAL CONFIGURATIONS

## IMPATT "POWER SECTION" AMPLIFIER COMBINATORIAL CONFIGURATIONS

### A. General Forms of Combination

#### 1. Active (intrastage) divider/combiner

- . most compact configuration
- . generally limited in bandwidth
- . prone to spurious mode oscillations
- . catastrophic degradation under random device failure
- . requires extremely closely matched IMPATTs
- . generally requires internal isolation resistance elements.

#### 2. Passive (interstage) divider/combiner

- . can be completely reactive for lowest residual insertion loss
- . potential wideband capability
- . can accomodate wide dispersion in device parameters
- . devices completely isolated from one another thus precluding multi-diode spurious mode oscillation
- . graceful degradation under random device failure
- . allows "power-down" operation to conserve prime power, by "turning off" selected building blocks.

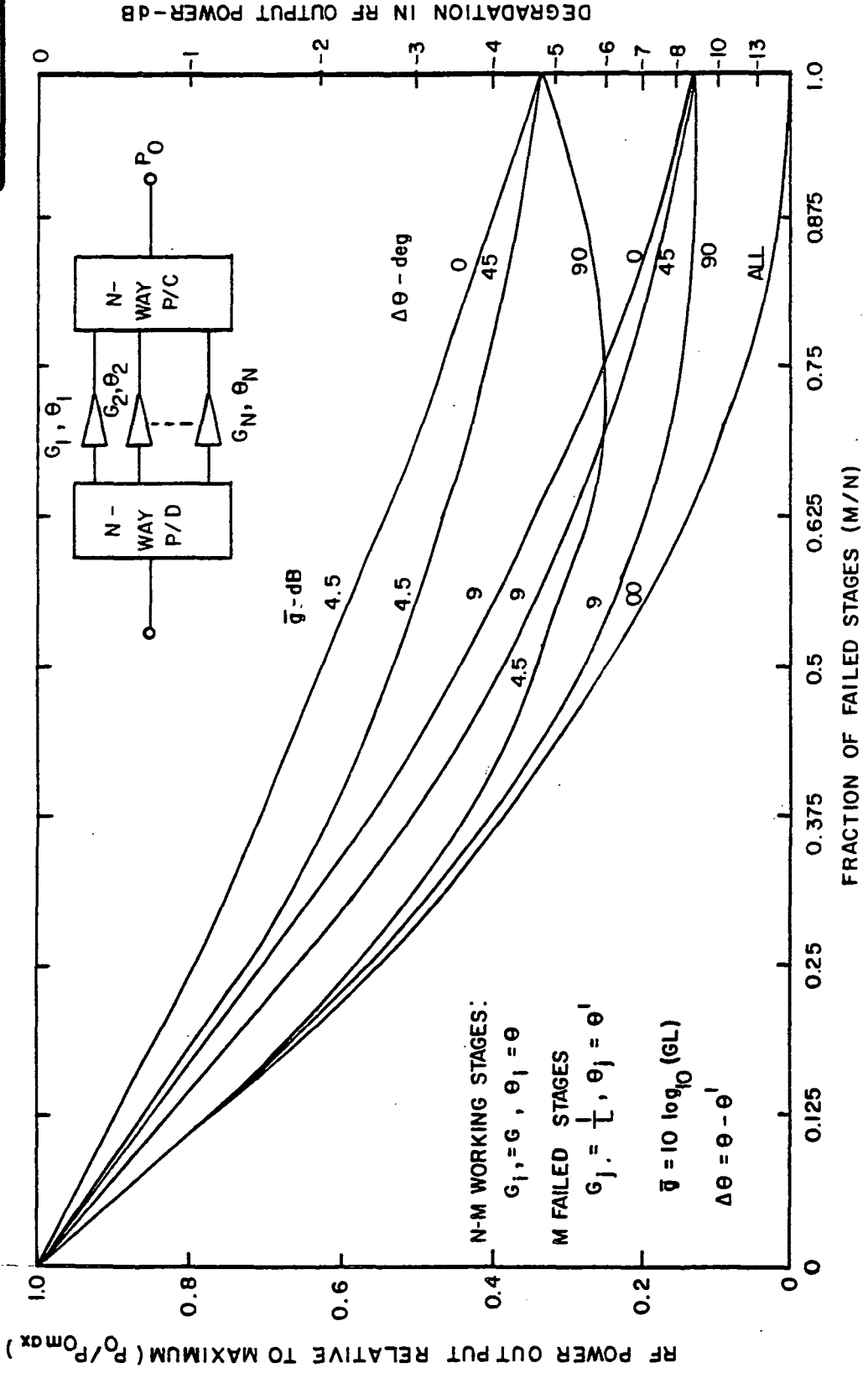
### B. Types of Combinatorial Networks

#### 1. Topology

- . corporate binary
- . N-way Wilkinson
- . reactive junction
- . extended interaction

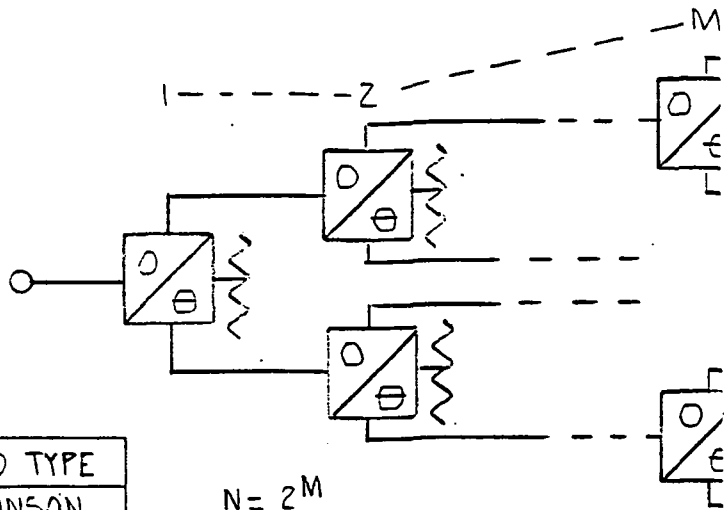
#### 2. Transmission media

- . waveguide
- . planar (microstrip, stripline)
- . radial or biconical (extended interaction).



GRACEFUL DEGRADATION PROPERTIES OF COMBINATORIAL POSTAMPLIFIER

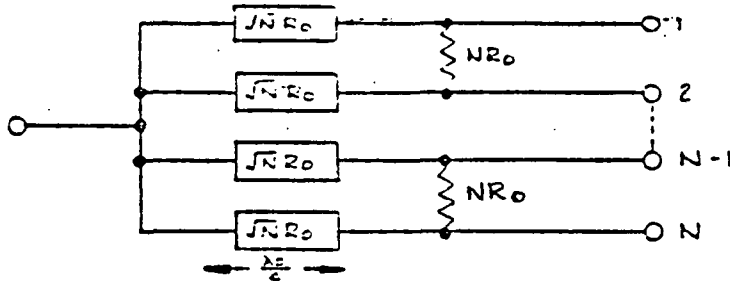




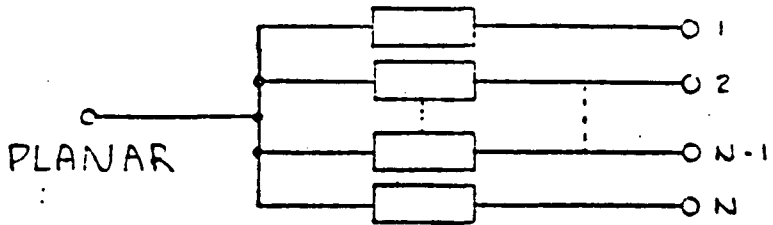
| $\theta$ DEG | HYBRID TYPE                         |
|--------------|-------------------------------------|
| 0            | WILKINSON                           |
| 90           | BRANCH-LINE<br>PLANGE<br>SHORT-SLOT |
| 180          | RAT-RACE                            |

$N = 2^M$

A. - CORPORATE BINARY COMBINING

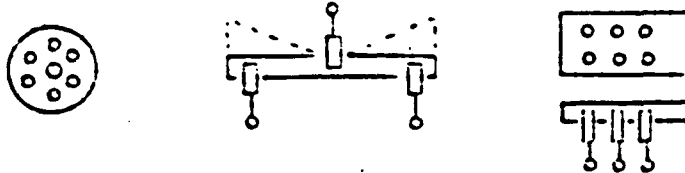


B. - N WAY WILKINSON COMBINING.



C. - N WAY REACTIVE JUNCTION COMBINING

RADIAL OR BICONICAL



D. - REACTIVE EXTENDED INTERACTION CAVITY

RELATIVE MERITS OF ALTERNATIVE 20 GHz POWER  
COMBINATORIAL CONFIGURATIONS

- . The corporate binary configurations in TEM line (in-phase/Wilkinson, quadrature/branch line and 0-180°/"rat-race") and waveguide (0-90°/short-slot or in phase/magic tee) all exhibit excessive size and residual insertion loss. Moreover the TEM configurations are somewhat difficult to implement at 20 GHz.
- . Generalization of the above to an N-way Wilkinson configuration results in a more compact TEM transmission line implementation (applicable to either passive or active combining) with moderate residual insertion loss and port to port isolation. Implementation of the series balancing resistors is extremely difficult, however, at 20 GHz.
- . A reactive junction configuration exhibits low insertion loss but no inherent port to port isolation and hence is only useable in passive combinatorial configurations with N circulator coupled "building blocks", such as the IMPATT amplifier stages. Within this category, the planar TEM junction is more compact and wider band but the waveguide junction exhibits the absolute minimum in insertion loss, and is easier to manufacture, align and accommodate in an N building block packaging concept.
- . The extended interaction reactive cavity configuration applicable to passive and active combining exhibits low loss, and narrow (radial and waveguide) to wider (biconical) bandwidth.
- . Preferred configuration for passive combining of 20 GHz circulator-coupled IMPATT "building blocks" is waveguide reactive junction.

METHODOLOGY FOR 20 GHz IMPATT AMPLIFIER COMBINATORIAL  
TECHNOLOGY PERFORMANCE ASSESSMENT

1. Assume following apportionment of passive and active RF power combining:
  - . active combining limited to maximum of two IMPATT chips (in individual or in single package(s)) per amplifier stage
  - . passive combining comprising N identical circulator coupled n-stage "building blocks" (n=1 or 2) paralleled between identical N-way power divider/combiners, of optimum waveguide reactive junction type.
2. Assume IMPATT diode parameters @ 20 GHz
  - .  $P_o = 1.5, 3, 6W/\text{chip}$
  - . Gain: 4.0-6 dB at nominal drive level
  - . RF/DC power added efficiency: 16, 20 and 25 percent
3. Compare alternative combiner configurations in conjunction with above diode parameters:
  - . using half, the same number and twice as many IMPATT diodes as in current POC model amplifier design
  - . providing 20W (current specification) and 40W (advanced capability) RF output power capability ( $P_{ORF}$ ) at 20 GHz.

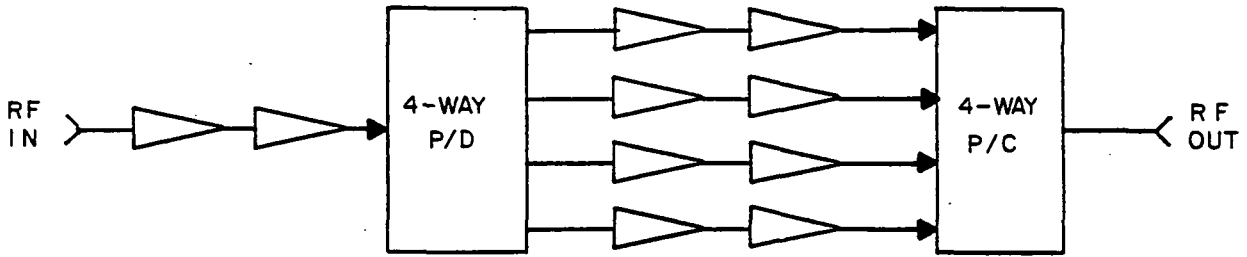
20 GHZ IMPATT COMBINATORIAL POSTAMPLIFIER  
CONFIGURATIONAL ALTERNATIVES

| Order of Combiner<br>(# of "building blocks")<br>N | # Stages/Building<br>Block<br>n | # IMPATT Chips<br>in each Building<br>Block Output Stage | Total<br>IMPATT Diode<br>Deployment  | Total RF<br>Power Output<br>W |
|--|---------------------------------|--|--------------------------------------|-------------------------------|
| 4*   | 2*                              | 2*   | 14 (total):<br>13 (3W) *<br>1 (1.5W) | 20W *                         |
| 4  | 2                               | 2  | 14 (total)<br>13 (6W)<br>1 (3W)      | 40W                           |
| 4<br>(19)  | 1                               | 1  | 6 (total)<br>5 (6W)<br>1 (1.5W)      | 20W                           |
| 8  | 2                               | 2  | 27 (1.5W)                            | 20W                           |
| 8  | 2                               | 2  | 27 (3W)                              | 40W                           |

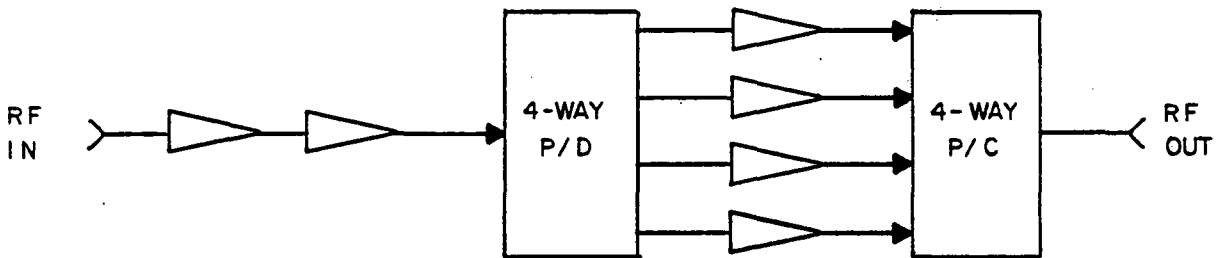
\*Current POC Model Design



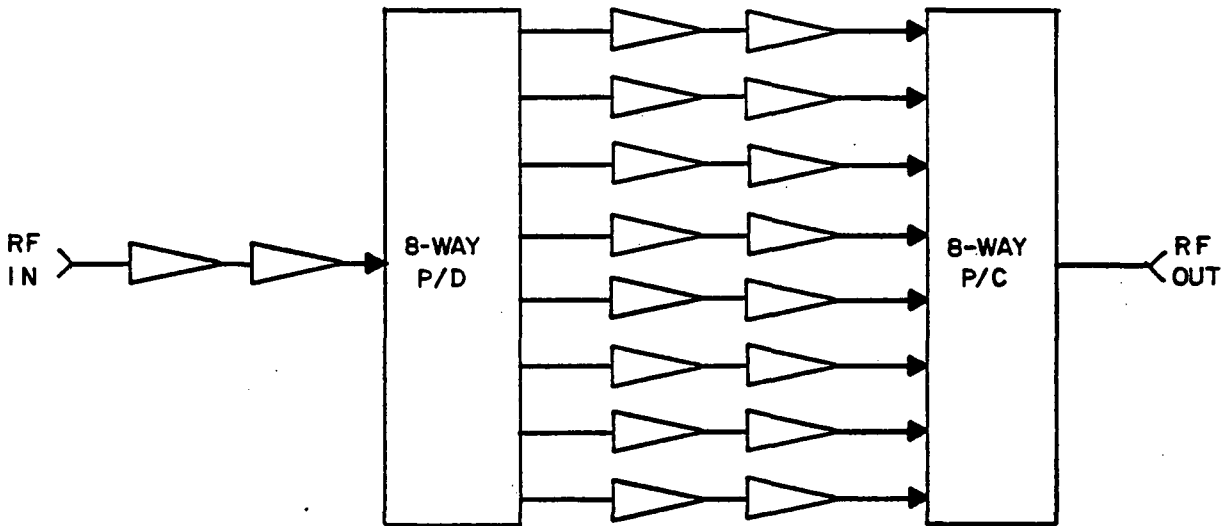
ALTERNATIVE IMPATT COMBINATORIAL POSTAMPLIFIER CONFIGURATIONS



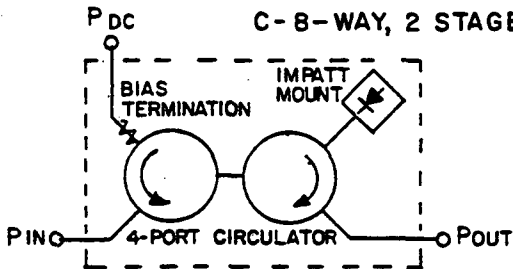
A - 4 WAY, 2-STAGE BUILDING BLOCK CONFIGURATION



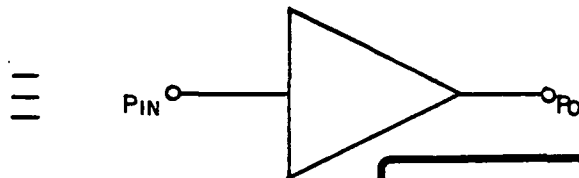
B - 4 WAY, SINGLE STAGE BUILDING BLOCK CONFIGURATION



C - 8-WAY, 2 STAGE BUILDING BLOCK CONFIGURATION



D - IMPATT AMPLIFIER STAGE MODEL



RATIONALE FOR 20 GHz IMPATT AMPLIFIER  
COMBINATORIAL TECHNOLOGY PERFORMANCE COMPARISON

1. Performance comparison based upon near-term and long term RF power output capability, e.g:
  - . 20W - representative of current POC model amplifier specification
  - . 40W - representative of potential IMPATT amplifier capability in the 1987 time frame.
2. Selection of IMPATT diode RF power output per chip, in combinatorial "building block" amplifier stage deployment, based upon:
  - . current to near term realizeability of 1.5 to 3W RF power output per chip, at 16 to 20 percent power added efficiency
  - . long term projection of 6W RF power output per chip, at 25 percent power added efficiency.
3. Selection of number of IMPATT chips used in each "building block" output stage based upon:
  - . maximum practical number of IMPATT diodes per amplifier stage limited to two, to minimize the impact of excessive combinatorial loss, stringent tolerances on diode parameters, catastrophic stage degradation on single device failure, and tendency toward spurious oscillations
  - . near term combining of two individually packaged IMPATT chips, and long term combining of two chips per diode package.

20 GHz IMPATT COMBINATORIAL POSTAMPLIFIER  
CONFIGURATIONAL PERFORMANCE TRADEOFFS

| Parameter  | Time Period |          |          |         |         |
|--|-------------|----------|----------|---------|---------|
|  | 0 - 1 Yr.   |          |          | 3 Yrs.  |         |
| Order of Combiner (N)  | 4           | 8        | 8        | 4       | 4       |
| # Stages/Building Block  | 2           | 2        | 2        | 1       | 2       |
| Building Block Gain-dB   | 9.0         | 9.0      | 9.0      | 5.6     | 9.0     |
| Building Block RF Power Output - W                               | 5.6         | 2.8      | 5.6      | 5.25    | 11.2    |
| RF Power-Added/Diode - W   | 1.8         | 0.9      | 1.8      | 3.6     | 4.0     |
| DC/RF Power Added Efficiency per diode - percent                 | 20          | 16       | 20       | 25      | 25      |
| Thermal Resistance per Diode (degrees C/W)                       | 18          | 25       | 18       | 10      | 10      |
| Maximum Diode Junction Temp. Rise above Baseplate (deg.C)        | 162         | 142      | 162      | 144     | 160     |
| Overall Gain (dB)  | 17.5        | 17.5     | 17.5     | 15      | 17.5    |
| Total RF Power Output (W)  | 21.5        | 21.5     | 43       | 20      | 43      |
| Total DC Power Drain (W)   | 124         | 152      | 245      | 88      | 196     |
| Overall DC-RF Power - Added Efficiency - Percent                 | 17          | 13.8     | 17       | 22      | 21.5    |
| Degradation in RF Output Power per "Building Block" Failure (dB) | 1.5-4.8     | 0.75-2.4 | 0.75-2.4 | 1.1-2.2 | 1.5-4.8 |



CONCLUSIONS OF IMPATT COMBINATORIAL POSTAMPLIFIER  
COMBINER TECHNOLOGY ASSESSMENT

1. Preferred Combinatorial Configuration(s)

- . Passive interstage combining preferred to active intrastage combining, primarily on basis of its accomodation of wider dispersion in device parameters, greater immunity to spurious oscillation and more graceful degradation under random device failure
- . Above considerations limit degree of active combining to maximum of two diodes per amplifier stage
- . Waveguide N-way reactive junction preferred combiner implementation based upon its ultralow insertion loss, wide band width and simplicity.

2. Combinatorial Postamplifier Performance Assessment

- . Preferred near term 20W combinatorial postamplifier (basis for POC design) utilizing 4 way divider/combiner and four 6W two-stage "building blocks" (each with two 3W diodes in its output stage) is most compact, highest DC/RF efficiency configuration, based on current near term 20 GHz IMPATT diode technology.
- . Eight way combinatorial 20W configuration provides even more graceful degradation capability than the the above, but only at the expense of higher DC prime power drain and greater size and complexity.
- . Eight way configuration is only viable combinatorial post amplifier for 40W capability using near term technology
- . Preferred long term 20W combinatorial postamplifier, utilizing four 6W single stage, single-diode "building blocks between four-way divider/combiner, provides optimum efficiency concurrent with minimum size and weight
- . Four way cobminatorial postamplifier, utilizing four 12W two stage "building blocks" (each with two 6W diodes in its output stage) results in the most efficient and compact 40W configuration.



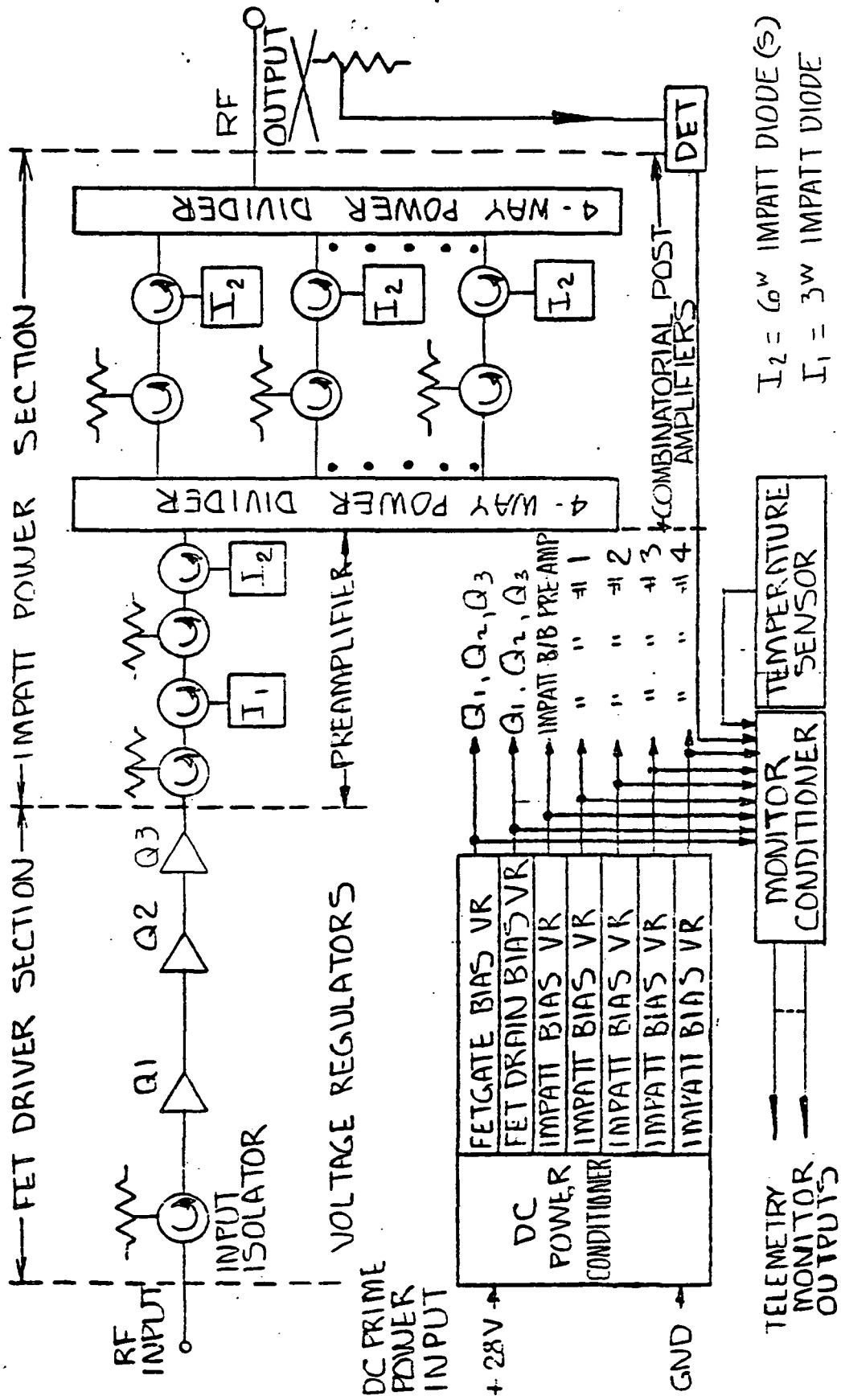
## 2.0 1987 IMPATT Transmitter Technology Assessment Study

RECOMMENDED ADVANCED 20 GHz IMPATT  
TRANSMITTER DESIGNS USING 1987 TECHNOLOGY

1. 20<sup>W</sup>, 2.5 GHz BW design
2. 40<sup>W</sup>, 2.5 GHz BW design

RATIONALE FOR ADVANCED 20 GHz IMPATT  
TRANSMITTER DESIGN RECOMMENDATIONS

1. 2.5 GHz transmitter bandwidth can accommodate single Gb/s rate angle modulated carriers.
2. 20W design compatible with current ground terminal projections
3. 40W design compatible with smaller, low cost, possibly mobile ground terminals.
4. Higher efficiency associated with 20W and 40W designs, results in tolerable DC power drains for IMPATT transmitters.



(27)

BLOCK DIAGRAM OF 20W, 20GHZ SOLID-STATE TRANSMITTER

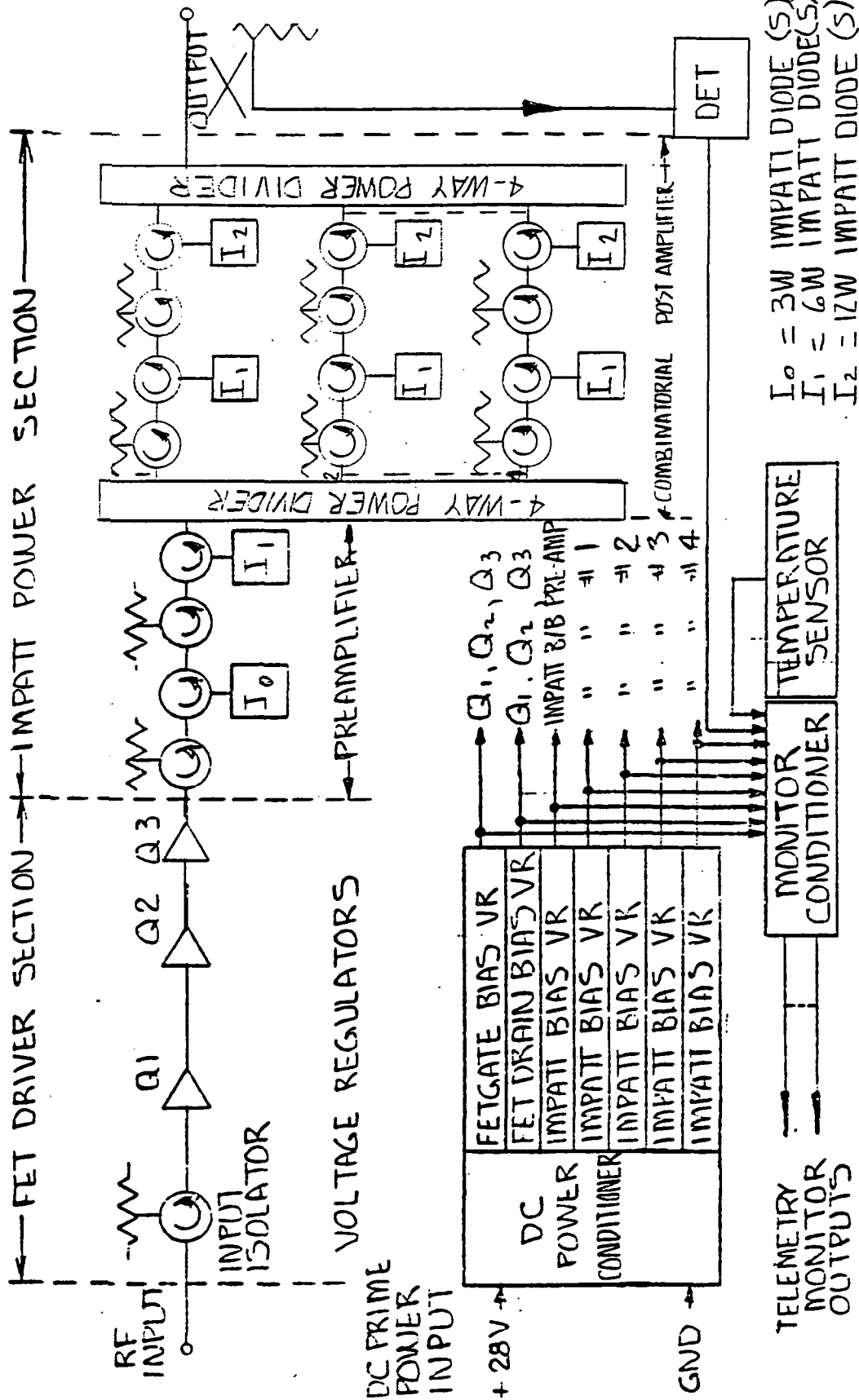


PROJECTED CHARACTERISTICS OF 20W, 20GHz

IMPATT SOLID-STATE TRANSMITTER DESIGN

|   |  |
|---|--|
| FREQUENCY RANGE                               | 17.7-20.2 GHz (Typ)  |
| -1 dB BANDWIDTH (MIN)                         | 2.5 GHz  |
| RF POWER OUTPUT (MIN)                         | 20W  |
| OPERATING GAIN (NOM)                          | 40 dB  |
| RF/DC POWER-ADDED EFFICIENCY (MIN)            | 22 PERCENT (EXCLUDING DC POWER<br>MONITOR CONDITIONER)           |
| AM/PM CONVERSION (MAX)                        | 5.0 deg/dB   |
| INPUT/OUTPUT VSWR (MAX)                       | 1.25:1   |
| GAIN VARIATION VS. FREQUENCY @<br>FIXED DRIVE | 1.0 dB p-p   |
| NOISE FIGURE (MAX)                            | 15 dB  |
| DC PRIME INPUT POWER-(MAX)                    | 90W - EXCLUDING DC POWER/MONITOR<br>CONDITIONER<br>100W. OVERALL |





BLOCK DIAGRAM OF 40W, 20GHz SOLID STATE TRANSMITTER



PROJECTED CHARACTERISTICS OF 40W, 20 GHz  
IMPATT SOLID-STATE TRANSMITTER DESIGN

|   |  |
|---|--|
| FREQUENCY RANGE                               | 17.7-20.2 GHz (Typ)  |
| -1 dB BANDWIDTH (MIN)                         | 2.5 GHz  |
| RF POWER OUTPUT (MIN)                         | 40W  |
| OPERATING GAIN (NOM)                          | 40 dB  |
| RF/DC POWER-ADDED EFFICIENCY (MIN)            | 21 PERCENT (EXCLUDING DC POWER<br>MONITOR CONDITIONER)           |
| AM/PM CONVERSION (MAX)                        | 6.0 deg/dB   |
| INPUT/OUTPUT VSWR (MAX)                       | 1.25:1   |
| GAIN VARIATION VS. FREQUENCY @<br>FIXED DRIVE | 1.0 dB p-p   |
| NOISE FIGURE (MAX)                            | 17 dB  |
| DC PRIME INPUT POWER-(MAX)                    | 190W - EXCLUDING DC POWER/MONITOR<br>CONDITIONER<br>200W OVERALL |





AREAS OF IMPROVEMENT IN ADVANCED 20 GHz IMPATT TRANSMITTER DESIGNS

| PARAMETER                    | DEGREE OF IMPROVEMENT |                  | REASON FOR IMPROVEMENT  |
|------------------------------|-----------------------|------------------|---|
|                              | Advanced Design       | Current Baseline |   |
| RF Output Power              | 40 W                  | 20 W             | Higher power IMPATT diodes, utilizing multiple or distributed mesas and/or dual chips/package.  |
| RF/DC Power Added Efficiency | 22 percent            | 15 percent       | Higher IMPATT diode efficiency due to <ul style="list-style-type: none"> <li>• reduction in <math>R_s</math></li> <li>• further optimization of Read profile</li> </ul> |
| Noise Figure                 | 15 dB                 | 25 dB            | Higher gain, lower noise FET preamplifier preceding IMPATT power section.   |
| Bandwidth                    | 2.5 GHz               | 1 GHz            | Lower parasitic IMPATT package and lower diode $R_s$ coupled with more extensive use of broad-banding techniques.   |



TASK DESCRIPTION FOR DEVELOPMENT OF ADVANCED  
20 GHz IMPATT TRANSMITTER

- A. Design Definition
  - 1. Parametric tradeoff analysis
  - 2. Technology assessment
  - 3. Preferred paper design
- B. Device/Assembly Development
  - 1. Advanced GaAs IMPATT device development
    - . optimization of Read doping profile
    - . optimization of chip mesa geometry
    - . maximum degree of substrate thinning for minimum  $R_s$
    - . minimization of packaging parasitics
    - . chip combining within package
    - . use of DHS for minimum thermal resistance
  - 2. Advanced amplifier circuit development
    - . broadbanding of IMPATT and FET amplifier stages and associated passive components for full 2.5 GHz bandwidth.
    - . dual diode IMPATT amplifier stage development
    - . development of higher gain lower noise FET preamplifier circuits.
  - 3. DC Power and monitor conditioner development
- C. POC Model Design, Fabrication, Assembly and Test
- D. QA/Reliability
  - 1. Reliability Analysis
  - 2. Product Assurance
- E. Documentation