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Improved SCR ac Motor Controller for Battery Powered Urban Electric Vehicles

Thomas S. Latos
Gould Laboratories, Electrical & Electronic Research
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December 1982

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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Under Contract DEN 3-60

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Foreword

This final report was prepared for the National Aeronautics and Space Administration, Lewis Research Center for the Department of Energy by Gould Laboratories of Gould Inc. in Rolling Meadows, Il. Mr. F. Gourash of the Lewis Research Center was the contract Project Manager. The author wishes to acknowledge the contributions of R. Ehrlich, T. Jahns J. Mezera, D. Thimmesch and D. Bosack to the contract technical effort and this report.

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Contents

Page

Appendices

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Executive Summary

DEN3-60 was a research contract funded by the Department of Energy and managed by NASA-Lewis Research Center to design and develop an electric vehicle propulsion system controller which uses an ac induction electric motor as the electrical to mechanical energy conversion unit. Specifically, the contract program was to design and test an improved ac motor controller, which when coupled to a standard ac induction motor and a dc propulsion battery, would provide a complete electric vehicle power train with the exception of the mechanical transmission and drive wheels. In such a system, the motor-controller converts the dc electrical power available at the battery terminals to ac electrical power for the induction motor in response to the drivers commands.

The performance requirements of a hypothetical electric vehicle with an upper weight bound of 1590kg (3500 lb) were used to determine the power rating of the controller. Vehicle acceleration capability, top speed, and gradeability requisites were contained in the Society of Automotive Engineers (SAE) Schedule 227a(d) driving cycle. The important capabilities contained in this driving cycle are a vehicle acceleration requirement of 0-72.4 kmph (0-45 mph) in 28 seconds, a top speed of 88.5 kmph (55 mph), and the ability to negotiate a 10% grade at 48 kmph (30 mph). A 10% grade is defined as one foot of verticle rise per 10 feet of horizontal distance.

With the aid of a computer simulation, the vehicle acceleration, top speed, and gradeability requirements were translated into electric motor torque and shaft power requirements. If shaft torque exceeds 40 N-m (29.5 ft-lb) until the vehicle speed surpassed 72.4 kmph (45 mph), the acceleration requirement would be attained. Similarly, if the electric motor shaft power capability was at least 12kW (16hp) at vehicle speeds of 88.5 kmph (55 mph) and 26kW (34.8hp) at 48 kmph (30 mph), the requirements of the SAE 227a(D) driving cycle could be met or exceeded. Since the mechanical transmission between the electric motor and the drive wheels determine both the rear wheel

torque and electric motor shaft speed at a given vehicle speed, a fixed ratio transmission with a speed reduction of 9.8:1 was selected to use in the computer simulation. This transmission would multiply the motor shaft torque available at the rear wheel axle. The simulated vehicle was assumed to be equipped with 0.33m (13") diameter wheels. The combination of transmission gearing and wheel diameter dictated the speed range of the electric motor to be 0-816 rad/s (0-7800 rpm).

The motor controller converts dc voltage and currents available at the battery terminals to ac voltages and currents required by the three phase ac induction motor. The translation from dc to ac is accomplished with an array of six switches schematically illustrated in Figure i-1. These six switches allow each motor terminal to be connected to either the "plus" battery terminal or the "minus" battery terminal. When two motor terminals are considered, it can be seen that the voltage polarity across motor terminals A and B in Figure i-1 can be positive, zero, or negative with respect to terminal B. These three polarities correspond to motor terminal A connected to the (+) battery terminal and motor terminal B connected the (-) battery terminal, both motor terminals A and B connected to the same battery terminal (either plus or minus), and finally motor terminal B connected to the (+) battery terminal and motor terminal A connected to the (-) battery terminal. By coordinating the switching of the six switches in Figure i-1, a three phase set of voltage waveforms can be applied to the motor terminals, each phase electrically displaced 120° from each other. By simply varying the rate at which the switching action accurs, the output electrical frequency of the motor controller can be varied.

In the Gould motor controller, the six switches are physically implemented with silicon controlled rectifiers or SCRs. This family of semiconductor switches is available with suitable voltage and current specifications to switch the motor terminals from the plus battery terminal to the minus battery terminal. Although SCRs are not the only candidate semiconductor family (for example, BIPOLAR transistors, gate-turn-off thyristors, or field effect transistors), the use of SCRs within the motor controller was a specific requirement of Contract DEN3-60.

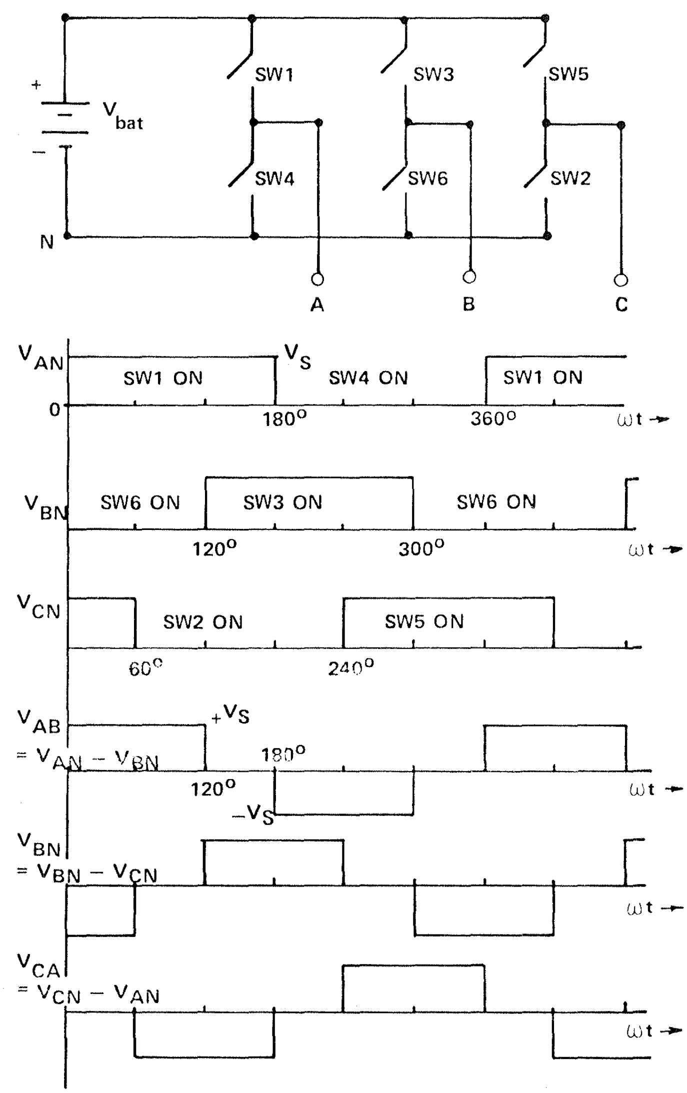

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Figure i 1 Six Switch Array to Convert dc to Three -Phase ac

The electrical schematic of the power electronics circuit within the motor controller is illustrated in Figure i-2. SCRs 1-6 form the six switch array. Diodes D1-6 allow the motor controller to successfully tolerate leading or lagging motor power factors by providing a path for reactive currents in the absence of a conducting SCR. The remaining components are used to commutate or turn off SCRs which have been gated into conduction.

The battery voltage was selected to be 120Vdc. This decision was based on the traditional use of golf-cart style batteries in electric vehicles and the availability of SCRs in stud mount packages (TO-93) with suitable voltage and current ratings.

The ac induction motor selected to complete the electrical propulsion system was a modified Gould E-plus three phase induction machine. The motor rated 7.46kW at 60Hz (10hp) is produced in a NEMA 215 TENV frame size. Motor rotor modification consisted of replacing the original ball bearings with a class C clearance bearing system removing the cooling fins from the rotor end castings, and precision balancing the rotor assembly. The original stator windings were removed and the stator rewound such that the motor was rated for 36V ac operation at 60Hz.

The control approach used to coordinate the voltage and frequency applied to the motor terminals is based on the accurate control of the slip or difference frequency between the motor mechanical frequency and the electrical excitation frequency. With this approach, the induction machine shaft torque is linear with slip frequency and independent of the mechanical speed of the rotor provided the machine air gap magnetic flux is held constant.

Two independent control loops within the controller control the slip frequency and the air gap flux in the induction motor. The slip frequency is added to the motor shaft frequency directly via tachometer feedback using digital phase lock techniques. For the selected induction motor, the torque constant is 30N-m/Hz of slip (22.1 ft-lb). The resulting sum of the slip frequency and the motor shaft frequency directly determines the motor excitation frequency supplied by the inverter.

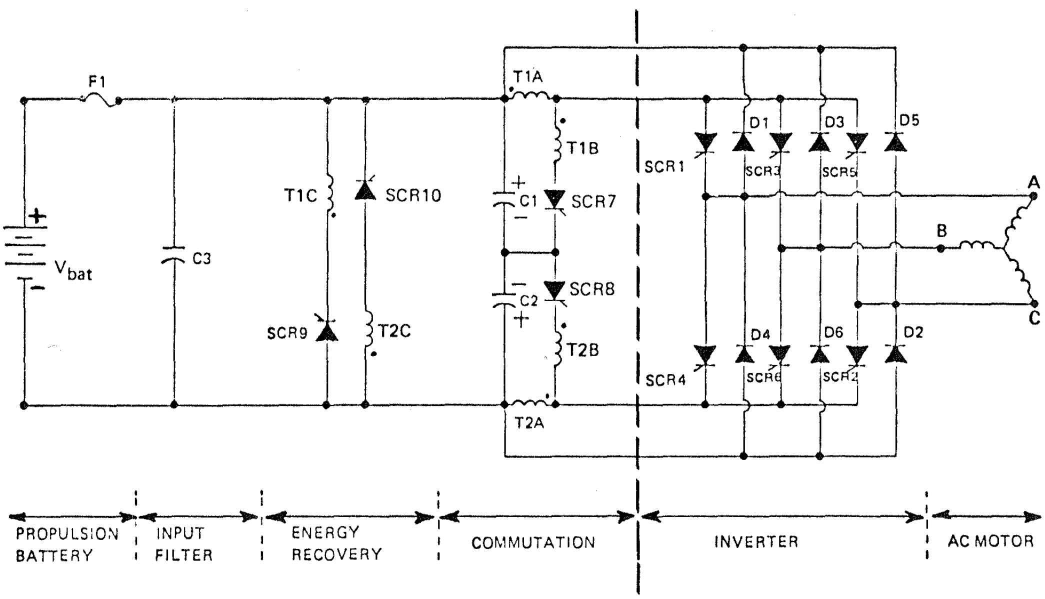

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Figure i–2 EV Propulsion System Power Stage Configuration

To achieve control of the air gap flux of the machine, ultimately the terminal voltage applied to the motor must be controlled. The applied voltage ideally should be smoothly variable between zero and the maximum available from the propulsion battery. A second requirement placed upon the applied motor voltage is that it be sinusoidal to minimize both motor ripple torque and peak controller currents. These requirements are achieved in the Gould controller with a Pulse Width Modulation (PWM) algorithm. The exact algorithm adopted which determines the on-off gating signals applied to the thyristor switch array examines the intersection of sine wave reference generated at the motor excitation frequency (f_{ex}) and a triangle function generated at nf_{ex} where n is a function of the excitation frequency. In this controller, n assumes discrete values of 9, 27, 45, 63, and 81. By controlling the amplitude of the sine wave and the triangle function, both the amplitude and the harmonic content of the applied motor voltage is controlled. Figure i-3 illustrates the PWM algorithm for n=9 and n=27.

The air gap flux control algorithm generates control signals to vary the amplitude of the sine and triangle functions. The control algorithm feedback measures the fundamental component of the applied motor voltage and implements a constant voltage/frequency strategy with low speed compensation for stator resistive losses.

The control logic which implements the air gap flux algorithm is accomplished with a Molorola 6802, 8 bit microcomputer system. Additional tasks assigned to the microcomputer are controller logic sequencing, thermal protection of the power circuit components, and controller interlocking to prohibit damaging operator commands. The remainder of the controller logic is implemented with discrete CMOS logic. Specific logic blocks generate the sine and triangle functions, perform the slip frequency addition, and generate the SCR gating signals.

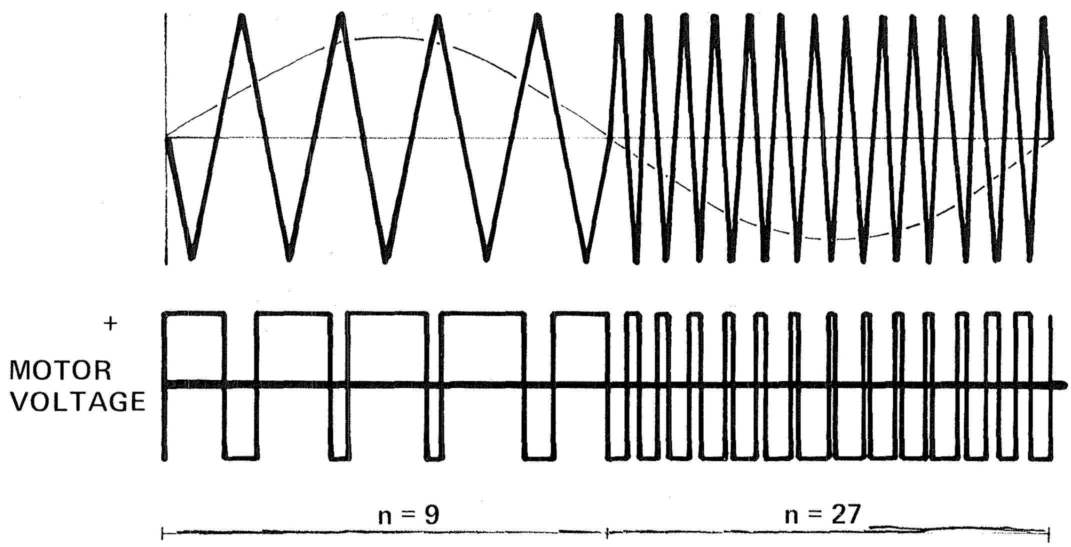

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Figure i 3 Sine Triangle Modulation Strategy Showing the Effect of Changing the Parameter n. For n=9, the First Significant Motor Harmonic is the 17th; for n=27, this Changes to the 53rd. The Developed Motor Terminal Voltage is Independent of n, but Varies with the Relative Amplitudes of the Sine and Triangle Reference Waveforms.

The complete controller and motor system is illustrated in Figure i-4. The power circuit is contained in the large enclosure and communicates with the logic system via the flexible conduit. Logic power is derived from the propulsion battery via a combination of linear and switching regulators.

The power circuit weighs 56.8kg (135 lb) and occupies a volume of 87 x 10^{-3} m^3 (3.10 ft^3) and its associated control logic weighs 8.2kg (18 lb) and occupies a volume of 17.8 x 10^{-3} m^3 (0.63 ft^3). The induction machine weighs 53.1 kg (117 lb) and is in a 215 TENV NEMA frame. Details of the controller construction can be seen in Figures i-5 and i-6 respectively which are photographs of the controller interiors.

System testing was accomplished with a dynamometer system capable of testing the motor/controller in both the 1st and 4th quadrants; i.e.motoring and regeneration. The motor controller system torque limits as a function of motor shaft speed are shown in Figure i-7. A shaft torque of 60N-m (44.2 ft-lb) is obtainable at locked rotor and peak torque capability exceeds 100N-m (73.6 ft-lb) at 315 rad/s (3008 rpm). An inspection of the torque speed envelope indicates the assumed vehicle will be able to successfully meet the schedule D requirements for acceleration, cruise, and gradeability.

The controller's electrical efficiency as a function of motor shaft speed is shown in Figure i-8. Peak controller efficiency of 92% is obtained at peak power. This is expected since the fixed controller losses become the smallest fraction of the input power. The commutation circuit components, primarily the magnetic elements, account for the largest portion of the controller losses.

The retail cost of the ac controller and motor developed in DEN3-60 is projected to be $1500 in annual manufacturing quantities of 100,000 units. The controller is projected to cost $1310 of this total and the motor $190.

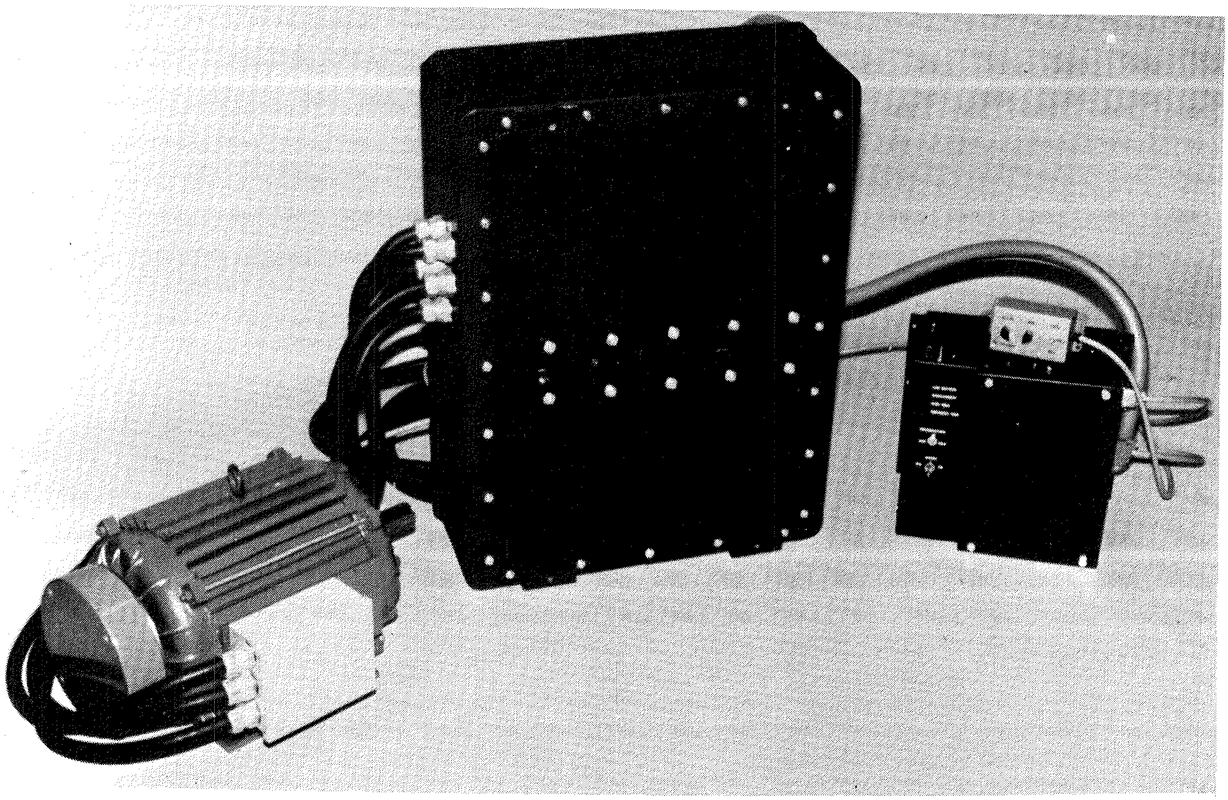

Figure i–4 Motor – Controller System
The three major components are induction motor (left), the power circuit (center), and the control electronics (right)

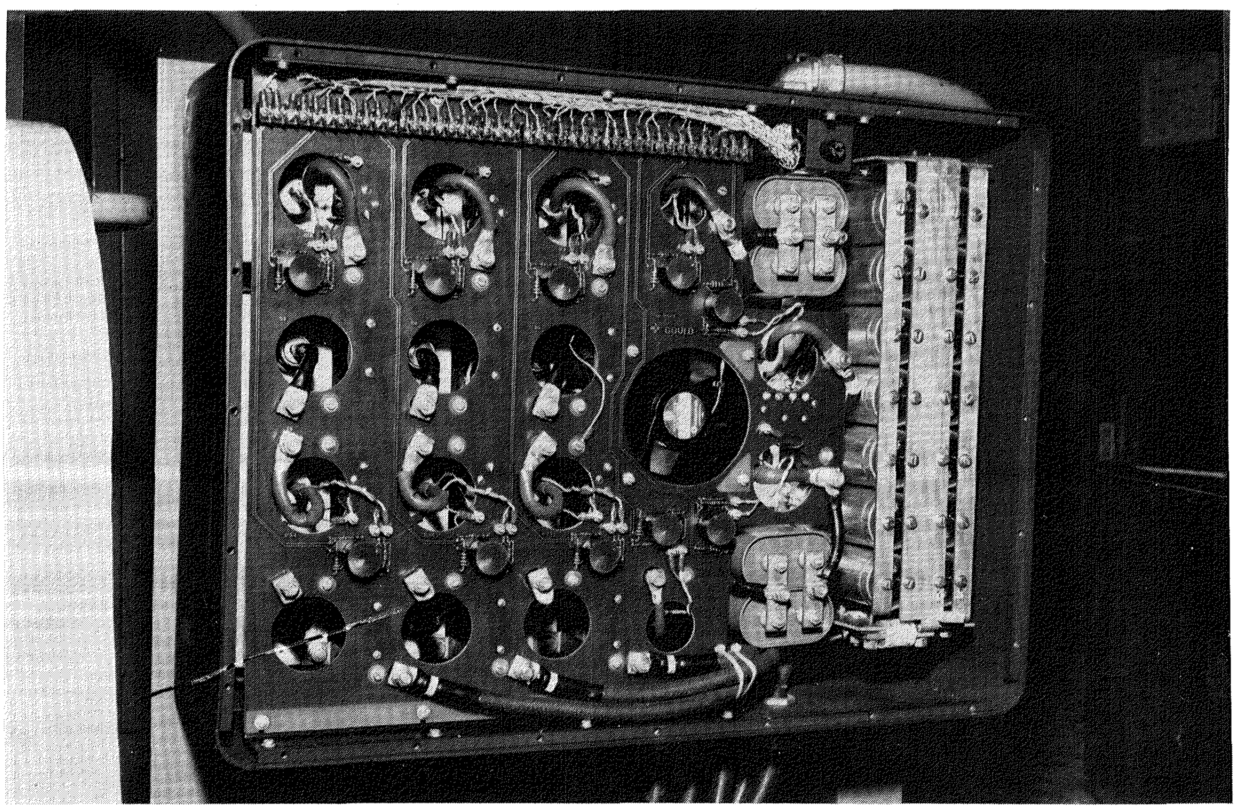

Figure i–5 Interior of Power Circuit Enclosure
Input filter is to the right. Commutation components are centered about the cooling fan. Main SCR's and diodes are to the left.

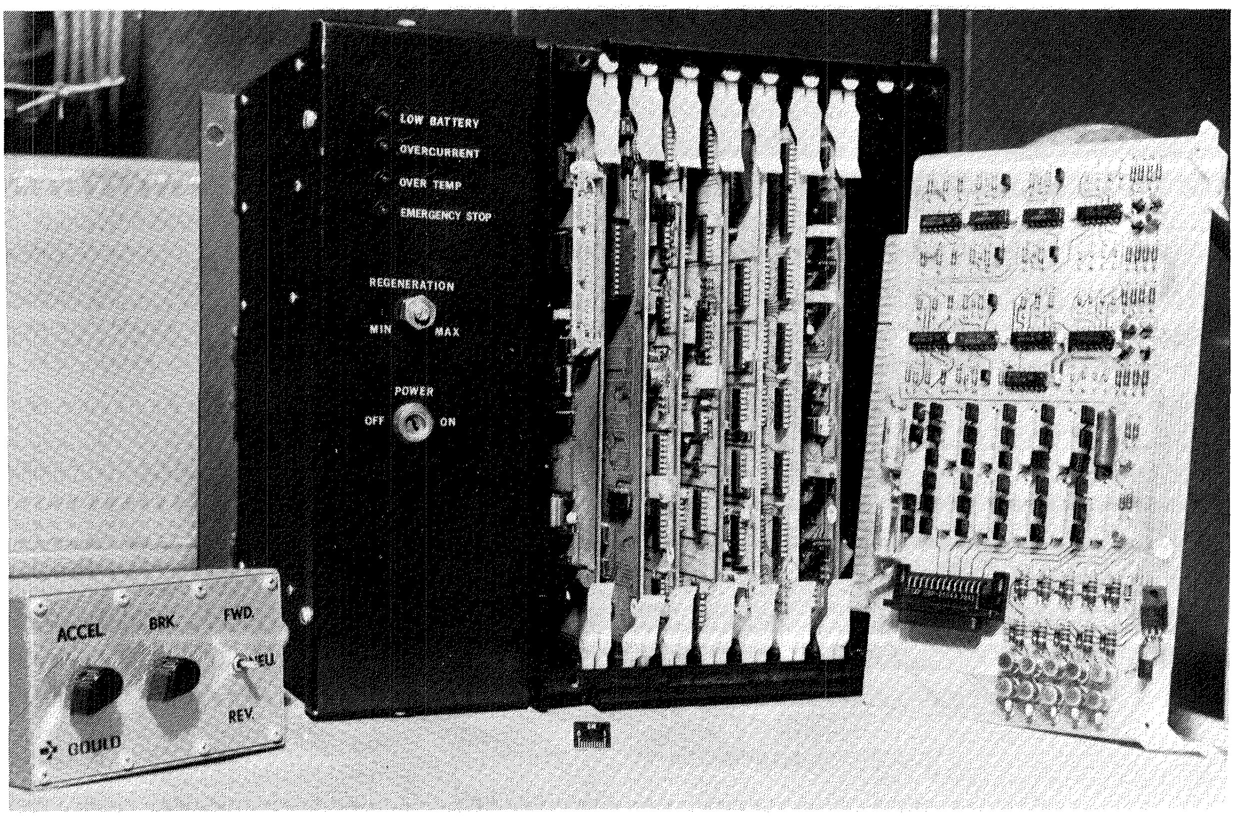

Figure i–6 Control Logic Enclosure Interior

Circuitry is modularized on eight printed circuit boards for servicing. A simulated drivers console is at the left. Braking energy is returned to the battery.

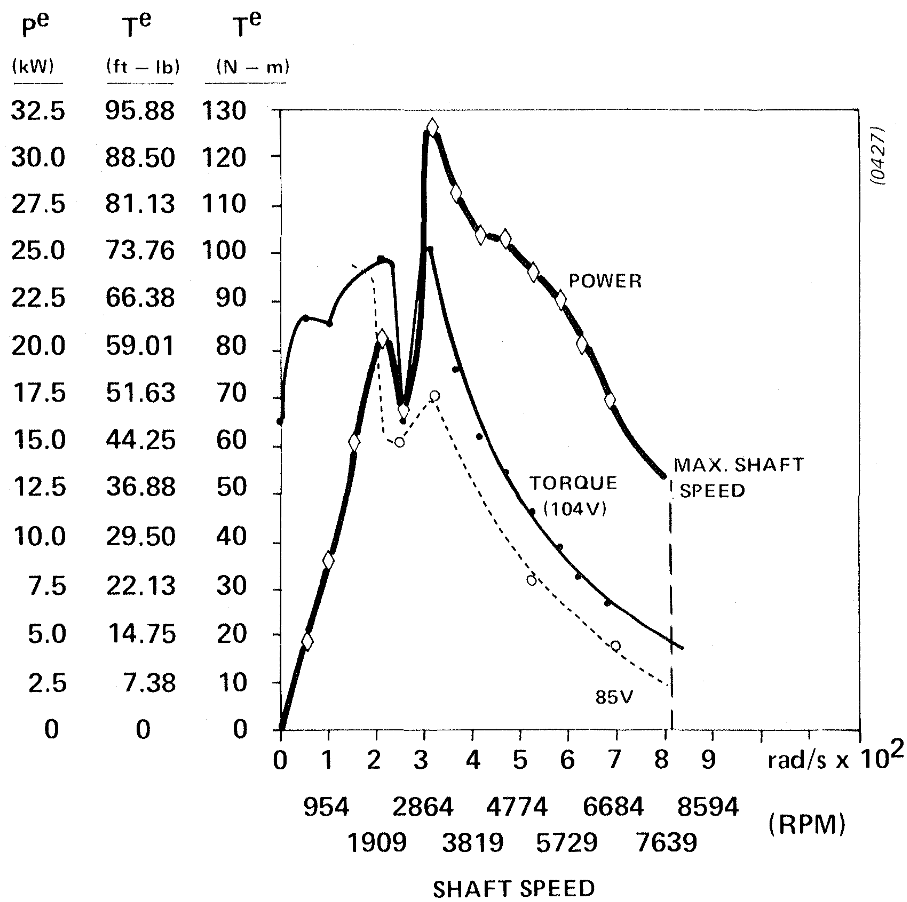

Figure i–7 Motor/Controller Torque Speed Envelope – 1st Quadrant

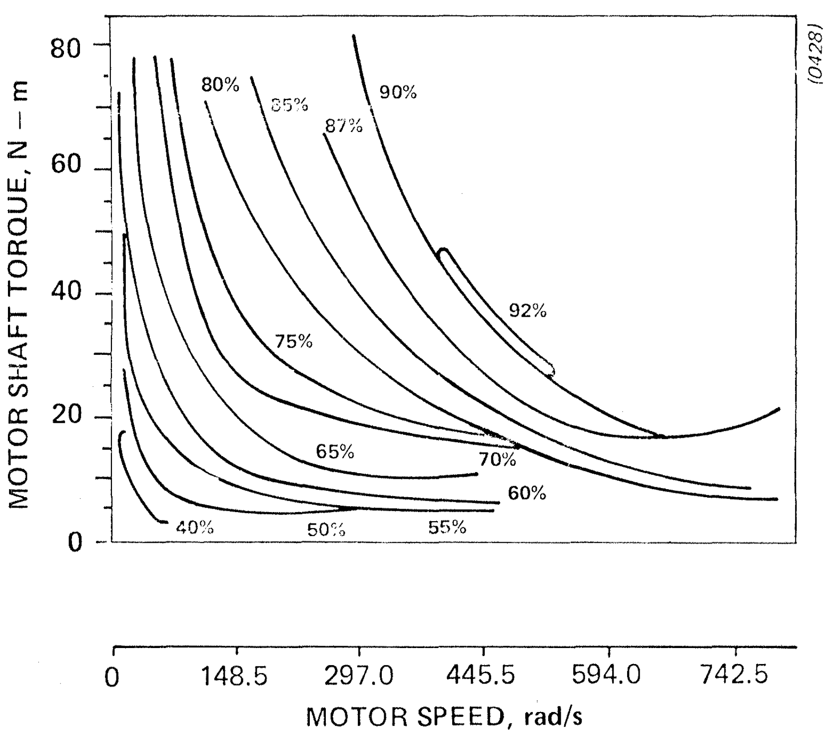

Figure i–8 SCR Controller Efficiency Data – 1st Quadrant Operation

I. Introduction

Nearly all electric vehicle propulsion systems in the past have employed a dc motor and controller to convert battery-stored electrical energy into mechanical energy at the vehicle drive wheels. The dc system has found wide acceptance since the controller design is straightforward and the dc machine provides torque-speed characteristics appropriate for traction applications. An advantage of this system approach is the basic simplicity of dc motor control techniques, typically employing battery tap-changers, resistive networks, or solid-state choppers to vary the applied motor voltage. However, the dc motor itself is responsible for providing the system with its major disadvantages. Dc machines are generally larger, heavier, and more expensive than alternative ac machines, largely due to the dc motor's mechanical commutator. In addition, mechanical commutators often pose special maintenance problems.

Ac machinery suffers none of the disadvantages associated with the mechanical commutators since the required commutating action is performed electronically in the controller circuitry. The ac squirrel-cage induction motor chosen for use in this program is inherently rugged, inexpensive, and capable of high-speed operation. Historically, the principal disadvantage of ac systems has been the control complexity associated with translating the system input commands into motor excitation waveforms of the proper frequency and voltage amplitudes. However, as the cost of power semiconductors and integrated circuitry decreases and general interest in electric vehicles increases, the potential of ac motors for EV propulsion is attracting renewed attention.

This report discusses a program to develop and design an improved induction motor controller for vehicle applications. The selected vehicle configuration used to size the power rating of the controller is a 3500 lb commuter-style vehicle with performance specifications drawn from the SAE J227a, Schedule D driving cycle. Specifically, these performance requirements include acceleration to 45 mph in 28 seconds, 10 percent gradeability at 30 mph, and capabilities for extended crusing at 55 mph. Regeneration of braking energy back to the propulsion battery is also specifically required. The controller rating was selected to allow the use of a fixed-ratio transmission in the drivetrain. The controller has been designed to employ conventional lead-acid batteries and an industrial-grade induction motor.

Thyristors, or silicon controlled rectifiers (SCR's), were chosen as the power semiconductor switching devices for the power stage on the basis of their proven ruggedness and low cost. In an effort to reduce controller cost by minimizing the number of power stage components, a bus-commutated circuit topology for the power stage was adopted at the outset of the program. The special demands made by this type of topology on the control logic are discussed in this report. The harsh vehicle operating environment dictated that the power stage be contained in a moisture-resistant enclosure making component cooling more difficult. Vehicle ram air directed over the power stage package provides sufficient cooling capability except during extended low-speed operation when thermal protection via controller shutdown is employed.

To insure suitability for vehicle applications, the control logic has been designed to give the propulsion system the characteristics of a torque controller. The control logic responds to operator acceleration and braking requests by making appropriate adjustments in motor excitation voltage and frequency. A motor shaft tachometer and motor voltage transducer provide the control logic with the necessary feedback information to make these adjustments. These control actions are performed by logic submodules under the supervision of an on-board microporcessor. Controller sequencing and protection are additional tasks of the microprocessor.

Contract DEN3-60 was a research contract funded by the Department of Energy and managed by NASA-Lewis Research Center.

II. Propulsion System Configuration

2.1 Vehicle Performance Requirements

The required performance level for an electric automobile for the contract work scope is defined by the SAE J227a Schedule D driving cycle. This driving cycle is schematically pictured in Figure 2.1 and contains an acceleration profile of zero to 72.4 km/h (45 mph) in 28 seconds, continued crusing at 72.4 km/h (45 mph) for 50 seconds, a coast period of 10 seconds and finally deceleration to zero speed in 10 seconds. A gradeability requirement, 48.3 km/h (30 mph) for one minute on a 10% grade, is also included along with a top speed requirement of 88.5 km/h (55 mph).

These performance goals, when applied to a commuter style electric powered vehicle, specify the necessary wheel torque and power. A standard vehicle used for this study has the following characteristics:

1)	Mass	1590 kg	(3500 lb)
2)	Frontal Area	1.86 m^2	(20 ft^2)
3)	Drag Coefficient	0.3	
4)	Drivetrain Efficiency	90%	

This vehicle requires a power of 11.3kW to maintain a speed of 88.5 km/h (55 mph) at zero grade and 27.0kW to maintain a speed of 48.3 km/h (30 mph) on a 10% grade. To aid in the determination of motor torque-speed requirements, a Vehicle Acceleration Profile Program (VAPP) was assembled to calculate acceleration time to a target speed. Program listings are included in Appendix I.

2.2 Drivetrain Selection

An electric vehicle drivetrain consists of the propulsion battery, the electric propulsion motor, a transmission (either fixed or multiple ratios), and finally, the drive wheels. These are symbolically represented in Figure 2.2. In any electric propulsion system, selection of the open-circuit battery

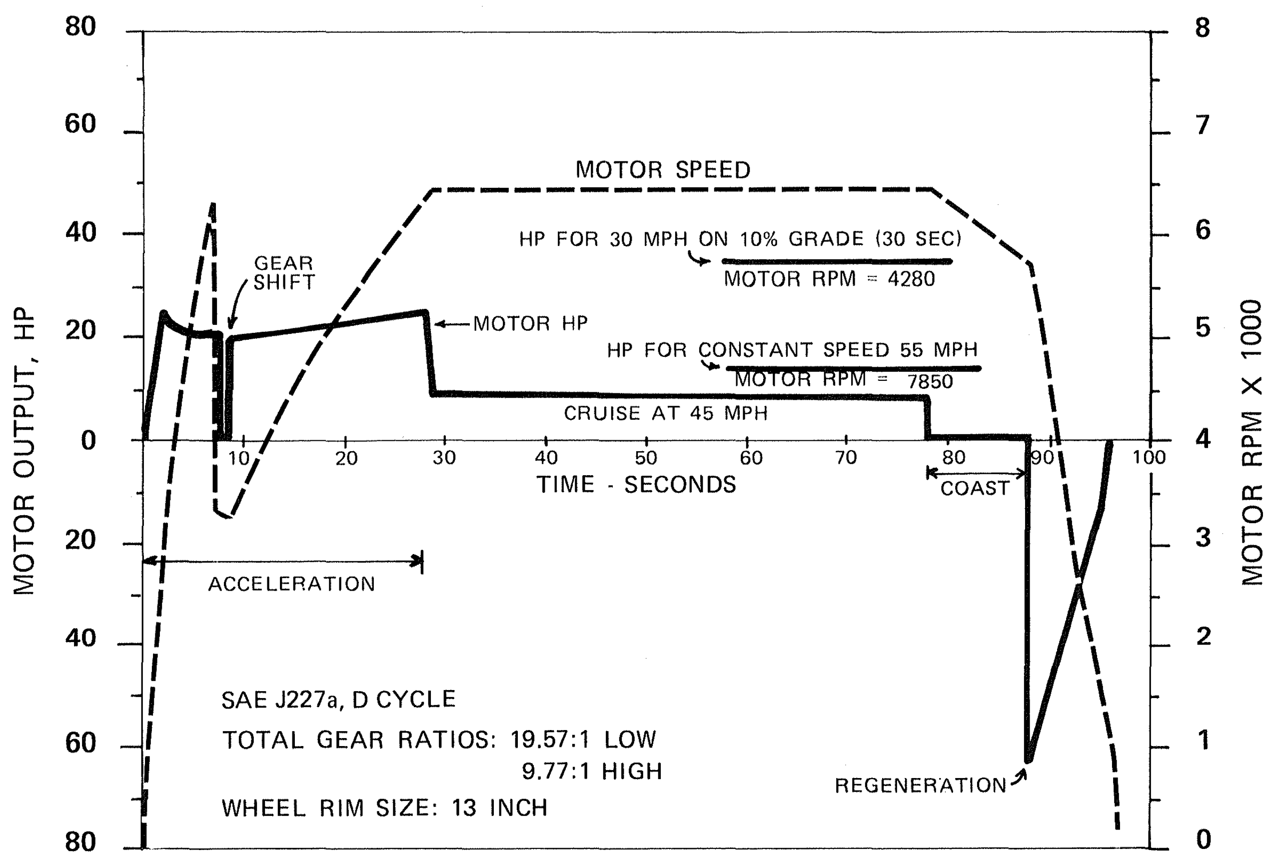

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Figure 2.1 **Typical Motor Performance in Vehicle—SAE J 227a, Schedule d, Driving Cycle**

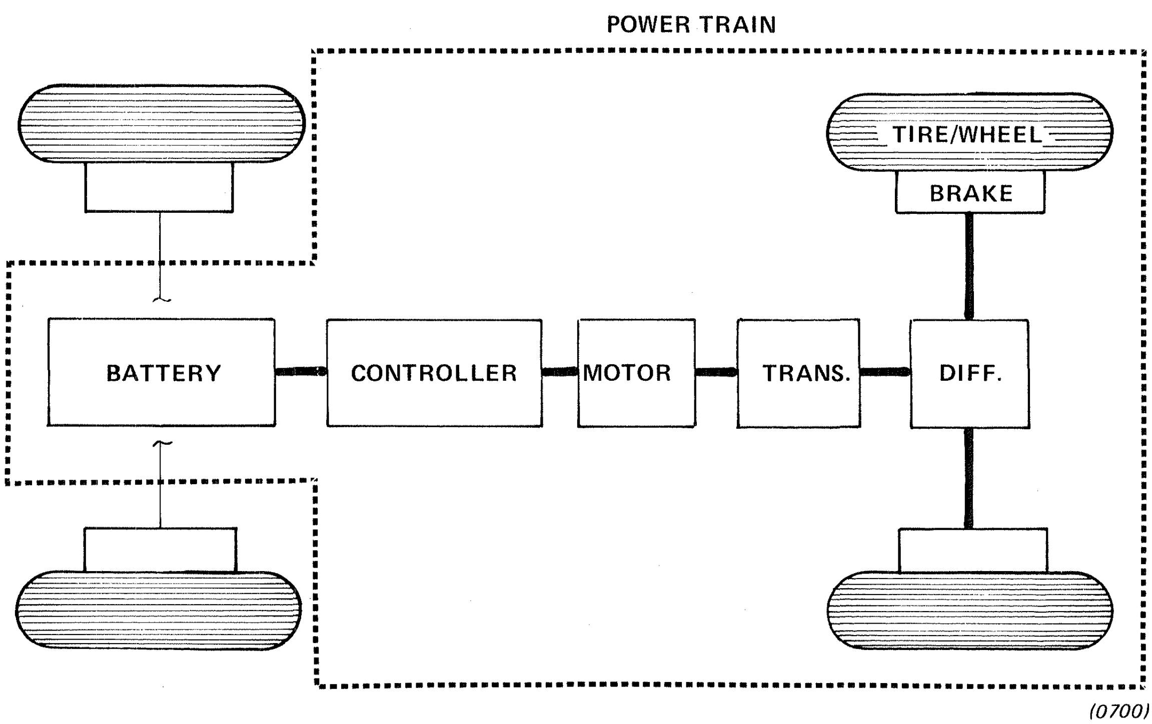

Figure 2.2 General Propulsion System Topology

terminal voltage is somewhat arbitrary given that the total battery energy capacity is adjustable independent of terminal voltage. Since the electric vehicle industry is presently manufacturing vehicles with off-the shelf components, however, custom battery modules are not available to allow the simultaneous optimization of battery capacity and terminal voltage. The batteries which are readily available with acceptable performance characteristics are golf-cart style batteries having a typical capacity of 125A-h at a 100 minute rate.

For this program a 120V battery consisting of 60 such golf-cart cells was selected. This gives a reasonable compromise between the desire to minimize controller currents (have a high terminal voltage) and the need to keep battery weight consistant with the target vehicle performance requirements.

To minimize the expense of the vehicle drivetrain, a fixed ratio transmission was selected with a ratio of 9.8:1. This ratio provides adequate wheel torque to meet acceleration goals and still limits the top speed of the ac motor to 7800 rpm at 55 mph. Although conventional ac squirrel-cage induction motors normally operate up to speeds of only 366 rad/s (3500 rpm), their structrual design allows operation at speeds exceeding 1047 rad/s (10,000 rpm).

To provide both the peak power requirements of 27kW and the steady state requirements of approximately 12kW at 55mph, a NEMA 215 TENV frame size induction motor was deemed adequate. This motor size was suggested by both NASA-Lewis during the procurement stage and by Rohr Industries as a result of their contract work[1]. This motor size can produce accelerating torques of 60 N-m which will successfully meet the 0-45 mph acceleration requirement when coupled with a 9.8:1 fixed ratio transmission.

The defined powertrain is summarized in Figure 2.3. It consists of a 120V battery, a dc-ac motor controller, a 215 TENV induction motor, and a fixed ratio, 9.8:1, differential torque multiplier.

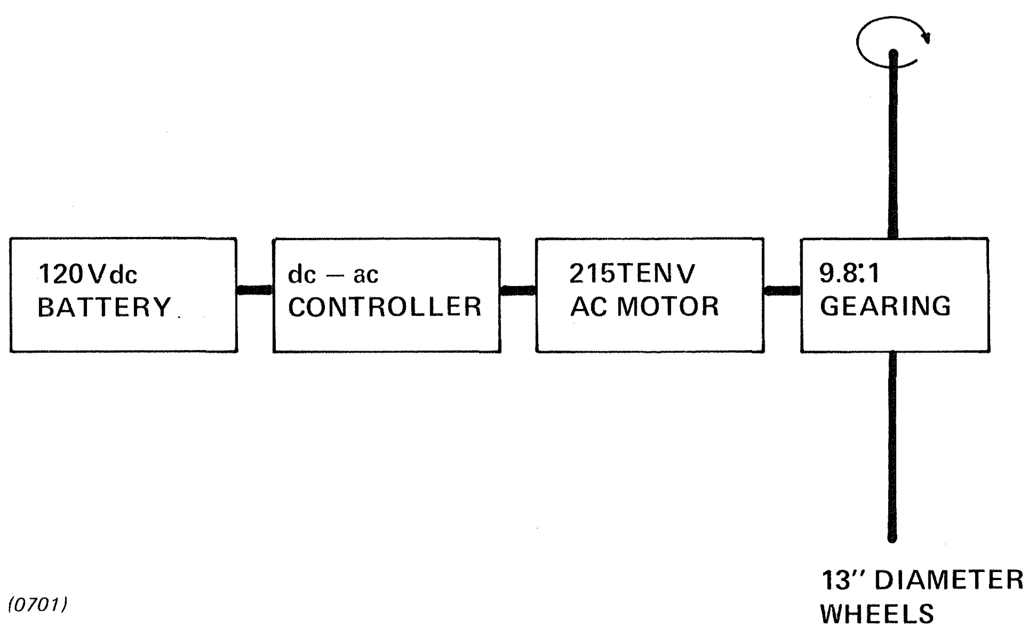

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Figure 2.3 Selected Propulsion System Power Train

2.3 Inverter System Requirements

The torque-speed envelope requirements at the shaft of the ac motor are illustrated in Figure 2.4 which also shows the vehicle speed corresponding to a given motor shaft speed. The critical torque-speed couples for gradeability and high speed operation are clearly indicated along with the acceleration torque requirements. As is seen in the Figure, the minimum acceptable torque to meet the acceleration requirements is approximately 40 N-m with 60 N-m required to successfully negotiate a 10% grade at 30 mph.

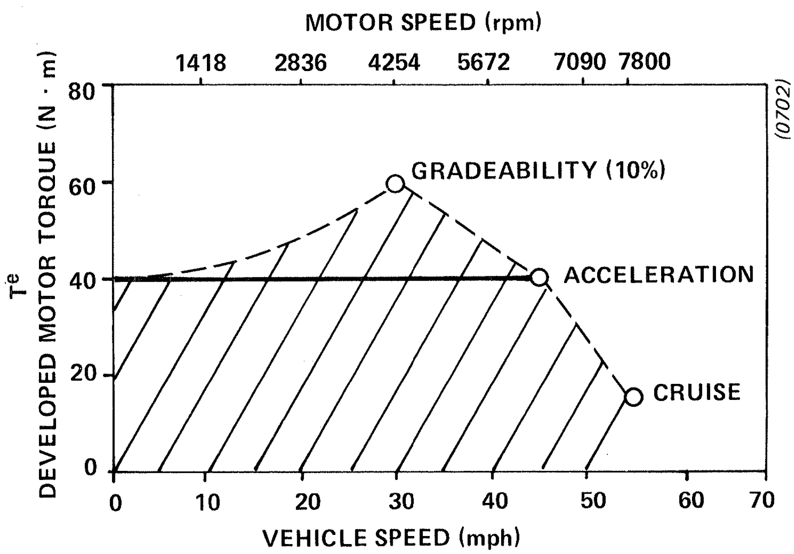


Figure 2.4 Motor - Torque - Speed Requirements

III. Motor/Controller Design

3.1 Induction Motor Selection and Modifications

Motor Selection

At the heart of the EV propulsion system is the ac motor. As called for in the contract requirements, this motor is a rugged squirrel-cage induction machine. From the beginning of this program it was clear that successful achievement of system performance goals demanded that the selected motor be fully compatible with the controller design.

The contract statement of work gave Gould the option of using a Government-furnished (GFE) induction motor or supplying an alternate motor subject to NASA Project Manager approval. After studying the GFE motor specification, Gould elected to supply an alternate motor. There were two principal reasons for this decision. First, the GFE motor, being necessarily wound for a fixed stator voltage, would limit Gould's freedom in choosing the controller system voltage. Second, tangible benefits in motor efficiency and power factor were forseen by selecting an appropriate alternate motor.

In place of the GFE machine, Gould supplied a motor from its own E-Plus™ line of induction machines. Introduced in 1975, these industrial grade machines are specially designed to provide higher operating efficiency and power factor than the standard industry-average motors. A cutaway view of the typical E-Plus™ motor is provided in Figure 3.1 together with short descriptions of the design techniques employed to reduce losses and improve power factor. The E-Plus™ motor selected for this program is constructed with an aluminum housing, steel stator and rotor laminations, copper stator windings, and aluminum rotor bars and end rings.

Selection of a specific motor for this program consisted of matching performance requirements with available motor ratings. This analysis confirmed the earlier results of the 1978 Rohr Industries study[1] showing that

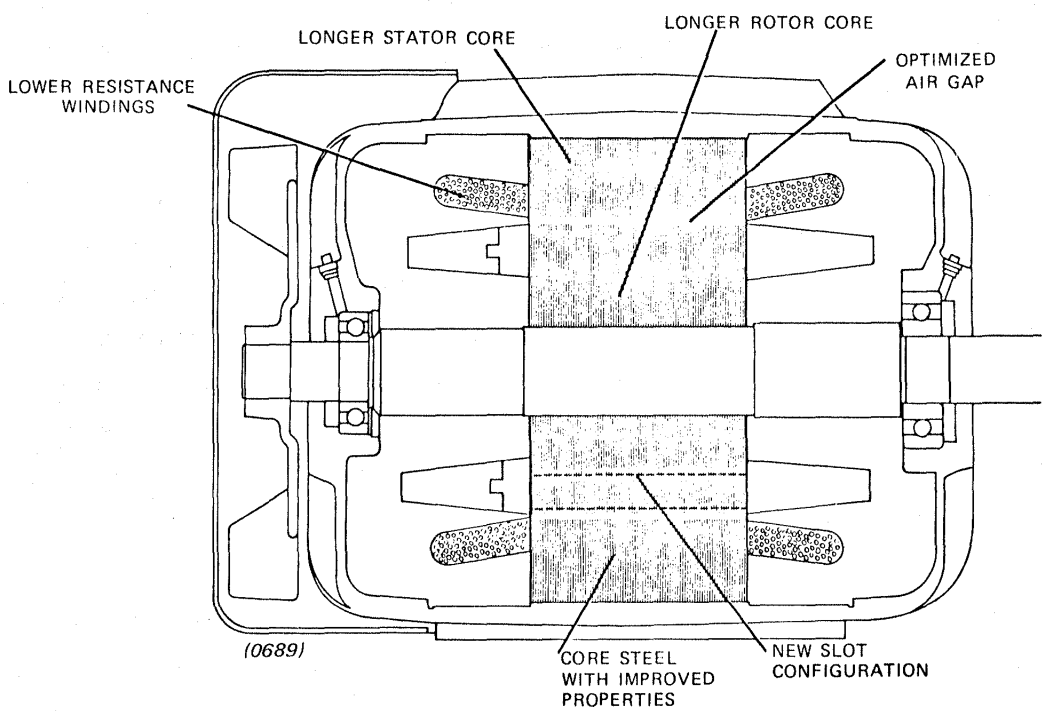


Figure 3.1 Construction Details of Gould E–Plus ™ Motor

the performance requirements are best met with a nominal 10 hp, 1800 rpm, four-pole NEMA 215T frame machine. This motor produces a 40 N-m torque under rated flux conditions and can produce over twice that amount during transient conditions at the same flux level. Provided that these torque levels can be delivered over a wide vehicle speed range, as will be described shortly, this motor is capable of meeting all contract power handling requirements. Key motor characteristics are summarized in Table 3.1.

Motor Modifications for the EV Application

Since the E-Plus™ motors are intended for industrial use, they have been designed for fixed-frequency (60 Hz), fixed speed (1800 rpm for a 4-pole design) and operation from a fixed standard utility voltage source (230V, 3-phase, typically). Nevertheless, these machines are useful over the wide speed ranges encountered in this EV application provided that a limited number of motor modifications are introduced. Mechanical modifications of the rotor assembly included rotor balancing and bearing replacement in order to extend motor shaft speed capabilities to 8000 rpm. Mechanical integrity of the rotor poses no problem since the tested burst speed for this type of squirrel-cage rotor assembly is 16,000 rpm. Following the suggestions of the NASA Technical Program Monitor for this contract, the rotor was fitted with Class C clearance single-shielded ball bearings lubricated with a high-quality, high-temperature grease, type SRI-2. Further modifications of the rotor to accommodate the extended speed range included removal of the aluminum rotor cooling fins which normally extend from the squirrel-cage end rings. Rotor balancing for 8000 rpm operation was performed using the same techniques used in balancing high-speed automotive engine shafts.

Since the chosen system voltage of 120V is considerably less than standard utility industrial supply voltages, it was necessary to rewind the stator for a reduced voltage level. A summary of the analysis underlying the choice of voltage rating for the new winding will be presented here. According to the contract specifications, the highest power delivery requirements for the propulsion system occurs at 30 mph under 10% grade conditions. Assuming a 9.8:1 drivetrain transmission gear ratio, 30 mph

Table 3.1

SUMMARY OF KEY MOTOR CHARACTERISTICS

Motor Type:	Gould E-Plus™ Squirrel-Cage Induction Motor
Motor Frame Size:	NEMA 215T
No. of Stator Phase/Poles:	3-Phase, 4 pole
Rated Power:	7.46kW at 1800 rpm
Rated Shaft Torque:	40 N-m at 1800 rpm
Rated Stator Voltage:	36V line-to-line at 60 Hz
Rated Stator Current:	140 A at 60 Hz
Rated Rotor Slip:	2.2% at 60 Hz
Rotor Burst Speed:	16,000 rpm
Rotor Bearings:	Class C Clearance Ball Bearings

corresponds to a motor excitation frequency of 140 Hz for the 4-pole motor. Since the battery terminal voltage may sag to the vicinity of 110V under maximum loading conditions, the fundamental frequency line-to-line rms voltage component, $V_1^{\ell\ell}$, will be only 86V under such conditions:

$$V_1^{\ell\ell}{}_{140\ \mathrm{Hz}} = \frac{\sqrt{6}}{\pi} V_{bat} = (.78)(110) = 86V \qquad [3.1]$$

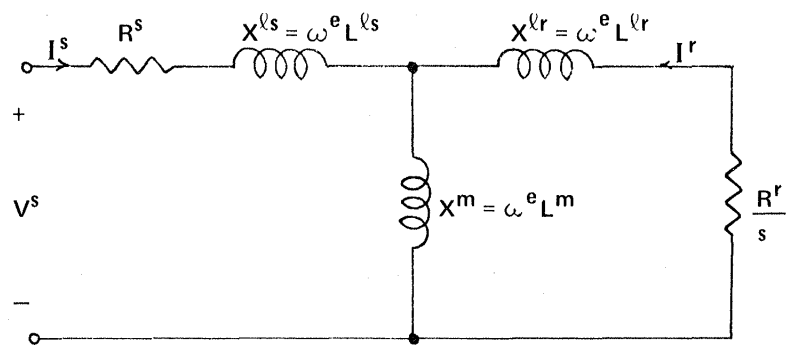
When this voltage rating is scaled down from its 140 Hz value to the equivalent 60 Hz value, assuming a constant volts-per-Herz ratio, we find

$$V_1^{\ell\ell}{}_{60\ \mathrm{Hz}} = \frac{60}{140} \times V_1^{\ell\ell}{}_{140\ \mathrm{Hz}} = 37V \qquad [3.2]$$

Consideration of convenient winding configurations for the selected E-Plus™ motor led to the specification of a 36V stator winding under 60 Hz excitation conditions. With the assistance of Gould's Electric Motor Division, the motor was fitted with a lap winding appropriately adjusted for this 36V rating.

Motor Equivalent Circuit and Measured Performance

Upon arrival of the selected rewound induction motor at Gould Laboratories, a set of tests was carried out to determine values for the motor single-phase equivalent circuit. As shown in Figure 3.2, this process involves identification of five key motor impedances: stator winding and rotor squirrel-cage resistances (R^s and R^r), stator and rotor leakage reactances ($X^{\ell s}$ and $X^{\ell r}$), and magnetizing reactance (X^m). Reactances are specified at a base frequency of 60 Hz and resistances are adjusted for operating temperatures of 70°C. ω^e is the electrical excitation frequency and ω^r is the mechanical frequency.



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$\omega^e = 2\pi \times f_{ex}$

$s = \frac{\omega^e - \omega^r}{\omega^e}$

$T = 70^oC$

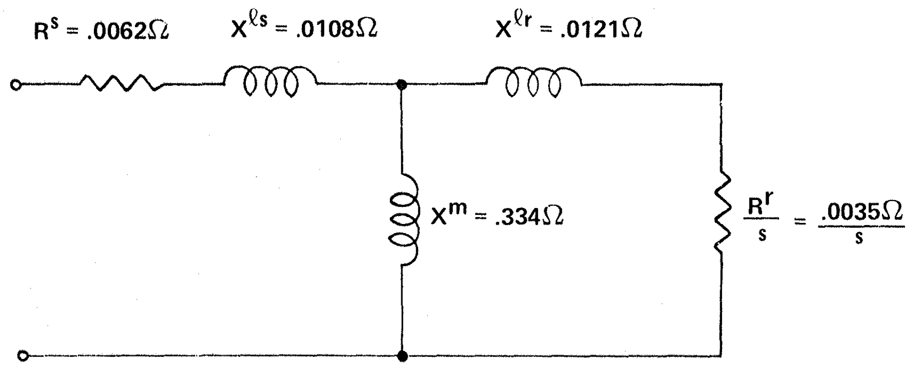
Figure 3.2 Induction Motor Equivalent Circuit

A set of motor tests was conducted to determine the machine parameters consisting of the following specific characterization tests:

- stator resistance measurement
- no-load saturation test
- locked-rotor test
- steady-state load test

Since all of these tests are standard in the industry, the interested reader is referred elsewhere for more details on testing procedures.[2] The results of this testing are presented in Figure 3.3 in the form of an identified equivalent circuit. These resistance and inductance values are relatively insensitive to excitation frequency provided that the motor is operating at low slip; that is, the rotor shaft frequency is within a few percent of the excitation frequency, typical for steady-state operation. However, if the rotor is locked to prevent rotation while the stator is excited at a substantially different frequency, frequency-dependent skin effects alter the rotor impedance values from their low-slip values. Thus, Figure 3.3 includes standstill values for the rotor resistance and leakage reactance for 60 Hz excitation. The equivalent circuit values shown in this figure fall within the range of expected impedance values for an industrial-grade induction motor of this rating.

Figure 3.4 complements the equivalent circuit presentation by providing results of the no-load saturation test for 60 Hz excitation. These results show that, consistent with good motor design practice in industrial machines, the motor is operating just below the knee of the magnetic saturation curve during rated voltage excitation. That is, the motor iron magnetic flux levels are maintained as high as possible without causing substantial saturation of the iron core with the associated losses. However, the curve also demonstrates that there is substantial latitude for temporary excursions towards the saturation region of the iron core if necessary to extract higher torques from the motor.



(0437)

AT STANDSTILL:

$X^{\ell r} = .0108\Omega$

$R^r = .0048\Omega$

Figure 3.3 Identified 36V Induction Motor Parameters at 60Hz Excitation Frequency

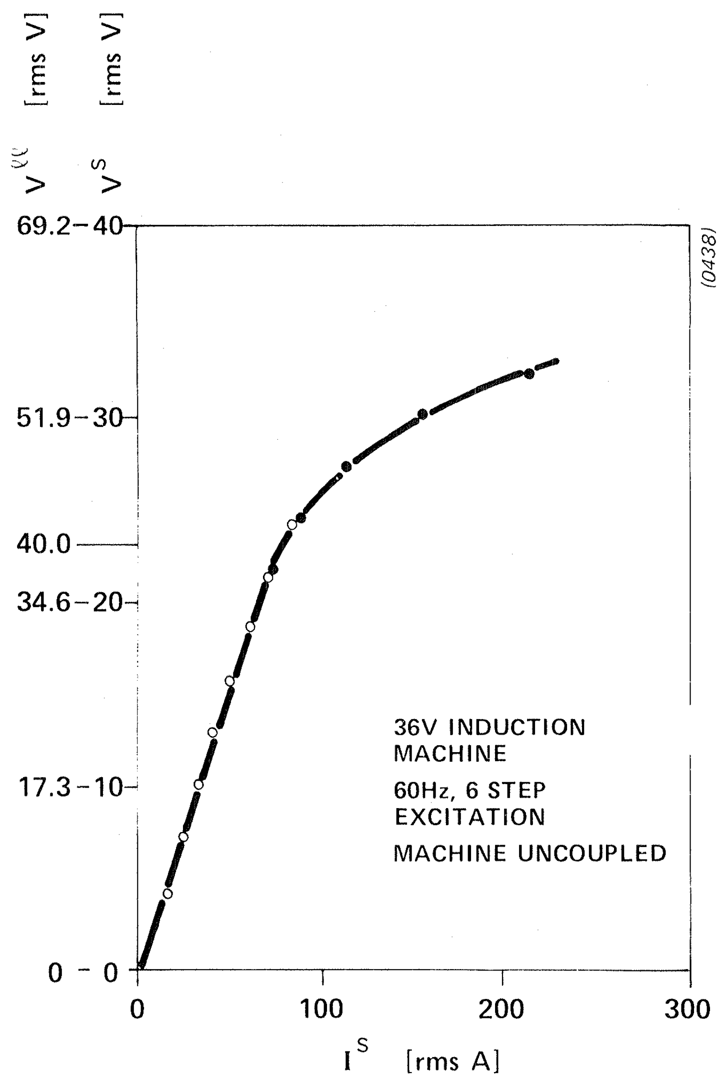


Figure 3.4 No Load Magnetization Saturation Test Curve

Measured electrical performance characteristics of the rewound induction motor during 60 Hz six-step excitation are presented in Figure 3.5 as a function of rotor slip. Plotted motor performance parameters include measured phase current (I^s), shaft torque (T^e), and motor efficiency (η_m). In addition, predictions for the phase current and torque generated by the equivalent circuit of Figure 3.3 are also included with the measured curves in Figure 3.5. Measured and predicted torque values agree quite well over the full tested slip range (0 to 4% slip). However, predicted currents are several percent lower than measured currents due in large part to the additional current harmonics resulting from the nonsinusoidal six-step excitation which are not reflected in the predictions.

Measured motor efficiency values presented in Figure 3.5 hover in the vicinity of 80% for most of the slip operating regime. These values are several percent lower than typical efficiency values for standard industrial induction motors with 60 Hz sinusoidal excitation.[3] Clearly, this loss of motor efficiency due to harmonic currents directly impacts overall system efficiency in an undesirable manner. Although techniques do exist for specifically designing the induction motor to minimize the effects of nonsinusoidal excitation,[4] such work fell outside the scope of the present program. In the absence of that degree of freedom, attention has been focused on reducing the harmonic content of the controller voltage output waveforms, as will be described later in this report.

3.2 Control Strategy

Desired Characteristics

The fundamental requirement for the selected control strategy is that it give the overall system the characteristics of a torque controller. That is, the system must respond to torque requests delivered to the propulsion system by the operator through the accelerator and brake pedal positions. The control strategy has responsibility for converting these torque requests into the appropriate inverter commands to control the excitation of the ac motor. Specifications for the response time of the propulsion system to step changes

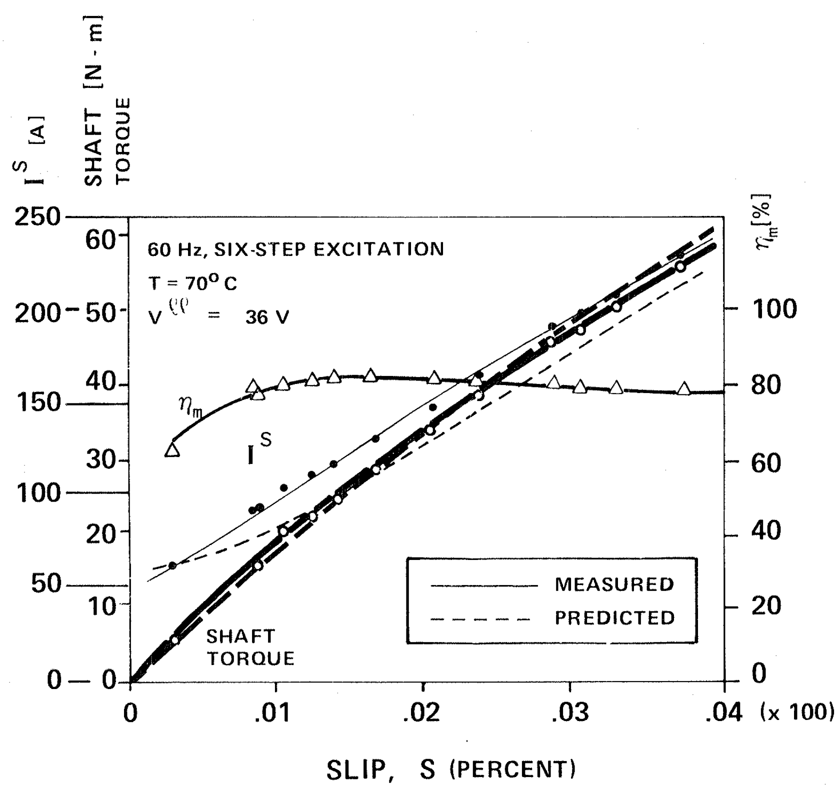


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Figure 3.5 36V Induction Motor Load Test Performance in the torque command are not explicitly defined in the contract system requirements. However, the rather sluggish response characteristics of the human operator make a response time on the order of 100 ms a reasonable goal for the EV controller. This response time goal applies over the full range of propulsion system output shaft speeds.

In addition, the control strategy is responsible for protecting the propulsion system components from operator torque requests which exceed system capabilities. This is particularly true at low speeds where component current capabilities could be exceeded if the operator torque requests were not suitably limited as part of the control strategy. The locus of system torque-speed operating points required to meet system performance specifications have been discussed previously in Section 2.3 and summarized graphically in Figure 2.4 On the basis of these minimum requirements, a decision was made early in the design process to require at least 60 N-m from the propulsion system at all vehicle speeds less than 48.3kph (30 mph) for improved acceleration. As shown in Figure 2.4, peak torque production requirements then fall off gradually as the vehicle speed increases beyond 30 mph towards the 55 mph maximum.

Basics of AC Motor Control

The nature of the EV propulsion system application requires that the ac induction motor deliver substantial steady-state torque over a wide speed range. If restricted to fixed-frequency excitation (e.g., 60 Hz line excitation), a high-efficiency induction motor is not capable of meeting this requirement. Inspection of the motor shaft torque versus speed characteristic for an induction motor during fixed-frequency excitation at frequency f_{ex} clarifies the source of this limitation (see Figure 3.6). Steady-state operation is limited to a narrow range of shaft speeds adjacent to the electrical excitation frequency corresponding to the negatively-sloped portion of the Figure 3.6 torque-speed characteristic. Note that the induction motor produces no steady-state torque when the rotor rotates exactly at the excitation frequency; braking (negative) torque is generated and power is fed back to the source when the rotor shaft frequency exceeds f_{ex}.

Excitation frequency and excitation voltage amplitude provide two important degrees of freedom in varying the operating speed of the induction motor. As shown in Figure 3.6, the steady-state operating point is determined by the intersection of the motor generated torque versus speed characteristic and the load torque versus speed characteristic. Since the amplitude of the motor torque-speed curve is proportional to the square of the applied excitation voltage, $(V^{\ell\ell})^2$, the steady-state operating point can be varied over a limited speed range by adjusting the excitation voltage at a fixed excitation frequency. This technique of induction motor speed control is illustrated in Figure 3.7.

In contrast, if the excitation source is designed such that the motor excitation frequency can be varied while holding the excitation voltage fixed, a continuous family of induction motor torque speed curves in produced as shown in Figure 3.8. A different curve corresponds to each excitation frequency value. All of these curves have virtually identical shapes although their amplitudes decay as the curves shift to the right (higher rotor speeds) for increasing excitation frequency values. The torque-speed curve amplitude scaling factor is proportional to the square of the air-gap flux $(\lambda_{ag})^2$, where the air-gas flux, λ_{ag}, can be approximated as well as

$$\lambda_{ag} = K_0 = \left(\frac{V^{\ell\ell}}{f_{ex}} \right) \qquad [3.3]$$

where K_0 is a machine constant. Thus, for fixed excitation voltage amplitude (fixed $V^{\ell\ell}$), the torque-speed curves scale as the inverse square of the excitation frequency, $(1/f_{ex})^2$.

Since the machine air-gap flux magnitude gradually increases as $1/f_{ex}$ for decreasing values of excitation frequency when the motor voltage is fixed, the motor iron becomes magnetically saturated during low frequency operation. In order to avoid this undesirable operating mode while retaining the advantages of variable-frequency operation, it is necessary to consider control techniques which simultaneously vary the excitation voltage and frequency.

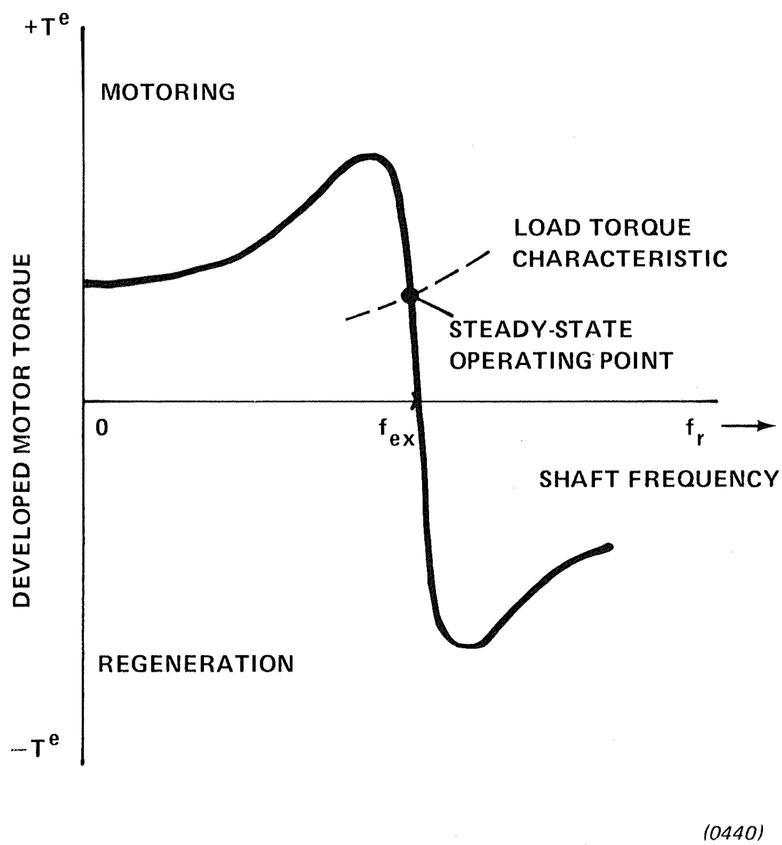

Figure 3.6 Induction Motor Torque vs. Frequency Characteristic for Fixed Voltage, Fixed Frequency Excitation

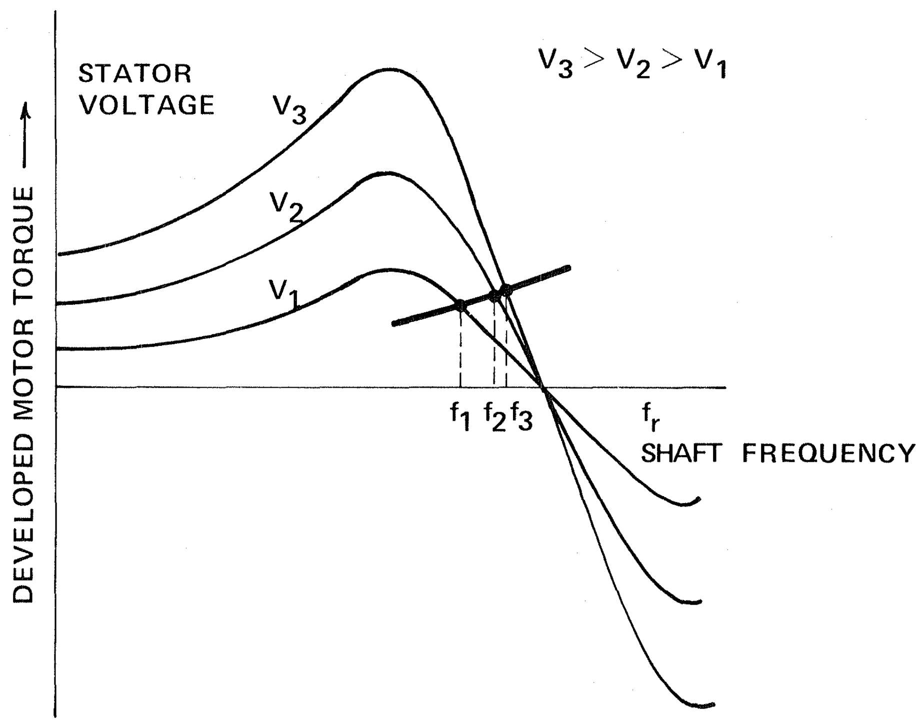

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Figure 3.7 Principle of Shaft Speed Control by Means of Variable Stator Voltage

One of the most popular techniques for coordinating the machine voltage and frequency excitation to avoid saturating the motor's iron core consists of adjusting the voltage so that the air-gap flux magnitude stays constant as the frequency is varied. When the air-gap flux is held constant, the locus of torque-speed curves for variable-frequency operation all have the same magnitude and shape, as shown in Figure 3.9. In this manner, the machine's full useful torque-producing capability becomes available over the entire speed range. As shown in Equation 3.3, regulating the air-gap flux to be constant requires that the voltage amplitude be varied in direct proportion to the excitation frequency. This scheme, commonly referred to as constant Volts-per-Hertz (V/Hz) operation, plays a role in the implemented control algorithm. However, the approximate nature of Equation 3.3 as well as basic system constraints have made it necessary to adopt a voltage algorithm which differs from the basic constant V/Hz relation in several important ways. Details of these differences will be provided in the following sections of this report.

Variable-Frequency Implementation Fundamentals

Having reviewed several of the available techniques for achieving variable speed control of ac motors, discussion in this section will be devoted to how these techniques have been incorporated into the final EV controller. At the heart of this implementation is an array of semiconductor switches illustrated schematically in Figure 3.10. This inverter power conversion stage generates the ac voltage waveforms needed to excite the induction motor using energy supplied by the dc battery source.

In its simplest operating mode, the two switches in each of the three legs of the inverter operate as a complementary pair, one switch closing as soon as the complementary switch opens. In this manner, the line-to-line motor terminal voltages are constrained at any time instant to take on one of three values, $+V_{bat}$, $-V_{bat}$ or 0, where V_{bat} is the battery terminal voltage. By properly coordinating the switching instants as shown in Figure 3.10, a balanced three-phase set of voltage waveforms is developed at the motor terminals. Although these waveforms are nonsinusoidal, the largest proportion

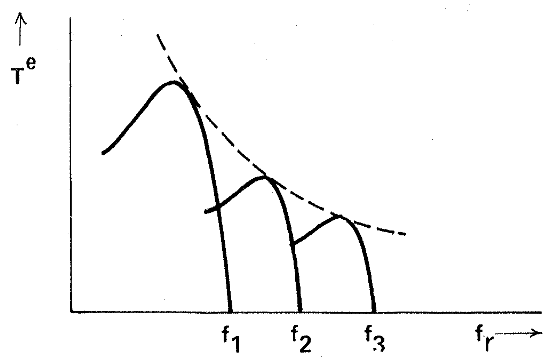


Figure 3.8 Constant Source Voltage, Variable Excitation Frequency

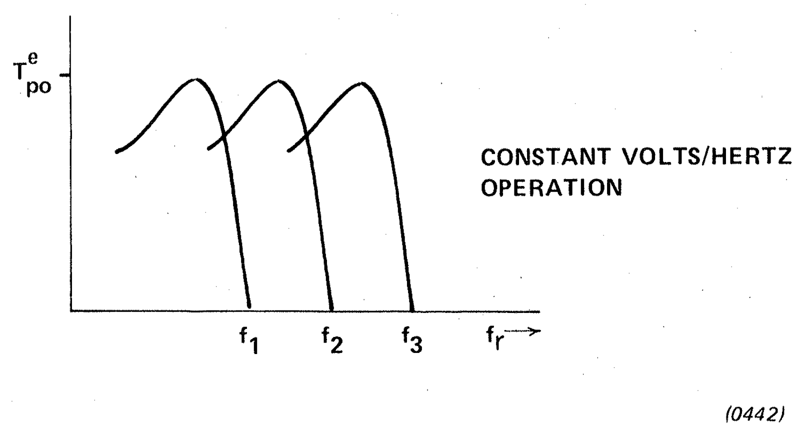
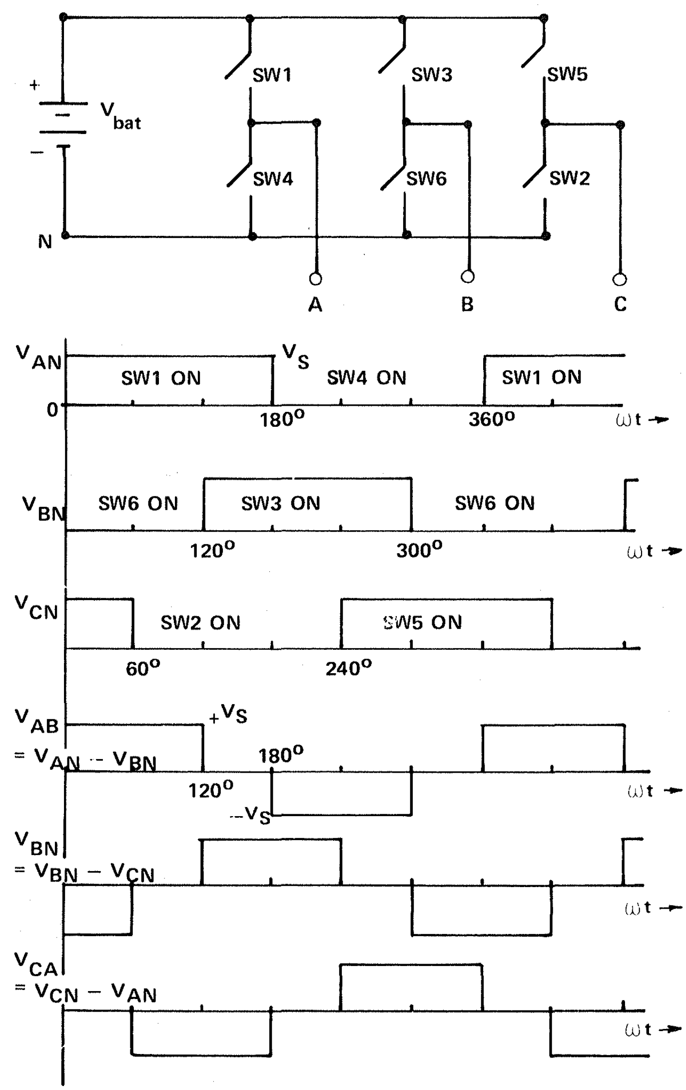


Figure 3.9 Variable Source Voltage, Variable Excitation Frequency



(0443)

Figure 3.10 Inverter Switch Configuration and Associated Switch Sequencing Diagrams for Producing a Set of Balanced Three–Phase Line-to-Line Voltage Waveforms at Terminals A, B, and C of their spectral energies are concentrated in their fundamental frequency components.

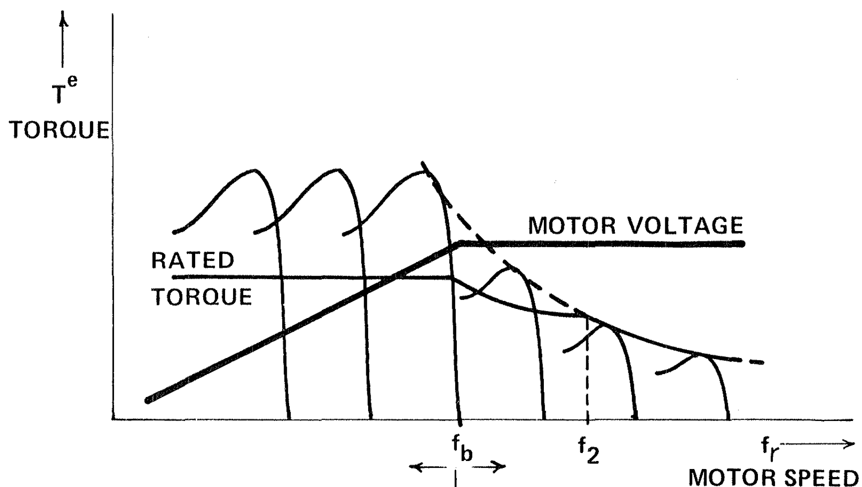
By simply varying the rate at which the switching sequence of Figure 3.10 proceeds, the frequency of the motor excitation can be varied over a wide continuous range. Thus, the basic requirement of variable-frequency speed control is satisfied. However, a second key requirement for variable-frequency speed control described in the preceding section is the capability of varying the applied motor voltage as the frequency is varied. Note that the simple waveforms displayed in Figure 3.10 do not satisfy this requirement since their amplitudes are fixed at the source voltage amplitude, V_{bat}.

One technique for providing this variable voltage capability is to add a power conversion stage between the battery source and inverter input to adjust to the dc bus voltage. Thus, the amplitudes of the Figure 3.10 waveforms become variable rather than fixed values. However, in order to avoid the cost of introducing this additional power stage, an alternate approach has been adopted which achieves this independent voltage control in the inverter stage itself. This is accomplished by increasing the sophistication of the inverter-stage switching algorithm using pulse-width modulation (PWM) techniques adapted from communications systems work. Such PWM algorithms provide the drive designer with a powerful tool for shaping the inverter output waveforms.

Since the voltage waveforms delivered by the inverter power stage are non-sinusoidal, undesirable harmonic components are present in the motor excitation waveforms of Figure 3.10. These harmonics produce pulsating torques and losses in the machine without contributing to the average torque, and hence reduce the system efficiency. Sufficient degrees of freedom are inherently provided by the pulse-width modulation algorithm to permit the concentration of the spectral energy of the generated voltage waveforms in the fundamental frequency component. The amplitude of the fundamental component is independently adjusted by means of a duty cycle control known as the modulation index. Further details about the implemented PWM voltage control algorithm are found in Section 4.

Fundamental voltage component amplitudes provided by the PWM alogrithm are limited to a maximum value set by the source voltage, V_{bat}. In fact, under maximum output voltage conditions the motor terminal voltage waveforms are identical to the simple "six-step" waveforms as shown in Figure 3.10. As a result of this upper limit, the propulsion system has been designed to operate in two distinct regimes during a typical driving cycle. At all speeds below a base frequency f_b, the motor voltage is controlled to follow a modified constant V/Hz program designed to hold the motor air-gap flux constant at its rated value. The resulting torque-speed curves associated with excitation frequencies in this regime all have the same shapes and amplitudes as illustrated in Figure 3.11. This operating regime is commonly referred to as the "constant torque" regime, consistent with the terminology typically applied to separately excited dc motors during variable armature voltage, fixed field strength operation.

When the excitation frequency is increased to values exceeding the base frequency f_b, insufficient battery voltage is available to maintain the motor air-gap flux at its rated value. Instead, the inverter delivers six-step waveforms to the motor terminals, providing a "full-on" motor voltage directly proportional to the battery terminal voltage. As explained earlier in this section, increasing the excitation frequency with a constant motor voltage results in a set of torque-speed curves with decreasing amplitudes as shown in Figure 3.11. Although the torque amplitudes of these curves actually scale as $(1/f_{ex}{}^2)$ rather than $1/f_{ex}$, this operating regime is typically referred to as the "constant horsepower" regime; such terminology is consistent with that developed for separately excited dc motor drives to describe similar performance in the field-weakening operation regime. Note that a true constant horsepower operating locus can be achieved, i.e., $T^e \propto 1/f_{ex}$, provided that the rated operating point at the base frequency f_b occurs at a slip less than the peak torque pullout slip. In this case, constant horsepower operation is achieved over a limited frequency range by gradually increasing the slip frequency until the peak torque value is reached at some elevated frequency, f_2 (see Figure 3.12). Above f_2, maximum available torque is limited to the $(1/f_{ex})^2$ locus described earlier.



- CONSTANT TORQUE REGIME
- CONSTANT FLUX OPERATION
- PWM VOLTAGE CONTROL

- CONSTANT POWER REGIME
- "FIELD WEAKENING" OPERATION
- SIX-STEP EXCITATION; MAXIMUM VOLTAGE

(0444)

Figure 3.11 Adopted Voltage and Frequency Control Strategy

In response to this program for motor excitation as a function of frequency, the full torque-speed operating locus for the propulsion system covers an area with the approximate shape shown in Figure 3.12. The compatibility of this torque-speed locus with the performance requirements discussed in Section 2.3 is quite evident by a comparison of Figure 3.12 and Figure 2.4. As indicated in Figure 3.12, the torque-speed operating locus for regenerative operation (negative braking torque is essentially the mirror image of the motoring locus (positive propulsion torque) reflected about the speed axis. This property results from the fundamental symmetry of the induction motor's torque-speed curve (Figure 3.6) about the zero-torque synchronous speed point during fixed-frequency constant voltage operation.

Figure 3.12 represents a simplified and somewhat idealized sketch of the propulsion system's operating locus intended to illustrate the fundamental concepts. The actual operating locus for the assembled prototype system as presented in Section 6 of this report deviates somewhat from this idealized shape due to controller implementation details which will not be addressed until later in this report. Notwithstanding, Figure 3.12 contains sufficient detail to set the stage for the propulsion system control strategy description presented in the following sections.

Slip Control Strategy

The propulsion system control module must respond to operator torque requests by properly adjusting the motor excitation frequency and terminal voltage to produce the desired torque. Several different strategies for executing this coordinated voltage and frequency excitation control have been developed over the years, each distinguished by its particular performance and implementation characteristics. One implementation feature shared in common by nearly all of these candidate control strategies is the necessity of a motor shaft tachometer. The availability of shaft speed information provides a powerful feedback variable to the control module for achieving system performance objectives. Although the undesirability of a tachometer in the propulsion system is generally acknowledged because of its expense and fragility, a satisfactory strategy for eliminating this key component is not yet commercially available.

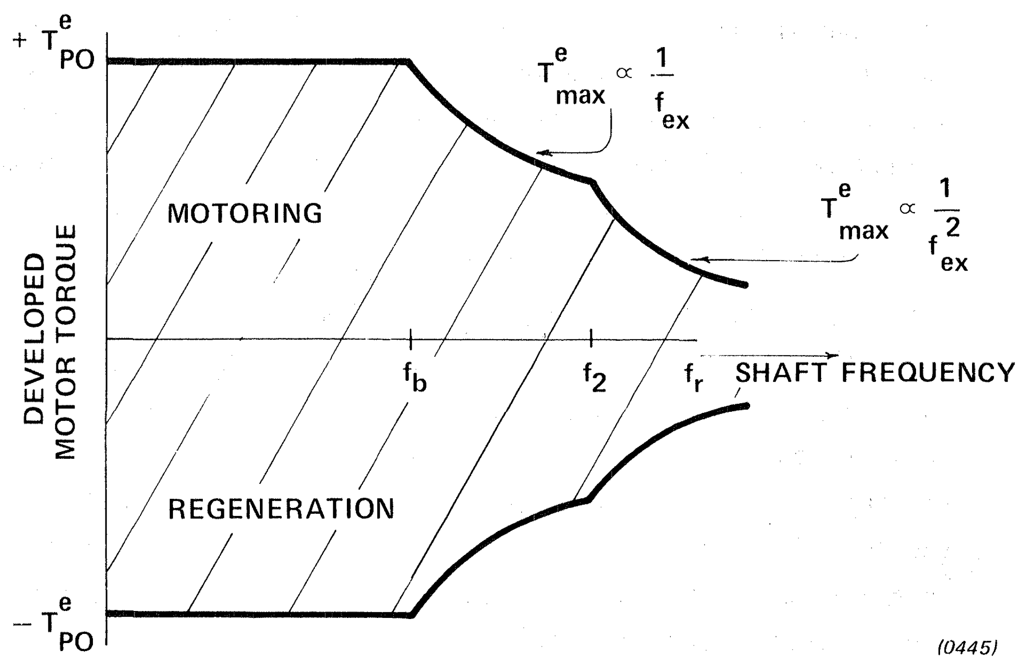


Figure 3.12 Simplified Illustration of System Torque -Speed Operating Locus

The principle of the chosen control strategy can be best described by referring to the expanded plot of the motor torque vs. motor speed relationship in the vicinity of the excitation frequency shown in Figure 3.13. Rotor speed in this figure is plotted as a difference frequency between the excitation and rotor frequencies ($f_{ex}-f_r$), referred to henceforth as the slip frequency, $f_{s\ell}$. Note that the developed motor torque is very sensitive to slip frequency values for a high efficiency induction motor; motor torque increases from zero to its rated value as the slip frequency changes by approximately 1 Hz.

Provided that the motor magnetic air-gap flux is held constant, the developed motor torque as a function of slip frequency plotted in Figure 3.13 is independent of excitation frequency, f_{ex}. That is, the developed torque will remain constant as the vehicle speed varies, provided that the excitation frequency is adjusted to hold the difference frequency between the shaft speed and the excitation frequency constant, and the excitation voltage is adjusted to maintain the motor flux constant as well. This feature provides the basis for a powerful torque regulation scheme known generally as slip control. Since the instantaneous shaft frequency, f_r, is available from the tachometer, the inverter excitation frequency, f_{ex}, is controlled by adding or subtracting an adjustable difference frequency, $f_{s\ell}$ to the rotor frequency. A schematic drawing of the basic slip control configuration is quite straightforward, as shown in Figure 3.14. One of the desirable characteristics of this control scheme is the near-linear dependence of motor torque on slip frequency in both the motoring (positive torque) and regenerative braking (negative torque) regimes. This linearity becomes seriously degraded only if the slip frequency is increased to values in the vicinity of the peak torque pullout slip.

Independence of motor excitation frequency and motor torque during slip frequency control is dependent on the condition of constant amplitude of the rotating magnetic air-gap flux wave. This flux amplitude must be held constant despite changes in the machine excitation frequency and torque loading which would change the flux amplitude if the voltage were held constant. The dependence of flux on frequency and loading can be described most easily with the help of the machine steady-state equivalent circuit, shown in Figure 3.15. Air-gap flux magnitude can be expressed as the product

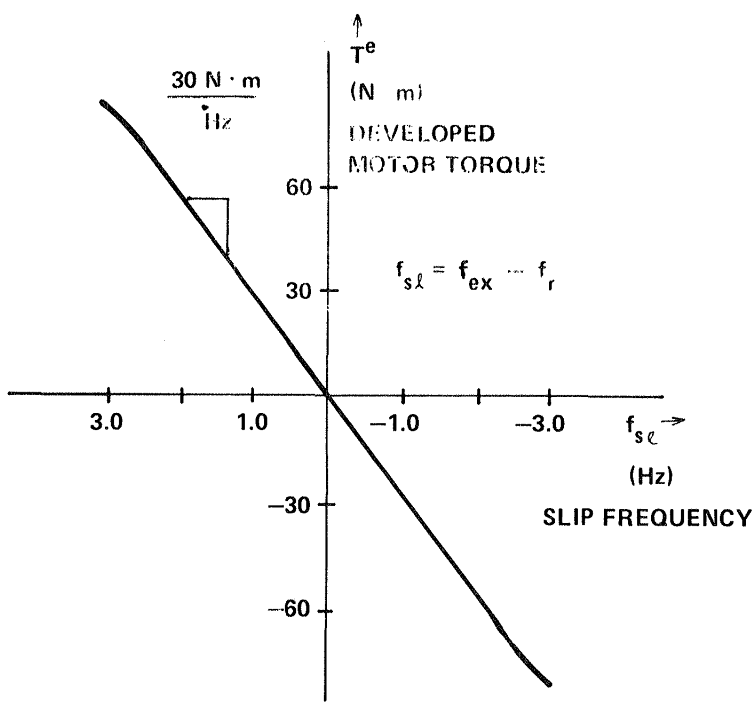


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Figure 3.13 Induction Motor Torque vs. Slip Curve in the Vicinity of the Excitation Frequency ($f_{s\ell} = 0$) for Rated Air-Gap Flux Operation

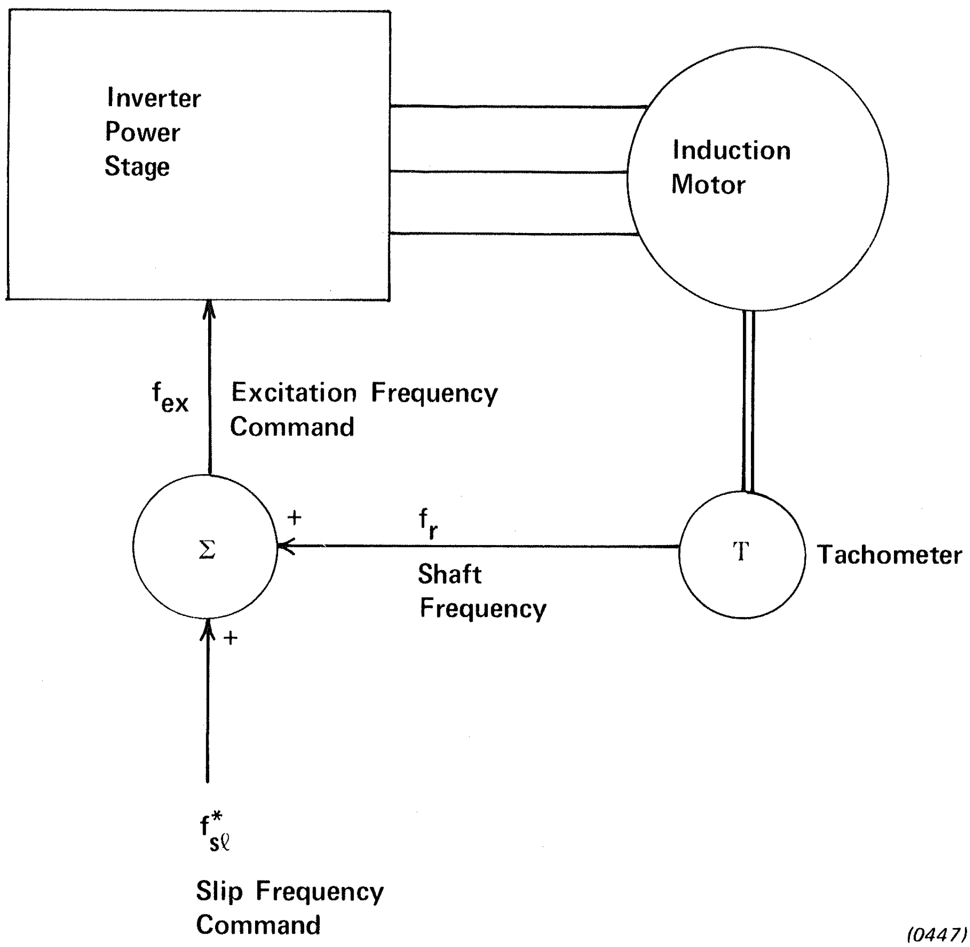
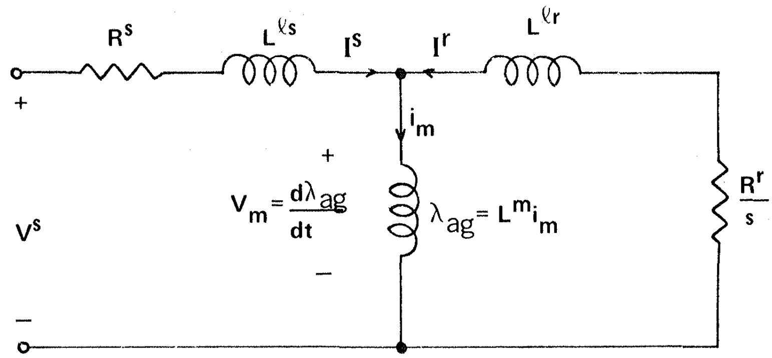


Figure 3.14 Slip Frequency Control Block Diagram



(0448)

Figure 3.15 **Equivalent Circuit of Induction Motor Highlighting Air-Gap Flux Dependence on Frequency and Loading**

of magnetizing inductance and the current through this circuit branch, That is,

$$\lambda_{ag} = L^m i_m \qquad [3.4]$$

As described earlier, the inductive nature of the motor equivalent circuit implies that, as a first-order approximation, motor voltage must be increased linearly with frequency to maintain constant flux. However, this simplified relation does not account for the effect of the machine loading. As the developed motor torque increases, the impedance of the rotor branch of the motor equivalent circuit decreases because of the increase in slip, s, which reduces R^r/s. For a given motor voltage amplitude and excitation frequency, an increase in the rotor current causes a decrease in the magnetizing current, i_m, because of increased stator resistance and leakage reactance voltage drops. Thus, the flux amplitude decreases as the motor loading increases, assuming constant voltage excitation. This phenomenon is exactly analogous to the speed regulation of a dc motor with loading caused by the armature resistive voltage drop.

Flux Regulation

Various strategies are available for regulating the magnitude of the air-gap flux. One class of flux regulation schemes relies on special flux transducers such as Hall effect probes and voltage-sensing coils installed inside the machine. By directly measuring the flux amplitude, a closed-loop regulator can be designed to adjust the motor excitation to hold the flux amplitude constant despite frequency and loading changes. Unfortunately, there are no manufacturers who produce standard industrial grade induction motors with flux sensors installed as standard equipment; rather, such sensors must be retrofitted into the motor at considerable expense. Consistent with the goal of designing an economical propulsion system based on the standard industrial grade induction motor, a decision was made to consider alternatives to internal flux sensors for flux regulation.

Although alternative motor variables such as phase currents are available for closing a flux regulation loop, one of the most straightforward approaches to controlling flux amplitude uses an open-loop configuration based on a priori knowledge of the motor's eqivalent circuit. Although an open-loop scheme by its nature sacrifices some accuracy in the flux regulation, the EV propulsion system performance requirements provide sufficient flexibility to assure the scheme's viability in this application. In particular, the most important characteristic of the torque-to-input command signal relationship is monotonicity rather than precise linearity.

Although implementation details of the flux regulation scheme will be reserved for the following section, the nature of this scheme can be described here in a straightforward manner. The amplitude of the air-gap flux (λ_{ag}) during steady-state operation is a unique function of the excitation frequency (f_{ex}), the excitation voltage amplitude (V^s), and the generated torque (T^e). That is

$$\lambda_{ag} = g_1 (f_{ex}, V^s, T^e). \qquad [3.5]$$

If we demand that the air-gap flux be held constant, then the excitation voltage can be expressed as a unique function of the other two variables, frequency and torque. That is

$$V^s = g_2 (f_{ex}, T^e) \text{ for } \lambda_{ag} = \text{constant}. \qquad [3.6]$$

Although a direct measurement of the developed torque is not available in the implemented system, equality of the torque command, T^{e*}, and the actual torque T^e is implicit in the regulating nature of the control circuitry. Thus the expression for the voltage can be rewritten as

$$V^s = g_2 (f_{ex}, T^{e*}) \qquad [3.7]$$

where both f_{ex} and T^{e*} are explicitly available as control inputs. This calculation is displayed schematically in Figure 3.16. V^{s*} is shown in the figure with an asterisk since the output of this block is a commanded value which is delivered to the pulse-width modulation circuitry.

The actual excitation voltage delivered to the motor is limited to a maximum value V^{s}_{max} which is directly proportional to the battery voltage. Hence, the PWM control circuitry simply saturates at this maximum value when the command signal V^{s*} exceeds V^{s}_{max}. This has the effect of causing the flux amplitude to fall off inversely with excitation frequency for further frequency increases. As described in a previous section, such operation corresponds to the "constant horsepower" regime since the amplitude of the torque-speed curve decreases for further increases in the excitation frequency. As a result of entering this operating regime, the slope of the torque vs. slip frequency characteristic shown in Figure 3.13 gradually decreases as the frequency increases above the transition value. In other words, the 'gain' of the system's accelerator pedal relating the torque to pedal position falls off at elevated speeds in the constant horsepower regime.

Dynamic Performance

Two issues which are of interest with respect to the dynamic performance of any candidate control alogrithm are the system stability, and dynamic response to input command changes. Dynamic characteristics of the slip frequency control system are generally quite compatible with the performance requirements for an electric vehicle propulsion system. General features of these dynamic characteristics will be described in the following paragraphs.

In the strictest sense, any torque controller is statically unstable at all operating points when driving a constant torque load which is independent of speed; specifically, any difference between the motor and load torque causes the motor to accelerate. Provided that this is the case, it has been shown that the dynamic stability of a slip-frequency controlled drive is superior to that of a conventionally excited motor with independent voltage

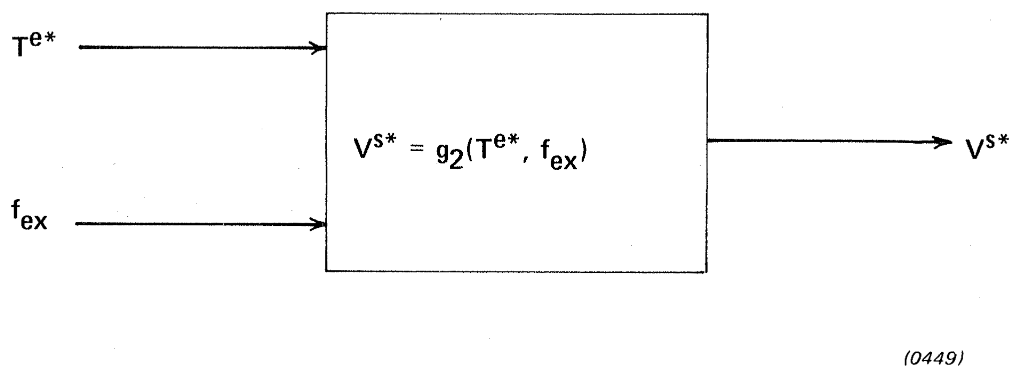


Figure 3.16 Schematic Diagram of Stator Voltage Calculation Algorithm

and frequency excitation.[5] That is, the damping ratio of the dominant poles in the slip-frequency controlled system is generally higher than those of a comparable conventional system. This is of particular importance at low excitation frequencies in the range of 10 to 20 Hz where conventionally-excited induction motors typically operate under conditions of marginal dynamic stability.[6]

Transient response of the developed motor torque to step changes in the input torque command is the second important dynamic issue. During the course of the doctoral thesis work of A. Miles at the University of Wisconsin [5], the dynamic response of the basic slip-frequency torque controller was investigated at a variety of operating points. Using the parameters of the EV propulsion system, analytical results derived from this work show that the small-signal transient torque response of the slip-frequency system is dominated by a decaying time constant of 100 ms or less over the full motor operating speed range. More detailed examination of the system natural frequencies indicates that the step transient torque response is adequately damped at all speeds, with a slightly oscillatory underdamped response occurring at excitation frequencies of 30 Hz (900 rpm) and lower. Experience with the actual system has generally borne out these calculations, although sampling delays introduced by the control logic implementation have extended the dominant time constant of the torque response to the range of 150-200 ms for most operating conditions. In addition, an adjustable RC circuit has been included in the torque control logic to allow the dominant time constant to be further extended by controlling the rise/fall time of the operator torque request.

Control System Implementation

As described in the last section, the propulsion system is given the characteristics of a torque controller by means of a slip-frequency control scheme requiring air-gap flux regulation. Implementation descriptions for this control system are presented in this section at the block diagram level, leaving detailed logic hardware and software presentations for later sections.

In order to place the control system in its proper perspective, Figure 3.17 provides a block diagram of the entire propulsion system. The voltage modulator logic prepares the thyristor gating signals according to a pulsewidth modulation algorithm. These signals are delivered to the inverter power stage where the actual dc to variable frequency, variable voltage power conversion takes place. Systems control functions are centralized in the system control module which gathers the necessary internal transducer signals as well as the operator torque request in order to perform the control functions. In addition, the system sequencing (e.g., start-up) and protection functions are performed in the system control module. At the heart of this module is a microprocessor which accomplishes many of these tasks via software real-time control.

A block diagram of the slip-frequency torque control algorithm performed in the system control module is presented in Figure 3.18. The lower half of this diagram consists of the induction motor slip-frequency control algorithm while the upper half executes the necessary flux regulation. Each of these two sections will be described in turn.

Slip Frequency Control Functions

The slip-frequency control functions are conceptually straightforward. First, the operator torque request, T^{e*}, is converted into an equivalent slip frequency command, $f^*_{s\ell}$. The relationship between the developed motor torque and applied slip frequency is nearly linear in the useful slip operating range between 3 Hz (motoring operation) and -3 Hz (regenerative braking). During rated flux operation this torque-slip relationship is essentially independent of the excitation frequency, with the motor torque increasing at a rate of 30 N-m per 1 Hz slip frequency in both the motoring and braking regions. This relationship has been plotted previously in Figure 3.13.

As a result of the simplicity of the actual motor torque-slip frequency relationship ($T^e = g\,[f_{s\ell}]$), the inverse of this relationship ($f_{s\ell} = g^{-1}\,[T^e]$) can be modeled very adequately as a linear function for both motoring and braking.

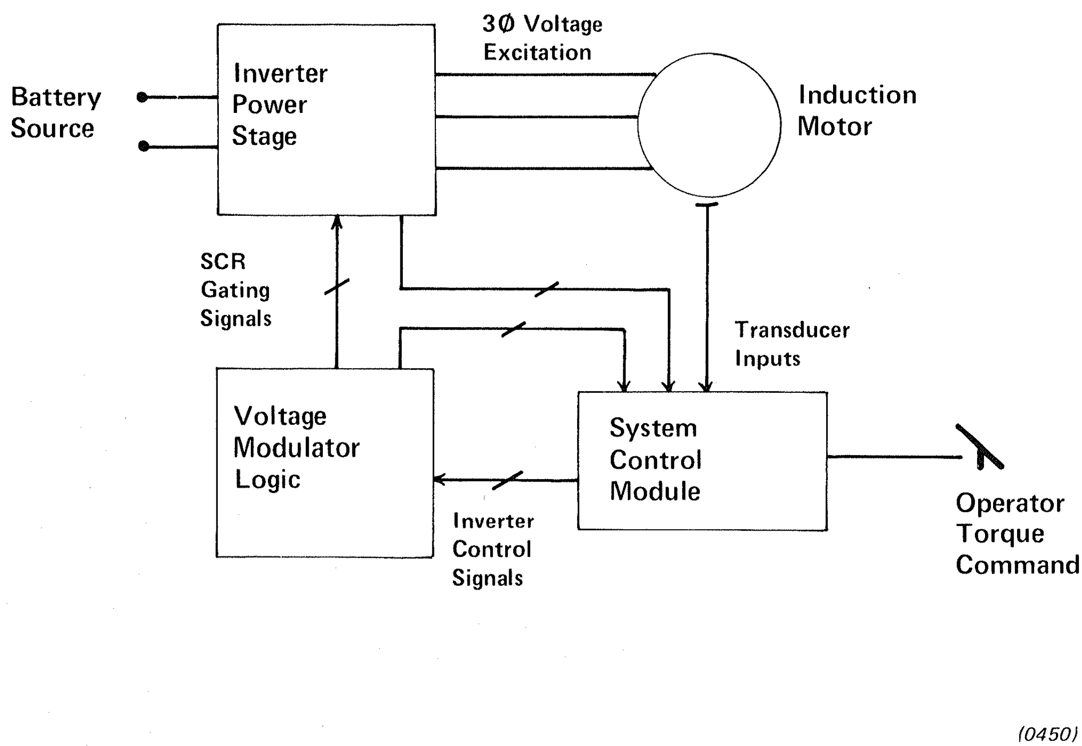


Figure 3.17 AC Controller Configuration Block Diagram

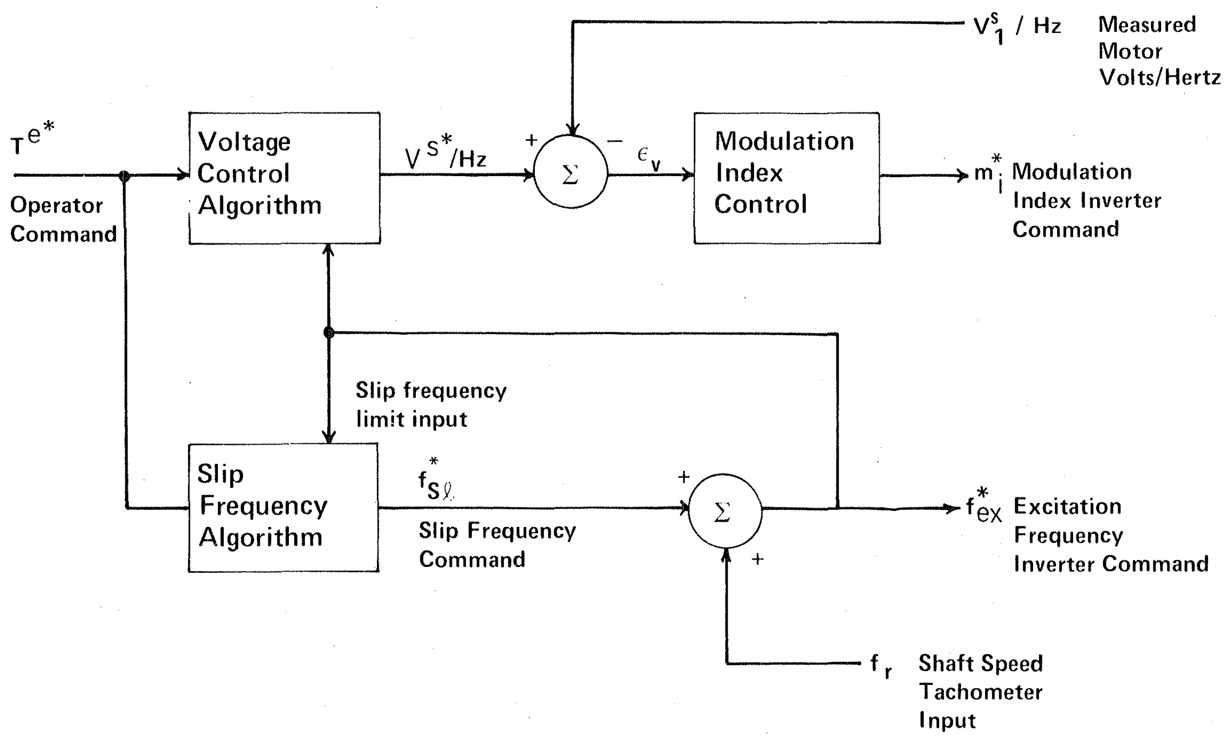


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Figure 3.18 System Control Module Block Diagram

$$f^*_{s\ell} = KT^{e*}, \quad \left| f^*_{s\ell} \right| < f_{s\ell_{max}} \qquad [3.8]$$

where the asterisks signify command values.

A reasonable choice for the gain constant, K, value is the reciprocal of the rated flux torque-slip curve slope, which is (1/30) Hz slip frequency per N-m torque request. That is,

$$K = .033 \text{ Hz/N-m}$$

As a result of this implemented slip frequency algorithm, the overall system gain relating the actual developed motor torque (T^e) to the torque request (T^{e*}) remains nearly constant at 1 throughout the lower speed constant flux region. However, at speeds above roughly 3600 rpm the system enters its declining air-gap flux regime, causing the slope of the motor torque-slip curve to decrease as speed is increased. A decision was made to hold the value of gain constant K relating the slip and torque requests fixed at .033 Hz/N-m at all speeds. As a result, the over all system gain T^e/T^{e*} decays in the flux weakening region as $1/(f_b/f_{ex})^2$, where f_{ex} is the excitation frequency and f_b is the transition frequency value separating the constant flux and flux weakening regimes. Since the highest allowable excitation frequency value is approximately twice the transition value, the system gain decreases from 1 at lower frequencies (f_{ex} < 3600 rpm) to approximately 0.25 at the highest excitation frequencies.

A second task performed in the slip frequency algorithm block is a safe operating regime current limit function. Under steady-state operating conditions, the current drawn by the motor is uniquely determined by the slip frequency and air-gap flux. In fact, at any given flux level, the motor current is a monotonically increasing function of slip frequency which is symmetrical for the motoring and braking regimes. Thus, by limiting the slip frequency command magnitude, $f^*_{s\ell}$, a current limit function is obtained. This functional relationship is known schematically in Figure 3.18 as part of the control system block diagram. The actions of the slip frequency algorithm block in this figure are summarized by the following equations:

$$f^*_{s\ell} = K\,T^{e*}\ , \ \frac{f_{s\ell 2}}{K} < T^{e*} < \frac{f_{s\ell 1}}{K} \qquad [3.9]$$

$$= \ f_{s\ell 1}, \qquad T^* > \frac{f_{s\ell 1}}{K} \qquad [3.10]$$

$$= \ f_{s\ell 2}, \qquad T^* < \frac{f_{s\ell 2}}{K} \qquad [3.11]$$

$$f_{s\ell 1} = \ h_1\ (f_{ex}) \qquad [3.12]$$

$$f_{s\ell 2} = \ h_2\ (f_{ex}) \qquad [3.13]$$

These relationships are illustrated in Figure 3.19. Note that the positive slip frequency limit, $f_{s\ell 1}$ and the negative limit, $f_{s\ell 2}$, are identical at each excitation frequency except at low speeds below 1200 rpm(40 Hz), where $f_{s\ell 2}$ is set at zero. As a result, regenerative braking is not permitted below 40 Hz in order to avoid undesirable current peaking in a speed regime where there is little kinetic energy available for regenerative recovery. This issue will be described in more detail later in this section.

The positive slip frequency limit is held at 3 Hz throughout the constant flux frequency range (0 to 120 Hz) corresponding to a maximum motoring torque of 90 N-m. At frequencies above 120 Hz corresponding to flux weakening operation, the slip limit is progressively relaxed since the motor current and torque developed at each slip frequency gradually decreases as the excitation frequency is raised. In this manner the steady-state motor rms phase current is held within a limit of approximately 350A at all speeds.

Of the various elements composing the system control block diagram in Figure 3.18, the only one accomplished using hardware rather than software is the slip frequency/shaft speed summation operator. This opertion is critical to the entire system since the quality of torque regulation depends directly on the accuracy of the slip frequency addition. Considering the fact that

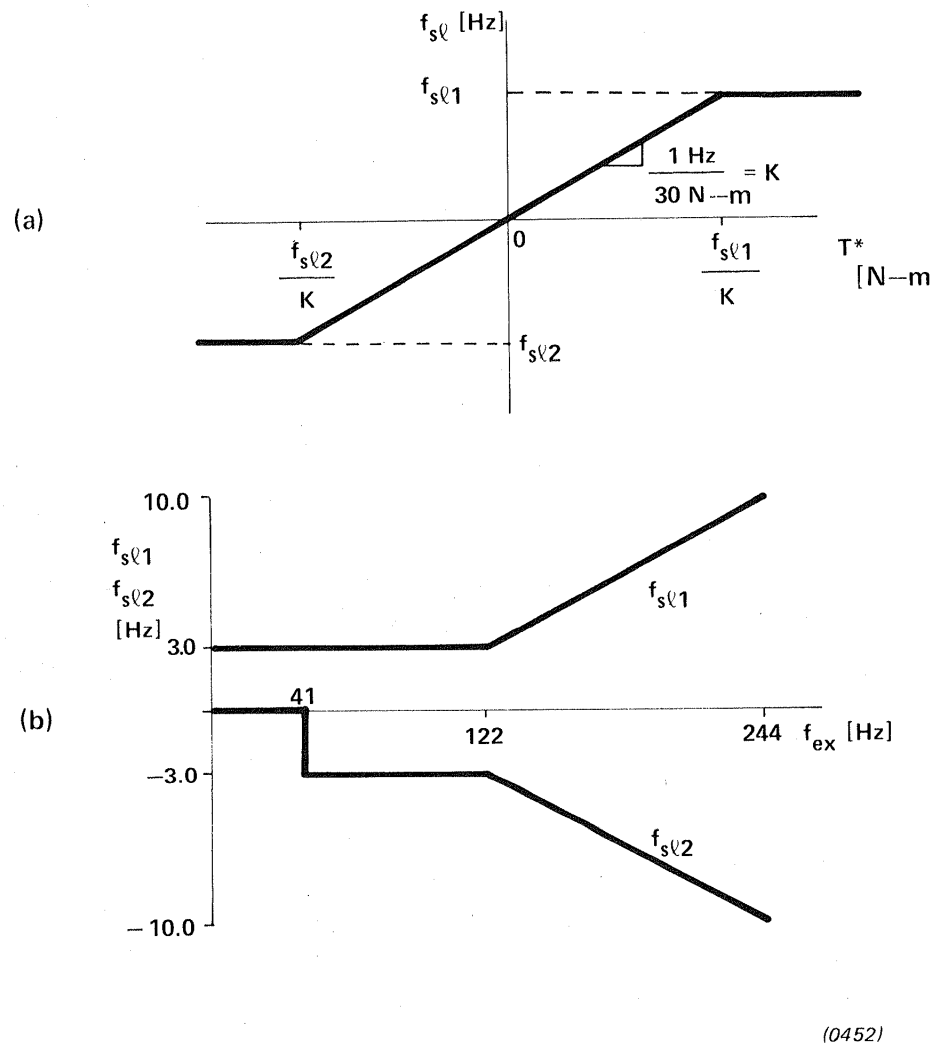

Figure 3.19 Control Algorithms

(a) $f_{s\ell}$ vs. T^{e*}

(b) $f_{s\ell 1}$, $f_{s\ell 2}$ vs. f_{ex}

rated slip is less than 2% of the rated motor speed, there is an acute demand for techniques which permit a small frequency to be accurately summed with a much larger frequency. This goal has been achieved quite admirably in the designed system using special phase-locked loop techniques together with rotor speed information derived from a shaft-mounted optical encoder. Details of this hardware will be presented in a later section of this report. For this discussion it is only necessary to note that slip frequency values can be accurately summed with arbitrary rotor shaft frequency values at a slip frequency resolution of better than 0.1 Hz.

The result of this summation process is a pulse train which is delivered to the voltage modulator block of Figure 3.17, directly setting the fundamental frequency of the inverter power stage f_{ex}. In addition, the value of f_{ex} is an important parameter used internally in the system control module at two key points as shown in Figure 3.18. One of these calculations consists of setting the slip frequency limit as a function of the excitation frequency as described in the preceding paragraphs. In addition, the excitation frequency information is used in setting the voltage amplitude of the inverter output waveforms. This issue of motor flux regulation, which comprises the upper half of the system control module block diagram in Figure 3.18, is described in the following paragraphs.

Desired Terminal V/Hz Alogrithm

The role of the flux regulation algorithm is to control the amplitude of the inverter output fundamental frequency voltage component so that the machine's internal air-gap flux magnitude is maintained nearly constant, independent of operating conditions. This constant flux algorithm has an adverse effect on system efficiency under light-load conditions due to the losses associated with establishing this flux. However, the desire for a straightforward microprocessor-compatible control algorithm and the infrequency of light-load conditions during typical driving cycles, the constant flux algorithm represents a good compromise between system efficiency and complexity.

As discussed earlier in this section, a prior knowledge of the machine's equivalent circuit is used to calculate the necessary terminal voltage for constant air-gap flux as a function of excitation frequency and desired motor torque. Inspection of the equivalent circuit is sufficient to derive the expression for terminal volts/Hz, λ_t, as a function of rated air-gap flux $\lambda_{ag(rated)}$ (in V/Hz), slip frequency, and excitation frequency. Strictly speaking, use of this expression requires one to assume that this system is continually operating under steady-state or quasi-steady-state conditions. The linearized expression for torque as a function of slip frequency during constant flux operation, ($T^{e*} = K f^*_{s\ell}$), is used to eliminate the frequency variable in favor of torque, yielding the final desired relationship

$$\left|\frac{V_1^{\ell\ell}}{f_{ex}\sqrt{3}}\right| \equiv \lambda_t = \lambda_{ag_{rated}} \left|\frac{(R^s + j2\pi f_{ex}L^{\ell s})\left[\frac{R^r K}{2\pi T^{e*}} + j2\pi(L^{\ell r}+L^m)\right]}{j2\pi f_{ex}L^m \left[\frac{R^r K}{2\pi T^{e*}} + j2\pi L^{\ell r}\right]} + 1\right| \qquad [3.14]$$

where $\lambda_{ag_{rated}}$ is the rated air-gap flux amplitude and λ_t is the motor terminal equivalent flux, both in V/Hz.

Using the measured parameters of the induction motor, the ratio of terminal volts per Hertz (line-to-neutral) to the desired constant air-gap flux (in V/Hz) is plotted in Figure 3.20 as a function of the desired torque for a family of excitation frequency values. This relationship has been linearized for microprocessor implementation and then adjusted empirically to improve torque/excitation frequency independence, yielding the following simplified expression in its final form

$$\lambda_t^* = 0.36 + A_1 \times T_1 \times f_{s\ell} \qquad [3.15]$$

where $T_1 = 1/f_{ex}$ $\quad f_{ex} < 25$ Hz

$\quad = 1/25$ $\quad f_{ex} \geqslant 25$ Hz

and

$A_1 = 0.9$ $\quad f_{s\ell} > 0$

$A_1 = 0$ $\quad f_{s\ell} < 0$

This expression is plotted in Figure 3.21 in a form which permits easy comparison with the analytical expression derived directly from the equivalent circuit and plotted in Figure 3.20. Such a comparison indicates that the curves are quite similar in the motoring regime ($f_{s\ell} > 0$), however, the implemented terminal V/Hz expression in the regenerative region ($f_{s\ell} < 0$), departs from the calculated curves of Figure 3.20. This notable departure requires an explanation, and leads naturally into a discussion of the rationale for the closed-loop terminal V/Hz control configuration which follows the voltage control algorithm block in Figure 3.18.

Closed-Loop Flux Regulator Rationale

First, attention must be turned to the interaction of the pulse-width modulation algorithm and the inverter power stage. The effective amplitudes of the output voltage waveforms are adjusted by means of a duty cycle control parameter known as the modulation index which introduces "notches" of variable widths into the output voltage waveforms. Additional details on the implemented PWM algorithm are given elsewhere in this final report. For this discussion, the important point is, as a result of the implemented inverter thyristor gating strategy, the output voltage is dependent on load power factor in addition to the modulation index and the battery terminal voltage.

As described in Section 3.3, the thyristor gating strategy selected for implementation required trade-offs between the quality of the output PWM waveform and inverter efficiency. Thus, in each of the three inverter legs, only one of the thrystors is alternately gated on and then commutated during each half-cycle of PWM operation. During the "off" intervals, the inverter depends on current flow through the complementary free-wheeling diode to pull the motor terminal voltage to the opposite bus potential since the complementary thyristor is never triggered. This situation is shown in Figure 3.22a. This scheme was adopted because it results in one-half the number of thyristor commutations required by the conventional triggering scheme, leading to an important reduction in the inverter commutation losses.

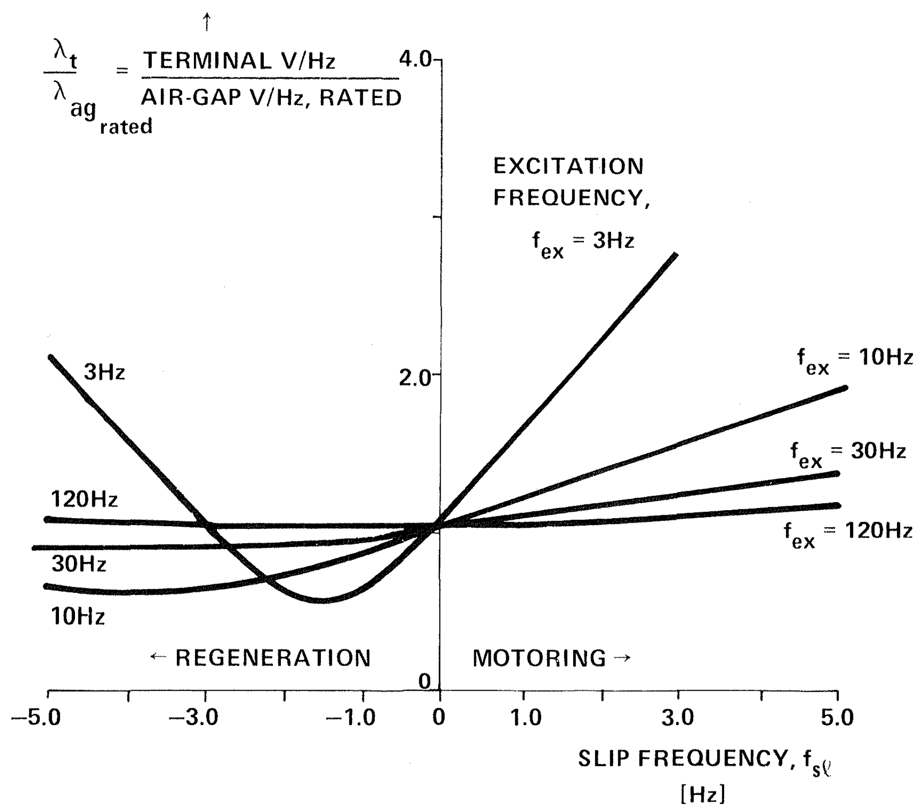

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Figure 3.20 Desired $\lambda_t/\lambda_{ag\ rated}$ Ratio as a Function of Excitation Frequency and Slip Frequency for Constant Flux Operation (calculated using motor equiv. circuit parameters of Figure 3.3)

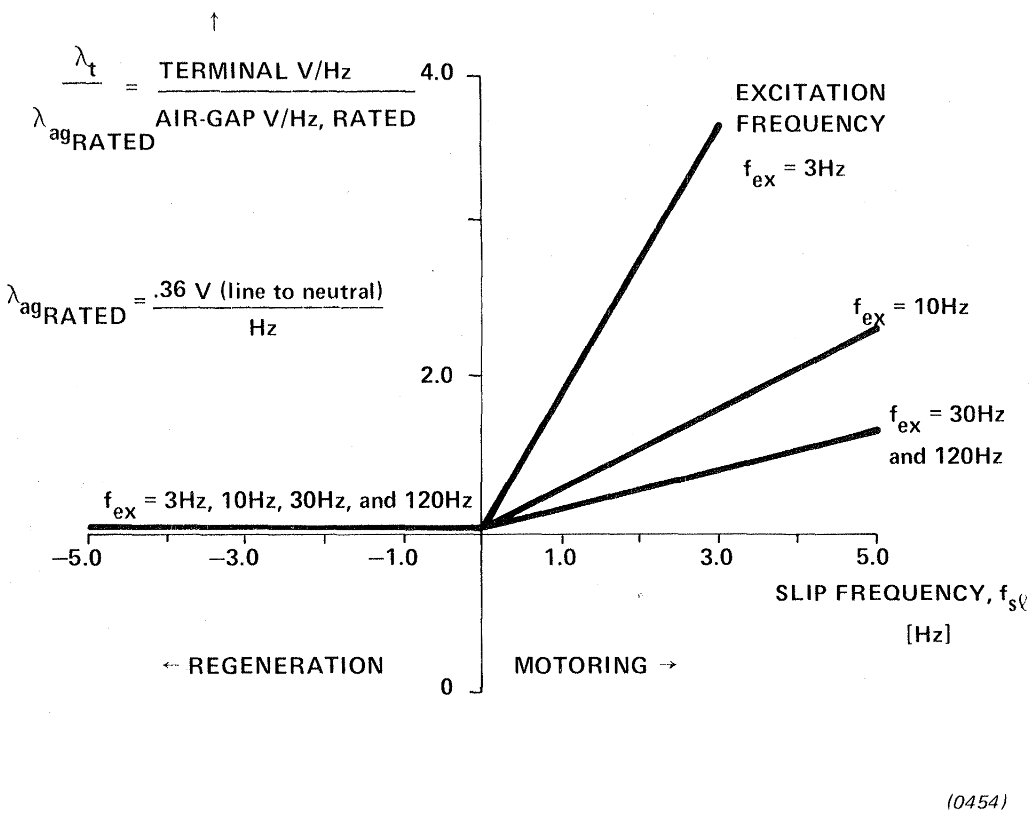


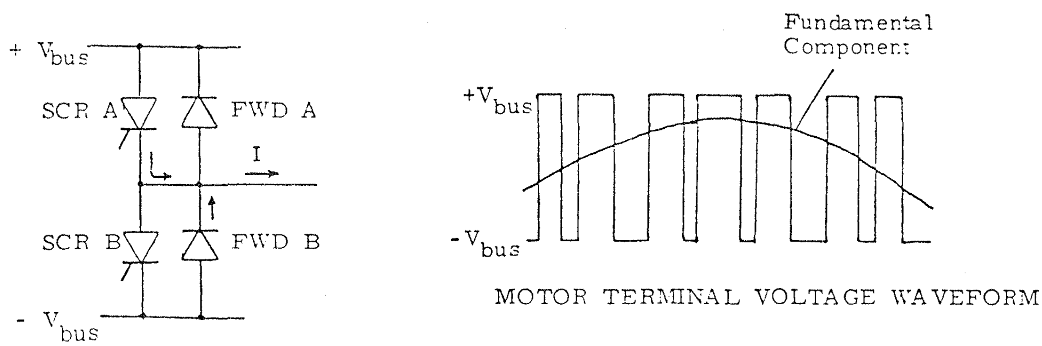
Figure 3.21 Implemented $\lambda_t/\lambda_{ag_{rated}}$ Ratio as a Function of Excitation Frequency and Slip Frequency, Approximating Constant Flux Operation

As long as the load power factor approaches 1.0 (motoring under load) so that each phase voltage and current is in phase, the adopted triggering scheme yields exactly the same results as when all of the thyristor gatings and commutations are performed. However, this is no longer true when the motoring load is decreased and reversed into a braking load so that the power factor exceeds 90° (phase voltage and current progressively more out of phase). During any interval in which the motor phase current is of opposite polarity to the associated fundamental frequency phase voltage (Figure 3.22b), the unavailability of the complementary thyristor for current conduction affects the voltage waveform. Instead, the current must flow through the free-wheeling diodes, forcing the motor terminal voltage to bus potentials opposite from those specified by the desired PWM algorithm. As illustrated in Figure 3.22b, notches disappear from the output voltage waveform, changing the fundamental frequency voltage amplitude.

This notch disappearance phenomenon results in the aforementioned sensitivity of the output voltage amplitude to load power factor. In addition, the output voltage is directly proportional to the propulsion battery voltage, reflecting its present state-of-charge. Clearly, the output voltage is not solely dependent on the PWM modulation index setting. Thus, the decision was made to adopt a closed-loop control scheme which regulates the modulation index in order to keep the motor terminal V/Hz setting as close to the desired value as possible, compensating for the other dependencies. Such regulation scheme is feasible because the output voltage amplitude has a monotonically increasing dependence on the modulation index.

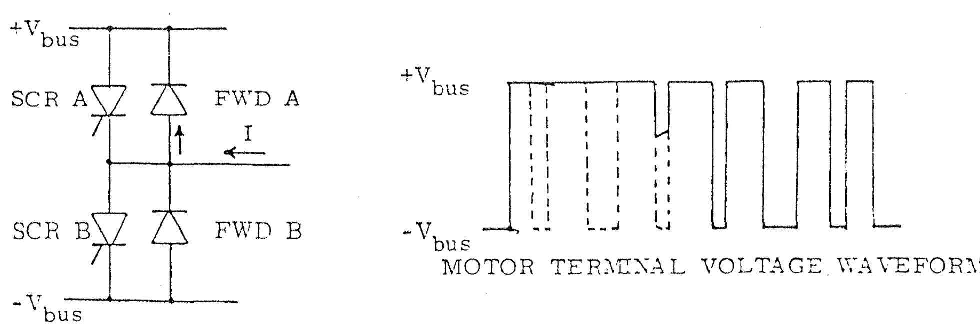
The closed-loop V/Hz regulation scheme works very effectively throughout the motoring regime. However, as increasing regenerative braking torques are called for, the gradual disappearance of output voltage waveform PWM notches makes it more difficult for the modulation index to exert effective control of the motor terminal voltage. Thus, there was no need to develop a sophisticated algorithm for calclating the desired terminal V/Hz in the regenerative region (Figure 3.21, $f_{s\ell} < 0$) since, to a large extent, the motor sets its own operating voltage during regeneration. The resulting nonlinearity in the regenerative torque dependency on slip frequency, which is

A) MOTORING REGIME OPERATION (HIGH POWER FACTOR)



- SINCE MOTOR VOLTAGE AND CURRENT WAVEFORMS ARE IN PHASE, FWD B CONDUCTS PHASE CURRENT WHEN SCR A IS OFF DURING POSITIVE HALF CYCLE

B) REGENERATION REGIME OPERATION (POWER FACTOR ANGLE > 90°)



- DURING HALF CYCLE WHEN SCR A IS TRIGGERED, VOLTAGE WAVEFORM NOTCHES DISAPPEAR SINCE SCR B IS NEVER TRIGGERED TO DIVERT REGENERATIVE CURRENT FROM FWD A

(0455)

Figure 3.22 Basis for Influence of Load on Motor Terminal Voltage During PWM Operation

not particularly severe, is part of the price paid for a substantial reduction in inverter commutation events and, hence, losses during motoring.

It is important to note that Volts per Hertz regulation is only an issue during PWM operation at vehicle speeds less than roughly 48.3Km/h (30mph), (f_{ex} = 140 Hz). At all higher speeds the motor calls for more terminal voltage than the propulsion battery/inverter combination can provide. Thus, the closed-loop regulator saturates with the modulation index at its maximum value, resulting in simple six-step voltage output waveforms throughout the flux weakening speed regime. Six-step excitation is fully compatible with regenerative motor operation, having no counterpart to the notch disappearance phenomenon which occurs during PWM operation at lower speeds. Thus, it was necessary to restrict regenerative operation by means of the slip frequency limit only for excitation frequencies of 40 Hz (1200 rpm) and under.

Flux Regulator Algorithm

At the heart of the terminal V/Hz regulator implementation is the modulation index control block of Figure 3.18 which converts the error signal, ε_V, representing the difference between the desired and measured motor V/Hz,into a modulation index command. This control function is executed by means of a proportional-integral (PI) algorithm implemented in the microcomputer's software. This digital algorithm has been designed to emulate the action of a PI controller in its more familar analog configuration according to the expression

$$m_i = A_p \varepsilon_V + \int_{t_0}^{t} A_I \varepsilon_V d\tau \qquad [3.16]$$

where m_i is the value of modulation index at time t, A_p is the proportional analog controller gain, A_I is the integral controller gain, and ε_V is the motor terminal V/Hz error. In its analog equivalent form, note that the presence of the integral term prevents the control loop from reaching a steady state condition (dm_i/dt = 0) until the error signal is forced to zero (ε_V = 0).

In the frequency domain, the PI controller law can be expressed in its Laplace transform form as

$$M_i(s) = \frac{A_I \, [1 + (A_P/A_I) \, s]}{s} \; \varepsilon_v(s) \qquad [3.17]$$

where $M_i(s)$ and $\varepsilon_v(s)$ represent, respectively, the Laplace transforms of the modulation index and the V/Hz error, and s (= $j\omega$) is the complex frequency.

The adopted digital implementation of the PI controller law is expressed as a difference equation relating the new values of the control variables to their most recent values one control cycle earlier. Since the measured terminal Volts per Hertz is updated once per excitation frequency cycle, the digital controller cycle time is conveniently set equal to the excitation frequency period, $T_{ex} = 1/f_{ex}$. Thus the digital PI controller law can be written as

$$M_{i(new)} = M_{i(old)} + \Delta m_1 \qquad [3.18]$$

where, $\Delta m_1 = [D_{p(new)} \, \varepsilon_{v(new)} - D_{p(old)} \, \varepsilon_{v(old)}] + D_{I(new)} \, \varepsilon_{v(new)}$

where the "new" subscript represents updated values of variables, whereas "old" subscripts represent variable values one cycle time earlier, D_p represents the gain of the digital proportional controller and D_I is the integral controller gain. Note that "new" and "old" subscripts are added to the gain values as well as to the modulation index and error values because these gains need not be constants. Provided that the dynamics of the controlled process are slow compared to the digital controller update frequency, the analog and digital controller update frequency, the analog and digital PI controllers will perform identically if A_p equals D_p and A_I equals the product $D_I f_{ex}$, where f_{ex} is the digital controller update frequency.

Based on a combination of analytical and empirical results, it was found necessary to adjust D_p and D_I, the digital proportional and integral gains, as a function of the excitation frequency. The implemented functions for D_p and D_I are plotted in Figure 3.23 over the full PWM frequency range, with the D_p/D_I ratio held at a constant value of 2.0 over this full range. Heurisically, it makes sense that, over much of this range, the gains increase with frequency, since the terminal V/Hz becomes less sensitive to modulation index as the excitation frequency increases. At higher frequencies approaching the upper limit of PWM operation, the gains are gradually decreased in order to ease the transition between PWM and six-step excitation operation. A bit of the dynamic response speed is sacrificed as a result of decreasing these gains, but the resulting transition smoothness justifies the compromise.

One aspect of the digital PI controller operation which is not reflected in the analog version is digital quantitization error. For example, a finite deadband exists around zero error in the digital controller for which the integral controller does not respond at all because of the quantitization effect. The width of this deadband varies as $1/D_I$ V/Hz, preventing a hunting instability from occurring near zero error. This feature works very well except at very low frequencies where the deadband gets so wide that undesirable steady-state V/Hz errors occur, allowing motor iron saturation and torque inaccuracies. As a result, for excitation frequencies below 14 Hz a second integral controller gain term is introduced as follows

$$m_{i(new)} = m_{i(old)} + \Delta m_1 + \Delta m_2 \qquad f_{ex} < 14 \text{ Hz} \qquad [3.19]$$

$$\Delta m_2 = D_k \, \varepsilon_v \qquad [3.20]$$

where $m_{i(new)}$, $m_{i(old)}$, and Δm_1 have been defined previously.

By implementing this auxiliary integral controller so that it has no deadband, the problem of steady-state V/Hz errors during low frequency operation is eliminated. The gain D_k in this second integral controller is purposely set at a constant value of 2.0 so that the system dynamics are dominated by the Δm_1 proportional-integral gain terms. In this manner acceptable regulator performance is achieved at all operating frequencies throughout the PWM excitation regime.

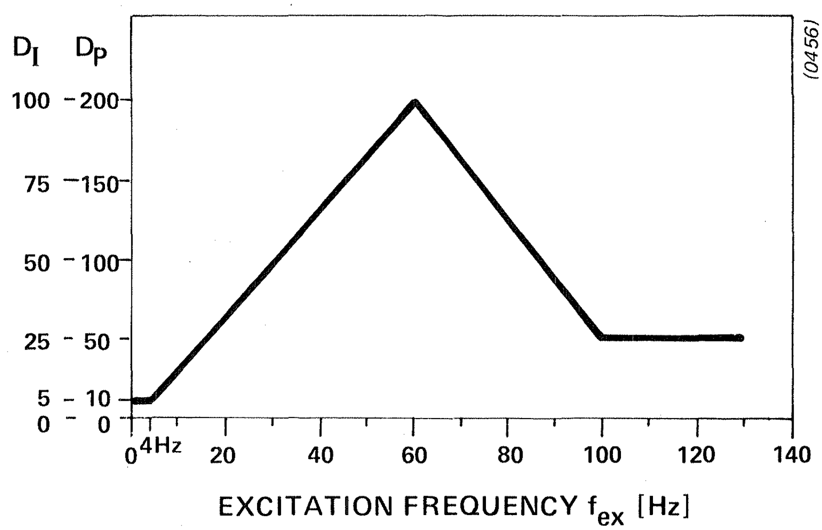


Figure 3.23 Gain Factors D_p and D_I as a Function of Excitation Frequency

Motor Terminal V/Hz Transducer

The final topic which requires discussion in this section is the structure and operation of the motor terminal Volts per Hertz transducer. More specifically, the motor variable of interest is the ratio of rms fundamental frequency terminal voltage to excitation frequency, or $V_1^{\ell n}/f_{ex}$. Since the motor terminal voltages have nonsinusoidal PWM waveforms, extracting the V/Hz term of interest is not a trivial task. Although rms conversion integrated circuits do exist which could perform the task, they require a tunable filter to provide accurate readings with acceptable dynamic response over a wide excitation frequency operating range. After investigation, this approach was rejected.

Instead, a special V/Hz transducer circuit was designed and built which performs an on-line Fourier transform of the motor terminal voltage according to the expression

$$\frac{V_1^{\ell n}}{f_{ex}} = \frac{1}{\sqrt{2}} \int_0^{1/f_{ex}} V^S\,(t)\ \sin\,(2\pi f_{ex} t)\ dt \qquad [3.19]$$

where $V^S(t)$ is the periodic line-to-neutral motor terminal voltage waveform varying at frequency $f_{ex} = 1/T_{ex}$. This expression yields the entire fundamental component of $V^S(t)$ as long as the fundamental component of $V^S(t)$ and $\sin(2\pi f_{ex}t)$ are exactly in phase. Fortunately, the fundamental component of the PWM line-to-neutral motor voltage waveforms are synchronized with reference sine waves generated inside the PWM modulator hardware. Thus, by multiplying an attenuated reproduction of one of the three motor line-to-neutral voltage waveforms with the appropriate reference sine wave, and then integrating this product, a new reading of the desired quantity $V_1^{\ell n}/f_{ex}$ is available at the end of each excitation period.

A block diagram of the V/Hz transducer is provided in Figure 3.24. A fast differential amplifier configuration is used to produce the attenuated motor line-to-neutral voltage signal. Be feeding this analog signal and the reference sine wave digital signals as inputs to a multiplying D/A converter, the required product is formed in real time. An operational amplifier

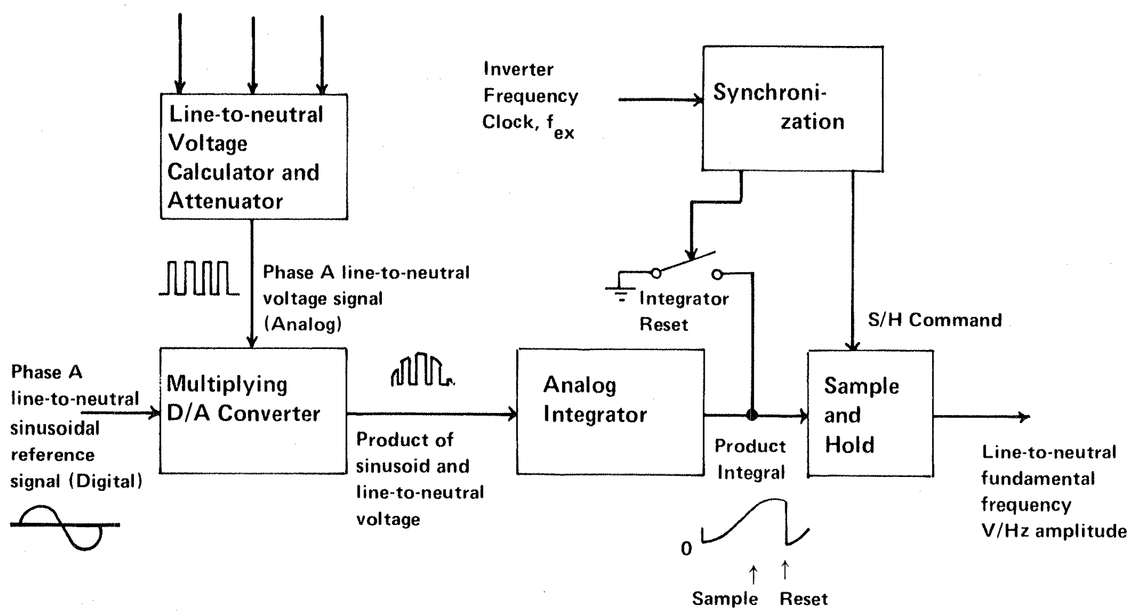


Figure 3.24 Block Diagram of the Fundamental Frequency Volts-per-Hertz Transducer

integrator circuit then integrates this product every cycle, being reset at the end of each cycle by an FET switch. Immediately preceding this reset pulse the integrated product value (an analog signal) is sampled by an IC sample-and-hold circuit; this level, representing the most recent reading of motor Volts per Hertz, is held until the next reading becomes available at the end of the cycle.

The gain of the V/Hz transducer varys little throughout the excitation frequency and loading operating ranges during motoring operation. On the other hand, gain falls off somewhat during regeneration due to a phase shift which develops between the reference sine wave and the fundamental component of the motor line-to-neutral voltage. This decay in gain, caused by the PWM notch disappearance phenomenon described earlier in this section, is compensated in the microcomputer software, assuring acceptable performance under all operating conditions.

3.3 Power Inverter Design

The power inverter is the physical implementation of the six switch array illustrated in Figure 3.10. Physically, each switch in the inverter is a thyristor, a semiconductor device which latches into conduction when a voltage is applied to its control or gate terminal. The device regains its voltage blocking capability when an external negative voltage is applied to the thyristor's anode-cathode terminals for a minimum time period determined by the device characteristics. If this reverse bias time is short, less than 15μS, the device is considered an inverter grade SCR or thyristor. Thyristors were chosen to implement the inverter switch array because they are readily available at low cost with suitable power handling capabilities.

Although SCR's would appear to offer a superior implementation advantage when compared to transistors, the external circuitry required to turn-off the SCR, or reverse bias the anode-cathode terminals, complicates the SCR inverter circuit implementation. This additional circuitry is generally termed the main SCR commutation circuitry. It was a goal in this program to select an inverter circuit topology which required a minimum of additional circuit components to accomplish the commutation function. The topology which was selected to meet this goal is generally termed a bus-commutated inverter and requires a minimum of commutation components.

Figure 3.25 illustrates the schematic diagram of the inverter power stage. The components shown may be grouped into two sub-circuits, one consisting of the main conduction devices, and the second the commutation circuitry. Those components to the right of the dotted line in Figure 3.25 carry the three motor phase currents, and those to the left of the line are used to commutate the main SCR's. A description of the operation of the bus-commutated inverter is useful to understand the advantages and limitations of this inverter topology.

Commutation Sequence Description

To set the stage for a commutation cycle, initial conditions of the inverter must be established. Figure 3.26 illustrates typical initial conditions. As shown in Figure 3.26, the motor phase terminals A and B are connected to the plus battery terminal via SCR's 1 and 3 and motor phase terminal C is connected to the minus battery terminal via SCR 2. The inverter is to be reconfigured such that motor terminal A is connected to the minus battery terminal. The polarities of the commutation capacitors C_1 and C_2 are as shown in Figure 3.26.

SCR7, which is blocking V_{C1}, is gated into conduction to initiate the commutation of upper bus thyristors. This places the top commutation capacitor voltage V_{C1} across the transformer windings T1A and T1B. If the voltage across T1A is greater than the battery voltage, then all three thyristors in the upper bus (SCR1,3,5) will be reverse biased. This can be shown by tracing a path in the circuit of Figure 3.26 from anode to cathode of each device. This path starts at the common anode connection, goes through T1A, the battery, and one of the lower bus diodes (D2, 4, or 6) to the cathode of either SCR1, 3 or 5. The only significant voltage drops encountered are those across T1A and the battery. This event allows all of the upper bus thyristors to regain their blocking state.

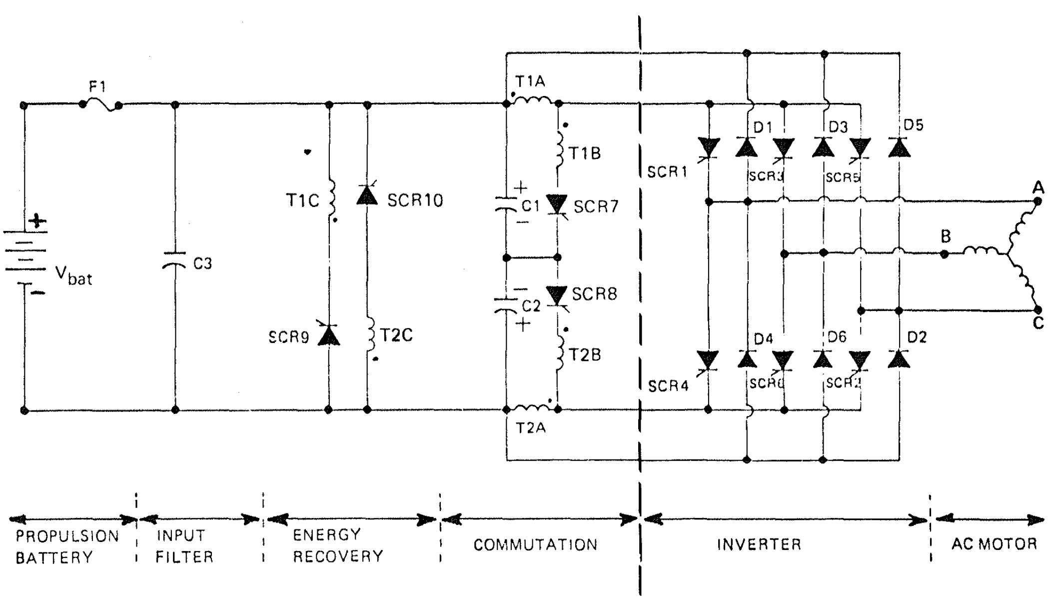


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Figure 3.25 EV Propulsion System Power Stage Configuration

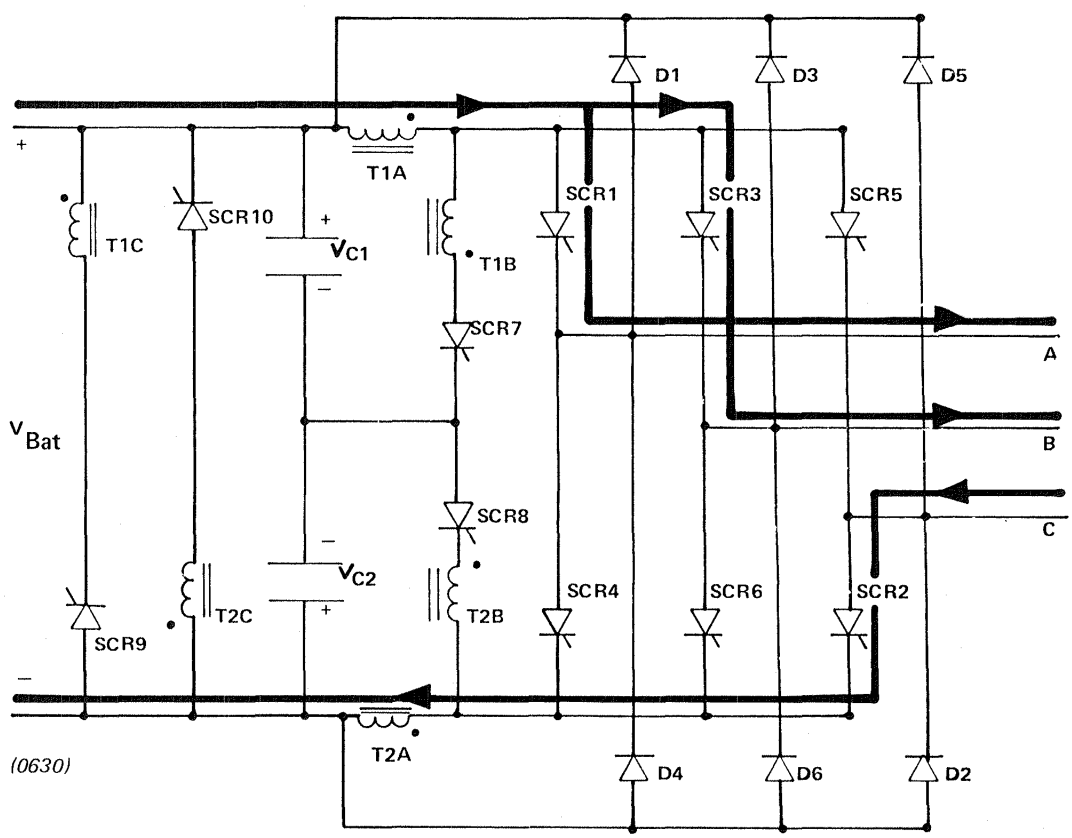


Figure 3.26 Initial Power Circuit Current Paths

Capacitor C1 will now discharge through the two paths shown in Figure 3.27. The time constant of this discharge is determined by the inductance and capacitance of the commutation circuit components. For a successful commutation, the main devices must be reverse biased for some minimum turn-off time, $T_{q_{min}}$, a characteristic of the devices. For the devices used in the Gould inverter, $T_{q_{min}} \leqslant 10\mu sec$. Thus, the voltage across T1A must remain greater than battery voltage for this time period.

During the commutation interval, the motor phase currents are carried by the freewheeling diodes D4-D6. In Figure 3.27, the current paths shown are those consistent with positive $I_A{}^S$ and $I_B{}^S$ phase currents immediately prior to the commutation.

Note that as shown in Figure 3.27, during the commutation interval, all three motor phases are connected to the negative battery terminal. Thus, during the commutation interval, the voltage applied to the motor is zero. Figure 3.28 shows the effect of this "notch" or zero voltage interval on a typical line to line motor voltage waveform.

After successfully turning off all conducting upper bus thyristors, the upper commutation capacitor C1 continues to discharge. At some point, after its voltage has reversed polarity, the transformed potential appearing across T1C (coupled to T1A and T1B) becomes greater than the battery voltage, forward biasing SCR9. When the capacitor C1 reaches a predefined negative voltage, SCR9 is gated into conduction. Since the transformed capacitor voltage was greater than the battery voltage now applied across T1C, the actual capacitor voltage, V_{C1} is greater than that across T1A, B. Thus, SCR7 is reverse biased, and turns off. For the rest of the interval, the commutation capacitor voltage remains constant. The energy that was contained in the transformer windings T1A and T1B is transferred to T1C, and is returned to the battery via the current path shown in Figure 3.29.

The clamp thyristor can be fired any time after the transformed potential across T1C is greater than the battery voltage. This allows limited control over the final commutation capacitor voltage, and, thus, over the

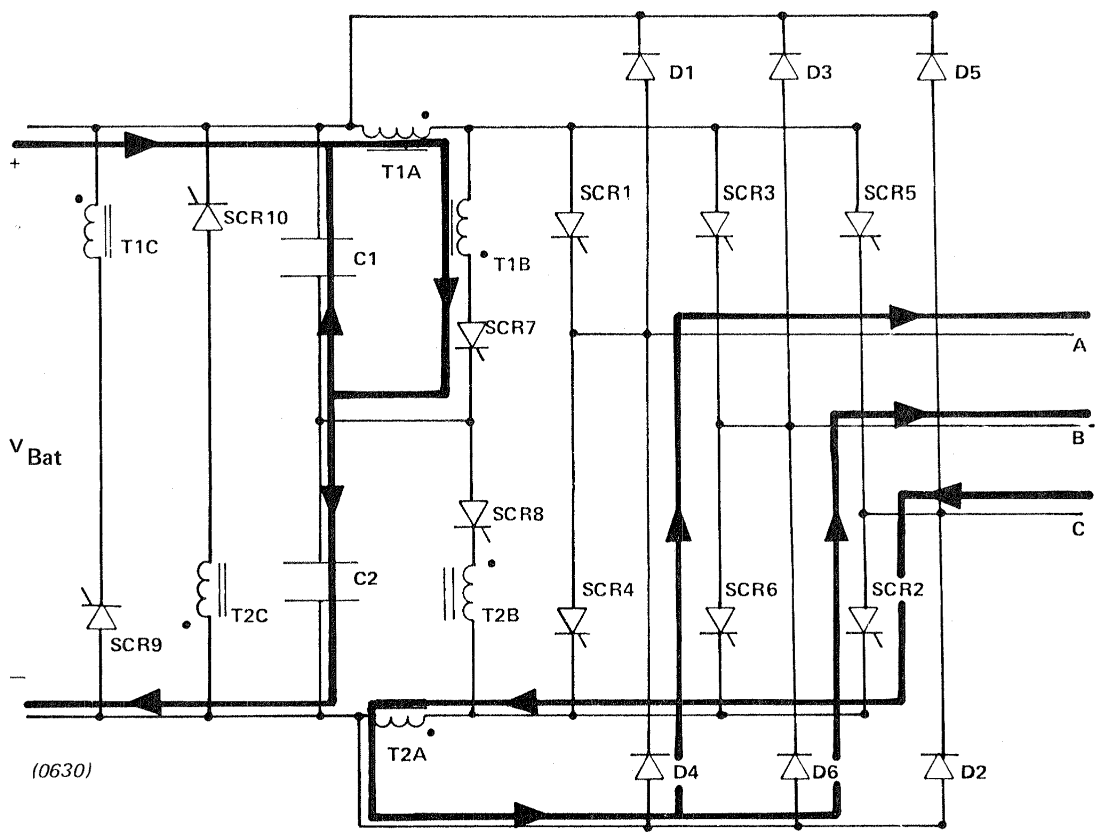
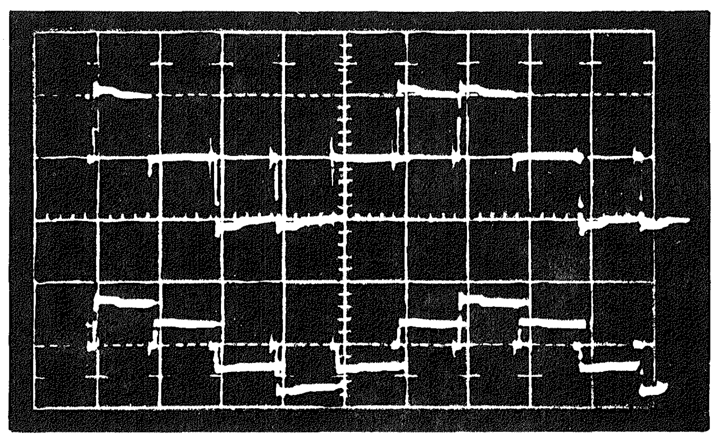


Figure 3.27 Currents Following the Initiation of a Commutation Cycle

$V^{\ell\ell}$

V^{s}



y = 100V/cm

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x = 1ms/cm

SHAFT SPEED = 538.05 rad/s (5138rpm)
POWER = 15kW

Figure 3.28 Inverter Six-Step Waveform.
The Instants of Zero Voltage Correspond to Commutation Intervals

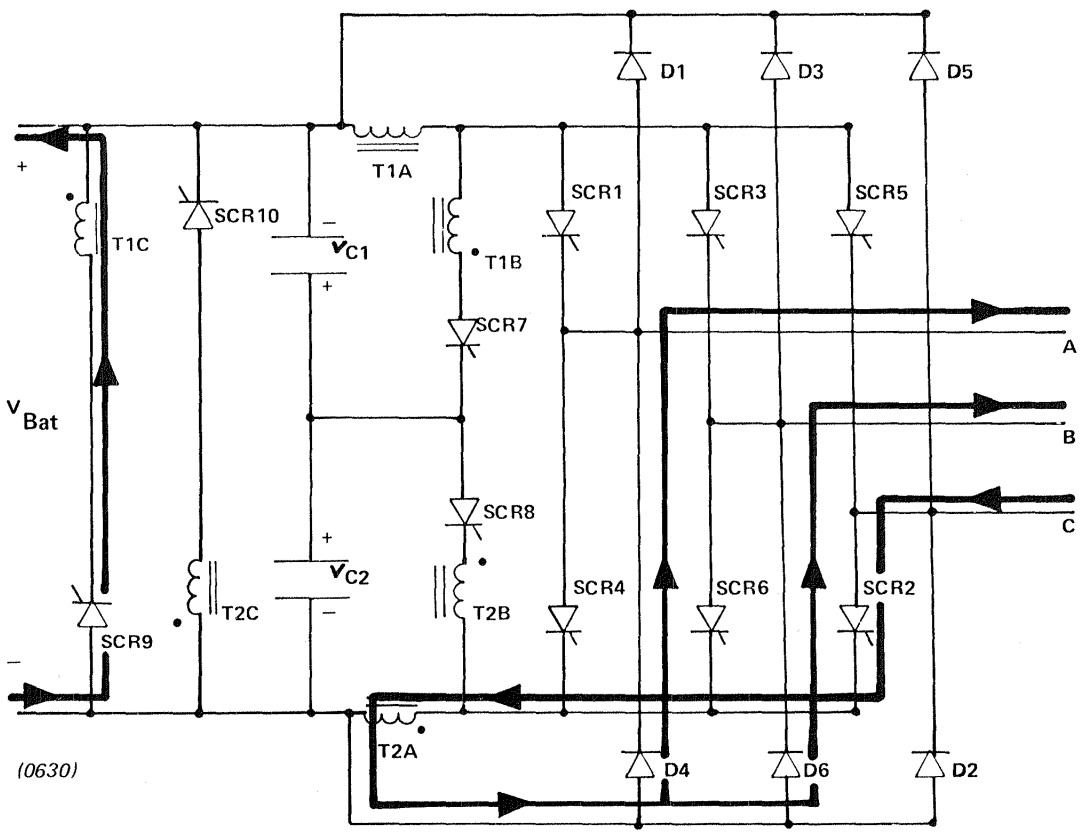


Figure 3.29 Energy Recovery Current Paths

initial voltages on C1 and C2 for the next commutation. The minimum attainable commutation voltage is determined by transformer parameters and the battery potential, while the maximum is limited only by circuit components.

After the clamp thyristor SCR9 is fired, the appropriate main devices may be enabled to reconnect the motor phases to the desired battery terminals. In the case examined here, SCR2 has remained in conduction, so only SCR3 and SCR4 need be triggered, completing the transfer of motor terminal A to the negative battery terminal illustrated in Figure 3.30.

If the upper bus main thyristors are enabled before the current in T1C goes to zero, the remaining energy in T1C will be transferred, through T1A, to the motor. This is usually the case, as it allows a shorter commutation "notch" in the motor voltage waveform. However, any transferred energy in excess of that necessary to attain the required dc bus current through T1A will be dissipated in the upper bus main semiconductors. The path of the excess current, for the case examined here, is shown in Figure 3.31. Thus, a compromise must be reached between the desire for a short voltage waveform notch, and the need to return a sufficient amount of energy to the battery before the main devices are re-enabled. After the main devices have been enabled, the commutation circuit is prepared exclusively for a lower bus commutation due to the voltage polarities on C1, C2.

Figure 3.32 shows an oscillograph of the major controller current waveforms during an upper bus commutation. The uppermost waveform is a logic signal. The other three waveforms in Figure 3.32 (from top to bottom) correspond to the currents through SCR7, SCR9, and the DC bus, respectively. The flow of energy through the controller can easily be traced with this diagram. In Figure 3.32, initially a current of about 100 Amps flows through the dc bus to the motor thru SCR1 and SCR3. Once the commutation begins, this current is diverted to the commutation circuit (part of the initial current through SCR7 is due to discharge of the snubber connected across it). The SCR7 current waveform is recognizably sinusoidal. When the energy recovery phase begins, this current is transferred to SCR9. The transfer takes several microseconds, due to leakage inductance in the T1A, T1B, and T1C windings.

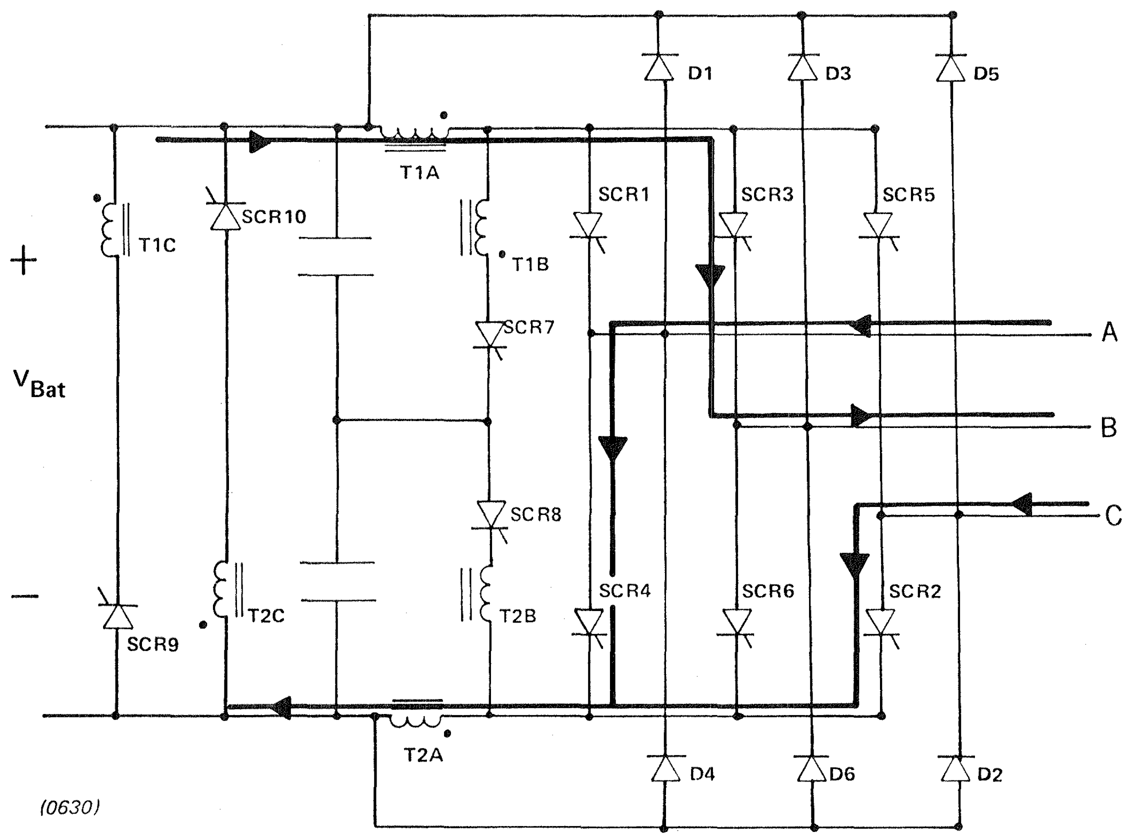


Figure 3.30 Reconnected Motor Terminals After Commutation

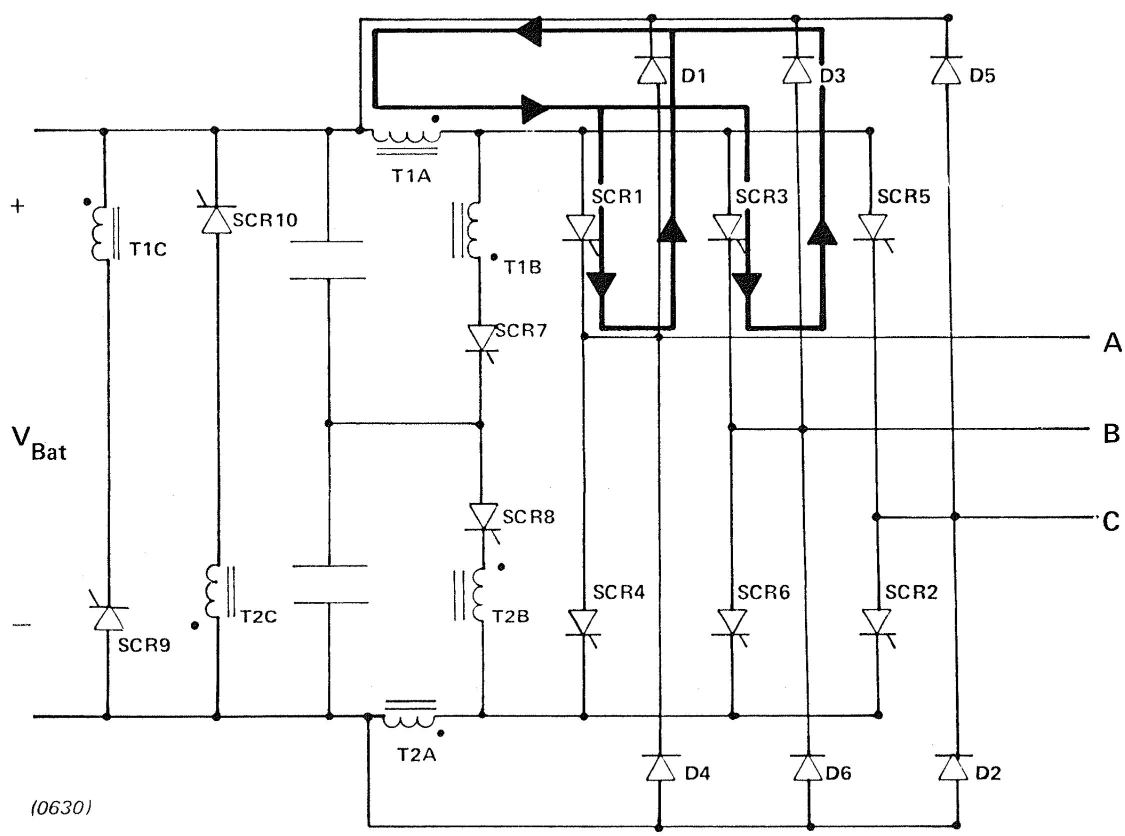
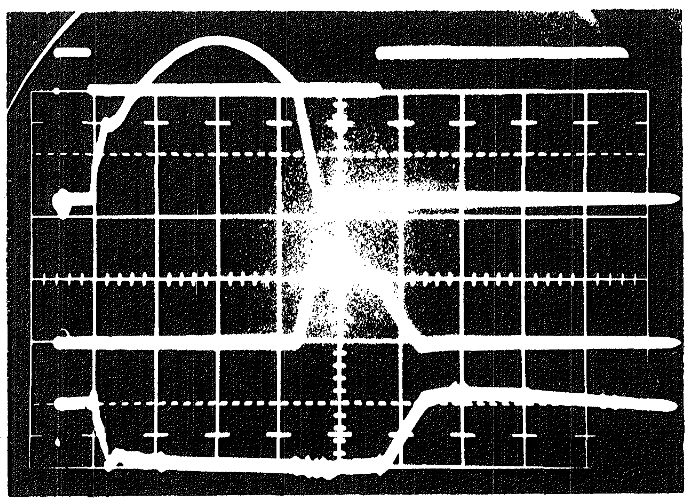


Figure 3.31 Current Paths for Excess Commutation Energy Remaining After Main Devices are Enabled

100A/cm



$I_{SCR\ 7}$

$I_{SCR\ 9}$

$I_{SCR\ 1}$

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20 μs/cm

Figure 3.32 Commutation Circuit Current Waveforms

Finally, when the upper bus main thyristors are re-enabled, the current in T1C is transferred back to the dc bus. The total commutation event duration is about 100μsec.

The description of a typical commutation sequence emphasises several important features about the Gould inverter. First, due to the circuit topology, whenever it is desired to turn off a thyristor in either the upper bus (SCR's 1,3 or 5) or the lower bus (SCR's 2,4, or 6), all three thyristors connected to that bus must be commutated. Since the amount of stored energy required to turn off a thyristor with an LC oscillating circuit depends on the commutated current, turning off all of the conducting thyristors in a bus requires more stored energy than turning off one alone.

Secondly, during the commutation interval (about 100μsec), the three motor phases are connected to the same battery terminal. When the excitation frequency f_{ex} is very high (260Hz) these intervals of zero applied voltage, which appear six times per cycle, have a significant effect on the maximum fundamental voltage which is applied to the motor.

A third restriction imposed by the bus-commutation circuit topology is the necessity of alternate top and bottom bus commutations to store energy in the commutation capacitors. This is not an important restriction when the inverter is delivering its maximum voltage since commutations are demanded alternately for top and bottom bus devices, but must be considered in designing PWM control logic.

Finally, the energy-recovery branch of the commutation circuit, including SCR's 9 and 10, as well as one winding on each transformer, allows control of the amount of energy used in turning off the main devices. Under light-load conditions, the circuit reduces its commutation capability and, thus, its losses. This allows the commutation circuit design to be optimized for efficient operation for cruising conditions, while the transient high loads encountered during startup and acceleration are handled by increasing the commutation voltage temporarily.

Inverter Power Stage Design Requirements

In this section, equations are presented which describe the constraints placed on the main and commutation circuit components by the operating requirements of the controller. These controller requirements are stated in terms of a battery current and voltage, V_{bat} and I_{bat}, respectively, and a controller three-phase output power, P. In addition, it is assumed that the main thyristors have a given minimum required turn-off time, $^{T}q_{min}$, and that the maximum commutation frequency, f_{com} (max) is known.

The commutation circuit design is addressed first. A mathematical analysis of the commutation sequence is used to determine component values for the resonant circuit which result in minimum stored energy while simultaneously meeting the reverse bias requirements for main thyristor turn-off. The actual component values are then used to derive current and voltage rating requirements for the thyristors and capacitors in the commutation circuit. It is shown that the topology of the Gould bus-commutated inverter, with its three-winding transformer, allows the designer a degree of freedom in adjusting either the peak current or voltage stress of the commutation circuit components.

The main device voltage and current ratings are functions of the peak commutation voltage and motor-controller performance requirements. These semiconductor stresses are shown to be within the limits of the devices selected. The gate drive requirements of the thyristors are specified. An analysis of the gate drive circuit employed shows that drive requirements are satisfied. Finally, the normal operating modes of the inverter are examined to determine those which necessitate semiconductor voltage protectors or snubbers.

Commutation Circuit Design

The function of the commutation circuit is to provide a reverse voltage across either the upper or lower bus of main thyristors for the specified turn-off time, $^{T}q_{min}$. The losses suffered by the commutation circuit are empirically found to be proportional to the peak stored energy of the transformer, Up, defined as (1/2) $L^{A+B} I_p^2$ where L^{A+B} is the total inductance of the transformer A and B windings and I_p is the peak commutation circuit current. Thus, in order to minimize commutation losses, it is desirable to choose circuit component values to allow successful turn-off of the main devices with the minimum possible peak stored energy.

A detailed analysis of this problem is presented in Appendix II. Only the results are summarized here. Given a required battery current, I_{bat}, battery voltage, V_{bat}, and device turn-off time, T_q, the minimum peak stored inductor energy which will allow commutation of the main devices is Up_{min}.

$$Up_{min} = \underline{Up}_{min} \cdot U_{diverted} \quad \text{[joule]} \qquad [3.22]$$

where

$$U_{diverted} \equiv V_{bat}\, I_{bat}\, T_q \qquad [3.23]$$

and

$$\underline{Up}_{min} \cong 3.80$$

$U_{diverted}$ is defined as the diverted energy of the controller, and $\underline{Up}_{min}$ is a mathematically determined constant. Its derivation is included in Appendix II. Thus, within the constraints of the given circuit topology, it is impossible to commutate the main devices without having a peak stored inductor energy equal to about four times the diverted energy of the controller. In order to achieve successful commutation with this peak energy, the component values of the two coupled inductors and capacitor of each bus commutation circuit must satisfy the constraints:

$$L^A = \frac{V_{bat}}{I_{bat}} \cdot \frac{T_{q_{min}}}{K_{min}} \qquad [3.24]$$

$$C^T = \frac{I_{bat}}{V_{bat}} \cdot \frac{T_{q_{min}}}{(1+x)^2\, K_{min}} \qquad [3.25]$$

where L^A, the inductance of the "A" winding of the transformer alone, x, the turns ratio of the "B" to "A" windings, and C^T, the total commutation capacitance, completely determine the three component values. K_{min} is another constant ($K_{min} = 0.5559$).

The commutation voltage necessary is

$$V_c = 1/Y_{min} \cdot (1+x)V_{bat} \qquad [3.26]$$

where $Y_{min} \cong 0.556$

Y_{min} expresses a ratio between the battery voltage and the voltage across C1.

The peak current in the commutation circuit, I_p, is

$$I_p = (2K_{min} \underline{U}_{p_{min}})^{1/2} \quad I_{bat}/(1+x) \qquad [3.27]$$

Thus, with no transformer "B" winding (i.e., x=0), and optimum component values for the particular motor load and turn-off time, the commutation voltage should be about twice the battery voltage, and the peak current in the commutation thyristor is about twice the commutated motor line current. As the number of turns in the "B" winding rises, the commutation voltage goes up and the peak current goes down, according to eqs. 3.26 and 3.27.

It should be noted that the minimum energy requirement places only two constraints on the three parameters, L^A, x, and C^T. The parameter, x, can be considered a free variable, whose value is determined by the desired peak voltage or current rating of the commutation circuit. Either one, V_c or I_p can be lowered, at the expense of raising the other, by choosing appropriate values of x. Also, note that x can actually be made negative, if desired, by winding the "B" turns in a direction opposite to that of the "A" turns (as long as $-1 < x$).

The nominal battery voltage and current used in this calculation for the Gould controller were V_{bat}=120 v, I_{bat}=600 A. With a minimum reverse-bias time of $T_{q_{min}}$=10μsec, L^A = 3.6μH, and if x is chosen as 0.67, peak voltages and currents compatible with available semiconductors are obtained.

$V_c = 360$ v

$I_p = 750$ A

then $C^T = 33\mu F$

The actual component values used were

$L^A = 8\mu H$

$x = 0.67$

$C^T = 60\mu F$

These values give an $L^{A+B}C^T$ time constant of about 36 μsec, as opposed to 18 μsec for the "ideal" components. This larger time constant is essentially an extra margin of safety during commutation. In the actual implementation, the commutation voltage varies between 360 and 440 volts. The peak commutation current is about 800 Amps.

The maximum commutation frequency $f_{com}(max)$, encountered during motoring is 2400 repetitions per second, which occurs at vehicle speeds of ∿88.5km/h. In regeneration, this rate can go as high as 3400 Hz. If the current in the commutation thyristor is assumed to consist of Fm half-sinusoids per second, each of duration Tcom and peak current I_p, the RMS thyristor current in SCR7 is

$$I_{RMS}^{SCR7} = \frac{1}{\sqrt{2}}(T_{com}\ F_m)^{1/2}\ I_p \qquad [3.28]$$

with

$I_p = 800$ A

$T_{com} = 80\mu S$

$F_m = 1200$ Hz

$I_{RMS}^{SCR7} = 175A$

Actually, the commutation thyristor current waveform is not a perfect halfsinusoid, being "chopped off" at both the beginning and end. Thus, the 80μsec pulse duration is used, rather than $\pi\sqrt{L_{A+B}C_T} = 108\ \mu$ sec.

The peak forward voltage across the commutation thyristor is nominally the commutation voltage, although some allowance must be made for over-ring. Thus, the commutation thyristor forward breakdown voltage must be greater than 440 volts by a sufficient margin of safety. The nominal reverse breakdown voltage requirement is somewhat smaller. The reverse recovery spike encountered when the thyristor turns off (see snubber analysis in this section) results in a 350 volt maximum reverse voltage. Since most thyristors have nearly equal forward and reverse voltage blocking capability, however, this is of little consequence.

To meet these criteria, a GEC184 thyristor rated at 600V and 250 A_{RMS} was selected for SCR7 and SCR8.

From the C184 specifications, the maximum allowable peak on-state current, given a pulse width of 80 sec, repetition rate of 1.2 kHz, and a case temperature of 90 C, is about 830 Amps. During regeneration, when the commutation rate can go as high as 1700 repetitions per device per second, the device rated steady-state peak current of about 660 Amps at 90°C is below that required. Thus, heavy regenerative braking requires use of the transient thermal capability of the devices and associated heatsinks, and cannot continue indefinitely.

The clamping thyristor (SCR9 and SCR10 in Figure 3.25) must be able to withstand substantial reverse voltages. If N_a, N_b, and N_c are the number of turns in the T1A, T1B, and T1C windings of the commutation transformers, then the necessary clamp thyristor reverse voltage capability is

$$V_R^{SCR9} = V_c \left[\frac{N_c}{N_a + N_b}\right] + V_{bat} \qquad [3.29]$$

The forward blocking requirement is less, determined by the following equation:

$$V_F^{SCR9} = V_C \frac{N_c}{N_a+N_b} - V_{bat} \left[\frac{N_a + N_b + N_c}{N_a + N_b} \right] \quad [3.30]$$

substituting $N_a = 3$, $N_b = 2$, $N_c = 5$, the number of turns on each commutation transformer in this equation yields

$$V_R^{SCR9} = 630V.$$

The actual clamp thyristor reverse recovery voltage of 170 volts is much smaller than this due to leakage inductance of T1.

The calculation of RMS clamp current is more complex. Essentially, the energy introduced into the commutation circuit from (a) the motor current, through T1A, and (b) the battery, must be returned to the battery via T1C as pictured in Figure 3.29. The peak current I_p^{SCR9} is

$$I_p^{SCR9} = \left[\frac{L^A}{L^C} I_{bat}^2 + \frac{C^T}{L^C} V_{bat} (2V_C - V_{bat}) \right]^{1/2} \quad [3.31]$$

This is determined by the constraint that the energy initially contained in T1C be equal to the excess commutation energy. The duration, T_{clamp}, during which current flows in SCR9 can be written as

$$T_{clamp} = \frac{L^C I_p^{SCR9}}{V_{bat}} \quad [3.32]$$

if it were not for the fact that the main devices are enabled before the energy-recovery phase is completed. The actual length of the interval, T_{clamp} is the difference between the (pre-determined) main blanking time and the commutation time before the clamps are fired.

$$T_{clamp} = T_{blank} - T_{com} \qquad [3.33]$$

For the present controller,

$$T_{blank} = 100\mu s$$

$$T_{com} = 80\mu s$$

Given the clamp current waveform shown in Figure 3.32, the RMS current is

$$I_{RMS}^{SCR9} = 87A$$

To fill the clamp device requirements, GE C164N thrysistors were selected with ratings of 800 V and 110 A_{RMS}.

The C164 data sheets give a peak allowable on-state current of 840 Amps for 20 μsec pulses at a 1.2 kHz rate. This corresponds to a 92 Amp RMS rating for sinusoidal pulses. Although the predicted RMS current is not much lower than this, it is a very conservative estimate, neglecting the effects of losses on the necessary initial clamp current.

Each commutation capacitor is subjected to current pulses whose magnitude is half that of the commutation thyristor pulses. However, both capacitors receive a pulse for every commutation. Thus, the RMS capacitor current is $1/\sqrt{2}$ times that of the commutation thyristors.

$$I_{RMS}^{C1} = 124A$$

The commutation capacitors (C1,C2) used are Sprague paper-polypropylene commutating capacitors. Each of the two capacitors actually consists of two 15 uF cans, having a terminal current rating of 50 Amps RMS current apiece. Thus, the 125 Amp RMS current encountered at the maximum motoring commutation frequency (62.5 Amps per can) is beyond their steady-state rating and again requires use of the transient capability of the controller.

MAIN THYRISTOR AND DIODE SELECTION

The primary controller specification which influences the main device current rating is the peak power requirement (35 HP at 30 mph). This constraint, combined with the battery voltage limit, determines the minimum RMS current rating of the devices. The voltage ratings are affected by both battery voltage and commutation voltage. If motor voltage and current waveforms are assumed sinusoidal, then the motor shaft power, P^e, is given by:

$$P^e = \sqrt{3}\ I^s\ V_1^{\ell\ell} \cos(\Theta)\ \eta_m \qquad [3.34]$$

where I^s is the fundamental RMS motor phase current, $V_1^{\ell\ell}$ is the fundamental line-to-line RMS motor voltage, cos (Θ) is the power factor, and η_m is the motor efficiency. In six-step operation, the fundamental RMS line-to-line voltage is related to the battery voltage

$$V_1^{\ell\ell} = \frac{\sqrt{6}\ V_{bat}}{\pi} \qquad [3.35]$$

Thus, with the selected battery voltage, shaft power, motor power factor, and efficiency, the RMS phase current requirement is

$$I^S = \frac{\pi}{3\sqrt{2}} \left[\frac{P^e}{V_{bat} \cos\Theta\ \eta_m} \right] \qquad [3.36]$$

With a battery voltage (under load) of 100v, shaft power of 26.1 kW, power factor and efficiency both equal to 0.8,

$$I^S = 302\ \text{A}$$

Since every motor phase is fed by two thyristors, each device must have a current rating $1/\sqrt{2}$ times the per phase requirement.

$$I_{RMS}^{SCR1} = 214\ \text{A}$$

As the controller must be capable of operation with regenerative currents that are as large as those encountered during motoring, the RMS current requirements of the main diodes D1-D6 are virtually the same as those of the main thyristors.

It should be noted that while, theoretically, the same phase currents are sufficient to obtain the peak torque at low frequencies, the RMS device currents are greater, due to the increased harmonic content of the waveform. At the same time, the RMS current rating of the main devices is slightly lower in this regime, due to the high thyristor switching frequency required to limit these harmonics.

The forward voltage blocking requirement of the main thyristors is set by the maximum forward voltage at the end of the commutation interval. Since the voltage across the corresponding capacitor is then $(V_c - V_{bat})$, the forward blocking voltage must be at least $V_F^{SCR1} = 340$ V.

The GE C184 thyristors are available with breakdown voltage ratings from 100 to 800 volts. It is seen from the previous analysis that 600 volt devices are sufficient. These have been selected for use as the main semiconductor devices. GE A198M diodes with ratings of 600V and 250A were employed as the free-wheeling diodes.

GATING REQUIREMENTS

The requirements for safe fast turn-on of a thyristor may be stated in terms of a minimum gate charge and limiting gate current. In the case of the GE C184 thyristor, it is recommended that 3 μCoul be injected into the gate over a period of not less than 3 μsec and not greater than 6 μsec in order to insure turn-on into a high di/dt load. In addition, it is suggested that the gate-cathode voltage spike which results from the fast turn-on not be allowed to reverse the gate current. For turn-on into low di/dt phase currents, a longer pulse of current, of at least the dc gate trigger level, i_{gt}, is recommended. This is necessary to allow the thyristor current to attain the latching value. For the C184, i_{gtm}=300 ma (A typical value for i_{gt} is 150 ma).

The gate drive circuit shown in Figure 3.33 is designed to deliver a large pulse of current to the thyristor for several μsec through an isolation transformer, then to supply a constant low current for the rest of the 10 μsec turn-on interval. In most cases, the thyristor turns on within 2 μsec. An oscillator repetetively triggers the gate circuit forming a picket fence drive to allow for variations in motor power factor. One pulse of this fence ultimately triggers the device.

Referring to Figure 3.33, the amount of charge delivered to the gate during the initial pulse is determined by the charge stored in Cg, and the transformer turns ratio N of the gate drive isolation transformer.

$$Q_{gate} \cong 2V_s CgN \qquad [3.37]$$

where $\pm V_s$ are the logic supply voltages in Figure 3.33.

With the components selected for the gate circuit implementation $Q_{gate} \cong 5\mu coul$.

COMMUTATION ENERGY CONTROL

The commutation voltage control capability of the Gould inverter gives the designer flexibility in selecting commutation circuit component values. The peak stored energy (and, hence, the loss) of the commutation circuit can be minimized for a standard set of operating conditions, and then the comutation capacitor voltage may be varied to accomodate extremely heavy or light loads.

The scheme used to control the peak commutation capacitor voltage is described in this section. It is shown that efficient commutation voltage modulation can be achieved through feedback control of the main thyristor reverse-bias time, T_q. The algorithm used to determine the desired commutation voltage from reverse-bias time measurements is outlined. Finally,

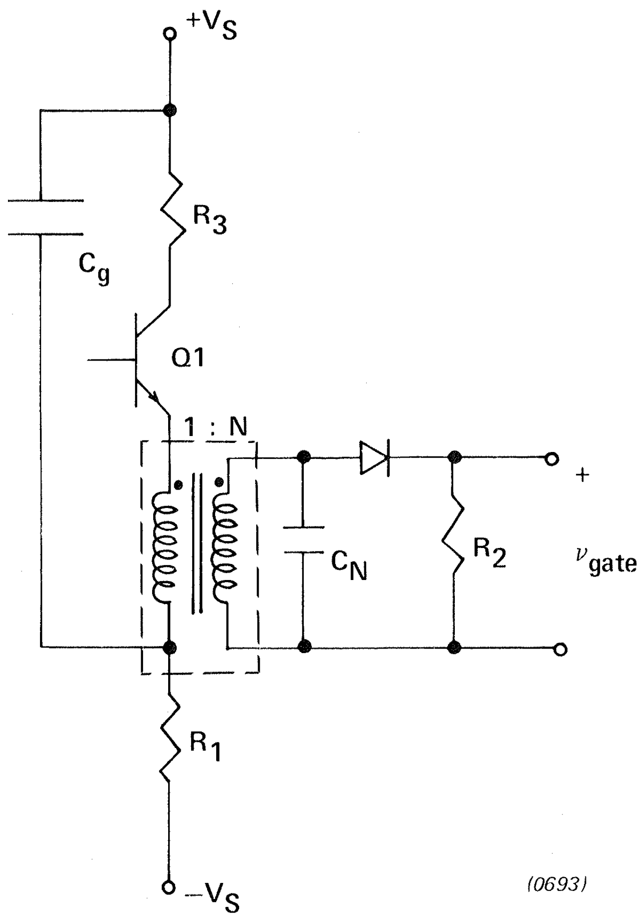

Figure 3.33 Schematic of Thyristor Gate--Drive Circuit. Transitor "Dumps" Capacitor (Cg) Charge, through Transformer, into Thyristor Gate. Repetedly Triggering Q1 Produces the Traditional Picket Fence Drive Shown in Section IV

the actual circuit implementation of the control scheme is discussed, which controls the triggering of SCR 9, and SCR 10 respectively. The power circuit topology was previously presented.

It is shown in Appendix II that, given a particular set of commutation circuit component values, the commutation voltage required to turn off the main devices varies with both battery voltage and current, according to the relation

$$\frac{V_c}{V_{bat}} = \left[\frac{1+x}{W_{min}} \right] \left[\frac{V_{bat}'}{V_{bat}} + \quad 1 - W_{min}^2 \quad \frac{I_{bat}'}{I_{bat}} \right] \qquad [3.40]$$

where V_{bat}' and I_{bat}' are the instantaneous battery voltage and current, respectively, V_c is the required commutation voltage, V_{bat} is the nominal battery voltage, I_{bat} is the nominal full load inverter current, and all other terms are defined in Appendix II.

Given the largest forseeable values of V_{bat}' and I_{bat}', a maximum necessary commutation voltage, $V_{c(max)}$, may be calculated. If V_c is simply set equal to $V_{c(max)}$, then the commutation circuit will always be able to turn off the main devices. The reverse bias time, T_q, will be at least $T_{q_{min}}$ with high power output levels, and much longer when the motor is unloaded.

Since a smaller voltage would be sufficient to obtain the required reverse-bias time at light loads, commutation circuit losses could be reduced by using only that voltage which is necessary to maintain $T_q > T_{q_{min}}$. The function of the commutation energy control circuit is, thus, to vary the commutation voltage so as to keep the reverse-bias time nearly equal to $T_{q_{min}}$.

The actual control algorithm can be best described as a two-stage process. In the first stage, the measured reverse-bias time for the last commutation is transformed into an intermediate voltage request for the next commutation, according to the relationship pictured in Figure 3.34. This request voltage is passed to a second stage, a non-linear low-pass filter. It

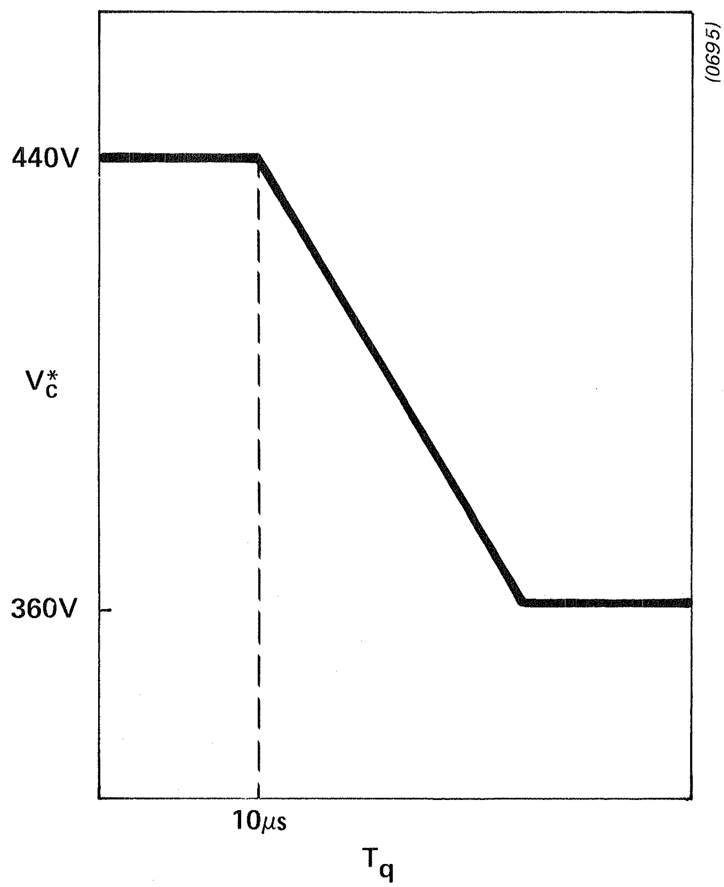

Figure 3.34 Plot Showing Commanded Commutation Capaciter Voltage, V_c^* as a Function of Measured Thyristor Reverse-Bias Time, T_q

is non-linear in that it has different time constants for rising and falling signals. The output voltage will rise towards the input signal level with a time constant on the order of 100μsec if it is lower. If the output level is above that of the input, then it will decay towards a minimum value with a 10 second time constant. Thus, if the measured reverse-bias time for a commutation is smaller than the desired time, the voltage for subsequent commutations is increased very quickly. If the reverse-bias time is longer than necessary, then the commutation voltage will fall slowly. This slow response to a long reverse-bias time is necessary for stable commutation voltage control.

Commutation voltage modulation occurs only when the controller is in the six-step mode (maximum motor voltage). For operation in the pulse width modulation regime, the commutation voltage is fixed at its maximum value. During six-step operation, the commutation voltage varies from 360 to 440 volts, depending on the motor load. The 37% reduction in initial stored energy has a significant impact on the circuit losses at light motor loads. The main device reverse-bias time measurement is provided by observation of the bus voltage, V_{ab} measured from the common anode of the upper bus thyristors to the cathode of the lower three (Figure 3.35). Whenever V_{ab} is negative, either the upper or lower main thyristors are reverse-biased.

The rectified bus voltage is passed through an isolation (step-down) pulse transformer to the control logic, where it is converted to a logic high value for the duration of the reverse-bias interval. This logic signal controls the charging of a timing capacitor whose voltage at the end of the interval is proportional to the latest reverse-bias time. The capacitor voltage is inverted, amplified, and sampled after the logic signal drops. This resulting voltage is the intermediate commutation voltage request, or, the first stage output. These stages are illustrated in Figure 3.35.

The non-linear low-pass filter is implemented with the circuit shown in Figure 3.36. The holding capacitor is charged through R_c, and discharged through Re. A factor of 10^5 between resistances allows rapid charge, but slow

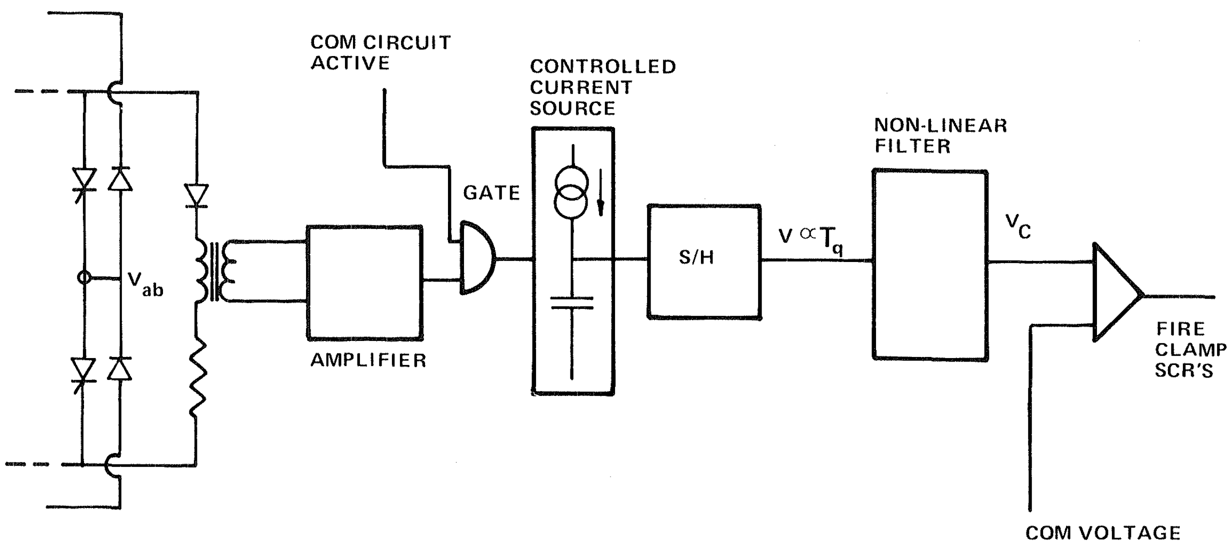

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Figure 3.35 Commutation Energy Control Block Diagram

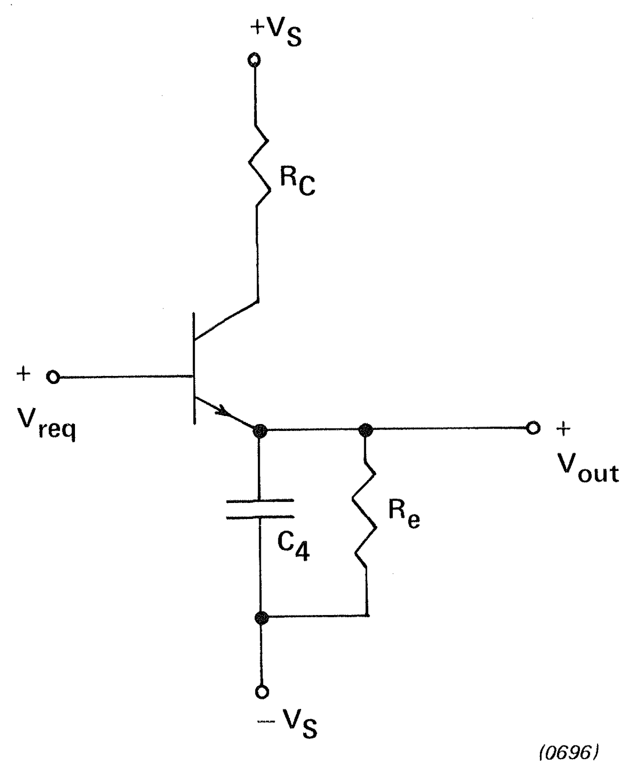

Figure 3.36 Non–Linear Low–Pass Filter (Output Stage for Commutation Energy Control Circuit)

discharge of C_4. This stage is followed by a circuit which limits the maximum and minimum commutation voltage signal.

The actual commutation capacitor voltage is measured by a sense winding on each commutation transformer, and compared to the energy control circuit output. The clamp thyristors are fired when the commutation voltage reaches the desired value. The implementations of the sense windings installed on each commutation transformer, T1 and T2, are illustrated in Appendix IV.

INVERTER LOSSES

In this section, the three major sources of inverter loss, main conduction, main switching, and commutation circuit loss are examined. It is seen that the contribution made by switching losses is small enough to be neglected. Equations are presented which approximate the remaining losses as a function of the inverter operating point.

The inverter electrical losses are dominated by the main SCR on-state conduction losses and commutation circuit component loss. Main device switching losses are small in comparison to these two. The category of main SCR switching loss is further divided into the areas of turn-on and turn-off loss. For the calculation of thyristor turn-on loss, the voltage and current waveforms shown in Figure 3.37 are used. The thyristor is assumed, initially, to be in the off state, blocking a forward voltage, V_{bat}. During the rise time, T_{on}, the voltage falls linearly to zero, while the current rises to the value, I_{bat}. Due to finite power stage leakage inductances, the current normally does not reach its final value by the time that the voltage has fallen. Thus, the estimate made here is a conservative one. The energy loss is simply the time integral of the v.i product over the turn-on interval. The power loss is the product of this energy and the total circuit independent inverter switching rate, f_{com}.

$$P^{SCR1}_{turn\text{-}on} = 1/6\ V_{bat} I_{bat} T_{on} f_{com} \qquad [3.41]$$

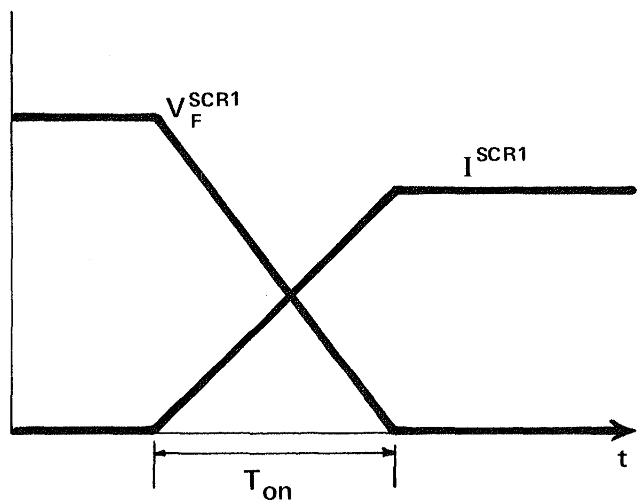

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Figure 3.37 Idealized Voltage and Current Waveforms used to Calculate Main Thyristor Turn–On Switching Loss

Actually, the battery current is sometimes distributed between two thyristors instead of one. But, since the loss is linear in I_{bat}, this does not affect the total loss estimate.

The turn-off loss is estimated by the use of data on the thyristor recovered charge, Q_r. Such data is normally supplied by manufacturers as a function of the peak thyristor current and rate of turn-off (di/dt). Figure 3.38 shows the idealized thyristor voltage and current waveforms. Again, the energy loss is simply the time integral of voltage and current.

$$P_{turn\text{-}off} \cong V_R^{SCR1} \; Q_r \; f_{com} \tag{3.42}$$

With a turn-off rate of 300 A/μsec, a junction temperature of 125C, and thyristor current of 600 Amps, the recovered thyristor charge is about 60 μcoul. V_R^{SCR1} has a maximum value of 190 volts (before reverse recovery), giving $P_{turn\text{-}off} = 27$ W.

The total main switching losses are less than 60 watts. An estimate of the on-state thyristor conduction loss, assuming two semiconductor voltage drops, V_d, in series with the motor, gives

$$P_{on\text{-}state} \sim 2 I_{bat} V_d \tag{3.43}$$

With an on-state voltage drop V_d of 1.3 volts, $P_{on\text{-}state} \sim 1560$ W

The main device switching losses are negligible in comparison. In Appendix III, the switching losses encountered in the main snubbers are examined. The estimated maximum main snubber loss is seen to be about 100 watts. During six-step operation, the maximum loss is closer to 45 watts.

A more accurate expression for the main device losses is obtained by accounting for reactive currents carried by the freewheeling diodes. The equation given below is derived in Appendix III. Given a semiconductor on-

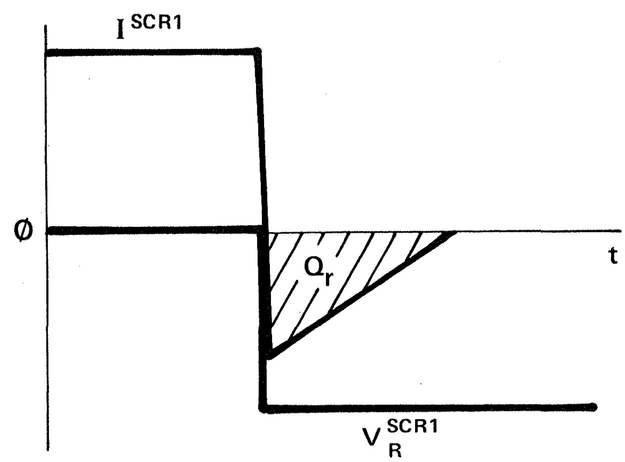

Figure 3.38 Current and Voltage Waveforms used to Estimate Thyristor Turn-Off Switching Loss

state voltage drop, V_d, battery voltage, V_{bat}, battery power, P_{bat}, and motor power factor, $\cos(\theta)$,

$$P_{on-state} = \frac{2V_d}{V_{bat}} \cdot \frac{P_{bat}}{\cos\theta} \qquad [3.44]$$

With the required shaft power, P^e, as well as motor and (estimated) inverter efficiencies, $P_{on-state}$ = 1530W when the battery is delivering approximately 36 kW, or full rated power.

The commutation circuit losses have been empirically found to be proportional to the peak stored energy of the commutation transformers. These losses are entirely due to the non-ideal nature of the commutation circuit elements (particularly the transformer). If V_c is the commutation voltage, C^T, the total commutation capacitance, L^A the transformer T1A winding inductance, I_{bat} the average dc bus current, this peak stored energy is

$$U_p = \tfrac{1}{2} C^T V_c^2 + \tfrac{1}{2} L^A (I_{bat})^2 \qquad [3.45]$$

Thus, the commutation circuit loss is

$$P_{com} = K_m f_{com} [\tfrac{1}{2} C^T V_C^2 + \tfrac{1}{2} L^A I_{bat}{}^2]$$

$$= 820 \text{ W at } 900 \text{ Hz}$$

Km is an empirically determined constant, equal to about 0.17 for the Gould controller. The dc bus current is roughly $\sqrt{2}$ times the RMS phase current if the phase waveforms are sinusoidal.

IV. Controller Operation and Description

The controller for the ac induction motor coordinates the voltage and frequency applied to the motor terminals. To accomplish this task, the controller physically consists of five major functional blocks. These circuit blocks are the control logic power, excitation frequency logic, PWM voltage algorithm logic, the system control module (a microcomputer) and the power inverter. The organization and the operation of these five major circuit groups is presented in this section.

4.1 Control Logic Power

The function of the control logic power section is to generate the voltages required by the controller circuitry. Since most electric vehicles currently in use have both a 12 Vdc battery and a propulsion battery, the input power source to the control logic power section may be selected from these two choices. Tapping the series battery chain which forms the propulsion battery is not permissible because it preferentially discharges those batteries which supply both tractive power and logic power. In this controller design the propulsion battery with a nominal rating of 120V was chosen as the input power source for the control power.

The voltages required by the controller circuitry are listed in Table 4.1.

TABLE 4.1

CONTROL LOGIC VOLTAGE REQUIREMENTS

+ 5V dc	2A
+15V dc	1A
-15V dc	1A
+12V dc	2A
-12V dc	20mA

The design approach selected for the control logic power supply is a dc-dc switching converter in series with a linear voltage regulator. The linear regulator limits the maximum dc-dc converter input voltage to 85V. During regeneration, the propulsion battery voltage can exceed 140V and drop below 80V during motoring. Figure 4.1 is a block diagram representation of the control logic power. The logic system of the motor controller consumes approximately 50W. The electrical schematic can be found in Appendix IV.

4.2 Excitation Frequency Logic

As previously described, the control strategy selected for this ac propulsion system is one employing slip control. A major advantage of this particular control philosophy is that it is easily adapted to conventional ac induction motors with only the addition of a tachometer. This provides a general scheme which is completely motor independent while incorporating customary types of industrial transducers.

The function block diagram is illustrated in Figure 4.2. As shown in the figure, accelerator and brake commands are summed to determine the overall torque, and thus slip frequency, requested. This slip command is then summed with the shaft speed tachometer signal to derive the motor excitation frequency.

The digital tachometer itself is constructed of a stainless steel disk with two tracks of information and optical detectors. Each track contains 252 pulses/revolution with the two tracks etched in quadrature. The tachometer logic sums the two pulse trains to generate a base pulse train of 1008 pulse/revolution by detecting logic level transitions. This signal corresponds to an electrical frequency, at zero slip, of 504Hz per mechanical Hz since the motor has four electrical poles. The disk is seen in Figure 4.3a along with the tachometer logic PC board. Figure 4.3b is a detailed picture of the disk. The quadrature relationship of the tachometer pulse trains also provides rotation direction information by observing the phase relationship between the two pulse trains. The tachometer logic schematic is contained in Appendix IV.

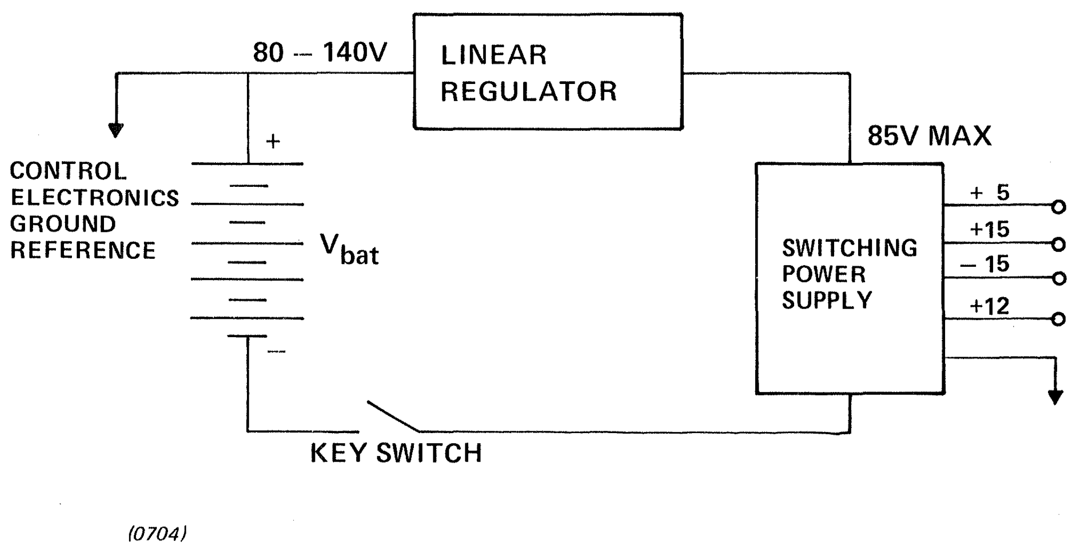

Figure 4.1 Control Power Electronics Suppy Schematic

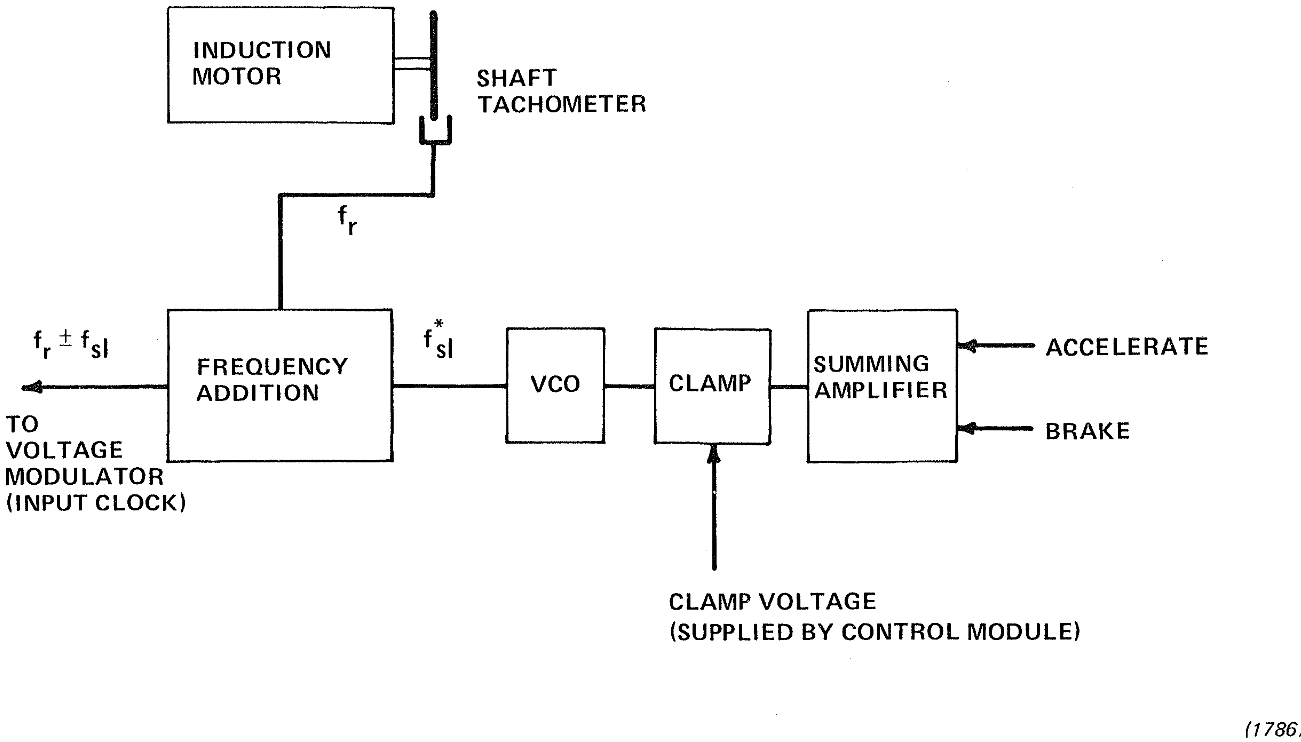

Figure 4.2 Excitation Frequency System Block Diagram

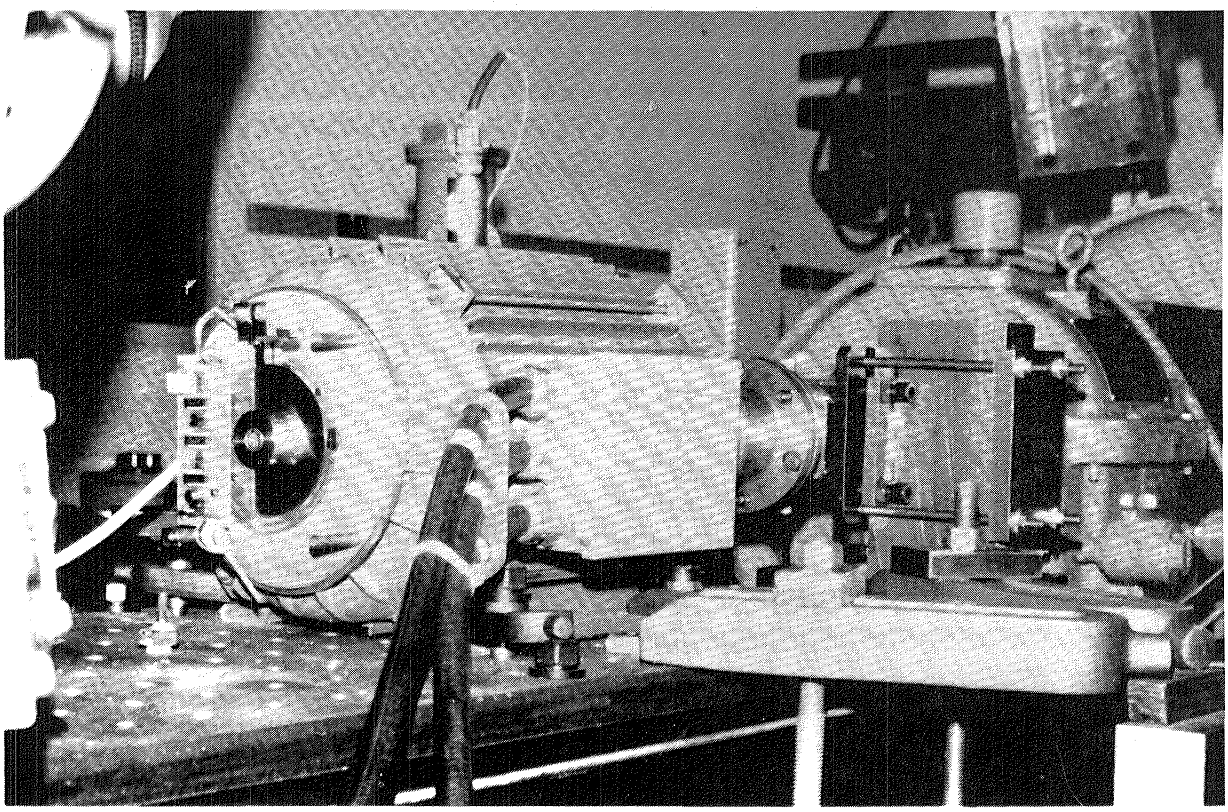

Figure 4.3(a) Motor Tachometer System

The tachometer is retrofitted onto the end of the induction motor. It consists of a stainless wheel and two optical detectors, one for each track. Tachometer electronics is included on the PC board to support the optical detectors.

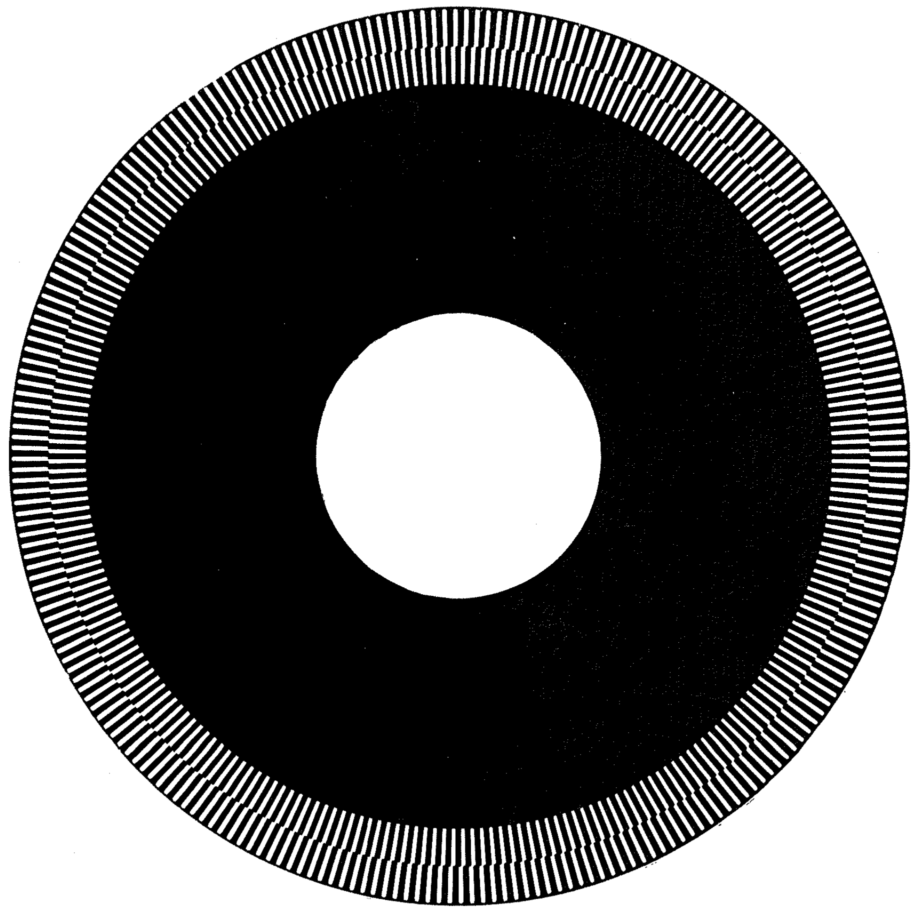

Figure 4.3(b) Detail of Tachometer Encoder Disk

Note that the two tracks of information are etched in quadrature to provide direction information.

The digital pulse train generated by the tachometer, f_{tach}, is algebraically summed with the slip frequency, f_{sl}^{VCO}, generated by the slip frequency VCO, to yield the voltage modulator clock frequency f_{vm}. f_{vm} is directly scaled to the inverter output frequency, f_{ex}. The output of the voltage modulator circuit is six parallel signals of frequency f_{ex}, each representing the desired state, off or on, of the six main thyristors in the power circuit. The following constants define the relationship among f_{tach}, f_{sl}^{VCO}, f_{vm}, and the mechanical shaft frequency f_{shaft}, f_{ex}, and the motor slip frequency f_{sl}. A complete schematic of the frequency excitation logic is included in Appendix IV.

$$f_{tach} = f_{shaft}/1008$$

$$f_{sl}^{VCO} = \frac{f_{sl}}{4032}$$

$$f_{vm} = f_{sl}^{VCO} + f_{tach}$$

$$f_{ex} = \frac{f_{vm}}{504}$$

4.3 Voltage Modulator Logic

The objective of the voltage modulator is to provide a means of controlling the inverter output voltage so that a constant air gap flux (i.e. volts/hertz) can be maintained over a wide motor speed range. This capability is essential for the control philosophy selected. Primary design objectives included a 20:1 dynamic control range in the fundamental output voltage, symmetrical excitation waveforms between all three phases and circuit modularity. These objectives were all achieved primarily using discrete low power digital logic and some support analog circuitry.

The voltage modulation hardware implements a standard pulse width modulation strategy based upon the comparison of a sine function generated at the inverter electrical frequency, f_{ex}, and a triangle function of frequency $n f_{ex}$, where n is restricted to the integer values of 9, 27, 45, 63 and 81. A schematic function diagram for the modulator circuit is illustrated in Figure 4.4 and the electrical schematic is included in Appendix IV.

The three sinusoidal waveforms originate from 8 bit PROMS which are clocked to generate a complete half cycle sinusoidal. These digital words are applied to multiplying D/A converters which result in discrete analog signals whose amplitudes are controlled by reference inputs set by the modulation index described in Section III. A similar technique is used for the triangle generation except that a simple up/down counter replaces the PROMS.

The digital data representing the sine wave is stored with 7 bit magnitude resolution. Half an electrical cycle is defined using 126 successive memory locations. To complete a triangle, 56 clock pulses are required. The triangle magnitude resolution is 4 bits. Table 4.2 illustrates the digital representations of the sine function and triangle functions. The gating of the main inverter power devices are determined by the intersections of the two functions as illustrated in Figure 4.5. Comparators with special debounce circuitry determine these points of intersection from the discrete analog waveforms. The relative amplitude of the sine and triangle therefore determine the points of intersection which in turn changes the PWM waveform and thus the voltage applied to the motor. The ratio of the sine and triangle reference amplitudes is known as the modulation index, m_i, as shown in Figure 4.5. These amplitude controls are the only control inputs to the voltage modulator. The ratio of the triangle wave frequency to the sine reference frequency, n, is always an odd integral value of 3 in order to achieve the desired symmetries among the three phase voltage and current waveforms. The value of n is adjusted as the excitation frequency is changed to control the harmonic content of the phase currents at all speeds without making unacceptable demands on the commutation circuit cycling frequency. The sine and triangle generators schematic is contained in Appendix IV.

Figure 4.6 illustrates the operation of the voltage modulation circuitry. Figure 4.6a displays the analog sine and triangle waveforms and 4.6b displays the output of the comparator circuitry. This logic signal provides the basis for controlling the SCR gating circuitry and commutation logic.

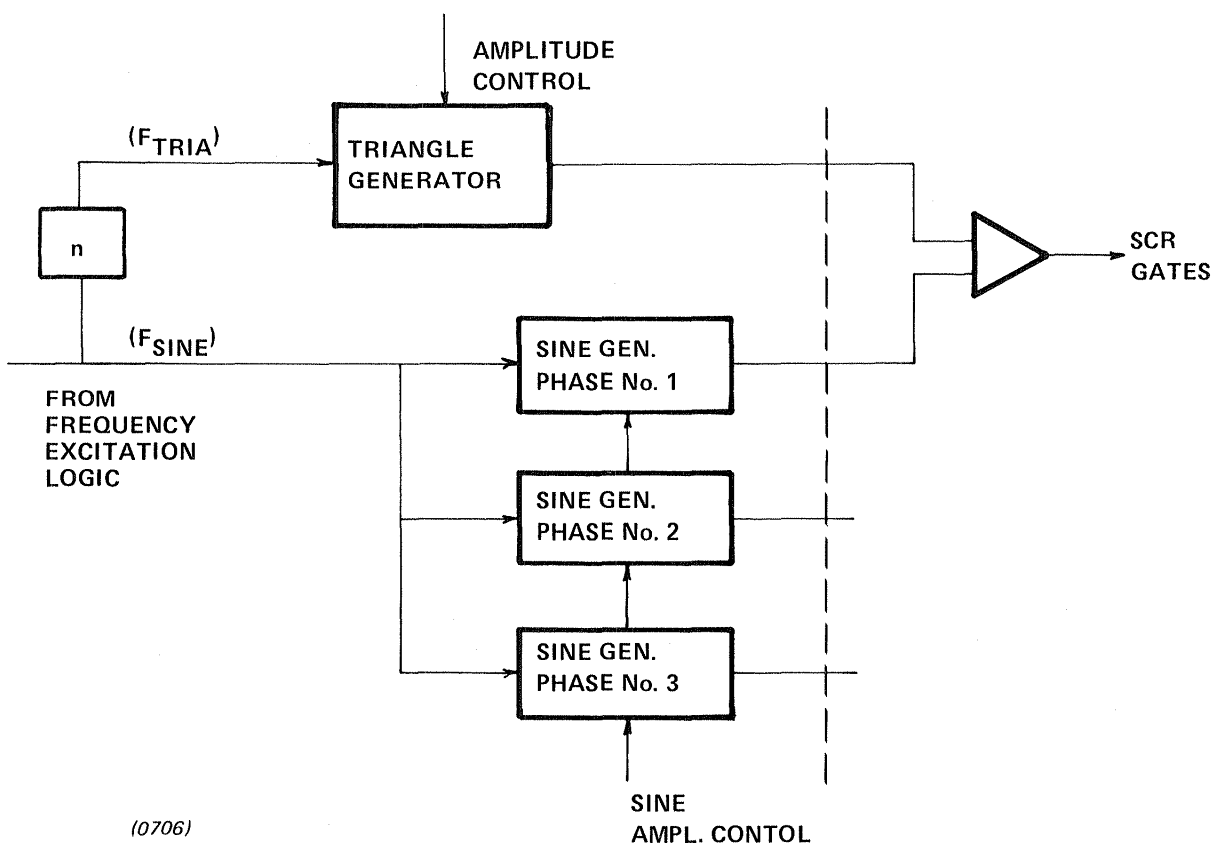

Figure 4.4 Voltage Modulator Function Schematic

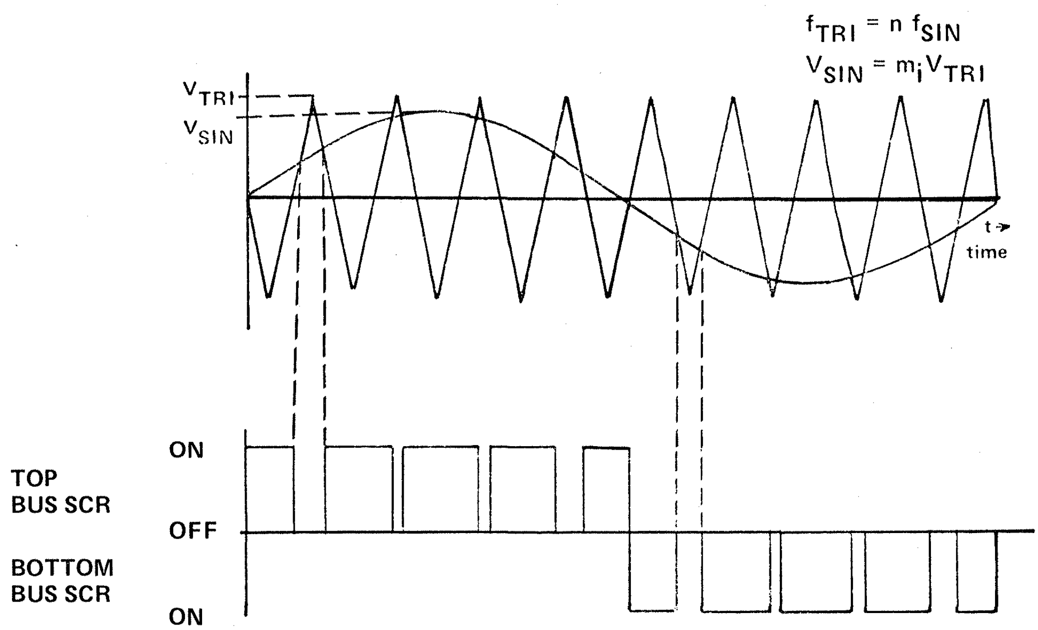

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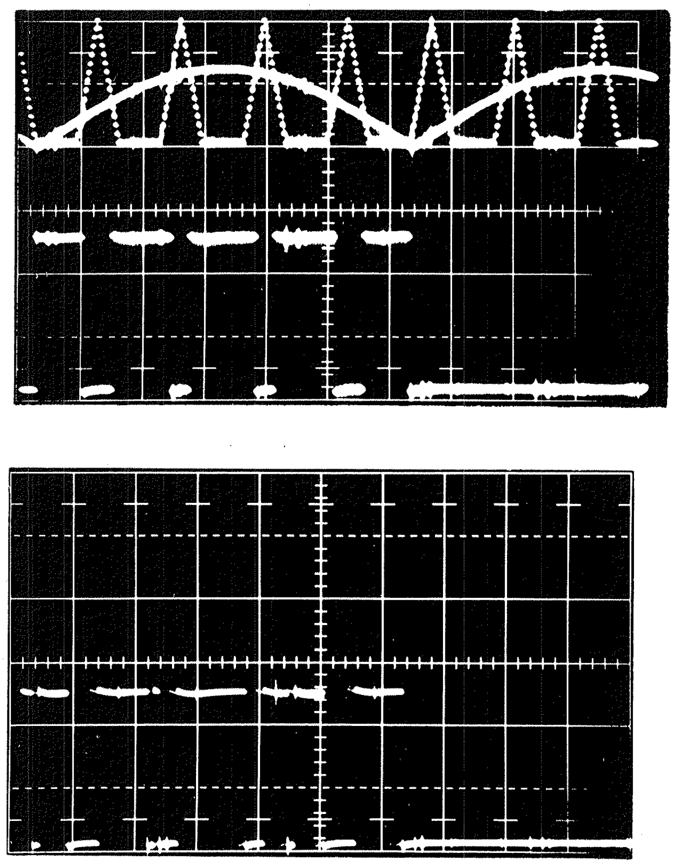
Figure 4.5 **Voltage Modulator Algorithm**



(a) GENERATED SINE AND TRIANGLE FUNCTIONS

(b) COMPARATOR OUTPUT

(c) COMPARATOR OUTPUT MODIFIED BY COMMON BUS COMMUTATION REQUIREMENTS

(0708)

Figure 4.6 PWM Algorithm Main Thyristor Gating Signals

TABLE 4.2

DIGITAL SEQUENCE REPRESENTING SINES AND TRIANGLES

(All Data Represented in Hexidecimal Notation)
(Bit 7 = Sign Bit 0 - Bit 6 = Magnitude)

Sine
Phase Prom
A Addresses

0000	FF	83	86	89	8C	8F	93	96	99	9C	9F	A2	A5	A8	AB	AE
0010	B1	B4	B7	BA	BD	C0	C2	C5	C8	CA	CD	CF	D2	D4	D7	D9
0020	DB	DD	DF	E2	E4	E6	E7	E9	EB	ED	EE	E0	F1	F3	F4	F5
0030	F7	F8	F9	FA	FB	FC	FC	FD	FE	FE	FF	FF	FF	FF	FF	FF
0040	FF	FF	FF	FF	FF	FE	FE	FD	FC	FC	FB	FA	F9	F8	F7	F5
0050	F4	F3	F1	F0	EE	ED	EB	E9	E7	E6	E4	E2	DF	DD	DB	D9
0060	D7	D4	D2	CF	CD	CA	C8	C5	C2	C0	BD	BA	B7	B4	B1	AE
0070	AB	A8	A5	A2	9F	9C	99	96	93	8F	8C	89	86	83	80	03
0080	06	09	0C	0F	13	16	19	1C	1F	22	25	28	2B	2E	31	34
0090	37	3A	3D	3F	42	45	48	4A	4D	4F	52	54	57	59	5B	5D
00A0	5F	62	64	66	67	69	6B	6D	6E	70	71	73	74	75	77	78
00B0	79	7A	7B	7C	7C	7D	7E	7E	7F	7F	7F	7F	7F	7F	7F	7F
00C0	7F	7F	7F	7E	7E	7D	7C	7C	7B	7A	79	78	77	75	74	73
00D0	71	70	6E	6D	6B	69	67	66	64	62	5F	5D	5B	59	57	54
00E0	52	4F	4D	4A	48	45	42	40	3D	3A	37	34	31	2E	2B	28
00F0	25	22	1F	1C	19	16	13	0F	0C	09	06	03	00	FF	FF	FF

Triangle

Counter Sequence

1 2 3 4 5 6 7 8 9 A B C D E F

E D C B A 9 8 7 6 5 4 3 2 1 0

Since independent control of all SCR's connected to one battery bus is not possible with the bus commutation power circuit topology, the need to commutate one SCR affects the gating signals applied to all SCR's on that bus. Figure 4.6c illustrates the logic signal actually controlling the SCR main conduction periods. It differs from 4.6b by the introduction of logic zeros to inhibit the gating signals to all of SCR's on a common bus during commutation. For example if SCR 1, 2, and 3 were in conduction, and SCR 1 was to be commutated off, the gating signal would be removed from SCR 1 and inhibited on SCR 3 during the top-bus commutation interval. The inhibit signals are derived from the logic signals which trigger SCR 7 or SCR 8. The gate waveform generator schematic is contained in Appendix IV.

4.4 System Control Module

The system control module performs the actual voltage and frequency excitation coordination. This is accomplished directly by varying the analog inputs to the voltage modulator in response to commanded torques and excitation frequency. In the controller itself, the hardware selected to perform this coordination is a microcomputer based on the MC6802 microprocessor.

The primary task which is placed on the microprocessor in this systemm design is that of performing the volts/hertz regulation to keep the induction machine air gap flux constant. The sensed input is a volts/hertz weighted signal derived from measuring the excitation voltage and frequency. The implemented algorithm consists of a proportional plus integral type of control scheme with machine and load dependent factors. The algorithm is discussed in detail in Section III of this report. The algorithm's operation is slaved to the operating frequency of the inverter so as to calculate a new voltage correction factor on a once-per-cycle basis. The calculated error signal is used to control the sine-triangle amplitudes of the voltage modulator to maintain constant air-gap flux.

The software which accomplishes the voltage and frequency coordination is designed using an interrupt program structure in which execution of the voltage control algorithm is initiated once every electrical cycle. All the remaining microcomputer functions, for example, controller sequencing (power-up) and protection coordination (temperature limits), are performed sequentially at low priority as real CPU time is available with an executive program. The executive/interrupt program interaction is illustrated in Figure 4.7.

Figure 4.7 emphasizes that the voltage control algorithm execution can be initiated at any time by suspending execution of the executive algorithm until the control routine is complete. The interruption occurs once per electrical cycle (excitation frequency) and is triggered by the excitation frequency pulse train.

The algorithms for the microcomputer are implemented in Motorola 6802 assembly language. The detailed programs are included in Appendix V. Flow chart representations of both the executive code and the voltage control code is illustrated in Figures 4.8 and 4.9 respectively.

On the executive level, (Figure 4.8), specific sequencing operations performed under microprocessor supervision include system power-up initialization, enabling of the main and commutation thyristor gating signals, and controller interlocking to prevent invalid operation. The system monitors key controller components for dangerous operating conditions such as overtemperature and overvoltage, and sends warnings to the operator and/or shuts down the controller as the situation warrants. A watchdog timer is included to protect the system from processor malfunctions.

As shown in Figure 4.9, the voltage control flow chart, the microprocessor receives updated readings of the operator torque request, the excitation frequency and the measured motor volts/Hz at the beginning of each interrupt cycle. These inputs are used to calculate an error signal corresponding to the difference between the desired and measured instantaneous motor volts per hertz values. This error signal then generates commands to the voltage modulator logic to control the reference sine and triangle waveform amplitudes, and hence, the motor terminal voltage. Execution of this algorithm is slaved to the excitation frequency to produce updated commands to

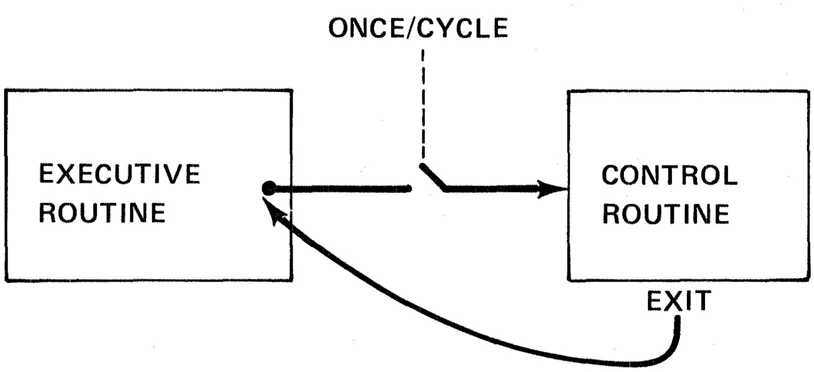


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Figure 4.7 Executive/Interrupt Code Interaction

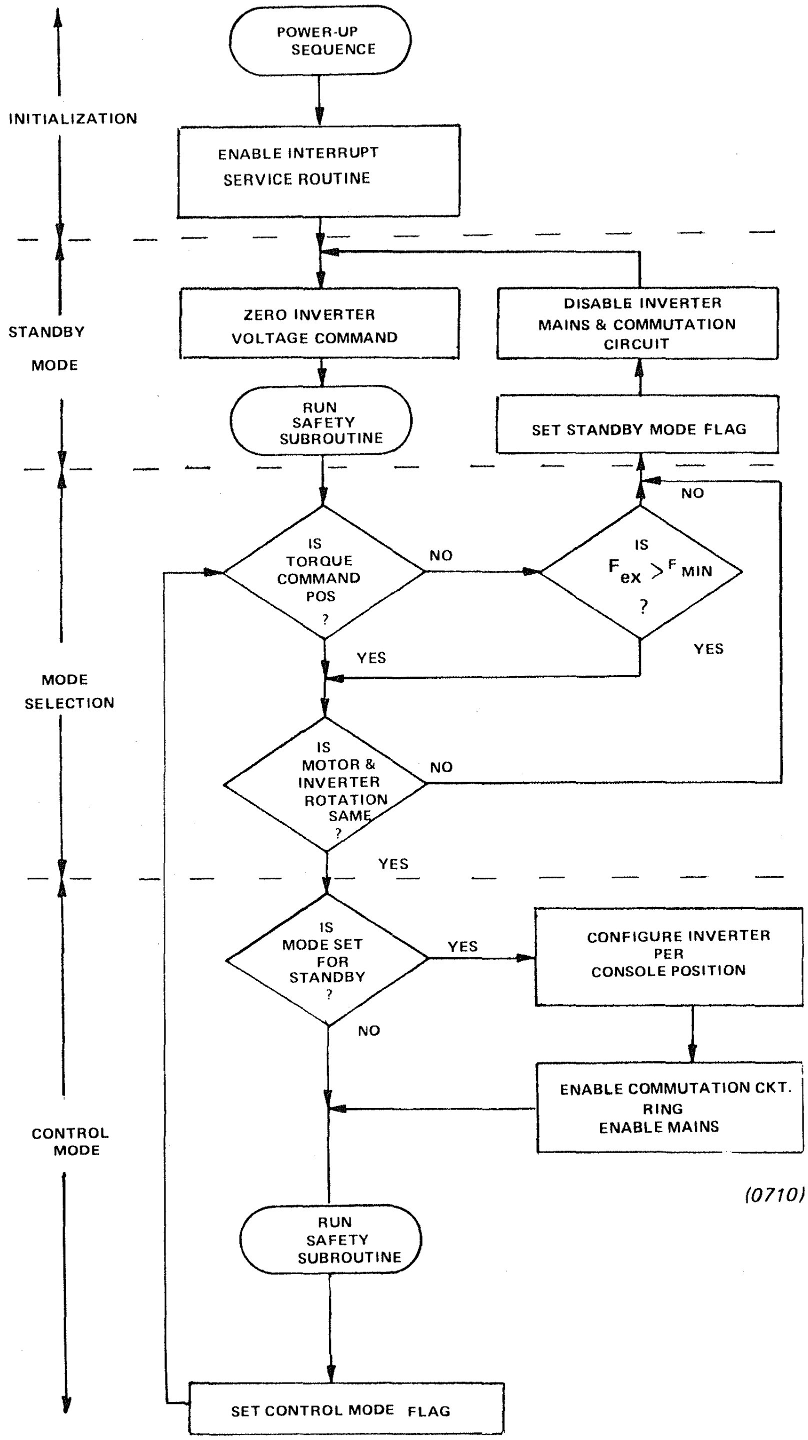


Figure 4.8 Executive Program Flowchart

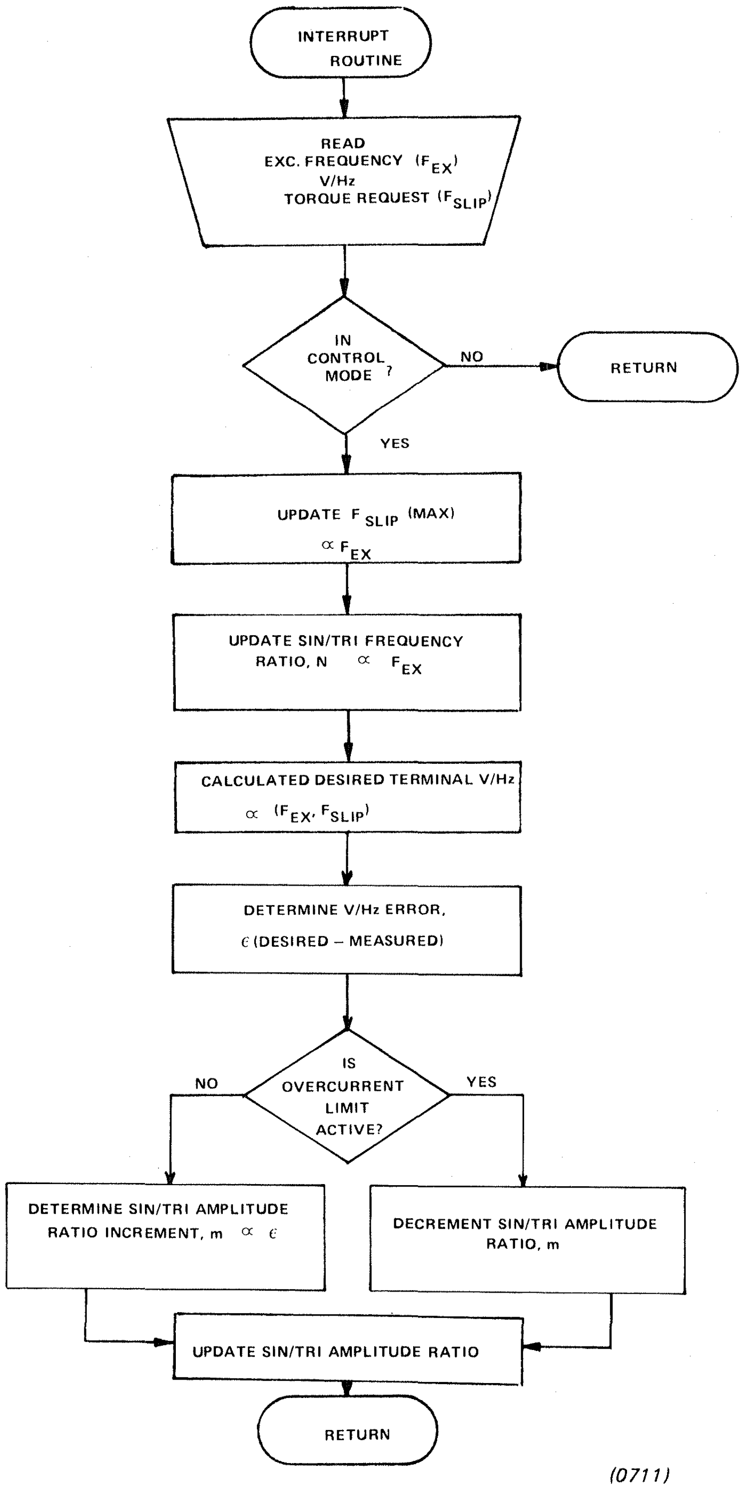


Figure 4.9 Flowchart of Voltage Control Interrupt Routine

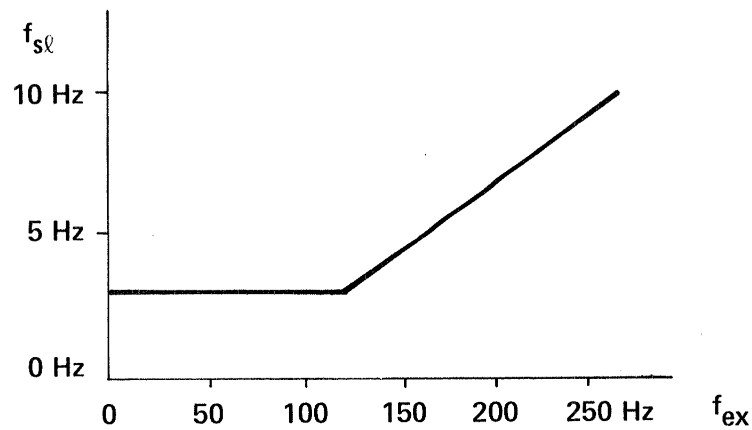
the voltage modulator once per cycle, which is the measurement period for the motor terminal voltage fundamental frequency component.

An additional task performed during the interrupt routine is the generation of a slip frequency limit command to override excessive torque requests by the operator. This function is illustrated in 4.10a. Below excitation frequencies of 120Hz, the slip limit is set to 3Hz, linearly increasing to 10Hz at the maximum excitation frequency of 266Hz. Finally, the interrupt routine also performs the selection of the desired triangle frequency multiplier based upon the instantaneous excitation frequency value. This function is shown in Figure 4.10b. Hysteresis is provided by the software to prevent oscillations in the multiplier value in the vicinity of the transition points.

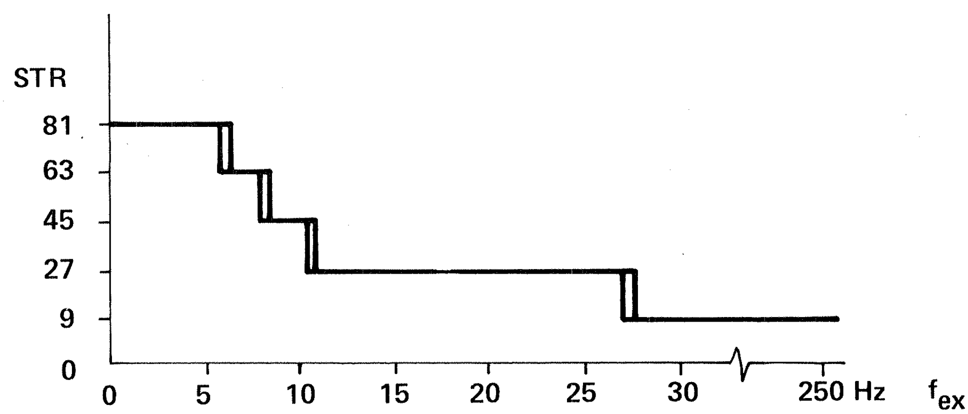
The control functions which have been discussed are accomplished using a Motorola 6802 microprocessor with 2K words of external program memory. A block diagram of the microcomputer architecture is illustrated in Figure 4.11. As illustrated in the figure, the microcomputer system contains a system clock, digital I/O capabilities, and analog I/O capabilities. Programmable timers are connected directly to the computer's data bus to measure inverter excitation frequency. Complete electrical schematics are included in Appendix IV.

Safety

The system includes several types of safety features for both the operator and controller protection. Thermal protection of critical controller components constitutes the major source of system protection. Thermistors continuously monitor the operating temperatures of both the main and commutation SCR's in addition to the commutation capacitors. Battery safeguards exist by calculating the effective open circuit battery voltage from a measurement of battery voltage and current. A fixed internal impedance of 2mΩ/cell is assumed The protection system functions at two levels for both over temperature and low battery. The first level results in a visual indication to the operator that an over temperature or low battery condition



(a) Slip Frequency Limit vs. Excitation Frequency



(b) Triangle Frequency Ratio vs. Excitation Frequency

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Figure 4.10 Control Functions Performed by the Microprocessor during the Interrupt Program

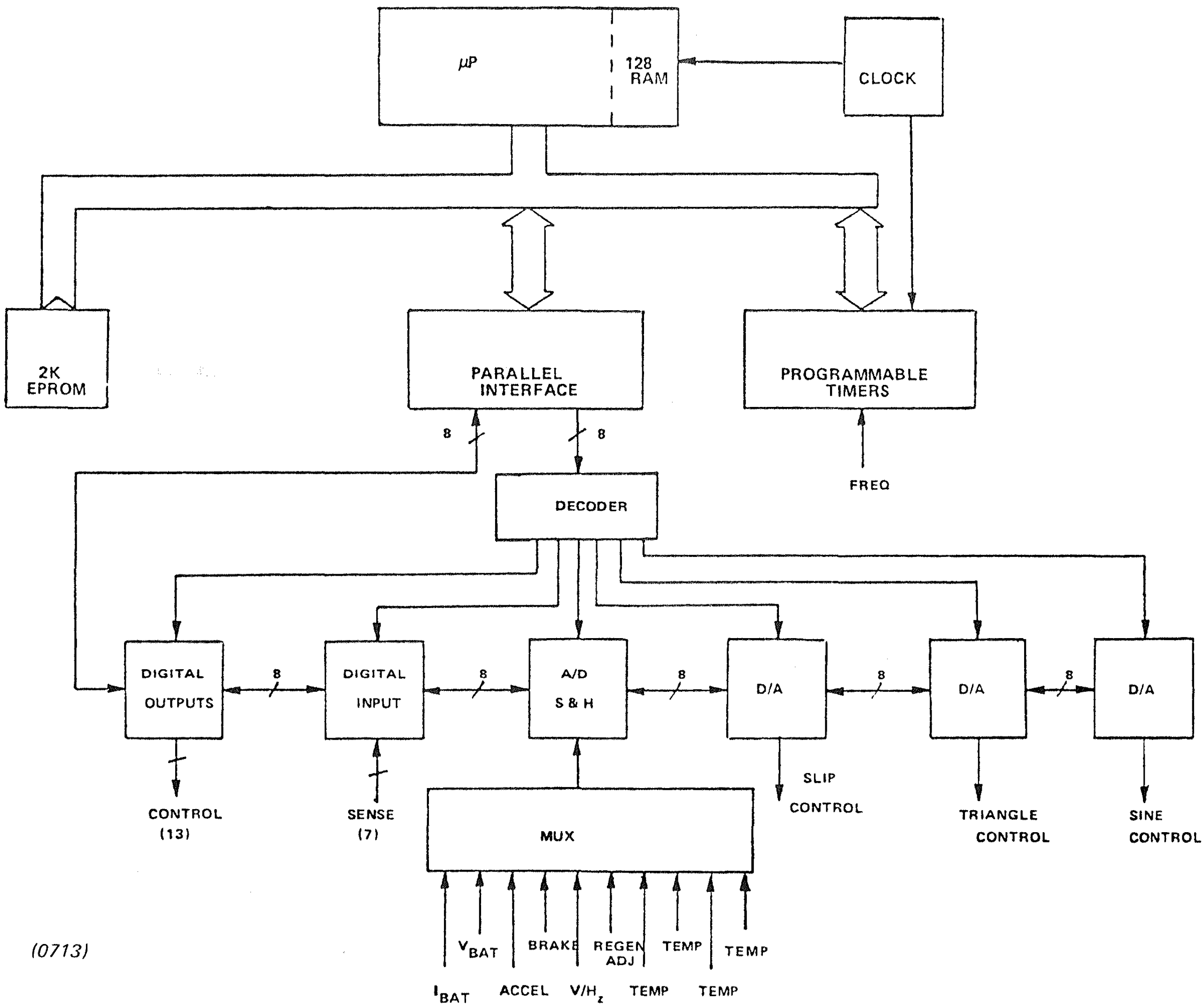

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Figure 4.11 Microcomputer Hardware System

TABLE 4.3

SYSTEM RESPONSE TO FAULT CONDITION

	System Condition	
	Stage 1	Stage 2
Temperatures		
Commutation Capacitor	>75 C	>80 C
Commutation SCR	>75 C	>80 C
Bottom Bus - SCR	>75 C	>80 C
Top Bus - SCR	>75 C	>80 C
Battery Voltage, V_{oc}	<111 V (1.85V/cell)	<102V (1.70V/cell
$V_{oc} = V_{bat} + I_{bat} * 120m\Omega$		
Current (Inverter Maximum)	>750A	

	System Indicators/Response	
	Stage 1	Stage 2
Temperature	"Overtemp" Indicator	"Emergency Shutdown" Indication and Controller Disable
Voltage	"Low Battery"	"
Current	Perform Commutation and "Overcurrent" Indication	n.a.

exists. The second level will actually cause an orderly propulsion system shutdown (all main SCR's are commutated off) with a visual indication provided to the operator showing that emergency shutdown has occurred. Table 4.3 illustrates the thermal temperature limits and the resulting controller reaction.

Interlocks have been designed into the system to offer an additional degree of safety. Operational interlocks prevent the controller from being operated in an invalid manner. Console direction selection will only be recognized if the motor is operating below 60 RPM. This prevents possible controller damage from inadvertent plugging commands. A "neutral" position which can be selected at any time forces the slip command to zero hertz and thus forces the developed motor torque to also be zero. These features are included in the excitation frequency logic. It should also be noted that after a shutdown has occurred the system will inhibit any further attempts to operate the controller. This mode will continue until the fault conditions subside and the system is reset with a power down - power up sequence using the front panel key switch. These interlocks should prevent unexpected system operation which could endanger the operator.

Several hardware interlocks can also inhibit controller operation. These features require proper connections (sensed by connector jumpers) to be made to the tachometer and console modules before normal operation is permitted. The controller key switch provides an ultimate means for system control by forcing an immediate shutdown under all operating conditions.

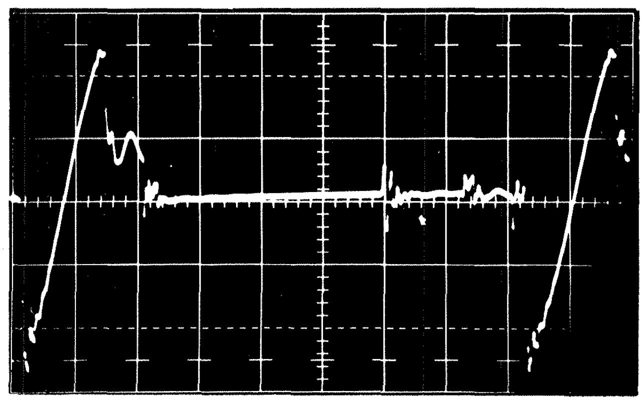
4.5 Power Inverter

The operation of the bus commutation inverter was described earlier in Section III with the aid of Figures 3.26 thru 3.30. This section presents oscillographs of the voltage and the current waveforms seen by the power stage components.

The voltage across SCR1 and SCR3 during an upper bus commutation interval is shown in Figure 4.12. The time that the voltage across SCR1 and SCR3 is negative is the available SCR turn-off time.

50V/DIV

0



(0714)

50μsec/DIV

Figure 4.12 SCR1 Voltage during Commutation Interval

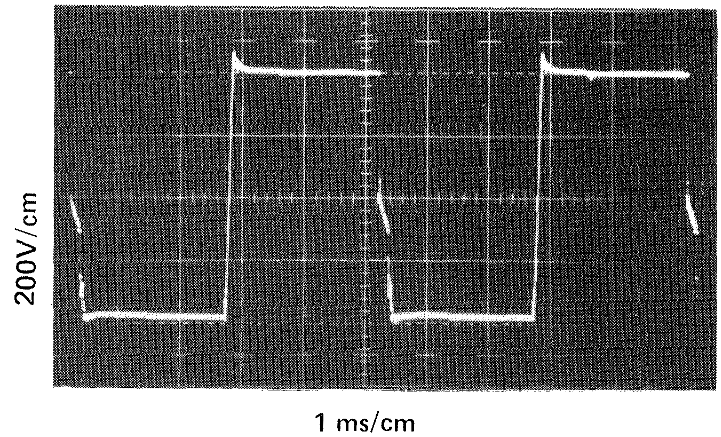
The voltage and current seen by SCR8 (or SCR7) during the commutation interval is shown in Figure 4.13. The current in SCR8 increases sinusoidally as determined by the characteristics of the resonant LC circuit.

After a period of time, depending on the resonant frequency of the LC circuit and the initial current in winding T1A, the voltage across capacitor C1 will reach zero and the current in windings T1A, B and SCR7 will be a maximum. For no-load operation, the time required for the current in SCR7 to reach its maximum value is approximately 50 μseconds. For operation under loaded conditions (i.e., an initial current in winding T1A), this time interval is reduced since the current in SCR8 will start the commutation cycle at a current proportional to that initially present in winding T1A. This is illustrated in Figure 4.13c and shows the current in SCR8 during a commutation cycle when current is initially present in winding T1A of the commutation transformer.

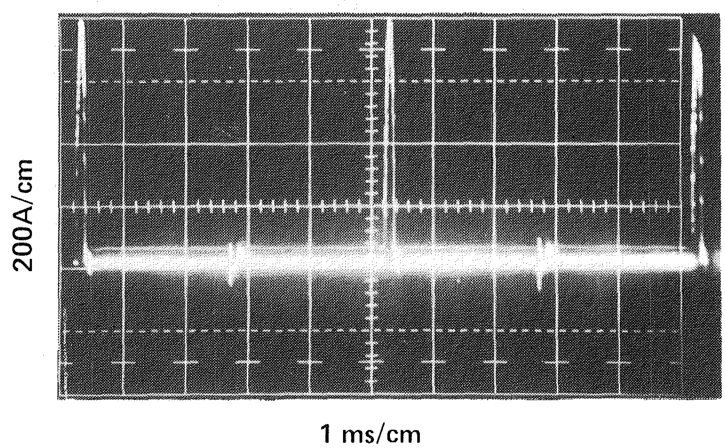
When the current in SCR7 has reached its maximum value capacitor C1 will begin to charge with a polarity opposite to that shown in Figure 3.25. At this point the voltage on capacitor C2 will also have a polarity opposite to that shown in Figure 3.25 and have a value equal to that of the propulsion battery.

When the voltage across capacitor C1 charges to a high enough value that SCR9 is forward biased, and assuming SCR9 is then gated, current will transfer to winding T1C, SCR9 and the propulsion battery. When this occurs the voltage across capacitor C1 will be higher than the relfected voltage across windings T1A, B and SCR7 will be reverse biased and thus turn-off. The voltage across commutation capacitor C1 is shown in Figure 4.14 and shows the voltage cycling between approximately 450 and 330 volts with a propulsion battery voltage of 120 volts. The transition time between these two extremes is the commutation interval.

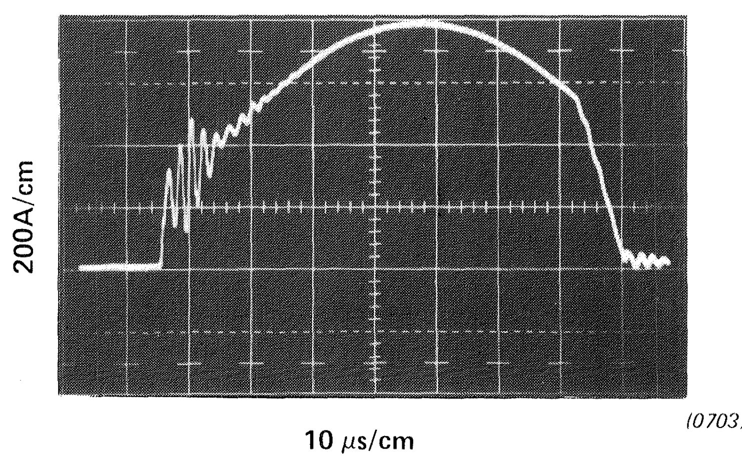
The current paths during the energy recovery portion of the commutation interval are shown in Figure 3.29. The voltage and current stresses seen by SCR9 are illustrated in Figure 4.15.



(a)
Voltage Across SCR 8 during Six - step Operation, f_{ex}=120 Hz



(b)
SCR 8 Current during Six - step Operation

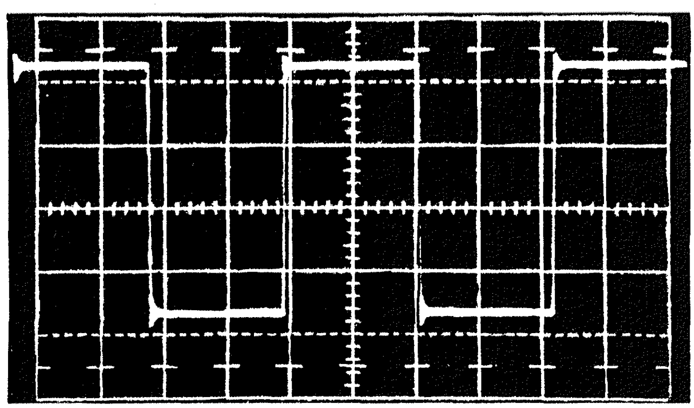


(c)
Expanded View of SCR 8 Current during Commutation

Figure 4.13 Commutation Thyristor Voltage and Current Waveforms during a Commutation

200V/DIV

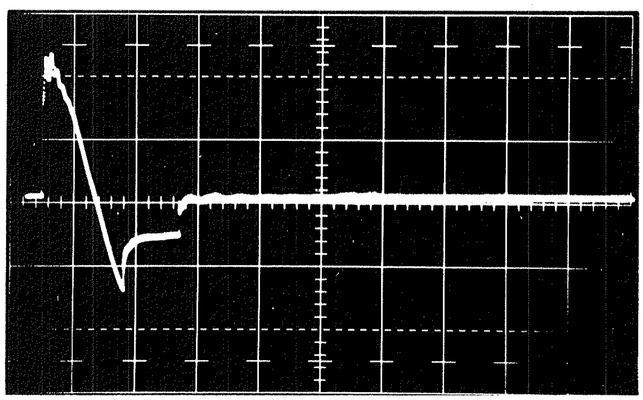
0



1ms/cm

(0715)

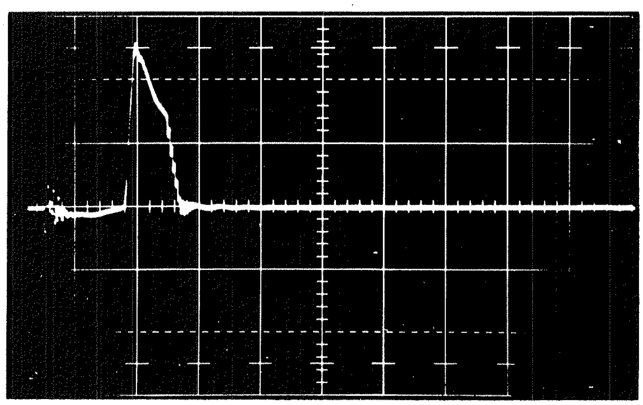
Figure 4.14 Capacitor (C1) Voltage during Commutation



200V/cm

10 μs/cm

(a)
Voltage Across SCR 9 during a Commutation Interval



100A/cm

10 μs/cm

(b)
Current Through SCR 9 during the Commutation Interval

(0716)

Figure 4.15 Clamp SCR Voltage and Current Waveforms during the Commutation Interval

In Figure 4.15, the rate at which the current increases in SCR9 is determined by the leakage inductance of winding T1C and the voltage difference between winding T1C and the propulsion battery voltage. The rate at which the current decreases is determined by the magnetizing inductance of winding T1C and the propulsion battery voltage. The discontinuity in the current waveform of Figure 4.15 coincides with the renabling of the main bus thyristor devices.

The voltage and current stresses on a main thyristor (SCR's 1-6) are illustrated in Figure 4.16 during six step operations at 4000 RPM. During the 180° conduction period of each SCR, the impact of the bus commutation is visible in both the voltage and current waveforms. The voltage spikes appearing on the device are caused by the cycling of the commutation circuit.

Similarly, the voltage and current waveforms of a main thyristor are illustrated in Figure 4.17 during PWM operation. For this figure, the machine is operating at 2000 RPM in the first quadrant. The triangle-sine frequency ratio in the voltage modulator is 9. Again, the impact of bus commutation during PWM operation is clearly visible in the device current waveform as a series of current waveform discontinuities of approximately 100μs duration.

4.6 Commutation and Gating Logic

The sequential bus commutation requirements of the Gould inverter topology requires the commutation logic to interpret the voltage modulation circuit gate drive logic waveforms. A computing circuit approach was elected whose inputs included turn-off or commutation requests from both the top-bus and bottom-bus groups of main thyristors and the present polarities of the commutation circuit capacitors. The polarities of these capacitors indicates whether the top or bottom bus is ready for commutation. A dc or battery overcurrent signal completes the list of commutation logic circuit input signals. A functional diagram of the logic system is illustrated in Figure 4.18. The output of the logic block directly controls the gating of the commutation thyristors SCR7 and SCR8. The logic truth table is contained in Table 4.4. The electrical schematic is contained in Appendix IV.

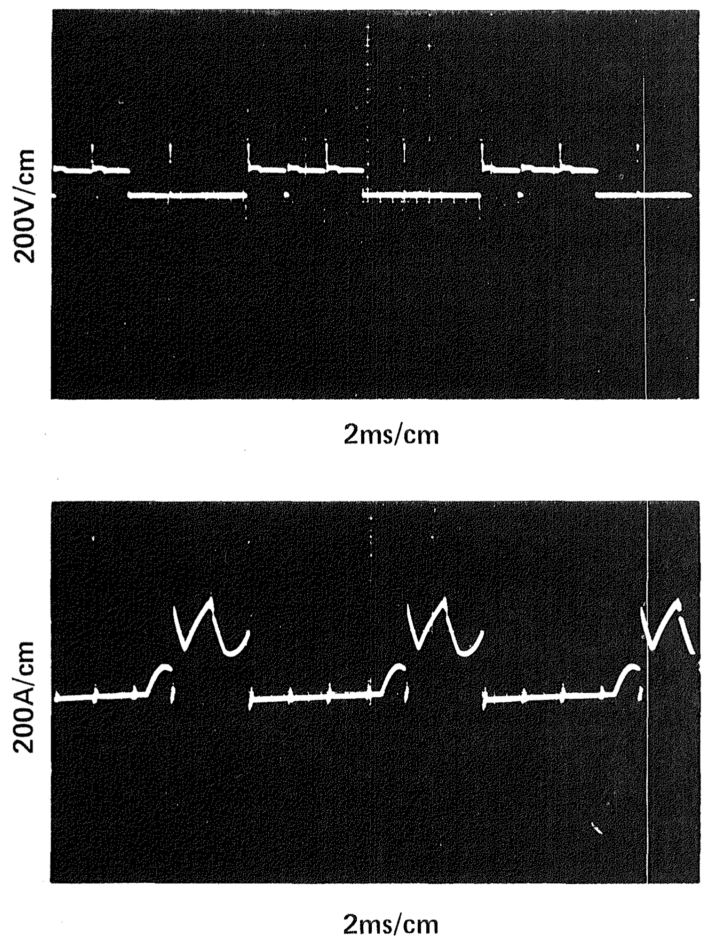
TABLE 4.4

COMMUTATION CIRCUIT TRUTH TABLE

LOGIC INPUTS	TOP BUS REQUEST	1	0	1	0	X	X	X
	BOTTOM BUS REQUEST	0	1	0	1	X	X	X
	OVERCURRENT	0	0	0	0	X	1	1
COMMUTATION STATUS	BUSY COMMUTATING	0	0	0	0	1	0	0
	TOP BUS READY	1	0	0	1	X	1	0
	BOTTOM BUS READY	0	1	1	0	X	0	1
OUTPUTS	GATE SCR 7	1	0	01*	10*	X	1	0
	GATE SCR 8	0	1	10*	01*	X	0	1

* indicates two sequential commutations

X = Don't care



(a)
Voltage Across a
Main Thyristor during
Six - step Operation
f_{ex} = 131.6 Hz

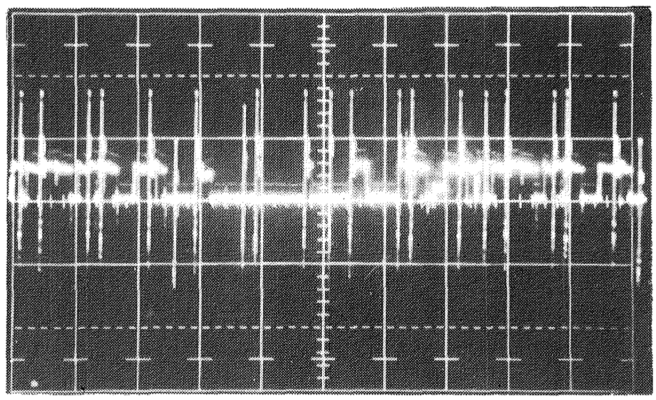
f_r = 4000 RPM

(b)
Current Through
a Main Thyristor during
Six - step Operation

(0717)

Figure 4.16 Main Thyristor Voltage and Current Stresses during Six-Step Operation

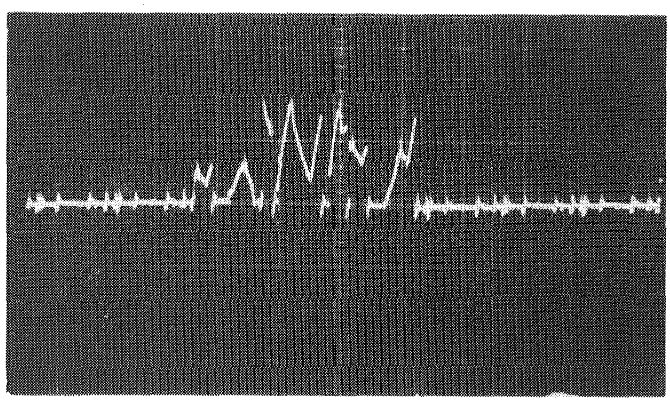
200V/cm



2ms/cm

(a)
Main Thyristor
Voltage Stress,
f_{ex} = 66.6 Hz
n = 9
f_r = 2000 RPM

200A/cm



2ms/cm

(b)
Main Thyristor
Current, PWM
Operation

Instants of Zero Current are caused by Buse Commutation

(0718)

Figure 4.17 Main Thyristor Voltage and Current Stresses during PWM Operation

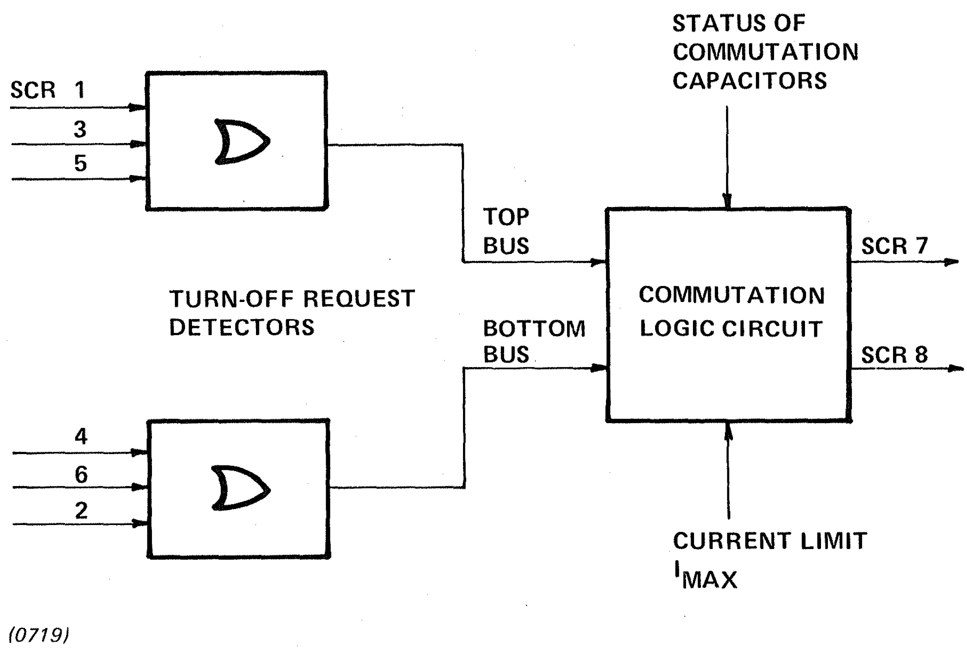
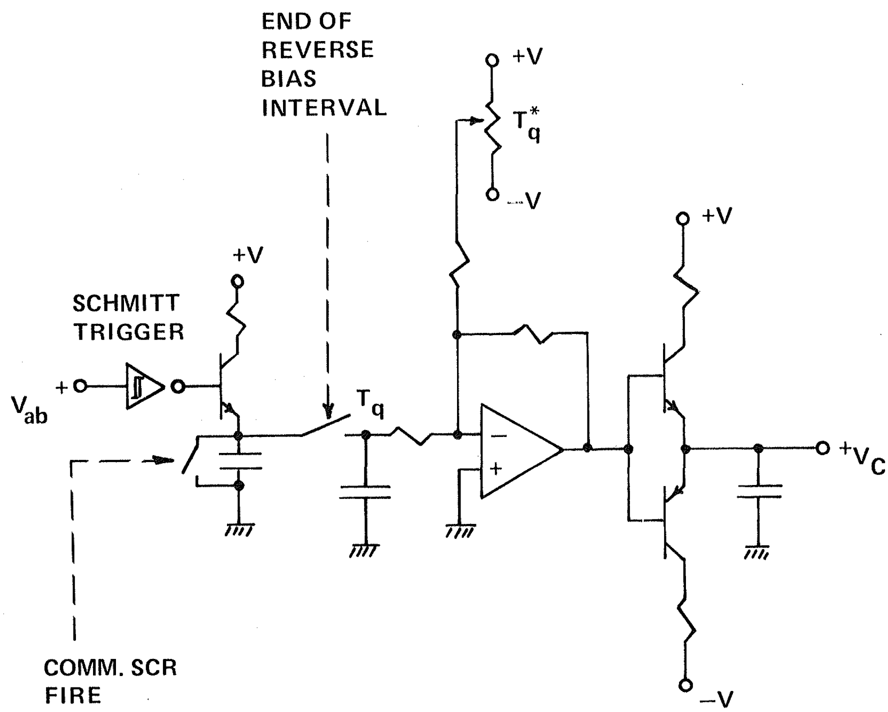


Figure 4.18 Commutation Sequencer Block Diagram

The control of the clamp SCR's, SCR9-10, is assigned to the commutation voltage control logic. As discussed in Section 3, the clamp SCR's are used to control the energy stored in the commutation capacitors. Figure 4.19 is a simplified schematic of the control circuitry for gating SCR9, 10. The circuit becomes enabled after the initiation of the commutation event as defined by the gating of SCR7 or SCR8. The time the main bus SCR's are reverse biased is compared to the desired reverse bias time. The error signal is used to increase or decrease the commutating voltage of the commutation capacitors.

When the desired voltage is achieved, the clamp thyristor which is forward biased is gated into conduction, effectively preventing the commutation capacitor from charging up to higher voltage. Circuit schematics are contained in Appendix IV.

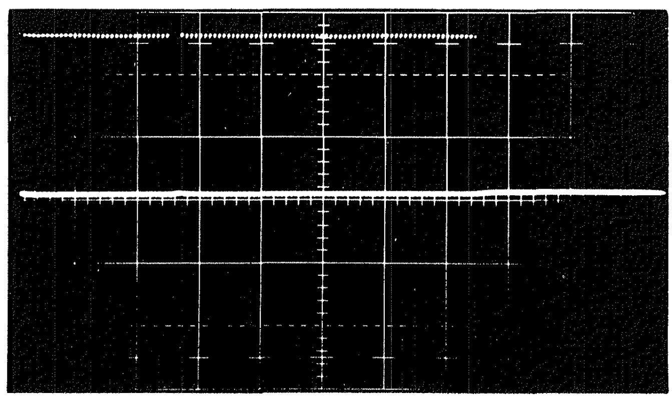
The actual gating signals applied to the main SCR's form a "picket fence" drive. A series of pulses is generated with a local CMOS oscillator operating at 27kHz. The oscillator duty cycle is such that gate current flows for 9μs leaving 28μs to reset the gate pulse transformer. A series of pulses is necessary because the machine power factor alters the exact moment when a given main SCR becomes forward biased and can be gated into conduction. Figure 4.20 portrays the series of gate pulses applied to a main SCR during six-step operation. Again, detailed electrical schematics are contained in Appendix IV.



(0720)

Figure 4.19 Commutation Energy Control Circuit Schematic

5V/cm



(0721)

500 μs/cm

Figure 4.20 Gate Oscillator Drive Waveform Six-Step Operation

V. Enclosure Design

5.1 Enclosure Design Approach

The mechanical layout of the controller is divided between two enclosures, one containing the power stage components and one containing the control electronics and logic power suplies. This division allows the control electronics to reside in the controlled environment of the passenger compartment away from the heat generated by the power stage components and from direct contact with the road environment. A moisture resistant enclosure was selected for the power stage to protect these components from road salt, dirt and other potential contaminants.

The two enclosures communicate with each other via twisted wire pairs residing in a flexible conduit. No connectors are used to terminate the conduit in order to avoid connector reliability problems.

5.2 Power Inverter Enclosure

The power inverter enclosure contains the power inverter circuit components, the device snubbers, and the transducers which are used to measure inverter operational parameters. The enclosure itself consists of two major structural parts. The first is an aluminum base extrusion which provides the mechanical rigidity required to hold the inverter components in place and also acts as the main heat exchanger between the inverter components and the ambient air. The second is an aluminum shell which forms the power inverter package sides and top. Figure 5.1a is a photograph of the main aluminum extrusion. The slot in the middle of the enclosure is used for mounting the commutation transformers. Figure 5.1b is a photograph of the component side of the aluminum extrusion. As seen in the photo, the stud type SCR's are mounted in aluminum blocks which are then secured to the aluminum baseplate with a two-part epoxy system. Figure 5.2 summarizes both the mechanical mounting technique and the resulting thermal impedance between the thyristor junction and ambient.

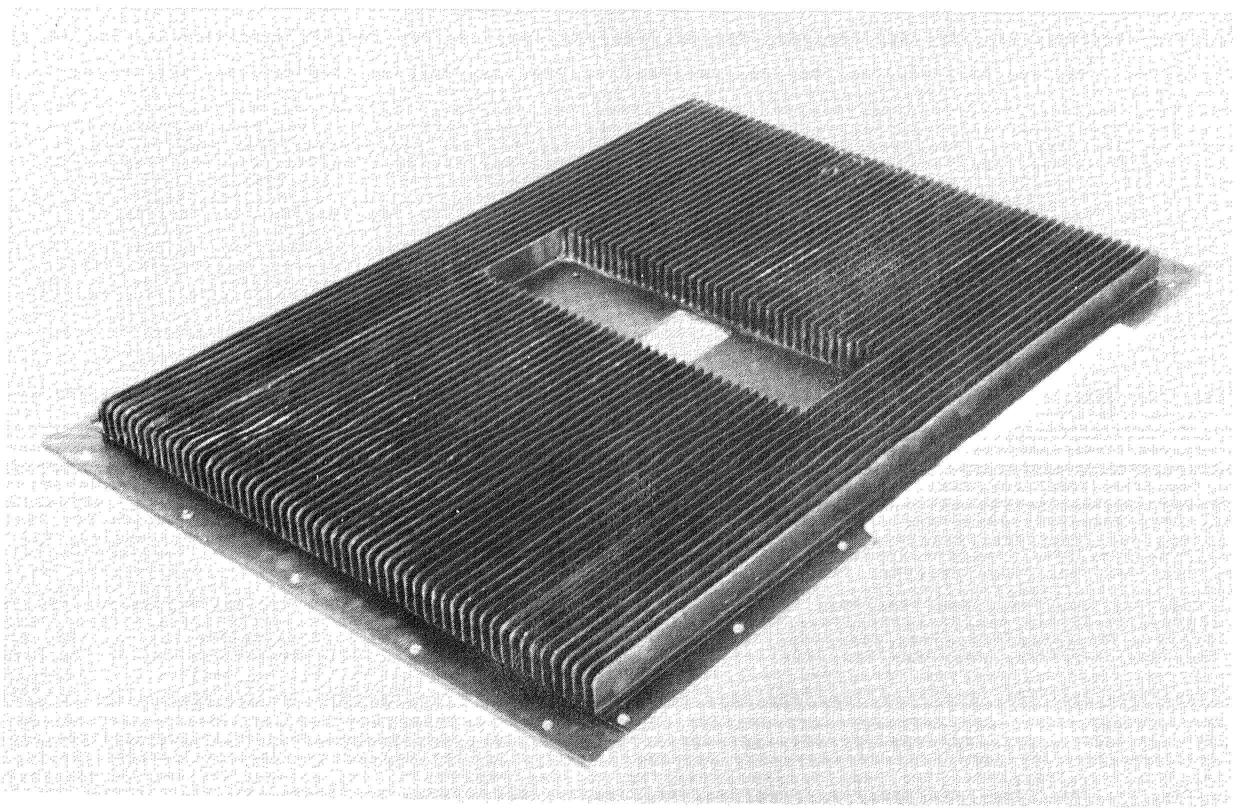


Figure 5.1a Main Aluminum Extrusion

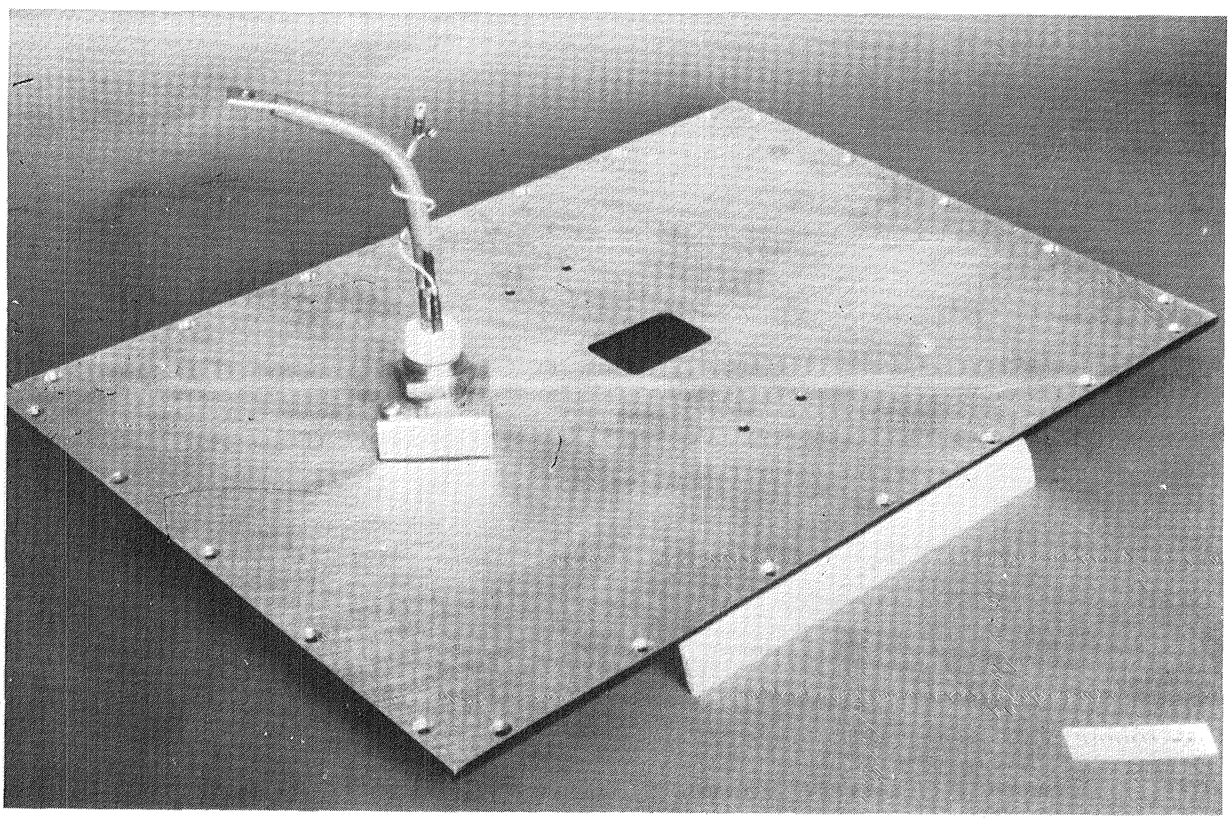


Figure 5.1b Component Side of Aluminum Extrusion

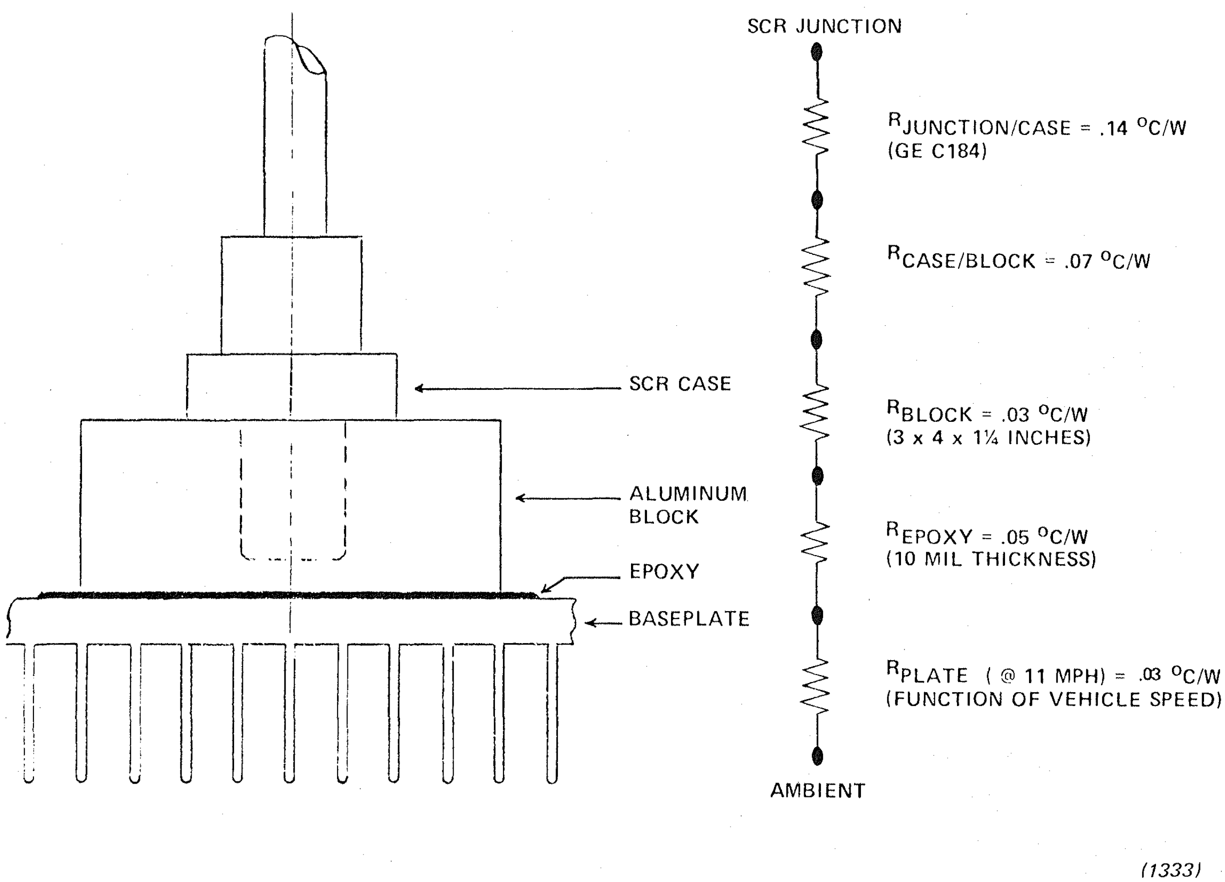


Figure 5.2 SCR Junction to Ambient Thermal Resistance

Several aspects of the controller package design were influenced by the field experience obtained with the fleet of 350 DJ-5E electric vehicles supplied by AMG and Gould to the U.S. Postal Service in 1975. For example, clamping-related assembly and servicing problems associated with hockey-puck thyristors influenced the choice of stud-mounted devices for this controller. Stud mounted thyristors and rectifiers lend themselves well to single-side cooling and require less operator skill during installation.

All of the 16 power semiconductors are mounted in aluminum blocks which in turn are bonded to the base extrusion. Mounting of the aluminum blocks to the finned aluminum extrusion is accomplished using a two-layer epoxy bonding technique. A thin epoxy layer providing high dielectric strength between the device mounting block and extrusion is used in combination with a relatively thick high thermal conductivity layer to fill the gaps between the two surfaces. Using this mounting technique, the SCR junction temperature was calculated for the condition when the loss of main diode and main SCR semiconductor was fixed at 800W. These results are illustrated in Figure 5.3. At vehicle speeds of 10 mph, the SCR junction temperature will be approximately 100°C. This result does make the assumption that a ram air flow of 880 ft/min is available for cooling the main aluminum extrusion. This air flow would be provided by vehicle ram air at the 10mph speed.

The total weight of the power package, 135 lb, is distributed among the components, enclosure, and mechanical hardware. Table 5.1 summarizes the weight distribution among the power inverter components. Approximately half of the total weight is contained in the aluminum base extrusion, mounting blocks, and enclosure.

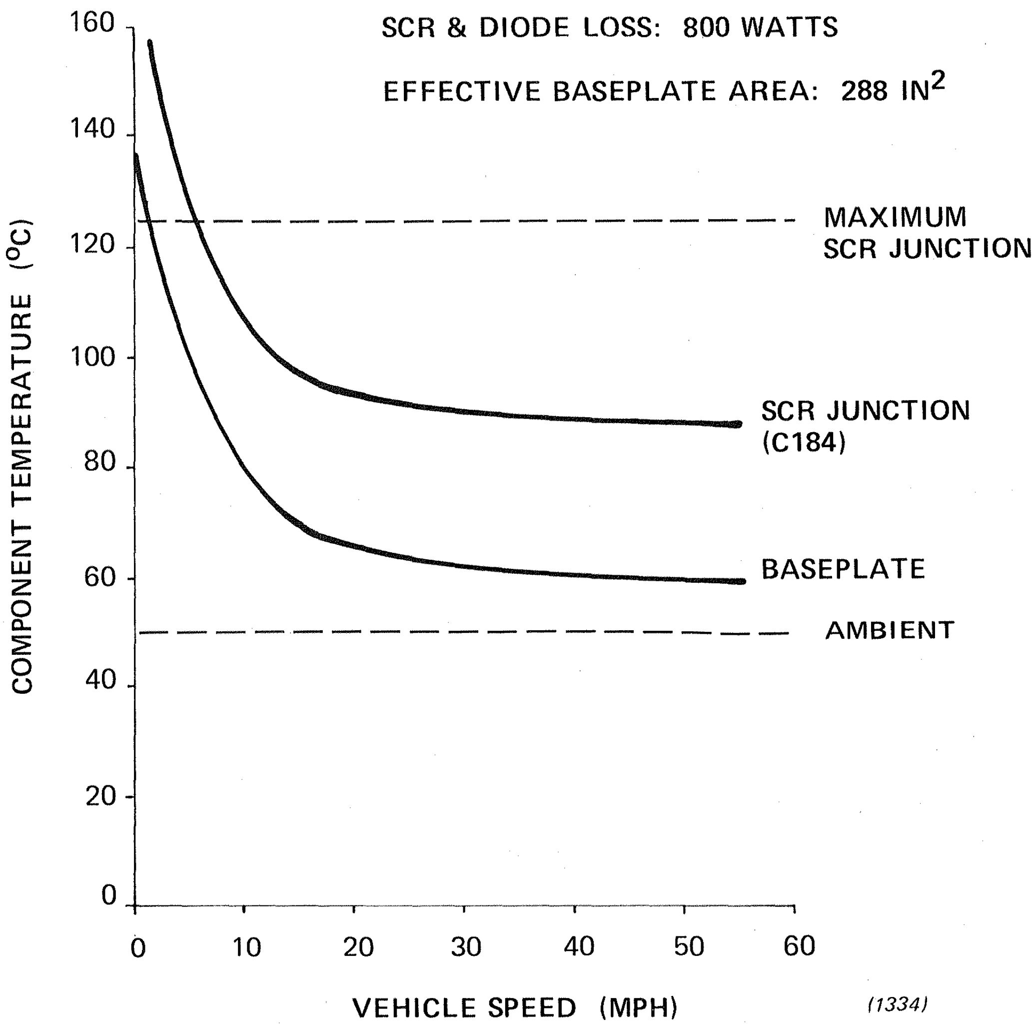


Figure 5.3 SCR Junction Temperature vs. Vehicle Speed

TABLE 5.1

AC CONTROLLER PACKAGE - PARAMETERS

- PROTOTYPE SIZE (POWER UNIT)
  28 x 21 x 8 inches

- POWER UNIT WEIGHT

ALUMINUM BASEPLATE	26 LBS.
ALUMINUM BLOCKS	24
ALUMINUM ENCLOSURE	14
FILTER CAPACITORS (14)	16
COMMUTATION TRANSFORMERS	15
SCRS (10) and DIODES (6)	8
COMMUTATION CAPACITORS (4)	4
SCR GATE DRIVE BOARD	3
BUS BARS	3
CABLE	8
HARDWARE and MISC.	14
	135 LBS.

terminals of the propulsion battery and the average battery current. The measured first quadrant controller efficiency is illustrated in Figure 6.4. This figure contains lines of constant controller efficiency plotted in the operating torque-speed envelope.

For operation in the fourth quadrant, the definition of controller efficiency is the inverse of the motoring definition, that is

$$\eta^{IV}_{controller} = \frac{P_{battery}}{P_{controller}} \qquad [6.3]$$

It should be noted that this definition is only valid if the power delivered by the battery is negative, $P_{battery} < 0$. This distinction has been made to avoid efficiency definition ambiguity for the case when power is being absorbed by the controller from both the motor and the battery. This occurs when the fixed controller losses are greater than the regenerative power delivered by the motor, to the controller. The fourth quadrant regenerative efficiency of the controller is illustrated in Figure 6.5.

Since the power flow between the controller and motor consists of multiplying non-linear voltage and current waveforms, a comment regarding the performance of the Ohio-Semitronics wattmeter is appropriate.

The technical specifications of the wattmeter are impressive; accuracy to 0.5% FS and a bandwidth of 5kHz. Since it is difficult to generate a non-sinusoidal waveform for calibration, the high frequency accuracy of the meter is difficult to verify. During the test program at Gould, the wattmeter provided consistent and repeatable data which seemed reasonable when compared with the precise mechanical power measurement and the battery power measurement. The accuracy of the wattmeter in our opinion is ±2% of reading.

TABLE 5.2

AC CONTROLLER PACKAGE - LOGIC UNIT

- SIZE 11 x 10 x 7 inches

- WEIGHT

LOGIC POWER SUPPLY	10 LBS
LOGIC BOARDS	3
ENCLOSURE	3
HARDWARE and MISC	2
	18 LBS

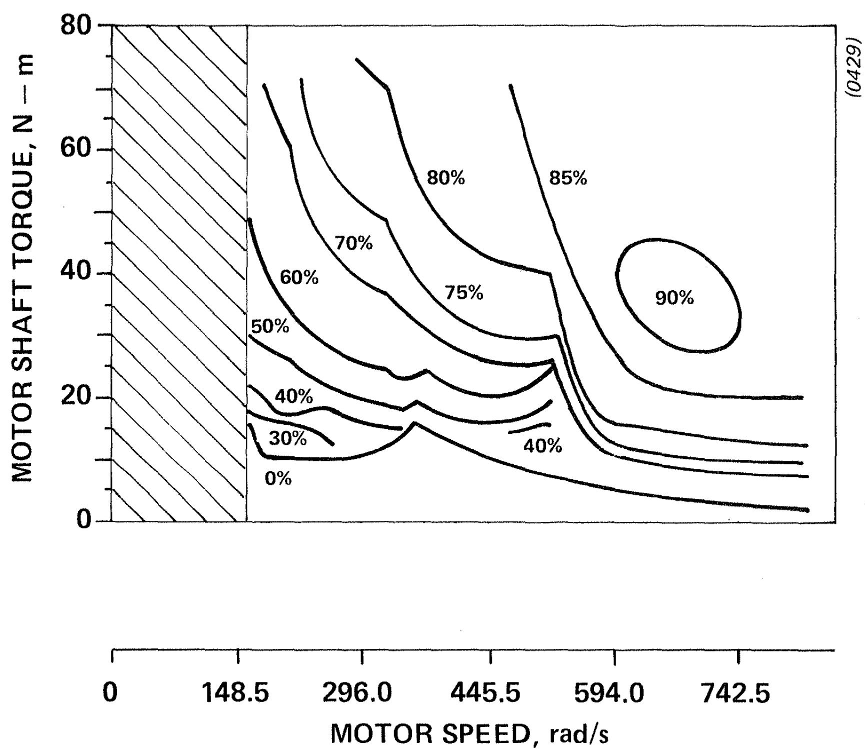


Figure 6.5 SCR Controller Efficiency Data — 4th Quadrant Operation

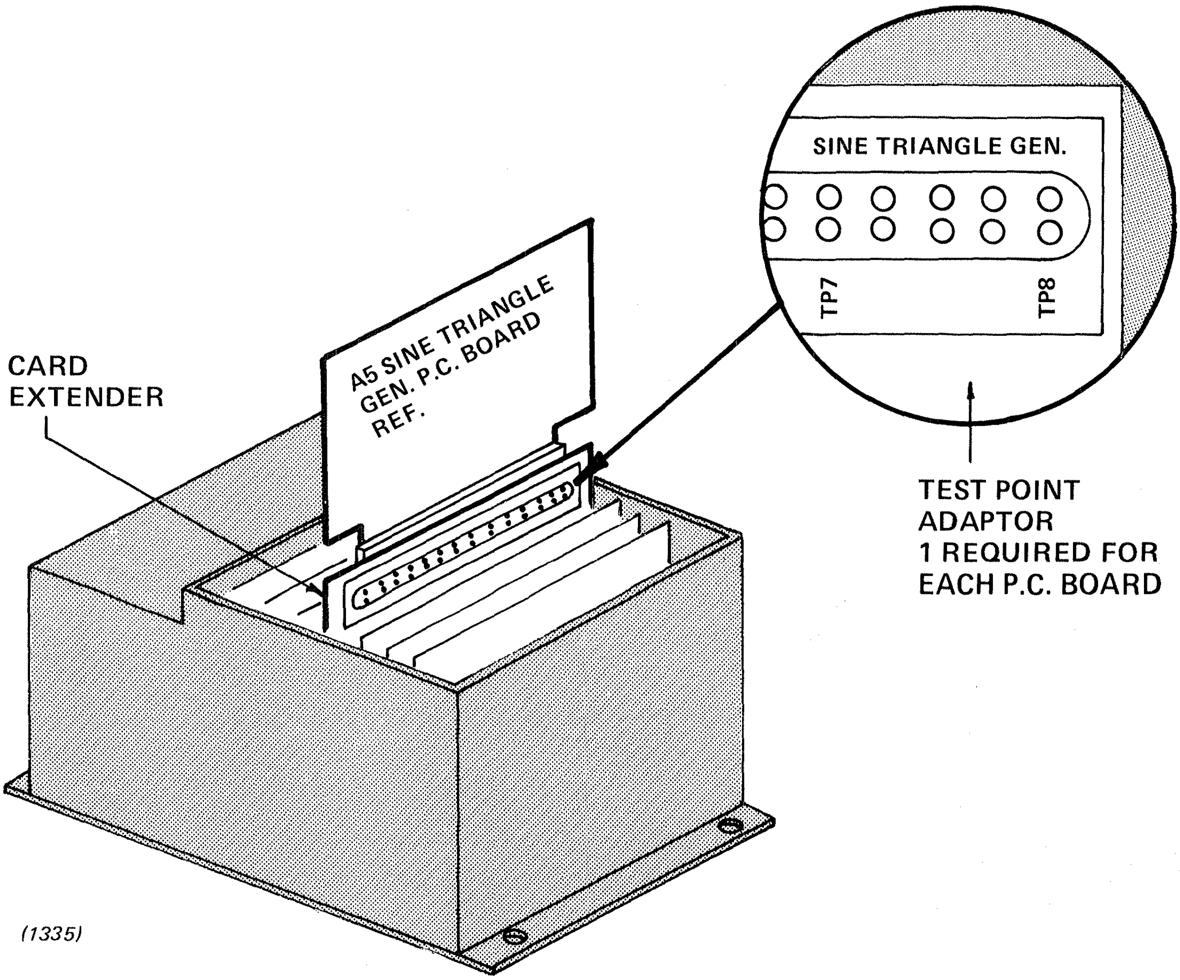


Figure 5.5 AC Controller Logic Unit Diagnostics

VI. Motor Controller System Performance

6.1 Testing Methods

This section discusses the measured motor-controller performance. Motor phase currents generated by the inverter for discrete operating modes are presented as well as the resulting mechanical power produced at the shaft of the induction motor. The mechanical dimensions and weights of the motor-controller system are tabulated to describe the system's physical parameters.

The measurement of the mechanical power produced at the shaft of the induction motor was obtained by loading the motor on a motoring dynamometer. A motoring dynamometer was required to provide both first and fourth quadrant loads at the shaft of the induction motor. First and fourth quadrant loads correspond to positive shaft torque and speed (vehicle motoring), and negative shaft torque and positive speed (regenerative braking), respectively. Figure 6.1 is presented to illustrate the four available load quadrants. Operation in quadrants II or III was not a system requirement, although operation in quadrant III is available to propel the vehicle in reverse.

The dynamometer system is illustrated in Figure 6.2. It consists of a GE dc dynamometer (Model 26G71 type TLC2462), a Lufkin gear (Model N600C), and an in-line torque/speed transducer manufactured by Himmelstein (Model MCRT9-02T). The mechanical power at the motor's shaft is the product of the shaft torque and speed, $P^e = T^e \omega^r$. The torque transducer is designed to measure 220 N-m full scale with an accuracy of 0.1% full scale. Speed information is obtained from a 60 tooth tachometer internal to the torque transducer. The specifications for the Himmelstein equipment are included in Appendix VI.

The electrical power delivered by the controller to the motor was measured with a 3-phase wattmeter manufactured by Ohio Semitronics. This wattmeter employs Hall sensors to measure both the individual phase currents and to compute the power in each of the three motor phases. Technical specifications for the wattmeter are also included in Appendix VI.

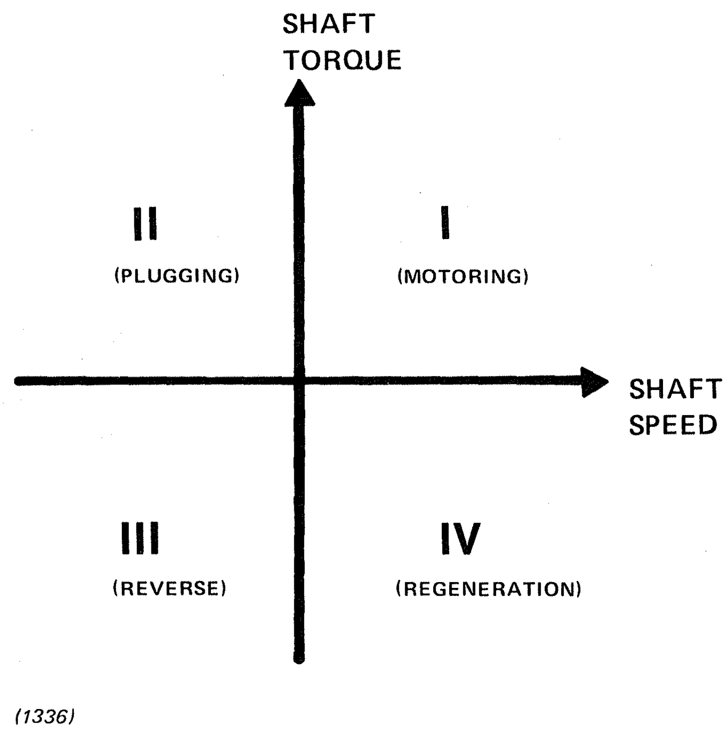


Figure 6.1 Motor Load Quadrants

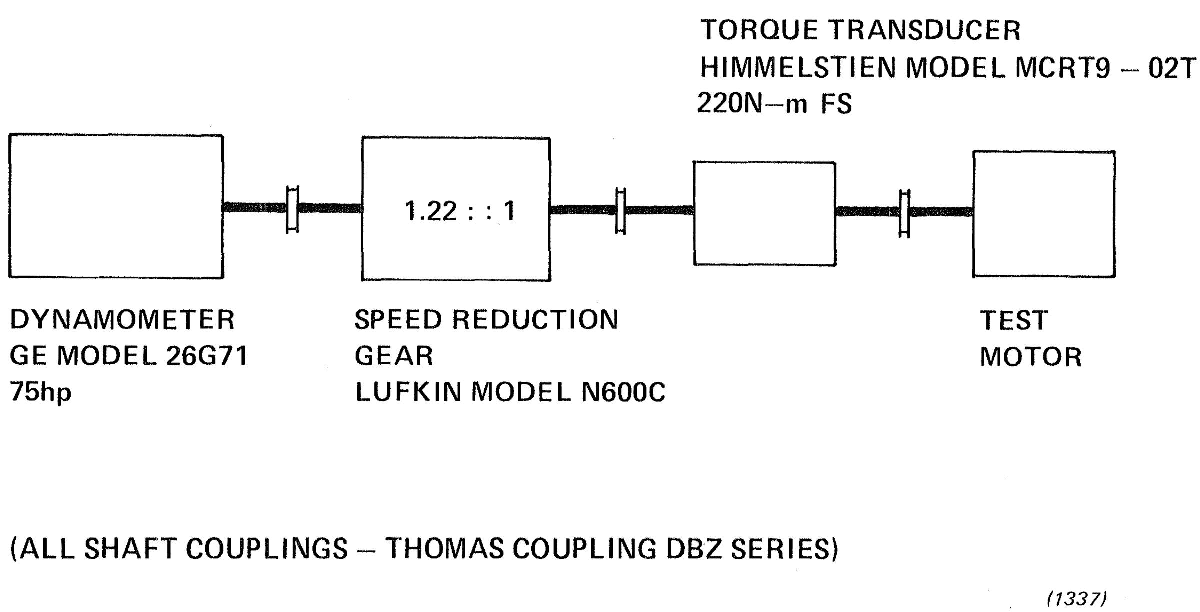


Figure 6.2 Motoring Dynamometer System Mechanical Schematic

Power delivered by the propulsion battery was measured with a Bell current meter (Model 103) and an integrating 3-1/2 digit Fluke voltmeter, their product representing the average battery power flow. This approximation is valid because of the low ac ripple battery voltage.

6.2 Controller Torque-Speed Operating Envelope

The maximum torque that the ac controller-motor system can produce is limited either by the RMS current rating of the controller thyristors or the commutating energy of the auxiliary thyristor-LC circuit. These limits imply a maximum controller operating temperature and a maximum peak battery or controller current. In the controller, the battery current is measured with a Hall current transducer and compared to a predetermined maximum current. This limit represents the maximum commutation capability of the commutation circuit. When that limit is exceeded, the main thyristors in the controller are commutated off and the voltage applied to the motor is decremented to reduce the main thyristor current. This event occurrence is indicated by the current limit LED on the front panel of the controller logic package and primarily determines the maximum torque envelope of the controller. At high speed, when the motor-controller system is operating in the constant horsepower regime, the limiting factor is not the torque capability of the machine but the integrity of the shaft speed transducer or tachometer signal. This limitation is discussed in Section 6.6 of this report and is designed to limit the maximum shaft speed to 816 rad/sec (7800 RPM).

The maximum torque limits of the controller, determined by the current limit criteria when operating from a 120V nominal propulsion battery, is illustrated in Figure 6.3 and tabulated in Table 6.1.

As illustrated in Figure 6.3, shaft torques of 64 N-m are available at stall and the system generates peak shaft torques of 100 N-m at shaft speeds of 315 rad/sec. The dip in the torque speed envelope at 259 rad/sec in Figure 6.3 is due to interaction of the PWM algorithm and the commutation circuit notches discussed in Section 3.3. At this operating point, the commutation circuit is significantly modifying the requested voltage waveform applied to

TABLE 6.1

MAXIMUM TORQUE-SPEED LIMITS
1ST QUADRANT OPERATION

MOTOR TORQUE (N-m)	(ft-lb)	MOTOR SHAFT SPEED (rad/S)	(RPM)
64	(47.2)	0	(0)
86.6	(63.81)	54.6	(521)
85.4	(62.9)	106.2	(1014)
97.0	(71.5)	157.1	(1500)
98.6	(72.7)	210.9	(2014)
65.2	(48.1)	259.4	(2477)
101.0	(74.5)	315.0	(3008)
76.8	(56.6)	367.5	(3509)
62.0	(45.7)	419.7	(4008)
54.6	(40.3)	471.2	(4500)
46.0	(33.9)	524.6	(5010)
38.8	(28.6)	581.4	(5552)
33.0	(24.3)	622.6	(5945)
27.0	(19.9)	683.2	(6524)

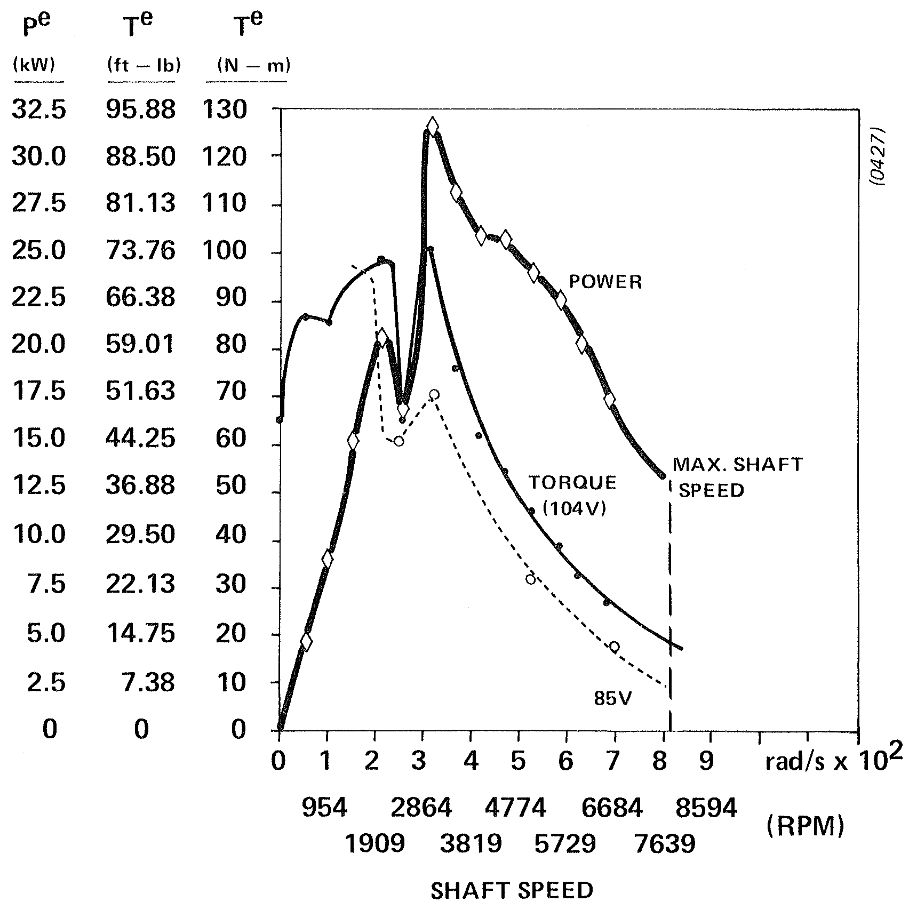


Figure 6.3 Motor/Controller Torque Speed Envelope — 1st Quadrant

each motor phase. Since the spectral energy is no longer closely confined to the fundamental frequency, harmonic currents in the motor are produced which exceed the selected dc current limit. The comutations introduced by the high stantaneous bus currents further degrade the voltage waveform quality until the transition regime is complete. This transition is indicated by a change in the carrier fundamental frequency ratio as discussed in Section 4.

6.3 Calculated System Efficiency

Controller Efficiency

Of special interest in electric vehicle power trains is the electrical to mechanical energy conversion efficiency as well as the conversion efficiency of the ac controller alone. These efficiencies directly affect the range of an electric vehicle and can be measured in both the motoring mode of operation and the regenerative mode of operation, which is permissible at motor shaft speeds above approximately 125 rad/sec.

The efficiency of the controller when operating in the first quadrant, delivering positive torque, is defined simply as:

$$\eta^{I}_{controller} = \frac{P_{controller}}{P_{battery}} \times 100 \qquad [6.1]$$

$P_{controller}$, the electrical power delivered by the inverter to the motor, was measured with the use of the Ohio-Semitronics 3Ø watt meter discussed earlier. This instrument performs the calculation

$$\frac{1}{T} \int_{0}^{T} (v_{AN} i_A + v_{BN} i_B + v_{CN} i_C)\, dt \qquad [6.2]$$

and outputs a dc voltage which is proportional to the result. The battery power was calculated from the product of the average voltage measured at the

5.3 Control Logic Enclosure

The logic enclosure contains an array of eight printed circuit boards and the logic power supplies described in Section 4. As discussed, the communication between the logic package and the power inverter is via a 3/4" flexible conduit. The enclosure itself is divided into two sections, one for the power supplies and the second which forms a card nest for the logic system. Table 5.2 summarizes the weight distribution of the logic enclosure components and the physical size of the unit.

The front panel of this enclosure contains LED's to indicate the controller's status and a key switch for activating the controller. The enclosure also has two "D" type connectors to accommodate the accelerator/brake potentiometer assembly/console selector and the tachometer cable connection. Figure 5.4 is a photograph of the logic enclosure in which the logic printed circuit boards are visible.

Controller diagnosis is simplified by the functional modularity of the printed circuit boards. The eight boards each contain discrete circuit functions which can be tested independently.

The eight circuit boards contain the following controller circuitry:

1. Micro computer (A8)
2. Digital-Analog I/O (A7)
3. Transducer Signal Conditioning (A6)
4. Slip Frequency Circuitry (A5)
5. Sine-Triangle Generator (A4)
6. Main Thyristor Gating Logic (A3)
7. Commutation and Clamp Thyristor Logic (A2)
8. Gate Drive Amplifiers (A1)

Access to all inter-circuit board connection is available via a card extender as pictured in Figure 5.5 or at the printed circuit card nest backplane.

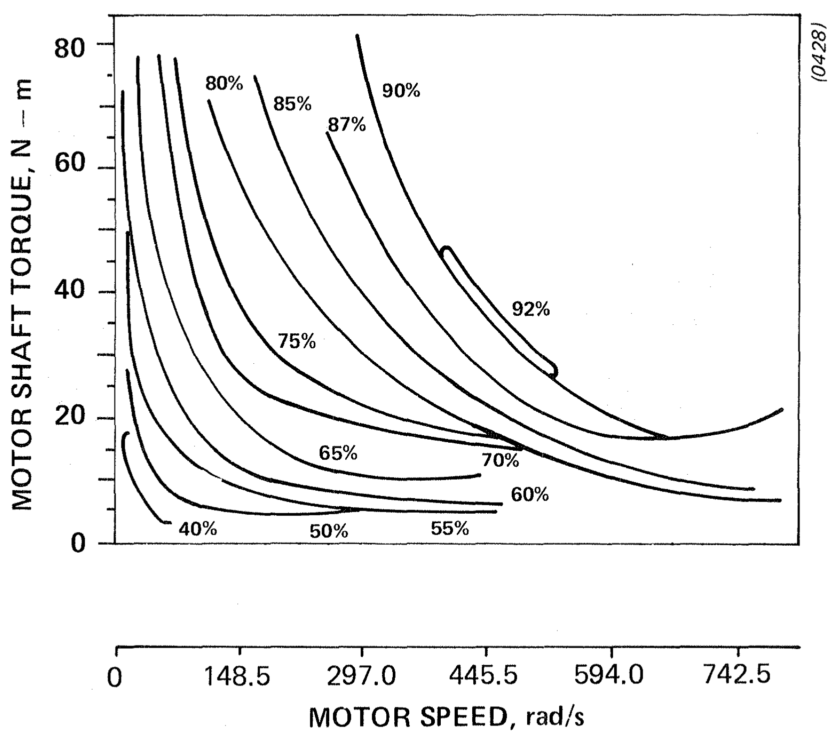


Figure 6.4 SCR Controller Efficiency Data – 1st Quadrant Operation

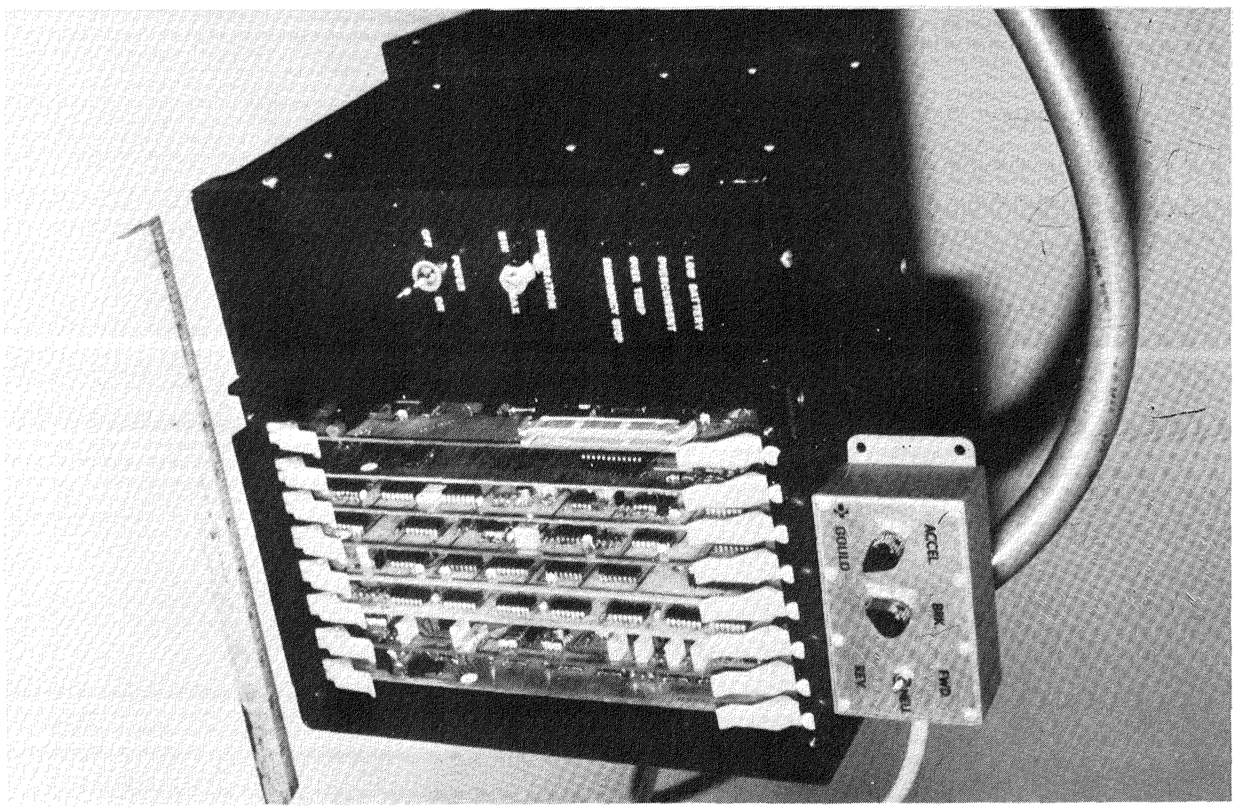


Figure 5.4 Control Logic Enclosure (Printed Circuit Boards Visible)

Motor-Controller Efficiency

A similar definition to those previously discussed is employed to calculate the efficiency of the entire electrical to mechanical conversion system. Since the battery power and shaft power can be each accurately measured, the efficiency of the ac system consisting of the motor and controller can be acertained to high accuracy, ±1%. The first quadrant efficiency of the motor controller system is defined by

$$\eta^{I}_{system} = \frac{P_{shaft}}{P_{battery}} \times 100 \qquad [6.4]$$

Again, a similar definition is possible for operation in the regenerative regime, but again for the definition to be valid, the battery power, $P_{battery}$, must be < 0. This insures that the direction of the power flow is unidirectional throughout the system.

$$\eta^{IV}_{system} = \frac{P_{battery}}{P_{shaft}} \times 100 \qquad [6.5]$$

The calculated system efficiency in the first quadrant is plotted as a function of both torque and speed in Figure 6.6a, which also includes the vehicle load line for level ground. As can be seen in Figure 6.6a, system efficiency approaches 70% at a vehicle speed of 45mph. The peak system efficiency, 80%, is obtainable when the controller is delivering near peak power, approximately 26kW. This result is expected since at that operating point the fixed losses of the controller become the smallest fraction of the power processed by the motor-controller system. Figure 6.6b illustrates the system regeneration efficiency above shaft speeds of 150 rad/s.

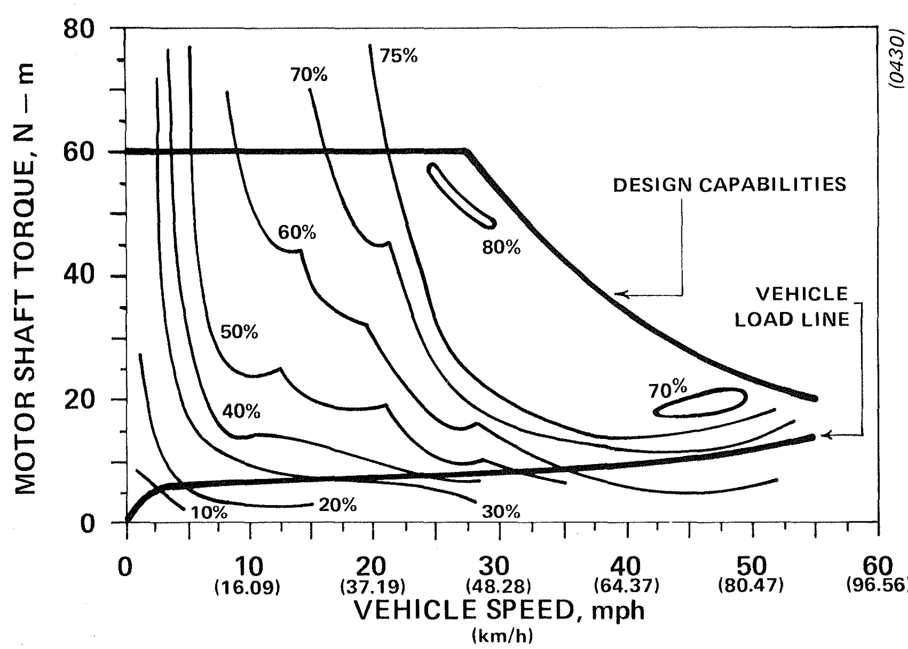


Figure 6.6a Motor/Controller Efficiency Map — Fixed Transmission Ratio

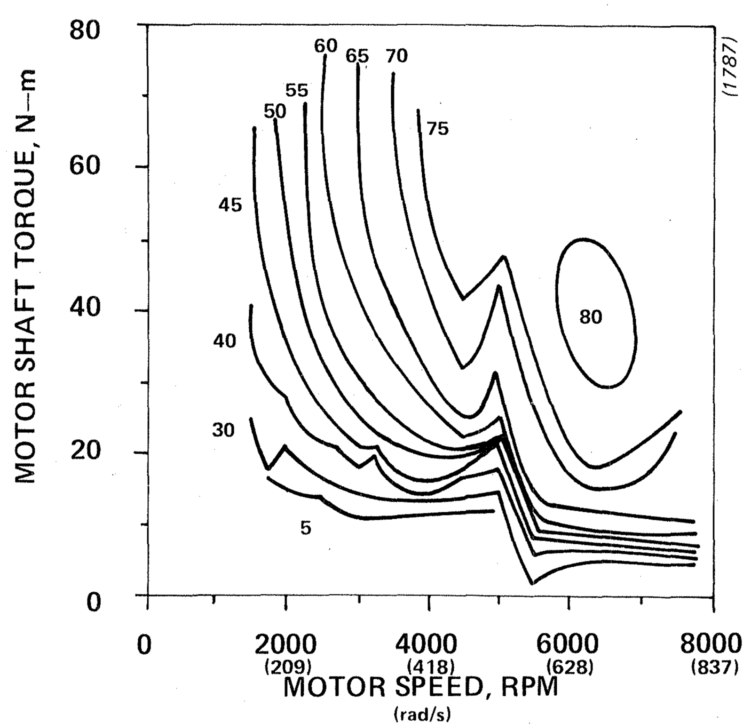


Figure 6.6b System Regeneration Efficiency

6.4 Pulse-Width Modulation Operation

The voltage modulator described in Section IV of this report has several distinct operating modes. These modes result from the selection of discrete triangle-sine frequency ratios as discussed earlier. Since the motor voltage waveforms in the time domain consist only of a series of pulses of magnitude V_{bat}, this section presents the motor voltage waveforms generated by the ac controller in the frequency domain. This data is discussed for discrete motor shaft speeds, each representing a different triangle-sine frequency ratio.

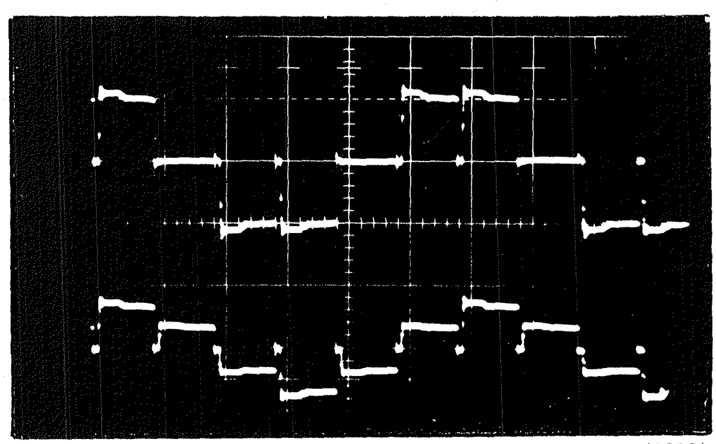
The motor line-to-line and line-to-neutral voltages are shown in Figure 6.7 when the inverter is operating in the "six-step" mode and delivering maximum output voltage. The effects of bus commutation can be clearly seen in Figure 6.7, producing a series of zero voltages intervals or notches which correspond exactly to the duration and occurrance of a commutation event.

The corresponding time domain motor phase current and the frequency domain representation of the motor voltage is shown in Figure 6.8. As seen in 6.8(a), the harmonic spectrum consists only of odd harmonics which are non-multiples of 3, which are suppressed in a 3-phase system. The suppression of the even harmonics is a measure of the waveform symmetry. As shown in Figure 6.8(a), the even harmonics are approximately -50db below the fundamental voltage component, demonstrating waveform symmetry. Figure 6.8(b) details the resulting time domain motor phase current. The shape of the current waveform is not controllable when the inverter is operating in the six-step regime.

Figure 6.9 shows the high speed PWM operation of the inverter. At this particular operating point, the inverter output voltage is just below the maximum obtainable in six-step operation. In Figure 6.9, the carrier frequency ratio is 9 but not all the triangles are intersecting the excitation frequency sine wave since the modulation index is greater than 1. The generated output voltage in the frequency domain is illustrated in Figure 6.9(a) while the corresponding time domain motor phase current is displayed in Figure 6.9(b). The commutation circuit is commutating each bus 9 times/cycle.

$V^{\ell\ell}$

$V^{\ell s}$



y = 100V/cm

(0690)

x = 1ms/cm

SHAFT SPEED = 5138 RPM

POWER = 15kW

Figure 6.7 Inverter Output Voltage in the "Six-Step" Mode of Operation Showing Bus Commutation Interaction

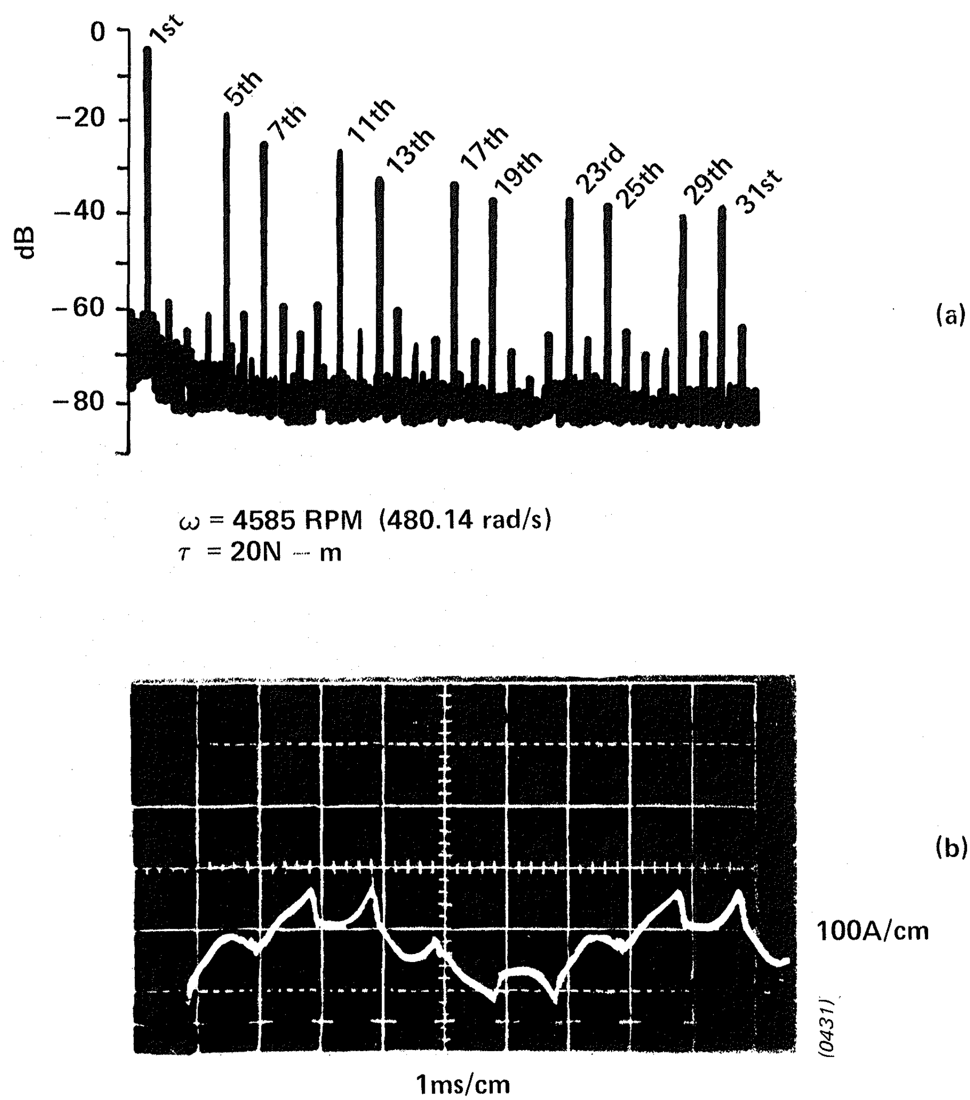


Figure 6.8 (a) Six-Step Voltage Waveform Represented in the Frequency Domain

(b) Six-Step Motor Current in the Time Domain

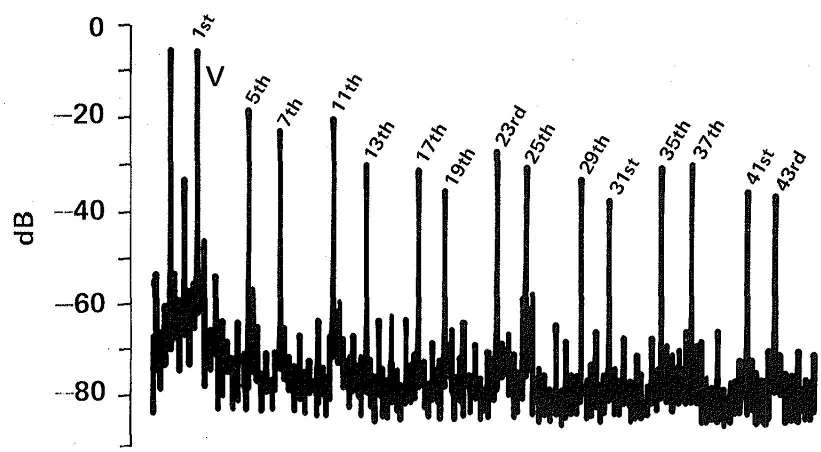
When the modulation index becomes less than one, all triangles intersect the base frequency sine wave and the inverter waveforms undergo a discrete change again. This situation is shown in Figure 6.10. Figure 6.10a contains the frequency domain representation of the inverter output voltage and Figure 6.10b represents the respective motor phase current. Note that the additional intersections have suppressed the 5th, 7th, 11th and 13th harmonics compared with the voltage spectrum illustrated in Figure 6.9(a).

At a still lower excitation frequency, the triangle-sine frequency ratio is increased from 9 to 27. This generates another discrete step in the waveform characteristics. Figure 6.11(a) shows the frequency domain representation of the inverter output voltage for the conditions of $m_i<1$ and the carrier frequency ratio of 27. Figure 6.11(b) shows the corresponding inverter phase current . The effect of the higher carrier frequency ratio is clearly seen in the suppression of harmonics up to the 53rd and 55th. This is the expected result in that the chosen modulation strategy should suppress harmonics below twice the carrier frequency ±1. For a carrier frequency rates of 27, this yields 54±1, the result evident in Figure 6.11(a).

Figure 6.12 illustrates the motor phase current time domain waveform when the modulator is operating with a carrier frequency ratio of 45. The oscillograph was recorded at a motor shaft speed of 245 RPM. The motor voltage represented in the frequency domain is not displayed due to limitations of the measurement equipment.

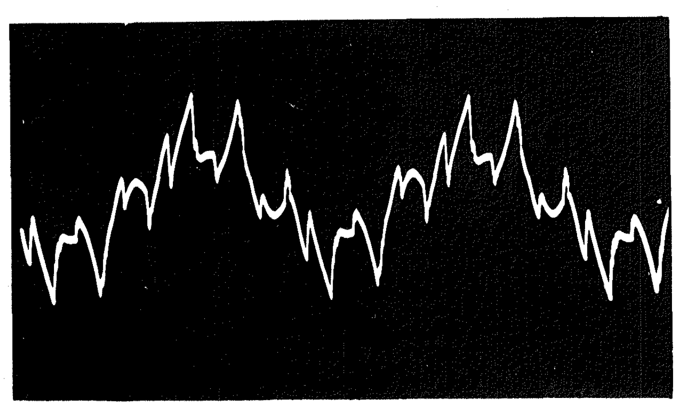
6.5 Thermal Performance

The steady-state capabilities of the motor-controller system are limited by the ambient temperature and the component cooling techniques employed in the package design. Since the motor and controller are designed to be cooled by vehicle ram air, cooling fans were used to simulate the vehicle air flow. The temperature of the controller components were monitored during the testing program to identify thermal management areas of concern which would limit the controller rating.



(a)

ω = 3289 RPM (344.42 rad/s)
τ = 32N – m



I = 100A/cm

(b)

(0432)

2ms/cm

Figure 6.9 (a) PWM Voltage Waveform, Frequency Domain
Triangle Frequency Ratio = 9, $m_i > 1$

(b) Motor Phase Current–Time Domain
Triangle Frequency Ratio = 9, $m_i > 1$

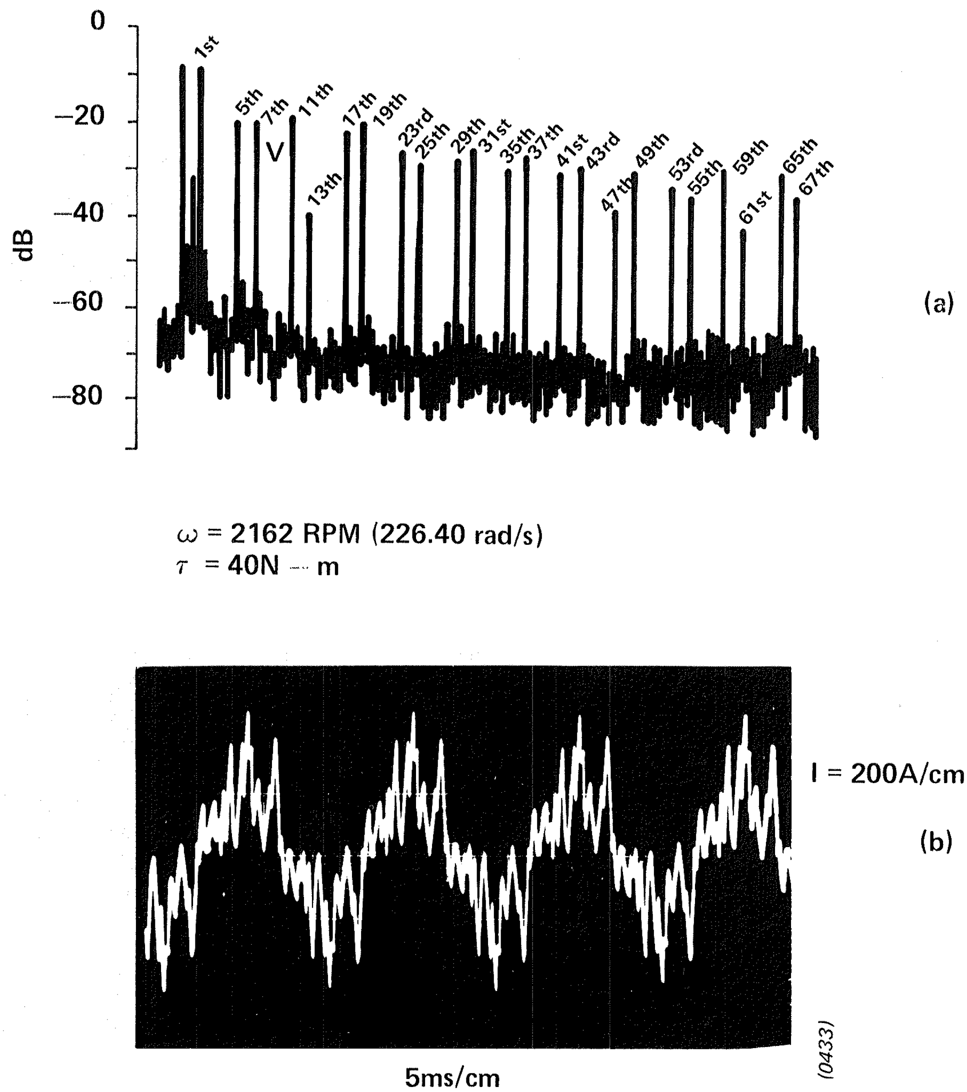
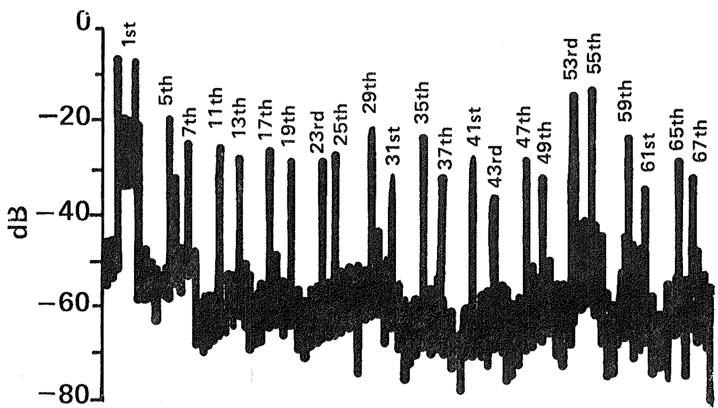


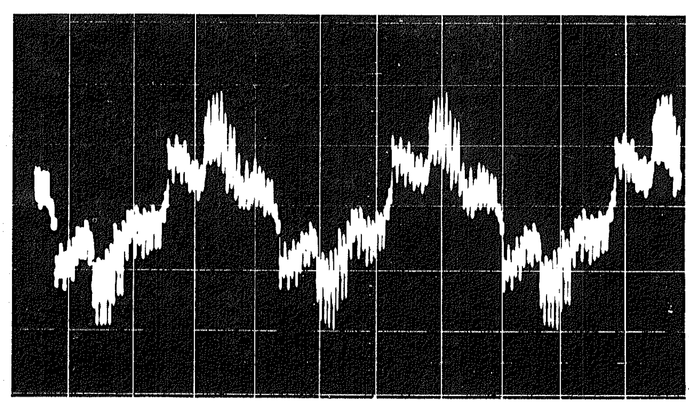
Figure 6.10 (a) PWM Voltage Waveform Frequency Domain Triangle Frequency Ratio= 9, $m_i < 1$

(b) Motor Phase Current–Time Domain Triangle Frequency Ratio= 9, $m_i < 1$



(a)

ω = 776 RPM (81.26 rad/s)
τ = 37N – m



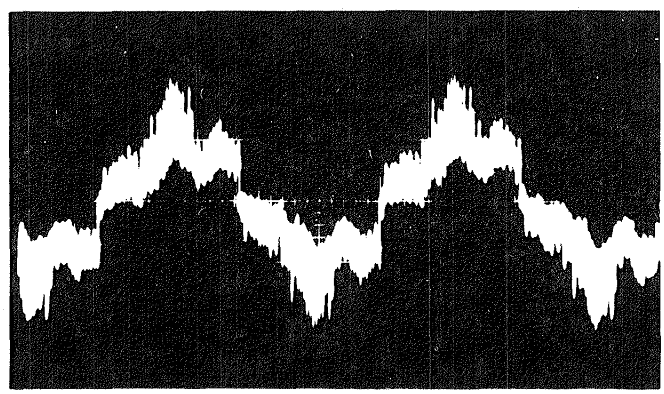
I = 200A/cm

(b)

10ms/cm

Figure 6.11 (a) PWM Voltage Waveform Frequency Domain Triangle Frequency Ratio = 27, $m_i < 1$

(b) Motor Phase Current—Time Domain Triangle Frequency Ratio = 27, $m_i < 1$



ω = 245 RPM (25.66 rad/s)
τ = 42N – m

Figure 6.12 Motor Phase Current--Time Domain
Triangle Frequency Ratio = 45, $m_i < 1$

The blowers which were used to simulate the vehicle ram air were two Dayton Model 2C962A blowers each generating airflow at a rate of 490 CFM. A third blower, Dayton Model 2C989, provided airflow over the frame of the 215 frame induction motor. During the tests, the flow rate was held constant, independent of the operating frequency of the inverter.

During the testing, the temperature of the three types of aluminum SCR mounting blocks were monitored. The maximum temperature rise observed was 30°C, which, when added to the ambient temperature of 25°C, limited the device case temperatures to less than 55°C. These measurements verified the design conservatism of the thermal system. The details of a typical device mounting cross-section are included as Figure 6.13.

The temperature of the commutation capacitors and magnetics was also monitored during the electrical testing phase. The magnetics, which were fabricated to Class H standards, did not exceed 185°C coil temperature. However, it was possible, during extended PWM operation, to trip the thermal protection circuit which sensed the temperature of the commutating capacitors. The upper temperature limit of the commutating capacitor was set to 80°C. During PWM operation, the commutation circuit cycling frequency exceeds that which is required for motoring at 55 mph, the thermal design point. A low loss commutation capacitator, GE type 97F, can be substituted for the 26F style capacitors presently employed to increase the commutation circuit's ability to support extended PWM operation.

6.6 Physical Description

The ac controller-motor system physically consists of three segments: the motor, a control electronics package, and the power inverter package. These are illustrated in Figure 6.14. The weight of each of these components is tabulated in Table 6.2 and equals 270 lb. This weight reflects the controller's design approach which emphasizes component access and serviceability.

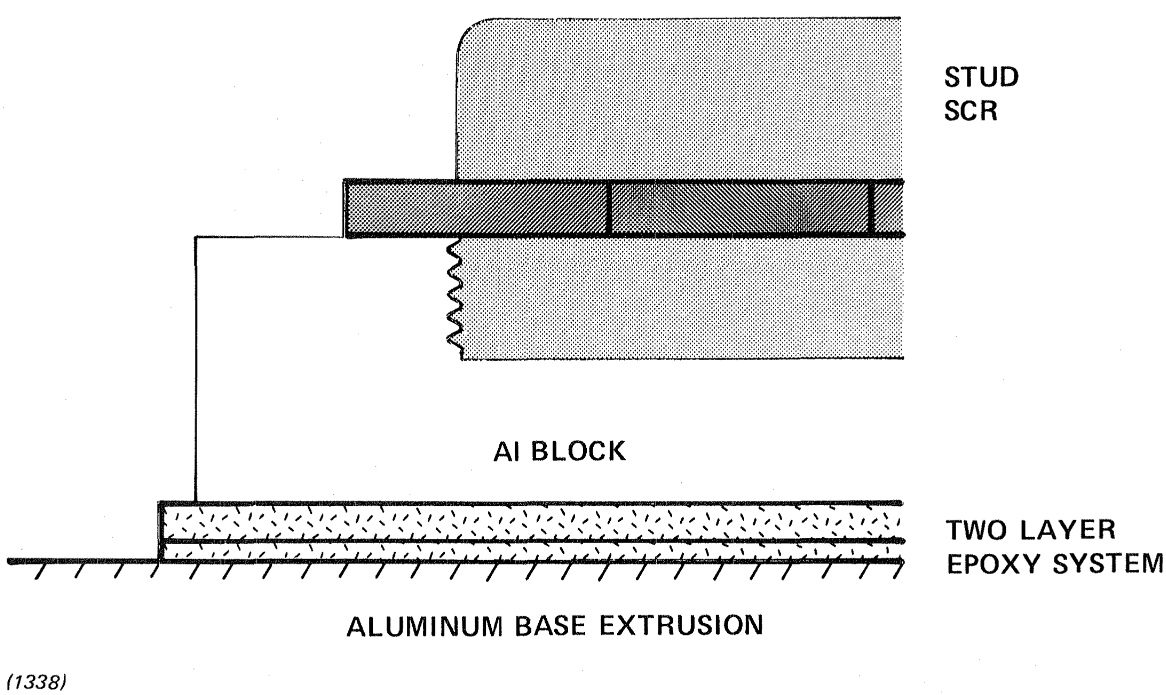


Figure 6.13 Stud Semiconductor Mounting Technique

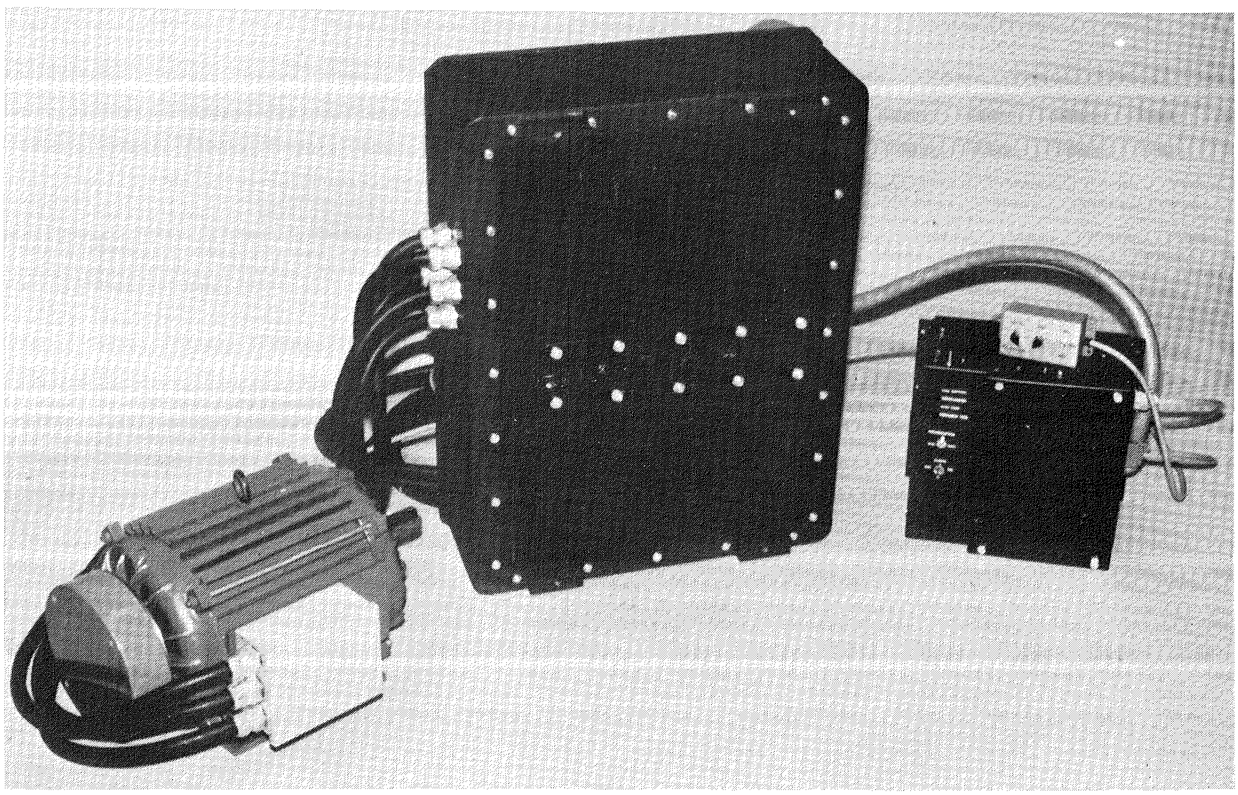


Figure 6.14 Motor- Controller System

The three major components are induction motor (left), the power circuit (center), and the control electronics (right)

The dimensions of the system are also summarized in Table 6.2, with the exact outline of each of the two controller packages illustrated in Figure 6.15 and 6.16 respectively.

Table 6.2

Controller Component Weights/Dimensions (Measured)

	WEIGHT (lbs)	DIMENSIONS
Motor	117 (53.18kg)	NEMA 215TENV
Inverter	135 (61.36kg)	21.5" x 28.5" x 8.75" (54.6cm x 72.4cm x 22.2cm)
Controller	18 (8.18kg)	12" x 11.28" x 8" (30.5cm x 28.7cm x 20.3cm)

The motor construction utilizes class H insulation, rated at 180°C. Although motor coil temperatures did not exceed 140°C, the performance of the optical detector mounted on the motor was affected by high motor ambient temperatures. Reliable tachometer operation at high speed (> 680 rad/s) is only possible when the tachometer enclosure remains below 50°C. This was ensured during the testing phase by not securing the protective tachometer end-bell. The redesign of the shaft speed transducer is an engineering task which should be addressed in the pre-production prototype redesign to increase the reliability of the motor tachometer.

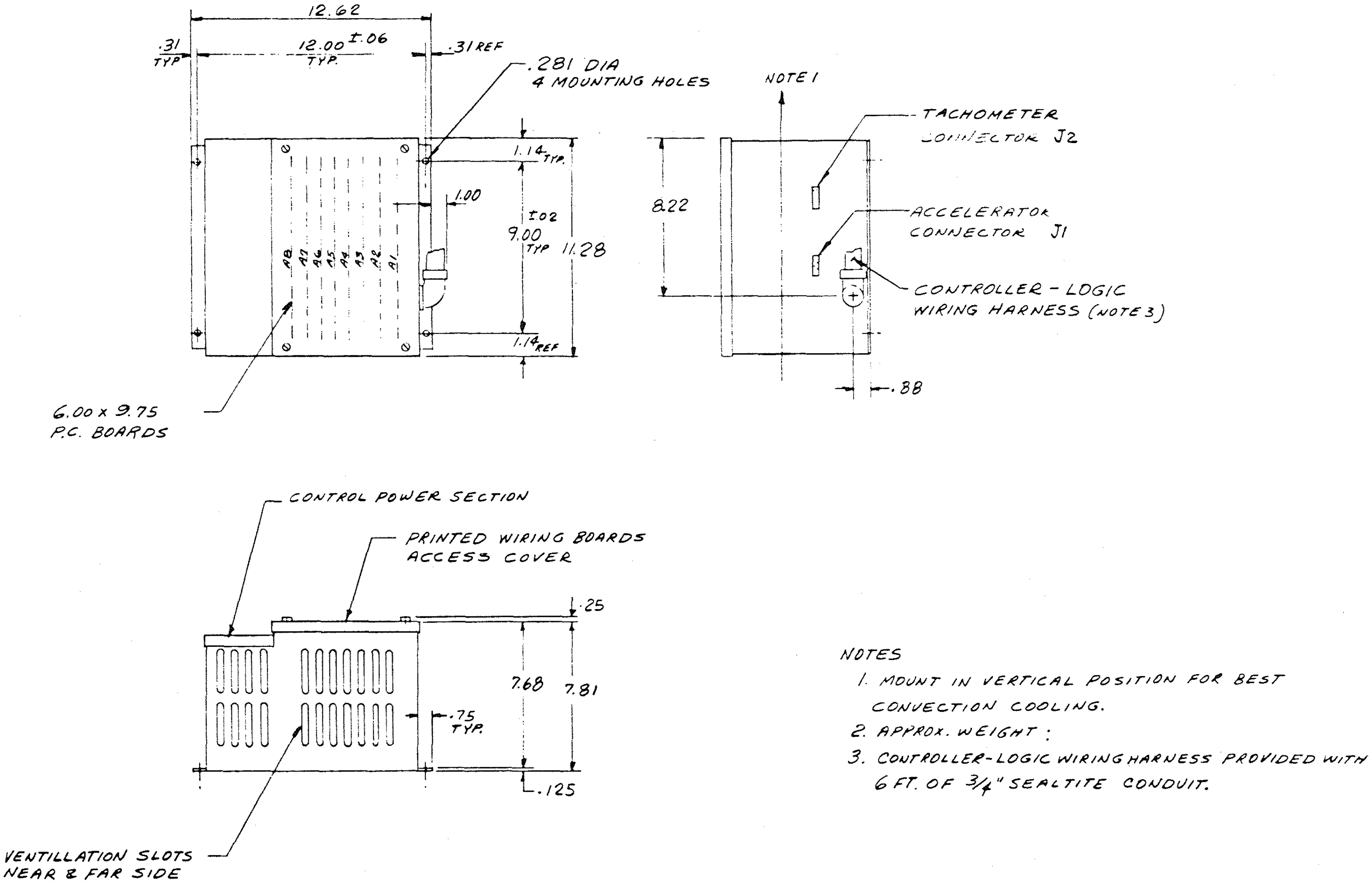
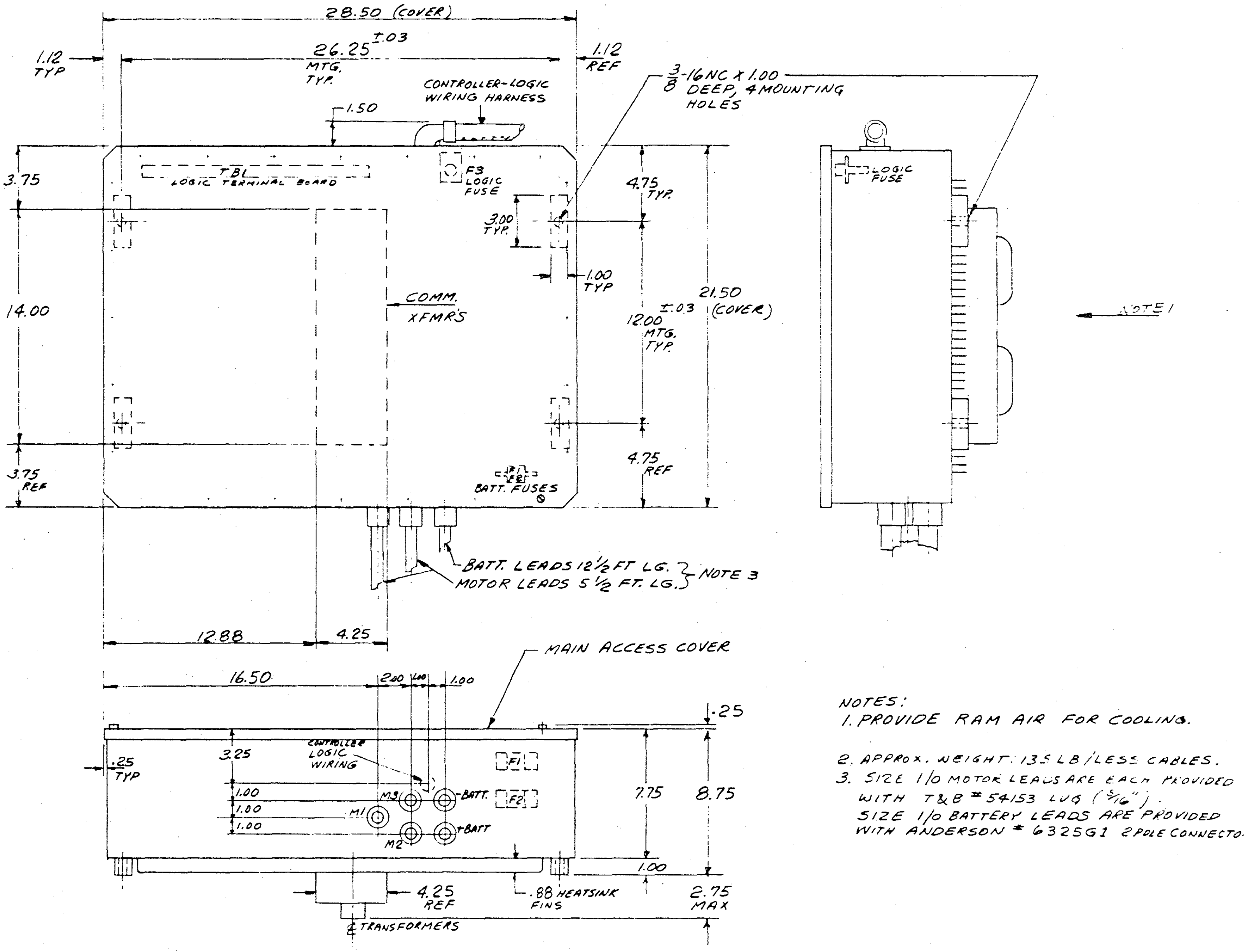


Figure 6.15 Mechanical Outline Drawings of the Control Logic Enclosure



ure 6.16 **Mechanical Outline Drawings of the Power Circuit Enclosure**

VII. Controller Power Scaling and Cost Assessment

The controller developed during the contract period is formally defined as a 10hp controller. Design guidelines are presented in this section to scale the present controller design up to defined power levels of 50 hp. The higher power levels are applicable to heavier passenger vehicles, delivery vans, and trucks in urban service in accordance with the SAEJ227a Schedule D driving cycle. The discussion of the ac controller family and cost assessment is divided into four areas. These include available inverter thyristors, commutation components, packaging impacts, and the motor controller costs.

7.1 Scaled Family Definition

The present ac motor-controller system has a nominal rating of 10 hp derived from the traditional 60 Hz rating of a NEMA 215 size frame induction motor. The actual power capabilities of the motor controller system include a peak rating of 26kW (35hp) and a steady state rating of 11.2 kW (15hp). The scaled family consisting of 20, 30, 40 and 50 hp controllers then represent motor-controller systems having actual peak power capabilities of up to 130 kW. Table 7.1 summarizes the exact controller ratings for the complete family of controllers. The nominal propulsion battery voltage is limited to be less than 300V throughout the controller family.

7.2 Inverter Component Requirements

The inverter components which are affected in a scaling exercise are the main inverter thyristors, the commutation and clamp thyristors, and the commutation capacitors. To determine the feasibility of scaling the original controller design upwards to 50 hp, component specifications were determined as a function of propulsion battery voltage. These specifications were then compared to existing commercially available components to ascertain both price and power capabilities.

TABLE 7.1

AC CONTROLLER FAMILY POWER LEVEL REQUIREMENTS

NOMINAL CONTROLLER/ MOTOR RATING	PEAK POWER RATING (HP)	CONTINUOUS RATING (HP)
10*	35	15
20	70	30
30	105	45
40	140	60
50	175	75

*Existing controller design

Using the analysis described in Section 3.3, the voltage and current ratings of the main inverter SCR's were derived for each member of the scaled family of controllers as a function of propulsion battery voltage. A criteria for determining the suitability of commercial SCR's included both their power capability and turn-off time. A maximum turn off time of 15μs was assumed so that similar scaling techniques could be applied to the commutation circuit components.

Figure 7.1 contains the plot of main thyristor RMS current requirements as a function of battery voltage. Commercially available inverter grade SCR's are included in Figure 7.1. As can be seen, there are no component restrictions related to main thyristor availability if the propulsion battery voltage is greater than 200Vdc.

The commutation circuit thyristor requirements for both the commutation and clamp thyristors must also be derived to determine the availability of commercial devices. Using the analysis presented in Section 3.3 of this report, and fixing the commutation capacitance, inductance and turn-off time requirements to those values selected for the 10 hp design, the requirements of both the commutation and clamp thyristors were derived. These results are illustrated in Figure 7.2, which plots the voltage and current requirements of the commutation SCR and the voltage requirements of the clamp thyristor vs the defined controller rating. As shown in the figure, commutation thyristors are available with turn-off times of 20-30μs and voltage ratings of 1400-1500 volts. By readjusting the commutation transformer turns ratio, the voltage margin on the clamp thyristor can be improved so that there are no scaling restrictions derived from the commutation thyristors.

Commutation type capacitors are commercially available with paper/polypropylene or all polypropylene dielectric materials. The major difference between these two dielectric materials is the much lower dielectric losses of the all polypropylene (dissipation factor of 0.02%) versus the paper/polypropylene (dissipation factor of 0.3%). This allows the polypropylene capacitors to be operated at much higher RMS currents for the same capacitor volume. Paper/polypropylene commutation capacitors can be

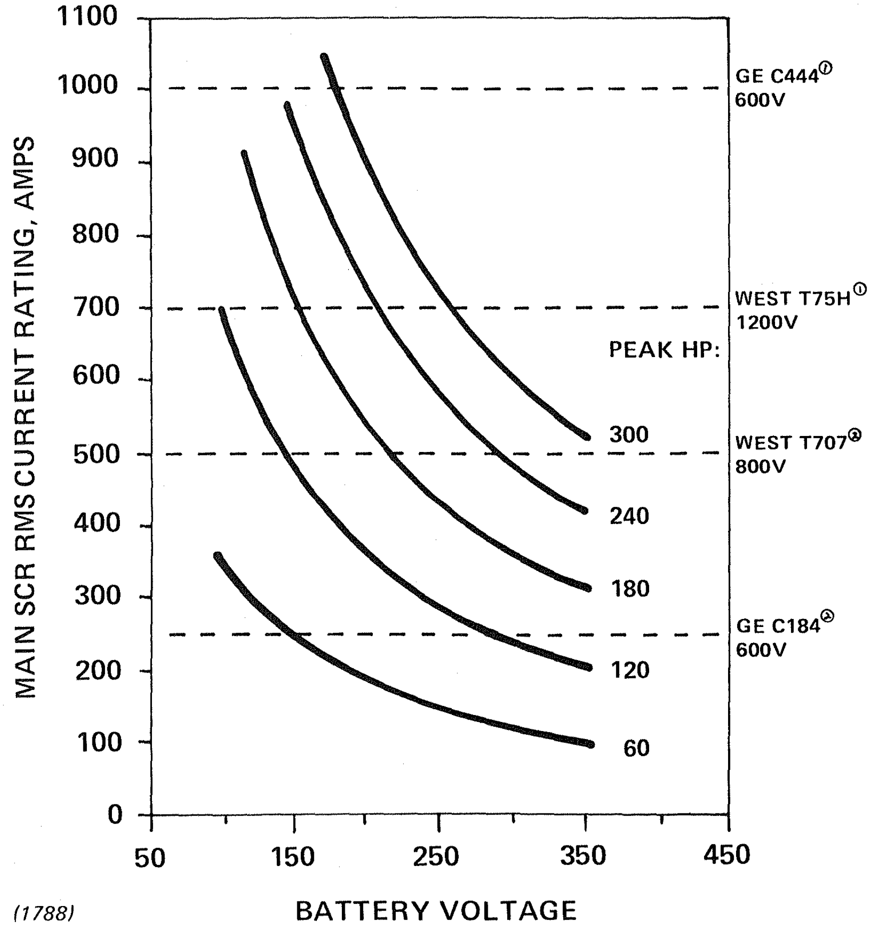


Figure 7.1 Main Thyristor Current Requirement as a Function of Battery Voltage

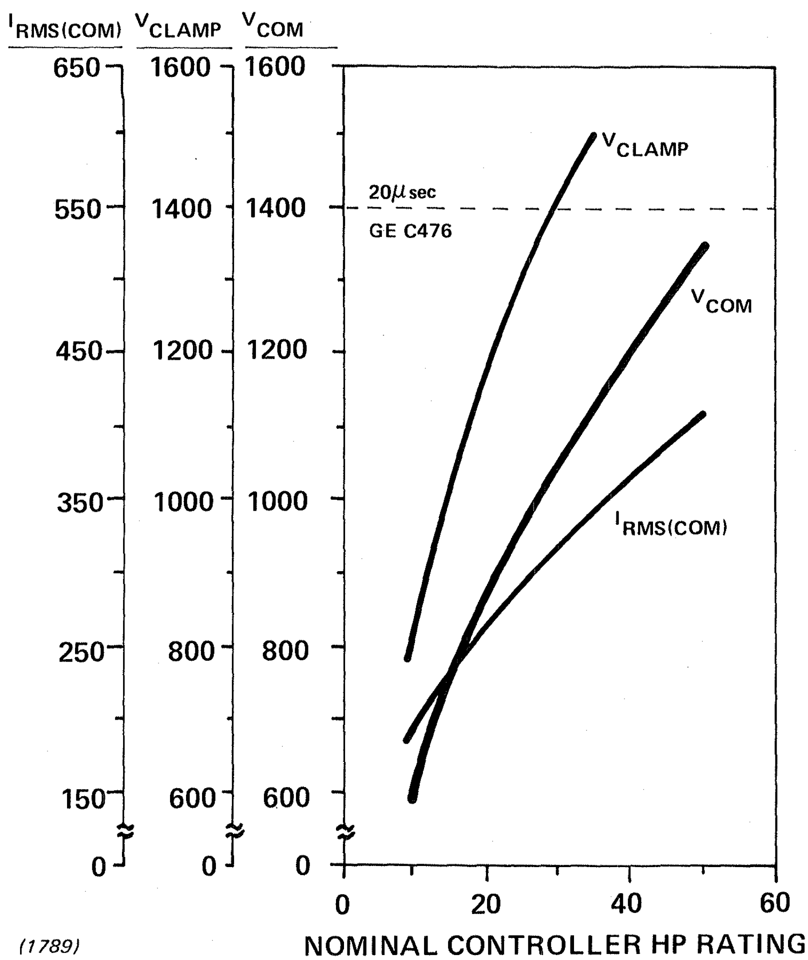


Figure 7.2 Commutaion Circuit Thyristor Requirement vs. Controller Rating

obtained with maximum dc voltage ratings from 400 to 2000 volts and a maximum CV product of approximately 0.03 where V is expressed in dc volts and C in farads. All-polypropylene commutation capacitors are available with maximum dc voltage ratings of 350 to 800 volts and a maximum CV product of approximately 0.01. The voltage ratings of the paper/polypropylene capacitors are suitable for scaling the controller family up through the 50 hp rating.

Finally, industrial-grade induction motors similar to the Gould E^{+}™ machine selected for the 10 hp controller are available up thru NEMA frame size 326, which would be rated at 50 hp at 60 Hz.

The results of the scaling exercise indicate that the present power stage inverter topology can be scaled to power levels of 50 hp. This controller would have a steady state power rating of 75 hp and be constructed with commercially available thyristors and commutation components.

7.3 Controller/Motor Cost Assessment

Estimated component cost (1979 dollars) for the nominal 10 hp ac controller is shown in Table 7.2 and is based on quoted component cost information. High volume cost estimates for the major power components is illustrated in Figure 7.3 and ac induction motor costs are illustrated in Figure 7.4. Shown in Table 7.3 is the estimated OEM and retail cost for both the ac controller and ac induction motor. OEM cost is defined as the expected selling price to a vehicle manufacturer with retail cost being the cost paid by the end user. Retail cost comparisons with state-of-the-art dc propulsion systems are shown in Table 7.4 where the ac controller/motor retail cost is compared to the estimated high-volume cost of Gould's second generation dc controller and motor and General Electric's SCR based dc controller/motor. Table 7-5 indicates the expected controller/motor life cycle cost including the estimated repair and maintenance cost.

TABLE 7.2

AC CONTROLLER/MOTOR COMPONENT COST ESTIMATE
(35 HP PEAK)

	1000 VEH	100,000 VEH
MAIN INVERTER DEVICES	$ 270	$ 180
COMMUTATION COMPONENTS	160	100
CONTROL ELECTRONICS (INL.TACH)	510	150
ENCLOSURE/HARDWARE/HEATSINKS	250	100
GEN.POWER CONDITIONING (FILTER CAPACITORS, CONTROL POWER SUPPLY	185	70
	$ 1375	$ 600
AC MOTOR	300	150
TOTAL COMPONENT COST	$ 1675	$ 750

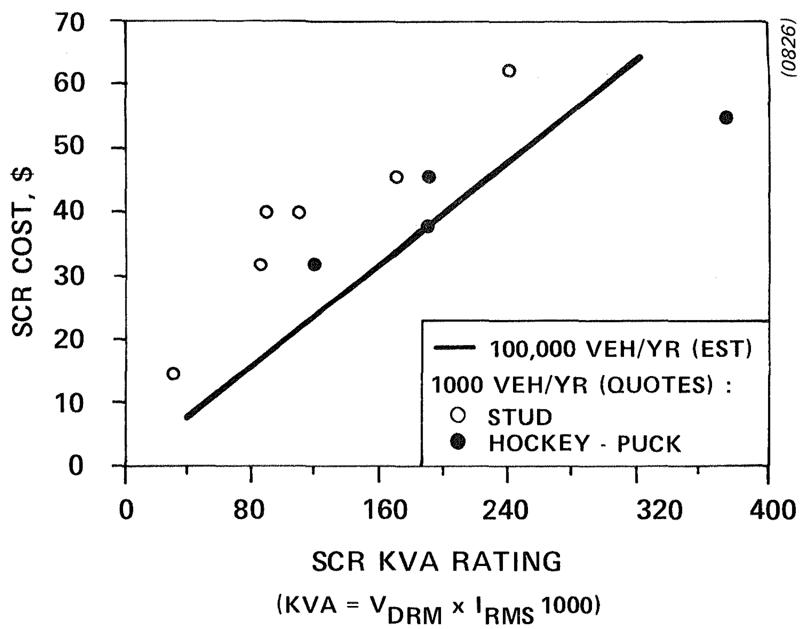


Figure 7.3 Main SCR Cost vs. K VA Rating (10μsec turn-off)

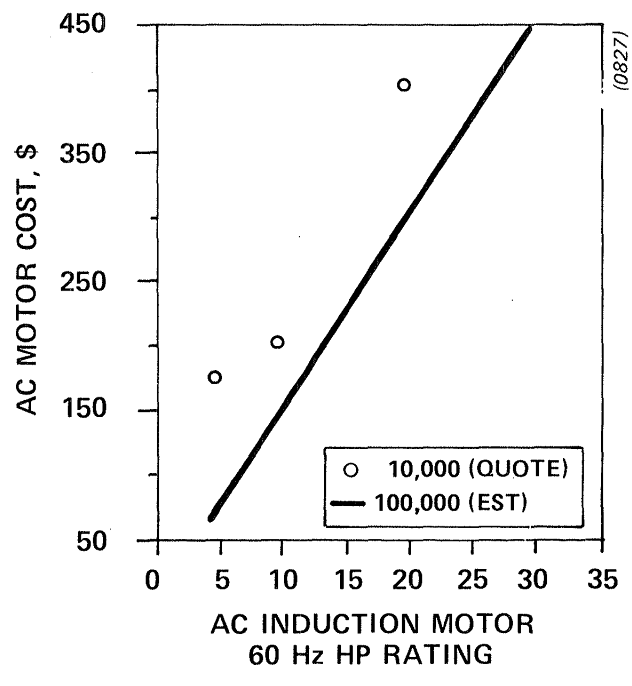


Figure 7.4 AC Induction Motor Cost vs. HP Rating

TABLE 7.3

AC CONTROLLER MOTOR - COMPONENT/OEM/RETAIL COST

100,000 VEH/YR
35 HP PEAK

	COMPONENT	OEM	RETAIL
CONTROLLER	$ 600	$ 1050	$ 1310
MOTOR	150	150	190
TOTAL	$ 750	$ 1200	$ 1500

TABLE 7.4

EV CONTROLLER/MOTOR - RETAIL COST COMPARISON

100,000 VEH/YR.
35 HP PEAK

	GOULD AC SCR	GOULD DC (MOD 1) SCR	GE-DC (EV-1)[1] SCR
CONTROLLER	$ 1310	$ 930	$ 879
MOTOR	190	890	959
	$ 1500	$ 1820	$ 1838

[1]NEAR-TERM ELECTRIC VEHICLE PROGRAM, PHASE 1, FINAL REPORT, 1977

TABLE 7.5

AC CONTROLLER/MOTOR LIFE CYCLE COST ESTIMATE

100,000 VEH/YR

100,000 CYCLES SAE J227A, D CYCLE
(APPROX. ONE MILE/CYCLE)

10 HP NOMINAL

INITIAL COST	$ 1500
INTEREST (4 YRS at 14%)	500
REPAIR/MAINT.*	300
	$ 2300

LIFE CYCLE COST - 2.3¢/MILE (0.037/Km)

* It is assumed that the controller will be reparied once during its life. Labor and materials are estimated to be 300.

7.4 On Board Battery Charger Modification

The power circuit of the present controller has been found to uniquely lend itself to the incorporation of a charging function. No additional semiconductor devices are required nor are the present operational characteristics of the drive affected. Thus with minor modifications to the motoring control logic and the addition of a contactor for isolation, an isolated on-board charger suitable for providing an 8-hour recharge at 208/240 Vac can be obtained.

The proposed on-board charger can be incorporated into the controller by the addition of a three-pole contactor (or circuit breaker) to the present ac controller power stage. This modification is illustrated in Figure 7.5.

The existing rectifiers D1, D3, D4, and D6, are used to convert the ac line voltage into a dc voltage for charging the propulsion battery. Existing transformers, T1 and T2, used during motoring to commutate the main inverter SCR's, are used in combination with the commutation SCR's and the energy recovery SCR's to charge the propulsion battery from the ac line. Utilizing existing components in this manner provides an on-board charger with minimal additional cost, weight and volume.

Charger Operation

Operation of the proposed on-board charging approach is described with the aid of Figure 7.5. For single phase ac line operation, ac power is supplied to two of the three output terminals of the inverter. One pole of the three pole circuit breaker is used to remove the ac motor from its position across the ac line. Rectifiers D1, D3, D4, and D6 are used in a full bridge configuration to convert the ac line voltage to a full-wave rectified dc voltage which appears across filter capacitor C3B. Capacitor C3B is part of the main capacitor bank used during motoring which has been separated into two units (C3A and C3B) by the remaining two poles of the circuit breaker. In the present ac controller the maximum voltage rating of filter capacitor C3 is 200 volts. For charger operation from a 208 or 240 Vac line the voltage

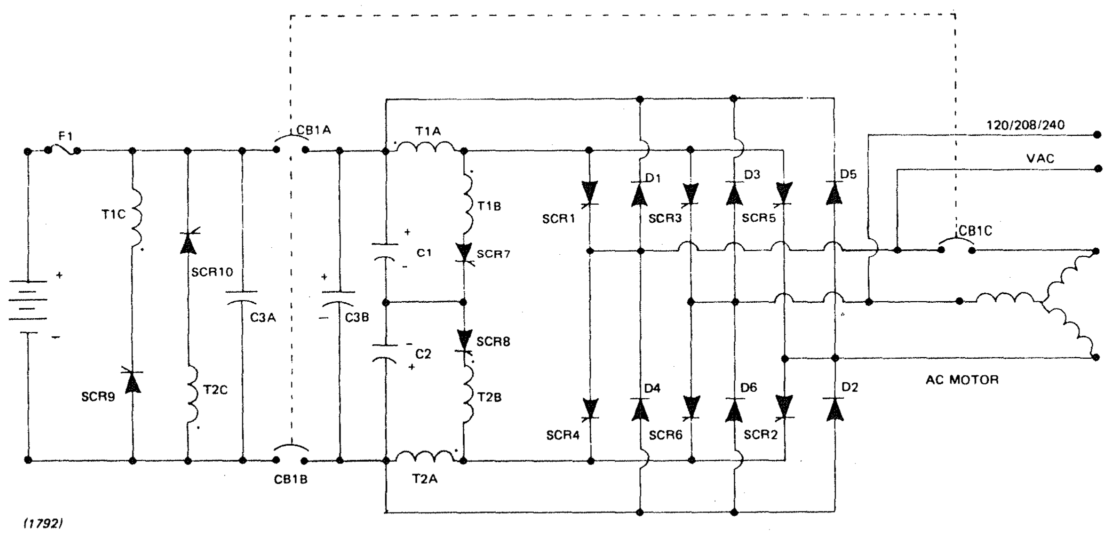


Figure 7.5 Modified AC Controller Incorporating an On-Board Charger

rating of filter capacitor C3B will be increased to 400 volts. By operating the cricuit consisting of T1, T2, C1, C2, SCR7 and SCR8 in a manner similar to that used during motoring, energy is transferred from the ac line and filter capacitor (C3B) to the propulsion battery via transformer windings T1C, T2C and SCR9 and 10.

Circuit operation can be described assuming the circuit initial conditions shown in Figure 7.5. The voltages on capacitors C1, C2 and C3B have polarities as shown. When SCR7 is gated the initial voltage on capacitor C1, defined as V_{C1}, is placed across the transformer windings T1A, B and the current increases sinusoidally in windings T1A, B. The LC circuit formed will allow C1 to discharge and C2 to charge. After a period of time depending on the resonant frequency of the LC circuit, the voltage across C1 will be zero and the current in windings T1A, B will be a maximum. Assuming current continues to circulate in windings T1A, B capacitors C1 and C2 will charge up with polarities opposite those shown in Figure 7.5. When the voltage across capacitor C1 charges to a high enough value that SCR9 is forward biased, and assuming SCR9 is then gated, current will transfer to winding T1C, SCR9, and the propulsion battery. When this occurs the voltage across capacitor C1 will be higher than the reflected voltage across windings T1A, B so that SCR7 will be reverse biased and thus turn-off.

With current circulating in winding T1C, SCR9, and the propulsion battery, the voltage on capacitor C1 will remain fixed and the energy stored in the magnetizing inductance (L_{AB}) of winding T1A, B will be transferred to the propulsion battery. The circuit conditions are now such that SCR8 can be gated and the above cycle repeated. Power flow rate is controlled by the gating frequency of SCR7 and SCR8.

VIII. Conclusion

A recent program leading to the design and construction of a prototype ac motor controller for electric vehicle applications has been described in this report. Design objectives laid out at the beginning of the program included low cost, excellent ruggedness/reliability characteristics, and high system efficiency. A desire to use readily-available technology dictated the choice of an industrial-grade squirrel-cage induction motor in this system so that development efforts focused on the electronic motor controller.

These efforts have led to the successful development of a 35 hp peak (26kW) ac motor propulsion system appropriate for use in a 3500 lb (1590kg) commuter vehicle. Voltage and frequency of the applied motor excitation waveforms are coordinated by the microprocessor-based controller in response to operator torque requests. This prototype controller in combination with a fixed-ratio gearbox drivetrain provides sufficient torque to complete the SAE J227a, Schedule D driving cycle with the simulated commuter vehicle. Controller testing has been conducted on a laboratory dynamometer.

The controller package consists of two separate modules; a larger enclosure for the power stage electronics and a smaller housing for the control electronics to be mounted in the passenger compartment. Combined weight of the ac motor and prototype controller is 270 lb which compares favorably with the weight of similarly-rated dc systems. Analysis of this first-generation controller prototype has indicated that at least a 30% reduction in both volume and weight are feasible by packaging improvements.

The bus-commutated inverter configuration adopted at the program's outset is responsible for providing both the controller's major advantages as well as its shortcomings. Low-cost thyristors possess the desired ruggedness while the bus-commutated topology provides additional cost advantages by requiring fewer power stage components than most alternative configurations. However, the bus-commutated topology produces some unique constraints on the switching algorithm, particularly during low-speed pulse-width-modulation operation. As a result, controller efficiency which exceeds 90% at crusing speeds drops to the vicinity of 70% for operation at 10 mph.

Experience gained during the development of the first-generation controller has suggested techniques for circumventing the shortcomings while retaining the advantages of the present power stage configuration. These include methods for optimizing the switching modulation strategy specifically for the bus-commutated configuration, and improvements in the inverter commutation magnetics for lower losses. Time limitations prevented their inclusion in the first-generation controller prototype.

In conclusion, this development program has successfully demonstrated the viability of ac electric vehicle propulsion systems using present technology. Future improvements in power semiconductor and controller technology can be expected to further enhance the attractiveness of ac motors over their dc counterparts for EV applications.

IX. References

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List of Abbreviations/Definitions

A	- ampere
ac	- alternating current
A_I	- proportional controller gain
C	- Centigrade
C^T	- equivalent parallel capacitance, commutation capcitors
dc	- direct current
D_I	- digital integral controller gain
D_K	- low frequency auxiliary integral controller gain
D_P	- digital proportional controller gain
EV	- electric vehicle
f_b	- base excitation frequency
f_{com}	- commutation circuit cycling frequency
f_{ex}	- motor excitation frequency
f^*_{ex}	- excitation frequency command
f_r	- rotor frequency
$f_{s\ell}$	- rotor slip frequency
$f^*_{s\ell}$	- slip frequency command
$f_{s\ell 1}$	- positive slip frequency limit
$f_{s\ell 2}$	- negative slip frequency
$f_{s\ell_{max}}$	- pullout slip frequency
ft	- foot
ft-lb	- foot-pound
hp	- horsepower
Hz	- Hertz
I_{bat}	- battery current

I_p - peak commutation circuit current

I_p^n - component n peak current

I^r - rotor current

I_{RMS}^n - component n RMS current

I^s - stator current

i_m - stator magnitizing current

j - $\sqrt{-1}$

kg - kilograms

km/h - kilometers/hour

kW - kilowatt

lb - pound

$L^{\ell s}$ - stator leakage inductance

$L^{\ell r}$ - rotor leakage inductance

L^m - stator magnitizing inductance

m - meter

m_i - modulation index

m_i^* - modulation index command

mph - miles/hour

N-m - Newton - meter

P^c - controller output power

P_{com} - power dissipated in the comutation circuit

P^e - motor shaft power

P_{bat} - battery power

PWM - pulse width modulation

Q_r - semiconductor recovered charge

rad - radians

rpm - revolutions per minute

rms - root means square

R^r - rotor winding resistance

R^s - stator winding resistance

s - % slip

SAE - Society of Automotive Engineers

SCR - silicon controlled rectifier

T_{com} - conduction interval of SCR7 (SCR8)

T_{clamp} - conduction interval of SCR9 (SCR10)

T^e - motor shaft torque

T^{e*} - torque command

TENV - Totally enclosed nonventillated

T_{ex} - motor excitation frequency period

T_q - thyristor reverse bias time

U_p - peak energy stored in the comutation circuit

V - volts

V_{ab} - inverter bus voltage defined across the main thyristors

V_{bat} - battery terminal voltage

V_C - comutation capacitor voltage

V_d - on-state semiconductor voltage drop

V_F^{SCRn} - foreward voltage SCRn

$V^{\ell\ell}$ - motor line - line voltage

$V_1^{\ell\ell}$ - fundamental motor line - line voltage

V_R^{SCRn} - reverse voltage - SCRn

V^s - line-neutral motor voltage

V^{s*} - commanded line - neutral motor voltage

V^s_{max} - maximum available line - neutral motor voltage

x - $^{N_B}/_{N_A}$ comutation transformer turns ratio

$X^{\ell s}$	- stator leakage reactance
$X^{\ell r}$	- rotor leakage reactance
X^{m}	- stator magnitizing reactance
E_v	- V/Hz error signal
ηm	- motor efficiency
λ_{ag}	- air gap flux
λ_t	- machine terminal volts/Hz
ω_b	- angular base frequency
ω^e	- angular excitation frequency
ω^r	- angular rotor frequency

APPENDIX I

VEHICLE ACCELERATION PREDICTION PROGRAM (VAPP)

Acceleration Program Equations:

The torque required at the drive wheels of a vehicle can be written as:

$$\tau_D = (F_R + F_A + F_I + F_g)R \qquad [1]$$

where F_R = rolling resistance (force)
F_A = aerodynamic drag force
F_I = inertial force
F_g = gravitational force due to grade
R = tire radius

These forces can be expressed as:

$$F_R = Mg\ (k_1 + k_2V)\cos\alpha \qquad [2]$$

$$F_A = .500\rho\ AV^2C_D \qquad [3]$$

$$F_I = \frac{MdV}{dt} \qquad [4]$$

$$F_g = Mg\ (\sin\alpha) \qquad [5]$$

Where M = vehicle mass (kg)
k_1 = tire rolling resistance (dimensionless)
k_2 = tire hysteresis coefficient (sec/m)
α = road grade (radians)
ρ = air density (kg/m^3)
V = vehicle velocity (m/s)
A = vehicle frontal area (m^2)
g = acceleration due to gravity (m/s^2)
C_D = drag coefficient (dimensionless)

The torque at the motor shaft is:

$$\tau_s = \tau_D/r\cdot eff \qquad [6]$$

Where r = drivetrain gear ratio

eff = drivetrain efficiency

The combination of equations [1] through [6] gives

$$\tau_s = \frac{.5\rho C_D AR}{r \cdot eff} V^2 + \frac{k_2 \cos\alpha\, MgR}{r \cdot eff} V + \frac{MR}{r \cdot eff}\frac{dV}{dt} + \frac{Mg(k_1\cos\alpha + \sin\alpha)R}{r \cdot eff} \qquad [7]$$

which is an equation of the general form:

$$\tau_s = A_1 V^2 + A_2 V + A_3 \frac{dV}{dt} + A_4 \qquad [8]$$

If τ_s is constant, then the time required to accelerate from V_1 to V_2 is:

$$t = \int_{V_1}^{V_2} \frac{A_3}{\tau_s - A_1 \nu^2 - A_2 \nu - A_4}\, d\nu \qquad [9]$$

This is the equation used for the constant torque acceleration calculation in the program.

Since motor output power, P_s, is related to the motor shaft speed, ω_s, by:

$$P_s = \tau_s\, \omega_s \qquad [10]$$

the shaft torque can be related to motor output power and vehicle speed by:

$$\tau_s = \frac{P_s}{k_3 V} \qquad [11]$$

where $$k_3 = \frac{r}{R} \qquad [12]$$

With the use of eq. [11], eq. [9] can be written for the constant motor shaft power case as:

$$t = \int_{V_1}^{V_2} \frac{k_3 A_3 \nu}{P_s - k_3 A_1 \nu^3 - k_3 A_2 \nu^2 - k_3 A_4 \nu} d\nu \qquad [13]$$

This is the equation used for the constant power acceleration calculations in the program.

```
      C     VAPP.FOR    PDP-11/RT11                 TSL:23-OCT-1978
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      C
      C WRITTEN BY -    Thomas S. Latos           23-OCT-1978
      C         GOULD LABS, ELECTRONIC RESEARCH
      C         ROLLING MEADOWS, ILL.
      C         312/640-4472
      C
      C MODIFICATIONS:
      C
      C **********************************************
      C         Vehicle acceleration performance   VER 1.0
      C **********************************************
      C
      C DESCRIPTION:
      C
      C     This program caculates the time to accelerate
      C     to a given velocity. The transistion from constant
      C     power to constant torque is accounted for.
      C     Input parameters are entered via an array of
      C     subroutines.
      C
      C INPUTS:
      C     All inputs are via subroutines
      C
      C OUTPUTS:
      C     Time to accelerate
      C
      C
      C SUBROUTINES CALLED:
      CVDP1
      C     EVRON
      C     DDP1
      C     MP1
      C     QATR
      C
      C
      C FOR>    VAPP=VAPP
      C LINK>VAPP=VAPP
      C
      C STANDARD FORMATS:
      11    FORMAT(80A1)
      12    FORMAT(10I8)
      13    FORMAT(X,80A1)
      14    FORMAT(6F12.0)
      18    FORMAT(10O8)
      19    FORMAT(4E20.8)
```

```
0007  22     FORMAT(40A2)
0008  24     FORMAT(20A4)
0009  28     FORMAT(10A8)
      C
      C DECLARATIONS:
0010         IMPLICIT REAL(M)
0011         DIMENSION RATIO(5)
0012         REAL                K3
0013         LOGICAL*1    HDAT(9),HTIM(8)
      C
0014         EXTERNAL TORQUE,POWER
0015         COMMON A1,A2,A3,A4,MTRTQ,MTPW,K3,HEDVEL
0016         DATA         RATIO/0.,0.,0.,0.,0./
0017         DATA ANS1,ANS2/0.,0./
0018         DATA                GRAV/9.815/
0019         DATA                VEHWT,VEHFA,DC/1590.91,1.858061,0.3/
0020         DATA                TRAD,VK1,VK2/.2667,.012,6.7E-5/
0021         DATA                HEDVEL,GRADE/0.,0./
0022         DATA                DIFRAT,DEFF/9.8,.80/
0023         DATA                MTRTQ,MTPW,TPTRPM,MSFPT/0.,0.,0.,0./
0024         DATA         IR,IW/5,5/,IO/5/
      C
      C MAIN BODY:
0025         CALL DATE(HDAT)
      C      INPUT PARAMETER CODE
0026         WRITE(IW,100)
0027  100    FORMAT(' INPUT PARAMETERS')
0028         WRITE(IW,101)
0029  101    FORMAT(10X,' REQUEST DESIRED INPUTS PER THE FOLLOWING CODE')
0030         WRITE(IW,102)
0031  102    FORMAT(15X,' VEHICLE DESIGN - 1')
0032         WRITE(IW,103)
0033  103    FORMAT(15X,' ENVIRONMENT - 2')
0034         WRITE(IW,104)
0035  104    FORMAT(15X,' VEHICLE DRIVETRAIN - 3')
0036         WRITE(IW,105)
0037  105    FORMAT(15X,' MOTOR DESIGN - 4')
0038         WRITE(IW,106)
0039  106    FORMAT(15X,' VEHICLE SUMMARY - 5',//)
0040  999    WRITE(IW,110)
0041  110    FORMAT('$INPUT CODE (1-4): ')
0042         READ(IR,12) IPARA
0043         IF(IPARA.EQ.9) STOP
0045         IPARA=IPARA+1
0046         GO TO (1000,1010,1020,1030,1040,1050) IPARA
0047  1010   CALL VDP1(VEHWT,VEHFA,DC,TRAD,VK1,VK2)
0048         GO TO 999
0049  1020   CALL EVRON(HEDVEL,GRADE)
0050         GO TO 999
0051  1030   CALL DDP1(DIFRAT,RATIO,DEFF)
0052         GO TO 999
0053  1040   CALL MP1(MTRTQ,MTPW,TPTRPM,RATIO,MSFPT)
0054         GO TO 999
0055  1050   CALL SUMARY(VEHWT,VEHFA,DC,TRAD,VK1,VK2,
```

```
           1    HEDVEL,GRADE,DIFRAT,RATIO,DEFF,MTRTQ,
           2    MTPW,TPTRPM,MSFPT)
                GO TO 999
         1000   CONTINUE
       C
                TEMP=TRAD/(DIFRAT*DEFF)
                A1=.6*DC*VEHFA*TEMP
                A2=VK2*COS(GRADE)*TEMP*VEHWT*GRAV
                A3=VEHWT*TEMP
                A4=(VEHWT*GRAV*(VK1*COS(GRADE)+SIN(GRADE)))*TEMP
                CALL SHFTSP(1.,DIFRAT,TRAD,MTRSPD)
                K3=MTRSPD
       C
                WRITE(IW,120)
          120   FORMAT(//,$,10X,'TEST SPEED (M/S): ')
                READ(IR,14) VEHSPD
                SPEED=VEHSPD
       C
       C        CACULATE RELATIONSHIP BETWEEN VEHICLE SPEED AND MOTOR SPEED
       C
                CALL SHFTSP(VEHSPD,DIFRAT,TRAD,MTRSPD)
                IF(MTRSPD.GT.TPTRPM) SPEED=TPTRPM*TRAD/DIFRAT
                IF(SPEED.EQ.0.) GO TO 500
       C        CACULATE ACCELERATION TIME
       C
                CALL QATR(0.,SPEED,1000,TORQUE,ANS1)
                IF(SPEED.EQ.VEHSPD) GO TO 2000
          500   CALL QATR(SPEED,VEHSPD,1000,POWER,ANS2)
         2000   ANS1=ANS1+ANS2
                WRITE(IW,130) ANS1
          130   FORMAT(' VEHICLE ACCELERATION TIME = ',F10.4)
                POW=(VEHSPD*(VEHWT*GRAV*VK1+VK2*VEHSPD)*COS(GRADE)
           1                +.6*VEHFA*DC*(VEHSPD+HEDVEL)**3
           2                +VEHWT*GRAV*SIN(GRADE)*VEHSPD)/DEFF
                WRITE(IW,150) POW
          150   FORMAT(' POWER TO  MAINTAIN SPEED =',F10.1,' WATTS')
                CALL SHFTSP(VEHSPD,DIFRAT,TRAD,MTRSPD)
                MTRSPD=MTRSPD*60/(2*3.1416)
                WRITE(IW,160) MTRSPD
          160   FORMAT(' MOTOR SPEED (RPM) @ SPEED =',X,F6.0)
                GO TO 999
                END
```

```
FORTRAN IV      Storage Map for Program Unit .MAIN.

Local Variables, .PSECT $DATA, Size = 000176 (    63. words)

Name    Type  Offset      Name    Type  Offset      Name    Type  Offset
ANS1    R*4   000046      ANS2    R*4   000052      DC      R*4   000072
DEFF    R*4   000122      DIFRAT  R*4   000116      GRADE   R*4   000112
GRAV    R*4   000056      IO      I*2   000142      IPARA   I*2   000144
IR      I*2   000136      IW      I*2   000140      MSFPT   R*4   000132
MTRSPD  R*4   000152      POW     R*4   000166      SPEED   R*4   000162
TEMP    R*4   000146      TPTRPM  R*4   000126      TRAD    R*4   000076
VEHFA   R*4   000066      VEHSPD  R*4   000156      VEHWT   R*4   000062
VK1     R*4   000102      VK2     R*4   000106

COMMON Block /      /, Size = 000040 (    16. words)

Name    Type  Offset      Name    Type  Offset      Name    Type  Offset
A1      R*4   000000      A2      R*4   000004      A3      R*4   000010
A4      R*4   000014      MTRTQ   R*4   000020      MTPW    R*4   000024
K3      R*4   000030      HEDVEL  R*4   000034

Local and COMMON Arrays:

Name      Type    Section Offset  ------Size----- Dimensions
HDAT    L*1       $DATA   000024  000011 (    5.) (9)
HTIM    L*1       $DATA   000035  000010 (    4.) (8)
RATIO   R*4       $DATA   000000  000024 (   10.) (5)

Subroutines, Functions, Statement and Processor-Defined Functions:

Name    Type    Name    Type    Name    Type    Name    Type    Name    Type
COS      R*4    DATE     R*4    DDP1     R*4    EVRON    R*4    MP1      R*4
POWER    R*4    QATR     R*4    SHFTSP   R*4    SIN      R*4    SUMARY   R*4
TORQUE   R*4    VDP1     R*4
```

```
      C     DDP1.FOR    PDP-11/RT11                 TSL:20-OCT-1978
      C
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      C WRITTEN BY -     Thomas S. Latos         20-OCT-1978
      C         GOULD LABS, ELECTRONIC RESEARCH
      C         ROLLING MEADOWS, ILL.
      C         312/640-4472
      C
      C MODIFICATIONS:
      C
      C **********************************************
      C         Drivetrain parameter subroutine   VER 1.0
      C **********************************************
      C
      C DESCRIPTION:
      C
      C     This is an I/O routine for entering vehicle
      C     drivetrain parameters. Up to five transmission
      C     ratios are permissible.
      C
0001        SUBROUTINE DDP1(DIFRAT,RATIO,DEFF,STIM)
      C INPUTS:
      C     DIFRAT                  DIFFERENTIAL GEAR RATIO
      C     RATIO                   ARRAY CONTAINING THE TRANSMISSION RATIOS
      C     DEFF                    THE DRIVETRAIN EFFICIENCY
      C
      C OUTPUTS:
      C     OUTPUTS - The outputs of this subroutine are the user inputs
      C
      C
      C SUBROUTINES CALLED:
      C     NONE
      C
      C
      C FOR>    DDP1=DDP1
      C
      C STANDARD FORMATS:
0002  12    FORMAT(10I8)
0003  14    FORMAT(6F12.0)
      C
      C DECLARATIONS:
0004        LOGICAL*1   HDAT(9),HTIM(8)
0005        DIMENSION RATIO(5)
      C
0006        DATA        ITR/0/
0007        DATA                IR,IW/5,5/,IO/5/
      C
```

```
C MAIN BODY:
              WRITE(IW,100)
        100   FORMAT(' DRIVETRAIN DESIGN PARAMETERS',/)
              WRITE(IW,110)
        110   FORMAT($,10X,' DIFFERENTIAL RATIO: ')
              READ(IR,14) DIFRAT
              WRITE(IW,120)
        120   FORMAT($,10X,' NUMBER OF TRANSMISSION RATIOS: ')
              READ(IR,12) ITR
              IF(ITR.EQ.0) GO TO 200
              WRITE(IW,142)
        142   FORMAT($,10X,' SHIFT TIME (SEC): ')
              READ(IR,14) STIM
              DO 150 I=1,ITR
              WRITE(IW,130) I
        130   FORMAT($,10X,' RATIO ',I2,X,':')
              READ(IR,14) RATIO(I)
              IF(I.EQ.5) GO TO 200
        150   CONTINUE
        200   WRITE(IW,140)
        140   FORMAT($,10X,' DRIVETRAIN EFFICIENCY(%): ')
              READ(IR,14) DEFF
              DEFF=DEFF/100.
              WRITE(IW,145)
        145   FORMAT(//)
              RETURN
              END
```

```
FORTRAN IV      Storase Map for Prosram Unit DDP1

Local Variables, .PSECT $DATA, Size = 000046 (   19. words)

Name    Type  Offset      Name    Type   Offset      Name    Type   Offset
DEFF    R*4 @ 000004      DIFRAT  R*4 @ 000000      I       I*2    000044
IO      I*2   000040      IR      I*2   000034      ITR     I*2    000032
IW      I*2   000036      STIM    R*4 @ 000006

Local and COMMON Arrays:

Name      Type    Section Offset  ------Size----- Dimensions
HDAT   L*1        $DATA   000010  000011 (    5.) (9)
HTIM   L*1        $DATA   000021  000010 (    4.) (8)
RATIO  R*4      @ $DATA   000002  000024 (   10.) (5)
```

```
      C     EVRON.FOR   PDP-11/RT11               TSL:23-OCT-1978
      C
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      C         GOULD LABS, ELECTRONIC RESEARCH
      C         ROLLING MEADOWS, ILL.
      C         312/640-4472
      C
      C MODIFICATIONS:
      C
      C **********************************************
      C         Environment ssubroutine   VER 1.0
      C **********************************************
      C
      C DESCRIPTION:
      C
      C     This is an I/O routine to enter vehicle operating
      C     environment to the main routine.
      C
0001        SUBROUTINE EVRON(HEDVEL,GRADE)
      C INPUTS:
      C     HEDVEL                 Headwind velocity (M/S)
      C     GRADE                  Road slope from horizontal (degrees)
      C
      C OUTPUTS:
      C     Outputs are the same as the inputs
      C
      C
      C SUBROUTINES CALLED:
      C     NONE
      C
      C
      C FOR>    EVRON=EVRON
      C
      C STANDARD FORMATS:
0002  14    FORMAT(6F12.0)
      C
      C DECLARATIONS:
0003        LOGICAL*1   HDAT(9),HTIM(8)
      C
0004        DATA        IR,IW/5,5/,IO/5/
      C
      C MAIN BODY:
0005        WRITE(IW,100)
0006  100   FORMAT(' OPERATING ENVIRONMENT',/)
0007        WRITE(IW,110)
0008  110   FORMAT($,10X,' HEADWIND VELOCITY (M/S): ')
```

```
      READ(IR,14) HEDVEL
      WRITE(IW,120)
120   FORMAT($,10X,' GRADE (DEGREES): ')
      READ(IR,14) GRADE
      GRADE=GRADE*2.*3.14159/360. !RADIANS
      WRITE(IW,130)
130   FORMAT(//)
      RETURN
      END
```

```
FORTRAN IV      Storage Map for Program Unit EVRON

Local Variables, .PSECT $DATA, Size = 000034 (    14. words)

Name    Type   Offset       Name    Type   Offset       Name    Type   Offset
GRADE   R*4 @ 000002       HEDVEL  R*4 @ 000000       IO      I*2    000032
IR      I*2    000026       IW      I*2    000030

Local and COMMON Arrays:

Name      Type     Section Offset   ------Size----- Dimensions
HDAT    L*1       $DATA   000004   000011 (     5.) (9)
HTIM    L*1       $DATA   000015   000010 (     4.) (8)
```

```
      C     MP1.FOR     PDP-11/RT11             TSL:20-OCT-1978
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      C WRITTEN BY -    Thomas S. Latos         20-OCT-1978
      C         GOULD LABS, ELECTRONIC RESEARCH
      C         ROLLING MEADOWS, ILL.
      C         312/640-4472
      C
      C MODIFICATIONS:
      C
      C **********************************************
      C         Motor Parameter Subroutine   VER 1.0
      C **********************************************
      C
      C DESCRIPTION:
      C
      C     This program is an I/O routine to input motor
      C     parameters to the main program via subroutine
      C     arguements.
      C
0001        SUBROUTINE MP1(MTRTQ,MTPW,TPTRPM,RATIO,MSFPT)
      C INPUTS:
      C     MTRTQ               Low speed motor torque
      C     TPTRPM              TORQUE/POWER transistion speed (RPM)
      C     RATIO(1)    ARRAY CONTAINING GEAR RATIOS FOR TRANSMISSION
      C     MTPW                MAXIMUN MOTOR POWER
      C     MSFPT               MOTOR SHIFT SPEED
      C
      C OUTPUTS:
      C     Outputs: the outputs of this program are the arguements
      C     of the subroutine.
      C
      C
      C SUBROUTINES CALLED:
      C     NONE
      C
      C
      C FOR>    MP1=MP1
      C
      C STANDARD FORMATS:
0002  12    FORMAT(10I8)
0003  14    FORMAT(6F12.0)
      C
      C DECLARATIONS:
0004        IMPLICIT    REAL(M)
0005        LOGICAL*1   HDAT(9),HTIM(8)
0006        DIMENSION   RATIO(5)
```

```
      C
0007        DATA        IR,IW/5,5/,IO/5/
      C
      C MAIN BODY:
0008        WRITE(IW,100)
0009  100   FORMAT(' MOTOR PARAMETERS')
0010        WRITE(IW,110)
0011  110   FORMAT($,10X,' MAXIMUM SHAFT TORQUE (N-M): ')
0012        READ(IR,14) MTRTQ
0013        WRITE(IW,115)
0014  115   FORMAT($,10X,' MAXIMUM SHAFT POWER (W): ')
0015        READ(IR,14) MTPW
0016        WRITE(IW,120)
0017  120   FORMAT($,10X,' TORQUE/POWER TRANSISSION SPEED(RPM): ')
0018        READ(IR,14) TPTRPM
0019        TPTRPM=TPTRPM*2.*3.1416/60. !RADIANS/SEC
0020        IF(RATIO(1).EQ.0) GO TO 135
0022        WRITE(IW,130)
0023  130   FORMAT($,10X,' MOTOR SHIFT POINT(RPM): ')
0024        READ(IR,14) MSFPT
0025        MSFPT=MSFPT*2.*3.1416/60.    !RADIANS/SEC
0026  135   WRITE(IW,140)
0027  140   FORMAT(//)
0028        RETURN
0029        END
```

```
FORTRAN IV      Storage Map for Program Unit MP1

Local Variables, .PSECT $DATA, Size = 000042 (    17. words)

Name    Type   Offset       Name    Type   Offset       Name    Type   Offset
IO      I*2    000040       IR      I*2    000034       IW      I*2    000036
MSFPT   R*4 @ 000010        MTPW    R*4 @ 000002        MTRTQ   R*4 @ 000000
TPTRPM  R*4 @ 000004

Local and COMMON Arrays:

Name      Type    Section Offset  -------Size----- Dimensions
HDAT    L*1       $DATA   000012  000011 (     5.) (9)
HTIM    L*1       $DATA   000023  000010 (     4.) (8)
RATIO   R*4     @ $DATA   000006  000024 (    10.) (5)
```

```
0001        SUBROUTINE SHFTSP(VEHSPD,DIFRAT,TRAD,MTRSPD)
      C
0002        IMPLICIT    REAL(M)
0003        MTRSPD=(VEHSPD*DIFRAT)/TRAD !RADIANS/SEC
0004        RETURN
0005        END
```

```
FORTRAN IV      Storage Map for Program Unit SHFTSP

Local Variables, .PSECT $DATA, Size = 000010 (     4. words)

Name   Type  Offset      Name   Type  Offset      Name   Type  Offset
DIFRAT R*4 @ 000002      MTRSPD R*4 @ 000006      TRAD   R*4 @ 000004
VEHSPD R*4 @ 000000
```

```
      FUNCTION TORQUE(V)
      IMPLICIT    REAL(M)
      REAL K3
      COMMON A1,A2,A3,A4,MTRTQ,MTPW,K3,HEDVEL
      TORQUE=A3/(MTRTQ-A1*(V+HEDVEL)**2-A2*V-A4)
      RETURN
      END
```

```
FORTRAN IV      Storage Map for Program Unit TORQUE

Local Variables, .PSECT $DATA, Size = 000006 (    3. words)

Name    Type  Offset       Name    Type  Offset       Name    Type  Offset
TORQUE  R*4   000002 Eqv V         R*4 @ 000000

COMMON Block /       /, Size = 000040 (   16. words)

Name    Type  Offset       Name    Type  Offset       Name    Type  Offset
A1      R*4   000000       A2      R*4   000004       A3      R*4   000010
A4      R*4   000014       MTRTQ   R*4   000020       MTPW    R*4   000024
K3      R*4   000030       HEDVEL  R*4   000034
```

```
      FUNCTION POWER(V)
      IMPLICIT    REAL(M)
      REAL        K3
      COMMON A1,A2,A3,A4,MTRTQ,MTPW,K3,HEDVEL
      POWER=(A3*K3*V)/(MTPW+K3*(-A1*(V+HEDVEL)**3-A2*V**2-A4*V))
      RETURN
      END
```

```
FORTRAN IV      Storage Map for Program Unit POWER

Local Variables, .PSECT $DATA, Size = 000006 (     3. words)

Name    Type  Offset        Name    Type  Offset      Name    Type  Offset
POWER   R*4   000002 Eqv V          R*4 @ 000000

COMMON Block /      /, Size = 000040 (   16. words)

Name    Type  Offset        Name    Type  Offset      Name    Type  Offset
A1      R*4   000000        A2      R*4   000004      A3      R*4   000010
A4      R*4   000014        MTRTQ   R*4   000020      MTPW    R*4   000024
K3      R*4   000030        HEDVEL  R*4   000034
```

```
      C      VDP1.FOR    PDP-11/RT11                 TSL:20-OCT-1978
      C
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      C
      C WRITTEN BY -     Thomas S. Latos           20-OCT-1978
      C          GOULD LABS, ELECTRONIC RESEARCH
      C          ROLLING MEADOWS, ILL.
      C          312/640-4472
      C
      C MODIFICATIONS:
      C
      C ***********************************************
      C          Vehicle Design Subroutine   VER 1.0
      C ***********************************************
      C
      C DESCRIPTION:
      C
      C      This program is an I/O routine to input vehicle
      C      design parameters.
      C
0001         SUBROUTINE VDP1(VEHWT,VEHFA,DC,TRAD,VK1,VK2)
      C INPUTS:
      C      VEHWT                Vehicle weight(kg)
      C      VEHFA                Vehicle frontal area(m2)
      C      DC          Drag coefficient
      C      TRAD                 Tire radius(m)
      C      VK1,VK2              Rolling resistance tire coefficients
      C
      C      OUTPUTS:
      C          Outputs are the inputs to the main program
      C
      C
      C SUBROUTINES CALLED:
      C      NONE
      C
      C
      C FOR>    VDP1=VDP1
      C
      C STANDARD FORMATS:
0002  12     FORMAT(10I8)
0003  14     FORMAT(6F12.0)
      C
      C DECLARATIONS:
0004         LOGICAL*1   HDAT(9),HTIM(8)
      C
0005         DATA        IR,IW/5,5/,IO/5/
      C
      C MAIN BODY:
```

```
      WRITE(IW,100)
100   FORMAT(' VEHICLE DESIGN PARAMETERS',/)
      WRITE(IW,110)
110   FORMAT($,10X,' VEHICLE WEIGHT(kg): ')
      READ(IR,14) VEHWT
      WRITE(IW,120)
120   FORMAT($,10X,' VEHICLE FRONTAL AREA(m2): ')
      READ(IR,14) VEHFA
      WRITE(IW,130)
130   FORMAT($,10X,' DRAG COEFFICIENT: ')
      READ(IR,14) DC
      WRITE(IW,140)
140   FORMAT($,10X,' TIRE RADIUS(m): ')
      READ(IR,14) TRAD
      WRITE(IW,150)
150   FORMAT($,10X,' TIRE COEFFICIENTS (k1,k2): ')
      READ(IR,14) VK1,VK2
      WRITE(IW,160)
160   FORMAT(//)
      RETURN
      END
```

```
FORTRAN IV      Storage Map for Program Unit VDP1

Local Variables, .PSECT $DATA, Size = 000044 (   18. words)

Name    Type   Offset      Name    Type   Offset      Name    Type   Offset
DC      R*4 @ 000004      IO      I*2    000042      IR      I*2    000036
IW      I*2    000040      TRAD    R*4 @ 000006      VEHFA   R*4 @ 000002
VEHWT   R*4 @ 000000      VK1     R*4 @ 000010      VK2     R*4 @ 000012

Local and COMMON Arrays:

Name      Type    Section Offset  ------Size----- Dimensions
HDAT    L*1       $DATA   000014  000011 (    5.) (9)
HTIM    L*1       $DATA   000025  000010 (    4.) (8)
```

```
0001          SUBROUTINE SUMARY (VEHWT,VEHFA,DC,TRAD,VK1,VK2,
             1     HEDVEL,GRADE,DIFRAT,RATIO,DEFF,MTRTQ,MTFW,TPTRPM,MSFPT)
0002          IMPLICIT REAL(M)
0003          DIMENSION RATIO(5)
0004          DATA IW,IR/5,5/
        C
        C
0005          WRITE(IW,100)
0006    100   FORMAT(/,' VEHICLE SUMMARY',/)
0007          WRITE(IW,110)
0008    110   FORMAT(8X,'BODY',15X,'TIRES')
0009          WRITE(IW,120)
0010    120   FORMAT(2X,'MASS',4X,'FA',4X,'DC',3X,'RADIUS',3X,'K1',
             1     6X,'K2')
0011          WRITE(IW,130) VEHWT,VEHFA,DC,TRAD,VK1,VK2
0012    130   FORMAT(X,F6.1,2X,F4.2,2X,F3.1,3X,F5.3,2X,F5.3,3X,E8.1,//)
0013          WRITE(IW,140)
0014    140   FORMAT(2X,'GRADE',2X,'HEADWIND')
0015          WRITE(IW,150) GRADE,HEDVEL
0016    150   FORMAT(3X,F3.1,5X,F4.1,//)
0017          WRITE(IW,160)
0018    160   FORMAT(2X,'REAR END',3X,'TRANSMISSION',3X,'EFFECIENCY')
0019          DO 10 I=1,5
0020               ITR=I-1
0021               IF(RATIO(I).EQ.0.) GO TO 20
0023    10         CONTINUE
0024    20    WRITE(IW,170) DIFRAT,ITR,DEFF*100.
0025    170   FORMAT(5X,F3.1,12X,I1,10X,F4.1,/)
0026          WRITE(IW,180)
0027    180   FORMAT(16X,'MOTOR')
0028          WRITE(IW,190)
0029    190   FORMAT(4X,'TORQUE',4X,'POWER',3X,'TRANSSION',3X,'SHIFT')
0030          WRITE(IW,200) MTRTQ,MTFW/1000.,TPTRPM,MSFPT
0031    200   FORMAT(3X,F5.1,5X,F4.1,5X,F6.1,5X,F6.1,//)
0032          RETURN
0033          END
```

FORTRAN IV   Storage Map for Program Unit SUMARY

Local Variables, .PSECT $DATA, Size = 000060 (24. words)

Name	Type	Offset	Name	Type	Offset	Name	Type	Offset
DC	R*4 @	000004	DEFF	R*4 @	000024	DIFRAT	R*4 @	000020
GRADE	R*4 @	000016	HEDVEL	R*4 @	000014	I	I*2	000044
IR	I*2	000040	ITR	I*2	000046	IW	I*2	000036
MSFPT	R*4 @	000034	MTPW	R*4 @	000030	MTRTQ	R*4 @	000026
TPTRPM	R*4 @	000032	TRAD	R*4 @	000006	VEHFA	R*4 @	000002
VEHWT	R*4 @	000000	VK1	R*4 @	000010	VK2	R*4 @	000012

Local and COMMON Arrays:

Name	Type	Section	Offset	------Size-----	Dimensions
RATIO	R*4	@ $DATA	000022	000024 (10.)	(5)

```
      SUBROUTINE QATR(XL,XU,NDIM,FCT,ANS)
      TEMP=0.
      H=(XU-XL)/NDIM
      IF(H.EQ.0.) GO TO 20
      ANS=FCT(XL)+FCT(XU)
      DO 10 I=1,NDIM-1
      TEMP=TEMP+FCT(XL+(I*H))
   10 CONTINUE
      ANS=(ANS+TEMP*2.)/2.*H
      RETURN
   20 ANS=0.
      RETURN
      END
```

```
FORTRAN IV      Storage Map for Program Unit QATR

Local Variables, .PSECT $DATA, Size = 000032 (    13. words)

Name    Type   Offset       Name    Type   Offset       Name    Type   Offset
ANS     R*4 @ 000010       H       R*4    000016       I       I*2    000022
NDIM    I*2 @ 000004       TEMP    R*4    000012       XL      R*4 @ 000000
XU      R*4 @ 000002

Subroutines, Functions, Statement and Processor-Defined Functions:

Name    Type    Name    Type    Name    Type    Name    Type    Name    Type
FCT      R*4
```

APPENDIX II

COMMUTATION CIRCUIT DESIGN ANALYSIS

This appendix presents an analysis of the inverter commutation sequence. Expressions are derived for the peak current, I_p^{SCR7} flowing in a commutation thyristor (SCR7-SCR8), the maximum commutation capacitor voltage V_C, and the stored energy, U_p, of the commutation circuit as functions of the battery voltage, V_{bat}, battery current, I_{bat}, thyristor turn-off time, T_{qmin}, and circuit component values L_a, C_1, and $x \equiv N_b/N_a$. The peak energy is then minimized with respect to normalized component values to determine "ideal" values for these components depending on I_{bat}, V_{bat}, and T_{qmin}. It is seen that this analysis yields only two constraints on the three components. The free parameter may be used to lower the peak current at the expense of raising the commutation capacitor voltage, or vice-versa.

The circuit is modeled as shown in Figure A2-1. The coupled inductors, L^A and L^B are characterized by two parameters L_a and x. L_a is the inductance of the L^A winding (L^B terminals open-circuited), and x^2 is the ratio of the L^B and L^A inductances.

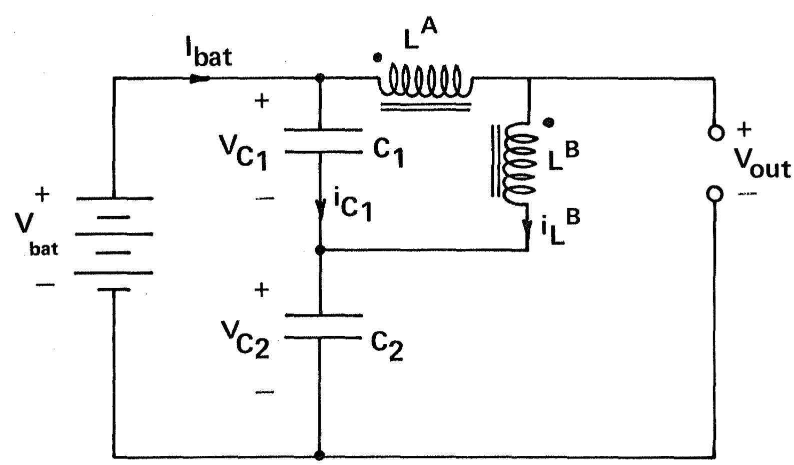
$$x^2 = \frac{L_b}{L_a} \qquad [1]$$

The effective inductance of the coupled inductors in series is thus

$$L_c = L_a\,(1+x)^2 \qquad [2]$$

C^T is defined as the total commutation capacitance, or twice the value of either commutation capacitor alone.

$$C^T = 2C_1 \qquad [3]$$



(1340)

Figure A2–1 This figure contains the commutation circuit for the bus commutated inverter. The design analysis concentrates on determining the value of commutation inductance, capacitance, and energy stored prior to commutating the main SCR's. The clamp windings are not included in this figure.

The initial conditions at the initiation of the commutation sequence are:

$$i_{L^B}\Big|_{t=o} = \frac{I_{bat}}{1+x} \quad [4]$$

$$v_{C_1}\Big|_{t=o} = V_o \quad [5]$$

where I_{bat} is the dc bus or motor current before initiation of the commutation, and V_o is the (as yet undefined) initial commutation capacitor voltage. The initial commutation current is smaller than the motor current, due to the added inductance of the L^B winding.

V_{out} is defined as the voltage across the thyristor bus to be commutated. It is assumed here that the thyristor was conducting before commutation, and that the motor phase current remains positive (negative, in the case of a bottom bus commutation) during the commutation interval, so that the thyristor reverse bias time is defined here as the interval of time over which V_{out} remains negative.

The analysis will proceed as follows. An expression for the reverse bias time will be derived, and set equal to T_{qmin}. This constraint will determine V_{C_1}, the commutation capacitor voltage. Given V_{C_1} and the original parameters of L_a and x, the peak stored energy will be evaluated and minimized.

Application of Kirchoff's voltage and current laws to the circuit of Figure A2-1 yields a second-order constant-coefficient differential equation in i_{L^B}.

$$\frac{d^2\, i_{L^B}}{dt^2} + \frac{1}{L_c\, C^T} \left(i_{L^B} \right) = 0 \quad [6]$$

The initial condition on v_{C1} can be restated in terms of i_{T1B}

$$L_C \left. \frac{di_{LB}}{dt} \right|_{t=o} = V_o \qquad [7]$$

The differential equation and initial conditions form a closed set. The solution is valid up to the point when the clamp thysistor (SCR 9-10-not considered here) is fired. Until that time,

$$i_{LB} = \frac{I_{bat}}{(1+x)} \left[\frac{1+y^2}{y^2} \right]^{1/2} \sin(\omega t+\alpha) \qquad [8]$$

$$\alpha \equiv \cos^{-1} \left[\frac{1}{(1+y^2)^{1/2}} \right] \qquad [9]$$

$$\omega^2 \equiv \frac{1}{L_c\ C^T} \qquad [10]$$

$$y \equiv \left(\frac{L_a}{C^T} \right)^{1/2} \left(\frac{I_{bat}}{V_o} \right) \qquad [11]$$

This expression for i_{T1B} can be used with Kirchoff's voltage law to determine v_{out} as a function of time.

$$V_{out} = V_{bat} - \frac{\left(\frac{L_a}{C^T} \right)^{1/2} I_{bat}}{(1+x)} \left[\frac{1+y^2}{y^2} \right]^{1/2} \cos(\omega t+\alpha) \qquad [12]$$

The time, t_{RB}, when $v_{out} < 0$ is thus given by

$$\omega t_{RB} = \cos^{-1} \left[q \frac{y}{\sqrt{1+y^2}} \right] - \cos^{-1} \left[\frac{1}{\sqrt{1+y^2}} \right] \qquad [13]$$

where

$$q \equiv \frac{1+x}{z} \qquad [14]$$

$$z = \frac{I_{bat}}{V_{bat}} \left(\frac{L_a}{C^T} \right)^{1/2} \qquad [15]$$

Now, t_{RB} is set equal to $T_{q_{min}}$, and the cosine of both sides is taken. Use of a trigometric identity yields

$$W \equiv \cos(\omega T_{q_{min}}) \qquad [16]$$

$$W = \frac{qy}{1+y^2} + \frac{y}{1+y^2} \left(1+(1-q^2)y^2 \right)^{1/2} \qquad [17]$$

Eq. 17 has four solutions for y, two imaginary roots, ±j, and two real roots.

$$y = \frac{W}{q \pm (1-W^2)^{1/2}} \qquad [18]$$

It can be shown that the "-" solution corresponds to a non-physical root of the equation, and that the "+" solution is the correct one.

The peak stored energy is defined as the energy stored in L^A and L^B when i_{L^B} is at its peak value.

$$U_p = \tfrac{1}{2} L_c \, I_p^2$$

$$= \tfrac{1}{2} L_a \, I_{bat}^2 \left(\frac{1+y^2}{y^2} \right) \qquad [19]$$

where the peak current, I_p, is obtained from Eq. 8. It is useful to normalize this peak stored energy to a quantity defined as the diverted energy, U_d, $\underline{U}_p$ is this normalized diverted energy. Then

$$\underline{U}_p \equiv \frac{U_p}{U_d} \equiv \frac{U_p}{V_{bat}\ I_{bat}\ t_{q_{min}}} \qquad [20]$$

Where U_d is the product of battery voltage, dc bus current, and minimum thyristor turn-off time. Thus

$$\underline{U}_p = \tfrac{1}{2}\left(\frac{1+y^2}{y^2}\right)\left(\frac{1}{q\ \cos^{-1}W}\right) \qquad [21]$$

Substitution for y yields

$$\underline{U}_p = \frac{W^2 + [q+ (1-W^2)^{1/2}]^2}{2\ q\ W^2\cos^{-1}W} \qquad [22]$$

The peak normalized energy of the commutation circuit is seen to depend on the two normalized parameters, q and W. Minimization with respect to q gives

$$\underline{U}_p\bigg|_{q=1} = \frac{W^2+[1+ (1-W^2)^{1/2}]^2}{2W^2\cos^{-1}W} \qquad [23]$$

A value of 1 for q yields the minimum energy for any particular W. Minimization with respect to W is done numerically. A plot of U_p (W) is shown in Figure A2-2. The minimum value of $\underline{U}_p$ is seen to occur for $W=W_{min}=0.8494$. The significance of $\underline{U}_p$ is that the peak stored energy in the commutation circuit must be greater than 3.81 times the diverted energy, U_d.

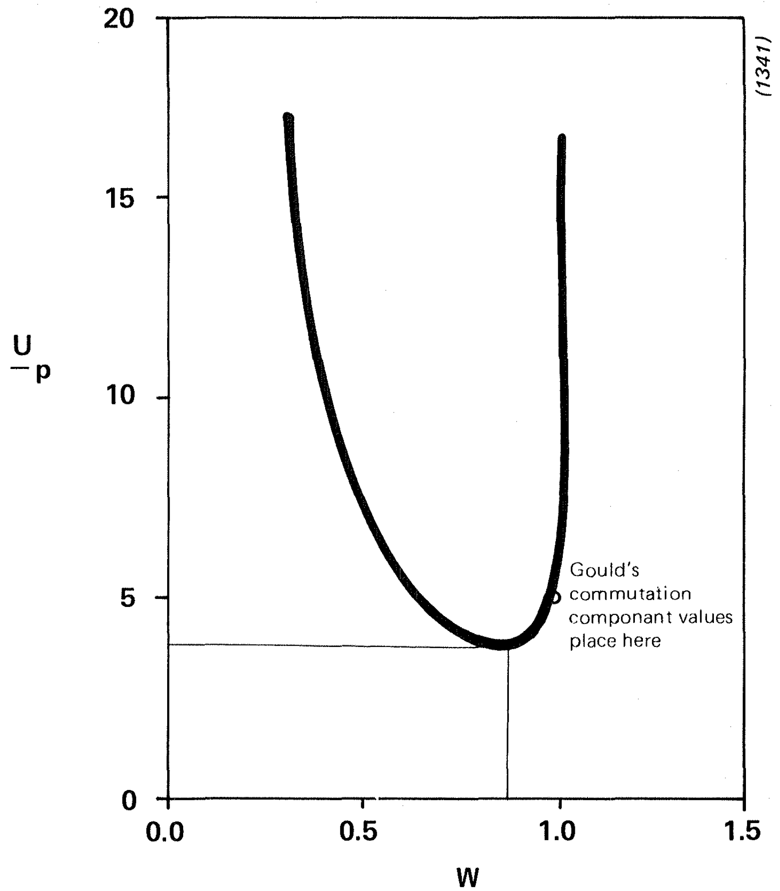


Figure A2–2 **Plot of $\underline{U}_p$ vs. W, q = 1**

Minimum Value, $\underline{U}_p \cong 3.81$, occurs at $W \cong 0.849$

At this point, using $q \equiv 1$ and $W_{min} \equiv 0.8494$, then

$$\underline{y} = 0.556 = Y_{min}$$

$$\underline{\omega T_{q_{min}}} = 0.5559 = K_{min}$$

The actual inductances, capacitance, and voltage corresponding to these normalized values are determined as follows. The normalized circuit time constant, K_{min}, is used to calculate the ideal inductance L_a.

$$L_a = \left(\frac{T_{q_{min}}}{K_{min}} \right)^2 \Big/ (1+x)^2 \, C^T \qquad [24]$$

At the minimum peak energy $q \equiv 1$, therefore

$$L_a = \frac{V_{bat} \, T_{q_{min}}}{I_{bat} \, K_{min}} \qquad [25]$$

$$V_o = \frac{(1+x) \, V_{bat}}{Y_{min}} \qquad [26]$$

$$C^T = \left(\frac{I_{bat}}{V_{bat}} \right) \left(\frac{T_{q_{min}}}{(1+x)^2} \right) \left(\frac{1}{K_{min}} \right) \qquad [27]$$

The peak current, I_p is given by

$$i_{L^B}\Big|_{peak} = \frac{I_{bat}}{(1+x)} \left[\frac{1+Y^2_{min}}{Y^2_{min}} \right]^{1/2} \qquad [28]$$

Thus, the main winding inductance for minimum peak stored commutation energy is given by Eq. 25. Then Eqs. 26 and 28 are used to determine a value of x which best suits the commutation thysistor voltage and current ratings.

APPENDIX III

INVERTER LOSS ANALYSIS

III.1 Controller Main Semiconductor On-State Loss Analysis

An expression for the on-state conduction loss of the controller main devices is derived in this appendix. First, the average battery power is calculated as a function of the peak motor phase current (assuming sinusoidal waveforms) and motoring power factor. Then, an assumption of constant semiconductor on-state voltage drop is used to compute the main device conduction loss. The two equations for battery power, and semiconductor conduction losses are then combined to yield a prediction of main semiconductor losses normalized to battery power as a function of the power factor and ratio of semiconductor on-state voltage drop to battery voltage.

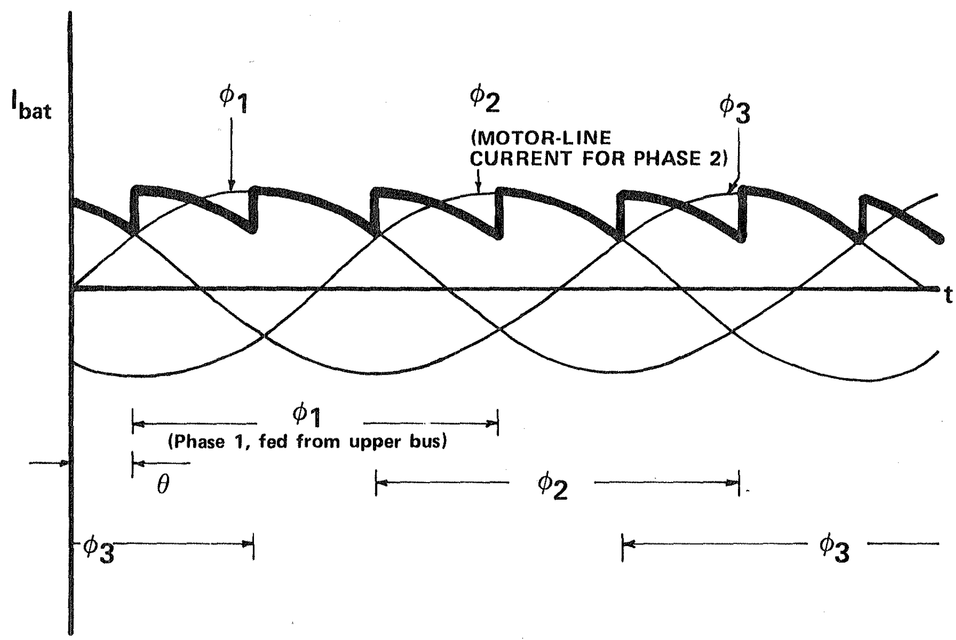
Figure A3-1 gives a schematic illustration of the three (fundamental) phase currents in the motor during operation of the inverter. The motor is assumed to be a set of three ideal current sources, and the battery is assumed an ideal voltage source.

The lighter lines in Figure A3-1 show the phase currents as a function of time. Underneath the plot are markings which indicate the time intervals during which each motor phase ($\phi 1$, $\phi 2$, and $\phi 3$) is fed from its upper bus thyristor or diode. Six step operation is assumed, so that one of the SCR's associated with any particular phase is on at any specific time. The solid line represents the sum of current in the bus as a function of time (i.e., the actual battery line current).

The voltage and current are out of phase by the power factor angle, as indicated in the Figure. The average battery line current is

$$i_{bat} = \frac{1}{\pi/3} \int_{\theta+\pi/3}^{\theta+2\pi/3} I_0 \sin\mu d\mu = \frac{3}{\pi} I_0 \cos\theta \qquad [1]$$

Since the motor phase current is always passing through a semiconductor, be it a diode or thyristor, an assumption of equal and constant on-state voltage



(1344)

Figure A3–1 This figure illustrates the three motor phase currents as a function of time. The motor is operating with a power factor angle θ and it requires a peak phase current of I_0.

The heavy line in this figure is the resulting dc link current flowing in the inverter.

drops, V_d, for both gives a simple approximation for the main semiconductor conduction loss, P_c

$$P_c = \frac{V_d}{\pi} \int_0^{\pi} I_o \sin\mu d\mu = \frac{2}{\pi} V_d I_o \qquad [2]$$

There are six SCR-Diode pairs, each on for a 50% duty-cycle. So, the total time average main conduction loss is

$$P_c^T = \frac{6}{\pi} V_d I_o \qquad [3]$$

Thus, the fraction of battery power (during motoring) that is lost to the mains is

$$\frac{P_c^T}{P_{bat}} = \frac{2V_d}{V_{bat} \cos\theta} \qquad [4]$$

Note that as $\theta \to \pi/2$, $\cos(\theta) \to 0$, and $(P_{Loss}/P_{bat}) \to \infty$. This is due to the fact that θ=90 corresponds to no battery power out, while there still exists finite semiconductor losses.

The motor power factor is sometimes defined as

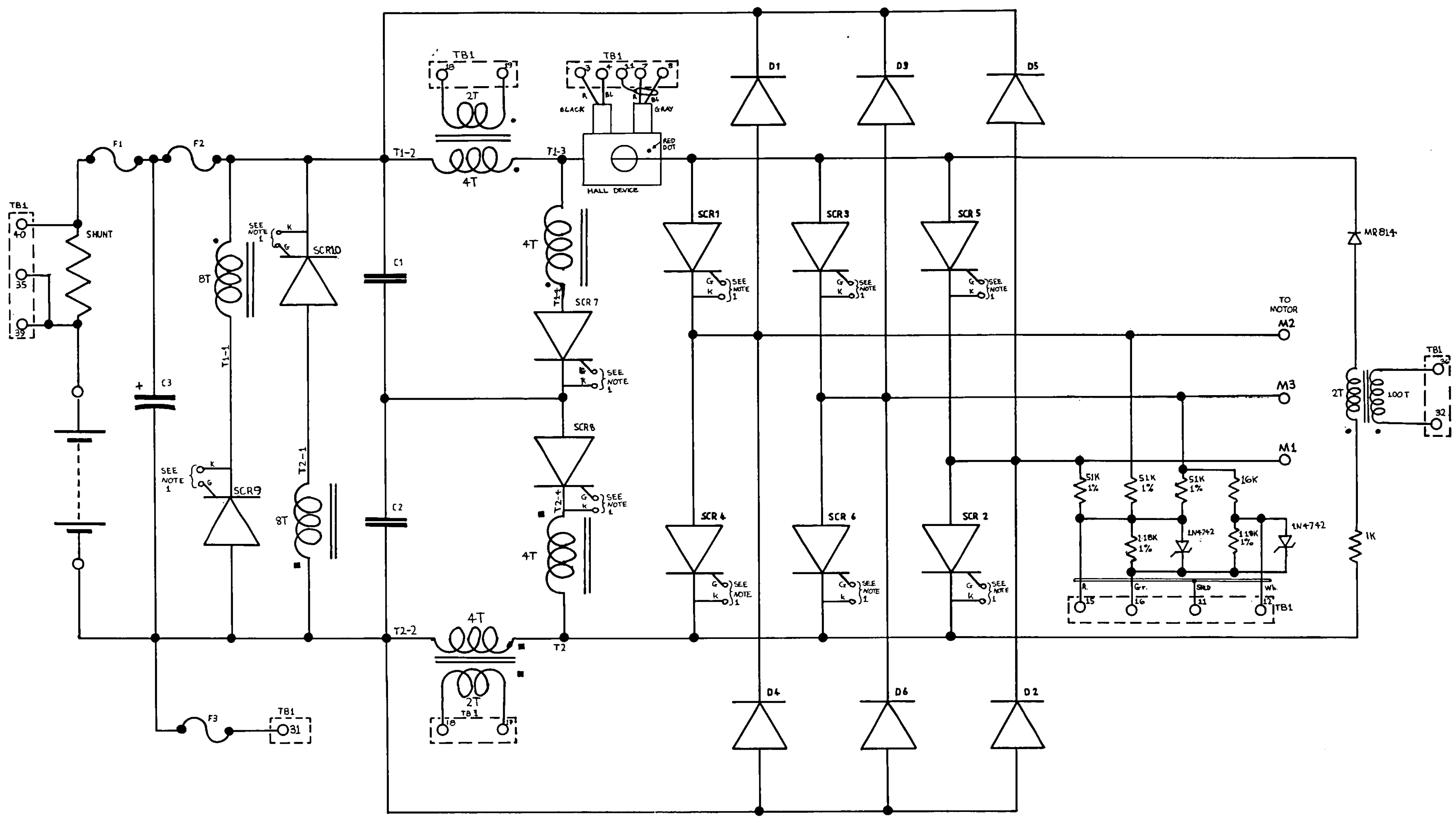
$$P.F. = \frac{P_{Motor}}{3V_{\ell-n} I_{RMS}} \qquad [5]$$

Caution should be exercised in using this definition of $\cos(\theta)$ in the formula of eq. 5, as the two definitions coincide only when the semiconductor voltage drops are negligible. In fact, the power factor, defined in terms of the motor power, will go to zero before θ reaches 90°. This is due to the fact that, for $\theta = 0$, the motor accepts current form the battery at a voltage that is less than the battery voltage by one diode drop, but returns it at a voltage that is greater by as much. When the net current out of the battery is small, this difference can become significant.

APPENDIX IV

CONTROLLER ELECTRICAL SCHEMATICS

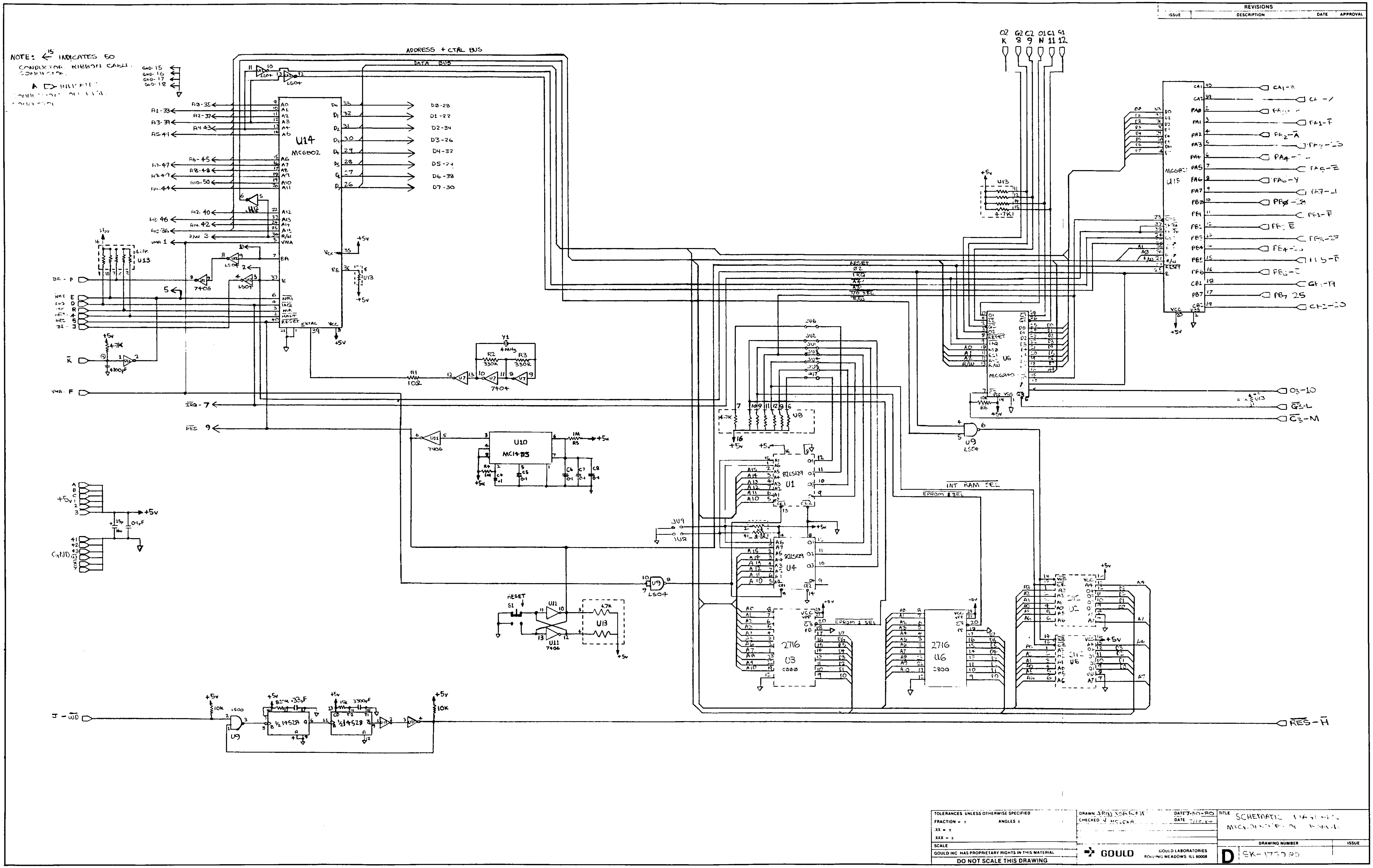
REVISIONS			
ISSUE	DESCRIPTION	DATE	APPROVAL



NOTES.

1/ CONNECT GATE AND CATHODE LEADS TO DRIVERS. SEE SCHEMATIC DIAGRAM SK-111979

TOLERANCES: UNLESS OTHERWISE SPECIFIED FRACTION = ± ANGLES ± .XX = ± .XXX = ±	DRAWN J.R.W. BARNES DATE 7/21/80 CHECKED G. Bates DATE 7/22/80	TITLE SCHEMATIC DIAGRAM POWER CIRCUIT	
SCALE GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL DO NOT SCALE THIS DRAWING	GOULD GOULD LABORATORIES ROLLING MEADOWS, ILL. 60008	DRAWING NUMBER D SK 172280	ISSUE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DATA BUS
U14
MC6802
U15
U10
MC14585
2716
U3
2716
U6
82LS129
U1
82LS129
U4
7404
7406
LS04
RESET
INT RAM SEL
EPROM 1 SEL
RES-H
REVISIONS
ISSUE
DESCRIPTION
DATE
APPROVAL
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTION ±
ANGLES ±
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ROLLING MEADOWS ILL 60008
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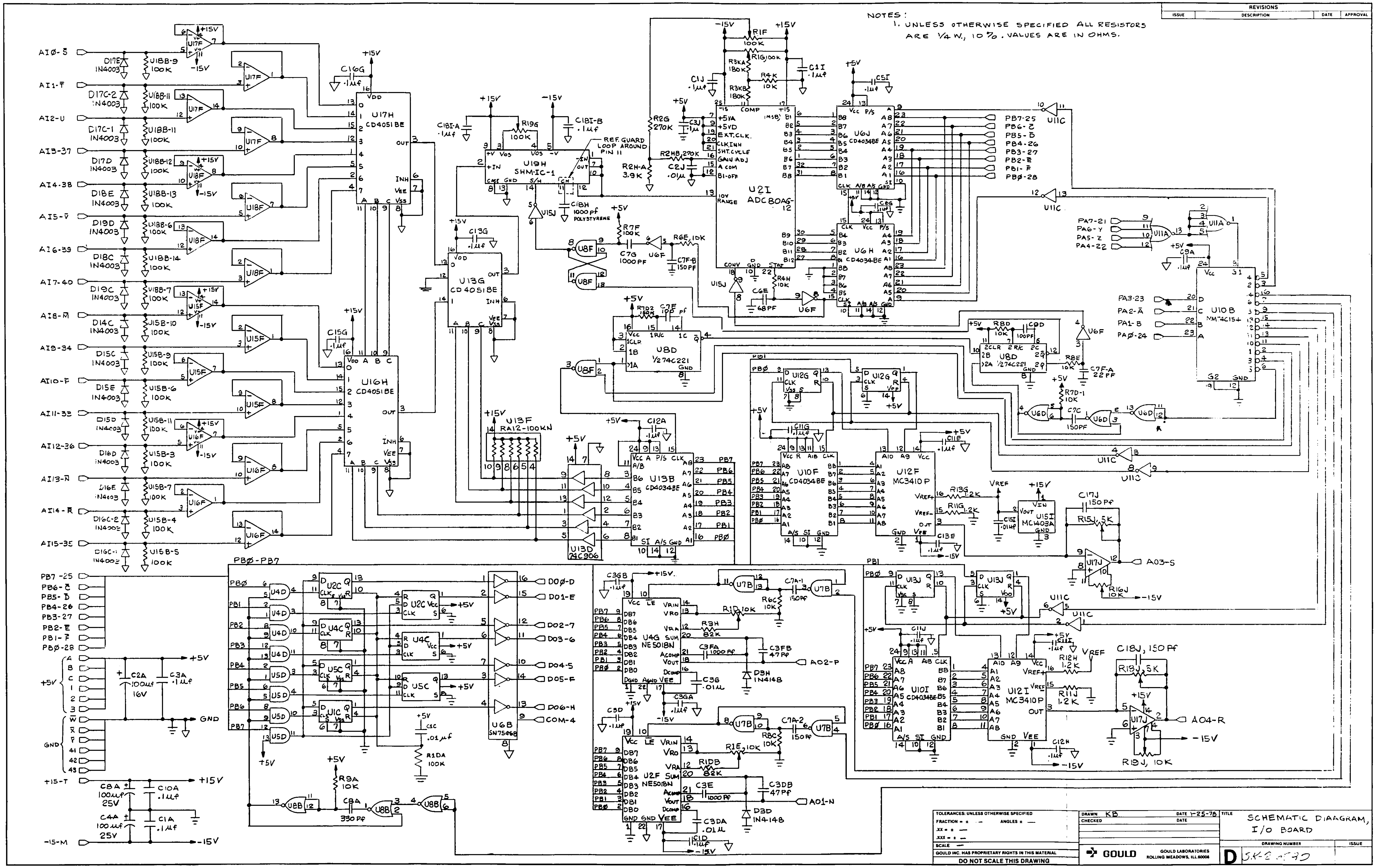
NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/4 W, 10%. VALUES ARE IN OHMS.
REVISIONS
TOLERANCES: UNLESS OTHERWISE SPECIFIED
GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL
DO NOT SCALE THIS DRAWING
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DATE 1-25-78
CHECKED
SCHEMATIC DIAGRAM, I/O BOARD
GOULD
GOULD LABORATORIES ROLLING MEADOWS, ILL. 60008
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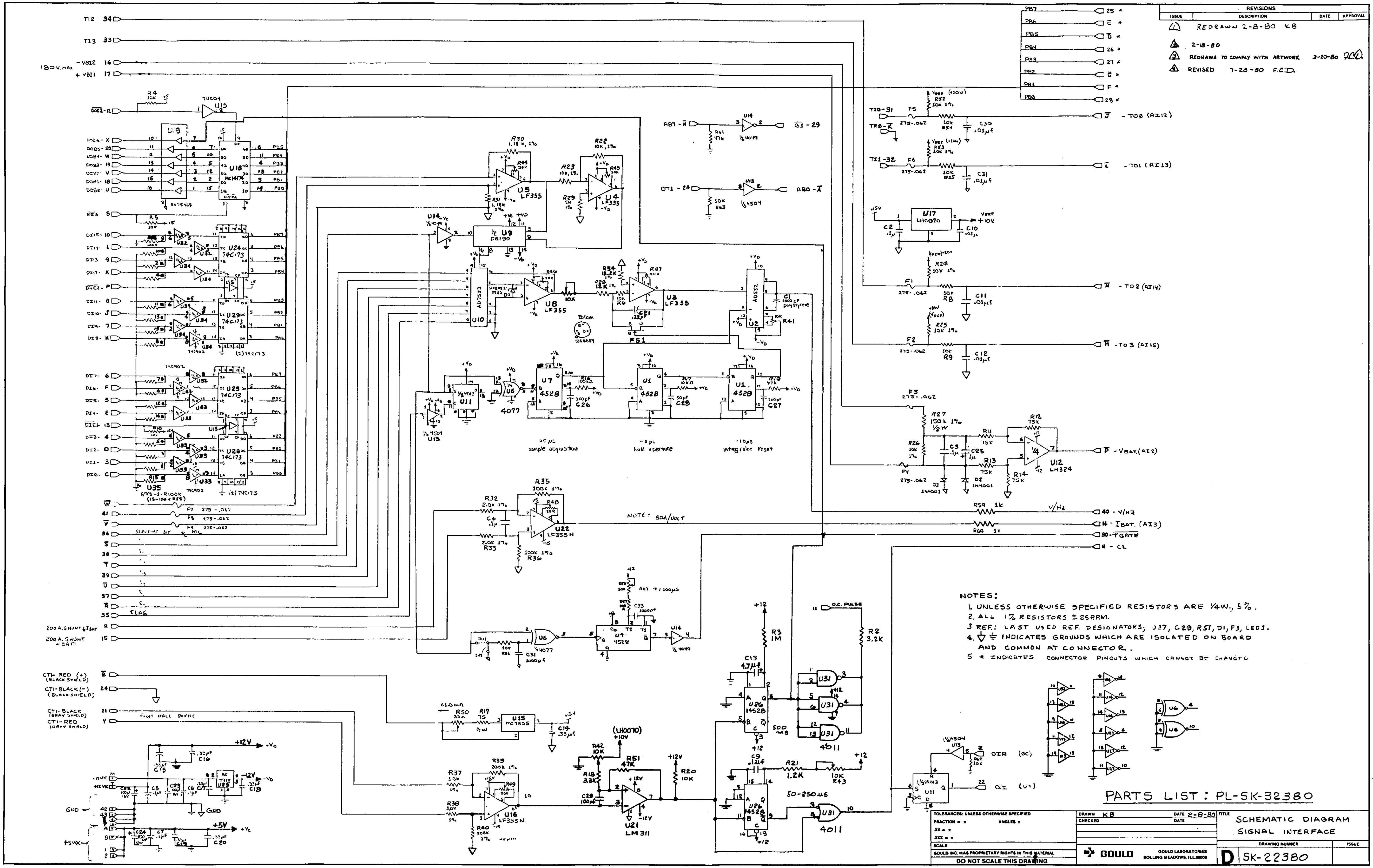
REVISIONS
ISSUE DESCRIPTION DATE APPROVAL
1 REDRAWN 2-8-80 KB
2 2-18-80
3 REDRAWN TO COMPLY WITH ARTWORK 3-20-80
4 REVISED 7-28-80 F.C.D.
NOTES:
1. UNLESS OTHERWISE SPECIFIED RESISTORS ARE 1/4W., 5%.
2. ALL 1% RESISTORS ±25P.P.M.
3 REF.: LAST USED REF. DESIGNATORS; U37, C29, R51, D1, F3, LED1.
4. INDICATES GROUNDS WHICH ARE ISOLATED ON BOARD AND COMMON AT CONNECTOR.
5 * INDICATES CONNECTOR PINOUTS WHICH CANNOT BE CHANGED
PARTS LIST : PL-SK-32380
TOLERANCES: UNLESS OTHERWISE SPECIFIED
FRACTION = ± ANGLES ±
.XX = ±
.XXX = ±
SCALE
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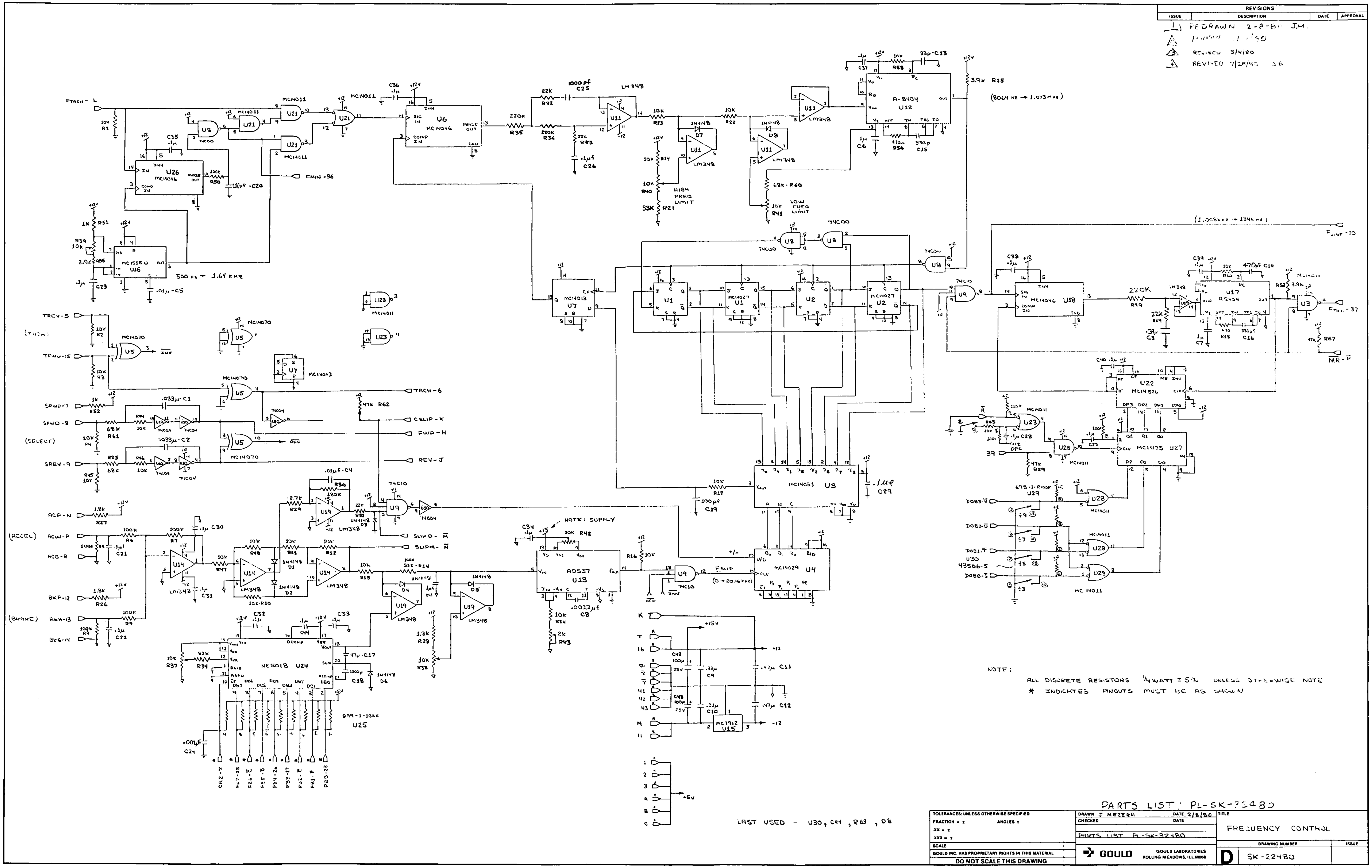
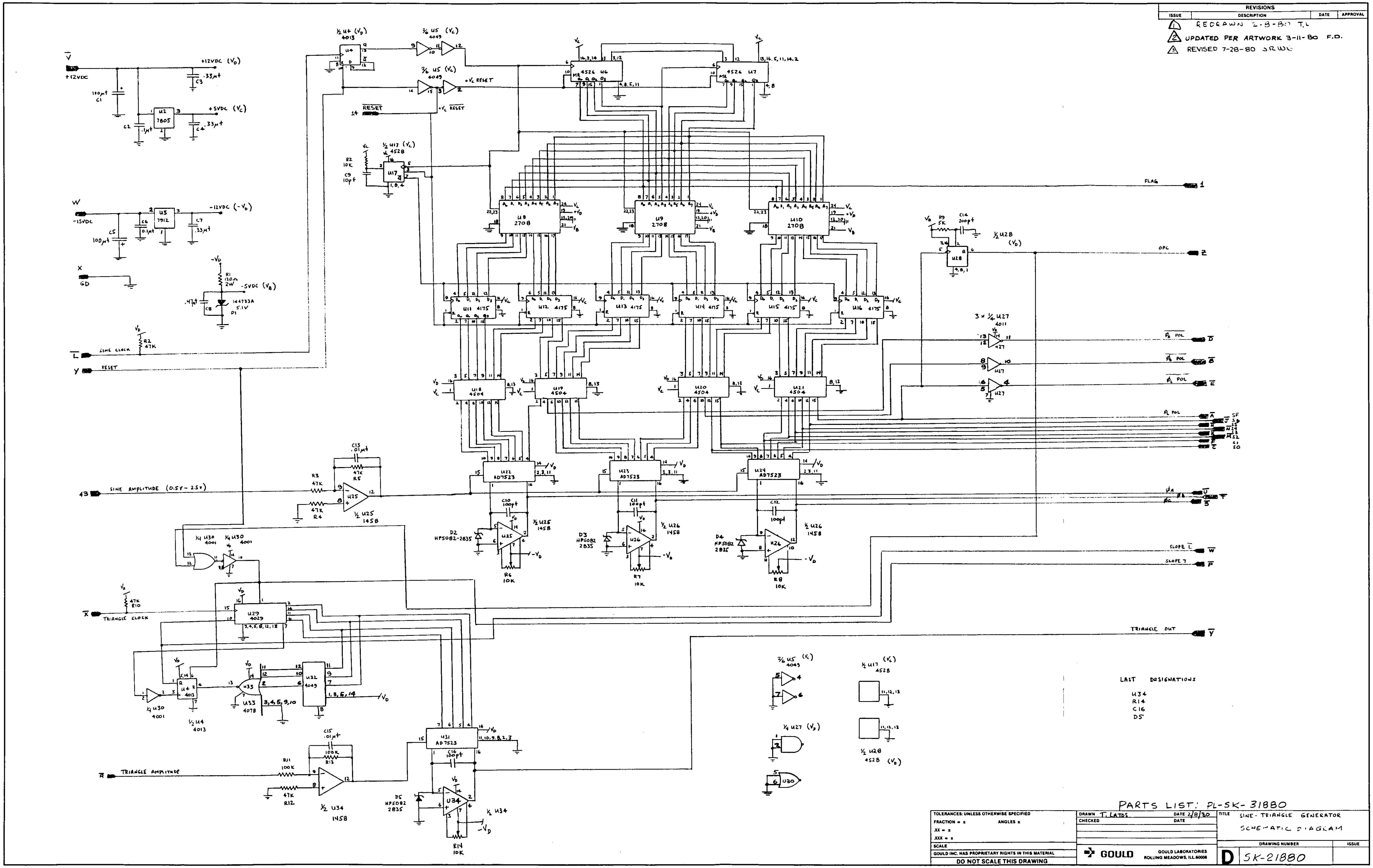
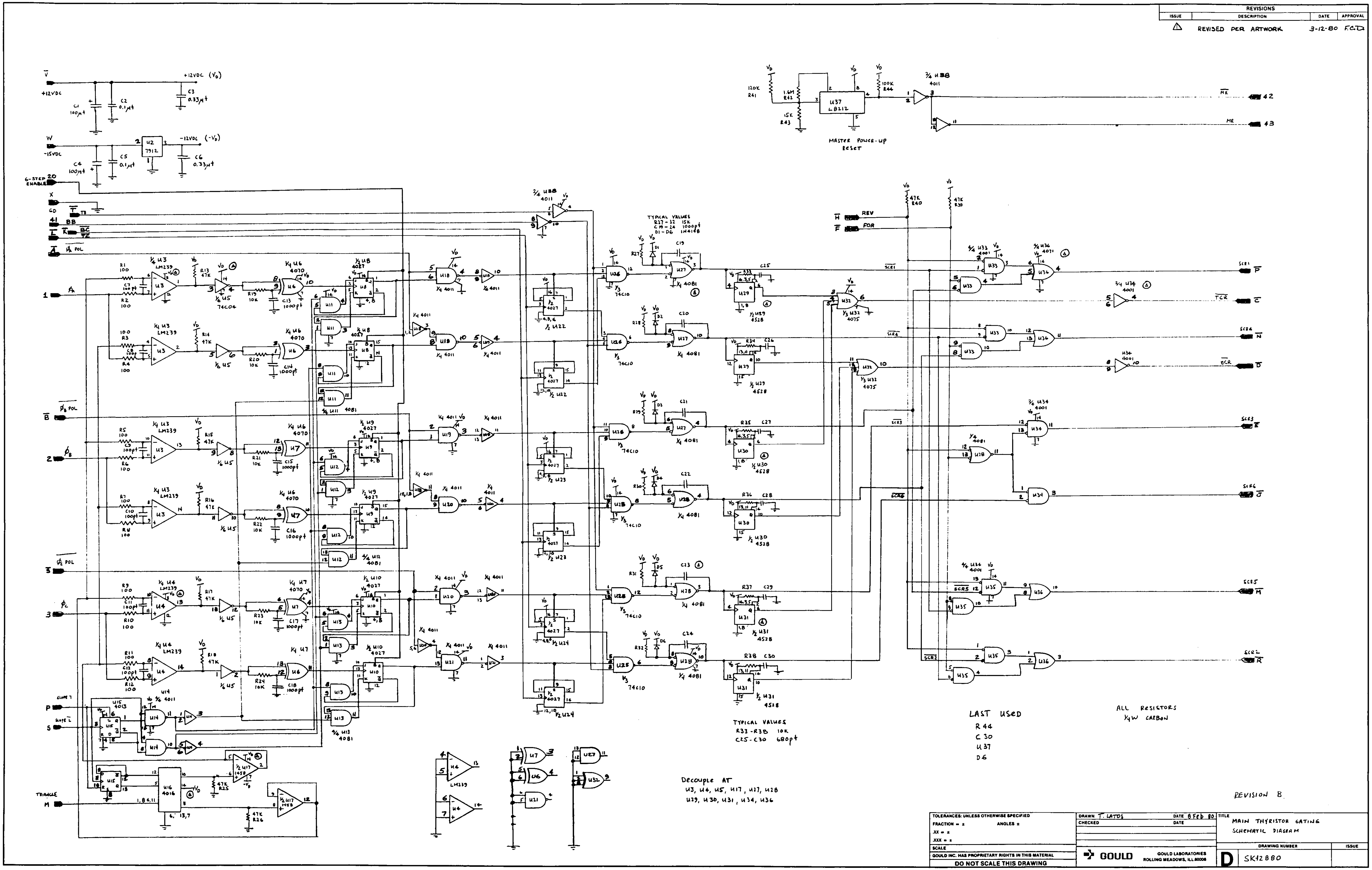
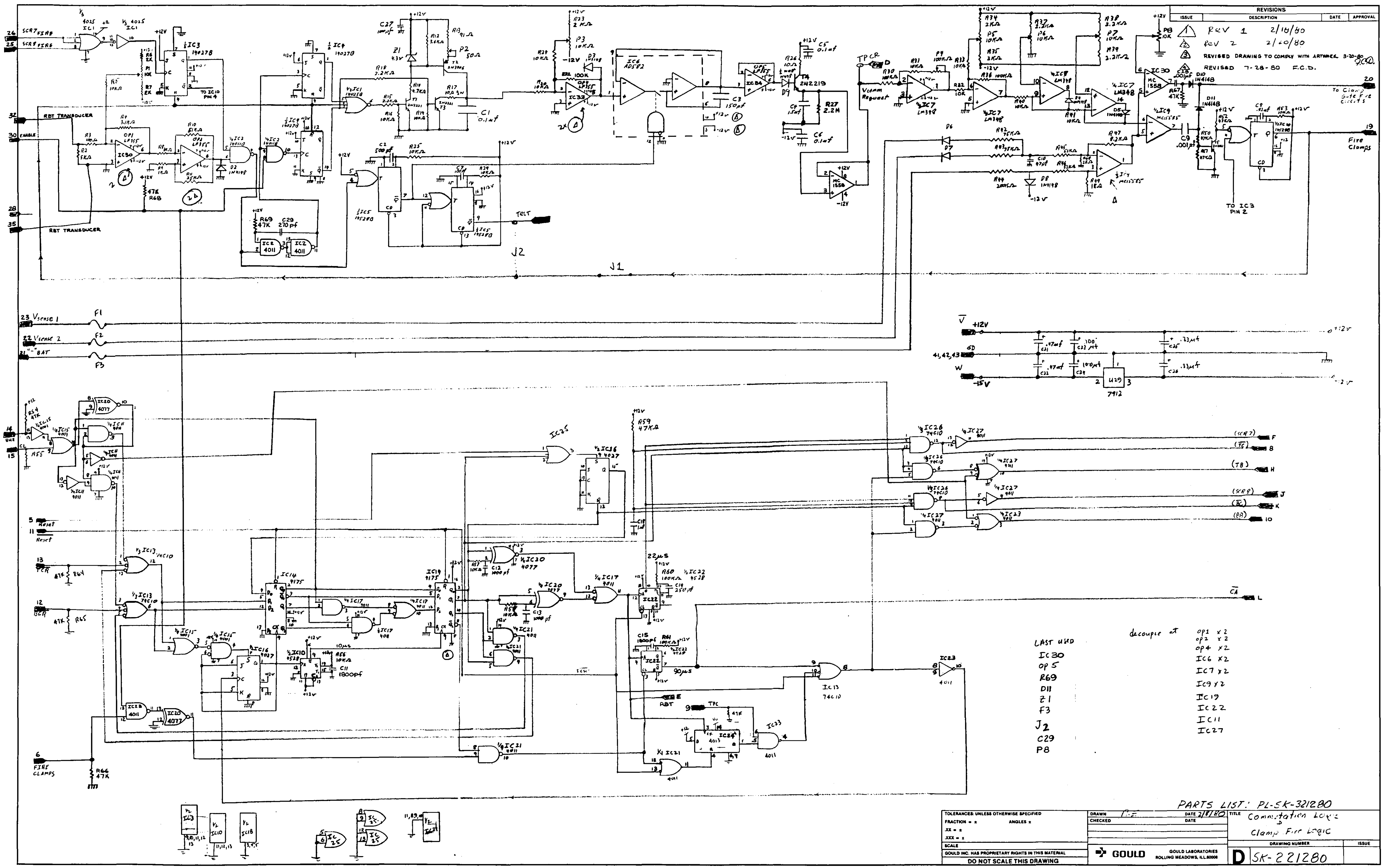
DO NOT SCALE THIS DRAWING
DRAWN KB DATE 2-8-80
CHECKED DATE
GOULD
GOULD LABORATORIES ROLLING MEADOWS, ILL.60008
TITLE SCHEMATIC DIAGRAM SIGNAL INTERFACE
DRAWING NUMBER ISSUE
D SK-22380

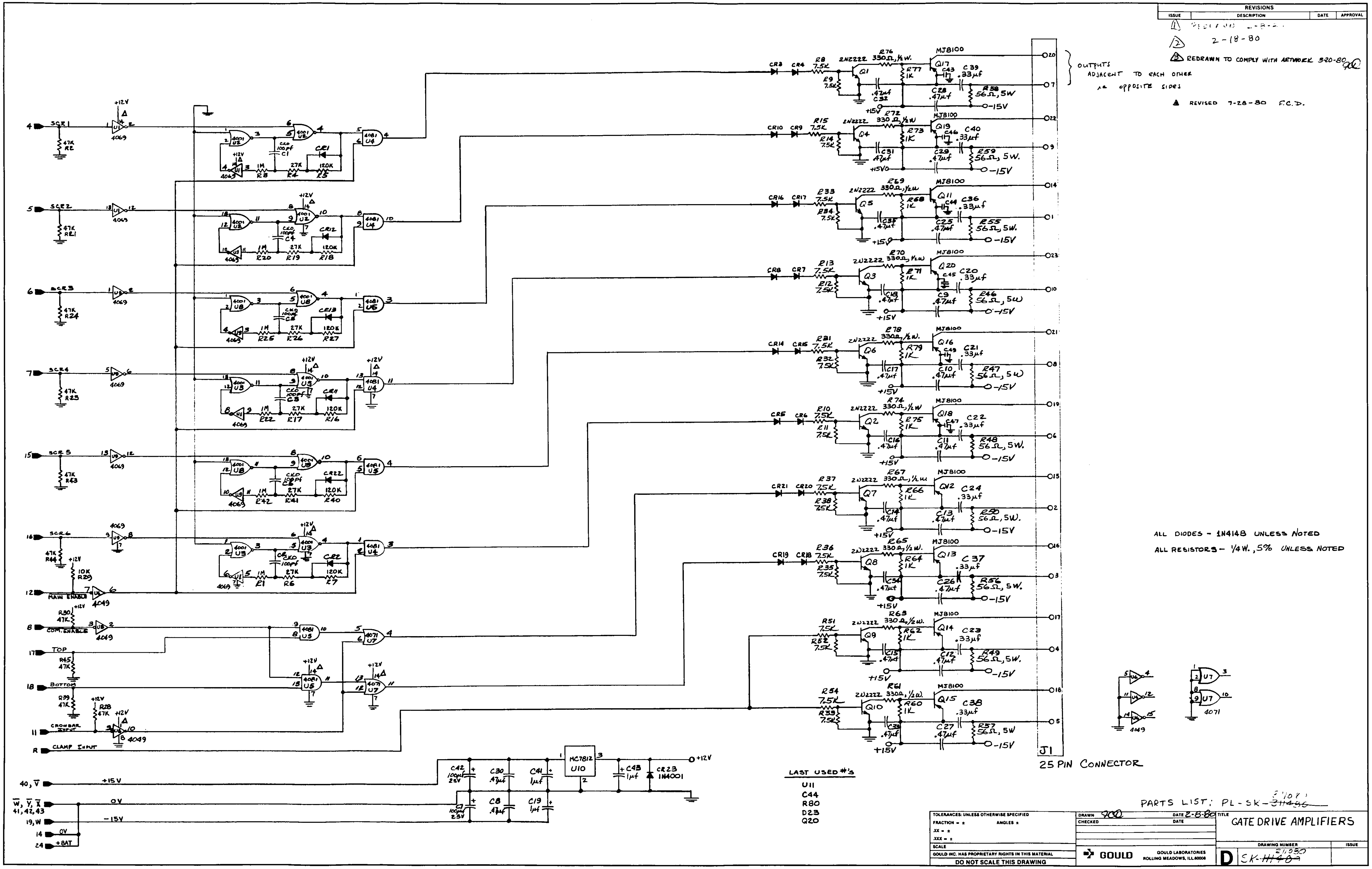

REVISIONS
ISSUE
DESCRIPTION
DATE
APPROVAL
REVISED 3/4/80
NOTE:
ALL DISCRETE RESISTORS 1/4 WATT ± 5% UNLESS OTHERWISE NOTED
* INDICATES PINOUTS MUST BE AS SHOWN
LAST USED - U30, C44, R63, D8
PARTS LIST: PL-SK-22480
TOLERANCES: UNLESS OTHERWISE SPECIFIED
FRACTION ±
ANGLES ±
SCALE
GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL
DO NOT SCALE THIS DRAWING
DRAWN
CHECKED
DATE
GOULD
GOULD LABORATORIES
ROLLING MEADOWS, ILL.
TITLE
FREQUENCY CONTROL
DRAWING NUMBER
D
SK-22480
FTACH - L
FMIN - 36
TREV - 5
TFWD - 15
SFWD - 7
SFWD - 8
(SELECT)
SREV - 9
ACD - N
(ACCEL)
ACW - P
ACG - R
BKP - 12
(BRAKE)
BKW - 13
BKG - 14
TACH - 6
CSLIP - K
FWD - H
REV - J
SLIP D - M
SLIP M - N
HIGH FREQ LIMIT
LOW FREQ LIMIT
NOTE: SUPPLY
FSLIP
(0 → 20.16 KHZ)
(8064 HZ → 1.073 MHZ)
500 HZ → 1.64 KHZ
MC14046
MC14011
MC14013
MC14027
MC14051
MC14029
MC14070
MC14528
MC14175
MC1455U
A-8404
LM348
74C00
74C04
74C10
AD537
NE5018
MC7912
+15V
+12
-12
+5V


REVISIONS
ISSUE
DESCRIPTION
DATE
APPROVAL
UPDATED PER ARTWORK 3-11-80 F.D.
REVISED 7-28-80
+12VDC
+12VDC (V_D)
+5VDC (V_C)
-15VDC
-12VDC ($-V_D$)
-5VDC (V_B)
SINE CLOCK
RESET
FLAG
SINE AMPLITUDE (0.5V-2.5V)
TRIANGLE CLOCK
TRIANGLE AMPLITUDE
TRIANGLE OUT
LAST DESIGNATIONS
U34
R14
C16
D5
PARTS LIST: PL-SK-31880
TOLERANCES: UNLESS OTHERWISE SPECIFIED
GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL
DO NOT SCALE THIS DRAWING
DRAWN T. LATOS
DATE 2/8/80
CHECKED
TITLE SINE-TRIANGLE GENERATOR
SCHEMATIC DIAGRAM
GOULD
GOULD LABORATORIES ROLLING MEADOWS, ILL. 60008
DRAWING NUMBER
ISSUE
D
SK-21880

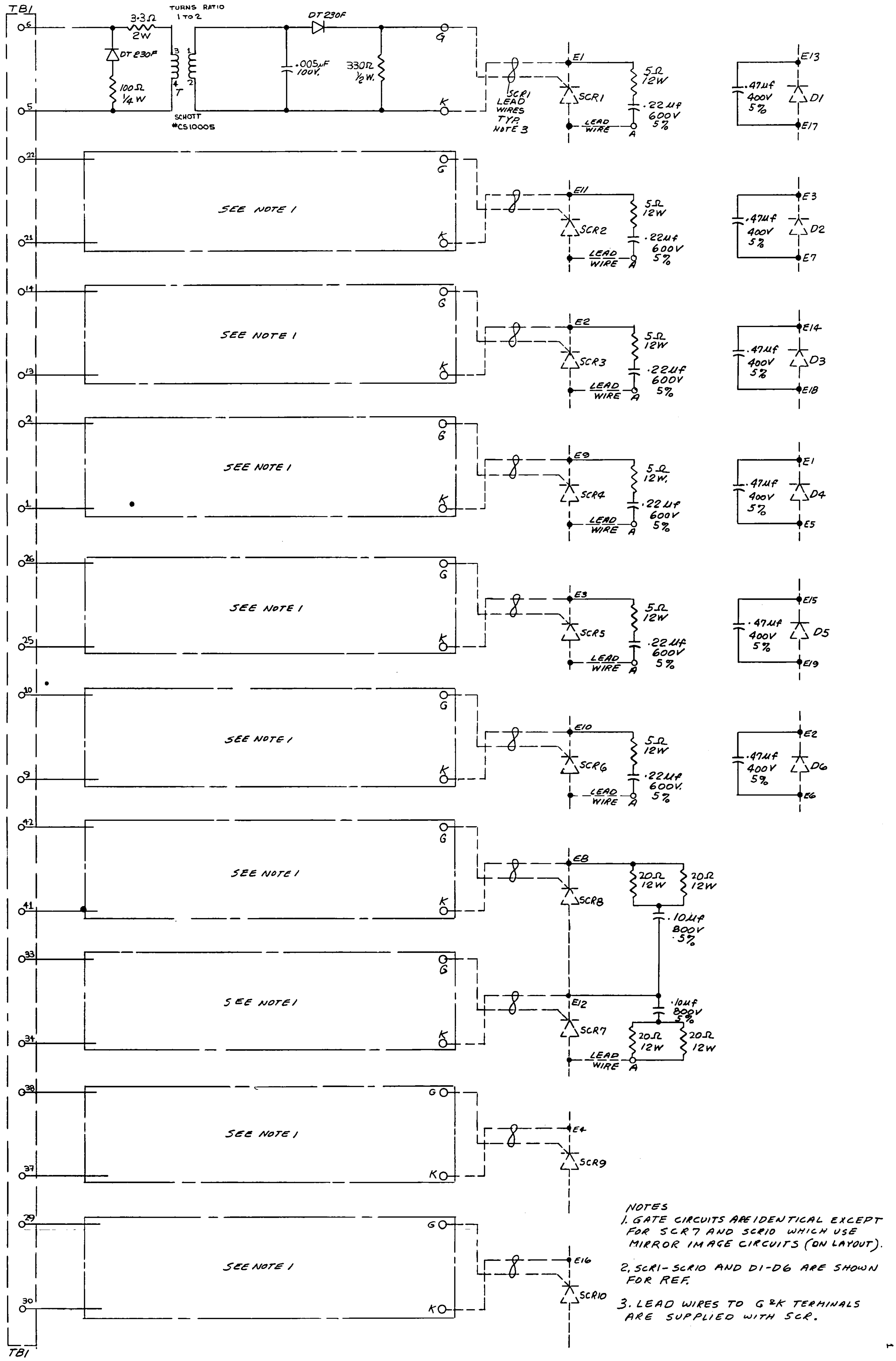


REVISIONS
REVISED PER ARTWORK 3-12-80
MASTER POWER-UP RESET
TYPICAL VALUES R27-32 15K C19-24 1000pf D1-D6 1N4148
LAST USED R44 C30 U37 D6
ALL RESISTORS 1/4W CARBON
TYPICAL VALUES R33-R38 10K C25-C30 680pf
Decouple AT U3, U4, U5, U17, U27, U28 U29, U30, U31, U34, U36
REVISION B
TOLERANCES: UNLESS OTHERWISE SPECIFIED
GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL
DO NOT SCALE THIS DRAWING
DRAWN T. LATOS DATE 8 Feb 80
GOULD
GOULD LABORATORIES ROLLING MEADOWS, ILL.
MAIN THYRISTOR GATING SCHEMATIC DIAGRAM
D SK12880


REVISIONS
ISSUE
DESCRIPTION
DATE
APPROVAL
Rev 1 2/16/80
Rev 2 2/20/80
REVISED DRAWING TO COMPLY WITH ARTWORK 3-20-80
REVISED 7-28-80 F.C.D.
SCR7 FIRE
SCR8 FIRE
RBT TRANSDUCER
ENABLE
23 Vsense 1
22 Vsense 2
F1
F2
F3
J1
J2
Fire Clamps
To Clamp Gate Fire Circuits
TO IC3 PIN 2
Vcomm Request
LAST USED
IC30
OP5
R69
D11
Z1
F3
J2
C29
P8
decouple at
Reset
FIRE CLAMPS
PARTS LIST: PL-SK-321280
TOLERANCES: UNLESS OTHERWISE SPECIFIED
FRACTION ± ANGLES ±
SCALE
GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL
DO NOT SCALE THIS DRAWING
DRAWN
CHECKED
DATE 2/8/80
TITLE Commutation Logic
Clamp Fire Logic
GOULD
GOULD LABORATORIES ROLLING MEADOWS, ILL. 60008
DRAWING NUMBER
ISSUE
D SK-221280



REVISIONS
2-18-80
REDRAWN TO COMPLY WITH ARTWORK 3-20-80
REVISED 7-28-80 F.C.D.
OUTPUTS ADJACENT TO EACH OTHER ARE OPPOSITE SIDES
SCR1
SCR2
SCR3
SCR4
SCR5
SCR6
MAIN ENABLE
COM. ENABLE
TOP
BOTTOM
CROWBAR INPUT
CLAMP INPUT
+15V
0V
-15V
+BAT
MC7812 U10
CR23 1N4001
+12V
2N2222
MJ8100
330Ω, 1/2W.
56Ω, 5W.
.33μf
.47μf
25 PIN CONNECTOR
J1
ALL DIODES - 1N4148 UNLESS NOTED
ALL RESISTORS - 1/4W., 5% UNLESS NOTED
LAST USED #'s
U11
C44
R80
D23
Q20
PARTS LIST: PL-SK-
TOLERANCES: UNLESS OTHERWISE SPECIFIED
GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL
DO NOT SCALE THIS DRAWING
GOULD
GOULD LABORATORIES ROLLING MEADOWS, ILL.
DRAWN
DATE 2-8-80
CHECKED
GATE DRIVE AMPLIFIERS
DRAWING NUMBER
D SK-



PARTS LIST: SK-211979

REVISIONS

ISSUE	DESCRIPTION	DATE	APPROVAL
1	CIRCUIT CHANGES	7/21/80	

TOLERANCES: UNLESS OTHERWISE SPECIFIED
FRACTION ± ANGLES ±
.XX ±
.XXX ±
SCALE

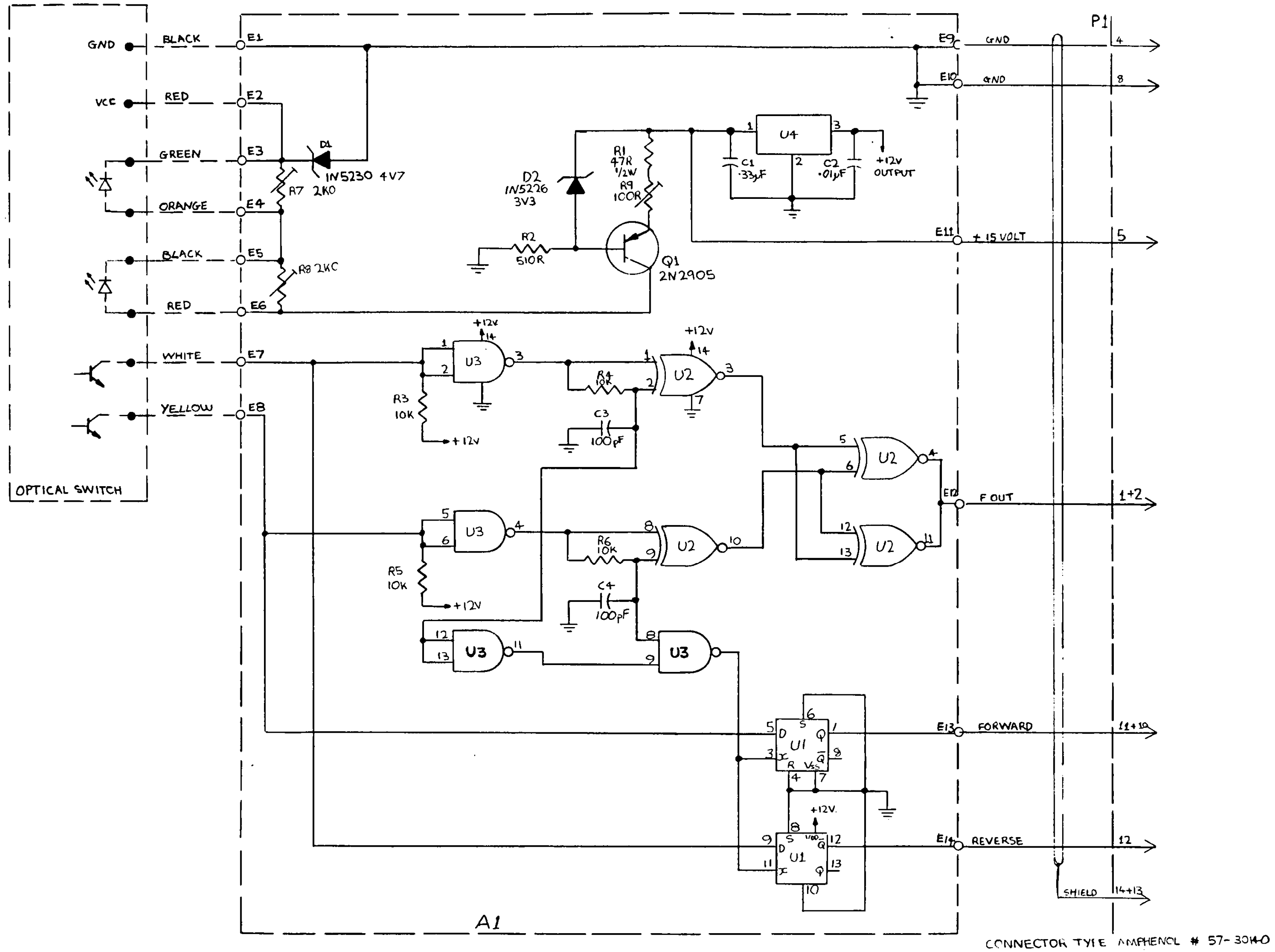
DRAWN KB DATE 11-8-79
CHECKED

GOULD
GOULD LABORATORIES ROLLING MEADOWS, ILL. 60008

TITLE PARTS LIST: PL-SK-211979
SCHEMATIC DIAGRAM
GATE FIRING & SNUBBER CIRCUITS

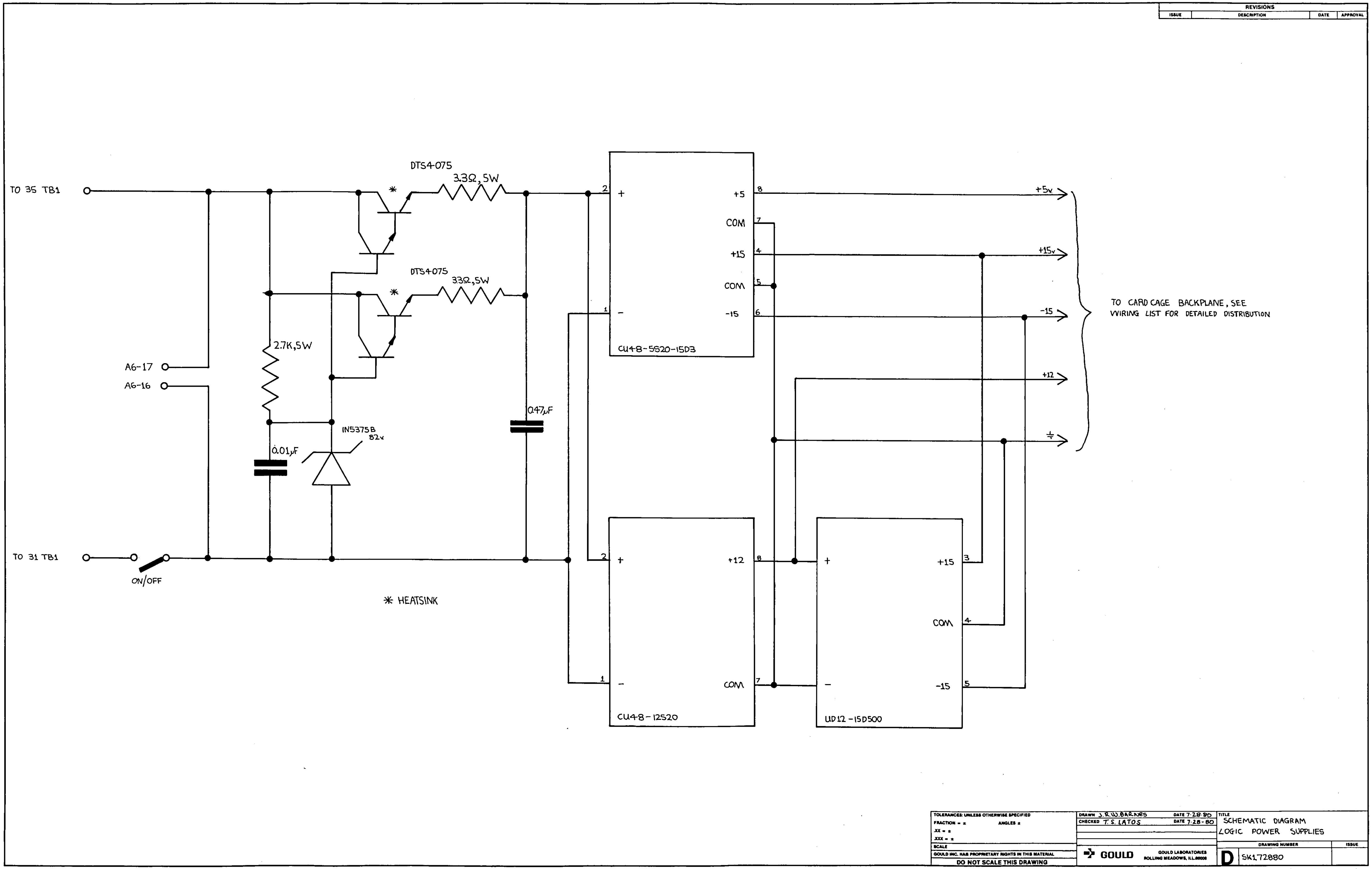
DRAWING NUMBER D SK-111979

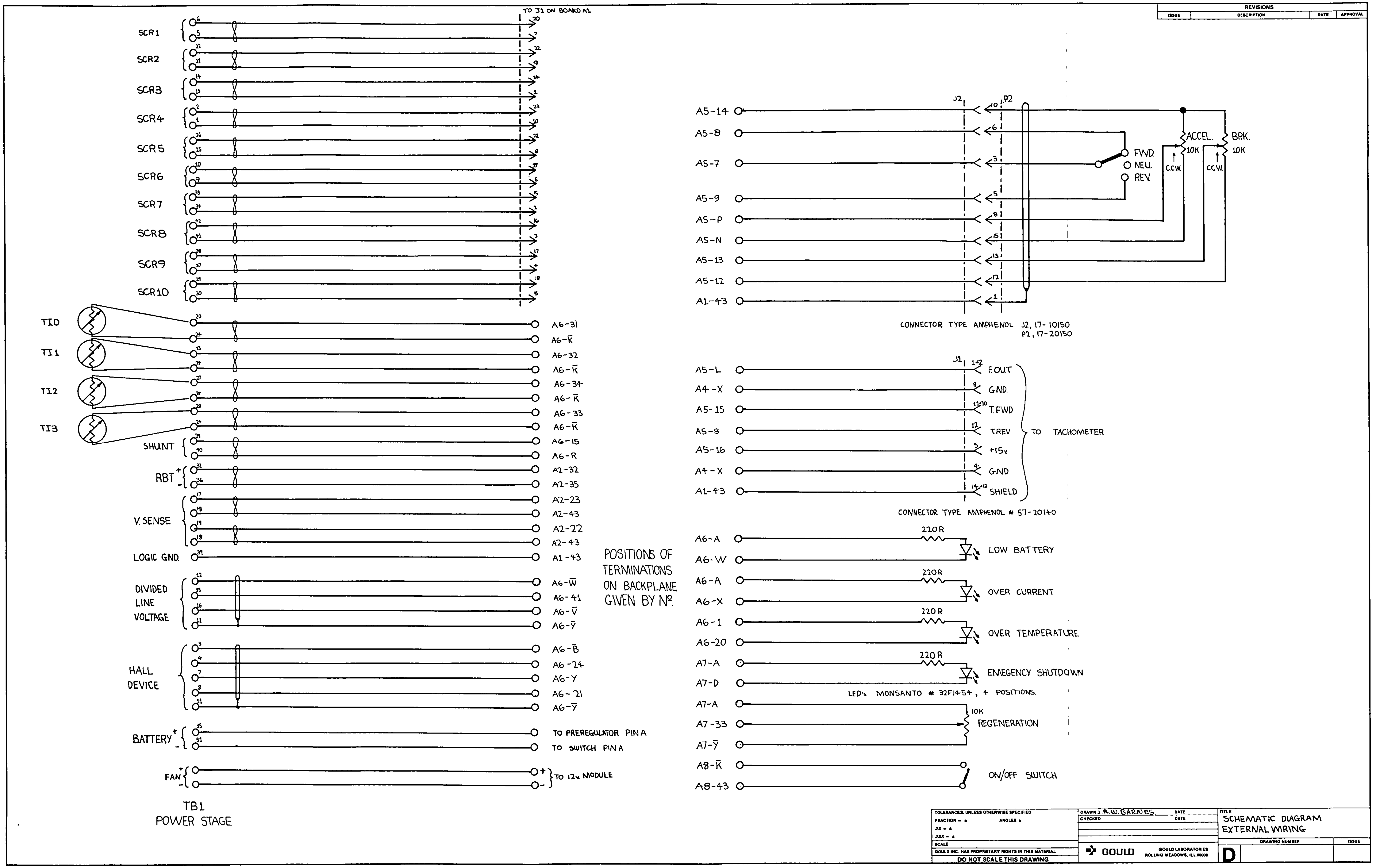
REVISIONS			
ISSUE	DESCRIPTION	DATE	APPROVAL
2	COMPONENT CHANGES	[illegible]	



NOTES:
1) ALL RESISTORS 1/8W UNLESS SPECIFIED
2) U1 CD4013B
U2 CD4077B
U3 CD4011B
U4 MC7812

TOLERANCES: UNLESS OTHERWISE SPECIFIED FRACTION = ± ANGLES ± .XX = ± .XXX = ±	DRAWN JRW GARNES DATE 7-18-90 CHECKED T. LATOS DATE [illegible]	TITLE SCHEMATIC DIAGRAM A1 [illegible]
SCALE		DRAWING NUMBER / ISSUE
GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL DO NOT SCALE THIS DRAWING	GOULD — GOULD LABORATORIES ROLLING MEADOWS, ILL.60008	D


REVISIONS
ISSUE
DESCRIPTION
DATE
APPROVAL
TO 35 TB1
TO 31 TB1
ON/OFF
A6-17
A6-16
DTS4-075
3.3Ω, 5W
DTS4-075
3.3Ω, 5W
2.7K, 5W
0.01μF
IN5375B
82v
0.47μF
✳ HEATSINK
CU48-5S20-15D3
CU48-12S20
UD12-15D500
+5v
+15v
-15
+12
TO CARD CAGE BACKPLANE, SEE WIRING LIST FOR DETAILED DISTRIBUTION
TOLERANCES: UNLESS OTHERWISE SPECIFIED
DRAWN J.R.W. BARNES DATE 7-28-80
CHECKED T.S. LATOS DATE 7-28-80
SCHEMATIC DIAGRAM
LOGIC POWER SUPPLIES
GOULD
GOULD LABORATORIES ROLLING MEADOWS, ILL.
DO NOT SCALE THIS DRAWING
D SK172880


REVISIONS
ISSUE
DESCRIPTION
DATE
APPROVAL
TO J1 ON BOARD A1
SCR1
SCR2
SCR3
SCR4
SCR5
SCR6
SCR7
SCR8
SCR9
SCR10
TI0
TI1
TI2
TI3
SHUNT
RBT
V. SENSE
LOGIC GND.
DIVIDED LINE VOLTAGE
HALL DEVICE
BATTERY
FAN
TB1
POWER STAGE
A6-31
A6-K̄
A6-32
A6-K̄
A6-34
A6-K̄
A6-33
A6-K̄
A6-15
A6-R
A2-32
A2-35
A2-23
A2-43
A2-22
A2-43
A1-43
A6-W̄
A6-41
A6-V̄
A6-Ȳ
A6-B̄
A6-24
A6-Y
A6-21
A6-Ȳ
TO PREREGULATOR PIN A
TO SWITCH PIN A
TO 12v MODULE
POSITIONS OF TERMINATIONS ON BACKPLANE GIVEN BY №.
A5-14
A5-8
A5-7
A5-9
A5-P
A5-N
A5-13
A5-12
A1-43
J2
P2
FWD.
NEU.
REV.
ACCEL. 10K
BRK. 10K
C.C.W.
C.C.W.
CONNECTOR TYPE AMPHENOL J2, 17-10150
P2, 17-20150
A5-L
A4-X
A5-15
A5-8
A5-16
A4-X
A1-43
J1
F.OUT
GND.
T.FWD
T.REV
+15v
GND
SHIELD
TO TACHOMETER
CONNECTOR TYPE AMPHENOL # 57-20140
A6-A
A6-W
A6-A
A6-X
A6-1
A6-20
A7-A
A7-D
220R
LOW BATTERY
OVER CURRENT
OVER TEMPERATURE
EMEGENCY SHUTDOWN
LED's MONSANTO # 32F14-54, 4 POSITIONS.
A7-A
A7-33
A7-Ȳ
10K
REGENERATION
A8-K̄
A8-43
ON/OFF SWITCH
TOLERANCES: UNLESS OTHERWISE SPECIFIED
DRAWN J. R. W. BARNES
CHECKED
DATE
SCHEMATIC DIAGRAM
EXTERNAL WIRING
DRAWING NUMBER
SCALE
GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL
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GOULD
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ROLLING MEADOWS, ILL.
D

APPENDIX V

MICROCOMPUTER PROGRAMS

```
                            NAM    ACDRIVE
                            OPT    REL,CRE,P=58,U,G,LLE=82
                            TTL    ***    AC DRIVE - ENGINEERING PROTOTYPE
                      *
                      *     7/30/80 ASSEMBLY DATE: J.R.M.
                      *
                      *     DISK #6      (BACKUP DISK #7)
                      *     ACDRIV10.SA  SOURCE FILE
                      *     ACDRIV10.RO  OBJECT FILE
                      *     ACDRIV10.LO  MEMORY IMAGE FILE
                      *
            0010   A FILE   EQU    $10      PROGRAM VERSION 1.0
                      *
                      *     BSCT = $40
                      *     PSCT = $C800
                      *     DSCT = $CFFF : SET END OF DSCT
                      *     STACK = $(00-3F)
                      *
A 0000                      ASCT
A E400                      ORG    $E400
            E400   A ASCT   EQU    $E400    MOTOROLA MICROMODULE MM01B
                      *
                      *      PARALLEL INTERFACE ADAPTER
                      *
            E400   A PIA1AD EQU    ASCT     DATA DIRECTION REGISTER - ADDR
            E401   A PIA1AC EQU    ASCT+1   CONTROL REGISTER - ADDRESS
            E402   A PIA1BD EQU    ASCT+2   DATA DIRECTION REGISTER - DATA
            E403   A PIA1BC EQU    ASCT+3   CONTROL REGISTER - DATA
                      *
                      *      PROGRAMMABLE TIMER
                      *
            E410   A PTM1CX EQU    ASCT+16  CONTROL #1 AND 3 / NOP
            E411   A PTM2CS EQU    ASCT+17  CONTROL #2 / STATUS
            E412   A PTM1LC EQU    ASCT+18  MSB BUFFER / COUNTER #1
            E413   A PTM1XX EQU    ASCT+19  LATCH #1 / LSB BUFFER
            E414   A PTM2LC EQU    ASCT+20  MSB BUFFER / COUNTER #2
            E415   A PTM2XX EQU    ASCT+21  LATCH #2 / LSB BUFFER
            E416   A PTM3LC EQU    ASCT+22  MSB BUFFER / COUNTER #3
            E417   A PTM3XX EQU    ASCT+23  LATCH #3 / LSB BUFFER
                      *
                      *      MULTIPLEXER ADDRESSES
                      *      (LABEL). - INDICATES LABEL'S MUX ADDRESS
                      *
            0000   A AI     EQU    0
            0000   A REGV.  EQU    AI       REGENERATION CONTROL
            0001   A SLIPM. EQU    AI+1     SLIP MAGNITUDE
            0002   A VBAT.  EQU    AI+2     BATTERY VOLTAGE
            0003   A IBAT.  EQU    AI+3     BATTERY CURRENT
            0004   A AI4.   EQU    AI+4     UNUSED
            0005   A AI5.   EQU    AI+5     UNUSED
            0006   A VHZ.   EQU    AI+6     VOLTS/HZ
            0007   A AI7.   EQU    AI+7     UNUSED
            0008   A AI8.   EQU    AI+8     UNUSED
            0009   A AI9.   EQU    AI+9     UNUSED
            000A   A AI10.  EQU    AI+10    UNUSED
            000B   A AI11.  EQU    AI+11    UNUSED
            000C   A TO0.   EQU    AI+12    TEMPERATURE 0 ,COM. CAP.
            000D   A TO1.   EQU    AI+13    TEMPERATURE 1 ,COM. SCR
```

```
00300 00059            000E  A TO2.    EQU    AI+14     TEMPERATURE 2 ,MAIN SCR BOTTOM
00305 00060            000F  A TO3.    EQU    AI+15     TEMPERATURE 3 ,MAIN SCR TOP BU
00310 00061                    *
00315 00062B 0000                      BSCT
00320 00063                    **
00325 00064                    **   VARIABLE STORAGE LOCATION
00330 00065                    **    NOTE: FULLSCALE (F.S.) INPUT = 10.000V INTO A/
00335 00066                    **
00340 00067B 0000      0001  A VBAT    RMB    1         BATTERY VOLTAGE : 180V F.S. -
00345 00068B 0001      0001  A IBAT    RMB    1         BATTERY CURRENT : 800A F.S. -
00350 00069B 0002      0001  A VHZ     RMB    1         VOLTS/HERTZ : .850V/HZ F.S.
00355 00070B 0003      0001  A SLIPD   RMB    1         SLIP DIRECTION : "1"=POS. :"0"
00360 00071B 0004      0001  A SLIPM   RMB    1         SLIP MAGNITUDE : 10HZ F.S. - .
00365 00072B 0005      0001  A REGV    RMB    1         REGENERATION CONTROL VALUE : M
00370 00073B 0006      0002  A FREQ    RMB    2         TIMER COUNT - 8US / BIT (COUNT
00375 00074                    *
00380 00075B 0008      0001  A DIA     RMB    1         DIGITAL INPUTS PORT A : BIT 7-
00385 00076                    *  OVERCURRENT , UNUSED , UNUSED , FMIN , TACH , REV
00390 00077B 0009      0001  A DIB     RMB    1         DIGITAL INPUTS PORT B : BIT 7-
00395 00078                    *  BIT 1-7 UNUSED , BIT0 = MAIN ENABLE
00400 00079B 000A      0001  A DOB     RMB    1         DIGITAL OUPUTS PORT B : BIT 0-
00405 00080                    *
00410 00081B 000B      0003  A PER     RMB    3         1ST-ROUNDED 8MSB;2ND & 3RD PER
00415 00082B 000E      0001  A SMAXV   RMB    1         SLIP MAX. VALUE -DERIVED
00420 00083B 000F      0001  A CSLIPV  RMB    1         CONTROL: SLIP VALUE
00425 00084B 0010      0002  A KGAIN   RMB    2         ERROR * GAIN CONSTANT 16 BITS
00430 00085B 0012      0002  A ERRA    RMB    2         16BIT ERROR TERM A
00435 00086B 0014      0002  A ERR     RMB    2         16BIT TOTAL ERROR TERM
00440 00087                    *
00445 00088B 0016      0001  A STR     RMB    1         SINE TRIANGLE RATIO CODE
00450 00089B 0017      0001  A STRF    RMB    1         SINE TRIANGLE RATIO FLAG :"1"=
00455 00090B 0018      0002  A INCI    RMB    2         INTEGRAL CORRECTION TERM 16BIT
00460 00091B 001A      0002  A INCP    RMB    2         PROPORTIONAL CORRECTION TERM 1
00465 00092B 001C      0002  A INCPO   RMB    2         PROPORTIONAL SUM
00470 00093B 001E      0002  A INC     RMB    2         LOW SPEED CORRECTION TERM 16BI
00475 00094B 0020      0002  A INCO    RMB    2         LOW SPEED SUM
00480 00095B 0022      0001  A VLOOP   RMB    1         LOOPING COUNTER
00485 00096B 0023      0001  A VSIGNF  RMB    1         VOLTAGE SIGN FLAG - (8BITS OF
00490 00097B 0024      0001  A MODEF   RMB    1         EXECUTIVE MODE FLAG :"1"=CONTR
00495 00098B 0025      0001  A IDIRF   RMB    1         INVERTER DIRECTION FLAG :"1"=F
00500 00099B 0026      0001  A SLIPF   RMB    1         ZERO SLIP FLAG :"0"=NORMAL ;"1
00505 00100B 0027      0001  A REGF    RMB    1         REGEN. SLIP LIMIT FLAG::"0"=NO
00510 00101B 0028      0001  A HOTF    RMB    1         THERMISTOR OVERTEMP FLAG :"0"=
00515 00102B 0029      0001  A SHUTF   RMB    1         EMERGENCY SHUTDOWN DELAY FLAG
00520 00103B 002A      0001  A ICOUNT  RMB    1         COUNTS INTERRUPTS BEFORE RETUR
00525 00104B 002B      0001  A COUNT   RMB    1         LOOP COUNTER
00530 00105B 002C      0001  A TIME    RMB    1         DELAY COUNTER
00535 00106B 002D      0001  A MULT    RMB    1         MULTPLICATION WORKSPACE
00540 00107B 002E      0002  A DIVW    RMB    2         DIVIDER WORKSPACE
00545 00108B 0030      0003  A TEMP    RMB    3         LOOK-UP TABLE WORKSPACE
00550 00109B 0033      0002  A CTEMP   RMB    2         CONTROL: WORKSPACE
00555 00110                    *
00560 00111B 0035      0001  A CPULSE  RMB    1         CONTROL: 2-PULSE VALUE
00565 00112B 0036      0001  A CSINE   RMB    1         CONTROL: SINE VALUE - 10.0V F.
00570 00113B 0037      0001  A CTRIA   RMB    1         CONTROL: TRIANGLE VALUE - 10.0
```

```
00580 00115P 0000                          PSCT
00585 00116                       **
00590 00117                       **
00595 00118                       **    INITIALIZATION ROUTINE
00600 00119                       **
00605 00120                       **
00610 00121P 0000 7E 000F   P START  JMP    INIT     BRANCH AROUND CONSTANT STORAGE
00615 00122                       *
00620 00123                       *    CONSTANTS STORAGE LOCATION
00625 00124                       *
00630 00125P 0003    10     A        FCB    FILE     PROGRAM FILE NUMBER
00635 00126P 0004    5C     A VHZM   FCB    92       .360 V/HZ MACHINE CONSTANT (37
00640 00127P 0005    DC     A KVHZ   FCB    220      256(.860)
00645 00128P 0006    E6     A KMOT   FCB    230      (1.56 V/HZ)/1.732
00650 00129P 0007    E6     A KREG   FCB    230      (1.56 V/HZ)/1.732
00655 00130P 0008    02     A KLOW   FCB    2        2/("256") LOW SPEED GAIN CONST
00660 00131P 0009    54     A KFREQ  FCB    84       16(5.23)
00665 00132P 000A    4C     A KPOT   FCB    76       76/("256")
00670 00133                       *
00675 00134P 000B    64     A IPOMAX FCB    100      PROPORTIONAL SUM MAX. LIMIT <=
00680 00135P 000C    9C     A IPOMIN FCB    -100     PROPORTIONAL SUM MIN. LIMIT >=
00685 00136P 000D    1B     A DIRQ   FCB    $1B      DISABLE IRQ LINE
00690 00137P 000E    5B     A EIRQ   FCB    $5B      ENABLE IRQ LINE
00695 00138                       *
00700 00139                       *
00705 00140P 000F 8E 003F   A INIT   LDS    #$3F     INITIALIZE STACK POINTER
00710 00141                       *
00715 00142                       *    PIA INITIALIZATION SEQUENCE
00720 00143                       *
00725 00144P 0012 7F E401   A        CLR    PIA1AC   SELECT A-DDR
00730 00145P 0015 7F E403   A        CLR    PIA1BC   SELECT B-DDR
00735 00146P 0018 86 FF     A        LDAA   #$FF
00740 00147P 001A B7 E400   A        STAA   PIA1AD   CONFIGURE PA0 -PA7 AS OUTPUTS
00745 00148P 001D B7 E402   A        STAA   PIA1BD   CONFIGURE PB0 -PB7 AS OUTPUTS
00750 00149P 0020 86 3E     A        LDAA   #%00111110
00755 00150P 0022 B7 E401   A        STAA   PIA1AC   CONFIGURE CA1-IN; CA2-OUT (HIG
00760 00151P 0025 86 3E     A        LDAA   #%00111110
00765 00152P 0027 B7 E403   A        STAA   PIA1BC   CONFIGURE CB1-IN; CB2-OUT (HIG
00770 00153P 002A B6 E402   A        LDAA   PIA1BD   CLEAR IRQ FLAG
00775 00154P 002D B6 E400   A        LDAA   PIA1AD   CLEAR IRQ FLAG
00780 00155                       *
00785 00156                       *   PTM INITIALIZATION SEQUENCE
00790 00157                       *
00795 00158P 0030 86 1B     A        LDAA   #%00011011 PULSE WIDTH COMPARISON MODE
00800 00159                       * OUTPUT MASK, IRQ DISABLE, X, X, X, 16BIT COUNT, INT
00805 00160                       * NOTE: IRQ DISABLED ONLY DURING INITIALIZATION ROUTI
00810 00161P 0032 B7 E410   A        STAA   PTM1CX   CONFIGURE TIMER #3
00815 00162P 0035 CE FF9B   A        LDX    #$FF9B   FULL SCALE - 100 US
00820 00163P 0038 FF E416   A        STX    PTM3LC   INITIALIZE COUNTER VALUE
00825 00164P 003B 86 03     A        LDAA   #%00000011 CONTINUOUS OPERATING MODE
00830 00165                       * OUTPUT MASK, IRQ DISABLED, X, X, X, 16BIT COUNT, IN
00835 00166P 003D B7 E411   A        STAA   PTM2CS   CONFIGURE TIMER #2
00840 00167P 0040 86 B2     A        LDAA   #%10110010 SINGLE SHOT MODE
00845 00168                       * OUTPUT ENABLED, IRQ DISABLED, X, X, X, 16BIT COUNT,
00850 00169P 0042 B7 E410   A        STAA   PTM1CX   CONFIGURE TIMER #1
00855 00170P 0045 CE 003C   A        LDX    #$003C   MIN. PULSE WIDTH - 60 US
00860 00171P 0048 FF E412   A        STX    PTM1LC   INITIALIZE COUNTER VALUE
00865 00172P 004B 86 02     A        LDAA   #$02     SETUP TO WRITE TO CR #3
```

```
00173P 004D B7 E411  A        STAA   PTM2CS
00174                      *    CHECK FOR POSSIBLE WATCHDOG RESET
00175P 0050 86 0B    A        LDAA   #$0B      PORT B MUX. ADDRESS
00176P 0052 BD 0473  P        JSR    INPUT
00177P 0055 C5 01    A        BITB   #$01      CHECK MAIN ENABLE BIT
00178P 0057 26 0F 0068        BNE    INIT1     NORMAL POWER-UP RESET
00179P 0059 F6 E411  A        LDAB   PTM2CS    SET-UP TO CLEAR IRQ FLAG
00180P 005C FE E416  A        LDX    PTM3LC    RESET IRQ FLAG
00181P 005F B6 000E  P        LDAA   EIRQ      RECONFIGURE TIMER #3
00182P 0062 B7 E410  A        STAA   PTM1CX    ENABLE IRQ
00183P 0065 7E 00E0  P        JMP    MODE      RE-ENTER EXECUTIVE VIA MODE
00184                      *
00185                      *    MISC. INITIALIZATION
00186                      *
00187P 0068 CE 0000  A INIT1  LDX    #0        INITIALIZE POINTER
00188P 006B C6 80    A        LDAB   #128      SET BYTES TO BE CLEARED
00189P 006D 6F 00    A ZERO   CLR    0,X       CLEAR BYTE
00190P 006F 08                INX              INCREMENT POINTER
00191P 0070 5A                DECB             DECREASE COUNT
00192P 0071 26 FA 006D        BNE    ZERO      NEXT LOCATION
00193                      *    INITIALIZE A/D CONVERTER
00194P 0073 86 00    A        LDAA   #$0
00195P 0075 BD 049B  P        JSR    AIN8
00196                      *
00197                      *    TURN ON PANEL LITES AND WAIT 500MS
00198                      *
00199P 0078 86 81    A        LDAA   #$81      CODE TO ENABLE DOA0
00200P 007A BD 0433  P        JSR    DOUTA     TURN ON "EMERGENCY SHUTDOWN"
00201P 007D 86 78    A        LDAA   #$78      CODE TO ENABLE DOB3-DOB6
00202P 007F BD 0438  P        JSR    DOUTB     TURN ON "LOW BAT","OVERTEMP","
00203P 0082 86 0A    A        LDAA   #10
00204P 0084 97 2C    B        STAA   TIME      SET DELAY FOR 10 X 50MS
00205P 0086 BD 04C4  P        JSR    DELAY     WAIT 500MS - SERVICE WATCHDOG
00206                      *
00207                      *    PRESET DIGITAL OUTPUTS
00208                      *
00209P 0089 86 7F    A        LDAA   #$7F      CODE TO DISABLE "A" OUTPUTS
00210P 008B BD 0433  P        JSR    DOUTA     TURN ALL DRIVERS OFF DOA0-DOA6
00211P 008E 86 08    A        LDAA   #$08      CODE FOR STR=81 & REMAINING "B
00212P 0090 97 0A    B        STAA   DOB       SAVE PRE-SET STATE
00213P 0092 97 16    B        STAA   STR       SAVE SINE-TRIANGLE RATIO
00214P 0094 BD 0438  P        JSR    DOUTB     SET DRIVERS DOB0-DOB6
00215                      *    ZERO VOLTAGE & INITIALIZE ENERGY CONTROL
00216P 0097 BD 04F1  P        JSR    ZVOLT
00217                      *    RESET CURRENT LIMIT INDICATOR
00218P 009A C6 0C    A        LDAB   #$0C
00219P 009C BD 043D  P        JSR    DEVSEL
00220                      *    RUN SYSTEM SAFETY CHECK
00221P 009F BD 0376  P        JSR    SAFETY
00222                      *    RING COMMUTATION CIRCUIT
00223P 00A2 BD 04DA  P        JSR    RCOM
00224P 00A5 86 10    A        LDAA   #$10      COMM SELECT CODE
00225P 00A7 BD 0433  P        JSR    DOUTA     DISABLE COMM'S
00226                      *    SERVICE WATCH DOG TIMER
00227P 00AA BD 0496  P        JSR    WDOG
00228                      *    ENABLE IRQ
00229P 00AD F6 E411  A        LDAB   PTM2CS    SET-UP TO CLEAR IRQ FLAG
00230P 00B0 FE E416  A        LDX    PTM3LC    RESET IRQ FLAG
```

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Ø1160 ØØ231P ØØB3 B6 ØØØE  P        LDAA   EIRQ      RECONFIGURE TIMER #3
Ø1165 ØØ232P ØØB6 B7 E41Ø  A        STAA   PTM1CX    ENABLE IRQ
Ø117Ø ØØ233                    *   ENTER EXECUTIVE ROUTINE
Ø1175 ØØ234P ØØB9 7E ØØBC  P        JMP    EXECA
```

```
                          **
                          **     EXECUTIVE ROUTINE
                          **
                          *
                          *      EXECUTIVE "A" ROUTINE - CONTROLLER STANDBY STAT
                          *            VOLTAGE CONTROL DISABLED  (MODEF=0)
                          *
00BC 7F 0024  B EXECA   CLR    MODEF     FLAG STANDBY MODE
00BF 7F 0025  B         CLR    IDIRF     RESET INVERTER DIRECTION FLAG
00C2 7F 002A  B         CLR    ICOUNT    RESET INTERRUPT COUNTER
00C5 BD 04F1  P         JSR    ZVOLT     SET VOLTAGE CONTROLS TO FOR.MI
00C8 86 26    A         LDAA   #$26      FWD,REV,MAINS - SELECT CODE
00CA BD 0433  P         JSR    DOUTA     DISABLE MAINS,FWD,REV
                          *    WAIT 150 MS THEN DISABLE COMM'S - WAIT IF DATA N
00CD BD 0376  P EXECA1  JSR    SAFETY    RUN SAFETY CHECK
00D0 86 03    A         LDAA   #$03
00D2 97 2C    B         STAA   TIME      SET DELAY FOR 3 X 50MS
00D4 BD 04C4  P         JSR    DELAY
00D7 86 10    A         LDAA   #$10      COMM - SELECT CODE
00D9 BD 0433  P         JSR    DOUTA     DISABLE COMM'S
00DC 96 06    B         LDAA   FREQ      CHECK TIMER READING
00DE 27 ED 00CD         BEQ    EXECA1    DATA NOT VALID WAIT
                          *
                          *    EXECUTIVE - MODE SELECTION SEQUENCE
                          *
00E0 96 03    B MODE    LDAA   SLIPD     READ DIRECTION OF TORQUE REQUE
00E2 27 06 00EA         BEQ    MODE1     TORQUE REQUEST NEGATIVE
00E4 D6 04    B         LDAB   SLIPM     READ MAGNITUDE VALUE
00E6 C1 05    A         CMPB   #$05      DOUBLE CHECK FOR VALID REQUEST
00E8 24 0A 00F4         BCC    MODE2     VALID REQUEST
00EA 96 0B    B MODE1   LDAA   PER       READ INVERTER PERIOD
00EC 81 C3    A         CMPA   #$C3      TEST FOR  2.5 HZ
00EE 22 CC 00BC         BHI    EXECA     < 2.5 HZ; RETURN TO STANDBY MO
00F0 D6 24    B         LDAB   MODEF     CHECK PREVIOUS MODE
00F2 27 C8 00BC         BEQ    EXECA     IF STANBY MODE; STAY THERE
00F4 96 08    B MODE2   LDAA   DIA       READ DIGITAL INPUT "A" PORT
00F6 85 10    A         BITA   #$10      CHECK FMIN BIT
00F8 26 20 011A         BNE    MODE4     CIRCUIT ACTIVE ; FMOT < FMIN
00FA 85 08    A         BITA   #$08      CHECK TACH BIT
00FC 27 07 0105         BEQ    MODE3     MOTOR - "REV"
00FE 7D 0025  B         TST    IDIRF     TEST INVERTER DIRECTION
0101 2E 17 011A         BGT    MODE4     INV - "FWD" ; MOTOR - "FWD"
0103 20 05 010A         BRA    MODE3A    STANDBY MODE
0105 7D 0025  B MODE3   TST    IDIRF     TEST INVERTER DIRECTION
0108 2B 10 011A         BMI    MODE4     INV - "REV" ; MOTOR -""REV"
                          * VERIFY TACHOMETER SIGNAL BEFORE ENTERING STANDBY M
010A 96 2A    B MODE3A  LDAA   ICOUNT    CHECK COUNTER FOR PREVIOUS ENT
010C 26 05 0113         BNE    MODE3B    PREVIOUS ENTRY
010E 7C 002A  B         INC    ICOUNT    PRESET COUNTER TO 1
0111 20 0A 011D         BRA    MODE5     RE-ENTER CONTROL MODE
0113 81 04    A MODE3B  CMPA   #$4       WAIT FOR TWO (4/2) INTERRUPTS
0115 25 06 011D         BCS    MODE5     RE-ENTER CONTROL MODE
0117 7E 00BC  P         JMP    EXECA     ENTER STANDBY MODE
011A 7F 002A  B MODE4   CLR    ICOUNT    RESET COUNTER
011D 01         MODE5   NOP              ENTER CONTROL MODE
                          *
                          *    EXECUTIVE "B" ROUTINE - VOLTAGE CONTROL ENABLED
                          *
```

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00294P 011E 96 24      B EXECB  LDAA   MODEF     CHECK PREVIOUS OPERATING MODE
00295P 0120 26 0B 012D          BNE    EXECB1    ALREADY SET UP FOR CONTROL MOD
00296P 0122 BD 04DA    P        JSR    RCOM      ENABLE & RING COMMS
00297P 0125 86 A0      A        LDAA   #$A0      MAIN ENABLE CODE
00298P 0127 BD 0433    P        JSR    DOUTA     ENABLE MAINS
00299P 012A BD 0568    P        JSR    IROT      SET INVERTER DIRECTION & ENABL
00300P 012D 7F 0026    B EXECB1 CLR    SLIPF     RESET SLIP FLAG
00301P 0130 C6 01      A        LDAB   #$01
00302P 0132 96 08      B        LDAA   DIA       READ CONSOLE POSITION
00303P 0134 85 10      A        BITA   #$10      CHECK FMIN BIT
00304P 0136 26 0A 0142          BNE    EXECB2    CIRCUIT ACTIVE ; FMOT < FMIN
00305P 0138 84 06      A        ANDA   #$06      CHECK "REV" BIT 2 ; "FWD" BIT
00306P 013A 9B 25      B        ADDA   IDIRF     "REV" 04+(-1) OR "FWD" 02+(1)
00307P 013C 81 03      A        CMPA   #$3       ONLY VALID RESULT =3
00308P 013E 27 02 0142          BEQ    *+4       INVERTER CONFIGURATION & CONSO
00309P 0140 D7 26      B        STAB   SLIPF     NEUTRAL OR OPPOSITE - SET FOR
00310P 0142 D7 24      B EXECB2 STAB   MODEF     SET MODE FLAG FOR CONTROL
00311P 0144 BD 0496    P        JSR    WDOG      RESET WATCHDOG TIMER
00312                    *    RUN SYSTEM SAFETY CHECK - AND RETURN TO MODE SEL
00313P 0147 BD 0376    P        JSR    SAFETY
00314P 014A 7E 00E0    P        JMP    MODE


00316                    **
00317                    **     EMERGENCY SHUTDOWN
00318                    **
00319P 014D 86 81      A ESHUTD LDAA   #$81      "EMERGENCY SHUTDOWN" LED CODE
00320P 014F BD 0433    P        JSR    DOUTA     TURN LED ON
00321                    **
00322                    **     NORMAL SHUTDOWN - DISABLE IRQ
00323                    **
00324P 0152 B6 000D    P SHUTD  LDAA   DIRQ      RECONFIGURE TIMER #3
00325P 0155 B7 E410    A        STAA   PTM1CX    DISABLE IRQ
00326P 0158 96 0A      B        LDAA   DOB
00327P 015A BD 0438    P        JSR    DOUTB     OUTPUT TO REQUIRED LED'S
00328P 015D 86 20      A        LDAA   #$20      MAIN'S SELECT CODE
00329P 015F BD 0433    P        JSR    DOUTA     DISABLE MAINS
00330P 0162 BD 04DA    P        JSR    RCOM      FORCE COMMUTATE MAINS DEVICES
00331P 0165 86 10      A        LDAA   #$10      COMM'S SELECT CODE
00332P 0167 BD 0433    P        JSR    DOUTA     DISABLE COMM'S
00333P 016A BD 04F1    P        JSR    ZVOLT     ZERO VOLTAGE CONTROLS
00334P 016D BD 0496    P SHUTD1 JSR    WDOG      SERVICE WATCHDOG TIMER
00335P 0170 20 FB 016D          BRA    SHUTD1    LOOP FOREVER
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01690 00337                       **
01695 00338                       **    INTERRUPT SERVICE ROUTINE
01700 00339                       **
01705 00340P 0172 B6 000D   P INT      LDAA   DIRQ      DISABLE IRQ CODE
01710 00341P 0175 B7 E410   A          STAA   PTM1CX    DISABLE IRQ
01715 00342P 0178 FE E411   A          LDX    PTM2CS    READ STATUS
01720 00343P 017B FE E416   A          LDX    PTM3LC    READ TIMER AND CLEAR IRQ FLAG
01725 00344P 017E DF 06     B          STX    FREQ      SAVE RAW VALUE
01730 00345P 0180 78 002A   B          ASL    ICOUNT    ADVANCE INTERRUPT COUNTER (IX2
01735 00346P 0183 86 05     A          LDAA   #VHZ.     V/HZ MUX ADDRESS
01740 00347P 0185 BD 049B   P          JSR    AIN8      READ LINE TO LINE VOLT/HZ SIGN
01745 00348P 0188 D7 02     B          STAB   VHZ       SAVE RAW VALUE
01750 00349P 018A 86 01     A          LDAA   #SLIPM.   SLIP MAGNITUDE MUX. ADDRESS
01755 00350P 018C BD 049B   P          JSR    AIN8      READ ACCELERATOR/BRAKE POSITIO
01760 00351P 018F D7 04     B          STAB   SLIPM     SAVE RAW VALUE
01765 00352P 0191 86 0A     A          LDAA   #$0A      DIGITAL INPUT SELECT CODE
01770 00353P 0193 BD 0473   P          JSR    INPUT     READ SLIP DIRECTION
01775 00354P 0196 C4 01     A          ANDB   #$01      MASK OFF SLIP DIRECTION BIT
01780 00355P 0198 D7 03     B          STAB   SLIPD     SAVE RAW VALUE
01785 00356                       *   CALCULATE CYCLE PERIOD FROM TIMER RAW DATA
01790 00357P 019A 96 06     B INT1     LDAA   FREQ      RAW 8MSB
01795 00358P 019C D6 07     B          LDAB   FREQ+1    RAW 8LSB
01800 00359P 019E BD 06D1   P          JSR    COM16     FORM 16BIT 2'S COMPLEMENT
01805 00360P 01A1 97 0C     B          STAA   PER+1     SAVE PERIOD 8MSB
01810 00361P 01A3 D7 0D     B          STAB   PER+2     SAVE PERIOD 8LSB
01815 00362P 01A5 2A 01 01A8           BPL    *+3
01820 00363P 01A7 4C                   INCA             ROUND 8MSB
01825 00364P 01A8 25 0A 01B4           BCS    INT1A     OVERFLOW
01830 00365P 01AA 97 0B     B          STAA   PER       SAVE ROUNDED 8MSB
01835 00366P 01AC 81 FF     A          CMPA   #$FF      INVALID DATA (FREQ <= 2HZ)
01840 00367P 01AE 27 04 01B4           BEQ    INT1A     RETURN
01845 00368                       *   CHECK EXECUTIVE OPERATING MODE
01850 00369P 01B0 96 24     B          LDAA   MODEF     READ MODE
01855 00370P 01B2 26 03 01B7           BNE    *+5       CONTROL MODE
01860 00371P 01B4 7E 0368   P INT1A    JMP    INTE      STANDBY MODE
01865 00372                       *   DETERMINE SINE TRIANGLE RATIO AND UPDATE
01870 00373P 01B7 BD 05FF   P          JSR    SINTR     LOOKUP RATIO VALUE
01875 00374P 01BA D6 17     B          LDAB   STRF      CHECK RATIO CHANGE FLAG
01880 00375P 01BC 27 09 01C7           BEQ    INT2      NO CHANGE-CONTINUE
01885 00376P 01BE 96 0A     B          LDAA   DOB       READ CURRENT STATUS OF "B" POR
01890 00377P 01C0 84 70     A          ANDA   #$70      RETAIN DOB4-DOB6
01895 00378P 01C2 9A 16     B          ORAA   STR       INSERT NEW RATIO VALUE
01900 00379P 01C4 BD 0438   P          JSR    DOUTB     UPDATE PORT WITH NEW RATIO VAL
01905 00380                       *   UPDATE SLIP MAXIMUN
01910 00381P 01C7 BD 0585   P INT2     JSR    SMAX
01915 00382P 01CA 96 0E     B          LDAA   SMAXV     READ SLIP MAX. VALUE
01920 00383P 01CC 91 04     B          CMPA   SLIPM     COMPARE REQUESTED VALUE TO LIM
01925 00384P 01CE 25 02 01D2           BCS    *+4       USE MAX. VALUE
01930 00385P 01D0 96 04     B          LDAA   SLIPM     USE REQUESTED VALUE
01935 00386P 01D2 97 0F     B          STAA   CSLIPV    SAVE IN CONTROL VALUE

01945 00388                       *
01950 00389                       *     ERROR CALCULATIONS
01955 00390                       *         ALL CALCULATIONS 8BIT MAGNITUDE
01960 00391                       *         SIGN INFORMATION IN CORRESPONDING UPPER BYT
01965 00392                       *              ERROR = VHZM - VHZ + KMOT (FSLIP/FINV)
01970 00393                       *         OR   ERROR = VHZM - VHZ - KREG (FSLIP/FINV)
01975 00394                       *         DEPENDING UPON SIGN OF TORQUE REQUEST (SLIP
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01980 00395                    *         FINV LIMITED TO 25HZ MAXIMUM FOR CALCULATIO
01985 00396                    *          RESULT: ERR =SIGN BIT ; ERR+1 = MAGNITUDE
01990 00397                    *
01995 00398                    *    DETERMINE NO LOAD ERROR TERM "A"
02000 00399P 01D4 96 02      B CTRL    LDAA   VHZ       READ PRESENT V/HZ SIGNAL
02005 00400P 01D6 F6 0005    P         LDAB   KVHZ      SCALE FACTOR
02010 00401P 01D9 BD 0687    P         JSR    MP8       SCALE V/HZ (8MSB -"A" REG)
02015 00402P 01DC 2A 01 01DF           BPL    *+3
02020 00403P 01DE 4C                   INCA             ROUND 8MSB
02025 00404P 01DF 97 34      B         STAA   CTEMP+1   SAVE MAGNITUDE ( VHZ * KVHZ )
02030 00405P 01E1 7F 0033    B         CLR    CTEMP     SET POSITIVE SIGN
02035 00406P 01E4 F6 0004    P         LDAB   VHZM      READ V/HZ MACHINE CONSTANT
02040 00407P 01E7 4F                   CLRA             SET POSITIVE SIGN
02045 00408P 01E8 D0 34      B         SUBB   CTEMP+1
02050 00409P 01EA 92 33      B         SBCA   CTEMP     VHZM - ( VHZ * KVHZ )
02055 00410P 01EC D7 13      B         STAB   ERRA+1    SAVE MAGNITUDE OF ERROR TERM "
02060 00411P 01EE 97 12      B         STAA   ERRA      SAVE SIGN ERROR TERM "A"
02065 00412                    *    DETERMINE LOAD DEPENDENT ERROR TERM "B"
02070 00413P 01F0 96 0B      B         LDAA   PER
02075 00414P 01F2 81 14      A         CMPA   #$14      CHECK FOR 25HZ
02080 00415P 01F4 24 02 01F8           BCC    *+4       IF FREQ < 25HZ , CONTINUE
02085 00416P 01F6 86 14      A         LDAA   #$14      SET FREQ TO 25HZ MAX.
02090 00417P 01F8 D6 0F      B         LDAB   CSLIPV    CONTROL SLIP VALUE
02095 00418P 01FA BD 0687    P         JSR    MP8       CSLIPV*PER
02100 00419P 01FD 2A 01 0200           BPL    *+3
02105 00420P 01FF 4C                   INCA             ROUND 8MSB
02110 00421P 0200 F6 0009    P         LDAB   KFREQ     SCALE TO FREQ. RATIO WEIGHTING
02115 00422P 0203 BD 06A6    P         JSR    SCALE     SCALE : CSLIPV*PER* KFREQ = FS
02120 00423P 0206 4D                   TSTA             TEST FOR MAGNITUDE OVERFLOW
02125 00424P 0207 27 02 020B           BEQ    *+4       NO OVERFLOW - CONTINUE
02130 00425P 0209 C6 FF      A         LDAB   #$FF      SET MAX VALUE
02135 00426P 020B 96 03      B         LDAA   SLIPD
02140 00427P 020D 27 05 0214           BEQ    CTRL1     TORQUE REQUEST NEGATIVE
02145 00428P 020F B6 0006    P         LDAA   KMOT      MOTORING GAIN CONSTANT
02150 00429P 0212 20 03 0217           BRA    *+5       CONTINUE
02155 00430P 0214 B6 0007    P CTRL1   LDAA   KREG      REGENERATION GAIN CONSTANT
02160 00431P 0217 BD 0687    P         JSR    MP8       ERRB = (FSLIP/FINV)*KMOT OR KR
02165 00432P 021A 2A 01 021D           BPL    *+3
02170 00433P 021C 4C                   INCA             ROUND 8MSB
02175 00434P 021D 16                   TAB              MAGNITUDE IN B-REG.
02180 00435P 021E 4F                   CLRA             SET POSITIVE SIGN
02185 00436P 021F C1 80      A         CMPB   #$80      (KVHZ-VHZM)  (.860 -.360) V/HZ
02190 00437P 0221 25 02 0225           BCS    CTRL1A    OK,CONTINUE
02195 00438P 0223 C6 70      A         LDAB   #$70      (KVHZ-VHZM-16) SET MAX VALUE W
02200 00439P 0225 7D 0003    B CTRL1A  TST    SLIPD
02205 00440P 0228 26 03 022D           BNE    CTRL2
02210 00441P 022A BD 06D1    P         JSR    COM16     FORM 16BIT 2'S COMPLEMENT
02215 00442                    *    CALCULATE TOTAL ERROR TERM:     (ERRA+ERRB)=ERR
02220 00443P 022D DB 13      B CTRL2   ADDB   ERRA+1
02225 00444P 022F 99 12      B         ADCA   ERRA      ADD A & B ERROR TERMS
02230 00445P 0231 BD 066F    P         JSR    TRUNC     TRUNCATE 16BITS T0 8BITS + SIG
02235 00446P 0234 97 14      B         STAA   ERR       SAVE SIGN
02240 00447P 0236 D7 15      B         STAB   ERR+1     SAVE TOTAL 8BIT ERROR ( ABSOLU

02250 00449                    *
02255 00450                    *    OVERCURRENT CORRECTION SEQUENCE
02260 00451                    *         PROCEDURE FOR UPDATED OF MODULATION INDEX
02265 00452                    *         WHEN ASYNCHRONOUS OVERCURRENT HAS BEEN ACTIVAT
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02270 00453                      *
02275 00454P 0238 86 0A      A INTV    LDAA   #$0A      DEVICE SELECT CODE
02280 00455P 023A BD 0473    P         JSR    INPUT
02285 00456P 023D C5 80      A         BITB   #$80      TEST OVERCURRENT INPUT
02290 00457P 023F 27 10 0251           BEQ    INTV1     NOT IN CURRENT LIMIT - CONTINU
02295 00458P 0241 C6 0C      A         LDAB   #$0C      CURRENT LIMIT DEVICE SELECT CO
02300 00459P 0243 BD 043D    P         JSR    DEVSEL    RESET CURRENT LIMIT INDICATOR
02305 00460P 0246 86 01      A         LDAA   #$01      CORRECTION MAGNITUDE
02310 00461P 0248 97 22      B         STAA   VLOOP     SET MODULATION INDEX UPDATE
02315 00462P 024A 86 FF      A         LDAA   #$FF
02320 00463P 024C 97 23      B         STAA   VSIGNF    SET SIGN FOR DECREASE
02325 00464P 024E 7E 0344    P         JMP    INTV2     SKIP NORMAL CORRECTION SEQUENC

02335 00466                      *
02340 00467                      *    CONTROL SEQUENCE
02345 00468                      *       INTERGRAL TERM CALCULATION : ERR * GAIN/200
02350 00469                      *       TABLE LOOK-UP USED TO DETERMINE MODULATION IN
02355 00470                      *       CORRECTION FACTOR
02360 00471                      *       RESULT: INCI = SIGN OF CORRECTION
02365 00472                      *               INCI+1 = MAGNITUDE OF CORRECTION (IN
02370 00473                      *
02375 00474P 0251 BD 0621    P INTV1   JSR    GAIN      DETERMINE CORRECT GAIN A-REG.
02380 00475P 0254 C6 64      A         LDAB   #100
02385 00476P 0256 D7 2E      B         STAB   DIVW      SET DIVISOR FOR 100
02390 00477P 0258 D6 15      B         LDAB   ERR+1
02395 00478P 025A BD 0687    P         JSR    MP8       (ERR+1)*GAIN
02400 00479P 025D 44                   LSRA
02405 00480P 025E 56                   RORB             PREDIVIDE BY 2; (ERR+1)*GAIN/2
02410 00481P 025F 97 10      B         STAA   KGAIN     SAVE FOR PROPORTIONAL CALCULAT
02415 00482P 0261 D7 11      B         STAB   KGAIN+1
02420 00483P 0263 BD 06D8    P         JSR    DIV       (ERR+1)*GAIN/200
02425 00484P 0266 17                   TBA
02430 00485P 0267 CE 0744    P         LDX    #TBLCOR   1ST TABLE LOCATION
02435 00486P 026A BD 0637    P         JSR    FUNC      CORRECTION LOOK-UP
02440 00487P 026D 17                   TBA              SAVE CORRECTION IN A-REG.
02445 00488P 026E D6 14      B         LDAB   ERR
02450 00489P 0270 D7 18      B         STAB   INCI      SAVE CORRECTION SIGN
02455 00490P 0272 2A 06 027A           BPL    INTV1A
02460 00491P 0274 40                   NEGA             FORM 2'S COMPLEMENT
02465 00492P 0275 26 03 027A           BNE    INTV1A    OK, CONTINUE
02470 00493P 0277 7F 0018    B         CLR    INCI      CORRECTION FACTOR=0, ZERO SIGN
02475 00494P 027A 97 19      B INTV1A  STAA   INCI+1    SAVE CORRECTION FACTOR

02485 00496                      *
02490 00497                      *    CHECK FOR VOLTAGE CONTROL SATURATION
02495 00498                      *       IF SATURATED ZERO PROPORTIONAL TERM
02500 00499                      *
02505 00500P 027C 96 36      B         LDAA   CSINE     SINE AMPLITUDE
02510 00501P 027E 81 0D      A         CMPA   #$0D      CHECK FOR MINIMUN LIMIT
02515 00502P 0280 23 06 0288           BLS    CTLP1     AT LIMIT
02520 00503P 0282 D6 37      B         LDAB   CTRIA     TRIANGLE AMPLITUDE
02525 00504P 0284 C1 00      A         CMPB   #$00      CHECK FOR MAX. LIMIT
02530 00505P 0286 22 05 028D           BHI    CTLP2     OK, CONTINUE
02535 00506P 0288 5F           CTLP1   CLRB
02540 00507P 0289 4F                   CLRA             ZERO PROPORTIONAL TERM
02545 00508P 028A 7E 02E4    P         JMP    CTLP8     SKIP PROPORTIONAL CONTROL

02555 00510                      *
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ØØ511                          *     CONTROL SEQUENCE
ØØ512                          *        PROPORTIONAL TERM CALCULATIONS :
ØØ513                          *        X = ERR * GAIN - INCPO
ØØ514                          *        INCP = TRUNCATION [X]
ØØ515                          *        INCPO = INCPO + INCP
ØØ516                          *         RESULT: INCP = SIGN OF CORRECTION OF MODULAT
ØØ517                          *                 INCP+1 = MAGNITUDE OF CORRECTION (IN
ØØ518                          *         TOTAL SUM SAVED AT INCPO & INCPO+1
ØØ519                          *
ØØ52ØP Ø28D 86 Ø7      A CTLP2  LDAA   #$7       2^7
ØØ521P Ø28F 97 2E      B        STAA   DIVW      PRESET DIVISOR FOR 128
ØØ522P Ø291 5F                  CLRB             ZERO 8LSB
ØØ523P Ø292 96 1D      B        LDAA   INCPO+1   INCPO*256
ØØ524P Ø294 47                  ASRA             MAINTAIN SIGN
ØØ525P Ø295 56                  RORB             SCALE TO KGAIN ACCURACY
ØØ526P Ø296 97 33      B        STAA   CTEMP
ØØ527P Ø298 D7 34      B        STAB   CTEMP+1   SAVE SCALED INCPO
ØØ528P Ø29A 96 1Ø      B        LDAA   KGAIN
ØØ529P Ø29C D6 11      B        LDAB   KGAIN+1   RETRIVE MULTIPLIED ERROR
ØØ53ØP Ø29E 7D ØØ14    B        TST    ERR
ØØ531P Ø2A1 2A Ø3 Ø2A6          BPL    CTLP2A    POSITIVE CORRECTION
ØØ532P Ø2A3 BD Ø6D1    P        JSR    COM16     FORM 16BIT 2'S COMPLEMENT
ØØ533P Ø2A6 DØ 34      B CTLP2A SUBB   CTEMP+1
ØØ534P Ø2A8 92 33      B        SBCA   CTEMP     COMPARE TO SCALED SUM,TERM
ØØ535P Ø2AA 2B Ø8 Ø2B4          BMI    CTLP3     INCPO > GAIN * (ERR+1)
ØØ536P Ø2AC CØ ØØ      A        SUBB   #$ØØ
ØØ537P Ø2AE 82 ØØ      A        SBCA   #Ø        DEAD BAND ADJUSTMENT
ØØ538P Ø2BØ 2B Ø8 Ø2BA          BMI    CTLP4     INCP < Ø
ØØ539P Ø2B2 2Ø Ø8 Ø2BC          BRA    CTLP4+2   INCP > Ø, CONTINUE
ØØ54ØP Ø2B4 CB ØØ      A CTLP3  ADDB   #$ØØ
ØØ541P Ø2B6 89 ØØ      A        ADCA   #Ø        DEAD BAND ADJUSTMENT
ØØ542P Ø2B8 2B Ø2 Ø2BC          BMI    *+4       INCP < Ø
ØØ543P Ø2BA 4F           CTLP4  CLRA             ZERO INCP
ØØ544P Ø2BB 5F                  CLRB             ZERO INCP+1
ØØ545P Ø2BC BD Ø6B7    P        JSR    QDIV      DIVIDE BY 128 (TRUNCATE) DIVIS
ØØ546P Ø2BF DB 1D      B        ADDB   INCPO+1
ØØ547P Ø2C1 99 1C      B        ADCA   INCPO     INCP + INCPO
ØØ548P Ø2C3 2B ØD Ø2D2          BMI    CTLP6     INCP + INCPO < Ø
ØØ549P Ø2C5 26 Ø5 Ø2CC          BNE    CTLP5     INCP + INCPO # Ø
ØØ55ØP Ø2C7 F1 ØØØB    P        CMPB   IPOMAX    CHECK FOR MAX. LIMIT
ØØ551P Ø2CA 23 14 Ø2EØ          BLS    CTLP7     INCP + INCPO <= IPOMAX
ØØ552P Ø2CC 4F           CTLP5  CLRA
ØØ553P Ø2CD F6 ØØØB    P        LDAB   IPOMAX    SET MAX. LIMIT
ØØ554P Ø2DØ 2Ø ØE Ø2EØ          BRA    CTLP7     CONTINUE
ØØ555P Ø2D2 81 FF      A CTLP6  CMPA   #$FF
ØØ556P Ø2D4 26 Ø5 Ø2DB          BNE    CTLP6A    8BIT OVERFLOW
ØØ557P Ø2D6 F1 ØØØC    P        CMPB   IPOMIN    CHECK FOR MIN. LIMIT
ØØ558P Ø2D9 22 Ø5 Ø2EØ          BHI    CTLP7     OK, CONTINUE
ØØ559P Ø2DB 86 FF      A CTLP6A LDAA   #$FF
ØØ56ØP Ø2DD F6 ØØØC    P        LDAB   IPOMIN    SET MINIMUN
ØØ561P Ø2EØ DØ 1D      B CTLP7  SUBB   INCPO+1
ØØ562P Ø2E2 92 1C      B        SBCA   INCPO     DETERMINE DIFFERENCE FROM LIMI
ØØ563P Ø2E4 D7 1B      B CTLP8  STAB   INCP+1    SAVE
ØØ564P Ø2E6 97 1A      B        STAA   INCP      PROPORTIONAL INCREMENT
ØØ565P Ø2E8 DB 1D      B        ADDB   INCPO+1   CALCULATE
ØØ566P Ø2EA 99 1C      B        ADCA   INCPO     PROPORTIONAL SUM
ØØ567P Ø2EC D7 1D      B        STAB   INCPO+1
ØØ568P Ø2EE 97 1C      B        STAA   INCPO     SAVE PROPORTIONAL SUM
```

```
                            *
                            *    CONTROL SEQUENCE
                            *       LOW SPEED ( < 13HZ) CORRECTION FACTOR
                            *       INCO = INCO + KLOW * ERR
                            *       INC = TRUNCATION [INCO]
                            *       INCO = INCO - INC
                            *     RESULT: INCO = REMAINDER
                            *             INC = SIGN
                            *             INC+1 = MAGNITUDE (IN COUNTS)
                            *       REMAINDER FROM INCREMENT SAVED AT INCO & INCO
                            *
P 02F0 96 0B     B                 LDAA   PER       READ PERIOD
P 02F2 81 26     A                 CMPA   #$26      CHECK FOR 12.85HZ
P 02F4 23 39 032F                  BLS    CTLS1     FREQ > 12.85
P 02F6 B6 0008   P                 LDAA   KLOW      GAIN CONSTANT
P 02F9 D6 15     B                 LDAB   ERR+1     ERROR TERM
P 02FB BD 0687   P                 JSR    MP8       KLOW *ERR
P 02FE 7D 0014   B                 TST    ERR       CHECK ERROR SIGN
P 0301 2A 03 0306                  BPL    *+5       OK, POSITIVE
P 0303 BD 06D1   P                 JSR    COM16     CORRECT FOR SIGN OF MULTIPY
P 0306 DB 21     B                 ADDB   INCO+1    SUM REMAINDERS
P 0308 99 20     B                 ADCA   INCO      INCO + KLOW * ERR
P 030A D7 21     B                 STAB   INCO+1    SAVE REMAINDER SUM
P 030C 97 20     B                 STAA   INCO      INCO = INCO + KLOW * ERR
P 030E 2A 08 0318                  BPL    CTLS      OK, POSITIVE SUM
P 0310 BD 06D1   P                 JSR    COM16     FORM COMPLEMENT
P 0313 C6 FF     A                 LDAB   #$FF      SIGN EXTEND
P 0315 40                          NEGA             TRUNCATE 8LSB AND CONVERT SIGN
P 0316 26 01 0319                  BNE    CTLS+1    CONTINUE, IF SIGN EXTEND VALID
P 0318 5F                   CTLS   CLRB             SIGN EXTEND TO 8MSB
P 0319 D7 1E     B                 STAB   INC       SAVE INCREMENT
P 031B 97 1F     B                 STAA   INC+1     INC = TRUNCATION [INCO]
P 031D D6 21     B                 LDAB   INCO+1
P 031F 96 20     B                 LDAA   INCO
P 0321 C0 00     A                 SUBB   #$0       SUBTRACT (INCREMENT X 256) FRO
P 0323 92 1F     B                 SBCA   INC+1
P 0325 D7 21     B                 STAB   INCO+1    SAVE ADJUSTED REMAINDER
P 0327 97 20     B                 STAA   INCO      INCO = INCO - INC
P 0329 D6 1F     B                 LDAB   INC+1
P 032B 96 1E     B                 LDAA   INC
P 032D 20 06 0335                  BRA    CTLS2
P 032F 5F                   CTLS1  CLRB             CLEAR REMAINDER TERMS
P 0330 4F                          CLRA
P 0331 D7 21     B                 STAB   INCO+1
P 0333 97 20     B                 STAA   INCO

                            *
                            *    CONTROL SEQUENCE
                            *       COMBINE ALL CORRECTION TERMS : VLOOP = INCI +
                            *       RESULT: VSIGNF = SIGN OF CORRECTION
                            *               VLOOP = MAGNITUDE OF CORRECTION ( IN
                            *
P 0335 DB 1B     B          CTLS2  ADDB   INCP+1
P 0337 99 1A     B                 ADCA   INCP      INC + INCP
P 0339 DB 19     B                 ADDB   INCI+1    ADD PROPORTIONAL AND INTEGRAL
P 033B 99 18     B                 ADCA   INCI      INC + INCP + INCI
P 033D BD 066F   P                 JSR    TRUNC     TRUNCATE TO 8BITS + SIGN
P 0340 D7 22     B                 STAB   VLOOP     SET CORRECTION FACTOR
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00628P 0342 97 23    B          STAA   VSIGNF    SET CORRECTION DIRECTION

00630P 0344 7D 0022  B INTV2    TST    VLOOP
00631P 0347 27 1F 0368          BEQ    INTE      NO, CORRECTION - RETURN
00632P 0349 BD 04FF  P INTV3    JSR    VCORR     VOLTAGE CORRECTION SUBROUTINE
00633P 034C 7A 0022  B          DEC    VLOOP     DECREMENT LOOP COUNTER
00634P 034F 26 F8 0349          BNE    INTV3     REPEAT UNTIL ZERO
00635                  *
00636                  *    AVOID POOR OPERATING REGION OF VOLTAGE MODULATOR
00637                  *     HARDWARE ( BETWEEN   CSINE/CTRIA =1.8 - 2.5 )
00638                  *       (TEMPORARILY SET FOR NO EFFECT: 8/26/80 J.R.M.
00639P 0351 86 00    A          LDAA   #00       LOWER LIMIT  M.I. = 1.8 (36)
00640P 0353 C6 00    A          LDAB   #00       UPPER LIMIT  M.I. = 2.5 (25)
00641P 0355 91 37    B          CMPA   CTRIA     CHECK CURRENT SETTING OF M.I.
00642P 0357 23 0C 0365          BLS    INTV4     CONTINUE, NOT IN POOR REGION
00643P 0359 D1 37    B          CMPB   CTRIA
00644P 035B 24 08 0365          BCC    INTV4     CONTINUE, NOT IN POOR REGION
00645P 035D 7D 0023  B          TST    VSIGNF    DETERMINE PROPER LIMIT
00646P 0360 27 01 0363          BEQ    *+3       SELECT UPPER LIMIT
00647P 0362 16                  TAB              SELECT LOWER LIMIT
00648P 0363 D7 37    B          STAB   CTRIA     CORRECT SETTING
00649P 0365 BD 053D  P INTV4    JSR    VOUT      OUTPUT NEW VOLTAGE
00650P 0368 0F         INTE     SEI
00651P 0369 FE E411  A          LDX    PTM2CS    READ STATUS
00652P 036C FE E416  A          LDX    PTM3LC    CLEAR IRQ FLAG
00653P 036F B6 000E  P          LDAA   EIRQ      IRQ ENABLE CODE
00654P 0372 B7 E410  A          STAA   PTM1CX    ENABLE IRQ
00655P 0375 3B                  RTI              RETURN TO EXECUTIVE
```

```
00657                          **
00658                          **     SAFETY SUBROUTINE
00659                          **       VERIFIES SAFE CONDITION OF INPUTS ON PORTS A&
00660                          **         PORT A : RESULTS IN EMERGENCY SHUTDOWN
00661                          **         PORT B : RESULTS IN " WARNING" INDICATOR
00662                          **
00663P 0376 86 0A      A SAFETY LDAA   #$0A      DEVICE CODE - CRITICAL INPUTS
00664P 0378 BD 0473    P        JSR    INPUT     READ PORT A INPUTS
00665P 037B D7 08      B        STAB   DIA       SAVE VALUE
00666P 037D C4 00      A        ANDB   #$00      MASK UN-TESTED INPUTS
00667P 037F C8 00      A        EORB   #$00      COMPARE TO SAFE STATE
00668P 0381 27 03 0386          BEQ    SAFET1    OK
00669P 0383 7E 014D    P        JMP    ESHUTD    EMERGENCY SHUTDOWN
00670P 0386 86 0B      A SAFET1 LDAA   #$0B      DEVICE CODE - NON CRITICAL INP
00671P 0388 BD 0473    P        JSR    INPUT     READ PORT B INPUTS
00672P 038B D7 09      B        STAB   DIB       SAVE VALUE
00673P 038D C4 00      A        ANDB   #$00      MASK UN-TESTED INPUTS
00674P 038F C8 00      A        EORB   #$00      COMPARE TO SAFE STATE
00675P 0391 27 06 0399          BEQ    SAFET2    OK
00676P 0393 86 40      A        LDAA   #$40      SYSTEM "WARNING" LED ON
00677P 0395 9A 0A      B        ORAA   DOB       SET BIT #6
00678P 0397 20 04 039D          BRA    *+6
00679P 0399 86 BF      A SAFET2 LDAA   #$BF      SYSTEM "WARNING" LED OFF
00680P 039B 94 0A      B        ANDA   DOB       ZERO BIT #6 ONLY
00681P 039D 97 0A      B        STAA   DOB       SAVE RESULTS
00682                          *
00683                          *    SAFETY:
00684                          *      THERMISTOR LIMIT CHECKING - TABLE : TBLTEM
00685                          *            TWO LEVEL CHECKING
00686                          *             1ST LEVEL : "OVERTEMP" INDICATION
00687                          *             2ND LEVEL : EMERGENCY SHUTDOWN
00688                          *
00689P 039F 86 04      A TEMP0  LDAA   #(ETBLTE-TBLTEM+1)/3 CALCULATE TABLE SI
00690P 03A1 97 2B      B        STAA   COUNT     SAVE SIZE
00691P 03A3 7F 0028    B        CLR    HOTF      CLEAR OVERTEMPERATURE FLAG
00692P 03A6 CE 070E    P        LDX    #TBLTEM   SET POINTER TO 1ST TABLE ENTRY
00693P 03A9 7F 0029    B TEMP1  CLR    SHUTF     PRESET SHUTDOWN FLAG
00694P 03AC A6 00      A        LDAA   0,X       READ MUX. ADDRESS
00695P 03AE BD 049B    P        JSR    AIN8      A/D CONVERT
00696P 03B1 53                  COMB             CORRECT FOR THERMISTOR VOLTAGE
00697P 03B2 E1 02      A        CMPB   2,X       CHECK FOR > TRIP LIMIT
00698P 03B4 23 0C 03C2          BLS    TEMP2     OK - CONTINUE
00699P 03B6 96 29      B        LDAA   SHUTF     DELAY EMERGENCY SHUTDOWN ( TO
00700P 03B8 4C                  INCA             ADVANCE DELAY
00701P 03B9 97 29      B        STAA   SHUTF     SAVE NEW VALUE
00702P 03BB 81 05      A        CMPA   #$5       CHECK FOR DELAY SETTING
00703P 03BD 25 ED 03AC          BCS    TEMP1+3   REREAD INPUT VALUE AND CHECK A
00704P 03BF 7E 014D    P        JMP    ESHUTD    EMERGENCY SHUTDOWN
00705P 03C2 E1 01      A TEMP2  CMPB   1,X       CHECK FOR > WARNING LIMIT
00706P 03C4 23 03 03C9          BLS    TEMP3     OK - CONTINUE
00707P 03C6 7C 0028    B        INC    HOTF      SET OVERTEMPERATURE FLAG
00708P 03C9 08           TEMP3  INX
00709P 03CA 08                  INX              ADVANCE TO
00710P 03CB 08                  INX              NEXT MUX. ADDRESS
00711P 03CC 7A 002B    B        DEC    COUNT     DECREMENT LOOP COUNTER
00712P 03CF 26 D8 03A9          BNE    TEMP1     CHECK NEXT THERMISTOR
00713P 03D1 96 28      B        LDAA   HOTF      TEST OVER TEMPERATURE FLAG
00714P 03D3 27 06 03DB          BEQ    TEMP4     OK- CONTINUE
```

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00715P 03D5 86 20       A        LDAA   #$20      "OVERTEMPERATURE" LED ON - COD
00716P 03D7 9A 0A       B        ORAA   DOB       SET BIT #5
00717P 03D9 20 04 03DF           BRA    *+6       CONTINUE
00718P 03DB 86 DF       A TEMP4  LDAA   #$DF      "OVERTEMPERATURE" LED OFF - CO
00719P 03DD 94 0A       B        ANDA   DOB       RESET BIT #5
00720P 03DF 97 0A       B        STAA   DOB       SAVE RESULTS
00721                     *
00722                     *   SAFETY:
00723                     *       BATTERY VOLTAGE LIMIT TESTING
00724                     *           TWO LEVEL CHECKING
00725                     *              1ST LEVEL : "LOW BATTERY" INDICATOR
00726                     *              2ND LEVEL : EMERGENCY SHUTDOWN
00727                     *
00728P 03E1 7F 0029     B BATT   CLR    SHUTF     PRESET SHUTDOWN FLAG
00729P 03E4 BD 0410     P        JSR    CALCVB    FIND OPEN CIRCUIT BATTERY VOLT
00730P 03E7 C1 91       A        CMPB   #145      CHECK FOR < 102 VOLTS (1.70V/C
00731P 03E9 24 0C 03F7           BCC    BATT1     OK - CONTINUE
00732P 03EB 96 29       B        LDAA   SHUTF
00733P 03ED 4C                   INCA             ADVANCE DELAY
00734P 03EE 97 29       B        STAA   SHUTF     SAVE NEW VALUE
00735P 03F0 81 02       A        CMPA   #$2       CHECK FOR DELAY SETTING
00736P 03F2 25 F0 03E4           BCS    BATT+3    REREAD INPUT VALUE AND CHECK A
00737P 03F4 7E 014D     P        JMP    ESHUTD    EMERGENCY SHUTDOWN
00738P 03F7 C1 9E       A BATT1  CMPB   #158      CHECK FOR < 111 VOLT WARNING (
00739P 03F9 24 06 0401           BCC    BATT2     OK - CONTINUE
00740P 03FB 86 10       A        LDAA   #$10      "LOW BATTERY" LED ON - CODE
00741P 03FD 9A 0A       B        ORAA   DOB       SET BIT #4
00742P 03FF 20 04 0405           BRA    *+6       CONTINUE
00743P 0401 86 EF       A BATT2  LDAA   #$EF      "LOW BATTERY" LED OFF - CODE
00744P 0403 94 0A       B        ANDA   DOB       RESET BIT #4
00745P 0405 0F                   SEI              SET IRQ MASK
00746P 0406 84 70       A        ANDA   #$70
00747P 0408 9A 16       B        ORAA   STR
00748P 040A 97 0A       B        STAA   DOB       SAVE VALUE
00749P 040C BD 0438     P        JSR    DOUTB
00750P 040F 39                   RTS
00751                     **
00752                     **  SUBROUTINE TO CALCULATE BATTERY
00753                     **      OPEN CIRCUIT TERMINAL VOLTAGE : VALUE RETURNE
00754                     **      "B" REG. = VBAT + IBAT * RBAT
00755                     **
00756P 0410 86 00       A CALCVB LDAA   #REGV.    REGENERATION CONTROL MUX. ADDR
00757P 0412 BD 049B     P        JSR    AIN8      A/D CONVERT
00758P 0415 C1 80       A        CMPB   #$80      CHECK FOR MAX LIMIT
00759P 0417 25 02 041B           BCS    *+4       OK
00760P 0419 C6 80       A        LDAB   #$80      SET MAX VALUE
00761P 041B D7 05       B        STAB   REGV      SAVE VALUE
00762P 041D 86 02       A        LDAA   #VBAT.    BATTERY VOLTAGE MUX. ADDRESS
00763P 041F BD 049B     P        JSR    AIN8      A/D CONVERT
00764P 0422 D7 00       B        STAB   VBAT      SAVE VALUE
00765P 0424 86 03       A        LDAA   #IBAT.    BATTERY CURRENT MUX. ADDRESS
00766P 0426 BD 049B     P        JSR    AIN8      A/D CONVERT
00767P 0429 D7 01       B        STAB   IBAT      SAVE VALUE
00768P 042B 54                   LSRB             /2 CORRECT FOR BATTERY RESISTA
00769P 042C DB 00       B        ADDB   VBAT      CORRECT VALUE READ
00770P 042E 24 02 0432           BCC    CALCV1    OK - CONTINUE
00771P 0430 C6 FF       A        LDAB   #$FF      MAGNITUDE OVERFLOW
00772P 0432 39            CALCV1 RTS
```

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03875 00774                      **
03880 00775                      **   DIGITAL OUTPUT SET-UP ROUTINE - "A" REG OUTPUT
03885 00776                      **           PORT "A" DOA0-DOA6 ( SELECT BITS)
03890 00777                      **              DOA7 : (VALUE BIT)
03895 00778                      **           LOGIC "1" SELECTS APPRORIATE OUTPUT (DOA
03900 00779                      **              DOA0 : "EMERGENCY SHUTDOWN" INDICATOR
03905 00780                      **              DOA1 : FWD ENABLE
03910 00781                      **              DOA2 : REV ENABLE
03915 00782                      **              DOA3 : RING COMM'S
03920 00783                      **              DOA4 : COM ENABLE
03925 00784                      **              DOA5 : MAIN ENABLE
03930 00785                      **              DOA6 : ENERGY CONTROL DISABLE
03935 00786                      **
03940 00787P 0433 C6 0E      A DOUTA  LDAB   #$0E      PORT "A" DEVICE SELECT CODE
03945 00788P 0435 7E 044E    P        JMP    OUTPUT    OUTPUT TO PORT


03955 00790                      **
03960 00791                      **   DIGITAL OUTPUT SET-UP ROUTINE - "A" REG OUTPUT
03965 00792                      **           PORT "B" DOB0-DOB6 (VALUE BITS)
03970 00793                      **           LOGIC "1" ENABLES THE FOLLOWING
03975 00794                      **              DOB0 : STR 27
03980 00795                      **              DOB1 : STR 45
03985 00796                      **              DOB2 : STR 63
03990 00797                      **              DOB3 : STR 81
03995 00798                      **              DOB4 : "LOW BATTERY" INDICATOR
04000 00799                      **              DOB5 : "OVERTEMP" INDICATOR
04005 00800                      **
04010 00801P 0438 C6 0D      A DOUTB  LDAB   #$0D      PORT "B" DEVICE SELECT CODE
04015 00802P 043A 7E 044E    P        JMP    OUTPUT    OUTPUT TO PORT


04025 00804                      **
04030 00805                      **   PIA - SELECT CODE OUTPUT  (DEVICE SELECT)
04035 00806                      **         REG "A" ALTERED; REG "B" DEVICE CODE
04040 00807                      **         NON - INTERRUPTIABLE    ( 30 CYCLES )
04045 00808                      **
04050 00809P 043D 0F             DEVSEL SEI              MASK IRQ
04055 00810P 043E F7 E400    A        STAB   PIA1AD    SET DEVICE CODE
04060 00811P 0441 86 36      A        LDAA   #%00110110 CONFIGURE A SIDE
04065 00812P 0443 B7 E401    A        STAA   PIA1AC    CA2 "LOW" ( SELECT )
04070 00813P 0446 86 3E      A        LDAA   #%00111110 RE-CONFIGURE A SIDE
04075 00814P 0448 B7 E401    A        STAA   PIA1AC    CA2 "HIGH" ( DESELECT )
04080 00815P 044B 01                  NOP
04085 00816P 044C 0E                  CLI              CLEAR MASK
04090 00817P 044D 39                  RTS


04100 00819                      **
04105 00820                      **   PIA OUTPUT - "A" OUTPUT; "B" DEVICE CODE
04110 00821                      **        NON - INTERRUPTIABLE    (67 CYCLES)
04115 00822                      **
04120 00823P 044E 0F             OUTPUT SEI              MASK IRQ
04125 00824P 044F 37                  PSHB             SAVE TEMP. DEVICE CODE
04130 00825P 0450 C6 3A      A        LDAB   #%00111010
04135 00826P 0452 F7 E403    A        STAB   PIA1BC    SELECT DATA DIRECTION REGISTER
04140 00827P 0455 C6 FF      A        LDAB   #$FF
04145 00828P 0457 F7 E402    A        STAB   PIA1BD    CONFIGURE PB0-PB7 AS OUTPUTS
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04150 00829P 045A C6 3E     A         LDAB   #%00111110
04155 00830P 045C F7 E403   A         STAB   PIA1BC   SELECT DATA REGISTER
04160 00831P 045F B7 E402   A         STAA   PIA1BD   OUTPUT VALUE
04165 00832P 0462 33                  PULB            RETRIEVE DEVICE CODE
04170 00833P 0463 F7 E400   A         STAB   PIA1AD   SET DEVICE CODE
04175 00834P 0466 86 36     A         LDAA   #%00110110
04180 00835P 0468 B7 E401   A         STAA   PIA1AC   CA2 "LOW" (SELECT)
04185 00836P 046B 86 3E     A         LDAA   #%00111110
04190 00837P 046D B7 E401   A         STAA   PIA1AC   CA2 "HIGH" (DESELECT)
04195 00838P 0470 01                  NOP
04200 00839P 0471 0E                  CLI             CLEAR MASK
04205 00840P 0472 39                  RTS


04215 00842                     **
04220 00843                     **   PIA INPUT "B" SIDE    NON-INTERRUPTIABLE  (56 CY
04225 00844                     **      A-REG. DEVICE CODE; B-REG. DATA READ
04230 00845                     **
04235 00846P 0473 0F            INPUT SEI             SET IRQ MASK
04240 00847P 0474 C6 3A     A         LDAB   #%00111010
04245 00848P 0476 F7 E403   A         STAB   PIA1BC   SET CRB2=0 ;DDR
04250 00849P 0479 C6 00     A         LDAB   #$00
04255 00850P 047B F7 E402   A         STAB   PIA1BD   CONFIGURE PB0-PB7 AS INPUTS
04260 00851P 047E B7 E400   A         STAA   PIA1AD   DEVICE SELECT
04265 00852P 0481 C6 3E     A         LDAB   #%00111110
04270 00853P 0483 F7 E403   A         STAB   PIA1BC   SET CRB2=1; PDR
04275 00854P 0486 C6 36     A         LDAB   #%00110110
04280 00855P 0488 F7 E401   A         STAB   PIA1AC   CA2 "LOW" (SELECT)
04285 00856P 048B 86 3E     A         LDAA   #%00111110
04290 00857P 048D F6 E402   A         LDAB   PIA1BD   READ DATA
04295 00858P 0490 B7 E401   A         STAA   PIA1AC   CA2 "HIGH" (DESELECT)
04300 00859P 0493 01                  NOP
04305 00860P 0494 0E                  CLI             CLEAR MASK
04310 00861P 0495 39                  RTS


04320 00863                     **
04325 00864                     **    WATCHDOG TIMER RESET ROUTINE
04330 00865                     **       RESETS HARDWARE TIMER
04335 00866                     **       TIMER CYCLE TIME ~ 50MS
04340 00867                     **
04345 00868P 0496 C6 0F     A WDOG    LDAB   #$0F     WATCHDOG DEVICE SELECT CODE
04350 00869P 0498 7E 043D   P         JMP    DEVSEL   SELECT DEVICE AND RETURN


04360 00871                     **
04365 00872                     **   I/O BOARD INPUT    "A" REG. MUX ADDRESS
04370 00873                     **         "B" REG. 8MSB     ( NON-INTERRUPTIABLE )
04375 00874                     **
04380 00875P 049B 0F            AIN8  SEI             MASK IRQ
04385 00876P 049C C6 3A     A         LDAB   #%00111010
04390 00877P 049E F7 E403   A         STAB   PIA1BC   SELECT DATA DIRECTION REGISTER
04395 00878P 04A1 C6 FF     A         LDAB   #$FF
04400 00879P 04A3 F7 E402   A         STAB   PIA1BD   CONFIGURE PB0-PB7 AS OUTPUTS
04405 00880P 04A6 C6 3E     A         LDAB   #%00111110
04410 00881P 04A8 F7 E403   A         STAB   PIA1BC   SELECT DATA REGISTER
04415 00882P 04AB B7 E402   A         STAA   PIA1BD   OUTPUT VALUE
04420 00883P 04AE C6 01     A         LDAB   #$01     SAMPLE HOLD & CONVERT CODE
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00884P 04B0 F7 E400  A         STAB   PIA1AD   SET DEVICE CODE
00885P 04B3 86 36    A         LDAA   #%00110110
00886P 04B5 B7 E401  A         STAA   PIA1AC   CA2 "LOW" (SELECT)
00887P 04B8 86 3E    A         LDAA   #%00111110
00888P 04BA B7 E401  A         STAA   PIA1AC   CA2 "HIGH" (DESELECT)
00889P 04BD 86 02    A         LDAA   #$02     8 MSB INPUT CODE
00890P 04BF BD 0473  P         JSR    INPUT    READ VALUE
00891P 04C2 53                 COMB            CONVERT TO STRAIGHT BINARY COD
00892P 04C3 39                 RTS


00894                   **
00895                   **   DELAY SUBROUTINE
00896                   **       DELAY = 50 MS X TIME
00897                   **       NOTE : MIN. DELAY = 50 MS
00898                   **       WATCHDOG TIMER RESET DURING DELAY
00899                   **
00900P 04C4 CE C350  A DELAY  LDX    #$C350   SET FOR 50 MS DELAY
00901P 04C7 FF E414  A         STX    PTM2LC   INITIALIZE TIMER - CLEAR FLAG
00902P 04CA BD 0496  P DELAY1 JSR    WDOG
00903P 04CD B6 E411  A         LDAA   PTM2CS   READ STATUS
00904P 04D0 85 02    A         BITA   #$02     TEST BIT #1 (TIMER #2 FLAG)
00905P 04D2 27 F6 04CA         BEQ    DELAY1   WAIT FOR TIME OUT
00906P 04D4 7A 002C  B         DEC    TIME     DECREMENT COUNT
00907P 04D7 2E EB 04C4         BGT    DELAY    AGAIN
00908P 04D9 39                 RTS


00910                   **
00911                   **   RING COMMUTATION CIRCUIT - SUBROUTINE
00912                   **        ENABLE COMMS; RING FOR 1MS
00913                   **        NOTE: COMM'S LEFT ENABLED
00914                   **
00915P 04DA 86 98    A RCOM   LDAA   #$98     RING COMM (BIT #3) COMM ENABLE
00916P 04DC BD 0433  P         JSR    DOUTA    ACTIVATE CIRCUIT & FORCE RING
00917P 04DF CE 0395  A         LDX    #$0395   1MS - 83US (EXECUTION COMPENSA
00918P 04E2 FF E414  A         STX    PTM2LC   INITIALIZE TIMER - CLEAR FLAG
00919P 04E5 B6 E411  A         LDAA   PTM2CS   READ STATUS
00920P 04E8 85 02    A         BITA   #$02     TEST BIT #1 (TIMER #2 FLAG)
00921P 04EA 27 F9 04E5         BEQ    *-5      WAIT FOR TIME OUT
00922P 04EC 86 08    A         LDAA   #$08     RING COMM CODE (BIT #3)
00923P 04EE 7E 0433  P         JMP    DOUTA    DEACTIVATE FORCED RINGING & RE


00925                   **
00926                   **   ZERO VOLTAGE CONTROLS - SUBROUTINE
00927                   **      SETS : CPULSE , CSINE , CTRIA - FOR MIN. MODU
00928                   **      AND OUTPUTS VALUE
00929                   **      RETURNS: FROM VOUT SUBROUTINE
00930                   **
00931P 04F1 7F 0035  B ZVOLT  CLR    CPULSE   SET 2-PULSE TO MIN
00932P 04F4 86 0D    A         LDAA   #$0D     VSIN = .508 VOLTS
00933P 04F6 97 36    B         STAA   CSINE    SET SINE AMPLITUDE TO MIN.
00934P 04F8 86 FF    A         LDAA   #$FF     VTRIA = 9.96 VOLTS
00935P 04FA 97 37    B         STAA   CTRIA    SET TRIANGLE AMPLITUDE MAX.
00936P 04FC 7E 053D  P         JMP    VOUT     OUTPUT VALUES AND RETURN
```

```
04695 00938                      **
04700 00939                      **    VOLTAGE CORRECTION SUBROUTINE
04705 00940                      **       CHECKS VSIGNF: FOR INCREASE OR DECREASE
04710 00941                      **       ALTERS: CPULSE, CSINE, CTRIA
04715 00942                      **       CTRIA IS UPDATED BY TABLE LOOK-UP TO APPROXI
04720 00943                      **       LINEAR CHANGE IN MODULATION INDEX
04725 00944                      **
04730 00945P 04FF 96 23       B VCORR  LDAA   VSIGNF   DETERMINE CORRECTION DIRECTION
04735 00946P 0501 26 1B 051E           BNE    VDEC     VOLTAGE DECREASE
04740 00947                      *   VOLTAGE INCREASE
04745 00948P 0503 96 36       B VINC   LDAA   CSINE    READ PRESENT SINE AMPLITUDE
04750 00949P 0505 81 40       A        CMPA   #$40     CHECK FOR 2.50V MAX. POSITION
04755 00950P 0507 24 05 050E           BCC    VINC2    SINE ALREADY MAX.
04760 00951P 0509 7C 0036     B        INC    CSINE    INCREASE SINE AMPLITUDE
04765 00952P 050C 20 0F 051D           BRA    VINC3    BRANCH TO RETURN
04770 00953P 050E 96 37       B VINC2  LDAA   CTRIA    READ PRESENT TRIANGLE AMPLITUD
04775 00954P 0510 81 00       A        CMPA   #$00     TEST FOR MIN. POSITION
04780 00955P 0512 23 09 051D           BLS    VINC3    BRANCH TO RETURN
04785 00956P 0514 CE 073C     P        LDX    #TBLVTR  SET POINTER TO 1ST LOCATION
04790 00957P 0517 BD 0637     P        JSR    FUNC     DETERMINE FUNCTION
04795 00958P 051A 10                   SBA             DECREASE TRIANGLE AMPLITUDE
04800 00959P 051B 97 37       B        STAA   CTRIA    SAVE NEW VALUE
04805 00960P 051D 39            VINC3  RTS             RETURN
04810 00961                      *   VOLTAGE DECREASE
04815 00962P 051E 96 37       B VDEC   LDAA   CTRIA    READ PRESENT TRIANGLE AMPLITUD
04820 00963P 0520 81 FF       A        CMPA   #$FF     TEST FOR MAX. 10.0V LEVEL
04825 00964P 0522 24 0F 0533           BCC    VDEC1    TRIANGLE ALREADY MAX.
04830 00965P 0524 CE 073C     P        LDX    #TBLVTR  SET POINTER TO 1ST TABLE LOCAT
04835 00966P 0527 BD 0637     P        JSR    FUNC     DETERMINE FUNCTION
04840 00967P 052A 1B                   ABA             INCREASE TRIANGLE AMPLITUDE
04845 00968P 052B 24 02 052F           BCC    *+4      NO 8 BIT OVERFLOW
04850 00969P 052D 86 FF       A        LDAA   #$FF     OVERFLOW - SET MAX. VALUE
04855 00970P 052F 97 37       B        STAA   CTRIA    SAVE NEW VALUE
04860 00971P 0531 20 09 053C           BRA    VDEC2    BRANCH TO RETURN
04865 00972P 0533 96 36       B VDEC1  LDAA   CSINE    READ PRESENT SINE AMPLITUDE
04870 00973P 0535 81 0D       A        CMPA   #$0D     TEST FOR MIN. POSITION
04875 00974P 0537 23 03 053C           BLS    VDEC2    SINE ALREADY MIN.
04880 00975P 0539 7A 0036     B        DEC    CSINE    DECREASE SINE AMPLITUDE
04885 00976P 053C 39            VDEC2  RTS             RETURN


04895 00978                      **
04900 00979                      **    VOLTAGE OUTPUT SUBROUTINE
04905 00980                      **     MODIFIES MODULATION INDEX BASED UPON VALUE AT
04910 00981                      **     CPULSE, CSINE, CTRIA
04915 00982P 053D 5F            VOUT   CLRB            ZERO 8 LSB
04920 00983P 053E 96 35       B        LDAA   CPULSE   READ TIMER VALUE
04925 00984P 0540 44                   LSRA            /2  8 MSB
04930 00985P 0541 56                   RORB            /2  8 LSB
04935 00986P 0542 44                   LSRA            /4  8 MSB
04940 00987P 0543 56                   RORB            /4  8 LSB
04945 00988P 0544 CB 3C       A        ADDB   #$3C     CORRECT FOR MIN. VALUE (60US)
04950 00989P 0546 D7 34       B        STAB   CTEMP+1  SAVE TEMPORARY 8 LSB'S
04955 00990P 0548 97 33       B        STAA   CTEMP    SAVE TEMPORARY 8 MSB'S
04960 00991P 054A DE 33       B        LDX    CTEMP
04965 00992P 054C FF E412     A        STX    PTM1LC   OUTPUT TO TIMER #1
04970 00993                      *   OUTPUT  SINE AMPLITUDE
04975 00994P 054F 96 36       B        LDAA   CSINE    READ VALUE
```

```
04980 00995P 0551 C6 06      A          LDAB   #$06      DEVICE SELECT CODE
04985 00996P 0553 BD 044E    P          JSR    OUTPUT    OUTPUT VALUE
04990 00997                    *   OUTPUT  TRIANGLE AMPLITUDE
04995 00998P 0556 96 37      B          LDAA   CTRIA     READ VALUE
05000 00999P 0558 C6 08      A          LDAB   #$08      DEVICE SELECT CODE
05005 01000P 055A BD 044E    P          JSR    OUTPUT    OUTPUT VALUE
05010 01001                    * CHECK FOR ENERGY CONTROL ACTIVATION REGION
05015 01002P 055D 86 C0      A          LDAA   #$C0      CODE TO DISABLE ENERGY CONTROL
05020 01003P 055F D6 37      B          LDAB   CTRIA     CHECK FOR SIX-STEP
05025 01004P 0561 26 02 0565            BNE    *+4       AMPLITUDE #0 , NOT IN SIX-STEP
05030 01005P 0563 86 40      A          LDAA   #$40      CODE TO ENABLE ENERGY CONTROL
05035 01006P 0565 7E 0433    P          JMP    DOUTA     OUTPUT VALUE AND RETURN


05045 01008                    **
05050 01009                    **    INVERTER ROTATION SUBROUTINE
05055 01010                    **       CHECKS CONSOLE POSITION : DIA
05060 01011                    **       AND CONFIGURES INVERTER ACCORDING
05065 01012                    **
05070 01013P 0568 7F 0025    B IROT     CLR    IDIRF     RESET INVERTER DIRECTION FLAG
05075 01014P 056B 96 08      B          LDAA   DIA       READ DIGITAL INPUTS A PORT
05080 01015P 056D 84 06      A          ANDA   #$06      MASK FWD & REV BITS
05085 01016P 056F 27 13 0584            BEQ    IROT2+3   "NEUTRAL"- CONTINUE
05090 01017P 0571 81 04      A          CMPA   #$04      CHECK REV BIT
05095 01018P 0573 26 07 057C            BNE    IROT1     FORWARD
05100 01019P 0575 86 84      A          LDAA   #$84      CONFIGURE INVERTER FOR REVERSE
05105 01020P 0577 7A 0025    B          DEC    IDIRF     SET INVERTER FLAG (-1=REV)
05110 01021P 057A 20 05 0581            BRA    IROT2
05115 01022P 057C 86 82      A IROT1    LDAA   #$82      CONFIGURE INVERTER FOR FORWARD
05120 01023P 057E 7C 0025    B          INC    IDIRF     SET INVERTER FLAG (1=FWD)
05125 01024P 0581 BD 0433    P IROT2    JSR    DOUTA     OUTPUT DIRECTION INFORMATION
05130 01025P 0584 39                    RTS


05140 01027                    **
05145 01028                    **     SLIP MAXIMUM SUBROUTINE
05150 01029                    **        DETERMINES MAXIMUN VALUE FOR SLIP
05155 01030                    **        BASED UPON FREQUENCY OR OVERRIDING CONDITION
05160 01031                    **        SLIP WILL BE FORCED TO ZERO
05165 01032                    **        IF SLIPF = 1
05170 01033                    **        OR NEGATIVE TORQUE IS REQUESTED BELOW 40 HZ
05175 01034                    **         TABLE: TBLSP
05180 01035                    **
05185 01036P 0585 D6 0C      B SMAX     LDAB   PER+1     READ PERIOD ( 8MSB )
05190 01037P 0587 CE 071C    P          LDX    #TBLSP    SET POINTER TO 1ST TABLE LOCAT
05195 01038P 058A A6 00      A          LDAA   0,X
05200 01039P 058C F1 071A    P          CMPB   PERMIN    COMPARE TO UPPER BREAK POINT
05205 01040P 058F 25 0D 059E            BCS    SMAX1     ABOVE CURVE'S RANGE
05210 01041P 0591 A6 10      A          LDAA   16,X
05215 01042P 0593 F1 071B    P          CMPB   PERMAX    COMPARE TO LOWER LIMIT
05220 01043P 0596 24 06 059E            BCC    SMAX1     BELOW CURVE'S RANGE
05225 01044P 0598 17                    TBA              TRANSFER MSB'S TO A REG.
05230 01045P 0599 D6 0D      B          LDAB   PER+2     READ 8 LSB'S
05235 01046P 059B BD 0647    P          JSR    TBL4      LINEARIZE FROM TABLE
05240 01047P 059E BD 05B8    P SMAX1    JSR    REG       CHECK REGENERATION LIMIT
05245 01048P 05A1 D6 03      B          LDAB   SLIPD     CHECK TORQUE REQUEST
05250 01049P 05A3 26 06 05AB            BNE    SMAX2     OK, POSITIVE REQUEST
05255 01050P 05A5 D6 0C      B          LDAB   PER+1     PERIOD 8MSB
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```
01051P 05A7 C1 0C     A          CMPB   #$0C      <=40.7 HZ
01052P 05A9 24 05 05B0           BCC    SMAX3     INHIBIT REGENERATION BELOW 40.
01053P 05AB 7D 0026   B  SMAX2   TST    SLIPF     OVERRIDE COMMAND ACTIVE
01054P 05AE 27 01 05B1           BEQ    *+3       OK CONTINUE
01055P 05B0 4F           SMAX3   CLRA             FORCE SLIP TO ZERO
01056P 05B1 97 0E     B          STAA   SMAXV     SAVE SLIP VALUE
01057P 05B3 C6 09     A          LDAB   #$09      DEVICE CODE SLIP LIMIT DAC
01058P 05B5 7E 044E   P          JMP    OUTPUT    OUTPUT TO DAC AND RETURN


01060                    **
01061                    **     REGENERATION SLIP CONTROL
01062                    **        REDUCES: PREVIOUS SLIP LIMIT IN REG. "A"
01063                    **        IF VBAT + (POT SETTING)  EXCEEDS PRESET LIMI
01064                    **        DEAD BAND IS INCORPORATED AROUND LIMIT
01065                    **        INCREASES: SLIP LIMIT TO NORMAL LIMIT IF VOL
01066                    **        BELOW DEAD BAND
01067                    **         RETURNS WITH SLIP IN "A"-REG
01068                    **
01069P 05B8 97 33     B  REG     STAA   CTEMP     SAVE LIMIT
01070P 05BA 96 05     B          LDAA   REGV      REGENERATION SETTING
01071P 05BC F6 000A   P          LDAB   KPOT      SCALE FACTOR
01072P 05BF BD 0687   P          JSR    MP8       SCALE
01073P 05C2 2A 01 05C5           BPL    *+3
01074P 05C4 4C                   INCA             ROUND 8MSB
01075P 05C5 16                   TAB
01076P 05C6 96 0E     B          LDAA   SMAXV
01077P 05C8 CB D2     A          ADDB   #210      150V - 2.5V
01078P 05CA D1 00     B          CMPB   VBAT
01079P 05CC 25 09 05D7           BCS    REG0      VBAT > (VLIM - 2.5)
01080P 05CE 7D 0027   B          TST    REGF      TEST REGENERATION LIMIT
01081P 05D1 26 1C 05EF           BNE    REG1      YES, ACTIVE
01082P 05D3 96 33     B          LDAA   CTEMP     USE NORMAL LIMIT VALUE
01083P 05D5 20 27 05FE           BRA    REG2      CONTINUE
01084P 05D7 CB 07     A  REG0    ADDB   #7        150V + 2.5V
01085P 05D9 D1 00     B          CMPB   VBAT
01086P 05DB 25 09 05E6           BCS    REG0A     VBAT > (VLIM + 2.5)
01087P 05DD 7D 0027   B          TST    REGF      TEST REGENERATION LIMIT
01088P 05E0 26 13 05F5           BNE    REG1A     YES, ACTIVE
01089P 05E2 96 33     B          LDAA   CTEMP     USE NORMAL LIMIT VALUE
01090P 05E4 20 18 05FE           BRA    REG2      CONTINUE
01091P 05E6 D7 27     B  REG0A   STAB   REGF      SET REGENERATION FLAG
01092P 05E8 80 01     A          SUBA   #$01      DECREASE SLIP LIMIT
01093P 05EA 24 01 05ED           BCC    *+3       NO, OVERFLOW
01094P 05EC 4F                   CLRA             SET MINIMUN
01095P 05ED 20 06 05F5           BRA    REG1A
01096P 05EF 8B 01     A  REG1    ADDA   #$01      INCREASE SLIP LIMIT
01097P 05F1 24 02 05F5           BCC    *+4
01098P 05F3 86 FF     A          LDAA   #$FF      SET MAXIMUN
01099P 05F5 D6 33     B  REG1A   LDAB   CTEMP
01100P 05F7 11                   CBA              COMPARE TO NORMAL LIMIT VALUE
01101P 05F8 25 04 05FE           BCS    REG2      SLIP(FREG) > SLIP(REG)
01102P 05FA 7F 0027   B          CLR    REGF      RESET FLAG
01103P 05FD 17                   TBA
01104P 05FE 39           REG2    RTS              RETURN
01105                    **
01106                    **      SINE / TRIANGLE RATIO SUBROUTINE
01107                    **         SELECTS PROPER SINE /TRIANGLE RATIO FROM TA
```

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05545 01108                    **        BASED UPON PRESENT OPERATING FREQUENCY
05550 01109                    **        HYSTERISIS INCLUDED AT SWITCH POINTS
05555 01110                    **         PERIOD INFO AT : PER
05560 01111                    **         ALTERS: STR
05565 01112                    **         TABLE: TBLSIN
05570 01113                    **
05575 01114P 05FF 96 0B     B SINTR  LDAA    PER       READ PERIOD VALUE ( 8MSB )
05580 01115P 0601 CE 072A   P        LDX     #TBLSIN-3 SET TABLE POINTER
05585 01116P 0604 08          SINTR1 INX
05590 01117P 0605 08                 INX               ADVANCE POINTER TO NEXT
05595 01118P 0606 08                 INX               THRESHOLD LEVEL
05600 01119P 0607 A1 02     A        CMPA    2,X       CHECK RATIO THRESHOLD
05605 01120P 0609 24 F9 0604         BCC     SINTR1    OUT OF RANGE - TRY NEXT LEVEL
05610 01121P 060B A1 01     A        CMPA    1,X       CHECK HYSTER. LIMITS
05615 01122P 060D 24 0E 061D         BCC     SINTR2    DEAD BAND - RETAIN PREVIOUS RA
05620 01123P 060F E6 00     A        LDAB    0,X       FIND CORRECT RATIO CODE
05625 01124P 0611 D1 16     B        CMPB    STR       CHECK FOR RATIO CHANGE
05630 01125P 0613 27 08 061D         BEQ     SINTR2    NO CHANGE
05635 01126P 0615 D7 16     B        STAB    STR       SAVE NEW RATIO
05640 01127P 0617 86 01     A        LDAA    #$01
05645 01128P 0619 97 17     B        STAA    STRF      SET CHANGE FLAG
05650 01129P 061B 20 03 0620         BRA     *+5       BRANCH TO RETURN
05655 01130P 061D 7F 0017   B SINTR2 CLR     STRF      RESET CHANGE FLAG
05660 01131P 0620 39                 RTS               RETURN


05670 01133                    **
05675 01134                    **   SUBROUTINE : CONTROL GAIN LOOK-UP
05680 01135                    **       BASED UPON FREQUENCY AT PER+1 & PER+2
05685 01136                    **       TABLE: TBLGLO   LOW FREQUENCIES < 30.5 HZ
05690 01137                    **       TABLE: TBLGHI   HIGH FREQUENCIES > 30.5 HZ
05695 01138                    **       RETURNS FROM TBL SUBROUTINE WITH GAIN IN A-
05700 01139                    **
05705 01140P 0621 96 0C     B GAIN   LDAA    PER+1     8MSB
05710 01141P 0623 D6 0D     B        LDAB    PER+2     8LSB
05715 01142P 0625 81 10     A        CMPA    #$10
05720 01143P 0627 24 06 062F         BCC     GAIN1     < 30HZ USE LOW FREQ. TABLE
05725 01144P 0629 CE 0761   P        LDX     #TBLGHI   USE HIGH FREQ TABLE
05730 01145P 062C 7E 064B   P        JMP     TBL       LINEARIZE & RETURN
05735 01146P 062F 16          GAIN1  TAB
05740 01147P 0630 4F                 CLRA
05745 01148P 0631 CE 0750   P        LDX     #TBLGLO   USE LOW FREQ. TABLE
05750 01149P 0634 7E 0643   P        JMP     TBL16     LINEARIZE & RETURN


05760 01151                    **
05765 01152                    **    DISCRETE FUNCTION TRANSFORMATION ROUTINE
05770 01153                    **       "X"-REG.  POINTING TO TABLE ADDRESS
05775 01154                    **       "A"-REG.  ARGRUMENT
05780 01155                    **     RETURNS:  "B"-REG. FUNCTION
05785 01156                    **               "A"-REG. UNALTERED
05790 01157                    **
05795 01158P 0637 E6 00     A FUNC   LDAB    0,X       READ REFRENCE ARG.
05800 01159P 0639 11                 CBA               CHECK RANGE
05805 01160P 063A 24 04 0640         BCC     FUNC1     ARG. RANGE FOUND
05810 01161P 063C 08                 INX               ADVANCE  POINTER
05815 01162P 063D 08                 INX               TO NEXT ARGUMENT
05820 01163P 063E 20 F7 0637         BRA     FUNC      AGAIN
```

```
01164P 0640 E6 01      A FUNC1   LDAB   1,X       READ FUNCTION VALUE
01165P 0642 39                   RTS              RETURN


01167                    **
01168                    **     LINEARIZING TABLE SUBROUTINE:
01169                    **       V=V0+(V0-V1)(A-A0)16/256
01170                    **       "X"-REG. = POINTER TO TABLE
01171                    **       "B" = ARG.  A<16
01172                    **       RESULT:  V<256 IN "A"-REG.
01173P 0643 58             TBL16   ASLB             TABLE LENGTH 16 BYTES
01174P 0644 49                     ROLA
01175P 0645 58             TBL8    ASLB             TABLE LENGTH 8 BYTES
01176P 0646 49                     ROLA
01177P 0647 58             TBL4    ASLB             TABLE LENGTH 4 BYTES
01178P 0648 49                     ROLA
01179P 0649 58                     ASLB
01180P 064A 49                     ROLA             ARGRUMENT "A", "B" = (A-A0)16
01181P 064B DF 30      B TBL       STX    TEMP      SAVE TABLE ADDRESS
01182P 064D 9B 31      B           ADDA   TEMP+1    ADJUST POINTER PLACEMENT
01183P 064F 24 03 0654             BCC    *+5       CHECK FOR CARRY
01184P 0651 7C 0030    B           INC    TEMP      CARRY BIT
01185P 0654 97 31      B           STAA   TEMP+1    SAVE ADJUSTED VALUE
01186P 0656 DE 30      B           LDX    TEMP
01187P 0658 A6 00      A           LDAA   0,X       READ LOWER VALUE (V0)
01188P 065A A0 01      A           SUBA   1,X       -V1
01189P 065C 97 32      B           STAA   TEMP+2    SAVE DIFFERENCE
01190P 065E 2C 01 0661             BGE    *+3
01191P 0660 40                     NEGA             FORM ABSOLUTE
01192P 0661 BD 0687    P           JSR    MP8       (V0-V1)(A-A0)16
01193P 0664 2A 01 0667             BPL    *+3       CHECK ( 8LSB )
01194P 0666 4C                     INCA             ROUND 8 MSB
01195P 0667 D6 32      B           LDAB   TEMP+2
01196P 0669 2F 01 066C             BLE    *+3       CHECK FOR POS. SLOPE
01197P 066B 40                     NEGA             NO, CORRECT FOR SIGN OF MULTIP
01198P 066C AB 00      A           ADDA   0,X       SCALE
01199P 066E 39                     RTS              RETURN


01201                    **
01202                    **     16 TO 8 BIT + SIGN TRUNCATION
01203                    **             ENTER: A REG. 8MSB  B REG. 8LSB (2'S COMP
01204                    **             EXIT: A REG. SIGN   B REG. 8BIT MAG. (ABS
01205                    **
01206P 066F 81 00      A TRUNC     CMPA   #$00
01207P 0671 27 13 0686             BEQ    TRUNC2    NO 8BIT OVERFLOW - CONTINUE
01208P 0673 81 FF      A           CMPA   #$FF
01209P 0675 27 0B 0682             BEQ    TRUNC1+4  NO 8BIT OVERFLOW - CONTINUE
01210P 0677 2D 05 067E             BLT    TRUNC1
01211P 0679 4F                     CLRA
01212P 067A C6 FF      A           LDAB   #$FF      SET MAX. POSITIVE VALUE
01213P 067C 20 08 0686             BRA    TRUNC2    CONTINUE
01214P 067E 86 FF      A TRUNC1    LDAA   #$FF
01215P 0680 C6 01      A           LDAB   #$01      SET MAX. NEGATIVE VALUE
01216P 0682 50                     NEGB             FORM ABSOLUTE VALUE
01217P 0683 25 01 0686             BCS    *+3       CHECK FOR [-256]
01218P 0685 16                     TAB              YES THEN SET +255
01219P 0686 39             TRUNC2  RTS
```

```
                               **
                               **    EXPANDED LOOP MULTIPLY
                               **            A*B : 2 UNSIGNED 8 BIT VALUES
                               **           RESULT = (A,B)
                               **            WORKSPACE = MULT
                               **            ( 114 CYCLES )
                               **
P Ø687 97 2D       B MP8      STAA   MULT       MULTIPLICAND
P Ø689 4F                     CLRA              CLEAR MS BYTE
P Ø68A 56                     RORB              SHIFT L.S. BIT INTO CARRY
P Ø68B 8D ØØ Ø68D             BSR    *+2        FAST X2 LOOP
P Ø68D 24 Ø2 Ø691             BCC    *+4        BIT NOT SET
P Ø68F 9B 2D       B          ADDA   MULT       OTHERWISE ADD MULT - CARRY CLE
P Ø691 46                     RORA
P Ø692 56                     RORB
P Ø693 24 Ø2 Ø697             BCC    *+4
P Ø695 9B 2D       B          ADDA   MULT
P Ø697 46                     RORA
P Ø698 56                     RORB              BIT2 (BIT6)
P Ø699 24 Ø2 Ø69D             BCC    *+4
P Ø69B 9B 2D       B          ADDA   MULT
P Ø69D 46                     RORA
P Ø69E 56                     RORB              BIT3 (BIT7)
P Ø69F 24 Ø2 Ø6A3             BCC    *+4
P Ø6A1 9B 2D       B          ADDA   MULT
P Ø6A3 46                     RORA
P Ø6A4 56                     RORB              BIT4 (BIT8)
P Ø6A5 39                     RTS

                               **
                               **    SCALING SUBROUTINE
                               **        SCALE X  16 : A OR B REG.
                               **        VALUE :  A OR B REG.
                               **        RESULT:  B-REG. ROUNDED TO 8MSB
                               **
P Ø6A6 BD Ø687     P SCALE    JSR    MP8        V(SCALE X 16)
P Ø6A9 44                     LSRA
P Ø6AA 56                     RORB              /2
P Ø6AB 44                     LSRA
P Ø6AC 56                     RORB              /4
P Ø6AD 44                     LSRA
P Ø6AE 56                     RORB              /8
P Ø6AF 44                     LSRA
P Ø6BØ 56                     RORB              DIVIDE BY 16
P Ø6B1 C9 ØØ       A          ADCB   #$Ø        ROUND 8MSB
P Ø6B3 24 Ø1 Ø6B6             BCC    *+3        TEST FOR OVERFLOW
P Ø6B5 4C                     INCA
P Ø6B6 39                     RTS

                               **
                               **   SUBROUTINE : QUICK DIVIDER; TRUE TRUNCATION
                               **       (A,B) / 2^(DIVW)
                               **        A,B 16BIT SIGNED NUMBER
                               **        DIVISOR PRESAVED AT DIVW <=127
                               **
P Ø6B7 7F ØØ2F     B QDIV     CLR    DIVW+1     CLEAR COMPLEMENT FLAG
```

```
01277P 06BA 4D                     TSTA
01278P 06BB 2A 05 06C2             BPL    QDIV1      OK, POSITIVE NUMBER
01279P 06BD 7C 002F  B             INC    DIVW+1     SET COMPLEMENT FLAG
01280P 06C0 8D 0F 06D1             BSR    COM16      16 BIT 2'S COMPLEMENT
01281P 06C2 47              QDIV1  ASRA              DIVIDE 8MSB BY 2 SIGN EXTENDED
01282P 06C3 56                     RORB              DIVIDE 8LSB BY 2
01283P 06C4 7A 002E  B             DEC    DIVW       DIVISOR
01284P 06C7 2E F9 06C2             BGT    QDIV1      AGAIN
01285P 06C9 7D 002F  B             TST    DIVW+1     CHECK FLAG
01286P 06CC 27 02 06D0             BEQ    QDIV2      OK, NOT SET
01287P 06CE 8D 01 06D1             BSR    COM16      16 BIT 2'S COMPLEMENT
01288P 06D0 39              QDIV2  RTS


01290                       **
01291                       **    16BIT 2'S COMPLEMENT OF (A,B)
01292                       **
01293P 06D1 43              COM16  COMA              1'S COMPLEMENT OF 8MSB
01294P 06D2 53                     COMB              1'S COMPLEMENT OF 8LSB
01295P 06D3 CB 01     A            ADDB   #$01       1'S COMPLEMENT OF 8LSB
01296P 06D5 89 00     A            ADCA   #0         2'S COMPLEMENT OF 8MSB
01297P 06D7 39                     RTS


01299                       **
01300                       **   EXPANDED LOOP DIVIDE: (A,B)/DIVW; WHERE A<128
01301                       **    15 BIT DIVIDEND, 7 BIT DIVISOR: DIVW<128
01302                       **    QUOTIENT<255 IN B REG.
01303                       **    168 CYCLES: OVERFLOW PORTION IN (DIVW+1)
01304                       **                   IF A>DIVW
01305                       **
01306P 06D8 7F 002F  B DIV         CLR    DIVW+1
01307P 06DB 7A 002F  B             DEC    DIVW+1
01308P 06DE 7C 002F  B DIV2        INC    DIVW+1
01309P 06E1 90 2E    B             SUBA   DIVW       TEST OVERFLOW
01310P 06E3 24 F9 06DE             BCC    DIV2       YES, TALLY COUNT
01311P 06E5 9B 2E    B             ADDA   DIVW       NO, RESTORE AND SET CARRY
01312P 06E7 59                     ROLB              M.S. BIT INTO CARRY
01313P 06E8 49                     ROLA              INTO L.S. OF A
01314P 06E9 8D 01 06EC             BSR    *+3
01315P 06EB 53                     COMB              1'S COMPLEMENT OF QUOTIENT
01316P 06EC 90 2E    B             SUBA   DIVW       TEST DIVISOR
01317P 06EE 24 02 06F2             BCC    *+4
01318P 06F0 9B 2E    B             ADDA   DIVW       NOT DIVISABLE, CARRY=1
01319P 06F2 59                     ROLB              FORM 1'S COMPLEMENT OF QUOTIEN
01320P 06F3 49                     ROLA              SECOND BIT
01321P 06F4 90 2E    B             SUBA   DIVW
01322P 06F6 24 02 06FA             BCC    *+4
01323P 06F8 9B 2E    B             ADDA   DIVW
01324P 06FA 59                     ROLB
01325P 06FB 49                     ROLA              THIRD BIT
01326P 06FC 90 2E    B             SUBA   DIVW
01327P 06FE 24 02 0702             BCC    *+4
01328P 0700 9B 2E    B             ADDA   DIVW
01329P 0702 59                     ROLB
01330P 0703 49                     ROLA              FOURTH BIT
01331P 0704 90 2E    B             SUBA   DIVW
01332P 0706 24 02 070A             BCC    *+4
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06670 01333P 0708 9B 2E    B          ADDA    DIVW
06675 01334P 070A 59                  ROLB
06680 01335P 070B 49                  ROLA                 2(REMAINDER)
06685 01336P 070C 53                  COMB                 1'S COMPLEMENT OF QUOT.
06690 01337P 070D 39                  RTS
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06705 01340                         **
06710 01341                         **  THERMISTOR TABLE:
06715 01342                         **        1ST BYTE - MUX. ADDRESS
06720 01343                         **        2ND BYTE - WARNING LIMIT
06725 01344                         **        3RD BYTE - TRIP LIMIT
06730 01345                         **
06735 01346P 070E    0C     A TBLTEM FCB    TO0.      THERMISTOR #0
06740 01347P 070F    6B     A        FCB    107       75 C
06745 01348P 0710    75     A        FCB    117       80 C
06750 01349P 0711    0D     A        FCB    TO1.      THERMISTOR #1
06755 01350P 0712    6B     A        FCB    107       75 C
06760 01351P 0713    75     A        FCB    117       80 C
06765 01352P 0714    0E     A        FCB    TO2.      THERMISTOR #2
06770 01353P 0715    6B     A        FCB    107       75 C
06775 01354P 0716    75     A        FCB    117       80 C
06780 01355P 0717    0F     A        FCB    TO3.      THERMISTOR #3
06785 01356P 0718    6B     A        FCB    107       75 C
06790 01357P 0719    75     A ETBLTE FCB    117       80 C


06800 01359                         *
06805 01360                         *   SLIP CONSTANTS - USEFUL TABLE RANGE
06810 01361                         *
06815 01362P 071A    02     A PERMIN FCB    $02       MAX. FREQ. 244HZ
06820 01363P 071B    04     A PERMAX FCB    $04       MIN. FREQ. 122HZ
06825 01364                         **
06830 01365                         **   MAXIMUM SLIP TABLE: SCALED FOR 8 ELEMENTS
06835 01366                         **
06840 01367P 071C    FF     A TBLSP  FCB    $FF       (0)
06845 01368P 071D    FF     A        FCB    $FF       (1)
06850 01369P 071E    FF     A        FCB    $FF       (2)
06855 01370P 071F    FF     A        FCB    $FF       (3)
06860 01371P 0720    FF     A        FCB    $FF       (4)
06865 01372P 0721    FF     A        FCB    $FF       (5)
06870 01373P 0722    FF     A        FCB    $FF       (6)
06875 01374P 0723    FF     A        FCB    $FF       (7)
06880 01375P 0724    FF     A        FCB    $FF       10.0HZ    (8) $0200-244HZ
06885 01376P 0725    D8     A        FCB    $D8       8.45HZ    (9) $0240-217HZ
06890 01377P 0726    B8     A        FCB    $B8       7.19HZ    (A) $0280-195HZ
06895 01378P 0727    9F     A        FCB    $9F       6.21HZ    (B) $02C0-178HZ
06900 01379P 0728    89     A        FCB    $89       5.35HZ    (C) $0300-163HZ
06905 01380P 0729    76     A        FCB    $76       4.61HZ    (D) $0340-150HZ
06910 01381P 072A    67     A        FCB    $67       4.03HZ    (E) $0380-140HZ
06915 01382P 072B    59     A        FCB    $59       3.46HZ    (F) $03C0-130HZ
06920 01383P 072C    4D     A        FCB    $4D       3.00HZ    (10) $0400-122HZ


06930 01385                         **
06935 01386                         **   TABLE: SINE / TRIANGLE RATIOS
06940 01387                         **          1ST BYTE ACTIVATION CODE STR
06945 01388                         **          2ND BYTE UPPER THRESHOLD
06950 01389                         **          3RD BYTE LOWER THRESHOLD
06955 01390                         **
06960 01391P 072D    00     A TBLSIN FCB    $00       SET STR TO 9 (X1 CODE)
06965 01392P 072E    11     A        FCB    $11       28.7 HZ
06970 01393P 072F    12     A        FCB    $12       27.1 HZ
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06975 01394P 0730     01    A           FCB      $01        SET STR TO 27 (X3 CODE)
06980 01395P 0731     2C    A           FCB      $2C        11.1 HZ
06985 01396P 0732     2D    A           FCB      $2D        10.6 HZ
06990 01397P 0733     02    A           FCB      $02        SET STR TO 45 (X5 CODE)
06995 01398P 0734     39    A           FCB      $39        8.57 HZ
07000 01399P 0735     3D    A           FCB      $3D        8.00 HZ
07005 01400P 0736     04    A           FCB      $04        SET STR TO 63 (X7 CODE)
07010 01401P 0737     4B    A           FCB      $4B        6.51 HZ
07015 01402P 0738     51    A           FCB      $51        6.03 HZ
07020 01403P 0739     08    A           FCB      $08        SET STR TO 81 (X9 CODE)
07025 01404P 073A     FF    A           FCB      $FF
07030 01405P 073B     FF    A           FCB      $FF


07040 01407                 **
07045 01408                 **     TABLE: VOLTAGE CORRECTION FACTOR
07050 01409                 **         AS A FUNCTION OF TRIANGLE VOLTAGE
07055 01410                 **
07060 01411P 073C     E6    A TBLVTR FCB      230,4      9.0 <= VTRIA < 10.0     ( 4 COU
            P 073D     04    A
07065 01412P 073E     A6    A           FCB      166,3      6.5 <= VTRIA <  9.0     ( 3 COU
            P 073F     03    A
07070 01413P 0740     59    A           FCB      89,2       3.5 <= VTRIA <  6.5     ( 2 COU
            P 0741     02    A
07075 01414P 0742     00    A           FCB      0,1        0.0 <= VTRIA <  3.5     ( 1 COU
            P 0743     01    A


07085 01416                 **
07090 01417                 **     TABLE: ERROR CORRECTION LOOK-UP
07095 01418                 **
07100 01419P 0744     CF    A TBLCOR FCB      207,5      .81 <= ERR < 1.0V/HZ   (5 COUNT
            P 0745     05    A
07105 01420P 0746     9C    A           FCB      156,4      .61 <= ERR < .81       (4 COUNT
            P 0747     04    A
07110 01421P 0748     69    A           FCB      105,3      .41 <= ERR < .61       (3 COUNT
            P 0749     03    A
07115 01422P 074A     36    A           FCB      54,2       .21 <= ERR < .41       (2 COUNT
            P 074B     02    A
07120 01423P 074C     03    A           FCB      3,1        .01 <= ERR < .21       (1 COUNT
            P 074D     01    A
07125 01424P 074E     00    A           FCB      0,0        .00 <= ERR < .01       (0 COUNT
            P 074F     00    A


07135 01426                 **
07140 01427                 **     TABLE: GAIN LOOK-UP
07145 01428                 **       LOW FREQUENCIES < 30.5 HZ
07150 01429                 **
07155 01430P 0750     6A    A TBLGLO FCB      106        (0)
07160 01431P 0751     63    A           FCB      99         (1) 30.52 HZ  $1000
07165 01432P 0752     30    A           FCB      48         (2) 15.26 HZ  $2000
07170 01433P 0753     1F    A           FCB      31         (3) 10.17 HZ  $3000
07175 01434P 0754     17    A           FCB      23         (4) 7.63 HZ   $4000
07180 01435P 0755     12    A           FCB      18         (5) 6.10 HZ   $5000
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07185 01436P 0756     0E     A          FCB     14          (6) 5.09 HZ    $6000
07190 01437P 0757     0C     A          FCB     12          (7) 4.36 HZ    $7000
07195 01438P 0758     0A     A          FCB     10          (8) 3.81 HZ    $8000
07200 01439P 0759     0A     A          FCB     10          (9)
07205 01440P 075A     0A     A          FCB     10          (A)
07210 01441P 075B     0A     A          FCB     10          (B)
07215 01442P 075C     0A     A          FCB     10          (C)
07220 01443P 075D     0A     A          FCB     10          (D)
07225 01444P 075E     0A     A          FCB     10          (E)
07230 01445P 075F     0A     A          FCB     10          (F)
07235 01446P 0760     0A     A          FCB     10          (10)


07245 01448                    **
07250 01449                    **    TABLE: GAIN LOOK-UP
07255 01450                    **      HIGH FREQUENCIES > 30.5 HZ
07260 01451                    **
07265 01452P 0761     32     A TBLGHI FCB     50          (0)
07270 01453P 0762     32     A          FCB     50          (1)
07275 01454P 0763     32     A          FCB     50          (2) 244 HZ   $0200
07280 01455P 0764     32     A          FCB     50          (3) 163 HZ   $0300
07285 01456P 0765     32     A          FCB     50          (4) 122 HZ   $0400
07290 01457P 0766     32     A          FCB     50          (5) 98 HZ    $0500
07295 01458P 0767     75     A          FCB     117         (6) 81.4HZ   $0600
07300 01459P 0768     A4     A          FCB     164         (7) 69.8HZ   $0700
07305 01460P 0769     C8     A          FCB     200         (8) 61.0HZ   $0800
07310 01461P 076A     B2     A          FCB     178         (9) 54.3HZ   $0900
07315 01462P 076B     9F     A          FCB     159         (A) 48.8HZ   $0A00
07320 01463P 076C     91     A          FCB     145         (B) 44.4HZ   $0B00
07325 01464P 076D     85     A          FCB     133         (C) 40.7HZ   $0C00
07330 01465P 076E     7A     A          FCB     122         (D) 37.6HZ   $0D00
07335 01466P 076F     71     A          FCB     113         (E) 34.9HZ   $0E00
07340 01467P 0770     6A     A          FCB     106         (F) 32.6HZ   $0F00
07345 01468P 0771     63     A          FCB     99          (10)30.5HZ   $1000


07355 01470D 0000                       DSCT
07360 01471                    **
07365 01472                    **     VECTOR LOCATIONS
07370 01473                    **
07375 01474D 0000     0172   P          FDB     INT         IRQ ( INTERRUPT SERVICE ROUTIN
07380 01475D 0002     0000   P          FDB     START       SWI ( DEFAULT )
07385 01476D 0004     0152   P          FDB     SHUTD       NMI ( STOP )
07390 01477D 0006     0000   P          FDB     START       RESET ( POWER-UP )
      01478                             END
TOTAL ERRORS 00000


   0000 AI       00044*00045 00046 00047 00048 00049 00050 00051 00052 00053 00054
                 00055 00056 00057 00058 00059 00060
   000A AI10.    00055*
   000B AI11.    00056*
   0004 AI4.     00049*
   0005 AI5.     00050*
   0007 AI7.     00052*
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  ØØØ8 AI8.    ØØØ53*
  ØØØ9 AI9.    ØØØ54*
P Ø49B AIN8    ØØ195 ØØ347 ØØ350 ØØ695 ØØ757 ØØ763 ØØ766 ØØ875*
  E4ØØ ASCT    ØØØ21*ØØØ25 ØØØ26 ØØØ27 ØØØ28 ØØØ32 ØØØ33 ØØØ34 ØØØ35 ØØØ36 ØØØ37
               ØØØ38 ØØØ39
P Ø3E1 BATT    ØØ728*ØØ736
P Ø3F7 BATT1   ØØ731 ØØ738*
P Ø4Ø1 BATT2   ØØ739 ØØ743*
P Ø432 CALCV1  ØØ77Ø ØØ772*
P Ø41Ø CALCVB  ØØ729 ØØ756*
P Ø6D1 COM16   ØØ359 ØØ441 ØØ532 ØØ589 ØØ595 Ø128Ø Ø1287 Ø1293*
B ØØ2B COUNT   ØØ1Ø4*ØØ69Ø ØØ711
B ØØ35 CPULSE  ØØ111*ØØ931 ØØ983
B ØØ36 CSINE   ØØ112*ØØ5ØØ ØØ933 ØØ948 ØØ951 ØØ972 ØØ975 ØØ994
B ØØØF CSLIPV  ØØØ83*ØØ386 ØØ417
B ØØ33 CTEMP   ØØ1Ø9*ØØ4Ø4 ØØ4Ø5 ØØ4Ø8 ØØ4Ø9 ØØ526 ØØ527 ØØ533 ØØ534 ØØ989 ØØ99Ø
               ØØ991 Ø1Ø69 Ø1Ø82 Ø1Ø89 Ø1Ø99
P Ø288 CTLP1   ØØ5Ø2 ØØ5Ø6*
P Ø28D CTLP2   ØØ5Ø5 ØØ52Ø*
P Ø2A6 CTLP2A  ØØ531 ØØ533*
P Ø2B4 CTLP3   ØØ535 ØØ54Ø*
P Ø2BA CTLP4   ØØ538 ØØ539 ØØ543*
P Ø2CC CTLP5   ØØ549 ØØ552*
P Ø2D2 CTLP6   ØØ548 ØØ555*
P Ø2DB CTLP6A  ØØ556 ØØ559*
P Ø2EØ CTLP7   ØØ551 ØØ554 ØØ558 ØØ561*
P Ø2E4 CTLP8   ØØ5Ø8 ØØ563*
P Ø318 CTLS    ØØ594 ØØ598 ØØ599*
P Ø32F CTLS1   ØØ583 ØØ611*
P Ø335 CTLS2   ØØ61Ø ØØ622*
B ØØ37 CTRIA   ØØ113*ØØ5Ø3 ØØ641 ØØ643 ØØ648 ØØ935 ØØ953 ØØ959 ØØ962 ØØ97Ø ØØ998
               Ø1ØØ3
P Ø1D4 CTRL    ØØ399*
P Ø214 CTRL1   ØØ427 ØØ43Ø*
P Ø225 CTRL1A  ØØ437 ØØ439*
P Ø22D CTRL2   ØØ44Ø ØØ443*
P Ø4C4 DELAY   ØØ2Ø5 ØØ253 ØØ9ØØ*ØØ9Ø7
P Ø4CA DELAY1  ØØ9Ø2*ØØ9Ø5
P Ø43D DEVSEL  ØØ219 ØØ459 ØØ8Ø9*ØØ869
B ØØØ8 DIA     ØØØ75*ØØ271 ØØ3Ø2 ØØ665 Ø1Ø14
B ØØØ9 DIB     ØØØ77*ØØ672
P ØØØD DIRQ    ØØ136*ØØ324 ØØ34Ø
P Ø6D8 DIV     ØØ483 Ø13Ø6*
P Ø6DE DIV2    Ø13Ø8*Ø131Ø
B ØØ2E DIVW    ØØ1Ø7*ØØ476 ØØ521 Ø1276 Ø1279 Ø1283 Ø1285 Ø13Ø6 Ø13Ø7 Ø13Ø8 Ø13Ø9
               Ø1311 Ø1316 Ø1318 Ø1321 Ø1323 Ø1326 Ø1328 Ø1331 Ø1333
B ØØØA DOB     ØØØ79*ØØ212 ØØ326 ØØ376 ØØ677 ØØ68Ø ØØ681 ØØ716 ØØ719 ØØ72Ø ØØ741
               ØØ744 ØØ748
P Ø433 DOUTA   ØØ2ØØ ØØ21Ø ØØ225 ØØ248 ØØ255 ØØ298 ØØ32Ø ØØ329 ØØ332 ØØ787*ØØ916
               ØØ923 Ø1ØØ5 Ø1Ø24
P Ø438 DOUTB   ØØ2Ø2 ØØ214 ØØ327 ØØ379 ØØ749 ØØ8Ø1*
P ØØØE EIRQ    ØØ137*ØØ181 ØØ231 ØØ653
B ØØ14 ERR     ØØØ86*ØØ446 ØØ447 ØØ477 ØØ488 ØØ53Ø ØØ585 ØØ587
B ØØ12 ERRA    ØØØ85*ØØ41Ø ØØ411 ØØ443 ØØ444
P Ø14D ESHUTD  ØØ319*ØØ669 ØØ7Ø4 ØØ737
P Ø719 ETBLTE  ØØ689 Ø1357*
P ØØBC EXECA   ØØ234 ØØ243*ØØ268 ØØ27Ø ØØ288
P ØØCD EXECA1  ØØ25Ø*ØØ257
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 P 011E EXECB   00294*
 P 012D EXECB1  00295 00300*
 P 0142 EXECB2  00304 00310*
   0010 FILE    00012*00125
 B 0006 FREQ    00073*00256 00344 00357 00358
 P 0637 FUNC    00486 00957 00966 01158*01163
 P 0640 FUNC1   01160 01164*
 P 0621 GAIN    00474 01140*
 P 062F GAIN1   01143 01146*
 B 0028 HOTF    00101*00691 00707 00713
 B 0001 IBAT    00068*00767
   0003 IBAT.   00048*00765
 B 002A ICOUNT  00103*00245 00282 00284 00289 00345
 B 0025 IDIRF   00098*00244 00276 00279 00306 01013 01020 01023
 B 001E INC     00093*00600 00601 00605 00608 00609
 B 0018 INCI    00090*00489 00493 00494 00624 00625
 B 0020 INCO    00094*00590 00591 00592 00593 00602 00603 00606 00607 00613 00614
 B 001A INCP    00091*00563 00564 00622 00623
 B 001C INCPO   00092*00523 00546 00547 00561 00562 00565 00566 00567 00568
 P 000F INIT    00121 00140*
 P 0068 INIT1   00178 00187*
 P 0473 INPUT   00176 00353 00455 00664 00671 00846*00890
 P 0172 INT     00340*01474
 P 019A INT1    00357*
 P 01B4 INT1A   00364 00367 00371*
 P 01C7 INT2    00375 00381*
 P 0368 INTE    00371 00631 00650*
 P 0238 INTV    00454*
 P 0251 INTV1   00457 00474*
 P 027A INTV1A  00490 00492 00494*
 P 0344 INTV2   00464 00630*
 P 0349 INTV3   00632*00634
 P 0365 INTV4   00642 00644 00649*
 P 000B IPOMAX  00134*00550 00553
 P 000C IPOMIN  00135*00557 00560
 P 0568 IROT    00299 01013*
 P 057C IROT1   01018 01022*
 P 0581 IROT2   01016 01021 01024*
 P 0009 KFREQ   00131*00421
 B 0010 KGAIN   00084*00481 00482 00528 00529
 P 0008 KLOW    00130*00584
 P 0006 KMOT    00128*00428
 P 000A KPOT    00132*01071
 P 0007 KREG    00129*00430
 P 0005 KVHZ    00127*00400
 P 00E0 MODE    00183 00261*00314
 P 00EA MODE1   00262 00266*
 P 00F4 MODE2   00265 00271*
 P 0105 MODE3   00275 00279*
 P 010A MODE3A  00278 00282*
 P 0113 MODE3B  00283 00286*
 P 011A MODE4   00273 00277 00280 00289*
 P 011D MODE5   00285 00287 00290*
 B 0024 MODEF   00097*00243 00269 00294 00310 00369
 P 0687 MP8     00401 00418 00431 00478 00586 01072 01192 01228*01256
 B 002D MULT    00106*01228 01233 01237 01241 01245
 P 044E OUTPUT  00788 00802 00823*00996 01000 01058
 B 000B PER     00081*00266 00360 00361 00365 00413 00581 01036 01045 01050 01114
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                 01140 01141
 P 071B PERMAX 01042 01363*
 P 071A PERMIN 01039 01362*
   E401 PIA1AC 00026*00144 00150 00812 00814 00835 00837 00855 00858 00886 00888
   E400 PIA1AD 00025*00147 00154 00810 00833 00851 00884
   E403 PIA1BC 00028*00145 00152 00826 00830 00848 00853 00877 00881
   E402 PIA1BD 00027*00148 00153 00828 00831 00850 00857 00879 00882
   E410 PTM1CX 00032*00161 00169 00182 00232 00325 00341 00654
   E412 PTM1LC 00034*00171 00992
   E413 PTM1XX 00035*
   E411 PTM2CS 00033*00166 00173 00179 00229 00342 00651 00903 00919
   E414 PTM2LC 00036*00901 00918
   E415 PTM2XX 00037*
   E416 PTM3LC 00038*00163 00180 00230 00343 00652
   E417 PTM3XX 00039*
 P 06B7 QDIV   00545 01276*
 P 06C2 QDIV1  01278 01281*01284
 P 06D0 QDIV2  01286 01288*
 P 04DA RCOM   00223 00295 00330 00915*
 P 05B8 REG    01047 01069*
 P 05D7 REG0   01079 01084*
 P 05E6 REG0A  01086 01091*
 P 05EF REG1   01081 01096*
 P 05F5 REG1A  01088 01095 01099*
 P 05FE REG2   01083 01090 01101 01104*
 B 0027 REGF   00100*01080 01087 01091 01102
 B 0005 REGV   00072*00761 01070
   0000 REGV.  00045*00756
 P 0386 SAFET1 00668 00670*
 P 0399 SAFET2 00675 00679*
 P 0376 SAFETY 00221 00250 00313 00663*
 P 06A6 SCALE  00422 01256*
 P 0152 SHUTD  00324*01476
 P 016D SHUTD1 00334*00335
 B 0029 SHUTF  00102*00693 00699 00701 00728 00732 00734
 P 05FF SINTR  00373 01114*
 P 0604 SINTR1 01116*01120
 P 061D SINTR2 01122 01125 01130*
 B 0003 SLIPD  00070*00261 00355 00426 00439 01048
 B 0026 SLIPF  00099*00300 00309 01053
 B 0004 SLIPM  00071*00263 00351 00383 00385
   0001 SLIPM. 00046*00349
 P 0585 SMAX   00381 01036*
 P 059E SMAX1  01040 01043 01047*
 P 05AB SMAX2  01049 01053*
 P 05B0 SMAX3  01052 01055*
 B 000E SMAXV  00082*00382 01056 01076
 P 0000 START  00121*01475 01477
 B 0016 STR    00088*00213 00378 00747 01124 01126
 B 0017 STRF   00089*00374 01128 01130
 P 064B TBL    01145 01181*
 P 0643 TBL16  01149 01173*
 P 0647 TBL4   01046 01177*
 P 0645 TBL8   01175*
 P 0744 TBLCOR 00485 01419*
 P 0761 TBLGHI 01144 01452*
 P 0750 TBLGLO 01148 01430*
 P 072D TBLSIN 01115 01391*
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P Ø71C TBLSP   Ø1Ø37 Ø1367*
P Ø7ØE TBLTEM  ØØ689 ØØ692 Ø1346*
P Ø73C TBLVTR  ØØ956 ØØ965 Ø1411*
B ØØ3Ø TEMP    ØØ1Ø8*Ø1181 Ø1182 Ø1184 Ø1185 Ø1186 Ø1189 Ø1195
P Ø39F TEMPØ   ØØ689*
P Ø3A9 TEMP1   ØØ693*ØØ7Ø3 ØØ712
P Ø3C2 TEMP2   ØØ698 ØØ7Ø5*
P Ø3C9 TEMP3   ØØ7Ø6 ØØ7Ø8*
P Ø3DB TEMP4   ØØ714 ØØ718*
B ØØ2C TIME    ØØ1Ø5*ØØ2Ø4 ØØ252 ØØ9Ø6
  ØØØC TOØ.    ØØØ57*Ø1346
  ØØØD TO1.    ØØØ58*Ø1349
  ØØØE TO2.    ØØØ59*Ø1352
  ØØØF TO3.    ØØØ6Ø*Ø1355
P Ø65F TRUNC   ØØ445 ØØ626 Ø12Ø6*
P Ø67E TRUNC1  Ø12Ø9 Ø121Ø Ø1214*
P Ø686 TRUNC2  Ø12Ø7 Ø1213 Ø1219*
B ØØØØ VBAT    ØØØ67*ØØ764 ØØ769 Ø1Ø78 Ø1Ø85
  ØØØ2 VBAT.   ØØØ47*ØØ762
P Ø4FF VCORR   ØØ632 ØØ945*
P Ø51E VDEC    ØØ946 ØØ962*
P Ø533 VDEC1   ØØ964 ØØ972*
P Ø53C VDEC2   ØØ971 ØØ974 ØØ976*
B ØØØ2 VHZ     ØØØ69*ØØ348 ØØ399
  ØØØ6 VHZ.    ØØØ51*ØØ346
P ØØØ4 VHZM    ØØ126*ØØ4Ø6
P Ø5Ø3 VINC    ØØ948*
P Ø5ØE VINC2   ØØ95Ø ØØ953*
P Ø51D VINC3   ØØ952 ØØ955 ØØ96Ø*
B ØØ22 VLOOP   ØØØ95*ØØ461 ØØ627 ØØ63Ø ØØ633
P Ø53D VOUT    ØØ649 ØØ936 ØØ982*
B ØØ23 VSIGNF  ØØØ96*ØØ463 ØØ628 ØØ645 ØØ945
P Ø495 WDOG    ØØ227 ØØ311 ØØ334 ØØ868*ØØ9Ø2
P ØØ6D ZERO    ØØ189*ØØ192
P Ø4F1 ZVOLT   ØØ216 ØØ246 ØØ333 ØØ931*
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APPENDIX VI

TEST INSTRUMENTATION SPECIFICATIONS

TECHNICAL SPECIFICATION

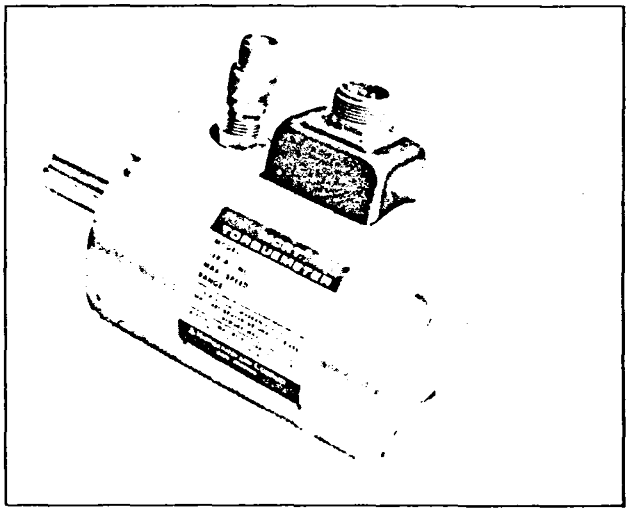
MCRT®9-02T Non-Contact Torquemeter

MAX. TORQUE–10,000 lb.-in.
SPEED – 0-7,500 rpm

GENERAL DESCRIPTION

The MCRT®9-02T is a general purpose, high accuracy shaft torquemeter ideal for continuous dynamometer readout and torque feedback applications. Six standard torque ranges provide maximum power capacities from 60 to 1200 horsepower. Performance is independent of speed from stall through 7,500 rpm.

The MCRT®9-02T uses a rotating strain gage torque bridge, temperature compensated for drift and modulus. The bridge is connected to a stationary electronic readout by integral, non-contact rotary transformers. The device is immune to water, lubricants, coolants, vibration, etc. and elimination of slip rings permits very low level measurements and long maintenance-free life. Thrust and bending loads are inherently cancelled by the transducer design. Factory options include an integral, non-contact speed pick-up and a foot mount.



Linearity: 0.1%

Temperature Effects: From 75 to 175° F maximum drift is 0.2% of full scale and maximum error due to modulus change is 0.2% of reading.

Maximum Operating Temperature: 220° F, assuming permanent lubrication. Above 175° F, the maximum shaft speed may have to be de-rated.

Readout: Any carrier amplifier suitable for strain gage service may be used.

Excitation Voltage: 10 volts rms, maximum.

Nominal Output: 0.75 millivolts/volt (open circuit).

Standard Ratings:

MODEL	FULL SCALE TORQUE	TORSIONAL STIFFNESS	MAXIMUM ROTATING INERTIA	MAXIMUM WEIGHT
MCRT® 9-02T	(lb. – in.)	(lb. – in./rad.)	(in. – oz. sec.^{2})	(lbs.)
–(5-2)	500	117,000	0.151	17
–(1-3)	1,000	197,000	0.152	17
–(2-3)	2,000	260,000	0.154	17
–(4-3)	4,000	427,000	0.186	22½
–(6-3)	6,000	515,000	0.188	22½
–(1-4)	10,000	605,000	0.192	22½

Overload Capacity: 2 times full scale rating

Shaft Speed: 0 to 7,500 rpm bi-directional. Optional speed pick-up produces 60 pulses per shaft revolution.

Construction: Load carrying member is 17-4 PH high strength stainless steel.

NOTES:

[1] Maximum speed rating assumes permanent lubrication. Consult factory for higher ratings.

[2] When mounted as a floating shaft, residual shaft mis-alignment to driving and driven shafts should be taken up with single flexible couplings and the stator assembly compliantly restrained. When a foot mount is used, double flexible couplings should be employed.

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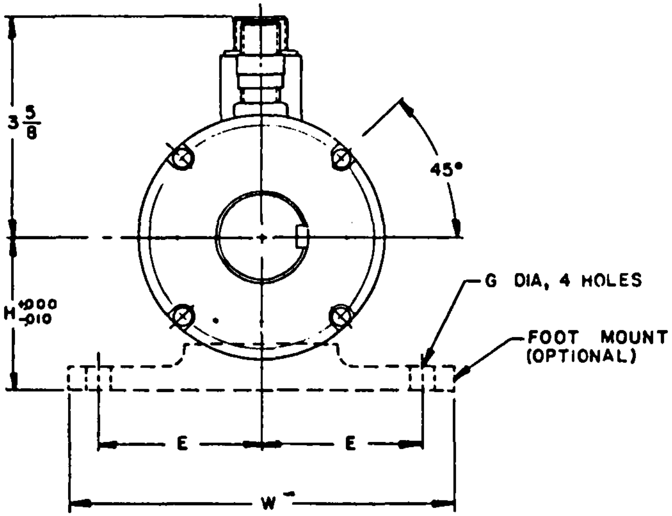
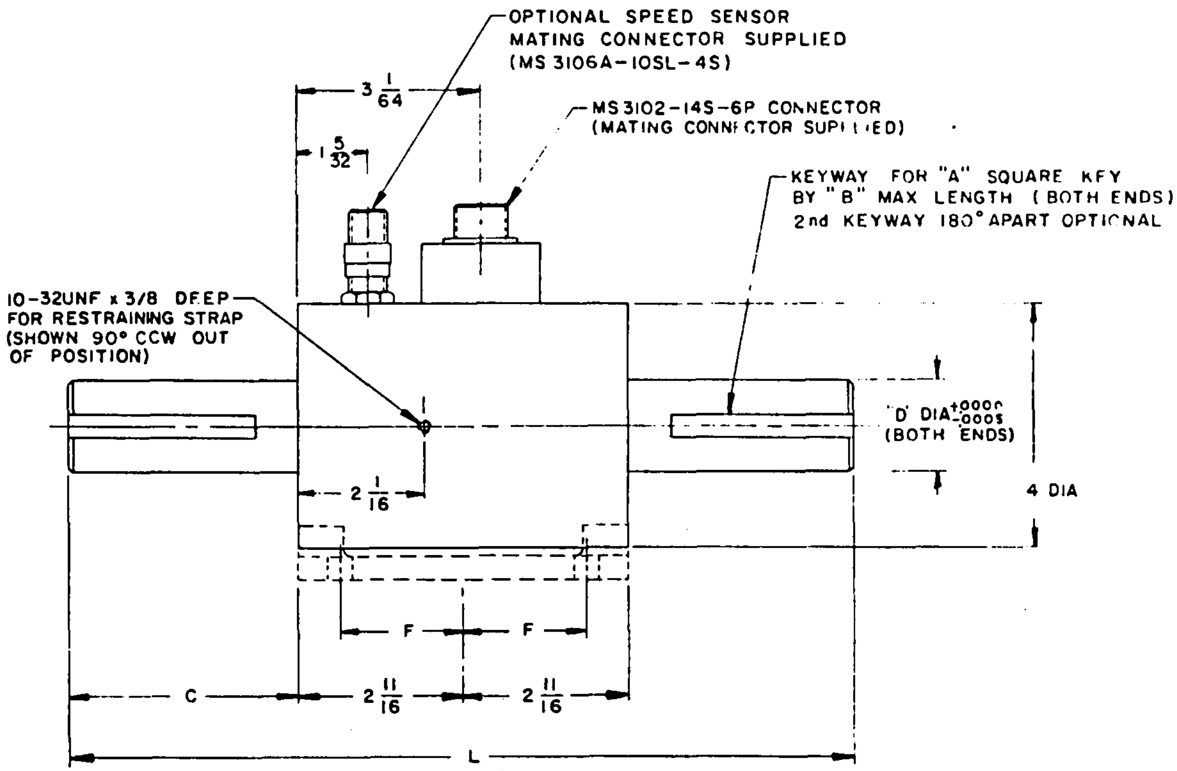
103/5-75 Patented





1. RPM RANGE: 0-7500 RPM

MODEL NO 9-02T	TORQUE RANGE LB. INCH	DIMENSION									
		A	B	C	D	E	F	G	H	L	W
5-2	0-500	.25	1.75	2.31	1.000	2.625	1.500	.41	2.500	10.00	6.25
1-3	0-1,000										
2-3	0-2,000										
4-3	0-4,000	.37	2.75	3.69	1.500					12.75	
6-3	0-6,000										
1-4	0-10,000										

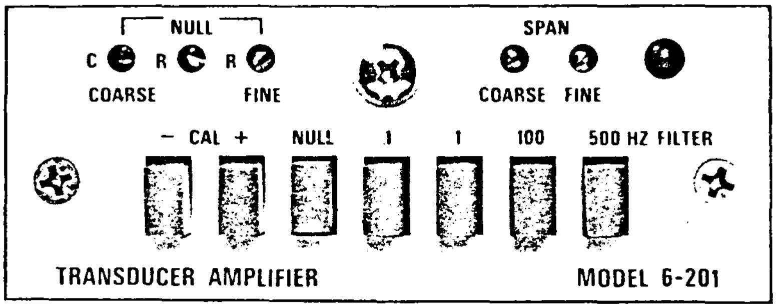
MCRT® 9-02T

BULLETIN 621

SYSTEM 6 Module Data Sheet

S. HIMMELSTEIN & CO.

TRANSDUCER AMPLIFIER MODEL 6-201



- HIGH ACCURACY
- 100 MEG INPUT RESISTANCE
- RATIOMETRIC OPERATION
- UNSURPASSED NOISE IMMUNITY
- BESSEL RESPONSE OUTPUT FILTER
- NEGATIVE SPAN ADJUSTMENT

Description

The Model 6-201 is a truely universal Transducer Amplifier. It will handle directly-wired or transformer-coupled strain gage transducers or, LVDT's. No effort has been spared to provide the most stable, accurate and noise-free performance obtainable. When incorporated in a SYSTEM 6, the module is complete in all respects; it provides transducer excitation, transducer balance, zero set, span set, switchable low pass filtering, dual polarity shunt calibration and output buffering functions. Versatility and high accuracy are enhanced by provision for 4, 6 or 7 wire input connections.

A-c excitation yields extremely stable operation and high sensitivity while eliminating the effects of thermocouple and galvanic voltages, voltages induced by rotating machinery or a-c magnetic fields and other industrial noise sources. While such noise immunity is inherent in a carrier amplifier with phase sensitive detection, the Model 6-201 attains a new level of noise immunity that is especially meaningful in noisy industrial environments. Such immunity is achieved, in part, by the unique detector circuit which yields unsurpassed quadrature rejection, by the incorporation of low level active filtering and by the very high Common Mode Rejection (CMR). The use of low level filtering increases the effective CMR ratio and prevents large, normal mode, noise signals from overloading the amplifier and causing reading errors. Additional normal mode rejection is provided by an active, output filter with switch selectable bandwidths. This Bessel response filter avoids data distorting group delays and overshoot errors that occur with other types. The very low cut-off frequencies provide long term signal averaging and prevent roll-over of the last display digit, even in the presence of ultra low frequency variations.

The 6-201's very high input impedance eliminates errors from shunting type balance controls found in older instruments. Stable, internally generated balancing voltages are summed with the residual transducer unbalance after the high impedance, differential input amplifier. An independent, Negative Span Adjustment is available to compensate for transducer with imperfect symmetry. This provides correct system symmetry when several transducer channels share a digital display.

The 3 kHz oscillator is amplitude-locked to the ultra-stable SYSTEM 6 reference. Additionally, the actual bridge excitation voltage is feedback locked via 6 (or 7) wire sensing to the system reference thus providing ratiometric operation. In the unlikely event the system reference changes, both the sensitivity of the digital indicator and the bridge excitation voltage change in the same ratio. Hence, the displayed digitized output will remain unchanged i.e., the equivalent system gain is independent of the reference.

The module includes SYSTEM 6 address decoding circuitry and will generate legend, A/D Converter Scaling, 5th digit blanking and decimal point location commands in accordance with switch-programmed, field-changeable instructions. A front panel LED indicates when the module output is addressed for display on the digital indicator.

Specifications, Model 6-201

Transducer Type: . . . . . Any strain gage transducer either directly wired or transformer coupled. Will also handle 1/4 and 1/2 bridges and LVDT* Transducers.
Transducer Impedance: . . . . 80 to 2000 ohms
Transducer Connections: . . . . . Provision for 4, 6 or 7 wire circuits
Transducer Cable Length: . . . . up to 5000 feet
Transducer Excitation:
Amplitude: . . . . 6 volts rms, regulated
Frequency: . . . . . 3 kHz ± 1%. Provision included for frequency "slaving" to other 6-201 modules.
Calibration: . . . . Dual-polarity shunt calibration with provision for CAL resistor feedback
Sensitivity: . . . . 0.1 mv/v, minimum
Sensitivity Range: . . . . . . Minimum SPAN adjust range from 5.0 to 0.1 mv/v via multi-turn, COARSE and FINE front panel controls. Negative SPAN independently adjustable over a 2% range
Input Impedance: . . . . 100 megohm shunted by 20 pf independent of NULL control settings.
Common Mode Rejection (CMR): . . . . 120 db, minimum
Normal Mode Rejection: . . . . At least 120 db at 60 hertz with selectable filter in 500 hertz position
Quadrature Rejection: . . . . at least 60 db at 3 kHz
Null Control Range: . . . . 1 1/2 mv/v both in-phase (R) and quadrature (C) via multi-turn controls. COARSE and FINE control provided for in-phase (R) adjustment. Amplifier response is flat regardless of selected filter bandwidth when in the NULL mode. Releasing the NULL switch automatically re-engages the selected filter bandwidth.

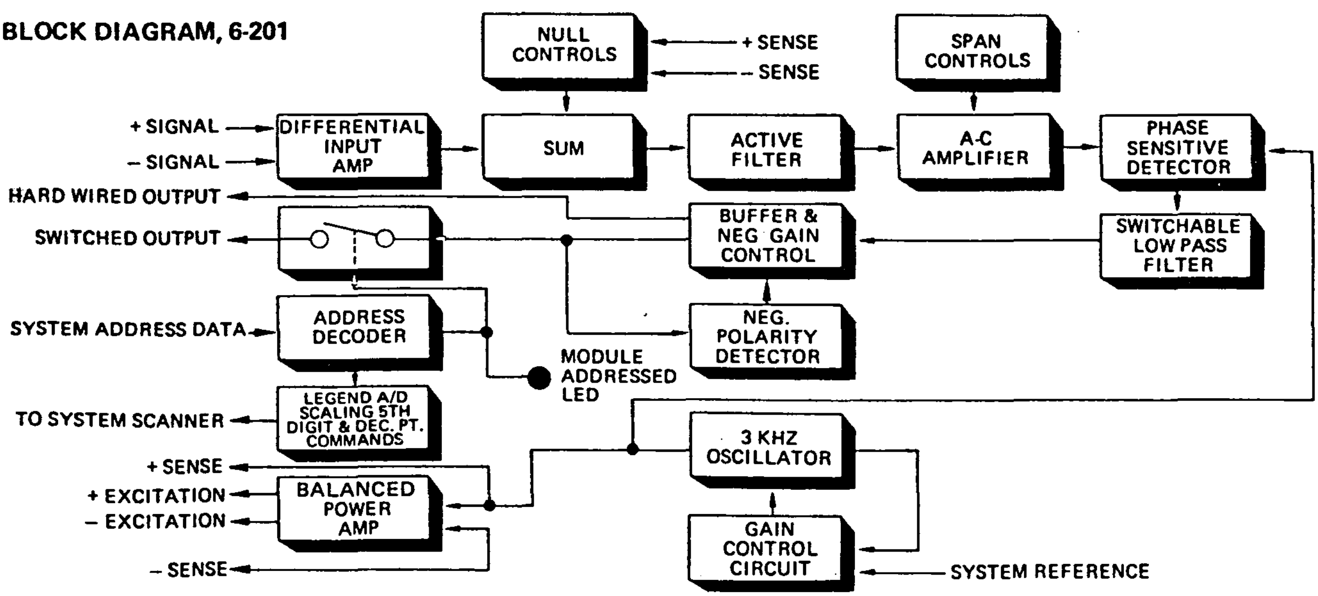
Analog Output: . . . . ±5 volts full scale with 40%** overrange at 5 milliamperes maximum
Output Impedance: . . . . Less than 0.1 ohms
Bandwidth: . . . . d-c to 0.1, 1, 100 or 500 hertz, switch selectable***
Signal-To-Noise-Ratio: . . . . 0.05% rms or better except 0.1% in 500 hertz bandwidth filter position
Switchable Filter Response Time: . . . . . . Assuming a step input, the filter output will reach the tabulated percentage of actual value in K/fc seconds where fc is the selected cut-off frequency

% of Actual Value	K
99.9%	2.0
99.0%	1.5
90.0%	1.0
63.2%	0.6

Filter Attenuation: . . . . 80 db per decade above cut-off frequency
Overall Accuracy: . . . . 0.05% of full scale. ****
Module Size: . . . . One standard width

NOTES:
- * *The 6-203 LVDT amplifier is recommended for dedicated LVDT Applications.*
- ** *See Bulletin 601 for separate A/D overrange specifications.*
- *** *Four individual pushbutton switches select desired response. When no filter switch is depressed, signal output is unfiltered.*
- **** *See Bulletin 601 for complete definition of operating conditions.*

BLOCK DIAGRAM, 6-201



S. HIMMELSTEIN & CO.
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OHIO SEMITRONICS WATT METER

SPECIFICATIONS:	Model PTP-948
INPUTS:	
Phase	3ϕ 3 wire, 30 4 wire
Voltage "fs"	120 VAC
range	0 to 150 VAC
overvoltage (continuous)	175 VAC
burden (per phase)	.1VA
Current "fs"	600 amperes ac
range	0 to 300 amperes ac
	0 to 600 amperes ac
overcurrent	10 times fs
burden	<.1VA
Power factor range	unity to 0 lead or lag
Frequency range	DC to 5K Hz ±1db
Response time	20 μsec to 90% fs
Isolation input/output/case	1500 VAC
Power ranges "fs"	(300A) 0 to 108 KW
	(600A) 0 to 216 KW
Accuracy (including setpoint, linearity, pf and temperature)	Analog ±0.5% fs
	Digital Meter ±1.0% fs
Instrument power	115VAC 10% 60 Hz
Current transducer size	4 1/8" x 5" x 1 1/4"
	2" dia.

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16. Abstract

A SCR ac motor controller for an electric vehicle application has been designed and constructed to excite a polyphase induction motor from a fixed 120-V dc propulsion battery source. The inverter, rated at 35-kW peak power, is fully regenerative and provides sufficient power to meet the SAE 227a Schedule d driving cycle if installed in a commuter style vehicle. Thyristors are employed for the bridge switching devices and the comutation devices and are arranged in a dc bus comutated topology to minimize the number of comutation circuit components required. The controller was measured to have a peak efficiency of 95% at peak power. Retail costs of the ac motor/motor controller package in 100K/year quantities is projected to be $1500 (FY79).

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