SHUTTLE SPECTRUM DESPREADER

FINAL REPORT

21 MAY 1976

TRW No. 28453
CDRL No. 0002

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
JOHNSON SPACE CENTER
HOUSTON, TEXAS

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA 90278

SHUTTLE SPECTRUM DESPREADER

FINAL REPORT

21 MAY 1976

TRW No. 28453
CDRL No. 0002

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
JOHNSON SPACE CENTER
HOUSTON, TEXAS

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA 90278

CONTENTS

CONTENTS (Continued)

ILLUSTRATIONS

ILLUSTRATIONS (Continued)

ILLUSTRATIONS (Continued)

ILLUSTRATIONS (Continued)

FIGURE 12 — A COMPARISON OF WEATHER TYPES AND WATER LEVELS IN THE LAC DES ALLEMANDS AREA

ILLUSTRATIONS (Continued)

TABLES

1. INTRODUCTION AND SUMMARY

This report summarizes the results of the spread spectrum despreader project. The project was conducted by TRW Systems for the Johnson Space Center of the National Aeronautical and Space Agency under contract NAS 9-14690. The period of performance was from June 1975 to May 1976.

The project produced three principal products:

1) A spread spectrum despreader breadboard, acceptance tested at TRW April 28-29, 1976 by NASA representative, J. Fowler.

2) Associated test equipment consisting of a spectrum spreader and bit reconstruction/error counter, also acceptance tested at TRW on April 28-29, 1976. These two items were delivered to NASA on 30 April 1976 with demonstration to NASA personnel on May 10-11, 1976.

3) Paper design of a Ku-band receiver which would incorporate the despreader as a principal subsystem. This design was described in the second design review on 15 September 1975.

The despreader and test set are designed for maximum flexibility. A choice of unbalanced quadriphase (UQPSK) or biphase (BPSK) shift keyed data modulation is available. Selectable integration time and threshold voltages on the despreader further lend true usefulness as laboratory test equipment to the delivered hardware. Table 1-1 shows the despreader design and performance values. Figures 1-1 and 1-2 are photographs of the despreader and test set drawers, respectively.

Table 1-1. Despreader Design and Performance Values

IF Input and Despread Output

Frequency	110 MHz
Input Power	-15 dBm ±1 dB
Output power	-22 dBm ±1 dB
Input Bandwidth	30 MHz
Impedance	50Ω ±20%
Carrier Doppler	±450 kHz

PN Code Characteristics

Code Rate	14.1 Mcps
Code Doppler	±460 chips/second
Code Search Increment	1/4 chip
Code Phase Dwell Time (Search)	361 μsec synchronous or 40 μsec -1 msec asynchronous
Code Phase Integrator Dump Time	11 μsec

Performance	Units	UQPSK		BPSK	
		Design	Measured	Design	Measured
$\overline{T}_{ACQ}$ (Average Acquisition Time)	sec	<10	<6.6	<10	<4.6
Minimum C/N_0 for $\overline{T}_{ACQ}$ < 10 sec	dB-Hz	68	66	60	53
BER Degradation	dB	<1.0	<0.8	<1.0	<0.8
Code Doppler Pull-In Range	Hz	±460	±600	±460	±500
Probability of Detection		>0.9	0.99	>0.9	∼0.95

Figure 1-1. K-Band Despreader
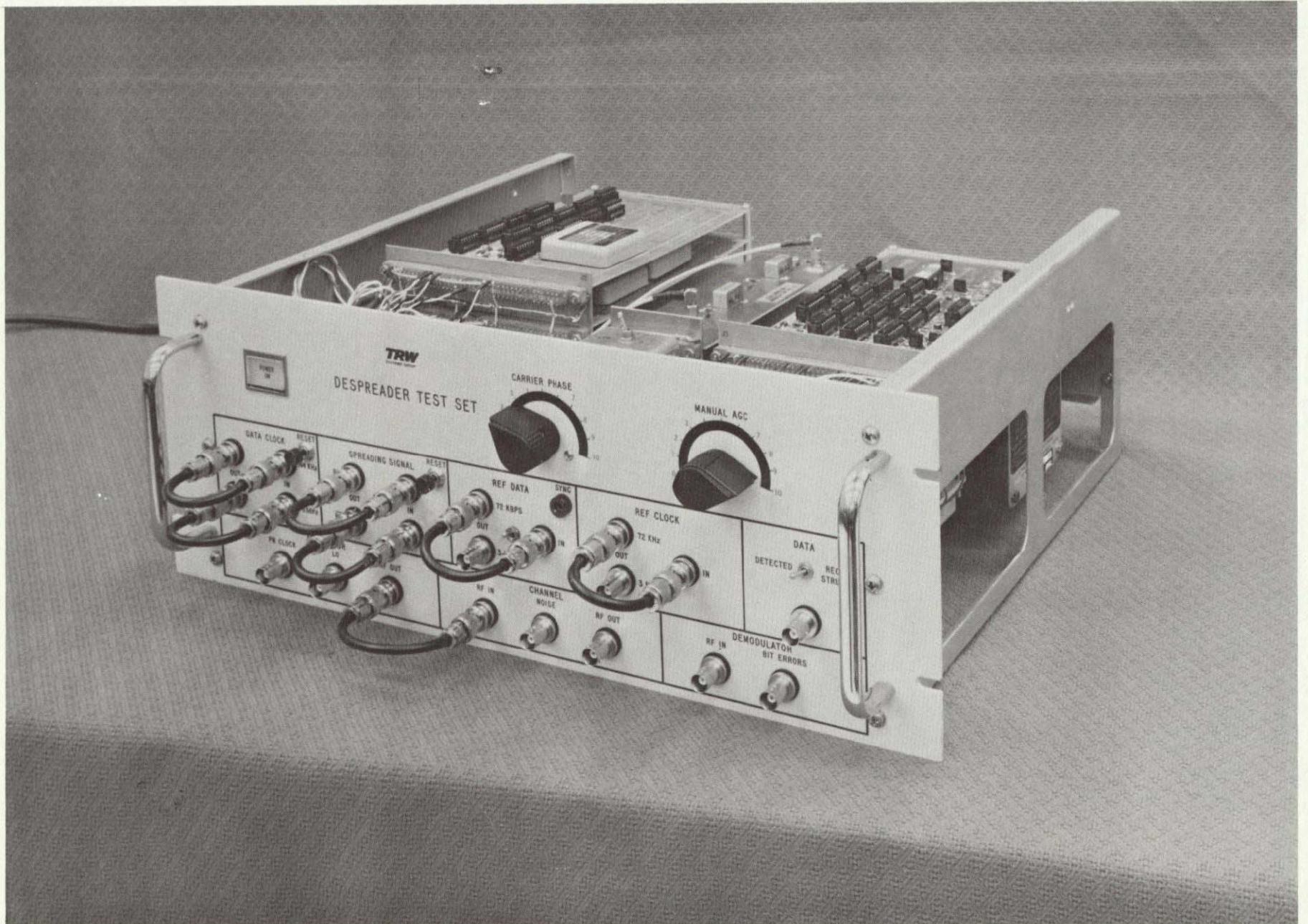
Figure 1-2. Despreader Test Set

2. SYSTEM OPERATION

The K-band despreader and test set have two entirely different modes of operation: 1) a 72 kbps and 3 Mbps, unbalanced quadriphase-shift keyed modem (UQPSK); and 2) a 216 kbps biphase-shift keyed modem (BPSK). Both units have been optimized for performance in either mode, with minimal changes. Because the original contract called for only the UQPSK modem, most nomenclature (including panel labelling) pertains directly to that mode of operation.

The 216 kbps (BPSK) mode primarily utilizes the 72 kbps channel circuitry and panel connections of the test set. Conversion of the test set is performed by making the following changes:

1) A single toggle switch on the rear panel of the test set must be set to the "216 kbps" position.

2) The proper modulator PC board must be installed in the middle of the top of the test set chassis. Two separate PC boards are provided — one for either modem. Only two cable connections plus the plug-in edge connector are made to either board.

3) The proper "receiver" input bandpass filter of the test set (located in a vertical bank of three tubular filters on the bottom of the chassis) must be connected. A 12 MHz data bandwidth filter (for UQPSK) and a 2 MHz data bandwidth filter (for BPSK) are permanently mounted in the test set. Either filter can be selected by cabling.

The despreader also requires few changes between modes. Again a single toggle switch on the rear panel alters most of the circuits as necessary. The only other modification is the selection of the proper bandpass filters (for determining post-correlation bandwidth). Two sets of three filters are permanently mounted in the despreader. The UQPSK filters (750 kHz helical resonator filters) are located underneath the RF PC board on the top of the despreader chassis and have white cables. The 1.5 MHz tubular filters (for the BPSK mode) are mounted on the rear panel and have tan-colored coax cables going to the RF PC board. All connectors are color-coded (red, orange, and yellow) to distinguish between the three channels of the despreader analog circuits. A row of dummy connectors (parallel to the rear panel) is provided on the RF PC board to anchor all unused filter cables.

2.1 72 KBPS/3 MBPS UQPSK MODE

Figures 1-1 and 1-2 show the despreader and test set. Data for the
test set is derived from two PN generators, one controlled by a 144 kHz crys-
tal oscillator, the other by a 6 MHz crystal oscillator. The oscillators
are packaged units producing TTL level outputs and are mounted on the data
generator boards. Twice the data rate is needed for the clock frequency
of the data generators so that a simple phase-shifter may be used to delay
the clock for signal demodulation. A divide-by-two circuit downconverts the
oscillator frequency to the necessary clock signal for driving the shift
registers of the PN generators.

The 144 kHz clock drives the 72 kbps data generator, which is a 10-bit
shift register producing a PN word 1023 (2^{10} - 1) chips long. The 3 Mbps
data generator uses a longer code (2^{13} - 1) produced by a 13-bit shift
register. Both data generators are reset to the initial (all "0") state
by a single switch on the front panel.

A third generator is utilized in the test set to produce the PN code
for spread spectrum modulation. This shift register is clocked by a 14.1
MHz external signal applied to a connector on the front panel. The genera-
tor is an 11-bit shift register producing a 2047-bit word (2^{11} - 1), uti-
lizing the 9 and 11 feedback taps. A reset switch is also available on the
panel for initializing the spreading code.

A simplified block diagram of the test set (Figure 2-1) shows how these
signals are used to modulate the 110 MHz carrier. The modulation processes
occur on the modulator PC board. The carrier is taken from the front panel,
divided in a two-way power splitter, and brought onto the modulator PC
board through a coax cable. An internal 110 MHz crystal oscillator has an
output on the rear panel of the test set which may be cabled directly to
the front panel for use when no Doppler simulation is required. If Doppler
is desirable, an external signal at +3 dBm must be used.

On the modulator PC board the carrier is first divided by a 90 degree
hybrid into two separate channels — I and Q. The I channel is then attenu-
ated 6 dB and modulated by 3 Mbps data, the data spectrum appearing as in
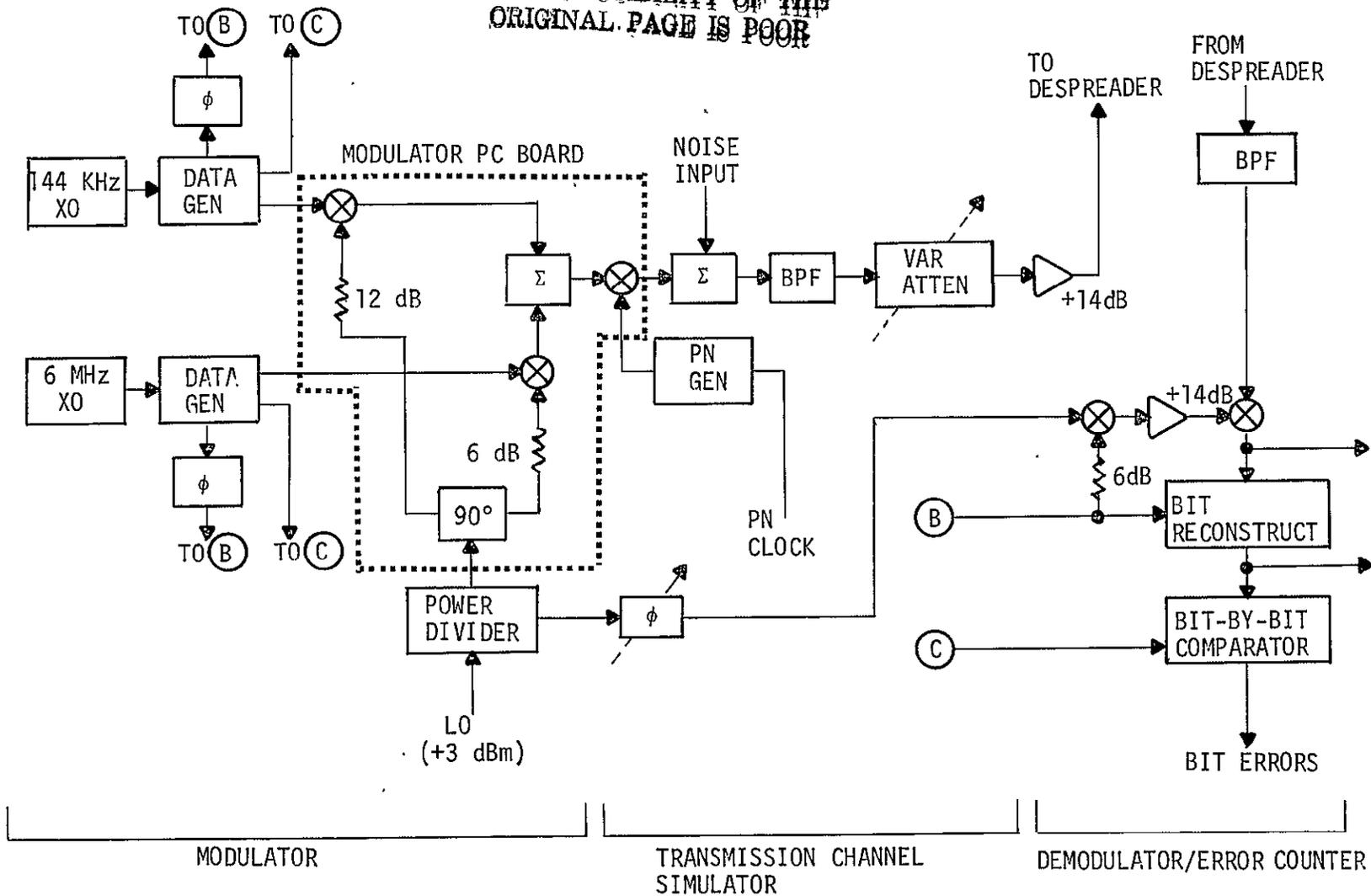
Figure 2-1. Test Set Block Diagram, UQPSK Mode

Figure 2-2 (with the Q channel unmodulated). The Q channel is attenuated
by 12 dB and then modulated by the 72 kbps data to produce the data spec-
trum shown in Figure 2-3. (Again only one channel is modulated for the
photograph). This creates the 4-to-1 power split between the quadriphase
channels. The two channels are then summed and spread by the 14.1 Mcps PN
code. The data modulated spread spectrum signal (appearing as shown in
Figure 2-4) is then cabled from the modulator PC board to the MODULATOR RF
OUT connection on the test set panel. This provides a monitoring point for
analyzing the spread spectrum signal. During normal use, the signal is
simply cabled back into the CHANNEL RF IN port, also located on the front
panel.
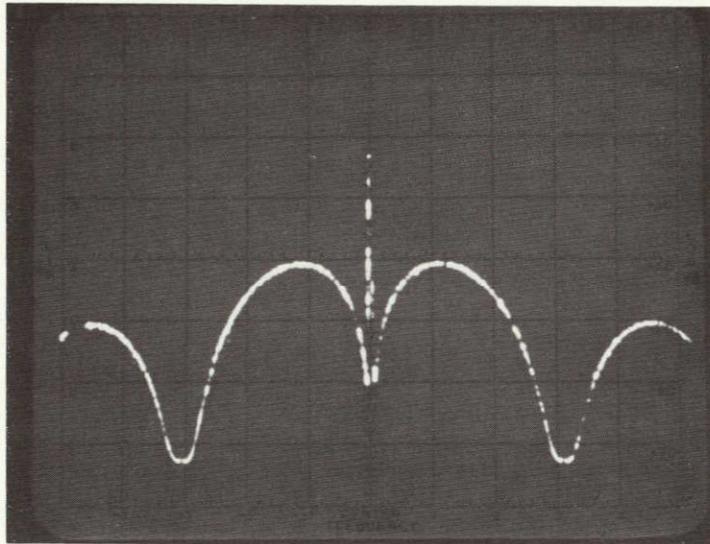
Vert: 10 dB/div   Hor: 2 MHz/div

Figure 2-2.   3 Mbps Data Spectrum

The modulated signal is summed internally with noise from the CHANNEL
NOISE port on the panel. The source for this noise can either be wideband
noise at 110 MHz from an external source or an internal noise generator
(having its output on the rear panel). The total signal plus noise is then
bandpass filtered to a 30 MHz bandwidth, amplified, level adjusted by the
MANUAL AGC attenuator, and brought to the CHANNEL RF OUT port on the panel
for use by the despreader. The effects of data modulation and noise on the
output PN code modulated signal of the test set are illustrated in Figure
2-5 a) through e).
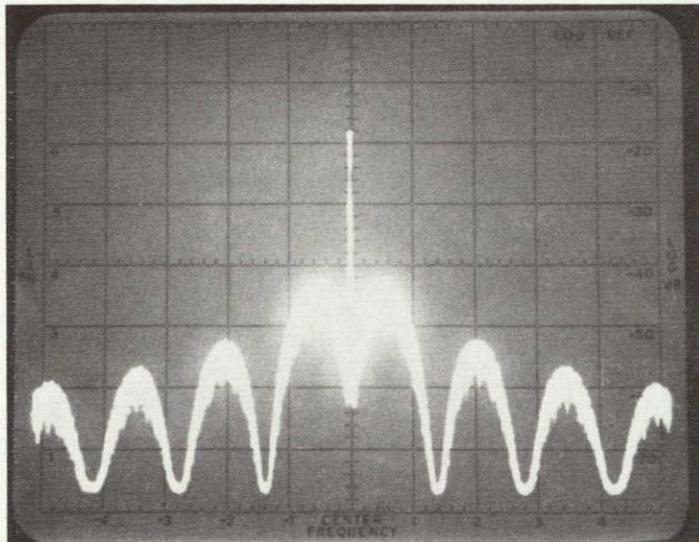
Vert: 10 dB/div

Hor: 100 kHz/div

Figure 4-2. 72 kbps Data Spectrum
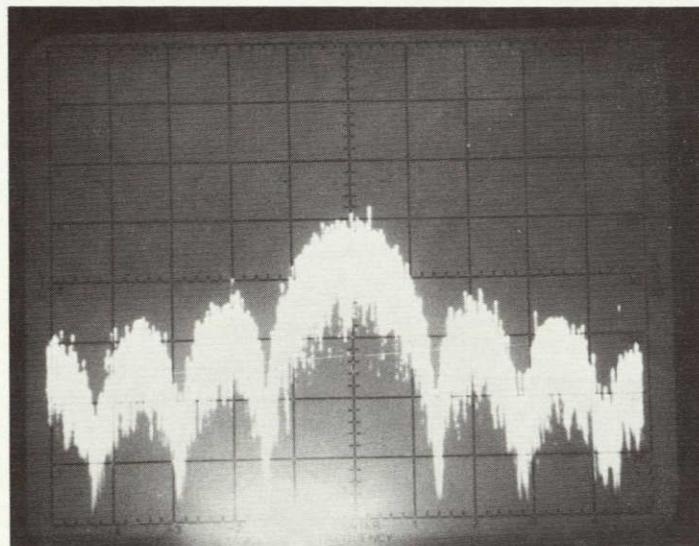
Vert: 10 dB/div

Hor: 10 MHz/div

Figure 4-3. 14.1 Mbps PN Spectrum
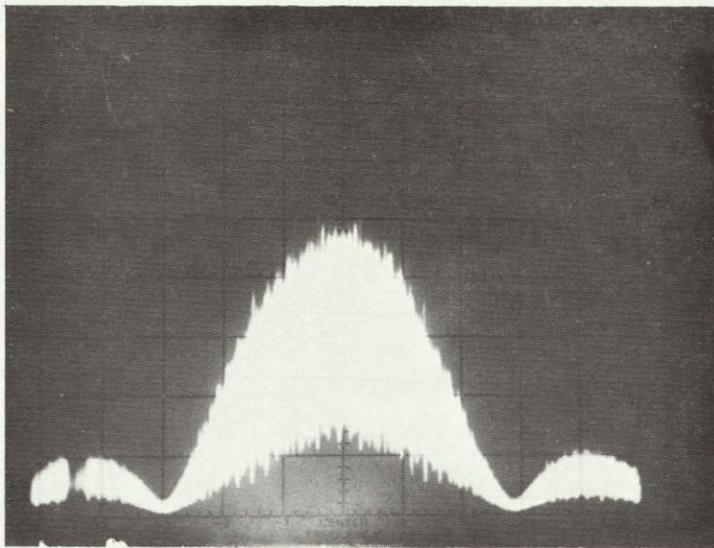
a. Carrier Only

    f_c = 110.000 MHz

    f_{code} = 14.1 MCPS

    5 MHz/cm - horizontal scale

    Linear vertical scale
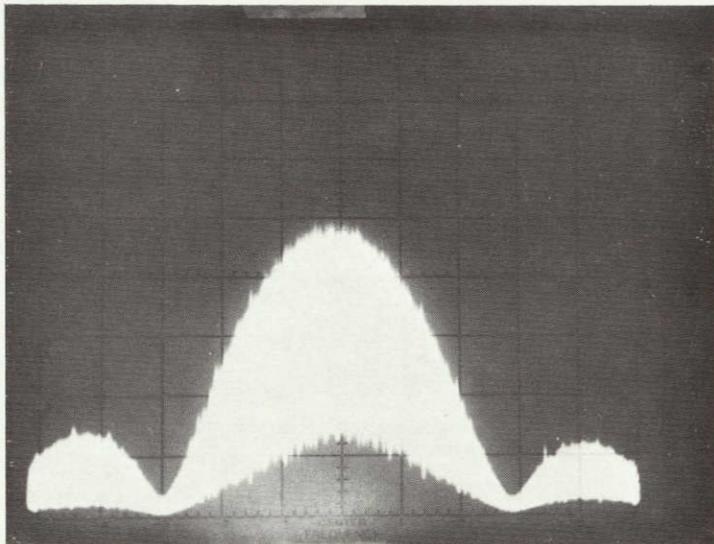
b. I channel unmodulated -
       80% of total power

    Q channel - 72 KBPS -
       20% of total power
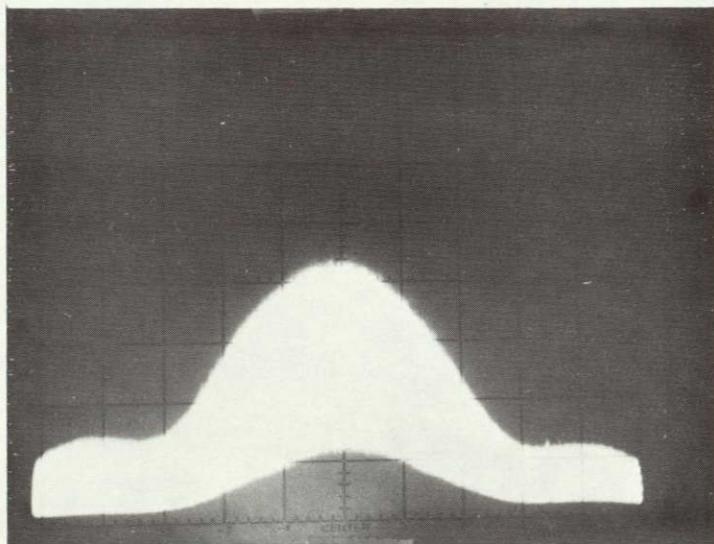
c. I channel - 3 MBPS -
       80% of total power

    Q channel - 72 KBPS -
       20% of total power

Figure 2-5. Spread Spectrum Signals
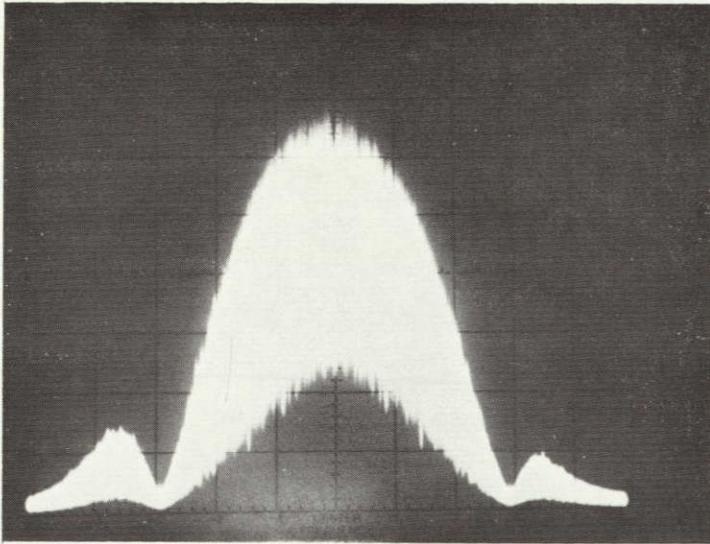
d. Spread Spectrum Signal of Figure 2 after passing through 30 MHz Wide Band Pass Filter
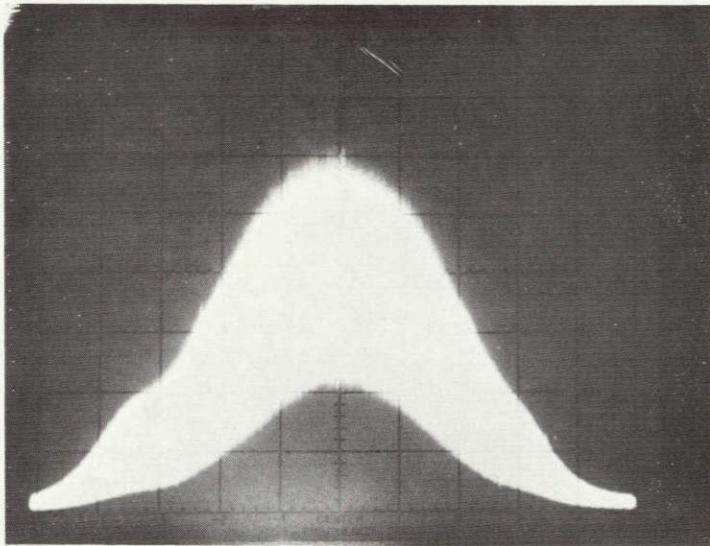
e. Spread Spectrum Signal of Figure 3 after passing through 30 MHz Wide Band Pass Filter

Figure 2-5. Spread Spectrum Signals (Continued)

The test set provides a -15 dBm noisy spread spectrum UQPSK signal to the DESPREADER IN port on the front panel of the despreader. As the despreader block diagram shows (Figure 2-6), the incoming signal is divided into three channels — two are used for acquisition (the punctual and reference channels); the third is used during tracking.

During acquisition the tracking channel is inactive. A FET switch grounds the output of the loop filter so that only a dc signal controls the VCXO. The VCXO is set to one of two selectable frequencies (chosen to divide the total code frequency range into two regions for positive and negative Doppler).

At the initiation of acquisition, the phase of the locally generated PN code is at an arbitrary orientation to the test set (i.e., transmitted) PN code. That is, the two PN words are randomly positioned with respect to each other when acquisition is started. The exact logic sequence followed is shown in Figure 2-7.

An initial code phase is tried for a dwell time of 361 μsec. The output of the summer (which subtracts the uncorrelated reference signal from the punctual signal) is integrated during this period. If at the end of one dwell time the integrated voltage does not exceed a certain threshold (established at zero by control of channel gains), the local PN code is slipped a quarter-chip, and the integration and decision process is repeated. When threshold is exceeded, quarter-chip stepping is inhibited and the tracking channel takes over.

A key element of the despreader is the subtraction of the reference and punctual channels. Mathematically, one subtracts the reference channel from the punctual channel, normalizes the punctual channel by dividing by the reference channel voltage (which reduces the effects of SNR and AGC variations), and sets threshold at a point above zero (shown by previous analyses to be 1.33 times the reference channel voltage). This is illustrated in Figure 2-8 a).

INPUT → P/S → ⊗ → COUPLER → BPF → DET → 30 KHz LPF → Σ

OUTPUT

PUNCTUAL CHANNEL

BPF → DET → 50 Hz LPF → GAIN ADJUST

REFERENCE CHANNEL

PUNCTUAL

INTEGRATE AND DUMP

PN GEN ← CODE CLOCK ← QTR CHIP STEP AND ÷4 ← ACQUISITION LOGIC ← THRESHOLD DETECTOR

LATE   EARLY

SW ← TIMESHARE

SW ← DOPPLER OFFSET

VCXO 56.4 MHz

Σ

TIME DELAY

BPF → DET → 30 KHz LPF → XY → LOOP FILTER

TRACKING CHANNEL
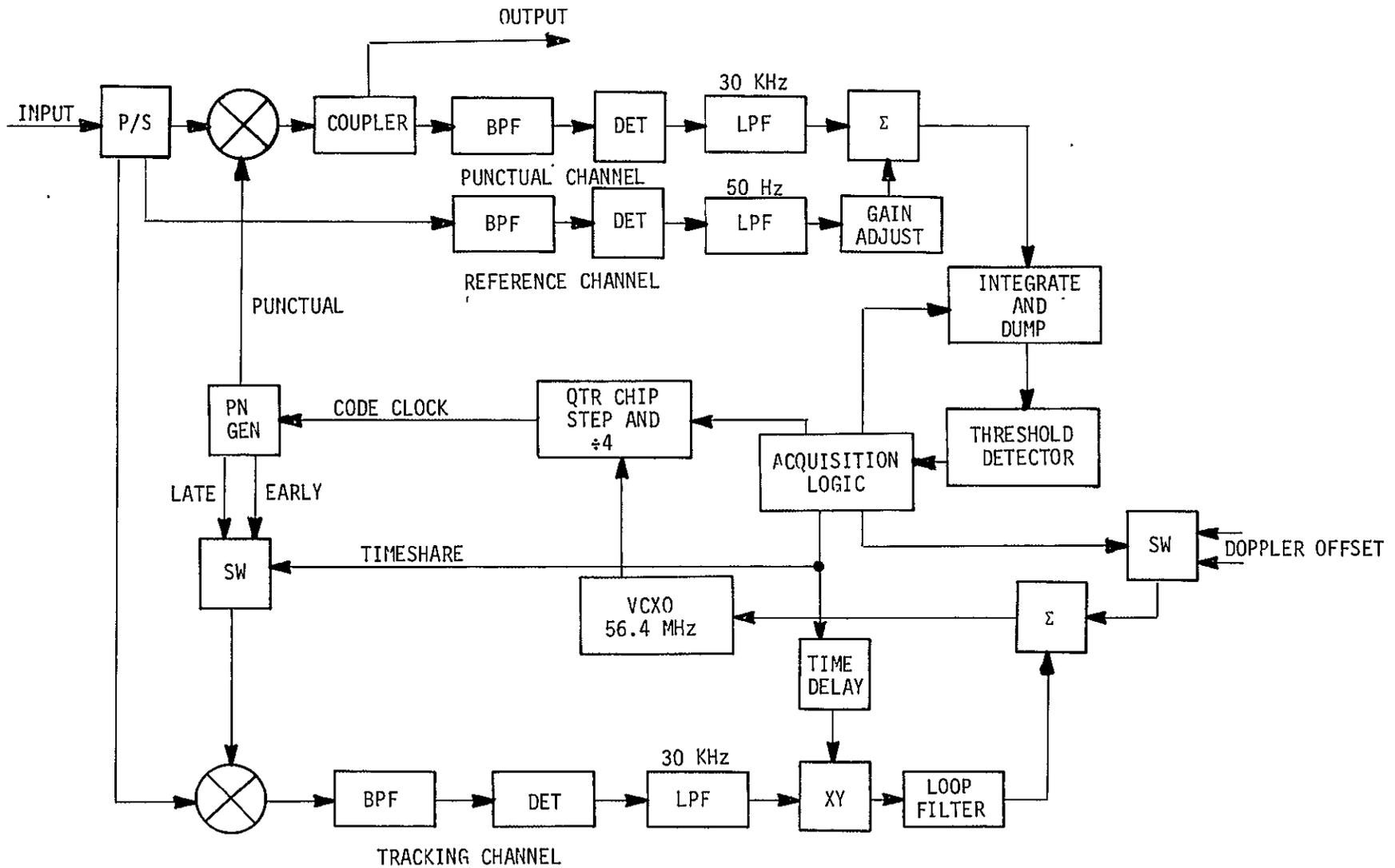
Figure 2-6. Despreader Block Diagram (Simplified)

Figure 2-7. Code Acquisition Logic and PN Generator Flow Diagram

$$V_{OUT} = \frac{V_{SIG} - V_{REF}}{V_{REF}} - V_{TH}$$

$$= \frac{V_{SIG}}{V_{REF}} - 1 - V_{TH}$$

$$= \frac{1}{V_{REF}} \left[V_{SIG} - V_{REF} (1+V_{TH}) \right]$$

a) Mathematical Model

$$V_{OUT} = V_{SIG} - K\,V_{REF}$$
$$\text{WHERE } K = 1 + V_{TH}$$
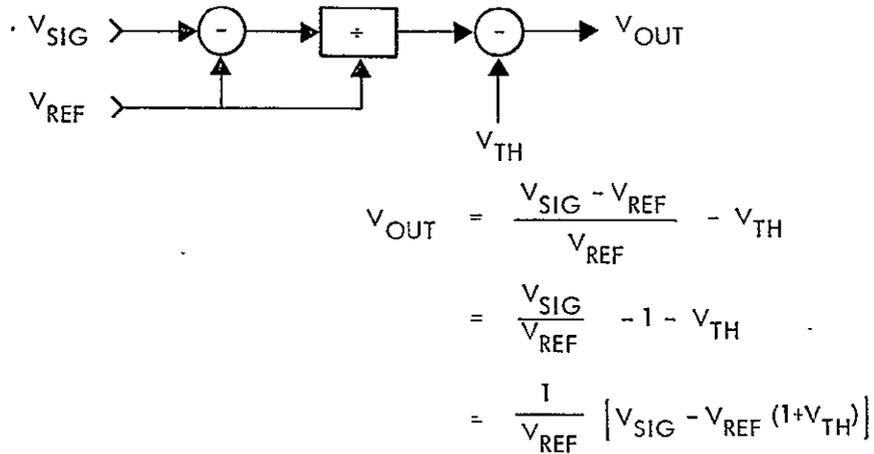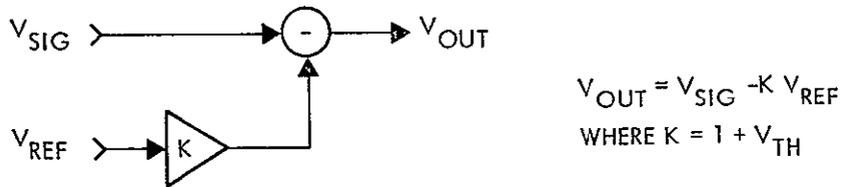
b) ·Hardware Realization

Figure 2-8. Normalization and Threshold of Punctual Channel

Note that the detection voltage is

$$V_{out} = \frac{1}{V_{ref}} \left[V_{sig} - V_{ref} (1 + V_{th}) \right]$$

where

$$V_{ref} = \sqrt{V_{noise}^2 + V_{spread\ sig}^2}$$

and

$$V_{sig} = \sqrt{V_{noise}^2 + V_{despread\ sig}^2}$$

This same process is implemented by the simple circuit of Figure 2-8 b). Except for a dc gain $1/V_{ref}$ which has no effect on a zero crossing threshold detector, the output is identical when $K = 1 + V_{th} = 1.33$. Appendix C includes measured data which illustrates the benefits (reduced SNR and AGC sensitivity) through this normalizing process.

The hardware realization incorporates operational amplifiers, electronic switches, and other imperfect devices which inject slight offsets, necessitating a small adjustment of threshold to balance the circuit. This offset can be modeled as an additional contribution to K in the equations of Figure 2-8.

Once acquisition threshold is exceeded, quarter-chip stepping ceases. The tracking channel, a delay locked loop aligns code phase, thereafter, by controlling the local PN code clock frequency. A 21.4 kHz early/late gating squarewave switches the correlating PN signal of the tracking channel between two states: one a half-chip ahead of the punctual local code and the other a half-chip late. (This is accomplished by tapping the shift register of the PN generator in the despreader). After filtering and detection, the tracking channel signal is processed through an X-Y multiplier which inverts the late signal, so that the loop filter output is approximately a dc signal corresponding to "early-minus-late." Figure 2-9 illustrates the generation of this tracking curve. Through careful selection of loop parameters (gain, filter cutoffs, etc.) the resultant signal is conditioned to drive the VCXO that clocks the PN generator, thereby closing the loop. High dc loop gain assures extremely small tracking error.

During tracking, the "on time" PN code is continually applied to the punctual channel correlator, and the integrator and threshold circuits monitor performance so that loss of lock can be detected, should it occur. A coupled port off the punctual channel, therefore, carries the desired despread signal, which is returned to the test set for demodulation and BER measurements. Examples of the despread spectrum are shown in Figure 2-10.

Upon its return to the test set via the DEMODULATOR RF IN port, the despread signal is bandpass-filtered to 12 MHz. The despread signal is simultaneously demodulated and converted from Bi-ϕ-L to NRZ format, by multiplying it by a carrier that has been PSK modulated by the data clock. The resultant is a downconverted "de-Manchestered" despread signal: that is, baseband data plus noise.
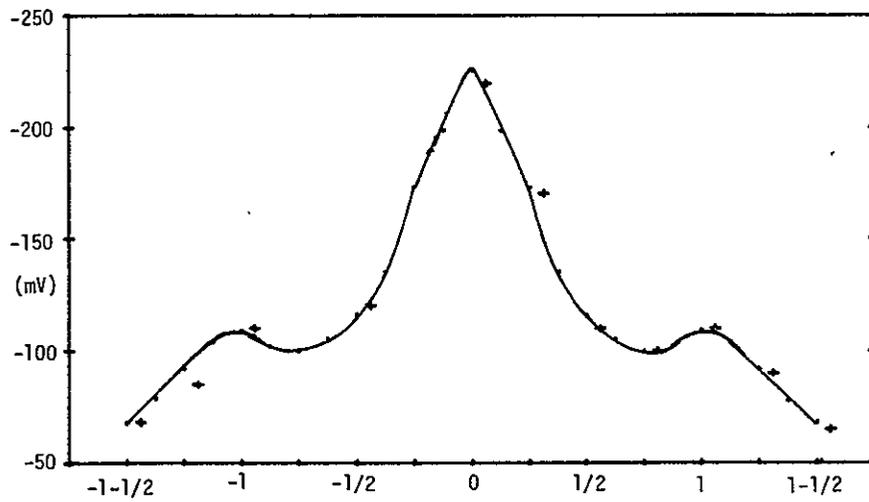
a. Correlation Peak (Inverted)
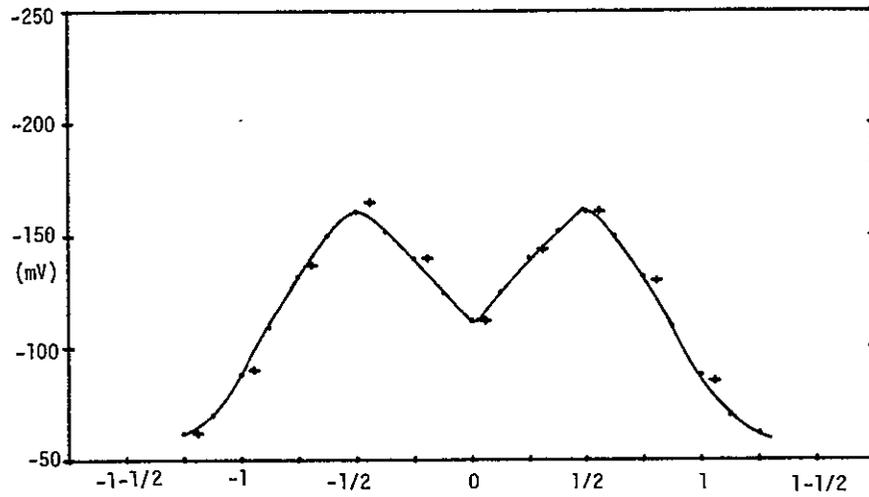
b. Tracking Channel Response Before X-Y Multiplier
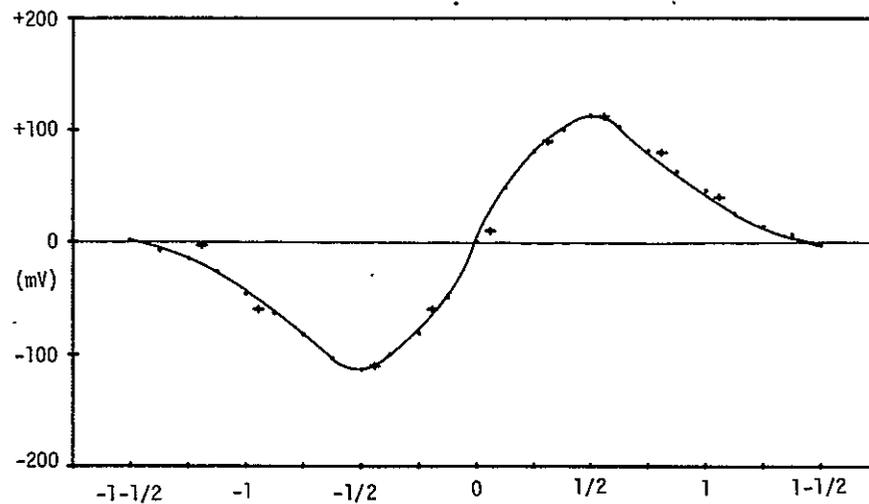
c. Tracking Channel Output (After X-Y Multiplier)

Figure 2-9. Tracking Curve Generation (Measured Data for UQPSK)

2-13
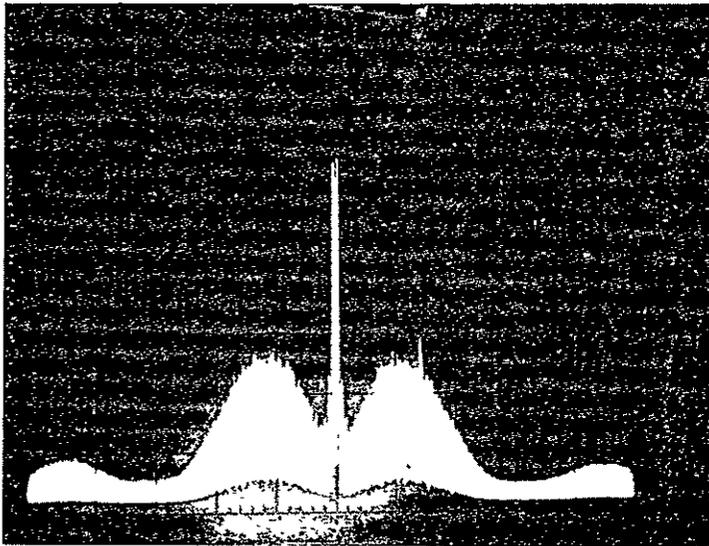
a). Despread Signal
   I channel=3MBPS-BiPhase L
      80% of total energy
   Q channel-72KBPS-BiPhase I
      20% of total energy

   Horizontal Scale: 2MHz/cm
   Vertical Scale: Linear
      f_c = 110.000 MHz
      f_{code} = 14.1 MCPS
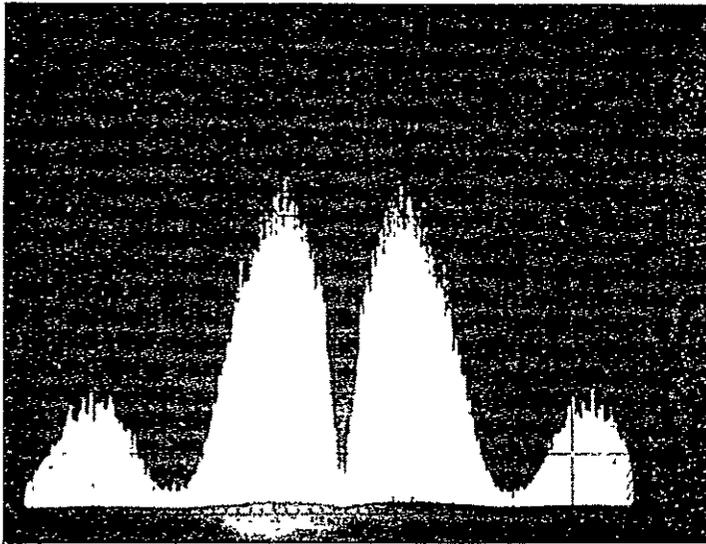
b). Despread Signal showing
    expanded center portion
    of Figure 6.

   72KBPS BiPhase L spectrum
   Horizontal Scale: 50KHz/cm
   Vertical Scale: Linear

Figure 2-10. Despread Signals

The phase-shifted data clock is the signal labelled on the test set front panel as REF CLOCK, selectable for either data rate to be 72 kHz or 3 MHz. Hard-wired phase-shifters on the data generator boards introduce time delays to match the signal delay in the despreader. The carrier phase is adjustable to either of the two states (0 or 90 degrees) necessary for demodulating the 72 kbps and 3 Mbps channels. This is accomplished by the CARRIER PHASE control on the front panel, in conjunction with the carrier phase switch accessible through the top cover of the test set.

The baseband data plus noise is processed by an integrate-and-dump bit reconstruct circuit to improve SNR and establish TTL levels for the data. The reconstructed data and reference data (selected for external monitoring via the REF DATA panel connections and switch) are compared and a single pulse is generated for each discrepancy which occurs. This is the DEMODU-LATOR BIT ERRORS output signal.

2.2 216 KBPS BPSK MODE

The operation of the test set and the despreader in the BPSK mode is very similar to that just described in Section 2.1 for the UQPSK mode. The format of data modulation is different, of course, but the same circuits are used wherever possible in performing similar functions.

In the BPSK mode, a 432 kHz crystal oscillator (mounted on the 72 kbps/ 216 kbps data generator board) drives the data generator, which is the same 10-bit shift register used for 72 kbps data. A phase-shifted downconverted clock at 216 kHz is also provided for later use in demodulating the despread signal. The PN code generator for the UQPSK mode is also used for the BPSK mode.

An external 14.1 MHz clock (from the test set panel MODULATOR PN CLOCK input) drives the 11-bit shift register, which produces the spreading PN code.

The carrier modulator is illustrated in Figure 2-11 — a simplified block diagram for the BPSK modem. The carrier is taken from the front panel MODULATOR LO input connection. Either the 110 MHz singal available at the
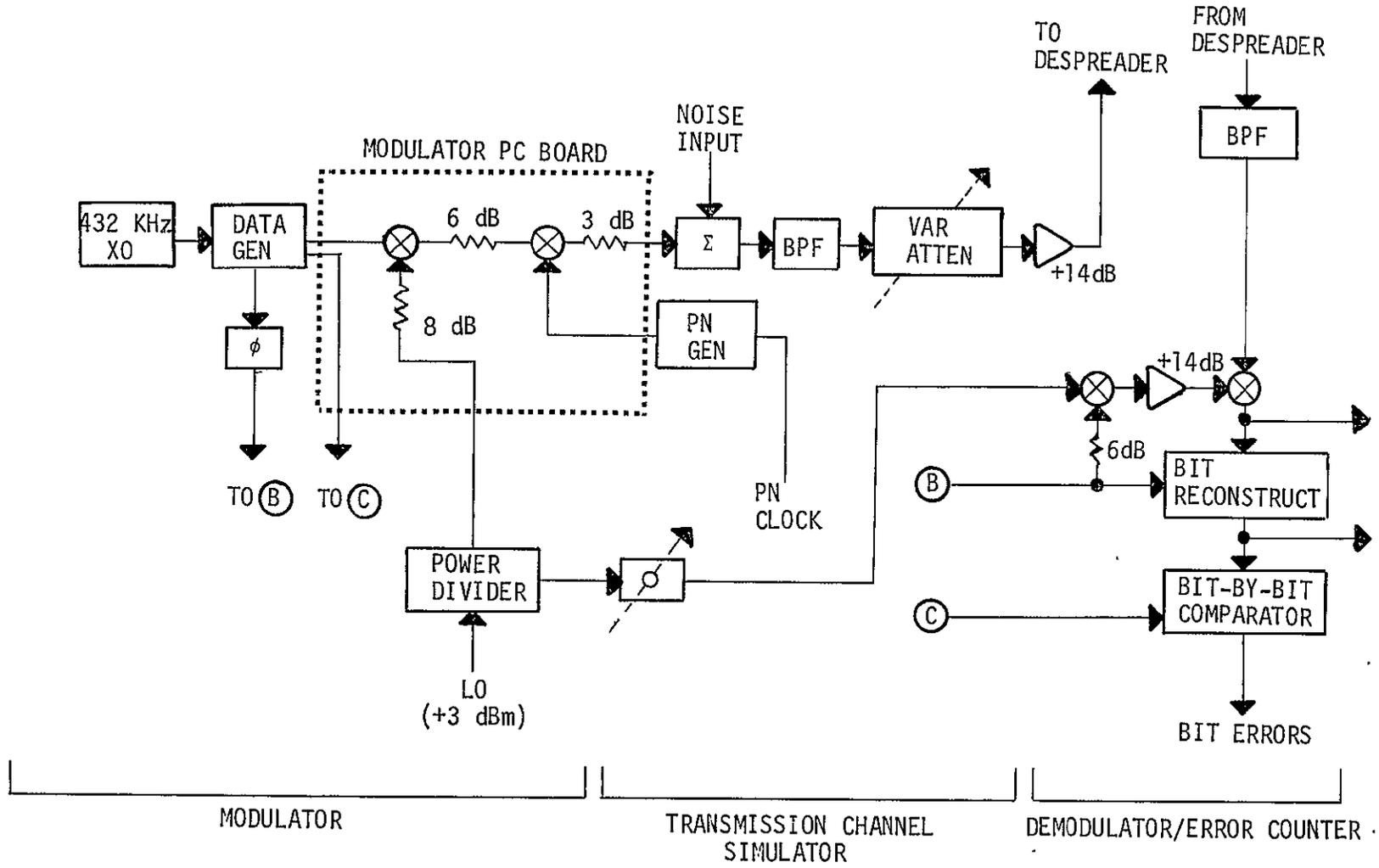
Figure 2-11. Test Set Block Diagram for BPSK

rear panel (if Doppler simulation is not desired) or an external 110 MHz signal at +3 dBm (Doppler desired) may be used. A two-way power splitter divides the carrier into signals used for modulation and demodulation.

A coax cable brings the carrier from the power splitter to the modulator PC board. The carrier is attenuated 8 dB, modulated by the Manchester-coded data signal (see Figure 2-12), and attenuated 6 dB more. The signal is then spread spectrum modulated by the 14.1 MHz PN code, attenuated 3 dB more, and finally carried from the PC board by another coax cable. The total signal attenuation on the BPSK modulator PC board is 5 dB greater than that of the UQPSK modulator PC board, in order to create decreased C/N_0 values corresponding to the lower transmitter power (40 dBw EIRP).

As in the UQPSK mode, the BPSK spread spectrum signal is brought to the front panel of the test set at the MODULATOR RF OUT port. This is connected to the CHANNEL RF IN port which carries the signal to a summer where noise is added (provided by the CHANNEL NOISE input). The total modulated signal-plus-noise is then filtered to a 30 MHz bandwidth, level adjusted (by the MANUAL AGC control), and returned to the panel at the CHANNEL RF OUT connection for presentation to the despreader.
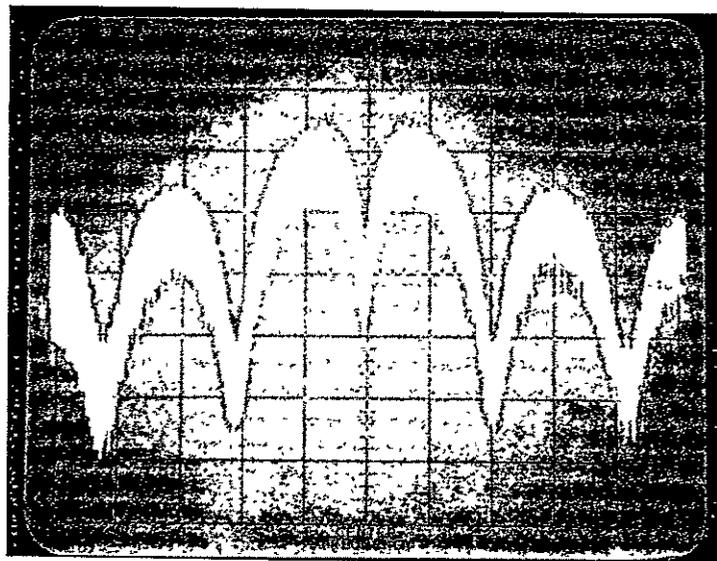
Vert: 10 dB/div   Hor: 200 kHz/div

Figure 2-12. 216 kbps Data Spectrum

The despreader functions basically in the same way as described previously for the UQPSK mode; (see Figure 2-6). The punctual channel provides the main acquisition signal, conditioned by the reference channel to lower sensitivity to SNR and AGC. Once threshold is exceeded, quarter-chip stepping ceases and the tracking loop aligns the PN codes by controlling the code clock VCXO. The despread output is coupled from the punctual channel.

There are significant differences to be noted, however. A primary change is the post-correlation bandwidth. This parameter is selected for optimum SNR through considerations of signal and noise spectral densities, as well as Doppler conditions. Essentially, the optimized bandwidth includes approximately 73 percent of the data energy under worst Doppler. Curves showing post-correlation SNR as a function of filter bandwidth for various C/N_0 values are presented in Figures 2-13 and 2-14 for 72 kbps Manchester-coded data and 216 kbps Manchester-coded data, respectively. The filter bandwidth producing the highest normalized SNR at maximum Doppler is this optimum.

An important difference between the two modes of despreader operation is found in the acquisition logic sequences. The UQPSK mode uses a double code search with Doppler offsets. This increases the SNR in the acquisition channels by halving the noise bandwidth and increases the correlation peak amplitude because the frequency uncertainty is reduced. The acquistion logic offsets the VCXO by half the maximum code Doppler, alternating between positive and negative offsets for each full sweep of the code phase. The BPSK mode has 7 dB more signal energy in the "acquisition data rate" spectrum. Even though the post-correlation filter bandwidth is larger and minimum C/N_0 is smaller, the BPSK mode acquires in a single search.

Because the BPSK mode uses single search, a number of circuits used for UQPSK are not needed. Aside from the obvious difference in logic requirements, the UQPSK mode utilizes dc offset voltages to pretune the VCXO code clock to frequencies in the middles of the two Doppler ranges (14.100230 and 14.099770 MHz). The BPSK mode simply sets the VCXO for the nominal clock of 14.100000 MHz. An asymmetry of the loop resulted in the need to offset the clock about -200 Hz. This is an implementation problem, however, entirely separate from what is being discussed here. The matter is described in detail in Section 3.2.
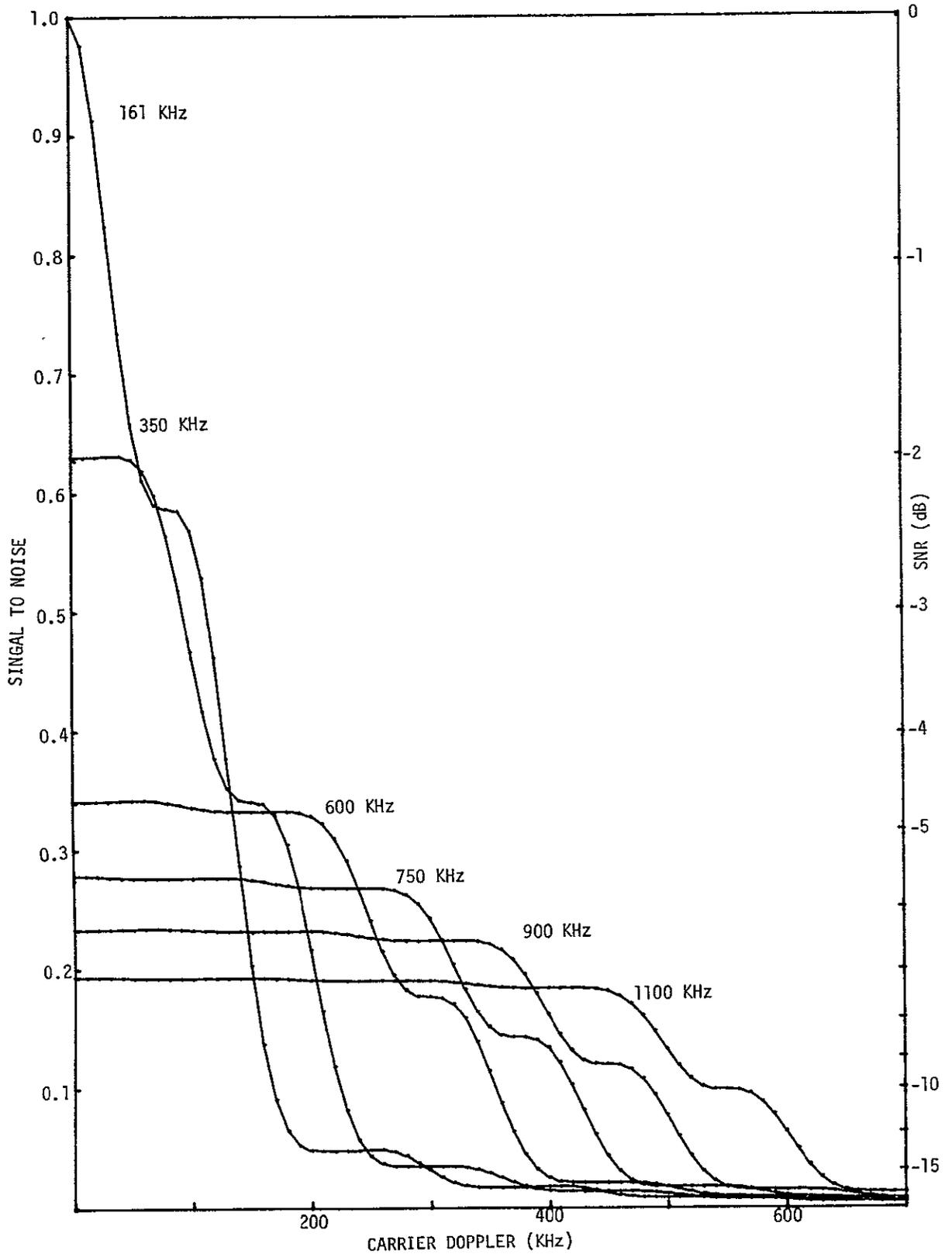
Figure 2-13.   Normalized Signal to Noise Versus Carrier
Doppler for Various IF Filter Bandwidths
(72 kbps)
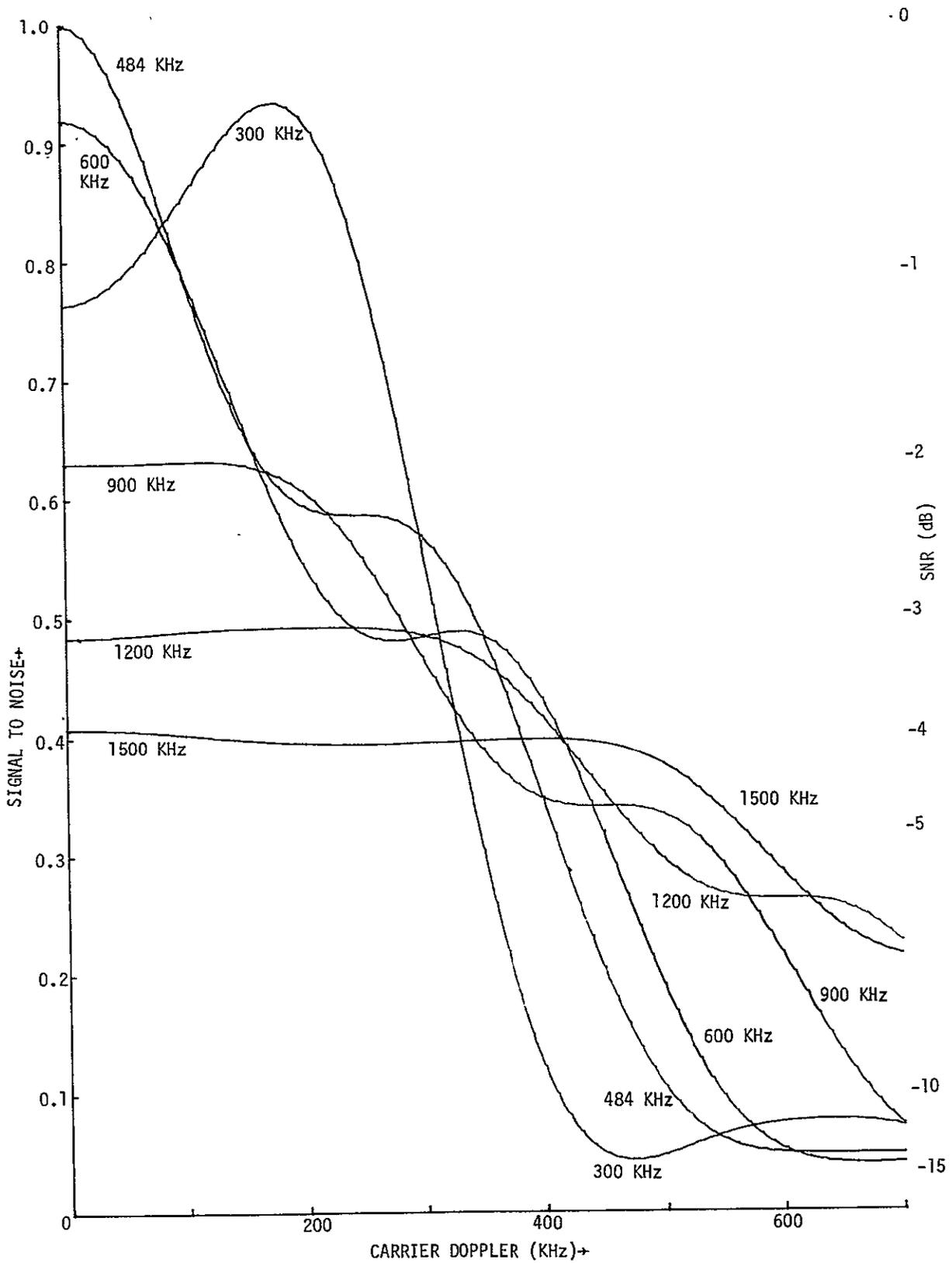
Figure 2-14.   Normalized Signal to Noise Versus Carrier
Doppler for Various IF Filter Bandwidths
(216 kbps)

Additional alterations are required in the despreader circuitry to adapt to the changed signal spectrum. The carefully set gains of the two channels used for acquisition — the punctual and reference channels — are different for the UQPSK and BPSK modes. Analysis shows that while the ratio of gains for UQPSK should be 1.33 for acquisition and 1.25 for tracking, the BPSK mode requires 1.1 for both. These changes are due to the difference in signal structure and minimum C/N_0 for acquisition.

One other significant change in the despreader circuitry is the loop filter of the delay locked loop. The single search of the BPSK mode requires roughly double the pull-in range needed for the UQPSK mode.

Code phase is measured by means of a combination of several components in the tracking channel, as was described previously for UQPSK operation. The S-curve generated has a slope which varies with signal strength, and the slope of that curve is one of the gains of the delay-locked loop, which influences pull-in range, damping, phase error, etc. Figures 2-15 and 2-16 show measured tracking curves for both modes. Changes in the loop filter were configured to widen the loop response.

The despread signal which is coupled from the punctual channel is returned to the test set for data demodulation and bit error measurements. The test set functions exactly as for the UQPSK mode, except that there is only one data channel and the REF DATA and REF CLOCK connections stay as for the 72 kbps data, but operate at the 216 kbps rate. There are, of course, some slight implementation considerations — bit reconstruct timing changes, for example. These are discussed in Section 4.5.

2.3 PANEL DESCRIPTIONS

This section is provided as a convenient reference for explaining the use of any panel connector, switch, adjustment, or test point found on either the test set or the despreader. The intended use of each item is briefly described to permit the reader to properly use the equipment and to supplement the detailed hardware descriptions of Sections 3 and 4.

2.3.1 Test Set Front Panel (See Figure 2-17)

POWER SWITCH. Illuminated push-type alternating action ac power switch. The test set requires 117 Vac power only.

Figure 2-15. UQPSK Tracking Curve
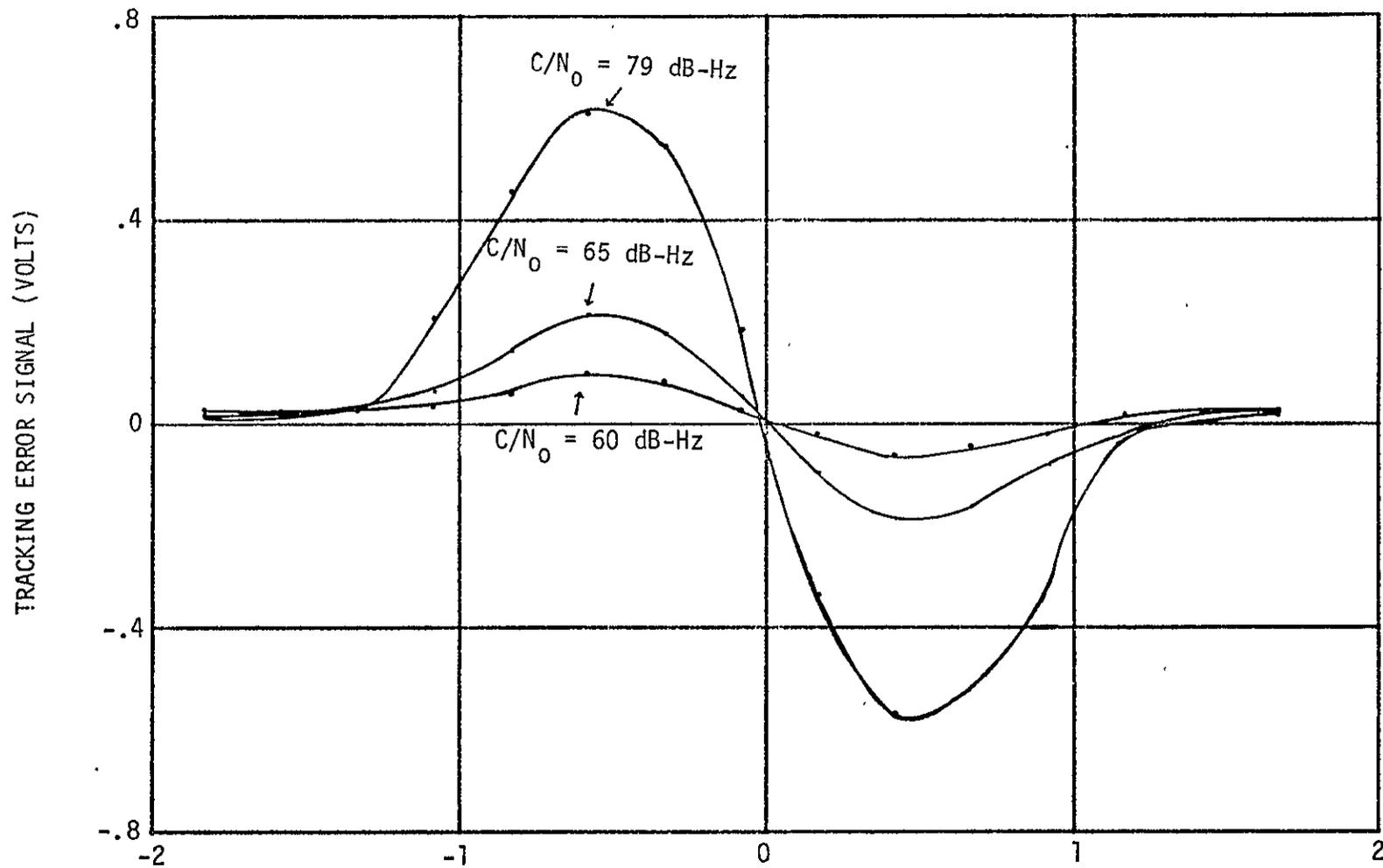
Figure 2-16. BPSK Tracking Signal

Figure 2-17. Test Set Front Panel

Figure 2-18. Test Set Rear Panel

CARRIER PHASE. This knob controls the phase shift of the carrier used in the bit reconstruct circuits of the demodulator. References are made in the acceptance test procedures to approximate dial settings necessary for demodulating any of the three data rates. A toggle switch accessible from the top of the test set acts in conjunction with this control.

A number of methods for finding the exact phase setting are possible. The best is to adjust the phase for minimum errors at the selected data rate, under minimum SNR conditions. Another is to monitor the DETECTED DATA output on an oscilloscope and adjust the phase for minimum deviation from a biphase-modulated waveform.

MANUAL AGC. The MANUAL AGC knob controls an attenuator which sets the level of the combined signal and noise power leaving the test set at the CHANNEL RF OUT port. Since the noise level can also be adjusted separately, the MANAUL AGC is used in setting the SNR as well as the total power level.

144 KHZ DATA CLOCK OUT. This port combined with DATA CLOCK IN below, is a cabled connection between a 144 kHz crystal oscillator outputting a TTL level signal, and a PN code generator which generates a sequence of 1's and 0's to simulate data. The internal oscillator can be used to clock the data generator, or an external TTL signal can be inputted. The frequency of the data train is one-half of the clock frequency; e.g., the 144 kHz clock generates 72 kbps data. Because the data clock is phase-shifted and then used to reconstruct the demodulated data returned by the despreader, and since the phase-shifting is accomplished by a fixed delay one-shot, the bit reconstruct of the test set will not function properly without internal adjustments when an external data clock is used. During BPSK operation, a 432 kHz crystal oscillator is switched in place of the 144 kHz XO and necessary phase-shifter changes are made. This is accomplished by the mode selector switch on the back panel.

144 KHZ DATA CLOCK IN. See DATA CLOCK OUT above.

6 MHZ DATA CLOCK OUT. The two 6 MHZ DATA CLOCK ports perform functions parallel to those given above the 144 kHz XO. The data output from the PN generator clocked by this signal, however, modulates the carrier in quadrature to the phase of the lower frequency data. Also this channel of data-modulated carrier contains 80 percent of the total signal power. Like the lower data clock, the internal 6 MHz clock can be disconnected and an external TTL signal at twice the desired data rate can be substituted, forefeiting the bit reconstruct and error count capabilities of the test set. During BPSK mode operation the data produced by this channel is not used.

6 MHZ DATA CLOCK IN. See DATA CLOCK OUT above.

DATA CLOCK RESET. This is a momentary contact switch which initializes the two data generators. When depressed, the switch sets the data generator outputs in predetermined states, providing a dc signal to both the I-and Q-channels of the modulator. There are two primary uses of the switch: 1) switching the data modulation on an off to observe spectrum changes; and 2) restarting the data generators in the event they lock in the forbidden state (all.1's) due to an improper clock signal.

SPREADING SIGNAL PN OUT. This port, together with PN IN provides a cabled connection in the code path through the PN generator which provides the spread spectrum modulation signal.

SPREADING SIGNAL PN IN. See PN OUT.

SPREADING SIGNAL $\overline{PN}$ OUT. This port and PN IN provide complimentary signals to PN OUT and PIN IN. Complimentary signals driving the mixers exhibit nearly 3 dB improvement over single-sided drivers.

SPREADING SIGNAL $\overline{PN}$ IN. See $\overline{PN}$ OUT.

SPREADING SIGNAL RESET. This momentary contact switch ini-
tializes the spread spectrum PN generator. It has the func-
tions of removing modulation for observing spectral changes
and restarting the code in the event of improper clocking.

72 KBPS REF DATA OUT. The triad of REF DATA BNC ports enables
one of the requisites for successful demodulation and error
counting. The two outputs provide replicas of the internally
generated data without Manchester coding. One data stream is
selected (by cabling to the input port) to be used for bit-by-
bit comparison and detection of errors. It is also possible
to use a TEE connector and an oscilloscope to view the
reference data for comparison with the reconstructed data
train. This port provides 216 kbps data when the mode
selector switch on the rear panel is set for BPSK.

3 MBPS REF DATA OUT. Provides 3 Mbps data as above.

REF DATA IN. Input connection for any selected data rate.

REF DATA SWITCH. This is a DPDT switch performing the
primary function of establishing the proper integration time
constant needed in the bit reconstruct circuits for reshaping
data. The "up" position selects either 72 kbps or 216 kbps.
The "down" position selects 3 Mbps. The output of the REF
DATA SYNC is also selected by this switch.

REF DATA SYNC. Because the data streams are PN codes, a
signal is necessary for trigerring an oscilloscope to
observe the data. The sync signal is selected by the REF
DATA SWITCH above.

72 KHZ REF CLOCK OUT. The triad of REF CLOCK ports permits
selection of another signal required for demodulation and
error counting. The two outputs are clocks that have been
phase-shifted to synchronize with the data returned from
the despreader. Either 72 or 216 kHz is provided at the 72
kHz output.

3 MHZ REF CLOCK OUT. See above.

REF CLOCK IN. See above.

DATA Selector Switch. This switch enables using the DATA output for the dual functions of observing a buffered version of the DETECTED DATA or the RECONSTRUCTED DATA. The DETECTED DATA is taken from the last mixer before the bit reconstruct circuits (see Figure 2-17). The RECONSTRUCTED DATA is a reclocked output of an integrate-and-dump circuit. Either data output must be observed using the sync signal in the REF DATA box. Only one data rate is available at a time, chosen by the four selections mentioned previously:

1) Carrier phase adjustment

2) REF DATA cabling

3) REF DATA selector switch position

4) REF CLOCK cabling.

DATA Output. See above.

MODULATOR PN CLOCK Input. As the internal spread spectrum PN code generator has no clock, TTL levels at the desired frequency must be supplied. The PN code rate will be the same as the input clock frequency; e.g., 14.1 MHz produces a 14.1 Mcps code.

MODULATOR LO Input. The LO input provides the carrier for the simulated spread spectrum signal. A 110 MHz +3 dBm signal is required, which may be taken from the rear panel.

MODULATOR RF OUT. This port makes the Manchester-coded data modulated spread spectrum carrier available before any filtering or introduction of noise. Whenever the test set is used to provide the despreader input, this signal must be fed back into the CHANNEL RF IN port.

DEMODULATOR RF IN. This port accepts the despread signal from the despreader and passes it to the bit reconstruct and error detection circuits of the test set.

DEMODULATOR BIT ERRORS Output. A TTL level pulse is provided
at this port whenever a discrepancy is detected between the
reconstructed data and reference data. The data channel to
which this applies is determined by the REF DATA and REF
CLOCK connections.

2.3.2 Test Set Rear Panel (See Figure 2-18)

110 MHZ. An internal crystal oscillator provides a +3 dBm
signal which is suitable for use as the MODULATOR LO when
no Doppler is to be simulated.

NOISE OUT. Internal amplifiers filtered to a 50 MHz band-
width at 110 MHz provide noise at a power level determined by
the NOISE LEVEL attenuator, located on the rear panel also.
This signal is suitable for the CHANNEL NOISE input needed on
the front panel.

Mode Selector Switch. As indicated by the labelled positions,
this switch provides for some of the circuit changes needed in
switching between the UQPSK and BPSK modes. The toggle switch
controls FET switches which alter the bit reconstruct integra-
tion time constant and threshold level, and change the data
clock oscillator and phase-shifter.

NOISE LEVEL Attenuator. This control provides a 65 dB range in
noise density available at the NOISE OUT port.

2.3.3 Despreader Front Panel (See Figure 2-19)

AC Power Switch. Illuminated push-type alternating action power
switch which supplies ac power to an internal 28 Vdc supply.
The despreader can either be operated on 117 Vac or external 28
Vdc. Half the switch is illuminated by ac power operating the
28 volt supply and the other half is lit by 28 Vdc operating
other internal supplies, so the switch is always at least
partly illuminated if the despreader is in operation.

28 VDC OUT. A banana jack which provides +28 volt dc power to
be returned to 28 Vdc IN for despreader operation from 117 Vac
power.

28 VDC IN. See above.

2-30
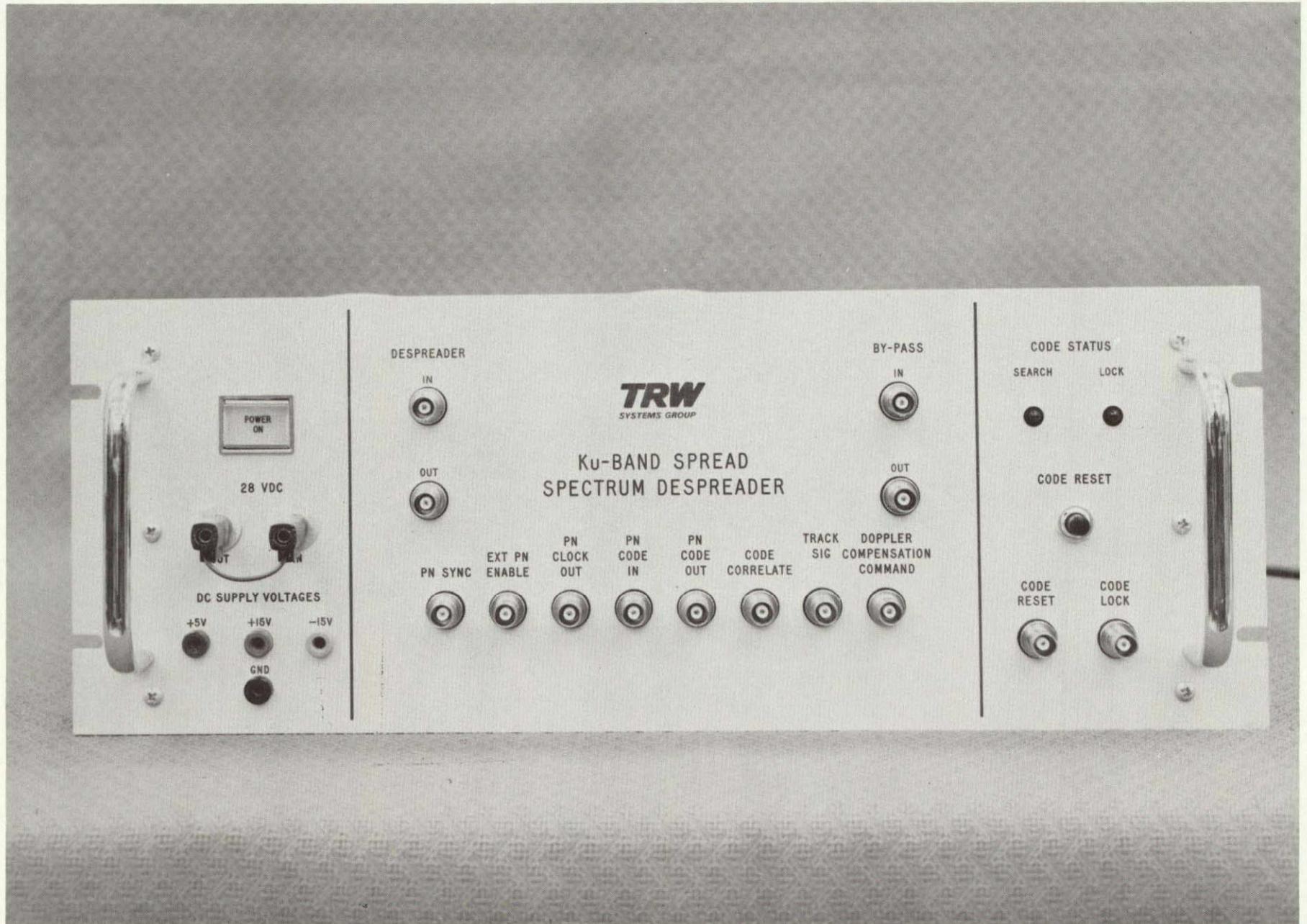
Figure 2-19. Despreader Front Panel

DC SUPPLY VOLTAGES. Test points for +5, +15, -15 volts, and a ground terminal (all as marked on panel). The test points are current-limited.

DESPREADER IN. This port accepts the proper spread spectrum signal for processing by the despreader. The signal is cabled directly to the RF PC board.

DESPREADER OUT. The despread output signal is coupled off the punctual channel of the RF PC board and cabled to this panel connection.

BY-PASS IN. The despreader has two ports for use in a "by-pass" mode, where no despreading is required. The by-pass circuit is simply a 7 dB coupler and coax cable simulating the phase shift and attenuation characteristics of the despreader analog circuits.

BY-PASS OUT. See above.

CODE STATUS SEARCH Light. This is an LED indicator light directly driven by a TTL gate. The light is turned on whenever acquisition threshold is not exceeded.

CODE STATUS LOCK Light. This is an LED indicator light directly driven by another TTL gate. The light is turned on whenever acquisition threshold is exceeded. This includes true correlation and false alarms.

CODE RESET Switch. This is a pushbutton switch which initializes the PN code generated in the despreader by clearing the shift register. The code acquisition circuits (counters, flip-flops, etc.) are also initialized when the button is depressed.

CODE RESET Connector. A TTL "0" at this port performs the same function as depressing the RESET button. The connection is provided to facilitate automatic testing for acquisition time measurements.

CODE LOCK Connector. A tri-level signal is available at this port as an indicator of code status. A low-pass filter on this output helps eliminate false alarm signals, but adds time delay. Search is indicated by a positive voltage (4 volts), reset produces a zero output, and a negative voltage (-8 volts) indicates lock.

PN SYNC. A sync pulse for viewing the despreader PN code is available at this port.

EXT PN ENABLE. The despreader can accept an external PN code at the PN CODE IN port to be used in place of the code generated internally. Grounding this input enables an external code. A TTL "1" or an open circuit enables the internal code.

PN CLOCK OUT. The code clock frequency (VCXO divided-by-four) can be monitored at this port. A 10 or 20 dB pad is desirable for reducing reflections, harmonics, etc.

PN CODE IN. An external PN code having TTL levels can be input at this port. The ENABLE connector must be grounded for this function.

PN CODE OUT. The internal code can be monitored at this connection.

CODE CORRELATE. An analog signal (buffered from the acquisition channels) is available to monitor the output of the two acquisition channels. The greater the correlation is, the more negative this signal becomes.

TRACK SIG. The control signal to the VCXO can be monitored at this port.

DOPPLER COMPENSATION COMMAND. A TTL level signal at this connector indicates which of the two Doppler regions is being searched during UQPSK acquisition. The signal is still present, but has no effect during BPSK operation.

2.3.4 Despreader Rear Panel (See Figure 2-20)

DUMP CMD. The signal which drives the FET switch of the acquisition integrate and dump circuit can be monitored at this jack. The integrator is grounded when this signal is TTL "0."

Dwell Mode Selector Switch. This toggle switch selects between two available signals suitable for dumping the integrator. One is a synchronous fixed-period signal derived from the VCXO frequency. The other is an asynchronous variable-period signal generated by an astable multivibrator. Both have 11 μsec dump times. The synchronous integration time is 361 μsec; the asynchronous integration time can be set between roughly 40 μsec and 1 msec.

DWELL PERIOD. This control is used to set the integration time for the acquisition integrate-and-dump asynchronous variable dwell mode.

Mode Selector Switch. This toggle switch sets the proper channel gains, thresholds, and loop parameters for either 72 kbps/3 Mbps UQPSK or 216 kbps BPSK operation.

Bandpass Filters. The 1.5 MHz bandpass filters for BPSK operation are permanently mounted on the despreader rear panel. The tan-colored cables run inside to the RF PC board where connections are switched for the two modes.

2.4 ESTABLISHING C/N_0

It is of obvious importance to correctly set up carrier-to-noise density ratios (C/N_0) in measuring despreader and by-pass performance. This normally entails a lengthy process of precise measurements, but has been tremendously simplified by the inclusion of an internal 30 MHz bandpass filter within the test set. In the procedure outlined here the 3 dB bandwidth of a 5-pole tubular bandpass filter is used for the noise bandwidth.
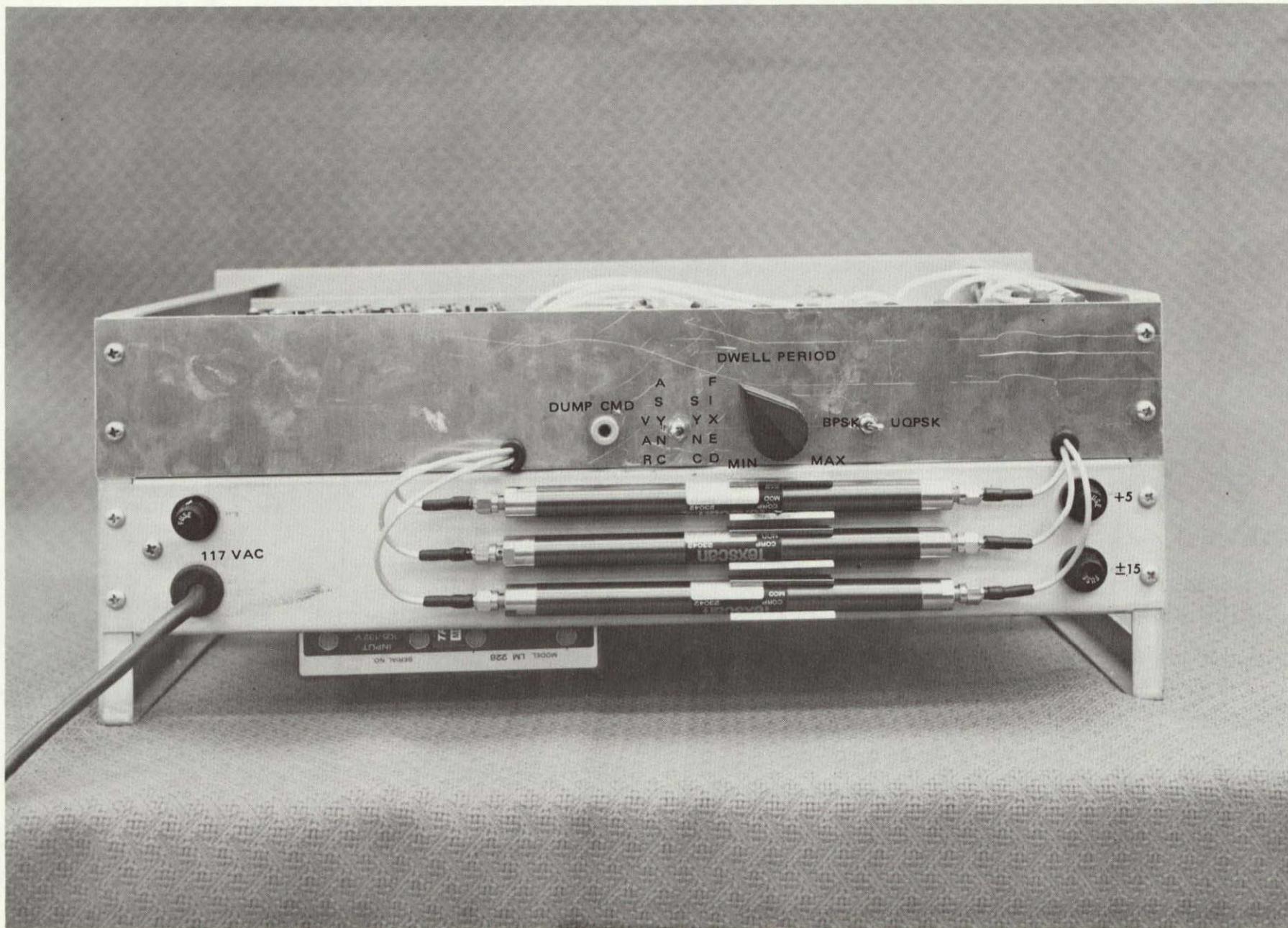
Figure 2-20. Despreader Rear Panel

The filter establishes the bandwidth (30 MHz or 75 dB) in which both noise and signal energy are measured. This determines the relationship that

$$C/N_o \text{ (dB)} = \text{SNR (dB)} + 75 \text{ dB}$$

Passing the spread spectrum signal through a 30 MHz filter introduces some loss of signal energy. Any real transmitter, however, would need to have some output bandwidth — probably very close to 30 MHz. Also, the energy of the PN spectrum attenuated by the filter is so small as to cause only about 0.1 dB extra loss.

The procedure for setting exact SNRs (C/N_o values) is simplified by some preliminary calculations. Since the total power — signal plus noise is to be -15 dBm, exact power levels for the signal and noise measured separately can be found for any SNR. Table 2-1 shows a list of these numbers.

With the noise being added to the signal reduced to a negligible value (i.e., either terminate NOISE port or add 50 dB or more attenuation), the MANUAL AGC control can be adjusted to set the signal power at CHANNEL RF OUT to the desired value. Then with the CHANNEL RF IN port terminated (so that no signal energy is present), the level of noise power being introduced at the CHANNEL NOISE input can be adjusted to obtain the proper power measurement at RF OUT without changing the MANUAL AGC setting.

When the signal is again injected, the total power measured at CHANNEL RF OUT should be quite near the -15 dBm desired for despreader operation. The SNR is already established, and so the MANUAL AGC control can be varied to exactly set the total power level at -15 dBm, or any other level desired. Since both signal and noise pass through the MANUAL AGC attenuator, changes in its setting have no effect on SNR.

It is convenient to set up one exact SNR ratio and then, by means of a step attenuator on the input to CHANNEL NOISE, vary the SNR by simply changing the noise attenuator and then resetting the total power. This method is nearly exact if the signal and power levels are several dB different. The small variations occurring, however, with such a method

can be acceptable in situations where it is only necessary to reproduce the same SNR without necessarily knowing precisely the true SNR value. This procedure is helpful for rough measurements, but is not recommended for any other uses.

Table 2-1. Power Levels for Various SNRs with -15 dBm Total Power

C/N_0	SNR	P_S (dBm)	P_N (dBm)
60	-15	-30.1352	-15.1352
61	-14	-29.1695	-15.1695
62	-13	-28.2124	-15.2124
63	-12	-27.2657	-15.2657
64	-11	-26.3320	-15.3320
65	-10	-25.4139	-15.4139
66	-9	-24.5150	-15.5150
67	-8	-23.6389	-15.6389
68	-7	-22.7901	-15.7901
69	-6	-21.9732	-15.9732
70	-5	-21.1933	-16.1933
71	-4	-20.4554	-16.4554
72	-3	-19.7643	-16.7643
73	-2	-19.1244	-17.1244
74	-1	-18.5390	-17.5390
75	0	-18.0103	-18.0103
76	1	-17.5390	-18.5390
77	2	-17.1244	-19.1244
78	3	-16.7643	-19.7643
79	4	-16.4554	-20.4554
80	5	-16.1933	-21.1933
81	6	-15.9732	-21.9732
82	7	-15.7901	-22.7901
83	8	-15.6389	-23.6389
84	9	-15.5150	-24.5150
85	10	-15.4139	-25.4139

2.5 BIT ERROR RATE (BER) MEASUREMENTS

The best single measurement of the quality of the despreader's perfor-
mance is bit error rate degradation. The test set itself, with its modula-
tor and demodulator sections has a characteristic bit error rate indicative
primarily of bit reconstruct performance. The extra degradation introduced
by the despreader can simply be measured by counting the excess errors for
a given SNR (or C/N_0) when the despreader is in the circuit.

The bit reconstruct and error indicating circuits of the test set are
discussed in detail elsewhere. Typical waveforms for strong signal demodu-
lation are presented in Figures 2-21 and 2-22. The photographs show DETECTED
DATA and RECONSTRUCTED DATA outputs in comparison with the REF DATA output
for the two data rates of the UQPSK system. The parallels are obvious.
(Under close inspection the pictures also show a one-chip time lag from REF
DATA to either of the received data waveforms. This is a characteristic of
the test set, occurring because bit reconstruct decisions are made at the
end of a one-chip integration period. (This does not affect the error mea-
surements.)

The same three waveforms — REF DATA, DETECTED DATA, and RECONSTRUCTED
DATA — are shown for the 216 kbps data rate, but at minimum signal-to-noise
(60 dB-Hz). Figure 2-23a shows a sequence of bits which were recovered
without any errors. Figure 2-23b shows the same sequence of bits (a repe-
tition of the data PN word) at a later time when an error did occur. Such
errors are caused by the random fluctuations of noise interfering with and
obscuring the true signal.

Where such errors occur a pulse is produced at the BIT ERRORS output
of the test set. Such pulses can be totalized by a counter when making
error measurements. Since the data is being transmitted at a high rate
(many thousands of bps) it is usually accurate to speak of an error rate
or frequency. Although the errors occur randomly, a time frame can be used
in which a statistically large number of errors exist. In the next time
interval of the same length, approximately the same number of errors should
occur unless the original measurement was too small.

.1V/div

5V/div
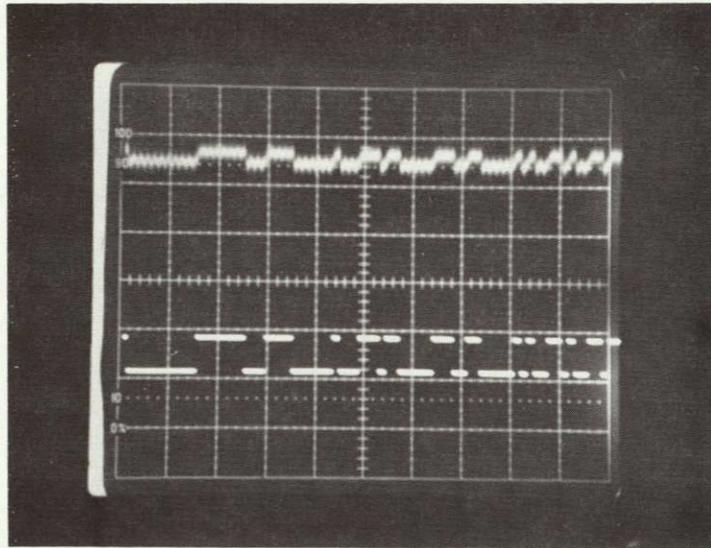
a.
DETECTED
DATA

REF DATA

5 V/div

5V/div
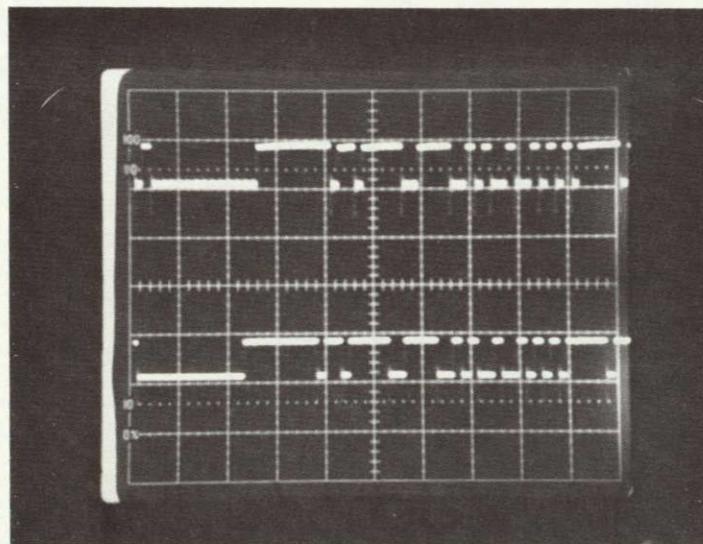
b.
RECONSTRUCTED
DATA

REF DATA

Figure 2-21. 72 kbps Data

.1V/div — a. DETECTED DATA

5V/div — REF DATA

5V/div — b. RECONSTRUCTED DATA

5V/div — REF DATA

Figure 2-22. 3 Mbps Data

REF DATA

a.
3V/div

DETECTED
DATA

0.2V/div

RECONSTRUCTED
DATA

3V/div

REF DATA

b.
3V/div

DETECTED
DATA

0.2V/div

RECONSTRUCTED
DATA

3V/div
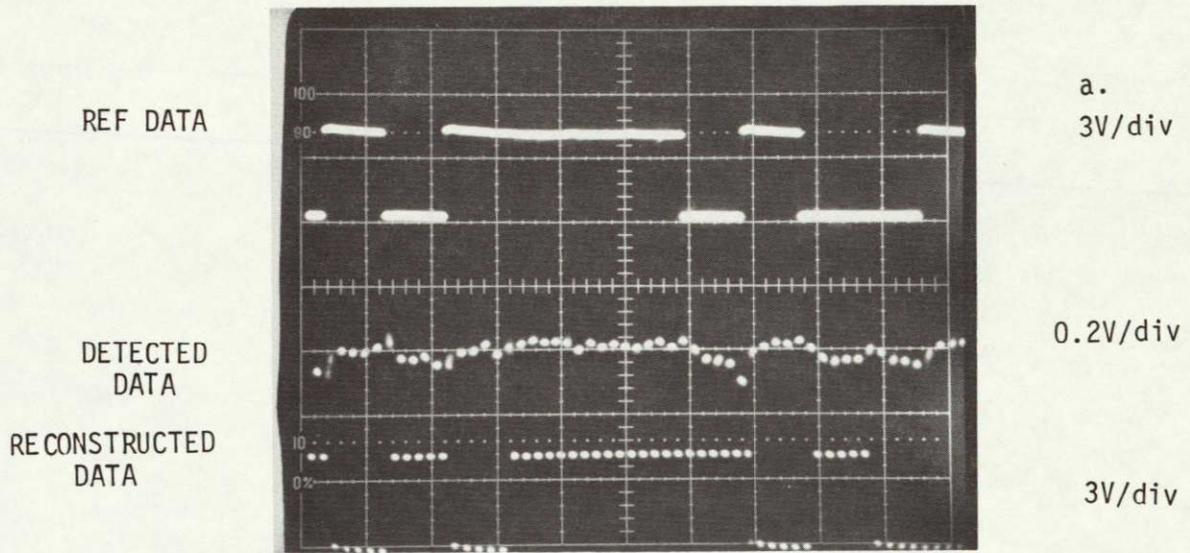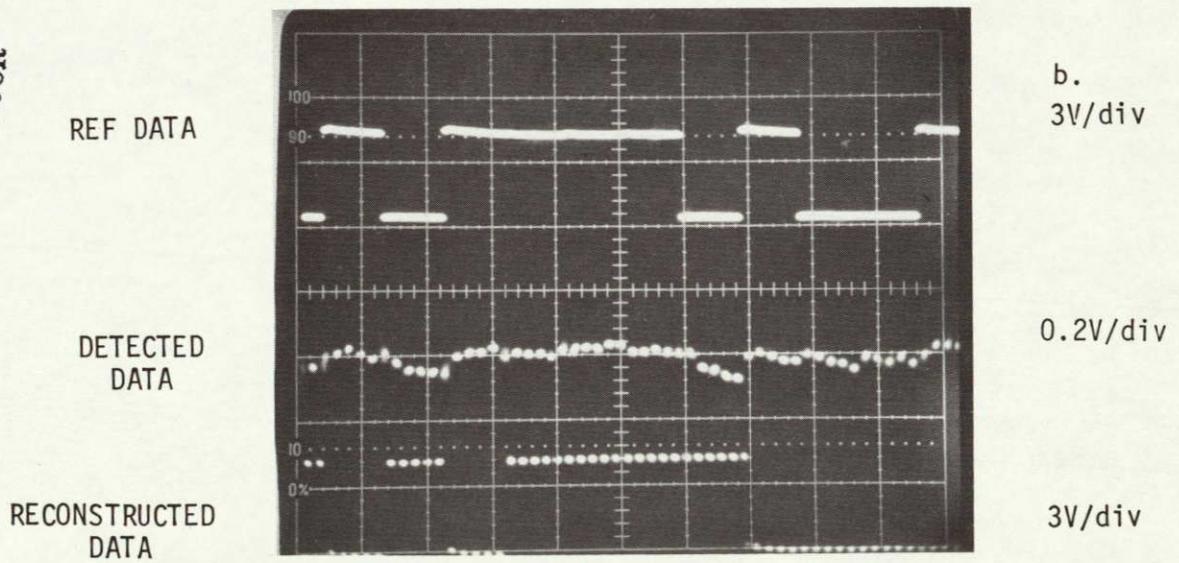
Figure 2-23.   216 kbps Data

2-41

It is precisely this problem which makes the 72 kbps BER measurements difficult. The 72 kbps channel has a sufficiently high E_b/N_0 to recover data at a BER on the order of 10^{-4} or better, even at minimum SNR. This means that the time interval mentioned above should be at least several minutes long to obtain a sufficient sample size. Figure 2-24 shows graphed error rate data for 10-second samples. In the 72 kbps case, this sample size is very likely not large enough.

Another interesting set of measurements is shown in Figure 2-25. Measured error rates versus SNR are plotted for the 216 kbps BPSK mode as a function of Doppler. In an ideal system the effect of the Doppler would probably not be seen in these graphs. A slight offset, however, in the X-Y multiplier could produce such an effect: while at 0 Doppler the offset could cause tracking at a slight phase error; one Doppler polarity would increase the tracking error, and the other would make it decrease.

The conversion from error rate to BER is easily made, and Figure 2-26 plots BER versus SNR. The graph displays by-pass and despread measurements made for the 216 kbps data rate, as well as a curve showing best character-istics theoretically possible.

Several months' experience in operating the despreader and test set has yielded helpful guidelines for making BER measurements. BER has proven to be the single most accurate indicator of despreader performance. Also, in that both by-pass and despreader measurements are usually made, BER can often demonstrate the current performance of the test set.

The single most important factor in making these measurements is cor-rect phasing of the signals hard-lined through the test set from the MODULATOR to the DEMODULATOR. The data clocks (REF CLOCK) have variable phase-shifters which can be adjusted by changing potentiometers on the data generator boards. However, these have been carefully set and normally need not be changed.

The carrier phase shifter, however, must be changed in order to demod-ulate either the I- or Q-channel of the UQPSK mode separately. This is the CARRIER PHASE control on the test set front panel, and it is perhaps the most difficult adjustment to make for any of the tests.
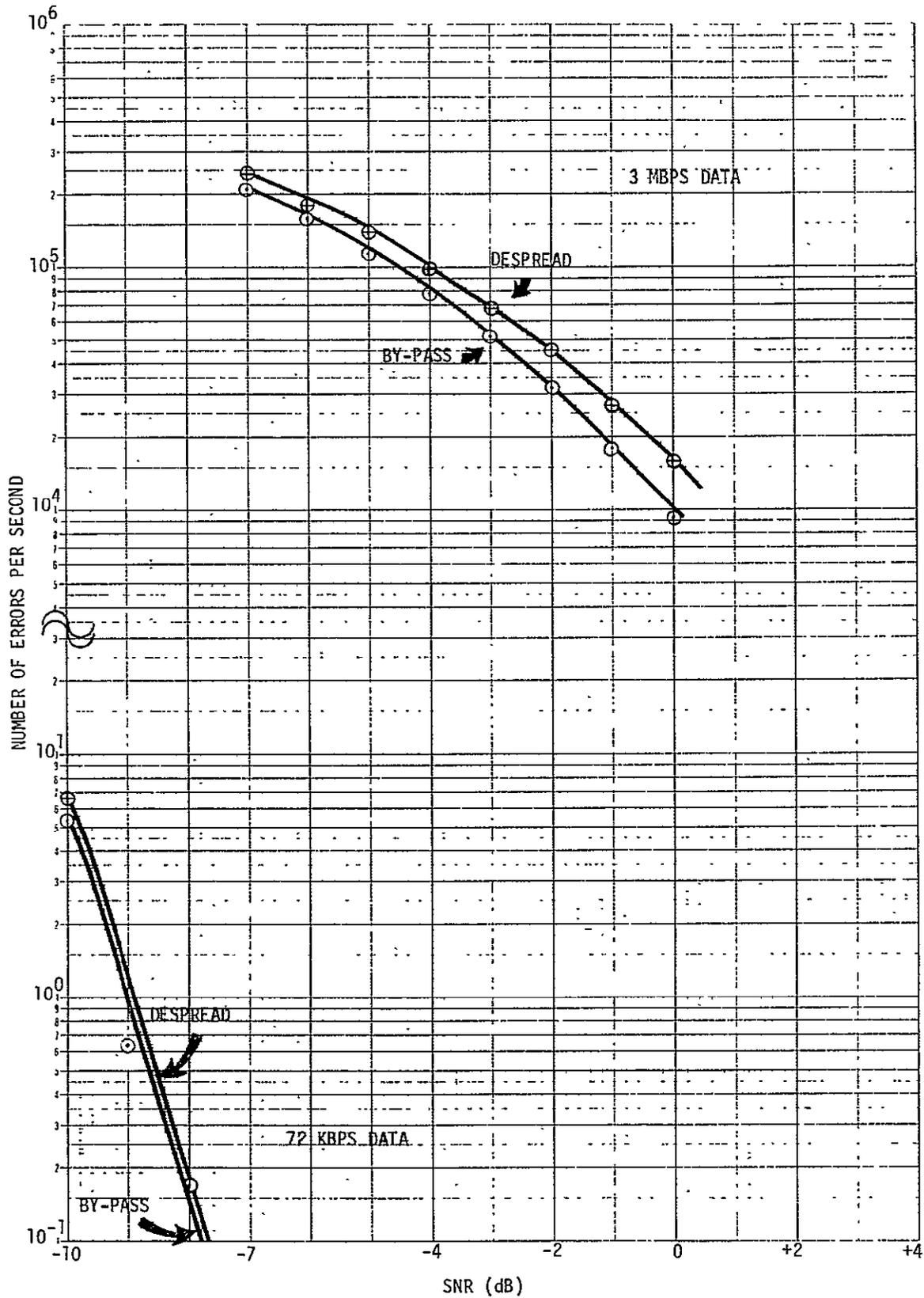
Figure 2-24. UQPSK Data
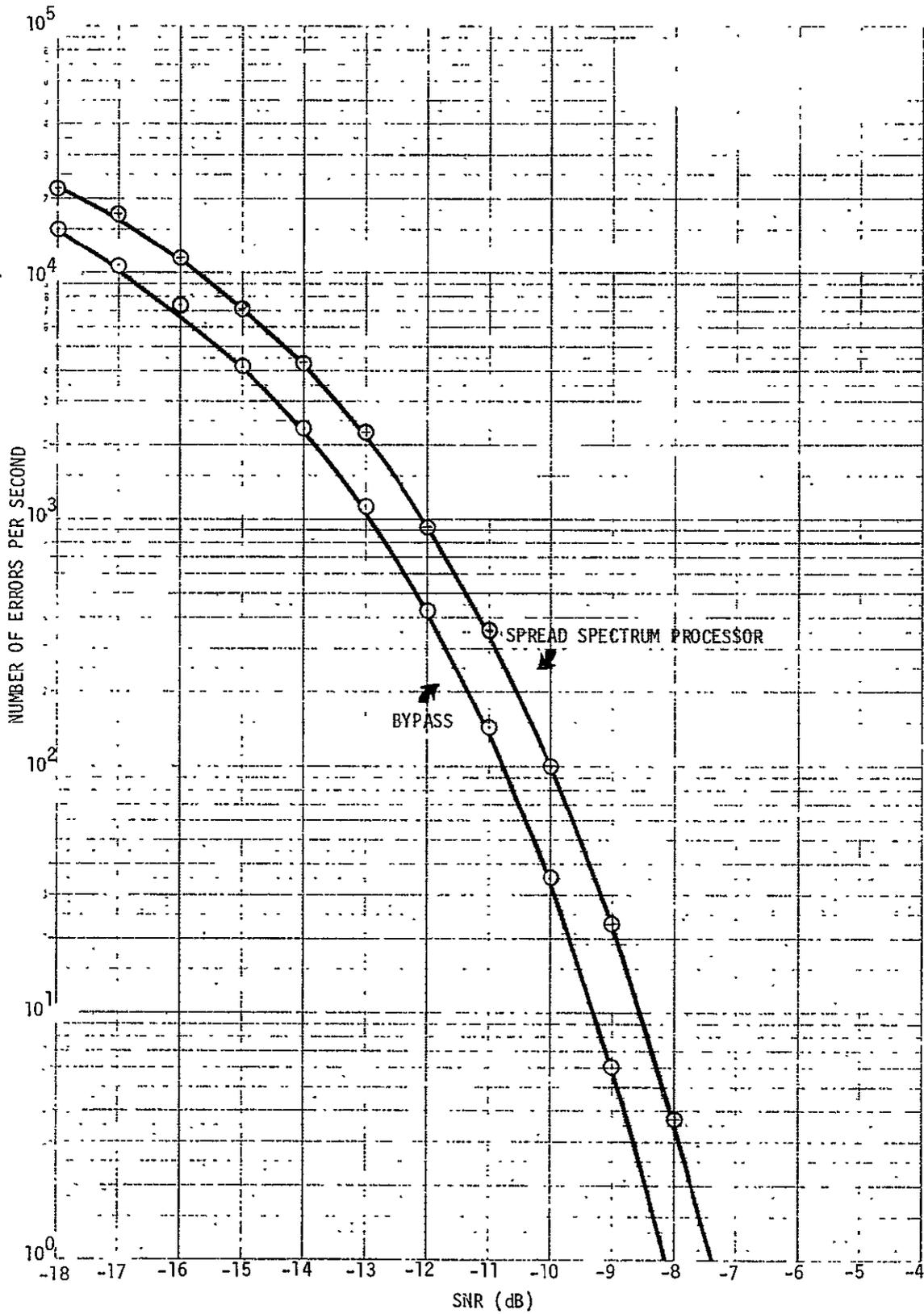
Figure 2-25a. Error Rate Versus SNR at Maximum Negative Doppler Ku-Band Spread Spectrum Processor Breadboard (216 kbps)
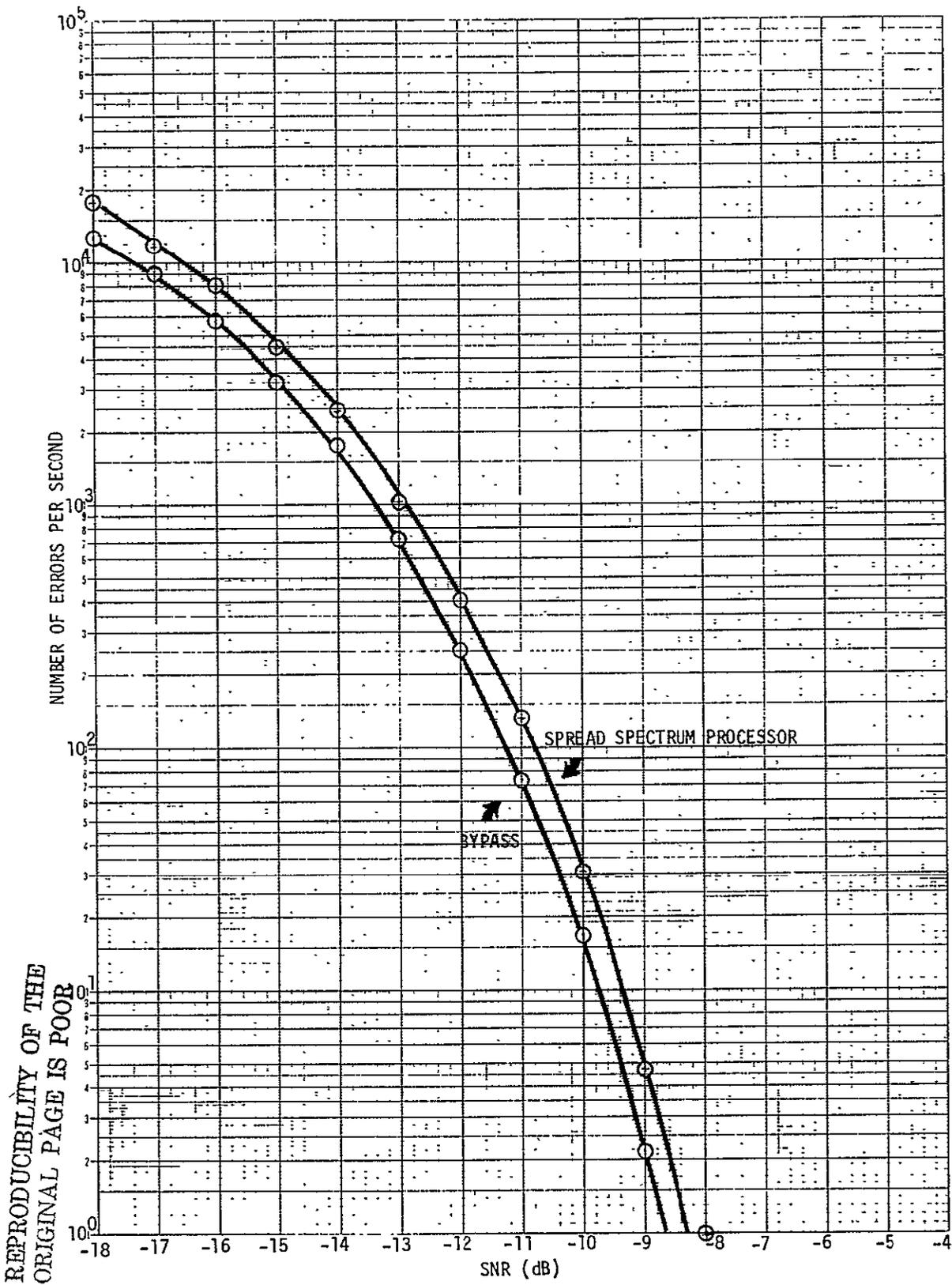
Figure 2-25b. Error Rate Versus SNR at 0 Doppler
Ku-Band Spread Spectrum Processor
Breadboard (216 kbps)
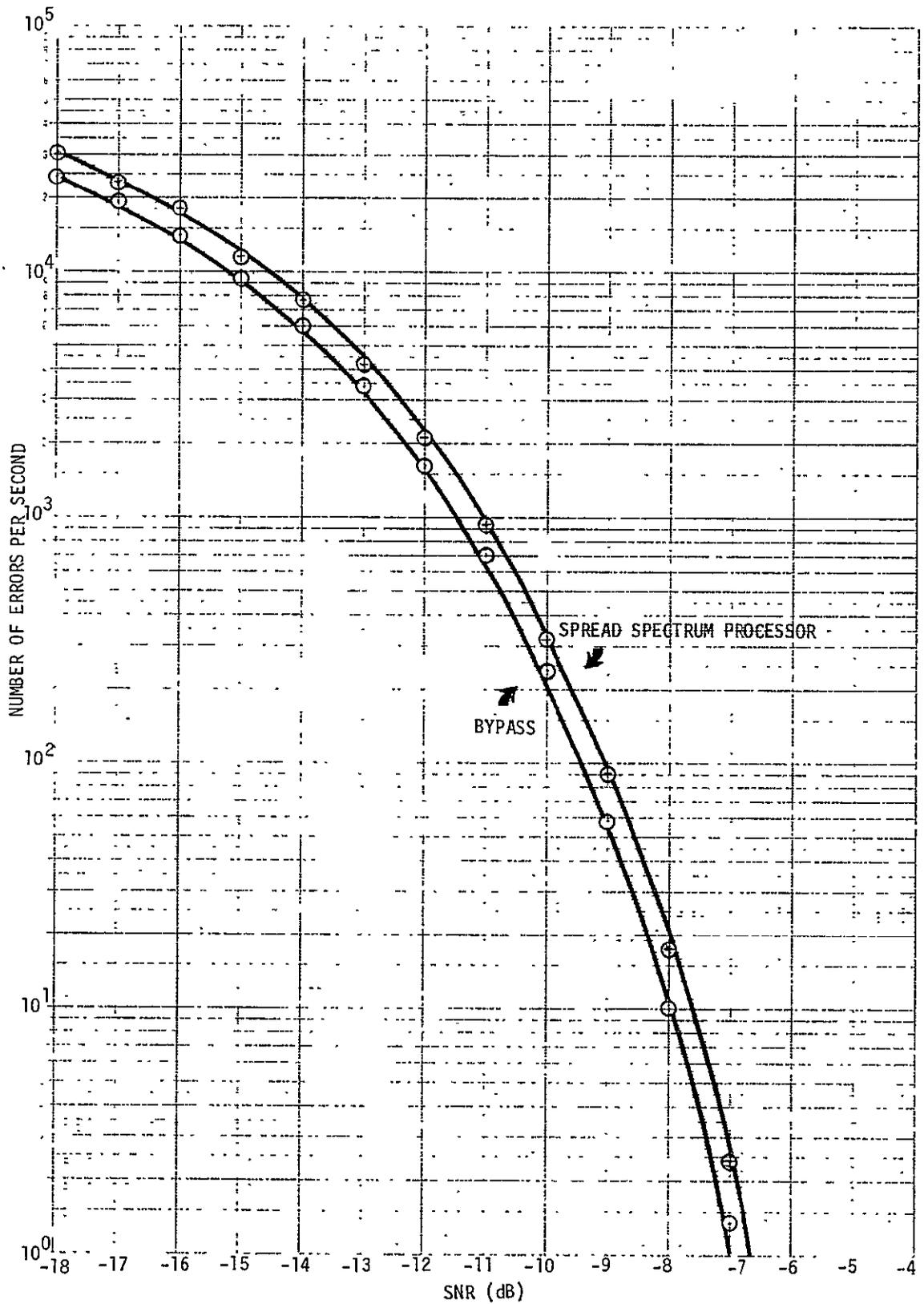
Figure 2-25c. Error Rate Versus SNR at Maximum Positive Doppler
Ku-Band Spread Spectrum Processor Breadboard
(216 kbps)

2-46
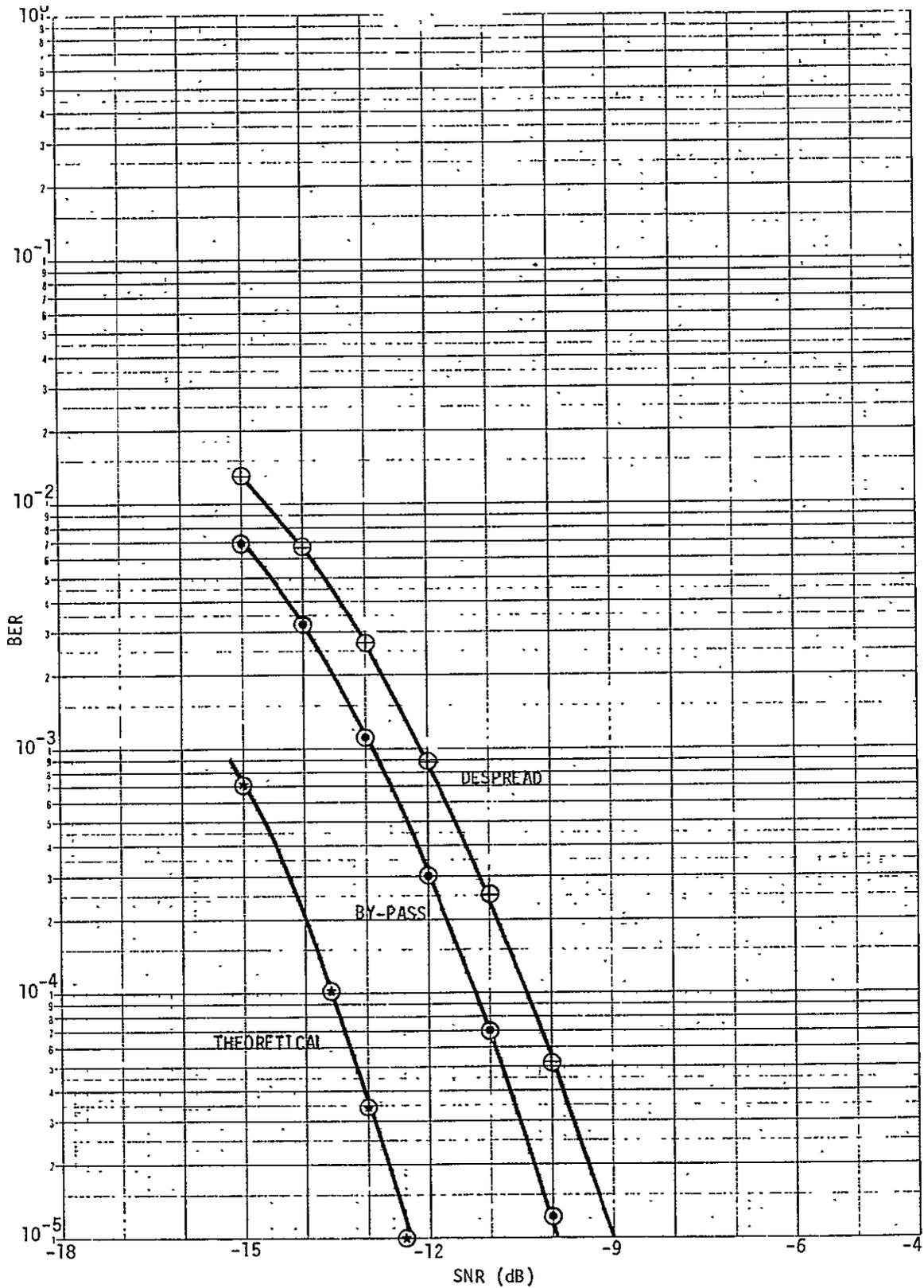
Figure 2-26. BPSK Mode BER

2-47

One source of the difficulty is that the phase shifter does not have a linear phase characteristic. Additionally, the combination of the dial setting and the switch position can create several "nulls" of unequal depth. It is necessary to select the best combination for repeatable measurements.

Another possible stumbling block is caused by inherent 180 degrees ambiguities and possible phase-reversals of both the test set and despreader. The most common result of this effect is counting the error compliment instead of the number of errors. The RESET buttons for both data and PN code generators can be used to correct this difficulty.

2.6 ACQUISITION TIME MEASUREMENTS

Acquisition time is by definitioning the period from the despreader begins searching for the code (either from turn-on or loss-of-lock) to the time when the code phases are locked. This measurement is again statitical in nature. Without prior information, the initial code phases can be, at most, one PN word apart-or any value lower. Therefore a random distribution of times is expected out to one word-scan time; and then, if P_D were exactly 1 and P_{FA} exactly 0, there would be no other values. That is, under those conditions and 0 Doppler the despreader would always lock after no more than 8188 (2^{11} -1 times 4) quarter-chip steps. The analysis is complicated by the probabilities for detection and false alarm not being ideal. P_D and P_{FA} both can effect acquisition time.

Whenever P_D is less than one, there will be occasions when the despreader must scan through the PN word a second time. Additionally, whenever a false alarm occurs, some amount of time is lost in getting through the logic sequence back to quarter-chip stepping. This costs at least an extra two dwell periods for each false alarm, and possibly more — due to the VCXO being moved from its preset frequency.

The length of time required to scan through the PN word is effectively changed by Doppler. If there is a difference between the transmitted (test set) code clock and the local (despreader) code clock, the two PN codes will "slide" past each other, independent of quarter-chip stepping. Due to the direction of the stepping, the effective scan time is shortened by positive Doppler and lengthened by negative Doppler. This effect either "bunches up" or "stretches out" the distribution of acquisition times.

Histograms showing the results of thousands of acquisition time measurements, and tables summarizing the histograms are included as Appendices A and B. The two summaries are repeated here as Tables 2-2 and 2-3 for convenience.

Table 2-2. Summary of UQPSK Acquisition Tests ($\overline{T_{acq}}$ in seconds)

SNR / Doppler	-7	+3	+51
Max Negative	6.519	6.560	6.275
50% of Max	3.287	3.679	3.329
0 Doppler	2.914	2.581	2.040
50% of Max	1.316	1.711	1.445
Max Positive	1.129	1.115	1.030

	-16	-15	-14
-7 SNR 0 Doppler	2.264	2.914	2.393

Table 2-3. Summary of BPSK Acquisition Tests ($\overline{T_{acq}}$ in seconds)

SNR / Doppler	-15	-10	-2
Max Negative	4.550	2.841	3.338
0 Doppler	1.164	1.383	1.207
Max Positive	2.482	0.840	0.839

2.7 ASYNCHRONOUS VARIABLE DWELL

Due to the importance of acquisition time performance of the despreader, it is of interest to study the effects of dwell time, the interval during which a given code phase is maintained during search. The main factor of this dependence is the relationship that acquisition time is roughly the number of code phases checked multiplied by the dwell time and modified by Doppler. But other factors must also be considered. Detection probability (P_D) and false alarm probability (P_{FA}) alter with changes in dwell time, and the effects of these terms on acquisition time can become appreciable.

Although the despreader was originally designed with a fixed dwell time (derived from the single oscillator in the despreader), an asynchronous variable dwell feature was subsequently provided. A bistable multivibrator is used for this purpose. The dump time is fixed at about 11 μsec (as is used by the original synchronous circuits) in order to assure sufficient discharge time for the integrate-and-dump circuit. The other state of the multivibrator is variable from about 40 μsec to over 1 msec. The circuit for the multivibrator and interfaces with the code acquisition board are shown in Figure 2-27. (Note that the rear panel dwell mode selector switch is duplicated in this drawing for convenience.)
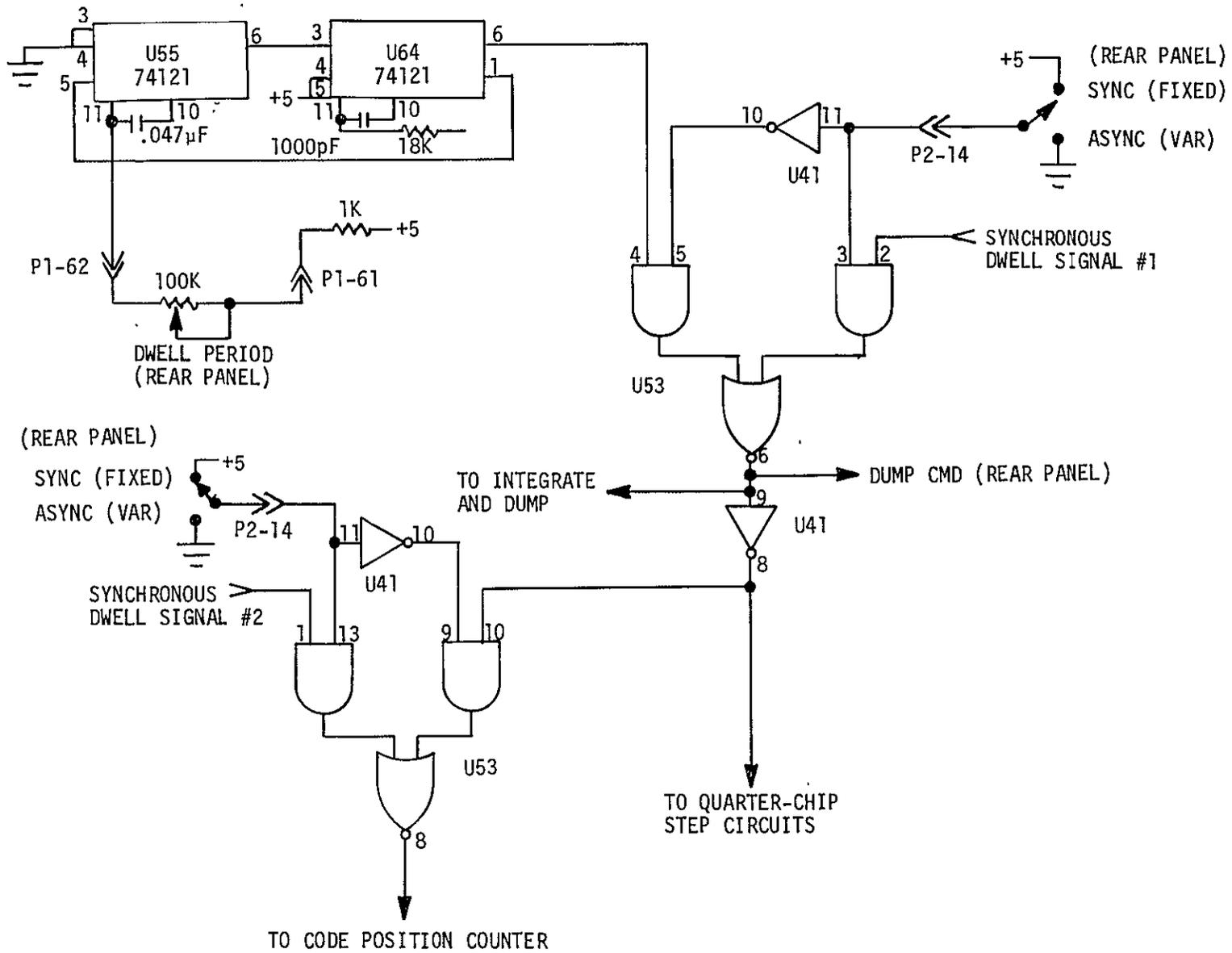
Figure 2-27. Variable Dwell Astable Multivibrator and Interfaces

3. SPECTRUM DESPREADER HARDWARE

This section contains a description of the despreader hardware, including block diagrams, schematics, circuit descriptions, layout drawings, connector interfaces, and photographs. Four divisions are made for the purposes of this section, and they are covered in detail under subsections of the following headings:

- RF PC Board

- Code Acquisition Logic Board

- PN Generator Board

- Chassis and Panels.

An introductory section first explains the despreader block diagram.

3.1 BLOCK DIAGRAM DESCRIPTION

A functional block diagram of the despreader is presented in Figure 3-1. The drawing has been greatly simplified in order to more clearly illustrate total operation of the unit.

The despreader consists primarily of three similar RF channels and supporting logic circuits. Of the three channels, two (the punctual and reference channels) are used for acquisition; the third is a tracking channel.

The incoming spread spectrum signal is divided between the three RF channels. In the punctual channel, the incoming signal is mixed with the locally generated PN code. The resultant signal is filtered to a narrow bandwidth (dependent on data rate and Doppler range) and then square law detected and low-pass filtered.

The signal in the reference channel is not mixed with the local code. This provides a totally uncorrelated reference signal which is used to effectively set threshold and eliminate AGC effects. The detectors of the two channels have opposite polarity output so that the summer actually subtracts the reference voltage. The gain adjust of the reference channel provides a means of establishing a threshold independent of SNR. The output of the summer changes polarity according to which of the inputs is larger.
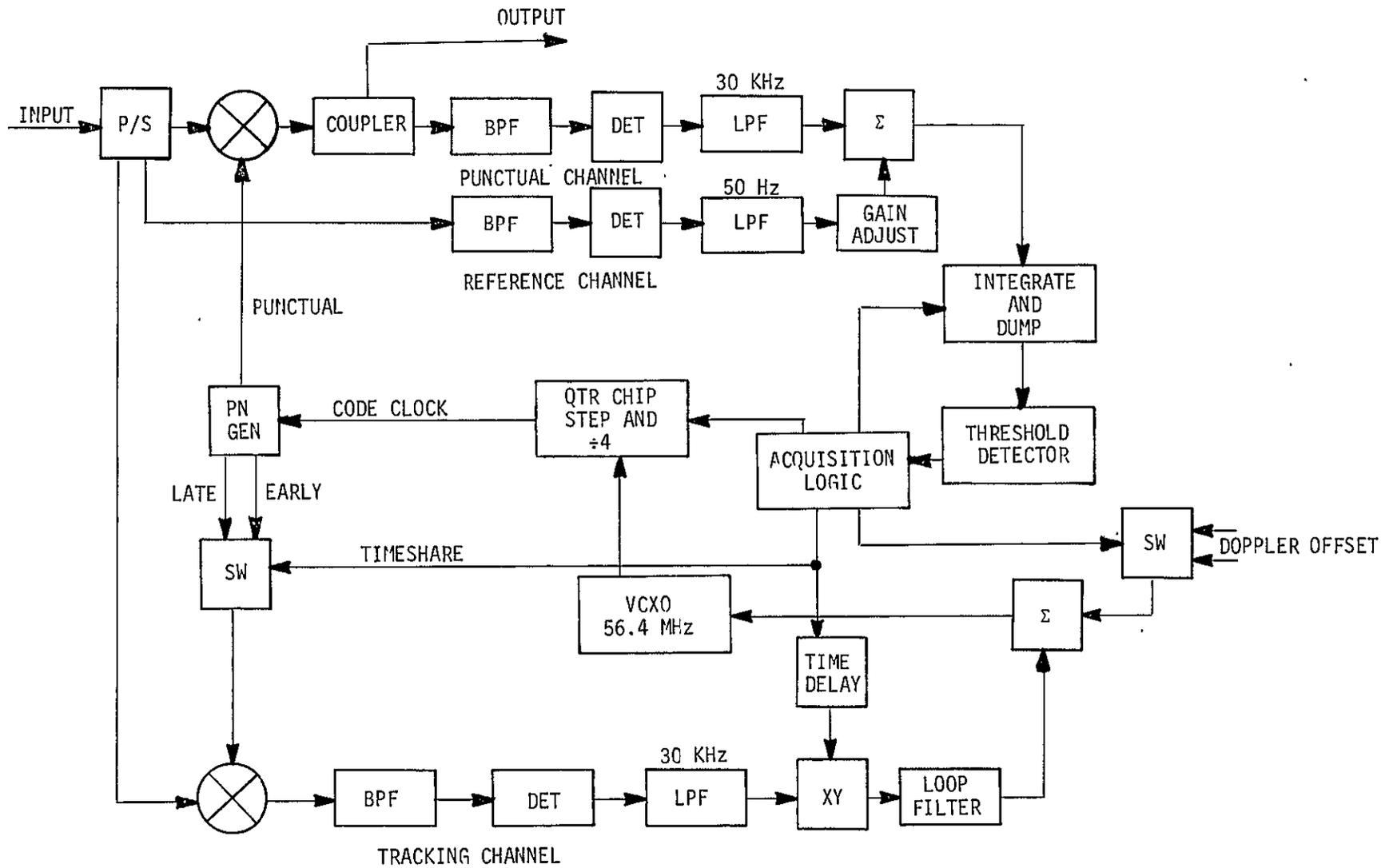
Figure 3-1. Despreader Block Diagram (Simplified)

The output of the summer is a noisy signal which is match filtered in an integrate-and-dump circuit and then threshold detected. If all components were perfect and accurate, the threshold would always be zero. In practice, it is convenient to vary the threshold as a minor adjustment for peak performance.

The acquisition logic controls the sequence of events occurring within the despreader. When code search is first started, an arbitrary local code phase is established. The despreader uses that code phase for one dwell time (selectable to either 361 μsec synchronous, or 40 μsec to 1 msec asynchronous), checks the level out of the integrate-and-dump, and delays the local code a quarter-chip if threshold was not exceeded. That procedure is reiterated until the proper code phase is found. (For the 72 kbps/3 Mbps mode a Doppler offset is used to search two frequency ranges, each requiring a full scan of the code phase.)

At some point of the acquisition cycle, the proper code phase is found (to within an eighth chip) and the tracking loop is enabled. During search mode, the loop output is grounded so it cannot pull the VCXO off the desired frequency. (Due to high dc loop gain (10^5) the open loop normally will drift to one polarity or the other, causing saturation.) With code phase acquired to within an eighth chip, the tracking curve of the detector provides the proper polarity to pull the VCXO for exact code alignment.

The tracking channel is a timeshared delay locked loop, where an independent timeshare function gates between a PN code which is either a half chip early or a half chip late with respect to the punctual channel. The same timeshare signal is then used (after proper phasing) to subtract the late response from the early response. The loop filter provides filtering to smooth the signal out and yields the proper loop response.

3.2 RF PC BOARD (DESPREADER ANALOG CIRCUITS)

The analog circuitry of the despreader is primarily located on the RF PC board. The schematic for this is given in Figure 3-2 and Figure 3-3 shows the layout.
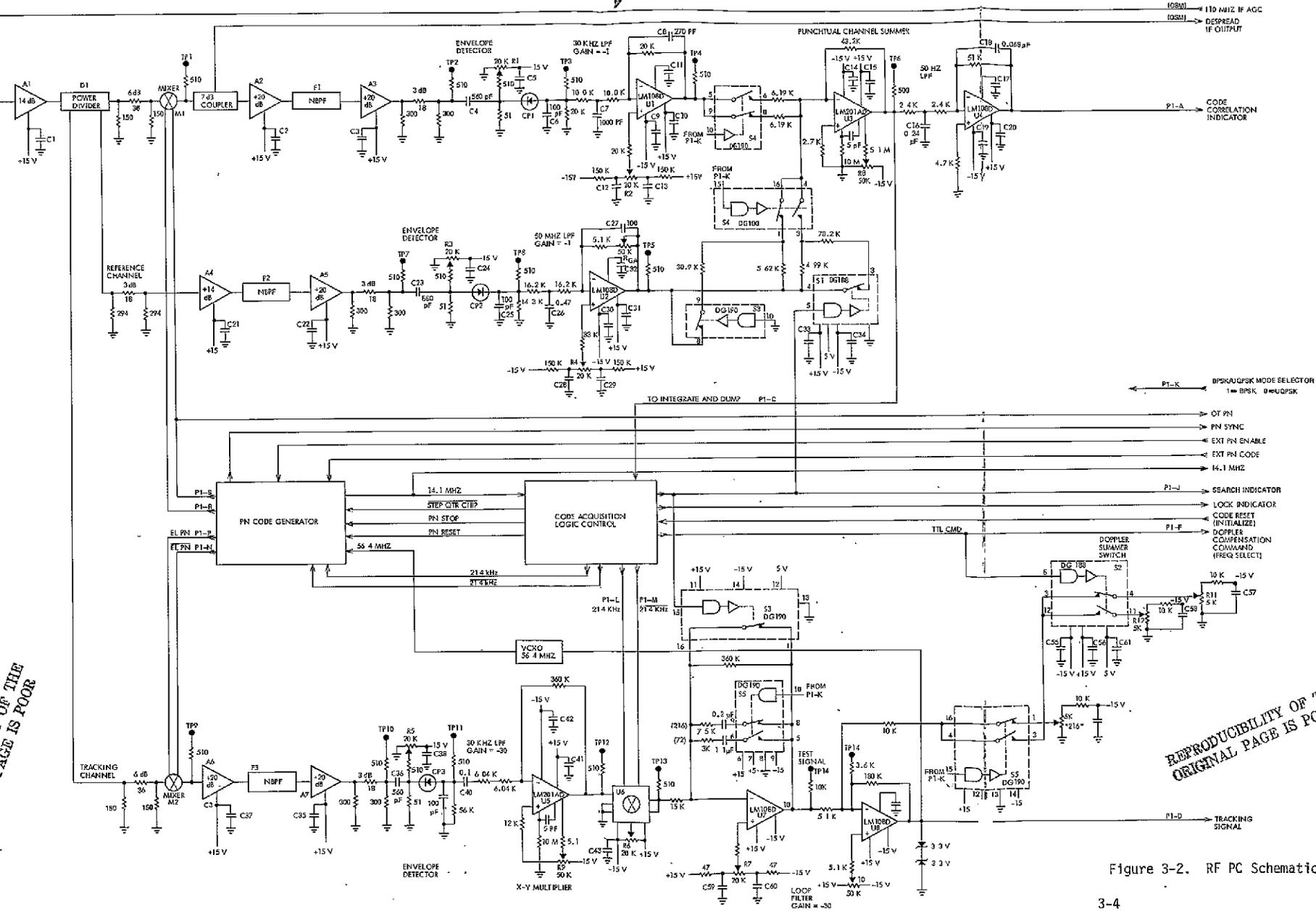
Figure 3-2. RF PC Schematic
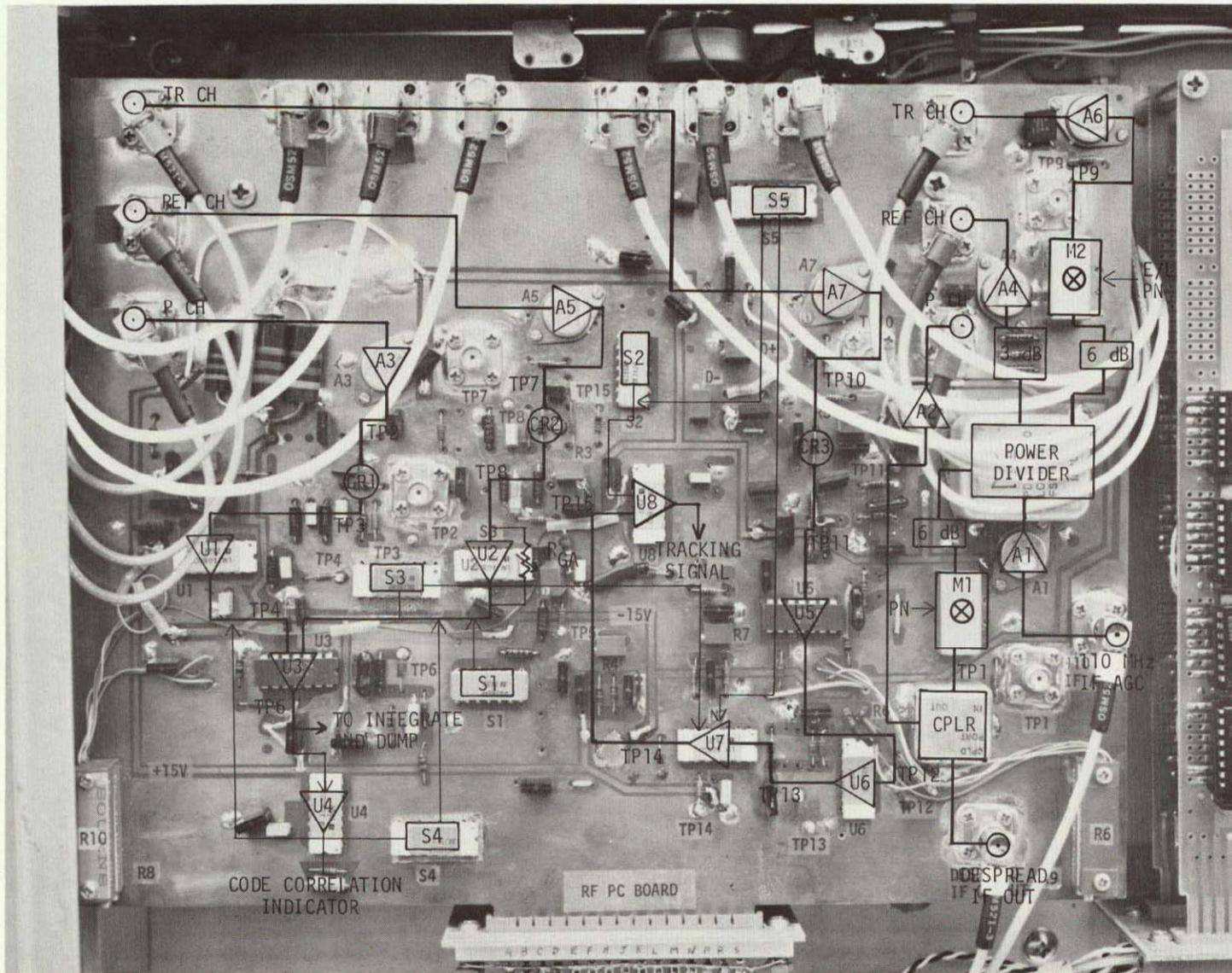
Figure 3-3. RF PC Layout

The spread spectrum signal at 110 MHz is input to the board at the lower right side via an OSM connector. The signal is then amplified 14 dB in an Avantek UTO-502, and a three-way power divider splits the signal into the three channels. The two channels having mixers (punctual and tracking channels) first have 6 dB pads to match the output impedance of the power splitter. The mixers used are the Mini-Circuits Lab SRA-3.

Included after the mixer in the punctual channel is a 7 dB coupler to split off some of the correlated signal for the output. All three channels then have amplifiers and bandpass filters. The amplifiers are either 14 dB UTO-502's or 20 dB UTO-512's.

The correlation bandwidths are selected by cabling either of two sets of filters into the circuit. One set of filters, for use with the 72 kbps/ 3 Mbps UQPSK modem, has a 3 dB bandwidth of 750 kHz. The bandwidth is determined by the SNR under maximum Doppler conditions. Since the data is Manchester-coded, the first peaks contain most of the signal energy (see Figure 3-4). Additional bandwidth must be used in order to allow for carrier Doppler and uncertainty. If the filter is too narrow then there is a tremendous change in SNR between the zero and full Doppler conditions. This is illustrated in Figures 3-4 through 3-6. The second two figures show plots of normalized SNR versus carrier Doppler for different filter bandwidths for the two modes. For example, the UQPSK mode has a maximum carrier Doppler of 225 kHz. If a 161 kHz filter were used, the post-correlation SNR would drop about 12 dB lower at maximum Doppler than for no Doppler. However, a 750 kHz filter (as used for UQPSK) maintains almost constant SNR and more importantly, provides the maximum possible SNR for maximum Doppler.

The extremely small bandwidth of these filters is a troublesome point, however. Helical resonator filters must be used to provide temperature stability, and even their performance in this respect is marginal.
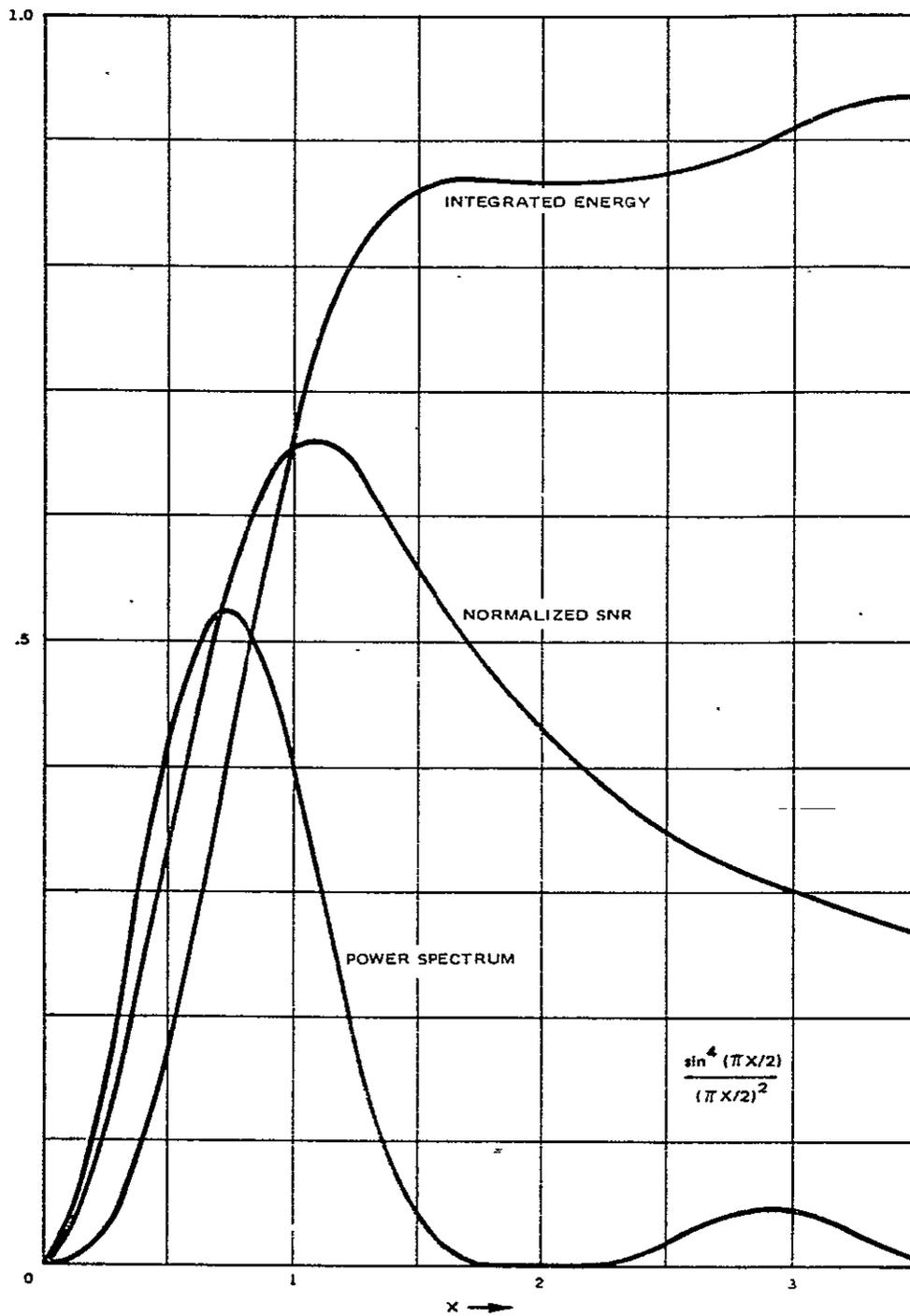
Figure 3-4.   Manchester Waveform Spectrum
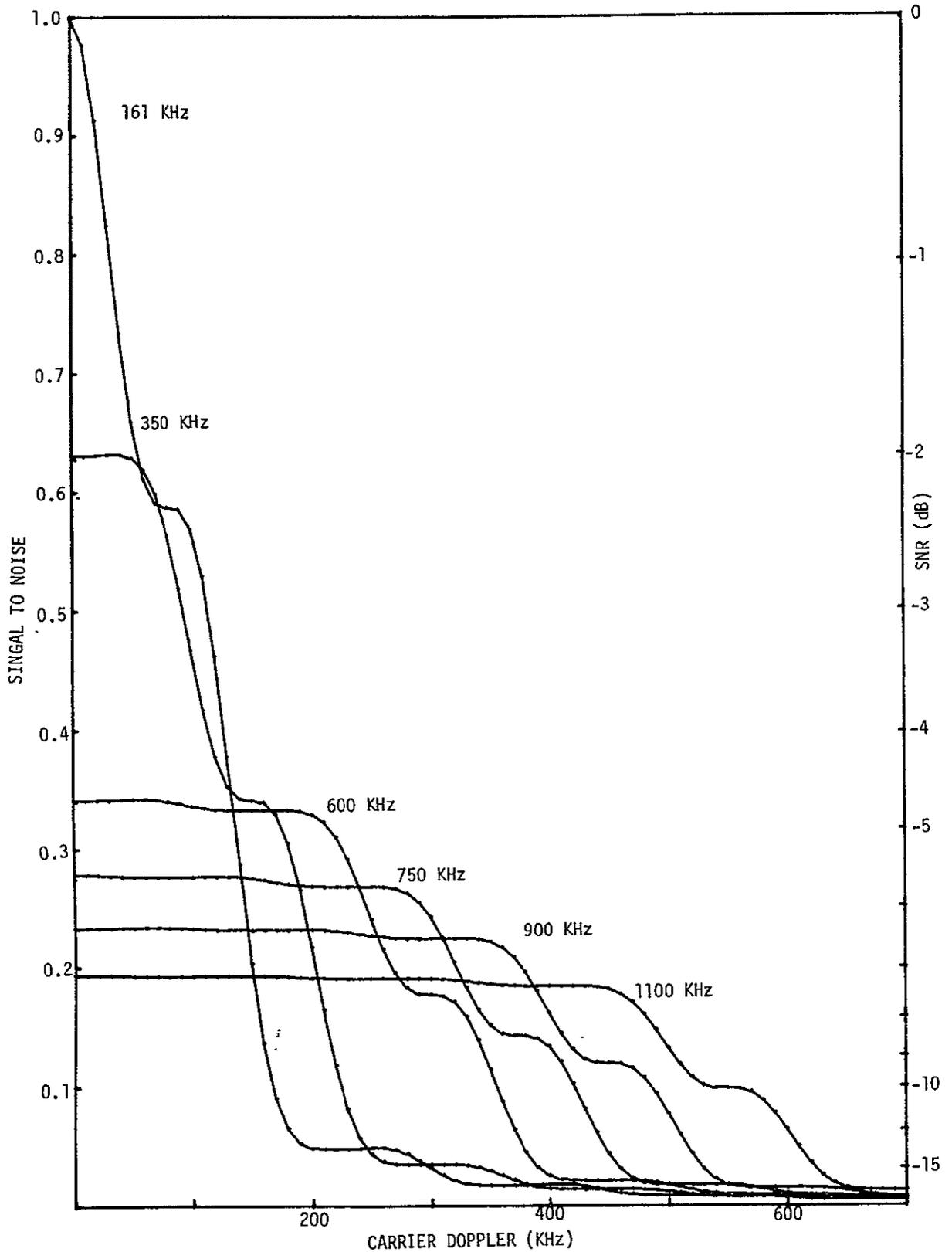
Figure 3-5.   Normalized Signal to Noise Versus Carrier Doppler for
Various IF Filter Bandwidths   (72 kbps)
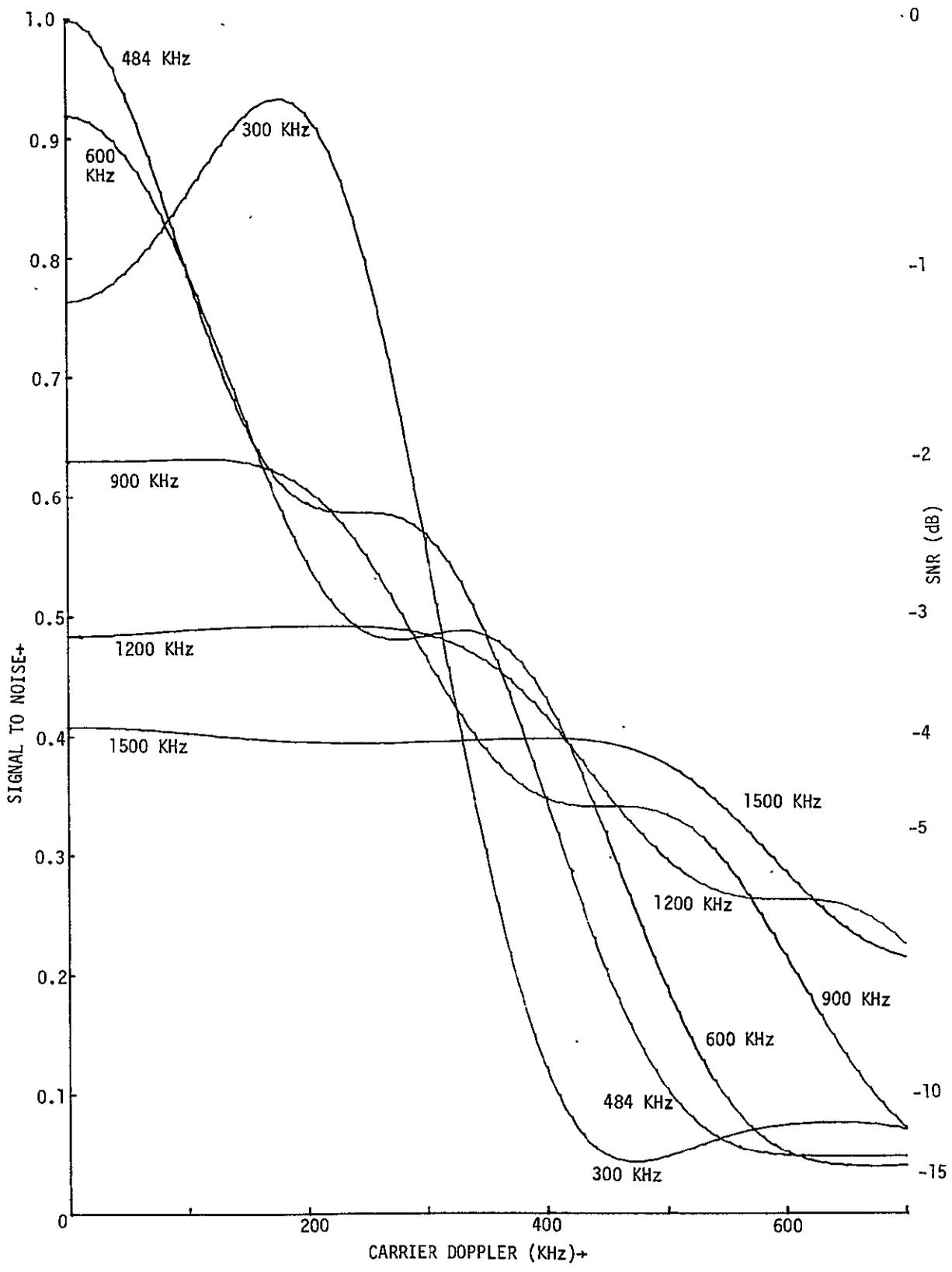
Figure 3-6. Normalized Signal to Noise Versus Carrier Doppler for Various IF Filter Bandwidths (216 kbps)

The 216 kbps (BPSK) modem utilizes filters that are 1.5 MHz·wide due
to the different data rate and a single search (full Doppler) acquisition.
Single search increases the Doppler to 450 kHz, maximum; and as Figure 3-6
illustrates, about 1500 kHz bandwidth is needed. Standard tubular filters
were used for this. The 1.5 MHz filters are mounted on the back panel and
have tan-colored coax cables, while the helical resonator filters for UQPSK
have white cables and are mounted directly underneath the RF PC board.
All filter cables are color coded.

Following the filter in each channel is another 20 dB amplifier to
increase power into the detector. Figure 3-7 illustrates the matching
between detector circuits of the punctual and reference channels. The
matched detectors are important in the gain normalization process, permit-
ting accurate normalization over a wide range of C/N_0 values.
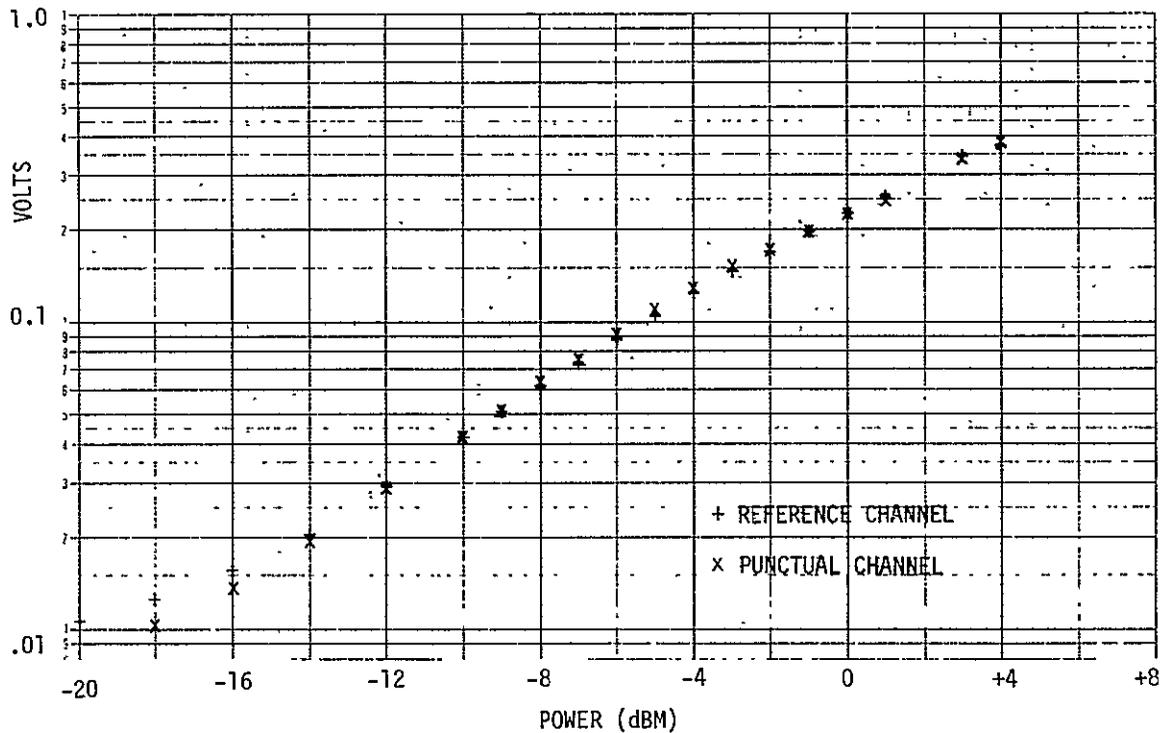
Figure 3-7. Detector Characteristics

3-10

Two-pole active low-pass filters are used in all three channels of the despreader analog circuits. The punctual and tracking channels both use 30 kHz filters immediately following the detectors to limit high frequency noise in the channels. The reference channel filter is lower, 50 Hz, so that the noise added when the punctual and reference signals are summed is insignificant. The reference channel low-pass filter also has a potentiometer, R_{GA}, for making slight adjustments for gain normalization. Figure 3-8 presents representative data comparing designed and measured frequency response curves.
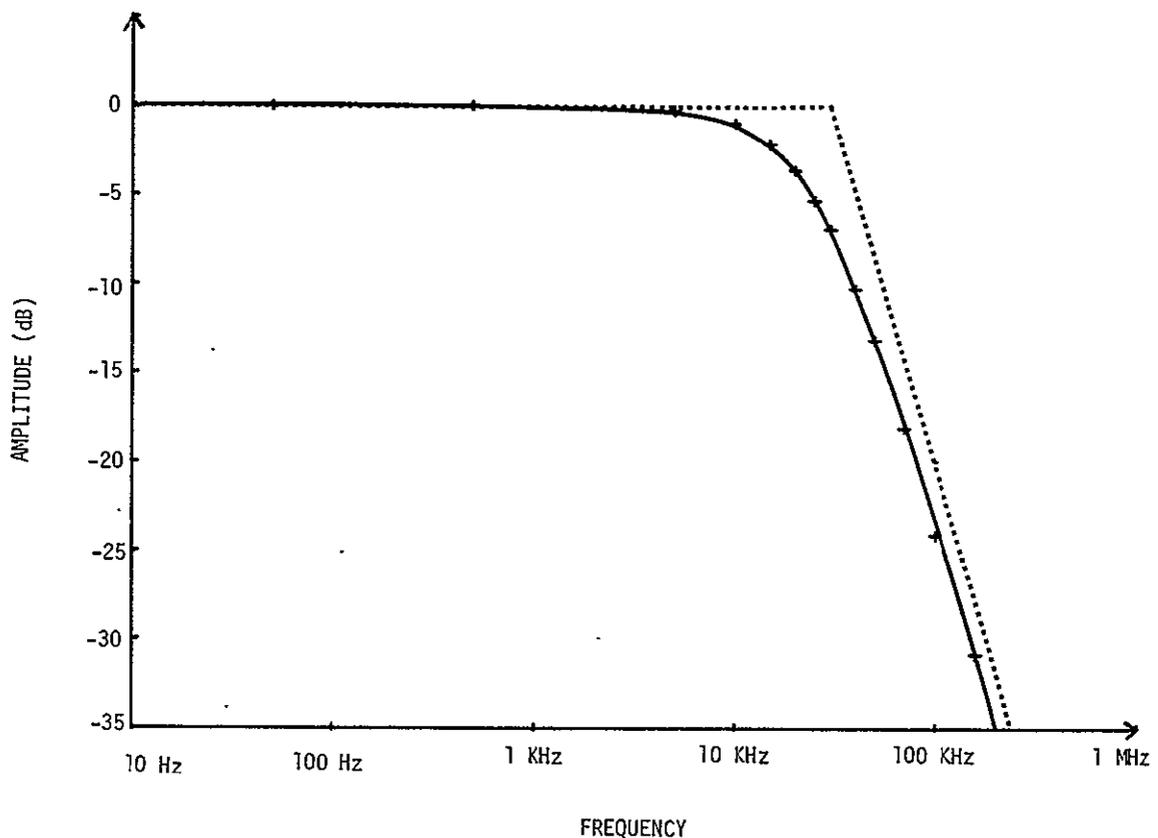
Figure 3-8. Two-Pole 30 kHz LPF Response

The low-pass filtered signals are summed and amplified in another op amp. The gain of each channel is controlled by FET switches which alter the resistances around the op amp, thus establishing proper gain ratios. Two sets of FET switches are used. One set selects between the ratios used during acquisition and tracking, and the other selects between UQPSK and BPSK normalization values.

The delay locked loop of the tracking channel provides the despreader capability of code phase tracking over large Doppler ranges. Essential to the loop is a phase detector producing an S-curve with a null at zero phase error. The generation of the tracking curve was described in Section 2.2; the S-curves for the two modes under several C/N_0 conditions are presented in Figures 3-9 and 3-11b.

The slope of the curve, and the phase detector gain, is an important parameter of the loop, since it is a basic component of dc loop gain. The distribution of gain in the code phase loop is shown in Figure 3-10. It is interesting to note that there is no single component which can be called the phase detector, but rather a series of components (the square-law detector, low-pass filter, and X-Y multiplier) and their individual gains all contribute to the phase detector sensitivity.

Figure 3-11 illustrates the coincident signal levels for code correlation and tracking, plotted as a function of phase error for BPSK. The important fact to be noted is that the correlation peak and the tracking null both occur at nearly the same code phase. While it is obvious that this should be true, in real hardware, care must be taken not to introduce phase difference between the acquisition and tracking channels.

Another basic element of the tracking loop is the VCXO. The VCXO tuning sensitivity also contributes to the total loop gain. The tuning curve for the 56.4 MHz VCXO is presented in Figure 3-12. The slope of the line approximated by the curve yields a VCXO gain (or sensitivity) of about 940 Hz/volt, as was noted in Figure 3-10.

The nonlinearity of the VCXO contributes to an interesting effect in the tracking loop. Loop performance (bandwidth and dampling, in particular) is strongly dependent on dc loop gain. The varying slope of the tuning curve makes the loop gain dependent on Doppler. While the effect was not observed during UQPSK operation (probably due to decreased Doppler) the BPSK mode exhibits asymmetrical pull-in ranges. Due partly to the changes in VCXO gain over a Doppler range of ±1840 Hz (±460 x 4) for the BPSK mode, the loop acquires roughly 150 Hz more positive Doppler than negative Doppler. The problem is easily corrected by offsetting the VCXO by that amount in the negative direction
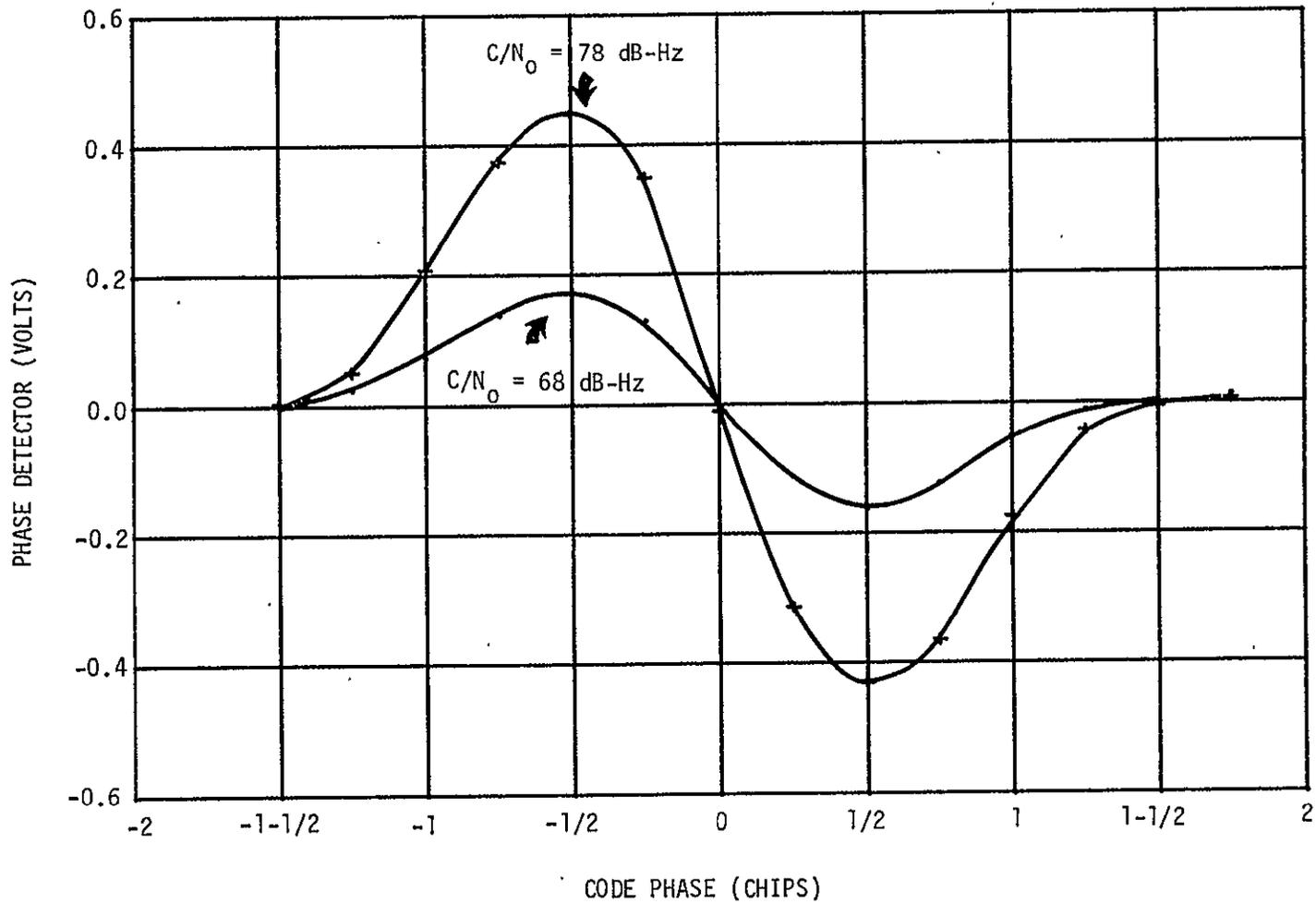
Figure 3-9. UQPSK Tracking Curve

3-13
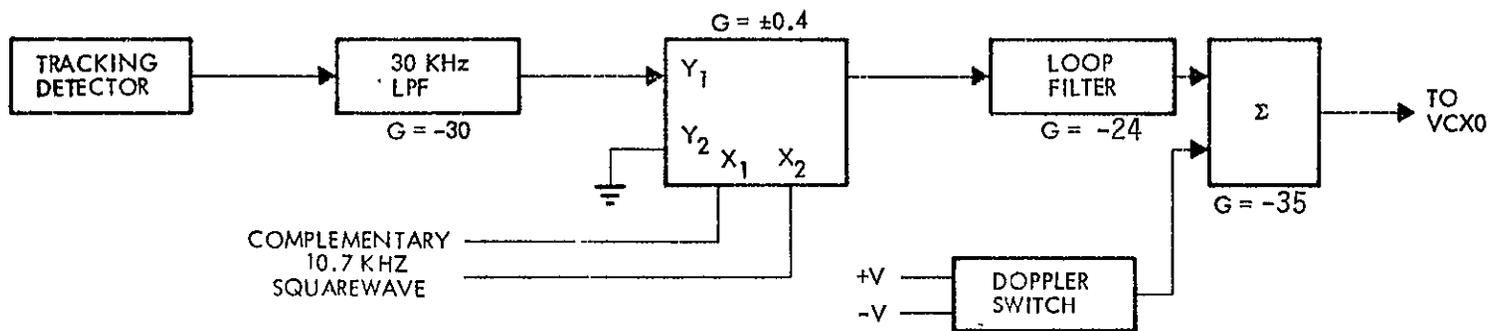
$$\text{DC LOOP GAIN} = \begin{pmatrix} \text{DETECTOR} \\ \text{CORRELATION} \\ \text{SENSITIVITY} \end{pmatrix} \times \begin{pmatrix} \text{30 KHz} \\ \text{LPF} \\ \text{GAIN} \end{pmatrix} \times \begin{pmatrix} \text{X-Y} \\ \text{MULTIPLIER} \\ \text{GAIN} \end{pmatrix} \times \begin{pmatrix} \text{LOOP} \\ \text{FILTER} \\ \text{GAIN} \end{pmatrix} \times \begin{pmatrix} \Sigma \\ \text{GAIN} \end{pmatrix} \times \begin{pmatrix} \text{VCXO} \\ \text{GAIN} \end{pmatrix}$$

$$= \quad \text{40 MV/CHIP} \quad \times \quad 30 \quad \times \quad 0.4 \quad \times \quad 24 \quad \times \quad 35 \quad \times \quad \text{940 Hz/V}$$

$$= \quad 400,000$$

Figure 3-10. Gain Distribution of Delay Locked Loop, UQPSK
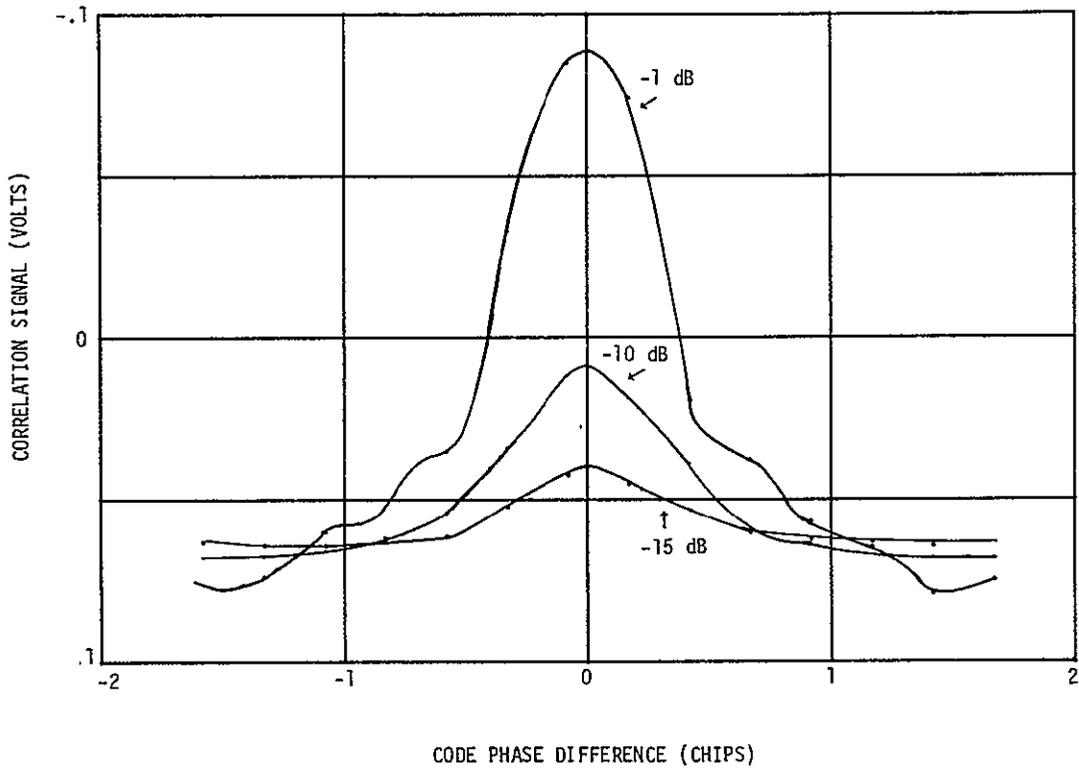
Figure 3-11a. Correlation Signal, Inverted
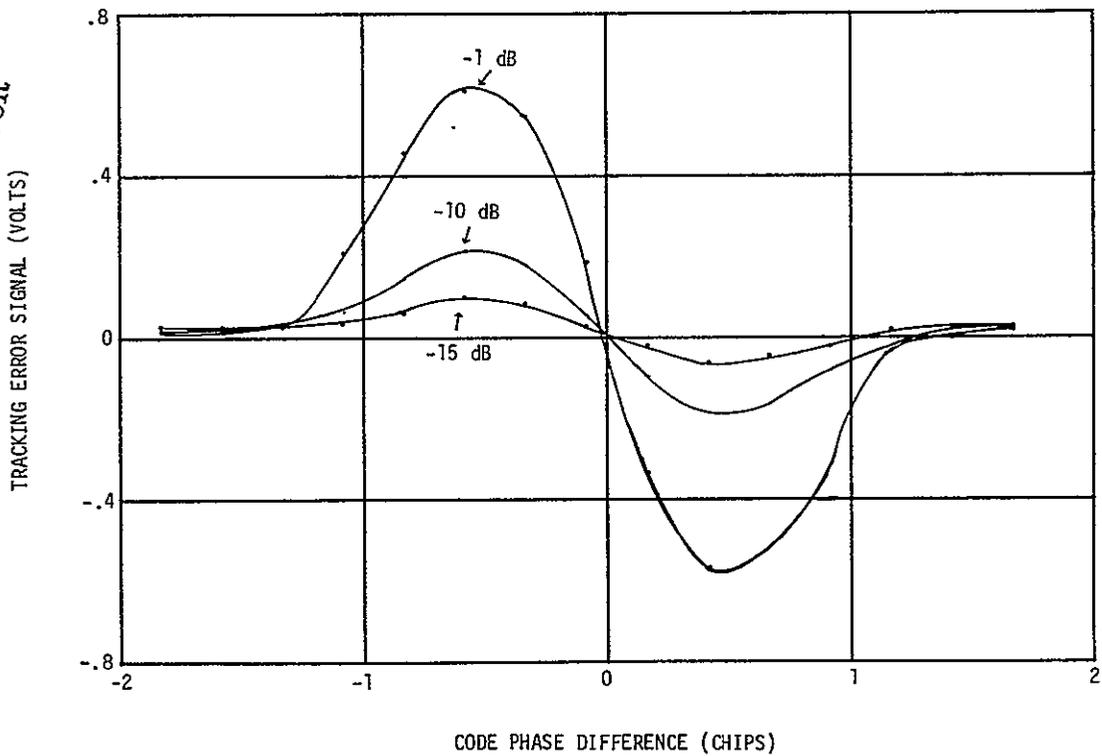
Figure 3-11b. Tracking Signal

3-15
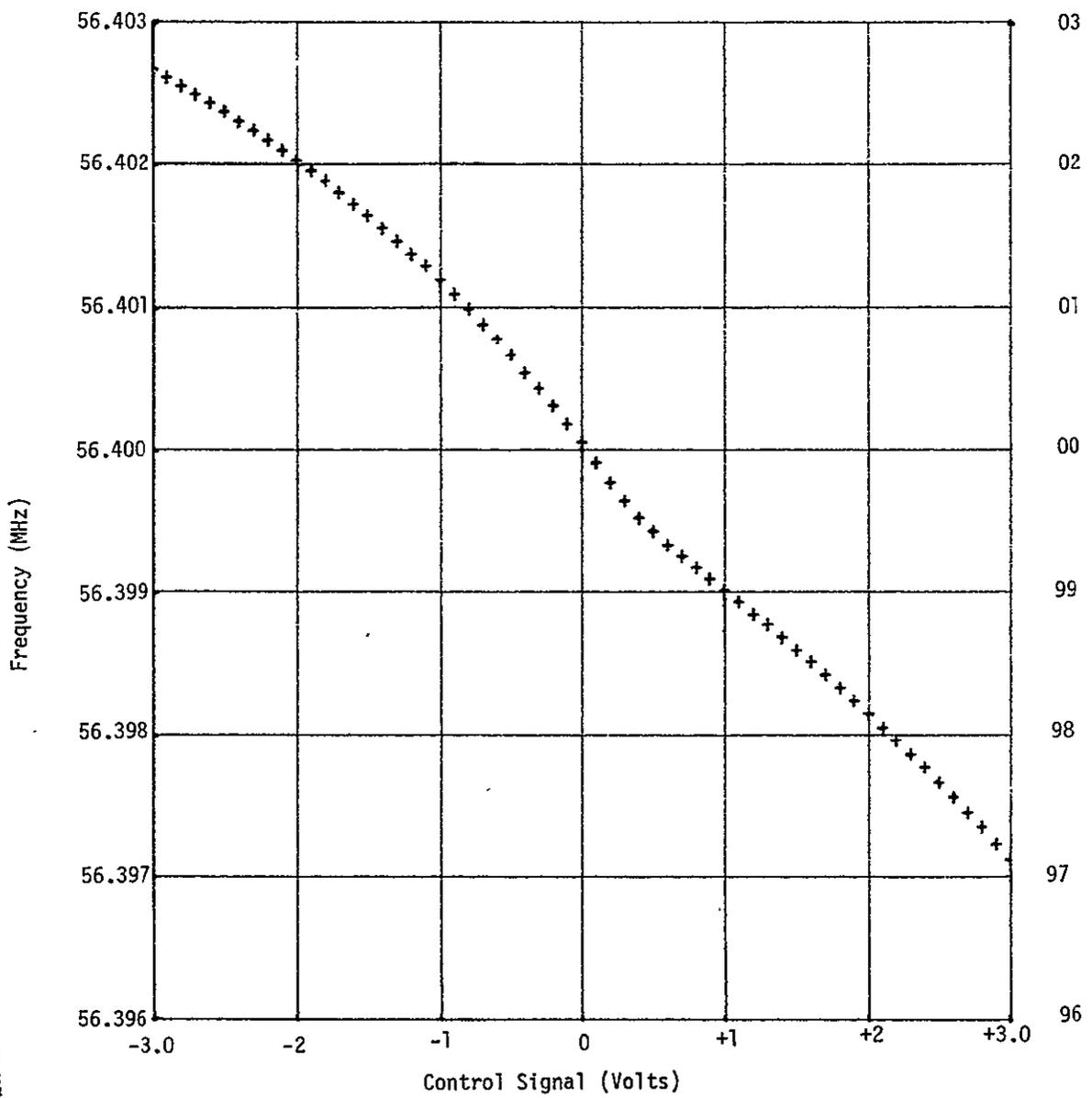
Figure 3-12.   56.4 MHz VCXO Characteristic

The loop filter is easily the most important component in determining tracking performance. The response of the loop is primarily determined by the location of a pole and zero for a second-order transfer function. (This fact makes it possible to alter the loop response for the two modes by simply switching the feedback network of an active loop filter.) The UQPSK loop was designed to have B_L = 0.707 and B_L = 265 Hz at 68 dB-Hz C/N_0 (-7 dB SNR). The measured response (Figure 3-13) indicates proper damping and B_L ~ 250 Hz for that SNR.

The BPSK loop filter was designed for B_L = 488 Hz and 0.707 damping at 64 dB-Hz C/N_0. Measured data verifies that design, also. Note that Figure 3-13 indicates wider loop bandwidth and increased damping for stronger signals. Conversely, this implies that the BPSK loop will be somewhat narrow and under-damped when operating at 60 dB-Hz C/N_0, i.e., with antenna and receiver loss margin. A graph illustrating loop response to AGC variations at minimum SNR is included as Figure 3-14.

Loop pull-in is illustrated in Figure 3-15, which shows the tracking signal (VCXO control voltage) at the time threshold is exceeded. The botton trace of Figure 3-15 shows the jump in code correlation when the last quarter-chip step is made. At that time the tracking loop is connected to the VCXO and the code phases aligned. Note the increase of code correlation as the phase is pulled-in independently of stepping.

3.3 CODE ACQUISITION LOGIC

Despreader operation is controlled by the code acquisition logic circuits, shown in Figure 3-16. The board holds mostly digital IC's which are hard-wired to perform the functions required by the acquisition logic flow diagram discussed in Section 2.1 (see Figure 2-7). Basically, the board consists of the following circuits:

1) A divider chain needed for a synchronous dwell times which derives all necessary frequencies (and periods) from the code clock

2) A code position counter needed for the UQPSK double search routine

3) A dump command pulse generator

4) An integrate and dump circuit

5) A threshold detector.

3-17
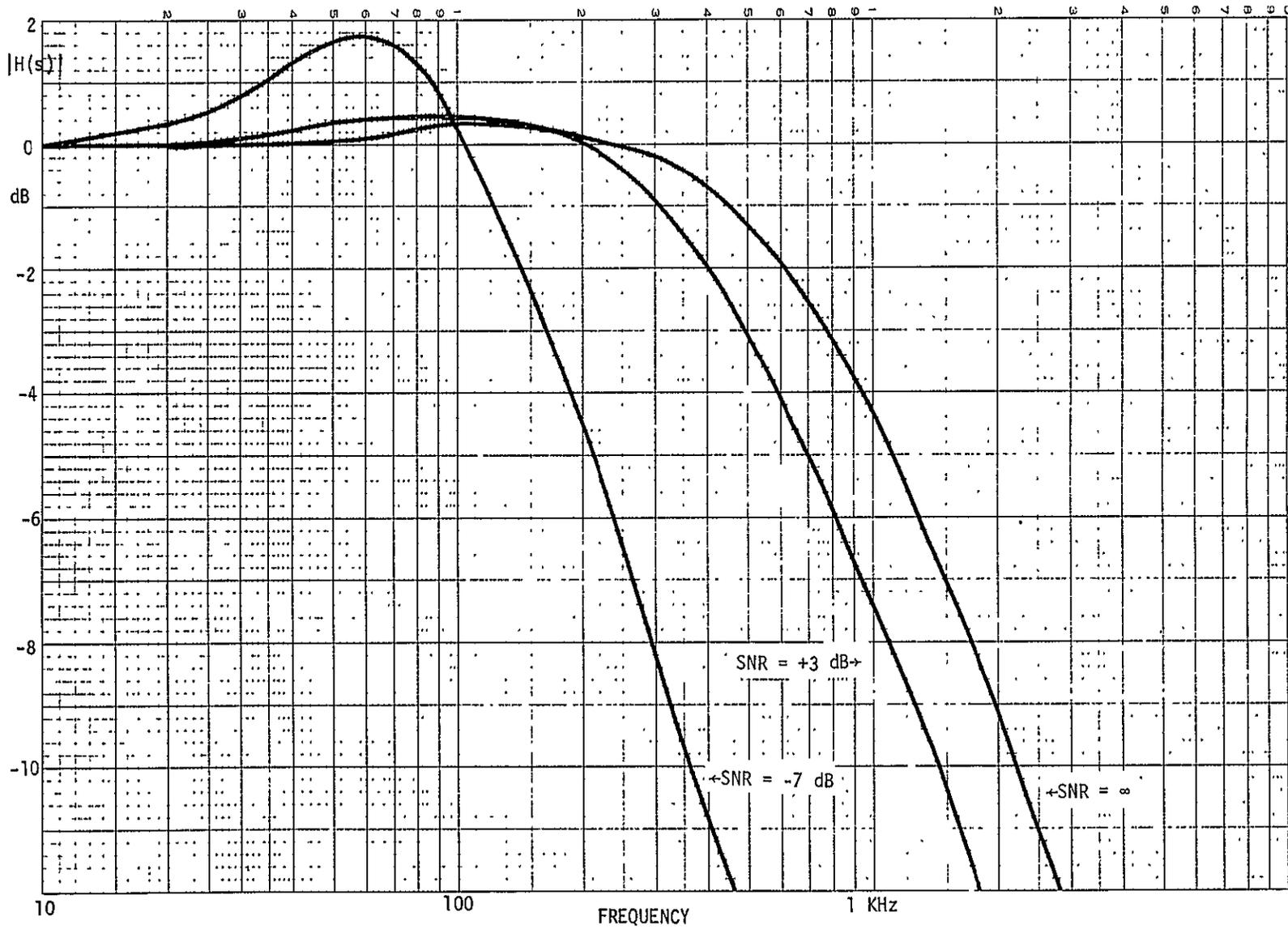
Figure 3-13. UQPSK Loop Response for Various SNRs

$|H(s)|$

dB

Input -15 dBm

Input -16 dBm

Input -14 dBm

FREQUENCY

10

100

1 KHz
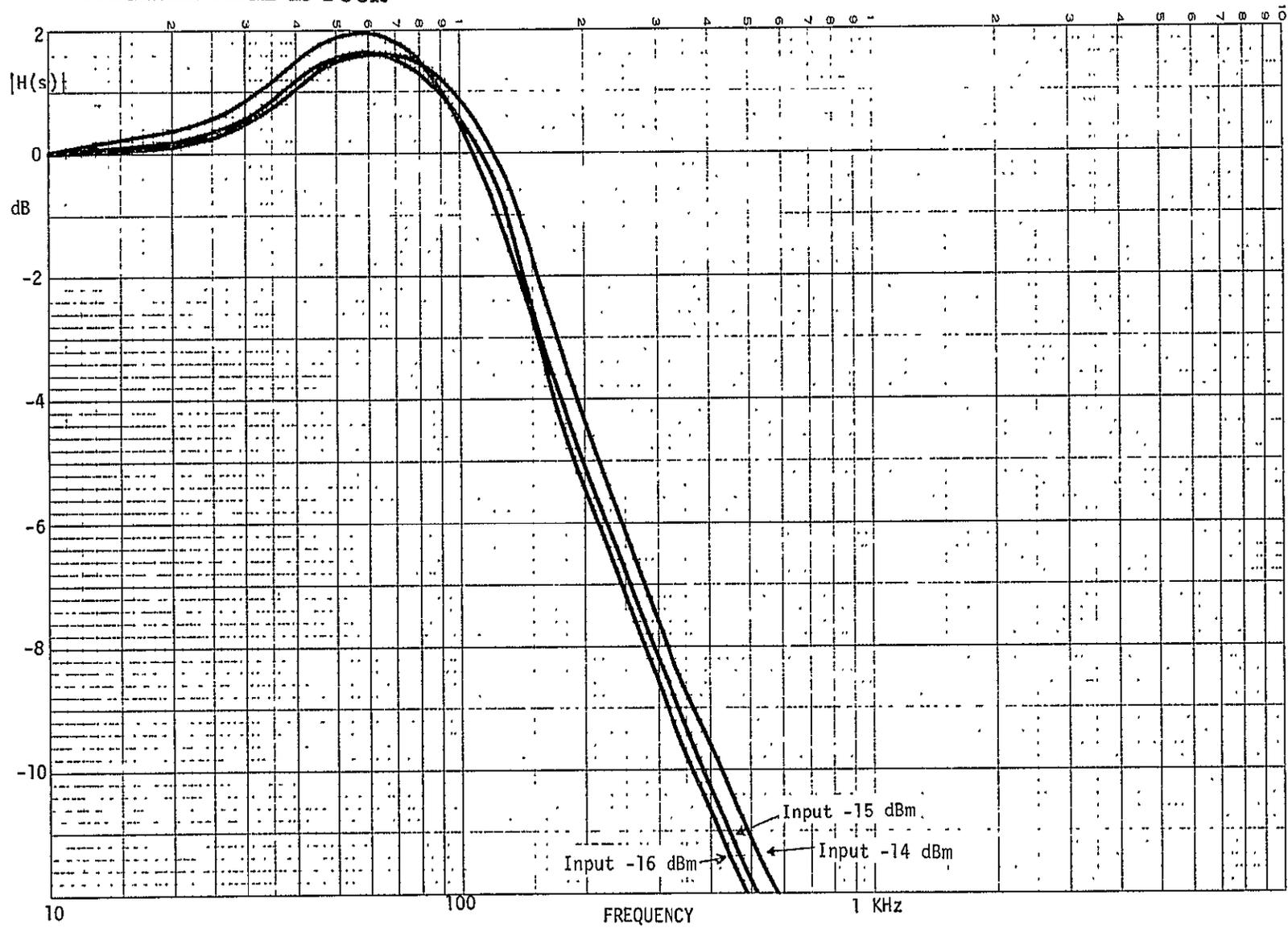
Figure 3-14. UQPSK Loop Response to AGC Variations

Threshold
Exceeded   Pull-In   Lock

TRACKING SIGNAL
2V/DIV

← GND

← GND
1V/DIV
CODE CORRELATION

0.1 mSEC/DIV →
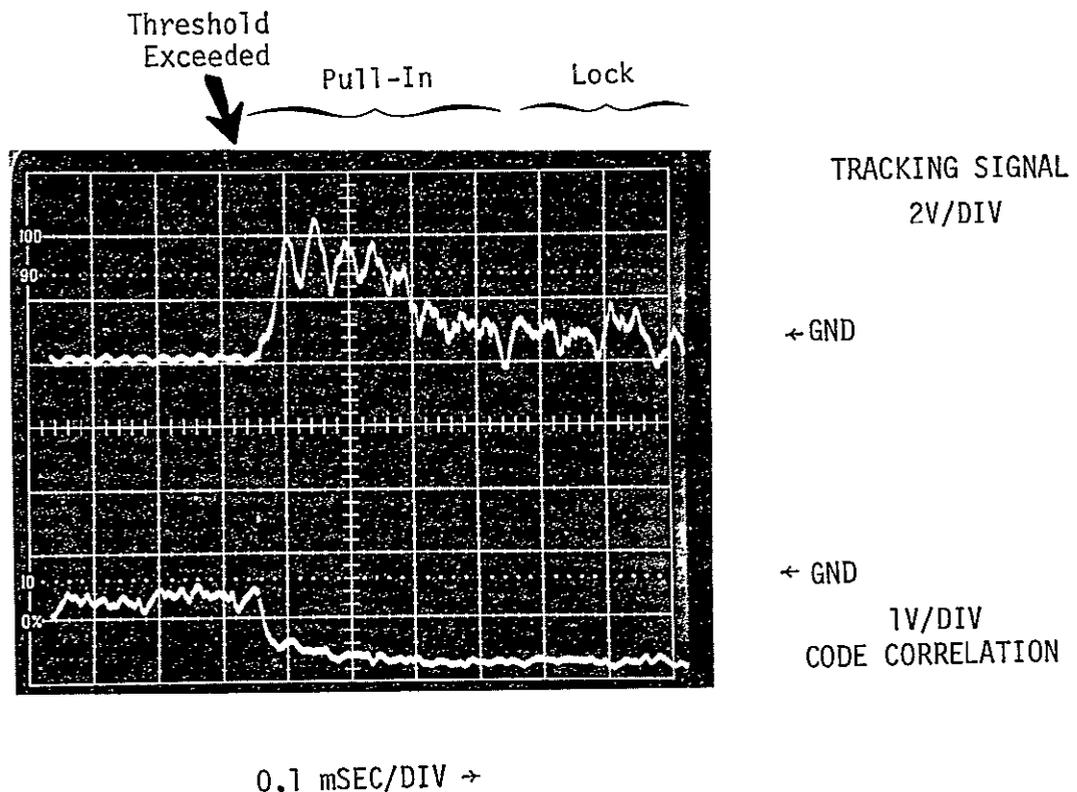
Figure 3-15. Tracking Signal During Pull-in

Figure 3-17 shows the board layout.

Key waveforms generated on the code acquisition logic board are shown in two timing diagrams. Figure 3-18 shows the relationship between frequencies which produce the synchronous dump command. Figure 3-19 illustrates the sequence of signals during acquisition.

The normalization of gains in the punctual and reference channels yields a zero voltage threshold. That is, correlated and noncorrelated signals are indicated by opposite polarities. An integrate-and-dump circuit is used for SNR improvement, match filtering the correlation voltage. Figure 3-20 shows the integrated voltage at 60 and 65 dB-Hz C/N_0 during lock, i.e., code phase alignment. A comparator level detects the integrator voltage, producing a "1" for voltages greater than threshold. The comparator output is sampled at the end of each integration period (dwell time). This sampled
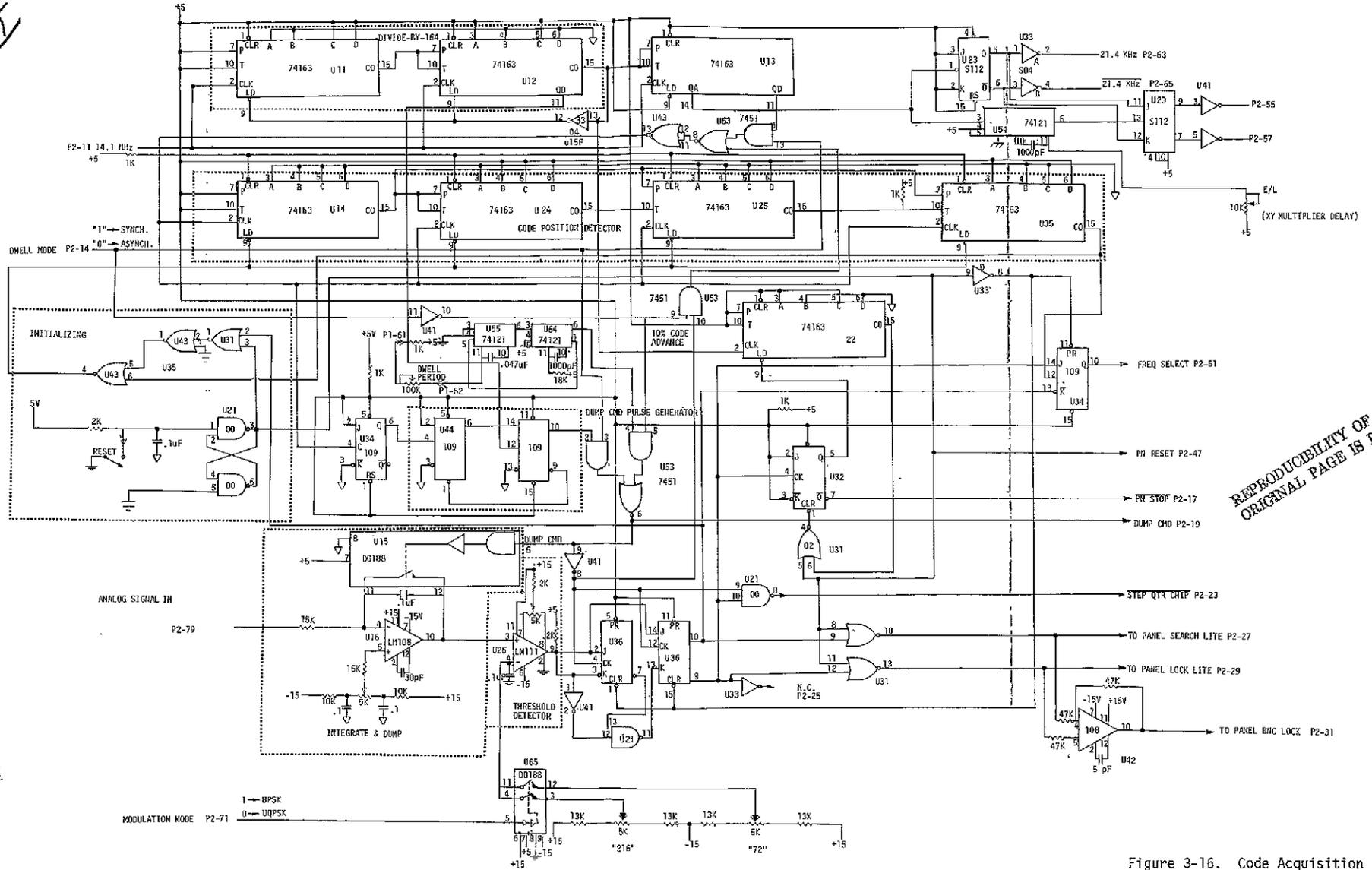
Figure 3-16. Code Acquisition Logic Schematic
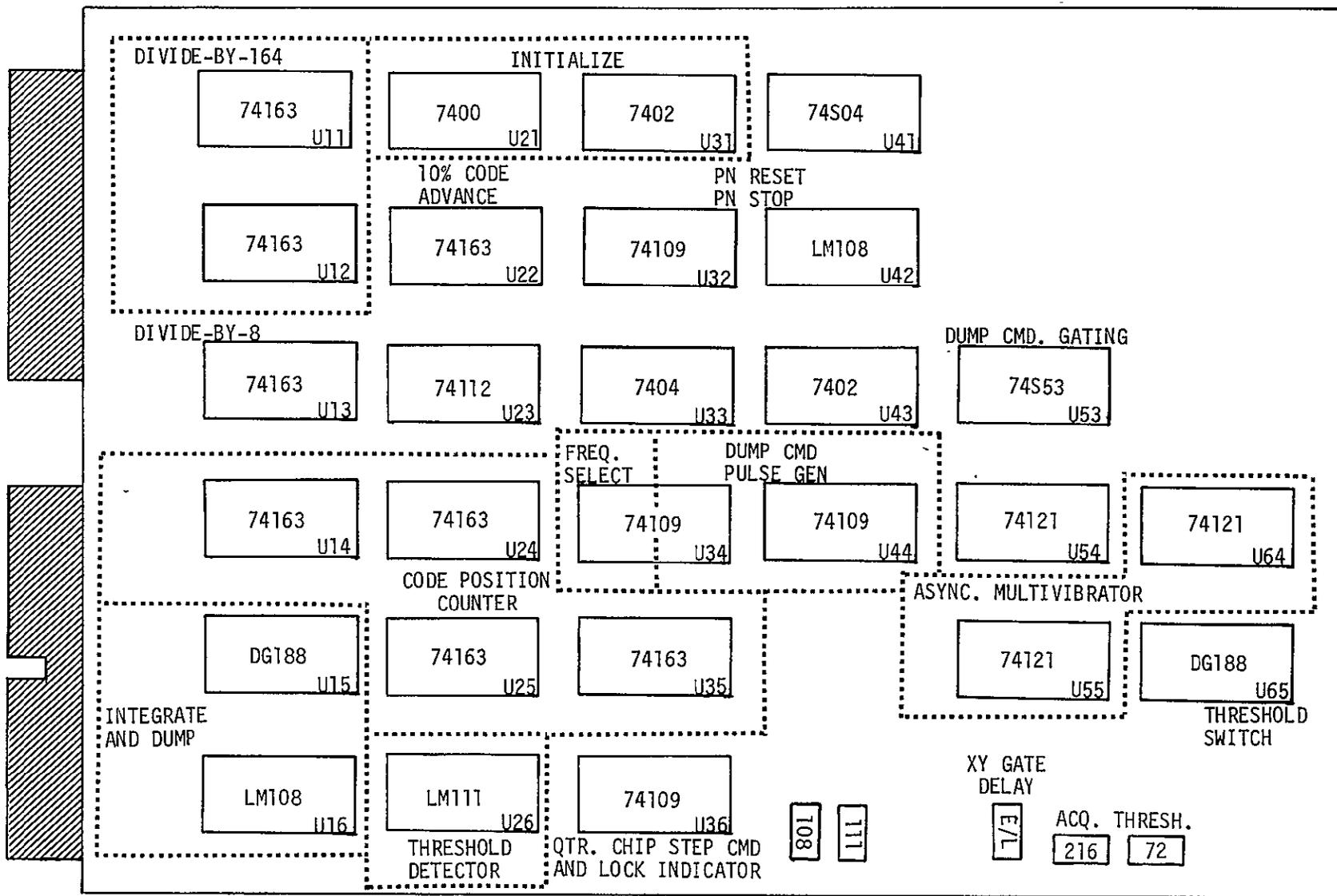
3-22

Figure 3-17. Code Acquisition Board Layout

(DIVIDER)   U13p11

U34p6

372 μSec

SYNCHRONOUS
DUMP CMD   U44p6

11.6 μSec

U12p11

(DUMP PULSE)   U49p9

11.6 μSec

U34p6

11.6 μSec

U12p11

U44p6

U44p9
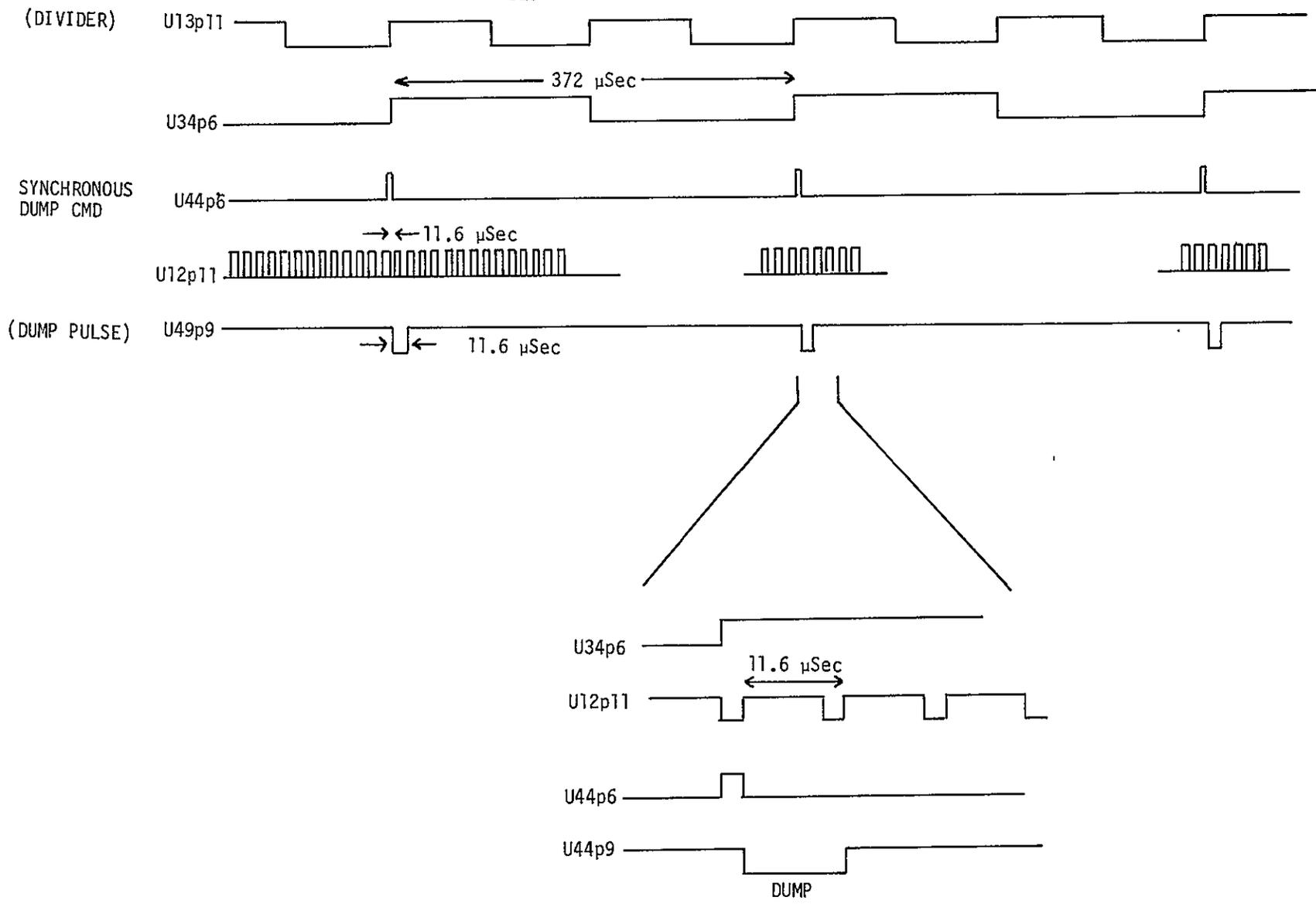
DUMP

Figure 3-18.   Code Acquisition Control Timing
(Dump Command)

DUMP PULSE U44p10

THRESHOLD COMPARATOR U26p9

U36p6

LOCK INDICATOR U36p10

STEP QTR CHIP U21p8

PN STOP U32p5
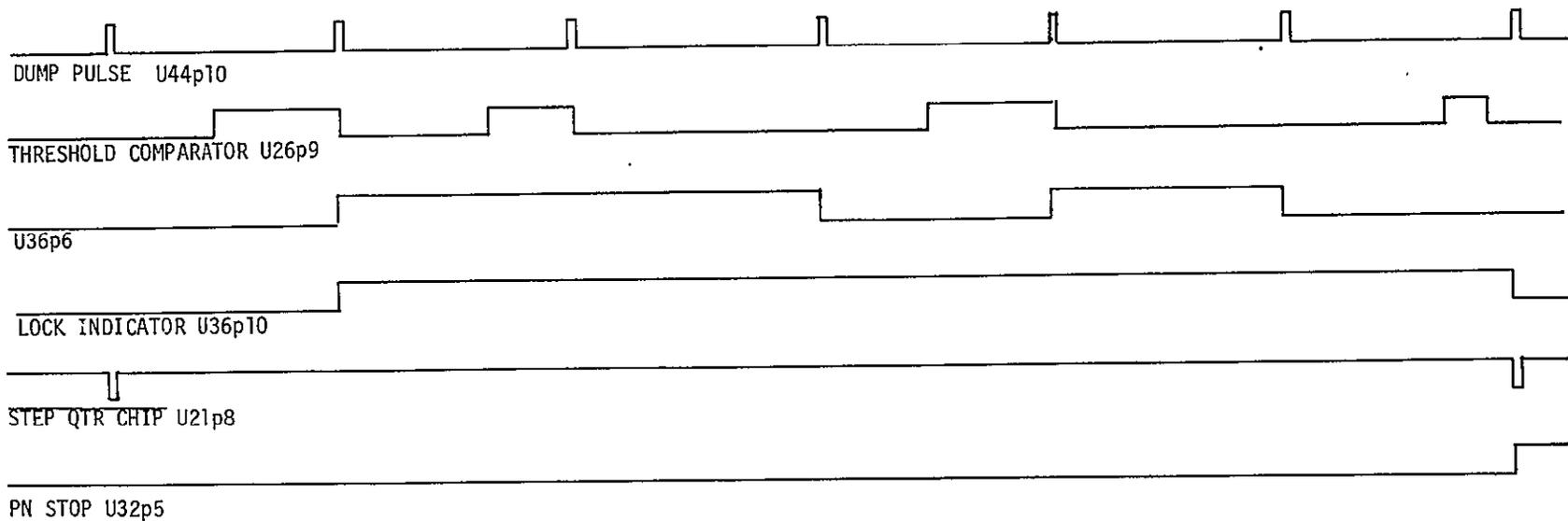
Figure 3-19.   Code Acquisition Control Timing
(Step Command)

a. -15 dB SNR

   BPSK Mode

     Hor: 0.1 msec/div
     Vert: 0.2 V/div
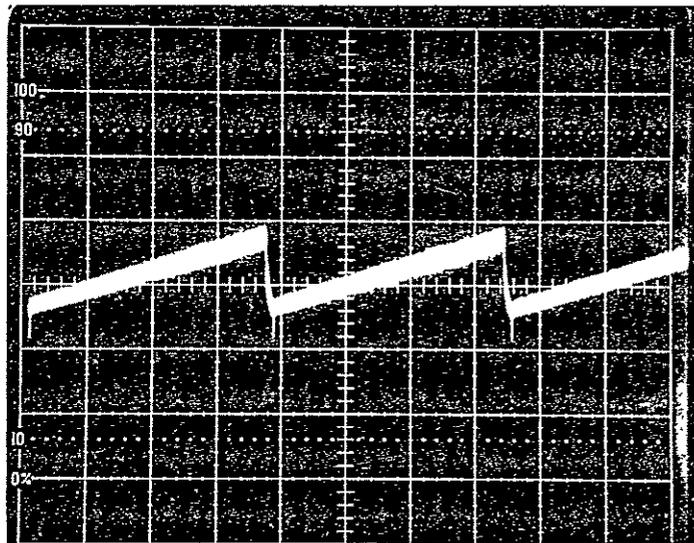
b. -10 dB SNR

   BPSK Mode

   Hor: 0.1 msec/div

   Vert: 0.2 V/div
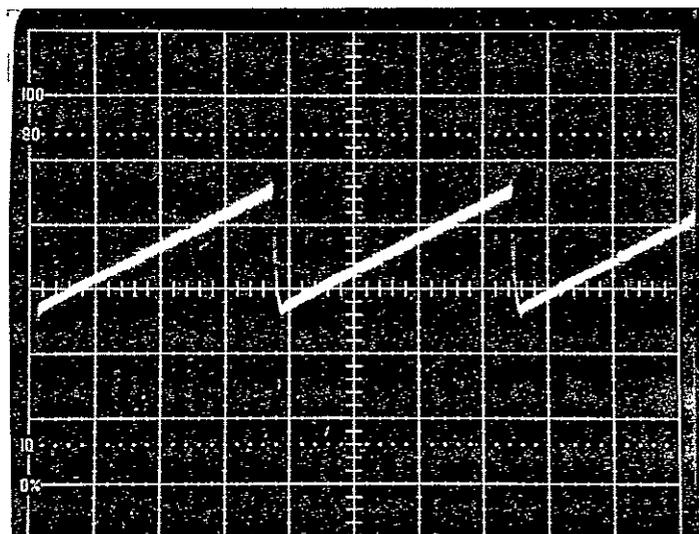
Figure 3-20. Integrate-and-Dump Signals During Lock

data controls the logic sequence, initiating a quarter-chip step command when the integrator is below threshold at the end of a dwell time. When threshold is exceeded, the code phase is not stepped, the LOCK light on the despreader is turned on, and the tracking channel output is allowed to pull-in the VCXO.

3.4 PN CODE GENERATOR

An 11-bit shift register is used to generate the despreader PN code, using the 9 and 11 feedback taps. The shift register is clocked by one-quarter times the VCXO frequency (14.1 MHz). Complementary outputs of the code are used to drive the punctual and tracking channel correlators, thus reducing losses. Figure 3-21 shows the circuitry of the PN generator board.

The board holds several auxilliary circuits beside the PN generator shift register itself. The divide-by-four and quarter-chip inhibit circuits are located on the PN generator board to reduce path length of the 56.4 MHz signals. The quarter-chip inhibit circuitry functions by making the divide-by-four "slip" a step so that when a step command is given there is one divide-by-three cycle. Figure 3-22 illustrates the timing sequence. A second divide-by-four provides the 14.1 MHz clock to the code acquisition logic. A 14.1 MHz clock independent of the step commands is needed because the clock itself is used to generate the step commands.

The PN generator board also has an activity detector, which monitors the PN code and resets the shift registers in the event the register locks in the forbidden state. Additionally, there is a sync circuit which generates a pulse once during every PN word. The position of the pulse relative to the word can be selected by hard-wiring the sync circuit. A one-shot lengthens the pulse produced so that an oscilloscope can be triggered easily.

Gating circuits are also provided for using an external PN code. The code can be input from the despreader front panel. The external enable connection, also on the panel, injects the external code into the final shift register stages so that early/late gating can function as normal. The external code must be clocked by the despreader's 14.1 MHz clock for proper despreader operation. Layout of the PN generator circuits is shown in Figure 3-23.

Figure 3-21. PN Generator Schematic
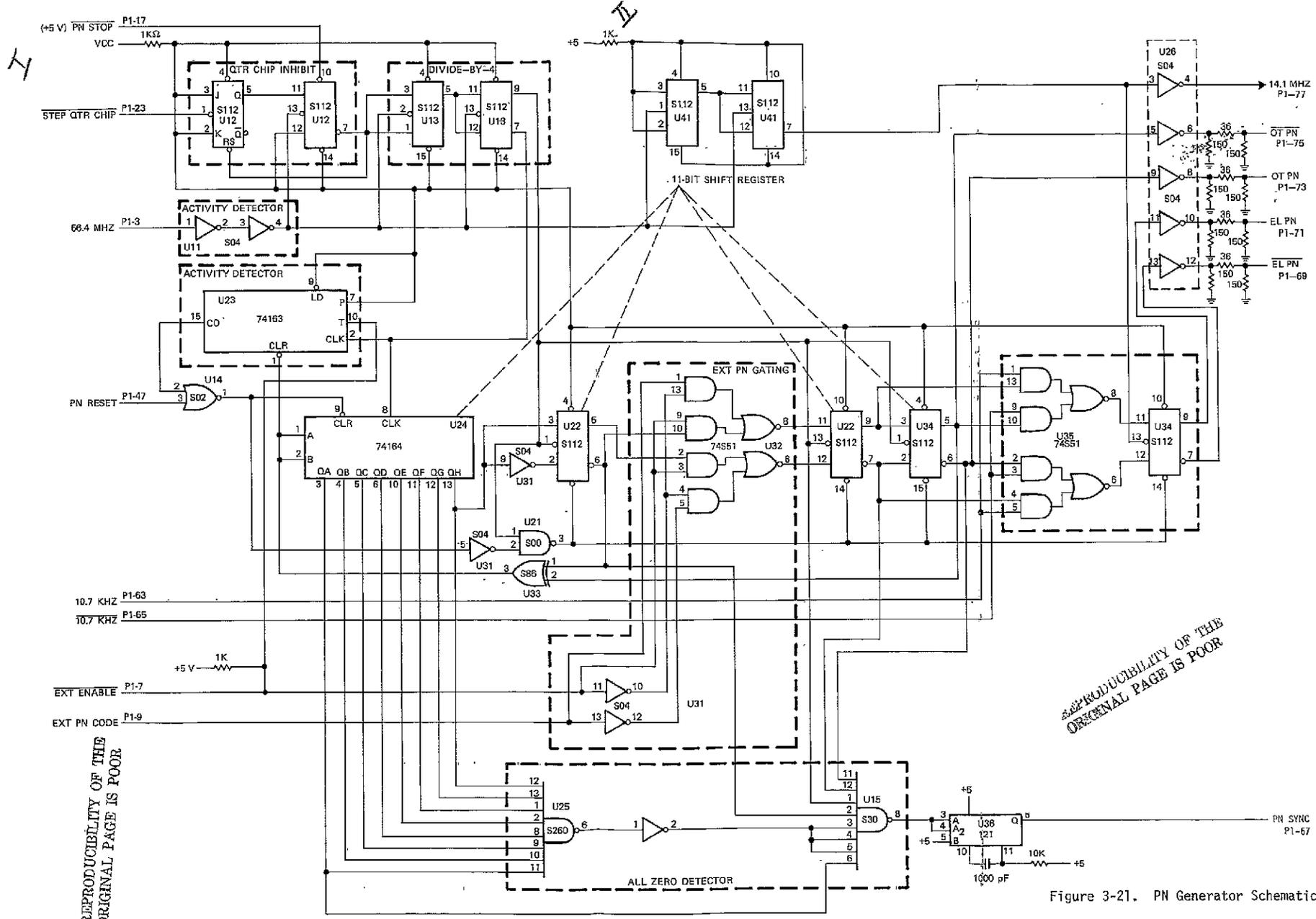
REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

56.4 MHz   U11-4

Step Qtr. Chip   P1-23

U12-5

U12-7

U13-5 .   Advanced by 1/4 chip

14.1 MHz   U13-9
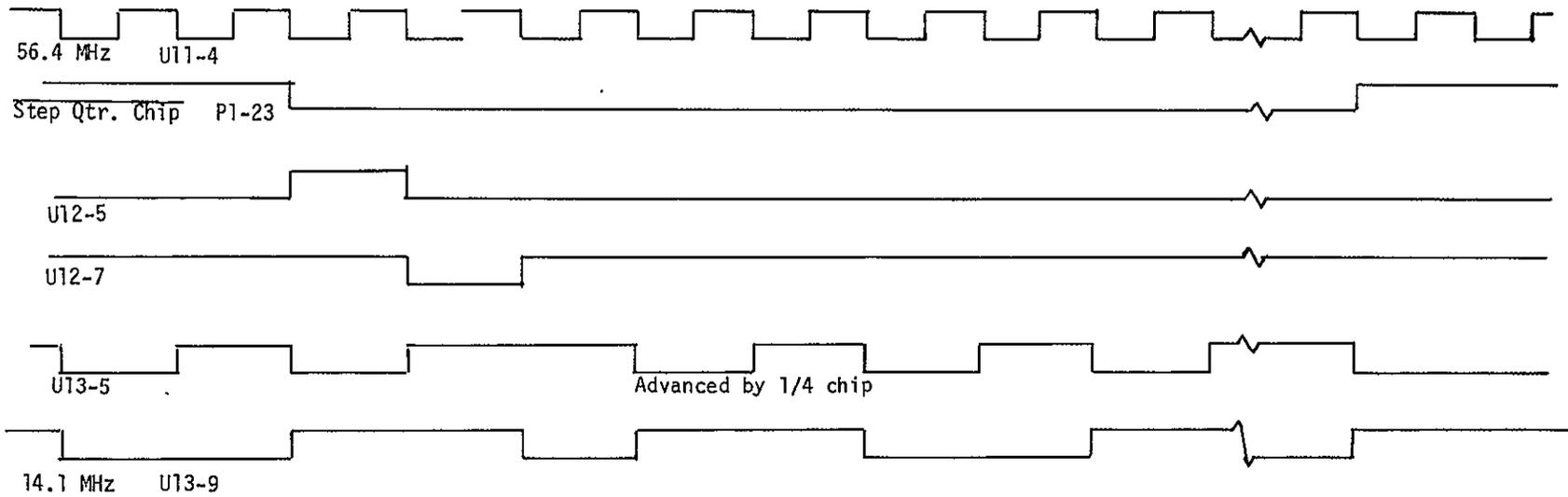
Figure 3-22.   PN Code Generator Timing
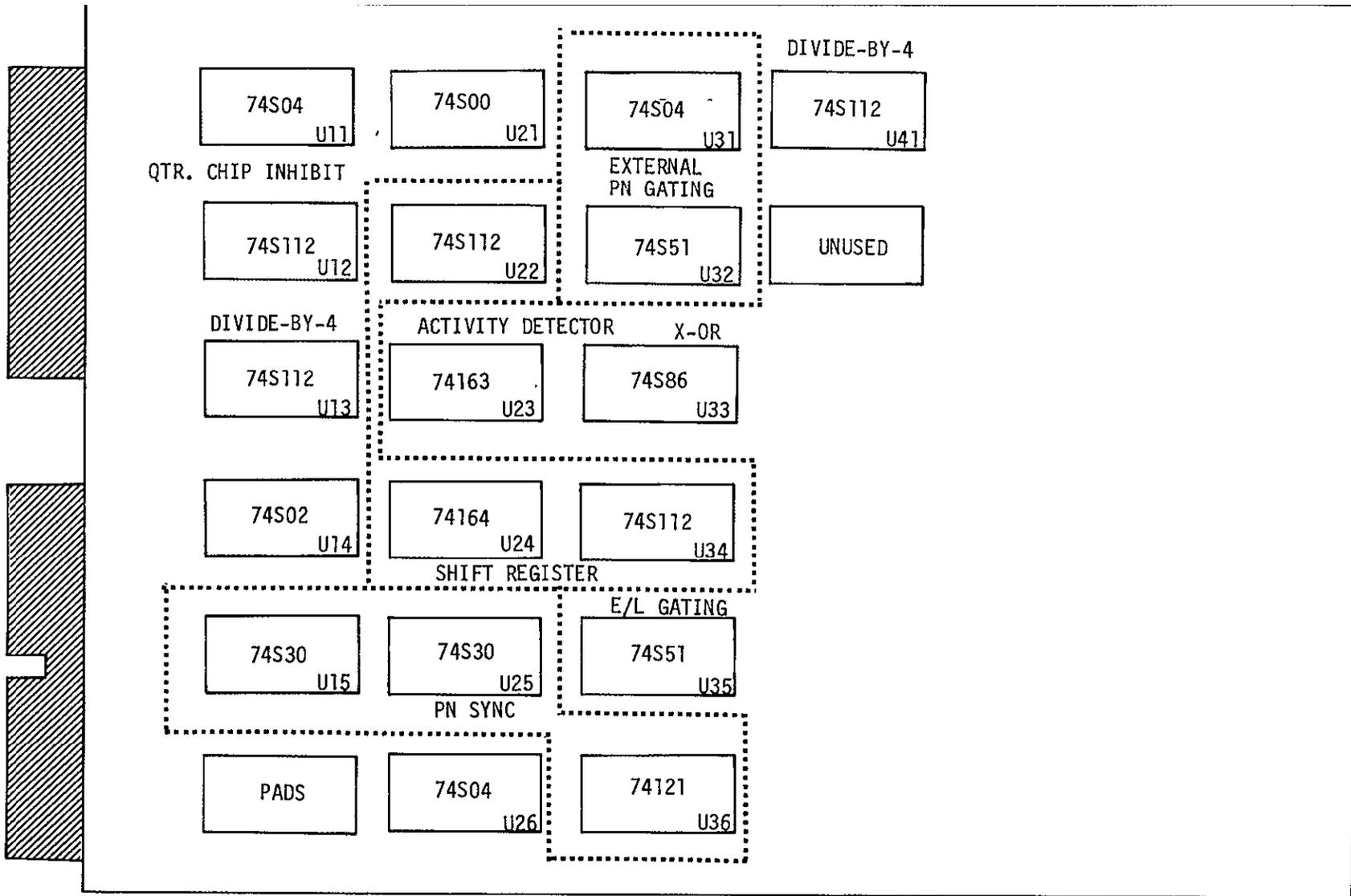
Figure 3-23. PN Generator Board Layout

3.5 DESPREADER PANELS AND CHASSIS

The despreader front and rear panels are shown in Figures 3-24 and 3-25. They are included here for convenience and completeness. The panel connections are discussed in detail in Section 2.3.

A top view of the despreader with the cover removed is shown in Figure 3-26. The RF PC board and code acquisition logic board locations are clearly shown. The PN generator board is located underneath the code acquisition logic board.

The despreader by-pass cable is also shown in Figure 3-26, mounted on the back of the front panel (lower right of picture). A brass-board circuit is also seen mounted on the back of the panel. It contains a 7 dB coupler and 50Ω termination. The incoming by-pass signal is sent through the coupler and terminated. The coupled port goes through the coax cable and returns to the panel. This circuit closely matches the phase shift and power level of the despreader output.

Five potentiometers on the top right of the code acquisition logic board are also shown clearly in Figure 3-26; they are labeled "72" "216," "E/L," "111" and "108." The last two mentioned, "111" and "108" are offset adjustments for the comparator and integrate-and-dump circuits, respectively. They should need no adjustment. The middle pot, "E/L" controls the delay of the 21.4 kHz gating signal going to the X-Y multiplier of the reference channel. It too should need no adjustments.

The two pots closest to the rear of the despreader, "72" and "216," control acquisition threshold for the UQPSK and BPSK modes, respectively. Although they have been set properly for despreader performance as specified, it may be desirable to experiment with different dwell times, false alarm and detection probabilities, etc.; such experiments would require threshold adjustment.

A bottom view of the despreader with covers removed is shown in Figure 3-27. The large 28 volt power supply as well as the two smaller dc-to-dc converters are shown. The VCXO is also to be noted, to the left of the 28 volt supply.
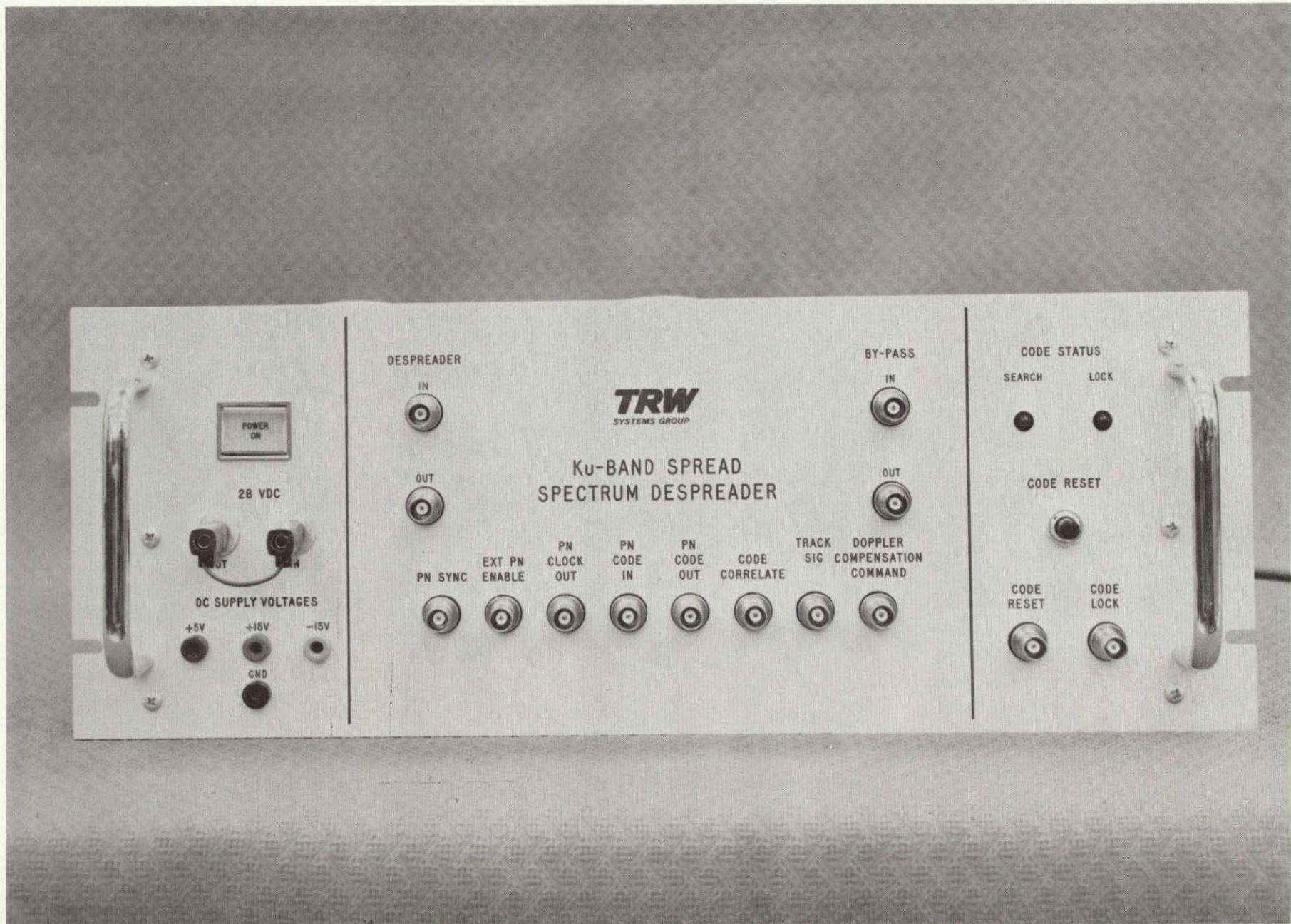
Figure 3-24. Despreader Front Panel
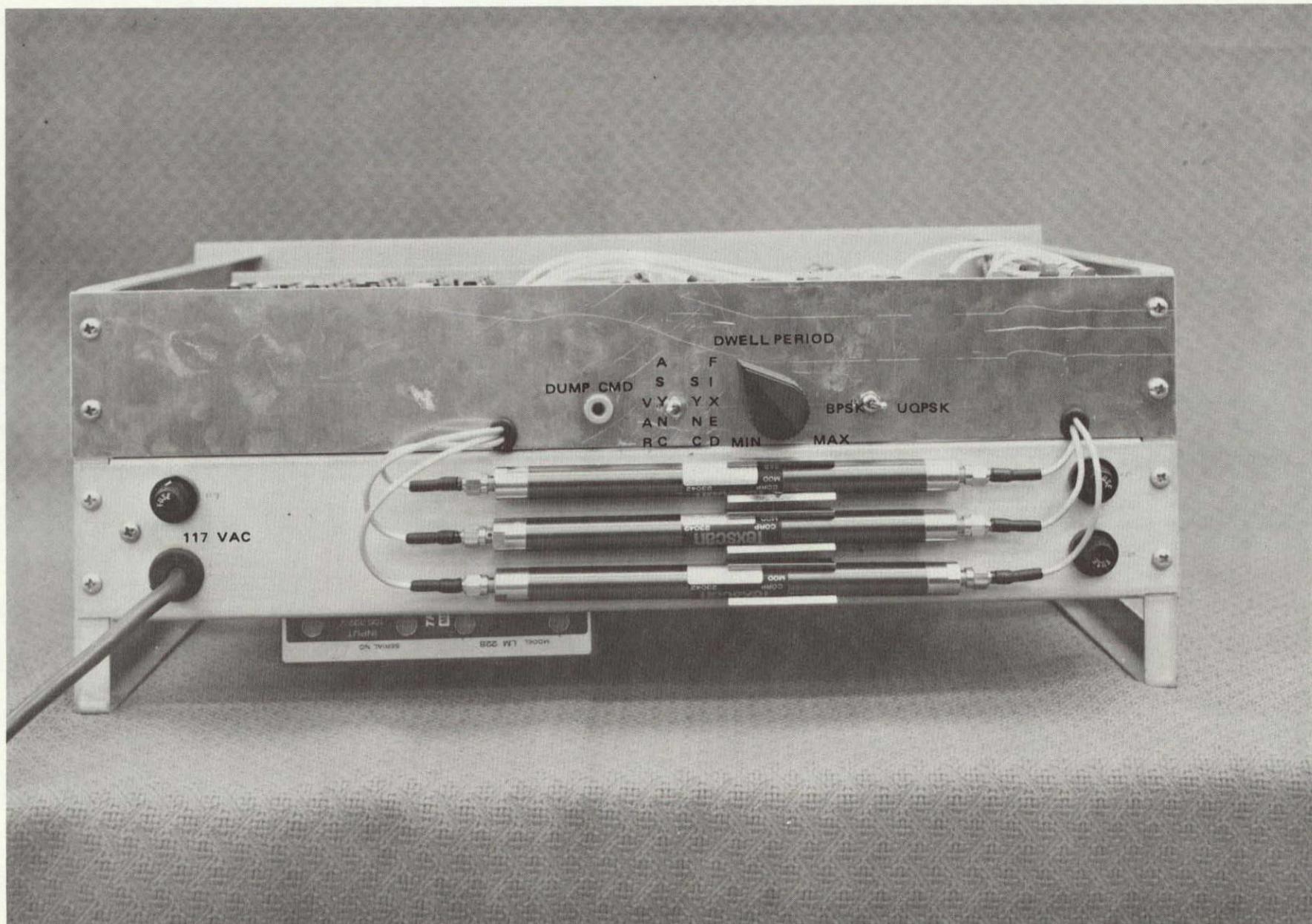
Figure 3-25. Despreader Rear Panel
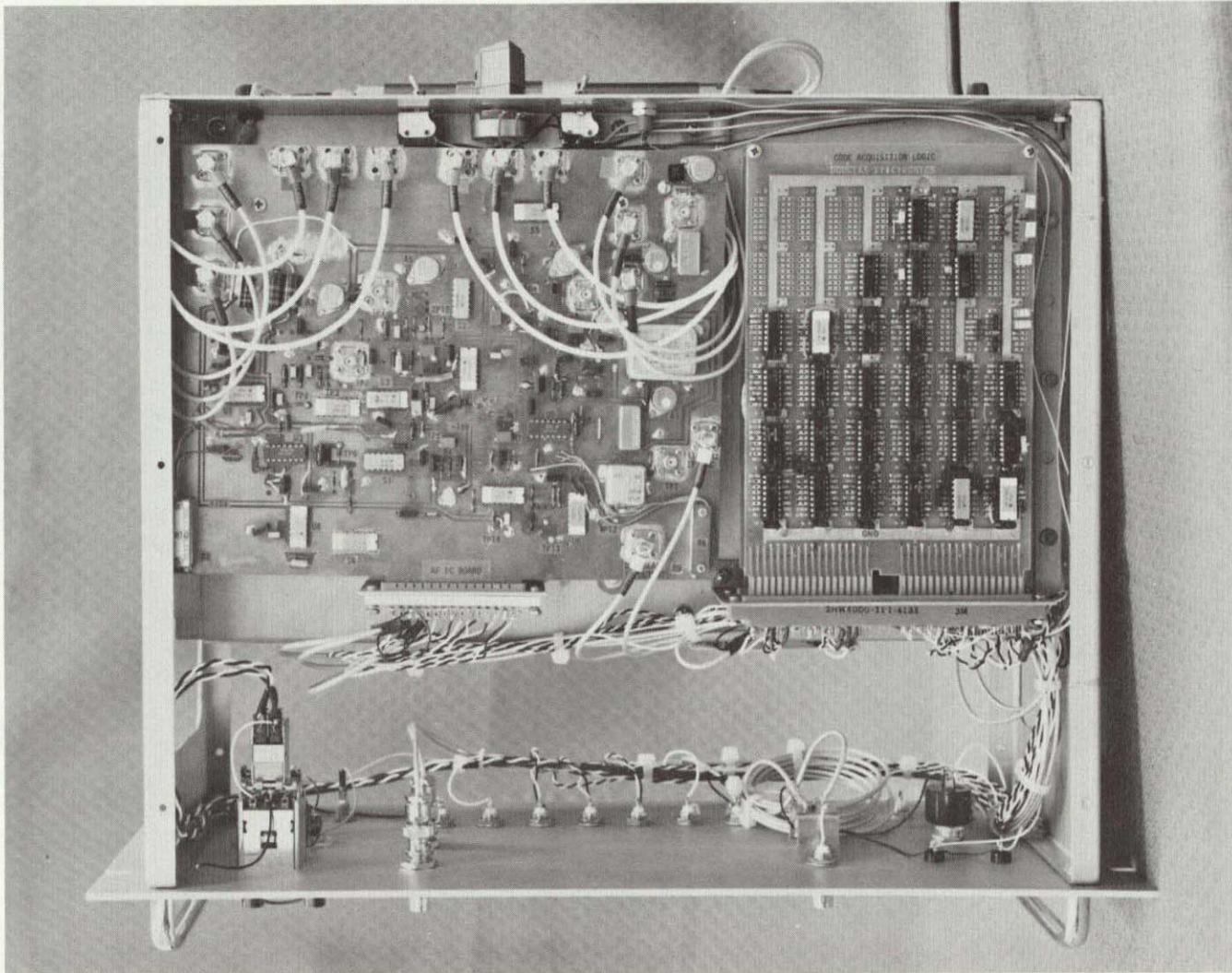
Figure 3-26.   Top View of Despreader Chassis
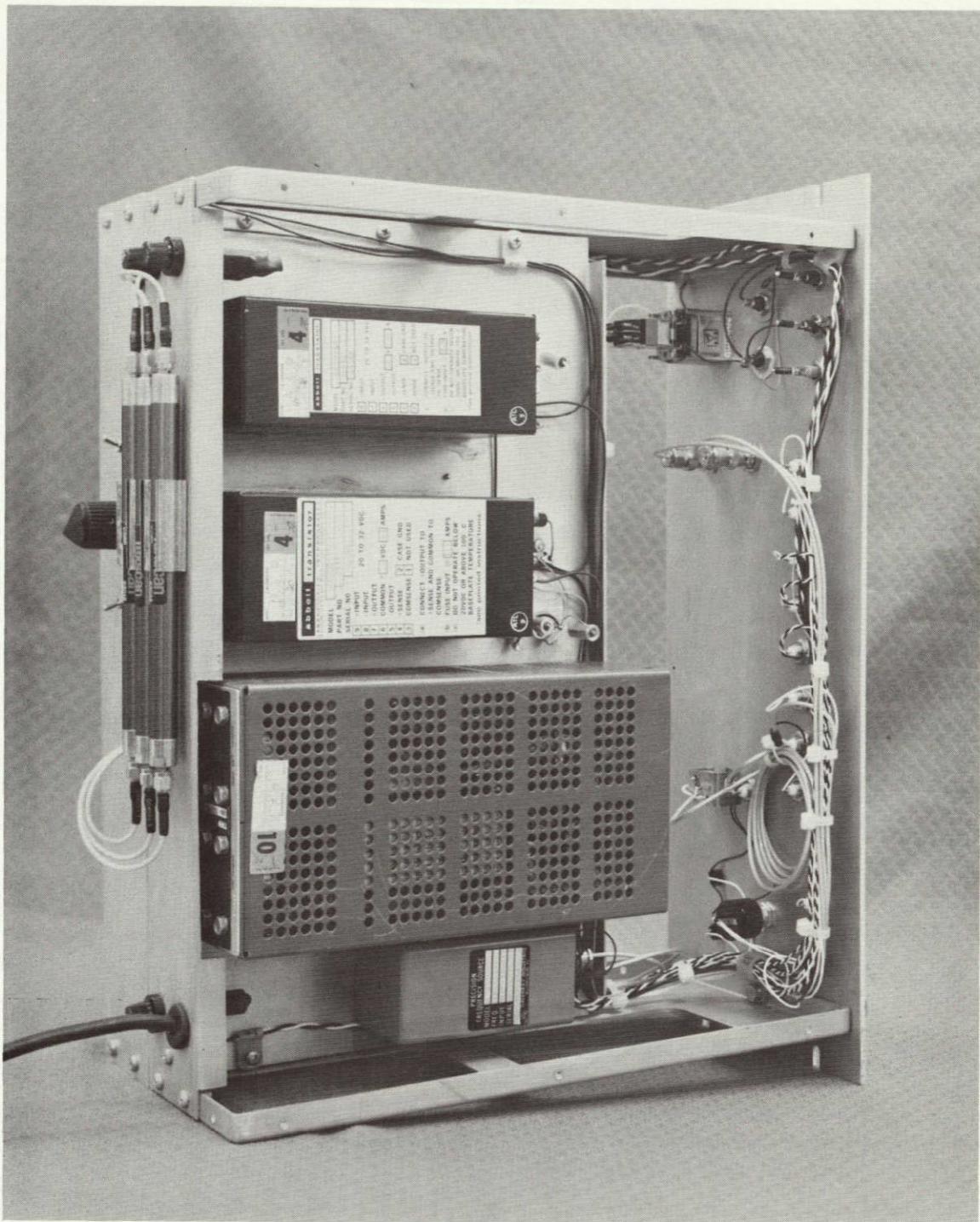
Figure 3-27.   Bottom View of Despreader Chassis

4. TEST SET

The despreader test set serves three basic functions:

1) It simulates a noisy received spread spectrum signal which has been downconverted to 110 MHz

2) It demodulates the despread signal which is produced by the despreader

3) It compares recovered data with the original data for bit error measurements.

Block diagrams for the two modes of operation are shown in Figure 4-1

Implicit to and associated with those basic functions are a myriad of capabilities, which make the test set suitable for simulating many spread spectrum communications problems — and therefore make the test set a useful piece of laboratory equipment. While the test set has already been described operationally (see Section 2), an understanding of the circuitry involved is both helpful for standard operation and necessary for extended experimentation. Figure 4-2 shows the despreader test set with covers removed.

4.1 72/216 KBPS DATA GENERATOR

To accurately analyze the spread spectrum communication problem simulated data is needed for transmission and recovery. Pseudorandon (PN) generators can provide suitable data streams. The randomness of the PN word provides a sequence of bits having nearly equal probabilities of being in either of the two data states with the use of a minimum amount of hardware, and the periodicity (PN word length) is selected to preclude the possibility of recovery circuits enhancing received data by means of "memory."

The 72/216 kbps data generator is a 10-bit shift register utilizing 4 and 11 feedback taps (thus producing a 1023-bit PN word). Originally designed for only 72 kbps operation, the data generator can produce the faster rate by simply changing the clock rate.
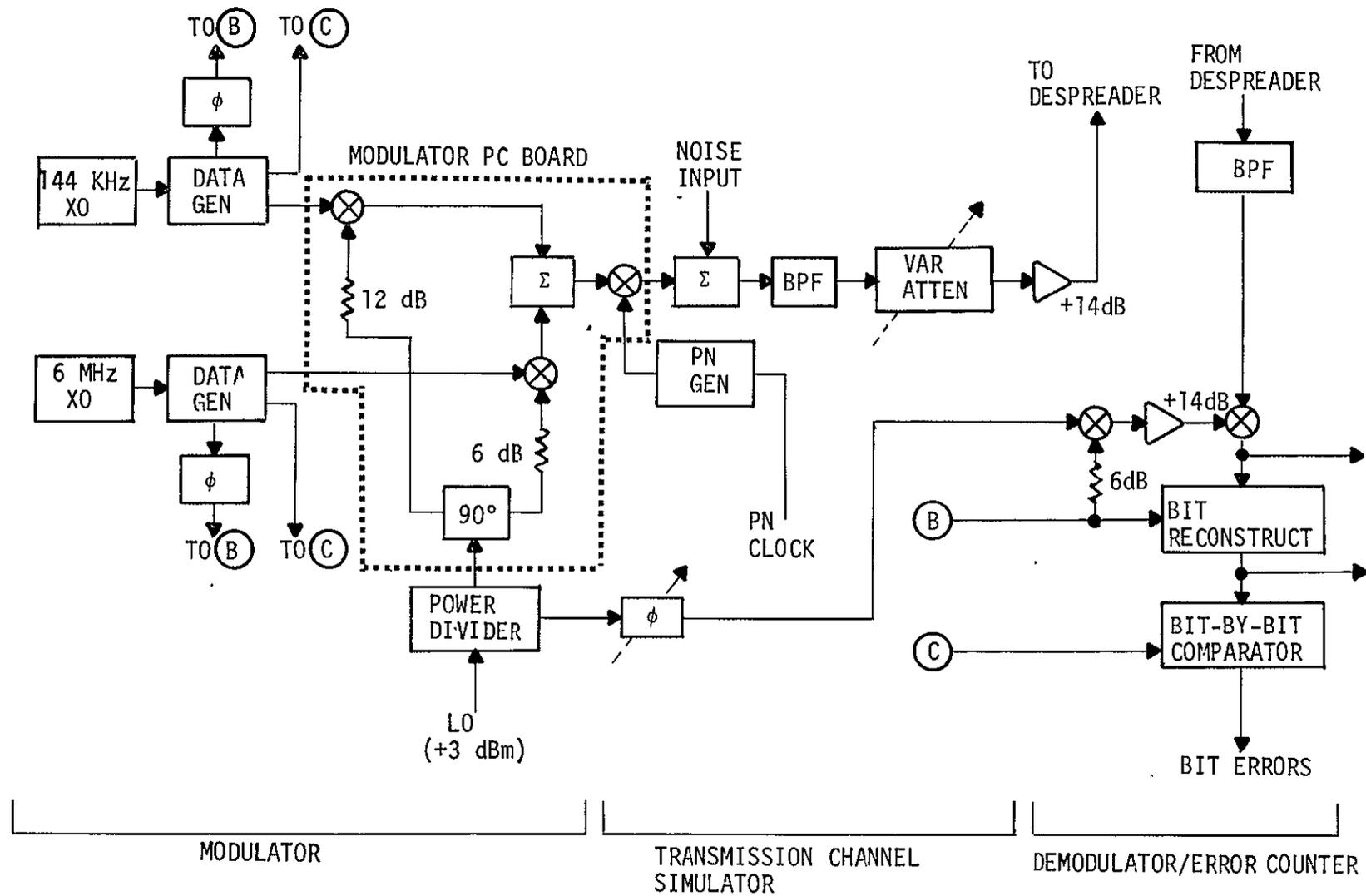
Figure 4-1. Test Set Block Diagram, UQPSK Mode
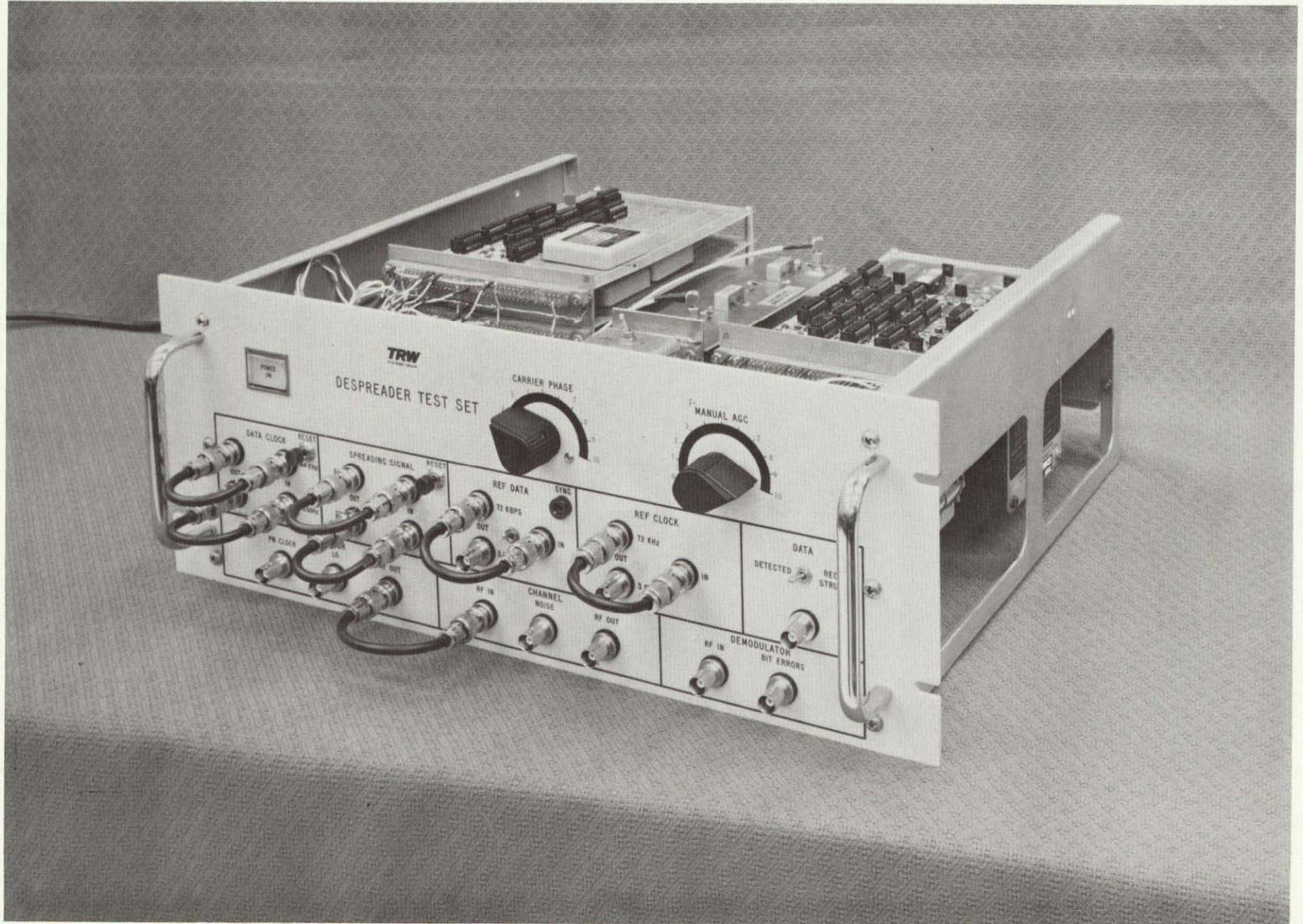
Figure 4-2. Despreader Test Set

Simple gating between the two data clocks is used for selecting either data rate, controlled by a mode selector switch on the test set rear panel.

The data generator schematic is shown in Figure 4-3. Twice the data rate is needed for a master oscillator frequency in the data generator, in order that a simple phase-shifting circuit could be implemented free of jitter. Hence two oscillators are found on the board, one producing a 144 kHz TTL output and the other providing 432 kHz. A flip-flop converts the oscillator frequency to the proper shift register clock.

The shift register has two auxilliary circuits. One is a sync detector circuit which fires a one-shot each time the PN word completes a cycle. This is necessary for triggering an oscilloscope if the data waveform is to be viewed. The other circuit initializes the shift register during turn-on and, thereafter, whenever the data reset button on the test set front panel is depressed. There is a forbidden state of the shift register (all 1s) which regenerates itself; the reset circuit places 0's in all bits of the register, from which the PN word can then be produced.

The data generator also has a phase-shifter which delays the data clock by an amount equal to the signal delay through the test set modulator circuits and through the despreader. The delayed clock is called REF CLOCK and is used to demodulate the received signal. A FET switch varies RC-constants of the phase-shifter in accordance with data rate selection.

The main outputs of the data generator are two sets of complimentary data. One set is the baseband data, Q_1 and $\overline{Q}_1$, also called REF DATA. The REF DATA is used for comparison with the recovered data. The other set of data, Q_2 and $\overline{Q}_2$ is Manchester coded (biphase-L) and is used to modulate the carrier to simulate a transmitter signal.
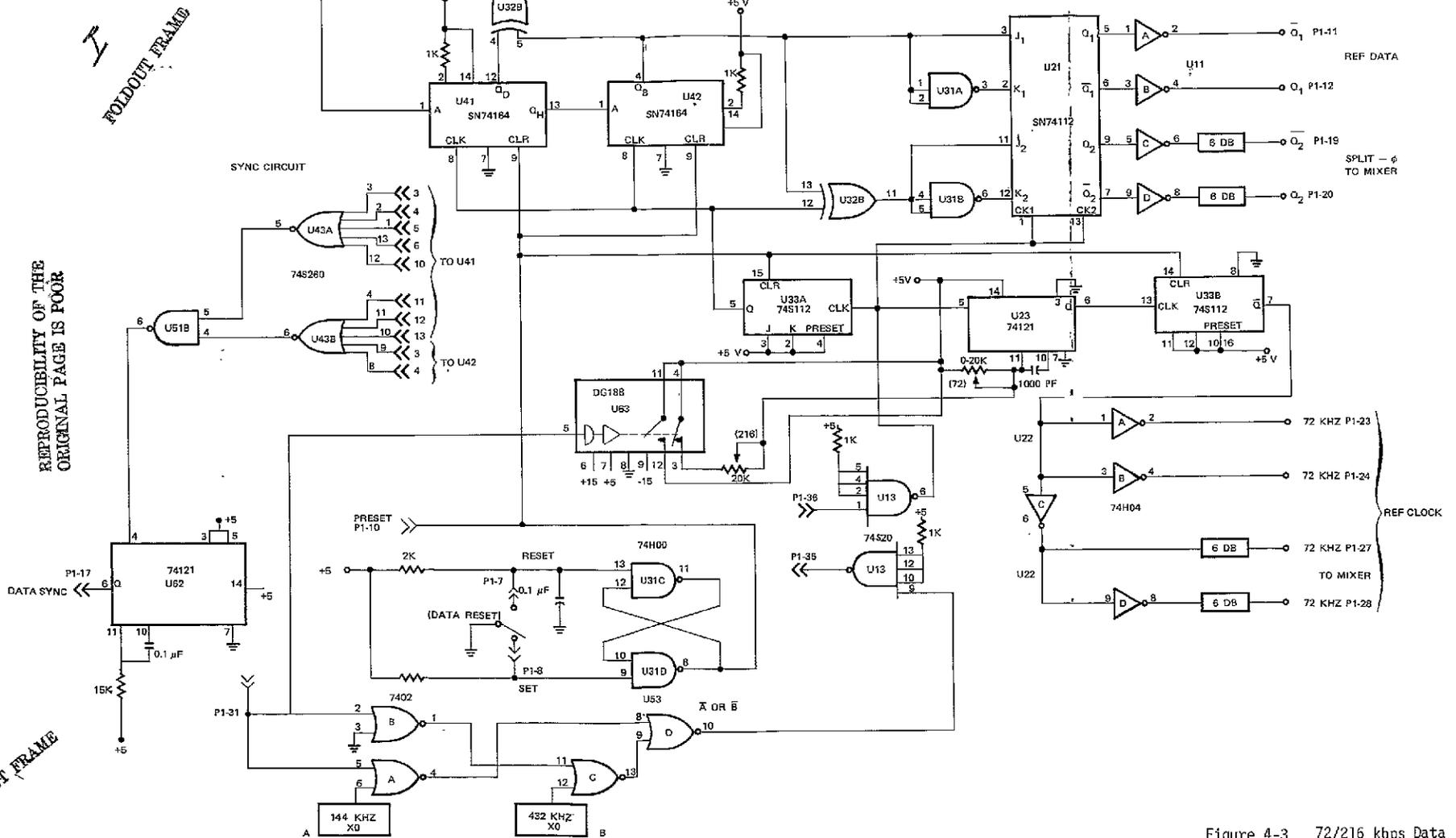
Figure 4-3. 72/216 kbps Data Generator

4.2 3 MBPS DATA GENERATOR

The 3 Mbps data generator is used only in the UQPSK mode. It consists of the same circuits as discussed above for the 72/216 kbps data generator, with only minor changes. A 13-bit shift register is used (9, 10, 12, and 13 feedback taps) in order that the two data rates of the UQPSK mode not have identical repetition rates. (Also note that the 11-bit spreading PN word has a length different from either data signal). The other differences between the high and low rate data generators are the master oscillator frequency (6 MHz in this case) and RC-time constants of the phase-shifter. The 3 Mbps data generator schematic is shown in Figure 4-4.

4.3 14.1 MCPS PN GENERATOR

The test set uses a third PN generator to produce the spreading code. Its design is basically the same as the two previously discussed. An 11-bit shift register with 9 and 11 feedback taps generates the 2047-bit word.

Since the spreading signal is simple NRZ, and also because there is no need for a delayed PN clock, there is little extra circuitry. Only sync and reset circuits are needed. The PN generator circuits are located on a board which also contains the bit reconstuct circuits. A schematic for the generator portion of that board is presented in Figure 4-5.

4.4 MODULATOR BOARDS

As was shown previously in Figure 4-1, two very different modulation schemes are used for the UQPSK and BPSK modes. Two different PC boards hold the components necessary to perform data modulation, level adjustment, and spread spectrum encoding. Layouts for the two boards are shown in Figure 4-6; the component connections are also indicated. The signal attenuation of the BPSK board makes possible the reduced C/N_0 values to be investigated for that mode. Figure 4-7 shows the test set with either board properly installed and connected for operation in the designated mode.
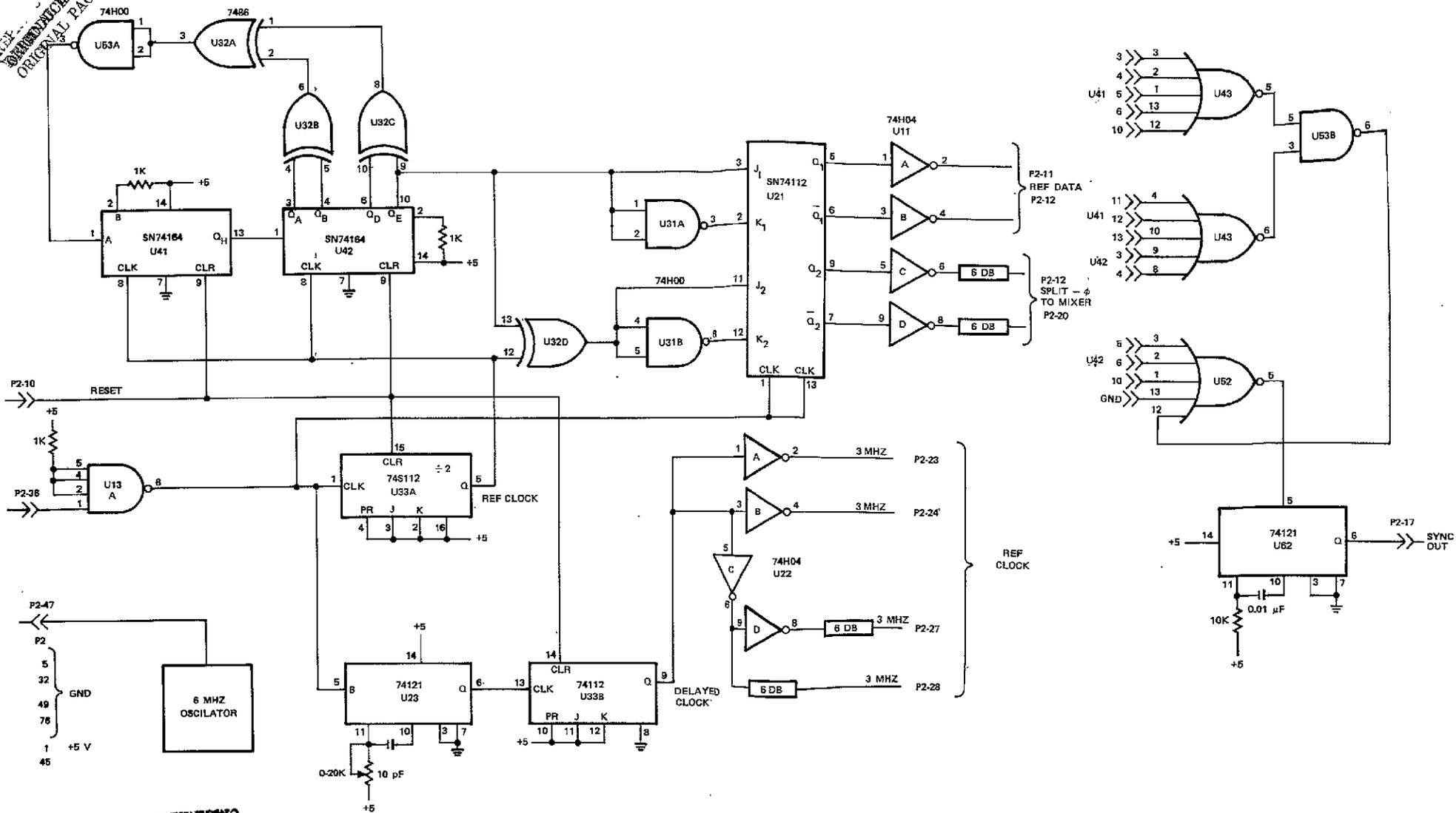
Figure 4-4. 3 MBPS Data Generator

4-7
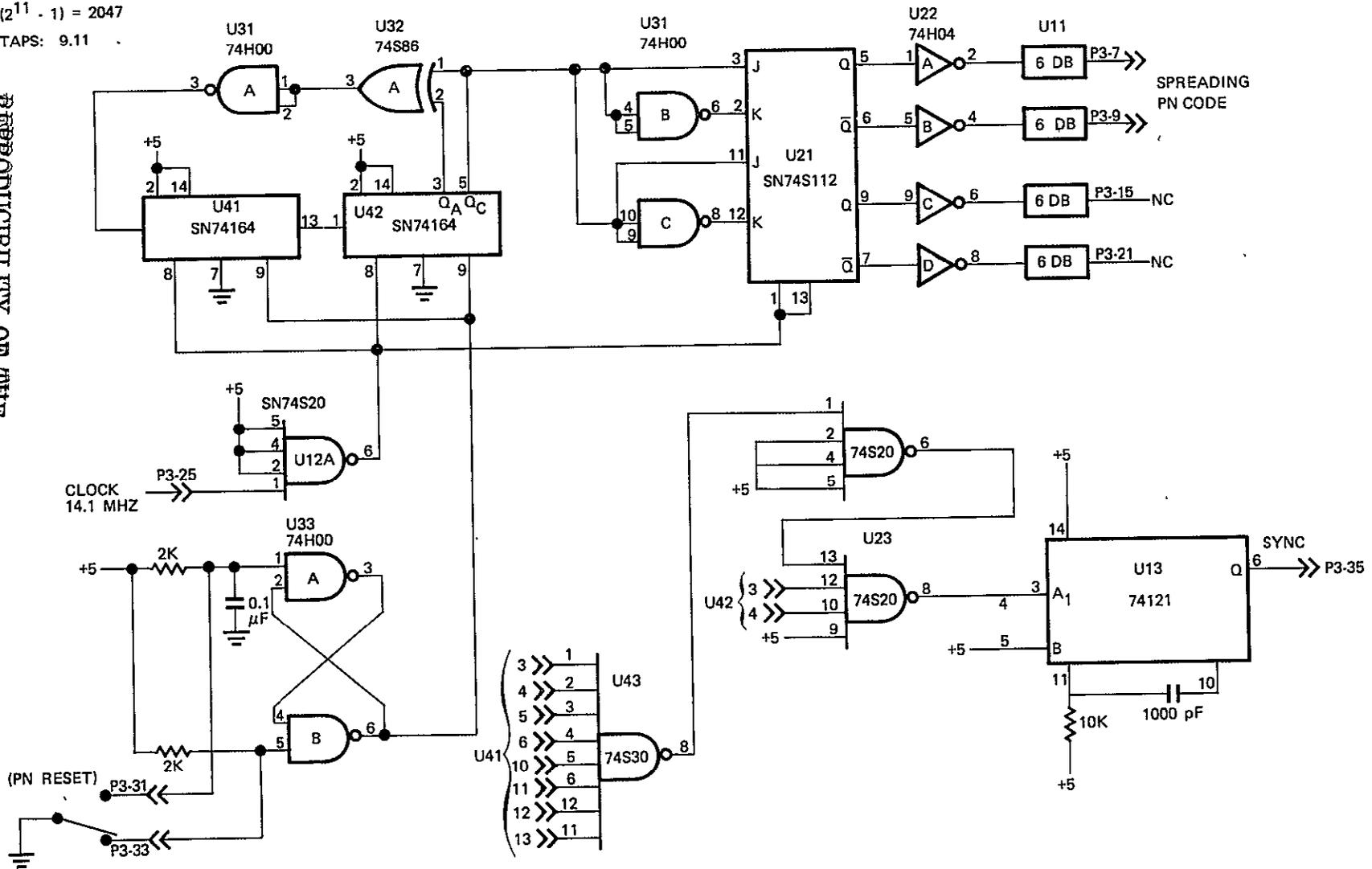
Figure 4-5. 14.1 Mcps PN Generator
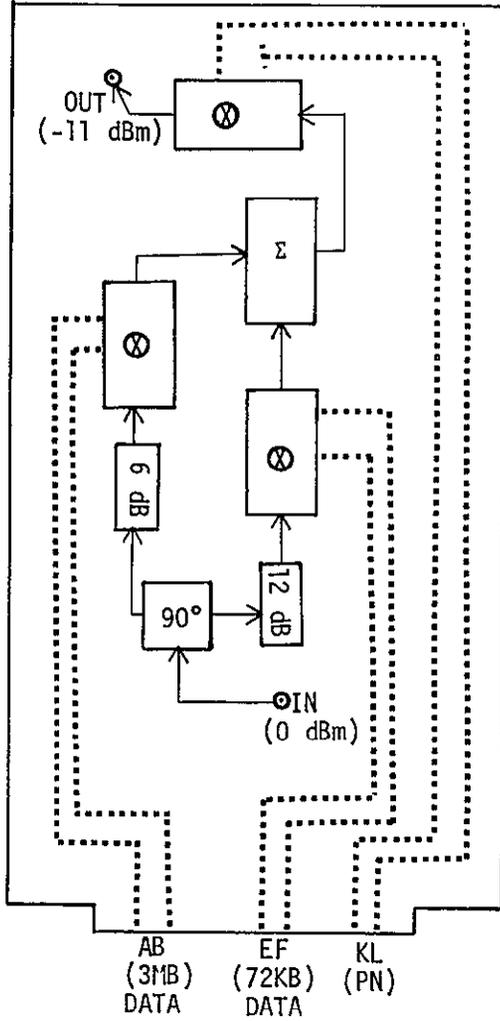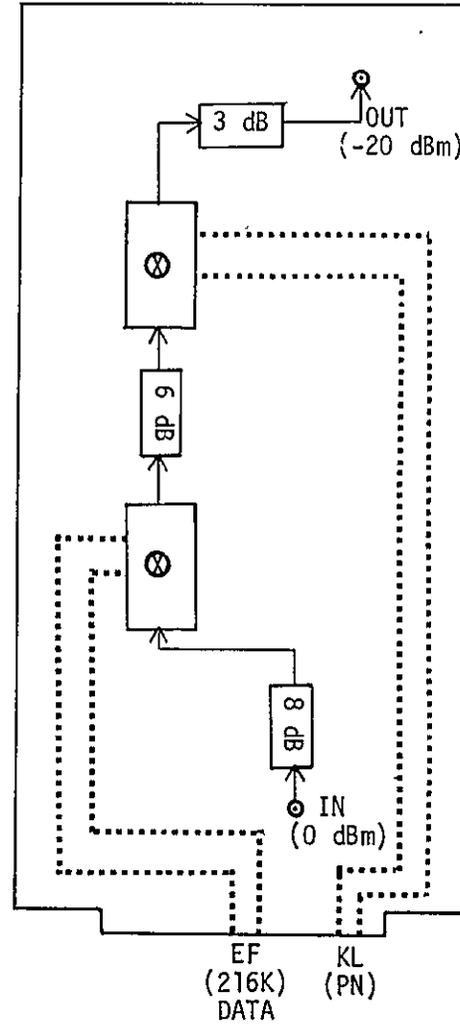
Figure 4-6. Test Set Modulator Boards
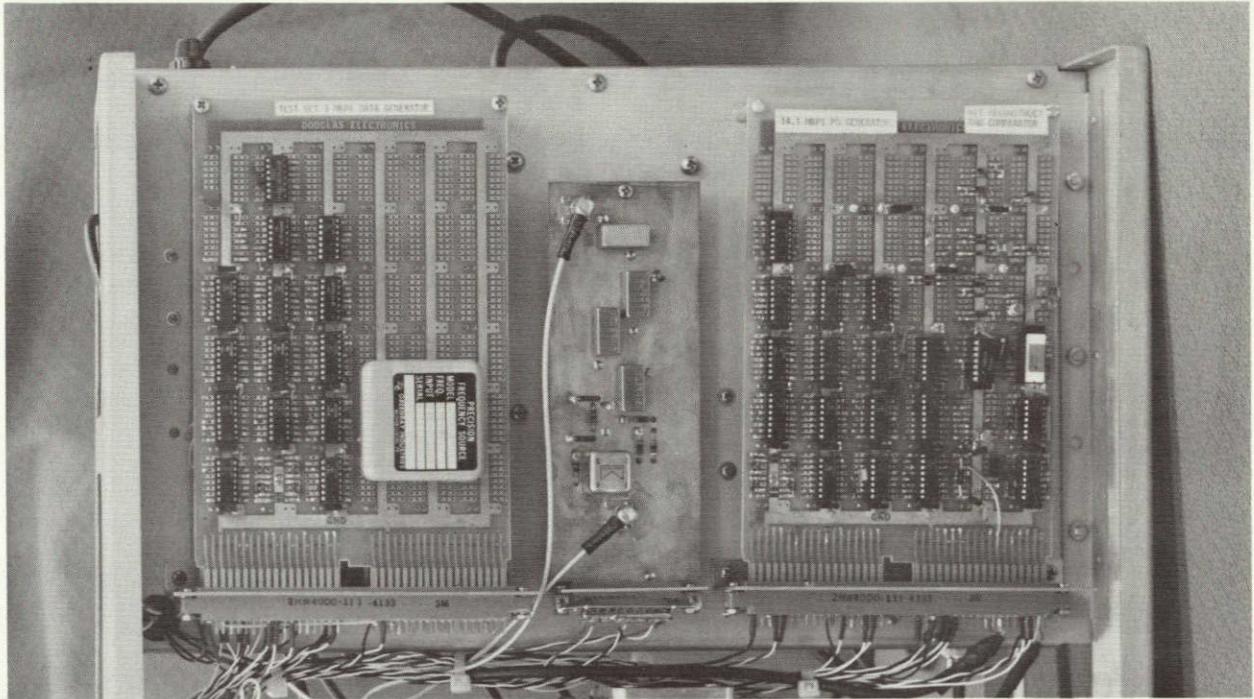
Figure 4-7a. UQPSK Modulator Board-In Situ
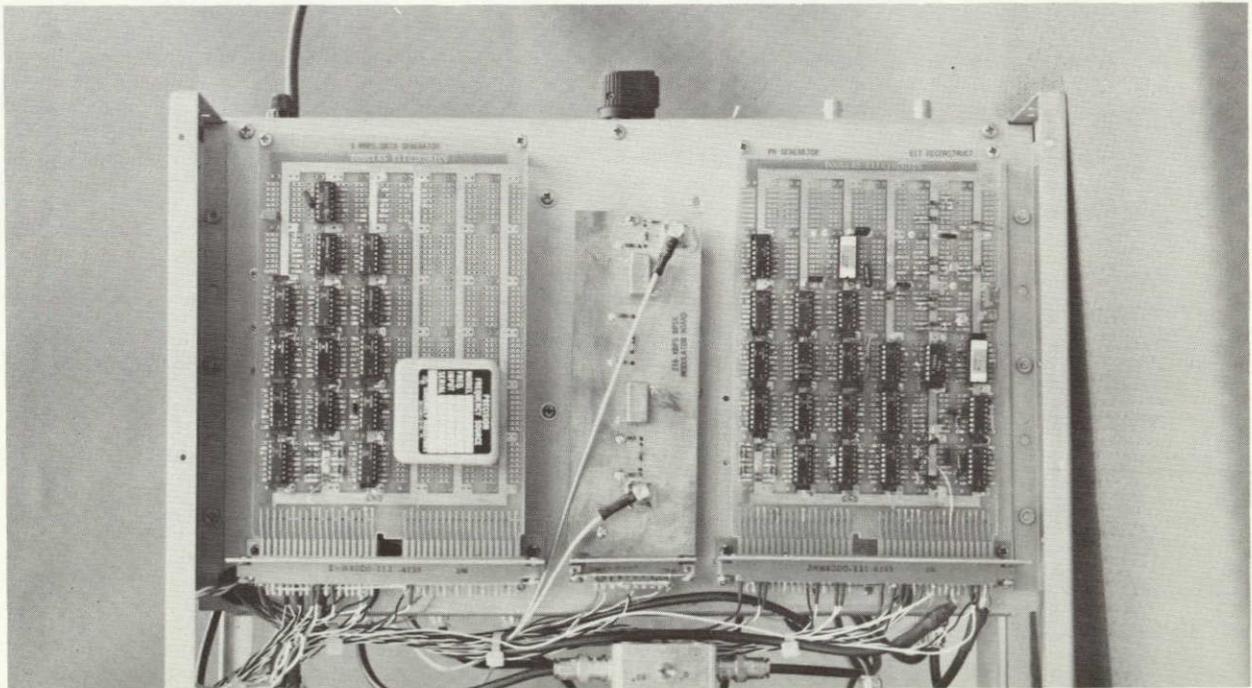
Figure 4-7b. BPSK Modulator Borad-In Situ

4.5 BIT RECONSTRUCT (AND ERROR DETECTOR)

After the despread signal is demodulated, the detected baseband data is processed in the bit reconstruct circuits (see Figure 4-8). Central to the reconstruction is an integrate-and dump circuit which match filters the data. The delayed clock (or REF CLOCK) signal is used to create the dump command. The integrator output drives a comparator, the output of which is reclocked to form the reconstructed data. (The comparator threshold can be adusted by either of the pots marked "72" or "3"). Due to delays in the circuits, the reference data is also reclocked. Figures 4-10 and 4-11 show typical data waveforms.

The two data streams are compared by an exclusive-OR gate to detect errors. This signal is AND-ed with the clock to create one pulse for each error (i.e., bit errors). The bit error signal is available at the test set front panel. Besides the integrator and other components just described, there are also FET switches on the board for changining the integrator time constant and the length of the dump pulse. There is also a TTL-to-bipolar level translator on the board which is used to decrease losses in the demodulator mixer that is driven by the REF CLOCK. Figure 4-9 shows the bit reconstruct and PN generator board.

4.6 TEST SET PANELS AND CHASSIS

Figures 4-12 and 4-13 show the front and rear panels of the test set. As the panel connections and controls were described in detail in Section 2, the pictures are included here for convenience and completeness.

A top view of the test set chassis (cover removed) is shown in Figure 4-14. The 3 Mbps data generator is visible on the left; the 72/216 kbps data generator is mounted beneath the 3 Mbps board. The locations of the modulator board and the bit reconstruct and PN generator board are clear in the figure also. The location of the PHASE CARRIER switch on the phase shifter mounted behind the front panel can also be seen.

FOLDOUT FRAME

4-12

Figure 4-8. Bit Reconstruct (and Error Detector)

P3-1, 45 >> +5 V
P3-54 >> +15 V
P3-56 >> -15 V

+5 V
+15 V
-15 V

5.1 V
200

BIT ERRORS >> P3-57
(NC) >> P3-55

74H00 U51
7486 U34

74109 U14
74109 U14

REFERENCE DATA >> P3-53

RECONSTRUCTED DATA >> P3-51

74109 U24

LM160 U35

RECEIVED SIGNAL >> P3-67

3.9K
3.3 V 1N746
3.3 V 1N746
56 pF
680 pF
0.1 µF
47 µF

DG190 U36
DG190 U53

"72"
5K
10K   10K
50K
+15   -15
+15 V -15 V

"1" ⇒ 72 KBPS OR 216 KBPS
"0" ⇒ 3 MBPS
P3-73

1K
+5

"1" ⇒ 216 KBPS
"0" ⇒ 72 KBPS
P3-61

680 pF
9.1K
+5

10 pF
74121 U26
A1 A2

74121 U16
A1 A2

100 pF
3K   5.1K
+5

REFERENCE CLOCK >> P3-75

SD212
SD305
390
+5
-5 V
38
3.6 V
1N3604
200
27
560
+15
-15 V

REFERENCE CLOCK (TO MIXER) >> P3-73
1N751
180
16
150
51
2N2369
1N543 1N543
100
+5

FOLDOUT FRAME

Figure 4-9. Bit Reconstruct and PN Generator Board

0.2 V/DIV

3 V/DIV
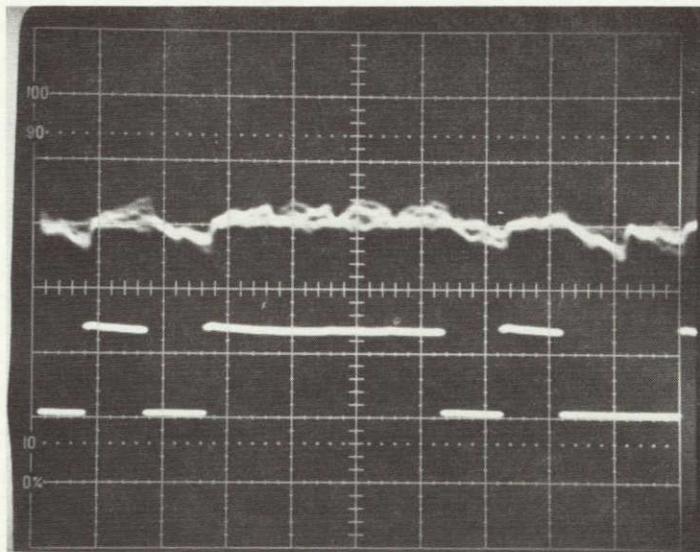
a.

INTEGRATOR
OUTPUT
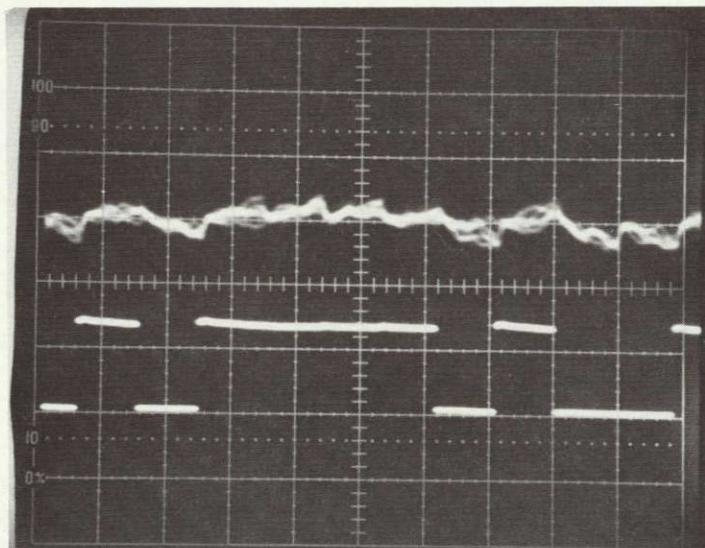
RECONSTRUCTED
DATA

HOR: 5 μsec/DIV

0.2 V/DIV

3 V/DIV

b.

INTEGRATOR
OUTPUT

REFERENCE
DATA

Figure 4-10. Data Reconstruction (-15 dB SNR)

0.2 V/DIV

3 V/DIV
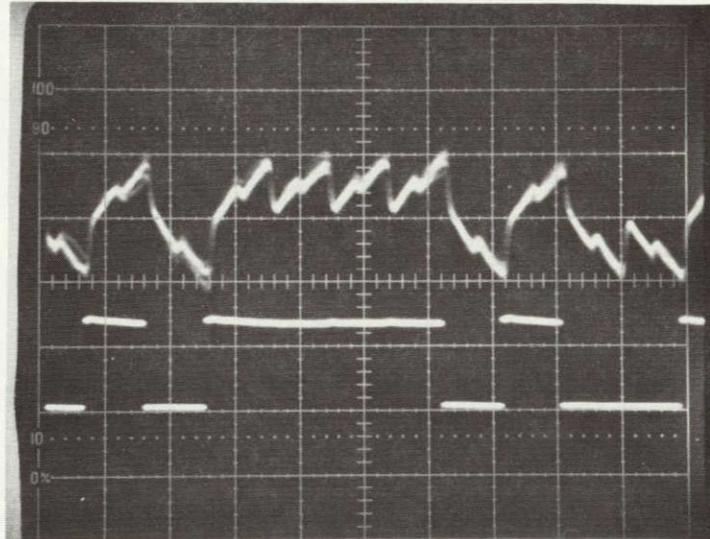
a.

INTEGRATOR OUTPUT

RECONSTRUCTED DATA

HOR: 5 µsec/DIV

0.2 V/DIV

3 V/DIV

b.
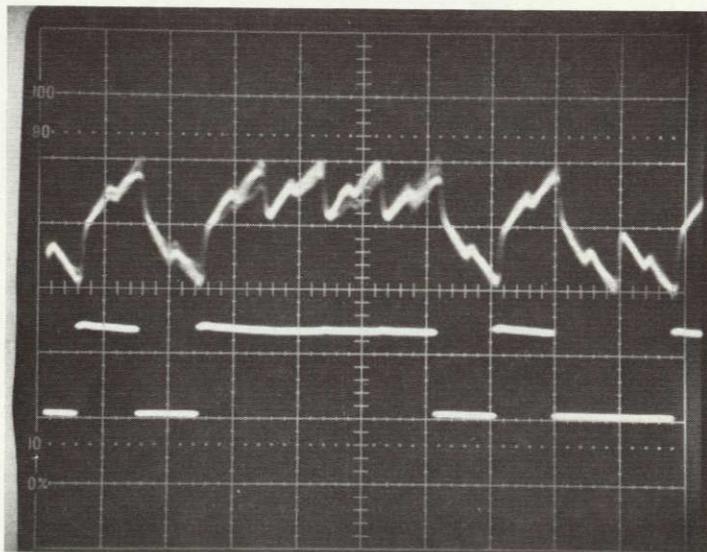
INTEGRATOR OUTPUT

REFERENCE DATA

Figure 4-11. Data Reconstruction (0 dB SNR)
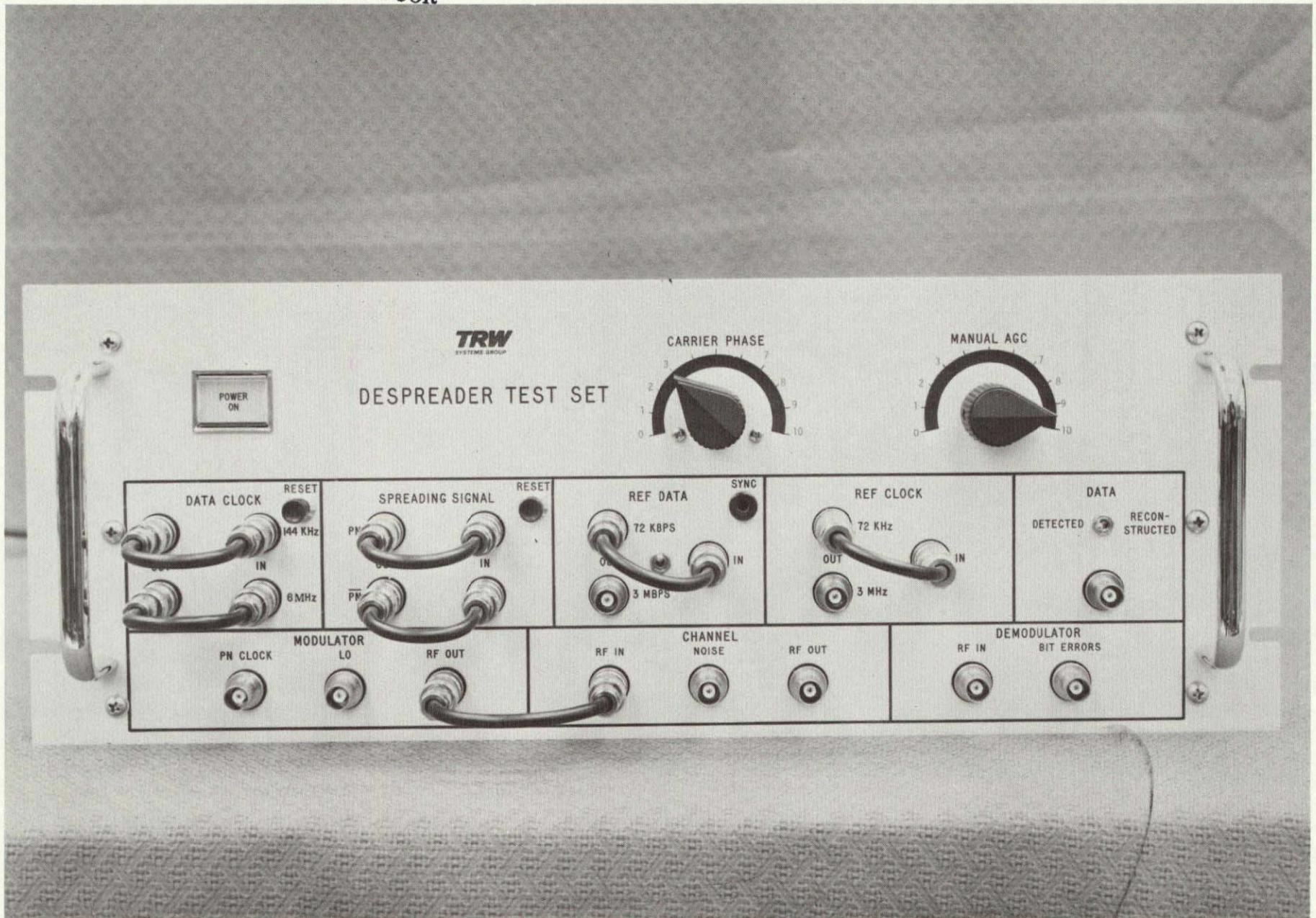
Figure 4-12. Test Set Front Panel
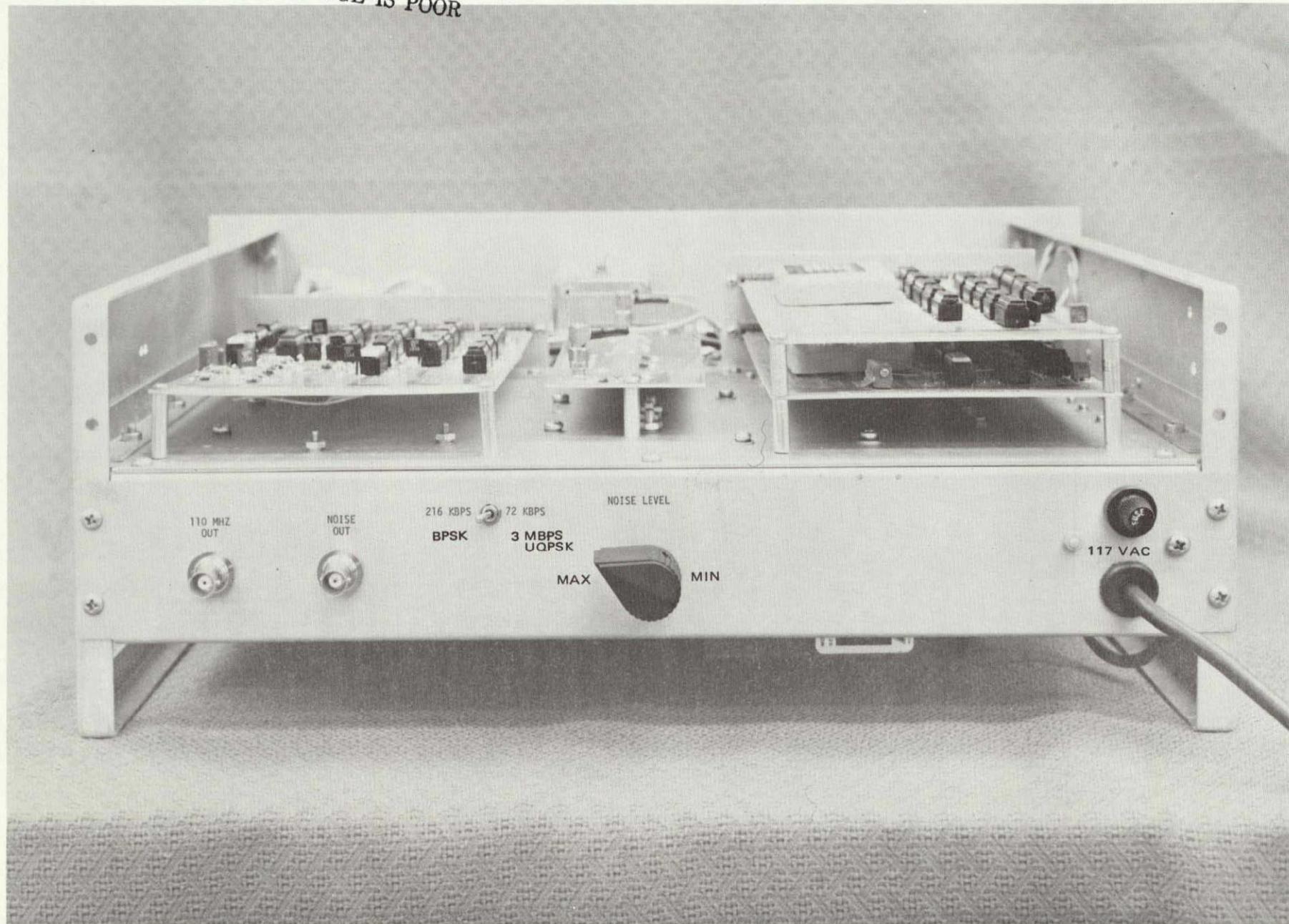
Figure 4-13. Test Set Rear Panel
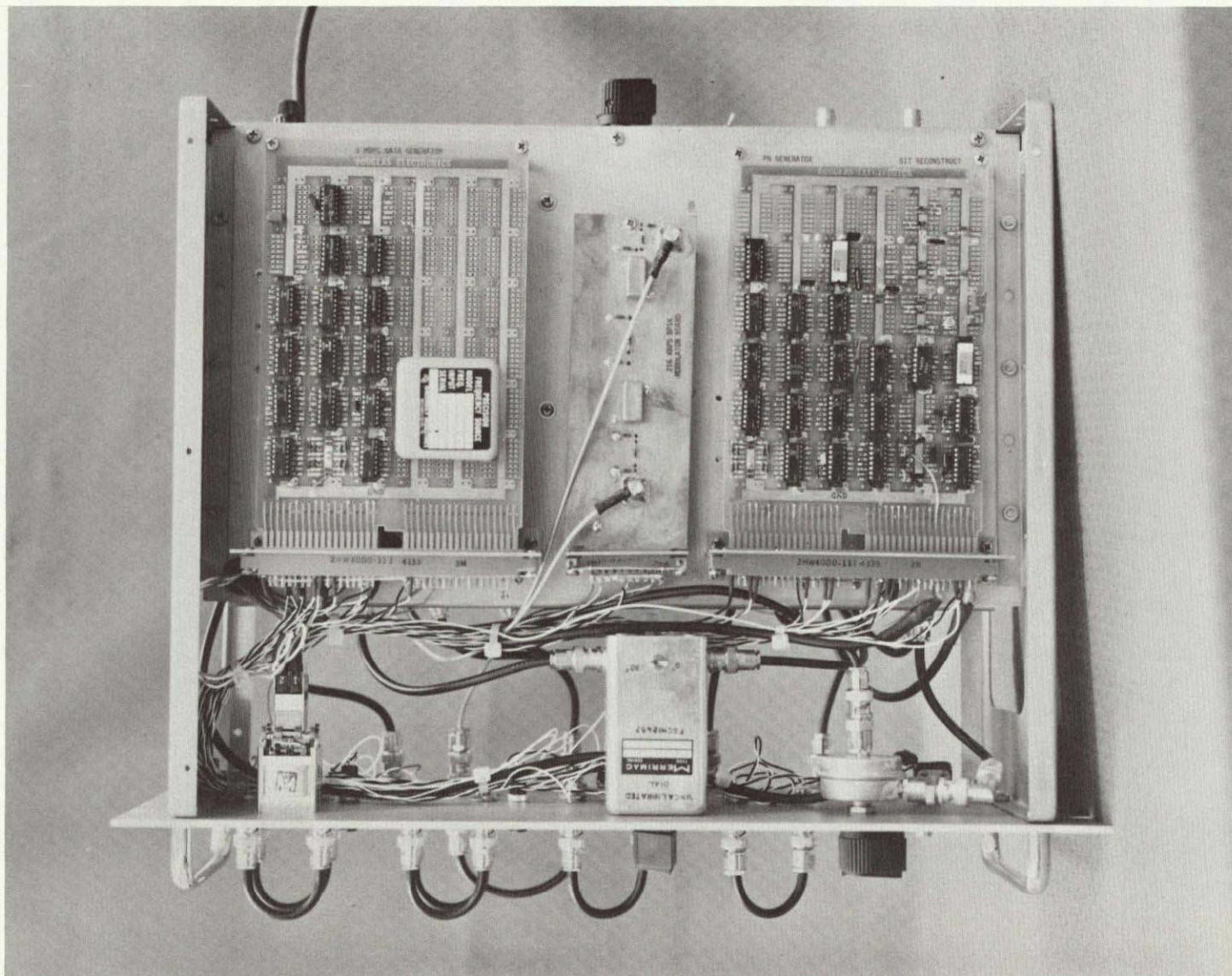
Figure 4-14. Top View of Test Set Chassis

Several important components can be seen in Figure 4-15, a bottom view of the test set. Located next to the rear panel (upper-right in photo) is a 110 MHz crystal oscillator. This oscillator puts out +3 dBm, providing a suitable signal for the LO input to the test set. An external source, however, must be used to simulate Doppler because the oscillator is not tunable.

Another input signal for the test set is also available at the rear panel. Wideband noise centered at 110 MHz is needed to create the required C/N_0 values. This is accomplished with four amplifiers which together provide 88 dB of gain (see Figure 4-16). Thermal noise (from a resistive load) is amplified 41 dB, and then filtered to a 35 MHz bandwidth. Filtering is necessary to prevent saturation of the wideband (500 MHz) amplifiers used. After filtering, the noise is amplified another 47 dB, level adjusted in a variable attenuator, and brought to the rear panel. Figure 4-16c shows the output signal frequency spectrum.

It is important to point out the location of the data bandwidth filters on the bottom of the test set chassis, since it is necessary to switch the cables from one to the other when changing operational modes (BPSK and UQPSK). While the bank of tubular filters can be seen in Figure 4-15, Figure 4-17 presents a better angle of view. The two top filters are the test set input filters being discussed. The photo shows the middle filter, a 2.0 MHz filter, connected; this is for BPSK operation. The BNC cables must be removed from the middle filter and connected to the top filter (12 MHz wide) for the UQPSK mode.

A final item to be pointed out in Figure 4-15 is a small box in the lower right corner of the chassis which contains two amplifiers. A schematic for that box is given in Figure 4-18. The demodulated data is input to the amplifiers. One output is a signal 40 dB stronger, which goes to the integrate-and-dump circuit. The other output is simply buffered in a unity-gain amplifier and connected to the DETECTED DATA output on the test set front panel.
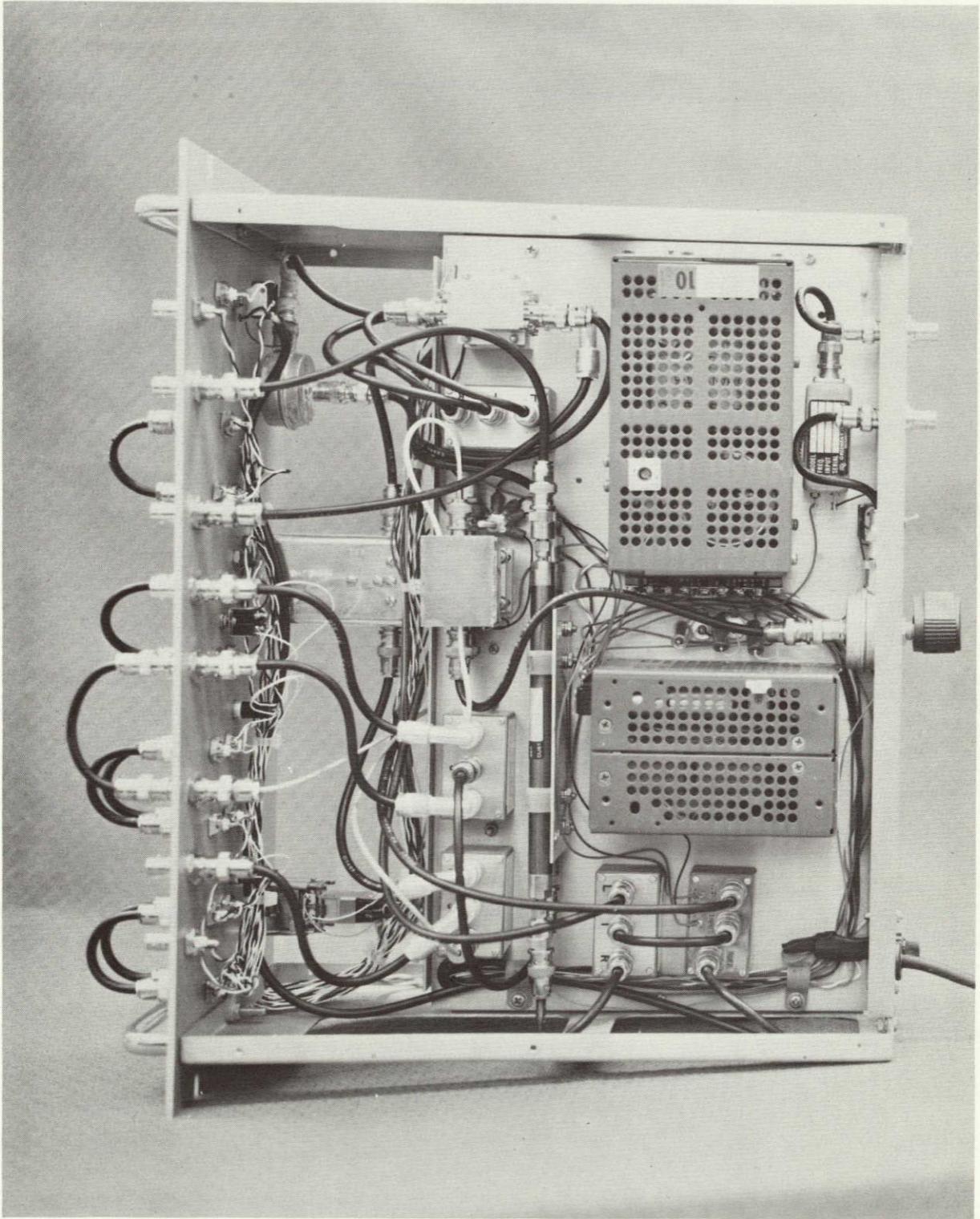
Figure 4-15. Bottom of Test Set Chassis
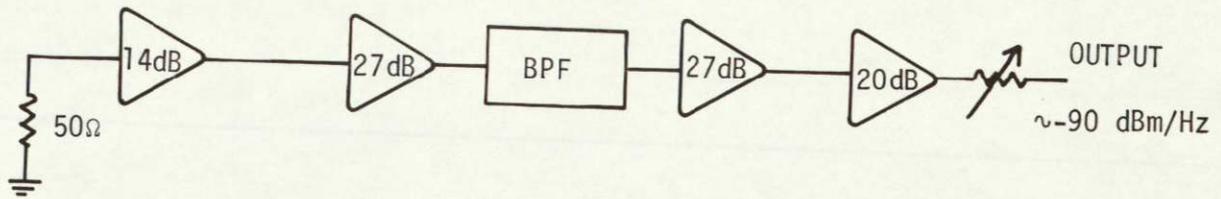
Figure 4-16a. Schematic
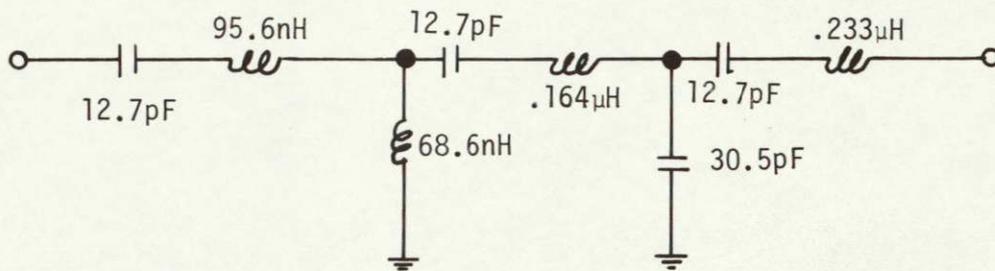
Figure 4-16b. Filter Design
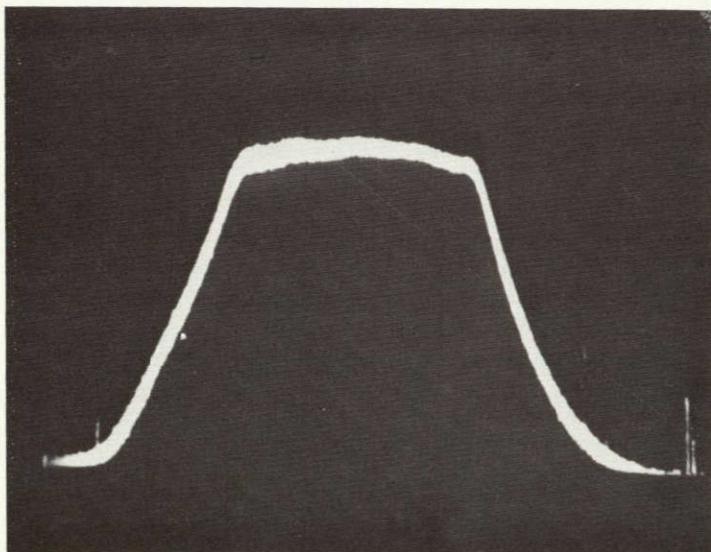
Vert: 10 dB/div
Hor: 10 MHz/div

Log Ref Level: -30 dBm
Center Freq: 110 MHz

Figure 4-16c. Measured Output

4-21
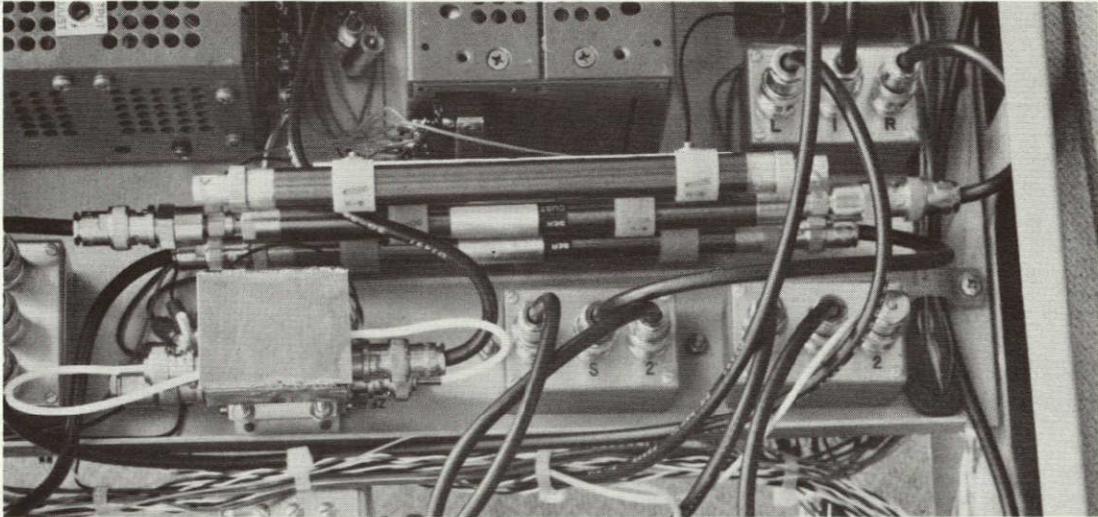
Figure 4-17. Data Bandwidth Filters
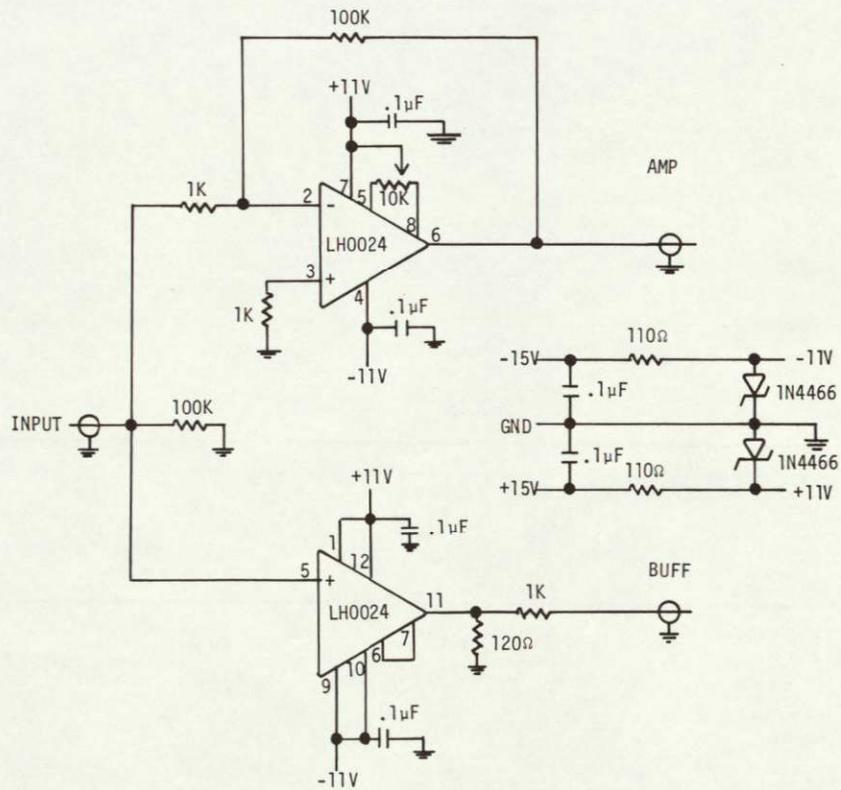
Figure 4-18. Detected Data Amplifier and Buffer

4-22

5. ACCEPTANCE TEST PROCEDURE

In keeping with the requirements of the Ku-Band Shuttle spectrum despreader contract, and to ensure that the completed despreader will meet the required specification, the following tests will be performed in the course of breadboard checkout and during acceptance testing. Five tests are required to ensure proper operation of the delivered hardware; three relate to proper operation of the test set, and two to the despreader meeting RFP specifications of acquisition time and degradation introduced by the despreader.

These tests are presented in a brief form where the underlying assumption has been made, that the operator shall be familiar with standard testing procedures, and basic operation of the two delivered units and supporting laboratory equipment. The instructions provide information for making necessary changes from the normal operating configuration of support equipments and interconnections (see Figure 5-1). A cumulative list of test equipment suitable for performing all tests is provided in Table 5-1. Substitutions and deletions are possible.

Performance of these tests in their given sequence is important in that proper evaluation of a module or section being tested is dependent upon previous modules having been proven operational and/or calibrated as noted. Sections A and B (the test procedures for the 72 kbps/3 Mbps UQPSK modem and the 216 kbps BPSK modem, respectively) can be performed independently of each other. Alternations for standard operation in the selected mode are assumed (see Section 2).
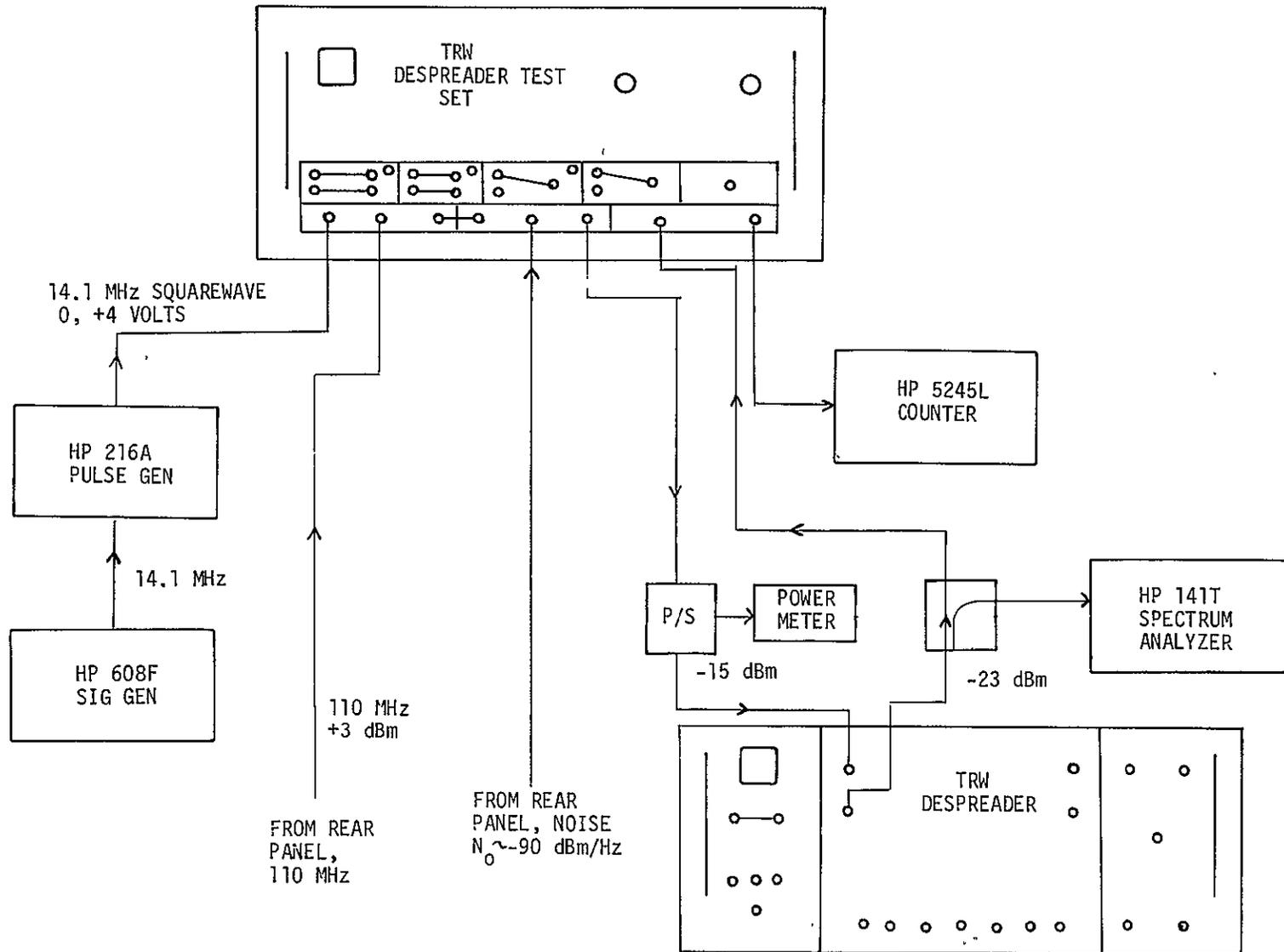
Figure 5-1. Normal Operating Configuration and Interconnections

5.1 72 KBPS/3 MBPS UQPSK MODEM

Test No. 1: Test Set UQPSK Modulator

Objective: To verify operation of the test set modulation

Procedure: Refer to Figure 5-1 for initial connections

1) Disconnect the cable on the test set front panel going
between MODULATOR RF OUT and CHANNEL RF IN.

2) Connect the HP141T spectrum analyzer to MODULATOR RF
OUT.

3) Disconnect input to MODULATOR PN CLOCK.

4) Disconnect the 144 kHz DATA CLOCK OUT from DATA CLOCK IN.

5) Observe the frequency spectrum which should appear as
shown in Figure 5-2 for the analyzer settings shown. Note
that the nulls occur at ±6 MHz and that there is a spike
at 110 MHz which is 16.8 dB higher than the first peaks
of the spectrum.

6) Reconnect the 144 kHz DATA CLOCK OUT and DATA CLOCK IN and
then disconnect the 6 MHZ DATA CLOCK OUT from the DATA
CLOCK IN.   _____

7) Again observe the spectrum, this time as pictured in
Figure 5-3. Note the nulls are now at ±144 kHz, and
there is a 27.4 dB spike at the center frequency.

8) Disconnect the 144 kHz DATA CLOCK and provide the pro-
per 14.1 MHz input to the MODULATOR PN CLOCK.

9) The spectrum should now appear as in Figure 5-4, with
nulls at ±14.1 MHz.

10) Disconnect the MODULATOR PN CLOCK. Connect the HP8407
network analyzer to the MODULATOR RF OUT instead of the
spectrum analyzer. (Be sure to use the 8601 sweeper for
110 MHz input to the MODULATOR LO, and connect the
sweeper's VCO output to the analyzer). While a reference
is needed for operation of the network analyzer, an abso-
lute reference is not necessary for this test. Connect

Table 5-1. Capital Equipment Required for Despreader
Acceptance Tests

Model Number	Description	Manufacturer	Quantity
HP216A	Pulse Generator	Hewlett Packard	1 ·
HP5245L	Counter	Hewlett Packard	1
HP5262	Time Interval Plug-In	Hewlett Packard	1
HP562	Digital Recorder	Hewlett Packard	1
454A	Power Meter	General Microwave	1
585	Oscilloscope	Tektronix	1
HP141T	Spectrum Analyzer	Hewlett Packard	1
HP8554B	SA-RF Section	Hewlett Packard	1
HP8407	Network Analyzer	Hewlett Packard	1
HP8414A	NA-Polar Display	Hewlett Packard	1
HP8601A	Generator Sweeper	Hewlett Packard	1
HP3310	Function Generator	Hewlett Packard	1
MISC	50Ω Terminations	—	2-3
MISC	BNC Cables	—	10-15
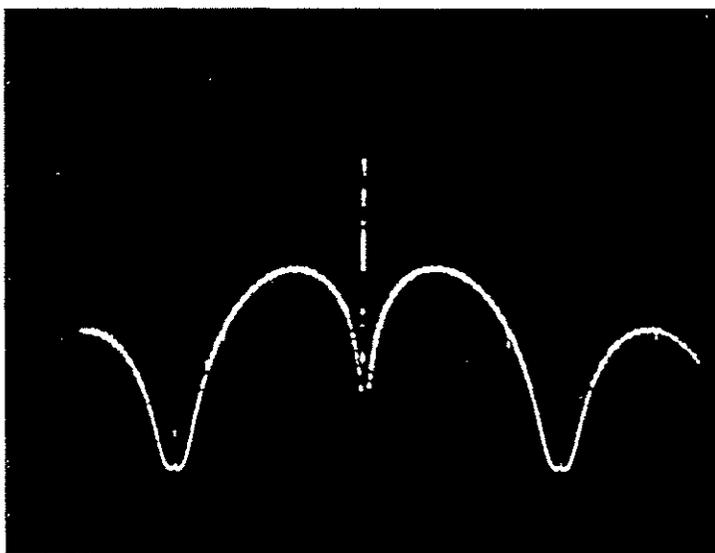
Analyzer Settings:

Vert: 10 dB/Div
Hor: 2 MHz/Div
BW: 30 kHz
Scan: 2 Sec/Div
Video: 100 Hz

Figure 5-2. High Data Rate Spectrum

5-4
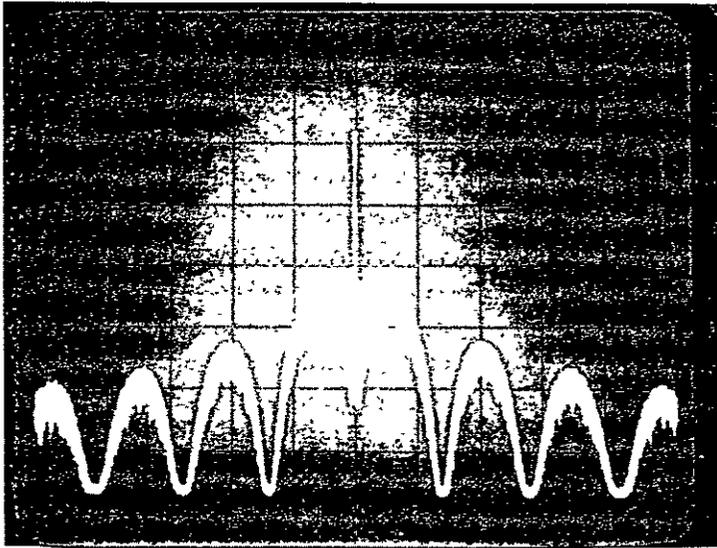
Analyzer Settings:

Vert: 10 dB/Div

Hor: 100 kHz/Div

BW: 1 kHz

Scan: 2 Sec/Div

Video: 100 Hz

Figure 5-3.   Low Data Rate Spectrum
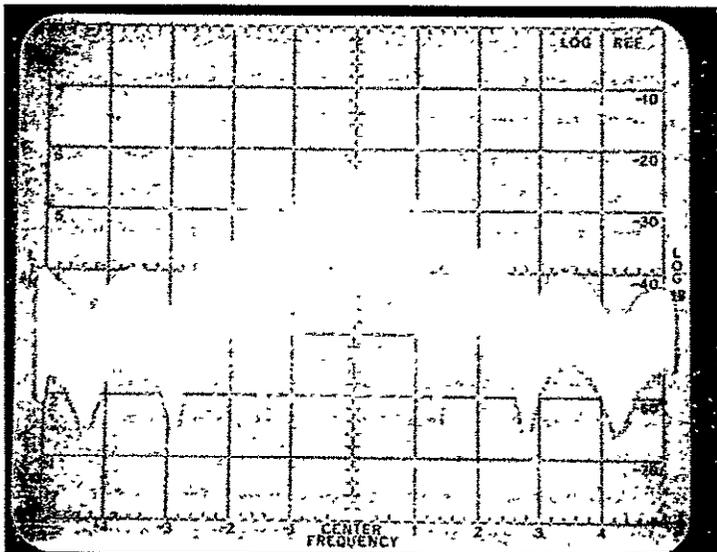
Analyzer Settings:

Vert: 10 dB/Div

Hor: 10 MHz/Div

BW: 10 kHz

Scan: 1 Sec/Div

Video: 10 kHz

Figure 5-4.   PN Code Spectrum

5-5

an external TTL source of approximately 300 Hz to both
DATA CLOCK inputs. (This is necessary because of limi-
tations in the network analyzer's frequency response).
Figure 5-5 shows the polar display output of the analyzer.
The figure should be a rectangle (sides at 90 degrees ±5
degrees with respect to each other) and there should be
a factor of two difference in the radial distances to
the sides. Note that because there was no phase zeroing,
there can be an arbitrary phase rotation of the figure on
the polar display.

Discussion. Manchester-coded data has a waveform as shown in Figures
5-2 and 5-3, with the position of the nulls determined by the data rate.
In the modulator section of the test set these spectra are translated to
110 MHz when the I and Q channels of the carrier are modulated by the data.
The orthogonality of the I and Q channels is checked with the network
analyzer.

Since biphase modulation is being used on two channels that should be
orthogonal to each other, the output should fall into one of four phase
states. These are the locations of the corners of the rectangle of Fig-
ure 5-5. The phase difference between the two channels is measured directly
as the angle between the sides of the figure on the polar display; i.e.,
nonorthogonal channels produce a nonrectangular parallelogram.
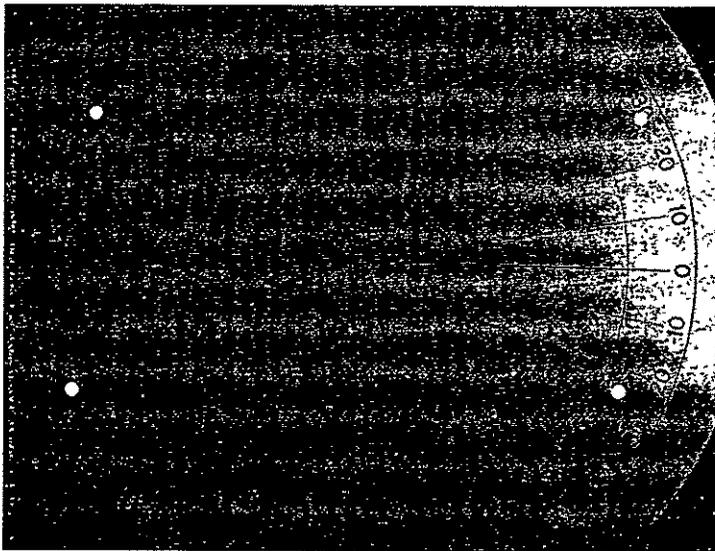
Analyzer Settings:

As Needed

Figure 5-5. Network Analyzer Polar Display

Furthermore, because this is an unbalanced QPSK system with one channel having 6 dB less power than the other, one can measure the power split between the two. The length of the long side of the rectangle should be two times the length of the short side. This is also verified by the spectrum figures; the carrier component of Figure 5-2 should have 6 dB more power than that of Figure 5-3.

Test No. 2: Signal Characteristics

Objective: To verify S+N/AGC Characteristics

Procedure: Refer to Figure 5-1 for initial connections

1) Terminate CHANNEL NOISE port, and measure power out of the CHANNEL RF OUT connection. (Use MANUAL AGC control to get roughly -18 dBm out).

2) Disconnect the MODULATOR RF OUT from the CHANNEL RF IN and terminate the CHANNEL RF IN port. Input sufficient noise power at CHANNEL NOISE to record same power out of CHANNEL RF OUT.

3) Reconnect CHANNEL RF IN to MODULATOR RF OUT. The output power will increase by 3 dB, verifying a 0 dB SNR.

4) Use MANUAL AGC control on panel to set the CHANNEL RF OUT power at -15 dBm for use with the despreader.

Discussion. The CHANNEL simulates a noisy communications transmission channel by summing noise with the spread spectrum signal. Signal-to-noise ratios are established by setting relative powers of the internal signal and external noise. The summed signal plus noise is then set at the proper level for despreader operation. Noise power is being measured in a 30 MHz bandwidth (filtering internal to the test set). This establishes the relationship that C/N_n (dB) = SNR (dB) + 75.

Test no. 3:   Receiver Performance

Objective: To verify proper receiver simulation and operation of
the bit synchronizer and test set

Procedure: Refer to Figure 5-1 for initial connections

1)   Disconnect 14.1 MHz MODULATOR PN CLOCK.

2)   Connect the test set CHANNEL RF OUT to the despreader
BY-PASS IN. Also, connect the despreader BY-PASS OUT
to the test set DEMODULATOR RF IN.

3)   Make proper REF DATA and REF CLOCK connections for 72 kbps
demodulation. (Be sure to put REF DATA switch in the 72
kbps position, also).

4)   Set CARRIER PHASE control for 8.0 with 0 degrees switch
position.

5)   Using a dual trace oscilloscope to monitor the data and
using the REF DATA SYNC output for external triggering
of the scope, monitor the REF DATA on the B channel of
the scope (using a tee connector at the test set panel).
Connect the A channel to the DATA output, monitoring
either DETECTED or RECONSTRUCTED data by switch selection.

6)   With a counter monitoring the DEMODULATOR BIT ERRORS output,
adjust the CARRIER PHASE control for minimum errors. (It
is helpful to temporarily use a higher level of noise for
this operation; -7 dB SNR is suitable). With the noise
again reduced for a 0 dB. SNR, the oscilloscope displays
of detected and reconstructed data will be as shown in
Figures 5-6 and 5-7.

7)   With no noise (amplitude into despreader adjusted accord-
ingly) no errors should be counted at the DEMODULATOR BIT
ERRORS output. Disconnecting the REF DATA IN cable should
yield 36,035 or 35,965 ±35 errors/second, about 50 percent.

8)   Repeat instructions 1 through 7 for the 3 Mbps data (see
Figures 5-8 and 5-9). Roughly 1,500,183 or 1,499,817
±100 errors/second should be counted when the REF DATA
is disconnected. Carrier phase should be 6.5 at 0
degrees.
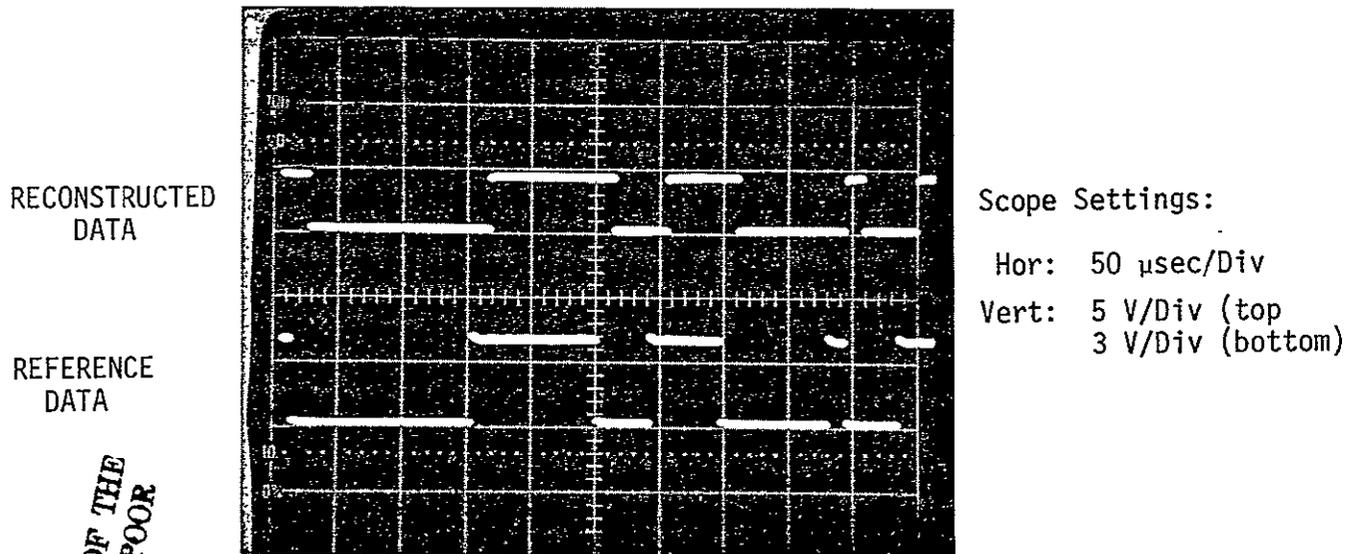
5-8

DETECTED
DATA

REFERENCE
DATA

Scope Settings:

Hor: 50 μsec/Div

Vert: 20 mV/Div (top)
3 V/Div (bottom)

Figure 5-6. 72 kbps Data

RECONSTRUCTED
DATA

REFERENCE
DATA

Scope Settings:

Hor: 50 μsec/Div

Vert: 5 V/Div (top
3 V/Div (bottom)

Figure 5-7. 72 kbps Data

DETECTED
DATA
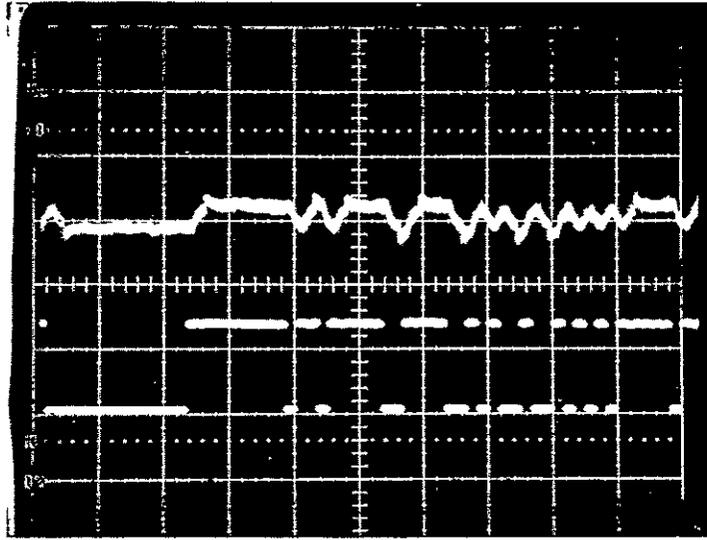
REFERENCE
DATA

Scope Settings:

Hor: 50 μsec/Div

Vert: 50 mV/Div (top)
3 V/Div (bottom)

Figure 5-8. 3 Mbps Data

RECONSTRUCTED
DATA

REFERENCE
DATA

Scope Settings:

Hor: 50 μsec/Div
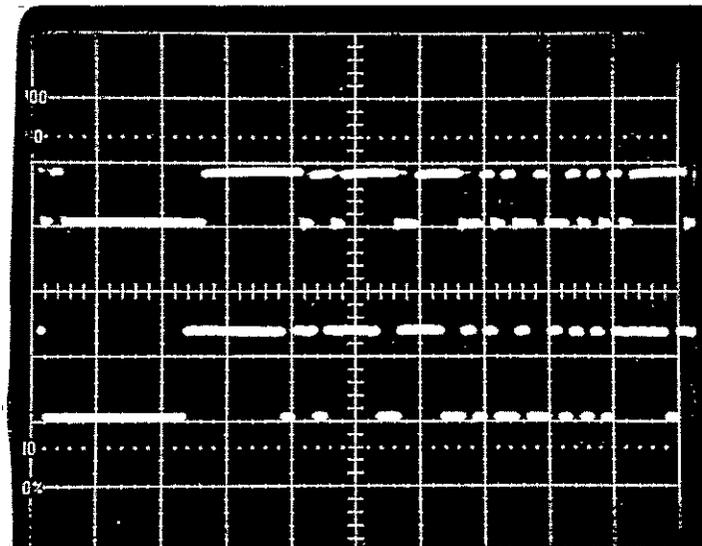
Vert: 5 V/Div (top)
3 V/Div (bottom)

Figure 5-9. 3 Mbps Data

Discussion. Disconnecting the PN code and by-passing the despreader eliminates spread spectrum techniques from the signal path. The demodulator works with one of the two data rates at a time, selected by cabling. With no noise added to the information, data should be recovered perfectly, with no resultant errors. When the REF DATA input is removed, the received data is compared with one state (either a "1" or a "0") always. Since the data is being generated by a PN generator the data consists of approximately 50 percent 1's and 50 percent 0's. Thus when the REF DATA input is removed about 50 percent errors should be counted.

The CARRIER PHASE ranges for the two data rates are 90 degrees apart, corresponding to the I and Q channels. The data demodulator requires extremely careful adjustment of the CARRIER PHASE. Any error results in degradation.

Test No. 4: Acquistion Tests

Objective: To verify average acquisition times of less than 10 seconds at C/N$_0$ of 68 dB-Hz to 126 dB-Hz

Procedure: Refer to Figure 5-1 for initial connections

1) Set desired SNR and Doppler simulation, maintaining a proper power level to the despreader.

2) Connect a time-interval counter to the CODE LOCK output of the despreader. Use the common start/stop function. Set start for -1 volt, negative-going edge, and set stop for -1 volt, positive-going edge.

3) Set the frequency of an HP3310 function generator to approximately 0.03 Hz, negative pulsed output, +5 to 0 volts. Check that over approximately a 30 second period the generator puts out +5 volts for 25 seconds and 0 volts for 5 seconds.

4) Connect the generator to the CODE RESET BNC input on the despreader panel.

5) Every 30 seconds the function generator will reset the despreader, forcing it to go into its initial acquisition routine. The reset command will start the time-interval counter. When the despreader locks or when the next reset command comes, the time measurement is ended. The number is displayed on the counter for 5 seconds as the despreader resets. The data can be recorded manually or automatically in this time period. One-hundred such measurements shall be made for each average time to be found. Of these, discard the 10 longest times and average the rest. This is the value $\overline{\dot{T}_{acq}}$.

6) The above steps 1 through 6 can be repeated for every combination of SNR and Doppler offset. A table of the form shown in Table 5-2 might be used. Additionally, average acquisition times for ± 1 dB AGC variations can be measured by simply changing the despreader input power to -14 or -16 dBm and repeating the above steps. Table 5-3 lists the data measured 29 April 1976.

Table 5-2. Data Summary for $\overline{T_{acq}}$ (sec)

C/N_0 ⟍ Doppler	68 dB-Hz	78 dB-Hz	126 dB-Hz
Max Positive Doppler	1.32	1.10	—
No Doppler	2.68	2.60	—
Max Negative Doppler	7.43	6.99	—

| AGC ⟍ C/N_0 Doppler | -1 dB | NOM | +1 dB |
	-16 dBm	-15 dBm	-14 dBm
68 dB-Hz No Doppler	2.40	2.68	2.50

Table 5-3. UQPSK T_{acq} Data (msec)

Maximum Negative Doppler, -7 dB SNR

0	0	0	6	8	5	0
0	0	0	8	7	7	3
0	0	0	9	4	3	1
0	0	0	8	4	0	5
0	0	0	7	0	2	0
0	0	1	6	7	3	3
0	0	1	5	8	2	2
0	0	0	9	7	0	0
0	0	0	7	9	6	1
0	0	1	6	5	3	6
0	0	0	7	8	9	1
0	0	0	7	4	3	4
0	0	0	6	0	9	7
0	0	0	7	7	0	4
0	0	0	6	7	9	0
0	0	0	5	5	7	7
0	0	0	7	8	3	5
0	0	1	7	1	1	0
0	0	0	7	8	6	8

0	0	0	6	5	9	1
0	0	0	8	0	5	9
0	0	1	5	5	9	6
0	0	0	5	8	9	7
0	0	0	7	3	3	4
0	0	0	9	1	0	1
0	0	0	6	5	8	4
0	0	0	6	2	0	6
0	0	0	8	5	9	8
0	0	0	8	7	9	7
0	0	0	8	0	7	5
0	0	0	8	3	2	0
0	0	0	7	0	2	2
0	0	0	6	7	7	7
0	0	0	6	7	3	0
0	0	0	7	3	3	8
0	0	0	9	2	6	2
0	0	0	7	9	3	1
0	0	0	3	3	5	7

0	0	1	0	9	3	8
0	0	0	7	5	1	5
0	0	0	6	3	5	3
0	0	0	7	4	3	3
0	0	0	7	4	5	4
0	0	0	6	6	1	9
0	0	0	5	3	9	5
0	0	1	5	7	7	8
0	0	0	9	7	2	2
0	0	0	8	1	0	8
0	0	0	7	4	5	4
0	0	0	5	6	0	4
0	0	0	8	2	8	0
0	0	0	7	2	8	0
0	0	0	5	2	8	5
0	0	0	5	9	0	3
0	0	0	5	5	9	1
0	0	1	1	5	7	1

Maximum Negative Doppler, 0 dB SNR

0	0	0	9	0	0	0
0	0	0	6	9	9	2
0	0	0	9	5	0	3
0	0	0	5	2	8	1
0	0	0	6	6	5	3
0	0	1	7	7	5	7
0	0	0	5	4	7	9
0	0	0	5	3	7	3

0	0	0	6	7	7	8
0	0	0	8	5	1	7
0	0	0	4	9	2	7
0	0	0	6	0	2	3
0	0	0	7	2	5	7
0	0	0	9	6	1	1
0	0	0	5	9	4	0
0	0	0	5	3	3	8

0	0	0	6	4	8	6
0	0	0	6	0	1	2
0	0	0	7	8	9	4
0	0	0	7	6	4	1
0	0	0	4	3	4	6
0	0	0	9	6	3	5
0	0	0	9	0	1	0

0 Doppler, 0 dB SNR

0	0	0	4	5	1	8
0	0	0	3	2	1	5
0	0	0	1	6	5	2
0	0	0	3	5	3	3
0	0	0	2	6	1	5
0	0	0	3	8	2	0
0	0	0	3	3	1	6

0	0	0	5	0	1	6
0	0	0	2	6	3	8
0	0	0	5	6	9	8
0	0	0	2	2	6	5
0	0	0	0	1	8	8
0	0	0	0	6	5	3
0	0	0	0	4	7	0

0	0	0	0	9	0	8
0	0	0	2	0	2	0
0	0	0	1	0	5	1
0	0	0	3	7	9	8
0	0	0	1	5	6	3
0	0	0	3	5	4	4
0	0	0	2	9	3	6
0	0	0	1	7	9	5

Table 5-3. UQPSK T_{acq} Data (msec) (Continued)

0 Doppler, -7 dB SNR		
0 0 0 2 0 5 9	0 0 0 1 7 1 2	0 0 0 2 0 2 4
0 0 0 2 6 9 8	0 0 0 3 0 9 2	0 0 0 3 9 5 8
0 0 0 1 6 3 9	0 0 0 4 1 3 8	0 0 0 1 1 0 6
0 0 0 1 7 4 4	0 0 0 1 5 0 9	0 0 0 3 1 4 0
0 0 0 2 8 1 4	0 0 0 1 0 0 5	0 0 0 2 8 3 7
0 0 0 2 2 5 1	0 0 0 3 9 1 8	0 0 0 4 4 0 7
0 0 0 2 7 1 1	0 0 0 4 1 4 3	0 0 0 0 8 5 7
0 0 0 3 0 9 7	0 0 0 5 0 2 1	0 0 0 5 7 3 7
0 0 0 5 0 9 0	0 0 0 4 0 7 5	0 0 0 4 2 2 6
0 0 0 5 3 6 2	0 0 0 3 7 4 3	0 0 0 0 1 3 5
0 0 0 2 6 0 4	0 0 0 3 6 6 4	0 0 0 1 9 3 3
0 0 0 1 1 9 3	0 0 0 0 3 5 5	0 0 0 1 2 0 0
0 0 0 0 1 0 5	0 0 0 3 5 3 7	0 0 0 0 6 7 3
0 0 0 0 1 2 2	0 0 0 3 4 8 5	0 0 0 1 8 0 4
0 0 0 3 2 3 3	0 0 0 1 2 3 2	0 0 0 0 7 6 3
0 0 0 2 3 4 6	0 0 0 3 1 0 3	0 0 0 7 1 6 2

Maximum Positive Doppler, -7 dB SNR		
0 0 0 3 0 4 3	0 0 0 0 6 2 4	0 0 0 4 3 2 0
0 0 0 0 8 4 0	0 0 0 4 1 4 5	0 0 0 2 4 9 1
0 0 0 0 8 0 1	0 0 0 1 0 3 5	0 0 0 0 6 9 4
0 0 0 1 5 6 7	0 0 0 2 8 3 2	0 0 0 1 2 9 3
0 0 0 1 7 1 6	0 0 0 1 4 1 8	0 0 0 0 6 2 5
0 0 0 6 8 7 0	0 0 0 2 4 0 9	0 0 0 0 0 7 3
0 0 0 0 6 5 3	0 0 0 0 3 2 8	0 0 0 0 3 0 0
0 0 0 0 5 3 4	0 0 0 1 2 6 6	0 0 0 0 7 3 3
0 0 0 0 7 7 0	0 0 0 0 4 4 9	0 0 0 0 4 0 8
0 0 0 1 1 0 8	0 0 0 0 6 6 7	0 0 0 2 0 2 3
0 0 0 0 4 2 6	0 0 0 1 8 1 8	0 0 0 0 1 3 7
0 0 0 1 9 5 1	0 0 0 1 4 5 0	0 0 0 1 9 1 2
0 0 0 1 3 2 3	0 0 0 0 2 4 0	0 0 0 0 3 9 3
0 0 0 0 5 2 3	0 0 0 2 1 8 6	0 0 0 1 1 6 3
0 0 0 0 5 7 7	0 0 0 1 3 1 1	0 0 0 1 1 0 8
0 0 0 0 7 5 2	0 0 0 0 5 1 2	0 0 0 0 4 5 0
		0 0 0 0 1 1 4

Maximum Positive Doppler, 0 dB SNR		
0 0 0 0 8 5 5	0 0 0 1 3 0 2	0 0 0 5 1 5 7
0 0 0 0 1 8 4	0 0 0 0 0 2 9	0 0 0 0 4 2 7
0 0 0 0 3 7 4	0 0 0 1 2 2 8	0 0 0 1 1 2 1
0 0 0 0 3 4 8	0 0 0 1 1 3 2	0 0 0 1 9 2 2
0 0 0 0 3 3 6	0 0 0 0 4 6 3	0 0 0 1 0 6 4
0 0 0 0 1 9 0	0 0 0 1 3 2 9	0 0 0 0 1 6 7
0 0 0 0 8 7 1	0 0 0 1 6 0 4	0 0 0 2 0 4 2
		0 0 0 0 9 5 7

Table 5-3. UQPSK T_{acq} Data (msec) (Continued)

-1 dB AGC		
0 0 0 4 9 8 8	0 0 0 3 4 9 4	0 0 0 1 0 9 0
0 0 0 3 2 6 4	0 0 0 1 6 5 9	0 0 0 4 3 7 0
0 0 0 6 4 1 1	0 0 0 1 3 4 0	0 0 0 6 6 3 0
0 0 0 4 4 4 1	0 0 0 0 1 9 5	0 0 0 3 0 3 8
0 0 0 1 3 3 7	0 0 0 4 1 3 8	0 0 0 0 0 6 3
0 0 0 2 2 2 0	0 0 0 0 1 7 8	0 0 0 4 3 0 2
0 0 0 0 2 8 7	0 0 0 3 4 2 5	0 0 0 0 3 2 3
0 0 0 1 0 1 1	0 0 0 1 9 9 6	0 0 0 0 0 1 1
0 0 0 0 4 6 0	0 0 0 0 3 5 4	0 .0 0 1 3 2 1
0 0 0 4 4 1 6		

+1 dB AGC		
0 0 0 3 0 4 1	0 0 0 2 3 4 3	0 0 0 0 9 9 8
0 0 0 5 7 7 1	0 0 0 2 9 3 1	0 0 0 1 3 3 4
0 0 1 1 2 7 7	0 0 0 1 8 9 6	0 0 0 3 6 3 2
0 0 0 0 1 3 1	0 0 0 5 1 4 1	0 0 0 0 0 5 4
0 0 0 1 0 4 2	0 0 0 4 3 8 2	0 0 0 4 1 0 6
0 0 0 1 0 8 7	0 0 0 0 3 4 9	0 0 0 1 1 7 1
0 0 0 0 9 8 7	0 0 0 2 3 9 0	0 0 0 2 4 8 4
0 0 0 3 5 5 2	0 0 0 0 6 1 7	0 0 0 0 8 7 2
0 0 0 0 0 3 7	0 0 0 3 5 1 6	0 0 0 1 5 6 1
0 0 0 2 3 1 1	0 0 0 6 5 6 1	0 0 0 1 3 8 7
0 0 0 5 5 7 7	0 0 0 6 0 8 8	0 0 0 2 3 4 0
0 0 0 3 3 9 9	0 0 0 1 2 9 9	0 0 0 3 4 6 5

Discussion. The CODE LOCK output is a tri-level signal indicating the three different states of acquisition: reset, search, and lock. Acquisition time is by definition the time from the end of reset to the beginning of lock. The automatic reset cycling forces an end to a given test if code lock has not been attained after 25 seconds of search time. This has been done to save time, since a 10 second average is required. It is quite suitable, however, to make automatic recycling slower or to switch to manual reset in the interest of obtaining statistical distributions, for example.

Test No. 5: Degradation Tests

Objective: To show that the despreader will not degrade the BER performance more than 1 dB

Procedure: Refer to Figure 5-1 for initial connections

1) Initialize the test set by repeating steps 1 through 6 of Test No. 3. During these tests, no external connection should be made to either unit, except for the counter.

2) Set up test set for C/N_o = 68 dB-Hz.

3) Measure BER.

4) Change C/N_o by 1 dB and repeat steps 2 and 3. Record BER and plot data as in Table 5-4 and Figure 5-10.

5) Reconnect 14.1 MHz MODULATOR PN CLOCK on the test set.

6) Connect despreader.

7) Repeat steps 2, 3 and 4 above, again using Table 5-4 and Figure 5-10, two curves should not be more than 1 dB plus spreading degradation apart at any point. To measure spreading degradation simply measure the power at the CHANNEL RF OUT port with the MODULATOR PN CLOCK both connected and disconnected. The difference should be about 0.1 dB yielding a 1.1 dB maximum spread between the two BER curves. A more complicated procedure was performed to isolate the effects of mixer leakage and excess filter loss due to despreading. The sum of these two factors is the reported 0.1 dB additional degradation.

8) Repeat steps 1 through 7 for 3 Mbps data demodulation, plotting another pair of curves as shown in Table 5-5 and Figure 5-11.

Discussion. A few guidelines should be established for practicality in making these measurements. First, in order to reasonably measure the number of errors occurring at any BER, a minimum of about 100 errors should be counted during a measurement. Therefore, a BER of 0.0001 was selected as the lowest rate to be measured since this value corresponds to about 7.2 errors/second and 300 errors/second at 72 kbps and 3 Mbps, respectively. The signal to noise will be degraded from the low BER starting point until minimum C/N_o (68 dB-Hz) is reached. Using these guidelines, note the small sample size of the measured 72 kbps error rate. This is due to a high E_b/N_o.

Very simply, the procedure outlined here first establishes a BER curve for the test set, without any spread spectrum techniques. Then the measurements are repeated, employing PN code spreading and despreading. The difference between the two curves less the signal loss caused by spreading the spectrum and filtering, is the degradation introduced by the despreader.

5-16
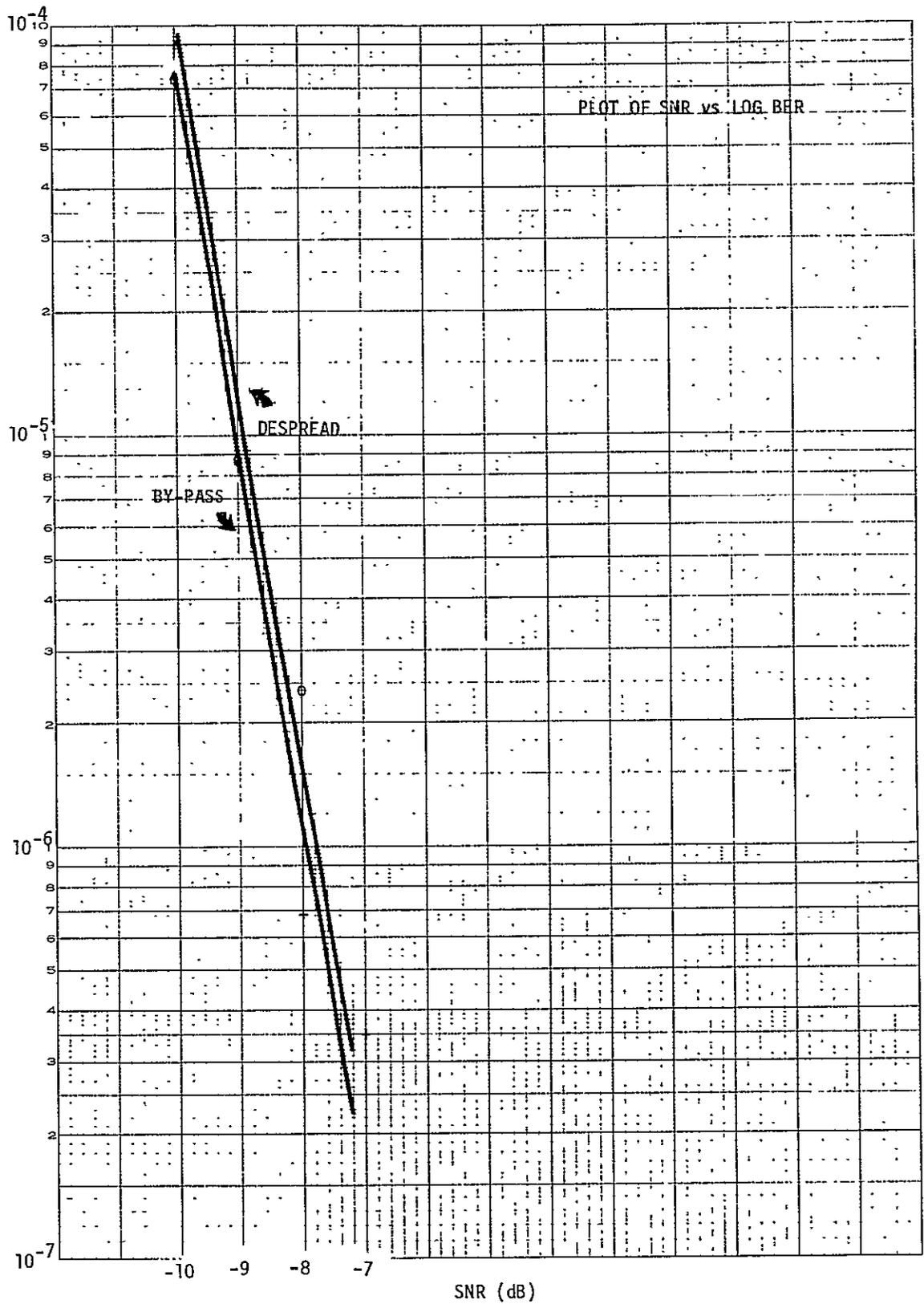
Figure 5-10. 72 kbps Error Degradation
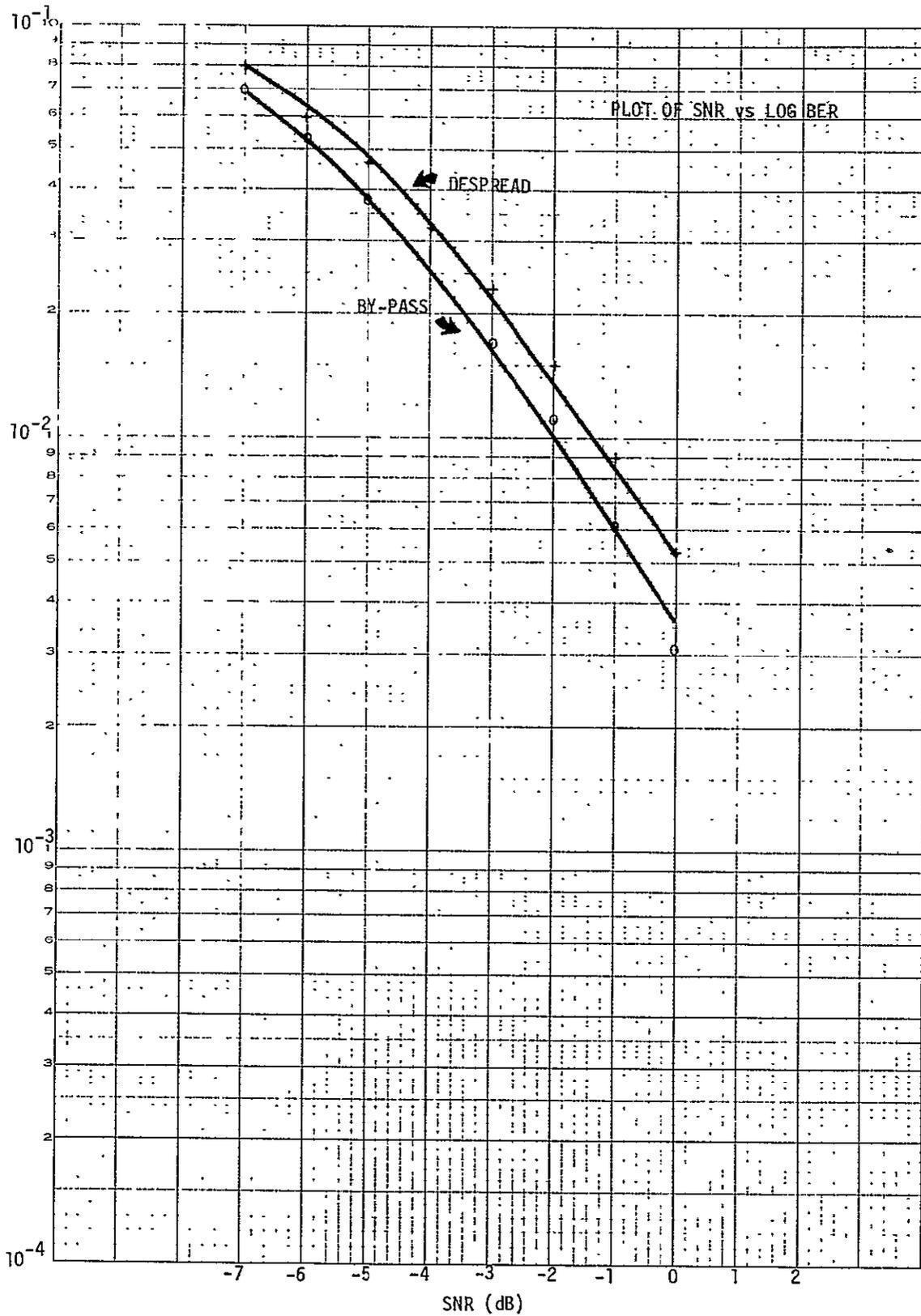
Figure 5-11. 3 Mbps Error Degradation

Table 5-4. 72 kbps Error Degradation Data, 10 Sec Samples

SNR (dB)	(dB-Hz) C/N_0	No Spreading		Spreading	
		Error Count (Hz)	BER	Error Count (Hz)	BER
-10	71	5.3	7.4×10^{-5}	6.5	9.0×10^{-5}
-9	70	0.63	8.7×10^{-6}	—	—
-8	69	0.17	2.4×10^{-6}	0.05	6.7×10^{-7}
-7	68	0.00	0	0.025	3.5×10^{-7}

Table 5-5. 3 Mbps Error Degradation

SNR (dB)	(dB-Hz) C/N_0	No Spreading		Spreading	
		Error Count (kHz)	BER	Error Count (kHz)	BER
-7	68	210	7.0×10^{-2}	240	8.0×10^{-2}
-6	69	160	5.3×10^{-2}	180	6.0×10^{-2}
-5	70	115	3.8×10^{-2}	140	4.7×10^{-2}
-4	71	79	2.6×10^{-2}	98	3.3×10^{-2}
-3	72	52	1.7×10^{-2}	68	2.3×10^{-2}
-2	73	32	1.1×10^{-2}	45	1.5×10^{-2}
-1	74	18	6.0×10^{-3}	27	9.0×10^{-3}
0	—	9.2	3.1×10^{-3}	16	6.3×10^{-3}

5.2 216 KBPS BPSK MODEM

Test No. 1:   Test set BPSK Modulator

Objective: To verify operation of the test set modulator

Procedure: Refer to Figure 5-1 for initial connections

1) Disconnect the cable on the test set front panel going between MODULATOR RF OUT and CHANNEL RF IN.

2) Connect the HP141T spectrum analyzer to MODULATOR RF OUT.

3) Disconnect input to MODULATOR PN CLOCK.

4) Observe the frequency spectrum, which should appear as shown in Figures 5-12 and 5-13 for the analyzer settings shown. Note that there are nulls at 110 MHz and 110 MHz ±432 kHz.

5) Disconnect the 144 kHz DATA CLOCK and provide the proper 14.1 MHz input to the MODULATOR PN CLOCK.

6) The spectrum should now appear as in Figure 5-10 with nulls at ±14.1 MHz.

7) Disconnect the MODULATOR PN CLOCK. Provide a TTL level input of roughly 300 Hz to the 144 kHz DATA CLOCK input. With the HP8407 network analyzer connected to the MODULATOR RF OUT, view the two phase states created by the data modulation. Figure 5-14 illustrates the two arbitrary phase states 180 degrees ±5 degrees apart.

Discussion. The biphase modulation being monitored in this test has a much simpler structure than the UQPSK signal seen previously. Only one channel exists, eliminating much of the earlier procedure. As before, the phase states are displayed on a polar coordinate system, making it possible to measure phase angle directly.

With all changes made to the test set for 216 kbps operation (data rate switch, modulator PC board, and receiver bandpass filter) the 72 kbps channel panel connections function as the 216 kbps connections. In this section, those points will be referred to as they are labeled, with the tacit understanding of their modified use.
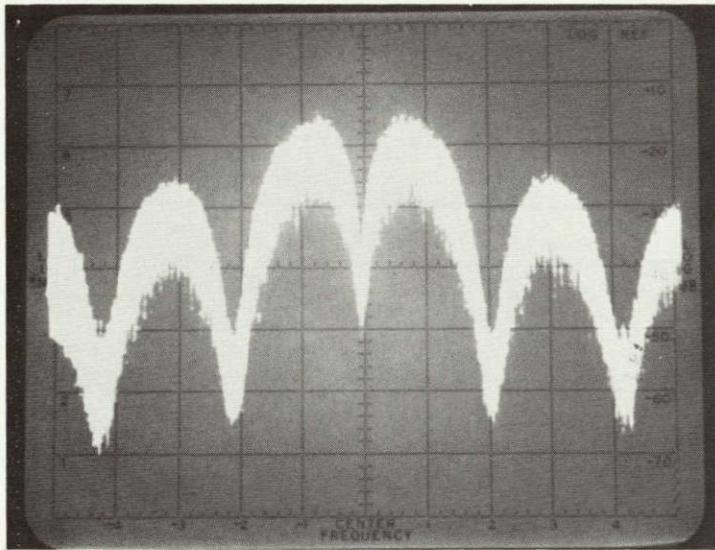
Analyzer Settings:

Vert: 10 dB/Div
Hor: 200 kHz/Div
BW: 10 kHz
Video: 10 kHz

Figure 5-12. 216 kbps Data Spectrum
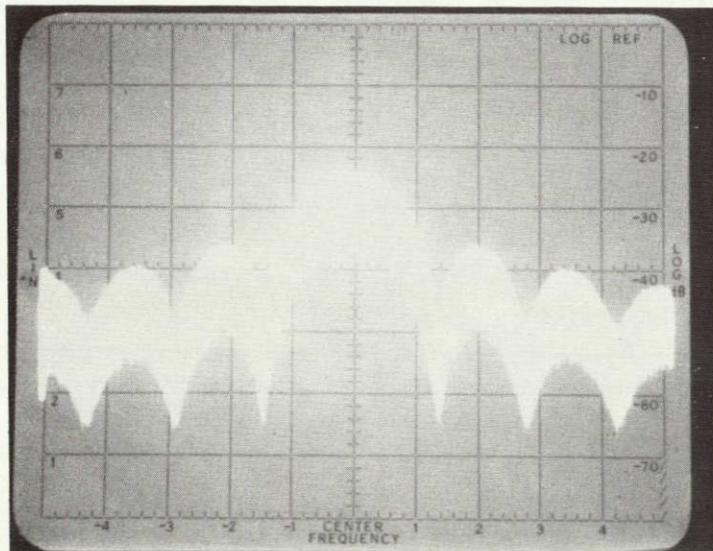
Analyzer Settings:

Vert: 10 dB/Div
Hor: 10 MHz/Div
BW: 10 kHz
Scan: 1 Sec/Div
Video: 10 kHz

Figure 5-13. PN Code Spectrum
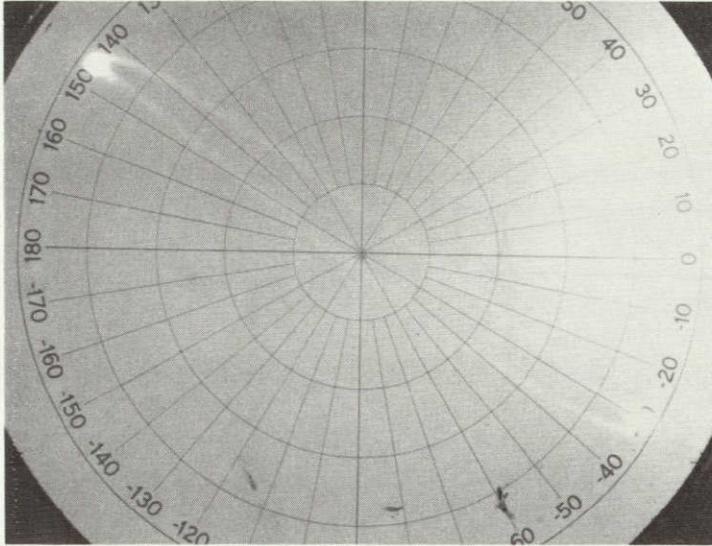
Analyzer Settings:

As Needed

Figure 5-14.   Network Analyzer Polar Display

Test No. 2:   Signal Characteristics

Objective: To verify S+N and AGC characteristics

Procedure: Refer to Figure 5-1 for initial connections

1) Terminate CHANNEL NOISE port, and use MANUAL AGC control
   to get -25 dBm out at the CHANNEL RF OUT port.

2) Disconnect the MODULATOR RF OUT from the CHANNEL RF IN
   and terminate the CHANNEL RF IN. Input sufficient noise
   power at CHANNEL NOISE to record -15 dBm out of CHANNEL
   RF OUT.

3) Reconnect CHANNEL RF IN and MODULATOR RF OUT. The output
   power will increase slightly, to about -14.6 dBm.

4) Use MANUAL AGC control on panel to set the CHANNEL RF OUT
   power at -15 dBm for use with the despreader. The SNR is
   -10 dB.

Discussion. The CHANNEL simulates a noisy communications transmission channel by summing noise with the spread spectrum signal. Signal-to-noise ratios are established by setting relative powers of the internal signal and external noise. The summed signal plus noise is then set at the proper level for despreader operation. Noise power is being measured in a 30 MHz bandwidth (filtering internal to the test set). This establishes the relationship that C/N_o (dB) = SNR (dB) + 75.

Test No. 3: Receiver Performance

Objective: To verify proper receiver simulation and operation of the bit synchronizer and test set

Procedure: Refer to Figure 5-1 for initial connections

1) Disconnect 14.1 MHz MODULATOR PN CLOCK.

2) Connect the test set CHANNEL RF OUT to the despreader BY-PASS IN. Also, connect the despreader BY-PASS OUT to the test set DEMODULATOR RF IN.

3) Make proper REF DATA and REF CLOCK connections for 72 kbps demodulation. (Be sure to put REF DATA switch in the 72 kbps position, too.)

4) Set CARRIER PHASE control to approximately 8.5 and set the toggle switch on the phase shifter to 180 degrees (access from top of test set).

5) Using a dual trace oscilloscope to monitor the data and using the REF DATA SYNC output for external triggering of the scope, monitor the REF DATA on the B channel of the scope (using a tee connector at the test set panel). Connect the scope A channel to the DATA output, monitoring either DETECTED or RECONSTRUCTED DATA by switch selection.

6) With a counter monitoring the DEMODULATOR BIT ERRORS output, adjust the CARRIER PHASE control for minimum errors. (It is helpful to temporarily use a higher level of noise for this operation, -15 dB SNR is suitable). With the noise again reduced for a -10 dB SNR, the oscilloscope displays of DETECTED and RECONSTRUCTED DATA will be as shown in Figures 5-15 and 5-16.

5-23
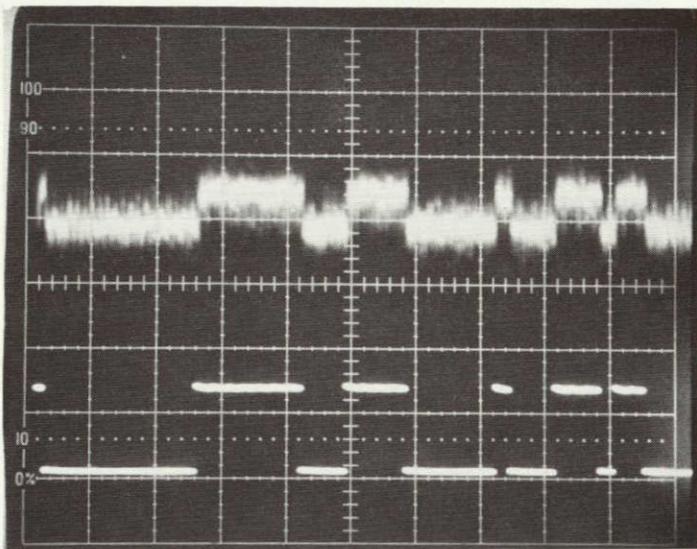
Scope Settings:

Hor: 20 μsec/Div

Vert: 10 mV/Div
(top)

3 V/Div
(bottom)

Figure 5-15.   216 kbps Data

Scope Settings:

Hor: 20 μsec/Div
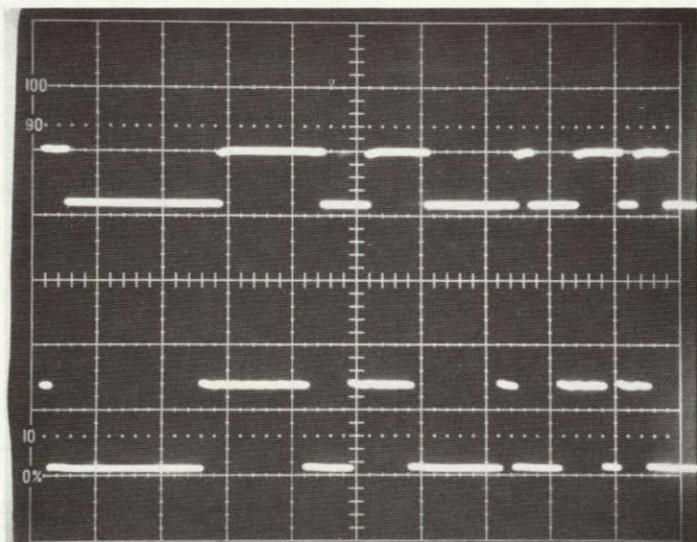
Vert: 5 V/Div (top)

3 V/Div
(bottom)

Figure 5-16.   216 kbps Data

7) With 0 dB SNR (amplitude into despreader adjusted accordingly) no errors should be counted at the DEMODULATOR BIT ERRORS output. Disconnecting the REF DATA IN cable should yield 108,106 or 107,894 ±35 errors/second.

Discussion. Disconnecting the PN code and by-passing the despreader eliminates spread spectrum techniques from the signal path. With no noise added to the information, data should be recovered perfectly, with no resultant errors. When the REF DATA input is removed, the received data is compared with one state (either a "1" or a "0") always. Since the data is being generated by a PN generator the data consists of approximately 50 percent 1's and 0's. Thus, when the REF DATA input is removed, about 50 percent errors should be counted.

Test No. 4: Acquisition Tests

Objective: To verify average acquisition times of less than 10 seconds at C/N_0 of 60 dB-Hz and higher

Procedure: Refer to Figure 5-1 for initial connections

1) Set desired SNR and Doppler simulation, maintaining a proper power level to the despreader.

2) Connect a time-interval counter to the CODE LOCK output of the despreader. Use the common start/stop function. Set start for -1 volt, negative-going edge, and set stop for -1 volt, positive-going edge.

3) For automatic operation, set the frequency of an HP3310 function generator to approximately 0.03 Hz, negative pulsed output, +5 to 0 volts. Check that over approximately. a 30.second period the generator puts out +5 volts for 25 seconds and 0 volt for 5 seconds.

4) For automatic operation, connect the generator to the CODE RESET BNC input on the despreader panel.

5) Every 30 seconds the function generator will reset the despreader, forcing it to go into its initial acquisition routine. The reset command will start the time-interval counter. When the despreader locks or when the next reset

command comes, the time measurement is ended. The number
is displayed on the counter for 5 seconds as the despreader
resets. The data can be recorded manually or automatically
in this time period. One-hundred such measurements shall be
made for each average time to be found. Of these, discard
the 10 longest times and average the reset. This is the
value $\overline{T_{acq}}$.

6) The above steps 1 through 6 can be repeated for every com-
bination of SNR and Doppler offset. A table of the form
shown in Table 5-6 might be used. Additionally, average
acquisition times for ±1 dB AGC variations can be measured
by simply changing the despreader input power to -14
or -16 dBm and repeating the above steps. Data measured
during acceptance testing is recorded in Table 5-7.

Table 5-6. Data Summary for $\overline{T_{acq}}$ (sec)

C/N_o \ Doppler	60 dB-Hz	65 dB-Hz	75 dB-Hz
Max Positive Doppler	1.06	0.89	
No Doppler	1.29	1.37	
Max Negative Doppler	2.73	3.02	

AGC \ C/N_o Doppler	-1 dB	NOM	+1 dB
	-16 dBm	-15 dBm	-14 dBm
No Doppler	1.23	1.29	1.28

Table 5-7. BPSK T_{acq} Data (msec)

Maximum Positive Doppler, -15 dB SNR

0 0 0 1 2 9 0	0 0 0 0 0 4 5	0 0 0 1 5 6 0
0 0 0 0 3 8 7	0 0 0 1 5 2 4	0 0 0 2 1 0 3
0 0 0 0 2 9 7	0 0 0 2 7 4 1	0 0 0 1 4 3 0
0 0 0 1 5 4 8	0 0 0 0 2 7 5	0 0 0 2 7 3 3
0 0 0 0 2 8 3	0 0 0 1 1 5 7	0 0 0 0 3 4 0
0 0 0 1 8 4 8	0 0 0 2 2 1 6	0 0 0 0 5 1 0
0 0 0 1 2 5 1	0 0 0 0 0 1 1	0 0 0 0 2 5 9
0 0 0 0 1 5 8	0 0 0 1 8 1 9	0 0 0 1 1 0 6
0 0 0 0 3 3 3	0 0 0 2 9 0 9	0 0 0 0 3 0 7
0 0 0 0 4 7 5	0 0 0 0 2 3 7	0 0 0 1 4 8 2
0 0 0 3 2 5 6	0 0 0 0 2 0 1	0 0 0 1 3 9 0
0 0 0 1 3 2 3	0 0 0 1 2 5 0	0 0 0 0 0 1 4
0 0 0 1 2 5 7	0 0 0 1 3 6 9	0 0 0 0 6 9 8
0 0 0 0 5 0 5	0 0 0 0 5 1 5	0 0 0 0 9 7 6
0 0 0 1 1 9 1	0 0 0 1 5 2 7	0 0 0 1 4 1 6
0 0 0 0 4 2 9	0 0 0 0 1 2 4	0 0 0 1 0 9 2
0 0 0 0 4 0 3	0 0 0 1 4 6 9	0 0 0 0 7 6 4
0 0 0 1 1 1 6	0 0 0 0 8 3 7	

Maximum Positive Doppler, -10 dB SNR

0 0 0 1 3 7 9	0 0 0 1 1 1 3	0 0 0 0 0 4 6
0 0 0 0 2 0 9	0 0 0 0 4 2 0	0 0 0 0 6 2 9
0 0 0 0 0 5 3	0 0 0 0 1 9 7	0 0 0 1 1 7 1
0 0 0 0 2 0 7	0 0 0 1 2 4 8	0 0 0 0 3 3 9
0 0 0 0 5 0 1	0 0 0 0 9 9 3	0 0 0 0 3 5 1
0 0 0 1 4 4 0	0 0 0 0 8 8 5	0 0 0 1 4 5 7
0 0 0 1 5 4 9	0 0 0 1 1 0 5	0 0 0 0 0 1 0
0 0 0 1 3 3 2	0 0 0 0 6 6 6	0 0 0 0 2 1 4
0 0 0 0 8 0 4	0 0 0 1 1 0 6	0 0 0 0 8 8 4
0 0 0 1 1 6 0	0 0 0 1 4 0 2	0 0 0 0 8 3 9
0 0 0 0 8 8 7	0 0 0 1 3 7 0	0 0 0 0 7 4 4
0 0 0 0 3 4 6	0 0 0 1 3 6 0	0 0 0 1 4 2 2
0 0 0 1 5 6 3	0 0 0 0 9 5 2	0 0 0 0 7 3 2
0 0 0 1 5 3 8	0 0 0 0 5 2 4	0 0 0 1 1 3 6
0 0 0 0 5 0 6	0 0 0 0 7 6 9	0 0 0 1 1 9 4
0 0 0 0 5 3 8	0 0 0 1 5 4 6	0 0 0 0 3 8 0
0 0 0 1 5 7 5	0 0 0 1 0 5 0	0 0 0 1 2 8 5
0 0 0 0 3 3 7	0 0 0 1 2 3 5	

Table 5-7. BPSK T_{acq} Data (msec) (Continued)

0 Doppler, -15 dB SNR

Col 1	Col 2	Col 3
0 0 0 0 3 8 5	0 0 0 0 6 8 5	0 0 0 1 6 5 9
0 0 0 1 3 8 5	0 0 0 1 3 0 6	0 0 0 0 8 5 5
0 0 0 0 8 8 4	0 0 0 2 4 6 7	0 0 0 1 3 5 0
0 0 0 1 9 0 1	0 0 0 2 2 8 6	0 0 0 1 2 2 7
0 0 0 0 1 9 0	0 0 0 2 2 0 5	0 0 0 1 4 1 9
0 0 0 0 8 2 2	0 0 0 0 3 8 9	0 0 0 2 3 3 7
0 0 0 0 4 2 4	0 0 0 0 5 4 5	0 0 0 1 7 8 2
0 0 0 0 6 1 2	0 0 0 0 3 2 3	0 0 0 2 2 0 3
0 0 0 1 5 8 7	0 0 0 1 0 6 5	0 0 0 2 3 9 5
0 0 0 0 8 8 0	0 0 0 2 0 4 2	0 0 0 2 3 2 6 3
0 0 0 0 1 6 6	0 0 0 1 5 3 6	0 0 0 0 7 6 3
0 0 0 0 4 3 4	0 0 0 2 1 7 5	0 0 0 1 4 9 5
0 0 0 2 0 5 4	0 0 0 2 0 9 9	0 0 0 1 8 9 9
0 0 0 1 6 3 5	0 0 0 2 1 0 1	0 0 0 0 4 4 4
0 0 0 0 2 9 9	0 0 0 0 4 5 6	0 0 0 1 3 0 9
0 0 0 0 7 6 1	0 0 0 0 9 1 6	0 0 0 1 6 7 8

0 Doppler, -10 dB SNR

Col 1	Col 2	Col 3
0 0 0 2 3 2 3	0 0 0 0 6 0 8	0 0 0 1 8 2 0
0 0 0 1 0 8 2	0 0 0 1 8 1 0	0 0 0 2 3 1 7
0 0 0 1 2 3 1	0 0 0 2 1 7 2	0 0 0 1 8 2 5
0 0 0 0 2 6 6	0 0 0 0 1 3 5	0 0 0 2 4 1 9
0 0 0 0 2 0 6	0 0 0 0 3 4 1	0 0 0 1 7 3 9
0 0 0 1 1 1 0	0 0 0 2 4 9 5	0 0 0 0 2 3 2
0 0 0 2 3 6 4 5	0 0 0 1 5 1 2	0 0 0 1 7 1 5
0 0 0 1 7 4 5	0 0 0 2 7 5 7	0 0 0 0 6 5 6
0 0 0 2 0 9 7	0 0 0 1 3 2 0	0 0 0 2 4 5 0
0 0 0 0 3 5 7	0 0 0 2 3 3 9	0 0 0 1 8 2 1
0 0 0 0 9 3 4	0 0 0 0 5 8 0	0 0 0 1 0 9 6
0 0 0 1 6 2 6	0 0 0 0 9 2 9	0 0 0 1 9 2 6
0 0 0 2 5 5 0	0 0 0 0 4 4 0	0 0 0 0 6 4 5
0 0 0 0 7 3 5	0 0 0 1 0 0 4	0 0 0 1 1 6 6
0 0 0 1 9 5 0	0 0 0 1 2 5 0	0 0 0 1 0 4 5
0 0 0 1 1 1 0	0 0 0 1 8 7 1	0 0 0 0 7 0 6
0 0 0 0 4 8 9	0 0 0 2 0 2 9	0 0 0 1 2 8 2
0 0 0 0 5 0 3	0 0 0 0 6 7 1	

Table 5-7. BPSK T_{acq} Data (msec) (Continued)

Maximum Negative Doppler, -15 dB SNR		
0 0 0 1 3 5 6	0 0 0 2 5 7 2	0 0 0 2 1 3 3
0 0 0 1 4 6 1	0 0 0 5 2 3 0	0 0 0 0 3 7 4
0 0 0 2 3 6 3	0 0 0 2 5 0 0	0 0 0 4 2 4 6
0 0 0 2 6 4 8	0 0 0 0 0 5 4	0 0 0 0 1 5 1
0 0 0 0 8 5 0	0 0 0 2 2 9 0	0 0 0 2 3 2 9
0 0 0 3 9 2 7	0 0 0 3 2 5 9	0 0 0 4 0 4 7
0 0 0 2 2 8 0	0 0 0 0 8 8 2	0 0 0 2 7 7 1
0 0 0 5 4 9 2	0 0 0 2 2 1 9	0 0 0 1 4 6 2
0 0 0 3 3 7 9	0 0 0 0 3 0 7	0 0 0 5 0 3 0
0 0 0 3 5 8 3	0 0 0 3 0 6 5	0 0 0 3 8 5 6
0 0 0 3 5 4 1	0 0 0 4 0 1 0	0 0 0 4 4 8 9
0 0 0 1 1 4 4	0 0 0 5 1 0 1	0 0 0 3 3 0 7
0 0 0 0 0 3 4	0 0 0 5 1 9 5	0 0 0 3 0 2 9
0 0 0 0 6 4 7	0 0 0 5 1 3 4	

Maximum Negative Doppler, -10 dB SNR		
0 0 0 3 5 7 8	0 0 0 0 9 0 6	0 0 0 5 2 9 9
0 0 0 2 1 1 6	0 0 0 8 4 7 7	0 0 0 0 2 8 3
0 0 0 1 3 9 3	0 0 0 3 0 8 0	0 0 0 1 4 3 6
0 0 0 1 6 4 2	0 0 0 2 5 8 7	0 0 0 5 4 5 2
0 0 0 3 4 5 1	0 0 0 3 3 9 4	0 0 0 7 2 0 9
0 0 0 1 6 2 5	0 0 0 3 6 8 6	0 0 0 2 3 4 0
0 0 0 3 1 0 5	0 0 0 0 0 6 3	0 0 0 1 7 3 1
0 0 0 5 1 7 0	0 0 0 2 2 3 5	0 0 0 2 5 2 5
0 0 0 3 3 6 1	0 0 0 0 5 0 6	0 0 0 4 3 8 4
0 0 0 1 5 5 0	0 0 0 2 1 6 3	0 0 0 4 6 4 9
0 0 0 4 9 4 3	0 0 0 2 1 6 7	0 0 0 3 3 9 0
0 0 0 0 5 0 0	0 0 0 5 3 0 7	0 0 0 2 4 7 7
0 0 0 5 0 9 7	0 0 0 3 4 4 5	0 0 0 3 5 4 7
0 0 0 1 8 6 7	0 0 0 2 0 9 3	0 0 0 1 2 4 1
0 0 0 1 3 6 3	0 0 0 1 1 6 8	0 0 0 4 3 1 2
0 0 0 6 2 6 3	0 0 0 6 2 7 9	0 0 0 2 2 5 4
0 0 0 0 8 2 0	0 0 0 3 0 4 6	0 0 0 3 5 5 9
0 0 0 3 2 5 1	0 0 0 1 9 7 0	

Table 5-7. BPSK T_{acq} Data (msec) (Continued)

-1 dB AGC		
0 0 0 0 9 7 0	0 0 0 2 2 3 3	0 0 0 0 2 9 3
0 0 0 1 8 5 7	0 0 0 1 1 7 2	0 0 0 0 5 9 0
0 0 0 1 7 4 1	0 0 0 1 8 9 6	0 0 0 0 5 2 6
0 0 0 2 3 4 7	0 0 0 1 9 1 2	0 0 0 0 5 0 8
0 0 0 2 4 9 0	0 0 0 0 2 9 2	0 0 0 0 2 5 2
0 0 0 1 0 8 4	0 0 0 3 6 5 9	0 0 0 0 9 1 7
0 0 0 2 4 6 0	0 0 0 0 7 5 5	0 0 0 3 2 3 9
0 0 0 1 2 0 1	0 0 0 1 3 9 7	0 0 0 2 1 7 9
0 0 0 0 5 9 6	0 0 0 0 5 5 4	0 0 0 0 7 2 6
0 0 0 2 2 8 5	0 0 0 1 4 4 1	0 0 0 0 3 1 7
0 0 0 1 9 2 2	0 0 0 0 0 7 2	0 0 0 0 3 9 2
0 0 0 0 7 8 9	0 0 0 1 7 0 6	0 0 0 2 3 4 3
0 0 0 1 0 2 0	0 0 0 0 7 5 6	0 0 0 0 3 1 2
0 0 0 2 3 2 0	0 0 0 1 1 4 6	0 0 0 0 9 6 1
0 0 0 1 0 8 1	0 0 0 0 4 9 9	0 0 0 2 2 1 4
0 0 0 0 4 5 3	0 0 0 1 2 6 3	0 0 0 0 3 3 3
0 0 0 0 3 1 2	0 0 0 0 3 6 9	

+1 dB AGC		
0 0 0 1 3 9 4	0 0 0 2 8 9 7	0 0 0 1 9 5 6
0 0 0 0 3 0 2	0 0 0 2 3 3 7	0 0 0 0 9 8 9
0 0 0 0 8 5 6	0 0 0 0 3 5 1	0 0 0 1 5 0 2
0 0 0 0 4 6 7	0 0 0 1 1 5 1	0 0 0 0 4 5 8
0 0 0 1 1 1 0	0 0 0 1 5 5 5	0 0 0 1 2 4 8
0 0 0 2 3 3 9	0 0 0 2 0 8 4	0 0 0 0 7 0 3
0 0 0 1 1 7 1	0 0 0 1 9 8 3	0 0 0 1 0 4 9
0 0 0 1 2 7 6	0 0 0 1 8 2 0	0 0 0 0 1 7 3
0 0 0 1 9 8 2	0 0 0 1 5 7 1	0 0 0 1 6 0 6
0 0 0 1 1 8 7	0 0 0 1 4 5 0	0 0 0 1 3 3 1
0 0 0 0 3 5 1	0 0 0 0 3 1 8	0 0 0 1 3 6 8
0 0 0 1 9 9 8	0 0 0 1 2 3 8	0 0 0 0 2 8 0
0 0 0 0 6 9 8	0 0 0 1 2 7 8	0 0 0 2 5 3 8
0 0 0 1 8 1 9	0 0 0 1 6 4 7	0 0 0 0 4 5 1
0 0 0 1 1 3 3	0 0 0 0 3 5 9	0 0 0 0 8 8 2
0 0 0 1 8 4 5	0 0 0 2 3 4 5	0 0 0 0 0 1 4
		0 0 0 1 1 4 4

Discussion. The CODE LOCK output is a tri-level signal indicating the three different states of acquisition: reset, search, and lock. Acquisition time is by definition the time from the end of reset to the beginning of lock. The automatic reset cycling forces an end to a given test if code lock has not been attained after 25 seconds of search time. This has been done to save time, since a 10 second average is required. It is quite suitable, however, to make automatic recycling slower or to switch to manual reset in the interest of obtaining statistical distributions, for example.

Test No. 5: Degradation Tests

Objective: To show that the despreader will not degrade the BER performance more than 1 dB

Procedure: Refer to Figure 5-1 for initial connections

1) Initialize the test set by repeating steps 1 through 6 of Test No. 3. During these tests, no external connection should be made to either unit, except for the counter.

2) Set up test set for C/N_0 = 60 dB-Hz.

3) Measure BER.

4) Change C/N_0 by 1 dB and repeat steps 2 and 3. Record BER and plot data as in Table 5-8 and Figure 5-17.

5) Reconnect 14.1 MHz modulator PN clock on the test set.

6) Connect despreader.

7) Repeat steps 2 through 4 above, again using Table 5-8 and Figure 5-17. The two curves should not be more than 1 dB plus spreading degradation apart at any point. To measure spreading degradation, simply measure the power at the CHANNEL RF OUT port with the MODULATOR PN CLOCK both connected and disconnected. The difference should be about 0.1 dB yielding a 1.1 dB maximum spread between the two BER curves. A more complicated procedure was performed to isolate the effects of mixer leakage and excess filter loss due to despreading. The sum of these two factors is the reported 0.1 dB additional degradation.

Table 5-8. 216 kbps Error Degradation

SNR (dB)	C/N$_0$ (dB-Hz)	No Spreading		Spreading	
		Error Count	BER	Error Count	BER
-15	60	1.5 kHz	6.9×10^{-3}	2.9 kHz	1.3×10^{-2}
-14	61	700 Hz	3.2×10^{-3}	1.45 kHz	6.7×10^{-3}
-13	62	230 Hz	1.1×10^{-3}	590 Hz	2.7×10^{-3}
-12	63	65 Hz	3.0×10^{-4}	190 Hz	8.8×10^{-4}
-11	64	15 Hz	6.9×10^{-5}	54 Hz	2.5×10^{-4}
-10	65	2.6 Hz	1.2×10^{-5}	11 Hz	5.1×10^{-5}

Discussion. A few guidelines should be established for practicality
in making these measurements. First, in order to reasonably measure the
number of errors occurring at any BER, a minimum of about 100 errors should
be counted during a measurement. Therefore, a BER of 0.0001 was selected
as the lowest rate to be measured since this value corresponds to about
21.6 errors/second. The signal to noise will be degraded from the low BER
starting point until minimum C/N$_0$ (60 dB-Hz) is reached.

Very simply, the procedure outlined here first establishes a BER curve
for the test set, without any spread spectrum techniques. Then the mea-
surements are repeated, employing PN code spreading and despreading. The
difference between the two curves less the signal loss caused by spreading
the spectrum and filtering, is the degradation introduced by the despreader.
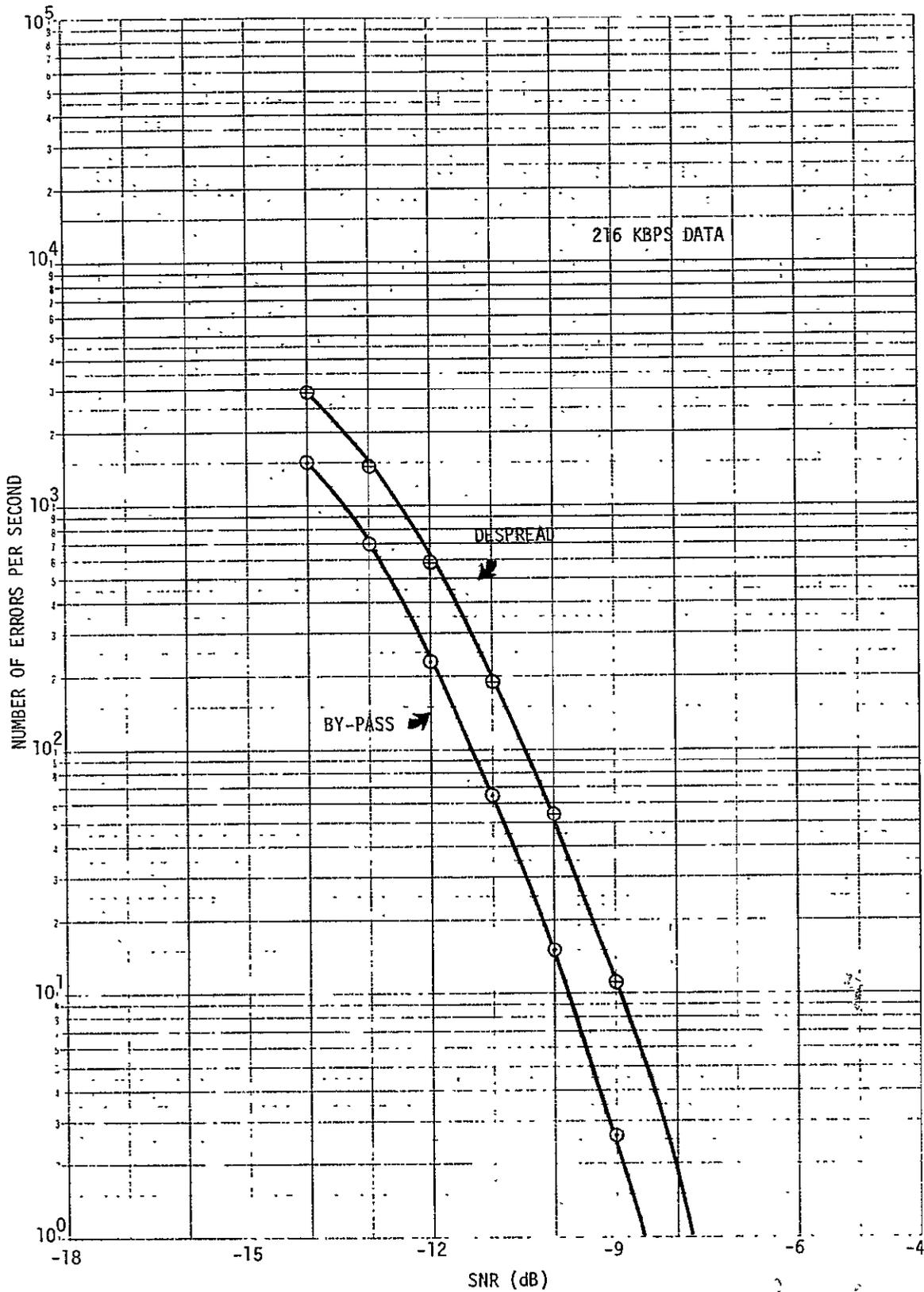
Figure 5-17. 216 kbps Error Degradation

5-33

6. FAULT ANALYSIS

In the event either the despreader or test set does not operate properly, it is most important to isolate the particular problem so that unnecessary alterations are not made to the circuits, as such alterations can thereafter create additional malfunctions. It is always wise to allow both the despreader and test set to establish an equilibrium with the environment before testing operation. Experience has shown that the most likely causes of malfunctioning are operator errors; it is therefore advisable to double-check all external equipment, as well as despreader and test set panel controls and cabling, before any internal adjustments are considered.

Table 6-1 is provided as an aid for correcting possible problems of either the despreader or test set. Several suggestions for probable cause of malfunctions are listed for different operational problems. Figures 6-1 and 6-2 also may be of assistance in fault analysis; they provide examples of signal levels at various test points on the despreader RF PC board.

Table 6-1. Fault Analysis

Problem	Corrective Action
Despreader does not lock	Check input spectrum for PN and data modulation
	Check test set and carrier frequencies
	Check SNR and power level
	Check despreader filter cabling
	Check despreader mode switch, dwell time switch, etc.
	Check VCXO offset during search
	Check acquisition threshold voltage
Despreader locks for high or low SNR, not both	Check gain normalization — i.e., RF PC test points 4, 5 and 6
Despreader does not pull-in for low SNR and full Doppler	Check VCXO offset during search
	Check acquisition threshold voltage
	Check input spectrum parameters·
Test set does not demodulate	Check spectrum returned to test set
	Check mode and channel connections
	Check phase adjustments
	Check bit reconstruct threshold
BER degradation excessive	Check CARRIER PHASE setting during despread measurements
$\overline{T_{ACQ}}$ too long	Check Doppler frequencies
	Check SNR
	Check VCXO offset during search
	Check acquisition threshold voltage

FOLDOUT FRAME

DC MEASUREMENTS   FOLDOUT FRAME

TP3	−156 mV	TP6	−800 mV	TP12	−1.1 mV
TP4	+144 mV	TP8	+106 mV	TP13	+4.4 mV
TP5	−18 mV	TP11	−298 mV	TP15	+6.1 mV

TP1
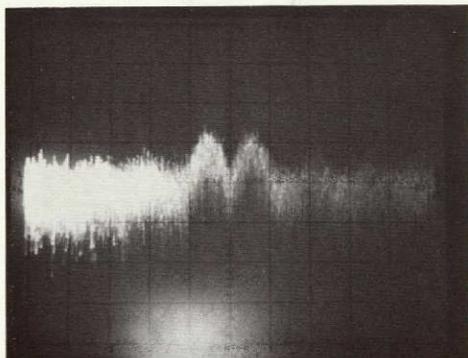
TP9
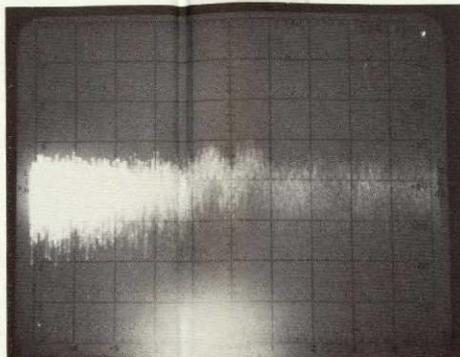
TP12
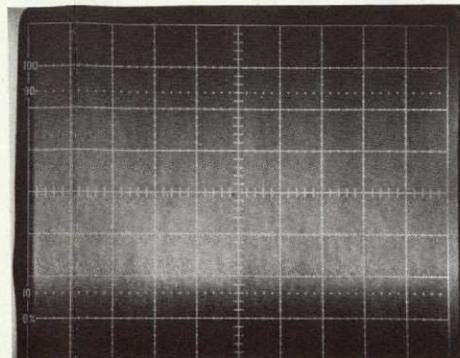
HOR: 100 kHz/DIV   VERT: 10 dB/DIV

BW: 10 kHz   LOG REF LEVEL: 30 dBm

HOR: 10 msec/DIV   VERT: 0.5V/DIV

TP2
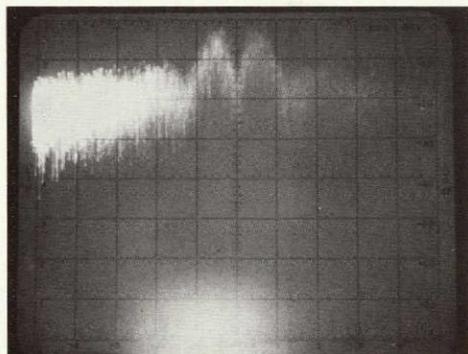
TP10
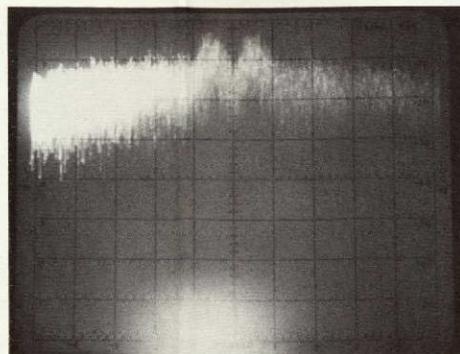
TP13
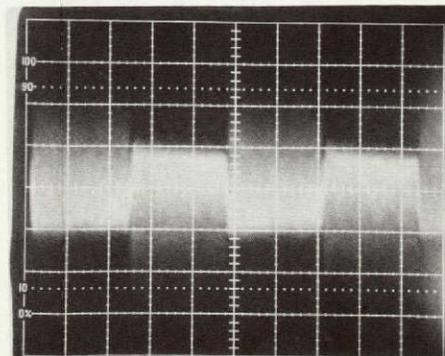
Figure 6-1. UQPSK RF PC Test Point
Signal Levels (Typical
Values for Minimum C/N_o)

FOLDOUT FRAME I.

TP3	−199 mV	TP6	−510 mV	TP12	−6.6 mV
TP4	+168 mV	TP8	+178 mV	TP13	+2.7 mV
TP5	−88 mV	TP11	−346 mV	TP15	+10.1 mV

TP1
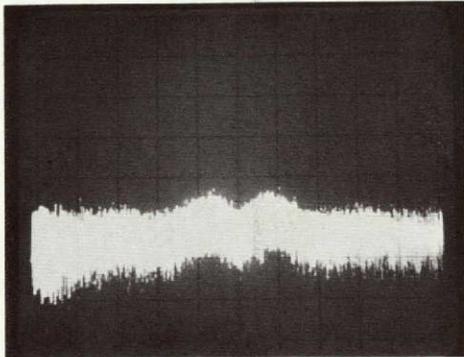
TP9
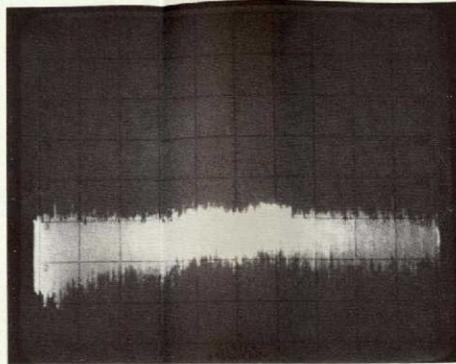
TP12
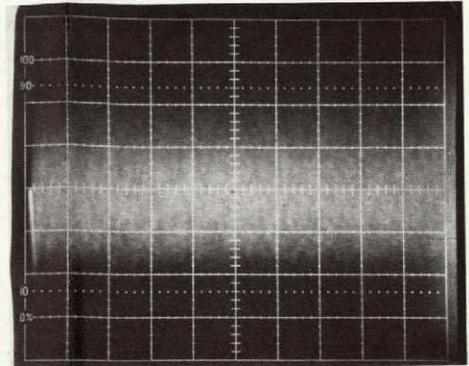
HOR: 200 kHz/DIV   VERT: 10 dB/DIV   BW: 10 kHz   LOG REF LEVEL: −10 dBm

HOR: 20 nsec/DIV   VERT: 1 V/DIV

TP2
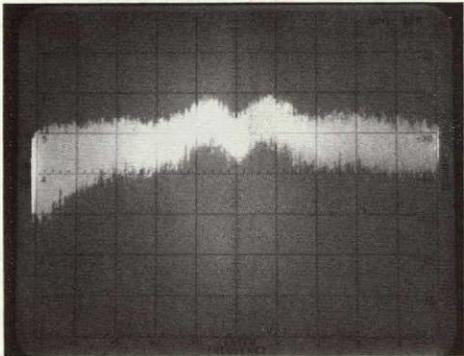
TP10
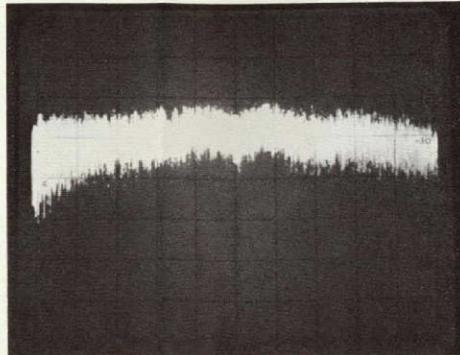
TP13
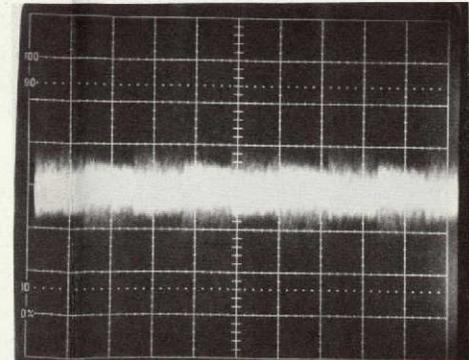
Figure 6-2.   BPSK RF PC Test Point
Signal Levels (Typical
Values for Minimum C/N_o)

APPENDIX A

UQPSK $\overline{T_{ACQ}}$ HISTOGRAMS

A complete set of acquistion time measurements for the UQPSK mode were made prior to acceptance testing. Histograms (Figure A-1 through A-17) showing the distribution of times measured were made for each specified set of signal conditions. Table A-1 provides a summary of the average values for acquisition time.

Table A-1. $\overline{T_{ACQ}}$ Summary for UQPSK (Seconds)

Doppler \ SNR	-7 dB	3 dB	51 dB
Maximum Positive Doppler	1.13	1.12	1.03
50% Positive	1.32	1.71	1.44
0 Doppler	2.91	2.58	2.04
50% Negative	· 3.29	3.68	3.33
Maximum Negative Doppler	6.52	6.56	6.28

DOPPLER/SNR \ AGC	-1 dB	NOM	+1 dB
0 Doppler/-7 dB SNR	2.26	2.91	2.39

CODE = 14.110460 MHZ   CARRIER = 110.230 MHZ   SNR = -7. DB

N TOTAL = 108.

N T>10 = 0.
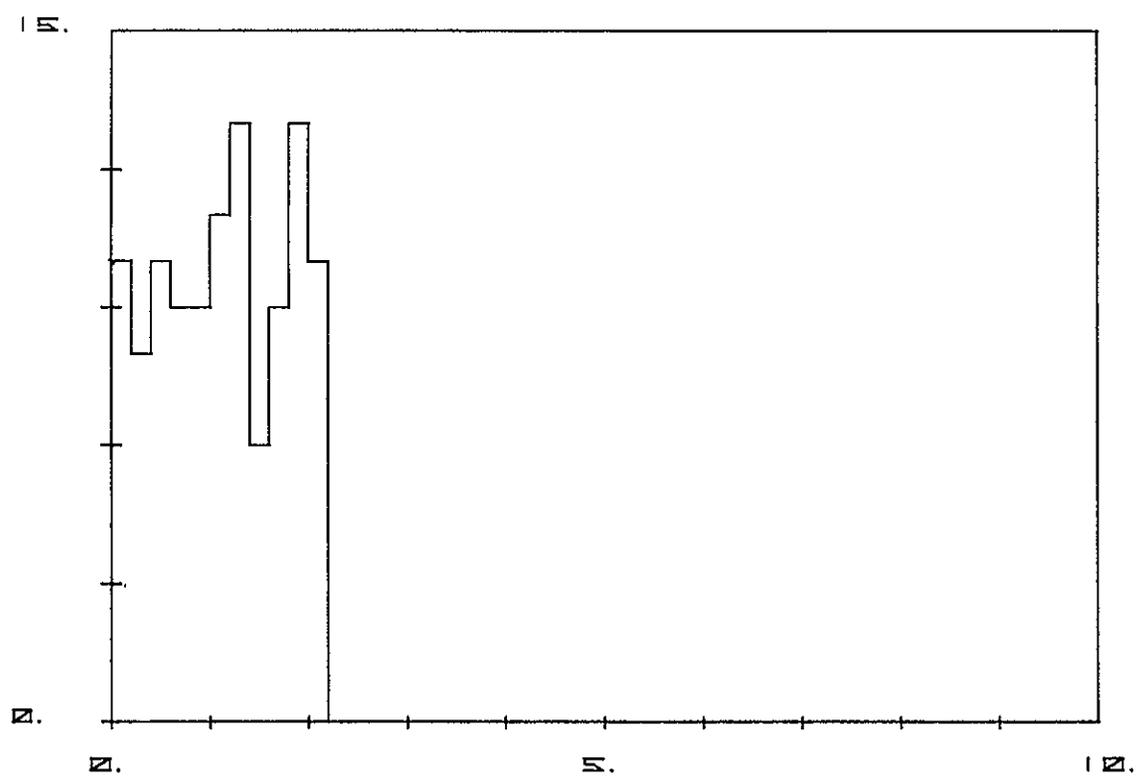
MEAN = 1.129 SEC

VAR = 0.401 SEC²

STD DEV = 0.633 SEC

Figure A-1. Acquisition Time Data

CODE = 14.100460 MHZ   CARRIER = 110.230 MHZ   SNR = 3. DB
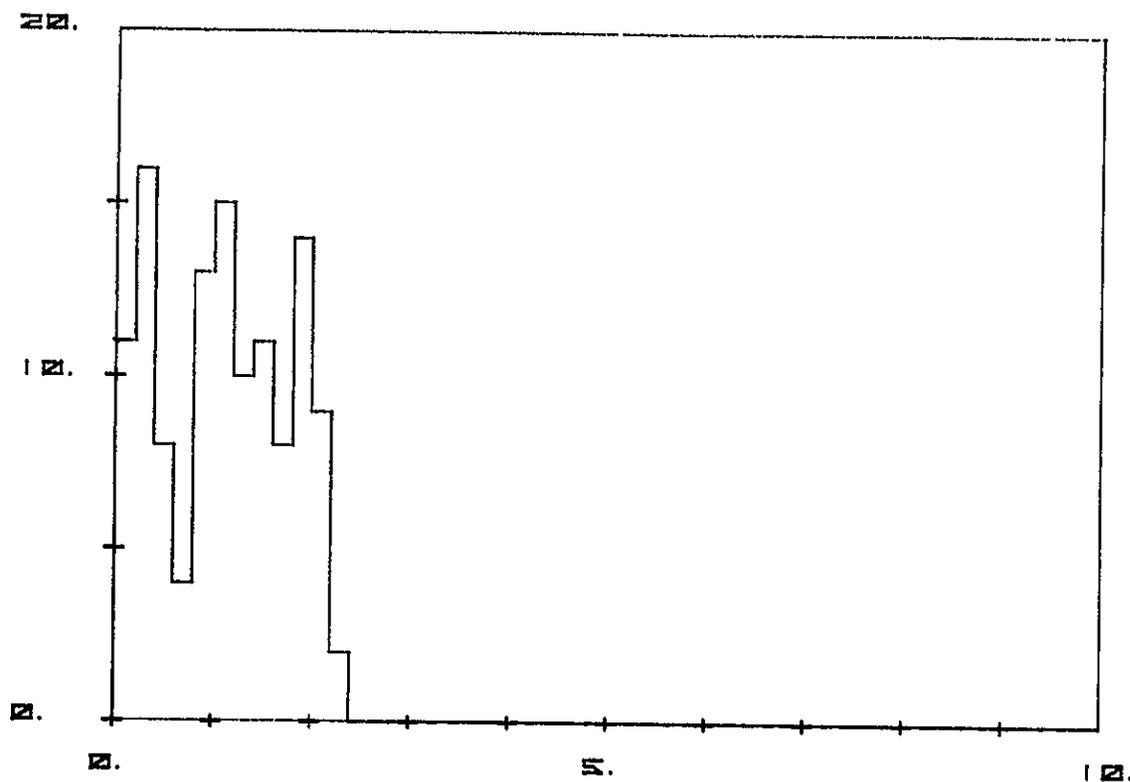
N_{TOTAL} = 121.

$N_{T>10}$ = 0.

MEAN = 1.115 SEC

VAR = 0.432 SEC^2

STD DEV = 0.657 SEC

Figure A-2. Acquisition Time Data

A-4

CODE = 14.100460 MHZ   CARRIER = 110.230 MHZ   SNR = 51. DB
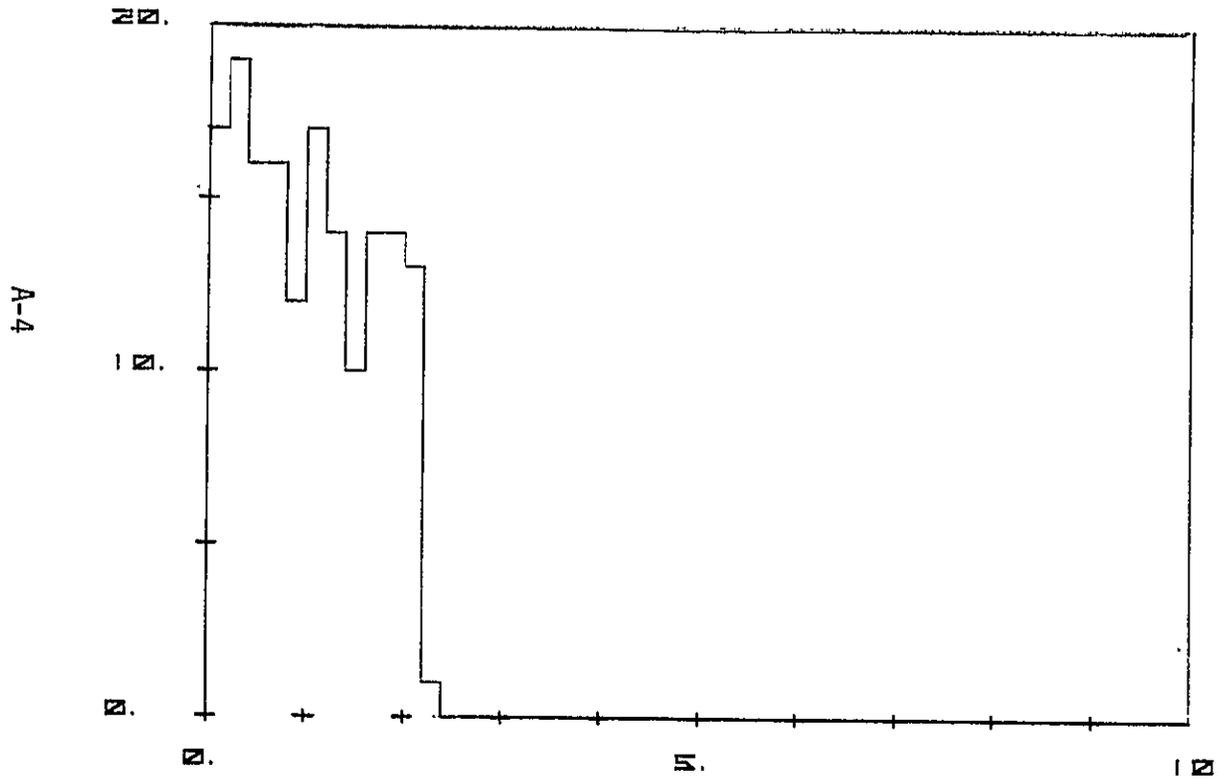
N_{TOTAL} = 163.

$N_{T > 10}$ = 0.

MEAN = 1.030 SEC

VAR = 0.418 SEC^2

STD DEV = 0.646 SEC

Figure A-3. Acquisition Time Data

CODE = 14.100230 MHZ   CARRIER = 110.115 MHZ   SNR = -7. DB

N_{TOTAL} = 230.

$N_{T>10}$ = 0.

MEAN = 1.316 SEC
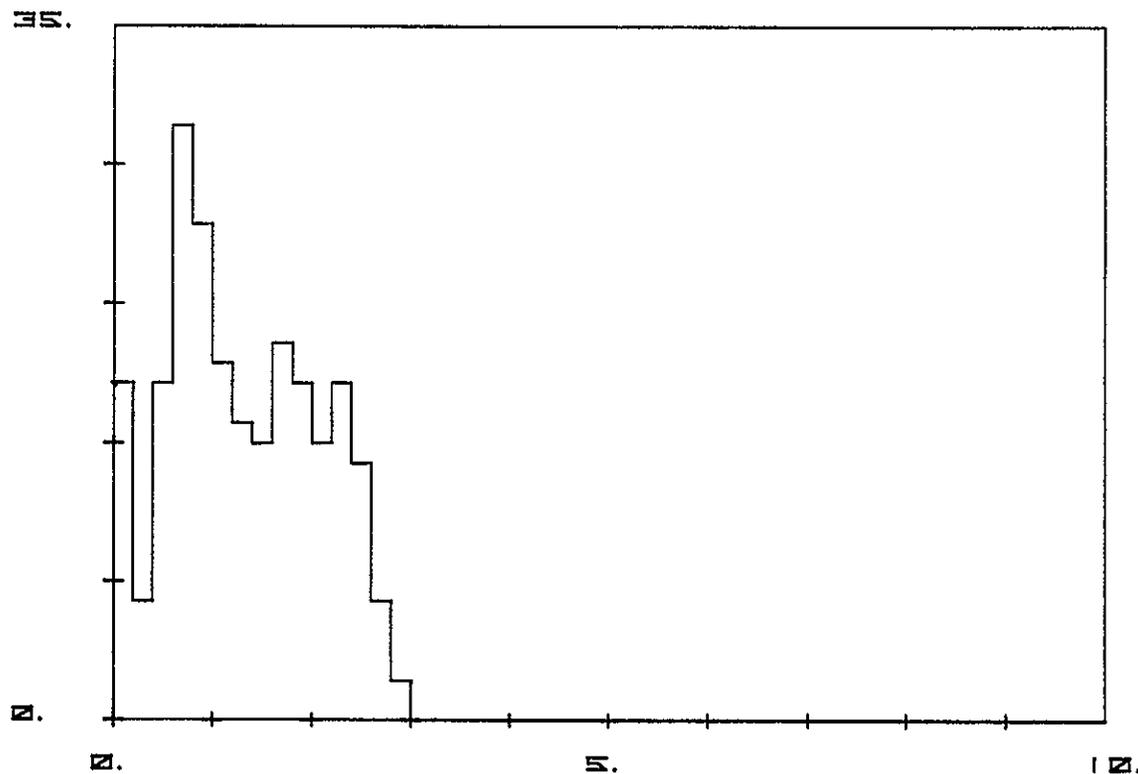
VAR = 0.559 SEC^2

STD DEV = 0.747 SEC

Figure A-4. Acquisition Time Data

A-6

CODE = 14.100230 MHZ   CARRIER = 110.115 MHZ   SNR = 3. DB

N TOTAL = 170.

N T>10 = 0.

MEAN = 1.711 SEC

VAR = 1.257 SEC²

STD DEV = 1.121 SEC
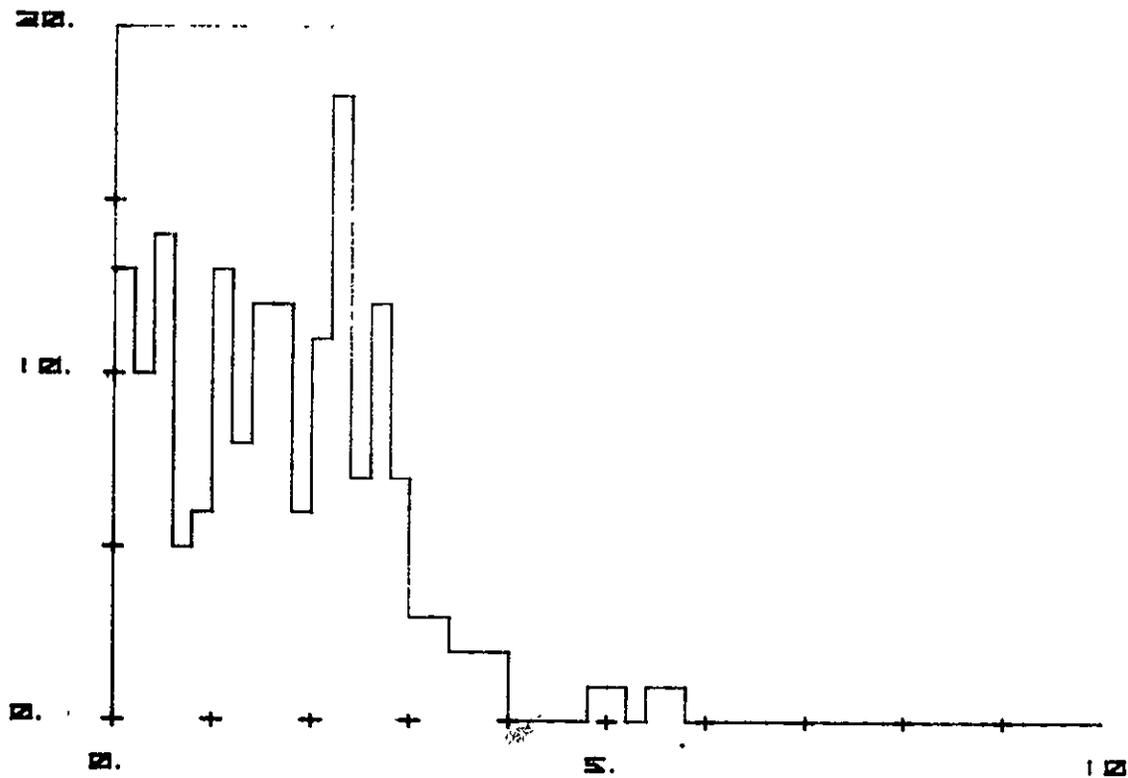
Figure A-5.   Acquisition Time Data

CODE = 14.100230 MHZ   CARRIER = 110.115 MHZ   SNR = 51. DB

N_{TOTAL} = 134.

$N_{T>10}$ = 0.
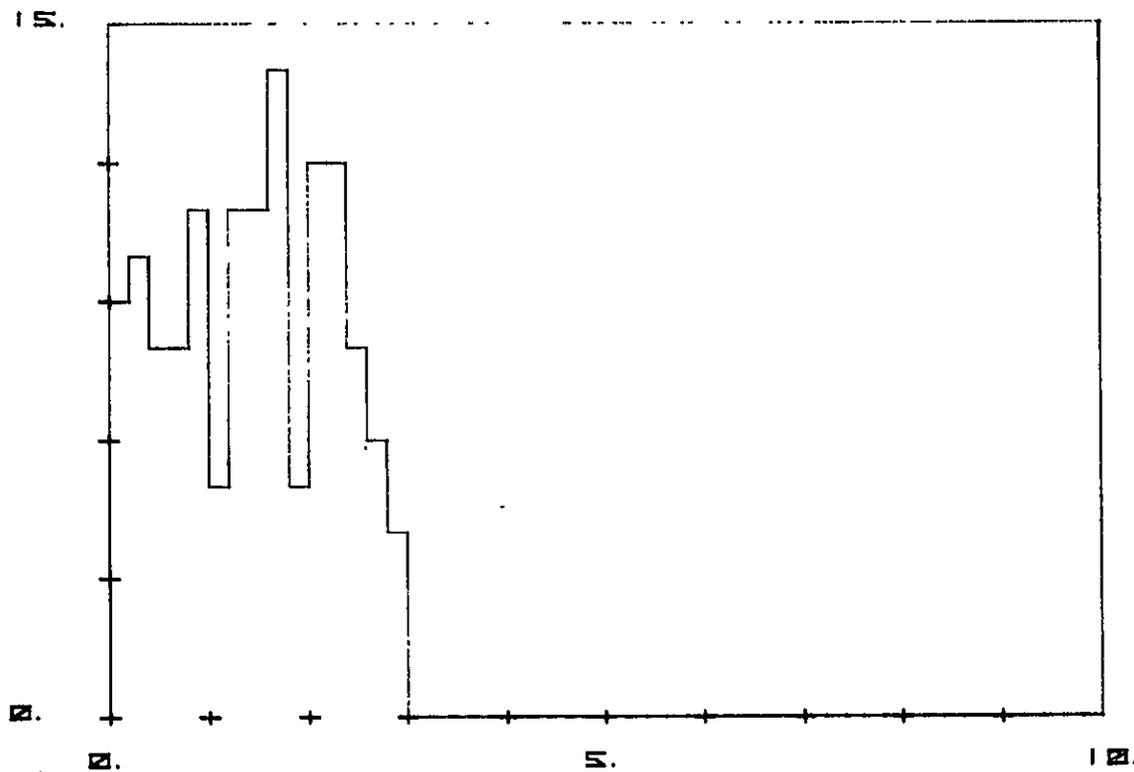
MEAN = 1.445 SEC

VAR = 0.551 SEC^2

STD DEV = 0.007 SEC

Figure A-6. Acquisition Time Data

CODE = 14.100000 MHZ   CARRIER = 110.000 MHZ   SNR = -7. DB

N_{TOTAL} = 157.

$N_{T>10}$ = 0.

MEAN = 2.914 SEC

VAR = 2.458 SEC^2

STD DEV = 1.568 SEC

Figure A-7. Acquisition Time Data

CODE = 14.100000 MHZ   CARRIER = 110.000 MHZ   SNR = 3. DB

A-9

N_{TOTAL} = 100.

$N_{T>10}$ = 0.

MEAN = 2.581 SEC

VAR = 3.622 SEC^2.
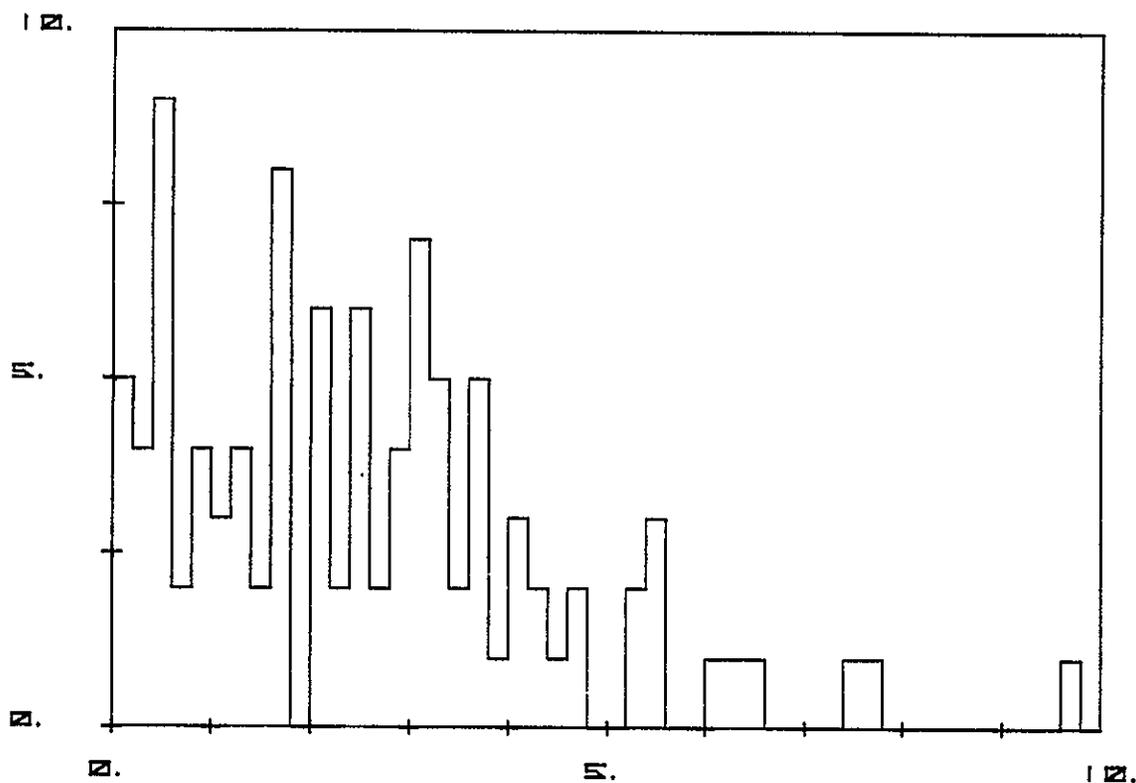
STD DEV = 1.903 SEC

Figure A-8. Acquisition Time Data

CODE = 14.100000 MHZ   CARRIER = 110.000 MHZ   SNR = 51. DB

$N_{TOTAL} = 111.$

$N_{T>10} = 0.$

MEAN = 2.040 SEC

VAR = 1.422 SEC^2
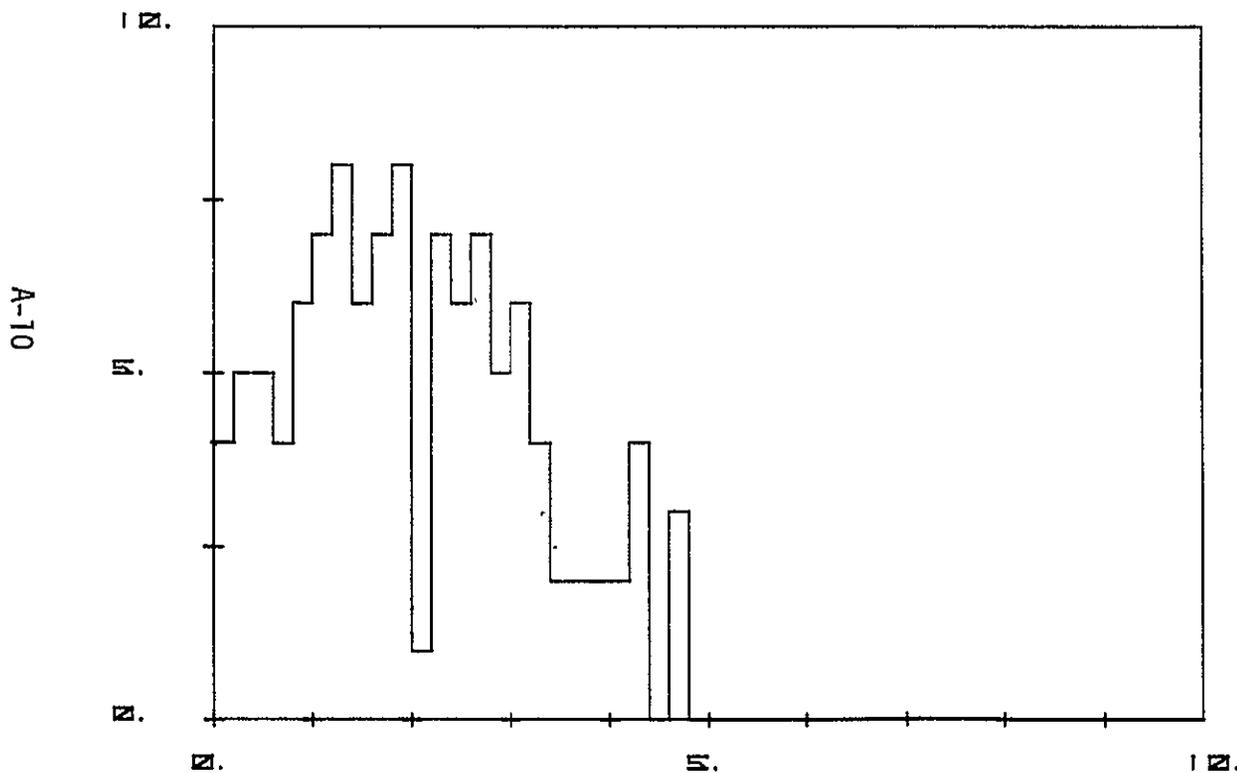
STD DEV = 1.192 SEC

Figure A-9. Acquisition Time Data

CODE = 14.099770 MHZ   CARRIER = 109.885 MHZ   SNR = -7. DB

N_{TOTAL} = 104.

$N_{T>10}$ = 0.

MEAN = 3.287 SEC

VAR = 3.715 SEC^2

STD DEV = 1.928 SEC

Figure A-10. Acquisition Time Data

A-11

Figure A-11. Acquisition Time Data

CODE = 14.295770 MHZ   CARRIER = 109.885 MHZ   SNR = 51. DB

$N_{TOTAL} = 115.$

$N_{T>10} = 0.$

MEAN = 3.329 SEC

VAR = 3.508 SEC^2

STD DEV = 1.873 SEC

Figure A-12. Acquisition Time Data

CODE = 14.098540 MHZ   CARRIER = 109.770 MHZ   SNR = -7. DB

N_{TOTAL} = 131.

$N_{T>10}$ = 0.

MEAN = 6.518 SEC

VAR = 1.865 SEC^2
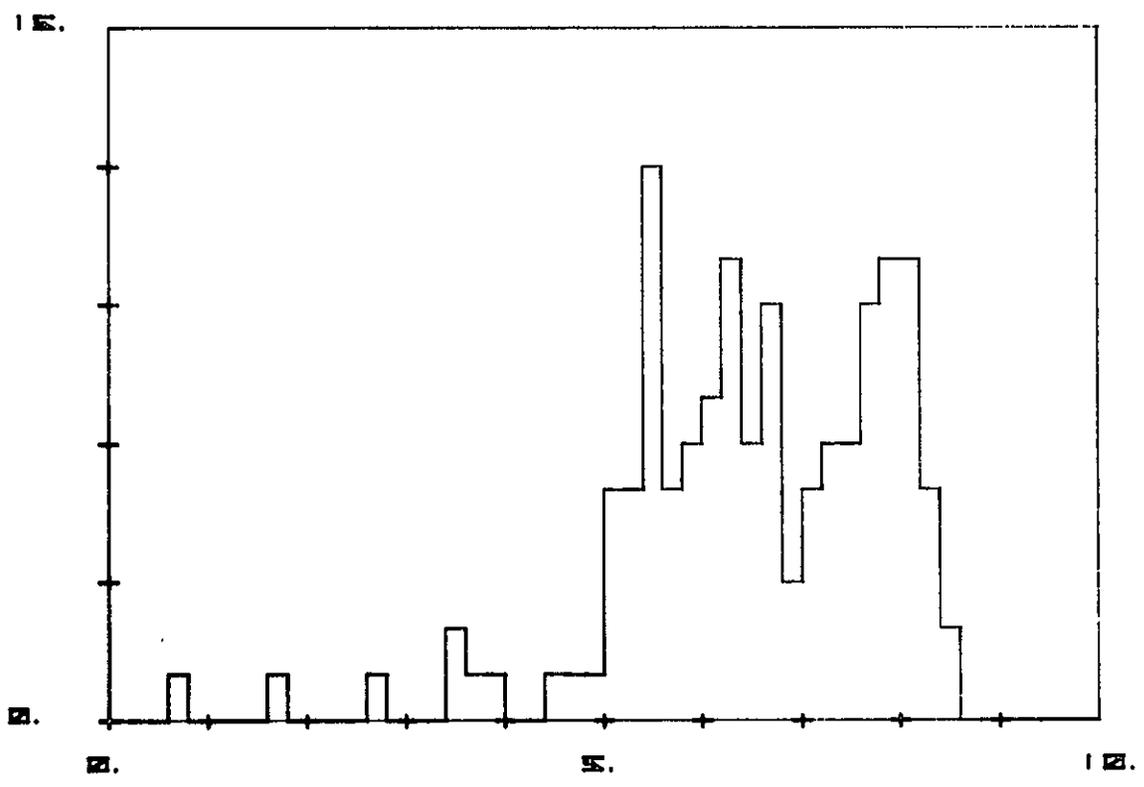
STD DEV = 1.366 SEC

Figure A-13. Acquisition Time Data

CODE = 14.099540 MHZ   CARRIER = 109.770 MHZ   SNR = 3. DB
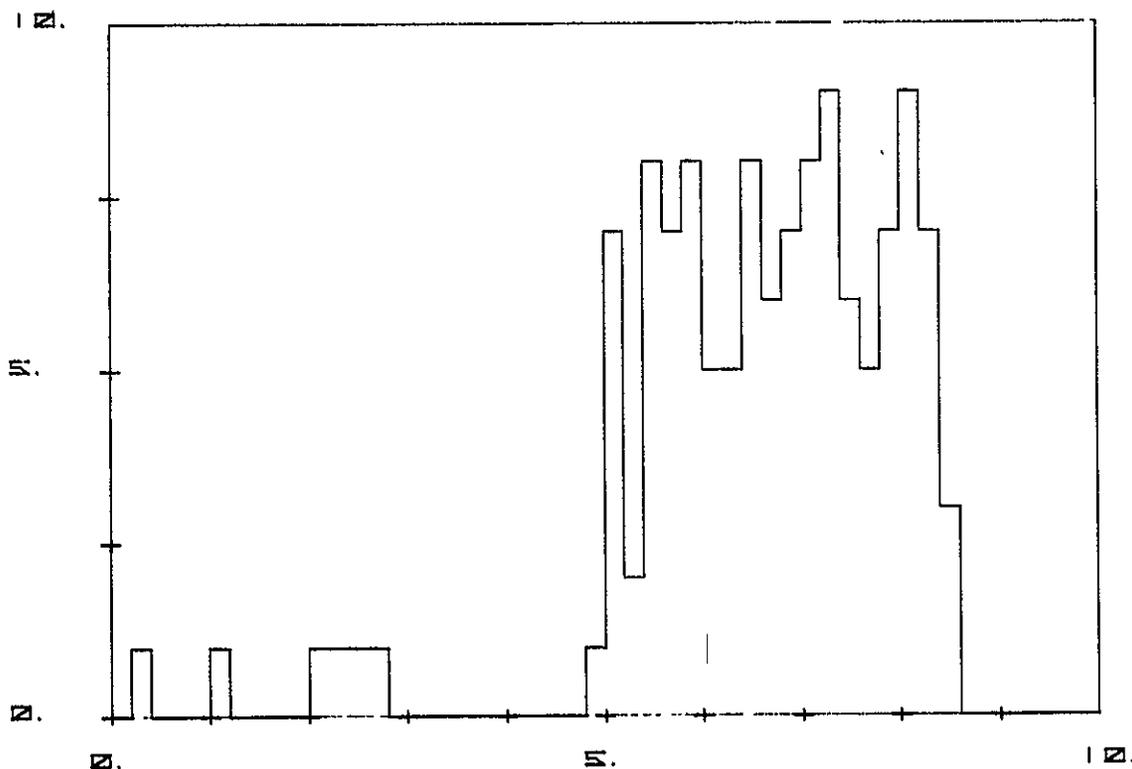
N_{TOTAL} = 124.

$N_{T>10}$ = 0.

MEAN = 6.560 SEC

VAR = 2.172 SEC²

STD DEV = 1.474 SEC

A-15

Figure A-14. Acquisition Time Data

CODE = 14.099540 MHZ   CARRIER = 109.770 MHZ   SNR = 51. DB
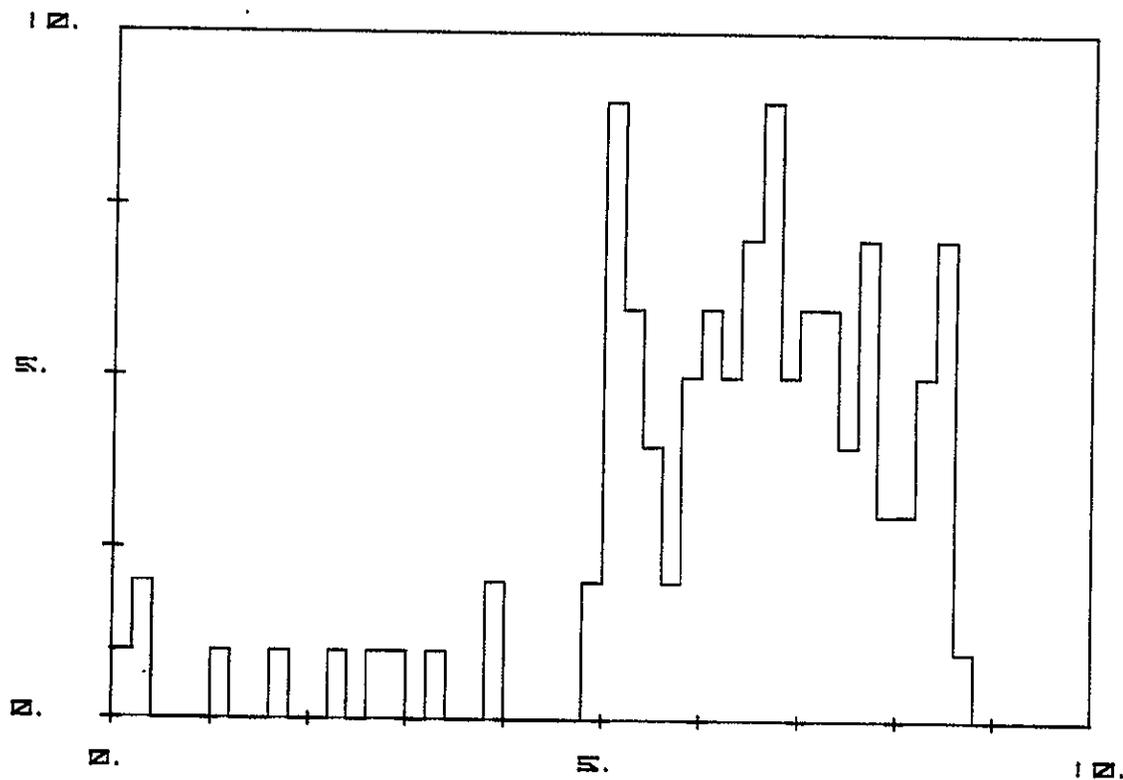
N_{TOTAL} = 113.

$N_{T>10}$ = 0.

MEAN = 6.275 SEC

VAR = 3.169 SEC^2

STD DEV = 1.780 SEC

Figure A-15. Acquisition Time Data

-1 DB AGC

CODE = 14.100000 MHZ   CARRIER = 110.000 MHZ   SNR = -7. DB

N_{TOTAL} = 141.

$N_{T>10}$ = 0.

MEAN = 2.264 SEC

VAR = 1.638 SEC^2

STD DEV = 1.280 SEC

A-17
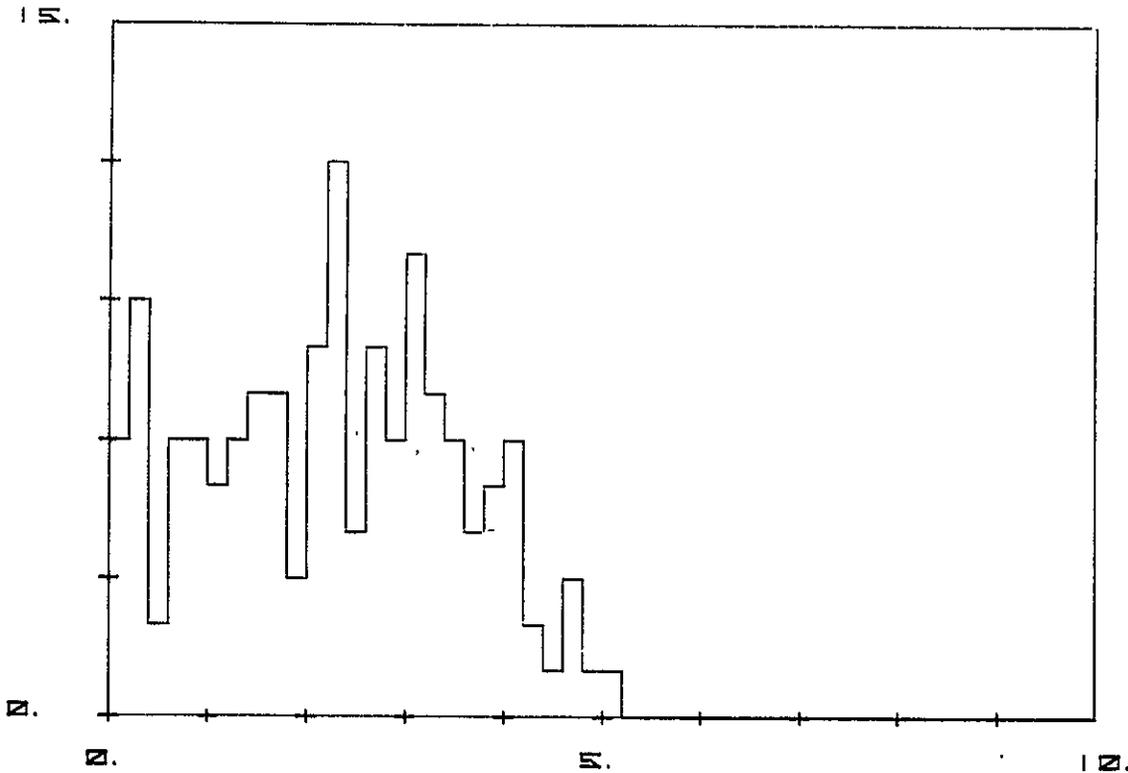
Figure A-16. Acquisition Time Data

+1 DB AGC

CODE = 14.100000 MHZ   CARRIER = 110.000 MHZ   SNR = -7. DB

N_{TOTAL} = 162.

$N_{T>10}$ = 0.

MEAN = 2.393 SEC

VAR = 1.439 SEC^2

STD DEV = 1.200 SEC

Figure A-17. Acquisition Time Data

APPENDIX B

BPSK $\overline{T_{ACQ}}$ HISTOGRAMS

A set of acquisition time measurements for the BPSK mode were made prior to acceptance testing. Histograms (Figure B-1 through B-10) showing the distribution of times were made for each specified set of signal conditions. Table B-1 provides a summary of the average values for acquisition time.

Additionally, Figure B-10 shows the results of 1204 acquisition time measurements for minimum SNR and 0 Doppler. The histogram shows a fairly even distribution out to the time required for one complete code search. There is then a sharp drop-off, followed by a second nearly even distribution to the time required for a second full word search. The drop-off and second level distribution are a result of P_D being less than unity. The P_D calculated form the histogram is 0.95.

Table B-1. $\overline{T_{ACQ}}$ Summary for BPSK (Seconds)

Doppler SNR	-15 dB	-10 dB	-2 dB
Maximum Positive Doppler	2.48	0.84	0.84
0 Doppler	1.16	1.38	1.21
Maximum Négative Doppler	4.55	2.84	3.34

CODE = 14.100460 MHZ   CARRIER = 110.450 MHZ   SNR = -15. DB

N_{TOTAL} = 111.

$N_{T>10}$ = 3.

MEAN = 2.482 SEC

VAR = 6.293 SEC^2
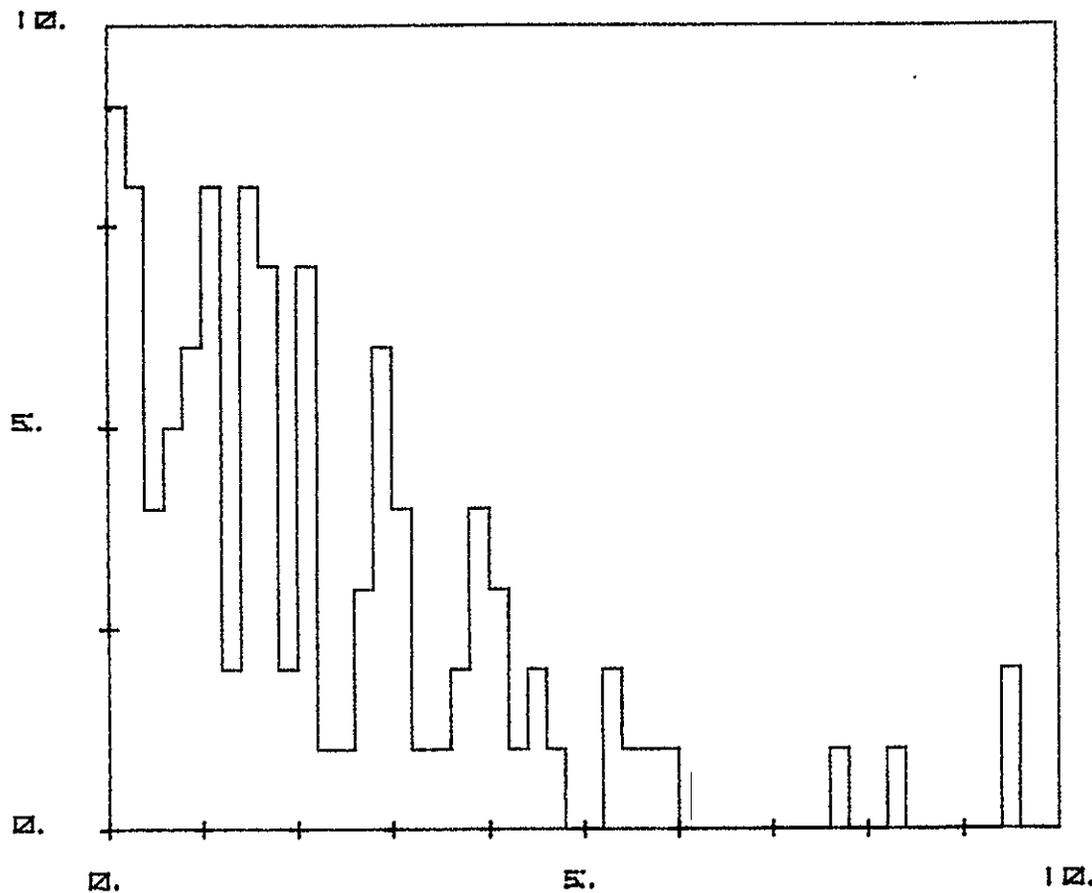
STD DEV = 2.509 SEC

Figure B-1.   Acquisition Time Data

CODE = 14.100460 MHZ   CARRIER = 110.450 MHZ   SNR = -10. DB
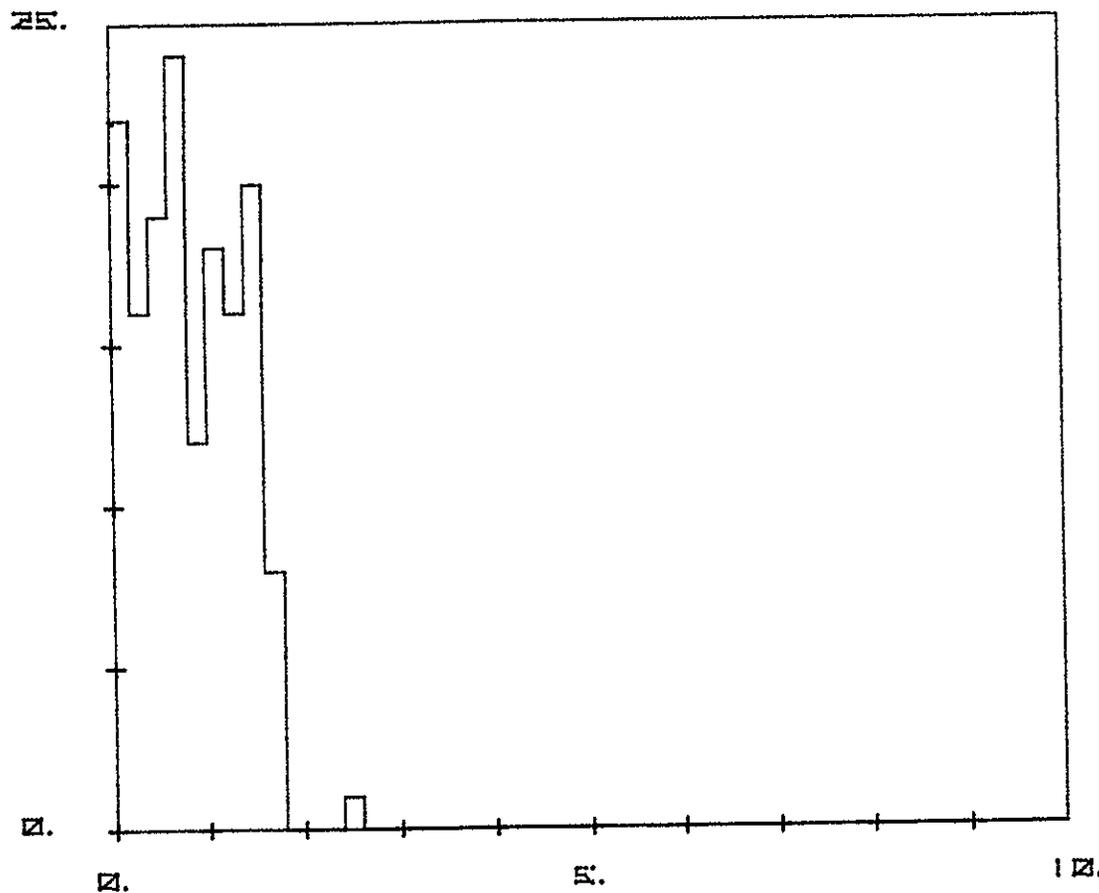
N TOTAL = 890.

N T>10 = 734.

MEAN = 0.840 SEC

VAR = 0.260 SEC²

STD DEV = 0.510 SEC

Figure B-2. Acquisition Time Data

CODE = 14.100460 MHZ   CARRIER = 110.450 MHZ   SNR = -2. DB
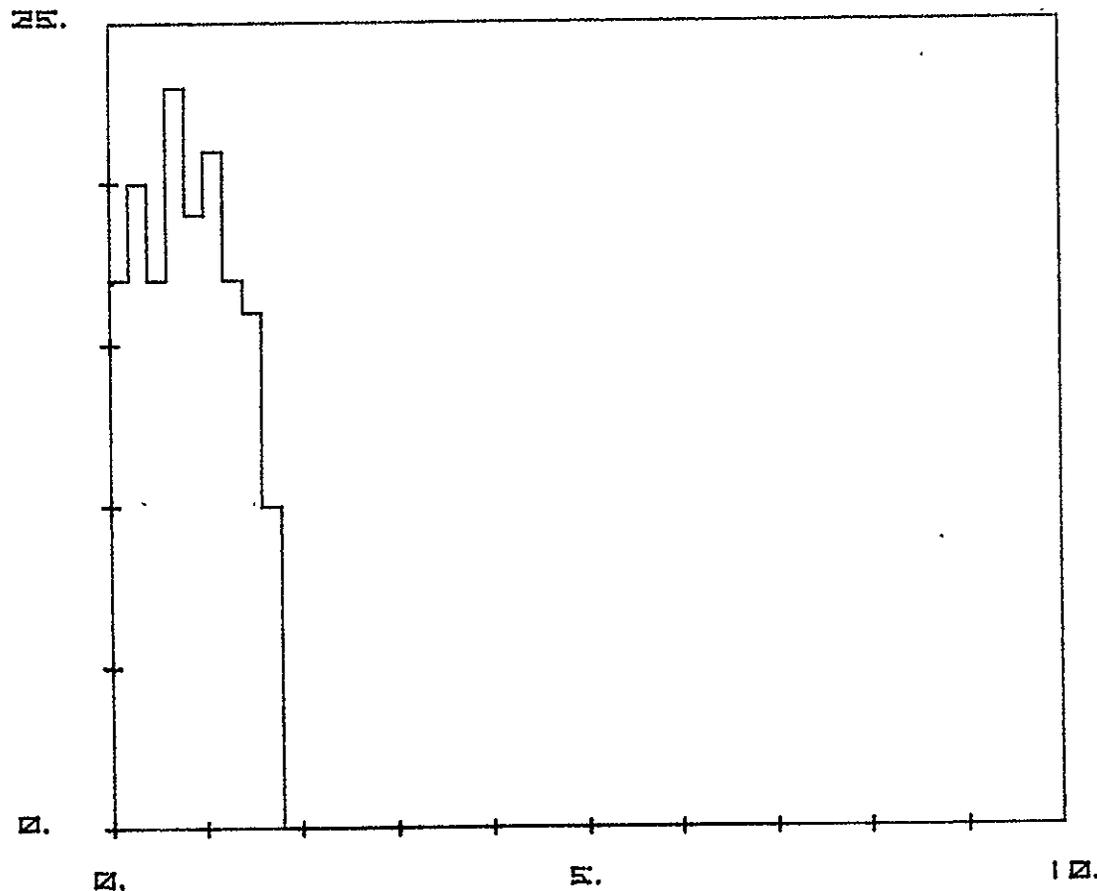
N_{TOTAL} = 150.

$N_{T>10}$ = 0.

MEAN = 0.839 SEC

VAR = 0.226 SEC^2

STD DEV = 0.476 SEC

Figure B-3. Acquisition Time Data

CODE = 14.100000 MHZ   CARRIER = 110.000 MHZ   SNR = -15. DB
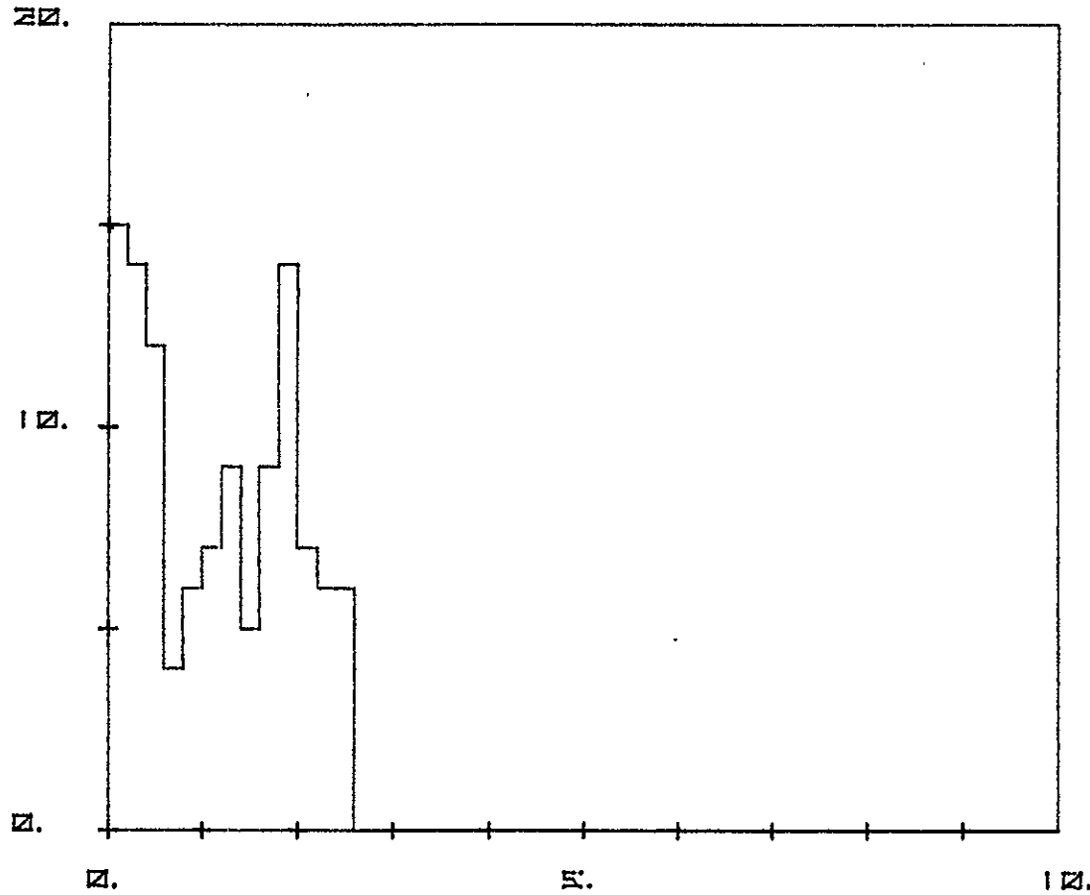
N_{TOTAL} = 114.

$N_{T>10}$ = 0.

MEAN = 1.164 SEC

VAR = 0.614 SEC^2

STD DEV = 0.784 SEC

Figure B-4. Acquisition Time Data

CODE = 14.100000 MHZ   CARRIER = 110.000 MHZ   SNR = -10. DB
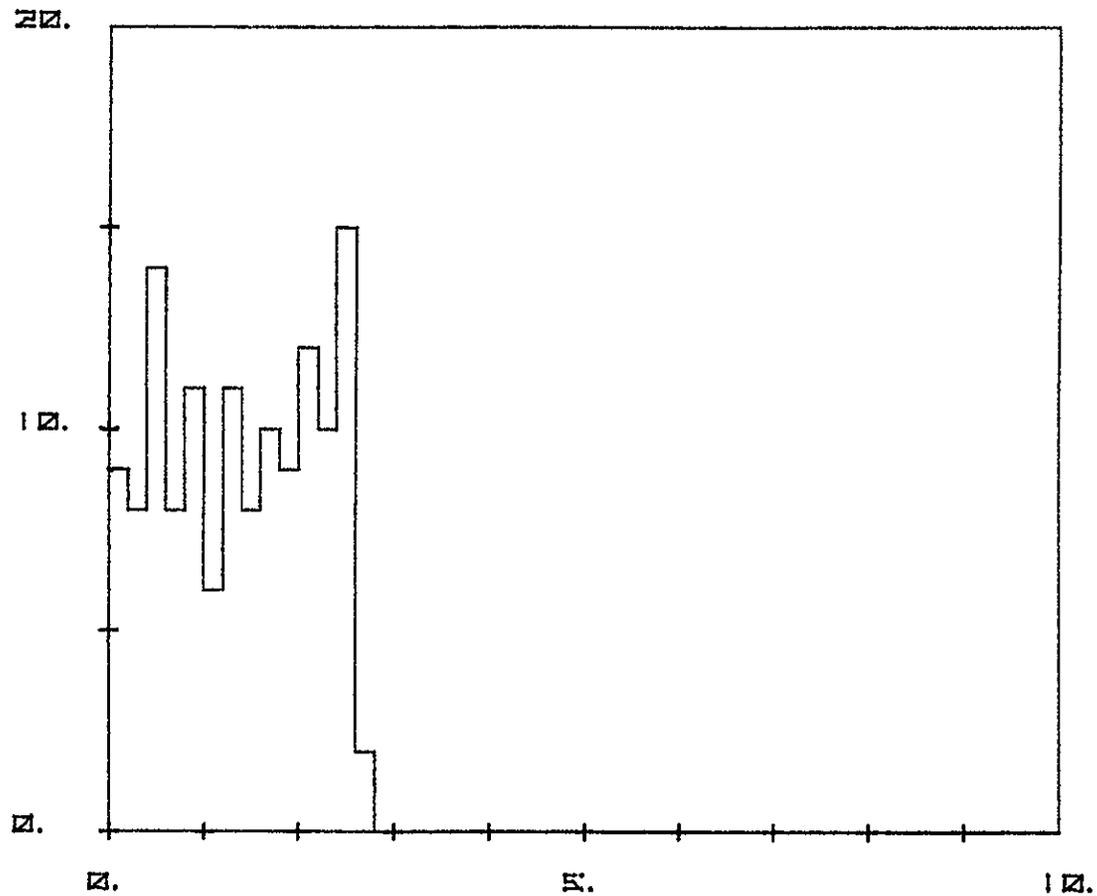
N_{TOTAL} = 133.

$N_{T>10}$ = 0.

MEAN = 1.383 SEC

VAR = 0.609 SEC^2

STD DEV = 0.781 SEC

Figure B-5. Acquisition Time Data

CODE = 14.100000 MHZ   CARRIER = 110.000 MHZ   SNR = -2. DB
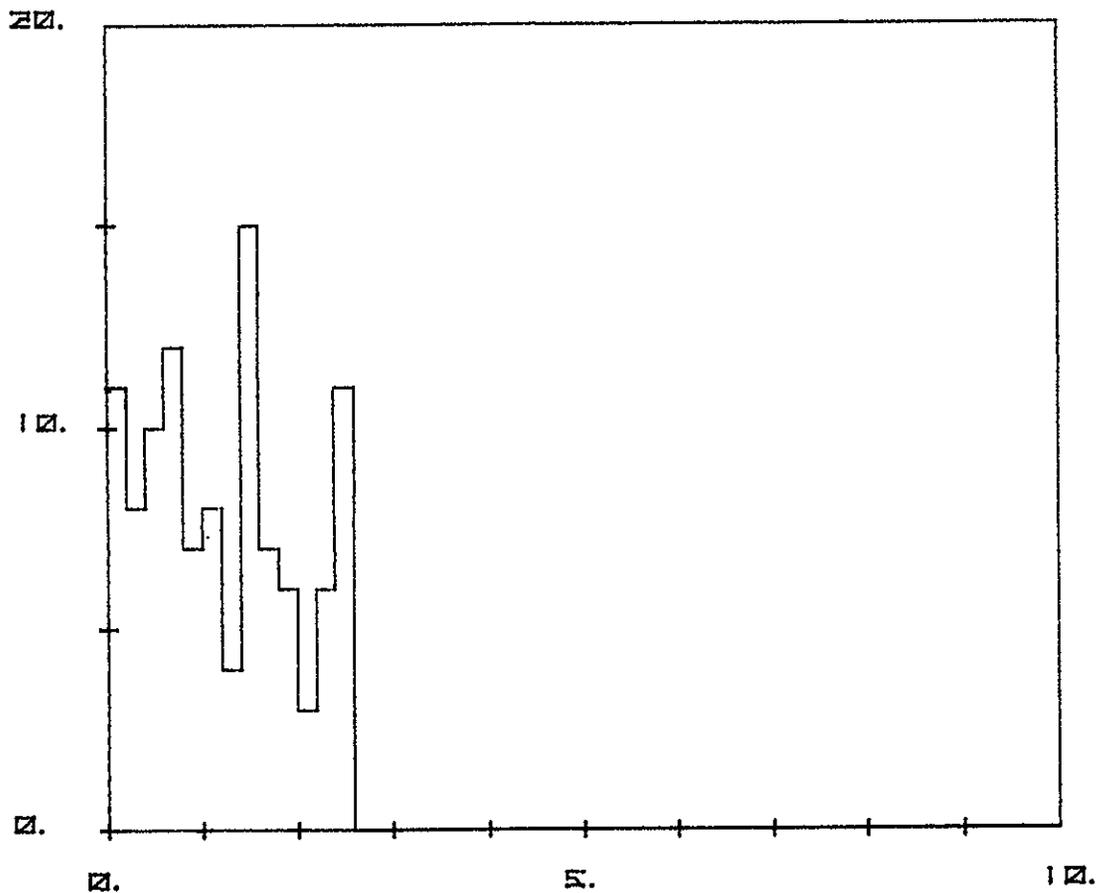
N_{TOTAL} = 108.

$N_{T>10}$ = 0.

MEAN = 1.207 SEC

VAR = 0.595 SEC^2

STD DEV = 0.771 SEC

Figure B-6. Acquisition Time Data

CODE = 14.099540 MHZ   CARRIER = 109.550 MHZ   SNR = -15. DB
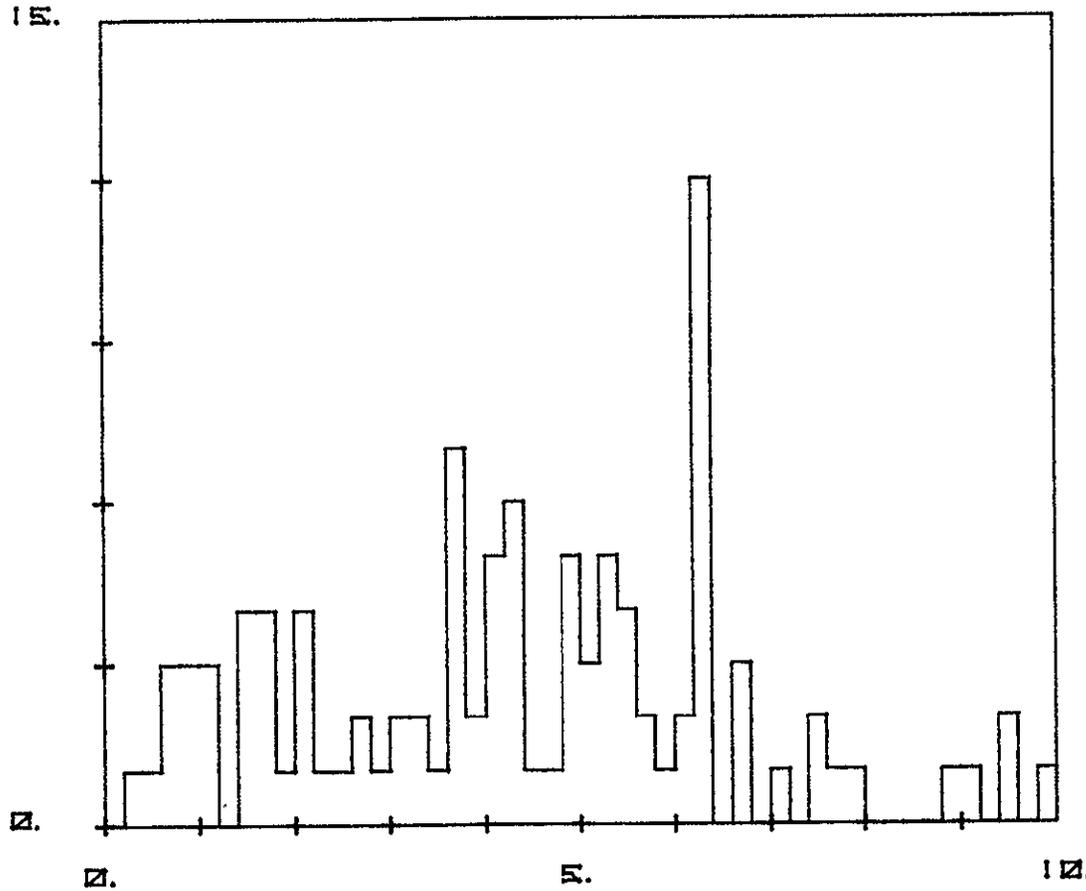
N_{TOTAL} = 109.

$N_{T>10}$ = 3.

MEAN = 4.550 SEC

VAR = 6.288 SEC^2

STD DEV = 2.508 SEC

Figure B-7. Acquisition Time Data

CODE = 14.099540 MHZ   CARRIER = 105.550 MHZ   SNR = -10. DB
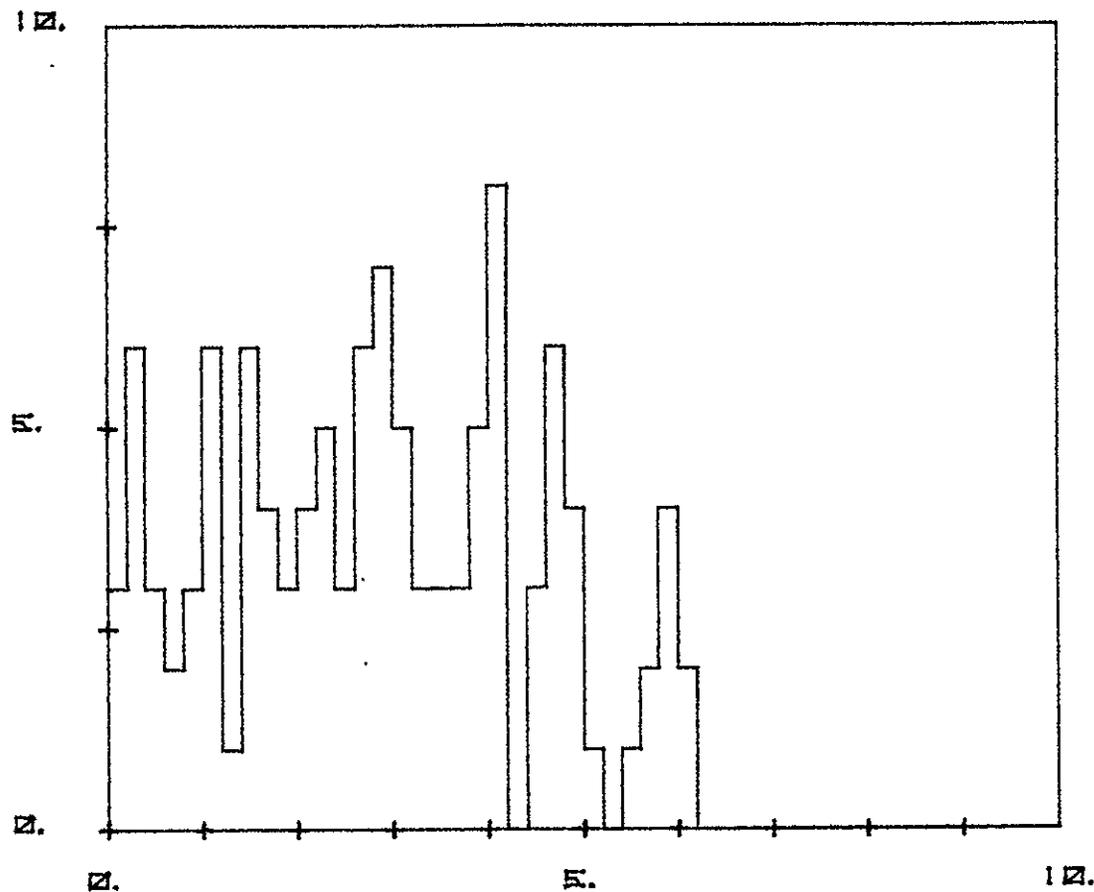
N_{TOTAL} = 112.

$N_{T>10}$ = 0.

MEAN = 2.841 SEC

VAR = 2.701 SEC^2

STD DEV = 1.643 SEC
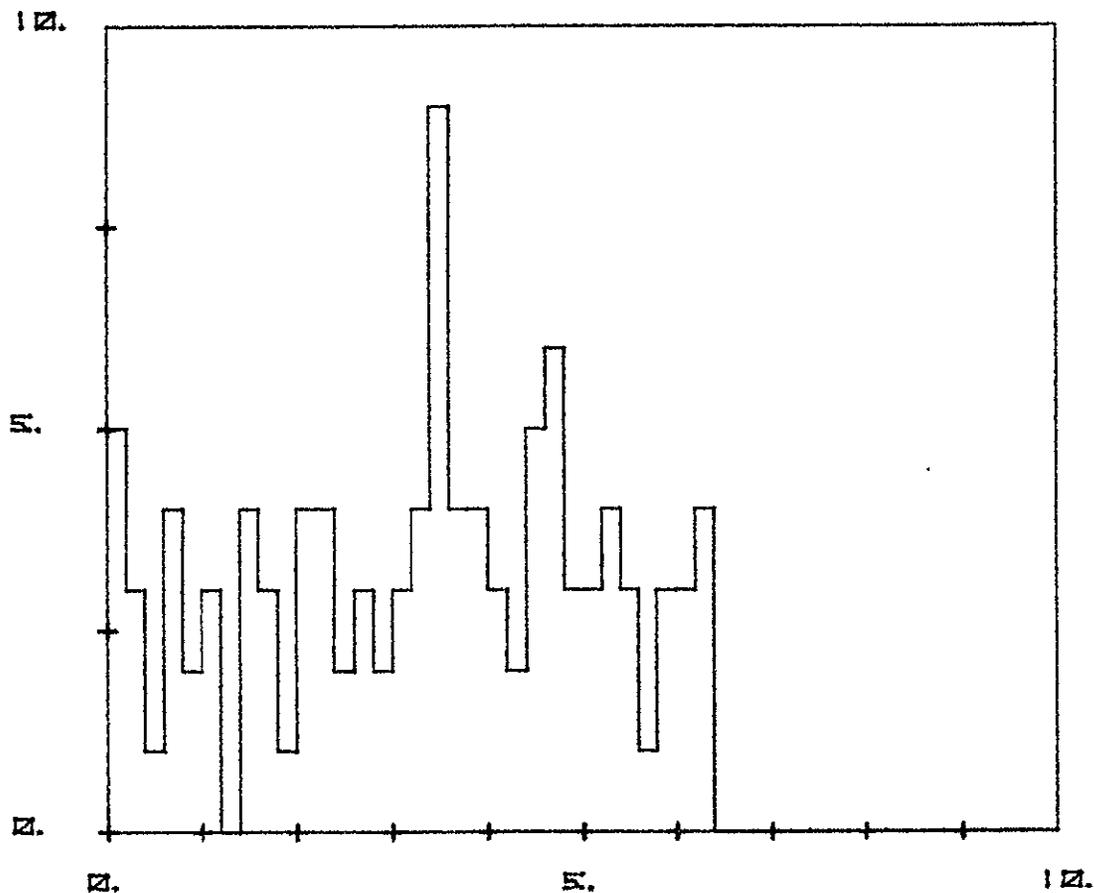
Figure B-8. Acquisition Time Data

Figure B-9. Acquisition Time Data

CODE = 14.100000 MHZ   CARRIER = 110.000 MHZ   SNR = -15. DB
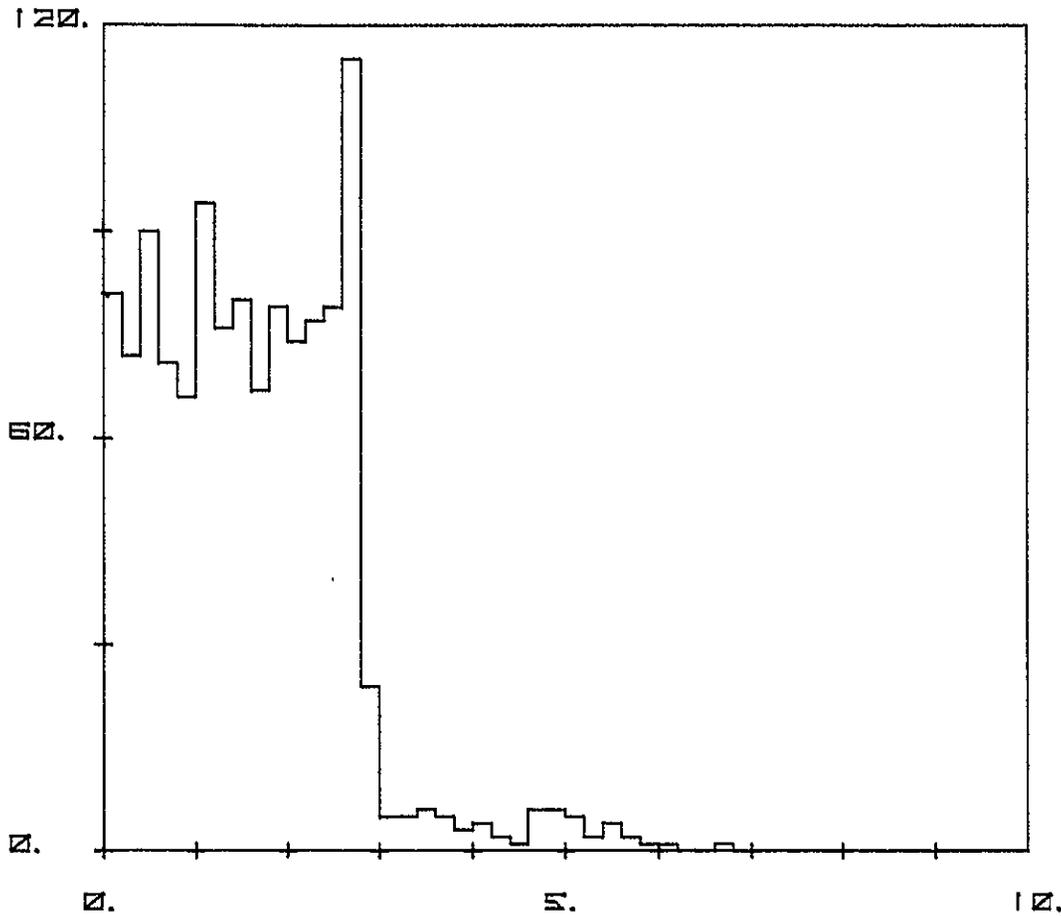
N_{TOTAL} = 1204.

$N_{T>10}$ = 0.

MEAN = 1.614 SEC

VAR = 1.127 SEC^2

STD DEV = 1.062 SEC

Figure B-10. Acquisition Time Data

APPENDIX C

ACQUISTION THRESHOLD

The need for using a "dynamic" threshold was demonstrated by the results of experiments performed during the design phase of this program. Correlation measurements for a noise-cluttered PN code were simulated for the 72 kbps and 3 Mbps data rates. The measurements showed wide variation of the correlation peaks caused by SNR and AGC levels. Figure C-3 illustrates the utility of the normalization process selected for use in the despreader. For these graphs V_{det} is the detector output for a correlated signal plus noise, and V_{ref} is the output for an uncorrelated signal plus noise.

C.1 TEST RESULTS

Point-by-point measurements of detector output versus code phasing were made in quarter-chip steps to 1-1/2 or 1-3/4 chips on either side of perfect correlation and in half-chip steps out to 3 or 3-1/2 chips. Measurements made using frequencies which simulate the high data rate system yielded data proving such a system unfeasible. The output of the square-law detector versus code phasing is plotted in Figure C-1a) and the normalized output versus phasing is plotted in Figure C-1b). Both are for an SNR of about 2 dB (i.e., 6 dB above minimum). Even with normalization (output scaled by the uncorrelated reference and translated about zero), the detector signal would not be a suitable correlation indicator for the high data rates since one would have to be within about 1/8 chip before one were able to distinguish code correlation. Furthermore, one has to detect a correlation peak of only about 3 percent.

Alternatively, the lower data rate can be used for code acquisition. Because of a higher processing gain, the lower rate yields a higher SNR in the post-correlation bandwidth. Figure C-2 shows graphs of the detector output versus phasing for several different SNR's, and Figure C-3 illustrates the normalized data. Specifically, Figure C-3b) demonstrates

the superiority of the low data rate for code acquisition at the lowest specified SNR, and Figure C-3a) shows that a significant signal is still obtained with 2 dB less signal. Data was taken with no noise. The results were very similar to the SNR = +11 dB data since in both cases, the signal power dominates the measurements .
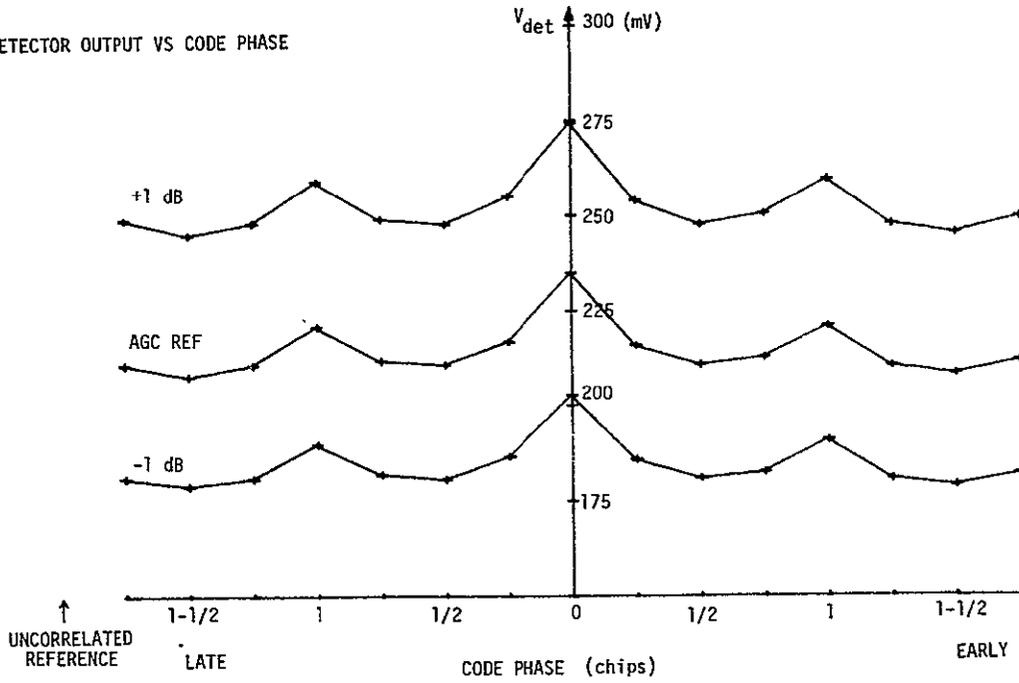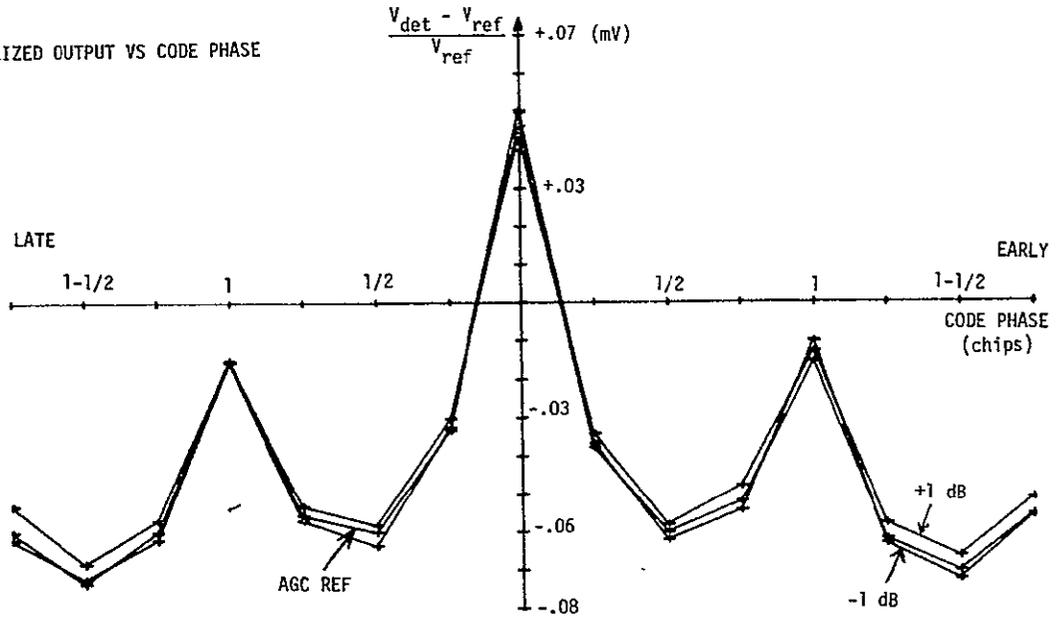
Figure C-1. Typical Results for High Data Rate, S/N ~ 2 dB

Figure C-2. Detector Output Versus Code Phase for Low Data Rate

(A) S/N = -1 dB

$$\frac{V_{det} - V_{ref}}{V_{ref}}$$

Figure C-3. Normalized Output Versus Code Phase for Low Data Rate

C-5