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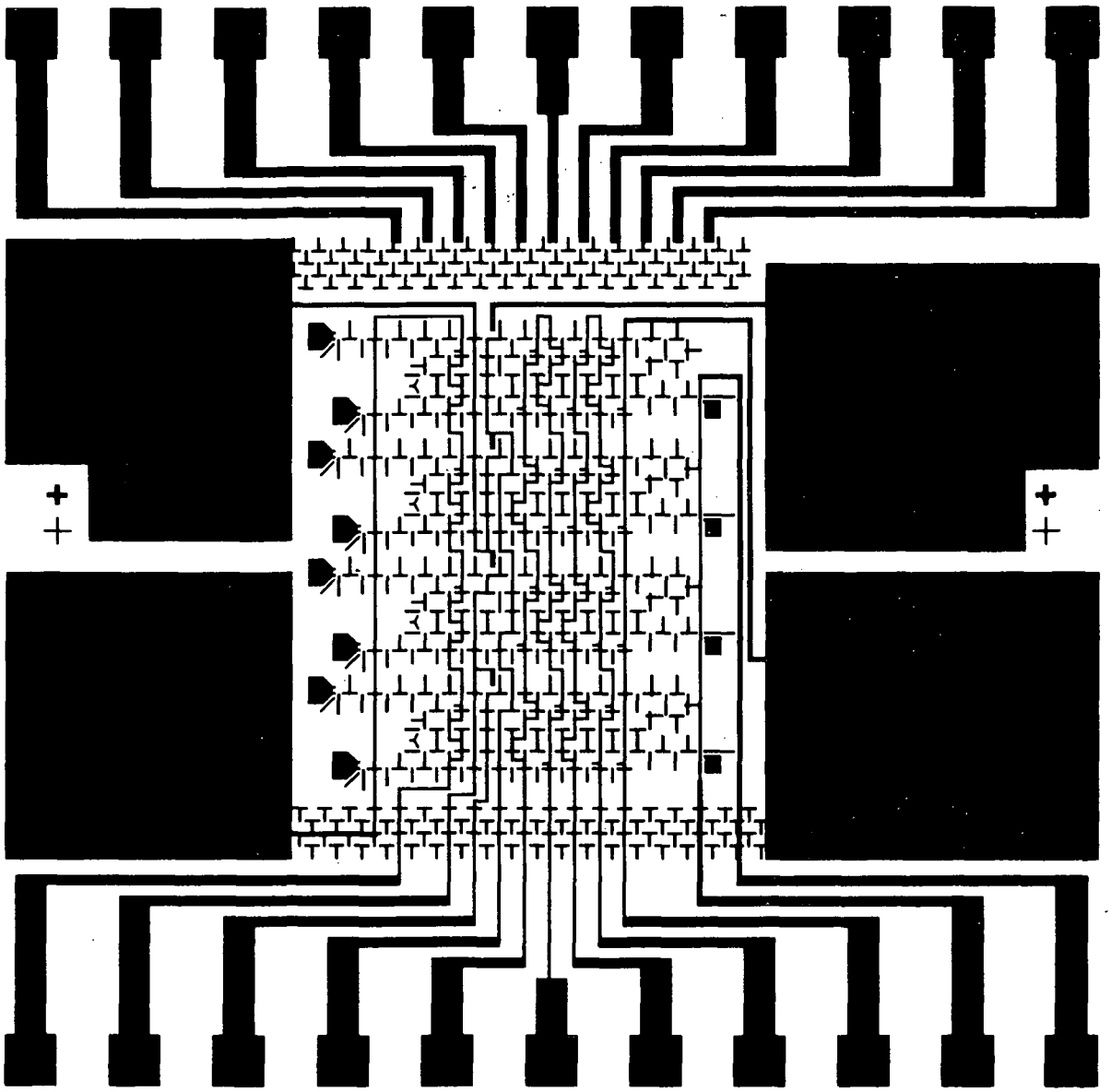
Conceptual Design of a 10^8-Bit Magnetic Bubble Domain Mass Storage Unit and Fabrication, Test and Delivery of a Feasibility Model

FINAL REPORT–

Contract No. NAS 8-26671



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Approved By R. T. Grimmer

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ABSTRACT

The first part of this report describes the conceptual design of a highly reliable 10^8-Bit Bubble Domain Memory for the Space Program. The Memory has random access to blocks of closed-loop shift registers, and utilizes self-contained bubble domain chips with on-chip decoding. Trade-off studies show that the highest reliability and lowest power dissipation is obtained when the memory is organized on a bit-per-chip basis. The final design has 800 bits/register, 128 registers/chip, 16 chips/plane, and 112 planes, of which only seven are activated at a time. A word has 64 data bits +32 checkbits, used in a "16-adjacent" code to provide correction of any combination of errors in one plane. 100 KHz maximum rotational frequency keeps power low ($\leq$ 25 watts) and also allows asynchronous operation. Data rate is 6.4 megabits/sec, access time is 200 μsec to an 800-word block and an additional 4 msec (average) to a word.

The second part of this report describes the fabrication and operation of a 64-bit bubble domain memory chip designed to test the concept of on-chip magnetic decoding. Access to one of the chip's four shift registers for the read, write, and clear functions is by means of bubble domain decoders utilizing the interaction between a conductor line and a bubble. All other functions are performed by a permalloy overlay driven by an external rotating field. The metallurgy consists of 200 Å evaporated permalloy for magnetoresistive sensors, 4000 Å electroplated permalloy for propagation etc., and 6000 Å electroplated copper for control lines. Chip operation was achieved for 15 Oe minimum rotating field and 30mA minimum control current. A sense signal of 0.2mV was obtained for 2mA input current and 11-μm diameter bubbles in an epitaxial garnet film.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

SECTION 1: CONTRACTUAL WORK REQUIREMENTS

The basic work requirements of this contract were a conceptual design, a program plan, and a feasibility model for a 10^8-bit Mass Storage Unit employing Magnetic Bubble Domain [BFPRV 69]* technology. The storage unit was to be designed for on-board use as a buffer memory in a space application such as Space Shuttle.

The conceptual design was to include trade studies covering systems architecture, error detection/correction, fault isolation, packaging approaches, and redundancy. The storage unit was to be designed to minimize size, power, and weight, and to maximize reliability, maintainability, and speed. The memory design was to be capable of satisfactory operation when exposed to the environments expected for space applications such as Space Shuttle (i.e., launch vibration, temperature, acoustics, RFI (radio frequency interference), shock, vacuum, and radiation).

The program plan was to outline how a follow-on design, development, fabrication, testing, and delivery of a full 10^8 bit breadboard unit could be accomplished within a fourteen month period.

A feasibility model of the designed mass storage system was to be fabricated, tested, and delivered to the Marshall Space Flight Center for evaluation. The model was to be limited in capacity to that necessary to prove feasibility of the approach used in the conceptual design.

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*Terms in square brackets refer to items in the Bibliography, Section 7.

SECTION 2: SUMMARY OF ACCOMPLISHMENTS

The design approach chosen to satisfy the contractual requirements was the use of self-contained bubble domain chips with on-chip decoding [CFLR70]. In this approach, the information on the memory chip is stored serially in a group of closed-loop shift registers, and random access is provided to any one of the registers by an on-chip magnetic decoder which utilizes the interaction between a bubble domain and a current-carrying conductor. In this way, n control lines can select one of 2^n shift registers.

Of the many organizations possible in expanding the on-chip decoding concept into a design for a 10^8-bit memory, three were studied in detail: bit-per-shift register, bit-per-plane, and bit-per-chip. The first allows the use of same-chip bubble domain logic devices for error correction, but has the highest vulnerability to failures. The second dissipates the most power. The bit-per-chip organization has the best overall reliability of the three, results in a reasonable power dissipation and became the recommended design. The operating characteristics of this conceptual design are summarized in Table 2.1.

The program plan has already been delivered [AGL71] under separate cover.

TABLE 2.1

CHARACTERISTICS OF THE BIT-PER-CHIP DESIGN OF THE 10^8-BIT MEMORY

Capacity: 1.6×10^6 words of 64 data bits each

Rotational frequency: 100 KHz (for low power)

Data rate: 6.4×10^6 bits/sec.

Access time: 0.2 msec to a block of 800 words

4 msec to a word

Weight: 27.4 lbs.

Power: 22.2 watts

Ultimate 24-month reliability: 92%

The feasibility model is intended to demonstrate the operability of the conceptual design. The operations necessary to perform the functions of the memory chip are:

Bubble Generation

Straight-line propagation

Cornering

Joining two paths into one (junction)

Bubble annihilation

These are all performed using a permalloy overlay driven by a rotating magnetic field (field-access operation [P69]), and are basic to the operation of the shift registers. To select one of the 2^n shift registers, write information into it, and clear that information out again, it is further necessary to be able to route a bubble along one of two possible paths in such an environment using a current-controlled switch. Finally, a sensing means is necessary to read out the information stored in the selected register.

To demonstrate these functions, a small four-register memory was designed, fabricated, and tested using $\sim$10μm bubbles in an epitaxial garnet film. Its operation is summarized in Table 2.2.

TABLE 2.2

MEASURED OPERATING CHARACTERISTICS OF FEASIBILITY MODEL

Bubble Material:	$Eu_{0.7}\ Y_{2.3}\ Fe_{3.8}\ Ga_{1.2}\ O_{12}$ film
Bubble Diameter:	11μm
Minimum Rotational Fields required for	
Straight Line Propagation:	10 Oe*
Corners and Junction:	13 Oe
Generators:	14 Oe
Annihilators:	< 10 Oe
Switches (25 mA control current):	15 Oe
Magnetoresistive sensor signal	
for 2mA input current:	200 μV

The conceptual design and the feasibility model will both be described in considerably more detail in Sections 3 and 4. It should be pointed out for those who are perhaps not interested in all the details of this report that a concise but comprehensive extract from this report treating the feasibility model and the conceptual design was published at the 17th Conference on Magnetism and Magnetic Materials as papers 4F3 and 4F4 [ACGHHJKPR71], [ABC71], which are reproduced in Appendix H for the reader's convenience.

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* 1 Oersted (Oe) = 80 Amperes/meter

SECTION 3: CONCEPTUAL DESIGN OF 10^8 BIT MSU

This section describes the conceptual design of the 10^8-bit bubble domain mass storage unit. The design principles will be discussed first (Section 3A), covering Chip and Module Design, System Design, Electrical and Mechanical Design, and Error Correction and Detection. This is followed in Section 3B by an evaluation of the conceptual design, covering the Calculated Operating Characteristics, Reliability Analysis, and Tradeoffs.

3A1 SYSTEM DESIGN-GENERAL

The system was designed to be used in a block-oriented mode, in which random access is provided to blocks of information, which are then read out or written in serially. Physically, this means that the bubble domain chip is divided into a number of closed-loop shift registers which store the blocks of information. Random access to these shift registers is provided by on-chip magnetic decoders which utilize the interaction between bubble domains and current-carrying conductors. The propagation in the shift registers, which occupy the major portion of the chip, is accomplished with a magnetic overlay pattern activated by an external rotating field. This concept was first set forth by Chang et al. [CFLR 70], who referred to it as a "self-contained bubble domain memory chip."

The further organization of such chips into a memory system depends on a number of design criteria. Since the application contemplated here was on-board use in a spacecraft, low weight, low power, and high reliability were at a premium. In addition, the memory must be able to survive the launch and space environments. Nevertheless, the design should be reasonably consistent with economical commercial prodcution: the chip design should give reasonable chip yields, the package should be reasonably easy to manufacture, and the means for obtaining the required reliability should not be a prohibitively expensive fraction of the total memory. These topics are considered in the next several sections, followed by a more detailed discussion of several specific system designs. The one remaining task of this section is to specify the access time and data rate of the memory. After examining present and future needs of the space program, it was decided to aim for average access times below 5×10^{-3} sec and data transfer rates of at least 5×10^{6} bits/sec. The next few sections describe the influence of these requirements on the evolution of the design.

3A2 CHIP, MODULE, AND PAGE DESIGN

3A2.1 Chip Size

It is desirable to have as many bits per chip as possible, consistent with a reasonable chip yield. In addition, high speed and low cost are both easier to obtain as the density of information storage (bits/square inch) is increased. These are the primary considerations in choosing the size of the chip.

Based on our fabrication experience so far (Sec. 4A2) and on progress in the industry, it seems reasonable for the 1972-1975 time frame to assume that overlay patterns with 0.0001" (2.5 μm) minimum linewidths w will be practical [B71]. Assuming that a bit of information requires a storage area of $40w^2$, this corresponds to a storage density of $\sim 2.5 \times 10^6$ bits/square inch. For an effective defect density of 100/square inch, a chip 0.2" x 0.2" (0.5cm x 0.5cm) has a yield of 37% and contains 10^5 bits of information (see Appendix A). The chip should be about this size.

3A2.2 Separate vs. Integrated Overlay

At one time, it was thought that defect-free overlays would be much easier to fabricate than defect-free bubble domain materials, in which case it would make sense to use a number of smaller bubble domain chips in conjunction with one common large separate overlay. Progress in epitaxial garnet film fabrication [N71] has brought about the opposite situation - defect counts less than 30/square inch are available on what appears to be a routine basis, whereas mask defects for 0.0001" lines are on the order of 100/sq. inch. In this case, separate overlays are economically justifiable only if the overlays are much more expensive per unit area than the epitaxial films. There is no obvious reason why this should be so. (The opposite approach, of having several small separate overlays on a large bubble domain chip, would encounter severe inter-

connection problems.)

Furthermore, the spacing between the overlay and the bubble domain material is very critical, (on the order of several thousand angstroms (Å) for 4μm bubbles) and is rather difficult to maintain with the separate overlay approach. In view of these considerations, it was decided to design a chip with an "integrated" overlay, that is, an overlay whose permalloy and conductor patterns have been deposited directly onto a spacer layer which was previously deposited directly onto the epitaxial garnet bubble domain material. as in the work of Ahn et al. [AHPRS 71]. However, the electron-beam fabricating technique described there should not be necessary here, since 2.5μm lines are still well within the capabilities of photolithographic technology.

3A2.3 Bubble Domain Material

The bubble diameter should be about 4μm to match the 2.5μm linewidths, and the mobility should be at least 100-200 cm/(Oe-sec) to allow 100 KHz operation. One such suitable garnet material is the $Eu_{0.7}\ Y_{2.3}\ Fe_{3.8}Ga_{1.2}\ O_{12}$ composition used for the feasibility model; a small change in Ga concentration will bring the bubble diameter down to 4μm from the 12μm used for the feasibility model [Sec. 4A]. Growth of such films has been described by Giess et al. [GACKMOPS 71], among others.

3A2.4 Chip Layout

The chip layout is rather uniquely determined by the average access time which the system is to have. Except for some relatively small decoder delays, the average access time $\bar{T}_A$ is given by

$$\bar{T}_A = 1/2B_{sR}\ T_R$$

where B_{sR} is the number of bits per shift register and T_R is the time period of one field rotation. The rotational frequency will be chosen to be

100 KHz to allow low-power and variable-speed operation, as described in the following sections on module design and also in Appendix B. Hence, $T_R = 10^{-5}$ sec. It was stated in Sec.3A1 that $\bar{T}_A$ should be less than 5×10^{-3} sec. Hence, B_{SR} must be less than 1000 bits, which would mean that a 10^5 bit chip would have 100 shift registers. A binary number of shift registers is more convenient for the on-chip decoding approach used here, and so the final chip design calls for 128 shift registers of 800 bits each, for an average access time of 4×10^{-3} sec plus a small additional amount of decoder and other additional delays, the exact value of which will be determined later.

The chip layout is shown schematically in Fig. 3A2-1. This is basically a scaled-up version of the feasibility model chip whose fabrication and operation are described in detail in Section 4. As already mentioned, the assumed line-width is 10^{-4} inch (2.5μm), corresponding to a bit density of 2.5×10^6/sq.inch. Each of the 128 closed-loop shift registers has a write decoder and a read decoder section. The number of steps and corresponding control lines in the decoder sections depends on the exact memory organization (Sec 3A5), which determines how many shift registers are being chosen among. For the bit-per-chip organization, which will be shown to be the preferred design, there are seven such decoder control lines per chip ($2^7 = 128$). These decoders select one of the 128 registers on the chip for write-in, read-out, or clear-out. Instead of a sensor per shift register, as in the feasibility model, each register has a bubble splittler (Fig. 3A2-2), from which one bubble re-enters the storage loop, while the other enters a 16:1 bubble fan-in leading to a magnetoresistive sensor. Thus, only 8 sensors (series-connectable) are required per 10^5-bit chip. The bubble fan-in consists of 16 paths converging on the sensor (Fig. 3A2-2). The path delays can be made equal (0.5 msec) by placing more undulations in some paths than others. It may be possible to

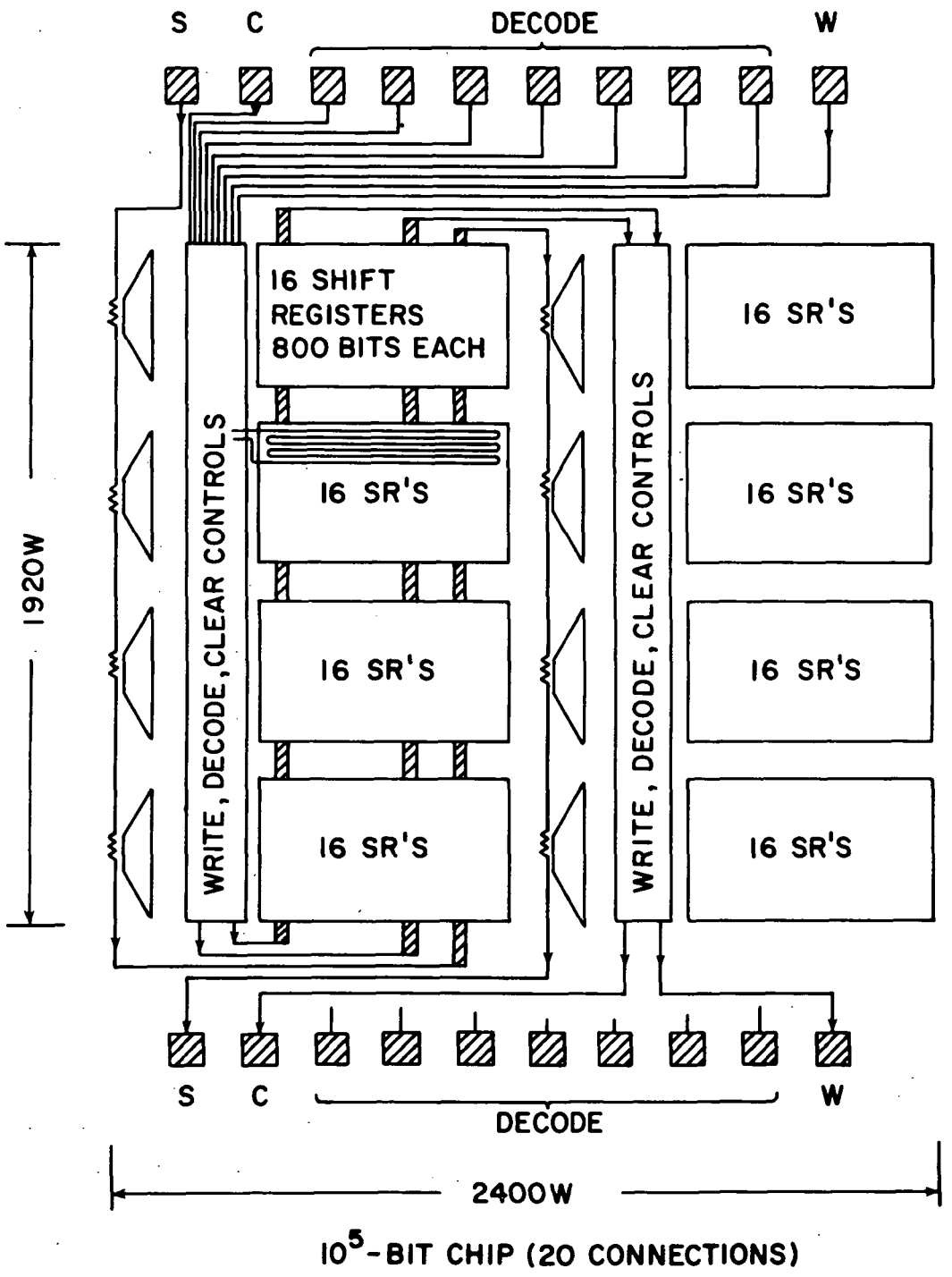


Fig. 3A2-1 Chip Layout (W = .0001" = 2.5μm)

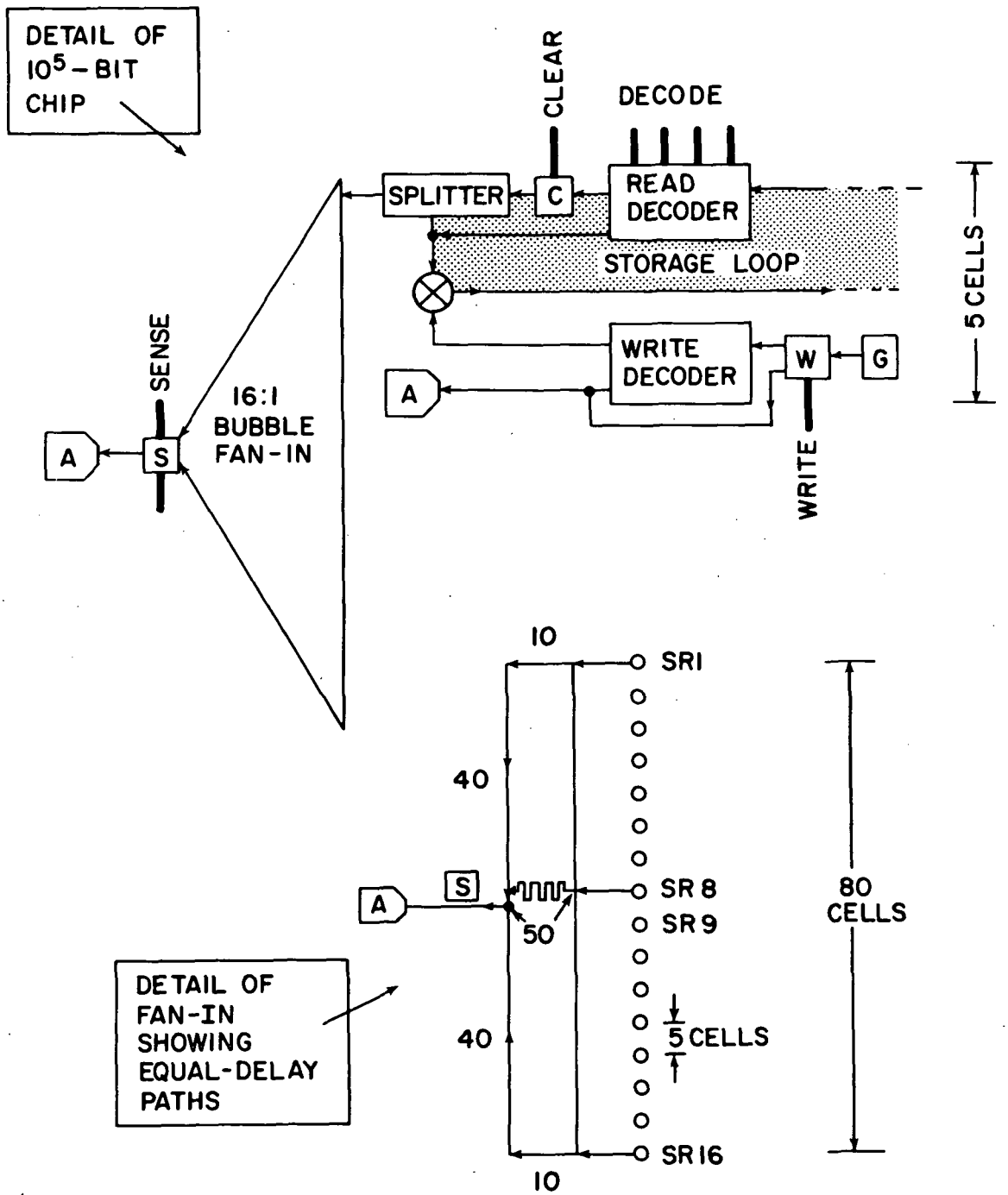


Fig. 3A2-2 Details of 10^5-Bit Chip

eliminate this delay by modifying a bubble compressor [BDKS 70] to accept 16 inputs.

The relative areas occupied by each function on the chip break down as follows: First, a "cell" is defined as the product of the vertical and horizontal periods in the storage section of the shift register. In the layout of Fig. A1 of Appendix A, this value is 5w x 8w or $40w^2$, where w = .0001" or 2.5μm. Since the storage section of each shift register is folded three times, it occupies an area of (6x5w) x ($\frac{800}{6}$ x 8w) = 32,000 w^2 = 800 cells. By comparison, the decoders occupy (6 x 5w) x (7 x 8w) = 1680 w^2 = 42 cells (see Appendix C, "A Compact Decoder for Bubble Domain Memories"), and if the fan-in of Fig. 3A2-2 is used, the fan-in section of each register occupies (6 x 5w)x (10 x 8w) = 2400 w^2 = 60 cells (a bubble compressor-type fan-in would occupy 10 to 20% of this area). Thus the storage occupies $\frac{800}{800+42+60}$ = 89% of the chip area, the decoding occupies $\frac{42}{902}$ = 4.6%, and the fan-in occupies $\frac{60}{902}$ = 6.4%. Except for the sensors, which occupy negligible space, the chip active area is thus 128 registers x 902 cells/register x $40w^2$/cell = 4.6 x $10^6 w^2$= .046 sq. inch = 0.29 cm^2. The proportions of the chip are 1920w high x 2400 w wide, or .192" x .240", or .49cm x .61 cm.

Several other details of the chip layout should be pointed out; in the active area of the decoder sections, the control line width is equal to a T-bar width, or .0001" (2.5μm). After coming in the top of the chip and passing through the decoders of the first 64 registers, the lines are broadened to perhaps as much as 100μm to reduce their resistance and effective field and proceed back to the top of the chip, crossing the storage portions of the first 64 registers enroute (see Fig. 3A2-1). The lines then narrow down to 2.5μm again, then, and pass through the decoders of the remaining 64 registers. By widening the lines to 17.5μ everywhere in the decoder except where the

interaction with the bubbles takes place, and by using 2μm thick copper conductors, the line resistance of one chip can be kept down to 4.5 ohms. Register selection, writing, clearing, and sensing are all accomplished with 10 control lines. In general, the decode and clear lines of a number of chips will be connected in series and will share a drive circuit. The connection of the write and sense lines will depend on the memory organization, but for generality, individual access is provided to both ends of each line, resulting in 20 connections/chip.

3A2.5 Module Design

Sixteen chips are placed on a $\tilde{\sim}$ 4.5 cm x 4.5 cm planar substrate, which then has X and Y coils wound around it to supply the rotating in-plane field (Fig. 3A2-3). (The choice of module size is discussed in Appendix B) The IBM Controlled-Collapse solder connection [T71] has established very high reliability in space applications, and should provide a satisfactory means of mounting the chips on the module substrate (see Sec. 3A3). However, other types of connection, such as "flying lead" or TC bond are also possible.

To keep the number of interconnections per module down to an acceptable level, the chips are arranged in groups of four or "tetrads", (Fig. 3A2-4). The four chips are oriented 0^0, 90^0, 180^0, and 270^0 from the horizontal, and four-way multiplexing is used on all the lines. This can be done because the sense signal pulse only lasts for about 1/4 T_r, or one-fourth of the rotational period, and likewise the current-controlled switches used to accomplish the write, decode, and clear functions can all be made to operate with a control current which is on for only 1/4 T_r. The chips are all identical, but 90^0 physical rotations are used to introduce 90^0 skews in the relative phase of the rotating field as seen by the chip in question. Thus, four chips can share one preamplifier chip, which is placed centrally in close proximity to each chip to

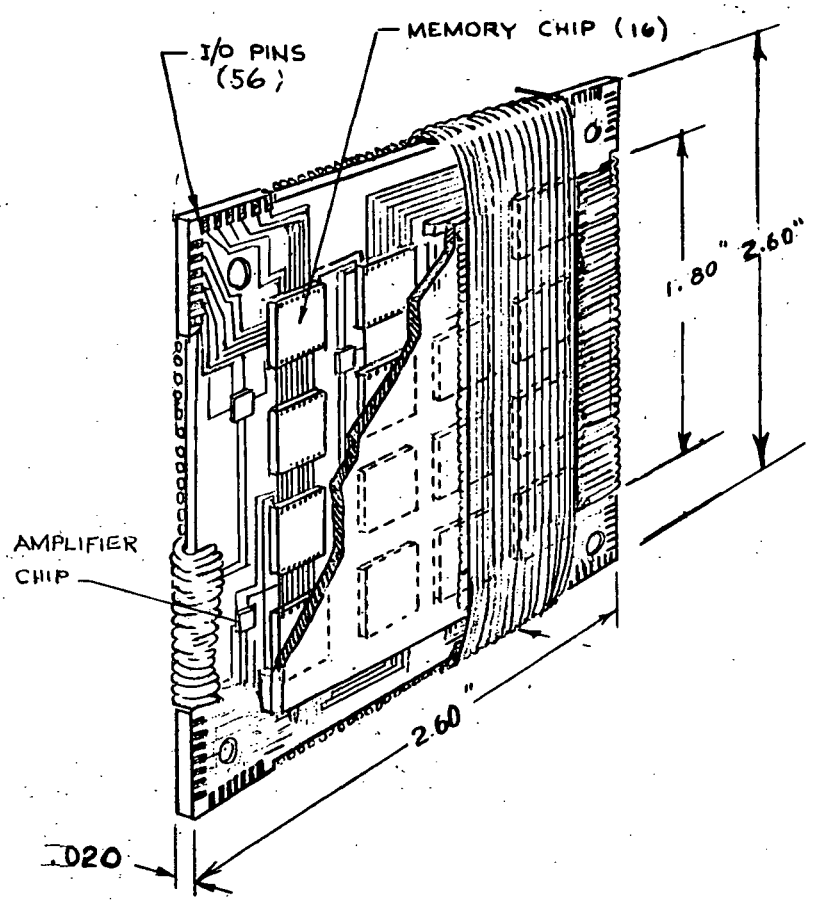


Fig. 3A2-3 Basic Memory Module (1.6×10^6 bits) Before Encapsulation

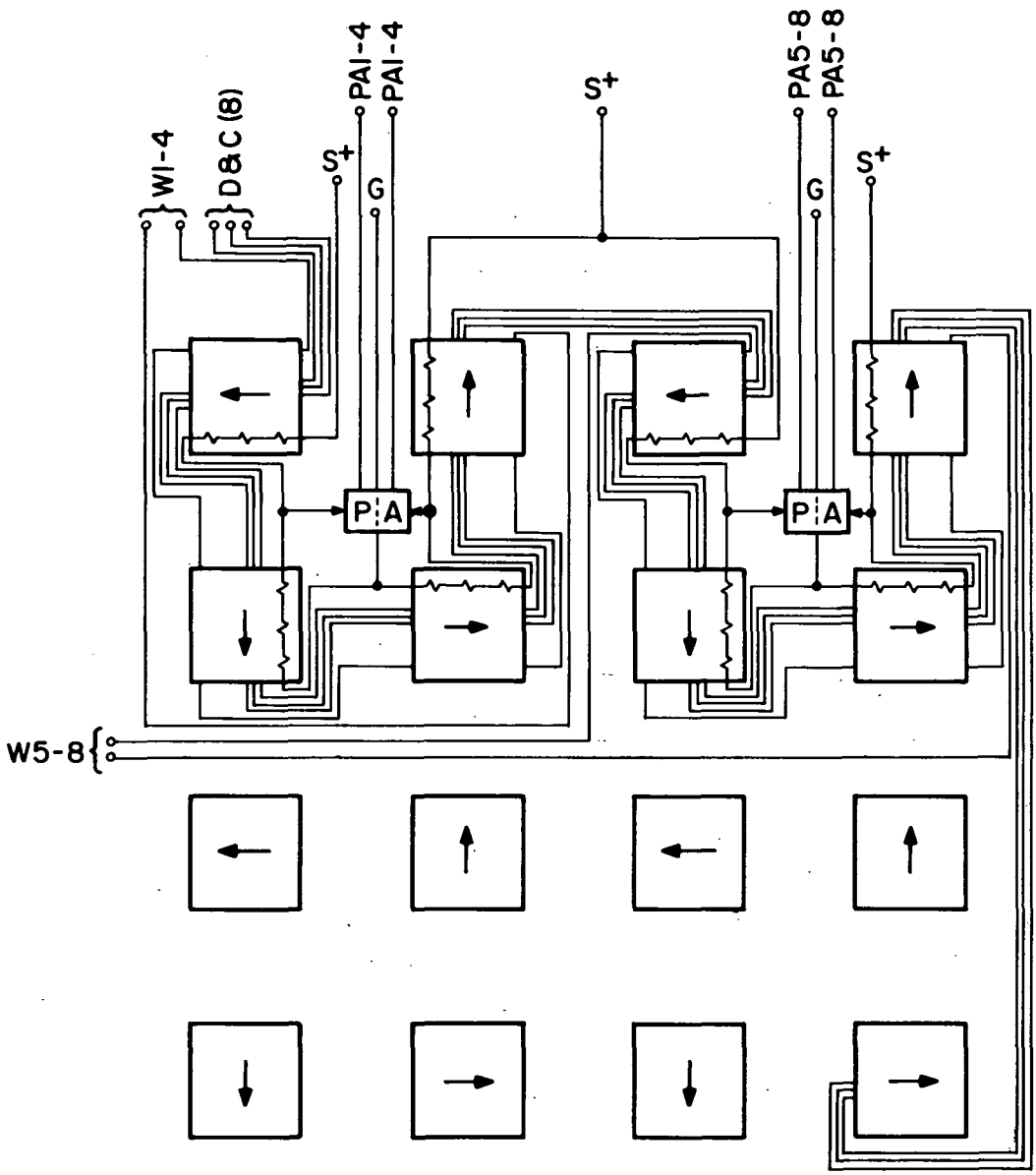


Fig. 3A2-4 "Tetrad" 16-Chip Planar Module (16 bits, 10^5 words, 50 connections)

minimize pickup noise. The preamplifier acts as the null detector in a bridge arrangement very similar to that used for the feasibility model (Sec. 4A), except that now a bridge element consists of the series combination of the eight sensors on a chip, rather than consisting of a single sensor. Note that there are no crossovers anywhere on the module. The conductors are assumed to be .005" lines on .01" centers (125μm lines on 250μm centers).

The advantage of this "tetrad" approach vs. a nonmultiplexing approach is not just in preamplifier sharing, but in total number of connections per module. Table 3A2-1 shows that the tetrad approach requires 50 connections, whereas the non-tetrad case would require 110, or more than twice as many. The advantage of the tetrad approach is even more drastic when the page connections are counted, as shown later in this Section (Table 3A2-2): 123 for the tetrad case vs. 411 for the non-tetrad case. (These numbers are all for the preferred design, the "bit-per-chip" organization.)

3A2.6 Page (or "Sub-Unit") Design

Further assembly of the memory proceeds by placing eight of the modules described above inside the permanent-bias-field package shown in Fig. 3A2-5. This package is the magnetic analogue of a parallel-plate capacitor, and is analyzed in detail in Appendix D. The magnetomotive force (MMF) is provided by small permanent magnet posts of Alnico, $GdCo_5$, or some other magnetically hard material, while the uniform bias field is provided by high-permeability plates made from permalloy ($Ni_{.81}Fe_{.19}$) or other suitable magnetically soft material. Since the permalloy almost completely surrounds the modules, it also provides good magnetic and electromagnetic shielding.

The memory sub-unit or "page" of Fig. 3A2-5 is actually a self-sufficient memory in its own right (except for logic and driving circuits), with provisions for bias and drive field and a total storage capacity of 1.28×10^7 bits. The

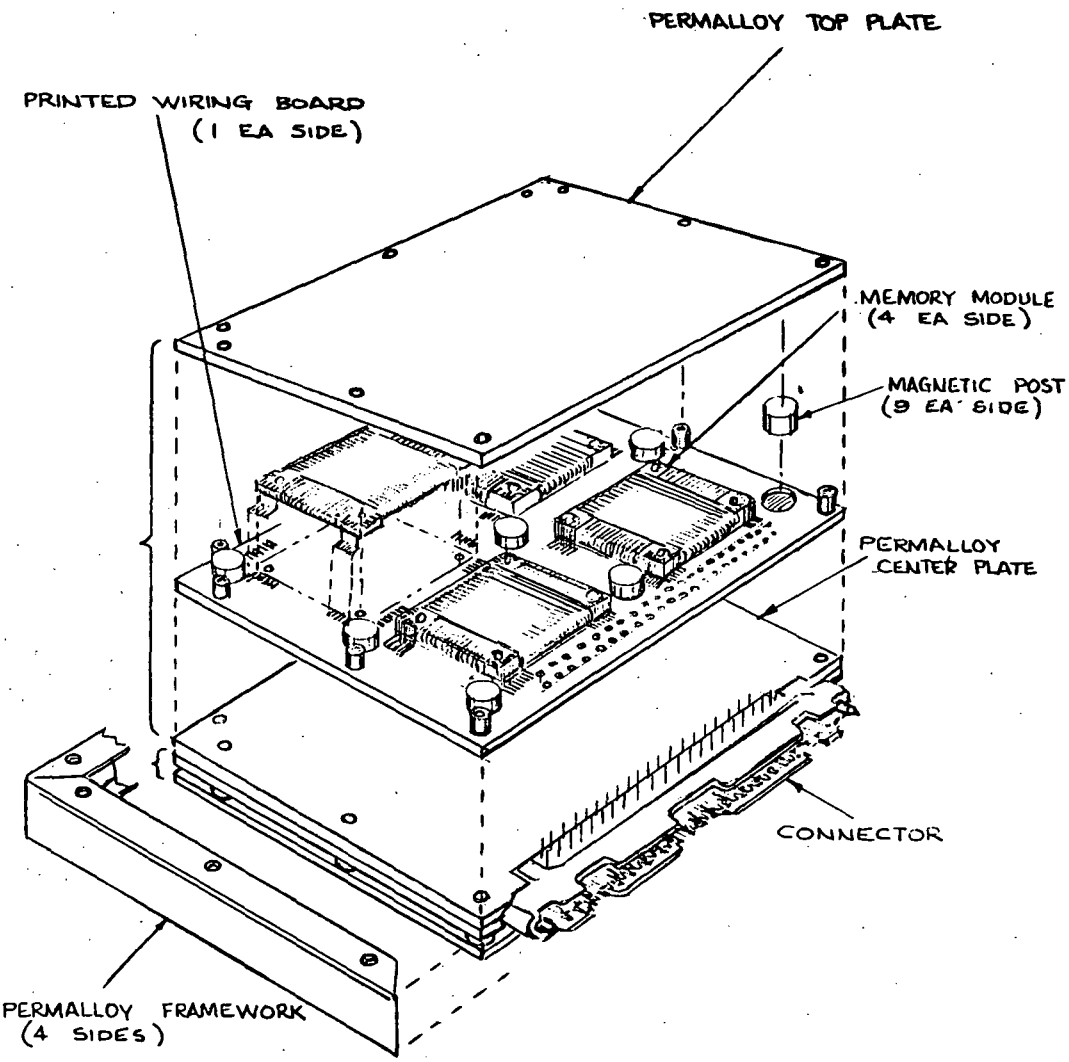


Fig. 3A2-5 . Memory Subassembly Exploded View
(Permanent Bias Field Package)

Table 3A2-1: Module Interconnection Count

(Bit-Per-Chip Organization is assumed)

Connection	Tetrad (Multiplexing)	Non-Tetrad (No Multiplexing)
Clear & Decode Lines In	8	8
Clear & Decode Lines Out	8	8
Write Lines In	4	16
Write Lines Out	4	16
Preamp Output (double-ended)	8	32
Sensor (+ Supply)	6	6
Sensor (- Supply)	4	4
Preamp Power	4	16
X	2	2
Y	2	2
TOTAL	50	110

10^8-bit memory is realized by stacking up the appropriate number of these basic building blocks. They lend themselves to several different memory organizations, and the exact number needed depends on the organization chosen. In the recommended "bit-per-chip" design (Sec. 3A5), a memory word consists of 64 data bits plus 32 check bits. Since each module has 16 chips, a memory word can be stored on 6 modules. Thus, a page can hold 10^5 memory words on 6 of its modules, the other two modules being used for spares to increase the reliability (Sec. 3B2). In this case, a page has 123 interconnections (Table 3A2-2), and sixteen pages are required for the full 10^8-bit memory (1.6×10^6 words x 64 data bits each = 10^8 data bits). The memory can be operated in a mode where rotating field power is supplied to only one page at a time, with a substantial saving on total memory power dissipation (Sec. 3B3). Since the pages are independent sub-memories with their own bias field source, replacement is simple, and pages can be moved back and forth between shelf storage, if desired.

3A2.7 Summary of Chip, Module, and Page Designs

Many of the reasons for the particular choice of chip design, module design, and page design have been given in sections 3A2.1 through 3A2.6. Some of the advantages of this approach have been pointed out. For further discussion, however, it is necessary to know how the memory will be organized, and this requires a knowledge of the electrical circuitry, packaging, and error correction coding needed to implement the various possible memory organizations. Therefore, these three topics will be discussed next (Sections 3A3 and 3A4), after which specific memory organizations and the advantages and disadvantages of the resulting systems will be discussed in Section 3A5. All the comparisons and tradeoffs, however, will be based on a 10^5-bit chip, a module with 16 chips and its own rotating field, and a page with 8 modules and its own permanent bias field, as described above.

Table 3A2-2: Page Interconnection Count[a]
(Bit-Per-Chip Organization is Assumed)

Connection	Tetrad (Multiplexing)	Non-Tetrad (No Multiplexing)
Clear & Decode Lines In	8	8
Write Lines In[b]	32	128
Preamp Output (single-ended)[c]	32	128
Sensor Bridge const Current Supplies	32	128
X + Y[d]	16	16
+V, -V	2	2
Ground	1	1
TOTAL	123	411

(a) For more detail, please see Sec. 3A3.
(b) Write Line Outputs run to a common ground.
(c) It is assumed that if the noise is too high to allow single-ended preamp outputs, then 32 "middle-amplifiers" are distributed on the page to allow the sense signal to come off the page single ended.
(d) Each coil is individually driven. This requires more connections than if several coils were interconnected (series or parallel), but results in higher reliability (see Sec. 3B2).

3A3 ELECTRICAL AND MECHANICAL DESIGN (PACKAGING)

3A3.1 Circuit Requirements and Power Estimates

This section is a study of the electronic requirements of the Mass Storage Unit (magnetic bubble storage). The objective of this study was to provide power and parts count estimates to be used in the mechanical design and in the tradeoff studies of Section 3B3.

First, it is necessary to do a preliminary electronic systems design. Circuits were designed to implement the functions defined in the systems design. The circuits obtained were not optimized and are intended only to represent a reasonable estimate of complexity and power consumption. The exact circuit count and power dissipation depends on the memory organization being considered and on the degree of redundancy or sparing being used. For the sake of discussion, all the numbers in the following discussion pertain to the recommended bit-per chip organization, with two spare modules (planes) per page for maximum reliability. This gives an upper bound on circuits and power.

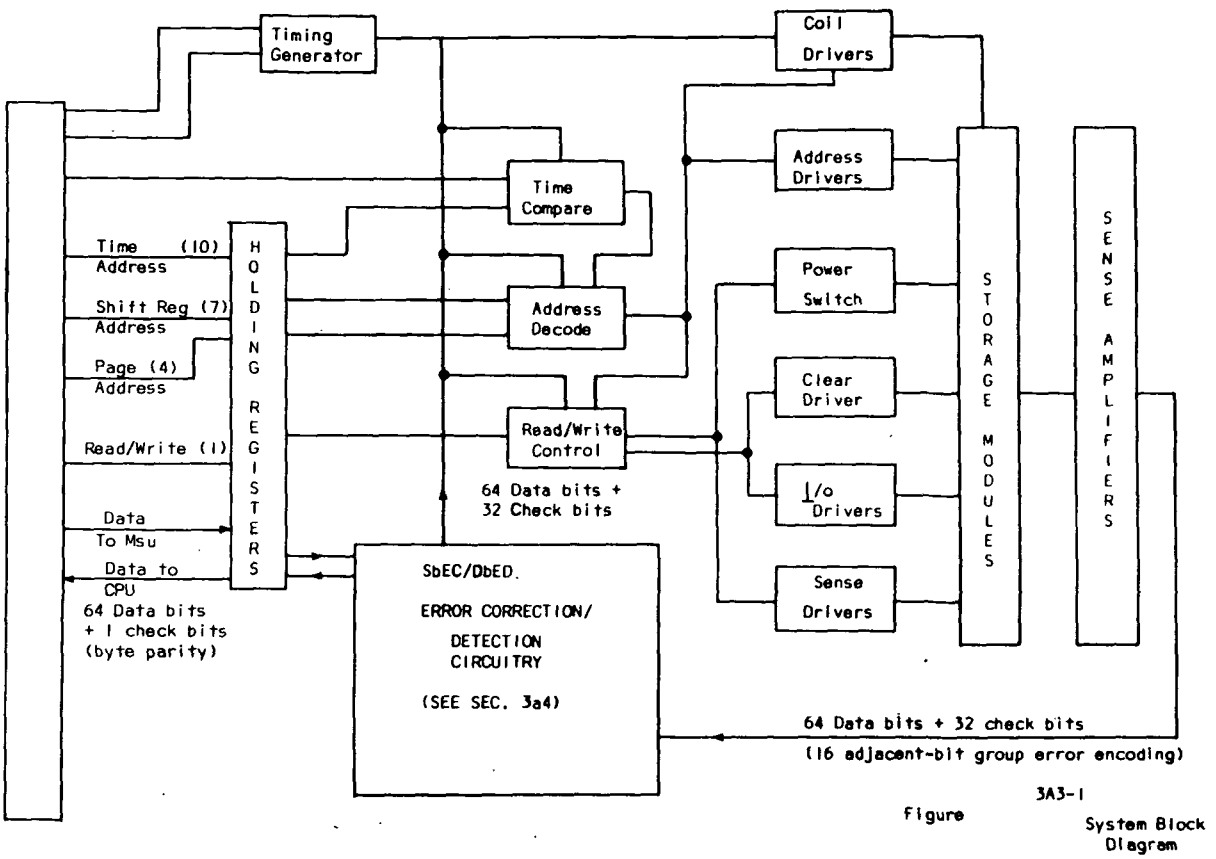
The general block diagram of the system is shown in Figure 3A3-1. The function of each block is explained in the following sections.

Timing Generator. - The logic and timing is shown in Figure 3A3-2. This circuit develops the fundamental timing for the MSU. The X and Y signals are applied to the drive coils. The signals (First X, etc.,) are typical timing signals that will be required to exercise the MSU. Additional timing signals may be required and provision for these has been included in the parts and power estimate.

Time Compare. -This logic compares the bit time wanted by the computer to the bit count maintained by the logic. (See Recommendations section). The logic consists of a 10-bit counter, a 10-bit comparator to compare the desired start time (from CPU) with the counter, and a 10-bit comparator to compare the counter with a count (hardwired) of 800 so the counter may be reset to zero.

Address Decoder. -This logic provides sequential decoding of the chip and shift register address bits. Sequential decoding is required when more than one block of data is being transferred(1 block = 800 words of 64 data bits each). The address of the second block is entered bit-by-bit each clock period as the last bits of the first block are being manipulated.

An eleven bit shift register (with a single "1") is assumed to provide gating of the address from the holding registers. A comparator is needed to detect the 788 bit time and start the shift register.



3A3-1

Figure System Block Diagram

(Note: This system block diagram applies specifically to the recommended bit-per-chip design)

Fig. 3A3-1 System Block Diagram

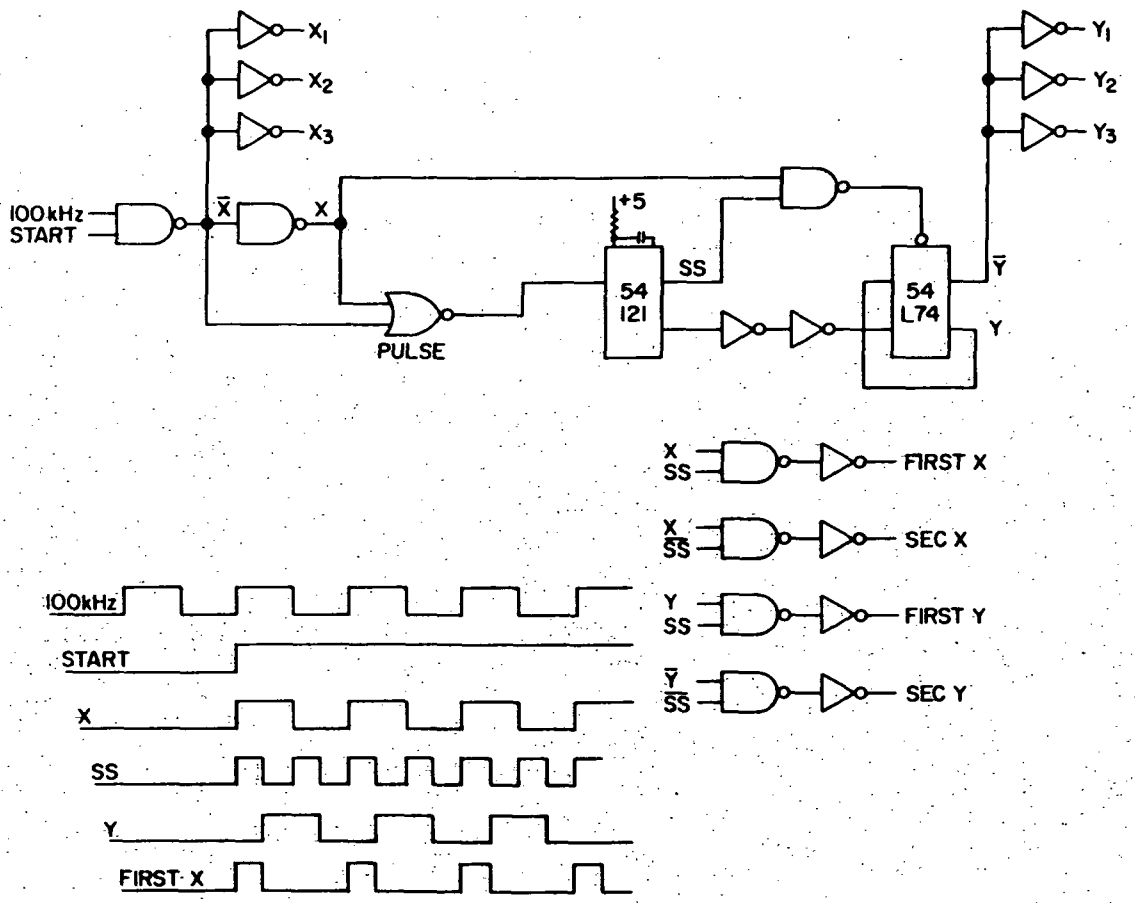


Fig. 3A3-2 Logic and Timing

Read/Write Control. - This logic controls the Clear Driver and I/O drivers during a write operation and the Power Switches and Sense Drivers during a read operation.

Coil Drivers. - Each of the generators must deliver $\pm$ 100 MA to the coils. The peak voltage across the coils will occur when the generators switch. From Appendix B, Table B-1, the peak voltage required is 7.9 volts. The power supply for the generators must be 7.9 volts plus enough control voltage to provide regulation of the 100 MA current. It appears that the minimum supply voltage is 10 VDC. A circuit to meet this requirement is shown in Figure 3A3-3.

If all the coils were driven all the time, this function would use most of the power required to operate the MSU. In the bit-per-chip design, only one page or 1/16 of the coils are driven at one time. Activation of the proper coil drivers is controlled by the address decode circuitry.

Address Drivers. - This circuit supplies 10 MA to the address lines on the magnetic chip. The lines of 16 chips (4.5Ω each) are connected in series on each module (72Ω) and 8 modules are connected in series (576Ω) to form the basic memory pages. Since there are 16 pages and 7 address lines, 112 current generators would be required. This represents an excessive number of components and wastes power. The tuned voltage source driver configuration shown in Figure 3A3-4 was adopted.

Clear Driver. - The clear driver operates only in the write mode. The circuit is the same as one of the address drivers.

One/Zero Control Drivers. - The 1/0 requires 32 drivers, one for each four bits on the word (because of the four-way multiplexing explained in Section 3A2.5). A 10 MA current into 72Ω is required. A driver similar to the voltage mode address driver is assumed. This is shown in Figure 3A3-5.

Sense Drivers. - This circuit supplies 2 MA to the 400Ω /leg bridge. One leg of the bridge is 8 of the 50Ω magnetoresistive elements in series. The bridge connection of four memory chips and one sense preamplifier chip was shown in Fig. 3A2-4. There are 512 bridges in the MSU but only 32 need to be powered at any given time.

Power Switches. - This circuit switches the power to the 32 preamplifiers on each page. Only one page is in use during any block transfer. By keeping the power off the other fifteen, a considerable power savings is realized:

$$(15)(32)(.064) = 30.6 \text{ W}$$

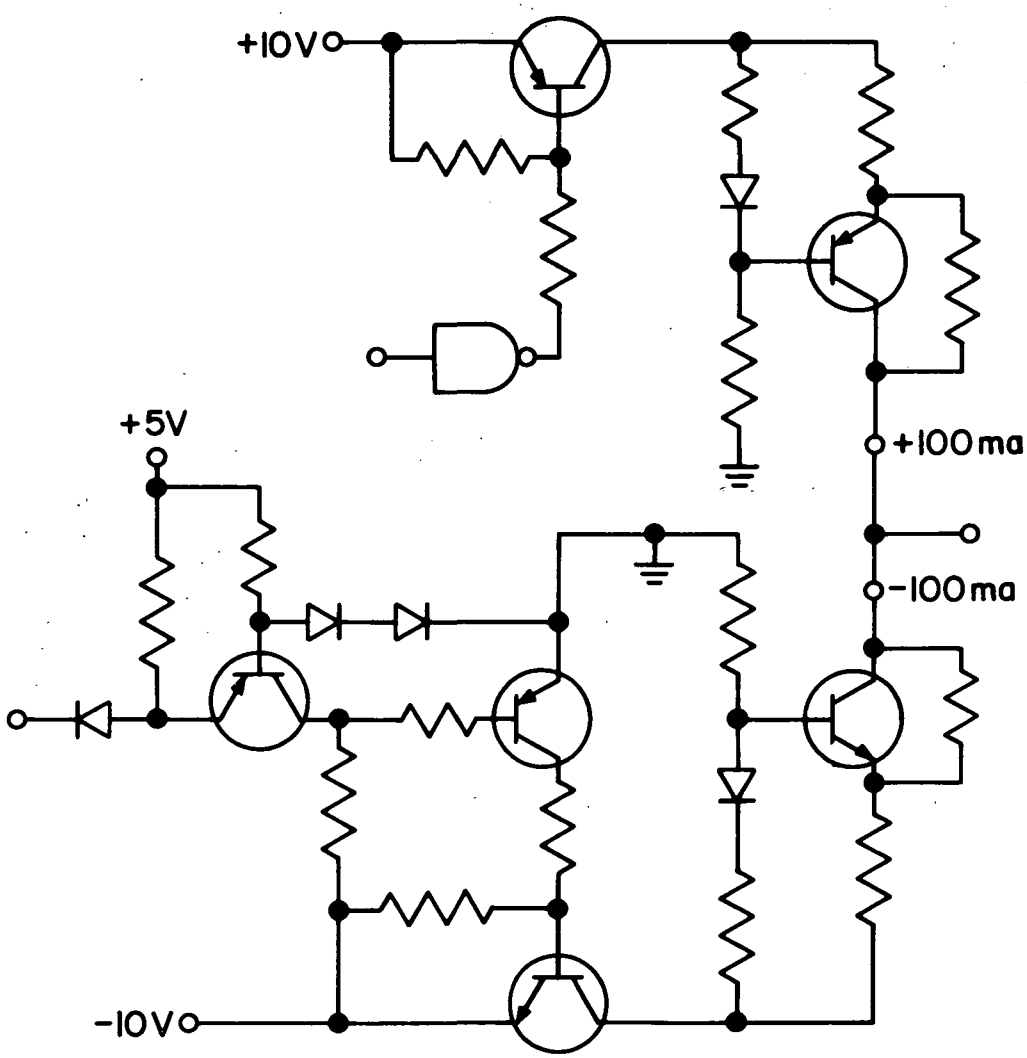


Fig. 3A3-3 Coil Driver

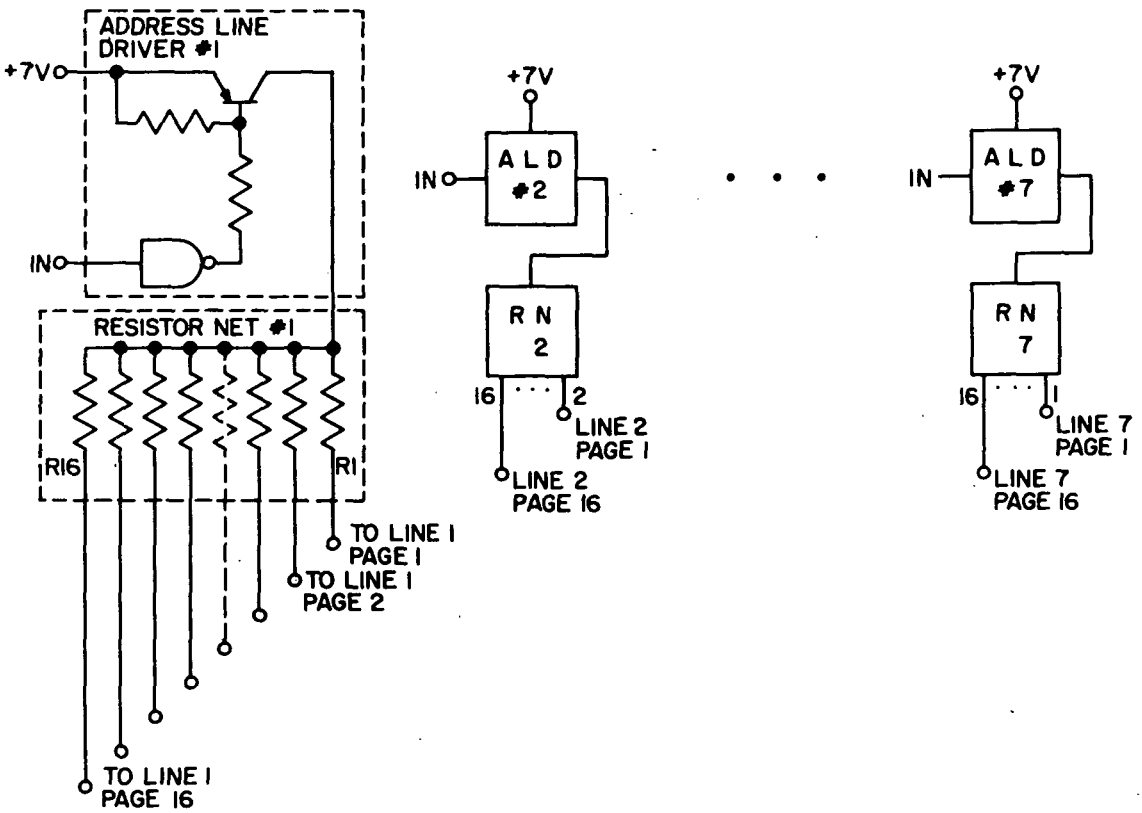


Fig. 3A3-4 Address Driver System

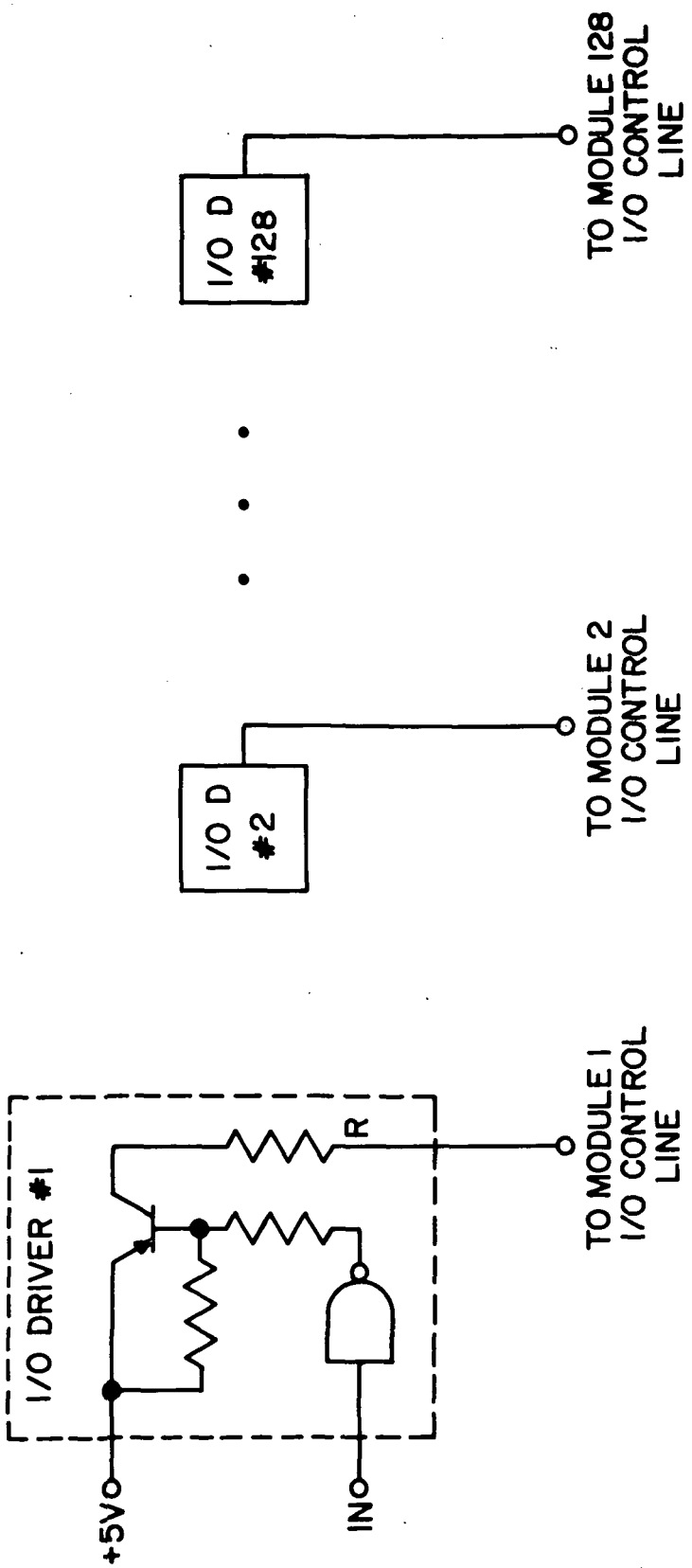


Fig. 3A3-5 One/Zero Control Driver System

Preamplifiers. - There are 512 preamplifiers in the MSU, 4 on each of 128 modules. An AC-coupled preamplifier has several advantages. It would get rid of the initial affect trimming and would reduce noise problems associated with switching the sense current since the associated sense amplifier could be cleared between the application of the sense drive and the arrival of the bit at the sensor.

Sense Amplifiers. - There are 32 sense amplifiers in the MSU, (again, because of the four-way multiplexing). The sense amplifier power estimates are from a study done by F. Grunberg (G70).

Error Correction Circuits. - The number of circuits needed to perform the error detection and correction are discussed in detail in Section 3A4. Typical gate counts are on the order of 7000, which if implemented in CMOS technology (Complementary MOS, ~ 100-200 μW/gate (A70)) would involve 0.7-1.4 watts total.

Organization. - The module has been shown in Figure 3A2-4, which illustrates the I/O requirements and the organization of the sense, power switch and preamp networks. Figure 3A3-6 illustrates the page assembly and defines the I/O across the magnetics/electronics interface.

Recommendations. - There should be a special timing shift register on each chip. Only one chip on each module would have electronics associated with it. No address lines or address drivers are required. The special shift register allows the chip to indicate what the bit time is on the chip. The true time is that indicated by the chip and the time kept by the logic should agree. However, if the logic ever developed the wrong time due to an electronics problem, (such as a power transient or an open line in one driver) there would be no way to determine the chip time and the data would be lost.

One configuration for the data written into the special register would be 10110-0 (800 bits). The first "1" would indicate bit time #1. The second and third "1"s would assure that the shift direction had not reversed itself; i.e., after the first "1" is detected check that the next bit is a "0".

Conclusions. - The power and parts count for each function are presented in Table 3A3-1. The system power and parts count are presented in Table 3A3-2. As mentioned in the beginning of this section, these numbers pertain to a bit-per-chip design with six active modules and two spare modules per memory page. These spare modules are not needed in all applications, and so these numbers are an upper bound on the circuit and power requirements for the various bit-per-chip designs.

For comparison purposes, the equivalent information for the bit-per-module (or bit-per-plane) design is also presented. This design (see Section 3A5)

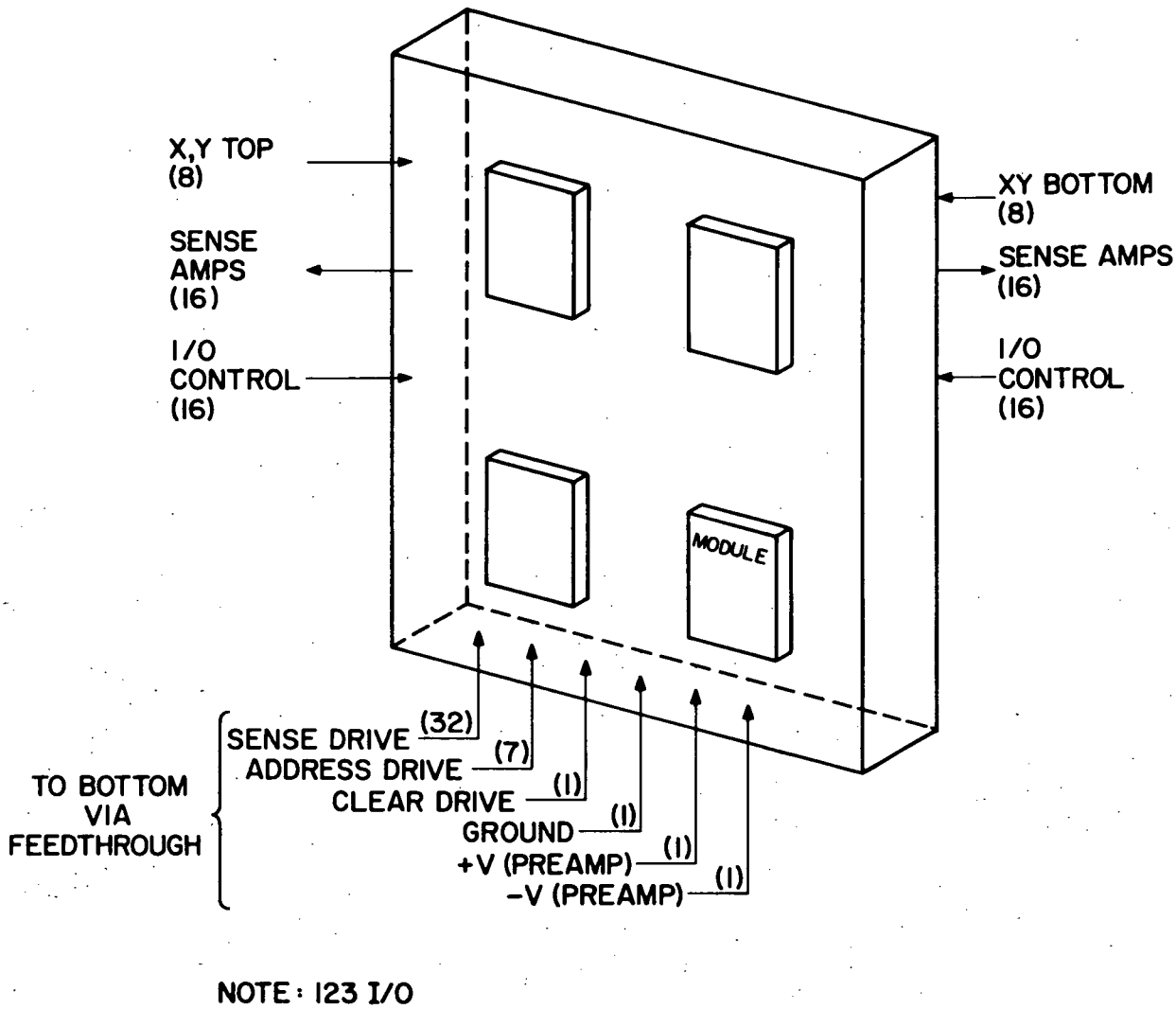


Fig. 3A3-6 Memory Page Assembly

has nine pages of eight modules each. The power and parts counts are given in Table 3A3-3 for each function and in Table 3A3-4 for the entire system. It can be seen that the bit-per-chip design requires considerably less power. This is discussed further in Sec. 3A5 and Sec. 3B3.

TABLE 3A3-1

MSU POWER REQUIREMENTS FOR BIT-PER-CHIP SYSTEM WITH TWO SPARE MODULES PER PAGE

(Qty)	Circuit Description/Parts Count	Power
(16)	Power Switches/56 resistors 24 PNP transistors 8 NPN transistors 2 IC (TTL) 90	Negligible (Controls power to preamps--charge power there--near zero when not in use).
(512)	Preamplifiers/512 (mounted on module)	32 (64 mw) = 2.05 w
(32)	Sense Amplifiers / 32 ICs	(32) (.136) = 4.35 w
(32)	One/Zero Control/32 PNP transistors 96 resistors 8 IC (TTL) 136	Peak power: (32) (.010)(5) = 1.6 w 50% probability 1/0: 0.8 w
(100)	Holding Registers (CPU →MSU) Parts: 50 IC (TTL)	.425 w
(1)	Timing Generator/9 IC (TTL) 7 capacitors 8 resistors 2 diodes 26	.3w
(1)	Time Compare/12 ICs (TTL)	.2 w
(1)	Address Decode/12 ICs (TTL)	.15 w
(1)	Read/Write Decode/20 IC (TTL)	.15 w
(1)	Error Correction Translator/140 IC (CMOS)	1.4 w

TABLE 3A3-1 (continued)

(Qty)	Circuit Description/Parts Count	Power
(7)	Address Drivers/7 PNP transistors 14 resistors 2 ICs (TTL) 112 trimmable resistors 135	Peak (7) (7) (.16) = 7.9 w 50% probability 1/0 3.95 w
(1)	Clear Driver/1PNP 2 resistors 16 trimmable resistors 19	Peak 1.1 w
(32)	Sense Drivers/32 PNP 64 resistors 8 IC (TTL) 104	1.0 w
(8 + 8)	X, Y Drivers/64 PNP (16 to -5) 32 NPN (16 to -5) 224 resistors 48 diodes 4 IC (TTL) 372	8 w

TABLE 3A3-2

POWER SUMMARY, BIT PER CHIP

Qty	Circuit Description	Power	
		Peak	Average
135	Address Drivers	7.9	3.95
19	Clear Driver o	1.1	1.1
104	Sense Drivers *	1.0	1.0
372	X, Y Drivers	16	8.0
90	Power Switch	---	---
32	Sense Amps *	4.35	4.35
136	One/Zero Control^{o}	1.6	0.8
50	Holding Registers	.425	.425
26	Timing Generation	.3	.3
12	Time Compare	.2	.2
12	Address Decode	.15	.15
20	Read/Write Decode	.15	.15
140	ECC Translator	1.4	1.4
1148			
512	Preamps *	2.05	2.05
1660			

Total Power

Peak Power -- Write 29.2 w Read 33.9 w
Average -- Write 16.5 w Read 22.2 w

^{o} Write Function

* Read Function

TABLE 3A3-3

MSU POWER REQUIREMENTS FOR
BIT-PER MODULE (BIT-PER-PLANE) CASE

(Qty)	Circuit Description/Parts Count	Power
(8 + 8)	Power Switches/56 resistors 24 PNP transistors 8 NPN transistors 2 IC (TTL) 90	Negligible (Controls power to preamps -- charge power there--near zero when not in use).
(576)	Preamplifiers/576 (mounted on module)	72 (64 mw) = 4.6 w
(72)	Sense Amplifiers/72 ICs	(72) (.136) = 9.8 w
(72)	One/Zero Control/72 PNP transistors 216 resistors 18 IC (TTL)	Peak power: (72) (.010)(5) = 3.6 w 50% probability 1/0: 1.8 w
(100)	Holding Registers (CPU → MSU) Parts: 50 IC (TTL)	.425 w
(1)	Timing Generator/9 IC (TTL) 7 capacitors 8 resistors 2 diodes 26	.3 w
(1)	Time Compare/12 ICs (TTL)	.2w
(1)	Address Decode/12 ICs (TTL)	.15 w
(1)	Read/Write Decode/20 IC (TTL)	.15 w
(1)	Error Correction Translator/54 IC (CMOS)	.54 w
(11)	Address Drivers/11 PNP transistors 22 resistors 3 ICs (TTL) 99 trimmable resistors 135	Peak (11)(7)(.1) = 7.7w 50% duty cycle 3.85 w 50% probability 1/0 1.925 w

MSU Power Requirements, Bit-Per-Module (Cont'd)

(Qty)	Circuit Description/Parts Count	Power
(1)	Clear Driver/1 PNP	Peak . 7 w
	2 resistors	50% duty cycle . 35 w
	9 trimmable resistors	50% probability
	12	1/0 . 175 w
(72)	Sense Drivers/72 PNP	4. 3 w
	144 resistors	50% duty cycle 2. 15 w
	18 IC (TTL)	
	234	
(18 + 18)	X, Y Drivers/144 PNP (36 to -5)	38 w
	72 NPN (36 to -5)	
	504 resistors	
	108 diodes	
	9 IC (TTL)	
	837	

POWER SUMMARY, BIT-PER-MODULE

Qty	Circuit Description	Power Peak	Power W. C. Average	Power Average
135	Address Drivers	7.7	3.85	1.925
12	Clear Driver °	.7	.35	.35
234	Sense Drivers *	4.3	2.15	2.150
837	X, Y Drivers	38.0	38.0	38.0
90	Power Switch	---	---	---
72	Sense Amps *	9.8	9.8	9.8
306	One/Zero Control °	3.6	1.8	1.8
50	Holding Registers	.425	.425	.425
26	Timing Generation	.3	.3	.3
12	Time Compare	.2	.2	.2
12	Address Decode	.15	.15	.15
20	Read/Write Decode	.15	.15	.15
54	ECC Translator	.54	.54	.54
1860				
576	Preamps *	4.6	4.6	4.6
2436				

Total Power

Peak Power	--	Write 51.79 w	Read 66.19 w
WC Average	--	Write 45.79 w	Read 60.19 w
Average	--	Write 43.86 w	Read 58.27 w

° Write Function

* Read Function

3A3.2 Packaging Design of the Mass Storage Unit (MSU)

To meet the packaging design requirements required for the MSU, a new packaging conceptual design of a planar configuration was established. This new design concept is shown in Figure 3A3-7. The technical objectives of this design concept, in addition to providing the required magnetic environment for the bubble domain memory, are: (1) realization of minimum weight and volume, (2) elimination of interconnection complexities, (3) adequate environmental protection, and (4) sufficient thermal/weight efficiencies so as to achieve modular flexibility features suitable for Space Shuttle application. Packaging techniques and environmental effects which were successfully used on other IBM Space programs were employed in this conceptual design of the MSU.

The following packaging design related areas will be discussed:

- Conceptual design of the MSU (Structure, Weight analysis).
- Memory subassembly (Basic memory module, Chip mounting, and Module mounting and interconnection)
- Logic circuits subassembly (Hybrid module, Component mounting and interconnection)
- Subassembly thermal design
- Subassembly installation and interconnection
- Reliability and Maintainability
- Environmental Considerations
- Conclusions and Recommendations

The overall packaging configuration of the MSU is described in Figure 3A3-7. The physical characteristics of the unit are estimated as follows: Again, in order to discuss a specific example, all the numbers presented here apply to the bit-per-chip system (Sec. 3A5).

Maximum dimensions	9" x 8" x 7 1/4"
Volume	520 cubic inches
Weight	27.4 pounds

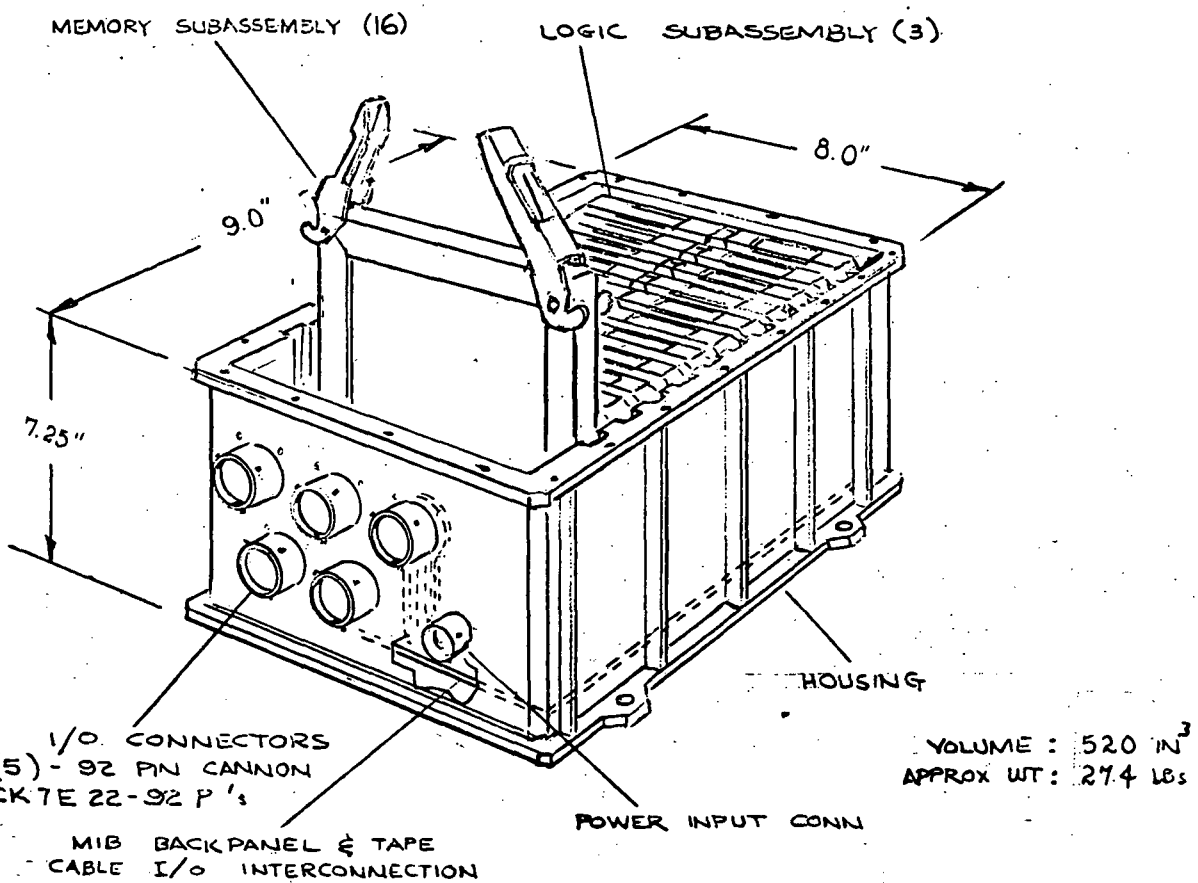


Fig. 3A3-7 Mass Storage Unit Assembly

The unit consists of a housing structure with five I/O connectors, a cover, sixteen memory subassemblies or pages (Figure 3A3-8), plus three pluggable modular subassemblies called pages (Figure 3A3-11) containing logic circuits. These subassemblies plug into and are interconnected by a multilayer distribution panel mounted to the base structure of the unit. This unit design does not include the power supply requirement. It is assumed power will be furnished from a centralized power source in the spacecraft.

3A3.3 Structure and Weight Analysis

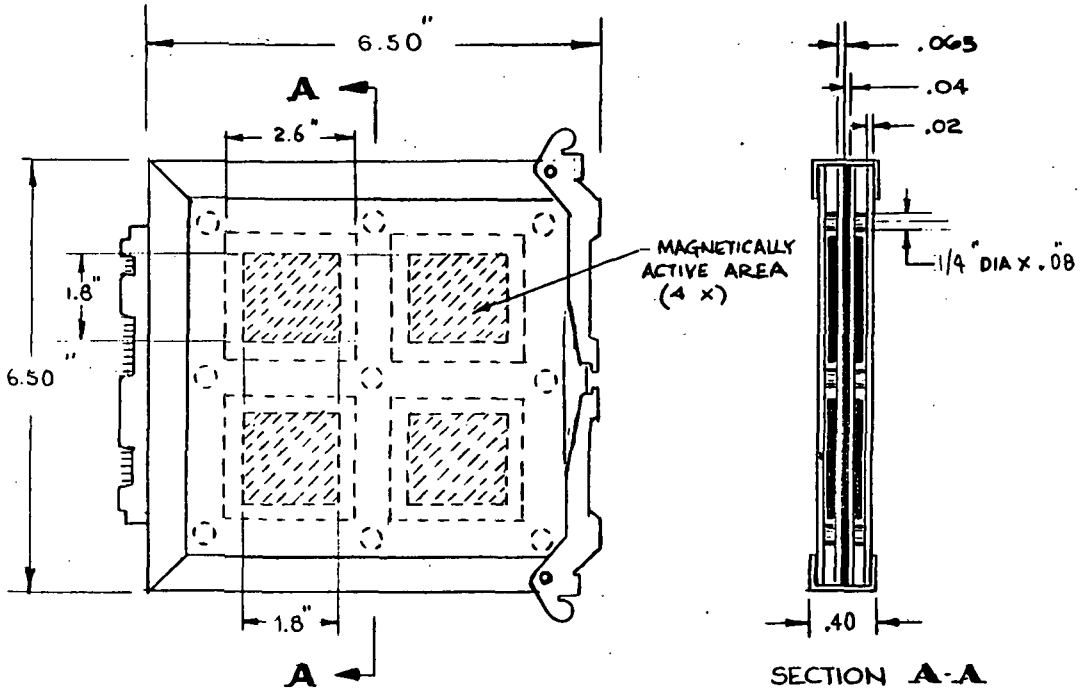
The MSU housing/cover structure is a rectangular box cast from materials with high strength/weight ratio such as magnesium alloy EZ33A-T5, with Iridite 15 finish, to provide corrosion protection. The housing is provided with four mounting feet for installing the unit to the Shuttle coldplate. The distribution panel is fastened to the base structure by means of four screws. Besides providing mechanical support for the subassemblies under specific vibration and shock environments, the housing structure serves as the heat conduction path between the subassemblies and the coldplate. The cover provides access to the subassemblies for unit maintenance and is secured to the housing flange by screws spaced to effect interface RFI integrity. A Parker Gasko seal is inserted around the periphery of the housing flange to effect a hermetic seal between the housing/cover interface. Five hermetically sealed Cannon 92-pin connectors provide signal and power inputs to the memory unit.

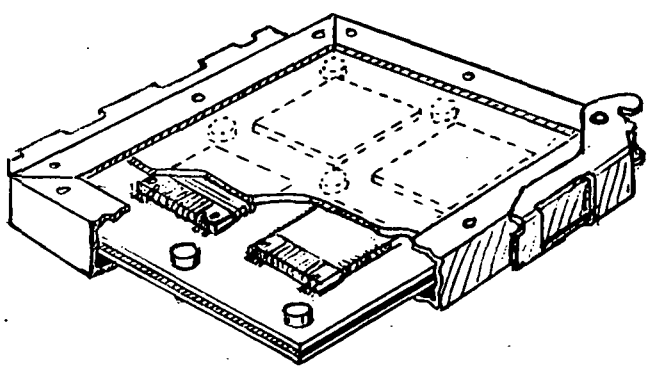
The following summation of the MSU weight breakdown represents the best estimated weight of the unit as a result of packaging studies:

Part	Qty.	Part Wt. lbs.	Total Wt. lbs.
Memory subassembly	16	1.36	21.8
Electronics subassembly	3	.400	1.2
Distribution panel assembly	1	.60	.60
Structure (housing & cover)	1	2.4	2.4
Tape cables	5	.01	.05
I/O connector	5	.25	1.25
Misc. (screws, spacers)			.05
		TOTAL	27.4

3A3.4 Memory Subassembly

The basic memory subassembly is a pluggable planar unit designed to mount and interconnect up to a maximum of eight basic memory modules. (Module description is given below). The memory subassembly as packaged is shown in Figure 3A3-8 and measures 6.5 x 6.5 x 0.4 inches, excluding





REF FIG 3A3-9 FOR DETAIL ASSY

Fig. 3A3-8 Memory Sub-Assembly (Page)

protrusions of the connector and mounting ears. An exploded view of the subassembly is shown in Figure 3A3-9. Major elements of the subassembly consist of eight basic modules, two printed wiring boards, three permalloy plates, four permalloy edge members, and a Burndy-type edge connector. A gold plated copper lead frame is used to connect the memory subassembly to the P. W. board (Figure 3A3-9).

In assembling, the first operation is to form the ribbon leads into "S" shape by means of a forming tool. After the inner support window structure is cut off, the lead frame is placed over the module and its leads are properly aligned to each corresponding metallized I/O pad on the module substrate by the use of a positioning fixture. The ribbon leads are bonded to the metallized pads by thermal compression bonding technique. After the outer lead support window frame is cut off, the module is bolted to the P. W. board surface and supported by four spacers which permit the module coils to be in touch with the board surface but prevent the coils from being overstressed. The other end of each lead is then thermal compressionally bonded to each corresponding conductor on the P. W. board surface. The P. W. boards are then married with the center permalloy plate by means of soldering the Burndy edge connector pins to the plated through holes on the edge of each board. At this point, the top and bottom permalloy and the permalloy edge members are installed and properly aligned, and the unit is finally held together by long screws. A total of sixteen memory subassemblies is required for a 10^8 bit MSU organized on a bit-per-chip basis. Each subassembly contains eight modules.

Basic Memory Module

The module is the basic building element of the MSU. As shown in Figure 3A3-10, the module is a self-contained element from both the construction and circuitry viewpoints. From the construction viewpoint, a basic module consists of 16 storage flip chips, 4 pre-amplifier chips, a common substrate (Al_2O_3 ceramic) with screened thick film conductor patterns, two common drive coils and a common set of input and output lines. From a circuitry viewpoint, the module (of 16 chips) shares the common propagation drive, and the use of write and read/clear decoder greatly reduces the input and output wirings requirements.

The estimated size and weight of the module are 2.6 x 2.6 x 0.067 inches and .004 pound respectively. Approximately 54 input and output terminal pads are provided at the edges of the substrate for electrical connections to the memory subassembly P. W. board. There are two coils per module; each coil consists of 360 turns of 5 mil copper wire wound around the module. A total of 96-128 modules is required for a 10^8 bits MSU.

Chip Mounting and Interconnection

The memory storage chips will be designed and built using packaging systems derived from IBM solid logic technology (SLT). Detail discussion on chip organization, design, and fabrication is presented in this report.

As described in Sec. 3A2, the bubble-domain device is a 20-terminal ball flip chip and measures approximately 200 x 250 x 10 mils. The interconnection between chip and substrate is made by reflow soldering the chip solder balls to the thick film substrate conductor [T71]. The interconnections between chips are accomplished by means of electrode patterns on the substrate (Figure 3A3-10). Chip mounting is normally performed by automated chip handling equipment which orients the chips and places them on the pre-tinned substrate electrodes. A small amount of water white rosin flux is deposited on the substrate conductor tips prior to chip mounting. The flux enhances the reflow soldering and acts as an adhesive to keep the chip properly positioned until it is soldered in place. Reflow soldering operation takes place in a belt furnace at approximately 335°C temperature.

A domed cover is bonded by Epoxy (Epon-828) to the substrate to cover the entire chip populated area. The cover will seal off the chips and thereby provide to them environmental protection during operation. At this point, the drive coil, first X and then Y, is wound around the module, with one lead grounded to the module support structure and the other lead terminated to a module Input/Output pad which connects to a generator on a logic page subassembly.

Module Mounting and Interconnection

The interconnection between the module and the memory subassembly PW board is made by soldering the module I/O contact pins to the plated through holes on the PW board. The module is also mechanically fastened to the PW board by four screws (Figure 3A3-9). Electrical connections between modules are achieved via PW boards. As shown in Figure 3A3-6, the memory subassembly has 123 I/O connections. A subassembly of eight modules is served by a single center permalloy plate and surrounded by a permalloy yoke formed by plates and edge members. It further shows that the groups of eight modules have their own control lines which are wired in series. The subassembly of Figure 3A3-8 thus constitutes a completely self-contained memory of approximately 1.3×10^7 bits.

3A3.5 Logic Circuits Subassembly (or Page)

The memory logic circuits contain approximately 1150 electrical components, of which 160 are T^2L integrated circuits, 140 are CMOS integrated

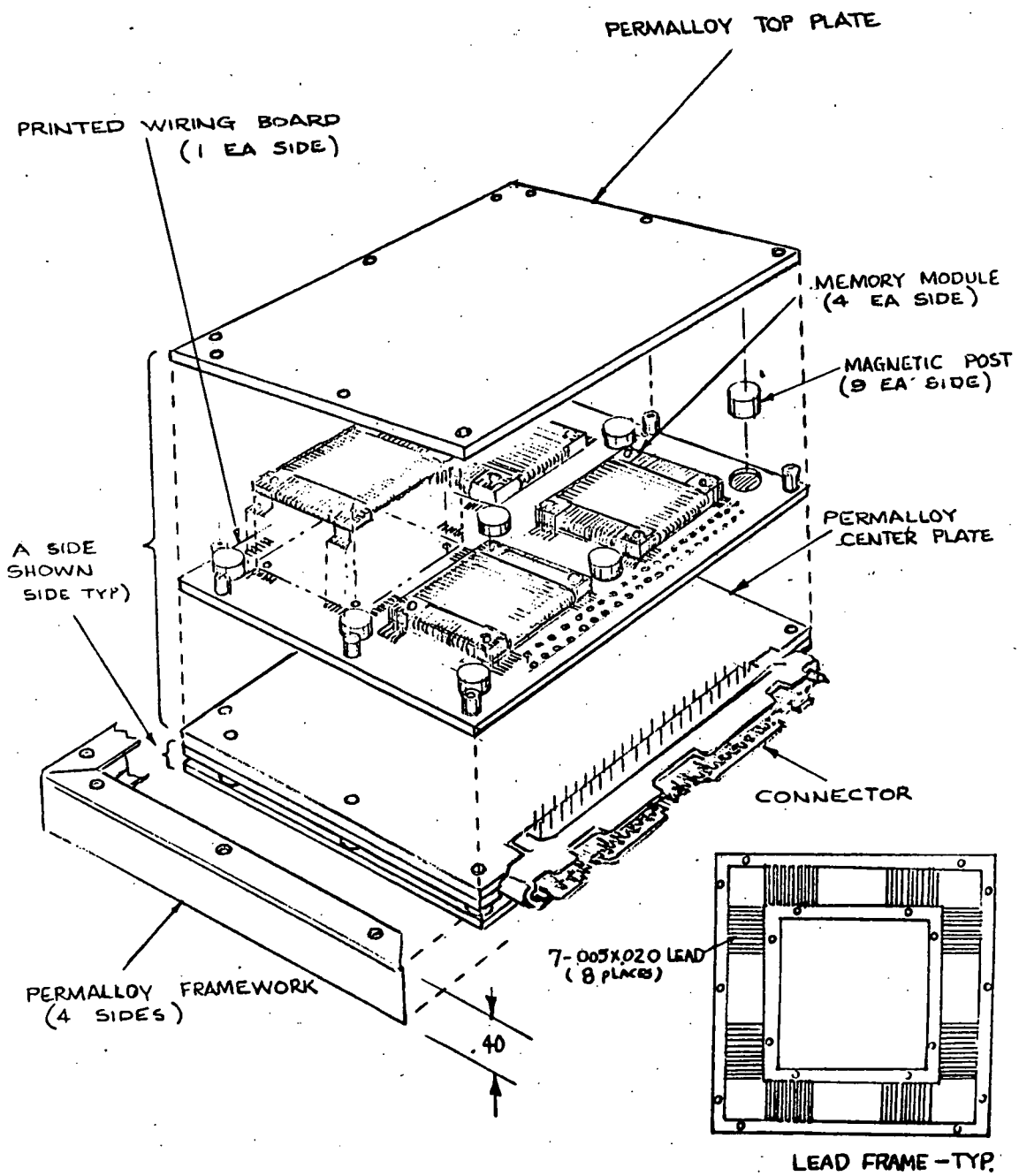


Fig. 3A3-9 Memory Sub-Assembly, Exploded View

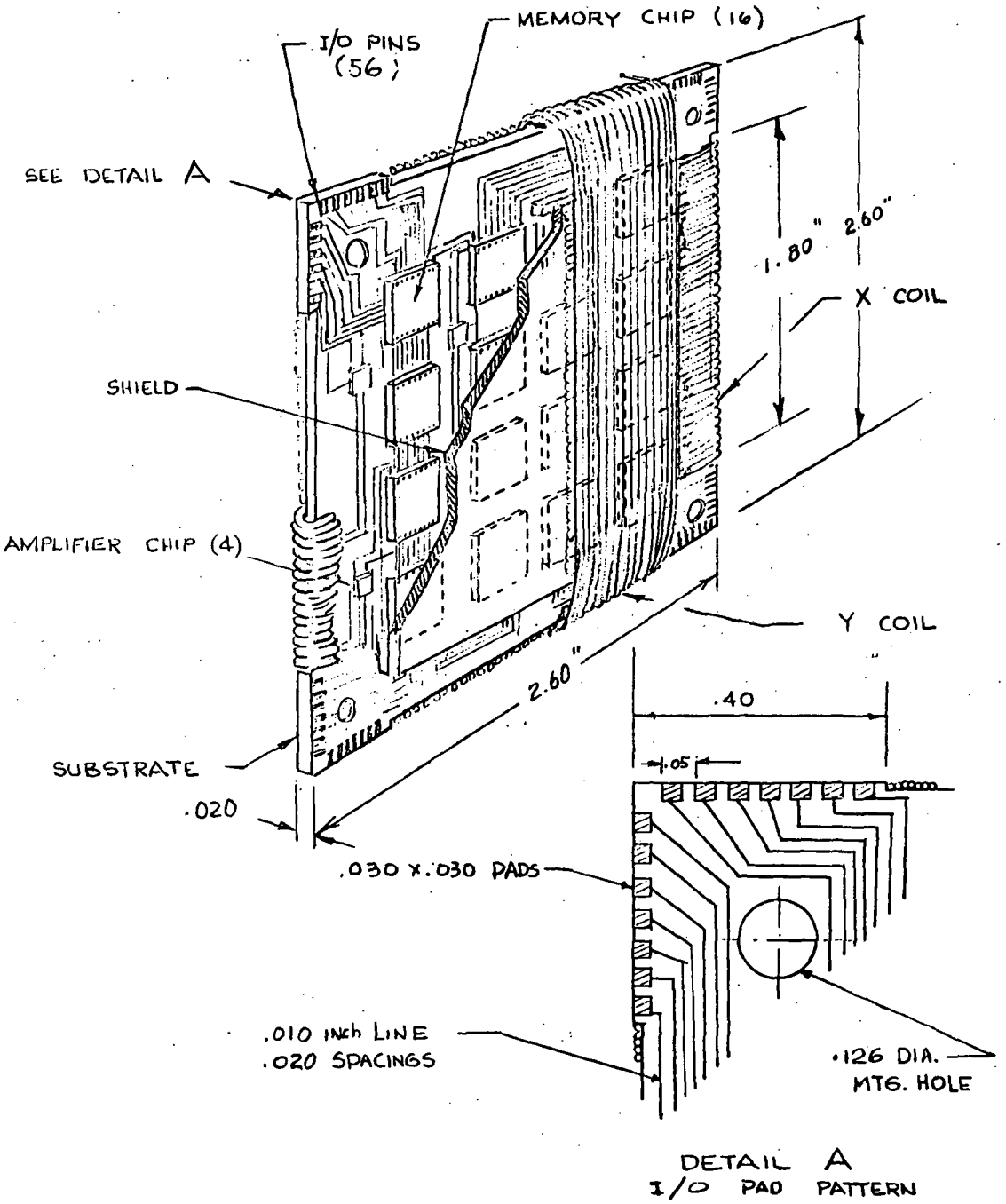


Fig. 3A3-10 Basic Memory Module (Plane)

circuits, and 1000 are resistors, capacitors and transistors, in chip form (Table 3A3-1). This count does not include the 512 pre-amplifiers which are distributed on the 128 memory module substrates. All chip devices are packaged into hybrid modules by means of thick film processes. Hybrid modules and T^2L flat packs are packaged in three plug-in second level packages, called page subassemblies.

A possible logic page subassembly is shown in Figure 3A3-11. The subassembly consists of two multilayer interconnection boards (MIBs) with metal heat transfer strips bonded to their outer surfaces. The MIBs are bonded to a page structure. Metal bars are provided on page edges to interface with spring clips on MSU structure inside the walls. A pluggable Burndy connector is attached to the bottom of the subassembly.

The dimensions of the page subassembly are 6.5 x 6.5 x 0.4 inches. This size is compatible with the memory subassembly.

Hybrid Module

A typical hybrid module package is shown in Figure 3A3-12 and consists of a flat pack case with external contacts, a substrate which accommodates discrete chip devices plus thick film resistors and conductors, and a package cover. The hybrid module will be made by conventional thick film technologies and processes. Approximate dimensions of the hybrid module are 1 x 1 x .18 inches.

Component Mounting and Interconnection

Hybrid modules and T^2L flat packs are bonded to the heat transfer strips. Their terminals are surface soldered to conductor patterns on the multilayer board between the metal strips. The package concept also accepts discrete components.

To achieve high density packaging, MIBs are used to interconnect the modules. MIBs are made of several layers of etched copper polyimide film laminates that are bonded together under heat and pressure. A Burndy edge connector connects the logic subassembly to the memory subassembly and the exterior equipment via distribution panel and I/O connectors.

3A3.6 Subassembly Thermal Design

Power analyses on the MSU design indicated an average thermal dissipation of approximately five watts for each memory subassembly and 6 watts for each logic page subassembly. This calls for a special thermal consideration of the logic page design.

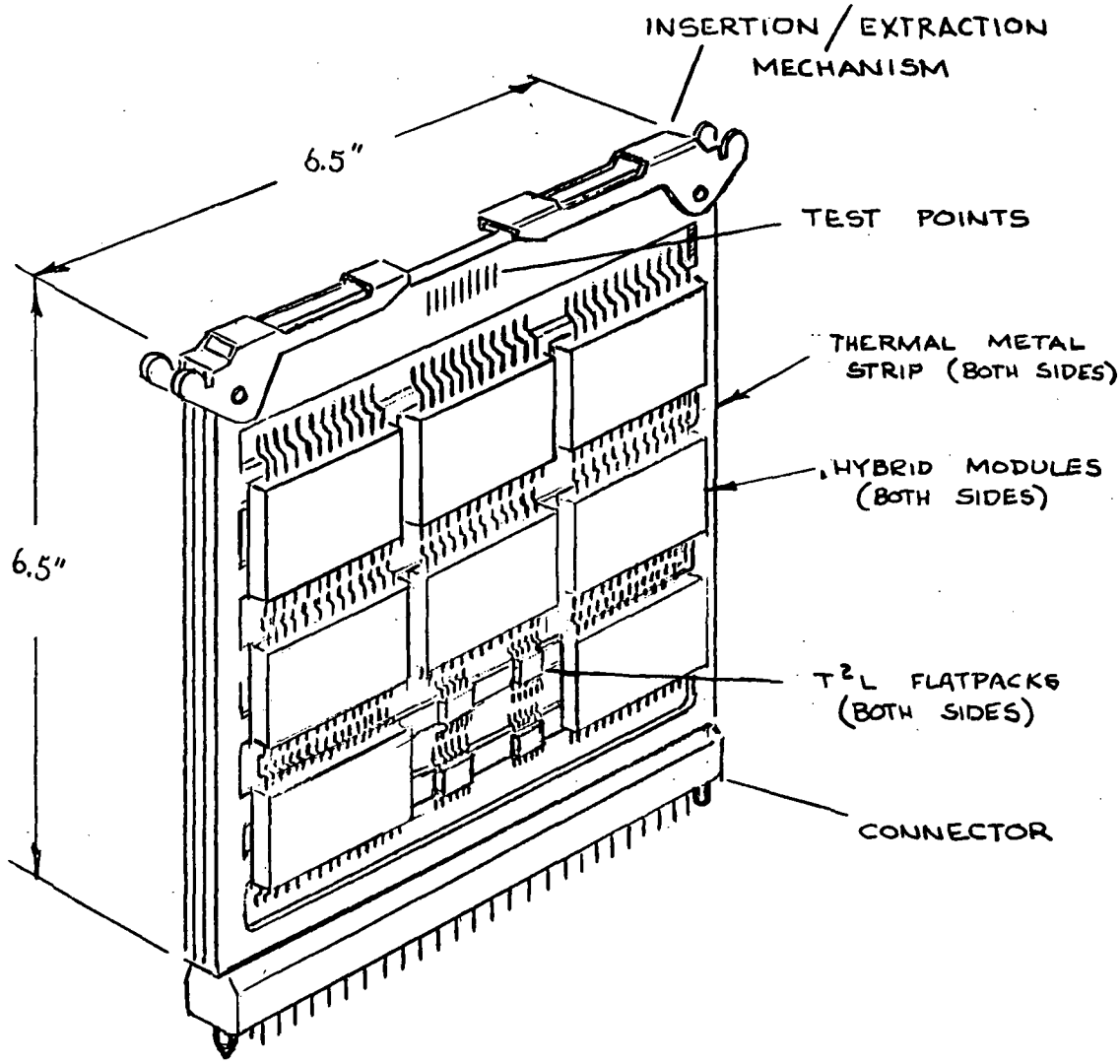


Fig. 3A3-11 Pluggable Logic Subassembly (Page)

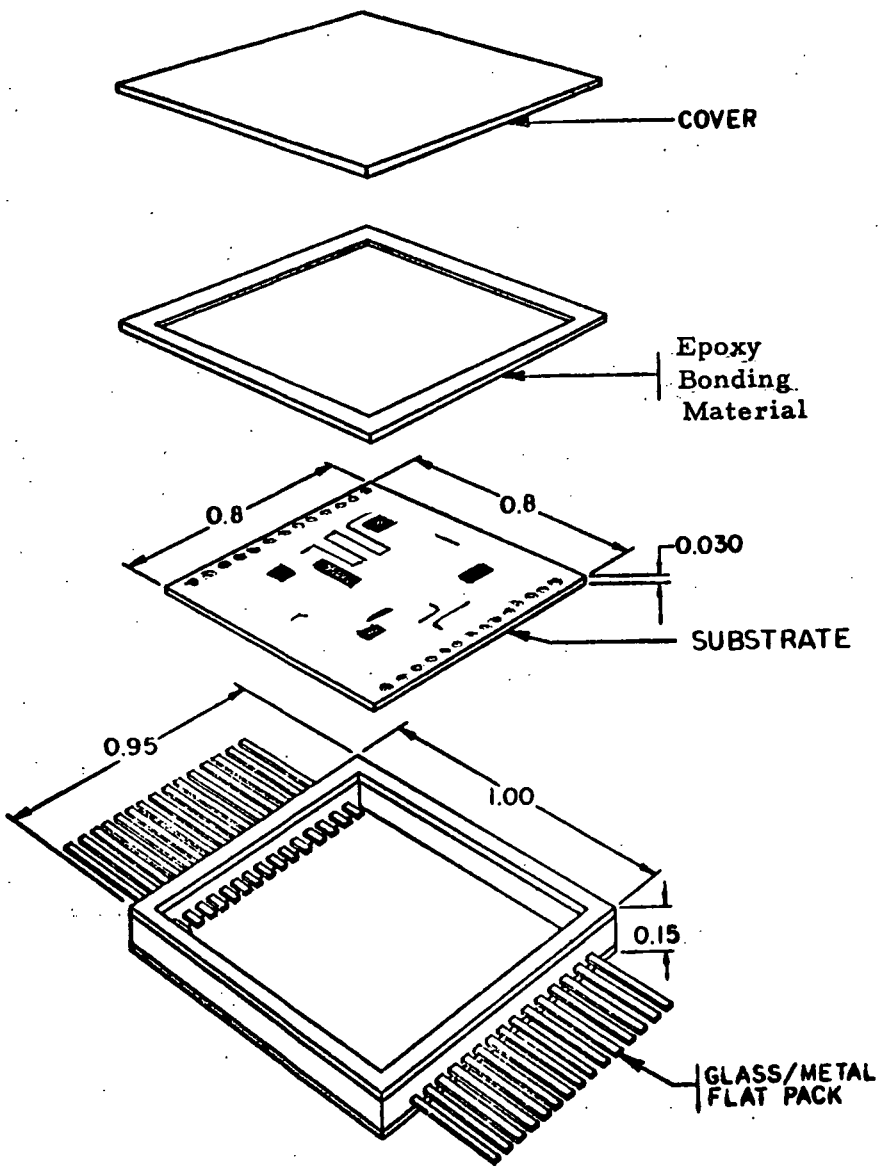


Fig. 3A3-12 Hybrid Module

An important page design consideration is incorporation of adequate thermal paths for conducting heat away from the components. This is achieved by structurally bonding metal heat strips on the surface of each MIB. The modules are bonded directly on the heat strip by conductive epoxy.

Heat is transmitted from the chip through the hybrid module base and the conductive epoxy to the metal bars on the page. Removal of heat from the metal bars is accomplished by thermal spring clips provided on the MSU structure inner walls.

This thermal design has the unique feature of variable conduction capacity for individual module page subassemblies. Preliminary thermal calculations indicate the page subassembly design of Figure 3A3-11 will handle 14 watts power dissipation.

3A3.7 Subassembly Installation and Interconnection

The subassemblies (logic and memory) plug into the distribution backpanel and are guided into place by the spring clip on the structure. These clips provide edge support to the subassembly; additional supports are from the backpanel connector and a restrainer on the MSU cover.

Interconnections between subassemblies are made through the distribution panel assembly in which a multilayer printed circuit board is bonded to a metal support plate and connector receptacle terminals are soldered to plated through holes in the board. Interconnections between the distribution panel in the MSU and to the external connectors are made via flat cables.

3A3.8 Reliability and Maintainability

Chip Joint Reliability

The reliability of flip chip joining to substrate by reflow soldering has been very good based upon test data and field experience with IBM System/360 computers. The mechanical stability of the strong ball interconnection has been shown in many life tests including thermal cycle, vibration, shock and centrifuge, and is also reflected by a failure rate in the field of .00002 percent per 1000 hours, which is superior to high reliability "flight level" TC bonds. The controlled collapse connection is estimated to have a failure rate less than .00001%/terminal/1000 hours. [T71].

The high tensile strength of the soldered terminal of the IBM SLT chip is credited for excellent mechanical and electrical stability in a

product built with flip chips. Tests show approximately 300 grams of normal force are required to pull a three ball terminal SLT chip away from the substrate, while comparing to a single, 1-mil diameter thermo-compression bonded gold wire usually withstands less than 10 grams of load before breaking.

The difference in thermal expansion coefficient between Si and Alumina and the known susceptibility of Pb-Sn solder to thermal cycle fatigue failure led to concern relating to the reliability of the memory flip chip solder joints. Available test data indicate that the expected failure rate due to thermal fatigue mechanism, for 112 mil square chips with 23 terminals, is 10^{-7}% per 1000 hours. This seems to indicate no problem is anticipated in flip chip joints due to thermal fatigue. However, for a substantially larger chip size like our memory chip of 200 mil square, additional analysis and test are necessary to determine the acceptable limit of fatigue failure rate. Preliminary calculations, however, are encouraging.

Reliability on Connections (other than chip joint)

Without exception, soldering is used to join component parts to both the memory subassembly and the logic page subassembly. Also, pluggable connections are employed to join both subassemblies to the next level assembly. Both joining techniques were employed and proven reliable in many previous aerospace programs.

Maintainability

The pluggable modular design concept provides mobility and ease of maintenance to both subassemblies (memory and logic). The mechanical structure design of the MSU permits replacement of individual subassembly by merely removing the top cover. The construction of each subassembly allows repair to component level. Adequate test points are provided on each subassembly to facilitate ease of electrical checkout and trouble-shooting.

In addition, partitioning of eight memory modules to share a common propagation drive by wiring their control lines in series greatly reduces the MSU wiring requirement and isolation fault time, and therefore reduces the frequency of MSU maintenance.

3A3.9 Environmental Considerations

Though no detailed environmental effects analysis has been performed in the course of MSU packaging design, the conceptual design configuration of the MSU shown in Figure 3A3-7 was established with broad considerations on environmental protection and with proven design features

which were successfully used in previous space programs. Representatives of these considerations are as follows:

a. In order to provide design with thermal characteristics compatible with worst case Space Shuttle environments, conductive heat transfer techniques were employed as the primary means of conveying heat from components to the thermally controlled cold plate on the Shuttle. Considerations also were given to thermal path, joint interfaces design in order to minimize component temperature rise and thereby providing maximum thermal protection for the MSU.

b. Vibration considerations include combining modules, subassemblies and distribution penal assembly into a rigid unit. This is accomplished by making these parts mutually supported and restrained.

c. A low unit leak rate under high pressure differentials is enhanced by using a one-piece housing structure and an effective seal for the cover and external connectors. This also provides the MSU dust-and humidity-free protection.

d. Preliminary study indicates radiation, electromagnetic pulse (EMP) appears to cause no adverse effects on the MSU under present Shuttle environmental levels.

However, it is important to point out that detailed thermal, vibration and other environmental analyses are essential in determining the environmental effects design parameters required for a final design of the MSU.

3A3-10 Conclusions and Recommendations

- The MSU packaging concept established by this study is a workable design that can be implemented into hardware with some refinement in design details and identification of material and processes requirements.

- The MSU packaging design meets the weight requirement of a storage system specified for space shuttle application, and exceeds the volume requirement by only 3%. It also compares favorably from the viewpoint of packaging density in terms of bits per pound and bits per cubic foot with a current tape system of same storage capacity (10^8 bits). It dissipates 10% more power over that of both systems. (See Table 3A3-5 for detailed comparison).

- In order to realize the full potential of the packaging concept established from this study, it is suggested that work be pursued to evaluate and determine materials compatibility and manufacturing processes necessary for MSU hardware implementation.

- It is also recommended a detailed, comprehensive thermal and vibration and other environmental effects analyses be performed in determining the environmental effects design parameter necessary for a final design of an MSU.

TABLE 3A3-5

MEMORY TECHNOLOGY COMPARISON

Memory Technology	Company	Total Bits K	Size Inches	Volume Ft^3	Weight Lbs	Wt. densi-tylb/ft^3	Bits/ Ft^3	Bits/ Lb	Tot. Pwr Watts	Watts/ Ft^3	Watts/ Lb.
Toroidal Core	IBM 4 Pi	288	12.8x3.2x9	.21	11.2	53	1400K	26K	78	370	7.0
Bubble	IBM proposed MSU	10^5K	7.25 x 8 x 9	.3	27.4	91	3.3 x 10^5K	3.7 x 10^3K	22	73	0.8
DRO Thin Film	CDC	288	6x7.5x9.6	.25	20	80	1200K	14K	40	160	2.0
MOSFET	Litton	32K	7.5x4.3x6	.011	.68	62	2900K	47K	---	---	---
Tape	--	10^5K	---	1.0	50	50	10^5K	2x10^3K	20	20	0.4
For Space Shuttle Application											
Any Memory System	Space Shuttle Application	10^5K	---	.29	30	104	3.4 x 10^5K	3.3 x 10^3K	20	69	0.66

	Volume Ratio	Weight Ratio	Power Ratio
MSU / Tape	.3	.55	1.1
MSU / Shuttle	1.03	.91	1.1

3A4 ERROR DETECTION AND CORRECTION REQUIREMENTS FOR BUBBLE MEMORIES*

3A4.1 Probable Failure Modes

A preparatory phase of formulating a highly-reliable structure for a bubble memory requires careful determination of failure modes for the class of devices to be used in the complete system implementation. Predication of classes of device failures for the complete memory system is thus used to impose redundancy constraints to assure the desired system reliability and availability. And, as will be explained subsequently in this report, the class of device failure modes for those devices implementing the circuitry used to enhance the reliability should also be considered. These considerations are based primarily upon the relative amount of circuitry used to implement the reliability - enhancement features.

For the bubble memory system under discussion in this report, two organizations were considered in detail: the bit per plane (also called bit-per-module), and the bit per chip. These two organizations were dictated by both power consumption and restriction of error effects. In the bit per plane organization, the largest fraction of possible malfunctions have been found to give rise to single bit errors in the data word. The bit per chip organization will suffer from some failure modes which manifest themselves as multiple bit errors in the data word. Finally, it is also possible that burst errors will be formed in the output data word as a result of some memory device failures

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*The work done on error detection and correction in this report was performed, in part, by Dr. E. P. Hsieh and Dr. A. B. Wadia, Research Division, IBM Corporation, working on an IBM, FSD, Huntsville IRAD Contract.

(the input terminal of a Decode and Clear line stuck at ground potential). These will have the characteristic of logically inverting a group of bits in the output word.

3A4.2 Required Encoding for Prevalent Failure Modes

In the previous section, it was explained that both independent random errors, usually single or double in number, can be found in bubble memories, as well as larger groups of errors. To overcome the effects of such data word errors, a special type of encoding must be used on the words being stored in the bubble memory. Extra bits (check bits) must be appended to the data word bits to permit detection and correction functions to be performed. In previous memory system organizations, the memory device failure modes manifested themselves as either single or, with lesser probability, double data bit errors. The effects of such errors were normally overcome by use of a single-error-correcting, double-error-detecting code (SEC/DED code). Check bits were appended to the data word to permit location and inversion of a single erroneous data bit or to provide system notification in the case of a double data bit error. The bubble memory system considered here, however, will have its words encoded, in a fashion to be described next, so that, as the subdivisions of the word suffer from one or more bit errors, all the errors within one such group of bits will be regarded by the decoding circuitry as a single error within its capacity to correct. Hence, the data word encoding used is referred to as single b-adjacent error-correcting, double b-adjacent-error-detecting (SbEC/DbED) and the error here can be the inversion of as many as all of the bits in the group (one data word subdivision).

The decoding circuitry used will be referred to as a translator because

of its multiple utility. It will not only decode and encode words in the SbEC/DbED format but it will perform the encoding as a translation from byte-parity encoded form to SbEC/DbED form and the decoding as a translation from SbEC/DbED form to byte-parity encoded form. In addition, as will be explained later in more detail, this translator will be designed to be self-testing. The code and its characteristics will be explained first.

3A4.3 The Chosen Code and Its Characteristics

It is well known [P61] that if α is a generating element for the finite field GF[2^b] then the parity check matrix for SEC/DED codes with elements in this field and 4 data bits may be written as

$$\begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 0 & 0 \\ 1 & \alpha & \alpha^2 & \alpha^3 & 0 & 1 & 0 \\ 1 & \alpha^2 & \alpha^4 & \alpha^6 & 0 & 0 & 1 \end{bmatrix}.$$

In 1959, J. Cocke [C59] showed that in the SEC case, α and 1 could be replaced by the corresponding b x b matrices with elements in GF[2], and all decoding and encoding could be done with ordinary Boolean algebra. In this case the correction is for elements in the field GF[2^b], which can be written as vectors of length b with elements in GF[2].

Bossen [B70] called the SEC encoding b-adjacent and gave an elementary description of the code and methods for encoding and decoding, both combinational and using shift registers.

For the bubble store the codes formerly described will be extended first

to the Single b-adjacent Error Correcting/Double b-adjacent Error Detecting case, and b will be taken to be 16. One will be replaced by the 16 x 16 identity matrix I and α will be replaced by the 16 x 16 matrix with primitive minimum equation $\lambda^{16} + \lambda^{10} + \lambda^{7} + \lambda^{6} + 1 = 0$ and minimum number of 1's [C69].

$$A = \begin{bmatrix}
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}$$

The parity check matrix may be rewritten as

$$\begin{pmatrix}
I & I & I & I & I & 0 & 0 \\
I & A & A^2 & A^3 & 0 & I & 0 \\
I & A^2 & A^4 & A^6 & 0 & 0 & I
\end{pmatrix}$$

Let S_1 represent the vector of syndrome bits $\begin{pmatrix} s_1 \\ \vdots \\ s_{16} \end{pmatrix}$, S_2 represent $\begin{pmatrix} s_{17} \\ \vdots \\ s_{32} \end{pmatrix}$ and S_3 represent $\begin{pmatrix} s_{33} \\ \vdots \\ s_{48} \end{pmatrix}$. If $e' = (e_1, .., e_{16})$ represents any of the 2^{16} -1 error patterns in a 16-adjacent group, then the equations to encode and decode are easily derived.

Clearly,

$$\overline{S}_1 = e'^T$$

$$\overline{S}_2 = A^i e'^T$$

$$\overline{S}_3 = A^{2i} e'^T.$$

Number the groups 1 to 7.

$$G1 = (\overline{S}_2 = \overline{S}_1) \wedge (\overline{S}_3 = \overline{S}_1)$$

$$G2 = (\overline{S}_2 = A\overline{S}_1) \wedge (\overline{S}_3 = A\overline{S}_2)$$

$$G3 = (\overline{S}_2 = A^2\overline{S}_1) \wedge (\overline{S}_3 = A^2\overline{S}_2)$$

$$G4 = (\overline{S}_2 = \overline{A}^3 S_1) \wedge (\overline{S}_3 = A^3 \overline{S}_2)$$

$$G5 = (\overline{S}_2 = 0) \wedge (\overline{S}_3 = 0)$$

$$G6 = (\overline{S}_1 = 0) \wedge (\overline{S}_3 = 0)$$

$$G7 = (\overline{S}_1 = 0) \wedge (\overline{S}_2 = 0)$$

The correction equations are

$$d_{ijc} = d_{ij} \oplus \overline{s}_i \; G_i \qquad i = 1,..,\, 16; \qquad j = 1,2,3,4$$

$$c_{ijc} = c_{ij} \oplus \overline{s}_i \; G_i \qquad i = 1,...,16; \qquad j = 5,6,7$$

The Boolean equations are as follows. If the error is in group G_i the set of equations $G_i = 1$ and all others are zero. If there is no error all $G_i = 1$.

The following equations define the S16EC/D16ED code with 64 data bits, $d_1,..., d_{64}$ and 48 check bits $c_1,..., c_{48}$. Matrix and vector notation will be used in general, but some equations will be written in normal Boolean algebra notation, with $\wedge$ (AND), $\vee$ (OR), $\oplus$ (XOR, i.e., Exclusive OR), ' (NOT).

The parity check matrix is, as before,

$$\begin{pmatrix} I & I & I & I & I & 0 & 0 \\ I & A & A^2 & A^3 & 0 & I & 0 \\ I & A^2 & A^4 & A^6 & 0 & 0 & I \end{pmatrix}$$

where A was previously defined.

$$\begin{pmatrix} s_1 \\ \vdots \\ s_{16} \end{pmatrix} = I \begin{pmatrix} d_1 \\ \vdots \\ d_{16} \end{pmatrix} + I \begin{pmatrix} d_{17} \\ \vdots \\ d_{32} \end{pmatrix} + I \begin{pmatrix} d_{33} \\ \vdots \\ d_{48} \end{pmatrix} + I \begin{pmatrix} d_{49} \\ \vdots \\ d_{64} \end{pmatrix} + I \begin{pmatrix} c_1 \\ \vdots \\ c_{16} \end{pmatrix}$$

or $s_i = d_i \oplus d_{16+i} \oplus d_{32+i} \oplus d_{48+i} \oplus c_i \quad i = 1, \ldots, 16$

$$\begin{pmatrix} s_{17} \\ \vdots \\ s_{32} \end{pmatrix} = I \begin{pmatrix} d_1 \\ \vdots \\ d_{16} \end{pmatrix} + A \begin{pmatrix} d_{17} \\ \vdots \\ d_{32} \end{pmatrix} + A^2 \begin{pmatrix} d_{33} \\ \vdots \\ d_{48} \end{pmatrix} + A^3 \begin{pmatrix} d_{49} \\ \vdots \\ d_{64} \end{pmatrix} + I \begin{pmatrix} c_{33} \\ \vdots \\ c_{48} \end{pmatrix}$$

$$s_{33} = d_1 \oplus d_{19} \oplus d_{37} \oplus d_{49} \oplus d_{55} \oplus c_{33}$$

$$s_{42} = d_{10} \oplus d_{28} \oplus d_{46} \oplus d_{64} \oplus c_{42}$$

$$s_{38} = d_6 \oplus d_{18} \oplus d_{24} \oplus d_{33} \oplus d_{36} \oplus d_{41} \oplus d_{51} \oplus d_{54} \oplus d_{60} \oplus c_{38}$$

The number of terms XOR'd together range between 5 and 10, and the examples show the limiting cases.

The pointer equations G_i, $i = 1,\ldots,7$ have the following equations

$$G_1 = \left[I \begin{pmatrix} s_1' \\ \vdots \\ s_{16}' \end{pmatrix} = I \begin{pmatrix} s_{17}' \\ \vdots \\ s_{32}' \end{pmatrix} \right] \wedge \left[I \begin{pmatrix} s_1' \\ \vdots \\ s_{16}' \end{pmatrix} = I \begin{pmatrix} s_{33}' \\ \vdots \\ s_{48}' \end{pmatrix} \right]$$

G_1 is the AND of 32 two variable equality circuits. Let

$$f_i \equiv (s_i' = s_{16+i}') \qquad i = 1,..,16$$

in basic Boolean operators

$$f_i = s_i' \, s_{16+i}' \vee s_i \, s_{16+i}$$

and let $g_i \equiv (s_j' = s_{32+j}')$. Now

$$G_1 = \left(\bigwedge_{i=1}^{16} f_i \right) \wedge \left(\bigwedge_{j=1}^{16} g_j \right)$$

$$G_2 = \left[I \begin{pmatrix} s_{17}' \\ \vdots \\ s_{32}' \end{pmatrix} = A \begin{pmatrix} s_1' \\ \vdots \\ s_{16}' \end{pmatrix} \right] \wedge \left[I \begin{pmatrix} s_{33}' \\ \vdots \\ s_{48}' \end{pmatrix} = A \begin{pmatrix} s_{17}' \\ \vdots \\ s_{32}' \end{pmatrix} \right]$$

G_2 is the AND of 28 two variable equality circuits and 4 three variable equality circuits of the form

$$s_{25}' = s_1' + s_{10}'$$

$$G_3 = \left[I \begin{pmatrix} s_{17}' \\ \vdots \\ s_{32}' \end{pmatrix} = A^2 \begin{pmatrix} s_1' \\ \vdots \\ s_{16}' \end{pmatrix} \right] \wedge \left[I \begin{pmatrix} s_{33}' \\ \vdots \\ s_{48}' \end{pmatrix} = A^2 \begin{pmatrix} s_{17}' \\ \vdots \\ s_{32}' \end{pmatrix} \right]$$

G_3 is the AND of 24 two variable equality circuits and 8 three variable equality circuits of the type described earlier.

$$G_4 = \left[I \begin{pmatrix} s'_{17} \\ s'_{32} \end{pmatrix} = A^3 \begin{pmatrix} s'_1 \\ s'_{16} \end{pmatrix} \right] \wedge \left[I \begin{pmatrix} s'_{33} \\ s'_{48} \end{pmatrix} = A^3 \begin{pmatrix} s'_{17} \\ s'_{32} \end{pmatrix} \right]$$

G_4 is the AND of 20 two variable equality circuits and 12 three variable equality circuits of the type described earlier.

$$G_5 = \bigwedge_{i=17}^{48} s_i$$

$$G_6 = \left(\bigwedge_{i=1}^{16} s_i \right) \wedge \left(\bigwedge_{i=33}^{48} s_i \right)$$

$$G_7 = \bigwedge_{i=1}^{32} s_i$$

The connection circuits have the following equations

$$d_{((i-1)16+k)c} = d_{16(i-1)+K} + G_i \bar{s}_K \quad i = 1,2,3,4,\ K = 1,\ldots,16$$

$$c_{ic} = c_i + G_5 \bar{s}_i \quad i = 1,\ldots,16$$

$$c_{ic} = c_i + G_6 \bar{s}_i \quad i = 17,\ldots,32$$

3A4.4 Translator Implementation

Now that the characteristics of the code have been explained, the implementation of the translator can be explained in detail. The structure of the translator in several respects, will be similar to that previously discussed in the literature [CEA70, CJW70] for simpler codes.

General Structure of the Translator

The general structure of the translator to be used for the bubble memory system is shown in Fig. 3A4.1. When an encoded word is read from the main store, it is first loaded directly into a register indicated at the top of Fig. 3A4.1. At this point the data and check bits are fed into the Syndrome Generator so that the syndrome vector, S, can be generated. Once the syndromes have been generated, they, in turn, can be used to generate the Group Pointers through the Group Pointer Generator shown. Once both the Syndrome and Group Pointer sets have been formed, they can be used to form the corrective conjunct terms to be added, modulo two, to the data and check bits. Thus, a single group error is corrected by forming the correct set of data and check bits in the Single Group Error Corrector from the memory output word, the syndromes formed, and the group pointers generated. Once the corrected word is formed, the data bits are fed through a Parity Encoder to generate byte parity for eventual removal over the system buss. The output of the Parity Encoder is gated into one of the two Memory Data Registers (MDR), which are used in an alternating fashion to maintain the desired memory output rate. The corrected check bits just stored are now used in conjunction with the corrected data bits to check for double errors as in [CJW70]. The other check is provided by an RCCO reduction of the self-testing line pairs produced as dual outputs of self-testing parity trees used to take parity across each

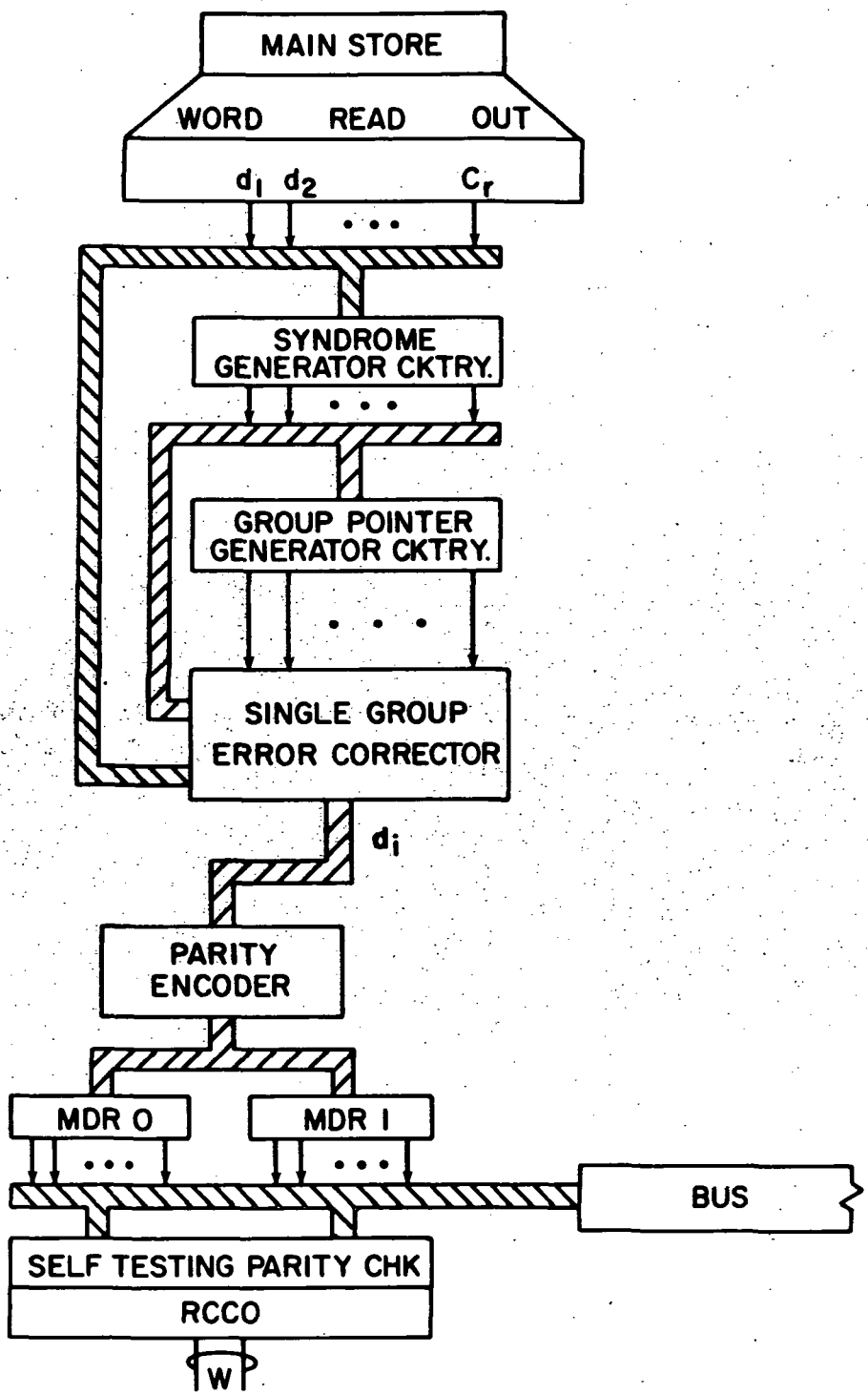

Fig. 3A4-1 General Structure of Translator

byte of the MDR. The general concepts of self-testing logic, as well as self-testing parity trees, has been discussed previously [CEA70, CJW70, CWJ71] and will not be presented here.

The implementation of the translator is achieved by a combination of functions implemented in a conventional fashion with functions implemented in self-testing circuitry. This permits the implementation to be self-testing over its range of operation in both code and error spaces while preserving a circuitry economy. A specific translator for a 64-data bit, 32-checkbit, 16-bit group on a 6-plane structure will be discussed in more detail later.

The Corrector Functions

The function of the Syndrome Generator circuitry is to form the code syndromes from the data word bits as provided by the Parity Check Matrix. explained previously, that is, a given syndrome, associated with a row of this matrix, is defined as the sum modulo two of all data and check bits having entries which are 1 in that row of the parity check matrix. A typical equation defining a syndrome is thus seen to be defined by the logic 1 entries in the Parity Check Matrix described in Section 3A4.3, previously. A typical circuit for a syndrome is shown in Figure 3A4.2. The syndromes themselves are used to form the Group Pointers and are to be also directly used in forming the corrective conjunct.

The Group Pointer Generator

The function of the Group Pointer Generator circuitry is to uniquely identify which of the sixteen bit groups contains the error to be corrected. The group pointers are actually utilized in the Single Group Error Corrector as one variable in the corrector conjunct. A typical equation defining a group

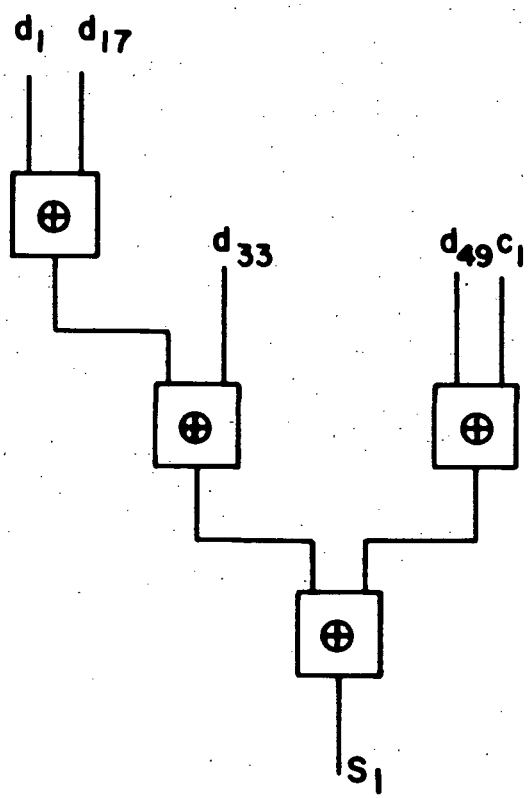

Fig. 3A4-2 Typical Circuit for a Syndrome

pointer is also seen to be given by the equations of Section 3A4.3. One such typical equation for a group pointer may be written as

$$G_2=(\overline{S_5}=\overline{S}_1) \wedge (\overline{S}_6=\overline{S}_2) \wedge (\overline{S}_7=\overline{S}_1 \vee \overline{S}_4) \wedge (\overline{S}_8=\overline{S}_1) \wedge (\overline{S}_9=\overline{S}_3)$$

$$\wedge (\overline{S}_{10}=\overline{S}_1 \vee \overline{S}_4) \wedge (\overline{S}_{11}=\overline{S}_1 \vee \overline{S}_2) \wedge (\overline{S}_{12}=\overline{S}_2) \qquad (2)$$

and this is implemented as shown in Fig. 3A4.3.

The Single Group Error Corrector

The final function implemented is the Single Group Error Corrector. This circuitry is actually a set of replication of smaller logic circuits, one of each such small circuit being uniquely associated with one bit of the data word. The theory behind the operation of each small circuit, as shown in Fig. 3A4.4, has already been explained in Section 3A4.3. A corrective conjunct is formed from the group pointer and the syndromes. Thus, a unique conjunct is formed from a group pointer and a particular pattern of the syndromes. The group pointers, in its logic 1 state, identified the 16 bit group in which the correction is to be made. The particular syndrome pattern, producing a logic 1 for the other terms of the conjunct, identified the bits of the group specified to be corrected (inverted). Thus, this conjunct assumes a logic 1 state, a set of bits of single group will be corrected via an Exclusive OR(XOR) block unless all applicable syndromes are 1. This, of course, follows from the equation $\zeta_i + 1 = \zeta_i' = \zeta_{ic}$, where ζ_i, is the i^{th} bit of the word (either a data or a check bit) with complement ζ_i'. Hence, if ζ_i is known to be incorrect, its correct form ζ_{ic} is seen to be ζ_i'.

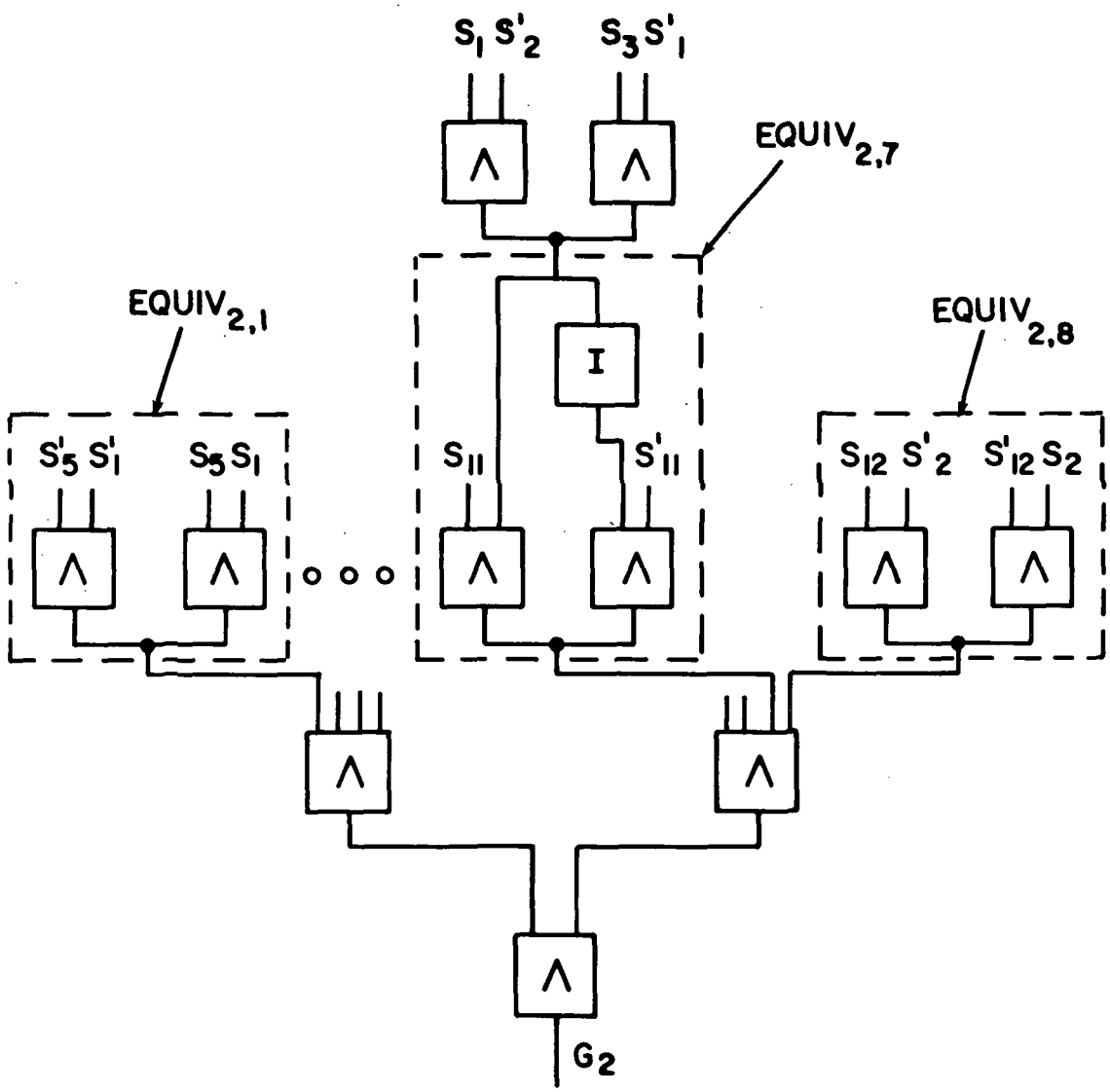

Fig. 3A4-3 Implementation of Group Pointer Equation

3A4.5 The READ and WRITE Processes

The process of reading and writing with a bubble main store having a translator of the type shown in Fig. 3A4.1 can be explained as follows.

The READ Process

Upon initiation of a READ request, the word is dropped into the Data Word Register (DWR) directly from the sense amps. The bits of the word are first gated into the Syndrome Generator and then into the Group Pointer Generator to form the syndrome pattern and the group pointer pattern. These two pattern sets are then gated directly into the Single Group Error Corrector so that single group errors can be corrected. The corrected data bits are then gated through the Parity Encoder and into a Memory Data Register (MDR). Each byte of data now in the MDR has a byte parity bit assigned to it by the Parity Encoder. The newly generated parity bits are gated to give the double error indication previously discussed. The final check on the parity encode data in the MDR is afforded by a set of self-testing parity checks performed on each data byte in the MDR and resulting in the self-testing signal pair, W. After all such checks are queried to ascertain the correctness of the word in the MDR, the error-free word can be gated out of the MDR and onto the bus for use elsewhere.

The WRITE Process

The preparation of a word to be written into main store requires the sequence of steps taken in a READ access to be taken in the reverse sense. The same physical hardware of the translator would be used. The word to be placed into a memory location is taken off the bus, in parity-encoded form, and re-encoded by the translator into the SEC/DED code form.

The parity-checked word is gated into one of the MDR buffers (for a given time pulse) from the bus. The parity of the incoming word is then checked

by the self-testing parity tree producing W. If W is in code space, the parity is correct for the incoming word and no single circuit failure has occurred in the parity-check circuitry out to W. Once the parity of the incoming has been verified as correct, the data bits of the word stored in the MDR can be gated through the syndrome XOR trees to obtain the code check bits that are stored in the sense-amp-fed register. The data bits from the MDR and the newly generated check bits may then be stored in the desired memory location.

3A4.6 Translator Circuit Failure Analysis

A single stuck failure in any circuit in the two self-testable checkers is detected in code space during normal operations. However, failures on lines providing single-rail signals are liable to accumulate if these lines do not change values in code space. Those failures that are untested over code space must be ultimately made detectable, either by themselves or as a combination of failures, over single error space.

To analyze the effect of circuit failures in the translator and to show how they are detected by the checkers provided, a detailed mathematical analysis must be carried out. This has been done, but the details will not be reproduced here because of the lack of general interest.

3A4.7 Reconfiguration and Recovery

The strategy for automatic repair of the bubble memory system is formulated upon the basis of being able to recover from error-inducing failures in the bubble planes, and the closely related electronics, as well as being able to survive one or more circuit failures in the translator which would impair its capacity to correct single errors or detect multiple errors properly or might mutilate a correct word. The recovery process for the bubble memory system of

this report is therefore based upon incorporating spares in the system for both the storage modules and the translator, as well as means for switching these spares in and out of operation.

3A4.8 Implementation of Subunit Switching Strategies

Sparing at the level of storage module units will be utilized to overcome the effects of a failure in a location which is to be considered unusable in that bits originating from that source will be erroneous for a pre-specified fraction of READ accesses. Replacement of such storage modules will occur after double or multiple b adjacent group errors have been detected.

Sparing and replacement of the translator will be utilized to overcome the effects of circuit failures within the translator. This reconfiguration must be performed to prevent the translator from operating with impaired capabilities due to an accumulation of circuit failures.

For the sake of modeling the storage modules for recovery, the storage system (no translator included) may be viewed as shown in Fig. 3A4.5. The memory unit, composed of q Basic Storage Modules (BSM) each contributing 16 bits to the word has s spare BSM's appended to it and must reconfigure these s units into the system as replacements when any of the original q, or a replacement from one of the spares, has failed. The BSM's would ordinarily accept the bits $d_{1i}, d_{2i} \ldots, d_{qi}$ $i = 1,\ldots,16$ as an input word on a WRITE access and produce the bits $y_{1i}, y_{2i}, \ldots, y_{qi}$ $i = 1,\ldots,16$ as an output word on a READ access. However, on the supposition that a failure condition will render one of the q BSM's inoperative, it is necessary to switch inputs into another unit and connect the outputs of the newly operative spare into the position ordinarily fed from the output of the failed BSM. For the switching used here, it will be seen that disconnection of a failed unit occurs simultaneously with its replacement by a

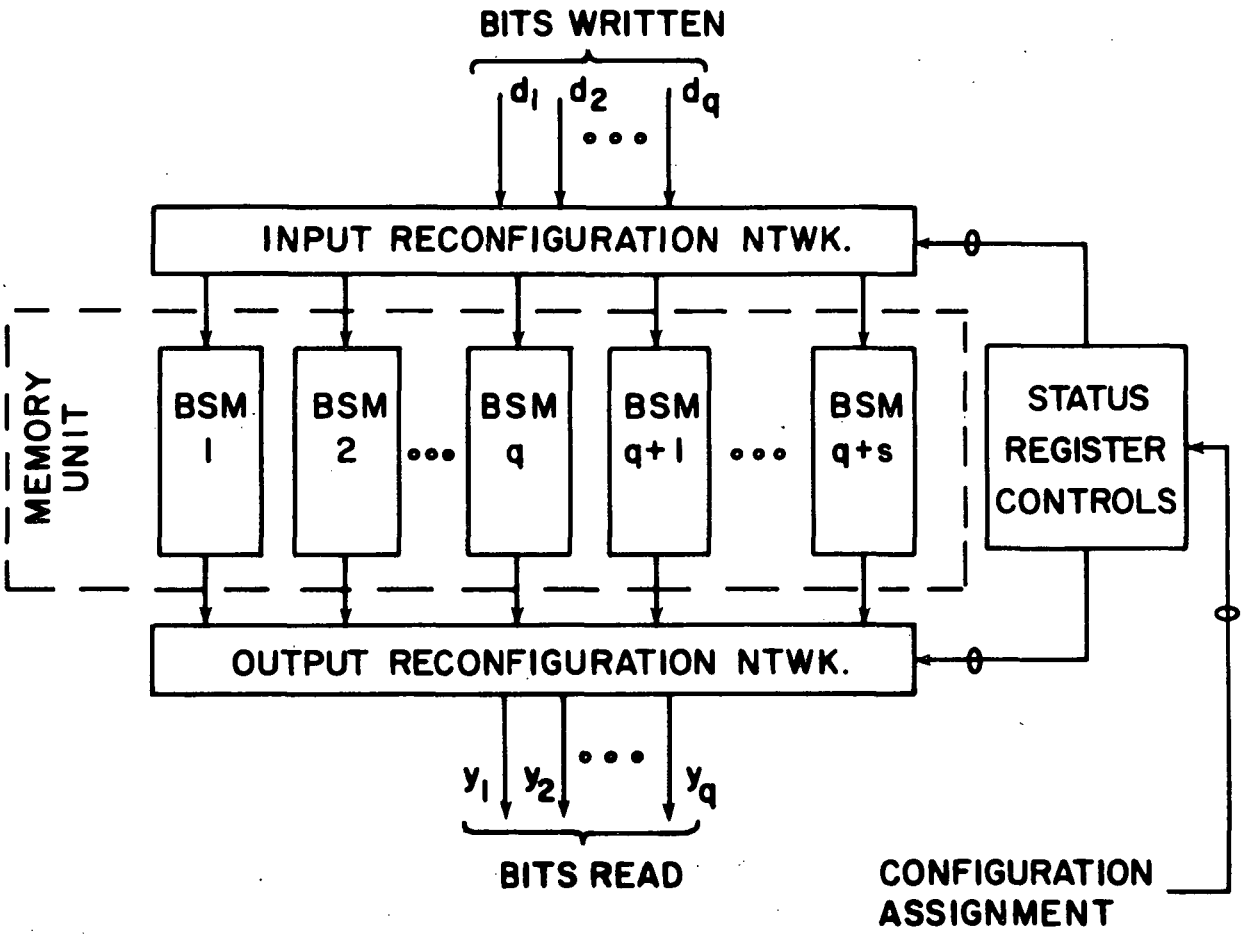

Fig. 3A4-5 Recovery in the Storage System

spare. The requisite reassignment of the inputs d_{ij} to the failed module, BSM_i, and its output y_{ij}, is here performed by embedding the q + s BSM's in between two logic circuits: the Input Reconfiguration Network (IRN) and the Output Reconfiguration Network (ORN). The output signals, y_{ij}, will be fed on to additional circuitry before being bussed away for use. The function(s) of this additional circuitry will be examined at greater length in later sections. The assignment of each of the d_{ji} to a BSM_k, by the IRN, and the assignment of a BSM_k to a y_{ji} by the ORN, will be governed by control signals generated by a set of registers, the Status Register Controls (SRC) which, in turn, function under the control of the Configuration Assignment (CA) line. The CA line may be directly under the Computer Supervisor program control. Supervisor control will also be used to carry out the individual loading of the BSM's as they are switched into operation within the Memory Unit. The memory unit may be refreshed, when switching, by reading out the words (with the ORN yet to be modified to reflect switching) and subjecting them to single group error correction. Then they may be written back into the new configuration of the memory unit by modifying the IRN into its post-switching status. At the termination the ORN is modified to effect the output connection reconfiguration and operation is resumed.

Several memory word encodings and final output buffer structures will be discussed in the section on Trade-offs. However, only one type of encoding and buffer structure will be considered in this section; the bubble store will be implemented for a bulk store (similar to a disc unit) and will be considered for its ability to output 64 x 1024 bit groups at a 10 μsec (100 kHz) rate. The general block diagram of a proposed highly reliable bubble memory system used for bulk memory applications is shown in Fig. 3A4.6. This is a simplex translator system configuration. The basic memory unit and reconfiguration networks depicted in Fig. 3A4.5 are now shown interconnected with the translator subunits and the buffer circuitry. The syndrome generation, group pointer generation,

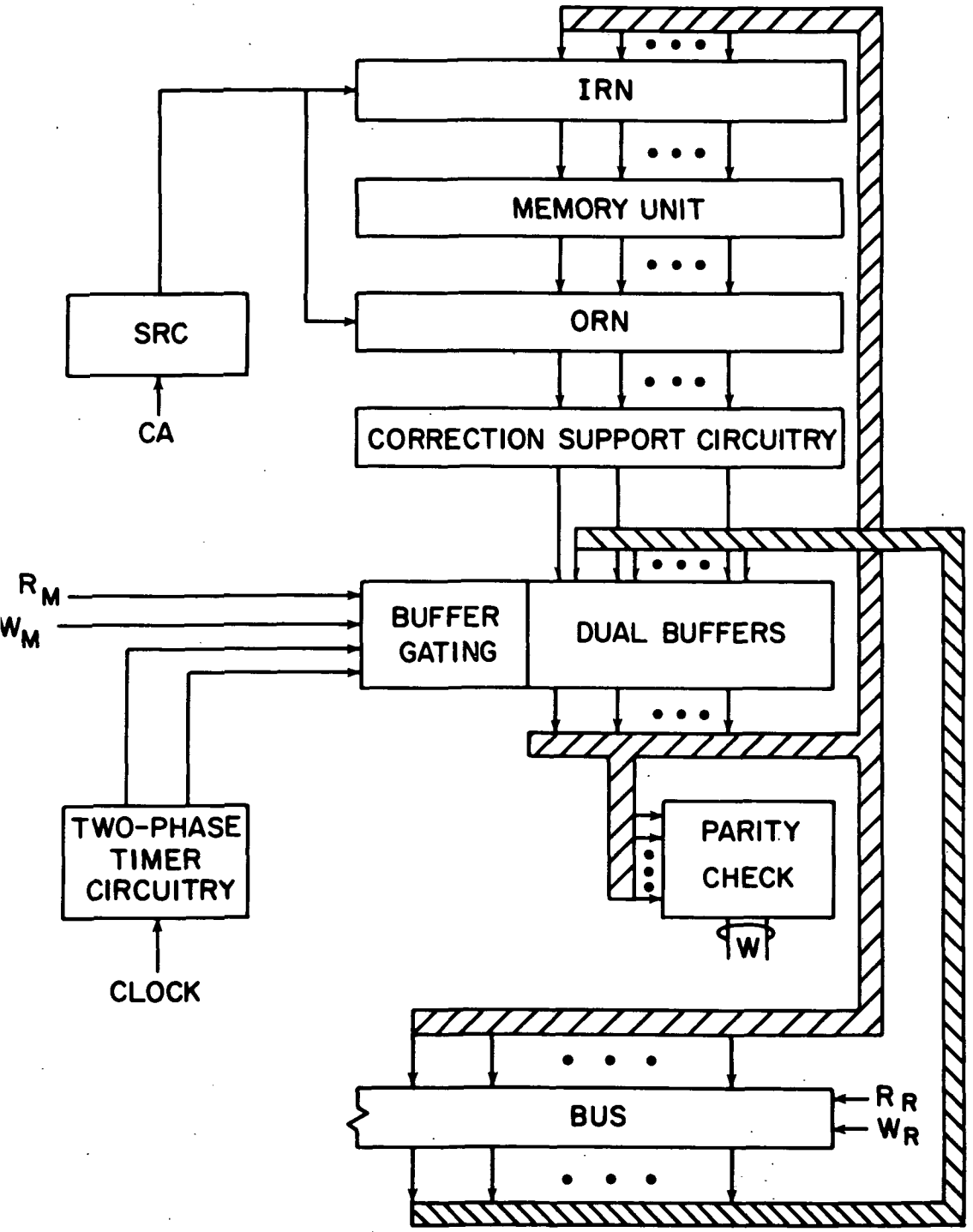

Fig. 3A4-6 Proposed Highly Reliable Bubble Memory System

single group error correction circuitry, and byte parity generation circuitry of Fig. 3A4.1 have now been combined, in Fig. 3A4.6, into the Correction Support Circuitry (CSC) fed directly from the ORN. A memory output word, with byte parity attached, is now gated directly into the Dual Buffer unit depicted in Fig. 3A4.6. The Dual Buffer unit is composed of two buffers, with associated controls, and replaces the MDR shown in the diagram of Fig. 3A4.1. The pair of registers in the Dual Buffer unit is used to permit serial accessing of the store with 64 x 1024 bit blocks at the desired 100 kHz rate and to permit convenient interconnection with faster electronic circuitry. The dual registers are used in an alternating manner to permit this method of store accessing and translation. Hence, a two-phase timing signal is generated (by the clock-driven Two-Phase Timing Circuitry) which, in conjunction with the control signals R_M (Read Memory) and W_M (Write Memory), permits successive, alternating input to be made to each of the two register halves of the Dual Buffer unit. The inputs to the Dual Buffer unit can originate from either the Correction Support Circuitry of the translator (for a Memory READ access) or from the bus (for a Memory WRITE access). The outputs from the Dual Buffer unit can be directed to either the bus for a Memory READ access or to the IRN for a Memory WRITE access. The Dual Buffer registers are loaded under the control of W_M and unloaded under the control of R_M; timing for loading and unloading the registers, as provided by the timer circuitry, is a signal pair (t_0, t_1) which is normally (0,1) or (1,0) for checking purposes. The bus is loaded from memory under the control of the signal R_R and unloaded to memory under the control of the signal W_R. The read/write operations are asynchronous, controls R_M and W_M being much slower than R_R and W_R, the circuitry connected to the bus. It has further been assumed here that no overrun or erroneous double access signals are possible.

In a READ access to memory, the data read out passes through the CSC and into one of the registers (dependent on the (t_0, t_1) value, as will be shown later) of the Dual Buffer unit before being dropped onto the bus. The CSC circuit failure check, and byte parity generation are performed before the word is gated onto the bus. In a WRITE access to memory, the word is gated from the bus to one of the registers of the Dual Buffer unit. Then the byte parity is checked and check bits are generated. The complete word is gated from the Dual Buffer unit to the memory. Figure 3A4.6 shows no data-transfer paths for the check bits. These paths have been purposely omitted to avoid unnecessary confusion for both the reader and Fig. 3A4.6. The transfer equations governing the exchange of data between the registers b_0 and b_1 in the Dual Buffer unit and the bus lines B can be expressed as follows:

$$b_0 = t_0 t_1' \ (R_M D \vee W_R B) \qquad \text{3A4 [1]}$$

$$b_1 = t_0' \ t_1 (R_M D \vee W_R B) \qquad \text{3A4 [2]}$$

for bus to buffer, and

$$B = R_R (t_0' \ t_1 \ b_0 \vee t_0 t_1' b_1) \qquad \text{3A4 [3]}$$

for buffer to bus. The term D is used here to represent data and check bits. The transfer equation governing the data input operation of the memory unit (MU) can be expressed by similar equations:

$$MU = W_M \ (t' t_1 \beta_0 \vee t_0 t_1' \beta_1) \qquad \text{3A4 [4]}$$

where β_0 and β_1 are the check bit set and the data bit portions of the b_0, b_1 registers, respectively. The equations 3A4 [1] - [4] then specify the contents of the subunit of the Dual Buffer unit provided as Buffer Gating, as well as the gating to and from the bus unit and the memory unit.

With this explanation of the system data exchange processes completed; the system description must now proceed with a detailed consideration of another exchange process carried out within the memory; the system reconfiguration by spare switching. As noted before, recovery requiring reconfiguration will only be performed within the memory unit, the Dual Buffer unit, and the Correction Support Circuitry: the bus has been assumed, throughout this discussion, to have no spare bit lines provided for bus line failures.

Referring once again to Fig.3A4-5, it should be noted that the reconfiguration of BSM's within the memory unit is conducted under the control of status registers, each of which is, in turn, controlled by a configuration assignment provided by the Computing System Supervisor. For a bubble bulk store with on spare BSM and no spare translator each BSM within the memory unit has a status register two bits long uniquely assigned to it. The outputs of these status registers are used, within the IRN, to determine which input word bit is located in a BSM and, within the ORN, to determine which BSM output is connected to a specific output terminal. The interconnection of input word bit, w_i, to BSM_j and BSM_j to output word bit, w_i, is defined as follows.

SR_i	IRN Interconnection	ORN Interconnection
00	w_i to BSM_i	$BSM_i \rightarrow w_i$
11	w_i to BSM_{i+1}	$BSM_i \rightarrow w_{i-1}$
10 or 01	BSM_i disconnected	

The even parity status of SR_i for an operative state of BSM_i permits easy identification of BSM's that are inoperative. Odd parity for a status register will mean that that status register is turned off.

As an example of this type of memory unit configuration, consider the case of four input and output lines being connected to four operating and initially unfailed BSM's and a spare BSM. With no failures initially, the following interconnections are observed:

IRN: $w_i \rightarrow BSM_i$,

ORN: $BSM_i \rightarrow w_i$,

and $SR_i = (0,0)$, for $i = 1,2,3,4,5$.

Suppose now that a failure occurs in BSM_3 which negates its ability to function is a normal system environment. Then, the reconfiguration is established as follows:

IRN: $w_1 \rightarrow BSM_1$, $w_2 \rightarrow BSM_2$, $w_3 \rightarrow BSM_4$, $w_4 \rightarrow BSM_5$

ORN: $BSM_1 \rightarrow w_1$, $w_2 \rightarrow BSM_2$, $BSM_4 \rightarrow w_3$, $BSM_5 \rightarrow w_4$

and SR is [(0,0), (0,0), (1,1), (1,1)]

So BSM_3 has now been reconfigured out of use.

The logic function formed by the IRN for this mode of reconfiguration can be expressed as

$$BSM_i = SR'_{io} S'_{ii} w_i \vee SR_{i-i,o} SR_{i-1,1} w_{i-1}$$

if BSM_i is not the failing BSM. Similarly, the logic function formed by the ORN can be expressed as

$$w_i = SR'_{io} SR'_{i1} BSM_i \vee SR_{i+1,o} SR_{i+1,1} BSM_{i+1}$$

if BSM_i is not the failing BSM. It should be understood that w_i represents no specific data bit value, but a terminal position for an input. The expression of the status register as SR_{io} and SR_{i1} merely refers to the two positions of the i^{th} status register flip-flops. Fig. 3A4-7 shows the circuit modules used to implement the IRN and ORN.

With this system of switching, a status register failure appears as a BSM failure and the erroneous effect of the status register failure is overcome by switching off the BSM associated with the status register. It should also be noted that a basic ground rule for switch design was observed in the design of the IRN and ORN. A failure in the switch should only disable the unit receiving the data. For this design, the gates comprising the switch may be added to the gates in the receiving unit for purposes of calculation in reliability modeling. In general, the rule for constructing the switch at a unit interface is that only the source unit lines may be fanned out. No switch gate may have its output fanned out or a single gate failure will affect more than one module.

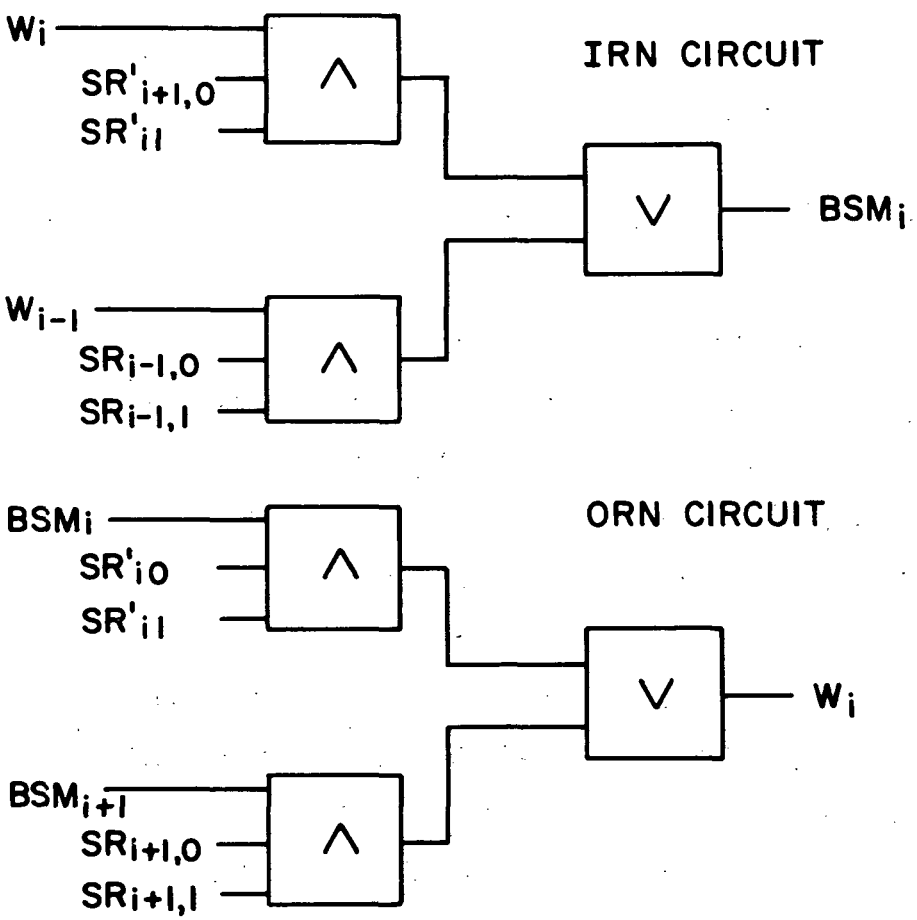

Fig. 3A4-7 Circuit Modules Used to Implement the Input-and Output-Reconfiguration-Networks.

Sparing, as noted above, will also be performed on two other subunits in the proposed bubble bulk memory system depicted in Fig. 3A4-6. Spare Correction Support Circuits will be added to permit replacement in the event of a circuit failure in that circuitry. Spare Dual Buffer units, with native Parity Check and correction circuits, will also be added. Hence reconfiguration can proceed in terms of the three basic subunits diagrammed in Fig. 3A4-8 sparing will be done on a BSM basis within the Storage System and on a subunit basis for the other two blocks of circuitry (the bus is not, of course, included in these considerations).

When a spare translation unit is included, three status bits are needed per BSM. The switches are similar but more complicated than those described above.

3A4.9 Implementation Costs of the Translator-Buffer Subunits

The amount of logic circuitry required for the complete implementation, sans spares, can be determined from a consideration of Fig. 3A4-6. For purposes of accounting, the following equivalences have been used. A register stage (one Set-Reset Flip-Flop) will count as four gates. An Exclusive-OR tree with n inputs will use 3n-4 gates. An RCCO tree of m input line pairs will use 4m-2 gates. The tabulation of Table 3A4-1 results as the gate count for the translator-buffer unit. This is for a 64 data-bit, 32 check-bit, 16-bit group, on a 6 plane structure of the bubble memory.

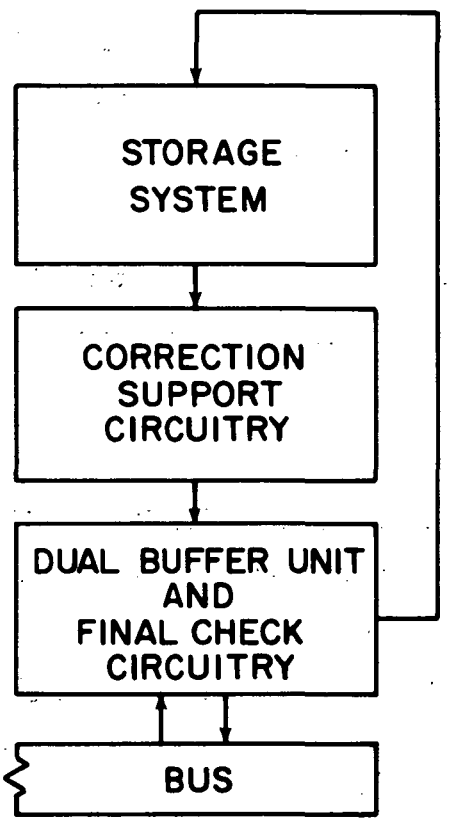

Fig. 3A4-8 Three Basic-Sub-Units Used for Re-Configuration

GATE COUNT CALCULATIONS

Subunit	Gate Count
Bus Connection Circuitry	292
Translator, Correction and Buffering	7095
Storage Connection	470
Total	7857

Table 3A4-1

3A4.10 Circuitry for Reliability Trade-Off Studies

The techniques described earlier for designing self-testing and self-checking translators and buffers to transfer data from the bubble store to a main bus were used to do paper designs for various cases for the reliability trade off study. The cases ranged from a simple 64 bit wide buffer with no checking and no spare switching to the case of Single and Double b Adjacent translation circuitry, switching for a spare bubble plane, and a translator unit with a spare.

The circuitry for all cases had to perform three functions, as described earlier; (a) connection and switching at the direct bubble memory interface; (b) buffering, translation, correction and checking as applicable to the data; (c) connecting switching at the internal bus interface. For good reliability design, the circuits in (a) were designed as previously described so that their failure rate could be added to the bubble failure rate, i.e. there was no hard core switching circuitry. The circuits in (b) were designed to be self-testing and self-checking as described earlier. The circuits in (c) were parts of the subunit hard core, e.g. no spare lines were assumed on the internal bus and so the subsystem reliability consisted of the product of the reliability of the circuits in the bus connection with the reliability of the rest. If this were unacceptable from a system reliability standpoint the bus could have spares and the bus connection could be redesigned. This is outside the scope of this study.

The cases, and the sets of circuits for each case will now be enumerated. A fan-in of two for NOR circuits with DOT-ORing was assumed. An exclusive-OR tree with n inputs will use 3n-4 gates. An RCCO tree of m input line pairs will use 4m-2 gates. A register stage (Set/Reset Flip-Flop) will count as 4 gates, with control gates added as needed.

Case 1 (R641)* 64 Bit wide data buffer. No checking. No spare planes or buffers.

	Circuits
Bus Connection	128
Buffer	778
Memory Connection	128

Case 2 (R52). 17 bits per bubble plane (16 data and 1 parity). 4 bubble planes/word, one spare plane per 4 plane group and 16 such groups. Two buffers with parity checking (one spare)

	Circuits
Bus Connections	276
Buffer and Checking	1610
Memory Connection	616

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* The term in parentheses identifies the corresponding reliability expression used in section 3B2, "Reliability Analysis."

Case 3 (R721). 1 bit per bubble plane, 72 planes per SEC/DED translator, 1 translator

	Circuits
Bus Connection	144
Translator	2620
Memory Connection	136

Case 4 (R722). 1 bit per bubble plane, 72 planes per SEC/DED translator, 2 translators (1 spare)

	Circuits
Bus Connection	292
Translator	2764
Memory Connection	418

Case 5 (R731). 1 bit per bubble plane, 72 planes per SEC/DED translator, 73 planes (1 spare) in all, 1 translator

	Circuits
Bus Connection	144
Translator	2764
Memory Connection	419

Case 6 (R732). 1 bit per bubble plane, 72 planes per SEC/DEC translator, 73 planes (1 spare) in all, 2 translators (1 spare)

	Circuits
Bus Connection	292
Translator	2768
Memory Connection	629

Case 7 (R61). 16 bits per bubble plane, 6 planes per BSM Error Correcting translator, 16 groups of planes, 1 translator

	Circuitry
Bus Connection	144
Translator	6922
Memory Connection	160

Case 8 (R62). 16 bits per bubble plane, 6 planes per BSM Error Correcting translator, 16 groups of planes, 2 translators (1 spare)

	Circuitry
Bus Connection	292
Translator	7018
Memory Connection	320

Case 9 (R71). 16 bits per bubble plane, 6 planes per BSM Error Correcting translator, 7 planes for group (1 spare), 16 groups of planes, 1 translator

	Circuitry
Bus Connections	144
Translator	7018
Memory Connection	302

Case 10 (R72). 16 bits per bubble plane, 6 planes per BSM Error Correcting translator, 7 planes per group (1 spare), 16 groups of planes, 2 translators (1 spare)

	Circuitry
Bus Connection	292
Translator	7065
Memory Connection	470

3A5 SPECIFIC SYSTEM DESIGNS

There are several ways in which the Mass Storage Unit (MSU) can be organized using the chip, module, and page designs of Sec. 3A2 and the electrical and mechanical design approaches of Sec. 3A3, and each organization allows a number of variations on the basic theme. A memory word can be stored entirely on one chip, with each bit stored in the same shift register, or the bits can each be allocated to a different shift register. A word could be stored entirely on one 16-chip module (plane), with one or several bits per chip. Alternately, a word could occupy one page (6 to 8 modules), with one bit per chip. And finally, the stored word could be spread through the entire memory, with one bit on each module (plane). The details and some general advantages and disadvantages of each organization are discussed in the next three sections, although numerical comparisons are deferred to Section 3B3 so that the reliability calculations of Section 3B2 may be included in the comparison.

3A5.1 Word-per-Chip Organizations

Perhaps the simplest possible memory organization would be to store at least one word (or several words) in each of the closed-loop shift registers of the chip of Figs. 3A2.1 and 3A2.2. If power were to be supplied only to the coils of the module containing the addressed shift register, then each chip would need eleven decode lines, since each module contains $128 \times 16 = 2^{11}$ registers. If all modules are powered, 17 decode lines are needed, since there are 2^{17} registers in the entire memory. Since only one shift register in the entire memory is being addressed at any one time, each chip would need only one sense preamplifier, and the entire memory could function with only one sense amplifier and one write generator, since information would be read-out and written-in bit-serially. Power consumption and parts count would be low. Furthermore, it should be possible to use the serial logic capabilities of bubble domains [S71, P69] to perform error detection and correction right on the chip, before the stored information is sensed. The advantage would be that an "exclusive-or" gate, a basic element of error correction circuits, can be achieved with far fewer bubble devices than transistors.

Against these attractive features are arrayed two major disadvantages: the system would be slow and unreliable. Slow because the data rate (in bits per sec) would be equal to the in-plane field's rotational frequency (in Hz), which is being kept low to conserve power (Sec. 3A2 and Appendix B). In the present case, the data rate would be 10^5 bits/sec, and even if power considerations were thrown to the wind, and the memory were run as fast as allowed by materials and engineering limitations, it is unlikely that the data rate could be increased much beyond 10^6 bits/sec. This is a consequence of the bit-serial operation.

The reliability problem comes about as follows. First, a basic ground rule is assumed: no 10^8-bit memory can achieve the type of reliability (~ 99%/2 mo.) required for this application without some sort of error-correction scheme. This is amply borne out by the calculations of Sec. 3B2. Even if the bubble domain devices themselves are assumed to be perfect (zero failure rate), the failure rates of the electronics necessary to operate the memory are high enough to prevent adequate reliability.

Most error correcting codes are better suited to bit-organized than to word-organized systems. The widely-used Hamming-type SEC/DED* codes [P61], for example, can correct any single-bit error in a memory word, but can only produce an error message in case of a double or higher-order bit error. Such codes, therefore, are most effective in systems organized so that as many failure mechanisms as possible cause only single-bit errors. This is clearly not the case here, since a single defect in one cell of one shift register (such as a defective T-bar) can cause error in all the bits of one word and therefore complete loss of the information of that word. So the word-per-shift register may be an attractive design for a small, low-cost, low-power, low-performance memory, but is not applicable to the 10^8-bit MSU being designed here.

Can the word-per-chip approach be made competitive by eliminating the bit-serial operating feature? The word would be stored with each bit in a different shift register, which would be written into and read out in parallel. This bit-parallel operation increases the data rate by a factor equal to the number of data bits per word. For 64 data bits, the data rate for 100 KHz rotation is 6.4×10^6 bits/sec. Eleven decode lines per chip would be required, since groups of 64 shift registers are being selected simultaneously, and there are 2^{11} such groups. On-chip bubble-domain error correction is still possible.

Unfortunately, this approach exchanges one serious problem for another. The bit-parallel word-per-chip organization would require at least 2(64) + 2(11) = 150 connections per chip, which is impractical. In addition, the reliability is still not satisfactory. The memory is vulnerable to failures down to the chip level, for example, one control line opening up on one chip will affect every bit of the words stored on that chip, resulting in the loss of that information.

It is concluded that word-per-chip organizations are not appropriate for high-reliability 10^8-bit memories.

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*Single-Error-Correction/Dougle-Error-Detection.

3A5.2 Bit-Per-Module (Plane) Organizations

Faced with the conclusions of the last section, one might take the opposite tack and proceed to design a system in which the largest number of the possible malfunctions fall into a category causing only a single-bit error, which can then be corrected using a Hamming-type SEC/DED error correcting code. The bit-per-module (plane) organization of Fig. 3A5-1 fits this description, since all malfunctions up to and including failure of one of the driving coils supplying the rotating field will affect only one bit of the memory word.

As shown in Fig. 3A5-1, one data bit of a memory word is stored on each of 64 modules (or planes) of the type shown in Fig. 3A2-3 or 3A3-10. Eight additional modules store the eight check-bits necessary for the SEC/DED coding in this case. Write-in and read-out are both bit-parallel, requiring 72 write drivers and 72 sense amplifiers. Since one shift register per module is being selected, 11 decode lines per chip are required. Since there are eight modules in one bias-field-supplying sub-assembly or page (Fig. 3A2-5), nine such sub-assemblies (Fig. 3A3-8) are needed to make up the 10^8-bit MSU (Fig. 3A3-7). The six possible variations treated in Sections 3A4 and 3B2 may depart slightly from Fig. 3A5-1 in some details, depending on how redundancy and error correction are implemented.

This approach yielded a quite competitive design, as discussed in more detail in Sections 3B1 and 3B3. Its main initial drawback was that it consumed more power (58 watts) than desired (Sec. 3A3). This results from the fact that rotating field power is supplied to all of the modules all of the time. However, it was not until after the reliability calculations of Sec. 3B2 that this design was eliminated in favor of the recommended bit-per-chip design described in the next section.

3A5.3 Bit-Per-Chip Organizations

The design pholosophy leading to the final, recommended, bit-per-chip system was as follows: the bit-per-plane approach offers random access (delay = 11 rotational periods = 110 μ sec) to a block of 800 words of 64 data bits each, and serial access (4 ms average) to a specific word within that block. The power is high because all of the bubbles are being moved all the time. Since only 72 shift registers (representing .05% of the total memory capacity) are being accessed at any one time, it must surely be possible to achieve the same operating characteristics at reduced power by supplying the rotating field to only a fraction of the memory at a time. A particularly convenient fraction is the 8-module self-sufficient page sub-assembly of Fig. 3A3-8. If each bit of a word is stored on a different chip of the page, then four modules will contain the 64 data bits of a word.

The problem with this approach is that since a module now contains 16 bits on its 16 chips, any malfunction on the module which affects

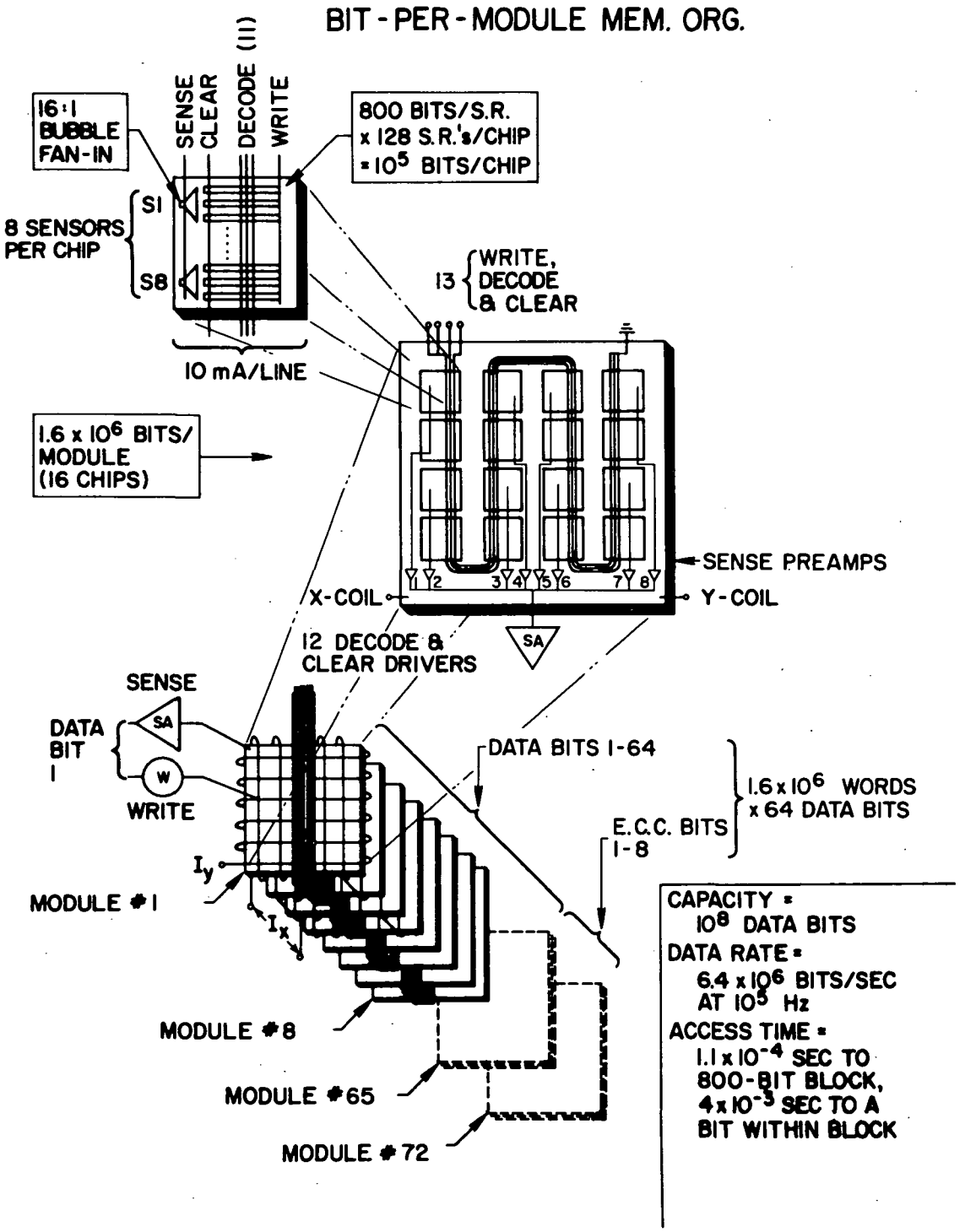

Fig. 3A5-1 Bit-Per-Module (Plane) Memory Organization

more than one chip (such as a rotating-field drive-coil failure) can no longer be corrected by a SEC/DED code as it was in the bit-per-module organization. However, the ability to withstand module-level malfunctions can be restored by using the 16-bit-adjacent-group (SbEC/DbED) error correcting code desscribed in Sec. 3A4. This code can be used to correct up to 16 simultaneously-occuring bit errors in the group corresponding to a module, and if the error condition persists beyond a certain prespecified length of time, a spare 16-bit module can be switched in. The memory can thus perform permanent repairs to itself.* For 64 data bits, implementation of this code requires 32 check bits, and so the page sub-assembly of Fig. 3A3-8 can hold 10^5 words with 64 data bits on four modules, 32 checkbits on two modules, and up to two spare switchable groups of 16 bits each on the remaining two modules.

The schematic organization corresponding to this bit-per-chip system is shown in Fig. 3A5-2. For clarity, the module is shown to have sixteen preamplifiers and sixteen write inputs, one for each chip; in actuality, the four-way multiplexing "tetrad" approach described in Sec. 3A2 divides these numbers by four, and results in a module with only 50 connections (Table 3A2-1 and Fig. 3A2-4). The decode lines must select one of the chip's 128 registers, hence seven lines are required ($2^7 = 128$). Since each page now contains 10^5 words of 64 data bits each, sixteen such sub-assemblies (Fig. 3A3-8) are required to make up the 10^8-bit MSU (Fig. 3A3-7) (16×10^5 words x 64 data bits $\approx 10^8$ data bits). Again, there may be minor deviations from Fig. 3A5-2, depending on the degree of redundancy (number of spare modules) required, etc.

The bit-per-chip approach thus offers a reduction in power (1/9 the coil power of the bit-per-module system) at the expense of increased weight and volume (16 pages vs. 9). In addition, the calculations of Sec. 3B2 will show that the reliability is better than the bit-per-module system of the last section, due to the more powerful error correction code. The tradeoffs made possible by these results are discussed in more detail in Sec. 3B3.

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*This feature can be achieved in the bit-per-module system as well.

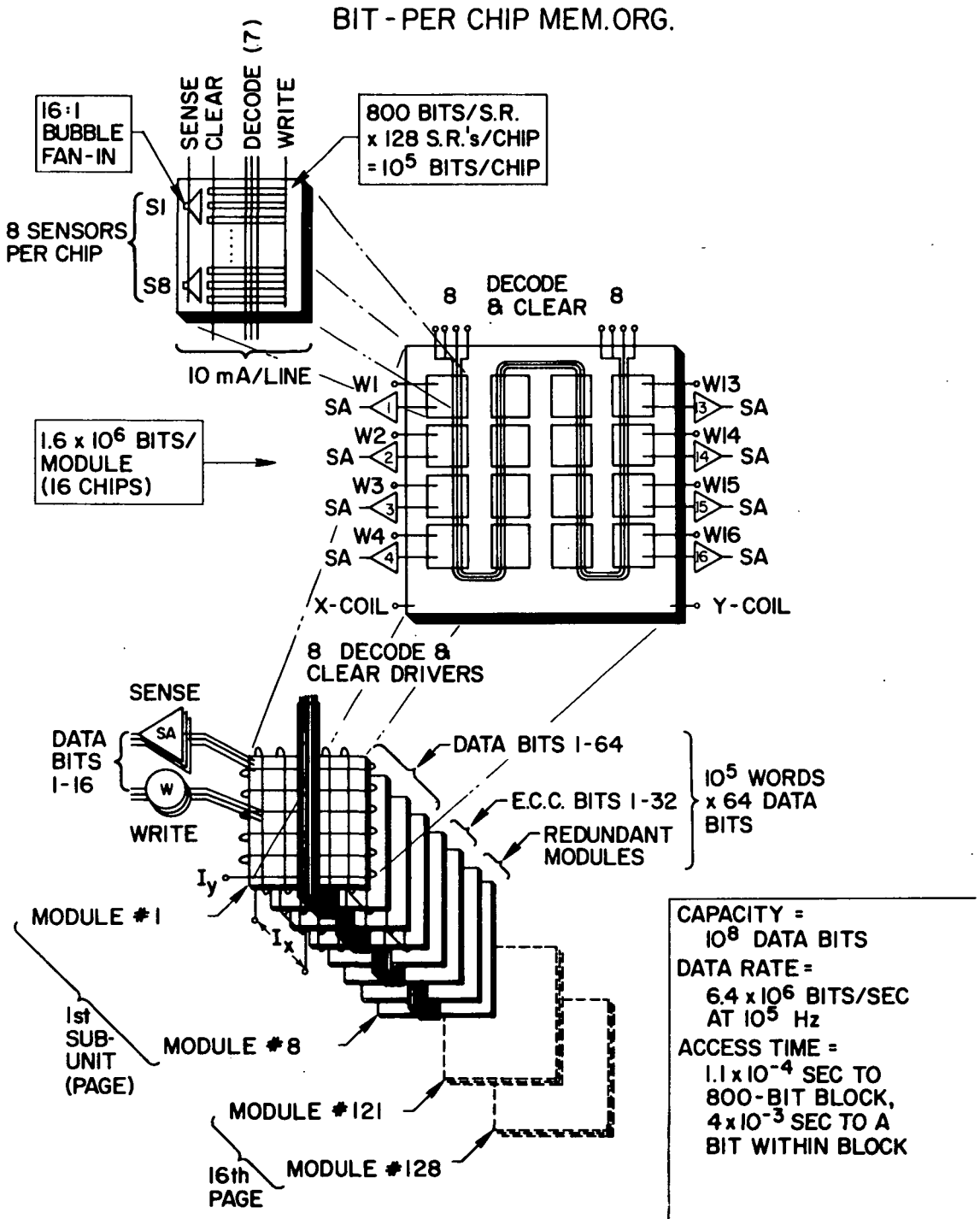

Fig. 3A5-2 Bit-Per-Chip-Memory Organization

3B1 - CALCULATED CHARACTERISTICS OF THE MASS STORAGE UNIT

The shape of the 10^8-bit Mass Storage Unit has been fairly well defined by the various design considerations discussed in detail in the last five sections. The purpose of this section is to review and enumerate the end results of those analyses and to put them into a compact and usable form, showing the remaining design choices and the memory characteristics that would result from each. This is followed in Section 3B2 by reliability analyses of the systems corresponding to these design choices, and in Section 3B3 by a discussion of the various tradeoffs (involving reliability, weight, power, etc.) which can be made within the family of designs. After that, the reasons for recommending the bit-per-chip approach are given.

The family of designs emerging from the discussions of Sections 3A1-3A5 is summarized in Table 3B1-1. It can be seen that the bit-per-chip approach appears to give a more elaborate system than the bit-per-module in terms of weight, volume, and total interconnections. The main advantage of the bit-per-chip approach apparent in Table 3B1-1 is a substantially lower power requirement (22.2 watts vs. 58.3 watts for the bit-per-module). However, in the next section (3B2), it is shown that this bit-per-chip system is also more reliable, a very important factor in the tradeoffs to be discussed in Section 3B3.

TABLE 3B1-1

Characteristics of the Conceptual Design

Chip Design

Minimum Linewidth: .0001" (~2.5 μm)
Bubble diameter: ∿.00015" (~4 μm)
Mobility required for 100 KHz: 100-200 cm/Oe-sec
Example of suitable bubble material: $Eu_{0.7}\ Y_{2.3}\ Fe_{3.8}\ Ga_{1.2}\ O_{12}$ epitaxial film
Overlay: Evaporated Permally for magnetoresistive sensors
Electroplated Permalloy for propagation patterns
Electroplated Copper or Gold for switch control lines
Integral with Garnet film
Chip Size: 0.19" x 0.24" (4.9 mm x 6.1 mm)
Chip Capacity: 10^5 bits (2.5×10^6 bits/sq. inch)
Chip Organization: 128 shift registers, 800 bits each
Access to shift registers: random (bubble domain on-chip decoders).
Rotating field required: 10 Oe (800 A/m)
Bias field required: ~100 Oe
Control current required: 10 mA

	Bit per chip	Bit per module
Connections per chip	20	28
Power dissipation on a chip (mW)	4.5	1.6
Storage Area (%)	89	86.3
Decoder Area (%)	4.6	7.2
Fan-In Area (%)	6.4	6.5

Module Design

Module Size: 6.5 cm x 6.5 cm (2.6" x 2.6")
Module Capacity: 1.6×10^6 bits (16 chips)
Module Coils: Each 360 turns of .005" diam. wire
Rotating Field: 100 KHz, 10 Oe (supplied by 100 mA/coil)
Coil impedance at 100 KHz: (52 + j 58) ohms

Table 3B1-1 (continued)

Module Design (continued)

	Bit per chip	Bit per module
Connections per module	50	56
Power dissipation per module (W) (16x chips + coils)	0.59	0.55

Page Subassembly Design

Size: 16.5 cm x 16.5 cm x 1 cm (6.5" x 6.5" x 0.4")
Weight: 422 g (0.93 lb)
Capacity: 1.28×10^7 bits (8 modules)
Permalloy sheet thickness: 0.5 mm
Permanent magnets: 18, each 6.2 mm diam., 2 mm high
Bias field supplied: 100 Oe

	Bit per chip	Bit per module
Connections per page	123	68
Power dissipation per page (W)	4.72	4.40

Memory Design

	Bit per chip	Bit per module
# of pages	16	9
Size	7.25" x 8" x 9" (0.3 ft^3)	7.25" x 8" x 6.25" (0.21 ft^3)
Weight	27.4 lbs	16.8 lbs
Power (Read):		
Magnetics	4.7 watts	39.6 watts
Circuits	17.5 watts	18.7 watts
Total	22.2 watts	58.3 watts
Capacity		
Info. Bits	1.024×10^8	1.024×10^8
Check Bits	5.12×10^7	1.28×10^7
Data Rate	6.4×10^6 bits/sec	6.4×10^6 bits/sec
Av. Access Time	4 mS	4 mS

3B2 RELIABILITY MODELING

Throughout the progress of this research concurrent reliability modeling was undertaken to help guide the evolving organizations and then to determine trade-offs between the reliability and other parameters.

3B2.1 Reliability and Power Consumption

Among the most important facts to consider in designing a mass store memory for space applications are the reliability and the power consumption. To explore the range of possibilities two designs were laid out, the bit-per-chip design and the bit-per-plane one. This section deals with the predicted reliabilities of a number of systems designed around each basic organization.

3B2.2 Failure Distribution

A Poisson failure distribution was assumed for all failure modes, first because this distribution is mathematically tractable, and second because nothing convincingly better is available.

3B2.3 Failure Rates

For the 1972-1975 time period the following assumed failure rates seem reasonable [BH 68, GJPB 70, W 70].

Discrete transistor	-	5×10^{-9}/hour
Integrated transistor	-	1×10^{-9}/hour
Pulse transformer	-	6×10^{-8}/hour

The determination of what failure rate to use for a cell in a bubble shift register presents a problem because no measurements are available with any statistical validity. Core failure rates of 1×10^{-11} are perhaps a rough guide since both are magnetic phenomena, but it was finally decided to make a parameter study with 3 values for the cell failure rates; 5×10^{-13}, 5×10^{-12} and 5×10^{-11}. This brackets the core failure rate and the smallest one of 5×10^{-13} was chosen so that the magnetics contributed half of the failures in a simplex organization.

The bubble generators, splitters, and annihilators are more complex than a shift register cell, so a ten times larger failure rate was assumed for them. The failure rate of the solder balls is so small that such failures are ignored [T 71]. Also, preliminary electromigration studies in permalloy indicate that the failure rate of the sensors themselves due to this phenomenon will be negligible [DR 71].

3B2.4 Failure Modes and Associated Errors

The next step in deriving a reliability equation is to examine all the possible failure modes and determine the consequences. The following tables give the magnitude of the effect and the errors caused by each failure.

Magnetics

Failure Rate Ratio	Failing Element	Number
1	cell	128 x 800/chip
10	generator	128/chip
10	splitter	128/chip
10	annihilator	256/chip
128	fan-in	8/chip

All these affect a shift register and can cause therein a signal error.

Chip Electronics (chip design)

Failure Equivalent	Failing Element	Number
1 discrete transistor	preamplifier	1/tetrad (4 chips)
20 integrated transistor	sense amplifier	1/tetrad
1 discrete transistor	write loop	1/tetrad

All these affect the four chips in the tetrad (See Sec. 3A1). Only the preamplifier affects the chips in the plane organization.

Planar Electronics (chip design)

Failure Equivalent	Failing Element	Number
1 Discrete transistor	(Clear &	8/plane
1 transformer	Decoder Loops)	8/plane
3 Discrete transistor	Field	2/plane
1 transformer	Coils	2/plane

Planar Electronics (plane design)

Failure Equivalent	Failing Element	Number
1 Discrete transistor	Write Loop	1/plane
20 Integrated transistors	Sense Amplifier	1/plane
1 Discrete transistor	(Clear &	12/plane
1 transformer	Decode Loops)	12/plane
3 Discrete transistors	Field	2/plane
1 transformer	Coils	2/plane

In the above tables, the magnetics affects only single shift registers, the Chip Electronics affects only the contents of a chip, and the Planar Electronics can affect the signals emanating from a whole plane.

3B2.5 Reliability Equations

Before equations for reliability can be formulated information in addition to that in the previous sections must be known. The complete organization must be known, the extent and type of error detection and/or correction must be known, and in the organizations involving standby spares the replacement strategy (or algorithm) must be known. In this study it was assumed that perfect detection, correction (if any), and recovery takes place (See Sec. 3A4).

In addition to the mass store proper, three other sources of failure were taken into account. These were the translator (described in Sec. 3A4 or a parity checker where translators are not used), the bus connections, and the memory connections. These are denoted by X, A, and W in the following equations for the reliability R.

$$R_{j,1} = A_{j,1}\, X_{j,1}\, (W_{j,1}\, r_j)^Q$$

$$R_{j,2} = A_{j,2}\, (X_{j,2} + X_{j,2}\, \underline{X}_{j,2})\, (W_{j,2}\, r_j)^Q$$

In these equations the subscript j designates the number of planes in the mass store (or 1/16 the mass store for the chip organization). Q is equal to 16 for the chip organization since 16 of them are needed to attain the same capacity as the plane organization. Q equals 1 for the plane organization. The second subscript on the R's designate the number of translators used. The r_j for j = N and N + 1 will be derived next, for both the chip and the plane organizations.

In the chip organization, 16 bits come from one plane to form one quarter of a data word, 4 planes are required for the data word, and 2 planes for the encoded bits. This encoding corrects any one of $2^{16}-1$ possible error patterns coming from one plane and detects double errors coming from separate planes. r_{N+1} has a spare plane, the seventh, that is switched in when a double error is detected. This replacement is prefaced by a software diagnosis to determine whether that particular error is permanent or transient, and the replacement occurs only in the latter case.

The equation for one chip store consisting of 6 planes (or 7 with a spare) is next derived.

Define the following:

N = 6 - the number of planes

M = 16 - the number of chips/plane

L = 128 - the number of shift registers/chip

O = 800 - the number of cells/shift register

Let

$\lambda_b = \lambda_p + M \lambda_c$ - the failure rate/block

$\lambda_s = \lambda_{cell} \times M \times O$ = the failure rate/M shift registers where λ_{cell} is the failure rate per cell, λ_c is the summed failure rate per chip, and λ_p is the summed failure rate per plane.

Then define, for mission time T,

$$B = e^{-\lambda_b T}, \quad \underline{B} = 1 - B$$

$$S = e^{-\lambda_s T}, \quad \underline{S} = 1 - S$$

Errors caused by any single failure composing λ_b can be corrected by the encoding, but any two distinct error may only be detected. On the other hand a multiplicity of failures in shift registers can often occur without causing a double error, one in each of two different planes.

$$r_N = B^N \left[S^{LN} + \binom{LN}{1} S^{LN-1} \underline{S} H_1 + \binom{LN}{2} S^{LN-2} \underline{S}^2 H_2 + \ldots + \binom{LN}{j} S^{LN-j} \underline{S}^j H_j + \ldots \right] + N B^{N-1} \underline{B} S^{L(N-1)} \quad \text{Eq. 3B2.1}$$

where H_j is the survival probability when j failures occur in shift registers. Consider the case when no failures occur in a clock, the probability of this happening is B^N, hence that factor in the first term. Then if no errors occur in the shift registers, the probability of survival is S^{LN}, hence that term within the brackets. Next, suppose one shift register has failed. This can happen $\binom{LN}{1}$ ways with probability $S^{LN-1}\underline{S}$. However, since single errors are corrected, the survival coefficient H_1 for this term is unity.

Next consider the case when $j > 1$ errors have occurred. In such circumstances, there is a probability that the errors occur in the same plane, or else occur at different locations in different planes. In either event the system survives and $H_j > 0$. These survival coefficients were calculated

employing the algorithms listed in Appendix E in the form of an APL program. For the above parameters of L and N the next 12 values following unity are listed here.

0.9934895833	0.9805619982	0.9614356513	0.9364480947
0.906046152	0.8707725877	0.8312498735	0.7881617358
0.7422332557	0.6942103395	0.6448393832	0.5948479126

The Survival Coefficients H_i

The last term in Equation 3B2.1 is the product of the probability of one block failure occurring and all the shift registers in the remaining N - 1 planes surviving.

When one standby spare plane is assumed the reliability becomes

$$r_{N+1} = (B^{N+1} + (N+1)\, B^{N}\underline{B}) \quad [\text{ Previous series }] + \binom{N+1}{2} B^{N-1}\, \underline{B}^{2}\, S^{L(N-1)}$$

For the plane organizations, define

N = 72 - number of planes

M = 16 - chips/plane

L = 128 - shift registers/chip

Let

$$P = e^{-\lambda_p T} \quad \text{and} \quad \underline{P} = 1 - P$$

$$C = e^{-\lambda_c T} \quad \text{and} \quad \underline{C} = 1 - C$$

$$S = e^{-\lambda_s T} \quad \text{and} \quad \underline{S} = 1 - C$$

From considerations similar to the chip organization, for this plane organization, the reliability is

$$r_N = \left[P^N \sum_{i=0}^{E} \binom{MN}{i} C^{MN-1} \underline{C}^i \sum_{j=0}^{i} G_{ij} D_j \right] + NP^{N-1}\underline{P} (CS^L)^{M(N-1)}$$

where

$$D_j = \sum_{k=0}^{E} S^{Lj(N-1)} \binom{L(M-j)N}{k} S^{L(M-j)N-k} \underline{S}^k H_{kj} .$$

Here G_{ij} and H_{kj} are survival coefficients, with G_{io} and H_{oj} equal to unity. D_o is equal to S^{LMN}. E is the number of errors considered in the series. For this study E is 14. A similar equation holds for r_{N+1} .

3B2.6 Parameter Study

In table 3B2.1 reliabilities for 6 organizations are given for three different cell failure rates and seven different mission times. R41 is a four-plane simplex organization. As expected, the reliability decreases rapidly with time. The last column shows the expected improvement by incorporating a spare fifth plane (and also two parity checkers). This is a fictitious organization in which a 17th chip is crammed into each plane for parity detection.

R61 is the basic chip organization of 64 data bits (4 planes) and 32 check bits (2 more planes). R62 has 2 translators which increases the reliability. R71 has only one translator but a spare seventh plane, while R72 has both a spare translator and a spare plane. The APL program for the chip organization parameter study is included in Appendix F.

LCELL = 5E-13 *E*=13 *MONTHS* = 1 3 6 12 18 24 36

R41 ↓	*R61* ↓	*R62* ↓	*R71* ↓	*R72* ↓	*R52* ↓
0.923	0.993	0.996	0.991	0.994	0.992
0.787	0.977	0.986	0.974	0.983	0.976
0.62	0.95	0.967	0.949	0.965	0.948
0.384	0.887	0.917	0.899	0.93	0.884
0.238	0.815	0.855	0.852	0.893	0.811
0.148	0.738	0.784	0.805	0.855	0.733
0.0567	0.58	0.63	0.715	0.776	0.574

LCELL = 5E-12 *E*=13 *MONTHS* = 1 3 6 12 18 24 36

R41 ↓	*R61* ↓	*R62* ↓	*R71* ↓	*R72* ↓	*R52* ↓
6.41E-1	9.91E-1	9.94E-1	9.91E-1	9.94E-1	9.84E-1
2.63E-1	9.63E-1	9.72E-1	9.73E-1	9.82E-1	9.10E-1
6.92E-2	9.01E-1	9.17E-1	9.46E-1	9.62E-1	7.28E-1
4.79E-3	7.33E-1	7.58E-1	8.86E-1	9.16E-1	3.43E-1
3.31E-4	5.54E-1	5.81E-1	8.21E-1	8.60E-1	1.17E-1
2.29E-5	3.96E-1	4.20E-1	7.51E-1	7.97E-1	3.14E-2
1.10E-7	1.81E-1	1.96E-1	6.04E-1	6.55E-1	1.31E-3

LCELL = 5E-11 *E*=13 *MONTHS* = 1 3 6 12

R41 ↓	*R61* ↓	*R62* ↓	*R71* ↓	*R72* ↓	*R52* ↓
1.66E-2	9.71E-1	9.74E-1	9.84E-1	9.87E-1	5.36E-1
4.56E-6	8.27E-1	8.34E-1	9.10E-1	9.18E-1	1.45E-2
2.07E-11	5.53E-1	5.63E-1	7.24E-1	7.36E-1	3.54E-6
4.31E-22	1.67E-1	1.72E-1	3.08E-1	3.18E-1	2.71E-15

Table 3B2.1 Reliabilities for Various Chip Organizations

The most significant conclusion to be drawn from this table is that the reliability of the chip organizations holds up much better than the simplex (R41) or simplex and spare (R52) organizations as the assumed cell failure rate increases to 5×10^{-11} from 5×10^{-13}. This conclusion justifies the design philosophy adopted of employing encoding and a translator to correct single errors and detect double errors in the process of translating to byte-parity representation of the data.

Another point to notice is that R72 holds up better than R62 as either the mission time increases or as the cell failure rate degrades. This is perhaps better shown in table 3B2.2.

Significant aspects of systems reliabilities can often better be shown by choosing a different measure of merit than reliability. One excellent measure is the mission time achieved at a specified (constant) reliability.

Table 3B2.2 gives these times at varying specified reliabilities for the same six organizations of table 3B2.1. One can see then that the R61 system is 5(42.36 ÷ 8.7) to 10(1.36 ÷ .13) times as reliable as the R41 system when LCELL = 5×10^{-13}, and is even better when LCELL is worse.

SYSRELS ARE 0.5 0.6 0.7 0.8 0.85 0.9 0.95 0.99

LCELL = $5E^{-}13$ *E* = 13 *TIMES ARE IN MONTHS*

R41 ↓	*R61* ↓	*R62* ↓	*R71* ↓	*R72* ↓	*R52* ↓
8.7	42.4	46.2	66.9	75.8	41.9
6.41	34.4	38.3	52.1	61.3	34
4.47	26.9	30.6	38.1	47	26.5
2.8	19.2	22.7	24.7	32.4	18.8
2.04	15.2	18.4	18.2	24.7	14.8
1.32	10.9	13.8	11.9	16.8	10.6
0.64	6.01	8.25	5.84	8.6	5.8
0.13	1.36	2.2	1.15	1.74	1.3

LCELL = $5E^{-}12$ *E* = 13 *TIMES ARE IN MONTHS*

R41 ↓	*R61* ↓	*R62* ↓	*R71* ↓	*R72* ↓	*R52* ↓
1.56	19.9	20.9	44.6	48.7	9.35
1.15	16.4	17.3	36.3	40.4	7.86
0.8	13.1	14	28.2	32.3	6.41
0.5	9.75	10.5	19.8	23.7	4.91
0.36	7.98	8.74	15.4	19	4.1
0.24	6.04	6.74	10.6	13.8	3.19
0.11	3.73	4.35	5.53	7.69	2.09
0.02	1.1	1.49	1.13	1.7	0.74

LCELL = $5E^{-}11$ *E* = 13 *TIMES ARE IN MONTHS*

R41 ↓	*R61* ↓	*R62* ↓	*R71* ↓	*R72* ↓	*R52* ↓
0.17	6.62	6.74	9.05	9.23	1.06
0.12	5.47	5.58	7.68	7.86	0.9
0.09	4.39	4.49	6.33	6.51	0.74
0.05	3.3	3.39	4.89	5.07	0.57
0.04	2.73	2.81	4.09	4.27	0.48
0.02	2.11	2.19	3.2	3.37	0.39
0.01	1.38	1.45	2.09	2.25	0.26
0	0.52	0.57	0.71	0.83	0.11

Table 3B2.2 Mission Times for Various Chip Organizations

In Table 3B2.3 are given the reliabilities for many plane organized stores. R641 is a simplex design with 64 planes. It is comparable to R41 but has more external bussing. R662 has one plane for parity and another for a standby spare. It has two parity checkers. The first two digits on R721, R722, R731 and R732 give the number of planes and the last digit gives the number of translators.

Note that R721 is superior to R662 only for long missions when the cell failure rate is large. This emphasizes the fact that an organization and system should be chosen to accomodate a definite mission application.

Table 3B2.4 bears the same relationship to table 3B2.3 as table 3B2.2 does to table 3B2.1.

LCELL = 5E-13 *E*= 14 *MONTHS* = 1 3 6 12 18 24 36

R641	*R721*	*R722*	*R731*	*R732*	*R662*
↓	↓	↓	↓	↓	↓
0.917	0.952	0.954	0.953	0.955	0.994
0.771	0.858	0.862	0.866	0.87	0.964
0.594	0.724	0.731	0.748	0.756	0.89
0.353	0.497	0.506	0.552	0.564	0.699
0.209	0.33	0.339	0.4	0.413	0.513
0.124	0.214	0.222	0.285	0.297	0.361
0.0438	0.0862	0.0909	0.139	0.148	0.165

LCELL = 5E-12 *E*= 14 *MONTHS* = 1 3 6 12 18 24 36

R641	*R721*	*R722*	*R731*	*R732*	*R662*
↓	↓	↓	↓	↓	↓
6.36E-1	6.32E-1	6.33E-1	6.32E-1	6.33E-1	9.16E-1
2.57E-1	2.52E-1	2.53E-1	2.54E-1	2.55E-1	5.89E-1
6.63E-2	6.54E-2	6.60E-2	6.81E-2	6.88E-2	2.31E-1
4.39E-3	8.36E-3	8.52E-3	1.15E-2	1.17E-2	2.49E-2
2.91E-4	4.49E-3	4.61E-3	8.32E-3	8.58E-3	2.19E-3
1.93E-5	3.19E-3	3.30E-3	6.93E-3	7.21E-3	1.76E-4
8.48E-8	8.35E-4	8.80E-4	2.30E-3	2.44E-3	9.90E-7

LCELL = 5E-11 *E*= 14 *MONTHS* = 1 3 6 12

R641	*R721*	*R722*	*R731*	*R732*	*R662*
↓	↓	↓	↓	↓	↓
1.65E-2	1.11E-2	1.11E-2	1.11E-2	1.11E-2	7.68E-2
4.46E-6	7.81E-4	7.85E-4	8.97E-4	9.02E-4	4.48E-5
1.99E-11	7.25E-6	7.32E-6	9.42E-6	9.52E-6	2.89E-10
3.95E-22	1.47E-13	1.50E-13	2.35E-13	2.40E-13	6.43E-21

Table 3B2.3 Reliabilities for Various Plane Organizations

SYSRELS ARE 0.5 0.6 0.7 0.8 0.85 0.9 0.95 0.99

LCELL = $5E^{-}13$ *E* = 14 *TIMES ARE IN MONTHS*

R641 ↓	*R721* ↓	*R722* ↓	*R731* ↓	*R732* ↓	*R662* ↓
7.98	11.9	12.2	13.9	14.3	18.4
5.88	9.07	9.3	10.4	10.7	15.1
4.11	6.56	6.74	7.33	7.6	12
2.57	4.26	4.38	4.62	4.79	8.91
1.87	3.17	3.26	3.37	3.5	7.33
1.21	2.1	2.16	2.19	2.27	5.64
0.59	1.05	1.08	1.07	1.11	3.67
0.11	0.21	0.22	0.21	0.22	1.37

LCELL = $5E^{-}12$ *E* = 14 *TIMES ARE IN MONTHS*

R641 ↓	*R721* ↓	*R722* ↓	*R731* ↓	*R732* ↓	*R662* ↓
1.53	1.51	1.51	1.51	1.52	3.58
1.13	1.11	1.11	1.11	1.12	2.93
0.79	0.78	0.78	0.78	0.78	2.33
0.49	0.48	0.49	0.49	0.49	1.74
0.36	0.35	0.35	0.35	0.35	1.44
0.23	0.23	0.23	0.23	0.23	1.11
0.11	0.11	0.11	0.11	0.11	0.73
0.02	0.02	0.02	0.02	0.02	0.28

LCELL = $5E^{-}11$ *E* = 14 *TIMES ARE IN MONTHS*

R641 ↓	*R721* ↓	*R722* ↓	*R731* ↓	*R732* ↓	*R662* ↓
0.17	0.15	0.15	0.15	0.15	0.39
0.12	0.11	0.11	0.11	0.11	0.32
0.09	0.08	0.08	0.08	0.08	0.26
0.05	0.05	0.05	0.05	0.05	0.19
0.04	0.03	0.03	0.03	0.03	0.16
0.02	0.02	0.02	0.02	0.02	0.12
0.01	0.01	0.01	0.01	0.01	0.08
0	0	0	0	0	0.03

Table 3B2.4 Mission Times for Various Plane Organizations

A comparison of the results of the reliability calculations in these four tables yields the following conclusion. The bit-per-chip design is superior to the bit-per-plane one and also suffers the least deterioration in reliability when the cell failure rates are larger.

At one point in the design process an impedance mismatch occurred which was solvable by having 4 field coils operate in series, and similarly with several clear and decoder loops. However, it was recognized that a driver failure could then cause a double or quadruple group error to occur and so rather than resorting to this series hook-up, the mismatch was overcome by employing pulse transformers. (Other methods of avoiding the series connection are also possible.) Even though the failure rate for such transformers is high, being 12 times that of a discrete transistor, the improvement in system reliability is quite impressive as shown in Tables 3B2.1a and 3B2.2a which give the reliabilities for systems R61, R62, R71, and R72 when the series hook-up is employed. These values are to be compared with those of tables 3B2.1 and 3B2.2. In all cases the use of transformers improves reliability.

LCELL = 5E-13 *E*=13 *MONTHS* = 1 6 18 36

R41	*R61*	*R62*	*R71*	*R72*	*R52*
0.953	0.975	0.978	0.973	0.976	0.993
0.748	0.856	0.871	0.848	0.863	0.953
0.419	0.623	0.654	0.61	0.639	0.85
0.175	0.382	0.415	0.371	0.403	0.684

LCELL = 5E-12 *E*=13 *MONTHS* = 1 6 18 36

R41	*R61*	*R62*	*R71*	*R72*	*R52*
6.61E-1	9.74E-1	9.77E-1	9.73E-1	9.76E-1	9.85E-1
8.35E-2	8.47E-1	8.62E-1	8.46E-1	8.61E-1	7.53E-1
5.82E-4	5.75E-1	6.03E-1	5.95E-1	6.24E-1	1.47E-1
3.39E-7	2.92E-1	3.17E-1	3.37E-1	3.65E-1	2.55E-3

LCELL = 5E-11 *E*=13 *MONTHS* = 1 6 18

R41	*R61*	*R62*	*R71*	*R72*	*R52*
1.71E-2	9.65E-1	9.68E-1	9.66E-1	9.69E-1	5.40E-1
2.50E-11	6.28E-1	6.39E-1	6.49E-1	6.60E-1	4.05E-6
1.57E-32	4.71E-2	4.94E-2	5.30E-2	5.56E-2	2.96E-25

Table 3B2.1a Reliability without Transformers for Various Chip Organizations

SYSRELS ARE 0.8 0.9 0.95 0.99

LCELL = $5E^{-}13$ *E* = 13 *TIMES ARE IN MONTHS*

R41	*R61*	*R62*	*R71*	*R72*	*R52*
↓	↓	↓	↓	↓	↓
4.61	8.59	9.63	8.12	9.05	23.5
2.18	4.07	4.6	3.83	4.29	12.3
1.06	1.99	2.25	1.87	2.1	6.41
0.21	0.39	0.44	0.36	0.41	1.33

LCELL = $5E^{-}12$ *E* = 13 *TIMES ARE IN MONTHS*

R41	*R61*	*R62*	*R71*	*R72*	*R52*
↓	↓	↓	↓	↓	↓
0.54	7.91	8.72	7.95	8.82	5.23
0.25	3.9	4.35	3.79	4.24	3.39
0.12	1.94	2.19	1.86	2.08	2.21
0.02	0.39	0.44	0.36	0.41	0.77

LCELL = $5E^{-}11$ *E* = 13 *TIMES ARE IN MONTHS*

R41	*R61*	*R62*	*R71*	*R72*	*R52*
↓	↓	↓	↓	↓	↓
0.05	3.74	3.87	3.93	4.06	0.58
0.02	2.25	2.35	2.34	2.46	0.39
0.01	1.33	1.41	1.36	1.45	0.27
0	0.34	0.38	0.33	0.37	0.11

Table 3B2.2a Mission Times without Transformers for Various Chip Organizations

3B3 - TRADEOFFS

This section is divided into two halves. The first discusseses tradeoffs possible within the design groundrules and framework presented in detail in Sec. 3A. The second half discusses tradeoffs obtained by changing the groundrules--different chip designs, module arrangements, etc. By necessity because of its nature, this latter half is more preliminary and sketchy, and to a certain extent is an interface with Section 5, Conclusions and Recommendations.

3B3.1 Tradeoffs Within Present Design Groundrules

The comparison of the bit-per-chip system and the bit-per-module system which was begun in Sec. 3B1 can now be completed using the reliability analysis results of Sec. 3B2. Some of these results are presented graphically in Fig. 3B3-1. This figure is extracted from Tables 3B2.1 and 3B2.3, and shows plots of reliability vs. mission time (elapsed operating time) for the most reliable bit-per-chip design (R72), the most reliable bit-per-module (or "plane") design (R662), and a simplex (no error correction) design (R641). The parameter on these curves is the failure rate of the basic bubble shift register cell, as explained in Sec. 3B2. It can be seen that the simplex reliability is very low for all but the lowest failure rate. The Hammming SEC/DED coding of the bit-per-module (plane) organization results in substantial improvement of reliability. However, the 16-bit-adjacent group error detecting/correcting coding (SbEC/DbED) of the bit-per-chip organization results in the highest reliabilities, in spite of the greater complexity and parts count of that system

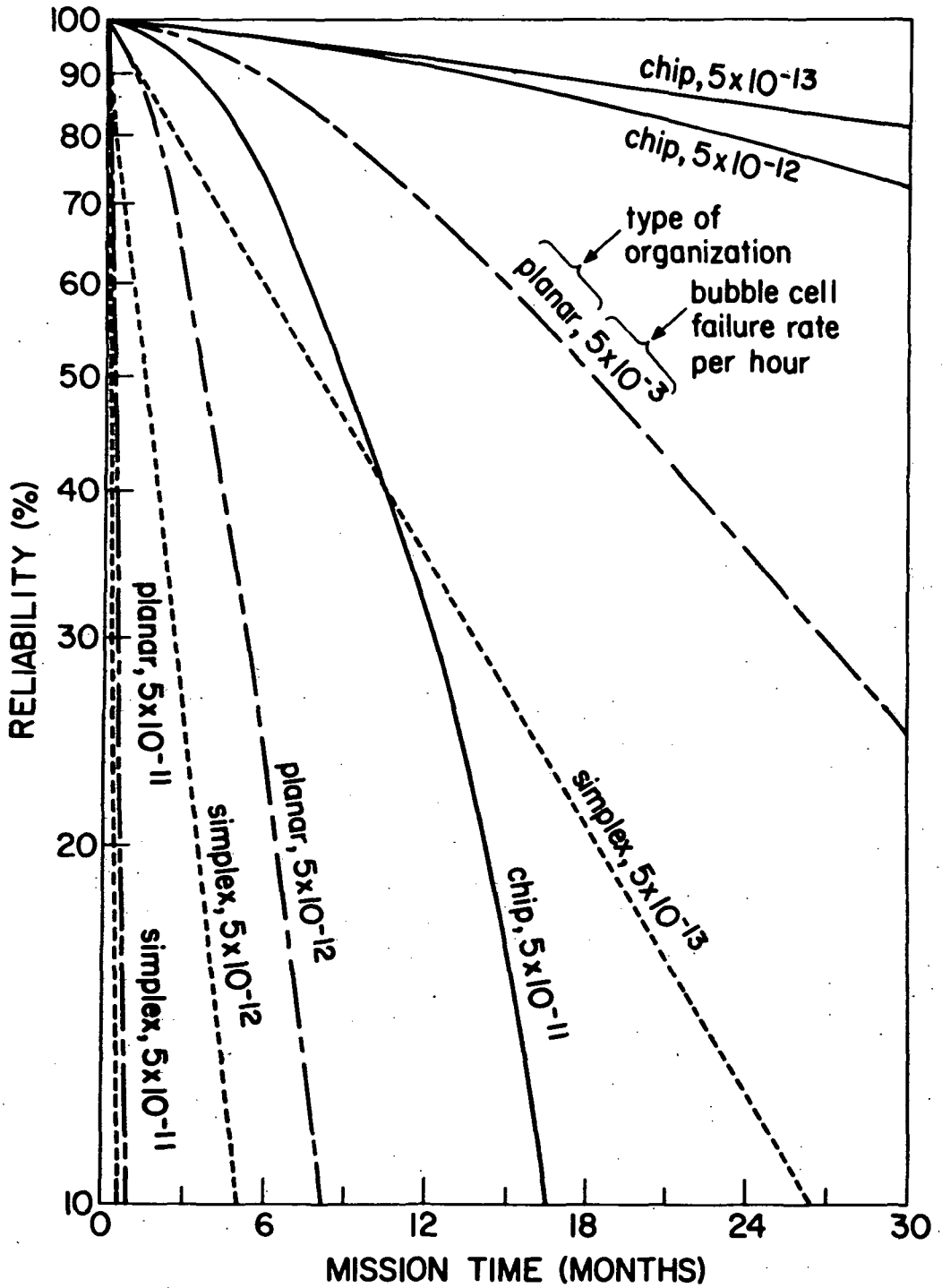

Fig. 3B3-1 Reliability of the Bit-Per-Chip and Bit-Per-Module (Planar) Memory Organizations vs. a Simplex Memory (no error correction). In all cases, bit capacity = 10^8.

The effect of the SbEC/DbED coding is shown perhaps more dramatically in Fig. 3B3-2, which shows that even an intermediate system such as R71 gives better reliabilities for a cell failure rate of 5×10^{-11}/hour than does the simplex organization for a hundred fold lower failure rate, 5×10^{-13}/hour. For comparison, a sort of "ultimate" reliability curve is also shown. This is basically for R72, with the exception that it has been assumed that there are <u>two</u> spare modules (in which case the system should be called R82) and that the translator is implemented using bubble domain "exclusive-or" gates. This has the effect of making the failure rate of the translator itself negligible. The corresponding increase of the 24-month reliability from 85% to 92% is thus a measure of the effect on overall reliability of failures in the translator - a rather small effect, it can be seen.

System reliabilities were also calculated for cell failure rates of 5×10^{-14} to 5×10^{-17} per hour, but the best 24-month reliability is only about 94%, because even for 5×10^{-13} per hour, only half of the memory failures are due to magnetics. The memory reliability becomes limited by the electronics.

An obvious tradeoff, then, is between the lower power and higher reliability of the bit-per-chip system vs. the lower weight, volume, and magnetics parts count of the bit-per-module (plane) system. If the bubble cell failure rate eventually turns out to be close to the 5×10^{-13}/hour value, then the bit-per-plane system may have sufficient reliability for short mission times (for example, $\sim 90\%$ for 3 months) that it may be preferable to the bit-per-chip system for an application where weight and volume rather than power are the most important quantities.

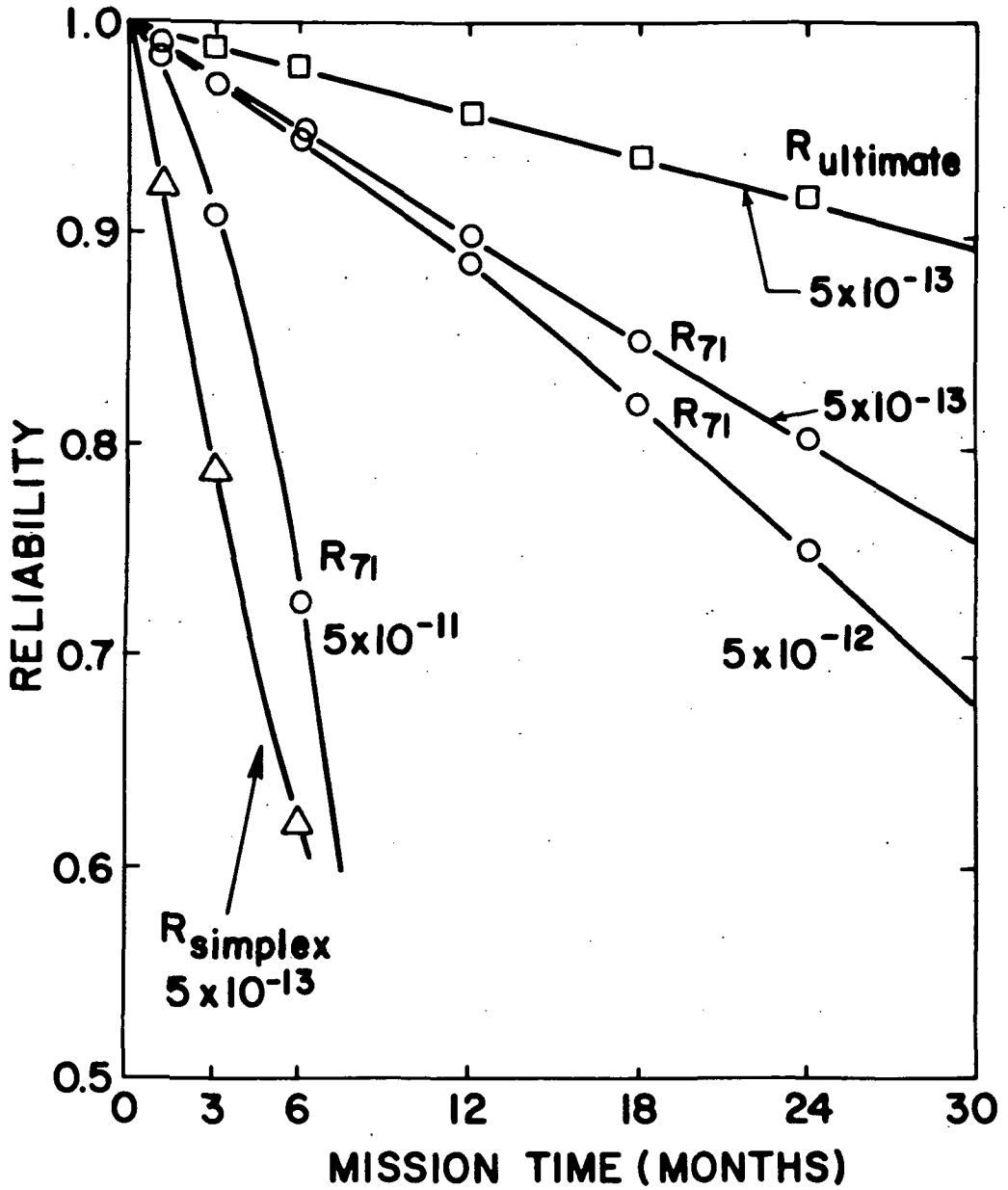

Fig. 3B3-2 Reliability Comparison of Intermediate vs. Ultimate Bit-Per-Chip System

However, in most space applications, power is at more of a premium than weight for the general design ranges being discussed here. Also, if the failure rate of the bubble cell turns out to be considerably greater than 5×10^{-13}/hour, the reliability of the bit-per-module approach plummets more rapidly than that of the bit-per-chip system. It appears, therefore, that the bit-per-chip organization gives the generally preferable system.

The question then remains, "Which bit-per-chip system?" This really depends on the mission--its duration and reliability requirements. If the mission is long and the highest possible reliability is required, then a system such as R82 should be used--two spare modules and two (one spare) translators. If these requirements can be relaxed somewhat, this will be reflected in lower power requirements and parts counts. The equations and data of Sec. 3B2, the computer programs of Appendix E and F, and the parts descriptions of Section 3A3 should provide the tools for these calculations.

3B3.2 Tradeoffs Beyond the Present Design Groundrules

A large number of tradeoffs is possible when one considers deviations from the present memory, page, module, and chip designs.

The memory capacity can be changed without departing very far from the present groundrules by simply stacking up more or less of the page subassemblies. These are self-sufficient 1.3×10^7-bit memories in their own right (except for driving circuits), and so storage units with bit capacity between $\sim 10^7$ and 2 or 3×10^8 can easily be obtained. Power and weight scale accordingly. The self-sufficiency of page sub-assemblies

preserves the basic modularity of the storage unit and results in good reliability and maintainability. In addition, since the page sub-assembly contains its own bias field, the stored information is maintained intact when the page is removed from the memory. Thus extra pages can be kept in shelf-storage and inserted into the MSU when their stored information is needed.

Changes in the memory's data rate and access time can be achieved by changing the frequency of the rotating drive field. For frequencies above 100 KHz, the power dissipation will asymptotically approach a linear function of frequency, unless the drive coils are capacitatively resonated and special drive circuitry is employed. Alternately, the high-frequency power dissipation can be reduced by re-designing the module to lower the coil inductance relative to the coil resistance, as by reducing the clearance space inside the coils. The price would be a more sophisticated manufacturing process.

The data rate and access time track the rotating frequency together. If they are to be varied independently, the memory organization or the chip design must be changed. Access time is varied independently of the data rate by changing the length of the shift registers on the chip. The data rate is varied independently of the access time by changing the number of bits being read out of the memory in parallel, i.e., by changing the number of bits per stored memory word. Power can be saved by reading out less bits in parallel, since the number of sense amplifiers as well as the number of simultaneously powered modules is reduced. However, the ratio of check bits to data bits increases as this is done, and so the power is a less-than-linear function of the number of data bits per word.

The number of modules per page is not a rigidly fixed quantity, and for a smaller memory, it may be desirable to have one module per page. In a large memory, this would cause a significant increase in the total number of interconnections. Likewise, for a small fast memory it may be advantageous to have one chip per module, but again the total number of interconnections in a large memory would be significantly increased by this approach.

The chosen chip size is itself a tradeoff between storage capacity and yield, as is the possibility of using smaller linewidths to obtain higher storage density on the chip. The dimensions used in this report are based on reasonable estimates of chip yields in the mid-1970's, but if the yields turn out differently from those projected in Appendix A, the chip size and linewidth tradeoff will have to be revised.

The redundancy approach used in the tradeoff studies of Section 3B2 was to supply spare modules which could be switched in automatically for a permanently failed module. It is also possible to provide redundant chips on a module, as discussed briefly in Sec. 3B2, or to provide redundant shift registers on a chip, as discussed in the second part of Appendix C. These approaches should be compared from the standpoint of reliability, power, and system complexity.

The tradeoff which is perhaps furthest removed from the present groundrules is a comparison of different chip organizations, i.e., comparing the on-chip decoding approach used here with the assembly-loop chip, coincident-block-access [B71] approach and/or other approaches. The reliability model set up in Sec. 3B2 is capable of providing valuable analytical comparisons. However, this is clearly beyond the scope of the present work.

Further tradeoffs available to the memory designer are described in Section 4B3, the commentary on the experimental results obtained from the feasibility model. Further recommendations for future work are contained in Section 5. The technical description of work done on this project now switches from the conceptual design to the feasibility model.

SECTION 4 FEASIBILITY MODEL

This major section is the second half of the detailed technical description and deals with the feasibility model which was built to test and demonstrate the major operating features of the conceptual 10^8-bit memory design described in Section 3. Again, the design principles are discussed first (Section 4A), covering Overlay Design, Fabrication Procedure, and Operating Instructions. This is followed in Section 4B by an evaluation of the feasibility model, covering Test Equipment and Procedures, Test Results (Data), and Evaluation and Interpretation of Data.

4A1 - FEASIBILITY MODEL DESIGN

A feasibility model of the designed mass storage unit (Sec. 3) was to be fabricated, tested, and delivered for evaluation. The model was to be limited in capacity to that necessary to prove feasibility of the approach used in the conceptual design.

4A1.1 Definition of the Feasibility Model

This section discusses the link between the conceptual design and the feasibility model. The essential features of the conceptual design are summarized in the first part of Table 4A1-1. The design objectives of the feasibility model are listed in the second part of the same table. The similarities and differences of these two entities, the conceptual design and the feasibility model, are as follows:

Chip Functions: The full-scale chip has 128 shift registers storing 800 bits each, for a total capacity of 10^5 bits/chip. The feasibility model's chip has 4 shift registers each storing 16 bits, for a total capacity of 64 bits. Both chips have on-chip magnetic bubble decoding which provides random access to 2^n shift registers with n current-carrying control lines. In addition, the operability of both chips demands that the permalloy overlay, driven by an external rotating magnetic field, perform the following functions:

- bubble generation
- straight-line propagation
- cornering
- joining two paths into one (junction)
- bubble annihilation.

TABLE 4A1-1

SUMMARY OF NASA CONTRACT

Part I: Conceptual Design of 10^8 Bit Mass Storage Unit

- Self-contained bubble domain chips with on-chip decoding.
- 1000 chips, 128 shift registers, 800 bits each.
- 2.5×10^6 bits/in^2 (0.1 mil line technology).
- Epitaxial garnet film bubble material.
- Permalloy magnetoresistive sensors, bridge connection.
- 100 KHz operation for low power.
- Permanent-magnet bias field source.

Part II: Operating Feasibility Model

- Self-contained bubble domain chip with on-chip decooding.
- 1 chip, 4 shift registers, 16 bits each.
- 0.25×10^6 bits/in^2 (0.3 mil line technology).
- Epitaxial garnet film bubble material.
- Permalloy magnetoresistive sensors, bridge connection.
- 10 KHz operation.
- Permanent-magnet bias field source

The main difference between the feasibility model chip and the conceptual design chip (aside from scale) is that the feasibility model has a sensor per shift register and the conceptual design has a sensor per sixteen shift registers. This is done in the conceptual design to reduce the required number of sense preamplifiers and is accomplished by inserting a two-for-one bubble splitter into each shift register (Sec. 3A1). One output of the splitter goes into a 16:1 bubble fan-in circuit which leads to a magnetoresistive sensor. There are eight sensors per chip, which are connected in series to form one of the four legs of a Wheatstone bridge. This bridge connection should provide noise cancellation and a substantial improvement in signal-to-noise ratio.

Bubble splitting is a relatively simple function to accomplish, as has been shown by workers from this laboratory [CFLR 71] as well as others [B71-II]. (As a matter of fact, spurious bubble splitting at unwanted locations was a problem which had to be eliminated in arriving at the overlay design for the present feasibility model.) Sensing, on the other hand, is not a simple problem, especially when working with small bubbles in epitaxial films, which do not allow one to place the sensor and the propagation means on opposite sides of the bubble material, as had been done in previous sensing of larger bubbles in bulk platelets [AKLT 71, S 71].

Since it would not be possible to implement both the splitting scheme and the bridge connection in a four-register chip, it was decided to forego the splitters, incorporate a sensor into each shift

register, and thus obtain important information on both the amplitude of the signal and the degree of noise cancellation which can be obtained with the bridge connection. The alternative approach of incorporating even four 4:1 splitter-fan in circuits and a four-legged bridge would have required a 16-shift register chip, which would have required expenditures of resources, manpower, and time which were considerably beyond the scope of the present contract.

Overlay Technology: In defining the fabrication steps of the overlay which simultaneously provides propagation, control, and sensing of the bubble domains, it was decided to choose a process which was demonstrably capable of making overlays with the .0001" (2.5 μm) linewidths called for by the conceptual design, while at the same time choosing a linewidth for the feasibility model which would result in reasonable yields during the 8-month time-frame of the contract. The combined additive-subtractive metallurgy process described later in this section meets the first requirement, and a line width of .0003" (7.5 μm) meets the second: the problems solved in fabricating such an overlay would push the state of the art ahead, since three-layer overlays (thin permalloy for sensing, thick permalloy for propagation, gold or copper for control and sense lines) had not been reported at the time this contract began. At the same time, the prospects of a model considerably more complex than any previously fabricated being fully operational within 8 months would be considerably better with the wider lines and a storage density of 0.25×10^6 bits/square inch. And since the same process is capable of making both 7.5 μm and 2.5 μm linewidth overlays, the 3X reduction needed to achieve the 2.5×10^6 bits/square inch storage density of the conceptual design should be relatively straightforward.

The yield calculations of appendix A show that overlay defects, not bubble material defects, will limit chip size. The measurements of Sec 4B show that the spacing between the overlay and the bubble material is very critical. Both of these facts imply that the final manufacturing process should be one in which the magnetic overlay is deposited onto a suitable thin spacer layer, which in turn has been deposited onto the epitaxial garnet film. In other words, the manufactured chip should be an integrated structure. The feasibility of this approach in making high-density shift registers has already been demonstrated [AHPSR 71]. For purposes of experiments involving a large number of cut-and-try approaches, however, it is much more convenient to fabricate the overlays on separate glass substrates and to obtain controlled comparisons between them by operating them with the same garnet film. Control of the overlay-garnet spacing in this case requires more care than would be acceptable in a manufacturing environment, but it is not unreasonable by laboratory standards. This, therefore, was the approach adopted here.

Bubble Domain Material: The 4 μm-diameter bubbles required for the conceptual design are clearly practical only in epitaxial films. The 12 μm bubbles of the feasibility model could be obtained both in polished-down bulk platelets and in epitaxial films, and a bulk platelet would have satisfied the contract. However, device operation was found to be better in the epitaxial films (Sec. 3B2, 3B3), and so the final model was delivered with a garnet film (details are given in Sec. 4A2). A slight change in the chemical composition of this film will result in 4 μm bubbles.

Feasibility Model Package: The conceptual design describes a compact package designed to operate at 100 KHz in a bias field supplied by a permanent magnet structure. Some compactness was sacrificed in designing the feasibility model package to allow different overlay designs to be inserted, measured, and extracted rapidly, and so the upper frequency limit is 10 KHz. The permanent bias field feature is incorporated, however, the bias field coils being used only for vernier adjustments, obtaining operating margins, etc.

4A1.2 Layout of the Feasibility Model Overlay

The design chosen for the feasibility model is shown in block-diagram form in Fig. 4A1-1. It consists of four shift registers and all the control functions necessary to write into, read out, and clear any one of the four shift registers. Each shift register has a built-in write decoder and read decoder section. Since the emphasis was on testing the control functions, the storage capacity of each register is small (only 16 bits). The same layout to be described here can provide access to four much longer shift registers, and in a full-scale chip, about 90% of the total area is available for storage (Sec. 3A1).

Methods for generation, propagation, and annihilation of bubbles with a permalloy overlay and a rotating in-plane field have already been described [BFPRV 69, P69]. Magnetoresistive sensors for bubble domains have also been reported [AKLT 71, S71]. The write, clear, read decoder, and write decoder functions make use of a current-controlled switch which is shown in Fig. 4A1-2. This switch allows a small control current to select one of two alternate paths in the permalloy overlay

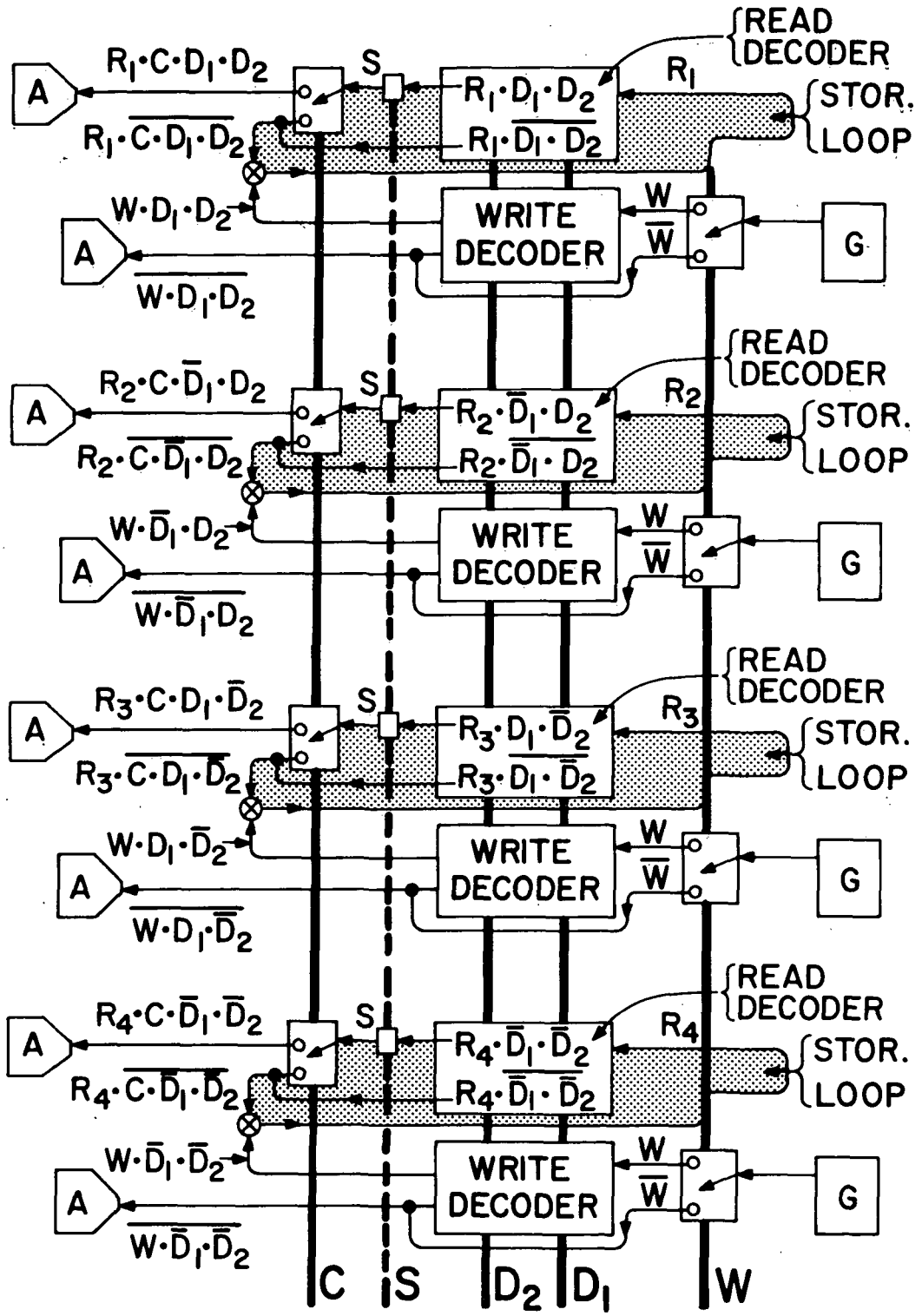

Fig. 4A1-1 Block Diagram of the Memory Chip's Operation. (G--generator, A--annihilator, S--sensor, W--write control line, D_1, D_2--decode control lines, C--clear control line, R_1, R_2, R_3, R_4--information stored in register 1, 2, 3, or 4)

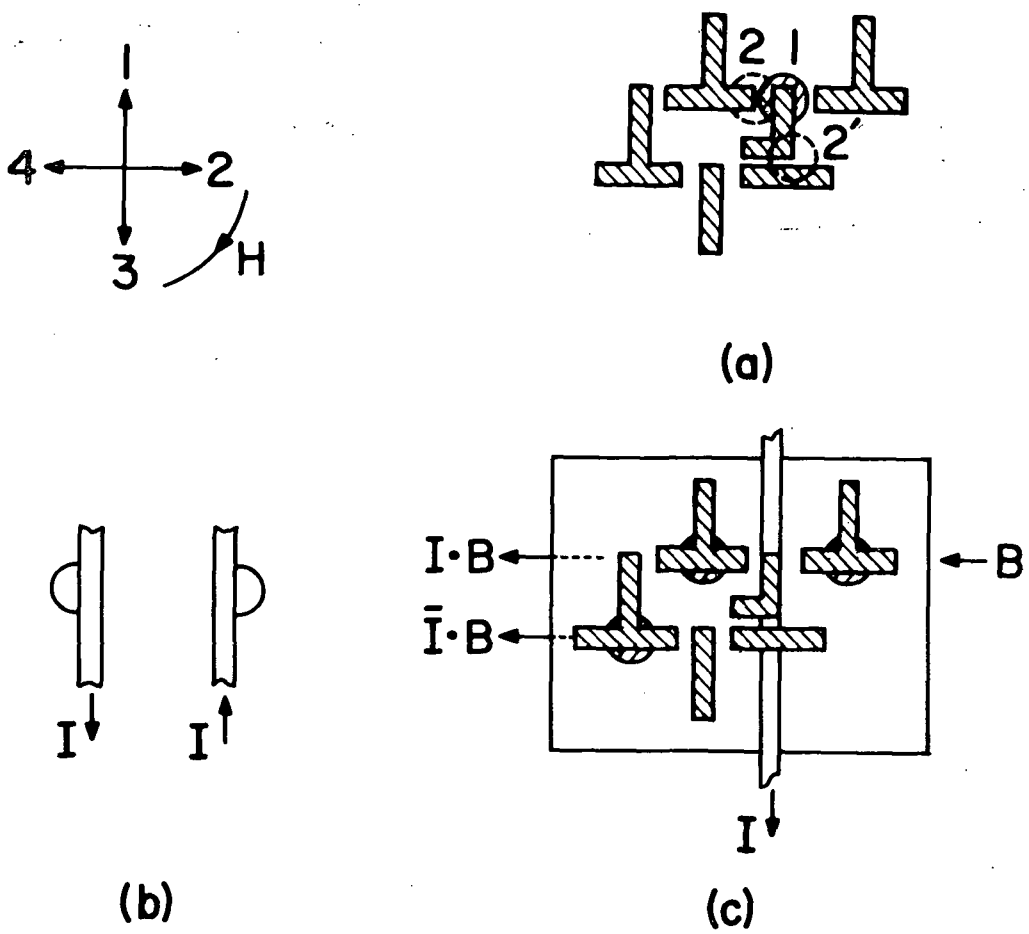

Fig. 4A1-2 The Basic Control Switch. a) In the absence of control current it is uncertain whether the bubble will move from position 1 to 2 or 2'. b) Effect on bubble position of current in a strip-line. c) Combining the permalloy and conductor patterns as shown results in the "single-pole, double throw" switch whose Boolean representation is shown here. (The current is on between field positions 1 and 2.)

for the bubble domain. A bubble B entering the switch from the right will emerge from the upper port if the current I is positive, and from the lower port if I is negative. The complete chip layout is shown in Fig. 4A1-3.

Since logic as well as storage are being accomplished on the chip, it is useful to represent the switch in Boolean algebra. The switch may be viewed as a two-output logic element operating on the two binary inputs B and I. B will be considered 1 when a bubble is present and 0 when a bubble is absent; I will be considered 1 for positive current and 0 for negative current. Then the output at the upper port is the Boolean "And" function $(B \cdot I)$, whereas the other output is $(B \cdot \bar{I})$, where $\bar{I}$ is the binary inverse of I.

The operation of the chip can now be explained in terms of Figs. 4A1-1, 2, and 3. The generators G are all designed to emit a steady stream of bubbles. To write a 1 into one of the 2^n registers, the write control current W is made positive. This allows a bubble to enter each of the 2^n write decoders. In one of these write decoders, the n decode currents will have the right combination to allow the bubble to propagate out the upper port and into the storage loop. In all the other $2^n - 1$ write decoders, the bubble will exit from the lower port and into an annihilator. In Fig. 4A1-3, the third register from the top, $(D_1 \cdot \bar{D}_2)$, is being written into. The simultaneous proceeding in an unselected register are shown in the bottom register $(\bar{D}_1 \cdot \bar{D}_2)$.

When writing is finished, the write switch is turned off (W becomes negative), and as long as the clear control current C is negative, the

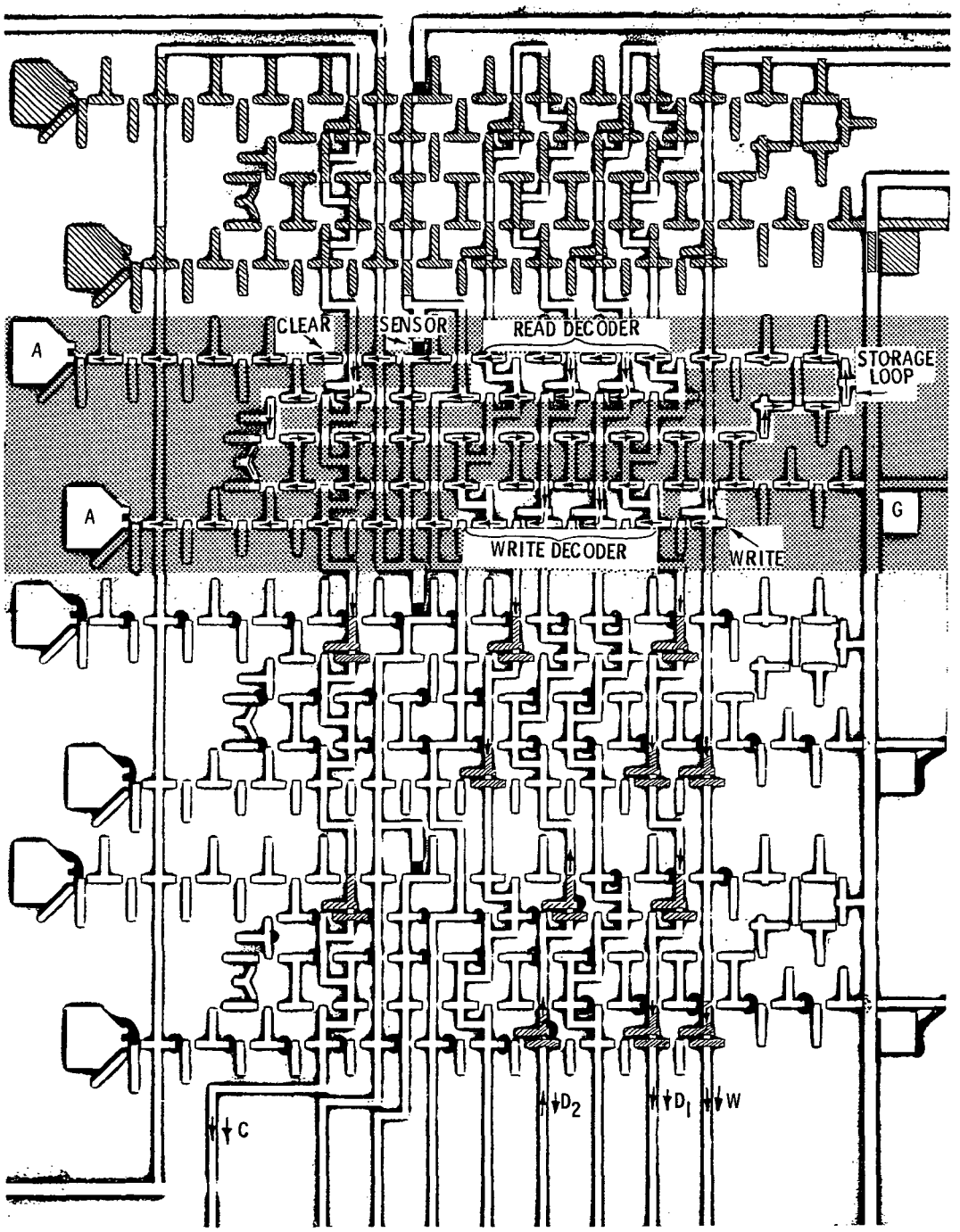

Fig. 4A1-3 Layout of the Chip. In the top register, the permalloy pattern is cross-hatched, the overlapping conductor is clear. In the next shift register down, the essential functions of Fig. 4A1-1 have been highlighted. The actual control currents are shown as arrows on top of the control lines.

information will circulate in the storage loop. Each storage loop contains a read decoder section whose layout is identical to that register's write decoder section. Therefore, the same combination of decode currents which selected a register for write-in also selects it for read-out. In the selected register, the bubble exits at the top port of the read decoder and goes by a magnetoresistive sensor. In all the other registers, the bubble exits at the bottom port and bypasses the sensor.

After passing the sensor, the bubble in the selected shift register enters the clear control switch. For negative clear control current $\bar{C}$, the bubble is returned to the storage loop. However, if new information is to be entered into the register, the clear current is made positive, and the bubbles go to an annihilator. This is shown happening in register $D_1 \cdot \bar{D}_2$, Fig. 4A1-3. Thus, information may be written into, read out of, and cleared out of any one of the 2^n registers by activating n decode lines.

The exact shapes and proportions of the layout of Fig. 4A1-3 were determined to a great extent by trial and error, as will be explained in more detail in Sec. 4B2 and 4B3. Many variations on this layout are possible, including an arbitrary increase in the length and capacity of the storage loop. The main rules to be followed in designing variations of Fig. 4A1-3 are : a) the travel time from the output of the write decoder to the junction point (the point where the output of the write decoder enters the storage loop) must be equal to the travel time from the read decoder output to the same junction point. This is necessary to preserve synchronization in the memory, as discussed in

Sec. 4A3. If this rule is violated, a new timing scheme must be devised.
b) The read decoder delay must be equal to the write decoder delay, for the same reason as a).

The design of the feasibility model chip layout and the theory of its operation have been described above. The next section describes how this layout and theory are brought to reality.

4A2 - FABRICATION PROCEDURE FOR THE FEASIBILITY MODEL

The approximate structure which must be achieved to make the feasibility chip operational is shown in Fig. 4A2-1. This latter figure shows a shows a highly enlarged region of Fig. 4A1-3 in the vicinity of one of the four sensors. A glass substrate supports the overlay of thin permalloy magnetoresistive sensors, thick permalloy T-bars, and copper (or gold) conductor lines necessary for the operation of the memory chip. A single-crystal non-magnetic garnet substrate supports the thin epitaxial magnetic garnet layer which contains the bubble domains. The chip is completed by pressing the two substrates together as shown in Fig. 4A2-1 while maintaining a small spacing between the layer of propagation permalloy and the epitaxial garnet layer.

Fabrication of the overlay will be described first.

4A2.1* Overlay Fabrication

The process for fabrication of the overlay consists of a sequence of metal deposition steps, followed by one subtractive etch which serves to define the sensors and to separate the functional parts of the overlay, which are all electrically and magnetically interconnected during the fabrication cycle. A representative sequence of steps is as follows (see the flow-chart of Fig. 4A2-2):

Step #1: A 200Å thick magnetoresistive film of Ni-Fe (nominally 81% Ni, 19% Fe) is deposited onto a glass substrate (∿.35 mm thick) by evaporation in a dc in-plane magnetic field >30 Oe, at a substrate temperature between

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*This section was prepared with the help of Dr. L. T. Romankiw

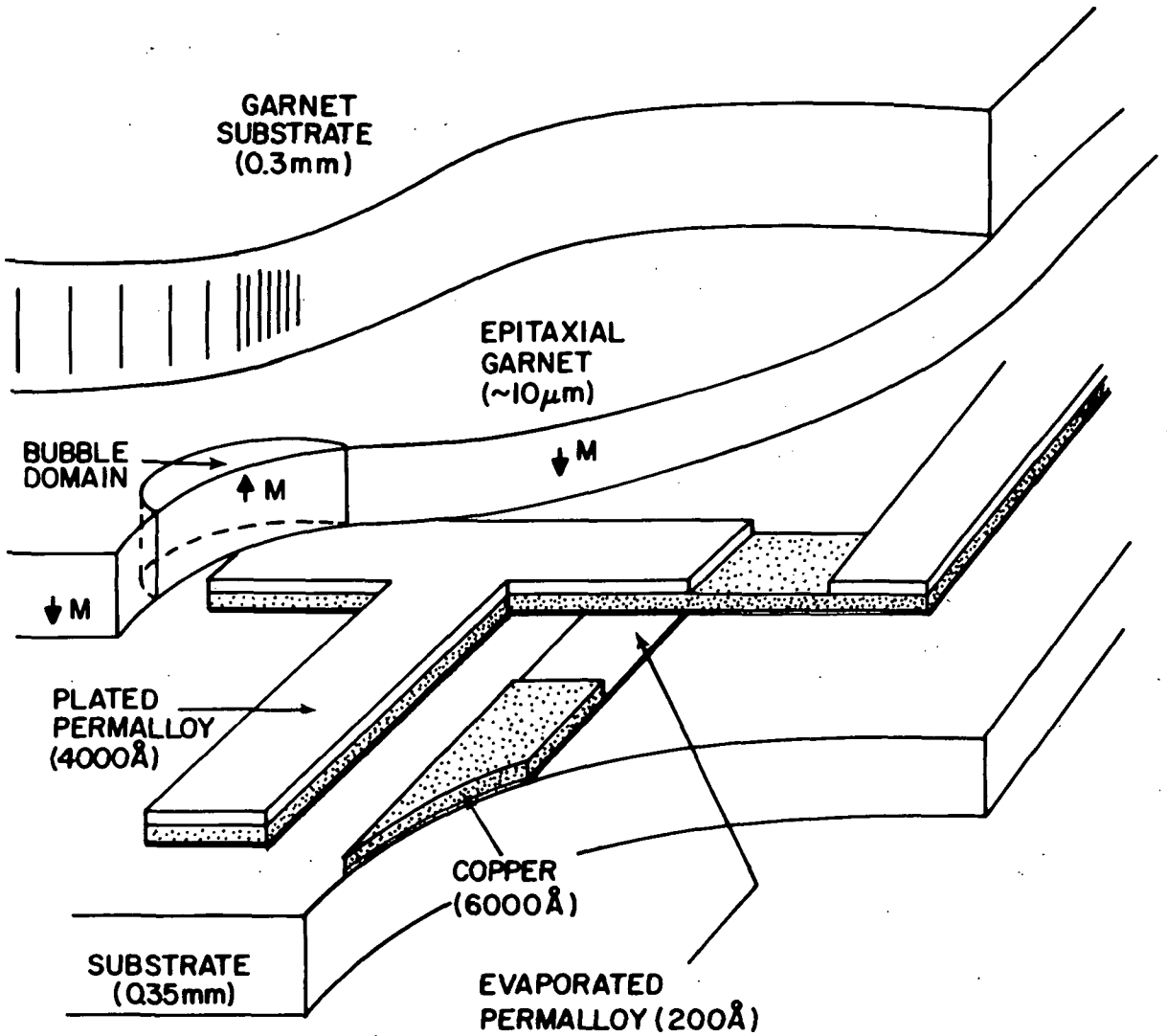


Fig. 4A2-1 Structure of the Feasibility Model Chip.

200°C and 350°C. This film is used as a plating surface for all subsequent electrodeposition steps; also, portions of it become sensors for the magnetic bubbles after the final etching step.

Step #2: The evaporated permalloy film is coated with a positive* photoresist such as Shipley AZ 111 or AZ 1350. After exposure and development of the inverse of the desired conductor pattern, copper or gold conductors are electroplated in the exposed and developed-away areas.

In order to obtain a uniform conductor thickness in all areas of the overlay during this step, it is important to design the plating mask in such a way that the plated and non-plated areas are properly balanced. To that end, it is sometimes necessary to deposit the conductor in some areas where it is not needed, but where it does not interfere with the operation of the final device. This and other aspects of the photolithographic masks are described in detail in Appendix G.

A second requirement for good results is proper pre-treatment of the evaporated permalloy film prior to electroforming the conductor. It is known in the art of electroplating that it is difficult to obtain good adhesion between copper or gold and iron or iron alloys. In our case, good adhesion was realized by pre-treating the evaporated permalloy film in the following way:

---

*Positive in this case means that the photoresist area which has been exposed to light is removed during development. Since the metal is to go where there is no photoresist, the corresponding area of the photolithographic mask must be transparent to light. Hence, the mask is clear where there is to be metal and opaque where there is to be no metal, in other words, the mask pattern is the inverse of the metal pattern.

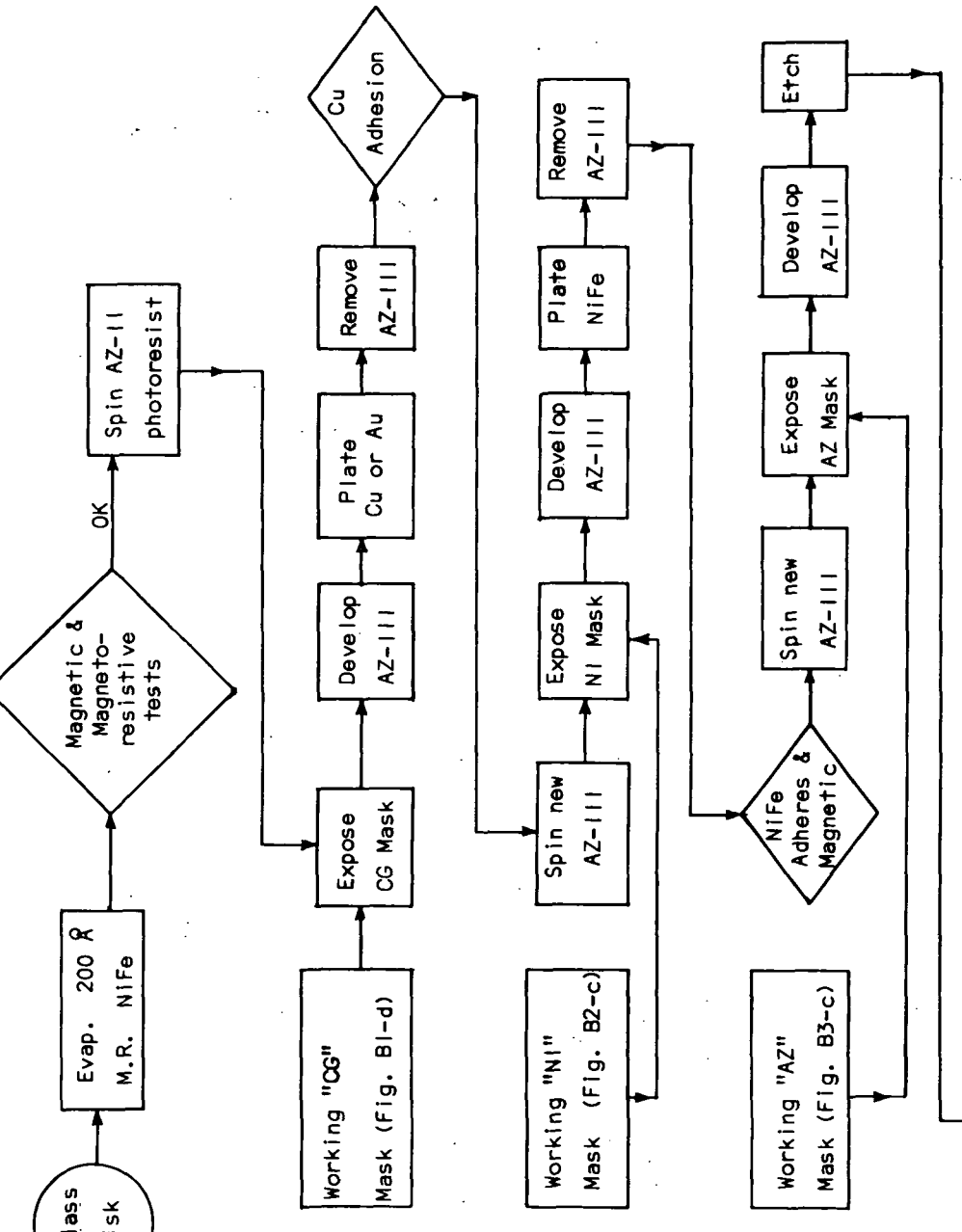


Fig. 4A2-2 Flow Chart of the Fabrication Process for the Overlay (The masks are described in Appendix G).

a) Using a very dilute copper electroplating bath (∿.075 molar copper sulfate), ∿80 to 140Å of Cu is deposited.

b) Following the deposition, the current is reversed for a short period of time, using a reverse pulse.

c) An additional 80 to 160Å layer of copper is deposited from the same bath.

Following step (c), the substrate is rinsed with water, and the conductor thickness is built up further to about 6000Å using a mixed sulfate/nitrate copper bath or a high throwing power gold bath (see [G59] page 485). The plating current density is adjusted to ∿2/3 of the maximum value which results in a low stress unburned deposit on a non-masked surface.

Following electroplating, the positive resist is removed using acetone or another suitable solvent.

Step #3: A fresh layer of positive photoresist is applied and an inverse pattern of the required thick permalloy areas (T and I bars, generators, etc.) is exposed and developed. The exposed area is again given a pre-treatment similar to the one of step #2 before electroplating.

Again it is very important to design the plate-through mask in such a way that the plated and non-plated areas are properly balanced. This balance is even more critical here because the film composition as well as its thickness uniformity is affected by improper design.

The permalloy is electroplated using a modified Wolf's plating bath, which exhibits relatively low sensitivity to small current density variations

(i.e., the composition vs. overall current density curve exhibits a relatively shallow slope). Overall current densities used were between 10 and 100 mA/cm^2. When the 10 mA/cm^2 current density was used, the resulting film contained 60% Fe, while 100 mA/cm^2 resulted in 20% Fe.

Following the electroplating of 4000Å of permalloy, the photoresist is removed as before.

Step #4: The final step in the process consists of simultaneous removal of the evaporated permalloy layer from unwanted areas and formation of the magnetoresistive sensors. Three techniques were tried:

a) Chemical etching

b) Electrochemical etching ("back plating")

c) Sputter etching

All three techniques were successfully used to give working overlays, but the yield with sputter etching was somewhat higher, probably because sputter etching is the least selective process and therefore easiest to control.

In case a), a positive resist such as AZ 111 is applied, exposed, and developed. All material which is not to be removed must be protected by photoresist after development-- T-bars and conductors as well as the areas which are to become sensors. The resist is baked at 100°C or higher in vacuum or dry N_2, and then the etching is performed with ferric chloride, Shipley Chem-polish 14, or other suitable agent. If the baking time does not exceed a few minutes, the remaining photoresist may be removed after etching if desired. In the case of the working model delivered to NASA, the photoresist was left on to provide the spaced layer between overlay and garnet film.

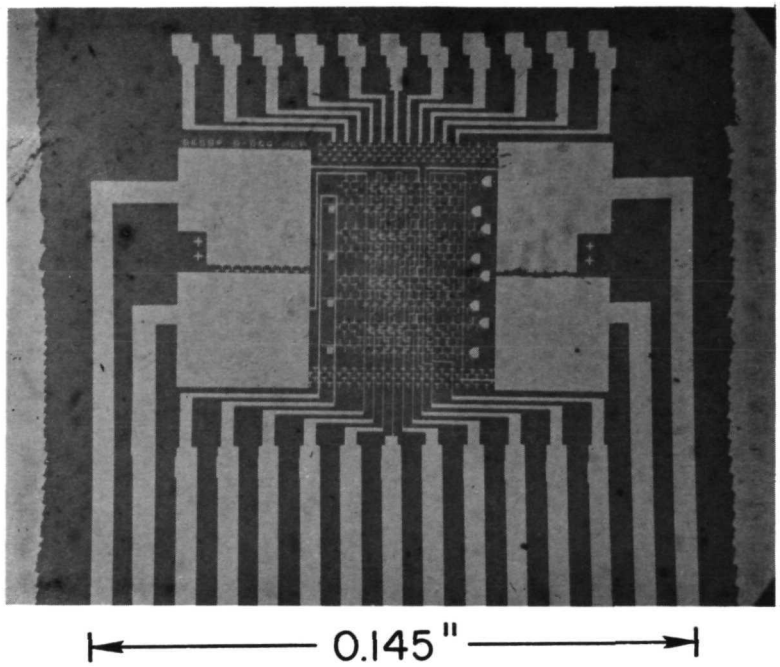
After exposure and development in cases b) and c), theoretically, only those areas must remain covered by photoresist which are to serve as magnetoresistive sensors. In practice, however, the same protect mask is used in all three cases, a), b), or c).

In case b), after the resist has been baked, the sample is mounted in a plating fixture and several alternate pulses of current are applied in forward and reverse directions using the dilute copper bath mentioned earlier as an electrolyte. If the net number of coulombs in the reverse direction is greater than in the forward direction, the evaporated permalloy layer is completely etched away.

In case c), the evaporated permalloy layer is removed using a conventional sputter-etching technique (in an argon atmosphere for 5-8 minutes). Sputtering makes the photoresist difficult to remove, and it is left on to provide spacing between the overlay and the bubble material as well as protection against atmospheric corrosion, etc.

As an example of the end product of the overall process described above, a complete overlay is shown in Fig. 4A2-3.

What has been described above is <u>one</u> consistent set of fabrication steps which works and which was used to make the overlay of Fig. 4A1-3 for the delivered feasibility model. A number of other approaches were also tried, and some resulted in working overlays, but were not incorporated into the final process for one reason or another. These working variations are discussed next.



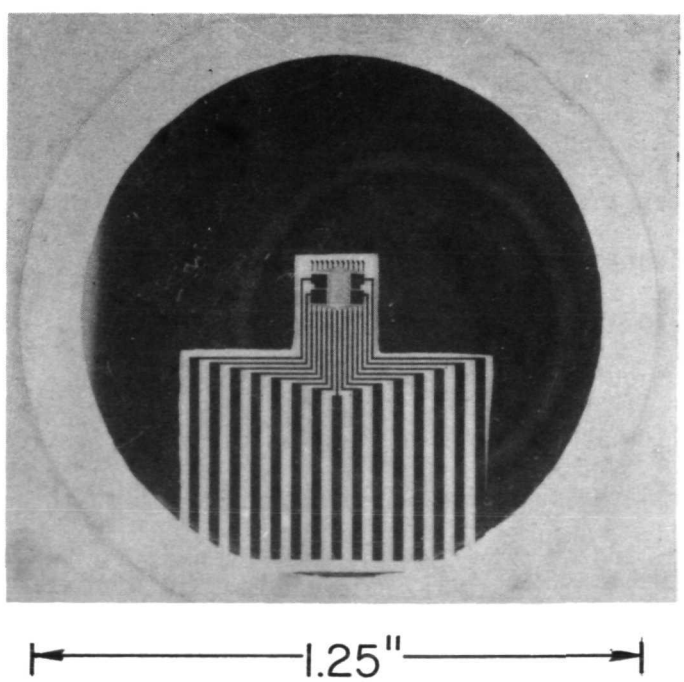


Fig. 4A2-3 Completed Overlay. (Viewed through glass substrate) Top: Active Area (metal appears as light lines on dark background) Bottom: Entire overlay (metal areas are dark).

4A2.2 Other Methods of Overlay Fabrication

This section discusses variations on the fabrication process described in section 4A2.1. The aspect which remains constant in these variations is that in all cases, the process starts with the evaporation of thin permalloy, followed by two electroplating steps and a final etch step. Some effort was devoted to forming the propation structure (T and I bars, etc.) by evaporating and then etching thick permalloy, but the results were not as attractive as those obtained by electroplating, and will be discussed no further.

"Permalloy-on-top" vs. "Copper-on-top"

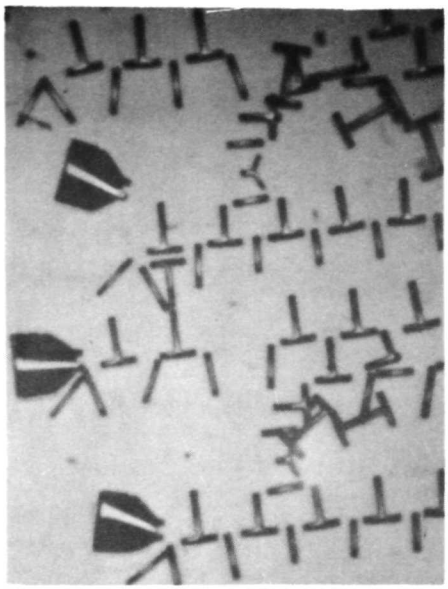
The biggest variant is the order of the propagation permalloy and the conducting copper. Section 4A2.1 has descibed a "permalloy-on-top" structure, that is, the T and I bars, etc. are formed last, on top of the conductor lines. The T and I bars are therefore the overlay layer nearest to the bubble material, and a suitable spacing must be provided to prevent direct contact between the T-bars and the bubble material; otherwise, spurious bubble nucleation can occur.

There are several reasons why the inverse structure, namely, "conductor-on-top", should actually provide a better structure from the standpoint of magnetics. The first is that the conductor provides a spacer separating the T-bar layer from the bubble material. Thus, the overlay can be in direct contact, and no extra spacer layer is needed. The second reason is that the propagation permalloy should provide a "keeper" action in the area of the control switches, concentrating more flux from the control-line current onto the bubble domain and thus reducing the current needed for

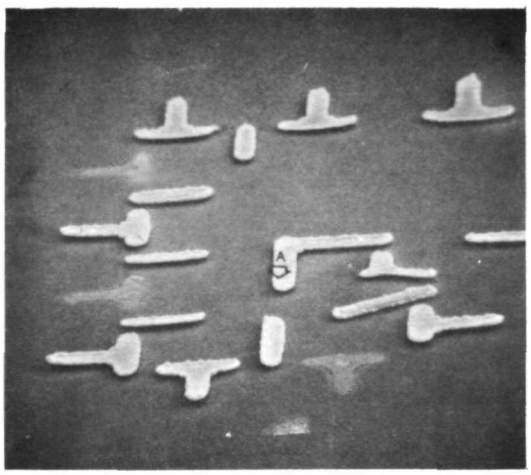
switching. In the "Permalloy-on-top" case, by contrast, the permalloy is between the control line and the bubble, thus acting as a partial flux shunt and increasing the amount of current required for switching. Finally, the use of a gold conductor would allow chemical-etch definition of the sensors with only the sensors protected by photoresist, since gold is immune to the ferric chloride etch which removes permalloy. Thus, the "protect" mask could be greatly simplified.

A number of working overlays was actually made this way. However, their fabrication was subject to a recurring problem, (nicknamed the "wooden permalloy" problem), in which the permalloy propagation structure would perform satisfactorily before copper plating, but would act completely non-magnetic after copper plating. This was eventually traced to a severe undercutting attack starting on the edges of the propagation permalloy during the copper plating (see Fig. 4A2-4, which shows the structure after copper plating and photoresist removal). By contrast, the structure of the permalloy T-bars before copper electroplating is quite acceptable, as shown in Fig. 4A2-5.

Gold plating was started rather late in the program, and it is not conclusively known whether the above problems also occur during gold plating. As mentioned, the problem was intermittent, depending perhaps on how well the exposed holes in the copper plating mask lined up with the T-bars underneath, and thus determining whether the copper plating solution could attack the edges of the permalloy bars. A small number of working copper-on-top overlays was nevertheless made by this method, and the minimum operating control currents were approximately 20-30 mA, which is within the range of operating currents for the permalloy-on-top overlays. These experiments were



a



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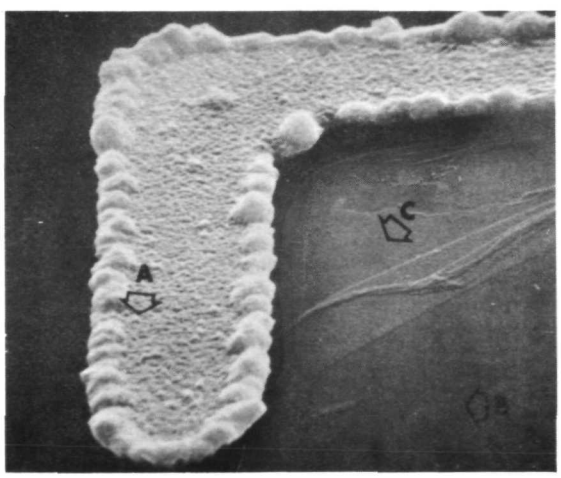

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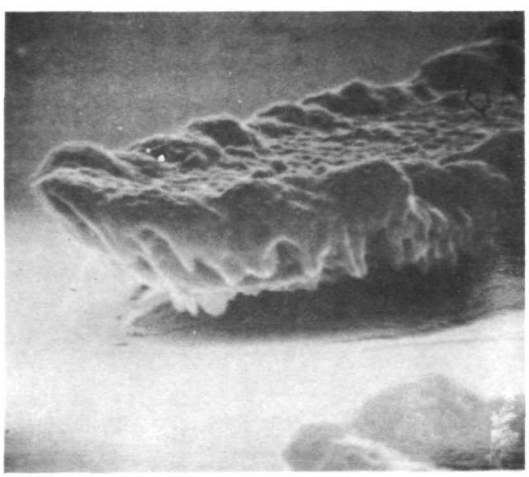


d

Fig. 4A2-4 Scanning Electron Microscope Views of Permalloy Propagation. Elements with Cu on top after Cu Electroplating. (Linewidth = 7.5μm). Note undercutting in part (d). (Courtesy of Mr. L. Bosch)

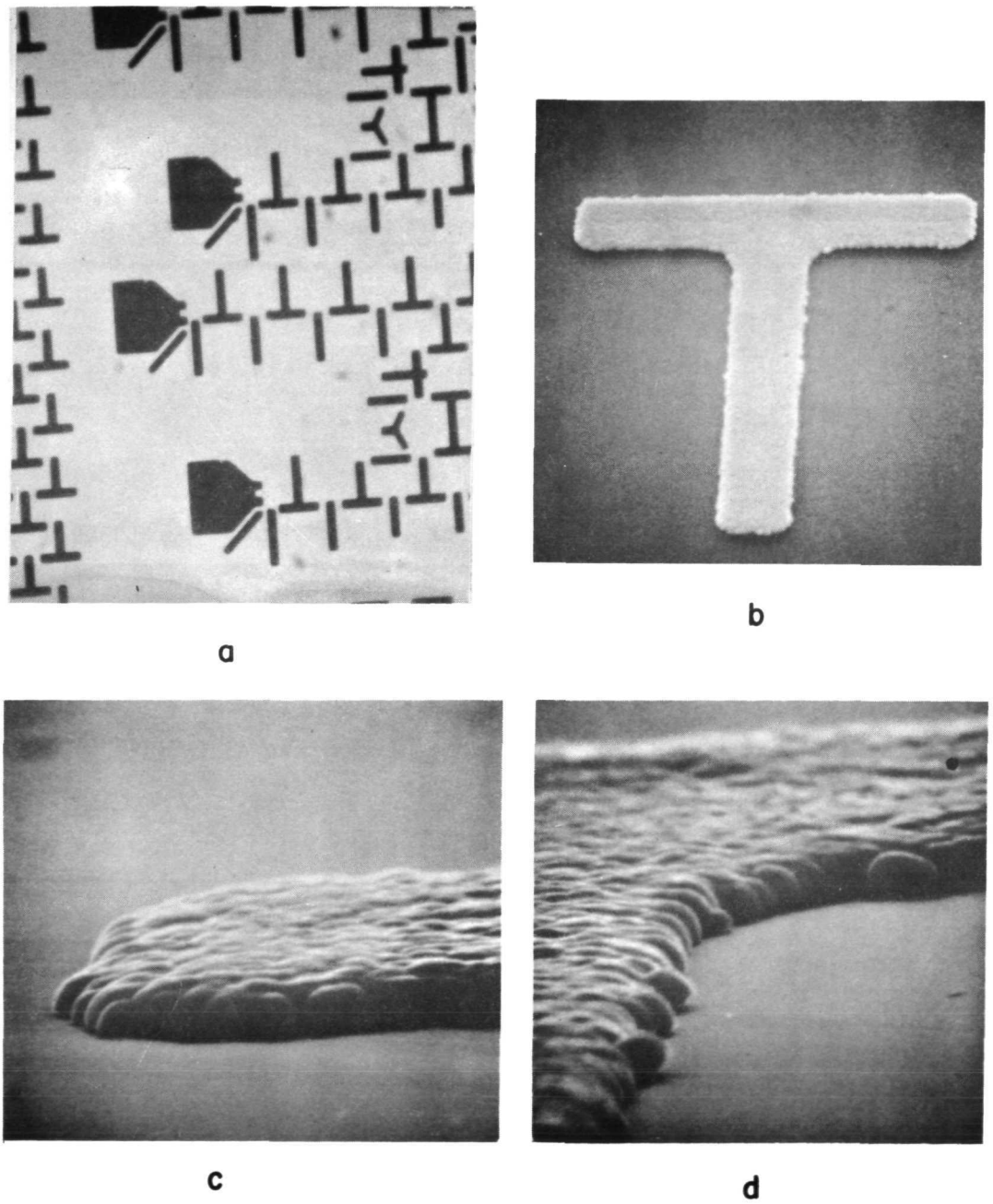


Fig. 4A2-5 S.E.M. Views of Permalloy Propagation Elements Before Cu Electroplating. (Linewidth = 7.5μm)

rather limited, but they failed to show that the copper-on-top overlays required substantially less control current. This, coupled with the fabrication difficulties described above, swung the balance in favor of the permalloy-on-top approach. (The permalloy plating bath does much less damage to the copper than vice versa.) The copper-on-top approach may eventually prove to give a superior structure, and the fabrication problems may eventually be solved.

The foregoing discussion merely explains why the course of this particular project was chosen as it was.

Negative Photoresist

The process of Section 4A2.1 uses positive photoresist throughout. Parts of the process can be and were carried out using negative photoresists such as KTFR. Of course, the negative of the corresponding mask must also be used. The problem with KTFR and its relatives is that removal of the unexposed portions is difficult, particularly if heating has occurred. Shipley stripper No. J-100 was found to work, but requires heating and is troublesome to use. The Cobehn spray reported by Reekstin [R71] was found to be ineffective. The only advantage of negative photoresist in this project was that it made the negative of the desired mask also useful. (See Appendix G.)

Permalloy pre-cleaning

The pre-cleaning of the evaporated permalloy described in Section 4A2.1 is necessary to obtain good adhesion of the adjacent electroplated layer. Presumably this is due to the formation of a thin layer of oxide on the evaporated permalloy surface. This oxide should be soluble in HCl, and indeed some preliminary experiments indicated that adhesion problems of layers electroplated onto the evaporated permalloy could be alleviated by pre-cleaning in HCl immediately prior to plating. However, the procedure of Section 4A2.1

is quite satisfactory, provided one guards against eventual copper contamination of the permalloy bath.

Other small derivations are possible besides the ones described above, but these are too numerous to mention. Fabrication of the bubble domain material is discussed next.

4A2.3 Fabrication of the Bubble Domain Material

Both bulk-grown single crystal platelets and epitaxial films of garnet were used as the bubble domain material for this study, the epitaxial film being chosen for final delivery. These materials will be described in turn.

Bulk-grown garnet platelets

The bulk garnet chosen for this study was $Sm_{0.1}Gd_{2.24}Tb_{0.66}Fe_5O_{12}$. To obtain a sufficiently low saturation magnetization $4\pi Ms$ [GSTV69], the iron lattice can be diluted (with gallium, for example) or the appropriate rare earth may be used. It was decided to choose a pure iron garnet to avoid the magnetization gradients resulting from the composition gradients that occur in Fe:Ga garnets. This narrows the choice of garnets to those having compensation temperatures near room temperature, e.g., Gd and Tb iron garnets. The proportions of these two rare earths are adjusted to give the proper amount of magnetostriction [CMN70], this being further adjusted by the addition of a small amount of samarium.

The crystals were grown by the fluxed melt technique [VBGPZ70] using a $PbO\text{-}PbF_2$ - B_2O_3 molten solvent and an 800 cm^3 volume platinum crucible. Bulk crystals were roughly oriented [111] by noting that the edges of {110} growth facets are $\langle 111 \rangle$. Precise orientation was obtained by Laue

X-ray techniques. Platelets about 0.03" thick were cut on a water-cooled diamond saw. Uniaxial regions in these slices were identified using an infrared polarizing microscope. The platelets were polished on both sides in successive stages with (30-, 9-, and 3 μm) diamond abrasive, followed by a final chemical-mechanical step until a thickness of about 0.001" was reached. This last step is performed with the platelet cemented to a glass disk for mechanical support.

The resulting magnetic properties were $4\pi Ms \sim 200$ gauss, H_c (coercinity) ~ 1 Oe, and μ (mobility) ~ 100 cm/Oe-sec. The bubble diameter was on the order of 10-12 μm, and the required bias field was ~130 Oe.

Epitaxial garnet films

As will be described in more detail in Section 4B, the garnet platelets have two main problems as bubble device materials -- a rather strong sensitivity to in-plane field and to temperature. The in-plane field response is probably due to the fact that the easy axis is not exactly normal to the platelet. The temperature sensitivity is a consequence of operating near the compensation temperature of the material. For these and for other reasons (Section 4B), it was felt that device operation would be improved by using an epitaxial garnet film as the bubble material.

Compositions investigated had the general formula

$$Eu_R Y_{3-R} Fe_{5-x} Ga_x O_{12}$$

in the range of $R \approx 0.4$ to 0.9 and $x \approx 0.9$ to 1.2. The use of Ga to control $4\pi Ms$ is permissible in an epitaxial growth process because lateral Fe:Ga

composition gradients are much less of a problem than in bulk crystal growth. This means that it is not necessary to operate near the compensation temperature of the material, and makes it possible to obtain much flatter curves of $4\pi Ms$ vs. temperature at room temperature (see Fig. 4A2-6). The temperature dependence of $4\pi Ms$ is critical because the bubble diameter is proportional to the characteristic length ℓ defined by Thiele [T69] and given by $\ell = \sqrt{AK}/\pi M^2$, where A is the magnetic exchange energy and K is the uniaxial anisotropy energy. The chosen composition of $Eu_{0.7}Y_{2.3}Fe_{3.8}Ga_{1.2}O_{12}$ has a temperature variation in $4\pi Ms$ of less than 0.3% per °C at 20°C.

Films were made and studied by procedures described in detail in the literature [GCKMR71, GACCKMP71, GACKMOPS71]. All substrates were Czochralski-grown GGG($Gd_3Ga_5O_{12}$ non-magnetic garnet) crystal wafers oriented (111). Most films were grown on substrates dipped into the melt in a horizontal plane and then rotated at 400 rpm while the melt was cooled 20°C in 5 minutes. The molar fluxed melt composition was: (Eu_2O_3 + Y_2O_3) 1.4 mole %; (Fe_2O_3 + Ga_2O_3)5.6; PbO 87.4; B_2O_3 5.6. Nominal film characteristics were a thickness of 15 μm, a bubble diameter of 12 μm, and a $4\pi Ms$ of 125 gauss. H_c was ∿ 1 Oe or less.

4A2.4 Assembly of the Feasibility Model

Assembly of the Feasibility Model can be explained with the aid of Fig. 4A2-7. Part a) of that figure shows the sample holder disassembled. The larger round disk with the visible pattern is the overlay, face up. The smaller disk is the epitaxial garnet film, face down. The structure at the extreme left is a set of bronze spring clips used to press the film and the overlay together and to control the spacing between them.

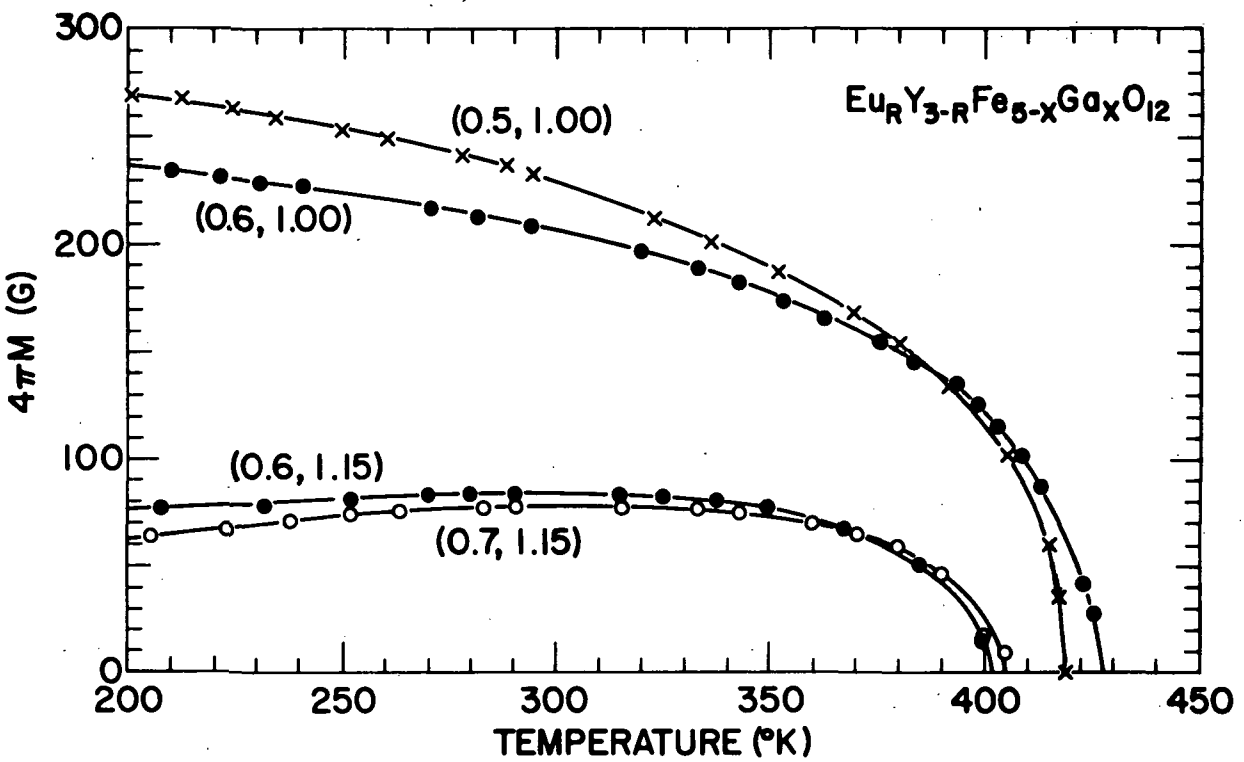
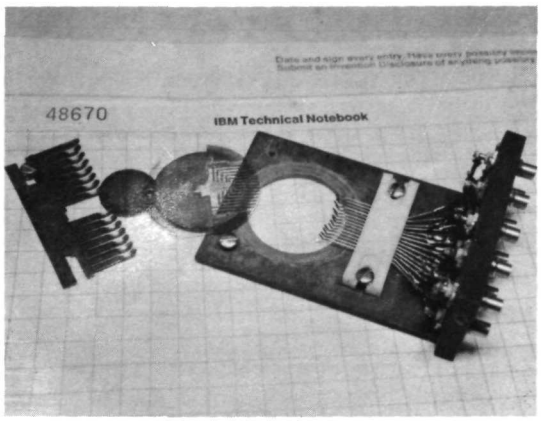


Fig. 4A2-6 $4\pi M_S$ at H = 0 vs. T for Ceramic Garnet Samples (99.99% pure) equilibrated at 1000°C. (T. McGuire and E. Giess, unpublished work).



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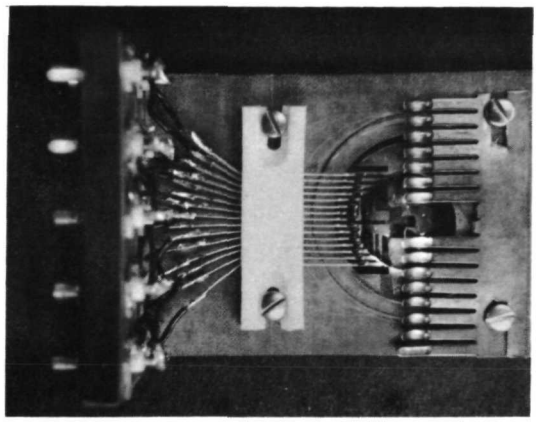

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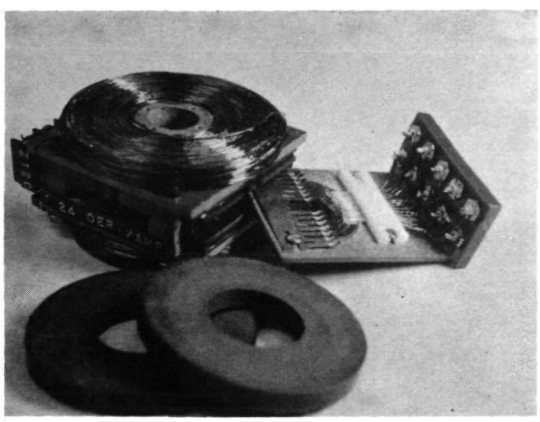

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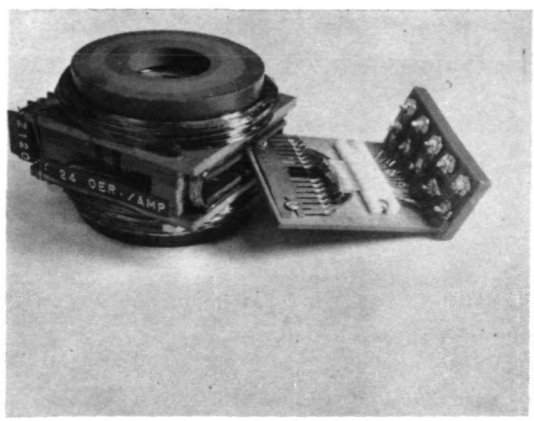

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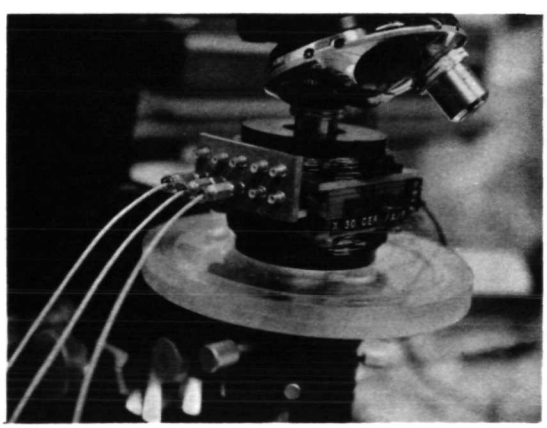

e

Fig. 4A2-7 Assembly of the Feasibility Model

Part b) of Fig. 4A2-7 shows the sample holder after assembly. The phenolic frame of the sample holder has a set of 10 miniature coaxial cable jacks, which are connected to fifteen reed-relay contacts which are pressed against the fan-out lines of the face-up overlay to provide electrical connection. The transition from part a) to part b) of the figure was made as follows. First, the two screws at either end of the white teflon bar are loosened, and the overlay is maneuvered into position; the reed relay contacts are aligned with the fan-out contacts of the overlay (using a magnifying glass if necessary), and the two screws in the teflon block are tightened again. This presses the reed relay contacts against the overlay and provides electrical contact. Next, the epitaxial garnet film is positioned (face down) so that the desired film area is opposite the active area of the overlay (using a polarizing microscope if necessary) and the sheet of bronze spring clips is placed on top of the film in such a position that several spring fingers are in place to press the film down on either side of the active area. Two screws are inserted through the slots in the spring clip sheet and tightened down until the proper spacing is achieved between the film and the overlay. The arrival of this proper spacing is usually heralded by the appearance of red interference fringes in the polarizing microscope, and can be verified by examining device operation.

Part c) of Fig. 4A2-7 shows the coil assembly which provides the rotating in-plane field and the vernier portion of the z-bias field (see also Section 4A3-1). It also shows the two permanent magnets which supply the permanent portion of the z-bias field. In part d), the permanent magnets have been put in place, and the sample holder is ready to be inserted. In part e), the sample holder has been inserted into the field assembly,

several cables have been connected, and the whole assembly is in position to allow observation of feasibility model device operation with a Leitz Ortholux polarizing microscope.

What has been provided is a simple but sturdy structure which nevertheless allows very rapid interchanging of sample holders in the field assembly, and quite rapid interchanging of either the overlay or the epitaxial film in the sample holder. The electrical and magnetic characteristics of the field assembly and sample holder are given in Section 4A3.

4A3 FEASIBILITY MODEL OPERATING INSTRUCTIONS

Viewed as a black box, the feasibility model has twenty-six electrical connections and a viewing port. This section describes what must be done to those twenty-six connections to make the action described in section 4A1.2 occur correctly in the viewing port.

4A3.1 Field Assembly Connections

As is partly visible in Fig. 4A2-7, six of the twenty-six connections mentioned above occur on a terminal block mounted on the field assembly. The field assembly contains three pairs of coils, each pair wired in parallel, and each pair producing a field in one of three mutually orthogonal directions x, y, and z. The axial direction will be called z, and the field in that direction is supplied by the pair of large coils visible in part C of Fig. 4A2-7. The coils are all visible in the disassembled view of Fig. 4A3-1. The x and y coils each consist of 50 turns of #26 copper wire with Heavy Formvar Insulation. The z-coil has 400 turns of #24 copper wire with Heavy Formvar Insulation, and is held together by Walsco Polystyrene Q-dope.

The bias field is applied in the z-direction, and although the z-coils have been called bias vernier coils, they are quite capable of providing the required bias field all by themselves, since they provide a measured 120 Oe field for 1A input current. In the position shown in part d) of Fig. 4A2-7, the pair of permanent magnets (Edmond Scientific #40482) supplies 90 Oe bias field. This can be decreased by increasing the spacing between the two magnets, or increased by adding another pair of magnets.

The remaining two pairs of coils supply fields in the x and y directions, and if they are driven 90° out of phase, they will supply the

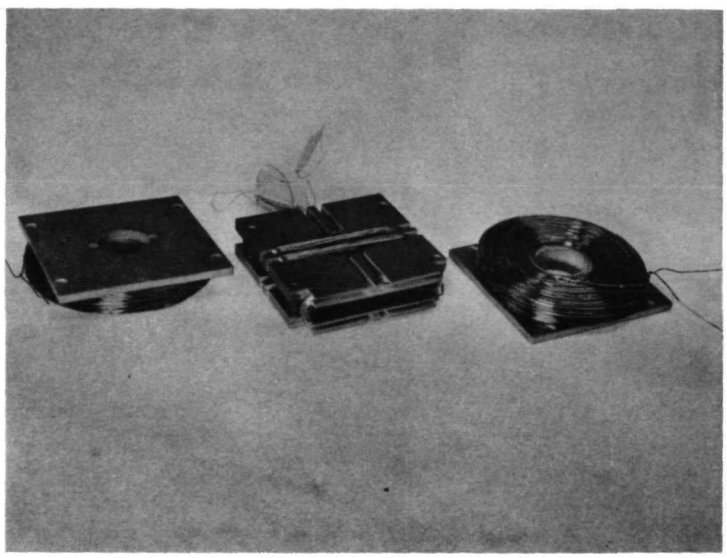

Fig. 4A3-1 Disassembled Coil Structure

rotating in-plane field needed to drive the permalloy overlay and propagate the bubble domains. Since one set of coils is wound inside the other, their field outputs are slightly different: x is 30 Oe/A, y is 24 Oe/A. If the rotating field is to have constant amplitude, the maximum x and y current amplitudes must have a 24:30 ratio.

As shown in Section 4B, it is useful to be able to supply H_z up to about 200 Oe and H_x, H_y up to about 60 Oe for measurement purposes. This requires about 2A in each pair of coils, and can be sustained for several minutes. However, the coils should not be left running with currents greatly in excess of $\sim$1A for long periods of time.

The coil characteristics are summarized below:

Coil	Field Sensitivity (Oe/A)	Nominal Current (A)	Maximum Current (A)	Resistance (ohms)	Inductance (milli-henrys)
x	30	1	2	1.6	1.4
y	24	1.25	2	1.2	1.2
z	120	+.66(a) - .1(b)	2	11	

(a) Without permanent magnets

(b) With permanent magnets

4A3.2 Sample Holder Connections

The remaining 20 of the Feasibility Model's 26 electrical connections have the form of ten miniature coaxial sockets, as shown in Fig. 4A2-7. These sockets are wired to 15 reed relay contacts which are pressed against the fan-in contacts of the overlay. The connections are as shown in Fig. 4A3-2. They allow the input of the control currents for the write, decode, and clear functions, the input current to the magnetoresistive sensors, and the output

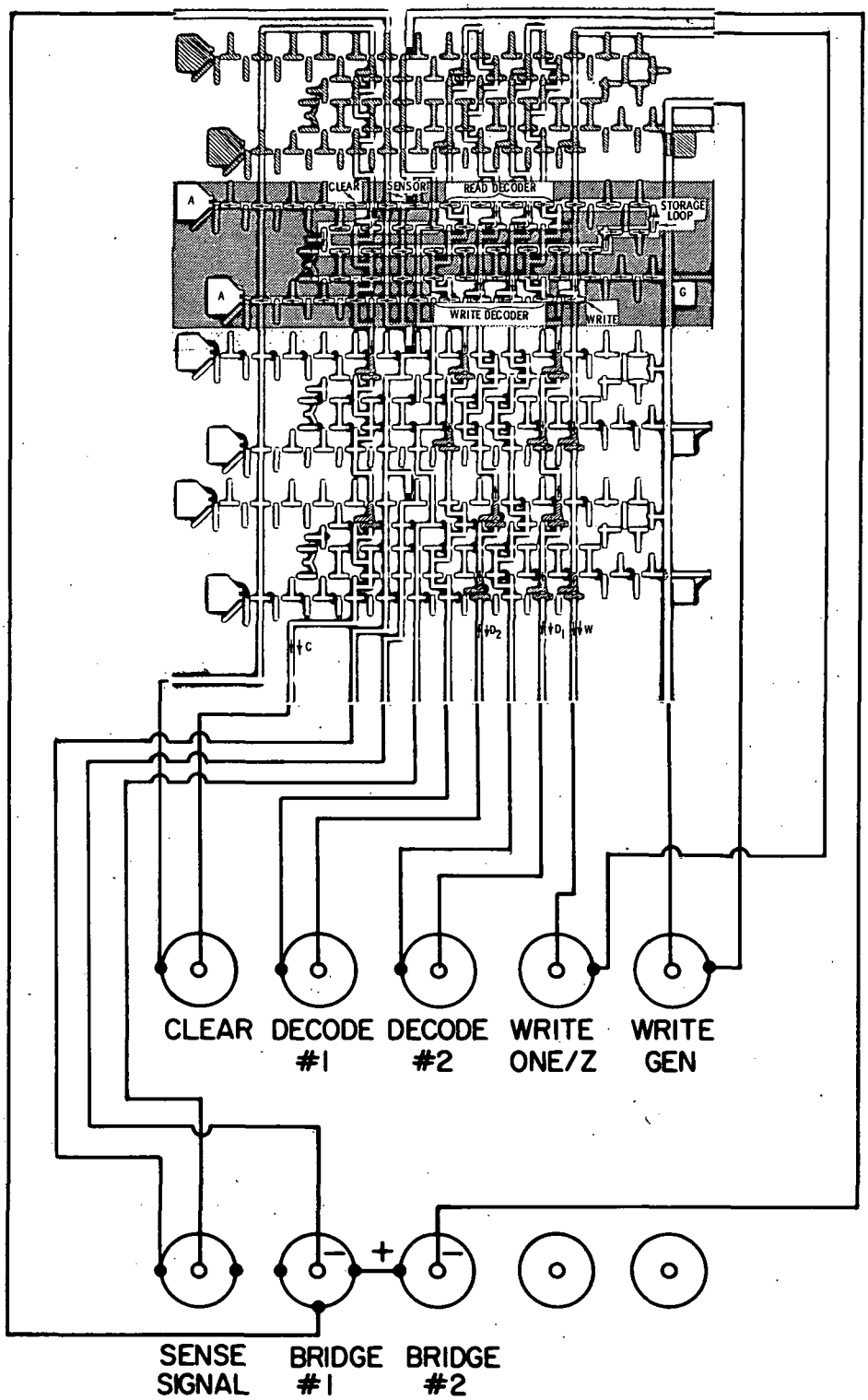

Fig. 4A3-2 Connection of the Coaxial Sockets on the Sample Holder to the Overlay.

of the resulting sense signals. The other ends of these coaxial cables are connected to a control panel shown in Fig. 4A3-3 (Except for the sense signal output, which goes to an oscilloscope or other detection means.) The schematic diagram of the control panel is shown in Fig. 4A3-4.

It will be noted that Fig. 4A3-2 shows provisions for five control current inputs in addition to the sensor connections, whereas only four control current inputs were discussed in Sec. 4A1 when the designed operation of the feasibility model was being described. This is because writing can be performed in two ways, both of which were studied in the course of this contract. The "Write Gen." connection provides current to a line which passes in the immediate vicinity of the generators, and can actually be used to inhibit the generator from emitting any bubble domains. (In the absence of this current, the generator emits a bubble during every field rotation). In this mode of operation, zeros are written into a selected register by a positive Write Gen. current, and ones will be written in for a negative or absent Write Gen. current.

As an alternative, the generator can be allowed to emit a bubble during every field rotation, and subsequently writing can be accomplished by using one of the current-controlled switches of Fig. 4A1-2 to steer the bubbles into the write decoders or to bypass the write decoders, as explained in Sec. 4A1. Only one of the four write decoders will let an input bubble pass into its storage loop, and so in this case, ones are written into a selected shift register for a positive "Write One-Zero" current, and zeros for a negative current.

It was found that the latter mode of operation required less control current amplitude, and so it was chosen as the preferred procedure. However, the other "Write-Gen." control is fully functional, and may be used if desired.

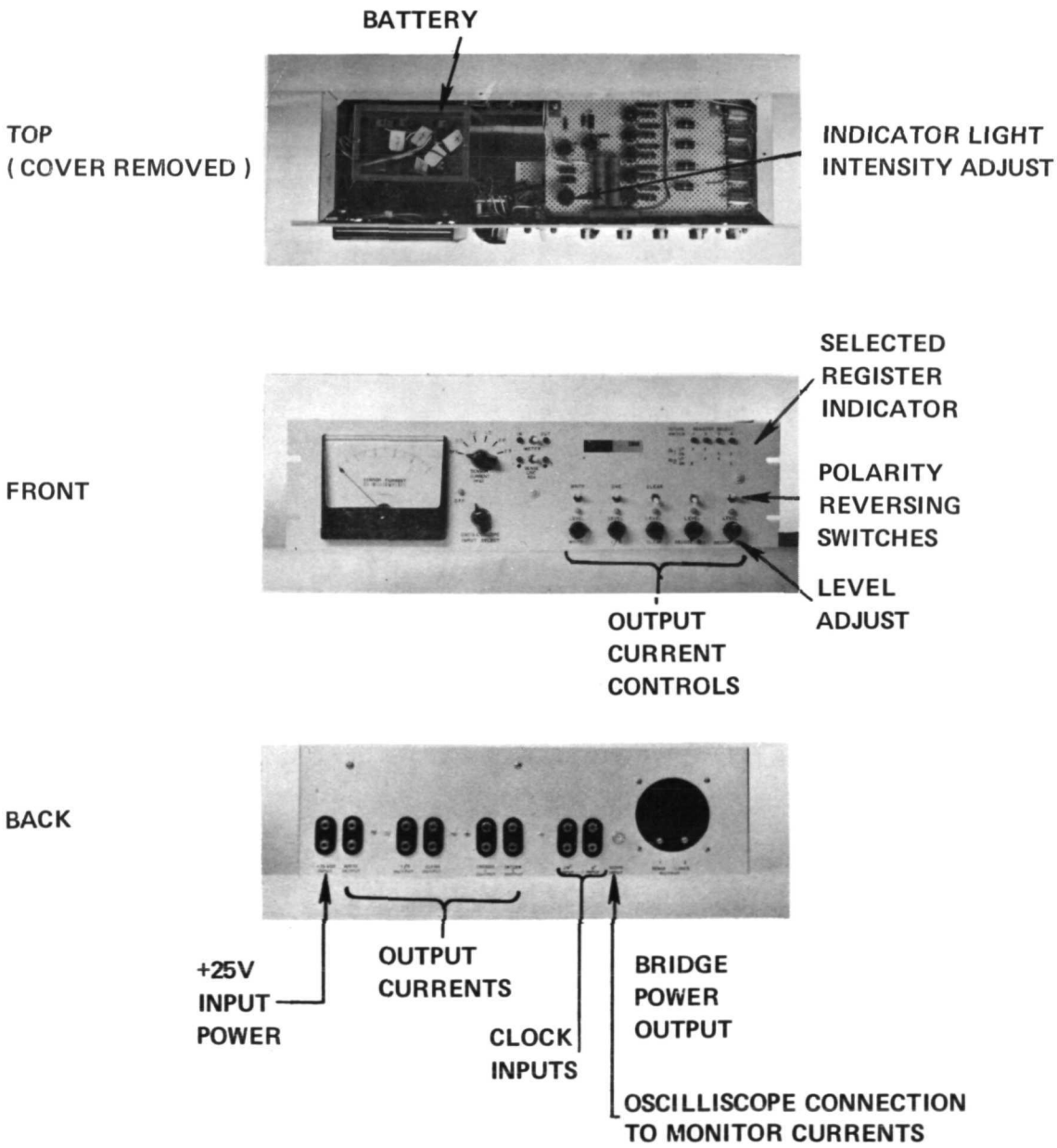

Fig. 4A3-3 Control Panel for Feasibility Model

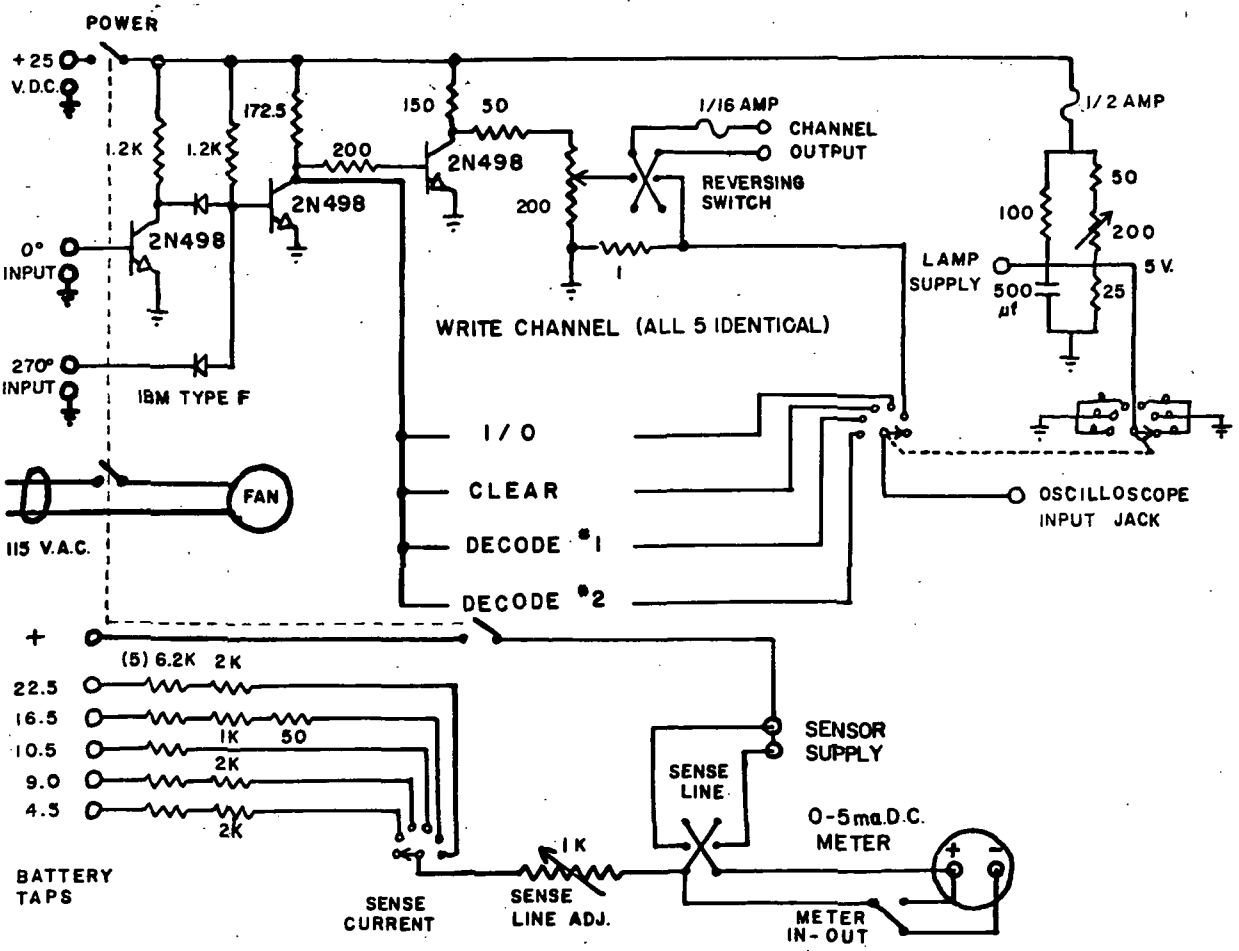

Fig. 4A3-4 Schematic Diagram of the Feasibility Model Control Panel

The control panel can supply 0-50 mA to any and all of the five control lines. As described in Section 3B2, the "Write One-Zero", "Decode 1", "Decode 2", and "Clear" line each require about 30 mA for operation, while the "Write Gen" line requires about 40 mA. The outputs of the control panel are fused for 60 mA, since currents exceeding this will damage the lines.

A sensor requires 2 mA input current to produce a 200 μV signal in sensing a bubble domain. The sensors of the feasibility model (Fig. 4A3-2 or 4A1-3) are connected in a standard Wheatstone bridge configuration, as shown in Fig. 4A3-5, with the exception that each side of the bridge has its own access. This allows each sensor to be measured separately if desired. In bridge operation, the two (-) inputs are shorted together. The control panel provides 0 - 2.5 mA sense current to each side of the bridge, i.e., to each sensor, in 0.5 mA steps. Although the sensor has been used with 16 mA input current, sense currents greater than 2.5 mA should not be used until further work is done to determine the safe operating limit of this type of sensor.

The control panel requires a $^{+}$25V DC power supply capable of putting out 1A, and a battery with 4.5, 9.0, 10.5, 16.5, and 22.5-volt taps, such as an RCA type VS131. A battery is used as the source of sensor current to lower the background noise level.

The control functions on the control panel are as follows:

CURRENT CONTROLS - The five black knobs in the lower right-hand corner are connected to potentiometers which adjust the current levels in, from left to right, the "write Gen" line, the "Write One-Zero" line, the "clear" line, and the two Decode lines. Above each black potentiometer knob

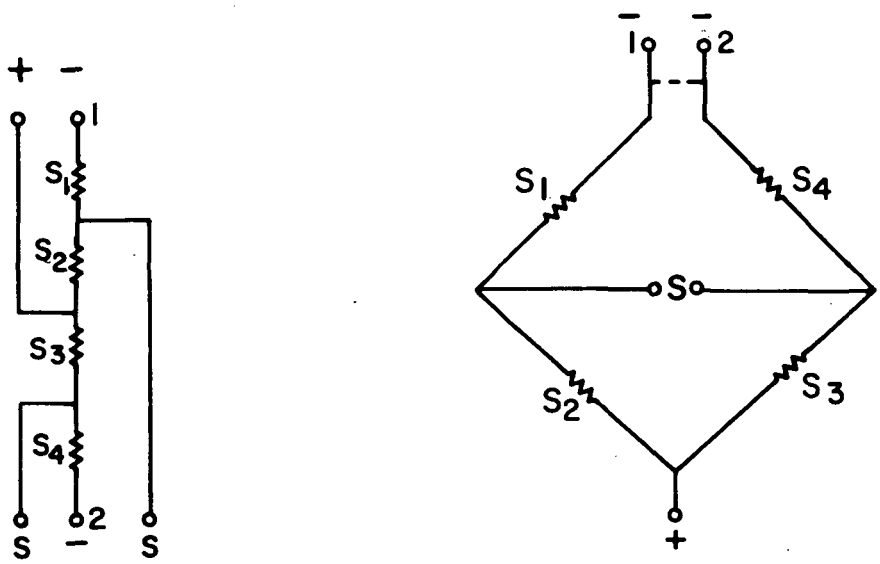

Fig. 4A3-5 Sensor Bridge Connection

is a switch which reverses the current in that particular line. When the "WRITE" switch is up, "ones" are written, when this switch is down, "zeros" are written. (as explained earlier, this function is not normally used). When the "I/O" switch is up, "ones" are written, when this switch is down, "zeros" are written. When the "CLEAR" switch is up, the bubbles in the selected shift register will be cleared out, when this switch is down, the bubbles in the selected shift register will be recirculated. The four possible up-down combinations of the two "DECODE" switches select one of the four registers, according to the following table:

Shift Register # (from the top in Fig 4A3-3)	Decode #1	Decode #2
1	up	down
2	up	up
3	down	up
4	down	down

The selected shift register is automatically indicated by the BLUE INDICATOR LIGHTS in the upper right hand corner of the panel, where there is also a small table to aid in register selection.

The currents being put out by the control panel may be monitored one at a time by connecting an oscilloscope to the

SCOPE INPUT (BNC Connector on rear of Control Box), which is across a 1-ohm resistor through which the current flows. The current to be monitored is chosen by rotating the

OSCILLOSCOPE SELECT SWITCH. Between the black potentiometer knob and the polarity reversing switch of each of the five output current controls is a yellow indicator light. As the oscilloscope select switch is rotated,

one of the YELLOW LIGHTS will be on at a time, indicating which current is being displayed on the oscilloscope. When this switch is rotated full counter clockwise, the input to the oscilloscope becomes an open circuit, and the YELLOW "OFF" LIGHT goes on indicating that nothing is being monitored.

SENSE LINE ADJ SWITCH - As shown in Fig. 4A3-5, the sensor connection of Fig. 4A3-2 is equivalent to a bridge with individual current control on each side. This switch allows the current on either side of the bridge to be monitored. Small adjustments in bridge current may be made with the SMALL TRIM-POT located under this switch. (This affects both currents.)

SENSOR CURRENT SWITCH - Selects the approximate sensor current in 0.5 mA steps up to 2.5 mA.

SENSOR CURRENT MILLIAMMETER - Reads the sensor current. Note that because of the connections described, this reads the current in one sensor, which is approximately half of the total bridge current.

METER IN-OUT SWITCH - With this switch in the "out" position (red light), the sense current milliammeter is shunted and the sense current flows directly to the bridge. Setting this switch to the "in" position (green light) puts the meter in series with the current.

The CONNECTIONS ON THE BACK OF THE PANEL are a pair of banana jacks for the 25 V DC Supply, five such pairs for the five control currents, two miniature coax connectors for the bridge currents, and a BNC connector for the scope input. These have all been discussed. The two remaining pairs of banana jacks, labelled 0° INPUT and 270° INPUT, are for the clock inputs which synchronize the control currents with the rotating in-plane field. As described in more detail in the next section, the square-wave outputs of a Hewlett-Packard HP203-A Two-channel function generator were used for this

purpose at the IBM Research Center. However, a slight modification to the control panel circuitry will allow the use of any 25V, 30 mA source synchronized with the rotating field for this purpose.

The components of the feasibility model to be delivered to NASA have now been described. The next section gives instructions for operating the feasibility model.

4A3.3 Operating the Feasibility Model

The operation of the feasibility model is best explained in terms of the timing diagram of Fig. 4A3-6, which shows how the control currents must be synchronized with the rotating field. Two separate timing schemes are shown, a simple one which allows 16 bits to be stored per register, and a slightly more sophisticated one which allows 21 bits to be stored per register.

Both timing diagrams correspond to the physical layout of Fig. 4A3-2. For convenience, the compass points N,E,S, W, (North, East, South, and West) are used to denote the rotating field direction, North being toward the top of the page in the figures showing the layout. A memory cycle consists of 23 N-E-S-W field rotations, since this is the time required for a round trip of a shift register storage loop. The notation N1, N2, ... N23 in Fig. 4A3-6 indicates a current pulse which comes on when the rotating field reaches the N direction during the 1st, 2nd, ... 23rd rotation.

In a practical memory, the storage loop cannot be quite fully populated, because it must be possible to follow a 23-rotation read or write cycle in one of the registers by 23-rotation read or write cycle in any of the other registers, and several rotations are required to make this transition. The exact number depends on the timing scheme.

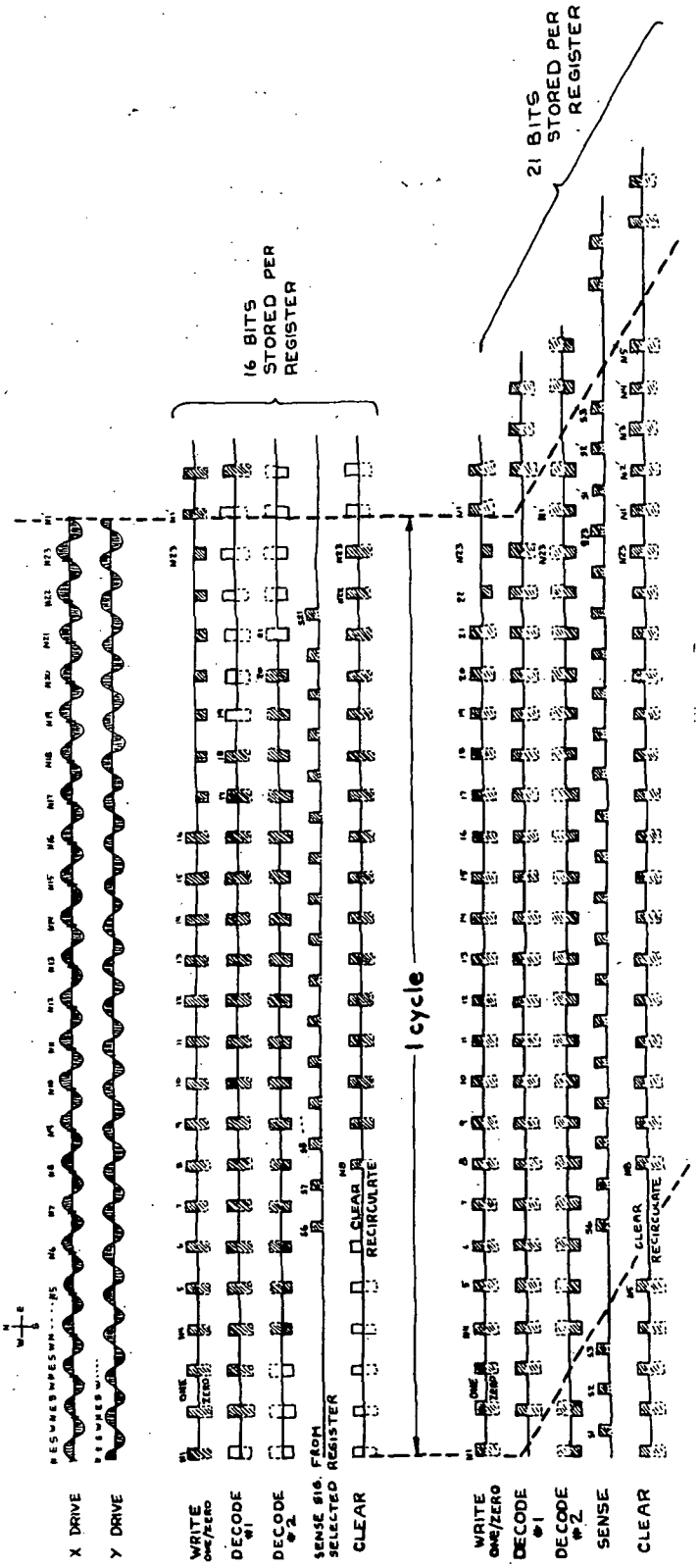

Fig. 4A3-6 Timing Diagrams for the Feasibility Model

Timing Scheme for 16-bit Storage

In the first timing scheme of Fig. 4A3-6, seven rotations are required between operations, so that 16 bits can be stored per register. In this mode of operation it is first decided which register is to be selected, and whether information is to be read out and kept in storage, or whether new information is to be written in while the old is read out. Having made this decision, the decode #1, decode #2, and clear current polarities are determined and are pulsed with that same polarity during each of the 23 field rotations, beginning with the first. If new information is to be written in, it starts on the first rotation. The successive write current pulses are positive or negative according to the information pattern to be written. The clear line current polarity is set to "clear", which means any information (bubbles) previously stored in that register is sent to the Read annihilator by the clear switch.

Because of delays in the read path (space required for the read decoder as well as implementation of the bridge sensor connection), the first of the previously stored bits does not reach the clear switch until the 8th rotation of the cycle (the new and old information blocks are synchronized, that is, the first new bit of information is entering the write decoder just as the first old bit of information is entering the read decoder). Since the proper clear current polarity is maintained only until the 23rd rotation, the last bit of information must be at the clear switch by the 23rd rotation. Therefore, the block of information can be 23-7 = 16 bits long.

This result is a consequence of setting all the control currents at the same time and keeping them set for the full 23 rotations, and of the delay between first-bit entry into the decoders and into the clear switch. Examination of the top timing scheme of Fig. 4A3-6 shows that the decode

and clear lines each carry six or seven pulses during each cycle which have no effect, because no bubble can be at the switches controlled by those lines while those pulses are occurring. The shaded pulses indicate that a bubble is allowed to be at a switch controlled by the corresponding line, the un-shaded pulses indicate that bubbles are forbidden to be at a switch controlled by that line, and that therefore un-shaded pulses cannot affect the operation of the memory. They are only there to make the timing simpler.

Reading with continued storage of the information is accomplished by proceeding as before but setting the Write line at "zero" and the clear line at "recirculate" for the entire 23 field rotations. As shown, readout of the first bit occurs during the 6th rotation, while the field is pointing south.

Timing Scheme for 21-bit Storage

As mentioned above, each control line has a "dead period" lasting from six to eight field rotations during which it enters or controls no information. The only problem is that there is no common overlap in time between these dead periods. However, by introducing delays into the various control signals and using sequential decoding these dead periods can be reduced and the information capacity of each register increased to 21 bits. This will be described shortly.

First, though, it should be pointed out that the real significance of this timing scheme is not that it allows 5 more bits storage in each feasibility model shift register, but that it allows information to be stored in the read decoder as well as in the portion of the storage loop preceeding it. One stage of the register must be kept empty. In the feasibility model, this corresponds to two cells; in the conceptual design, using the more compact decoder of Appendix C, this corresponds to one cell. Thus a decoder with

n lines, controlling 2^n registers, can store n-1 bits. In the case of conceptual design, the chip area devoted to storage is thus increased from 89% to 91%. In chips with proportionately more registers, the effect is even greater.

Returning to the 21-bit storage scheme of Fig. 4A3-6, the operation is as follows: for writing, the write line is activated at N1, as before. However, the desired decode current is delayed one rotation before it is applied to decode #1 line, and delayed three rotations before being applied to decode #2 line. The choice between writing and reading was made at N1, of course, but the clear signal is delayed by seven rotations, until N8.

The write line proceeds to write 21 bits, and finishes off the cycle with two definite zeros, instead of seven as before. By N23, the last bit of information in the block (written at N21) is in the second cell controlled by the #1 decode line, so that at the next rotation (N1'), the current in decode #1 can be changed without affecting the information block just written. The last bit of the old information block being cleared out has similarly passed out of the first decoder stage by N1', and so it is not affected by the change in current polarity either. Since the first bit of the new information block is just entering the first stage of the read decoder at N1', one has the freedom to follow the write operation in a register by 1), another write operation in that register (though that is probably not necessary), or 2) a read operation of the newly written information in that register, or 3) a read or write operation in one of the other registers.

During N1', it is possible to simultaneously be writing in the first bit of a new block, and clearing or recirculating the 4th-from-last bit of the old block. Half a cycle later, at S1', the second-from-last bit of the old block is sensed. By N3' the last bit of the old block is beyond the control of

decode #2 line, half a cycle later (at S3') it is sensed, and one and a half cycles later (at N5') it is either cleared or recirculated, depending on whether the operation from N1 to N23 was write or read.

Summary and Demonstration

With the proviso, therefore, that the skews of Fig. 4A3-6 do exist in the 21-bit timing scheme, the memory operation of the feasibility model for both schemes can be summarized in Table 4A3-1.

Table 4A3-1 - Operating Settings of Feasibility Model

Line / Operation	Write	Decode #1	Decode #2	Clear
Select Register #1		+(up)	+(down)	
Select Register #2		-(up)	+(up)	
Select Register #3		+(down)	-(up)	
Select Register #4		-(down)	-(down)	
Write	+ or -- (1 or 0)			+(clear)
Read	-(zero)			-(recirc.)
Write & Read	+ or - (1 or 0)			+(clear)

One useful laboratory demonstration allowing visual observation at quadi-static speeds, (which was used in the project presentation on 10-28-71 as well as in the movie accompanying ref. [ACGHHJKPR 71]) is the following:

1) Successive Writing - With all registers clear, set Write to "zero", Clear to "Recirculate", and decode lines to select register #1; set rotating field frequency at $\sim$1 Hz, and set Write to "one" for a few

seconds, followed by zero select register #2 and repeat, followed by registers #3 and #4. Each register now has a pattern of bubbles circulating in it. (If registers are not clear to start with, proceed as in Step 3.)

2) Successive reading - set Write to "zero", Clear to "Recirculate", and decode lines to select register #1. A sense signal corresponding to the stored information pattern in register #1 will appear across the bridge and will re-appear every 23 rotations. This can be displayed on an oscilloscope, as described in Sec. 4B1. Repeat for the other three registers.

3) Successive clearing - Set Write to "zero", Clear to "clear", and decode lines to select register #1. The sense signal corresponding to the stored information will appear once, followed by a pattern of all zeros. Twenty-three cycles are sufficient for complete clearing. Repeat for the other three registers.

This demonstration proves the essential operability of the feasibility model. It does not require the synchronization of Fig. 4A3-6 which would be used during actual memory operation, although this feature can be incorporated if desired.

The features of the feasibility model itself and the instructions for its operation have now been given. The next section (4B) describes the auxiliary equipment used to test the feasibility model, and gives procedures, results, and interpretation of those tests.

4B1 FEASIBILITY MODEL TEST EQUIPMENT AND PROCEDURES

4.B1.1 Test Equipment

The setup used to test the feasibility model is shown schematically in Fig. 4B1-1. Variations on this setup are of course possible. The components are described below. (The parts to be delivered are shown in heavy outline in the figure.)

Polarizing Microscope

A polarizing microscope is a basic necessity for observing magnetic bubble domains. This is essentially a microscope for observing samples by transmitted light. The light falling onto the sample is polarized by having been passed through a polarizing element (such as polaroid sheet), and the sample is observed through another polarizing element, placed between the objective and the eyepiece. Some ordinary microscopes can be modified for this purpose; to obtain adequate contrast, the placement and the quality of the optical elements must be such that the extinction ratio is at least 10^3. The extinction ratio is the ratio of the maximum light transmitted (obtained with parallel polarizers) to minimum light transmitted (obtained with crossed polarizers).

The inverse of the extinction ratio must be small compared to the obtained Faraday rotation in radians, which for the garnets used here is on the order of 2-5 x 10^{-3}. For further elaboration of this point, see ref [A71]. The microscope used for this purpose at the IBM Research Center is a shock-mounted Leitz Ortholux equipped with a 100 watt halogen lamp illuminator. The magnification most commonly used with the feasibility model and its 10 μm bubbles is 80X, obtained with an 8X objective and a 10X eyepiece. This allows the entire overlay pattern to be observed at once.

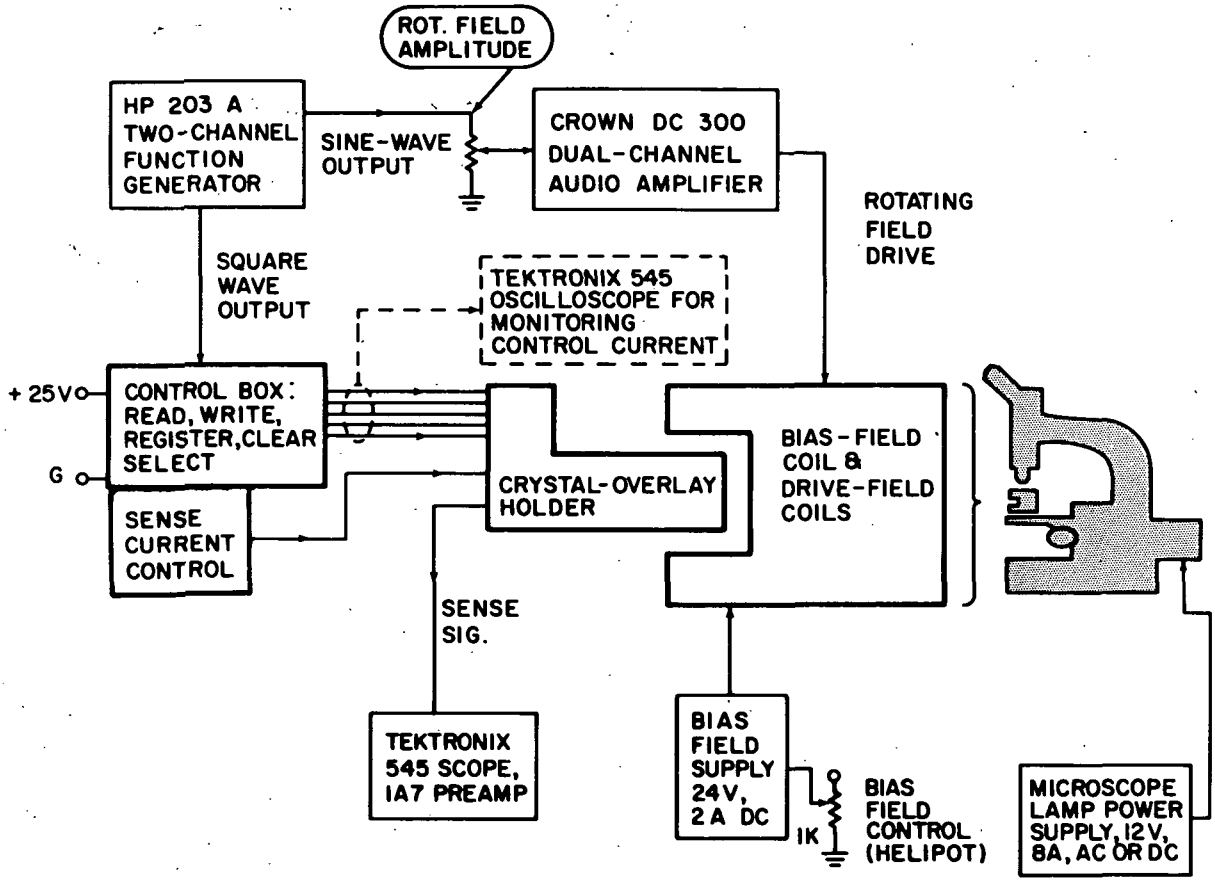

Fig. 4B1-1 Test Station for Feasibility Model

Bias Field and Rotating Drive Field Assembly

This was described in detail in Sections 4A2.4 and 4A3.1.

Control Box (Panel)

This was described in detail in Section 4A3.2.

Rotating Field Source

The rotating field which actuates the permalloy overlay is supplied by two sets of coils which are at 90° to each other in space and which are driven by currents which are 90° out of phase with each other in time. The X-coils have a net d.c. resistance of 1.6Ω and provide 30 Oe/A, while the Y-coils have a net d.c. resistance of 1.2Ω and provide 24 Oe/A. A maximum of 50 Oe is sufficient to demonstrate all effects of interest, so whatever drives the coils must be able to provide $\sim$ 2A into about a 1.5Ω load, for a maximum r.m.s. power of 6 watts per coil.

This can be accomplished in several ways. For example, four pulse generators (one positive and one negative per coil) can be connected to a programmed timing ring. However, for various reasons,the approach taken at the IBM Research Center was to use a HP 203-A Variable Phase two-channel function generator. Each channel generates both a sine wave and a square wave at frequencies between .005 Hz and 60 KHz. The internal impedance of this unit is too high to drive the coils directly, and so the two sine-wave outputs (90° apart in phase) are connected to a CROWN DC 300 dual-channel amplifier (See Fig. 1). This unit has considerably more power capacity than needed (190 watts RMS per channel), but is one of the few amplifiers available with adequate low-frequency characteristics (it is dc-coupled). Normal operating frequency for usual observation is on the order of 1 Hz, but for detailed studies the very low frequencies ($\geq$ .005 Hz) are often useful. The feasibility

model has also been run at frequencies up to 10 KHz, the 2dB point of the coils. The amplifiers 3dB point is $\sim$ 100 KHz.

The amplitude of the rotating field is adjusted by attenuating the input to the CROWN amplifier. The single control consists of two ganged 1 KΩ potentiometers. Each has been indivudually wired in series with the proper resistance so that the peak amplitude of the X and Y field are always equal and so that the potentiometer dial reads directly in oersteds. Otherwise, it is necessary to monitor the current in both the X and the Y coil.

This amplitude control requires re-calibration if a power amplifier other than a CROWN DC 300 is used.

Bias Field Supply

The bias field can be provided entirely by permanent magnets. However, to allow operating margins to be examined, the feasibility model has z-field coils which act as a vernier control in addition to the permanent field supplied by the ring magnets of the structure. The z-coil sensitivity is 120 oersted/amp and its resistance is 11 Ω . A two-amp, 24 volt dc supply will allow 240 Oe to be generated by the z-coil. This is probably twice the maximum that will ever be needed. To allow precise settings of the bias field, it is recommended that a power supply be used which can be remotely controlled by a variable resistor. Using a 10-turn potentiometer for this variable resistor provides adequate precision.

Crystal-Overlay (Sample) Holder

This is described in detail in Sections 4A2.4 and 4A3.2

Control Current Source (in Control Panel)

Control current is needed in five control lines of the feasibility model: generator control, one/zero control (both associated with writing), two decode lines, and clear control. Each line has $\approx$ 20Ω resistance and

requires ± 50 mA maximum for test purposes. The control currents must be on for ≈ 1/4 of a rotational field cycle, and must be synchronized with the rotating field. With a programmed timing ring, this requires an extra generator or two. In the present approach at the IBM Research Center, one of the square-wave outputs of the HP 203-A function generator was connected to a special control box which cuts the pulse length in half, splits the signal five ways, and amplifies it sufficiently to drive the lines. The control currents can be monitored by connecting a 1 Ω resistor in series with the control lines and displaying the voltage across this resistor on an oscilloscope with 10 mV/cm sensitivity. The polarity and amplitude of current in any of the five control lines can be controlled by switches and potentiometers on the control box. This control panel is described in detail in Sec. 4A3.2, and will be supplied to NASA. If a HP 203A is not used, slight modification will allow the control box to be driven by any 25V, 30 mA source synchronized with the rotating field.

Sense Current Source (in Control Panel)

The sensor bridge requires a supply current of about 4 mA into 50 Ω. This is supplied by a simple battery-resistor network with a milliammeter readout, which is described in Sec. 4A3.2, and will be delivered to NASA.

Sense Signal Detection

The sense signal can be observed on any differential-input oscilloscope with an 0.1 mV/cm sensitivity. We have been using a Tektronix 545 oscilloscope with a high-gain 1A7A preamplifier.

In summary, the test station for the feasibility model is described in Fig. 4B1. Those parts outlined with heavy lines will be supplied to NASA. The remaining equipment or their equivalent must be supplied by NASA.

4.B1.2 Test Procedures

Overlays were tested with bulk-grown single-crystal garnet platelets polished down to the required (20-30 μm) thickness, as well as with epitaxial garnet films grown from the liquid phase. The platelets whose growth was described in Sec. 4A2.3 had the composition $Sm_{0.1}Gd_{2.24}Tb_{0.66}Fe_5O_{12}$. For comparison, tests were also performed using a $(Er,Tb)_3(Fe,Al)_5O_{12}$ platelet obtained from the Xtalonics Division of Harshaw Chemical Company. Growth of the $Eu_{0.7}Y_{2.3}Fe_{3.8}Ga_{1.2}O_{12}$ epitaxial films was described in Sec. 4A2.3. For brevity, both platelets and films will be referred to as crystals.

The crystal was mounted in the crystal-overlay holder shown in Fig. 4A2-7. The spacing between the crystal and the overlay was found to be very critical. If the crystal is too close to the permalloy overlay ($\leq$5000Å), domain nucleation results while if the crystal is too far from the permalloy overlay ($\geq$ 10,000Å), the field from the permalloy is too low for proper device operation. The spring clip shown in Fig. 4A2-7 was used to press the glass-mounted platelet or the epitaxial film against the overlay. This procedure caused some nucleation problems with overlays which had the permalloy plated over the copper control-line metallurgy. This could be prevented by leaving a non-magnetic spacer layer, such as photoresist, on top of this type of overlay. Overlays which were fabricated with the control line metallurgy plated over the permalloy metallurgy gave a sufficient space between the crystal and the permalloy to eliminate nucleation problems. Additional problems were dust particles on the overlay or crystal, and a non-planar crystal surface. The problems encountered in this work clearly indicate that a separate overlay technology will require that the overlay and crystal surfaces be polished to an optical flatness.

The test frequency was determined by the HP 203A function generator and could be varied from 0.005 Hz to 10 KHz. Most of the visual observations were made with a test frequency of approximately 1.0 Hz. Occassionally the frequency was reduced to less than 0.1 Hz to study the details of domain behavior during the cycle.

The bias field was adjusted to give an optimum bubble diameter. Most of the testing of the first three overlay designs consisted of determining the minimum rotating drive-field required for operation of the various device functions. Failure modes were studied in order to improve the design. In the fourth and final overlay design, more extensive operating margin measurements were made.

Results of the tests described above are given in the next section.

4B2 FEASIBILITY MODEL TEST RESULTS

Three preliminary overlay designs were executed and tested before fully satisfactory operation was obtained with the fourth design, shown in Figs. 4A1-3 and 4A3-2 and until now referred to simply as the overlay design. These four overlay designs are shown in Fig. 4B2-1 (a-d) in chronological order. In parts, a, c, and d, only the permalloy pattern is shown. In part b, both the permalloy pattern and the conductor lines are shown. All four patterns are to the same scale - the bottom edge of any one of the four parts (a - d) of Fig. 4B2-1 corresponds to a distance of .0424" or 1.08 mm. Variations from the 7.5 μm nominal linewidth are due to over-or-under-exposure which occurred during the fabrication of the four overlays shown in the photographs.

The preliminary designs will be summarized first, followed by a more detailed discussion of the final design.

4.B2.1 Tests On the Three Preliminary Designs

The test results for the first three overlay designs (using the garnet platelets of Sec. 4B1.2) are summarized in Table 4B2-1. The emphasis here is not so much on detail as it is on tracing the evolution of the final design and presenting a brief catalogue of pitfalls to avoid in designing bubble domain devices.

Design I (Fig. 4B2-1a)

The overlay fabrication process was in the early stages of development while this design was fabricated. The fan-out mask was not yet completed, therefore there is no data on control line or sense functions. The major conclusion reached from the results of testing overlay design I was that the operation might be improved by decreasing the gap space between the T and I bars from 7.5 μm to 3.8 μm.

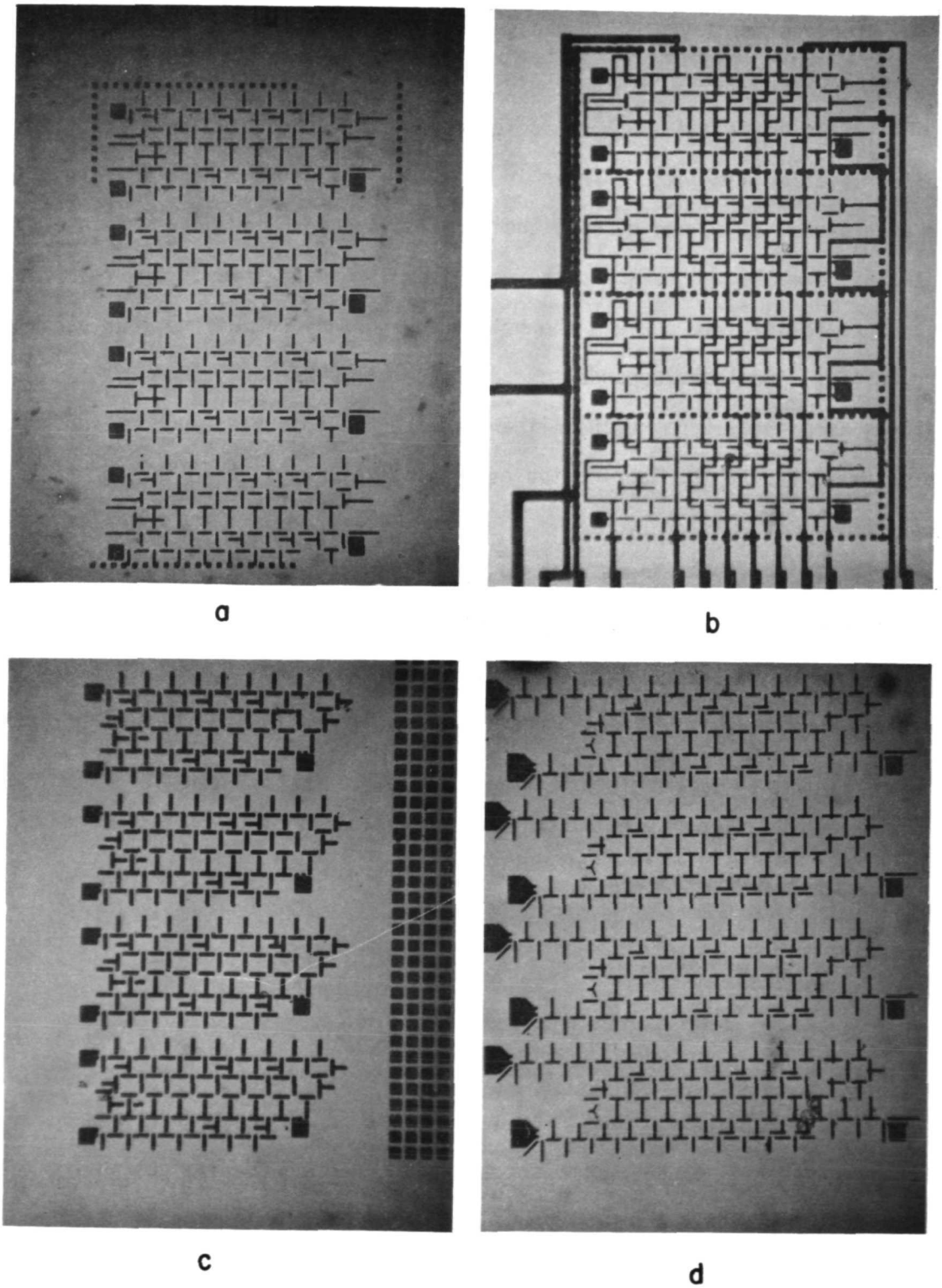

Fig. 4B2-1 Evolution of the Final Overlay Pattern

Table 4B2-1: Summary of Overlay Test Results (Minimum Operating Values)

Device Function	Design I	Design II	Design III	Design IV
Generator	requires $\geq$ 60 Oe (thin permalloy, $\sim$ 2300A)	Fairly good (5000A permalloy better than 2000A)	Does not work (Mother pulled off)	OK (14 Oe) (4000A permalloy)
Annihilator	Marginal	Poor	Poor (current helps)	Good (< 10 Oe)
Corner #1[(a)] Corner #2 Corner #3 Corner #4		marginal marginal	OK (10-20 Oe) OK (10-20 Oe)	OK (< 13 Oe) OK (< 13 Oe) " "
Junction[(a)]		unreliable (50%)	Tendency to split bubble	OK (< 13 Oe)
Write-Gen	no fan-in lines	OK(30-40 mA)	Pulls domain off gen. (20-60 Oe)	OK (30-40 mA)
Write-One/Zero		OK($\sim$20 mA)	Not in overlay	15 Oe, 25 mA
Decode		OK ($\sim$20 mA)	OK (20 mA)	15 Oe, 25 mA
Clear		OK ($\sim$20 mA)	OK	15 Oe, 25 mA
Sense		$\sim$ 0.1 mV (a) 0.5mA very noisy	not tested	$\sim$0.2 mA (a) 2 mA, sig/noise $\sim$3

(a) See Fig. 4B2-2 for this nomenclature.

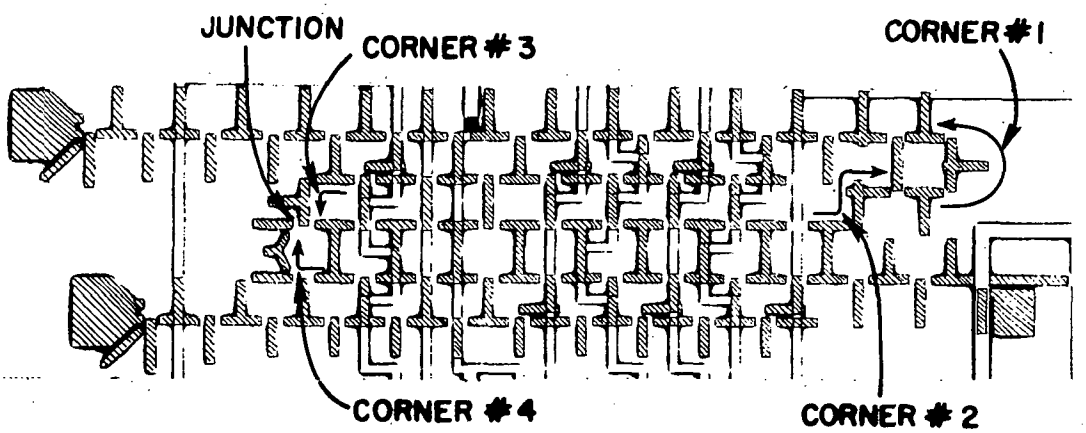

Fig. 4B2-2 Explanation of Nomenclature in Table 4B2.1

Design II (Fig. 4B2-1b)

The second overlay design was fabricated with the reduced gap (3.8 μm), and small changes were made to generators and annihilators to try to improve their performance. In addition, each register was surrounded by a "bubble corral" made up of a series of small permalloy squares, intended to keep stray bubbles from entering or leaving a register (Due to programming difficulties, only a portion of this corral appears in the Design #1 overlay of Fig. 4B2-1a).

The reduced gap of 3.8 μm caused a poor yield in the magnetoresistive film etching step. In addition, the test results indicated a number of problem areas:

a.) Generators - for 2000 Å-thick plated permalloy, the generators failed because the "mother" bubble was pulled off the generator. This was eliminated by using 5000 Å permalloy, which resulted in fairly good operation.

b.) Corners and Junction - these were unreliable, due to the strong poles produced by the extra-long bars used at these locations.

c.) Storage Loop - The storage loop is too narrow, as shown by the fact that in one case 12 mA suffices to operate the decode switch when there is only one bubble in the storage loop, but a fully populated loop requires 35 mA to overcome bubble - bubble interactions.

d.) Corral - This turned out to be more trouble than it was worth. The little squares trapped bubbles, all right, but these trapped bubbles would then interact with legitimate bubbles near them, thus turning one-shot errors into permanent ones. Also, they present a shorting hazard between the control lines.

e.) Annihilators - these were quite poor, failing to annihilate incoming bubbles most of the time. This caused backups making the clear switch difficult to test, and allowed stray bubbles to wander to all kinds of unwanted locations.

f.) Sensing - One of the worst effects of annihilator failure is a large noise in the sense line. This comes about as follows: at this point in the design, the bridge arrangement was not being used. Rather, a series-compensation scheme was used in which a dummy sensor was to cancel the magneto-resistive drive-field response of the active sensors. The resistance of the dummy sensor was equal to the sum of the four active sensors' resistance, and the dummy sensor had its easy axis transverse to the measuring current, while the active sensors had easy axes parallel to the measuring current. When all the sensors are being driven only by the drive field (i.e., no bubbles are present), the resistance of the dummy is high while the active sensors' resistance is low, and vice versa. The sum resistance of the series combination thus tends to stay constant as long as all sensors are being driven by the same field, which means that any net resistance change must be due to a bubble. This scheme has the further advantage of needing only two connections.

The trouble is that the whole scheme depends on no bubbles ever getting to the dummy sensor. Unfortunately, the dummy sensor was fairly close to an annihilator, and stray bubbles from the malfunctioning annihilator would pass the dummy sensor often enough to shoot the whole cancellation scheme to hell.

In addition, the series-compensation scheme provides no cancellation at all for inductive pickup noise, which at 10 KHz rotating drive field is on the order of 1-3 mV.

Design III (Fig. 4B2-1c)

Overlay design III used a gap space of 7.5 μm between the T and I bars. This change improved the yield in etching the magnetoresistive sensors, which were located between T and I bars. Other changes and their results were:

a.) Generators - The generator design was changed from one with a continuous mode to a normally-off, current-controlled mode. In addition, the one/zero switch was eliminated, leaving generator control as the only means of writing. This proved to be a mistake, since the new generator design was found to be much poorer than that of design II, and the current control was unable to bring the generator out of its normally-off state. This meant that the only way to test the overlay was to run the annihilators backwards as generators, obtain some bubbles, reverse the field, make measurements on the fly, and repeat the procedure.

b.) Corners and Junctions - All T and I bar lengths were made approximately equal, which improved cornering and junction operation. However, the new junction had a strong tendency to split bubbles, and further improvement was clearly needed. (In retrospect, it can be shown that the junction of Fig. 4B2-1c should split bubbles).

c.) Storage Loop - This was widened, and the discrepancy between decode currents needed for singly-populated and fully populated registers was significantly reduced, indicating a decrease in bubble-bubble interaction. This experience was thus useful in showing how narrow a storage loop can be made.

d.) Corral - This was eliminated, with no ill effects.

e.) Annihilators - In this third overlay design, a current loop was used around the annihilator. This improved its operation, but the annihilator was still very marginal.

f.) Sensing - It must be realized that there were overlaps in testing the various designs. The permalloy pattern is usually ready first, followed by overlays with both conductors and permalloy, and finally, overlays with sensors. By the time the extent of the sensing problem on the design II overlays became known, the masks for design III were already made, and so design III suffers from the same sensor problems as design II.

4B2.2 Tests on the Final Design

In view of the problems described above, design III was abandoned, and an intensive effort was put into design IV. The generator chosen was the one from the second round, which had worked quite well. All "split-T's" were eliminated from the propagation paths and replaced by solid T-bars. The troublesome junction-splitter was replaced with a Y-bar design. Whenever possible, functions were separated - generators and eaters were moved far from propagation tracks, double corners were moved further from each other. An L-bar corner was added at the generator end of the storage loop. The shape of the annihilator was changed and its size was increased by more than 50%. The gaps between the T and I bars were again reduced to 3.8 μm, and the fabrication difficulties of Design II were solved by the sputter-etch technique of Sec. 4A2.1. Finally, the sensor location was changed, and the sensors were connnected in a bridge rather than a series - compensation configuration to lower the noise level.

In addition, it was decided that some of the previously mentioned problems were due to the fact that a 10 μm-diameter bubble in a 30 μm-thick platelet is a "tall, thin" bubble whose proportions are removed by a factor of 6 from the preferred 2:1 diameter: height ratio defined by Thiele [T 70], and that operation of the overlay should be improved by using bubbles with the "right" proportions. Particularly in the case of annihilators, it seems intuitively obvious that it should be easier for the same annihilator to collapse a bubble with one-sixth the volume. Therefore, for design IV, a large number of tests were performed with epitaxial garnet films as well as with garnet platelets.

The changes described above resulted in a design which was completely operable. In general, the device operation was better for the LPE films than for the bulk platelets: sensitivity to temperature and in-plane field were much better with the film, and the platelet still required 40 Oe for operation of the annihilator vs. 10 Oe or less for the film. However, the larger bubble diameter to height ratios obtained with films required minor design changes in some of the device functions which were satisfactory for platelets. The corner design was found to be more critical for films than platelets. The current-controlled switches also required modification. Typical in-plane drive field requirements at quasi-static frequencies for operation with the $Eu_{0.7}\ Y_{2.3}\ Fe_{3.8}\ Ga_{1.2}\ O_{12}$ film described in Sec. 4A2.3 are given in the last column of Table 4B2-1. Quasi-static operating margins for the various functions are shown in Fig. 4B2-3.

The significance of these results is discussed in the next section.

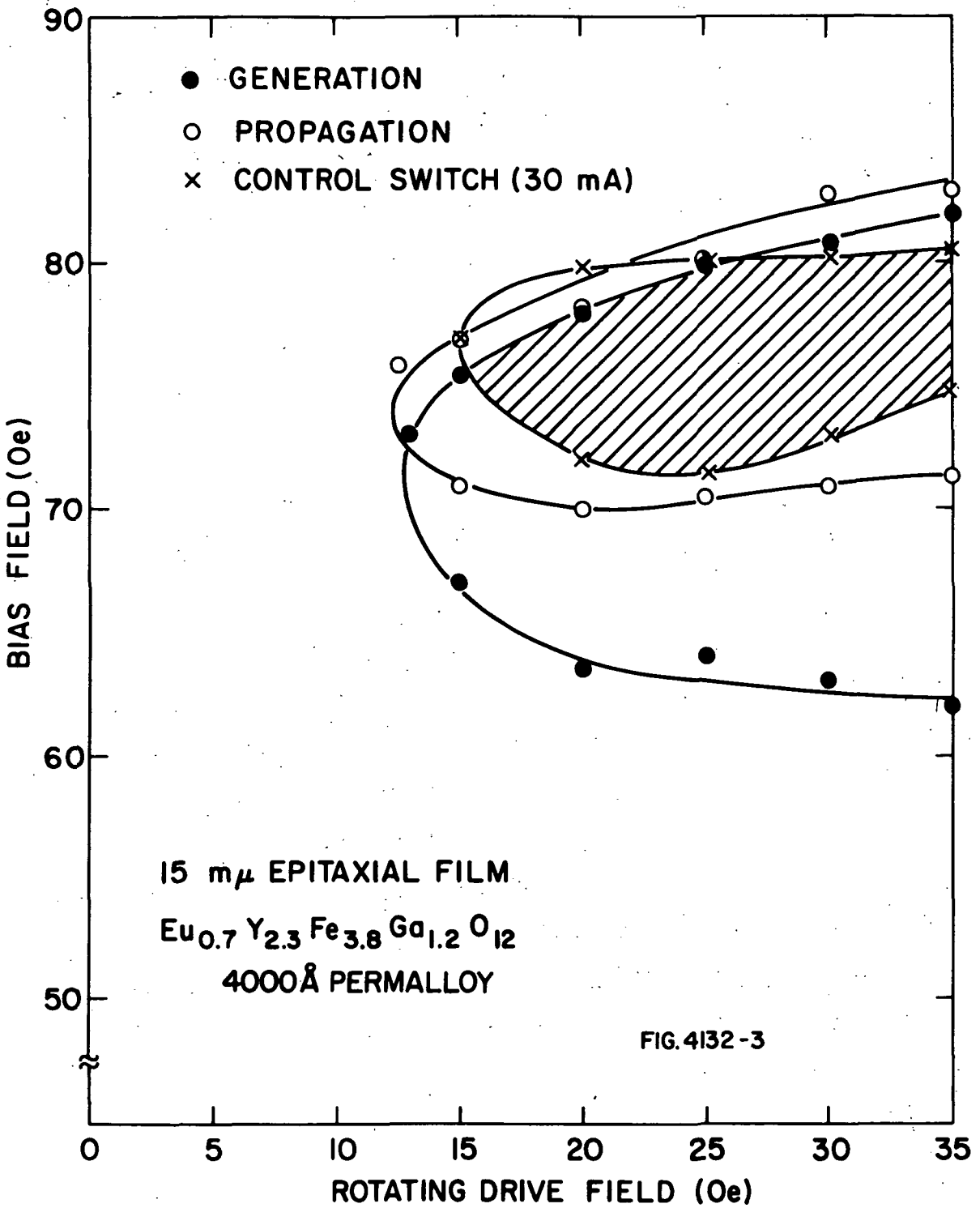

Fig. 4B2-3 Operating Margins of Overlay Design IV

4B3 DATA EVALUATION AND COMMENTS ON THE EXPERIMENTS

The first part of this section discusses the significance of the feasibility model test results. The second part of this section is devoted to some general insights gained during the course of the experiments.

4B3-1 Significance of the test results

The operating margin data of Fig. 4B2-3 show that a bubble domain memory chip with 7.5 μm line technology and 11 μm bubbles can be made fully operational for rotating fields $\leq$15 Oe and control currents $\leq$25-30 mA. Furthermore, individual function operation has been obtained for values as low as 4 Oe for straight-line propagation, 5 Oe for cornering, 6 Oe for generation, 6 Oe for annihilation, and 12 mA for decoder switch operation. Thus it seems quite certain that with further good design engineering, the 15-Oe, 30 mA operating point can be made to be in the center of the operating region rather than at its edge, as it is now in Fig. 4B2-3.

What does this imply for the operation of a memory chip with 2.5 um line technology and 4 μm bubbles? If all the dimensions of the overlay are scaled down by a factor of 3, and the magnetization M_s and the coersive field H_c of the 4-μm bubble material remained unchanged, then the rotating field amplitude would remain at 15 Oe and the control currents would be reduced from 30 down to 10 mA. Since the power estimates of Table 3B3-2 were based on a 10 Oe rotating field, the total average power during a read cycle would be increased from 22 up to 30 watts if a 15 Oe rotating field were required.

Actually, $4\pi M_s$ in a 4 μm bubble material will most likely be somewhat higher than the 125 gauss value used in the feasibility model. This comes about because the bubble diameter is proportional to $\sqrt{AK}/M^2_s$, where A is

the bubble material's exchange energy and K is its uniaxial anisotropy energy [T70]. It can be seen that a 3X reduction in bubble diameter requires a $\sqrt{3}$ X increase in M_s or a 9X decrease in K. However, the ratio $\sqrt{K}/M_s$ must remain sufficiently large to insure stable bubbles [GSTV69]. (A is not easily changed). For this reason, $4\pi M_s$ will probably be ~200 gauss, which seems to be borne out by the 4 um bubble experiments and predictions reported so far in the literature. [AHPRS 71, B71, SSC 71].

However, it is not $4\pi M_s$ but the coercive field H_c which determines the required rotating field amplitude of a given overlay design. Therefore, if M_s is increased without increasing H_c, the drive field required remains constant. The theory of coercivity in bubble materials is not well established, but experimental evidence both in our laboratory and in the literature seems to suggest a relation between H_c and crystalline perfection, and no strong dependence of H_c on M_s in the range of interest. Therefore, a 3X reduced feasibility model overlay in conjunction with a 4 μm bubble material having H_c = 1 Oe should operate for 15 Oe rotating field and 10 mA control current. It seems reasonable to predict sufficient progress in materials growth and overlay design over the next year or two to make 10 Oe rotating field and 10 mA control current realistic final values.

Approaches for improved materials are beyond the scope of this report. However, some avenues toward improved overlay design are discussed in the next section.

4B3-2 Comments on the Experiments

The operating margin plot of Fig. 4B2-3 shows a bias field margin of 76 Oe ± 5% at 25 Oe drive field. For an ideal isolated bubble domain, the

bias field can be varied about a midpoint by ± 18% before either collapse or runout occurs [T 70]. Thus, the margins of Fig. 4B2-3 represent a noteworthy accomplishment, but also indicate that further improvements in the overlay are possible. Hopefully, the comments in this section will be an aid in that direction.

Propagation Permalloy Thickness

In contrast to the tight bubble material thickness control implied necessary by the operating margins, the device operation was relatively insensitive to propagation permalloy thickness in the range 2000-6000 Å. For thicknesses below 2000 Å, there was a noticeable increase in the required drive field (the T-bars were evidently beginning to saturate), while for thicknesses above 6000 Å, some anomalous results were noted, such as bubbles being repelled by T-bars in the absence of in-plane field. In general, however, the minimum propagation fields were within 1 or 2 Oe of the ≈15 Oe values shown in Fig. 4B2-3 for 4000 Å-thick permalloy. Since the demagnetizing field for a 2000 Å-thick, 37.5 um-long bar is roughly 53 Oe, and 160 Oe for a similar 6000 Å-thick bar, the bar is far from saturation in this range of thicknesses, and the pole strength depends only on the drive field, a conclusion reached also by Copeland [C 72]. Overlay malfunctions were rarely cured by varying the permalloy thickness within this range.

Overlay Design

Unlike the permalloy thickness, the in-plane geometry was quite critical, as described already in Sec. 4B2. Through painful experience, we learned that to design a good overlay, one must pay attention to at least three and perhaps four magnetic pole patterns:

1.) Proper attractive pole pattern- this first step is obvious. Having decided on the path one wishes the bubble to follow, one designs the overlay so that there is a moving pattern of attractive poles to pull the bubbles along the desired path.

2.) Proper repelling pole pattern - this step is less obvious, and is not as noticeable in straight-line propagation as in corners. But the repelling poles play an important role in straight-line propagation, as can be verified by varying the amount by which an I-bar extends between two T-bars. It is the absence of a proper repelling pole in most corner designs which makes the drive field requirement higher for corners than for straight-line propagation.

3.) Improper attractive pole pattern - this seems obvious in retrospect, but a bubble does not know which of two attractive poles it was intended to go to, and so after the second design step above, one must examine the overlay very carefully to see if in addition to the desired attractive poles, the bubble will ever see along its path an approximately equi-distant pole of approximately the same length, or a more remote but stronger attractive pole than the one corresponding to the proper path. In particular, this was the fault of Design II, although even Design IV needed some fine adjustments in the switch configuration before this problem was overcome.

4.) Improper repelling pole pattern - we found this effect to be the most subtle and the most difficult to anticipate. In particular, this led to the re-designed Y-bar turn leading from the write decoder to the storage loop of Design IV.

Going through this four-step checking procedure of a prospective overlay design significantly increases its chances of successful operation.

Intermittent Errors.

Although the feasibility model will perform reliably for periods $\sim 10^5$ rotations, malfunctions can be observed occasionally, especially near the edges of the operating region. Most of the errors caused by faulty overlay design have been eliminated, and the main problem remaining is one of bubble-bubble interaction. The main effects of this interaction are failures in the control switches and bubble collapse in the propagation path when a steady stream of bubbles is being processed.

This problem could be alleviated by further reducing the packing density through an overlay design change, but is is believed that the proper approach is to decrease the interaction by using shorter bubbles (smaller height-to-diameter ratios than the present 15:12) and to decrease the tendency to collapse by further reducing the bubble coercivity H_c. This is one of the conclusions reached by comparing platelets and films, as discussed below.

Platelets vs. Films

The practical advantages of epitaxial films vs. bulk-grown crystal platelets have already been discussed. The platelets are hard to handle, have tall bubbles which are difficult to annihilate, and exhibit strong sensitivity to temperature and in-plane field. However, not all aspects of overlay operation are improved by using an epitaxial film. In particular, straight-line propagation, the least troublesome function with platelets, was much more tricky with films, and required the use of "half-width" 3.8 μm gaps to prevent bubble collapse in the middle of the straight-line propagation

tracks. This result was quite puzzling until it was realized that although the coercivity of both film and platelet was $\approx$1 Oe, the film $4\pi M_s$ was only 125 gauss vs. 200 gauss for the platelet, which brought home in a very real way the point that $H_c/4\pi M_s$ must be less than 1% for satisfactory device operation [B71]. Films with coercivity $\approx$2 Oe would fail even with the modified overlay.

The question of bubble height also enters into sensing, as discussed below.

Sensing

Sensor optimization played a secondary role vs. obtaining a fully operational chip. Nevertheless, valuable information about sensing was obtained. Past experience [AKLT 70] indicated that for best results, the sensor center should not be more than d/4 away from the edge of a bubble of diameter d, and the sensor diameter should be $\approx$3/4 d to d. Also, when the bubble is at the sensor, the bubble field and the rotating field acting on the sensor should be at 90° to each other.

These rules were followed in designing and placing the sensor of Fig. 4A1-3. The signal was $\approx$200 μV at 2 mA input for the epitaxial film and approximately twice that much for the platelet (both bubble diameters $\approx$12 μm). This compares quite favorably with the 110 μV/1 mA obtained for a 5 μ bubble stretched 3X for sensing [SSC 71].

The larger sense signal from the platelet is due partly to the larger magnetization and partly to the fact that the stray fields from a tall bubble extend farther up. This last effect enters into the choice of bubble height (i.e., film thickness), as discussed next.

Choice of Bubble Height

Tall bubbles give better signals but have stronger interactions and are difficult to annihilate. Shorter bubbles have smaller signals, and when the height-to-diameter ratio, h/d, goes below 0.5, it is difficult to generate and propagate at the same bias field, because $4\pi M_s$ must also be decreased to keep d constant, and thus $H_c/4\pi M_s$ increases. A reasonable compromise seems to be a h/d somewhat less than the 1.25 value of the feasibility model, but greater than the optimum packing density of value of 0.5 [T 70]; i.e., h/d should be $\approx$3/4 to 1. This seems to agree with the recent thinking of other workers in the field [B71-III].

SECTION 5: SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS

Summary

The first part of this report concerned a high reliability, low power, 10^8-bit Bubble Domain Mass Storage Unit for Space applications. A particular design approach, that of using on-chip magnetic decoding, was carried all the way through to a complete conceptual design, including magnetic, electrical, mechanical, and reliability aspects of the chip, module, page, and completed memory assembly. The final design assumed 4 μm-diameter bubbles and 2.5 μm-linewidth photolithographic technology to achieve a memory weighing 27 lbs and having a maximum data rate of 6.4×10^6 bits/sec with 200 μ sec access time to an 800-word block and an additional 4 m sec (average) to a particular word within that block. Assuming a 10 Oe rotating drive field and 10 mA on-chip control switch currents, the average power dissipation was calculated to be 22 watts.

The second part of this report describes the fabrication and operation of a 64-bit memory chip designed to demonstrate the feasibility of the conceptual design approach. Using 12 μm bubbles and 7.5-μm linewidth technology, full simultaneous operation of the chip's four shift registers and their sense, decode, and other control functions was obtained for a minimum rotating drive field of 15 Oe and a control current of 30 mA. Using a reasonable scaling rationale, this projects to 15 Oe and 10 mA for the conceptual design.

Conclusions

Early in the conceptual design process it became apparent that the design objective of several tens of watts total power could not be met while circulating all the bubbles all the time. Furthermore, even if the bubble

devices had negligible failure rates, the finite failure rates and large numbers of support circuits needed for such a large memory made at least a Hamming-type single error correction/double error detection (SEC/DED) coding scheme mandatory in achieving reasonable memory reliability. Tradeoff studies show that the highest reliability and lowest power dissipation is obtained when the memory is organized on a bit-per-chip basis, and the stored information is encoded into a 16-adjacent-bit single error correcting/double error detecting (SbEC/DbED) code. The price is that there are 32 check bits vs. 64 data bits in a memory word.

From the work on the feasibility model, it is concluded that a valid fabrication procedure capable of manufacturing the conceptual design chip has been demonstrated, and that the assumption of 10 mA control currents in the conceptual design has been justified. If the rotating drive field remains at 15 Oe, the power estimate will have to be increased by about 30%. However, further bubble device design engineering may well reduce the drive field below 10 Oe.

Although the feasibility model is a noteworthy accomplishment, one should not overlook that the narrow ($\pm$ 5%) operating margin implies rather stringent control over the epitaxial film characteristics. Even for the theoretical margins of $\pm$ 18%, Bobeck [B71-III] predicted that both magnetization M_s and thickness t would have to be controlled to within $\pm$ 1% over the active area of a chip as well as from one chip to the next. With sorting, using perhaps three slightly different permanent magnetic packages, these requirements can probably be relaxed to $\pm$ 2% for t and $\pm$ 2 1/2% for M over the chip and $\pm$6% for t and $\pm$7 1/2% for M over a wafer and from wafer to wafer. Nevertheless, this implies that the Ga concentration over the area

of one chip can vary only in the third decimal place, for example. In other words, the degree of care required in manufacturing these chips should not be underestimated.

The other implication of the narrowness of even the theoretical margins is that it may be necessary to provide some temperature tracking of the bias field with the permanent magnets if the memory is to be used over a wide temperature range.

Finally, it is concluded that although much was accomplished, much also remains to be done. Some specific areas requiring more work are outlined in the next section.

Recommendations

The significance of the operating margins was just discussed. In view of this, more work should be done on device design to improve these margins, particularly since memories for space applications are apt to be subjected to wider environmental variations than commercial machines. It is suggested that this work be conducted using 12 μm bubbles and 7.5 μm linewidths, as in the Feasibility Model. A valuable body of knowledge and experience has been accumulated both in the fabrication and operation of such devices, and so this approach should give important information for a minimum investment of time and money. Furthermore, both the 4 μm bubble material and the 2.5 μm-linewidth overlay of the conceptual design will probably be made by the same process used for the feasibility model, and so the further experience should be readily transferable.

In conjunction with the margin work, there should be a thorough study of the overall temperature sensitivity of a bubble memory. The work reported here showed a path toward decreased temperature sensitivity of the

bubble material through the use of specific liquid-phase epitaxial garnet films, but a more detailed investigation is needed. This should include a study of the temperature characteristics of permanent magnet materials and possible ways in which these can be used to compensate the temperature sensitivity of the bubble material.

Still considering environmental effects, there should be a study of possible special passivation requirements for space applications, as well as radiation effects on bubble memories and possible requirements for shielding beyond that provided by the permanent-bias package itself.

There is a great need for statistically valid failure rates and failure mode studies on bubble domain devices to allow reliability calculations to be made. Such work should definitely be done, perhaps in conjunction with accelerated aging tests.

Much work remains to be done on sensing, both for commercial and for space applications, and it may well be that the noise environment and hence the signal requirements will be different in space. This should be investigated.

A much wider range of tradeoffs is open to investigation than was done here. The approach here was to stick to basically one chip design, one module design, and one page design, and vary the way in which information was assigned and thus vary the memory system. In addition to removing these constraints, other chip organizations should be considered as well. In all of these tradeoff studies, the reliability modeling procedure of the present work should be applicable and should yield valuable comparisons.

A number of other work areas suggest themselves. More detailed electronic design and thermal analysis are needed. The proposed interconnection

approaches need more thorough examination. The coil assembly supplying the rotating in-plane field can certainly be improved. More component economy may be possible in the error correction circuitry.

There should, of course, be further hardware experimentations to backup the studies described. For example, additional small scale chips would be desirable to experimentally verify the margins and temperature sensitivity studies. The next major hardware milestone would be to build a complete chip (10^5 bits) and temperature test and evaluate it. Once the chip design is proven, a cross section of a 10^8 bit mass storage unit would follow. The cross-section would be electrically identical to a complete 10^8 bit storage unit, but would only require a small percentage of the total memory to be operable. The cross sectional model would provide the opportunity to optimize and verify the electronic circuit designs, i.e. the sense amplifiers, drivers, coil, resonators and drivers, permanent magnet bias fields, etc.

It would also be a good vehicle for environmental performance evaluation. Once the magnetic and electrical designs are proven by successful performance of a cross-section, a full 10^8 bit mass storage unit breadboard would follow with all bits operating, and a full complement of error detection and correction circuitry.

It can be seen that although this study has answered many questions simply by carrying through a self-consistent design and examining its ramifications, there are still many questions to be answered. The final operating design may or may not resemble the present design, but at least there now exists a point of departure. The above list of additional work topics is not all-inclusive, and the reader may well spot some additional ones. However, it is felt very strongly that the first two topics, margins and temperature sensitivity, are of initial concern and therefore deserve a high priority.

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217-218

APPENDIX A

CHIP YIELD ANALYSIS*

It is first assumed that the yield of chips will be limited by defects in the photolithographic masks, rather than by defects in the bubble domain material. At the end of the calculation, this assumption will be checked for self-consistency.

Following the treatment in "Yield Degradation of Integrated Circuits Due to Spot Defects", by Yanagawa [Y72], the mask-limited yield for a bubble domain chip is

$$Y = \exp - (D_b A_b + D_c A_c + D_s A_s) \qquad (A1)$$

where D_b = defect density in permalloy overlay bars (T, I, or Y)

D_c = " " " conductor

D_s = " " " sensor

A_b = permalloy bar susceptible area

A_c = conductor " "

A_s = sensor " "

These quantities are calculated as follows: the linewidth W of bars, conductors, and sensors is assumed to be 0.0001"(2.5μm). The defect size tolerances for the permalloy bars, conductors, and sensors are assumed to be respectively $W/2$, $W/4$, and $W/4$. (This is consistent with our experimental observations.) Critchlow, et al., found that in certain prescribed regions of interest, the density of defects with diameter X in a unit area was distributed as $\frac{\alpha}{X^3}$, i.e., the smaller the defects, the more of them there were. For values of $X < 4 \times 10^{-4}$ inches (10μm), α is about $\frac{1}{2} \times 10^{-6}$. Hence, D_b is found from

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* The first pass of this analysis was performed by Dr. Y. S. Lin

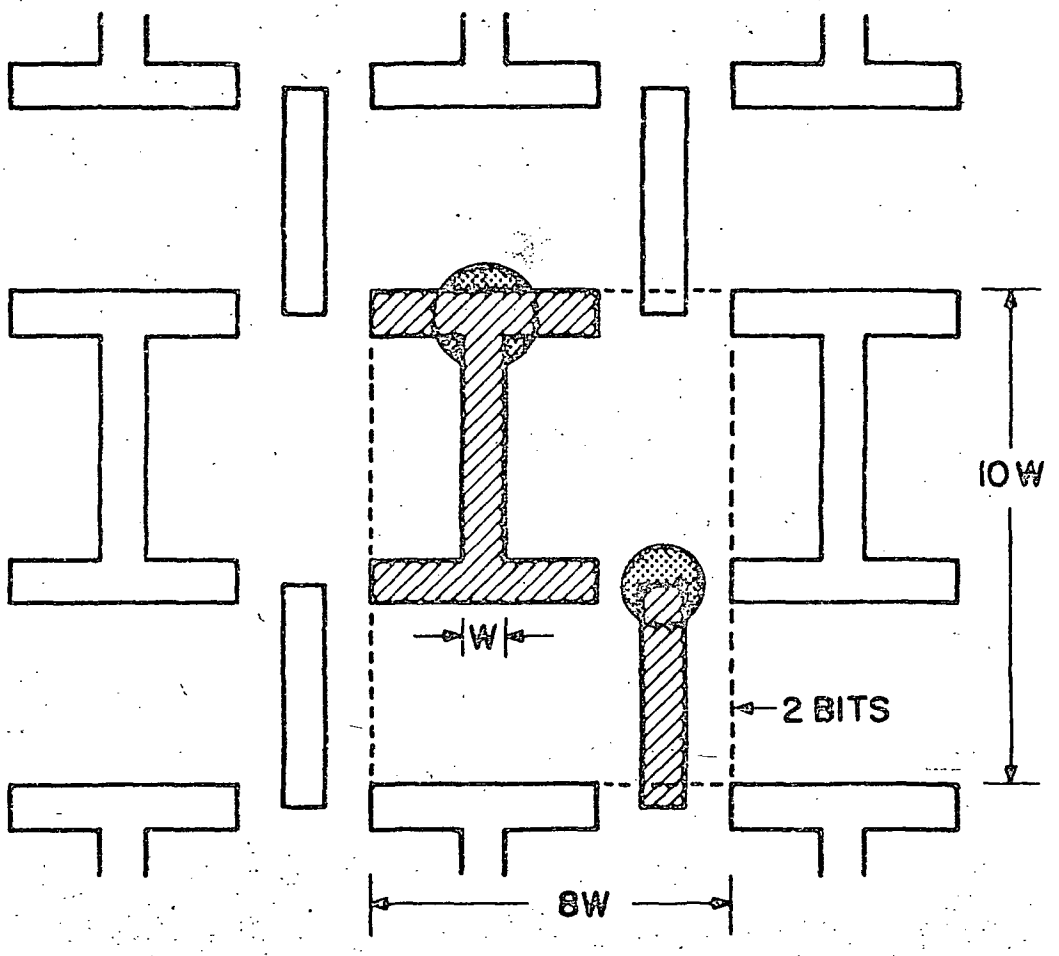

Fig. A1 Permalloy Area of Shift Register Cell
(Cell dimensions: height = 5w, width = 8w)

$$D_b = \int_{x_1}^{x2} \frac{\alpha}{x^3}\, dx = -\frac{\alpha}{2x^2} \Bigg|_{x = 5 \times 10^{-5} \text{ inch}}^{x = 4 \times 10^{-4} \text{ inch}}$$

D_b = 100/square inch (= 16/sq. cm)

Similarly D_c = 400/square inch

D_s = 400/square inch

To obtain expression for A_b, A_c, and A_s, one must know something about the chip layout. A typical section of shift register storage area (permalloy overlay only) is shown in Fig. A1. It can be seen that a bit of information occupies an area of 40 W^2, of which 10 W^2 or 25% is covered by permalloy. Assuming that these conditions hold all over the chip, $A_b = 1/4\ L_1L_2$ where L_1L_2 is the area of a chip with edges of length L_1 and L_2.

The vulnerable conductor area Ac for the chip of Section 3A2 is approximately 10 WL_1 x 2, and as long as 20 $W << \frac{L_2}{4}$, i.e., as long as the chip edge is >> .008", A_c will be negligible compared to Ab, and even 1/4 Ab.

A_s can similarly be shown to be negligible compared to 1/4 Ab, in which case equation (A1) becomes simply

$$Y = \exp(-D_bA_b) = \exp(-25\ L_1L_2)$$

Thus for a chip area L_1L_2 = .2" x .2" = .04 inch^2, Y will be exp(-1) = 0.37. This area should be the approximate target of the chip design.

Since the effective defect density in permalloy bars was found to be 100/square inch and the reported defect densities in epitaxial garnet films are less than 30/square inch [N71], the assumption of mask-limited yield is seen to be justified.

It should be pointed out that Bobeck [B71] arrived at similar conclusions regarding defect densities, chip capacities, and chip yields.

APPENDIX B*
MODULE DESIGN

As described in Section 3A2.5, sixteen memory chips are placed on a planar substrate which is then supplied with a pair of coils to provide a uniform rotating in-plane drive field for all 16 chips. The result is a module with 1.6×10^6 bit storage capacity. Designing this module is thus largely a problem in coil design. This appendix explains the considerations that went into this design.

The coils may consist of wire wound around the substrate, as shown in Fig. 3A2.3, or they may be fabricated by printed-circuit techniques. The final product would probably go beyond Fig. 3A2.3 by one step: an encapsulation in epoxy or the like after the winding of the coils. This would provide passivation as well as strength. Otherwise, the strength of the module comes entirely from the chip-carrying substrate, which should be as thin as possible to minimize coil inductance.

For purposes of calculation, one of the two coils is represented in Fig. B1 as being comprised of a series of striplines, i.e., a flattened solenoid made up of ribbon-like conductors. Such a coil may be made by printed-circuit techniques as well as the more conventional wire-winding approach.

Three things are important in the coil design: the power dissipated, the L/R time constant, and the impedance. It is desired to 1) provide $\sim$ 10 Oe (800 A/m) rotating field for a minimum amount of power, 2) to be able to stop and start this rotating field in a small fraction of the rotational period, and 3) to supply this field at current and impedance levels which are consistent with semiconductor driving circuits.

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* MKS units are used unless otherwise specified.

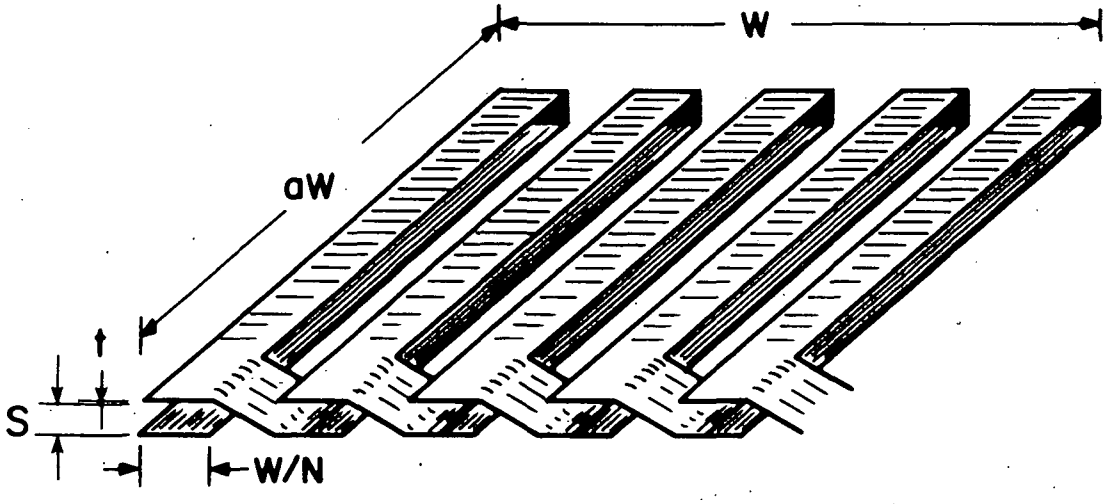

Fig. B1 Coil Used for Calculations

From Ampere's circuital law ($\oint H \cdot dl = I$), the field H inside the coils can be shown to be approximately

$$H = \frac{NI}{W} \tag{B1}$$

where N is the number of turns, I is the input current, and W is the edge dimension of the coil (Fig. B1) (It is assumed that the coil clearance $s \ll$ the coil edge W).

The resistance R of the coil is

$$R = \rho \frac{\ell}{A} = \rho a \frac{2WN}{t(W/N)} = 2a \frac{\rho N^2}{t} \tag{B2}$$

where ρ is the resistivity of the coil windings, t is their thickness, and aW is the breech-edge dimension of the coil (Fig. B1). For a square coil, $a = 1$.

The power P dissipated in the coil is simply I^2R, and by combining this with (B1) and (B2), one obtains

$$P = H^2W^2a \left(\frac{2\rho}{t} \right) . \tag{B3}$$

In other words, for a given coils size (aW^2), a given field H is obtained for minimum power (condition #1) by minimizing the conductor resistivity and maximizing the conductor thickness. This is not surprising. Note, however, that (B3) does not contain N, the number of windings.

The inductance L is given by

$$L = N \frac{\phi}{I} = \frac{N}{I} \left(\mu_o \frac{NI}{W} \right) aWs = aN^2 \mu_o S \qquad \text{(B4)}$$

where μ_o is the permittivity of free space ($\mu_o = 4\pi \times 10^{-7}$ henry/meter) and s is the clearance inside the coils. The L/R time constant of the coils is found from (B4) and (B2) to be

$$\frac{L}{R} = \frac{\mu_o st}{2\rho} . \qquad \text{(B5)}$$

This quantity must be small ($\leq$) compared to $\frac{1}{f_{max}}$, the rotational period (condition #2), unless special circuitry is used to turn the field on and off [G71]. Note that (B5) is independent of both the extent of the coil (aW^2) and also the number of turns N. An adequately small L/R can be obtained only by keeping the coil clearance s (and thus the module thickness) small, the conductor thickness t small, and the resistivity large. Note that the last two approaches are the opposite of what is required for low power.

From the standpoint of the semiconductor circuit supplying the coil current, it is desirable (although not essential) that the load voltage be $\sim$ 5V, and that the load current be $\lesssim$ 1A. Smaller voltages result in poor regulation efficiency, larger voltages require proportionately larger supply voltages, and larger currents require heavy-duty, high-current transistors.

As long as $2\pi f_{max} L \lesssim R$, the load voltage will not be much larger than IR. Using (B1) and (B2), this condition becomes

$$IR = 5$$

$$K \left(\frac{HW}{N}\right) \left(2 \rho a \frac{N^2}{t}\right) = 5$$

where K is the number of coils to be driven in series. Rearrangement gives

$$N = \frac{5}{aK(HW)\frac{2\rho}{t}} \quad . \tag{B6}$$

At this point there is an interaction between the coil design and the reliability analysis and physical limitations on the module. First, the reliability considerations: intuition may dictate that the most reliable design would be the one with the fewest semiconductor circuits, and that therefore the more coils sharing one driver, the better. This turns out not to be true, because adequate reliability for such a large memory can be obtained only by error correction coding, and a single coil driver failure would play havoc with the error correction coding because it would cause simultaneous errors in a large number of bits in a memory word. The analysis of Section 3B2 shows that a system with one driver per coil has better reliability, even though the circuit count is higher, because the admittedly higher failure rate is nevertheless made up of events each of which can be handled by the error correction circuits. So we choose K=1 in Eq. (B6).

But then what we have really done with our current and voltage specifications is to say that we do not want to dissipate more than 5 watts in one coil, which sets a limit on the extent of the coil (and therefore of the module) through Eq. (B3):

$$W^2 < \frac{5}{H^2 \left(\frac{2\rho}{t}\right)} \tag{B7}$$

We are now in a position to choose numerical values for the coil parameters W, N, S, ρ, and t.

The "sheet resistance" ρ/t of the windings requires a compromise. Equation (B3) shows that for minimum power per unit area for a given magnetic field, ρ/t should be minimized. However, this tends to maximize the time constant L/R, as shown by Eq. (B5). Since low power is considered more important in this application than high speed, $2\rho/t$ will be maximized: copper ($\rho = 1.7 \times 10^{-8}$ ohm-m) will be picked for the conductor, and the thickness t will be as large as possible consistent with skin depth and other considerations.

At this point, the operating frequency must be decided upon. Mobility limitations in the bubble material preclude operation much above 1MHz. However, even 1 MHz is too high a frequency to satisfy the design conditions specified here: at 1MHz, the skin depth in copper is 66μm, and so the maximum practical thickness t is twice this, or 132 μm (about .005") This minimizes the power dissipation, but results in too high an L/R ratio: The module and the substrate for the epitaxial gamet film must each have a thickness of at least 0.2 mm for simple mechanical reasons. Thus s, the clearance inside the coils, must be at least 0.5 mm. Then, from Eq. (B5),

$$L/R = \frac{4\pi \times 10^{-7} \times 4 \times 10^{-4} \times 132 \times 10^{-6}}{2 \times 1.7 \times 10^{-8}} = 2. \times 10^{-6} \text{ sec},$$

which is too large compared to the rotational period of 10^{-6} sec at 1 MHz.

However, adequate data rate and access time can still be obtained for 100 KHz operation. The skin depth is increased by $\sqrt{10}$, hence the maximum L/R is increased by $\sqrt{10}$ to 6.4×10^{-6} sec. However, this is still acceptable compared to the new rotational period of 10^{-5}sec at 100 KHz.

The maximum allowable module size can now be found from Eq. (B7):

for H = 10 Oe = 800 A/m, $\rho = 1.7 \times 10^{-8}$ Ω-m, and t = .42mm, W <9.7 cm.

Other considerations lead one to a somewhat smaller module: as shown in Appendix A, yield considerations indicate a chip size of approximately 0.5 cm x 0.5 cm, which would mean about 64 chips per module. This number is somewhat too large; it requires too many connections per module (See Sec. 3A3), begins to raise module yield problems, and severely limits the designer's flexibility in organizing the memory, since each module contains 1/16th of the memory's information storage capacity. The bricks are too big.

For these and other reasons, the final module active area was chosen to be 4.5 cm x 4.5 cm, holding 16 chips. The number of turns and thickness of conductor are then specified by Eq. (B6) as

$$N/t = \frac{5}{2HW\rho a} = \frac{5}{2(36)\ 1.7\times10^{-8} \times 1.44} = 2.84 \times 10^{6}\ m^{-1} \qquad (B8)$$

Before substituting the twice-skin depth value of .42mm for t, we specify that the conductor will not be thicker than it is wide, i.e.,

$$t \leq \frac{W}{N} \qquad (B9)$$

(We limit our considerations to single-layer coils, since in eventual manufacture they will probably be made by printed-circuit or photolithographic techniques) Combining (B9) and (B8) gives

$$t \leq \sqrt{\frac{W}{2.84 \times 10^{6}}}$$

$$t \leq 126\ \mu m$$

$$N = 356 \text{ turns}$$

The final coil design is a slight variant on the foregoing numbers, and is summarized in Table B1.

TABLE B1

FINAL MODULE COIL DESIGN

aW x W	(Coil Dimensions)*	6.5 cm x 4.5 cm
S	(Clearance Inside Coils)	.04 cm
ρ	(Winding Conductivity)	1.7×10^{-8} ohm-m
t	(Conductor Thickness)	125μm (.005")
N	(Number of Turns)	360
P	(RMS Power per Module)	0.52 watt
H	(Field Strength)	800 A/m (10 Oe)
I	(Input Current)	0.1A
R	(Resistance)	52 ohms
L	(Inductance)	9.3×10^{-5} henry
L/R	(Time Constant)	1.8×10^{-6} sec
f	(Operating Frequency)	100 KHz
$R + j2\pi fL$	(Impedance at 100 KHz)	(52 + j58) ohms
V(0)	(dc load voltage)	5.2 V
$V(10^5)$	(Peak Voltage at 100KHz)	7.9 V

* See Fig. 3A2-3 or 3A3-10

APPENDIX C*

COMPACT DECODER FOR BUBBLE DOMAIN MEMORIES

and

REDUNDANCY APPROACHES IN BUBBLE DOMAIN MEMORIES**

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* The material in this appendix is also being submitted separately to NASA as a New Technology Report.

** Prepared with the Help of Mr. S. E. Schuster.

IBM Federal Systems Division
Space Systems Center,
Huntsville, Alabama

Reportable Item: 26671-002
IBM No.: 72W-00003
Contract No.: NAS8-26671
Originators: G. S. Almasi
G. E. Keefe

NEW TECHNOLOGY REPORT

Compact Decoder for Bubble Domain Memories

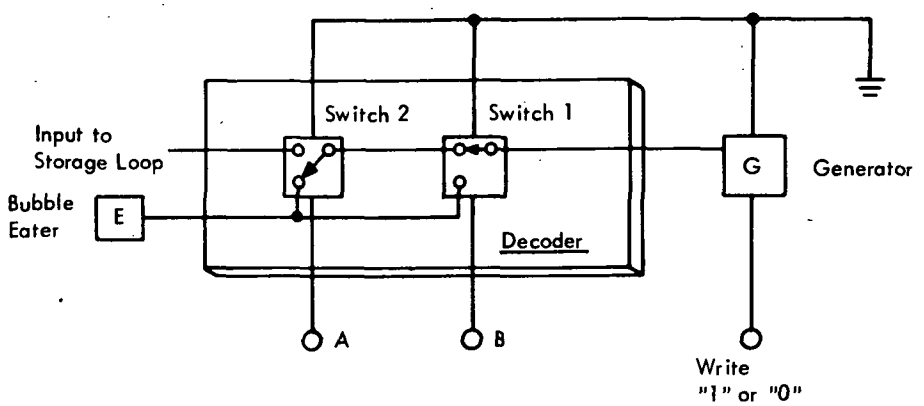

Fig. C1 Conventional Write Section of Bubble Domain Decoder

The Problem: As with semiconductor memories, early bubble-domain memories used 2n decode lines to select one of 2^n shift registers. This arrangement requires much area on an integrated circuit chip committed to shift register selection.

The Solution: Use an arrangement of complementary single pole-double throw (SPDT) switches at the control line crossing with each shift register.

How It's Done: A block diagram of a write section of a bubble-domain decoder is shown in Figure 1. It consists of two parallel bubble paths with a number of "bridges" where a bubble may cross from the upper path to the lower path. Each bridge has a current-carrying control line, which determines whether or not a bubble will cross over a bridge.

The memory design is so each shift register has a corresponding current-controlled bubble generator as shown in Figure 2. The control lines of all the generators are wired in series to produce a single write line. Depending on the binary input to this write line, one of two things happens during each field rotation. Either all the generators emit a bubble or none do. A "one" is written into the single shift register chosen from the 2^n shift registers by having all 2^n generators emit a bubble and then steering 2^n-1 bubbles into bubble annihilators (eaters).

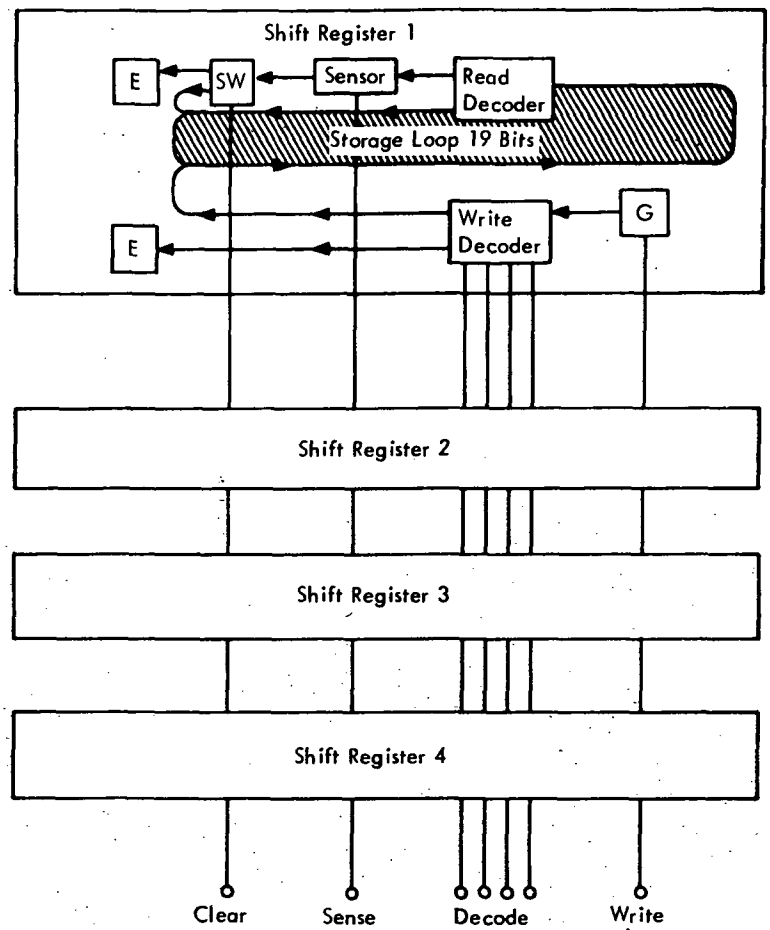

Fig. C2 Block Diagram of a Memory Chip

The decoder section of Figure 1 is used for this purpose by connecting the generator to the upper path input and connecting the bubble eater to the lower path output. The upper path output leads to the storage loop of the shift register. The bubble starts traveling from the generator, along the upper path, but it must pass every bridge without being shunted to the lower path in order to emerge into the storage loop. This happens in only one of the 2^n shift registers. The read decoder functions in an analogous manner, as shown in Figure 2.

NEW TECHNOLOGY REPORT Reportable Item: 26671-002

The details of the switch shown in the block diagram of Figure 1 are shown in Figure 3. Bubble location 1 is a point of ambiguity in that the absence of current in the control line, the bubble is not sure whether to proceed to location 2' or 2". A positive current, i.e., in the direction shown, steers the bubble to 2" and on to the lower path. This type of switch is designated SW-1 and is shown in symbol form in Figure 3. Using this notation the decoder of Figure 2 can be represented as shown in Figure 4, which is made up entirely of switches of the type SW-1 and each control line also has a complement line. The development of the SW-2 complementary switch eliminates the need for the N complement lines.

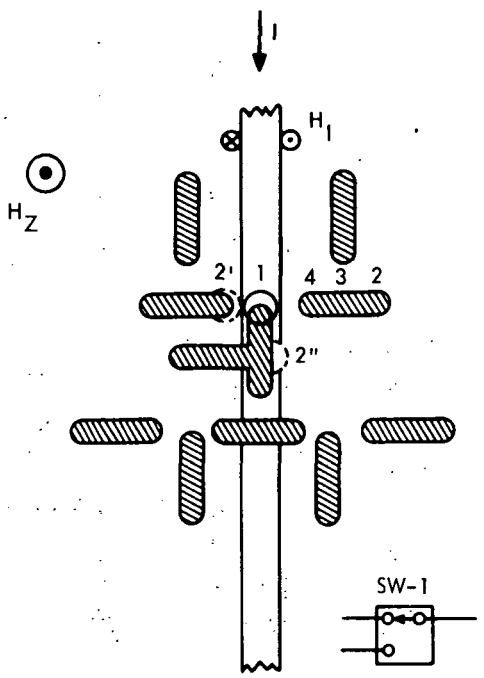

Fig. C3 Switch SW-1 Detail

The SW-2 switch is shown in Figure 5. Comparison with Figure 3 shows that the permalloy patterns are identical, but the control line conductor patterns are different. Now, a positive (downward) current pushes the bubble to the lower path, while a negative (upward) current leaves the bubble on the upward path. Thus, the switch of Figure 5 is the complement of the one shown in Figure 3 and is designated SW-2. Figure 6 shows a decoder which performs the identical function as the conventional decoder of Figure 4, but occupies only half the space. In addition, the decoder delay time is cut in half.

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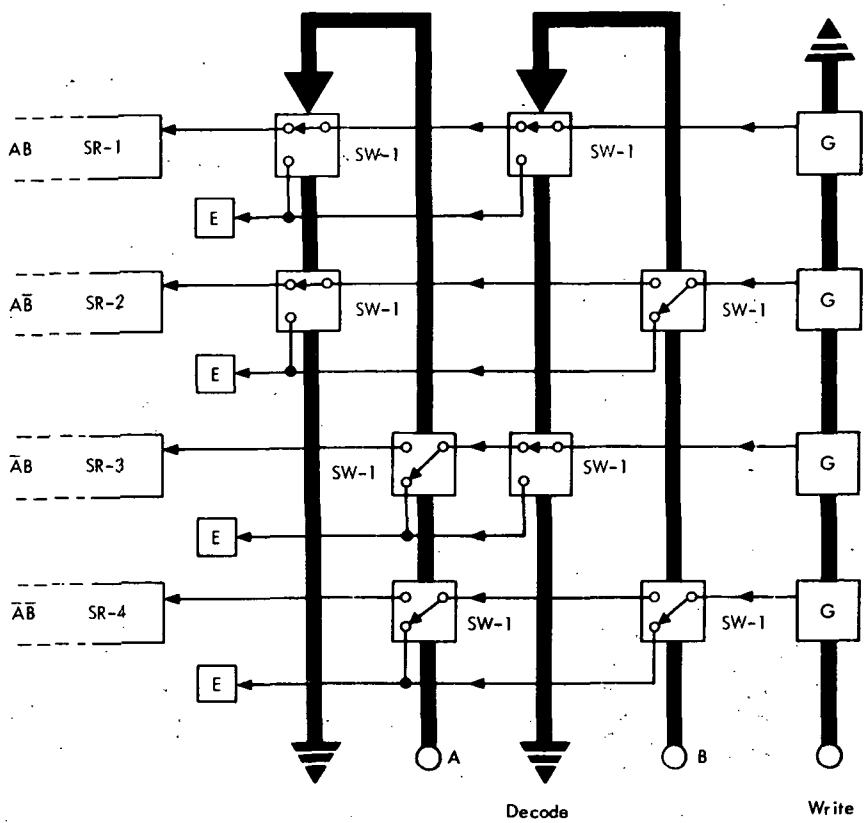

Fig. C4 Conventional Decoder

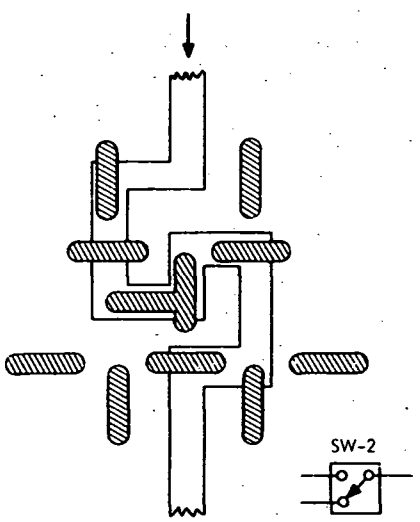

Fig. C5 Switch SW-2 Detail

NEW TECHNOLOGY REPORT Reportable Item: 26671-002

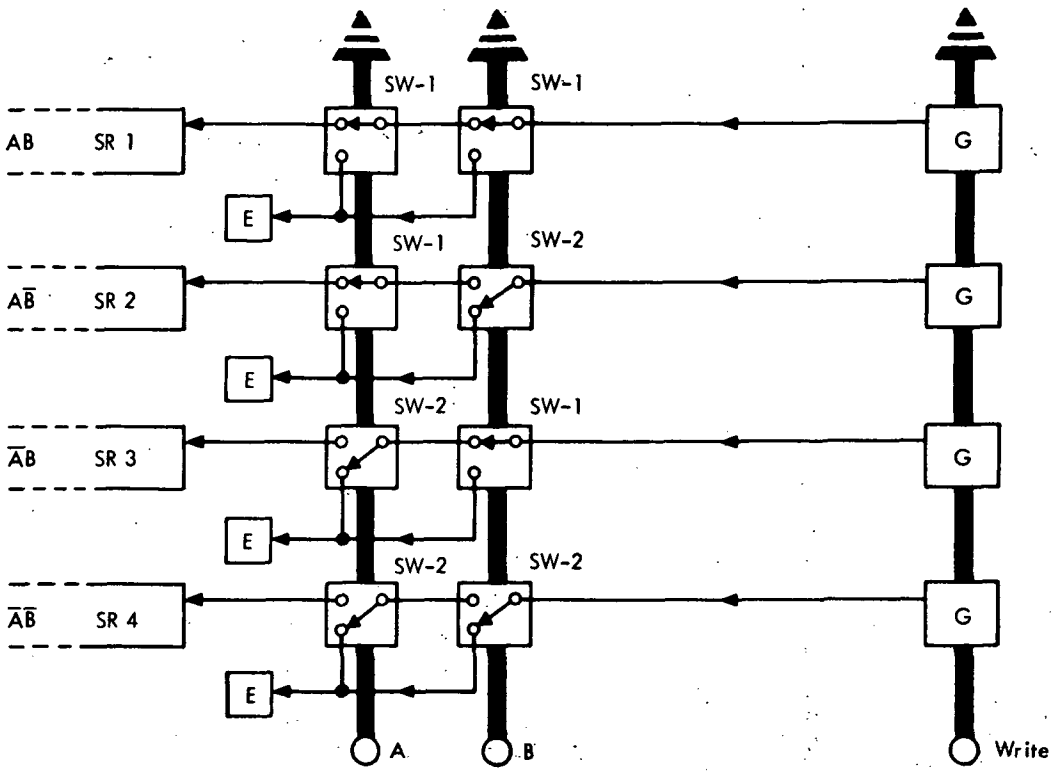

Fig. C6 Improved Compact Decoder

New Technology Representative Approval: 7 January 1972

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Reportable Item: 26671-003
IBM No.: 72W-00004
Contract No.: NAS8-26671
Originators: G. S. Almasi
S. E. Schuster

NEW TECHNOLOGY REPORT

Redundancy Approaches in Bubble Domain Memories

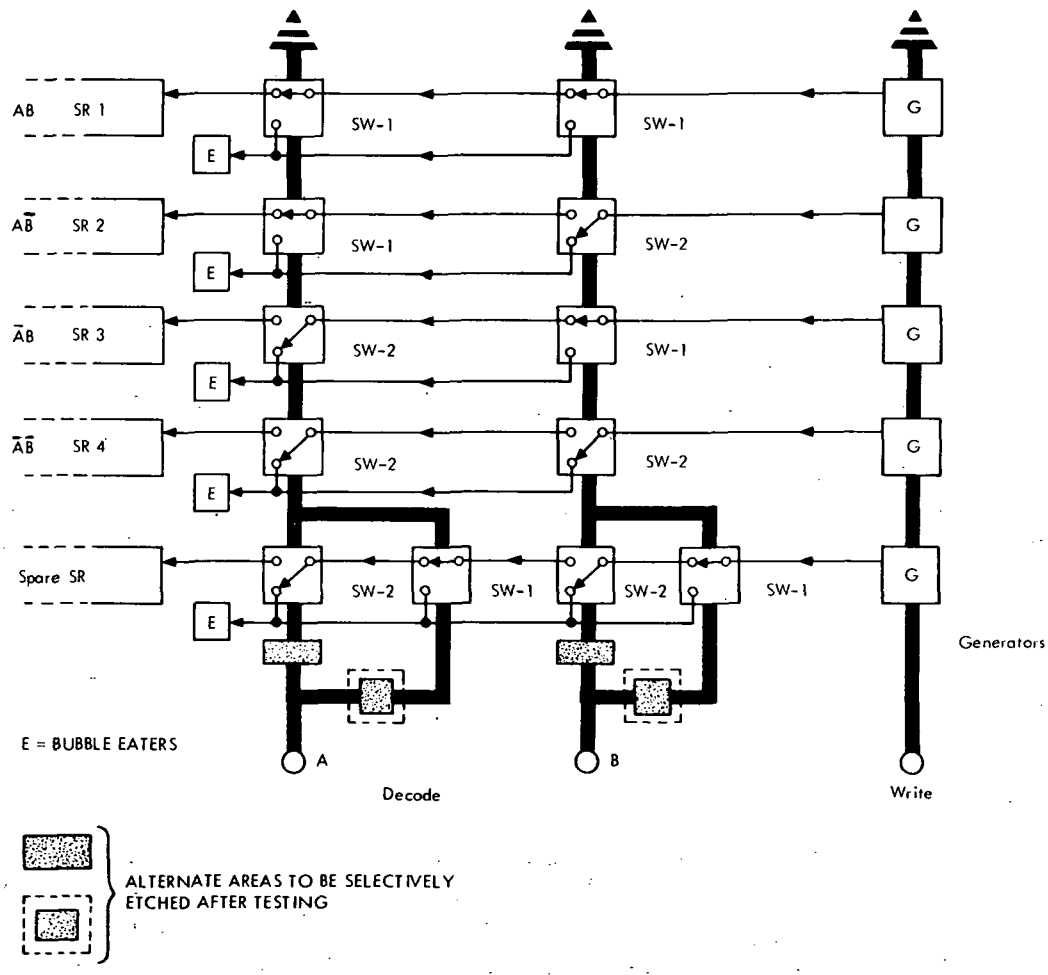


Fig. C7 Implementation of On-Chip Redundancy

NEW TECHNOLOGY REPORT

Reportable Item: 26671-003

The Problem: During the fabrication process of integrated circuit chips, errors or inconsistencies appear which render portions of the elements of the chip useless. With the fabrication of chips for a memory having a minimum number of storage elements, the faulty chips must be discarded or each chip must contain a number of excess memory elements and interface connections so that the excess elements can be used in lieu of the faulty elements.

The Solution: Use a method of redundancy where the makeup of each chip can be altered after fabrication to circumvent the faulty memory elements. This technique requires no additional interface connections and greatly reduces the number of excess or redundant elements formerly built into the chip.

How It's Done: A simplified block diagram of a bubble memory chip with redundancy is shown in Figure 1. Switch SW-1 is a "normally-upper-path" switch and SW-2 is a "normally-lower-path" switch.

The chip is tested after fabrication either electrically or visually. If all the regular shift registers, i.e., 1, 2, 3, and 4 in this case, perform correctly nothing more is done. The chip performs as a normal non-redundant chip with only four registers. No matter what combination of currents is applied to decode lines A and B, i.e., (++), (+-), (-+), or (--), the magnetic bubble from the redundant generator always goes to a bubble eater.

If one of the four shift registers or its associated decoder section is faulty, the redundant register is given the personality of the faulty register as follows:

- In the decoder section corresponding to the spare register, each decode line branches out to two lines which then rejoin each other again. During the personalizing process one branch of line "A" and one branch of line "B" is opened. Since the spare register can be switched in any one of four ways, the spare can be given the personality of any one of the four regular registers.

- The additional area per chip required for this capability is small because only the decoder is doubled in size. In a memory of 2^n shift registers of B bits each, the increase is:

$$\frac{(2n + \frac{B}{2})\ 2^{-n}}{(n + \frac{B}{2})} + \frac{n}{(\frac{B}{2} + n)} \approx \frac{n}{(\frac{B}{2} + n)}$$

NEW TECHNOLOGY REPORT Reportable Item: 26671-003

For example, a memory of 2^{16} shift registers (n=16) with 512 bits each (B=512), the increase in area is 1/17, or less than 10 percent. The line branches may be opened by selective etching, fusable links or laser beams.

New Technology Representative Approval: 7 January 1972

J. E. Morcom

APPENDIX D:

PERMANENT MAGNET BIAS FIELD PACKAGE FOR 10^8-BIT NASA MEMORY*

In order to prevent loss of stored information during a power failure, permanent magnets will be used to supply the bias field needed to operate the 10^8-bit NASA bubble domain memory. In Sec. 3A2 it is estimated that the modules making up the 10^8-bit memory would each have an area of $\approx$2.6" x 2.6". The preferred bit-per-chip design has up to 128 such modules. This is a total of 870 in^2 of module surface area, over which a uniform perpendicular bias field on the order of 50-100 Oe must be provided.

The permanent magnet structure should satisfy the following conditions:

1) Variations in field uniformity over the active area probably no more than 1%, otherwise operating margins will be significantly reduced.

2) Minimum weight, always important in space applications.

3) Maximum shielding against external fields and radiation.

4) Minimum external stray fields, to avoid interference with other spacecraft equipment in the vicinity of the memory.

5) Minimum amount of permanent magnetic materials; this comes about because magnetically "hard" materials are generally also physically hard and brittle, and thus more difficult to form than magnetically "soft" materials such as permalloy, which can easily be made into a foil or sheet and bent into desirable shapes. Permalloy is also cheaper.

---

*This appendix was prepared with the help of Dr. D. A. Thompson.

In general, field uniformity is obtained by minimizing fringing effects and using oversized magnet structures, as discussed in the contract proposal [IBM 70]. A detailed consideration of field uniformity will be deferred to a more thorough calculation in the future. This appendix concerns the remaining four conditions.

Several conclusions have been reached in arriving at a recommended design:

1) Problems with Original Design - The original permanent magnet structure in the contract proposal consisted of a long stack of alternating single modules and permanent magnet slabs, the stack being enclosed by a single yoke (Fig. D-1). This structure is poor from the standpoint of "volumetric efficiency", that is, it takes a large amount of permanent magnet material to produce a sufficiently uniform field over all the modules. Also, the yoke as shown in Fig. D-1 will tend to act as a magnetic short-circuit for the magnetomotive force of the permanent-magnetic slabs.

2) Somewhat Improved Planar Structure - The problems with the design of Fig. D-1 can be largely eliminated by going to a more planar structure, such as the one in Fig. D-2. This shows a sub-unit of 8 modules being served by one permanent magnet slab and surrounded by a permalloy yoke. This sub-unit could constitute a completely self-sufficient memory of $\approx 1.3 \times 10^7$ bits total storage capacity. The 10^8-bit information storage capacity of the complete memory is equivalent to eight such sub-units, not counting the storage capacity needed for error correction bits.

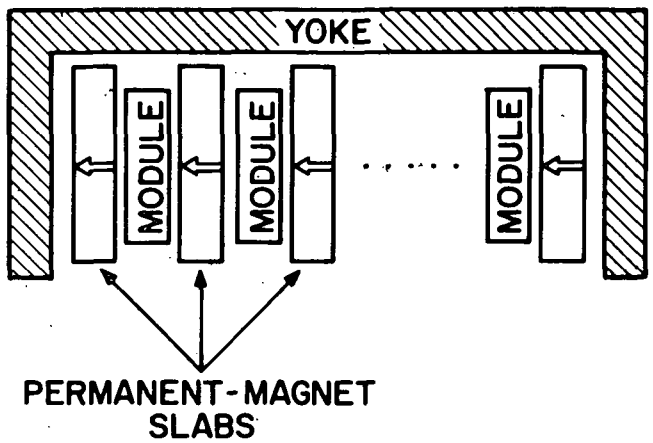


Fig. D1 Original Permanent Magnet Structure

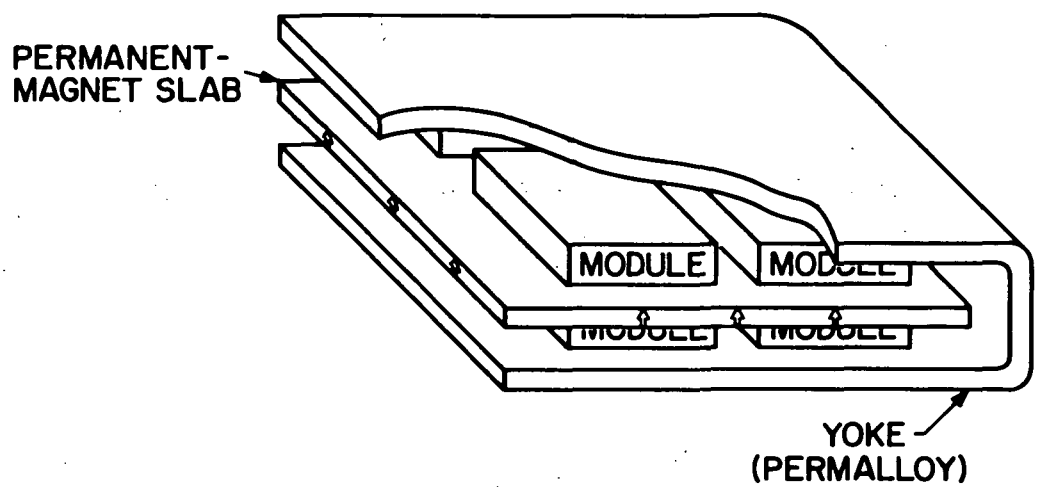


Fig. D2 Planar Structure

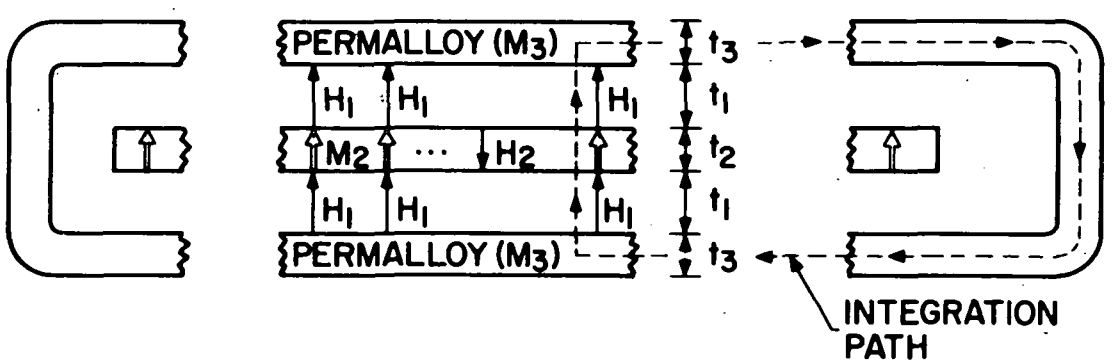


Fig. D3 Integration Paths

The thicknesses of the permanent magnet slab and permalloy yoke may be calculated with the aid of Fig. D-3. To the first order H_1 and H_2 are assumed to be vertical and uniform. From Gauss' law, the normal component of B at an interface must be continuous, hence

$$H_1 = M_2 - H_2 \text{ (MKS)}$$

or

$$H_1 + H_2 = M_2 \text{ (MKS)} \qquad \text{D-(1)}$$

From Ampere's law, the integral of $\bar{H}$ around a closed path is zero in the absence of current, hence

$$2H_1 t_1 - H_2 t_2 = 0 \qquad \text{D-(2)}$$

where it has been assumed that $\bar{H}$ in the permalloy is negligible. Combining D-(1) and D-(2),

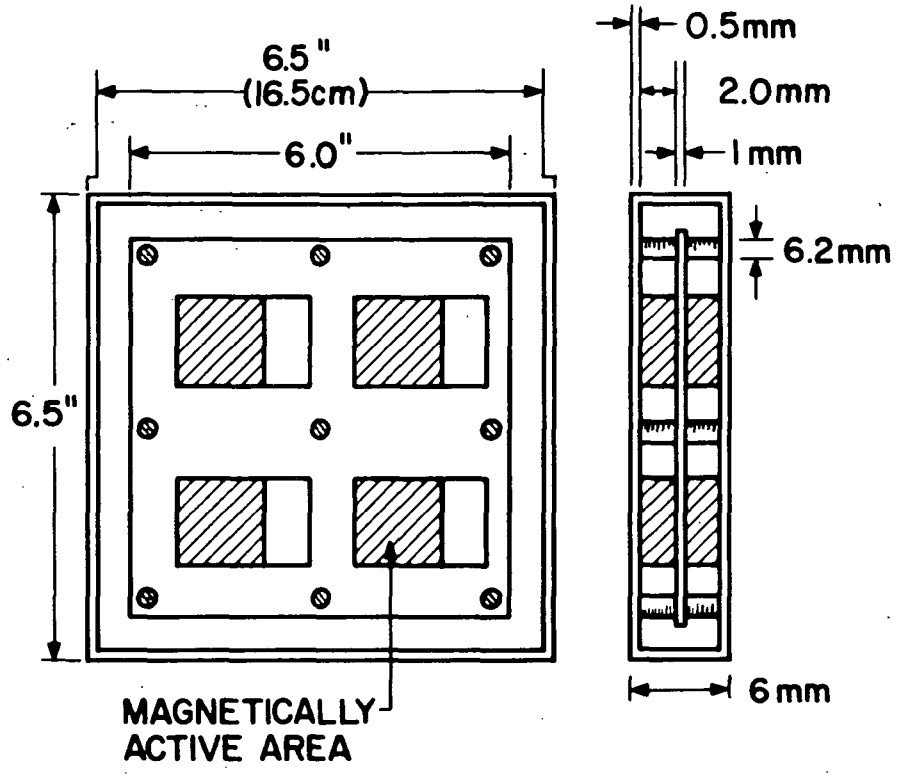
$$t_2 = t_1 \frac{2H_1}{H_2} = t_1 \frac{2H_1}{M_2 - H_1} \qquad \text{D-(3)}$$

Assuming that t_1, the clearance required for a module, is 80 mils = 2 mm = 2×10^{-3}m, that H_1, the required bias field, is 100 Oe = 800 A/m, and that M_2, the hard magnetization, is 800,000 A/M (corresponding to $4\pi M_2 = 10^4$ gauss in cgs units which is valid, for example, for Alnico 5-7 [IG 63] or Samarium-Cobalt [R69],) one obtains that $t_2 = .0202 \quad t_1 = 1.6$ mils = 4.04×10^{-5}m = 40.4 μm. Thus the permanent magnet "slab" is actually a large, thin, fragile wafer. Permanent magnets with a smaller magnetization could be used, resulting in thicker slabs, but this is inefficient from the weight standpoint.

The permalloy must be thick enough to avoid being saturated by the flux it must carry. Near the edges of the structure, the permalloy must carry the entire flux corresponding to the product of package area and field. Four modules have a combined area of 27 square inches, and assuming that the package is oversized by about half a module-width along each edge, the 100 Oe field exists over an area of approximately 6.5" x 6.5" or 42 in^2, giving a flux of 2.7×10^{-4} weber. The saturation flux density of permalloy is 1 weber/m^2 (10^4 gauss), so the cross-section area must be greater than 2.7×10^{-4} $meter^2$, and if the edge is to be 5", the thickness must be greater than 1.25×10^{-3} meter or .065".

3) Recommended Design - A lighter and more practical version of the planar package of Fig. D-2 is shown in Fig. D-4, which is an adaptation of a design shown by Bell Labs [G71]. The flux to be supplied is the same as for Fig. D-2, and thus the total cross-section area of the posts will be $(0.1)\ (5")^2 = 2.7 \times 10^{-4}\ m^2$. Since there are 9 posts on each side of the sub-unit, each will have an area of $3.0 \times 10^{-5}\ m^2$ and a diameter of 6.2×10^{-3} m or 6.2 mm. The volume of permanent magnet material is $6.2 \times 1.08 \times 10^{-6}\ m^3$ per sub-unit, identical to that of the design of Fig. D-2. However, it will be shown that the permalloy volume is considerably less.

The permalloy thickness t_3 is again chosen to avoid saturation, but now the permalloy need no longer carry the total flux, since the flux return paths now are shorter. If saturation is to be avoided more than one post-diameter d away from the post, then the area $\pi t(3d)$ must $> \pi d^2/4$, t must be greater than d/12 or 5×10^{-4}m or .2" (i.e., about 20 mils vs. 65 mils in the previous design). The shield may be thinner if circular



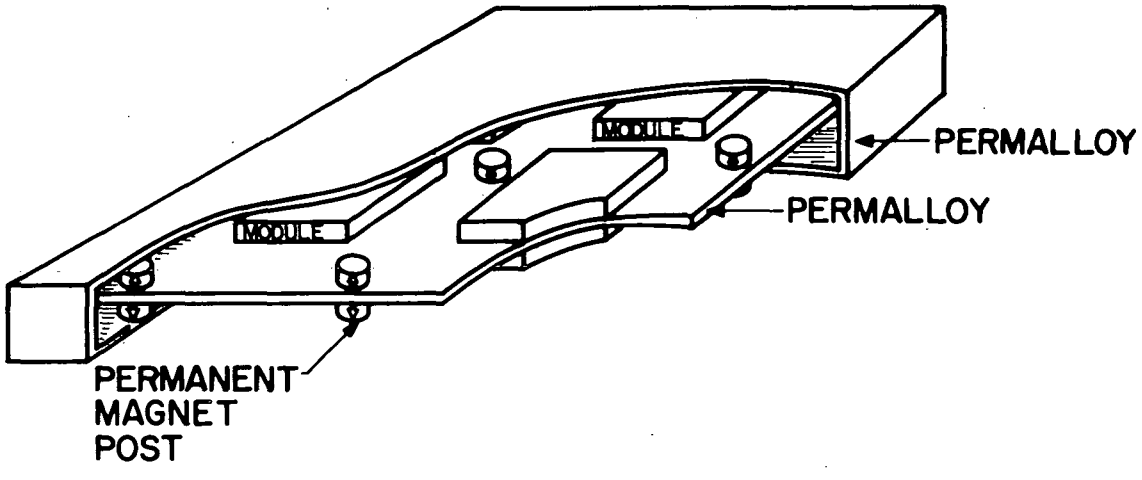


Fig. D4 Preferred Magnetic Design

Weight of Permalloy = 413g (0.91 lb)
" " Per. Mag. = 9g (0.02 lb)
Total = 422g (0.93 lb)

(Assumes density of 8g/cc for each)

patches of thicker permalloy foil are placed at the end of each post. Thus, the package of Fig. D-4 will be lighter than that of Fig. D-2, more easily fabricated, and will still provide good shielding against both internal and external fields. Its integration into the total memory package is described in Section 3A3.

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APPENDIX F

CHIP ORGANIZATION PARAMETER STUDY

```
    ∇ SYSCALC;JJ;RELS
[1]   JJ←1
[2]   INITIATE
[3]  AGAIN:RELS←((ρV1),6)ρ0
[4]   TT←T×V1÷12
[5]   HEADER
[6]   I←1
[7]  NEXT:RELS[I;]←(⍳6) RCHIP TT[I]
[8]   →((ρTT)≥I←I+1)/NEXT
[9]   RELS
[10]  LCELL←LCELL×10
[11]  LAMBDAS←LAMBDAS×10
[12]  →(2=JJ←JJ+1)/AGAIN
[13]  V1←V1[⍳4]
[14]  →(3≥JJ)/AGAIN
[15]  LCELL←LCELL÷1000
    ∇
      V1
1  3  6  12  18  24  36

    ∇ R←RS RCHIP T;J
[1]   AUX
[2]   R←⍳0
[3]   →(~R41∈RS)/L61
[4]   R←R,A[1]×X[1]×(W[1]×(B×S*L)*4)*Q
[5]   →(∧/~(R61,R62,R71,R72)∈RS)/L52
[6]  L61:SUM←1++/(S SERIES E)×H[⍳E]
[7]   →(∧/~(R61,R62)∈RS)/L71
[8]   R6←((B*N)×(S*LN)×SUM)+N×(B*N-1)×B×S*L×N-1
[9]   →(~R61∈RS)/L62
[10]  R←R,A[2]×X[2]×(W[2]×R6)*Q
[11]  →(~R62∈RS)/L71
[12] L62:R←R,A[3]×(X[3]+X[3]×1-X[3])×(W[3]×R6)*Q
[13] L71:→(∧/~(R71,R72)∈RS)/L52
[14]  R77←(2!N+1)×(B*N-1)×B×B×S*L×N-1
[15]  R7←(((B*N+1)+(N+1)×(B*N)×B)×(S*LN)×SUM)+R77
[16]  →(~R71∈RS)/L72
[17]  R←R,A[4]×X[4]×(W[4]×R7)*Q
[18] L72:→(~R72∈RS)/L52
[19]  R←R,A[5]×(X[5]+X[5]×1-X[5])×(W[5]×R7)*Q
[20] L52:→(~R52∈RS)/0
[21]  R5←(R1*5)+5×(R1*4)×1-R1←B×S*L×17÷16
[22]  R←R,A[6]×(X[6]+X[6]×1-X[6])×(W[6]×R5)*Q
    ∇

    ∇ SER←S SERIES E;J;Q
[1]   SER←,LN×Q←(1-S)÷S
[2]   J←1
[3]  NEXT:SER←SER,SER[J]×(LN-J)×Q÷J+1
[4]   →(E>J←J+1)/NEXT
    ∇

    ∇ INITIATE
[1]   N←6
[2]   LN←N×L←128
[3]   LMN←LN×M←16
[4]   O←800
[5]   Q←16
[6]   R52←1+R72←1+R71←4
[7]   R62←1+R61←1+R41←1
[8]   LXISTOR←5E¯9
[9]   LINTEGRATED←1E¯9
[10]  LXFORMER←6×1E¯8
[11]  FAILRATES
    ∇

    ∇ AUX
[1]   S←1-S←*-LAMBDAS×T
[2]   B←1-B←*-LAMBDAB×T
[3]   X←1-X←*-LAMBDAX×T
[4]   W←*-LAMBDAW×T
[5]   A←*-LAMBDAA×T
    ∇
```

```
    ∇ GO J;RELS;TIMES;K
[1]   INITIATE
[2]   K←3
[3]   RELS← 0.99 0.95 0.9 0.85 0.8 0.7 0.6 0.5
[4]   2 1 ρ' '
[5]   '   SYSRELS ARE ';φRELS[⍳J]
[6]   TIMES←(J,6)ρ1
[7]  AGAIN:HEADING
[8]   JJ←J
[9]  MORE:I←1
[10]  RSPEC←RELS[JJ]
[11] NEXT:FIND I
[12]  TIMES[JJ;I]←0.01×⌊100×(T÷730÷2÷3)+0.004
[13]  →(6≥I←I+1)/NEXT
[14]  →(0<JJ←JJ-1)/MORE
[15]  φ[1] TIMES
[16]  LCELL←LCELL×10
[17]  LAMBDAS←LAMBDAS×10
[18]  →(0<K←K-1)/AGAIN
[19]  LCELL←LCELL÷1000
[20]  T←8768
    ∇

    ∇ FIND I;PS;T0;R0;V
[1]   EXP←1.5
[2]   V←0.1
[3]   E←3
[4]   RSYS←(I RCHIP T)
[5]  AGAIN:T0←T
[6]   R0←RSYS
[7]   T←T×((1-RSPEC)*1E¯10⌈1-RSYS)**EXP
[8]   RSYS←(I RCHIP T)
[9]   EXP←0.9⌈(●(1E¯10⌈1-R0)÷1E¯10⌈1-RSYS)÷●T0÷T
[10]  →(V<|RSPEC-RSYS)/AGAIN
[11]  →(V=0.01)/LAST
[12]  →(V=1E¯5)/0
[13]  E←6
[14]  V←0.01
[15]  →AGAIN
[16] LAST:E←13
[17]  V←1E¯5
[18]  →AGAIN
    ∇

    ∇ FAILRATES
[1]   LAMBDAS←M×LCELL×O+40+1024÷L
[2]   LAMBDAC←0.25×(2×LXISTOR)+20×LINTEGRATED
[3]   LAMBDAP←(10×LXFORMER)+14×LXISTOR
[4]   LAMBDAB←LAMBDAP+M×LAMBDAC
[5]   LAMBDAW←LINTEGRATED× 128 160 320 302 470 616
[6]   LAMBDAX←LINTEGRATED× 778 6922 7018 7018 7065 1610
[7]   LAMBDAA←LINTEGRATED× 128 144 292 144 292 276
    ∇
```

APPENDIX G

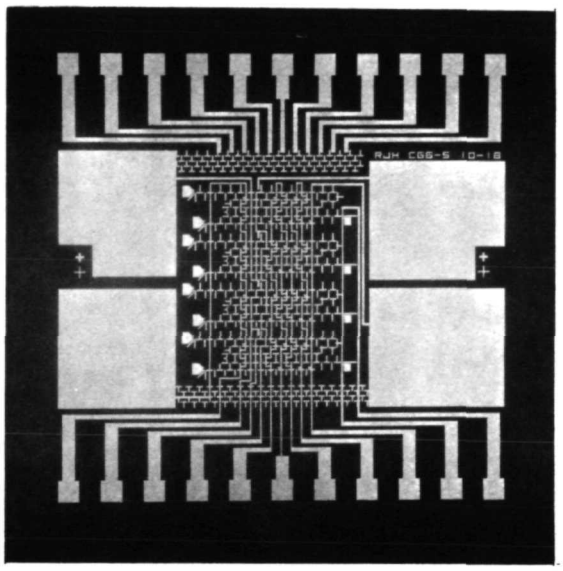
PHOTOLITHOGRAPHIC MASKS FOR THE FEASIBILITY MODEL

This appendix describes the photolithographic masks used to fabricate the feasibility model overlay, and how these masks are made.

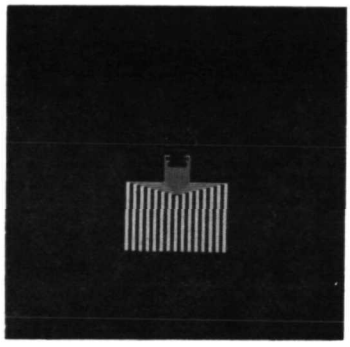
How the Masks are Used

The three masks used in the fabrication process of Sec. 4A2.1 are shown in Figs. G1, G2, and G3. Briefly reviewed, the overlay fabrication process is as follows:

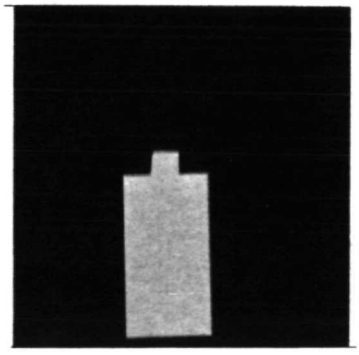
1) 200Å magneto-resistive permalloy is evaporated onto a 1-1/4" diam. glass substrate.
2) Photoresist is spun onto the evaporated film, and the composed "CG" ("copper or gold") mask (Fig. G1-d) is used to expose the photoresist, which is then developed. After that, ~6000Å copper or gold is electroplated through the resulting holes in the photoresist to form the control (decode, write, clear) and sense lines.
3) The old photoresist is removed and replaced by a new layer, which is then exposed using the composed "NI" (permalloy) mask (Fig. G2-C). The photoresist is developed, and 4000Å permalloy is electroplated through the holes to form the propagation pattern (T-bars, generators, annihilators, etc.)
4) Again, the old photoresist is removed and replaced by a new layer, which is then exposed using the composed "AZ" (protect) mask (Fig. G3-C). After development, photoresist remains on top of all propagation permalloy and control



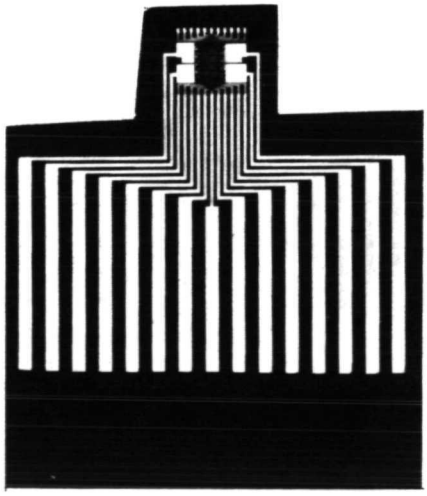
a



b



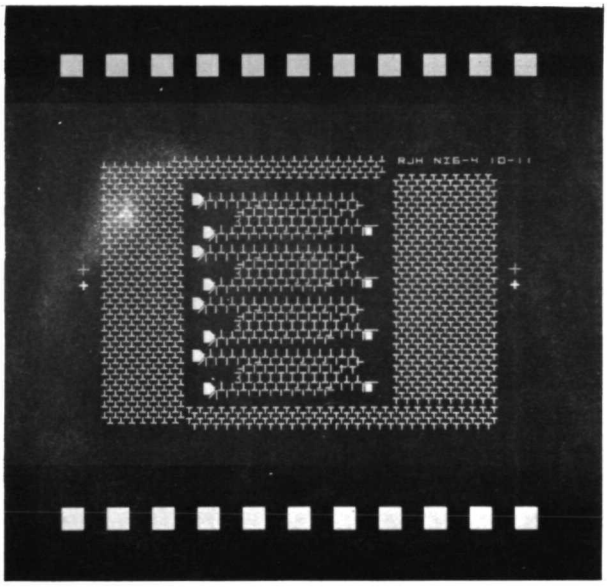
c



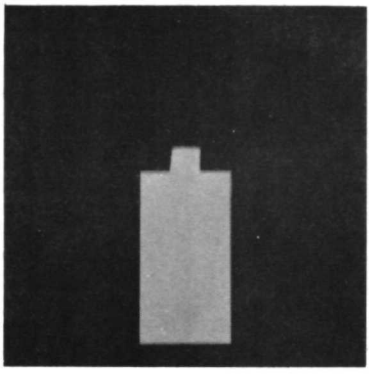
d

Fig. G1 Conductor Pattern ("CG") Mask.
a) Chip mask, generated by PLT (boxes at extremities of lead-in lines are .005" x .005" (125μm x 125μm).

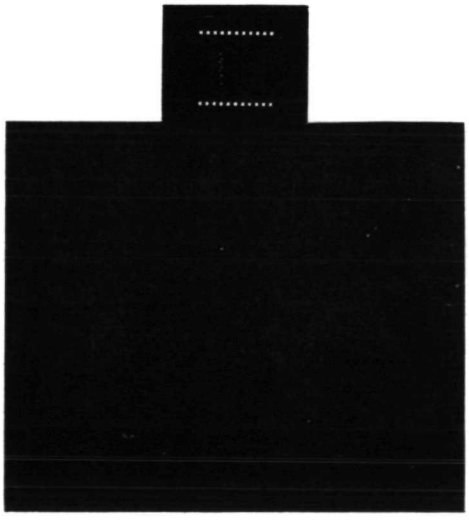
b) Fan-in mask, reduced from stabilene cut-out. Widest portions of lines are 20 mils (0.5mm) on 40 mil (1mm) centers.
c) Shroud mask
d) Composed working mask



a

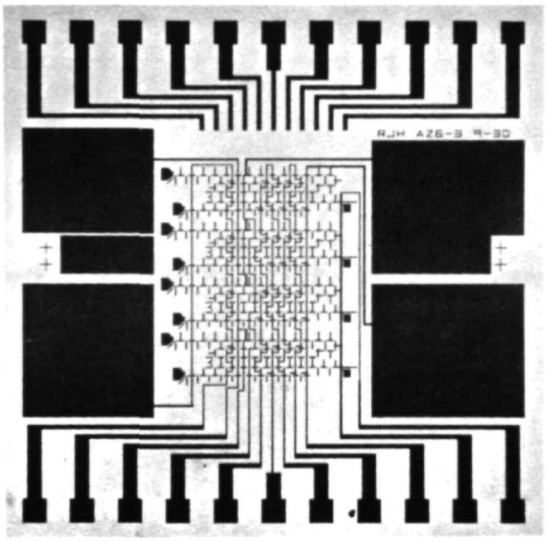


b

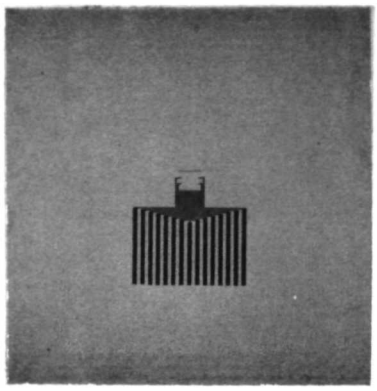


c

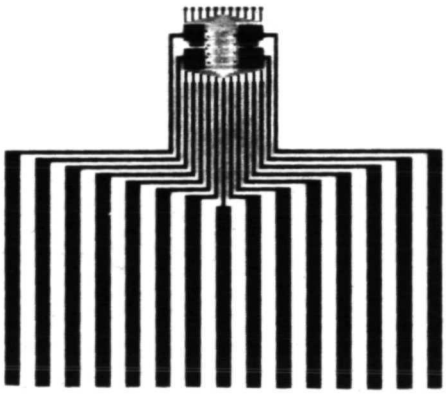
Fig. G2 Propagation Permalloy ("NI") Mask.
a) Chip mask. Boxes are .005" x .005" (125μm x 125μm)
b) Shroud mask
c) Composed working mask



a



b



c

Fig. G3 Sensor Protect ("AZ") mask.
a) Chip mask. Boxes at ends of lines are .005" x .005" (125μm x 125μm)
b) Fan-in mask; widest lines are 20 mils wide on 40 mil centers (0.5mm wide on 1mm centers)
c) Composed working mask

lines plus in the small areas where the sensors are to appear. The overlay is then subjected to one of the etch processes described in Sec. 4A2.1. This removes the 200Å Permalloy everywhere except where masked by photoresist or plated metal.

The resulting overlay structure is shown in Figs. 4A2-1, 4A2-3, and 4A1-3.

Why the Masks look the Way they do

Positive* photoresist (Shipley AZ-111) is preferred over negative photoresist (KTFR, KPR) for better resolution and greater ease of removal (see Sec. 4A2.1). Hence, the "CG" and "NI" masks, which are to result in control lines or T-bars must consist of clear control lines and T-bars on a dark background (Figs. G1, G2). They must be "correct negatives", which means that any lettering on them will read correctly where the masks are placed emulsion-side-down. The "AZ" mask, on the other hand, is designed to leave photoresist behind where there are T-bars and control lines (and sensors), and so it must have dark T-bars and control lines on a light background (Fig. G3). It must be a "correct positive".

One obvious feature of the "CG" mask (Fig. G1-a) is that in addition to conductor lines, copper (or gold) T-bars, generators, etc. will also be plated, to be topped eventually by permalloy T-bars, generators, etc. In other words, all propagation permalloy has a 6000Å layer of conductor under it. Among other reasons, this is done to maintain a uniform

*A positive photoresist is one in which the areas exposed to light are removed by the developer.

spacing between the permalloy elements and the epitaxial bubble layer. Plating considerations are also involved in this, as well as in the placement of the four large copper pads near the active area.

This is also partly the reason for the belt of close-packed T-bars which surrounds the active area in the "NI" mask (Fig. G2-a). In addition, these T-bars act as "getters" which guide stray bubbles away from the active area.

The active area of the "AZ" protect mask is almost an exact correct positive of the "CG" mask. The only difference is that the four small sensor areas identified in Fig. 4A1-3 appear as gaps in the "CG" mask whereas they are solid in the "AZ" mask.

How the masks are made

The complexity of the permalloy and conductor patterns of even this small chip is such that the only practical way to generate the corresponding artwork is with a computer-controlled Programmed Light Table (PLT). Can the whole mask be generated this way? In our case, the answer is no, because the smallest aperture on the PLT available to us is 0.5 mil (.0005"), which can be moved in 0.5 mil steps within a 2" x 2" area. Thus, an overlay with 0.3 mil (7.5 μm) or smaller features must be drawn to a larger scale by the PLT and then reduced 10x or 20x photographically.

The required resolution was obtained only with 20x reduction, which meant that the reduced mask from the PLT would cover an area 0.1" x 0.1" (100 mil x 100 mil). This is large enough to contain the active area of the feasibility chip, but not the fan-in lines.

Because of the way in which the feasibility model is assembled (Fig. 4A2-7), these fan-in lines must run $\approx$ 3/8" or more to the pressure

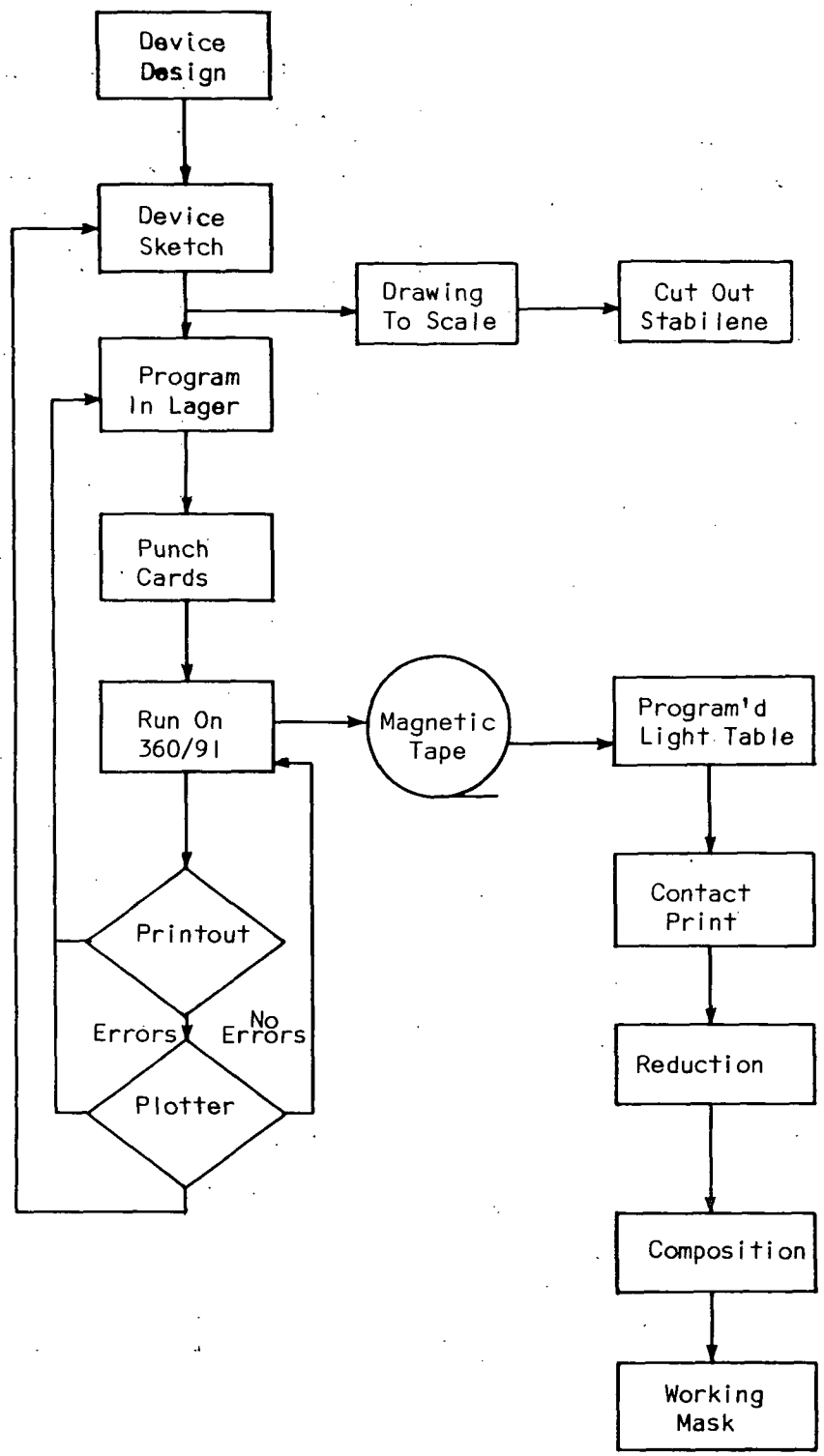


Fig. G4 Artwork Generation for the Masks

contacts. The feasibility model is a sandwich of a 3/4" diameter epitaxial garnet film and a 1-1/4" glass disk. All the T-bars, conductors, etc. are sandwiched between these two disks with an allowable air gap of at most 0.5 μm. Thus, the fan-in lines must be long, flat lines directly on the glass disk. Conventional chip-joining techniques cannot be used to contact the overlay in this case, because they would result in too much separation between overlay and garnet. This is the price one must pay for the quick-interchange capabilities of this sample holder which was so useful during the testing stages.

Accordingly, the artwork for each of the final masks (Figs. G1-d, G2-C, and G3-C) was supplied in two or three parts which had to be composed (see the flowchart of Fig. G4, which describes artwork generation). The chip masks (shift registers, etc., Figs. G1-a, G2-a, and G3-a) were drawn 20x larger than needed by the PLT and then reduced 20x. The fan-in lines were cut from K & E Stabilene Cut-and-strip Film Type 44-5545 and also reduced 20x to give the fan-in masks of Figs. G1-b and G3-b. The "mantle" or "shroud" pattern of Fig. G1-C and G2-b was cut to exact scale from the same material. Photographic composition of these parts into complete working masks turned out to be a non-trivial problem, as will now be described.

The flowchart of the photographic process is shown in Fig. G5. The PLT master is a correct positive 2" x 2" pattern on a 4" x 5" photographic plate. The contact print of this master is therefore a reversed negative (letters read backwards with emulsion down). If this were reduced 20x and developed in the normal way, the result would be a 20x reduced correct positive. The "AZ" mask (Fig. G3-a) is done this

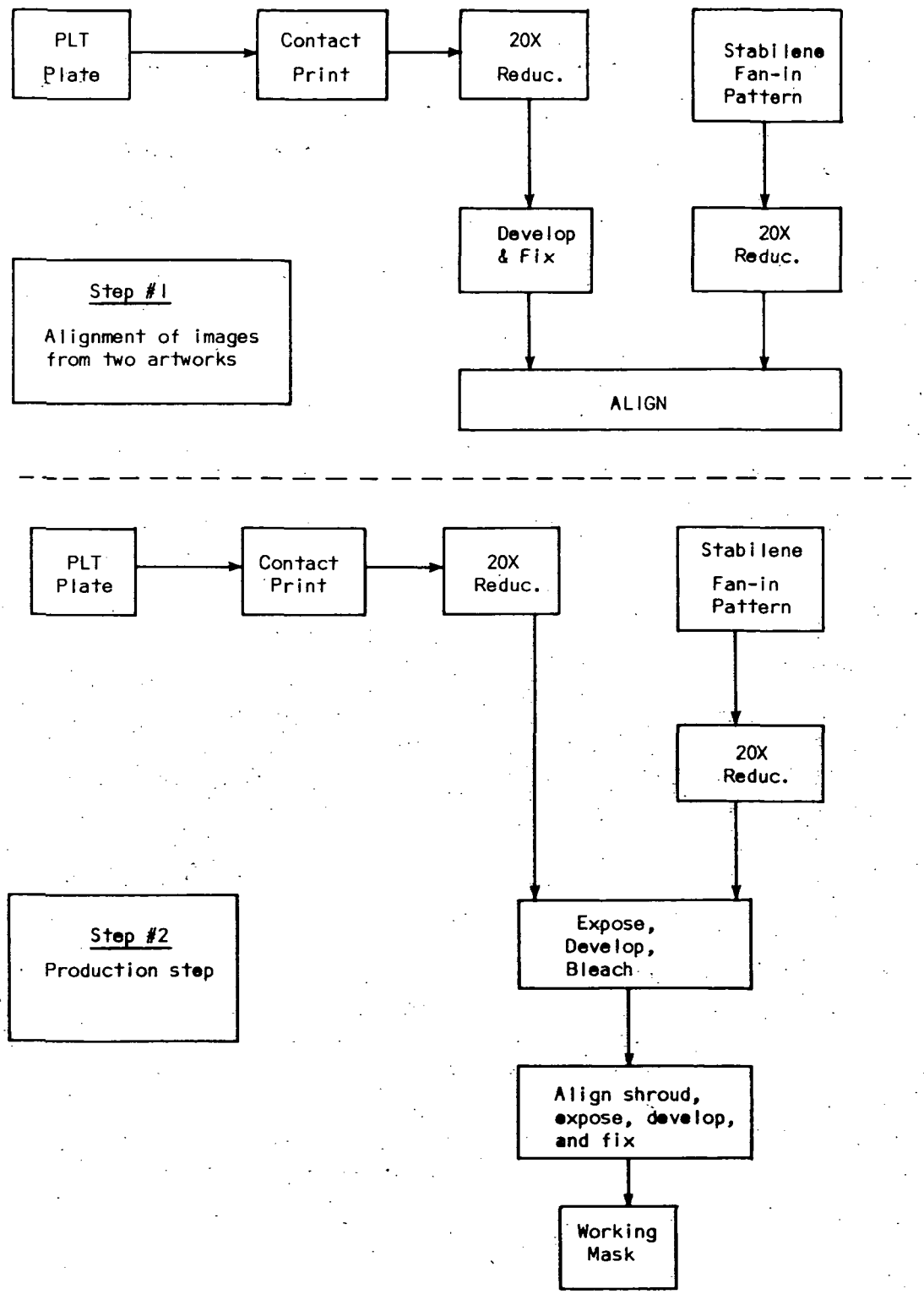


Fig. G5 Photographic Steps in Production of a Working Mask

way. However, the "NI" and "CG" masks must be correct negatives. This can be done by positive processing instead of negative processing, i.e., by bleaching the exposed portion of the reduced correct positive before fixing (the bleach affects only the exposed portions and renders them permanently clear), re-exposing the entire mask to light, developing and fixing. The correct negative chipmasks of Fig. G1 and G2 were made in this way.

The procedure for obtaining the correct negative composed masks of Fig. G1-d and G2-c is more complicated. Two cameras holding 2" x 2" photographic plates are set up; one to take 20x-reduced pictures of the contact print of the PLT master (reversed negative), and one to take 20x-reduced pictures of the fan-in master (reversed negative). The first camera takes a picture of the PLT master contact print (chip mask) which is developed and fixed, put into the second camera, and aligned with the fan-in pattern. After alignment has been achieved, it is discarded. A second picture is now taken with the first camera, placed directly into the second camera, aligned mechanically, and exposed to the fan-in lines. This is developed and bleached, but not fixed. (The unfixed emulsion is still sensitive to light).

At this point, the working mask is certain to have clear T-bars, etc. and clear fan-in lines. Everything else is still light-sensitive. Exposure, development, and fixing at this stage would give a final metal pattern on the glass disk consisting only of metal T-bars, etc., and fan-in lines. For plating purposes, however, it is desired to form metal everywhere that it is not objectionable (see Sec. 4A2.1).

To do this and achieve a pattern similar to that of Fig. 4A2-3, the shroud mask of Figs. G1-c or G2-b is placed over the bleached fan-in lines and active area of the 2" x 2" photographic plate, which is then exposed to light, developed, and fixed. This provides the dark background for the bleached light T-bars, etc. and fan-in lines, and leaves a substantial portion of the surrounding area clear so that metal will be formed there as desired. The result is the composed working mask of Fig. G1-d or G2-c.

The procedure for the correct positive working mask of Fig. G3-c is analogous.

Variations on the Process

As with the description of the fabrication scheme of Sec. 4A2.1, the intent here has been to give one representative, consistent process which results in a set of useful masks. There are other ways to make the same masks, and there are fabrication processes which do not use composed masks.

As an example of the former, it may be noted from Fig. G1-d that the shroud mask is not very critical. In fact, the overlay of Fig. 4A2-3 was made using a mask which had been exposed, developed, and fixed after the chip mask and the fan-in mask had been joined. This resulted in the entire periphery of the mask being black. The unwanted exposed emulsion was simply scraped away with a razor blade, giving a result similar to the use of a shroud mask.

In addition, it is possible to shift the burden of aligning and composing from the mask fabrication process to the overlay fabrication process by using separate masks and multiple exposures of the photoresist.

This proved feasible in a laboratory environment but would probably be impractical as a manufacturing process.

Other variations are also possible. In all cases, however, it is well for the mask designer and fabrication process designer to become quite familiar with the capabilities and limitations of the mask-making facilities at his disposal.

APPENDIX H

PUBLISHED EXCERPTS

The following comprehensive summary of the present work was presented as papers 4F3 and 4F4 at the 17th Conference on Magnetism and Magnetic Materials, Chicago, November 1971, and will appear in the proceedings of that conference. These papers are reproduced here for the convenience of the reader. In case of slight numerical discrepancies, the final report is correct.

FABRICATION AND OPERATION OF A SELF-CONTAINED BUBBLE DOMAIN MEMORY CHIP*

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ABSTRACT

This paper describes the fabrication and operation of a 52-bit bubble domain memory chip designed to test the concept of on-chip magnetic decoding. Access to one of the chip's four shift registers for the read, write, and clear functions is by means of bubble domain decoders utilizing the interaction between a conductor line and a bubble. All other functions are performed by a permalloy overlay driven by an external rotating field. The metallurgy consists of 200 Å evaporated permalloy for magnetoresistive sensors, 4000 Å electroplated permalloy for propagation etc., and 6000 Å electroplated copper for control lines.

INTRODUCTION

The concept of a self-contained magnetic bubble domain memory chip was set forth in a recent paper by Chang, et al.[1]. The chip contains a number of individual shift register, and is designed to be used in a memory which provides random access to blocks of information which are then read out serially. However, rather than using coincident block access[2] to select a chip and a common communication channel[3] to transfer information into and out of a chip, these functions are both performed using an on-chip magnetic decoder made up of logic gates utilizing the interaction between a bubble domain and a current-carrying conductor. The chief advantage of this approach is the simplicity of the resulting memory organization, as further discussed in a companion paper[4]. Here, we describe the design, fabrication, and operation of such a memory chip.

DESIGN

The design chosen to test this concept is shown in block-diagram form in Fig. 1. It consists of four shift registers and all the control functions necessary to write into, read out, and clear any one of the four shift registers. Each shift register has a built-in write decoder and read decoder section. Since the emphasis was on testing the control functions, the storage capacity of each register is small (only 13 bits). The same layout to be described here can provide access to four much longer shift registers, and in a full-scale chip, between 90% and 95% of the total area is available for storage.

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Methods for generation, propagation, and annihilation of bubbles with a permalloy overlay and a rotating in-plane field have already been described[5,6]. Magnetoresistive sensors for bubble domains have also been reported[7,8] The write, clear, read decoder, and write decoder functions make use of a current-controlled switch which is shown in Fig. 2. This switch allows a small control current to select one of two alternate paths in the permalloy overlay for the bubble domain. A bubble B entering the switch from the right will emerge from the upper port if the current I is positive, and from the lower port if I is negative. The complete chip layout is shown in Fig. 3.

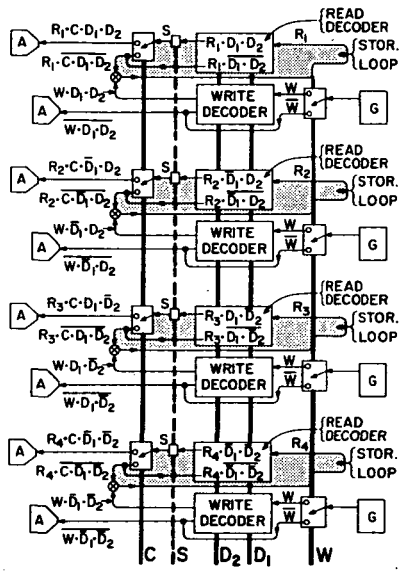

Fig. 1. Block diagram of the memory chip's operation. (G--generator, A--annihilator, S--sensor, W--write control line, D_1, D_2--decode control lines, C--clear control line, R_1, R_2, R_3, R_4--information stored in register 1, 2, 3, or 4)

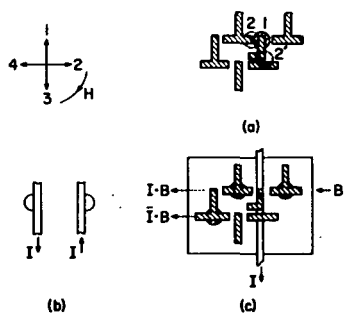

Fig. 2. The basic switch.
a.) In the absence of control current, it is uncertain whether the bubble will move from position 1 to 2 or 2'.
b.) Effect on bubble position of current in a stripline.
c.) Combining the permalloy and conductor patterns as shown results in the "single-pole, double throw" switch whose Boolean representation is shown here. (The current is on between field positions 1 and 2.)

Since logic as well as storage are being accomplished on the chip, it is useful to represent the switch in Boolean algebra. The switch may be viewed as a two-output logic element operating on the two binary inputs B and I. B will be considered 1 when a bubble is present and 0 when a bubble is absent; I will be considered 1 for positive current and 0 for negative current. Then the output at the upper port is the Boolean "And" function (B•I), whereas the other

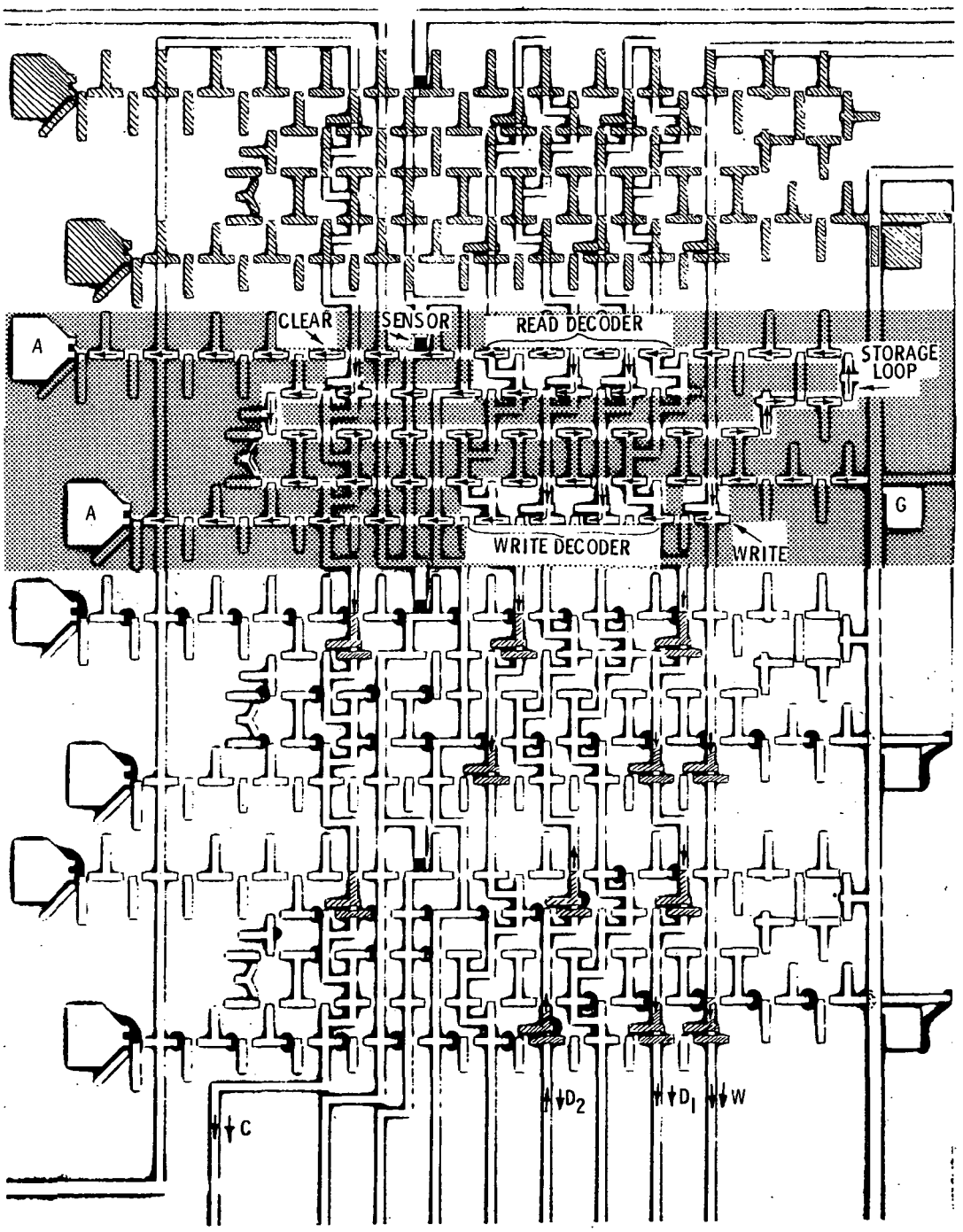

Fig. 3: Layout of the chip. In the top register, the permalloy pattern is cross-hatched, the overlapping conductor is clear. In the next shift register down, the essential functions of Fig. 1 have been highlighted. The actual control currents are shown as arrows on top of the control lines.

output is $(B \cdot \overline{I})$, where $\overline{I}$ is the binary inverse of I.

The operation of the chip can now be explained in terms of Figs. 1, 2, and 3. The generators G are all designed to emit a steady stream of bubbles. To write a 1 into one of the 2^n registers, the write control current W is made positive. This allows a bubble to enter each of the 2^n write decoders. In one of these write decoders, the n decode currents will have the right combination to allow the bubble to propagate out the upper port and into the storage loop. In all the other $2^n - 1$ write decoders, the bubble will exit from the lower port and into an annihilator. In Fig. 3, the third register from the top, $(D_1 \cdot \overline{D}_2)$, is being written into. The simultaneous proceeding in an unselected register are shown in the bottom register $(\overline{D}_1 \cdot \overline{D}_2)$.

When writing is finished, the write switch is turned off (W becomes negative), and as long as the clear control current C is negative, the information will circulate in the storage loop. Each storage loop contains a read decoder section whose layout is identical to that register's write decoder section. Therefore, the same combination of decode currents which selected a register for write-in also selects it for read-out. In the selected register, the bubble exits at the top port of the read decoder and goes by a magnetoresistive sensor. In all the other registers, the bubble exits at the bottom port and bypasses the sensor.

After passing the sensor, the bubble in the selected shift register enters the clear control switch. For negative clear control current $\overline{C}$, the bubble is returned to the storage loop. However, if new information is to be entered into the register, the clear current is made positive, and the bubbles go to an annihilator. This is shown happening in register $D_1 \cdot \overline{D}_2$, Fig. 3. Thus, information may be written into, read out of, and cleared out of any one of the 2^n registers by activating n decode lines.

OVERLAY FABRICATION

The design was tested using separate overlays formed on a glass substrate. A 200 Å film of permalloy (81% Ni, 19% Fe) was evaporated onto the glass substrate at a substrate temperature of 330°C; this 200 Å permalloy film serves as a base for subsequent electroplating and is also used to form the sensor element. The 7.5μm-linewidth copper conductor metallurgy was formed by electroplating to a thickness of 6000 Å using a mixed copper sulfate/nitrate plating bath. The 7.5μm-linewidth T-bar metallurgy was formed by electroplating permalloy to a thickness of 4000 Å using a modified Wolf's plating bath. Finally, the magnetoresistive sensor elements were defined by etching of the 200 Å permalloy.

OPERATION

The overlay designs were tested with $Sm_{0.1}Gd_{2.24}Tb_{0.66}Fe_5O_{12}$

bulk garnet platelets and $Eu_{0.7}Y_{2.3}Fe_{3.8}Ga_{1.2}O_{12}$ epitaxial garnet films[9] grown by the LPE technique. The bulk garnet platelets were polished down to a thickness of about 30 μm. Nominal epitaxial film characteristics were a thickness of 15 μm, a bubble diameter of 12 μm, and a $4\pi M_s$ of 125 gauss.

The main problem encountered with the bulk platelets was a rather strong sensitivity to temperature and in-plane field. All of the device functions shown in Fig. 3 were operational; however, the annihilators required greater than 40 Oe drive field at quasi-static frequencies. Spacing between the overlay and the platelet was found to be very critical. A spacing of less than 5,000 Å caused domain nucleation, and a spacing greater than 10,000 Å resulted in poor device operation. The sensitivity of the bubble diameter to the in-plane field was quite serious for fields greater than 30 Oe. This in-plane field response was probably due to the fact that the easy-axis was not exactly normal to the platelet. There were also problems associated with stray bubbles in the regions surrounding the active device; these stray bubbles tended to enter the active device and cause errors.

In general the device operation was better for the LPE films than the bulk platelets; however, the larger bubble diameter to height ratios obtained with films required design changes in some of the device functions which were satisfactory for platelets. The corner design was found to be more critical for films than platelets. The current-controlled switches also required modification. Typical in-plane drive field requirements at quasi-static frequencies were as follows: straight line propagation - 10 Oe, corners and junction - 13 Oe, generators - 20 Oe, and annihilators - 25 Oe. The switches required a control current of 25 mA with an in-plane drive field of 30 Oe. The magnetoresistive sensor signal was 200 μV for a sensor current of 2 mA.

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RELIABILITY AND ORGANIZATION OF A 10^8-BIT BUBBLE DOMAIN MEMORY*

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ABSTRACT

This paper describes the conceptual design of a highly reliable 10^8-Bit Bubble Domain Memory for the Space Program. The Memory has random access to blocks of closed-loop shift registers, and utilizes self-contained bubble domain chips with on-chip decoding. Tradeoff studies show that the highest reliability and lowest power dissipation is obtained when the memory is organized on a bit-per-chip basis. The final design, has 800 bits/register, 128 registers/chip, 16 chips/plane, and 112 planes, of which only seven are activated at a time. A word has 64 data bits +32 checkbits, used in a "16-adjacent" code to provide correction of any combination of errors in one plane. 100 KHz maximum rotational frequency keeps power low ($\leq$ 25 watts) and also allows asynchronous operation. Data rate is 6.4 megabits/sec, access time is 200 μsec to an 800-word block and an additional 4 msec (average) to a word.

SYSTEM ORGANIZATION

Of the many organizations possible in expanding the on-chip decoding concept[1] into a design for a 10^8-bit memory, three were studied in detail: bit-per-shift register, bit-per-plane, and bit-per-chip. The first allows the use of same-chip bubble domain logic devices for error correction, but has the highest vulnerability to failures. The second dissipates the most power. The bit-per-chip organization has the best overall reliability of the three, results in a reasonable power dissipation, and is the subject of the remainder of this paper. It is described in Fig. 1. The basic 10^5-bit memory chip (Fig. 1a) is scaled-up version of the functioning chip whose operation has been described elsewhere[2]. Assumed linewidth is 0.1 mil (2.5μm) corresponding to bit density of 2.5×10^6/sq. in. Each of the 128 closed-loop shift registers has a write decoder and a read decoder section, with seven control lines ($2^7 = 128$). These decoders select one of the 128 registers on the chip for write-in, read-out, or clear-out. Instead of a sensor per shift register[2], each register has a bubble splitter (Fig. 2b), from which one bubble re-enters the storage loop, while the other enters a 16:1 bubble fan-in leading to a magnetoresistive sensor. Thus, only 8 sensors (series-connectable) are required per 10^5-bit chip. The bubble fan-in consists of 16 paths converging on the sensor (Fig. 2b). The path delays can be made equal (0.5 msec) by placing more undulations in some paths than others. It may be possible to eliminate this delay by modifying a bubble compressor[3] to accept 16 inputs.

Sixteen chips are placed on a planar substrate, which then has X and Y coils would around it to supply the rotating in-plane field

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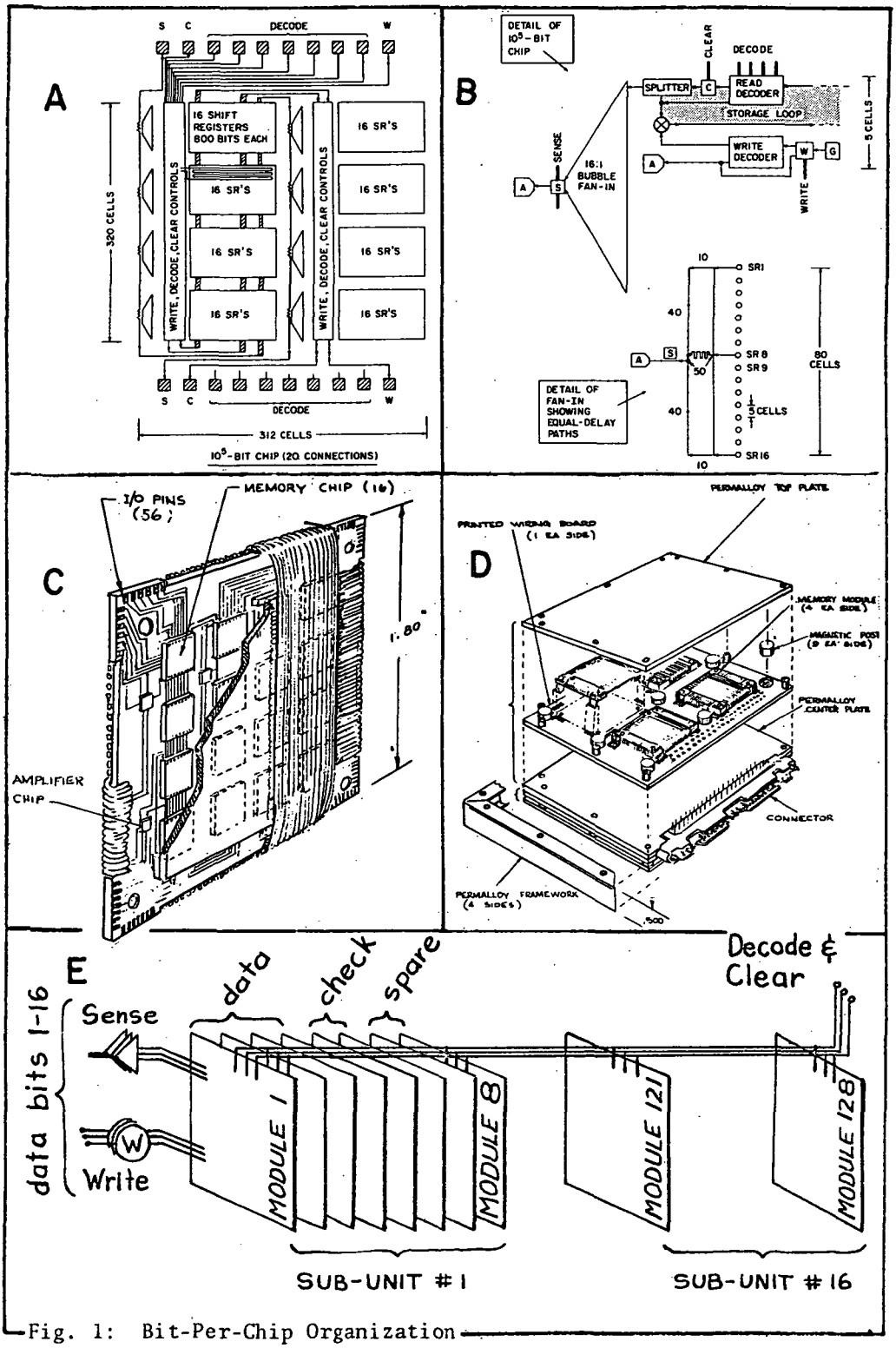


Fig. 1: Bit-Per-Chip Organization

(Fig. 1c). The result is a 1.6 x 10^6-bit module. Eight of these modules are arranged inside a permanent-bias-field package, forming one of the memory's 16 sub-assemblies (Fig. 1d). A memory word is stored on a bit-per-chip basis; each sub-assembly thus contains 10^5 words, each consisting of 64 data bits, 32 check bits, and possibly 16 or 32 spare bits, depending on the degree of reliability required. A stack of 16 of these sub-assemblies results in a memory with 1.6 x 10^6 words of 64 data bits each; it weighs 19 lbs. and occupies 450 in^3. Only one sub-assembly is activated at a time, resulting in an average operating power (circuits included) of only 25 watts (assuming 10 Oe rotating field and 10 mA control currents on the chip). The price for this is the relatively complex error correction code; only 50% of the memory's bit storage capacity is used for data.

ERROR CORRECTION

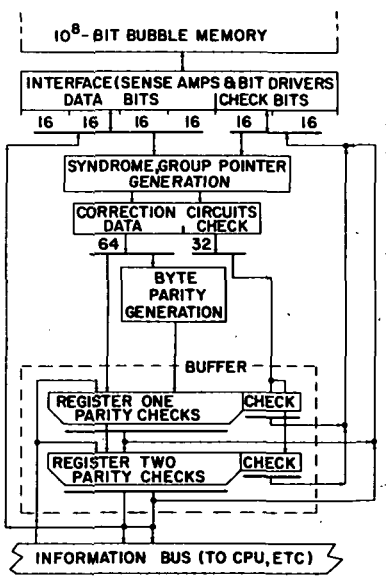


Fig. 2

The power requirement of a bubble domain memory can be reduced by operating only part of the memory at a time. However, this leaves the memory more susceptible to failure. To increase the basic reliability of the memory, the stored information is encoded into a 16-adjacent-bit single error correcting/double error detecting (SbEC/DbED) code[4,5] with 64 data bits and 32 check bits. This information is stored 16 bits to a plane on 6 planes.

The decoding circuitry used is called translator because it translates words between the SbEC/DbED form and byte-parity encoded form. The flow chart of the translator is shown in the Fig. 2. The 64 data bits are considered to be in groups 1 to 4 and the check bits in groups 5 and 6. The action of the translator during readout is as follows: First, 32 characteristic bits called syndromes (one corresponding to each check bit) are generated from known parity relations among the data bits and check bits. Next, six characteristics bits called group pointers are generated from known Boolean conditions satisfied by the 32 syndromes. Further action then depends on the error condition which exists in the word:

1) No error - the word proceeds to the parity generation process, where 8 parity bits are generated, one for each of the 8 groups of 8 data bits (i.e., one for each of the 8 bytes).

2) Error or errors in a single group - the group pointers indicate which group contains the error(s), and the syndromes indicate which bits are in error and must be inverted by the correction circuits, after which byte parity is again generated.

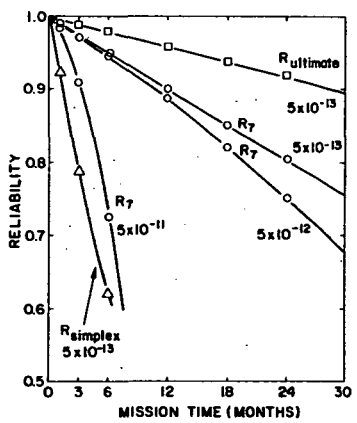
Any one of the $(2^{16}-1)$ possible erroneous patterns in one group can be corrected in this way.

3) Error(s) in more than one group - the group pointers are used to generate an appropriate multiple error signal to be sent to the CPU (Central Processing Unit).

After parity generation and checking, the 9-bit bytes are stored in the buffer and checked before use by the computer via the bus. During a write cycle, the process is reversed.

To guard against circuit failures in the translator itself, self-checking circuits must be used[6]. These techniques can be extended to handle syndromes, group pointers, etc., by the concept of morphic Boolean functions[7]. Thus, a completely checked, self-testing unit can be obtained. For this example, the increase in circuits over an unchecked design is about 25% (4583 circuits vs. 3665).

RELIABILITY ANALYSIS



Fig, 3

The model used to calculate the reliability of the bubble memory included failures in the driving, sensing, and control electronics as well as failures in the storage medium itself. A Poisson failure distribution was assumed, and failures were categorized according to whether they affected one or a group of shift registers, one or a group of chips, and one or a group of memory planes. Transistor failure rates of 5×10^{-9}/hour and 1×10^{-8}/hour were used for discrete and integrated circuits, respectively. A failure rate of 6×10^{-8}/hour was used for pulse transformers. The failure rate of sensors, control lines, and interconnections was calculated to be negligible compared to the failure rates of the associated electronics.

Statistically valid failure rates for bubble domain devices are not yet available. Therefore, the analysis was conducted as a parameter study to find what the bubble device failure rate had to be in order to obtain a specific reliability. The bubble generators, splitters, switches, and annihilators are more complex than a shift register cell, so a ten times larger failure rate was assumed for them. For a cell failure rate of 5×10^{-13}/hour, half of the failures in a simplex organization (no error correction) were due to the magnetics, i.e., for smaller cell failure rates, the reliability becomes limited by the electronics. Results are also presented for cell failure rates of 5×10^{-12}/hour and 5×10^{-11}/hour, which brackets the failure rates of cores ($\sim 10^{-11}$/hour). Larger cell failure rates give unusably small reliabilities.

The errors caused by all the various component failures with the SbEC/DbED code were determined and five sub system reliabilities were established. These reliabilities were B, for a plane of bubble chips; S, for 16 shift registers in the same word on the 16 chips of a plane; X, for the translator; A, for the bus connections and W, for the memory connections. Each sub assembly contains N = 6 planes plus $ standby spares. The sub-assembly reliability $r_{N+\$}$ and the 10^8-bit memory reliability $R_{N+\$}$ are, where L = 128 is the number of

$$r_{N+\$} = \sum_{i=0}^{\$} \binom{N+\$}{i} B^{N+\$-i} (1-B)^i \sum_{j=0}^{E} \binom{LN}{j} S^{LN-j} (1-S)^j H_j + \binom{N+\$}{\$+1} B^{N-1} (1-B)^{\$+1} S^{L(N-1)}$$

$$R_{N+\$} = AX\left(Wr_{N+\$}\right)^{16}$$

shift registers per chip and H_j is the survival probability of the store given j shift register failures.

Figure 3 has three curves for R_7 for three assumed values of the failure rate of a cell in a bubble shift register -5×10^{-13}, 5×10^{-12}, and 5×10^{-11}. For further comparison purposes the reliabilities of two other organizations are given; a straightforward simplex organization, and the ultimate system where an extra spare plane is provided and the translator is put into bubble technology. Both of these latter organizations assume the better cell failure rate of 5×10^{-13}. It can be seen that for cell failure rates $\leq 5 \times 10^{-12}$, reliabilities for a 24-month mission will be in the 75-92% range.

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