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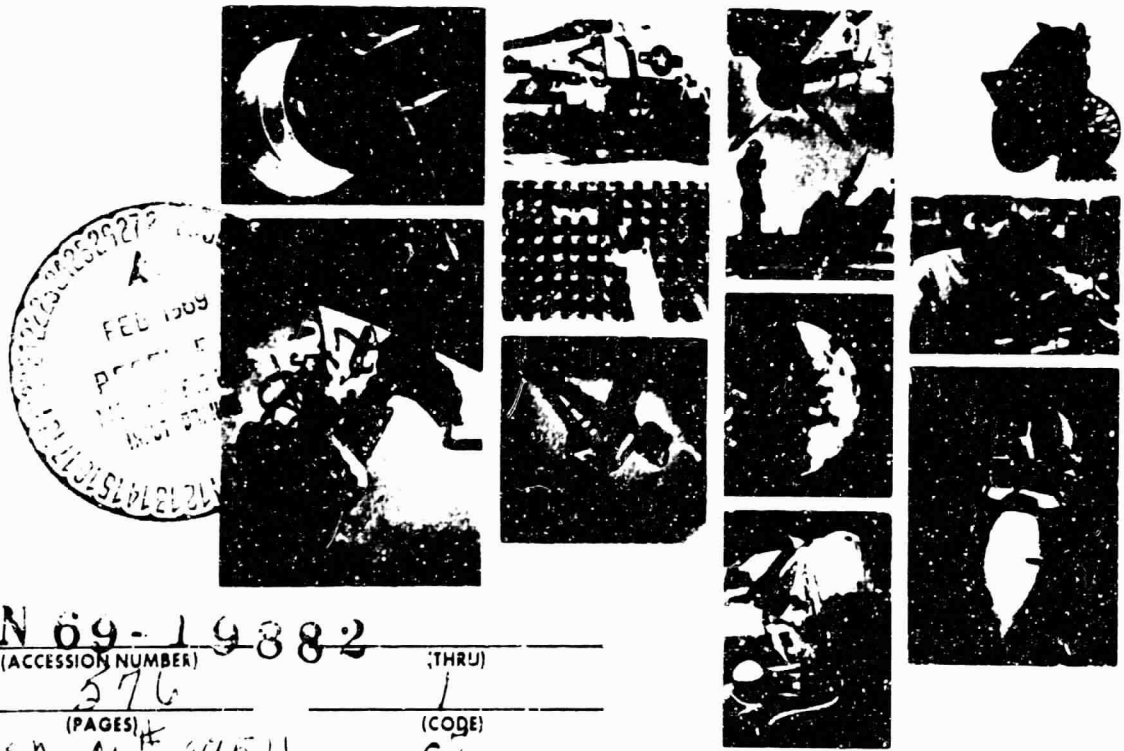

VOLUME II

NASA CR 99511

FINAL REPORT

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ADVANCED S-BAND TRANSPONDER STUDY PROGRAM

PREPARED FOR

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MOTOROLA . Government Electronics Division

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VOLUME II

ABSTRACT

This report presents the details of an Advanced S-Band Transponder Study Program, which was performed under contract to NASA (NAS-9-7483). During this program several block diagram configurations were studied and a simpler and much more flexible configuration was developed. A breadboard model of the new transponder was tested and proven to be feasible. Several closely related theoretical studies were also completed. This report includes the results of the analyses, the details of the breadboard design, and the measurements taken. A highly condensed version of the Final Report is presented in Volume I for readers who do not have the need or the time to read the detailed report presented as Volume II.

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SECTION I
INTRODUCTION

1. GENERAL

This document comprises Volume II of the final report documenting the work performed under NASA Contract NAS-9-7483. Volume I provides a brief summary of the entire project and Volume II gives a detailed description of each part of the study.

The study includes analysis and circuit investigation directed toward improved performance of the Apollo S-band system for future missions. A new transponder configuration was conceived, studied, and tested in a breadboard system and proven to be feasible and free from serious fundamental problems. The new configuration has much greater flexibility and usefulness than previous systems.

The Statement of Work defining the contractual requirements of the study is included as Appendix A of this report.

1.1 TASK DEFINITION

The project was divided into five major tasks to fulfill the program objectives. These tasks are defined below.

Receiver Task

1. Optimize the block diagram configuration.
2. Operational range extension.
3. Circuit development.

Transmitter Task

1. Increase power output (solid-state).
2. Improve modulation performance.
3. Improve reproducibility of RF circuits.

Analysis Task

1. Recommendations for future systems in terms of phase lock loop and modulation techniques to give improved performance.
2. Changes to the existing Apollo Unified S-Band (USB) system which could be made to give improved performance with minimum changes to current equipment.

Reliability Study

1. Comparison of stress analysis and reliability estimate with present USBE transponder.
2. Redundancy (active and standby) and the advantages of each as applied to the transmitter.
3. Parts procurement policy based on Military ER (Established Reliability) Specifications.
4. Failure mode and effect, stress, and computer circuit tolerance analysis with respect to future hi-rel transponders.

Packaging Analysis of a Phase Lock Loop Transponder

1. Environmental Considerations
2. Packaging Techniques
3. Structural Design
4. Shielding and housing requirements

1.2 TRANSPONDER

The Advanced S-Band Transponder differs in several ways from previously used similar transponders. The advanced transponder in its complete form has several distinct advantages over previous comparable equipment. The most significant advantages are listed on the following page.

1. Higher efficiency as to power consumption

2. Reduced size and weight

3. Increased flexibility as to frequency, power output, modulation bandwidth, and transponder ratio.

4. Lower cost.

Most significant, it is anticipated that a transponder of this basic design would be sufficiently flexible to allow its use in many different programs with only very slight special modifications. For example, a change in input frequency, output frequency, or transponder frequency ratio requirements would not necessitate a redesign of the transponder, but would only require changes in crystal frequencies and multiplier and divider ratios.

The salient features of this transponder design are tabulated below:

Salient Features	Advantages
1. Single Conversion Receiver Offset Oscillator	Mechanization much simpler, improved reliability, reduced spurious modes, easily adapted to center frequency changes, adapts easily to applications not requiring coherent reception.
2. Receiver has S-band preamplifier	Greater potential for improving noise figure by taking advantage of advances in the state of the art. Less sensitivity at the intermediate frequency.
3. Receiver has automatic acquisition circuitry	Shorter acquisition time, decreased stress on phase lock loop during acquisition.

	Salient Features	Advantages
4.	Coherent drive to transmitter provided by frequency synthesizer (synchronizer)	Allows greater flexibility in terms of transponder frequency ratio and center frequency, adapts readily to system not requiring coherent reception or coherent re-transmission.
5.	X32 frequency multiplication to obtain output frequency	Allows mechanization with simple X2 multipliers which can be wideband, stable, and do not need idlers.
6.	Phase modulator at 1/4 output frequency	Provides low distortion in wide bandwidth.
7.	Power amplification at 1/2 output frequency	Eliminates high order multiplication of high power signals, reduced size, improved modulation response, high solid state power output.

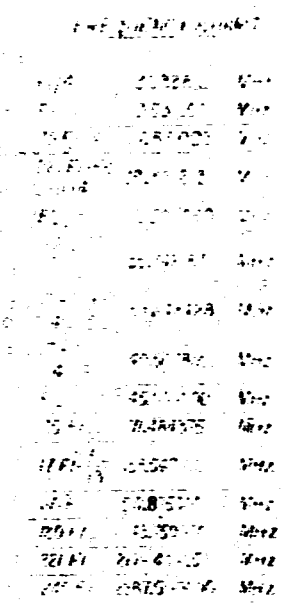
A block diagram of the transponder is shown in Figure 1-1. The diagram shows the division of receiver, synthesizer, and transmitter. Each large block in the diagram represents a module in the physical system as it was fabricated in the breadboard system. Power supply voltage and current requirements are shown for each module as well as signal power levels and frequencies.

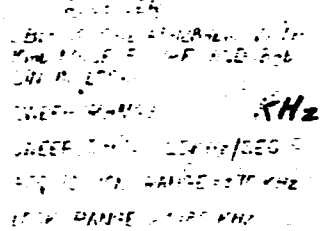
1.3 TRANSPONDER SPECIFICATIONS

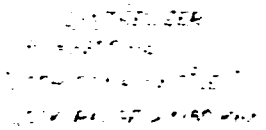
Some of the basic performance factors of the transponder are listed below. The measured values given in this list were measured on breadboard modules developed during this program.

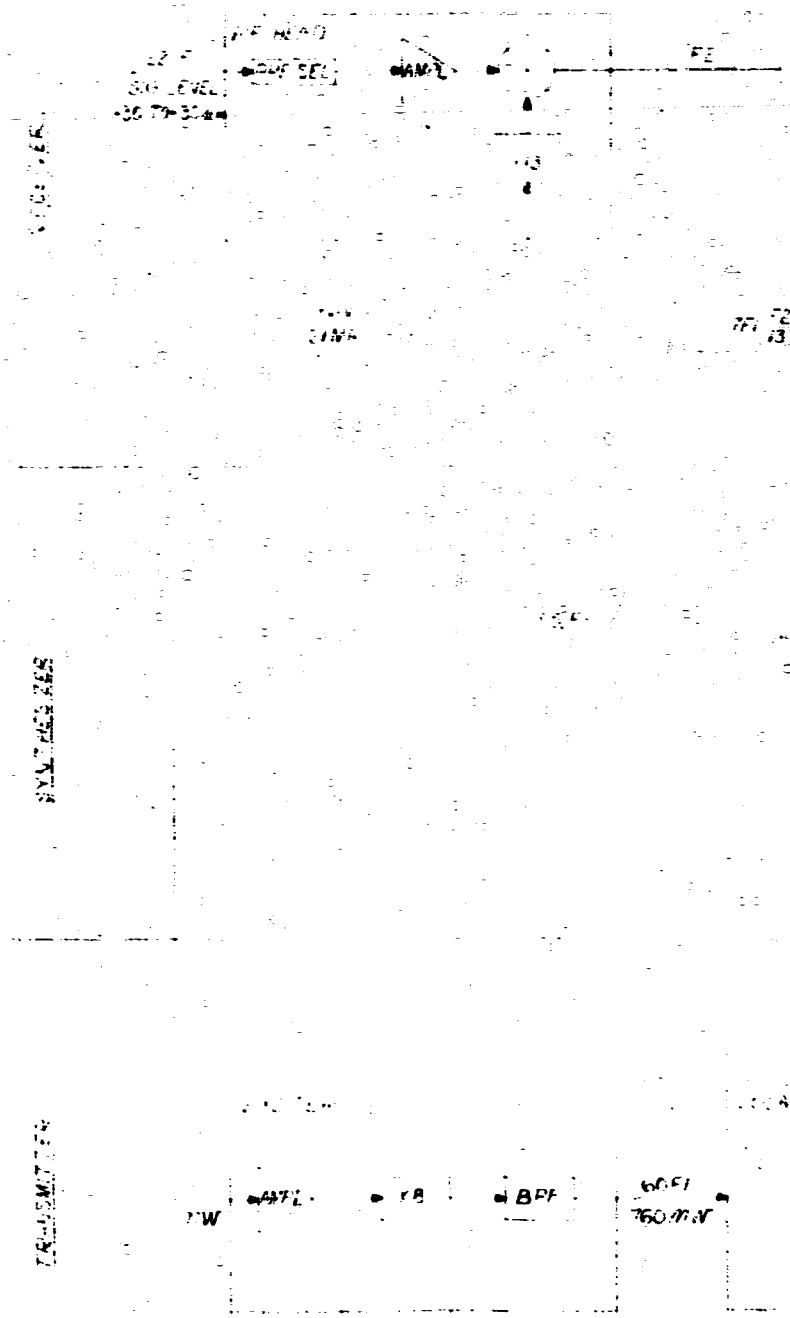
Frequency

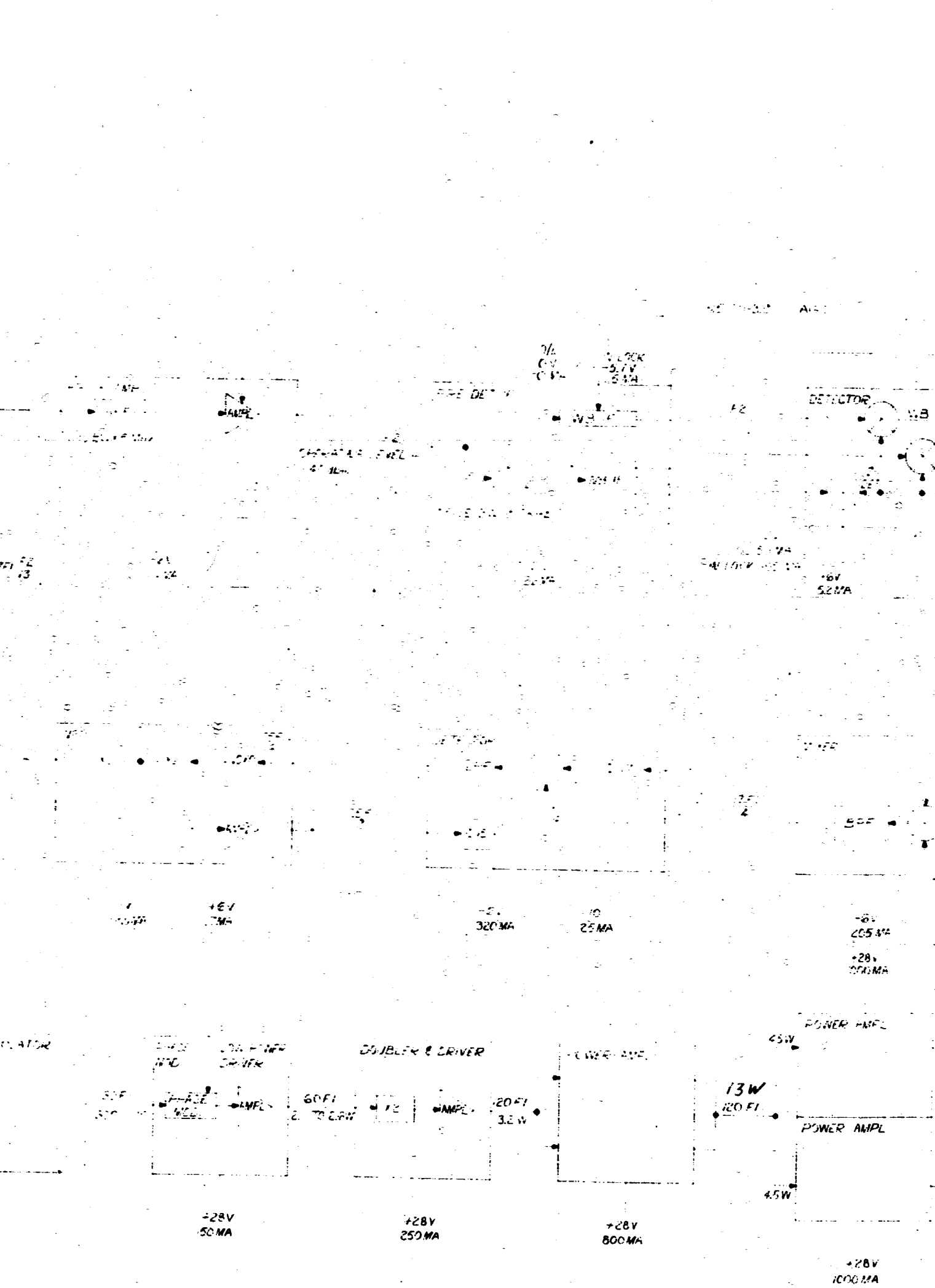
Received	2106.40625 MHz
Transmitted	2287.5 MHz (240/221 transponder ratio, Apollo Block II frequencies)










DETECTOR
+6V
5.2MA
-6V
265 MA
+28V
200MA
POWER AMPL
45W
13W
120 FT
POWER AMPL
4.5W
DOUBLER & DRIVER
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120 FT
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+28V
250MA
+28V
800MA
+28V
1000MA

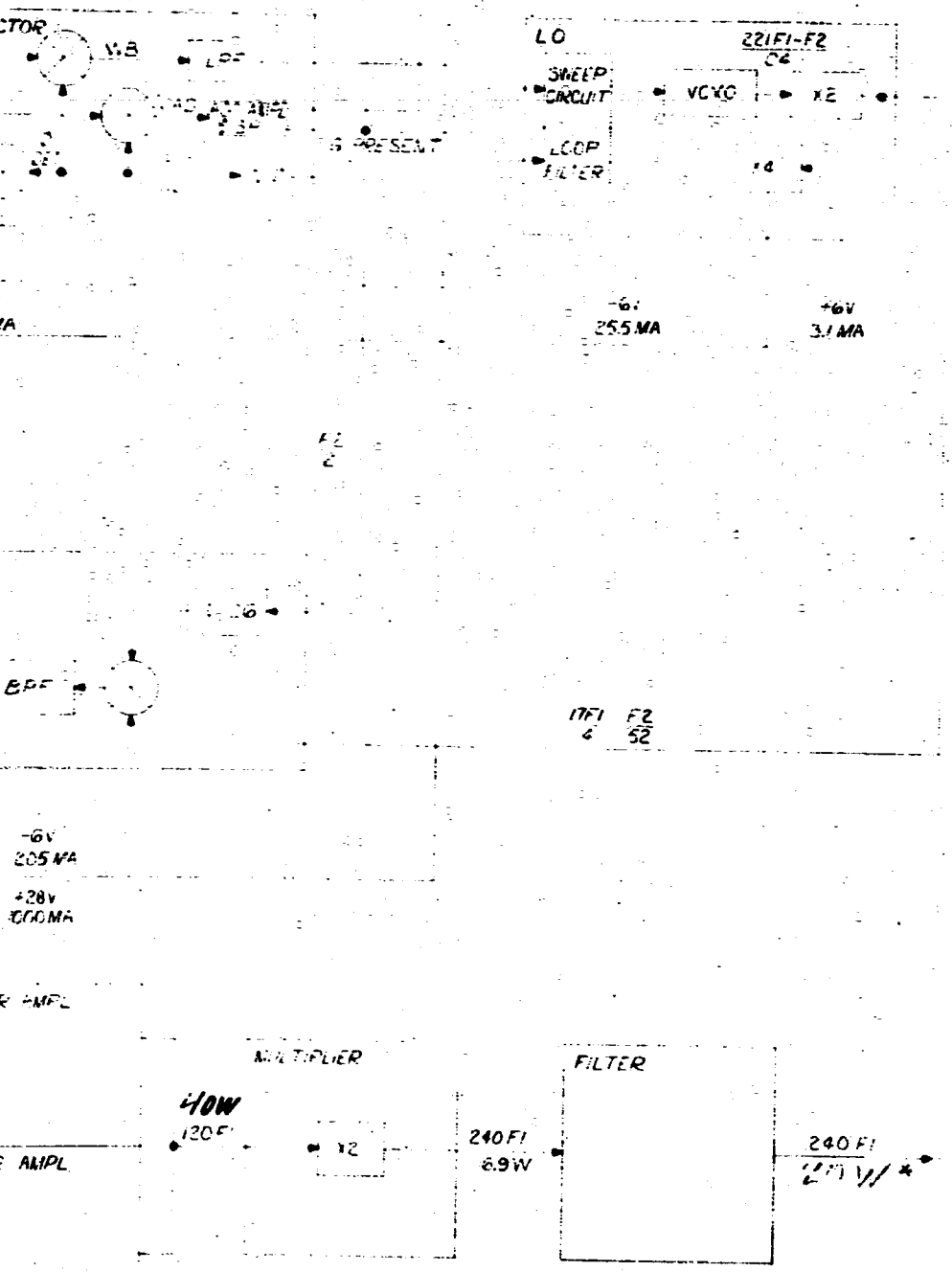

Figure 1-1.
ADVANCED S-BAND TRANSPONDER

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*Power levels are nominal design goal values.

Noise Figure	Design Goal 6 db Measured Value 8 db
Power Output	Design Goal 20 watts nominal Measured Value 13.7 watts
Dynamic Range	-40 dbm to -127 dbm
Phase Lock Loop Bandwidth ($2B_{LO}$)	1000 Hz at -127 dbm with +6 db S/N in the loop (the point of optimization)
Acquisition	By internal automatic sweep Acquisition time less than 6.5 seconds at -127 dbm.
Wideband Output Bandwidth	800 Hz to 2 MHz at baseband
Modulation Bandwidth (Baseband)	Design goal 100 Hz to 10 MHz Measured 60 Hz to 3 MHz
Power Consumption (less power supply loss)	Transponder in Sweep Mode, 1 watt Transponder in Receive Mode, 1.3 watts Transponder in Transpond Mode, 130 watts

1.4 BREADBOARD TRANSPONDER

A complete electrical breadboard transponder, except for the power supply, was assembled. The objective in building this breadboard was to prove the feasibility of the block diagram and verify the soundness of the transponder configuration.

The breadboard transponder was constructed using a combination of circuit construction techniques. These are listed as follows:

1. Multi-chip hybrid circuits
2. Monolithic integrated circuits

3. Discrete component circuits

4. Distributed constant stripline circuits

The breadboard construction uses conventional discrete component circuitry in many cases where the engineering model is proposed to use a far greater number of integrated circuits, therefore the breadboard model is physically larger than the proposed engineering model. A photograph of the breadboard transponder is shown in Figure 1-2.

The results of the breadboard construction and testing are briefly summarized as follows:

1. The proposed block diagram was proven feasible and free from serious fundamental problems, such as spurious lock modes and coherent leakage. This opens the door to the much greater flexibility and usefulness inherent in the block diagram.

2. An S-band RF preamplifier proved practical to provide performance comparable to existing diode converters. This approach, however, holds a reasonable promise of providing lower noise figures as better devices become available.

3. A multi-chip hybrid phase detector was designed with better than 50 db balance and high adaptability, complete in a TO-5 type package.

4. Monolithic linear amplifiers were investigated for the 45 MHz RF amplifier use. It was clearly established that there are still no units available which offer a significant practical advantage over discrete component type amplifiers. This is because the monolithic units available require external discrete components for biasing, bypassing and tuning and result in no real advantage over the total discrete approach.

5. Multi-chip hybrid amplifiers, limiters and AGC attenuators were designed for use in the receiver. Each of these circuits was designed to be complete

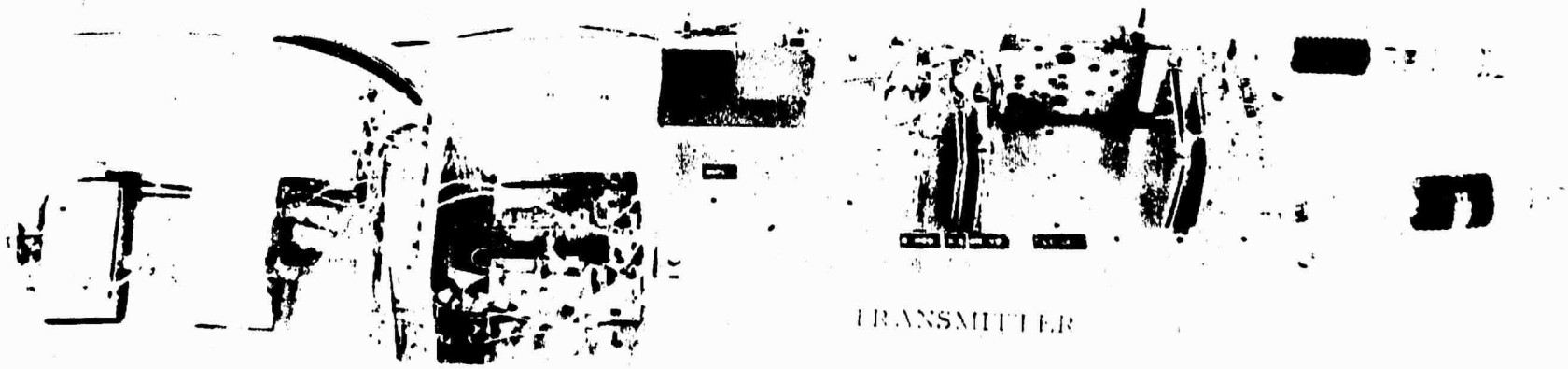


Figure 1-2. Breadboard Transponder

in itself, requiring no external components. These circuits performed well and were shown to have considerable advantage over discrete amplifiers, or monolithic devices. Also these circuits are versatile and have the potential of being used in several applications throughout the receiver.

6. The state-of-the-art in crystal oscillator noise, including the associated measurement technology, was reviewed. Existing Motorola equipments were shown to be as good as any in the industry.

7. The digital frequency synthesizer, was designed and tested. Measurements were made proving that the basic scheme does not significantly degrade phase noise performance.

8. A stripline phase modulator operating at 560 MHz was designed and tested. Measurements were made that showed great improvement in linearity and bandwidth over existing equipments.

9. Power amplification at S-band was investigated. Test results showed that devices were not capable of giving required performance at this time.

10. A power amplifier operating at 1.1 GHz was designed using 4 transistors in parallel with 25 watts output, with collector efficiency greater than 45%, and 4.5 to 5 db gain. Improvements in stripline construction techniques greatly improved the reproducibility and reliability of the amplifier.

11. A high power, dual device, varactor multiplier was designed to develop the output frequency and power. The device prototype exhibited an efficiency of over 60%.

12. The output bandpass filter was designed to relieve problems associated with corona which can occur during critical pressure. This design was an air stripline incorporating shorted quarter wave stubs to eliminate high impedance points.

In general the performance of the receiver portion of the breadboard transponder was satisfactory. The transmitter modules by themselves gave satisfactory performance. During transmitter integration three major problems became evident. These were:

1. The power amplifier matching networks were very narrow band and thus restricted the modulation bandwidth.
2. Th power combining techniques used in the dual varactor multiplier presented an anomaly to the power amplifier and output filter that is unexplained at this time.
3. The actual thermal resistance of the power amplifier transistor (TRW type PT6694) was much higher than the value used for design. Thus the transistors were over stressed thermally.

1.5 ANALYSES SUMMARY

The analyses problems which have been considered fall into two broad areas. First, recommendations for future systems and second, changes to the existing Apollo USBE system which could be made to give improved performance. These analyses are summarized below.

1.5.1 Phase-Lock Loop Analysis

From the analysis, it may be concluded that to extend the capability of the phase lock loop to the utmost the following steps could be taken:

1. Use self acquisition
2. Narrow the bandwidth
3. Use Type II or Type III loop
4. Use envelope AGC instead of limiters

For missions out to lunar distances, a Type III loop is not necessary. For these missions, the choice of AGC or limiters is also not critical since only a db in

signal threshold is involved. The bandwidth can generally be chosen to optimize the acquisition time since signal to noise densities for these distances are quite high.

For planetary distances the phase lock loop could operate as a Type II with command switching to a Type III when high rate dynamics are expected. A more detailed discussion of Type II and Type III loops is given in Volume II of this report.

1.5.2 Modulation Analysis

The modulation analysis was concerned with the use of an all-digital format for a space transmission system. An all-digital communication system has a great deal to offer in future space missions. Digital systems can be made more efficient, are certainly more flexible, and allow encryption for security purposes. The digital format circumvents many of the nonlinear problems inherent to a linear system. There are many questions as yet unanswered with regard to system problems, but the overall prognosis seems excellent.

1.5.3 Antenna Analysis

By examining the implementation of the antenna tracking function the basic scheme was found to be a sequential lobing configuration. The problems attendant with this system lead to the recommendation of converting to a monopulse tracker. No change in the configuration of the transponder is required since the tracking information can be derived from the existing wideband phase detector. First analysis of these new functions leads to the conclusion that devices exist which can be used to meet the system requirements.

1.5.4 Turnaround Ranging Analysis

Removal of the uplink subcarriers from the turned around baseband by band rejection filtering in the vicinity of the subcarriers can bring about significant improvements in the present Apollo system without severely impairing the ranging.

Removing the subcarrier allows:

1. The use of video limiting, thus maintaining a constant modulation index.
2. The release of power which had been necessary to transmit the subcarriers.
3. The elimination of suppression of the ranging.
4. The reduction of linearity constraints on the system.

After removal of the subcarriers, a further improvement in the ranging is possible by proper low-pass filtering. A 5-pole chebyshev low-pass with a noise bandwidth of 700 kHz will improve the ranging signal by 2 db over the present system.

1.6 RELIABILITY SUMMARY

A reliability analysis was conducted during the design of the Advanced S-Band Transponder. Since the program objective was to investigate a general purpose, state of the art, transponder with no definite specifications, a maximum ambient temperature had to be assumed for the purpose of performing a reliability estimate.

The results of the stress analysis and reliability estimate are discussed and a comparison made with that of the present USBE Transponder. The estimated failure rates of the USBE Transponder was 3.05%/1000 hours; of the advanced transponder, 1.5/1000 hours (with reasonable assumption of improved thermal resistance in the PA transistors). The effects of redundancy, active and standby, and the advantages of each as applied to the driver, power amplifier, and X2 multiplier modules of the transmitter are discussed. For example, the failure of only one transistor in the power amplifier would cause only a small drop in power output. When such an event is not regarded as a system failure, the realistic estimated failure rate is reduced much further. Military ER (Established Reliability) Specifications were the basis for the general parts procurement policy which is presented in the reliability section. Failure Mode and Effect, Stress, and Computer Circuit Tolerance Analyses are discussed with respect to the future development of a hi-rel transponder.

1.7 PACKAGING SUMMARY

The packaging task analyzed a composite of the environmental conditions and packaging requirements of the LEM, Apollo Block II, and Satrun IV-B Transponders. Methods of packaging a common transponder were studied and a compatible set of environmental conditions are given as a guide for the design of the advanced transponder.

A comparison of the operating and/or flight environment of the three existing transponders and of these general mounting provisions indicates that, with the exception of the thermal environments, there is sufficient similarity in the specifications to allow making a worst case composite without imposing any undue restraints on the electrical design.

Thermal environments presented a problem on past programs because of the various derating policies that were imposed on the three existing systems. The most realistic solution appears to be to use the LEM derating policies as a design guide.

Preliminary estimates, based on the breadboard transponder, indicate that there will be no problem in adapting the advanced transponder to any of the three envelopes specified for the existing transponders. Most of the effort in packaging has been expended in developing techniques that will allow a modular configuration that will adapt to almost any configuration. The proposed engineering model receiver is packaged in five basic modules and the transmitter in seven basic modules. Additional modules could be added as required to provide other functions and the output power of the transmitter could be varied by minor changes in the design.

1.8 CONCLUSIONS AND RECOMMENDATIONS

1.8.1 Conclusions

1. The transponder configuration is feasible and entirely practical.
2. The transponder configuration offers a significant improvement in reliability and flexibility.

3. The advanced transponder is physically adaptable in terms of size and weight to the applications of Apollo Block II, LEM, and Saturn IV-B Transponders.

4. The mechanization of the phase-lock loop can be changed to give the required performance for a given mission.

5. The multi-chip hybrid RF circuits worked well, are versatile, and are relatively inexpensive.

6. The stripline techniques developed proved to be reliable and reproducible.

7. Power amplification at frequencies above 500 MHz are practical but levels are limited by available devices.

1.8.2 Recommendations

1. An engineering model of the transponder be developed based upon the concepts and techniques of the study.

2. The results of the phase-lock loop analysis be implemented and evaluated.

3. The single channel monopulse antenna pointing scheme be implemented and evaluated.

SECTION II
RECEIVER

2. RECEIVER

The receiver problems that have been considered, fall into three broad areas: First, the block diagram configuration; second, range extension; and third, circuit development. For this report the block diagram study is contained in its own paragraph, range extension is a part of the r-f head paragraph, and circuit development is contained throughout the entire receiver section.

The results of evaluation of the receiver are presented in Section VII of this report. Selected test results are contained in the module descriptions.

2.1 RECEIVER BLOCK DIAGRAM ANALYSIS

At the beginning of this study program, one of the early steps was to perform a block diagram analysis in hopes of creating an optimum block diagram configuration. This study was directed toward the finding of an optimum block diagram (i.e. frequency scheme) for a complete transponder, capable of coherent receive and transmit operation. This study did not specifically include consideration of the transmitter, except to the extent that the transmitter configuration might be constrained by the receiver providing the coherent excitation. The most obvious transmitter performance limitations had to be taken into account to the extent that they appear important in determining the optimum receiver configuration.

The receiver is required to perform the following basic functions:

1. Receive and demodulate an S-band phase modulated carrier.
2. Provide an output signal for control of an associated transmitter in such a way as to insure that the transmitter output carrier is coherent with the received carrier at the prescribed ratio. The prescribed ratio of transmit to receive frequency is 240/221.

3. Provide a switching signal output which indicates whether the receiver is or is not phase-locked to an incoming r-f signal.

The above functions were defined in a broad manner to avoid, as much as possible, the exclusion of any workable techniques of achieving the desired objectives. The basic performance requirements (such as sensitivity, bandwidth, etc.) were generally considered to be comparable to their counterparts on the Apollo Block II CSM transponder. The a-m detection used in Block II for r-f antenna track was (for the purposes of this block diagram study) considered to be unnecessary. Automatic acquisition was considered to be a separate subject and therefore was not considered strongly in selecting the optimum block diagram.

Various block diagrams have been considered in the interest of finding one which offers an optimum combination of advantages. It must be recognized that such an evaluation is necessarily highly subjective and it is not reasonable to expect that a particular configuration can be shown to possess all of the desired characteristics. This section describes the most important considerations used in comparing block diagrams. It further describes the general block diagram which was selected as best suited for the goals of this project, and discusses the important considerations upon which it depends and the problem areas. Alternate configurations and their most important aspects are then discussed.

2.1.1 Block Diagram Considerations

At this time, the exact applications of the equipment are not very specifically known. Consequently, the relative weighting of the considerations could not be accurately assigned and will still be subject to variations as required by future needs. The aspects which seem to be most significant are listed below with a brief explanation of each, but not necessarily in the order of importance.

1. Simplicity - This implies high reliability, few parts, low cost, small size, and low power consumption in comparison with the present day equivalent.

2. High Performance - This implies high sensitivity, efficiency, low distortion, fast acquisition, minimal spurious responses, and rugged mechanical design.

3. Channel Flexibility - This implies that a minimum of differences in parts and adjustments exists between units for different channels, so that units may be manufactured simultaneously for different channels, with relatively minor differences between them. At this time there has been no attempt to devise a scheme for making a single unit capable of switching between channels by means of a control panel. Though it is possible to do it, the requirement for such a multichannel unit is not evident at present. It is attractive however, to minimize the number of individual parts (such as modules) which must necessarily be different for different channels.

4. Ratio Flexibility - It is desirable to have a system which is adaptable to either the 205/256 (SGLS) transponder ratio or the 221/240 (DSIF) ratio. Here, the hope is that many of the parts (such as modules) could be usable in transponders of either ratio. Furthermore, it is desirable to have the capability of configuring the same parts in a transponder of inverse ratio - that is, a transponder which has the transmit and receive frequencies interchanged so that it can operate in two way communication with the normal transponder.

5. Flexibility for Non-Coherent Operation - There may be applications for receivers where there is no need to operate with a coherent transmitter. It is desirable to have a block diagram scheme which can take advantage of such a simplification in requirements.

6. Low Power Consumption - It is particularly important to minimize power consumption in the receiver since it normally operates for long periods compared to transmitter operating times.

7. Minimum Size and Weight - Obviously, it is very important to work toward reduced size and weight.

8. Assumed Advance in the Art - Since it is not required that the equipment be developed immediately, it is reasonable and necessary to anticipate advances in the state-of-the-art.

2.1.2 Receiver Block Diagram

A block diagram of the final receiver system and synthesizer is shown in figure 2-1. A more detailed block diagram of the complete transponder is given in figure 2-1. The frequencies and ratios indicated on the block diagram represent this particular implementation. Related to this scheme, one can readily visualize, there are many other minor variations which are worthy of consideration in the event of a design for a specific application. The distinguishing features of the block diagram are:

1. S-band amplification of the received signal.
2. Single conversion superheterodyne.
3. Reference oscillator is not coherent with respect to the received frequency.
4. No AGC system.
5. Coherent drive is not a direct output of the receiver.
6. Automatic acquisition.

Number (5) above may seem to be in opposition to the requirements, but sufficient information is present in the two receiver outputs to enable the generation of coherent drive for the transmit signal. The circuitry to perform this conversion can be considered separately from the receiver. For the purposes of this report, the device for performing this conversion is referred to as a synthesizer. In a final version of this system, the synthesizer could logically be part of the receiver, a separate unit, or part of the transmitter. In any case, it is needed only during coherent transmission, and therefore should not have power applied except during coherent transmitter operation.

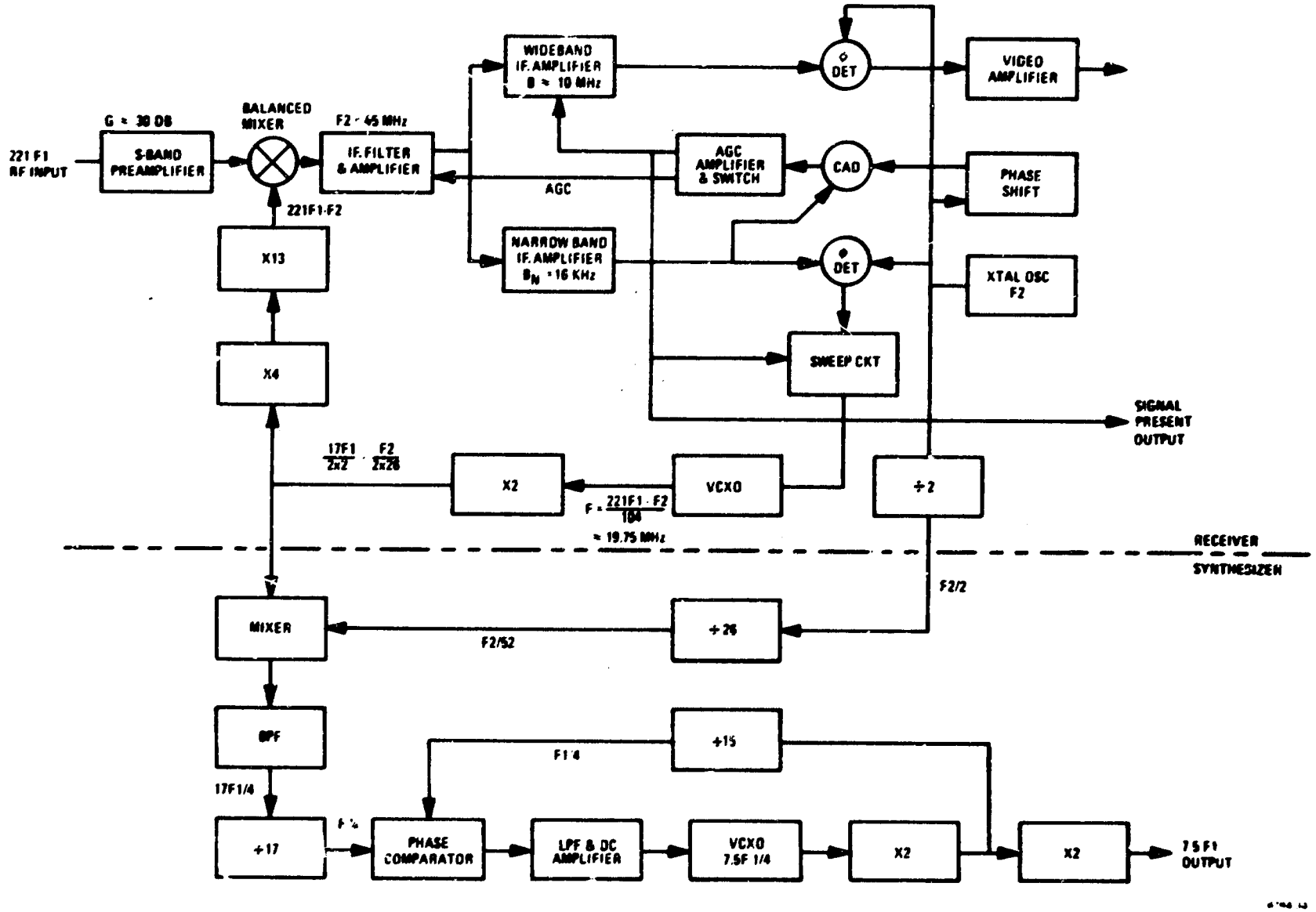


Figure 2-1. Block Diagram of Receiver and Synthesizer

What are the advantages of the proposed system in comparison with previously used similar systems. This question is best answered by showing the advantages which accrue from each of the distinguishing characteristics previously pointed out.

2.1.2.1 Advantages of the Block Diagram Configuration

The use of S-band amplification has two significant advantages. First, it holds the promise of an improved noise figure; and second, it enhances the practicability of using single conversion. With the transistors available today, there is reason to expect a room temperature noise figure as low as about 5.5 db. With a microwave mixer at the input, a room temperature noise figure of 5.5 db is again about the best. It seems unlikely that there will be very much improvement in the mixer noise figure whereas a steady improvement down to about 2 db for an S-band amplifier seems reasonable as the device technology continues to advance. When an r-f amplifier is used, it is possible to obtain r-f selectivity with negligible increase in noise figure, whereas with a mixer type front end, all preselector losses add directly to the noise figure.

It is stated above that the use of S-band amplification enhances the practicability of using single conversion. This is true because it reduces considerably the sensitivity required at the input to the first i-f amplifier. If single conversion were to be used without S-band amplification, it would be extremely difficult to prevent leakage of the phase detector reference into the first i-f amplifier. In general, the extra shielding complexity necessitated by such a system would more than compensate for the simplifications offered by single conversion.

Single conversion as compared with dual conversion offers a reduced number of parts and a reduced number of spurious responses. Also, since it involves a relatively high i-f. (45 MHz rather than 12.25 or 9.53 MHz, for example) it is much more amenable to high modulation bandwidths. Thus, a 10 or even 20 MHz modulation bandwidth would be practical with this receiver. In the proposed

receiver the i-f bandwidth is set primarily by the filter which follows the first mixer. Also, in this receiver, the i-f is a fixed frequency - that is, the i-f is independent of channel frequency or of doppler frequency shift in the received signal. Thus, any phase shift or time delay variations which might be a function of IF frequency are avoided.

The reference oscillator operates at a fixed frequency, independent of the channel frequency or frequency shift on the incoming signal. Thus, the phase shift in the predetection (crystal) filter does not vary with doppler shift as in some systems. This eliminates one source of error in phasing the reference signal for the wideband phase detector. This may be important since de-phasing of the wideband phase detector causes distortion and reduced output level in the video output. Another important advantage is that no differences in parts or adjustment would be required in the i-f detector, or reference oscillator circuits for receivers operating with different channel assignments.

The coherent drive output is really two outputs from the receiver. It is shown in the block diagram as $\frac{17}{2X2}$ F1 - $\frac{F2}{26X2}$ and F2. The synthesizer circuitry for converting this into a useable coherent drive signal will now be discussed in more detail. Figure 2-2 shows conceptually the proposed synthesizer scheme. It will be seen upon examination that it consists almost entirely of digital circuitry. Thus, it is subject to a very high degree of miniaturization by use of commercially available monolithic integrated circuits.

2.1.2.2 New Development Areas

There are several aspects of the proposed receiver and synthesizer system which were considered to be problem areas at the outset, by virtue of the fact that the circuit techniques involved had not been perfected nor utilized in existing transponders. Consequently the R&D time and money required to put the newer techniques into effect is significant.

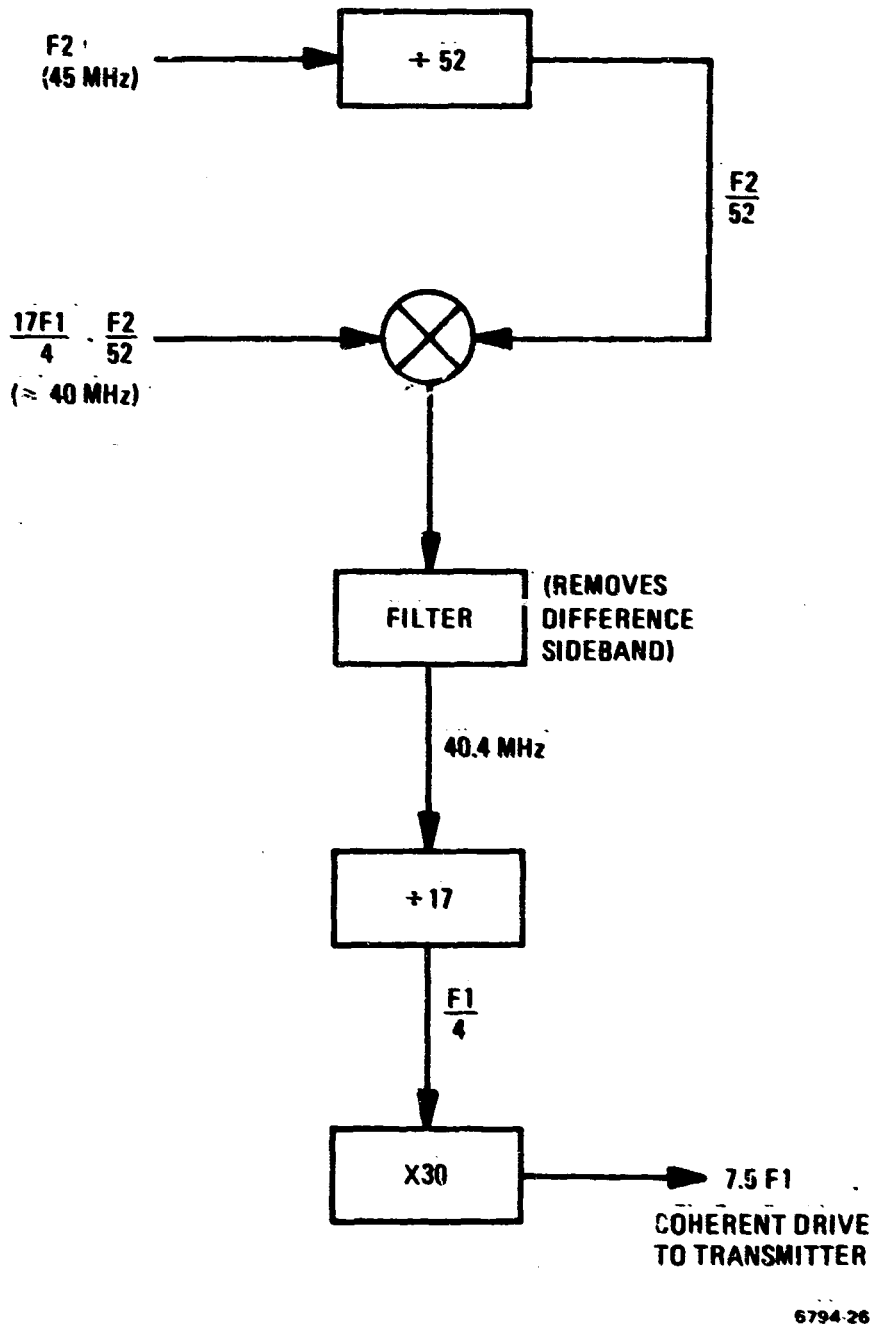


Figure 2-2. Proposed Synthesizer Block Diagram (Conceptual)

The major areas where new circuit development has been required are listed below:

1. S-band amplifier
2. Digital synthesizing circuits
3. 45 MHz crystal filter
4. 45 MHz phase detector
5. 45 MHz limiters (with highly stable phase characteristics)

These areas all represent relatively straightforward extensions of previously existing circuit technology.

Even though the digital circuitry is very attractive in terms of small size, low cost, and high flexibility, it has some rather severe limitations. The most formidable limitation is due to the basic antagonism between high speed and low power consumption. The MECL II series is the fastest commercially available digital integrated circuit series. Its power consumption is rather high - 300 mw for a J-K flip-flop which is capable of 120 MHz operation. Whereas a simple divide-by-two circuit using MECL II will work at frequencies up to 120 MHz, the more complex clocked divider circuits are limited to operation at some lower frequency between 50 MHz and 100 MHz.

2.1.3 Alternate Configurations of Receiver Frequency Scheme

2.1.3.1 Generalized Block Diagram

As stated earlier, the specific frequencies and multiplier ratios indicated are not the only means of obtaining the desired results with the general block diagram configuration. For convenience in discussion of alternate configurations, the block diagram is redrawn in figure 2-3 in a more general way. The multiplier and divider ratios are indicated by the literal symbols A, B, $\frac{(13)\,(17)\,M}{B}$, and R. There is a wide choice of values for each of these terms with the fundamental restriction that they must all be integers, and practical restrictions making only

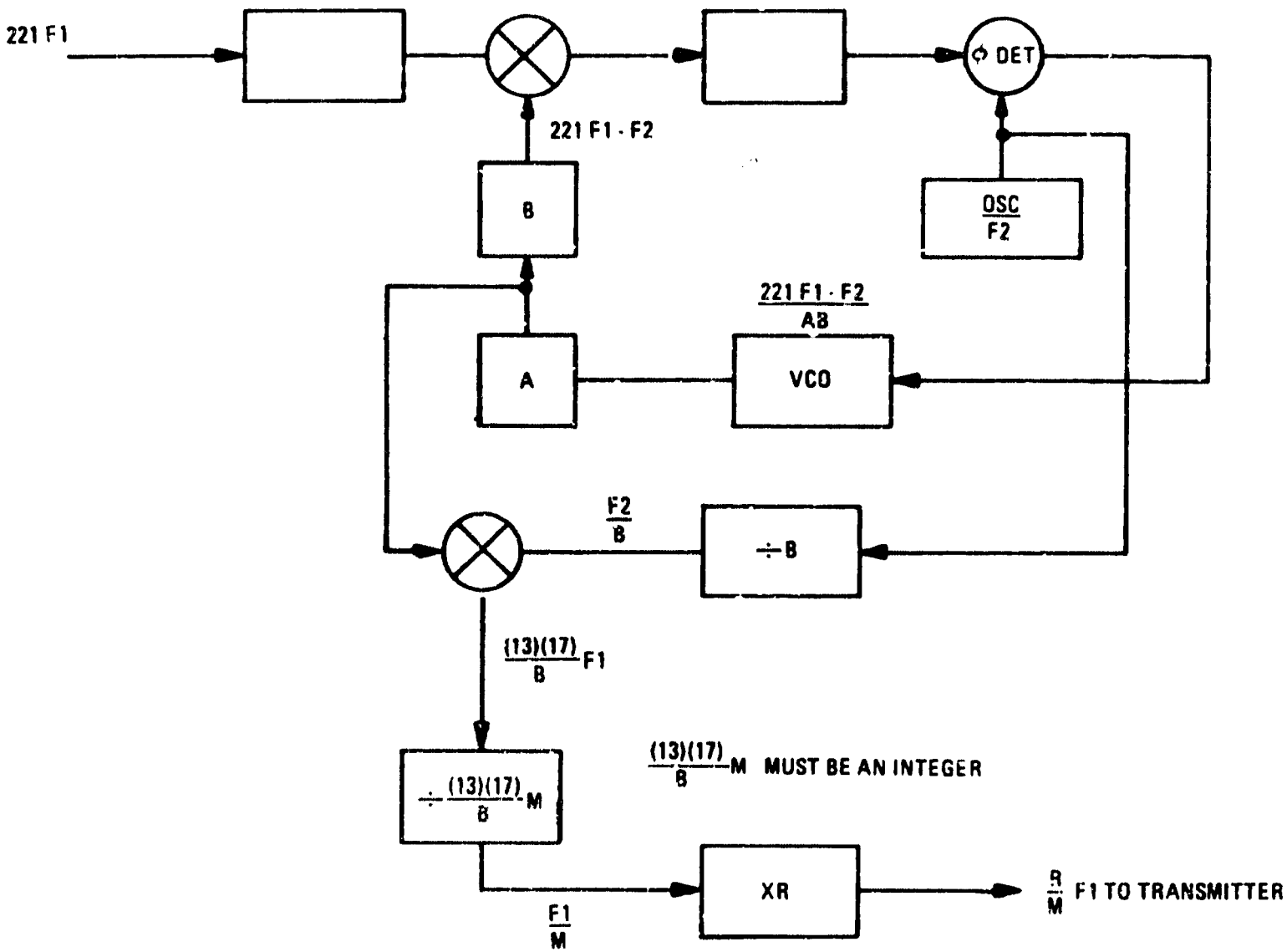


Figure 2-3. Generalized Receiver and Synthesizer

certain integers practical. The most restrictive integer is the divider ratio, $\frac{(13)(17)M}{B}$. For this ratio to be an integer, B must be evenly divisible into 13, 17, or M. With these and other practical restrictions, table 2-1 has been constructed showing the possible combinations of these factors. Note that the factor 13 appears in the B multiplier of every combination. This can logically be a step-recovery diode multiplier. There is another set of possibilities using 17 in the multiplier, but it has no advantage over this set. The divide-by-17 and the divide-by-13 circuits are common to all the schemes. There is a wide choice of frequencies at which to operate the digital circuitry. Clearly, the higher frequencies require more dc power and more critical techniques, whereas the lower frequencies consume less power but result in closer interfering sidebands and somewhat more complexity in the final frequency multiplier circuits. Another potential problem is that as the value of the final multiplier (R) is increased, there is a greater possibility of being effected by noise in the lowest frequency digital circuits.

In any of the schemes considered, the frequency of the digital circuitry can be reduced by using an analog type of divider preceding the digital circuits. There are several such dividers in common use today which can be used here. Such a modification, reduces the frequency of the nearest spurious sideband, and increases the required multiplication ratio at the output.

2.1.3.2 Inverse Ratio Transponder

An inverse ratio transponder might be used to operate in two way communication with a normal transponder. Thus, the transmit frequency would be 221F1 and the receive frequency would be 240F1. It is immediately apparent that there is some difficulty in converting the conventional scheme (such as the JIM or Apollo Block II) transponder to this ratio because of the fact that 221 is a product of the prime numbers, 13 and 17. These factors would be rather difficult to implement with efficient frequency multipliers. However, using the advanced transponder configuration, relatively slight changes from the recommended block diagram lead

Table 2-1. Possible Frequency Schemes

F2 = 45 MHz
F0 = 221 F1 = 2100 MHz
Coherent Drive = 10F1

No.	A	B	AB	VCO Freq. (MHz)	Div. Input Freq (MHz)	(13) 17M B	F1 M M (MHz)	R	F2 B (MHz)	Remarks
1	2X5	13	130	15.8	161.5	17	1 9.5	10	3.46	Frequency too high for practical digital circuitry (at this time).
2	5	2X13	130	15.8	80.7	17	2 4.75	20	1.73	Frequency at upper limit of digital capability - pushes the state-of-the-art with rather high power consumption.
3	1	2X5X13	130	15.8	16.15	17	10 .95	100	.346	Entirely feasible, but multiplication by R=100 requires many parts and may tend to limit noise performance.
4	3X3	13	117	17.6	161.4	17	1 9.5	10	3.46	Similar to 1.
5	3	3X13	117	17.6	53.9	17	3 3.16	30	1.15	Good, frequency range ok for digital circuitry, but near top.
6	1	3X3X13	117	17.6	[illegible]	17	9 1.05	90	.384	Similar to 3.

Table 2-1. Possible Frequency Schemes (cont)

No.	A	B	AB	VCO Freq. (MHz)	Div. Input Freq. (MHz)	(13) 17M B	M	$F1_M$ (MHz)	R	$F2_B$ (MHz)	Remarks
7	2	2X2X13	104	19.7	40.4	17	4	2.38	40	.87	Good - This is the recommended approach.
8	4	2X13	104	19.7	80.8	17	2	4.75	20	1.73	Similar to 2.
9	1	2X2X2X13	104	19.7	20.2	17	8	1.19	80	.432	Good, but does not push state-of-the-art. A few more parts than number 7.
10	8	13	104	19.7	161.6	17	1	9.5	10	3.46	Similar to 1.
11	3	2X13	78	26.4	80.6	17	2	4.75	20	1.73	Similar to 2 and 8.
12	6	13	78	26.4	162	17	1	9.5	10	3.46	Similar to 1.
13	1	2X3X13	78	26.4	27.0	17	6	1.58	60	.58	Similar to 9, but VCO frequency is somewhat high.
14	5	13	65	31.6	161	17	1	9.5	10	3.46	Similar to 1.
15	1	5X13	65	31.6	32.3	17	5	1.9	50	.683	VCO frequency too high.

to a suitable scheme for the inverse ratio system. Figure 2-4 illustrates the essential elements of the synthesizing system when configured for this purpose. Note that the preselector and local oscillator multiplier circuits operate in the same frequency range as in the original system (figure 2-1), thus the identical circuits could be used with retuning. The i-f and the detector circuitry is identical in both systems, and would be unaffected. The synthesizer circuitry is similar but would require all new digital divider circuits of slightly increased complexity. The factors of 160 are 2^5X5. Because of the 2^5 factor the divider could be relatively simple and take advantage of low power low speed circuits in places.

The block diagram includes a digital divide-by-221, but this may be superfluous. Initial analysis indicates that this multiplication by 221 can be done directly by comparing the phase of the input and output signals, even with a ratio of 221 between the signals. This is possible because of the high stability of a crystal controlled output (auxiliary) oscillator. If this does not prove feasible in the lab, then the divide-by-221 can be directly constructed using a divide-by-13 and a divide-by-17. These could be identical to the equivalent dividers in the normal-ratio-transponder of figure 2-1. There is an opportunity, however, to use low speed circuits for one, and high speed circuits for the other.

With this system the transmitter frequency multipliers can be products of 2 and 3. The indicated ratio of $3X2^3$=(24) is compatible with the original system, consequently if the tuning range can be made sufficient to operate in either level, the same transmitter design can be used with only retuning required.

As with the other system, there is a large family of possible multiplier and divider ratios for the inverse-ratio-transponder based on this configuration. A table similar to table 2-1 could be constructed but it is unnecessary at this point. The most interesting point is that the design of the inverse-ratio-transponder requires very small design differences from the normal-ratio-transponder. Consequently, the development of either system would pay most (estimated 90%) of the cost of development for both systems.

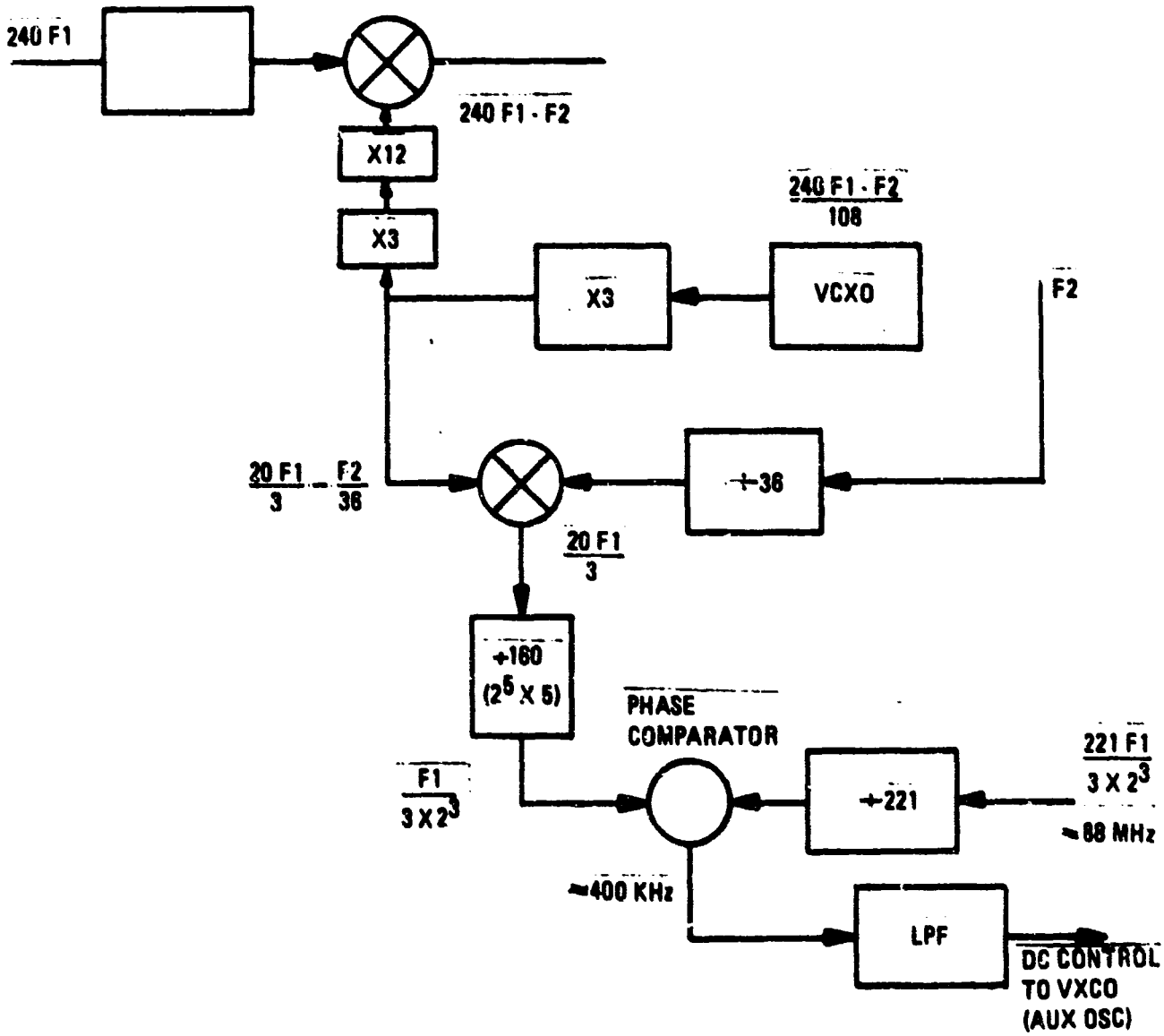


Figure 2-4. Frequency Scheme for Inverse Ratio Transponder

2.1.3.3 Other Transponder Ratios

The frequency scheme has been shown for transponder ratios of 221/240 and 240/221. An important feature of the recommended scheme is that it is very adaptable to other ratios. For any ratio, the same i-f and detector circuitry can be used unchanged. The other circuitry - the vcxo, the frequency multipliers, the preselector, and the synthesizer will require minor modifications for the changed operating frequencies. Generally, these modifications would be in the nature of component value changes, except for the digital circuitry. Here, the change would be mainly a new interconnection of the same kind of integrated circuit elements.

A simplified block diagram of the system is shown in figure 2-5, as it could be configured to operate with the SGLS ratio of 205/256. The synthesizer generates F1/4 and multiplies by 32 to generate 8F1 in the vcxo,. The 8F1 is then available for multiplication in the transmitter by 32 ($32 = 2^5$).

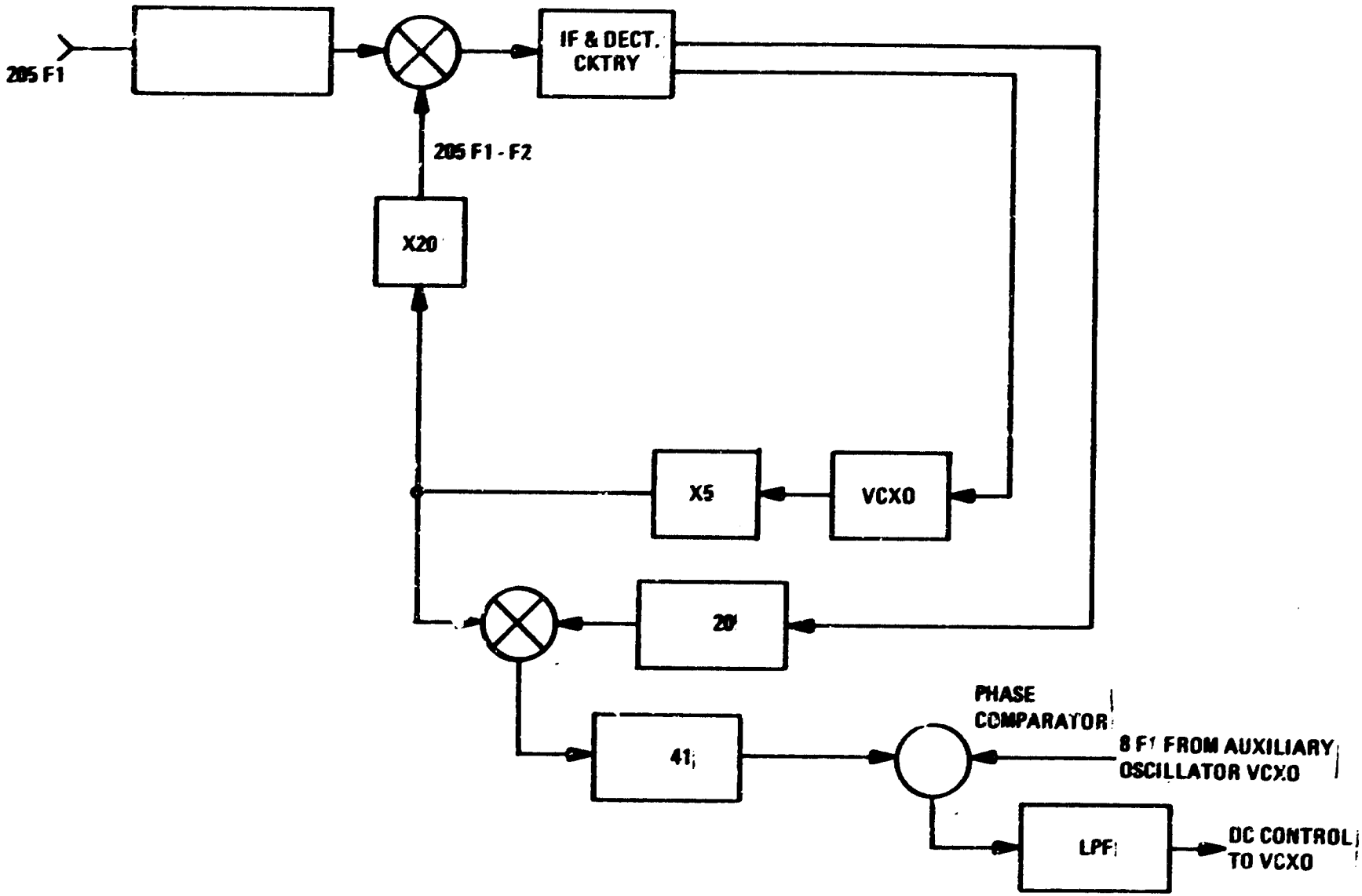


Figure 2-5. 205/256 Configuration

2.2 R-F HEAD

2.2.1 Introduction

The receiver proposed in this program includes an r-f head which is the receiving end of the receiver. This portion of the report describes work done to develope a workable breadboard unit. This enables the laboratory testing of the receiver design concept. Design goals are presented along with test results to verify the designs.

A discussion is included concerning the choice of the S-band amplifier and mixer. The results reflect the feeling of project engineers on the ultimate configuration to be used for future missions. This may mean that other configurations would perform better today but are expected to be replaced in the future.

2.2.2 R-F Head Requirements

The r-f head receives the 2106 MHz input signal, amplifies it, and converts it to a 45 MHz i-f frequency. This module has to supply the 2061 MHz LO signal to the mixer while receiving the coherent 159 MHz signal. This means a frequency multiplication of X13 has to be performed. The block diagram of the r-f head is shown in figure 2-6. Below are listed the design goals or specifications of this module.

1.	R-F Input Frequency for B/B Unit	2106 MHz
2.	Input Signal Range	+3 dbm to -130 dbm
3.	Input Impedance	50 ohms; vswr $\leq$1.3:1
4.	Input Noise Figure	<6 db
5.	R-F Bandwidth - -3db	20 MHz minimum
6.	Image Rejection	<-60 dbm input
7.	LO Feedthru	<-80 dbm

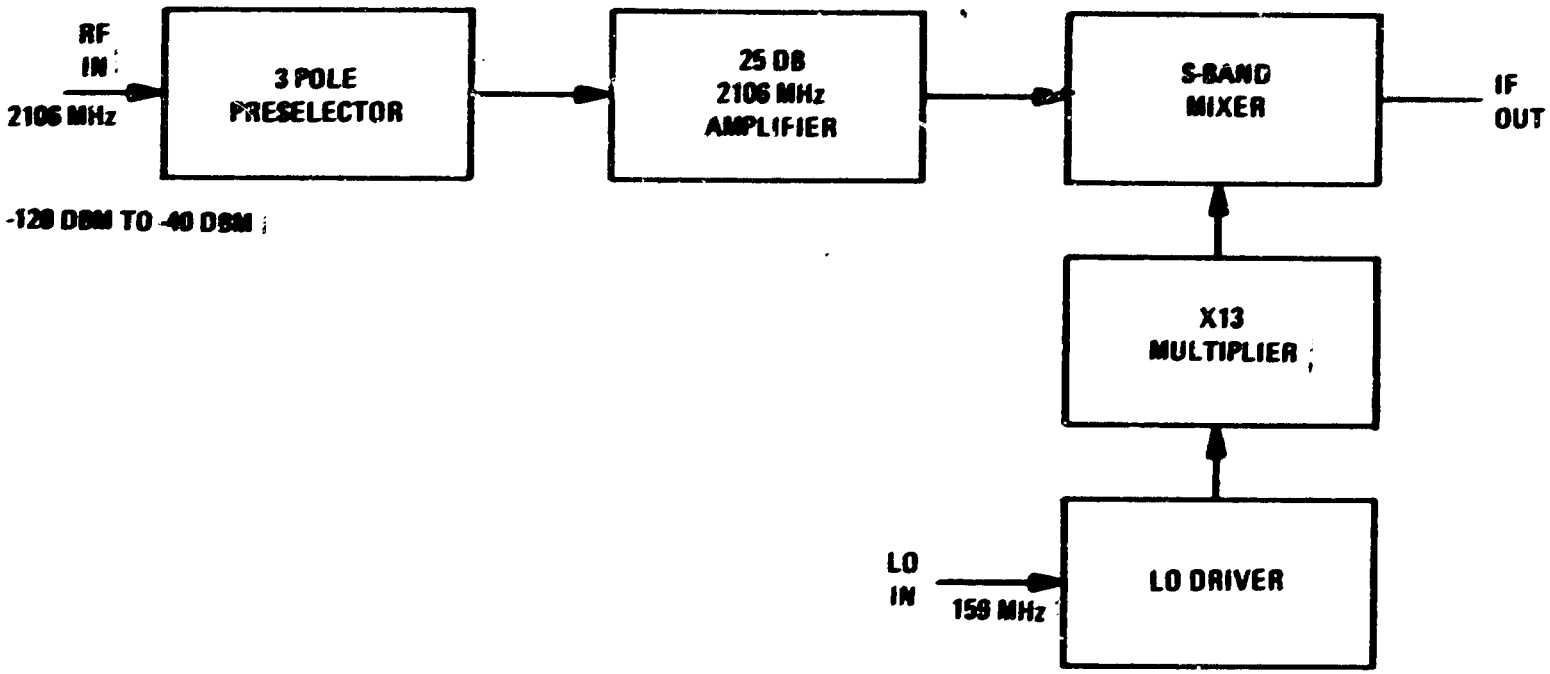


Figure 2-6. RF Head Block Diagram

8.	R-F Gain	<50 db
9.	LO Mult. Ratio	X13
10.	LO Input Impedance	50 ohms; vswr <1.3:1
11.	LO Input Power	-7 dbm ±3 db
12.	I-F Frequency	45.000 MHz
13.	Output Impedance	50 ohms; vswr ≤1.5:1
14.	Operating Temperature Range	-40°C to +80°C

2.2.3 Front End Configuration

The most difficult design goal to meet at this frequency is a low noise figure in the S-band amplifier. As expected, this block comprised most of the development effort.

There are various devices which can be used to amplify 2 GHz signals, such as: tunnel diodes, parametric devices, traveling wave tubes, and the newest, the transistor. In choosing the best type of amplifier for this application, factors such as size, weight, and power requirements must be considered. No specific objectives have been established at this time for such factors. However, it is known that size always becomes a limiting factor in space applications as more and more electronic hardware is desired in spacecrafts. Prime power, too, is usually limited to a minimal amount.

The lowest noise figure can be achieved with a parametric amplifier. However, it requires a pump source at a higher frequency. Since this would greatly complicate the amplifier and consume considerable power, the parametric amplifier concept was discarded. The next lowest noise figure device would be a tunnel diode amplifier. Such amplifiers, however, are known to have stability problems; especially at cold temperatures. A heater would therefore be required to operate at -40°C. Heaters, of course, consume large amounts of power. For example, one

manufacturer extends the temperature range of a 4 db noise figure tunnel diode-transistor hybrid amplifier from -10°C to -50°C using a 30 watt heater. Because of this temperature problem, the tunnel diode amplifier was not considered suitable for this application.

The only real choice left is the transistor. Advances in the state-of-the-art in transistor technology have produced transistors with up to 8 db gain and 4 db noise figure at 2 GHz. This noise figure, however, is for a germanium device. Since it would be difficult to operate germanium devices at +80°C, they are also considered unsatisfactory. Silicon transistors have advanced to the point where a 6 db noise figure and 7 db gain are possible. With such transistors, an amplifier noise figure of 7 db should be possible. A transistor amplifier can be built in a small volume and consumes little power. For these reasons, a transistor amplifier was decided on for the S-band gain needed. It is felt that this choice is still valid assuming that increasingly better transistors become available. Even though silicon transistors are inherently limited to operation below about 8 GHz, it should not be too much to expect that higher gains will be achieved at 2 GHz. Looking back at the progress made in past years, a noise figure of 4 db with a gain of 10 to 12 db seems likely for silicon transistors within two years.

2.2.4 LO Multiplier

2.2.4.1 Step Recovery Diode Multiplier

The X13 multiplier is achieved with a step recovery diode driven at 159 MHz. To eliminate the critical interface between diode and driving source at the module level, it was decided to incorporate a single stage amplifier-limiter in this module also. The schematic diagram is shown in figure 2-7.

Reference was made to Hewlett Packard application note #913 to design the multiplier. The combination of L4, C7, and C8 transforms the diode impedance to approximately 50 ohms. All harmonics caused by the varactor are kept inside the cavity filter by C9. The filter is tuned to the 13th harmonic and provides a low impedance to other harmonics.

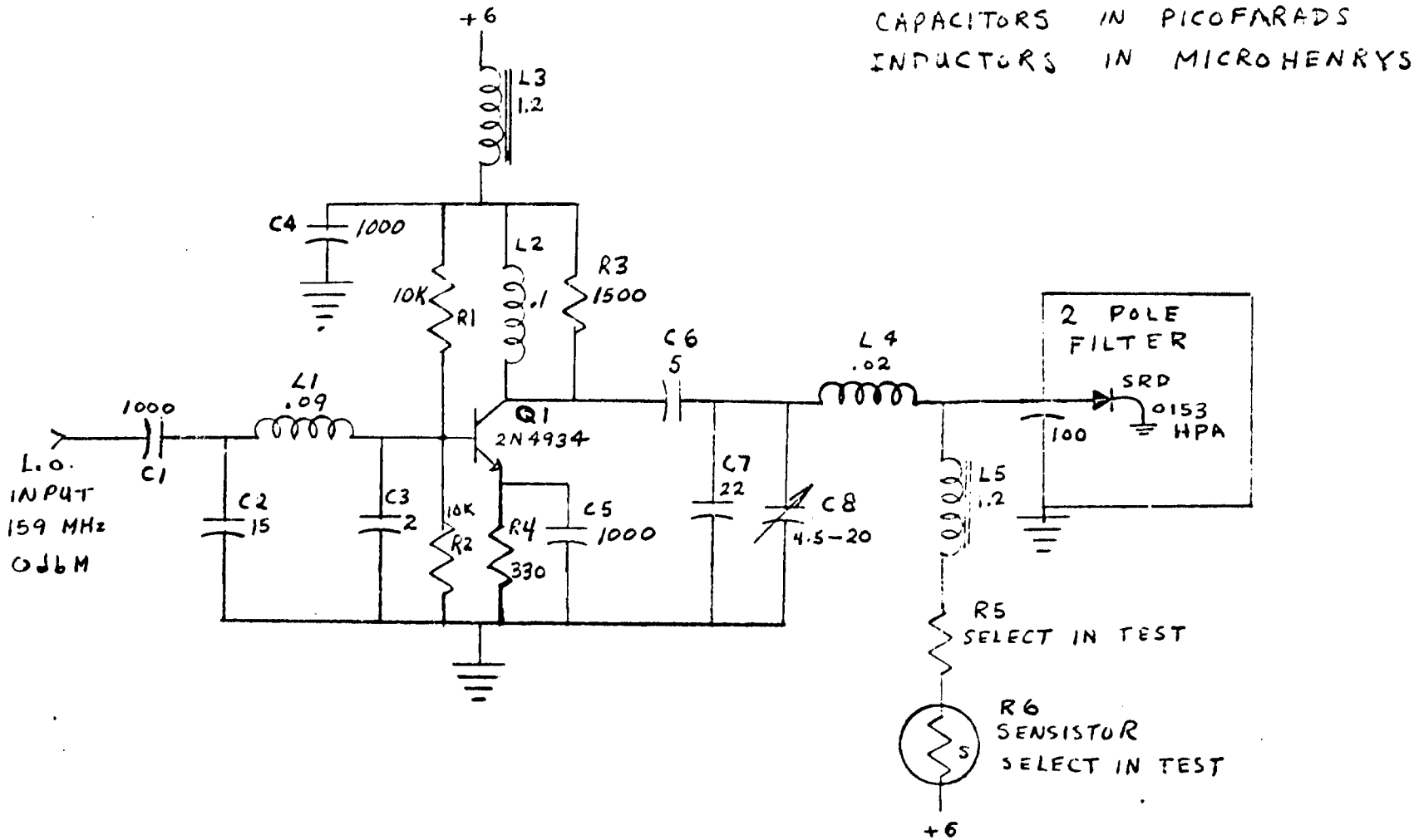


Figure 2-7. LO Driver and X13 Multiplier

2.2.4.2 LO Driver

The value of C6 was chosen to provide the desired gain such that 0 dbm input power is required to deliver 10 milliwatts to the diode. The diode has a 10% efficiency which gives an overall conversion gain of unity. The input matching network consisting of L1, C2, and C3 transforms the transistor input impedance of about 100 ohms to 50 ohms. The transistor is biased at 6 milliamperes and has an input vswr less than 1.5:1 at center frequency. Resistor R3 is used to insure stability of the amplifier.

2.2.4.3 Temperature Stability

The diode is biased at .5 to 2 milliamperes by R5 and R6 which are selected in test to give the desired response and temperature compensation. A Texas Instrument sensistor is used for R6 which has a .7%/°C positive temperature coefficient. The total resistance versus temperature will be nearly linear. This characteristic was found to be satisfactory. A curve of desired resistance versus temperature is found for each circuit and a linear approximation made graphically. Then the value of R6 at room temperature is found by:

$$R6 = \frac{R2 - R1}{.007(T_2 - T_1)}$$

where R2 is the resistance at temperature T_2 and R1 is the resistance at T_1. Then R5 is chosen to give the required total resistance at room temperature. Test results show that local oscillator power available to the mixer varies ± 2 db over the temperature range -35°C to +80°C.

2.2.4.4 Two Pole Filter

The filter following the step recovery diode is a two pole interdigital cavity filter. It has a ripple bandwidth of 18 MHz and a 3 db bandwidth of 44 MHz. Its loss is .5 db at center frequency. The cavity dimensions are 1.432 x 0.375 x 0.972 inches. The resonators are 1/8 inch round rods placed symmetrically 0.2

inch from the ends. The filter is tuned by slugs which screw into the open circuit end of the rods. Tuning is achieved by the stray capacity from slug to ground planes. Access holes in the chassis allow them to be tuned externally. The output of the filter is capacitively coupled to a small probe which is connected by a .050 inch pin to the mixer stripline board. Its position must be adjusted for the best swept response seen at a mixer test point. The filter cover is removed for this adjustment.

The rejection of this filter to the 12th and 14th harmonics is calculated to be 35 db while the 11th and 15th harmonics are attenuated 47 db. The design data sheet is given in table 2-2.

2.2.5. S-Band Amplifier

2.2.5.1 Preselector Filter

The amplifier is preceded by a three pole filter which prevents the receiver from overloading on outband signals. The minimum bandwidth allowable is determined by the filter loss. A compromise must be made between selectivity and filter size (or loss). It was decided to use a three pole cavity filter with a 3 db bandwidth of 63 MHz. The dimensions are 1.401 x 0.375 x 1.475 inches. The resonators are 1/8 inch diameter rods spaced symmetrically with the end rods 0.20 inch from the ends. Its construction is identical to the multiplier filter. The input is coupled by a tap near the ground end of the input resonator. The output is a capacitive tap. Both input and output tap positions are varied to obtain the least return loss at the input. The three slugs are varied to obtain the desired input vswr swept response. The insertion loss is 0.55 db if the cavity walls and rods are silver plated.

The calculated rejection at the image frequency (2016 MHz) is 30 db while attenuation to the LO frequency is 11 db. The ripple bandwidth is 40 MHz with a 1.2:1 ripple in the vswr. The design data sheet is reproduced as table 2-3.

```
DESIGN DATA FOR  2 POLE INTERDISHAL FILTER.  PASSBAND RIPPLE  .036 DB.
CENTER FREQUENCY  2.0610 GC.  CUTOFF FREQ'S  2.0520 AND   2.0700 GC.
RIPPLE BW =   .0180  BW3DB =   .0440  GC.  FRACTIONAL BW =   .00873  FILTER Q = 46.82.
EST QU =  1184.   LOSS BASED ON THIS QU   .49 DB
DELAY AT BAND CENTER     10.2.976 NANOSECONDS
LOSS AT   2.106 GC  IS   13.2DB
LOSS AT   1.902 GC  IS   35.1DB
LOSS AT   1.744 GC  IS   47.1DB
QUARTER WAVELENGTH =  1.432  INCHES
LENGTH OF INTERIOR ELEMENTS =  1.327 INCHES
TOP LOADING  .026 PAR PLATE +  .084 FRINGING =  .110 PF. TOTAL
LENGTH OF END ELEMENTS   1.333 INCHES
TOP LOADING  .028 PAR PLATE +  .084 FRINGING =  .112 PF. TOTAL
CAVITY INSIDE DIMENSION   1.432  INCHES
GRND-PLANE SPACE   .375  ROD DIA   .125 INCHES.  END PLATES   .200 IN. FROM C/L OF END ROD.
TAP EXTERNAL LINES UP   .077 INCHES FROM SHORTED END
LINE IMPEDANCES. END RODS  76.20  OTHER  80.41  EXTERNAL LINES  50.00 OHMS.
G VALUES BASED ON RIPPLE BW.  Q/COUP ON 3-DB.  REVISED   06/19/67  C. W. ROOK
                  DIMENSIONS
EL. NO.     END TO C    C TO C      G(K)     Q/COUP

   0                                1.000     1.546

   1          .200                   .632      .708
                        .572
   2          .772                   .527     1.546

   3                                1.200

  END              .972
.ENDJOB.
```

L. O.
2 pole
HIGH Q

post LENGTHS
Input 1.350
Output 1.280

Table 2-2. 2060 MHz Filter Design

```
DESIGN DATA FOR  3 POLE INTERDISHAL FILTER.  PASSBAND RIPPLE  .036 DB.
CENTER FREQUENCY  2.1060 GC.  CUTOFF FREQ'S  2.0860 AND    2.1260 GC.
RIPPLE BW =    .0400  BW3DB =    .0631  GC.  FRACTIONAL BW =   .01899  FILTER Q = 33.38.
EST QU =   1197.   LOSS BASED ON THIS QU    .52 DB
DELAY AT BAND CENTER      10.84849 NANOSECONDS
LOSS AT   2.016 GC  IS   30.1DB 2196
LOSS AT   2.061 GC  IS   11.3DB
LOSS AT   1.947 GC  IS   45.2DB  1265
QUARTER WAVELENGTH =  1.401  INCHES
LENGTH OF INTERIOR ELEMENTS =  1.297 INCHES
TOP LOADING  .026 PAR PLATE +  .084 FRINGING =  .110 PF. TOTAL
LENGTH OF END ELEMENTS   1.303 INCHES
TOP LOADING  .028 PAR PLATE +  .084 FRINGING =  .112 PF. TOTAL
CAVITY INSIDE DIMENSION   1.401  INCHES
GRND-PLANE SPACE   .375  ROD DIA   .125 INCHES.  END PLATES   .200 IN. FROM C/L OF END ROD.
TAP EXTERNAL LINES UP   .098 INCHES FROM SHORTED END   .180
LINE IMPEDANCES. END RODS  76.20  OTHER  80.41  EXTERNAL LINES  50.00 OHMS.
G VALUES BASED ON RIPPLE BW, Q/COUP ON 3-DB.  REVISED   06/19/67  C. W. ROOK
                 DIMENSIONS
EL. NO.    END TO C    C TO C     G[K]     Q/COUP

   0                              1.000     1.291

   1          .200                 .818      .671
                        .538
   2          .738                1.090      .671
                        .538
   3         1.275                 .818     1.291

   4                              1.000

    END           1.475
```

port lengths { Output 1.236, Input 1.323, Center 1.280

3 Pole
Low Q

Table 2-3. 2106 MHz Filter Design

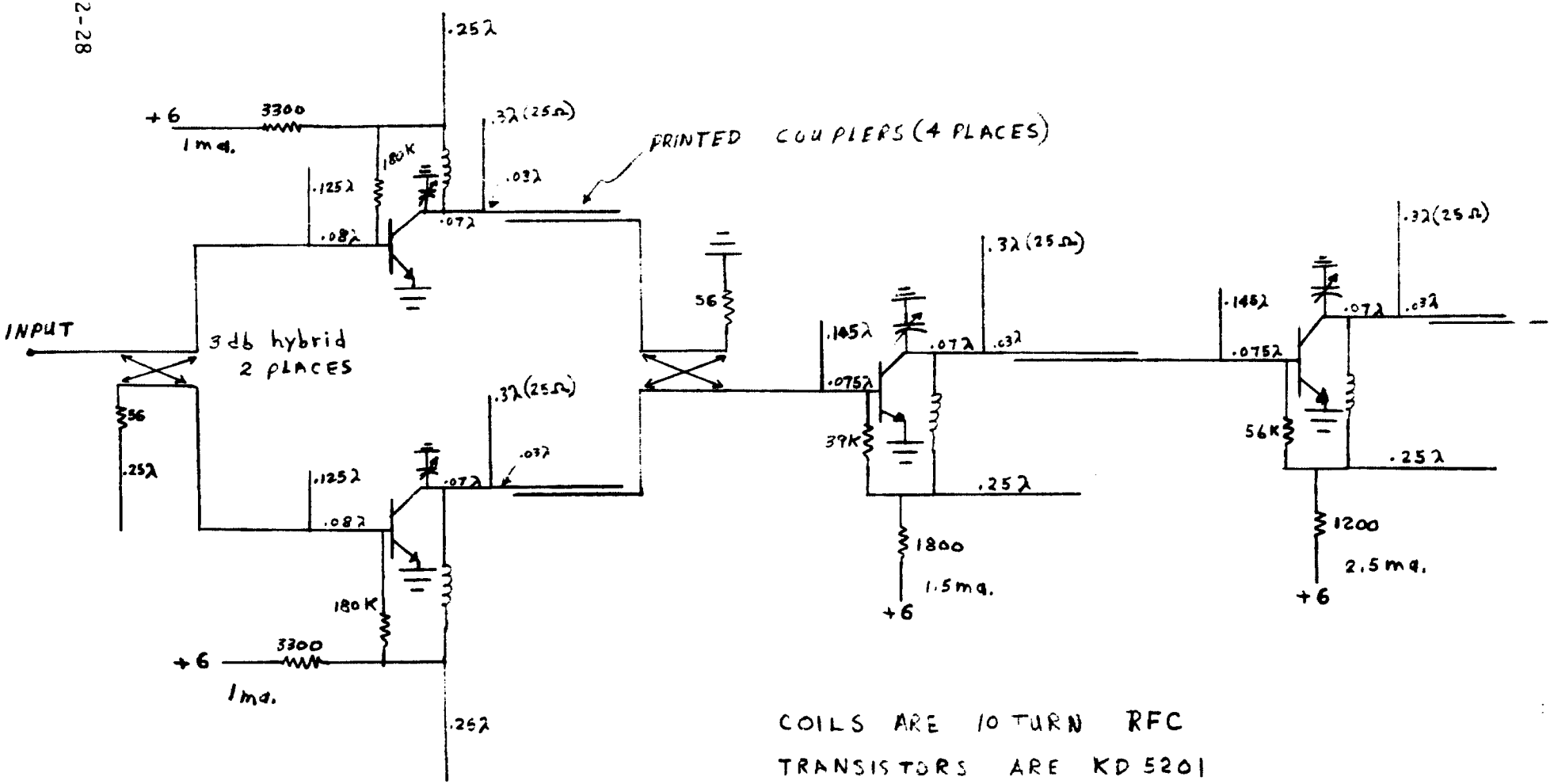
2.2.5.2 Amplifier Configuration

The S-band amplifier consists of 5 stages using six KD5201 transistors. The average gain of these transistors at 2100 MHz is 6 db with an expected noise figure of 6 db. The first stage uses two transistors in a balanced configuration. The purpose in this is to operate the transistors from an optimum scurce impedance for best noise figure, and at the same time terminate the preselector filter properly. For further information on transistor noise figures, refer to paragraph 2.2.10.

It was found that a 1 milliampere bias is optimum for the first stage noise figure. This, however, reduces the gain to 4 or 5 db. Assuming a transistor NF of o db, an amplifier with a 7.5 db noise figure could be constructed. The amplifier built is shown in figures 2-8 and 2-9. The first three stages are built on a 1.8 x 3.8 inch stripline module consisting of two 1/32 inch thick teflon printed circuit boards and two aluminum backing plates. A similar stripline module includes two stages of S-band amplification and the mixer circuit. The r-f is fed between boards by .050 inch interconnect pins soldered to the tracks.

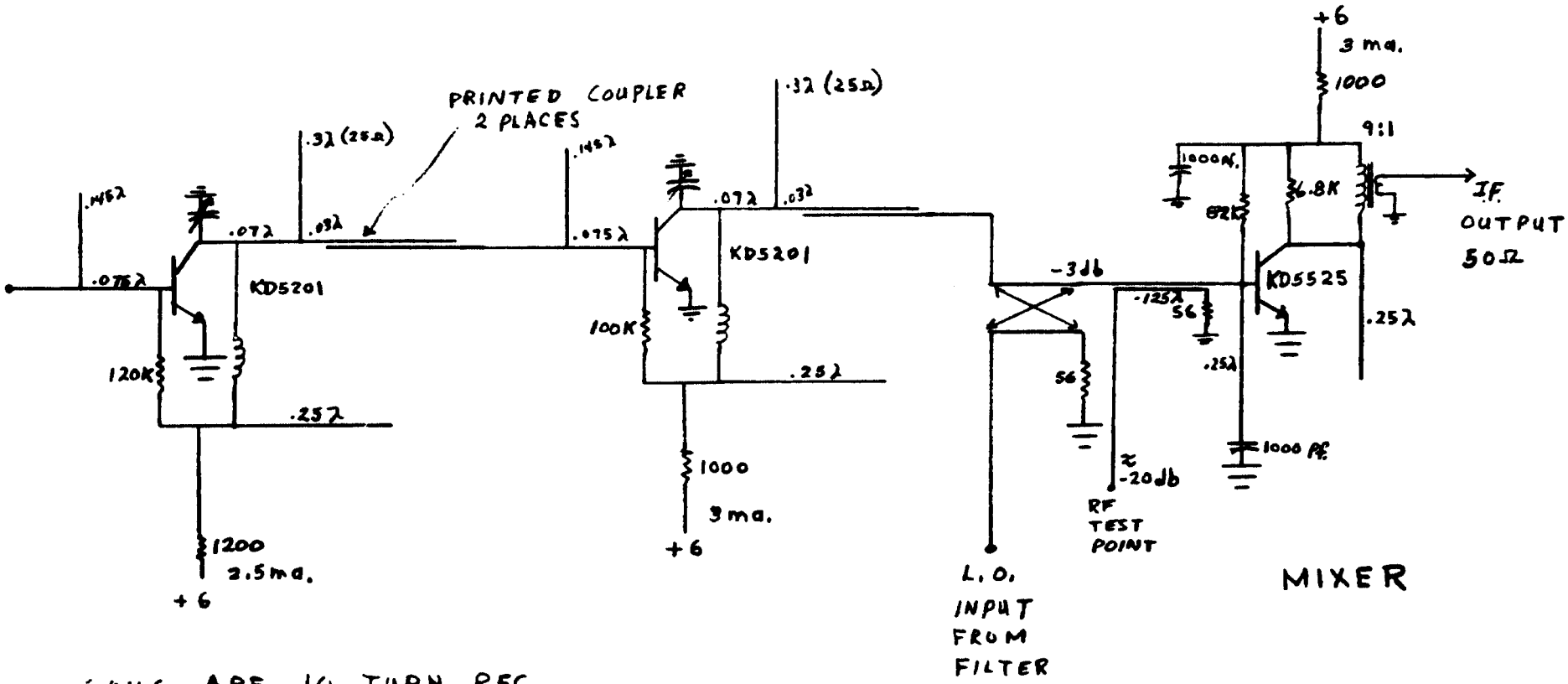
The 3 db couplers of the balanced stage are miniature couplers purchased from Merrimac Research and Development and were used mainly for their small size. They have .5 db insertion loss. Stripline couplers could be used if more room were available. The couplers between transistors are used only for dc isolation. They consist of two different width lines printed on opposite sides of a .010 inch teflon board. One of the lines could as easily be printed with the rest of the circuitry. One might alsc consider printing the entire amplifier circuitry on both sides of the .010 inch teflon board. However, this may cause problems in mounting other components. With one end of the coupler terminated in 50 ohms, the input admittance is .46 + j.9 from 1800 MHz to 2200 MHz. The couplers used are .5 inch long but other dimensions could be used.

Stripline stubs and line lengths are used to match the collector and base to their load and source respectively. A variable capacitor is used in the collector circuit due to the high Q. This capacitor consists of an adjustable ground slug of



COILS ARE 10 TURN RFC
TRANSISTORS ARE KD 5201
50Ω TRANSMISSION LINE EXCEPT WHERE NOTED
5GΩ LINES ARE .091" WIDE
25Ω LINES ARE .113" WIDE
VARIABLE CAPACITORS ARE .1 - 1.1 pf.

Figure 2-8. PREAMPLIFIER SCHEMATIC DIAGRAM -- 2106 MHz



COILS ARE 10 TURN RFC

50Ω TRANSMISSION LINES EXCEPT WHERE NOTED

BASE RESISTORS DEPEND ON H_{FE} OF TRANSISTORS

VARIABLE CAPACITORS ARE .1 – 1.1 pf.

Figure 2-9. AMPLIFIER – MIXER SCHEMATIC DIAGRAM

#10-80 UNC threads and .13 inch diameter plates. The dielectric is partly air and partly ceramic due to a .020 inch thick ceramic spacer fastened to the slug. The ceramic used has a relative dielectric constant of 20 and gives a maximum capacitance of 1.1 pf.

The r-f chokes consist of 10 turns #30 AWG enameled wire wound on a .040 inch form which is later removed. All resistors are 1/8 watt carbon resistors. The base resistors are calculated after first determining the H_{FE} of each transistor and knowing the desired bias current.

Both stripline circuits are sandwiched together between three 1/8 inch thick aluminum plates. Screws are used between plates for mechanical rigidness and to eliminate undesirable modes from propagating. Aluminum tape was used on the edges of the module since there was r-f present here A sketch of the amplifier mechanical layout is shown in figure 2-10.

2.2.5.3 Test Results

The first breadboard built of the first three stages had a gain of 15 db and a noise figure of 7.6 db. It was different from the schematic of figure 2-8 in that dc isolating couplers were used in the base circuit of the first stage transistors. Also the 50 ohm load on the first coupler was returned to dc ground and a 10 volt supply was used. It had a 35 MHz 3 db bandwidth and gain varied ± 2 db over the temperature range $-40^{o}C$ to $+80^{o}C$.

The second and final breadboard corresponds to figure 2-8. Its layout is slightly different from the first breadboard and was designed to fit into the housing which contains the two filters and LO driver. The performance was degraded from the first breadboard in that it has 13.5 db gain and a 9.5 db noise figure. The 3 db bandwidth of the first three stages measured 30 MHz with an input vswr of 1.3:1 and output vswr of 1.3:1. Time did not permit a new layout to be tried but a better noise figure should be achievable.

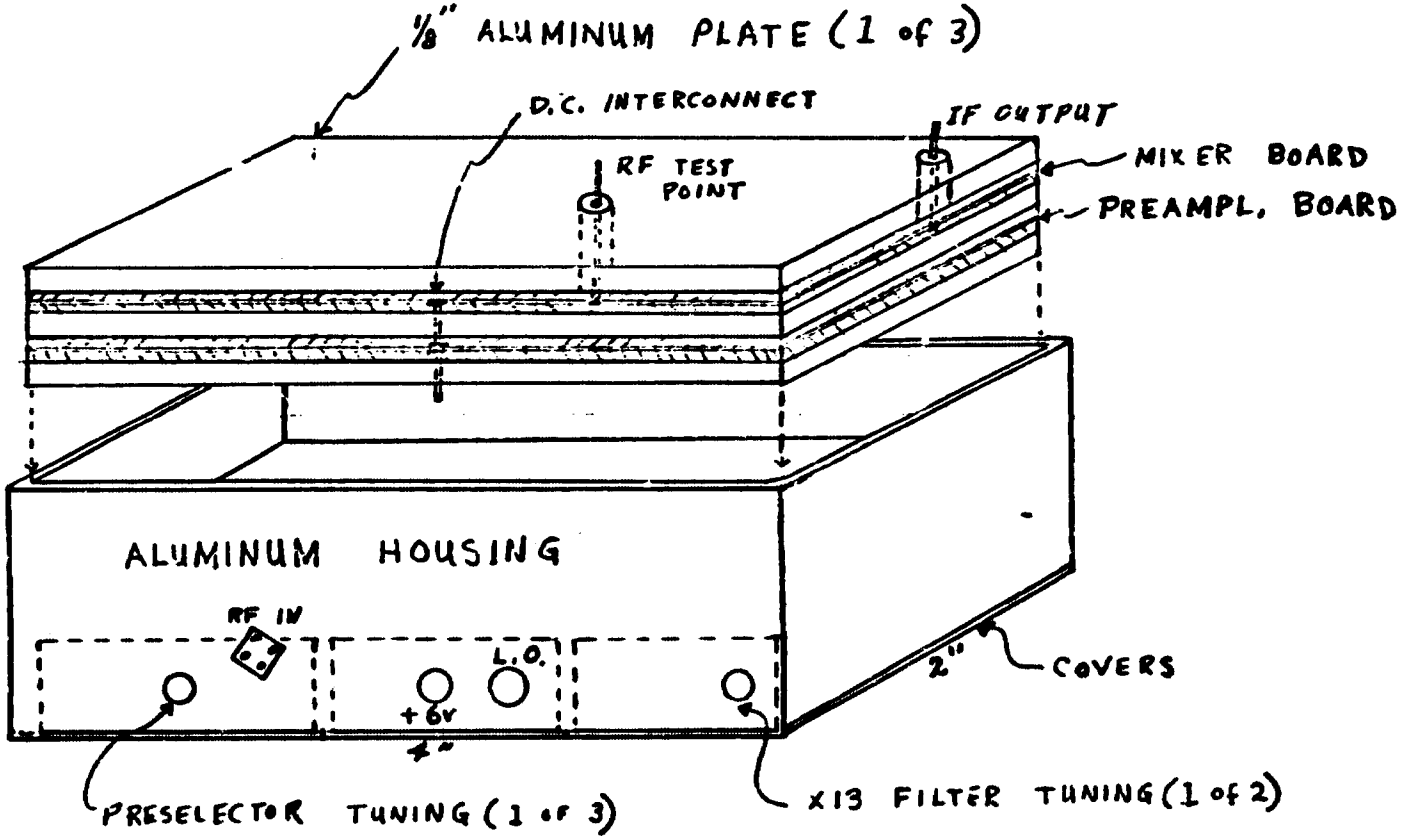


Figure 2-10. R-F Head Mechanical Configuration

2.2.5.4 Measured Transistor Characteristics

An attempt was made to find the transistor best suited to this application as a low noise low level amplifier. It appeared at the start of this project that Texas Instruments and KMC Corporation were the only semiconductor manufacturers which could supply the needed devices. The T1XM105 was first tried. Its performance is good but was not used because it is a germanium device. The L-186 experimental TI transistor was never tried due to its high cost (3 times that of KD5201). It was specified to have a 6 db maximum noise figure and a typical gain of 7 db with 2 ma bias at 2 GHz. The KD5201 was finally chosen partly because of the package used which is very easy to mount in stripline. The KD5525 is similar to the KD5201 except in maximum power rating and gain. The manufacturer's data sheets for the KD5201 and KD5525 are included in paragraph 2.2.10.

A stripline test fixture was built to determine the input and output impedances of the transistors. The biasing used is the same as shown in the schematics previously. No matching networks were included. Stub tuners were used to obtain maximum gain or lowest noise figure. The impedances were then measured using a slotted line setup with either the input or output connector terminated with the appropriate tuner. These impedances were then checked by plotting on the Smith Chart the source and load impedances of the tuners themselves when terminated in 50 ohms. The typical results are tabulated below. Only slight variations were found from transistor to transistor; the most variation being in the input impedances.

Y_{in} = 64-j8 millimhos

Y_{out} = 24j14 millimhos

Y_{source} = 50+j8 millimhos (BEST NOISE FIGURE)

The above parameters were measured at 2100 MHz with the transistors biased at 5 volts and 2 ma. Changing the current from 1 ma to 3 ma did not appreciably affect the tuning. Also the impedances of the KD5525 were the same as the KD5201. The first type is newer and was tried to see if it has an advantage of higher gain. Such an advantage was not detected in that its typical gain was about the same as KD5201.

The H_{FE} of 20 transistors were measured and ranged from 25 to 190. However. these transistors were obtained from many different manufacturing lots. The transistors from a particular lot exhibited a narrow range of H_{FE} variations. The H_{FE} variations with temperature were tested for one device. The current gain decreased from its room temperature value of 163 by 39% at -40°C. H_{FE} increased by 24% at +90°C. This is a two to one variation over this temperature range. The collector to base feedback biasing used will then result in a collector voltage variation of $\pm$1.2 volts which was considered satisfactory even though the room temperature V_{CE} is only 3 volts.

No attempt was made to try to determine the internal feedback of these transistors due to lack of adequate test equipment at 2 GHz. As better test equipment is developed, reliable measurement of "S" parameters would be valuable to the design engineer.

2.2.6 S-Band Mixer

2.2.6.1 Transistor Configuration

The most common S-band mixer used today is a two diode balanced mixer with a 3 dB quadrature hybrid coupler used to isolate the LO and signal inputs. However, since transistors are used to amplify the signal, these same transistors should make efficient mixers at the same frequency. Also, a low noise figure mixer is not mandatory since it is preceded by 20 to 30 db of gain. A 3 db coupler is still used to isolate the LO and signal sources but half the power is dissipated in the termination while the other half goes to the transistor base. This waste of power is not considered significant since it should not affect the receiver noise figure noticeably. It may be possible to built a two transistor balanced mixer but simplicity was also a goal. Another advantage of the transistor mixer is that it has a conversion gain instead of a loss as in diode mixers.

The intermediate frequency is coupled from the collector using a step down transformer to the 50 ohm load. The primary inductance was selected to resonate the transistor capacitance at 45 MHz. It is 18 turns on a CF101 ferrite core. The

transformed load impedance is 3200 ohms. The 6800 ohm collector resistor shunting the collector impedance provides a 50 ohm output impedance. A different i-f frequency can be accommodated providing a suitable transformer is used on the output.

2.2.6.2 Test Results

A tradeoff had to be made between conversion gain and i-f bandwidth. During development a 9 db gain was achieved using a 4300 ohm collector load. However, the BW_3 was only 1 MHz with an lc pi matching network and 7 MHz using a transformer. The loading shown in figure 2-9 resulted in 4.5 db conversion gain with a BW_3 of 16 MHz. This is considered satisfactory.

It was found that tuning of the base to match the 50 ohm coupler was not needed. When a tuner was placed in the base circuit, slightly more gain could be achieved but operation was acceptable over a very narrow range of LO power inputs. With the circuit shown, the input vswr at either LO or signal port was 1.5:1 or less. The LO to signal isolation measured 16 db.

The conversion gain of this mixer as a function of LO drive was measured for the high gain mixer discussed earlier. The results are graphed in figure 2-11. Also shown on this graph is the mixer noise figure. The noise figure is high but would only degrade the system NF by .16 db if preceded by 20 db gain or .02 db if preceded by 30 db gain assuming an 8 db nominal system noise figure.

2.2.7 Module Test Results

2.2.7.1 Spurious Responses

The r-f head provides the only receiver isolation to outband signals. Of main interest is the image frequency which is 2106-90 MHz or 2016 MHz. The specification decided upon is the receiver must not lock to the image frequency at an input level of -60 dbm or less. Assuming a threshold of -130 dbm, the r-f head must attenuate the image signal 70 db minus the module gain at the desired frequency.

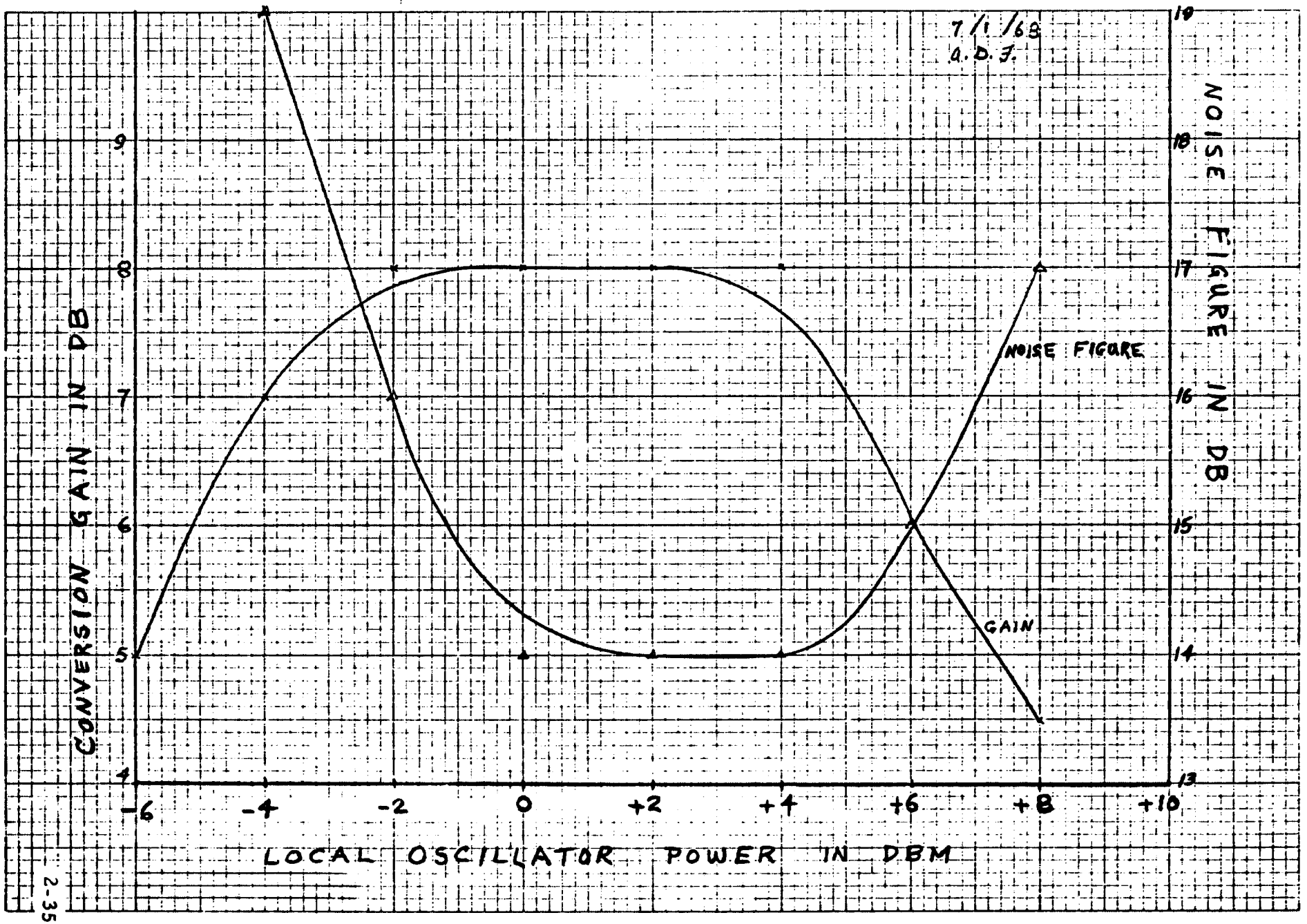


Figure 2-11. Noise Figure and Mixer Gain Vs LO Drive

Thus an attenuation of 40 to 50 db would be desirable. Attenuation to the image frequency of the amplifiers was measured as 38 db. This added to the 30 db rejection of the preselector is sufficient .

The local oscillator signal emanating from the input of the amplifier was measured at -60 dbm. For this test, the X13 was replaced by an external S-band source and the preselector was not used. Since the preselector attenuates the LO frequency 11 db, a -70 dbm signal is expected at the receiver input.

2.2.7.2 Module Gain and Noise Figure Characteristics

Table 2-4 summarizes the characteristics of some individual circuits of the r-f head. The amplifier results are those of the first breadboard and not the final breadboard incorporated into the module. These results do typify what is achievable at present with silicon transistors.

The preselector response is almost precisely that calculated. The insertion loss was measured to be .9 db with an unfinished aluminum housing. However, the loss was reduced to .55 db after silver plating which agrees closely with the expected value of .52 db.

The LO multiplier exhibits good temperature stability as shown in table 2-4. Hot temperature lowers the output power partly due to lower power output of the driver. A ± 3 db variation in LO power output will not degrade performance appreciably.

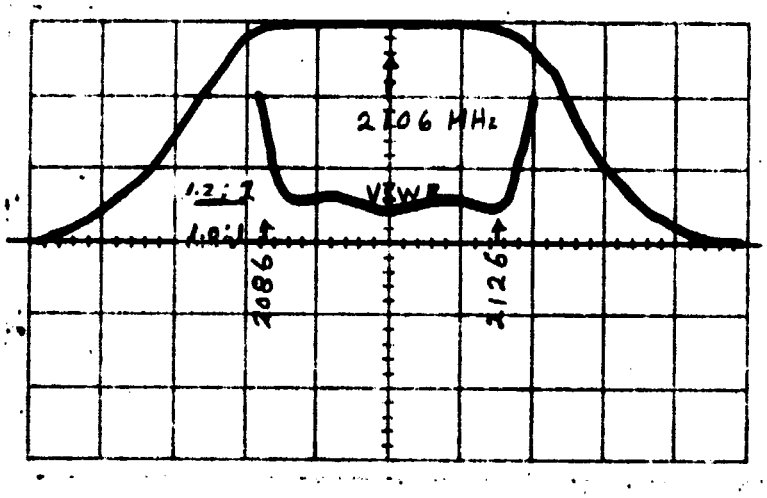
Figure 2-12 shows the gain compression curve of the r-f head. A linear gain of 28 db resulted with limiting occurring around 0 dbm output. Limiting occurs since the transistors are biased at only three milliamperes. This is considered sufficient for the application.

A summary of the module test results is given in table 2-5. Also included is the swept response of the if. output impedance. As can be seen the response is centered at 45 MHz. The if. bandwidth was measured to be 13 MHz which is narrower than the 16 MHz was designed for. However, this can be widened, if desired, at the expense of decreased conversion gain.

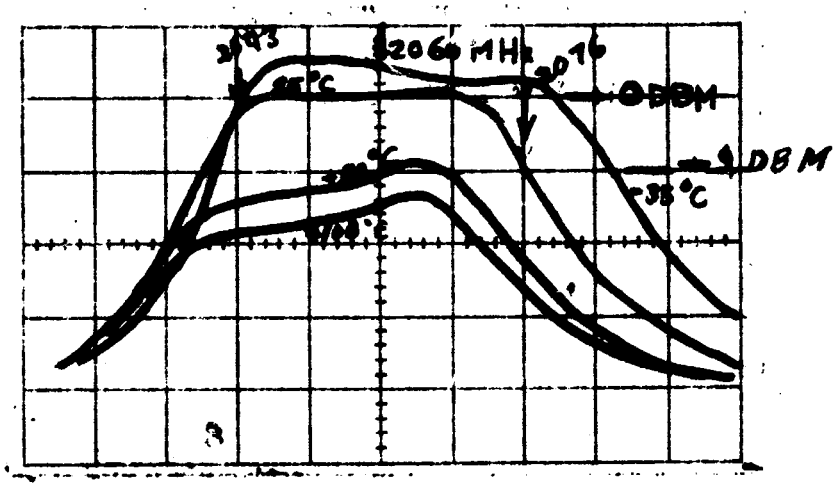
Table 2-4. Experimental Data

5-15-68
A.A.S.

3 POLE PRESELECTOR RESPONSE



TIMES 13 MULTIPLIER



S BAND AMPLIFIER -- 3 STAGES

GAIN = 15 DB NOMINAL
N.F. = 7.6 DB
BW_{3DB} = 35 MHz
LIMITING LEVEL = -5 DBM
INPUT & OUTPUT IMPEDANCES = 50 Ω; VSWR ≤ 1.5:1
TEMPERATURE GAIN VARIATION = -2 DB

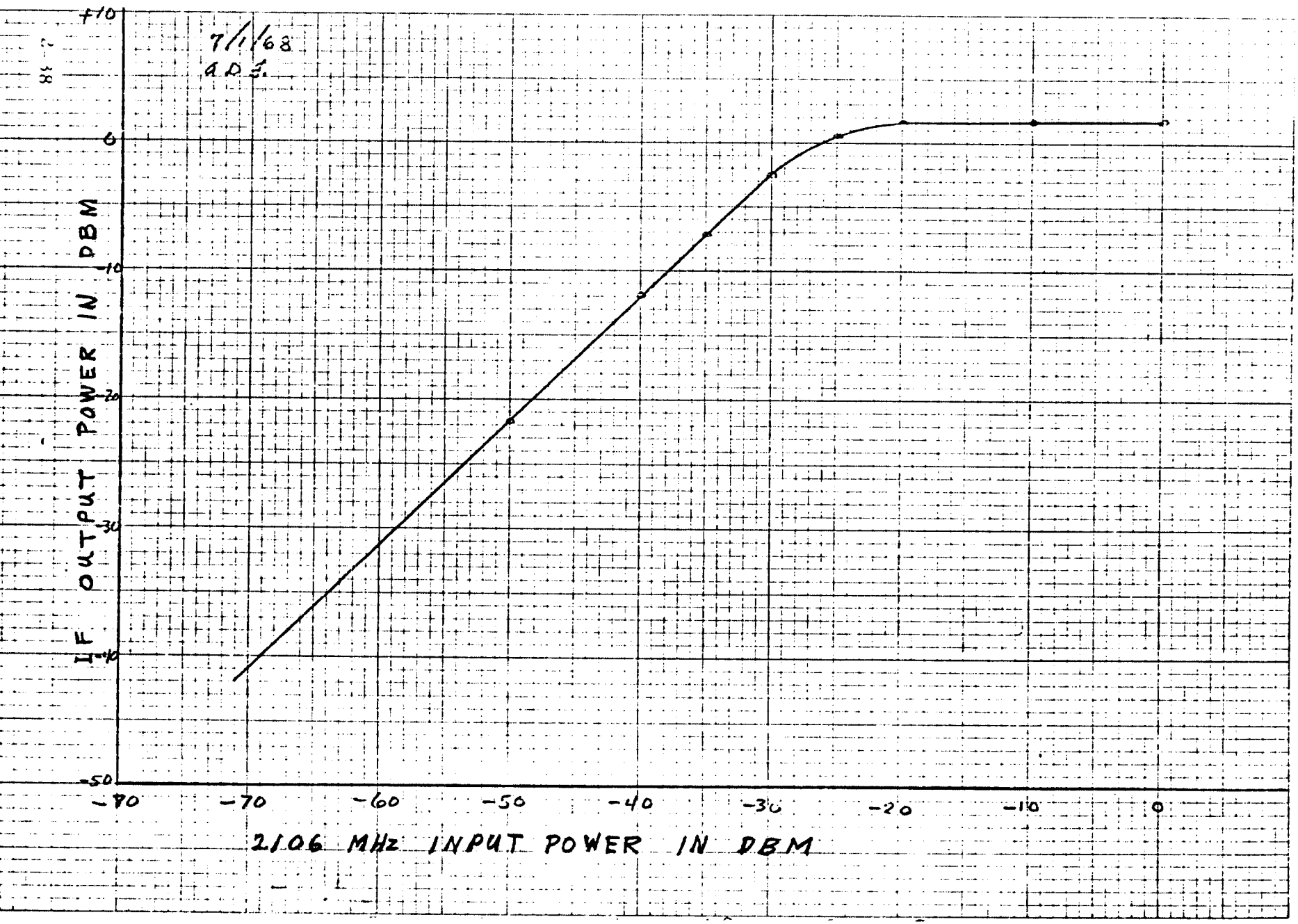


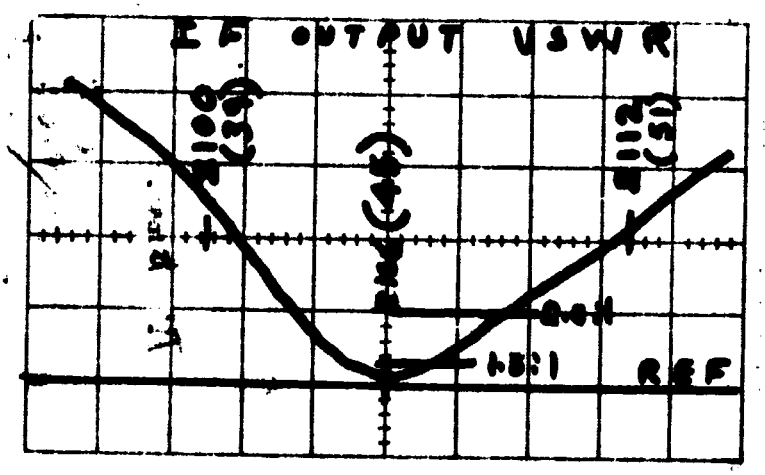
Figure 2-12. R-F Head Gain Characteristic

Table 2-5.

RF HEAD MEASURED RESULTS
ROOM TEMPERATURE

	MEASURED	DESIGN GOAL
GAIN :	27.5 db	30 db
3db BANDWIDTH :	13 MHz	20 MHz
INPUT VSWR :	1.35:1	1.3:1
OUTPUT VSWR :	< 1.5:1	1.5:1
NOISE FIGURE :	9.5 db	6 db
D.C. POWER :	22 ma. @ 6V	25 ma.
IMAGE REJECTION :	< -60 dbm	< -60 dbm
L.O. FEEDTHROUGH :	≯ -70 dbm	< -80dbm
L.O. VSWR :	1.5:1	1.5:1
L.O. POWER IN :	0 dbm	-7 ± 3dbm
IF FREQUENCY :	45 MHz	45 MHz

MIXER OUTPUT VSWR



2.2.8 Problem Areas

The work done on this program revealed some problems related to using S-band gain. Such problems are discussed here.

2.2.8.1 Amplifiers

It is felt that noise figure reduction will always be the most difficult task in this type of receiver application. It has been demonstrated that an amplifier with less than 8 db noise figure can be constructed using silicon transistors. This could be reduced to 6 db with germanium transistors if environmental conditions are not too severe. Further work might also be done to see if collector-to-base neutralization could possibly be employed to decrease the noise contributed by feedback.

The exact reason for the high noise figure on the breadboard r-f head is not known. However, it is assumed that a low gain transistor, poor layout, or a poor solder joint is causing it. An 1800 MHz r-f head was built for another project using the same configuration and exhibited an 8.2 db noise figure with 38 db gain. The temperature characteristics of that module are given in figure 2-13.

After the poor temperature stability indicated in figure 2-13 was noted, investigations were carried out to determine the cause. It was found that changing V_{CE} with temperature was causing the amplifier to detune. Figure 2-14 shows the marked difference between using 3 volts nominal bias and 5 volts. The maximum gain was determined by varying the input frequency. The optimum frequency versus bias voltage is shown in figure 2-15. The collector-emitter voltage changes with temperature due to changing H_{FE}.

These results indicate the need for a different type biasing if only a six volt supply is to be used. The best method would be some way of efficiently bypassing the emitter such that dc emitter degeneration can be used. Even with proper biasing, a gain variation of 5 db for a 30 db amplifier can be expected over the temperature range. If this is a problem, some means of temperature compensation is required.

Figure 2-13. R-F Head Gain and Noise Figure Vs Temperature

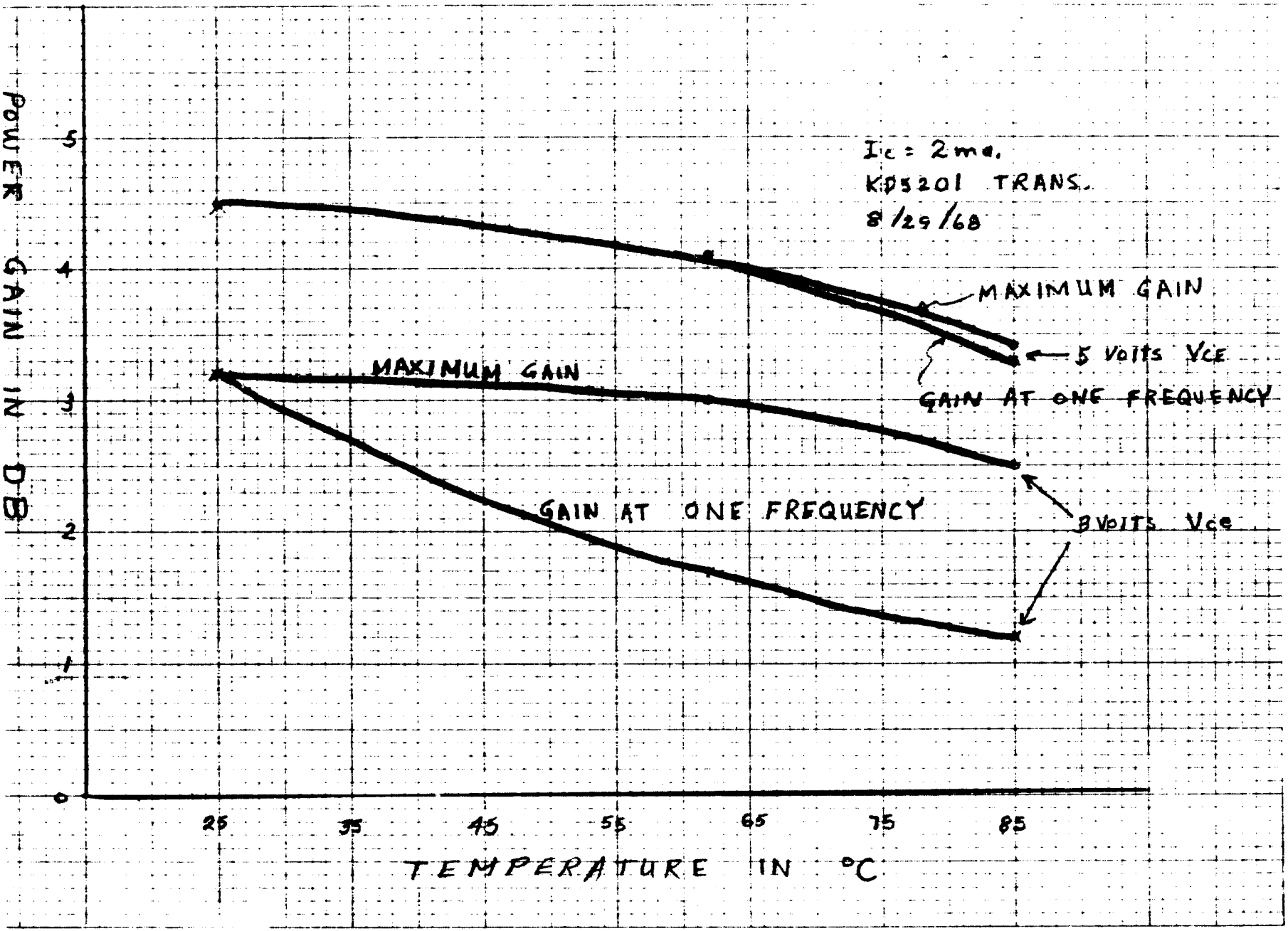


Figure 2-14. 2 GHz Amplifier Gain Vs Temperature

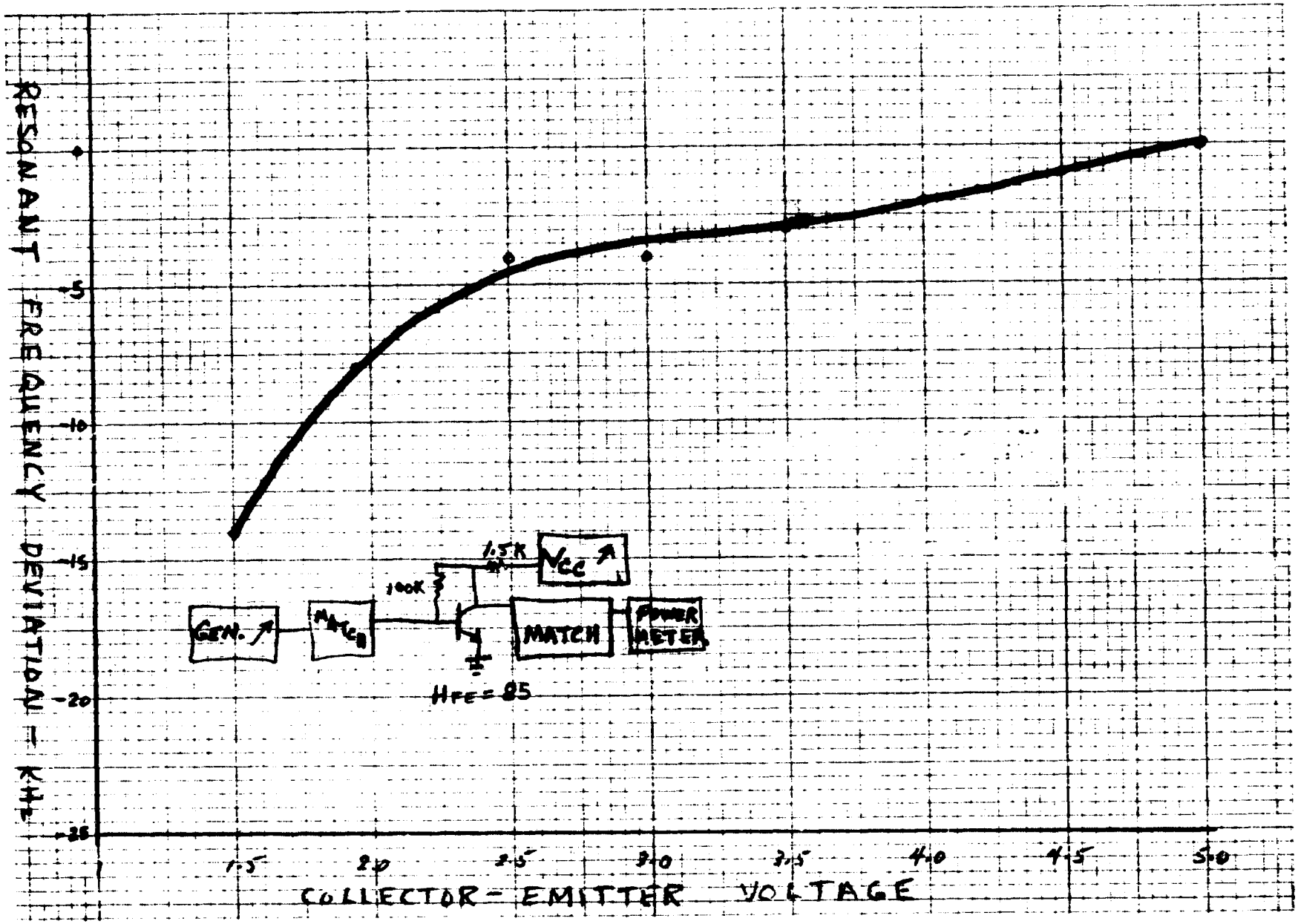


Figure 2-15. KD5201 2 GHz Amplifier Resonant Frequency Vs V_{CE}

2.2.8.2 Mechanical Construction and Alignments

The mechanical design of the r-f head was closely associated with the electrical design. This was done to eliminate all connectors between amplifiers and filters. This is especially critical at the preselector-preamplifier interface where any loss adds directly to the receiver noise figure. A brief description of the assembly and alignment of the module is included here, along with the problems involved.

1. First, the preamplifier board was assembled and tested for correct dc current. The bottom 1/8" aluminum plate is threaded for 2-56 screws which are installed through the center aluminum plate. Special test terminals made of 1/2" by 1-1/2" stripline boards with OSM connectors and dc isolation are installed at the input and output interconnect terminals. The preamp is then tested for correct gain, noise figure, and input vswr using swept frequency techniques. The four variable capacitors are adjusted for best response.

2. The input test terminal is removed and the 2-56 threads removed from the bottom plate. The preamp is installed in the chassis with 2-56 screws through the middle plate to taps in the chassis. The preselector is now aligned for best vswr swept response. Tuning of the preselector is accomplished by 3 post adjustments, input and output coupling. The input coupling is achieved using a probe which slides simultaneously along the input resonator post and connector pin. Its position is approximately .18" from the cavity top and mainly affects magnitude of the vswr. The output probe is a 1/2" circular capacity tap which is soldered to the preamp input .050" pin. The distance between the probe and output resonator post determines mainly the ripple and bandwidth of the swept vswr response. The position of this output probe is approximately .020" from the post, is quite critical, and difficult to adjust. A better mechanism for output coupling is desired. The gain of the preamplifier can now be rechecked.

3. The mixer board is now installed on top of the center plate. Screws are installed through the top plate to taps in the center plate. The LO input pin extends through the preamp and chassis to the LO filter. It is surrounded by a .175" diameter teflon spacer which makes a 50 ohm transmission line. The dc and S-band interconnects from the preamp board are soldered to the mixer board before installing the top plate. Test connectors are used at the i-f output and r-f test point. The vswr at the test point connector is not important since it is from a 20 db coupler and a narrow frequency range is used. A capacity probe identical to the preselector output probe is used in the LO cavity. The step recovery diode provides an inductive coupling into the filter and is not adjustable. The X13 multiplier and filter are now aligned by adjusting the two post lengths, output coupling probe, diode bias, and LO driver matching networks. The swept response is taken from the r-f test point which must be fed to an amplifier and high gain scope head in series. Again the output coupling is the most difficult and time consuming adjustment. An easier coupling method is desired. The variable capacitors on the mixer board are adjusted while sweeping the r-f input and using the same r-f test point. The i-f output vswr can be viewed by injecting a swept signal into the output port through a rho-tector. The LO power should be applied for this test.

This completes the major part of the mechanical assembly. One can see that removing a circuit for rework is quite difficult in that many alignments have to be repeated once the circuit is replaced. It is felt that this is the price one has to pay for small physical size. The r-f head would be much easier to build and align if the two stripline circuits were entities in themselves with r-f connectors. This, however, would probably increase the volume of the module by a factor of 2.

2.2.9 Recommendations and Conclusions

There are many small changes which can and should be made to the mechanical configuration of the r-f head before any production takes place. Already mentioned

is the need for better filter couplings which could save hours of test time on each unit. Also, three separate covers are used on the breadboard unit. It was found that removing and replacing a cover did not alter the filter tuning which would make the use of a single large cover feasible.

It was found that an r-f field existed at the edges of the stripline submodules. Space permitting, the aluminum plates should contain flanges around the edges to prevent external influences from altering the amplifier performance. It is felt that aluminum tape is not satisfactory for flight models.

Many transponder applications do not necessitate the need for a preselector since filtering occurs at the antenna multiplexer. The r-f head could be made much simpler without a preselector. The LO multiplier and filter could as easily be made using stripline. This would mean the whole module could be contained in 3 stripline submodules. Also the noise figure would be decreased since there would be no preselector loss.

Eventually, more dc supply line filtering may be needed. No provisions were made on the breadboard to reduce susceptibility to interferences on the power line. No tests were performed to determine audio or r-f susceptibility.

It was intended that the bottom aluminum plate of the amplifiers be removed before installation in the housing. To do this, clearances must be made in the housing for the dc biasing components. This was not carried out on the breadboard but would save weight on flight models. Then only one bottom plate would be made to test each preamplifier board by itself.

There will always be advantages to amplifier redesign efforts. One area which may be improved is the collector matching networks. The present matching networks probably limit the bandwidth. Time did not permit analyzing the frequency response of the amplifiers so optimization for large bandwidth was not carried out. The present overall S-band amplifier bandwidth is near 30 MHz. It is felt that this could be increased to no more than 50 MHz while retaining a conjugate match at the collector of all five stages. This results from the gain-bandwidth

product being limited by the transistor output capacitance. The matching could also be broadened by using higher impedance 3 db couplers and interfaces. However, this usually makes it much more difficult to test since most test equipment has a 50 ohm impedance level. A broader matching would be desirable in that variable capacitors could probably be eliminated.

The results of this work are considered quite encouraging even though a lower noise figure was anticipated. This is mainly due to low gain the the transistors used. Since this project started, higher gain transistors have been reported by such companies as Texas Instruments and Nippon Electric. The difference in gain is only minimal at present but is expected to widen in the near future. This is the primary basis for beginning the development of a miniature receiver front end using transistor amplifiers at the input frequency.

Work is also being done in the industry on integrated circuit S-band amplifiers. At present most of these advances use distributed components in the form of microstrip. Some work was started on this project to build a lumped constant 2 GHz integrated amplifier. However, due to long turn-around time in our integrated circuit facility, this work was not completed. Little emphasis was placed on this work since it was felt that development time would not allow a workable unit to be achieved in time to test the receiver. It is felt that an integrated S-band amplifier is feasible but will be quite costly to develop. It would, however, tremendously reduce the receiver size. In the future, it will probably become the ultimate configuration.

2.2.10 Transistor Noise Figure Analysis

An attempt was made to determine analytically the optimum source resistance and bias current needed to obtain the best noise figure in any particular transistor. The relationship used to obtain the transistor noise figure is given by equation[1] 1.

$$F = 1 + \frac{r_e}{2R_g} + \frac{r_b}{R_g} + \frac{\left(R_g + r_e + r_b\right)^2}{2\,\alpha_o R_g r_e}\left[\frac{1}{H_{FE}} + \frac{I_{co}}{I_E} + \left(\frac{f}{f_\alpha}\right)^2\right] \qquad (1)$$

[1] Texas Instruments Inc., Communications Handbook--Part II, 1965 Edition, Dallas 22, Texas.

In equation 1:

$r_e = 25/I_{Ema}$ ohms

R_g = Source Resistance

r_b^1 = Intrinsic base resistance at operating frequency

α_o = low frequency common-base current gain (not dc α)

H_{FE} = d-c common-emitter current gain

I_{co} = d-c collector cutoff current

I_E = d-c emitter current

f = operating frequency

f_α = Common base cutoff frequency or frequency where $\alpha = .707\ \alpha_o$ ($\cong 1.5\ f_T$)

This equation accounts for the three main internal noise generators of a transistor:

1. Shot noise in the base-emitter junction
2. Shot noise in the collector-base junction, and
3. Thermal noise in the base resistance

Equation 1 is valid over the entire frequency spectrum except at very low frequencies where the 1/f noise occurs. The last term of equation 1 predicts the 6 db/octave rise in noise figure vs frequency.

The main problem with applying equation 1 is determining the appropriate transistor parameters of which f_α is probably the most difficult to measure. In fact the noise figure measurement itself is probably the most accurate way to determine f_α.

Equation 1 gives the noise figure of the first stage of an amplifier only. If the gain of this stage is not large, following transistors will also contribute to the overall amplifier noise figure. This overall noise figure is given by equation 2.

$$F_A = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \frac{F_n - 1}{G_1 G_2 \ldots G_{(n-1)}} \qquad (2)$$

In equation 2, F_n is the absolute noise figure of the nth stage while G_n is the power gain of that stage.

To further complicate calculations, the gain of each individual stage is a function of its emitter current. This relationship is different for various transistor types and is not known exactly. For purposes of calculations, it is assumed that power gain is proportional to the square root of the emitter current. This should be good enough in the low current range of interest.

A computer program was written using equations 1 and 2 along with the power gain vs current relationship. Listed below are the constants used which typify the T1XM105 transistor.

$r_b{}^1 = 10$ ohm

$f_T = 2200$ MHz

$f_\alpha = 3300$ MHz

$A_p = 112\sqrt{I_E}$

f = 2100 MHz

$NF_2 = 4$ (=6 db)

The results of the computer analysis are given in figures 2-16 through 2-19. Figure 2-16 shows the effect of gain varying with bias current. It shows that the overall noise figure minimum occurs at a higher current than does the first stage NF minimum. The second stage is assumed to have infinite gain which is valid if NF_2 includes the noise contribution of all subsequent stages.

Figure 2-16 predicts that an optimum source resistance will occur when the first stage is biased at a particular current (chosen as 2 ma for illustration).

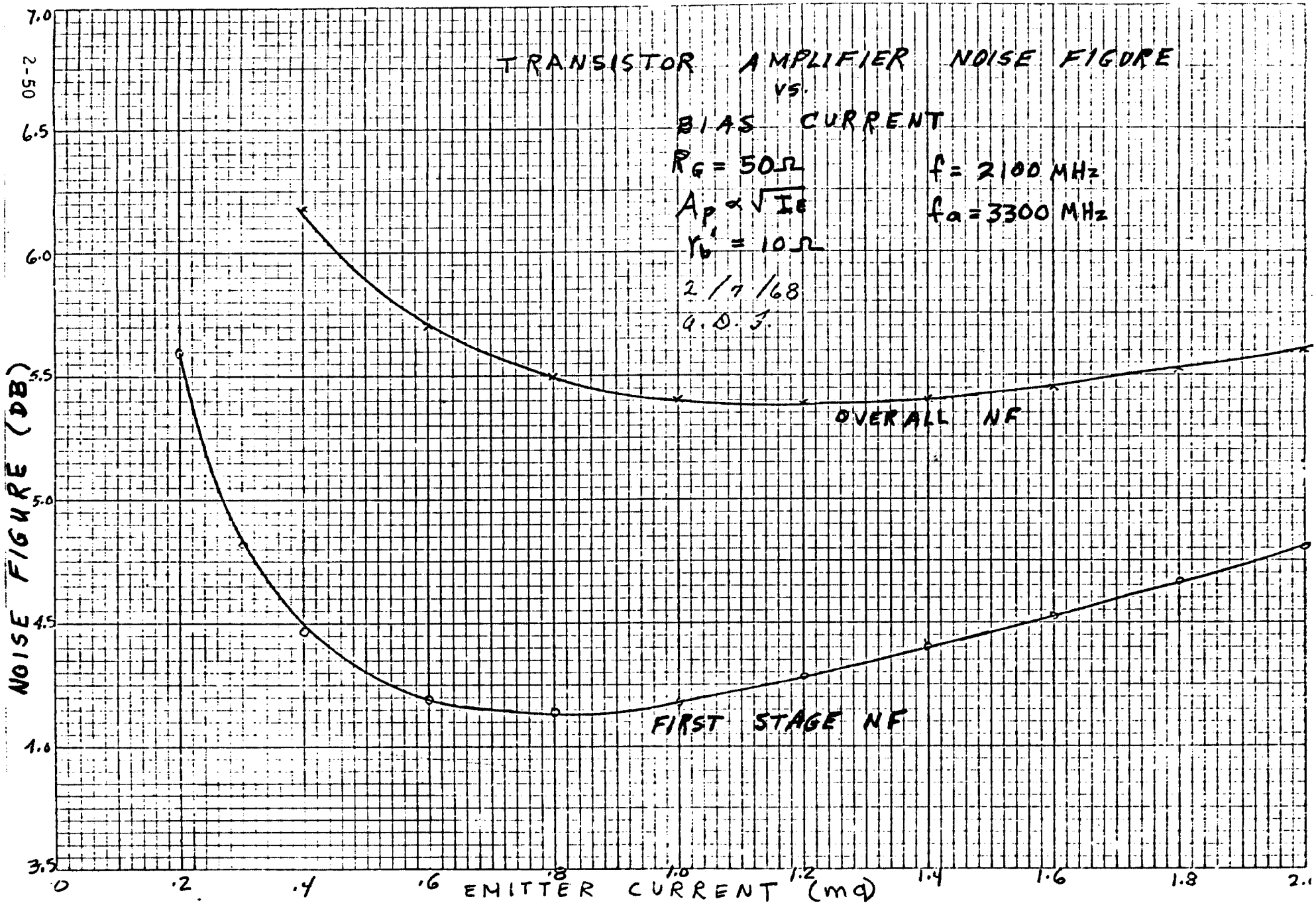


Figure 2-16. Transistor Amplifier Noise Figure Vs Bias Current

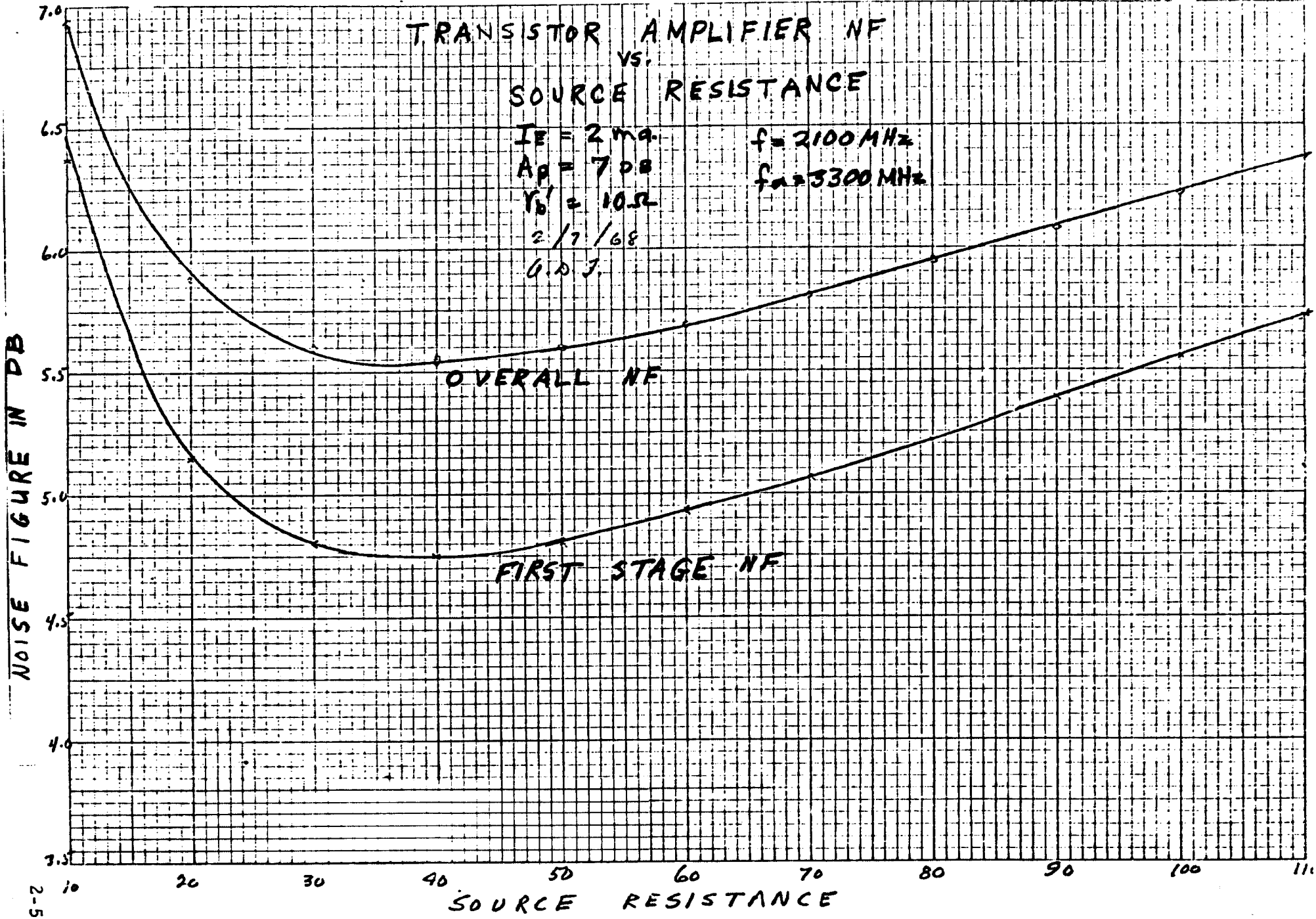


Figure 2-17. Transistor Amplifier NF Vs Source Resistance

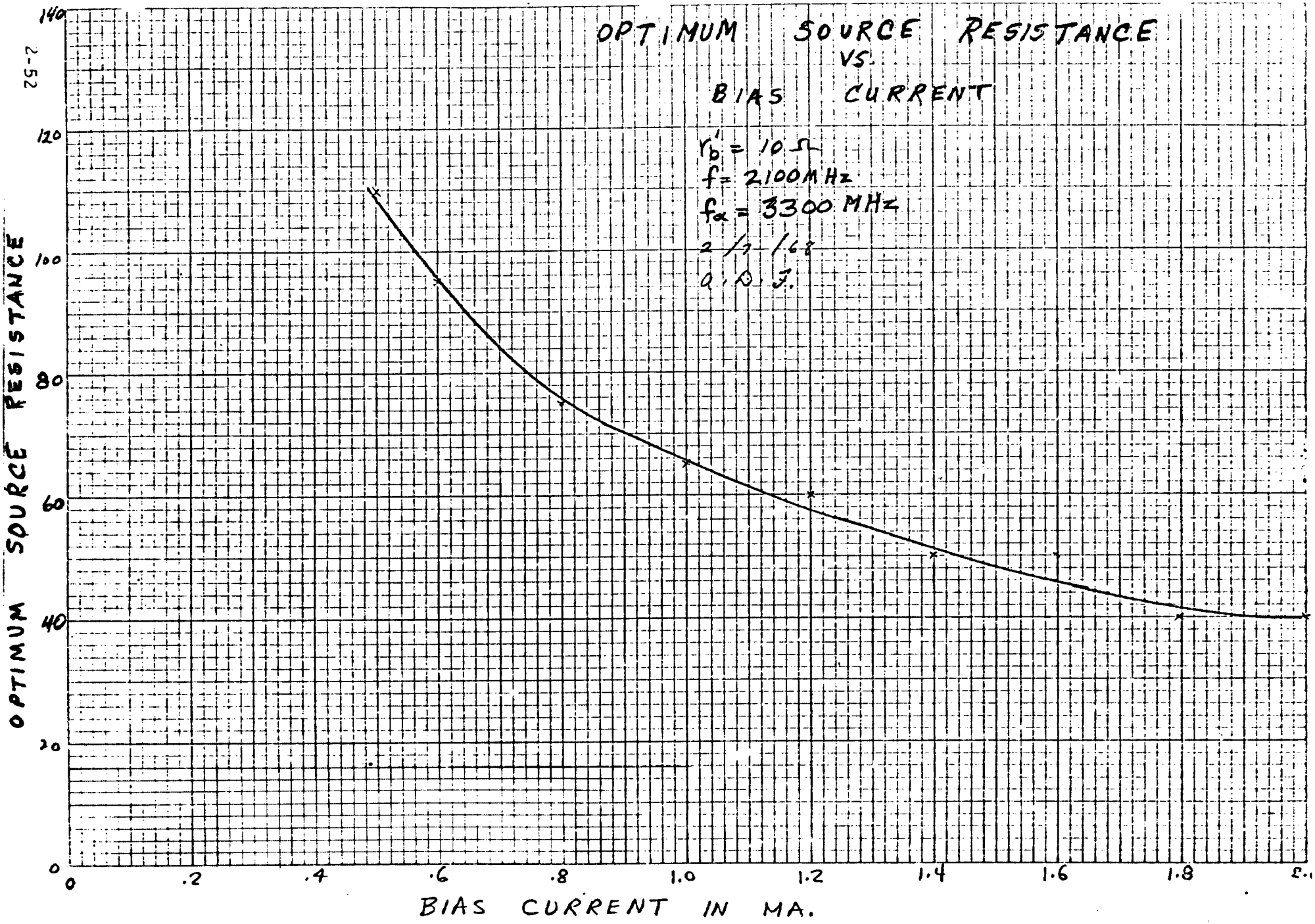


Figure 2-18. Optimum Source Resistance Vs Bias Current

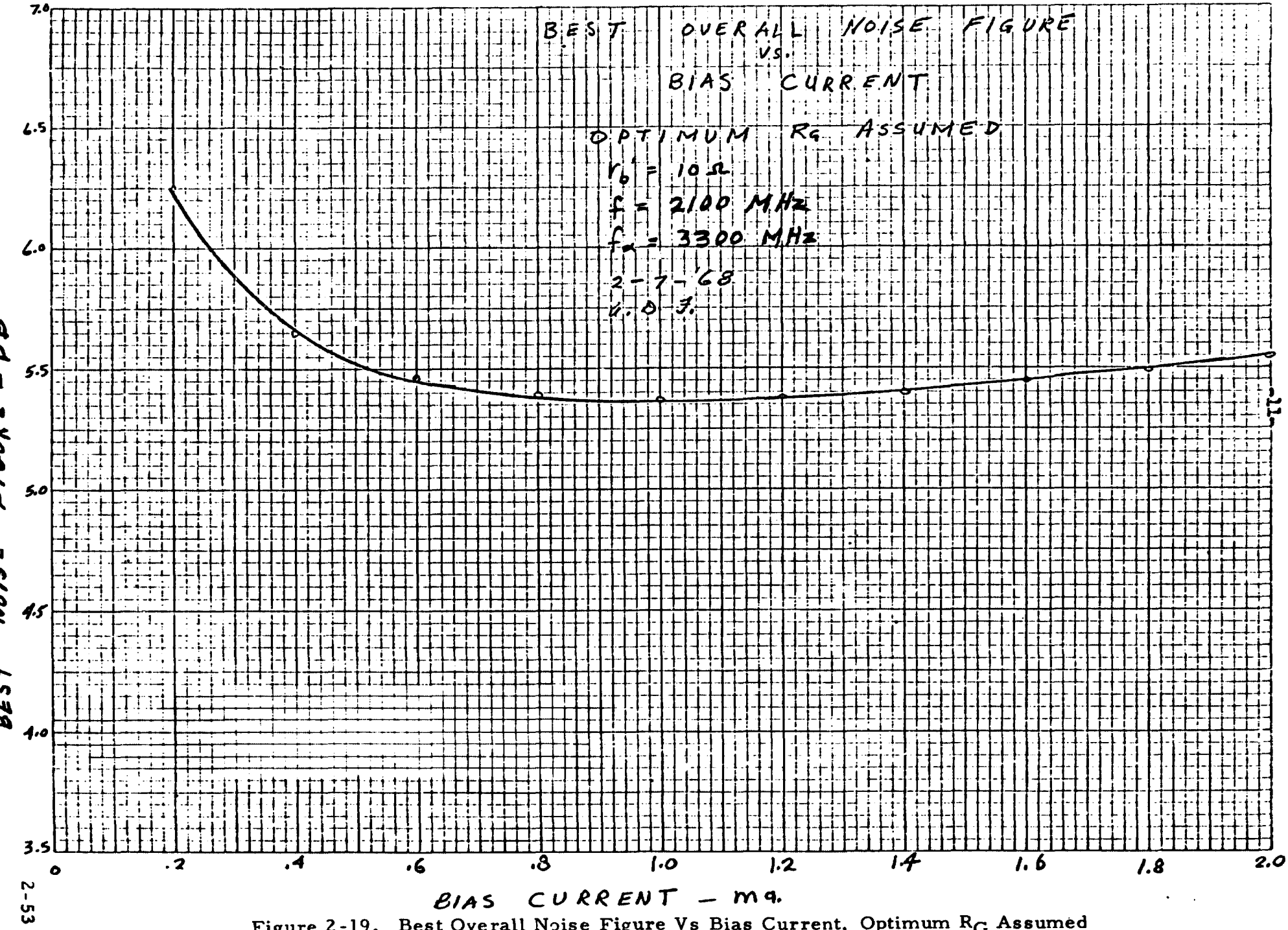


Figure 2-19. Best Overall Noise Figure Vs Bias Current, Optimum R_G Assumed

Figure 2-18 indicates that a range of source impedances could be accommodated by choosing the appropriate bias current. Figure 2-19 illustrates the lowest NF possible for optimum conditions and any current level. The broadness of this curve indicates that the selection of operating current is not critical for best noise performance.

Since the best microwave transistors available are not yet characterized with published parameters, it was decided to build a test fixture with a single transistor and its biasing circuitry. The first test fixture and biasing technique used are shown in figures 2-20 and 2-21. The capacitors are large coupling and bypass capacitors. OSM type stripline connectors are used at input and output. The impedances at the connectors are the input and output impedances of the test transistor since the connecting lines are a half wavelength at 2100 MHz. The biasing is applied to the transistors via shorted quarter wave lines which appear as open circuits at the transistor terminals at the signal frequency.

The biasing configuration first tried is that of figure 2-21 where the emitter current is determined by the emitter resistor. Later it was found necessary to ground the emitter to dc and change the base biasing network to include a variable resistor to set the collector current. In this case, a screw was inserted from the top ground plane and provided pressure contact to the transistor case which was electrically connected to the emitter. This improved performance considerably at the expense of a less attractive biasing scheme.

2.2.10.1 Experimental Results

The main purpose of the experiments is to determine the optimum source impedance and load impedance for the transistor. Double stub tuners are placed between generator and input, and between load and transistor output. These tuners are then simultaneously adjusted to provide the best noise figure. The test setup is shown in figure 2-22. The optimum noise figure is then found for different bias currents thereby achieving the best possible noise figure.

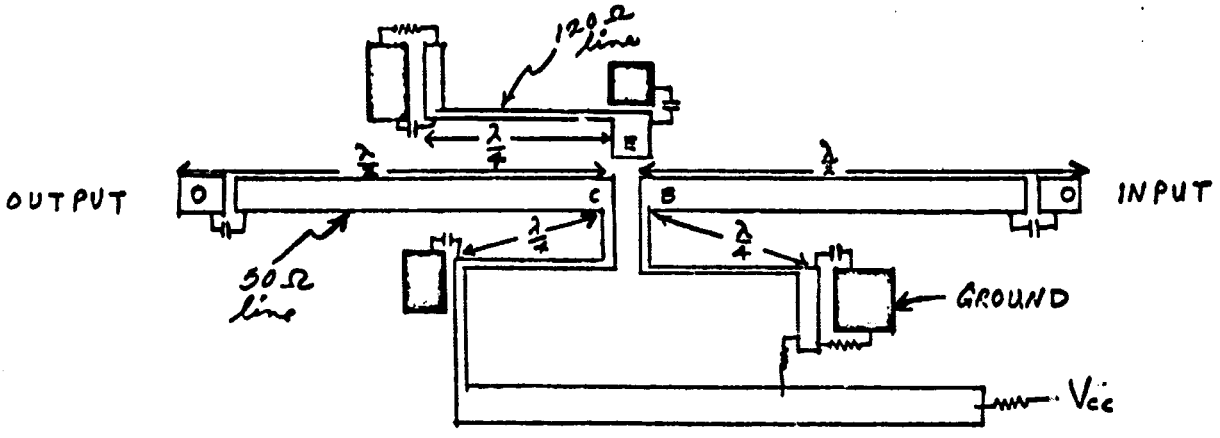


Figure 2-20. Stripline Test Fixture

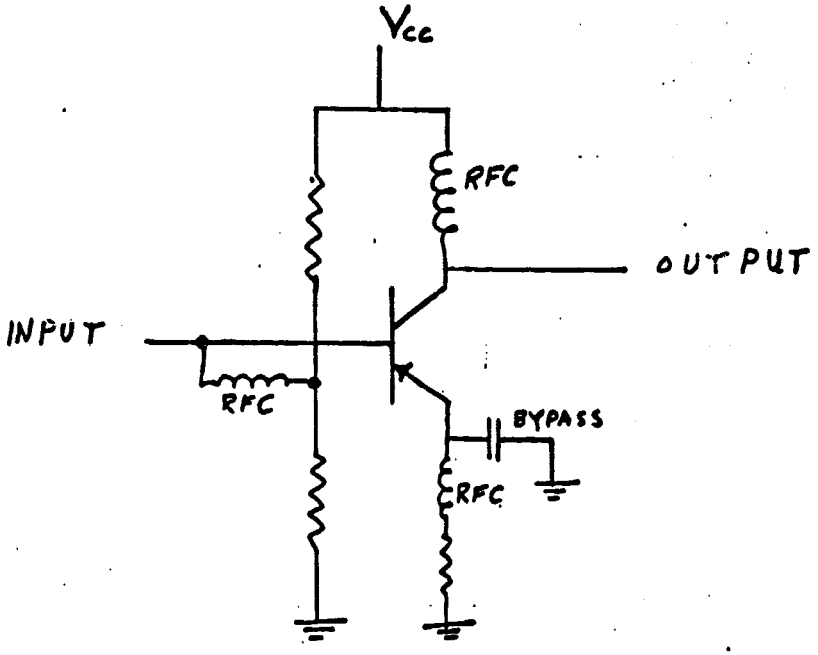


Figure 2-21. Equivalent Test Circuit

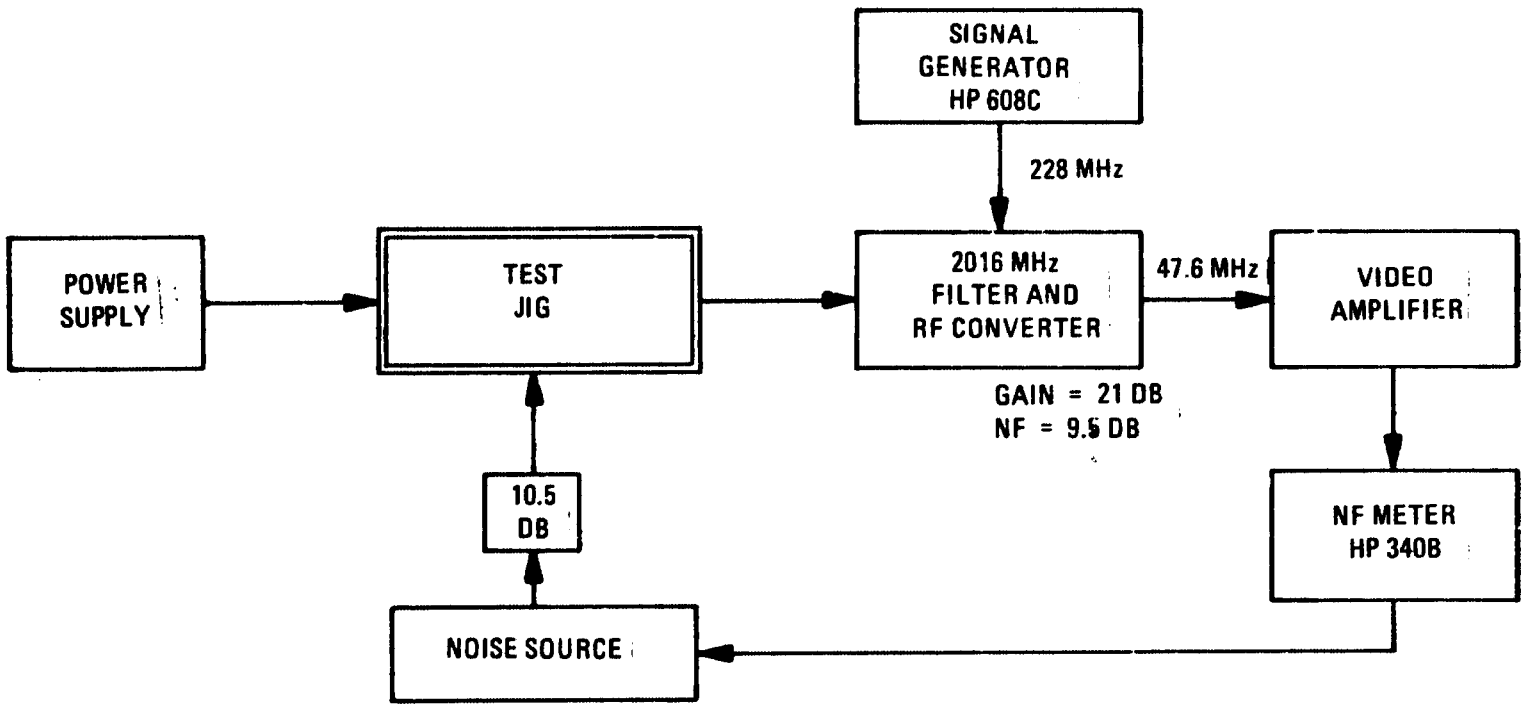


Figure 2-22. Noise Figure Test Setup

The first transistor tested using the previously described test fixture was the K5201 silicon NPN device by KMC corporation. It does not have a metal case but has 2 wide emitter leads. Only the biasing technique shown in figure 2-21 was tried. It produced a transistor noise figure of 5.5 db with 7 db gain. It is felt that this could be improved slightly by providing better emitter grounding. It is important to ground the emitter to both ground planes at the same point to suppress oscillations.

Of the commercially available transistors, the T1XM105 has the best published noise figure at 2100 MHz. Its metal case is connected to the emitter and is designed for stripline application.

The bypassed emitter resistor biasing tecnhique produced a 5.3 db noise figure with 5 db gain with the T1XM105. The emitter case was then grounded and a NF of less than 4 db with 6.5 db gain was obtained. At this noise figure the amplifier input vswr is 1.7:1.

Based upon input and output impedance measurements using slotted line techniques, matching stubs were placed on the input and output of the transistor of appropriate lengths and distances from the transistor. For a single transistor the following data was then taken at 2106 MHz.

I_E = 2 ma

NF (overall) = 6.4 db

NF (test transistor) ≅ 4 db

Gain = 6.5 db

Input vswr = 1.7:1

Output vswr = 1.4:1

R_s ≅ 35 ohms

$BW_{1\ db}$ = 115 MHz (first stage)

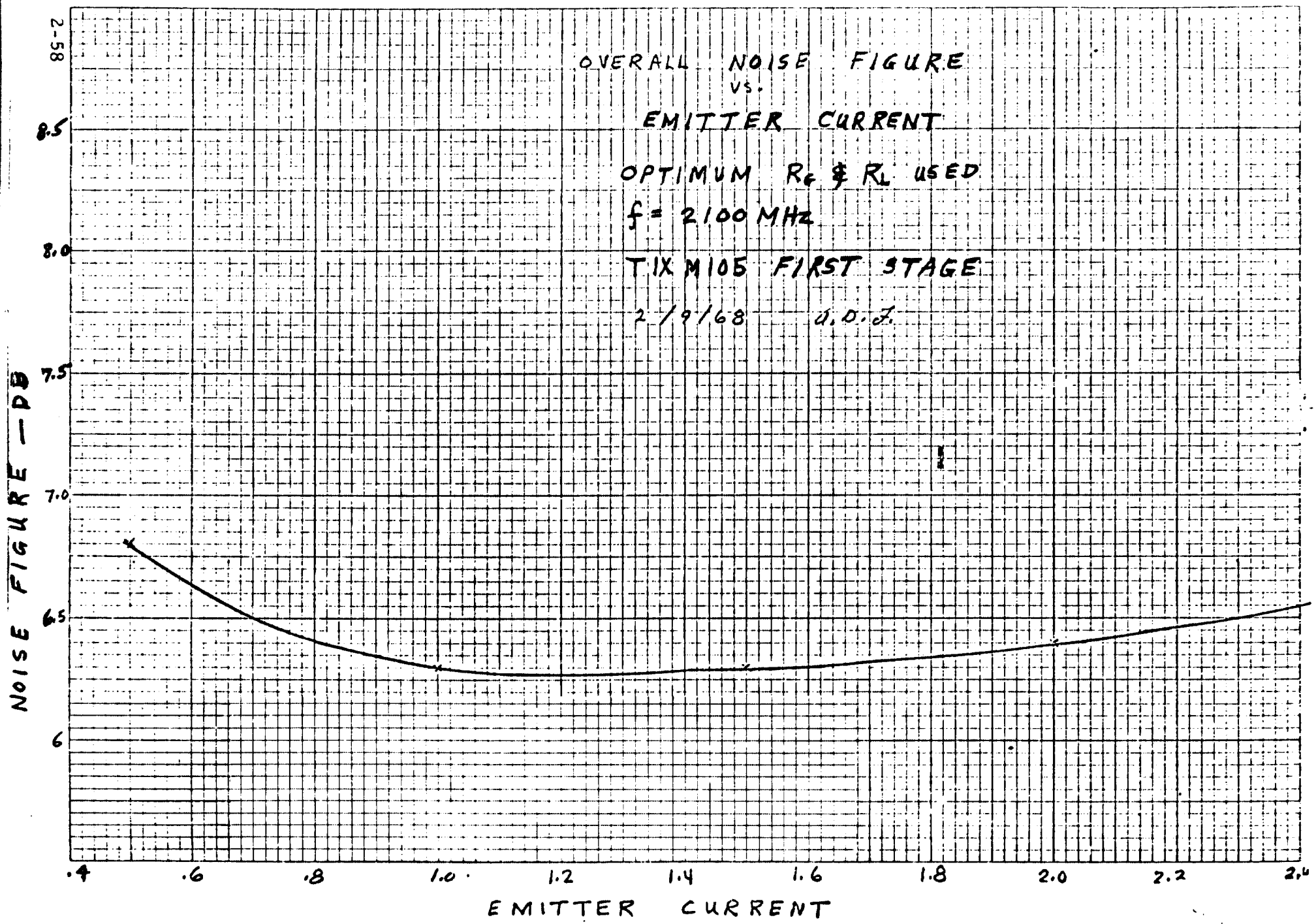


Figure 2-23. Overall Noise Figure Vs Emitter Current

It should be noted that the converter used has a noise figure of 9.5 db which is worse then succeeding stages of the S-band amplifier will have. This should then give an overall noise figure near 5 db.

It was found that the noise figure was not a critical function of bias current as predicted by figure 2-19. Figure 2-23 shows the experimentally obtained best noise figure vs emitter current. The reason for the high noise figures is that the T1XM105 stage is followed by the rf converter which has a 9.5 db noise figure. From the above information it can be concluded that, for this application, a 1.5 ma bias current is optimum.

The "typical" transistor parameters and the approximate nature of the equations used makes the calculated noise figures questionable at best. However, the real value of figures 2-16 through 2-19 lie in their general shape. They show that an optimum bias current and source resistance do exist for low noise operation. It is encouraging to note that the experimental results of NF versus current does indeed have the predicted shape.

The most important analytical result is that the noise figure vs current goes through a very broad minimum. This indicates that the choice of operating current is not too critical and can be chosen to some extent with power gain in mind. A current between 1.5 and 2 ma seems a reasonable choice. On the basis of experiments thus far, it seems likely that an amplifier with a noise figure between 4.5 and 5 db can be built using Germanium devices.

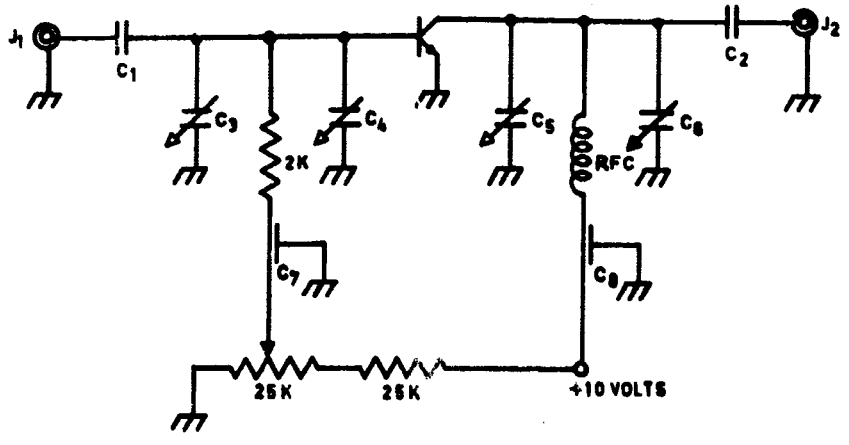
2.2.10.2 KD5201 and KD5525 Transistors Data Sheets

from KMC SEMICONDUCTOR CORPORATION **NEW**

KD5201 & KD5204 IN OUR EXCLUSIVE K DISK PACKAGE ARE SPECIFICALLY DESIGNED FOR SUPERIOR PERFORMANCE IN L&S BAND AMPLIFIER APPLICATIONS.

- **NEW DOUBLE EMITTER HERMETIC PACKAGE GIVES 10 d.b. IMPROVEMENT IN FORWARD TO REVERSE GAIN**
- **ULTRA LOW NOISE – 3 d.b. MAXIMUM SYSTEM N.F. @ 1 GHz**
- **ULTRA HIGH F_T – 1.8 GHz GUARANTEED MINIMUM F_T**
- **ULTRA HIGH Fmax – 6 GHz TYPICAL UNITY POWER GAIN**
- **NPN SILICON – EPITAXIAL PLANAR CONSTRUCTION FOR HI-REL MILITARY APPLICATIONS**

TEST CIRCUIT 1 GHz AIR STRIP-LINE AMPLIFIER



3 db System Noise Figure Guaranteed when tested in this circuit

C_1 - C_2 – 470 pf no lead ceramic disks
$C_{3\text{-}4\text{-}5\text{-}6}$ – 1-6 pf concentric air trimmers
C_7 - C_8 – 1000 pf mica feed thru's
J_1 - J_2 – Type "N" co-axial connectors

Note:
C_1 soldered to J_1 and C_3
C_3 mounted 1 inch center to center from C_4 – Base lead of transistor tied directly to C_4 –5/16" copper strap joins C_3-C_4

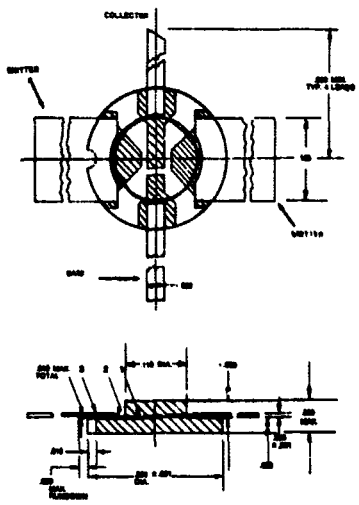
KD5201
KD5204

ALL TESTS AT 25° C. ± 3° C. AMBIENT, UNLESS OTHERWISE STATED.

PARAMETER	CONDITION	MIN.	MAX.	UNITS
V_{CBO}			25	Volts
V_{CEO}			12	Volts
V_{EBO}			2.5	Volts
Junction Temperature		−65	+200	°C
Power Diss.	@ 25°C Ambient		125	MW
BV_{CBO}	@ I_C = 10 μ amps	25		Volts
BV_{EBO}	@ I_E = 10 μ amps	2.5		Volts
I_{CBO}	@ V_{CB} = 15 Volts		0.05	μ amps
h_{FE}	@ I_C = 3 ma. @ V_{CE} = 1 Volt	20	300	
C_{ob}	@ V_C = 10 Volts		1.0	pf.
f_t	V_C = 6 Volts I_C = 5 ma.	1800		MHz
G_{pe} for KD5201	f = 1GHz BW. = 10%	10		db
	V_C 6 Volts I_C 1 5 ma.		15	db typical
G_{pe} for KD5204	f = 1GHz BW. = 10%	10		db
	V_C = 6 Volts I_C = 1.5 ma.		13	db typical
N.F. for KD5201	f = 1GHz BW. = 2% V_C = 6 Volts I_C = 1.5 ma.		3	db
N.F. for KD5204	f = 1GHz BW. = 2% V_C = 6 Volts I_C = 1.5 ma.		4	db

K DISK

LOW INDUCTANCE MICROWAVE PACKAGE



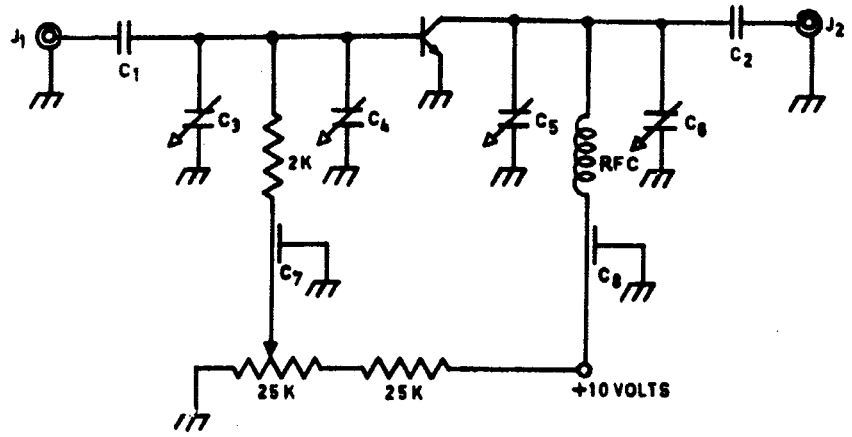
1. Beryllium Oxide disc
2. Metalizing
3. Kovar lead frame, gold plated

from KMC SEMICONDUCTOR CORPORATION NEW

KD5525 & KD5526 IN OUR EXCLUSIVE K DISK PACKAGE ARE SPECIFICALLY DESIGNED FOR SUPERIOR PERFORMANCE IN L&S BAND AMPLIFIER APPLICATIONS.

- **NEW DOUBLE EMITTER HERMETIC PACKAGE GIVES 10 d.b. IMPROVEMENT IN FORWARD TO REVERSE GAIN**
- **ULTRA LOW NOISE – 3 d.b. MAXIMUM SYSTEM N.F. @ 1 GHz**
- **ULTRA HIGH F_T – 2.0 GHz GUARANTEED MINIMUM F_T**
- **NPN SILICON – EPITAXIAL PLANAR CONSTRUCTION FOR HI-REL MILITARY APPLICATIONS**

TEST CIRCUIT 1 GHz AIR STRIP-LINE AMPLIFIER



3 db System Noise Figure Guaranteed when tested in this circuit

C_1 - C_2 – 470 pf no lead ceramic disks
$C_{3\text{-}4\text{-}5\text{-}6}$ – 1-6 pf concentric air trimmers
C_7 - C_8 – 1000 pf mica feed thru's
J_1 - J_2 – Type "N" co-axial connectors

Note:
C_1 soldered to J_1 and C_3
C_3 mounted 1 inch center to center from C_4 – Base lead of transistor tied directly to C_4 –5/16" copper strap joins C_3-C_4

SEMICONDUCTOR Kmc CORPORATION

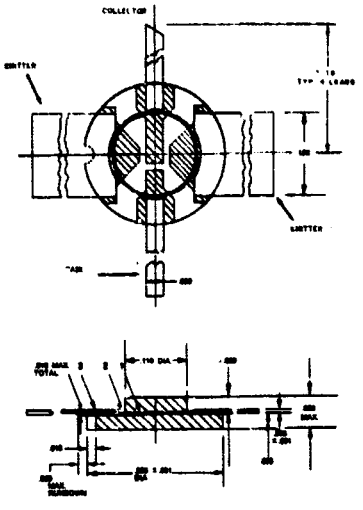
KD5525
KD5526

ALL TESTS AT 25° C. ± 3° C. AMBIENT, UNLESS OTHERWISE STATED.

PARAMETER	CONDITION	MIN.	MAX.	UNITS
V_{CBO}			20	volts
V_{CEO}			12	volts
V_{EBO}			2.5	volts
Junction Temperature		−65	+ 200	°C
Power Diss.	@ 25°C Case		450	mw
BV_{CBO}	@ I_C = 10 μ amps	20		volts
BV_{EBO}	@ I_E = 10 μ amps	2.5		volts
I_{CBO}	@ V_{CB} = 10 Volts		0.05	μ amps
h_{FE}	@ I_C = 3 ma. @ V_{CE} = 1 Volt	20		
C_{ob}	@ V_C = 10 Volts		0.75	pf.
f_t	V_C = 10 Volts I_C = 10 ma. f = 400 MHz	2.0		GHz
G_{pe} for KD5525	f = 1 GHz BW. = 10% V_C = 6 Volts I_C = 3 ma.	12	15	db db typical
G_{pe} for KD5526	f = 1 GHz BW. = 10% V_C = 6 Volts I_C = 5 ma.	14	16	db db typical
N.F. for KD5525 $90	f = 1 GHz BW. = 2% V_C = 6 Volts I_C = 3 ma.		3	db
N.F. for KD5526 $50	f = 1 GHz BW. = 2% V_C = 6 Volts I_C = 3 ma.		4.5	db

K DISK

LOW INDUCTANCE MICROWAVE PACKAGE



1. Beryllium Oxide disc
2. Metalizing
3. Kovar lead frame, gold plated

2.3 AGC I-F AMPLIFIER

2.3.1 Introduction

This subsection describes development of a 45 MHz i-f amplifier used in the Advanced S-Band Transponder. This i-f amplifier is a broadband, untuned, amplifier with AGC and an input filter to set the input noise bandwidth. The objectives were to design and build an i-f amplifier that would meet the requirements of the receiver and demonstrate a capability in the following areas.

1. Reduced size and weight.
2. Reduced power consumption.
3. Use of integrated circuits in circuit miniaturization.

2.3.2 Requirements

This i-f amplifier is to be used in a single conversion receiver. It must provide all of the gain from the mixer to the point where the channels split (wideband and narrowband). The AGC must have the dynamic range necessary to cover the range of input signal levels. The input filter shall set the input noise bandwidth and provide rejection to undesired out-of-band signals. Some basic assumptions were made concerning the parameters of the rest of the receiver in order to develop the requirements for the i-f amplifier. These assumptions are listed below.

Receiver Front End Noise Figure, 7 db maximum

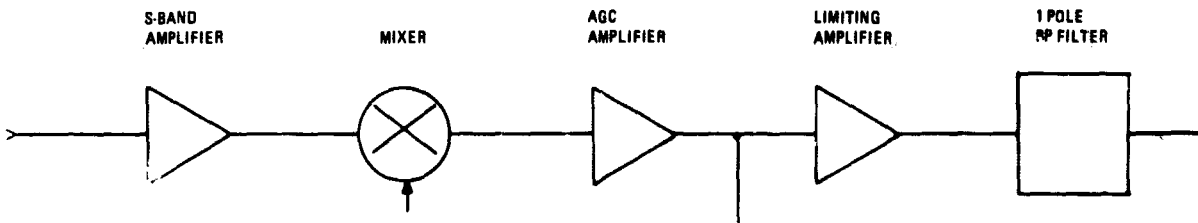
Equivalent Noise BW through the mixer, 25 MHz

Gain from front end through mixer, 30 db

Minimum Input Signal Strength, -140 dbm

Maximum Input Signal Strength, -40 dbm

I-F output AGC Operating Level, -40 dbm



MAX NOISE FIGURE (DB)	7										
GAIN (DB)		+25		+5		+70/-30 IN LOCK +76 OUT OF LOCK		+50		-1	
STRONG SIGNAL INPUT (DBM)	-40		-15		-10		-40		+1		0
WEAK SIGNAL INPUT (DBM)	-140		-115		-110		-40				
EQUIV NOISE BANDWIDTH		25 MHz							10 MHz		
BANDWIDTH REDUCTION (DB)						4					
MAX NOISE POWER (DBM) (LOCKED AT -140 DBM)	-93		-68		-63		+3				
MAX NOISE POWER (DBM) (OUT OF LOCK)	-93		-68		-63		+9				
EXCESS GAIN TO ASSURE HARD LIMITING (DB)								9			
EXCESS GAIN IN AGC AMPL (DB)						6					

FOLDOUT FRAME 1

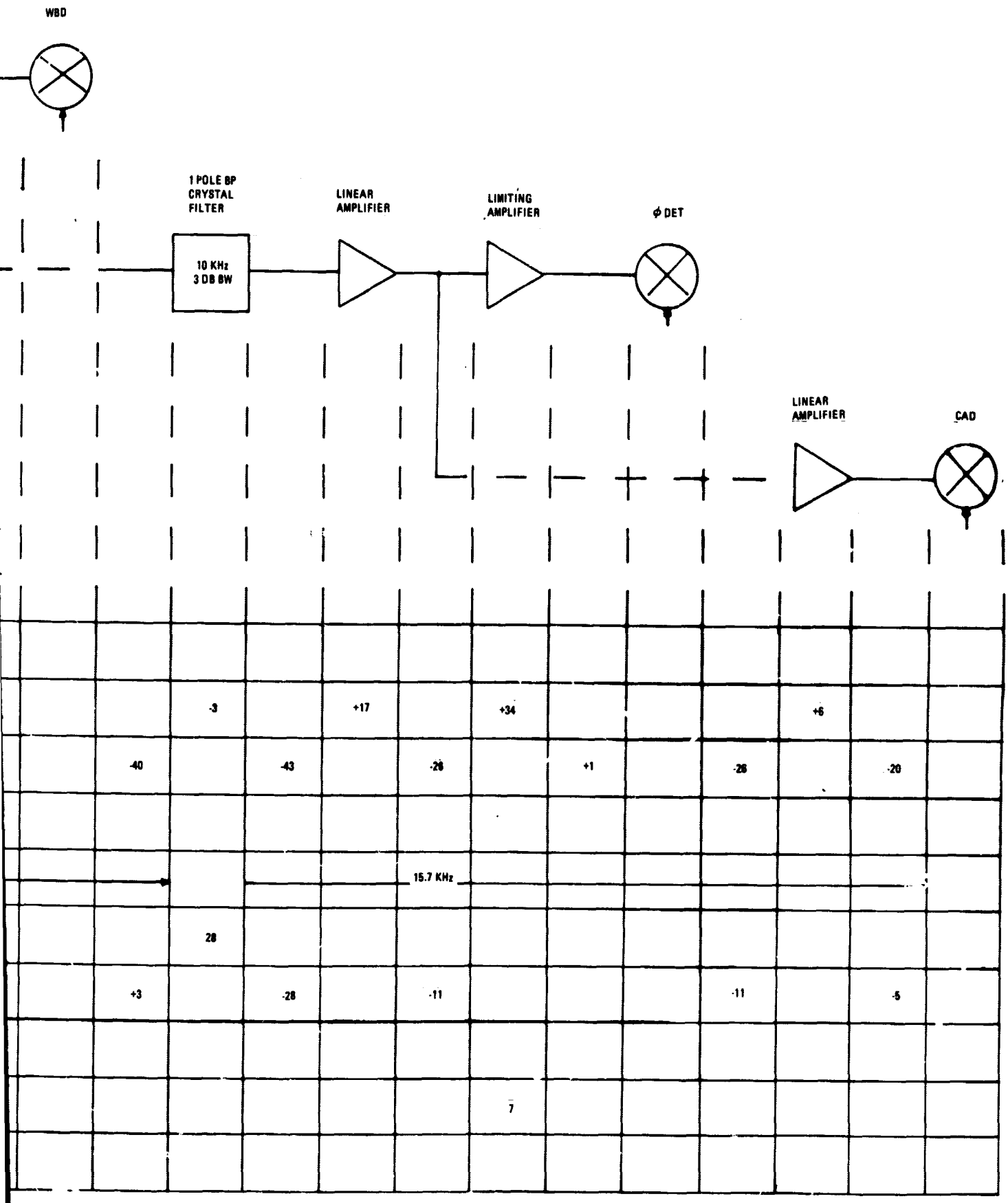


Figure 2-24. AGC I-F Amplifier, Block Diagram

FOLDOUT FRAME 2

Using the above assumptions the block diagram of figure 2-24 was constructed to show the distribution of gain and bandwidth, and to show power levels from the receiver front end to the three detectors (wideband, narrowband, and coherent amplitude).

The design goals for the i-f amplifier are listed below:

AGC Dynamic Range	106 db
AGC Voltage Range	0 to -4 volts
Maximum I-F Gain	+76 db
Minimum I-F Gain	-30 db
Input Filter Center Frequency	45 MHz
Input Filter 3 db Bandwidth	8 MHz
Input Filter Response	3 pole 0.1 db Chebyshev
Supply Voltage	-6 volts
Current Drain	low as possible

2.3.3 Survey of Available Integrated Circuits

A survey of available integrated circuits was made to determine what devices could possibly be used as broadband AGC amplifiers at 45 MHz. The criteria used in selecting possible devices are listed below.

1. 20 to 50 db of gain from 20 to 100 MHz
2. Good limiting characteristics
3. Automatic gain control
4. Only one 6 volt supply required
5. Few or no external parts required

The devices that showed the most promise are tabulated in table 2-4. The two most promising devices in the above list were the PA7600 and the PA7713. These two devices were tested and found to have the following undesirable characteristics.

1. Several external components were required for compensation and tuning.
2. Bandpass shifts drastically with AGC.
3. AGC range is covered with less than 300 mv of change in the AGC voltage.

The decision was made to abandon further effort on trying to fit commercially available IC's to this application. Instead, effort was directed toward designing and building our own integrated circuits by employing the services of Motorola's Hybrid Integrated Circuit Facility.

2.3.4 Hybrid Integrated Circuit Approach

The objective of the hybrid circuit design effort was to develop a set of hybrid circuits that could be used to build the i-f amplifier and could also be used in other applications in the receiver. The design objectives for these circuits are listed below.

1. Circuits must operate from -6 volt supply.
2. Circuits must have very low power consumption.
3. Circuits must be complete, i.e. requiring no external parts for compensation, tuning, coupling or decoupling.
4. Design a minimum of different circuits to satisfy a maximum of applications in the i-f amplifier and the rest of the receiver.

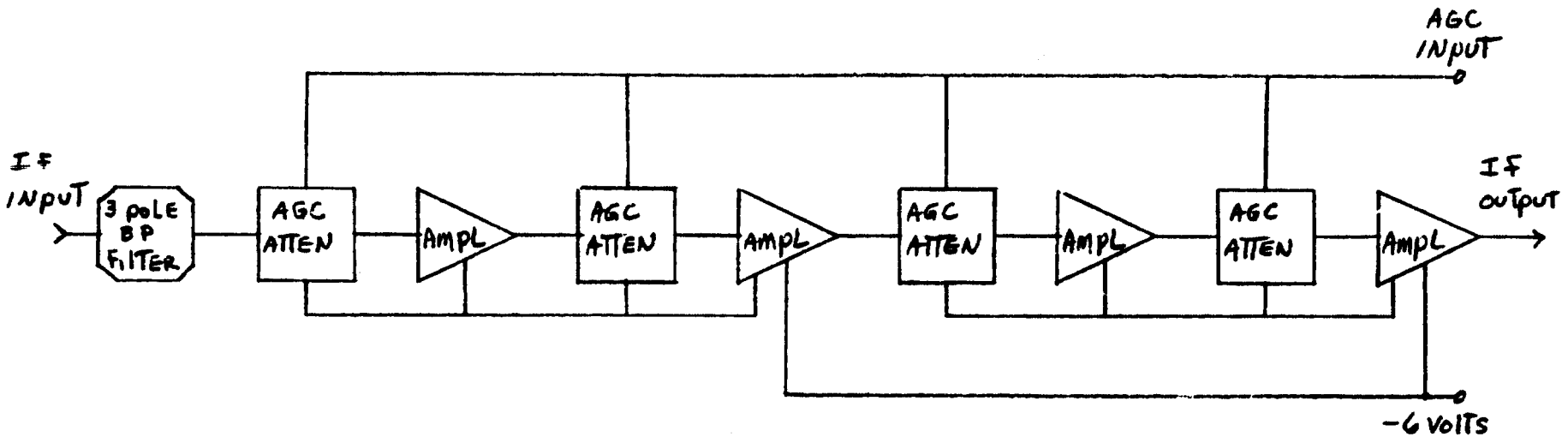
With these design objectives in mind a block diagram (figure 2-26) of the i-f amplifier was constructed. This shows that the i-f amplifier could be built with three different kinds of IC's. Four circuits were actually developed during this effort. They were (1) bandpass filter, (2) AGC attenuator, (3) feedback pair amplifier, and (4) limiter amplifier. The reason for the two kinds of amplifiers

Device	Type of Amplifier		Remarks
	Limiter	AGC	
RCA CA3028	x	x	Must be tuned to operate at 45 MHz, requires many external parts.
Motorola MC1550 MC1550G		x	Must be tuned to operate at 45 MHz, requires many external parts
Motorola MC1552			High gain video amplifier, not broad enough.
Sylvania SA20 SA21			Appears to have good gain and bandwidth but requires 20 to 25 volt supply.
Motorola MC1110	x	x	Emitter coupled pair, requires many external parts, low gain.
Philco PA 7600		x	50 MHz matched power gain = 45 db, Nf = 5 db, uses -6 volt supply, looks promising.
Philco PA 7601		x	Similar to PA 7600, uses $\pm$6 volt supplies, 18 db gain from 45 MHz to 130 MHz, looks promising.
Philco PA 7713		x	Video amplifier performance to 60 MHz, tuned amplifier performance to 200 MHz. At 60 MHz tuned, 22 db gain, 7 db noise figure. Uses +6 volt supply; looks promising.

Table 2-4. Survey of 45 MHz Amplifier Devices

Device	Type of Amplifier		Remarks
	Limiter	AGC	
Amelco 911C	x	x	Emitter coupled pair, must be tuned to operate at 45 MHz, requires many external parts.
Signetics SE510J NE510A	x	x	Dual emitter coupled pair, versatile, requires many external parts.
Motorola Hybrid IC, CR30A/23, CR29, CR30B/27	x	x	Low gain, probably requires tuning, requires some external parts.

Table 2-4. Survey of 45 MHz Amplifier Devices (cont)



GAIN -30 db TO +76 db

BANDWIDTH 8 MHz 3db

Figure 2-25. AGC I-F Amplifier Block Diagram

was that a limiter amplifier was needed in another part of the receiver and it was desirable to evaluate it on the same basis as the feedback pair amplifier for possible application in the i-f amplifier. The following sections cover the details of these four circuits.

2.3.4.1 Bandpass Filter

The input filter is a 3 pole, 0.1 db Chebichev design with center frequency at 45 MHz and 3 db bandwidth of 8 MHz. A 3 db pad is included at each end of the filter to isolate the filter from source and load impedance variations. This isolation seems necessary since the signal source is the mixer output and its impedance can vary 2:1. The load impedance that the filter sees is an AGC attenuator connected to a feedback pair amplifier. This impedance can vary 3:1 as the AGC voltage is varied. The schematic of the filter is shown in figure 2-26. Figure 2-27 shows a sketch of the internal construction.

One hybrid version of this filter was built. Slight "tuning" was necessary to center the response at 45.0 MHz. This tuning was done quite easily by slightly adjusting the turns on the inductors L_1, L_2 and L_3. This was done before the lid was sealed to the header.

Figure 2-28 shows the frequency response of the filter alone. In order to show the effect of a varying load impedance the response of figure 2-42 was taken with the filter connected to an AGC attenuator (in the i-f) and curves were taken for various AGC settings. This shows that the passband does not shift as a function of AGC.

The center frequency insertion loss of the filter is about 10 db (7 db total for the isolation pads and 3 db for the filter itself).

2.3.4.2 AGC Attenuator

The function of the AGC attenuators is to provide the attenuation needed to hold the signal level at the output of the if. amplifier at -40 dbm over the dynamic range of the input signal. It is desired to have a dynamic range capability of at least

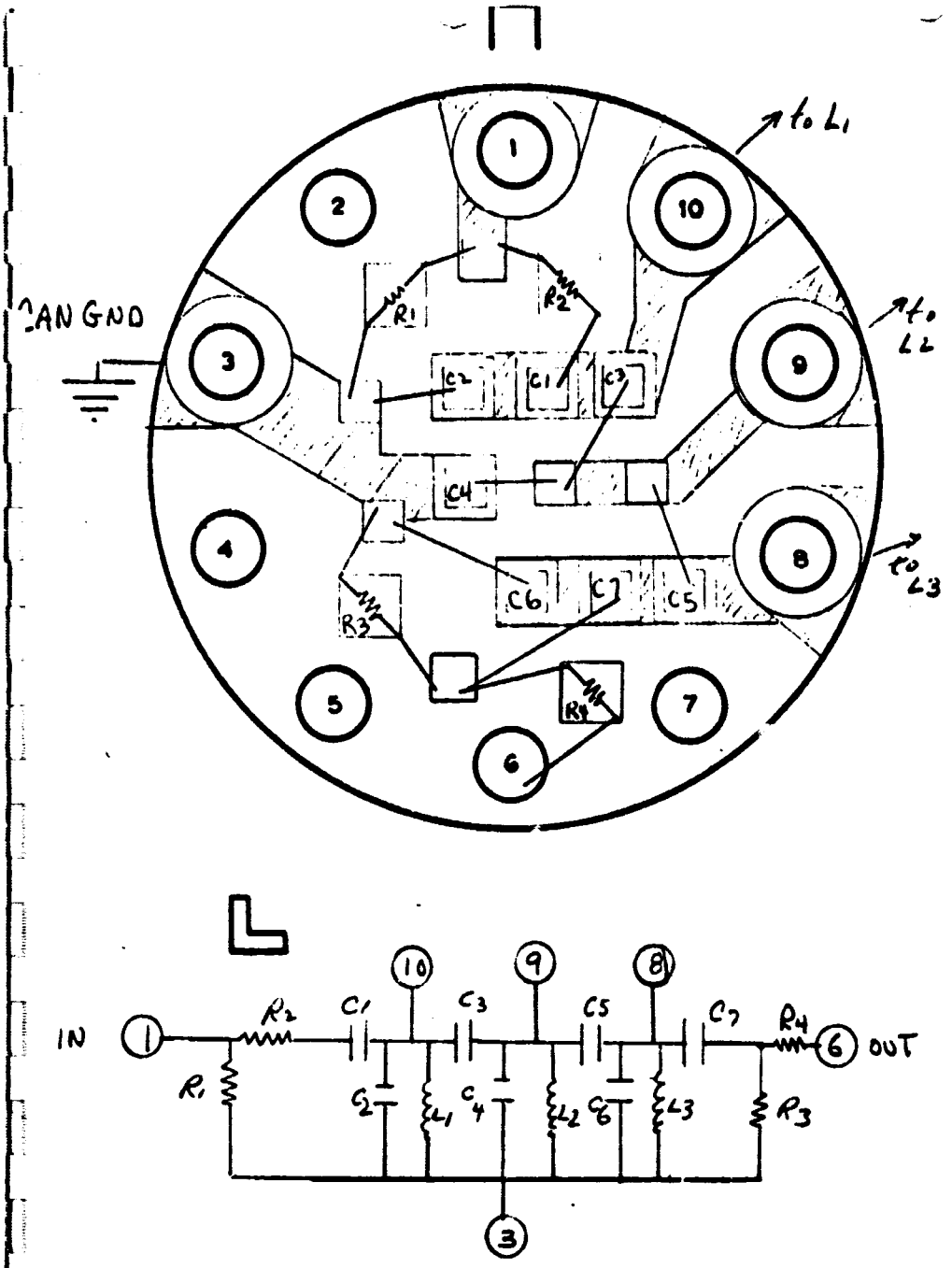


Figure 2-26.

PROBING REQUIREMENTS
R1 67Ω ± 7%
R2 39Ω ± 7%
R3 120Ω ± 7%
R4 56Ω ± 7%
C1 12pf
C2, C6 22pf
C3, C5 4.0pf ± 7%
C4 27pf
C7 15pf
L1, L2, L3 .35μh
ALL INDUCTORS ARE WOUND AS follows: 9 TURNS #38 WIRE ON CF118-Q2 CORE 7-26-68 DOS

REV.									
DATE									
EFF.									
APP'D									

CIRCUIT LAYOUT & LIST REQUIREMENTS TO-5 HEADER I. C. FACILITY

DR W. S. Lee

CK G. Wilson

APP'D

TITLE: Bandpass filter

PROJECT NO. 3433

PRINT NO.

SCALE 15:1

ORIG. ISSUE

DATE 5-22-69

PAGE 2-73

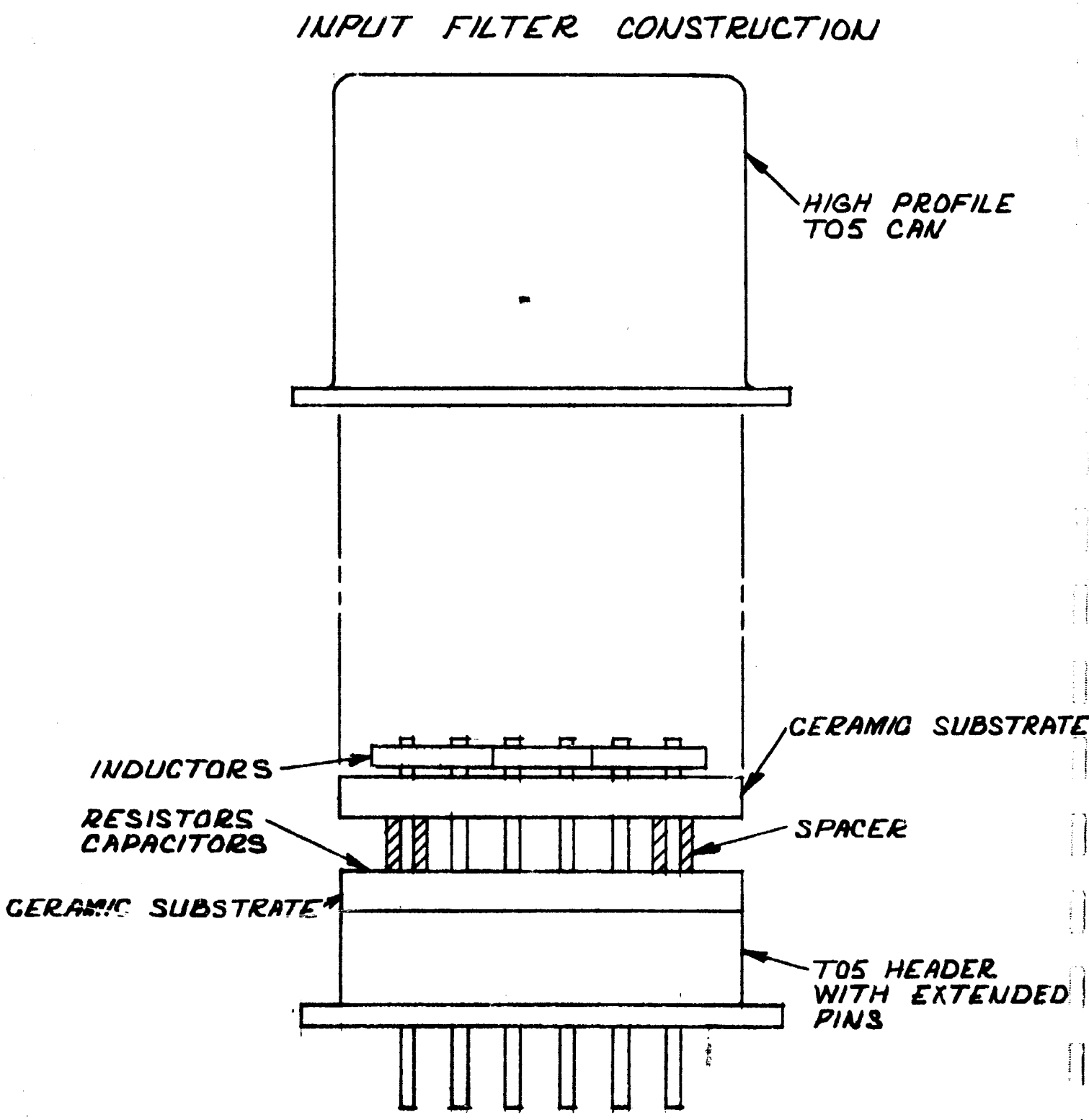


Figure 2-27. Input Filter Construction

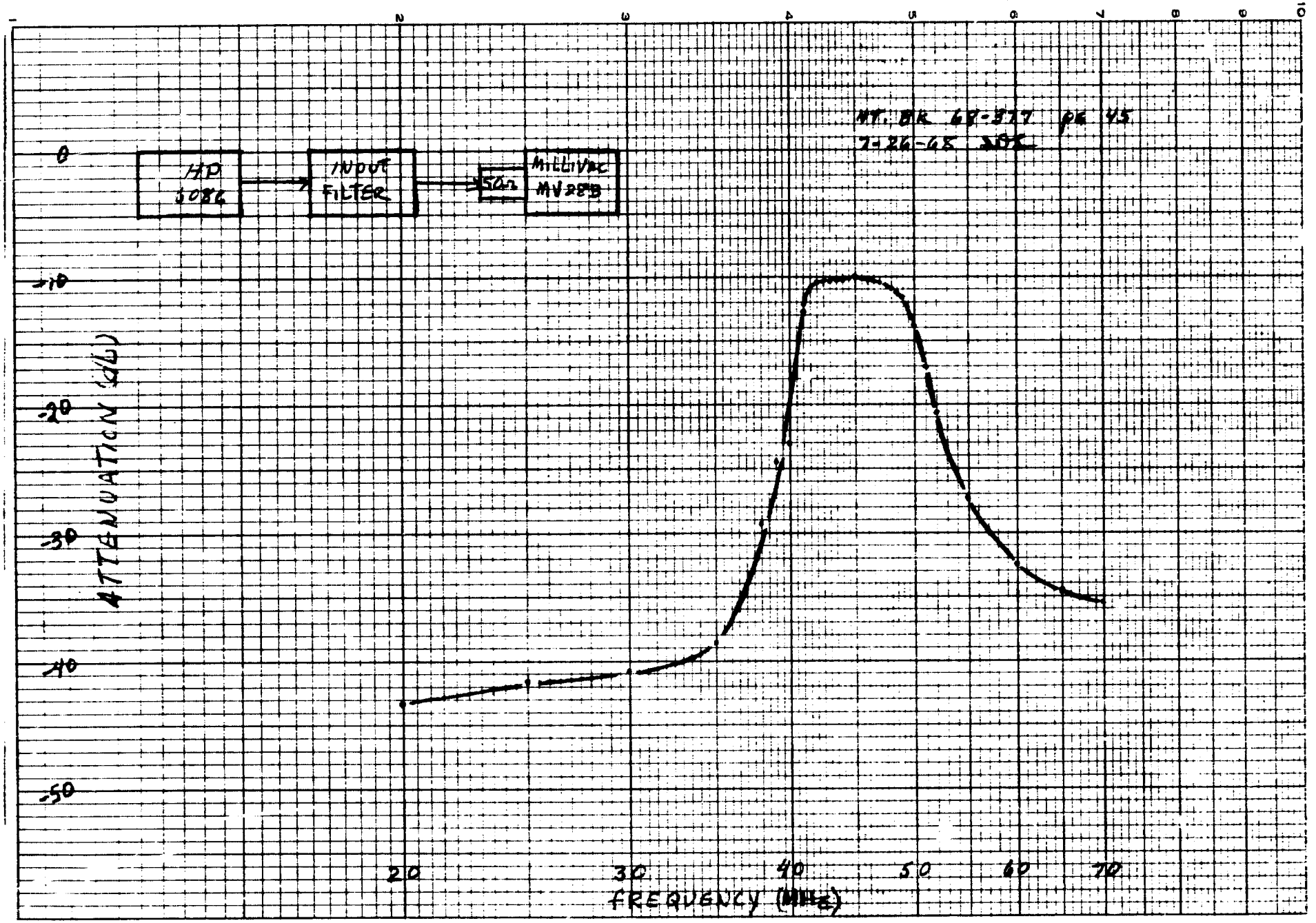


Figure 2-28. Input Filter Frequency Response

106 db, therefore with 4 AGC attenuators in the i-f each attenuator needs an attenuation range of at least 27 db. It is also desirable that the db per volt characteristic be nearly linear over the portion of the attenuation range that is used.

The schematic for the circuit is shown in figure 2-29. This is basically the same diode attenuator circuit that was used on SGLS and Block II Apollo only this one is scaled down to work from lower voltages.

C4, the bypass for CR4, is brought out on a separate pin (pin 2) to allow the flexibility of altering the shape of the attenuation characteristic by changing the shunt impedance. Pin 2 can be left open, grounded or grounded through some series resistance.

A frequency response and an attenuation curve are shown in figures 2-30 and 2-31.

The input impedance and output impedance for various AGC levels are listed below.

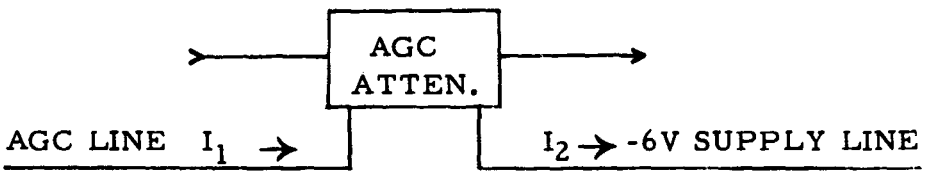
Input Impedance at 45 MHz

AGC Voltage	Z_{in} R_P	C_P
0	260 ohms	14 pf
-1	230	11
-2	260	8
-3	320	8
-4	760	6
-5	910	5

Output Impedance at 45 MHz

AGC Volts	Z_{out} R_P	C_P
0	220 ohms	11 pf
-1	155	14
-2	106	14
-3	78	12
-4	63	10
-5	47	6

The current drain on the supply line and AGC line is shown below.



AGC (Volts)	I_1 (ma)	I_2 (ma)
+1	+1.05	+1.22
0	+ .85	+1.02
-1	+ .60	+ .85
-2	+ .14	+ .70
-3	- .4	+ .54
-4	- .8	+ .41
-5	-1.2	+ .33
-6	-1.5	+ .33

The hybrid version of the AGC attenuator circuit was packaged in a 12 pin T08 can. All coupling, bypass and decoupling, components were mounted internally on the ceramic substrate. No external components are required to use this circuit.

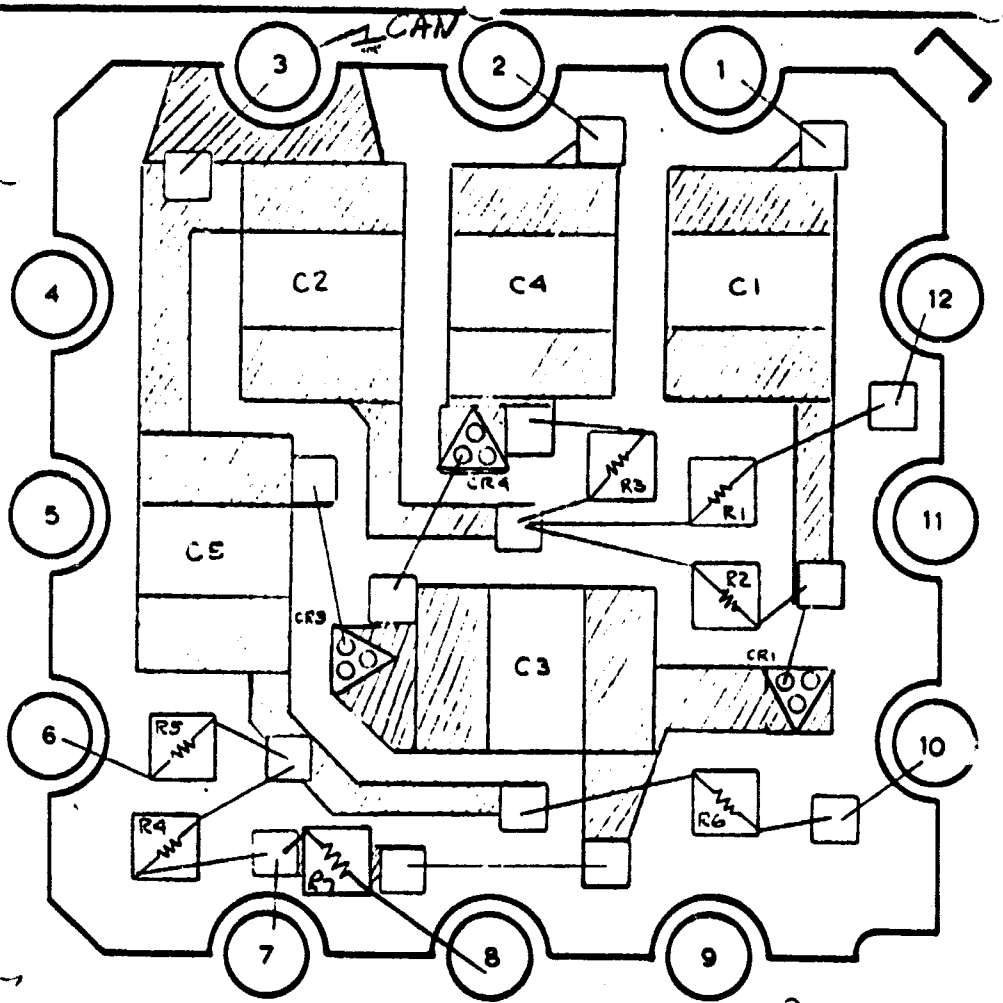
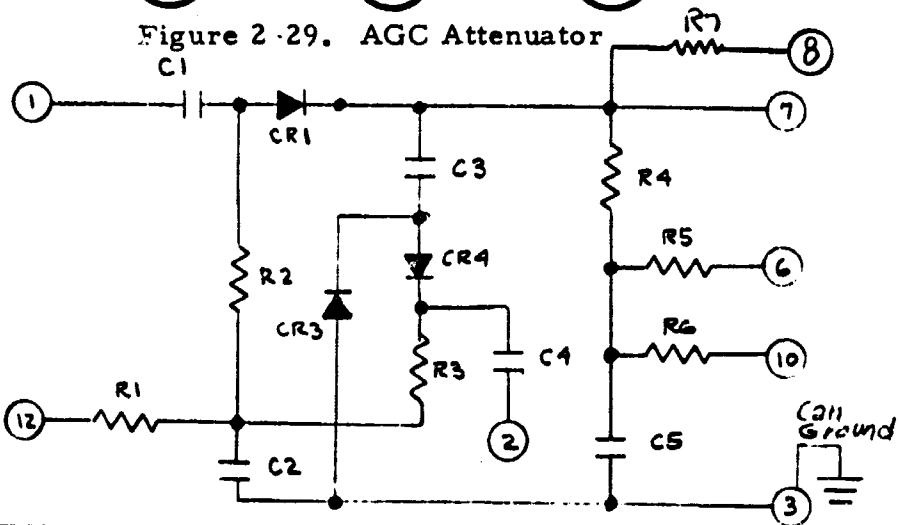


Figure 2-29. AGC Attenuator



PROBING REQUIREMENTS

RESISTORS:

R1 = 27Ω ± 7%

R2 = 1.0K ± 7%

R3 = 3.3K ± 7%

R4 = 4.7K ± 7%

R5 = 27Ω ± 7%

R6 = 27Ω ± 7%

R7 = 15K ± 7%

DIODES:

CR1, 2, 3, 4 = MSD6100

$V_{BR} > 50V$ at 1μa

V_f from .55 to .7 Volts at 1ma

CAPACITORS:

C1 = C2 = C3 = C4 = C5 =

2200 pf ± 20%

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APP'D										

CIRCUIT LAYOUT & LIST REQUIREMENTS TO-8 HEADER

2-78 **I.C. FACILITY**

DR E. HAUSER 5/9/68	TITLE AGC ATTENUATOR		
LAYOUT APPROVAL 5/9/68			
PROBE REG. APP. 5/13/68	PROJECT NO. 3433	PRINT NO.	
SCALE 15:1	ORIG. ISSUE O	DATE 5-8-68	PAGE CWT-65

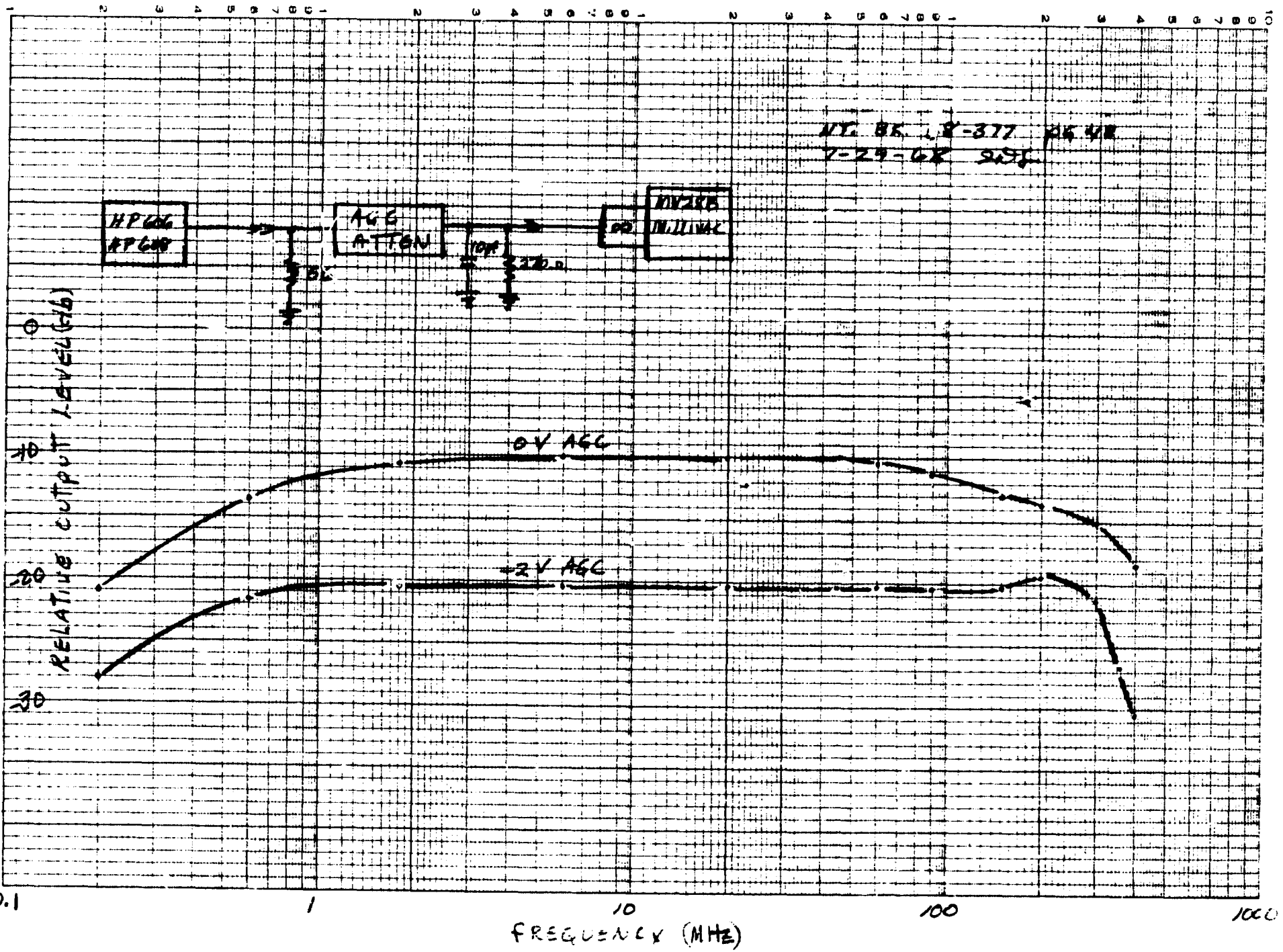

Figure 2-30. AGC Attenuator Frequency Response

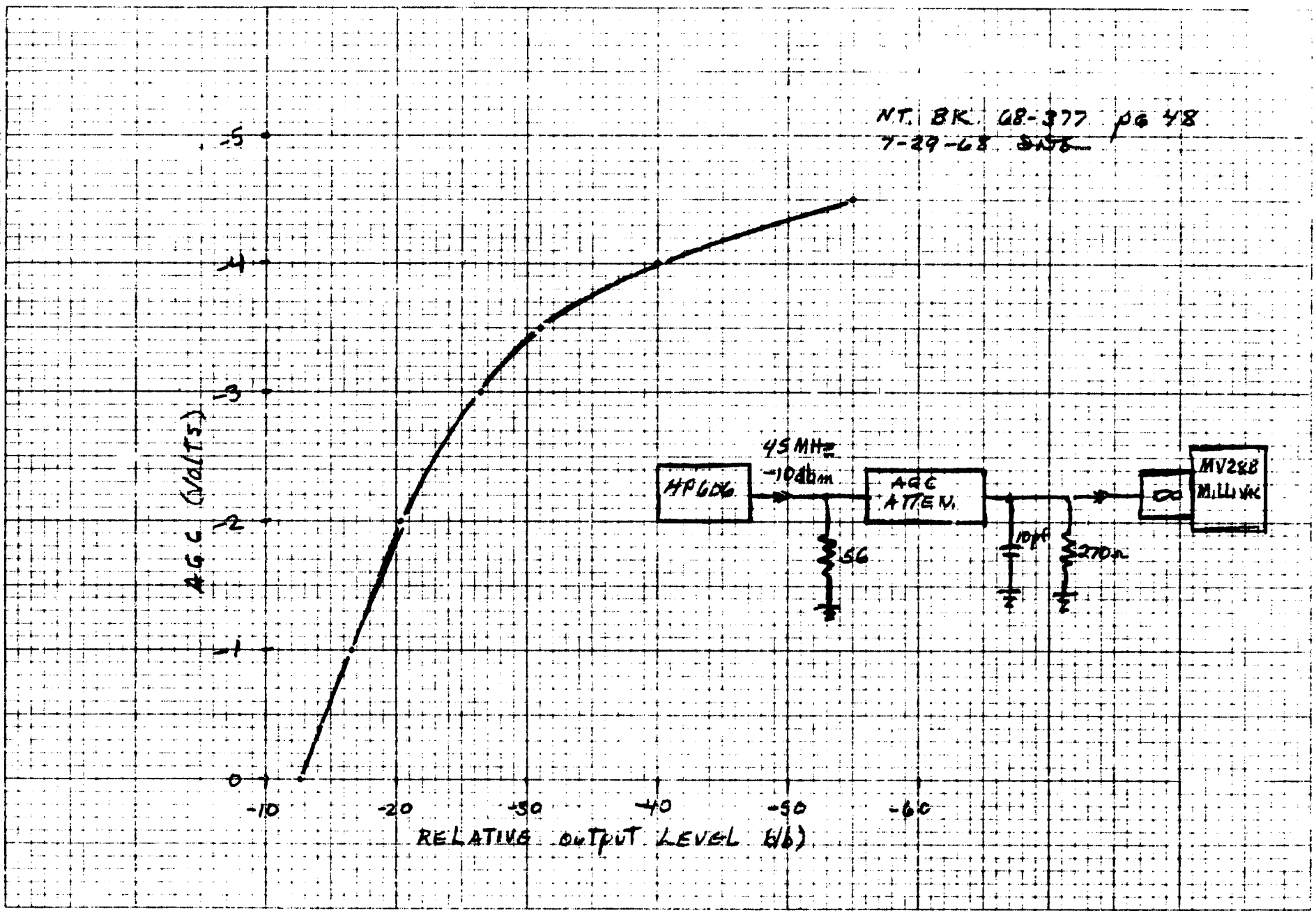

Figure 2-31. AGC Attenuation Curve

2.3.4.3 Feedback Pair Amplifier

The feedback pair amplifier is basically the same circuit that was used in the i-f on SGLS and Block II Apollo. The objective on this effort was to scale the design down to operate from lower voltage, build the amplifier in hybrid form and use it in the i-f as well as other applications in the receiver where gain from 10 to 100 MHz is needed.

The schematic is shown in figure 2-32. This circuit is complete in itself. No external parts are needed for bypassing, coupling or decoupling.

Figures 2-33 and 2-34 show frequency response (voltage gain versus frequency) and linearity data. These curves show that with a 470 ohm load the amplifier has a voltage gain of 28 db at 45 MHz and a video bandwidth of about 120 MHz. The output of the amplifier limits at 710 mv rms. The low frequency end of the response goes down to about 2 MHz. This is undesirable because gain is not needed at the low end and when several of these amplifiers are connected together, as in an i-f amplifier, there is a tendency for 1 to 2 MHz oscillations unless heavy decoupling is used on the supply line. This decoupling requires added parts that are costly in terms of size and weight.

Rolling off the low end of the frequency response on this type of a feedback amplifier is a problem since the feedback will tend to compensate for any rolloff or change within the feedback loop.

In the i-f amplifier the problem was solved by using "small" coupling capacitors between each feedback pair amplifier and AGC attenuator. This had the effect of reducing the overall i-f gain at the low end thus eliminating the low frequency oscillations. This also resulted in some loss in overall gain at 45 MHz.

The input and output impedance measured with the RX meter at 45 MHz is shown on the following page.

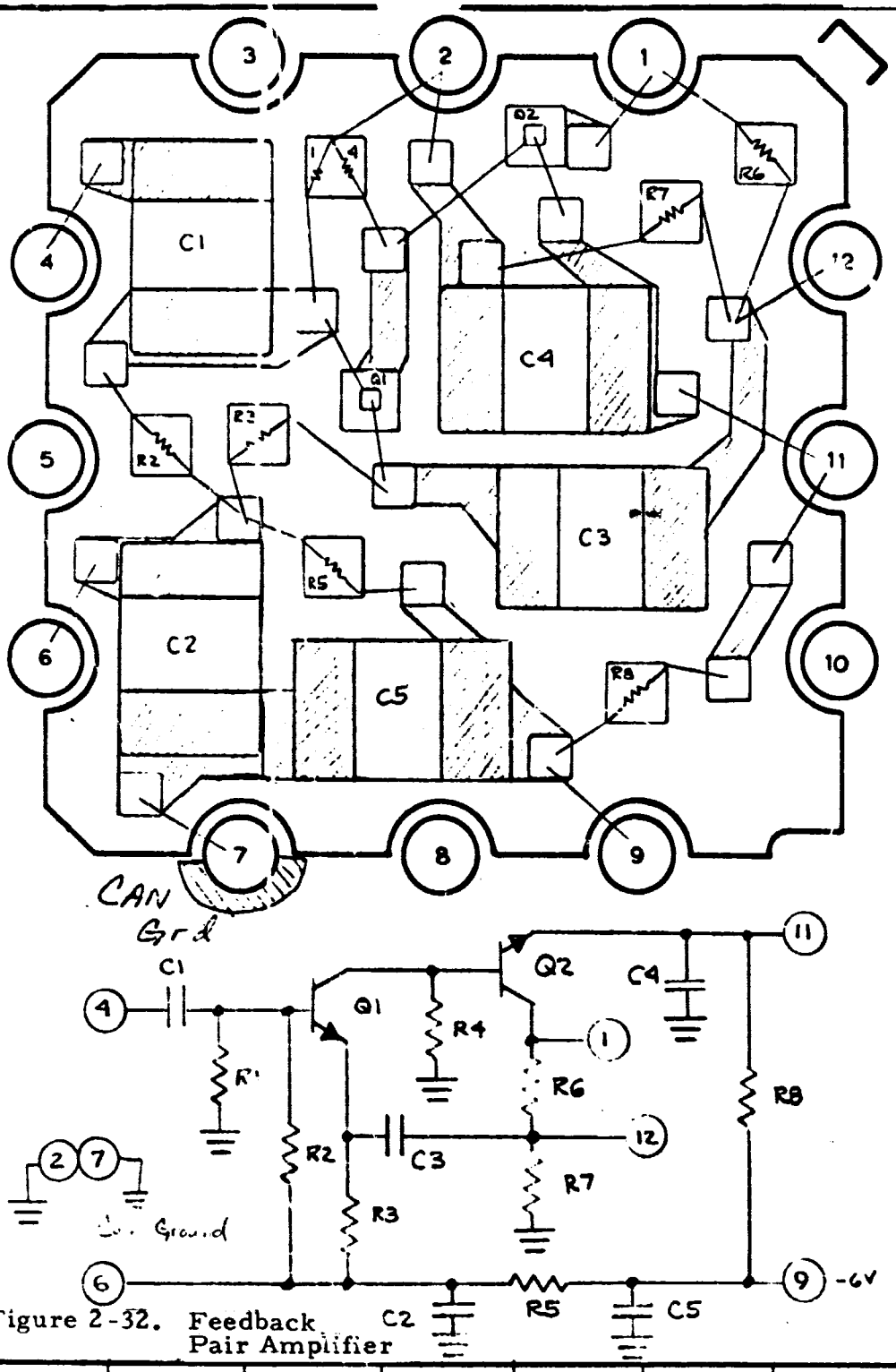

Figure 2-32. Feedback Pair Amplifier

PROBING REQUIREMENTS

RESISTORS:

1 CHIP { R1 = 10K, R4 = 2.7K, R2 = 5.6K, R3 = 1.2K } ± 7%

R5 = 27Ω ± 15%

R6 = 470Ω ± 7%

R7 = 22Ω ± 15%

R8 = 680Ω ± 7%

TRANSISTORS:

Q1 = Q2 = 2N2857 / 2N918

β > 30 @ 3 ma 1V

BV CEO 15V @ 3 ma

I CEO < .01 @ 15V

CAPACITORS:

C1 = C2 = C3 = C4 = C5 = 520 pf

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EFF.									
APP'D	WS								

CIRCUIT LAYOUT & LIST REQUIREMENTS TO-8 HEADER I.C. FACILITY

2-82

DR W SHEA	TITLE FEEDBACK PAIR AMPL		
LAYOUT APPROVAL			
PROBE REQ. APP.	PROJECT NO. 3433	PRINT NO.	
SCALE 15:1	ORIG. ISSUE O	DATE 5-3-68	PAGE -19- CWT-165

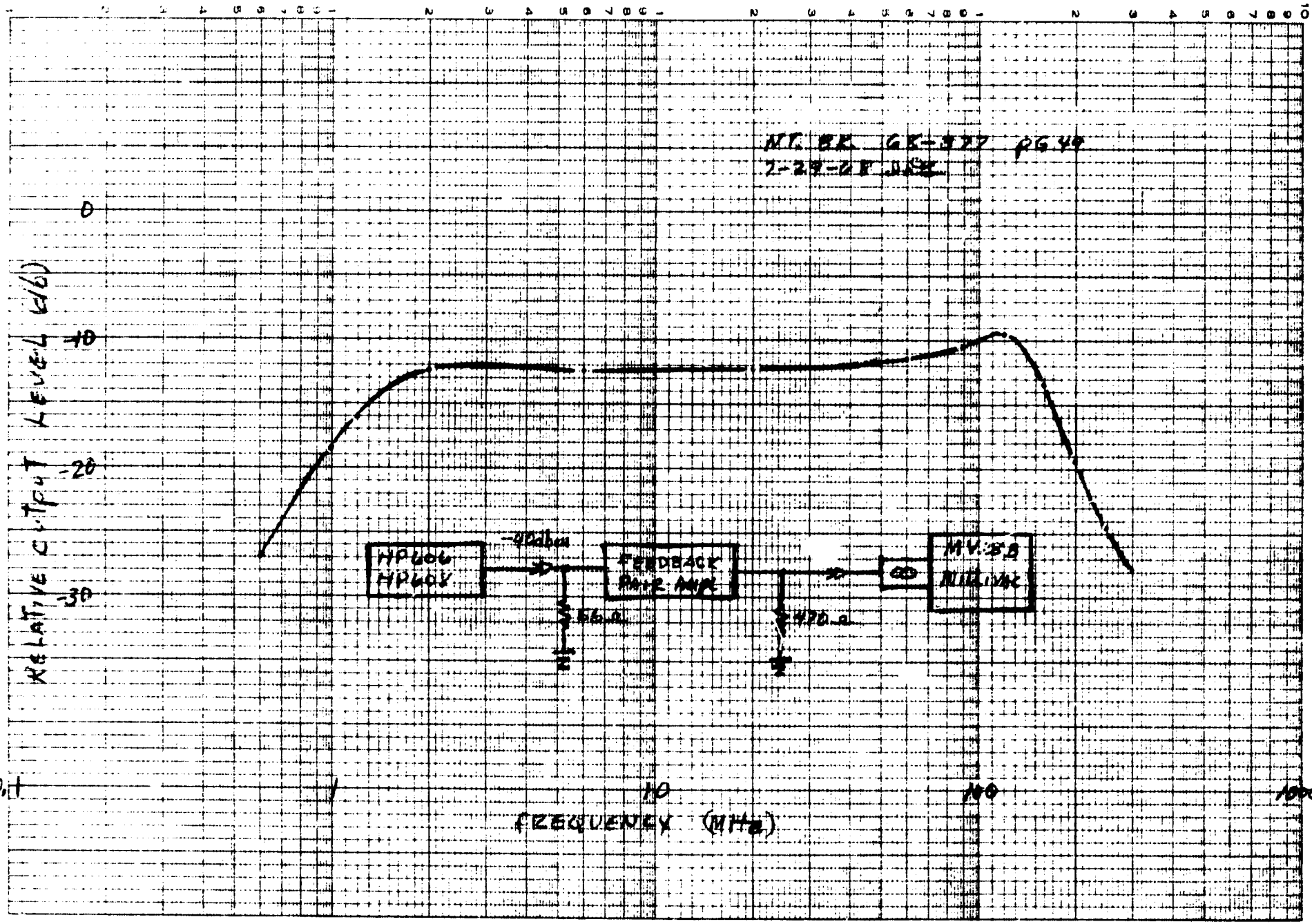


Figure 2-33. Feedback Pair Frequency Response

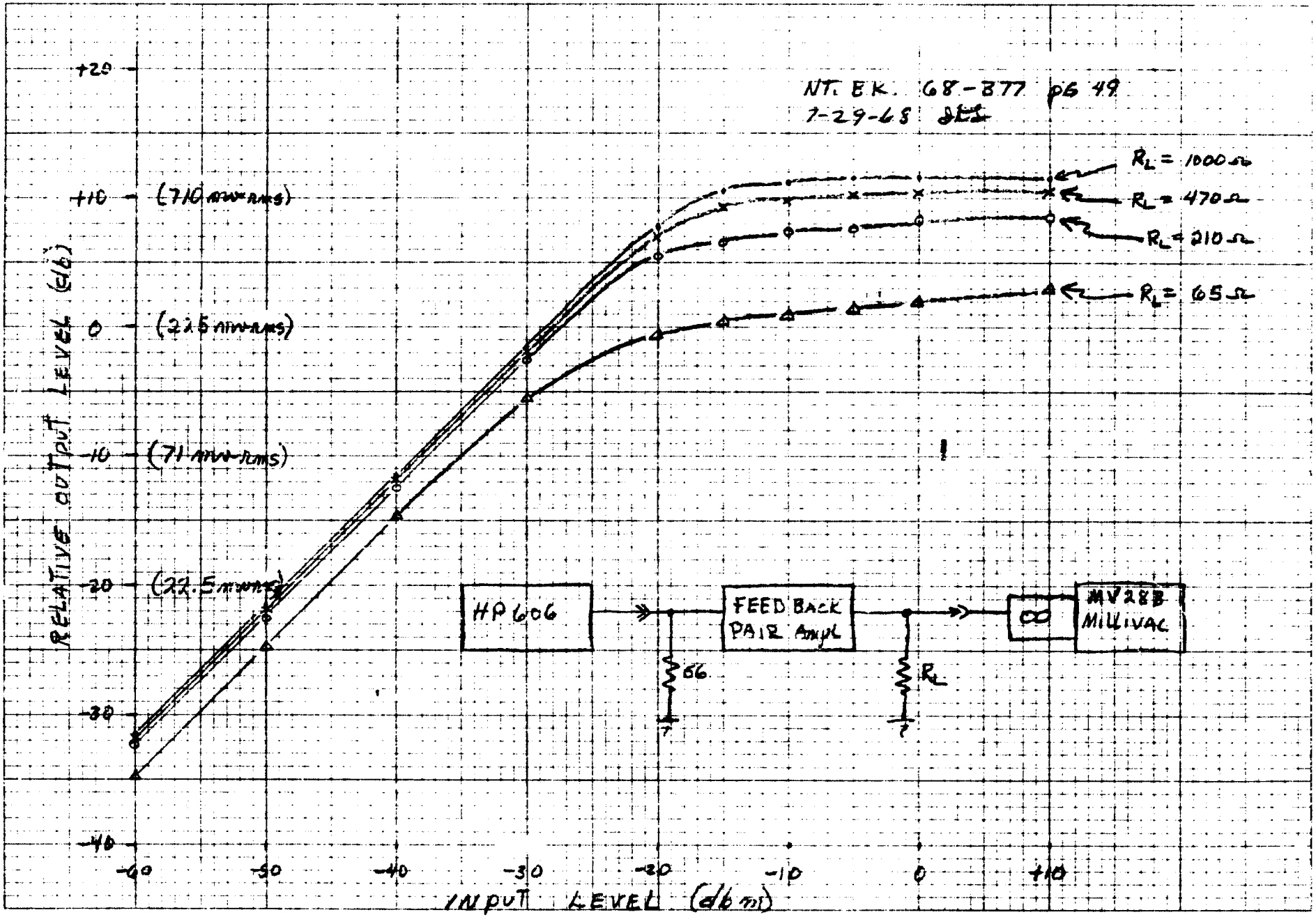


Figure 2-34. Feedback Pair Gain Linearity

$R_P = 450$

Z_{in}

$C_P = 8$ pf

$R_P \approx 50$

Z_{out}

$C_P = 1.5$ pf

The current drain from a -6 volt supply is 4.5 ma.

2.3.4.4 Limiter Amplifier

The limiter amplifier was designed mainly to be used as the limiter before the narrowband and wideband phase detectors. It also could be used as a direct replacement for the feedback pair amplifier in other applications, if its frequency response, gain, linearity and efficiency were equal to or better than, the feedback pair.

The schematic of the limiter amplifier circuit is shown in figure 2-35. The circuit is basically an emitter coupled pair amplifier with an emitter follower output fed from an transistor current source. The emitter follower output makes a dramatic improvement in the high frequency video amplifier performance since the external load capacitance is isolated from the emitter coupled pair load resistance. The transistor current souce supplies the current for the emitter follower and for the external load circuit. The emitter follower only has to be capable of driving the external load since the current source presents a high internal load impedance. This feature improves the efficiency of the amplifier.

This circuit is packaged in a 12 pin T08 can and requires no external components for decoupling, bypassing or courling. At 45 MHz the input impedance is 800 ohms in parallel with 9 pf. The output impedance is 40 ohms in parallel with 0.6 μh.

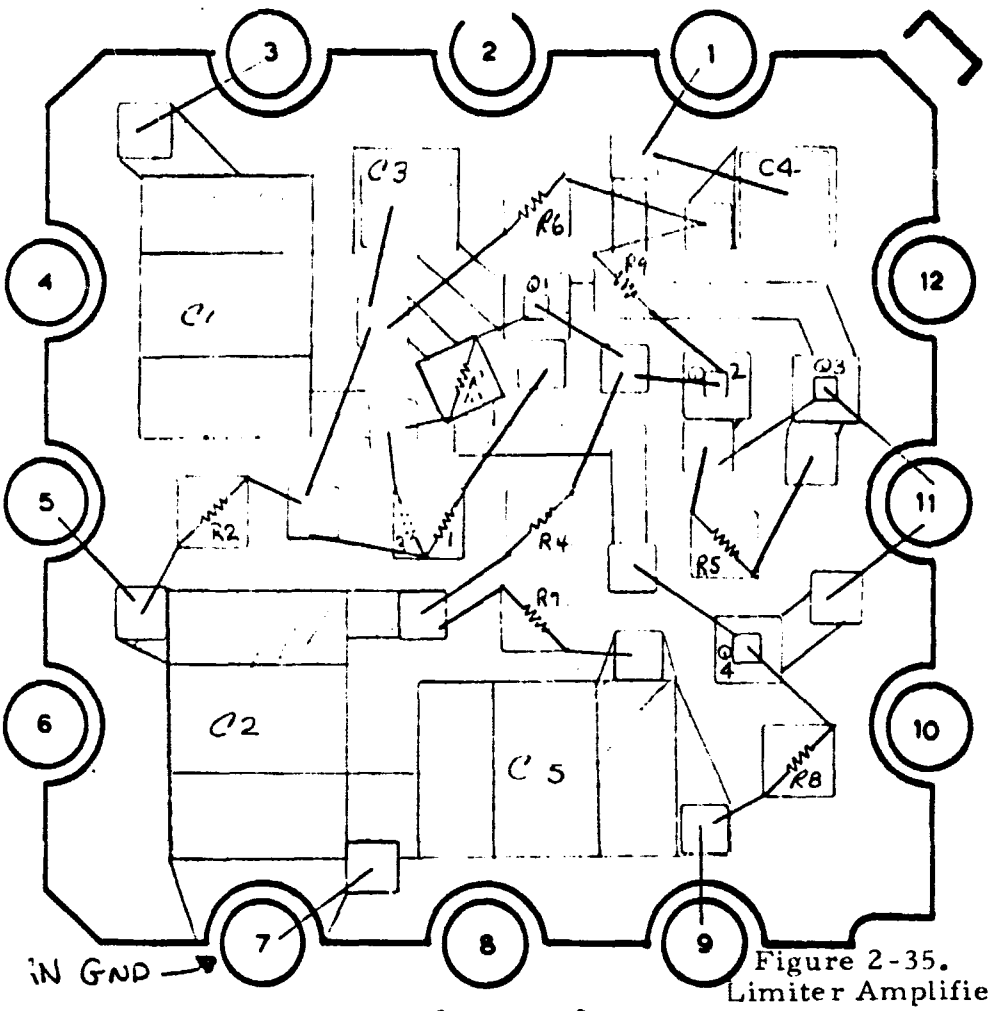
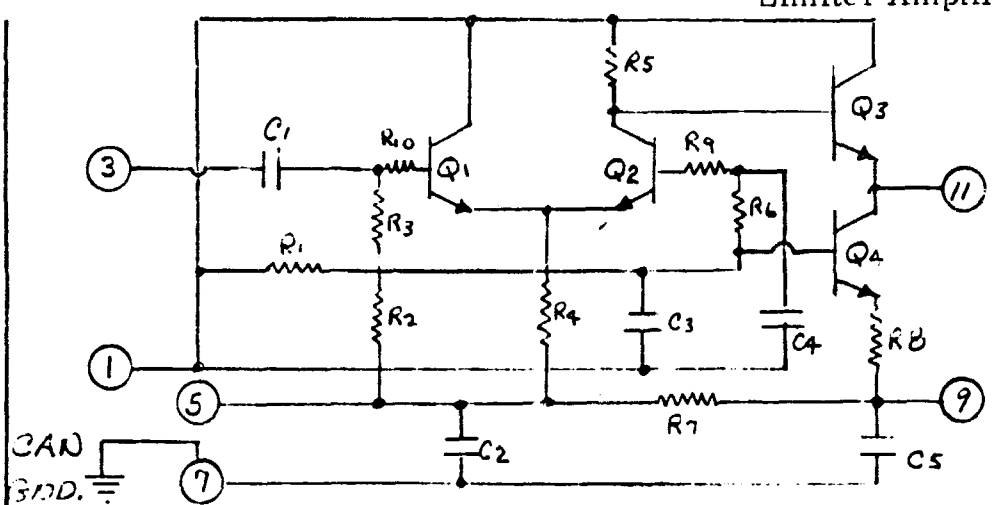


Figure 2-35. Limiter Amplifier



PROBING REQUIREMENTS

1 chip
- R_1 = 12K ± 7%
- R_3 = 1.0K ± 7%
- R_2 = 10K ± 7%
- R_4 = 680Ω ± 7%
- R_5 = 1500Ω ± 7%
- R_6 = 1.0K ± 7%
- R_7 = 27Ω ± 25%
- R_8 = 390Ω ± 15%
- R_9 = 35Ω ± 15%
- R_{10} = 35Ω ± 15%

CAPS, CERAMIC

$C_1 = C_2 = C_5$ = 1000pf

CHIP CAPS:

$C_3 = C_4$ = 47 pf

TRANSISTORS

$Q_1 = Q_2 = Q_3 = Q_4$

2N2857

REV.	X-1	X-2	X3						
DATE	5-23-68	5-25-68	5-31-68						
EFF.	" "	" "	" "						
APP'D	[illegible]								

CIRCUIT LAYOUT & LIST REQUIREMENTS TO-8 HEADER

2-86 **I.C. FACILITY**

DR [illegible]	TITLE Limiter Ampl		
LAYOUT APPROVAL [illegible] 6/21 6/25/68			
PROBE REQ. APP.	PROJECT NO.	PRINT NO.	
SCALE 15:1	ORIG. ISSUE	DATE	PAGE

Figure 2-36 shows a plot of output level versus input level. In the linear region the amplifier has a voltage gain of 22 db. The limiting level is 710 mv rms.

Figure 2-37 shows a frequency response of the amplifier. The response is relatively flat from 2 to 100 MHz. The dc current drain from a -6 volt supply is 6 ma.

The limiter amplifier, as shown in figure 2-35, was used in the detector module prior to the loop phase detector and prior to the wideband detector. It was not used in the i-f amplifier, however, if the gain could be increased about 6 db this amplifier would be a logical choice for future AGC i-f amplifier models. The gain might be increased in this amplifier by using a higher frequency transistor. Also the low end frequency response could be rolled off by reducing the value of bypass capacitors C3 and C4. This feature makes the limiting amplifier seem more favorable than the feedback pair amplifier.

2.3.5 I-F Amplifier Module

This paragraph describes and discusses the completed i-f amplifier module, its layout, connection, shielding, and circuit configuration.

2.3.5.1 Layout and Construction

The objective in laying out the i-f was to put the entire circuit on a PC board that could someday be mounted to one side of the r-f head module. This requires that the PC board have a maximum outside dimension of 1.8 x 3.8 inches. The i-f consists of one filter, 4 AGC attenuators and 4 feedback pair amplifiers (as shown by the block diagram of figure 2-25. This means one tall T05 can (input filter) and eight T08 cans have to be mounted on this PC board. The layout is shown in figure 2-38. R-F shielding was added as shown in the figure. For convenience the PC board was mounted in a commercial-type chassis with BNC connectors for signal input and output. The AGC and -6 volt lines were brought out through the chassis on feedthru filters.

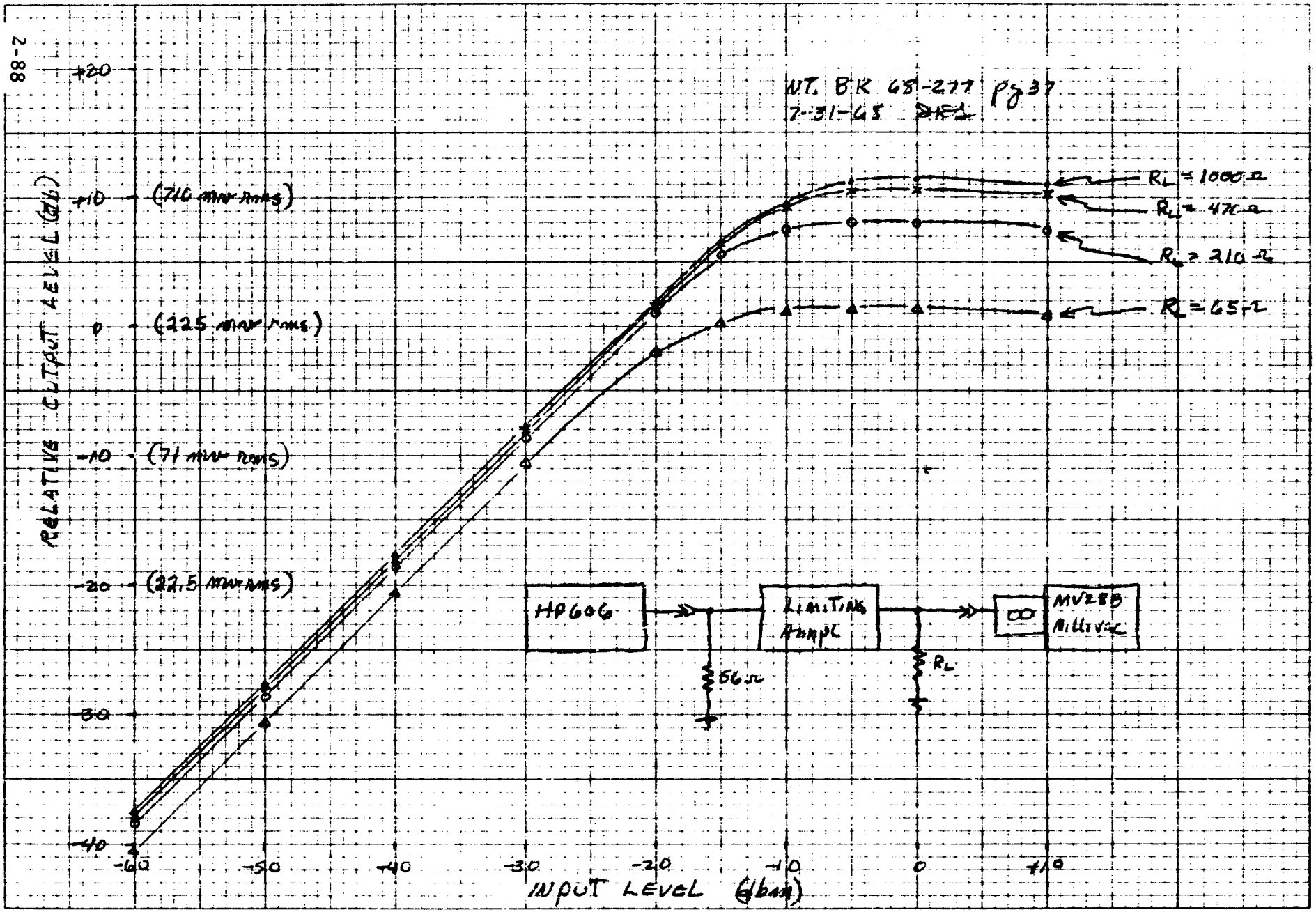


Figure 2-36. Limiting Amplifier Output Characteristic

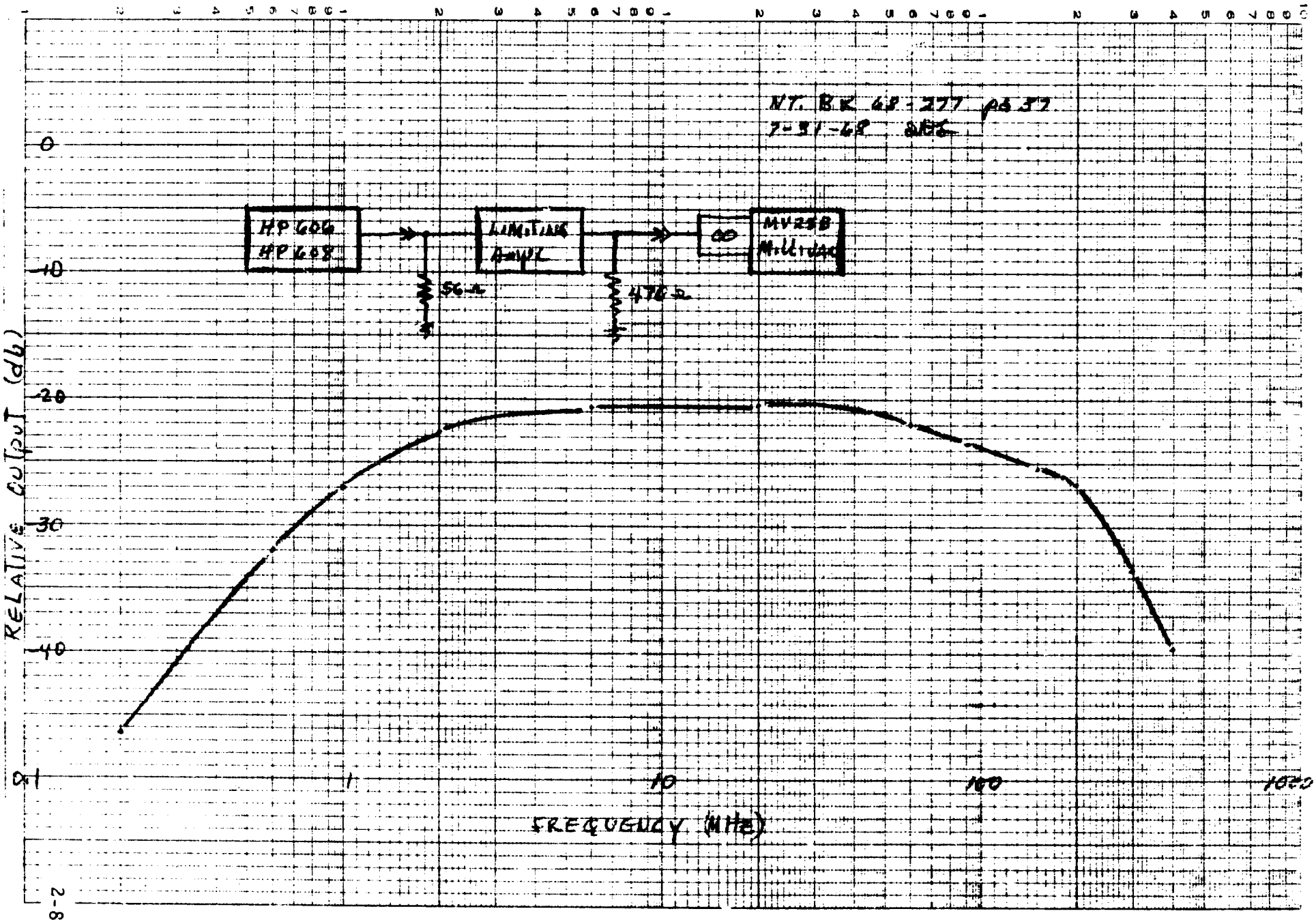


Figure 2-37. Limiting Amplifier Frequency Response

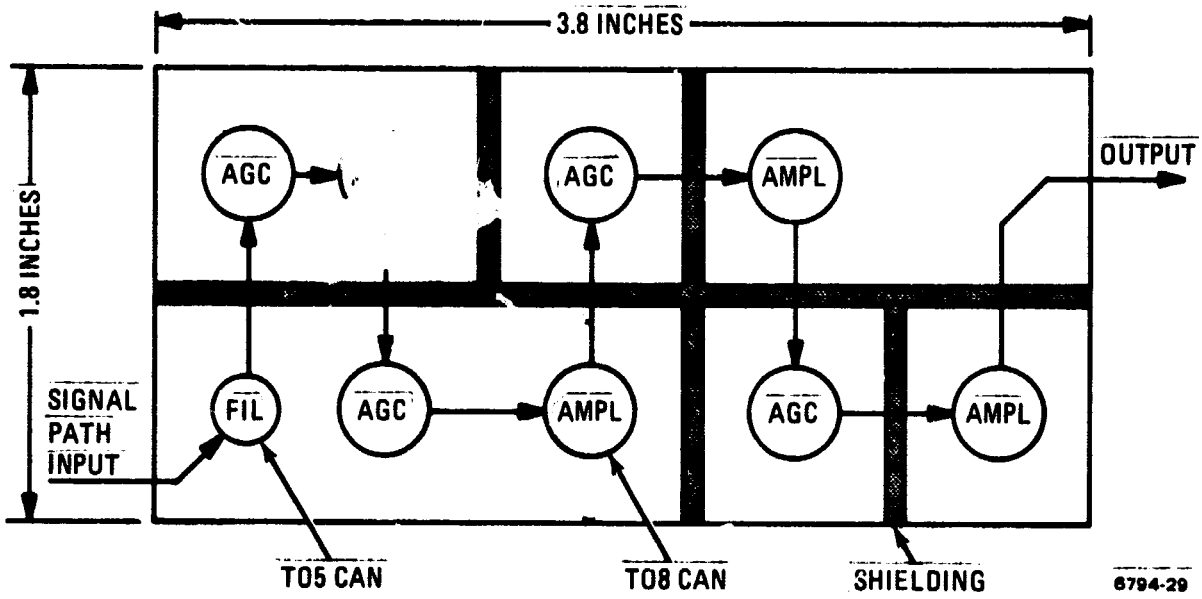


Figure 2-38. I-F Amplifier Layout

An attempt was made to operate the i-f amplifier (when it was first assembled) without any shielding between cans. At the time this did not appear to be practical since there was a problem with oscillations and shielding seemed to help. There is reason to believe that there is still some hope of operating the i-f without shielding. These reasons are as follows:

1. The T05 and T08 can lids were all attached to the headers with clips at the time the test was made. This does not seem to be a fair test since the clips prevent the cans from being pushed all the way down to the board. Also the can lids may not have been grounded well enough with the clip.

2. Another consideration is the fact that the reason the addition of the shields stopped the oscillations is that the shields may have provided desired ground current paths rather than shielding. This could be determined by making a careful study of the layout, considering ground current paths and by testing a layout with optimized ground current paths and no shielding.

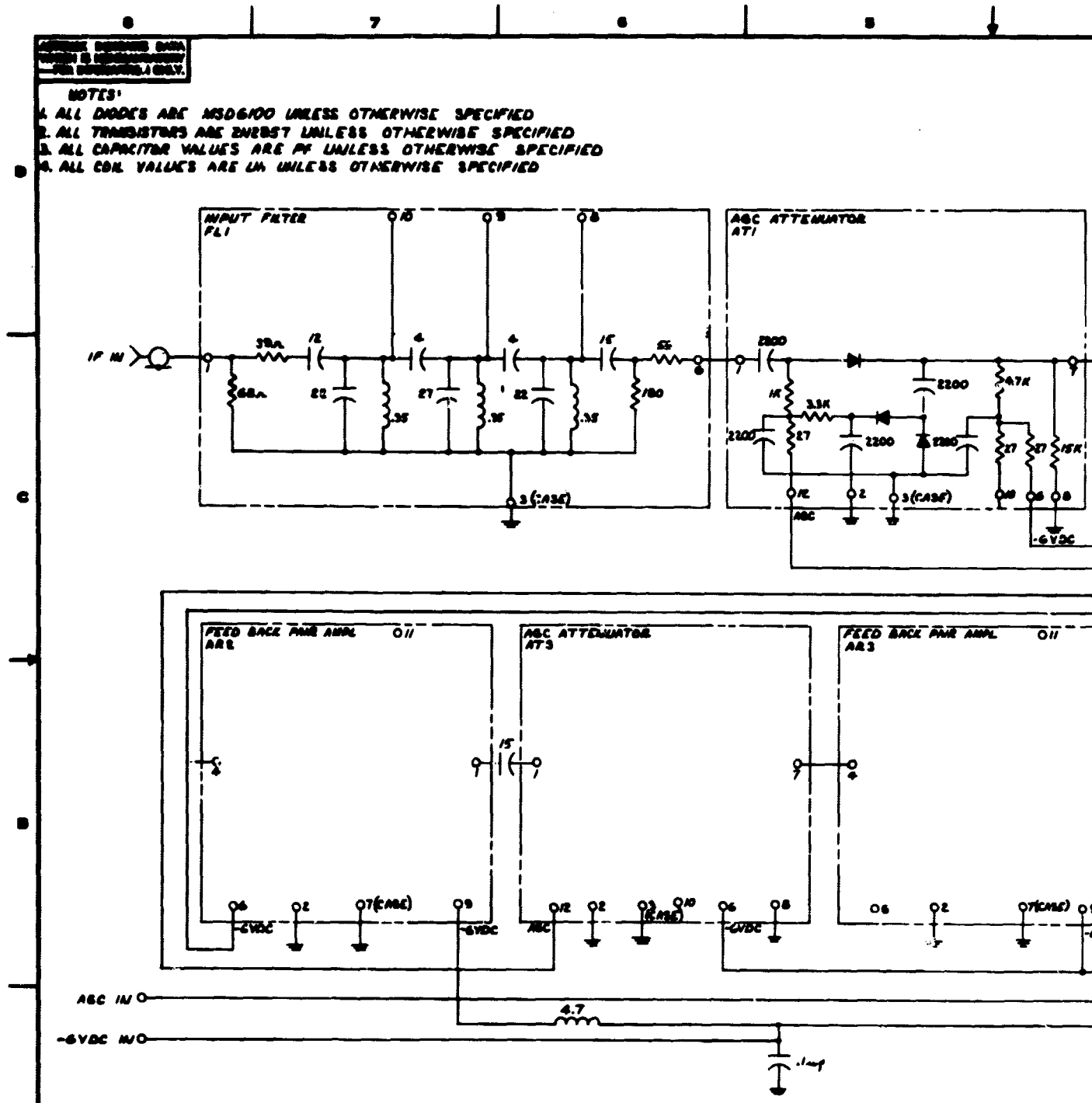
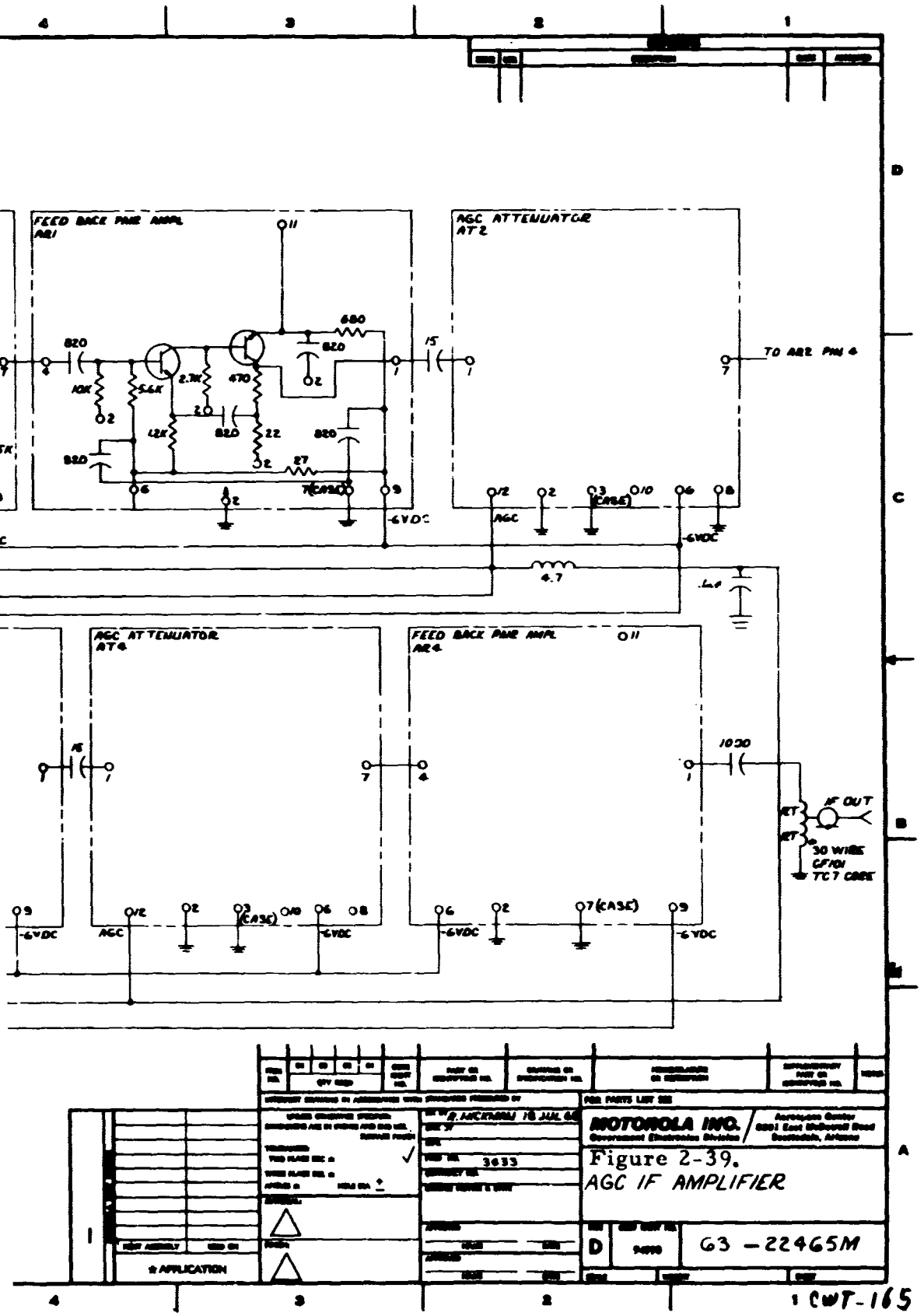


FIGURE 17

FOLDOUT FRAME 1



1 CWT-165

2-91, 2-92

There is a potential for considerable increases in part density on the i-f PC board. This can be illustrated as a size reduction of the board or as an increase in parts (and function) on the original size board. These two possibilities are described below.

1. By compressing the original layout configuration the board could be made 0.8 inch shorter and 0.6 inch narrower (making a 3.0 x 1.2 inch board). This is equivalent to a reduction in board area of 47%.

2. By using the original 3.8 x 1.8 inch board, and giving no consideration to possible printed circuit layout problems, there is room to mount nine more T08 cans on the board (making a total of 18 cans). This is an indication of the possibilities of adding more functions to this board.

2.3.5.2 Circuit Configuration

The schematic for the completed i-f amplifier is shown in figure 2-39. It was necessary to add some discrete components to make a complete working i-f amplifier. A tabulation of the total parts used is shown below.

Quantity	Part	Function
3	15 pf capacitors	Interstage coupling to roll off low end response.
1	1000 pf capacitor	Output dc block.
1	Transformer	Output impedance transformation.
2	.1 μf capacitor	Power line and AGC line filtering
2	4.7 μh indicator	
1	Input Filter	
4	AGC Attenuators	
4	Feedback Pair Ampl.	

18 Total Parts

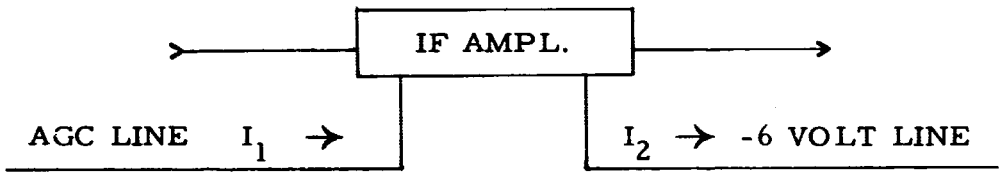
8 Different Parts

The three interstage coupling capacitors were added as a fix for the low frequency response problem on the feedback pair amplifier mentioned in paragraph 2.3.4.3. Paragraph 2.3.4.4 mentions the possibility of using limiter amplifiers in the i-f instead of feedback pairs. If this change were made it appears that the three interstage coupling capacitors would not be needed since the low end response could be controlled in the limiter amplifiers.

2.3.5.3 Data

The data presented in the following paragraphs was taken on the completed i-f amplifier.

2.3.5.3.1 Dc Current Drain. The dc current drain from the -6V supply and the AGC line is shown below for various values of AGC voltage.



AGC (Volts)	I_1 (ma)	I_2 (ma)
+1.0	+4.2	
0	+3.3	23.7
-1.0	+2.3	22.9
-2.0	+0.5	22.2
-3.0	-1.4	21.6
-4.0	-3.4	21.1
-5.0	-4.8	
-6.0	-6.0	

The total power consumption is about 130 mw.

2.3.5.3.2 AGC Characteristic. The AGC characteristic is shown in figure 2-40. The slope of this curve is relatively constant at 24 db/volt from -0.5 to -3.5 volts. From -3.5 to -4.0 volts the curve starts to flatten out since the diode attenuators are past the linear region.

2.3.5.3.3 Linearity. Figure 2-41 shows the linear range of operation as a function of AGC voltage. There are two important points illustrated here.

1. The amplifier is linear at an output level of -40 dbm in all cases (-40 dbm is the AGC's operating level).

2. With full gain (OV AGC) the limiting level of the amplifier is +2 dbm.

2.3.5.3.4 Frequency Response. Figure 2-42 shows the amplifier frequency response for four values of AGC. The amplifier frequency response is essentially the response of the input filter. The important point here is the fact that the bandpass does not shift with AGC. The bandpass does show a little ripple in the OV AGC case. This is due to the input impedance of the AGC attenuator in the minimum attenuation case.

2.3.5.3.5 Noise Figure and Output Noise Power. The output noise power of the if. amplifier with full gain (OV AGC) was measured under two conditions, as shown below.

	Input Terminated in 50 ohms	Input Connected to r-f Converter
RMS Noise Power	-7.5 dbm	-3.5 dbm

This data points out two important facts.

1. The total output noise power with the r-f converter connected is only 5.5 db below the limiting level of the output amplifier. This will result in approximately 0.6 db signal suppression. This is not a problem, however, it does point out that if more i-f gain were desired, the linear range of the output amplifier would have to be extended assuming the noise bandwidth and front end noise figure were kept the same.

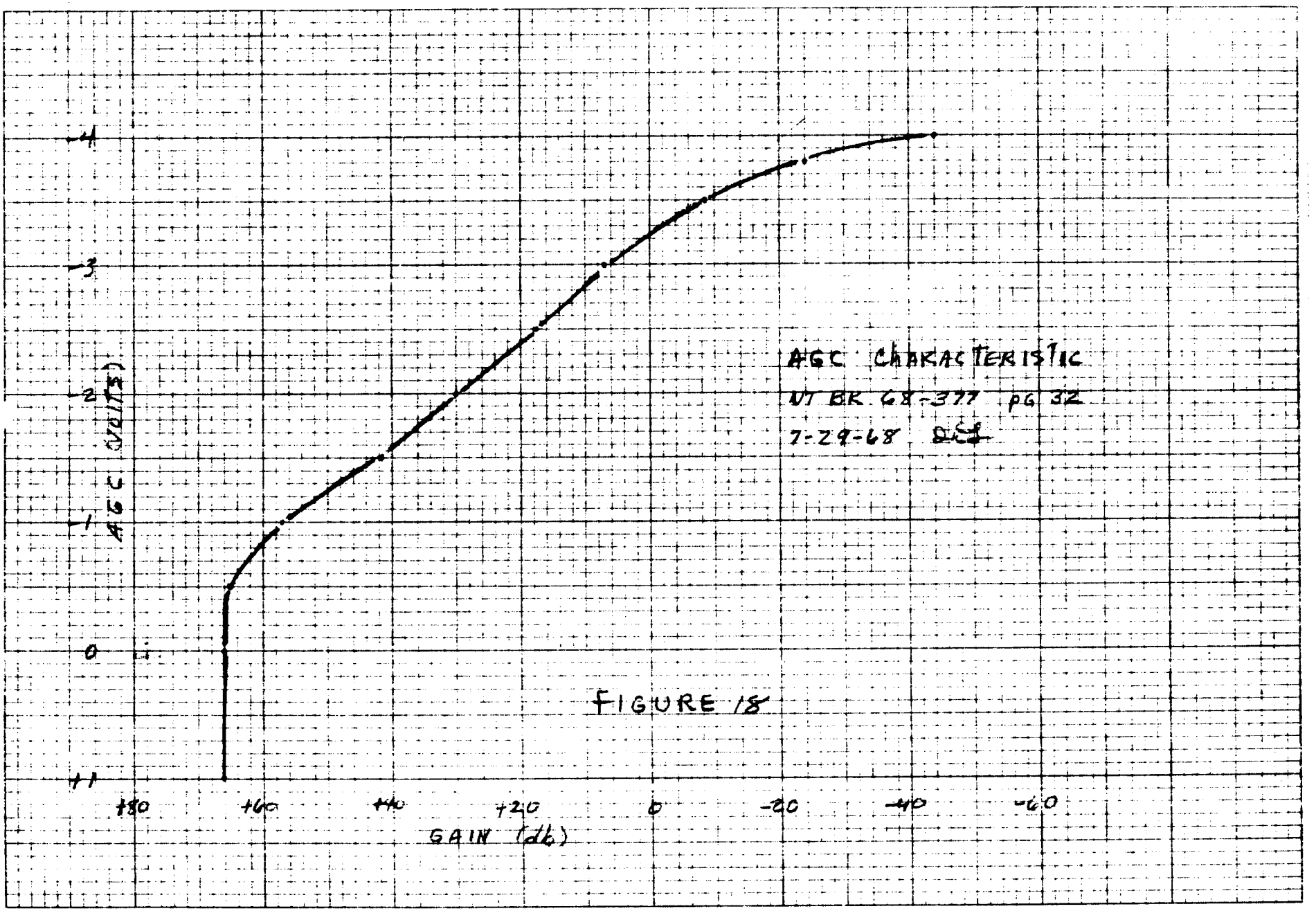


Figure 2-40. I-F Amplifier AGC Characteristic

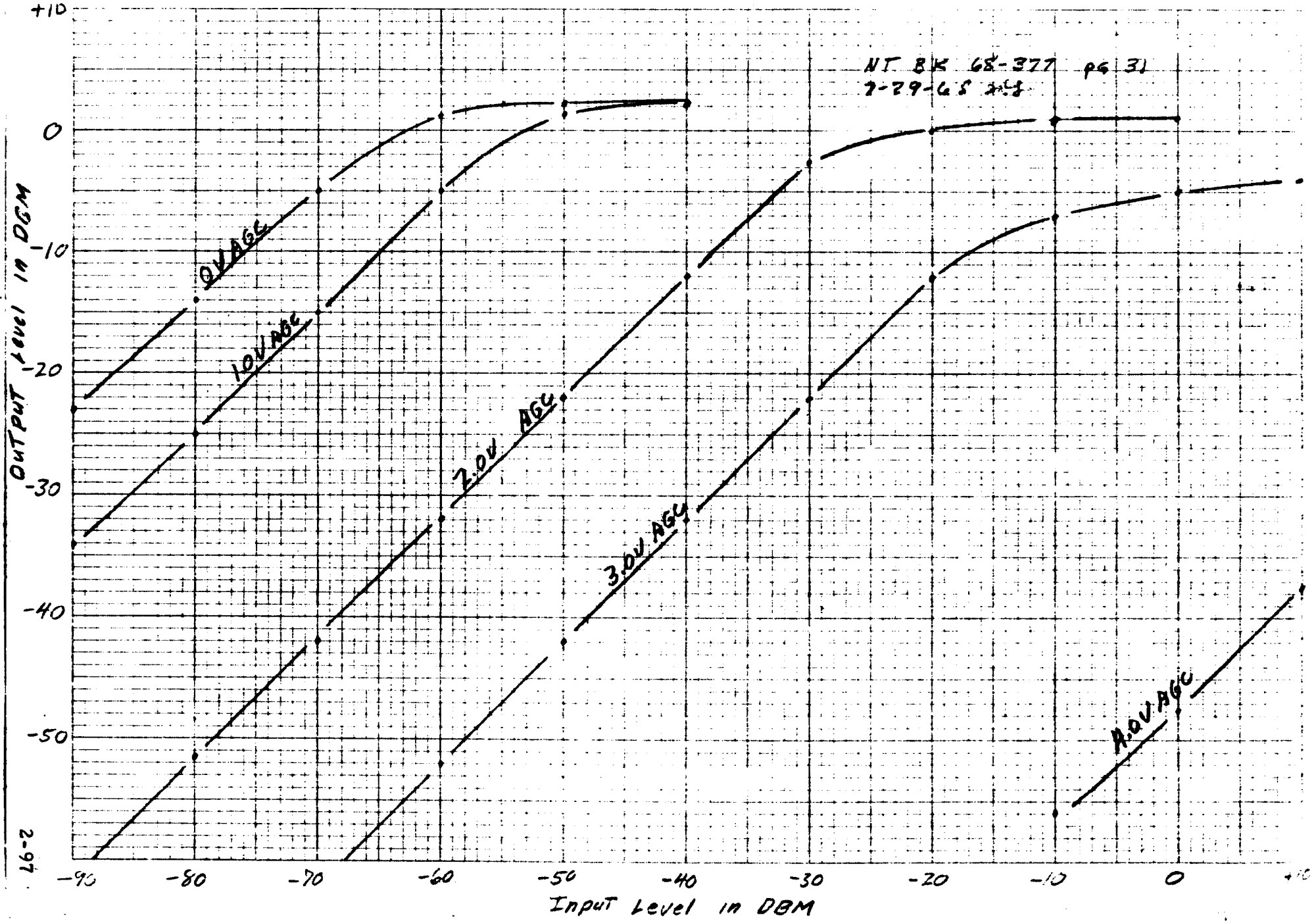


Figure 2-41. I-F Amplifier Linearity

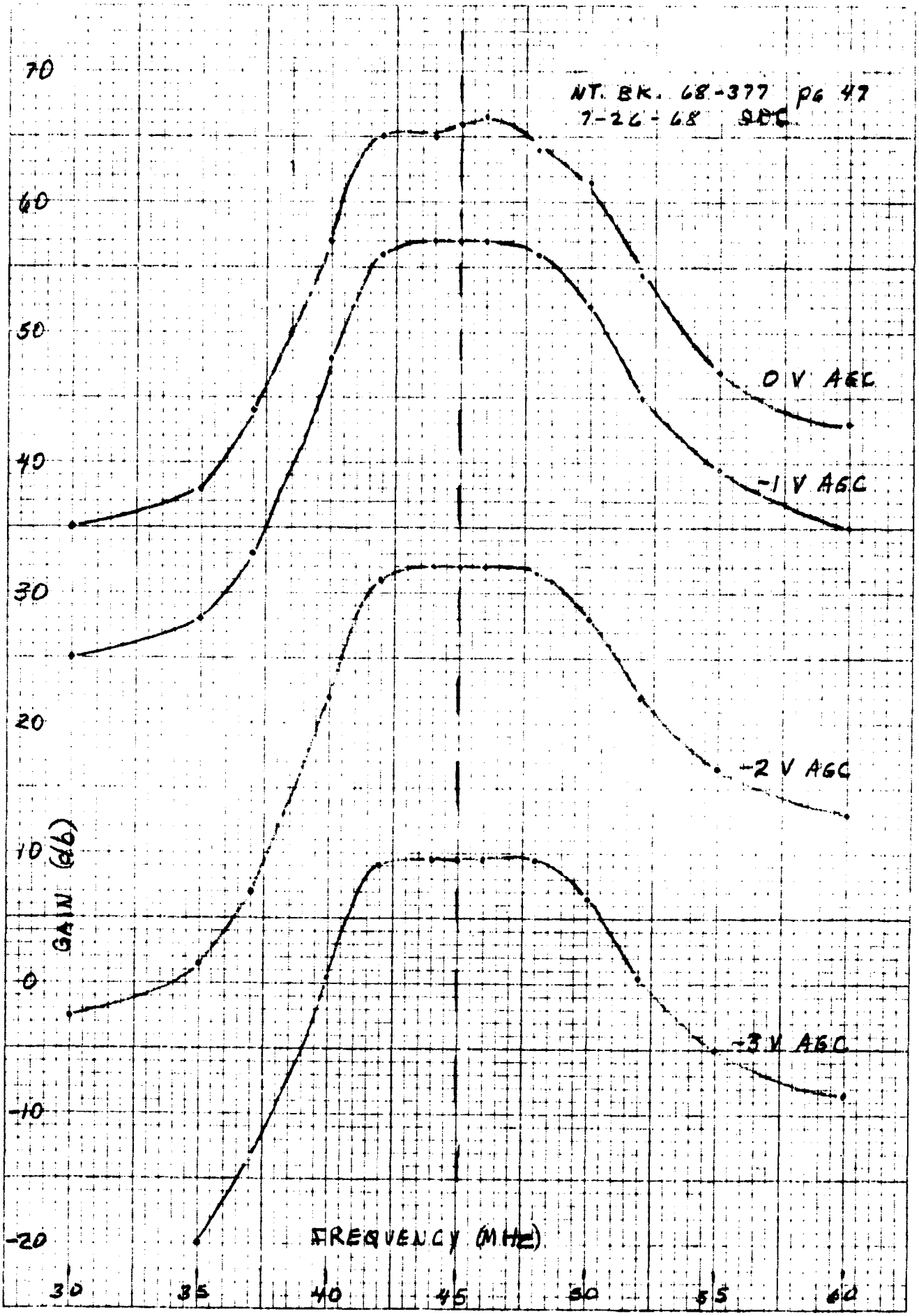
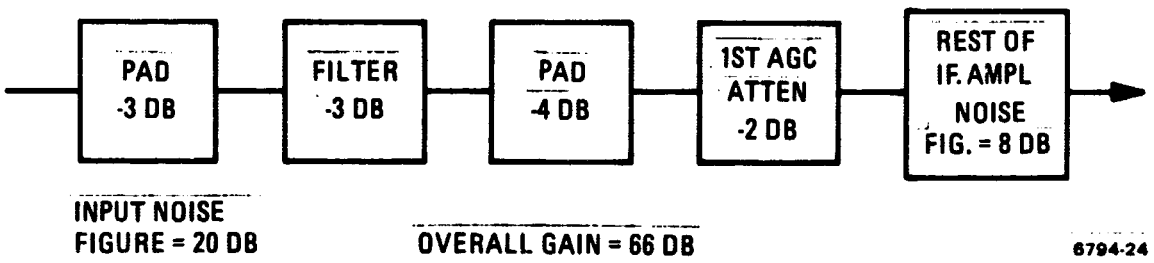


Figure 2-42. I-F Amplifier Frequency Response

2. The noise power of the i-f amplifier alone is almost as great (4 db lower) as the total noise power when connected to the r-f converter. This indicates that the noise figure of the i-f amplifier front end is high and/or the noise contribution of the wideband amplifier stages (after the input filter) is significant. It turns out that both are true.

The condition described above did not degrade the performance of the i-f amplifier (for the gain it has) or the performance of the receiver; however, if a more sensitive receiver were built, more gain would be required in the i-f amplifier and this condition would be a problem. The following paragraphs describe this problem in more detail.

2.3.5.3.5.1 Noise Figure Detail Explanation. The block diagram below illustrates how the input noise figure of the i-f amplifier accumulates to 20 db due to the losses through the input filter, isolation pads and first AGC attenuator. Since the input



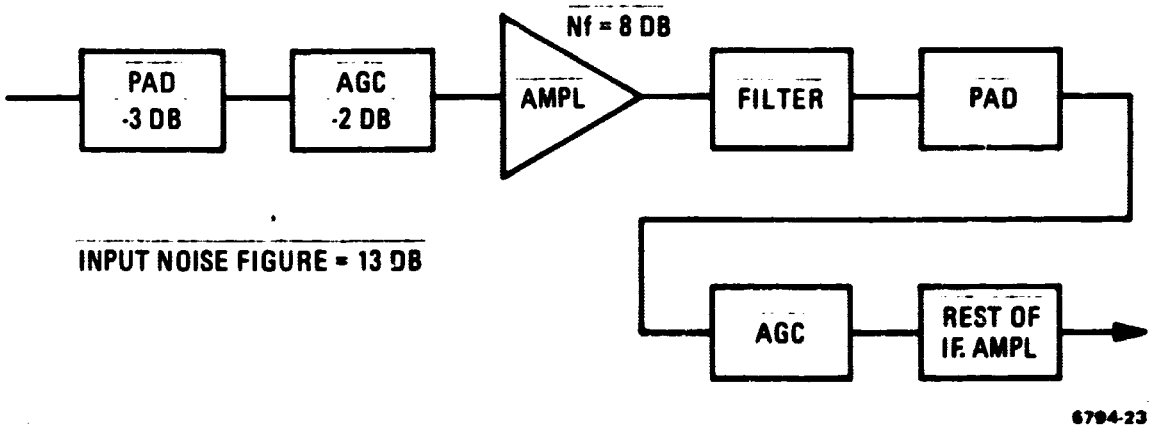
filter is ahead of all of the i-f gain it only band limits the noise coming in from the r-f converter. All of the gain after the input filter is broadband (about 120 MHz equivalent noise bandwidth). The calculations below verify the measured i-f noise power.

Noise Figure	20 db
Gain	66 db
Bandwidth Ratio	81 db ($10 \log 1.2 \times 10^8$)
	167 db

-174 dbm + 167 db = -7 dbm noise power

From the above illustration one might readily conclude that the input filter and first AGC attenuator should be moved "downstream" in the i-f amplifier so that the first amplifier stage is right at the input, thus reducing the input noise figure to 8 db. This would solve the noise figure problem; however, it might generate a new problem unless the input amplifier was a special type with increased linear range. The new problem is the fact that there is no gain control in the receiver ahead of this amplifier and under strong signal conditions (-40 dbm at the receiver input) this amplifier would see an input level of -10 dbm. This level would drive the feedback pair amplifier used in this i-f well into limiting.

Now, let us consider the compromise of moving the filter "downstream" but leaving the AGC attenuator at the input. This would put some gain control before the first amplifier stage, thus eliminating the linearity problem. The noise figure would be 10 db which is still a large improvement over 20 db. It is still not this simple however, because the input impedance of the AGC attenuator varies widely and must be isolated from its source (the mixer in the r-f converter) by a 3 db pad. This would increase the i-f input noise figure to 13 db. The filter could then be inserted between the first amplifier stage and the AGC attenuator that follows it if the filter and AGC are isolated by a 3 db pad. This approach appears to be an improvement that would not require adding any new parts, but just redistributing the existing ones. This configuration is illustrated below.



2.3.6. Conclusions and Recommendations

The results of this effort have been quite encouraging with respect to applying chip and wire techniques to miniaturization of linear r-f circuits. The goal of making each integrated circuit complete in itself (requiring no external components) proved to be readily attainable, however, for the active circuits it required packaging the IC in a T08 can instead of a smaller T05 can. This is true because the ceramic capacitors used for coupling and bypassing are quite large (50 mils x 95 mils) in terms of integrated circuit components. These capacitors can be seen on the integrated circuit layouts of figures 2-29, 2-32, and 2-35. An obvious question at this point might be: "Is it more practical to use larger T08 cans with all of the components inside, or smaller T05 cans and some of the components outside?". The answer depends on the application. In the case of the i-f amplifier where much gain is envolved and dense packaging was the goal it seems more practical to use the larger T08 can with all of the components inside.

The i-f amplifier met all of the design goals described in paragraph 2.3.2 except the maximum gain. The maximum gain design goal was 76 db, however, the completed i-f amplifier measured 66 db. The reasons the completed i-f had 10 db less gain than intended are; (1) the AGC attenuators have more loss at 0 V AGC than anticipated, (2) adding the 15 pf capacitors between stages to roll off the low end response caused some loss of gain at 45 MHz. In the receiver the lower value of maximum gain was not a problem because the noise bandwidth of the receiver was set to give a front end threshold sensitivity of -130 dbm instead of -140 dbm.

2.3.6.1 Recommendations

After reviewing the results of this effort, there appears to be several areas in which further investigation would be appropriate if funds were available. These areas are listed briefly below.

1. Investigate optimizing layout of the i-f amplifier with respect to ground current paths to try to eliminate shielding (paragraph 2.3.5.1).

2. Investigate increasing the part density by decreasing the size of the i-f pc board or adding some other functions to the present board (paragraph 2.3.5.1).

3. Design future models with higher maximum gain and with input filter moved "downstream" in the i-f (paragraphs 2.3.5.3.5 and 2.3.5.3.5.1).

4. Investigate the need of extending the linear range of the output amplifier if the total maximum gain is increased (paragraph 2.3.5.3.5).

5. Check out feasibility of increasing gain and decreasing bandwidth of limiter amplifier. Then try using it to replace the feedback pairs in the i-f amplifiers (paragraph 2.3.4.4).

6. Investigate more efficient AGC attenuator circuit (paragraph 2.3.6).

2.4 PREDETECTION I-F AMPLIFIER

2.4.1 Introduction

The Predetection i-f amplifier (PDIF) was originally designed to be part of the detector and packaged in the same module. It later was decided to separate the PDIF from the detector because: (1) more isolation was needed between the i-f amplifiers and the reference oscillator, and (2) there was not enough room in the detector for the PDIF. This subsection describes the PDIF after it was built as a separate module.

2.4.2 Function

The function of the PDIF is to provide the i-f gain required by the receiver from the point where the channels split, to each of the three detectors. A block diagram of the PDIF is shown in figure 2-43.

2.4.3 Description

The crystal filter in the narrowband channel has one pole and a 3 db bandwidth of 10 kHz. The phase detector channel must have enough gain to drive the last limiter stage well into limiting with an input level of -40 dbm. The gain in the

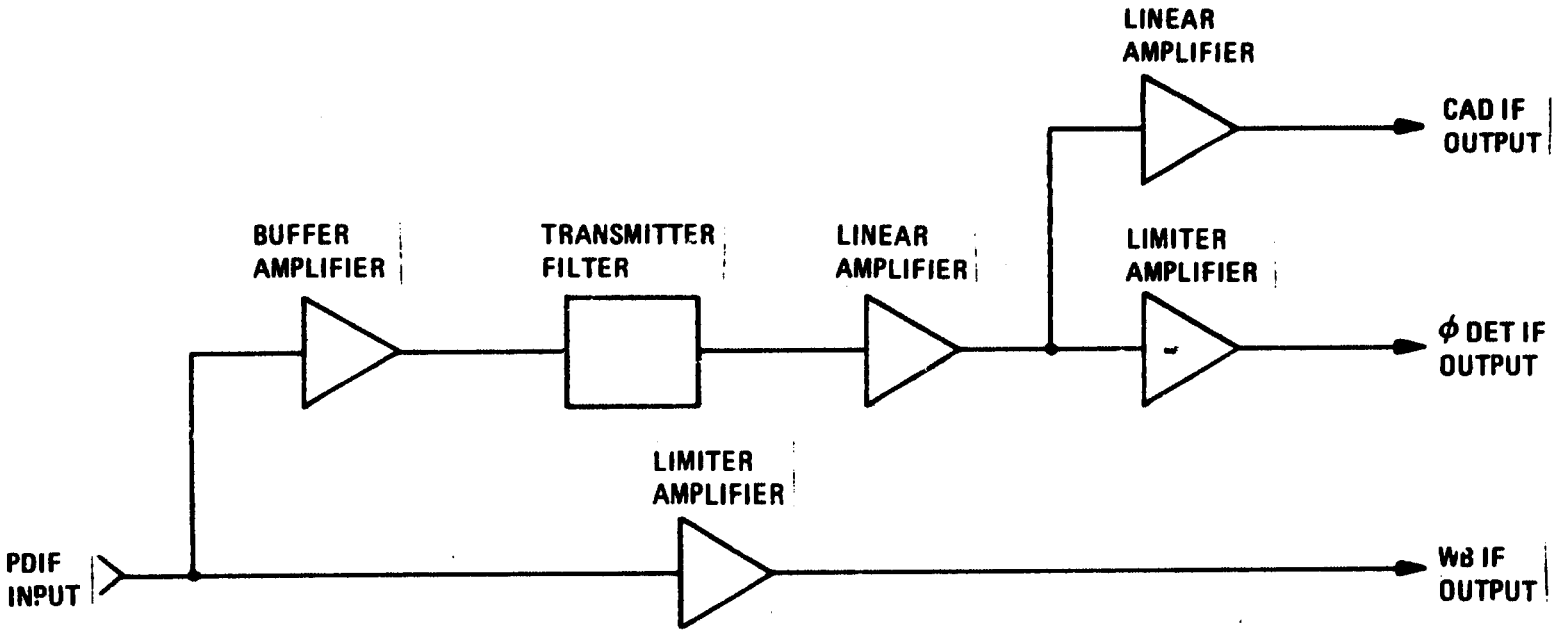


Figure 2-43. PDIF Block Diagram

CAD channel must be linear for an input level of -20 dbm. The wideband channel must have enough gain to drive the last limiter stage well into limiting with an input level of -40 dbm. Figure 2-44 shows a breakdown of gain, bandwidth and noise power at various points through the PDIF.

A schematic of the PDIF is shown in figure 2-45. A discussion of the feedback pair amplifier and the limiter amplifier is presented in paragraphs 2.3.4.3 and 2.3.4.4 of this report. A design discussion of the crystal filter is given in paragraph 2.4.6.

2.4.4 Mechanical Configuration

The components for the PDIF were mounted on a 1.8 x 3.8 inch printed circuit board and the board was mounted in a 2 x 4 inch Apollo Block II type frame. A sketch of the layout is shown in figure 2-46.

2.4.5 Test Data

Figure 2-47 shows the limiting characteristics of the WB, CAD and phase detector channels. These curves show that the CAD channel is about 27 db below the limiting level with an input level of -40 dbm. The WB and phase detector channels are about 5 db in limiting with an input level of -40 dbm. This is marginally adequate. It would be desirable to have 5 db more limiting in each of these channels.

Figures 2-48 and 2-49 show the phase shift of the wideband i-f output and CAD i-f output with respect to the phase detector i-f output as a function of input signal level. These curves show that the phase shift does not change drastically until the input signal level goes above -15 dbm.

Figure 2-50 shows the frequency response of the wideband channel. This channel has a 3 db bandwidth of about 30 MHz.

Figure 2-51 shows the phase and amplitude response of the narrowband channel as a function of frequency over a 200 kHz range around center frequency. One phase response is shown at an input level of -40 dbm, and one is shown at an input level

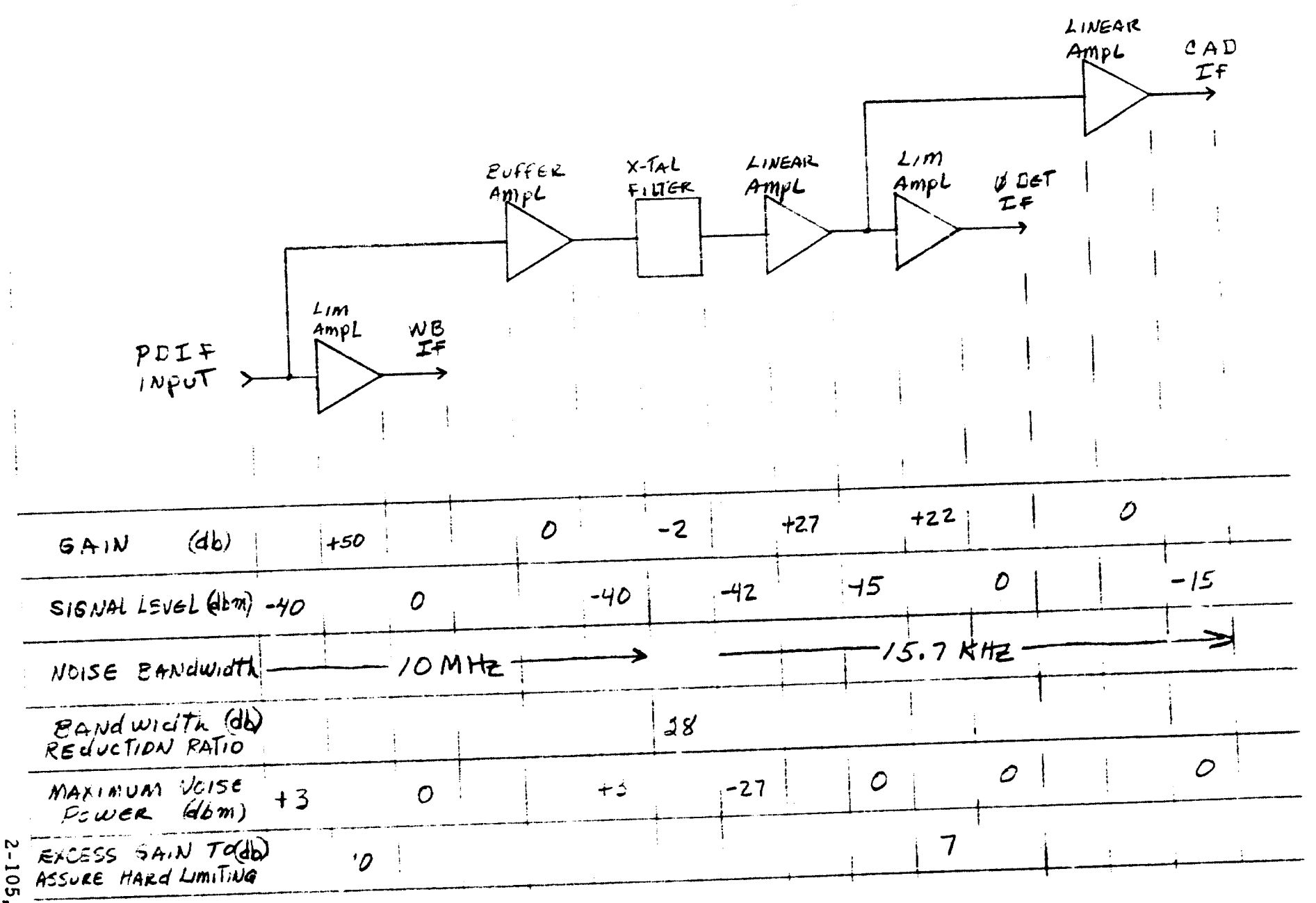
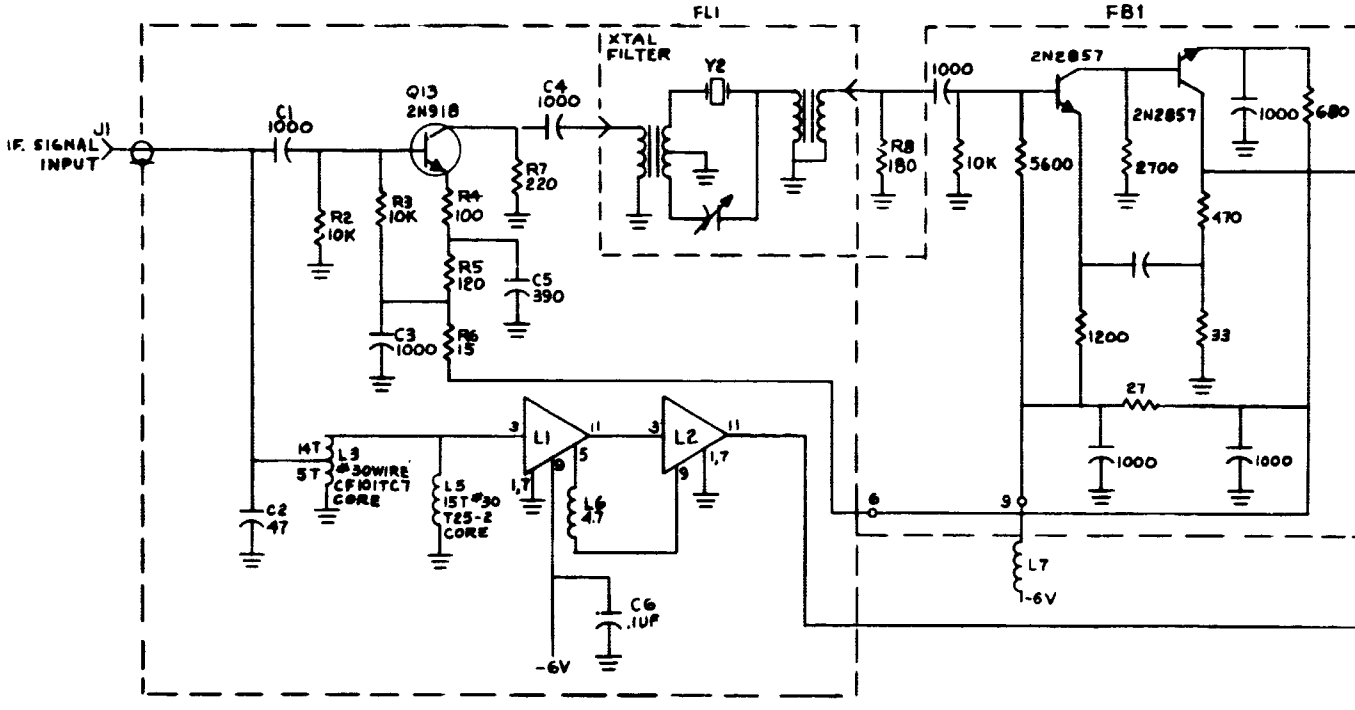


Figure 2-44. Predetection I-F Amplifier

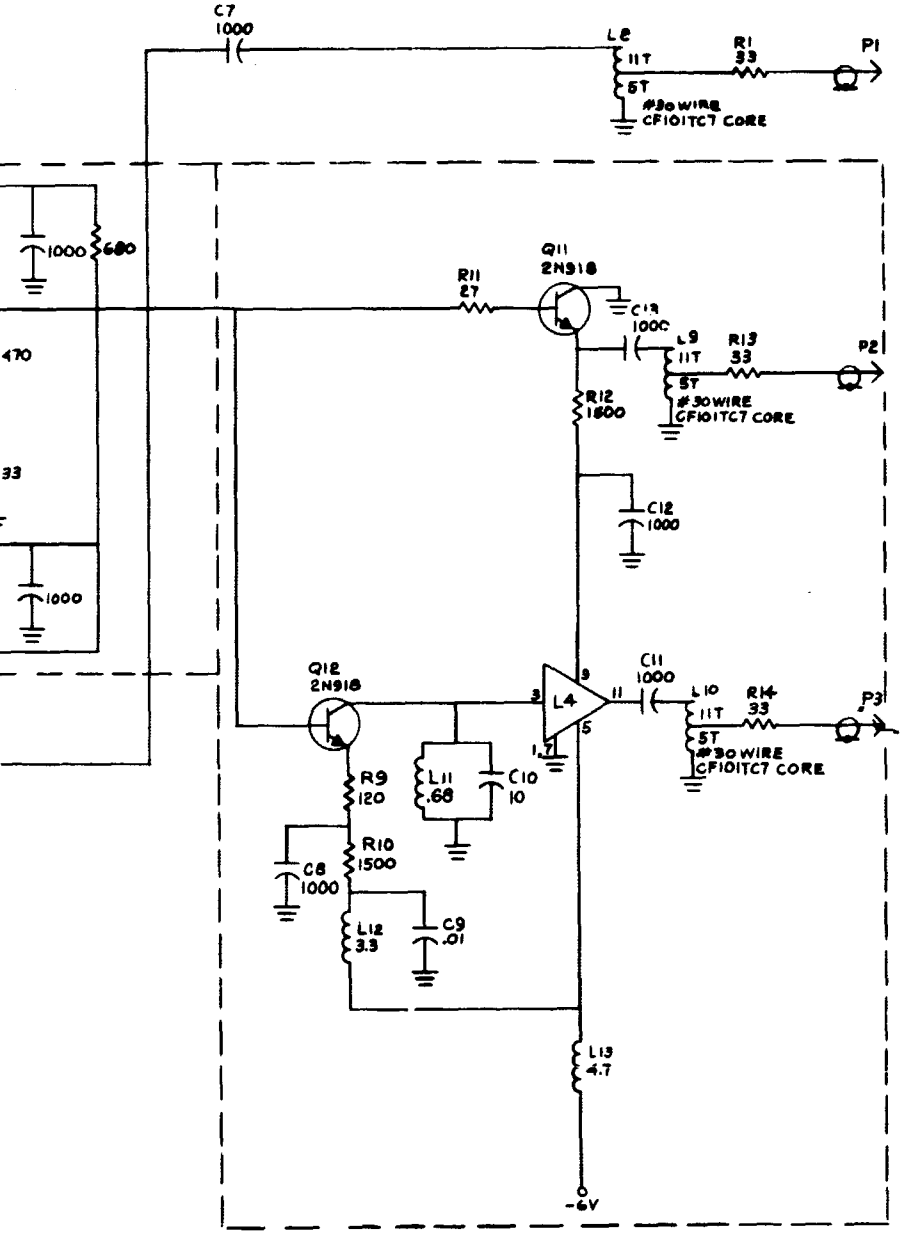
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS.
   ALL CAPACITORS ARE IN MMF.
   ALL INDUCTORS ARE IN UH.

▽ COMMON SIGNAL, CONNECT TOGETHER.



FOLDOUT FRAME 1



LAST USED	NOT USED
C74	
CR12	
J7	
L40	
P3	
Q19	
R76	
T6	
Y2	

Figure 2-45. Pre-Detection I-F Amplifier, Schematic Diagram

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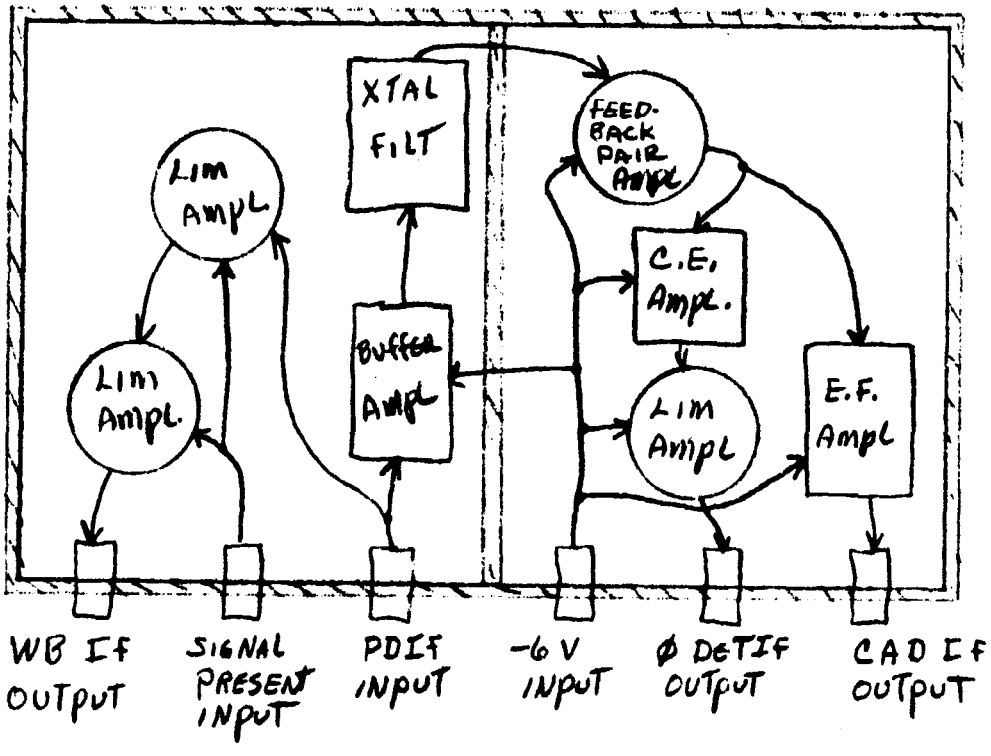


Figure 2-46. PDIF Layout

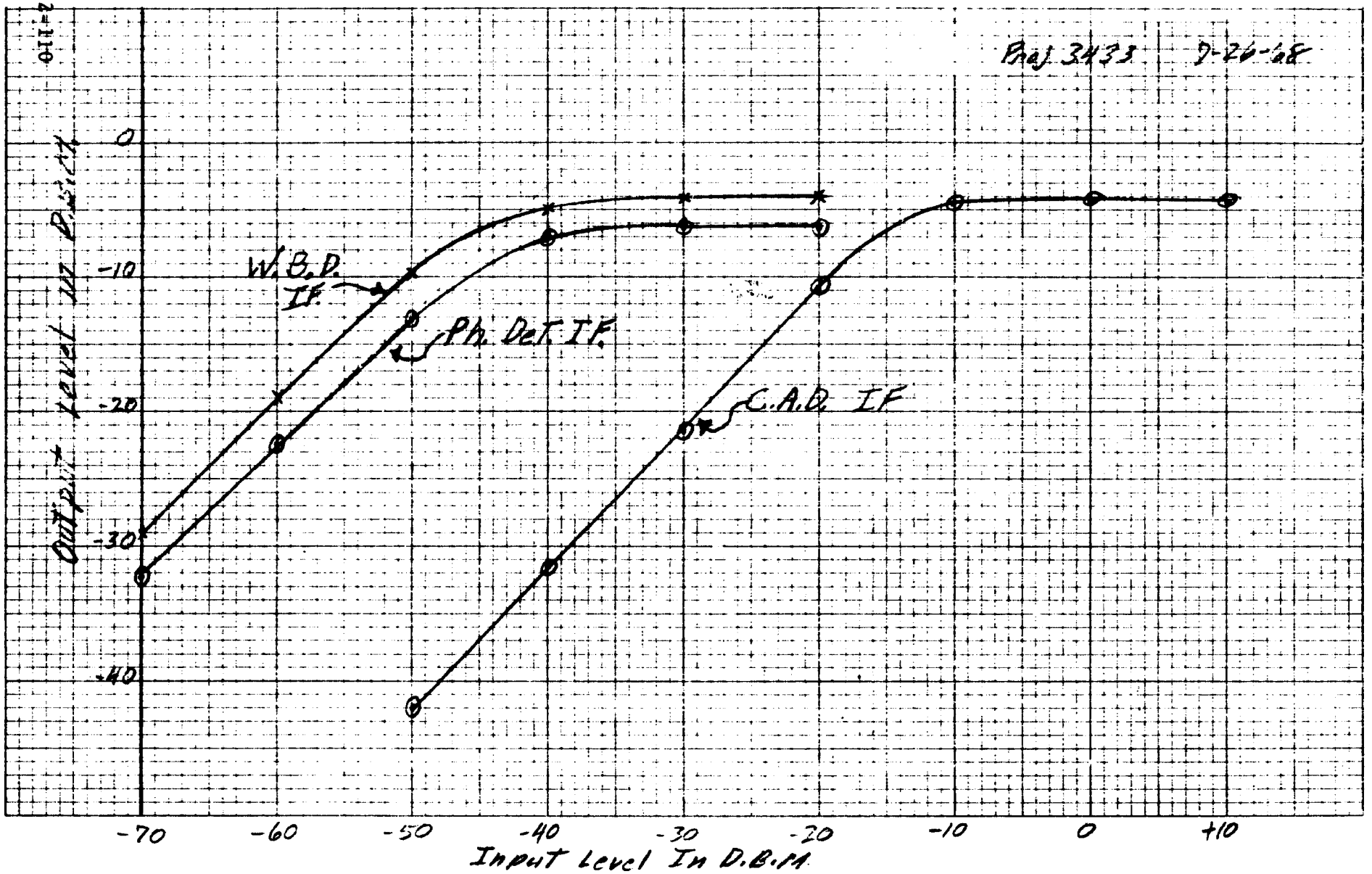


Figure 2-47. Limiting Characteristics of Predetection I-F Amplifier

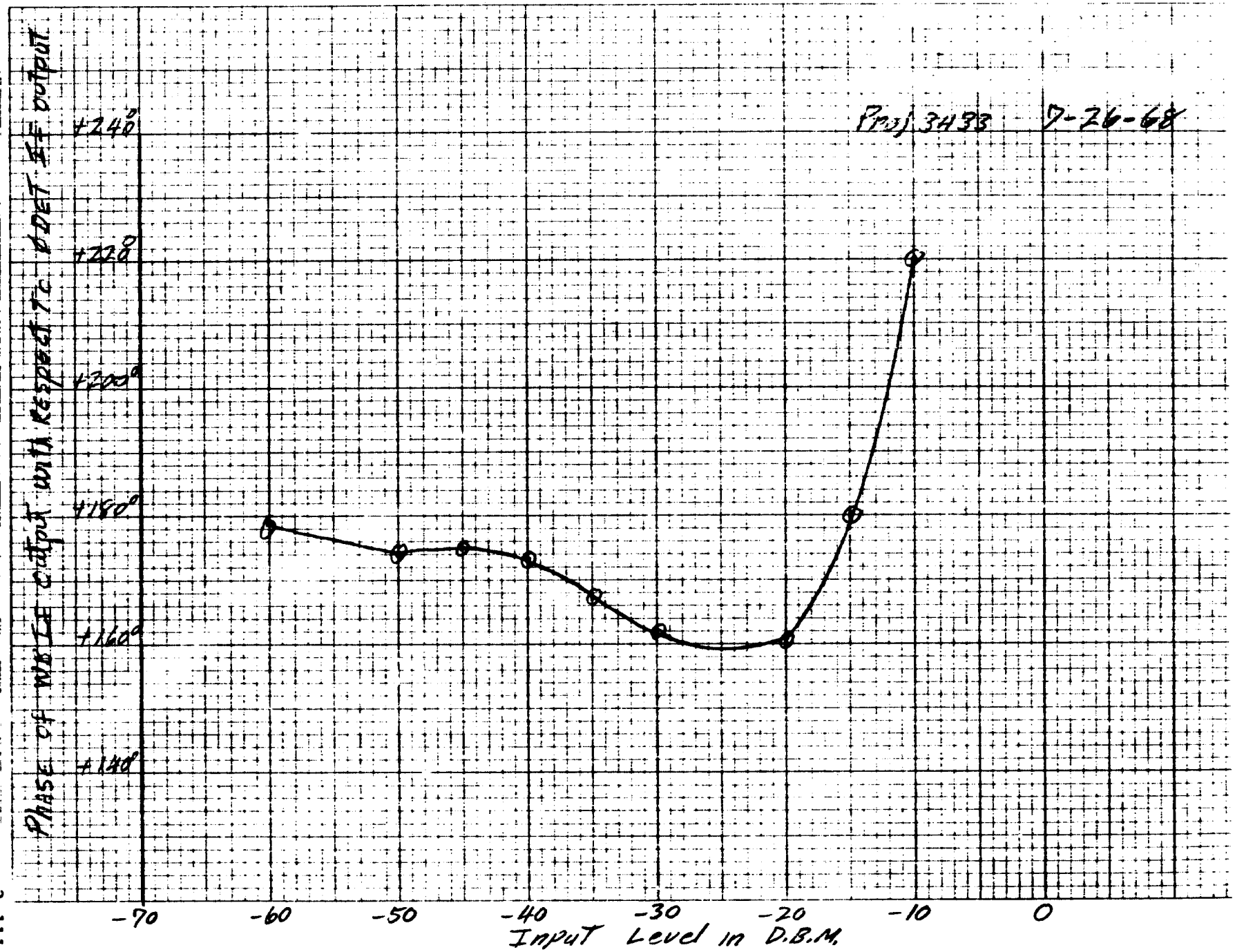


Figure 2-48. Phase Shift Vs Sig Level for WBD I-F

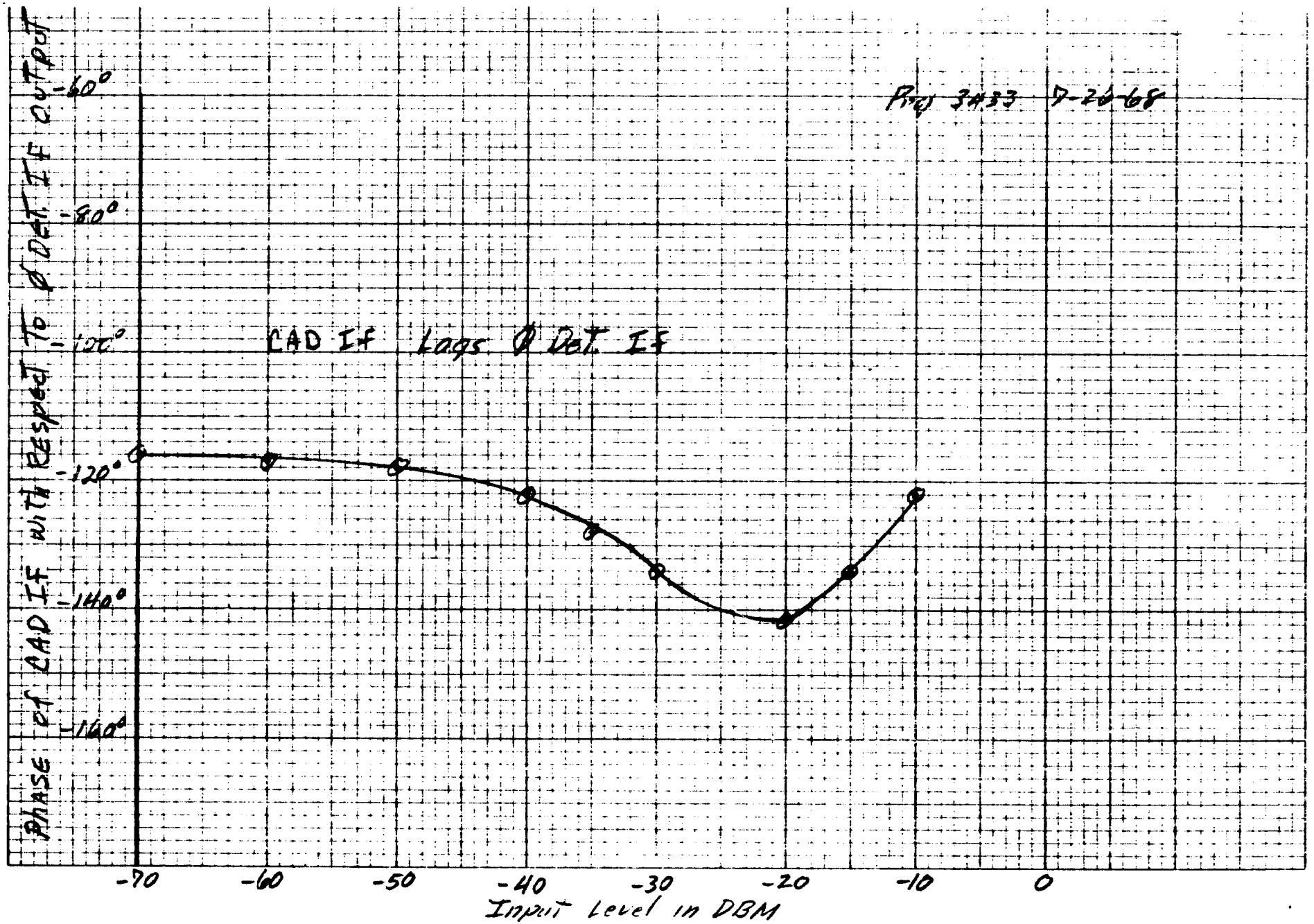


Figure 2-49. Phase Shift Vs Sig Level for CAD I-F

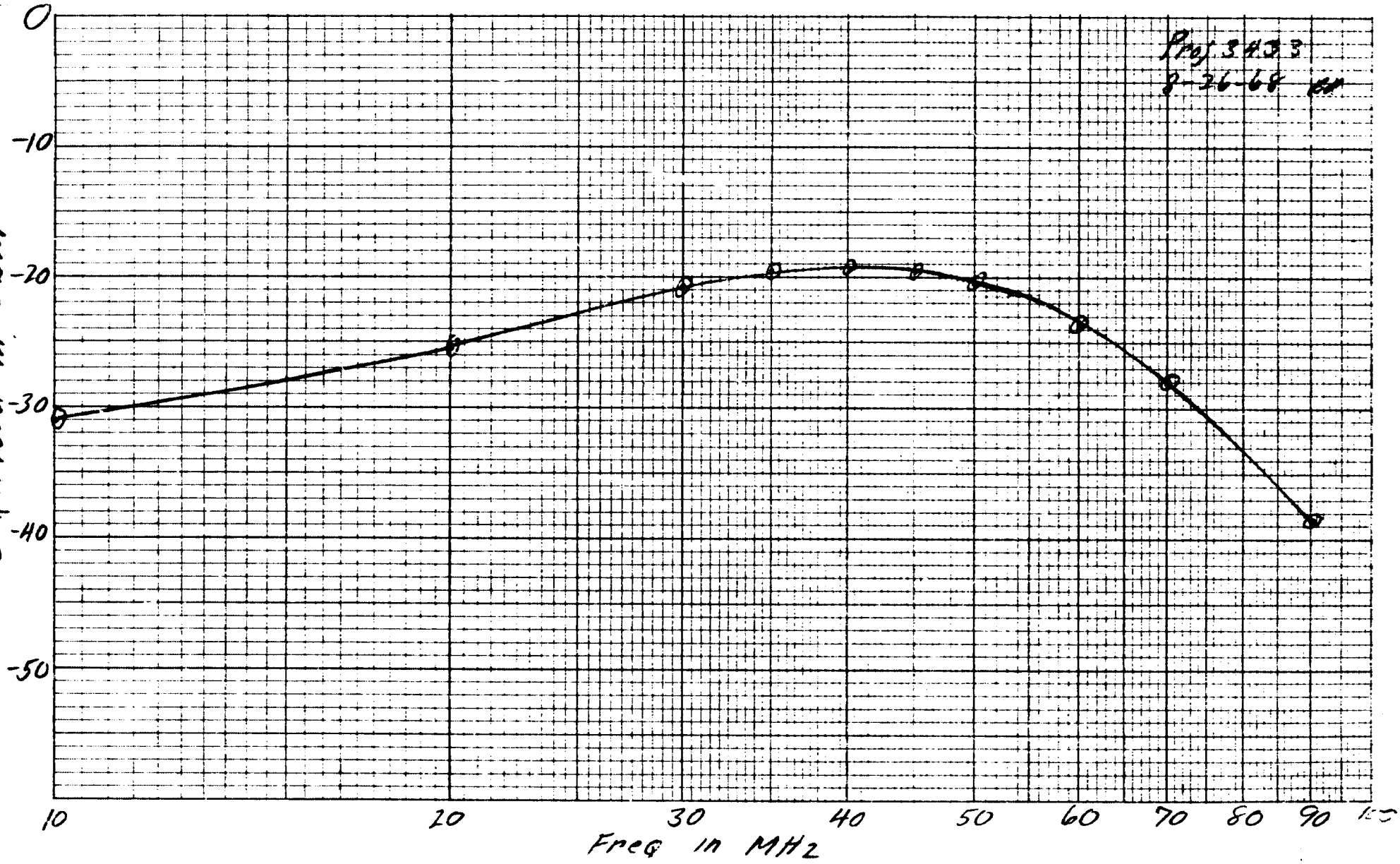


Figure 2-50. Frequency Response of WBD I-F Amplifier

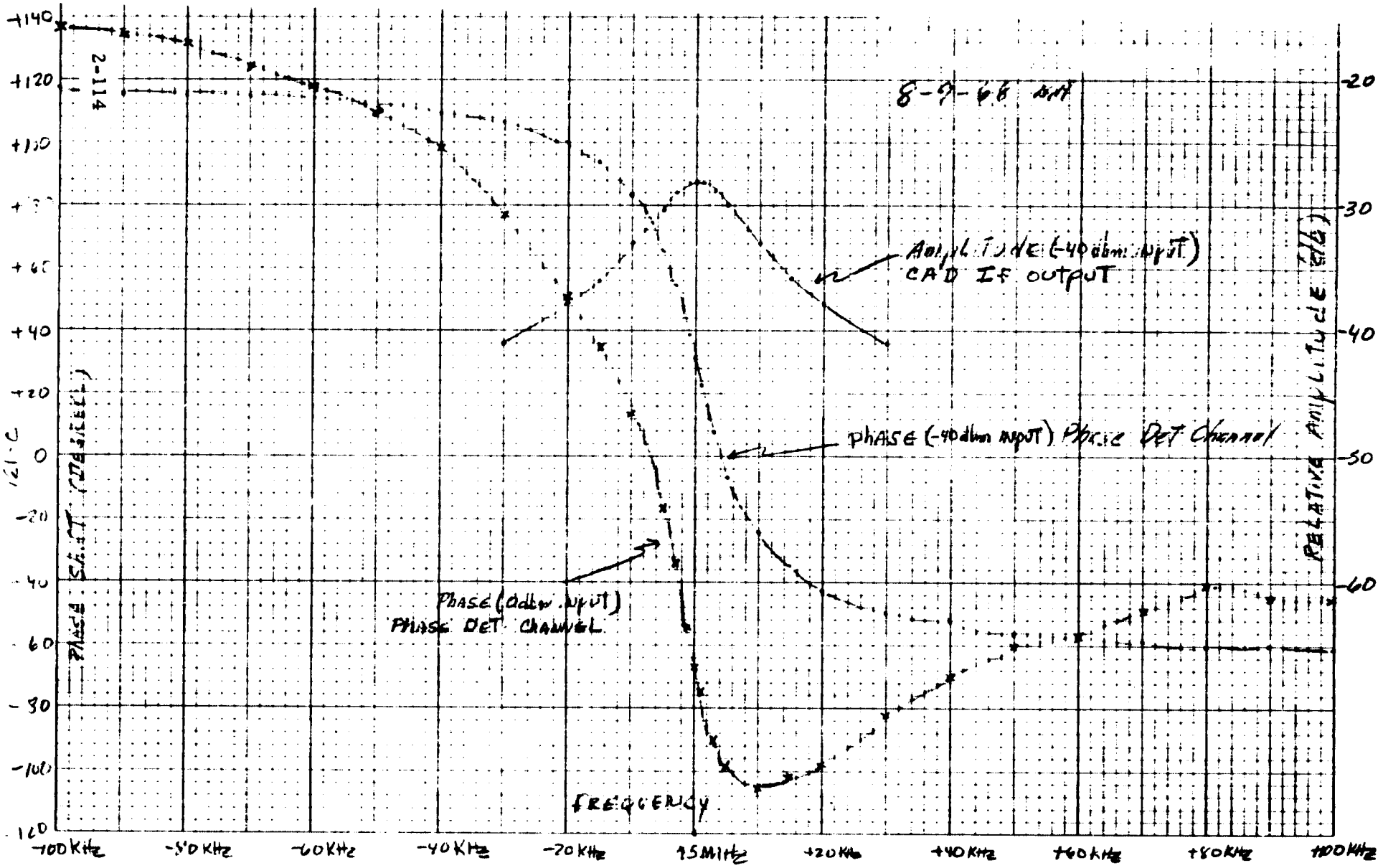


Figure 2-51. Phase and Amplitude Response of Predetection I-F Amplifier Phase Det Channel

of 0 dbm. The significance of the curve at 0 dbm is that it shows the effect of limiting in the feedback pair amplifier following the crystal filter, which occurs at strong input signal levels. This condition occurs in the receiver during acquisition before phase lock and before the AGC has returned the PDIF input level to -40 dbm. The effect on acquisition is discussed in the Transponder Test Data section. Corrective action for this problem would be to replace the feedback pair amplifier (following the crystal filter) with a limiter amplifier. Since this is a lower gain amplifier, the gain distribution would have to be reconsidered also.

2.4.6 Predetection Narrow Bandpass Filter

Receiver design considerations show the need for a small percentage bandpass filter at the i-f frequency. This predetection filter increases the signal-to-noise ratio sufficiently to allow phase detection at low input signal levels.

Phase lock loop design dictates the need for a single pole, high Q filter, with stringent phase characteristics. The only practical circuit suitable is a quartz crystal filter. The design requirements, considerations, and conclusions for such a filter are included in this report.

2.4.6.1 Filter Requirements

The major purpose in designing a new crystal filter is to achieve a small physical size compatible with receiver miniaturization. The electrical design goals set forth are:

Center Frequency	45000. $\pm$1 kHz
3 db bandwidth	10 $\pm$1 kHz
30 db points	$\pm$350 kHz max.
50 db points	$\pm$2.0 to 3.0 MHz
30 db symmetry	$\pm$50 kHz max.

Furthermore the spurious responses of the filter must be minimized. These spurs are purely a crystal characteristic and are included in the crystal item requirement specification. This IRS is given in paragraph 2.4.6.5.

2.4.6.2 Filter Design

In designing this filter, Technical Memorandum 3330/3.17 was referred to. This report covers work done on the SGLS 770 crystal filter and includes some helpful suggestions on tuning interactions.

2.4.6.2.1 Circuit Configuration. Figure 2-52 shows the conventional filter circuit being used. However, it contains many bulky capacitors and select components. Figure 2-53 shows the configuration under consideration.

The exact center frequency is determined by the reactance of the termination while the resistive component determines the bandwidth. There is considerable interaction between these two effects, making analysis difficult. It is thought that making the parallel reactance of the terminations equal to $-2C_o$, where C_o is the crystal shunt capacitance, will give the filter a center frequency equal to the crystal center frequency. Thus it is desired to make the transformers in figure 2-53 resonate with about 4 pf at 45 MHz.

2.4.6.2.2 Component Design. The impedance levels needed at the crystal, and the load and source impedances to be used must be determined before transformer turns ratios are known. The load consists of a feedback pair amplifier which has 10 pf shunt capacitance and approximately 500 ohms resistance. It was decided to pad the load resistively to give a shunt resistance of 200 ohms. This will make amplifier impedance variations have less undesirable effects. The source impedance was chosen to be 200 ohms resistive with negligible reactance.

The filter Q is 45000/10 = 4500 which, along with the crystal series reactance, determines the series loop resistance needed. With a motional capacitance of .00032 pf, the required resistance is about 2700 ohms. It is decided to split this resistance equally between input and output circuits. This condition will probably result in the least filter variations as load and source impedances are varied.

To obtain the required high inductance with a reasonable number of turns requires the use of ferrite cores. Using CF101-Q2 toroid cores, 11 turn

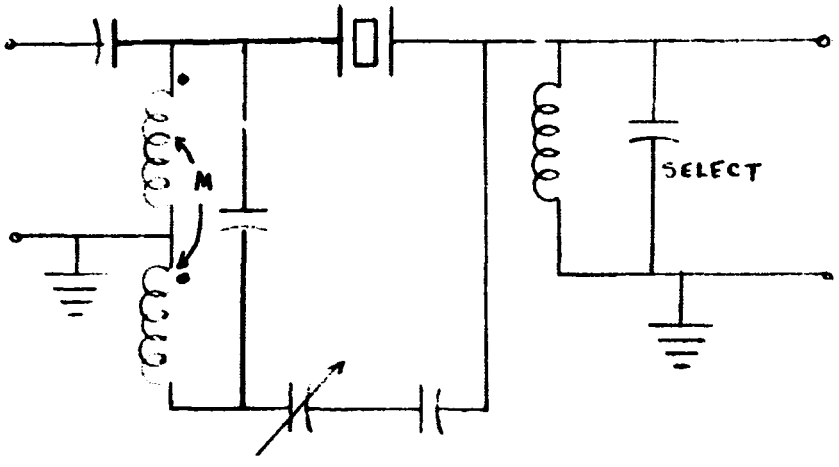


Figure 2-52. SGLS 770 Crystal Filter

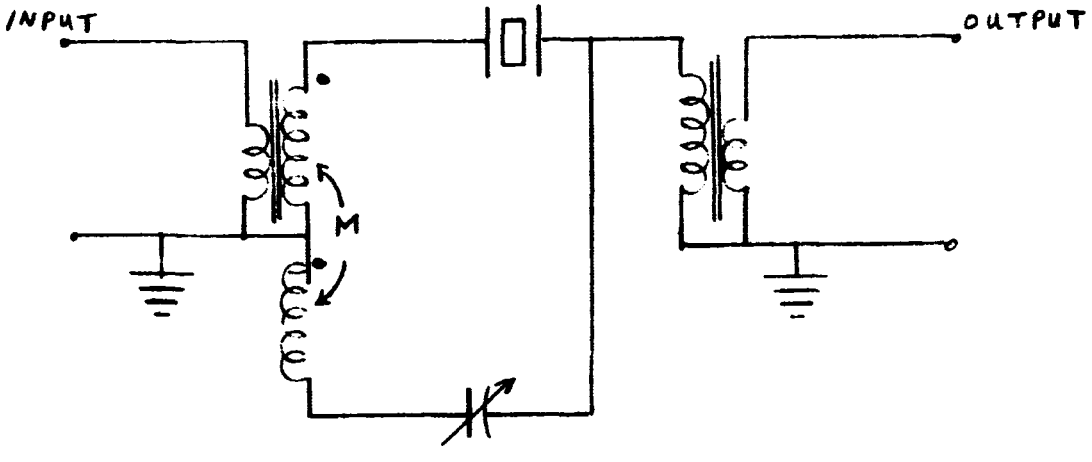


Figure 2-53. Proposed Filter Configuration

secondary windings are required along with a 4 turn primary. Typical R-X meter readings with 220 ohms connected across the primary are:

C_p = -5 pf $\pm$1.5 pf

R_p = 1350 ohms $\pm$50 ohms

The output transformer uses the same core and has a 19 turn primary and 7 turn secondary. Its R-X meter readings at 45 MHz with 220 ohms across the secondary are:

C_p = -3.4 pf $\pm$.2 pf

R_p = 1350 ohms $\pm$50 ohms

The variable capacitor is used to null the effect of Co and requires that the 1:1 input transformer secondary provide a 180° phase reversal. This capacitor tends to limit the small physical size which can be obtained with a crystal filter. It was decided to fabricate a capacitor rather than use a commercially available item. The one used on breadboard models is a parallel plate capacitor using a .032 inch thick teflon board as the dielectric. One side of this .4" x .3" device contains many small squares of copper clad material which can be joined through soldering to increase capacitance.

2.4.6.3 Experimental Results

Early in the filter development, transformers resonant at 45 MHz were tried to determine the effect of purely resistive loads. As predicted by theory, the lower 3 db frequency was 45.000 MHz. Making the terminations inductive does indeed lower the center frequency.

The filter was designed using a purely resistive load. With the transformer impedances given, the center frequency was within 500 Hz of 45 MHz (usually high). When a 10 pf capacitor was included, the center frequency went to about 45001 kHz with a bandwidth near 10 kHz. This is where the present filter is centered. The effect of a shunt capacitor is to change the series equivalent load resistance and therefore change the primary resistance.

The voltage gain of the filter is about unity. However, measured coil impedances indicate about 1 db power loss per transformer so a 2 db power loss occurs.

The variable balancing capacitor is adjusted to give symmetrical -30 db points which are typically ±150 kHz. Too small a capacitance will give a null above 45 MHz while too large a capacity results in a null below 45 MHz. Another effect of this capacitor being wrong is to allow leakage on the far out skirts. Typically a 35 db attenuation cannot be achieved on at least one skirt if this capacitor is mistuned. An outband attenuation of 50 db results near 2 MHz when properly tuned. The actual tuning of this balance capacitor, however, is not difficult and usually does not need retuning if other things are changed excluding the input transformer.

Temperature stability of the filter was also tested. These results are shown below.

Temperature (^{o}C)	F_o (kHz)	Lower 3 db (kHz)	Upper 3 db (kHz)
+25	45000.84	44995.96	45005.94
+80	45001.50	44997.00	45006.04
-40	45000.87	44998.00	45003.89

Performance is severely degraded at -40^{o}C and is probably due to a changing transformer core permeability or loss factor or both. Time die not permit looking further into the cause.

2.4.6.4 Problem Areas

The primary problem of concern in this crystal filter is the temperature stability. Obviously the crystal source and/or load impedances are changing as a function of temperature. The ferrite cores are probably the cause and may not be usable at low temperatures when stable core characteristics are needed. It may be possible to obtain a ferrite core which has a low temperature coefficient down to that temperature.

Some improvement can be made to the input transformer design. Presently the secondary windings are twisted loosely and wound bifilar. Because of the phase reversal connection, the capacity between the two windings affects the R-X meter reading quite appreciably. The tightness with which the wires are twisted affects the C_p reading. This problem might be alleviated by no twisting or crossing over of the two windings providing better repeatability. If this is done, the number of turns may have to be changed for correct center frequency to be achieved.

It is believed that the center frequency can be moved much closer to 45 MHz with a minimum amount of experimental testing by changing the number of transformer turns. Once the transformer inductances and turns ratios are determined, the center frequency and bandwidth will occur simultaneously.

The real space saving as well as problem-incurring device of this crystal filter is the ferrite transformer. Obtaining a temperature stable transformer is the ultimate requirement to build a crystal filter in the proposed circuit configuration. Evidence indicates that performance is quite repeatable depending only on correct transformer impedances. Presently these transformers are suitable at room temperature.

2.4.6.5 Quartz Crystal Item Requirement Specification (IRS)

ITEM REQUIREMENTS SHEET

MOTOROLA DOCUMENT NO.

FED SUP CLASS

REQUIREMENTS

SERIES RESONANT FREQUENCY, THIRD OVERTONE

45.0 MHz, ±.0015% at 25°C
±.001% over range - 30 to +80°C

MOTIONAL CAPACITANCE

.00035 ±.00005 pf

EQUIVALENT SERIES RESISTANCE

300 Maximum

Crystal is to be used in a single-pole filter and spurious responses are important.

DESIGN GOALS

The following are considered design goals for the spurious responses when measured in a balanced half lattice.

Deviation From F_o	Spurious Level db Below F_o Response
0 ±50 kHz	40
±(50 to 150)	25

CONSTRUCTION

Crystal element shall be mounted at three points minimum. Electrical connections to the resonator made to pins 1 and 3 of T0-5 case. Case to be evacuated. Dimensions of case as defined in JEDEC 12-E except flange dia. (D) to be .410 max.

SUPPLIER

McCoy Electronics Co.
Mt. Holly Springs, Pa. 17065

REV

CHK

MOTOROLA INC.
Government Electronics Division
Aerospace Center

CRYSTAL, QUARTZ

PROJECT 3433

MOTOROLA DOCUMENT NO. 48-22404M01

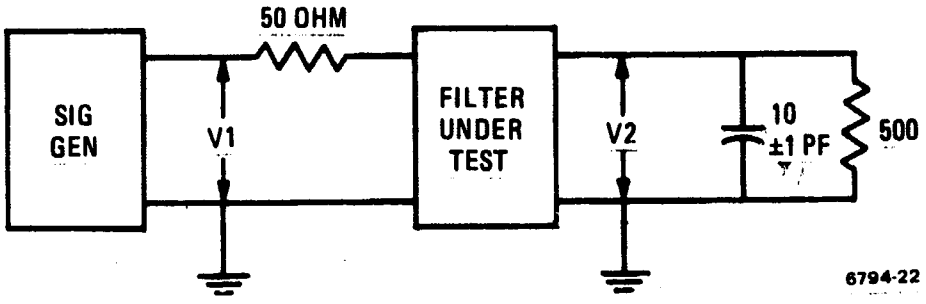
PROCUREMENT SPECIFICATION | FIIN

CONTRACT NO. | SHEET OF | CODE 14990

2.4.6.6 Crystal Filter Specifications

Exerpts of a crystal filter IRS used on a previous project are included in this section to provide an example of typical filter design requirements. Of special interest is the phase shift and amplitude symmetry requirements.

FED SUP CLASS 5915



$$\text{INSERTION LOSS IN DB} = 20 \log \frac{V1}{V2} + 4.$$

Figure 2. Insertion Loss Test Circuit

1. SCOPE : This Item Requirements Sheet (IRS) specifies minimum requirements for Single Pole Crystal Bandpass Filters. This document is not a complete description of the items; it must be used with the Applicable Documents, Section 2.

1.1 RATINGS: Per MIL-F-18327, Type FR4SX22YY.

1.1.1 Ambient Temperature Range: -34°C to +90°C, Operating
-65°C to +100°C, Storage

1.1.2 Barometric Pressure: 30 psia

1.1.3 Power Input: -3 dbm max. (0 dbm = 1.0 mw in 50 ohms).

2. APPLICABLE DOCUMENTS: Per MIL-F-18327, Filters, High Pass, Low Pass, Band Pass, Band Suppression, and Dual Functioning. In addition, the following documents, of the issue in effect on the date of request for quotation, apply to the extent specified herein.

MIL-STD-130	Identification Marking of U.S. Military Property
MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
Handbook H4-1	Federal Supply Code for Manufacturing
MIL-STD-456	Electronic Parts, Date and Source Coding for

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MOTOROLA INC. Government Electronics Division Aerospace Center	FILTER, BANDPASS - CRYSTAL, SINGLE POLE	PROJECT 3330
PROCUREMENT SPECIFICATION MIL-F-18327 / FIIN		MOTOROLA DOCUMENT NO. 25-28960E
CONTRACT NO.	SHEET 2 OF	CODE 94990

FED SUP CLASS 5915

3. REQUIREMENTS: Per MIL-F-18327, Type FR4SX72YY and this IRS. The electrical parameter specified for attenuation shall be measured using the Attenuator Substitution Method or approved equivalent.

3.1 QUALIFICATION: Listing on the QPL is not required.

3.2 TERMINALS: Four pin or hook type terminals shall be provided, and shall be capable of accommodating three No. 22 AWG stranded wire leads. Compression glass terminals shall be used for the "IN" and "OUT" terminals and the "Gnd" terminals shall be connected to the case.

3.3 DIELECTRIC WITHSTANDING VOLTAGE: Not applicable.

3.4 INSULATION RESISTANCE: Not applicable.

3.5 REFERENCE FREQUENCY: 12.250000 MHz.

3.6 POWER INSERTION LOSS AT REFERENCE FREQUENCY (see figure 2) 3 db maximum.

3.7 PASSBAND CHARACTERISTICS: Over the temperature range, the filter shall meet the following requirements.

Attenuation	Deviation From Reference Frequency
3.0 db	5.00 kHz ±500 Hz at 25°C, 3 db frequency change over temperature range from 25°C frequency: ±500 Hz maximum.
30 db	175 kHz max.
30 db symmetry	±50 kHz max.
50 db Min.	2.0 to 3.0 MHz

3.8 PHASE CHARACTERISTICS

3.8.1 Phase Shift at Reference Frequency: The output signal shall lag the input signal by 251.5 ±5° at 25 ±5°C. The change in reference frequency phase shift over the specified ambient operating temperature range from that at 25 ±5°C shall not exceed 10°.

3.8.2 Outband Phase

3.8.2.1 At ±30 kHz from the reference frequency: ±92° maximum from the reference frequency phase shift at the corresponding temperature.

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MOTOROLA INC. Government Electronics Division Aerospace Center	FILTER, BANDPASS - CRYSTAL, SINGLE POLE		PROJECT 3330
PROCUREMENT SPECIFICATION MIL-F-18327	FIIN		MOTOROLA DOCUMENT NO. 25-28960E
CONTRACT NO.	SHEET 3 OF	CODE 94990	

FED SUP CLASS 5915

3.8.2.2 At +100 kHz from the Reference Frequency: 112° maximum from the reference frequency phase shift at the corresponding temperature.

3.8.3 Phase Slope Over ±1 kHz from the Reference Frequency: 11.5 ±2°/kHz.

3.9 SPURIOUS RESPONSE: There shall be no spurious response greater than 1.0 db peak-to-peak within ±80.0 kHz from the reference frequency or greater than 8.0 db peak-to-peak within ±300 kHz from the reference frequency.

3.10 FILTER IMPEDANCES

3.10.1 Driving Source: 50 ohms ±10 per cent.

3.10.2 Load: 500 ohms ±10 per cent shunted by 10.0 ±1 pf.

3.11 VIBRATION: Phase modulation during vibration shall not exceed 1.0 degree at reference frequency.

3.11.1 Sinusoidal: MIL-STD-202, Method 204, Test Condition D, except 20 to 88 cps, 0.25 inch DA; 88 to 2000 cps, 100 g's.

3.11.2 Sinusoidal: MIL-STD-202, Method 204, Test Condition C, except 20 g's.

3.12 SHOCK

3.12.1 Shock: 10,000 g's peak, half sine wave, 0.2 ms., MIL-STD-750, Method 2016.

3.12.2 Shock: MIL-STD-202, Method 202, 50 g's one shock in each direction in each plane.

3.13 WEIGHT: 3.0 oz. maximum.

3.14 MARKING: The source, identified per MIL-STD-456, the unique serial number, the part number, the vendor's identification number in parentheses, and the terminal identification shall be marked on the part per MIL-STD-130.

3.15 WORKMANSHIP: The requirements of Motorola Workmanship Standards shall apply to the assembly, internal and external.

3.16 LIFE (Group C Test); 1000 hours at 85°C. Reference frequency phase shift measurements shall be made at 25, 250, 500, and 1000 hours at 25 (±5)°C.

4. QUALITY ASSURANCE PROVISIONS

4.1 QUALIFICATION INSPECTION: Not applicable.

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2.5 DETECTOR MODULE

The subsection of the Advanced S-Band Transponder Program final report describes the detector. The detector module performs the following functions:

1. Contains a 45 MHz crystal oscillator used for detector references.
2. Drives the synthesizer with a 22.5 MHz signal.
3. Provides narrowband phase detection for the phase locked loop.
4. Provides coherent amplitude detection and output AGC voltage.
5. Provides wideband detection and ranging information output.
6. Provides phase adjustment between the three detectors, and,
7. Provides a signal present output.

The Detector block diagram is shown along with the predetection i-f block diagram in figure 2-54. The schematic of the detector module is included as figure 2-55.

2.5.1 Reference Oscillator and Divider

The 45 MHz reference oscillator is a common base Colpitts oscillator which uses a crystal in its fundamental series resonant mode as the feedback element. The temperature characteristics of the crystal determine the oscillator stability. Temperature compensation could be included but is felt unnecessary.

The buffer transistor, Q3, drives a digital ÷2 consisting of an MC1213 flip flop, used because of its simplicity. This ÷2 was placed in the detector module to prevent transporting a high level 45 MHz signal to another module. This eliminates one source of possible coherent leakage. The MC1213 has a 15 ohm output impedance and delivers approximately -5 dbm to the high impedance synthesizer load. However, one disadvantage of this device is its relatively large 125 mw power dissipation. The 22.5 MHz output square wave of the ÷2 drives the ÷26 frequency divider of the synthesizer.

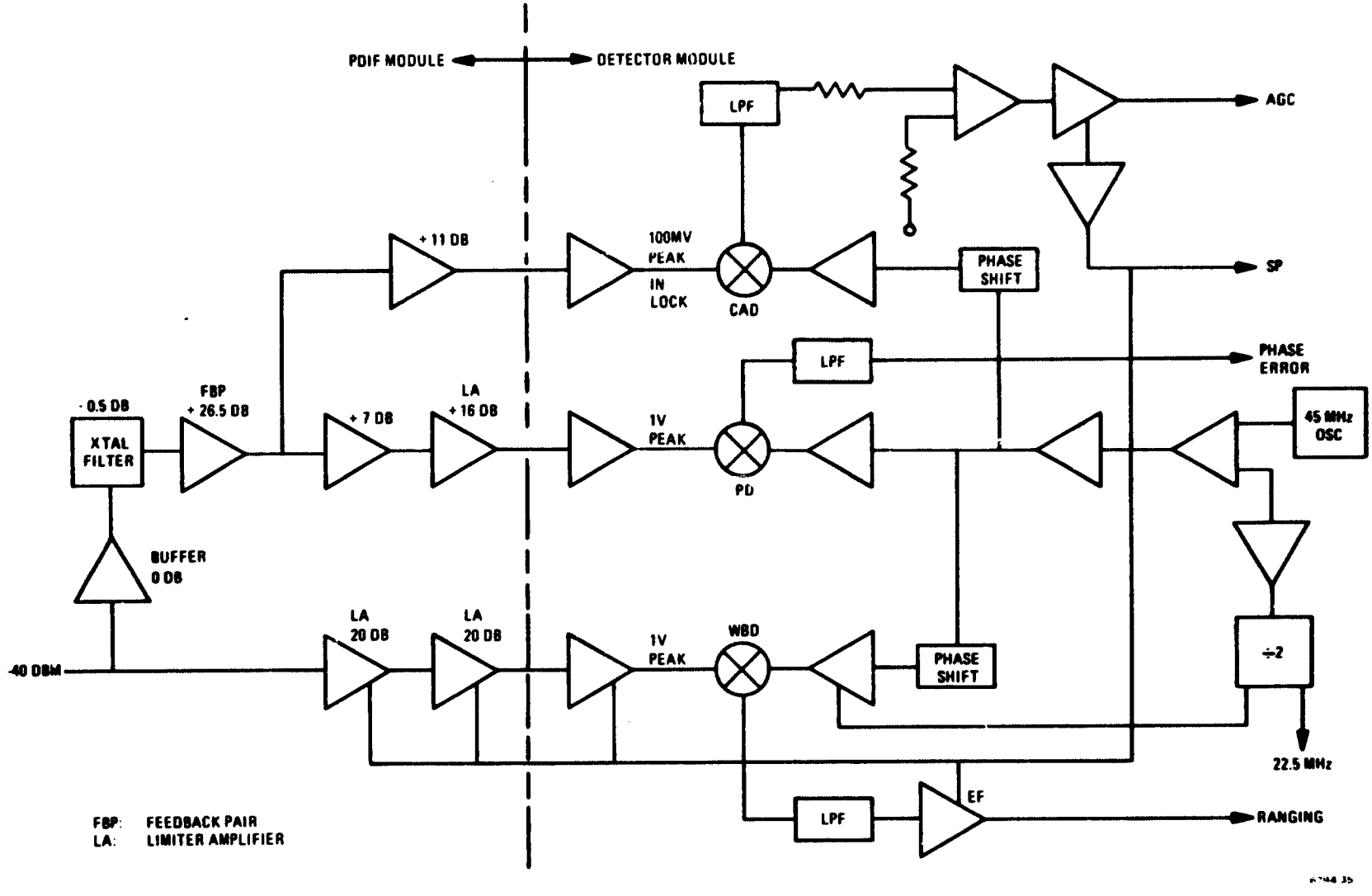


Figure 2-54. Predetection I-F and Detector Block Diagram

2.5.2 Phase Detector

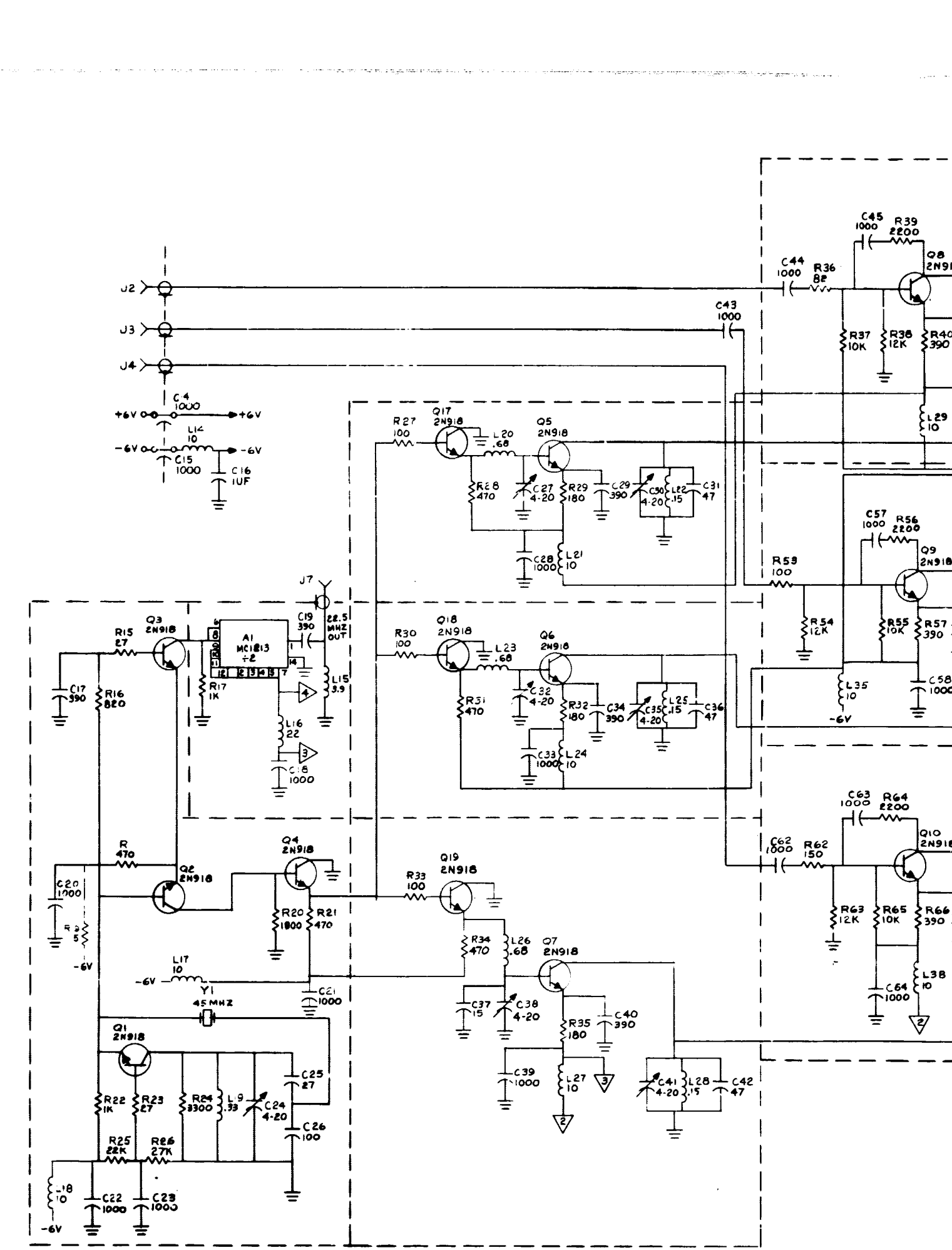
The three phase demodulators used in this module are identical . They are built using a ceramic substrate, leadless-inverted-device (LID), packaged hot carrier diodes, chip resistors, and miniature ferrite transformers mounted on a TO-5 header. The layout and schematic are given in figure 2-56. The first detectors built did not perform well due to a large unbalance. It was found that the diodes were damaged during their mounting process. After this was corrected, a typical isolation of 55 db was obtained, which is considered quite satisfactory. To obtain this amount of balance, selected quads of diodes are needed. This selection process is discussed in paragraph 2.5.7. The transformers are made on CF-118 Indiana General cores of type H material. The windings consist of 21 turns #40 wire wound trifilar. The high permeability and loss factor of H material should give a wideband low Q transformer.

The phase detector is in the phase lock loop and provides an error voltage which corrects the VCXO to track the input frequency. The reference voltage obtained from the oscillator and limiting amplifier controls the conductance of each diode pair by switching them off at each alternate half cycle. For more detail on the detector operation, refer to TM # CWT-135, Detector Module Design and Evaluation for Receiver, IDP 7689, by Ed Smoot.

The smaller of the two detector signals is obtained from the predetection i-f module after first being amplified by a feedback amplifier. The gain of this amplifier controls the phase detector gain which is $E_p \sin \theta$. The value of $E_p (K_d)$ is presently near 1.0 volts. Only the dc component of the output is used so a low pass filter shunts to ground any high frequency leakage present. The dc amplification of the error voltage is contained in the vcxo module.

2.5.3 Coherent Amplitude Detector and AGC

The CAD is simply a phase detector which is phased 90° from the loop phase detector just discussed. The reference drivers of all three detectors are identical and provide the larger switching signals to the demodulators. The signal input to



FOLDOUT FRAME 1

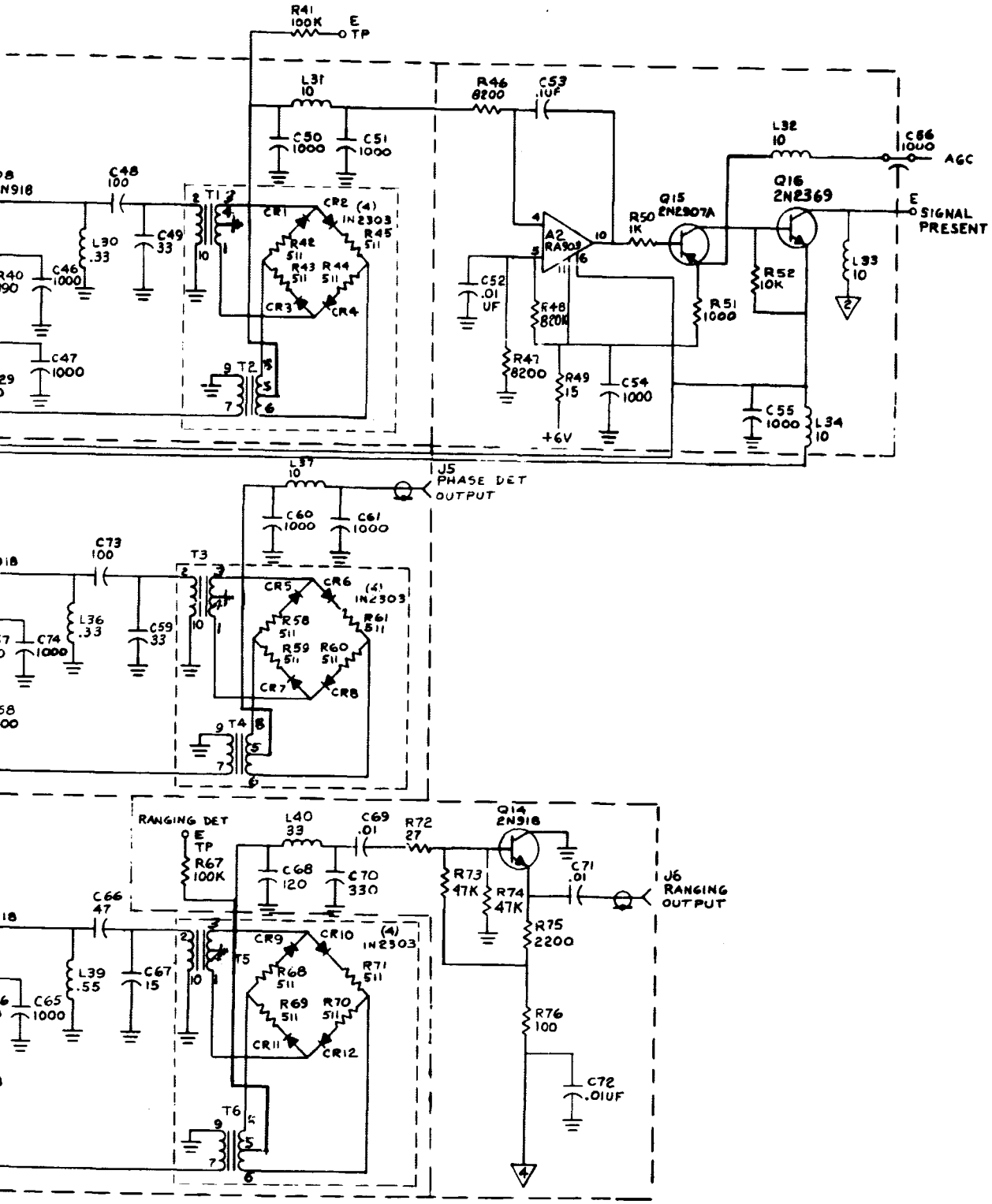


Figure 2-55. Detector Module, Advanced S-Band Transponder

FOLDOUT FRAME 2

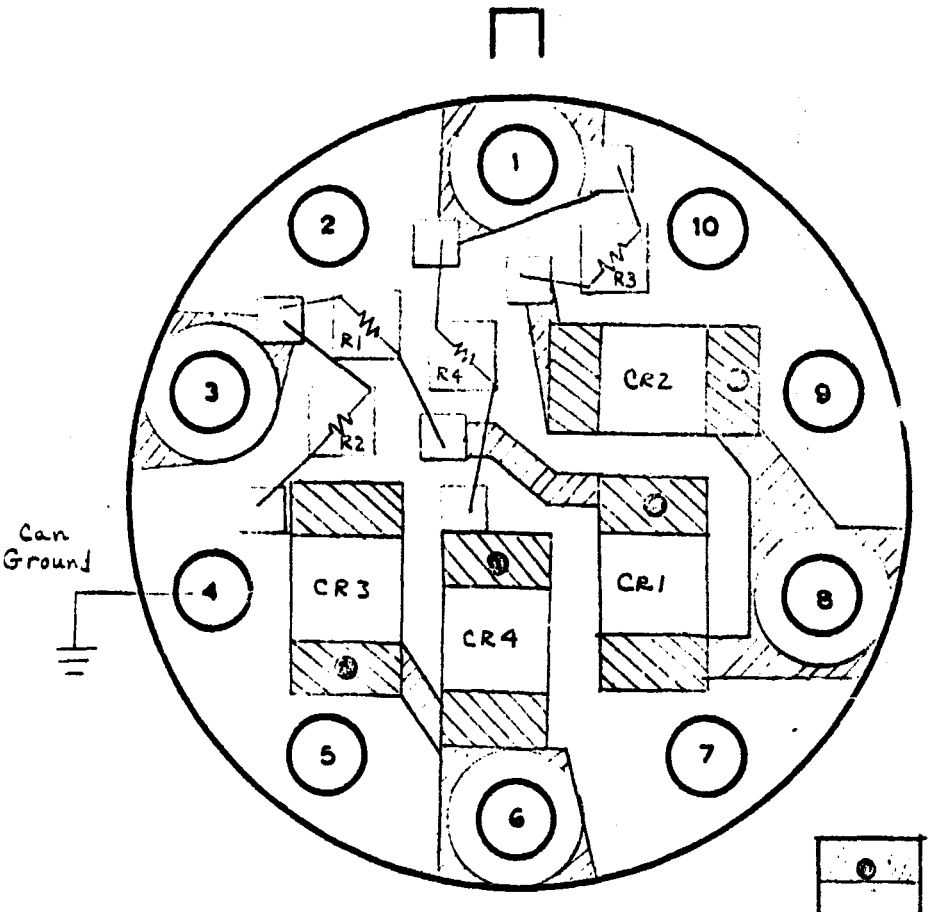
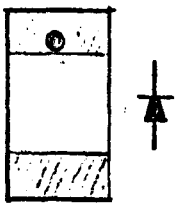
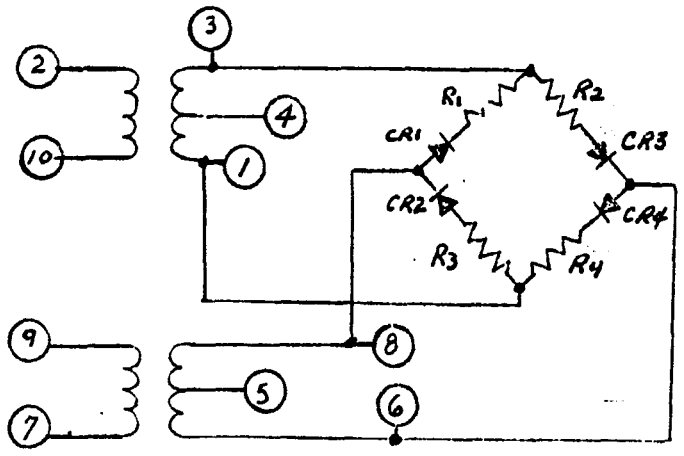


Figure 2-56. ES 418





PROBING REQUIREMENTS

Resistors:

$R_1 = R_2 = R_3 = R_4 = 512\ \Omega \pm 1\%$

All ratios ±1%

Diodes:

CR1 = CR2 = CR3 = CR4

MATCHED

HP LID Packaged

Hot Carrier Diodes

REV.	X
DATE	7/15/68
EFF.	7/15/68
APP'D.	

CIRCUIT LAYOUT & LIST REQUIREMENTS TO-5 HEADER I. C. FACILITY

DR: W. Shaw

LAYOUT APPROVAL: [illegible]

PROBE REQ APP: [illegible]

TITLE: ES 418

PROJECT NO.: 5433

PRINT NO.:

SCALE 15:1

ORIG. ISSUE

DATE: 5-14-68

PAGE: 2-131

the CAD is obtained from the predetection i-f module and a feedback amplifier. The gain of this detector is phased for $E_p \cos\theta$ where E_p is approximately 100 mv. The low gain in this channel is necessary in order for the amplifiers succeeding the crystal filter to handle noise 20 db higher than the signal without limiting.

A low pass filter follows the CAD output since only the dc component is used. This dc error voltage is amplified by high gain operational amplifier A2 and buffered by Q15 as shown in figure 2-55. The AGC voltage is fed to the first i-f amplifier and automatically keeps its output near -40 dbm. In case of no signal present, the phase detector output is near 0 volts, the noninverting input of A2 is biased near +60 mv which saturates the output at +5 volts. This causes Q15 to turn off and the AGC output is positive which allows the first i-f to operate at maximum gain. If the loop is locked, however, a strong signal drives the CAD, and A2 is driven negative on its output causing Q15 to conduct and transfer this negative voltage to the AGC output. This negative voltage will attenuate the signal in the first i-f causing a balanced closed loop condition to exist.

Before lock, Q16 in figure 2-55 is turned off resulting in 0 volts at the signal present output. This turns off the wideband channel to conserve power and allows the vcxo sweep circuitry to search for an incoming signal. After lock has been achieved, this signal present output is between -5.5 and -6 volts which squelches the vcxo sweep and turns the wideband channel on.

2.5.4 Wideband Detector

The wideband detector is used to demodulate the phase modulated ranging information on the input signal. The signal input is obtained from the predetection i-f limiters. A feedback amplifier, Q10, is used to raise the signal level to nearly 1 volt peak. This detector is phased the same as the loop phase detector giving an output equal to Sin θ.

The wideband output drives a low pass filter with a cutoff frequency of 2.2 MHz. The output impedance of the preliminary cordwood phase detectors was measured to be 400 ohms which was used to design the singly terminated filter shown in

figure 2-55. The response is shown in figure 2-57. Later it was found that this filter would not work with the TO-5 detectors. The problem lies in the detector output impedance. The TO-5 detector had a 600 ohm output resistance and started to increase above 1.5 MHz. A redesigned filter worked satisfactorily but the exact shape near 2 MHz is not as calculated due to this changing impedance. It is believed that this is the reason for the flattening of the response in figure 2-57 also. The emitter follower, Q14, is used to provide a high impedance load to the filter and a low output impedance.

2.5.5 Phase Shifters

Variable phase shifters are included in all three reference drive circuits. Only two are ultimately necessary but three gives more adjustment range which is needed for breadboard work. The variable capacitors, C27, C32, and C38 allow these adjustments. Approximately 90^{o} phase shift range is possible for each one. This range was found sufficient in the breadboard receiver. It was found necessary to isolate the phase shifters with an emitter follower to prevent interaction.

It has been noted that a dephasing can occur when the wideband channel is turned off or on by the signal present voltage. It was found that applying -6 volts to the signal present terminal with no signal input, caused the loop phase detector output to shift 60 mv or 3.5^{o}. This effect could be due to differential loading on Q4 of figure 2-55, or it might result from differing amounts of coherent leakage. Future modifications may include leaving the WBD reference driver on at all times to eliminate this source of error.

2.5.6 Diode Matching Techniques

The phase detectors used in this receiver require a high degree of balance, or input-output isolation. This is achieved by using matched quads of diodes and matched resistors. Since it is very easy to obtain matched resistors when using integrated circuits, this section deals with selecting the diodes.

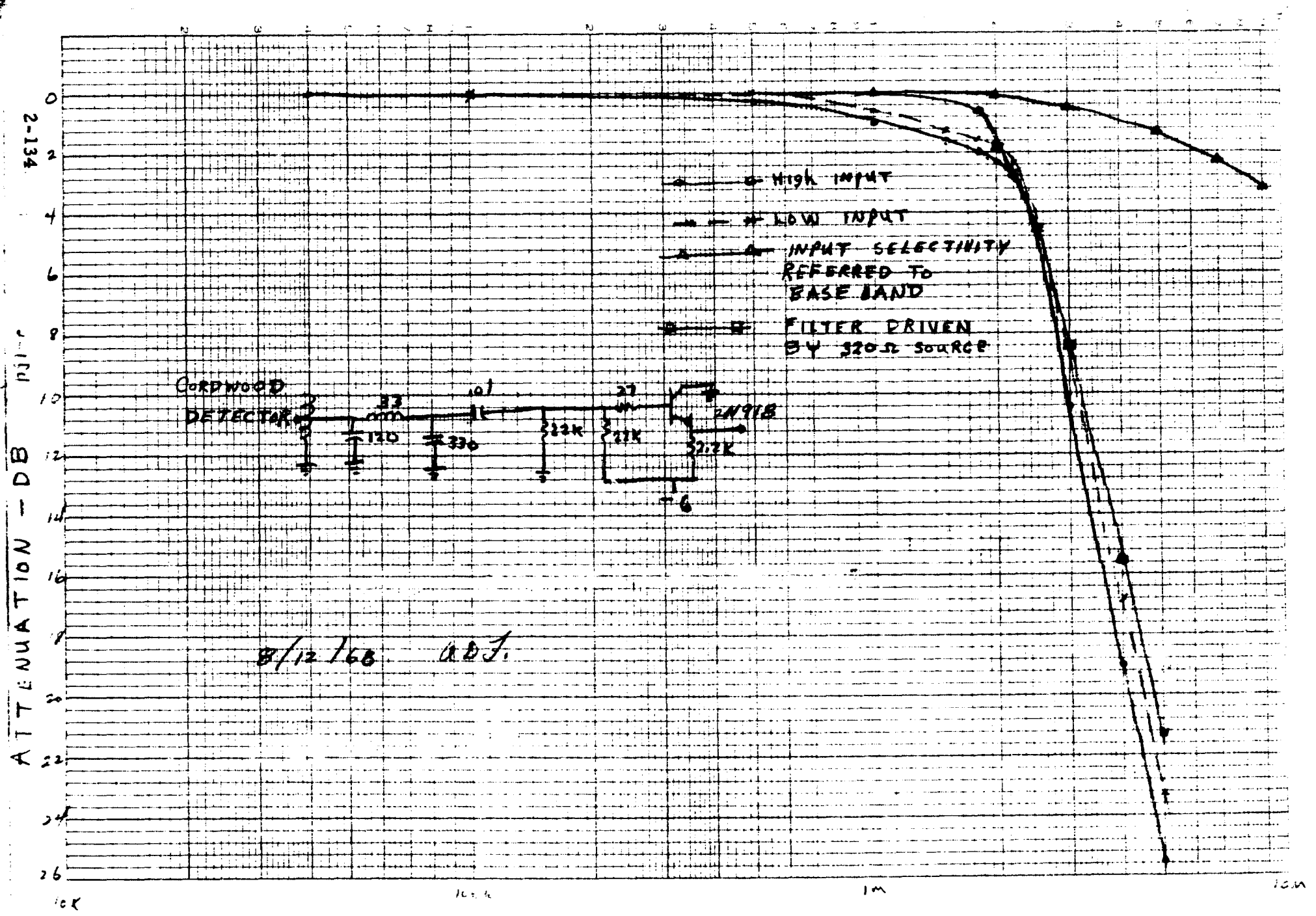


Figure 2-57. Wideband Frequency Response

There are two ways to select the diodes for each phase detector matched quad. The most involved method is the ac test shown in figure 2-58. Each diode of a given lot is compared against a reference diode by observing the difference in the rectified voltage that is developed at points A and B due to the reference diode and the diode under test, respectively. The smaller the difference the better the match. This method would be difficult to implement when testing chips, mini-strips, or LIDS, however.

The second method has been used with excellent results and is a much easier test to perform. Each diode is merely probed for forward voltages versus forward current using an HP 3444A dc multi-function plug-in unit for an HP 3440A digital voltmeter. This method can be used with confidence on a high quality hot-carrier diode that has low junction capacity, but is not recommended beyond that.

The diode data of table 2-5 is from an order of 30 HPA 2300 series hot-carrier diodes in the LID configuration using method 2. The forward voltage is checked at various levels of current. Particular interest is given to the diodes in the low current region to see if the voltage charge is close to the theoretical 60 mv per decade of current.

The latest data taken on the diodes that make up the quads for each of the detectors presently in use is shown in table 2-6.

When the first hybrid phase detectors were built, one or more diodes in each were found to be defective and it is suspected that they were damaged during the bonding and/or soldering process. Each step in the construction process must be carefully controlled with care given to the amount of heat applied when soldering the transformer leads to the header pins and when soldering the LIDs to the substrate. The melting point of the tin-lead solder used for the latter process is 180°C and an effort was made to keep the applied temperature at less than 200°C.

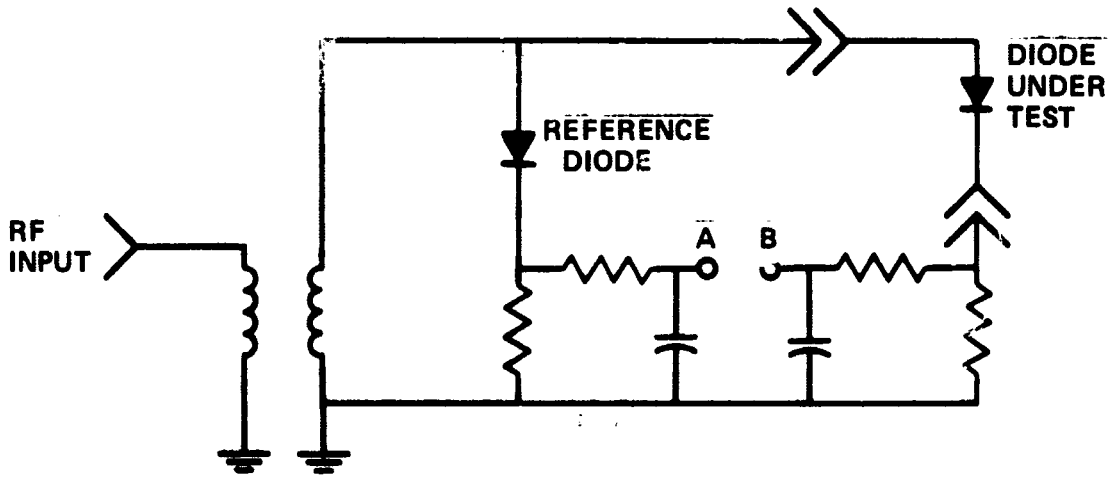
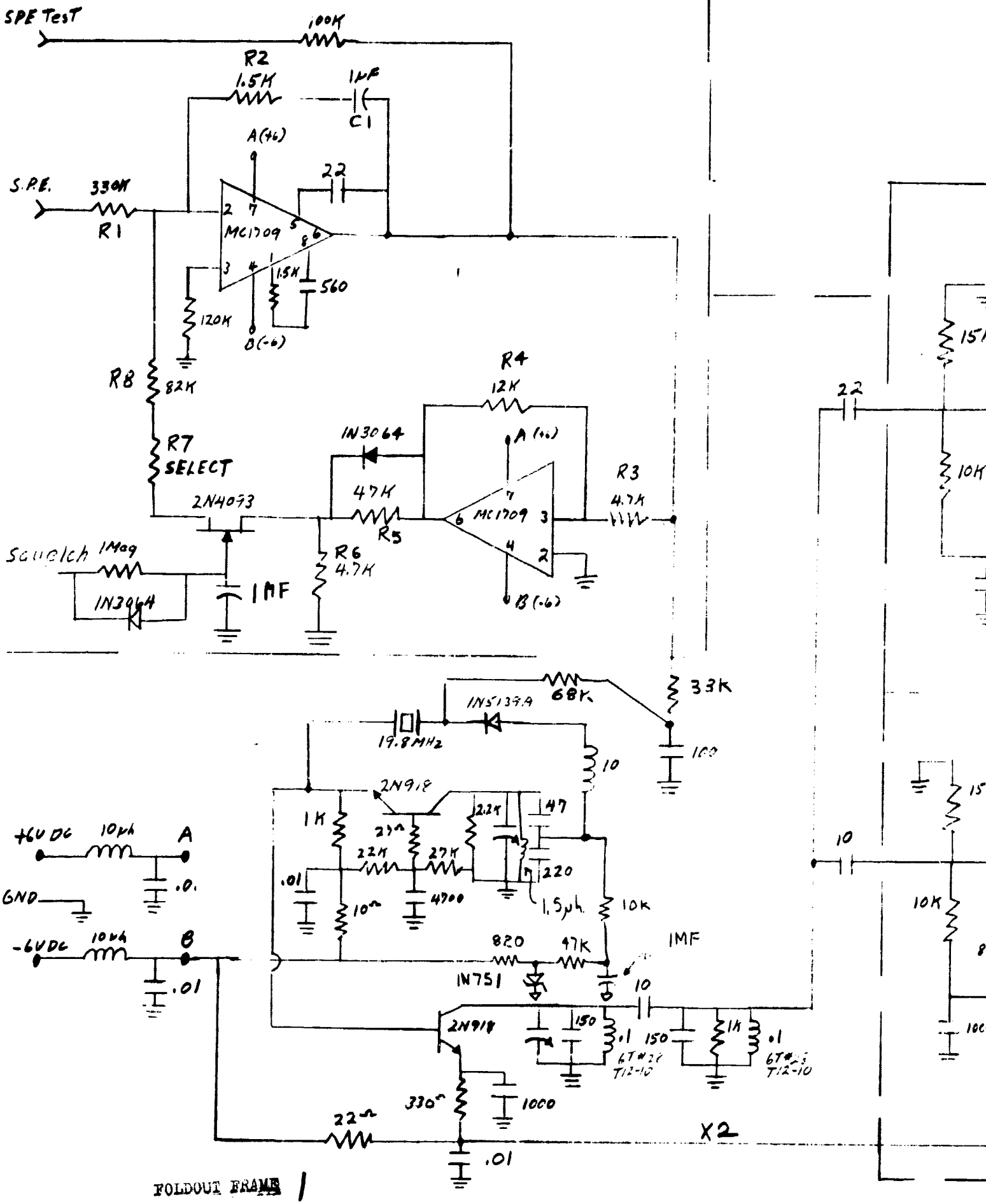


Figure 2-58. AC Matching Technique

Table 2-5. Forward Voltage vs Forward Current

Diode No.	1 ma	100 μa	10 μa	1 μa
1	390.2	313.8	249.8	187.7
2	334.2	260.1	195.0	134.3
3	345.8	270.9	204.1	144.6
4	347.6	272.2	208.2	146.8
5	348.5	273.6	209.8	148.3
6	340.6	266.1	202.0	140.9
7	334.8	260.9	197.1	136.0
8	358.1	280.2	215.5	153.7
9	328.1	254.9	191.5	130.5
10	332.6	258.7	195.2	134.0
11	336.5	263.1	199.4	137.9
12	344.8	266.9	202.8	141.5
13	338.3	267.7	204.3	142.8
14	354.7	281.2	217.3	155.7
15	342.4	267.4	200.6	129.1


SPE TesT
100K
R2
1.5K
1MF
C1
A(+6)
22
S.P.E.
330K
R1
MC1709
1.5K
560
120K
B(-6)
R8
82K
R4
12K
IN3064
A (+6)
R7
SELECT
47K
R3
4.7K
2N4093
R5
MC1709
Squelch
1Meg
R6
4.7K
IN3064
1MF
B (-6)
68K
33K
IN5139A
19.8MHz
100
10
2N918
1K
2.2K
47
27K
22K
220
.01
10K
4700
1.5μh.
820
47K
IMF
IN751
10
+6V DC
10μh
A
.01
GND
-6V DC
B
.01
150
.1
6T#22
T12-10
1K
.1
6T#
T12-10
330Ω
1000
22Ω
.01
X2
FOLDOUT FRAME 1

159 mHz filters modified 7-19-68 A.U.J.
Varacto bias modified 7-25-68 AJ:

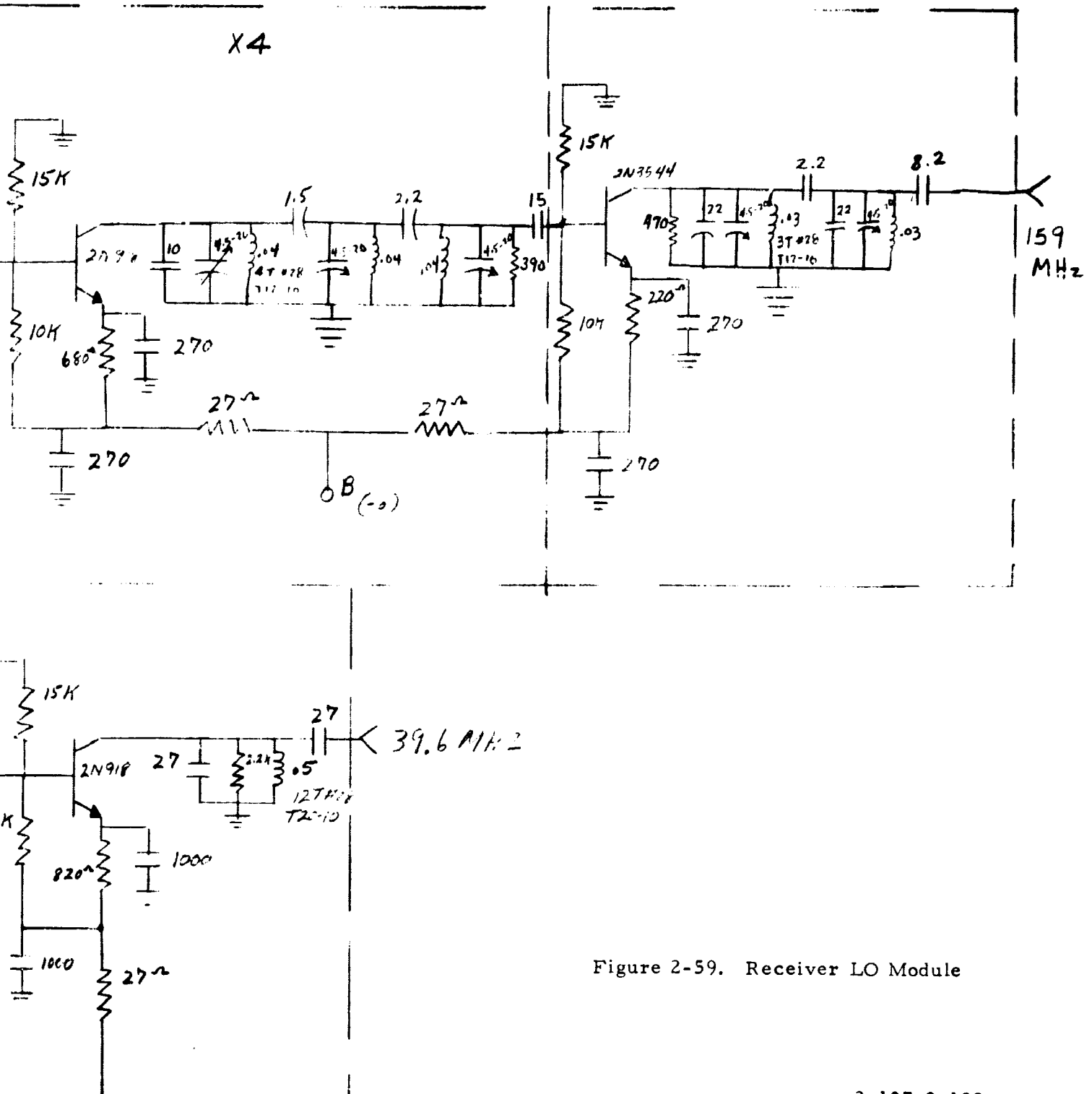


Figure 2-59. Receiver LO Module

2-137, 2-138

FOLDOUT FRAME 2

Table 2-5. Forward Voltage vs Forward Current (cont)

Diode No.	1 ma	100 μa	10 μa	1 μa
16	363.8	288.5	224.3	162.6
17	322.7	249.8	186.6	125.7
18	350.0	275.8	211.7	149.8
19	350.6	276.3	212.2	150.5
20	329.9	256.1	192.6	131.4
21	335.5	261.0	197.2	135.9
22	351.8	277.6	213.6	152.0
23	337.4	263.6	194.4	136.5
24	329.6	255.7	192.1	131.0
25	333.8	258.5	194.7	133.4
26	325.8	252.6	188.9	128.2
27	340.2	266.3	202.5	141.1
28	343.8	264.6	192.0	86.6
29	371.5	296.3	231.5	169.6

Table 2-6. Forward Voltage vs Forward Current

TO-5 Can No.	1 ma	100 μa	10 μa	1 μa
	342.8	267.7	202.6	141.1
6	344.0	269.2	204.6	143.1
	343.6	268.5	203.0	141.4
	346.3	269.4	205.0	142.2
	356.8	282.7	219.3	157.6
8	351.4	277.4	214.1	152.6
	355.0	279.0	215.5	153.6
	352.8	277.3	213.5	151.7
	338.5	263.9	201.1	140.1
5	340.7	265.6	202.3	141.0
	340.2	266.3	203.2	141.8
	334.0	260.8	198.1	137.1

2.5.7 Packaging

The detector is probably the most critical portion of the whole receiver as far as packaging is concerned. Coherent leakage from the reference oscillator must not be present at the i-f module inputs at a level which will degrade performance. Equally critical is the layout within the detector module to make sure reference signals do not appear in the signal amplifiers. This would result in dc offsets at the detector outputs.

Extreme care was taken in the module layout to prevent harmful ground currents. The ground planes for input amplifiers and reference drivers are separate. This is possible due to the transformer coupling into the phase detectors. Each ground plane ties to the frame at only one point. This point is where the particular input or output exists. This technique seems to work well as only 2.5 mv detector offset is noted. The frame used is 3 x 5 x 6 inches. It is anticipated that this can be reduced to 2 x 4 x .5 inches if some hybrid circuitry is used. Prime circuits for hybrid adaptation are the oscillator, feedback amplifiers, and reference drivers.

Problems were encountered in shielding the module to prevent radiation to other modules. To keep the high level 45 MHz inside the detector clamped shields had to be used around the module. Using aluminum adhesive tape alone, was not adequate. This problem requires further investigation to determine the exact source of the radiation and a suitable shielded package.

2.6 LOCAL OSCILLATOR MODULE

The local oscillator module (LO) contains the phase lock loop vco, dc amplifier, sweep circuit for automatic acquisition, and part of the multiplier chain (X8). The circuitry used is quite conventional with no attempt at miniaturization. The schematic diagram is given in figure 2-59.

2.6.1 Voltage Controlled Crystal Oscillator (vcxo)

The oscillator is a common base Colpitts type with feedback provided by a series resonant fundamental mode crystal. The breadboard crystal frequency is

19.821 MHz. A series varicap is used to control the vco frequency from an amplified loop error voltage. The inductor in series with the varicap is used to bring the oscillator center frequency to the correct value. A zener diode regulated supply reverse biases the varicap. An r-c decoupling network prevents power supply noise from modulating the diode. A ceramic 1 μf capacitor is used for the least capacitor noise.

The sensitivity of this vcxo is approximately 1.3 kHz/volt. Its characteristic is included in figure 2-60. The linearity could be improved with an inductor shunting the crystal but is not considered necessary due to the limited sweep range necessary.

2.6.2 Loop Filter

The loop filter determines the tracking and acquisition capabilities of a phase lock loop. For a desired threshold of -128 dbm, a loop noise bandwidth, $2B_{LT}$, of 1000 Hz was chosen. This gives a suppression factor, α_{th}, of .43 assuming a 10 db noise figure. Letting the damping factor, ζ, equal .707 at threshold, $B_{LT} = .53 W_n$. Now $W_n^2 = Kv\ Kd\ M\alpha/T_1$ and $\zeta^2 = .25T_2\ Kv\ Kd\ M\alpha/T_1$ where T_1 and T_2 are the filter time constants. From these equations it can be seen that $T_1 = .281\ Kv\ Kd\ M\alpha/B_{LT}^2$ and $T_2 = .75/B_{LT}$. Also, $T_1 = R_1C$ and $T_2 = R_2C$ in figure 2-59. Choosing C = 1 μf , R1 = 316K and R2 = 1600 ohms. The nearest standard value resistors are used.

The operational amplifier provides high gain (45,000) to dc which allows the loop phase detector output to contain a very low static phase error (spe) voltage. The spe test point allows monitoring of the phase error after dc amplification.

2.6.3 Automatic Acquisition

An automatic sweep circuit results when feedback is applied between the input and output of the loop filter which is then used as an integrator. A rectangular wave will appear at the feedback amplifier output. This waveform is integrated by the loop filter producing a ramp output. When the ramp voltage reaches a certain

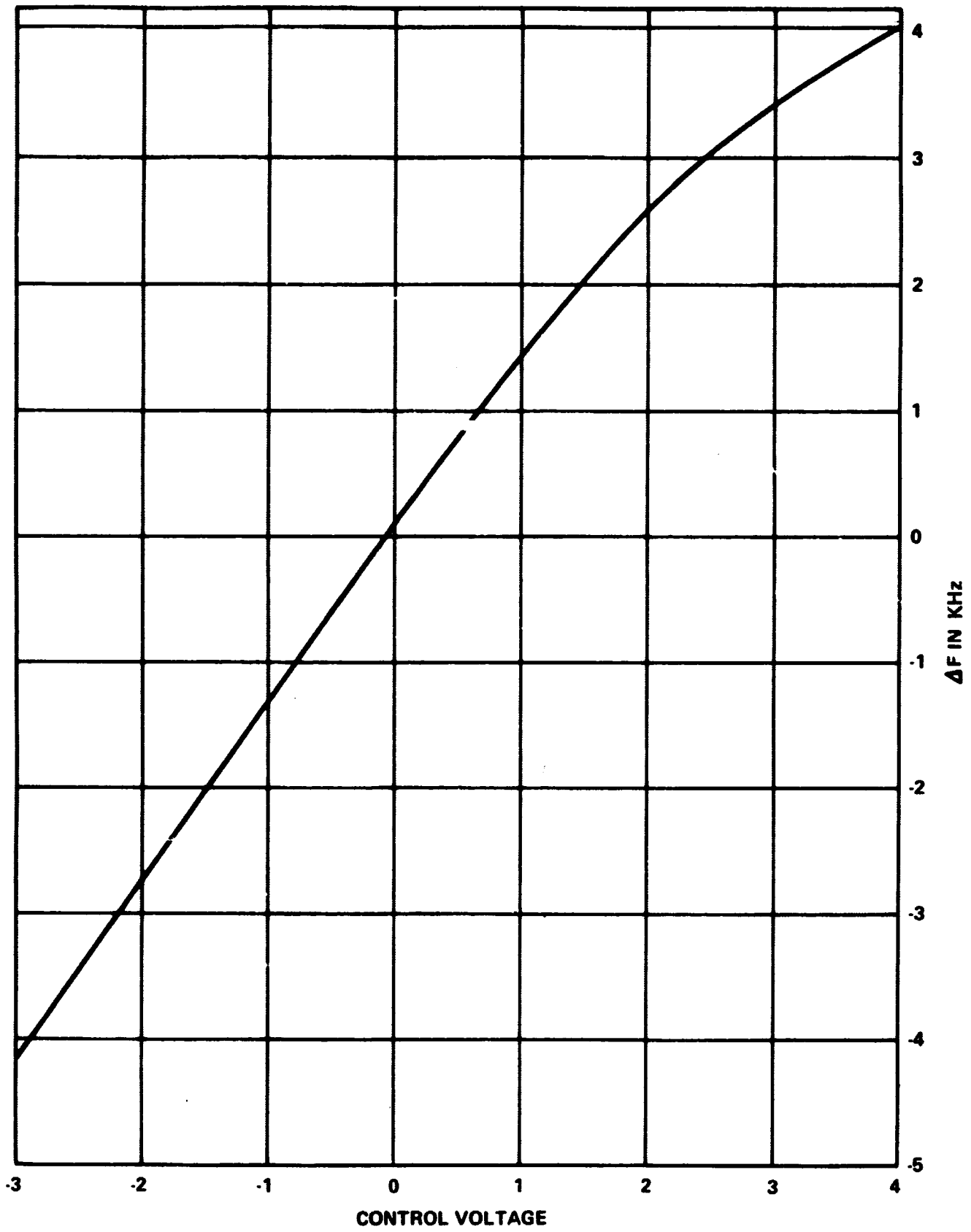


Figure 2-60. 19.8 MHz VCXO Sensitivity

level, such that the feedback amplifier input passes through 0 volts, the amplifier output will swing to the opposite polarity and saturate due to positive feedback. The point at which this amplifier switches is fixed by R3 and R4 in figure 2-59.

A ratio of rise to fall time of 10 is obtained using R5 = 10 R6 and shunting R5 with a diode. When the feedback amplifier output is +5 volts, the current feeding the loop filter input is 5 volts divided by R7 and R8. This provides the ramp output a fast return to its negative peak which in turn switches the amplifier to -5 volts output. Now the diode is reversed biased and . 5 volt divided by R7 and R8 charges C1. This being 1/10 th the previous current, the rise time will be 10 times slower than the fall time.

An FET switch is incorporated to disable the sweep under locked conditions. The squelch input is taken from the Signal Present output of the detector . A -6 volt Signal Present turns the FET off while 0 volts indicates unlock and turns the switch on. The capacitor at the FET gate provides the desired delay time before disabling the sweep.

2.6.4 Multipliers

A X2 transistor stage is driven directly from the oscillator. A two pole filter selects the second harmonic of the collector current waveform. This 39.6 MHz signal is used as one synthesizer input. A current limiter stage is employed to deliver the required 0 dbm output. The required load is nominally 50 ohms.

An output 8 times the vco frequency is needed to drive the X13 step recovery diode in the r-f head. Other requirements are 0 dbm power level, very low spurious outputs, and nominal 50 ohm output impedance. An acceptable alternative for the 50 o' n output impedance is a 2 db 50 ohm pad. This is needed to drive the Class C Amplifier in the r-f converter.

A X4 transistor stage is driven from the X2 output. A three pole singly terminated butterworth filter selects the 4th harmonic. This 159 MHz signal drive a current limiter to provide the required output power. The output stage reduces

spur levels with a 2 pole equally terminated butterworth filter. The measured output vswr is 1.5:1. No interface problems exist with the r-f head.

2.6.5 Packaging

At the present time, all circuits in this module are made from discrete components. Some miniaturization can be accomplished using hybrid techniques. The oscillator seems to be the only real target for this, however, since many narrow bandpass filters are needed which cannot be integrated practically while maintaining tunability. At any rate, the vcxo module should fit in a 2 x 4 x .5 inch module compatible with the present mechanical concept.

2.7 FREQUENCY SYNTHESIZER

2.7.1 Introduction

This subsection describes the digital frequency synthesizer designed for the breadboard system of the Advanced S-Band Transponder Study. The frequency synthesizer operates between the receiver and the transmitter to derive a coherent transmitter excitation from certain receiver output signals. During this study a complete transponder block diagram was conceived and a breadboard model of the complete system was constructed. The original receiver and synthesizer block diagram concepts are discussed in paragraph 2.3.

The feasibility of this type frequency synthesizer was an especially important question because the feasibility of the complete receiver concept was strongly dependent on it. A breadboard model of the frequency synthesizer has been constructed and tested in several ways. Extensive testing has been done to determine the severity of the phase noise in the output and the susceptibility to extraneous modulation by power supply ripple and noise.

2.7.2 Conclusions and Recommendations

The major conclusion reached in this study is that the digital synthesizer designed and tested in this program can operate satisfactorily to perform the intended function. There are yet some unanswered questions regarding phase

noise, but the breadboard model operated with an output phase noise equivalent to about 2.5° rms. This phase noise was measured using an Apollo Block II transmitter with the synthesizer and measuring the output noise modulation in the Block II STE receiver using the 21 Hz $2B_L$ bandwidth.

The most significant problems are (1) the sensitivity of the digital circuits to power supply noise and ripple, and (2) the rather large power consumption of the digital circuits.

To continue development of this concept in coherent transponders, it is recommended that further work be done to determine the best way of minimizing the sensitivity to interference from power lines and strong magnetic and electric fields. More study is also needed to determine the bandwidth and stability requirements of the 40.4 MHz bandpass filter. It was not possible with the time and manpower available in this study to determine the ultimate limitation of phase noise on the output.

Also, packaging of the flat-pack IC's is not really optimized. This is a type of circuit which must use both IC and discrete components, and in such cases, the flat-pack style package is little better than the TO-5 can. The really attractive concept is to separate the digital circuitry into three groups of IC's, procure the IC's as chips, and put them in TO-8 packages with about 7 chips per package. This technique undoubtedly offers significant improvements in size, power consumption and higher frequency capability. Its cost, of course, is a little higher (at least the R&D cost).

This type of synthesizer is readily adaptable to other transponder ratios and only minor changes are required to convert the design to a new ratio. For detailed discussion on this matter, see paragraph 2.3.

2.7.3 Summary of Results

The following data was measured on the breadboard frequency synthesizer. It represents typical measurements made under laboratory ambient conditions.

1. Power Consumption

Mixer and divide by 26 module	.92 watt
Detector, Divide by 17 and divide by 15 module	1.7 watts
Synthesizer Output Oscillator	.15 watt

2. Output Noise ($2B_L$ = 21 Hz, STE Receiver) — 2.5° rms at S-band

3. Output tracking or lock-in range — ±12 kHz minimum

4. Output Power Level (7.5F1) — +1.5 dbm

5. Spurious signals on 7.5F1 output

Frequency	db from desired
7.5F1	0 (ref)
7.5F1/4	-55
7.5F1/2	-44
7.5F1 (3/4)	-72
7.5F1 (5/4)	-65
7.5F1 (3/2)	-55
7.5F1 (7/4)	-64

6. Spurious emissions from input terminals

F2/2 terminal: -53 dbm at 39.6 MHz $\left(\frac{17F1}{4} - \frac{F2}{52}\right)$, others < -70 dbm

$\frac{17F1}{4} - \frac{F2}{52}$ terminal: all < -70 dbm

7. Power line conducted interference

		Signal in Microvolts
Approximate Frequency (MHz)	-6 Vdc	-10 vdc (phase detector power supply)
8.0		50
12.0		230

Approximate Frequency (MHz)	-6 Vdc	Signal in Microvolts -10 Vdc (phase detector power supply)
16.6	30	30
19.0	30	30
36.0 (15F1/4)		400
45.0 (F2)	25	
54.0 (45F1/8)		100
72.0 (7.5F1)	30	
108.0 (45F1/4)	30	

All others $< 25\ \mu v$

8. Output phase locked loop 3 db bandwidth: 2100 Hz

9. Acquisition time (average of 10 tries): 7 milliseconds

2.7.4 Description of Breadboard Synthesizer

2.7.4.1 Functional Requirements

The frequency synthesizer is required to accept two input signals from the receiver and from these signals generate an output to provide coherent excitation to the transmitter. The receiver, synthesizer, and transmitter are the major elements of the Advanced S-Band Transponder. The synthesizer inputs, as can be seen in the block diagram of figure 2-61 are

$$\frac{17F1}{4} - \frac{F2}{52} \text{ and } \frac{F2}{2}.$$

F1 is, by definition, the received r-f carrier frequency divided by 221. F2 is the exact receiver i-f frequency, nominally 45.0 MHz. By study of the block diagram it will be seen that the synthesizer processes and combines the input signals in such a way as to generate an output signal at 7.5F1. The 7.5F1 output is then used to drive the associated transmitter which includes a X32 frequency multiplication. Since the received signal is an exact harmonic of F1, the transmitter output is then coherent with the received signal. The Transmit/Receive ratio is 240/221.

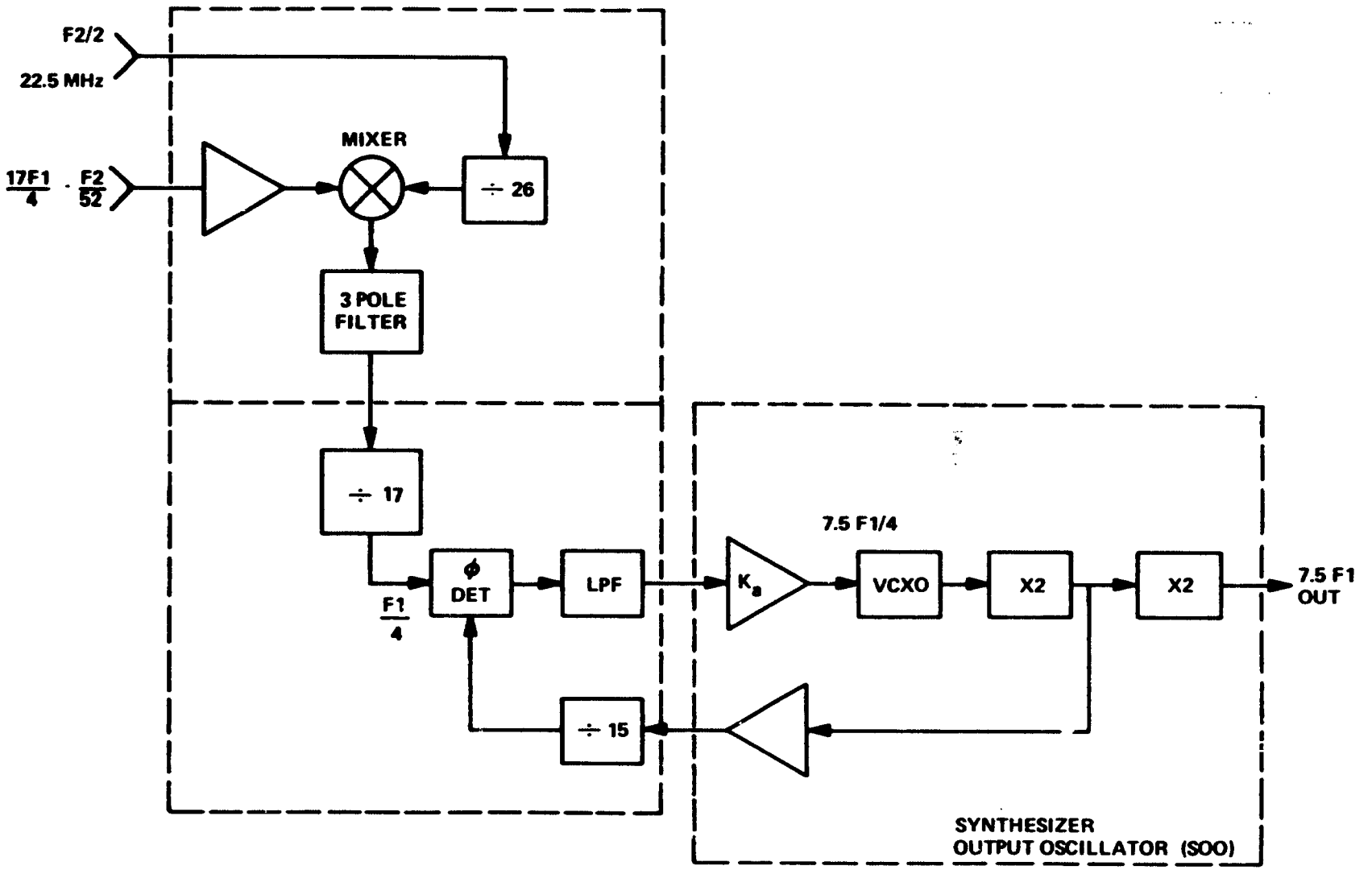


Figure 2-61. Frequency Synthesizer Block Diagram

The frequency synthesizer used in this application has in some cases been referred to as a synchronizer because it serves to synchronize the transmitter with the receiver.

The schematic diagram of the frequency synthesizer mixer and phase detector modules is shown in figure 2-62. It can be seen that the circuitry is almost entirely digital. It uses a total of 22 monolithic integrated circuits. The Synthesizer Output oscillator uses essentially discrete components. No attempt was made in this program to utilize IC techniques in the output oscillator. It is presumed that some simplification could reasonably be made in the circuitry so that in an engineering model, it could be conveniently put in a 2 x 4 x .5 inch module. Such a design would probably use some hybrid circuitry. The circuitry used in the output oscillator module can be considered somewhat as test equipment needed to test the synthesizer.

2.7.4.2 Digital Circuits

The digital circuits are constructed of Motorola MECL II monolithic integrated circuits. The basic gate of this family has a 4.0 ns propagation delay. The MC1213 J-K flip-flop is the key device for use in frequency dividers. It is specified for operation up to at least 70 MHz. A higher power series is also available (MECL III) in which the basic gate delay is 2 ns, the J-K flip-flop has a maximum speed of 120 MHz, and the power dissipation is doubled.

No attempt is made here to describe the theory of the frequency dividers used in the circuit. A review of the MECL II data sheets, included in paragraph 2.7.6, should be sufficient to guide the reader to an understanding of the circuits to any depth desired.

The frequency dividers are "clocked" rather than "ripple-through" type. This type of design generally requires more components, but almost completely eliminates the accumulation of phase jitter in passing through the counter.

The balanced mixer consists of two NOR gates driven in push-pull. This provides an excellent, simple, small, wideband mixer. Of course, the output is not linear with respect to either input when the normal level signals are used. The output signal was measured to have approximately 27 db attenuation of both input signals with respect to either output sideband.

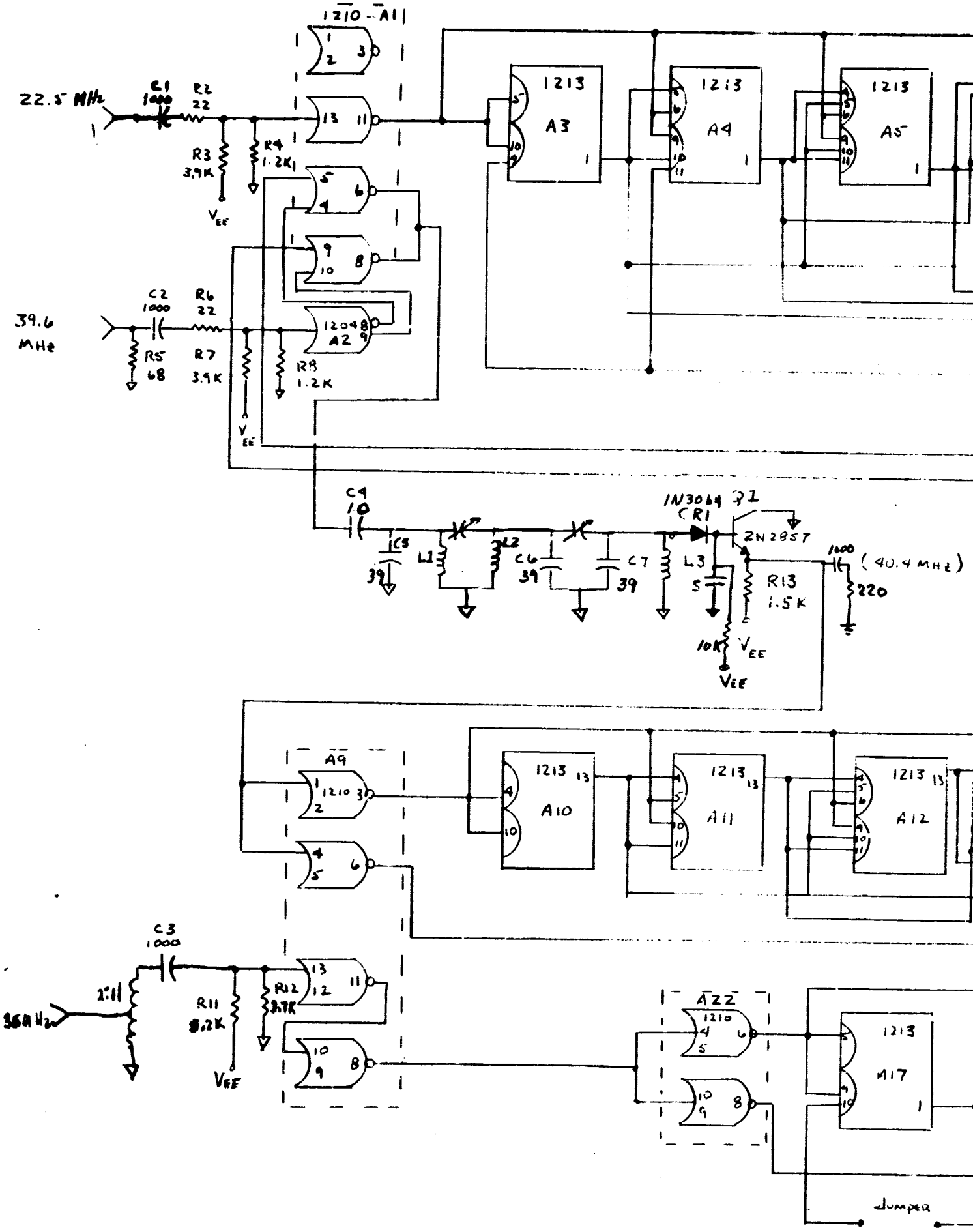
In the original concept of the synthesizer it was planned to use two balanced mixers of this type, with appropriate phasing, to generate the desired output sideband with little or no filtering. This was referred to as a digital converter. The digital converter was tested and it worked--somewhat. The unwanted sideband and the carrier were suppressed by 25 to 30 db as anticipated, but other spurious were not. The higher order products were suppressed on the wrong side.

The following tabulation shows what happened.

$f_1 + f_2$	enhanced as desired
$f_1 - f_2$	suppressed as desired
$3f_1 - 3f_2$	enhanced (surprise)
$3f_1 + 3f_2$	suppressed (surprise, but okay)
$5f_1 - 5f_2$	suppressed
$5f_1 + 5f_2$	enhanced

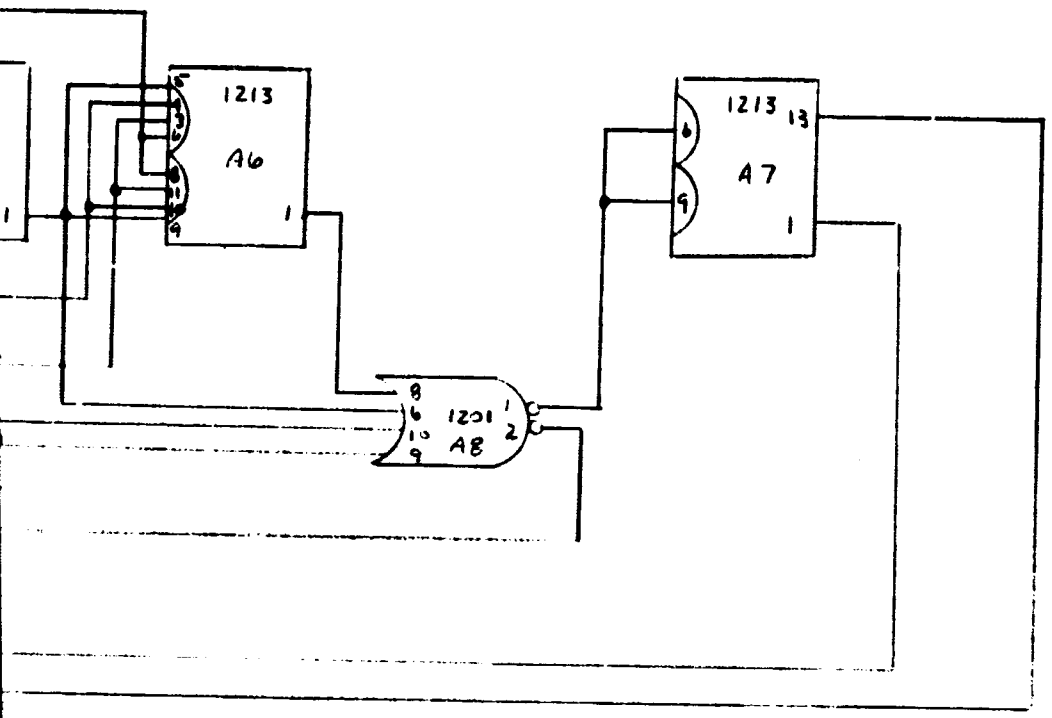
After observing such conditions on the spectrum analyzer, it took only a brief look at the trigonometric expansion to see that this could have been predicted. Having gone this far, it was interesting to put the signal through the divide-by-17 circuit and observe the output. The output in this case was a disastrous noise spectrum. The noise peaked as expected at $(f_1 + f_2)/17$, and was at least 10% wide at the 3 db points. Figure 2-63 presents a rough idea of the results.

After seeing the results shown in figure 2-63, the reader will readily recognize that this is inadequate performance. However, before dismissing the technique completely it is interesting to contemplate the reasons for the extremely noisy



FOLDOUT FRAME 1

CUT-169



MHz)

V_{EE} = -6.0V NOMINAL

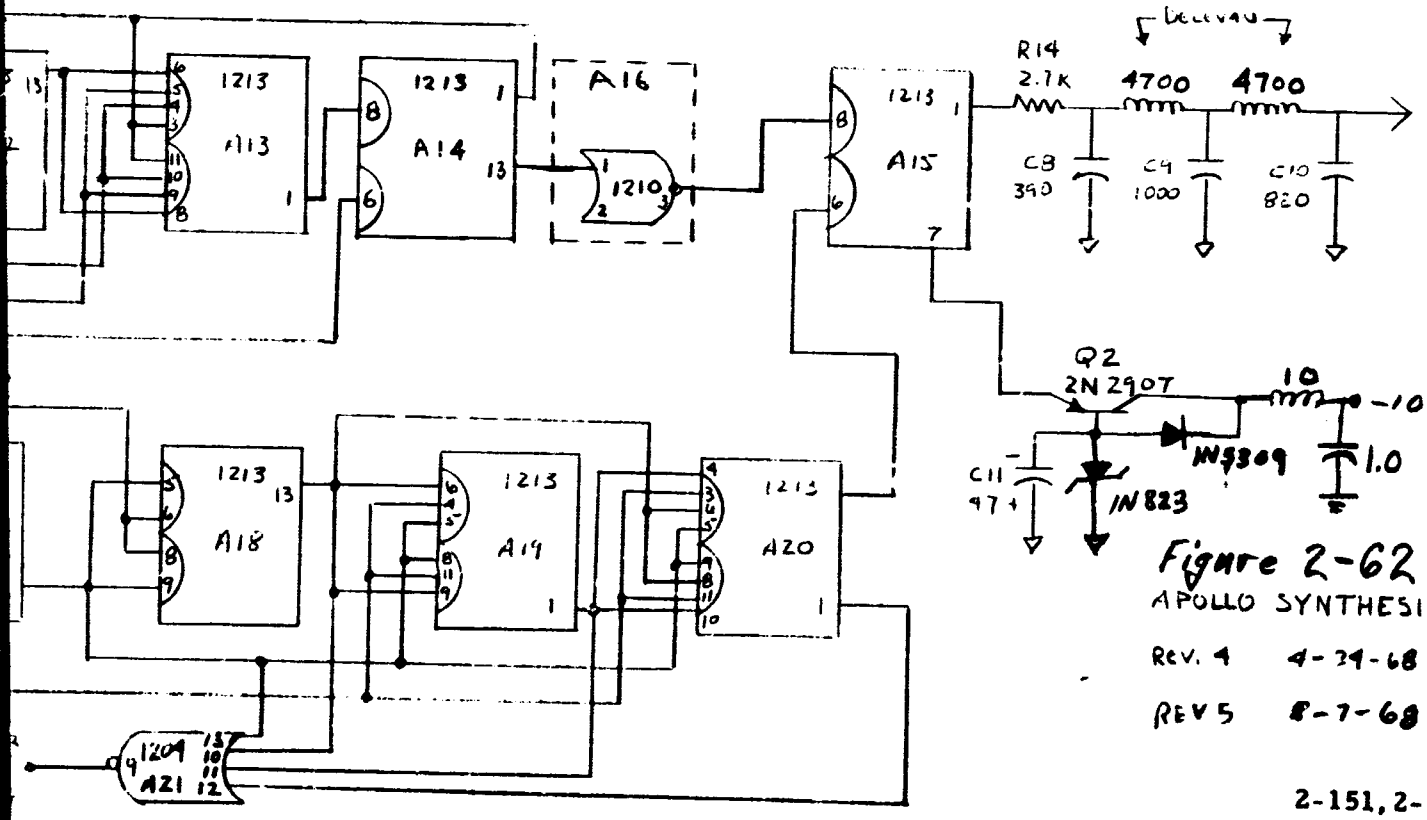


Figure 2-62
APOLLO SYNTHESIZER.
Rev. 4 4-29-68
REV 5 8-7-68 O.D.1.

2-151, 2-152

FOLDOUT FRAME 2

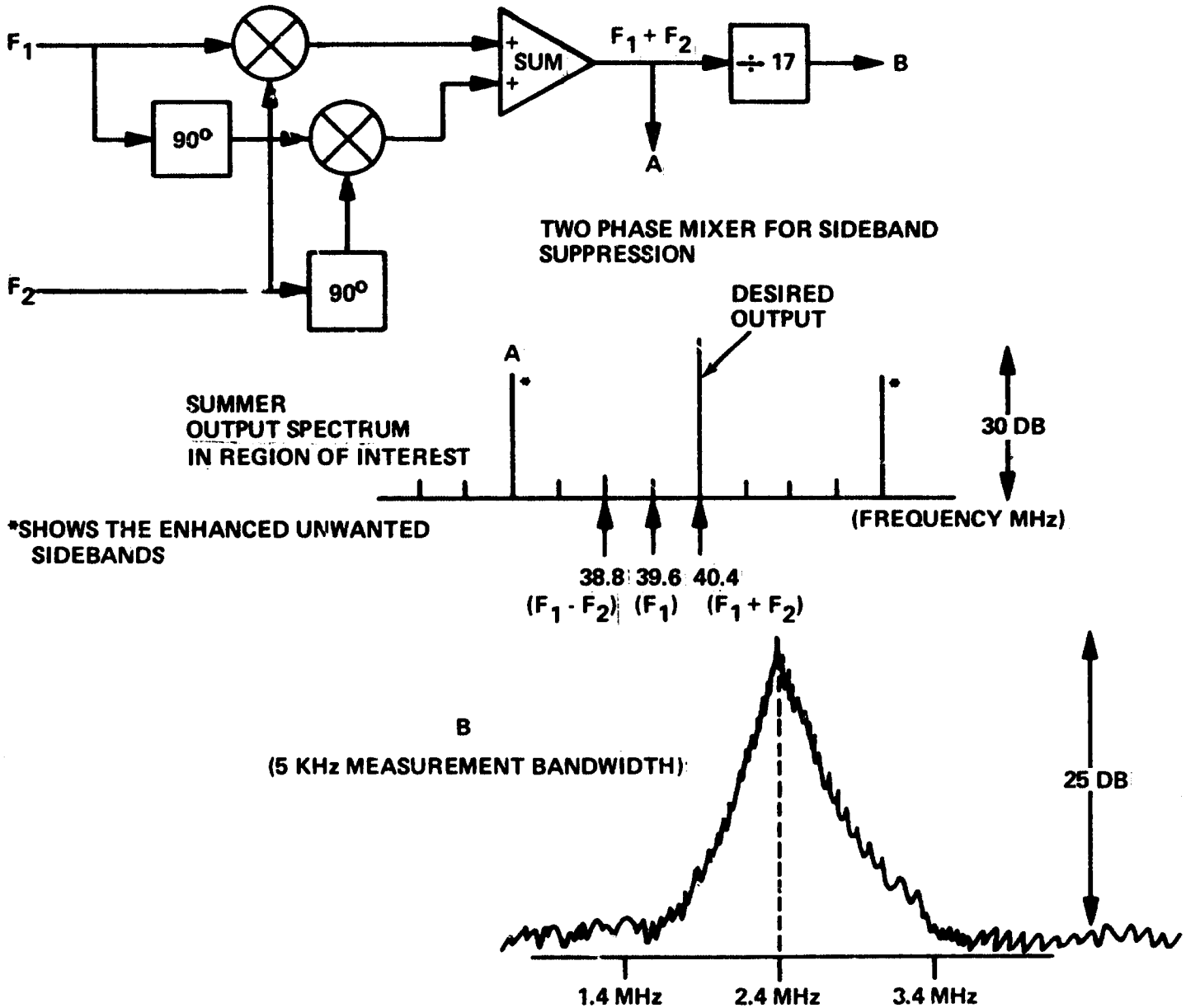


Figure 2-63. Results with 2-Phase Digital Mixer and ÷17

output. Certainly, a phase modulated signal could be put through the divider and no measurable degradation in S/N ratio would be observed. The problem is that the summer output contains much a-m. If digital devices had idealized off-on type outputs, with zero rise and fall time, then no a-m could exist, and only pm would be present. In such a case, the output S/N would not be degraded. However, such a condition is not obtainable and the existing a-m on the divider input is very sever.

In this program, it was concluded that the a-m could be reduced to an acceptable value only by extensive filtering and limiting. Then, it was obvious that a simple balanced mixer and a three pole filter would be a big improvement. Once the decision is made to include filter components, there is no longer any need for the added complexity of the two-phase mixer.

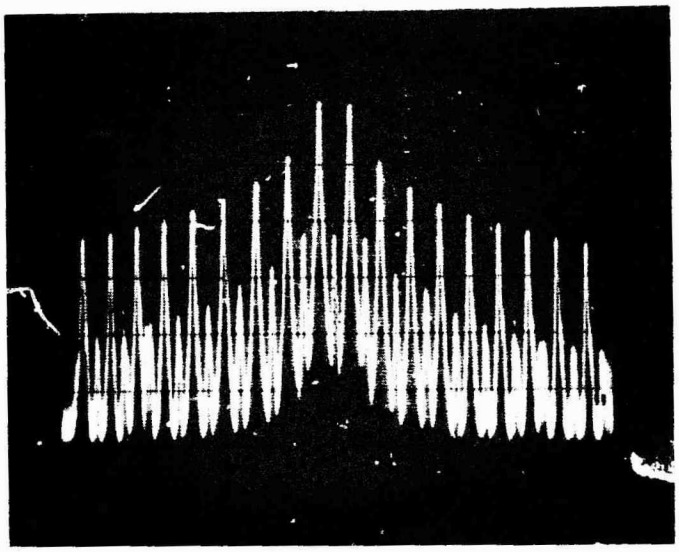
2.7.4.3 Bandpass Filter

The final circuit then, as shown on the schematic (figure 2-62) consists of the balanced mixer (2 NOR gates) and the three pole filter. The three pole filter is a rather narrow bandpass filter, being only about 1.5% wide at the 3 db points. Figure 2-64 shows the output spectrum of the mixer which drives the filter. Figures 2-65 and 2-66 show the measured frequency response and the output spectrum of the three pole filter.

It will be recognized that the output signal from the filter will contain some a-m. This is a normal condition to consider and further investigation of this is important. It is possible that detuning in this filter could be a serious limitation on the ultimate purity of the output signal because the a-m components in the output give rise to noise in the digital divider. Further investigation of this possibility is recommended as very important. It may, for example, be necessary to use a different type of filter or an ultra-stable design.

2.7.4.4 Synthesizer Output Oscillator

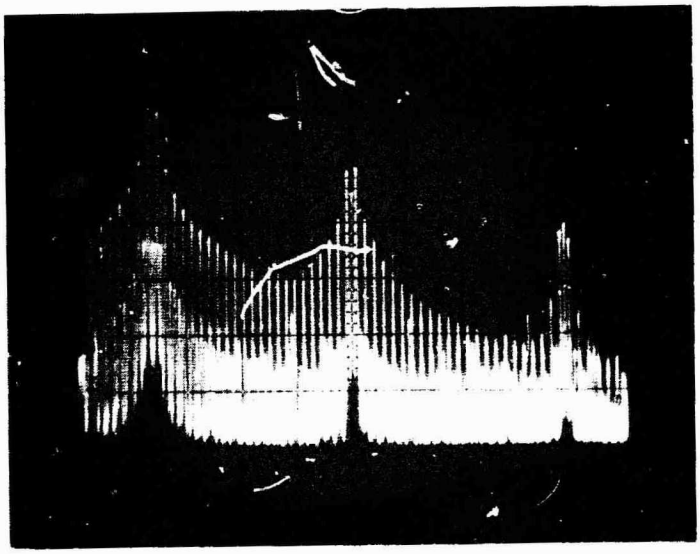
The voltage controlled oscillator and transistor frequency doublers are contained in a separate module referred to as the synthesizer output oscillator (SOO).



Vertical: 10 db/cm

Horizontal: 3 MHz/cm

100 kHz bandwidth



Vertical: 10 db/cm

Horizontal: 10 MHz/cm

100 kHz bandwidth

Figure 2-64. Mixer Output Spectrum

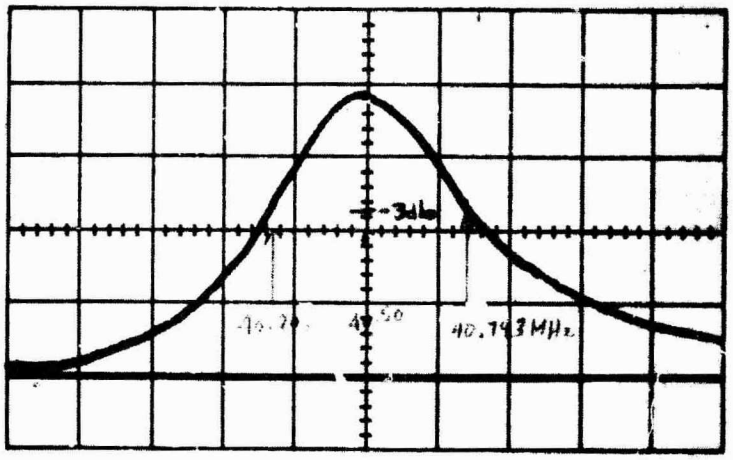
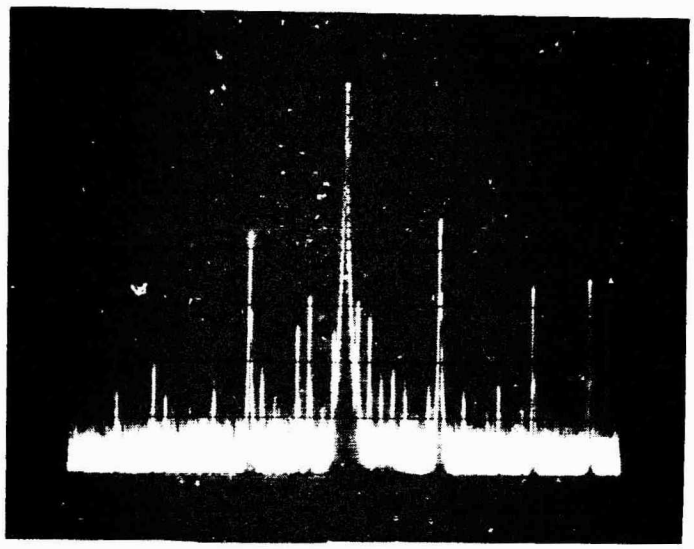


Figure 2-65. 17 F1/4 Bandpass Filter Response



Vertical: 10 db/cm

Horizontal: 1 MHz/cm

10 kHz bandwidth

Figure 2-66. 17 F1/4 Filter Output Spectrum

NOTES:

1. UNLESS OTHERWISE INDICATED:
   ALL RESISTORS ARE IN OHMS
   ALL CAPACITORS ARE IN PF
   ALL INDUCTORS ARE IN UH
   ALL VOLTAGES ARE DC.

2. NO. 28 T12-10.

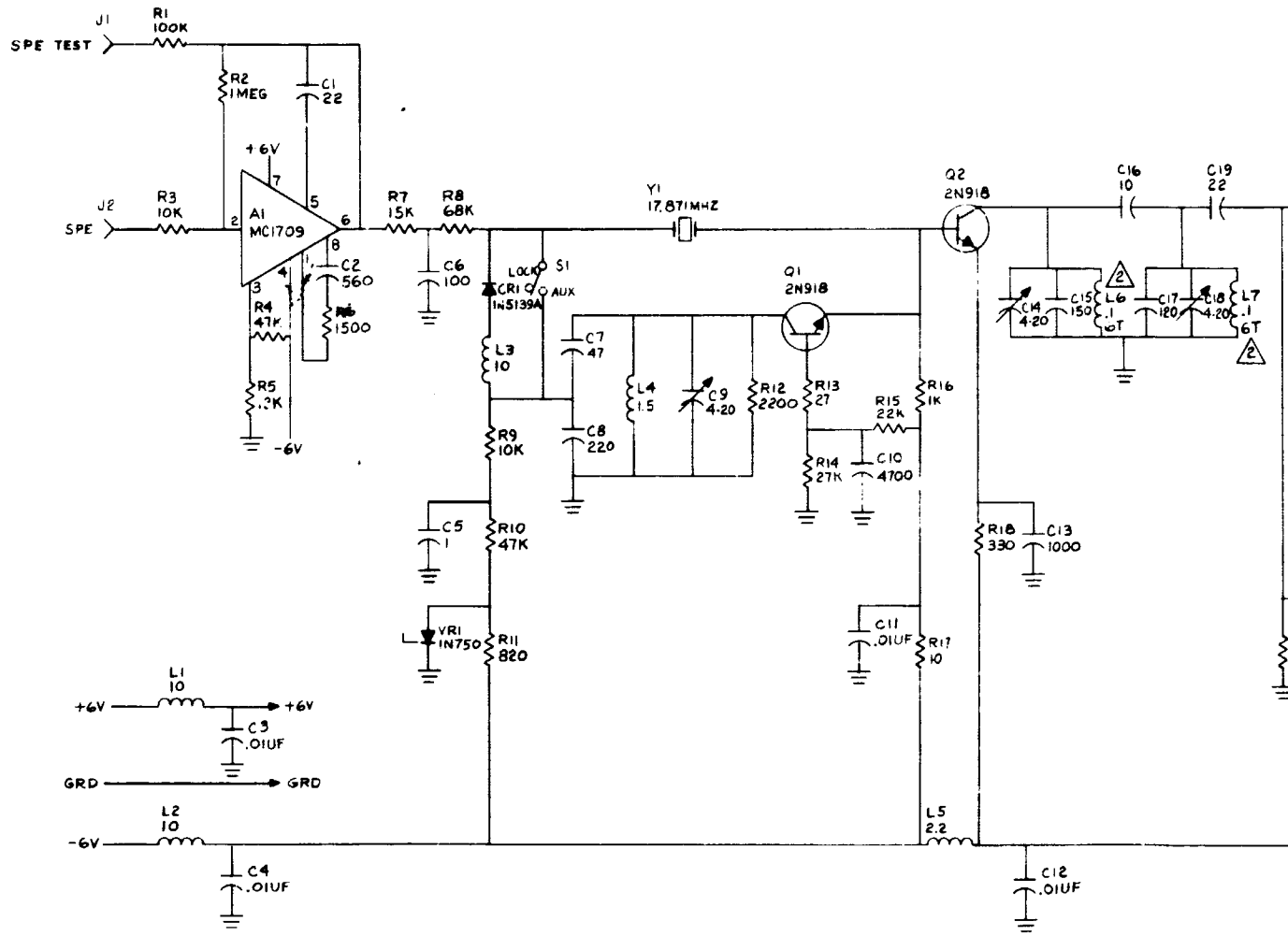
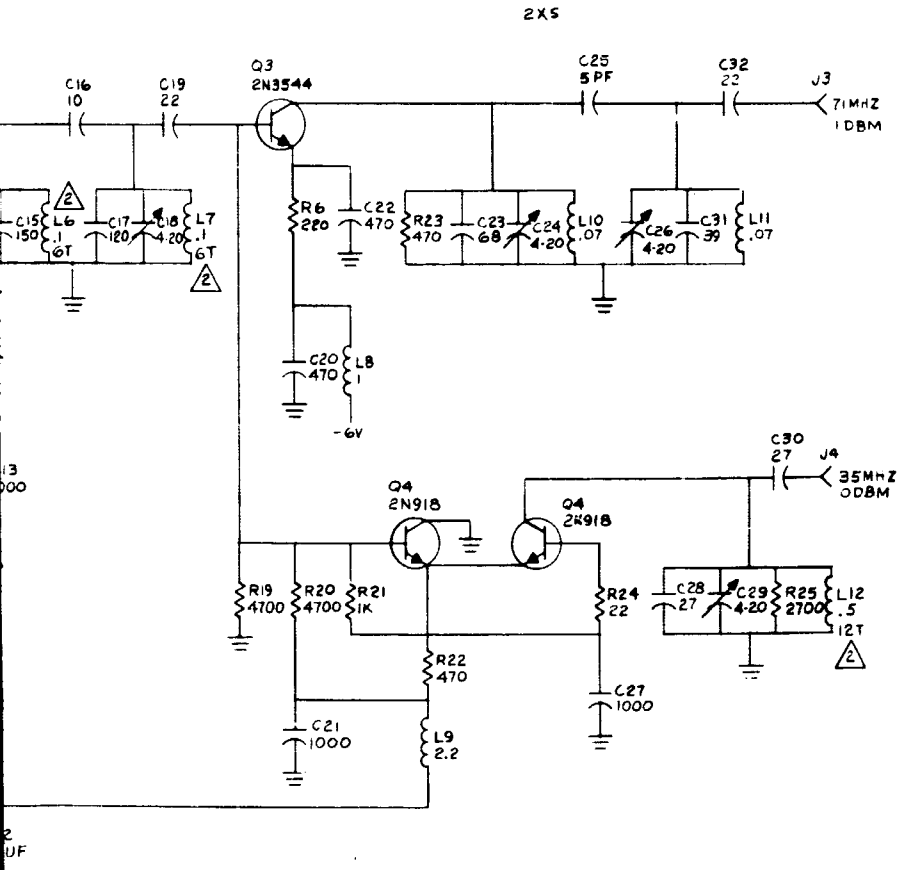


Figure 2-67. Synthesize
Transl ide

FOLDOUT FRAME 1



67. Synthesizer Output Oscillator Module, Advanced S-Band Transponder, Project 3433

2-157, 2-158

CUT-168

FOLDOUT FRAME 2

A schematic of this module is shown in figure 2-67. The oscillator is simiiar to the receiver vcxo. The control voltage is obtained from the digital phase detector discussed in the following paragraph. All discrete components are used in the SOO as no attempt was made at miniaturization. This module would possibly be contained as part of the transmitter in production systems since it contains the oscillator needed for excitation in the non-coherent mode. The toggle switch used to select coherent or non-coherent mode could be replaced by an electronic switch with a dc control voltage. The frequency of the oscillator is 7.5F1/4. A higher frequency oscillator, 7.5F1, was originally considered. However, a fifth overtone crystal is very "stiff" and it is impractical to obtain the required lock range. Therefore, the more practical design uses a fundamental mode crystal oscillator to provide adequate lock-in range.

The first doubler and buffer amplifier provide the 7.5F1/2 phase lock loop feedback signal. Another X2 is required to provide the 7.5F1 transmitter drive of +1.5 dbm. The 7.5F1/2 power output is -.5 dbm into a 50 ohm load. These two outputs have no spurious signals present greater than -50 dbm except the harmonics.

The vcxo sensitivity is approximately 1 kHz/volt measured at the test terminal. A dc amplifier is required to give the needed loop gain. Figure 2-68 shows the vcxo frequency deviation characteristics. Assuming the vcxo control voltage is allowed to swing between ± 4 volts, the capture range referred to the 39 MHz synthesizer input is near ± 6 kHz which is more than sufficient when considering the receiver vcxo sweep range involved.

2.7.4.5 Phase Lock Loop

The output circuit of the synthesizer can be considered to be a digital frequency multiplier which multiplies F1/4 by 30 to provide an output at 7.5F1. The multiplication is achieved by using a divide-by 15 circuit in the feedback loop of a phase locked oscillator. Figure 2-61 shows the operation of this loop rather clearly. The 7.5F1/2 signal is divided by 15 and compared with the output from the divide-by 17 circuit, using a digital phase detector. The digital phase detector is a

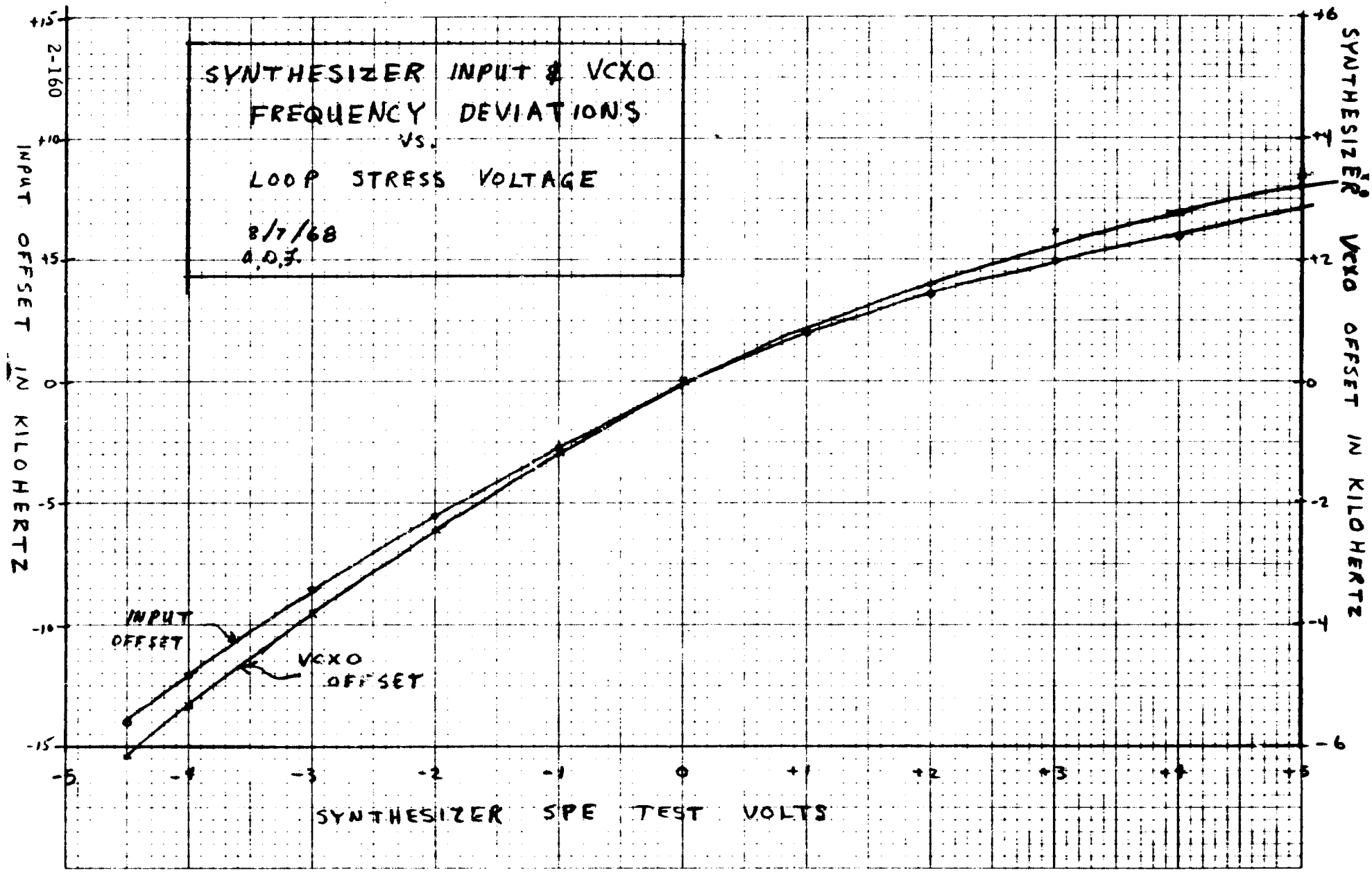


Figure 2-68. Synthesizer VCXO Characteristics

flip-flop which is triggered by the leading edges of the two signals being compared. The input frequency at the p'' se detector is F1/4.

The operation of the dig e detector can be easily understood by referring to the timing diagrams in fi -69. Figure 2-69(a) is a typical input to the $\overline{J}$ input and 2-69(b) is the $\overline{K}$ input to the flip flop. Propagation delays, rise times, and fall times are not depicted. The non-inverted output, Q, is shown in figure 2-69(c) for non-coherent input signals. As can be seen the output pulse width is proportional to the phase shift between the two input frequencies. Filtering the carrier frequency from the output will result in a dc component proportional to the phase shift between the two coherent input signals. This digital phase detector has a linear range of 320^{o} with a .9 volt peak-to-peak characteristics centered at -1.2 volts dc.

Figure 2-69(d) shows the detector characteristic obtained at the low pass filter output when the two input signals are noncoherent; the sawtooth frequency being the difference frequency. A problem occurred before using A16 of figure 2-62 as an inverter. The negative going transition of the filtered detector output (figure 2-69 (d)) had a peculiar breakup. The exact cause is obscure, but it is related to pulse width and shape. With the inverter in place, only a slight and probably insignificant step is present.

The loop filter is an LC low pass filter whose poles do not appreciably affect the loop characteristics other than reducing high frequency noise at the vcxo input. The closed loop response is then a simple one pole filter. The bandwidth of the loop is determined by the loop gain constants. The cutoff frequency equals $2 K_d K_v K_a / 15$ where K_d is the detector gain ($\cong 1/2\pi$ volt/rad), K_v is the vcxo gain ($\cong$ 6280 rad/sec/volt), and K_a is the dc amplifier gain. Using a dc amplifier gain of 100, the 3 db loop bandwidth should be 2200 Hz. This was chosen as a nominal value such that its influence on the overall receiver narrow band phase response is negligible. The question arose later as to why this bandwidth cannot be reduced significantly. This would provide much better filtering of the coherent output signal while the low

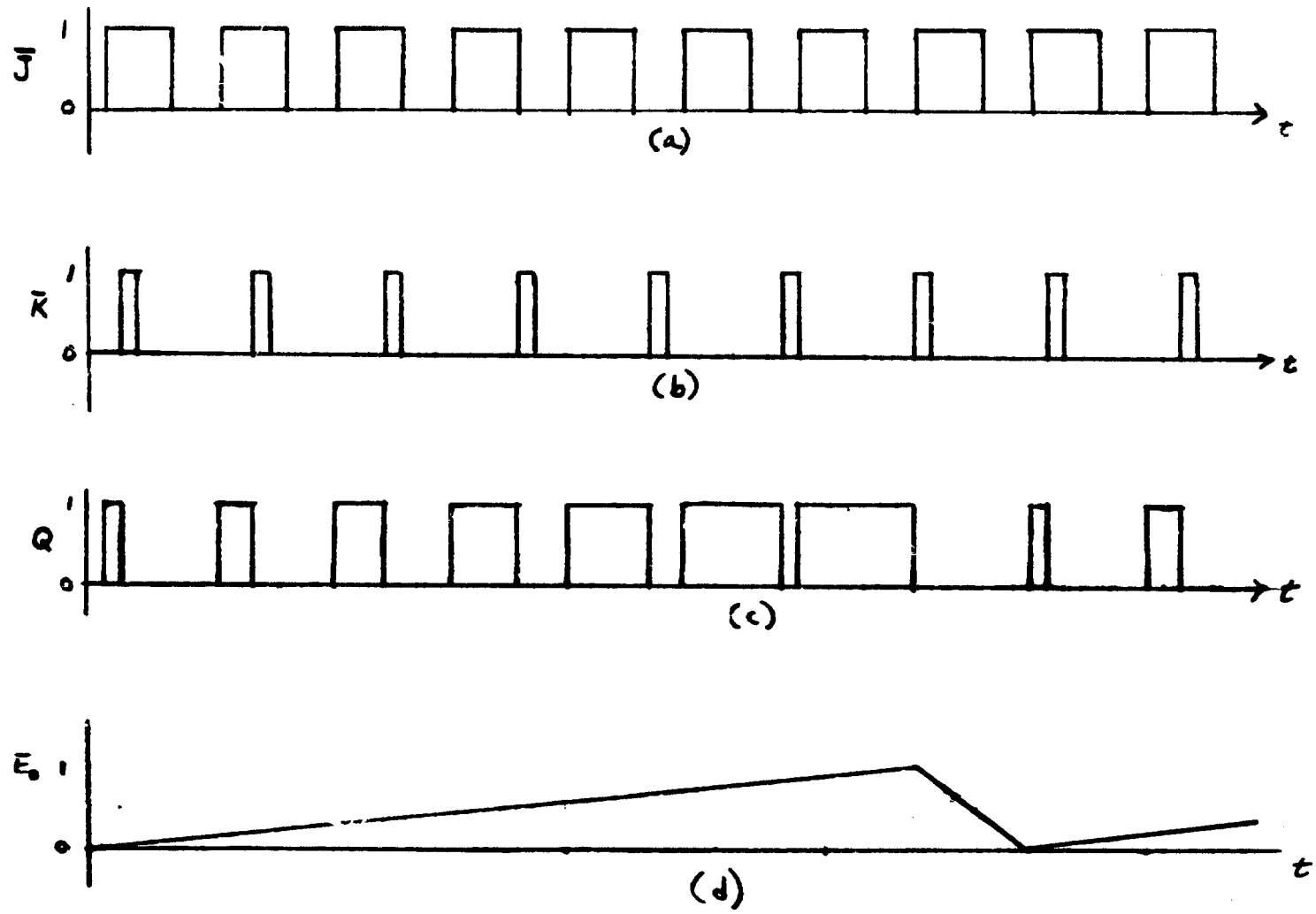


Figure 2-69. Digital Phase Detector Waveforms

frequency modulation information is not used anyway. Figure 2-70 shows the measured H(s) response for the closed loop. The measured 3 db bandwidth of 2100 Hz agrees well with the calculated value. The second curve shown in figure 2-70 is the loop response with the dc amplifier gain reduced to 10. The bandwidth is reduced almost by a factor of 10 as predicted.

Reducing the loop bandwidth involves reducing loop gain. The easiest adjustment here is the dc amplifier gain. It must be determined what effect this low gain has on the synthesizer lock-in range. If the receiver vcxo sweeps the range ± 1 kHz at 19.8 MHz, the synthesizer vcxo must cover the range, ± 1 kHz (17.9/19.8) = ± 900 Hz centered at 17.9 MHz. This will require ± 1 volt to shift the vcxo. Since the phase detector range is $\pm .5$ volt, a dc gain of at least 2 is required. This means a loop bandwidth of 44 Hz could be used.

It is interesting to note the dynamic phase error range which this phase lock loop will tolerate and still remain linear. The phase error for a ramp frequency input is $\Delta\omega/K^5$ where $K = K_a \cdot K_v \cdot K_d$. Since a divider is used before detection, the input phase error can be 17 times that normally tolerable. Also, the sawtooth phase detector has a linear range of almost 2π radians which is twice that of a sine wave detector. Therefore, 34 times more phase error can be present at the synthesizer input than could normally be tolerated without dividers. Assuming $\Delta\omega = 2\pi$ (4000) rad/sec preceding the divider, the minimum loop gain needed is 235 sec^{-1}. The chosen loop gain is 1.33×10^4 sec^{-1}. With this loop gain the maximum phase error will be .11 radian or 6.3^o. Clearly, the synthesizer is no limitation on receiver acquisition.

The reader will note that there are other means of performing the F1/4 to 7.5F1 multiplication which might possibly have advantages over the method used. It is agreed that such is the case, and some consideration should be given to other methods. In fact, further investigation of this part of the problem could probably lead to several improvements for specific design goals.

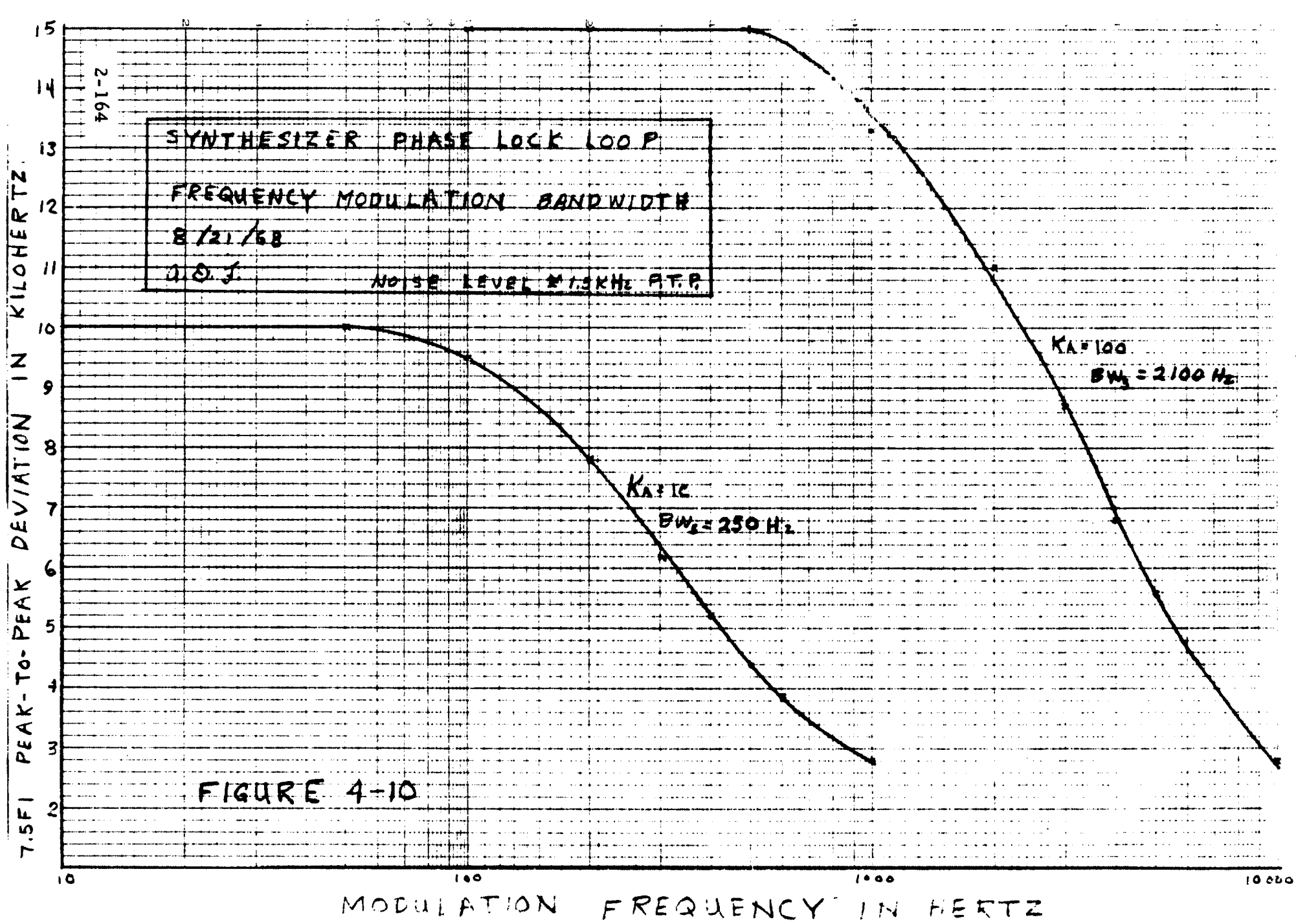


Figure 2-70. Synthesizer Phase Lock Loop Frequency Modulation Bandwidth

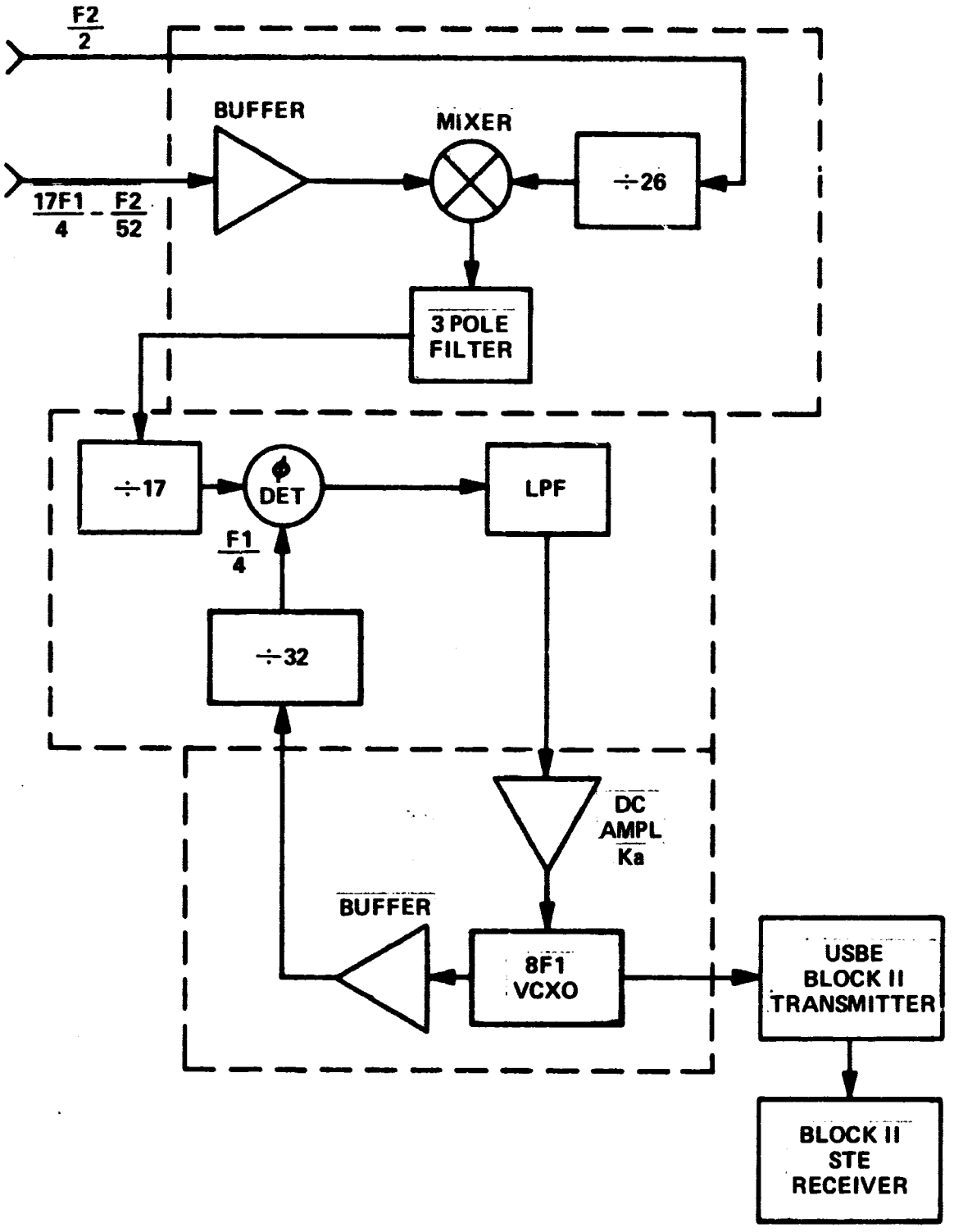


Figure 2-71. Phase Noise Test Setup

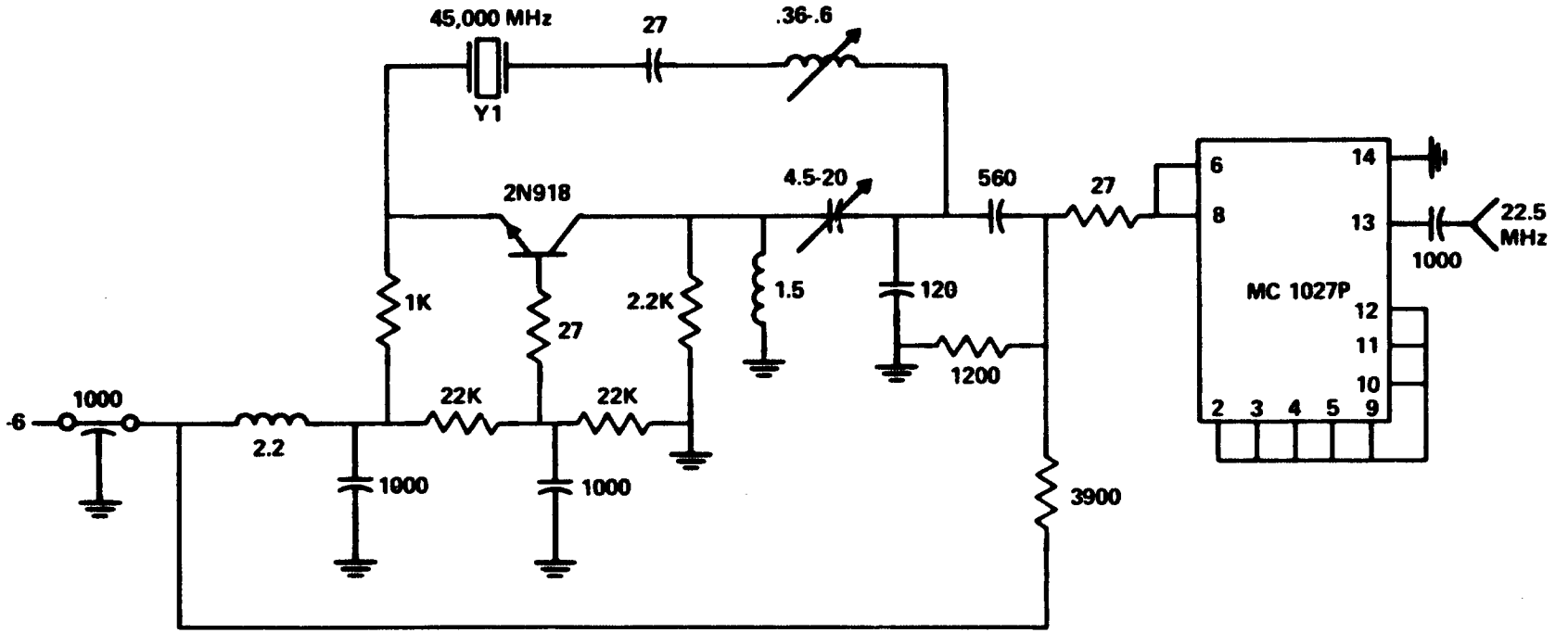


Figure 2-72. 45 MHz Test Crystal Oscillator and ÷2

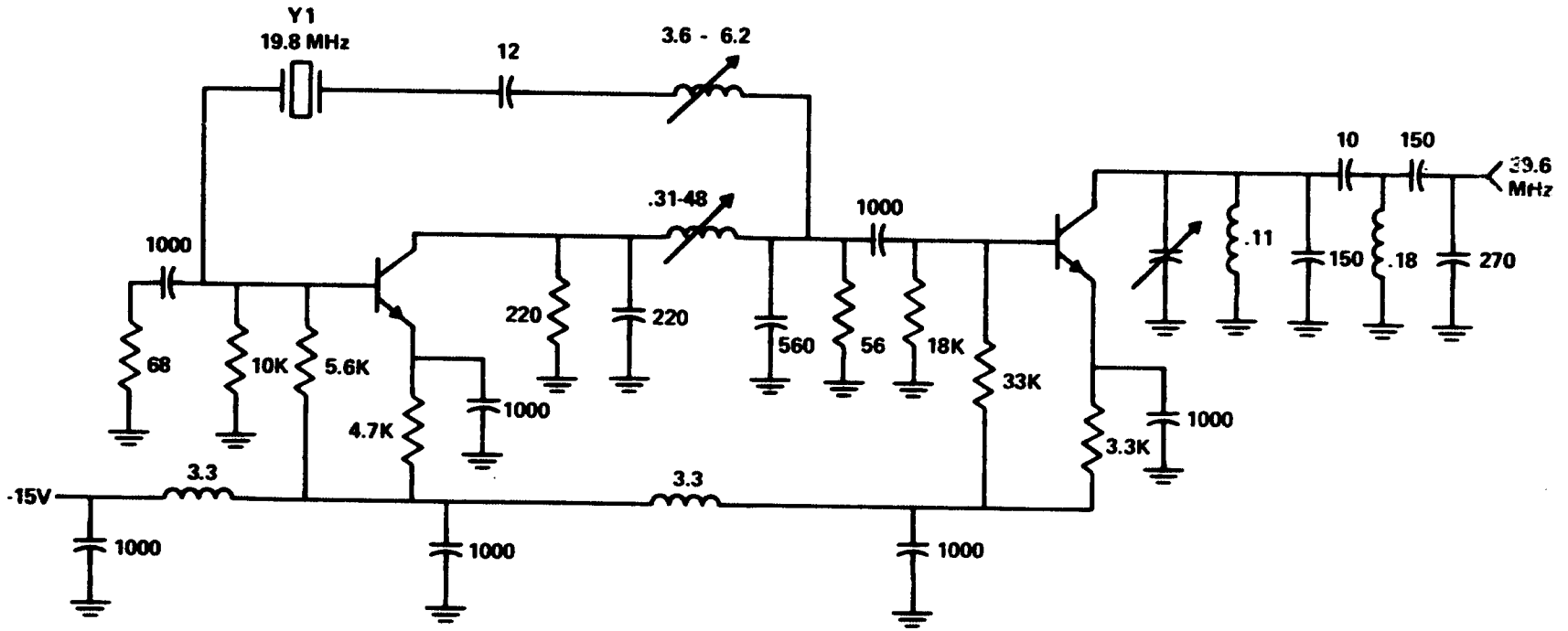


Figure 2-73. 19.8 MHz Xtal Oscillator and X2

It is generally recognized that a phase lock multiplier may be made by comparing the fundamental frequency and the desired harmonic directly in the phase detector. In this case, the divider could be eliminated by application of this technique. (Such a multiplier in earlier days has been called an "Impulse Governed Oscillator", abbreviated IGO.) This technique was considered here, and no doubt would work to some extent. It was not pursued, however, for the following reasons:

1. Phase noise was potentially a serious limitation, and it was felt that the IGO might be worse in this respect.

2. Since the IC divider is so simple and reliable, it is questionable that the IGO would be simpler, even though it would almost certainly consume less power. Additional filter requirements and higher dc gain with more restrictions of stability and bandwidth apply to the IGO system.

2.7.4.6 Noise Tests

The digital circuits involved in the synthesizer were found to be particularly susceptible to audio interference on the power lines. It was found that most sensitivity was due to the phase detector which, at the time of this test, was not fed by a separate regulated power supply as shown in figure 2-62. The test setup used for measurement of phase noise is shown in figure 2-71. Only a Block II transmitter was available which requires 8F1 coherent drive instead of 7.5F1 so a few minor modifications had to be made in the synthesizer. The vcxo used the fifth overtone 8F1 crystal and the divide by 15 is changed to divide by 32. This divider change is simple in that a single divide by 2 flip-flop was added along with one wire change to make the divide by 15 a divide by 16.

Typical data at 100 Hz interference frequency shows 3.8° rms noise at S-band for 17 mv modulating the -6 V power supply while the phase detector is fed from a separate unmodulated supply. The receiver noise bandwidth, $2B_L$, is 21 Hz. Modulation of .6 mv applied to only the phase detector supply causes 20° phase noise. This indicates the need for a low frequency filtering of the phase detector supply. Phase noise without modulation is $\cong 2.5^{\circ}$ rms.

The series regulator shown in figure 2-62 was incorporated to supply the phase detector flip-flop from a well filtered supply. A field effect constant current diode is used to bias the zener diode. This technique allows an improvement of 100:1 or better in sensitivity due to the high dynamic impedance of the current regulator diode.

With the synthesizer corresponding exactly to the schematic in figure 2-62, the phase noise was measured while modulating the power lines again with a 21 Hz STE receiver bandwidth. For this test, the mating transmitter was available so a 7.5F1 drive could be used.

With modulation on the -6 V line, a level of 100 millivolts caused 21° phase noise. Applying the 100 Hz signal to the -10 volt line (phase detector), a level of 125 mv resulted in 5° phase noise at S-band. The residual noise level is 4° rms. This is clearly an improvement over the previous test results. The previous tests on the -6 V line incorporated extensive audio filtering and explains, along with the modulation levels, why the noise previously was only 3.8°. This does mean that audio filtering is required which is not presently being used.

The phase noise reading on the STE receiver with a 400 Hz $2B_L$ is 3.0° compared to 4° with the 21 Hz bandwidth. Also, the phase noise without the test transponder is 2.5° rms with 21 Hz bandwidth. These results indicate that about 1.5° rms phase noise is due to the transponder and consists mainly of components above 200 Hz. These higher frequency components of noise are probably due to the synthesizer. It is anticipated that phase noise can be reduced to a level which will allow satisfactory transponder operation under all typical test conditions.

2.7.4.7 Packaging

A choice had to be made as to whether flat pack IC's or T0-5 cans were to be used based on which occupied less space. It turns out that there is little difference when discrete components also have to be added. It was decided to lay out the 2" x 4" printed wiring board so as to mount IC's on both sides with interconnections

made using plated through holes. Flat packs were chosen to give at least one side a low profile with discrete components mounted on one side only.

2.7.5 Special Test Circuits

The synthesizer inputs from the receiver come from the vcxo and Reference Oscillator circuits. These signals are contained in two separate modules. Since these modules were not available throughout the synthesizer development, special test boxes were built to supply these two needed signals at their exact frequencies. This eliminates the need for two bulky signal generators whose frequencies would have to be continually monitored.

Figure 2-72 shows the F2/2 generator which consists of a 45 MHz oscillator and a digital divide-by-two. This circuitry is similar to that actually used in the detector-reference generator module of this receiver. Figure 2-73 is the schematic of a crystal oscillator at 19.8 MHz which is the receiver vcxo center frequency. Following the oscillator is a X2 multiplier which gives the required nominal 17F1/4 - F2/52.

2.7.6 Digital Divider Phase Noise Investigation

2.7.6.1 Introduction

For various reasons, it may be desirable to incorporate one or more digital frequency dividers into the frequency synthesizing system of phase locked transponders. Consequently it is important to determine whether such a divider can be used without significant degradation of the phase noise in the system. This section describes an experiment which was performed in order to evaluate the digital divider in such an application.

The method used to evaluate the noise contribution of the divider is illustrated in the block diagrams of figures 2-74 and 2-75. The dashed line of figure 2-74 represents the electrical configuration for the first part of the test. In this step, the phase noise from the SGLS receiver vco module is measured and is used as a reference reading. The solid line connections represent the second half of the test.

Here the frequency divider in question is included between the SGLS vco and the phase noise test fixture (PNTF). This noise measurement can then be compared with the results of part one to determine whether or not the noise contribution of the frequency divider is significant. Figure 2-75 shows a block diagram of the PNTF.

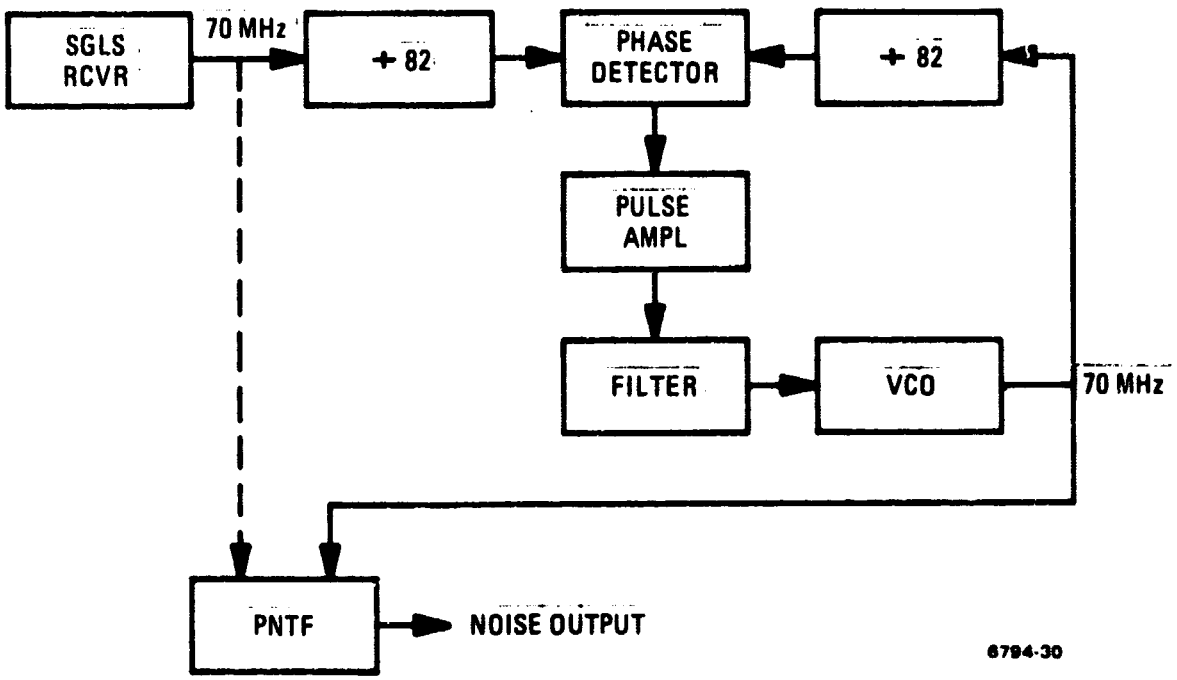


Figure 2-74. Divider Phase Noise Test Setup

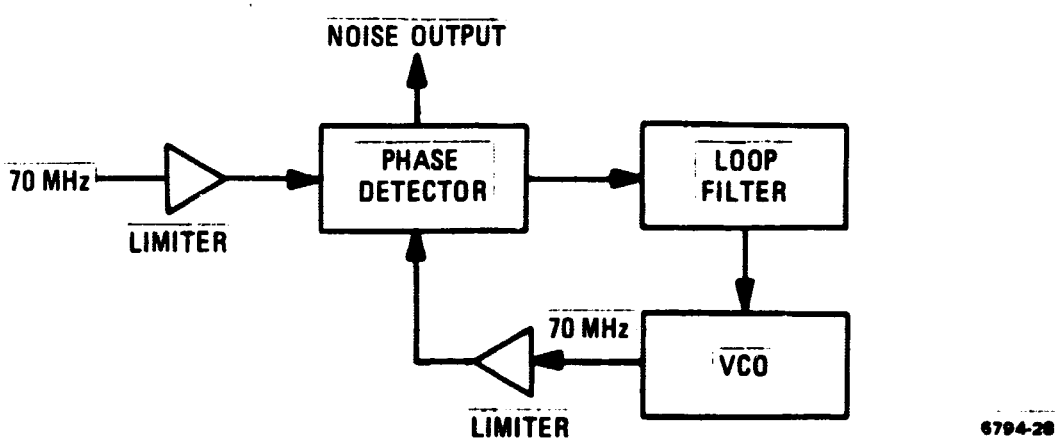


Figure 2-75. Phase Noise Test Fixture

2.7.6.2 Conclusion

The digital frequency divider can be used as described in the introduction with no significant degradation of the system phase noise.

2.7.6.3 Results

Table 2-7. Part One: Dashed Line Configuration of figure 2-74

Test Condition	Total rms Noise Voltage
1. SGLS vco Connected directly to the Phase Noise Test Fixture 2. $2B_L$ bandwidth set to 42 Hz position on the PNTF loop filter	20 mv

Table 2-8. Part Two: Solid Line Configuration of figure 2-74

		rms Noise Voltage				
			Frequency Components			
	Test No. Test Conditions	Total	60	120	180	300
I.	1. System bandwidth = 1560 Hz 2. $2B_L$ BW of PNTF = 42 Hz 3. Bench power supplies 4. Using vcxo	120 mv	80 mv	15 mv	80 mv	30 mv
II.	1. Same as above. except that a battery is used for the pulse amplifier	25 mv	10 mv	1.5 mv	6.5 mv	.1 mv
III.	1. Same as I, except that both the pulse amplifier and the divider use a battery	20 mv	4 mv	1.5 mv	3.5 mv	
IV.	1. Same as III, except using LC vco and bandwidth = 975 Hz	20 mv	5 mv		3.0 mv	2.5 mv

Test Equipment Used

1. B & K 2409 VTVM (True rms voltmeter)
2. HP 302A Wave Analyzer
3. Tektronix 541 Scope
4. SGLS Phase Noise Test Fixture (S/N 01-21341L)

2.7.6.4 Circuit Descriptions

Frequency Divider

The divide-by-82 circuits of figure 2-74 is comprised of a divide-by-two circuit followed by a divide-by-41 circuit.

The divide-by-two is simply a MECL MC1027 JK flip flop.

Divide-by-41

The circuit diagram of figure 2-76 shows the configuration used, including the feedback function. Also shown is the method used to provide a synchronous clock to all six stages. The configuration for this type of divider or counter is to have each stage driven from each of the preceding stages in addition to the synchronous clock. From this it is evident that the fifth and sixth stages would require five and six inputs, respectively. However, the flip flops used have only four $\overline{J}$ and four $\overline{K}$ inputs which provide a maximum of four clocked inputs per stage (i.e., $\overline{J}$ tied to $\overline{K}$). By "or"ing the outputs of the first three stages, as shown in figure 2-74, this problem is overcome.

The circuit counts until the Q output of each stage is zero. This state is detected by the six input NOR gate (MC 1001) at which time the NOR output goes to the logic 1 state. This output is then applied to the $\overline{J}$ inputs of stages B, D, E and F to inhibit their change of state. This effectively jumps the counter ahead by 23 states resulting in a 41 counter (64-23 = 41).

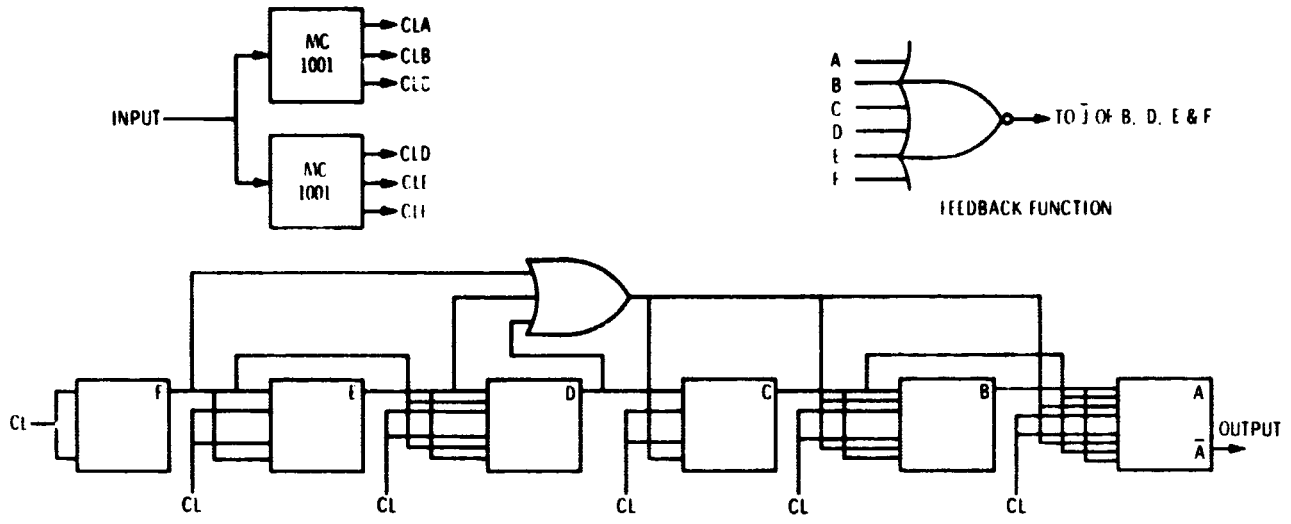


Figure 2-76. Divide-by-41 Circuit Diagram

The maximum frequency to which the divide-by-41 circuit will operate is 50 MHz at this time. The primary limiting factor is the accumulated propagation delay. The propagation delay of both the MC1001 and the MC1027 is four to six nanoseconds. Since the flip flops are synchronously clocked only one delay time is contributed by them and the six-input nor gate of the feedback function adds another. The delay could be as mcuh as 12 ns not including effects of circuit layout (i. e. lead length and stray capacitance). One further factor adds approximately 5 ns and that is the frequency limitation of 100 MHz for the MC1027. This means that there is approximately 5 ns delay in the input circuit of the J-K flip flop before it can respond to a data change at its inputs. The total time of the delays and the frequency limitation approaches the period of a 50 MHz input signal.

Digital Phase Detector

The phase detector of figure 2-74 is a digital type employing an MC1027 JK flip-flop. The $\overline{A}$ output of one of the divide-by-82 circuits is fed to the $\overline{J}$ input of the phase detector while the $\overline{A}$ output of the other divider of figure 2-74 is fed to the $\overline{K}$ input. The output is a square wave, the duty cycle (and therefore the dc valve) of which is a function of the relative phase of the two input signals. A pulse amplifier follows the phase detector. Its function is to amplify and limit the phase detector output, thus eliminating any ripple voltage. This amplifier is followed by a filter which provides the dc voltage to the vco.

2.7.6.5 Loop Gain and Bandwidth

VCXO Circuit

The gain of the phase detector and pulse amplifier is

$$K_{\phi} = \frac{5V}{2\ \pi rad} = \frac{5V}{Hz}$$

The vcxo gain is

$$K_{vcxo} = 400\ Hz/_{V}$$

A (X4) multiplier in the vcxo, the divider and a dc amplifier introduces a factor of $\frac{4X100}{82}$.

$$K_{dc} = \left(\frac{400\ Hz}{V}\right)\left(\frac{5V}{Hz}\right)\left(\frac{4X100}{82}\right) = 9750$$

The loop frequency response drops at a rate of 6 $db/_{oct}$. Therefore, unity gain occurs at $\omega = 9750$ or $f = \frac{9750}{2\pi} = 1560$ Hz.

L-C VCO Circuit

$$K_{l\text{-}c\text{-}vco} = 100\ \frac{kHz}{V}$$

$$K_{dc} = \left(100\ \frac{kHz}{V}\right)\left(\frac{5V}{Hz}\right)\left(\frac{1}{82}\right) = 6,100$$

The use of an MC1023 high speed gate will be investigated since its delay is typically half that of the MC1001. Also, the frequency limitation described above is the reason the divide-by-two precedes the divide-by-41 circuits.

Phase Noise in the Frequency Divider

Phase noise results from a random variation in the position of the leading edge of the divider's output pulse. This variation in the pulse position is due to noise voltage which causes the output level of the pulse to vary. The amount of ripple that can be tolerated is calculated below.

Assuming that the phase noise contribution at 2 GHz, due to the frequency divider, is to be $\leq 1^{\circ}$ rms, then at 1 MHz it must be $\leq .0005$ degrees.

Now, assuming the output of the divide-by-82 is 1 MHz, the period is then 1 μsec. Figure 2-77 shows the approximate shape of the divider output pulse with the associated slope of $\frac{.2V}{nsec}$. At 1 MHz, the time variation of the leading edge of the pulse that would correspond to .0005 degrees would be

$$\frac{10^{-6}\ sec}{360\ deg} \times .0005\ deg = 1.4 \times 10^{-12}\ sec = .0014\ nsec$$

For a slope of $\frac{.2V}{nsec}$ it would require $\frac{.2V}{nsec} \times .0014$ nsec = 28 μv peak noise to cause approximately .0005 degrees of phase modulation at the divider output.

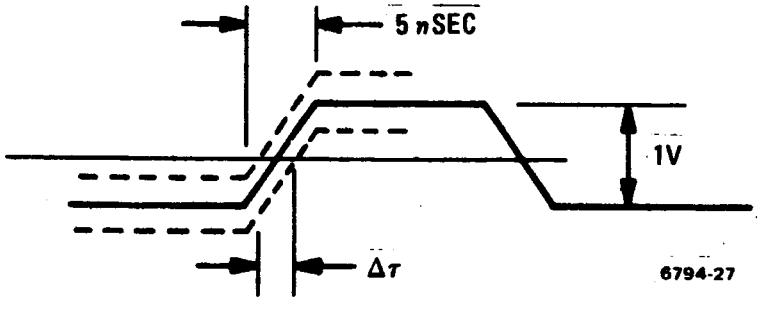
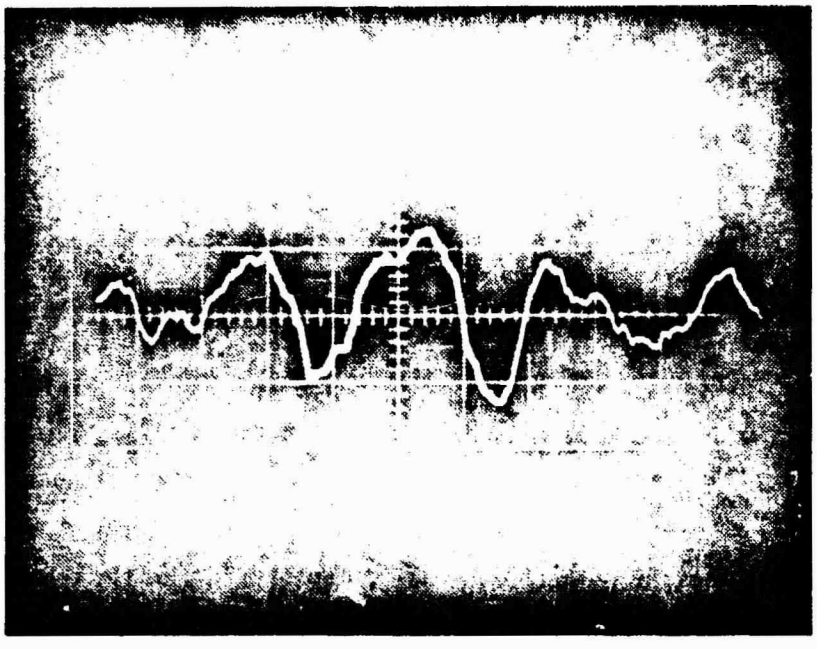
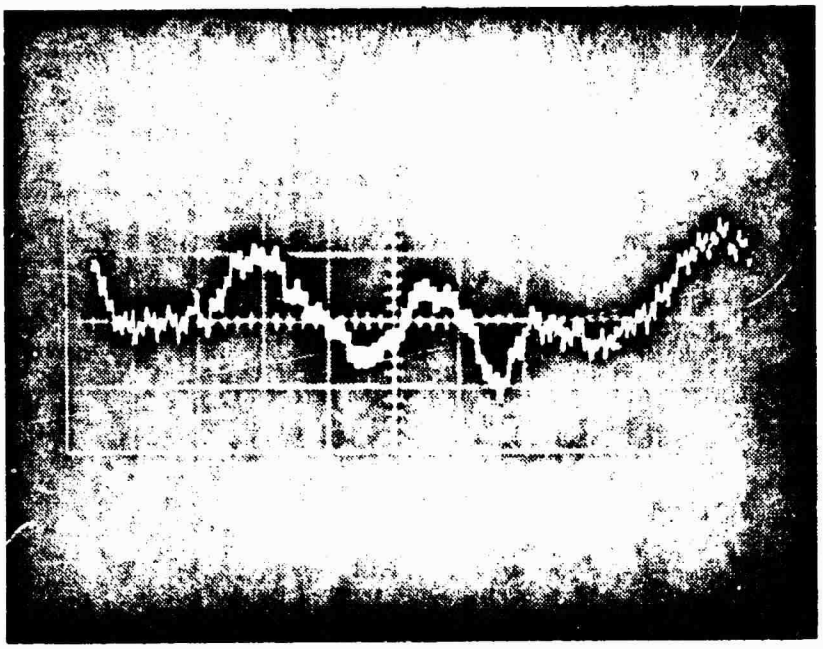


Figure 2-77. Divider Output Pulse



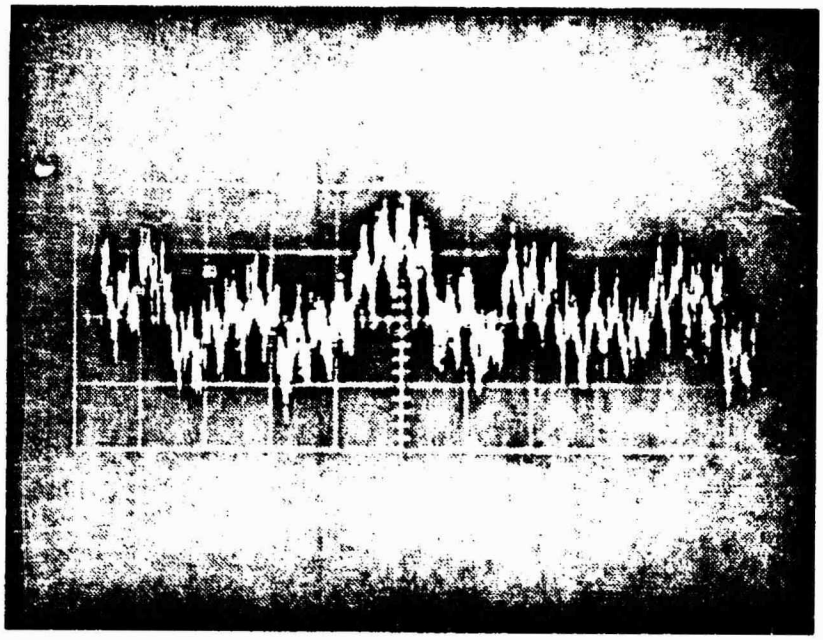
SENSITIVITY = .05 V/ cm
TIME = 50 MS/ cm

Figure 2-78. ϕ Det Output with Reference Signal Only



SENSITIVITY = .05 V/ cm
TIME = 50 MS/ cm

Figure 2-79. ϕ Det Output with Crystal VCO in Loop



SENSITIVITY = .05 V/ cm
TIME = 50 MS/ cm

Figure 2-80. ϕ Det Output Using LC VCO in Loop

$$f = \frac{6100}{6.28} = 975 \text{ Hz}$$

A comparison of the noise voltage can be made at the noise output of the phase noise test fixture for the following test conditions:

1. Reference oscillator only.
2. Divider included and a vcxo in the phase locked loop of figure 2-74.
3. Same as 2 except vcxo replaced by an l-c vco.

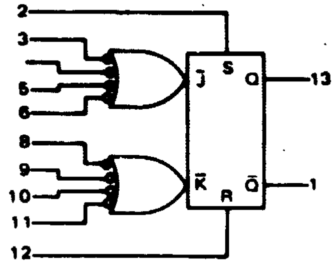
Conditions 1, 2, and 3 can be seen in figures 2-78, 2-79, and 2-80, respectively. These waveforms were photographed from an oscilloscope.

Although the amplitude and characteristics of the basic noise waveform is very similar in the three figures, the higher frequency noise superimposed on the waveforms of figures 2-79 and 2-80 is believed to be the 60, 120, 180, and 300 Hz components measured and recorded in table 2-8 that were not detected in table 2-7.

The correlation between measured results and the noise observed on the oscilloscope help support the conclusion that the divider does not significantly degrade the systems phase noise. However, further testing should be done to determine the significance of the higher frequency noise observed.

2.7.7 MC1013/MC1213 Data Sheets

ELECTRICAL CHARACTERISTICS



	@Test Temperature	$V_{IL\,min}$ to $V_{IL\,max}$	V_{IH}* min
MC1213	−55°C	-5.2 to -1.405	-1.165
	+25°C	-5.2 to -1.325	-1.025
	+125°C	-5.2 to -1.205	-0.875
MC1013	0°C	-5.2 to -1.350	-1.070
	+25°C	-5.2 to -1.325	-1.025
	+75°C	-5.2 to -1.260	-0.950

Characteristic	Symbol	Pin Under Test	MC1213 Test Limits −55°C Min	Max	+25°C Min	Max	+125°C Min	Max	Unit	MC1013 Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max	Unit	TEST VOLTAGE/ $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$
Power Supply Drain Current	I_E	7	-	-	-	29	-	-	mAdc	-	-	-	29	-	-	mAdc	-	
Input Current	I_{in}	2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc	-	
		3	-	-	-		-	-		-	-	-		-	-		-	
		4	-	-	-		-	-		-	-	-		-	-		-	
		5	-	-	-		-	-		-	-	-		-	-		-	
		6	-	-	-		-	-		-	-	-		-	-		-	
		8	-	-	-		-	-		-	-	-		-	-		-	
		9	-	-	-		-	-		-	-	-		-	-		-	
		10	-	-	-		-	-		-	-	-		-	-		-	
		11	-	-	-		-	-		-	-	-		-	-		-	
		12	-	-	-		-	-		-	-	-		-	-		-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc	-	
Q Logical 1 Output Voltage†	V_{OH}†	13	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	-	
Q Logical 0 Output Voltage	V_{OL}	13	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	-	
Q̄ Logical 1 Output Voltage†	V_{OH}†	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	-	
Q̄ Logical 0 Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	-	
"Q" or "Q̄" Latch Voltage	V_L	2	-1.16	-1.34	-1.09	-1.21	-0.93	-1.07	Vdc	-1.11	-1.25	-1.09	-1.21	-1.02	-1.14	Vdc	-	
		12	-1.16	-1.34	-1.09	-1.21	-0.93	-1.07	Vdc	-1.11	-1.25	-1.09	-1.21	-1.02	-1.14	Vdc	-	
																	Pulse In	Pul
Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	-	-	70	-	-	-	MHz	-	-	70	-	-	-	MHz	6,8	
Sensitivity (No Toggle)	-	1	See Figure 1							See Figure 1							6,8	
		13	See Figure 1							See Figure 1							6,8	
Sensitivity (Toggle)	-	1,13	See Figure 2							See Figure 2							6,8	1
Switching Times ④			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max			
Propagation Delay	t_{6+1+}	1	6.0	8.5	6.0	8.5	8.0	10.5	ns	6.0	8.5	6.0	8.5	6.5	9.0	ns	6	
	t_{6+1-}	1					7.5										6	
	t_{8+13+}	13					8.0										8	
	t_{8+13-}	13					7.5										8	
Rise Time	t_{1+}	1	4.0	7.5	4.0	7.5	5.5	9.5		4.0	7.5	4.0	7.5	5.0	8.0		6	
	t_{13+}	13	4.0		4.0		5.5	9.5		4.0		4.0			8.0		8	
Fall Time	t_{1-}	1	5.0		5.0		7.5	10		5.0		5.0			8.5		6	
	t_{13-}	13	5.0		5.0		7.5	10		5.0		5.0			8.5		8	

* Individually test each input using the pin connections shown.

† V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

① $V_{in(set)}$ V_{OH} then $V_{OL(max)}$.

② $V_{in(reset)}$ V_{OH} then $V_{OL(max)}$.

③ Input voltage is adjusted to obtain dV_{1} : dV_{in} = ∞.

④ AC fan-out 3

TEST VOLTAGE/CURRENT VALUES							
Vdc ±1.0%					mAdc		
$V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}		I_L		
-1.405	-1.165 to -0.825	-	-5.2		-2.5		
-1.325	-1.025 to -0.700	-0.700	-5.2		-2.5		
-1.205	-0.875 to -0.530	-	-5.2		-2.5		
-1.350	-1.070 to -0.740	-	-5.2		-2.5		
-1.325	-1.025 to -0.700	-0.700	-5.2		-2.5		
-1.260	-0.950 to -0.615	-	-5.2		-2.5		
TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:							
$V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}		I_L	ΔV_{in}	V_{CC} (Gnd)
	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12		-	-	14
	-	2	3, 4, 5, 6, 7, 8, 9, 10, 11, 12		-	-	14
	-	3	2, 4, 5, 6, 7, 8, 9, 10, 11, 12		-	-	
	-	4	2, 3, 5, 6, 7, 8, 9, 10, 11, 12		-	-	
	-	5	2, 3, 4, 6, 7, 8, 9, 10, 11, 12		-	-	
	-	6	2, 3, 4, 5, 7, 8, 9, 10, 11, 12		-	-	
	-	8	2, 3, 4, 5, 6, 7, 9, 10, 11, 12		-	-	
	-	9	2, 3, 4, 5, 6, 7, 8, 10, 11, 12		-	-	
	-	10	2, 3, 4, 5, 6, 7, 8, 9, 11, 12		-	-	
	-	11	2, 3, 4, 5, 6, 7, 8, 9, 10, 12		-	-	
	-	12	2, 3, 4, 5, 6, 7, 8, 9, 10, 11		-	-	
	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12		-	-	14
	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12		13	-	14
	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11		-	-	14
	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11		1	-	14
	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12		-	-	14
	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11		-	2 ③	14
	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11		-	12 ④	14
in	Pulse Out		V_{EE} = −4.0 Vdc				(+1.2V)
	13	-	2, 3, 4, 5, 7, 9, 10, 11, 12		-	-	14
	1	-			-	-	
	13	-			-	-	
	1, 13	-			-	-	
	1	-	2, 3, 4, 5, 7, 9, 10, 11, 12		-	-	14
	1	-			-	-	
	13	-			-	-	
	13	-			-	-	
	1	-			-	-	
	13	-			-	-	
	1	-			-	-	
	13	-			-	-	

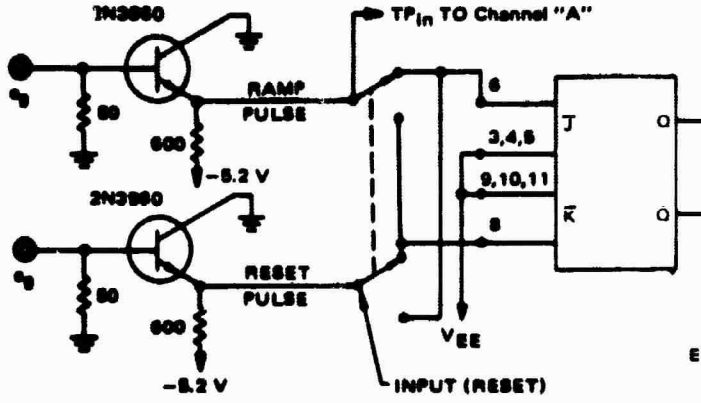
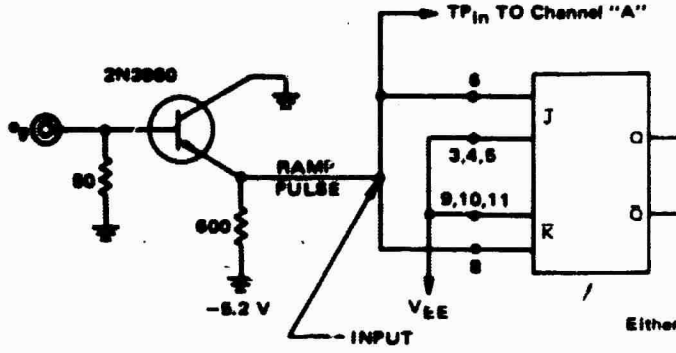
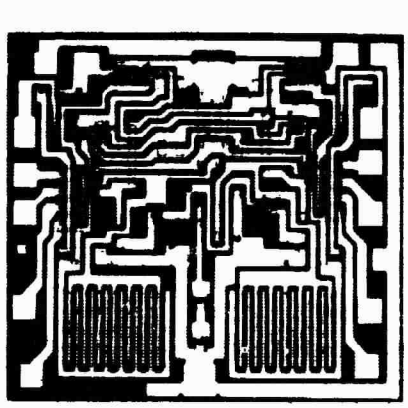


FIGURE 2 - SENSITIVIT





V$_{CC}$ = +1.2 Vdc ± 1% O

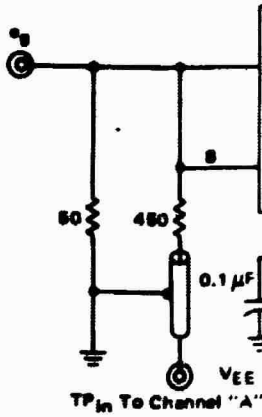
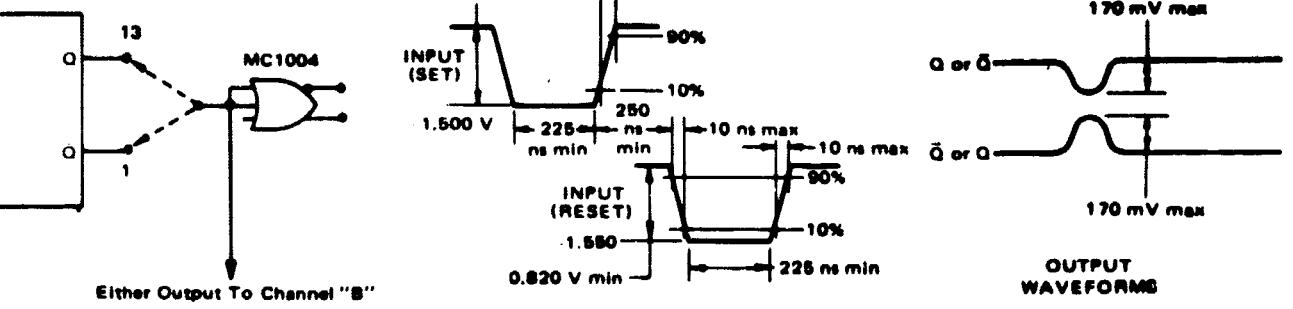


FIGURE 1 - SENSITIVITY (NO TOGGLE)



NSITIVITY (TOGGLE)

FIGURE 3 - INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

nnel "A"

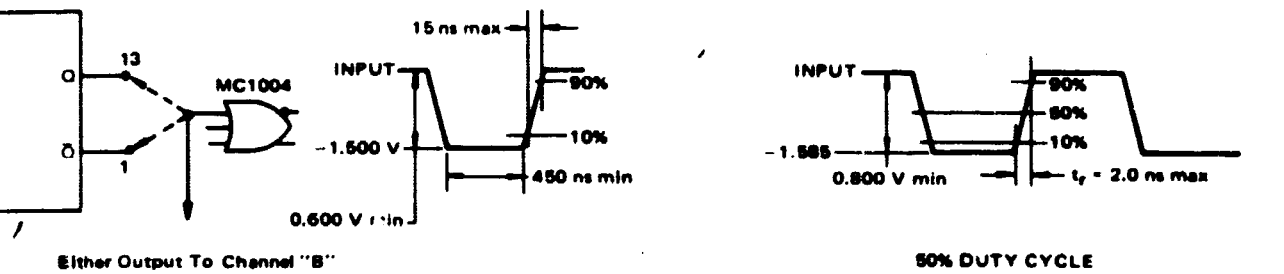
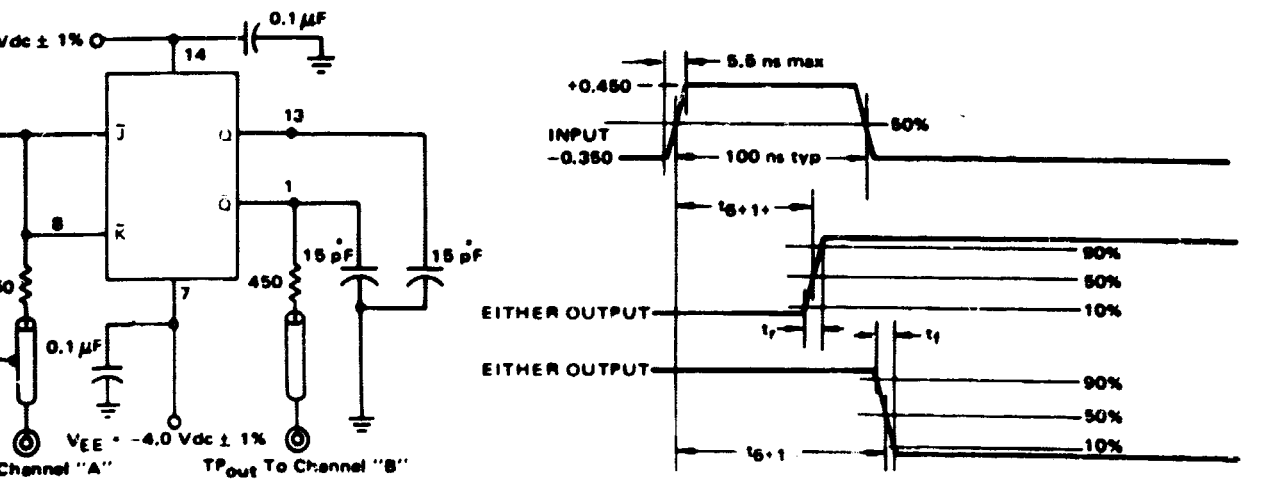


FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



*Load Corresponds to a Fan out 3

APPLICATIONS INFORMATION

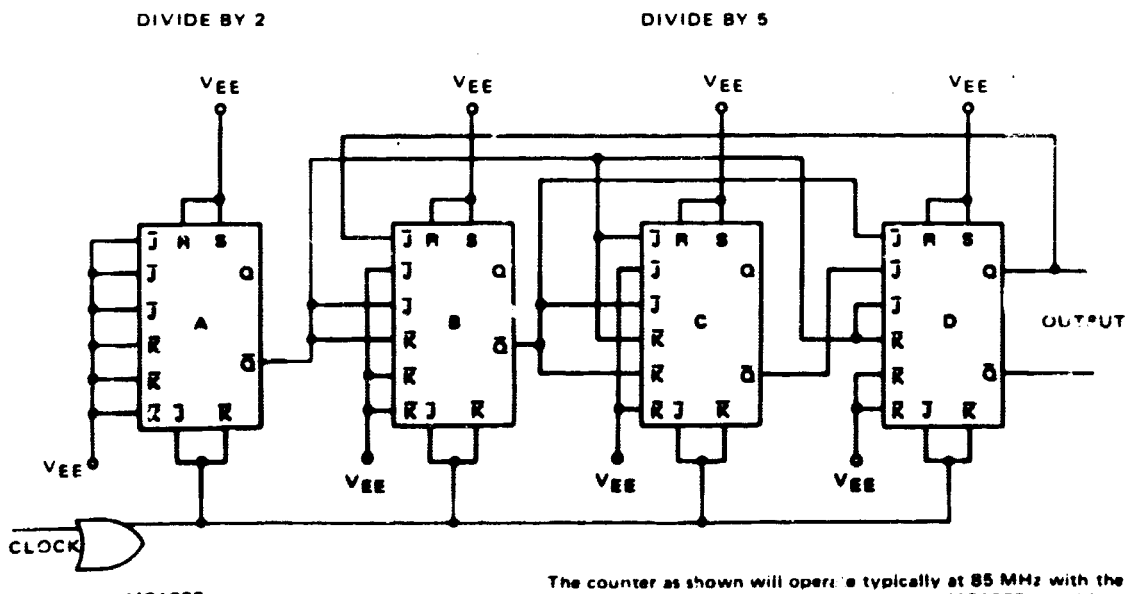
The MC1013 MC1213 J-K flip-flop is used in both counter and shift register applications. Typically the flip-flop will shift and toggle at 85 MHz. Flip-flop operation is illustrated by the curves shown on the back page. For a complete characterization of the device, refer to Motorola Application Note AN-280. Circuit operation is essentially the same as the MC314/MC364 flip-flop which is explained in Application Note AN-244. Due to the four $\bar{J}$ and four $\bar{K}$ inputs, many clocked and ripple through counters may be built without additional logic. Figure 5 is a table illustrating the $\bar{J}$ and $\bar{K}$ input equations for clocked counters, divide by 3 through 10. Figure 6 is a clocked BCD counter utilizing the logic equations shown in the table.

FIGURE 5 - INPUT EQUATIONS FOR CLOCKED COUNTERS

Divide By:	J_A	K_A	J_B	K_B	$\bar{J}_C$	$\bar{K}_C$	J_D	K_D
3	B	0	$\bar{A}$	0				
4	0	0	$\bar{A}$	$\bar{A}$				
5	C	0	$\bar{A}$	$\bar{A}$	$\bar{A}+\bar{B}$	0		
6	0	0	$\bar{A}+C$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A}$		
7	BC	0	$\bar{A}$	$\bar{A}+\bar{C}$	$\bar{A}+\bar{B}$	$\bar{B}$		
8	0	0	$\bar{A}$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}$		
9	D	0	$\bar{A}$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}+\bar{C}$	0
10	0	0	$\bar{A}+D$	$\bar{A}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}$	$\bar{A}+\bar{B}+\bar{C}$	$\bar{A}$

0 (logic zero) $\leq$ 1.6 V (pin usually tied to V_{EE})
All but ÷ 7 may be obtained without additional gating.
All $\bar{J}$ inputs and all $\bar{K}$ inputs are ORed together.

FIGURE 6 - CLOCKED BCD COUNTER USING MECL $\bar{J}$-$\bar{K}$ FLIP-FLOPS



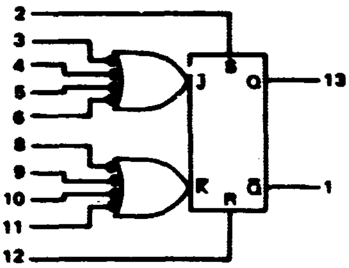
The counter as shown will operate typically at 85 MHz with the MC1001 as a driver and at 90 MHz with the MC1023 as a driver.

MC1013
MC1213

NOVEMBER 1967

Designed for use at clock frequencies to 70 MHz minimum (85 MHz typical). Logic performing inputs ($\bar{J}$ and $\bar{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 125 mW typical

*Any $\bar{J}$ or $\bar{K}$ input, not used for $\bar{C}_D$.
**$\bar{C}_D$ obtained by connecting one $\bar{J}$ and one $\bar{K}$ input together.

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

R-S TRUTH TABLE

	R	S	Q^{n+1}
Pin No.	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\bar{J}$-$\bar{K}$ Inputs Are Static

$\bar{J}_D$-$\bar{K}_D$ TRUTH TABLE

	$\bar{J}_D$	$\bar{K}_D$	Q^{n+1}
Pin No.	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

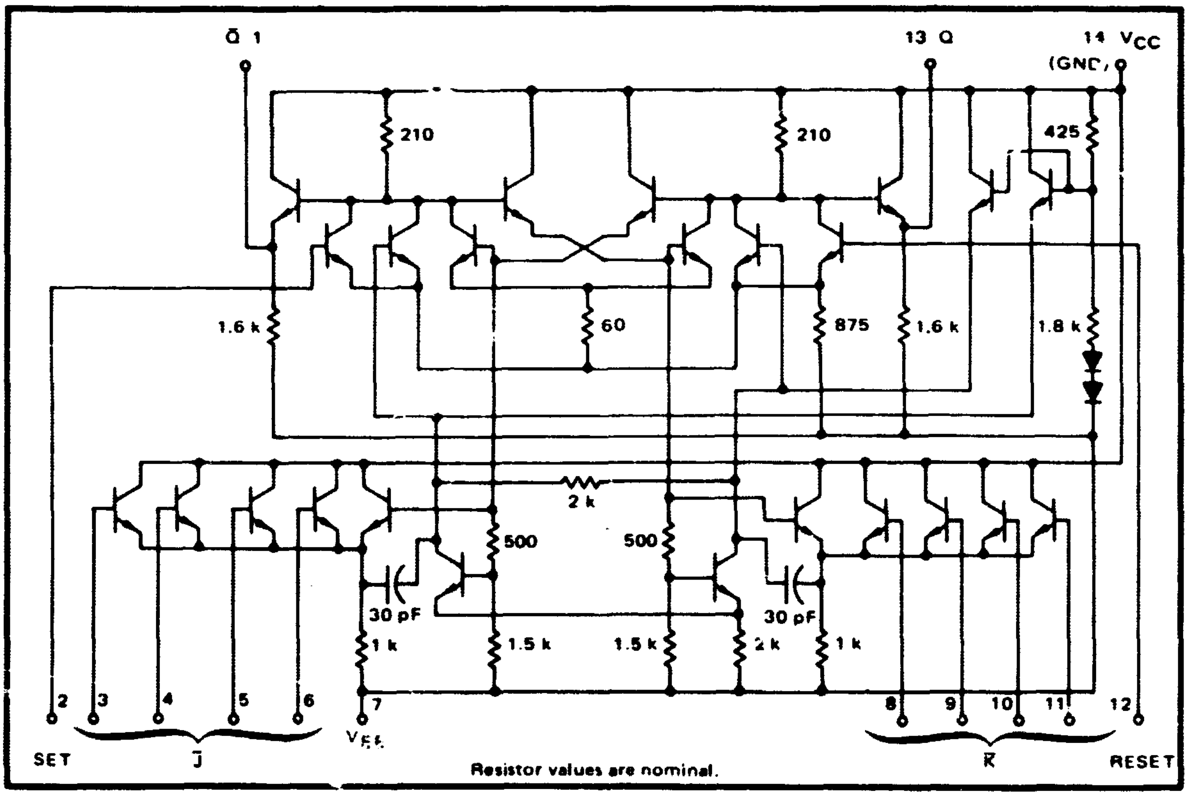
All Other $\bar{J}$-$\bar{K}$ Inputs And The R-S Inputs Are At a "0" Level

CLOCKED $\bar{J}$-$\bar{K}$ TRUTH TABLE

	$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^n
Pin No.	*	*	**	13
	φ	φ	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

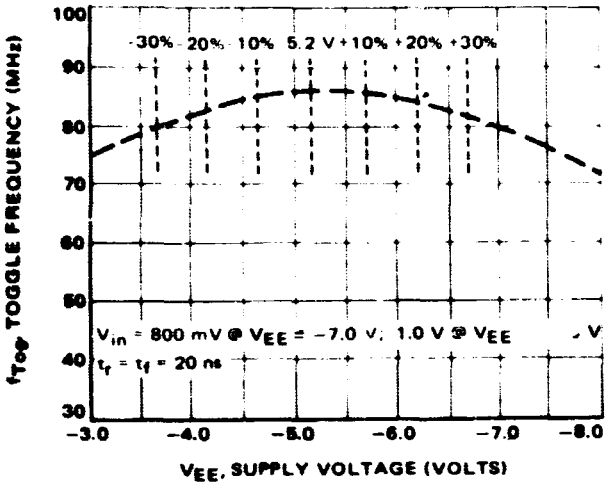
All Other $\bar{J}$-$\bar{K}$ Inputs And The R-S Inputs Are At a "0" Level

CIRCUIT SCHEMATIC



9-183B

FIGURE 7 - TYPICAL TOGGLE FREQUENCY versus V_{EE}



ALL UNUSED INPUTS RETURNED TO V_{EE}.
V_{EE} = −5.2 V, V_{in} = 800 mV, T_A = 25°C unless otherwise noted.
——— WORST CASE - - - - TYPICAL

FIGURE 8 - TYPICAL AND WORST CASE TOGGLE FREQUENCY versus AMBIENT TEMPERATURE

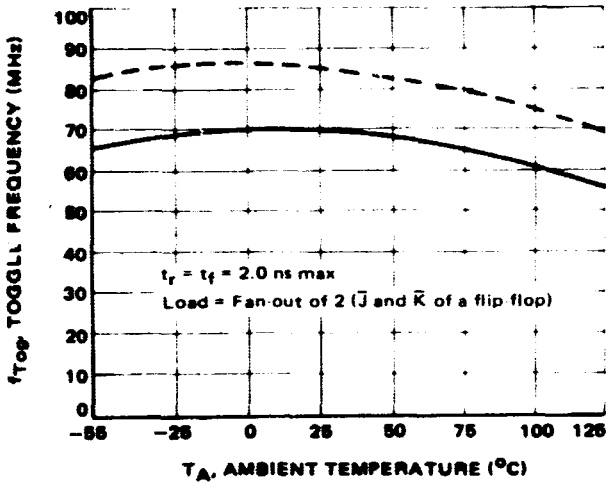


FIGURE 9 - AMPLITUDE versus RISE TIME TO INSURE TOGGLE

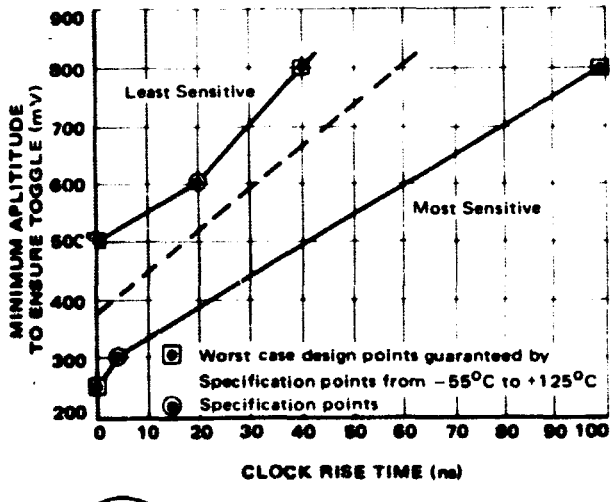
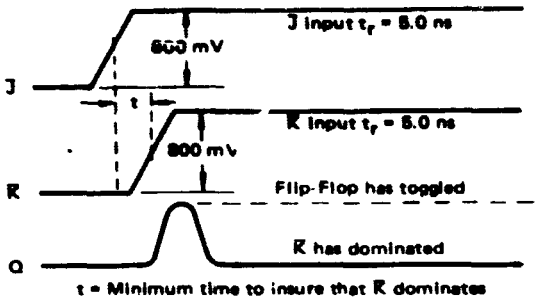


FIGURE 10 - TIME TO DOMINATE



t = Minimum time to insure that $\overline{K}$ dominates and that the flip-flop does not toggle

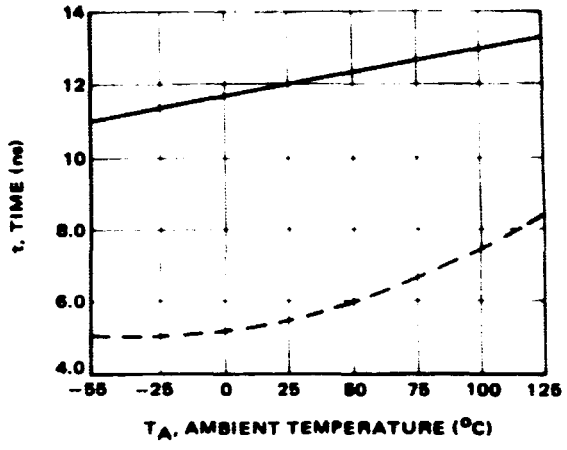
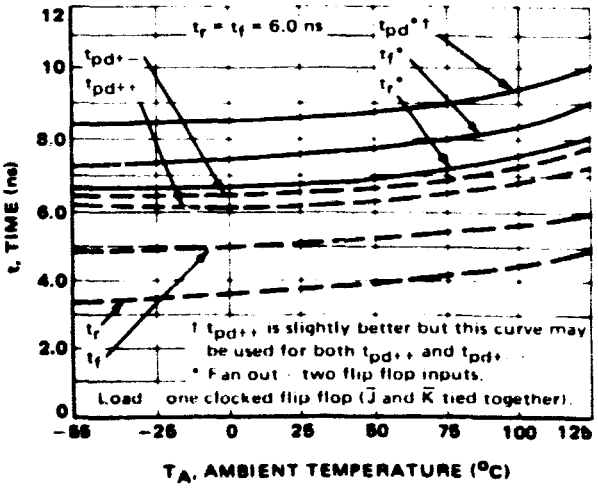


FIGURE 11 - PROPAGATION DELAY TIMES, RISE TIME, FALL TIME versus TEMPERATURE



2.7.8 Bibliography of Pertinent References

1. Asher, Gil, "Crystal Oscillator Phase Noise Study", TM CWT-140, 10 April 1968.

2. Elliott, W. S., "Stability of a Phase-Locked Oscillator with a Counter Type Divider in the Loop", Masters Thesis, Iowa State University, Ames, Iowa, 1963.

3. Byrne, C. J., "Properties and Design of the Phase-Controlled Oscillator with a Sawtooth Comparator", Bell System Technical Journal #41, pp 559-602, March 1962.

4. Goldstein, A. J., "Analysis of the Phase-Controlled Loop with a Sawtooth Comparator", Bell System Technical Journal #41, pp. 603-633, March 1962.

5. Gardner, F. M. and Kent, S. S., "Theory of Phase Lock Techniques as Applied to Aerospace Transponders".

2.8 CRYSTAL OSCILLATOR PHASE NOISE

2.8.1 Introduction

This subsection describes the results of a study of phase noise in crystal oscillators for application in an Advanced S-Band Transponder. This study has been directed toward:

1. The surveying of phase noise test measurement techniques used industry-wide and in Motorola.

2. Determining the causes of and minimizing the phase noise in crystal oscillators and vcxo's.

3. Determining how the oscillators designed and built at Motorola compare with oscillators designed and built at other companies.

A short section is included which compares the broadband phase noise of several transponders designed and built at Motorola.

Following the last section of this memo is a bibliography from which additional information can be found concerning phase noise, transistor noise, transistor noise, and oscillator noise in general.

2.8.2 Conclusion

The significant causes of crystal oscillator noise, and their relative importance, continues to be difficult to ascertain. Applicable measurement techniques for investigating the subject are complex, expensive, and very inflexible. Published information on the subject is in forms which allow very little comparison of performance between the devices of various manufacturers.

This study has been discontinued with many obvious questions left unanswered because it appears that the advances to be expected from its continuation are not of sufficient value to merit further pursuit at this time. On the basis of the work done in this study, the following conclusion can be stated with a reasonable degree of certainty.

1. The crystal oscillator used in Motorola CW transponders of recent design have as low a noise as any comparable crystal oscillators for which information is available.

2. Crystal oscillator noise is not at this time a significant factor in limitation of S-band transponder performance.

3. The significant causes or sources of noise in crystal oscillators are:

   a. Transistor r-f noise
   b. Transistor a-f noise (1/f noise)
   c. Tantalum capacitor noise
   d. Oscillator design parameters such as loaded Q, gain margin, limiter operation, etc.

   The relative importance of these factors is believed to vary drastically between oscillator designs.

4. The phase noise expected on an S-band signal is about .3 to .5 degrees rms in the band from approximately 5 to 10,000 Hz from the carrier. When expressed in terms of spectral density, relative to the carrier amplitude, typical numbers to be expected are -90 db/Hz at 40 Hz, -100 db/Hz at 100 Hz, and -112 db/Hz at 400 Hz.

2.8.3 Phase Noise Measurement Methods

2.8.3.1 Industry Wide

The typical way of measuring phase noise is by means of a phase-locked loop. This method is shown in figure 2-81. Several variations of this measurement scheme were found when the literature was surveyed. For example one method utilizes two oscillators of identical frequency, one is fixed in frequency and the other is a vcxo. The frequencies of both oscillators are multiplied to the microwave region and applied to a phase detector. The error signal from the phase detector is connected to a low pass filter and then to the vcxo, phase locking one oscillator to the other. This method provides a measure of the phase noise directly in degrees. Another method does not multiply the oscillator outputs to higher frequencies, but rather uses a lower frequency phase detector.

2.8.3.2 Motorola

One of the several methods used at Motorola is similar to the preceding one. It is basically a 70 MHz receiver and is used to compare crystal residual phase noise with crystal vibration phase noise.

The method used for this study utilizes the phase lock method, but is somewhat more sophisticated. Figure 2-82 depicts the test configuration. The r-f oscillator analyzer (figure 2-83) is actually a phase lock receiver that multiplies f and f + Δf of the two oscillators to S-Band, mixes them to form a 20 MHz i-f and compares the i-f phase to an internal reference oscillator. The output of the phase detector is then fed through a low pass filter and either applied to the internal reference or an external vcxo. The analyzer has the advantage of having noise bandwidths of 1000, 300, 100, 30, 10 and 3 Hz.

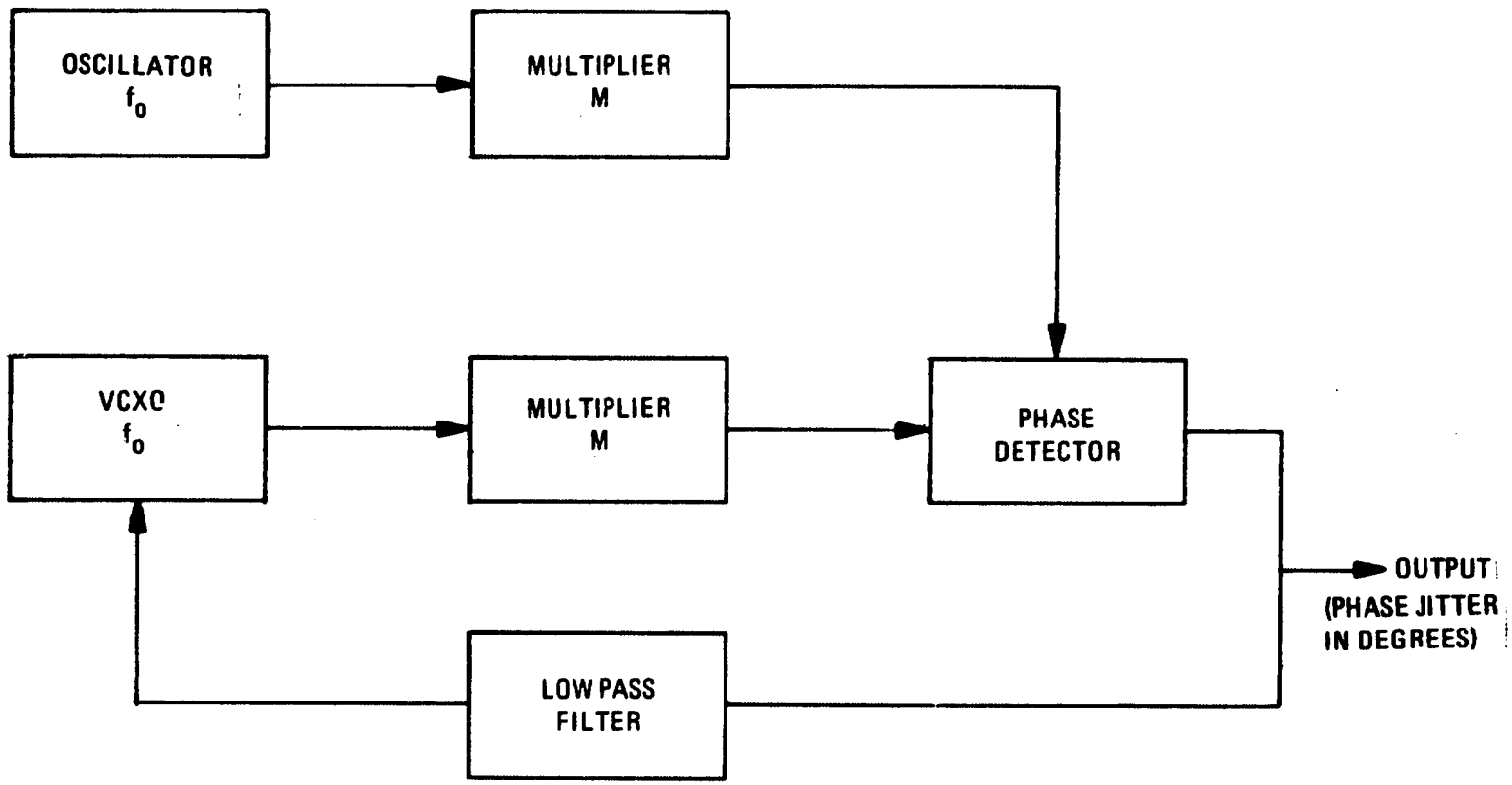


Figure 2-81. Phase-Lock Method

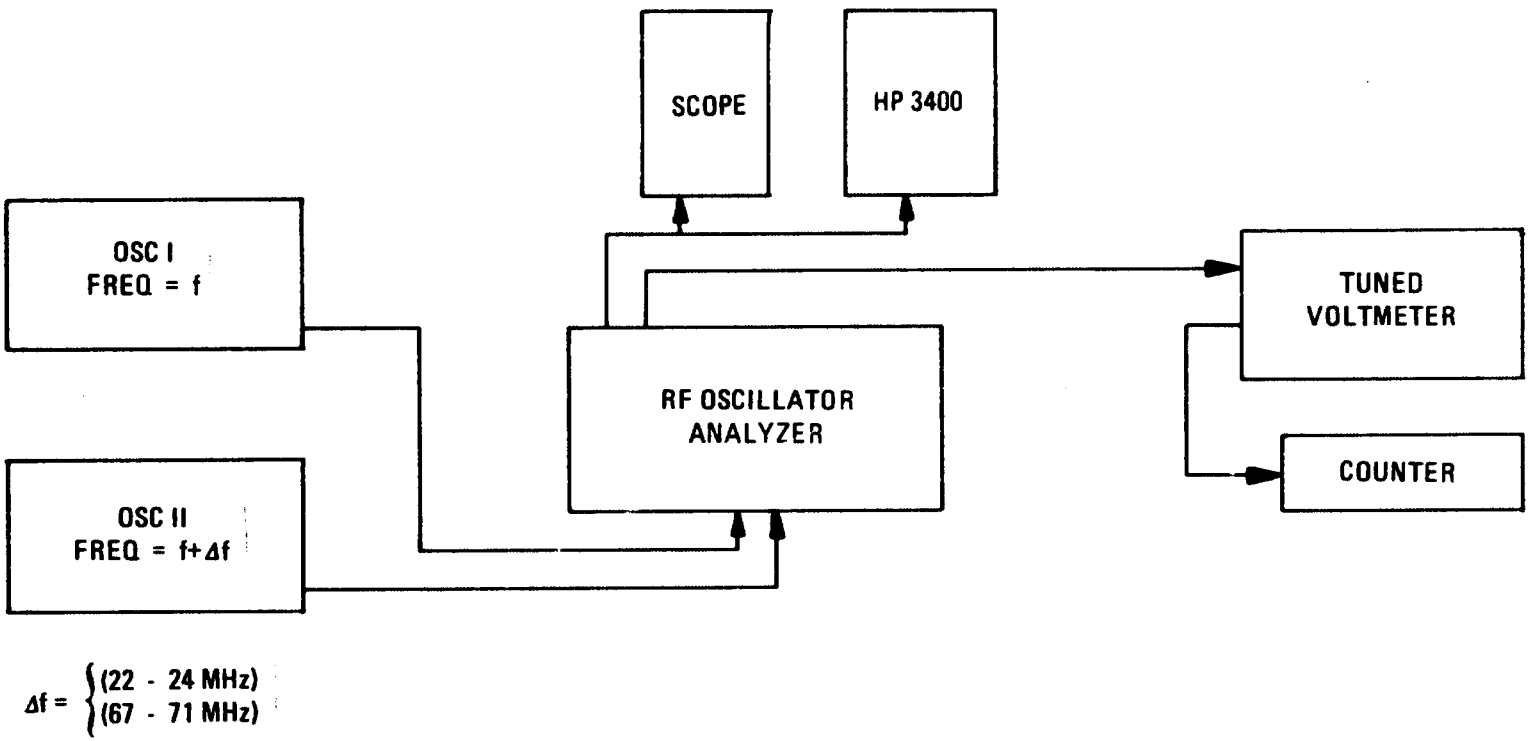


Figure 2-82. Noise Measurement Test Configuration

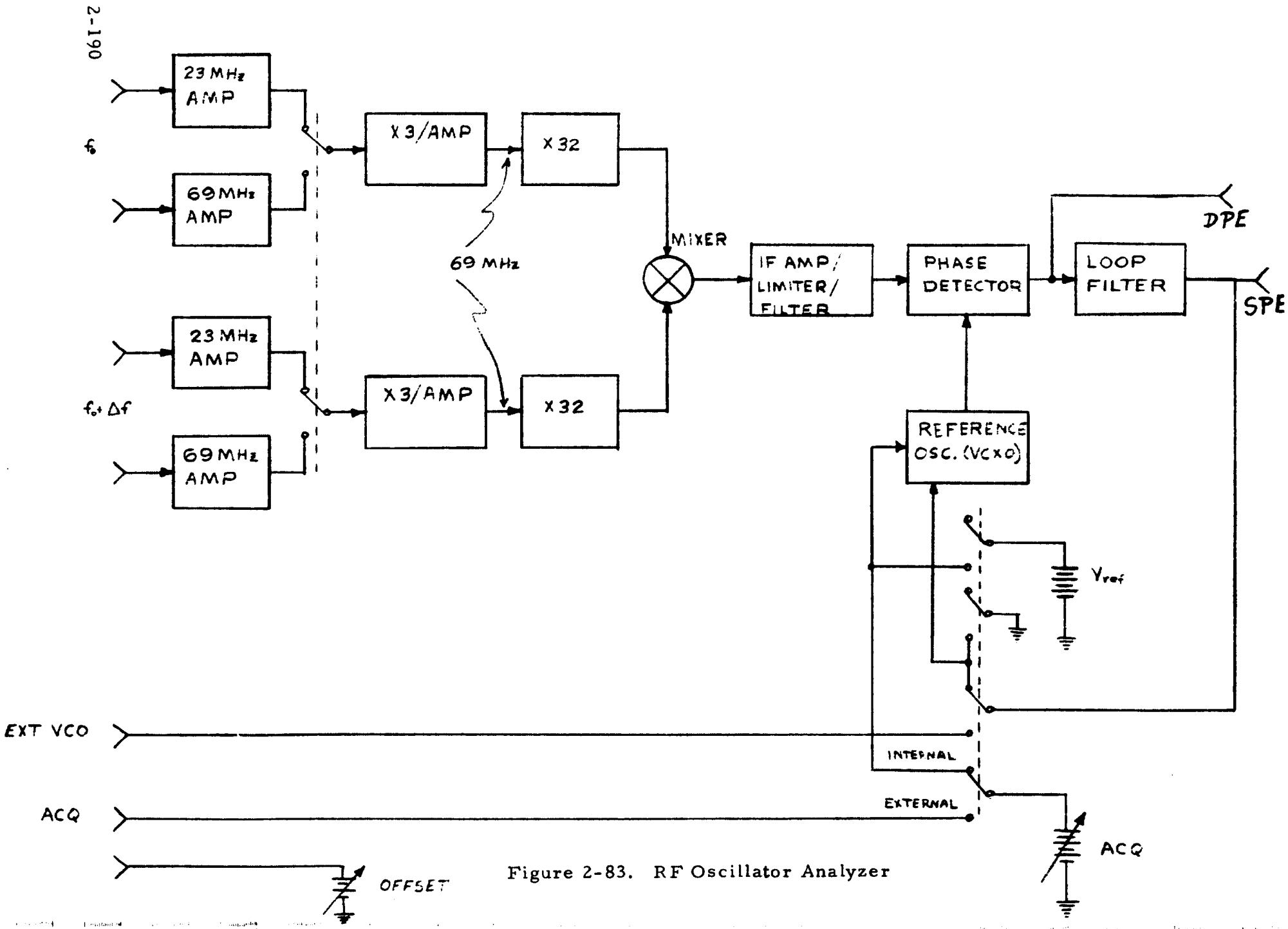


Figure 2-83. RF Oscillator Analyzer

The broadband phase noise measurements were measured using the r-f oscillator analyzer, in $2B_L$ of 30 Hz, and an H-P 3400 which has a low frequency cutoff of 5 Hz. The analyzer upper frequency cutoff is approximately 10 kHz. The frequency spectra were measured using an HP-302A Wave Analyzer and the r-f oscillator analyzer in $2B_L$ of 30 Hz. The results were converted to radians and normalized to 1 Hz noise bandwidth.

Using the oscillator analyzer, two oscillators at a time were measured. By interchanging crystals and circuits, each oscillator was compared to each of the other two. In this way, a set of three simultaneous equations involving three unknowns was obtained and solved for the unknowns to arrive at the phase noise contribution of each oscillator.

Another measurement technique uses a Frequency Error Expander (figure 2-84) in phase noise measurements. The error expander (figure 2-85) is a device which accepts any of eight commonly used standard frequencies 100 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz, 3 MHz, 4 MHz, and 5 MHz, converts it to 1 MHz, then effectively expands phase deviations by 10, 100, or 1,000 by means of multipliers and mixers, and provides the output at 1 MHz. The output of the error expander and reference oscillator are fed into a phase comparator whose output is connected to a scope or voltmeter.

The main disadvantage of all measurement methods described here is the limited frequency range of each device and the requirement for a stable reference. At present, there doesn't seem to be a very wide frequency band test set available to measure the phase instabilities of oscillators of different frequencies. Each frequency range is relatively narrow due to the specialized circuitry necessary to the measurement methods.

2.8.4 Sources of Noise

To determine the main sources of phase noise, this section of the study is divided into four parts. The first part deals primarily with the effects of crystal

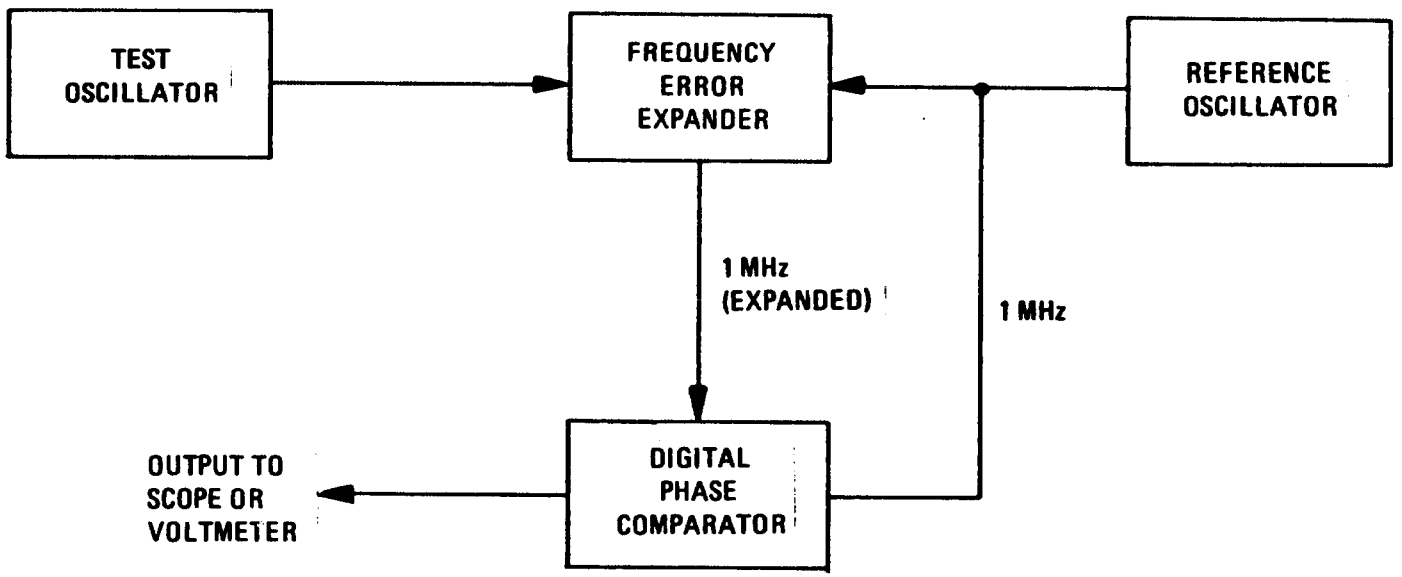


Figure 2-84. Error Expander Method

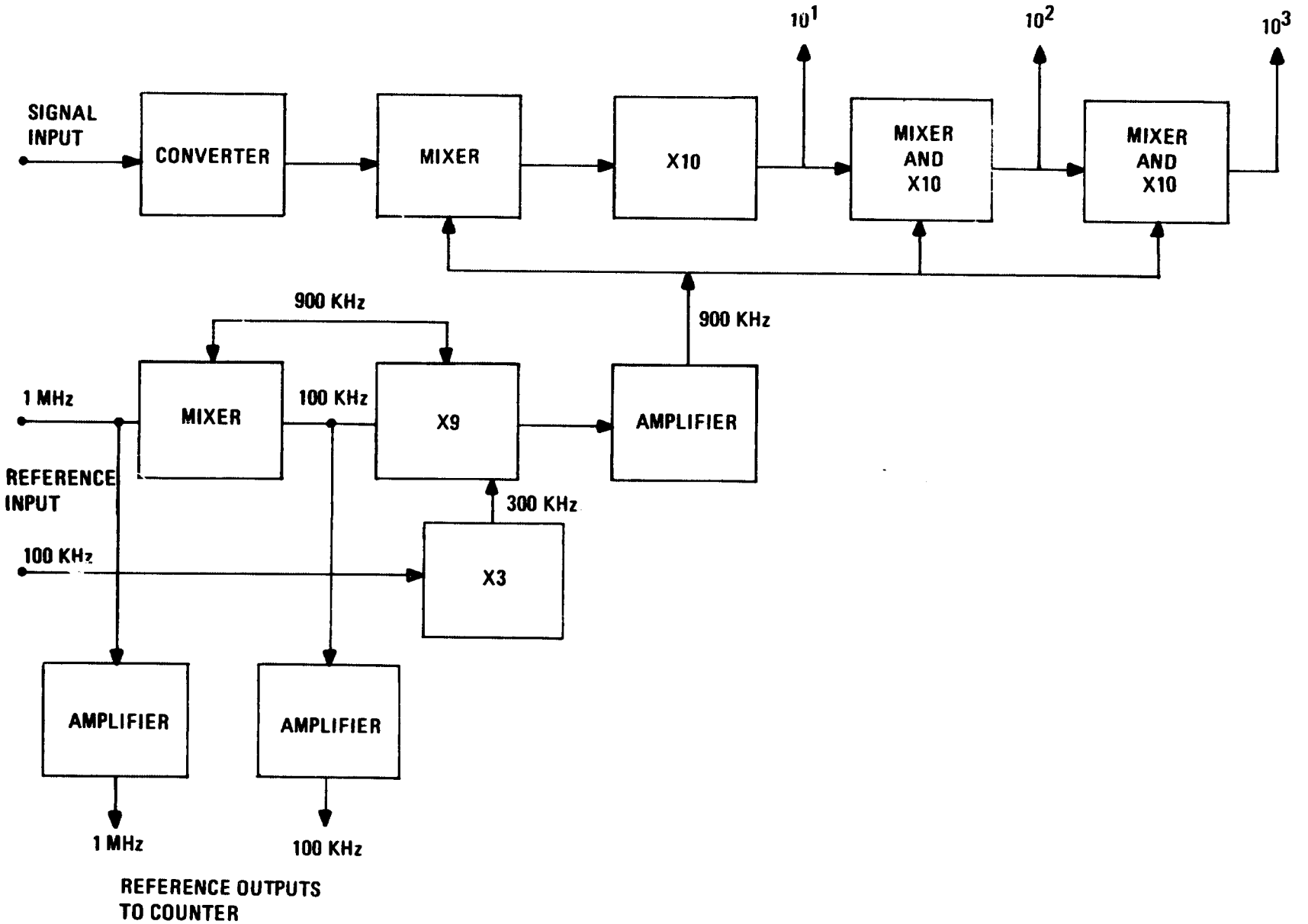


Figure 2-85. Error Expander

parameters on phase noise. As a continuation of the work done during the first part of the study, the second part takes up the effects of the active elements used in the amplifier of the oscillator circuit. The third part combines the results of the first two parts and takes into consideration the noise contribution of the non-linear device in the feedback circuit. Part four deals with circuit elements as causes of phase noise.

2.8.4.1 Crystal Parameters

The crystal itself does make a minor contribution to oscillator phase noise. Table 2-9 shows the phase jitter of two crystal oscillators measured using a phase locked loop with variable noise bandwidths ($2B_L$).

Table 2-9. Crystal Oscillator Phase Jitter
(22.7 MHz @ S-Band)

$2B_L$ (Hz)	I(^{o}RMS)	II(^{o}RMS)
300	.064	.067
100	.259	.271
30	.525	.603

These measurements were made on identical circuits, shown in figure 2-86, using the r-f oscillator analyzer method described in paragraph 2.8.3.2. This contribution depends on the loaded Q of the crystal circuit, which is somewhat dependent on the Q of the crystal and how the feedback circuit loads the crystal. The loaded Q of the crystal is a factor in determining the closed loop bandwidth of the oscillator. This in turn controls the amount of noise which is fed back to input of the oscillator. The value of loaded Q at which this noise becomes significant is as yet undetermined.

2.8.4.2 Active Devices in Oscillator Amplifiers

The active device used in the oscillator is the main contributor of phase noise in oscillators. The phase noise contribution of transistors can be separated into two parts. These are phase noise due to r-f noise and phase noise due to 1/f

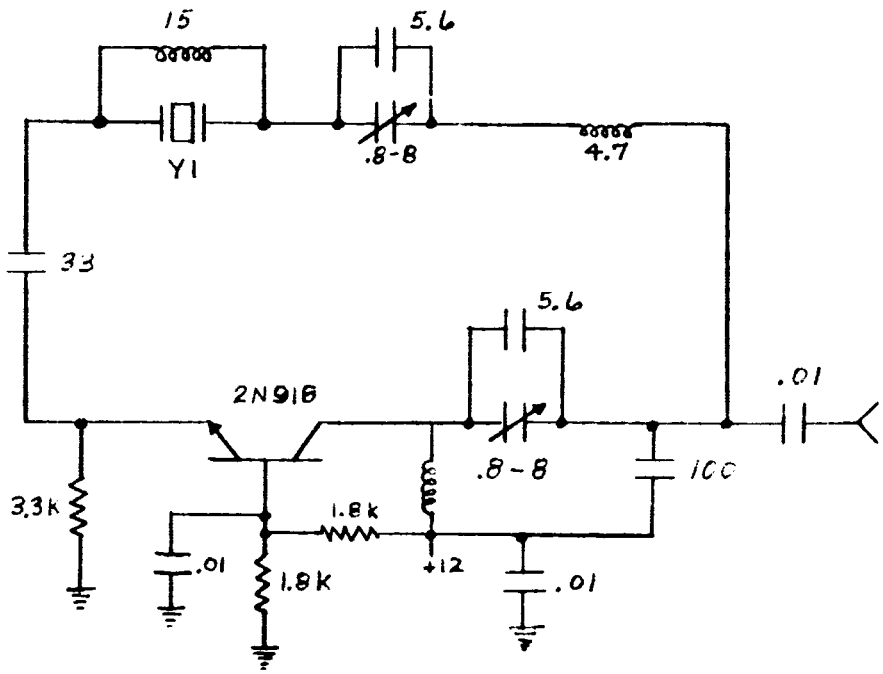


Figure 2-86. Transistor Oscillator

(or low frequency) noise, with the latter appearing to be the prime factor according to most articles surveyed. Figure 2-88 shows the low frequency noise spectrum of two crystal oscillators, one of figure 2-86 configuration and the other of figure 2-86 configuration. Both of these curves exhibit an approximate 1/f shape which is typical of oscillators.

2.8.4.3 Non-Linear Devices in Feedback Circuit

The use of a voltage-variable capacitor (varactor) as a feedback circuit element contributes little or no phase noise to an oscillator. Certain conditions must be met for this to be true. For example, the loss of the varactor must be low compared with the other circuit losses which fix the noise level. Also, care must be taken to ascertain that the bias applied to the capacitor does not apply noise modulation. It is also necessary to maintain the voltage level across the varactor at a sufficiently low level to avoid voltage breakdown. This means that a fixed crystal oscillator could have approximately the same phase noise as a properly designed voltage controlled crystal oscillator. The broadband phase noise of a crystal oscillator and vcxo is shown in table 2-10 and, the low frequency phase noise spectrum is indicated in figure 2-89.

Table 2-10. Oscillator Broadband Phase Noise

$2B_L$ (Hz)	VCXO (^{o}RMS)	Fixed Osc. (^{o}RMS)
300	.127	..154
100	.177	.177
30	.354	.354

As can be seen in table 2-10, the broadband phase noise of vcxo and fixed crystal oscillator are approximately equal in this case.

2.8.4.4 Other Sources of Phase Noise

During the course of this study, it was found that tantalum capacitors are a source of broadband noise. Table 2-11 shows the results of the investigation into tantalum capacitors. These measurements were made on a crystal oscillator

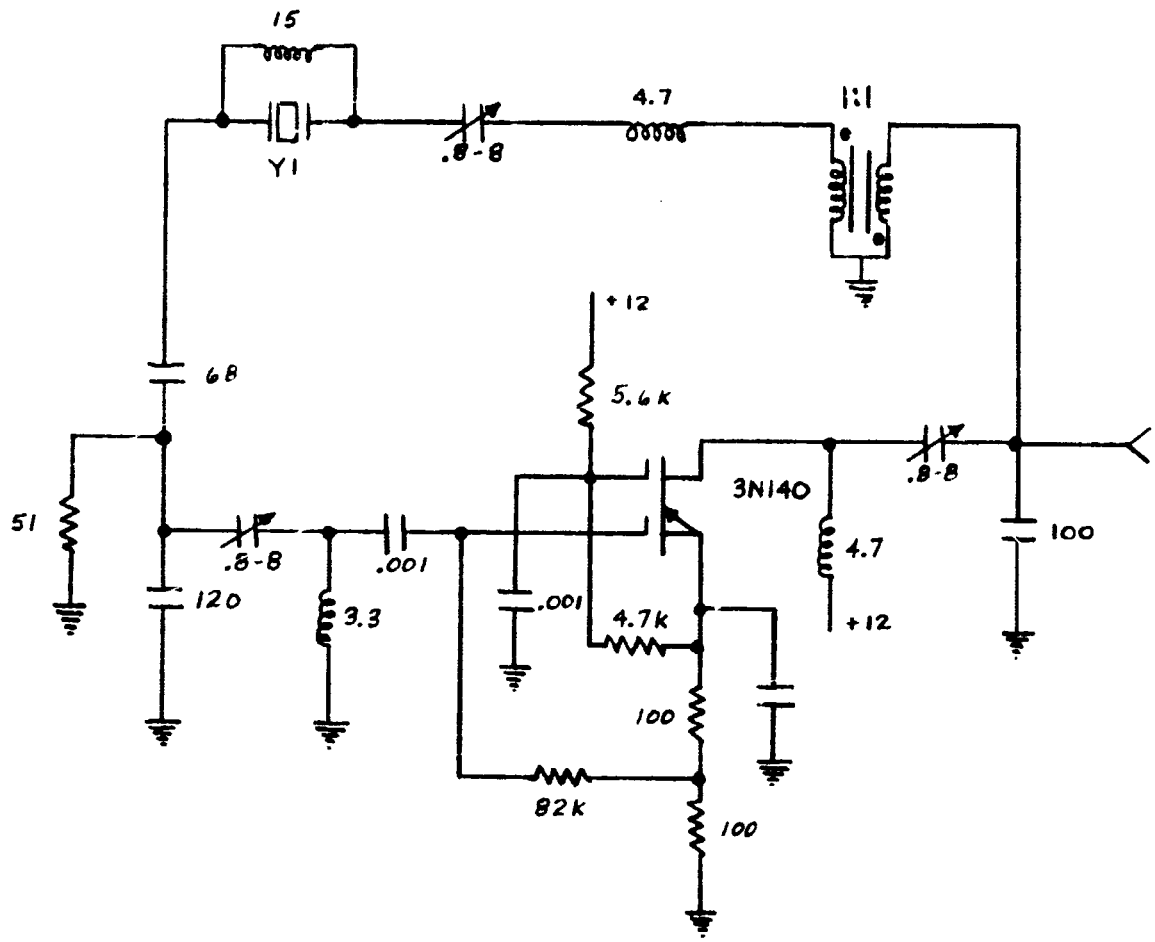


Figure 2-87. MOSFET Oscillator

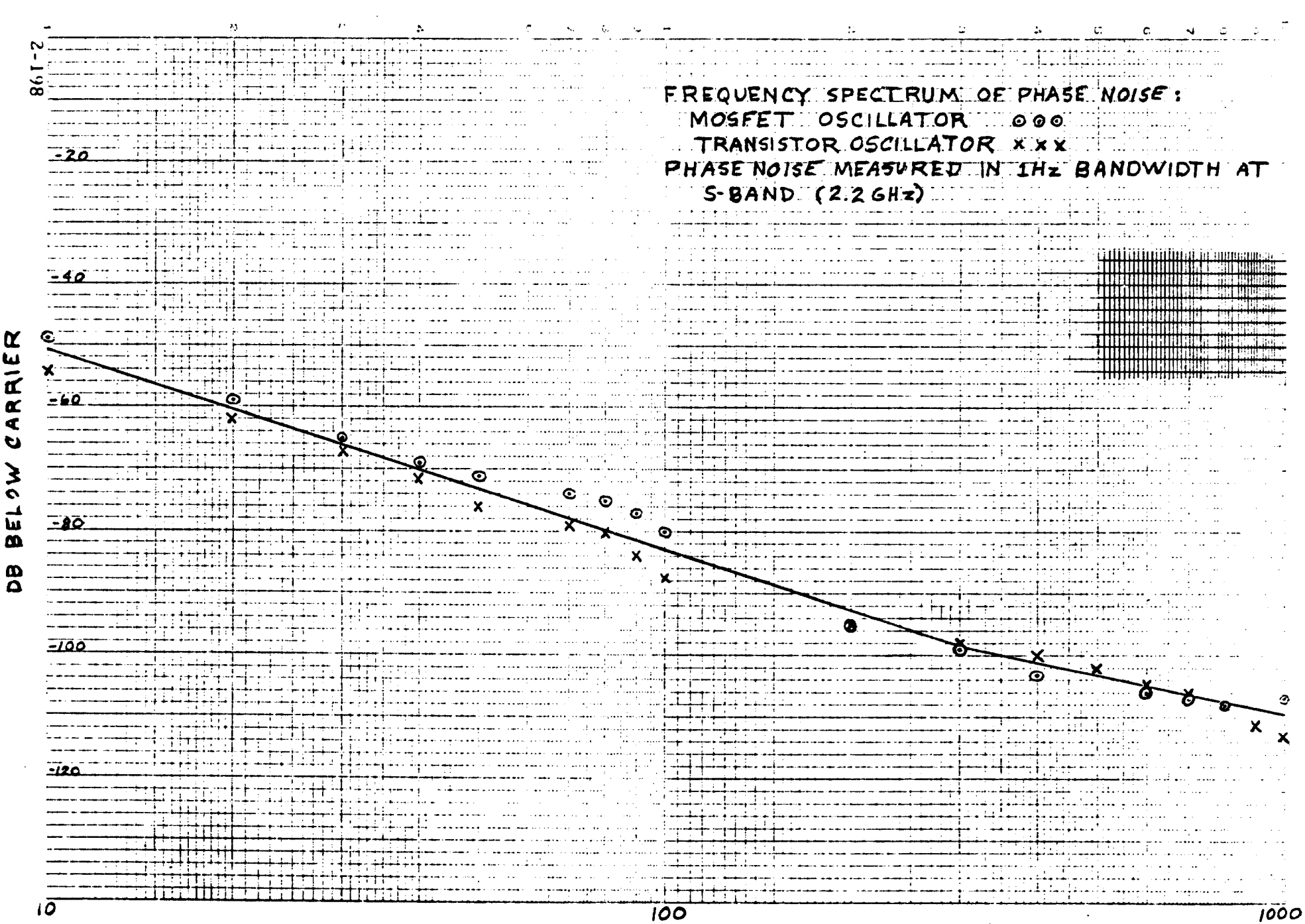

FREQUENCY SPECTRUM OF PHASE NOISE:
MOSFET OSCILLATOR ⊙⊙⊙
TRANSISTOR OSCILLATOR xxx
PHASE NOISE MEASURED IN 1Hz BANDWIDTH AT S-BAND (2.2 GHz)
-20
-40
-60
-80
-100
-120
DB BELOW CARRIER
10
100
1000
FREQUENCY (Hz FROM CARRIER)

Figure 2-88

Table 2-11. Tantalum Capacitor Broadband Noise

Equipment	Phase Noise (Degrees RMS)
70 MHz Xtal Osc. (no zener)	.354
70 MHz VCXO (with zener)	
Tantalum Capacitor bypass	.421
Ceramic Capacitor bypass	.388

that was converted to a vcxo and a zener diode used to provide bias to one side of the voltage-variable capacitor with tantalum and ceramic capacitors used as bypass capacitors. It appears that the noise generated by the tantalum capacitors modulate the voltage-variable capacitor causing phase noise. Tantalum capacitors didn't appear to increase the low frequency noise level as shown in figure 2-89. Ceramic or mylar capacitors, used as bypass capacitors yield a broadband phase noise level of 1-2 db lower than tantalum capacitors in this particular case. This phenomenon was discovered several years ago by other investigators and was passed along to Motorola personnel in informal discussion. As shown in table 2-11, it was verified by test in this study. Further investigation of this phenomenon is required before specific recommendations can be made concerning minimization of its effects. At this point it is sufficient to recognize the potential effect and consider the use of capacitor types other than tantalum.

2.8.5 Performance

2.8.5.1 Motorola Units

An attempt was made to measure and compare the oscillators presently used in Motorola equipment. The results (table 2-12) are hard to correlate because of the different noise bandwidths associated with each system. In addition to the table, figure 2-90 shows the shape of the low frequency phase noise spectrums of the SGLS 770 Receiver-Demodulator and SGLS 770 Transmitter AOPM auxiliary oscillator.

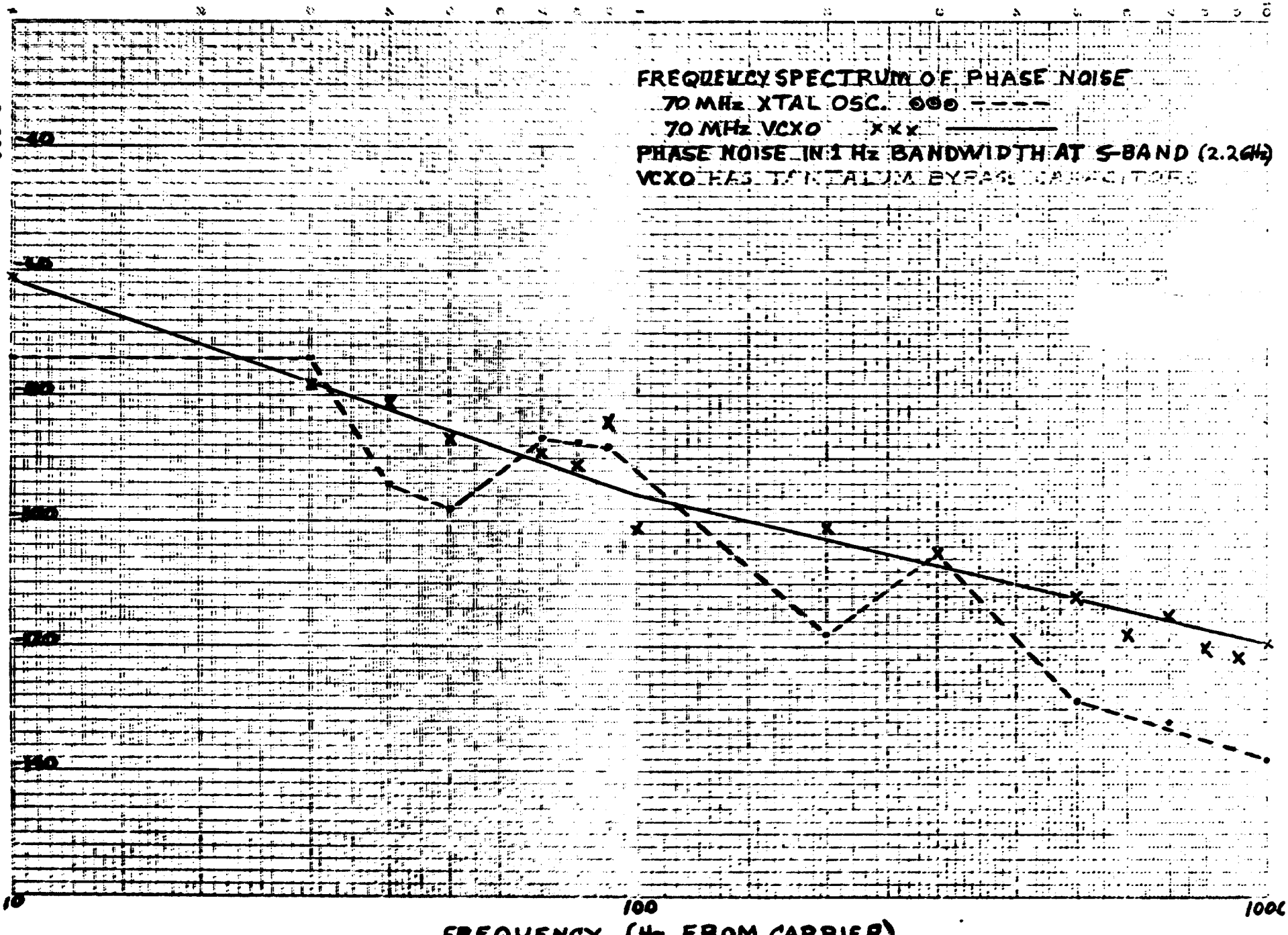

FREQUENCY SPECTRUM OF PHASE NOISE
70 MHz XTAL OSC. ooo ----
70 MHz VCXO xxx ——————
PHASE NOISE IN 1 Hz BANDWIDTH AT S-BAND (2.2GHz)
VCXO HAS TANTALUM BYPASS CAPACITORS
2-200
dB BELOW CARRIER
10
100
1000
FREQUENCY (Hz FROM CARRIER)

Figure 2-89

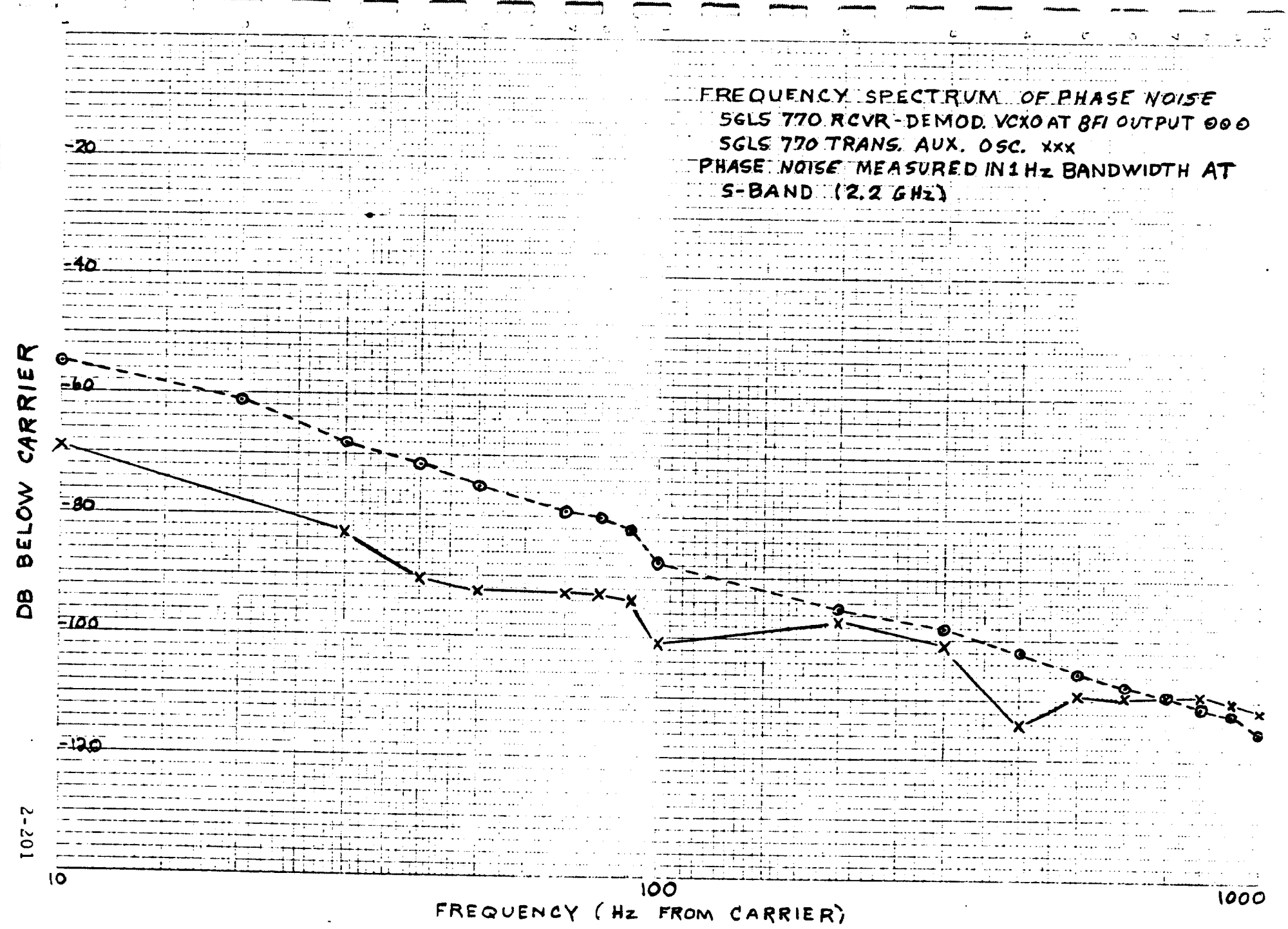

FREQUENCY SPECTRUM OF PHASE NOISE
SGLS 770 RCVR-DEMOD. VCXO AT 8FI OUTPUT ooo
SGLS 770 TRANS. AUX. OSC. xxx
PHASE NOISE MEASURED IN 1 Hz BANDWIDTH AT
S-BAND (2.2 GHz)
DB BELOW CARRIER
-20
-40
-60
-80
-100
-120
10
100
1000
FREQUENCY (Hz FROM CARRIER)
2-201

Figure 2-90

Table 2-12

$2B_L$ (Hz)	Block II PM Transmitter (°RMS)	SGLS 770 Transmitter (°RMS)	AOPM Aux. Oscillator (°RMS)	SGLS 770 Rcv'r-Demodulator (°RMS)
300	---	---	.059	.396
200	---	1.1	---	---
100	---	---	.118	1.111
30	---	---	.354	2.475
21	.705	---	---	---

2.8.5.2 Industry Wide Units

H. S. Pustarfi of Bell Telephone Laboratories has written a paper (see item (30) paragraph 2.8.6, bibliography for this subsection), which describes a 5.0 MHz vcxo. This oscillator, figure 2-91, utilizes two 2N3823 field-effect transistors and was shown to have phase noise in a 1 Hz bandwidth, at 5 MHz, on the order of 120 db to 125 db below the carrier in the range 100 Hz to 5.0 KHz from the carrier. This oscillator was again measured when the 2N3823's were replaced by 2N2222 silicon planar transistors, and the corresponding measurements revealed 8 db more phase noise in the same range. Figure 2-92 shows how this oscillator compares to two oscillators built during this study in phase noise frequency spectra. In the frequency range 100 Hz to 1000 Hz, these oscillators were 0 - 25 db less noisy than the Bell Telephone oscillators, whereas below 100 Hz, the oscillators have about the same noise density. The Bell Telephone oscillator was designed primarily for very good long term stability, and it is generally considered that the short term stability must be sacrificed for this feature. There is also a possibility of a significant difference in the measurement techniques employed in each case.

Note that the oscillator noise is compared at the oscillator frequency rather than on a normalized basis such as "ppm" or "referenced to S-Band."

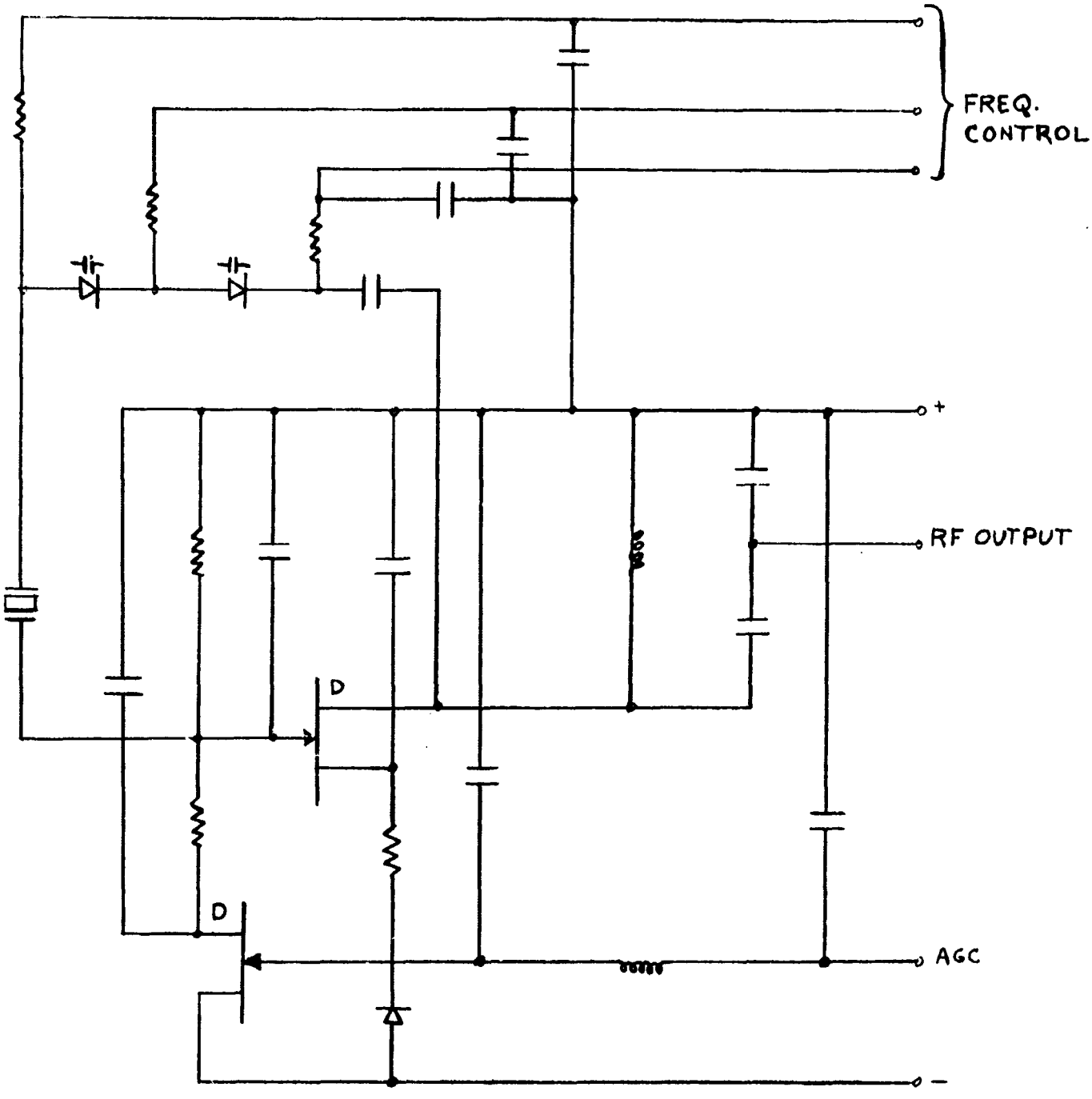


Figure 2-91. Bell Telephone Labs FET Oscillator

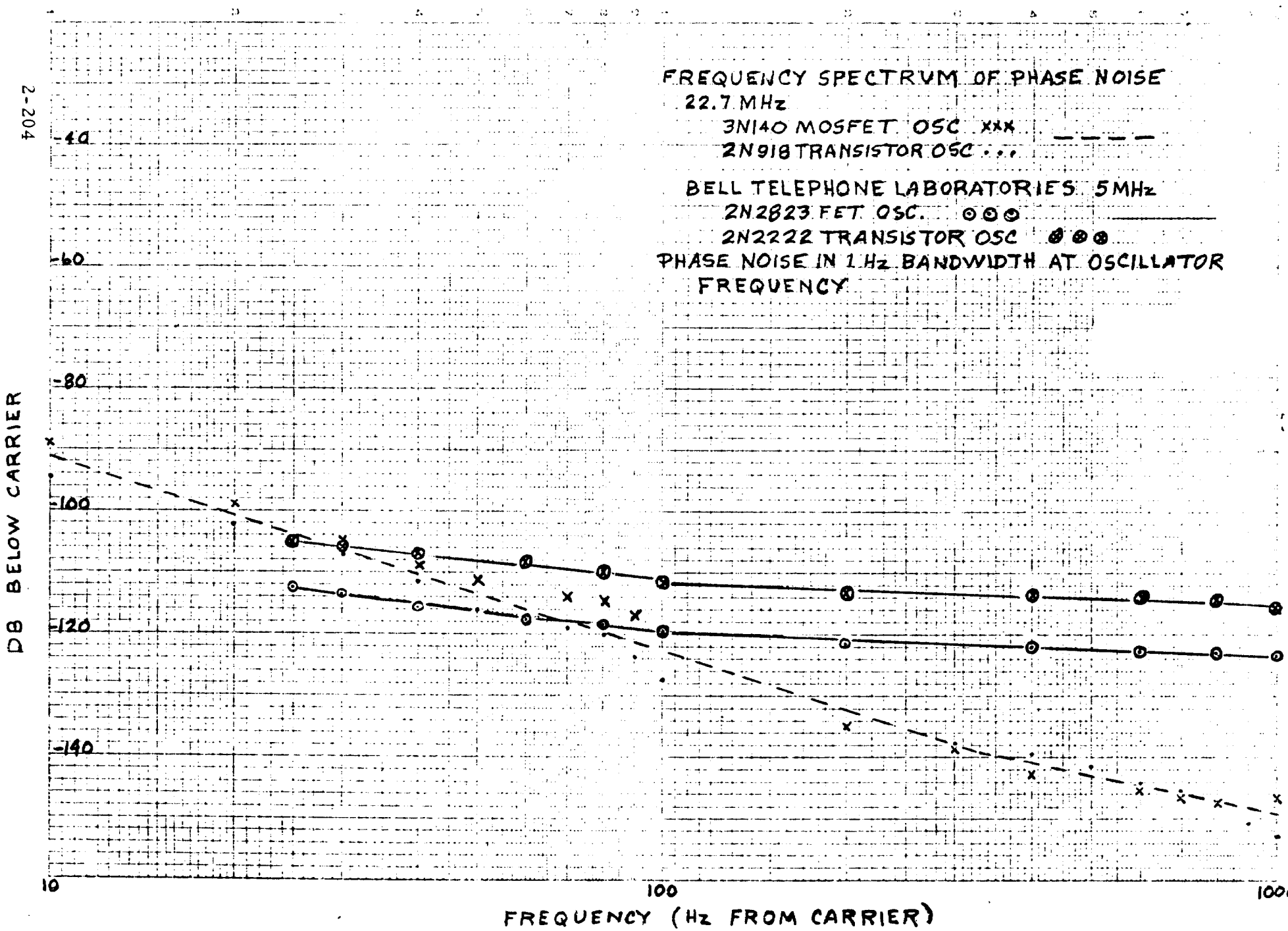

FREQUENCY SPECTRUM OF PHASE NOISE
22.7 MHz
3N140 MOSFET OSC xxx
2N918 TRANSISTOR OSC ...
BELL TELEPHONE LABORATORIES 5MHz
2N2823 FET OSC. ⊙⊙⊙
2N2222 TRANSISTOR OSC ⊗⊗⊗
PHASE NOISE IN 1 Hz BANDWIDTH AT OSCILLATOR FREQUENCY
-40
-60
-80
-100
-120
-140
DB BELOW CARRIER
10
100
1000
FREQUENCY (Hz FROM CARRIER)

Figure 2-92

For a normalized comparison, the Bell Labs oscillator noise can be modified by adding 20 log (22.7/5) db (13 db) to the indicated spectrum level.

A 3.0 MHz crystal oscillator, built at Collins Radio, discussed in item (29) of the bibliography. This oscillator was 0 - 10 db better in the frequency range 20 Hz to 100 Hz from the carrier than both the SGLS 770 Receiver-Demodulator vcxo and the Transmitter Auxiliary Oscillator but 0 - 6 db worse from 100 Hz - 1000 Hz as shown in figure 2-93. Table 2-13 gives a broadband phase noise comparison of the Collins oscillator and all oscillators evaluated during this study. The Collins oscillator is 6.8 db better (broadband basis) than any oscillator evaluated in absolute terms, but is 10.4 db worse than the Motorola oscillators when referred to S-Band.

Table 2-13. Broadband Phase Noise Comparison

Equipment	Phase Noise (Degrees RMS)
Collins 3 MHz Osc.	.00285
SGLS 770 Rcvr-Demod VCXO (19 MHz)	.01929
SGLS 770 Transmitter Aux. Osc. (70 MHz)	.01102
22.7 MHz Trans. Osc.	.00628
22.7 MHz MOSFET Osc.	.01030
70 MHz VCXO	.0143

The phase noise measurements in table 2-13 are all at the actual oscillator frequency.

Table 2-14(a) shows the phase noise frequency spectra of the Collins Radio, Bell Telephone, and all other oscillators evaluated in this study. All phase noise measurements are referred to the actual oscillator frequency. Table 2-14(b) shows the same information normalized to S-Band.

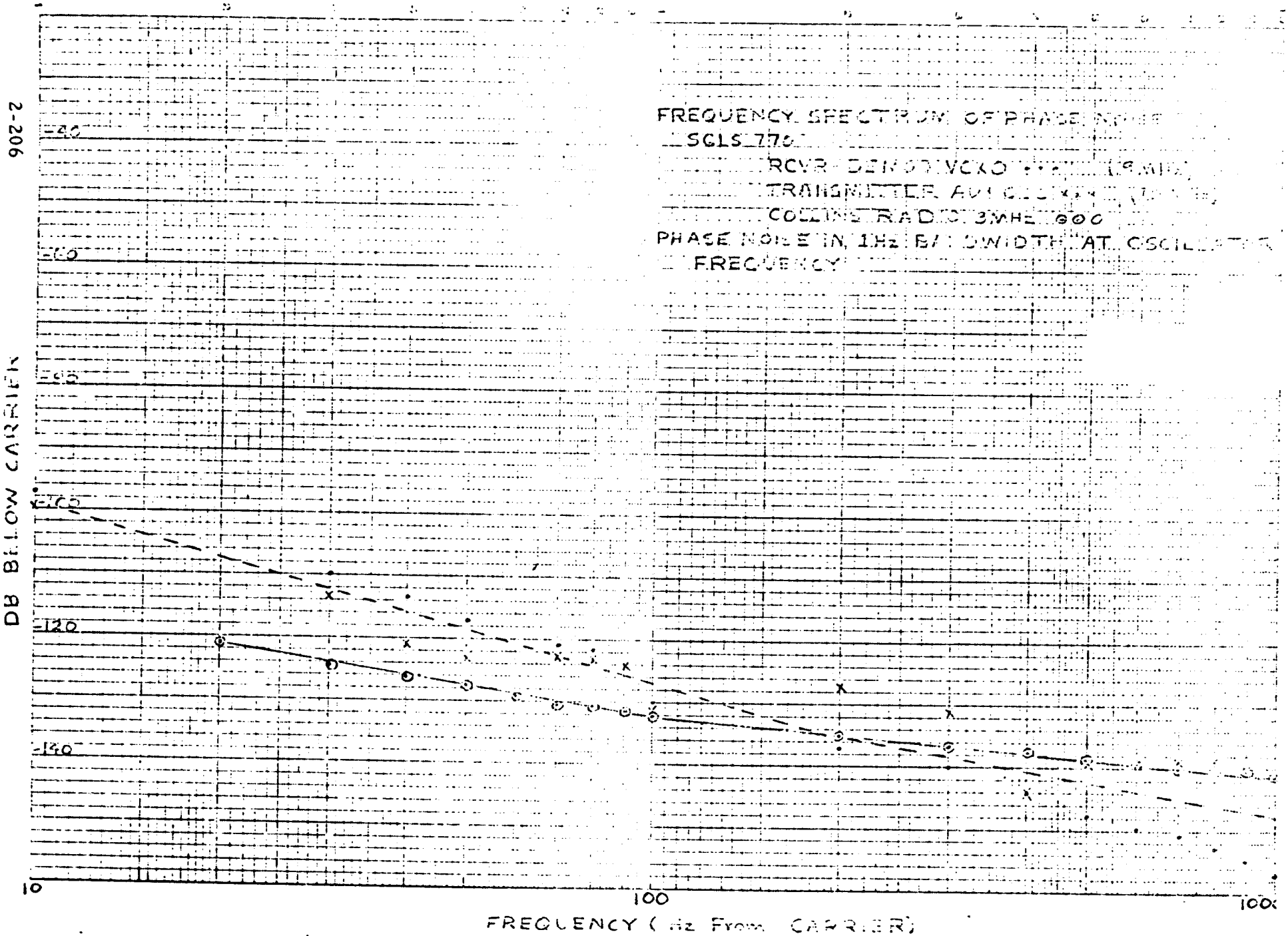

FREQUENCY SPECTRUM OF PHASE NOISE
SGLS 7760
RCVR DEMOD VCXO
TRANSMITTER AUX
COLLINS RADIO 3MHz 000
PHASE NOISE IN 1Hz BANDWIDTH AT OSCILLATOR
FREQUENCY
-40
-60
-80
-100
-120
-140
DB BELOW CARRIER
10
100
1000
FREQUENCY (Hz From CARRIER)

Figure 2-93

Table 2-14(a). Composite Oscillator Spectra (Oscillator Frequency)

Frequency (Hz)	Collins (3 MHz)	Bell Tel. (5 MHz FET)	Bell Tel. (Transistor 5 MHz)	RCVR-DEMOD VCXO (19 MHz)	Transmitter Aux. Osc. (70 MHz)	MOSFET 22.7 MHz	Transmitter 22.7 MHz	70 MHz VCXO
1000	-141	-123.5	-115.5	-157	-141.5	-146.4	-152.6	-168
900	-140.5	---	---	-154.1	-140.3	---	-150.4	-150.4
800	-140.2	-123	-114.5	-152.9	-139.4	-147.8	-147.8	-149.7
700	-140	---	---	-151.0	-139.4	-147.3	-146.2	-162
600	-139.2	-122.5	-114.0	-149.6	-139.8	-145.6	-144.7	-146.4
500	-138.4	---	---	-147.5	-139	---	-141.6	-158.5
400	-137.7	-122	-113.5	-143.9	-144.4	-142.8	-140.1	-138.3
300	-136.5	---	---	-140.4	-131	-138.4	-137.6	---
200	-135.0	-121.5	-113	-137	-127	-134.1	-134.1	-148
100	-132	-119.5	-111.5	-129.6	-131	-119.5	-127.3	-126.2
90	-131.4	---	---	-123.9	-124.2	-116.8	-123.6	---
80	-130.7	-118.5	-110	-122.2	-123.4	-115	-119.9	---
70	-130.2	---	---	-120.7	-123.3	-113.9	-118.6	---
60	-129.1	-117.5	-108.5	---	---	---	---	---
50	-127.6	---	---	-117	-122.6	-111.1	-113.8	-128
40	-126.4	-115.5	-107	-113.5	-120.6	-108.6	-111.3	-123.9
30	-124.4	-113.5	-106	-109.9	-112.9	-105	-106.8	---
25	---	-112.5	-105	---	---	---	---	---
20	-120.9	---	---	-102.9	---	-98.3	-102	- 94.9
10	---	---	---	-97.0	- 99.3	- 88.6	- 94.1	-104.5

All measurements in db below the carrier and are measured in a 1 Hz bandwidth.

Table 2-14(b). Composite Oscillator Spectra (Normalized to S-Band)

Frequency (Hz)	Collins (3 MHz)	Bell Tel. (5 MHz FET)	Bel Tel. (Transistor 5 MHz)	RCVR-DEMOD VCXO (19 MHz)	Transmitter Aux. Osc. (70 MHz)	MOSFET 22.7 MHz	Transmitter 22.7 MHz	70 MHz VCXO
1000	- 84	- 70.5	- 62.5	-115	-111.5	-106.8	-113	-138
900	- 83.5	---	---	-112.1	-110.3	---	-110.8	-120.4
800	- 83.2	- 70	- 61.5	-110.9	-109.4	-108.2	-108.2	-119.7
700	- 83	---	---	-109	-109.4	-107.7	-106.6	-132
600	- 82.2	- 69.5	- 61	-107.6	-109.8	-106	-105.1	-116.4
500	- 81.4	---	---	-105.6	-109	---	-102	-128.5
400	- 80.7	- 69	- 60.5	-101.9	-114.4	-103.2	-100.5	-108.3
300	- 79.5	---	---	- 98.4	-101	- 98.8	- 98	---
200	- 78	- 68.5	- 60	- 95.0	- 97	- 94.5	- 94.5	-118
100	- 75	- 66.5	- 58.5	- 87.6	-101	- 79.9	- 87.7	- 96.2
90	- 74.4	---	---	- 81.9	- 94.2	- 77.2	- 84	---
80	- 73.7	- 65.5	- 57	- 80.2	- 93.4	- 75.4	- 80.3	---
70	- 73.2	---	---	- 78.7	- 93.4	- 74.3	- 79	---
60	- 72.1	- 64.5	- 55.5	---	---	---	---	---
50	- 70.6	---	---	- 75	- 92.6	- 71.5	- 74.2	- 98
40	- 69.4	- 62.5	- 54	- 71.5	- 90.6	- 69	- 71.7	- 93.9
30	- 67.4	- 60.5	- 53	- 67.9	- 82.9	- 65.4	- 67.2	---
25	---	- 59.5	- 52	---	---	---	---	---
20	- 63.9	---	---	- 60.9	---	- 58.7	- 62.4	- 64.9
10	---	---	---	- 55	- 69.3	- 49	- 54.5	- 74.5

All measurements in db below the carrier and are measured in a 1 Hz bandwidth.

2.8.6 Selected References on Crystal Oscillator Noise

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SECTION III
TRANSMITTER

3. INTRODUCTION

The transmitter problems that have been considered fall into three broad areas. First, study and development to provide increased power output; second, improved modulation performance; and third, improved reproducibility of the r-f circuits. Although many other problems and questions can be posed along these lines of consideration, the effort by necessity must be constrained to provide a useful output within the resources allotted.

Results of the evaluation of the transmitter are presented at the end of this section. Selected test results of the various transmitter modules are presented throughout this section. The results of the evaluation of the transmitter with the receiver in a transponder configuration are presented in Section VII of this report. This data is different in that the power output is reduced. This is the result of the attempt to improve the efficiency of the transmitter. It is not felt that this reduced power output affects the results to any significant degree.

3.1 TRANSMITTER TRADE-OFF STUDY

The transmitter configuration was arrived at using trade-off study information. The results of that study are presented in the paragraphs which follow.

Recently, Motorola has developed several high power transmitters operating in the 2200 to 2300 MHz telemetry band. The power amplification has been at 560 MHz with varactor multipliers used to develop the output frequency. With recent improvements in semiconductor devices it now appears feasible to obtain power amplification at higher frequencies.

This trade-off study has been used to determine the actual configuration of power amplifiers and frequency multipliers. To facilitate the trade-off study semiconductor models were selected to provide a basis for implementation of the several transmitter block diagrams.

The data used for the newer S-band devices was discounted from the manufacturer's data. At the lower frequencies newer devices were used as models so that a transmitter with power amplification at 560 MHz would not be penalized from the use of older, less efficient devices. The models used are shown in figure 3-1.

Transmitters of three different power outputs were examined to determine if power output affected the results. The r-f output levels of the transmitters were 20 watt minimum, 23.1 watt typical; 10 watt minimum, 13.2 watt typical; and a 2 watt minimum, 3.3 watt typical. Eight 20-watt, seven 10-watt, and five 2-watt configurations were examined. Block diagrams of the models are shown in figures 3-2 through 3-4, respectively. The r-f drive level was carried back to approximately a one watt level as a stage which would make dissipation equivalent. The dc and r-f power dissipations were then used as a basis for comparison of the efficiency of each configuration. Complexity and common devices such as filters and isolators at the output were disregarded as being irrelevant.

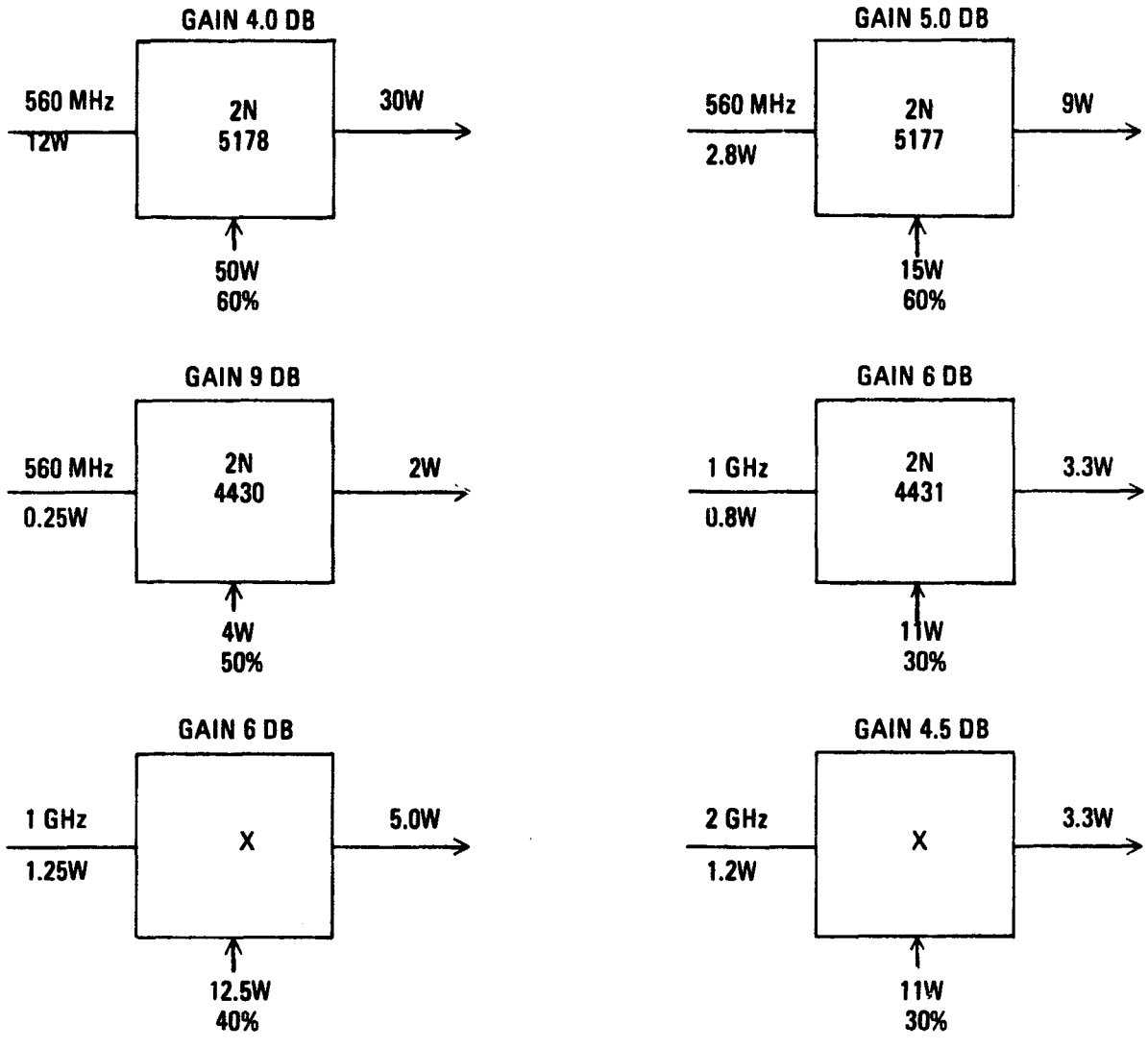
Examination of the block diagrams indicates that power amplification at the output frequency offers the best overall efficiency. Amplification at 1/2 and 1/4 the output frequency offer second and third choices, respectively.

Realistically, the results of this study must be tempered with the availability and reliability of devices. Thus, S-band amplification with their advantages of higher efficiency and smaller size may have to be left for another period in time.

3.2 DESIGN APPROACH

3.2.1 Design Considerations and Approaches

Motorola is currently utilizing stripline techniques for power amplification and multiplication above 400 MHz. Many advantages can be realized from its use, such as production reproducibility at microwave frequencies. However, there exist some drawbacks in its construction, these disadvantages being mainly in component restrictions, such as tuning capacitors, chip dc blocking capacitors,



The varactor multiplier models are shown below:

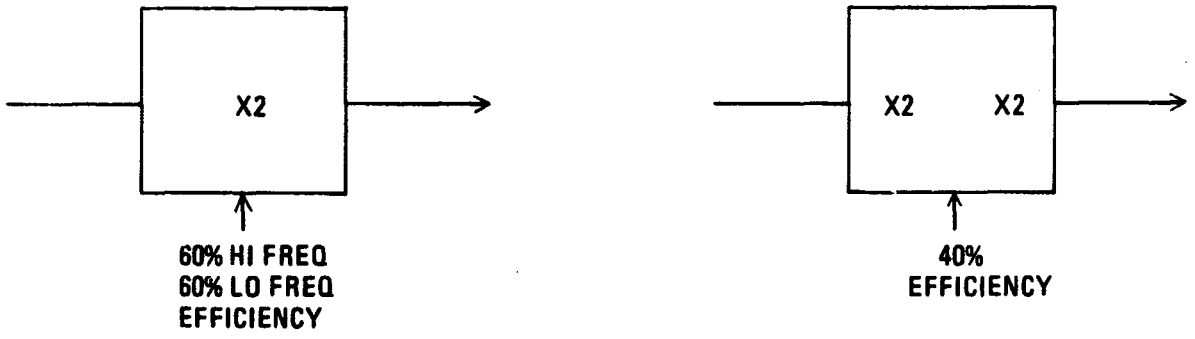


Figure 3-1. Trade-Off Study Semiconductor Models

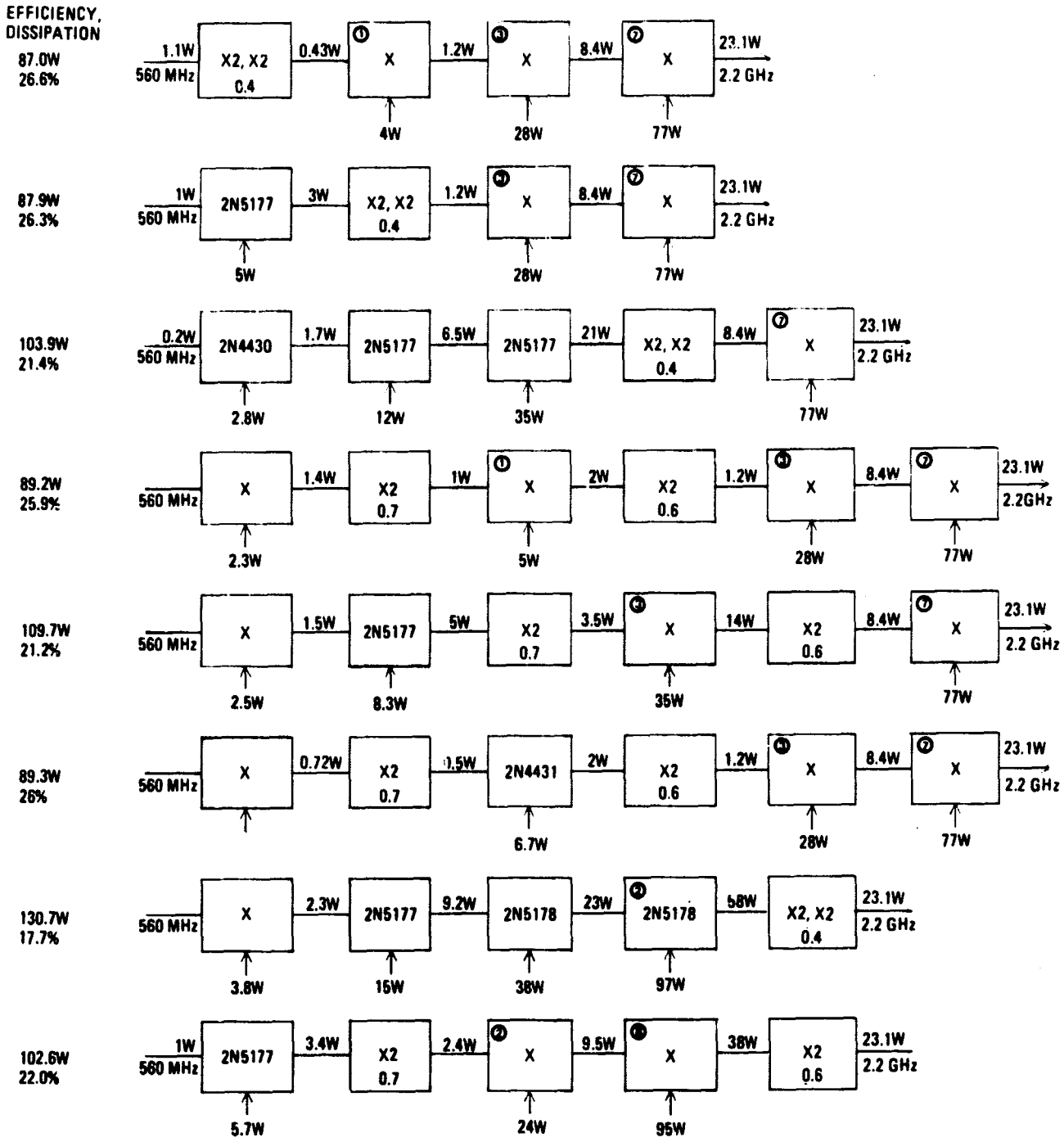


Figure 3-2. 20-Watt Transmitter Trade-Off Study

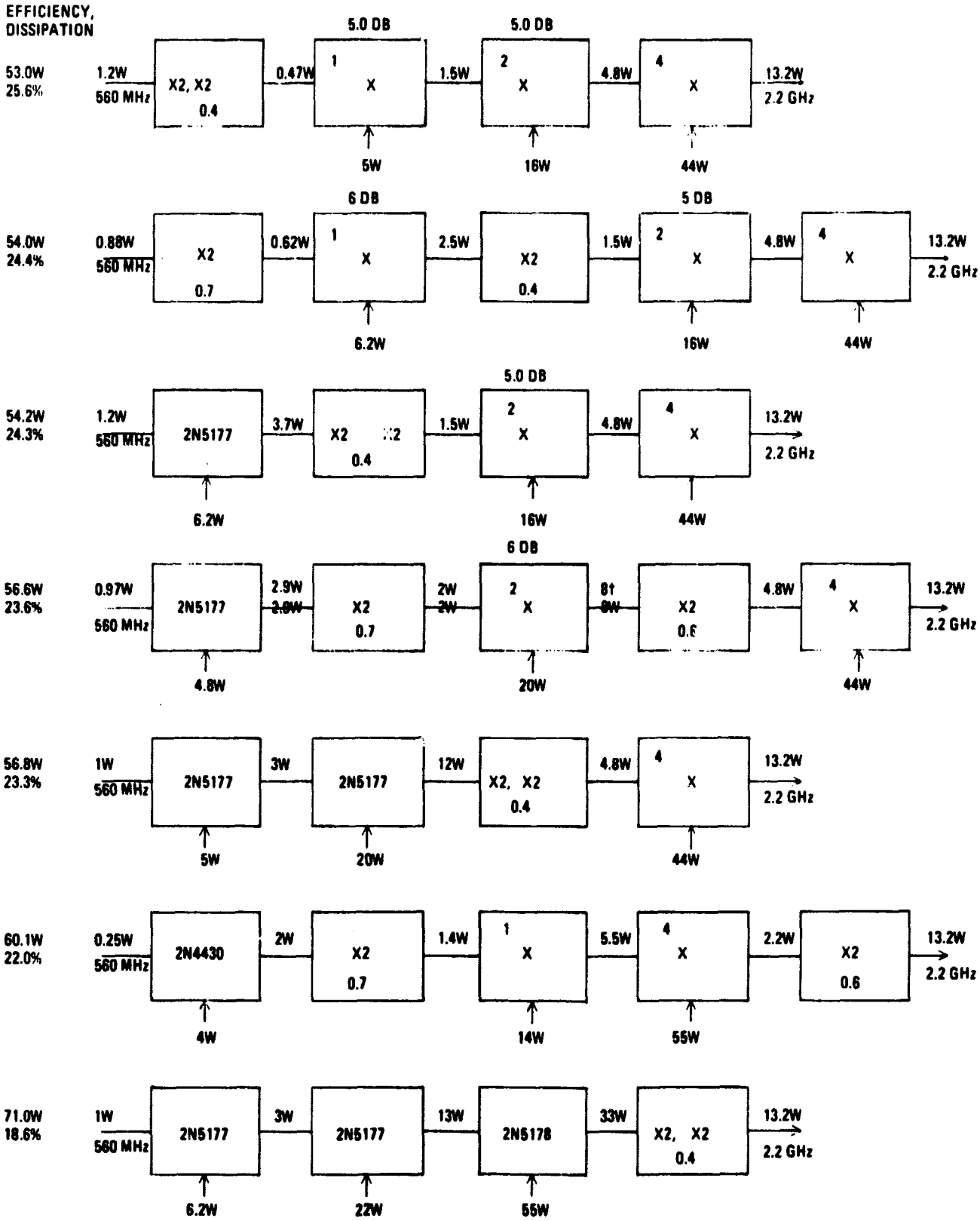


Figure 3-3. Ten-Watt Transmitter Trade-Off Study

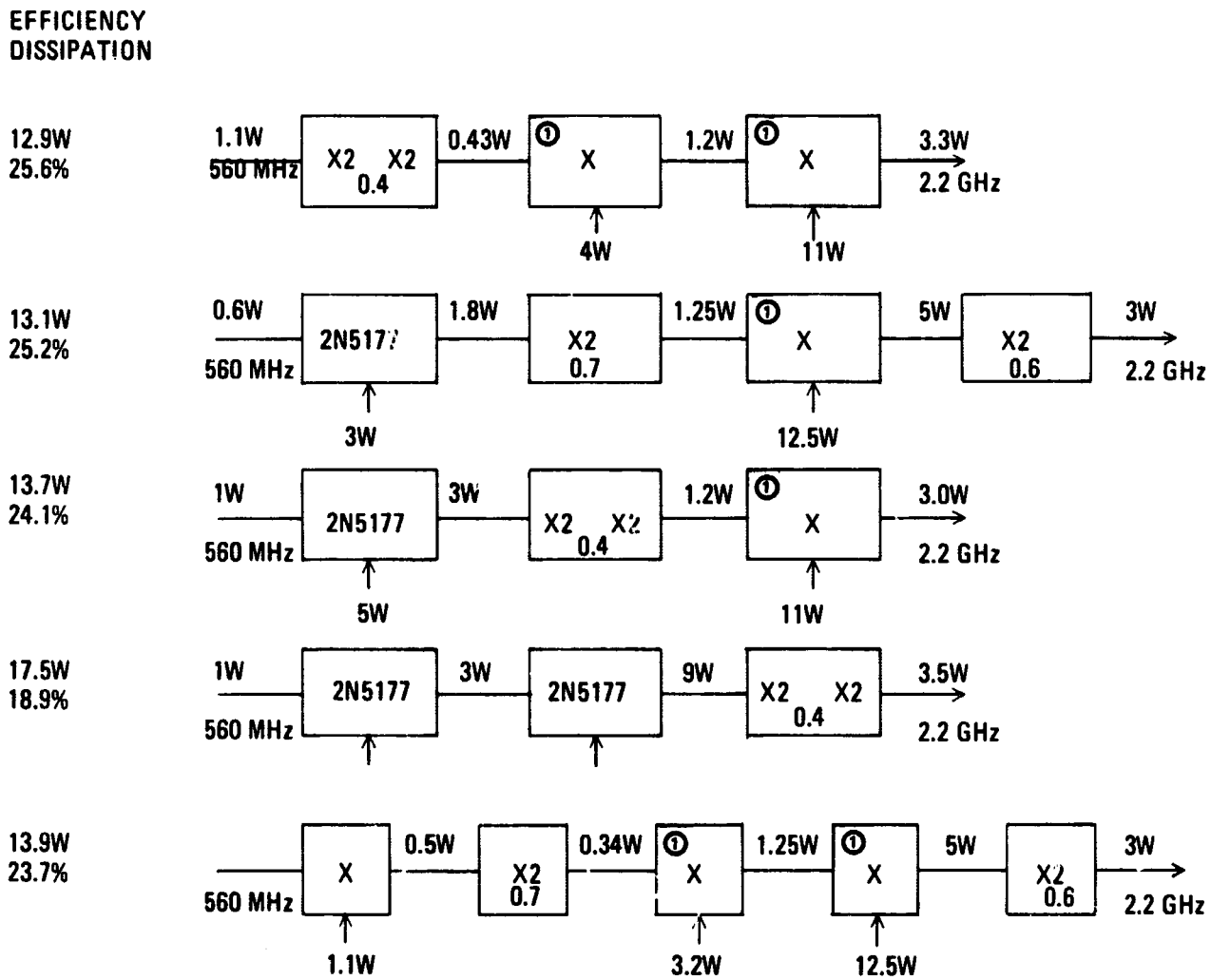


Figure 3-4. 2-Watt Transmitter Trade-Off Study

and board alignment problems. These problem areas were examined on this program in an effort to alleviate these restrictions. A review of promising techniques can be found in the circuit development section of this report.

A study was made to determine what new high power microwave transistors were available in the industry and to determine optimum block diagram utilization of these devices.

From the block diagram study it was determined that if a transistor device could produce a collector efficiency of greater than 40%, power amplification at 1.1 GHz would be practical.

A device under development by TRW had just been released at the beginning of the program. Examination of this device, PT6694, proved to yield power gains of 4.5 to 5 db and equal to, or greater than 45% collector efficiency at 1.1 GHz.

The advantages gained by providing power amplification at 1.1 GHz are: smaller size of stripline networks with attendant reduction in weight, increased power handling requirements over an X2 multiplier at the low frequency, efficient removal of spurious sidebands in the multiplication chain by the resonant networks in the amplifiers, bandwidth can be wider to handle video modulation, and the output filter bandwidth can be greater, thus reducing its insertion loss.

In examining the phase modulation techniques of previous transmitters it was apparent that improvements in this area would be desirable. Ideas formulated previous to the program were evaluated and one was developed into a phase modulator operating at 560 MHz with low distortion and sensitivity variations.

With the selection of the frequency for power amplification, and the frequency appropriate for the phase modulator, the output power requirements were next investigated.

A design goal of 18 watts output was selected based on a power amplifier of four summed transistors at 1125 MHz which would supply 26 watts. The use of a summed power amplifier forced into the design for the development of circuit

techniques that would provide even higher power outputs with a minimum of new development. This combined with a varactor multiplier of 70% efficiency would provide the final output at 2250 MHz.

The phase modulator development pointed to 560 MHz operating frequency in a stripline configuration.

From the receiver a synthesized frequency, 70 MHz, would be provided with a resultant overall transmitter multiplication of 32.

To provide a good interface with the modulator a low level 560 MHz amplifier and a low level X2 varactor multiplier would drive the power amplifier chain. This requires X8 multiplication from the 70 MHz input to provide 560 MHz to the modulator.

Based on this study, the block diagram of figure 3-5 was set forth. As explained elsewhere in this report the power levels indicated on this block diagram were not achieved in the actual breadboard system. Three stages of amplification drive a step diode X8 multipler. To remove the combline generation of 70 MHz sidebands, a four pole combline filter was utilized with a bandwidth of 28 MHz for filtering the output.

To interface with the stripline phase modulator, it was found later in the program that the multiplier provided a source impedance which had large variations over the temperature range. To alleviate this problem an isolator was installed at the output of the combline filter. The isolator proved successful in providing a good isolation so that the modulation index was not effected.

The phase modulator and 560 MHz low level amplifier drive a X2 single diode varactor multiplier. The major part of the power amplification thus takes place at 1125 MHz by means of a single driver splitting the power to two parallel drivers which in turn provide dual power to two sets of power amplifiers.

The high power is combined in the X2 high power, dual device, varactor multiplier. A filter with low insertion loss, wide bandwidth, and construction to relieve corona breakdown under critical pressure was designed to be used at the output.

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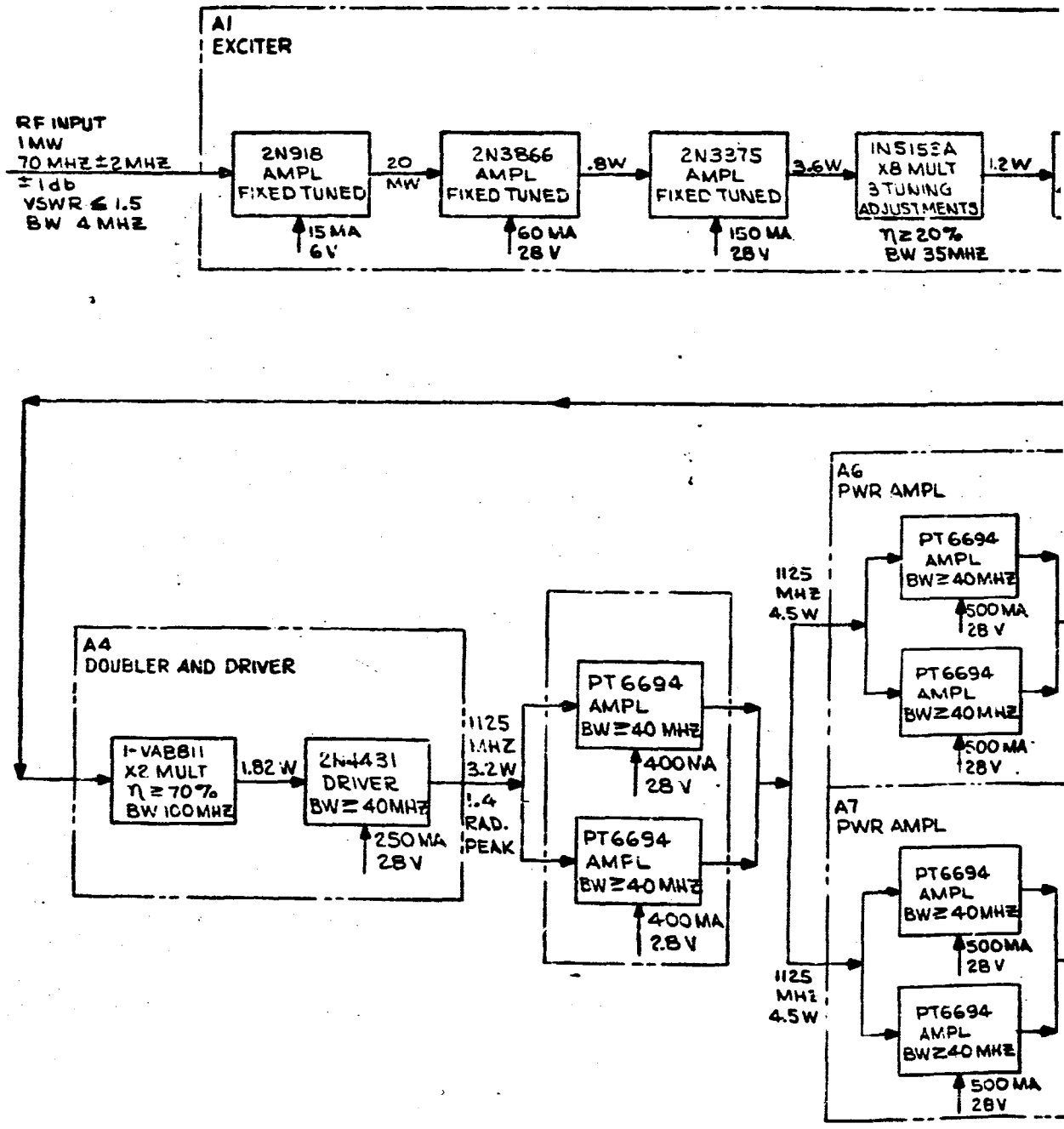
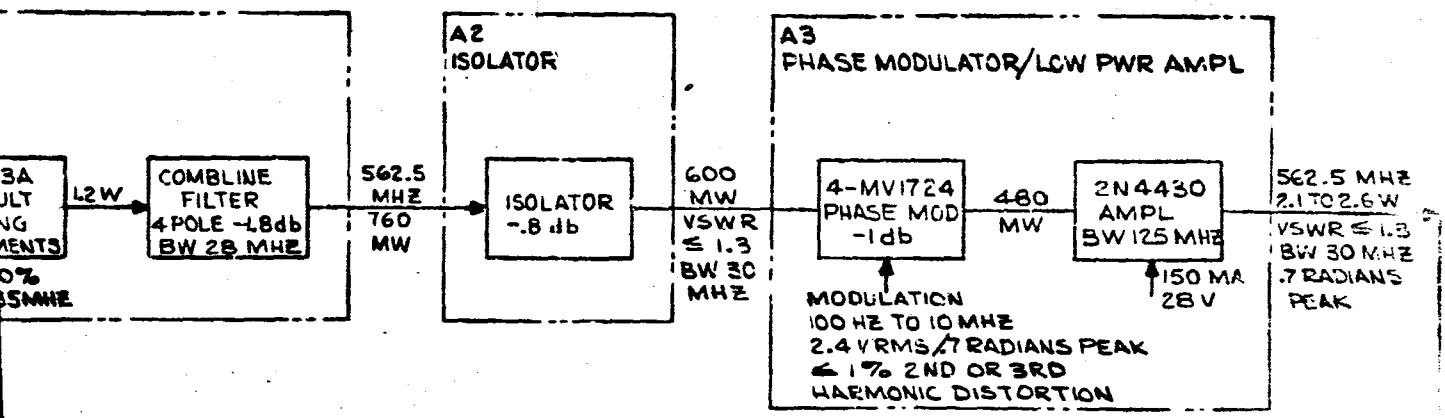
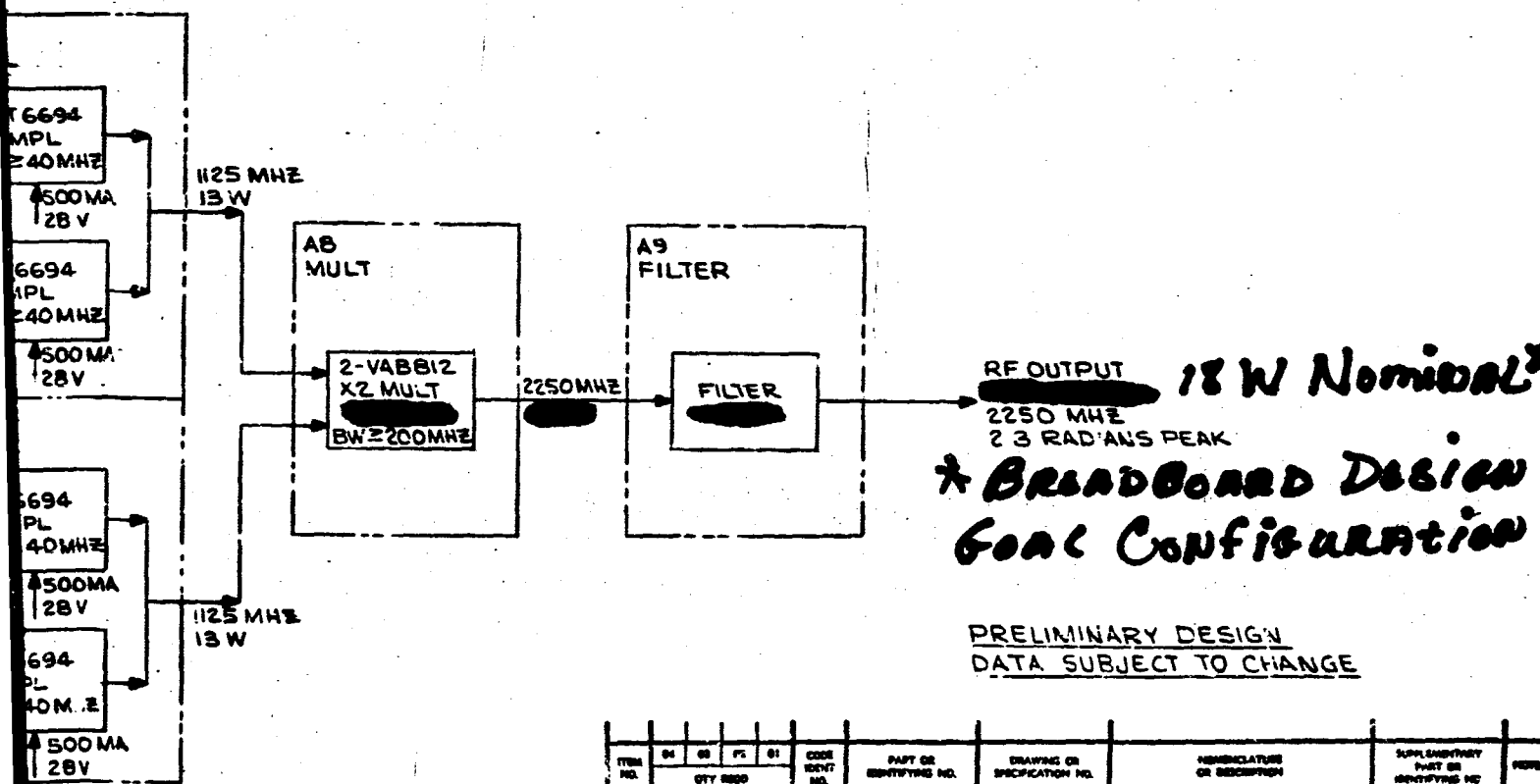


SYM	REV	QTY

HOLE LIST

REVISIONS				
LTR	LTR	DESCRIPTION	DATE	APPROVED
	X1	REVISED IN DRIVER AND PWR AMPL AREA, REVISED PWR VALUE	6/11/68	





PRELIMINARY DESIGN
DATA SUBJECT TO CHANGE

ITEM NO.	QTY REQD	CODE IDENT NO.	PART OR IDENTIFYING NO.	DRAWING OR SPECIFICATION NO.	NOMENCLATURE OR DESCRIPTION	SUPPLEMENTARY PART OR IDENTIFYING NO.	NOTES

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

FOR PARTS LIST SEE

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND END USE SURFACE FINISH
TOLERANCES: TWO PLACE DEC ± ✓ THREE PLACE DEC ± ANGLES ± HOLE DIA +

DRAWN C. HUTTO 5 MAY 68
CHK BY
APVD
PROJ NO. 3 33
CONTRACT NO
RELEASED DATE

MOTOROLA INC. Government Electronics Division / Aerospace Center 8201 East McDowell Road Scottsdale, Arizona

Figure 3-5.
S-BAND TRANSMITTER
(BLOCK DIAGRAM)

NEXT ASSEMBLY	USED ON
★ APPLICATION	

APPROVED NAME DATE
APPROVED NAME DATE

SIZE D | CODE IDENT NO. 94990 | 69-22458M
SCALE NONE | WEIGHT | SHEET

3.3 COMPONENT DEVELOPMENT

The following paragraphs describe circuit components developed during the course of the program. It was from these components that the functional circuits were developed.

3.3.1 3 DB Hybrid Designs

The design, investigation, and results of a study to eliminate registration errors in 3 db hybrid couplers is described below.

3.3.1.1 Design

The first approach was to try a method whereby two lines would be printed on one board and coupling would be to a common conductor placed over the two lines. This scheme is shown in figure 3-6.

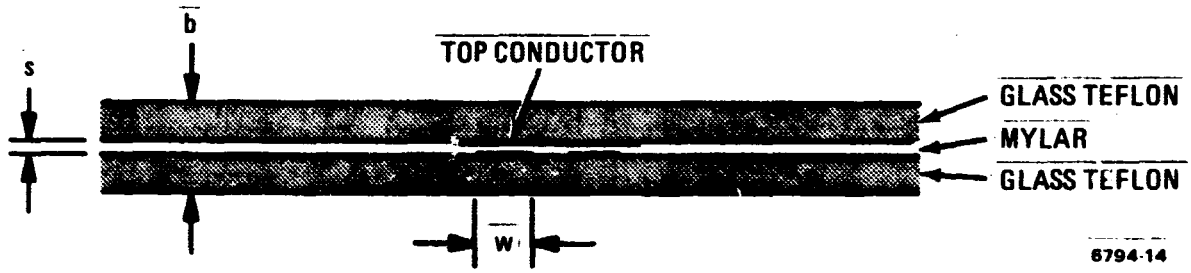


Figure 3-6. Stripline Coupling Configuration

In order to alleviate registration errors the top conductor overlapped the parallel lines on each side. This allowed the top board to move and still maintain the proper coupling.

As a first approximation assume there is a 1.5 db loss from the first line to the upper conductor and another 1.5 db loss from the upper conductor to the second line. Using papers by Cohn[1] and Jones and Bolljohn[2] we find the coupling coefficient is given by

1. S. B. Cohn, "Characteristic Impedances of Broadside-Coupled Strip Transmission Lines," IRE Transactions on Microwave Theory and Techniques, November, 1960.

$$k = \frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}} \quad \text{where } Z_{oe}\, Z_{oo} = Z_o^2 \tag{2}$$

For a 1.5 db coupler k = .84

Solving the above equations we have

Z_{oe} = 170 ohm

Z_{oo} = 14.7 ohm

Now from "Cohn's" paper

$$Z_{oe} = \frac{188.3/\sqrt{Er}}{\frac{W/_b}{1 - s/_b} + C^1 fe/E} \tag{1}$$

Assume s/b = 0.50 and from figure 3.0 in the article

$$c_{fe/E} = .50\, c_{fo/E} = 1.40$$

Solving equation(1) for $W/_b$ we get

$$W/_b = .175 - .175\, s/_b$$

A plot of this equation is made such that

$s/_b$ =	.02	.04	.06	.08	.10
$W/_b$ =	.172	.167	.164	.161	.157

Also solving for $W/_s$ by dividing $W/_b$ by $s/_b$ we get

$s/_b$ =	.02	.04	.06	.08	.10
$W/_s$ =	8.6	4.20	2.74	2.01	1.57

---

2. E. M. T. Jones and J. T. Bolljohn, "Coupled-Strip-Transmission-Line Filters and Directional Couplers," IRE Transactions on Microwave Theory and Techniques, April, 1956.

The second of "Cohn's" equations is

$$Z_{oo} = \frac{188.3}{\sqrt{E_1}\left(\frac{w/_b}{1 - s/_b}\right) + \sqrt{E_2}\left\{\frac{W}{s} + \frac{C_{fo}}{E}\right\}} \qquad (2)$$

where E_1 is the dielectric constant of the glass teflon board and E_2 is the dielectric constant of the mylar spacer.

Substituting the quantities obtained from equation (1) into equation (2) we find that for

$s/_b =$ .02 .04 .06 .08 .10

$Z_{oo} =$ 11.3r 19.8r 33.6r 53.1r 61.3r

A plot of $w/_b$ versus $s/_b$ and also a plot of Z_{oo} as a function of $s/_b$ are combined on one graph and is shown in figure 3-7. As was calculated previously the required Z_{oo} is 14.7 ohms. From this we find

$s/_b \cong .028$ and $w/_b \cong .166$

Therefore b = .121

W= .021 and s = .0032

A unit was built with a line width of .021 and a mylar spacer of 3.5 mils. The two lines were spaced .020 mils apart so that mutual coupling would not affect the performance. The top conductor was made so that it overlapped the lines on each side by .010 inches.

A second method of improving the registration of couplers was to use the old coupler design (i.e. offset design) but not print the coupler on the circuit boards, but have the unit printed on the spacer separating the coupling elements. Small drop-in units could be built where registration was already accomplished during etching.

The design of this type of coupler is similar to the design procedure covered above except for 3 db, k becomes $1/\sqrt{2} = .707$.

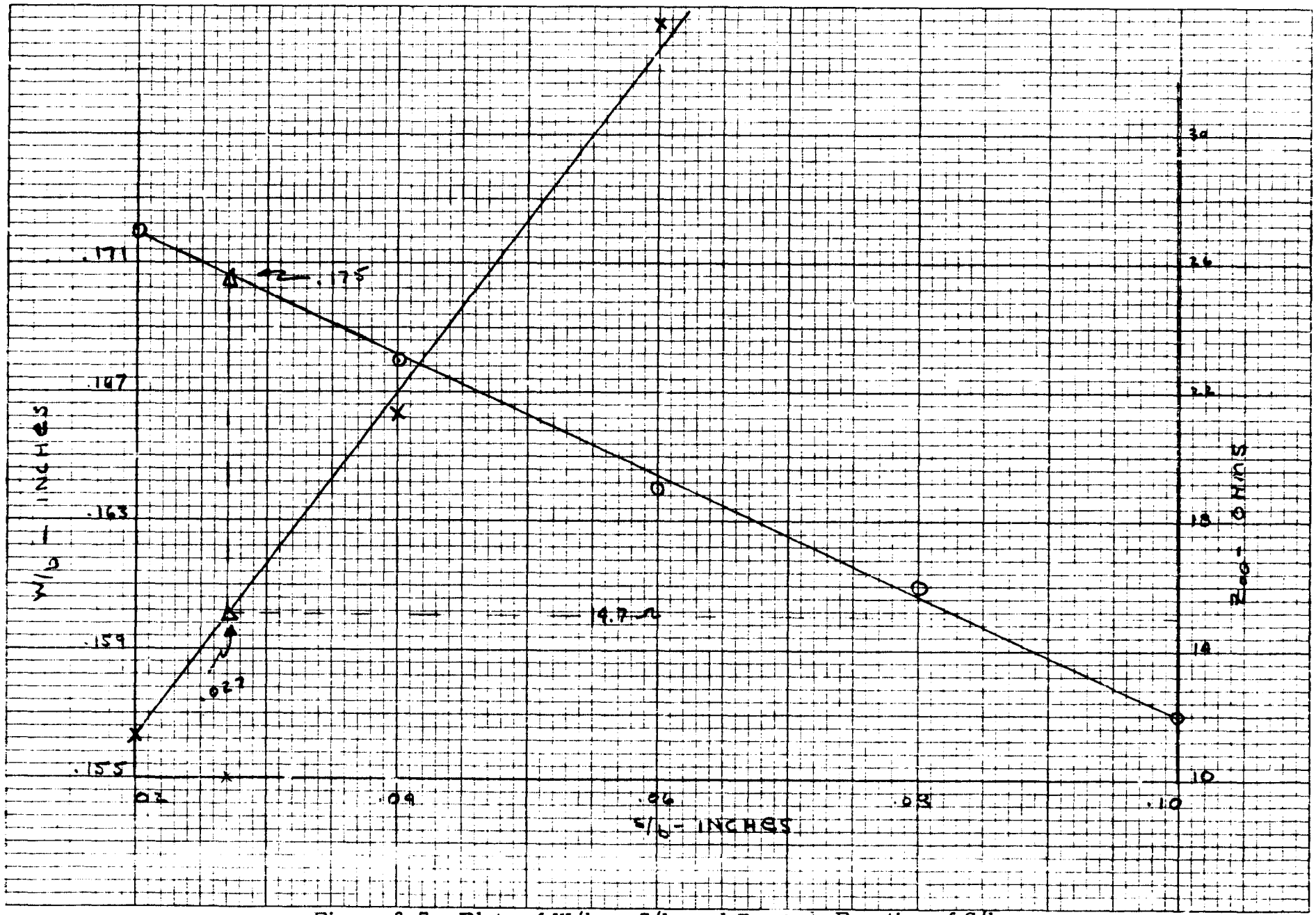


Figure 3-7. Plots of W/b vs S/b; and Z_{00} as a Function of S/b

Therefore;

Z_{oe} = 120.9 ohm

Z_{oo} = 20.7 ohm

Using the same calculations we get the following dimensions

S = .013" W = .042"

Since a .013" spacer is not available, an offset in the coupling elements is required. For a spacer of .010", the offset is .014". This unit is displayed pictorially in figure 3-8.

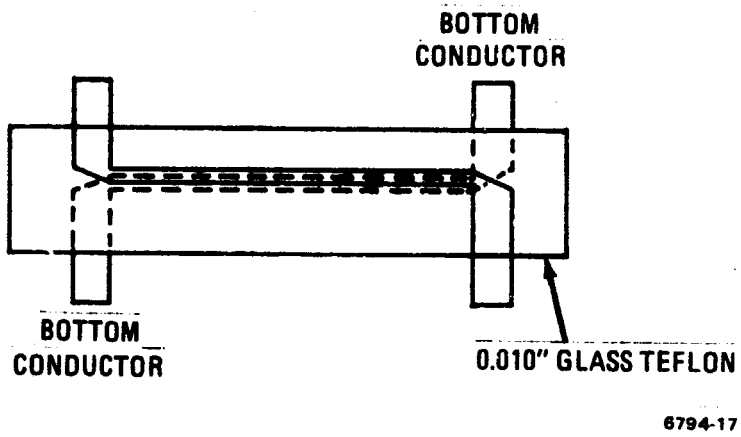


Figure 3-8. Drop in Coupler

3.3.1.2 Data

A breadboard of each unit was built and tested. Data was taken to show coupling, input vswr, and isolation as a function of frequency. For the single sided overlap coupler this data is shown in figures 3-9 and 3-10. The same data for the drop in coupler is shown in figure 3-11 and 3-12. A calculation of total power summed was performed at three frequencies 2200, 2250, and 2300. A tabulation of this data is shown in figure 3-13 (see figure 3-14 for port designations).

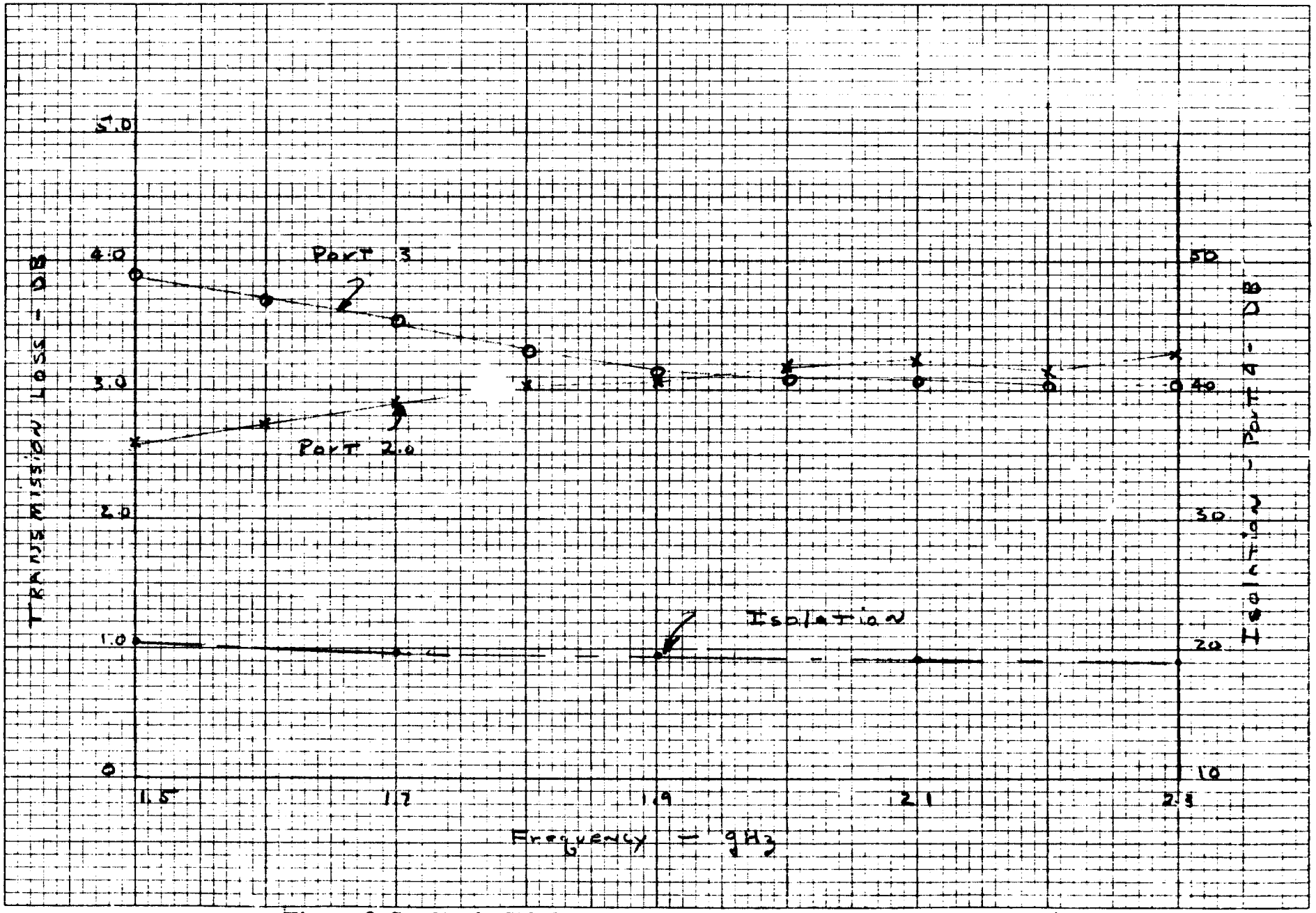


Figure 3-9. Single Sided Overlap Coupler-Coupling Characteristics

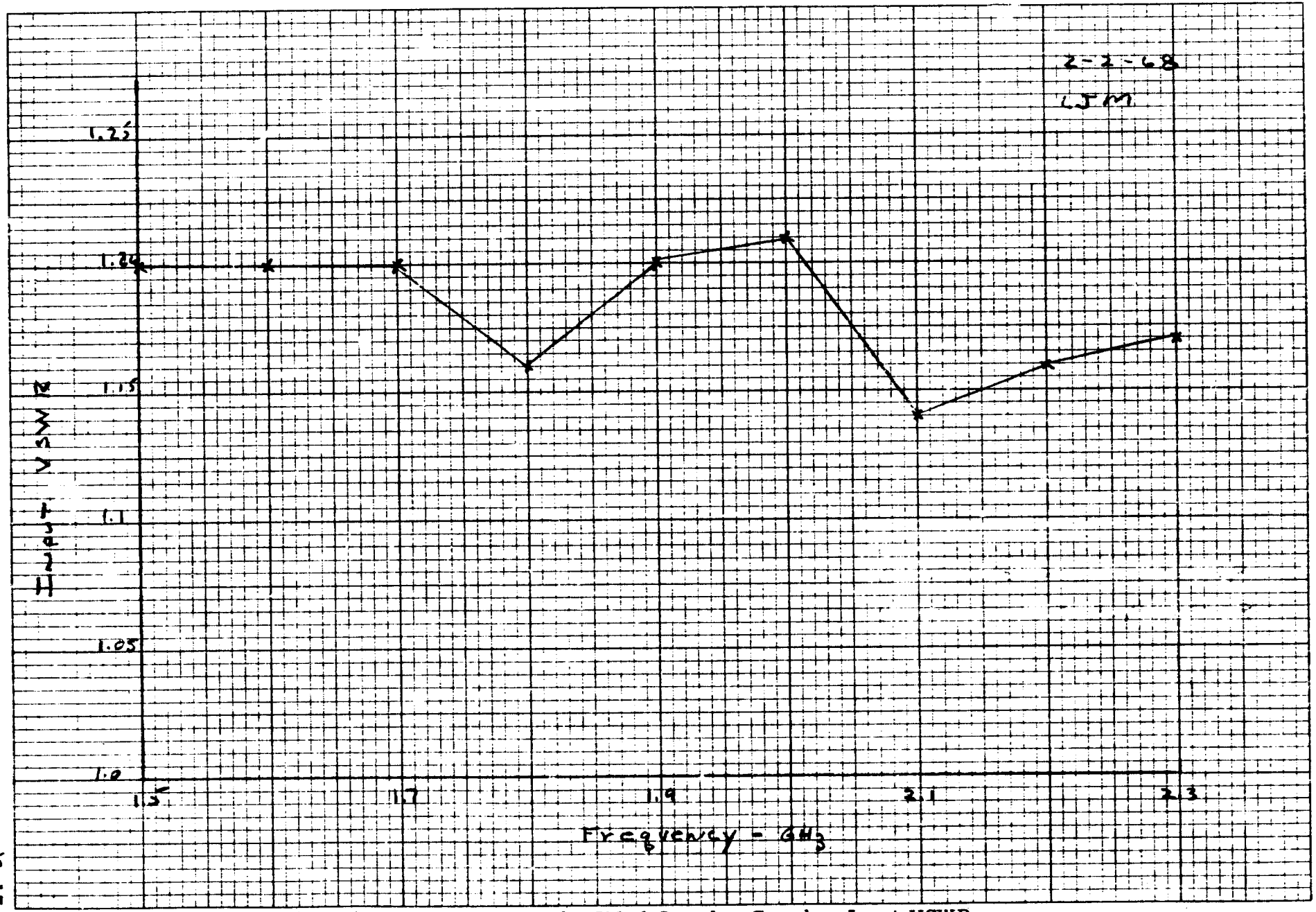


Figure 3-10. Single-Sided Overlap Coupler-Input VSWR

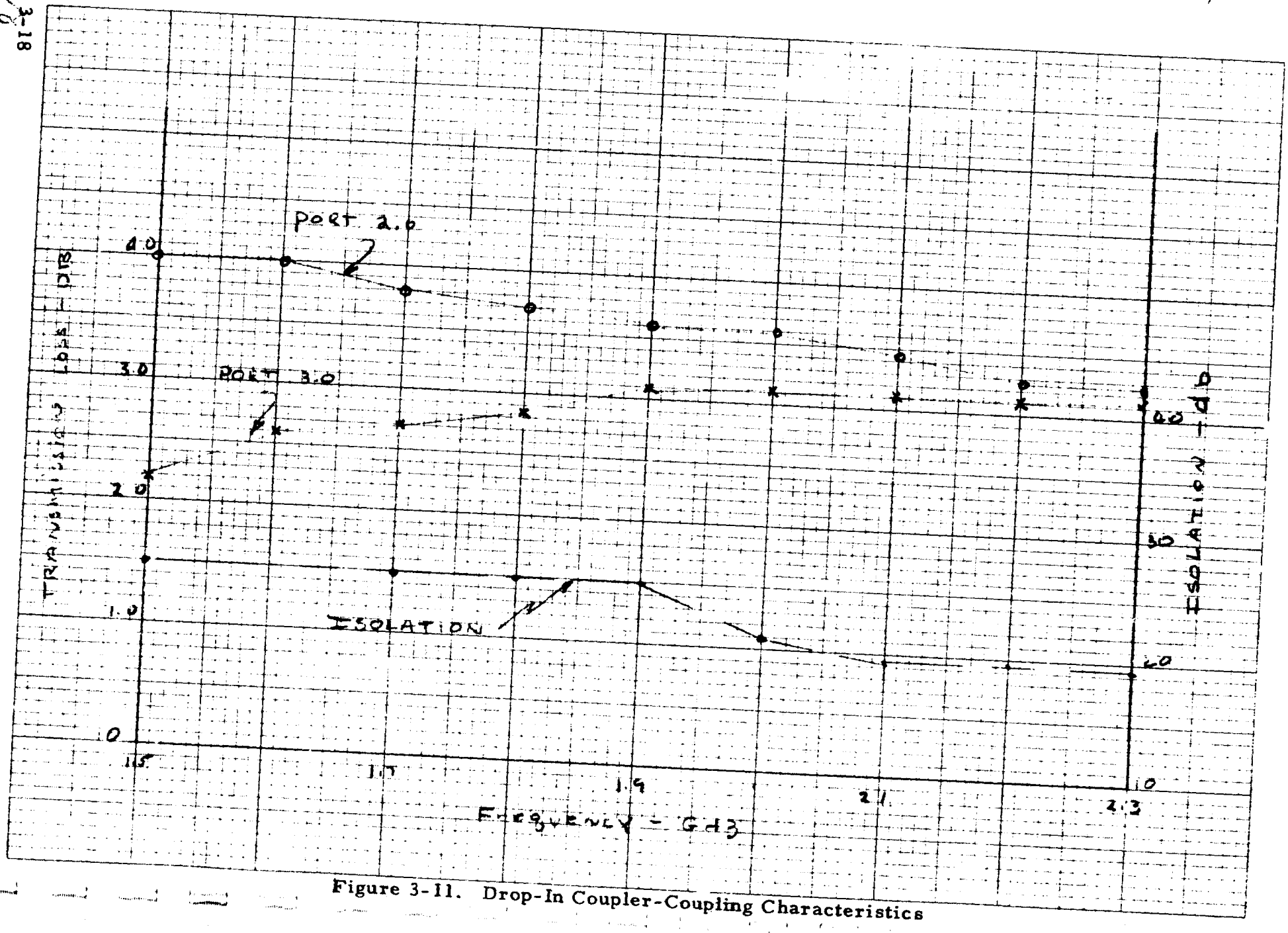


Figure 3-11. Drop-In Coupler-Coupling Characteristics

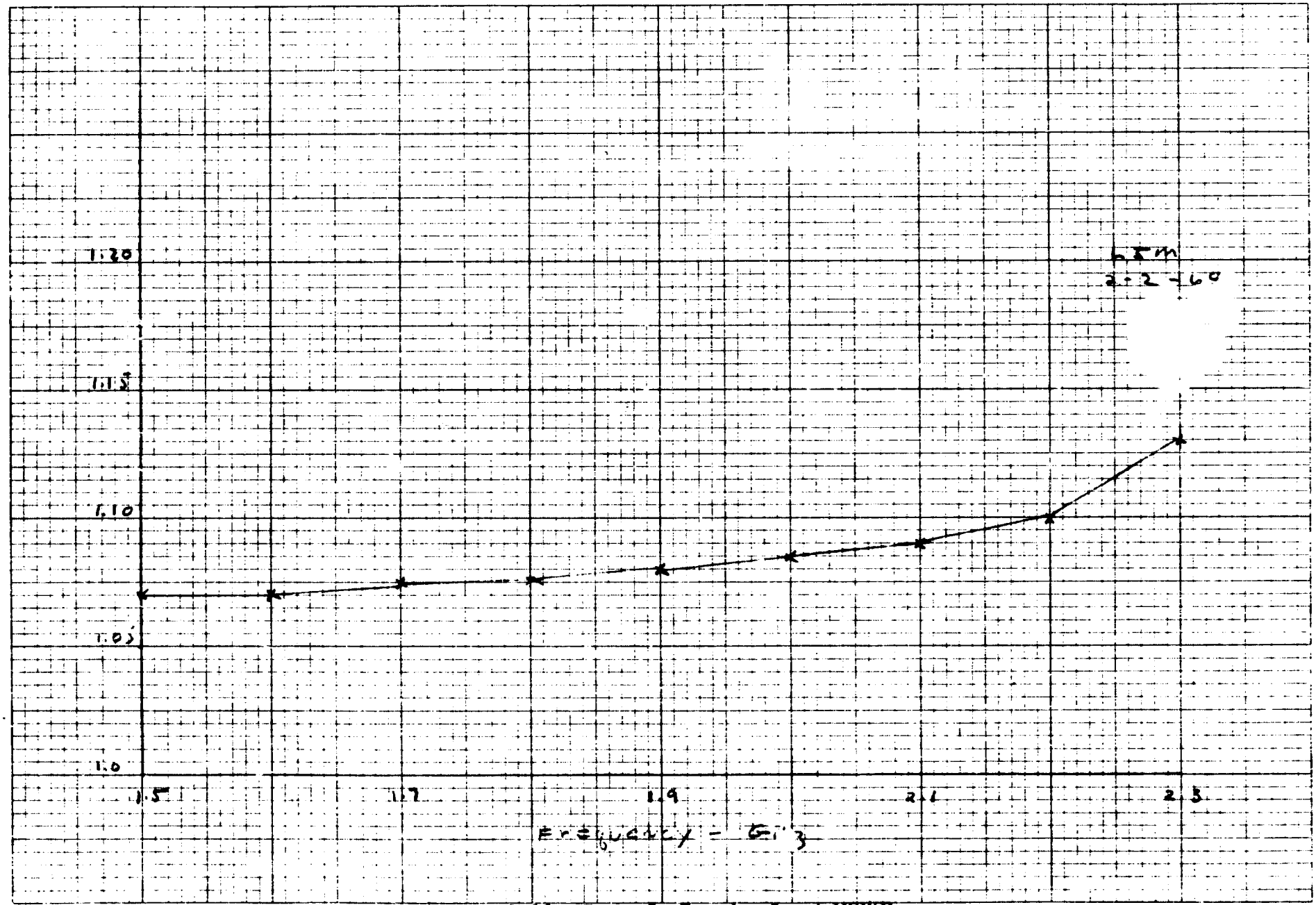


Figure 3-12. Drop-In Coupler Input VSWR

Freq. GHz	Transmission Loss - Port 2.0	Transmission Loss - Port 3.0	Power Transmitted Port 2.0	Power Transmitted Port 3.0	Total Power Transmitted	Total Transmission Loss
2.2	3.20	3.35	48%	46.5%	94.5%	.235 db
2.25	3.20	3.30	48%	47%	95%	.22 db
2.3	3.20	3.30	48%	47%	95%	.22 db

Single-Side Overlap Coupler-Transmission Characteristics

Freq. GHz	Transmission Loss - Port 3.0	Transmission Loss - Port 4.0	Power Transmitted Port 2.0	Power Transmitted Port 3.0	Total Power Transmitted	Total Transmission Loss
2.2	3.25	3.15	47.5%	48.5%	96%	.175 db
2.25	3.30	3.25	47%	47.5%	94.5%	.245 db
2.3	3.30	3.25	47%	47.5%	94.5%	.245 db

Drop In Coupler-Transmission Characteristics

Figure 3-13. Coupler-Transmission Characteristics

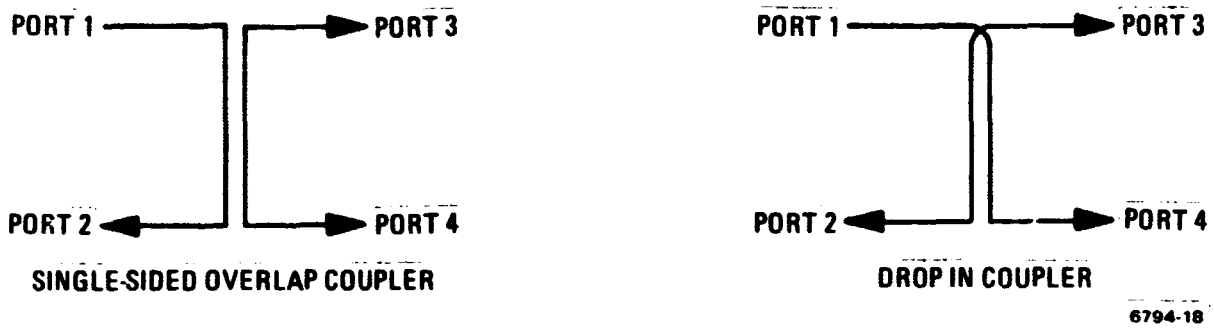


Figure 3-14. Coupler Port Designations

3.3.1.3 Conclusion

Performance of the two types of couplers was very much similar, however, for the single-sided overlap coupler the coupling was very sensitive to dielectric thickness (i.e. at 2200 MHz the following data was taken: with a 3.5 mil spacer, port 2 was down 2.70 db and port 3 was down 4.0 db. However, with a 2.5 mil spacer, port 2 was 3.3 db down and port 3 was 3.2 db down). As can be seen the coupling changes drastically with about a 1.0 mil change in the dielectric spacer. The drop-in coupler appears to be the superior design in that it is not squeeze sensitive and registration is no longer a problem.

3.3.2 Printed Inductors

These paragraphs cover the investigation of printed inductors which are to be used at S-band to isolate dc inputs from r-f circuits.

Several types of distributed parameter inductors, using stripline techniques, were tried to obtain a wideband r-f choke to be used to block r-f at the collector of a transistor amplifier stage. This concept would then allow lumped elements to be placed on the outside of a module and insure amplifier stability. Several configurations which were tried are shown in figure 3-15.

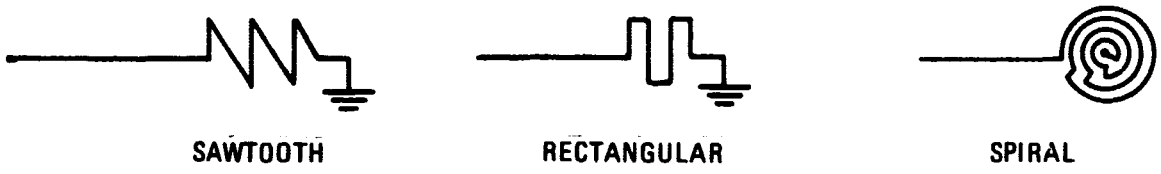


Figure 3-15. Types of Distributed Inductors

The spiral was wound as tight as printing practice would allow, thereby obtaining as much inductance as possible. Using the equations for low frequency inductors[1]

$$h = \frac{a^2 n^2}{8a + 11c} \qquad (1)$$

where $a = (ro + ri)/2$ $c + 40 - ri$

where ro and ri are shown in figure 3-16

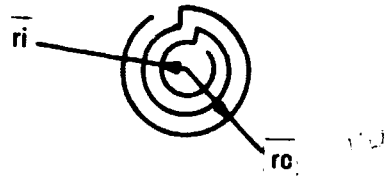


Figure 3-16. Spiral Inductor

Equation (1) assumes that the spiral is wound tightly enough so that mutual inductance is realizable. Dimensions such that conductor widths of 2.5 mils and conductor spacings of 1.5 mils are required. If the inductor is wound too loosely the unit will act merely as a shorted transmission line.

1. F. W. Grover, "Inductance Calculations," D. Van Nostrand Company, Inc., 1946.

Another method which could be used to simulate an inductor is to use the out band impedance of a low pass filter section. The impedance plot is shown in figure 3-17.

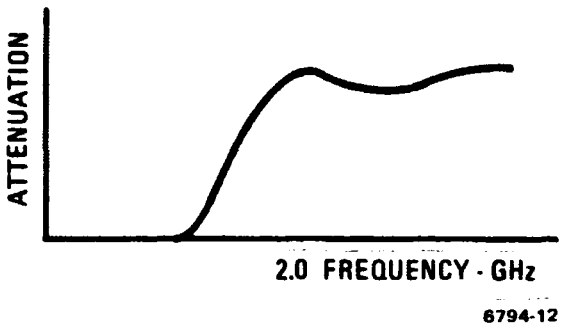


Figure 3-17. Low Pass Filter Impedance Plot

This would present a high impedance at 2 GHz when using the out band portion of the attenuation curve. In order to control the dc input side of the filter the unit was designed with a short in the output. This could be replaced with an open circuited $\lambda/4$ length of line so that dc could be applied to the collector. A drawing of the configuration is in figure 3-18.

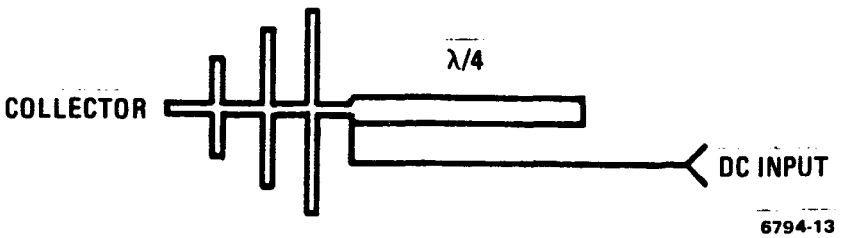


Figure 3-18. Shorted Collector Output

As a first approximation the unit was designed with equal length element as a low pass filter (see reference 2. for design equations). Then in order to broad band the unit the elements were tapered and adjusted. It was found that if the element

lengths were adjusted properly the unit went through a series resonance at 2.25 GHz. The unit was then programmed on the computer using the element lengths empirically obtained above.

3.3.2.1 Test Data

Each type of distributed inductor shown in figure 3-15 was tested over a frequency range from 2.0 to 2.4 GHz and plotted on Smith Charts. The data taken for the saw tooth inductor is shown in figure 3-19, for the rectangular design in figure 3-20, and for the spiral configuration the data is shown in figure 3-21.

For the out band filter type design, the data is plotted in figure 3-22. The theoretical computer design is also plotted in the same figure as a comparison.

3.3.2.2 Conclusion

An inspection of figures 3-19 and 3-20 leads to the conclusion that the units are not acting as inductors, but as shorted lengths of transmission line. The spiral of figure 3-21 has some of the qualities of a good r-f choke, low Q, and high reactive component in the frequency range of interest. However, the unit exhibits a wide-band characteristic not suitable for amplifier use. The outband filter type (figure 3-22) has a series resonance at 2.25 GHz, has a high series R, and a high reactive component in the range from 2.2 GHz to 2.3 GHz. This unit can then cover the frequency range and still maintain good r-f choke qualities.

3.3.3 Variable Capacitors and Tuning Devices

This paragraph covers the design and testing of several types of tuning devices which can be used with stripline circuitry.

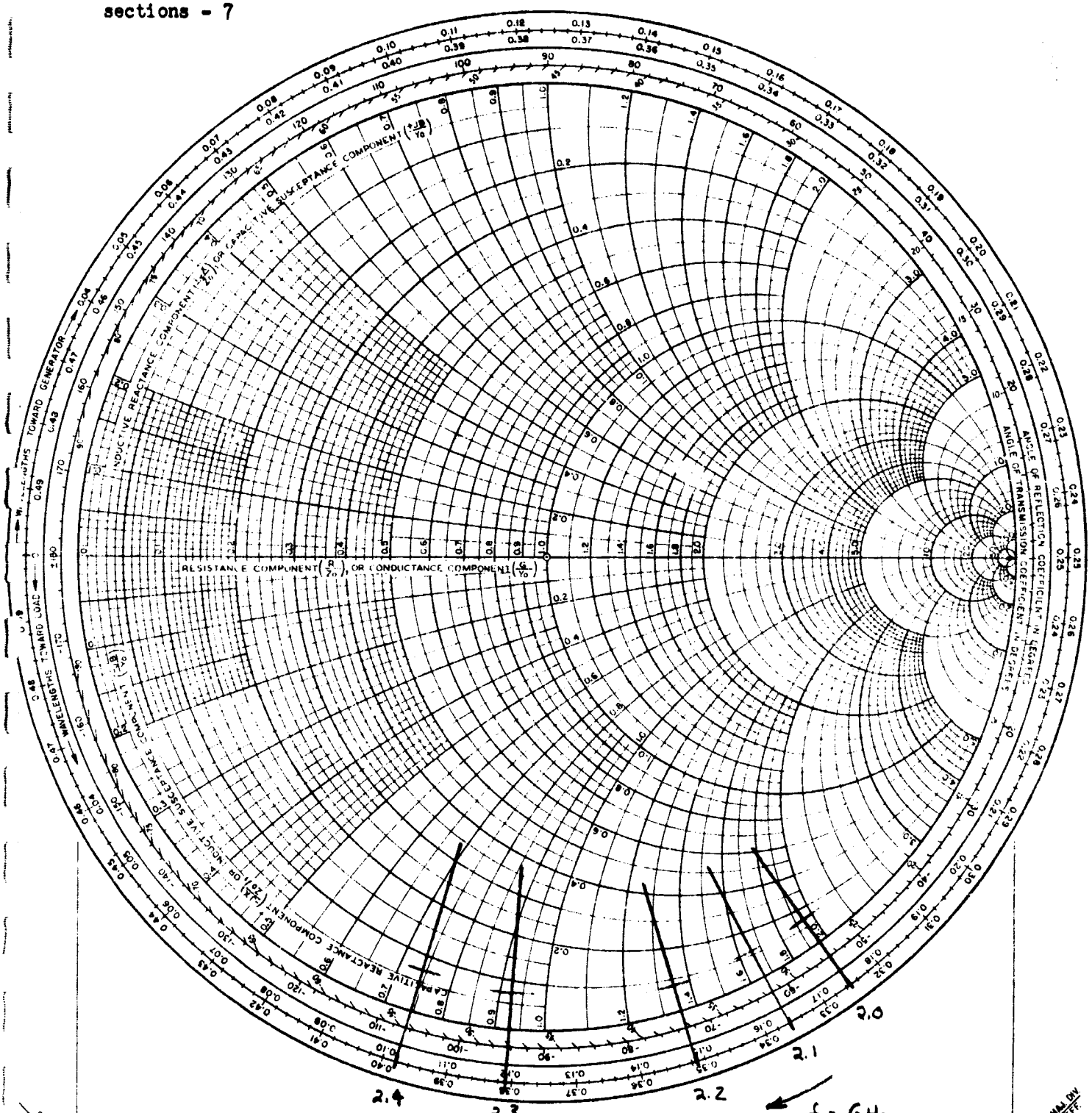
The basic problem to be solved is one of being able to change the apparent electrical lengths of an open circuited line to simulate a changing capacitance. The most obvious solution would be to change the dielectric constant of the medium surrounding the length of line since $\lambda_d = \lambda / \sqrt{E_r}$, where λd is the wavelength of the

2. "Handbook of Tri-Plate Microwave Components," Sanders Associates.

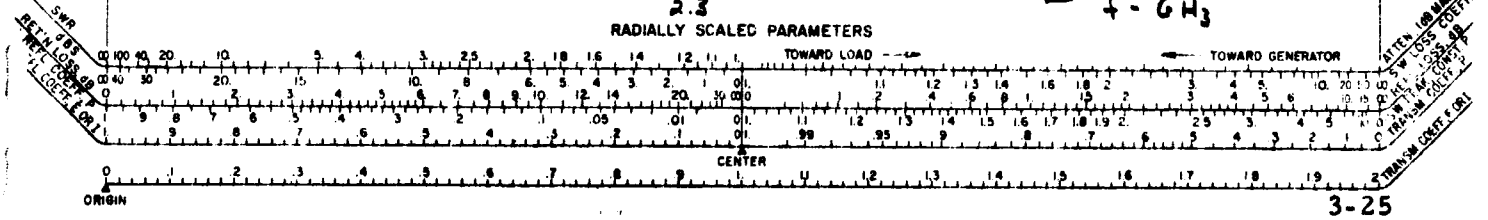
NAME	Figure 3-19. Impedance vs Frequency for Sawtooth Inductor	DWG. NO 3433
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. ©1966. PRINTED IN U.S.A.	DATE 2-7-68

IMPEDANCE OR [redacted] COORDINATES

No. of sawtooth sections - 7



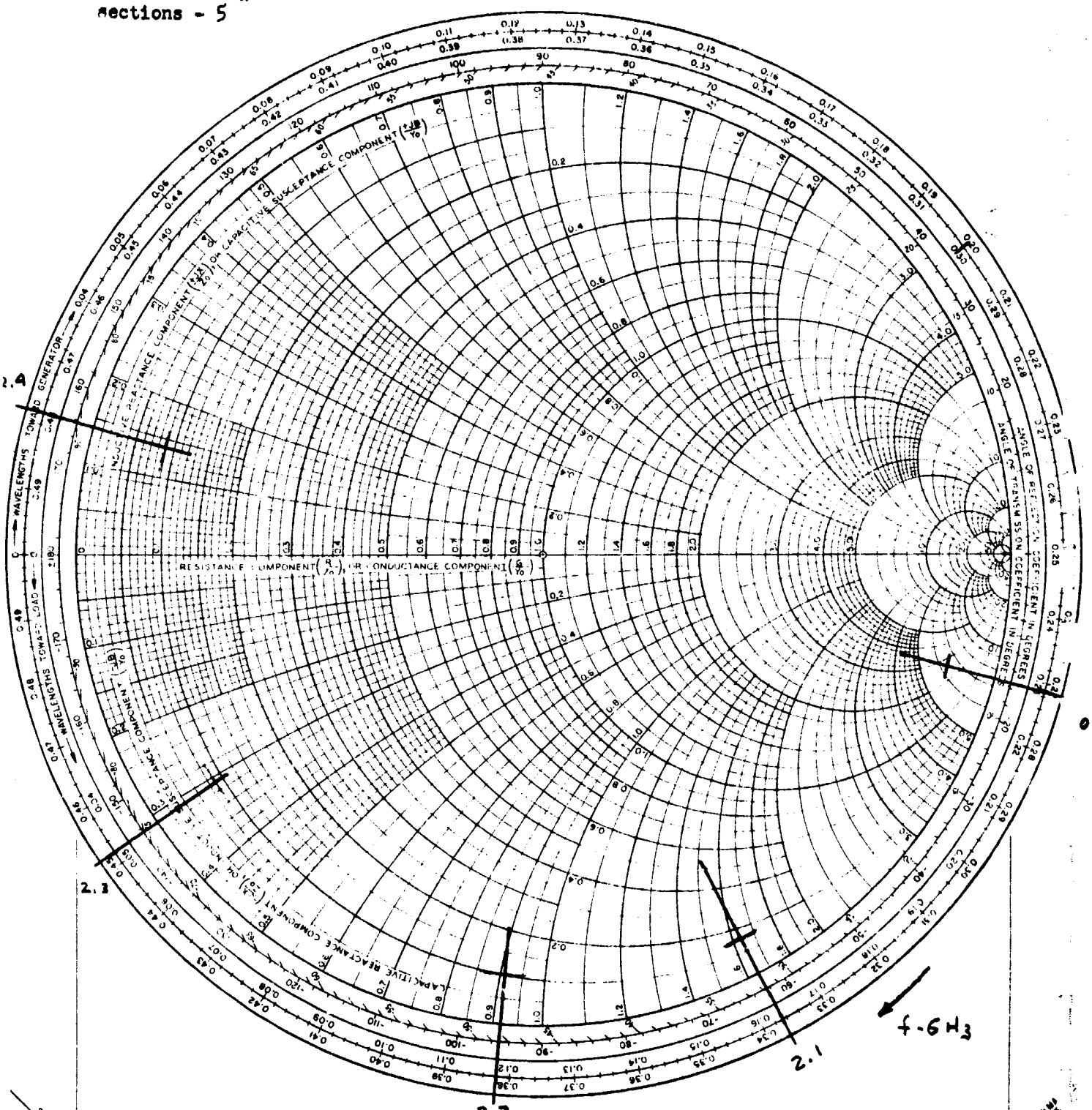
RADIALLY SCALED PARAMETERS



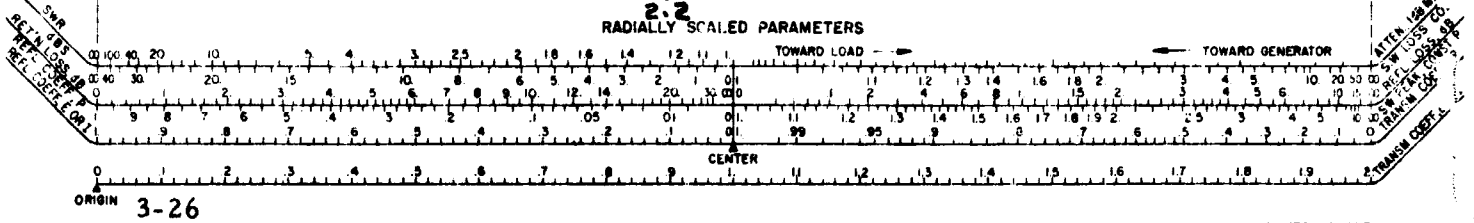
NAME Figure 3-20. Impedance vs Frequency for Rectangular Inductor	DWG NO 3433
SMITH CHART FORM 82-BSPR(9-66) KAY ELECTRIC COMPANY, PINE BROOK, N.J., © 1966 PRINTED IN U.S.A.	DATE 2-7-68

No. of rectangular sections - 5

IMPEDANCE OR [redacted] COORDINATES



RADIALLY SCALED PARAMETERS

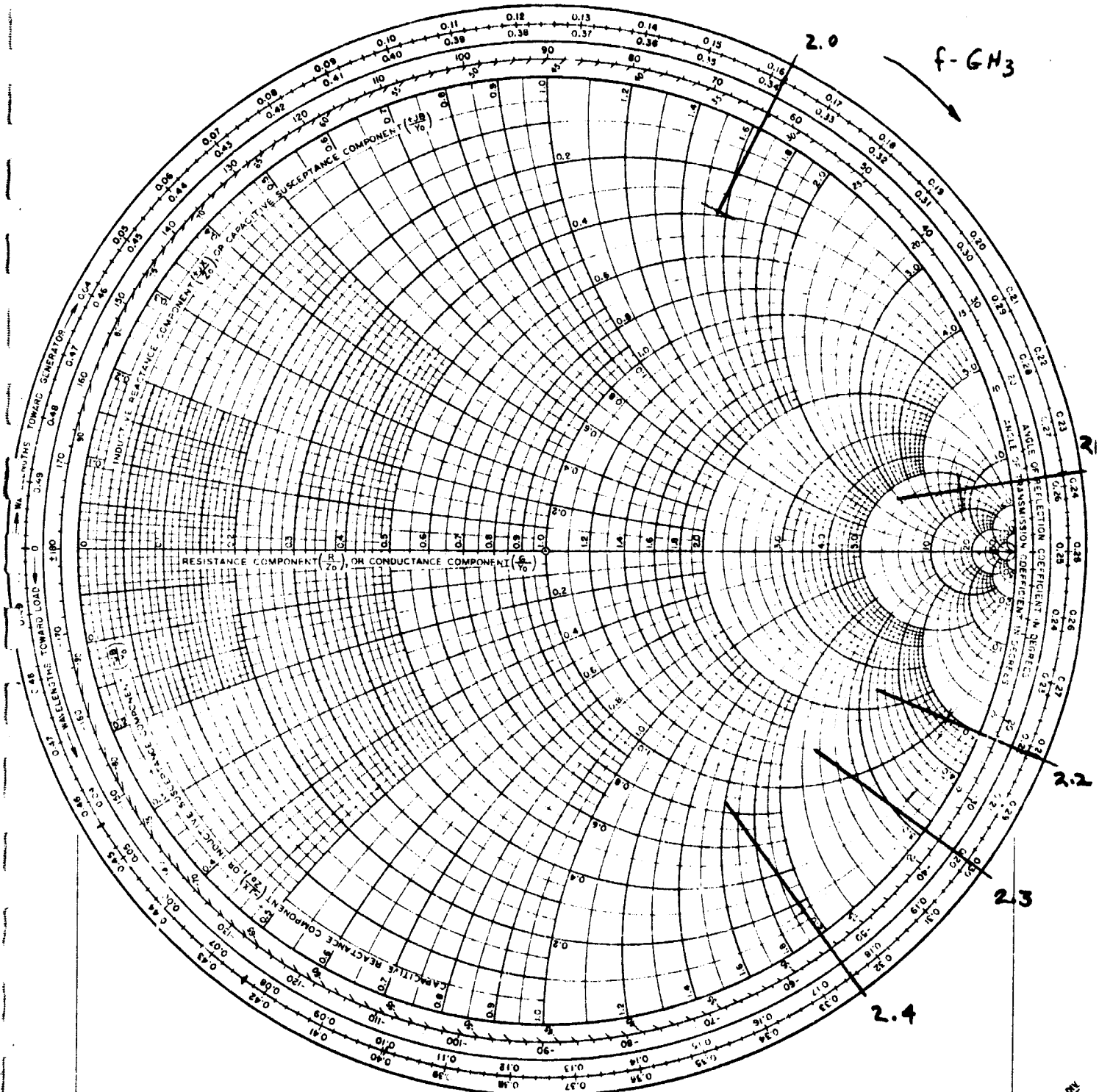


A MEGA-CHART

NAME Figure 3-21. Impedance vs Frequency for Spiral Inductor	DWG NO 3433
SMITH CHART FORM 82-BSPR (9-66) KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966 PRINTED IN U.S.A.	DATE 2-7-68

No. of spirals - 6

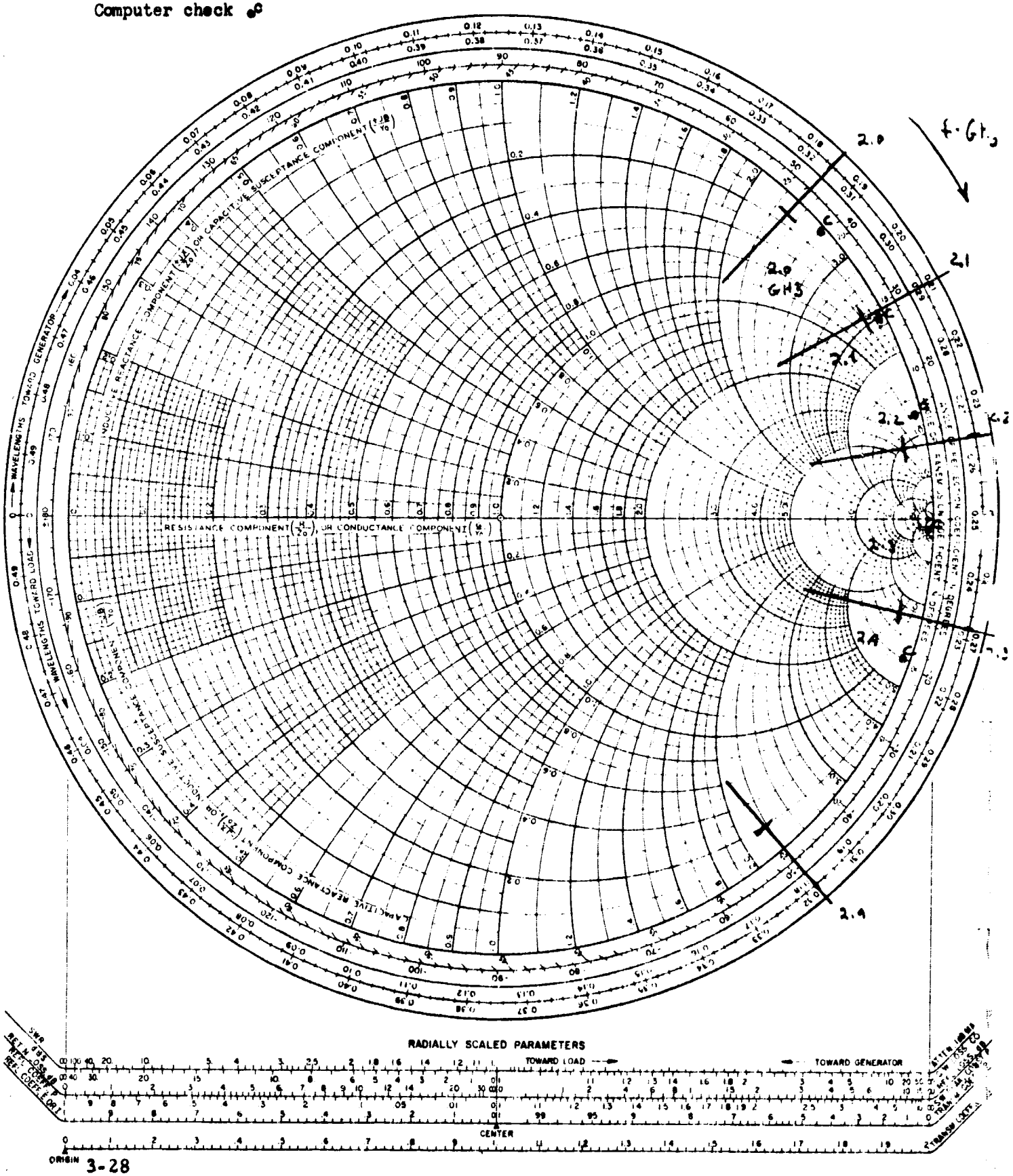
IMPEDANCE OR [redacted] COORDINATES



NAME	Figure 3-22. Impedance vs Frequency for Outband Filter Design	DWG. NO 3433
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966 PRINTED IN U.S.A.	DATE 2-7-68

Observed data +
Computer check ⊕

IMPEDANCE OR [redacted] COORDINATES



RADIALLY SCALED PARAMETERS

line in the medium, d, and Er is the relative dielectric constant of the medium. λ_o is the free space wavelength. Another approach is the parallel plate capacitor approach. The capacitance of a parallel plate device is given by:

$$C = .0885 \frac{K\,(n - 1)A}{d} \text{ pf}$$

k = dielectric constant

A = area of plate - in^2

d is the thickness of the dielectric - in

For this arrangement there are several variables which might be used to vary C. The dielectric constant K may be varied, increasing K increases C; also d may be varied giving an inverse relation of d vs C.

Each of the above methods was tried. The first was a rotating disk of different dielectric constants. This scheme is shown in figure 3-23.

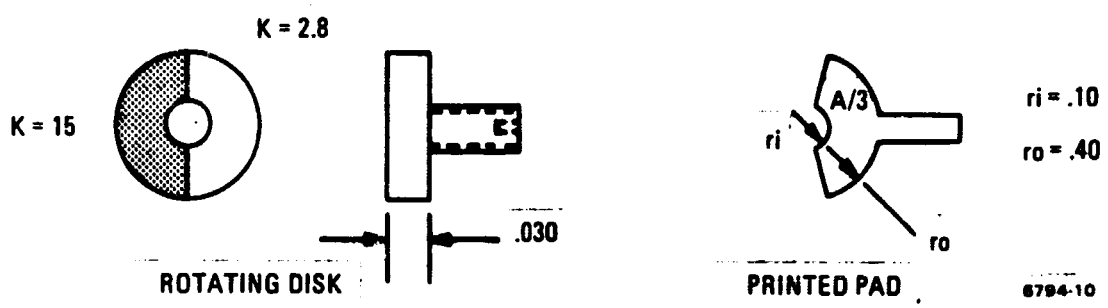


Figure 3-23. Rotating Dielectric Disk

As shown above, the disk had as one half of its area a dielectric whose constant was 15 and as the other half a material with a dielectric constant of 2.8. The capacitance could be calculated as follows. Using the capacitance formula we have:

$$C = .0885 \frac{(K)(A)}{d} \text{ pf} \quad d = .030$$

$$\frac{A}{3} = \pi(.4 - .1)^2 = .094 \text{ in}^2$$

$$\text{For } K = 2.8 \quad C = \frac{.0885(2.8)(.282)}{.03} = .73 \text{ pf}$$

$$\text{For } K = 15 \quad C = \frac{.0885(15)(.282)}{.03} = 3.15 \text{ pf}$$

From the above we can see that the total change is 2.42 pf.

Another arrangement is changing the electrical length of the line by changing the surrounding dielectric constant. Figure 3-24 illustrates this method. The high dielectric material is covered by the threaded insert. For air the line appears to be .37λ and has a capacitance of .? pf at 2250 MHz. When the line is surrounded by dielectric it is .148 λ or has an effective capacitance of approximately 2 pf. An increase in range can be obtained by making the line approach λ/4 when loaded with the dielectric.

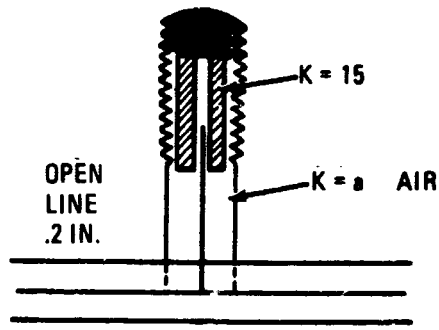


Figure 3-24. Variable Dielectric Constant

The last method tried was a dielectric disk cemented to the bottom of a threaded screw. By rotating the screw, the distance and therefore the capacitance, could be varied. For the arrangement in figure 3-25

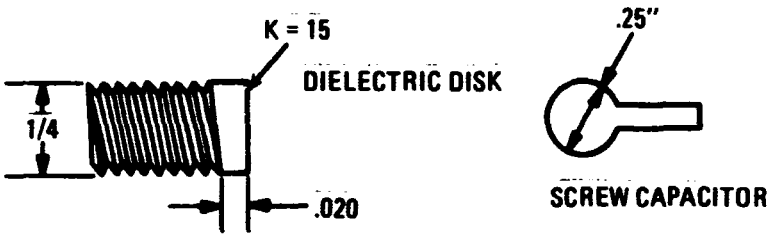


Figure 3-25. Variable Capacitor

the maximum capacitance can be calculated as

$$C \text{ max} = 0885 \frac{(15)\pi(.25)^2}{.020} = 13 \text{ pf}$$

The minimum capacitance therefore, is approximately

$$c \text{ max}/_4 = 3.25 \text{ pf.}$$ (Since the distance increases by approximately 4)

3.3.3.1 Tuning Elements

Each of the above variable capacitors may be used as tuning elements of miniature double stub tuners. The tuning elements are placed $\lambda/8$ wavelengths apart to simulate a quarter-wave tuner. A sketch of this is shown in figure 3-26.

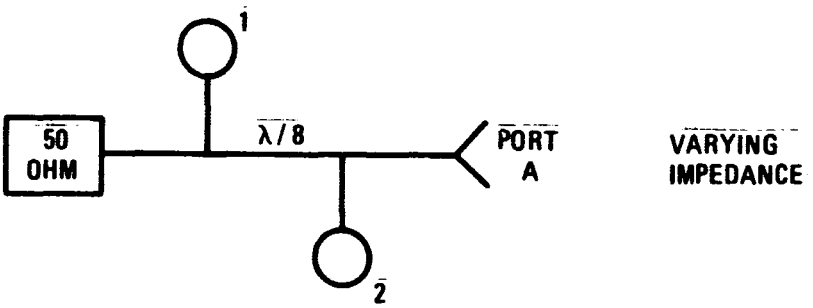


Figure 3-26. Variable Tuning Elements

The first variable tuning element essentially controls the real part of the impedance while the second variable tuning element controls the imaginary part of the impedance seen at port A.

3.3.3.2 Test Data

A plot of the capacity range for the three types of variable capacitors is shown in figures 3-27, 3-28, and 3-29. The range over which the impedance may be varied using the capacitors in a tuning arrangement is shown in figure 3-30. This data is for the rotating screw capacitors, with the other configurations yielding the same results.

3.3.3.3 Conclusion

Since it is almost a requirement that some sort of tuning be incorporated in the base circuit of a transistor power amp, the need for variable tuning elements is apparent. The types noted above all yielded satisfactory results, however, the first types and the third type (the rotating dielectric disk and the electrical line change) were extremely difficult to fabricate from a mechanical standpoint. The tuning element arrangement also proved satisfactory since a large range of impedances could be realized with two variables. The search for a good variable capacitor is far from over, however, since several problems were encountered in these units. First capacitance changes were very coarse. This was alleviated somewhat by going to finer thread for the variable function. Another problem was the fabrication methods for the units tolerances had to be held close to obtain a workable unit. Additional thought and work are still needed in this area.

3.3.4 DC Blocking Impedance Transforming Networks

This paragraph describes the design and test results of a study to eliminate chip capacitors from stripline power amplifiers.

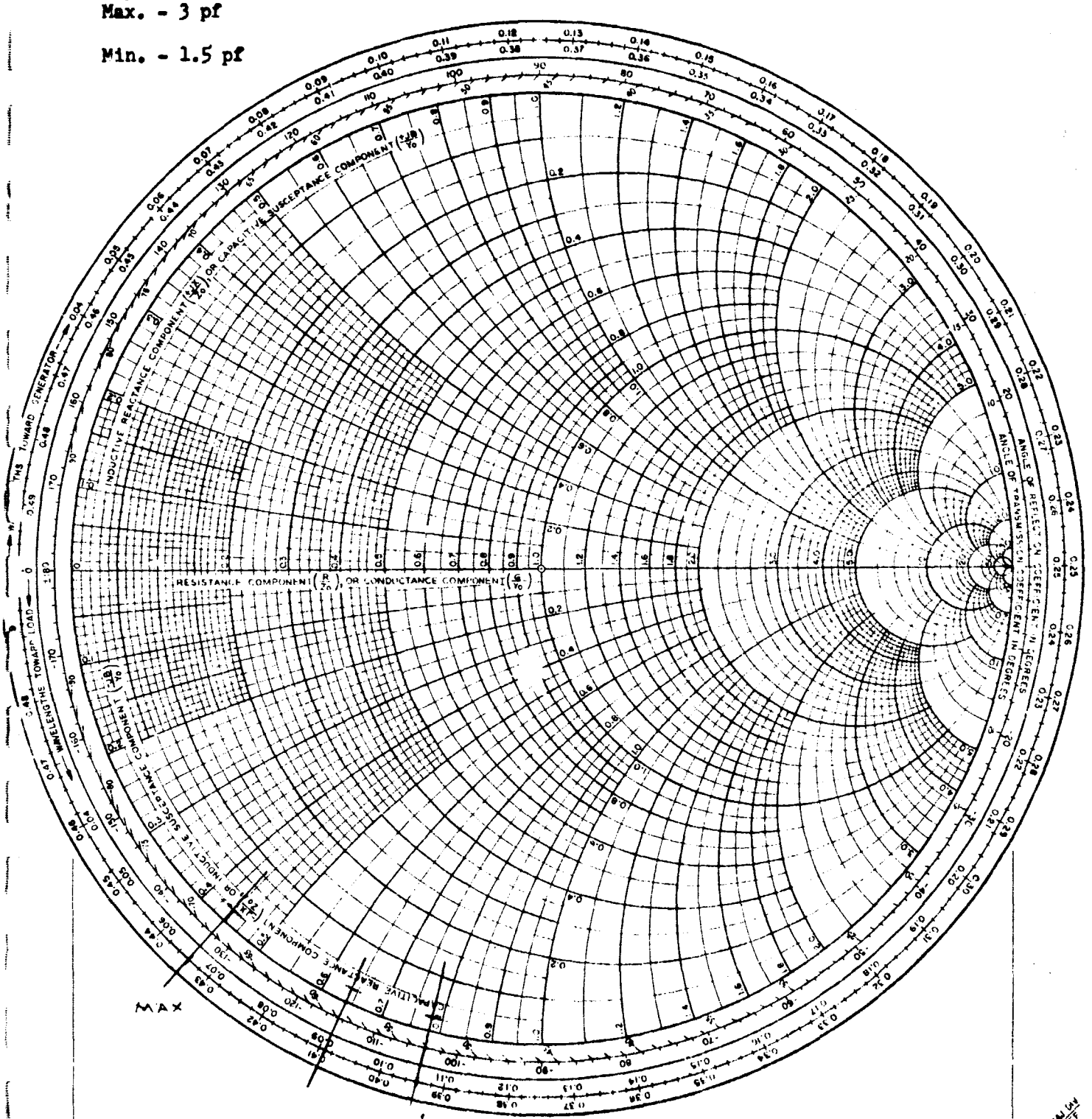
The problem presented is to design a network that provides a dc blocking capability while also providing an impedance transformation. This must be accomplished at extremely low circuit losses. One approach to the problem is shown in figure 3-31.

NAME Figure 3-27	Rotating Ceramic Disk Variable Capacitor	DWG. NO 3433
SMITH CHART FORM 82-BSPR (9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. ©1966 PRINTED IN U.S.A.	DATE 2-9-68

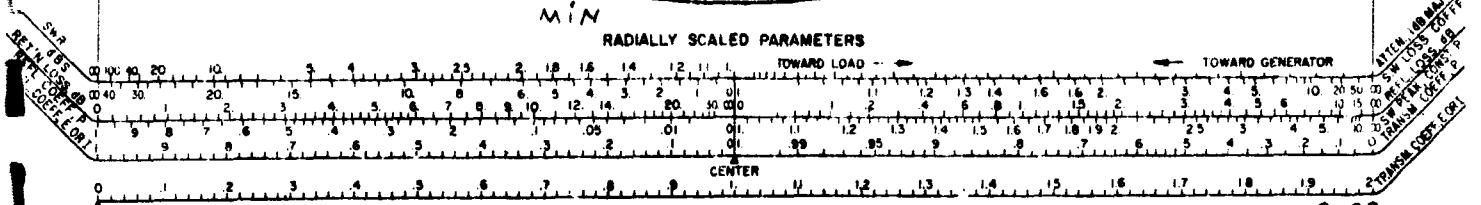
Capacitance range
Max. - 3 pf

Min. - 1.5 pf

IMPEDANCE OR ADMITTANCE COORDINATES



RADIALLY SCALED PARAMETERS



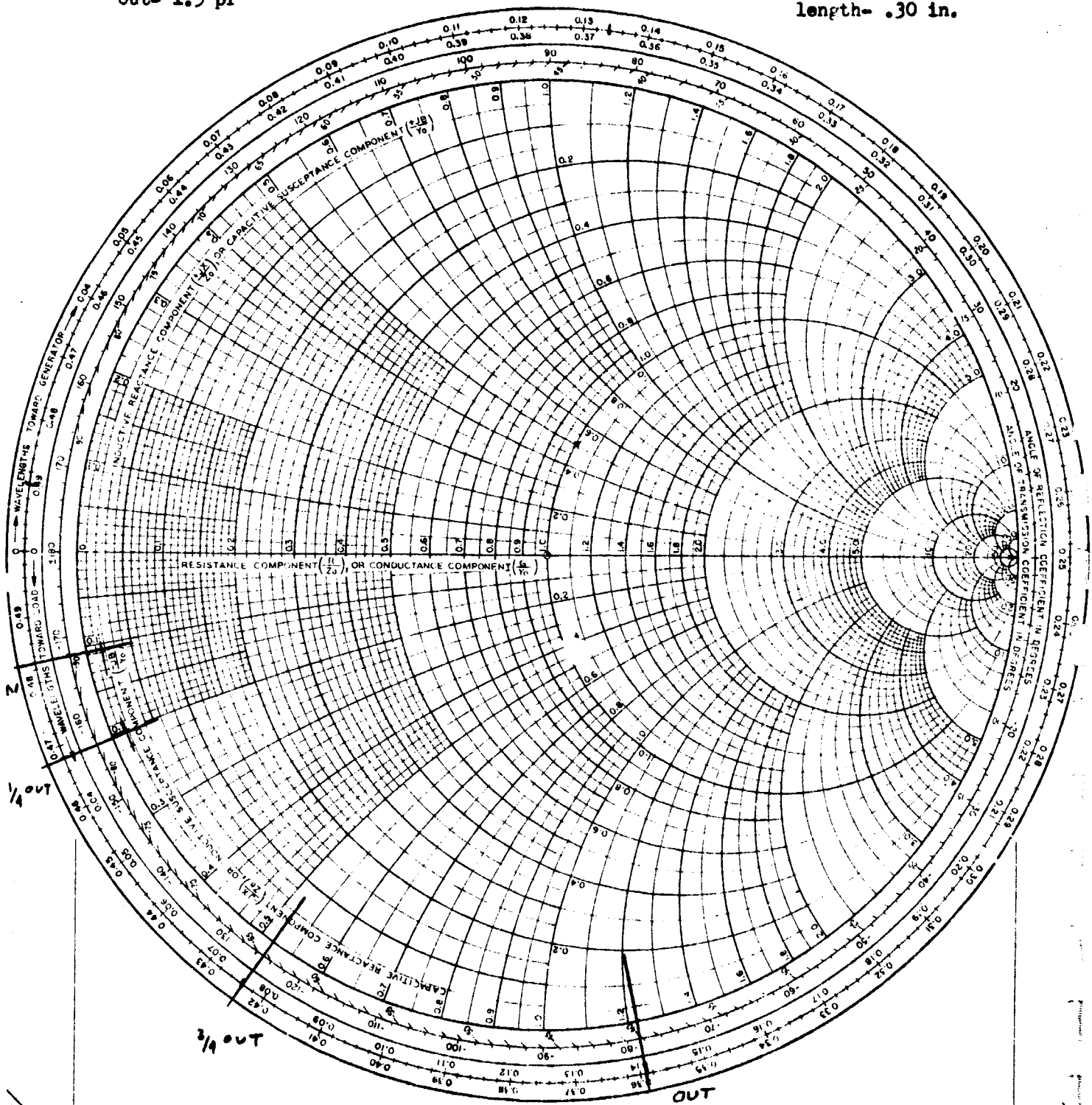
A MEGA-CHART

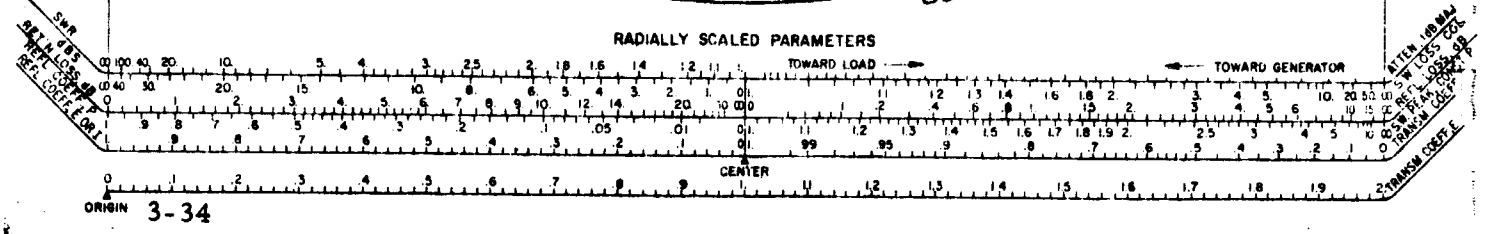
NAME	Figure 3-28. Stand-up Capacitor Tuning Range	DWG. NO	3433
SMITH CHART FORM 82-B3PR (9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966. PRINTED IN U.S.A.	DATE	2-9-68

Tuning range
In- 15 pf
Out- 1.5 pf

IMPEDANCE OR ADMITTANCE COORDINATES

Open circuit line
length- .30 in.





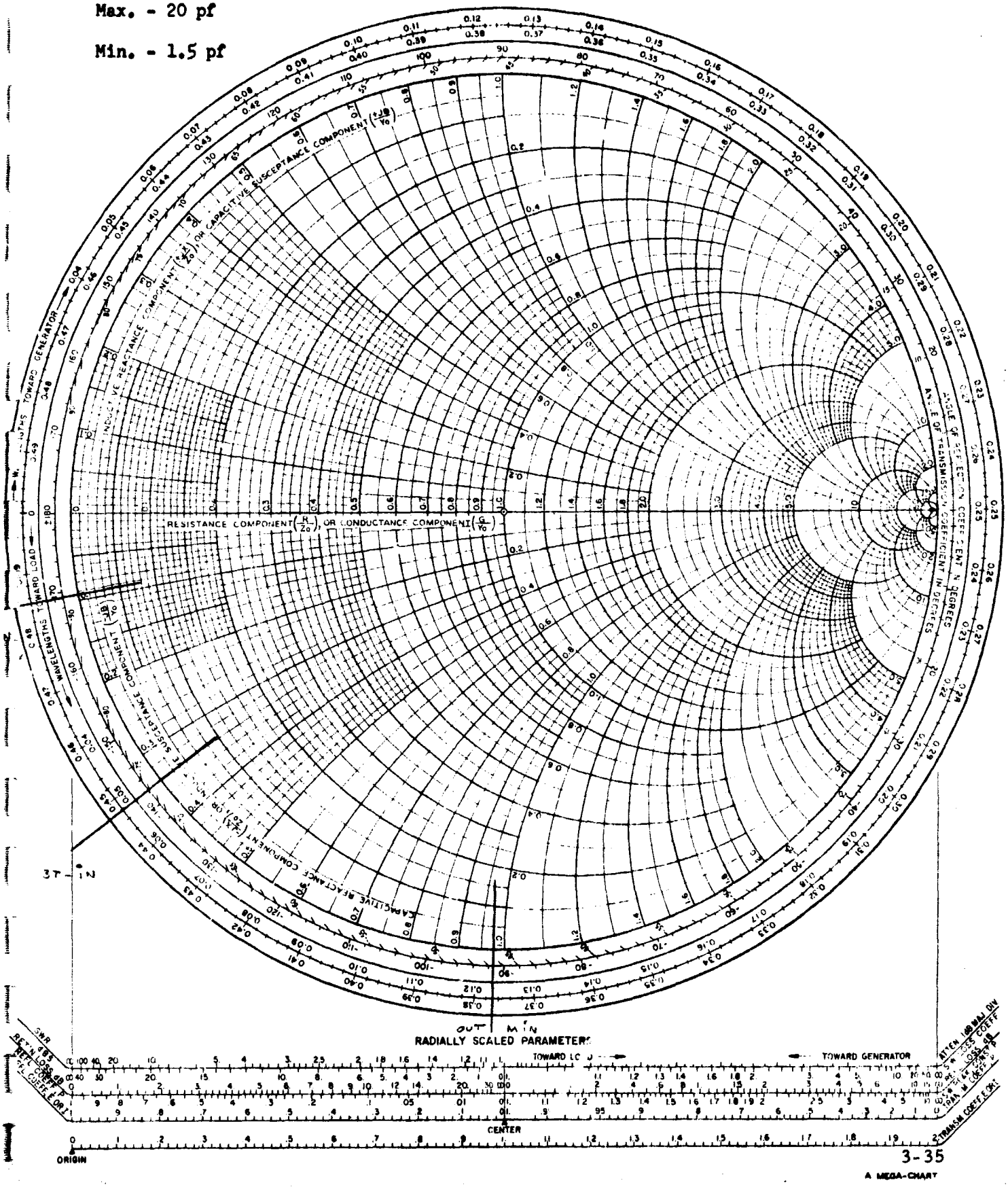
A MEGA-CHART

NAME	Figure 3-29.	TITLE	Rotating Screw Variable Capacitor	DWG. NO	3433
SMITH CHART FORM 82-BSPR (9-66)		KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966 PRINTED IN U.S.A.		DATE	2-9-68

Capacitance range: **IMPEDANCE OR ADMITTANCE COORDINATES**

Max. - 20 pf

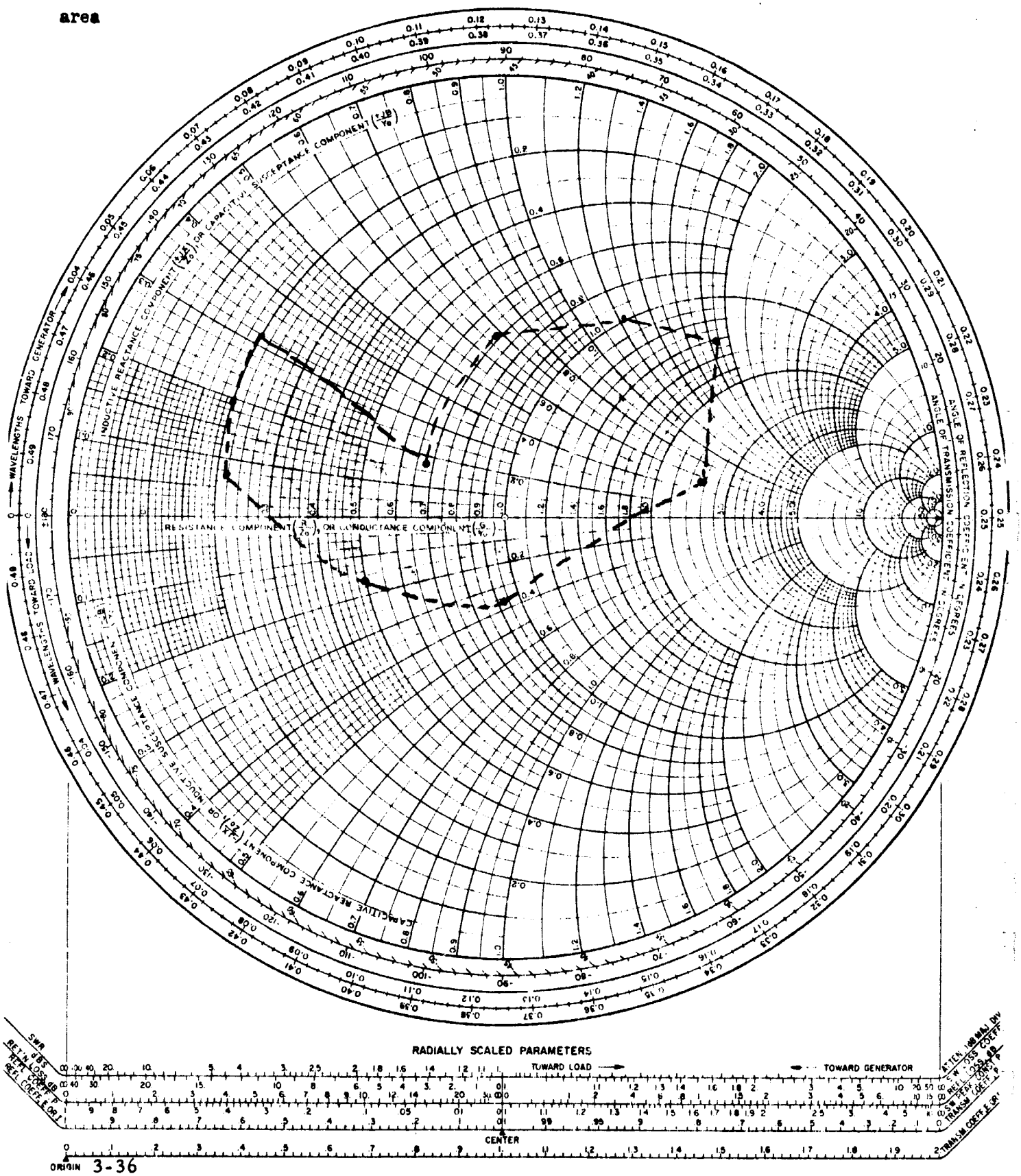
Min. - 1.5 pf



A MEGA-CHART

NAME Figure 3-30.	TITLE Tuning Elements-Tuning Range	DWG. NO. 3433
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966 PRINTED IN U.S.A.	DATE 2-9-68

Tuning Range - Shaded area



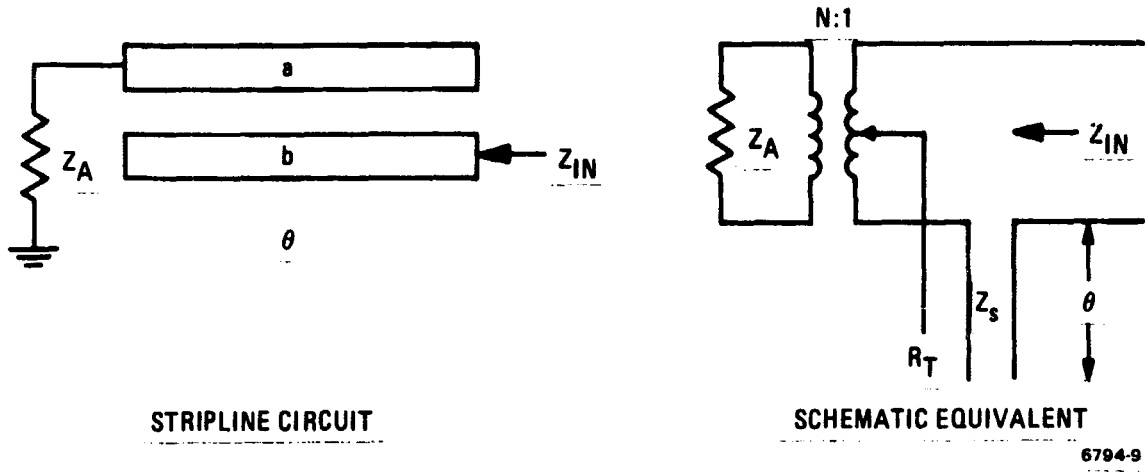


Figure 3-31. DC Blocking and Impedance Transformation

where

(1) $$Z_{oe}^{a} = Z_A\left[\sqrt{\frac{R_T}{Z_A}} + 1\right] ,$$

(2) $$Z_{oo}^{a} = 2Z_A = Z_{oe}^{a}$$

(3) $$Z_{oe}^{b} = Z_{oo}^{b} + Z_{oe}^{a} - Z_{oo}^{a} ,$$

(4) $$Z_{oo}^{b} = Z_s - Z_A\left[1 - \frac{R_T}{Z_A}\right] + Z_{oo}^{a} ,$$

(5) $$Z_s = Z_A\left(\frac{N^2 - 1}{N^2}\right) + Z_{oo}^{b} - Z_{oo}^{a} ,$$

(6) $$N = \frac{2Z_A}{Z_{oe}^{a} - Z_{oo}^{a}}$$

(7) $$2Z_A = Z_{oe}^{a} + Z_{oo}^{a} ,$$

(8) $$R_T = \frac{Z_A}{N^2}$$

The above equations describe all parameters of the circuit.

Assumption: 1.0

Assume very tight coupling (i.e. k = .94)

$$\text{Then } N = \frac{2Z_A}{Z^a_{oe} - Z^a_{oo}} = \frac{Z^a_{oe} + Z^a_{oo}}{Z^a_{oe} - Z^a_{oo}} = 1/k$$

$$\text{Therefore } N = \frac{1}{k} = \frac{1}{.94} = 1.06$$

Assumption: 2.0

Matching into 50 ohms Z_A 50 ohms

$$\text{From (8)} \quad R_T \frac{Z_A}{N^2} \quad \frac{50}{(1.06)^2} = 44.5 \text{ ohms}$$

and From (1) $$Z^a_{oe} = Z_A\left[\sqrt{\frac{Z_A}{R_T}} + 1\right] = 50\left[\left(\frac{44.5}{50}\right)^{1/2} + 1\right]$$

$$Z^a_{oe} = 50\left[1.945\right] = 97 \text{ ohms}$$

$$Z^a_{oo} = 2Z_A - Z^a_{oe} = 100 - 97 \text{ ohms} = 3 \text{ ohms}$$

$$\therefore Z^a_o = \sqrt{97(3)} = 17.5 \text{ ohms}$$

Assumption: 3.0

Assume that $Z_s = 30$ ohms

$$\text{Then } Z^b_{oo} = Z_s - Z_A\left(1 - \frac{R_T}{Z_A}\right) + Z^a_{oo} = 30 - 50\,(1 - .89) + 3.0$$

$$Z^b_{oo} = 27.5 \text{ ohms}$$

From equation (3)

$$Z^b_{oe} = Z^b_{oo} + Z^a_{oe} - Z^a_{oo} = 27.5 + 97 - 3 = 131.5 \text{ ohms}$$

$$\text{Therefore } Z^b_o = \sqrt{Z^b_{oo}\, Z^b_{oe}} = 60 \text{ ohm}$$

The real part of the input Z is controlled by the coupling factor k. Since we have for k

$$k = \frac{1}{M} \text{ and } R_T = \frac{Z_A}{N^2}$$

This gives

$$R_T = Z_A k^2$$

From this it can be seen that as the coupling is decreased, the real part also decreases.

A circuit was built with the dimensions shown in figure 3-32.

Z_a = 17.5 ohms, Z_b = 60 ohms

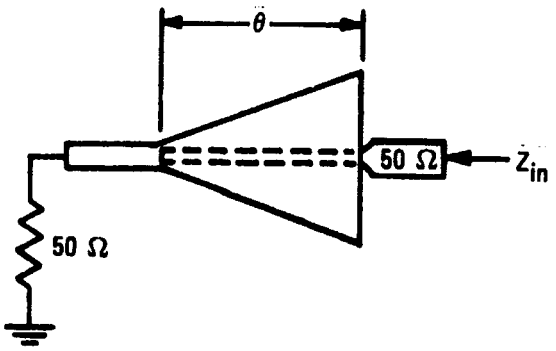


Figure 3-32. Test Circuit

θ was fixed at .825 inches. This length controls the imaginary part of the input impedance and may be adjusted to make Z_{in} look either inductive or capacitive.

3.3.4.1 Test Results

The above circuit was tested on a slotted line setup as shown in figure 3-33.

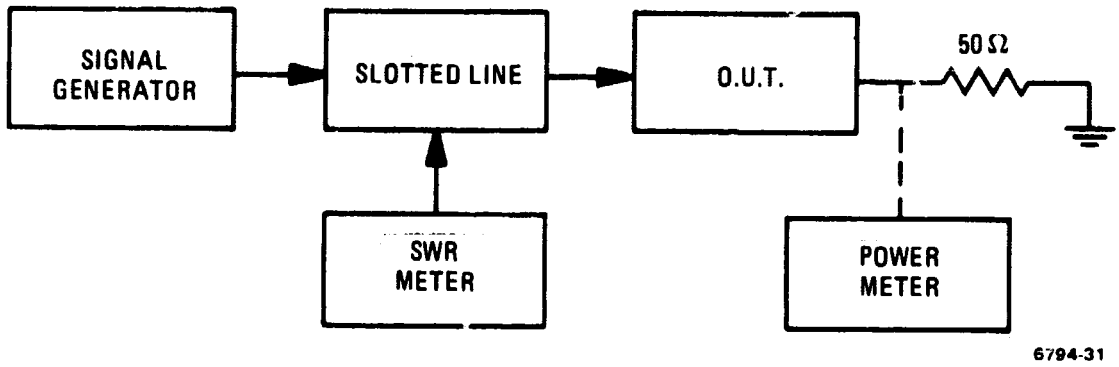


Figure 3-33. Test Setup

The signal generator was varied from 2.0 GHz to 2.4 GHz in 100 MHz steps. At each frequency the input impedance (Z_{in}) was measured and recorded. This data is shown below:

With 2.0 Mil Mylar Spacer

Freq	Angle (mm)	VSWR	Ref Short (mm)
2.0	286.5	3.50:1	272.0
2.1	301.0	3.50:1	286.0
2.2	306.0	3.45:1	299.2
2.3	262.5	3.55:1	310.0
2.4	214.0	3.55:1	321.5

With 4.0 Mil Mylar Spacer

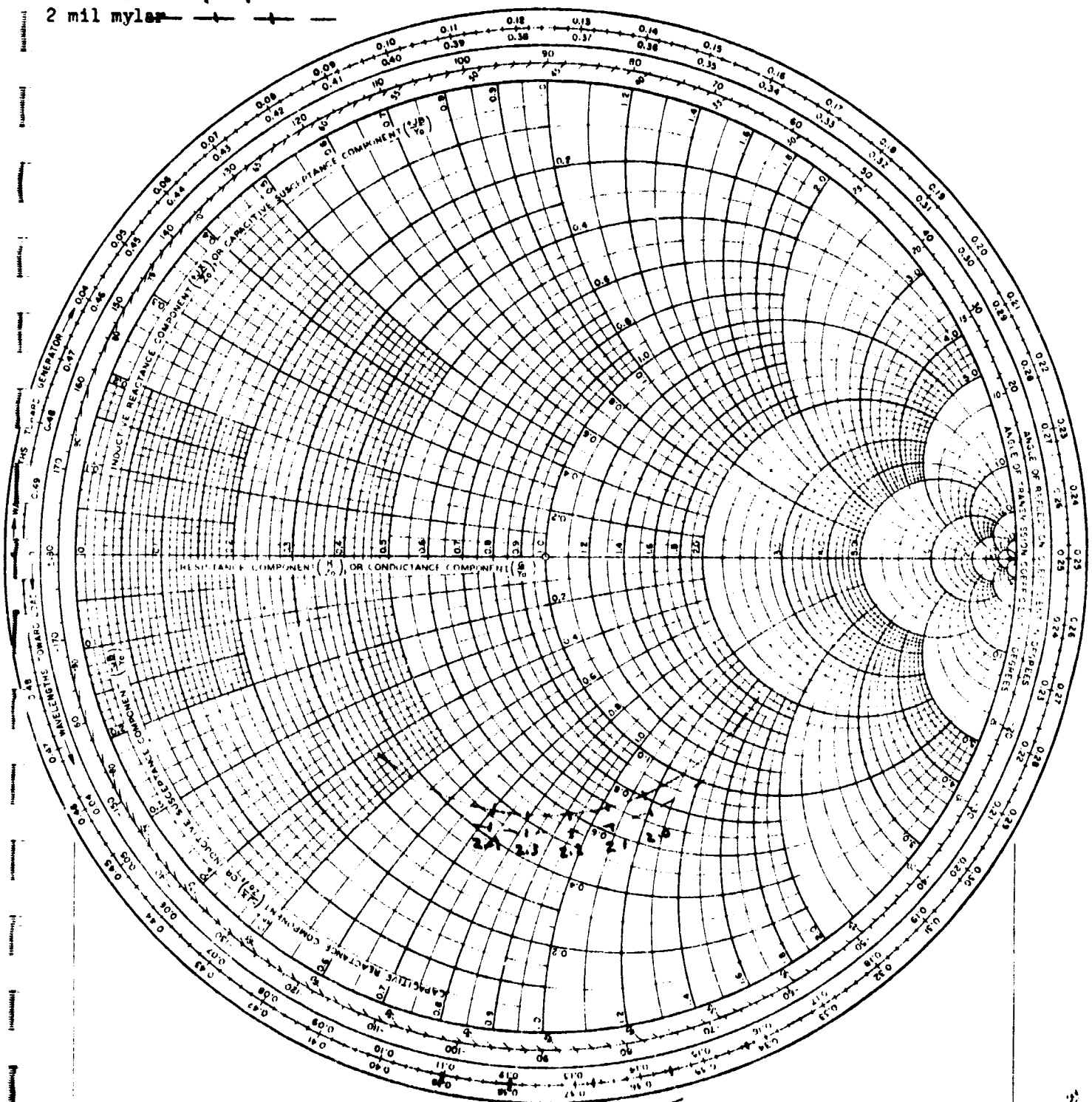
Freq.	Angle (mm)	VSWR
2.0	286.5	3.8:1
2.1	301.0	3.8:1
2.2	306.0	3.8:1
2.3	262.0	3.8:1
2.4	214.0	3.8:1

NAME Figure 3-34.	TITLE Impedance Transformer Characteristics	DWG NO
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966 PRINTED IN U.S.A.	DATE March 5, 1968

~~IMPEDANCE~~ OR ADMITTANCE COORDINATES

1 mil mylar

2 mil mylar



f-gH3

A plot of this data is shown in figure 3-34. The dotted line shows the 4.0 mil mylar spacer.

To measure the loss of the transformer section, the test setup shown in figure 3-35 was used. The triple stub tuners are used to match the output impedance to 50 ohms.

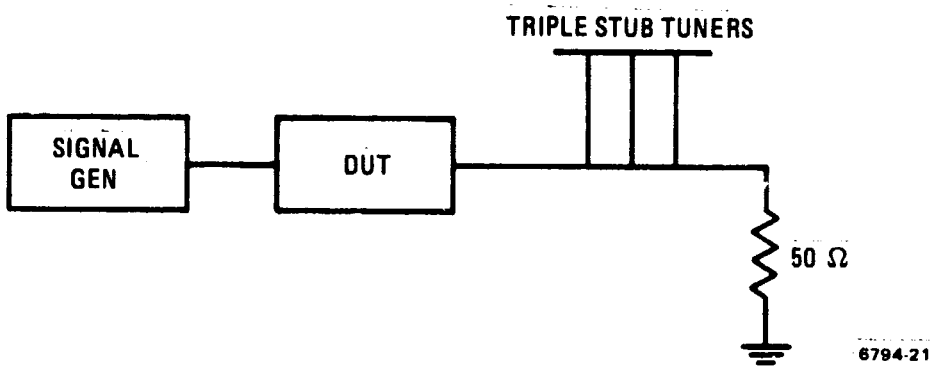


Figure 3-35. Insertion Loss Measurement

The measured insertion loss for the circuit designed was .08 db. It was found that if the transformer had high standing waves internal to the device high losses resulted.

3.3.4.2 Conclusion

Because of the need to eliminate the highly unreliable chip capacitors, this study was important. A network could be used for both base and collector to provide dc decoupling. Each network could be adjusted so that the proper input impedance could be realized in helping to match either the input or output circuit. To help the bandwidth, several tapering methods could be investigated (i.e. linear, logrithmic, etc.) to best accomplish this task.

3.4 CIRCUIT DEVELOPMENT

The following paragraphs present a more detailed description of the circuit comparing the transmitter functions.

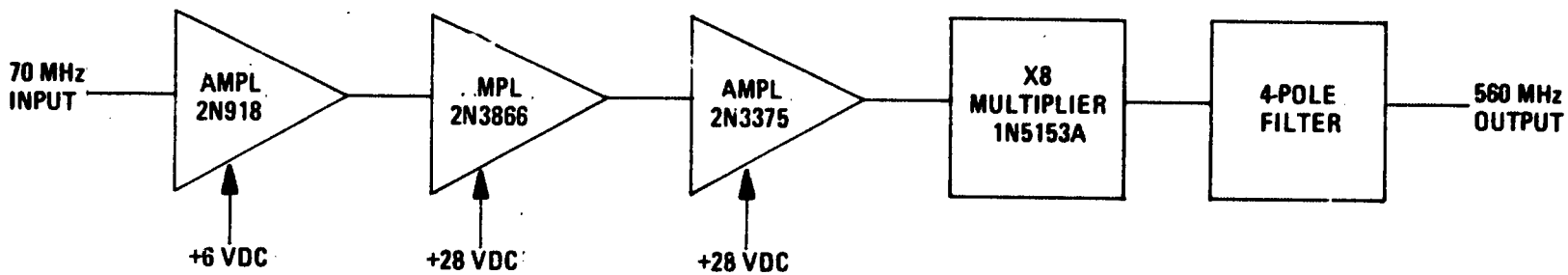


Figure 3-36. X8 Module Block Diagram

3.4.1 Exciter

The transmitter operating in the coherent mode, receives a low level 70 MHz signal from the receiver, amplifies, multiplies, and modulates this signal. This paragraph describes the exciter module of the transmitter. The module develops a 560 MHz, 0.5 watt signal from a 70 MHz, 1 mw input. The objectives were to generate this signal in the most efficient manner and in the least amount of space.

3.4.1.1 Block Diagram

A block diagram for this portion of the transmitter is shown in figure 3-36. The plan chosen was to amplify the 70 MHz signal, multiply it in one step by eight, and filter the signal to provide a clean 560 MHz drive to the next stage of the transmitter. The requirements for this module are:

1) Output Frequency - 560 MHz
2) Output Power - 0.5 watt nominal into 50 ohms
3) Spurious Responses - 70 db down for $f_{out} \pm 70$ MHz.
4) Input Frequency - 70 MHz
5) Input Power - 1 mw nominal into 50 ohms

Assuming 23% efficiency for the X8 multiplication and assuming 2 db loss for filtering, the required drive power to the multiplier must be 3.5 watts. Therefore, the total gain required for the 70 MHz amplifier chain is 35.5 db. This amount of gain can be achieved with 3 stages of amplification.

The multiplier uses a step-recovery type varactor diode. The design approach used was taken from Hewlett-Packard application note 913, "Step Recovery Diode Frequency Multiplier Design".

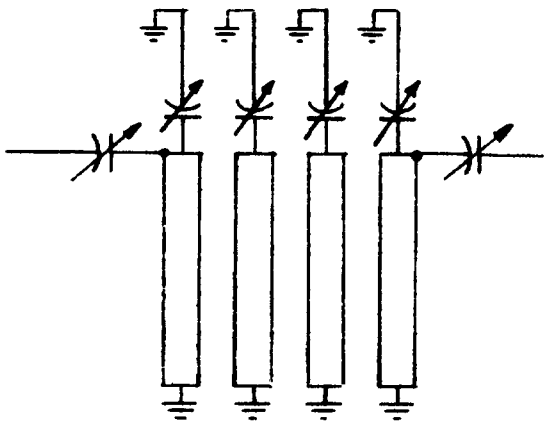
Several methods of filtering the 560 MHz signal were investigated. Two stripline filters (interdigital and comb-line) and a lumped constant filter were investigated. It was determined that a Chebychev response with a minimum of four poles was required to sufficiently filter the signal and allow a bandwidth of 30 MHz. An interdigital filter requires the element lengths to be about one-quarter

wavelength (which is about 3.5 inches in teflon). The use of high dielectric ceramic material was considered, but was found to be unrealizable because the higher dielectric constant caused excessively high fringing and coupling capacitances which yielded negative line widths in the design equations. The interdigital design was rejected in favor of the comb-line configuration shown in figure 3-37 because the length of the resonators would be considerably less than one-quarter wavelength. The final package size of the filter is two by two inches with one-quarter inch ground plane spacing and air dielectric. The lumped constant filter was abandoned after minor investigation because of the difficulty of controlling stray reactances in a multi-pole filter at the frequency range involved.

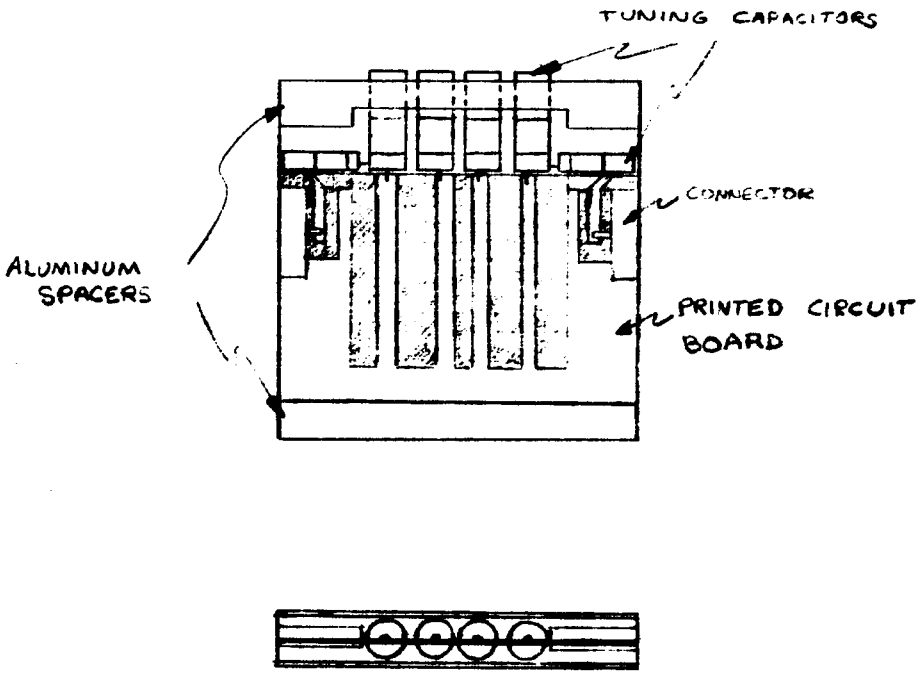
3.4.1.2 Circuit Description

A schematic diagram of the module is shown in figure 3-38. The amplifier chain uses three transistors, a 2N918, 2N3866 and a 2N3375. The coupling networks are broadband to eliminate the need for tuning. The first and second stages provide approximately 13 db of gain each, and the third stage provides approximately 9 db of gain. All stages are operated in common emitter configuration. The first stage operates from a 6 volt dc supply and the last two stages operate from a 28 volt dc supply.

The X8 multiplier uses a 1N5153A step recovery diode which has a reverse capacitance of approximately 6 pf. The self bias resistor R9 is selected for each diode and is also used for temperature compensation. The impulse generating network is formed by L6 and C18. L6 is the drive inductance and C18 is chosen to make the input impedance of the impulse generating network look resistive and to act as a short at the output frequency. Series resonant circuits at the input and output allow undesired frequencies to be recirculated in the diode and desired frequencies to pass. The multiplier output is matched into 50 ohms. The filter is first tuned separately to match into 50 ohms at input and output. The filter is capacitively coupled in and out.



(a) SCHEMATIC



(b) CONSTRUCTION

Figure 3-37. Comb-Line Filter

3.4.1.3 Test Results

The data below indicates results of tests performed on a breadboard model of the amplifier, X8, and multiplier filter module.

Data at room temperature with 1 mw, 70 MHz drive:

Power Output = 600 mw

DC Input Power = 5.95 watts

Overall Efficiency = 8.5%

Overall Output Bandwidth = 28 MHz

Temperature Test Data:

Temperature	Power Output	Bandwidth (3 db)
- 35°C	530 mw (-.58 db)	31.5 MHz
+100°C	500 mw [illegible] db)	28 MHz

The data indicates that the module can successfully meet the requirements over the temperature range of -35°C to +100°C.

3.4.2 Phase Modulator

Modulating a transmitter at a low frequency requires that all multipliers and amplifiers following the modulator be broadband in order to maintain high modulation bandwidths. The advantages of modulating at the highest possible frequency are that it simplifies design of multipliers and amplifiers preceding the modulator and that it reduces distortion by providing fewer bandpass networks between the modulator and output.

The requirements for the modulator are:

1. Second and third harmonic distortion of 1% or less.
2. Modulation index of 0.7 radian or greater.
3. Frequency response to 10 MHz or greater.

3.4.2.1 General Design Approach

Two types of phase modulators were investigated. The first is shown in figure 3-39 and the second in figure 3-40. The constant amplitude, variable phase filter (figure 3-39) was rejected as a practical stripline modulator because it would be very difficult to realize the circuit configuration using stripline techniques, eg. extensive use of series inductors and power splitters.

Effort was concentrated on the phase modulator of figure 3-40 since it showed early promise of satisfactorily meeting the requirements and lent itself to stripline techniques. A quadrature hybrid is a four port device which splits the incoming signal into two outputs, 2 and 3, which are in phase quadrature and 3 db below the input power. Typical insertion loss is 0.5 db with the two quadrature outputs balanced within 0.5 db. Terminal 4 is loaded with a resistance equal to the hybrid characteristic impedance and receives no power unless the loads on terminals 2 and 3 have a vswr other than 1.00. An isolation between terminals 1 and 4 of 30 to 50 db can be achieved.

It can be shown that whenever terminals 2 and 3 are loaded equally (not necessarily with R_o), the input vswr remains low. Thus if 2 and 3 are shorted, the power reflected from 2 splits between 1 and 4 while the reflected power from 3 also splits equally between 1 and 4. However, the two reflected components are exactly out of phase at terminal 1 and are in phase at terminal 4. This is the very basis for using the quadrature hybrid as a phase modulator. However, instead of shorting 2 and 3, these terminals are identically terminated with reactances. Since no power is absorbed in a pure reactance, most of the power input will appear at terminal 4 loaded in R_o. The phase relationship between the input and output will now be dependent on the reactance value with which 2 and 3 are terminated. By using varactor diodes as the terminating capacitances, the reactances can be varied by applying a modulating voltage to the varactors.

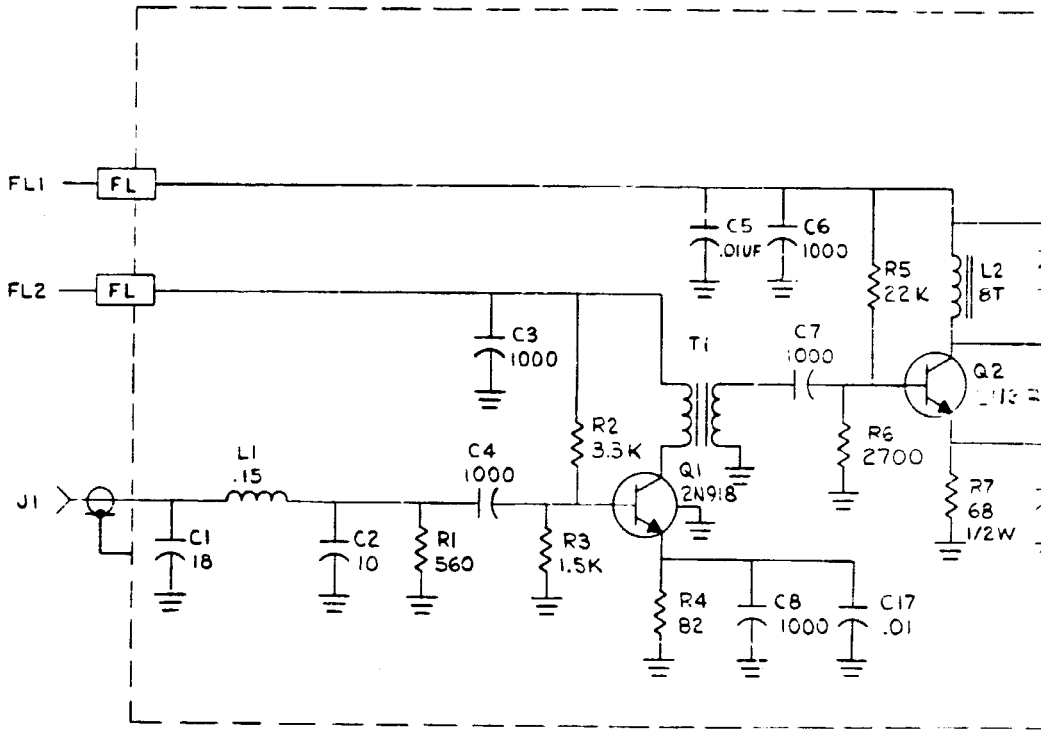
Equation 1 gives the reflection coefficient in terms of terminating impedance and characteristic impedance.

ASTERISK INDICATES DATA WHICH IS NONMANDATORY — FOR INFORMATION ONLY.

NOTES:

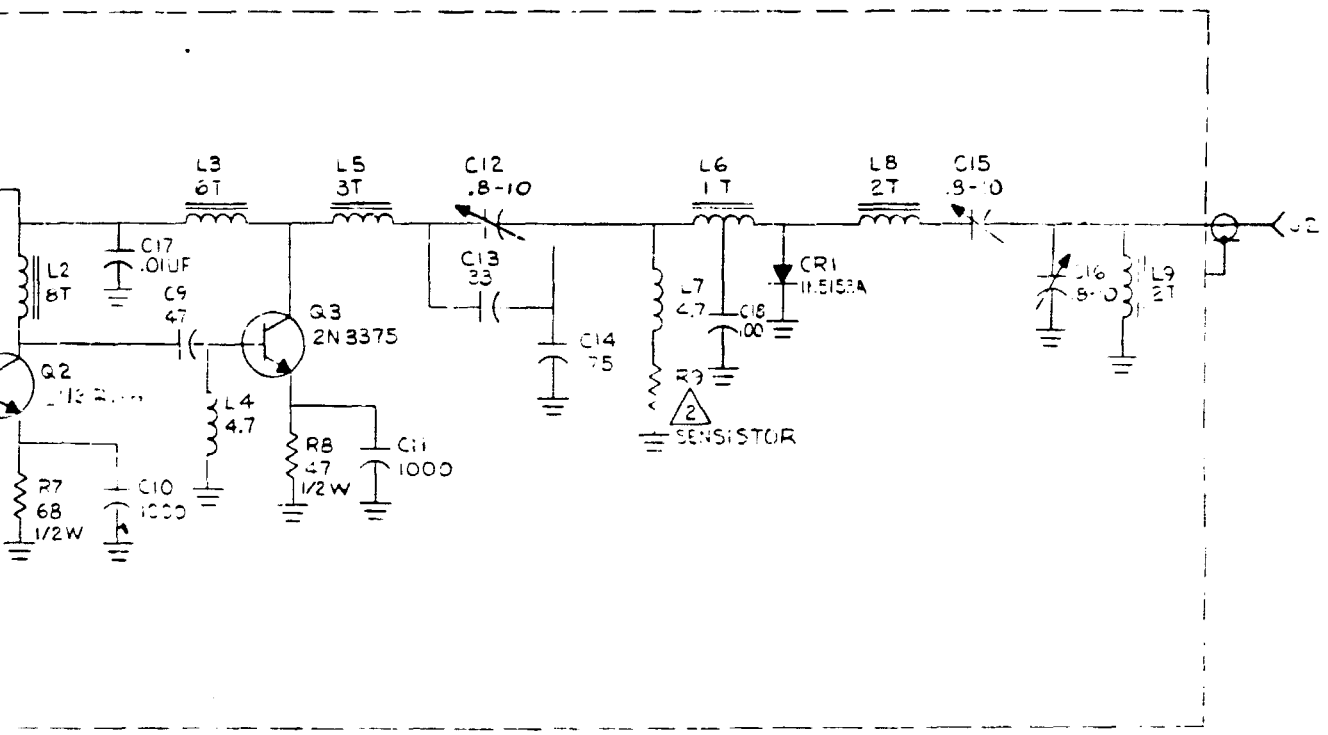
1. UNLESS OTHERWISE SPECIFIED,
   ALL RESISTORS ARE IN OHMS,
   ALL CAPACITORS ARE IN MICRO MICRO FARADS,
   ALL INDUCTORS ARE IN MICRO HENRIES.

2. VALUE TO BE SELECTED AT TEST.



NOLE LIST

FOLDOUT FRAME 1



REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

ITEM NO	QTY REQD 04	03	02	01	CODE IDENT NO	PART OR IDENTIFYING NO	DRAWING OR SPECIFICATION NO	NOMENCLATURE OR DESCRIPTION	SUPPLEMENTARY PART OR IDENTIFYING NO	NOTES

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

FOR PARTS LIST SEE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND END USE
SURFACE FINISH
TOLERANCES
TWO PLACE DEC ±
THREE PLACE DEC ±
ANGLES ± HOLE DIA ±

MATERIAL

FINISH

DR BY
CHK BY
MFG
PROJ NO
CONTRACT NO
SEE MOTOROLA NOTICE & DATE

APPROVED NAME DATE
APPROVED NAME DATE

MOTOROLA PART NUMBER

NEXT ASSEMBLY USED ON

★ APPLICATION

MOTOROLA INC. Government Electronics Division / Aerospace Center, 8201 East McDowell Road, Scottsdale, Arizona

Figure 3-38. X8 Multiplier (Schematic Diagram)

SIZE D | CODE IDENT NO 94990 | 63-2244M

SCALE | WEIGHT | SHEET

3-49, 3-50

FOLDOUT FRAME 2

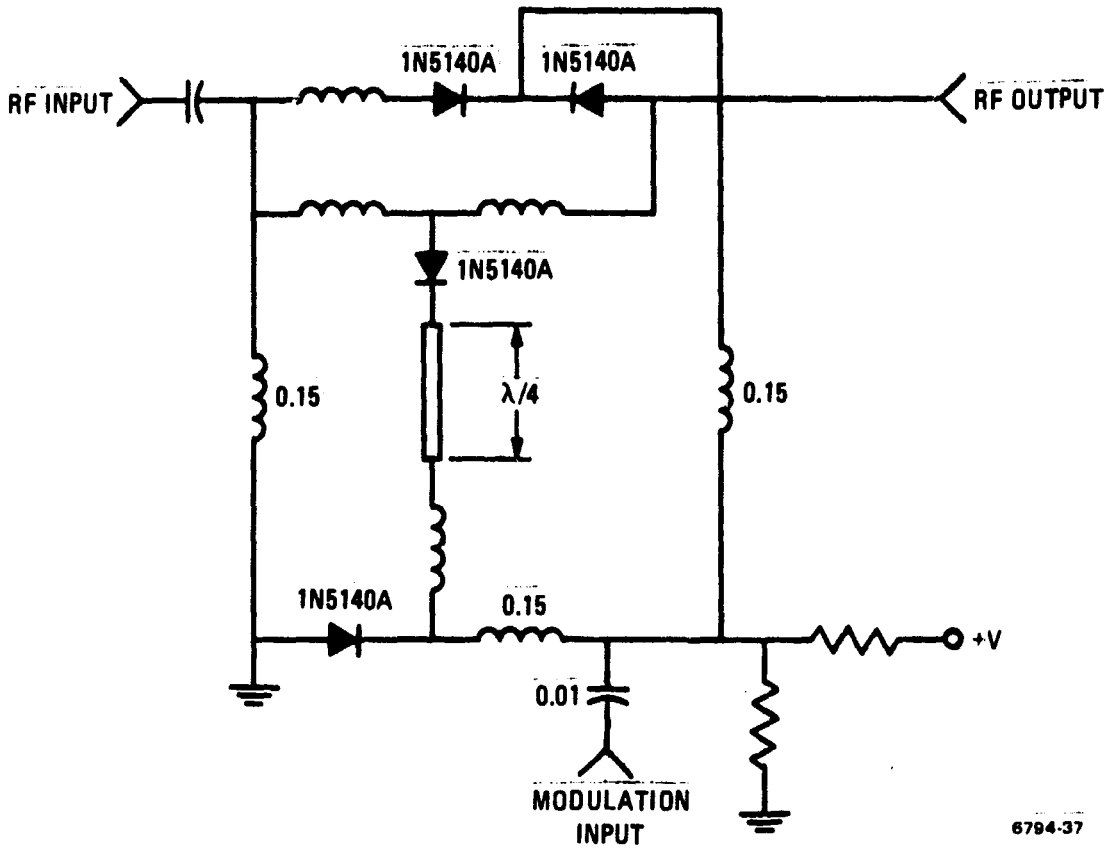


Figure 3-39. Constant Amplitude - Variable Phase Filter

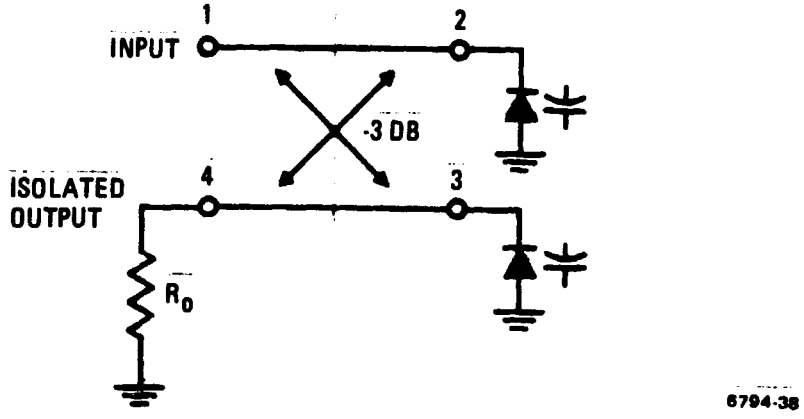


Figure 3-40. VHF Phase Modulator

$$\frac{E_r}{E_i} = p = \frac{Z_T - Z_o}{Z_T + Z_o} = \frac{Z_T/Z_o - 1}{Z_T/Z_o + 1} \qquad (1)$$

The angle of the reflected wave, assuming the incident wave has zero phase, is the angle of equation 1. The simplest form for θ can be found using vectors as shown in figure 3-41 assuming Z_T/Z_o is imaginary.

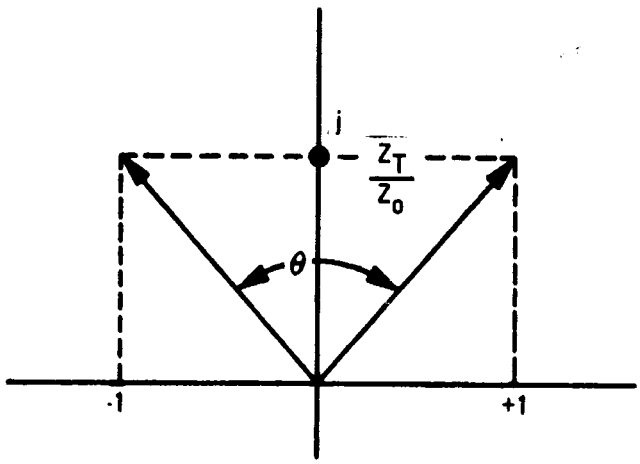


Figure 3-41. Angle of Reflection

Now θ is the angle between the two vectors representing the numerator and denominator of equation 1. Equation 2 gives the expression for the reflection angle.

$$\theta = 2 \tan^{-1} \frac{Z_o}{Z_T} \qquad (2)$$

One accepted formula for a varactor diode capacitance versus voltage characteristic is given by $C = XV^{-\alpha}$ where α is between 1/3 and 1/2 depending on the manufacturing process used for a particular diode.

It was decided to try placing an inductor either in series or shunt with the diode to improve the linearity between phase shift and applied voltage. A computer program was written which allowed voltage, characteristic impedance, inductance, and frequency to vary over specified limits.

The first derivative of θ with respect to voltage was also calculated to determine the % non-linearity of any desired curve. Table 3-1 lists the formulas used for the series "L" and shunt "L" cases. Not included in table 3-1 are the lengthy equations for the second derivatives which were also found in order to determine the inflection point on a curve if one exists. This may be used to find the most nearly linear portion of a curve.

Table 3-1. Formulas for θ and $d\theta/dv$

	Series "L"	Shunt "L"
θ (radians)	$2\tan^{-1}\dfrac{R_o}{WL-V^{\alpha}/WX}$	$2\tan^{-1}\left[\dfrac{R_o}{WL}(1-W^2LXV^{-\alpha})\right]$
$d\theta/dv$ (radians/volt)	$\dfrac{2R_o\alpha V^{-1}}{WX\left[(WL-\frac{V}{WX})^2+R_o^2\right]}$	$\dfrac{2R_oXW^3L^2V^{-\alpha-1}}{W^2L^2+R_o^2(1-W^2LXV^{-\alpha})^2}$

3.4.2.2 Computed Data

To obtain some typical curves the frequency was arbitrarily chosen to be 500 MHz with a diode whose capacitance is 10 pf at 0 volts (5 pf at -4 volts) with $\alpha = .5$. Characteristic impedances between 20 and 100 ohms are considered.

Figures 3-42 through 3-45 show information with an inductance placed across the varactor diode. They show the sensitivity of θ versus voltage increasing with increasing characteristic impedance. These curves do not indicate good linearity over a wide range of control voltage.

Figures 3-46 through 3-48 show the effect of using a series inductance. For this case the sensitivity is good and the linearity can be very good depending on the value of inductance used. These curves show decreased sensitivity with increased characteristic impedance.

It is interesting to note what effect the varactor diode law, α, has on sensitivity. Figure 3-49 shows the dependence of linearity and sensitivity on the value of "L" for R_O = 20 ohms and $\alpha = .4$. A better evaluation of the effect α has is shown

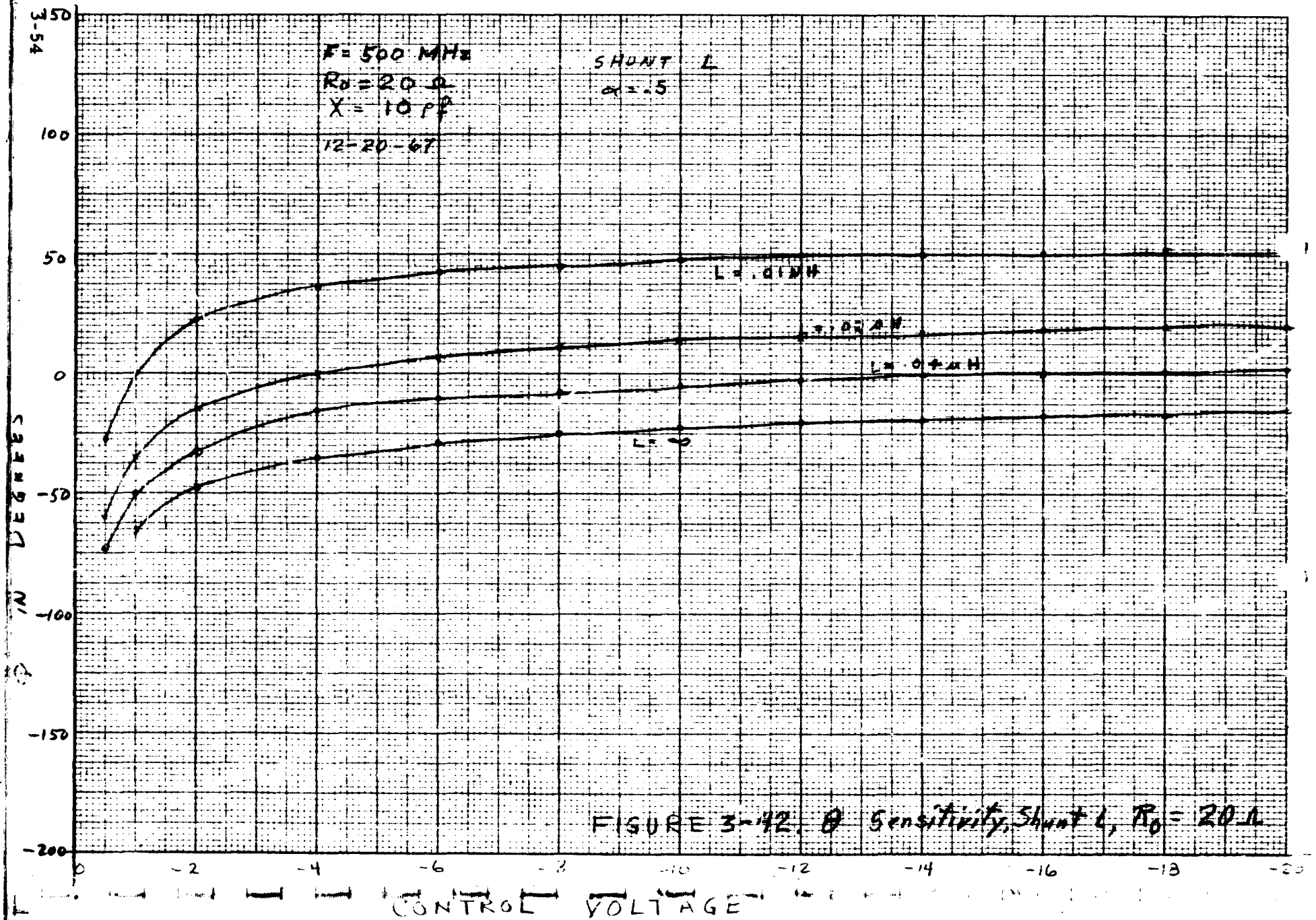


FIGURE 3-42. Q Sensitivity, Shunt L, R_0 = 20 Ω

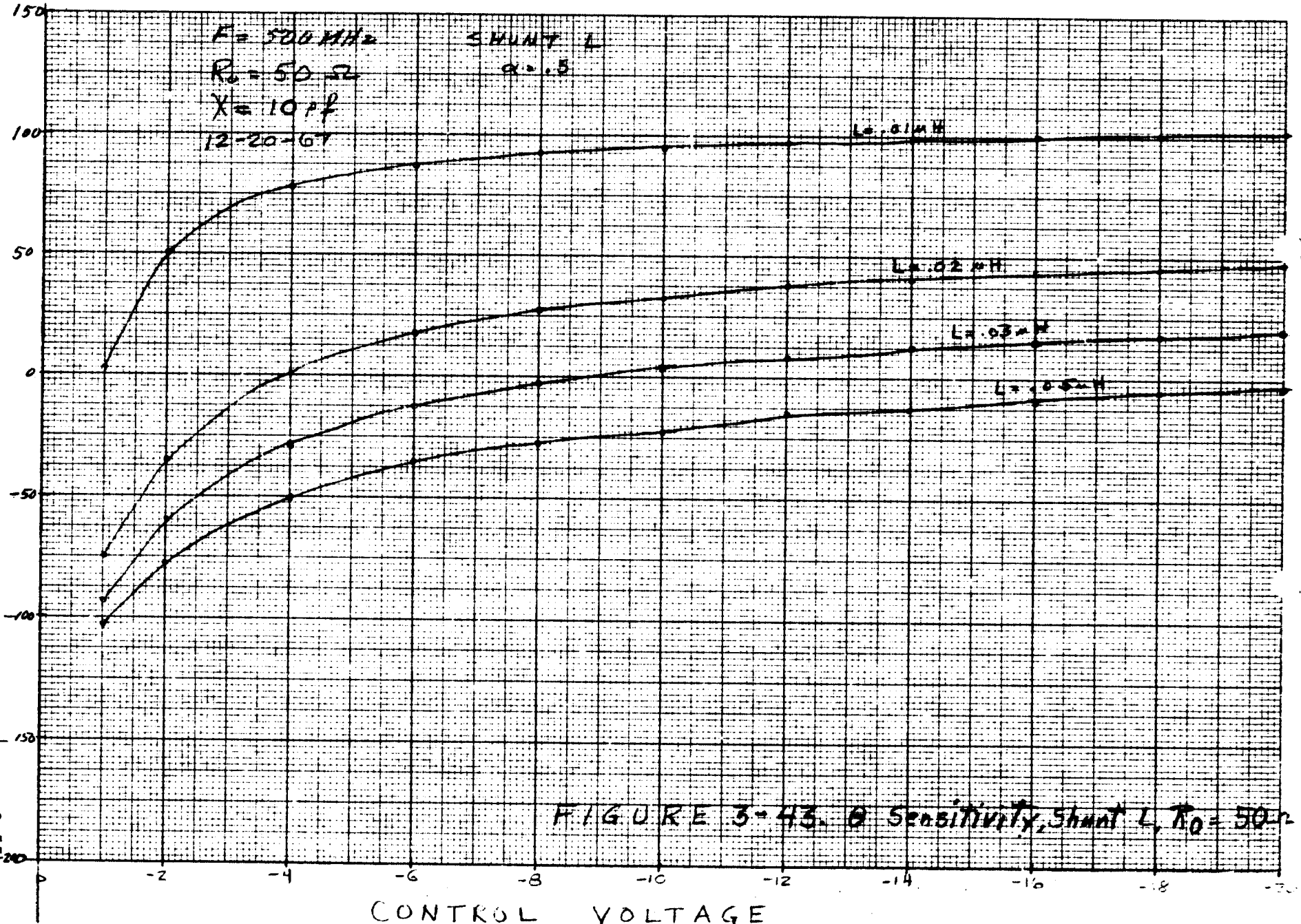


FIGURE 3-43. Φ Sensitivity, Shunt L, R_o = 50 Ω

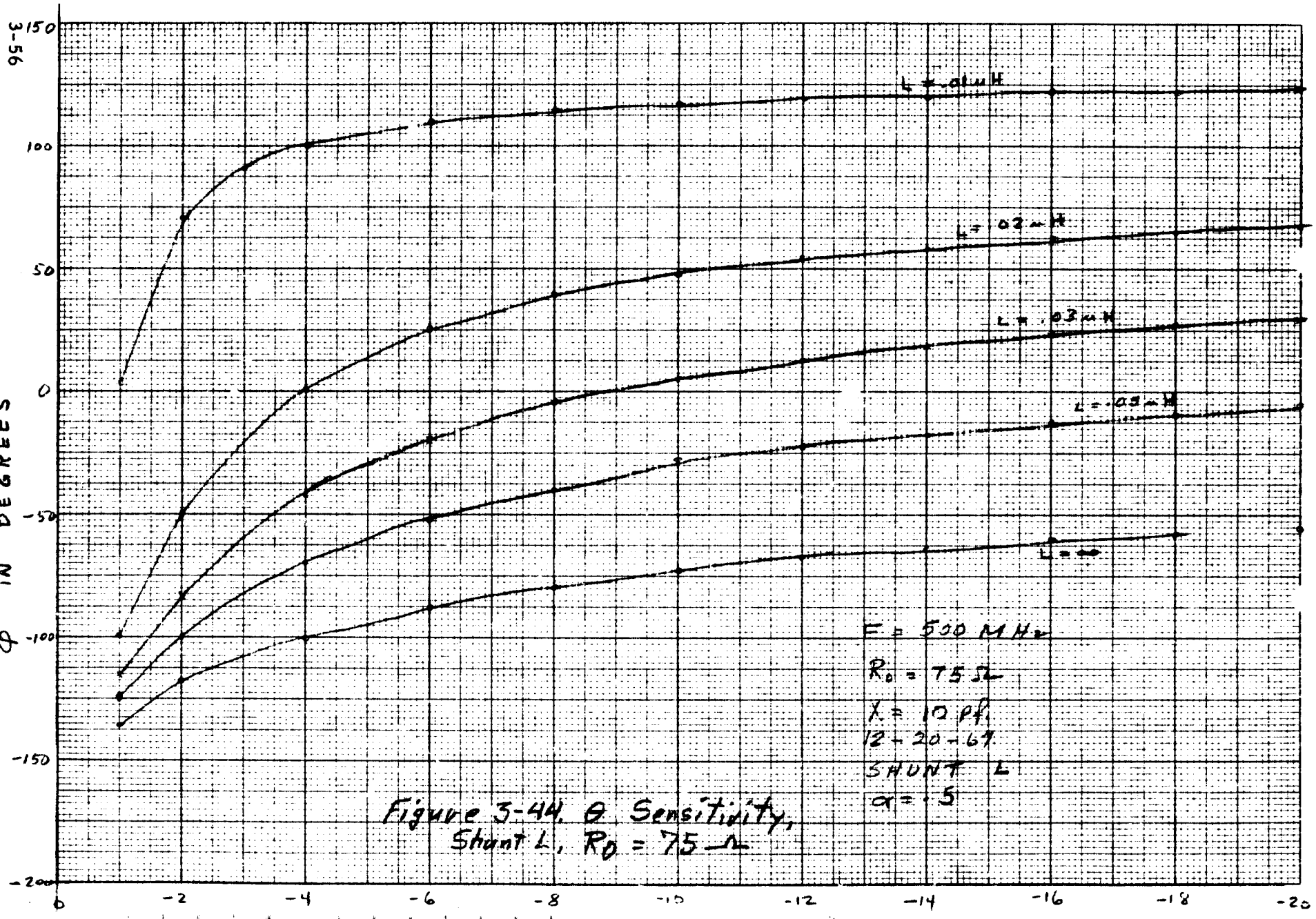


Figure 3-44. θ Sensitivity, Shunt L, $R_0 = 75\ \Omega$

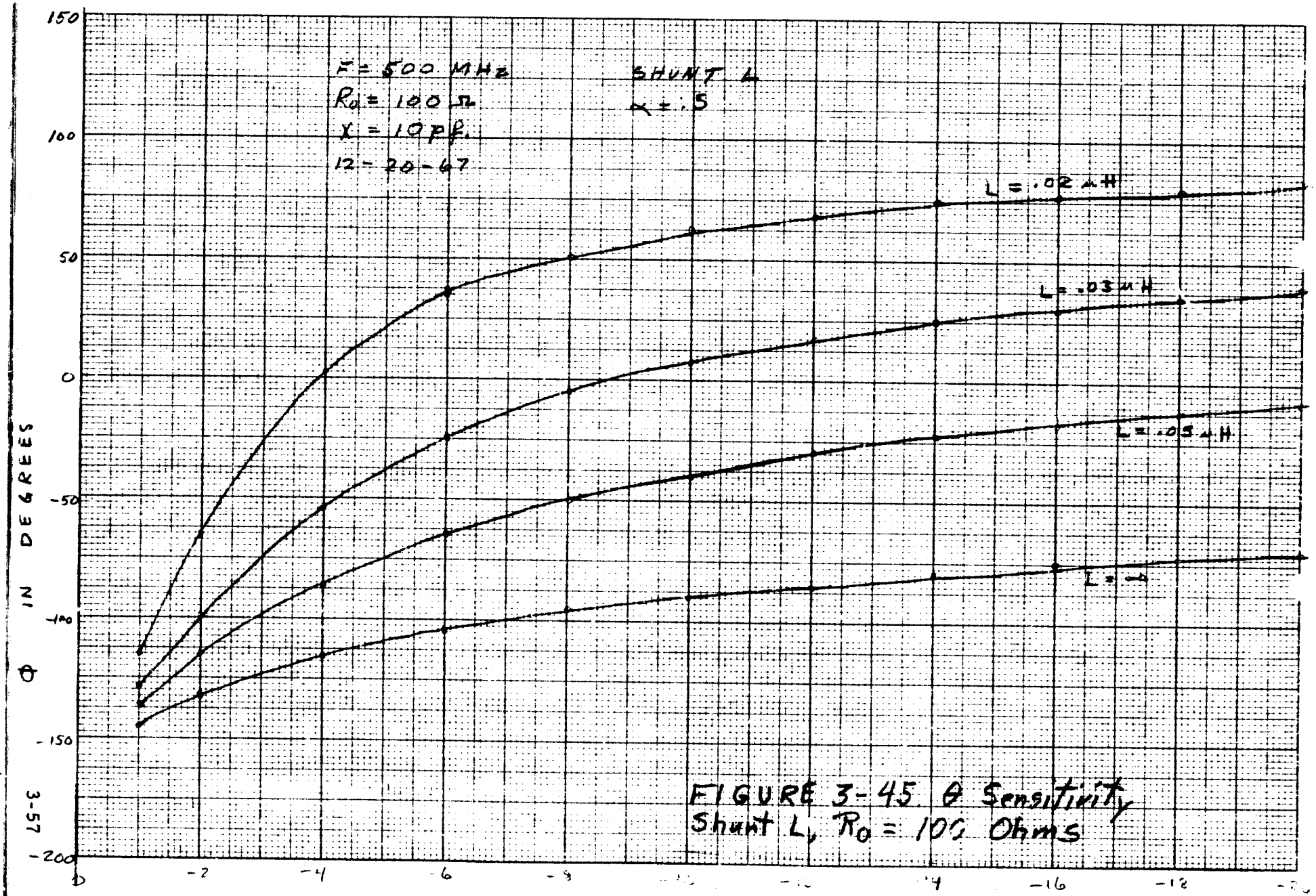


FIGURE 3-45 θ Sensitivity, Shunt L, R_o = 100 Ohms

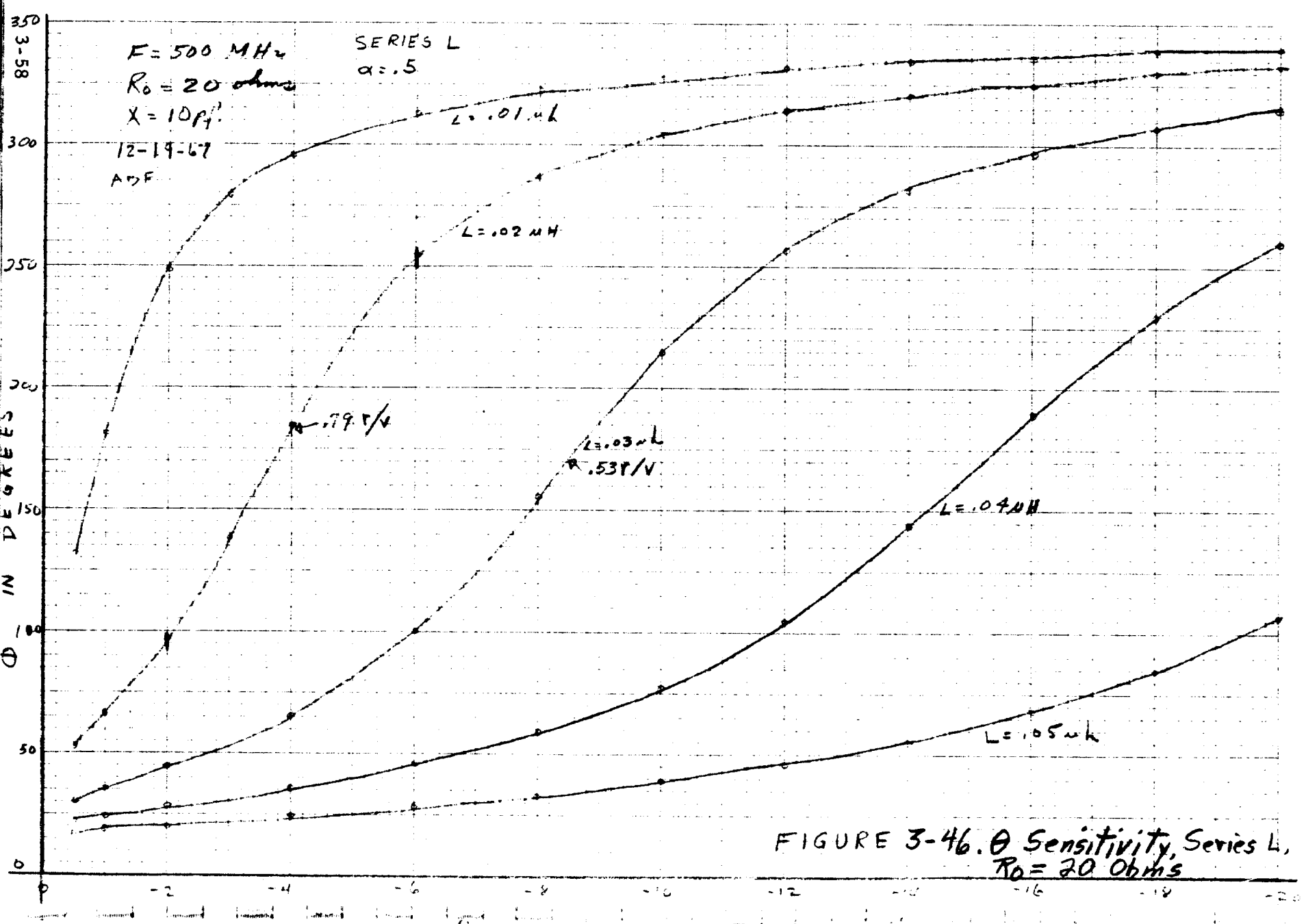


FIGURE 3-46. Θ Sensitivity, Series L, R_0 = 20 Ohms

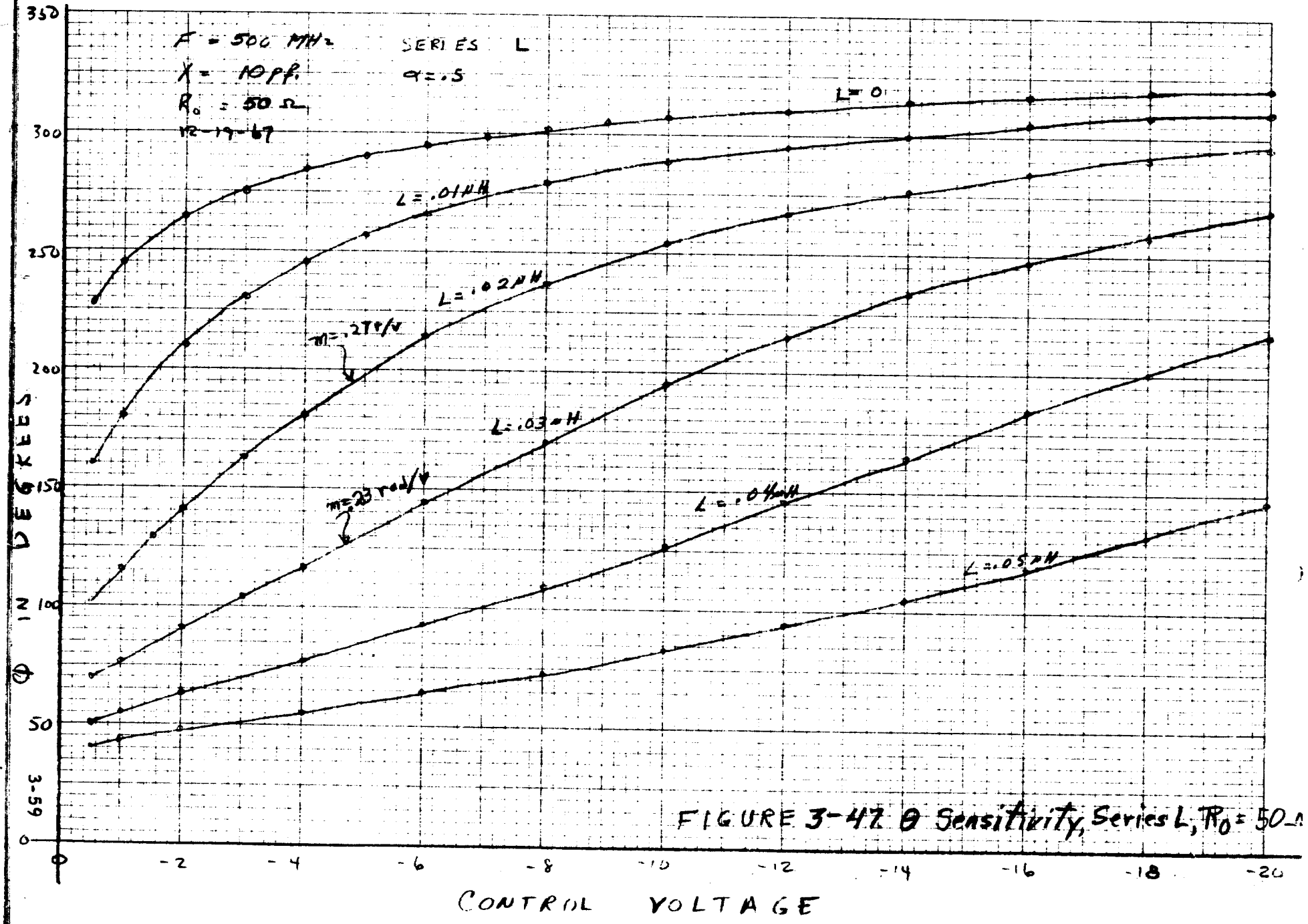


FIGURE 3-47 Θ Sensitivity, Series L, R_o = 50Ω

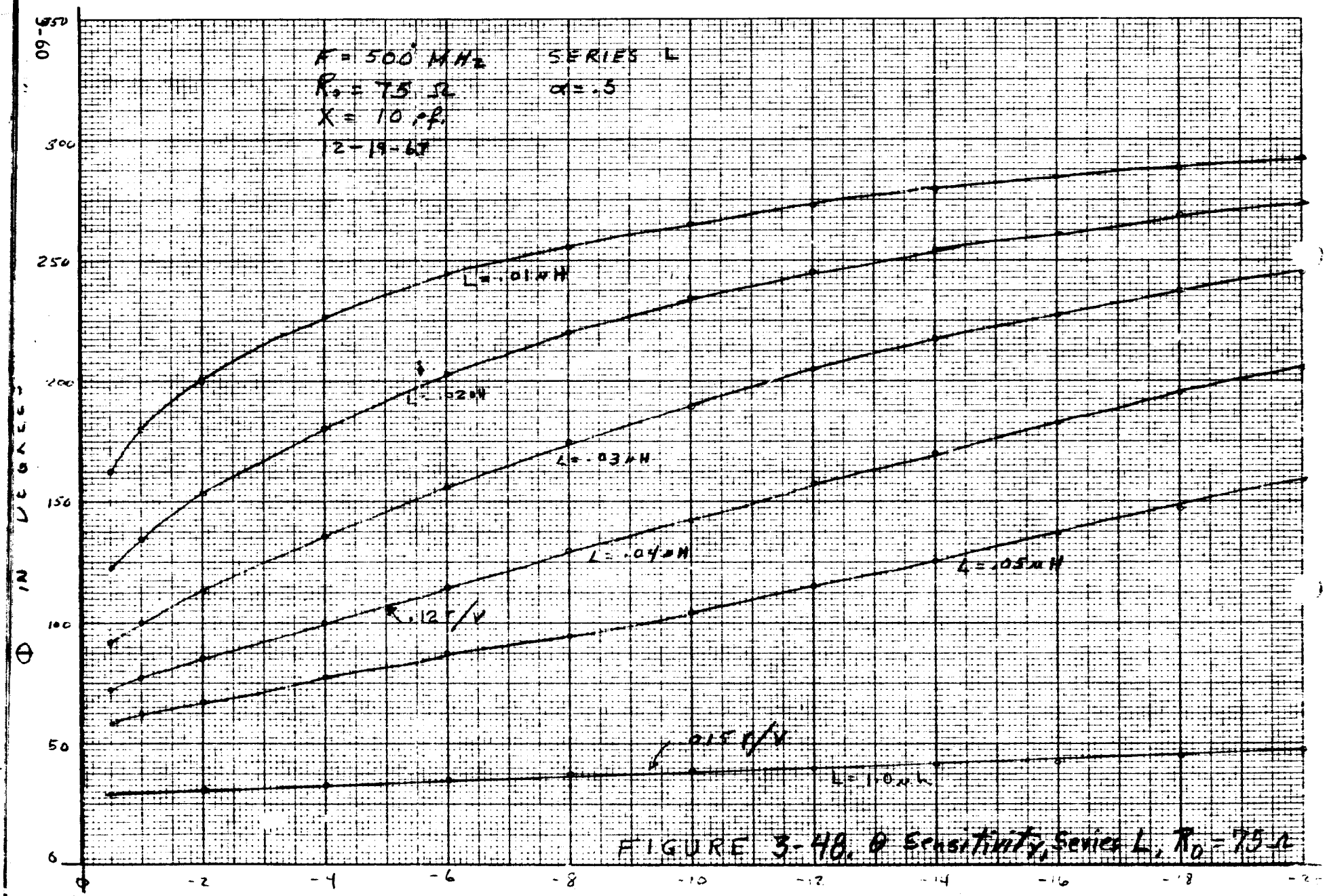


FIGURE 3-48. Φ Sensitivity, Series L, R_o = 75 Ω

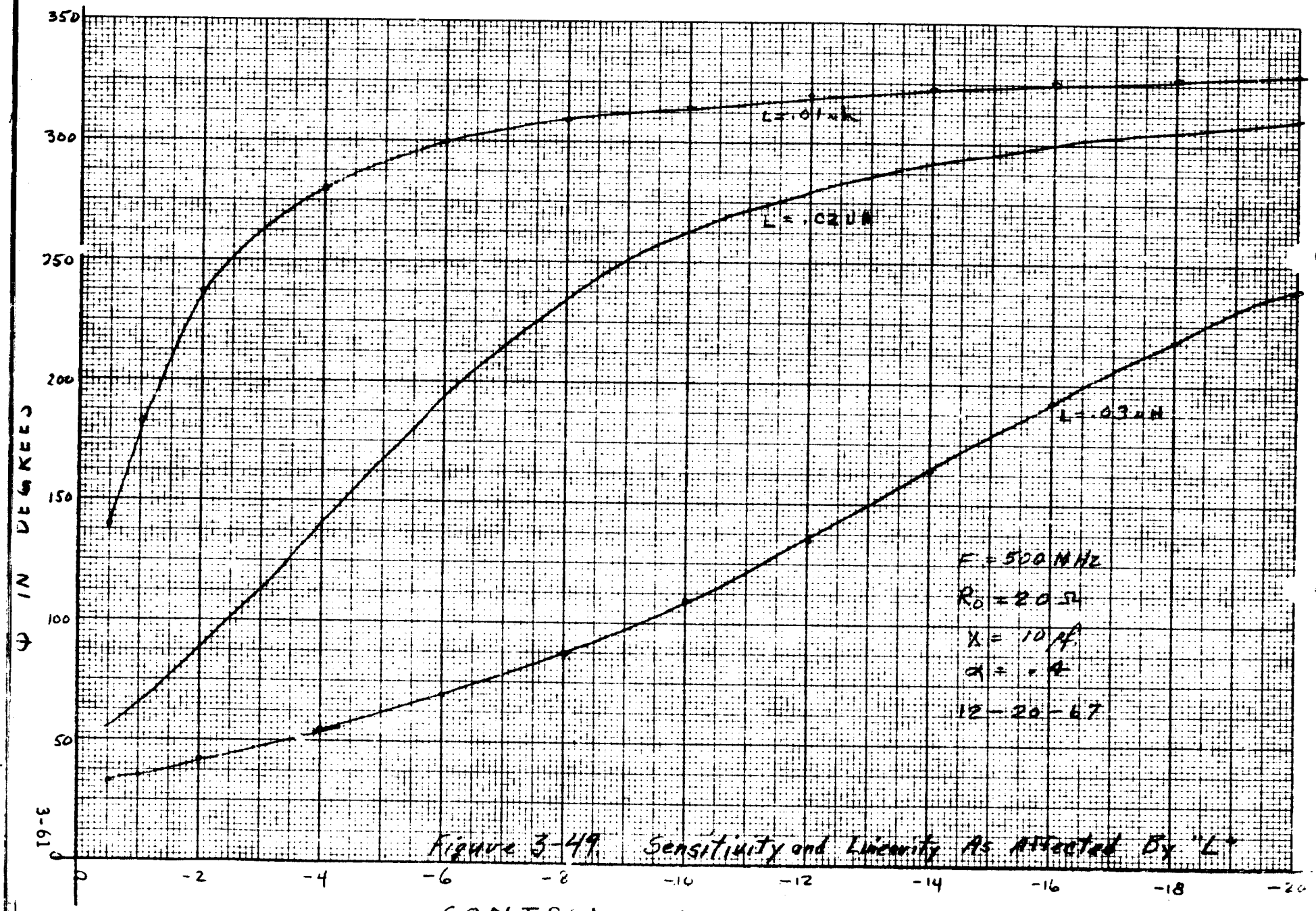
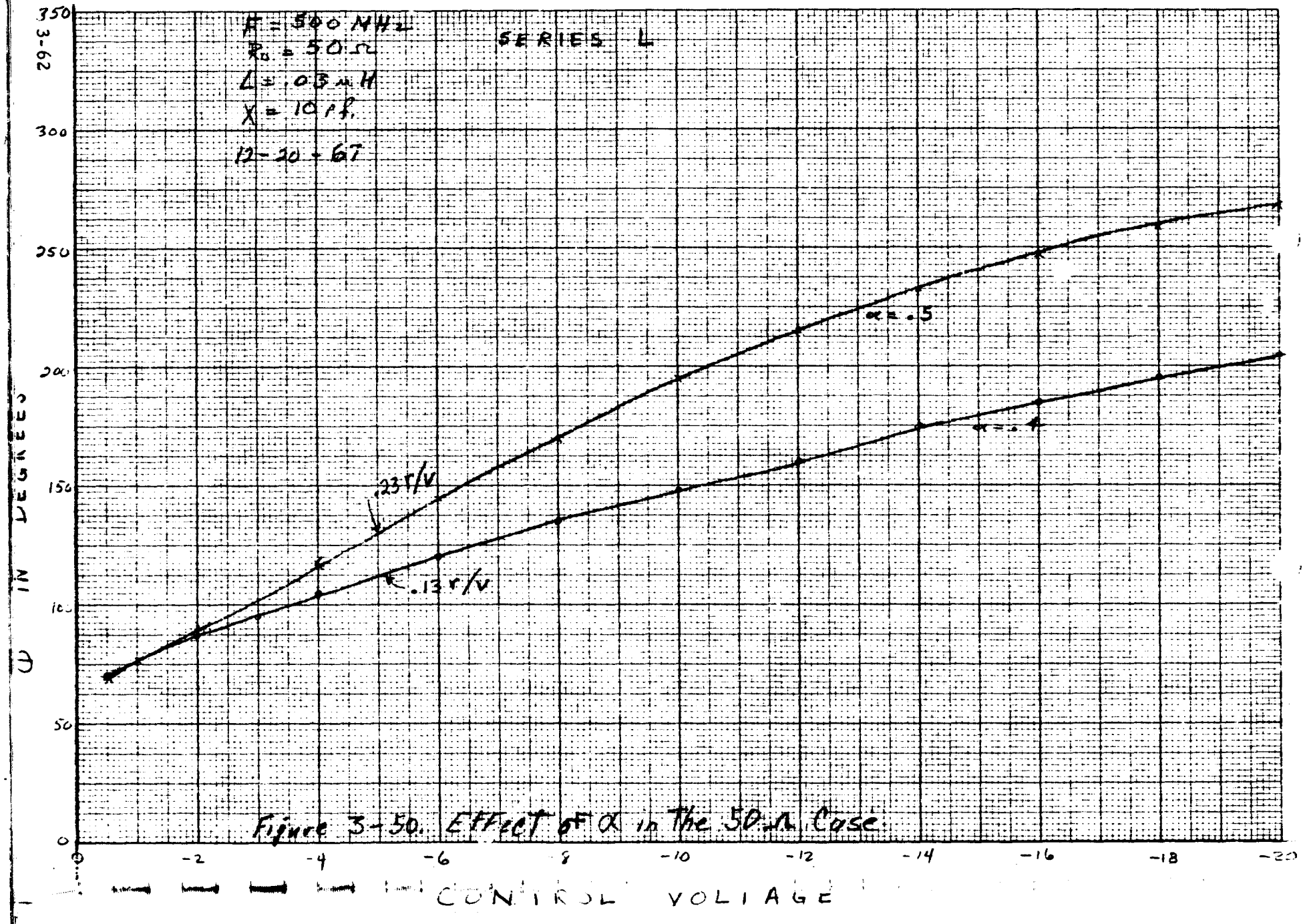
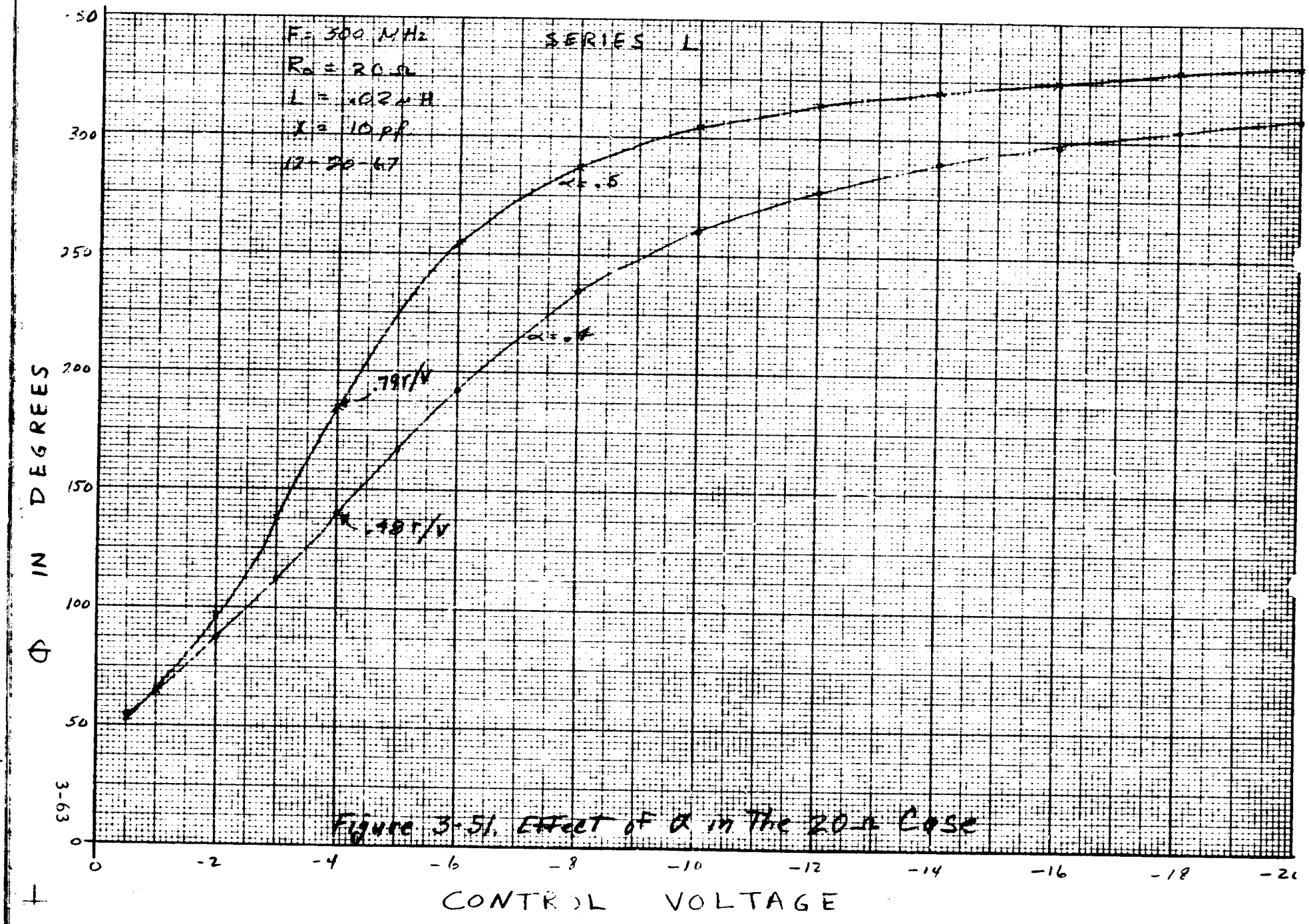


Figure 3-49. Sensitivity and Linearity As Affected By 'L'



3-62

Figure 3-50. EFFECT OF α in The 50Ω Case



3-63

Figure 3-51. Effect of α in The 20-Ω Case

by figures 3-50 and 3-51. These curves show the effect of α for a fixed value of inductance for the 20 ohm and 50 ohm cases. The different sensitivities are indicated for additional comparison.

It is now desired to determine just how linear this phase modulator could be. The method chosen to express the non-linearity is per cent deviation from linear. The definition can better be understood by referring to figure 3-52. The per cent deviation is $\Delta\theta'/\Delta\theta$ taken over the interval ΔV. This non-linearity is referenced to a straight line through (θ_o, V_o) and the slope is equal to the calculated slope at (θ_o, V_o). The computer program now gives enough information to calculate the per cent non-linearity at any point, V_1 or V_2.

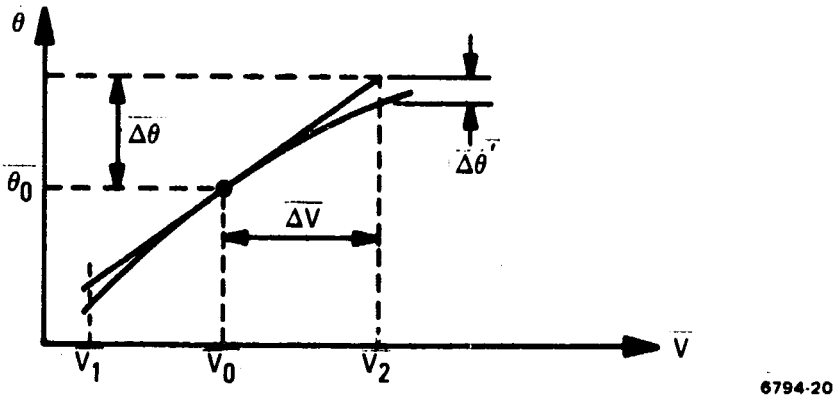


Figure 3-52. Definition of Non-Linearity

Table 3-2 lists a few selected curves for which the non-linearity was calculated. If the signs of the per cent non-linearities for $\pm$ V are opposite, the actual curve is tangent to, but does not cross over the straight line reference. This is the case for the 75 ohm hybrid as listed in table 3-2.

The per cent non-linearity could be reduced by reference to a slightly different nominal sensitivity (or slope). This can only be done if the percentage change for + V is different than the percentage change for - V. No attempt was made to do this for the computed data.

Table 3-2. Non-Linearity in UHF Phase Modulator Series Inductance

$\alpha = .5$

R_o(ohms)	L(μH)	V_o	V	θ (radians)	% Non-Linearity
20	.02	-3.5	+1	+.79	-5.1
20	.02	-3.5	-1	-.79	-4.3
20	.02	-3.5	+.5	+.41	-1.5
20	.02	-3.5	-.5	-.41	-1.0
50	.03	-6	+4	+.89	-5.9
50	.03	-6	-4	-.93	-1.5
50	.03	-6	+3	+.68	-3.7
50	.03	-6	-3	-.70	-1.0
50	.03	-6	+2	+.46	-1.9
50	.03	-6	-2	-.47	-0.5
75	.04	-8	+4	+.48	-1.6
75	.04	-8	-4	-.49	+0.8
75	.04	-8	+2	+.24	-0.4
75	.04	-8	-2	-.25	+0.2

Figures 3-42 through 3-48 clearly indicate that a series inductance works much better than a shunt inductance to linearize this type of modulator. This is rather unfortunate since a shorted transmission stub would make a good shunt inductance. Inductances from 20 to 40 nanohenrys could be difficult but not impossible to make. For best results it will probably have to be an adjustable coil. A larger coil can be used only at the expense of a smaller capacitor or lowering the frequency. It is felt that a smaller capacitance diode would not be desirable due to strays and other uncertainties. The quadrature hybrid itself is easily built using stripline techniques.

Table 3-2 contains most useful information, in that it indicates that a half radian peak variation with only $\pm$1% error can be expected. There is also the

possibility of cascading 2 or more of these phase modulators which may result in better linearity at the expense of more circuitry. For example, the last 75 ohm entries in table 3-2 indicate the possibility of getting .5 radian peak variation with only $\pm$.6% distortion by cascading two identical modulators.

One important characteristic of this phase modulator which has not been mentioned is the amplitude modulation present on the output for a constant voltage modulating signal. Such amplitude variation would arise if the diode Q varied over the dynamic range of modulating signal. This could be a problem because present varactors do not have a high Q at 500 MHz and their Q probably varies somewhat with reverse voltage. The extent of this problem deserves additional investigation consisting of experimental results. The diode Q will also affect the device insertion loss.

More sophisticated phase modulators have been designed and can be found in the literature. One paper[1] describes the design of an S-band modulator with only 0.5% distortion. It consists of 4 quarter wavelength lines, two varactors, 4 line stubs, and a circulator. Another idea uses a symmetrical LC bridge network with 2 L's and 2 varactors. However, its input impedance may vary as C varies.

3.4.2.3 Circuit Design

From the computed data the inductive reactance of approximately 100 ohms in series with the varactor diode is the condition for optimum linearity, assuming the capacitance of the diode varies as $\frac{1}{\sqrt{E}}$ where E is the diode reverse voltage.

Various lengths of line less than a quarter wave were tried for the series inductance, but nothing less than 3% could be obtained. Triple stub tuners were then placed in place of the stripline. By adjusting the stubs less than 0.5%

1. Kim, Lee, and Borer, "Varactor S-band Direct Phase Modulator", IEEE Journal of Solid-State Circuits, Vol. SC-1, No. 1, Sept. 1966.

distortion could be obtained. It became obvious that the length of line could not be controlled closely enough to get this low distortion. Therefore, tuning capacitors were added in parallel with a nominal length of line. By tuning the capacitors, second and third harmonic distortion of approximately 0.5% could be obtained.

Input vswr was most adversely affected by imbalances in the diode capacitances. The imbalance caused unequal reflection angles from the two high impedance ports causing incomplete cancellation at the input port. Therefore, balanced diodes must be used. Figure 3-56 is a schematic of the complete circuit.

3.4.3.4 Test Results

The results of tests performed on the breadboard 560 MHz phase modulator described above, are tabulated below.

1. Modulation Sensitivity

   0.212 radian peak/volt rms measured at 100 kc

2. Distortion

   Tabulated below is the second and third harmonic distortion for various input power levels.

RF Power Input (dbm)	Distortion (%) 2nd Harmonic	3rd Harmonic
+ 5.0 (3.2 m watts)	.75	.10
+10.0 (10 m watts)	.63	.88
+15.0 (31.5 m watts)	.79	.50
+20.0 (100 m watts)	.79	.50
+25.0 (253 m watts)	.89	.50
+30.0 (1.0 watts)	1.40	.16
+31.7 (1.5 watts)	1.50	.14
+33.0 (2.0 watts)	1.00	.20
+35.0 (3.2 watts)	1.68	-

Figure 3-53

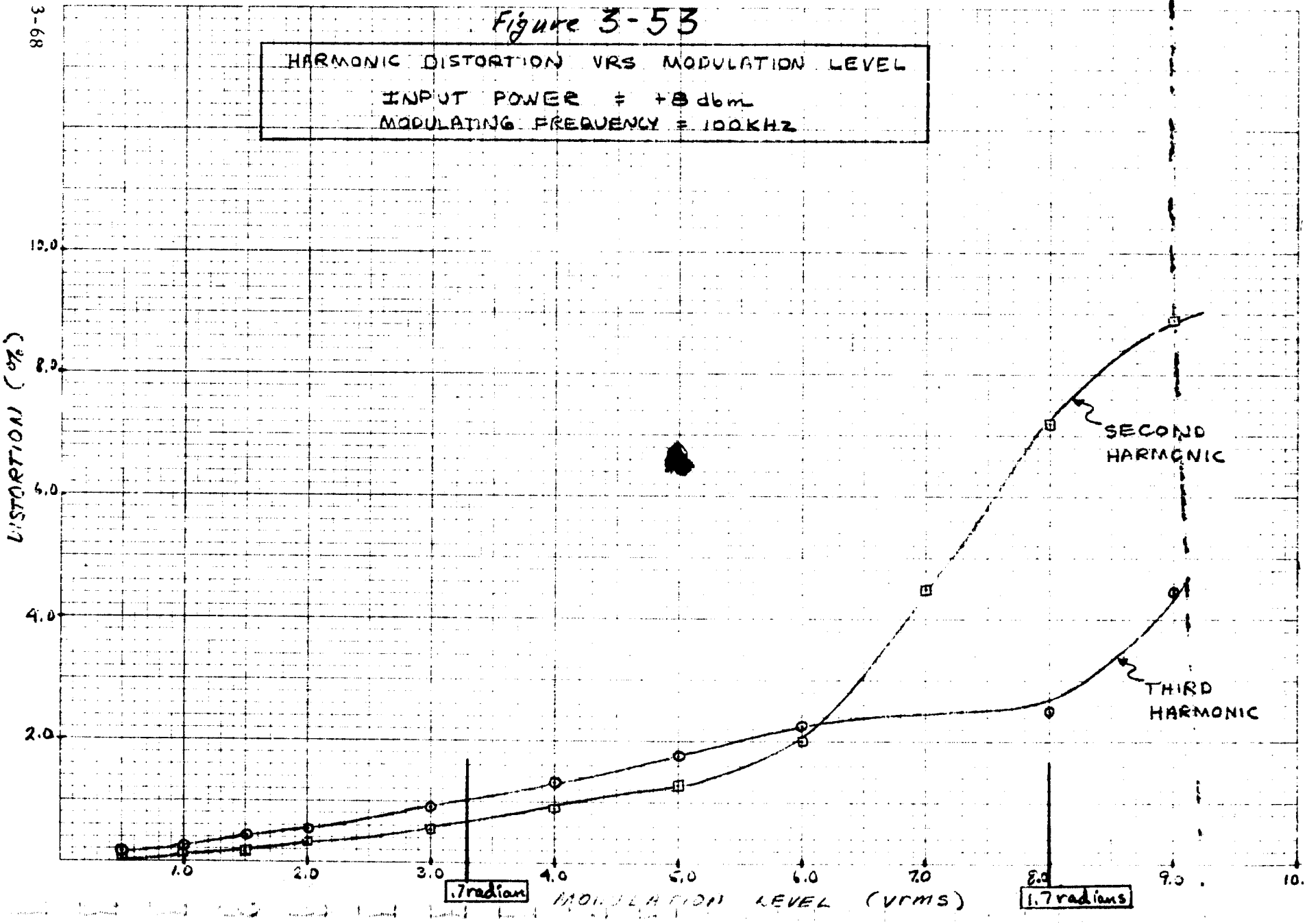
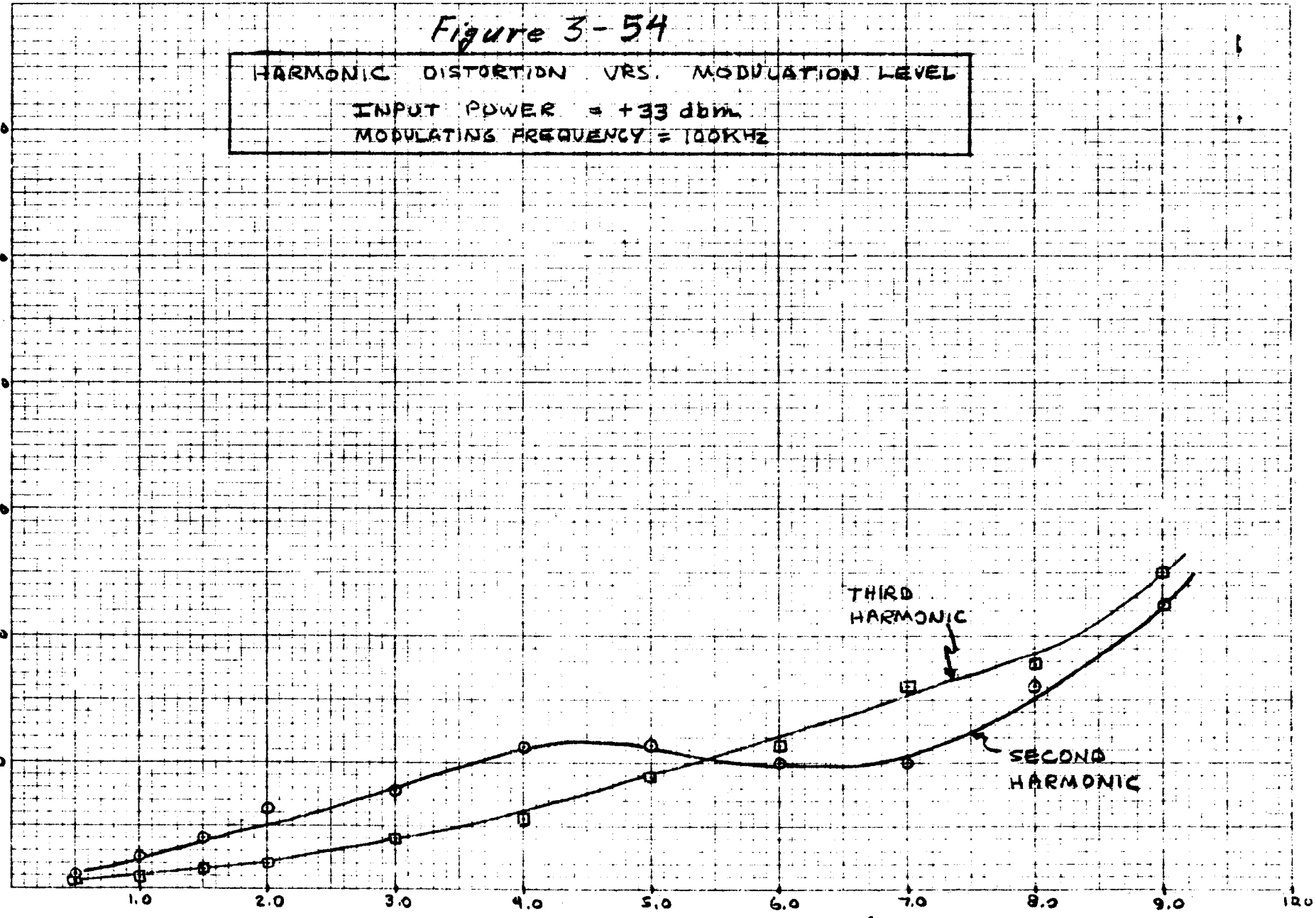

HARMONIC DISTORTION VRS MODULATION LEVEL
INPUT POWER = +8 dbm
MODULATING FREQUENCY = 100KHz
DISTORTION (%)
10.0
8.0
6.0
4.0
2.0
SECOND HARMONIC
THIRD HARMONIC
1.0
2.0
3.0
.7radian
4.0
5.0
6.0
7.0
8.0
1.7radians
9.0
10.
MODULATION LEVEL (VRMS)

Figure 3-54

HARMONIC DISTORTION VRS. MODULATION LEVEL

INPUT POWER = +33 dbm
MODULATING FREQUENCY = 100KHz



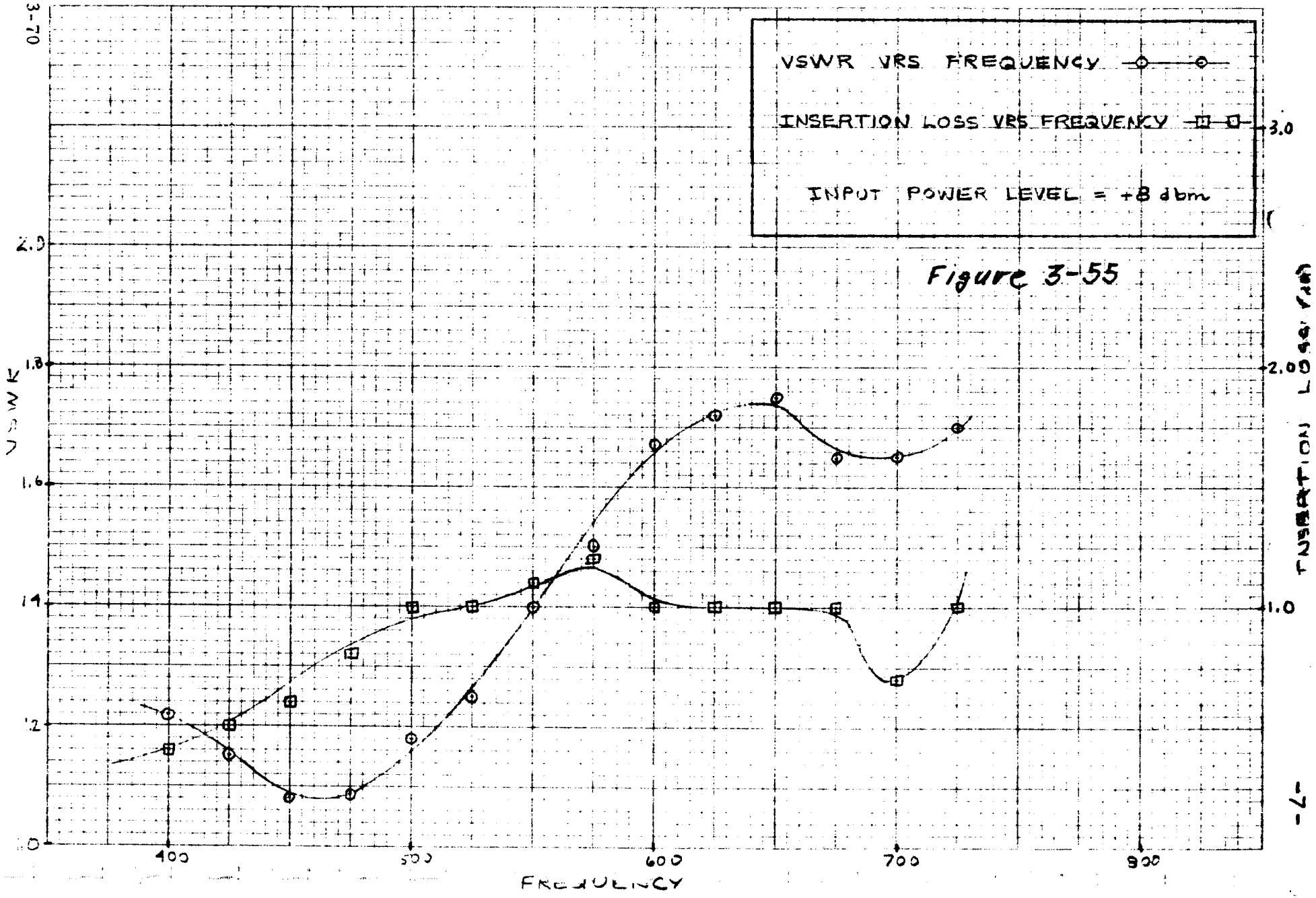


Figure 3-55

Figures 3-53 and 3-54 show 2nd and 3rd harmonic distortion versus modulation level at two power levels (+8 dbm and +33 dbm). Additional distortion is in the form of a-m. Approximately 1.6% a-m is produced.

3. Frequency Response

   Upper 3 db bandwidth is 46.5 MHz

4. Insertion Loss

   See figure 3-55

5. VSWR

   See figure 3-55

6. Temperature

   No significant deterioration from the above data is evident over the temperature range of +85°C to -30°C.

The data presented shows that a phase modulator operating at 560 MHz is capable of excellent performance. With the incorporation of the above mentioned improvements this circuit should provide an easily manufactured and reliable phase modulator.

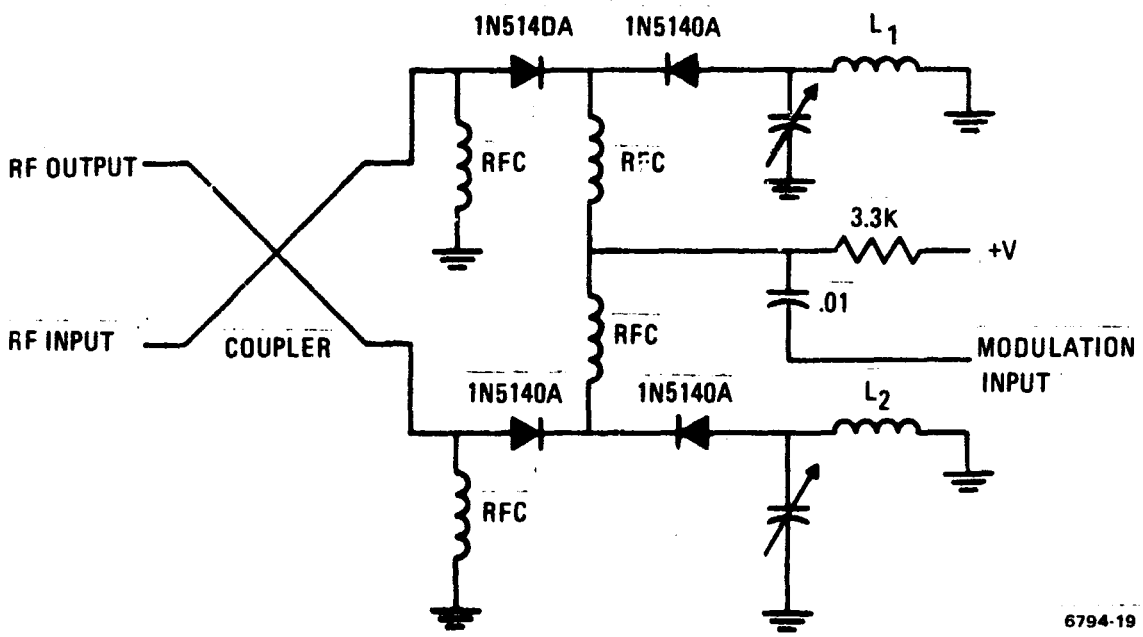


Figure 3-56. Phase Modulator

3.4.3 Low Level Power Amplifier

The objectives were to develop a 560 MHz single transistor amplifier with a 500 milliwatt drive with 2.5 watts out and greater than 60 per cent efficiency.

A schematic diagram of the amplifier is shown in figure 3-57. The TRW 2N4430 was chosen for its stripline packaging and power rating. A test fixture was used to determine the device parameters under Class C operation. A diagram of the fixture is shown in figure 3-58. The base and collector impedances were measured by substituting a test point at the base and collector when the transistor was removed. The base input impedance was measured to be 6 ohms and the collector output impedance was measured to be 47.5 ohms. Since the collector impedance transformation is not severe, a broadband matching network can be easily achieved. The base requires a high impedance transformation and broad bandwidths are harder to achieve. Tapered line techniques appeared to yield the broadest bandwidths possible. Test fixtures were made to determine the network for best matching the base and collector impedances to 50 ohms. Impedance transformers using steps in line width are usually one-quarter wavelength long. Tapering lines allow for considerable foreshortening of the lines. Figure 3-59 shows the final layout after the lines had been trimmed in the final configuration. Second harmonic traps (stubs S1 and S2 in figure 3-59) present a short circuit to the second harmonic at the base and collector and are necessary for maximum gain. Stub S3 adds the capacitive-reactive component to the collector. The base had two tuning adjustments (C1 and C2) to account for transistor parameter variations.

The matching networks, printed on both sides of .01 inch teflon board, also form coupling networks with the input and output on one side of the board and the transistor on the other to eliminate the need for chip capacitors for dc blocking.

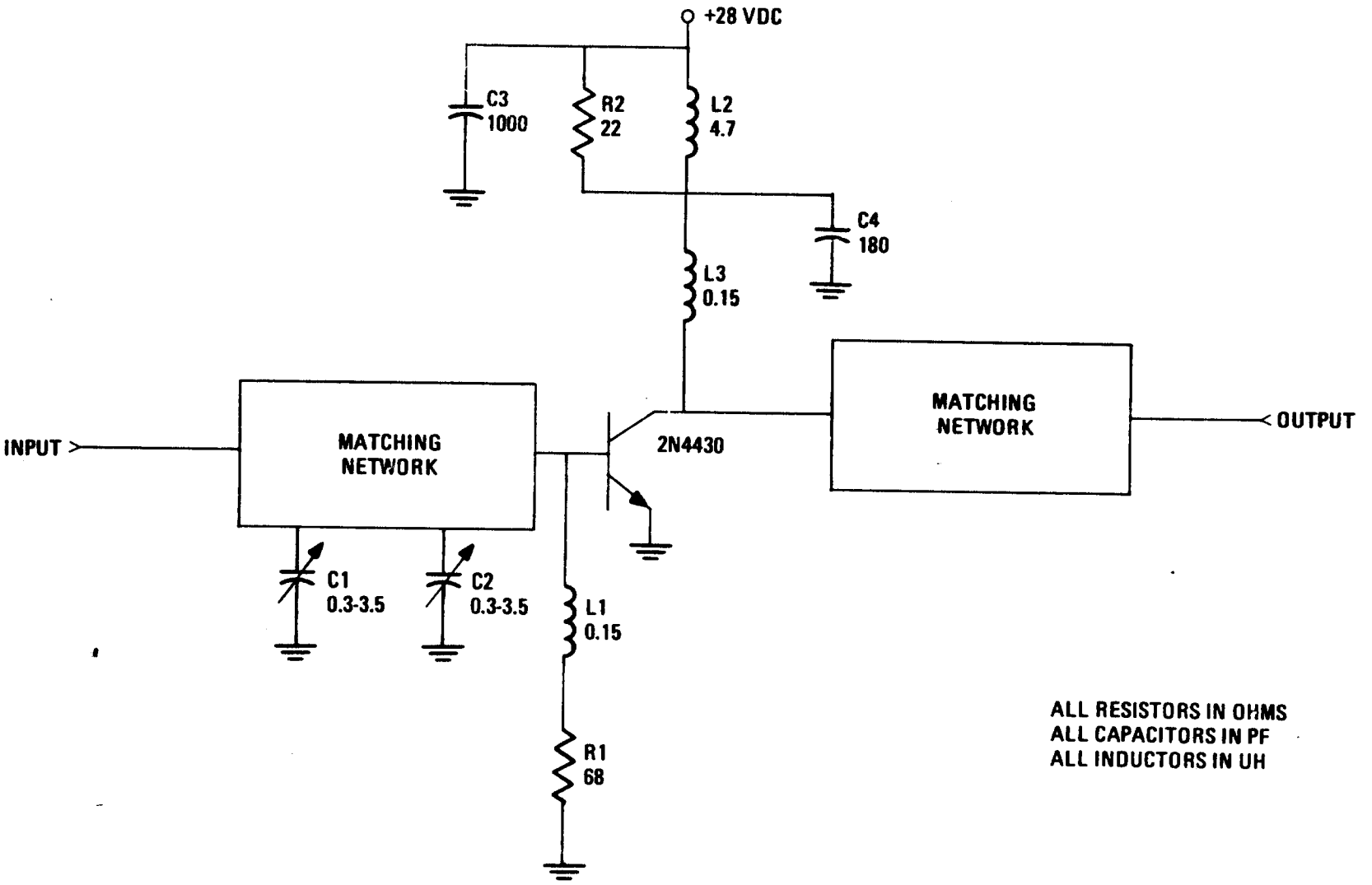


Figure 3-57. 560 MHz Amplifier Schematic Diagram

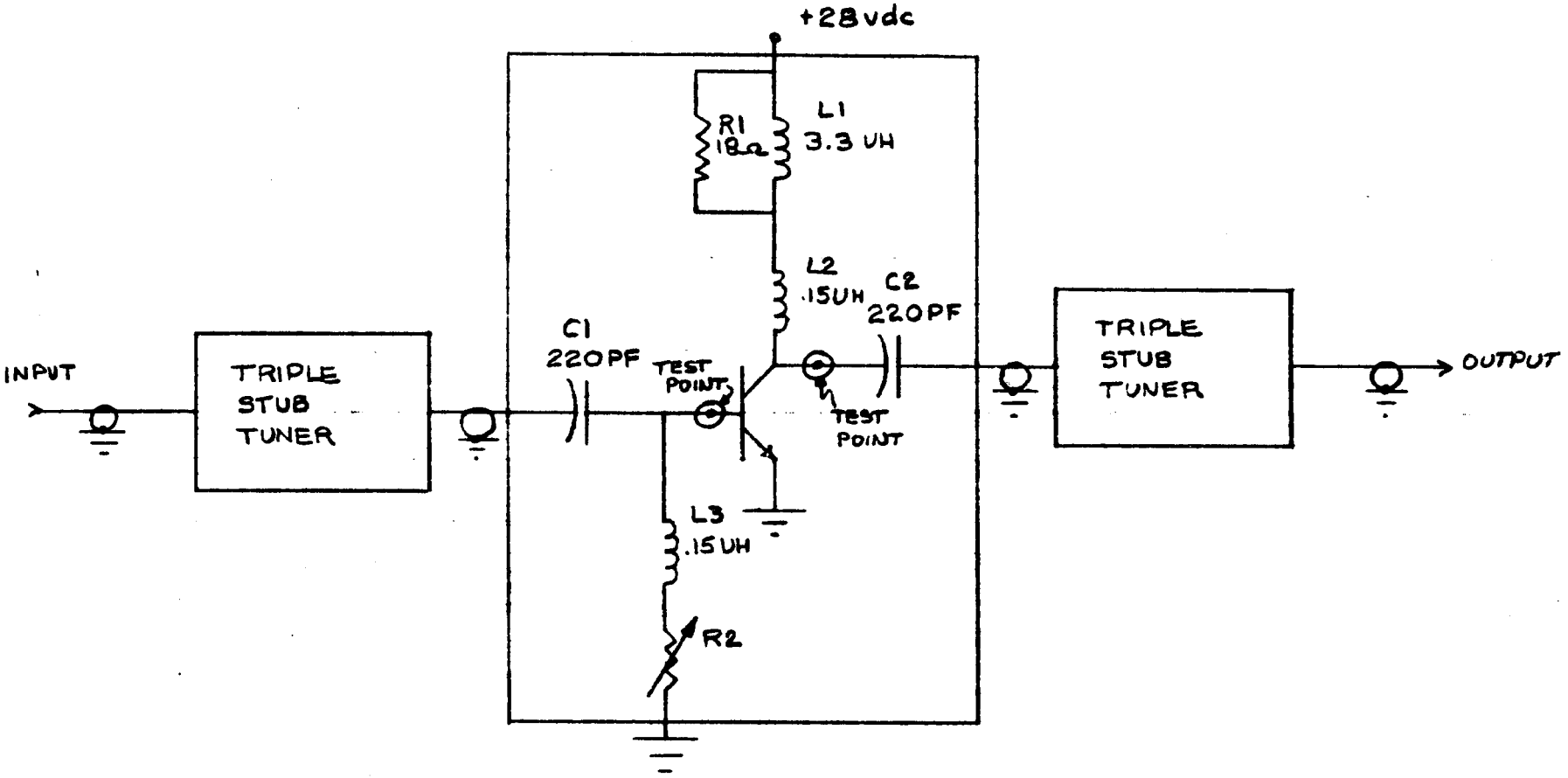


Figure 3-58. 560 MHz Transistor Test Fixture

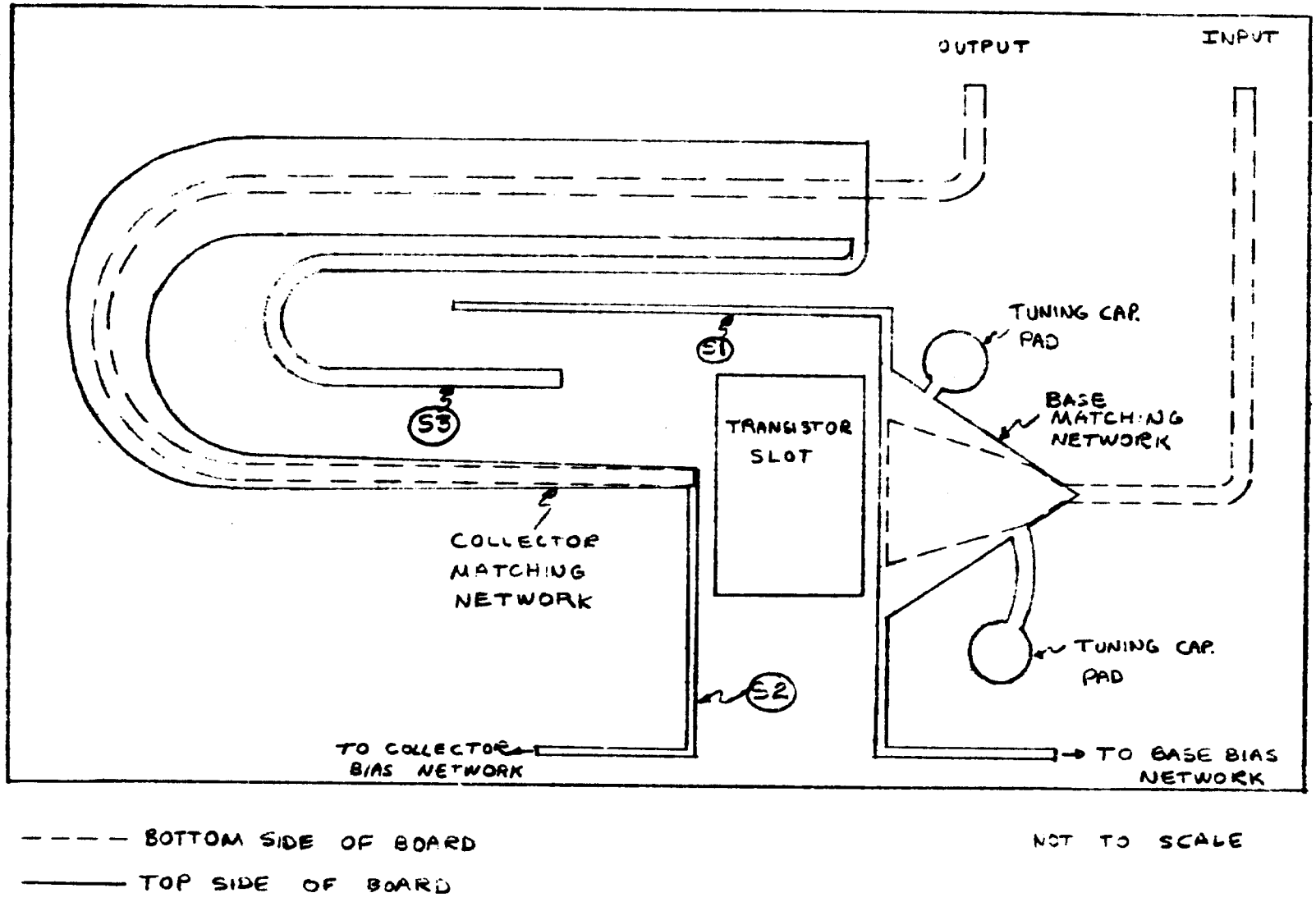


Figure 3-59. Layout of Matching Networks in Amplifier

With an input power of 500 milliwatts at 560 MHz the following data was taken.

Temperature (^{o}C)	Power Out (Watts)	Input VSWR	Efficiency (%)
Ambient	2.6	1.32:1	57.3
0	2.58	1.32:1	60.8
+90	2.54	1.75:1	49.0

Input vswr 2.1:1 bandwidth is 33 MHz.

Output 1 db bandwidth = 49 MHz.

Output 3 db bandwidth = 88 MHz.

3.4.4 Multipliers

The high frequency multipliers used in the transmitter are described in this paragraph. The 1.1 and 2.2 GHz varactor frequency multipliers are of the same design except for frequency input and output coupling.

3.4.4.1 Single Diode Multiplier

A single diode varactor multiplier is utilized in multiplying from 560 to 1125 MHz. It is basically a half section of the dual output multiplier but scaled down in frequency.

A half section of the multiplier, in stripline configuration, is shown schematically in figure 3-60.

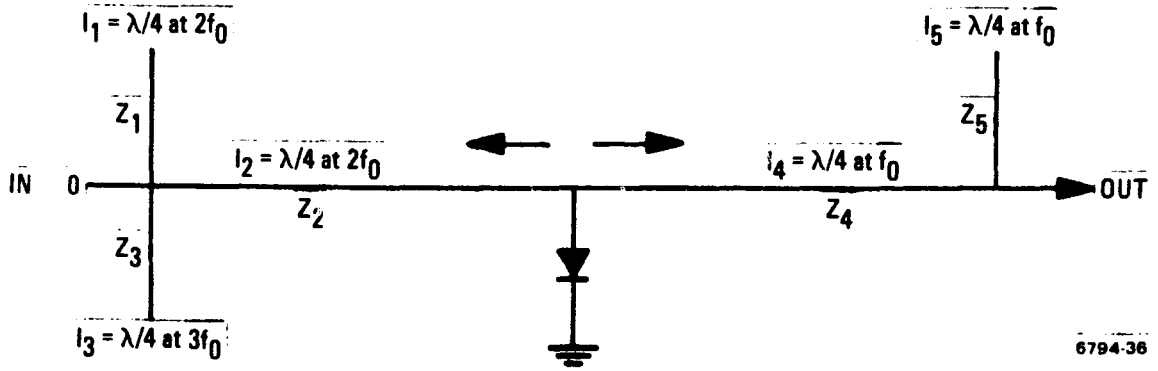


Figure 3-60. Single Diode Frequency Multiplier, Stripline Configuration

Line lengths are provided which restrict the generated frequency from being loaded by the input but the output port is not seen by the input frequency. This is accomplished by means of resonant lines in stripline form.

Looking back to the input from the diode, which is the $2f_o$ generator, one sees lines l_1 and l_2 which provide an open circuit for $2f_o$ because the total line length is $\lambda/2$, open circuit. The input obtains its match to the diode by means of the characteristic impedance of l_2 and the shunt impedance of l_1 at the f_o frequency. Line l_3 provides a short to $3f_o$ because it is a $\lambda/4$ open line at $3f_o$.

Looking from the diode to the output one sees basically the reverse, f_o sees a high impedance by means of l_4 and l_5 which are $\lambda/4$ length lines at f_o. Again the impedance of the diode to the $2f_o$ output is matched by means of the characteristic impedance of line l_4 and shunt line l_5.

The single device low frequency multiplier can be constructed to obtain 70% or greater efficiency.

3.4.4.2 Dual Diode Multiplier

The output multiplier (1100 to 2200 MHz) utilizes two of the single diode multiplier configurations. Combining the inputs and outputs of a dual unit provides in a unilateral arrangement advantages in both isolation and heat dissipation.

A schematic of a unilateral stripline frequency multiplier is shown in figure 3-61.

The use of 3 db couplers splits the power on the input and sums the doubled frequency in the output. The diodes are fed 90^o out of phase, and an added 90^o phase shift is needed in the output circuit to put the signal into proper phase to sum.

Advantages of this configuration are, that larger amounts of power may be handled with good diode derating and that the input vswr remains constant when the output load varies.

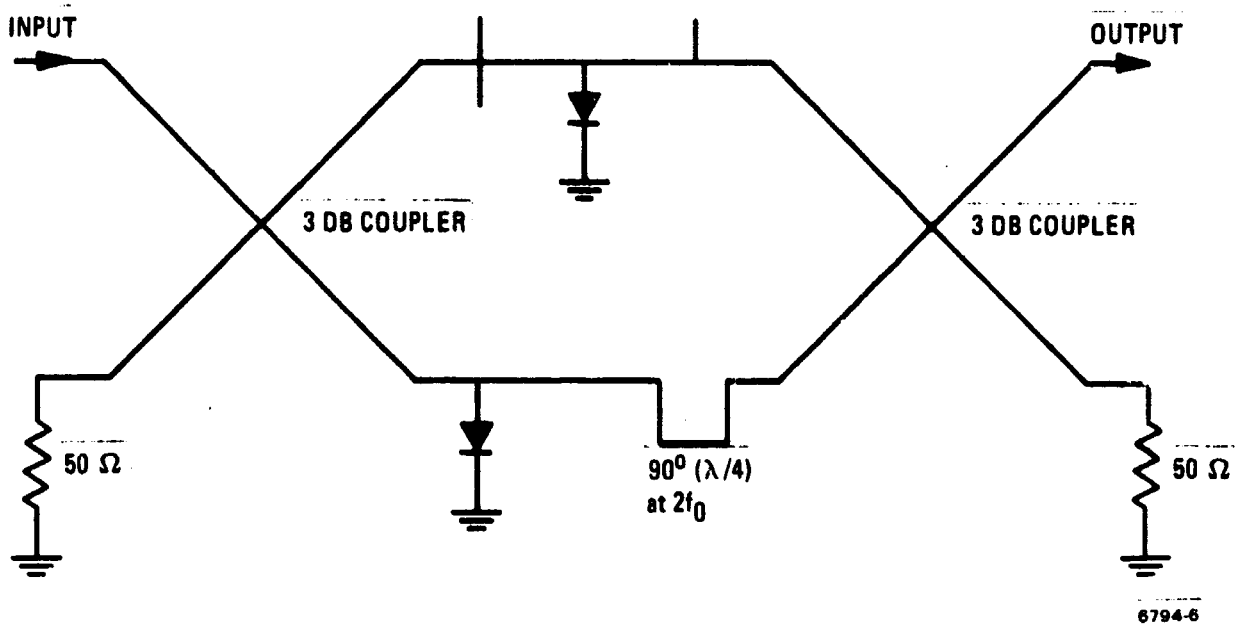


Figure 3-61. Unilateral Stripline Frequency Multiplier

The high frequency, dual device unit, can provide greater than 60% efficiency.

3.4.4.3 Multiplier Construction

Each multiplier requires a self bias and therefore requires a dc blocking device to maintain the bias on the diode. In the past, miniature ceramic chip capacitors were used in this application. During the program a network which performed the dc blocking function was developed.

The multipliers are designed such that the function performed previously by the chip capacitors, are now integrated into the module by use of the .010 glass teflon board. The bias voltage developed by the step recovery diode is isolated by means of capacitors formed by using this network. Figure 3-62 shows a typical multiplier layout. Since it was found that any components which required cutouts in the board material were expensive in terms of production, the module was designed to eliminate all internal lumped components. This was accomplished

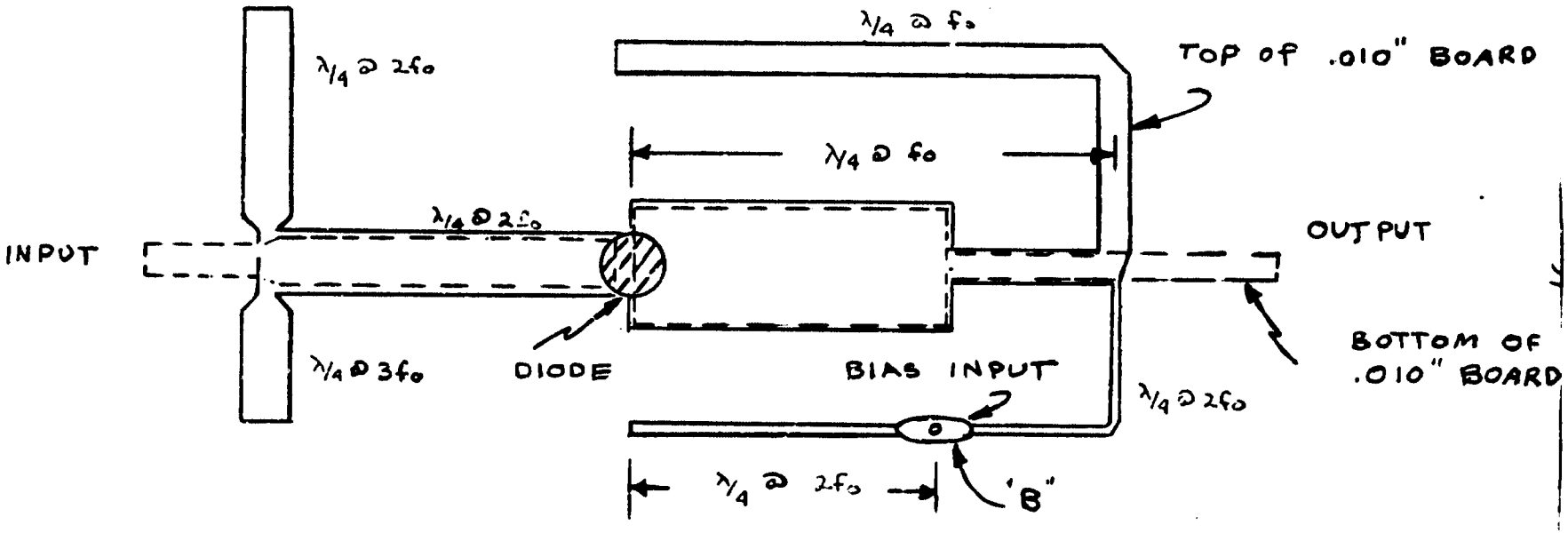


Figure 3-62. Typical X Multiplier Layout

by isolating the dc bias point by means of stripline networks. This is shown as point "B" in figure 3-62.

3.4.4.4 Test Data

Data measured on the low frequency multiplier is listed below:

	P in	P out
Room Temperature	2.6 w	1.68 w
80°C	2.6 w	1.50 w
-30°C	2.6 w	1.45 w
Bandwidth	1125 MHz center	
	1150 MHz down .2 db	
	1100 MHz down .2 db	

Data measured on the high frequency multiplier is listed below:

Single Unit

Pin = 12 w - Pout = 7.9 w

Bandwidth	2250 MHz center
	2300 MHz -.4 db
	2200 MHz -.2 db

Dual Unit

Pin = 24 w - Pout = 15.8 w

Bandwidth	2250 MHz center
	2300 MHz -.5 db
	2200 MHz -.25 db

3.4.5 Power Amplification

New transistors for power amplification at high frequencies began to appear on the market at the beginning of the program. Three were considered for evaluation; they were 2N4976, 2N4431 and the PT6694. These devices are produced by TRW and are designed for stripline integration.

At the very beginning of the program the 2N4976 was evaluated at 2.25 GHz and is rated to give 1 watt at 2.0 GHz and 5.0 db gain. This device proved to perform very poorly at 2.25 GHz and was abandoned.

The 2N4431 specification is 5 w output at 1000 MHz with 5 db gain and greater than 35 percent collector efficiency. This device proved to be useful as the first driver in the power amplifier chain. At 1125 MHz the efficiency was a consistent 45 per cent with lower power gain.

Later in the program the PT6694 was introduced, which is an updated 2N4431. This device provided a consistent 6.5 watts output at 1125 MHz, with greater than 45% collector efficiency and 4.5 to 5 db gain.

Using this as a building block a power amplifier chain was arrived at which would have 26 watts of r-f power at 1125 MHz as outlined in paragraph 3.2.

To improve the implementation of stripline for production and improve its reproducibility, new techniques of construction were initiated and included in the goals of the program.

To provide the output power a technique now finding wide usage in the industry is the distribution and recombining of r-f power by means of 3 db couplers. In stripline form it consists of two coupled lines of one quarter wave length terminated at each port by its characteristic impedance. Such devices also provide isolation of the ports by greater than 20 db. In the past construction has been by means of a mylar spacer sandwiched between two stripline boards with one circuit printed on the upper board and the other on the lower board. This presents a serious problem in the alignment of these boards.

A technique was developed which utilizes a double copper clad stripline material, .01 inch thick, in which couplers can be etched with exacting accuracy and then be sandwiched between the stripline boards, thus relieving the alignment problem.

To take advantage of printing the couplers on this thin material another problem was investigated. This problem was the chip capacitor problem as discussed under the paragraph on multipliers. These networks were incorporated into the power amplifier providing a composite of couplers, networks associated with matching, dc blocking, and a new dc connection network, all investigated and developed on this program.

To provide a low profile stripline package and remove an unreliable part, air trimmer capacitors commonly manufactured by Johanson and JFD, a threaded slug capacitor with a high dielectric material on its end, provided adequate capacitance change for all of the stripline modules that require variable capacitors.

The thermal resistance of the PT6695, as listed by the manufacturer, is 9.7°C/watt. During the course of the program, measurements were made which indicated that the thermal resistance of the device should be 4.8°C/watt. Further study must be undertaken to resolve this area. If the device has a thermal resistance of 9.7°C/watt, six amplifiers may be necessary in the final output to keep the junction temperatures reasonable in any future development.

3.4.5.1 Amplifier Construction

A sketch of a typical amplifier layout is shown in Figure 3-63. The solid lines are the top of the board and the bottom is shown in dashed lines. Reference "A" shows the stripline transformer used to accomplish the impedance match, and to isolate the output from dc. The base is returned through a shorted stub, also functioning as part of the input matching network. Variable capacitors are included, on the input port, to allow for parameter changes of the transistors. Figure 3-64 shows the same basic amplifier, but with the addition of the 3-db hybrids integrated into the circuit. The dc is applied to the collector through a 470 pf feed-through capacitor whose impedance characteristics have been established by slotted line measurement. The impedance thus found, is included as part of the collector match.

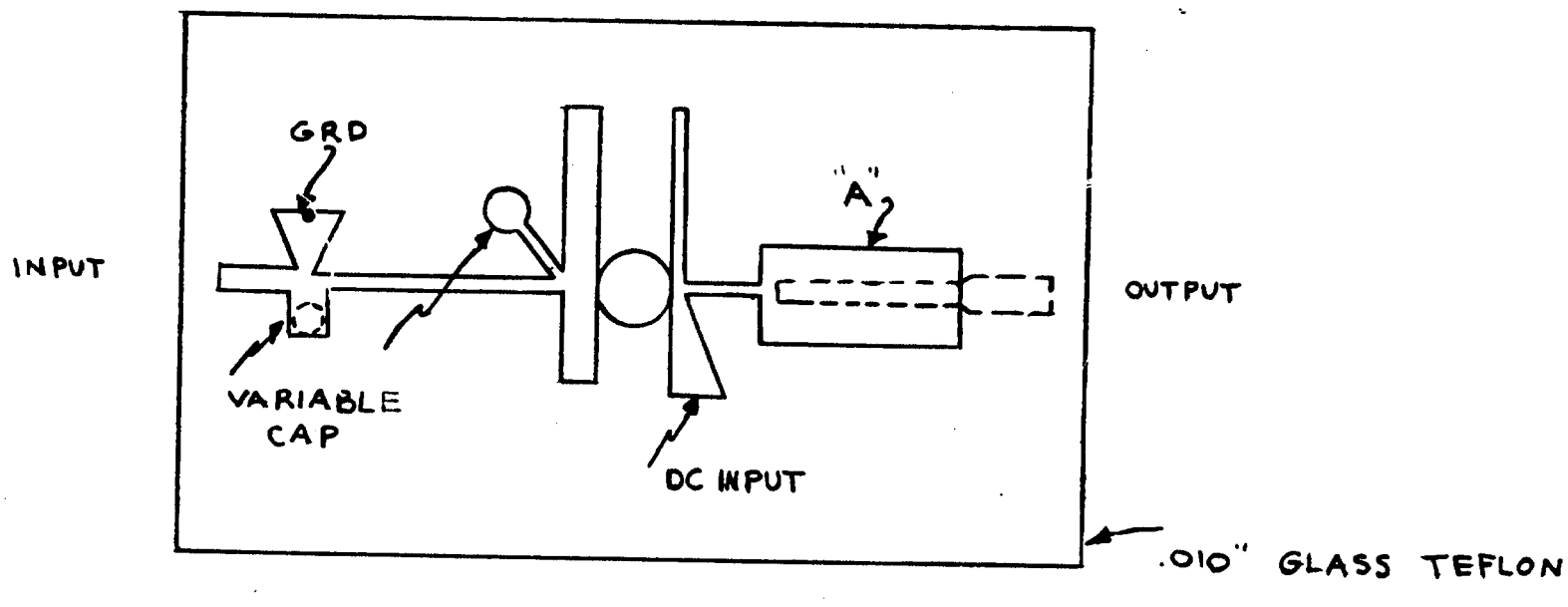


Figure 3-63. Typical Amplifier Layout

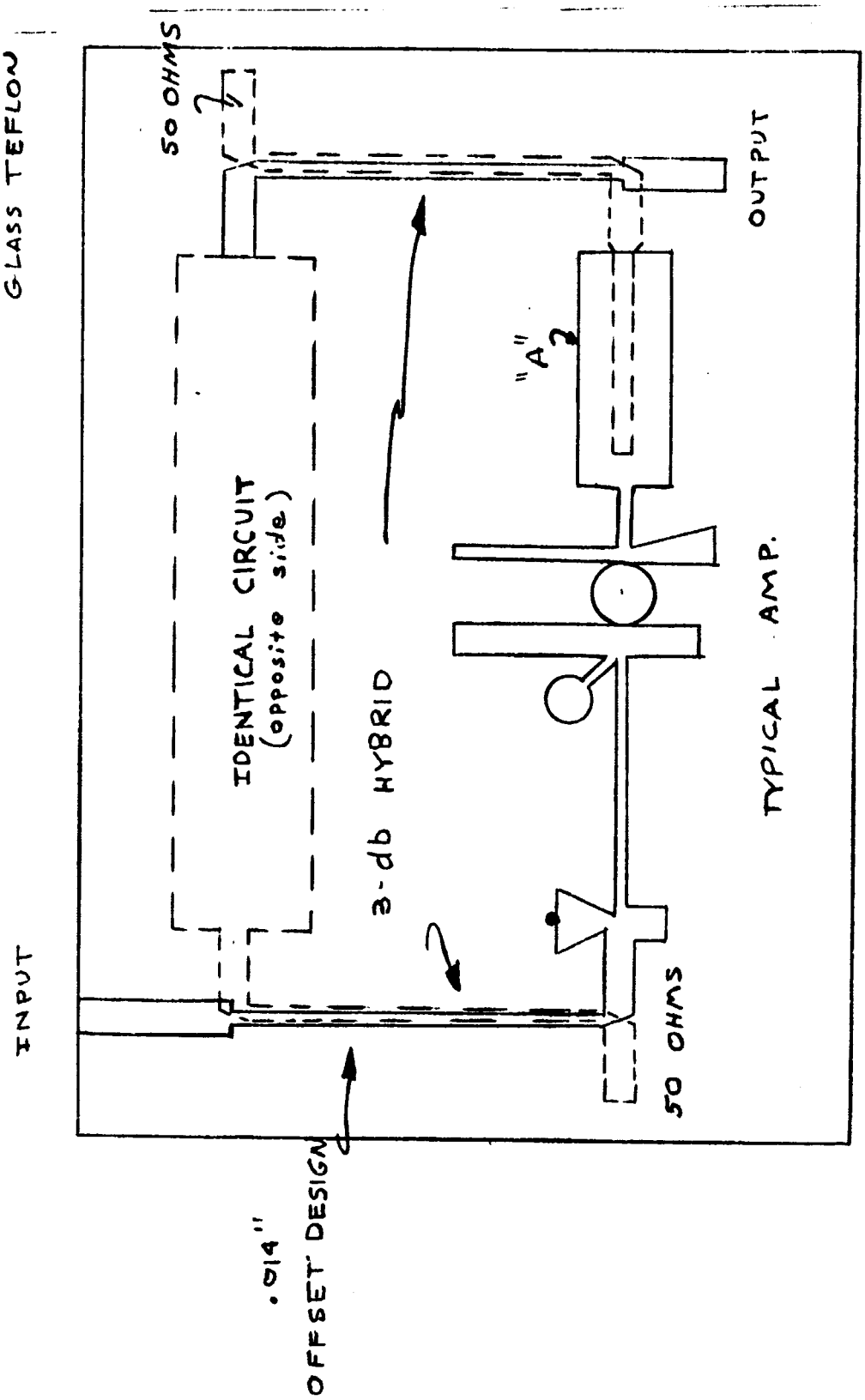


Figure 3-64. Summed Amplifier

3.4.5.2 Amplifier Data

Data measured on a single amplifier:

Pin = w - Pout = 6.2 watts

Collector Efficiency: 45.5%

Bandwidth, 3 db pts: 36 MHz

Dual amplifier measurements:

Pin = 4 w - Pout = 12.5 w

Collector Efficiency: 45.5%

Bandwidth, 3 db pts: 40 MHz

3.4.6 Output Filter

The output bandpass filter developed for this program was designed to relieve problems associated with corona which can occur during critical pressure.

The bandwidth of the filter needed to restrict the spurious sidebands associated with this transmitter could be met with a three pole network having a bandwidth of 1000 MHz, thus minimizing the insertion loss of the filter.

An air dielectric interdigital filter can be constructed in a small size and minimum insertion loss, but its elements will have high vswr and high impedance points which further complicate problems associated with corona.

A filter designed in air stripline which is constructed using shorted quarter-wave stubs and connecting lines can eliminate high impedance points and reduce the elements standing wave ratio.

A computer aided design was employed to calculate the impedances of the elements of the filter. Its basic layout is shown in figure 3-65.

The filter was constructed and found to have less than .2 db loss and an inband vswr of 1.3:1. Improvements in this unit can be made in future construction. The biggest disadvantage of this type of filter is its physical size, being about twice the size of a rod type interdigital filter.

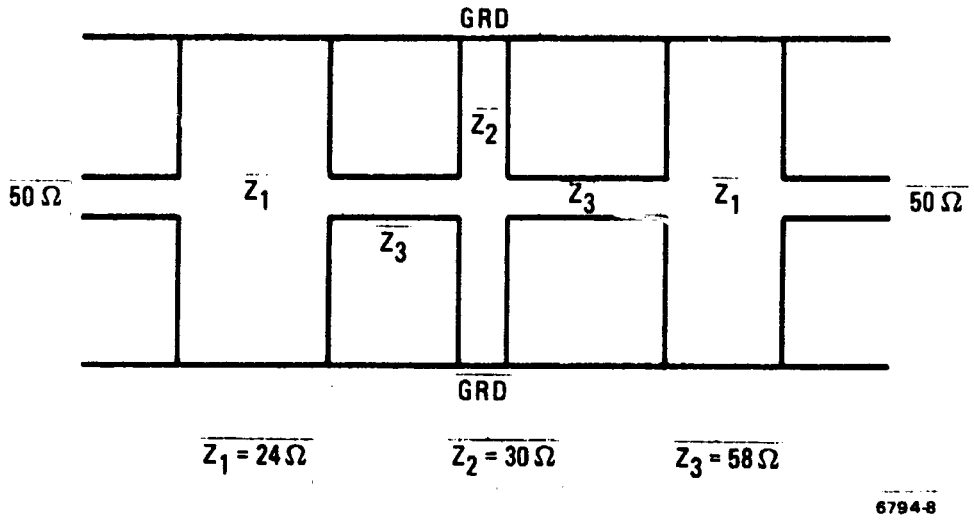


Figure 3-65. Stripline Filter Layout

3.5 PERFORMANCE TESTS

The completed breadboard transmitter was subjected to selected tests to determine its operating characteristics.

The unit was not subjected to any environmental tests as its construction does not lend itself to these tests. Limited module tests were performed and can be found under the appropriate circuit description paragraph.

The transmitter was designed for a center frequency of 2250 MHz which is the center of the telemetry band; however, t' nit is capable of being tuned approximately $\pm$40 MHz. Since the USBE test set was available for taking measurements of distortion and frequency response, the transmitter was tuned to 2287.5 MHz for final testing.

The unit was found to have lower output power than was predicted from the block diagram. The problem was traced to the output multiplier.

The power supplied by the power amplifier was 26 watts at 1125 MHz. With a 60 percent efficient multiplier, the output would be 15.6 watts at 2250 MHz. The measured performance at 2250 MHz was 14 watts r-f output power with 95 watts of consumed dc power. This is a multiplier efficiency of 53.6 percent. The efficiency appeared to be low, not from a phasing problem; but rather from an incompatibility of the multiplier and the power amplifier. When driven from a laboratory signal generator, an efficiency of 67 percent with a single diode and an efficiency of [illegible] percent as a dual diode unit. It is believed that when the interface problem is solved, the multiplier can achieve an efficiency of at least 60 percent (rather than 53.6) driven from the power amplifier.

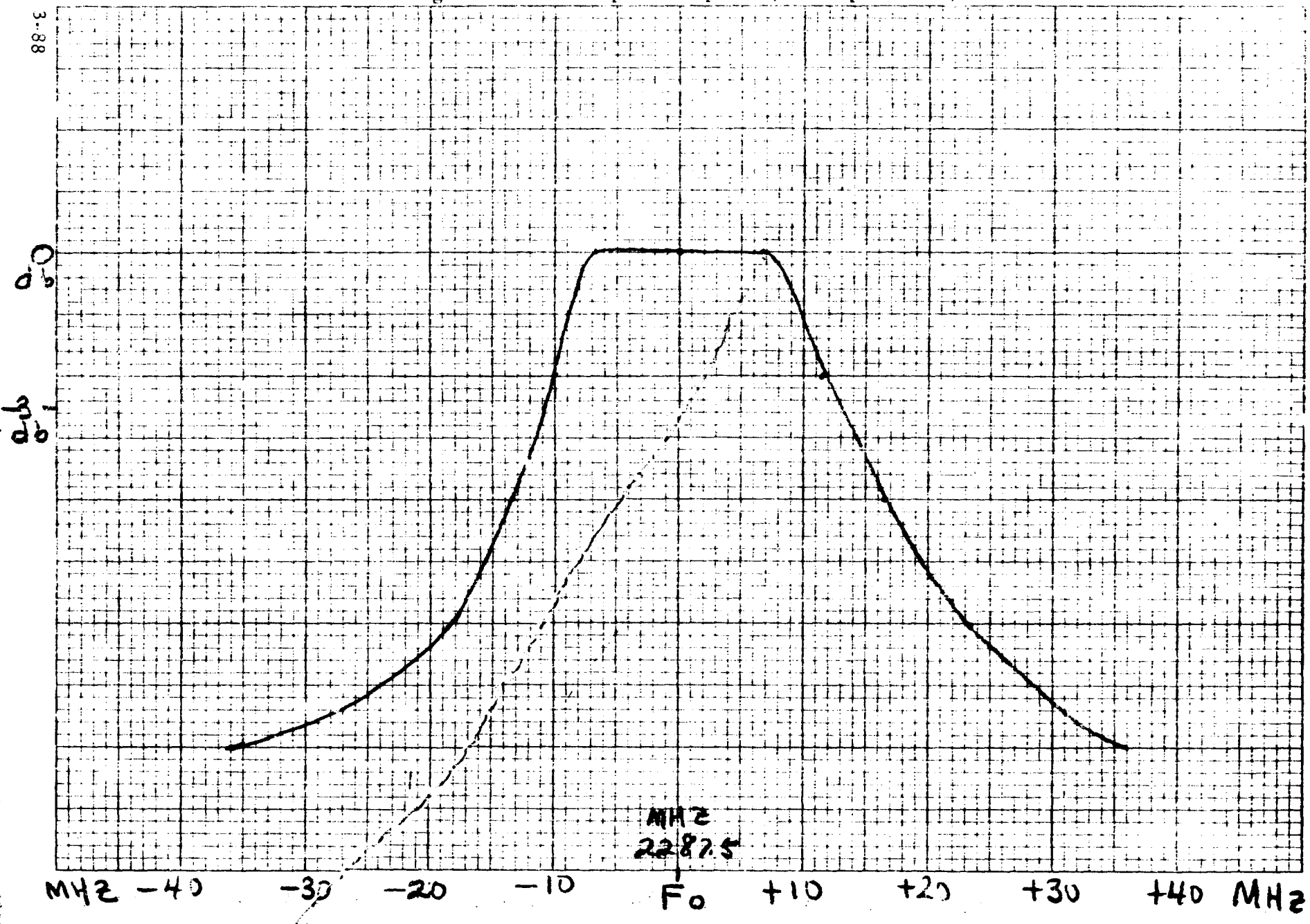
A similar Motorola transmitter, developed on another program and now in production, has such a multiplier. Efficiencies of greater than 60 percent are consistently obtained in the production units. Comparable success in this transmitter could provide an overall efficiency of 16 percent based on the ratio of r-f power output to DC power input, including the effects of losses in the power converter.

The typical .1 db bandwidth of the transmitter is 14 MHz. This is shown in figure 3-66. A large phase change undoubtedly exists at the band edges. The baseband frequency response surely illustrates this point as shown in figure 3-67. A rise in the response occurs at approximately 7 MHz. The bandwidth restriction occurs because of the power amplifier chain bandpass.

Data on harmonic content of the baseband was taken at .7 radians of peak deviation. Figure 3-68 shows that 2nd and 3rd harmonic distortion remains below 2 per cent throughout the frequency covered. The deviation capability of the unit was pressed to 5.5 radians peak deviation before major distortion was evident.

Figure 3-69 shows the transmitter's sensitivity to +28 vdc power supply variations. It appears that good saturation exists from 27 to 29 vdc.

Figure 3-66. Bandpass Response (No Output Filter)



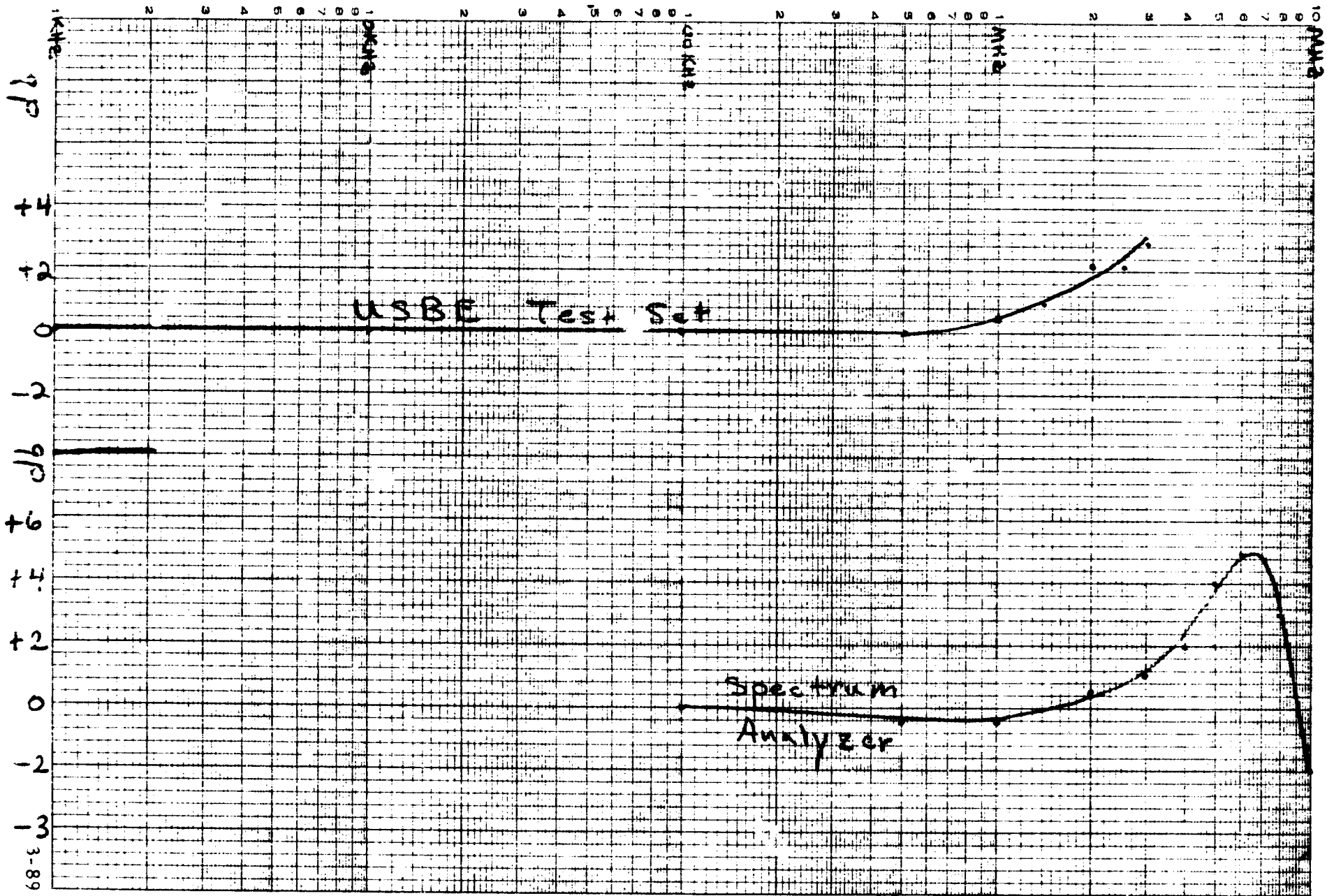


Figure 3-67. Baseband Frequency Response (.7 Radians Peak Deviation)

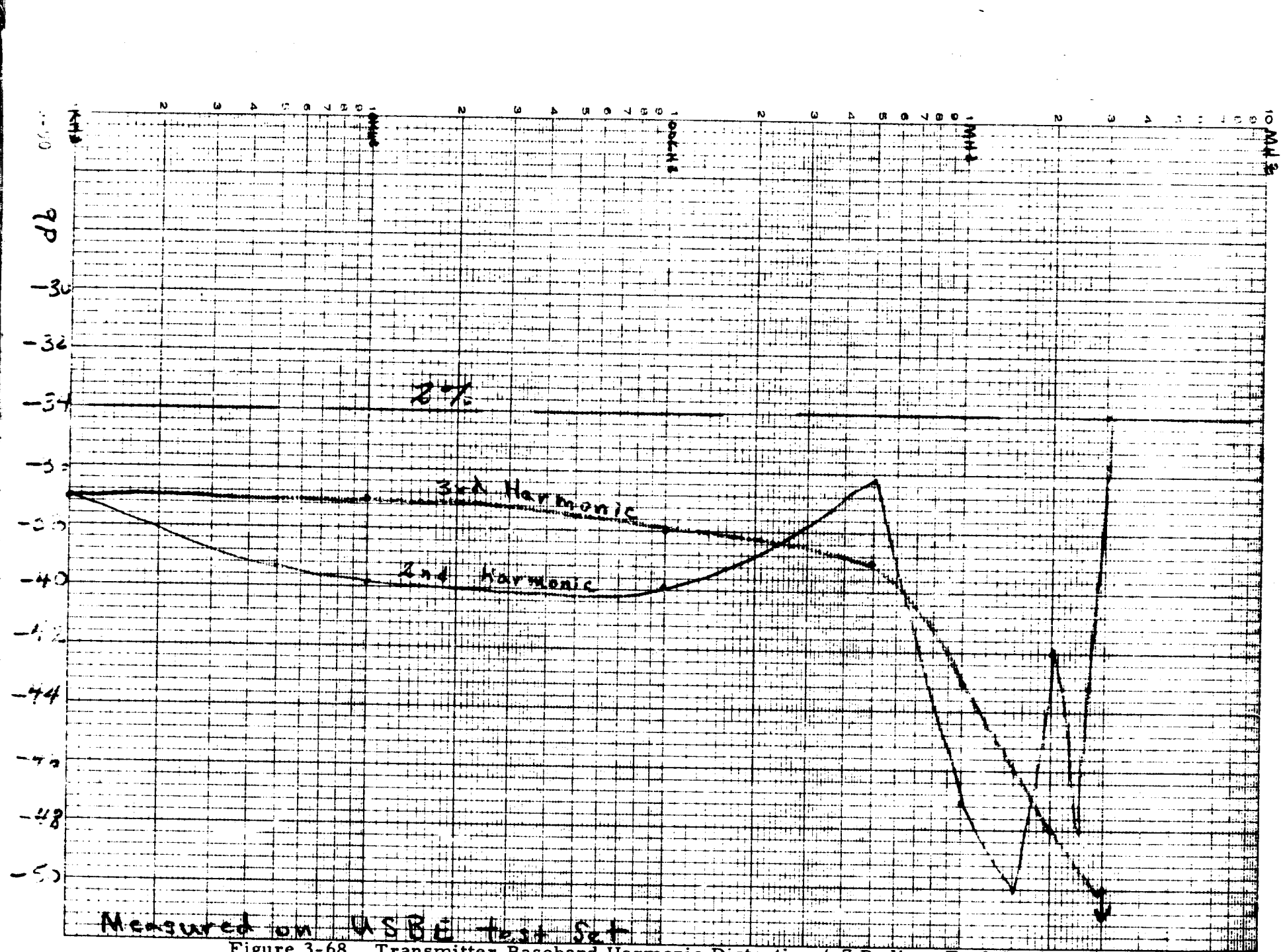


Figure 3-68. Transmitter Baseband Harmonic Distortion (.7 Radians Peak Deviation)

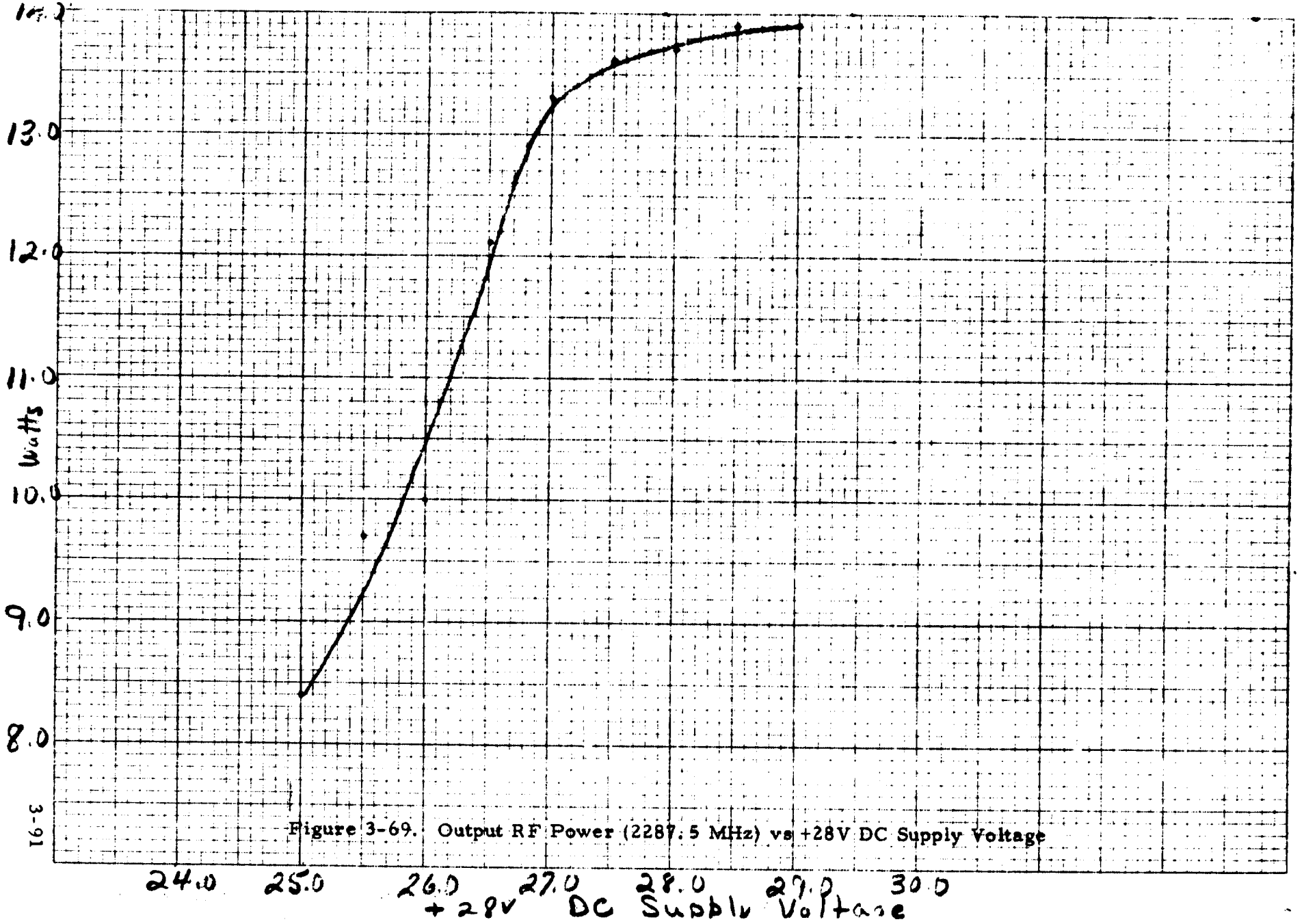


Figure 3-69. Output RF Power (2287.5 MHz) vs +28V DC Supply Voltage

Data taken at 2287.5 MHz is summarized below:

R-f power out	13.7 watts
Dc power	28 v, 3.815A = 106.82 6 v, 15 ma = .09
	Total = 106.91 watts

Data taken at 2250 MHz is summarized below:

R-f power out	14.0 watts
Dc power	28 v, 3.4A = 95.20 watts 6 v, 15 ma = .09 watts
	Total 95.29 watts
Bandwidth	23 MHz, 3 db

Power in vs power out:

Pin dbm	Pout watts
+3.0	14
0	13.7
-3.0	12.5

Spurious sidebands: (no output filter)

Major Signals

3431.25 MHz -28 db

1143.75 MHz -29 db

560 MHz >-50 db

Distortion: See figure 3-68

Deviation: Designed for 2.8 radians peak

Major distortion occurs at 5.5 radians peak

Sensitivity - .875 radians per vrms

Frequency response: See figure 3-68

SECTION IV
ANALYSES

4. INTRODUCTION

The analysis problems which have been considered fall into two broad areas. First, recommendations for future systems in terms of the phase lock loop and the modulation techniques to give improved performance, and second, changes to the existing Apollo USB system which could be made to give improved performance with minimum change to the current equipment. Although many other problems and questions can be posed along these lines of consideration, the analyses were constrained by the available time and resources.

4.1 PHASE-LOCK LOOP ANALYSIS

The phase lock loop (PLL) receiver, at this point in time, appears to be a necessary part of any space communications system because of the need to extract a radio carrier of varying frequency for purposes of homodyne detection and doppler measurements. Since the PLL is inherently mathematically a non-linear device, analyses tend to be extremely difficult and in many cases are suspect. The past experience with PLL's has been very cautious because of lack of confidence in the technology and in analytical designs. More modern computer techniques have, to a great extent, overcome some of the past difficulties. In addition to the analysis, more practical experience has been gained in the use of PLL, most of which tend to substantiate the analysis recommendations.

The model used for the phase lock loop is described in paragraph 4.1.5.

Open loop bode plots and root locus plots obtained during analysis of the type III loop are presented in paragraph 4.1.6

Paragraph 4.1.7 contains a Bibliography of terms and techniques used in the analysis.

In the Apollo Unified S-Band Transponder, a phase lock loop was used to filter the S-band carrier. This filtered carrier was used to detect the up-link modulation by multiplying the S-band modulated signal with the filtered carrier in a product detector. The filtered carrier output was also used to derive the down-link carrier to provide a transmitted carrier phase coherent with the received carrier. For this type of operation the important characteristics are acquisition, speed and phase errors, due to noise and dynamics. For small noise phase errors one criteria is to narrow the loop bandwidth. This, however, leads to high dynamic errors as well as longer acquisition times. One method of overcoming this problem is to employ a second or third order loop. Both of these loops become practical if self-acquistion is used instead of the method used now where the received signal frequency is swept past the natural frequency of the receiver. A further possibility of reducing phase errors due to noise is to use an AGC system instead of hard limiting after the predetection filter.

This analysis was limited to the following possible areas for loop operation improvement:

1. Non-limiting loop operation.
2. Higher order loops.
3. Self acquisition.

4.1.1 Predetection Limiting vs Nonlimiting

In the Apollo carrier phase lock loop mechanization, predetection limiting is used to limit the peak signal level applied to the phase detector. This nonlinear operation using perfect limiters degrades the signal to noise ratio by 1.06 db. If linear operation can be used, the possibility exists of effectively gaining 1 db better sensitivity at usable signal levels. Since practical limiters generally convert some of the a-m noise into phase noise, the degradation can be worse than 1 db. The amount of additional degradation can be held to a minimum by careful design of the limiter. A well designed limiter typically has less than one degree phase shift per db in limiting. This additional noise is spread over the predetection bandwidth

and has only a minor effect on loop threshold. For this reason this effect will not be considered further in this study. For a Type I loop using no DC amplification, limiting is necessary if highest possible phase gain is desired in the loop. As an example, in the Apollo phase lock loop the predetection bandwidth to loop threshold bandwidth ratio is 20/1. Thus at unity signal to noise ratio in the loop bandwidth, the predetection S/N ratio is -13 db. If no limiter is used, the peak design phase detector gain would have to be 20 db above the threshold detector gain. By using a limiter, the peak design gain to threshold operating gain is determined by $1/\alpha_o$ wherefore

$$\alpha_o = \frac{1}{\sqrt{1 + \frac{4}{\pi} \frac{BW_{IF}}{2B_{Lo}}}}$$

the 20/1 bandwidth ratio, $1/\alpha_o = 5.14$ or 14.2 db. Thus limiting in this case allows the loop to be mechanized with 6 db more gain over a linear type of operation. By removing the restriction against use of dc amplification, the 6 db gain advantage of the limited loop disappears so that choice of using limiting or linear amplifiers can be made on other criteria. A byproduct of the predetection limiting is the increase in loop gain with increase in signal to noise ratio. This increase in gain increases the loop bandwidth as well as decreases the dynamic errors with increasing signal level. For near earth orbits this "adaption" of the loop is desirable since the velocity and rate dynamics are highest at close range. For linear operation a similar type of loop adaption can be obtained by employing envelope AGC to maintain the rms signal plus noise constant. For this type of operation, the signal suppression factor becomes:

$$\alpha_{agc} = \frac{1}{\sqrt{1 + \frac{N}{S}}}$$

If we equalize the gain at loop threshold by lowering the phase detector gain of the AGC loop, then at strong signal, the α of the AGC loop would be less than the limited loop by the amount of the attenuation used to equalize the gains. For the 20/1 bandwidth ratio this would amount to a maximum α_{agc} of 0.89. For large predetection

to loop bandwidth ratios the limit would be $(\pi/4)^{1/2}$. The major effect of this would be 10% less strong signal bandwidth and 10% greater dynamic errors. By using Type II or Type III loops, this net effect on the dynamic errors can be made insignificant.

An additional non-linear element in the phase lock loop is the phase detector. The output of this detector is equal to the sine of the signal angle relative to the reference. In order to determine the effect of this non-linearity upon the performance of the loop a computer simulation of the loop was utilized. By using identical noise sequences, a comparison of the rms output phase noise versus input signal to noise ratio in a bandwidth equal to the noise bandwidth of the loop was computed. The results are shown in figure 4-1. As expected, the difference in output signal to noise ratio between loops using a limiter and one without a limiter is approximately 1.1 db in the region where the limiter is operating with a negative signal to noise ratio. One surprise, however, was in the performance of the loop without a limiter. The output phase noise compared to the input phase noise shows a slight improvement in the signal to noise ratio range between 2 and 8 db. The maximum improvement of approximately 0.5 db occurs in the input signal-to-noise ratio range of 4 to 6 db. This improvement is due to the non-linearity of the phase detector. The loop tends to lose lock on the input signal plus noise for the duration of the extreme noise peaks. This, in effect, clips the noise peaks off of the signal. At lower signal to noise ratios, loss of lock in the loop occurs with such frequency and duration that the signal to noise ratio is degraded over the input signal to noise ratio. The noise used in this analysis was simulated by using two normally distributed random variables with one of the variables in-phase and one in-quadrature with the signal. This noise simulates the actual noise on the input signal and is not the same as white phase noise assumed by some investigators where unity signal to noise is assumed as an angle variance of one radian.

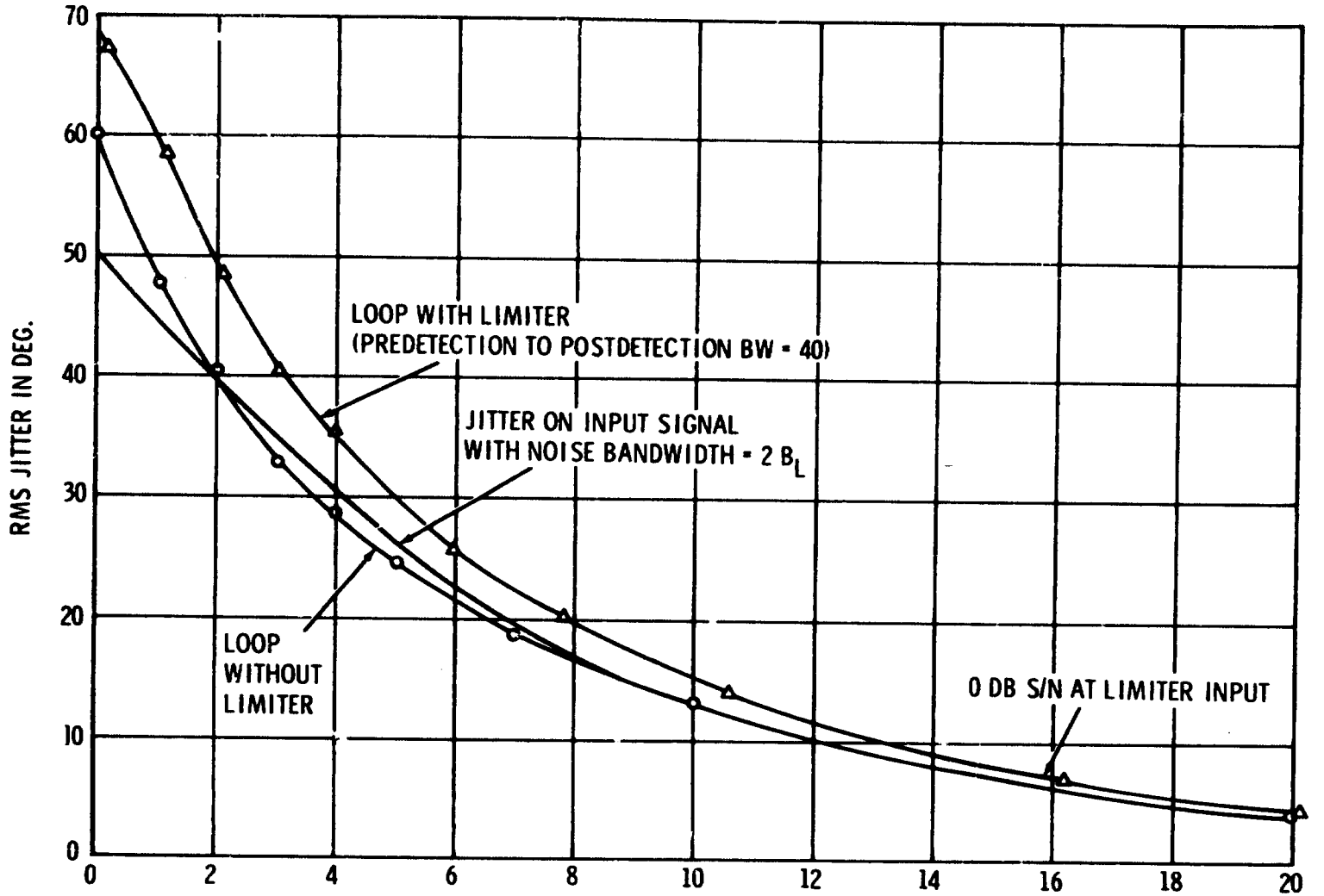


Figure 4-1. DB SIGNAL TO NOISE RATIO IN AN R-F BANDWIDTH EQUAL TO NOISE BANDWIDTH OF LOOP (2 B_L)

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4.1.2 Higher Order Loops

The present spacecraft Apollo carrier loop is a high gain Type I loop. This type of loop has a velocity error when the signal frequency is different than the natural rest frequency of the vco. With doppler rate dynamics the loop will have a rate error in addition to the velocity error. The total error in degrees of a Rechtin optimized loop is given by

$$\epsilon = \frac{360 \times f}{K_v} + \frac{101.25\ \dot{f}}{(\alpha/\alpha_o)\ B_{L_o}^{\ 2}}$$

where: B_{L_o} is one sided loop noise bandwidth at optimization.

f is frequency error in Hz.

$\dot{f}$ is frequency rate in Hz/sec.

ϵ is loop error in degrees.

α_o is signal suppression factor of loop at optimiazation.

α is operating point signal suppression.

This equation assumes a linear phase detector and is thus only approximately correct for large phase error of loops using a sine type phase detector. Excessive phase error in the loop degrades the performance of the loop at low signal to noise ratios by increasing the probability of the loop losing lock. At 5 db S/N, 0.1 radian degrades the loop by 0.1 db while 0.2 radian will degrade the loop by 0.7 db. A second effect of phase error is to reduce the demodulated signal level by a factor equal to cos (ϵ). Thus since the demodulated noise level does not change, the output signal to noise ratio is degraded.

By using a Type II loop where $K_v = \infty$, the velocity error is reduced to zero. In practice, without using mechanical resolvers, it is difficult to mechanize a true Type II loop. By using an operational amplifier with high gain to produce an active time constant it is possible to obtain a K_v in the order of 10^{11}. For all practical purposes, this gain is close enough to infinity so that the loop performs in a manner similar to a true Type II. Several operational advantages in addition to the elimination of velocity errors are derived by using the integrating amplifier. One of

these advantages is to reduce the operating level of the phase detector. In the Type I loop with no dc gain the phase detector is operated at the highest level consistent with the diode voltage ratings to obtain as high a K_v as possible in the loop. This high operating level requires high power drivers and presents shielding problems as far as coherent signal leakage is concerned. Using the active time constant, the phase detector can be operated at the lowest level consistent with diode balance offset voltage and operational amplifier voltage and current offsets. A second advantage is the frequency memory of the loop. If the loop should lose lock due to momentary loss of signal, the large active time constant will keep the frequency of the loop at the value it had when it lost lock. This allows the loop to regain lock without initiating frequency search if the signal returns within a short period of time.

In substituting a Type II for a Type I loop, a change in acquisition procedure must be made. Acquisition of this type of loop is practically impossible if attempted by sweeping the input signal frequency as is done in the present Apollo System. Self acquisition is quite practical and if used properly, a reduction in the acquisition time can be achieved. Acquisition will be discussed in more detail in the next section of this report.

A further reduction in the dynamic errors can be made by utilizing a Type III loop. As contrasted with the Type II loop, there is not a generally accepted optimized configuration. Three general configurations are discussed in the literature. These are referred to as:

1. Weiner
2. Mallincrodt
3. Pool

Each of these configurations has slightly different characteristics. The Weiner loop was designed to have minimum mean square error to a frequency ramp. The Mallincrodt loop has the maximum phase margin while the Pool loop is a practical implementation of the Weiner loop using real zeros instead of the complex zeros required in the Weiner loop filter. Since maximum phase error is a criteria of

loop operation when considering minimum acquisition time or minimum probability of unlock in the presence of noise, a Type III loop design was optimized to yield minimum peak error for a frequency ramp. The resulting loop filter for this optimization, like the Weiner loop, contained complex zeros. A second optiminzation restricting the loop filter zeros to the real axis yielded a fifth Type III loop with certain advantages over the original three varieties. As a means of comparing the various loops, the following definitions apply.

1. Loop Transfer function:

$$H(s) = \frac{B_o + B_1 S + B_2 S^2}{A_o + A_1 S + A_2 S^2 + A_3 S^3}$$

$$= \frac{G\left((S + d)^2 + \lambda^2\right)}{(S + c)\left((S + \sigma)^2 + \omega^2\right)}.$$

2. Loop Filter:

$$F(s) = \frac{G\left((S + d)^2 + \lambda^2\right)}{S^2}$$

3. Transient Behavior (considering phase detector to be linear)

   T = Time to peak error for a frequency ramp input

   $V_{in} = \frac{1}{S^3}$ to a loop with a B_{L_o} = 1.0 Hz.

   ϵ = Peak phase error in radians for a frequency ramp input of 1 rad/sec^2 for loop with a B_{L_o} = 1.0 Hz.

   B_{L_o} = One sided noise bandwidth of loop in Hz.

4. Stability

   GM = Gain Margin in db

   PM = Phase Margin in Deg.

The Type III loop comparisons are given in table 4-1.

Table 4-1. Comparison Between Various Types of Type III Loops

	Weiner	Mallincrodt	Pool	Min Peak	Approx. Min. Peak (real zeros)
B_o in rad	1.72800	0.60949958	1.245339	1.2066443	1.0543378
B_1 in rad	2.8800	2.7171496	3.273935	3.1436057	3.2556585
B_2 in rad	2.400	3.0282637	2.151754	2.5462450	2.5132628
A_o in rad	1.72800	0.60949958	1.245339	1.2066443	1.0543378
A_1 in rad	2.8800	2.7171496	3.273935	3.1436057	3.2556585
A_2 in rad	2.400	3.0282637	2.151754	2.5462450	2.5132628
A_3 in rad	1.000	1.0000	1.0000	1.0000	1.00000
G in rad	2.400	3.0282637	2.151754	2.5462450	2.5132628
d in rad	0.6000	0.4489337	0.7607598	0.6173023	0.6476537
λ in rad	0.6000	0.0	0.0	0.30467942	0.0
C in rad	1.2000	0.33670031	0.5114270	0.61829684	0.45442006
σ in rad	0.6000	1.3462362	0.8201633	0.9639741	1.0293391
W in rad	1.0392305	0.0	1.327539	1.0110962	1.1225812
T in sec	1.7123577	2.3139169	1.69366	1.7963144	1.8047117
ϵ in rad	0.28087018	0.3047343	0.2862066	0.2746985	0.27484593
B_{L_o} in Hz	1.0	1.0	1.0	1.0	1.0
GM in db	12.07	22.52	15.06	16.44	17.81
PM in deg	60.45	73.47	54.3	63.47	62.61
Loop Filt Gain	1.72800	0.609499	1.24533905	1.2066443	1.0543378

In comparing the loops, it is apparent that the Weiner and Min-Peak loops require complex zeros in the loop filter. These two loops do not offer enough significant advantages over the other three loops to warrant their use due to the added complexity required to provide the complex zeros. Comparing the other three loops, the only advantage that the Mallincrodt loop has is greater phase and gain margin. The higher peak phase error plus the larger time that the loop remains at maximum error is a definite disadvantage when it comes to threshold performance in the presence of dynamic transient errors. This leaves the tradeoff to be made between the Pool loop and the approximate minimum peak loop. No real significant difference exists in the transient behavior. The Pool loop may have slightly higher phase error, but does not stay at the maximum error as long as the minimum peak loop. The major difference between the loops is in the gain and phase margin. The higher gain and phase margin of the approximate minimum peak loop makes it the most desirable of the two loops for this application.

In using the transient data provided in table 4-1 for determining time and phase error for other than a B_{L_o} of 1.0 Hz and a frequency ramp of 1.0 rad/sec^2, the time to peak (T) varies inversely as the bandwidth while the peak error (ϵ) varies inversely as the square of the bandwidth and directly as the magnitude of the ramp for linear phase detectors. If a sine phase detector is used, significant errors in the magnitude and time to peak will result in using the table modified as above. For sine type phase detector with the approximate minimum peak loop the transient behavior is given in table 4-2.

From table 4-2 it may be seen that the sine detector has little effect on the transient behavior for a ramp of 1.0 rad/sec^2. The effect of the nonlinearity is quite apparent at 4.0 rad/sec^2. This is the maximum tolerance ramp that the loop will handle without losing lock.

Table 4-2. Transient Behavior of Approximate Minimum Peak Loop with Frequency Ramp Input

	Frequency Ramp in rad/sec^2		
	1.0	3.5	4.0 (max value)
T in sec	1.80	2.10	2.55
ϵ in rad	0.2782	1.2226	1.7291

A large concern in using a Type III loop is stability since these loops are only conditionally stable (a gain above a minimum amount is necessary for stability). This problem is not as severe as it might at first seem. In the normal mechanization of the loop, the loop gain changes with signal level, with minimum gain occurring at minimum signal level. Since the loop becomes more stable with increased gain, optimizing the loop at threshold signal level will ensure that adequate gain exists to keep the loop stable. In using a sine phase detector, a possibility exists of having a steady phase error sufficient to reduce the detector gain to the instability point. For the approximate minimum peak loop with the gain margin of 17.8 db, the required phase error would be in excess of 82.6°. This error is equal to 0.99 of the peak phase detector output. At minimum signal level where the lowest amount of gain margin exists, enough noise error would be present to prevent the loop from locking in any case. Above threshold levels, the gain margin increases due to increased signal level. For instability a phase error approaching 90° would be required. For other reasons, such as threshold bandwidth, the nominal gain of the phase detector and vco are held to close tolerances usually within 10% or 1 db. Thus, no problem exists due to nominal gain variations. The last stability question is loop operation under transient conditions that produce phase errors traversing the "unstable" phase error region. By observing the transient response, using the sine type phase detector, it is seen that the loop behaves in a normal manner with the only effect being (1) longer time to maximum peak error, and (2) a larger peak error than that calculated by using a linear de-

tector. The transient for a 4.0 rad/sec^2 ramp is shown in figure 4-2. Thus it is seen that by using reasonable care in setting up the loop only some abnormal failure in the circuitry would allow the loop to become unstable.

Another consideration of a Type III loop is the acquisition problem. It was determined that the loop could be acquired by sweeping the vco using an error voltage input to the second integrator to derive the sweep provided no offset errors exist at the first integrator. Acquisition with offset errors can be done by acquiring as a Type II loop. This is discussed in more detail in paragraph 4.1.3

The mechanization of either the Type II or Type III loop utilizes operational amplifiers to approximate the required integrators. Figure 4-3 indicates the type of filters used for the Type II or Type III loop. For the third order loops having real zeros it is seen that

$$B_o = \left(\frac{1}{R_1 C}\right)^2$$

$$B_1 = \frac{2\,R_2}{R_1^{\,2} C}$$

$$B_2 = \left(\frac{R_2}{R_1}\right)^2$$

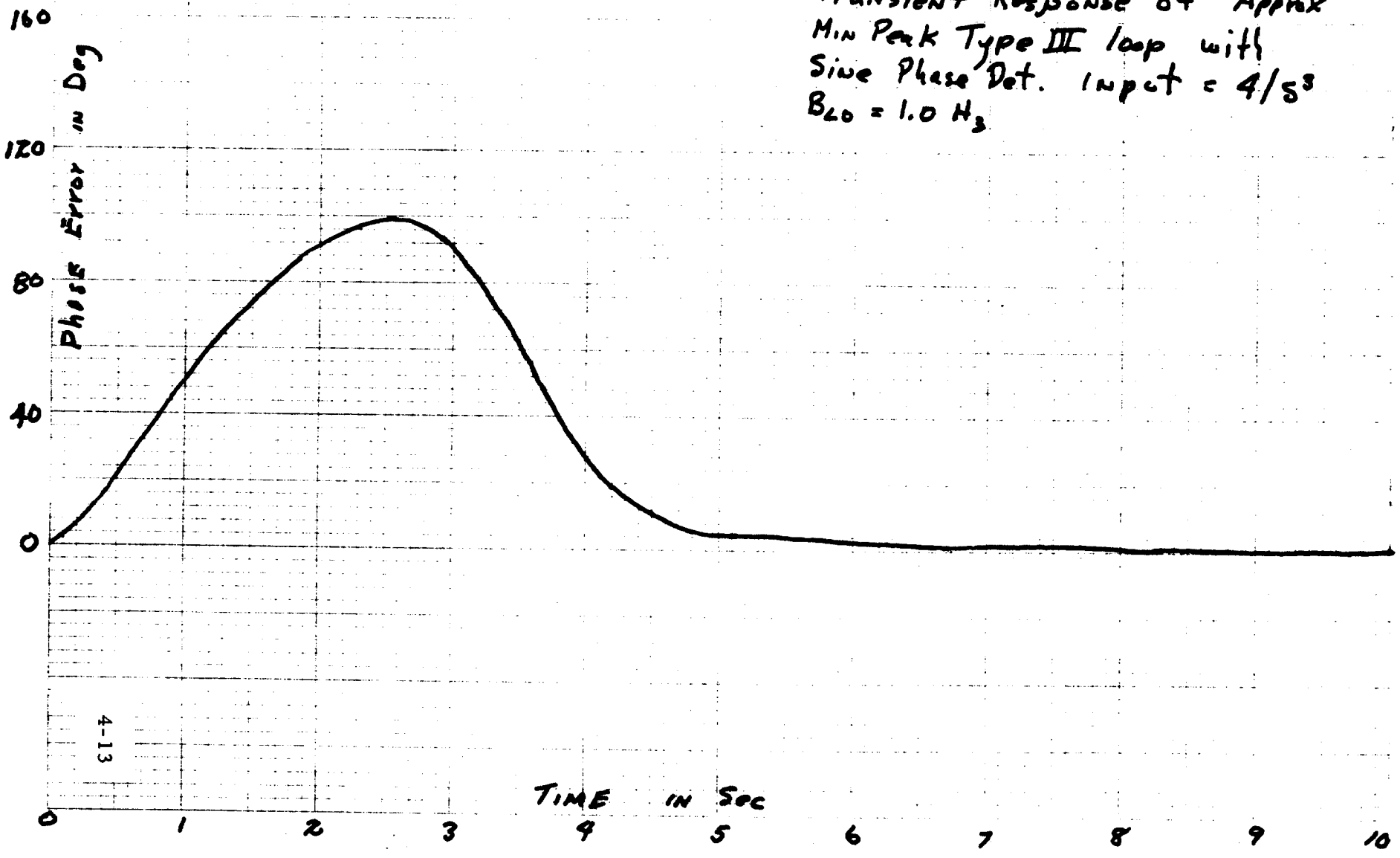
With a certain amount of switching it would be easy to change loop types by shorting out the first integrator capacitor with a resistor as well as changing the value of the resistance in the second integrator.

4.1.3 Acquisition

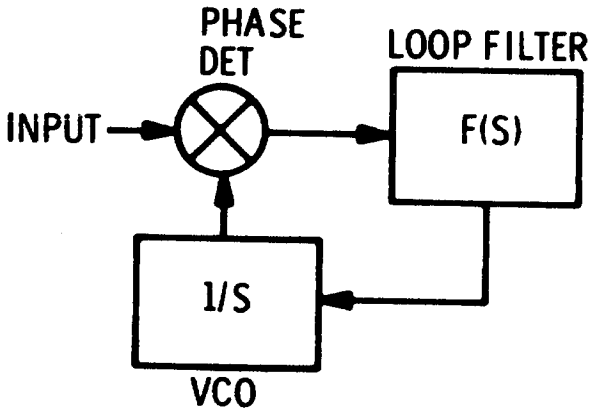
The acquisition procedure for the present Apollo S-band carrier loop requires that the ground transmitter frequency be offset and swept in a triangular sweep so that at the transponder, the received signal frequency will sweep past the receiver frequency and thus allow the loop to lock. After locking to the received signal, the sweep is maintained until the ground receiver acquires the sweeping transponder transmitted signal. For speed of acquisition, high sweep rates are used

Figure 4-2.

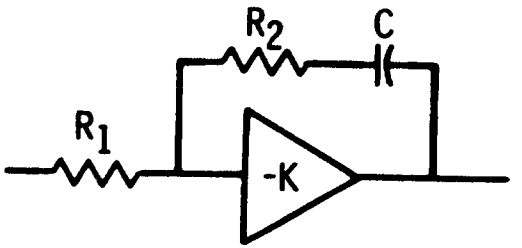
Transient Response of Approx Min Peak Type III loop with Sine Phase Det. Input = $4/S^3$
$B_{LO} = 1.0\ H_3$



4-3A PHASE LOCK LOOP BLOCK DIAGRAM

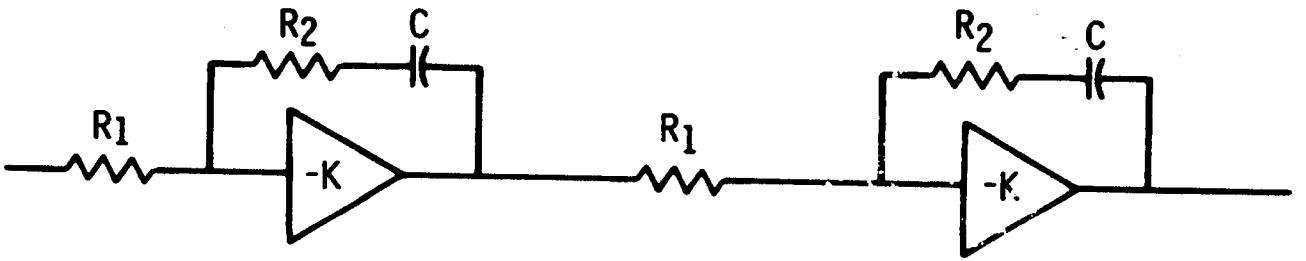


4-3B SECOND ORDER APPROX LOOP FILTER



$$F(S) \approx -\frac{R_2}{R_1}\left[\frac{S+\frac{1}{R_2C}}{S}\right]$$

4-3C THIRD ORDER APPROX LOOP FILTER



$$F(S) \approx \left(\frac{R_2}{R_1}\right)^2\left[\frac{S^2+\frac{2}{R_2C}\,S+\left(\frac{1}{R_2C}\right)^2}{S^2}\right]$$

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(35 kHz/sec). This acquisition requires that the loop has to track the sweeping signal. Thus the loop must be designed to operate with the high dynamics of the acquisition signal. The rate dynamics of acquisition is approximately 10 times the normal orbital dynamics. From the formula for phase error, for equivalent errors due to rate dynamics, the bandwidth of the loop must be over three times wider to track the acquisition dynamics as required to track the orbital dynamics. Using self acquisition it is possible to greatly reduce the acquisition time, or loop bandwidth, or both. To accomplish self acquisition, some means is provided to sweep the local oscillator past the signal frequency. In one method, a detection circuit is used to determine when the incoming signal is equal to the local oscillator and stop the sweep allowing the loop to lock. The most common method of acquisition utilizes an error voltage inserted in the input of the integrator or loop filter preceding the vco causing the vco to sweep in a linear frequency ramp until the loop locks to an incoming signal. The locked loop develops error voltage at the phase detector to cancel out the sweep input signal. In Type I or Type II loop, this offset voltage at the phase detector makes the loop more prone to unlock in the presence of noise than if it is operated with no offset voltage. The probability of unlock is directly related to the probability of noise plus offset voltage exceeding $\pi/2$ radians of error. The longer the loop remains operating with an offset phase noise, the greater the probability $\pi/2$ radians will be exceeded. The maximum acquisition rate allowable for probability of lock is directly related to the amount of S/N ratio in the loop as well as the time it takes to recognize lock and remove sweep voltage. This latter fact has not been treated well in the literature but has been verified experimentally in the lab. In a Type I loop, acquisition speed is also affected by loop gain and maximum frequency offset that the signal has from the natural rest frequency of the vco. This is due to the additional error in the loop due to frequency offset. The general method of detecting lock is to use the output of the loop coherent amplitude detector. The bandwidth of this detector output is set to provide just the necessary probability of detecting lock with the minimum signal level to be encountered. This avoids undue delay in detecting this signal and removing the sweep voltage.

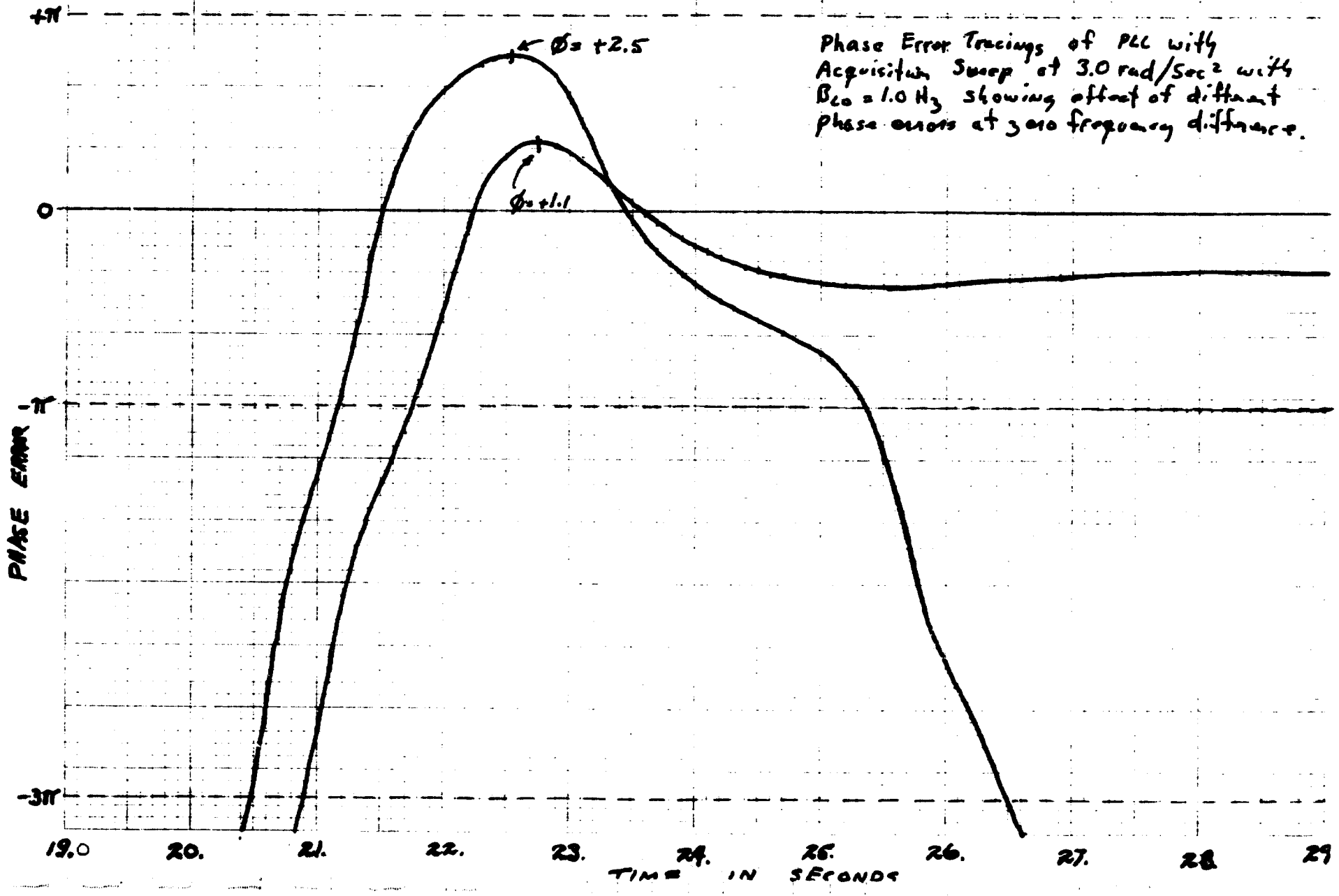
For fastest acquisition a Type II loop should be used. The Type I loop acquisition speed is degraded by frequency offset error. The Type III loop acquisition is not practical due to offset errors at the input to the loop filter. This also was an early objection to Type II loops since it was felt that any offset error at the input to the integrator would cause the integrator to charge up to maximum voltage and push the vco out of range of the signal. This type of problem in the Type II loop is avoided by using the integrator to generate the sweep waveform. This is accomplished by injecting a voltage into the integrator. A voltage level detector on the output of the integrator is used to limit the maximum output voltage level. This detector senses this maximum level and reverses the polarity of the input sweep voltage. Thus the output voltage sweeps back and forth between two preset levels. By using a higher input voltage for the retrace than for the sweep, a sawtooth waveform is generated. The normal unbalance and operational amplifier offsets must be kept much smaller than the sweep voltage input. Since these offsets could add or subtract from the sweep input, the sweep voltage must be set so that the maximum offset added to the applied sweep does not exceed the maximum sweep rate. A valid objection in the past against Type II loops has been the excessive amplifier offset voltage errors. Since they were random in nature they could not be compensated out so that acquisition and loop behavior was seriously affected. The stability of present day operational amplifiers plus use of self acquisition has eliminated the need to employ a Type I loop for space applications.

As an indication of reacquisition behavior of higher order loops, the relative acquisition speed between the Type II loop and the Type III loop was calculated. This was determined by computing the maximum sweep rate in the presence of no noise, assuming no offset errors. For the Type II loop, it might be surmised by looking at its phase plane plot that the maximum sweep speed would be a function of the relative phase between the signal and vco at the instant of zero frequency error. By analyzing the loop by state variable techniques, this was indeed found to be true. Figure 4-4 shows two typical phase error trackings of a Type II loop having acquisition sweep applied to the vco. The sweep having a phase error of 1.1 radian at

zero frequency error allowed the loop to lock and track out the sweep voltage. The sweep with 2.5 radians of error had too large a transient error to allow lock. Figure 4-5 indicates the region of acquisition as a function of phase error and sweep rate. It is interesting to compare this chart with one "rule of thumb" used to determine acquisition sweep speed. By this rule, the rate is equivalent to a rate producing 0.5 radian phase error. For a loop with a B_{L_o} = 1 Hz, the sweep rate is 1.88 rad/sec^2.

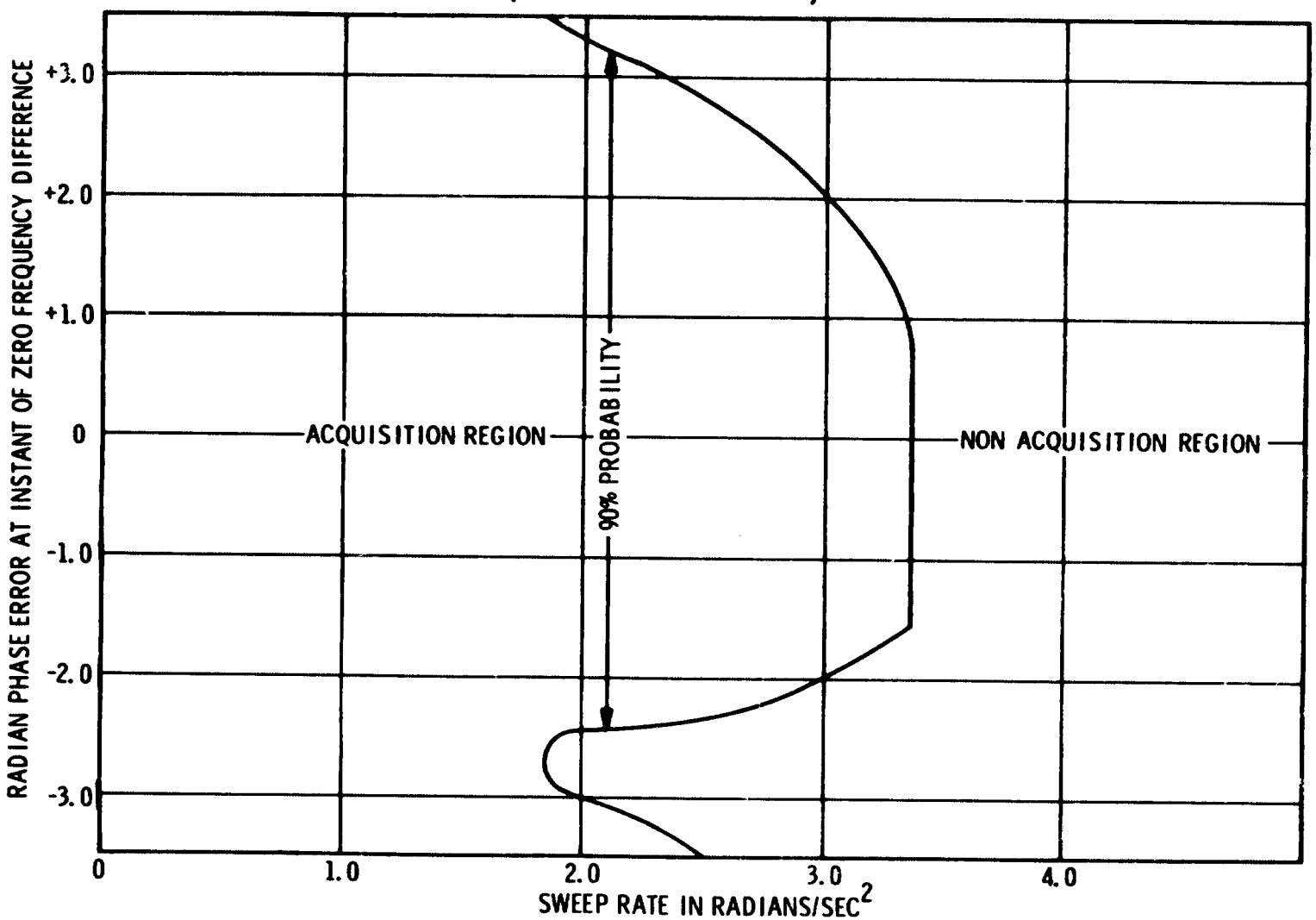
For a Type III loop, the first integrator levels off the phase transient effect so that the phase error at zero frequency crossing has little effect on the acquisition rate. The remaining sweep rates are shown in table 4-3. It would appear that the Type III loop would be faster than the Type II loop. However, in the presence of noise much of this difference would be eliminated since the Type II loop has a large region whose higher sweep speeds are allowable and noise would not affect the lock probability as fast due to this region as would the Type III loop which has no such region. The large amount of computing time necessary to determine the probability of lock with noise present, precluded its study. A serious problem in acquiring a Type III loop is the effect of offset bias errors at the input to the first integrator. This error forms a ramp voltage at the integrator output. This output can get quite large so that it overloads the second integrator preventing control of the sweep. The effect of this error was not included in table 4-3. In practice it would be impossible to eliminate this problem so that Type III loops cannot be directly acquired. The Type III loop is acquired as a Type II loop by shorting out the capacitor in the first integrator with a resistor. After acquisition, the resistor shunt is lifted, changing the order of the loop to Type III. The block diagrams of the Type II and Type III acquisition circuit are shown in figure 4-6. The acquisition switching is shown on the Type III loop. As shown in the figure, the zero of the second integrator section must be changed to provide an optimized Type II loop with the same bandwidth as the Type III loop.

Figure 4-4.


Phase Error Tracings of PLL with Acquisition Sweep at 3.0 rad/sec² with B_{Lo} = 1.0 Hz showing effect of different phase errors at zero frequency difference.
ϕ_e +2.5
ϕ_e +1.1
+π
0
-π
-3π
PHASE ERROR
19.0
20.
21.
22.
23.
24.
25.
26.
27.
28
29
TIME IN SECONDS

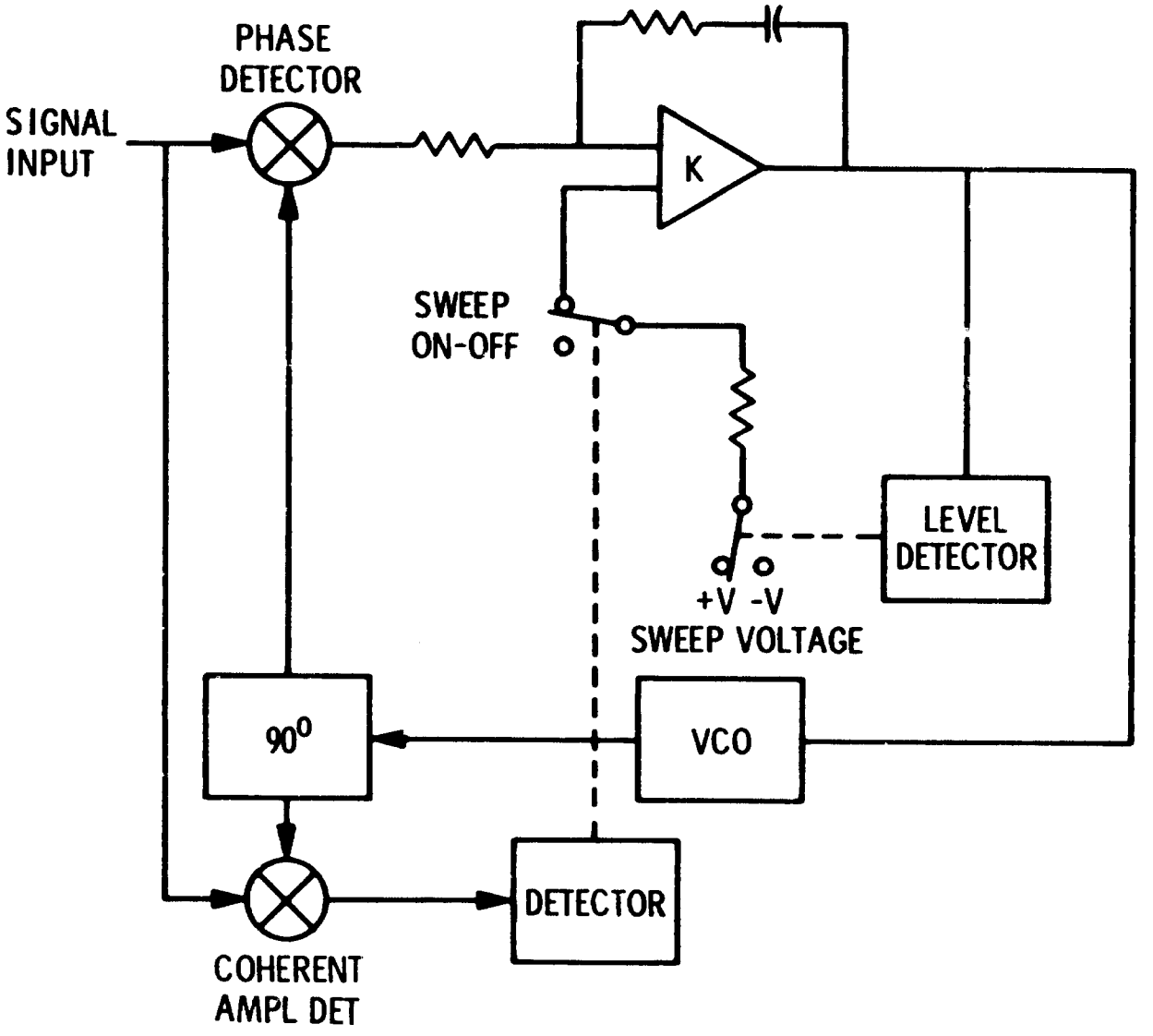
4-5 ACQUISITION REGION OF 2ND ORDER PLL WITH BL_0 = 1.0 Hz USING FREQUENCY SWEEP

(STRONG SIGNAL CASE)



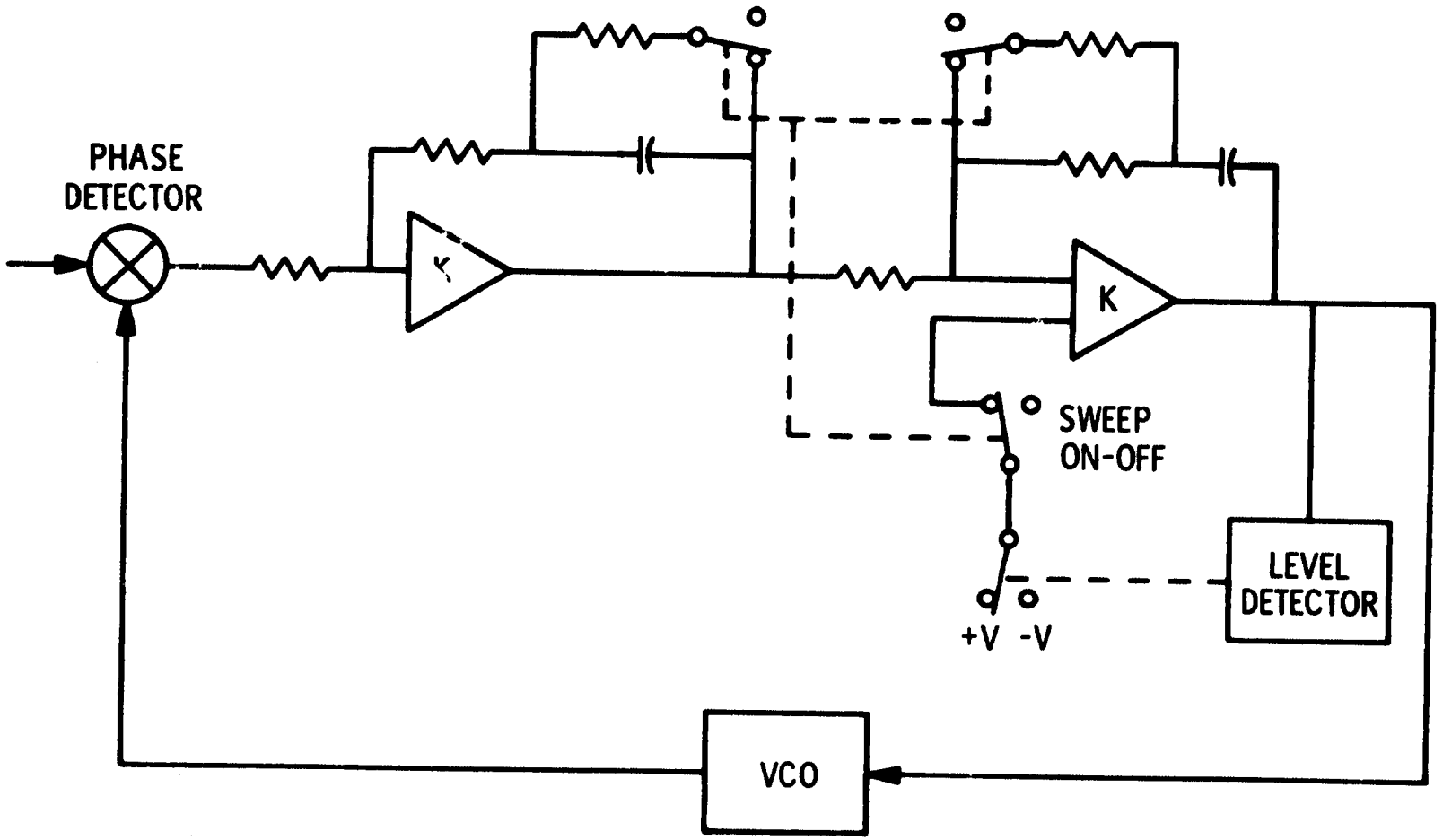
8278-60

4-6A TYPE II ACQUISITION



8278-54

4-6B TYPE III ACQUISITION



8278-55

Table 4-3. Maximum Strong Signal Acquisition Sweep Rates

Type II Maximum Rate	3.36 rad/sec^2
Type II (90% probability)	2.10 rad/sec^2
Mallincrodt Loop	2.04 rad/sec^2
Pool Loop	2.06 rad/sec^2
Approx. Minimum Peak Loop Type II	2.42 rad/sec^2

The frequency memory that a Type II loop possesses at time of loss of lock can be utilized to good advantage. Upon loss of lock the acquisition sweep is not reinitiated until such time as the difference between the vco and signal frequencies exceeds the self pull-in range. For near earth orbits, the dynamic plus the nominal offset errors permit a wait time of about 1 second. Using this type of operation, a minimum of unlock time is experienced due to a momentary loss of lock. The Type III loop possesses rate memory as well as frequency memory. Both can be used in a similar manner. The wait time is limited by circuit unbalances which drive the vco beyond the self pull-in range. At that time the loop would revert back to a Type II loop and sweep would be initiated.

4.1.4 Conclusions

From the analysis, it may be concluded that to extend the capability of the phase lock loop to the utmost the following steps could be taken:

1. Use self acquisition.
2. Narrow the bandwidth.
3. Use Type II or Type III loop.
4. Use envelope AGC instead of limiters.

For missions out to lunar distances, a Type III loop is not necessary. For these missions, the choice of AGC or limiters is also not critical since only a db in signal threshold is involved. The bandwidth can generally be chosen to optimize the acquisition time since signal to noise densities for these distances are quite high.

For planetary distances the phase lock loop could operate as a Type II with command switching to a Type III when high rate dynamics are expected.

4.1.5 Phase Lock Loop Model

The model for the phase lock loop is shown in block diagram form in figure 4-7. For linear amplifier operation, the noise is added after the phase detector since at that point only one normally distributed random variable needs to be used. The algorithm for the integrals uses a first order hold so that the integration operator is:

$$D(z) = \frac{\frac{T}{2}(3Z - 1)}{Z(Z - 1)}$$

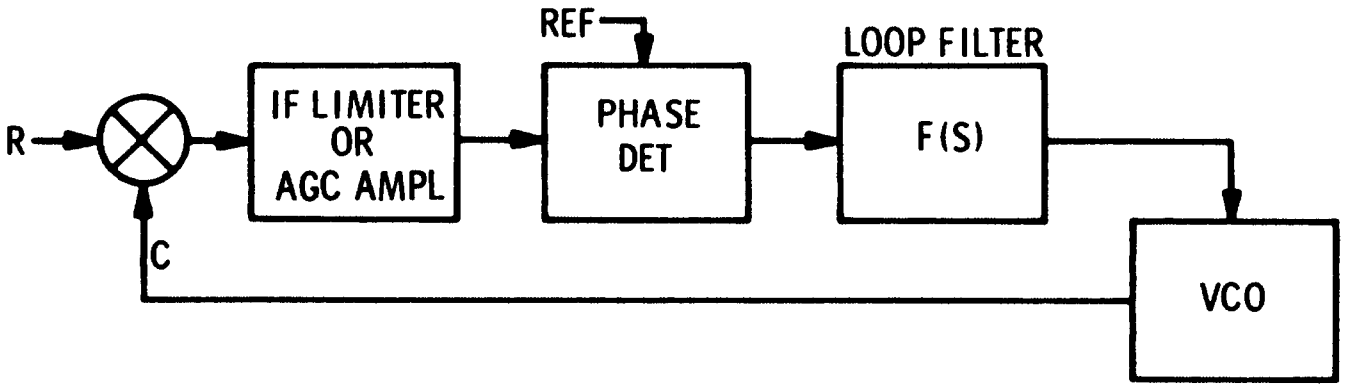
The operation is

$$Y_{k+1} = Y_k + \frac{T}{2}(3Y'_k - Y'_{k-1})$$

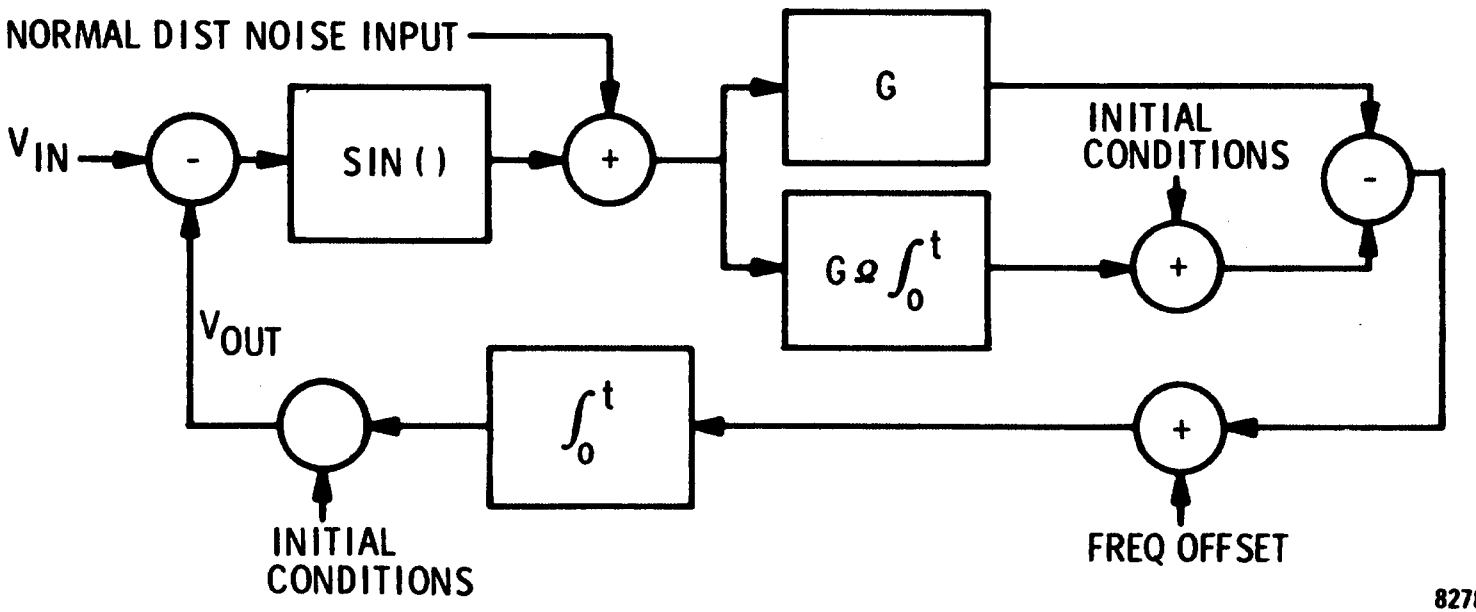
where the Y are outputs and the Y' are inputs. For a one sided noise bandwidth of 1 Hz, a T of 0.025 second was used. For the loop without noise input, a sample rate corresponding to T = 0.5 was sufficient to describe the transient behavior within 10% of the continuous function. The higher sample rate was used to ensure a flat noise spectrum input over the bandwidth. The noise spectrum used was checked by using a Fast Fourier Transfer to provide a square filter equivalent to the noise bandwidth of the loop. The output of this filter was analyzed to ensure its conformance to Gaussian noise.

For the limited amplifier, a different noise input was used to conserve computer time. The noise was inserted as an input signal by choosing numbers at random from a population conforming to the angle density distribution function for a given predetection signal to noise ratio. The input signal to noise corresponded to a bandwidth 16 db wider than the loop bandwidth. To provide the same bandwidth, the phase detector gain was increased by $1/\alpha_o$ where α_o is the signal suppression factor due to limiting. Again the noise signal was checked to ensure its conformance to the desired signal.

4-7A BLOCK DIAGRAM OF PLL



4-7B COMPUTER MODEL FOR LINEAR TYPE II LOOP



8278-52

The same model without noise input was used to check acquisition. For a Type III loop the loop filter consisted of two sections similar to the Type II loop filter.

4.1.6 Type III Loop

Open Loop Bode Plots and Root Locus Plots

Pool loop

```
G[S] NUMERATOR
      S 0 =          .12453391E 01
      S 1 =          .32739361E 01
      S 2 =          .21517536E 01

G[S] DENOMINATOR
      S 0 =          .00000000E 00
      S 1 =          .00000000E 00
      S 2 =          .00000000E 00
      S 3 =          .10000000E 01

LOOP GAIN AT          .10000000E-01  EQUALS       74.074  DB
FREQUENCY START =          .10000000E-01  HERTZ,      FREQUENCY FINISH =          .11220185E 03  HERTZ
INCREMENTS PER DECADE =   20

LOOP ZEROS, [SIGMA, OMEGA] IN HERTZ
             -.12107878E 00        .00000000E 00
             -.12107878E 00        .00000000E 00

LOOP POLES, [SIGMA, OMEGA] IN HERTZ
              .00000000E 00        .00000000E 00
              .00000000E 00        .00000000E 00
              .00000000E 00        .00000000E 00
```

Gain Margin = 15.06 DB

Phas-Margin = 54.30 Deg

Figure 4-8. Pool Loop

pool loop

FREQUENCY HERTZ	GAIN DB	PHASE DEG
	Δ PHASE	-180 -90 0 +90
	* MAG	- 40.0 - 20.0 0 20.0
.1000E-01	74.07	99.44.
.1122E-01	71.09	100.59.
.1259E-01	68.11	101.87.
.1413E-01	65.13	103.31.
.1585E-01	62.16	104.91.
.1778E-01	59.20	106.71.
.1995E-01	56.25	108.72.
.2239E-01	53.31	110.95.
.2512E-01	50.38	113.44.
.2818E-01	47.47	116.21.
.3162E-01	44.59	119.27.
.3548E-01	41.73	122.67.
.3981E-01	38.91	126.40.
.4467E-01	36.12	130.50.
.5012E-01	33.39	134.97.
.5623E-01	30.71	139.82.
.6310E-01	28.10	145.05.
.7079E-01	25.57	150.63.
.7943E-01	23.12	156.53.
.8913E-01	20.78	162.71.
.1000E 00	18.53	169.11.
.1122E 00	16.40	175.64.
.1259E 00	14.38	-177.77Δ
.1413E 00	12.48	-171.20.
.1585E 00	10.69	-164.76.
.1778E 00	9.00	-158.50.
.1995E 00	7.42	-152.50.
.2239E 00	5.92	-146.81.
.2512E 00	4.51	-141.47.
.2818E 00	3.16	-136.50.
.3162E 00	1.88	-131.90.
.3548E 00	.65	-127.68.
.3981E 00	-.54	-123.83.
.4467E 00	-1.69	-120.33.
.5012E 00	-2.82	-117.16.
.5623E 00	-3.91	-114.30.
.6310E 00	-4.99	-111.73.
.7079E 00	-6.06	-109.41.

Figure 4-9. Pool loop Bode Plot

Pool loop

•7943E 00	-7•11	-107•33•
•8913E 00	-8•15	-105•47•
•1000E 01	-9•18	-103•81•
•1122E 01	-10•21	-102•32•
•1259E 01	-11•23	-100•99•
•1413E 01	-12•24	-99•80•
•1585E 01	-13•26	-98•74•
•1778E 01	-14•27	-97•79•
•1995E 01	-15•28	-96•95•
•2239E 01	-16•28	-96•19•
•2512E 01	-17•29	-95•52•
•2818E 01	-18•29	-94•92•
•3162E 01	-19•30	-94•39•
•3548E 01	-20•30	-93•91•
•3981E 01	-21•30	-93•48•
•4467E 01	-22•30	-93•11•
•5012E 01	-23•30	-92•77•
•5623E 01	-24•30	-92•47•
•6310E 01	-25•30	-92•20•
•7079E 01	-26•31	-91•96•
•7943E 01	-27•31	-91•75•
•8913E 01	-28•31	-91•56•
•1000E 02	-29•31	-91•39•
•1122E 02	-30•31	-91•24•
•1259E 02	-31•31	-91•10•
•1413E 02	-32•31	-90•96•
•1585E 02	-33•31	-90•88•
•1778E 02	-34•31	-90•78•
•1995E 02	-35•31	-90•70•
•2239E 02	-36•31	-90•62•
•2512E 02	-37•31	-90•55•
•2818E 02	-38•31	-90•49•
•3162E 02	-39•31	-90•44•
•3548E 02	-40•31	-90•39•
•3981E 02	-41•31	-90•35•
•4467E 02	-42•31	-90•31•
•5012E 02	-43•31	-90•28•
•5623E 02	-44•31	-90•25•
•6310E 02	-45•31	-90•22•
•7079E 02	-46•31	-90•20•
•7943E 02	-47•31	-90•17•
•8913E 02	-48•31	-90•16•
•1000E 03	-49•31	-90•14•

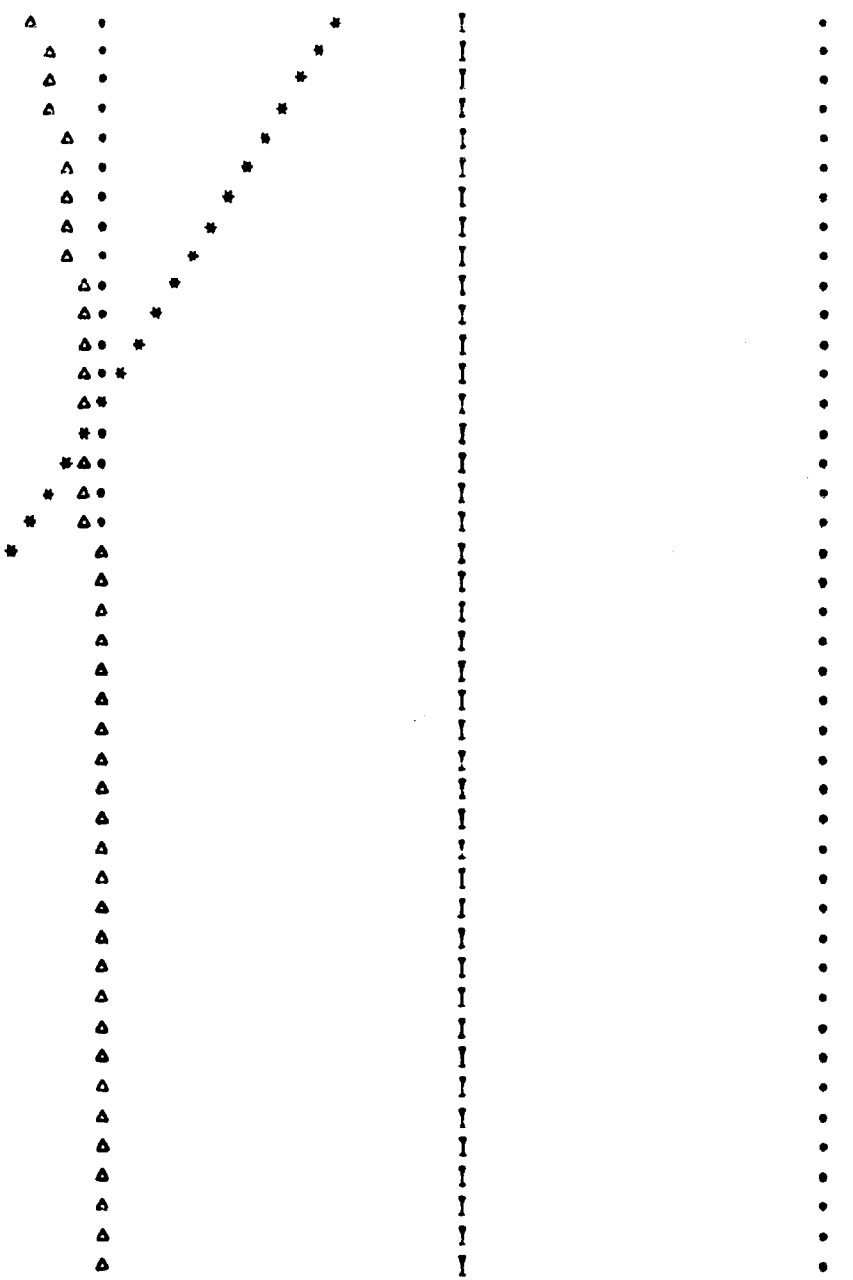


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Figure 4-10. Pool loop Bode plot.

Approx Min peak loop

```
G[S] NUMERATOR
      S 0 =          .10543378E 01
      S 1 =          .32556585E 01
      S 2 =          .25132628E 01


G[S] DENOMINATOR
      S 0 =          .00000000E 00
      S 1 =          .00000000E 00
      S 2 =          .00000000E 00
      S 3 =          .10000000E 01


LOOP GAIN AT          .10000000E-01  EQUALS       72.650  DB
FREQUENCY START =          .10000000E-01  HERTZ,      FREQUENCY FINISH =          .11220185E 03  HERTZ
INCREMENTS PER DECADE =   20


LOOP ZEROS, [SIGMA, OMEGA] IN HERTZ
             -.10308404E 00        -.21465232E-06
             -.10308404E 00         .21465232E-06


LOOP POLES, [SIGMA, OMEGA] IN HERTZ
              .00000000E 00         .00000000E 00
              .00000000E 00         .00000000E 00
              .00000000E 00         .00000000E 00
```

Gain Margin = 17.81 DB

Phase Margin = 62.61 Deg

Figure 4-11. Approx Min Peak Loop

Approx Min Peak Loop

FREQUENCY HERTZ	GAIN DB	PHASE DEG
4-30		
	Δ PHASE	-180 -90 0 +90
	* MAG	-40.0 -20.0 0 20.0
.1000E-01	72.65	101.08
.1122E-01	69.67	102.42
.1259E-01	66.70	103.93
.1413E-01	63.73	105.61
.1585E-01	60.77	107.48
.1778E-01	57.82	109.58
.1995E-01	54.89	111.91
.2239E-01	51.97	114.51
.2512E-01	49.07	117.39
.2818E-01	46.19	120.58
.3162E-01	43.35	124.11
.3548E-01	40.54	127.99
.3981E-01	37.78	132.23
.4467E-01	35.06	136.86
.5012E-01	32.41	141.86
.5623E-01	29.83	147.23
.6310E-01	27.33	152.94
.7079E-01	24.92	158.96
.7943E-01	22.62	165.23
.8913E-01	20.42	171.69
.1000E 00	18.33	178.26
.1122E 00	16.36	-175.15
.1259E 00	14.50	-168.62
.1413E 00	12.75	-162.24
.1585E 00	11.11	-156.08
.1778E 00	9.56	-150.20
.1995E 00	8.10	-144.65
.2239E 00	6.71	-139.45
.2512E 00	5.39	-134.63
.2818E 00	4.13	-130.18
.3162E 00	2.92	-126.11
.3548E 00	1.75	-122.40
.3981E 00	.60	-119.03
.4467E 00	-.51	-115.99
.5012E 00	-1.60	-113.24
.5623E 00	-2.67	-110.78
.6310E 00	-3.73	-108.56
.7079E 00	-4.78	-106.57

Figure 4-12. Approx Min Peak Loop Bode Plot

Approx Min peak loop

.7943E	00	-5.81	-104.79.
.8913E	00	-6.84	-103.20.
.1000E	01	-7.87	-101.77.
.1122E	01	-8.89	-100.50.
.1259E	01	-9.90	-99.36.
.1413E	01	-10.91	-98.35.
.1585E	01	-11.92	-97.44.
.1778E	01	-12.93	-96.64.
.1995E	01	-13.94	-95.92.
.2239E	01	-14.94	-95.27.
.2512E	01	-15.94	-94.70.
.2818E	01	-16.95	-94.19.
.3162E	01	-17.95	-93.73.
.3548E	01	-18.95	-93.33.
.3981E	01	-19.95	-92.97.
.4467E	01	-20.95	-92.64.
.5012E	01	-21.96	-92.36.
.5623E	01	-22.96	-92.10.
.6310E	01	-23.96	-91.87.
.7079E	01	-24.96	-91.67.
.7943E	01	-25.96	-91.49.
.8913E	01	-26.96	-91.33.
.1000E	02	-27.96	-91.18.
.1122E	02	-28.96	-91.05.
.1259E	02	-29.96	-90.94.
.1413E	02	-30.96	-90.84.
.1585E	02	-31.96	-90.75.
.1778E	02	-32.96	-90.66.
.1995E	02	-33.96	-90.59.
.2239E	02	-34.96	-90.53.
.2512E	02	-35.96	-90.47.
.2818E	02	-36.96	-90.42.
.3162E	02	-37.96	-90.37.
.3548E	02	-38.96	-90.33.
.3981E	02	-39.96	-90.30.
.4467E	02	-40.96	-90.26.
.5012E	02	-41.96	-90.24.
.5623E	02	-42.96	-90.21.
.6310E	02	-43.96	-90.19.
.7079E	02	-44.96	-90.17.
.7943E	02	-45.96	-90.15.
.8913E	02	-46.96	-90.13.
.1000E	03	-47.96	-90.12.

Figure 4-13. Approx Min Peak Loop Bode Plot

Mallinckrodt loop

```
G(S) NUMERATOR
     S 0 =          .60949958E 00
     S 1 =          .27171496E 01
     S 2 =          .30282637E 01

G(S) DENOMINATOR
     S 0 =          .00000000E 00
     S 1 =          .00000000E 00
     S 2 =          .00000000E 00
     S 3 =          .10000000E 01

LOOP GAIN AT        .10000000E-01  EQUALS      67.977  DB
FREQUENCY START =        .10000000E-01  HERTZ,     FREQUENCY FINISH =        .11220185E 03  HERTZ
INCREMENTS PER DECADE =   20

LOOP ZEROS, (SIGMA, OMEGA) IN HERTZ
            -.71401997E-01      -.21465232E-06
            -.71401997E-01       .21465232E-06

LOOP POLES, (SIGMA, OMEGA) IN HERTZ
             .00000000E 00       .00000000E 00
             .00000000E 00       .00000000E 00
             .00000000E 00       .00000000E 00
```

Gain Margin = 22.52 DB

Phase Margin = 73.47 Deg

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Figure 4-14. Mallinckrodt Loop

Mallinckrodt loop

FREQUENCY HERTZ	GAIN DB	PHASE DEG
	△ PHASE	-180
	* MAG	- 40.0
•1000E-01	67•98	105•95•
•1122E-01	65•02	107•86•
•1259E-01	62•07	110•00•
•1413E-01	59•14	112•38•
•1585E-01	56•23	115•03•
•1778E-01	53•33	117•97•
•1995E-01	50•46	121•23•
•2239E-01	47•62	124•82•
•2512E-01	44•82	128•76•
•2818E-01	42•07	133•08•
•3162E-01	39•36	137•78•
•3548E-01	36•73	142•85•
•3981E-01	34•16	148•28•
•4467E-01	31•68	154•06•
•5012E-01	29•29	160•13•
•5623E-01	27•00	166•45•
•6310E-01	24•82	172•93•
•7079E-01	22•76	179•51•
•7943E-01	20•80	-173•90•
•8913E-01	18•97	-167•40•
•1000E 00	17•24	-161•06•
•1122E 00	15•61	-154•94•
•1259E 00	14•08	-149•12•
•1413E 00	12•64	-143•63•
•1585E 00	11•27	-138•50•
•1778E 00	9•96	-133•75•
•1995E 00	8•71	-129•38•
•2239E 00	7•50	-125•38•
•2512E 00	6•34	-121•74•
•2818E 00	5•20	-118•43•
•3162E 00	4•09	-115•45•
•3548E 00	3•01	-112•76•
•3981E 00	1•94	-110•34•
•4467E 00	•88	-108•16•
•5012E 00	-•17	-106•22•
•5623E 00	-1•20	-104•47•
•6310E 00	-2•23	-102•91•
•7079E 00	-3•25	-101•52•

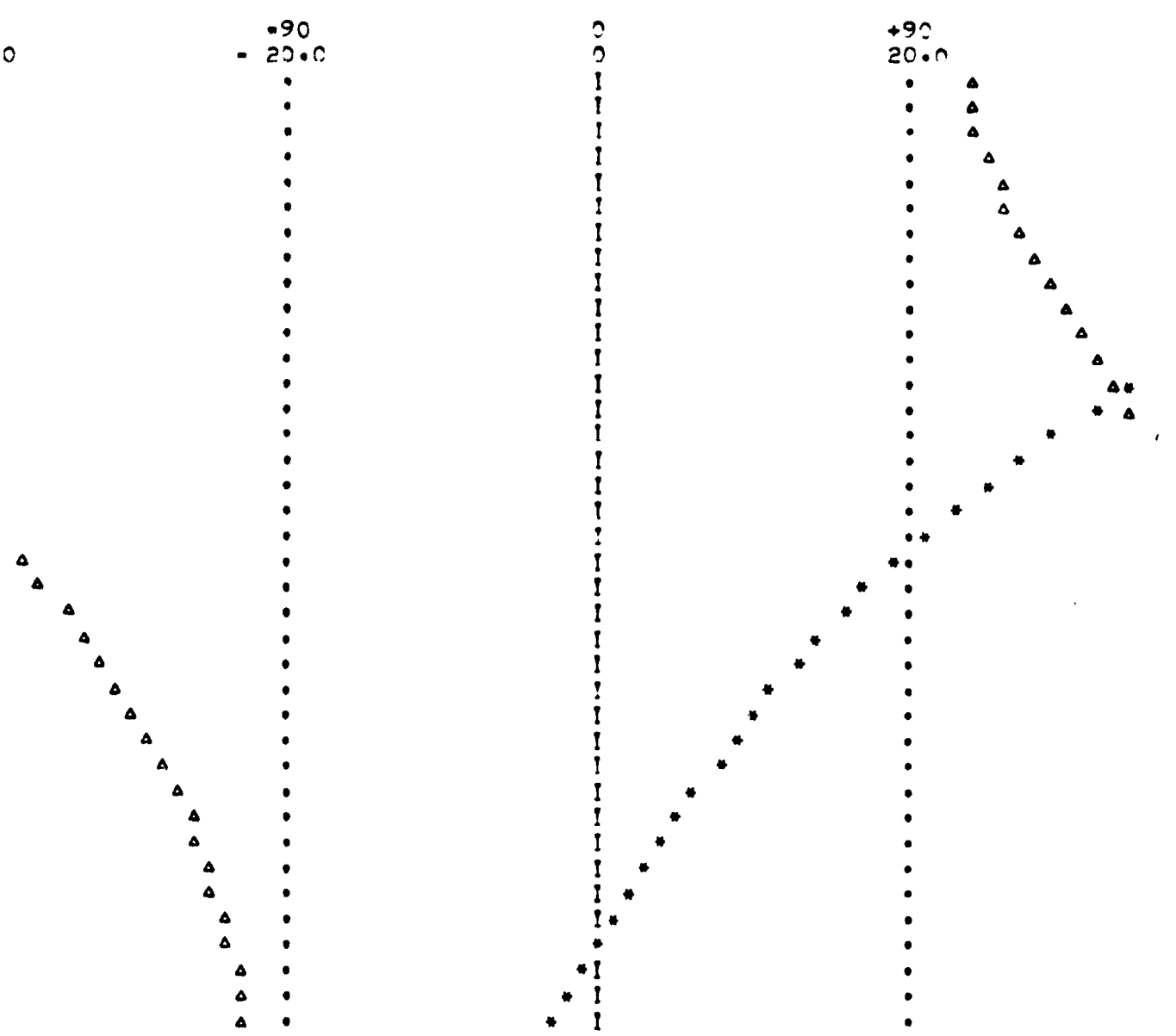


Figure 4-15. Mallinckrodt Loop Bode Plot

"Mallinckrodt" Loop

.7943E 00	-4.27	-100.27.
.8913E 00	-5.28	-99.16.
.1000E 01	-6.30	-98.17.
.1122E 01	-7.30	-97.28.
.1259E 01	-8.31	-96.49.
.1413E 01	-9.32	-95.79.
.1585E 01	-10.32	-95.16.
.1778E 01	-11.33	-94.60.
.1995E 01	-12.33	-94.10.
.2239E 01	-13.33	-93.65.
.2512E 01	-14.33	-93.26.
.2818E 01	-15.33	-92.90.
.3162E 01	-16.33	-92.59.
.3548E 01	-17.34	-92.31.
.3981E 01	-18.34	-92.06.
.4467E 01	-19.34	-91.83.
.5012E 01	-20.34	-91.63.
.5623E 01	-21.34	-91.45.
.6310E 01	-22.34	-91.30.
.7079E 01	-23.34	-91.16.
.7943E 01	-24.34	-91.03.
.8913E 01	-25.34	-90.92.
.1000E 02	-26.34	-90.82.
.1122E 02	-27.34	-90.73.
.1259E 02	-28.34	-90.65.
.1413E 02	-29.34	-90.58.
.1585E 02	-30.34	-90.52.
.1778E 02	-31.34	-90.46.
.1995E 02	-32.34	-90.41.
.2239E 02	-33.34	-90.37.
.2512E 02	-34.34	-90.33.
.2818E 02	-35.34	-90.29.
.3162E 02	-36.34	-90.26.
.3548E 02	-37.34	-90.23.
.3981E 02	-38.34	-90.21.
.4467E 02	-39.34	-90.18.
.5012E 02	-40.34	-90.16.
.5623E 02	-41.34	-90.15.
.6310E 02	-42.34	-90.13.
.7079E 02	-43.34	-90.12.
.7943E 02	-44.34	-90.10.
.8913E 02	-45.34	-90.09.
.1000E 03	-46.34	-90.08.

Figure 4-1o. Mallinckrodt Loop Bode Plot

Wiener Loop

```
G[S] NUMERATOR
      S 0 =          .17280000E 01
      S 1 =          .28800000E 01
      S 2 =          .24000000E 01


G[S] DENOMINATOR
      S 0 =          .00000000E 00
      S 1 =          .00000000E 00
      S 2 =          .00000000E 00
      S 3 =          .10000000E 01


LOOP GAIN AT          .10000000E-01  EQUALS       76.860  DB
FREQUENCY START =          .10000000E-01  HERTZ,      FREQUENCY FINISH =          .11220185E 03  HERTZ
INCREMENTS PER DECADE =   20


LOOP ZEROS, [SIGMA, OMEGA] IN HERTZ
             -.95493047E-01       -.95493047E-01
             -.95493047E-01        .95493047E-01


LOOP POLES, [SIGMA, OMEGA] IN HERTZ
              .00000000E 00        .00000000E 00
              .00000000E 00        .00000000E 00
              .00000000E 00        .00000000E 00
```

Gain Margin = 12.07 DB

Phase Margin = 60.45 Deg

Figure 4-17. Wiener Loop

Direct loop

FREQUENCY HERTZ	GAIN DB	PHASE DEG
•1000E-01	76•86	96•01•
•1122E-01	73•86	96•75•
•1259E-01	70•86	97•58•
•1413E-01	67•86	98•51•
•1585E-01	64•86	99•55•
•1778E-01	61•86	100•73•
•1995E-01	58•86	102•06•
•2239E-01	55•86	103•55•
•2512E-01	52•87	105•24•
•2818E-01	49•87	107•15•
•3162E-01	46•87	109•31•
•3548E-01	43•88	111•76•
•3981E-01	40•89	114•54•
•4467E-01	37•91	117•71•
•5012E-01	34•94	121•33•
•5623E-01	31•99	125•47•
•6310E-01	29•06	130•21•
•7079E-01	26•18	135•63•
•7943E-01	23•35	141•82•
•8913E-01	20•61	148•83•
•1000E 00	18•00	156•67•
•1122E 00	15•55	165•23•
•1259E 00	13•30	174•33•
•1413E 00	11•28	-176•36•
•1585E 00	9•48	-167•19•
•1778E 00	7•89	-158•49•
•1995E 00	6•47	-150•49•
•2239E 00	5•18	-143•29•
•2512E 00	3•99	-136•92•
•2818E 00	2•86	-131•33•
•3162E 00	1•78	-126•45•
•3548E 00	•73	-122•19•
•3981E 00	-•30	-118•46•
•4467E 00	-1•32	-115•20•
•5012E 00	-2•34	-112•34•
•5623E 00	-3•34	-109•82•
•6310E 00	-4•35	-107•60•
•7079E 00	-5•35	-105•64•

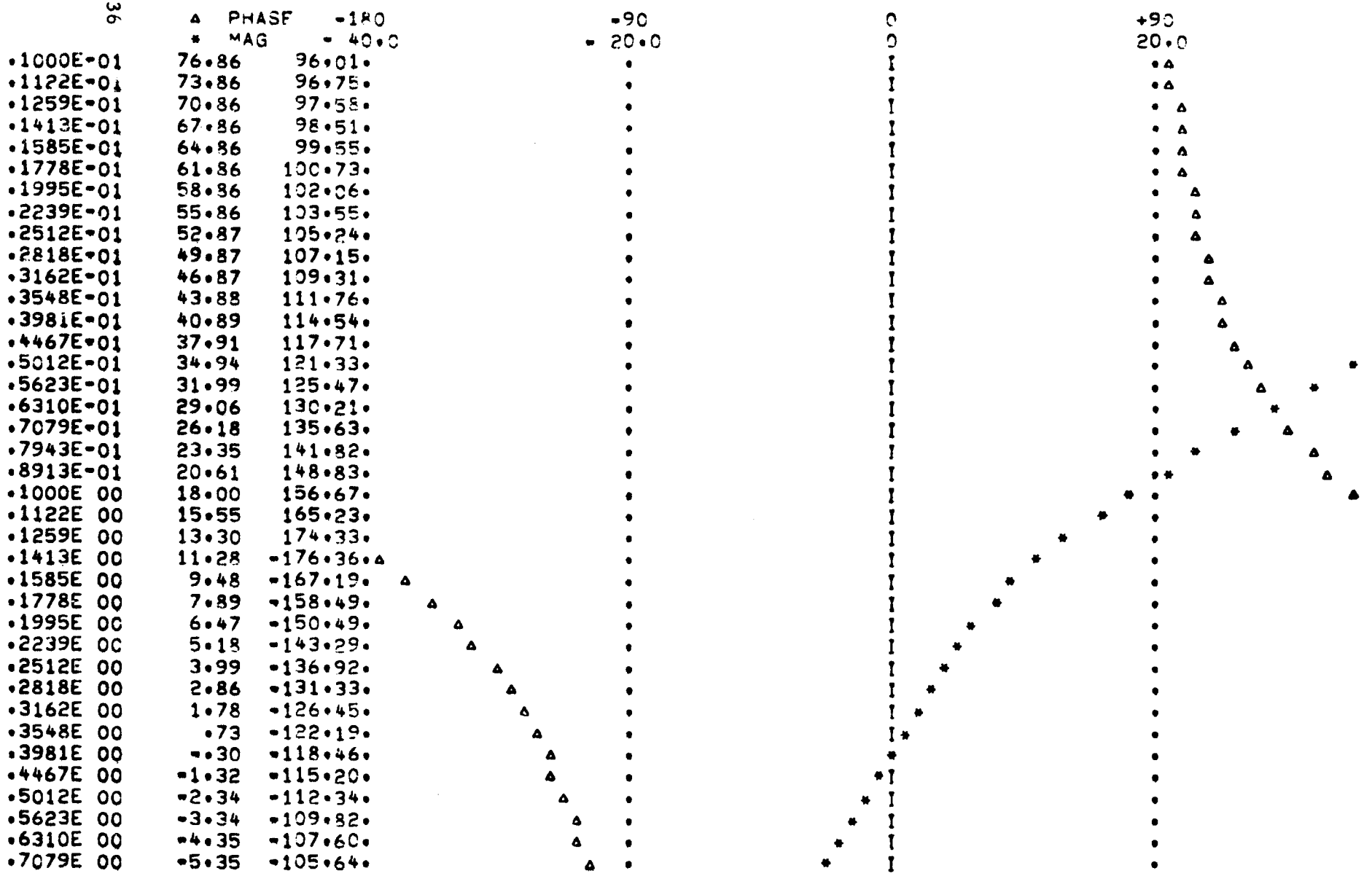


Figure 4-18. Wiener Loop Bode Plot

Wien loop

.7943E 00	-6.36	-103.91.
.8913E 00	-7.36	-102.37.
.1000E 01	-8.36	-101.01.
.1122E 01	-9.36	-99.80.
.1259E 01	-10.36	-98.73.
.1413E 01	-11.36	-97.77.
.1585E 01	-12.36	-96.92.
.1778E 01	-13.36	-96.17.
.1995E 01	-14.36	-95.49.
.2239E 01	-15.36	-94.89.
.2512E 01	-16.36	-94.36.
.2818E 01	-17.36	-93.89.
.3162E 01	-18.36	-93.46.
.3548E 01	-19.36	-93.09.
.3981E 01	-20.36	-92.75.
.4467E 01	-21.36	-92.45.
.5012E 01	-22.36	-92.18.
.5623E 01	-23.36	-91.95.
.6310E 01	-24.36	-91.73.
.7079E 01	-25.36	-91.55.
.7943E 01	-26.36	-91.38.
.8913E 01	-27.36	-91.23.
.1000E 02	-28.36	-91.09.
.1122E 02	-29.36	-90.98.
.1259E 02	-30.36	-90.87.
.1413E 02	-31.36	-90.77.
.1585E 02	-32.36	-90.69.
.1778E 02	-33.36	-90.62.
.1995E 02	-34.36	-90.55.
.2239E 02	-35.36	-90.49.
.2512E 02	-36.36	-90.44.
.2818E 02	-37.36	-90.39.
.3162E 02	-38.36	-90.35.
.3548E 02	-39.36	-90.31.
.3981E 02	-40.36	-90.27.
.4467E 02	-41.36	-90.24.
.5012E 02	-42.36	-90.22.
.5623E 02	-43.36	-90.19.
.6310E 02	-44.36	-90.17.
.7079E 02	-45.36	-90.15.
.7943E 02	-46.36	-90.14.
.8913E 02	-47.36	-90.12.
.1000E 03	-48.36	-90.11.

Figure 4-19. Wien Loop Bode Plot

Min peak loop

```
G(S) NUMERATOR
     S 0 =          .12066443E 01
     S 1 =          .31436057E 01
     S 2 =          .25462450E 01


G(S) DENOMINATOR
       S 0 =        .00000000E 00
       S 1 =        .00000000E 00
       S 2 =        .00000000E 00
       S 3 =        .10000000E 01


LOOP GAIN AT          .10000000E-01  EQUALS       73.785  DB
FREQUENCY START =          .10000000E-01  HERTZ,      FREQUENCY FINISH =          .11220185E 03  HERTZ
INCREMENTS PER DECADE =    20


LOOP ZEROS, (SIGMA, OMEGA) IN HERTZ
              -.98246794E-01       -.48491277E-01
              -.98246794E-01        .48491277E-01


LOOP POLES, (SIGMA, OMEGA) IN HERTZ
              .00000000E 00        .00000000E 00
              .00000000E 00        .00000000E 00
              .00000000E 00        .00000000E 00
```

Gain Margin = 16.44 DB

Phase Margin = 63.47 Deg

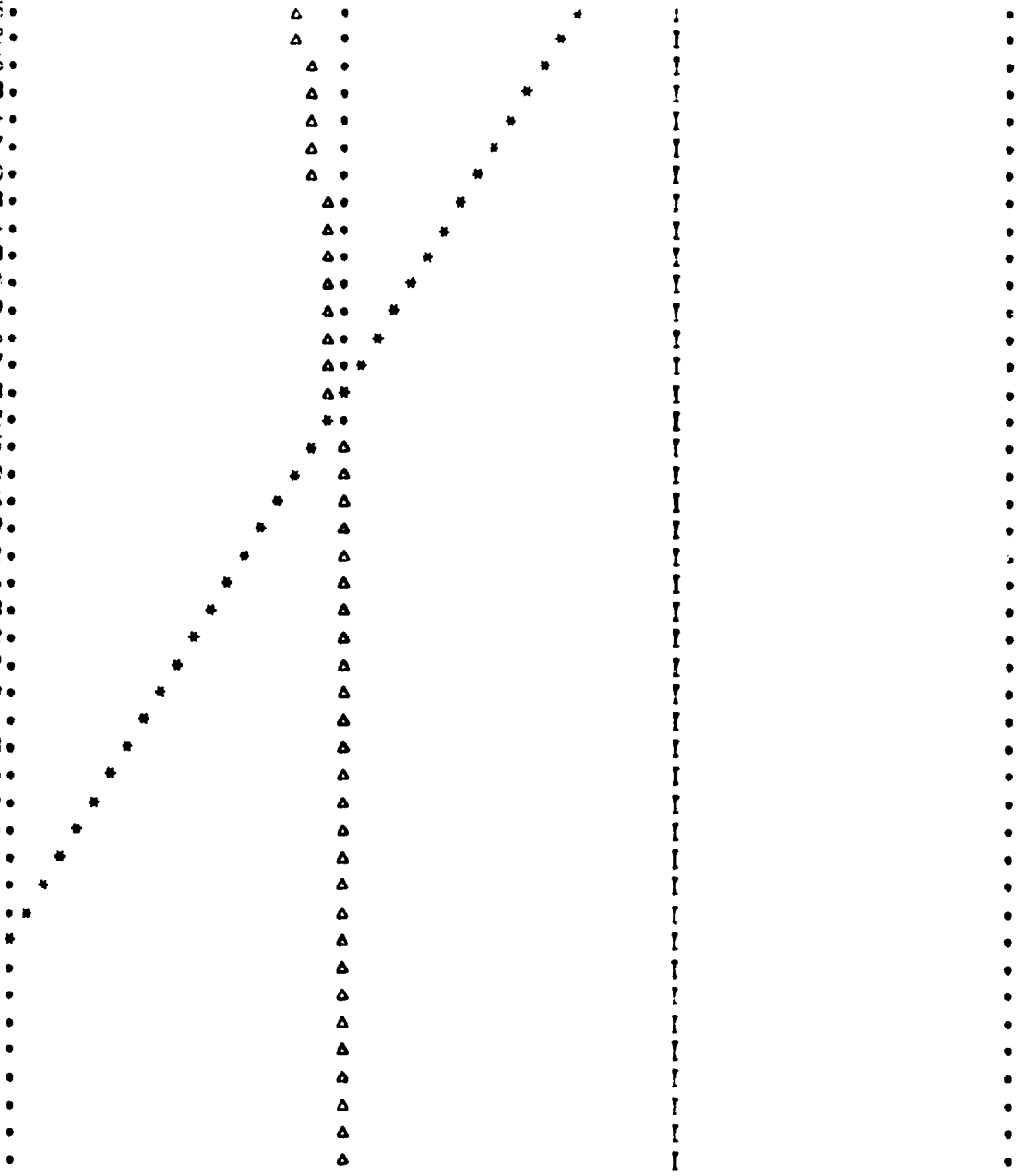
Figure 4-20. Min Peak Type III Loop

Min. peak Loop

FREQUENCY HERTZ	GAIN DB	PHASE DEG
	Δ PHASE	-180 -90 0 +90
	* MAG	- 40.0 - 20.0 0 20.0
.1000E-01	73.78	99.37.
.1122E-01	70.80	100.52.
.1259E-01	67.81	101.80.
.1413E-01	64.83	103.23.
.1585E-01	61.85	104.84.
.1778E-01	58.88	106.64.
.1995E-01	55.92	108.67.
.2239E-01	52.96	110.93.
.2512E-01	50.02	113.46.
.2818E-01	47.09	116.29.
.3162E-01	44.19	119.45.
.3548E-01	41.30	122.98.
.3981E-01	38.45	126.90.
.4467E-01	35.64	131.25.
.5012E-01	32.87	136.05.
.5623E-01	30.17	141.33.
.6310E-01	27.54	147.09.
.7079E-01	25.00	153.31.
.7943E-01	22.56	159.96.
.8913E-01	20.25	166.95.
.1000E 00	18.07	174.18.
.1122E 00	16.02	-178.48Δ
.1259E 00	14.13	-171.16. Δ
.1413E 00	12.36	-164.02. Δ
.1585E 00	10.73	-157.16. Δ
.1778E 00	9.21	-150.69. Δ
.1995E 00	7.79	-144.65. Δ
.2239E 00	6.45	-139.09. Δ
.2512E 00	5.18	-134.01. Δ
.2818E 00	3.97	-129.40. Δ
.3162E 00	2.80	-125.23. Δ
.3548E 00	1.67	-121.47. Δ
.3981E 00	.56	-118.10. Δ
.4467E 00	-.52	-115.08. Δ
.5012E 00	-1.59	-112.38. Δ
.5623E 00	-2.64	-109.96. Δ
.6310E 00	-3.69	-107.80. Δ
.7079E 00	-4.72	-105.87. Δ

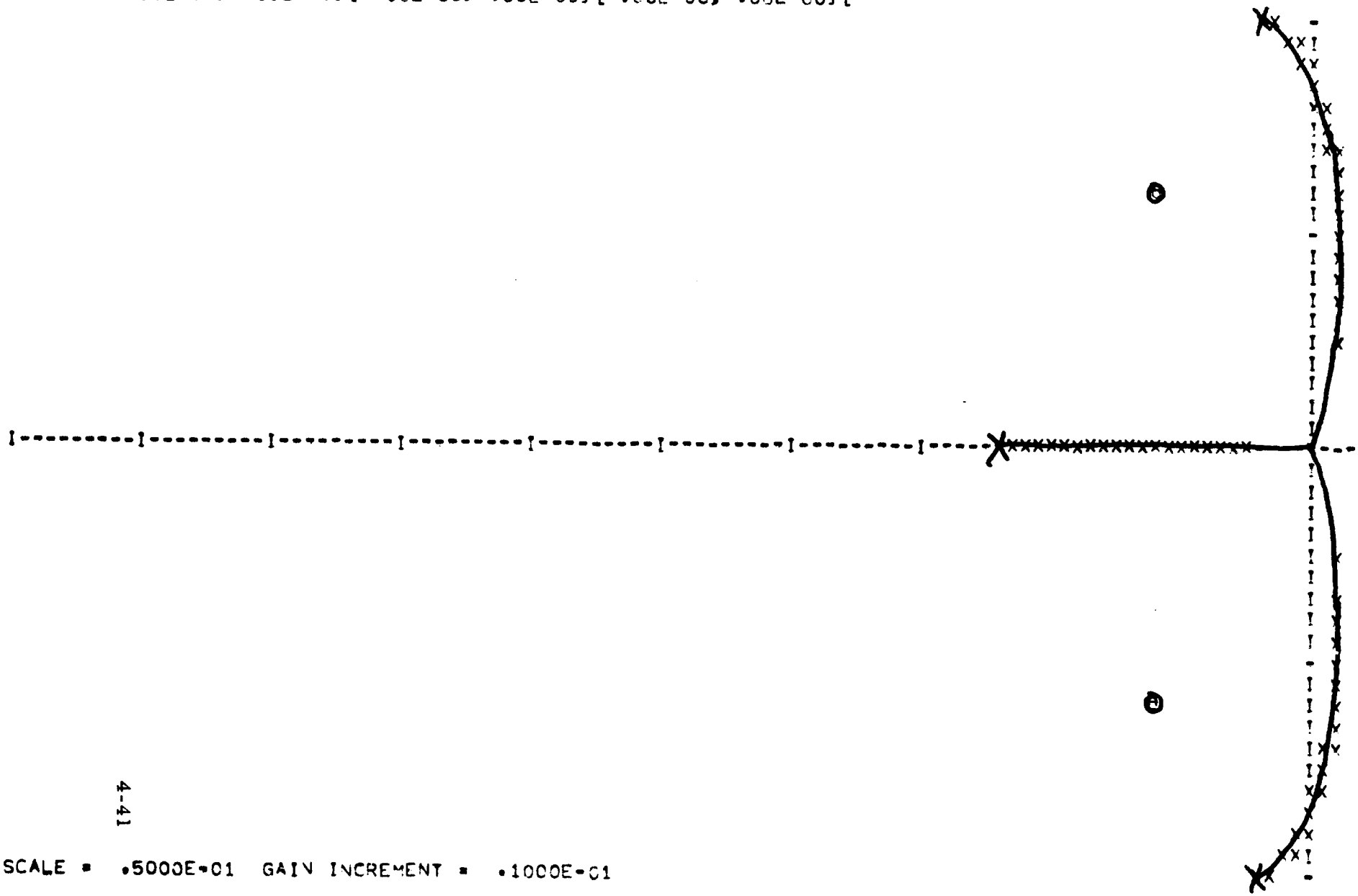
Figure 4-21. Min Peak Type III Loop Bode Plot

•7943E 00	-5•74	-104•15•
•8913E 00	-6•77	-102•62•
•1000E 01	-7•78	-101•25•
•1122E 01	-8•80	-100•03•
•1259E 01	-9•81	-98•94•
•1413E 01	-10•81	-97•97•
•1585E 01	-11•82	-97•10•
•1778E 01	-12•83	-96•33•
•1995E 01	-13•83	-95•64•
•2239E 01	-14•83	-95•03•
•2512E 01	-15•84	-94•48•
•2818E 01	-16•84	-93•99•
•3162E 01	-17•84	-93•56•
•3548E 01	-18•84	-93•17•
•3981E 01	-19•84	-92•83•
•4467E 01	-20•84	-92•52•
•5012E 01	-21•84	-92•25•
•5623E 01	-22•84	-92•00•
•6310E 01	-23•84	-91•78•
•7079E 01	-24•84	-91•59•
•7943E 01	-25•84	-91•42•
•8913E 01	-26•84	-91•26•
•1000E 02	-27•84	-91•13•
•1122E 02	-28•85	-91•00•
•1259E 02	-29•85	-90•89•
•1413E 02	-30•85	-90•80•
•1585E 02	-31•85	-90•71•
•1778E 02	-32•85	-90•63•
•1995E 02	-33•85	-90•56•
•2239E 02	-34•85	-90•50•
•2512E 02	-35•85	-90•45•
•2818E 02	-36•85	-90•40•
•3162E 02	-37•85	-90•36•
•3548E 02	-38•85	-90•32•
•3981E 02	-39•85	-90•28•
•4467E 02	-40•85	-90•25•
•5012E 02	-41•85	-90•22•
•5623E 02	-42•85	-90•20•
•6310E 02	-43•85	-90•18•
•7079E 02	-44•85	-90•16•
•7943E 02	-45•85	-90•14•
•8913E 02	-46•85	-90•13•
•1000E 03	-47•85	-90•11•



▲ENDJ98•

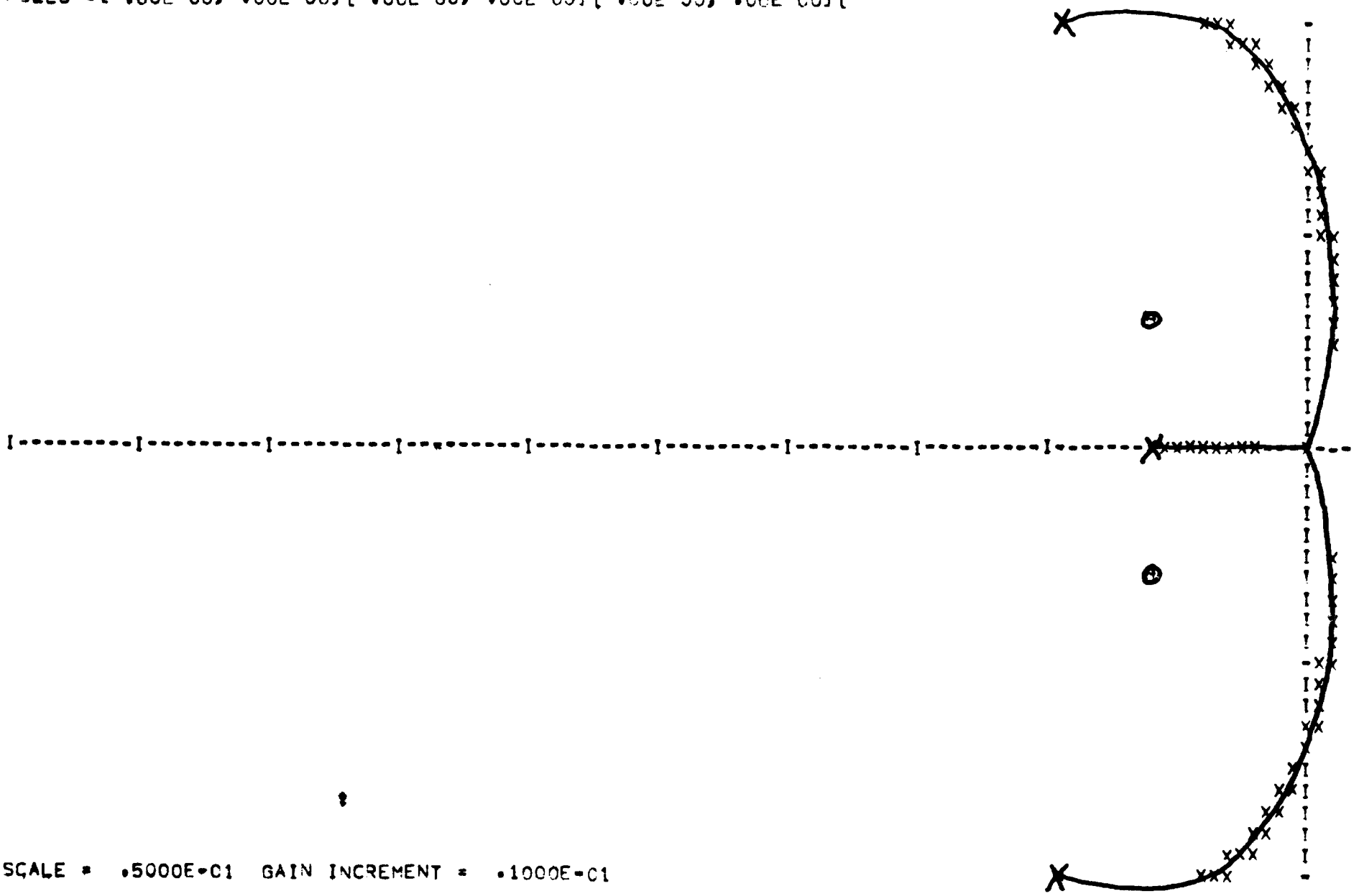
Figure 4-22. Min Peak Type II Loop Bode Plot



SCALE = .5000E-01 GAIN INCREMENT = .1000E-01

Figure 4-23. Weiner Loop Root Locus

ZEROS =[-.62E 00,-.30E 00][-.62E 00, .30E 00][
POLES =[.00E 00, .00E 00][.00E 00, .00E 00][.00E 00, .00E 00][



SCALE = .5000E-01 GAIN INCREMENT = .1000E-01

Figure 4-24. Minimum Peak Loop Root Locus

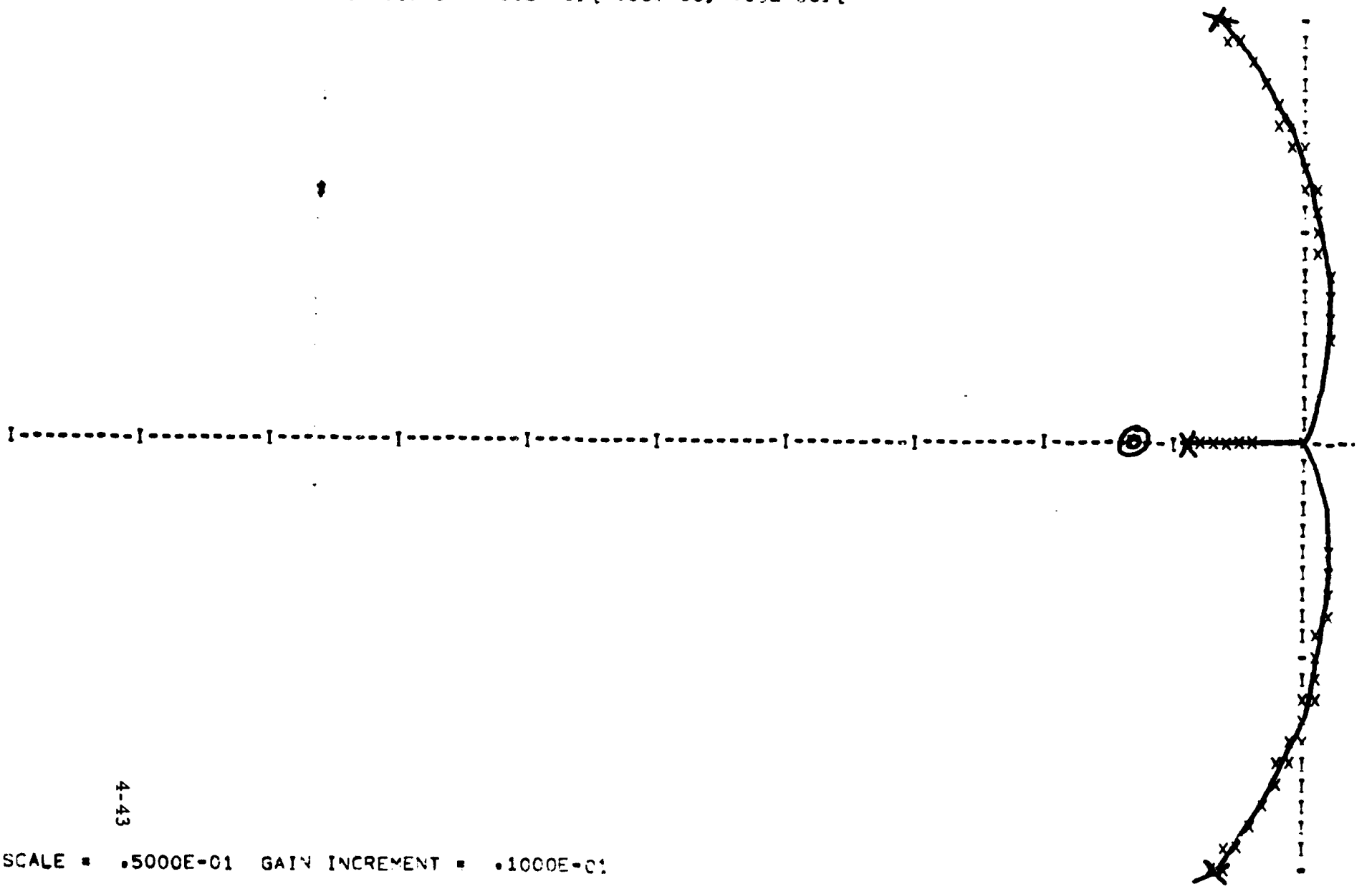
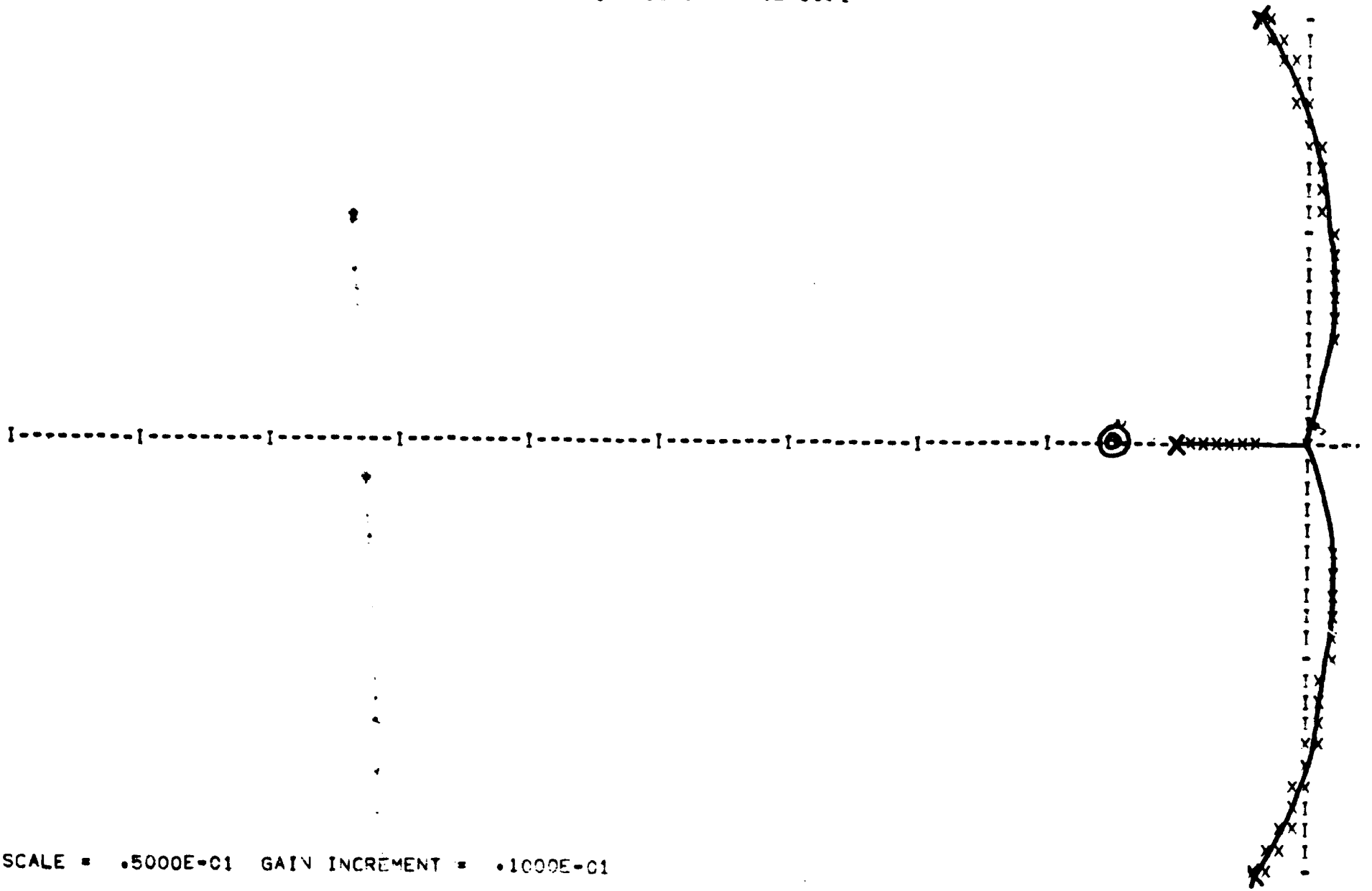


Figure 4-25. Approx Min Peak Root Locus

ZEROS =[-.76E 00, .00E 00][-.76E 00, .00E 00][
POLES =[.00E 00, .00E 00][.00E 00, .00E 00][.00E 00, .00E 00][



SCALE = .5000E-01 GAIN INCREMENT = .1000E-01

Figure 4-26. Pool Loop Root Locus

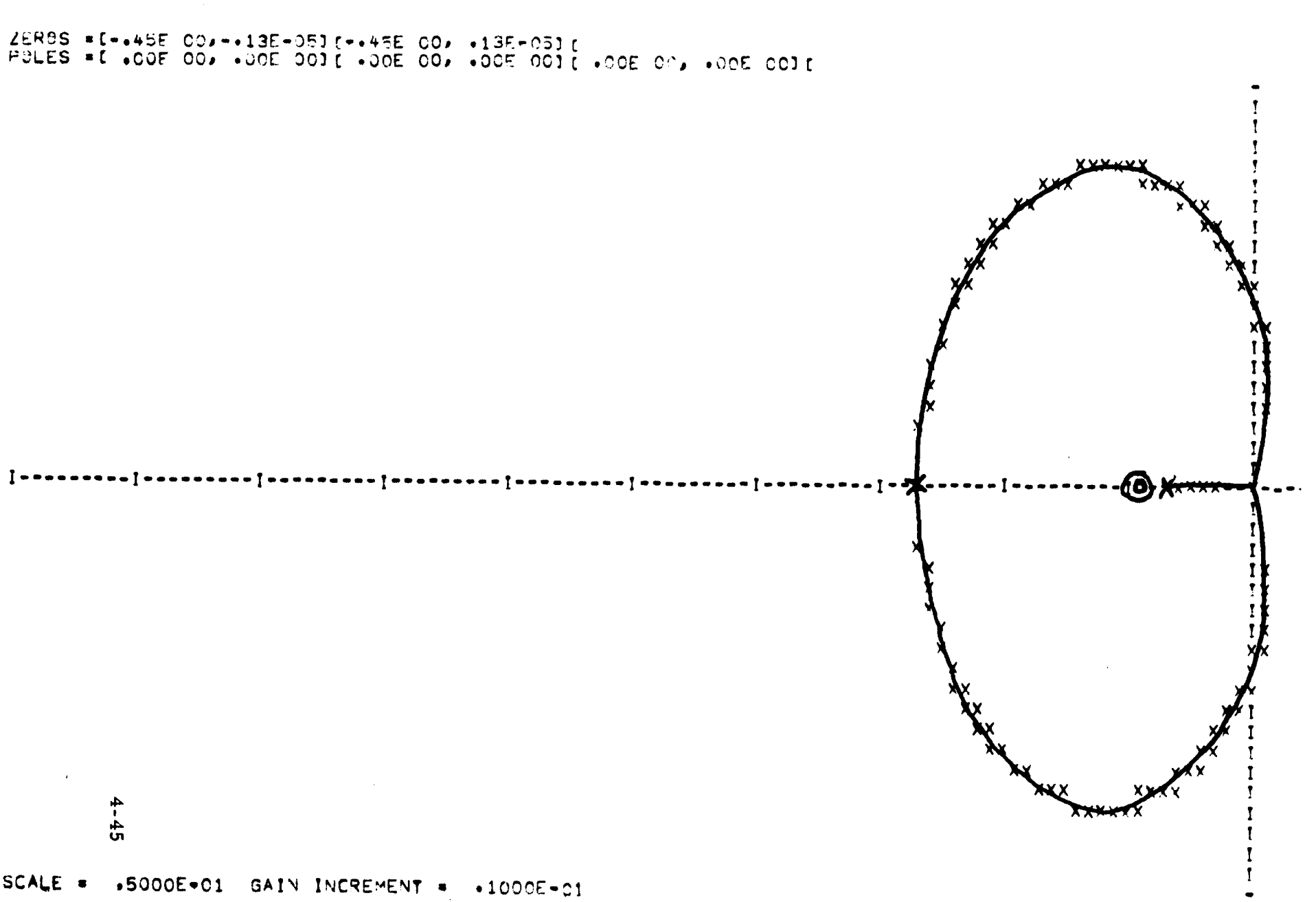


Figure 4-27. Mallincrodt Root Locus

4.1.7 Bibliography

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2. Weiner, N., Extrapolation, Interpolation, and Smoothing of Stationary Time Series, The Technology Press and John Wiley and Sons, Inc., 1949.

3. Pool, R. H., A Comparison of Second-Order and Third-Order Phase-Lock Loop Receivers, Master Thesis, State University of Iowa, 1962.

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6. Middleton, D., Introduction to Statistical Communication Theory, McGraw-Hill, 1960, pp. 416-417.

7. Charles, F. J. and Lindsey, W. C., "Some Analytical and Experimental Phase-Locked Loop Results for Low Signal-to-Noise Ratios, Proc. of IEEE, Vol. 54, September 1966.

8. Weaver, C. S., "Thresholds and Tracking Ranges in Phase-Locked Loops", IRE Transaction on Space Electronics and Telemetry, September 1961.

4.2 MODULATION ANALYSIS - AN ALL DIGITAL TRANSMISSION SYSTEM

4.2.1 Introduction

The present Apollo Unified S-Band Equipment (USBE) Communications System, although probably satisfactory for earth orbital and lunar missions, would be woefully lacking for Mars or other deep space missions. The USBE system is rather inefficient in terms of the power necessary to transmit the given information. More efficient means exist and probably should be used if the overall system is changed.

The existing system is also plagued by its high susceptibility to phase distortion and non-linear modulation-demodulation equipment. Furthermore the USBE is not really unified but is a bifurcated system. Television information is transmitted on a separate carrier from the other information thereby requiring an additional transmitter, modulator, coupling circuits, and other paraphernalia which could possibly be eliminated in another type of system. The USBE system is also hampered by a lack of flexibility in changing to meet other information transmission requirements. Finally, techniques are available today which were considered impossible or marginally impractical at the inception of the USBE system, and thus could not be exploited at that time.

In light of the above, it seems like a good time to review the requirements placed upon a space-earth communications system. To do this requires an investigation of the information requirements and the constraints that form the framework within which the system must be considered. Using these requirements and constraints as a base, a digital system can be described which will surpass the existing system with regard to both efficiency and performance.

4.2.2 System Information Requirements

4.2.2.1 Up-Link Voice

The present requirement to handle voice with a given intelligibility of 90% seems reasonable. To achieve this intelligibility requires about 31 db peak signal to rms noise[1] in a 3 kHz band. Three bit PCM gives a peak signal to rms noise ratio of only 22.8 db due to the quantizing noise. However, companding[2] will increase the signal to noise ratio by 9 db, thus meeting the requirement. Little additional noise is added if the probability of error is less than 10^{-3}. The information rate necessary will be 3 bits/sample, multiplied by two samples per cycle of the highest frequency, or 18 kilobits/second.

---

[1] Licklider, Journal of American Acoustical Society, October 1946.

[2] Smith, B., Instantaneous Companding of Quantized Signals, Bell Systems Technical Journal, May 1957.

4.2.2.2 Up-Link Data

An allocation of 2 kilobits/second appears to be sufficient to handle the present as well as future needs. The bit error rate of 10^{-6} which was a previous requirement will be assumed necessary. To be compatible with the up-link voice (in terms of same error rate) simple coding of three symbols per information bit may be employed which will then allow the same error rate. At a bit error rate of 10^{-3}, the equivalent bit rate is 6 kilobits/second.

4.2.2.3 Down-Link Voice

The down-link voice requirement will be assumed the same as the up-link voice requirement thus leading to a rate of 18 kilobits/second with a probability of error of 10^{-3}.

4.2.2.4 Down-Link Data

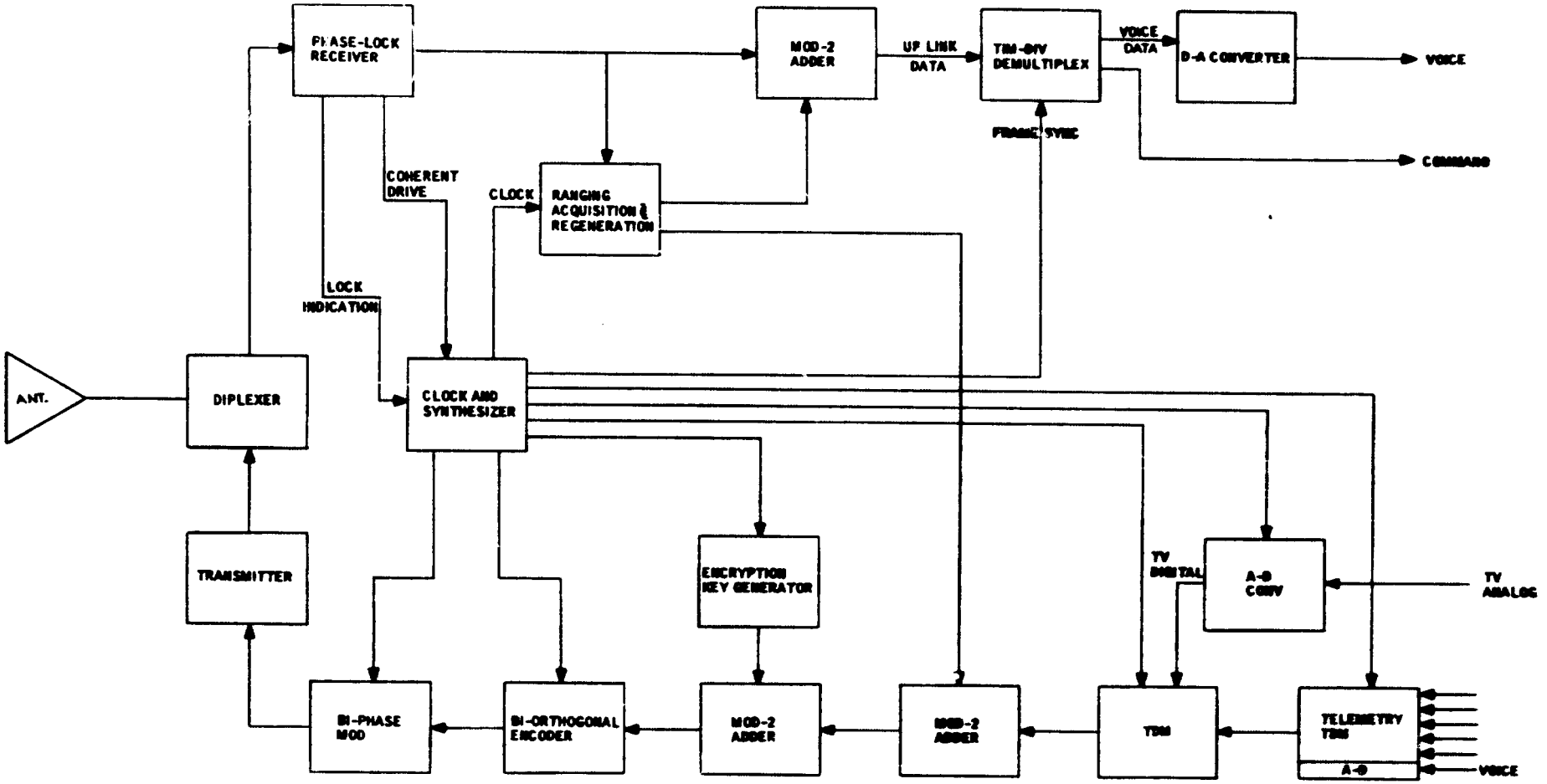
The present requirement calls for about 50 kilobits/second data rate with a bit error rate of 10^{-3}. This appears to be sufficient for present and future needs.

4.2.2.5 Down-Link Video

Television requirements for the Apollo mission call for two modes, the normal mode of 320 lines, 10 frames/second and a high resolution mode of 1280 lines/frame, .625 frame per second. With a digital system for other missions, it would seem reasonable and certainly more prudent, to find the information capacity of the channel first, and then tailor a television system to the channel characteristics and limitations. The allocation of bits/second for television will be discussed further after consideration of the transmission system.

4.2.2.6 Ranging

There seems to be some question about the efficacy of transmitting a ranging code in an all digital system. However, since no time was allotted to answering this question, it is assumed that a ranging code will be used. In the system considered here (see figure 4-28) the ranging code does not really use any of the transmitter power after acquisition has taken place. Prior to acquisition, the code must be transmitted alone to lock up the ranging system. After acquisition, the code is modulo-two added with the information data to provide a serial bit stream for



SPACECRAFT DIGITAL TRANSPONDER

Figure 4-28.

transmission. At the receiver, the serial stream is regenerated and modulo-two added with a replica of the ranging code thus restoring the original information data.

A summary of the system requirements is given in table 4-4 below along with the necessary information capacity and concomitant error probability.

Table 4-4. Information Requirements

Service	Capacity Required	Max Prob of Error
Uplink Voice	18 kb/s	10^{-3}
Uplink Data	2 kb/s	10^{-6}
Downlink Voice	18 kb/s	10^{-3}
Downlink Data	50 kb/s	10^{-3}
Downlink Video	To be determined	10^{-3}

4.2.3 System Constraints and Limitations

4.2.3.1 Power Limitation

Space systems are, for the most part, power limited systems since spacecraft must generate their own power from solar energy for long mission applications. In a recent study, Goldstein[1] considers 400 watts as a representative estimate of the maximum power to be available on a spacecraft in the future. Increases in power beyond 400 watts, require an increase in the vehicle weight which is considerably larger than the improvement would justify. Considering the usual transmitter efficiency to be about 20 percent sets the transmitter power at about 80 watts maximum.

4.2.3.2 System Noise Temperature

In the past, spacecraft communication system noise temperatures of about 2610 degrees Kelvin (10 db noise figure) have been the norm. Future systems are expected to have an improved system noise temperature. Current technical prowess[2] has demonstrated a 7.5 db noise figure front end using silicon transistors and 5.5 db using germanium devices. Further advances are expected to reduce

1. Goldstein, B.S., "Communication from Mars: Requirements and Limitations," IEEE Trans. on Aerospace and Electronics Systems, May 1968.

2. "Advanced S-Band Transponder Concept Review, "Motorola, Inc., May 28, 1968.

this figure to 5 db (1740°K), the figure which will be used here. The ground terminal has a more elaborate maser front end which allows a system noise temperature of about 30°K maximum.

4.2.3.3 Antenna Gain

The antenna capability imposes a definite system constraint. The largest antenna considered to date (but not flown) has been a 30 foot erectable paraboloid. The results of anticipated tests on the Applied Technology Satellite should uncover the feasibility of using an antenna with this large an aperture. Other programs in the planning stage at this time propose using phased arrays with an aperture equivalent to the 30 foot paraboloid. The point is, a great deal of current effort is being expended to solve the problems of using large antennas in space. The prognosis appears favorable, and it does not require sophistry to argue that large antennas will be used in the near future. Accordingly, a 30 foot antenna is considered here. For earth-based stations, it does not seem reasonable to expect more antenna gain than would be available from the existing 210 foot antennas[1] although future needs may require combining a number of the antennas.

4.2.3.4 Other Considerations

The selection of frequencies is somewhat limited by certain factors. Increasing frequency would yield an increase in overall received signal if other factors did not enter into the picture. However, increasing frequency usually means a decrease in transmitter efficiency and also requires a better mechanical tolerance on the antenna. As a result, in the near future the frequency will probably be limited to S-band.

4.2.4 Transmission Capability

The transmission capacity of a space-earth communication system can now be determined from the assumed conditions which have been elaborated upon earlier. A summary of the system parameters is given in table 4-5.

1. Goldstein, et al.

Table 4-5. System Parameters

Parameter	Spacecraft	Earth Station
Transmitter Power	49 dbm	70 dbm
Receiver Noise Temperature	1740 degrees K	30 degrees K
Receiver Noise Density	-166.2 dbm/Hz	-184 dbm/Hz
Operating Frequency	2 GHz	2 GHz
Antenna Gain	43 db	60 db
Margin	6 db	6 db

Using these parameters results in a signal to noise density ratio (S/N_o) of 100.4 db/Hz and 96.6 db/Hz for spacecraft to earth and earth to spacecraft links respectively for a distance of 10 million statue miles. A plot of S/N_o is given in figure 4-29.

The next question to be answered is what is a reasonable S/N_o to give a maximum probability of error of 10^{-3}. If phase shift keying (PSK) without coding is used, the required predetection S/N is about 7 db. This, however, could be reduced using biorthogonal coding. This type of coding operation is sufficiently simple to be used on the down link. Biorthogonal coding techniques have been demonstrated, [1, 2] and the improvement in performance was shown to correspond to theoretical predictions. The up-link system probably should have a simple PSK modulation format in order to keep the amount of spacecraft equipment as minimal as possible.

1. Barnes, W. P., Reich, B. W., & Sos, J. W., A Data Handling System with Efficient Synchronization for an 8-bit, Biorthogonal Telemeter, NASA TM X-563-67-555, November 1967.
2. Saliga, T. V., An 8-bit Biorthogonal Telemeter System with Efficient and Flexible Sync for Space Communication, NASA TM X-711-67-76.

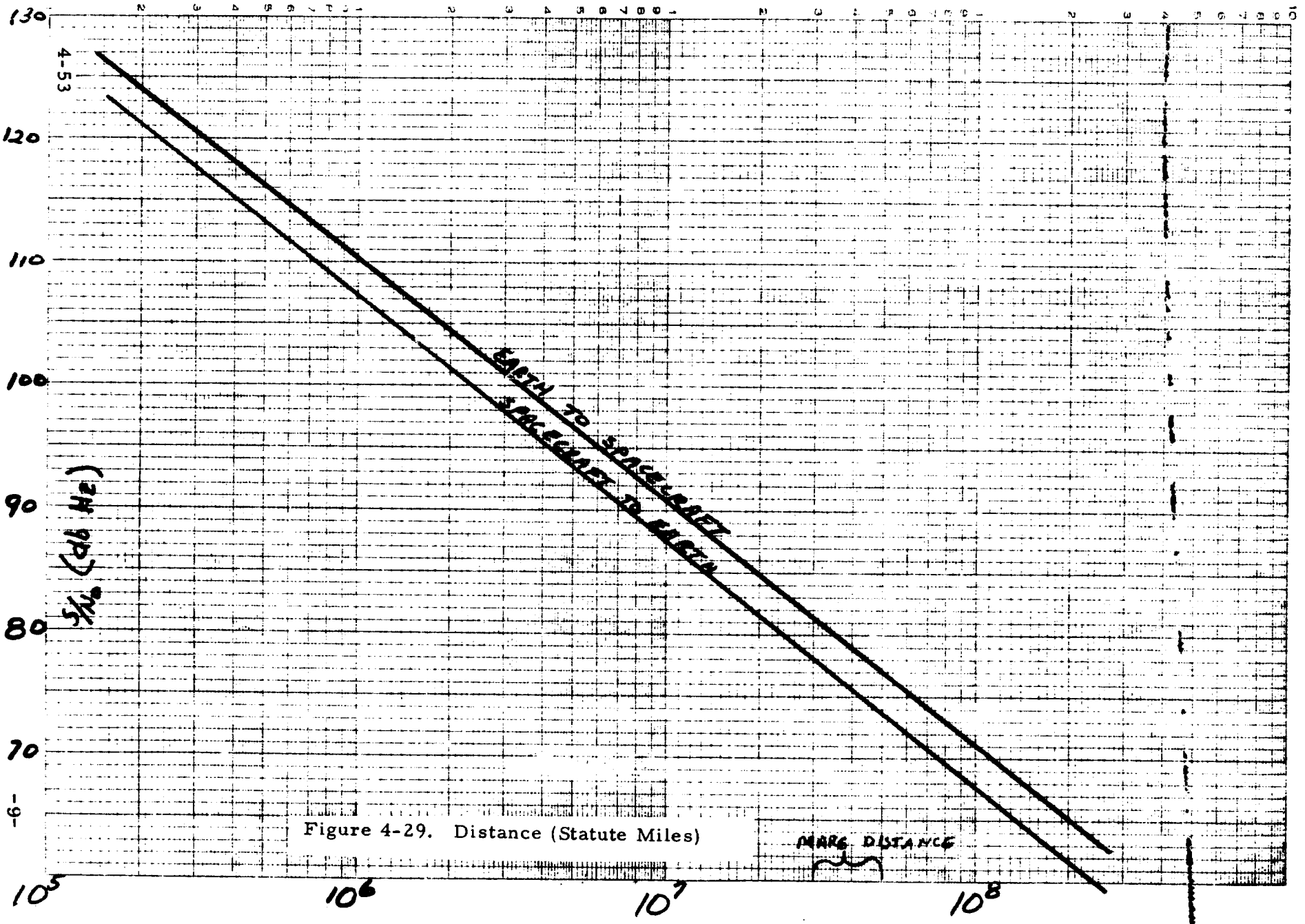


Figure 4-29. Distance (Statute Miles)

In considering the allocation of the channel capacity to the various services, it is apparent that only about 70 kb/s are needed for voice and telemetry, and therefore the majority of the capacity can be used for video transmission. For a Mars flight, 5 megabits per second is available for the video. If 5 bit encoding (32 discrete levels) of the video is used, about 500 kHz of bandwidth is supportable for the video, which means the Apollo television could be used. At distances larger than Mars-Earth, the frame rate or resolution would have to be decreased.

4.2.5 Digital System Description

A simplified block diagram of an all digital communication system is shown in figure 4-28. The received signal is a biphase modulated carrier from which the carrier is retrieved by folding and filtering with a phase-lock loop. A coherent detector and regenerator are used to reconstitute the data and provide buffering for the rest of the system. The incoming serial data is modulo-two added with a replica of the PRN ranging code to provide the original uplink data. Frame synchronization separates the uplink voice from the command data.

The transmitted carrier is derived from the uplink carrier thus providing a coherent turn-around for Doppler purposes. Time division multiplexed streams of digital video, telemetry, and voice are synchronized from a central synthesizer to give a serial data stream. The serial stream of data is modulo-two added with the ranging and with a key generator (if security is desired) and is then encoded in a biorthogonal encoder. The encoded data is used to biphase modulate the transmit carrier for down-link transmission.

As in any digital transmission system, synchronization is of paramount importance, but insufficient time does not permit more than a cursory look at the synchronization and acquisition problems inherent in this type of system. The acquisition can be accomplished initially by locking-up the carrier and ranging

without transmitting data. After the system is locked up, the data can be transmitted.

There are, of course, a myriad of problems incident to this type of system which have not been covered here. The antenna track, encryption synchronization, and framing are among some of these problems which need to be considered.

4.2.6 Conclusions

An all-digital communication system has a great deal to offer in future space missions. Digital systems can be made more efficient, are certainly more flexible, and allow encryption for security purposes. The digital format circumvents many of the non-linear problems inherent to linear systems. There are many questions as yet unanswered with regard to system problems, but the overall prognosis seems excellent. Further study is recommended to outline and resolve some of the problems. The design and construction of an all digital communication system is well within the present data capability and would seem like a worthwhile project.

4.3 ANTENNA ANALYSIS

4.3.1 Introduction

Several deficiencies in the LEM and CSM antenna tracking systems were displayed during system testing. Tracking errors of larger than expected magnitude were experienced when the uplink carrier was modulated. The combination of ranging and voice information caused the largest antenna excursions with the result that the system became unlocked on occasion. Because these effects were not predicted, a study was undertaken by TRW Systems to determine the causes of the problem and to suggest solutions from the results. Two conclusions were drawn from their analysis: [1] (1) Reduction of the modulation indices will diminish the tracking errors if no hardware changes can be made; and (2) replacement of

1. Sullivan, D. P., Wong, C. C., Chan, R. J., "Preliminary Analysis of the LM and CSM Antenna Tracking Systems", LM and CSM S-Band Antenna Tracking Studies: Task E-53A, Contract No. NAS9-4810, TRW Systems, October 24, 1967.

the coherent amplitude detector with a noncoherent one will reduce the effects if this constraint is removed. Both of these are reasonable, however, neither entirely solves the problem. The first would decrease the energy in the interference, but would not remove it, while the second would reduce the effect at the expense of tracking threshold. By a few modifications, the present system can be changed to a true monopulse system which will not have the problems described.

The recommended implementation has three significant advantages: (1) The single channel configuration of the present system is retained, (2) Minimal equipment changes are required, and (3) The error signal, including undesired a-c components, is proportional to the boresight error. The first of these is provided by the quadrature addition of the sum and difference signals. The error channels must first be phase modulated with a subcarrier so that this difference signal can be phase shifted 90^{o} and added to the sum channel signal. Because the tracking angle information is now contained in the composite signal phase, the existing wideband phase detector can be used as a demodulator for the tracking signal. Minimal equipment changes would be required to provide phase modulators for multiplexing the azimuth and elevation signals and to provide detectors for determining the error voltages from the wideband output. These hardware changes would provide a difference channel which is made up of the azimuth and elevation signals summed orthogonally on a subcarrier and a sum channel signal which is in quadrature with the difference signal. This total scheme converts the present system to a monopulse tracker without significantly modifying its configuration.

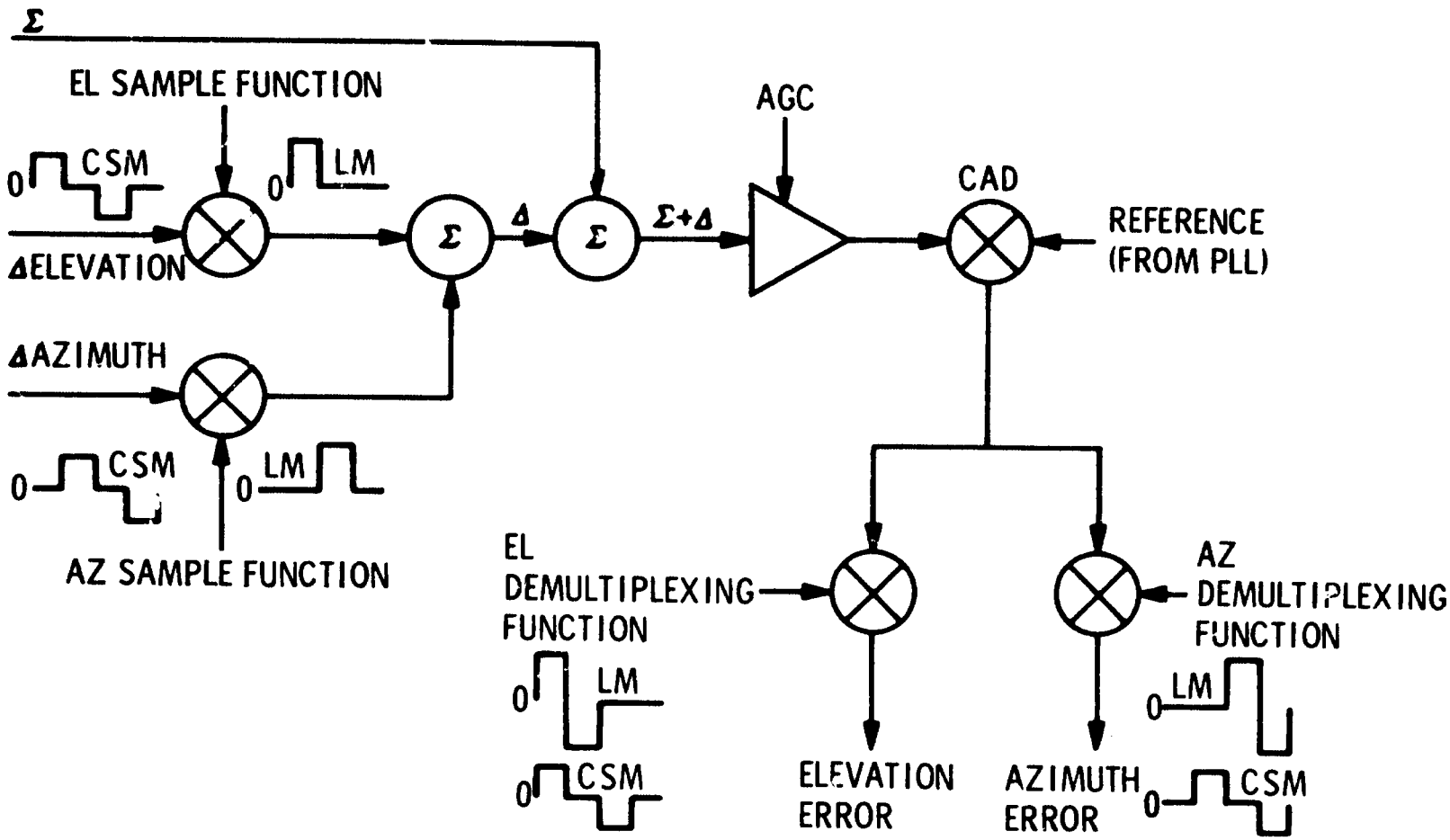
Conversion to the monopulse system provides the advantage that the antenna tracking error is proportional to the tracking angle. In the present configuration interfering signals remain in the servo loop bandwidth even when the system has no boresight error. The modified system will provide a nulling of the error signal so that even the undesired a-c components are proportional to the detector null as the system approaches boresight. This scheme is also insensitive to any incidental AM which may be transmitted by ground station. A wide band AGC loop or, as in

the case of the Apollo equipment, the video limiter provides the mechanism for removing any a-m from the incoming signal. These advantages associated with the use of most of the existing equipment can provide the antenna tracking service within the constraints of the Apollo missions. The objective of determining a system configuration which provides usable antenna tracking signals, and the analysis of this mechanization of a monopulse scheme are detailed in the succeeding paragraphs.

4.3.2 Mechanization for Lunar Missions

As a basis for comparison with the suggested system, the fundamental functions of the LEM and CSM antenna tracking systems are indicated in figure 4-30. The r-f signal inputs from the antenna sum-and-difference network contain the information required to determine the tracking error in the amplitude of the Δ Elevation (Δ El) and Δ Azimuth (Δ Az) signals. Each is multiplied by the appropriate sampling function so that the difference (Δ) signal is composed of alternate pulses of Δ El and Δ Az. The significant difference between the LEM and CSM implementations of this scheme is the shape of the sampling waveform. As shown in figure 4-30, the CSM employs a balanced waveform, whereas the LEM uses only a positive pulse. In either case, the function performed is to time multiplex Δ El and Δ Az. The composite signal when added to the sum (Σ) signal becomes an amplitude modulated r-f input to the receiver. The ratio of Δ energy to Σ energy is held constant by the AGC so that signal strength should not be a factor in the tracking process. The bandwidth of this AGC function is set so that the sampling a-m remains on the signal from which it can be recovered by the coherent amplitude detector (CAD). Since the initial sampling was done by orthogonal functions, the azimuth and elevation error signals can be determined by multiplying the demodulated a-m by orthogonal demultiplexing functions. The output from each detector should therefore be a dc voltage which is proportional to the pointing error. It is this output which is used to drive the antenna toward a null in the Δ signal.

4-30 EXISTING LM AND CSM ANTENNA TRACK SYSTEM



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This system has nominally been termed a single channel monopulse tracker, however, it retains the properties of a sequential lobing system because of the sampling technique. In succession, the receiver input ($\Sigma+\Delta$) contains azimuth information and then elevation information in much the same manner that a sequential lobing technique samples information in each quadrant. The only difference is that ΔAz and Δ El signals are formed by the antenna sum-and-difference network instead of by processing the pulse amplitude received from each lobe. As a result, the difficulties encountered can be attributed in part to the inherent problems of sequential lobing schemes. One of particular note is the system sensitivity to a-m other than that produced by the lobing, especially if the frequency components are near the lobing rate. That frequency components exist near the lobing rate can be determined from one of the properties of speech . This trait is the syllabic rate which can be characterized as an envelope on the speech pattern. Therefore, even though the voice channel bandwidth cuts off at 300 Hz, the frequencies and harmonics of the syllabic rate will be contained in the modulation. These are the low frequency components which will contribute heavily to the tracking error problem. This interference together with the interference defined by the previous analyses indicate some of the problems which accompany the existing mechanization for antenna tracking.

Since the large tracking excursions have been shown as an inherent difficulty encountered by the system, any solution which does not change modulation format must convert from the sequential lobing scheme to a configuration of monopulse tracking. In addition to designing a usable system, the number of changes from existing hardware must also be considered. One design which maintains the same basic configuration is shown in figure 4-32. In this scheme the ΔAz and Δ El signals are biphase modulated by a clock signal operating at about 800 KHz. The 90° phase shift in the clock line provides quadrature addition of these error terms. By shifting the composite difference signal 90°, the Δ and Σ signals can also be added orthogonally. Figure 4-31 indicates the spectrum of each prior to their addition into a single channel. Wideband AGC removes any amplitude variation which has been introduced by the quadrature summing of Σ and Δ . In the

present Apollo receivers this function is performed by a video limiter. The wide-band phase detector (WBD) then demodulates the initial modulation and the error signal from the i-f to a baseband and a subcarrier signal. The magnitudes of Δ Az and Δ El is then determined by phase detectors which use the clock as reference. Thus the proper error voltages are sensed and delivered to the antenna drive hardware. A detailed signal analysis of this system is included in the appendix.

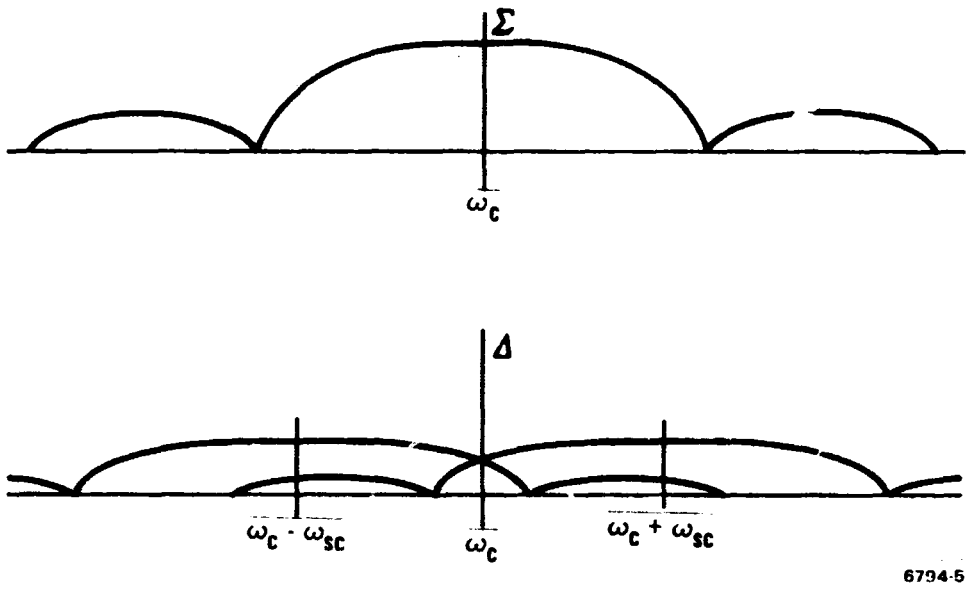
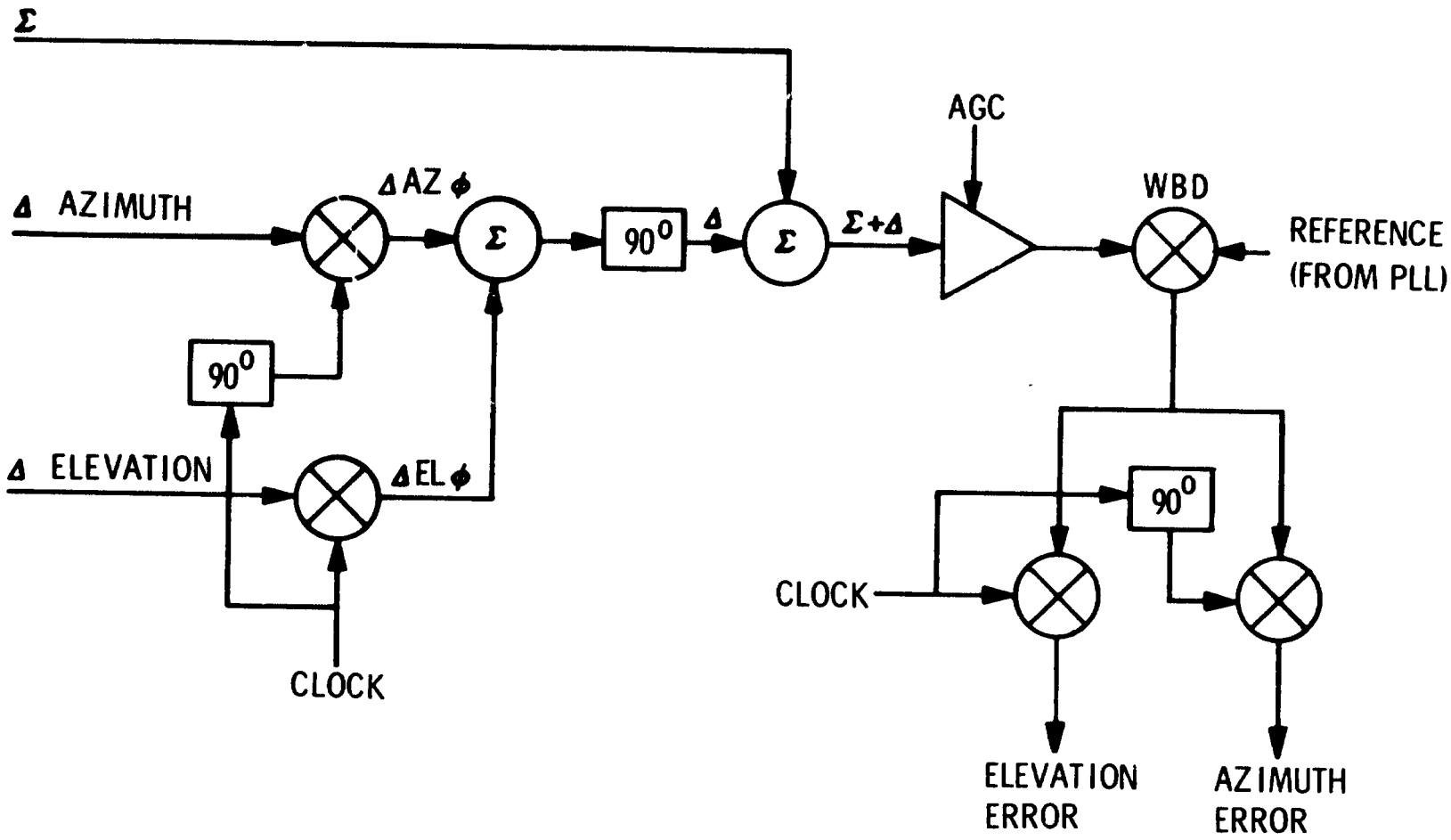


Figure 4-31. Modulation Envelopes of the Σ and Δ Signals

Selection of an appropriate oscillator frequency for the clock is important for the successful operation of this system. It must be chosen so that it falls in a region of the ranging spectrum which contains only a small amount of PRN code energy. An initial analysis indicates that a range where spectral components are 40 db below the unmodulated carrier exists near 800 KHz. This frequency falls well within the bandwidth of the exisitng wideband detector; therefore, the additional development of hardware for the transponder is not required. An additional constraint on the selection of the clock rate is the bandwidth of the error channels: 4 Hz for the LEM system and 2 Hz for the CSM system. The spectrum near the

4-32 RECOMMENDED MONOPULSE ANTENNA TRACK SYSTEM



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subcarrier frequency will appear as noise in this bandwidth. Three factors which contribute to this energy are: (1) the uplink PRN code spectrum in the region near 800 KHz, (2) the intermodulation terms between the code and the modulated subcarriers, and (3) the code spectrum near d-c. The first two of these are terms which are introduced through the Σ channel; therefore, the level is determined by the uplink modulation indices. The third results from modulating the Δ channel with the subcarrier. The level of this interference will be proportional to the amplitude of the Δ signal and is determined by the ratio of the interference near the carrier to the carrier power. A judicious choice of subcarrier frequency made by considering the spectrum of the PRN code, the intermodulation terms, and the error channel bandwdith, will provide the capability for demodulating the Δ signal without impairment from the phase modulation transmitted on the carrier.

The reduction of tracking errors can be understood by comparing the spectrum of the suggested scheme with that of the present configuration. In either the intermodulation terms between the PRN ranging spectral components and the modulated subcarriers are present. The time sampling of the Δ Az and Δ El signals by the present system causes spectral lines to occur at 50 Hz and its harmonics. Intermodulation between these components and terms of the signal spectrum easily fall within the antenna servo bandwidth. In the phase multiplexing scheme, there are no spectral lines caused by lobing, which removes this source of tracking error. Another reason that the interference can be reduced is evident when the condition of no boresight error is examined. Because of the demultiplexing function of the present system, spectral lines at 50 Hz and harmonics will still occur thereby generating interference even though no sighting error exists. The result is that the tracking error is not proportional to the angle between boresight and ground transmitter. The subcarrier of the monopulse scheme, however, will null when the angle is zero. This action will also null the interference since it is modulation on this tone. Thus the only noise remaining is the combination of thermal noise and PRN code spectral lines in the error detector bandwdith. Therefore, the suggested monopulse system decreases the tracking error in two ways: (1) by

removing the lobing spectrum, and (2) by making the interference proportional to the tracking angle.

In order to realize this reduction in error, some equipment changes will be required. The necessary modifications are restricted to the process of modulating and demodulating the Δ El and Δ Az signals. A source which operates at approximately 800 kHz is needed to provide the reference signal. This clock can be used as the subcarrier oscillator for the phase modulators and as the reference for the error detectors. The modulating function can be accomplished by switching the S-band signal phase by 180° at the 800 kHz rate, thus effectively providing a biphase modulated signal. The demodulation processing can be done by using a balanced detector which is fed from the wideband detector output of the receiver and from the clock. In order to accommodate these changes, the tracking output must be moved from the coherent amplitude detector output to the wideband detector output. Making these basic changes to the existing equipment will convert the tracking function from a sequential lobing system to monopulse implementation within the basic configuration of the present system.

4.3.3 Signal Analysis of the Recommended Monopulse System

The three signals received from the antenna sum and difference network can be written:

$$\Sigma = A_{\Sigma} \sin (w_c t + \phi)$$

$$\Delta \text{ Az} = A_{az} \sin (w_c t + \phi)$$

$$\Delta \text{ El} = A_{El} = A_{El} \sin (w_c t + \phi)$$

where ϕ denotes the total uplink modulation. The two difference signals are biphase modulated at the subcarrier rate of approximately 800 kHz. At the output of the modulators, the signal terms of interest are:

$$\Delta A_{z\phi} = A_{az} \sin (w_c t + \phi) \cos w_{sc} t$$

$$\Delta El_{\phi} = A_{El} \sin (w_c t + \phi) \sin w_{sc} t$$

Summing these two and shifting the phase by 90° yields the Δ signal:

$$\Delta = (A_{az} \cos w_{sc} t + A_{El} \sin w_{sc} t) \cos (w_c t + \phi)$$

$$\Delta = A_\Delta \cos (w_c t + \phi)$$

This composite is added to the Σ signal to form the input to the receiver:

$$\Delta + \Sigma = A_\Sigma \sin (w_c t + \phi) + A_\Delta \cos (w_c t + \phi)$$

In the receiver this signal is mixed to an i-f:

$$IF = \sqrt{A_\Sigma^2 + A_\Delta^2} \quad \cos \left(w_{if.} t + \phi - \tan^{-1} \frac{A_\Sigma}{A_\Delta}\right)$$

and then limited:

$$IF_L = A_L \cos \left(w_{if} t + \phi - \tan^{-1} \frac{A_\Sigma}{A_\Delta}\right)$$

$$= A_L \left\{ \cos \left(\tan^{-1} \frac{A_\Sigma}{A_\Delta}\right) \cos (w_{if} t + \phi) + \sin \left(\tan^{-1} \frac{A_\Sigma}{A_\Delta}\right) \sin (w_{if} t + \phi) \right\}$$

$$IF_L = \frac{A_L}{\sqrt{A^2 + A^2}} \left\{ A_\Delta \cos (w_{if} t + \phi) + A_\Sigma \sin (w_{if} t + \phi) \right\}$$

In the wideband detector, this signal is multiplied by a reference generated by the carrier phase locked loop.

$$WBD = \frac{A_L}{\sqrt{A^2 + A^2}} \left\{ A_\Delta \cos (w_{if} t + \phi) + A_\Sigma \sin (w_{if} t + \phi) \right\} A_R \cos w_{if} t$$

$$= K \left\{ A_\Delta \cos \phi + A_\Sigma \sin \phi \right\}$$

These two terms represent the tracking signal and the information signal, respectively. The tracing error is then determined in the error detector using the same reference as was used for the biphase modulator:

$$El\ Error = K^1 \left\{ A_\Delta \cos \phi + A_\Sigma \sin \phi \right\} \sin w_{sc} t$$

$$= K^1 \left\{ (A_{az} \cos w_{sc} t + A_{El} \sin w_{sc} t) \cos \phi + A_\Sigma \sin \phi \right\} \sin w_{sc} t$$

By filtering the output, the error signal is:

$$\text{El Error} = K_1 A_{El} \cos \phi$$

Similarly, the azimuth channel is:

$$A_z \text{ Error} = K_2 A_{Az} \cos \phi$$

Thus the two error voltages are proportional to the amplitude of the difference signals.

4.3.4 Conclusion

By examining the implementation of the antenna tracking function, the basic scheme has been found to be a sequential lobing configuration. The problems attendant with this system lead to the recommendation of converting to a monopulse tracker. The result would be a service which will operate within the allowable tracking errors. No change in the configuration of the transponder is required since the tracking information can be derived from the existing wideband phase detector instead of the coherent amplitude detector. The hardware modifications are restricted to the devices required to convert from a time sampling system to one which carries the information in the signal phase. Preliminary analysis of these new functions leads to the conclusion that devices exist which can be used to meet the system requirements. In order to determine how these devices should be mated to the existing hardware, a more thorough study is necessary to define the new hardware and its interfaces with existing equipment.

4.4 APOLLO TURNAROUND BASEBAND PROCESSING

4.4.1 Introduction

In the Apollo communication system, the up-link Unified S-band carrier is phase modulated by a baseband signal consisting of a linear sum of a 30 kHz f-m voice subcarrier, a 70 kHz f-m data subcarrier, and a PRN ranging code 1 megabit/second. The entire up-link baseband signal is detected and modulated on the down-link carrier along with the down-link subcarriers. As a consequence of turning around the unnecessary voice and data subcarriers:

1. The voice and data subcarriers rob power from the down-link services and ranging.

2. The up-link subcarriers suppress the ranging.

3. The transponder modulator linearity requirements are unnecessarily severe.

4. The down-link turned-around signal modulation index varies with up-link signal to noise ratio.

In addition to these, further inefficiencies can be noted because the less than optimum turnaround ranging bandwidth has the effect of suppressing the ranging signal by excess noise.

It has been known for sometime that removing the up-link subcarriers before retransmission by the transponder could bring about some system improvements. The only previously documented attempt at removing the subcarriers is given in a report entitled "Review of the Unified S-Band System Tests Contract NAS 9-2563," dated June, 1964. In this effort a 100 kHz high-pass filter, which was used, was a complete failure because the filtering created an intolerable distorting effect on the ranging.

The method recommended here to remove the subcarriers is to band-eliminate the energy in the vicinity of the subcarriers either by a direct method of band stop filters or by a modulation cancelling loop. The former has the advantage of less equipment whereas the latter eliminates high order modulation sidebands. A second recommended method of enhancement of the system performance is to low pass filter the ranging for the improved performance.

There are numerous advantages to be gained by the removal of the subcarriers and by the proper low pass filtering. Removal of the subcarriers, which have a modulation index greater than the ranging and thus use more carrier power than the ranging, will free some of this carrier power for other services. Additional improvement could be anticipated from the reduction in suppression from the sub-

carriers. With the subcarriers removed, the ranging signal can be subjected to video limiting thus maintaining the modulation index of ranging plus noise at a constant value. Precise quantitative evaluation of expected improvement has not been determined, however a substantial improvement should be expected.

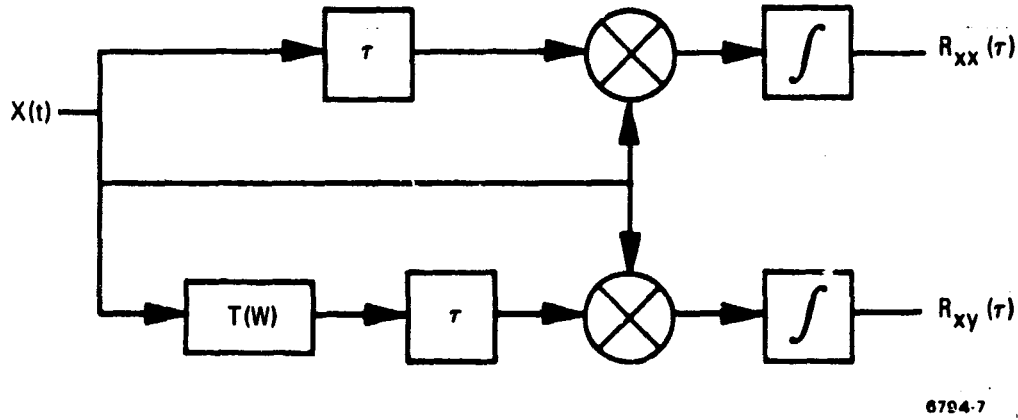
Reducing the ranging bandwidth with a low-pass filter should improve the pre-limiting S/N and reduce the concomitant suppression of the ranging, thus producing a more favorable turned-around signal. Reduction of the bandwidth also causes distortion thereby requiring an increase in S/N which will offset the improvement by filtering.

Distortion causes changes in the correlation function of the ranging which impairs the acquisition capability. A measure of the distortion is difficult to evaluate by analytical means. Essentially the impairment has been evaluated by taking the larger of either the change in the difference in correlation levels or the change in correlation levels. This information is contained in the cross correlation function. For example, if when correlated and not filter, components X and C give levels of .5 and .25 respectively; and then with filtering the levels are .4 and .16, the distortion would be the larger of .5 - .4)/.5 or (.25 - .16)/.25 or (.5 - .25) - (.4 - .16) /(.5 - .25). For the example, the distortion would be 5.5 db.

The problem considered here is to determine the effects of filtering on the ranging and to find the best bandwidth for the transmission of the ranging. First the problem of separating the up-link subcarriers from the ranging by eliminating the energy in the vicinity of the subcarriers is treated. The effect of the filters on the ranging signal will be determined. Second, the problem of low pass filtering the ranging signal will be considered. The distorting effect of the filter, and the improvement in S/N by the filter will be considered.

4.4.2 Filtering Effect on Ranging Code Correlation Function

The effect upon the ranging correlation function will be analyzed with Fourier Techniques. A diagram of the system to be evaluated is given below.



The undistorted - (unfiltered) cross correlation function (in this case auto correlation function) is designated by $R_{xx}(\tau)$ and is symbolically performed as shown in the diagram. However, the identical correlation function can be found by performing an inverse Fourier Transformation on the cross spectrum (or for R_{xx} on the self-spectral density). Thus if the spectral responses are available, then so are the correlation functions.

If the autocorrelation function is represented by $R_{xx}(\tau)$, the self-spectral density is given by

$$S_{xx}(w) = F\left[R_{xx}(\tau)\right] \tag{1}$$

where F (.) represents the Fourier Transform of the bracketed quantity. The self-spectral density can also be represented by

$$S_{xx}(w) = F\left[X(t)\right] \cdot F\left[X(t)\right]^* \tag{2}$$

$$= X(w) \cdot X(w)^*$$

where * indicates complex conjugate.

If y(t) represents the filtered ranging x(t), then

$$y(t) = \int_{-\infty}^{\infty} x(t)\, h(t - \lambda)^*\, d\lambda \tag{3}$$

or taking transforms.

$$T(w) = F\left|h(t)\right|$$

$$y(w) = F\left|y(t)\right| = x(w) \cdot T(w)$$

The Fourier Transform of the cross correlation of the filtered ranging gives the cross spectral density

$$S_{xy}(w) = F\left[R_{xy}(\tau)\right] \tag{4}$$

which is also given by

$$S_{xy}(w) = F\left[x(t)\right] \cdot F\left[y(t)\right]^*$$

$$= x(w) \cdot Y(w)^* \tag{5}$$

From (4) and (5)

$$S_{xy}(w) = x(w) \cdot x(w)^* \cdot T(w)^* \tag{6}$$

and taking an inverse transform

$$R_{xy}(\tau) = F^{-1}\left[x(w) \cdot X(w)^* \cdot T(w)^*\right]$$

or

$$R_{xy}(\tau) = F^{-1}\left[S_{xx}(w) \cdot T(w)^*\right]$$

$$R_{xy}(\tau) = F^{-1}\left[F\ R_{xx}(\tau) \cdot T(w)^*\right] \tag{7}$$

From (7) the effect of any transfer function T(w) upon the correlation function may be determined.

4.4.2.1 Ranging Model

A model of the ranging code was developed which had some of the attributes of the Mark 1 ranging code although not as long. The model is a composite code having a length of 506 bits. The Mark 1 code is also a composite code but is over 5 million bits in length. The code is made up of a clock, an 11 bit PN sequence (L) and a 23 bit PN sequence (M) which are combined by module-two addition, ie:

$$X = CL \oplus (LM) \tag{1}$$

Part of the auto correlation function (R_{xx}) for this code is shown in figure 4-33. This code has about the same correlation levels as the Mark 1. The effect of filtering upon this code will be investigated.

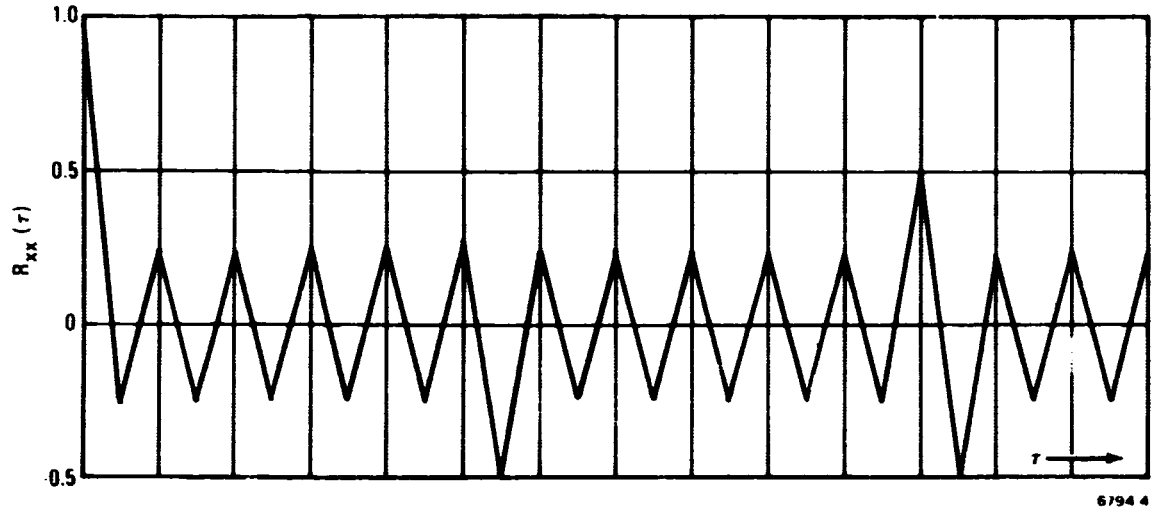


Figure 4-33. Ranging Code Autocorrelation Function

4.4.3 Removing Up-Link Subcarriers

The up-link subcarriers and ranging are transmitted by being summed and then phase modulated on the up-link carrier. After detection in the transponder, the ranging and up-link subcarriers are summed with the down-link subcarriers, and the composite signal is modulated on the down-link carrier for transmission to earth. Some of the penalities incurred from this method are:

1. The up-link subcarriers waste some of the transmitter power since they are transmitted along with the ranging on the down-link.
2. The subcarriers cause suppression of the ranging.
3. Video limiting cannot be used so the modulation index is not constant and the other down-link services are robbed of power when the transponder signal to noise ratio is small.

It has been known for sometime that the system could be improved by the removal of the up-link subcarriers. The only previously documented attempt to remove the subcarriers was when a 100 kHz high pass filter was used with no

success. The method recommended here is to either use band stop filters or to use a modulation cancelling loop. The analysis shows the effect on the ranging code to be less than 1/2 db.

4.4.3.1 Band Stop Filtering

The effect of the filtering upon the ranging code cross correlation function was evaluated with the greatest emphasis placed upon the effect on the acquisition properties: Equation (7) of paragraph 4.4.2 gives the expression for the cross correlation function after filtering.

$$R_{xy}(\tau) = F^{-1}\left[F\ \left|R_{xx}(\tau)\right|\quad T(w)^{*}\right] \tag{1}$$

The filter function T(w) is the expression for the complex transfer function of the band stop filters.

A prototype low pass 3 pole Thompson was used to develop the band stop filters needed. The transfer function for the low pass prototype filter is:

$$T(w_i) = \frac{3}{(3 - W^2/wo^2) + j\ (3w/w_o)} \tag{2}$$

Then applying a banp stop transformation

$$w_1 = \frac{1}{a(w_2 + \frac{1}{w_2})} \tag{3}$$

where a is the percent bandwidth. The transfer function is normalized for unity delay. The transfer function used for filtering was the product of two transfer functions. The first was a 30 kHz center frequency 30 percent bandwidth band stop filter and the second was a 70 kHz center frequency 30 percent bandwidth band stop filter.

Applying these filter transforms to the correlation function shown in figure 4-33, through the use of equation (7) in paragraph 4.4.2, results in the cross correlation function of the filtered ranging signal. Comparison of the cross correlation function with the undistorted version at all points reveals a maximum degradation of 0.5 db.

There are two approaches to filter the up-link subcarriers from the ranging. One way is to use band stop filters as shown in figure 4-34.

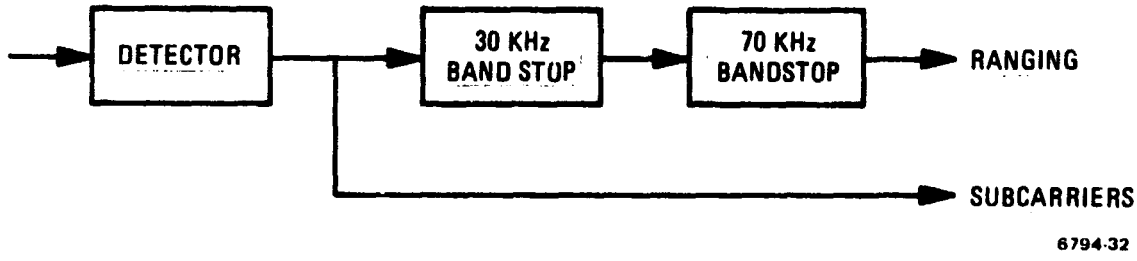


Figure 4-34. Band-Shop Filter

The second method employs a feedback modulation cancelling loop as shown in figure 4-35. In this scheme, bandpass filters allow only the subcarriers to be returned out of phase to cancel the subcarrier modulation before detection.

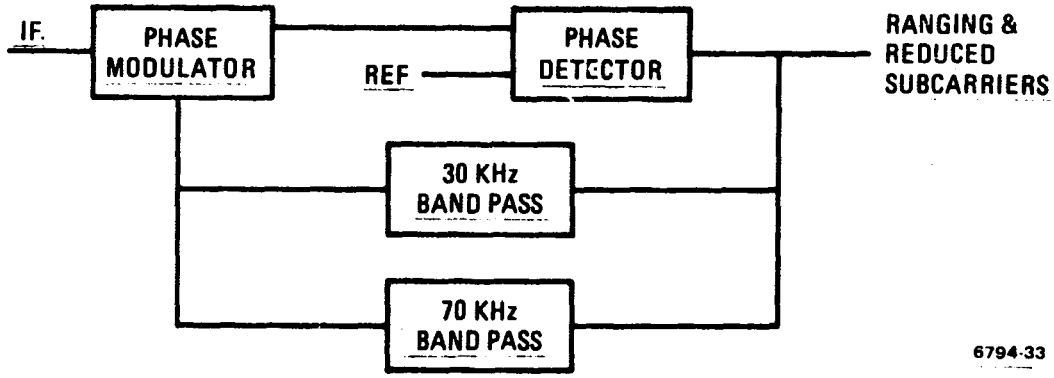


Figure 4-35. Feedback Modulation Cancelling Loop Filter

The second method provides a better way of removing the subcarriers since it removes all sidebands of the subcarriers as well as the energy in the vicinity of the carrier. The first method, however, is much simpler to implement and will reduce the subcarrier power substantially. Both techniques affect the ranging only by the amount of 1/2 db of distortion. The additional delay caused by the filters was not measurable.

4.4.4 Low Pass Filtering the Ranging

The ranging signal at the transponder is generally contaminated by thermal noise which has the effect of causing suppression of the ranging by the limiter. If the bandwidth is too large, the ranging is suppressed more than necessary, and the amount of ranging power available for down link transmission is less than maximum. As the bandwidth is reduced, the pre-limiting signal to noise ratio will increase, reaching a maximum in the vicinity of zero bandwidth. Reducing the bandwidth, however, introduces distortion which will offset any further improvements in S/N. This point of diminishing return would be expected to have a dependence on pre-limiting S/N and generally would be different for each set of conditions.

The approach taken here to ascertain the band limiting effect is to first evaluate the distortion penalty caused by the band limiting, then determine the improvement in the signal power after limiting. The best bandwidth to use is then determined by finding the maximum value of the ratio of signal power increase to distortion penalty (B). The function B is calculated for various filters in terms of the filter noise bandwidth and will be presented with S/N as a parameter.

4.4.4.1 Distortion From Band Limiting

The effect of band limiting on the ranging correlation function is determined in the same manner as before. The 506 bit ranging code is used to generate an auto-correlation function $R_{xx}(\tau)$ as shown in figure 4-33. The cross correlation $R_{xy}(\tau)$ between the band limited code and undistorted code is then found using the expression given by equation (7) of paragraph 4.4.2.

$$R_{xy}(\tau) = F^{-1}\left[F\left[R_{xx}(\tau)\right] \quad T(w)^{*}\right]$$

where F and F^{-1} represent the Fourier and inverse Fourier transforms respectively, and T(w) is the filter transfer function.

Four different filters were arbitrarily chosen to be used for the band limiting; an RC low pass, a 1/2 db ripple Chebyshev 5 pole, a 1/2 db ripple Chebyshev 3 pole, and a Thompson 3 pole.

The distortion was evaluated by calculating the cross correlation function and comparing with the undistorted correlation function in the manner which was described earlier. Plots of distortion as a function of the noise bandwidth of several of the various filters are given in figure 4-36.

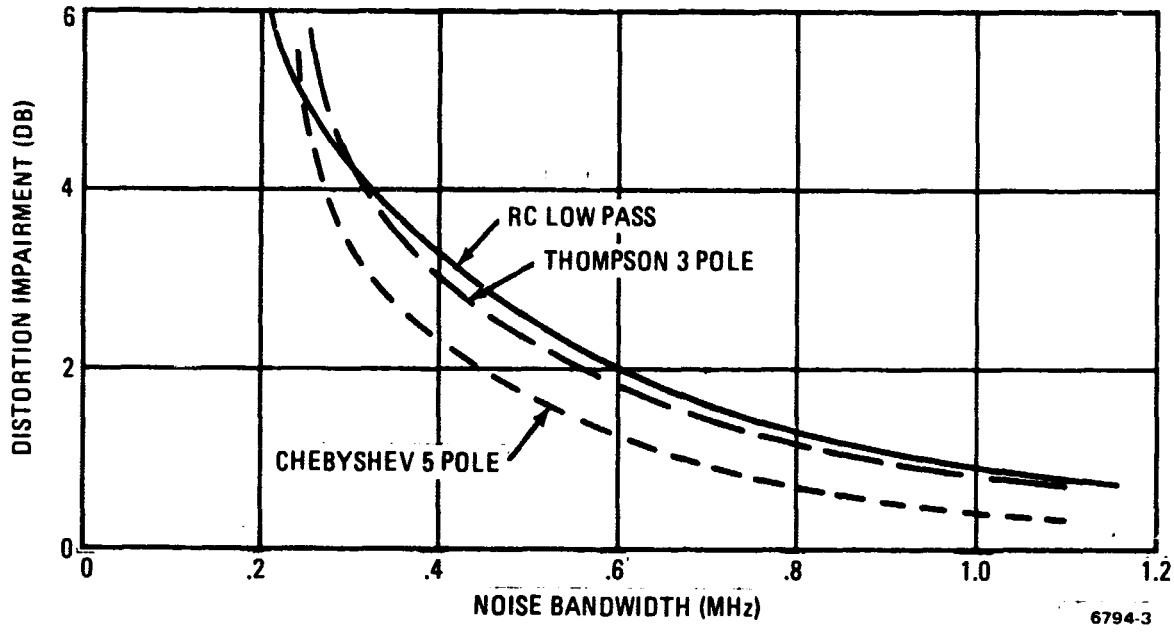


Figure 4-36. Filter Distortion

4.4.4.2 Signal Improvement From Band Limiting

Band limiting should improve the pre-limiting signal to noise ratio, and concomitantly reduce the noise suppression of the signal due to the amplitude limiter. The suppression factor (α^2) is approximately

$$\alpha^2 = \frac{1}{1 + \frac{4 B_N \alpha}{\pi S_T \varphi(B_N)}} \qquad (4)$$

where B_N is the filter noise bandwidth, α is the noise power density, S_T is the total signal power, and $\varphi(B_N)$ is the signal power reduction factor from band limiting. The minimum suppression takes places in the vicinity of $B_N = 0$.

$$\alpha_o^2 = \frac{1}{1 + \frac{4}{\pi}\frac{\alpha_o}{S_o}} \tag{5}$$

The increase in signal power suppression with increasing bandwidth is given by:

$$\frac{\alpha_s^2}{\alpha_o^2} = \frac{1 + \frac{4}{\pi}\frac{\alpha_o}{S_o}}{1 + \frac{4}{\pi} S_T \frac{B_N \alpha}{\varphi(B_N)}} \tag{6}$$

The term $\varphi(B_N)$ is evaluated by calculating the normalized autocorrelation function $R_{xx}(\tau)$ of the filtered ranging and evaluating at zero delay.

$$\varphi(B_N) = R_{yy}(o) \tag{7}$$

The function α_s^2 for the 5 pole, 1/2 db ripple, Chebyshev filter is given in figure 4-37 below. The S/N that is specified on the graph is defined as the ratio of the total signal power to the noise power in a 1 MHz bandwidth.

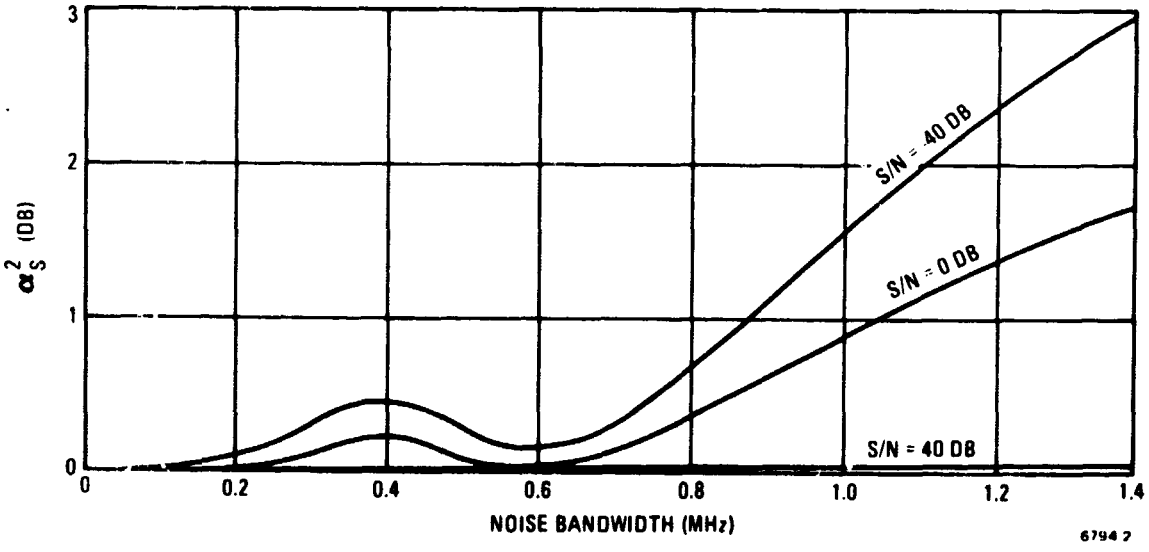


Figure 4-37. α_s^2 for 5 Pole, 1/2.db Ripple, Chebyshev Filter

4.4.4.3 Optimum Bandwidth

The optimum for the turn around ranging can now be found since the effect of the low pass filter on the distortion and on the signal suppression have been identified. The optimum bandwidth will occur at the maximum of the (suppression - distortion) relation. Defining this as the useful signal power (B):

$$B = \alpha_s^2 \text{ (db)} - \text{dist. (db)}$$

Curves of B versus Noise Bandwidth are shown in figure 4-38 for the four filters. The S/N given is ratio of the total signal power to noise power in a 1 MHz Band.

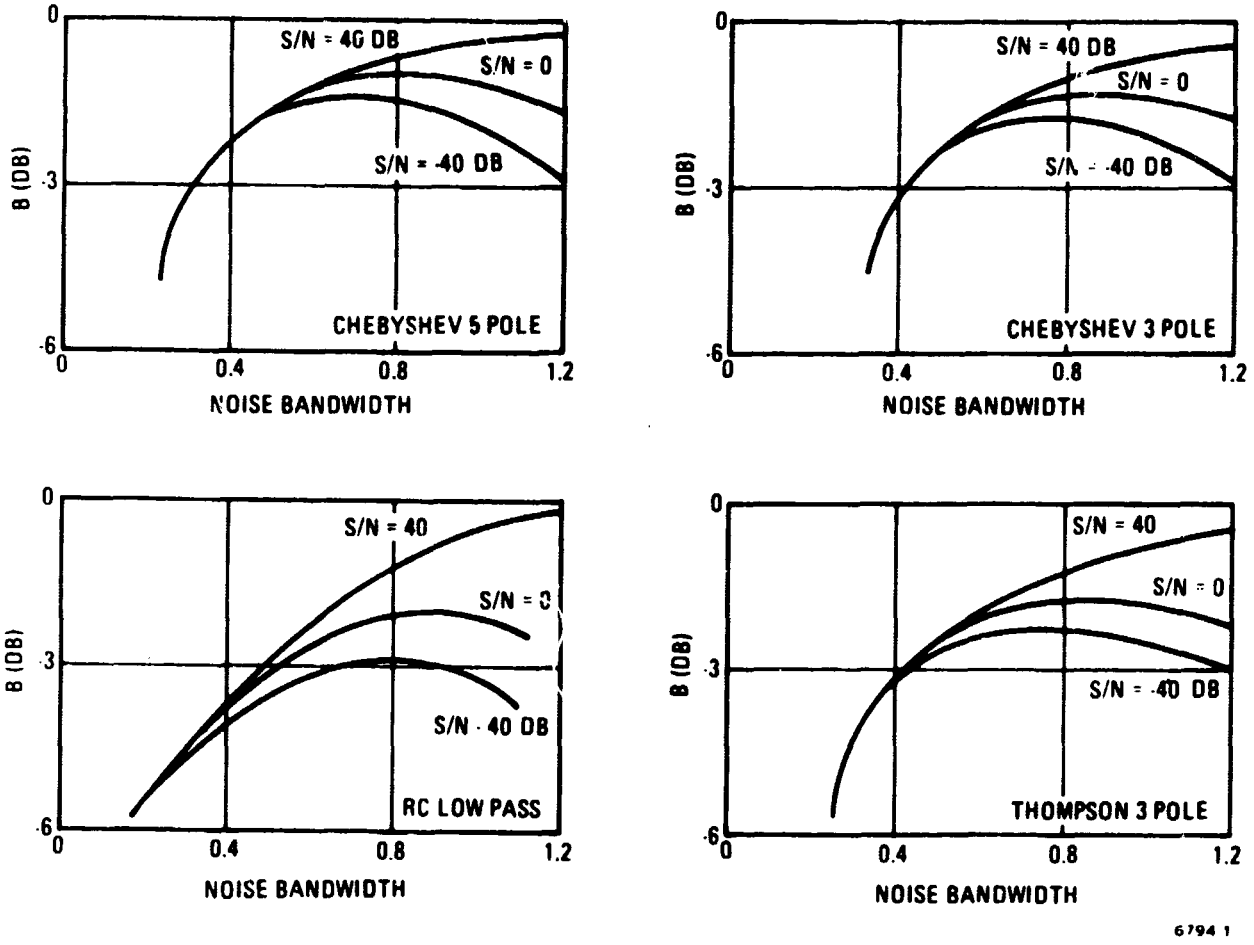


Figure 4-38. B vs Noise Bandwidth.

The 5 pole Chebyshev appears to give the best ranging performance of the filters considered. The best noise bandwidth for the case of large noise/signal ratios occurs at 700 KHz. This filter offers about 2 db better performance than the 1.5 MHz low pass now implemented in a Block II Transponder for low S/N ratios. The three pole Chebyshev offers almost the same improvement and will not increase the delay as much.

4.4.5 Summary

Removal of the up-link subcarriers from the turned around baseband by band rejection filtering in the vicinity of the subcarriers can bring about significant improvements in the present Apollo system without severely impairing the ranging. Removing the subcarriers allows: (1) the use of video limiting, thus maintaining a constant modulation index; (2) the release of power which had been necessary to transmit the subcarriers; (3) the elimination of suppression of the ranging; and (4) the reduction of linearity constraints on the system. After removal of the subcarriers, a further improvement in the ranging is possible by proper low pass filtering. A 5 pole Chebyshev low pass with a noise bandwidth of 700 kHz will improve the ranging signal by 2 db over the present system.

SECTION V
RELIABILITY

5. INTRODUCTION

This section describes reliability studies conducted during the Advanced S-Band Transponder study program. Since the purpose of the program was to investigate a general purpose, state of the art, transponder with no definite specifications, a maximum ambient temperature had to be assumed for the purpose of performing a reliability estimate.

The report is divided into four subsections. In the first, results of the stress analysis and reliability estimate are discussed and a comparison made with that of the present USBE Transponder. The estimated failure rate of the USBE Transponder was 3.05%/1000 hours; that of the advanced transponder, 2.73%/1000 hours. The second subject discussed is redundancy, active and standby, and the advantages of each as applied to the driver, PA and X2 multiplier modules of the transmitter. Military ER (Established Reliability) Specifications were the basis for the general parts procurement policy which is presented in the third subsection. In the last subsection, Failure Mode and Effect, Stress, and Computer Circuit Tolerance Analyses are discussed with respect to the future development of a hi-rel transponder.

Two areas in the report that are inconclusive and suggest additional investigation in order to obtain more accurate reliability estimates are:

1. What multiplying factors should be applied to semiconductors with junction temperatures exceeding the 80-90°C range?
   The multiplying factors used in this report (assigned by Collins Radio to the USBE Transponder) resulted in the semiconductors accounting for over 75 percent of the failure rate assigned to the transmitter, which is higher than experience indicates.

2. What are the junction temperature rises above case of the TRW 6694 power transistors used in the driver and PA modules of the transmitter? These temperatures are usually estimated by multiplying the device power dissipation by the thermal resistance (^{o}C/watt) rating of the device. For most semiconductor device types, Motorola's measurements of thermal resistance agree with the vendor's. However, on these particular devices, correlation with the vendor has been unsuccessful to date.

5.1 RELIABILITY ESTIMATE

5.1.1 Failure Rate Calculations

The failure rate, λ, for the advanced S-Band Transponder was estimated to be 2.733201%/1000 hours. The reliability logic diagram and modular failure rates are shown in Figure 5-1, while the failure rates assigned to the individual parts are summarized in Tables 5-1a through 5-1c.

The failure rate for the present USBE Transponder and the associated power amplifier developed for the Apollo Block II program was estimated to be 3.053347%/1000 hours. The reliability logic and failure rates for the USBE Transponder are shown in Figure 5-2. Failure rates for the receiver, transmitter and associated power supply modules of the transponder were obtained from the "Reliability Prediction and Apportionment Report for the Apollo USBE Block II Program", prepared by Motorola. Failure rates for the attenuator, TWT and associated power supply of the power amplifier were obtained from Collins Radio Company.

The following assumptions were used in preparing the failure rate for the Advanced S-Band Transponder.

1. The transponder failure rate is constant.
2. All parts are considered in series and, as such, any part failure will cause failure of the system.
3. Failure rates assigned to the individual parts were those used for the USBE Transponder Reliability Estimate and were initially determined by Collins Radio. These failure rates are detailed in Tables 5-2a through 5-2e.

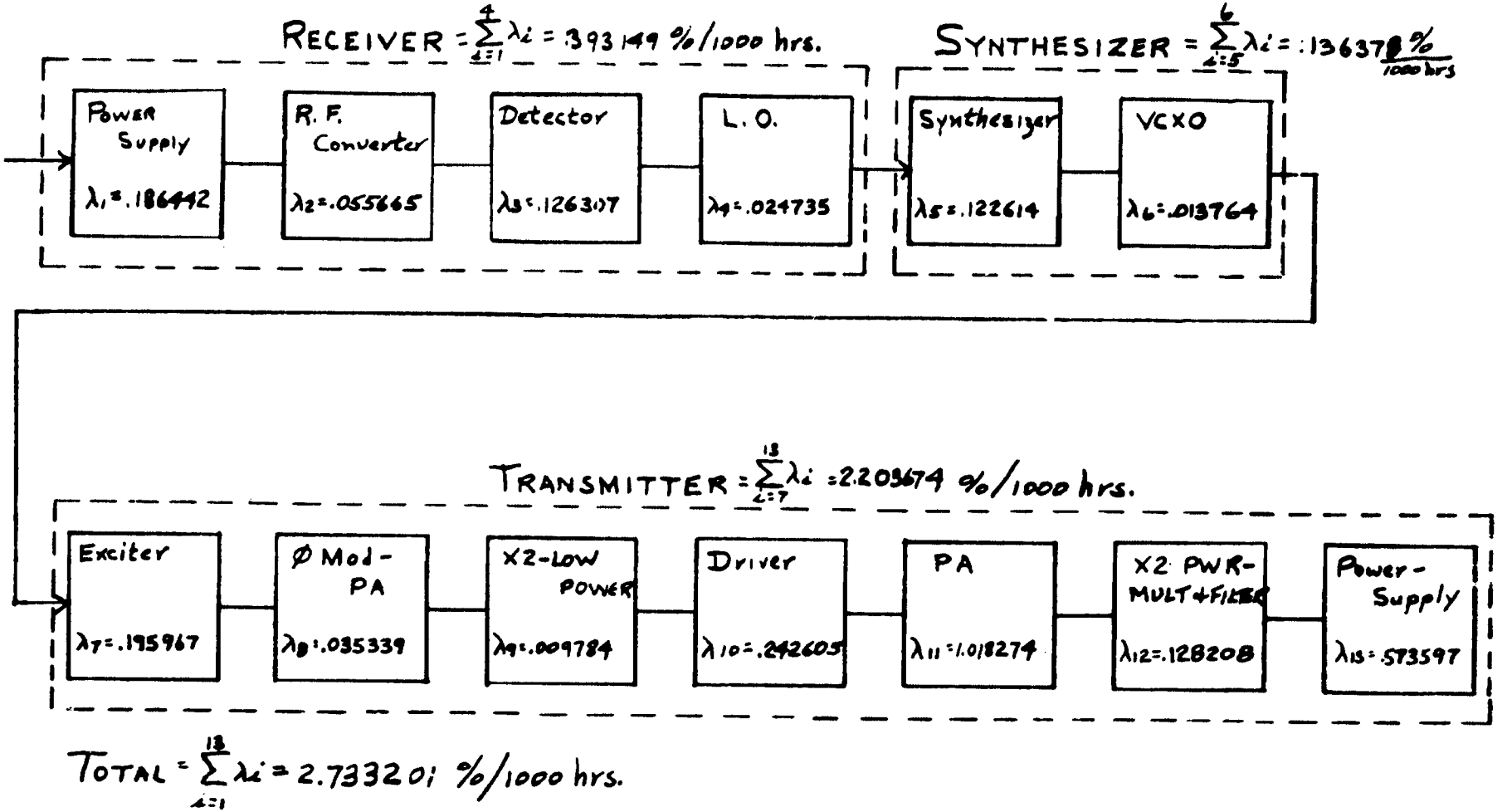
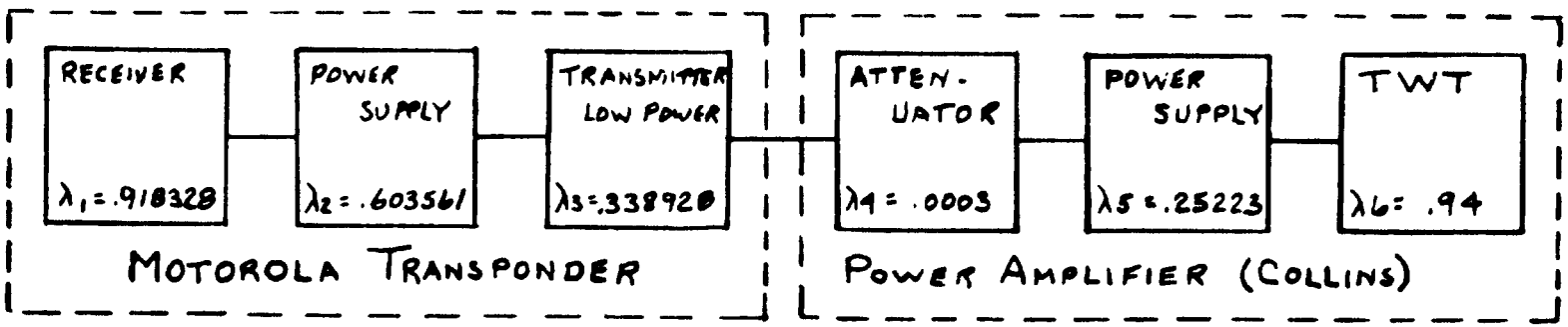


Figure 5-1. RELIABILITY LOGIC DIAGRAM for the ADVANCED S-BAND TRANSPONDER



TOTAL FAILURE RATE = $\lambda_1 + \lambda_2 + \ldots \lambda_6$ = 3.053347 %/1000 hrs

Figure 5-2.

RELIABILITY LOGIC DIAGRAM FOR THE USBE TRANSPONDER (PM MODE - NO TLM) AND ASSOCIATED POWER AMPLIFIER

Table 5-1A

FAILURE RATE APPORTIONMENT

PART TYPE	Stress Level, 55°C Amb.	Failure Rate, λ Z/1000 hr		RECEIVER R.F. CONVERTER	RECEIVER DETECTOR	RECEIVER L.O.	RECEIVER POWER SUPPLY	SYNTHESIZER SYNTHESIZER	SYNTHESIZER V.C.X.O.
Diode, Signal ΔTjc 5°C	Tj=60°	.000114	N				5	1	
			λ				.00057	.000114	
Diode, Signal Δ Tjc 10°	Tj=65°	.000135	N		8	2	1		
			λ		.00108	.00027	.000135		
Diode, Zener ΔTjc 20°C	Tj=75°	.0036	N	1					
			λ	.0036					
Diode, (Volt.Var.Cap) ΔTjc 5°C	Tj=60°	.000228	N						2
			λ						.000456
Diode, Power ΔTjc 5°C	Tj=60°	.0057	N				1		
			λ				.0057		
Diode, Power ΔTjc 10°C	Tj=65°	.00675	N				1		
			λ				.00675		
Diode, Power ΔTjc 15°C	Tj=70°	.0075	N				2		
			λ				.015		
Diode, Power ΔTjc 25°C	Tj=80°	.0135	N				2		
			λ				.027		
Diode, Zener ΔTjc 5°C	Tj=60°	.00228	N				3		
			λ				.00684		
Diode, Zener ΔTjc 25°C	Tj=80°	.0054	N				1		
			λ				.0054		
Transistor,Sig.ΔTjc 5°C	Tj=60°	.00008	N		9		4	1	1
			λ		.00072		.00032	.00008	.00008
Transistor,Sig.ΔTjc 10°	Tj=65°	.0000945	N		6	3	2	1	
			λ		.000567	.000284	.00019	.000095	
Transistor,Sig.ΔTjc 1..	Tj=70°	.000105	N			1			
			λ			.000105			
Transistor,Sig.ΔTjc 20°	Tj=75°	.000126	N			2	1		
			λ			.000252	.000126		
Transistor,Sig.ΔTjc 25°	Tj=80°	.000189	N	7					
			λ	.001323					
Transistor,Sig.ΔTjc 30°	Tj=85°	.000266	N				1		2
			λ				.000266		.000532
Transistor,Sig.ΔTjc 35°	Tj=90°	.000357	N	1	3				
			λ	.000357	.001071				
Transistor Mod Pwr ΔTjc 15°	Tj=70°	.0015	N				1		
			λ				.0015		
Transistor Pwr ΔTjc 5°	Tj=60°	.00684	N				1		
			λ				.00684		
Hybrid I.C. Filter ΔT 5°C	Tj=60°	.002822	N	1					
			λ	.002822					
Hybrid I.C. AGC ΔT 5°C	Tj=60°	.001506	N	4					
			λ	.006024					
Hybrid I.C. I.F. Amp ΔT 5°C	Tj=60°	.00147	N	4	2				
			λ	.00588	.00294				
Hybrid I.C. Limiter Amp ΔT 10°C	Tj=65°	.001088	N		3				
			λ		.003264				

Table 5-1A (cont)

FAILURE RATE APPORTIONMENT

PART TYPE	Stress Level 55°C Amb	Failure Rate, λ %/1000hr		RECEIVER R.F. CONVERTER	RECEIVER DETECTOR	RECEIVER L.O.	RECEIVER POWER SUPPLY	SYNTHESIZER SYNTHESIZER	SYNTHESIZER V.C.X.O.
Monolithic I.C. RA909 ΔT 5°C	Tj=60°C	.000719	N		1				
			λ		.000719				
MC1201 ΔT 30°C	Tj=85°C	.003015	N					1	
			λ					.003015	
MC1204 ΔT 25°C	Tj=80°C	.002295	N					2	
			λ					.00459	
MC1210 ΔT 30°C	Tj=85°C	.004167	N					3	
			λ					.012501	
MC1213 ΔT 35°C	Tj=90°C	.005916	N		1			16	
			λ		.005916			.093656	
MC1709 ΔT 10°C	Tj=65°C	.00113	N			2			
			λ			.00226			
MC1533 ΔT 20°C	Tj=75°C	.001608	N						1
			λ						.001608
Resistor, Comp Tc <70°C	Pd<20%	.000052	N	20	63	34	12	14	20
			λ	.00104	.003276	.001768	.000624	.000728	.00104
Resistor, Comp Tc <80°C	Pd<40%	.000064	N				1		
			λ				.000064		
Resistor, Film Tc <70°C	Pd<20%	.00013	N	3		2	8		
			λ	.00039		.00026	.00104		
Resistor, Thermal Tc<70°C	Pd<20%	.013	N	1					
			λ	.013					
Capacitor, Ceramic/Mica	V<20%	.000032	N	9	48	30	7	11	15
			λ	.000029	.00154	.000096	.000021	.000035	.000048
Capacitor, Ceramic/Mica	V<40%	.000064	N				3		
			λ				.000192		
Capacitor, Ceramic/Mica	V<60%	.00032	N				2		
			λ				.00064		
Capacitor, Solid Tant.	V<60%	.00192	N			2	1		
			λ			.00384	.00192		
Capacitor, Tant. Foil	V<40%	.000048	N				8		
			λ				.000384		
Capacitor, Tant. Foil	V<60%	.00024	N				3		
			λ				.00072		
Transformer Pwr ΔT 5°C	T60°C	.042	N				1		
			λ				.042		
Transformer Pwr ΔT 25°C	T80°C	.051	N				1		
			λ				.051		
Chokes, Iron Core ΔT 15°C	T70°C	.0014	N	2	14	10	8	5	6
			λ	.0028	.0196	.014	.0112	.007	.0084
Chokes Air Core ΔT 15°C	T70°C	.00028	N	10					
			λ	.0028					
Transformer RF ΔT 15°C	T70°C	.014	N	1	6				
			λ	.014	.084				
Crystal		.001	N		2	1			1
			λ		.002	.001			.001
Connector R.F.		.0002	N	8	5	3		4	3
			λ	.0016	.001	.0006		.0008	.0006
Total, %/1000 hours				.055665	.126307	.024735	.186442	.122614	.013764

Table 5-1B

Transmitter (except Power Supply)

FAILURE RATE APPORTIONMENT

PART TYPE	Stress Level 68°C Amb	Failure Rate, λ %/1000hr		X2 LOW POWER	DRIVER	PA (2 MODULES)	Y2 HIGH POWER	EXCITER	2 MODULATOR P.A.	
Diode, Varactor ΔTjc 12°C	Tj=80°	.0054	N	1					4	
			λ	.0054					.0216	
Diode, Varactor ΔTjc 32°C	Tj=100°	.02	N					1		
			λ					.02		
Diode, Varactor ΔTjc 44°C	Tj<115°	.06	N				2			
			λ				.12			
Diode, Zener ΔTjc 5°C	Tj<75°	.0036	N	1			2			
			λ	.0036			.0072			
			N							
			λ							
Transistor, Signal ΔTjc 24°C	Tj<95°	000525	N					1		
			λ					000525		
Transistor, Med Pwr ΔTjc 32°C	Tj=100	.01	N					1	1	
			λ					.01	.01	
Transistor, Med Pwr ΔTjc 50°C	Tj<118	.042	N					1		
			λ					.042		
Transistor, Power ΔTjc 28°C	Tj<100	.06	N		1					
			λ		.06					
Transistor, Power ΔTjc 34°C	Tj<105	.09	N		2					
			λ		.18					
Transistor, Power ΔTjc 51°C	Tj<120	.252	N			4				
			λ			1.008				
Resistor, Comp Tc <80°C	Pd<20%	000064	N	1	3	4	2	8	4	
			λ	000064	000192	000256	000128	000512	000256	
Resistor, Comp Tc <85°C	Pd<30%	000084	N					3	2	
			λ					000252	000168	
Resistor, Film Tc <80°C	Pd<15%	.00016	N	2	3	4	3			
			λ	.00032	.00048	.00064	.00048			
Capacitor, Ceramic	V<20%	000044	N		3	4		6	3	
			λ		000132	000176		000264	000132	
Capacitor Solid Tant.	V<60%	.0032	N			2				
			λ			.0064				
Capacitor, Glass, Fxd & Variable	V<10%	000009	N					12	2	
			λ					000108	000018	
Coils, Transformers RF ΔT 10°C	T<80%	.017	N					7		
			λ					.119		
Connectors RF		.0002	N	2	2	4	2	2	3	
			λ	.0004	.0004	.0008	.0004	.0004	.0006	
Chokes, Air Core ΔT 20°C	T<90°	.00054	N		3	4		6	5	
			λ		.00162	.00216		.00324	.0027	
Total, %/1000 hours				009784	242605		128208	195967	035339	

1.018274

Table 5-1C

Power Supply for Transmitter

FAILURE RATE APPORTIONMENT

PART TYPE	Stress Level 60°C	Failure Rate, λ %/1000hr		POWER SUPPLY (TRANS)
Diode, Signal ΔTjc 5°C	Tj=65°	.00135	N	7
			λ	.00945
Diode, Rectifier ΔTjc 5°C	Tj=65°	.00405	N	6
			λ	.0243
Diode, Rectifier ΔTjc 10°C	Tj=70°	.0045	N	5
			λ	.0225
Diode, Rectifier ΔTjc 15°C	Tj=75°	.0054	N	1
			λ	.0054
Diode, Rectifier ΔTjc 20°C	Tj=80°	.0081	N	14
			λ	.1134
Diode, Rectifier ΔTjc 25°C	Tj=85°	.0114	N	4
			λ	.0456
Diode, Zener ΔTjc 5°C	Tj=65°	.0027	N	2
			λ	.0054
Transistor, Sig ΔTjc 5°C	Tj=65°	.00094	N	6
			λ	.00567
Transistor, Signal ΔTjc 10°C	Tj=70°	.00105	N	3
			λ	.00315
Transistor, Med. Pwr. ΔTjc 5°C	Tj=65°	.00135	N	4
			λ	.0054
Transistor, Med. Pwr. ΔTjc 15°C	Tj=75°	.0018	N	2
			λ	.0036
Transistor, Med. Pwr. ΔTjc 20°C	Tj=80°	.0027	N	2
			λ	.0054
Transistor, Med. Pwr. ΔTjc 25°C	Tj=85°	.0038	N	1
			λ	.0038
Transistor, Pwr ΔTjc 15°C	Tj=75°	.0108	N	5
			λ	.054
Transistor, Pwr ΔTjc 30°C	Tj=95°	.045	N	1
			λ	.045
Capacitor, Tant. Solid	V <20%	.00024	N	1
			λ	.00024
Capacitor, Tant. Solid	V <40%	.00048	N	2
			λ	.00096
Capacitor, Tant. Solid	V <60%	.00192	N	2
			λ	.00384
Capacitor, Tant Foil	V <40%	.00048	N	2
			λ	.00096
Capacitor, Tant Foil	V <60%	.00024	N	17
			λ	.00408
Capacitor, Tant Foil	V <80%	.00096	N	2
			λ	.00192
Capacitor, Ceramic	V <20%	.000032	N	8
			λ	.00026
Capacitor, Ceramic	V <40%	.00064	N	1
			λ	.00064

Table 5-1C (cont)

Power Supply for Transmitter

FAILURE RATE APPORTIONMENT

PART TYPE	Stress Level 60°C	Failure Rate, λ #/1000 hr		POWER SUPPLY TRANSMITTER
Resistor Comp Tc <70°C	Pd<20%	.000052	N	25
			λ	.0013
Resistor Comp Tc <85°C	Pd<40%	.000084	N	5
			λ	00042
Resistor Film Tc <70°C	Pd<20%	.00013	N	8
			λ	00104
Transformer Pwr <10°C Rise	Tc=70°	.042	N	5
			λ	.210
Chokes, Iron Core < 10°C Rise	Tc=70°	.0014	N	10
			λ	.014
Assume 10 operate Relay 10 ns per hour		.0002	N	1
			λ	.0002
				.573597

Table 5-2A. Predicted Failure Rates in %/1000 Hours for Inductive Devices (Class S or Grade B)

Part Type	Body Temperature in °C			
	56-70	71-80	81-85	86-90
RF Chokes				
Powdered Iron Chokes	.0014	.0017	.0022	.0027
Other than Powdered Iron	.00028	.00034	.00044	.00054
I-F/R-F Coils	.014	.017	.022	.027
Transformers				
I-F/R-F	.014	.017	.022	.027
Audio	.014	.017	.022	.027
Power	.042	.051	.066	.081

Table 5-2B. Predicted Failure Rates in %/1000 hours for Resistors

Part Type	Body Temperature in °C			
	61-70	71-80	81-85	86-90
Carbon Composition	.000052	.000064	.000084	.00092
Carbon & Metal Film	.00013	.00016	.00021	.00023
Thermistor	.013	.016	.021	.023

Table 5-2C. Predicted Failure Rates in %/1000 hours for Semiconductors

Junction Temperature in °C	Part Type						
	Transistor (Silicon)			Diode (Silicon)			
	Signal <1 w	Med Pwr <10 w	Power >10 w	Signal	Power	Zener, Varac.	Rectifier
51 - 60	.00008	.00114	.00684	.000114	.0057	.00228	.00342
61 - 65	.0000945	.00135	.0081	.000135	.00675	.0027	.00405
66 - 70	.000105	.0015	.009	.00015	.0075	.003	.0045
71 - 75	.000126	.0018	.0108	.00018	.009	.0036	.0054
76 - 80	.000189	.0027	.0162	.00027	.0135	.0054	.0081
81 - 85	.000266	.0038	.0228	.00038	.019	.0076	.0114
86 - 90	.000357	.0051	.0306	.00051	.0255	.0102	.0153
91 - 95	.000525	.0075	.045	.00075	.0375	.015	.0225
96 - 100	.0007	.01	.06	.001	.05	.02	.03
101 - 105	.00105	.015	.09	.0015	.075	.03	.045
106 - 110	.0014	.02	.12	.002	.10	.04	.06
111 - 115	.0021	.030	.18	.003	.15	.06	.09
116 - 120	.00294	.042	.252	.0042	.210	.084	.126

Integrated Circuits

Monolithic:

a. Transistors and diodes: assign a failure rate 1/3 that of a discrete signal transistor or diode at the appropriate temperature stress.

b. Capacitors and Resistors: asssign a failure rate of a diode as described in (a) above.

Hybrid:

a. Transistors and diodes: assign a failure rate of a discrete signal transistor or diode at the appropriate temperature stress.

Table 5-2C. Predicted Failure Rates in %/1000 hours for Semiconductors (cont)

b. Silicon Dioxide Capacitor Chips: assign a failure rate of a glass capacitor at the appropriate voltage and temperature stress.

c. Ceramic Capacitor Chips: assign a failure rate of a discrete ceramic capacitor at the appropriate voltage and temperature stress.

d. Resistor chips: assign a failure rate of a discrete film resistor at the appropriate temperature stress.

Table 5-2D. Predicted Failure Rates in %/1000 Hours for Capacitance

Part Type	% of Rated Voltage	Body Temperature in °C	
		51-60	66-70
Tantalum, Foil	40	.000048	.00008
	60	.00024	.0004
	80	.00096	.0016
Tantalum, Solid	20	.000024	.00004
	40	.00048	.0008
	60	.00192	.0032
Glass, Fxd. & Variable	20	.00000064	.0000009
Ceramic & Mica	20	.0000032	.0000044
	40	.000064	.000088
	60	.00032	.00044

Table 5-2E. Predicted Failure Rates in %/1000 Hours for Miscellaneous Parts

Part Type	Failure Rate (%/1000 Hours)
Crystal	0.001
Relay	0.0002%/10,000 operations
Connector	0.0001 + 0.00005 per pin
TWT	0.94

4. The exception to (3) above, was IC's (integrated circuits). No failure rates had been assigned to IC's by Collins; consequently, the following general rules were used: for hybrid circuits, the chips were treated as discrete parts; for monolithic circuits, the resistors and capacitors were considered as diodes, and diodes and transistors were assigned failure rates 1/3 that of the discrete semiconductor. Details are given in Table 5-2C.

5. The part temperatures for the USBE Transponder were obtained by thermal measurements of critical areas with a cold plate temperature of 48°C. For the advanced transponder thermal measurements obviously were not possible in the final package configuration. Consequently, the following assumptions were made based upon thermal experience with similar packaging: cold plate temperature 48°C; receiver and synthesizer modules, 7°C rise above cold plate; transmitter modules, 20°C rise above cold plate; and transmitter power supply, 12°C rise above cold plate.

   The junction or case temperatures of the parts were determined by calculating the temperature rise caused by the power dissipation and then adding this rise to the assumed modular temperature.

6. Electrical stresses were obtained from design calculations and from measurements performed on breadboard circuits where available.

7. Power supplies for the receiver and transmitter were not designed during this phase of the program. However, in order to compare the advanced transponder with the USBE system which contained 3 power supplies, it was necessary to consider compatible supplies. Consequently, supplies from another presently designed receiver and transmitter were selected for the reliability analysis. Since the power supply used for the transmitter had been designed for 150°C maximum junction temperatures of the semiconductors, it was assumed for this estimate that any semiconductors with junction temperatures in excess of 40°C rise above case would be paralleled and that this would halve the temperature rise.

8. Zero failure rates were assigned the loaded isolators, mechanical filters and strip-line tuning screws as they were mechanical in nature. (This policy was also followed on the USBE estimate.)

Because of the unspecified requirement of the mission, no firm derating limitations were stated to govern the application of parts for the advanced transponder. All parts except some semiconductor devices are operated much below their rated stress levels and, given a moderate operating ambient, could meet any reasonable derating policy.

Although no semiconductors approach the manufacturer's junction temperature limits, the junction temperatures of some devices do exceed the limit of 80°C imposed on the USBE Block II program. The amount of derating imposed on any part is a matter of engineering judgement influenced by the type of mission, money available, penalty for failure, and other factors. Junction temperatures can often be lowered by design changes, parallel operation, or relocation. However, this is not always feasible in high power applications such as the transmitter and the associated power supply. The impact of junction temperatures for semiconductors in the transmitter is discussed in more detail in the following section.

5.1.2 Failure Rate Discussion

Semiconductors account for 75.4 percent of the total failure rate assigned to the advanced transponder. Their percent contribution per assembly is shown in Table 5-3. A distribution of the number of semiconductors vs junction temperature rise above ambient is shown in Table 5-4.

The principle reason for the large contribution by the semiconductors to the total failure rate is the high penalty imposed for junction temperatures above 80°C when using the Collins failure rates. For example, a semiconductor operating with a junction temperature of 100°C is assigned a failure rate 3.7 times that of one with a 80°C junction temperature. At 110°C, the failure rate assigned is 7.4 times the 80°C rate. By comparison, MIL-HDBK-217A assigns a failure rate at 110°C of only 1.6 times that of a device with an 80°C junction temperature. This comparison shows

Table 5-3. Percent Contribution of Semiconductor Devices to Total Failure Rate

	Discrete Transistors and Diodes	Monolithic IC's	Hybrid IC's	Total
Receiver	21.9	2.3	5.3	29.5
Synthesizer	1	83.4	-	84.4
Transmitter	83.2	-	-	83.2
Transmitter (No Pwr Supply)	92.0	-	-	92.0
Transmitter Pwr Supply	58.5	-	-	58.5
Complete Transponder	70	4.6	0.8	75.4

Table 5-4. Distribution of the Quantities of Semiconductor Vs. Junction Temperature Rise

Function (Ambient)	Junction Temperature Rise Above Ambient or Case, °C									
	5	10	15	20	25	30	35	40	45	50
Receiver (55°C)	35	28	4	4	10	1	5	--	--	--
Synthesizer (55°C)	5	1	--	1	2	6	16	--	--	--
Transmitter (68°C) (except Pwr Supply)	3	--	5	--	1	1	5	--	2	5
Transmitter (60°C) Power Supply	25	8	8	16	5	1	--	--	--	--

the large difference of opinion existing concerning the assignment of failure rates to parts and illustrates the importance of using the same failure rates in comparing reliability estimates.

In the PA (power amplifier) modules of the transmitter, four power transistors are operated in parallel. The junction temperature was calculated to be 51°C above the case temperature. In the driver modules of the transmitter, the calculated junction temperature rise for the two transistors in parallel was 34°C and for the series transistors 28°C. These calculations were based upon Motorola's measurement of thermal resistance of 5°C/watt, performed on 3 devices. However, the vendor has

reported somewhat higher values, which point out a problem of correlating measurement techniques, and a possible inaccuracy in assumption of the operating junction temperature of the seven transistors discussed above.

In order to obtain lower junction temperature rises in the PA and driver, it would be necessary to use additional transistors in parallel. This would require additional couplers both before and after the transistors. The couplers induce a loss of approximately 0.1 db each; thus, lower junction temperatures for these power transistors in the PA and driver can be obtained, but at the cost of power efficiency. This power loss is described in more detail in the redundancy section that follows.

The second type of parts that were a major contributor to the total failure rate were the five transformers in the transmitter power supply. These contributed 36.6 percent of the failure rate of the power supply and 7.7 percent of the system. These transformers were calculated to have less than $10^{o}C$ temperature rise over ambient; thus, reducing the rise would have negligible effort on the assigned failure rate. (As noted previously, the power supply for the transmitter has not been designed and a similar supply was considered in order to complete a reliability estimate for the entire transponder.)

5.1.3 Comparison of the Two Systems

The estimated failure rate of the new system is 2.73%/1000 hours, which compares quite favorably with the estimated failure rate of the present system (PM Mode -- No TLM) which is 3.05%/1000 hours. It should be realized that the failure rate estimate of the advanced transponder is based on the specific parts complement and design of a breadboard model and that future changes to meet different requirements would alter this failure rate.

The failure rate improvement was due to design improvements including:

1. Use of a receiver frequency scheme that reduces susceptibility to self-jamming, thus requiring less shielding and fewer filter and isolation circuits.

2. Designing the synthesizer as a separate, switchable assembly, resulting in reduced duty cycle and power consumption. (In the USBE Transponder the synthesizer function was integrated within the receiver.)

3. Use of S-band amplification which eliminates certain functions such as the second mixer.

4. Substitution of semiconductor devices for the short-lived TWT in the power amplifier, thus eliminating high voltage, corona and replacement problems.

5. Use of stripline, thus reducing the number of discrete reactive devices.

5.2 REDUNDANCY

5.2.1 General

By the use of redundancy at the part, circuit, or system level, a significant degree of reliability improvement can often be obtained. However, this improvement requires a compromise among several factors, the common ones being weight, power and cost which must be balanced against the importance of a successful mission. In many instances, firm upper limits exist for some of these factors, further restricting the tradeoff. However, since no specific limits have been defined for this program, tradeoffs involved with various combinations of redundancy will be examined but no specific recommendations will be developed.

The reliability of a part, circuit, or equipment, that is, the probability that it will not fail in "t" hours, is a function of λ (the failure rate of the part, circuit, or equipment, normally stated in %/1000 hours). For a non-redundant equipment built with parts having an exponential survival characteristic, that is, a constant failure rate (the usual assumption), $R = \exp(-\lambda t)$ where λ is the sum of the part failure rates. In this case, either R or λ satisfactorily describe the reliability characteristics. However, the survival characteristic of a parallel combination of parts, circuits, or equipments is not exponential and the failure rate of the combination is not constant. Therefore, redundant configurations should be compared in terms of R. To do this it is necessary to assume a value for "t", the mission time, as will be done in the examples to follow.

The failure rate of the transmitter is quite large when compared to those of the receiver and synthesizer (see Figure 5-1). The exciter, driver, power amplifier, power multiplier, and power supply modules are the major contributors to the transmitter failure rate. The power supply and the exciter will not be considered for the application of redundancy; the power supply was an assumed supply and not designed for this project, and the exciter, because of its high parts count, does not lend itself to redundancy at the parts level. The driver, power amplifier, and power multiplier modules do, however, have high failure rates associated with low parts count and lend themselves to examining redundancy at the parts level. These circuits will be considered in some detail with respect to redundancy.

Figure 5-3 illustrates the arrangement used for power amplification in the transmitter of the advanced transponder (the basic system). The semiconductor devices in the multiplier are varactor diodes; those in the driver and power amplifier are power transistors. Each rectangle drawn with a solid line represents a module weighing approximately 0.4 pounds.

The nature of the circuits is such that if one of the semiconductors in parallel fails, the power output of that module is reduced by approximately half; that is, the remaining semiconductor does not receive the extra drive and correspondingly, increase its output. For example, failure of one transistor in the power amplifier would cause a 50% reduction in output power of that module but only a 25% reduction in the output power of the power amplifier.

The failure rate of the basic transmitter was calculated to be 2.20% per 1000 hours (see Figure 5-1) of which the power amplifier accounts for 45% of the total. The parallel devices were not considered redundant; the parallel configuration is necessary for power sharing and failure of any device comprises transmitter failure in this calculation. For a 1000 hour mission, 100% duty cycle, the reliability of this transmitter is calculated to be .978. However, if the performance requirements were defined such that a loss of 25% of the output power of the transmitter is acceptable; that is, one of the four transistors in the power

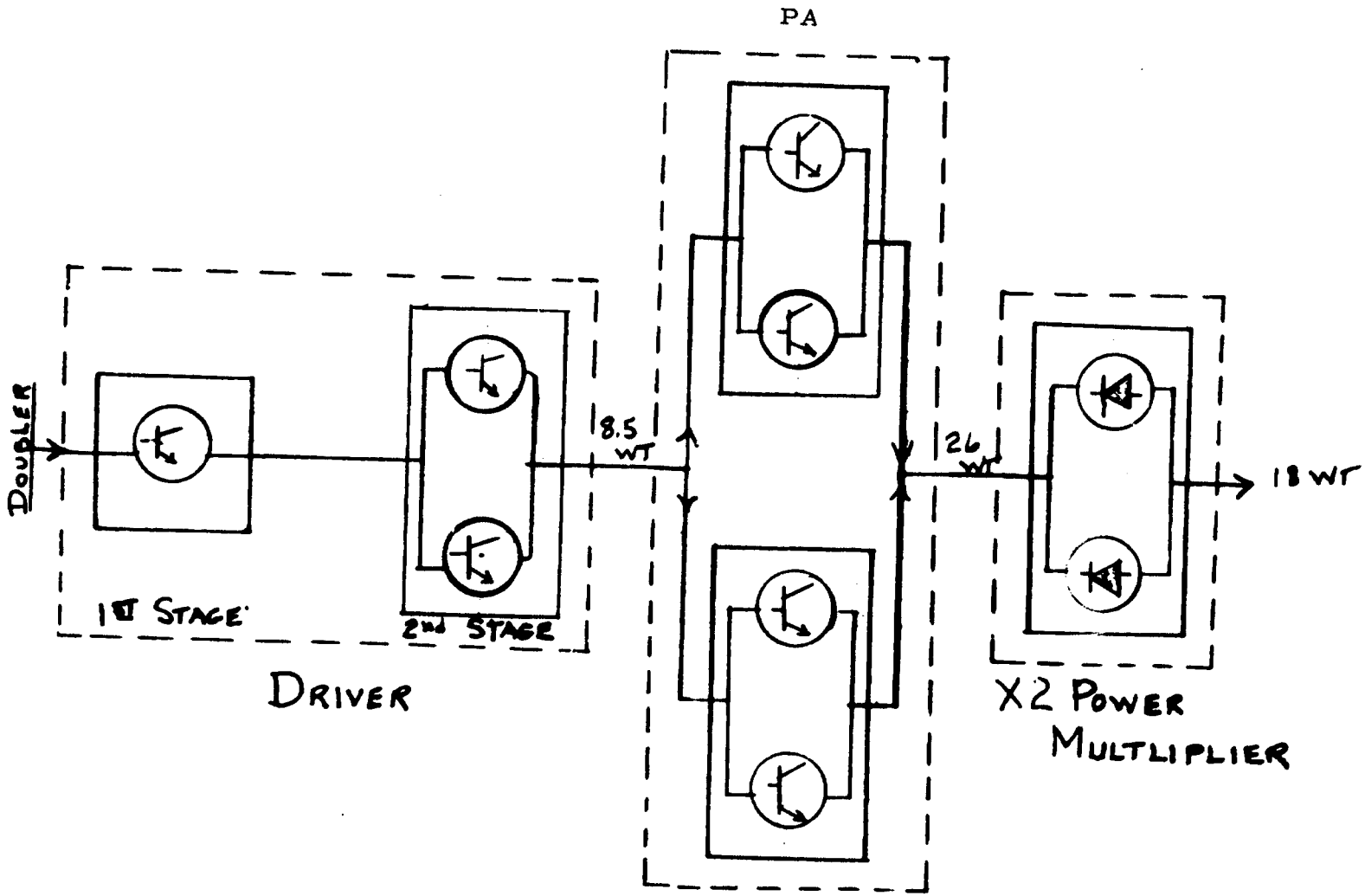


Figure 5-3.

Module and Semiconductor arrangement for Power Stages of Transmitter, Basic Design

amplifier were allowed to fail, (see Figure 5-3), then the reliability as calculated in example 5.1 would be .988 and the contribution of the power amplifier to the transmitter unreliability would be negligible. (The power supply module would then be the largest contributor to the transmitter failure rate; 45%.) If a single failure occurred in the second stage driver module or the power multiplier module instead of the power amplifier, the transmitter output power would decrease by approximately 50%. Therefore, the probability (reliability) of the transmitter retaining at least 50% of its initial output power for a 1000-hour mission, 100% duty cycle, would be .991. Consequently, the probability is quite high that if the transmitter fails, the failure will be caused by a semiconductor in the second stage driver, power amplifier, or power multiplier, in which case the transmitter power output will decrease by one-fourth if the failure occurred in either of the power amplifier modules or one-half if it occurred in the second stage driver or power multiplier modules. However, the probability that two semiconductor failures will occur in these modules during a 1000-hour mission is negligible compared to the probability of a failure in the rest of the transmitter.

5.2.2 Augmented System

From the previous paragraph it is seen that when parts are in parallel, a considerable increase in reliability is observed when one semiconductor is allowed to fail. If in the basic transmitter a 25 or 50 percent loss of output power is unacceptable but the advantages of increased reliability are desired, then an obvious solution is to use more semiconductors in parallel. Not only will the loss of a semiconductor result in a smaller reduction in output power, but the probability of the first failure is reduced because the increased sharing of the load reduces the individual semiconductor junction temperature. There are, of course, disadvantages.

The stripline characteristics are such that it is desirable to add semiconductors in pairs. Each pair represents a module weighing approximately 0.4 lbs. In addition to the weight penalty there is also the cost of the added parts. Power loses are also introduced; these are discussed later.

EXAMPLE 5-1

(See Figure 5-4)

Reliability of the Basic Transmitter allowing one transistor, or associated circuit, failure in the PA.

The reliability, R_T, of the transmitter using the failure rates from Figure 5-1, allowing one transistor or associated circuit failure in the PA, and assuming a mission time (t) of 1000 hours, 100 percent duty cycle is:

$$R_T = R_T' \cdot R_{PA} = (.9884)(.99996) = .98836$$

$R_T' = \exp(-\lambda t) = .9884$, the reliability of the transmitter exclusive of the PA with a failure rate of 1.17%/1000 hours.

$$R'_{PA} = R_{PA}^4 + 4R_{PA}^3 (1-R_{PA}) = .99996$$

where R'_{PA} is the reliability of the PA allowing one transistor failure. This is the probability that no devices fail plus the probability that any one of the 4 devices fail and the remaining 3 devices work. The probability of a device failing is $(1-R_{PA})$. $R_{PA} = e^{-\lambda t} = .9974$ is the reliability of a single transistor and associated circuitry with a failure rate one fourth of the PA or 0.255%/1000 hours.

Figure 5-4 shows a scheme in which the basic transmitter of Figure 5-3 has been augmented by an additional PA module in parallel. In this scheme the loss of one transistor in the PA represents a 16.7 percent output power loss instead of the 25 percent loss in the basic transmitter as discussed previously. Adding this third module requires additional stripline couplers which introduce power losses of 0.1 db apiece. To maintain the same transmitter output power would require an additional 1.45 watts of prime power from the transmitter power supply; an increase of 1.6%. Because of the characteristics of the stripline couplers, a fourth PA module could be added with no increased losses.

The scheme of parallel modules is not restricted to the PA. Another module could be added in parallel with the second stage driver with negligible power losses or with the power multiplier, which would require approximately a 4 percent increase in prime power to maintain the same transmitter output power.

5.2.3 Standby Redundancy

The type of redundancy just discussed is often referred to as active or parallel redundancy. Another type of redundancy makes use of "stand-by" units, generally non-operating until used to replace a unit that fails. The advantage of such a system over the active system is that the same degree of reliability is generally obtained without incurring performance degradation. A disadvantage is that the stand-by system normally requires failure-sensing and switching devices which, in a complex unmanned system, may limit the reliability of the stand-by redundant system to the reliability of the switch.

Figure 5-5 illustrates a scheme in which a typical stand-by switching arrangement has been applied to the PA modules of the basic transmitter. Diode type switches and sampling and switching logic were assumed. As previously discussed, the reliability of the basic transmitter for a 1000-hour mission was .978. With a stand-by PA module, as calculated in example 5-2, the reliability increases to .9875, the same (.988) as the previous example that allowed 25 percent degradation in the PA power output. It should be noted that although the

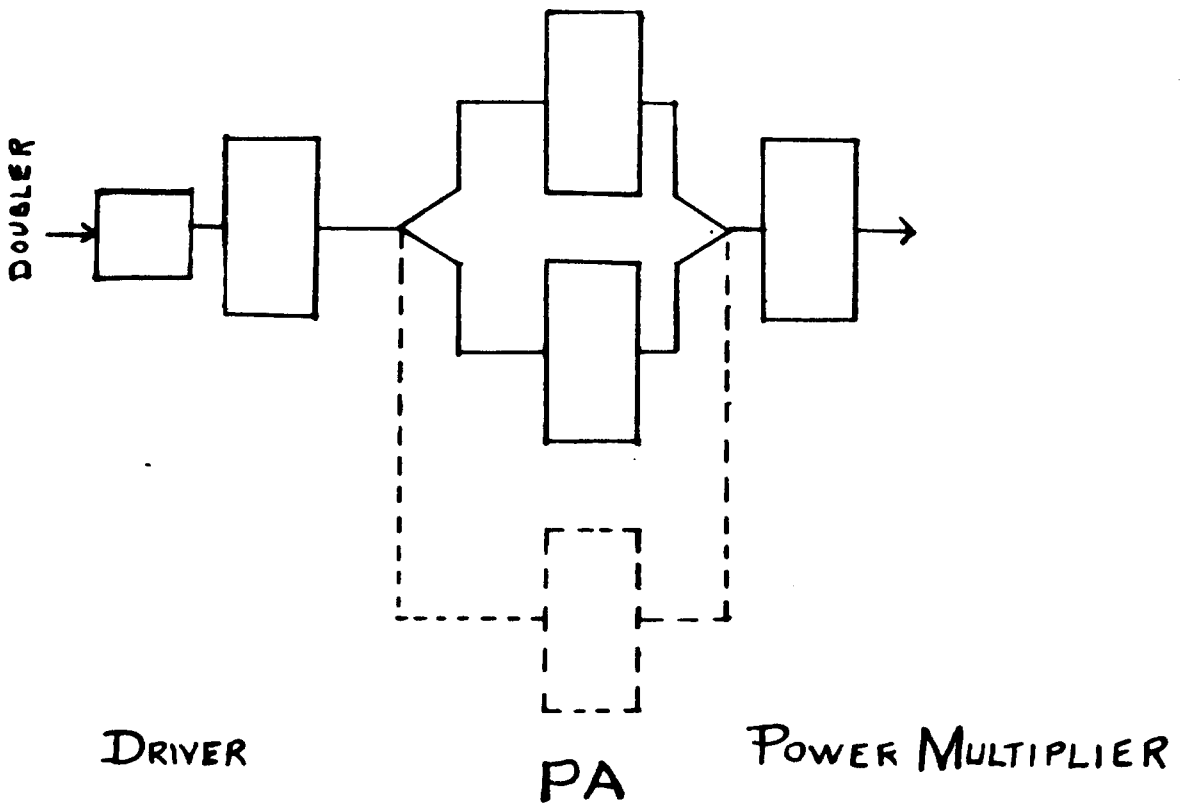
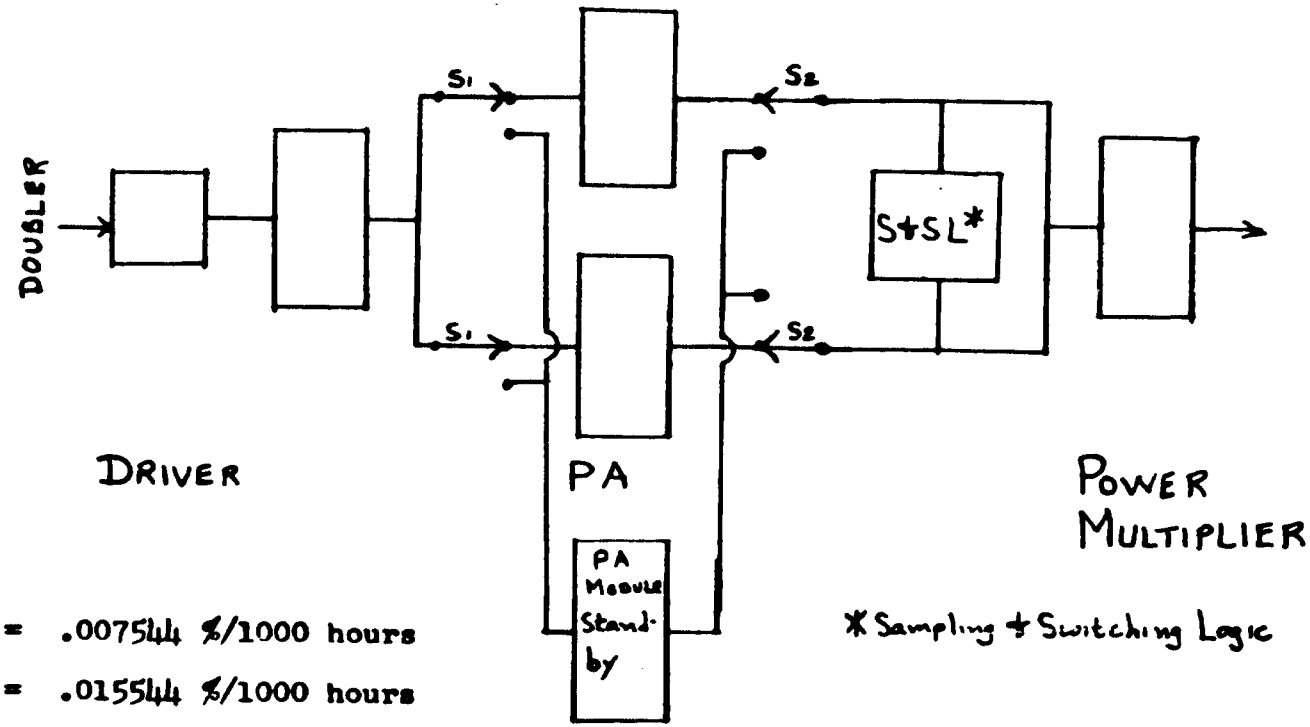


Figure 5-4. Transmitter Scheme Augmented by an Additional Power Amplifier Module



Failure Rates

Switch 1: $\lambda 1$ = .007544 %/1000 hours

Switch 2: $\lambda 2$ = .015544 %/1000 hours

S & SL: $\lambda 3$ = .001003 %/1000 hours

PA Module: $\lambda 4$ = .509137 %/1000 hours = $(\lambda PA)/2$ from Figure 2.1

Figure 5-5. Typical Transmitter Standby Switching Arrangement

reliability of the PA with stand-by redundancy is .99995, the reliability of the switch and associated logic reduced the achieved reliability of the PA to .99971. The switches used in the example introduce 0.2 db power loss each which amounts to an additional 3.6 watts of prime power required to maintain the same power output.

To summarize, in the example of the PA, stand-by redundancy provided the same increased transmitter reliability as parallel redundancy without the disadvantage of degradation of power output, but with the disadvantage of introducing more than twice the power losses.

5.2.4 Conclusion

Many different arrangements of redundancy could be investigated, each one resulting in a unique mix of reliability, weight, size, power requirement and, of course, cost. In the case of stand-by redundancy the reliability results would depend heavily upon the type of switching methods required. For example, manually operated toggle switches, if feasible, might be more reliable than the diode switches discussed above. Also, redundancy can be applied to the switches.

When considering redundancy for a specific application, matters not specifically discussed herein may be important. For instance, in considering power losses one cannot ignore the effects of the additional heat generated. With respect to the reliability of the associated parts, compensating for losses by increasing the power output would result in increased operating temperatures and also reflect upon the reliability of the power supply. When considering the addition of redundant modules, the weight of the additional modules is appreciable; also weight may be added because of a resultant increased size of the equipment case and cover, or increased cabling requirements.

EXAMPLE 5-2.

(See Figure 5-5)

Reliability calculations for Standby Redundant PA module configuration.

The reliability, R_T, of the basic transmitter using the failure rates of Figure 5-1, using a third PA module as standby (Figure 5-5), and assuming a mission time of 1000 hours, 100% duty cycle, is:

$$R_T = R_T' R_S R'_{PA} = (.9884)(.99976)(.99995) = .98811$$

where

$R_T' = .9884$ from example 5.1

$R_S = \exp - (2\lambda_1 + 2\lambda_2 + \lambda_3)t = .99976$

$\lambda_1 = .007544\%/1000$ hours

$\lambda_2 = .015544\%/1000$ hours

$\lambda_3 = .001003\%/1000$ hours

R_S is the reliability of the switches and logic used to sample the output and switch the standby unit in case of failure.

$$R'_{PA} = \left[\exp(-2\lambda t)\right] \left[1 + 2\lambda t\right] = .99995$$

λ = failure rate of one PA module = $.509137\%/1000$ hours

R'_{PA} is the reliability of the PA with one module with zero failure rate while nonoperating performing as standby to either of the 2 PA modules. Mission success requires the operation of two modules.

NOTE 1. The expression for R'_{PA} is an approximation since the dc power would be applied to the third module during standby. However, the transistors are operating Class C during standby which results in low power dissipation and correspondingly negligible failure rates in comparison with the

operating modules. The correct expression is:

$$R'_{PA} = \left[\frac{\lambda b + 2\lambda a}{\lambda b}\right] \exp(-2\lambda at) - \left[\frac{2\lambda a}{\lambda b}\right] \exp(-2\lambda at + \lambda bt)$$

where λa is the failure rate of the operating units and λb is the failure rate of the standby unit during standby.

If $\lambda b = \lambda a$ the expression immediately reduces to $R'_{PA} = 3 \exp(-2\lambda t) - 2 \exp(-3\lambda t) = 3R^2 - 2R^3 = R^3 + 3R^2(1-R)$ which is the expression for three units in active parallel redundancy where one failure is allowed.

If b = 0, it can be shown in the derivation of the above expression that $R = e^{-2\lambda t}(1+2\lambda t)$ which was the expression used in the example.

NOTE 2. The analysis of the switch reliability was performed using worst case conditions, that is, any switch failure was assumed to cause system failure--an untrue assumption. In this example the switch reliability was such that it had little effect on the final transmitter reliability. For example, assumption of a perfect switch would change the transmitter reliability estimate from .98811 to .98835. However, if one were interested in only the PA, the switch would not be negligible since it would reduce the PA reliability from .99995 to .99971. If this situation were critical in the overall estimate, then a more realistic estimate of the switch reliability could be obtained by the aid of a failure mode and effect analysis. For example, in Figure 5-5, a failure of any of the diode switches in the open mode does not fail the system, but merely prevents that branch from being switched out and the standby unit switched in. All combinations should be considered, probabilities of open open and shorted diodes assigned, and the switch reliability estimate upgraded.

5.3 PART PROCUREMENT POLICY

5.3.1 Scope

For reliability commensurate with a hi-rel mission (critical, manned, or long duration in space), it is desirable to obtain the highest reliability parts that are practically available. The military established reliability (ER) part specifications appear a suitable choice for use in the procurement of such parts. (For this discussion, TX Specifications for semiconductors are considered as ER specifications.) However, ER specifications are not presently available for all types of parts and in some instances qualified suppliers are non-existent or are qualified to only the highest failure-rate level. Even with the assumption that these conditions improve with time there remains certain areas where clarification is needed or improved techniques should be considered. For these reasons a review of ER specifications was conducted.

Following are general and specific guidelines that should be used in applying ER and other specifications to the procurement of parts for this type program.

5.3.2 General

5.3.2.1 Quality Conformance Inspection

5.3.2.1.1 Inspection Lot. The definition of a lot should be determined for each part type at the time procurement documents are being prepared. For high usage items, such as film resistors or ceramic capacitors and where qualified suppliers exist for low failure rate level parts it may be sufficient to define a lot per the applicable ER specification. For special parts or part types for which no qualified suppliers exist, it may be necessary to define a lot as consisting of only the units manufactured to a particular purchase order.

5.3.2.1.2 Traceability. Unless otherwise noted in the individual discussions of part types, all parts should, as a minimum, be traceable to a production lot, (exceptions: carbon composition resistors and connectors). The vendor should

be required to maintain adequate records to identify all of the types of materials, parts and types of processes utilized in the production of the end item.

5.3.2.1.3 Screening. It should be required that 100 percent screening (Group A, subgroup 1 of most ER specifications) be imposed for all parts. Where more than one level of screening is available per the ER specification, parts should be purchased to the lowest failure rate levels (i.e., that which provides the strictest screening requirements).

5.3.2.1.4 QC (Quality Conformance) Sample Inspection. For most part types it should be required that the QC sample inspection involving the electrical and environmental tests be performed on samples from each lot purchased. Exceptions to consider are high usage parts such as metal film resistors where much test data has been accumulated on automated production.

For part types not qualified to a sufficiently low failure rate level or where the vendor has insufficient history in producing parts to ER specifications the sample size should be substantially increased and/or life tests should be required.

5.3.2.1.5 Qualification. For special part types, parts with unique applications, or parts for which no ER specifications exist, qualification of the parts should be considered. Sample sizes and tests required should follow that of the closest ER specification. Where qualification is required, selecting samples from the same lot as offered for acceptance to a purchase order should serve as fulfilling the requirements for QC sampling inspection.

5.3.2.1.6 Test Plans. For ER parts requiring special acceptance or qualification testing and for all non ER parts, a test plan containing details such as testing methods, procedures, test equipment, etc. should be submitted by the vendor for approval prior to the start of part testing.

5.3.2.2 Vendor Selection

Vendors qualified (or in the process of being qualified) to the lowest failure rate levels should be selected. Preferential consideration should be given to

vendors using separate production facilities for hi-rel parts. Where qualification does not exist or a qualification to a desired failure rate level is non-existent, first consideration again should be to vendors who have developed special production lines, inspection, procedures, etc. for hi-rel parts.

All vendors, including those qualified, should be required to meet the workmanship requirements of the purchaser's QA department prior to procurement.

5.3.3 Specific

5.3.3.1 Transistors, Diodes

Where available, TX devices should be specified with the addition of 100 percent visual "pre-cap" inspection at 30 power magnification and 100 percent X-ray. (Glass diodes and devices using internal aluminum bonding wires may be excluded from X-ray). For some applications it may be necessary to tighten the requirements on the delta limits and/or require higher power dissipation during the burn-in tests.

Manufacturers who have developed their own hi-rel programs should be considered first for devices for which TX specifications do not exist.

5.3.3.2 Integrated Circuits Including Multi-Chip and Hybrid Types

The same philosophy applies as for transistors except that, at the conclusion of the screening tests, electrical measurements should be required at high and low temperatures.

5.3.3.3 Connectors, RF

Screening should consist of, as a minimum, visual examination, continuity, and time-domain-reflectometer measurements of VSWR. When applicable, dielectric withstanding voltage (DWV), X-ray, and hermetic seal tests should be included.

For connectors that are received unassembled, the initial screening should consist of visual examination under magnification. After assembly to the cable,

all assembly should be checked for VSWR and, if applicable, DWV. Samples of the cable assembly should then be randomly selected, potted, and sectioned so that the internal cross sections of the assembly may be inspected for workmanship.

5.3.3.4 Connectors, Power

Screening should consist of, as a minimum, insertion-withdrawal force, contact resistance, pin diameter measurements, DWV and hermetic seal when such tests are applicable.

5.3.3.5 RF Coils, Molded

In-process inspection should be performed on all parts prior to sealing, molding or encapsulation. All parts should then be subjected to the Group A and B inspection requirements. The temperature cycling test of Group A should be extended to 10 cycles.

5.3.3.6 RF Transformers, Molded

Although no ER specifications exist for RF transformers, these parts should be procured to the same general requirements as the RF coils except that the electrical measurements should be modified to correspond to the transformer requirements.

5.3.3.7 Transformers, Audio and Power

In-process inspection should be performed on all parts prior to sealing, molding or encapsulation. All parts should then be subjected to the Group A and B inspection requirements. A temperature cycling test (10 cycles) should be added to Group A inspection.

5.3.3.8 Coils (Reactor) Audio and Power

Although no ER specifications exist for these parts, they should be procured to the same general requirements as the Power Transformers except that the electrical requirements should be modified to correspond to the coil requirements.

5.3.3.9 Resistors, Special: Thermal, Termination, etc.

Screening requirements should consist of, as a minimum, short time overload, temperature cycling (10 cycles), and 150 hours soak at high temperature.

5.3.3.10 Relays, Crystals, Filters, etc.

These parts are often used for special applications; consequently the qualification, acceptance and screening tests should be modified to the specific application.

For some complex assemblies, such as filters, it may be required that in-process inspection be performed by the purchaser's inspector prior to encapsulation or sealing.

5.3.3.11 Capacitors

At the present it is Motorola's philosophy to subject all capacitors to 168 hours of voltage conditioning (also called voltage aging or voltage stabilization). The ER specifications range from 24 hours to 100 hours. Data is continually being analyzed by the capacitor part specialist at Motorola to determine what the optimum time period should be. Consequently, the voltage stabilization time on capacitors may be increased over the ER requirements for some capacitors, depending upon the data available at the time of procurement.

For mica capacitors (MIL-C-39001) the high voltage stabilization voltage and the dielectric withstanding voltage should be changed from 1000 volts to twice rated.

5.3.3.12 Non-ER Parts

Procurement requirements for which no ER specifications exist should be consistent with the nearest applicable ER specification and the additional requirements discussed above under general requirements. Screening requirements and sample quantities may need to be increased, depending upon factors such as the part/vendor history, similarity to approved parts, and construction techniques.

As a minimum, each procurement document should require that the part conform to the application requirements during and after exposure to the environmental conditions specified for the program.

5.3.3.13 Microwave Printed Wiring Boards (Stripline)

No military or industry specifications presently exist concerning extra reliability requirements for this type part. Consequently the tests and examinations listed below are suggested. (Electrical measurement of the sheet laminate (raw stock) is to assure that the desired electrical properties are as specified. The purpose of repeating these measurements on samples of the finished boards is to assure that the manufacturing processes have not changed these properties beyond acceptable limits.)

Identification of the finished boards to the sheet laminate may be required depending upon the confidence in the supplier and the stability of his processes.

I. Sheet Laminate (raw stock)

A. Fabricate a disc, $0.5\ ^{+.000}_{-.010}$ inch diameter, from each of the four corners of each sheet of the raw stock.

B. Determine the DC (dielectric constant) and DF (dissipation factor) by the re-entrant cavity method at 500 MHz.

II. Finished Boards

A. 100 percent Inspection - Every finished board shall be subjected to the following examination:

1. Measure copper line width and spacing of critical areas on the board.

2. Measure thickness, warp and twist of the boards.

B. Sample Inspection - Sample boards shall be subjected to the following examination:

1. Fabricate disks, $0.5^{+.000}_{-.010}$ inch from areas of the board where; a) no copper exists, b) complete copper coverage exists on one side, and c) complete copper coverage exists on both sides (for double sided boards).

Three samples of each type coverage shall be obtained.

2. Repeat step IB.

5.4 RECOMMENDATIONS FOR ANALYSES

5.4.1 Failure Mode and Effect Analysis (FMEA)

The Failure Mode and Effect Analysis (FMEA) is performed to identify the principle modes of failure of all parts, to assign a probability of occurrence, and to determine the effect and criticality that each failure mode will have on the functional performance of the system. As a result of the FMEA, potentially critical failure areas may be determined in the equipment so that steps can be taken to minimize them through circuit redesign, selection of different parts, redundancy, isolation, or other techniques as appropriate.

The thoroughness of a FMEA should be suited to the reliability requirements of the mission and the complexity of the equipment. It is particularly important in redundant configurations. For example, in parallel active redundancy, a shorted part in the first unit might also short out the input signal to the other unit, failing both units. In standby units, a poorly designed switching circuit may result in the same problem, the failure in one unit causing the standby unit to become inoperative.

FMEA is also important with respect to interfaces between functions. For instance, failure of the transmitter should not effect the receiver function, and vice-versa.

In most instances, eliminating the failure interface between two components or units by circuit redesign will result in a considerable increase in reliability even though additional parts may be required.

As a minimum, it is recommended that a FMEA be performed on the interface between any redundant units, and on the interface between major equipment functions.

5.4.2 Stress Analysis

The reliability estimate and stress analysis included in this report were based on design calculations and available electrical measurements on breadboards. Upon the decision to build transponders for a definite mission, the stress analysis should be updated using known voltages and currents and using ambient and part temperature estimates verified by thermal measurements in critical areas.

5.4.3 Computer Analysis of Circuits

Computer analysis of circuits has proven to be very advantageous and should be applied, as appropriate, to the advanced transponder design when it progresses beyond the feasibility study phase. These circuit analysis methods utilize a digital computer to analyze the effects of nominal part parameter value and of variations therein on the performance of electronic circuits. The analysis is accomplished by constructing a mathematical model of an equivalent circuit that simulates the actual circuit and by applying appropriate analytical methods to obtain the desired solutions. These analysis methods are Worst Case, Moment, and Monte Carlo, the last two being probabilistic methods.

5.4.3.1 Objectives

The objectives of applying circuit analysis methods during the design phase are to:

1. Aid the design engineer in optimizing circuit design by evaluating circuit performance and performance variability as functions of selected component parts.
2. Assure that each equipment is designed for producibility by assuring that random selection of parts will not cause out-of-specification performance.

3. Assure that interchangeability or reliability is not impaired by component tolerance build-up, environmental effects or aging.

4. Increase reliability by reducing the number of part replacements and adjustments required.

5. Determine worst case component part stress levels.

5.4.3.2 Modes of Analysis

All circuit analysis methods are dependent on the existence of a valid mathematical model. DC, AC or transient modes of circuit operation can be analyzed, with each mode of operation requiring a specific type of equivalent circuit.

5.4.3.2.1 DC Analysis. The DC analysis of circuits is performed primarily to determine the effect of part parameter drift and tolerance limits on the stability of transistor circuits and component part stress levels. The important criteria for the analysis are transistor bias stability, power dissipation of dissipative parts, voltage stress on certain types of parts, and total power consumption.

5.4.3.2.2 AC Analysis. The AC analysis of circuits is performed primarily to determine the effect of component part parameter values on such steady state performance characteristics as gain, power output, input impedance and frequency response.

5.4.3.2.3 Transient Analysis. The transient analysis of a circuit is performed to determine the effect of component part parameter values on nonsinusoidal circuit waveforms. Important performance criteria generally include rise time, overshoot, droop, and delay time of the waveform.

5.4.3.3 Applicable Circuits

5.4.3.3.1 DC Analysis. Circuit analysis methods should be applied to all circuits which can be represented by linear DC equivalent circuits. This should include bias circuitry for transistors. A worst case DC analysis should be performed to determine component part stress levels. The results of this analysis

should be used to verify that the part derating limits are not exceeded under worst case conditions.

5.4.3.3.2 AC Analysis. Circuit analysis methods should be applied to all circuits which can be accurately represented by an AC linear equivalent circuit. Circuits operating at very high frequencies (avove 10 megacycles) usually cannot be analyzed, since effects of stray capacitance and coupling often make the development of a valid equivalent circuit extremely difficult.

5.4.3.3.3 Transient Analysis. Transient circuit analysis methods should be applied to circuits that can be represented by piecewise linear equivalent circuits. These circuits should include only those which are in critical applications and have a large effect on the equipment reliability.

5.4.3.4 Documentation

The following information should be prepared for each circuit analyzed.

1. A brief description of the circuit and its function in the equipment.
2. A schematic drawing of the circuitry being analyzed and the resulting equivalent circuits.
3. A result sheet showing component part number, nominal part type or value and tolerance, and relative contribution of the component part to performance variability. The appropriate worst-case DC stress levels for each part should also be included.
4. A brief narrative summary of the analysis, stating the circuit function and the criteria for its successful performance, the most critical part parameters, and any changes made as a result of the analysis.

5.4.4 Reliability Trade-Off Analyses

Reliability trade-off analyses should be performed whenever alternate circuit design approaches are available. The objective should be to select the optimum design approach considering reliability, performance, weight, size and power

consumption factors. Whenever possible trade-off analyses should be made using figures of merit, representing the relative importance of each parameter under consideration.

5.5 INTENT OF ANALYSIS AND PARTS PROGRAM

At such time as a definite specification is invoked, it would be expected that the tradeoff analysis of 5.4.4 and the guidance of subsection 5.2 would be of value in arriving at decisions regarding redundancy. When the advanced transponder design is relatively firm the other analyses of subsection 5.4 could be important in obtaining a highly reliable design. The parts program of subsection 5.3 would assure the procurement of high reliability parts and materials consistent with the design intent.

SECTION VI
PACKAGING

6. INTRODUCTION

This section describes problems pertinent to packaging a phase locked loop transponder. The main topics analyzed or discussed are environmental criteria, packaging techniques, structural design, and shielding and housing requirements.

6.1 ENVIRONMENTAL

6.1.1 Selection of Environmental Design Criteria

The selection of a set of environmental conditions to be used as design criteria for the advanced transponder assumed that its most probable use would be on Apollo type hardware and that the environments defined in the specifications for the LEM S-Band Transceiver, the Block II CSM Transponder, and the Saturn IV-B S-Band Transponder are representative of the environments that would be imposed on any flights using Apollo type hardware.

It should be noted that there is some question about the validity of such an assumption, specifically in the case of the LEM Transponder. The vibration profiles currently imposed on the LEM Transponder are unique to the transponder in that they were derived from tests with a mockup of the transceiver and a secondary structure simulator. There is some indication that subsequent testing of a mockup of the LEM aft equipment bay resulted in levels in excess of those currently imposed. In any event, tests on a secondary structure simulator with a lighter weight unit, or imposition of vibration levels taken from a mockup containing a different transceiver could result in significantly different levels than those presently defined. It does not appear that a similar situation exists with either the Block II or S-IVB Transponders as the vibration spectrums for these programs appear to be generalized rather than specific.

6.1.2 Environmental Design Criteria

A comparison of the operating and/or flight environments of the three existing transponders and of their general mounting provisions indicates that, with the exception of the thermal environments, there is sufficient similarity in the specifications to allow making a worse case composite without imposing any undue restraints on the electrical design.

The thermal environments present a problem, not so much because of their severity, as because of the various derating policies that were imposed on the three existing systems. The major area of difficulty lies in the maximum allowable junction temperatures for semiconductor devices and also in the maximum allowable parts case temperature allowed on the LEM Transceiver. These are as follows:

1. For Block II CSM Transponder:

   Transistors <3 watts = 75°C maximum junction

   Transistors >3 watts = 80°C maximum junction

2. For LEM Transponder

   Maximum junction temperature = 100°C

   Maximum case temperature = 71°C

3. For Saturn IVB Transponder

   Maximum junction temperature = 150°C
   (Motorola imposed criteria)

4. Heat Sink Temperature Range

Block II CSM	17° to 48°C
LEM	2° to 57°C
Saturn IVB	-50° to 85°C

From the preceding, it can be seen that the Saturn IV-B heat sink exceeds the junction temperature allowed on Block II CSM and the maximum case temperature allowed on the LEM. Similarly, a unit designed to meet the 43°C sink to junction rise allowed on the LEM would not be acceptable under the Block II CSM derating policy which would allow only a 27°C or a 32°C sink to junction temperature rise.

The most realistic solution appears to be to use the LEM derating policies as a design guide. Such an approach would give conservative temperatures for the S-IVB version and slightly excessive temperatures under the CSM Block II policies. The effect of the slightly excessive temperatures will probably only show up on higher dissipation devices and the net effect can be determined from the system reliability numbers.

6.1.3 Flight and Pre-Launch Environments

6.1.3.1 Heat Sink Definition

In order to allow for realistic derating, it is necessary to define all three heat sink conditions. The LEM heat sink will be used for design considerations.

6.1.3.1.1 Block II, CSM, S-Band Transponder. The heat sink is defined as maintaining the cold plate mating surface temperature between 62.5°F and 118°F while the ambient varies between 32°F and 150°F. The unit shall be designed to operate within performance specifications with the heat sink maintained at 140°F for a period of 15 minutes. Derating policies are not applicable during this period of high temperature operation.

6.1.3.1.2 LEM S-Band Transponder. The heat sink is defined so that the flange root temperature of the mounting flanges is maintained between 35°F and 135°F while the ambient varies between 0°F and 160°F. The preceding definition is true for heat densities along the cold rails that do not exceed 2.25 watts per linear inch of cold rail.

6.1.3.1.3 Saturn IV-B Transponder. The heat sink is defined such that the temperature of the heat sink will vary between -50°C and +85°C.

6.1.3.1.4 Cooling Method. The thermal design shall be based on heat transfer by conduction to the heat sink only.

6.1.3.2 Pressure Range

The unit shall be designed so that all specifications are met while the pressure varies between sea level and 10^{-14} mm Hg. All vacuum tests shall be conducted at 10^{-4} mm Hg or better. The unit shall be operated during any pressure cycling.

6.1.3.2.1 Thermal-Vacuum. The unit shall be designed to operate within specification under any combination of pressure and temperature defined in paragraphs 6.1.3.1 and 6.1.3.2.

6.1.3.3 Random Vibration

The design shall be such that the unit will operate within specification while subjected to the following random noise vibration for a period of 15 minutes in each plane.

20 - 59 Hz	Constant 0.04 g^2/Hz
59 - 126 Hz	9 db/octave linear increase*
126 - 700 Hz	Constant 0.4 g^2/Hz
700 - 900 Hz	18 db/octave linear decrease*
900 - 2000 Hz	Constant 0.09 g^2/Hz

*Linear is defined as a linear on a log-log plot of spectral density versus frequency

6.1.3.3.1 Criteria for Use of S-IVB Random Vibration Envelope. Plots of the qualification test random vibration levels are shown in Figure 6-1. These plots represent the inputs to the primary transponder mounting structure. These inputs are then modified by the dynamic response of the mounting structure into loads on the structure and components. In the absence of any specific response

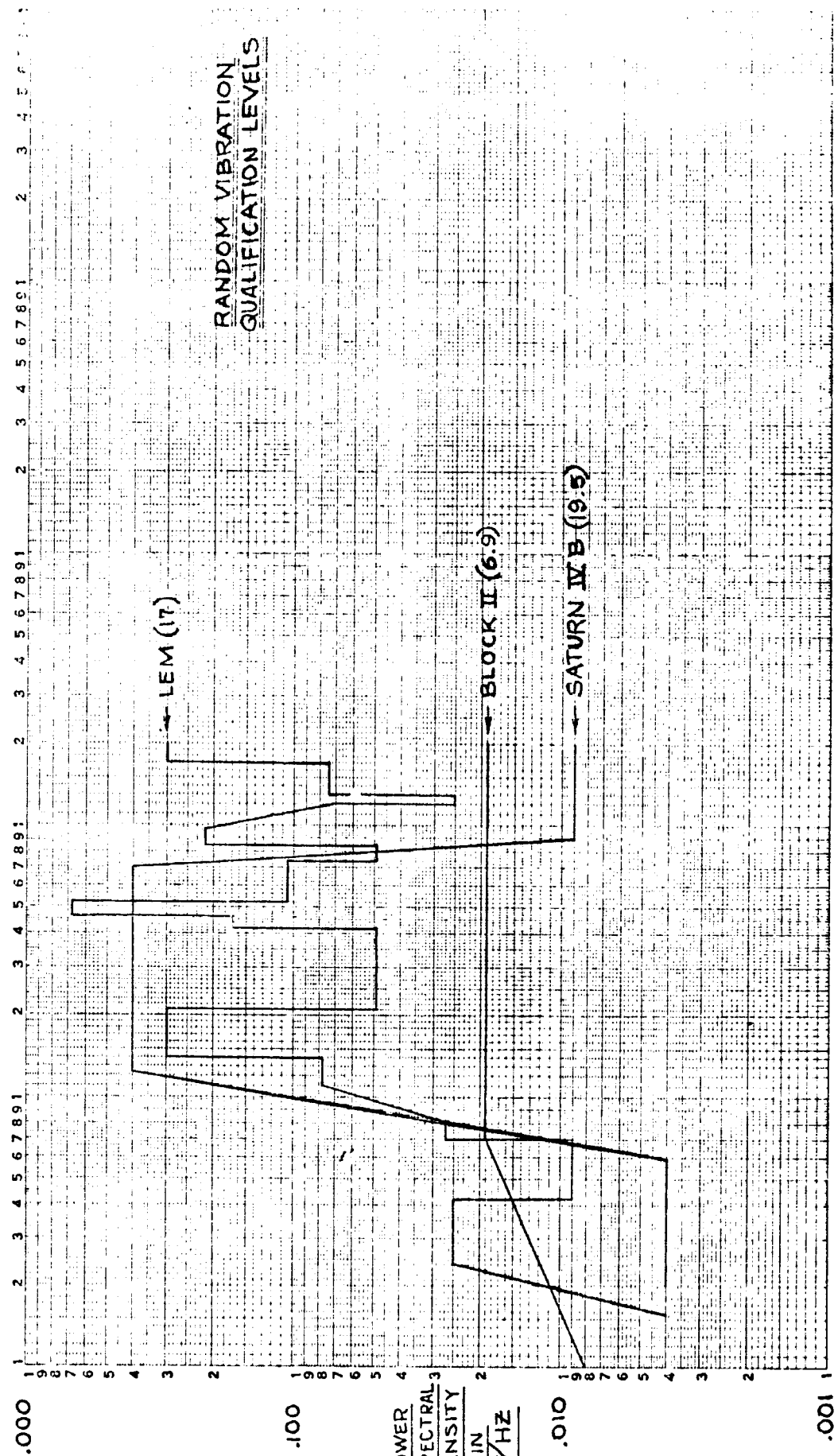


Figure 6-1.

data for use in modifying the input, a common technique is to assume a resonance with a transmissibility of 10 at any frequency within the spectrum. The use of this technique gives Figure 6-2 which represents load curves based on the three inputs. Figure 6-2 is plotted in terms of RMS g's (σ) but stress analysis is based on 3σ limits.

It is evident from an examination of Figure 6-2 that the load curve for the LEM input gives much higher loads at specific frequencies than does the S-IVB, however, response data from a LEM Transceiver indicates a resonance at about 400 Hz and it is reasonable to expect a response for any repackaging in the LEM configuration to lie between 400 and 1000 Hz. The effect of a response in this frequency range is to eliminate the peaks at 1900 and 90 Hz shown in Figure 6-2. With these peaks eliminated, a load curve based on the S-IVB input is sufficiently representative for design purposes in that a system designed to meet that load curve could reasonably be expected to survive any of the three inputs.

6.1.3.4 Maximum Transmissibility

The design shall be such that transmissibilities shall not exceed 10 for any structural element used to mount electronic components. A maximum transmissibility of 25 is acceptable for non-structural items such as covers and EMI shields.

6.1.3.5 Acoustic Noise

The design shall be such that all specifications are met while the unit is subjected to the following acoustic noise levels:

Center Band Octave Frequency (Hz)	Sound Pressure Level (db)*
11.2 to 22.4	113
22.4 to 45	121
45 to 90	127
90 to 180	127

Center Band Octave Frequency (Hz)	Sound Pressure Level (db)*
180 to 355	126
355 to 710	127
710 to 1400	129
1400 to 2800	131
2800 to 5600	125
5600 to 11,200	118
Overall	137

*re 0.0002 dynes/cm^2

6.1.3.6 Shock

The unit shall meet all specifications after being subjected to 3 shocks in each of six directions. The shock pulse shall be a 78 g sawtooth with 11 $\pm$1 ms rise time and 1 $\pm$ ms decay time for a total of 18 shocks.

6.1.3.7 Acceleration

The unit shall meet all specifications while subjected to a sustained acceleration of 100 g's. The duration of the acceleration shall be 1 minute in each of the six planes.

6.1.3.8 Humidity

The unit shall meet all specifications after being exposed to an atmosphere containing 95% O_2 at 95% relative humidity for 120 hours. The temperature cycle shall be as defined in MIL-STD-810, Method 507, Procedure I.

6.1.3.9 Fungus

The unit shall meet MIL-STD-810, Method 508, Procedure I. Certification by the contractor in lieu of testing is acceptable.

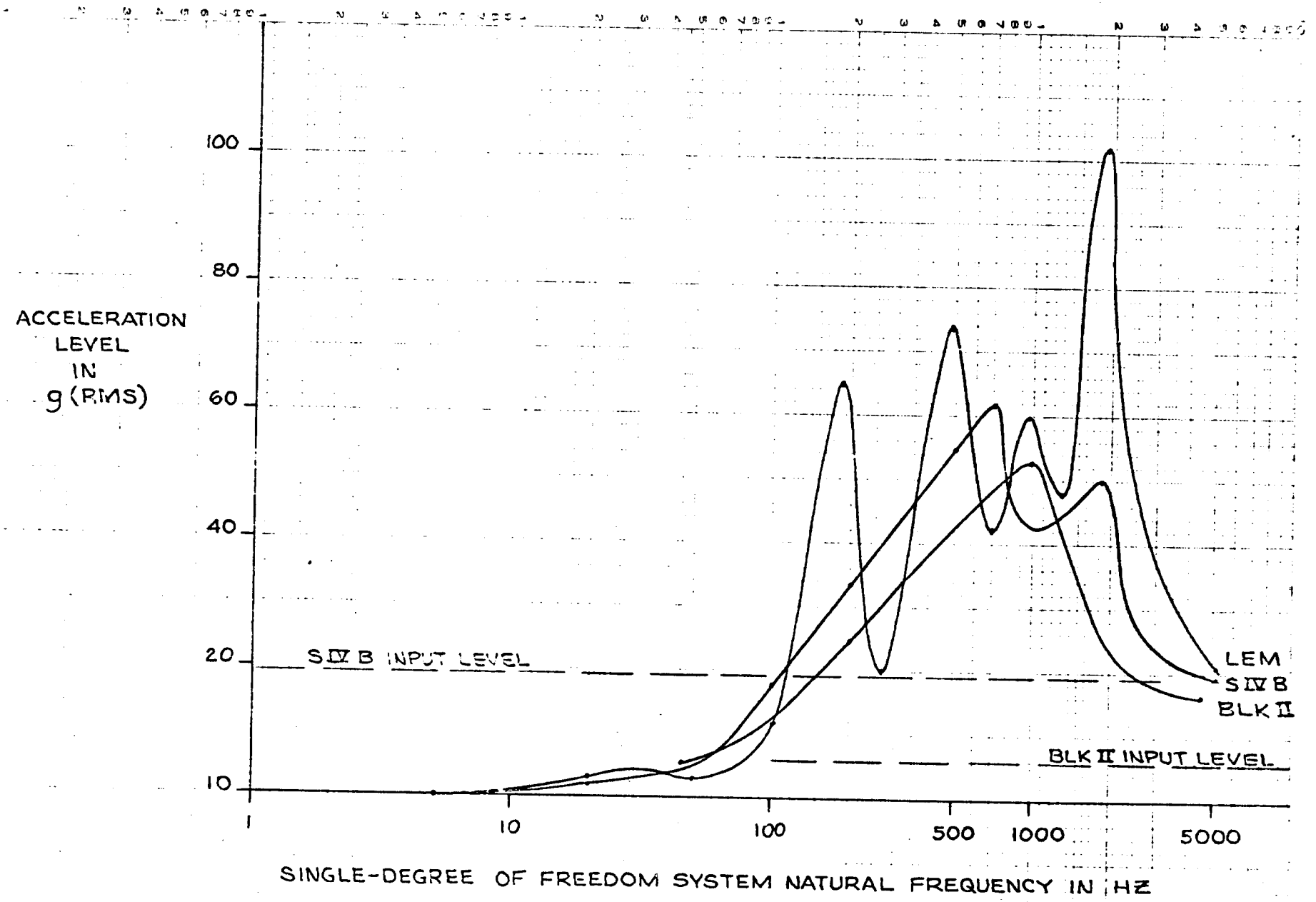


Figure 6-2. Load Curves

6.1.3.10 Explosion Proof

The unit shall be designed to meet MIL-STD-810, Method 511.

6.1.3.11 Other Environments

The unit shall be designed to meet such other environments as may be required by specific missions. Radiation and meteoroids are two such environments. These levels of exposure can only be defined in terms of specific mission requirements.

6.2 PACKAGING TECHNIQUES

6.2.1 General Packaging Philosophy

Since the three existing Apollo Transponders were designed, there have been improvements in packaging techniques and devices that will allow equivalent transponders to be built in less volume at less weight.

Preliminary estimates, based on the breadboard unit, indicate that there will be no problem in adapting the techniques to any of the three envelopes specified for the existing transceivers. See Figures 6-3 through 6-5 for a comparison of the envelopes.

The advanced transceiver could be packaged using either the LEM or the CSM Block II techniques and meet all specifications. However, these approaches were somewhat inefficient in their use of weight and volume when compared to the efficiencies obtainable by using techniques and devices presently available. See Table 6-1 for a comparison of the predicted weight and volume versus the weight and volume for the existing units.

Most of the effort in packaging has been expended in developing techniques that will allow a modular configuration that will adapt to almost any configuration. The breadboard receiver is packaged in four basic modules and the breadboard 18 watt transmitter is packaged in seven basic modules. Additional modules can be added as required to provide other functions and the output power of the transmitter can be varied by minor changes in design.

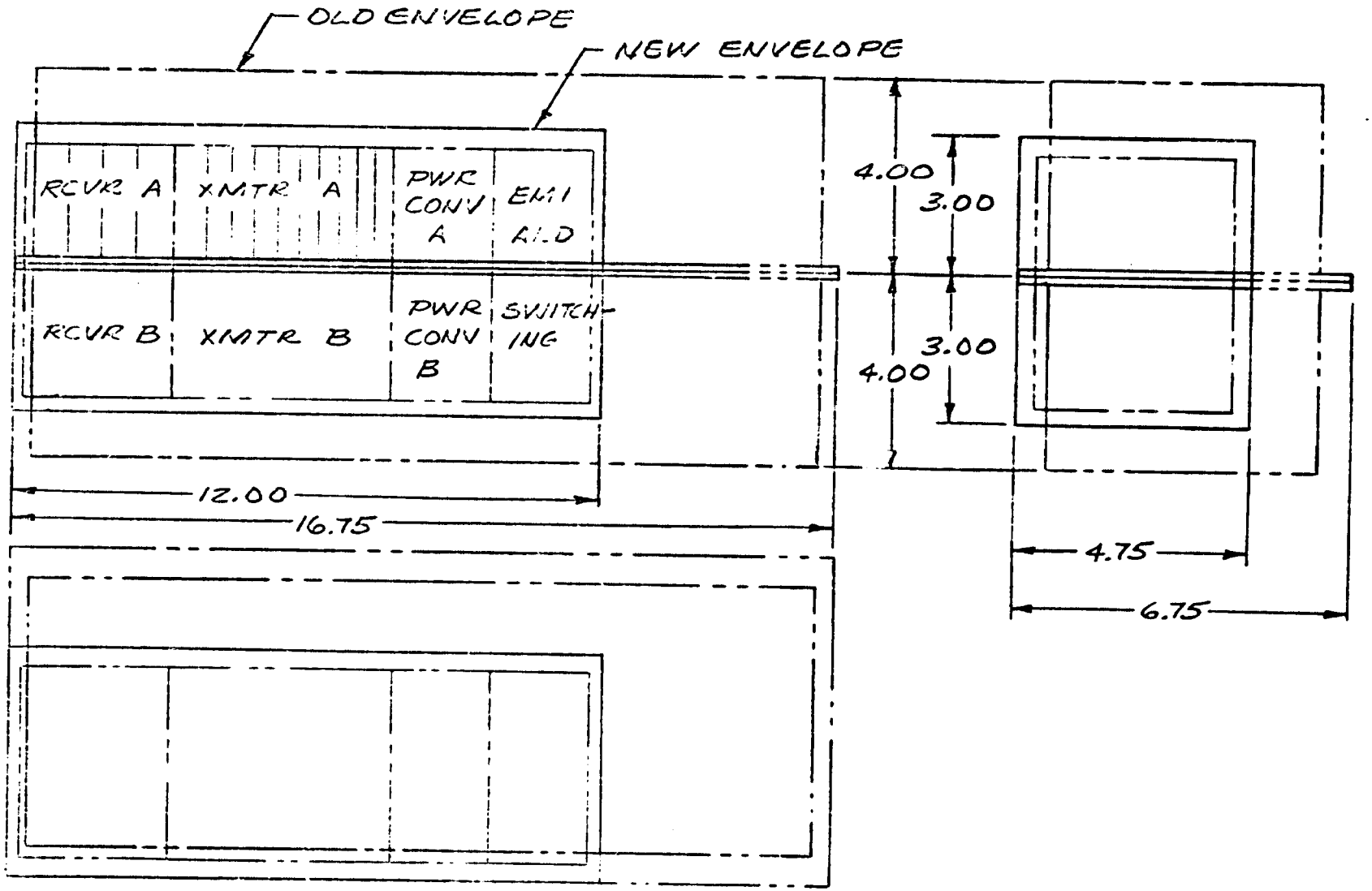


Figure 6-3.
TENTATIVE LEM CONFIGURATION
18 WATT TRANSCEIVER

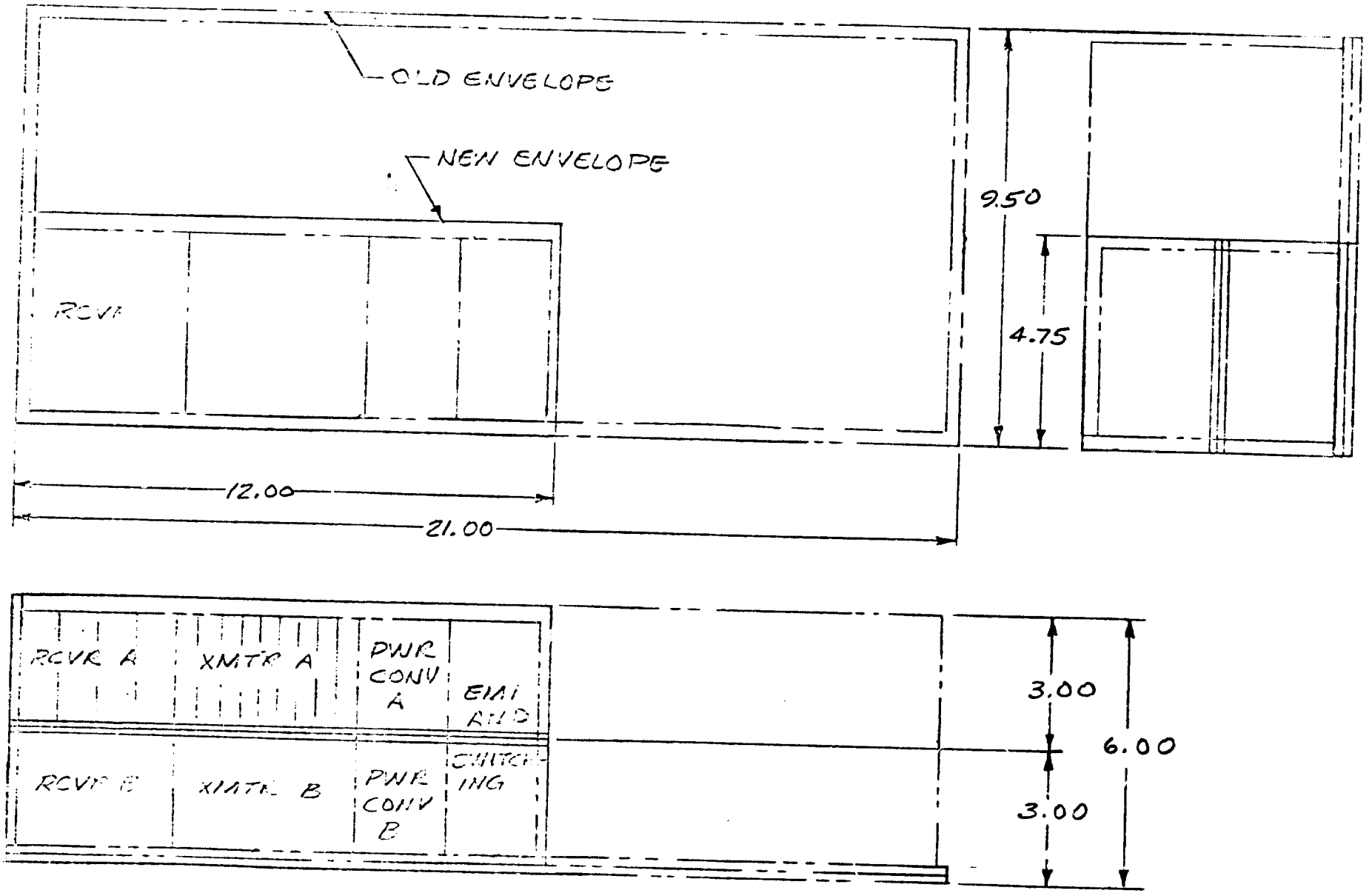


Figure 6-4.

TENTATIVE BLOCK II CSM
18 WATT TRANSPONDER

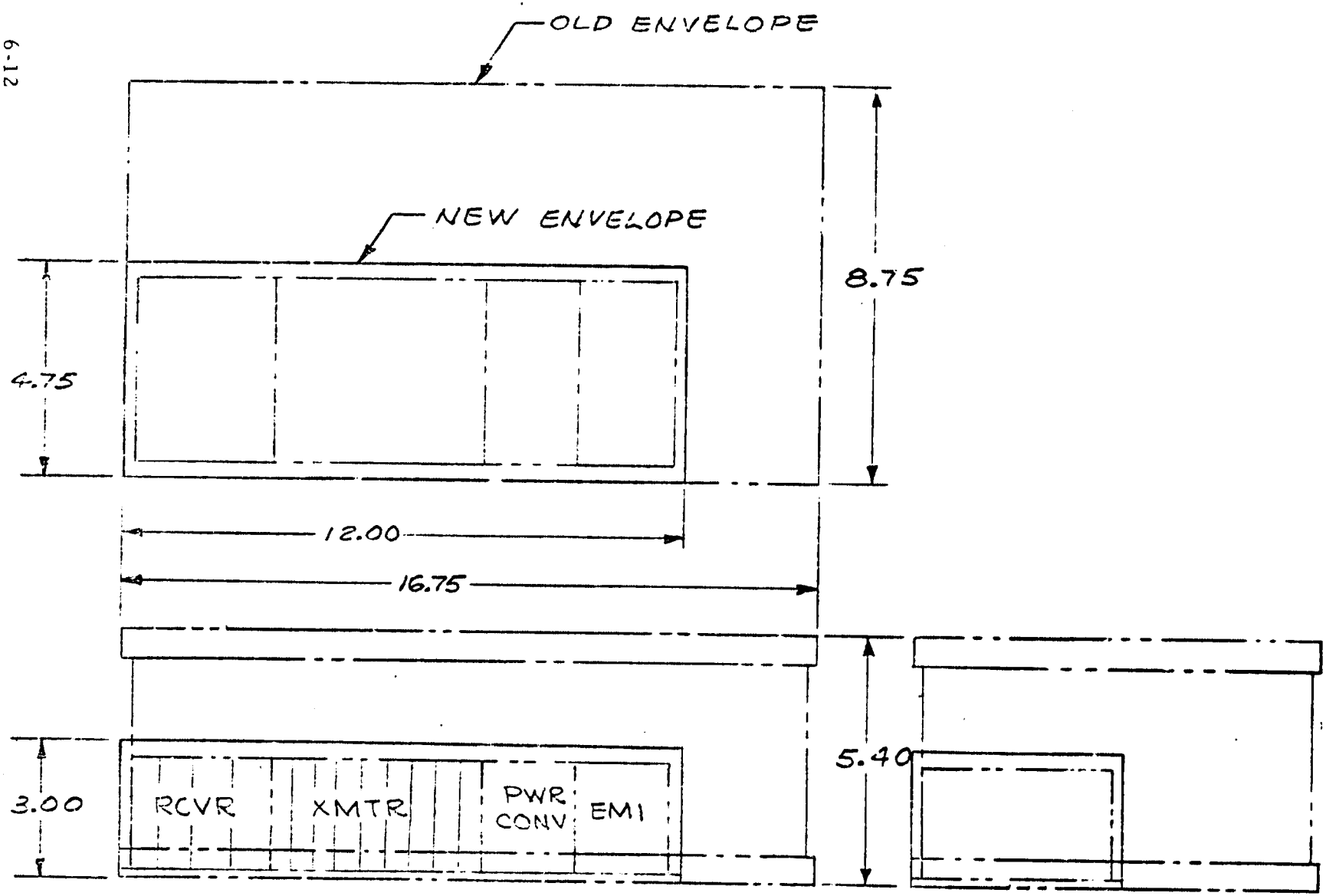


Figure 6-5.

TENTATIVE SATURN IV B
18 WATT CONFIGURATION

Table 6-1. Weight/Volume Breakdown

UNIT	SGLS			LEM			S-IVB			ADVANCED		
	Vol	Wt	Pwr	Vol	Wt	Pwr	Vol	Wt	Pwr	Vol	Wt	Pwr
Single Receiver	89.7	3.31	-	89.3	3.31	-	159.2	-	-	38	2.12	-
Single Transmitter	123	4.17	3.0	61.6	3.65	0.75	-	-	0.25	55	3.69	18.0
Overall	540	17.9	3.0	697	19.6	0.75	704	21.5	0.25	160	12.0	18.0
Configuration	Single			Redundant			Single			Single		

Vol = in^3

Wt = pounds

Pwr = RF out min. (watts)

6.2.2 Module Size

The envelopes allowed on the three existing systems permit wide latitude in selecting a standard module size. This, coupled with reduction in size obtained with higher component densities, would allow the selection of a module configuration to be almost an arbitrary choice. However, some basic ground rules were established. These are:

1. Module Complexity: The number of functions per module would be similar to Block II to avoid unnecessary complication of module testing.
2. Adaptability: A survey of recently specified envelopes would be made and a size chosen that would adapt to most of the envelopes.
3. Parts Count: A module size would be chosen that would allow about 120 to 160 discrete components per module.

The packaging approach used on the advanced transponder will allow 15 to 20 discrete components per square inch of board area. The modules used on Block II contained from 100 to 150 parts/module. The above yields a number somewhere between 5 and 10 for the number of square inches of board area required. Based on the assumptions that (1) a layout will expand to fit any area allowed, and (2) some of the circuits will be packaged utilizing chip and wire techniques, the number of square inches of board was chosen as approximately eight.

See Table 6-2 for a tabulation of the various envelopes used to select the module configuration. It is evident that a module 2-3/8 inches in height will conform to most envelopes. The selection for width is not quite so evident, however, a 4 inch wide module would fulfill the area requirements noted above. Therefore, the module size chosen is 2.38 x 4.00 overall which yields a printed circuit board area of about 8.3 in^2.

Table 6-2. Module Physical Dimensions

	Net Envelope			Height		Width	
Nomenclature	W	H	L	2-3/8"	3-3/8"	4"	5"
2 Watt Xmtr	3.25	3.38	8.75	X	X		
P-95	3.25	2.38	9.25	X			
P-110	5.75	2.38	8.75	X		X	X
1 Watt Xmtr	5.25	0.38	5.25			X	X
FM Xmtr	5.75	3.88	6.25	X	X	X	X
UHF Xmtr	5.25	1.38	4.25			X	X
TLM Xmtr	5.25	3.38	5.75	X	X	X	X
Type 13	9.95	3.88	11.25	X	X	X	X
20 Watt Xmtr	7.75	3.88	11.75	X	X	X	X
10 Watt Xmtr	5.35	1.75	8.25			X	X
2 Watt Xmtr	5.25	2.38	5.25	X		X	X
10 Watt Xmtr	7.75	3.88	11.75	X	X	X	X
LEM	4.5	7.38	16.00	X	X	X	
S-IVB	8.0	4.88	14.15	X	X	X	X
Block II	8.45	5.38	19.95	X	X	X	X
CTLI	5.25	2.38	8.75	X		X	X
Wideband	6.75	3.88	11.25	X	X	X	X
Poseidon	4.25	2.38	4.25	X		X	
SGLS	6.5	4.18	21.25	X	X	X	X
8 Watt Xmtr	3.88	2.38	3.88	X			
(20)				17	11	17	15

Gross envelopes have been reduced by the following:

1. On length and width: Allow 3/4" for Sealing Flanges.

2. On height: Allow 5/8" (1/4" for cover and base, 3/8" for interconnects)

The breadboard transmitter is currently packaged in a 3 x 4 inch module. An examination of the layouts indicates that to conform to a 2-3/8 inch height, the module containing the 70 MHz amplifier and X8 multiplier will have to be split into two modules and the module containing the 560 MHz amplifiers and phase modulator will have to be split into two modules. The functional breaks are clean and no problems are anticipated. The breadboard receiver is currently in 2 x 4 inch modules and consequently no problems are anticipated.

6.2.3 Mounting Arrangement and Typical Modules

The most advantageous mounting arrangement is one where the modules are all individually mounted to a mounting plate and heat sink as shown in Figure 6-6.

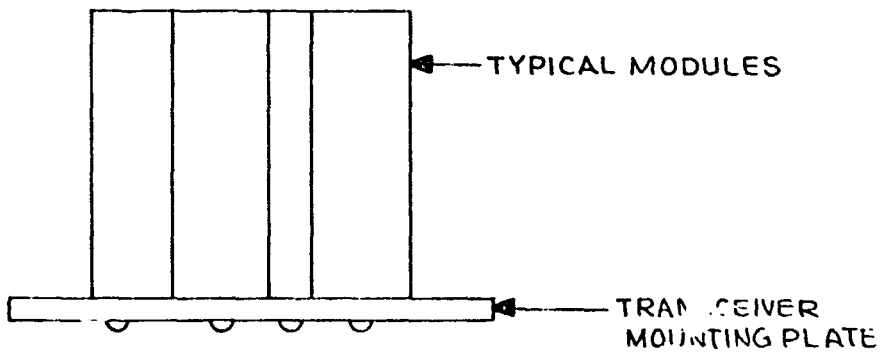


Figure 6-6. Preferred Module Mounting Arrangement

With the modules mounted in this manner, the module size being 2-3/8 x 4 inches with varying thickness and with there being nine modules for a PM transmitter and four for the basic receiver, rough layouts of the various existing transceivers using the new design are represented by Figures 6-3 through 6-5.

Typical modules are represented by Figure 6-7 for stripline modules and Figure 6-8 for foamed, printed circuit modules.

6.2.4 Component Density Comparison

As previously noted, it is possible to obtain parts densities on the order of 15 to 20 parts per square inch of board area. Layouts of the receiver modules have been made with parts densities of about 19 parts/in^2 with no particular problems.

Tables 6-3 through 6-5 represent parts densities obtained on the existing Apollo Transponders. The data for SGLS was substituted for Block II data since SGLS represented a generation beyond Block II and presumably yielded higher parts densities.

6.3 GENERAL STRUCTURAL DESIGN

All the environments specified have some effect on the design of the transceiver, however, the following environments have little or no effect on the structure.

1. Acoustic Noise: Acoustic noise has little effect on small, stiff structures although severe damage is possible on large, flat panels.
2. Fungus: The requirement that the transceiver be non-fungus nutrient has considerable effect on material selection but has no effect on the structure.
3. Explosion Proof: The requirement that the transceiver not ignite an explosive mixture is met by eliminating any switching contacts or any material that could react with the mixture. Thermal design requires surface temperatures well below the ignition temperature of the mixture. The requirement then has no effect on the structure.

The environments that must be considered are vibration, shock, acceleration, temperature, pressure and humidity. Vibration and temperature are covered in

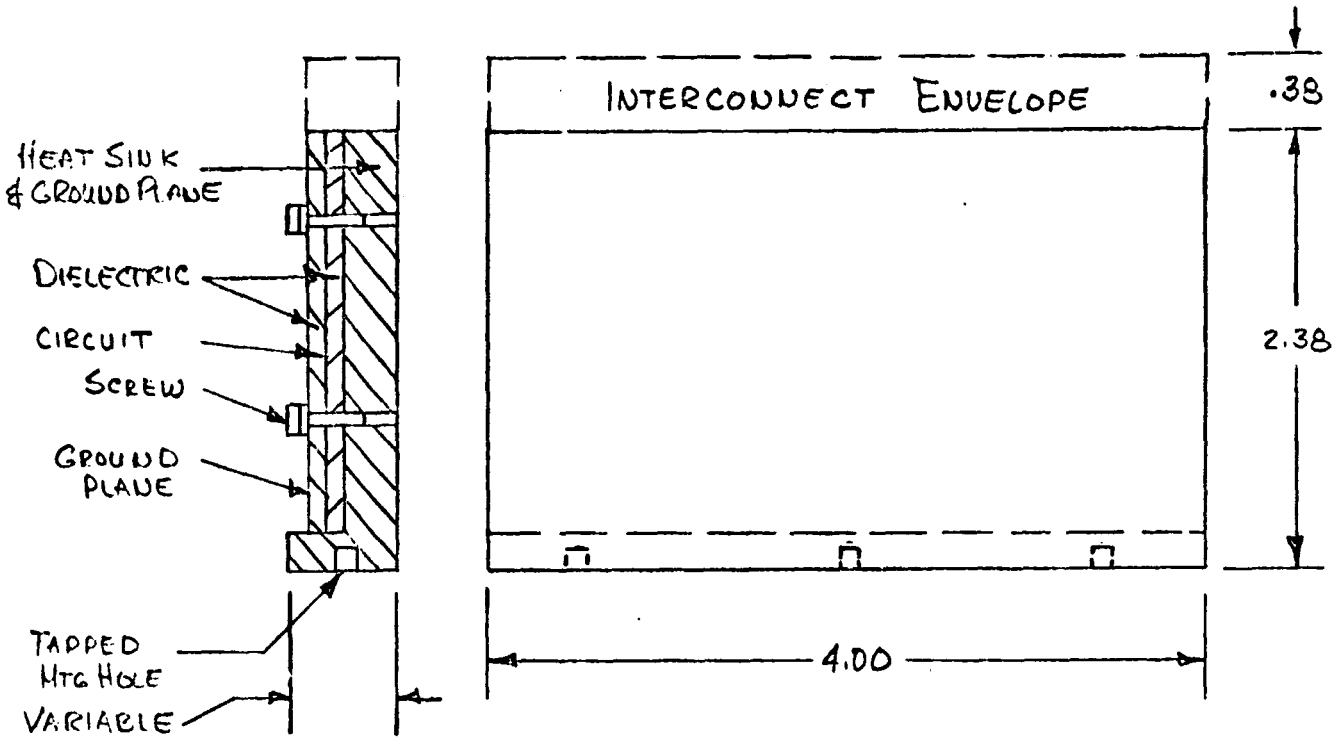


Figure 6-7. STRIPLINE MODULE

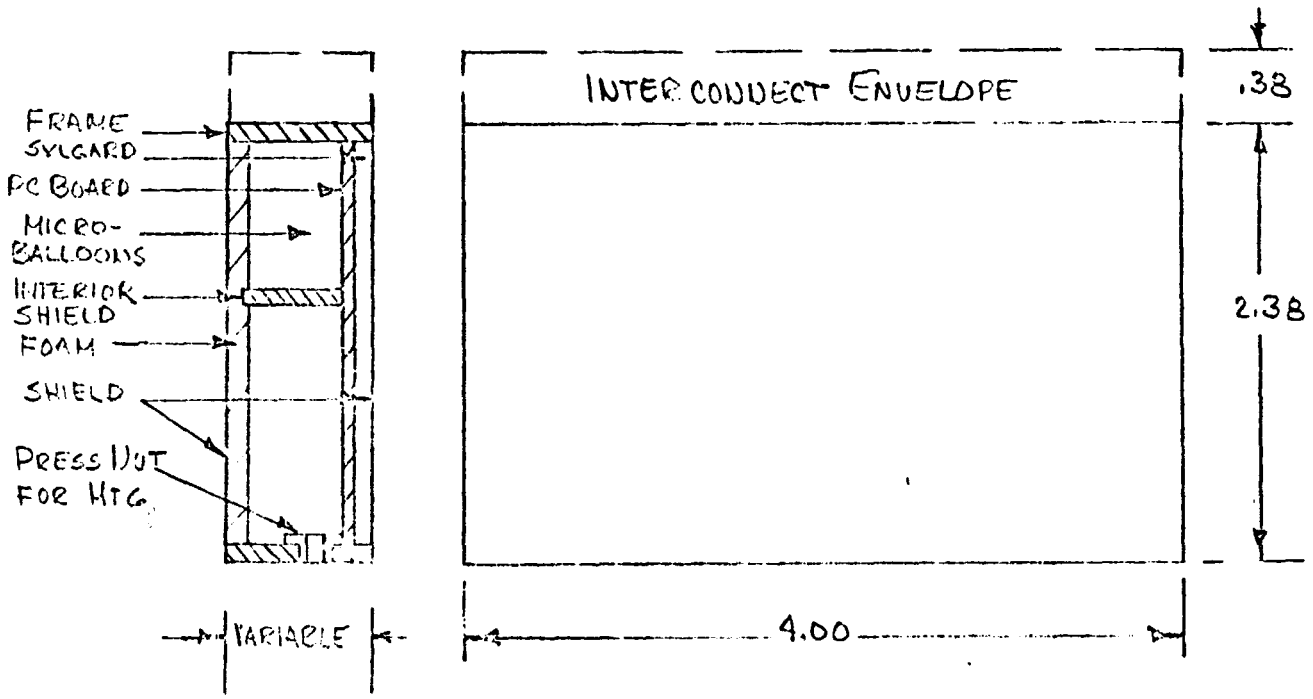


Figure 6-8. PC BOARD MODULE

Table 6-3. SGLS Transponder

RF Design	Module	Parts	Mounting Area	Module Volume	Parts in^2	Parts in^3	Total Volume	Parts in^3	Weight #	Pounds in^3
	Receiver						(3)	(3)		(3)
A1	RF Converter	65	24.2	19.0	2.7	3.4	22.9	2.8	0.49	.021
A2	Wideband Det.	144	21.9	10.6	6.6	13.6	12.8	11.2	0.38	.030
A3	Signal Cond.	159	22.2	11.8	7.2	13.5	14.2	11.2	0.34	.024
A4	IF Ampl/Mixer	169	21.9	10.6	7.7	15.9	12.8	13.2	0.42	.033
A5	Freq Synthesizer	135	22.2	11.8	6.1	11.4	14.2	9.5	0.34	.024
A6	Ref Generator	144	21.9	10.6	6.6	13.6	12.8	11.2	0 50	.039
A7	Nar. Band Det.	168	21.9	10.6	7.7	15.9	12.8	13.1	0.65	.051
A8	VCO	100	22.2	11.8	4.5	8.5	14.2	7.1	1.03	.073
A9	Pwr Converter	79	24.2	19.0	3.3	4.2	22.9	3.4	0.69	.030
--	EMI Assembly	29	17.5	7.6	1.7	3.8	7.6	3.8	0.43	.057
	Total	1192	220.1	123.4	----	----	147.2	----	5.27	----
	Average	----	-----	-----	5.4	9.6	-----	8.1	----	.036
	Rcvr Only (1)	1084	178.4	96.8	6.1	11.2	116.7	9.3	4.15	.036
	LEM Equiv. Rcvr (2)	781	134.3	74.4	5.8	10.5	89.7	8.8	3.31	.037

(1) Excludes A9 and EMI Assembly

(2) Excludes A3 and A6, no similar function on LEM

(3) Includes mounting feet and interconnections

Table 6-3. SGLS Transponder (cont)

RF Design	Module	Parts	Mounting Area	Module Volume	Parts in^2	Parts in^3	Total Volume	Parts in^3	Weight #	Pounds in^3
	Transmitter									
A1	Multiplier	27	22.0	14.5	1.3	1.8	14.5	1.8	0.69	.047
A2	Power Amplifier	47	22.0	14.9	2.1	3.2	14.9	3.2	0.83	.056
A3	Exciter/Mult	51	22.2	11.8	2.3	4.3	14.2	3.6	0.36	.025
A4	Aux Osc/Phase Mod	116	22.2	11.8	5.2	9.9	14.2	8.2	0.36	.025
A5	Pwr Converter	160	29.1	38.0	5.5	4.2	45.8	3.5	1.11	.024
--	EMI Assembly	50	14.8	16.8	3.4	3.0	16.8	3.0	0.64	.038
--	Filter	5	5.4	1.6	0.9	3.4	2.8	1.8	0.18	.064
	Total	456	187.7	109.4	---	---	123.2	---	4.17	---
	Average	---	---	---	2.4	4.2	---	3.6	---	.034
	Baseband									
A1	Power Converter	90	23.3	15.8	3.8	5.7	19.0	4.7	0.49	.026
A2	Subcarrier Cont.	67	22.4	12.6	3.0	5.3	15.2	4.4	0.32	.021
A3/A4	PRN Range Ampl.	135	21.9	10.6	6.2	12.2	12.8	10.5	0.33	.026
A5/A6	170 MHz Subcar.	75	21.9	10.6	3.4	7.1	12.8	5.9	0.27	.021
--	Pwr & Sig. Dist.	61	24.4	12.8	2.5	4.8	15.6	3.9	0.79	.051
	Total	428	113.9	295.2	---	---	75.4	---	2.20	---
	Average	---	---	---	3.7	6.9	---	5.8	---	.030

Table 6-4. LEM Transceiver

Ref Design	Module	Parts	Module Volume	Parts in^3	Total Volume	Parts in^3	Weight	Pounds in^3
					(2)	(2)		(2)
A1	Phase Modulator	195	22.6	8.6	28.2	6.9	1.056	.037
A2	Freq Modulator	208	22.6	9.2	28.2	7.2	0.744	.026
A3	RF Amplifier	176	31.5	5.6	38.5	4.6	2.374	.062
A4	Output Combiner	---	---	---	---	---	---	---
A5	Pwr Combiner	186	31.1	6.0	35.0	5.3	2.533	.072
A6	VCO	171	17.3	9.0	21.3	8.0	0.770	.036
A7	Detector	202	14.7	13.7	18.4	11.0	0.678	.037
A8	9.5 MHz IF Ampl	229	20.0	11.4	24.6	9.3	0.843	.034
A9	47.5 MHz IF Ampl	164	20.5	8.0	25.0	6.6	1.019	.040
A10	VCO	171	17.3	9.9	21.3	8.0	0.770	.036
A11	Detector	202	14.7	13.7	18.4	11.0	0.689	.037
A12	9.5 MHz IF Ampl	229	20.0	11.4	24.6	9.3	0.843	.034
A13	47.5 MHz IF Ampl	170	20.5	8.0	25.0	6.6	1.032	.041
A14	EMI Assembly	72	23.5	3.1	23.5	3.1	1.116	.047
A15	Pwr Converter	186	31.1	6.0	35.0	5.3	2.533	.072
	Total	2561	307.4	---	367	---	17.000	---
	Average	---	---	8.3	---	7.2	---	---
	Rcvr Only (1)	766	72.5	10.8	89.3	8.7	3.31	.037

(1) Single receiver consists of A6, A7, A8, A9.
(2) Includes mounting and interconnections.

Table 6-5. Saturn IV-B Transponder

Ref Design	Module	Parts	Mounting Area	Module Volume	Parts in^2	Parts in^3	Total Volume (2)	Parts in^3 (2)
A1	RF Converter	46	7.82	4.85	5.9	9.5	6.4	7.2
A2	Preamplifier	97	19.00	16.34	5.1	5.9	19.1	5.1
A3	1st IF Amplifier	106	21.44	16.34	4.9	6.5	19.1	5.5
A4	2nd IF Amplifier	103	26.00	16.34	3.8	6.1	19.1	5.4
A5	ϕ Det/Loop Filter	81	21.44	16.34	3.8	5.0	19.1	4.2
A6	VCO	118	25.67	16.34	4.6	7.2	19.1	6.2
A7	Freq. Divider	121	21.50	16.34	5.6	7.4	19.1	6.3
A8	Ampl/Detector	114	23.46	16.34	4.9	7.0	19.1	6.0
A9	ϕ Det/Modulator	112	19.29	16.34	5.8	6.8	19.1	5.9
A10	Command Demod.	106	27.20	16.34	3.9	6.5	19.1	5.5
A11	Aux. Osc.	119	23.06	16.34	5.2	7.3	19.1	6.2
A12	Freq Mult/Xmtr	170	35.00	32.80	4.9	5.2	39.0	4.4
A13	Power Converter	134	77.58	44.82	1.7	3.0	46.5	2.9
A14	SCO & Biphase Mod	65	29.63	16.34	2.2	4.0	19.1	3.4
A15	TLM Iso. Ampl.	---	---	---	---	---	---	---
	Total	1492	377.05	700.00	---	---	302.0	---
	Average	---	---	---	4.1	5.7	---	4.9
	Rcvr Only (1)	898	185.6	135.7	4.8	6.6	159.2	5.7

(1) Receiver only is A1 thru A9

(2) Includes mounting and interconnections.

separate areas and pressure/humidity are covered in the general discussion on the housing.

The steady state acceleration level of 100 g's and the maximum single degree of freedom response to the 78 g sawtooth shock of about 100 g's are significant but they are less severe than the vibration load of 186 g's (3σ value from Figure 6-2) that would be used in any stress analysis and therefore test and analysis was limited to vibration for this program. Since no housing was developed on this program, test and analysis of vibration was limited to the module level.

Since no housing was developed, no stress analysis was made as it is the housing and its mounting that are critical in terms of allowable stress levels. Thermal considerations tend to make the modules and their supporting hardware vastly oversized in terms of allowable stress levels and need not be analyzed.

6.3.1 Vibration

6.3.1.1 Transmitter Modules

With the modules mounted in the manner shown in Figure 6-6, it is necessary to restrain the unsupported long edge of the module to obtain adequate vibration characteristics in a plane normal to the plane of the modules. Figures 6-9 and 6-10 are transmissibility curves taken from two mockups of a typical transmitter module. The combination of low resonant frequency and high transmissibility results in large displacements (approximately $\pm .05$ inch for a 3 g input) which are unsatisfactory in electronic equipment.

The methods for restraining the unsupported edge of the module range from no support (as represented above) to a rigid support. A rigid support could be expected to yield an increase in resonant frequency, provided that some of the modules being tied together are of stiffer construction, but very little decrease in transmissibility. Figures 6-11 and 6-12 show the results of rigidly tying two modules together where one has a 1/16 inch heat sink and one has a 3/16 inch

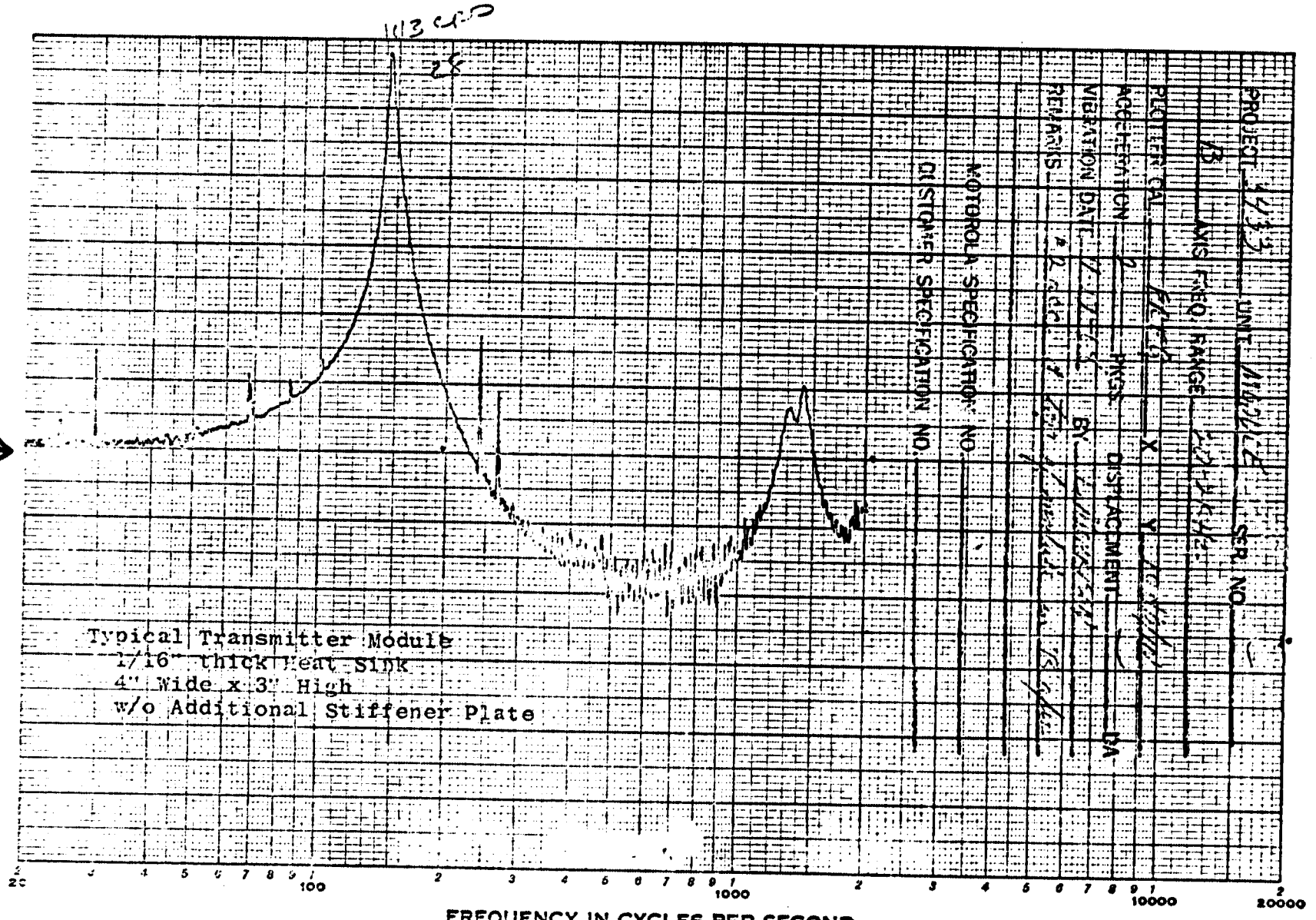


Figure 6-9. Unstiffened Transmitter Module

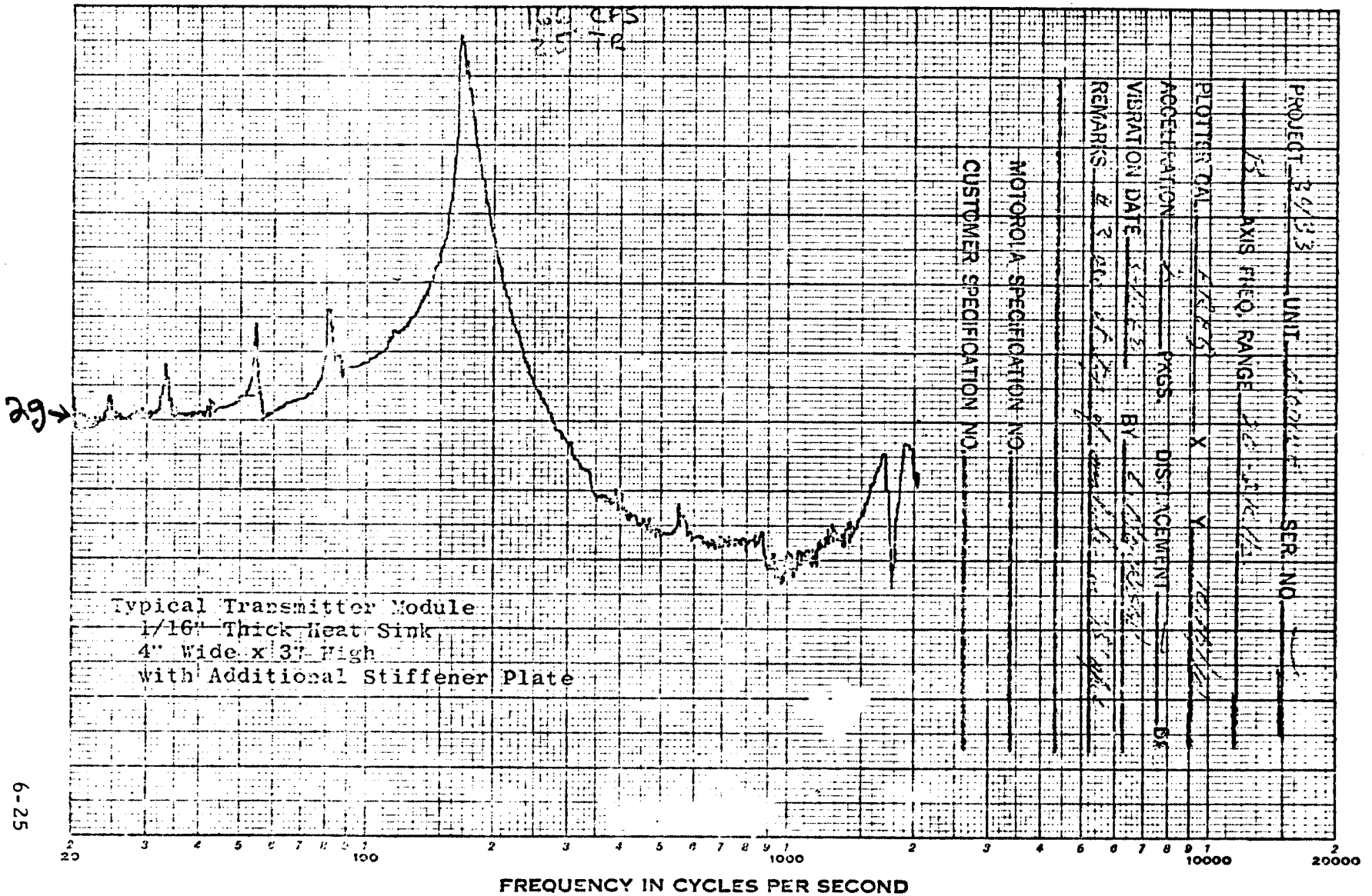


Figure 6-10. Stiffened Transmitter Module

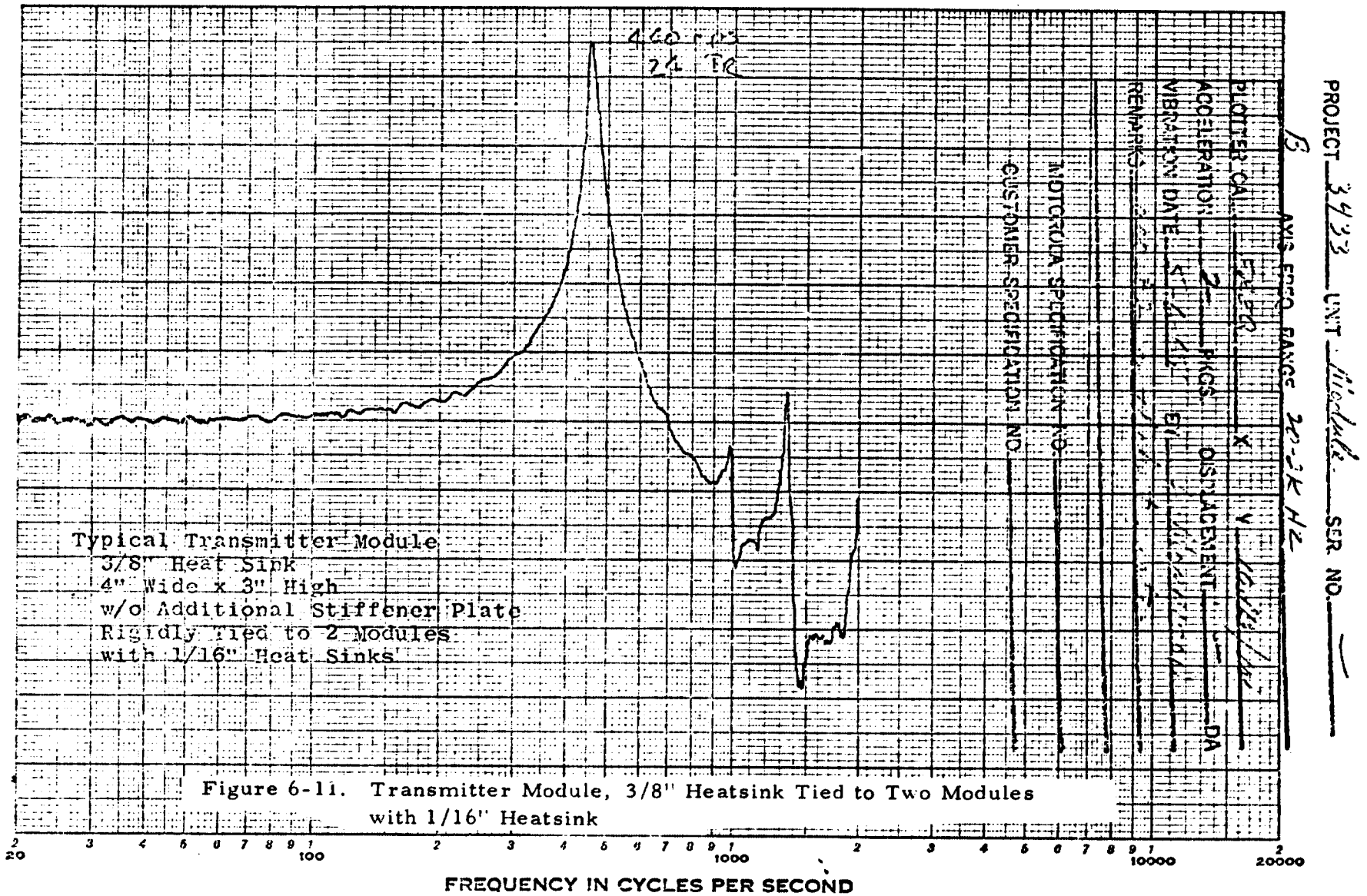


Figure 6-11. Transmitter Module, 3/8" Heatsink Tied to Two Modules with 1/16" Heatsink

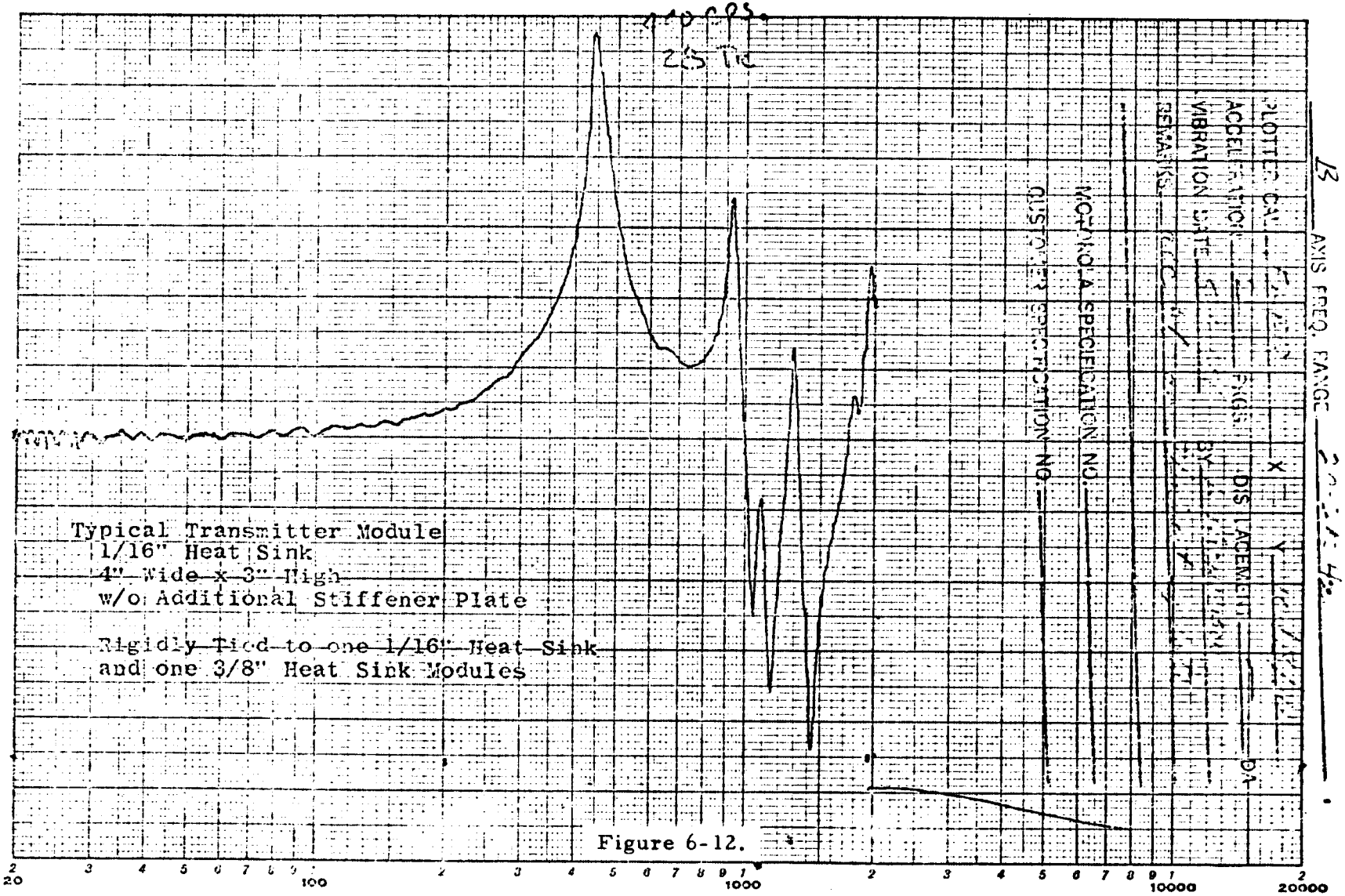


Figure 6-12.

Figure 6-12. Transmitter Module, 1/16" Heatsink Tied to One 1/16" Heatsink and One 3/8" Heatsink

thick heat sink. This represents a more satisfactory arrangement than no support at all due to the higher resonance since the transmissibility remained essentially unchanged. The displacement has been reduced to about ±.005 for a three g input.

The recommended method of support is one where the resonance can be raised and the transmissibility reduced. This can be achieved by the use of a resilient support. Figures 6-13 and 6-14 show the results of the use of such a system. The displacement remains at ±.005 for the 3/16" heat sink module but has been reduced to ±.002 for the 1/16" heat sink module for a 3 g input.

The method used to obtain the damping was simple but effective and requires only 2-3/8" diameter areas on each module. Figure 6-15 shows a cross section view of the isolation system. Further refinement in choice and size of materials will probably yield a more effective system. Some degree of improvement is also available in the location and quantity of supports used.

6.3.1.2 Receiver Modules

Most of the testing was based on transmitter modules, however, the results can be applied to the receiver modules. It can reasonably be expected that similar tests on a receiver mockup will yield similar results. The major difference that will occur is a shift in resonance point to around 1000 Hz. The shift in resonance will occur for several reasons:

1. The resonant frequency is greatly influenced by the end conditions at the mounting surface. The receiver modules are much wider than the transmitter modules with the result that the end condition looks more built in than simply supported with a resulting increase in resonant frequency.

2. The receiver modules are of a stiffer and lighter weight construction than the transmitter module. The increase in stiffness, and the reduction in mass will also tend to increase resonant frequency.

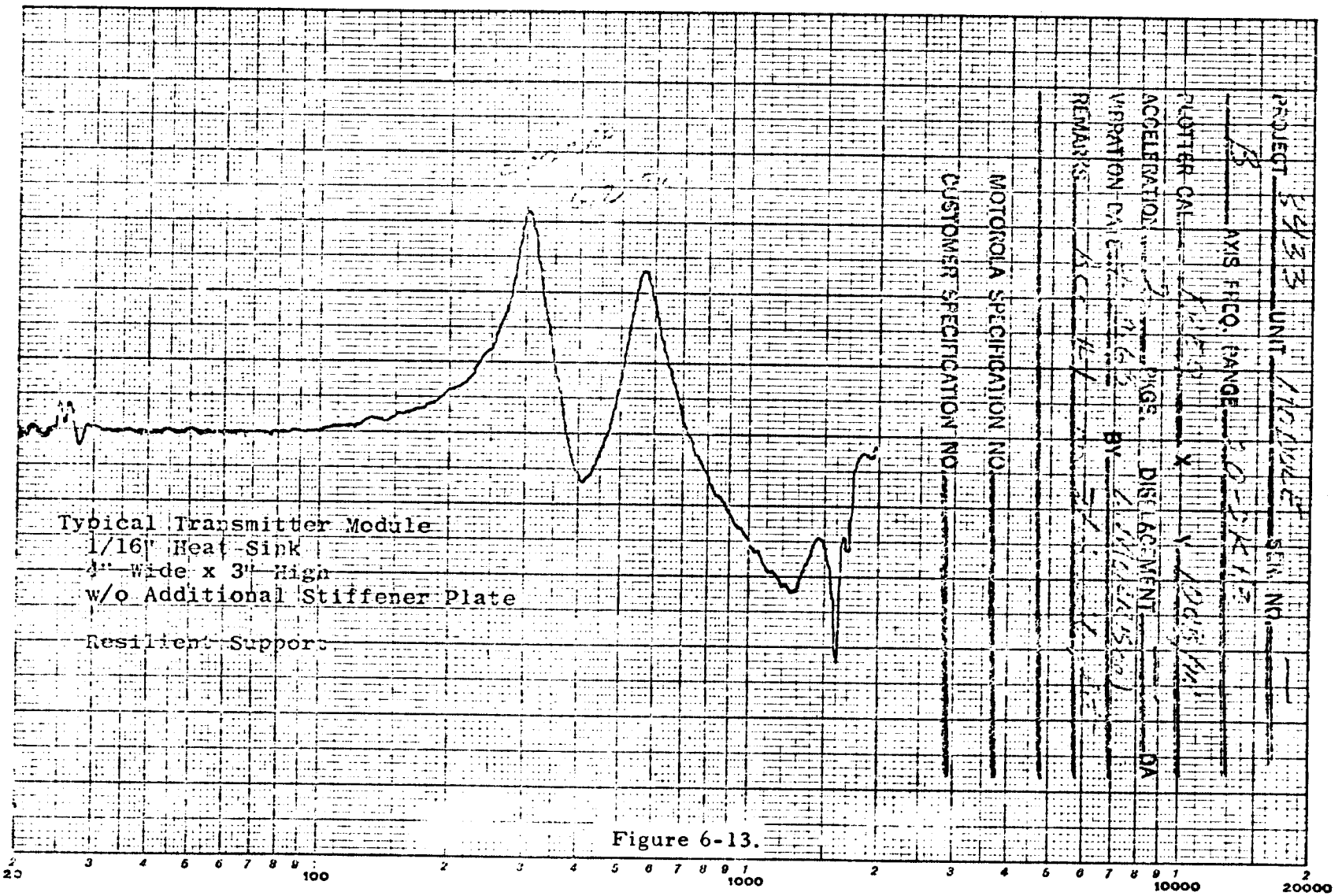


Figure 6-13.

Figure 6-13. Transmitter Module, Resilient Support, 1/16" Heatsink

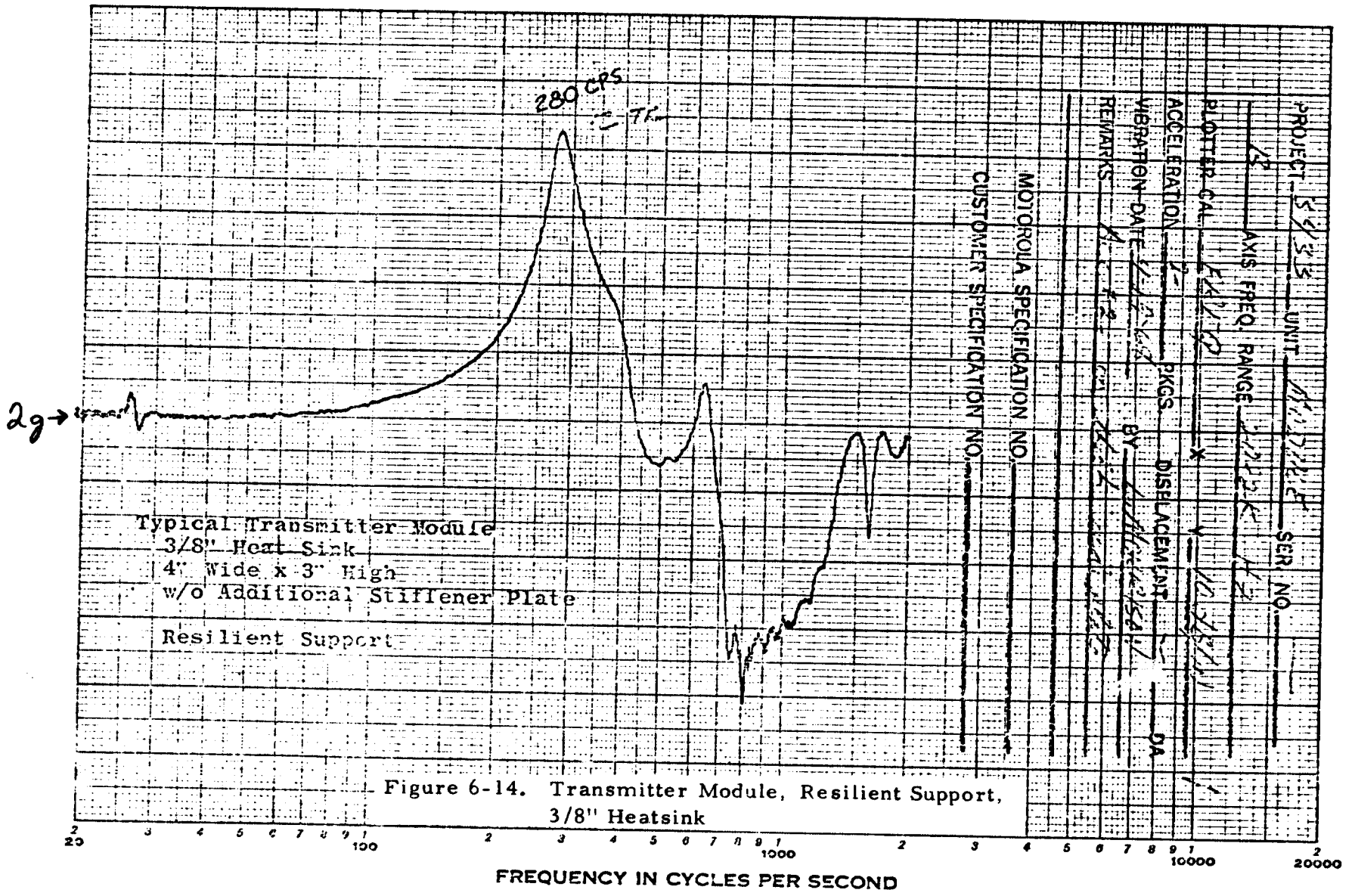


Figure 6-14. Transmitter Module, Resilient Support, 3/8" Heatsink

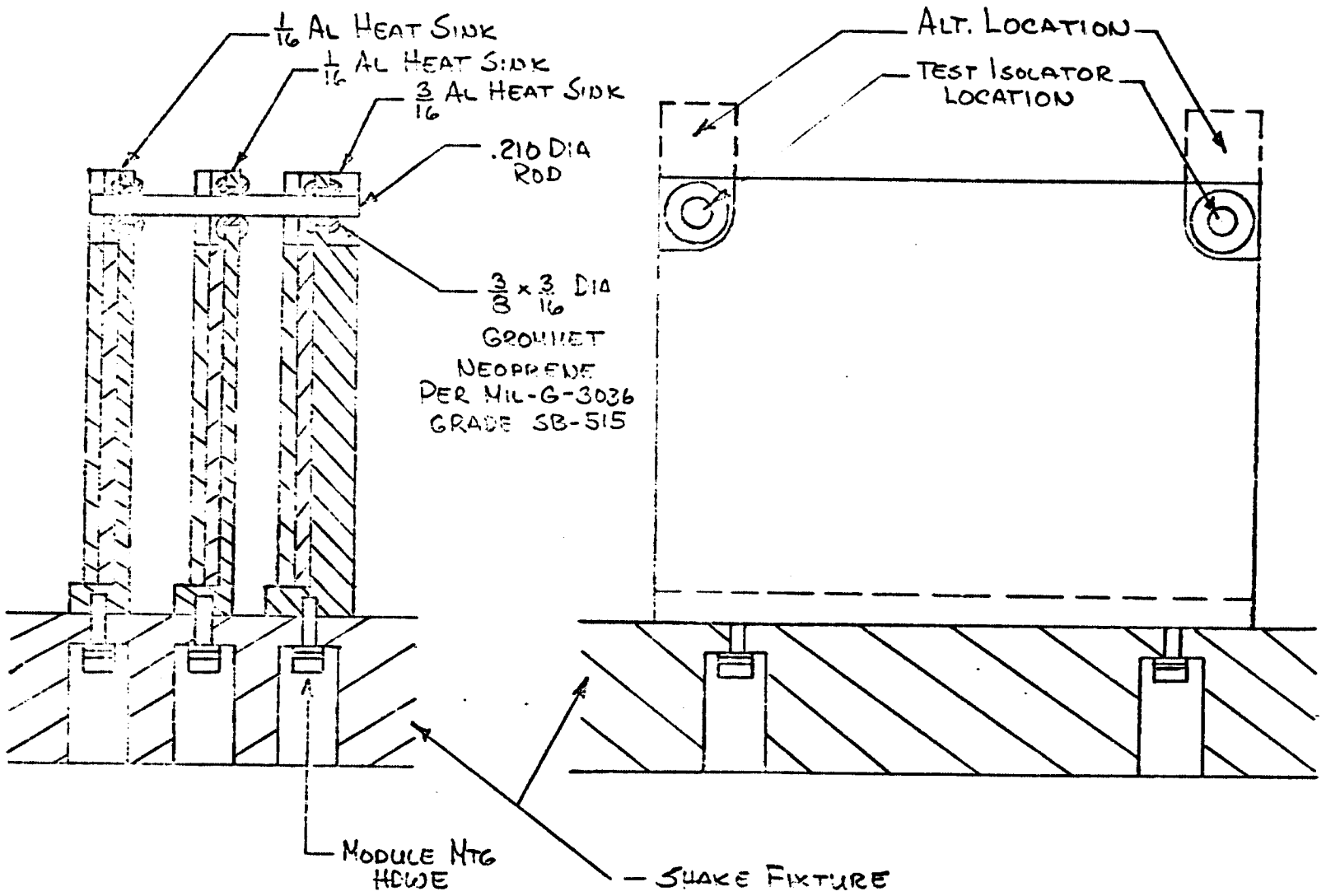


Figure 6-15. TRANSMITTER MOCKUP W/RESILIENT SUPPORT

6.3.1.3 Foaming

The use of foam as a means of supporting circuitry has been well established. It is desirable because it provides a rigid light weight structure that will survive in some of the more severe dynamic environments. On the Apollo Transponders, a rigid, CO_2 blown, polyurethane foam with density in the 6-9 lb/ft^3 range was used. The foam was chosen primarily for its excellent dielectric properties.

The use of stripline in the higher frequency portions of the transmitter has considerably eased the need for the use of a foam with extremely good dielectric properties. It is now possible to consider the use of other techniques that will reduce the cost and maintainability problems inherent in the use of a blown foam and at the same time yield improved dynamic response characteristics.

The encapsulation system that is recommended is one that utilizes loose, phenolic microballoons and a syntactic foam. A module encapsulated with this system will have a cross section similar to that shown in Figure 6-16.

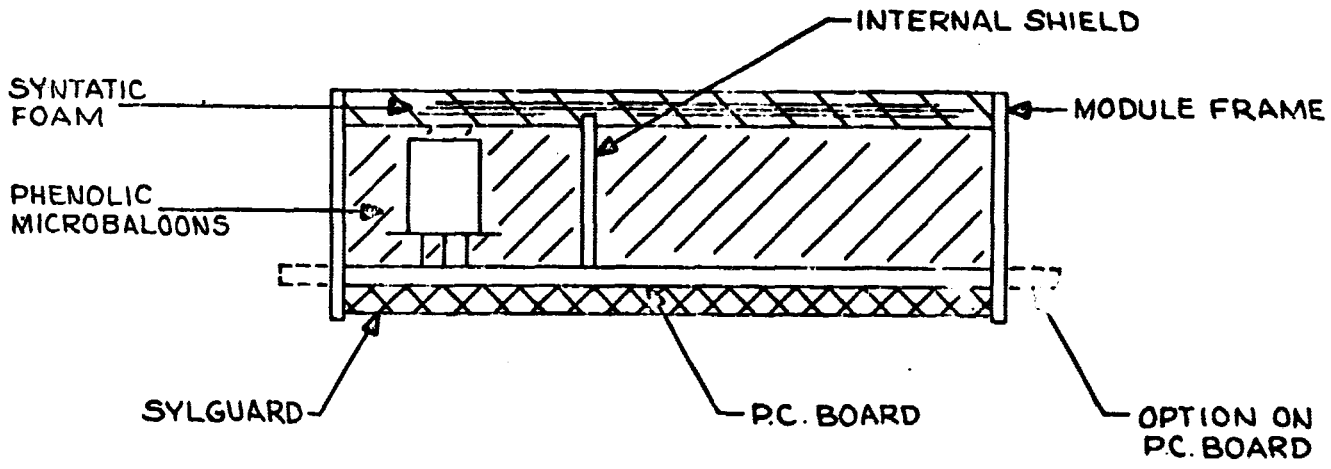


Figure 6-16. Recommended Module Encapsulation System

The use of loose microballoons has two advantages. The first is that rework is simplified and the possibility of damage during a repair or rework cycle is greatly reduced. The second, and perhaps the most important, is that the loose microballoons provide damping during vibration which gives lower G levels on the components.

Figure 6-17 is a transmissibility curve taken from a module mockup entirely encapsulated with a syntactic foam. Resonance occurred at 1400 Hz with a transmissibility of 10. Figure 6-18 is a transmissibility curve for the same mockup using loose microballoons and syntactic foam. Resonance occurred at 1300 Hz with a transmissibility of 5.5 which represents a reduction in G levels of about 50%.

The chief purpose of the syntactic foam is to provide a rigid cover to restrain the loose microballoons. In order for the syntactic foam to survive handling, it must be conformally coated to provide a film that will withstand abrasion since the individual cells do not adhere well to each other.

6.3.2 Thermal Design

The most severe environment from a design standpoint on any hi-rel program is generally the thermal environment. This usually becomes the design criterion due to a severe restriction on semiconductor junction temperatures coupled with the need for an extremely light weight system. As a general rule, low junction temperatures will require mass in excess of that required to fulfill structural requirements.

6.3.2.1 Receiver

No particular problems are expected in the receiver since the techniques used in packaging are generally similar to those used on the Block II CSM Transponder and power dissipation is lower. The transmitter and power supply will present the most difficulty; however, since no power supply was developed for this program, thermal analysis was limited to the transmitter.

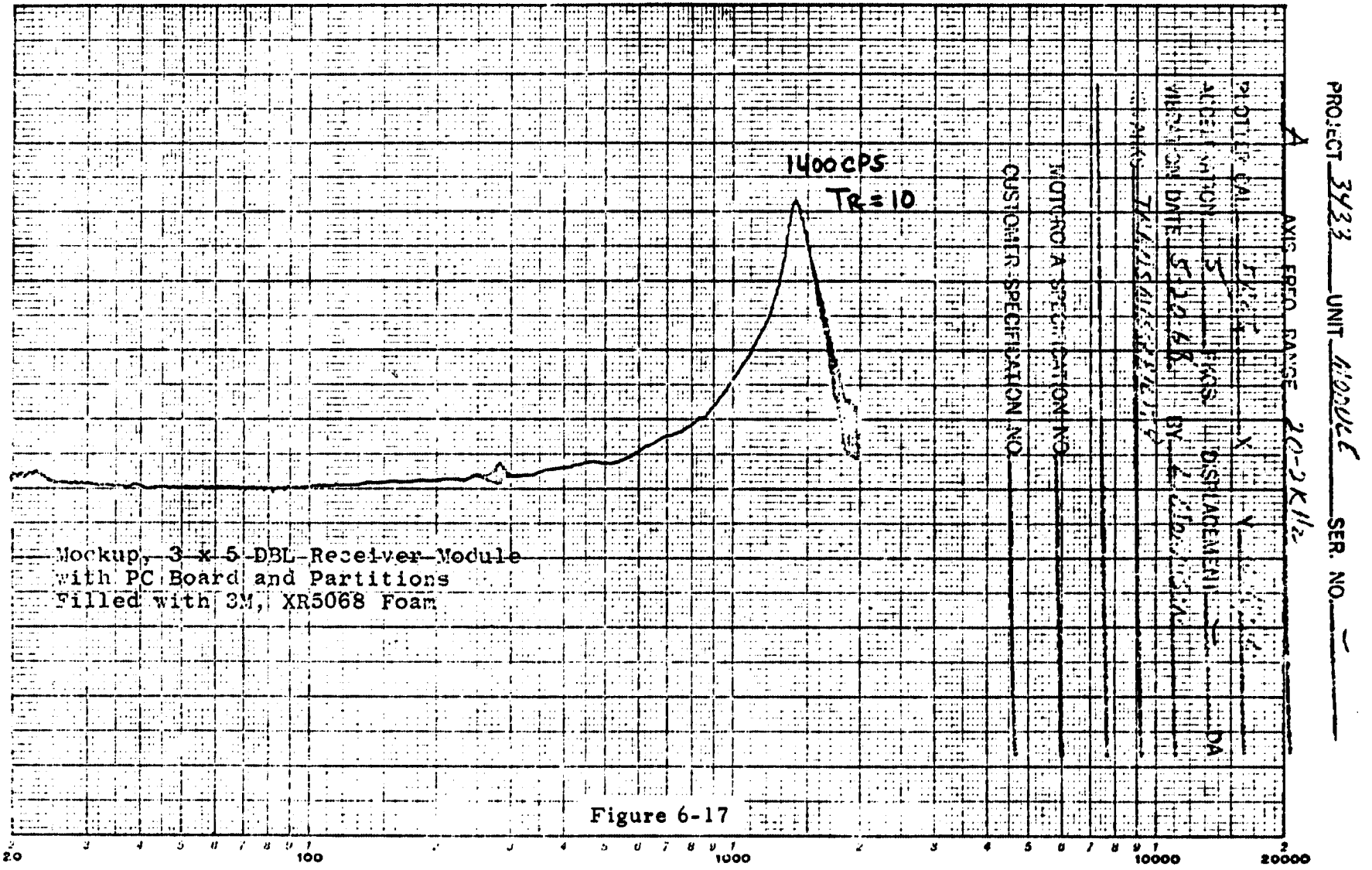
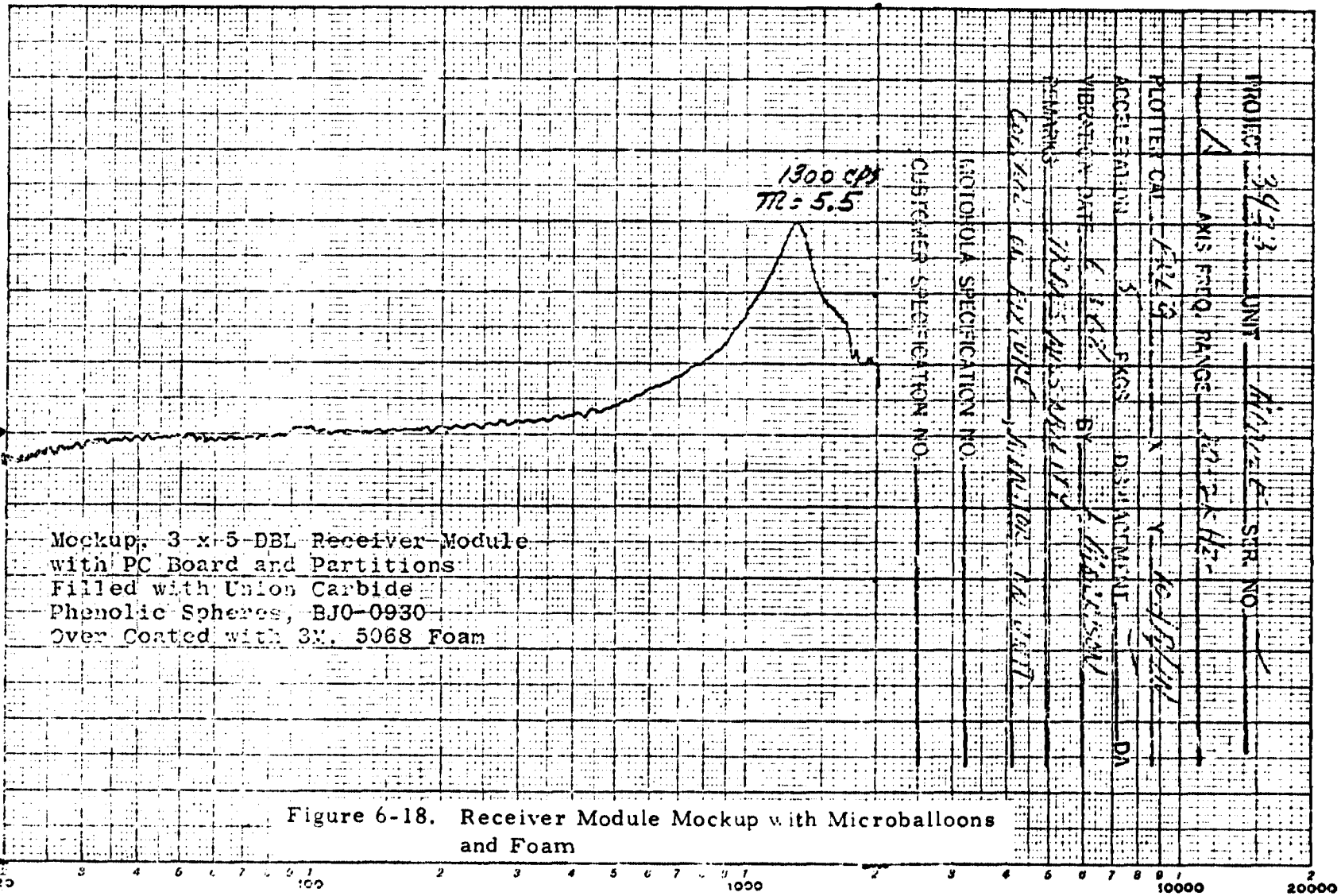


Figure 6-17

Figure 6-17. Receiver Module Mockup Foam Encapsulated



Mockup, 3-x-5-DBL Receiver Module with PC Board and Partitions Filled with Union Carbide Phenolic Spheres, BJO-0930 Over Coated with 3M, 5068 Foam

Figure 6-18. Receiver Module Mockup with Microballoons and Foam

6.3.2.2 Transmitter

The dual amplifier module presents the worse thermal problem due to the high dissipation (20 watts) and a high case to junction rise (θ_{jc} = 4.8°C/watt) for the PT6694 transistors. Since there is nothing that can be done through packaging to reduce the case to junction temperature rise, it is essential that all other temperature rises affecting junction temperature be minimized.

Taking the mounting plate for the modules as a reference point, the temperature rise to the semiconductor junction is expressed as:

$$\Delta_t = \Delta_{t_1} + \Delta_{t_2} + \Delta_{t_3} + \Delta t_{c-j}$$

where Δ_t = rise of junction to sink

Δ_{t_1} = rise at module/sink interface

Δ_{t_2} = conduction rise from base of module to transistor heat sink

Δ_{t_3} = sink/case rise for transistor mounting

$\Delta_{t_{c-j}}$ = case to junction rise

Figure 6-19 shows that except for Δ_{t_2} all temperature rises are essentially constant. Δ_{t_2} can be varied by two methods: (1) By increasing the area in the thermal path and/or (2) by using a material with a higher thermal conductivity. Figure 6-19 shows the effect of both of the above variables on the overall mounting plate to junction rise.

Another item to be considered is the effect on weight and dynamic response due to variations in the module heat sink. Figure 6-20 shows the effects, although the effect on resonance shown is for comparison only and has no relation to the absolute value since end restraints were not considered. The optimum heat sink for the dual amplifier is seen to be a 3/16 inch thick aluminum plate.

Figure 6-21 gives the expected junction temperature rises for typical devices in the transmitter. Thickness of the heat sink required to achieve these temperatures is also indicated. The absolute temperatures of the junctions are not noted, only the rise over the mounting plate. In the case of Block II CSM, it

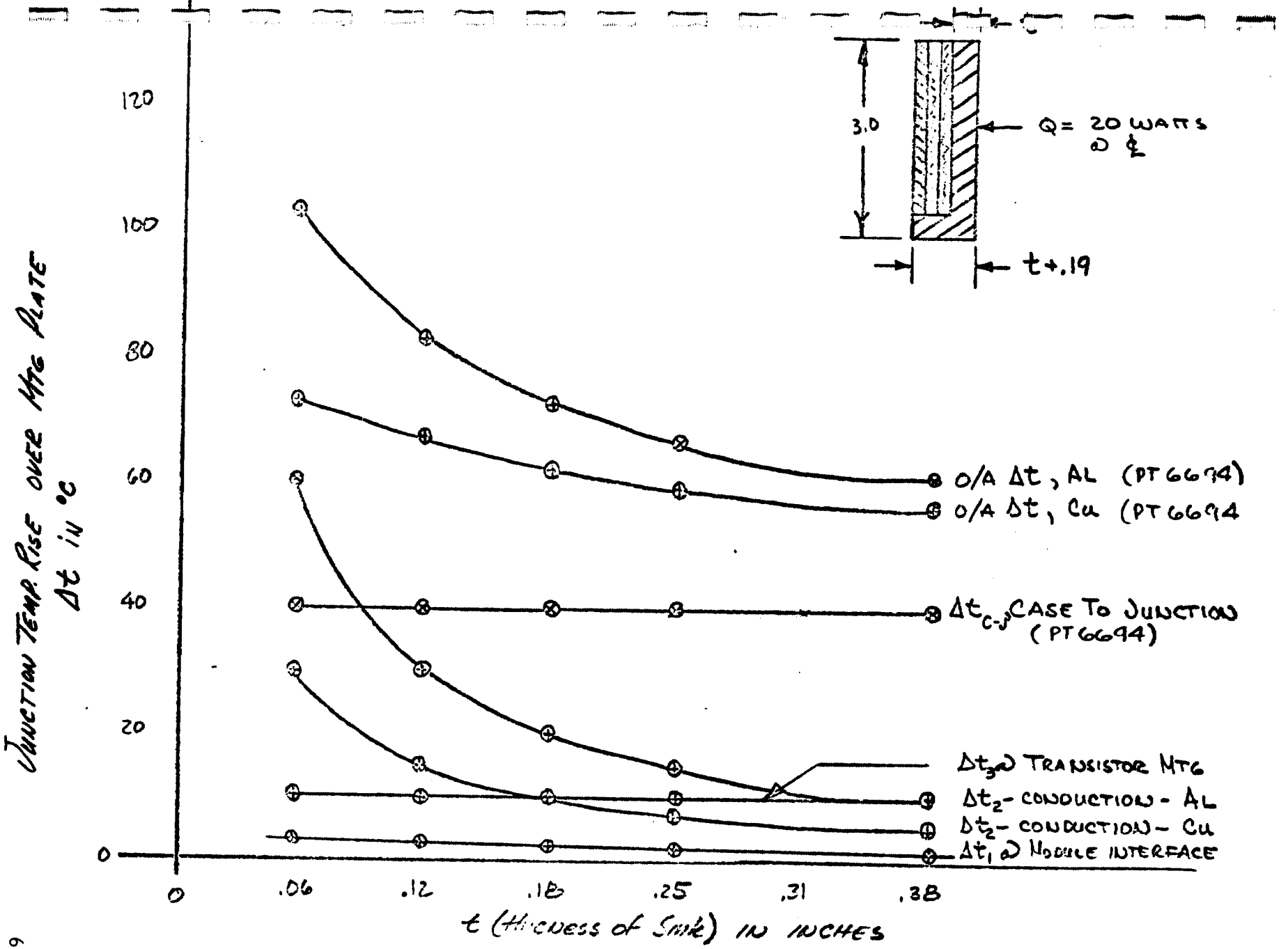


Figure 6-19. Temperature Rise vs Heat Sink Conductivity and Area

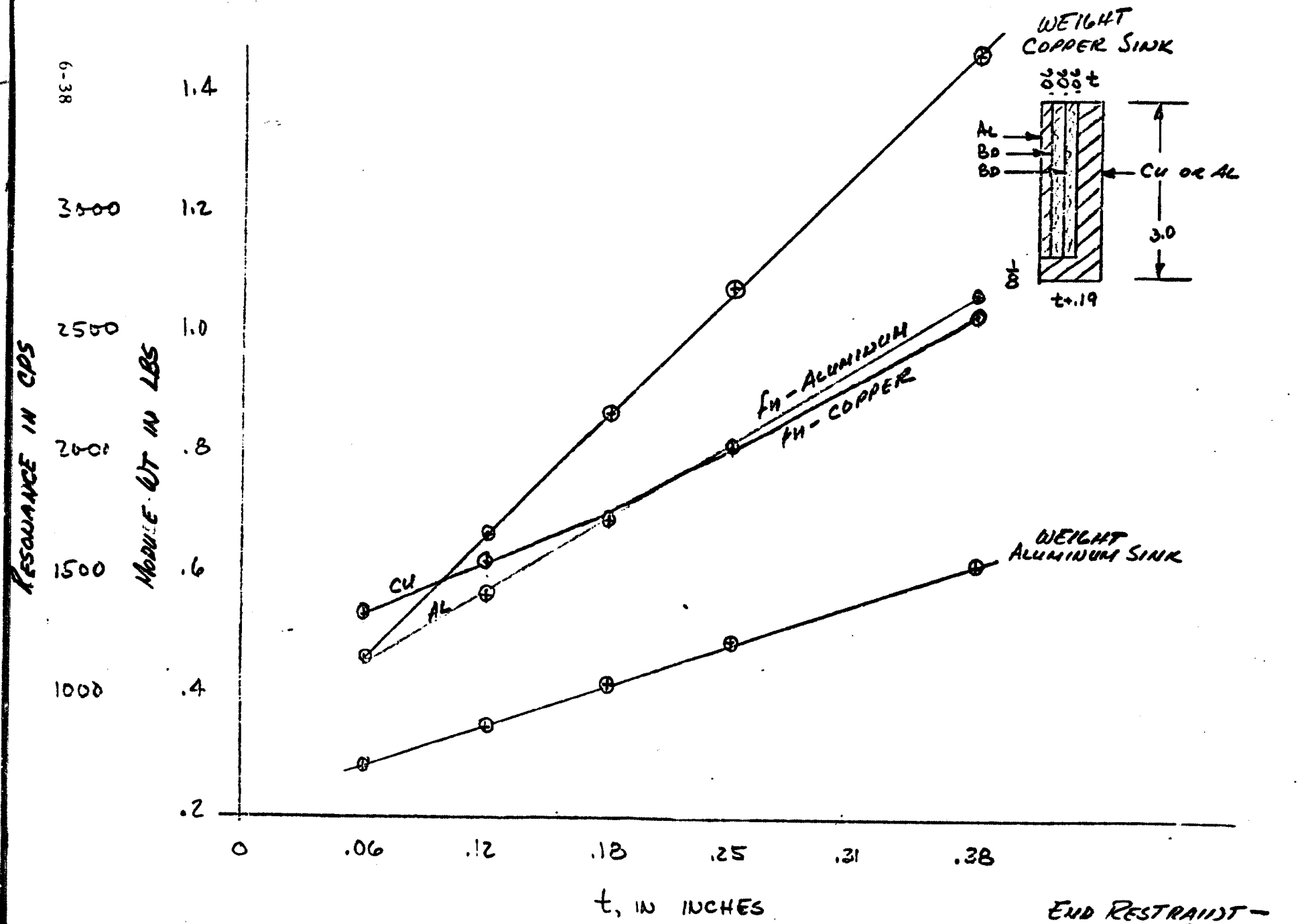
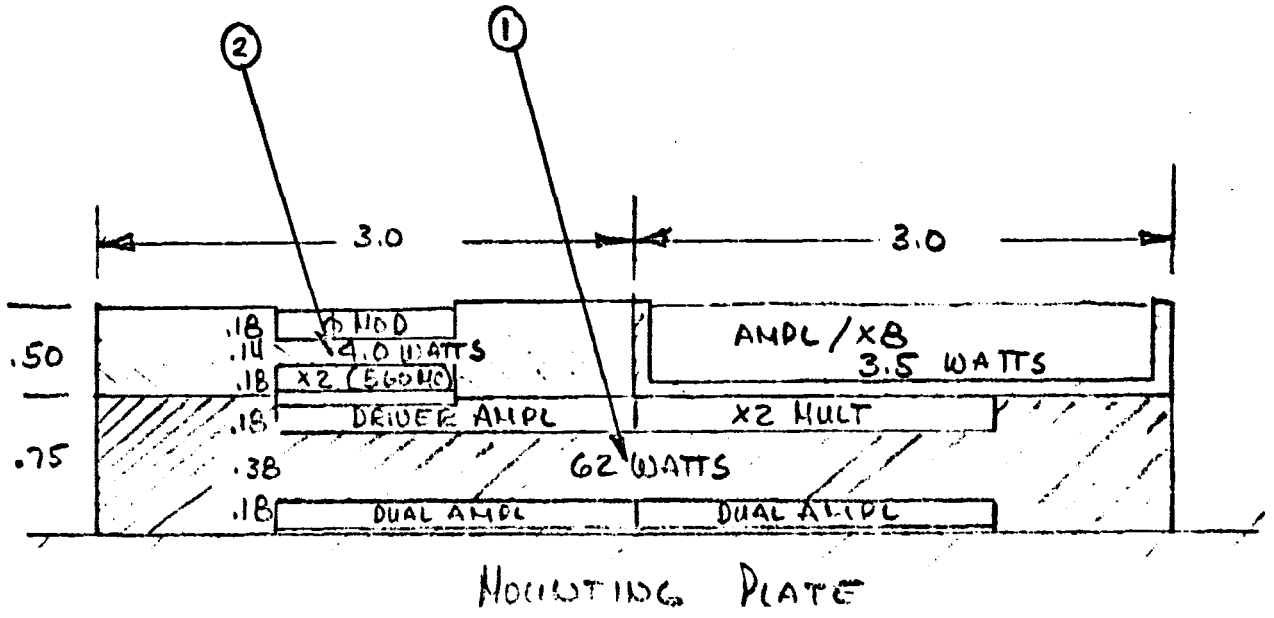


Figure 6-20. Effects of Thickness and Weight on Dynamic Response



CONDUCTIVITY OF ALUMINUM = 100 BTU/HR/FT/°F
CONTACT RESISTANCE @ JOINT = .2 °C/WATT/IN²
PT 6694 SINK TO CASE = 1°C/WATT
VAB 811 HEATSINK TO CASE = 1.9°C/WATT
PT6694 $\theta_{j,c}$ = 4.8 °C/WATT
VAB 812 $\theta_{j,c}$ = 11°C/WATT
VAB 811 $\theta_{j,c}$ = 7°C/WATT

DEVICE	MOUNTING PLATE TO JUNCTION Δt HORIZONTAL	VERTICAL (W .18 SINK)
PT6694 @ ①	82°C	76°C
VAB 811 @ ②	24° C	9.5°C
VAB 812 @ ①	73° C	64.0°C

Figure 6-21. Heat Sink Thickness and Junction Temperature Rise

does represent the rise over the heat sink temperature (62.5°F to 118°F) but for the LEM and S-IVB an additional rise due to conduction through the mounting plate to the cold rails or the mounting feet must be included. This additional temperature rise has not been calculated since it is largely a tradeoff between weight and temperature rise and can best be determined during the design phase for each specific configuration.

6.4 ALTERNATE MOUNTING ARRANGEMENTS

The module mounting methods described in paragraph 6.2.3 are recommended largely on the basis of an overall desirability. Other possible configurations were examined in order to determine their effects on size and temperature.

6.4.1 Transmitter

The limiting module in selection of a module height suitable for the transmitter has been the dual 1100 MHz amplifier. This occurs chiefly because of the couplers used to parallel devices and the necessity for maintaining phase relationships while interconnecting the individual devices.

The most desirable arrangement electrically would be for all four stages and the six 3 db couplers to be on a single board; however, this would require a module roughly 6 x 4 inches which is not compatible with most envelopes.

The other extreme, which is desirable for a maximum flexibility, is to place each device in a separate module with the input and output couplers being in separate modules as shown in Figure 6-22.

This would allow wide variation of output power by changing or eliminating the coupler modules and selecting the quantity of amplifiers desired; however, the large number of interconnecting cables with their connectors makes it extremely difficult to maintain phase relationships. An effective compromise has been achieved in the present design by the use of a dual amplifier module as in Figure 6-23.

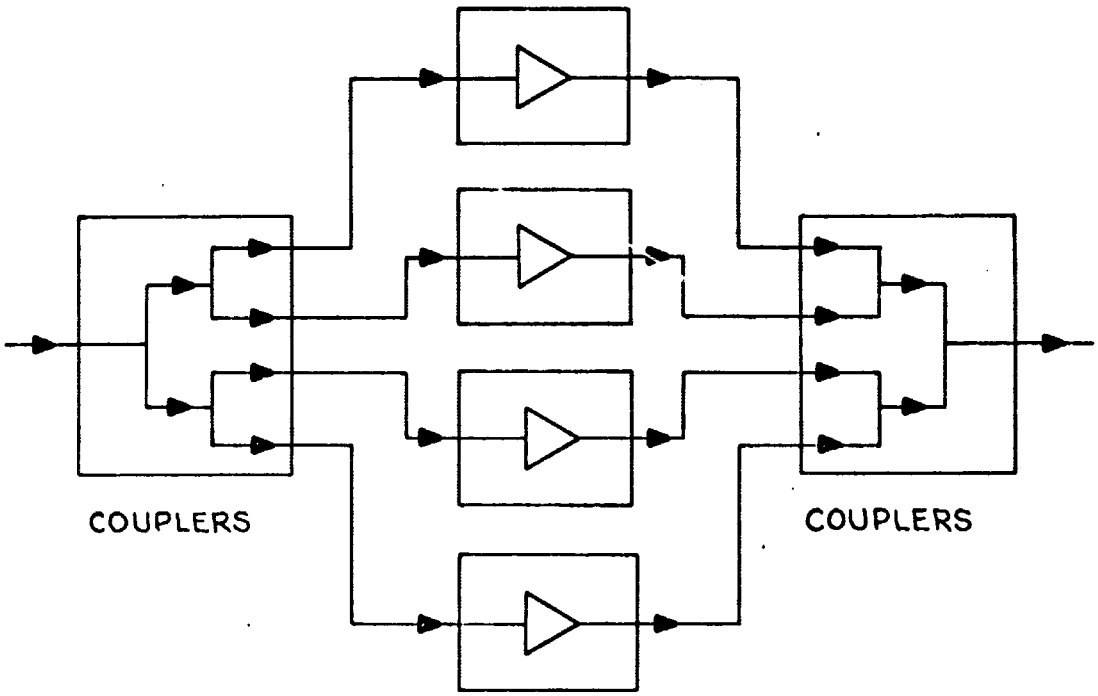


Figure 6-22. SINGLE STAGE AMPLIFIER MODULES

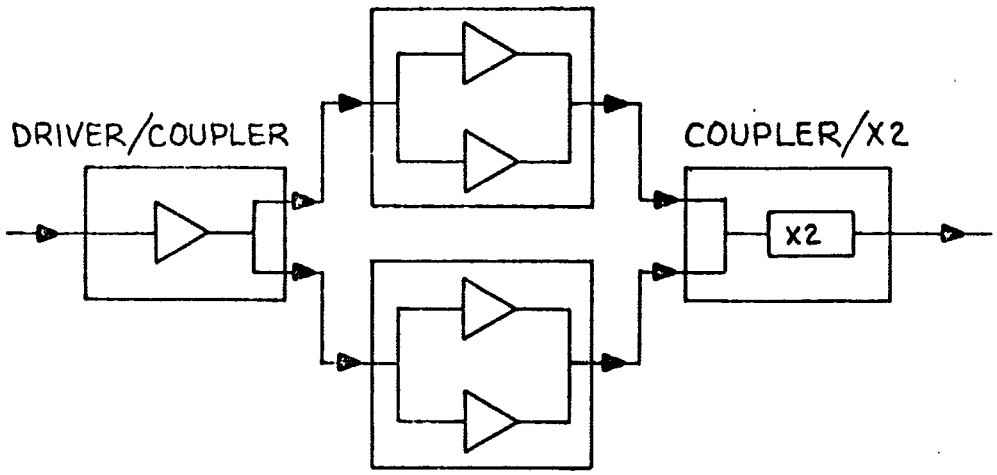


Figure 6-23. DUAL AMPLIFIER MODULES

An alternate mounting arrangement that is immediately obvious is to place all the couplers and amplifiers in a single 6 x 4 inch module and to stack the modules horizontally with respect to the mounting plate. The primary difficulty with such an arrangement is that more thermal interfaces are added and thermal conduction paths are lengthened. Figure 6-21 shows a layout based on this approach and a comparison of temperature rises in this configuration versus those expected for the recommended mounting arrangement.

It should be noted that the temperatures given are from simplified calculations. Normal design practice would be to construct a nodal temperature pattern throughout the transmitter using a three dimensional computer analysis, however, at this time the data effecting thermal design is not sufficiently well defined to justify the use of such a technique.

Other configurations were analyzed using similar comparisons. One approach involving the use of both vertical and horizontal stacking techniques would have yielded a slightly lower junction temperature for the PT6694 transistor; however, this approach was discarded because it made assembly virtually impossible. A horizontal stacking arrangement will, in general, yield a lower profile assembly at the expense of assembly time and thermal design. Such a tradeoff may be desirable under some circumstances but does not appear to be desirable for this program.

6.4.2 Receiver Modules

The receiver modules are not nearly so adaptable to variation in mounting arrangements as are the transmitter modules. They may be stacked horizontally in a manner similar to that used in the transmitter tradeoffs, however, this requires volume from the module that is not generally as available from printed circuit board modules as it is from stripline modules. The tradeoffs involved in the mounting configuration of the receiver are largely those of space, weight and cost rather than thermal since thermal dissipations are at least an order of magnitude lower for the receiver than for the transmitter.

The configuration used on the LEM Transceiver represents one of many possible versions for stacking modules (see Figure 6-24). The relative fabrication and assembly costs of LEM versus Block II modules was roughly 2:1 which makes a Block II type module very desirable. A Block II type of module could be stacked horizontally by redesigning the module as shown in Figure 6-25.

The approximately 1/2 inch chamfered corners are dictated by the #8 or #10 screws and washers required to tie down the stacked modules and also to serve as a good thermal path to the mounting plate. The slight (.007 $\pm$.005 typ) elevation at the corners is required to ensure that there is intimate contact between the interfaces in the thermal path. The reduction in area on the printed circuit board is about .5 in^2, or about a 6% reduction, or about 8-9 parts that room must be found for. The added weight represents approximately .05 lbs/module. These do not appear to be drastic penalties to pay; however, assuming a five module receiver and a redundant system as on LM and Block II will give about a 0.5 lb. increase in weight, which would have been significant on either program.

Other items to be included in consideration of a horizontal mounting arrangement are: (1) The thermal penalty of successive interfaces in the thermal path, (2) the maximum length of the tie down bolts (about 3 inches for 2000 Hz vibration) and (3) the general adaptability of the system to adding and deleting functions on an as-required basis.

Consideration of the above leads to the choice of a vertically mounted module, similar in construction to a Block II module, for use on this program. The selection is seen as being optimum from a weight, volume, cost and adaptability point of view.

6.5 SHIELDING

The packaging approach used on the CSM Block II and SGLS Transponders represents considerable improvement in cost and flexibility over LM and S-IVB Transponders, however, some improvements in shielding of modules is mandatory

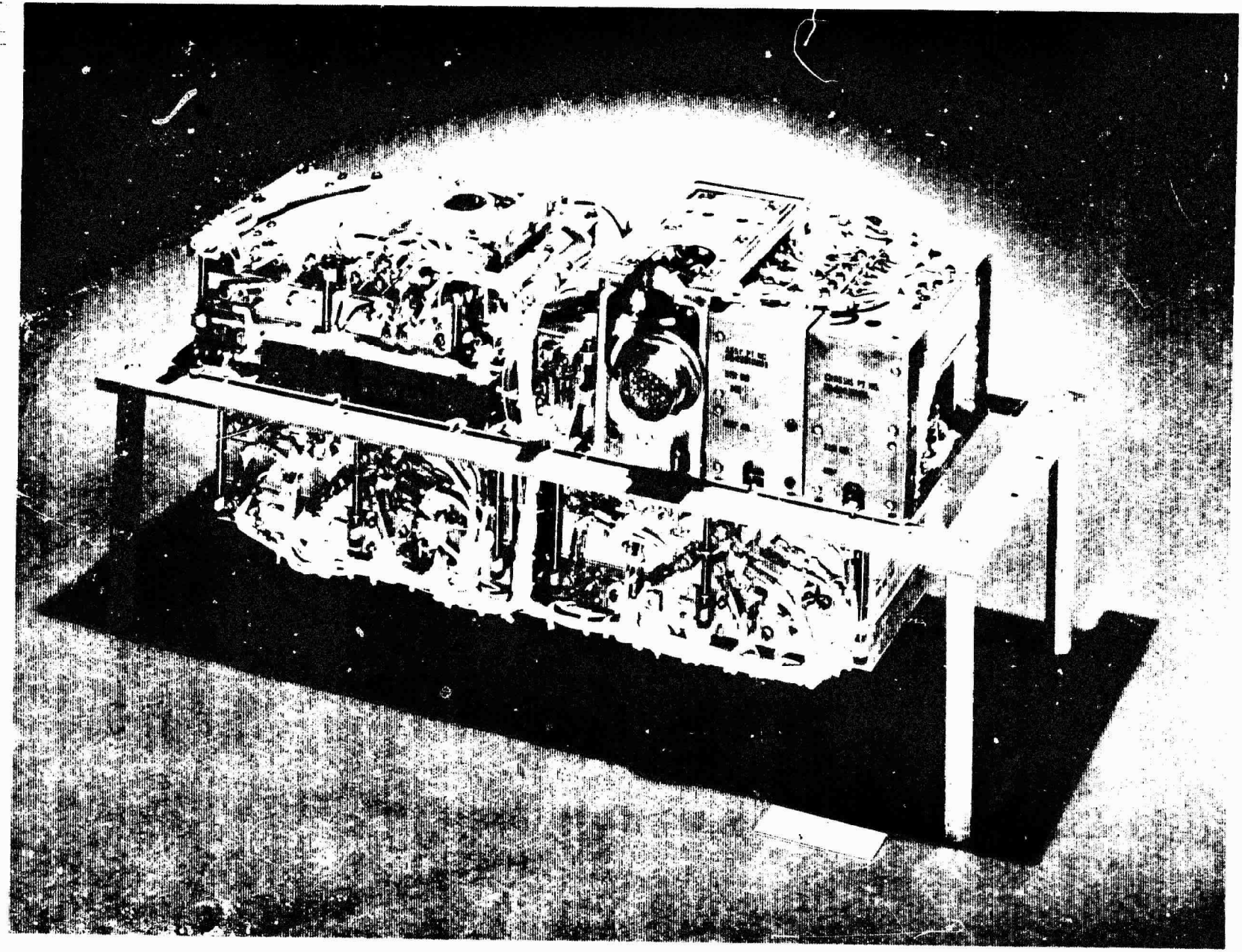


Figure 6-24. LEM Module Mounting Configuration

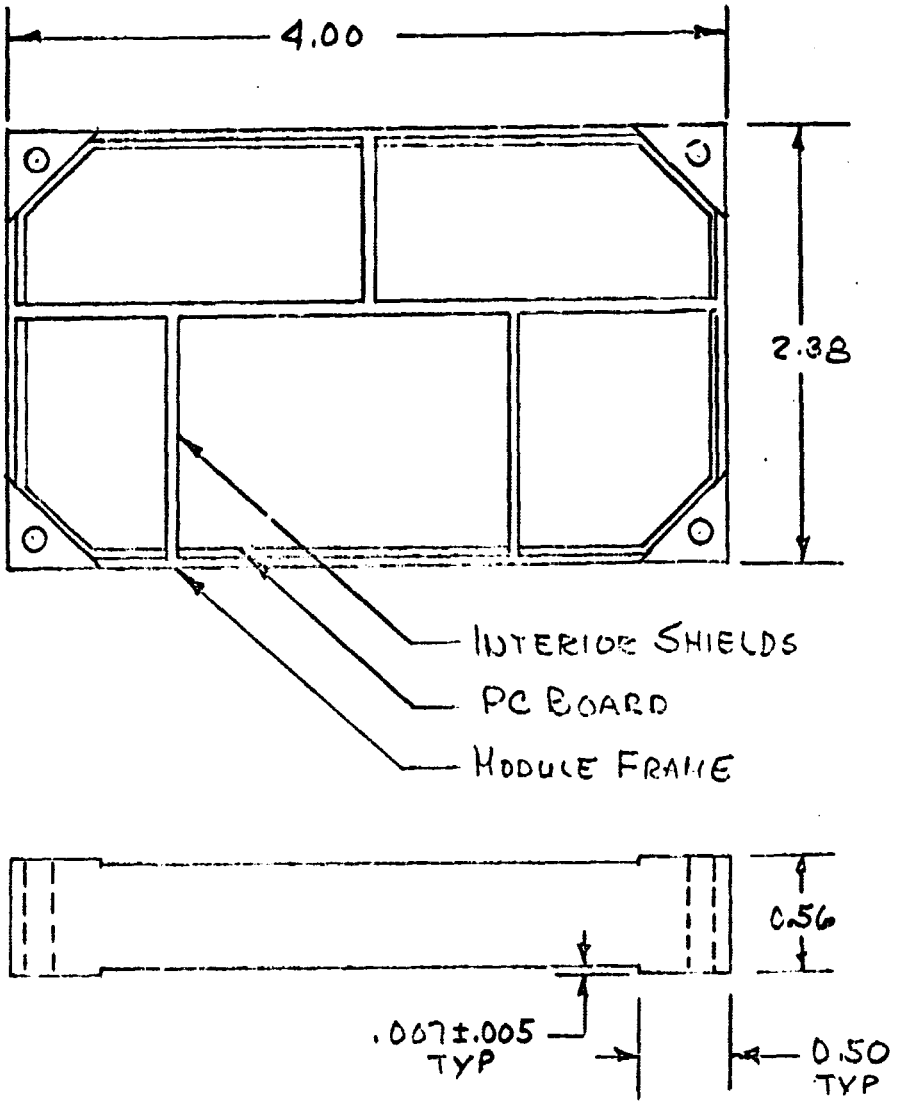


Figure 6-25. BLOCK II CSM MODULE MODIFIED FOR HORIZONTAL MOUNTING

for the single conversion receiver and a reduction in cost and weight is desirable if it can be achieved at no sacrifice in performance.

Figures 6-26 and 6-27 show the attenuation available through the use of conductive adhesive and conductive paint as used on the Block II CSM Transponder. Figures 6-28 and 6-29 give comparisons between various copper shields and the paint. Figures 6-30 and 6-31 give the attenuation available for various combinations of aluminum foil compared to the paint. It can be seen from Figures 6-30 and 6-31 that the use of aluminum foil with EC-56C will give a significant improvement in shielding.

A cursory examination revealed that a 3M aluminum foil with conductive adhesive backing had been used on space programs by other manufacturers of space hardware, however, no data was available from any source on the effects of vacuum and humidity on the foil and its adhesive.

The weight loss of the adhesive was determined to be 1.62% after four days at 10^{-6} mm Hg at temperatures between 150 to 260°F. This appears to be excessive when compared to weight loss data for other Apollo approved materials but by itself does not constitute adequate grounds for not using the foil.

The effects of humidity were determined by preparing 12 samples of two strips each and subjecting six samples to humidity with the remaining six used as control samples. The results of these tests are tabulated in Table 6-6.

The results of the humidity tests indicate the necessity of conformally coating the foil to protect it from humidity. Selection of a low outgassing coating would also serve to protect the adhesive during exposure to high vacuum, however, the test results indicate the unsuitability of the foil for shielding use due to the wide variation in resistance at DC of identical samples of foil. It was noted during the tests to obtain base line data that the resistance of any sample was extremely sensitive to any pressure on the foil or to any flexing of the sample. While resistance at DC is a poor indication of performance as an r-f shield, the indication is clear that there is considerable risk and difficulty involved in the use of the foil in an as-supplied condition.

Table 6-6. Humidity Test

Test Condition: 11 days, MIL-STD-202, Method 106

Specimen: (1) 2, 2-1/2 x 2-1/2 samples 3M X1170 Al Foil/Panel.

(2) 2, 1 x 3-1/8 samples 3M X1254 Copper Foil/Panel.

Test Panel: 1/16" Thick Aluminum Sheet, Perforated with 7/64" dia. holes on 3/32 centers, alodyne finish

Resistance: Measured at 0.1 amp DC.

Peel Strength: Weight to pull 1/2" wide strip perpendicular from test panel surface.

Sample	MTL	Test	Resistance (Ω)		Peel Strength (#)	
			Initial	Final	Strip #1	Strip #2
1	1	Humidity	1.16	0.69	1.40	1.42
2	1	Humidity	4.53	∝	1.32	1.31
3	1	Humidity	0.62	∝	1.46	1.44
4	1	Humidity	0.74	3.53	1.13	1.26
5	1	Humidity	0.32	∝	1.28	1.24
6	1	Humidity	0.97	1.68	1.42	1.45
7	1	Control	1.42	1.48	1.08	1.13
8	1	Control	0.29	0.30	1.14	1.17
9	1	Control	2.80	0.29	1.11	1.11
10	1	Control	4.10	4.29	1.16	1.17
11	1	Control	4.39	1.16	1.16	1.16
12	1	Control	0.75	0.75	1.16	1.17
13	2	Humidity	0.47	1.84	See Note 1	
14	2	Humidity	2.75	2.18	"	"
15	2	Humidity	2.79	0.52	"	"
16	2	Control	1.15	1.06	"	"
17	2	Control	1.31	1.25	"	"
18	2	Control	1.30	1.60	"	"

Note 1: Samples 13 - 15 all lifted during humidity and peel strength tests not made.

Figure 6-26. Attenuation Effects of Magnetic Shielding

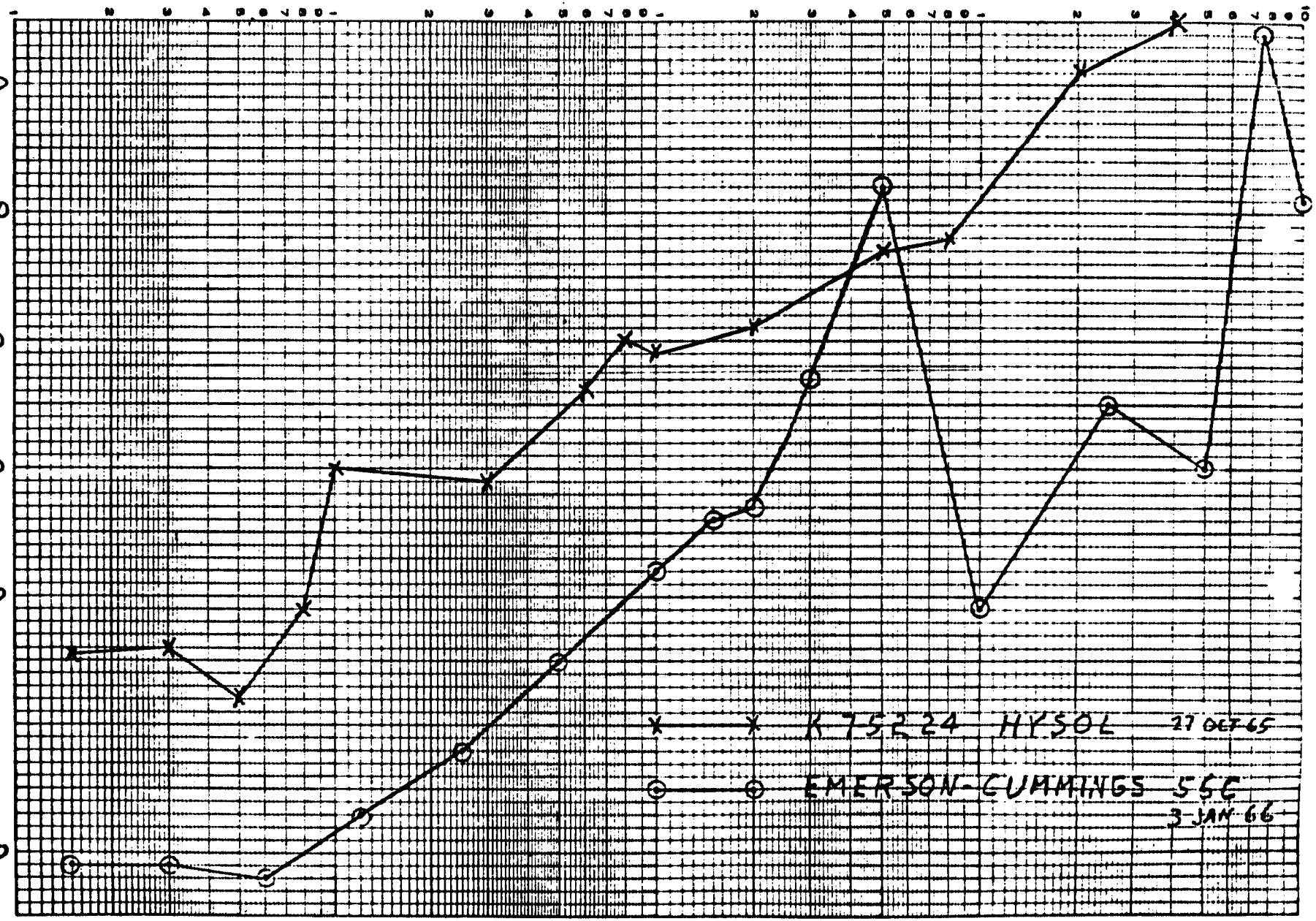
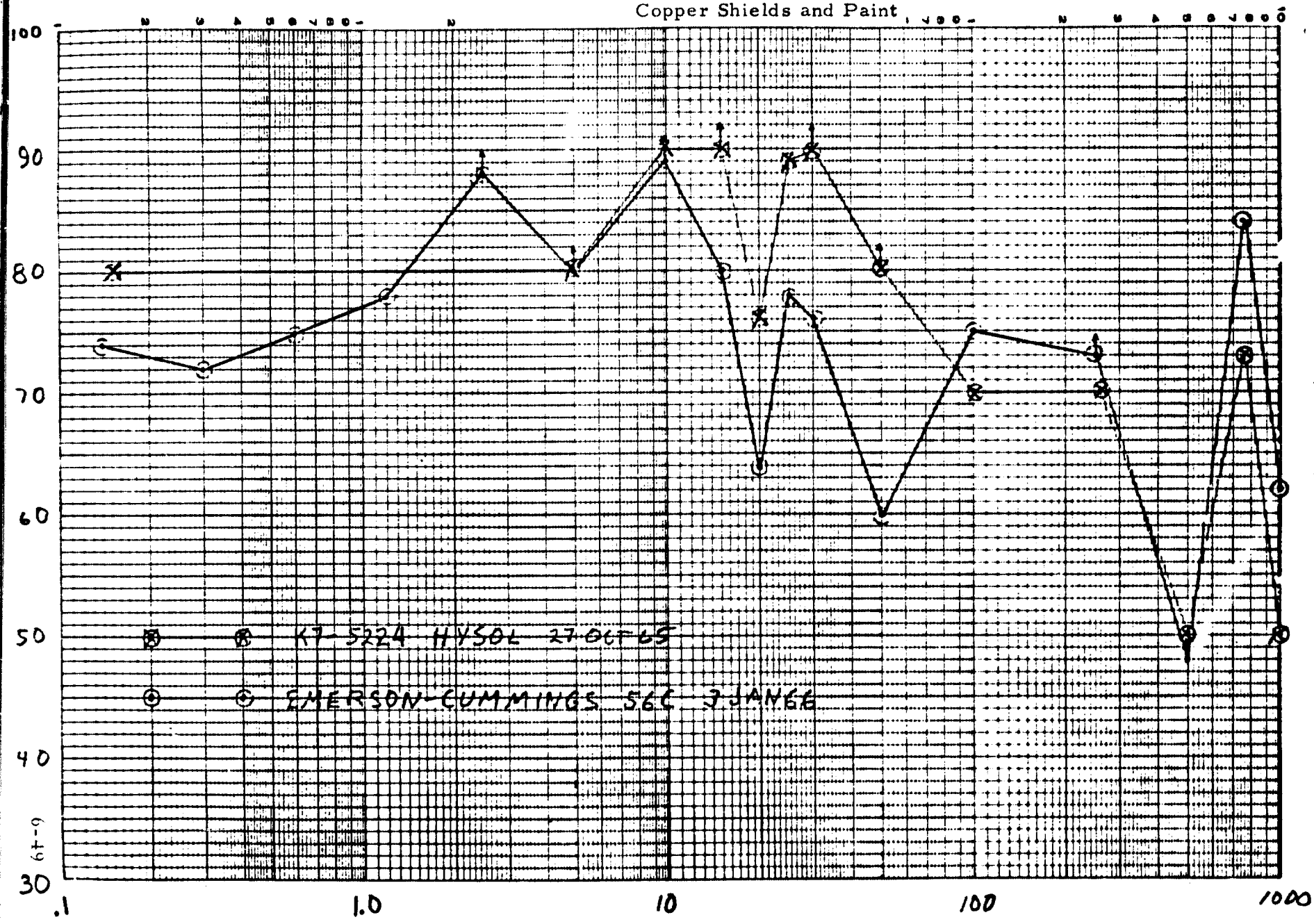


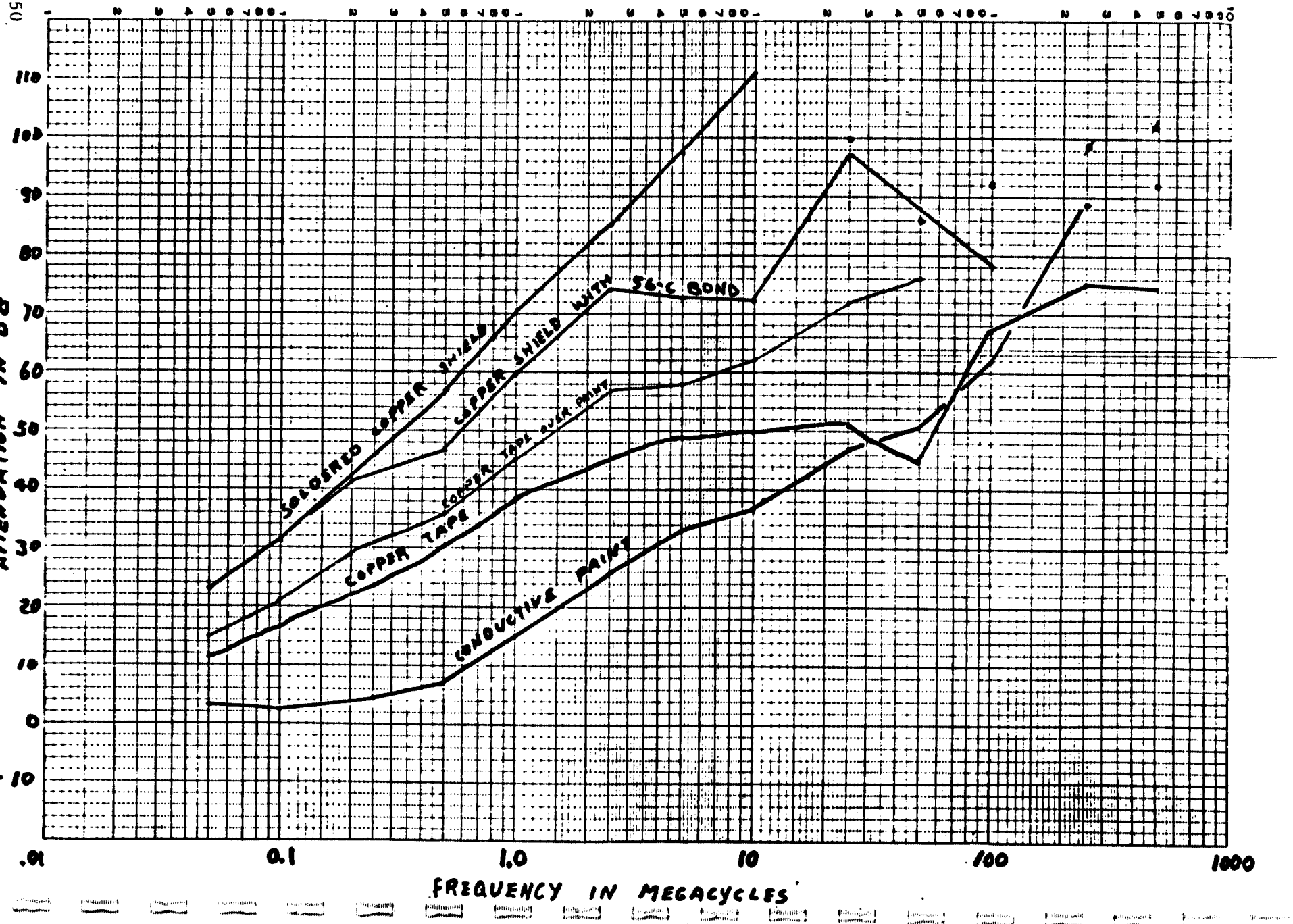
FIG. 26

Figure 6-27. Electromagnetic Shielding



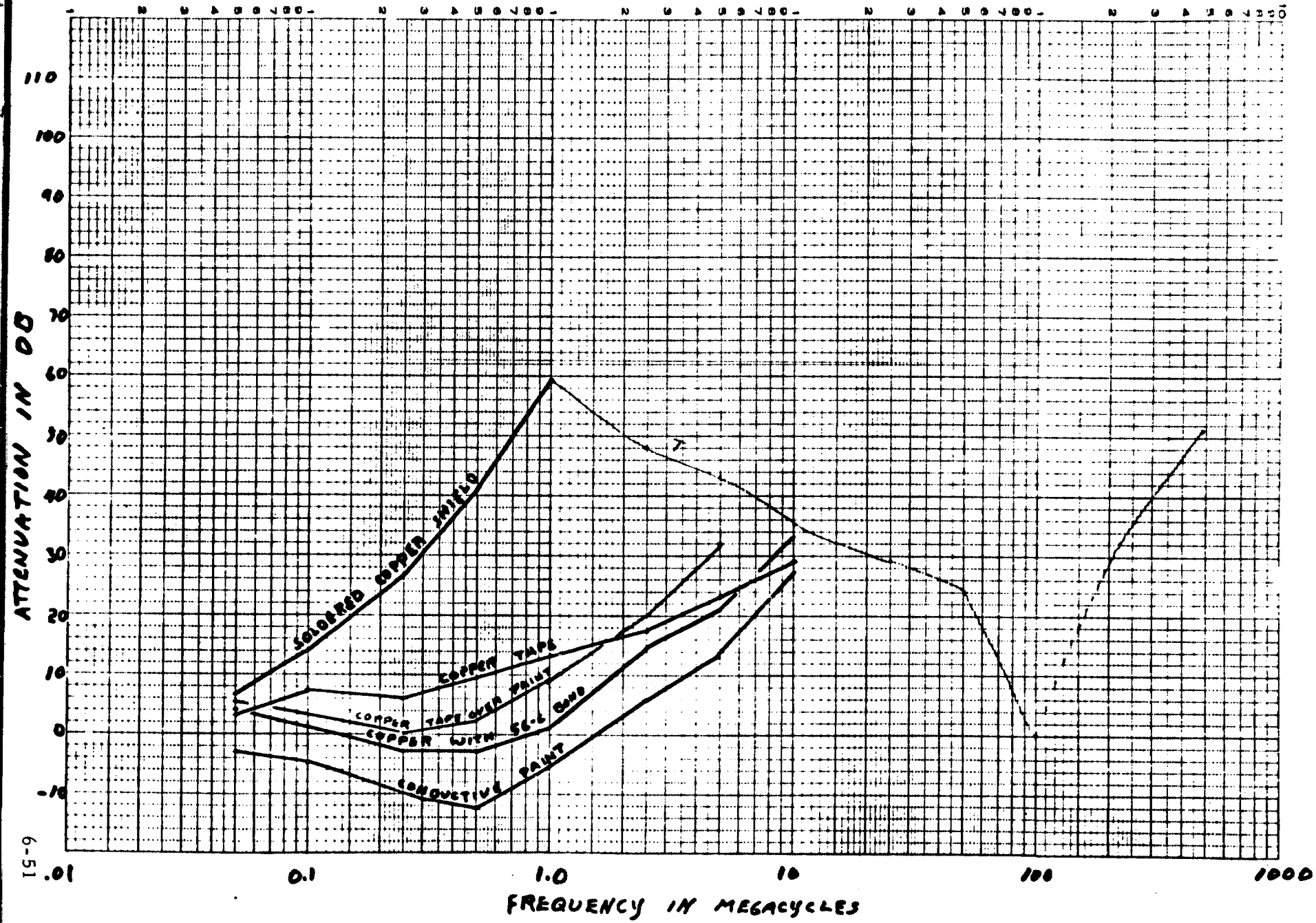
MID 1A
1B

Figure 6-28. Effect of Shielding Using Spiral Radiators



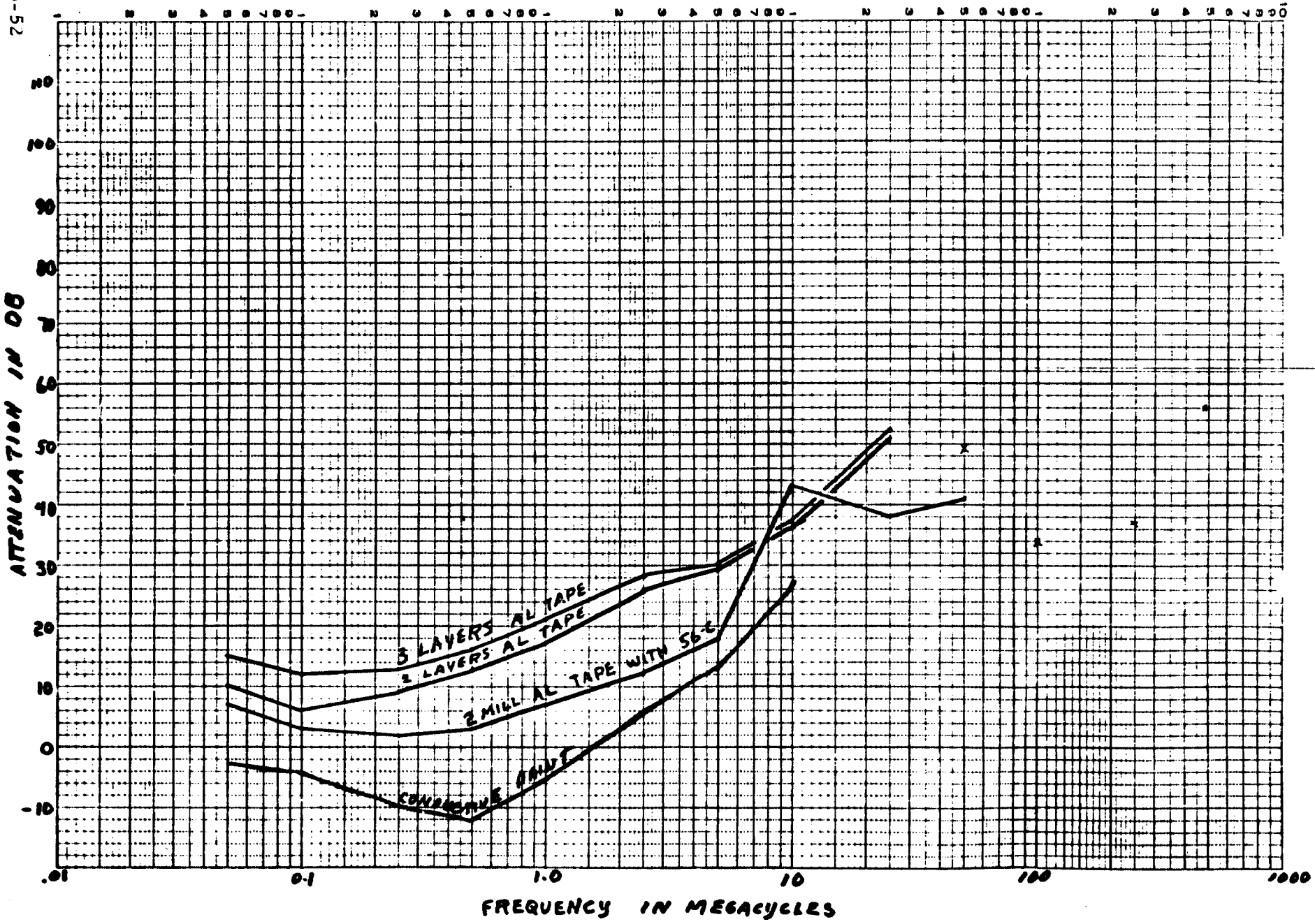
MOV 19
18

Figure 6-29. Effect of Shielding Using R-F Chokes



MOD 24
2B

Figure 6-30. Effect of Shielding Using R-F Chokes

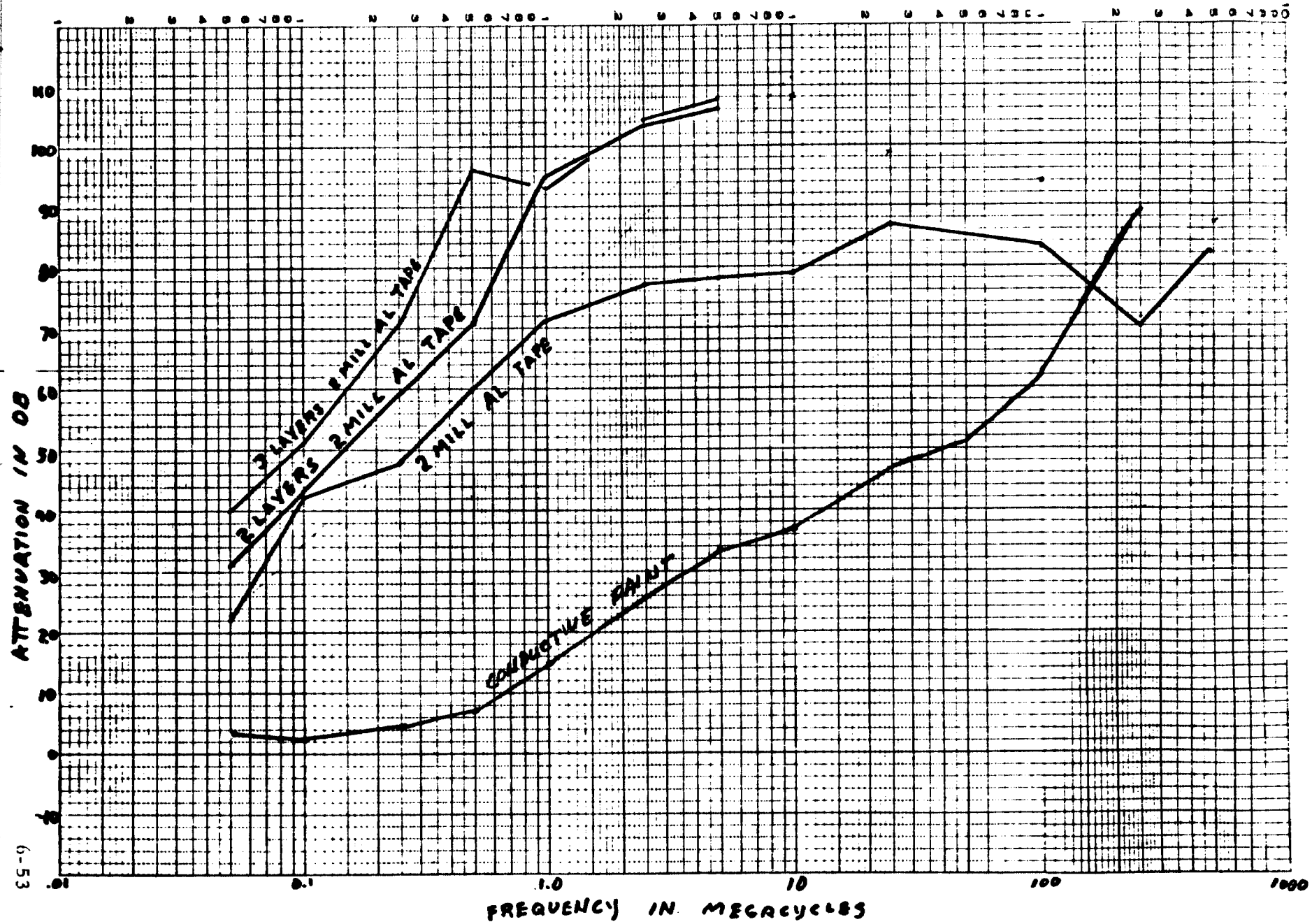


NO. 340 \ 510 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
5 CYCLES X 10 DIVISIONS PER INCH

EUGENE DIETZGEN CO.
MADE IN U.S.A.

MOD 2A
2B

Figure 6-31. Effect of Shielding Using Spiral Radiators



The recommended method for obtaining an EMI shield is to use an aluminum foil with no adhesive backing. The foil will be bonded to the chassis with EC-56C or an equivalent adhesive. The foil will also be bonded to the Sylgard and foam surfaces with a nonconductive adhesive to secure the foil during handling and vibration in order to establish a fixed ground plane.

6.6 HOUSING

There are many approaches that will yield a light weight housing capable of surviving the specified environments. The configuration of the housing is dependent upon many items, one of which is the form factor desired. Another item to be considered is whether the transponder is to be supplied as a transponder or as a separate transmitter and receiver. Since the current program was limited to construction of a breadboard transceiver, no effort was expended to select an optimum housing configuration and no testing was done; however, there are several generalizations that can be made that will be reflected in any firm design.

The transmitter will have to be housed in a sealed package. A sealed unit is required primarily to protect the stripline circuitry from moisture, which has severe effects on the stripline dielectric material being used. There are stripline materials not subject to this problem but they are extremely difficult to use and, in any event, the presence of moisture on the circuitry itself degrades performance. It may also be necessary to seal the unit to prevent corona in the output filter. It may become necessary to use an interdigital filter to achieve small volume and in that event either the filter or the housing must be sealed.

The receiver is capable of operating in no housing at all except for EMI. However, it is desirable to place the receiver in a sealed housing for protection against fuel spillage, radiation, micro meteroids, etc.

The housings can be vented to ambient through the use of a double acting pressure relief valve operating over a 2 or 3 psi pressure differential, however, the reduction in weight theoretically realizable through reduction in stress levels by venting

is offset by the weight and volume requirements for the valve and also by practical limitations on the thinness of the wall sections.

The housing recommended for any firm design is one that will generally conform to that shown in Figure 6-32. The figure is that of a 3 watt transmitter developed for LMSC on the SGLS program. Figure 6-33 shows how this basic design was adapted to provide a sealed housing for the LEM S-Band Transceiver.

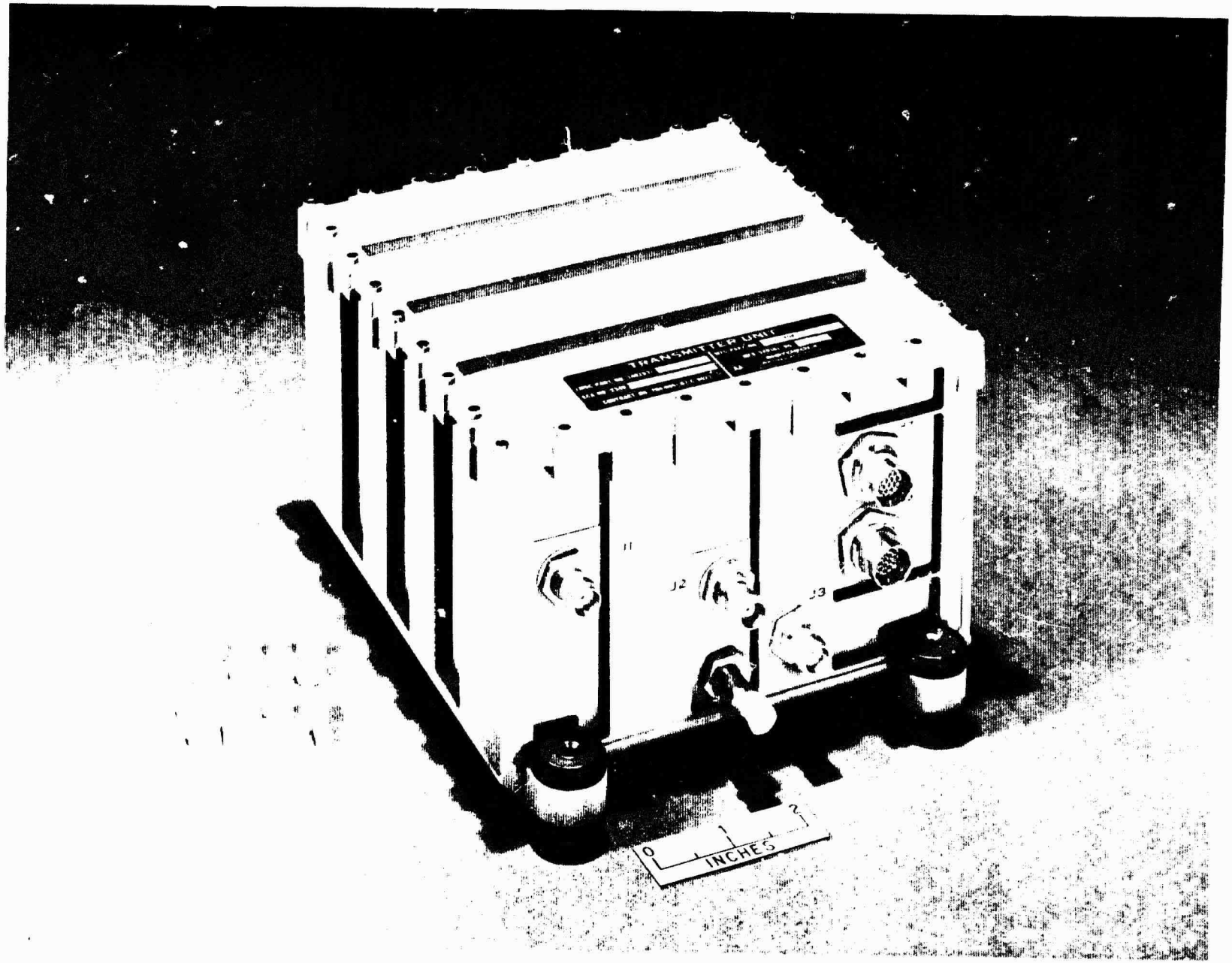


Figure 6-32. SGLS Transmitter

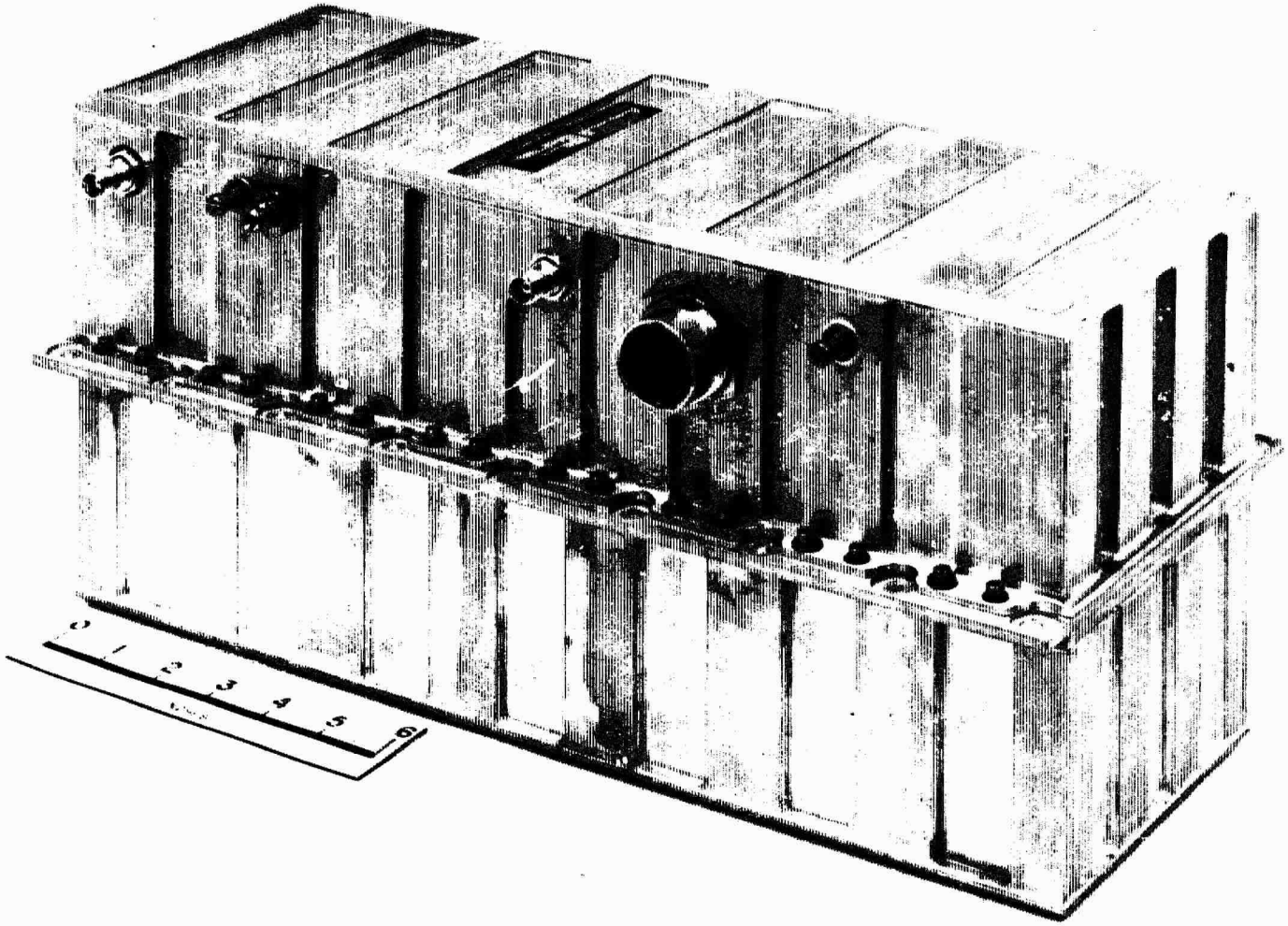


Figure 6-33. LEM S-Band Transceiver

SECTION VII
BREADBOARD TEST RESULTS

7. INTRODUCTION

The Advanced S-Band Transponder was tested at room temperature in accordance with the "Test Plan For Breadboard S-Band Transponder". A copy of the test plan is included at the end of this report as Appendix A.

At the time this test was performed the transmitter was not available in complete form. It is believed that the results of the test of the transmitter are reasonably representative of the final configuration except for power output. A block diagram of the transmitter configuration used in the test is shown in figure 7-1. Test data for the complete transmitter can be found in Section 3 of this report.

Some of the tests performed deviated slightly from the test plan. These deviations plus a discussion of the results are presented ahead of each group of test data. The individual test is identified by the same paragraph number as in the test plan.

The results of the test are generally satisfactory. Sufficient data is included in the results to allow adequate characterization of the transponder for ordinary purposes.

Additional special tests not specified in the Test Plan were performed. These tests are presented in subsection 7.2.

7.1 TEST RESULTS

5.1 Receiver Dynamic Range and AGC Linearity

A plot of the receiver AGC characteristic is shown in figure 7-2. As can be seen in the plot, the AGC characteristic is relatively linear from -127 dbm to -60 dbm. From -60 dbm to -30 dbm the characteristic starts to flatten out because the diode attenuators in the AGC IF Amplifier are operating in a nonlinear region.

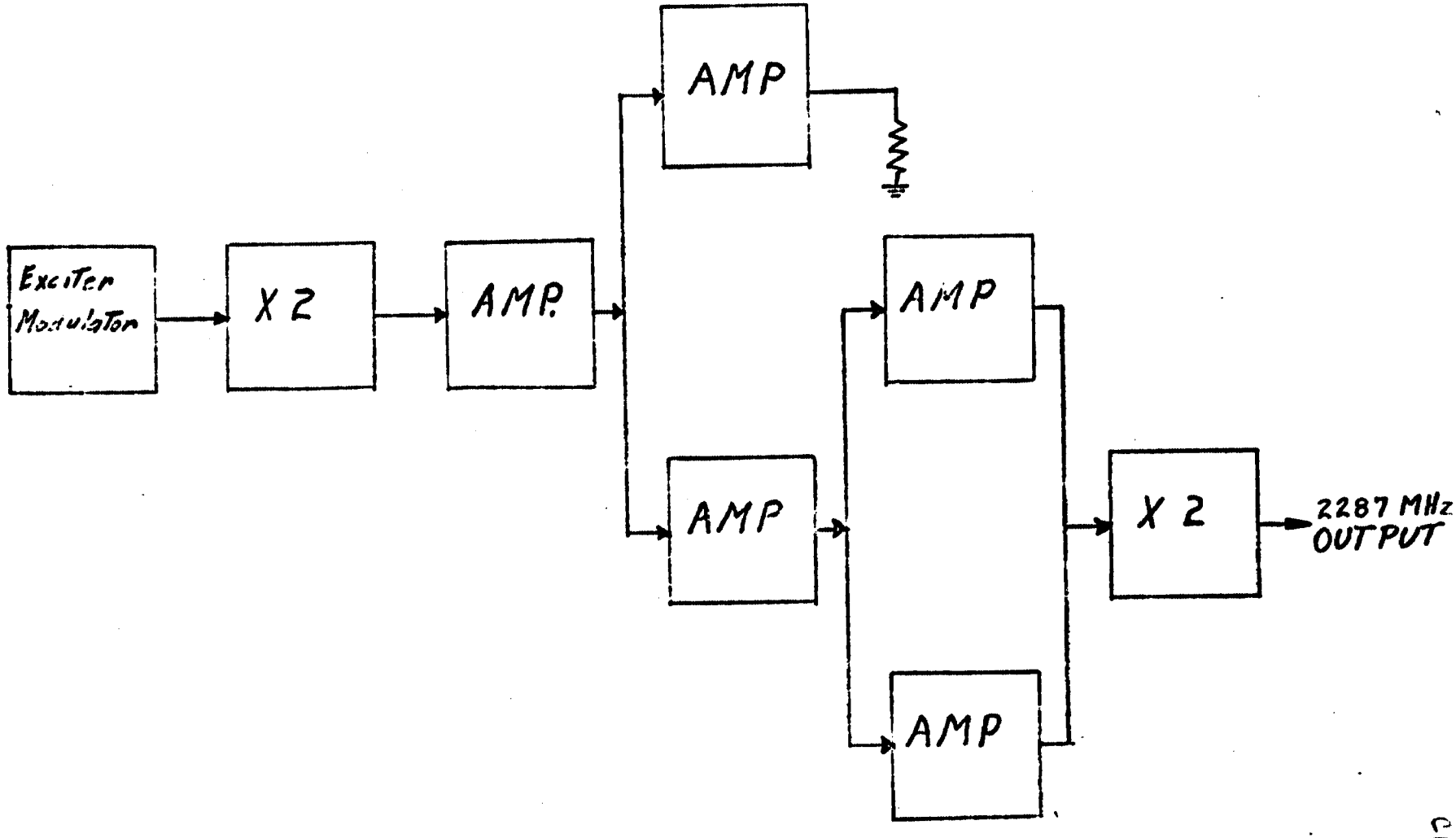


Figure 7-1. Abbreviated Transmitter Configuration

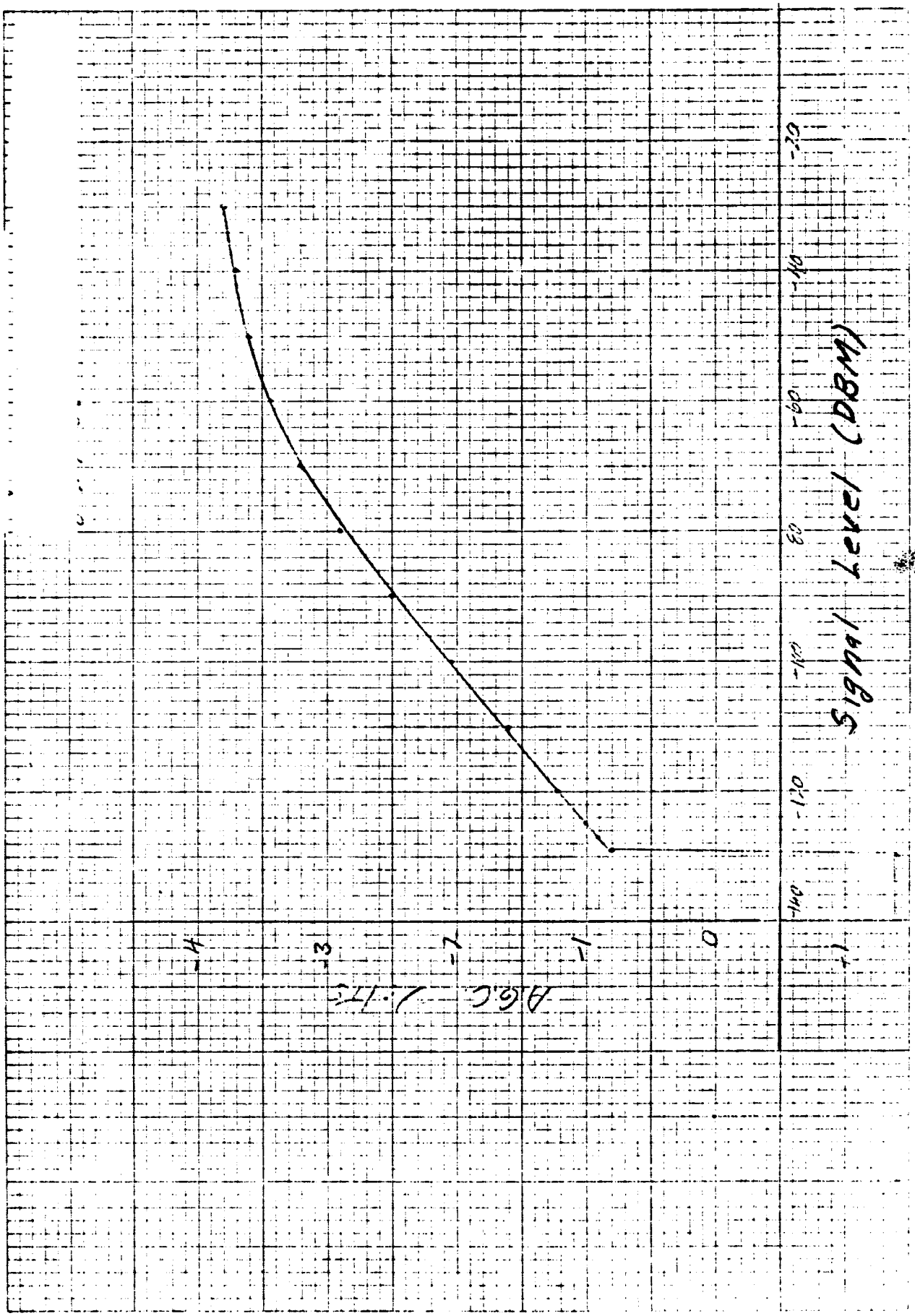


Figure 7-2. Receiver AGC Characteristic

5.2 Receiver Acquisition Threshold

The acquisition threshold for the receiver measured -127 dbm. The phase lock loop is optimized at +6 db S/N in the noise bandwidth $2B_{LO}$ = 1000 Hz. With a noise figure of 11 db the calculated optimization point is -127 dbm, therefore measured results are in agreement with calculations.

The sweep rate = 24.8 kHz/sec and the sweep range is +58.1 kHz and -60.8 kHz from receiver center frequency. The receiver center frequency is defined as the frequency at which the receiver static phase error (SPE) is zero. This frequency (referred to S-band) is 2106.380256 MHz. The transponder was designed for the Block II Apollo specified center frequency of 2106.406250 MHz.

This means the breadboard receiver center frequency is offset -25.994 kHz from the specified center frequency. At the time these tests were performed, it did not seem important to trim out this offset since the STE had adequate range to test the acquisition range of the receiver.

5.3 Receiver Acquisition Range

The receiver acquires a carrier that is actually beyond the sweep range limits by the amount shown below.

High Side	10.5 kHz
Low Side	8.0 kHz

5.4 Receiver and Synthesizer Lock Range

The receiver and the synthesizer both remain locked out to the full carrier frequency limits of the STE. This test shows that the receiver and synthesizer will track an r-f carrier out to at least +180 kHz and -202 kHz from the receiver center frequency.

5.5 Wideband Channel Frequency Response

The frequency response through the wideband channel of the transponder was measured three ways. The three measurements are: (1) receiver wideband

channel only, (2) transmitter wideband channel only, and (3) receiver and transmitter response through the complete ranging loop. These three response curves are shown in figure 7-3.

The curve that shows the combined response, labeled TRANSPONDER may appear to be inconsistent with the other two curves in the range of 100 Hz to 3 kHz. However, the rise at 100 Hz and the dip at 1 kHz in the response is due to the transmitter being modulated through the ranging channel as well as through the coherent transmitter drive. The phasing of these two modulation sources cause the rise and the dip in the response.

5.6 Wideband Channel Output Linearity

The measurement of the "transmitter only" output linearity deviated from the test plan. The measurement was made with steps in modulation voltage instead of specified modulation indices since the modulation sensitivity of the transmitter was not known at each of these indices. The output linearity was measured through the 10 kHz and 500 kHz bandpass filters on the Test Receiver.

Plots of the Test Data for the receiver and transmitter wideband channel linearity at 500 kHz are shown in figures 7-4 and 7-5. Each plot shows a ± 10 percent envelope as was specified in the Block II Apollo USBE specification. In each case the measured data was within the ± 10 percent envelope.

Additional data was taken to determine the transmitter modulation sensitivity at indices that can be identified by observing the spectrum. This data is shown below.

Index (radians)	Spectrum	Modulation Sensitivity (radians/volt)
1.42	$J_o = J_1$	0.72
1.84	$J_o = J_2$	0.72
2.4	J_o = null	0.74

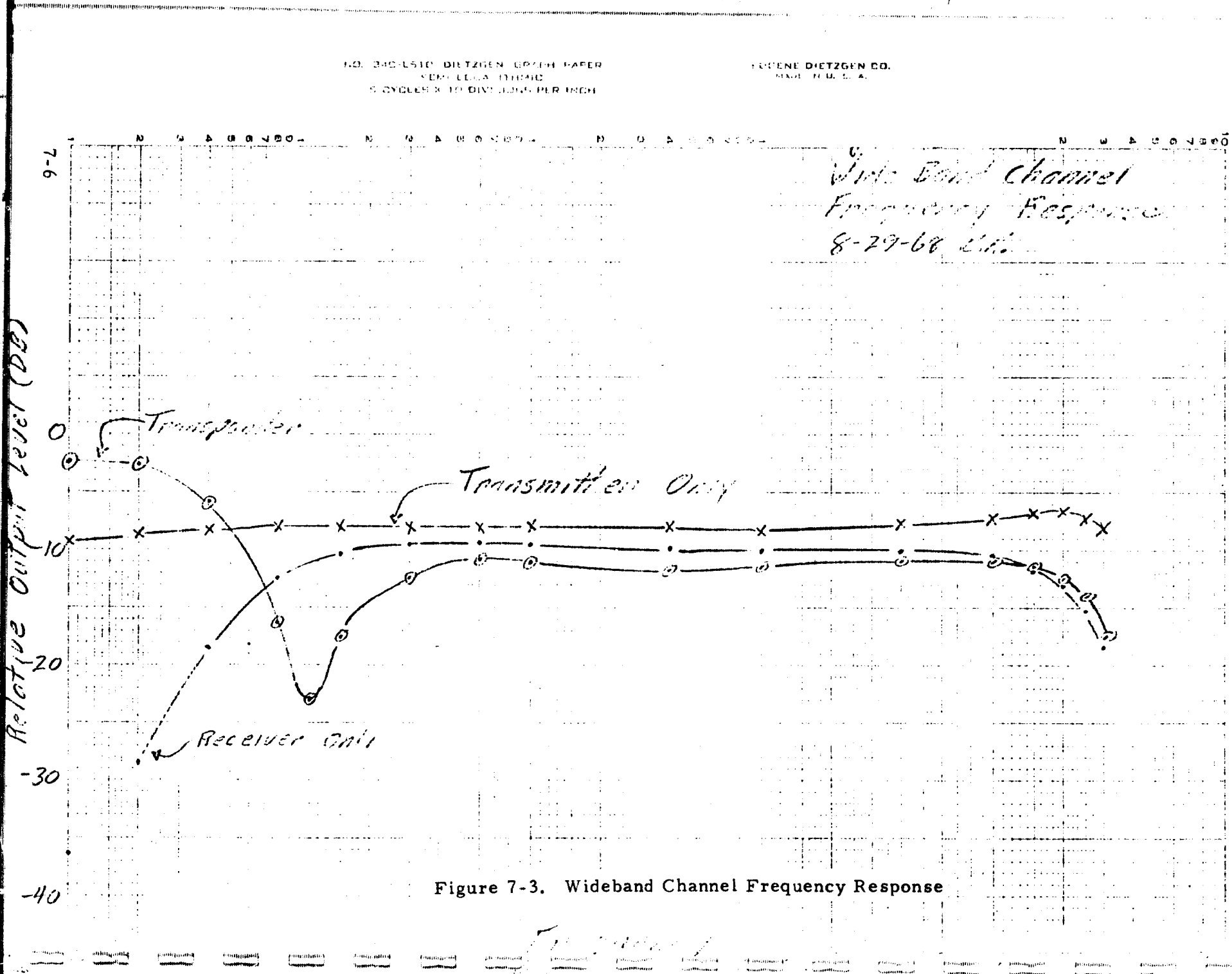


Figure 7-3. Wideband Channel Frequency Response

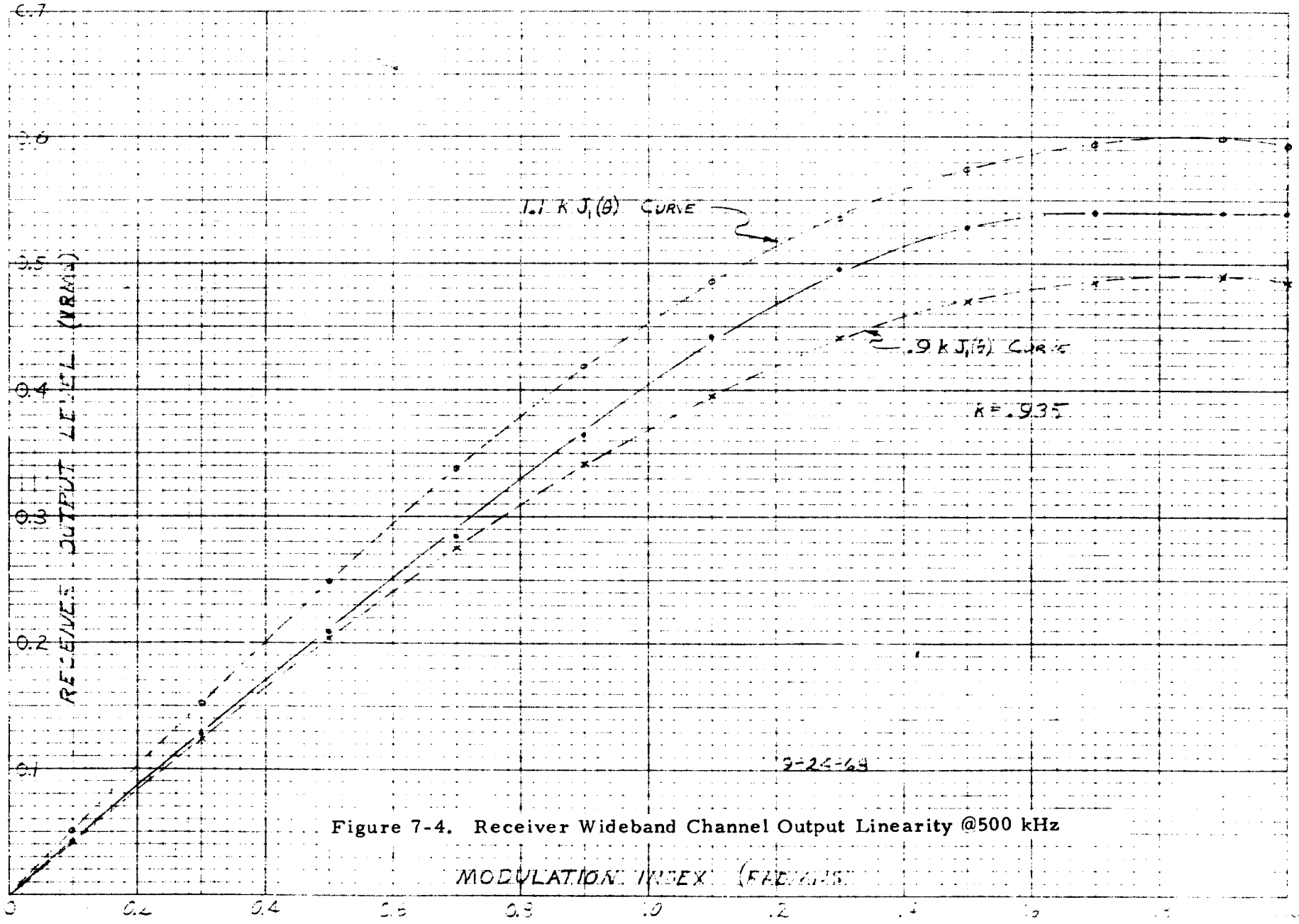


Figure 7-4. Receiver Wideband Channel Output Linearity @500 kHz

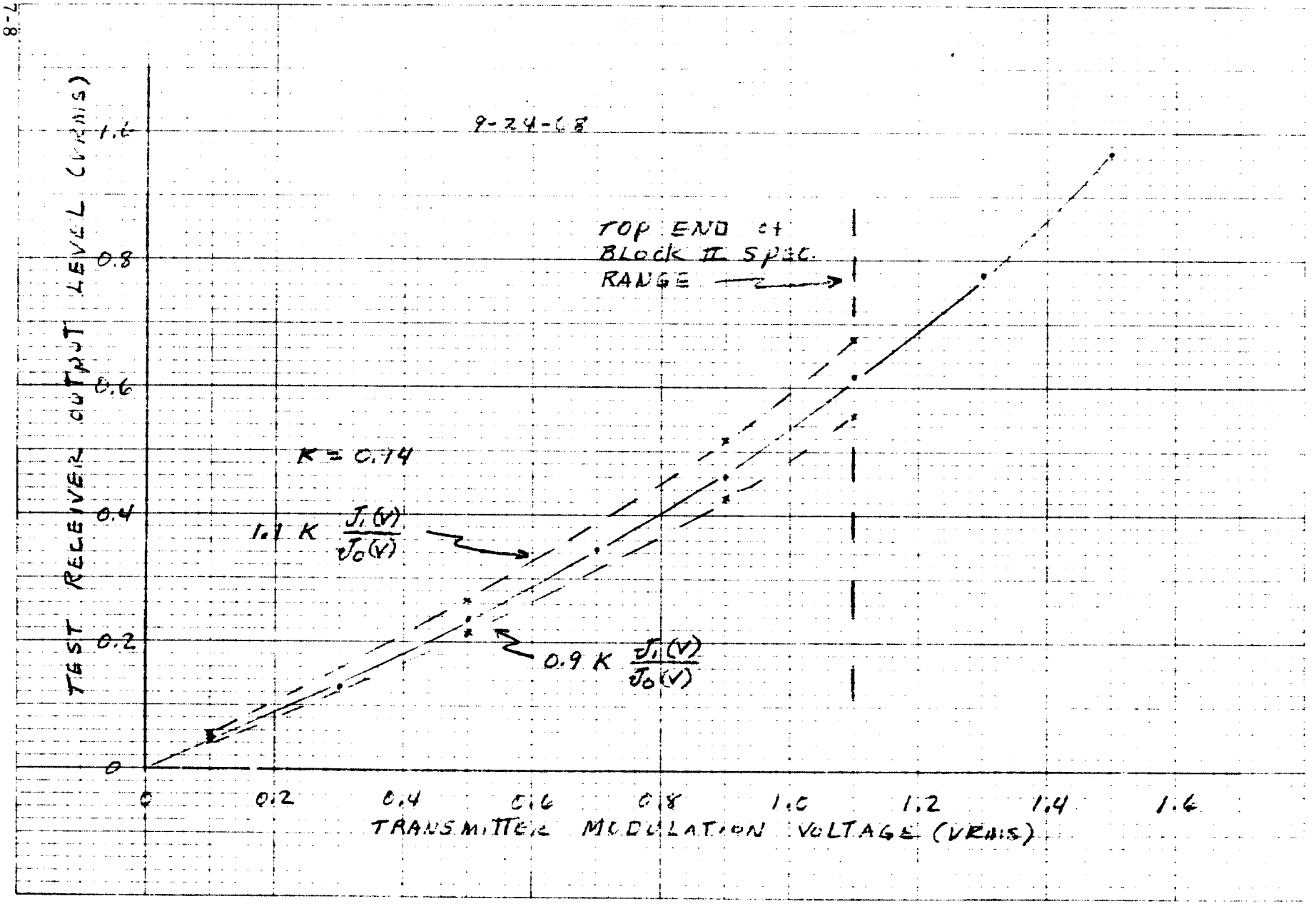


Figure 7-5 Transmitter Wideband Channel Output Linearity @500 kHz

5.7 Receiver Wideband Channel S/N Ratio Versus Signal Strength and Receiver Noise Figure

This test was performed by measuring the S/N ratio versus signal strength in an 18.4 kHz equivalent noise bandwidth using a 30 kHz subcarrier. When the noise through the filter was being measured the subcarrier was moved out to 100 kHz to assure that it did not add to the noise measured through the passband of the 30 kHz filter. A plot of the test data is shown in figure 7-6.

This data could be related back to front end noise figure, however there are uncertainties that make this determination questionable. A direct measurement of front end noise figure was made and the results of this test are given in the last section of this test report.

5.8 Residual Phase Noise

To provide more data for future reference and comparisons, the phase noise was measured in both the 21 Hz and 400 Hz bandwidth of the Test Receiver. A photograph of the oscilloscope trace of the noise is shown in figure 7-7. A spectral analysis of the phase noise was made with a HP 302A Wave Analyzer from 10 Hz to 30 kHz in each case. Plots of this data are shown in figures 7-8 through 7-13.

It is obvious from a study of the oscillographs and the spectral photo that the transponder does make a significant contribution to the total phase noise. The harmonics of the 60 Hz power frequency are clearly predominant. As discussed elsewhere, the sensitivity of the circuitry to the strong 60 Hz fields and extraneous voltages is a serious problem, requiring further investigation. Also, there is a significant noise level in the band from 100 Hz to 20 kHz which appears to be due to the transponder. This is thought to be generated in the digital synthesizer, although this has not been proven conclusively. This should be studied further with at least the following questions considered:

1. What is the cause of the noise and what is the maximum practical limit to which it can be improved by further design?

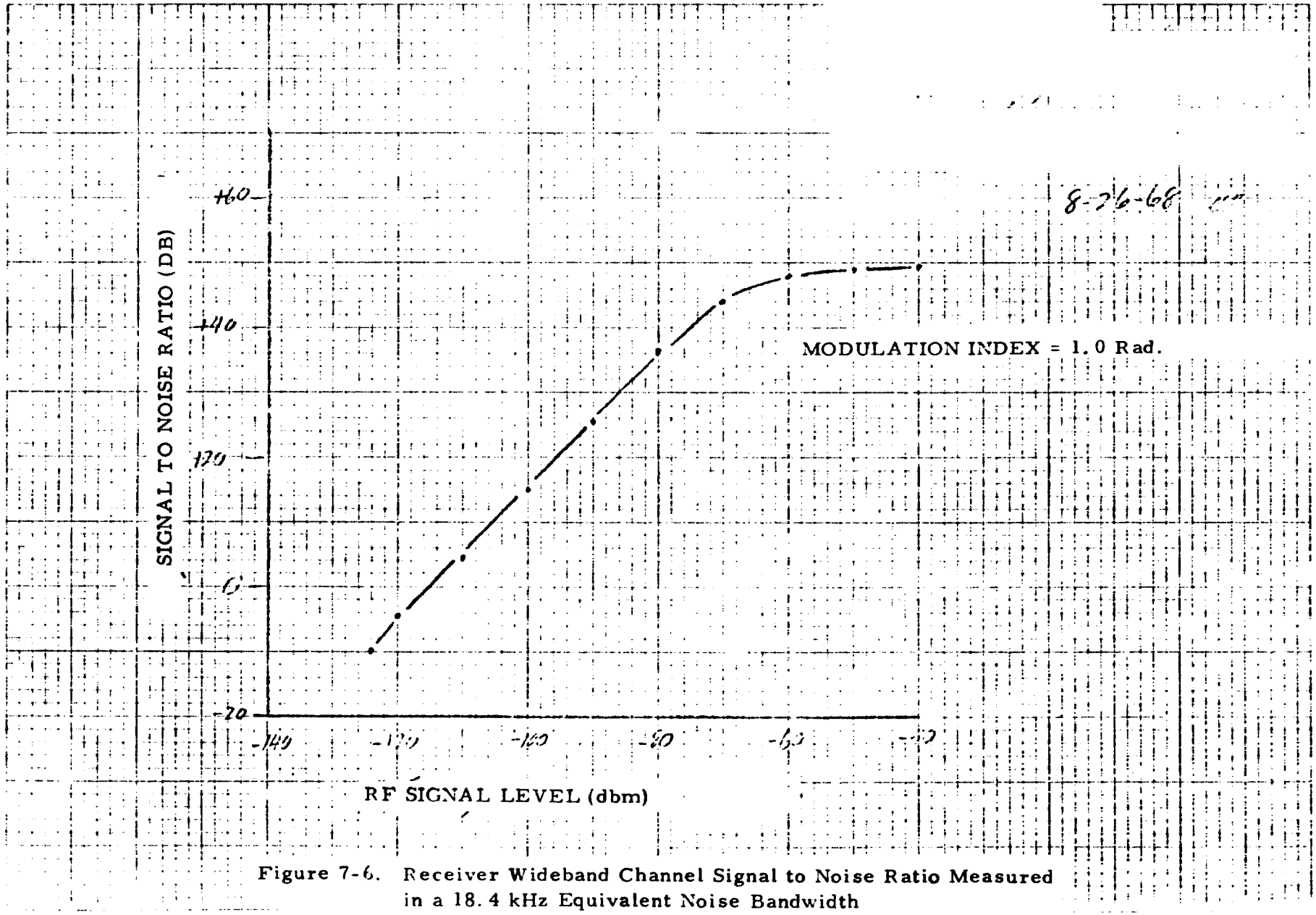
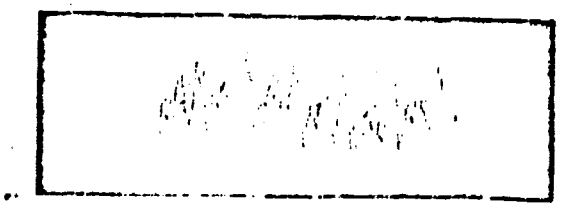


Figure 7-6. Receiver Wideband Channel Signal to Noise Ratio Measured in a 18.4 kHz Equivalent Noise Bandwidth



4°/CM

10 MS/CM

a) STE Receiver Bandwidth, $2B_L$ = 21 Hz

4°/CM

10 MS/CM

b) STE Receiver Bandwidth, $2B_L$ = 400 Hz

Figure 7-7. Residual Phase Noise, Oscillograph

Figure 7-8.

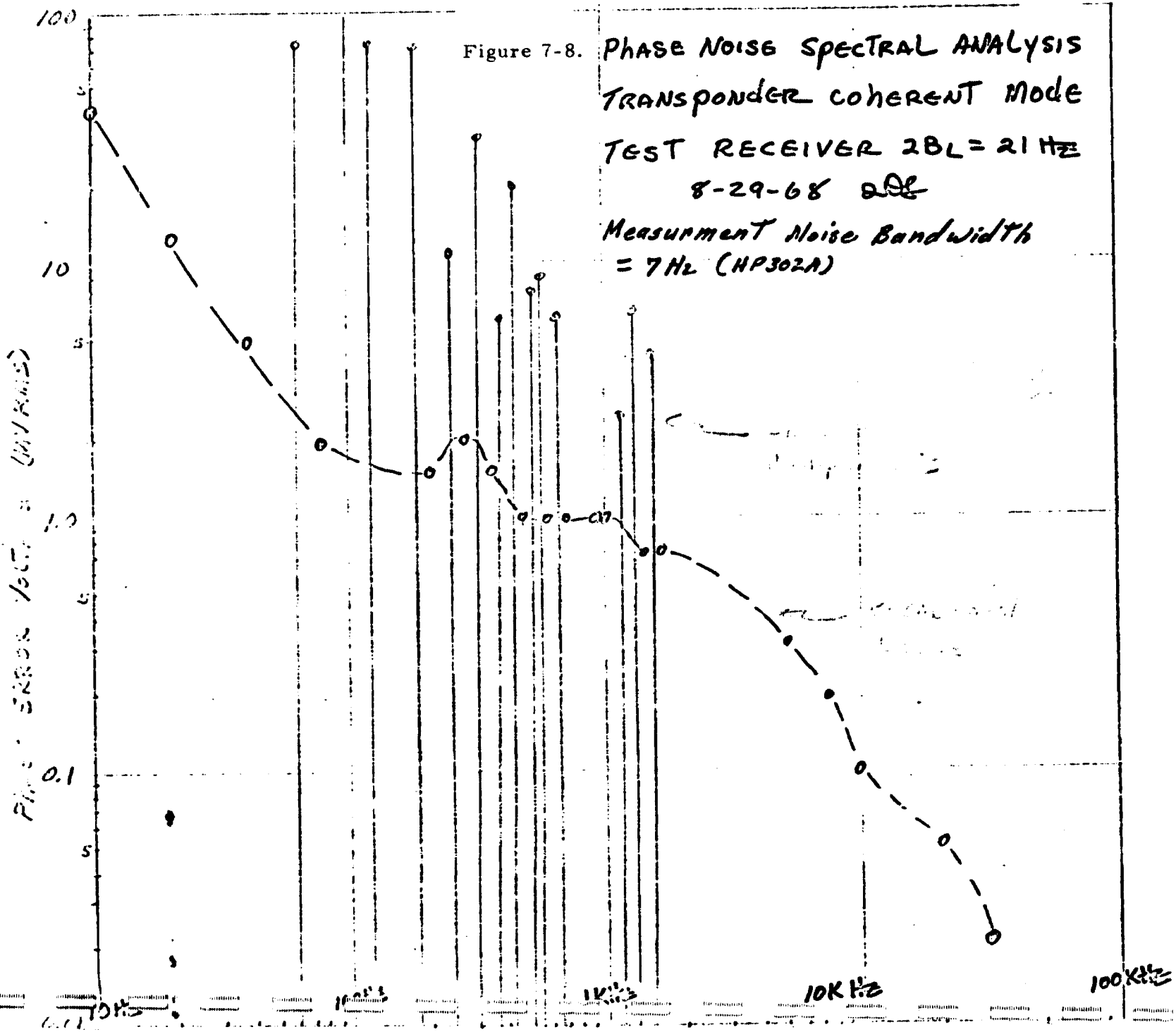

PHASE NOISE SPECTRAL ANALYSIS
TRANSPONDER COHERENT MODE
TEST RECEIVER 2BL = 21 Hz
8-29-68
Measurment Noise Bandwidth
= 7 Hz (HP302A)
100
10
1.0
0.1
10K Hz
100K Hz

Figure 7-9. Phase Noise spectral Analysis
TRANSPONDER COHERENT MODE
TEST RECEIVER $2B_L = 400$ Hz
8-29-68 SDS
Measurment Noise Bandwidth
= 7 Hz (HP302A)

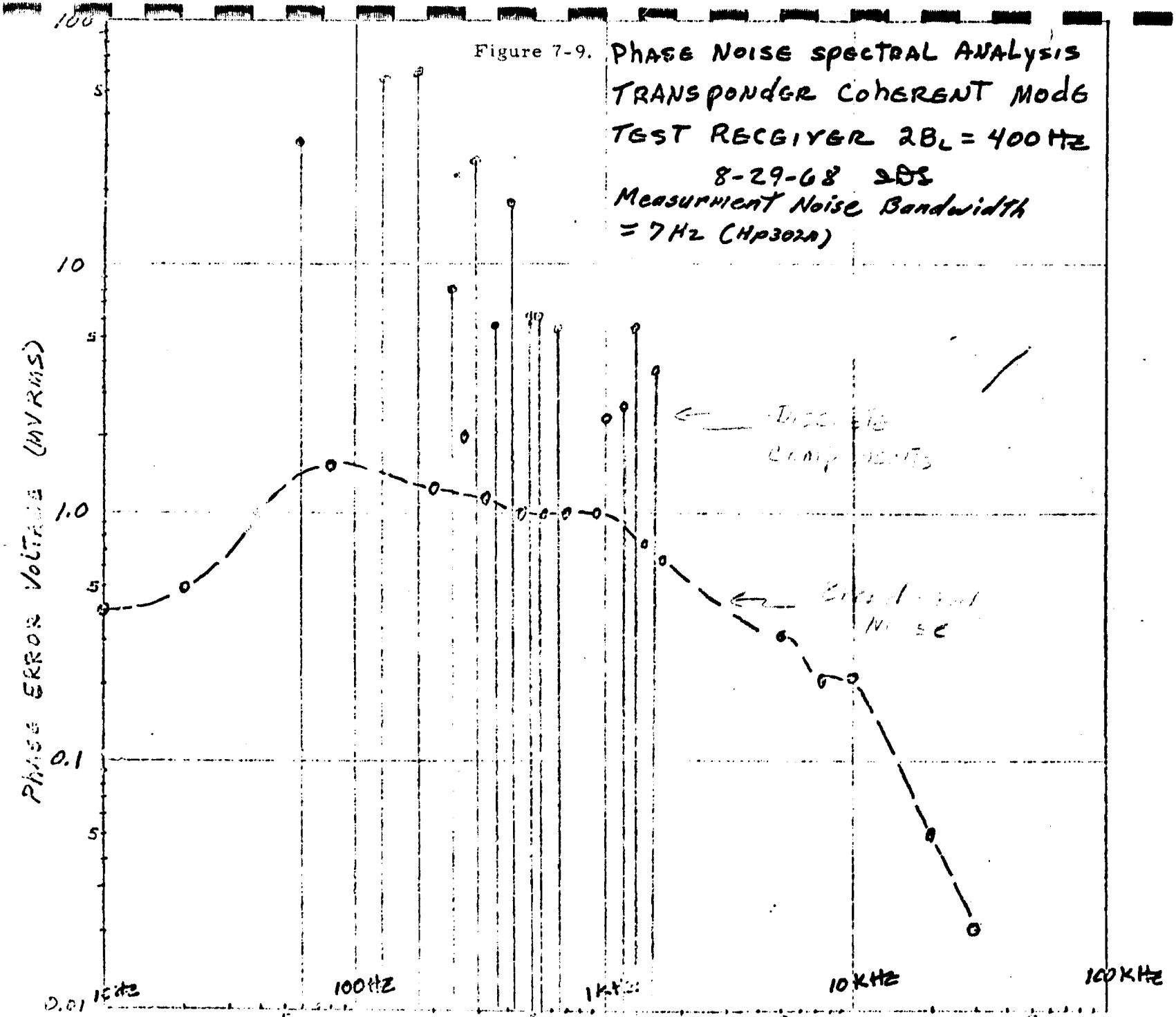


Figure 7-10. PHASE NOISE SPECTRAL ANALYSIS

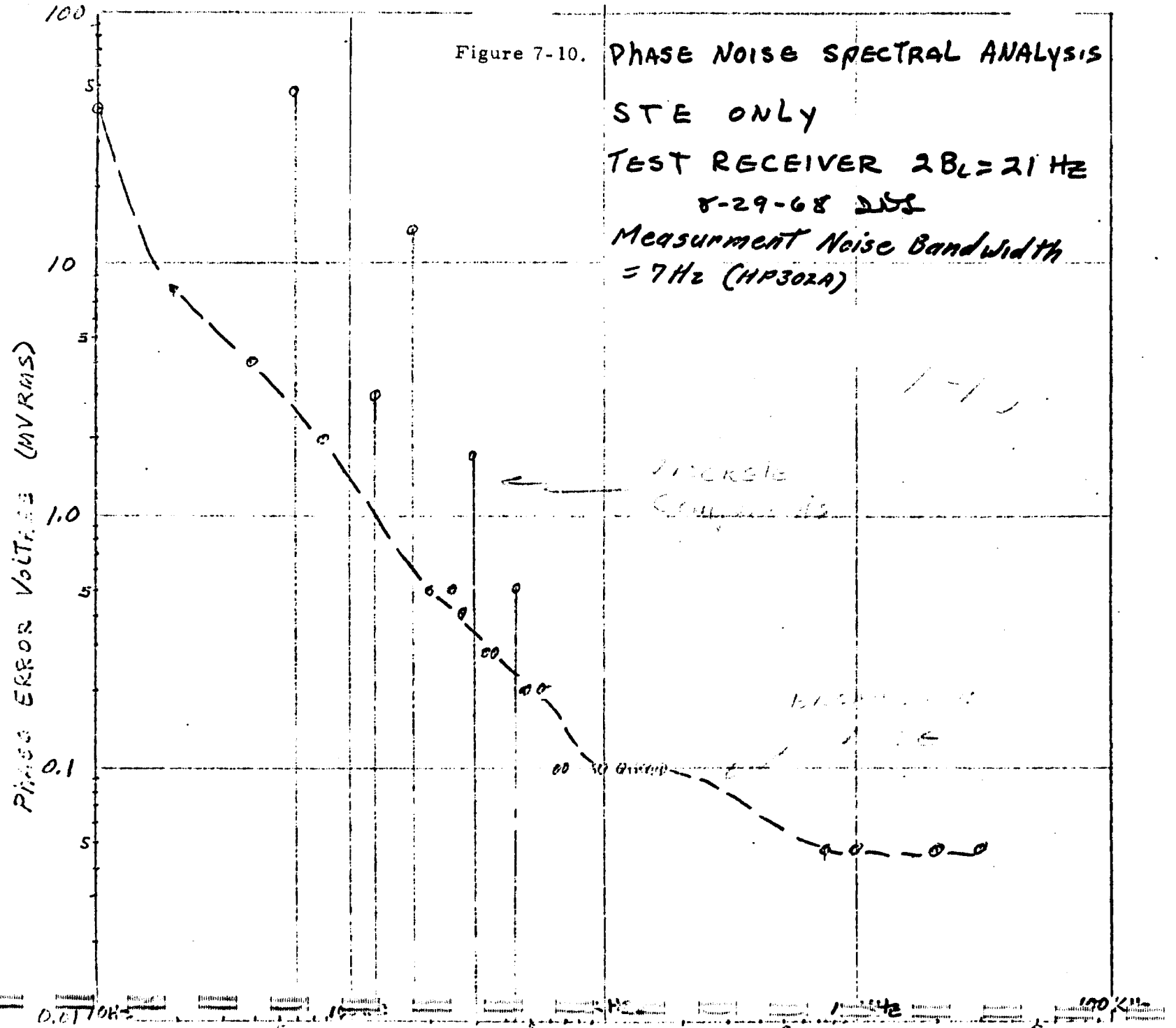


Figure 7-11. Phase Noise Spectral Analysis

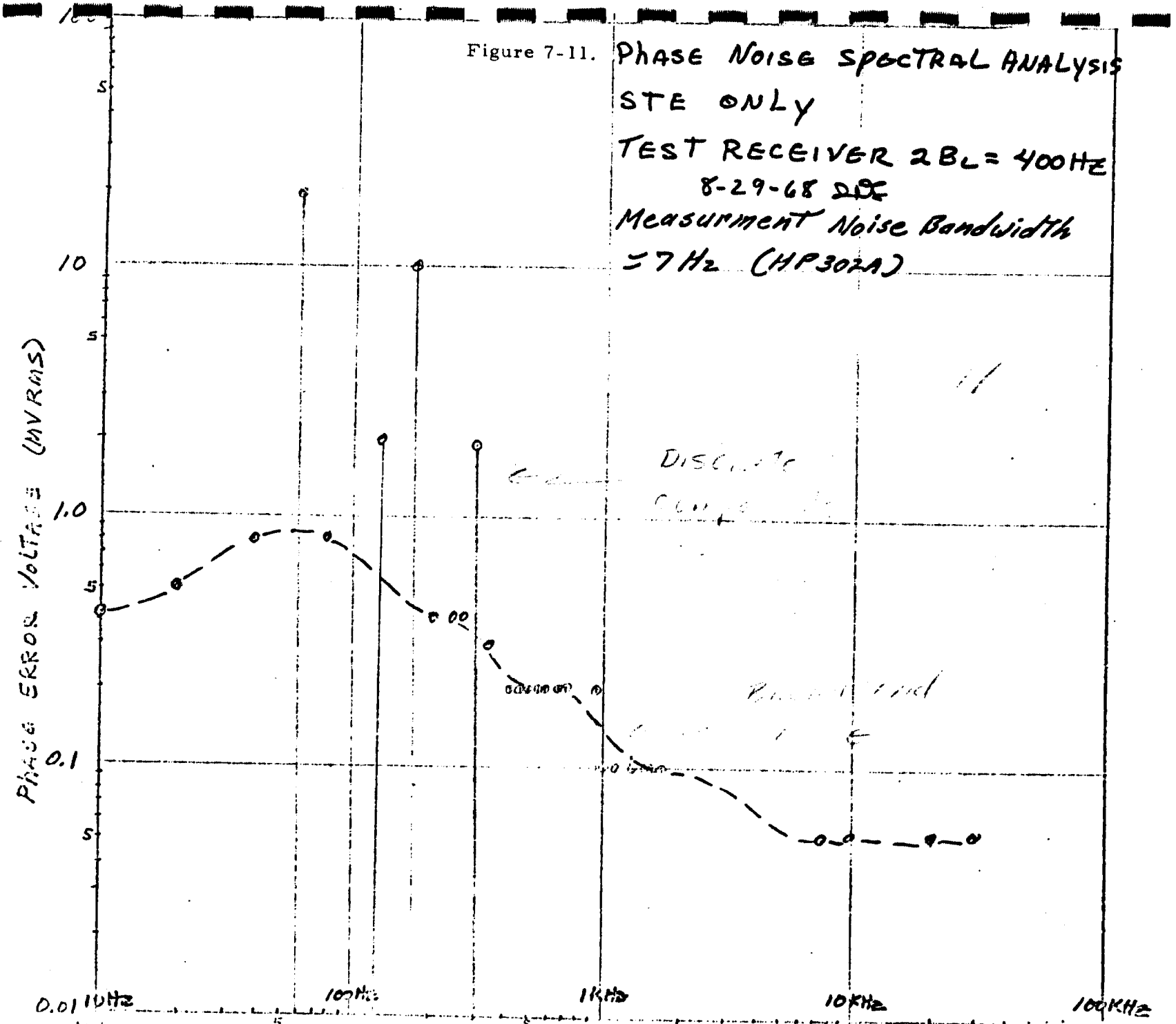


Figure 7-12.

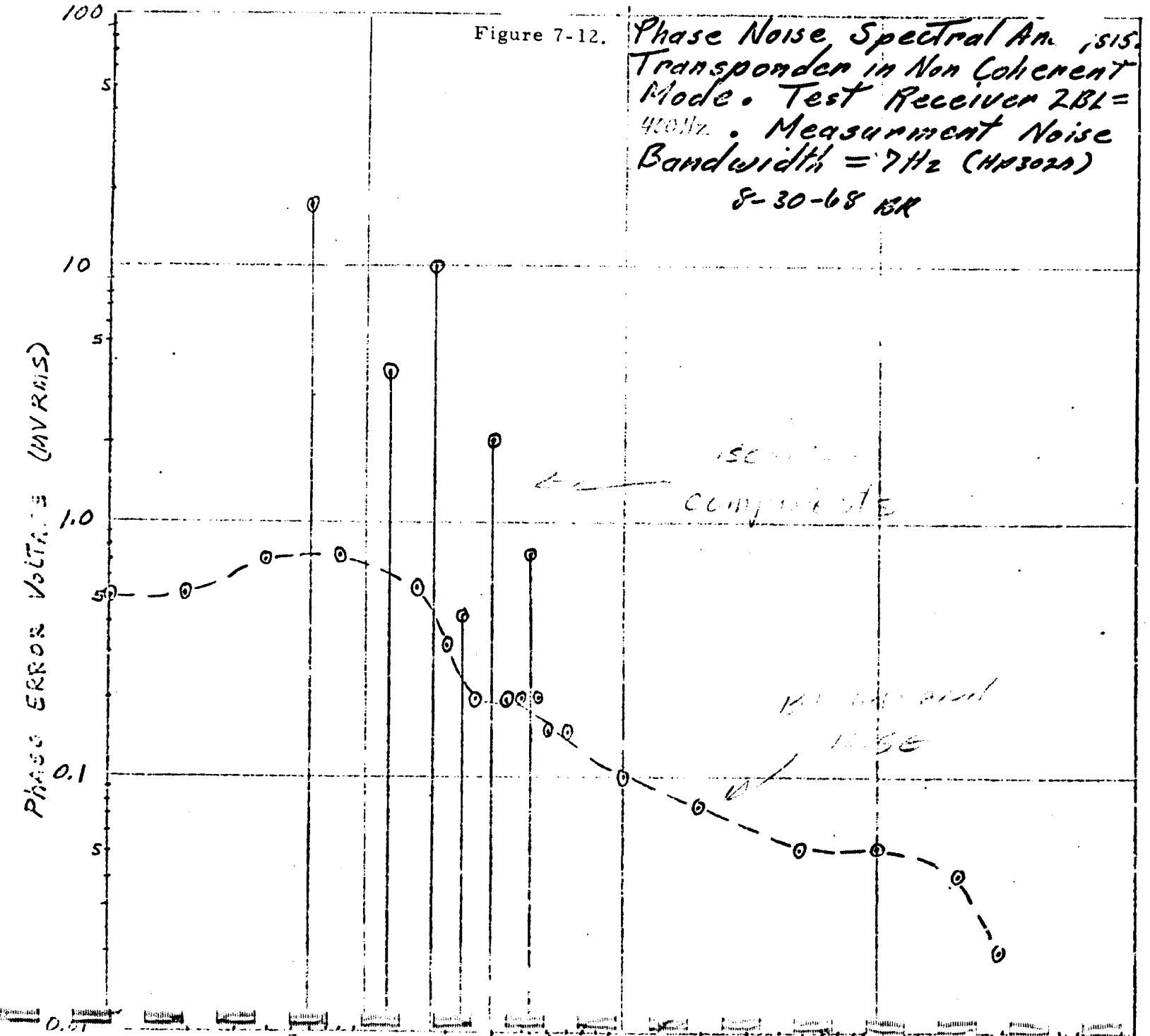
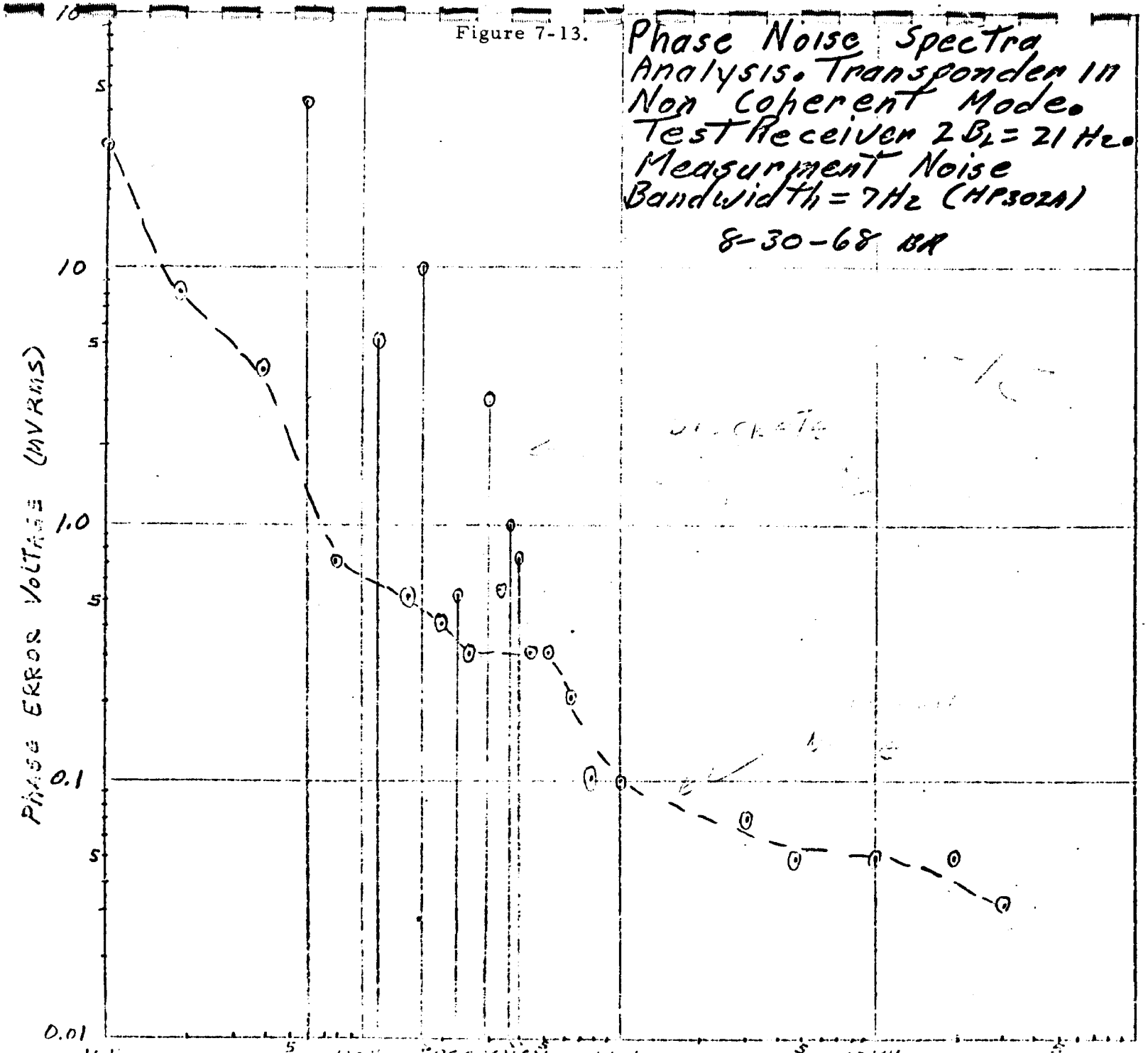

Phase Noise Spectral An. 1515. Transponder in Non Coherent Mode. Test Receiver 2BL = 400Hz. Measurment Noise Bandwidth = 7Hz (HP302A)
8-30-68 KR
PHASE ERROR VOLTAGE (MV RMS)
100
10
1.0
0.1
0.01
5

Figure 7-13.


Phase Noise Spectra
Analysis. Transponder in
Non Coherent Mode.
Test Receiver 2BL = 21 Hz.
Measurment Noise
Bandwidth = 7Hz (HP302A)
8-30-68 BR
PHASE ERROR VOLTAGE (MV RMS)
10
5
1.0
5
0.1
5
0.01

2. In what way does this characteristic degrade overall system performance?

Test Data

	Test Receiver Bandwidth	
Residual Phase Noise	400 Hz	21 Hz
STE Residual Phase Noise	0.6	1.6 degrees rms
Coherent Mode		
Peak Phase Noise	5.0	6 - 8 degrees peak
RMS Phase Noise	2.1	3.3 degrees rms
Non-Coherent Mode		
Peak Phase Noise	2.0	6 - 8 degrees peak
RMS Phase Noise	0.9	2.9 degrees rms
Test Receiver - DPE Sensitivity		49.5 mv/degrees

5.9 Receiver Acquisition Characteristic

The receiver acquisition characteristic (plotted in figure 7-14) shows that an abnormal condition exists within the receiver loop. This is illustrated by the asymmetry of the curve and the fact that there is considerable spread between the error voltage at -100 kHz and the error voltage at +100 kHz. After some investigation it was decided that the cause of this condition is the feedback pair amplifier following the crystal filter (in the PDIF) which is being driven into limiting during strong signal acquisition. The feedback pair amplifier is not a phase stable amplifier when driven into limiting, therefore, its phase characteristic will contribute to the phase shift around the receiver loop and affect the acquisition characteristic.

This theory was fortified by performing the acquisition characteristic test as in paragraph 5.9 of the test plan, except with external AGC applied sufficiently to reduce the signal level into the PDIF to -40 dbm. This curve is shown in figure 7-15. The proposed correction of this problem is to replace the feedback pair amplifier with a limiting type amplifier which has a stable phase characteristic.

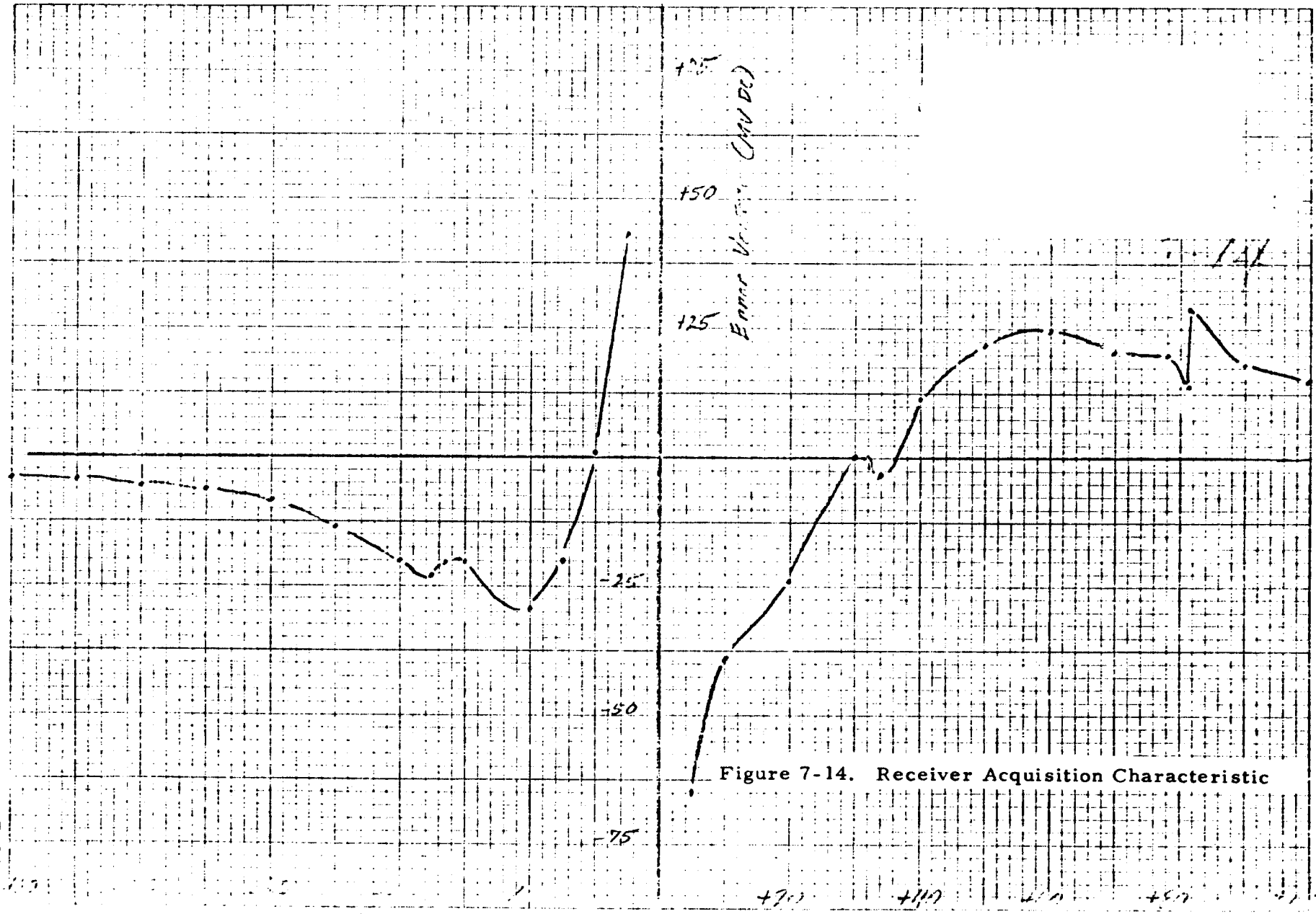


Figure 7-14. Receiver Acquisition Characteristic

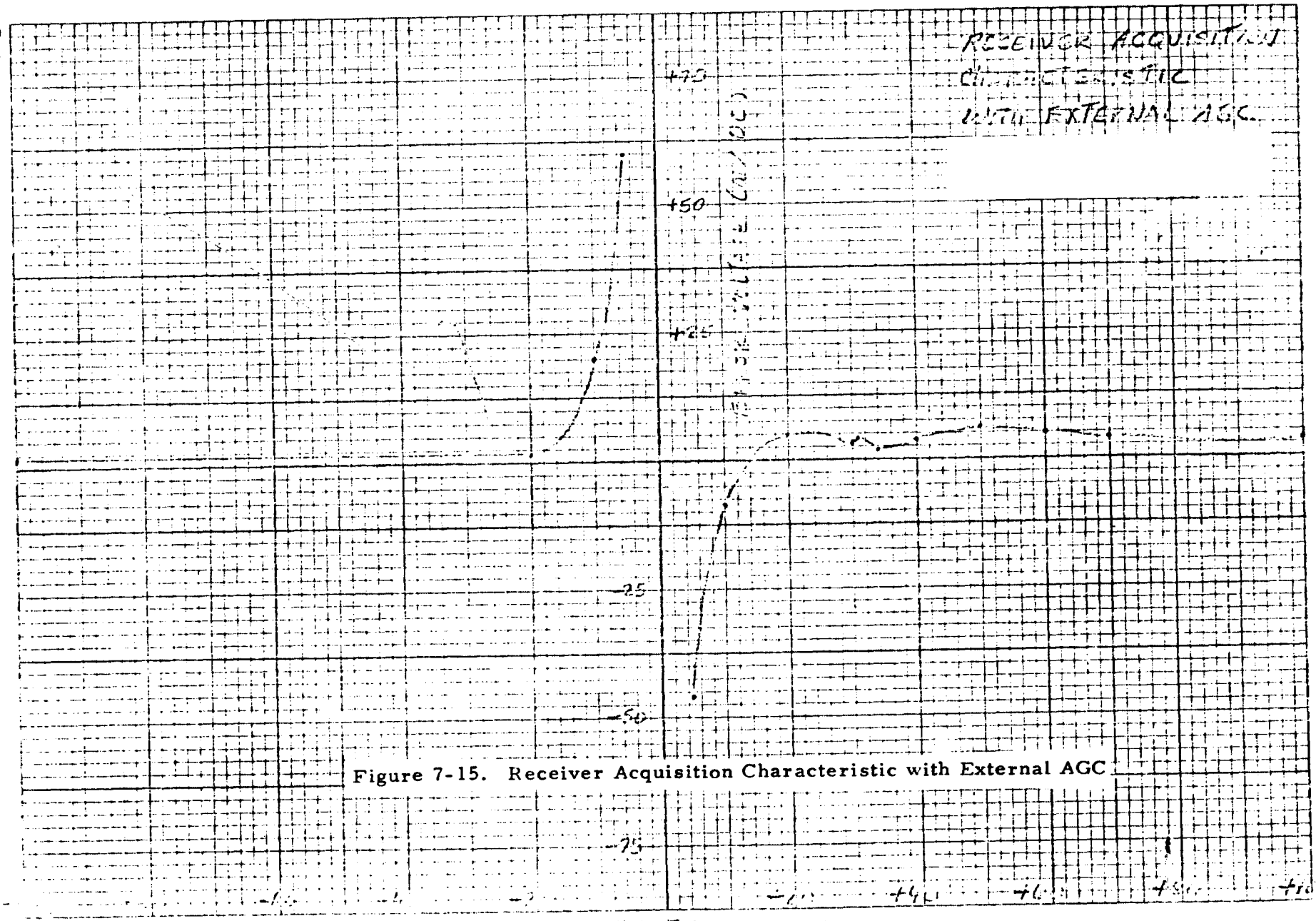


Figure 7-15. Receiver Acquisition Characteristic with External AGC

Although this condition is undesirable, the tests performed did not reveal any degradation of transponder performance as a result of it.

5.10 Transmitter Power Output and Frequency

Nominal supply voltage

	Coherent Mode	Non-Coherent Mode
Transmitter Output Power	2.5 watts	2.5 watts
Transmitter Output Freq.	2287, 500, 120 Hz	2287, 440, 200 Hz
Transmitter Output Spectrum	OK	OK

5.11 Line Voltage Sensitivity

-5% supply voltage

	Coherent Mode	Non-Coherent Mode
Transmitter Output Power	1.0 watts	1.05 watts
Transmitter Output Freq.	2287, 500, 310 Hz	2287, 440, 600 Hz
Transmitter Output Spectrum	OK	1.2 MHz sidebands due to output oscillator instability

+5% supply voltage

Transmitter Output Power	3.4 watts	3.4 watts
Transmitter Output Freq.	2287, 500, 230 Hz	2287, 441, 000 Hz
Transmitter Output Spectrum	OK	OK

5.12 Transmitter Power Output Versus Load Phase Angle (VSWR = 1.5)

Load Phase Angle Position	Power Delivered to the Load (watts)	Spectrum
(Each position is a Δ of approximately 45°)		
0	2.3 w	OK
1	2.0	OK

Load Phase Angle Position	Power Delivered to the Load (watts)	Spectrum
2	1.87	OK
3	1.73	OK
4	1.73	OK
5	1.92	OK
6	2.14	OK
7	2.35	OK
8	2.1	±60 MHz Sidebands

5.13 Input Power

	Power (watts)		
	Receiver	Synthesizer	Transmitter
Mode 1	0.9 w	-	-
Mode 2	1.2 w	-	-
Mode 3	1.2 w	3.79 w	50 w

5.14 Spurious and Harmonic Levels at Transmitter Output

Frequency	Relative Output Level (db)
3.43 GHz	25 db down
4.56 GHz	30 db down
6.9 GHz	33 db down

5.15 Self Lock (Ring-Around) Test

Description of Results:

There were no false lock indications.

5.16 Transponder Time Delay

Signal Level (dbm)	Ranging Time Delay (nsec)
- 60	401
- 80	405

Signal Level (dbm)	Ranging Time Delay (nsec)
-100	409
-115	411

7.2 SPECIAL TESTS

Additional tests that were not prescribed by the test plan were performed on the transponder. A description of these tests and the test results are presented in the following paragraphs.

7.2.1 Wideband Detector Dephasing

As the received signal strength is varied, the signal level at the limiters in the wideband channel is held constant by the AGC system. However, the noise level increases and eventually exceeds the signal level, as the received signal level is reduced below about -96 dbm. In the actual limiters, there may be some phase shift of the signal as this noise level increases. Such phase shift, if it occurs will cause dephasing at the detector and consequent distortion in signal strength.

A single test was made to determine the extent of such phase shift. The test signal was modulated at 0.5 radian with a 1000 Hz sinewave. The ranging output level was measured with a selective voltmeter, and the detector dc test point dc voltage was measured while varying the signal level from -40 to -124 dbm. The ranging output at 1000 Hz is plotted in figure 7-16. Figure 7-16 also shows the theoretical suppression (simplified expression) which would be expected to occur due to the limiters operating with a negative signal-to-noise ratio. As can be seen on figure 7-16, the measured data matches the theoretical curve very closely, indicating that any dephasing is insignificant. A varying dc output voltage is shown in the data tabulation below, its exact significance is not clear.

Measurements of the effect of signal level variations on the wideband detector phasing:

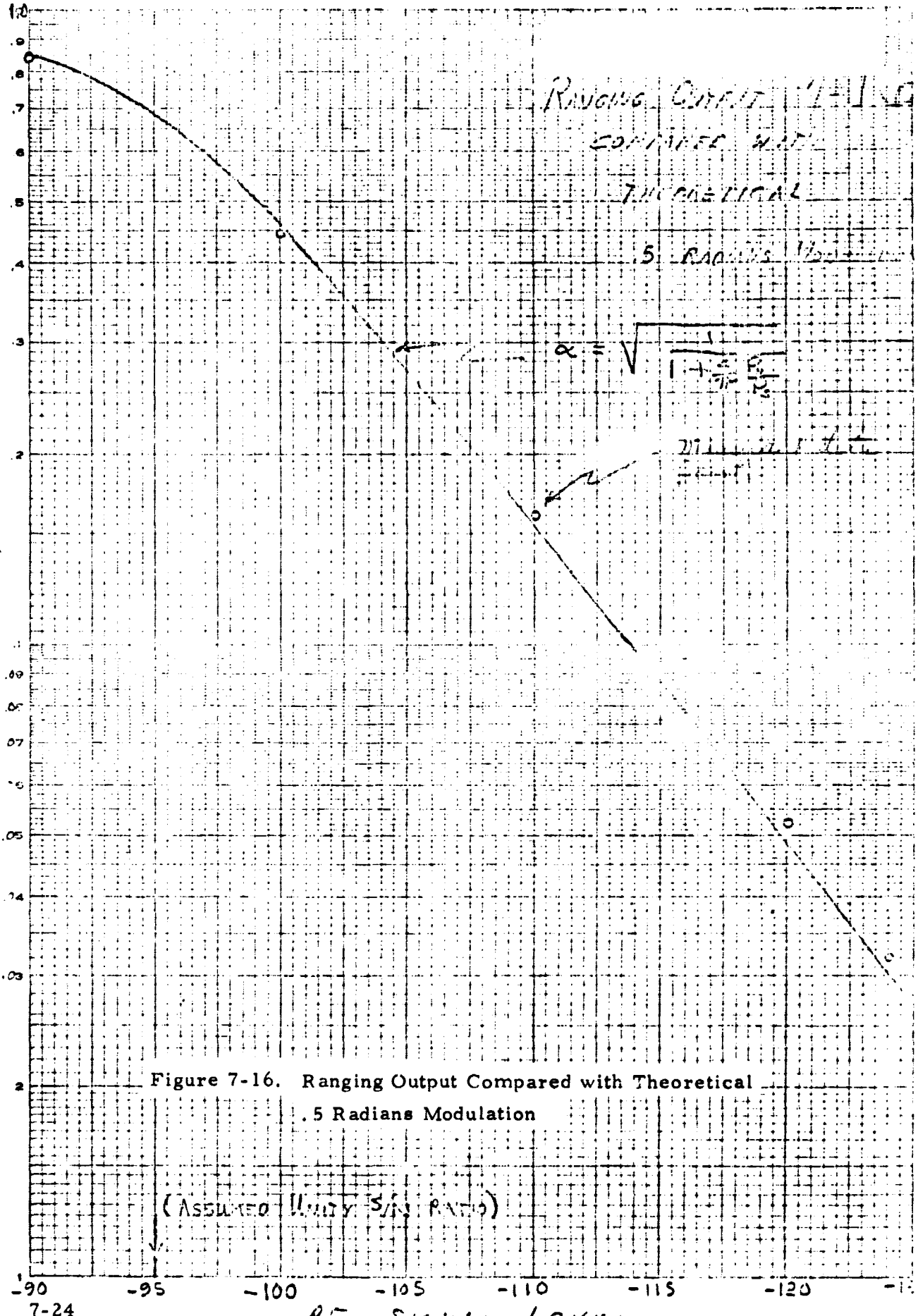


Figure 7-16. Ranging Output Compared with Theoretical .5 Radians Modulation

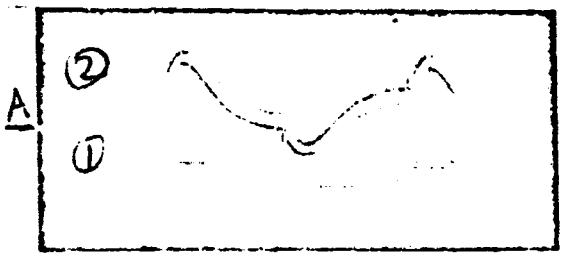
Test Data Tabulation (0.5 Radian Modulation, 1000 Hz)

RF Level	WBD Test Point Vdc	Ranging Output Mvrms	Relative Suppression
-40	+.024	193	1.0
-50	+.026	193	1.0
-60	+.026	193	1.0
-70	+.026	193	1.0
-80	+.0245	188	0.975
-90	+.013	163	0.845
-100	-.016	86	0.445
-110	-.031	32	0.16
-120	-.041	10	0.052
-124	-.044	6.2	0.032

7.2.2 Transponder Polarity

It is generally desirable to use a positive transponder ranging polarity so that the low frequency and high frequency components of the transponded signal will not be reversed. Obviously, the dc and low frequency response of the transponder has positive polarity because the transmitted carrier and the received signal are coherent. When the modulation through the ranging channel is phased positive, the overall frequency response has a dip near the crossover frequency - about 1100 Hz - as shown in the data of Test Plan paragraph 5.5.

It is interesting to look at the transponder square wave response to see how this polarity is observable. Figures 7-17A, B, and C, show the response to a 100 Hz, 0.5 radian modulation, under three conditions. (A) shows the response with positive polarity ranging, (B) shows the response with negative polarity ranging, and (C) shows the response with the ranging channel open. (C) in other words, is the response of the carrier phase lock loop only. In reality, of course, all the pictures include the response of the test transmitter, the receiver, the



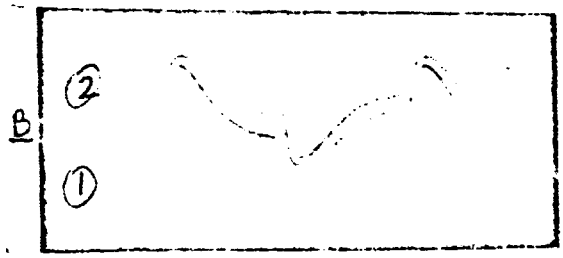
CH 1 = 2V/CM

CH 2 = .5V/CM

1MS/CM

A) Channel 1 = 100 Hz square wave modulation input to test transmitter.

Channel 2 = Demodulated 100 Hz square wave out of test receiver with normal positive ranging polarity.



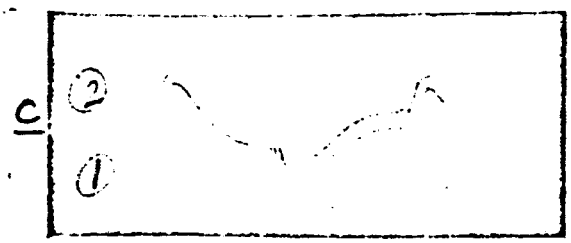
CH 1 = 2V/CM

CH 2 = .5V/CM

1 MS/CM

B) Channel 1 = 100 Hz square wave modulation input to test transmitter.

Channel 2 = Demodulated 100 Hz square wave out of test receiver with phase reversal in ranging channel.



CH 1 = 2V/CM

CH 2 = .5V/CM

1MS/CM

C) Channel 1 = 100 Hz square wave modulation input to test transmitter.

Channel 2 = Demodulated 100 Hz square wave out of test receiver with ranging channel disconnected.

Figure 7-17. Transponder Square Wave Responses

synthesizer, and the test receiver. Therefore, even though the transponder response extends down to dc, the dc response is not retained in the test receiver output.

7.2.3 Noise Figure

The receiver front end noise figure was measured directly using a HP-349A Noise Source and a HP J28-340B Noise Figure Meter. AGC voltage was applied to the receiver from an external source to simulate the effect of various signal strengths. A plot of the measured results is shown in figure 7-18.

The plot shows that the noise figure is relatively constant at about 11 db for weak signals, then at strong signals it increases rapidly. The rapid increase in noise figure at signal levels above -80 dbm results from the increase in i-f noise figure as AGC is applied.

Noise figures of 8 to 10 db were achieved during the project, however, the configuration, available at the time this test was made, had a noise figure of 11.4 db at weak signal.

7.2.4 I-F Filter Characteristics

The frequency response of each of the i-f filters was measured at the module level. The bandwidth of the rest of the circuits in the i-f are broad enough so that the overall response is determined by these two filters. The i-f input filter is located at the input of the AGC i-f module. Its frequency response is shown in figures 7-19 and 7-20. The crystal filter is located in the PDIF module just after the point where the wideband and narrowband channels split. Its frequency response is shown in figure 7-21.

7.2.5 I-F Limiter Suppression Characteristic

The limiter suppression characteristic was measured in the wideband and narrowband channels. This was measured with a 2 kHz beat note at the output of each detector and external AGC applied to correspond to the input signal level. A plot of this characteristic is shown in figure 7-22.

Figure 7-18. Receiver Noise Figure vs. Signal Level and AGC Voltage

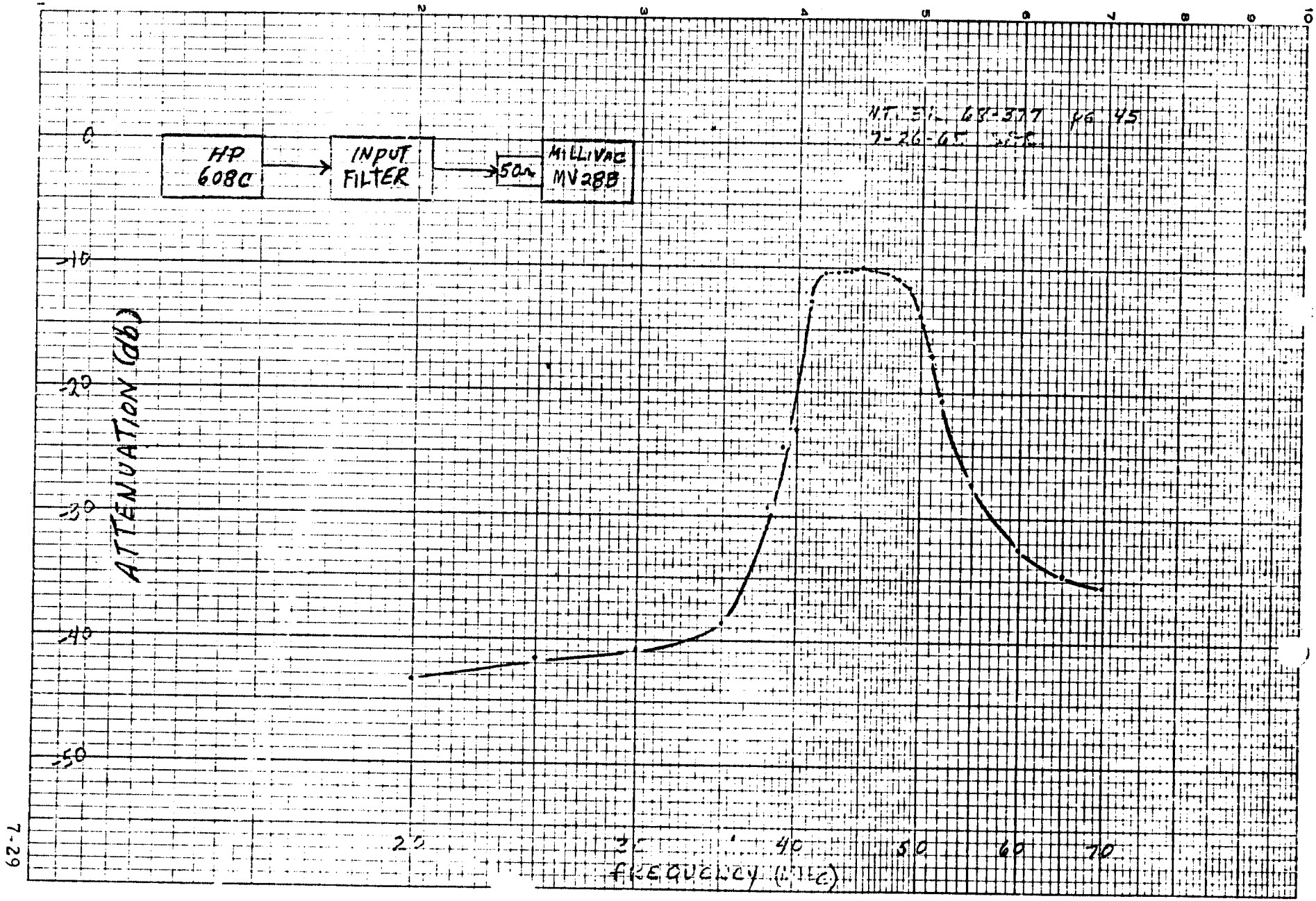
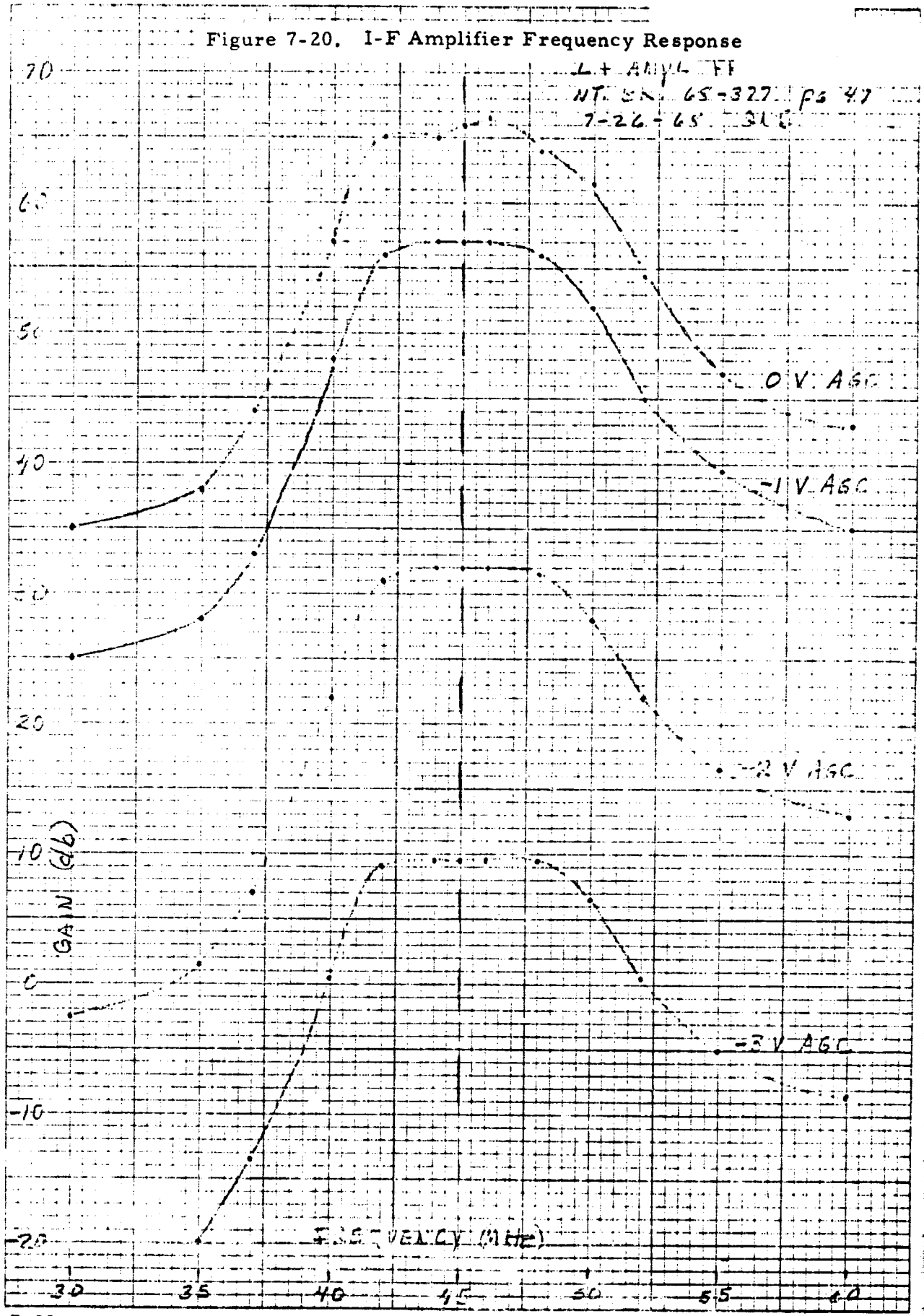
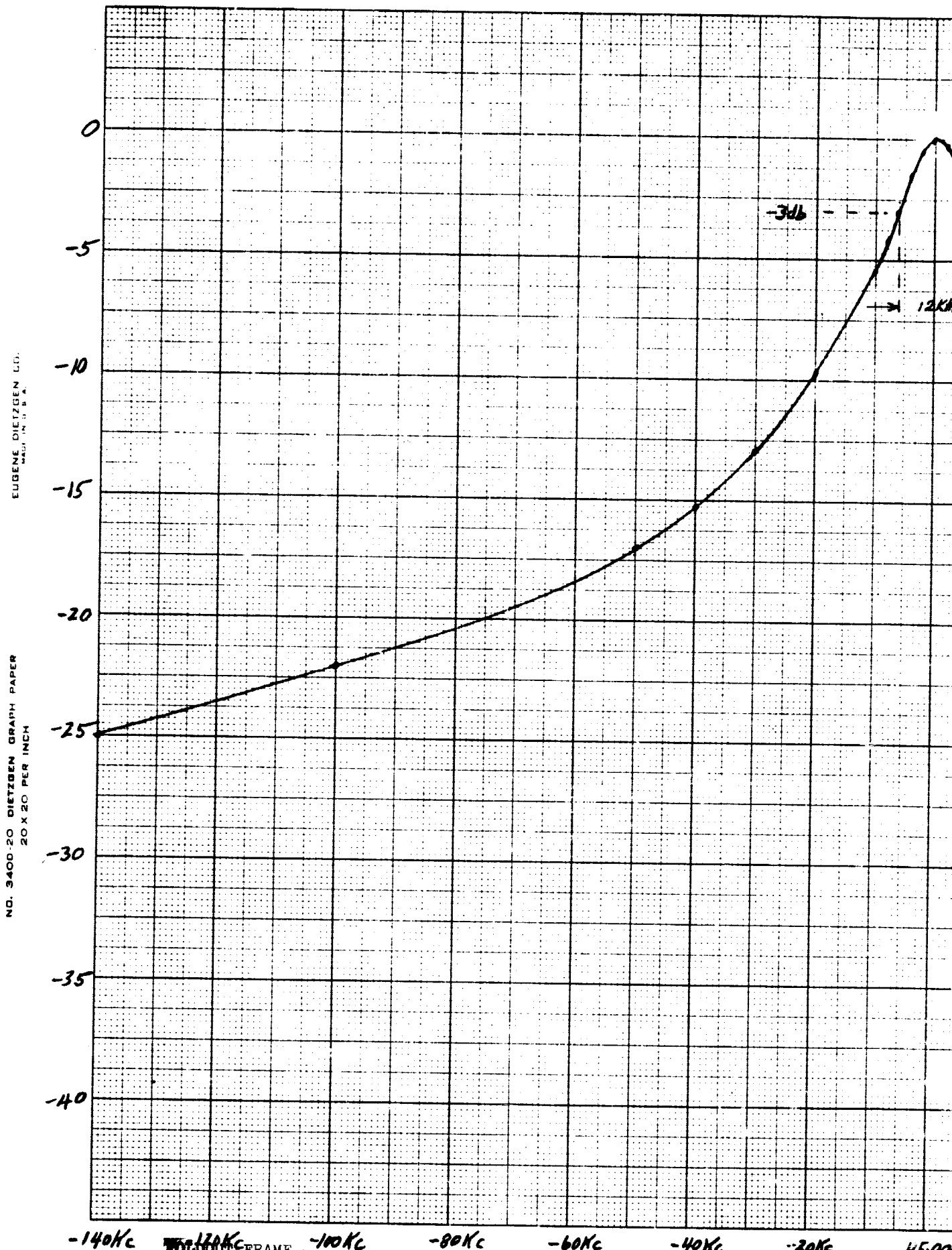


Figure 7-19. Input Filter Frequency Response

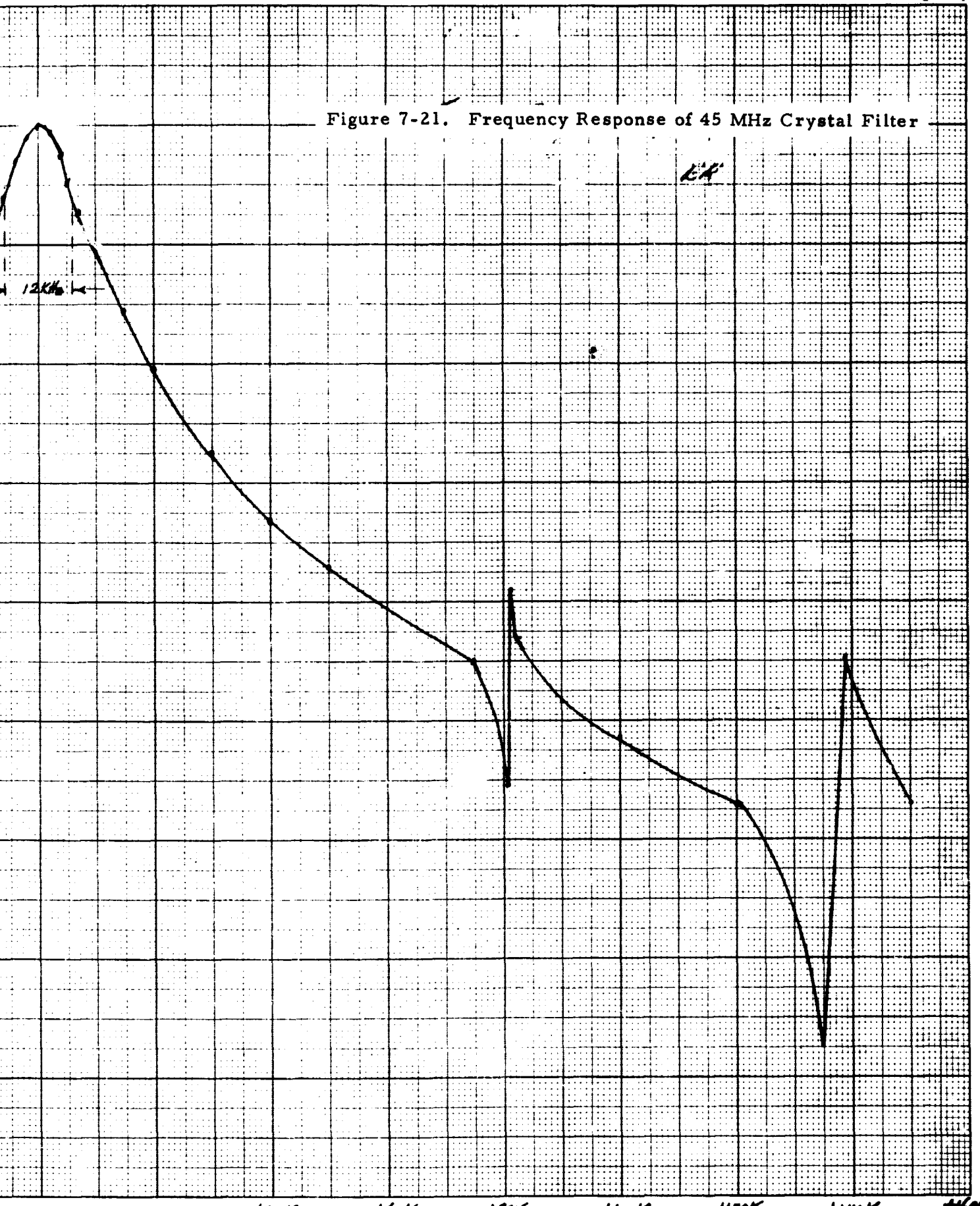
Figure 7-20. I-F Amplifier Frequency Response





FOLDOUT FRAME 1

Figure 7-21. Frequency Response of 45 MHz Crystal Filter



FOLDOUT FRAME 2

7-31.7-32

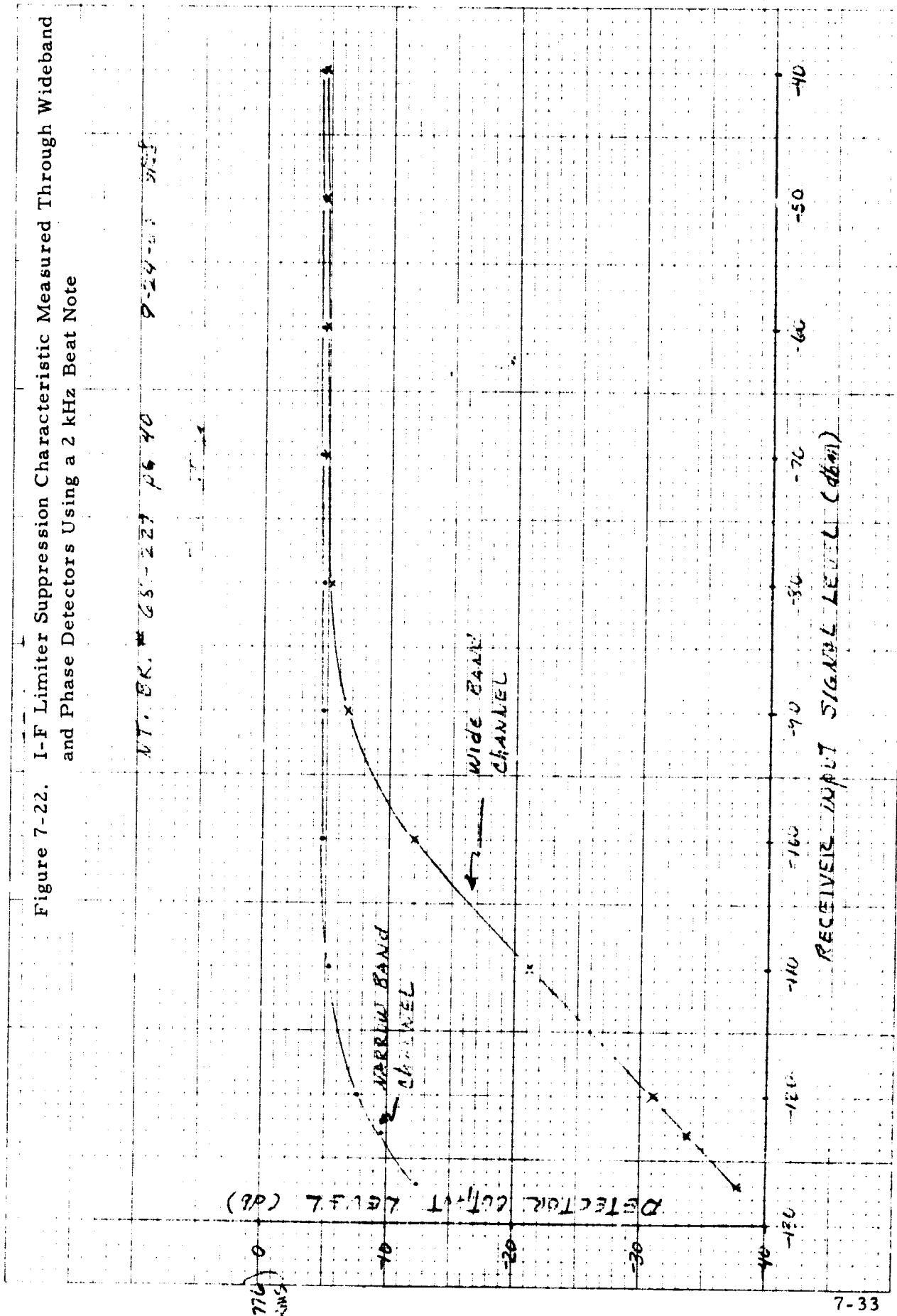


Figure 7-22. I-F Limiter Suppression Characteristic Measured Through Wideband and Phase Detectors Using a 2 kHz Beat Note

7.2.6 Loop Bandwidth vs. Signal Strength

An attempt was made to measure loop bandwidth as a function of signal strength. This was done by measuring the modulation frequency response through the transponder with the ranging loop open. The test setup block diagram and test results are shown in figure 7-23. The curves clearly show the effect of bandwidth narrowing as signal strength decreases.

There is a problem in determining the actual loop bandwidth accurately from these curves. The noise bandwidth ($2B_L$) should be given by $2B_L$ = 2 (3 db bandwidth) $\pi/2$. The problem is in determining the 3 db bandwidth from the curves since the reference level is not clearly defined. The curves appear to level off at 100 Hz, however, the loop response typically has a peak in this region and there is a measurement problem in getting more data points below 100 Hz.

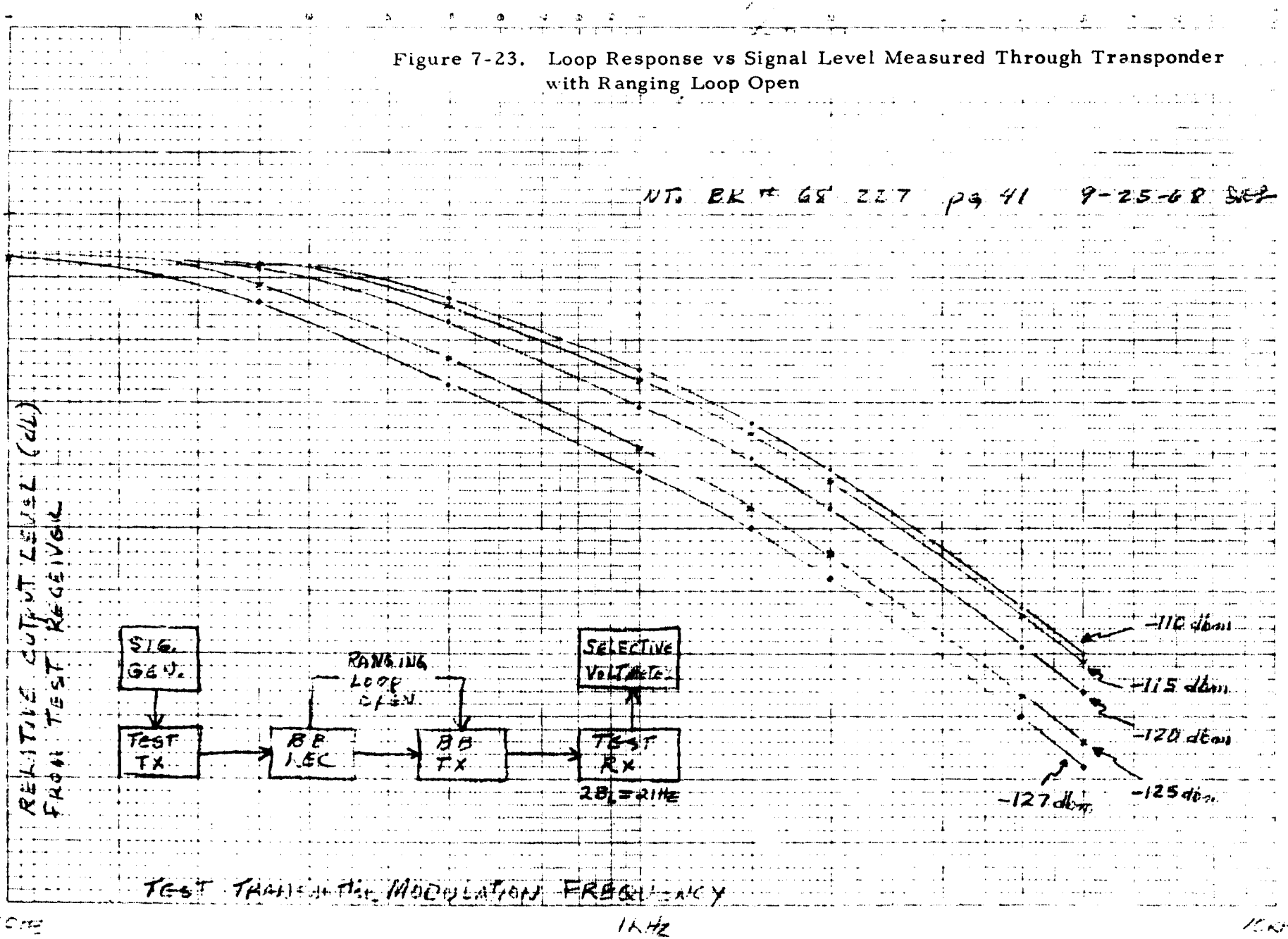
7.2.7 Ranging Turn-Around Ratio

Figure 7-24 shows a plot of ranging turn-around ratio vs. signal level. This characteristic was measured by modulating the uplink at a given index, measuring the downlink modulation index and taking the ratio. This data was measured as a function of signal level to show the effect of suppression by noise in the wideband bandwidth.

7.2.8 Acquisition Test with Doppler

This test was performed to determine the effect of doppler on the acquisition probability. The test was performed by the same method described in paragraph 5.2 of the test plan, except that the test transmitter carrier is swept at a rate of 3.5 kHz/sec. The results of this test indicate that the acquisition threshold is not degraded by the doppler. Recorder traces from these tests are shown in figures 7-25 and 7-26.

Figure 7-23. Loop Response vs Signal Level Measured Through Transponder with Ranging Loop Open



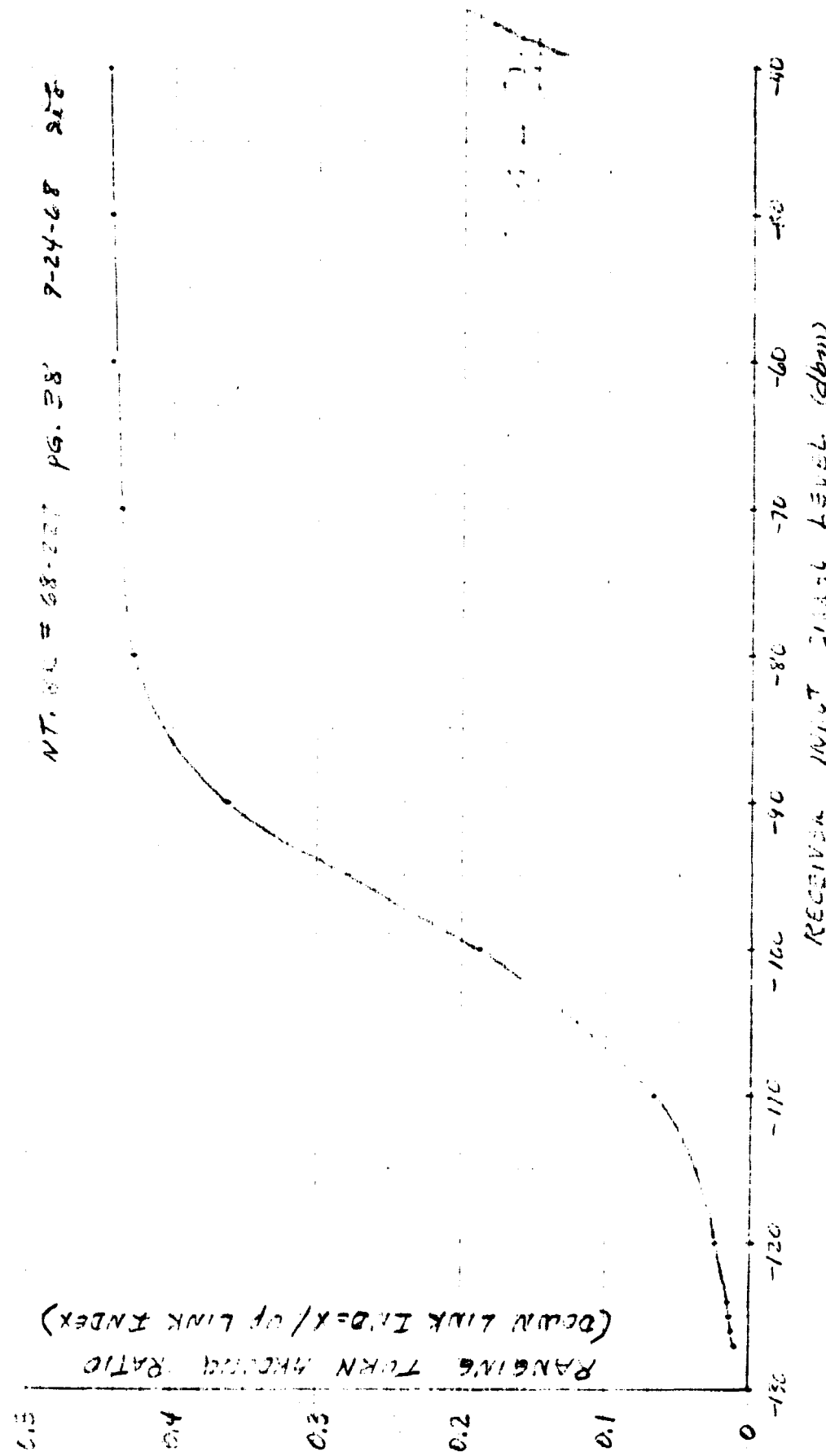


Figure 7-24. Ranging Turn Around Ratio vs Signal Level Measured with a 500 kHz Tone at an Index of 0.5 Radians on the Up-Link

9-25-68

RECEIVER ACQUISITION THRESHOLD TEST WITH TEST TRANSMITTER SWEEPING ± 30 KHz AT A RATE of 3.5 KHz/sec. RECEIVER INPUT LEVEL - 127 dbm.

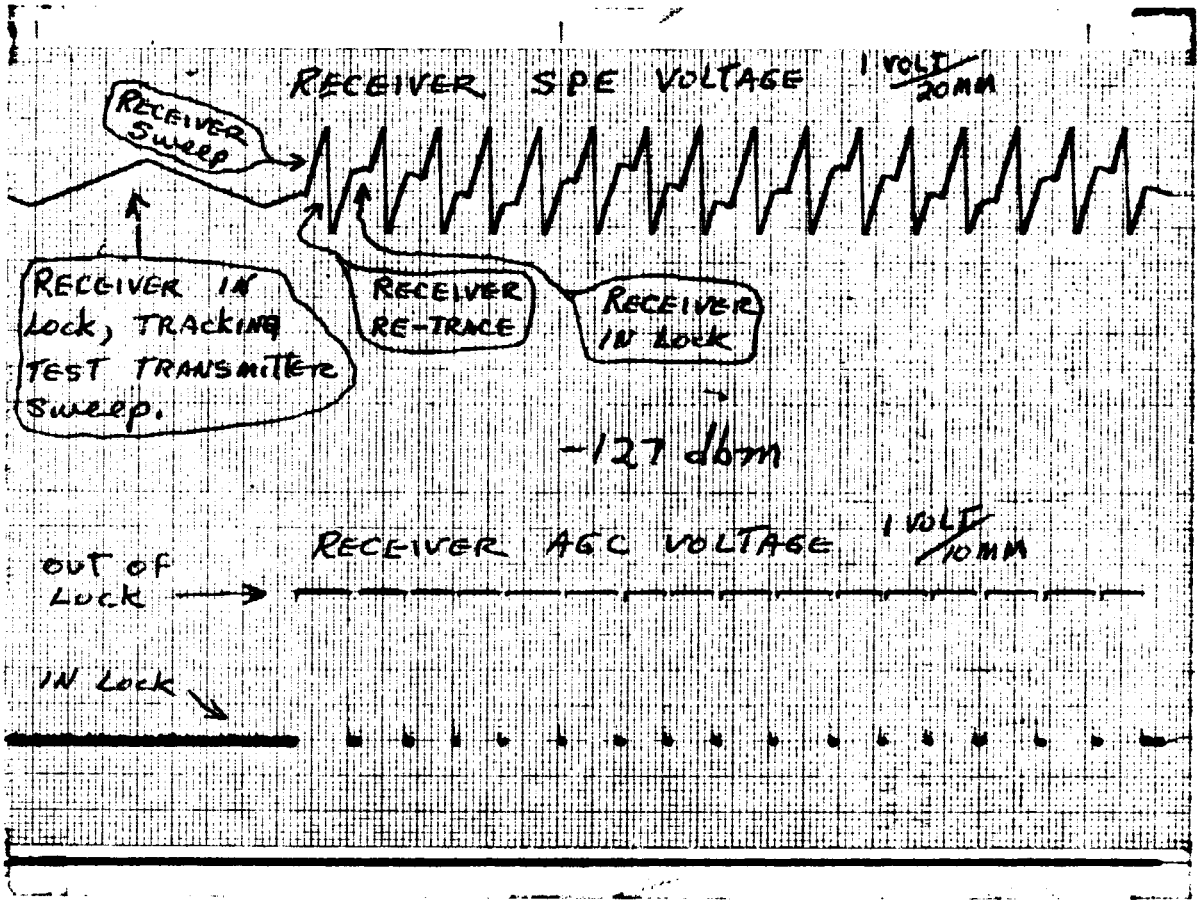


Figure 7-25. Receiver Acquired Lock 16 Times in 16 Trials

9-25-68

RECEIVER ACQUISITION THRESHOLD TEST WITH TEST TRANSMITTER SWEEPING ± 30 KHz AT A RATE of 3.5 KHz/sec. RECEIVER INPUT LEVEL −128 dbm

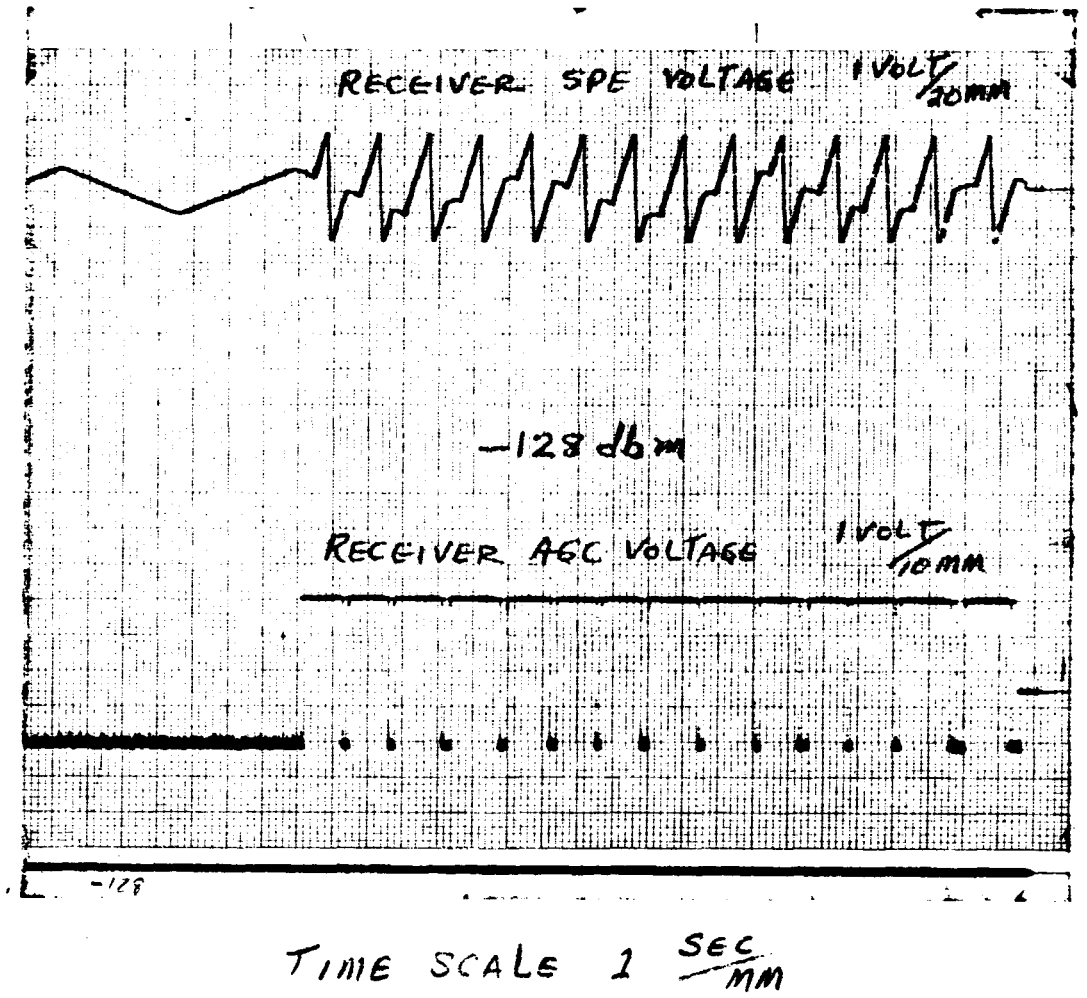


Figure 7-26. Receiver Acquired Lock 14 Times in 14 Trials

APPENDIX A

STATEMENT OF WORK

EXHIBIT "A"

STATEMENT OF WORK

1.0 INTRODUCTION

The planned analysis and circuit investigation will be directed to improving performance of the Apollo S-band system for advanced missions. The areas of investigation will include extending the operating environmental range, reducing power consumption in the receiver, improving receiver operating threshold, as well as increasing transmitter power output and information bandwidth. The investigation will also include a modulation analysis to better optimize the link for increased data handling capability. The analysis will include both theoretical investigations and breadboard circuit evaluation to arrive at a more optimum mechanization of the transponder equipment taking full advantage of the advancements in the state of the art that have occurred since the concept of the present unified S-band Equipment (USBE).

1.1 PROGRAM DESCRIPTION

The program shall include an overall analysis and investigation of circuit design areas. The results of the various analyses and investigations shall be used to arrive at a transponder configuration which will be breadboarded and tested to verify the analysis. An output of Phase I shall be an end-to-end specification for an engineering model transponder.

1.2 ANALYSIS

The analysis task shall consist of theoretical and breadboard circuit investigation of the following areas:

a. Transponder Block Diagram
b. Modulation Analysis
c. Operational Range Extension
d. Reliability Analysis
e. Packaging
f. Commonality
g. Antenna System Analysis
h. Transponder Circuit Problem Areas
i. Recommended Transponder Design
j. Transponder Breadboard
k. Engineering Model End-to-End Specification

The extent of the investigation in these various areas is described in detail under each sub-task heading.

1.2.1 Block Diagram Analysis

The block diagram analysis shall consist of a trade study to determine if a more optimized block diagram can be arrived at to provide wider information bandwidths, minimize ranging delay variations and provide more commonality between CSM and LM circuitry, and dual ratio transponders.

Since the original concept of the present USBE configuration, many advancements in the state of the art have been made which may make other mechanizations more attractive as far as performance, weight, and power consumption are concerned. Certain of these advancements include practical S-band amplifications with a low noise figure, practical power amplification at 500 MHz and higher, higher frequency crystal filters permitting a higher frequency selective i-f amplifier, stripline techniques, and high performance integrated circuits. All of these advanced techniques will be considered in arriving at a configuration yielding increased performance with adequate margin for reproducibility.

Some of the possible block diagrams to be considered for the transponder will consist of the following configuration:

a. Variable frequency receiver i-f amplifiers whose center operating frequency is coherent to the received frequency. This configuration includes the present USBE where the first i-f is now 5/221 of the received frequency. An example of an alternate configuration would be to increase this ratio to 11/221 to achieve better image rejection and reduced local oscillator radiation problems.

b. Semi-fixed frequency receiver i-f amplifiers whose center operating frequency is a fixed offset plus a coherent ratio of the received frequency. This configuration allows quite a bit of freedom in selecting the i-f operating frequency but has added complexity in synthesizing the local oscillator frequency since it is produced by mixing a fixed frequency source with the coherent voltage controlled oscillator (vco).

c. Fixed frequency i-f amplifiers where the center frequency is not coherent to the received frequency. This is accomplished by using an "offset oscillator" for the phase detector reference and mixing the coherent vco with this oscillator to produce a variable local oscillator injection source that follows the incoming frequency variations in a manner to produce a constant frequency output from the mixer. This arrangement allows a major portion of the transponder receiver design to be fixed and relatively independent of operating frequency to facilitate greater commonality between LM, CSM, and dual ratio transponders.

Other configurations involving combinations of these types as well as tradeoffs between one i-f versus two i-f frequencies will be evaluated. In the transmitter, tradeoff studies will be performed considering multiplication sequence, point of power amplification, and modulation. A spurious signal analysis will be done on the most promising configuration.

1.2.2 Modulation Analysis

The modulation analysis shall consist of two parts. (a) Investigation of methods to improve the modulation efficiency and minimize existing problems utilizing the present modulation spectrum. This analysis of the first part shall consist of the following:

a. Modulation sensitivity variation analysis.
b. Modulation linearity requirements.
c. Adjacent Channel interference.
d. Turnaround ranging.

(b) Investigation of other modulation schemes that could provide increased data rates, minimize adjacent channel and cross modulation interference problems.

1.2.2.1 PART A MODULATION ANALYSIS

1.2.2.1.1 Modulation Sensitivity Variation

The first part of this investigation shall be to identify the major sources of variation. Although the Block II CSM transponder has actual performance variations which are minor over its present operating environmental range, extending this range may result in intolerable variations. Tests shall be made to determine the extent of the variations to be expected when operating over a wider environmental range. Methods to reduce these variations as well as the expected practical residual variations may be an output of this analysis.

1.2.2.1.2 Modulation Linearity

An analysis of the effect of modulation linearity on the cross modulation inference problem shall be made. A major source of modulation nonlinearity is in the phase nonlinearities of the filters following the modulator. As the information bandwidth is widened, this nonlinearity can be the limiting factor upon performance. Utilizing all pass type of modulators, wider linear deviations can be obtained in the modulator stage allowing the modulation to be done closer to the final output frequency. The results of the linearity requirement analysis will be used to determine an optimum point to modulate the transmitter.

1.2.2.1.3 Adjacent Channel Interference

The adjacent channel interference problem existing when simultaneous transmissions are made to the LM and CSM transponders shall be investigated in detail to determine if more optimum filtering can be done to reduce this problem. Narrow band r-f or i-f filters tend to generate a potential range code time delay variation problem. The major effects of the interference shall be determined and methods to minimize these effects will be explored.

1.2.2.1.4 Turnaround Ranging Channel

The ranging channel in the transponder shall be analyzed to determine methods to improve the operation of the ranging function. In the present configuration, the base bandwidth of the ranging function

is about 1.5 MHz. Since essentially all the ranging information is contained in less than 1-MHz bandwidth, the optimum bandwidth is less than the present 1.5 MHz. The up-link voice and command subcarrier information is also contained in the turned around ranging spectrum and subtracts power from other down-link channels as well as providing potential interference spectrum lines. Combination of filtering, processing, and limiting shall be considered to determine a more optimum ranging channel.

1.2.2.2 PART B MODULATION TECHNIQUES

1.2.2.2.1 Multiplexing Analysis

The present use of subcarriers combined with direct modulation on the carrier for the range function does not result in the most efficie utilization of the transmitted power. Cross modulation interference occurs between the different function channels, separation of the desired down-link ranging information from the up-link voice and command is difficult, and troublesome adjacent channel interference spectrum lines are generated. Various different methods of multiplexing shall be studied and evaluated as to their capability of reducing these effects as well as providing capability for expanded down-link data rates and reducing sensitivity to modulator nonlinearities and drift problems. The methods included shall be digital encoding and multiplexing so that the carrier can be directly modulated by the digital stream, subcarrier techniques, and hybrid combinations of these two techniques.

1.2.3 Operational Range Extension Analysis

1.2.3.1 Introduction

To effectively extend the range of the present transponder, a reduction must be made in the system noise figure as well as an increase in effective power output of the transmitter. Medium power output amplifiers exist in the present equipment and high power amplifiers are under development in the industry that could be used to further increase this power output. However, it would be highly desirable to provide medium power output as an integral part of the transponder to avoid adding the extra complexity of a separate power amplifier to satisfy the medium output power level requirements, as well as providing the exciter for the high power requirements.

1.2.3.2 Noise Figure Reduction

Advancements in the state of the art that have occurred since the design of the present USBE provide the means to significantly reduce the system noise figure of the transponder. One of the methods that could be used is low noise r-f amplification before mixing. This method when used in conjunction with higher frequency crystal filters could result in a

receiver with a single conversion, with a resultant possible simplication of the receiver. Other methods of reducing the noise figure such as choosing the optimum i-f and optimizing the mixer/i-f amplifier combination shall be investigated.

The most promising method resulting from the initial analysis and trade study shall be breadboarded to verify the results of the analysis.

1.2.3.3 Medium Output Power Wideband Transmitter

A study shall be made to determine the feasibility of operating the power amplifier at higher than the present USBE design frequencies to reduce weight, size, and number of components required.

A trade study shall be made to determine the operating frequency for the phase modulator.

During the breadboard phase, a strip transmission line phase modulator may be developed. Power output efficiency will be optimized for minimum prime power requirements.

1.2.4 Reliability Analysis

This analysis shall include methods of increasing the reliability of the transponders for long duration missions, and shall also include the following:

a. Identification of the parts with the lowest reliability that are used in the present transponder.

b. Determination as to which to these parts can be replaced with more reliable parts which are now available.

c. Recommendation of methods of increasing performance reliability where no satisfactory substitutes are available.

d. Provision of a recommended high-rel parts list that could be used in design with the view of reducing the type and total number of components.

1.2.5 Packaging Analysis

The objective of the packaging study shall be to develop a standardized packaging concept which shall meet the CSM, LM, and SIV-B/IV environmental requirements. Weight and volume trade studies shall be made and documented for the various packaging concepts.

A thermal and vibration analysis shall be performed on the resultant package.

The output of this analysis shall be a recommended design concept.

1.2.6 Commonality Analysis

Using the results of the block diagram studies and packaging analysis, a summary trade study shall be performed to determine the maximum practical commonality utilizing interchangeable modules that could be achieved between LM and dual ratio transponders.

This analysis may also utilize the results of the transmitter part of the program to determine whether a simple low weight FM transmitter could be achieved to allow inclusion in the LM transponder envelope restrictions.

1.2.7 Antenna System Analysis

Methods of obtaining antenna track error signals such as monopulse shall be investigated along with sequential lobing and electronic steering as to their comparative performance and practicality. Also included in this trade study shall be various techniques such as automatic selection of optimum signal path, cross correlation and diversity reception.

1.2.8 Transponder Circuit Investigation

This effort shall include an analysis of various circuits where significant performance improvement can be made. In the receiver portion of the transponder, the major effort shall be expended on the phase-lock loop function. In the transmitter portion, it shall consist of work on the multiplier/modulator circuitry.

1.2.8.1 Phase-Lock Loop

Alternate methods of improving receiver performance shall be investigated. These methods shall include the following:

a. Third order loops
b. Use of a discriminator to aid phase tracking
c. Self-acquisition
d. Use of limiting in place of AGC

Promising techniques resulting from the analysis will be breadboarded and tested to provide experimental performance data to back up the analysis effort.

1.2.8.2 Transmitter

A transmitter circuit investigation shall consist of breadboarding a transmitter and phase modulator utilizing the latest techniques.

1.3 BREADBOARD MODEL TRANSPONDER

The conclusions derived from the analysis and circuit investigation efforts shall be used to derive a preliminary transponder configuration. A complete electrical breadboard transponder, except for the power supply, will be assembled. A test

program shall be conducted to check critical parameters and verify the soundness of the transponder configuration.

1.4 DOCUMENTATION

The documentation requirements of this program shall consist of the following:

a. Monthly Reports (including Cost Reports)
b. Final Report - In additional to the requirements of Clause C.9, the final report will include, but will not be limited to the following:

   1. Results of analysis, trade studies, circuit investigations of:

      a. Transponder Block Diagram
      b. Modulation Analysis
      c. Operational Range Extension
      d. Reliability Analysis
      e. Packaging
      f. Commonality
      g. Antenna System Analysis
      h. Transponder Circuit Problem Areas
      i. Recommended Transponder Design

   2. Results of evaluation of breadboard transponder

   3. End-to-End specification for engineering model transponder
c. Test Plan (two weeks prior to intended use for review)

1.5 DESIGN REVIEW

The Contractor shall conduct a conceptual design review at his facility for MSC personnel. This design review shall be conducted at the approximate midpoint of the program.

APPENDIX B

COMPARISON OF ADVANCED DESIGN TO APOLLO BLOCK II USBE TRANSPONDER

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COMPARISON OF ADVANCED DESIGN TO APOLLO BLOCK II USBE TRANSPONDER

Receiver	Apollo Block II Transponder	Advanced Transponder
Type	Double Conversion, Type I phase lock loop	Single conversion, Type II phase lock loop (velocity error reduced to zero)
Noise figure	10 db	4 db (projected)
Acquisition Time	By sweeping ground transmitter, >30 seconds at -114 dbm	By automatic self acquisition, 6.5 seconds at -127 dbm
Acquisition Threshold	-114 dbm	-127 dbm
Tracking Threshold	-127 dbm	-127 dbm
Acquisition Range	±90 kHz	±70 kHz
Dynamic Range	-51 to -127 dbm	-40 to -127 dbm
Ranging Bandwidth	1.5 MHz	2 MHz
Transmitter		
Power output	.275 to .400 watts	13 to 18 watts
Efficiency	4 to 7%	13 to 18%

Transmitter	Apollo Block II Transponder	Advanced Transponder
Modulation bandwidth	1.5 MHz	3 to 10 MHz
Modulator frequency	76 MHz	572 MHz
Power amplifier frequency	152 MHz	1144 MHz
Power amplifier circuitry	Discrete	Stripline
General		
Power Output	20 watts (with TWT PA)	18 watts
Input power (based on redundant transponders)	120 watts R-T 10 watts R (with TWT PA)	140 watts R-T 2 watts R
Extent of change required for new input frequency, output frequency or transpond frequency ratio	Redesign	Slight modifications
Reliability, failure rate	3.05%/1000 hrs.	1.5%/1000 hrs.
Size	1923 cu. inches	630 cu. inches
Weight	62 lbs	30 lbs.

APPENDIX C

PERFORMANCE SPECIFICATION

APPLICATION	
NEXT ASSEMBLY	USED ON

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
X1	Preliminary Release	12/17/68	[illegible]

REV STATUS OF SHEETS	REV	SHEET

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY

FOR PARTS LIST SEE

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE

MATERIAL:

DR BY	Terry Nelson
CHK BY	
MFG	PROJ NO.
CONTR NO.	
RELEASE NOTICE	
APPROVED D. Wolfe	DATE 11-25-68
APPROVED	DATE

MOTOROLA INC. Government Electronics Division / AEROSPACE CENTER 8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA

PERFORMANCE SPECIFICATION

ADVANCED S-BAND TRANSPONDER
(Engineering Model Use Only)

SIZE	CODE IDENT NO.	
A	94990	12-P08050A

SCALE | SHEET 1 OF 14

3.0 PERFORMANCE

3.1 FUNCTIONAL CHARACTERISTICS

The equipment shall perform per the functional characteristics detailed in the following paragraphs and generalized as follows:

(1) Receive a phase-modulated r-f carrier in the frequency range between 2030 and 2120 MHz from an antenna system.

(2) Transmit a phase-modulated r-f carrier in the frequency range between 2200 and 2300 MHz which is coherent with the received r-f carrier when operating in the coherent mode, or derived from an auxiliary oscillator when operating in the noncoherent mode.

(3) Detect a ranging code signal modulated on a received r-f carrier and phase-modulate the transmitted carrier with this signal, maintaining the polarity and phase-coherency with the received signal.

(4) Detect subcarrier signals modulated on the received r-f carrier.

(5) Phase-modulate telemetry or other data in the frequency range between 1 and 2 MHz on the transmitted r-f carrier.

(6) Upon command inputs, provide switching to the various modes of operation.

3.2 ELECTRICAL POWER SOURCE

The equipment shall operate from a source with the characteristics specified below.

3.2.1 Input Power

The equipment shall operate on vehicle unregulated 28 Vdc power except that the voltage level may vary between 22.0 and 29.5 Vdc. The

equipment shall withstand application of up to 30 Vdc of the reverse polarity. When receiving and transmitting, the nominal dc power drain shall be 160 W. When receiving only, the nominal dc power drain shall be 2 watts.

a. Maximum voltage 29.5 Vdc

b. Nominal voltage 24.5 Vdc

c. Minimum voltage 22.0 Vdc

3.2.2 ON/OFF Control

The equipment shall have power applied continuously. ON/OFF control shall be supplied to the equipment as specified in the appropriate parts of this document. When in the OFF state, no power shall be drawn by the equipment from the unregulated 28 Vdc power source.

3.2.3 Isolation

The input prime power circuits and the command input circuits shall be isolated from the unit case, all other circuits, and each other. The isolation shall be 1 megohm dc minimum with ±50 Vdc applied between isolated functions.

3.3 INPUTS/FUNCTION

The equipment shall operate with the Inputs/Functions herein under the following headings:

a. RF Input (Coaxial)

b. Command Inputs

c. Composite Baseband Channel

d. PRN Ranging Channel

3.3.1 RF Input

The equipment shall receive any preselected frequency within the range 2033 to 2122 MHz. The center frequency shall be as specified. The input frequency variations shall be within ±84 KHz of the specified center frequency. The input frequency rate of change shall not exceed ±0.00019% per second (approximately 3.5 KHz/second).

3.3.1.1 Input Impedance

The input impedance at the r-f input shall be 50 ohms nominal with a maximum VSWR of 1.3:1 at the specified center frequency.

3.3.1.2 Source Impedance

The equipment shall perform as specified herein when driven from a source impedance of 50 ohms nominal with a maximum VSWR of 2:1.

3.3.1.3 Susceptibility of Interfering Signals

The equipment shall perform as specified herein when subjected to an interfering received r-f carrier separated 5 MHz or more from the specified r-f carrier. The interfering r-f carrier shall be angle-modulated at one radian index with a simulated PRN ranging code. The signal power of the interfering signal shall not exceed that of the specified r-f signal.

3.3.1.4 RF Input Level

The operating dynamic range of the r-f carrier shall be -40 dbm to -126 dbm. No damage shall result from r-f carrier input levels up to -3 dbm. The equipment shall operate normally when the r-f carrier input level varies up to 15 db peak-to-peak at a rate of 5 Hz or less.

3.3.1.5 RF Carrier Threshold

For any input frequency within the limits specified in 3.3.1, the r-f carrier threshold shall be -127 dbm or lower. The r-f carrier threshold is defined as the carrier signal level for which the equipment will maintain lock for one minute with a 90% probability.

3.3.1.6 Carrier Acquisition

When an unmodulated r-f carrier meeting the requirements of 3.3.1 and 3.3.1.4 is applied at the r-f input, the phase lock acquisition shall have a 90% minimum probability of occurring within 6.5 seconds.

3.3.1.7 Modulation Characteristics

The ranging and subcarrier modulation indices range shall each be between 0.1 and 1.0 radian. The ranging and subcarrier modulation shall be on separately or simultaneously.

3.3.2 Command Inputs

The equipment shall accept the following command inputs:

a. Turn-On Command

b. Turn-Off Command

c. Ranging Squelch On (prohibits equipment from unsquelching ranging channel)

d. Ranging Squelch Off (allows equipment control of ranging channel)

e. Coherent Mode On (allows equipment control of RF Output)

f. Coherent Mode Off (prohibits equipment from operating in coherent mode)

3.3.2.1 Command Characteristics

Each input command shall have the following characteristics:

a.	Amplitude	False	0 to 1 Vdc
		True	+22 to 29.5 Vdc
b.	Pulse Width		125 ±25 milliseconds measured at the 50% amplitude points

3.3.2.2 Command Input Impedance

Each command input circuit shall have an input resistance of 200 ohms minimum. The circuit time constant (L/R) shall be 1.5 milliseconds maximum.

3.3.3 PRN Ranging

The equipment shall:

(1) Coherently demodulate the ranging signal to baseband.

(2) Band limit the demodulated signal.

(3) Combine this signal into a composite baseband signal to phase modulate the transmitted carrier.

3.3.3.1 Ranging Delay

The time delay of a satellite range code through the equipment shall be 2600 nanoseconds maximum over all environmental conditions. The time delay variation shall not exceed 100 nanoseconds over the combined conditions of (a) the specified flight environmental conditions, (b) changing the r-f input modulation index from 0.1 to 1.0 radian, and (c) changing the r-f input signal level from -40 to -120 dbm.

3.3.3.2 Polarity

The polarity of the incoming PRN ranging code shall be maintained at the r-f output.

3.3.3.3 Turnaround Index

The ranging code modulation index on the transmitter carrier shall be continuously field adjustable within the range of 0.1 to 1.0 radian when the received carrier index is at a 1 radian reference.

3.3.3.4 Ranging Squelch

The ranging squelch channel shall be squelched OFF when the equipment is not locked to a received carrier.

3.3.3.5 Ranging Command

The ranging signal channel shall be turned OFF or ON by a command signal as specified in 3.3.2. In the OFF condition, this command shall have priority over 3.3.3.4.

3.3.4 Composite Baseband Channel

The equipment shall provide a coaxial wideband modulation input to accept baseband signals as specified.

3.3.4.1 Modulation Sensitivity and Frequency Response

The nominal phase modulation sensitivity of the transmitted carrier shall be 43 degrees per volt. The modulation sensitivity shall not vary more than ±10% from nominal over the frequency range of 100 Hz to 2 MHz. The sensitivity shall not vary more than ±10 % from values measured under laboratory ambient conditions over all flight environmental conditions. The peak modulation capability shall be 3.0 radians minimum.

3.3.4.2 Modulation Distortion

The equipment shall meet the following harmonic distortion requirements

when the transmitted carrier is deviated 1.5 radians by a sinusoidal input. This only applies to distortion products which fall within the baseband modulation bandwidth of 2 MHz.

a. The second order harmonic distortion product shall not exceed 2.5%.

b. The third order harmonic distortion product shall not exceed 4.0%.

3.3.4.3 Modulation Input Level

The modulation input level shall vary from zero volts to a maximum input level not to exceed 10 volts peak-to-peak.

3.3.4.4 Modulation Source Impedance

The modulation source impedance will be 100 ohms maximum.

3.3.4.5 Modulation Input Impedance

The input resistance shall be 5000 ohms ±15% with a shunt capacitance not to exceed 50 picofarads.

3.3.4.6 Modulation Polarity

A positive polarity voltage shall cause the carrier phase to lead from nominal or rest phase.

3.4 OUTPUTS/FUNCTIONS

The equipment outputs/functions shall be as listed below, and shall have the characteristics as described in the succeeding paragraphs:

a. RF Output (coaxial)

b. Subcarrier Output (coaxial)

c. Diagnostic Monitor Outputs

3.4.1 RF Carrier Frequency

The equipment shall transmit any preselected frequency within the range of 2200 to 2300 MHz. The center frequency shall be specified.

3.4.1.1 RF Output Power

The nominal RF power output shall be 20 watts.

3.4.1.2 RF Output Characteristics

The r-f output shall be coherent with the received signal when the equipment is phase-locked to a received carrier. When the equipment is not phase-locked to a received carrier or in the non-coherent mode, the r-f output shall be derived from an internal oscillator. The output frequency shall be 240/221 of the r-f input frequency in the coherent mode and within ±0.002% of the specified frequency in the non-coherent mode.

3.4.1.3 Phase Noise

The short term phase noise shall not exceed the limits listed below when measured in a phase lock receiver ($2BL_O$ bandwidth of 200 Hz).

MODE	MAXIMUM LIMIT
Coherent	
Static Operation	1^{o}RMS
Random Noise Vibration	12^{o}RMS
Non-Coherent	
Static Operation	2.5^{o}RMS
Random Noise Vibration	12^{o}RMS

3.4.1.4 RF Output Coherent Mode Timing

The r-f output shall switch from non-coherent to coherent mode within 70 milliseconds after the equipment is phase locked to the received carrier. The r-f output shall switch from coherent to non-coherent mode in 0.5 to 2.0 seconds after the equipment loses phase lock.

3.4.2 Subcarrier Output

The equipment shall coherently demodulate the subcarrier frequencies that are phase modulated on the received carrier.

3.4.2.1 Subcarrier Output Bandwidth

The amplitude frequency response of the subcarrier channel from the

received input to the output shall conform to the following:

Frequency	Maximum Output	Minimum Output
10 KHz (Reference)	0 db reference	
2 KHz to 2 MHz	+ 1 db	-4 db
Below 2KHz	As determined by the phase locked loop tracking characteristics	

3.4.2.2 Subcarrier Output Level

The composite subcarriers output level shall be 1/2 volt per radian ±20% when the received carrier power is between -40 dbm and -90 dbm, and the modulation index is one radian.

3.4.2.3 Subcarrier Output Squelch

The output shall be squelched when the equipment is not phase locked to a received carrier.

3.4.2.4 Subcarrier Output Linearity

The subcarrier output linearity shall be within ±10 % of the curve described by:

$E_o = K J_1(\theta), \quad 0.1 \leq \theta \leq 1.5$

E_o = output voltage

θ = carrier phase deviation in radians

K = equipment scale factor

J_1 = first order Bessel function

3.4.2.5 Subcarrier Output Signal-to-Noise

The signal plus noise power to noise power at the subcarrier output shall be no less than 12 db in any 20 KHz bandwidth over the range of

10 KHz to 2 MHz when the r-f input level is at -100 dbm and the modulation is a single tone in the appropriate band deviating the carrier 1 radian. The signal-to-noise ratio shall increase proportional to increasing r-f input until a signal-to-noise ratio of at least 40 db is achieved.

3.4.2.6 Subcarrier Source Impedance

The subcarrier source impedance shall not exceed 100 ohms.

3.4.2.7 Subcarrier Load Impedance

The load resistance shall be no less than 1000 ohms with a shunt capacitance of 100 picofarads maximum.

3.4.3 Diagnostic Monitor Output

The equipment shall have the following diagnostic monitoring outputs to provide indication of operational status. The source impedance on all diagnostic outputs shall be 10 kilohms maximum. The output voltages shall be as specified when measured into an open circuit.

a. Voltage Monitor

b. ON/OFF Monitor

c. Temperature Monitor

d. Loop Stress Monitor (LSM)

e. Tracking Signal Present Monitor (TSPM)

f. Coherent Ready Mode Monitor (CRMM)

g. Ranging Channel Mode Monitor (RCMM)

3.4.3.1 Voltage Monitor

A monitor output shall be provided to indicate that the power supply

is energized. A voltage of +2.9 ±0.4 volts shall indicate normal operation.

3.4.3.2 ON/OFF Monitor

A monitor output shall be provided to indicate the status of the power control relay. The output voltage shall be +3.5 to +5.5 Vdc when the equipment is commanded ON. The output voltage shall be -0.4 to +0.6 Vdc when the equipment is commanded OFF. Excitation voltage for the monitor shall be from an external source.

3.4.3.3 Temperature Monitor

A temperature sensor shall be provided to monitor average case temperature. Excitation voltage shall be from an external source. The output voltage shall indicate equipment operating temperatures over a 0 to 5 Vdc range.

3.4.3.4 Loop Stress Monitor (LSM)

The LSM shall provide a DC voltage output indicative of the phase error voltage applied to the equipment internal voltage controlled oscillator. The DC level corresponding to no loop stress (phase error) shall be 2.9 ±0.2 Vdc. The scale factor shall be 16 ±3.2 millivolts per KHz offset of the r-f carrier frequency over the voltage range of 0 to 5 Vdc.

3.4.3.5 Tracking Signal Present Monitor (TSPM)

The TSPM output voltage shall be 3.5 to 5.5 Vdc when the equipment is phase locked on an r-f carrier. When the equipment is not locked on a carrier, the TSPM output voltage shall be -0.4 to +0.6 Vdc.

3.4.3.6 Coherent Ready Mode Monitor (CRMM)

The CRMM output voltage shall be 3.5 to 5.5 Vdc when the coherent transmit relay is in the coherent ready position. When the coherent transmit relay is in the non-coherent position the CRMM output voltage shall be -0.4 to 0.6 Vdc.

3.4.3.7 Ranging Channel Mode Monitor (RCMM)

The RCMM output voltage shall be 3.5 to 5.5 Vdc when the ranging channel mode control relay is in the ranging ON position. When the ranging channel mode control relay is in the ranging OFF position, the RCMM output voltage shall be -0.4 to 0.6 Vdc.

3.5 ENVIRONMENTAL

The equipment shall be capable of meeting the performance requirements of this specification while being subjected to the following environmental conditions. .

3.5.1 Vibration

Vibration shall be applied along each of three mutually perpendicular axes at the levels specified below. Duration shall be 15 minutes in each plane for a total of 45 minutes.

a. Random Vibration

20 - 59 Hz	Constant 0.04 g^2/Hz
59 -126 Hz	9 db/octave linear increase*
126 -700 Hz	Constant 0.4 g^2/Hz
700 -900 Hz	18 db/octave linear decrease*
900 -2000Hz	Constant 0.09 g^2Hz

*Linear is defined as linear on log-log plot of spectral density vs. frequency.

3.5.2 Shock

The equipment shall be capable of operation as specified after being subjected to 3 shocks in each of six directions. The shock pulse shall be a 78g sawtooth with 11±1 mg rise time and 1±1 mg decay time.

3.5.3 Acceleration

The equipment shall be capable of operation as specified while being subjected to a sustained acceleration of 100 g's. The duration of the acceleration shall be one minute in each of the six directions.

3.5.4 Humidity

The equipment shall be capable of operation as specified after being exposed for 120 hours of humidity-temperature cycling as defined in MIL STD -210 Method 507, Procedure I.

3.5.5 Temperature-Pressure

The equipment shall be capable of operation as specified herein during and after exposure to a vacuum of 10^{-4}mm of Hg and over the temperature range of -30°F to 140°F.

3.6 DESIGN AND CONSTRUCTION

3.6.1 Weight

The weight of the equipment shall not exceed 9.0 kilograms (19.9 lbs).

3.6.2 Volume

The volume of the equipment shall not exceed 6900 cubic centimeters (420 cubic inches).