TEXAS INSTRUMENTS INCORPORATED
Apparatus Division
13500 North Central Expressway
Dallas, Texas

FINAL ENGINEERING REPORT

INTEGRATED CIRCUIT SEQUENCE GENERATOR

8-66348-Final

JPL Contract No. 950693

25 June 1964

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Prepared for
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

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TABLE OF CONTENTS

APPENDIX

LIST OF ILLUSTRATIONS

LIST OF TABLES

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References:
(a) Texas Instruments Proposal No. A63-109, dated 13 May 1963

(b) Jet Propulsion Laboratory Contract No. 950693, dated 26 September 1963

SECTION I

INTRODUCTION

Texas Instruments has delivered an Integrated Circuit Sequence Generator to Jet Propulsion Laboratory in accordance with References (a) and (b). The sequence generator described in JPL Design Specification Number 31243 was designed and built using only integrated circuits. The specification relating to this effort is shown in Appendix A. The primary design objective was to minimize the size and weight of the system while maintaining an economical throw-away level. The module configuration conforms to the standard Mariner B modules which makes it compatible with discrete components.

Texas Instruments has fabricated the integrated circuit sequence generator subsystem using the Series 53 SOLID CIRCUIT® semiconductor networks as logic building blocks. This approach has resulted in a subsystem of minimum size and weight. In addition, Texas Instruments has taken full advantage of past experience in the design, development and application of the SOLID CIRCUIT networks to supply a sequence generator with high reliability and minimum power consumption. Figures 1 and 2 show the complete subsystem.

This report is the Final Engineering Report required by the contract and has been written in accordance with JPL General Specification Number 20017.

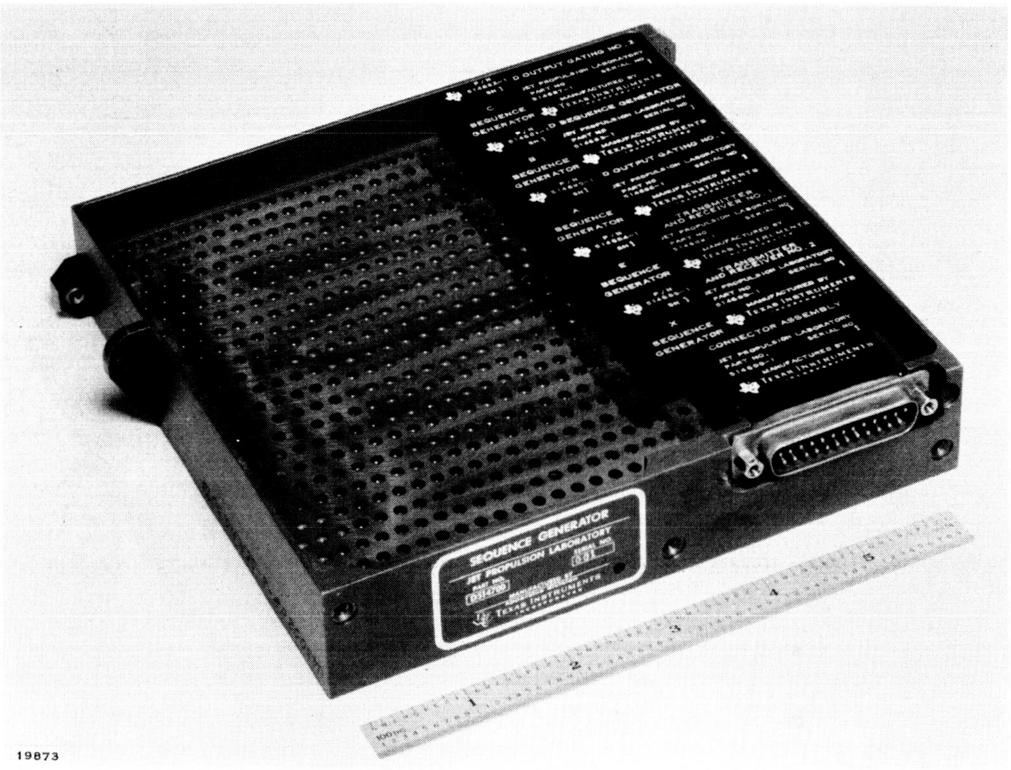

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Figure 1. Integrated Circuit Sequence Generator - Top View

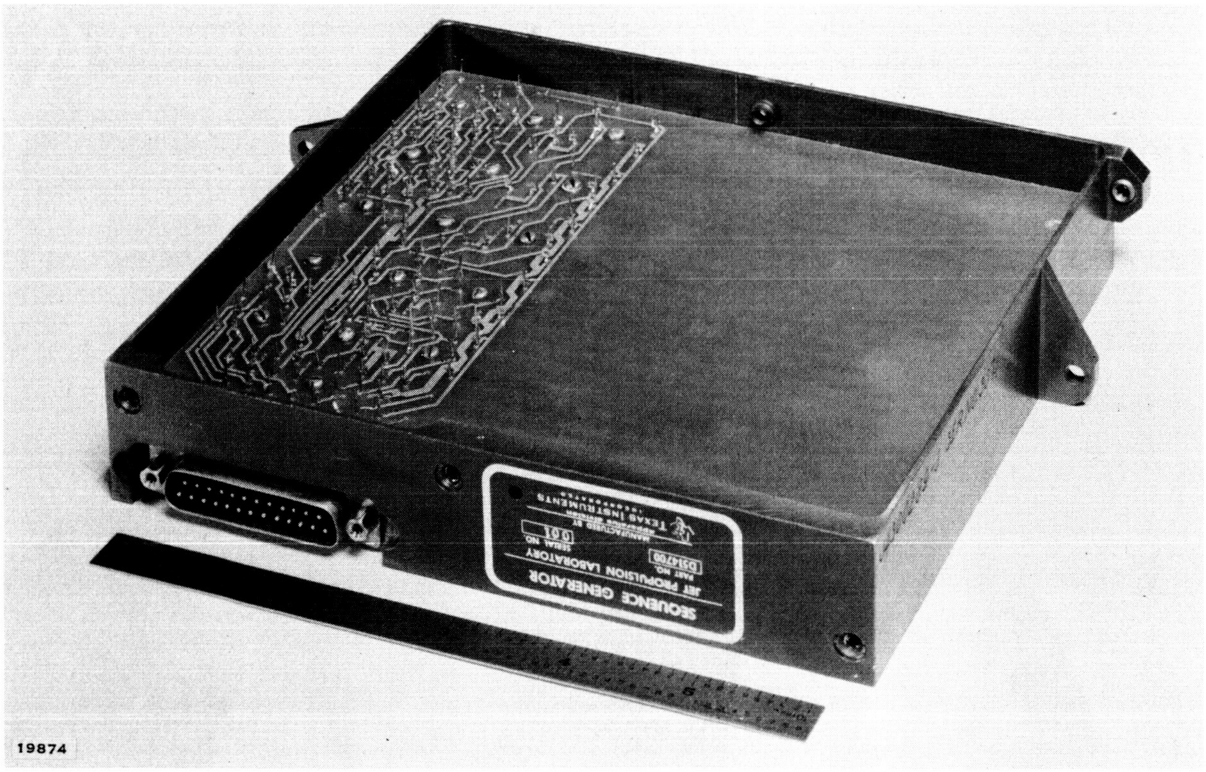

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Figure 2. Integrated Circuit Sequence Generator - Bottom View

SECTION II

PLANETARY RANGING SYSTEM DISCUSSION

A. General

Prior to the description of the Integrated Circuit Sequence Generator, the problem of long-distance ranging will be discussed. This will serve as a foundation for the abbreviated discussion of the subsystem details that follow.

B. Long-Distance Ranging Problem

The conventional method of determining distance to a target or object is one using radar apparatus in which a pulse of rf energy is transmitted, and the round-trip time T for the reflected pulse is measured, converted to range units, and displayed. The range is computed according to the equation

$$r = Tc/2$$

where c is the radio propagation velocity in the medium.

A problem arises, however, when the returned signal drops below the threshold of detectability; therefore, some means of increasing the energy of the transmitted (and received) pulse must be devised in order to increase the maximum range capability of the system. Several possibilities are:

1. Increasing the peak power of the transmitter
2. Increasing the pulsewidth
3. Increasing the prf and correlate over a number of pulses
4. Using a higher gain antenna
5. Installing a transponder on the vehicle being ranged.

Some of these approaches will alter the performance of the system. For example, the second alternative (longer pulsewidth) will reduce the range-resolution capability of the system in general (an exception will be discussed later). Increasing the pulse repetition rate (prf) and correlating would provide a considerable improvement in the detection of weak signals from relatively longer ranges; however, since range ambiguity is a function of c/prf, then a means of tracking (a priori information) must be used to establish the correct range category.

The chief alternative to the basic method discussed previously is one called a coded-pulse system, which takes advantage of certain desirable correlation properties of the transmitted signal. In fact, at certain extremely long distances in our planetary system, it appears that there may be no alternative to ranging other than a coded-pulse system of the type to be discussed. The coded-pulse radar or ranging system accomplishes a greater range by using alternative 2 in the following manner:* A longer pulse is transmitted which is made

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*A transponder is also used.

up of many shorter pulses coded (e.g., in binary fashion) in such a way that when the received pulse arrives at the receiver, the out-of-phase correlation with a locally generated (or stored) version of the code maintains a relatively stable, low mean value in comparison with the in-phase correlation which produces a maximum value. The peak is used to mark the arrival of the return pulse and may be resolved easily within a fraction of the time period of a single bit of the code. Thus, the usual compromise with range resolution in using a longer pulsewidth is avoided.

In the system developed at JPL, the coded-pulse ranging signal is transmitted continuously so that the range ambiguity of the system is a function of the time period of the code. In short, the code-repetition rate is similar to the pulse-repetition rate in a conventional radar in defining the range ambiguity of the system. To increase the maximum unambiguous range r_{max} capability of the system, the code period P must be increased as indicated in the following equation:

$$r_{max} = (1/2)Pct$$

where

P = the period of the code in symbols or bits

c = the propagation velocity

t = the symbol or bit period.

The range accuracy r_a of the system is a function primarily of the code symbol or bit period (i.e., bandwidth) input signal-to-noise ratio and the integration time constant in the correlation detector (for vernier resolution).* For greater range accuracy, the code or bit period must be reduced, and/or the effective signal-to-noise ratio must be increased.

As in all systems which offer solutions to major problems, other problems may arise; in the coded ranging system, the primary problem ordinarily is one of acquiring the received code. In particular, this is a problem when it must be done in real time and in a relatively short period of time. In theory, to mark one symbol out of P symbols requires only $\log_2 P$ information bits. For example, ten information bits define unambiguously any one of 1024 symbols, provided the ten information bits are without error. Since the received signal is degraded by noise, it would be unrealistic to expect that $\log_2 P$ bits would be received without error with a high probability; hence, some means of error correction of the received bits would be necessary to recover accurately $\log_2 P$ bits. Presently, no simple or relatively straightforward technique is known to do this with a reasonable amount of equipment. On the other hand (and at the other extreme), the received code could be acquired by exhaustive trial correlation of each bit or symbol position of the sequence. Each trial would consist of comparing the locally generated code with the received code from which the clock rate has been recovered for driving the local code generator. This comparison or correlation is performed for a period of time depending on the signal-to-noise ratio and desired confidence level, both of which specify the time interval of the correlator integrator; then the output of the integrator is sampled to determine whether the requisite threshold has been exceeded. If not exceeded, the

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*The signal-to-noise ratio is increased (effectively) by increasing the integrator time constant; thus, the two are related.

next trial consists of shifting the phase of the locally generated code by one bit (with reference to the received code) and repeating the process just described. A scanning operation is, thereby, performed until the correct phase is determined, at which time the output of the integrator will exceed the predetermined threshold and the received code will have been acquired. To maintain track or, in other words, to produce a continuous readout of the range, it is necessary to continue to step the local code generator at the same clock rate as that of the received code by using a clock phase-locked loop in the receiver. The range is directly proportional to the displacement, in bit periods, between the transmitter and receiver code by using a clock phase-locked loop in the receiver. The range is directly proportional to the displacement, in bit periods, between the transmitter and receiver code generators.

To show how impractical such an exhaustive trial process would be, consider the following example. The coded sequence is 1.435 billion bits long, which is adequate for unambiguous ranging up to approximately 133.4 million miles at a megabit transmitter rate; the time constant in the integrator is 1 second, and a sampling or scanning interval of 1 second is used (thus, the signal is correlated over an interval of 1 million bits). In the worst possible case (no a priori range information), it would take 45.5 years, or an average of 22.75 years, to acquire this sequence.

A means of avoiding this exhaustive trial process is mandatory. An excellent alternative devised by communications systems research scientists at JPL is summarized briefly in the following list.[1,2,3]

1. Select j sequences (code components) with the desired ideal or two-level autocorrelation function (maximal-length shift register generator sequences and Legendre sequences) of length p_i such that each p_i is relatively prime to all the others and such that the following inequality is satisfied:

   $$P_i P_2 \cdots P_j = \prod_{i=1}^{j} p_i \geqq P$$

   where P is the minimum code period required to achieve a specified maximum unambiguous range. Since each of the j sequences is relatively prime to every other, a composite sequence will have a period equal to the product of the individual periods of the j sequences (least-common multiple). In addition, it is best if each p_i is as close as possible to the jth root of P.[4]

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[1] S.W. Golomb, "Deep Space Range Measurement," Research Summary, No. 36-1 (JPL, 15 February 1960).

[2] M. Easterling, "Acquisition Ranging Codes and Noise," Research Summary, No. 36-2 (JPL, 15 April 1960).

[3] "A Long Range Precision Ranging System," Technical Report No. 32-80 (JPL, 10 July 1961)

[4] R.C.Titsworth, "Optimal Ranging Codes," Technical Report No. 32-411 (JPL, 15 April 1963).

2. By suitable combination of these sequences bit-by-bit (preferably majority logic), it is relatively simple for the receiver to acquire the phasing on each one independently by correlating it with the received composite sequence and determining the shift position which produced the highest correlation integral. Therefore, the entire combined sequence is acquired (with a nominal S/N) in no more than N trials where N is defined by

$$N = p_1 + p_2 + \cdots + p_j = \sum_{i=1}^{j} p_i$$

In the case of the coded sequence used in a planetary ranging system which contains 1.435 billion bits, N represents 304 trials (2+7+11+23+31+103+127), or about 5 minutes at most using a 1-second integration period per trial.

SECTION III

SYSTEM DESCRIPTION

A. General

The integrated circuit sequence generator is an integral part of the complete ranging system. The function of the subsystem, described by Figure 3, is to generate the long binary codes mentioned in the previous section. In the following paragraphs, the electrical and mechanical characteristics will be discussed briefly since the basic design and been accomplished by JPL. The drawing index, Appendix B, gives a complete listing of all the drawings generated during this program.

B. Electrical

The subsystem generates six pseudorandom codes with feedback shift registers as shown in Figure 4 and Table I. The period lengths and symbol sequences of the six codes are listed in Table II. These pseudorandom codes are combined as shown in Table IIIA and IIIB. The three modes of operation of the subsystem are dictated by the acquisition (Ac) and correlation (Co) variables which are also included in Table IIIA and IIIB.

1. SOLID CIRCUIT Semiconductor Networks

The Series 53 SOLID CIRCUIT semiconductor networks are similar to the more familiar Series 51. The Series 53 networks were designed specifically for operation at clock frequencies to 3 megacycles. This increase in speed was accompanied by a proportional increase in power. However, the sequence generator described by this report will require a maximum of 2.1 watts. All of the logic functions described in the design specification have been implemented using the Series 53 SOLID CIRCUIT in the NAND/NOR configuration. This configuration requires only one positive supply voltage, whereas the AND/OR configuration requires an additional negative supply voltage.

With the J-K Flip-Flop SN530, no inverter is required for steering since both the normal and the complimentary inputs are available. This results in a savings in power and circuitry. The other logic implementation is straightforward.

All six types of networks were used in the sequence generator. SN531 and SN533 NAND Gates were used for all feedback and combination logic. The SN535 was used for the clock driver and inverter. SN532 and SN534 AND Gates were used for word detector logic. In addition, the SN532 was used to increase the fan-in of SN531.

Reliability data on the SOLID CIRCUIT semiconductor networks is presented in Appendix C. This data is applicable to the Series 53 as well as the Series 51.

In July, the Series 53 application report will be published and will be forwarded to be included as Appendix D.

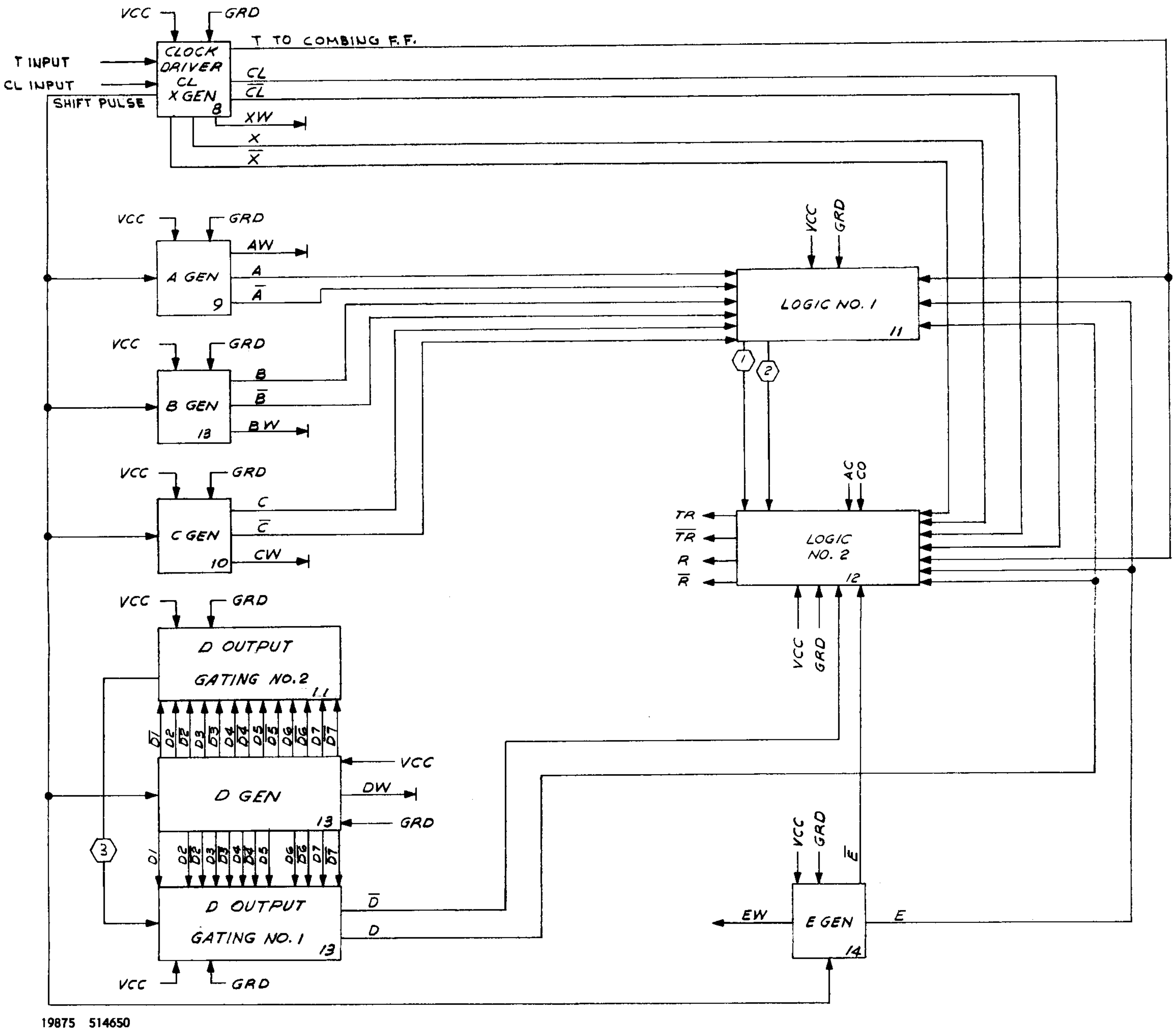


Figure 3. Block Diagram - Integrated Circuit Sequence Generator

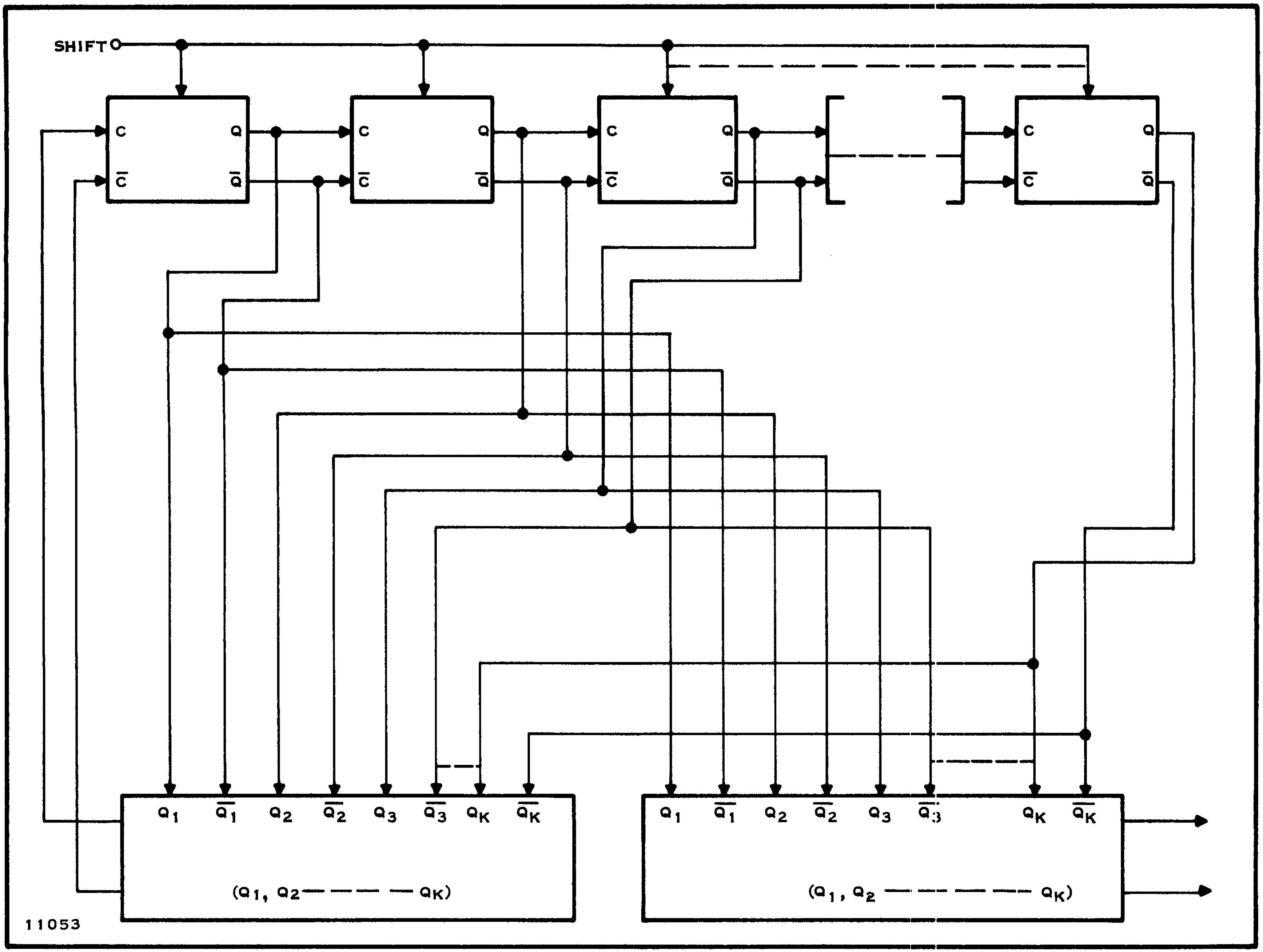


Figure 4. Code-Component Generator

Table I. Code-Component Generation

Code Component	k	Feedback f ( )	Output g ( )
X	3	$X_1\bar{X}_3 + \bar{X}_1X_3 + \bar{X}_1\bar{X}_2$	
A	5	$\bar{A}_1\bar{A}_4 + \bar{A}_2\bar{A}_5 + \bar{A}_3A_4A_5$	
B	7	$\overline{B_3B_5\bar{B}_6 + \bar{B}_3B_4\bar{B}_5 + B_1B_4B_6 + B_1B_5\bar{B}_7 + \bar{B}_5B_6B_7}$	
C	5	$C_2\bar{C}_5 + \bar{C}_2C_5 + \bar{C}_1\bar{C}_2\bar{C}_3\bar{C}_4$	
D	7	$D_6\bar{D}_7 + \bar{D}_6D_7 + \bar{D}_1\bar{D}_2\bar{D}_3\bar{D}_5\bar{D}_6$	$D_1\bar{D}_2\bar{D}_3\bar{D}_4D_5 + D_1D_2D_3\bar{D}_4\bar{D}_6 + D_1\bar{D}_2D_3\bar{D}_6\bar{D}_7 + D_1D_2D_3D_5D_7$ $+\bar{D}_1\bar{D}_2\bar{D}_3D_4 + \bar{D}_2\bar{D}_4D_6\bar{D}_7 + \bar{D}_1\bar{D}_2D_4\bar{D}_6D_7 + \bar{D}_1D_2D_3\bar{D}_4D_6$ $+D_2\bar{D}_3\bar{D}_4D_5D_7 + \bar{D}_1\bar{D}_2\bar{D}_4\bar{D}_5D_7 + \bar{D}_1\bar{D}_3D_4\bar{D}_7 + \bar{D}_2D_5D_6\bar{D}_7$ $+\bar{D}_1D_2D_4\bar{D}_5D_7 + \bar{D}_1\bar{D}_3D_5\bar{D}_6\bar{D}_7 + D_2\bar{D}_3D_4D_5\bar{D}_6\bar{D}_7$ $+D_3D_5D_6\bar{D}_7 + \bar{D}_1D_4\bar{D}_5\bar{D}_6 + \bar{D}_3\bar{D}_4\bar{D}_5D_6$
E	6	$E_1\bar{E}_7 + \bar{E}_1E_7$ $+\bar{E}_1\bar{E}_2\bar{E}_3\bar{E}_4\bar{E}_5\bar{E}_6$	

Table II. Code-Component Definition

Code Component	Length	Binary Sequence
C_1	2	01
X	7	1110100
A	11	11100010110
B	23	11111010110011001010000
C	31	1111100110100100001010111011000
D	103	011010011100011111110001011011101110101001000010011010011011 1101101010001000100101110000000111000110100
E	127	00000011111110101010011001110111010010110001101111101101011011001 001000111000010111110010101110011010001001111000101000011000001

Table III. Combinational Logic

Table IIIa. Receiver and Transmitter Code Combinations

Output	Code Combination
Receiver	$A \oplus B \oplus C \oplus D \oplus E \oplus X$
Transmitter	$X \cdot Cl + \bar{X}\,[G(A, B, C, D, E) \oplus Cl]$

Table IIIb. G (A, B, C, D, E) Vs. Control State

Mode	Control State	G (A, B, C, D, E)
1	$\overline{A_c}$	O
2	$A_c\,\overline{C_o}$	ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE
3	$A_c\,C_o$	$A \oplus B \oplus C \oplus D \oplus E$

2. Subsystem Description

a. Clock Shaper and Driver

The clock shaper and driver is composed of two inverter circuits tied in parallel and feeding into three additional inverters in parallel. The output of these three inverters is common to each of the code-component generators. The output of the two parallel inverters is used to clock the combining logic flip-flops. These clock inverters are physically located in the X Sequence Generator Module along with the CL Flip-Flop. The logic diagram for this module is shown in Figure 5.

b. Code-Component Generators

The maximal-length sequences X, C and E are generated with linear feedback. Legende sequences A and B are generated with non-linear feedback which derives the output from the shift register. The Legende sequence D is generated indirectly by short-cycling the linear feedback and deriving the output with combination logic. The logic diagrams of the code generators are shown in Figures 5, 6, 7, 8, 9, 10, 11 and 12.

Investigation has shown that this logic design requires the minimum total circuitry which insures maximum reliability. The number of shift registers in generators A and B may be reduced, but an increase in feedback logic is required; hence, no gain would be realized.

c. Code-Component Combiners

The code-component combiners, Figures 13 and 14, are designed to require a minimum number of Series 53 SOLID CIRCUIT building blocks. Tables IIIA and IIIB show the code combination generated in each of the three modes of operation.

d. Output Timing

To insure that the code outputs are in phase with the system timing, the final code combination is followed by flip-flops which are clocked by the input timing.

3. Subsystem Specifications

The sequence generator will meet or exceed the following specifications:

a. Timing Input

Waveform	Square 50% duty cycle
Frequency	1mc nominal
Amplitude	+3 volts
Reference	Ground
Source	<1K ohm

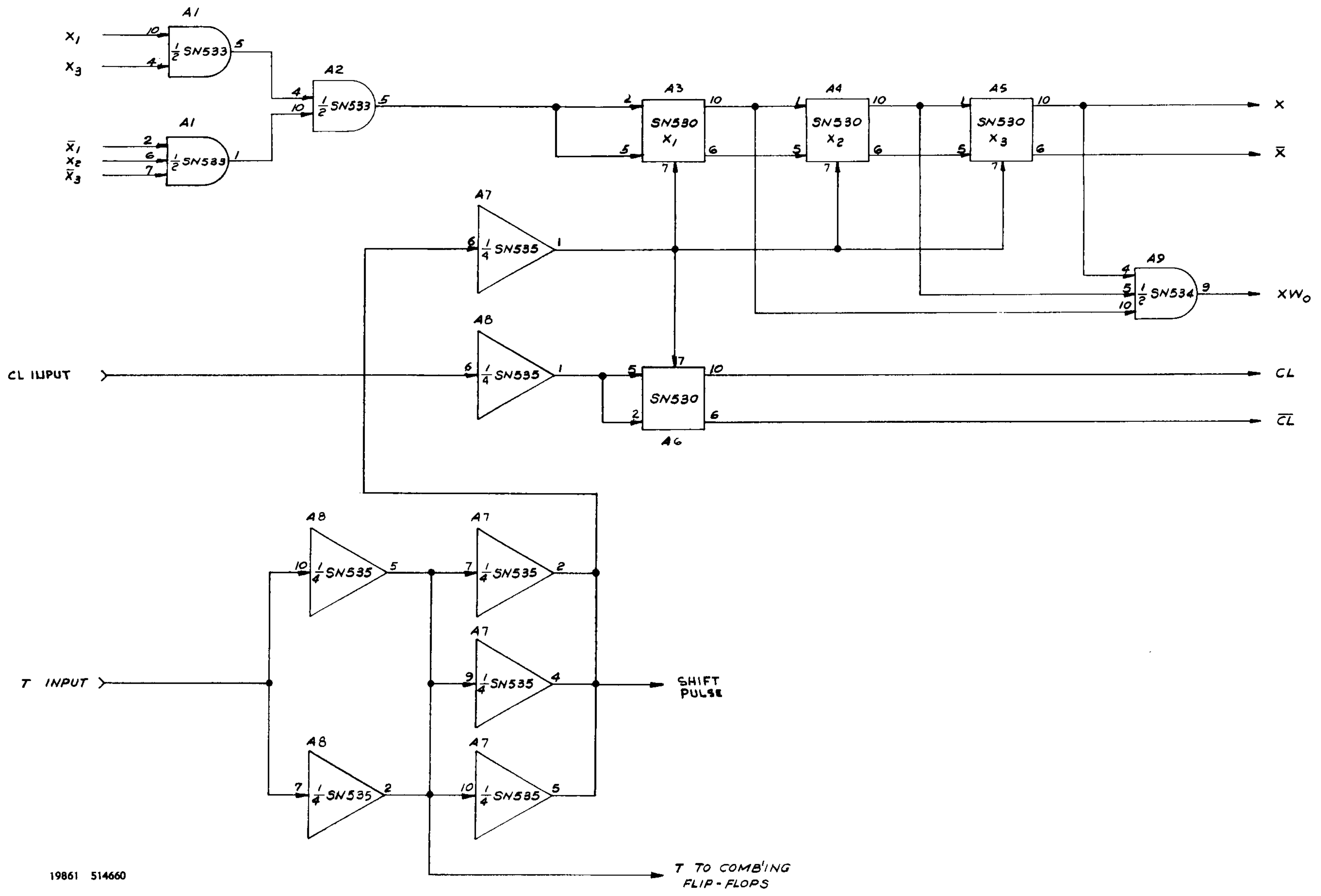
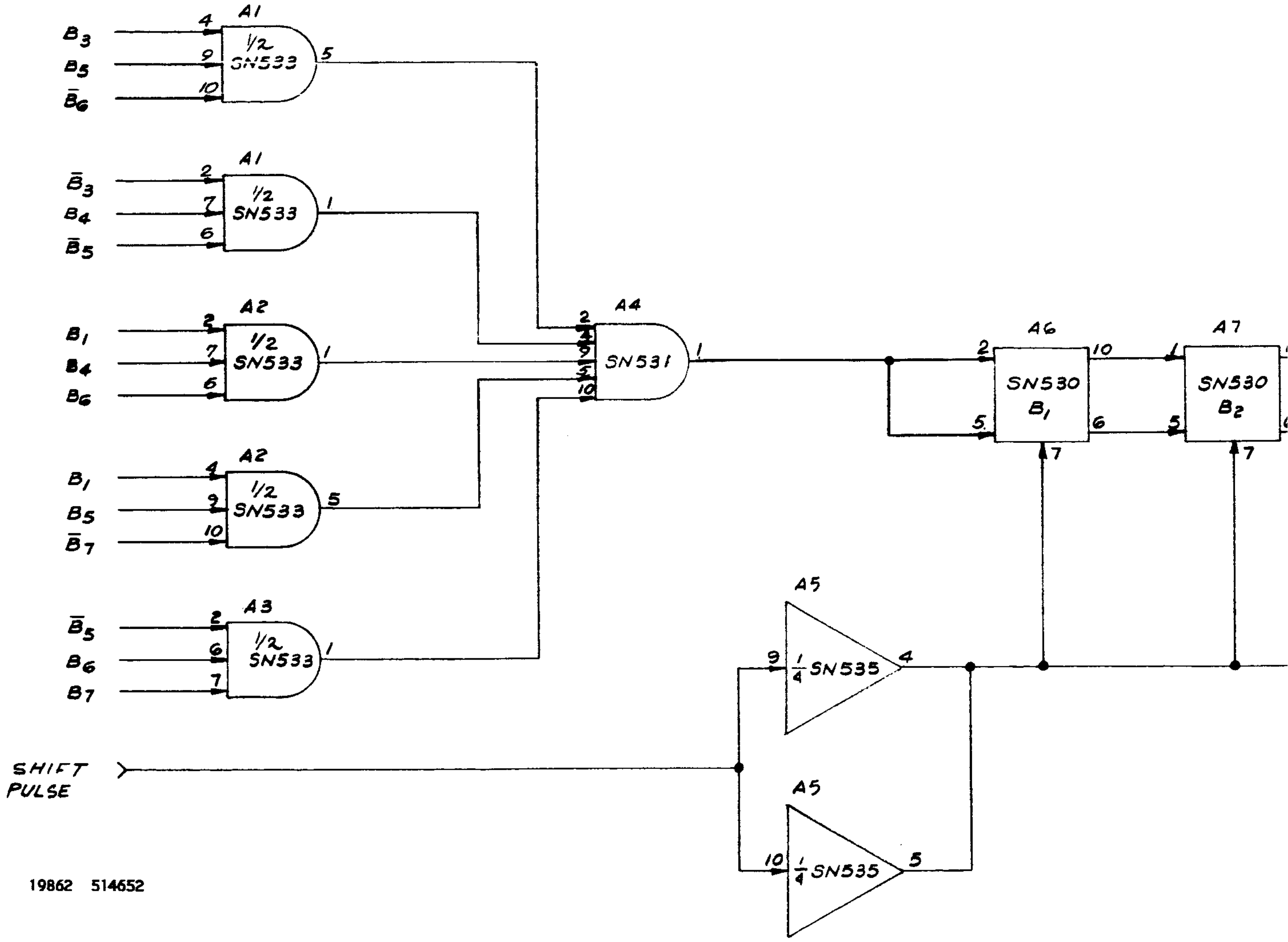


Figure 5. X Sequence Generator



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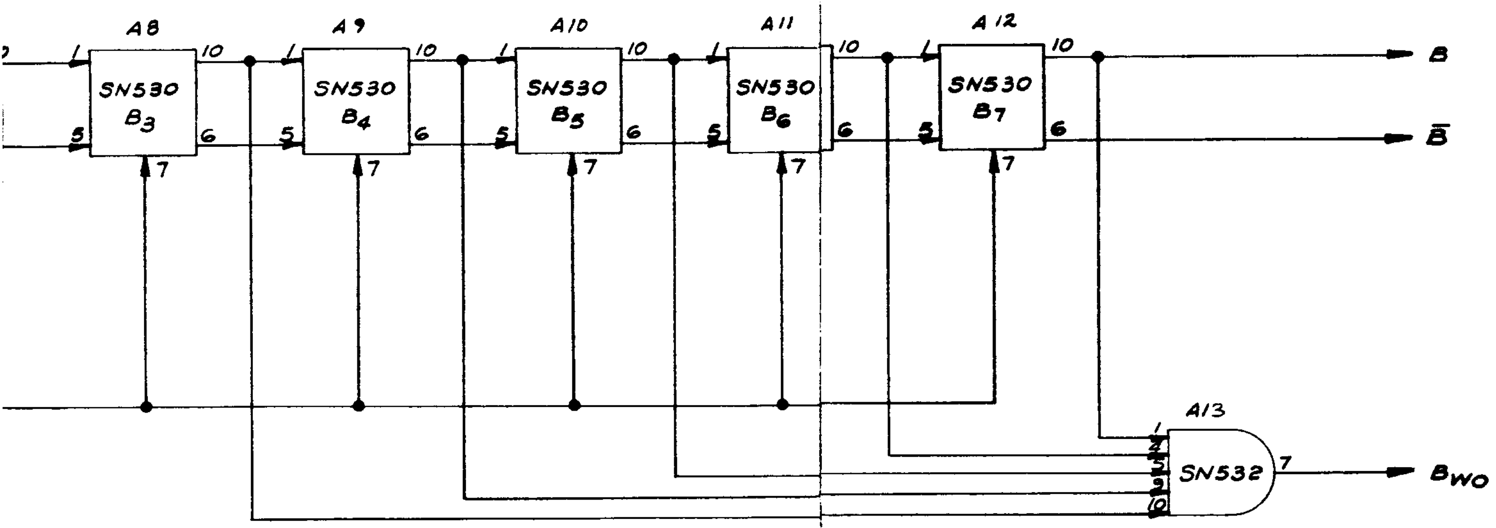


Figure 6. B Sequence Generator

3

2

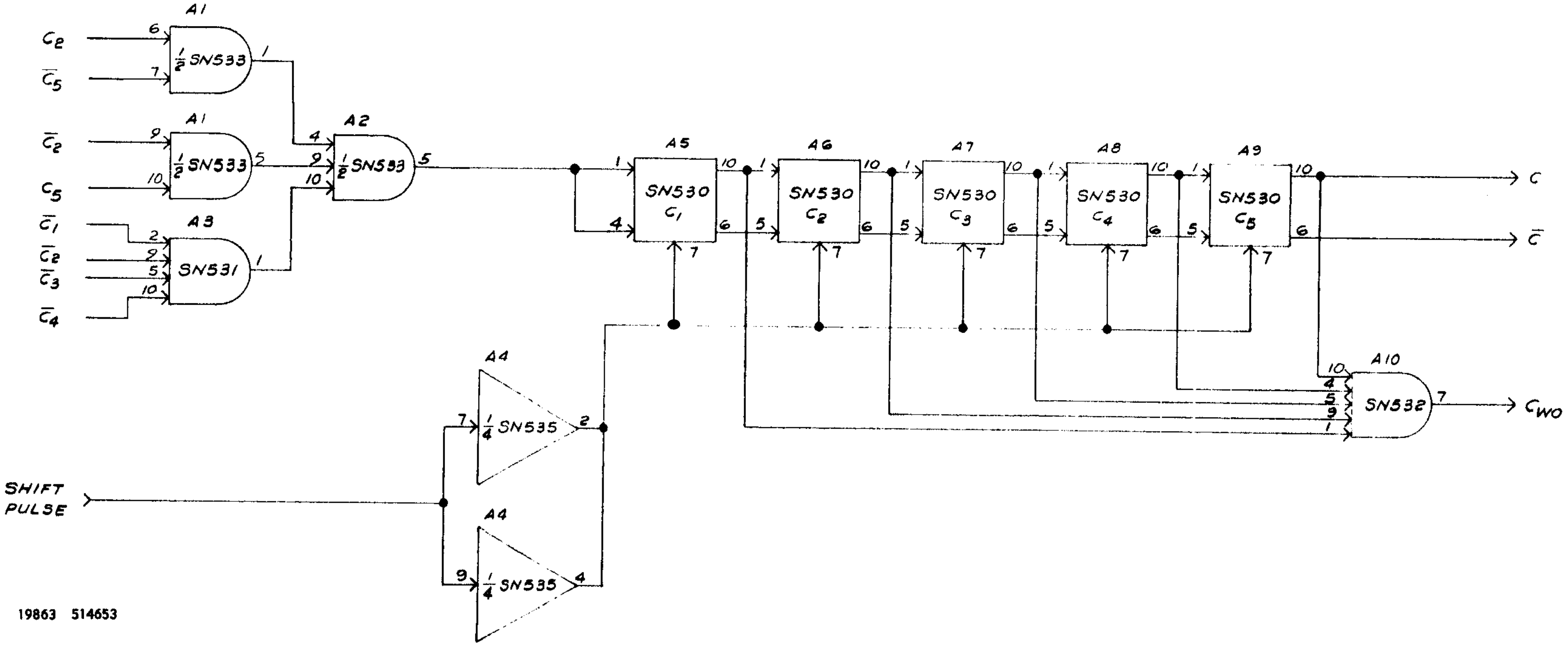
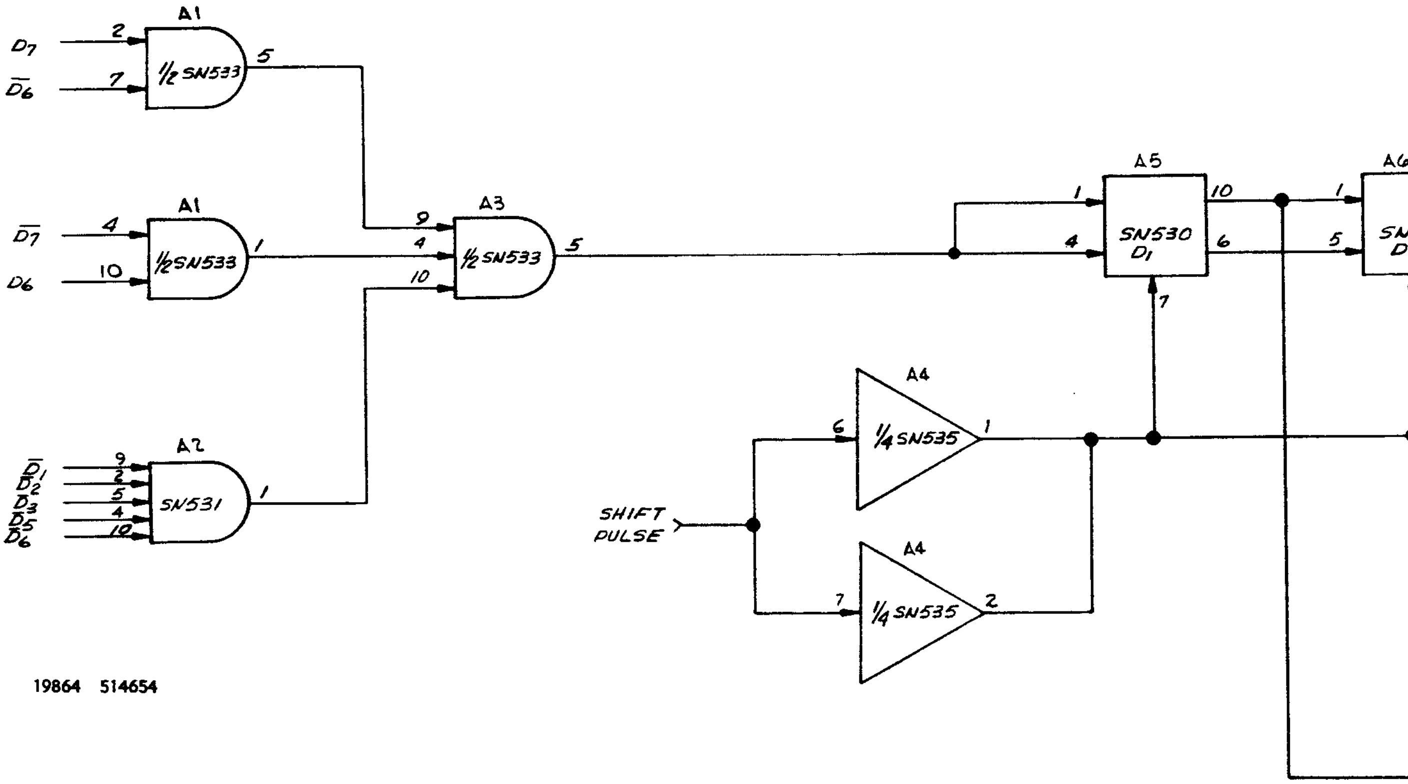


Figure 7. C Sequence Generator



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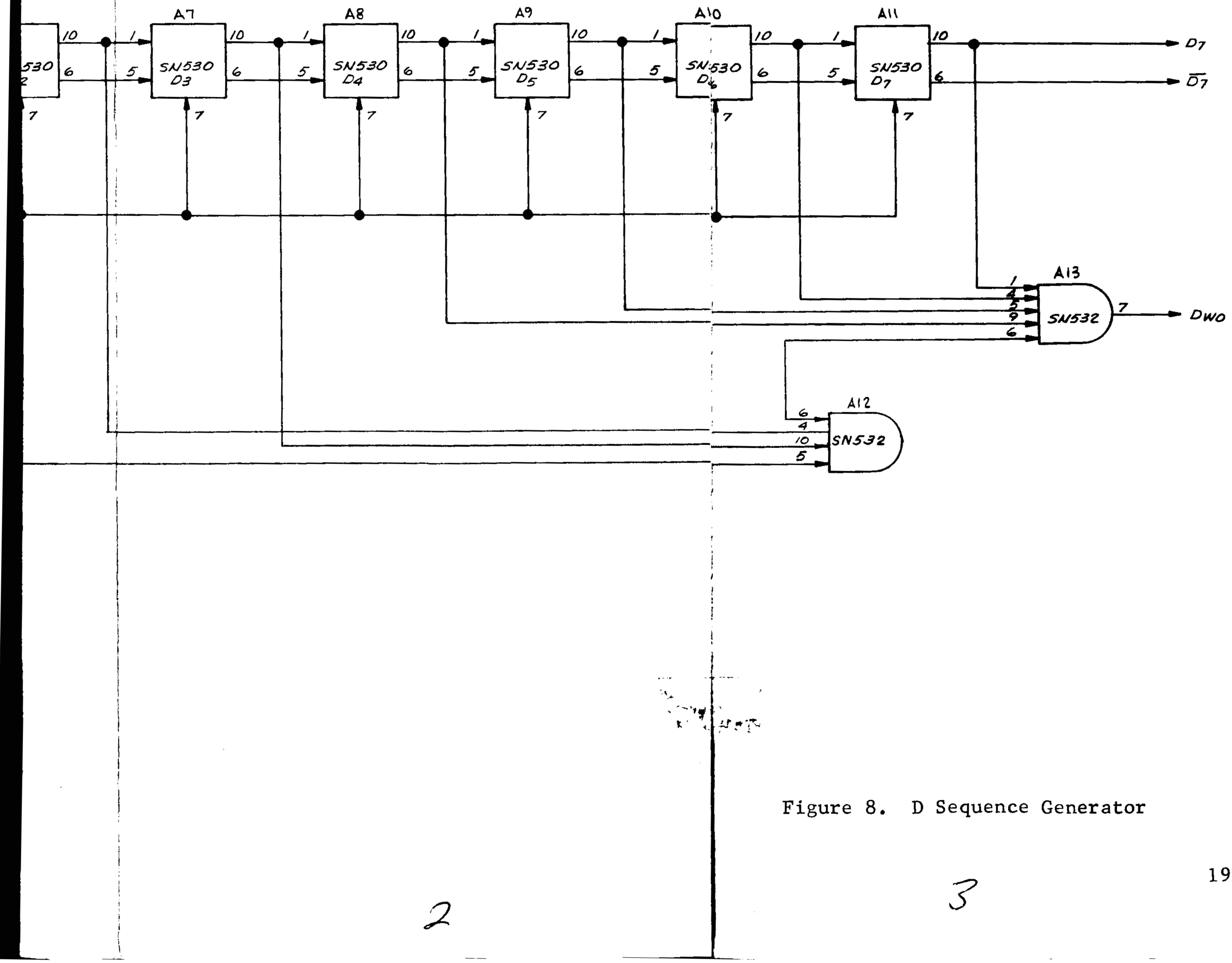


Figure 8. D Sequence Generator

2

3

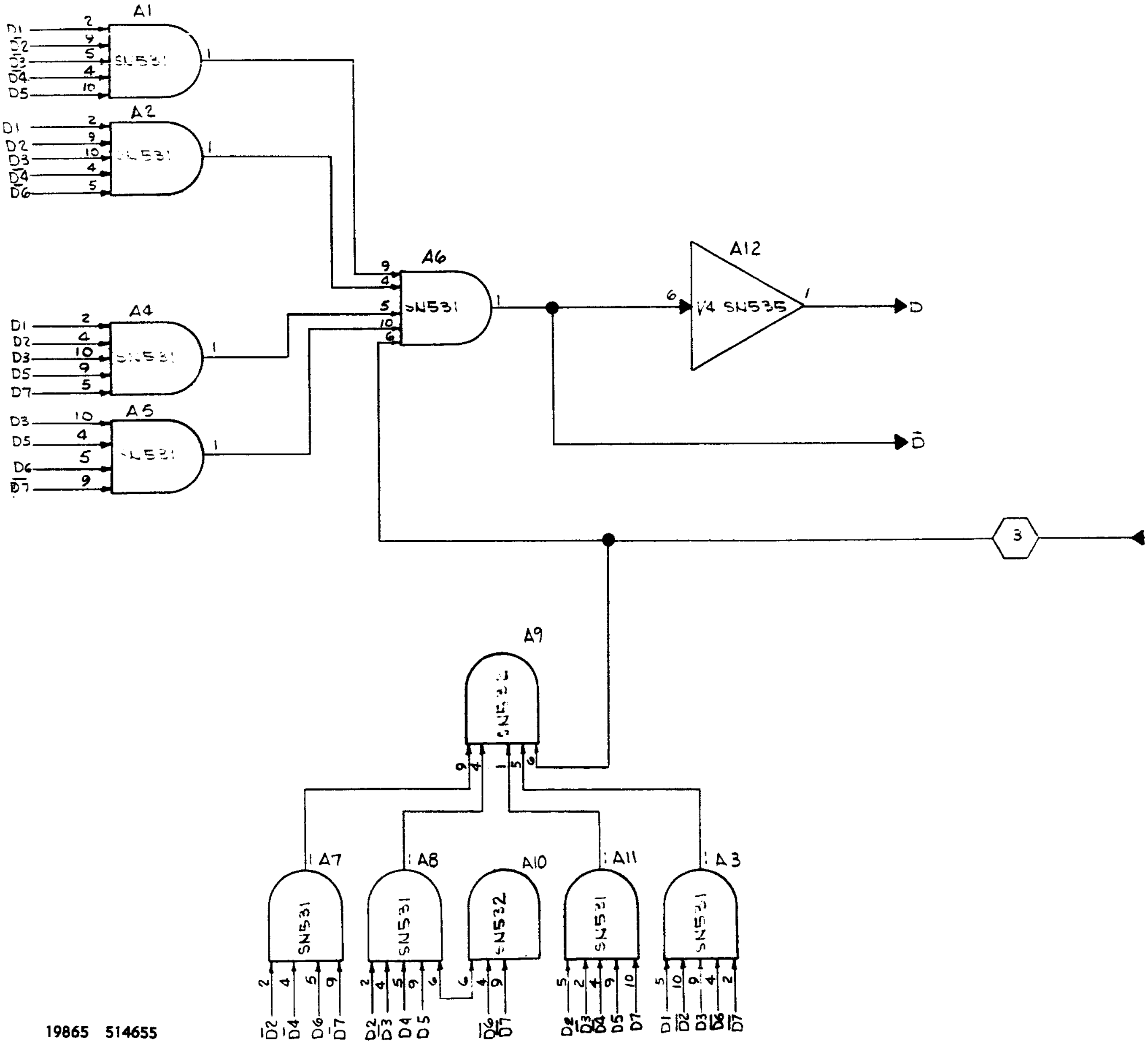


Figure 9. D Output Gating No. 1

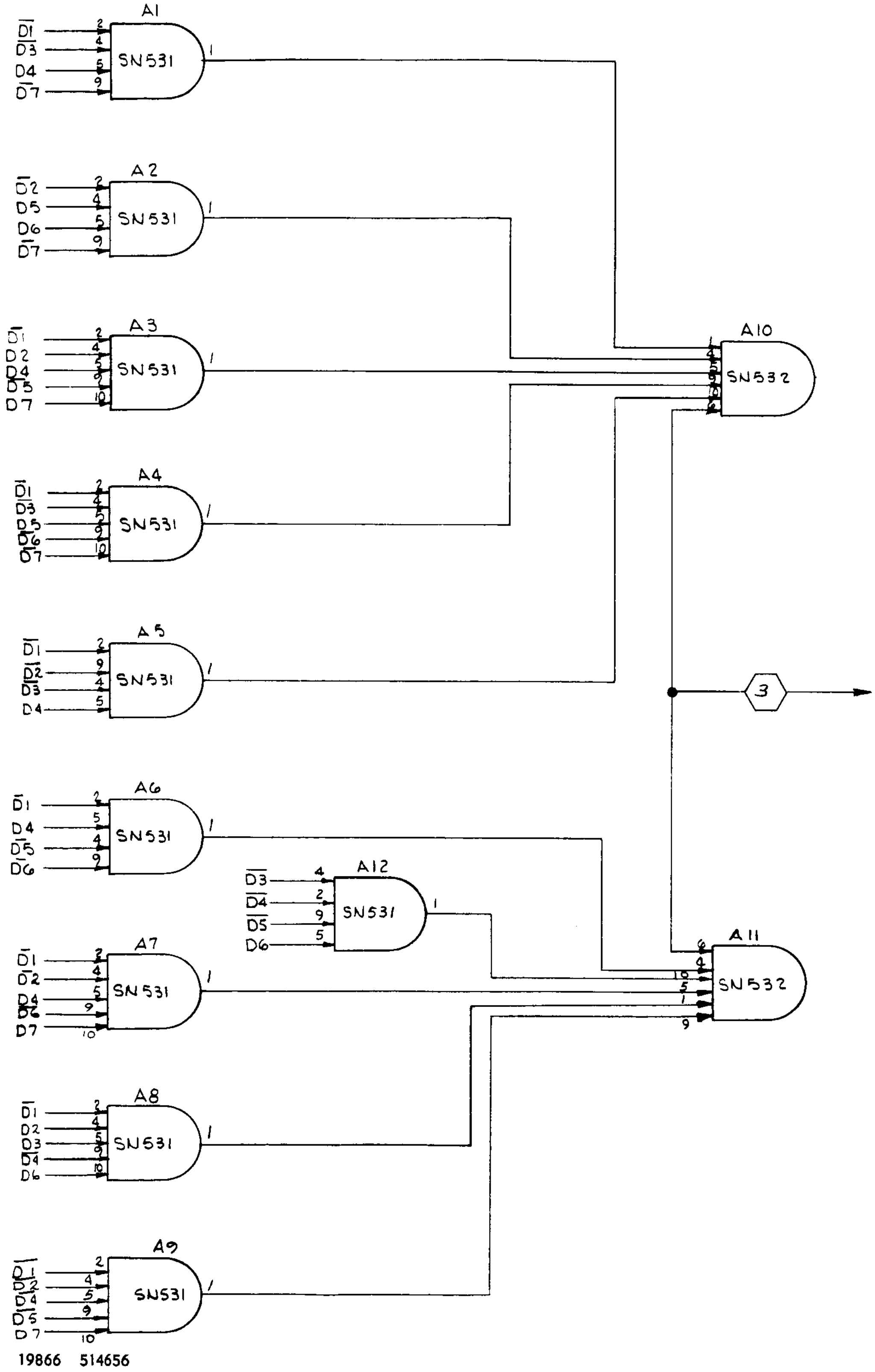


Figure 10. D Output Gating No. 2

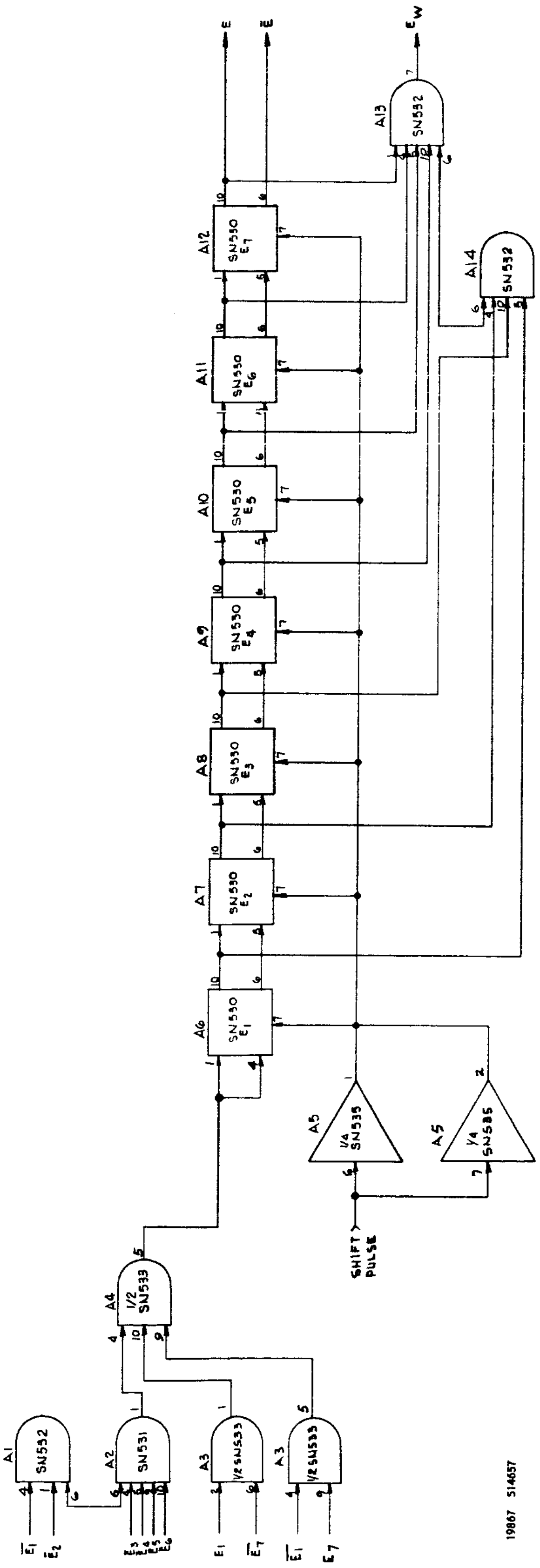


Figure 11. E Sequence Generator

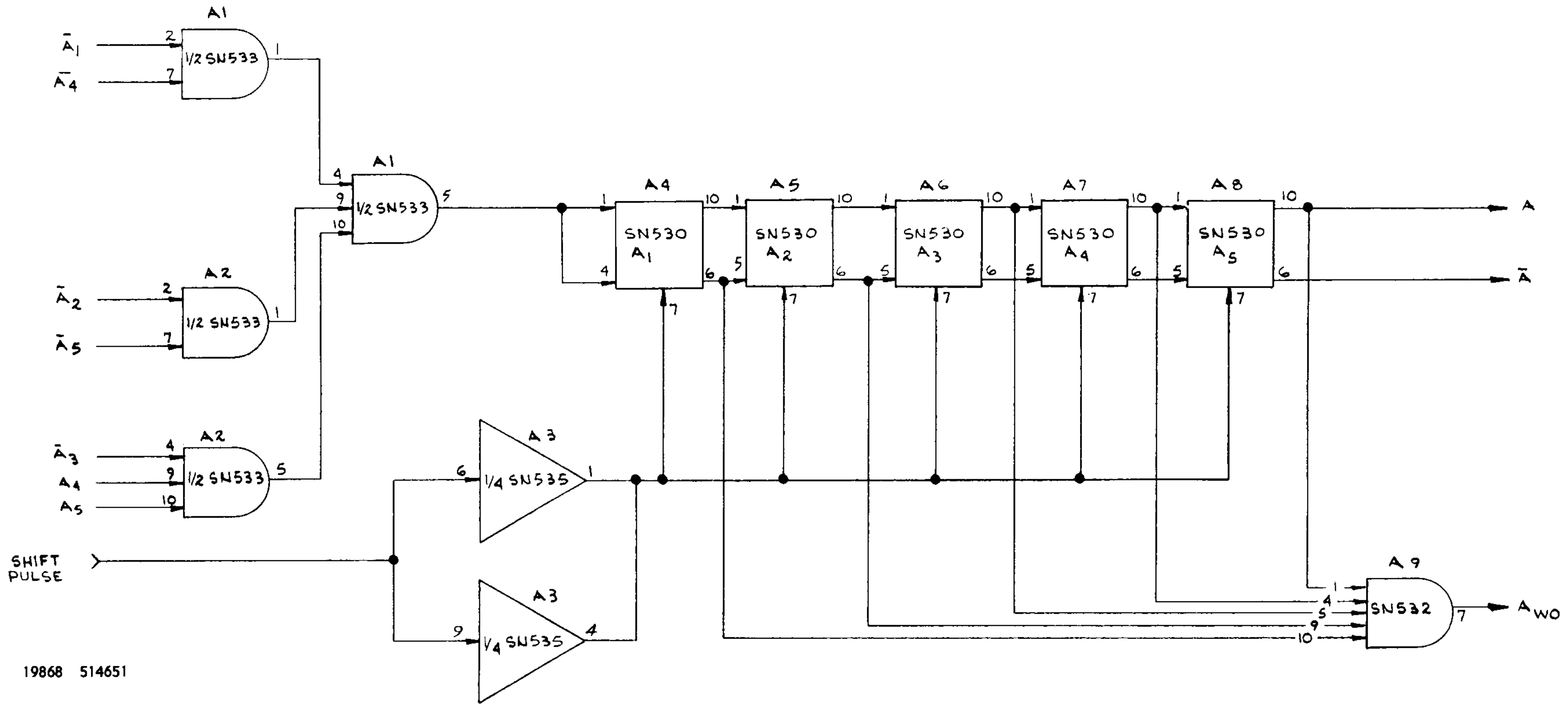


Figure 12. A Sequence Generator

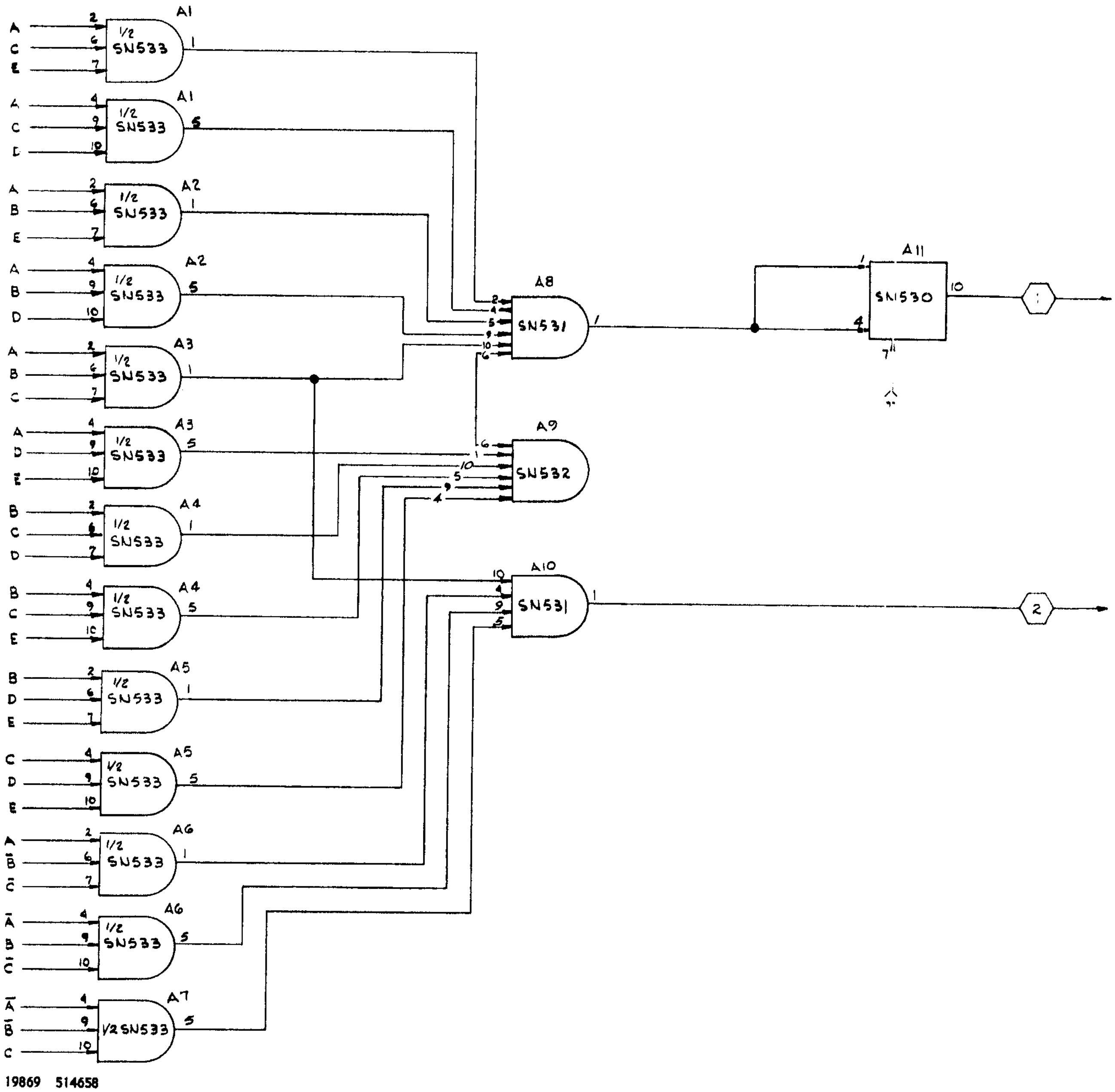
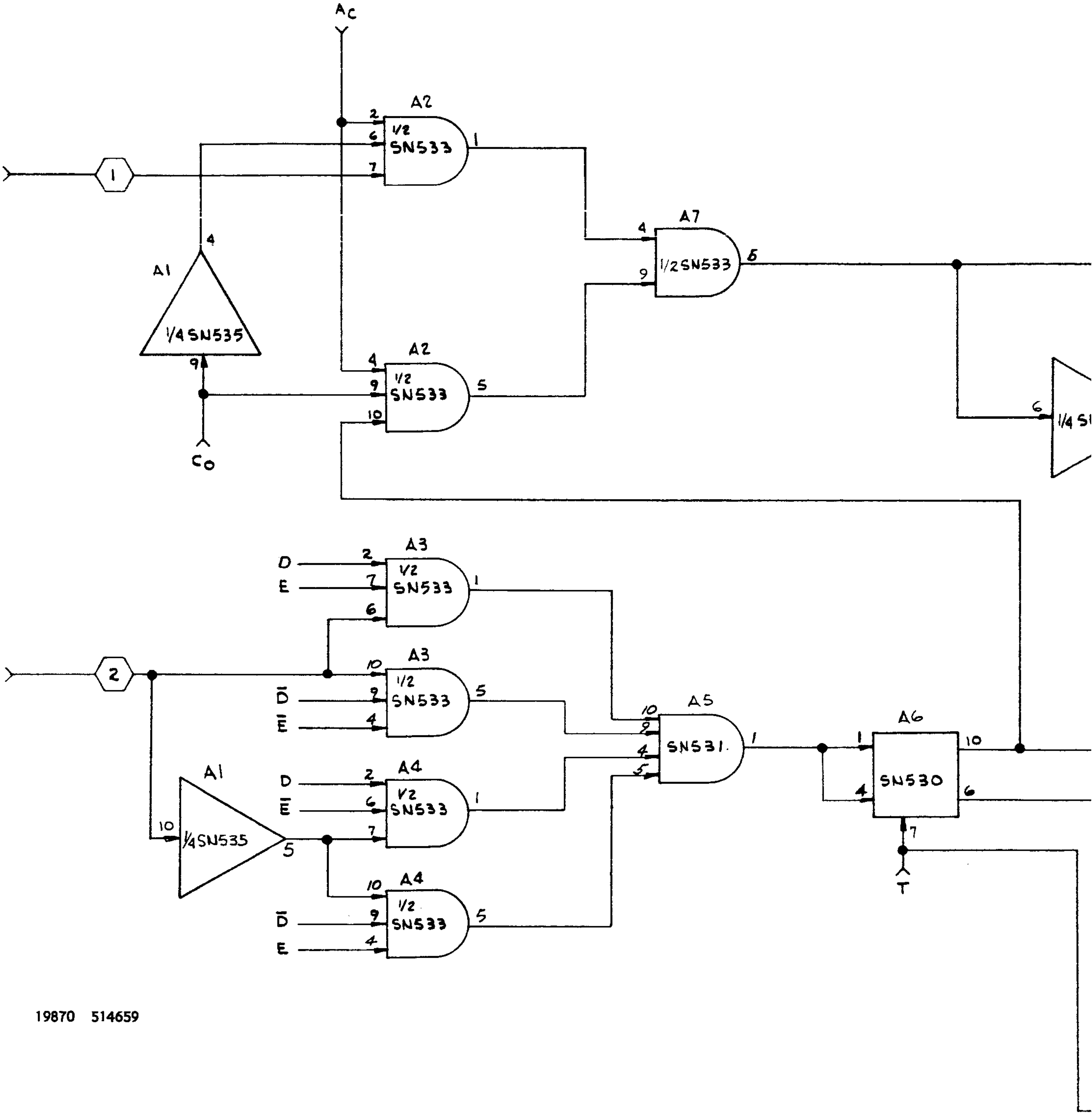


Figure 13. Transmitter and Receiver No. 1



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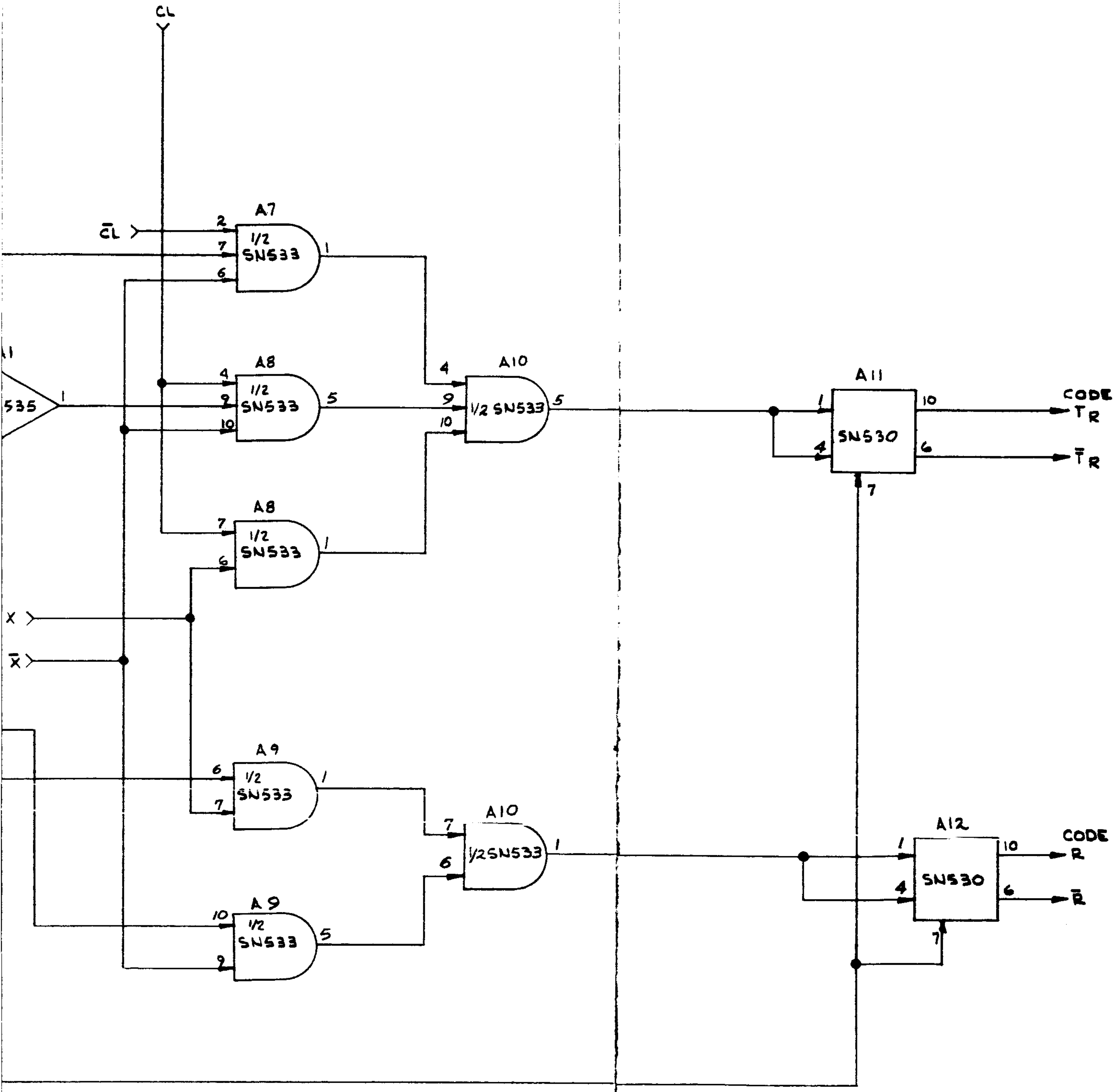


Figure 14. Transmitter and Receiver No.2

2

3

b. Clock Input

Waveform	Square 50% duty cycle
Frequency	500KC nominal
Amplitude	+3 Volts
Reference	Ground
Source	< 1K ohm
Phase	In phase with 1mc squarewave

c. Acquisition and Correlation Inputs

Waveform	Either of two dc voltage levels
Logic Levels	+3 Volts = true (1) 0 Volts = false (0)

d. Transmitter and Receiver Code Outputs

Waveform	NRZ binary voltage waveform switch nominal 1 usec bit period. Signal and complement is provided.
Logic Levels	3 Volts = 1 0 Volts = 0
Transition Timing	In phase with system timing.

e. Test Outputs	Test points are provided for each code component, its associated word detector, and the internal timing pulse.
f. Power	Voltage 3.2 volts ± 5% Current 650 ma Power 2.1 watts
g. Packaging	The entire sequence generator is mounted on one standard JPL subchassis referenced in JPL Specification Number 31224. Almost two-thirds of the chassis is not used.

C. Mechanical

1. General

The component parts of the sequence generator, the modules, are broken into functional parts of the total system. The system is broken into five 1X modules, five 2X modules, and one connector module. The breakdown of these modules is shown in Figure 3. The interconnections from module to module is made by a double sided nickle printed circuit board with all welded construction. All interconnections in the complete system are made by either tweezer, parallel-gap, or butt welding technique.

2. 1X Modules

The five 1X modules contain the A, B, C, E and X code component generators. The X code component generator module also contains the clock flip-flop and the clock driver circuits.

These 1X modules each contain one TI stack of networks. The number of networks per stack varies from nine to fourteen. The modules are standard in size, i.e., .918 x .750 x .575.

The TI stacks are mounted on an epoxy coated fiber glass header board for adapting the stack leads to the final module lead configuration. The package is shown in Figures 15 and 16 which readily show the amount of space and weight wasted in conforming to the standard subchassis.

After assembly and test, the modules are dip coated with RTV 11 silicon rubber. This coating was used to provide a thin cushion for the networks. Final encapsulation of the modules was made using Stycast 2850 FT.

3. 2X Modules

In order to provide sufficient lead holes in the standard JPL subchassis for all inputs and outputs and maintain an economical throw-away level, the other functions, i.e., D code-component generator and the code-component combiners, were made into 2X modules which were .918 x 1.518 x .575. Each of these modules contain two standard TI stacks side by side with interconnections between the stacks made across the top of the stack as well as under the header board. The D code-component generator is contained in three of the 2X modules labeled D Sequence Generator, D Output Gating No. 1 and D Output Gating No. 2. This splitting of the function was necessary to maintain an economical throw-away level of fifteen networks or less. However, the complexity of the interconnection board was increased considerably. The remaining two 2X modules contain the code-component combining logic. These modules are labeled Transmitter and Receiver No. 1 and Transmitter and Receiver No. 2.

As in the 1X modules, these modules were dip coated with silicon rubber prior to encapsulation in Stycast 2850 FT.

4. Connector Assembly

The connector assembly is an all welded connection. The connector, Cannon Type DBM-25P-NMB-B1, has terminals which provide for butt welding of the .020 nickle wire. This subassembly was potted in Silastic 881 prior to encapsulation in Stycast 1090 to allow the pins to float. The Stycast 1090 was used to reduce the overall weight of the system since no power was dissipated in this connector.

5. Subsystem Assembly

The assembly of the subsystem was unique as for as interconnections of the modules. The modules were held mechanically in the subchassis in the normal manner by bonding them to the subchassis, then inserting a stainless steel No. 2-56 screw into the insert encapsulated in the module.

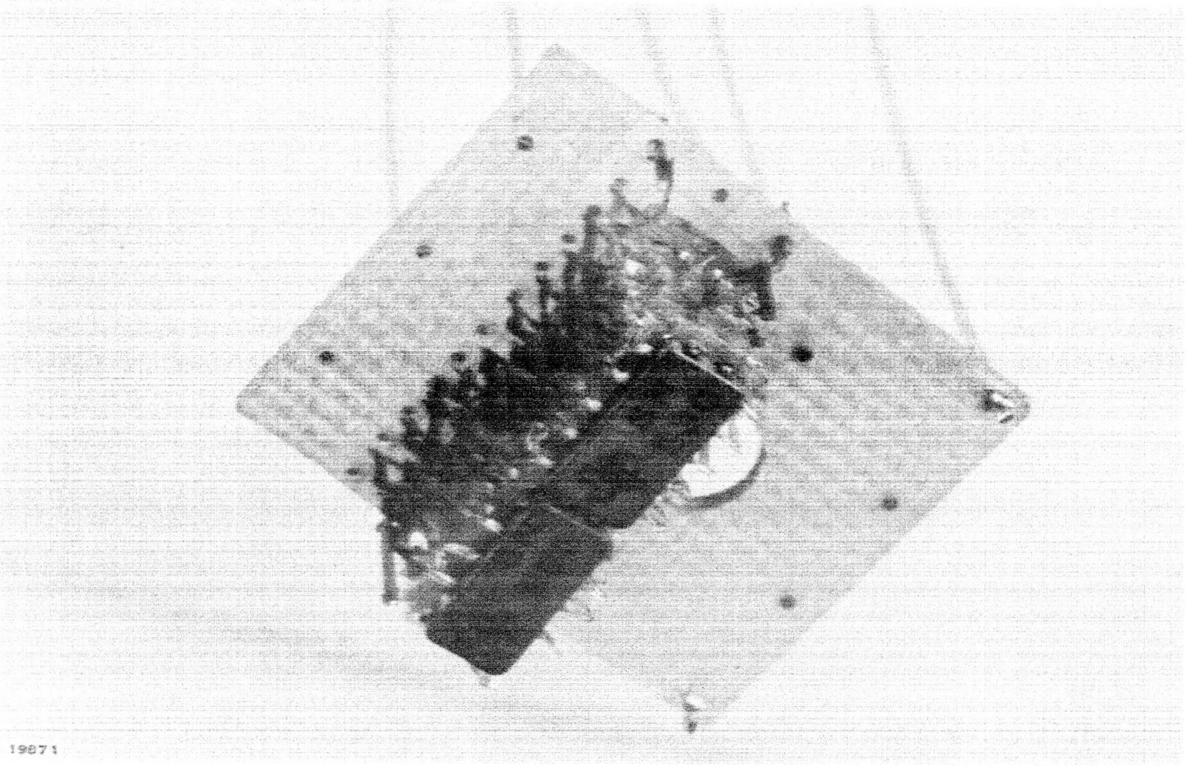


Figure 15. 1X Module - Top View

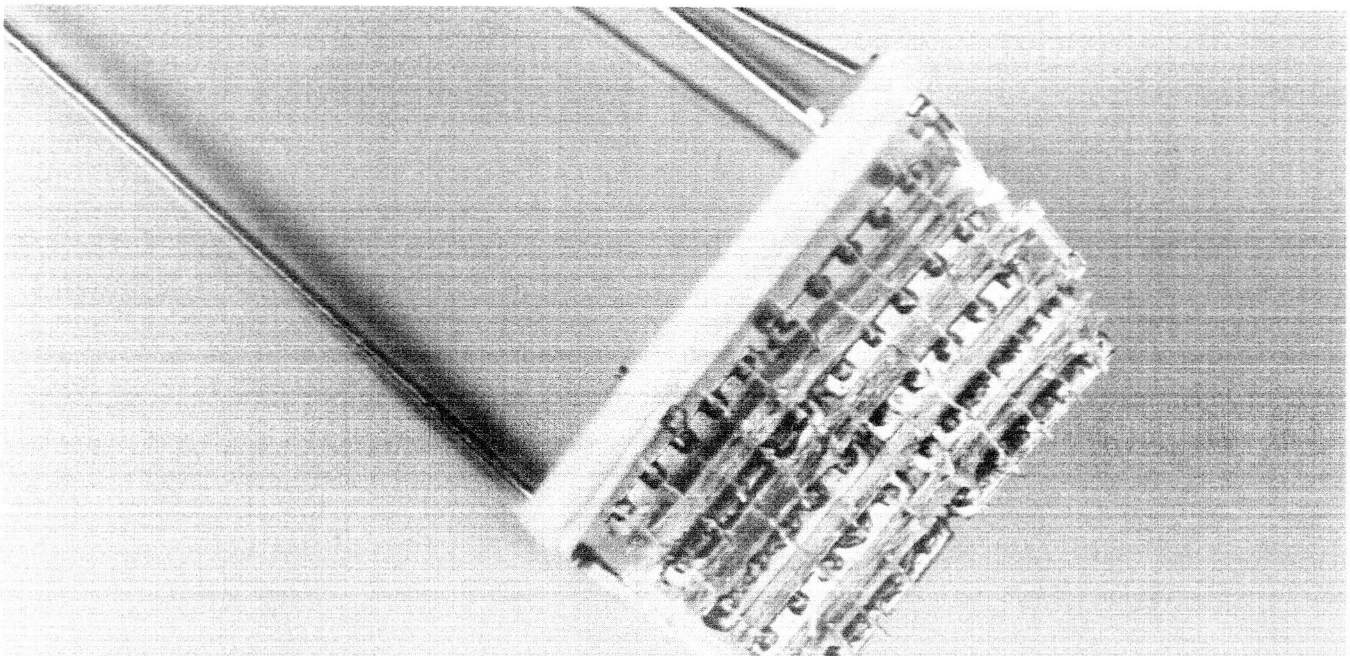


Figure 16. 1X Module - Side View

The interconnecting board was a double-sided nickle board. The etch on the two sides of the board was connected by using kovar ribbon feed-throughs that are parallel-gap welded to the etch. The backing or insulation sheet was then bonded to the printed circuit board. Finally the riser connections are parallel-gap welded to the printed circuit board approximately .020 to .050 inches from the module lead holes. Thus, when the modules are installed in the subchassis, the risers are beside and perpendicular to the module leads for easy tweezer welding. There are many ways to remove and replace a module. The best is to cut the riser ahead of the weld to the module lead and splice in a small piece of ribbon when the new module is installed.

The riser connections mentioned above are in a configuration as shown:  The shank portion of the riser is parallel-gap welded to the printed circuit board. The riser is then bent 90° to align the upper portion with the module leads that are protruding through the board. This procedure allows for an all welded construction while maintaining the simplicity of a conventional printed circuit board. The technique is illustrated in Figure 2 quite clearly.

After final assembly, the printed circuit board and connections are conformal coated with Solithane 113. This process provides mechanical support for the interconnections as well as insulation.

The functions that are accessible on the bottom of the subsystem can be located by the use of Figure 17 and Table IV. Figure 17 shows the location of each module lead. Table IV gives the functions associated with each module lead and also gives the connector pin numbers associated with each function.

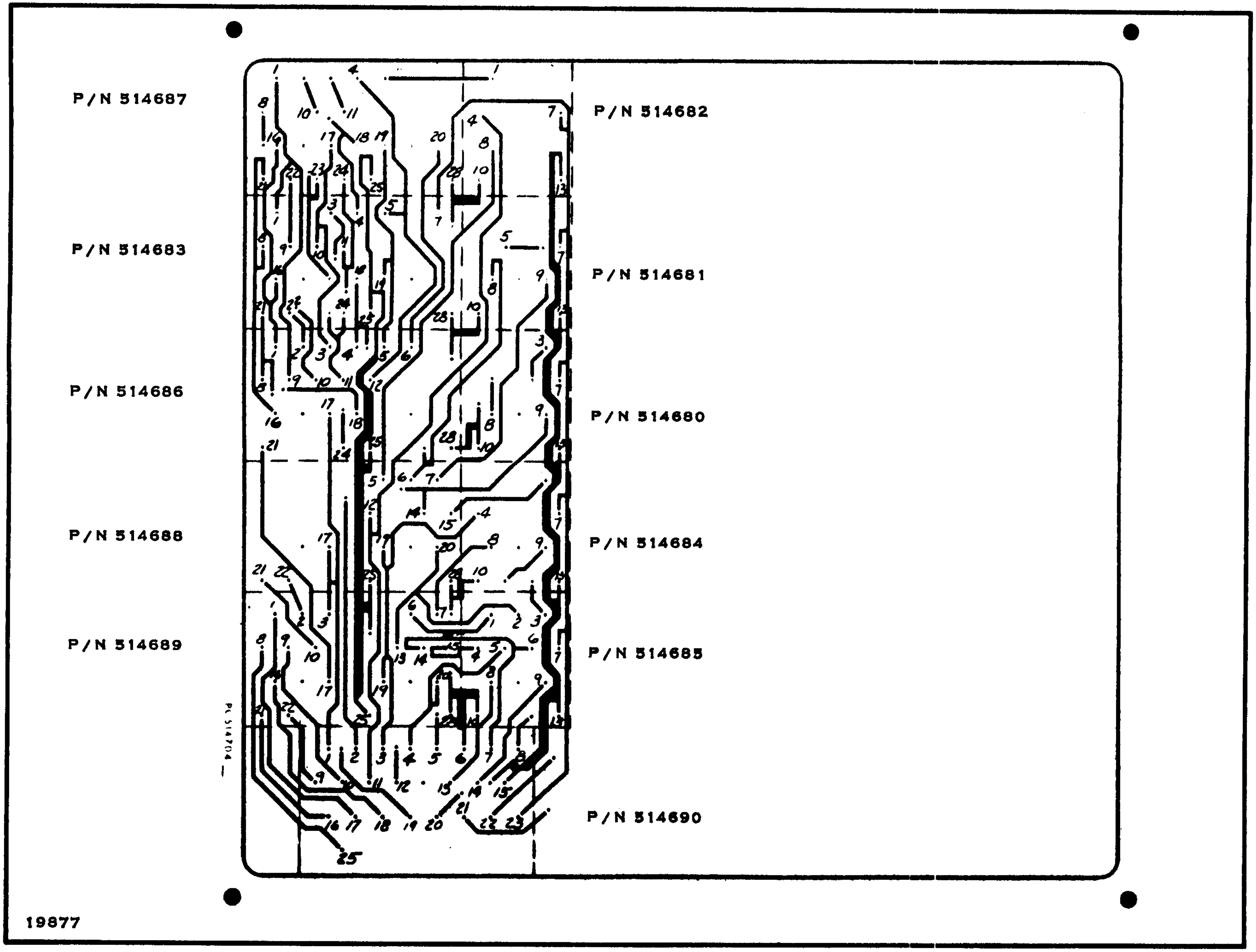


Figure 17. Module Lead Designation

Table IV. M

Module Lead No.	P/N 514680 A Seq. Gen.	P/N 514681 B Seq. Gen.	P/N 514682 C Seq. Gen.	P/N 514683 D Seq. Gen.	P/N 514684 E Seq. Gen.	P/N X S
1			C Word	$\overline{D_6}$		$\overline{\text{CLO}}$
2						Tim
3	$\overline{\text{A}}$ Code			D Word		CLO
4			C Code	$\overline{D_5}$	E Code	$\overline{\text{X}}$ C
5		B Word		D_7		X C
6						CLO
7	Shift Pulse	Shift Pulse	Shift Pulse	Shift Pulse	Shift Pulse	Shi
8	A Word	B Code	$\overline{\text{C}}$ Code	D_2	$\overline{\text{E}}$ Code	X W
9	A Code	$\overline{\text{B}}$ Code		$\overline{D_1}$	E Word	Tim
10	GROUND	GROUND	GROUND	D_4	GROUND	GRO
11				D_5		
12						
13	V_{CC}	V_{CC}	V_{CC}		V_{CC}	V_{CC}
14						
15						
16				D_3		
17				$\overline{D_3}$		
18				D_6		
19				$\overline{D_7}$		
20						
21				$\overline{D_2}$		
22				$\overline{D_1}$		
23						
24				$\overline{D_4}$		
25				V_{CC}		
26						
27						
28				GROUND		

odule Lead Designation

514685 eq. Gen.	P/N 514686 D Output Gating No.1	P/N 514687 D Output Gating No.2	P/N 514688 Trans. & Recvr. No. 1	P/N 514689 Trans. & Recvr. No. 2	P/N 514690 Connector Assembly Function	Connector Pin Number
$\overline{CK}$	D_3	$\overline{D_6}$		Acquire	D Code	12
ing	D_1			1	C Word	10
CK IN	D_4			D Code	E Code	8
ode	D_6	D_7			X Code	6
ode	$\overline{D_7}$		$\overline{C}$ Code		B Code	5
CK	3		B Code	$\overline{CLOCK}$	GROUND	3
ft Pulse			$\overline{B}$ Code	$\overline{E}$ Code	CLOCK	2
ord	$\overline{D_2}$	$\overline{D_2}$		T_R Code	CLOCK IN	1
e In	$\overline{D_6}$			Correlation	R Code	13
UND	$\overline{D_3}$	$\overline{D_4}$		2	Correlation	11
	$\overline{D_4}$	D_6			C Code	9
	D_7		C Code		A Code	7
				Timing	X Word	4
			A Code	CLOCK	Time In	17
			$\overline{A}$ Code	$\overline{X}$ Code	V_{CC}	15
	D_2	D_3		$\overline{TR}$ Code	$\overline{R}$ Code	24
	D	D_4	D Code	$\overline{D}$ Code	Acquire	22
		$\overline{D_5}$			$\overline{TR}$ Code	21
		$\overline{D_7}$	E Code	E Code	D Word	20
		3	Timing	X Code	A Word	19
	$\overline{D}$	D_2	2	$\overline{R}$ Code	B Word	18
		$\overline{D_1}$	1	R Code	E Word	16
		$\overline{D_3}$			Shift Pulse	14
	D_5	D_5				
	V_{CC}	V_{CC}	V_{CC}	V_{CC}	TR Code	23
	GROUND	GROUND	GROUND	GROUND		

2

3

SECTION IV

PROGRAM HISTORY

During the early portion of the program, implementation of the logic expressions was investigated. Since the Series 53 SOLID CIRCUIT gives the designer the option of using either NAND/NOR or AND/OR, investigation of the two approaches was warranted. The results of this investigation revealed an advantage in power and network if the AND/OR approach were used. However, providing two supply voltages offsets this advantage and the NAND/NOR approach was used.

The sequence generator in its entirety was breadboarded during November and December. However, difficulty in acquiring the SN531, 5 Input NAND Gate, delayed evaluation of the breadboard in any great detail.

During this time, the problem of power dissipation was investigated. The results of the investigation implied that use of the Stycast 2850 FT was warranted instead of the Stycast 1090. However, the assumption that all the heat would be conducted only through the potting compound was extremely conservative since each of the modules have at least six leads which are excellent heat conductors. Also, a laboratory test of a module disputed the calculations. This test, however, was not conducted in a vacuum and was, therefore, not conclusive either. Quite possibly, Stycast 1090 would be sufficient since the leads were not taken into account and since with V_{CC} of +3 volts the total maximum power per module is only 300 milliwatts. For a ΔT of $30^{\circ}C$, the maximum power that could be dissipated using only the Stycast 1090 potting compound was 154 milliwatts. Taking the leads into account, this would rise to at least 300 milliwatts. Therefore, by taking the leads into account and by using the minimum V_{CC} supply voltage, the use of Stycast 1090 or some other light potting compound could be used with little difficulty. However, since this was a development contract and was the first time the Series 53 SOLID CIRCUITS were used, encapsulating the modules in the Stycast 2850 FT was warranted.

Development of a completely weldable printed circuit board and interconnection arrangement was accomplished during the next phase of the program. The use of parallel-gap welding of kovar risers to the nickle etch and of the kovar feed-throughs to connect both sides of the board has proved quite satisfactory. These connections have been vibrated according to or in excess of the high frequency vibration requirements called out in JPL Specification 30257.

After completion of the interconnection board layout, module and stack layouts were made and fabrication of these units begun. The printed circuit board was also being fabricated during this time.

The assembled modules after prepot testing were potted in Stycast 2850 FT, but had difficulty in temperature after potting. It was found after careful evaluation that the potting was too severe on the package. Therefore, prior to potting the modules in the Stycast 2850 FT, they were dip coated in RTV 11 silicon rubber.

The potted modules were finally symbolized and installed in the subchassis. The module leads were welded to the printed circuit board risers and the system was tested from -25°C to +100°C.

For a more detailed history of the program, refer to Progress Reports No. 1 through No. 7.

SECTION V

TESTING AND CALIBRATION

The testing involved in this program other than breadboard evaluation was in the form of prepot and postpot testing of the modules and system test. The test procedures for each of these tests, prepot and postpot, are shown in Appendix E.

Some mention of the exact prepot testing is in order due to the rigorous thermal shock given the units. After assembly, the modules are tested in the following manner:

1. Perform all performance tests at room temperature.
2. Place unit in -55°C chamber for one-half hour and perform all performance tests.
3. Take immediately from -55°C chamber to +110°C chamber and leave for one-half hour. Perform all tests.
4. Immediately return unit to -55°C chamber for one-half hour and perform all tests.
5. Take from -55°C chamber back to +110°C chamber and leave fof one-half hour. Perform all performance tests.

This sequence was performed on each module prior to dip-coating in RTV 11 and again prior to encapsulation in Stycast 2850 FT.

Prior to assembly of the system, the modules were installed on a printed circuit board with the module leads soldered to the long ribbons welded to a printed circuit board. They were then given a room temperature system test to verify that the modules and the printed circuit board were correct.

SECTION VI

RECOMMENDATIONS

A. Electrical

If the present Series 53 networks are considered, the first recommended change involves loading the D code output with an inverter stage to clean the output when it is in the ONE state. At present, when the inverter output assumes the ONE state, its level changes as the other inputs to the driven gates switch. This is due to the top transistor in the inverter stage operating below the knee of its V_c vs i_c curve since there is virtually no load on the circuit. Thus, any leakage current needed by the driven gates produces a noticable voltage change at the output of the inverter. Therefore, the number of gates disabled by other signals determines the amount of leakage current drawn from the inverter which in turn determines the voltage level at which any particular ONE will be. The inverter load or a 5 to 10K load causes this inverter to operate beyond the knee of its V_c vs i_c curve and thus, these changes in ic are not evident in the output voltage level. Since this was not discovered until systems test and has no effect on the reliability of the system, it was felt that any corrective action at this stage could only be time consuming and expensive with no real purpose being gained.

Second, the word detector pulse for the X code component generator could be generated in a different manner and save one network. This would be done by using half of SN533 A2 and inverting its output with the unused circuit in SN535 A8.

When the new additions to the standard Series 53 line are developed and available (sometime in August) a savings of between 20 and 30 networks can be realized in implementing the logic expressions. This in turn will result in a less complex package.

The proposed new standard networks to be added to the standard line are as follows:

1. 4-2 input NAND
2. 3-3 input NAND
3. 2-5 input NAND
4. 3-2 input AND
5. 2-EX OR
6. 1-ONE SHOT

Some of the networks would be in the 14 lead package.

The modules resulting from this addition would require the following quantities of networks.

	Present Network Types					New Devices				Total	No.
Module	SN530	SN531	SN532	SN533	SN535	1.	2.	3.	5.	No.	Leads
X Seq. Gen.	4				2		2			8	11
A Seq. Gen.	5			1	1		1			8	6
B Seq. Gen.	7			1	1		1	1		11	6
C Seq. Gen.	5				1		1	1		8	6
D Seq. Gen.	7	2	1		1		1			12	18
D Out Gating		2	4					9		15	18
T and Rcvr.	4	1	1	1	1	1	5		2	16	23
E Seq. Gen.	7	2	2		1		1			13	6
TOTAL	39	7	8	3	8	1	12	11	2	91	Networks

This is a savings of 24 networks over the present system. Each function could be generated in one module while still maintaining a throw-away level of 16 networks.

The logic functions would be generated in the same manner as the present system except for the word detector pulses and the combination logic. The word detector pulses would be generated using NAND Gates followed by inverter stages. If the polarity of the word detector pulse was not important, the inverter could be left off.

The code-component combining logic would only be changed in the area of performing the function $A \oplus B \oplus C \oplus D \oplus E$. At present, this function is generated by the following manipulation:

$$[A \oplus B \oplus C] \oplus [D \oplus E]$$

The new EX OR network would allow this expression to be generated with less networks in the following manner:

$$[(A \oplus B) \oplus (C \oplus E)] \oplus [D]$$

The system logic design could be tailored a little more to the new networks with further investigation and save a few additional networks.

The circuits for these new devices are identical to those of the present NAND and AND gates except that each emitter output pull-down resistor of the AND gates are brought out on individual leads to $-V_{EE}$. The EX OR device is similar to two AND gates tied together feeding an inverter.

The modules using the 10 lead network package measures 0.350 x 1.100 inches for the three network stack. With the 14 lead package the length would be increased to 1.400 inches. The height of the module would be determined by the number of network and interconnections involved. A sample using 15 networks was only 0.350 inches in height prior to encapsulation. The height of an 18 network module would be about 0.425 inches unpotted. This allows 0.150 for potting compound and header board or carrier board before the 0.575 standard module height is reached. An example of the modified stack is shown in Figure 18.

3. Stacked Printed Circuit Boards

The second approach to packaging the networks is to use small etched printed circuit boards to interconnect the networks. The printed circuit boards would be small enough to be encapsulated in one module. Four networks would be attached to each printed circuit board and interconnections would be made around the periphery. These boards would then be connected to a header board if a predesigned hole pattern were used and if not, there would be no need for a header board. The leads would protrude from the package as they were spaced inside around the printed circuit boards.

This system would be very advantageous in a high volume production contract. The assembly time of a module would be greatly shortened.

The one shot is very similar to the J-K Flip-Flop. The range of delay within the one shot has not been disclosed. Like the J-K Flip-Flop, the normal and complement inputs are available to allow the device to be triggered by either a positive or negative pulse.

B. Mechanical

1. General

Due to the configuration of the integrated circuit package, the general packaging philosophy must be investigated. This investigation must be conducted at the system level, although subsystem and module packaging changes could take better advantage of the small network package.

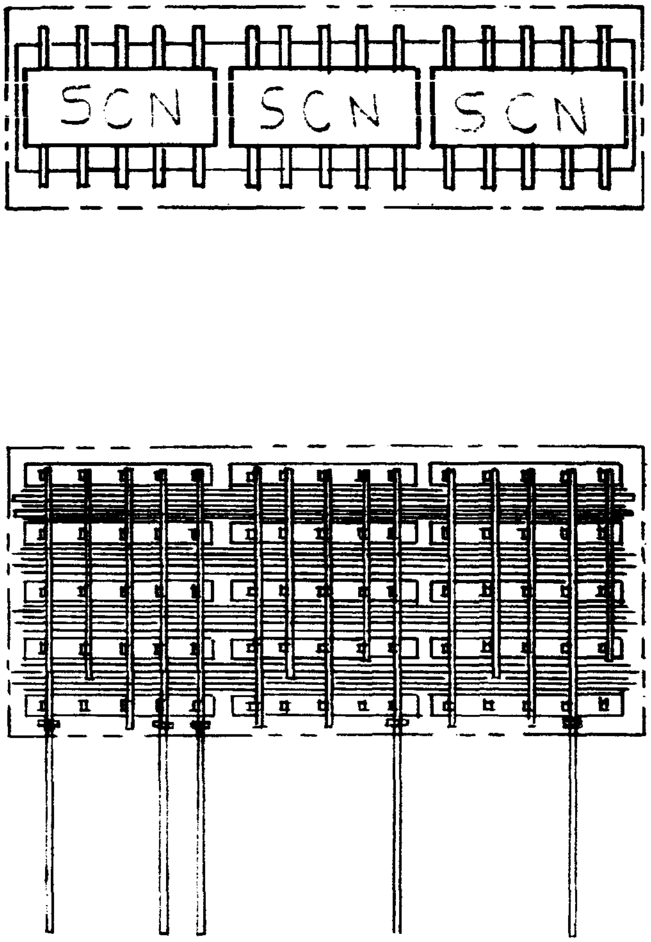
Restraining the package configuration to the subchassis is in itself not detrimental to miniature packaging. However, confining the modules to the standard hole pattern places extreme limitations on the packaging. Given complete freedom within the subchassis, Texas Instruments can produce a much smaller and lighter sequence generator than was produced during this contract period. However, all interconnections between modules would be made on the same side of the chassis where the modules are located. There are several approaches that can be taken to package the individual units. The two most attractive to Texas Instruments at this time are a modified network stack and a stacked printed circuit board package.

2. Modified Stack

The modified stack takes advantage of Texas Instruments past experience in three dimensional network packaging. The stacks would be three networks in width thus accommodating more circuitry in a shorter stack. The interconnections would be made using a sheet of kovar etched with leads spaced on .050 centers and located to align with the network leads. The insulation tape between these interconnections would be increased in width and length to prevent shorts from occurring. There would be an overlay of tape at least .015 on each side of the network and .030 between interconnection wafers. This coupled with the experience of the layout personnel would eliminate any shorting problems.

This type of stack could easily house 15 networks and could incorporate as many as 18 networks. The stack leads could be adapted to the standard module lead pattern, but this creates unnecessary use of space and involves two more welds per lead. A better approach and the one recommended by Texas Instruments is to use the stack leads as module leads and not feed them through the subchassis hole pattern. This would double the packaging space by allowing components to be mounted on each side of the subchassis.

The modules would be mounted to a carrier board in a manner similar to that used on the sequence generator. The complete assembly would then be mounted in the subchassis by means of screws and studs. Prior to being installed in the subchassis, the modules are bonded to the board.



19634

Figure 18. Modified Stack

SECTION VII

CONCLUSION

The contents of this report were not designed to present a complete picture of the work done by Texas Instruments Incorporated on the Integrated Circuit Sequence Generator contract. However, it is hoped that by giving the program highlights and making specific recommendations for improvements, some redundancy in effort and time can be eliminated in future programs of similar nature.

The equipment delivered to Jet Propulsion Laboratory is regarded with a high degree of confidence. However, it is our policy to continually strive for improved reliability, quality, and performance. It is in this realm that the recommendations were made for improvement in the existing equipment.

Texas Instruments has been pleased to work with Jet Propulsion Laboratory on this contract. It is hoped that our experience, technology and insight developed in this effort may be applied to future programs.

F. D. Clark

F. D. CLARK
Engineer
Space Instrumentation Systems

W. D. Thomas

W. D. THOMAS
Project Engineer
Space Instrumentation Systems

WDT:FDC:jb

APPENDIX A

SPECIFICATION INDEX

SPECIFICATION INDEX

The integrated circuit sequence generator and associated documentation was designed and built to meet the requirements of the following JPL specifications.

20016	General Specification, Workmanship Requirements for Electronic Equipment as applicable to the stack method of SOLID CIRCUIT semiconductor welded modules
20017	General Specification, Preparation of Reports of Contractors
20064	General Specification, Packing Equipment for Shipment Within the Continental United States
30257	Environmental Specification, Mariner B Flight Equipment as specified in JPL Specification No. 31243 Section 3.5.7.1
31224	Design Specification, Flight Equipment Telecommunication Development, Component Packaging
31243	Design Specification, Spacecraft Flight Equipment Telecommunication Development, Integrated Circuit Sequence Generator.

APPENDIX B

DRAWING INDEX

514708

A

DASH NO.	QTY	NEXT ASSY NO.	SIZE	PROJ NO.
				464

REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPROVED

DRAWING INDEX
FOR
INTEGRATED CIRCUIT
SEQUENCE GENERATOR

QTY REQD -2	QTY REQD -1	ITEM NO.	DWG SIZE	TEXAS INSTRUMENTS PART OR IDENTIFYING NO.	GOVT OR INDUSTRY PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

LIST OF MATERIALS

DR G Secondini	DATE 6-15-64	
CKD		
ENGR		
APPD		
DESIGN ACTIVITY RELEASE		

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

TITLE
INDEX, INTEGRATED
CIRCUIT SEQUENCE GENERATOR DRAWING

CODE IDENT NO. 96214
SIZE A
DRAWING NO. 514708
SCALE NONE
WT
SHEET 1 of 5

TI 1E1793-A

DATE:		96214 CODE IDENT	DL SHEET 2 OF 5 SHEETS

	SPECIFICATION	MODEL
GOVT		
CONTR		

CONTRACT NO: 950693

ITEM NOMENCLATURE

INTEGRATED CIRCUIT
SEQUENCE GENERATOR

REV

DWG SIZE	CODE IDENT	DOCUMENT IDENT NO.	REV	DOCUMENT NOMENCLATURE
A		F-48		TIN PLATE
A		F-59		ENAMEL, LIGHT GRAY
A		F-100		MARKING
A		410499		INSULATION SLEEVING, ELECTRICAL
A		411329		PLASTIC SHEET, LAMINATED
A		412599		RESIN, EPOXY
A		412600		HARDENER, EPOXY RESIN
A		415218		INSULATION SHEET, ELECTRICAL
A		415501		WIRE, NICKEL, FLAT
A		415528		INSULATION VARNISH, ELECTRICAL
A		415572		WIRE, NICKEL, ROUND
A		415584		NICKEL-COBALT-IRON ALLOY STRIP
A		415593		COMPOUND, EPOXY RESIN, CURED
A		415806		WIRE, FLAT, NICKEL-COBALT-IRON ALLOY
B		490861		WIRE, ELECTRICAL, NICKEL, ROUND, MODIFIED
D		514650		BLOCK DIAGRAM, SEQUENCE GENERATOR
C		514651		DIAGRAM, LOGIC, A SEQUENCE GENERATOR
D		514652		DIAGRAM, LOGIC, B SEQUENCE GENERATOR
C		514653		DIAGRAM, LOGIC, C SEQUENCE GENERATOR
D		514654		DIAGRAM, LOGIC, D SEQUENCE GENERATOR
C		514655		DIAGRAM, LOGIC, D OUTPUT GATING NO. 1

REV LTR

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION
DALLAS, TEXAS

DWG NO. DL 514708

CODE IDENT NO. 96214 SHEET 2

TI-1786

DATE:		96214 CODE IDENT	DL SHEET 3 OF 5 SHEETS	REV

	SPECIFICATION	MODEL
GOVT		
CONTR		

CONTRACT NO: 950693

ITEM NOMENCLATURE

INTEGRATED CIRCUIT
SEQUENCE GENERATOR

DWG SIZE	CODE IDENT	DOCUMENT IDENT NO.	REV	DOCUMENT NOMENCLATURE
C		514656		DIAGRAM, LOGIC, D OUTPUT GATING NO. 2
D		514657		DIAGRAM, LOGIC, E SEQUENCE GENERATOR
C		514658		DIAGRAM, LOGIC, TRANSMITTER AND RECEIVER NO. 1
D		514659		DIAGRAM, LOGIC, TRANSMITTER AND RECEIVER NO. 2
D		514660		DIAGRAM, LOGIC, X SEQUENCE GENERATOR
D		514661		SUBCHASSIS, MODIFIED
D		514662		SEMICONDUCTOR NETWORK, A SEQUENCE GENERATOR
D		514663		SEMICONDUCTOR NETWORK, E SEQUENCE GENERATOR
D		514664		SEMICONDUCTOR NETWORK, C SEQUENCE GENERATOR
D		514665		SEMICONDUCTOR NETWORK, X SEQUENCE GENERATOR
D		514666		SEMICONDUCTOR NETWORK, B SEQUENCE GENERATOR
D		514667		SEMICONDUCTOR NETWORK, TRANSMITTER AND RECEIVER NO. 1 (STACK NO. 2)
D		514668		SEMICONDUCTOR NETWORK, D OUTPUT GATING NO. 2 (STACK NO. 1)
D		514669		SEMICONDUCTOR NETWORK, D OUTPUT GATING NO. 2 (STACK NO. 2)
D		514670		SEMICONDUCTOR NETWORK, TRANSMITTER AND RECEIVER NO. 2 (STACK NO. 1)
D		514671		SEMICONDUCTOR NETWORK, TRANSMITTER AND RECEIVER NO. 2 (STACK NO. 2)
C		514672		MODULE HEADER BOARD NO. 1
B		514673		STACK INSULATOR
C		514674		INSULATION SHEET, PRINTED CIRCUIT BOARD

REV LTR

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION
DALLAS, TEXAS

DWG NO. DL 514708
CODE IDENT NO. 96214 SHEET 3

		96214	DL	
DATE:		CODE IDENT	SHEET 4 OF 5 SHEETS	REV

	SPECIFICATION	MODEL
GOVT		
CONTR		

CONTRACT NO: 950693

ITEM NOMENCLATURE

INTEGRATED CIRCUIT
SEQUENCE GENERATOR

DWG SIZE	CODE IDENT	DOCUMENT IDENT NO.	REV	DOCUMENT NOMENCLATURE
D		514675		SEMICONDUCTOR NETWORK, D SEQUENCE GENERATOR (STACK NO. 1)
D		514676		SEMICONDUCTOR NETWORK, D SEQUENCE GENERATOR (STACK NO. 2)
D		514677		SEMICONDUCTOR NETWORK, TRANSMITTER AND RECEIVER NO. 1 (STACK NO. 1)
D		514678		SEMICONDUCTOR NETWORK, D OUTPUT GATING NO. 1 (STACK NO. 1)
D		514679		SEMICONDUCTOR NETWORK, D OUTPUT GATING NO. 1 (STACK NO. 2)
D		514680		A SEQUENCE GENERATOR
D		514681		B SEQUENCE GENERATOR
D		514682		C SEQUENCE GENERATOR
D		514683		D SEQUENCE GENERATOR
D		514684		E SEQUENCE GENERATOR
D		514685		X SEQUENCE GENERATOR
D		514686		D OUTPUT GATING NO. 1
D		514687		D OUTPUT GATING NO. 2
D		514688		TRANSMITTER AND RECEIVER NO. 1
D		514689		TRANSMITTER AND RECEIVER NO. 2
C		514690		CONNECTOR ASSEMBLY 25 PIN
D		514691		MODULE HEADER BOARD NO. 2
A		514692		MARKING, A SEQUENCE GENERATOR
A		514693		MARKING, B SEQUENCE GENERATOR

REV LTR

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION
DALLAS, TEXAS

DWG NO. DL 514708	
CODE IDENT NO. 96214	SHEET 4

TI-1786

		96214	DL	
DATE:		CODE IDENT	SHEET 5 OF 5 SHEETS	REV

	SPECIFICATION	MODEL
GOVT		
CONTR		

CONTRACT NO: 950693

ITEM NOMENCLATURE

INTEGRATED CIRCUIT
SEQUENCE GENERATOR

DWG SIZE	CODE IDENT	DOCUMENT IDENT NO.	REV	DOCUMENT NOMENCLATURE
A		514694		MARKING, C SEQUENCE GENERATOR
A		514695		MARKING, D SEQUENCE GENERATOR
A		514696		MARKING, E SEQUENCE GENERATOR
A		514697		MARKING, X SEQUENCE GENERATOR
A		514698		MARKING, D OUTPUT GATING NO. 1
A		514699		MARKING, D OUTPUT GATING NO. 2
D		514700		SEQUENCE GENERATOR ASSEMBLY
A		514701		MARKING, TRANSMITTER AND RECEIVER NO. 1
A		514702		MARKING, TRANSMITTER AND RECEIVER NO. 2
A		514703		MARKING, CONNECTOR ASSEMBLY
D		514704		PRINTED CIRCUIT BOARD, SEQUENCE GENERATOR
B		514705		CONNECTOR SUBASSEMBLY, 25 PIN
A		514706		RISER CONNECTIONS, KOVAR
A		514707		MARKING, SEQUENCE GENERATOR

REV LTR

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION
DALLAS, TEXAS

DWG NO. DL 514708
CODE IDENT NO. 96214 SHEET 5

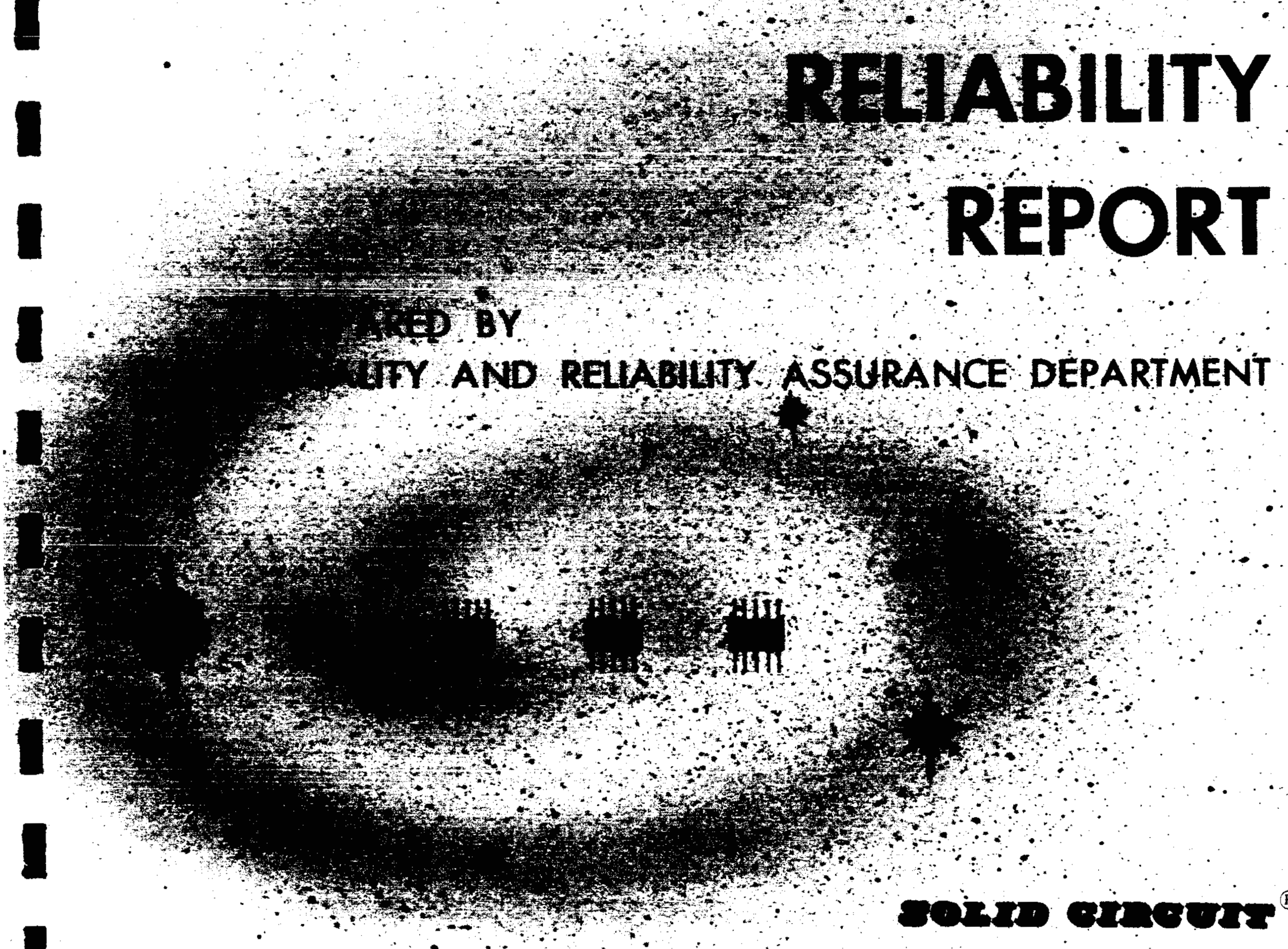
APPENDIX C

NETWORK RELIABILITY

1963

RELIABILITY REPORT

ARED BY
LITY AND RELIABILITY ASSURANCE DEPARTMENT



SOLID CIRCUIT®

SEMICONDUCTOR NETWORKS

TEXAS INSTRUMENTS INCORPORATED

P. O. BOX 5012 • DALLAS 22, TEXAS

SEMICONDUCTOR NETWORK
REPORT ON RELIABILITY

1963

Prepared by
QUALITY & RELIABILITY ASSURANCE DEPARTMENT
SEMICONDUCTOR-COMPONENTS DIVISION

TEXAS INSTRUMENTS INCORPORATED

FOREWORD

This report contains reliability test results on SOLID CIRCUIT® semiconductor net works. It was prepared by the Quality and Reliability Assurance Department, Semiconductor-Components Division, Texas Instruments Incorporated.

The semiconductor networks tested were production units of the Series 51 family, manufactured during the period January 1963 through March 1964.

This data is presented to assist in the use of Texas Instruments Semiconductor Networks. While the data presented is accurate to the best of our knowledge, it is not intended to constitute a guarantee of product reliability.

Samuel L. Carrell, Manager
Quality and Reliability Assurance Department
Semiconductor - Components Division

TABLE OF CONTENTS

SUMMARY

The 1963 SOLID CIRCUIT® Semiconductor Network Reliability Report contains reliability information on over 9000 Series 51 semiconductor networks. This extensive reliability program, initiated over three years ago by Texas Instruments Incorporated, produced resultant data and information from manufacturing facilities that were constructed with specially designed equipment for increased production. With this increased production rate, the reliability of semiconductor networks continues to improve.

Implementation of process improvements and increased number of components per package will continue to give improved reliability. More and more circuit functions are being designed into a single network package. This has the advantage of giving a potentially lower cost per function and an improvement in reliability. This reliability improvement is due to the fact that the reliability of a single circuit on a master bar would have approximately the same reliability as if several circuits were incorporated into the same bar.

The table below summarizes the results of test performed on Series 51 semiconductor networks.

Type Test	Units on Test	Total Equivalent Network Hours	Failure Rate
Weekly-Add-To and Accelerated Testing at 125°C and 200°C	1454	9,151,000 at 85°C	0.06%/1000 hours thru 1st quarter 1964
Operational Field Data	7116	5,643,492	0.018%/1000 hours
Environmental Testing	605	--	Capability in excess of Mil test levels

All test results shown in this report have been obtained on semiconductor networks tested as a complete circuit. Each network is the equivalent of approximately 20 discrete components (transistors, diodes, resistors, and capacitors) interconnected as a circuit.

Although test results are for Series 51 semiconductor networks, all networks are made on the same process lines using the same process controls. Consequently, similar test results are expected from test programs on Series 52 and Series 53.

SEMICONDUCTOR NETWORKS RELIABILITY TEST PROGRAM AND TEST RESULTS

This brochure summarizes the results of the reliability test program conducted on semiconductor networks for the period January 1963 through March 1964. The tests are designed to obtain information on the reliability of semiconductor networks, to determine device capability under severe stress, to determine existing failure modes, and to indicate corrective action in the process necessary for continued improvement of product reliability.

TEST METHODS AND FAILURE CRITERIA

Networks under test go through initial and post stress parameter testing. The conditions for parameters chosen are per the applicable Series 51 network type data sheet. To give consistent test results the criteria for failure on all internal testing is kept the same. The parameters selected are those which are most indicative of satisfactory performance in use conditions. They are measured using maximum temperature (125°C) and worst case input voltages.

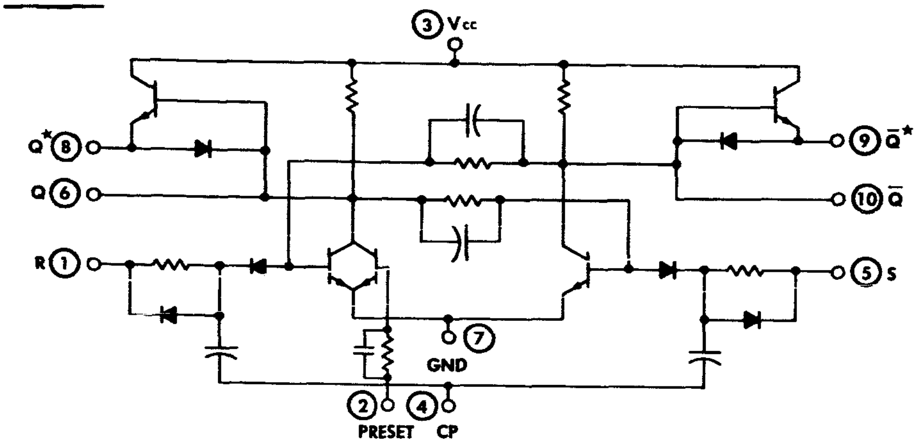
Criteria for failure are as follows:

Catastrophic Failure:	A network which becomes inoperative (short or open) or degrades sufficiently to cause definite circuit malfunction.
Degradation Failure:	
Input Current	changes more than ± 20% from initial reading.
Output Voltage	
On Level	changes more than +20% from initial reading and exceeding 0.30 volts.
Off Level	changes more than -20% from initial reading.

Circuit Diagram and Test Conditions

SN510 R-S Flip Flop
SN511A R-S Flip Flop with emitter follower output.

Circuit



Test Conditions

V_{OFF} at $V_{CC} = 6$ v, $V_{in} = 0.30$ v, $N = 0$, $T_A = 125°C$

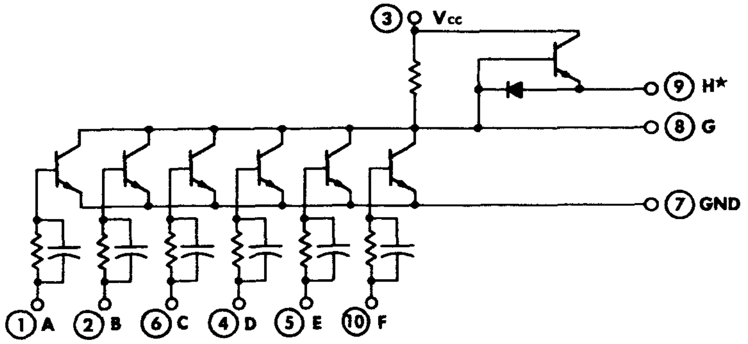
V_{OFF} at $V_{CC} = 6$ v, $V_{in} = 0.30$ v, $N = 4$, $T_A = 125°C$

V_{ON} at $V_{CC} = 6$ v, $V_{in} = 2.0$ v, $N = 4$, $T_A = 125°C$

I_{in} at $V_{CC} = 6$ v, $V_{in} = 2.0$ v, $N = 0$, $T_A = 125°C$

SN512 6 Input NOR/NAND Gate
SN513A 6 Input NOR/NAND Gate

Circuit



Test Conditions

V_{OFF} at $V_{CC} = 6$ v, $V_{in} = 0.30$ v, $N = 0$, $T_A = 125°C$

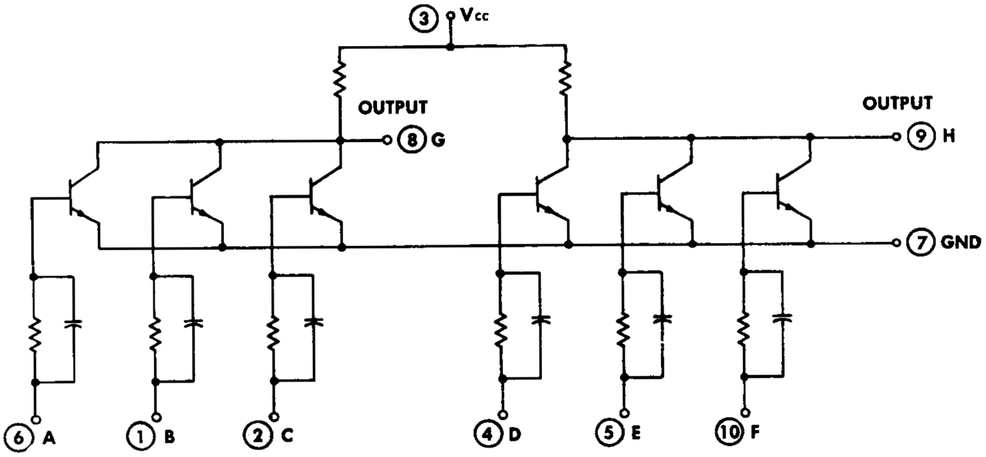
V_{OFF} at $V_{CC} = 6$ v, $V_{in} = 0.30$ v, $N = 5$, $T_A = 125°C$

V_{ON} at $V_{CC} = 6$ v, $V_{in} = 2.0$ v, $N = 0$, $T_A = 125°C$

I_{in} at $V_{CC} = 6$ v, $V_{in} = 2.0$ v, $N = 0$, $T_A = 125°C$

SN514A Dual NOR/NAND Gate

Circuit



Test Conditions

V_{OFF} at $V_{CC} = 6$ v, $V_{in} = 0.30$ v, $N = 0$, $T_A = 125°C$

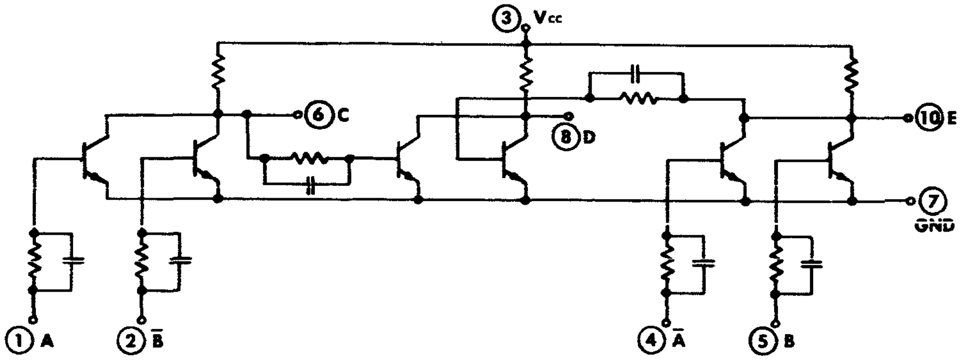
V_{OFF} at $V_{CC} = 6$ v, $V_{in} = 0.30$ v, $N = 5$, $T_A = 125°C$

V_{ON} at $V_{CC} = 6$ v, $V_{in} = 2.0$ v, $N = 0$, $T_A = 125°C$

I_{in} at $V_{CC} = 6$ v, $V_{in} = 2.0$ v, $N = 0$, $T_A = 125°C$

SN515A "Exclusive OR" Gate

Circuit



Test Conditions

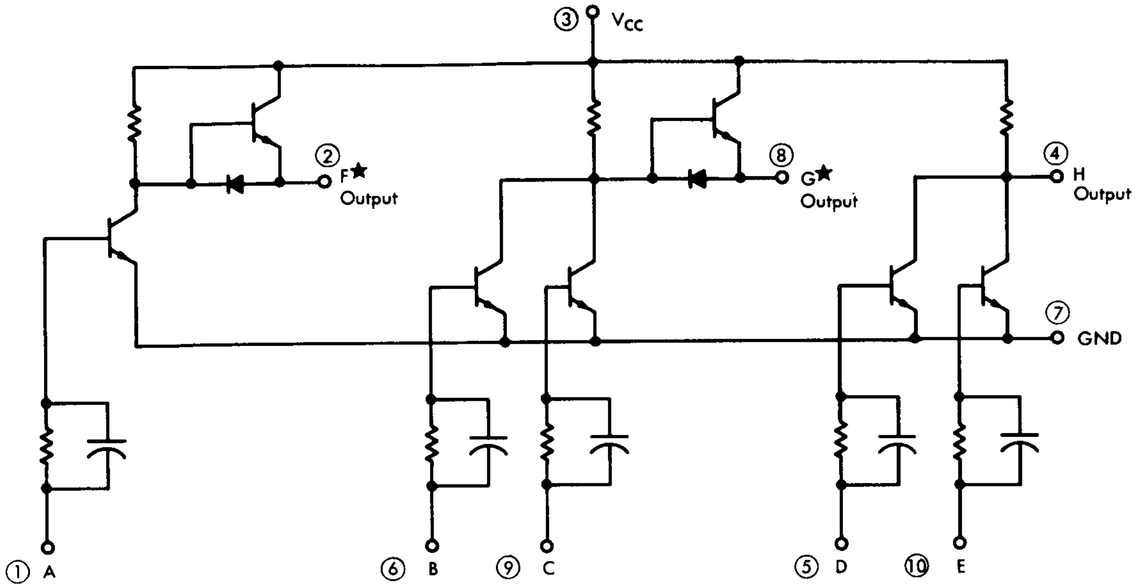
V_{OFF} at $V_{CC} = 6$ v, $V_{in} = 0.30$ v, $N = 0$, $T_A = 125°C$

V_{OFF} at $V_{CC} = 6$ v, $V_{in} = 0.30$ v, $N = 4$, $T_A = 125°C$

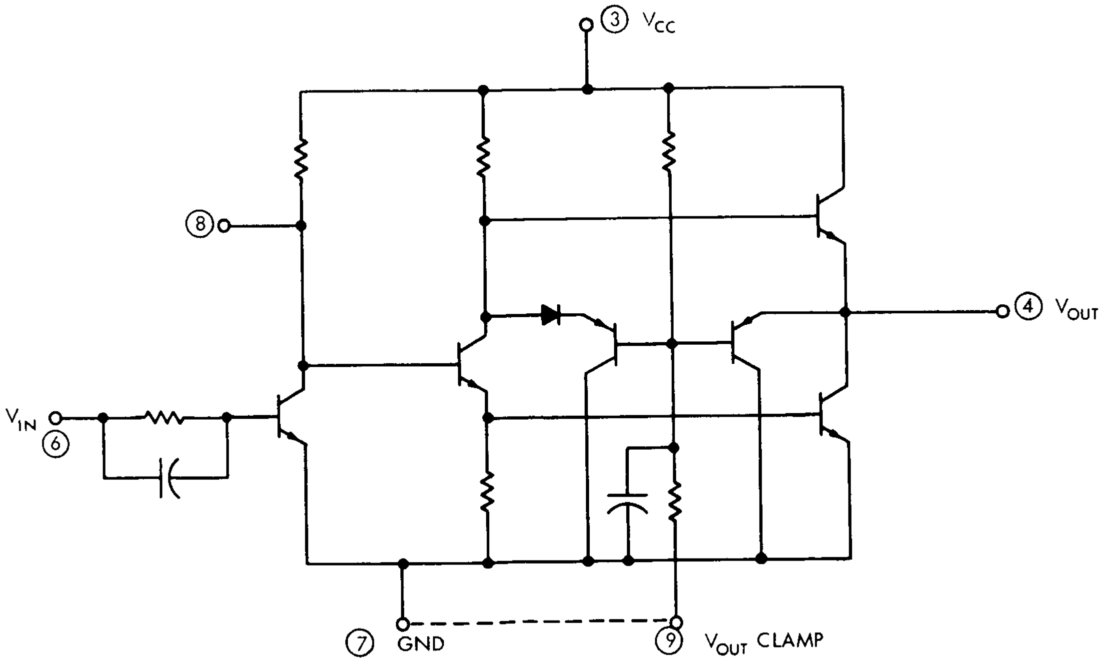
V_{ON} at $V_{CC} = 6$ v, $V_{in} = 2.0$ v, $N = 0$, $T_A = 125°C$

Although the following devices are not represented in the tests presented, they are catalog device types made from the same master slice as the devices tested. As such, they utilize the same technology, the same process controls, and the same production line. It is expected that the reliability of these devices is the same as that of the devices tested and presented.

SN516A DIFFUSED SILICON "TRIPLE GATE" LOGIC NETWORK CIRCUIT



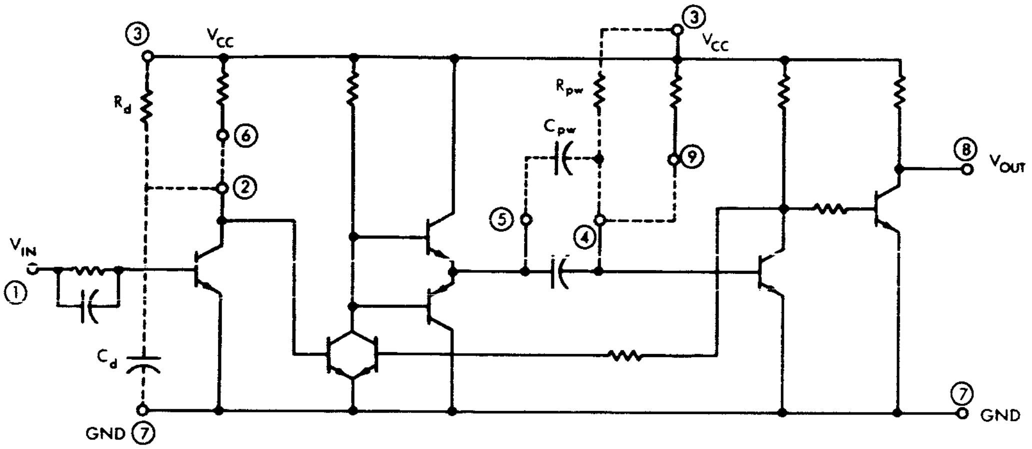
SN517A DIFFUSED SILICON "CLOCK DRIVER" NETWORK CIRCUIT



NOTE: Dotted connection shows clamped condition

SN518A DIFFUSED SILICON "ONE SHOT" NETWORK

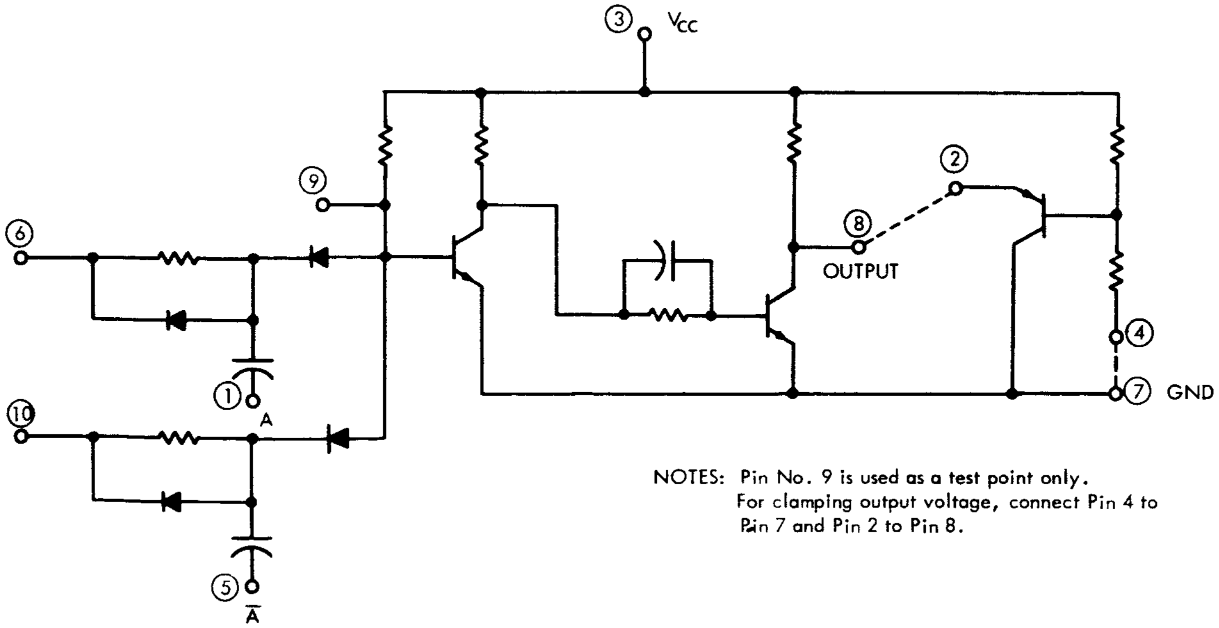
CIRCUIT



NOTE: When using internal timing, Pin No. 2 should be connected to Pin No. 6, Pin No. 4 should be connected to Pin No. 9, and Pin No. 5 should be left unconnected.

SN519A DIFFUSED SILICON "PULSE EXCLUSIVE OR" NETWORK

CIRCUIT



NOTES: Pin No. 9 is used as a test point only.
For clamping output voltage, connect Pin 4 to Pin 7 and Pin 2 to Pin 8.

A. HIGH TEMPERATURE STORAGE LIFE TESTS

Storage life tests on semiconductor networks are performed for the following reasons:

> To determine failure mechanisms in shorter test times than would be necessary at conditions during normal use.
>
> Failure rates obtained by accelerated tests can be extrapolated to fit normal use conditions.
>
> Complexity of tests performed, considering quantity and time, can be reduced through accelerated test methods.

Test Methods

Networks are first tested on failure indicative parameters and then placed on high temperature storage. These parameters are monitored at periodic test intervals. The storage temperatures used are 125°C, 200°C, and 300°C.

Summary

The table below summarizes the test results on accelerated testing at 125°C, 200°C, and 300°C storage conditions.

Type Test	Units on Test	Number Failed	Network Hours	Failure Rate %/1000 Hours
125°C Storage	100 48	2 0	934,000	0.21 (0.078 at 85°C
200°C Storage	44	0	44,000	0
300°C Storage	20	0	20,000	0

These tests continue to show capability far in excess of normal use condition storage temperatures.

Test Results

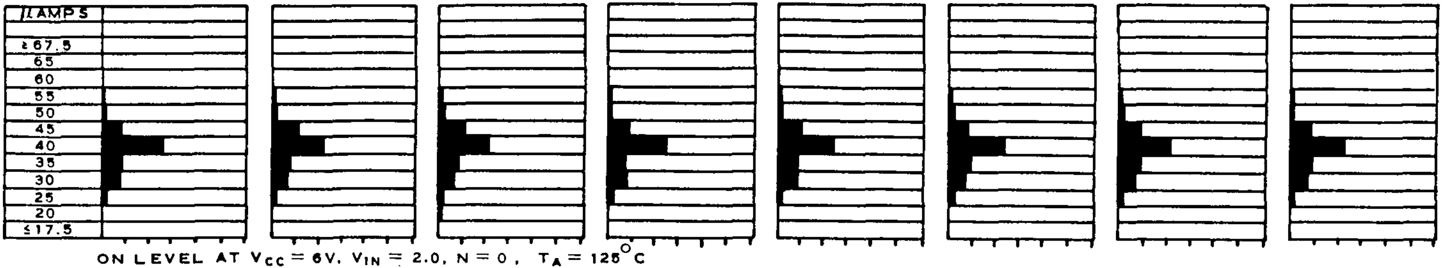
In the 1962 Reliability Brochure, test results were presented for two groups of 50 networks tested to 3000 hours at 125°C. In this report two cracked bars were noted after 2000 hours of testing. These same two groups of networks were extended to 9000 hours with no additional failures. Pages 10 and 11 show parameter distributions on these networks to 9000 hours. The corrective action steps shown in Fig. 4 under code 3 have been effective in reducing the cracked bar failure mechanism in subsequent tests.

The remainder of the following pages show six weeks of testing at 125°C, 200°C, and 300°C. These tests were performed on the new lead pattern material which eliminates the Au-Al interface that can result in formation of "purple plague." No failures occurred on the three storage tests shown.

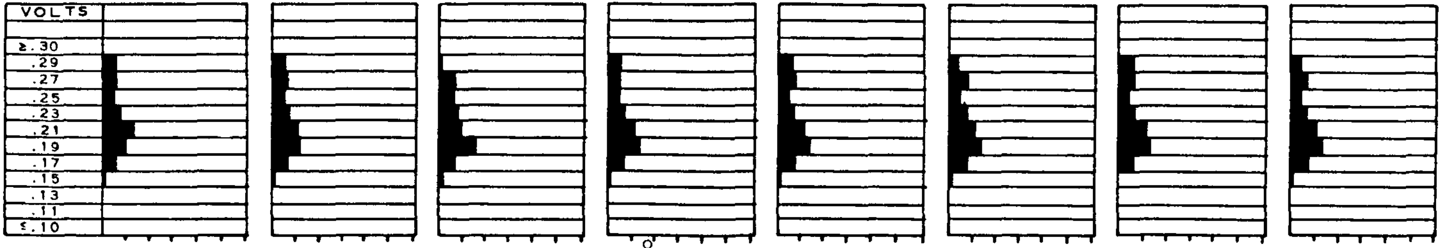
TEST PERFORMED: STORAGE LIFE @+125°C	TYPE TESTED SN512	SAMPLE SIZE 50

INITIAL DISTRIBUTION		PARAMETER BEHAVIOR ANALYSIS						
INTER-VALS		6 WEEKS	12 WEEKS	18 WEEKS	24 WEEKS	30 WEEKS	36 WEEKS	54 WEEKS

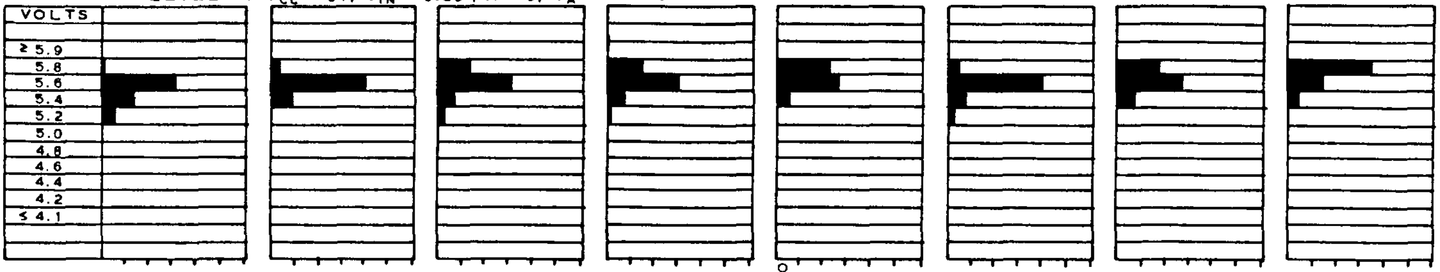
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



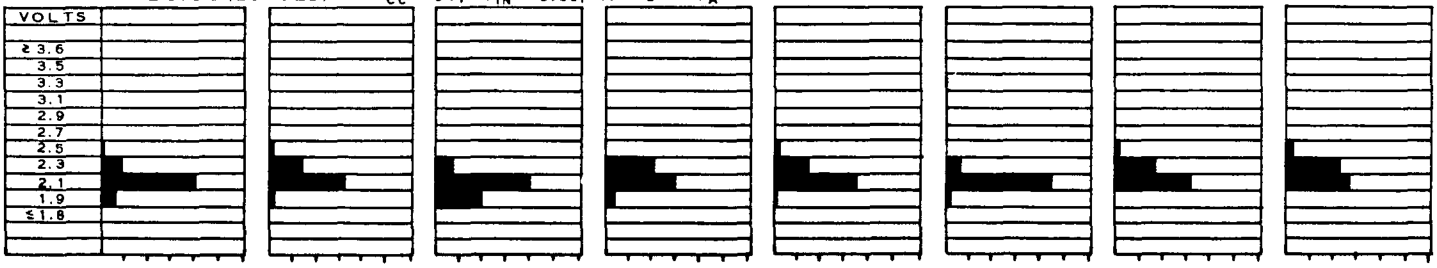
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 0, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



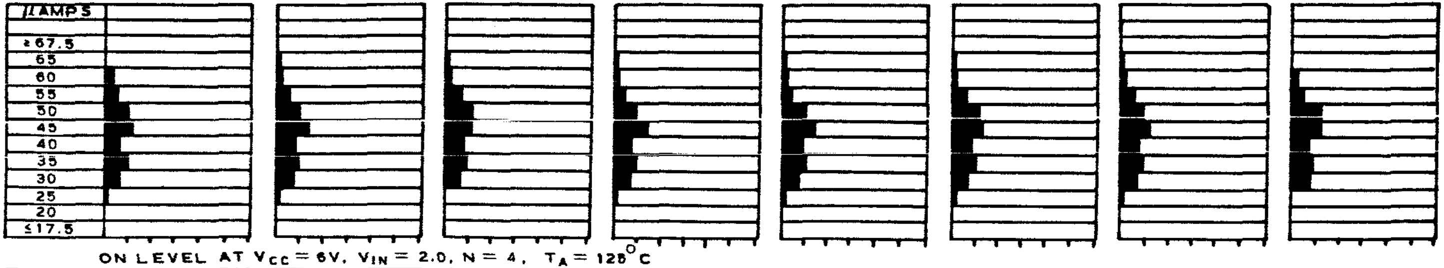
OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 5 T_A = 125°C



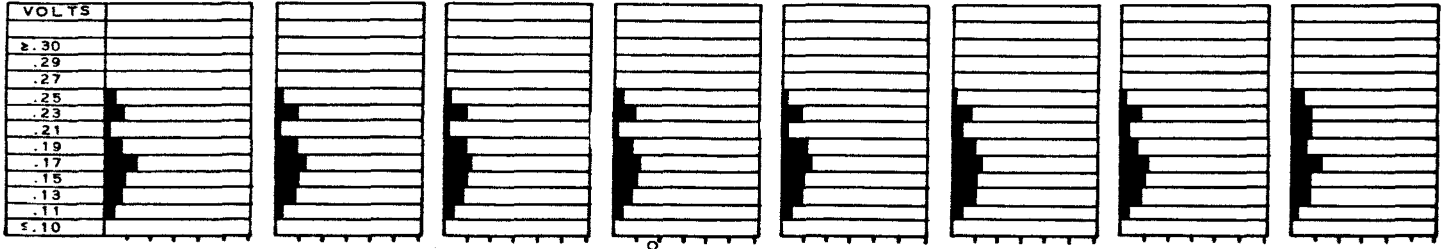
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
STORAGE LIFE @+125°C	SN510	50

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS						
INTER-VALS			6 WEEKS	12 WEEKS	18 WEEKS	24 WEEKS	30 WEEKS	36 WEEKS	54 WEEKS

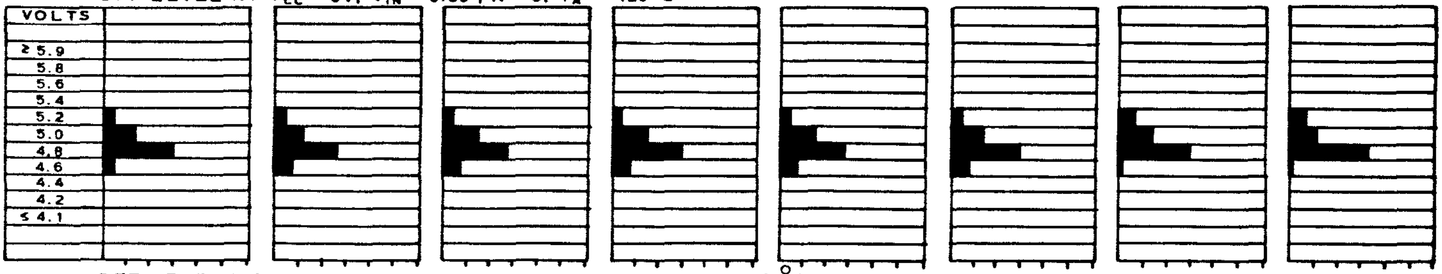
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



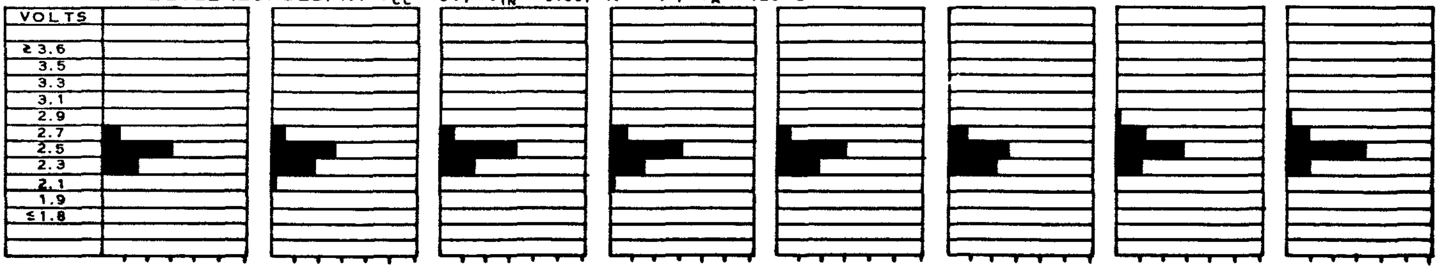
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 4, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30 , N = 0, T_A = 125°C



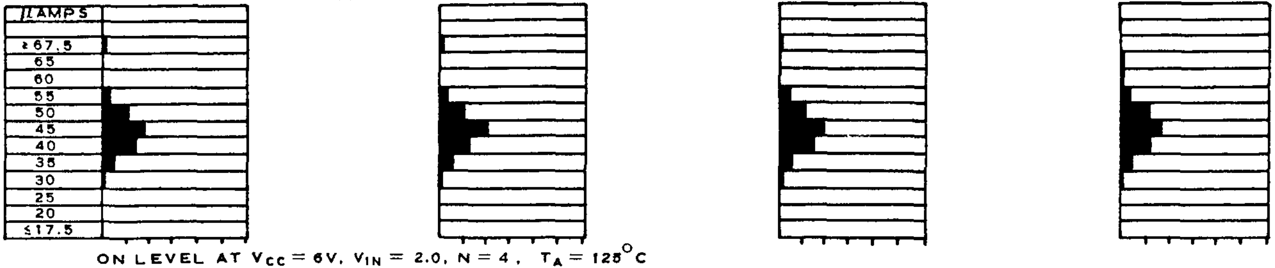
OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 4 , T_A = 125°C



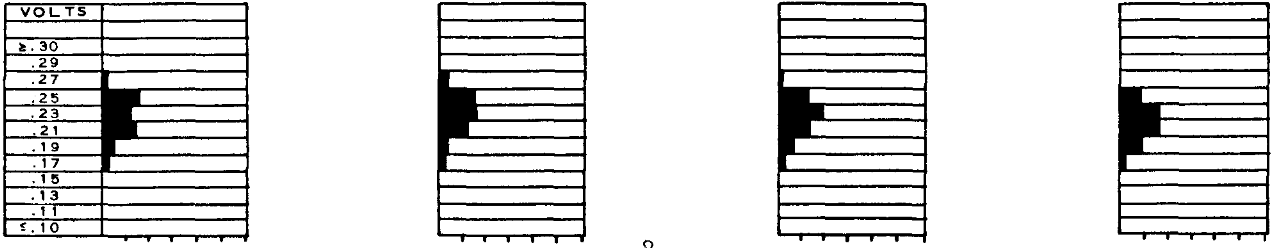
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
STORAGE LIFE @ + 125°C	SN510	48

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTERVALS				1 WEEK		3 WEEKS		6 WEEKS

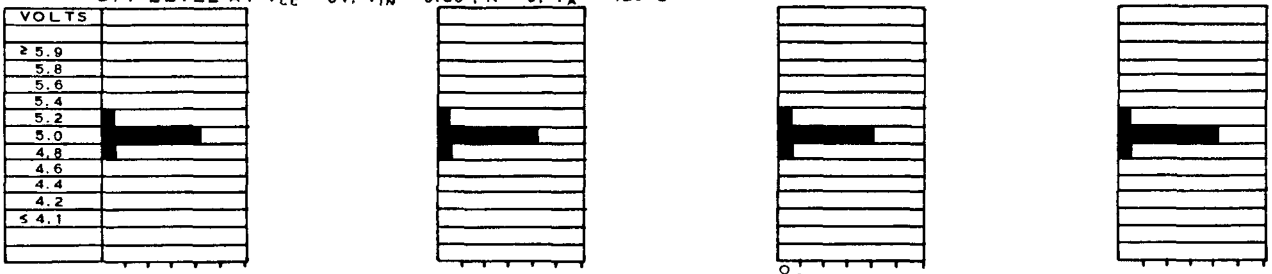
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



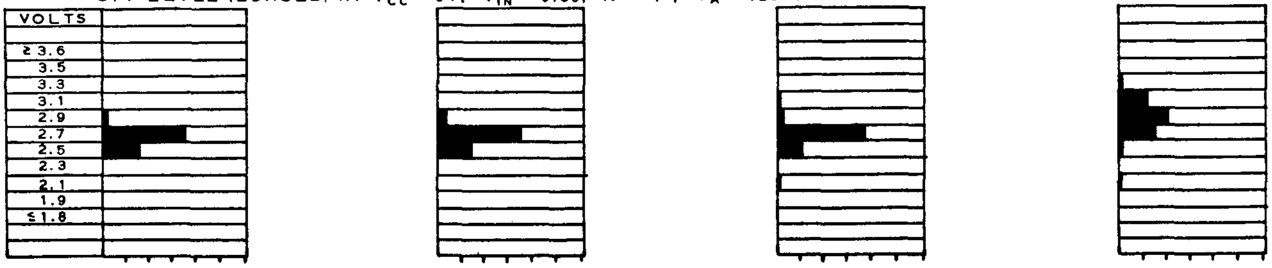
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 4, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



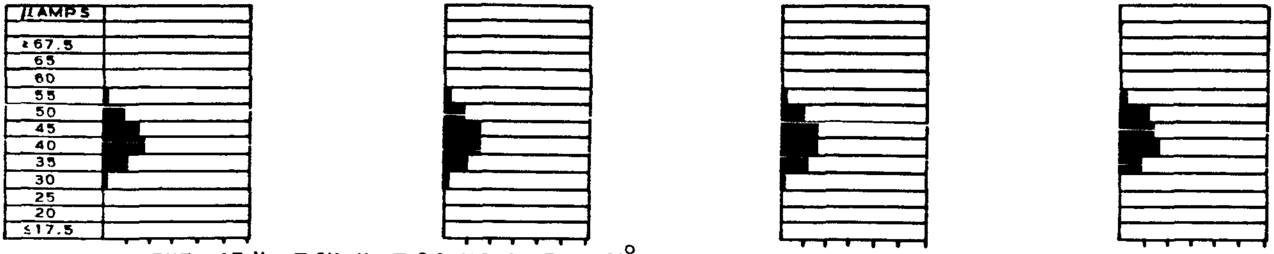
OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 4, T_A = 125°C



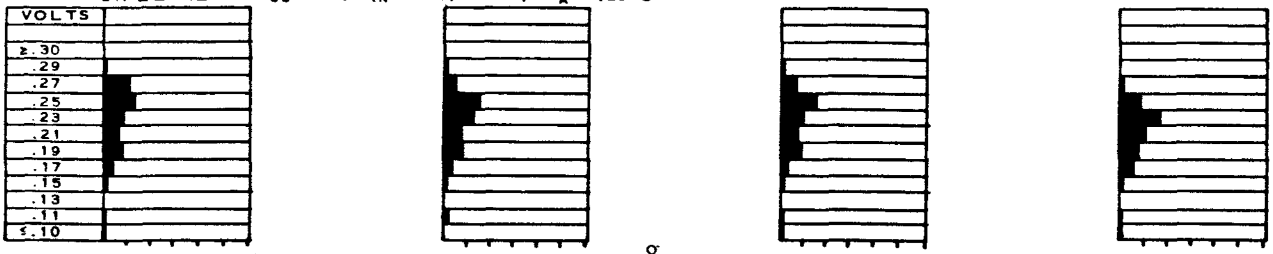
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
STORAGE LIFE @ + 200°C	SN510	44

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTERVALS				1 WEEK		3 WEEKS		6 WEEKS

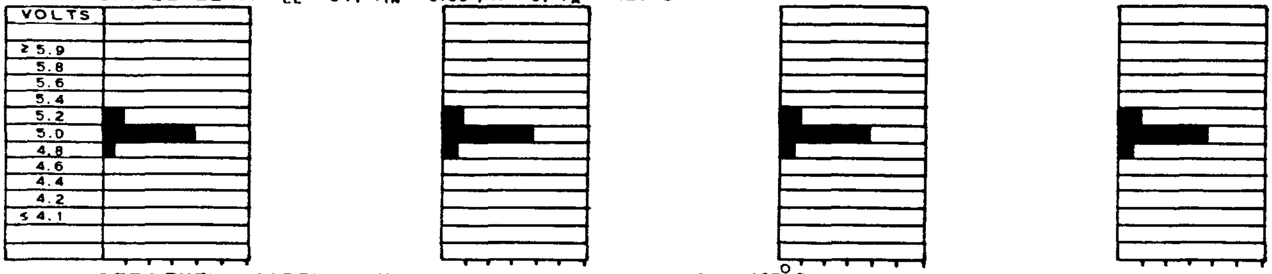
INPUT CURRENT AT $V_{CC} = 6V$, $V_{IN} = 2.0$ N = 0, T_A = 125°C



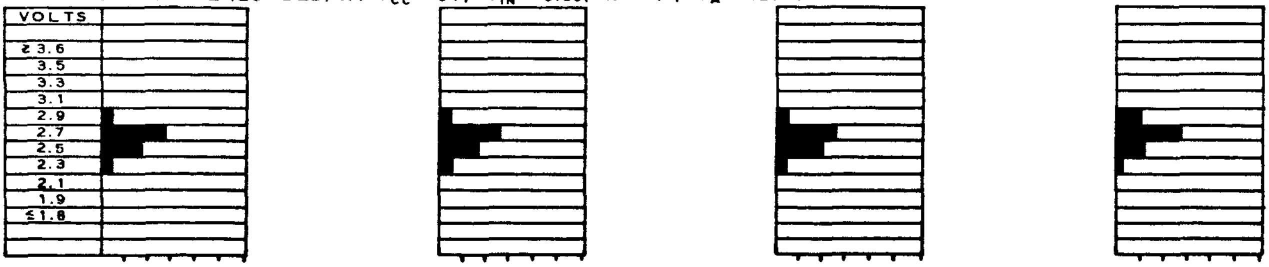
ON LEVEL AT $V_{CC} = 6V$, $V_{IN} = 2.0$, N = 4, T_A = 125°C



OFF LEVEL AT $V_{CC} = 6V$, $V_{IN} = 0.30$, N = 0, T_A = 125°C



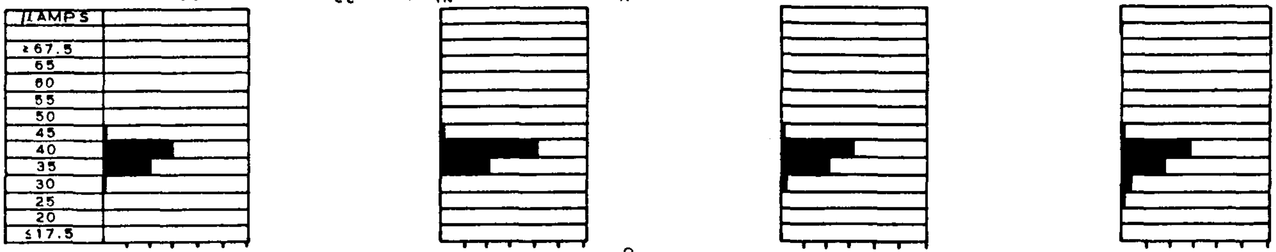
OFF LEVEL (LOADED) AT $V_{CC} = 6V$, $V_{IN} = 0.30$, N = 4, T_A = 125°C



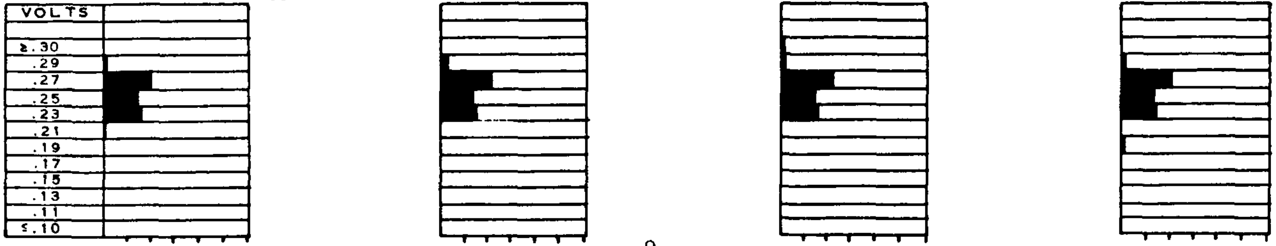
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
STORAGE LIFE @ + 300°C	SN514	20

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTERVALS				1 WEEK		3 WEEKS		6 WEEKS

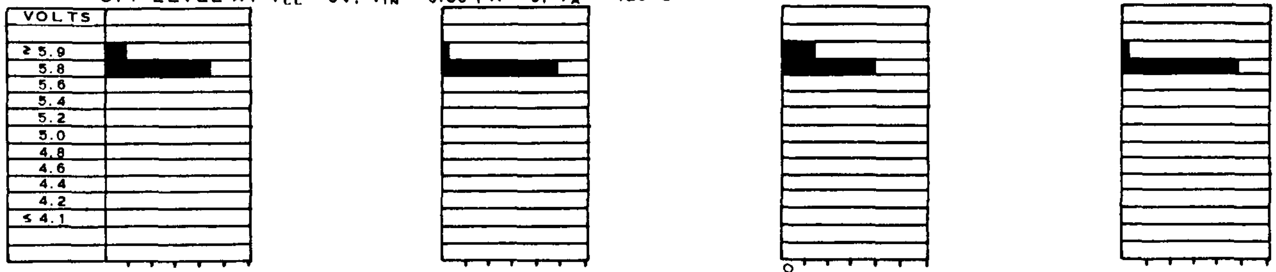
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



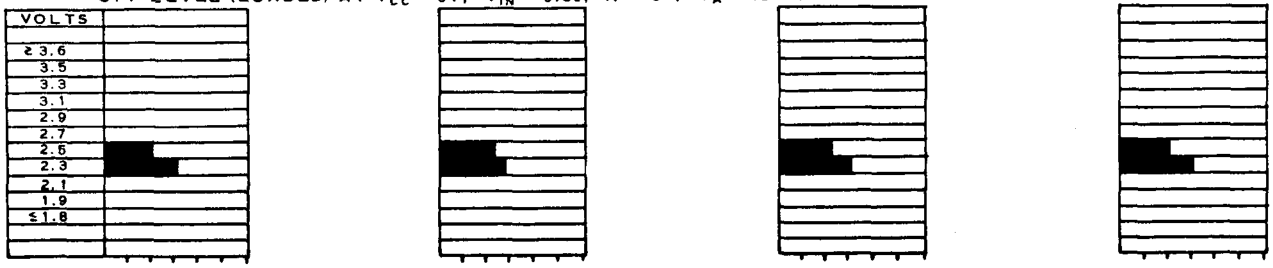
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 0, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 5, T_A = 125°C



B. WEEKLY-ADD-TO TESTS

Test Program

The Weekly-Add-To test program is a continuous reliability control test of production networks. Each week a random sample of twenty Series 51 semiconductor networks is taken from devices produced in the previous week and placed on operating life at $T_A = 125°C$, $V_{CC} = 6$ v, and storage life at $T_A = 200°C$. Ten networks are subjected to each test. The networks remain on test for twelve weeks. They are then removed and the tests are discontinued except for those units which each quarter are extended on test indefinitely to obtain long-term reliability data.

Defect analysis of all Weekly-Add-To failures is performed so that the information obtained can be passed back to the Integrated Circuits Department and/or Process Control Stations, as appropriate, for implementation of necessary corrective action.

Summary

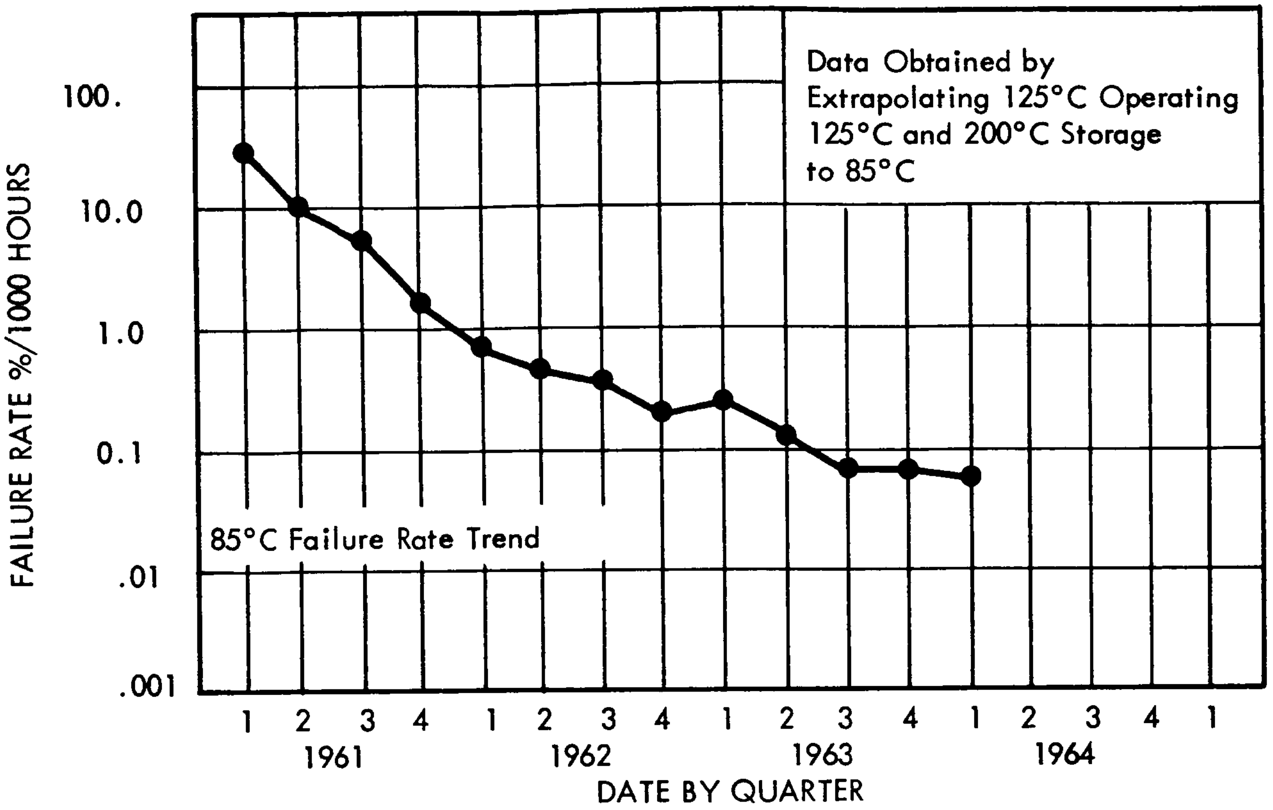
The reliability trend shows failure rates currently below 0.1%/1000 hours. Indications are that network failure rates are approaching those of discrete components. Recent articles comparing systems composed of networks versus discrete component counterparts verify that this is the case — quotes of MTBF improvements ranging from 6.6 to 30 have been noted.

Test Results

A combined summary of 125°C operating life and 200°C storage life results by quarter is given in Fig. 1. The points are obtained by considering the relationship of failure rate versus temperature. Testing performed at 200°C and/or 125°C is related to 85°C by use of the appropriate acceleration factor. These acceleration factors are given below:

Temperature	Factor
300°C	20.0
200°C	7.5
125°C	2.7
85°C	1.0
55°C	0.4
25°C	0.15

SERIES 51 SEMICONDUCTOR NETWORK RELIABILITY TREND



UNITS TESTED - DEVICE HOURS SUMMARY

Year	Quarter	Number of Units Tested	Number Failed	Actual Device Hours (000)	Equivalent 85°C Device Hours (000)
1962	First Second Third Fourth	200 55 50 158	5 1 1 2	275 85 95.5 368	743 230 258 994
1963	First Second Third Fourth	219 160 76 204*	3 2 0 0	239 317.5 152 358	1217 1618 948 967
1964	First Second Third Fourth	240*	0	183	1087

*Tests in progress

Figure 1

To convert failure rates at one temperature to 85°C, divide the failure rate by the appropriate factor, or alternately, multiply the hours accumulated by the same factor. Where no failures occurred, it was not possible to divide the number of failures by test hours to obtain failure rate. In these cases, the 50% confidence level point was used. In general this is slightly more conservative than the failures divided by hours method.

Due to the fact that tests in the fourth quarter of 1963 and the first quarter quarter of 1964 are still underway, parameter plots for fourth quarter, on subsequent pages, are done only on devices completing 12 weeks of testing.

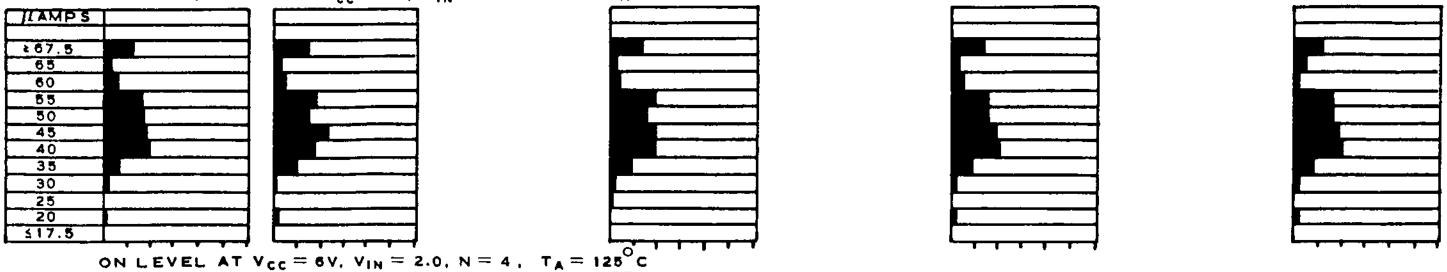
Test Failures

Condition	Production Date	Discussion	Corrective Action
Operating at 125°C	1/5/63	Unit not bistable. Surface leakage, suspect inversion layer.	Implementation of welded package has eliminated solder flux. Improved clean up technique. Improved heat treating after aluminum evaporation. Added 200°C post can bake.
	1/12/63	Input current degradation. Surface leakage caused by either contamination or inversion layer.	Same as above.
	4/13/63	Unit not bistable, input current degradation. Contamination caused input resistor degradation.	Same as above.
	2/2/63	Open. Aluminum oxide formation. Bonds mechanically but not electrically sound.	Have not been able to reproduce or explain this mechanism. There have been no recurrences.
Storage at 200°C	4/13/63	Open pins. Formation of Au-Al compound caused open bonds.	Added 200°C post can bake. Installed hot tip bonding capillaries for positive temperature control. Studies currently underway to eliminate Au-Al interface by use of new lead pattern material.

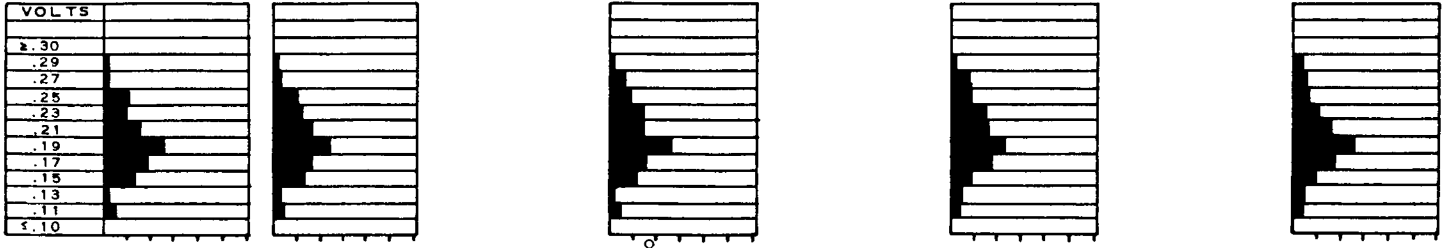
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
OPERATING LIFE @+125°C, V_{CC} = 6	SN511	63

INITIAL DISTRIBUTION		PARAMETER BEHAVIOR ANALYSIS						
INTERVALS		1 WEEK		3 WEEKS		6 WEEKS		12 WEEKS

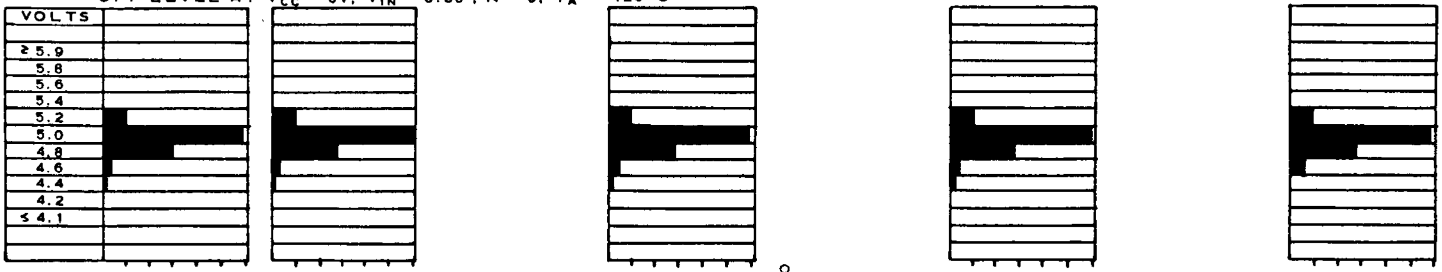
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



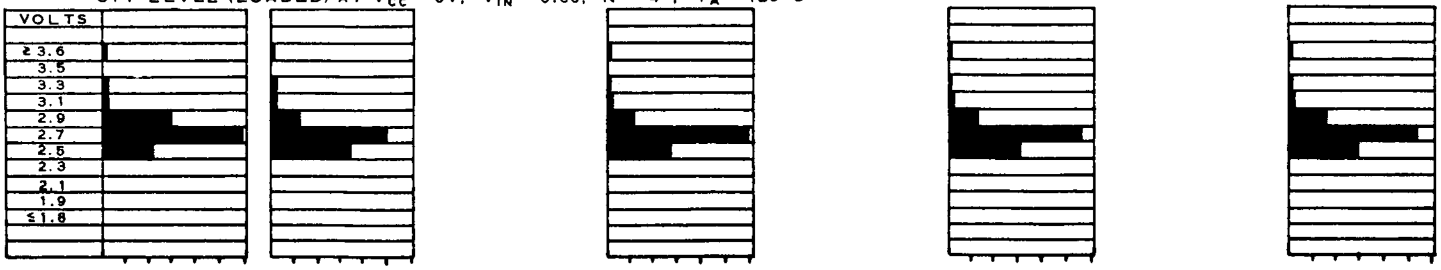
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 4, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



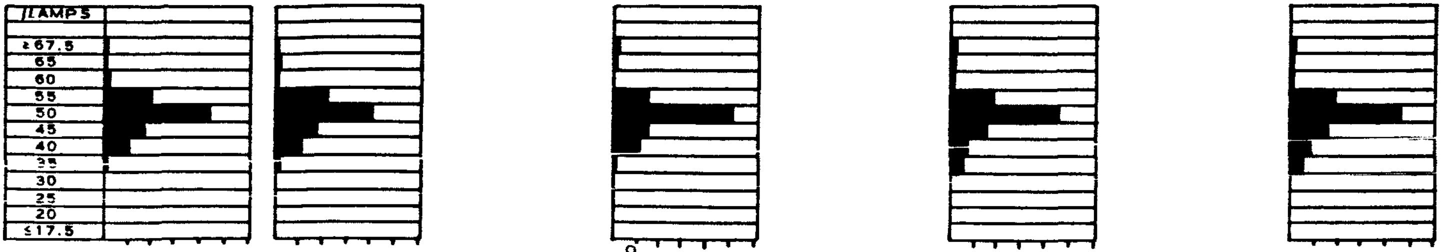
OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 4, T_A = 125°C



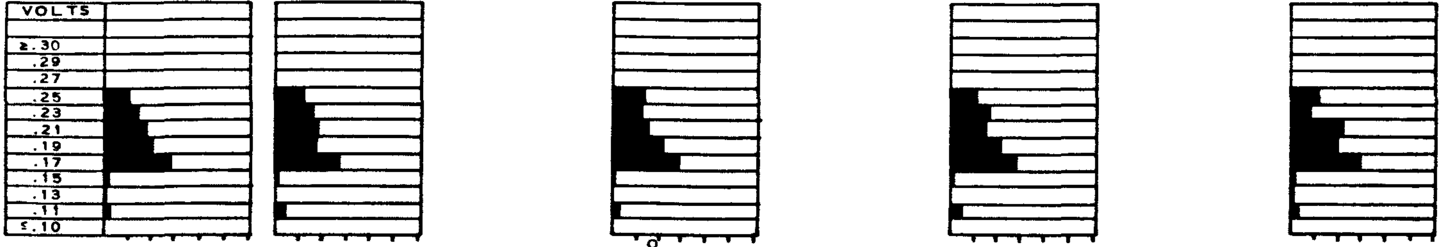
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
OPERATING LIFE @ +125°C, $V_{CC} = 6$	SN513	25

INITIAL DISTRIBUTION		PARAMETER BEHAVIOR ANALYSIS						
INTERVALS		1 WEEK		3 WEEKS		6 WEEKS		12 WEEKS

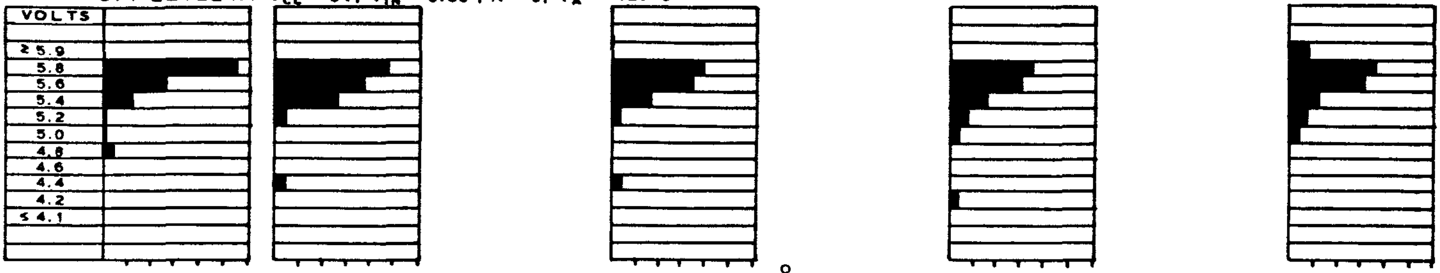
INPUT CURRENT AT $V_{CC} = 6V$, $V_{IN} = 2.0$ N = 0, $T_A = 125°C$



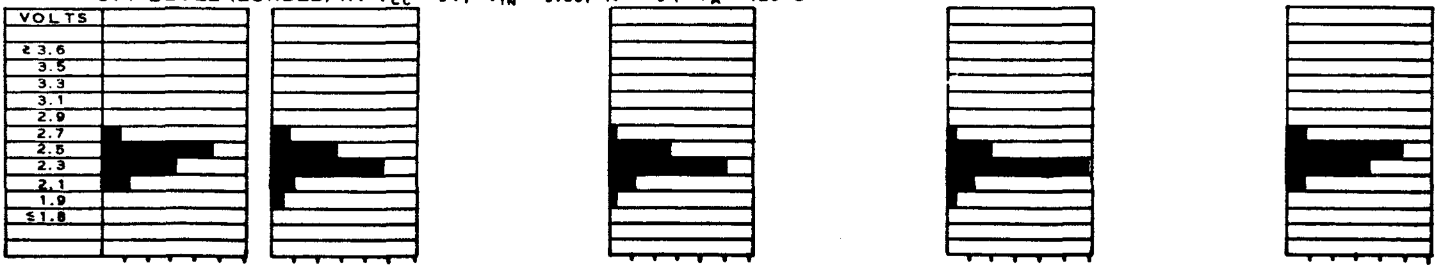
ON LEVEL AT $V_{CC} = 6V$, $V_{IN} = 2.0$, N = 0, $T_A = 125°C$



OFF LEVEL AT $V_{CC} = 6V$, $V_{IN} = 0.30$, N = 0, $T_A = 125°C$



OFF LEVEL (LOADED) AT $V_{CC} = 6V$, $V_{IN} = 0.30$, N = 5, $T_A = 125°C$



C. FIELD DATA REVIEW

Actual use condition testing performed by networks consumers offers the potential of many hours of test data. Applications of 7116 networks have accumulated 5,643,492 hours of test data.

These applications are typically shift registers, computers, and counters operating near 25°C. A failure is considered to be observed when the equipment ceases functional operation due to a network failure. Failures which occur due to mechanical stressing in system checkout are not considered as life or operating failures. In the hours accumulated one failure has occurred. This failure was due to difficulties with the solder seal on the old Series 51 device. Implementation of the welded package eliminates this mechanism.

One failure out of 5,643,492 hours gives a failure rate estimate of 0.018%/1000 hours, with 60% confidence this proves a use condition failure rate of 0.032%/1000 hours.

The curve in Fig. 2 indicates the 0.032% graphically, along with 90% and 95% confidence limits.

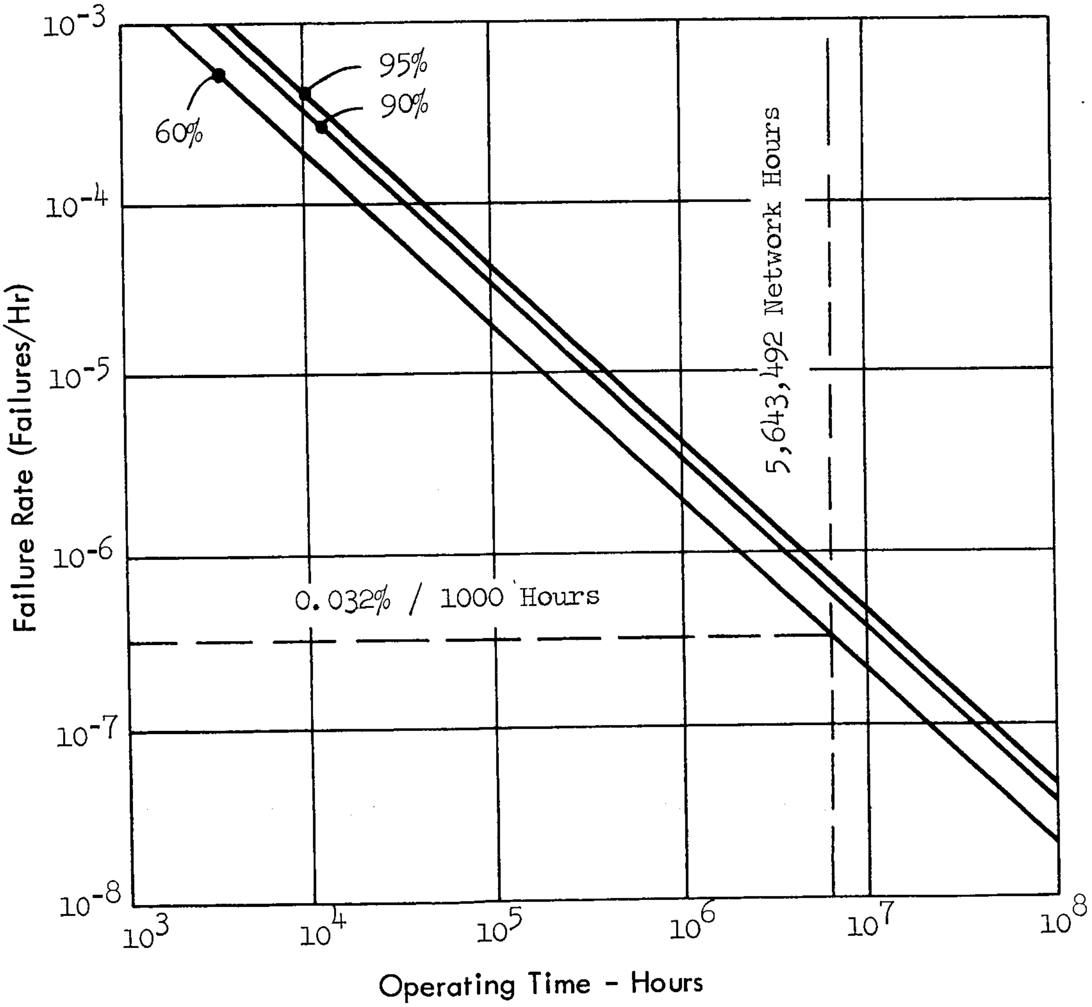


Fig. 2. Upper Confidence Limits - Operational Field Application Data

D. STEP STRESS TESTS

Temperature step stress testing is performed to indicate product capability and to confirm process improvements. However, as a product's capability improves, this indicator becomes less sensitive since very few failures are observed up to temperatures that induce total failure. Consequently, testing during 1963 was limited to the amount necessary to show no degradation from previous levels had occurred.

The applicability and use of operating step stress is being investigated to determine if its use will give a more sensitive indicator of product capability.

Test Methods

Networks are measured on failure indicative parameters initially. The first level of stress (temperature or operating power) is then applied for a specified step length — generally four to twenty four hours. Parameters are measured after this stress, and the same units are stressed to the next higher step level. This sequence of testing continues to predetermine percent failure. Failures are removed after the level where failure is indicated.

Summary

Step stressing shows product capability far in excess of normal storage temperature levels. Repetition of the same tests over a period in time shows that process improvements have been effective in extending the temperature capability and reducing percent failure under extreme temperature stresses.

Test Results

Figure 3 shows the curve of percent failures versus temperature for tests performed in 1962 and 1963. Because the major failure mode uncovered was open ball bonds, specific emphasis was placed on developing new contact materials by the Integrated Circuits Department. These materials are being incorporated into the construction of extensively tested and evaluated samples which are being used in the reliability investigations in progress.

The results of the most recent test are shown on page 23. It is significant to note that these networks show capability in excess of 377°C, the silicon-gold eutectic point. This was not previously the case. Even higher temperature capabilities are contemplated for the new lead pattern material.

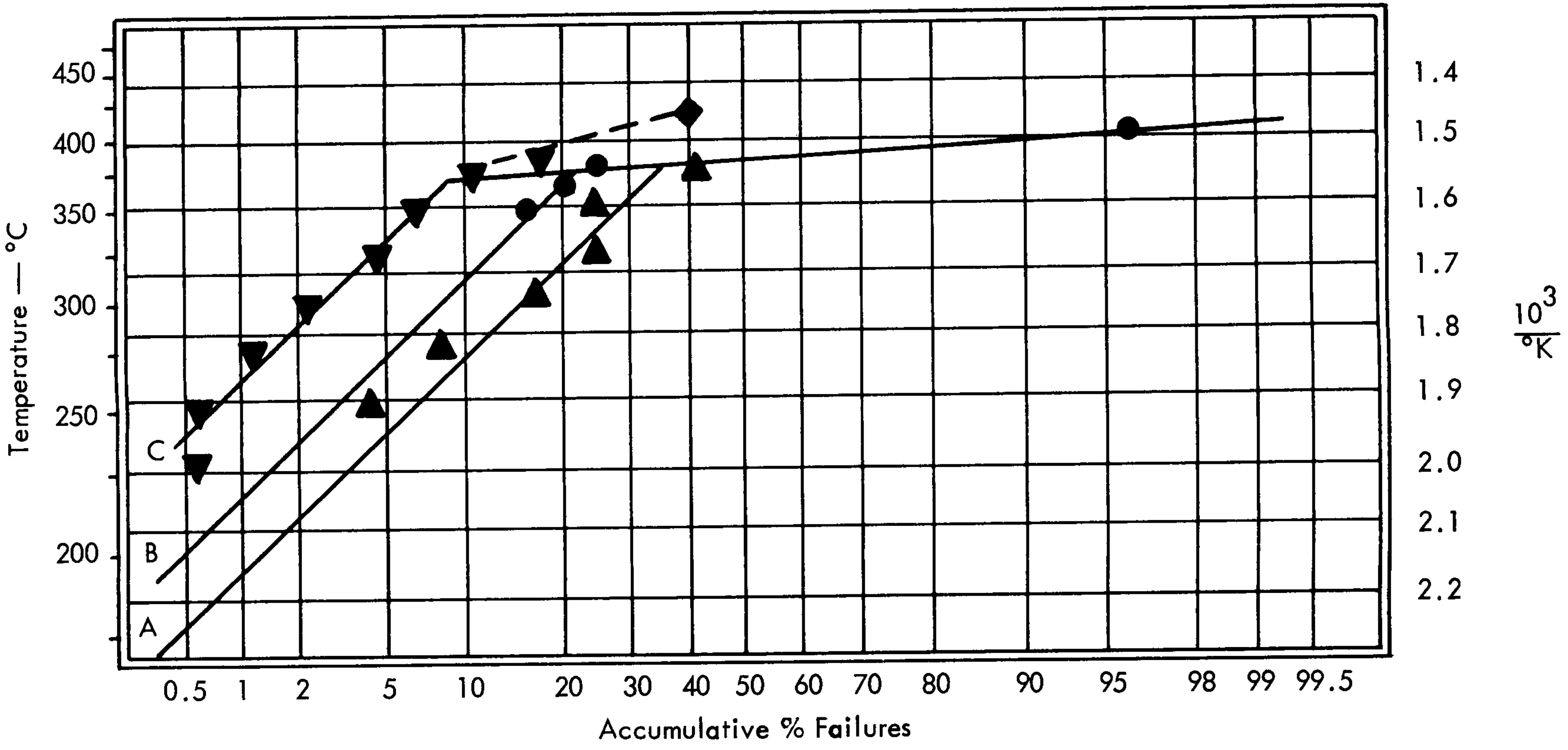
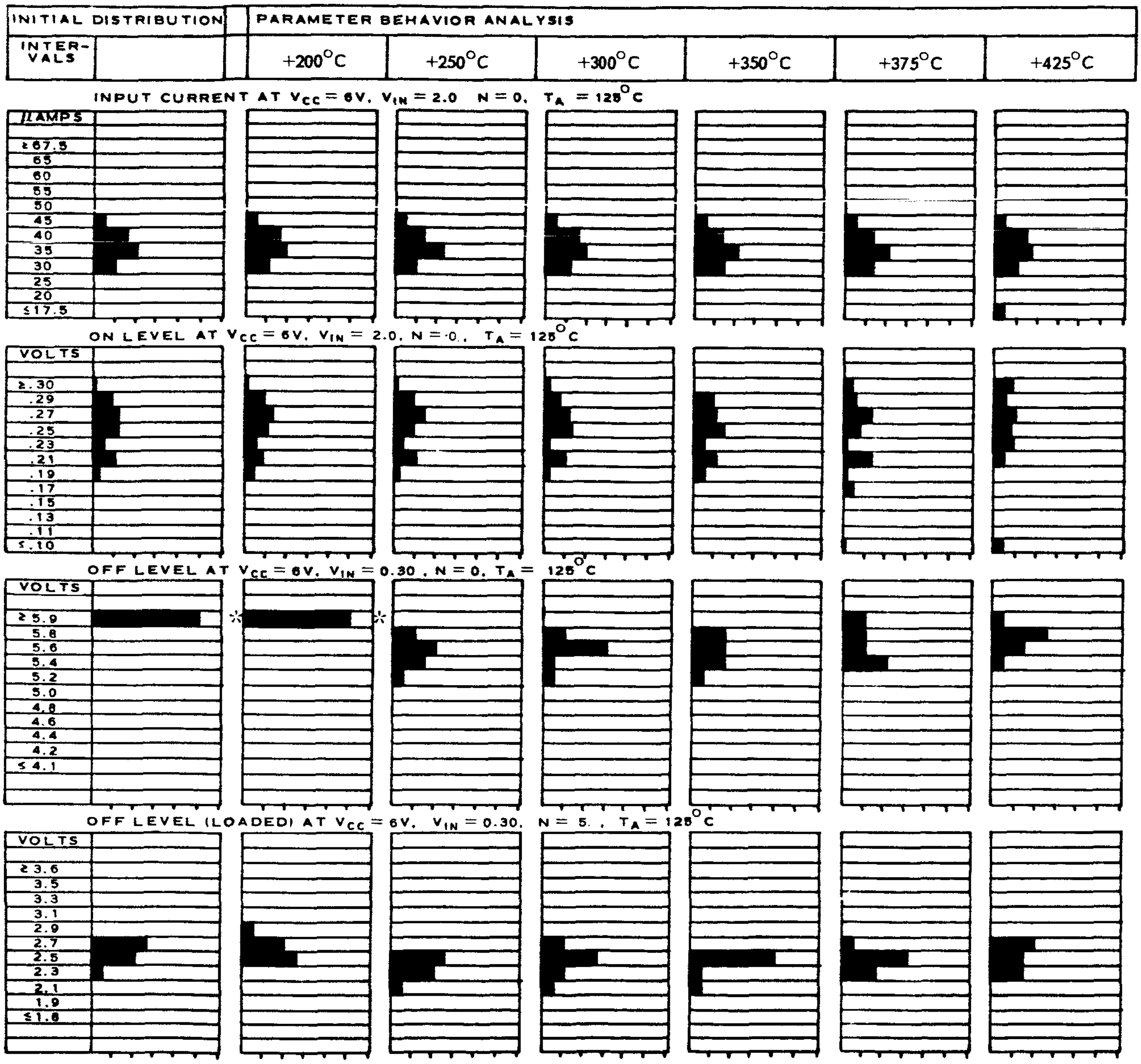


Fig. 3. Semiconductor Networks Step Stress Test Results

TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
TEMPERATURE STEP STRESS, 4 HOURS	SN513	10



* The shift in Voff readings after the first two levels of stress was due to improper readings initially and after the 200°C step.

E. ENVIRONMENTAL TESTS

Test Program

Environmental tests are performed to demonstrate the ability of the semiconductor networks to withstand mechanical and physical stresses. The results illustrate compliance with existing environmental requirements of Mil-S-19500. The tests were then extended to even higher levels to demonstrate the ability to withstand even higher stress conditions.

Test Results

Figure 4 summarizes the tests run and the failures found in tests performed in 1962 and 1963. Failure modes are indicated and corrective action noted. Subsequent pages report detail results of each test performed including the initial and post test parameter behavior patterns. Tests performed on over 600 networks prove capability in excess of standard military testing levels.

It should be pointed out that the failures at 20,000 G and 35,000 G occurred in 1962. Since the date of those failures, 45 units have been tested at 20,000 G with no additional failures, indicating that the implemented corrective action steps have been effective.

Fig. 4. Series 51 — Semiconductor Networks Environmental Evaluation

TEST	NUMBER TESTED	CONDITIONS	FAIL	CODE
Thermal Shock	50*	5 Cycles -0°C to +100°C	0	
	30	45 Cycles	0	
	30	135 Cycles	1	1
	9	270 Cycles	0	
Temperature Cycling	73*	5 Cycles -55°C to +125°C	0	
	40	45 Cycles	0	
	40	135 Cycles	0	
	20	160 Cycles	0	
Shock	93*	1,500 G, 0.5MS, Total 20 Blows 4 Planes	0	
	40	2,000 G	0	
	70	3,000 G	0	
	40	3,500 G, 0.2MS	0	
Vibration Variable Frequency	103*	20 G, 100-2000CPS, 3 Planes	0	
	50	30 G	1	2
	40	40 G	0	
	50	50 G	0	
Vibration Fatigue	50*	20 G, 60 CPS, 96 Hours	0	
	50	30 G 9 Hours	0	
	40	40 G 9 Hours	0	
	40	50 G 9 Hours	0	
Constant Acceleration	108*	20,000 G	1	3
	32	35,000 G	1	4
	124	40,000 G (98 Y1 Plane Only)	3	3,4
	24	45,000 G	1	5
	28	50,000 G	1	4
Moisture Resistance	20*	10 Cycles	0	
	10	20 Cycles	0	
	20	30 Cycles	1	6
	9	40 Cycles	1	6
	8	50 Cycles	1	6
Salt Atmosphere	30*	24 Hours, 5% Solution	0	
	10	48 Hours	0	

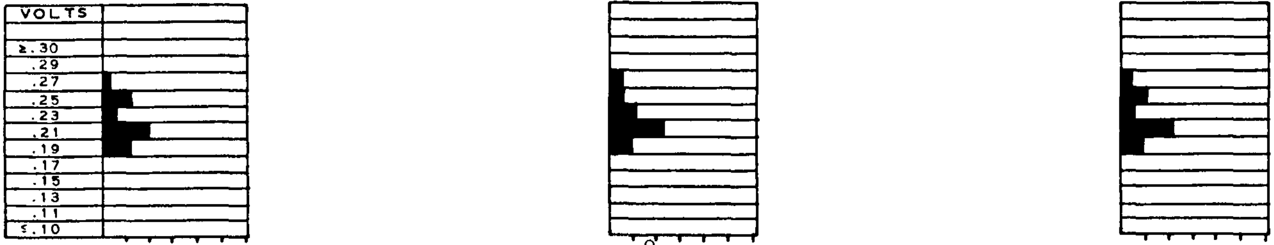
* Tests at MIL-S-19500 Level

CODE	FAILURE MODE	SUBSEQUENT PROCESS CHANGES
1	Degradation Failure	Eliminated Solder Flux by Going to Welded Package
2	Open Bond	Added QRA Bonding Controls, Expanded Contacts Hot Tip Bonder and Insulated Base Plate
3	Broken Bar	Increased Bar Thickness, Changed Mounting Glass & Improved Operator Procedure by X-ray Monitor
4	Package or Lead Failure	Test Fixture Caused Problems — Fixture Redesigned New Welded Package Is More Rigid
5	Degradation Input Current	High Temperature Slice Bake, Installed 100% 48-Hour 200°C Bake and 10 Cycles of Temperature Cycling (-55°C to +150°C), Added Welded Package
6	Lead Failure	Current Welded Package Results Indicate Improvement on Salt Atmosphere and Moisture Resistance

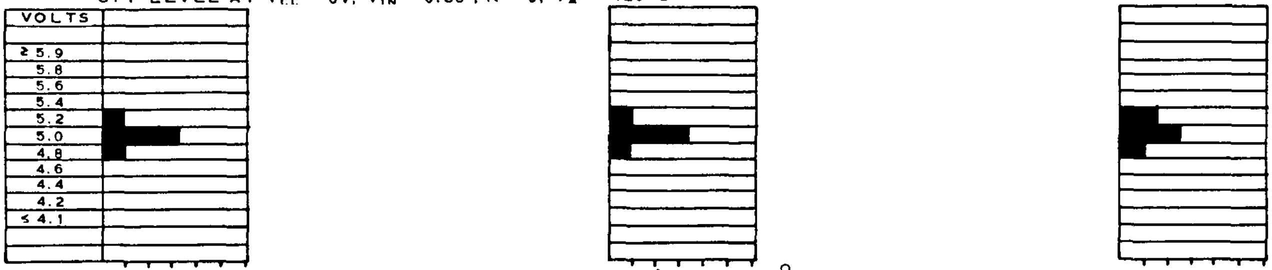
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
THERMAL SHOCK, +100°C to 0°C	SN515	10

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTER-VALS					5 Cycles			45 Cycles

ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 0, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 4, T_A = 125°C

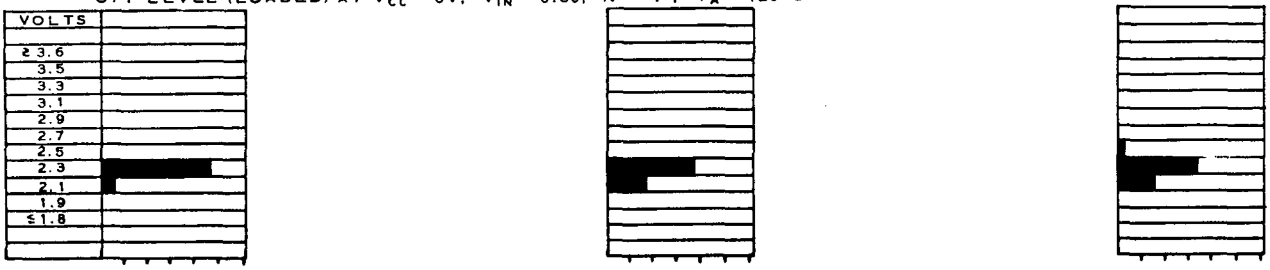


Fig. 4. Series 51 — Semiconductor Networks Environmental Evaluation

TEST	NUMBER TESTED	CONDITIONS	FAIL	CODE
Thermal Shock	50*	5 Cycles -0°C to +100°C	0	
	30	45 Cycles	0	
	30	135 Cycles	1	1
	9	270 Cycles	0	
Temperature Cycling	73*	5 Cycles -55°C to +125°C	0	
	40	45 Cycles	0	
	40	135 Cycles	0	
	20	160 Cycles	0	
Shock	93*	1,500 G, 0.5MS, Total 20 Blows 4 Planes	0	
	40	2,000 G	0	
	70	3,000 G	0	
	40	3,500 G, 0.2MS	0	
Vibration Variable Frequency	103*	20 G, 100-2000CPS, 3 Planes	0	
	50	30 G	1	2
	40	40 G	0	
	50	50 G	0	
Vibration Fatigue	50*	20 G, 60 CPS, 96 Hours	0	
	50	30 G 9 Hours	0	
	40	40 G 9 Hours	0	
	40	50 G 9 Hours	0	
Constant Acceleration	108*	20,000 G	1	3
	32	35,000 G	1	4
	124	40,000 G (98 Y1 Plane Only)	3	3,4
	24	45,000 G	1	5
	28	50,000 G	1	4
Moisture Resistance	20*	10 Cycles	0	
	10	20 Cycles	0	
	20	30 Cycles	1	6
	9	40 Cycles	1	6
	8	50 Cycles	1	6
Salt Atmosphere	30*	24 Hours, 5% Solution	0	
	10	48 Hours	0	

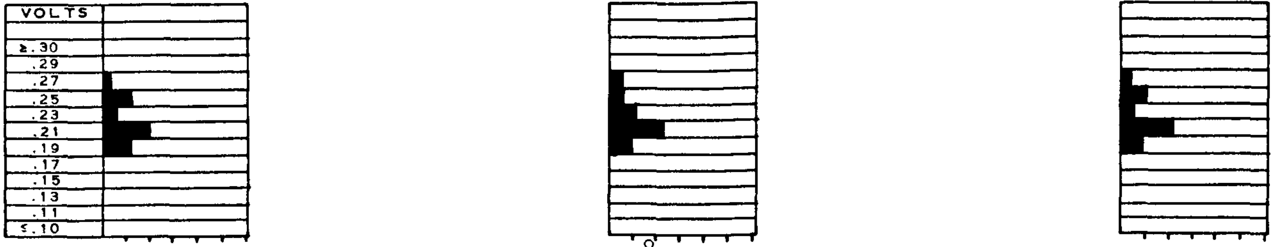
* Tests at MIL-S-19500 Level

CODE	FAILURE MODE	SUBSEQUENT PROCESS CHANGES
1	Degradation Failure	Eliminated Solder Flux by Going to Welded Package
2	Open Bond	Added QRA Bonding Controls, Expanded Contacts Hot Tip Bonder and Insulated Base Plate
3	Broken Bar	Increased Bar Thickness, Changed Mounting Glass & Improved Operator Procedure by X-ray Monitor
4	Package or Lead Failure	Test Fixture Caused Problems — Fixture Redesigned New Welded Package Is More Rigid
5	Degradation Input Current	High Temperature Slice Bake, Installed 100% 48-Hour 200°C Bake and 10 Cycles of Temperature Cycling (-55°C to +150°C), Added Welded Package
6	Lead Failure	Current Welded Package Results Indicate Improvement on Salt Atmosphere and Moisture Resistance

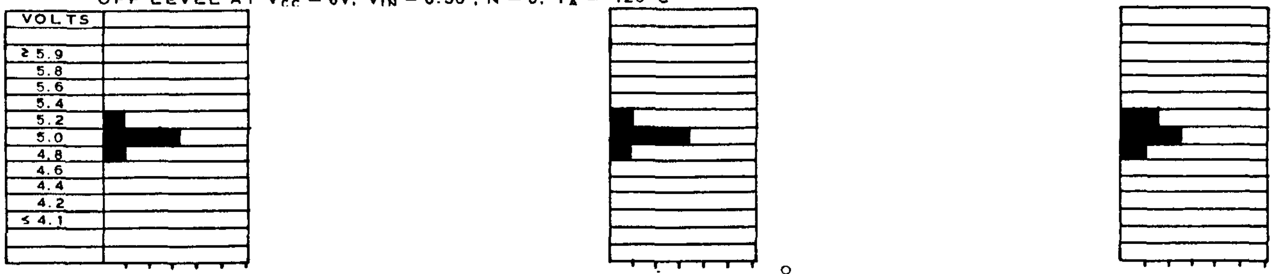
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
THERMAL SHOCK, +100°C to 0°C	SN515	10

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTERVALS					5 Cycles			45 Cycles

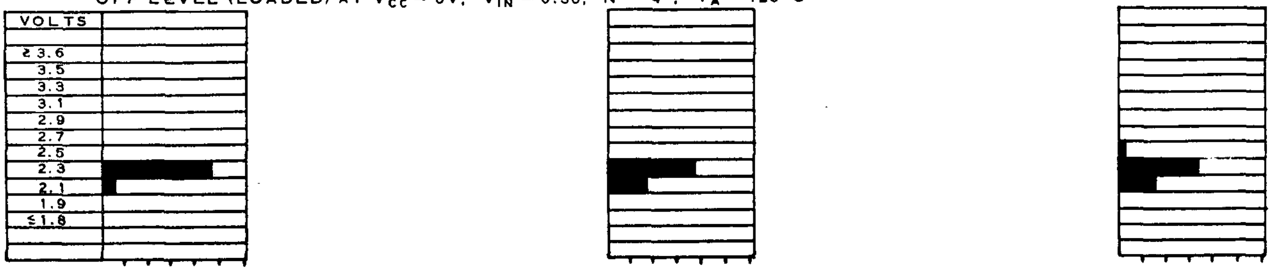
ON LEVEL AT $V_{CC} = 6V$, $V_{IN} = 2.0$, N = 0, $T_A = 125°C$



OFF LEVEL AT $V_{CC} = 6V$, $V_{IN} = 0.30$, N = 0, $T_A = 125°C$



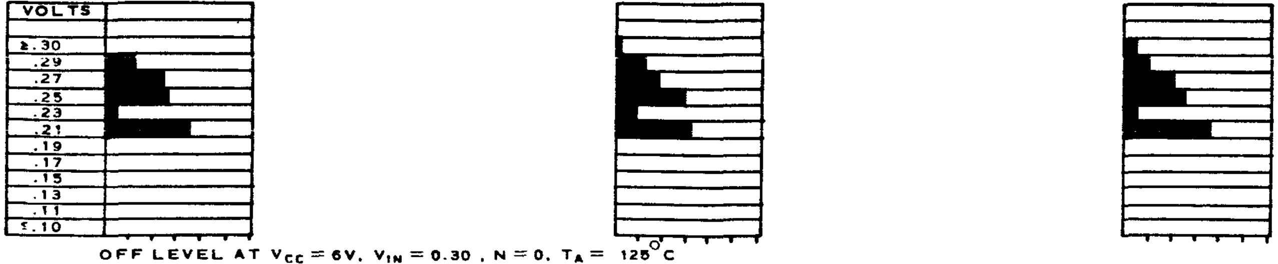
OFF LEVEL (LOADED) AT $V_{CC} = 6V$, $V_{IN} = 0.30$, N = 4, $T_A = 125°C$



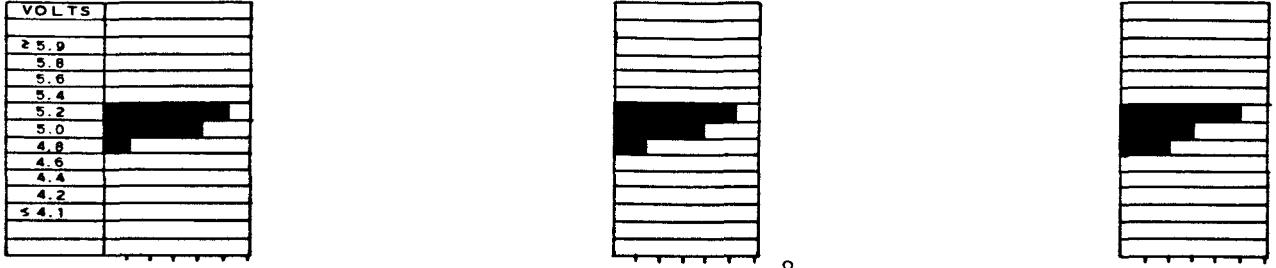
TEST PERFORMED: TEMPERATURE CYCLING, +125°C to -55°C	TYPE TESTED SN515	SAMPLE SIZE 10

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTER-VALS					5 Cycles			45 Cycles

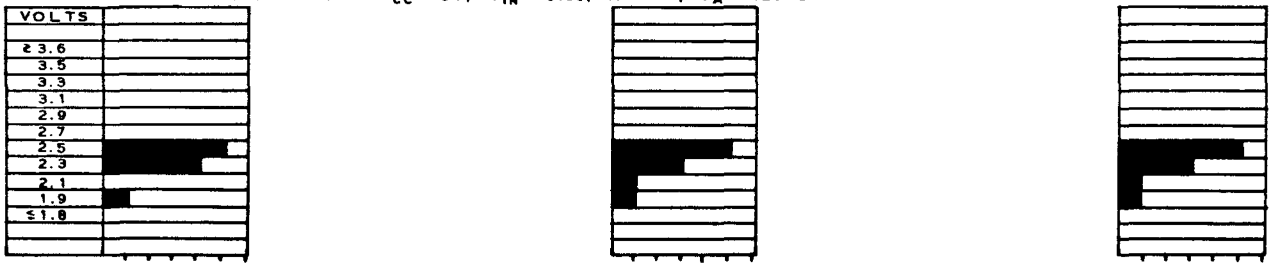
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 0, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



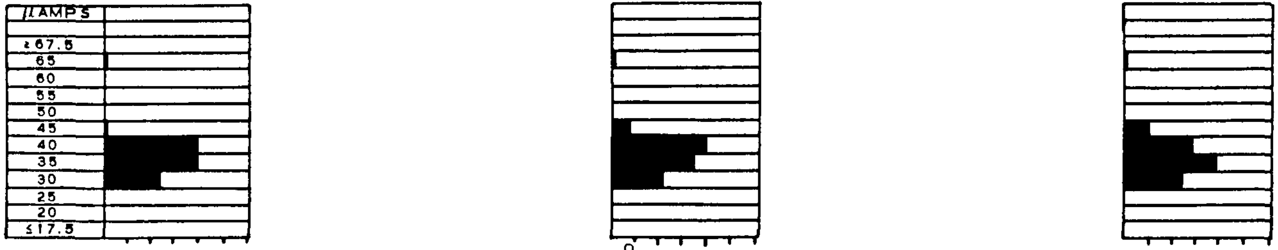
OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 4, T_A = 125°C



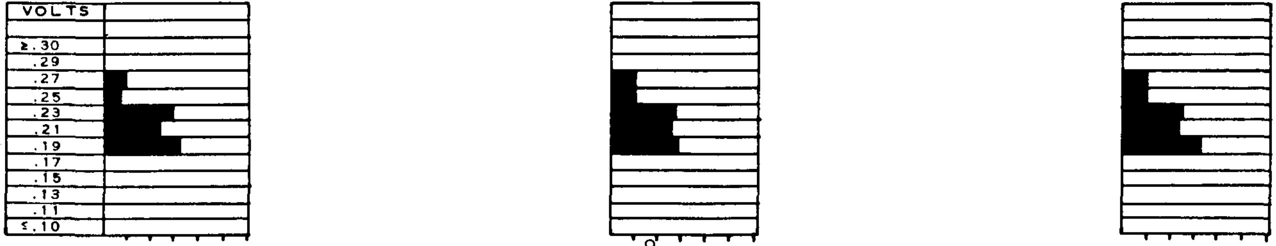
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
SHOCK, 0.5 msec duration	SN514	10

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTER-VALS					1500 G			3000 G

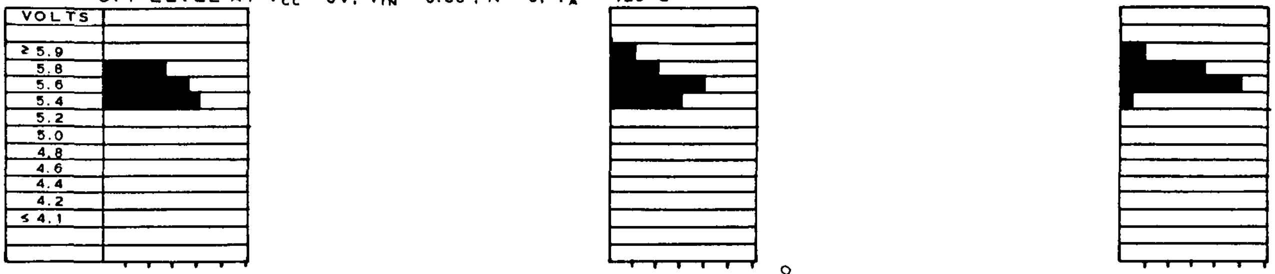
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



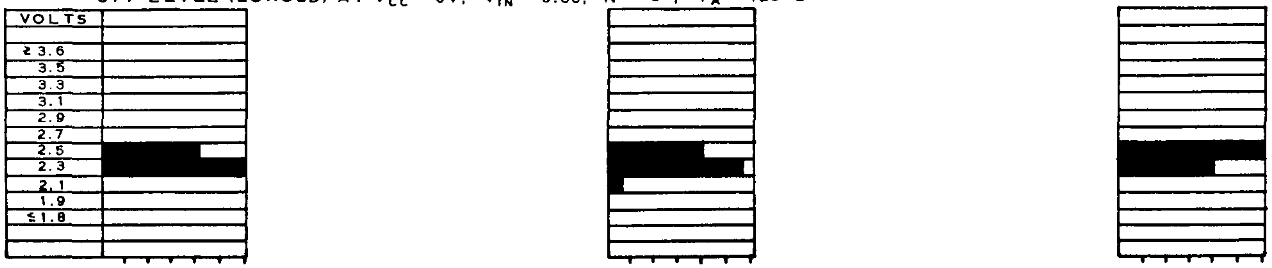
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 0, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



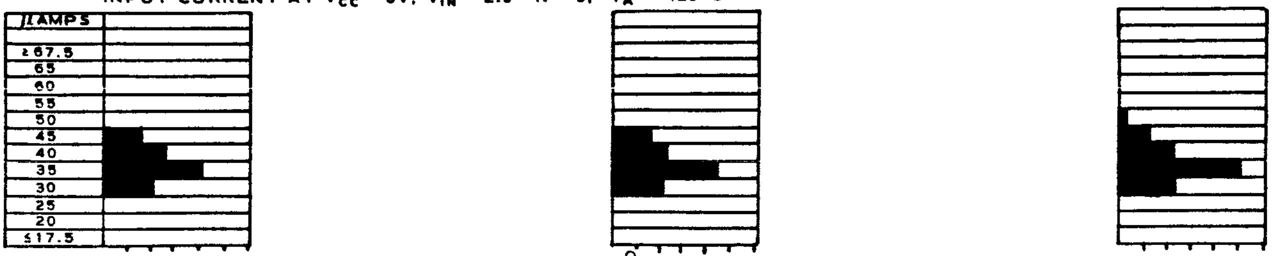
OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 5, T_A = 125°C



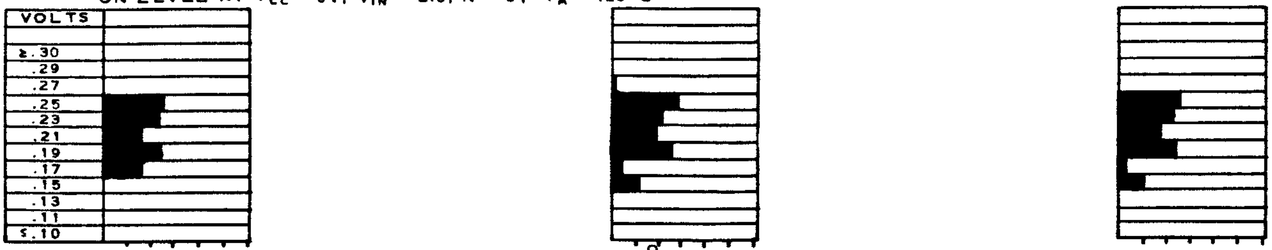
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
VARIABLE FREQUENCY VIBRATION, 100 to 2000 cps	SN514	10

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTER-VALS					20 G			30 G

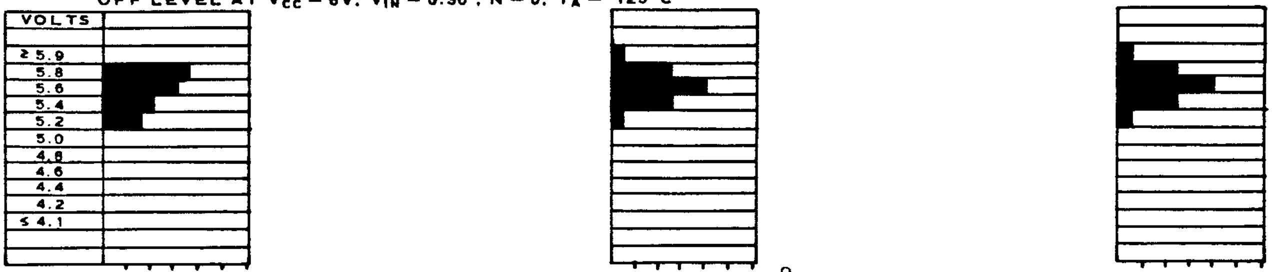
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



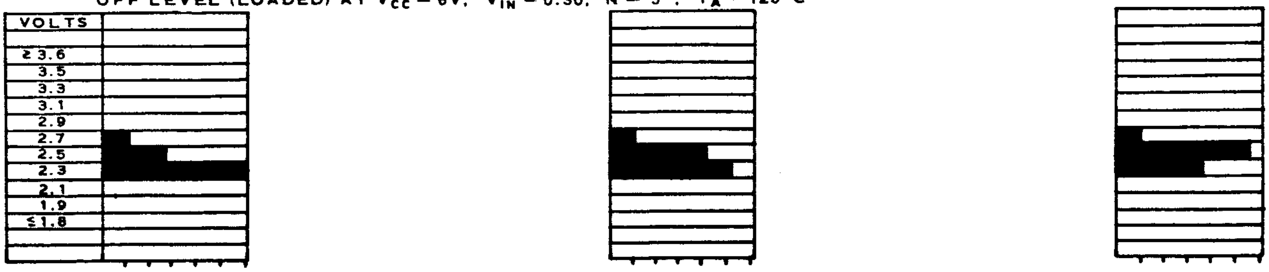
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 0, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



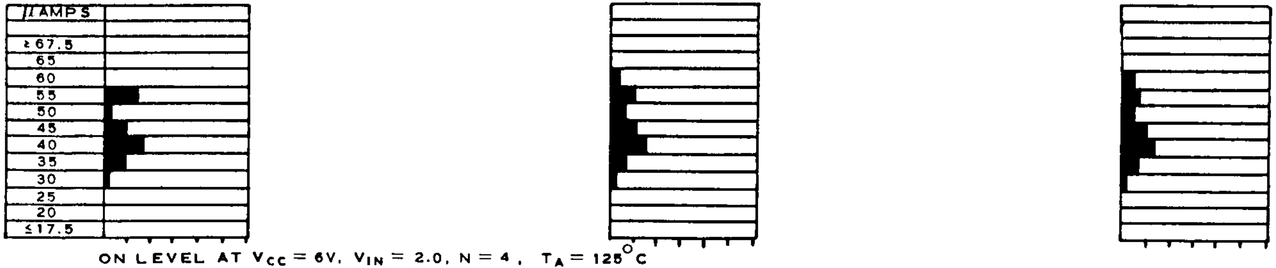
OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 5, T_A = 125°C



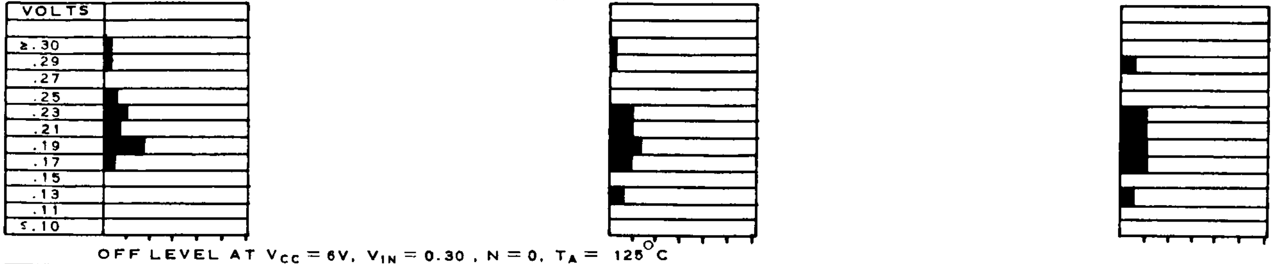
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
VIBRATION FATIGUE, 96 hours at 60 cps	SN511	10

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTER-VALS					20 G			30 G

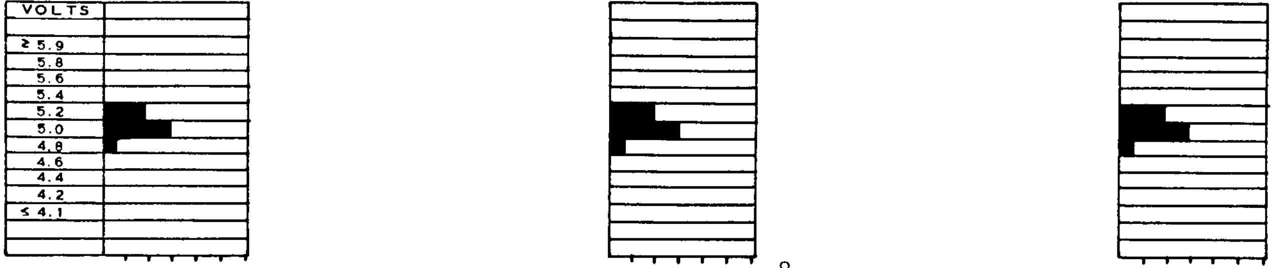
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



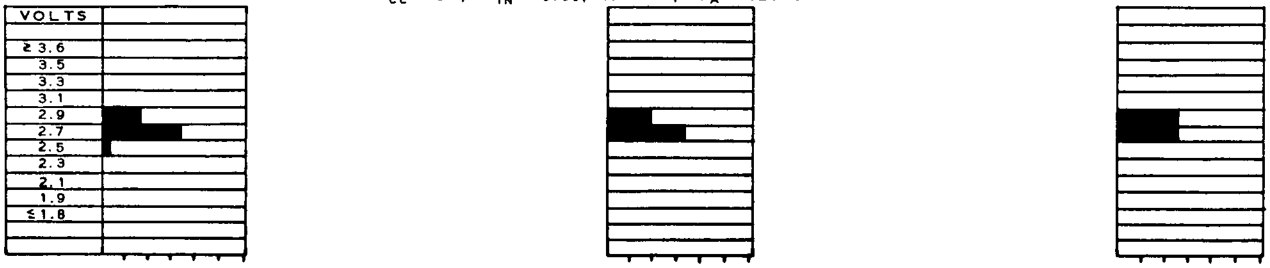
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 4, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



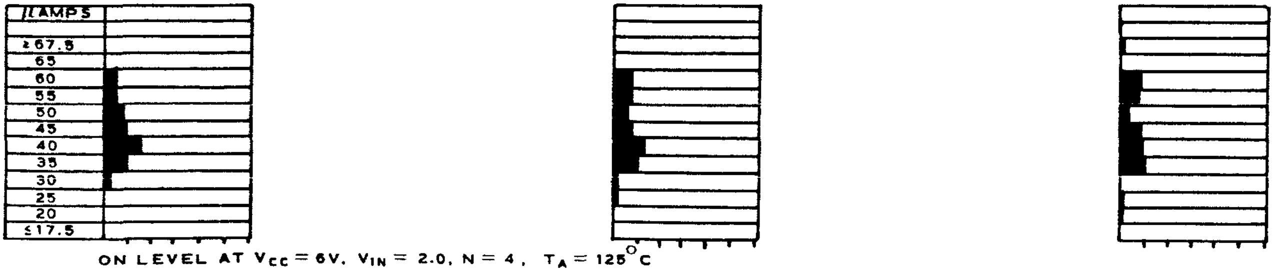
OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 4, T_A = 125°C



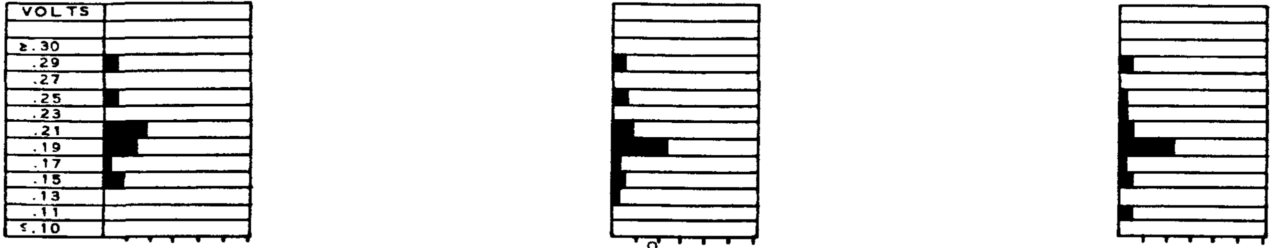
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
CONSTANT ACCELERATION (CENTRIFUGE)	SN511	10

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTER-VALS					20,000 G			35,000 G

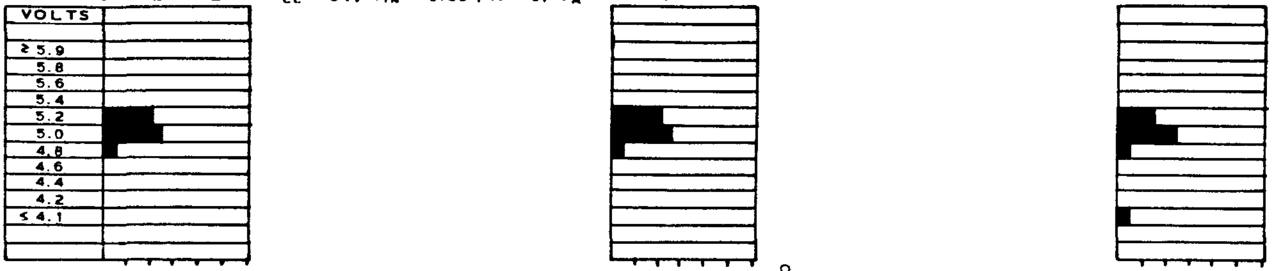
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



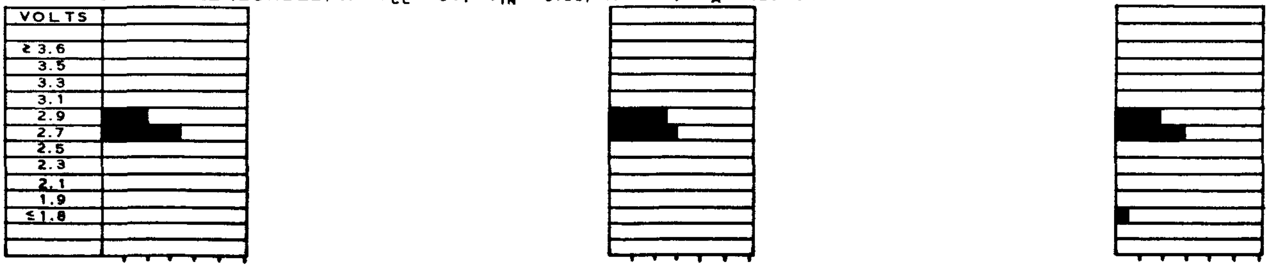
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 4, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 4, T_A = 125°C

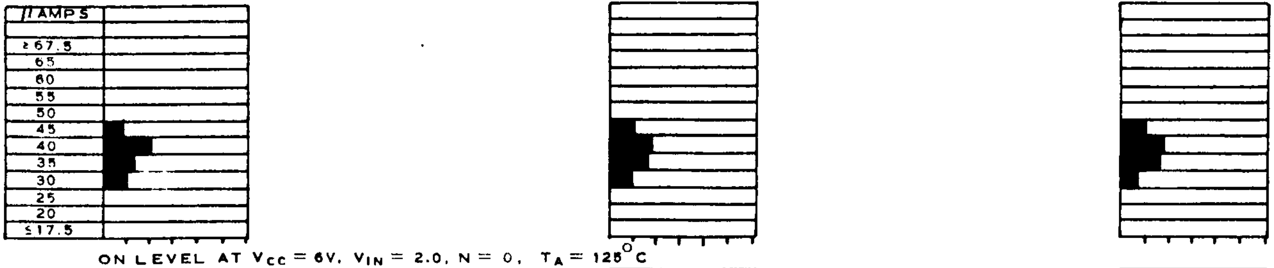


One failure occurred after 35,000 G testing.

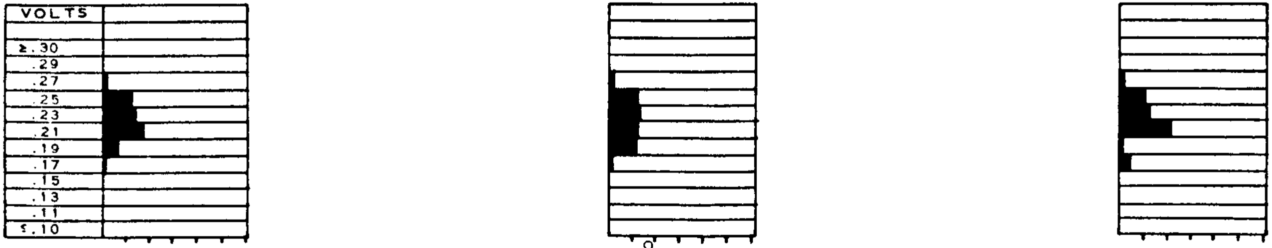
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
MOISTURE RESISTANCE (1 day per cycle)	SN513	10

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTER-VALS					10 Cycles			30 Cycles

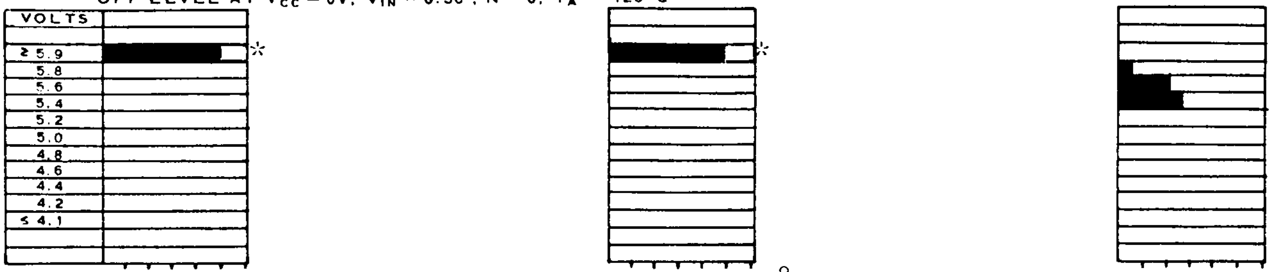
INPUT CURRENT AT $V_{CC} = 6V$, $V_{IN} = 2.0$ N = 0, $T_A = 125°C$



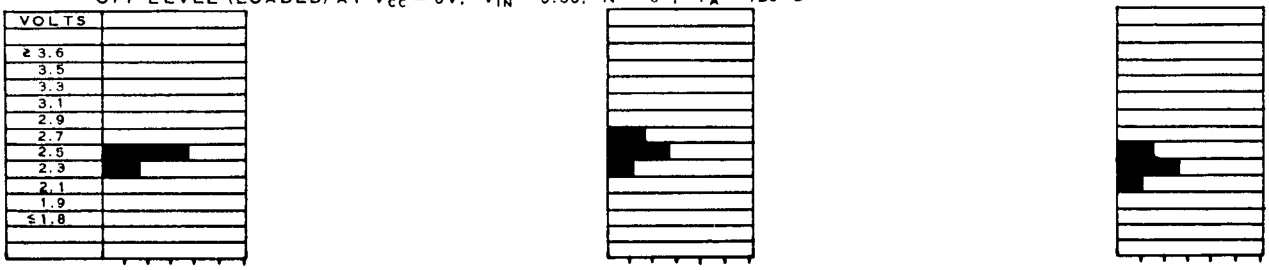
ON LEVEL AT $V_{CC} = 6V$, $V_{IN} = 2.0$, N = 0, $T_A = 125°C$



OFF LEVEL AT $V_{CC} = 6V$, $V_{IN} = 0.30$, N = 0, $T_A = 125°C$



OFF LEVEL (LOADED) AT $V_{CC} = 6V$, $V_{IN} = 0.30$, N = 5, $T_A = 125°C$

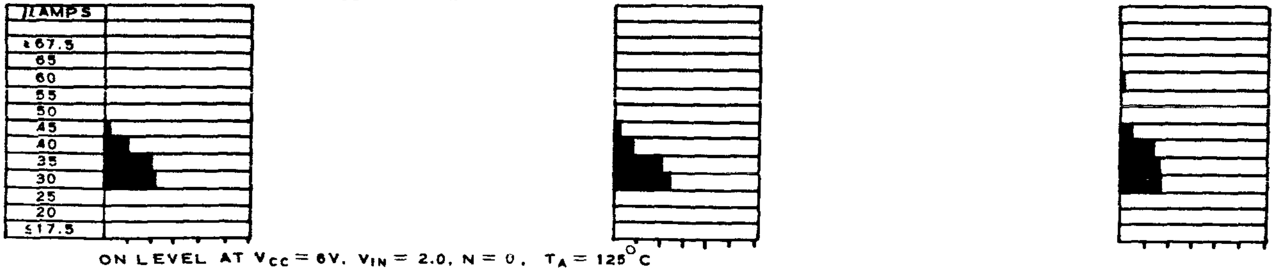


* The shift in Voff after 30 cycles of moisture resistance was due to improper reading of initial and post 10 cycle Voff parameters.

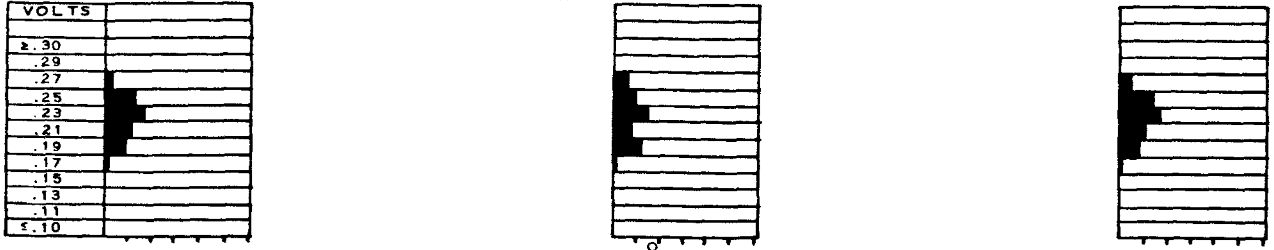
TEST PERFORMED:	TYPE TESTED	SAMPLE SIZE
SALT ATMOSPHERE	SN513	10

INITIAL DISTRIBUTION			PARAMETER BEHAVIOR ANALYSIS					
INTER-VALS					24 Hours			48 Hours

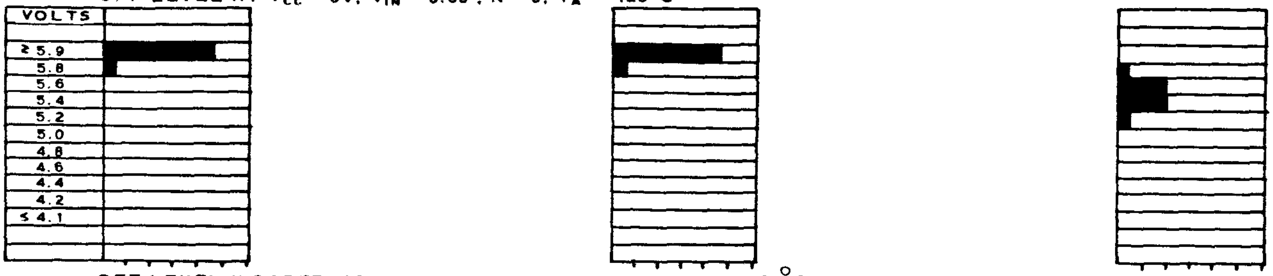
INPUT CURRENT AT V_{CC} = 6V, V_{IN} = 2.0 N = 0, T_A = 125°C



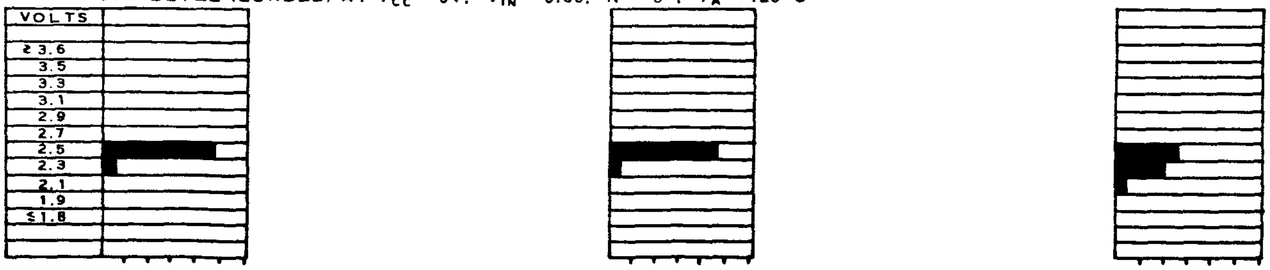
ON LEVEL AT V_{CC} = 6V, V_{IN} = 2.0, N = 0, T_A = 125°C



OFF LEVEL AT V_{CC} = 6V, V_{IN} = 0.30, N = 0, T_A = 125°C



OFF LEVEL (LOADED) AT V_{CC} = 6V, V_{IN} = 0.30, N = 5, T_A = 125°C



F. FAILURE ANALYSIS

The Quality Assurance department performs an analysis on the failures experienced in the test programs described. Through centralization of this activity, two advantages are obtained: (1) Cross pollination of techniques from analysis of other semiconductor device failures. (2) The ability to run a more efficient, better equipped activity on a large scale basis. The failure analysis activity contains over 55 pieces of equipment which are used in analysis. The equipment includes a complete photographic layout, a chlorine etch apparatus for evaluation of oxide surface porosity, a complete metallurgical capability which utilizes a high resolution metalograph and microsection equipment, and an electrical probe capability which allows complete voltage probing under a variety of circuit bias conditions. The flow diagram in Fig. 5 shows the procedures and equipment used in performing failure analysis on semiconductor networks. Results of analyses performed are constantly fed back to product department personnel responsible for process corrective action.

The major reason for failure analysis is to uncover failure mechanisms and develop information to make corrective action possible. There is another reason for failure analysis which becomes more important in highly accelerated testing. This is the discovery that the failure mechanism uncovered cannot exist at lower temperatures. A recent example of this typifies this case: device failures exhibiting high leakage on a 200°C storage test were found to be conductive externally. Analysis of 125°C data using non-parametric statistics showed, with 80% confidence, that this mechanism was non-existent at the lower stress levels. Proper failure analysis is also necessary to separate test error — a difficult task on some of the more complex networks.

Results of failure analysis are utilized in process control changes as well as process changes. These process controls are threefold: quality assurance controls, manufacturing controls, and engineering controls. These controls, together with the utilization of quality material — properly specified and inspected, make up the total control system.

Fig. 5. Semiconductor Network Failure Analysis Procedure

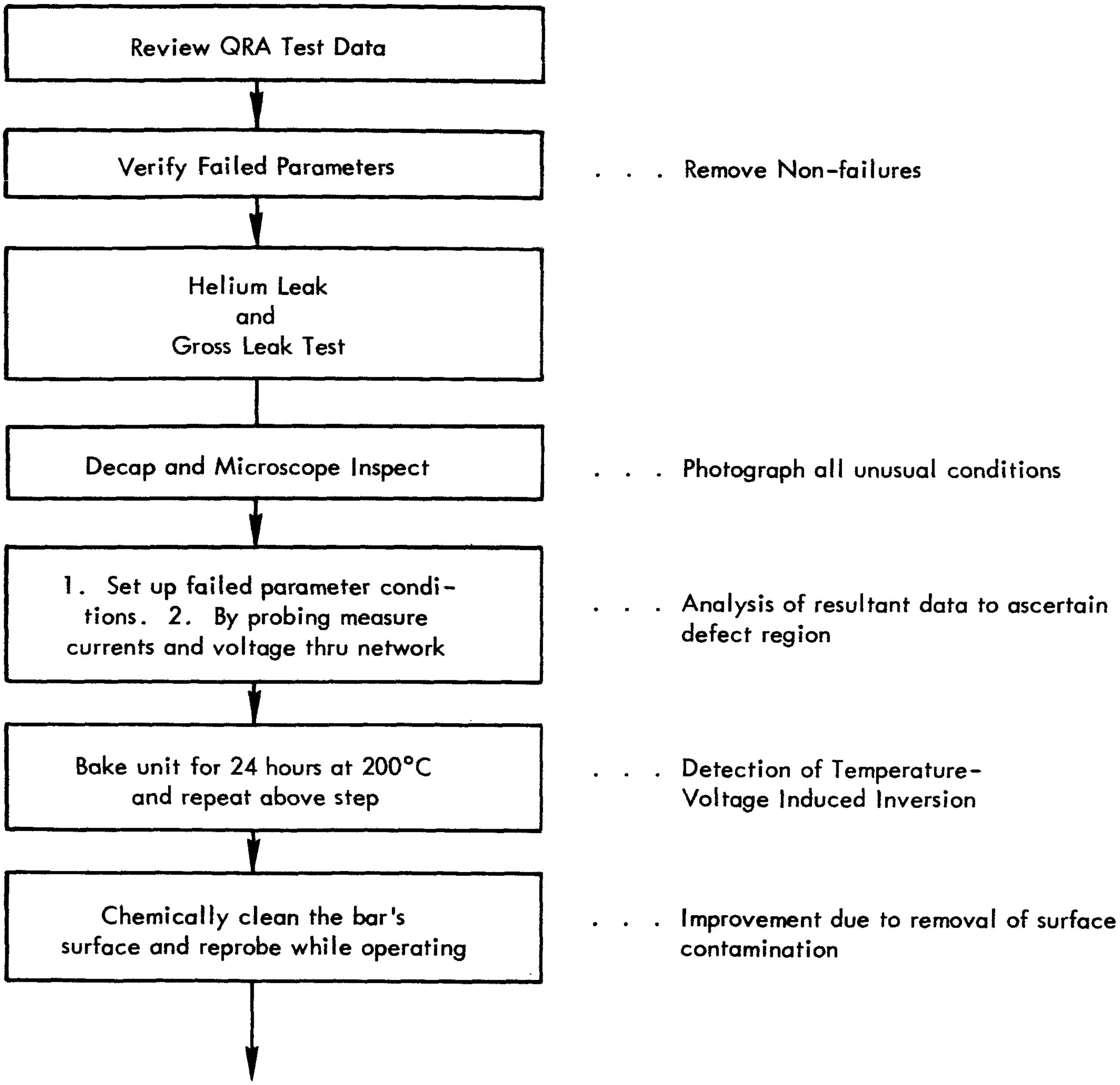
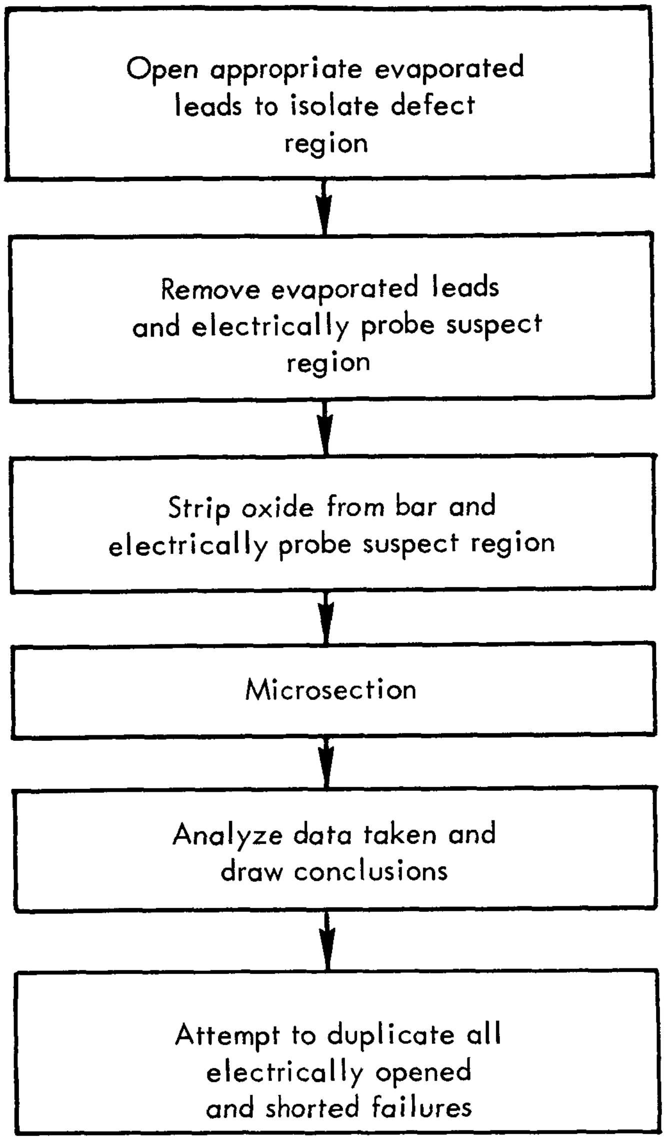


Fig. 5. (Continued)



. . . Improvement of suspect region denotes incorrect region chosen. Bond across opens and recheck

. . . Record electrical characteristics

. . . Record electrical characteristics

. . . Devices are examined for the following:
- Punch Through
- Cracked Bars
- Bonding Problems
- Diffusion Spikes

APPENDIX D

NETWORK APPLICATIONS

NETWORK APPLICATIONS

The applications report for the Series 53 SOLID CIRCUIT semiconductor network is due to be published in July. As soon as copies are available, they will be forwarded to JPL.

APPENDIX E

TEST PROCEDURES

DASH NO.	QTY	NEXT ASSY NO.	SIZE	PROJ NO.
				464

A 514715

REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPROVED

INSPECTION TEST PROCEDURE

PART I

INDIVIDUAL TEST

FOR

INTEGRATED CIRCUIT SEQUENCE GENERATOR

JET PROPULSION LABORATORY

CONTRACT NO. 950693

MANUFACTURER - TEXAS INSTRUMENTS INCORPORATED

TEST DATA SHEET 514722 TO BE FILLED OUT AS PART OF THIS TEST PROCEDURE

QTY REQD -2	QTY REQD -1	ITEM NO.	DWG SIZE	TEXAS INSTRUMENTS PART OR IDENTIFYING NO.	GOVT OR INDUSTRY PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

LIST OF MATERIALS

	DATE
DR bd/ Fred	5/22/64
CKD H. Miller M	5-26-64
ENGR Fred	5/[illegible]/64
APPD W. D. Thomas	5-27-64
DESIGN ACTIVITY RELEASE K. M. McNeil	5-27-64

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

TITLE
TEST PROCEDURE, INSPECTION,
PART I, INDIVIDUAL TEST,
INTEGRATED CIRCUIT SEQUENCE GENERATOR

CODE IDENT NO.	SIZE	DRAWING NO.
96214	A	514715

SCALE	WT	SHEET
		1 of 12

TI-1E1793-A

TABLE OF CONTENTS

		Paragraph No.
1.	TABLE OF TESTS	
1.1	Preparation	3.1
1.2	Room Temperature Test	3.2
1.2.1	Performance Test No. 1	3.2.1
1.2.2	Performance Test No. 2	3.2.2
1.2.3	Performance Test No. 3	3.2.3
1.2.4	Performance Test No. 4	3.2.4
1.3	Low Temperature Test	3.3
1.4	High Temperature Test	3.4
1.5	Vibration Test	3.5
1.6	Final Test	3.6

2. LIST OF TEST EQUIPMENT

2.1 Data Sheet (TI Drawing 514722) shall be completed as part of this test.

2.2 Verify that test equipment designated WORKING STANDARD, or better, is currently certified per TI Standard Procedure No. 12-28.

2.3 Commercial Test Equipment - The following commercially available test equipment (or equivalent) is required to complete the tests required by this specification.

2.3.1 Oscilloscope - Tektronix 543/ Plug-in Type CA

2.3.2 Power Supply, dc, 0-50 VDC, 1.5 amp Sorenson T50-1.5

2.3.3 Pulse Generator, TI Model 6563 (or equivalent)

2.3.4 Temperature Chamber - TI Controlled Environmental Unit

2.3.5 Recorder 18 Channel Visicorder - Honeywell Model 1012

2.4 Special Test Equipment - The following special test equipment is required to complete the test required by this specification.

2.4.1 Control Box, TI Drawing 514713

3.0 TEST PROCEDURES

The following test procedures cover the systems test requirements to evaluate the Integrated Circuit Sequence Generator.

3.1 Preparation

3.1.1 Visually inspect the chassis, modules, printed circuit board, etc. for any mechanical faults such as wiring mistakes, broken leads, open welds, etc. before making any connections to the system.

3.1.2 Adjust V_{cc} supply voltage to 3.1 VDC ± 0.1 VDC.

3.1.3 Adjust pulse generator for a partial going pulse (50 nsec to 500 nsec wide) from 0 to +3V ± 0.1V at a rate of 1mc ± 50KC with rise and fall times at a minimum (minimum ringing at 0 and +3 volts).

Caution: Only a positive going signal is to be applied to this system.

3.1.4 Connect Control Box to recorder as follows:

Function	Test Point	Recorder Channel
A Code	7	1
A Word	19	2
B Code	5	3
B Word	18	4
C Code	9	5
C Word	10	6
D Code	12	7
D Word	20	8
E Code	8	9
E Word	16	10
X Code	6	11
X Word	4	12
CL	2	13
SP	14	14
TR Code	23	15
$\overline{\text{TR}}$ Code	21	16
R Code	13	17
$\overline{\text{R}}$ Code	24	18

3.1.5 Set recorder paper feed to 2 inches/second.

3.1.6 Connect unit to control box.

3.2 Room Temperature Test

3.2.1 Performance Test No. 1

a. Connect Ac pin 22 and Co pin 11 to ground.

b. Observe the code component outputs on the oscilloscope. See Diagram, Section 4 and Table I, Section 5.

   1. A Code
   2. A Word
   3. B Code
   4. B Word
   5. C Code
   6. C Word
   7. D Code
   8. D Word
   9. E Code
   10. E Word
   11. X Code
   12. X Word
   13. CL
   14. S.P.

   Note: The oscilloscope should be triggered on the positive going edge of the specific code's and word detector pulse; i.e., sync on A Word when observing the A Code.

c. Reduce the repetition rate of the pulse generator to 10 cps.

d. Turn on recorder for approximately 10 seconds.

e. Check the recorded waveforms by performing the following manipulations:

   1. Check TR Code for Mode 1 operation.
   2. Check R Code

   Note: See Table II, Section 5 for TR and R Code evaluation.

3.2.2 Performance Test No. 2

a. Connect Ac pin 22 to ground and Co pin 11 to V_{CC}.

b. Repeat 3.2.1.b.

c. Repeat 3.2.1.c.

d. Repeat 3.2.1.d.

e. Check the recorded waveforms by performing the following manipulations:

1. Check TR Code for Mode 1.

2. Check R Code.

3.2.3 Performance Test No. 3

a. Connect Ac pin 22 to V_{cc} and Co pin 11 to ground.

b. Repeat 3.2.1.b.

c. Repeat 3.2.1.c.

d. Repeat 3.2.1.d.

e. Check the recorded waveforms by performing the following manipulations:

1. Check TR Code for Mode 2.

2. Check R Code.

3.2.4 Performance Test No. 4

a. Connect Ac pin 22 and Co pin 11 to V_{cc}.

b. Repeat 3.2.1.b.

c. Repeat 3.2.1.c.

d. Repeat 3.2.1.d.

e. Check the recorded waveforms by performing the following manipulations:

1. Check TR Code for Mode 3.

2. Check R Code.

3.3 Low Temperature Test

3.3.1 Precool temperature chamber to -25°C. Place system connected to control box inside and allow one half hour for stabilization.

3.3.2 Repeat 3.2.1.

3.3.3 Repeat 3.2.2.

3.3.4 Repeat 3.2.3.

3.3.5 Repeat 3.2.4.

3.4 High Temperature Test

3.4.1 Preheat temperature chamber to + 100°C. Place system connected to control box inside and allow one half hour for stabilization.

3.4.2 Repeat 3.2.1.

3.4.3 Repeat 3.2.2.

3.4.4 Repeat 3.2.3.

3.4.5 Repeat 3.2.4.

3.5 Vibration Test - The following tests will be performed while repeating paragraph 3.2. (sections d and e).

3.5.1 The assembly shall be attached firmly and securely to the vibration exciter by its normal attachment points. The vibration level shall be observed on the exciter as near to the supporting bracket as possible. The assembly shall be subjected to the vibration test in three mutually perpendicular directions, one of which shall conform as nearly as possible to the booster thrust axis.

3.5.2 Low Frequency Vibration Test - The assembly shall be subjected to sinusoidal vibrations at frequencies between 12 cps and 40 cps for 5 minutes in each of three orthogonal directions. The frequency of vibration shall be swept at a rate varying directly with frequency. The levels and sweep procedures are as follows:

Amplitude	Frequency	Time	Sweep Method
3 g's peak	12 to 40 cps	5 minutes	Swept once from 12 to 40 cps and back to 12 cps

3.5.3 High Frequency Complex Wave Vibration Test - The test shall consist of the following two segments of combined white Gaussian noise (WGN) band-limited between 40 and 1500 cps and sweeping sinusoidal vibration. The sinusoid shall be swept once from 35 cps to 1500 cps and back to 35 cps in the time period of the segment. The total test time shall be eight minutes in each of the three directions.

a. Segment (1) - Combined 10g rms WGN and 4g rms sweeping sinusoid for 2 minutes.

b. Segment (2) - Combined 5g rms and 4g rms sweeping sinusoid for 6 minutes.

c. Notes on vibration test:

Note 1 - The complex wave test signal will have the following characteristics.

Time (sec)	Type of Signal	Ratio at Test Level to Calibration	rms g level
0-15	Noise (calibration)	1	2
0-30	None	0	0
Segment 1			
30-150	Noise plus sinusoid	5.4	10.8
	Noise only	5	10
	Sinusoid only	2	4
Segment 2			
150-510	Noise plus sinusoid	3.2	6.4
	Noise only	2.5	5
	Sinusoid only	2	4

Note 2 - For creating the random noise, the output of a random noise generator, General Radio Model 1390-A or equivalent, may be used if proper care is taken to ensure the correct amplitude distribution of the signal. For testing the noise generator or any associated equipment, the use of amplitude distribution analyzer, described in JPL Memorandum No. 20-190, is suggested. For ensuring correct noise bandwidth, a filter with an asymptotic slope of at least 24 db per octave and 3 db points at 40 and 1500 cps shall be considered acceptable.

3.6 Final Test

3.6.1 Performance Test No. 1

a. Repeat 3.2.1.

3.6.2 Performance Test No. 2

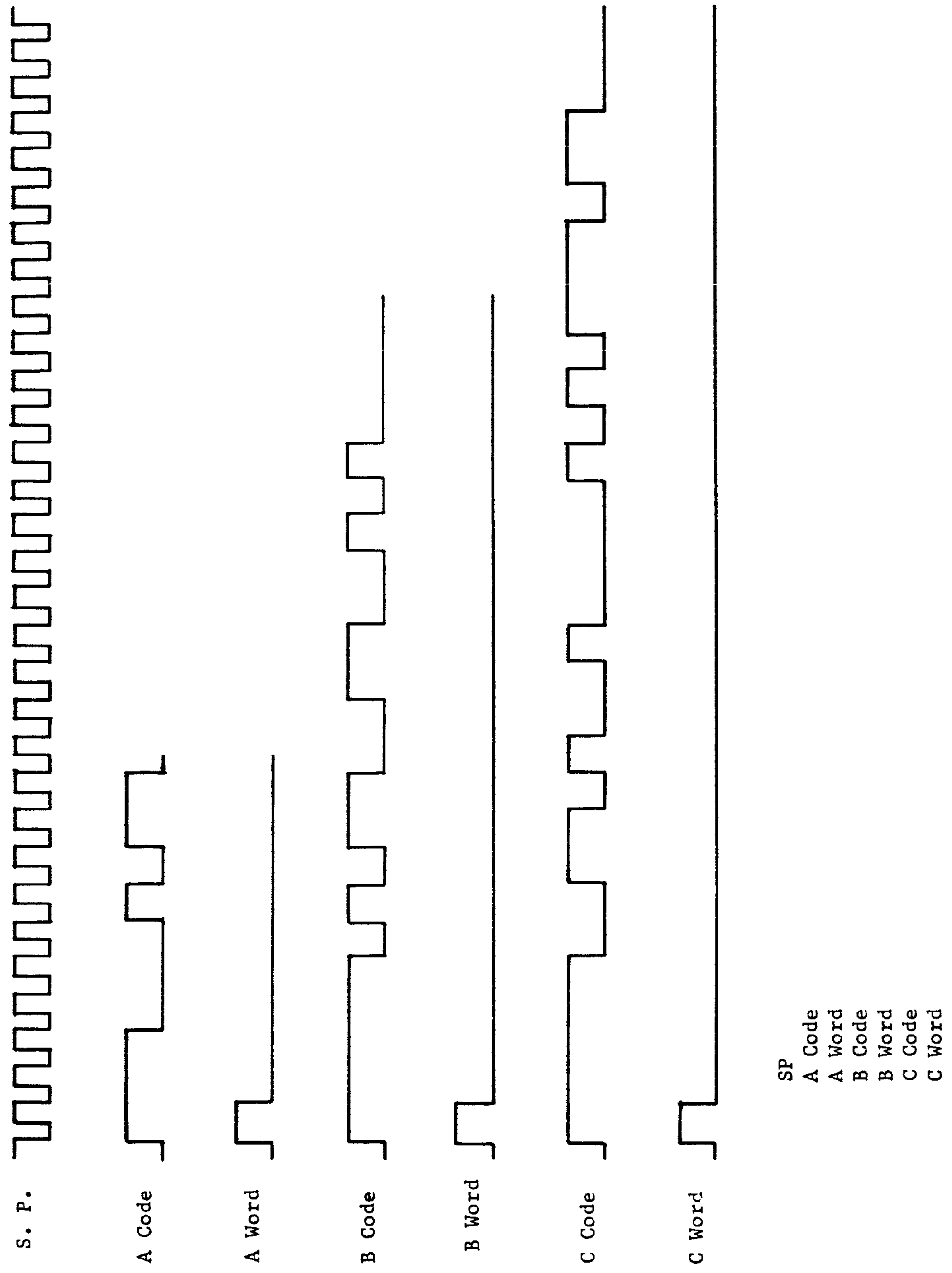
b. Repeat 3.2.2.

3.6.3 Performance Test No. 3

c. Repeat 3.2.3.

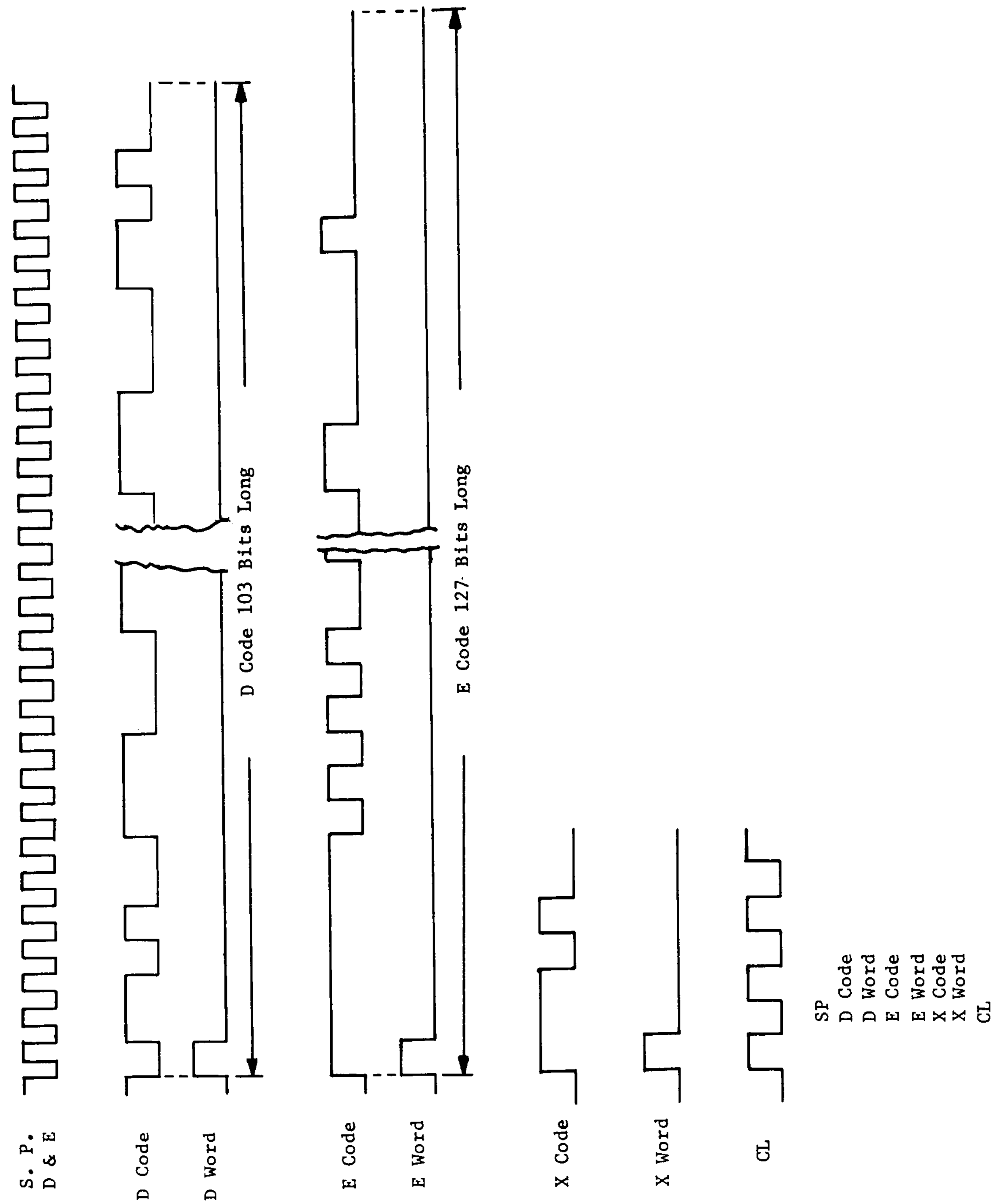
3.6.4 Performance Test No. 4

d. Repeat 3.2.4.



TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS, TEXAS	CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514715
SYM.	SCALE	WT	SHEET 9

TI-5419



TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514715
SCALE	WT	SHEET 10

SYM.

TI-5419

5. TABLES

5.1 Table I

Function	Output
A Code	11100010110
A Word	10000000000
B Code	11111010110011001010000
B Word	10000000000000000000000
C Code	1111100110100100001010111011000
C Word	1000000000000000000000000000000
D Code	0110100111000111111110001011011101110101 00100001001101001101111101101010001000100 101110000000111000110100
D Word	1000000000000000000000000000000000000000000 00000000000000000000000000000000000000 000000000000000000000000
E Code	111111101010100110011101110100101100011011110110 101101100100100011100001011111001010111001101000100 1111000101000011000001000000
E Word	100000000000000000000000000000000000000000000000 000000000000000000000000000000000000000000000000000 0000000000000000000000000000
X Code	1110100
X Word	1000000
CL	10

5.2 Table II

Output		**Code Combination**
R_{tn+2} Code		$(A \oplus B \oplus C \oplus D \oplus E)_{tn} \oplus X_{tn+1}$
TR_{tn+2} Code	Mode 1	CL_{tn+1}
TR_{tn+2} Code	Mode 2	$(X \cdot CL)_{tn+1} + \overline{X}_{tn+1} \cdot [CL_{tn+1} \oplus (ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE)_{tn}]$
TR_{tn+2} Code	Mode 2	$(X \cdot CL)_{tn+1} + \overline{X}_{tn+1} \cdot [CL_{tn+1} \oplus (A \oplus B \oplus C \oplus D \oplus E)_{tn}]$

A 514716

DASH NO.	QTY	NEXT ASSY NO.	SIZE	PROJ NO.
				464

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

INSPECTION TEST PROCEDURE

PART I

INDIVIDUAL TEST

FOR

TRANSMITTER AND RECEIVER NO. 2 MODULE

INTEGRATED CIRCUIT SEQUENCE GENERATOR

Contract No. 950693

MANUFACTURER - TEXAS INSTRUMENTS INCORPORATED

TEST DATA SHEET 514723 TO BE FILLED OUT AS PART OF THIS TEST PROCEDURE

QTY REQD -2	QTY REQD -1	ITEM NO.	DWG SIZE	TEXAS INSTRUMENTS PART OR IDENTIFYING NO.	GOVT OR INDUSTRY PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

LIST OF MATERIALS

DR BD/ Fred Clark	DATE 5/21/64	TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS, TEXAS
CKD H. Miller M	5-26-64	
ENGR Fred Clark	5/21/64	TITLE TEST PROCEDURE, INSPECTION, PART I, INDIVIDUAL TEST, TRANSMITTER AND RECEIVER NO. 2 MODULE
APPD W. S. Thomas	5-27-64	
DESIGN ACTIVITY RELEASE L. M. McPeek	5-27-64	CODE IDENT NO. 96214 · SIZE A · DRAWING NO. 514716
		SCALE · WT · SHEET 1 of 12

TI-1E1793-A

TABLE OF CONTENTS

		Paragraph No.
1.	TABLE OF TESTS	
1.1	Preparation	3.1
1.2	Room Temperature Test	3.2
1.3	Low Temperature Test	3.3
1.4	High Temperature Test	3.4

2. LIST OF TEST EQUIPMENT

2.1 Data Sheets (TI Drawing 514723) shall be completed as part of this test.

2.2 Verify that test equipment designated WORKING STANDARD, or better, is currently certified per TI Std. Procedure No. 12-28.

2.3 Commercial Test Equipment - The following commercially available test equipment (or equivalent) is required to complete the test required by this specification.

2.3.1 Oscilloscope - Tektronix 543/Plug-in Type CA

2.3.2 Power Supply, dc. 0-50 VDC, 1.5 amp Sorenson T50-1.5

2.3.3 Pulse Generator, TI Model 6563

2.3.4 Temperature Chamber - TI Controlled Environmental Unit

2.4 Special Test Equipment - The following special test equipment is required to complete the test required by this specification.

2.4.1 Test Set, Module, TI Drawing 514711

2.4.2 Control Box, TI Drawing 514713

2.4.3 Five Stage Counter, TI Drawing 514714

3. TEST PROCEDURES

The following test procedure covers the module test requirements to evaluate the Transmitter and Receiver No. 2 module of the Integrated Circuit Sequence Generator.

3.1 Preparation

3.1.1 Visually inspect module for any mechanical faults such as wiring mistakes, broken leads, bad welds, etc. before plugging module into test set.

3.1.2 Adjust V_{cc} supply voltage to 3.1 VDC ± 0.1 VDC

3.1.3 Adjust pulse generator for a positive going pulse (50 nsec to 500 nsec wide) from 0 to +3V ± 0.1V at a rate of 1mc ± 50KC with rise and fall times at a minimum (minimum ringing at 0 and +3 volts).

Caution: Only a positive going signal is to be applied to these modules.

3.1.4 Plug module into test set.

3.1.5 Connect test set to control box.

3.1.6 Connect V_{cc} to test point 25 and GRD to test point 26 of control box.

3.1.7 Connect the five stage counter to control box as follows:

Counter Lead	Control Box
$\underline{S_1}$	Test Point 20 ($\underline{X}$)
$\overline{S_1}$	Test Point 15 (X)
$\underline{S_2}$	Test Point 3 ($\underline{D}$)
$\overline{S_2}$	Test Point 17 (D)
$\underline{S_3}$	Test Point 19 ($\underline{E}$)
$\overline{S_3}$	Test Point 7 (E)
$\underline{S_4}$	Test Point 2 (1)
$\overline{S_4}$	No Connection
$\underline{S_5}$	Test Point 10 (2)
$\overline{S_5}$	No Connection

3.1.8 Connect pulse generator to test point 13 of the control box.

Note: Oscilloscope should be triggered on the positive going edge of $\overline{S_5}$.

3.2 Room Temperature Test

3.2.1 Performance Test No. 1

a. Connect the following test points to GRD.
   1. TP 14 (CL)

b. Connect the following test points to V_{cc}.
1. TP 6 ($\overline{CL}$)
2. TP 1 (AC)
3. TP 9 (CO)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
1. R TP 22
2. $\overline{R}$ TP 21
3. TR TP 8
4. $\overline{TR}$ TP 16

3.2.2 Performance Test No. 2

a. Connect the following test points to GRD.
1. TP 6 (CL)

b. Connect the following test points to V_{cc}.
1. TP 14 (CL)
2. TP 1 (AC)
3. TP 9 (CO)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
1. R TP 22
2. $\overline{R}$ TP 21
3. TR TP 8
4. $\overline{TR}$ TP 16

3.2.3 Performance Test No. 3

a. Connect the following test points to GRD.
1. TP 14 (CL)
2. TP 9 (CO)

b. Connect the following test points to V_{cc}.
1. TP 6 ($\overline{CL}$)
2. TP 1 (AC)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
1. R TP 22
2. $\overline{R}$ TP 21
3. TR TP 8
4. $\overline{TR}$ TP 16

3.2.4 Performance Test No. 4

a. Connect the following test points to GRD.
1. TP 6 ($\overline{CL}$)
2. TP 9 (CO)

b. Connect the following test points to V_{CC}.
1. TP 14 (CL)
2. TP 1 (AC)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
1. R TP 22
2. $\overline{R}$ TP 21
3. TR TP 8
4. $\overline{TR}$ TP 16

3.2.5 Performance Test No. 5

a. Connect the following test points to GRD.
1. TP 14 (CL)
2. TP 1 (AC)

b. Connect the following test points to V_{CC}.
1. TP 6 ($\overline{CL}$)
2. TP 9 (CO)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
1. R TP 22
2. $\overline{R}$ TP 21
3. TR TP 8
4. $\overline{TR}$ TP 16

3.2.6 Performance Test No. 6

a. Connect the following test points to GRD.
1. TP 6 ($\overline{CL}$)
2. TP 1 (AC)

b. Connect the following test points to V_{CC}.
1. TP 14 (CL)
2. TP 9 (CO)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
1. R TP 22
2. $\overline{R}$ TP 21
3. TR TP 8
4. $\overline{TR}$ TP 16

3.2.7 Performance Test No. 7

a. Connect the following test points to GRD.
1. TP 14 (CL)
2. TP 1 (AC)
3. TP 9 (CO)

b. Connect the following test points to V_{cc}.

1. TP 6 ($\overline{CL}$)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.

1. R TP 22
2. $\overline{R}$ TP 21
3. TR TP 8
4. $\overline{TR}$ TP 16

3.2.8 Performance Test No. 8

a. Connect the following test points to GRD.

1. TP 6 ($\overline{CL}$)
2. TP 1 (AC)
3. TP 9 (CO)

b. Connect the following test points to V_{cc}.

1. TP 14 (CL)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.

1. R TP 22
2. $\overline{R}$ TP 21
3. TR TP 8
4. $\overline{TR}$ TP 16

3.3 Low Temperature Test

3.3.1 Precool temperature chamber to -25°C. Place test set with module plugged-in, inside and allow one half hour for stabilization.

3.3.2 Repeat 3.2.1

3.3.3 Repeat 3.2.2

3.3.4 Repeat 3.2.3

3.3.5 Repeat 3.2.4

3.3.6 Repeat 3.2.5

3.3.7 Repeat 3.2.6

3.3.8 Repeat 3.2.7

3.3.9 Repeat 3.2.8

3.4 High Temperature Test

3.4.1 Preheat temperature chamber to +100°C. Place test set, with module plugged-in, inside and allow one half hour for temperature stabilization.

3.4.2 Repeat 3.2.1

3.4.3 Repeat 3.2.2

3.4.4 Repeat 3.2.3

3.4.5 Repeat 3.2.4

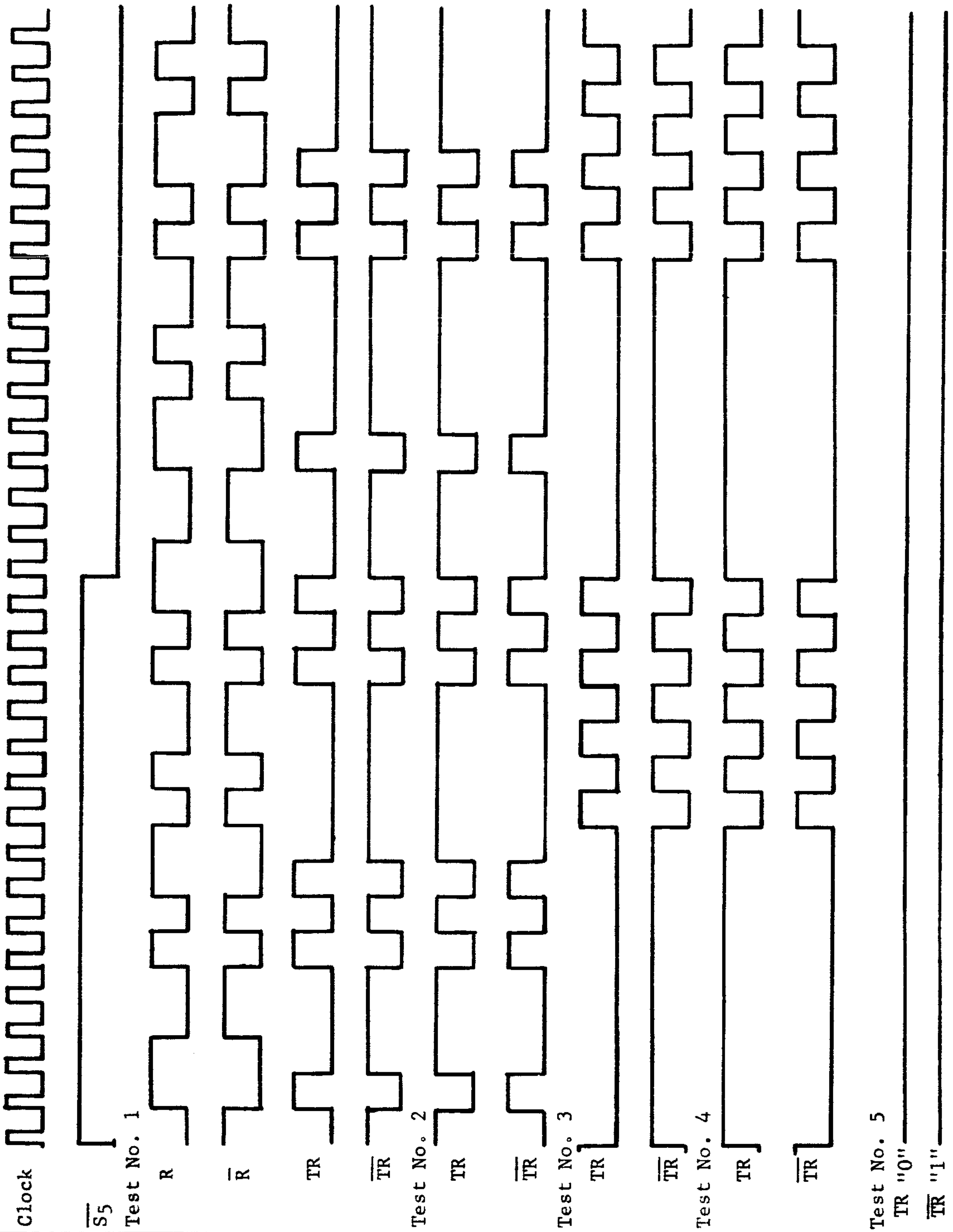
3.4.6 Repeat 3.2.5

3.4.7 Repeat 3.2.6

3.4.8 Repeat 3.2.7

3.4.9 Repeat 3.2.8

4. DIAGRAMS



TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

SYM.

CODE IDENT NO. 96214

SIZE A

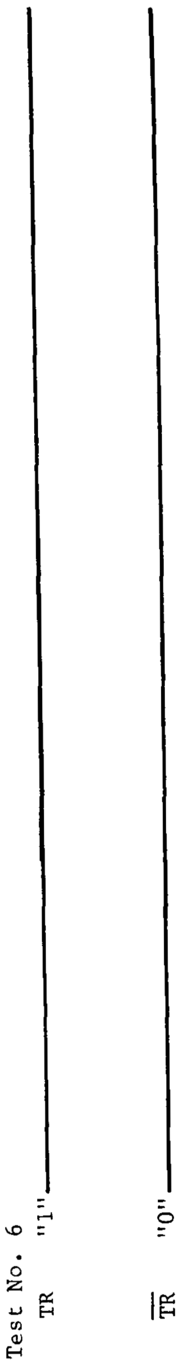
DRAWING NO. 514716

SCALE

WT

SHEET 9

TI-5419



TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS, TEXAS	CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514716
SYM.	SCALE	WT	SHEET 10

TI-5419

5. TABLE I

Performance Test	Function	Output
No. 1	R	01100101101001011001101001011010
	$\overline{R}$	10011010010110100110010110100101
	TR	01000101000001010001000001010000
	$\overline{TR}$	10111010111110101110111110101111
	$\overline{S5}$	11111111111111110000000000000000
No. 2	R	Same as R for Performance Test No. 1
	$\overline{R}$	Same as $\overline{R}$ for Performance Test No. 1
	TR	10111010111110101110111110101111
	$\overline{TR}$	01000101000001010001000001010000
	$\overline{S5}$	Same as $\overline{S5}$ for Performance Test No.1
No. 3	R	Same as R for Performance Test No. 1
	$\overline{R}$	Same as $\overline{R}$ for Performance Test No. 1
	TR	00000000010101010000000001010101
	$\overline{TR}$	11111111101010101111111110101010
	$\overline{S5}$	Same as $\overline{S5}$ for Performance Test No.1
No. 4	R	Same as R for Performance Test No. 1
	$\overline{R}$	Same as $\overline{R}$ for Performance Test No. 1
	TR	11111111101010101111111110101010
	$\overline{TR}$	00000000010101010000000001010101
	$\overline{S5}$	Same as $\overline{S5}$ for Performance Test No.1
No. 5	R	Same as R for Performance Test No. 1
	$\overline{R}$	Same as $\overline{R}$ for Performance Test No. 1
	TR	All zero's
	$\overline{TR}$	All one's
	$\overline{S5}$	Same as $\overline{S5}$ for Performance Test No.1
No. 6	R	Same as R for Performance Test No. 1
	$\overline{R}$	Same as $\overline{R}$ for Performance Test No. 1
	TR	All one's
	$\overline{TR}$	All zero's
	$\overline{S5}$	Same as $\overline{S5}$ for Performance Test No.1
No. 7	R	Same as R for Performance Test No. 1
	$\overline{R}$	Same as $\overline{R}$ for Performance Test No. 1
	TR	All zero's
	$\overline{TR}$	All one's
	$\overline{S5}$	Same as $\overline{S5}$ for Performance Test No. 1

Performance Test	Function	Output
No. 8	R	Same as R for Performance Test No. 1
	$\overline{R}$	Same as $\overline{R}$ for Performance Test No. 1
	TR	All one's
	$\overline{TR}$	All zero's
	$\overline{S_5}$	Same as $\overline{S_5}$ for Performance Test No. 1

A 514717

DASH NO.	QTY	NEXT ASSY NO.	SIZE	PROJ NO.
				464

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

INSPECTION TEST PROCEDURE
PART I
INDIVIDUAL TEST
FOR
TRANSMITTER AND RECEIVER NO. 1 MODULE
INTEGRATED CIRCUIT SEQUENCE GENERATOR
CONTRACT NO. 950693
MANUFACTURER - TEXAS INSTRUMENTS INCORPORATED

TEST DATA SHEET 514724 TO BE FILLED OUT AS PART OF THIS TEST PROCEDURE.

QTY REQD -2	QTY REQD -1	ITEM NO.	DWG SIZE	TEXAS INSTRUMENTS PART OR IDENTIFYING NO.	GOVT OR INDUSTRY PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

LIST OF MATERIALS

	DATE
DR jb/	3/23/64
CKD H. Miller M	5-26-64
ENGR	5/22/64
APPD W. L. Thomas	5-27-64
DESIGN ACTIVITY RELEASE	5-27-64

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS. TEXAS

TITLE
TEST PROCEDURE, INSPECTION,
PART I, INDIVIDUAL TEST,
TRANSMITTER AND RECEIVER NO. 1 MODULE

CODE IDENT NO.	SIZE	DRAWING NO.
96214	A	514717

SCALE
WT
SHEET 1 of 7

TI-1E1793-A

TABLE OF CONTENTS

1. TABLE OF TESTS

		Paragraph No.
1.1	Preparation	3.1
1.2	Room Temperature Test	3.2
1.3	Low Temperature Test	3.3
1.4	High Temperature Test	3.4

2. LIST OF TEST EQUIPMENT

2.1 Data Sheets (TI Drawing 514724) shall be completed as part of this test.

2.2 Verify that test equipment designated WORKING STANDARD, or better, is currently certified per TI Standard Procedure No. 12-28.

2.3 Commercial Test Equipment - The following commercially available test equipment (or equivalent) is required to complete the tests required by this specification.

2.3.1 Oscilloscope - Tektronix 543/Plug-in Type CA

2.3.2 Power Supply, dc, 0-50 VDC, 1.5 amp Sorenson T50-1.5

2.3.3 Pulse Generator, TI Model 6563

2.3.4 Temperature Chamber - TI Controlled Environmental Unit

2.4 Special Test Equipment - The following special test equipment is required to complete the test required by this specification.

2.4.1 Test Set, Module, TI Drawing 514711

2.4.2 Control Box, TI Drawing 514713

2.4.3 Five Stage Counter, TI Drawing 514714

3. TEST PROCEDURES

The following test procedures cover the module test requirements to evaluate the Transmitter and Receiver No. 1 Module of the Integrated Circuit Sequence Generator.

3.1 Preparation

3.1.1 Visually inspect module for any mechanical faults such as wiring mistakes, broken leads, bad welds, etc. before plugging module into test set.

3.1.2 Adjust V_{CC} supply voltage to 3.1 VDC ± 0.1 VDC.

3.1.3 Adjust pulse generator for a positive going pulse (50 nsec to 500 nsec wide) from 0 to +3V ± 0.1V at a rate of 1mc ± 50kc, with rise and fall times at a minimum (minimum ringing at 0 and +3 volts).

CAUTION: Only a positive going signal is to be applied to these modules.

3.1.4 Plug module into test set.

3.1.5 Connect test set to control box.

3.1.6 Connect V_{CC} to test point 25 and ground to test point 26 of control box.

3.1.7 Connect the five stage counter to control box as follows:

Counter Lead	Control Box
S_1	Test Point 14 (A)
$\overline{S_1}$	Test Point 15 $(\overline{A})$
S_2	Test Point 6 (B)
$\overline{S_2}$	Test Point 7 $(\overline{B})$
S_3	Test Point 12 (C)
$\overline{S_3}$	Test Point 5 $(\overline{C})$
S_4	Test Point 17 (D)
$\overline{S_4}$	No Connection
S_5	Test Point 19 (E)
$\overline{S_5}$	No Connection

3.1.8 Connect pulse generator positive output to test point 20 of the control box.

NOTE: Oscilloscope should be triggered on the positive going edge of $\overline{S_5}$.

3.2 Room Temperature Test

3.2.1 Observe the output (Section 4 and 5) of the module on the oscilloscope.

3.3 Low Temperature Test

3.3.1 Precool temperature chamber to -25°C. Place test set with module connected inside chamber and allow one half hour for stabilization.

3.3.2 Repeat 3.2.1

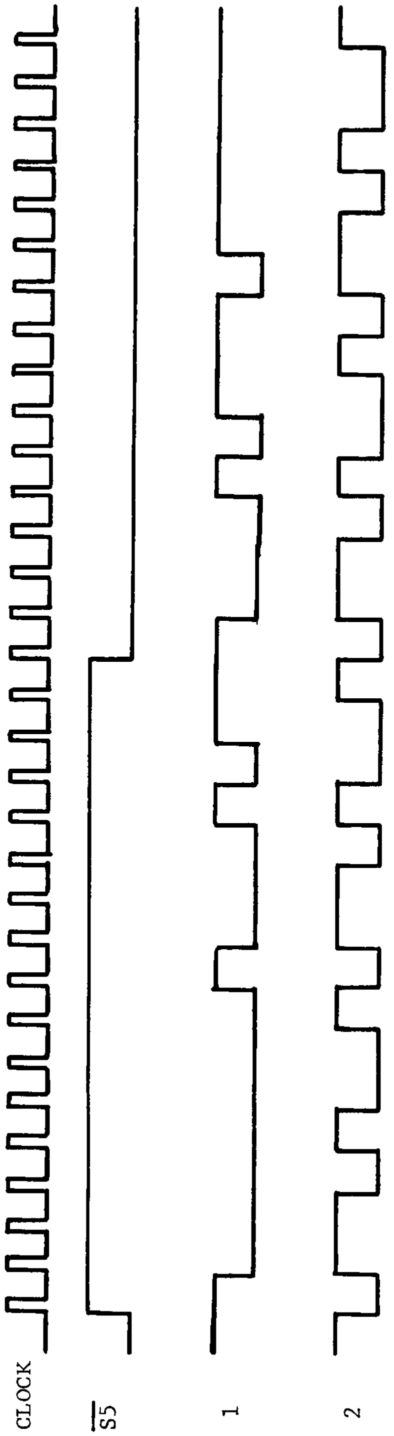
3.4 High Temperature Test

3.4.1 Preheat temperature chamber to +100°C. Place test set with module connected inside chamber and allow one half hour for stabilization.

3.4.2 Repeat 3.2.1

TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS TEXAS	CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514717
SYM	SCALE	WT	SHEET 5

4. DIAGRAMS



TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

CODE IDENT NO.	SIZE	DRAWING NO.
96214	A	514717

SCALE
WT
SHEET 6

SYM.

TI-5419

5. TABLE I

Function	Output
1 (Test Point 22)	100000001000101110C0101110111111
2 (Test Point 21)	01101001011010010110100101101001

TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS, TEXAS	CODE IDENT NO.	SIZE	DRAWING NO.
SYM.	96214	A	514717
	SCALE	WT	SHEET 7

514718

A

DASH NO.	QTY	NEXT ASSY NO.	SIZE	PROJ NO.
				464

REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPROVED

INSPECTION TEST PROCEDURE

PART I

INDIVIDUAL TEST

FOR

D SEQUENCE GENERATOR MODULE

INTEGRATED CIRCUIT SEQUENCE GENERATOR

Contract No. 950693

MANUFACTURER - TEXAS INSTRUMENTS INCORPORATED

TEST DATA SHEET 514725 TO BE FILLED OUT AS PART OF THIS TEST PROCEDURE

QTY REQD -2	QTY REQD -1	ITEM NO.	DWG SIZE	TEXAS INSTRUMENTS PART OR IDENTIFYING NO.	GOVT OR INDUSTRY PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

LIST OF MATERIALS

		DATE
DR BD/	Roy	3/26/64
CKD	H. Miller, M	5 26 64
ENGR	Paul Clark	5/13/64
APPD	W. S. Thomas	5-27-64
DESIGN ACTIVITY RELEASE	K. M. McPeak	5-27-64

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

TITLE
TEST PROCEDURE, INSPECTION,
PART I, INDIVIDUAL TEST,
D SEQUENCE GENERATOR MODULE

CODE IDENT NO.	SIZE	DRAWING NO.
96214	A	514718

SCALE
WT
SHEET 1 of 9

TABLE OF CONTENTS

		Paragraph No.
1.	TABLE OF TESTS	
1.1	Preparation	3.1
1.2	Room Temperature Test	3.2
1.3	Low Temperature Test	3.3
1.4	High Temperatore Test	3.4

2. LIST OF TEST EQUIPMENT

2.1 Data Sheets (TI Drawing 514725) shall be completed as part of this test.

2.2 Verify that test equipment designated WORKING STANDARD, or better, is currently certified per TI Std. Procedure No. 12-28.

2.3 Commercial Test Equipment - The following commercially available test equipment (or equivalent) is required to complete the test required by this specification.

2.3.1 Oscilloscope - Tektronix 543/Plug in Type CA

2.3.2 Power Supply, dc, 0-50 VDC, 1.5 amp Sorenson T50-1.5

2.3.3 Pulse Generator, TI Model 6563

2.3.4 Temperature Chamber - TI Controlled Environmental Unit

2.4 Special Test Equipment - The following special test equipment is required to complete the test required by this specification.

2.4.1 Test Set, Module, TI Drawing 514711

2.4.2 Control Box, TI Drawing 514713

3. TEST PROCEDURES

The following test procedure covers the module test requirements to evaluate the D Sequence Generator Module of the Integrated Circuit Sequence Generator.

3.1 Preparation

3.1.1 Visually inspect module for any mechanical faults such as wiring mistakes, broken leads, bad welds, etc. before plugging module into test set.

3.1.2 Adjust V_{cc} supply voltage to 3.1 VDC ± 0.1 VDC.

3.1.3 Adjust pulse generator for a positive going pulse (50 nsec to 500 nsec wide) from 0 to +3V ± 0.1V at a rate of 1mc ± 50KC with rise and fall times at a minimum (minimum ringing at 0 and +3 volts).

Caution: Only a positive going signal is to be applied to these modules.

3.1.4 Plug module into test set.

3.1.5 Connect test set to control box.

3.1.6 Connect V_{cc} to test point 25, and ground to test point 26 of control box.

3.1.7 Connect pulse generator positive output to test point 7 of control box.

Note: Oscilloscope should be triggered on the positive going edge of D Word.

3.2 Room Temperature Test

Observe the following outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.

a.	D_7	TP 5
b.	$\overline{D_7}$	TP 19
c.	D_6	TP 18
d.	$\overline{D_6}$	TP 1
e.	D_5	TP 11
f.	$\overline{D_5}$	TP 4
g.	D_4	TP 10
h.	$\overline{D_4}$	TP 24
i.	D_3	TP 16
j.	$\overline{D_3}$	TP 17
k.	D_2	TP 8
l.	$\overline{D_2}$	TP 21
m.	D_1	TP 22
n.	$\overline{D_1}$	TP 9
o.	D Word	TP 3

3.3 Low Temperature Test

3.3.1 Precool temperature chamber to -25°C. Place test set, with module plugged-in, inside and allow one half hour for stabilization.

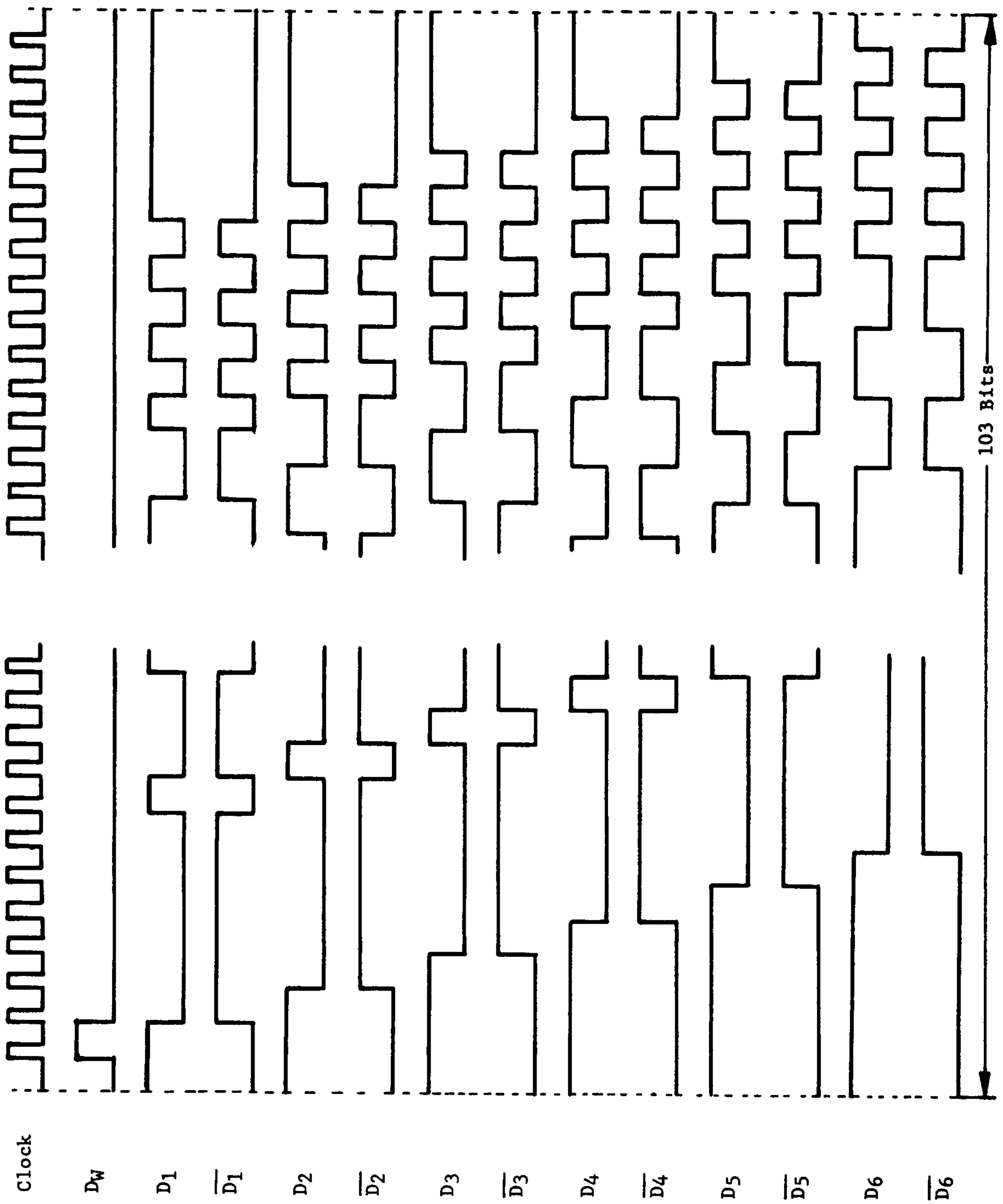
3.3.2 Repeat 3.2.1

3.4 High Temperature Test

3.4.1 Preheat temperature chamber to 100°C. Place test set, with module plugged-in, inside and allow one half hour for stabilization.

3.4.2 Repeat 3.2.1

4. DIAGRAMS

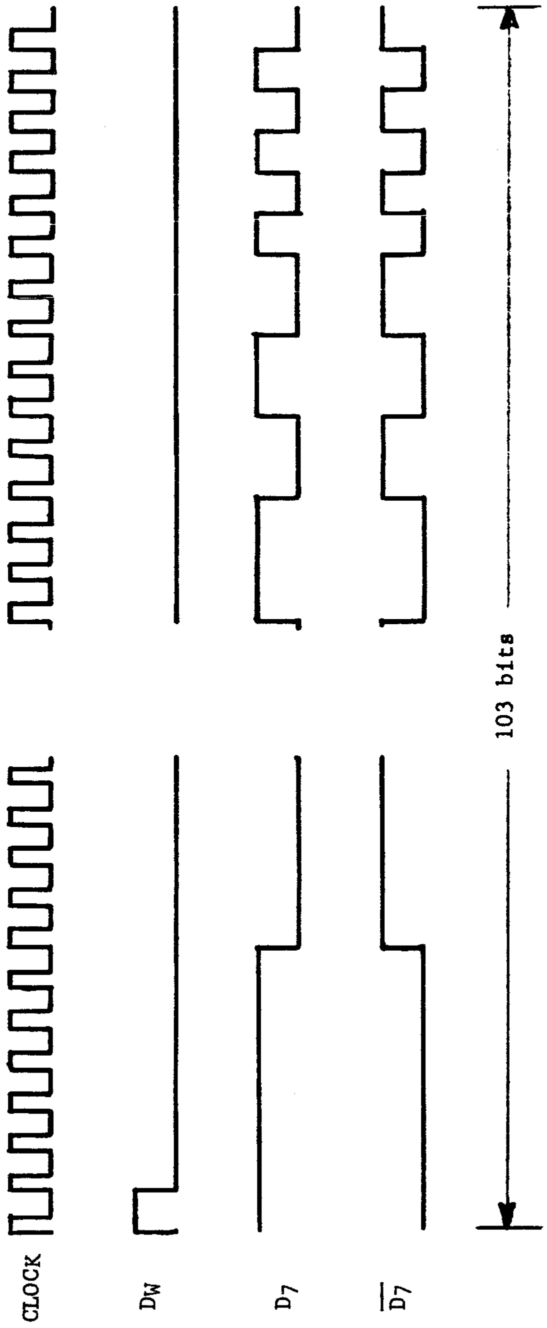


TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

CODE IDENT NO.	SIZE	DRAWING NO.
96214	A	514718
SCALE	WT	SHEET 6

SYM.

TI-5419



TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514718	
SCALE	WT		SHEET 7

SYM.

TI-5419

5. TABLE I

Function		Output
a.	D_7	11111110000000100010110011101010 01111110100001110001001001101101 01101111011000110100101110111001 100101010
b.	$\overline{D_7}$	00000001111111011101001100010101 10000001011110001110110110010010 10010000010011100101101000100011 0011010101
c.	D_6	1111110000000100010110011101010 01 11110100001110001001001101101011 0111101100011010010111011100 1100 1010101
d.	$\overline{D_6}$	000000111111011101001100010101 10 00001011110001110110110010010100 10000100111001011010001000110011 0101010
e.	D_5	11111000000010001011001110101001 1 1110100001110001001001101101011 0 1111011000110100101110111001100 1 0101011
f.	$\overline{D_5}$	00000111111011101001100010101100 00010111100011101101100100101001 00001001110010110100010001100110 1010100
g.	D_4	11110000000100010110011101010011 1 1101000011100010010011011010110 1 1110110001101001011101110011001 0 1010111
h.	$\overline{D_4}$	00001111110111010011000101011000 00101111000111011011001001010010 00010011100101101000100011001101 0101000
i.	D_3	11100000001000101100111010100111 1 10100001110001001001101101011011 11011000110100101110111000110110 10101111

Function	Output
j. $\overline{D_3}$	00011111101110100110001010110000 01011110001110110110010010100100 00100111001011010001000110011010 1010000
k. D_2	11000000100010110011101010011111 01000011100010010011011010110111 10110001101001011101110001100101 01011111
l. $\overline{D_2}$	00111111011101001100010101100000 10111100011101101100100101001000 01001110010110100010001100110101 0100000
m. D_1	10000001000101100111010100111110 10000111000100100110110101101111 01100011010010111011100011001010 10111111
n. $\overline{D_1}$	01111110111010011000101011000001 01111000111011011001001010010000 10011100101101000100011001101010 1000000
o. D Word	10000000000000000000000000000000 00000000000000000000000000000000 00000000000000000000000000000000 000000

A 514719

DASH NO.	QTY	NEXT ASSY NO.	SIZE	PROJ NO.
				464

REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPROVED

INSPECTION TEST PROCEDURE

PART I

INDIVIDUAL TEST

FOR

D OUTPUT GATING NO. 2 MODULE

INTEGRATED CIRCUIT SEQUENCE GENERATOR

CONTRACT NO. 950693

MANUFACTURER - TEXAS INSTRUMENTS INCORPORATED

TEST DATA SHEET 514726 TO BE FILLED OUT AS PART OF THIS TEST PROCEDURE

-2	-1	ITEM NO.	DWG SIZE	TEXAS INSTRUMENTS	GOVT OR INDUSTRY	NOMENCLATURE OR DESCRIPTION
QTY REQD				PART OR IDENTIFYING NO.		

LIST OF MATERIALS

	DATE
DR BD/ Roy	3/26/64
CKD H. Miller M	5-26-64
ENGR Fred Clark	5/23/64
APPD W. D. Thomas	5-27-64
DESIGN ACTIVITY RELEASE K. M. McLeod	5-27-64

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

TITLE
TEST PROCEDURE, INSPECTION,
PART I,
INDIVIDUAL TEST,
D OUTPUT GATING NO. 2 MODULE

CODE IDENT NO.	SIZE	DRAWING NO.
96214	A	514719
SCALE	WT	SHEET 1 of 8

TI-1E1793-A

TABLE OF CONTENTS

		Paragraph No.
1.	TABLE OF TESTS	
1.1	Preparation	3.1
1.2	Room Temperature Test	3.2
1.3	Low Temperature Test	3.3
1.4	High Temperature Test	3.4

2. LIST OF TEST EQUIPMENT

2.1 Data Sheets (TI Drawing 514726) shall be completed as part of this test.

2.2 Verify that test equipment designated WORKING STANDARD, or better, is currently certified per TI Standard Procedure No. 12-28.

2.3 Commercial Test Equipment - The following commercially available test equipment (or equivalent) is required to complete the test required by this specification.

2.3.1 Oscilloscope - Tektronix 543/Plug in Type CA

2.3.2 Power Supply, dc, 0-50 VDC, 5 amp Sorenson T50-1.5

2.3.3 Pulse Generator, TI Model 6563

2.3.4 Temperature Chamber - TI Controlled Environmental Unit

2.4 Special Test Equipment - The following special test equipment is required to complete the test required by this specification.

2.4.1 Test Set, Module, TI Drawing 514711

2.4.2 Control Box, TI Drawing 514713

2.4.3 Five Stage Counter, TI Drawing 514714

TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS, TEXAS	CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514719
SYM.	SCALE	WT	SHEET 3

3. TEST PROCEDURES

The following test procedure covers the module test requirements to evaluate the D Output Gating No. 2 Module of the Integrated Circuit Sequence Generator.

3.1 Preparation

3.1.1 Visually inspect module for any mechanical faults such as wiring mistakes, broken leads, bad welds, etc. before plugging module into test set.

3.1.2 Adjust V_{cc} supply voltage to 3.1 VDC ± 0.1 VDC.

3.1.3 Adjust pulse generator for a positive going pulse (50 nsec to 500 nsec wide) from 0 to +3V ± 0.1V at a rate of 1mc ± 50KC with rise and fall times at a minimum (minimum ringing at 0 and +3 volts).

Caution: Only a positive going signal is to be applied to these modules.

3.1.4 Plug module into test set.

3.1.5 Connect test set to control box.

3.1.6 Connect V_{cc} to test point 25 and ground to test point 26 of control box.

3.1.7 Connect the five stage counter to control box as follows:

Counter Lead	Control Box
S_1	No Connection
$\overline{S_1}$	Test Point 22 ($\overline{D_1}$)
S_2	Test Point 21 (D_2)
$\overline{S_2}$	Test Point 8 ($\overline{D_2}$)
S_3	Test Point 16 (D_3)
$\overline{S_3}$	Test Point 23 ($\overline{D_3}$)
S_4	Test Point 17 (D_4)
$\overline{S_4}$	Test Point 10 ($\overline{D_4}$)
S_5	Test Point 24 (D_5)
$\overline{S_5}$	Test Point 18 ($\overline{D_5}$)

Note: Oscilloscope should be triggered on the positive going edge of $\overline{S_5}$.

3.2 Room Temperature Test

3.2.1 Performance Test No. 1

a. Connect the following test points to Ground.
   1. TP 11 (D_6)
   2. TP 4 (D_7)

b. Connect the following test points to V_{cc}.
   1. TP 1 $(\overline{D_6})$
   2. TP 19 $(\overline{D_7})$

c. Observe the output of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
   1. 3 - TP 20

3.2.2 Performance Test No. 2

a. Connect the following test points to Ground.
   1. TP 1 $(\overline{D_6})$
   2. TP 4 (D_7)

b. Connect the following test points to V_{cc}.
   1. TP 11 (D_6)
   2. TP 19 $(\overline{D_7})$

c. Observe the output of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
   1. 3 - TP 20

3.2.3 Performance Test No. 3

a. Connect the following test points to Ground.
   1. TP 11 (D_6)
   2. TP 19 $(\overline{D_7})$

b. Connect the following test points to V_{cc}.
   1. TP 1 $(\overline{D_6})$
   2. TP 4 (D_7)

c. Observe the output of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
   1. 3 - TP 20

3.2.4 Performance Test No. 4

a. Connect the following test points to Ground.
   1. TP 1 $(\overline{D_6})$
   2. TP 19 $(\overline{D_7})$

b. Connect the following test points to V_{cc}.
   1. TP 11 (D_6)
   2. TP 4 (D_7)

c. Observe the output of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.
   1. 3 - TP 20

3.3 Low Temperature Test

3.3.1 Precool temperature chamber to -25°C. Place test set, with module plugged-in, inside and allow one half hour for stabilization.

3.3.2 Repeat 3.2.1

3.3.3 Repeat 3.2.2

3.3.4 Repeat 3.2.3

3.3.5 Repeat 3.2.4

3.4 High Temperature Test

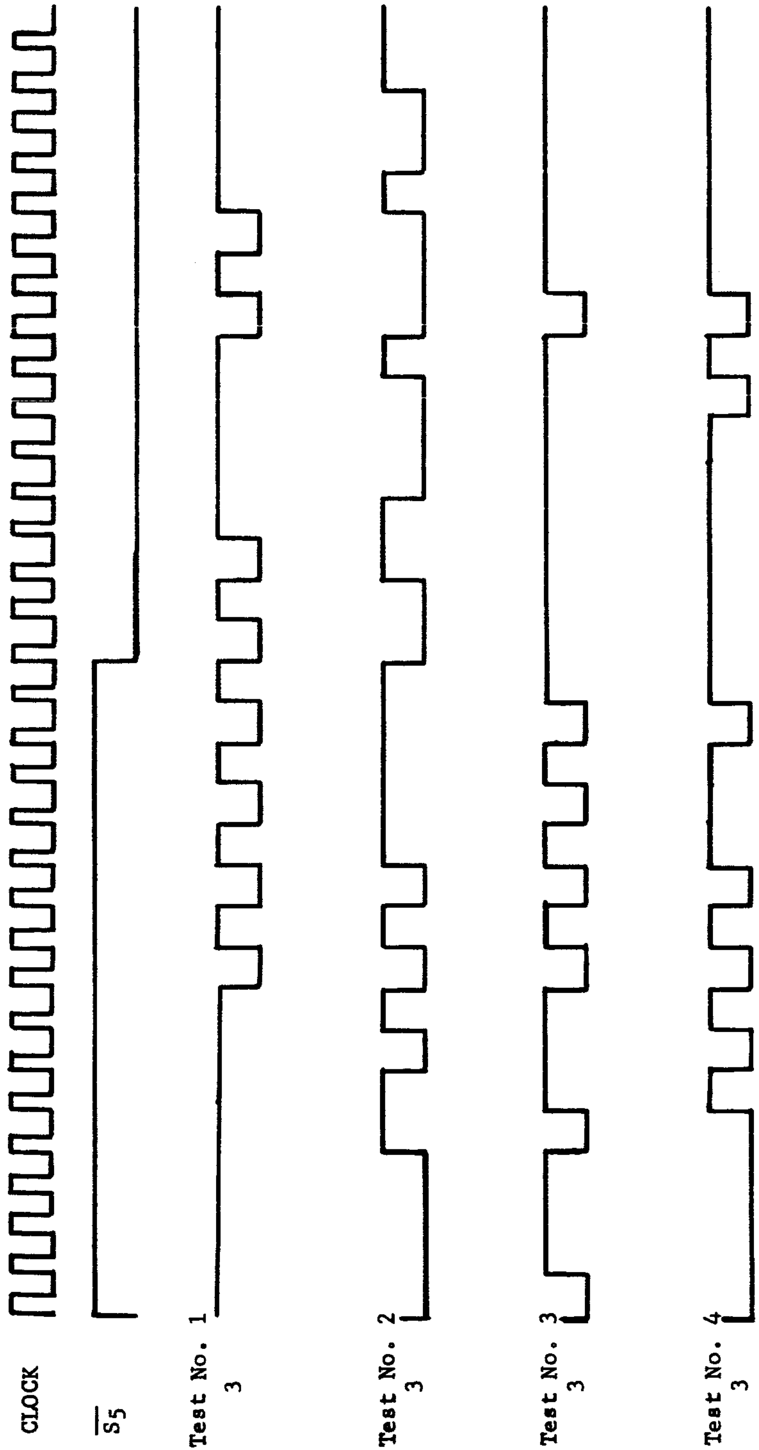
3.4.1 Preheat temperature chamber to +100°C. Place test set, with module plugged-in, inside and allow one half hour for stabilization.

3.4.2 Repeat 3.2.1

3.4.3 Repeat 3.2.2

3.4.4 Repeat 3.2.3

3.4.5 Repeat 3.2.4



TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

SYM.

CODE IDENT NO.	SIZE	DRAWING NO.
96214	A	514719

SCALE	WT	SHEET 7

TI-5419

5. TABLE I

Performance Test	Function	Output
No. 1	$\frac{3}{S_5}$	11111111010101010101111101011111 11111111111111110000000000000000
No. 2	$\frac{3}{S_5}$	00001101010111110011000100010011 11111111111111110000000000000000
No. 3	$\frac{3}{S_5}$	01110111010101011111111101111111 11111111111111110000000000000000
No. 4	$\frac{3}{S_5}$	00000101010111011111110101111111 11111111111111110000000000000000

A 514720

DASH NO.	QTY	NEXT ASSY NO.	SIZE	PROJ NO.
				464

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

INSPECTION TEST PROCEDURE

PART I

INDIVIDUAL TEST

FOR

D OUTPUT GATING NO. 1 MODULE

INTEGRATED CIRCUIT SEQUENCE GENERATOR

CONTRACT NO. 950693

MANUFACTURER - TEXAS INSTRUMENTS INCORPORATED

TEST DATA SHEET 514727 TO BE FILLED OUT AS PART OF THIS TEST PROCEDURE.

QTY REQD -2	QTY REQD -1	ITEM NO.	DWG SIZE	TEXAS INSTRUMENTS PART OR IDENTIFYING NO.	GOVT OR INDUSTRY PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

LIST OF MATERIALS

	DATE
DR jc/Roy	3/27/64
CKD H. Miller M	5-26-64
ENGR Fred Clark	5/22/64
APPD W. D. Thomas	5-27-64
DESIGN ACTIVITY RELEASE K. M. McPeak	5-27-64

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

TITLE

TEST PROCEDURE, INSPECTION,
PART I,
INDIVIDUAL TEST,
D OUTPUT GATING NO. 1 MODULE

CODE IDENT NO.	SIZE	DRAWING NO.
96214	A	514720

SCALE WT SHEET 1 of 9

TI-1E1793-A

TABLE OF CONTENTS

1. TABLE OF TESTS

		Paragraph No.
1.1	Preparation	3.1
1.2	Room Temperature Test	3.2
1.3	Low Temperature Test	3.3
1.4	High Temperature Test	3.4

2. LIST TEST EQUIPMENT

2.1 Data Sheets (TI Drawing 514727) shall be completed as part of this test.

2.2 Verify that equipment designated working standard, or better, is currently certified per TI Std. Procedure No. 12-28.

2.3 Commercial Test Equipment - The following commercially available test equipment (or equivalent) is required to complete the test required by this specification.

2.3.1 Oscilloscope - Tektronix 543/Plug-in Type CA.

2.3.2 Power Supply - Sorenson T50-1.5.

2.3.3 Pulse Generator - TI Model 6563.

2.3.4 Temperature Chamber - TI Controlled Environmental Unit.

2.4 Special Test Equipment - The following special test equipment is required to complete the test required by this specification.

2.4.1 Test Set, Module, TI Drawing 514711.

2.4.2 Control Box, TI Drawing 514713.

2.4.3 Five Stage Counter, TI Drawing 514714.

3. TEST PROCEDURES

The following test procedure covers the module test requirements to evaluate the D Output Gating No. 1 Module of the Integrated Circuit Sequence Generator.

3.1 Preparation

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

SYM.

CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514720	
SCALE	WT		SHEET 3

TI-5419

3.1.1 Visually inspect module for any mechanical faults such as wiring mistakes, broken leads, bad welds, etc.before plugging module into test set.

3.1.2 Adjust V_{CC} supply voltage to 3.1 VDC ±0.1 VDC.

3.1.3 Adjust pulse generator for a positive going pulse (50 nsec to 500 nsec wide). from 0 to +3V ±0.1V at a rate of 1 mc ±50KC with rise and fall times at a minimum (minimum ringing at 0 and +3 volts).

CAUTION: Only a positive going signal is to be applied to these modules.

3.1.4 Plug module into test set.

3.1.5 Connect GRD to TP 26 of control box.

3.1.6 Connect V_{CC} to TP 25 of control box.

3.1.7 Connect test set to control box.

3.1.8 Connect five stage counter to control.box as follows.

	Counter	Control Box
a.	S_1	T.P. 2 (D_1)
b.	S_2	T.P. 16 (D_2)
c.	$\overline{S_2}$	T.P. 8 ($\overline{D_2}$)
d.	S_3	T.P. 1 (D_3)
e.	$\overline{S_3}$	T.P. 10 ($\overline{D_3}$)
f.	S_4	T.P. 3 (D_4)
g.	$\overline{S_4}$	T.P. 11 ($\overline{D_4}$)
h.	S_5	T.P. 24 (D_5)
i.	$\overline{S_5}$	T.P.18 ($\overline{D_5}$)

Note: Oscilloscope should be triggered on the positive going edge of $\overline{S_5}$ of the five bit counter.

3.2 Room Temperature Test

3.2.1 Performance Test No. 1

a. Connect the following test points to GRD.

1. T.P. 4 (D_6)
2. T.P. 12 (D_7)

b. Connect V_{CC} to the following test points.

1. T.P. 9 ($\overline{D_6}$)
2. T.P. 5 ($\overline{D_7}$)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.

1. 3	T.P. 6
2. D	T.P. 17
3. $\overline{D}$	T.P. 21

3.2.2 Performance Test No. 2

a. Connect the following test points to GRD.

1. T.P. 9 ($\overline{D_6}$)
2. T.P. 12 (D_7)

b. Connect the following test points to V_{CC}.

1. T.P. 4 (D_6)
2. T.P. 5 ($\overline{D_7}$)

c. Osberve the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.

1. 3	T.P. 6
2. D	T.P. 17
3. $\overline{D}$	T.P. 21

3.2.3 Performance Test No. 3

a. Connect the following test points to GRD.

1. T.P. 4 (D_6)
2. T.P. 5 ($\overline{D_7}$)

b. Connect the following test points to V_{CC}.

1. T.P. 9 ($\overline{D_6}$)
2. T.P. 12 (D_7)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.

1.	3	T.P. 6
2.	D	T.P. 17
3.	$\overline{D}$	T.P. 21

3.2.4 Performance Test No. 4

a. Connect the following test points to GRD.

1. T.P. 9 ($\overline{D_6}$)
2. T.P. 5 ($\overline{D_7}$)

b. Connect the following test points to V_{CC}.

1. T.P. 4 (D_6)
2. T.P. 12 (D_7)

c. Observe the outputs of the module on the oscilloscope. See Diagram, Section 4, and Table I, Section 5.

1.	3	T.P. 6
2.	D	T.P. 17
3.	$\overline{D}$	T. P. 21

3.3 Low Temperature Test

3.3.1 Precool temperature chamber to -25°C. Place test set, with module plugged-in, inside and allow one half hour for stabilization.

3.3.2 Repeat 3.2.1.

3.3.3 Repeat 3.2.2.

3.3.4 Repeat 3.2.3.

3.3.5 Repeat 3.2.4.

3.4 High Temperature Test

3.4.1 Preheat temperature chamber to +100°C. Place test set, with module plugged-in, inside and allow one half hour for stabilization.

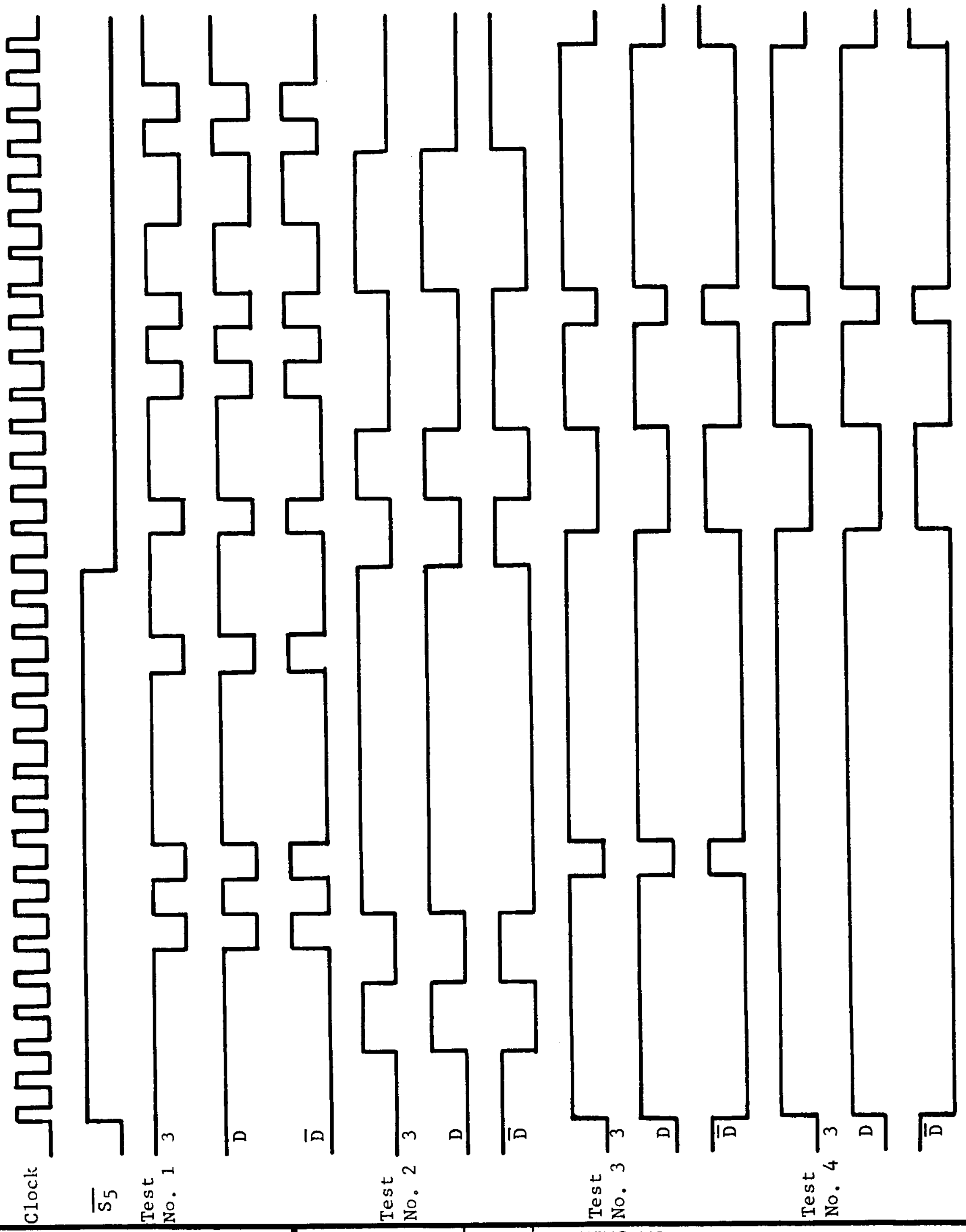
3.4.2 Repeat 3.2.1.

3.4.3 Repeat 3.2.2.

3.4.4 Repeat 3.2.3.

3.4.5 Repeat 3.2.4.

4. DIAGRAMS



TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS, TEXAS	CODE IDENT NO. 96214	SIZE A	DRAWING NO. 512720
SYM.	SCALE	WT	SHEET 8

TI-5419

5. TABLE I

Performance Test	Function	Output
No. 1	3	11111010111110111011101011001011
	D	11111010111110111011101011001011
	$\overline{D}$	00000101000001000100010100110100
	$\overline{S_5}$	11111111111111110000000000000000
No. 2	3	00110011111111110011000011110000
	D	00110011111111110011000011110000
	$\overline{D}$	11001100000000001100111100001111
	$\overline{S_5}$	11111111111111110000000000000000
No. 3	3	11111110111111110001110111111110
	D	11111110111111110001110111111110
	$\overline{D}$	00000001000000001110001000000001
	$\overline{S_5}$	11111111111111110000000000000000
No. 4	3	11111111111111110001110111111110
	D	11111111111111110001110111111110
	$\overline{D}$	00000000000000001110001000000001
	$\overline{S_5}$	11111111111111110000000000000000

A 514721

DASH NO.	QTY	NEXT ASSY NO.	SIZE	PROJ NO.
				464

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

INSPECTION TEST PROCEDURE

PART I

INDIVIDUAL TEST

FOR

X, A, B, C, AND E CODE SEQUENCE GENERATOR MODULES

INTEGRATED CIRCUIT SEQUENCE GENERATOR

CONTRACT NO. 950693

MANUFACTURER- TEXAS INSTRUMENTS INCORPORATED

TEST DATA SHEET 514728 TO BE FILLED OUT AS PART OF THIS TEST PROCEDURE

QTY REQD -2	QTY REQD -1	ITEM NO.	DWG SIZE	PART OR IDENTIFYING NO. TEXAS INSTRUMENTS	PART OR IDENTIFYING NO. GOVT OR INDUSTRY	NOMENCLATURE OR DESCRIPTION

LIST OF MATERIALS

	DATE
DR jc/	3/25/64
CKD H. Miller M	5-26-64
ENGR Fred Clark	5/13/64
APPD W. D. Thomas	5-23-64
DESIGN ACTIVITY RELEASE	5-27-64

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

TITLE
TEST PROCEDURE, INSPECTION,
PART I,
INDIVIDUAL TEST,
X, A, B, C, AND E CODE SEQUENCE GENERATOR
MODULES

CODE IDENT NO.	SIZE	DRAWING NO.
96214	A	514721

SCALE	WT	SHEET
		1 of 7

TI—1E1793-A

TABLE OF CONTENTS

		Paragraph No.
1.	TABLE OF TESTS	
1.1	Preparation	3.1
1.2	Room Temperature Test	3.2
1.3	Low Temperature Test	3.3
1.4	High Temperature Test	3.4

2. LIST OF TEST EQUIPMENT

2.1 Data Sheets (TI Drawing 514728) shall be completed as a part of this test.

2.2 Verify that test equipment designated WORKING STANDARD, or better, is currently certified per TI Std. Procedure No. 12-28.

2.3 Commercial Test Equipment - The following commercially available test equipment (or equivalent) is required to complete the tests required by this specification.

2.3.1 Oscilloscope - Tektronix 543/Plug in type CA

2.3.2 Power Supply - Sorenson T50 - 1.5

2.3.3 Pulse Generator - TI Model 6563

2.3.4 Temperature Chamber - TI Controlled Environmental Unit

2.4 Special Test Equipment - The following special test equipment is required to complete the tests required by this specification.

2.4.1 Test Set, Module, (Red, White, Green Connector), TI Drawing No. 514710.

2.4.2 Control Box, TI Drawing No. 514712.

3. TEST PROCEDURES

The following test procedures cover the module test requirements to evaluate the X, A, B, C, and E Code Sequence Generator Modules of the Integrated Circuit Sequence Generator.

TEXAS INSTRUMENTS
INCORPORATED
APPARATUS DIVISION DALLAS, TEXAS

CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514721	
SCALE	WT		SHEET 3

SYM.

TI-5419

3.1 Preparation

3.1.1 Visually inspect module for any mechanical faults such as wiring mistakes, broken leads, bad welds, etc. before plugging module into test set.

3.1.2 Adjust V_{CC} supply voltage to 3.1V.D.C. ±0.1V.D.C.

3.1.3 Adjust pulse generator for a positive going pulse (50 nsec to 500 nsec wide) from 0 to +3V ±0.1V at a rate of 1 mc ±50KC with rise and fall times at a minimum (minimum ringing at 0 and 3V).

CAUTION: Only a positive-going signal is to be applied to these modules.

3.1.4 Plug module into test set.

a.	X Code Generator	Red Connector
b.	A Code Generator	White or Green Connector
c.	B Code Generator	White or Green Connector
d.	C Code Generator	White or Green Connector
e.	E Code Generator	White or Green Connector

3.2 Room Temperature Test

3.2.1 Connect test set to control box.

3.2.2 Observe the outputs of the module under test on oscilloscope at the test points on the control box. See Diagram, Section 4, and Table I, Section 5.

	Output	Test Point
a.	X Code	Red 1
b.	$\overline{X}$ Code	Red 2
c.	X Word	Red 3
d.	CL	Red 4
e.	$\overline{CL}$	Red 5
f.	S.P.	Red 6
g.	T	Red 7

	Output	Test Point	
h.	A Code	White 6	Green 6
i.	$\overline{A}$ Code	White 2	Green 2
j.	A Word	White 5	Green 5
k.	B Code	White 5	Green 5
l.	$\overline{B}$ Code	White 6	Green 6
m.	B Word	White 4	Green 4
n.	C Code	White 3	Green 3
o.	$\overline{C}$ Code	White 5	Green 5
p.	C Word	White 1	Green 1
q.	E Code	White 3	Green 3
r.	$\overline{E}$ Code	White 5	Green 5
s.	E Word	White 6	Green 6

NOTE: More than one module may be tested at a time. The outputs of the modules under test will appear at test points corresponding to the color of the module connector. The oscilloscope should be triggered on the positive-going edge of the module word under test.

3.3 Low Temperature Test.

3.3.1 Precool temperature chamber to -25°C. Place test set, with module plugged in, inside and allow one half hour for stabilization.

3.3.2 Repeat paragraph 3.2.1.

3.3.3 Repeat paragraph 3.2.2.

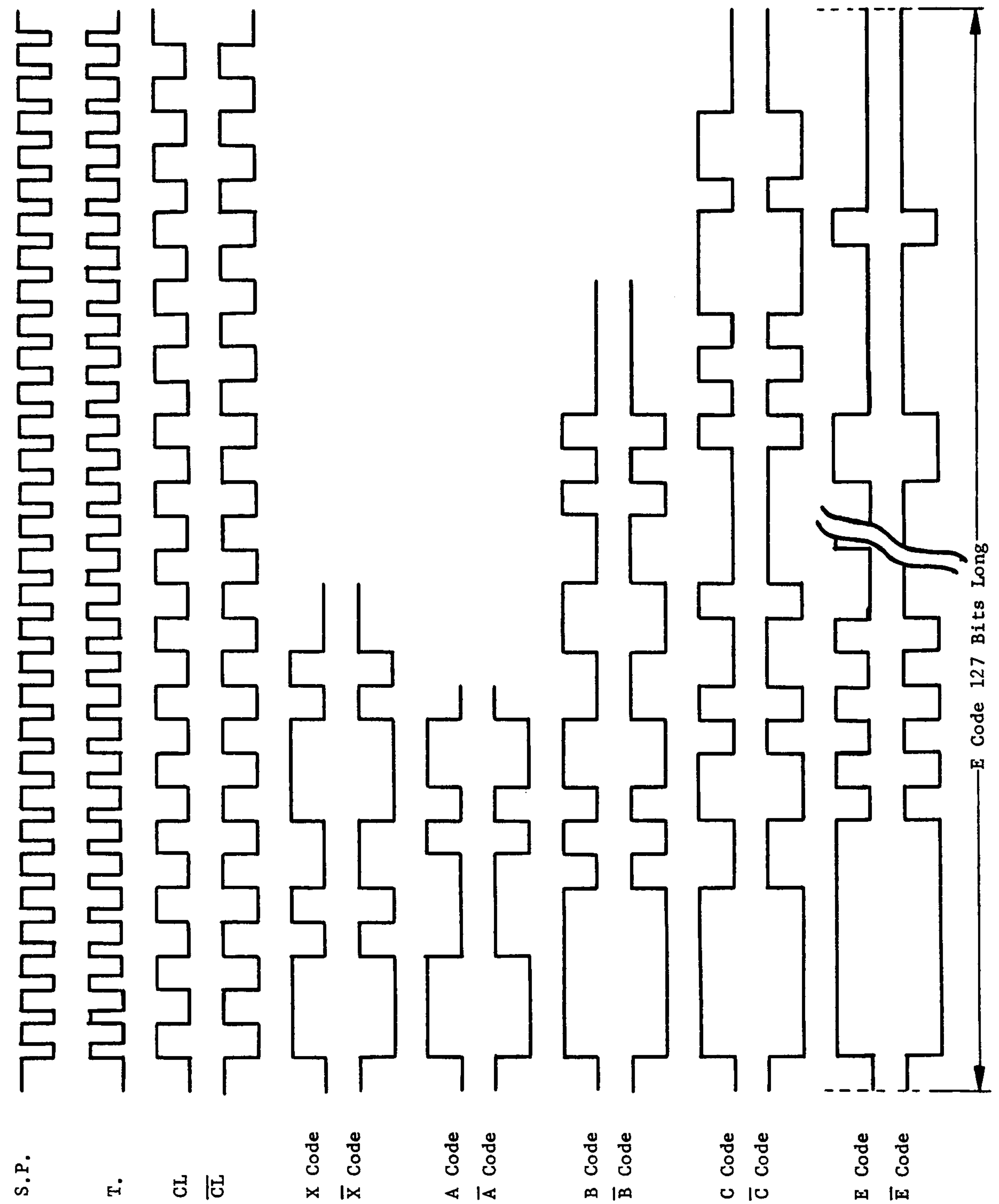
3.4 High Temperature Test

3.4.1 Preheat temperature chamber to +100°C. Place test set, with module plugged in, inside and allow one half hour for stabilization.

3.4.2 Repeat paragraph 3.2.1.

3.4.3 Repeat paragraph 3.2.2.

4. DIAGRAMS



TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS, TEXAS	CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514721
SYM	SCALE	WT	SHEET 6

TI-1E1793-1-A

5. TABLE I

Function	Output
X Code	1110100
$\overline{X}$ Code	0001011
CL	10
$\overline{CL}$	01
A Code	11100010110
$\overline{A}$ Code	00011101001
B Code	11111010110011001010000
$\overline{B}$ Code	00000101001100110101111
C Code	1111100110100100001010111011000
$\overline{C}$ Code	0000011001011011110101000100111
E Code	11111110101010011001110111010010110001101111011010 11011001001000111000010111111001010111001101000 1001 1110001010000110000001000000
$\overline{E}$ Code	00000001010101100110001000101101001110010000100101 00100110110111000111101000000110101000110010111 0110 0001110101111001111110111111

TEXAS INSTRUMENTS INCORPORATED APPARATUS DIVISION DALLAS, TEXAS	CODE IDENT NO. 96214	SIZE A	DRAWING NO. 514721
SYM.	SCALE	WT	SHEET 7