Master's thesis

NTNU
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Kunnskap for en bedre verden

Department of Electronic Systems

Master Thesis

# RF Envelope Tracker

# A Hybrid DC-DC Converter, Utilizing a High-side Gate Charge-pump and Digital Logic Current Control for RF PA's

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# Abstract

In radio frequency (RF) transmitters, the largest portion of energy is lost in the power amplifier (PA). This is dude to the constant demand for higher data rates that has produced modulation schemes of increasing complexity. PA's can be made efficient, however, current modulation schemes incorporate input signals that have a varying amplitude, and therefore require PA's to run in hard back-off. This forces the overall system to be less efficient. Envelope tracking is the chosen technology of this investigation, where as others such as envelope-elimination and restoration (EER) pose too many non-linearity's. Envelope tracking involves the dynamic modulation of the drain voltage of a RF PA (transistor) that holds the active device in or around its $1dB$ compression point; this boosts the efficiency. However, the tracker itself must therefore be efficient to make it work the extra complexity. This is the narrative of the project where a hybrid solution is investigated. The switch-mode circuit takes care of the bulk of the RF power located at lower frequencies ($0Hz - 1MHz$), leaving the linear regulator to handle the higher frequencies ($1MHz - 80MHz$) where efficiency is not as critical. A pre-existing masters project is used to create a proof of concept prototype ($Tracker_{011}$) in KiCad that is manufactured, and verified. The results yield problems associated with the non-inverting linear regulator; it could not handle the current load. A simulation is then constructed using Ngspice, and KiCad to simulate the prototype using accurate component models; this verifies the incorrect current loading. Two other points are also noted, where the gate-source voltage of the high-side switch is on average only $\approx 3.7V$, and that gate driving signal is highly proportional to the input signal. This make the high-side switch act as a source follower; this is not efficient. From the investigation of $Tracker_{01X}$ the innovation section is introduced employing low-voltage digital control, charge pumps and emitter-followers to combat the problems associated with the first architecture. With an excitation signal of $1MHz$, all of the circuits show sub $300mW$ operation with correct transient characteristics. The innovation is then compiled into the final tracker architecture ($Tracker_{021}$). While the second revision functions up to $100kHz$, correct gain of $2.95\frac{V}{V}$, and shows promising transient behaviour the average efficiency is poor at $\approx 30\%$. At $1MHz$ and higher, the switch-mode regulator stops to function, as intended, to allow the linear regulator to take care of the higher frequencies. An average gate-source voltage of $\approx 9.9V$ is obtained with the new revision, and is the reason for the larger anti-ripple inductor. The gate voltage of the high-side switch is also broader in frequency, which should cause the switching frequency to be spread out over the spectrum, thereby reducing its impact. The digital logic circuit consumes a staggering $2.6kW$'s. This eludes to a $5m\Omega - 10m\Omega$ load and is cause for concern although it is not understood; the contribution of this unit is not accounted for in the efficiency calculation. The current load of the non-inverting linear regulator is removed resulting in the linear regulator being independent of the switch-mode. Interesting points for future work are to increase the voltage gain of the comparator, developing reset circuity for the charge pump and using parallel high-side switches with differing output inductors to improve the output ripple.

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Table 1: Table of abbreviation.

| Parameter | Abbreviation |
|---|---|
| Alternating Current | AC |
| AC Voltage Gain | $A_v^{AC}$ |
| Collector Current Gain | $\beta$ |
| Bias-junction Transistor | BJT |
| DC Voltage Gain | $A_V^{DC}$ |
| Direct Current | DC |
| Duty Cycle | D |
| Envelope Tracking | ET |
| Transconductance | $G_m$ |
| Integrated Circuit | IC |
| Metal-oxide Field-effect Transistor | MOSFET |
| N-type BJT | NPN |
| N-type MOSFET | N-channel |
| Operational Amplifier | OPAMP |
| P-type BJT | PNP |
| P-type MOSFET | P-channel |
| Printed Circuit Board | PCB |
| Radio-frequency | RF |

# 1 Introduction

Wireless communication is an attractive means of connecting data infrastructure in the modern digital world. While radio-frequency (RF) power-amplifiers (PA), that run on frequency modulation, can be optimised to be $\approx 90\%$ efficient, the demand for high data-rate applications are causing the continued growth in modulation signal complexity. Consequently, modulation schemes may now include both frequency and amplitude modulation that result in added spectral efficiency, utilising a broader bandwidth, causing higher peak-to-average power ratios. One example is the Enhanced data rates for GSM evolution (EDGE) modulation schemes that increase the spectral efficiency by modulating the amplitude of the information stream. This equates to modulation signals that have a large dynamic range, due to the device needing to run in hard back-off to avoid non-linear clipping, therefore making efficiency a problem. One example includes CDMA reverse-links, or handsets, that have an output signals that may vary between $50db - 70db$ within one millisecond. This is particularly a problem with battery powered applications, where the largest portion of energy lost may be due to the on-board radio-frequency (RF) power-amplifier (PA). Pressure is therefore put on hardware engineers to develop new methods of maintaining power-amplifier efficiency whilst delivering the expected data rates of the modern era.

There exists efficiency boosting methods like parallel PA architectures such as Doherty, and Chireix, however, while showing effective boosts in efficiency with adequate linearity, they rely on resonance, and can only accommodate 10.0% changes in bandwidth. Two other technologies are envelope-elimination and restoration (EER), and envelope tracking. These approaches dynamically modulates the drain of the RF PA to keep the active device close to or past its $1dB$ compression point; this increases the efficiency. Envelope tracking is a simpler version of EER, where instead of both amplitude and phase modulation being extracted, only the amplitude portion is taken to produce a proportional drain voltage for the RF PA. Choosing amplitude modulation to steer the envelope tracking system has the added benefit of improving the linearity of the operation as it avoids clipping. EER on the other hand removes the envelope of the input signal, leaving a constant amplitude composed of the phase information, whilst re-applying the envelope to the output signal by modulating the PA's voltage supply according to the envelope; this method is highly non-linear since the PA is in hard saturation leaving envelope tracking as the point of interest for this project.

Envelope tracking is achieved using regulation circuity to create an ideal current source at the drain of the RF PA; the drain voltage should not fluctuate with dynamic loading. Regulation architectures include both linear (transistors), and switch-mode methods (buck or boost converters) where those of the linear class are fast, and linear, however, lack in efficiency. Switch-mode methods on the other hand are more efficient, but are less linear, and struggle with switching losses when the control frequency is increased. The compromise between the two is the narrative of this investigation, where the trade-offs between the two approaches are put against each-other to create a hybrid system that utilises the benefits of both where necessary. This project investigates the feasibility of a hybrid DC-DC converter with respect to output transient behaviour, efficiency, speed, and complexity, for the application of improving RF PA devices through means of dynamically controlling their drain proportionally to the input envelope amplitude [1].

The report first arms the reader with the necessary theoretical tools needed for the design, analysis, and discussion. Also, within the theory section the differing system requirements are specified to serve as a guide for the development of electrical hardware in the design phase. Once the conceptual bases are covered, the narrative moves onto the design of the circuity needed to fulfill the specification previously defined. There are three main developments during the design section. One is the design of the initial prototype ($Tracker_{011}$), the innovation section that focus on solving the problems of the latter, and the final tracker architecture ($Tracker_{021}$). The report thereafter moves onto present the results of each contributing design, before they are used by the discussion to comment on their significance. Trailing the discussion is the future work, where motivation is handed down to continue this investigation, leaving a summary of the project's narrative in the conclusion.

# 2 Theory

The aim of this section is to arm the reader with enough information to gain a developing understanding of the concepts related to the design and operation of this investigation. The theory section begins with the two most relevant RF topics; radio-amplifiers and envelope tracking followed by a summary of the key points. Following is a brief breakdown of operational amplifiers (OPAMPS), and the basic properties of transistors. The theory section is concluded with a brief overview of digital control logic, and the simulation software utilised in this project. Note that the radio amplifier, and envelope tracking sections are motivated by an existing masters project [1].

## 2.1 Radio Amplifier

The point of this section is to express that there is not one optimal system; there will always be a compromise that is governed by the following topics. It is also assumed that modulation schemes, such as enhanced data rates for GSM evolution (EDGE), that include amplitude, and phase encoded information, are used together with the PA.

### 2.1.1 Compression

Compression is the mission of envelope tracking, and describes the point when a transistor can no longer produce an output proportional to the input. The $1dB$ compression point is used to define this point, and is extremely important in the device's specification since the amplifier no long has a linear relationship to the input. An example of amplifier compression is seen in Figure 1, where the output increases linearly with respect to the input. Although operating the amplifier past this point causes increased inter-modulation products, harmonics, and distortion (the device is no longer linear), the point precisely before the $1dB$ is of great importance, and leads into the next topic.

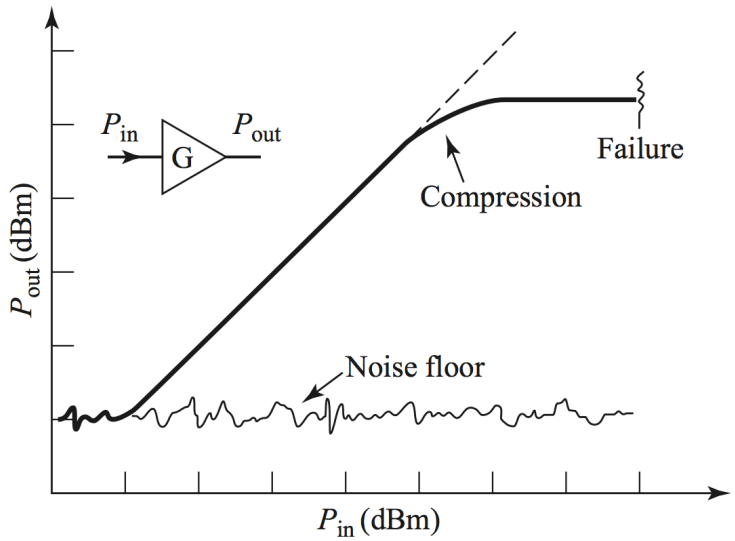


Figure 1: The $1dB$ compression point, where the linear output deviates from the input by $1dB$, is illustrated in the figure above as a function of input and output power with respect to the noise floor.

### 2.1.2 Efficiency

Power added efficiency (PAE) shows how much the direct current (DC) source of the amplifier contributes to the amplified input signal; this is show in Figure 2.

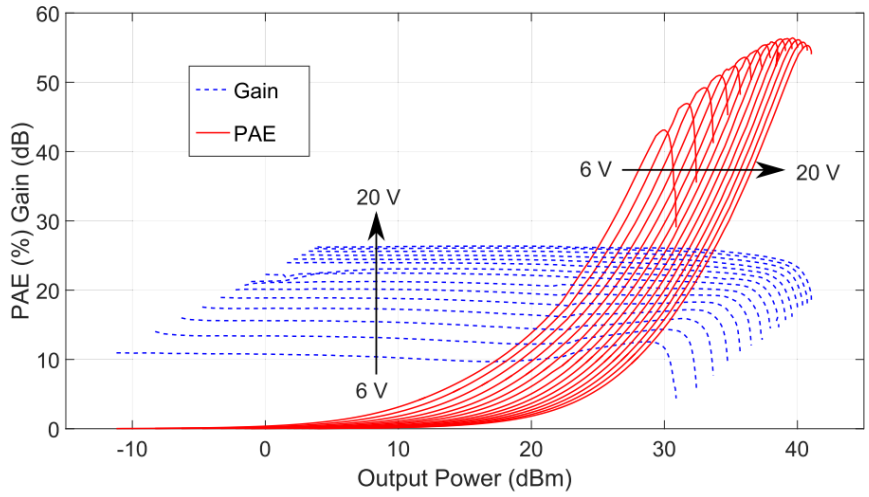


Figure 2: The PAE of a supply modulated power amplifier as a function of output power; a supply voltage of $6V$ is stepped ($1V/$ step) up to $20V$; the resulting efficiency curves are then observed.

Considering Figure 2 with (Figure 1), shows that the crest of maximum PAE coincides with the $1dB$ compression point. This makes intuitive sense, as compression dictates the point where the amplifier can no longer do what is expected, and saturates. If the input is then increased further, past the compression point, then there is a net negative effect; this is visually seen by the dipping slope following the crest. The point of this section is to state that maximum efficiency is obtained by running the amplifier in the region to the $1dB$ compression point. The reason why this is not always possible in conventional amplifier systems is covered in the next topic.

### 2.1.3 Dynamic Range

Amplifiers can work efficiently ($\approx 78.5\%$ for $class - B$) by tailoring the circuit to place the amplifier's output near its compression point. This in reality is not possible due to modulation schemes that require PAs' to run in hard back-off. Consequently this forces the overall system to be less efficient, and is a nightmare for radio hardware engineers; it does, however, ensure future employment. Envelope tracking is the method used in this investigation to combat the problem of dynamic range.

### 2.1.4 Transistor Impedance

Before moving on, it is important to understand the dynamic characteristics of RF amplifiers. These devices are at heart semiconductor technology that do not have a constant impedance over their workable frequency range. This creates problems for matching networks, filter responses, and will change the behaviour of external systems such as an envelope tracker. For the application of this project, the transistor is assumed to be an ideal $50\Omega$ load.

## 2.2 Envelope Tracking

Envelope tracking is one prospect technology with the potential to improve the efficiency of amplifier devices that incorporate modulation schemes using a large dynamic range. The punch-line of envelope tracking is to dynamically control the voltage applied to the supply of the amplifier (transistor), that is proportional to the input, so that the amplifier keeps its operating point close to its $1dB$ compression point; this increases the efficiency of the system. The general concept of using envelope tracking with respect to radio amplifiers is presented in Figure 3. The figure shows how the envelope signal, taken from the modulated RF signal, is used to control the tracker block. The tracker amplifies the amplitude modulated envelope to produce a proportional output to supply the radio amplifier. The discussion in the following sections outline the different regulation technologies, and specification requirements regarding power, bandwidth, signal delay, and output voltage ripple.

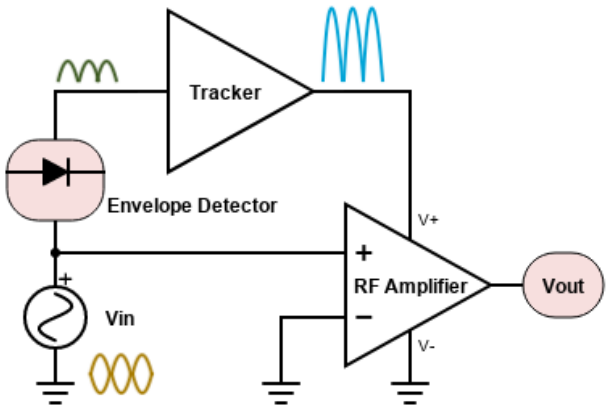


Figure 3: The figure shows the top-view circuit position of the envelope tracker with respect to the radio amplifier, where the envelope detector extracts the envelope from the signal input, the tracker thereafter amplifies the envelope before delivering it to the RF amplifier.

### 2.2.1 Linear Regulation

Linear regulation can be described using a voltage divider with two resistors; the top resistor is variable; these resistors are internally native to the regulator. A linear regulator can change the top resistor so that its output voltage is proportional to its current input; usually through feedback. The voltage difference between the output, and the supply, multiplied by the current load, is the power converted to heat. In short, linear regulators burn the voltage difference between the output and the supply; this is extremely in-efficient. The power loss for linear regulators is presented in Equation 1, where $P_{loss}$ is the power dissipated into heat internally, $V_{supply}$ is the supply voltage of the regulator, $V_{out}$ is the output voltage, and $I_{out}$ is the load current. This regulator topology is most effective when its output is near the voltage supply, and is less efficient when it must output a smaller voltage; linear regulation is not desired for high power applications. Note that acceptable efficiency performance is achieved when the device is operated near its supply; this is the key point that the following topic builds on.

$$P_{loss} = (V_{supply} - V_{out}) \cdot I_{out} \tag{1}$$

### 2.2.2 Switch-Mode Regulation

Switch-mode regulators are more efficient than linear regulators since they are either on or off. This method tacks advantage of the small conduction loss ($R_{on}$) of semiconductors, whilst completely eliminating the need to burn voltage differences internally. Passive components are used to smooth out the harsh voltage transitions to acceptable output ripple values. Conventional pulse-width-modulation (PWM) uses a switching frequency to control the average output voltage. The unusable power lost to heat by the device is seen in Equation 2, where $P_{loss}$ is the power lost to heat, $R_{ds}$ is the internal conducting resistance of the device, and $I_d$ is the conducting current through the device; $R_{ds}$ is typically in the $m\Omega$ range. The inherent advantage of this regulator architecture is increased efficiency, at the expense of linearity. Switch-mode regulation must operate in a defined bandwidth, and thus is naturally the next topic to be covered.

$$P_{loss} = R_{ds} \cdot I_D^2 \tag{2}$$

### 2.2.3 Bandwidth

According to the Equation 3 and Equation 4, the envelope's bandwidth is infinite. This creates a problem for reaching 100% efficiency; infinite bandwidth is not possible. The high power tracking bandwidth must be at least three times the base-band signal. Despite this, in the case for Enhanced Data Rates for GSM Evolution (EDGE) common to digital communication, 85% of the signals total power is associated with the spectrum's DC component, as can be seen in Figure 4. The magnitude of the envelope at higher frequencies is much smaller than at low frequencies; this is of significance for the eventual tracker architecture. Power envelope tracking (PET) is a solution for infinite bandwidth.

$$v_{envelope} = |v_s(t)| = \sqrt{v_I(t)^2 + jv_Q(t)^2} \implies BW_{env} = \infty, \text{ where,} \tag{3}$$

$$v_s(t) = v_I(t) + j \cdot v_Q(t) \implies BW = \frac{BW_{RF}}{2} \tag{4}$$

PET is created by taking a power series expansion of the envelope signal, and thereafter taking a given number of coefficients of an even order. This new signal will therefore emulate the portion of the spectrum that contains the majority of the power, reducing bandwidth requirement; this is shown in Figure 4.

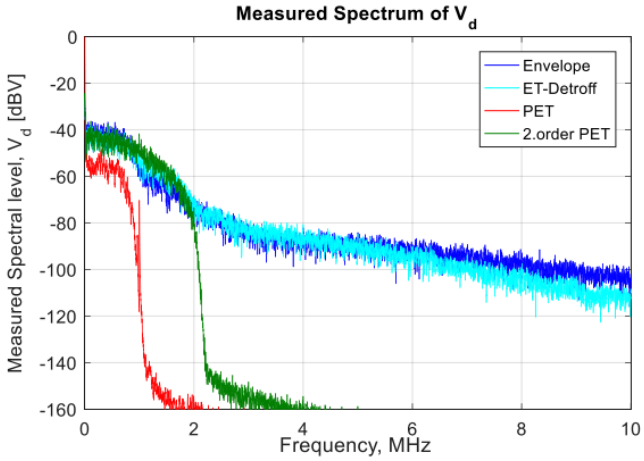


Figure 4: The spectrum above (*darkblue*) shows how the bandwidth of the envelope is infinite in nature, along with the three different bandwidth reduction techniques.

Referring to Figure 4, a good approximation of the envelope's bandwidth can be made by noting at which point the magnitude of the envelope falls below a given value. For example, when the magnitude falls below $-80dB$ at $5MHz$, this provides acceptable tracking performance. The effect of this bandwidth relaxation is presented in Figure 5, where the power envelope tracker (PET) cannot fully track the input signal in the large dips; efficiency is therefore lost in these areas, as the PA will operate in back-off.

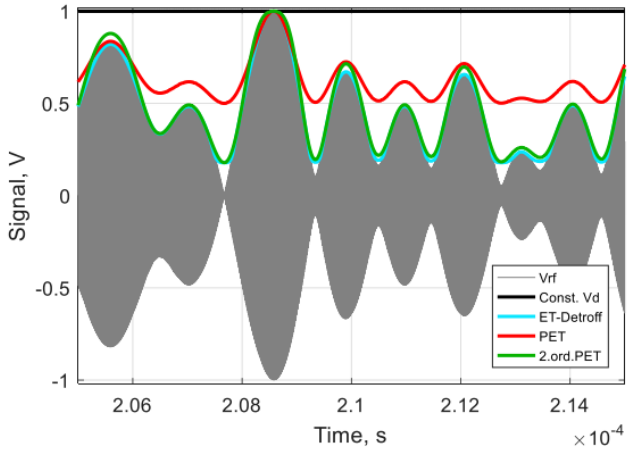


Figure 5: The figure above shows the variation in applying different bandwidth limiting techniques for envelope tracking control hardware; increasing the order of the PET envelope approximation will improve the tracking performance.

### 2.2.4 Delay

The resulting tracking supply signal will naturally be time delayed with respect to the input signal, and will cause the PA to potentially enter hard compression on the leading edge of the input signal resulting in distortion, and then over compensate on the trailing edge potentially putting the PA into hard back-off resulting in reduced efficiency. This problem can be mitigated using pre-distortion via digital signal processing (DSP), although the cost, complexity and calibration overheads of the system are likely to increase. The solutions associated with pre-distortion are not considered in this project.

### 2.2.5 Voltage Ripple

Voltage ripple is used to characterise the extent to which the output voltage of the regulator varies from its average value. Voltage ripple is an unavoidable product of switch-mode regulation, and its influence can only be mitigated to acceptable magnitudes through the use of filters in the form of capacitors, inductors', or active devices. While capacitors try to maintain steady voltage through applying electric fields, inductors strive to maintain constant current by using magnetic fields; active devices, such as linear regulators, will drive a set point through the use of feedback.

## 2.3 Summary

The dynamic range of RF PA's kill their efficiency, where envelope tracking is a potential solution by noticing the efficiency gains surrounding compression. A hybrid tracking system, composed of both a linear and switch-mode regulator, for the high and low frequencies respectively is introduced. It must, however, perform according to the specification in Table 2. This summary concludes the theory around RF and PA concepts. The report now hops over to cover the basics of operational amplifiers.

Table 2: Specification for the hybrid tracker architecture

| Parameter | Abbreviation | Value | Unit |
|---|---|---|---|
| Input Voltage | *input* | 2-10 | V |
| Output Voltage | *output* | 6-28 | V |
| Switching Bandwidth | $BW_{switch}$ | 0-1.0M | Hz |
| Linear Bandwidth | $BW_{linear}$ | 0.0-80M | Hz |
| Efficiency | $\mu$ | 70-100 | % |
| Load | $R_{load}$ | 50 | Ω |
| Power | $P_{load}$ | 22 | W |

## 2.4 Operational Amplifiers

Operational amplifiers (opamps) are legacy devices that were first used in early computers to perform mathematical operations. Today, this task has been largely taken over by dedicated processor chips, however, opamps remain useful devices due to their ability to output a voltage proportional to the difference between its input terminals. They also exhibit large input impedance's for its input terminals, and a low output impedance for driving loads. The ideal circuit model for the OPAMP is presented in Figure 6, where the triangle denotes the component case, voltage sources $V+ \& V-$ are the two voltage potentials present at the two input terminals ($V+$) and ($V-$), and Zin and Zout is the OPAMP's internal input and output impedance's, Rload is the output load resistor, the voltage dependent voltage source models the linear output voltage gain, and Vss+/Vss- are the two supply voltages for the OPAMP.

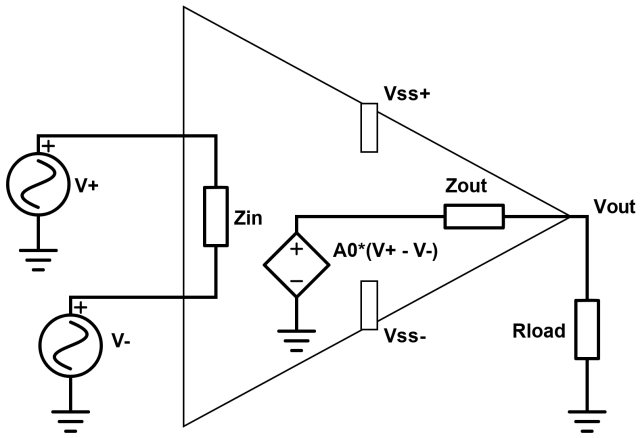


Figure 6: The linear operational amplifier model showing the applied input voltages ($V+$ & $V-$), the internal input terminal impedance (Zin), the internal output inpedance (Vout), and external load impedance (Zload). The voltage controlled output voltage source is described by $A0 \cdot (V^+ - V^-)$.

While OPAMP's may be used in a fully differential manner, this project considers purely single ended implementations, and is therefore the nature of this section. The two supply terminals ($Vss+$ & $Vss-$) are referenced to a positive supply and ground (0V) respectively, as are the input terminals ($V+$ & $V-$). Zin is ideally $\infty\Omega$, while Zout is ideally $0\Omega$, with the open-loop gain (A0) $\approx \infty$ for all frequencies. In reality this is not the case and the THS3001 is used as an example. The input impedance is $\approx 1.5M\Omega$, the output impedance is $\approx 10\Omega$ at $5.0MHz$, and the small-signal bandwidth whilst having a closed-loop gain of five and a supply voltage of $\approx 30V$, is $\approx 350MHz$ [2]. The main concept of the OPAMP is that it will produce a proportional output voltage with respect to the difference between it's input terminals; this is described by the voltage dependent voltage source, and it's corresponding equation $A0 \cdot (V + -V-)$. The resulting output voltage of the OPAMP must not exceed the range of the provided supply voltage, where the output voltage is described by Equation 5.

$$V_{out} = A0 \cdot (V^+ - V-) \cdot \frac{R_{load}}{R - load + Z_{out}} \tag{5}$$

This is, however, the open-loop response, and requires the voltage difference between the two input terminals to be very small so that the output voltage does not saturate at one of its two rails ($Vss+$ & $Vss-$). The open-loop response is engineered to have the characteristics of a low-pass filter, and therefore producing a bandwidth of equal to the $3dB$ corner frequency of the first pole. The gain and bandwidth of OPAMP's are design points and must be correctly set. This is done through the use of negative feedback, and is discussed in the next section [3].

### 2.4.1 Feedback

Negative feedback is an important concept in the development of OPAMP circuits, where the gain and bandwidth of the system can be manipulated by applying a negative feedback path from the output of the OPAMP to its corresponding inverting input terminal; this may be visually depicted in Figure 7. From this figure, a output relation with respect to it's input may be defined to further understand the effect of feedback by understanding the input/output relationship with respect to the feedback loop-gain $\beta$ (BETA), and the open-loop gain A(s).

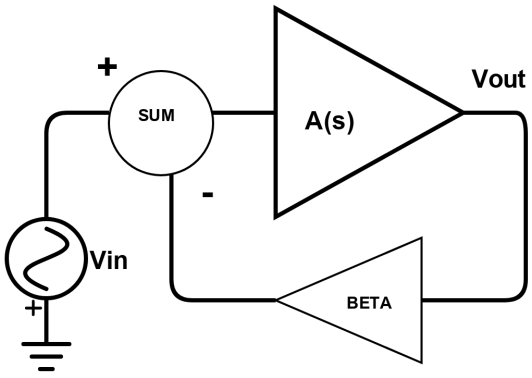


Figure 7: The concept of amplifier feedback is presented, where the main amplifier gain is described by $A(s)$, the feedback factor ($\beta$), the summing node $SUM$, the input signal ($V_{in}$), and the output signal $V_{out}$. This figure is used to derive the closed-loop transfer function.

By visual observation, the output voltage expression may be described by $V_{out} = A(s) \cdot (V_{in} - \beta \cdot V_{out})$, and with some manipulation, can be written as Equation 6. $A_v^{Cl}$ is the closed-loop voltage gain, and $LG_V$ is the voltage loop gain expressed in Equation 7.

$$A_V^{CL} = \frac{A(s)}{1 + A(s) \cdot \beta} = \frac{A(s)}{1 + LG(s)} \tag{6}$$

$$LG_V = A(s) \cdot \beta \tag{7}$$

Considering Equation 6, if the feedback factor $\beta$ is assumed to be much greater than 1.0, then the equation may be reduced to $\frac{1}{\beta}$. In doing this the overall system's gain and bandwidth is altered, and can be visually seen in Figure 8. The red dashed line is the open-loop (OL) response with $A(0)$ describing the open-loop $\approx DC$ voltage gain, with its first pole ($Wp1^{OL}$) denoting its bandwidth ($BW^{OL}$). The same is for the closed-loop (CL) response where the suffix is denoted with "CL" opposed to "OL", and its close-loop $\approx DC$ voltage gain given by $\frac{1}{\beta}$. It can be seen that with the addition of the feedback network, the overall gain of the system is equivalent to that of the feedback network, and is therefore smaller, however, the system has increased its bandwidth by a

factor of $A(0) \cdot \beta$. At the expense of gain, the speed of the system may be boosted to the extent that the closed-loop response strikes the open-loop $-20dB$ gradient, causing both configurations (OL & CL) to have equivalent unity gain frequencies ($w_t$). It should also be noted that so long as open-loop DC voltage gain (A(0)) is large and that $\beta >> 1.0$ then the closed-loop response is desensitised to variations in component tolerances. $\beta$ may be used as a design tool to create low-pass, high-pass or band-pass filters by adding additional poles and zeros to the closed loop response of the circuit [4].

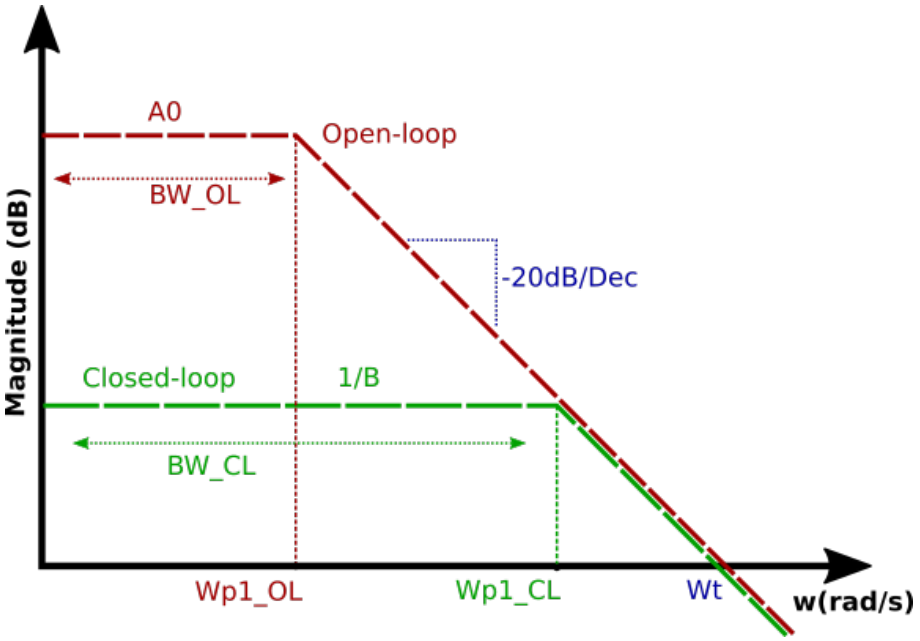


Figure 8: How a negative feedback network impacts the commonly engineered low-pass response of the open-loop transfer function is presented in this figure; the magnitude in $dB$ is on the y-axis plotted against frequency on the x-axis. The red dashed line is the open-loop information, where the corresponding green response if that of the closed-loop. $A0$ (red) is the open-loop DC gain, $\frac{1}{\beta}$ is the closed-loop DC gain, and $W_{p1OL,CL}$ denotes the first pole of both the open-loop and closed-loop responses respectively. $w_t$ places the unity gain frequency, and the gradient of both sloped are $-20dB/Dec$. [4]

### 2.4.2 Summary

Operational amplifiers are extremely useful devices, and are in an ideal sense straightforward to understand. So long as the input impedance's are extremely large ($M\Omega$), the output impedance is small ($\approx 1m\Omega - 10\Omega$), and the internal voltage gain is extremely large ($\approx 10,000$), feedback may be used to create highly accurate circuits that are desensitised to component variation. Assuming that $\beta >> 1.0$ he closed-loop response is dictated by $\frac{1}{\beta}$, with the feedback network allowing designers to control the response of the circuit by externally placing poles and zeros natively in the feedback network. While OPAMPs are great for signal processing, they are usually inadequate for driving loads, leaving the next section open for the discussion of current control devices such as Transistors.

## 2.5 Transistors

Transistors are the most fundamental example of active device, where the input to the device produces a proportional output and therefore delivering a power gain by accessing its available external supply [3]. Transistor devices use a PN-junction to create a proportional output current flow based on either an input voltage or an input current; this is the main differentiation between bias-junction transistors (BJT's), and metal-oxide field-effect transistors are described in the following sections [4].

### 2.5.1 Bias-Junction Transistors

Bias-junction transistors (BJT's) are active current gain devices, and are represented by the two different sysmbols presented in Figure 9. NPN and PNP denote the physical order of doped material, where "N" describes negative doped material composed of electrons, and "P" describes the absence of electrons called holes. The letters "B", "C", and "E" represent base, collector, and emitter respectively. Both device have a diode connection between their base, and their emitter denoted by the small arrow; the base-emitter arrow always points from positive to negative. There also exists another diode between the base and the collector, that must be considered when the device is saturated. The base is commonly used as the control port, leaving the collector and emitter to be connected to a given positive voltage supply, and negative supply in the case of the NPN type, or in the reverse arrangement for the case of the PNP. In summary, NPN BJT's are commonly used as low-side switches that pull current from a node to ground, and PNP BJT's are used as high-side switches that draw current from a voltage supply and then inject it into a circuit node.

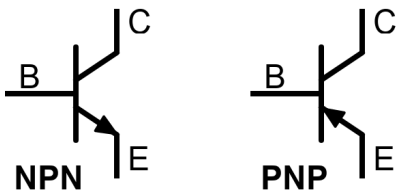


Figure 9: There are two types of BJT transistor devices presented, where one requires a positive base-emitter voltage (NPN), and the other requires one that is negative (PNP). Each type has a base (B), collector (C), and emitter (E).

The benefit of BJT devices utilised as active devices are that they are linear if used correctly; designers commonly use small-signal together with large-signal models to achieve this. The large-signal response of the circuit defines the bias-point of the circuit making use of Equation 8, where $I_C$ is the collector current, $I_B$ is the base current, and $\beta$ is the current gain for the transistor. The large-signal response of the BJT causes the $V_{BE}$ voltage to be that of a forward-biased diode ($\approx 0.7V$) due to it being a pure PN-junction, leaving the current in the base to be ($\frac{V_{IN}-V_{BE}}{R_b} = \frac{V_{IN}-0.7}{R_b}$); $R_b$ is the series resistance in the base. The resulting current in the collector is a function of Equation 8. The BJT input impedance ($r_{pi}$) and the transconductance ($g_m$) are two important AC parameters (discussed later) that are defined using DC analysis. These values are derived at a constant bias, or constant collector current, where Equation 9 defines the transconductance, and Equation 10 defines the input impedance. BJT devices are amplifiers, where it is possible to apply an AC signal on top of the DC bias point requiring a different analysis method; this is called AC analysis, via a small-signal model. This behavior is best described visually with the aid of the hybrid-pi model of a NPN BJT shown in Figure 10, where the three terminals, base (B), collector (C), and emitter (E) are displayed. The input impedance is described by $r_{pi}$ ($\Omega$), the output impedance is described by $r_o$ ($\Omega$), and the voltage gain is displayed by the voltage dependent current source encompassing the gain expression $gm \cdot v_{pi}$ ($\Omega$). This model is linear, and may be used for both NPN and PNP BJT devices where the collector-emitter current course need only be inverted [4] [3].

$$i_c = \beta \cdot i_b \tag{8}$$

$$g_m = \frac{i_c}{v_t} \tag{9}$$

$$r_{pi} = \frac{v_t}{i_c} = \frac{\beta}{g_m} \tag{10}$$

$I_C$ is the collector current, and $A$, $V_T = \frac{k \cdot T}{q}$ is the thermal voltage, where $k$ is Boltzmann constant, $T$ is the temperature in kelvin, and $q$ is the charge of an electron. The input impedance is directly proportional to the thermal voltage, and the collector current, as well as the current gain ($\beta$) and the transconductance. This yields that the current gain ($\beta$) is variable and should be considered in designs; the circuit should be immune to changes in $\beta$. While BJT devices are current gain elements, there exists voltage gain devices, and are discussed in the proceeding section.

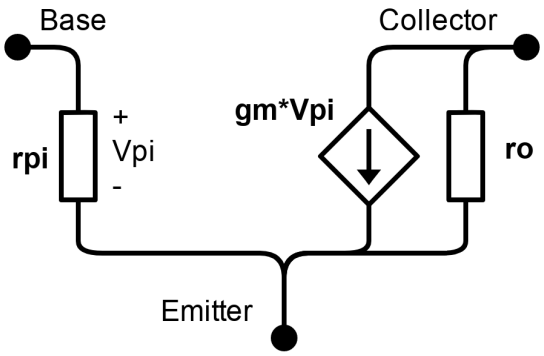


Figure 10: The linear small-signal model of a BJT transistor for both NPN and PNP types is displayed, where $r_{pi}$ is the input impedance, $r_0$ is the output impedance, and $g_m \cdot V_{pi}$ is the gain of the voltage controlled current source sourcing it's output response [4].

The last and final point to be made with BJT devices is the reality of saturating the device. This is when the base of the device is supplied with enough current that causes a non-proportional collector current; the collector current saturates producing a $V_{CE}$ voltage of $\approx 0.3V$. For example, a NPN transistor with a $1.0k\Omega$ series collector resistor, a $5.0V$ supply, and a gain ($\beta$) of 100 cannot have a base current larger than $\frac{5.0}{\beta \cdot 1.0k}$. Saturation causes minority charge carriers to congregate in the base, and collector making the device slower to turn off. Also, the no longer proportional relationship between the input base current and the output collector current, causes a drop in $\beta$. It is therefore ideal to give the device more base current when intending to saturate the BJT to compensate for the drop in current gain [4].

### 2.5.2 Metal-Oxide Field-Affect transistors

Metal-oxide field-effect transistors (MOSFET) active devices, while are similar to BJT transistors, are voltage controlled devices; BJT's are current controlled. They are commonly represented in in schematic designs using the symbols presented in Figure 11, where N-channel types require a positive voltage ($V_{gs}$) applied to its gate to conduct the device, where as P-channel types need a negative voltage ($V_{gs}$). N-channel devices are commonly used as low-side switches, where the gate (G) is used as the control terminal ($V_{gs}$ must be positive), the source (S) is connect to ground, and the drain (D) is connected to a circuit node or supply. In the case of the P-channel device, the source and drain are interchanged, the drain is connected to a circuit node or ground, and the source is connected to a supply voltage; this is a high-side switch configuration. The gate voltage in this case must now be less than the voltage that the source terminal is connected to in order for the device to conduct (($V_{gs}$ is negative). This project uses MOSFET devices to step current from a supply, and into a lower output node. Therefore there is only use for MOSFETS driven in hard saturation, leaving no need for small-signal analysis.

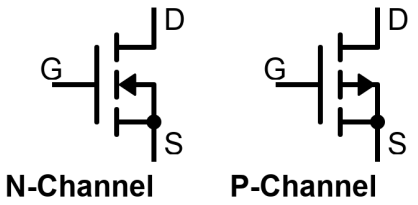


Figure 11: There are two types of MOSFET transistor devices presented, where one requires a positive base-emitter voltage (N-channel), and the other requires one that is negative (P-channel). Each type has a gate (G), drain (D), and source (S).

The large-signal model for MOSFET transistors is presented in Figure 12, where the three terminals of the active device are denoted by gate (G), drain (D), and source (s). MOSFET's are voltage controlled devices and lack an input impedance accordingly; this opening may be considered as a capacitor with gate capacitance $C_{gs}$, and is a design consideration when one is intending to commutate the device as a switch. The output current source ($I_D$) is proportional to the input voltage according to the relation of Equation 11, where this is known as the square-law current-voltage relationship. $\mu \cdot C_{ox}(\frac{A}{V^2})$ is commonly known as KP, and is the charge mobility and oxide capacitance respectively. W and L are the width and length of the channel, $V_{GS}$ is the gate-source voltage, and $V_{tn}$ is the threshold voltage.

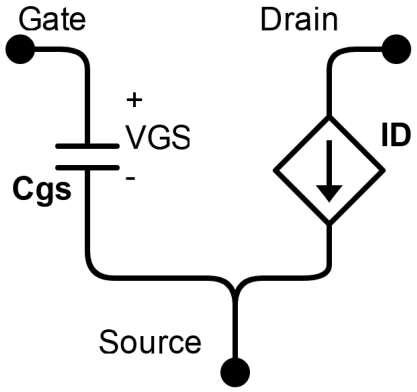


Figure 12: The linear large-signal model of a MOSFET transistor for both N-channel and P-channel types are displayed, where $V_{GS}$ is the input gate-source voltage, and $I_D$ is the collector current of the voltage controlled current source. Note that a P-channel model has its drain current arrow inverted [4].

The main point of using MOSFET's as switches is to drive them into hard saturation at which point their conduction resistance ($R_{ds}$) is minimal. This has two main advantages, where there is little loss ($P_{loss} = I_D^2 \cdot R_{ds}$), and therefore less thermal load reducing the chance of thermal run-away. While this is accomplished by simply by applying adequate voltage to the gate it does, however, become an increasing problem with increased switching frequency; even more so to do it efficiently. The main limiting factor, regarding the switching frequency, is the gate capacitance ($C_{gs}$), that requires that the gate be driven hard by injecting, and removing charge extremely quickly; the current must increase for an increasing conduction frequency. Once enough charge is injected to exceed the threshold voltage ($V_{tn}$) then the drain current relates to the effective voltage ($V_{GS} - V_{tn}$) in a square manner.

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{2 \cdot L} \cdot (V_{GS} - V_{tn})^2 \tag{11}$$

The lack of a resistor at it's input terminal make MOSFET devices ideal when applied as switches, and are often used in switch-mode regulators; N-channel devices are faster, and have a smaller saturation resistance reducing conduction losses [4].

### 2.5.3 Summary

This section covers the three differing active analogue devices related to this project, where OPAMP's are highly accurate, and allow customized devices that can readily be used to make an amplifier with the help of feedback. BJT's are current controlled devices that have high current gain making them ideal for responding to current loads, and transporting charge quickly. MOSFET's on the other-hand are voltage controlled devices, and require an input voltage to control its drain-source current, and are ideal for switch-mode regulation. This concludes the analogue theory section, where the report moves onto digital theory hereafter.

## 2.6 Digital Signals

While being fixed with two different states, opposed to analogue that advertises two, digital control does offer some benefits to analogue circuits. Some of these include noise resilience, and faster hardware design due to active devices railing at their respective supplies. The following sections discuss the basic digital concepts related to this report [3].

### 2.6.1 NOT Gates

The digital block that performs the task of inverting the state of a given logical signal is defined as an inverting gate or a NOT gate; this symbol may be seen in Figure 13. It should be noted that the triangle itself denotes the gate, while the circle at the output denotes the logic inversion.

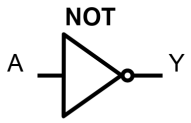


Figure 13: The inverted logic symbol, or a "NOT" gate, is presented in this figure [3].

The input and output relationship for this logic is provided visually through the use of a truth table presented in Table 3 where the input to the gate is "A", while its output is "B". NOT gates in reality, like all other things, are not ideal and entertain a time delay between the input, and its responding output; this is called the propagation delay ($t_p$), and is typically in nanoseconds [3].

Table 3: Digital NOT gate truth table [3].

| Input (A) | Output (Y) |
|---|---|
| 0 | 1 |
| 1 | 0 |

### 2.6.2 NOR Gates

The next gate of interest is the inverted OR gate. The inversion is achieved in the same manner as the previous section, whereas the OR block is described by the possibility of one of two inputs being either logic high, or both hence the gate name OR; together they create the NOR logic gate. Figure 14 shows the symbol associated with NOR gates, where the 90 deg tilted cup-like block represents the OR gate and the circle again represents the inverted logic [5].

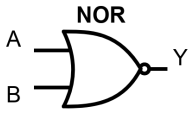


Figure 14: The inverted "OR" logic symbol, or a NOR gate, is presented in this figure [3].

The input and output behaviour of the NOR gate is presented using a truth table found in Table 4, where the two inputs are denoted with "A" and "B", that in-turn produce the output of the block denoted by "Y". As was the case for the NOT gate, NOR gates also suffer from the reality of time, and posses a propagation delay ($t_p$). With NOR gates defined, the digital section of this project is concluded leaving a brief summary before moving to the next topic [5].

Table 4: Digital NOR gate truth table [3].

| Input01 (A) | Input10 (B) | Output (Y) |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

### 2.6.3 Summary

In this digital section, the varying logic operations are discussed, and described through the means of visual representation and functionality. These simple, yet powerful, building blocks serve as a means of reflection for the design discussion that follows after a swift introduction to the simulation platform that is used in this investigation.

## 2.7 Spice Simulator

Ngspice is an open source software platform, made from Spice3f5 (the last release from Berkeley's Spice3 simulator project), that can simulate both linear and non-linear circuits. It can handle all passive devices, lossey and loss-less transmission lines, dependent and independent sources, the five most common active devices (diodes, BJTs, JFETs, MESFETs, and MOSFETs), and switches. Via a terminal prompt in Ubuntu (Linux), a net-list made using KiCad, is compiled. The resulting signal vectors may then be manipulated locally in the terminal prompt, and thereafter exported. External model vectors such as Pspice, Hspice models may be imported into the net-list and then run by Ngspice. It is an extremely powerful tool, that is easy to use, versatile, and does not require a licence to use. While this project is associated with RF design, the envelope tracking system proposed in this project need only operate in the sub $GHz$ frequency range making a spice simulator sufficient. The proceeding section diverges from theoretical description and into design analysis, where the first tracker version is introduced [6].

# 3 Design

## 3.1 Tracker Architecture One

This report is a continuation of an earlier Masters Project [1], that describes a combined linear, and switch-mode regulator verified using a spice simulator (LTspice); this is a simulation under ideal conditions, and using component models that do not reflect real world realities. This project explores the feasibility of using a hybrid linear tracker, and concludes a hypothetical tracker architecture that is implemented as a verification step for this thesis; hereafter this initial simulation derived tracker architecture is referred to as $Tracker_{011}$. Prior to the summary of this section there is a heading describing the simulation of $Tracker_{011}$'s architecture using component models that reflect their real world operation; this new system is referred to as $Tracker_{012}$. A summary of the tracker revisions is found in Table 5, where "Tracker" describes the project, the first two digits describe the architecture revision, and the last digit describes the simulation revision for a given architecture.

Table 5: Envelope tracker architecture revision summary

| | | |
|---|---|---|
| $Tracker_{011}$ | Architecture One, Simulation One | Master Project |
| $Tracker_{012}$ | Architecture One, Simulation Two | Master Thesis |
| $Tracker_{021}$ | Architecture Two, Simulation One | Master Thesis |

This project is of relevance as it is used to develop the initial prototype serving as a proof of concept. Before describing the prototype derived from the masters project, the technical details related to the operation of this design are reiterated. The schematic is presented in Figure 15 with the system specification displayed in Table 6. The tracker is a hybrid combination between linear regulation described in subsubsection 2.2.1, and switch-mode regulation described in subsubsection 2.2.2; linear regulation, is less efficient than that of a switch-mode regulator. This is due to the inherent need of the active device to deplete its supply voltage internally for a given output. While it may be obvious to develop a switch-mode tracking system, since switch-mode regulators are more efficient, losses begin to compound with high frequency switching; see the referenced sections for a more in depth breakdown of linear and switch-mode regulation. While switch-mode regulators are more efficient, they do perform in a less linear fashion compared to linear regulation. The combined hybrid envelope tracker endeavour's to explore the potential benefits of the two systems by creating a linear output reference that the switch-mode regulator uses to switch current into the output node when needed [1]. The next sections cover the engineering of prototype $Tracker_{011}$, followed by the simulation of $Tracker_{012}$ using accurate component models before finishing with a summary concluding the investigation of the $Tracker_{01X}$ architecture.

Table 6: $Tracker_{011}$ system specification

| Parameter | Value | Unit |
|---|---|---|
| Supply Voltage ($V_{CC}$) | 34.0 | Volts (V) |
| Input DC Shift ($V_{DC}$) | 6.2 | Volts (V) |
| Input Voltage ($V_{in}$) | 0.1-4.0 | Volts (V) |
| Output Voltage ($V_{out}^{pp}$) | 6-28 | Volts (V) |
| Gain $G$ | 2.7 | no units $\frac{V}{V}$ |
| Switch-Mode Bandwidth $BW$ | 1.0M | Hertz (Hz) |
| Linear-Mode Bandwidth $BW$ | 80.0M | Hertz (Hz) |
| Load ($R_{load}$) | 50-100 | Ohms ($\Omega$) |

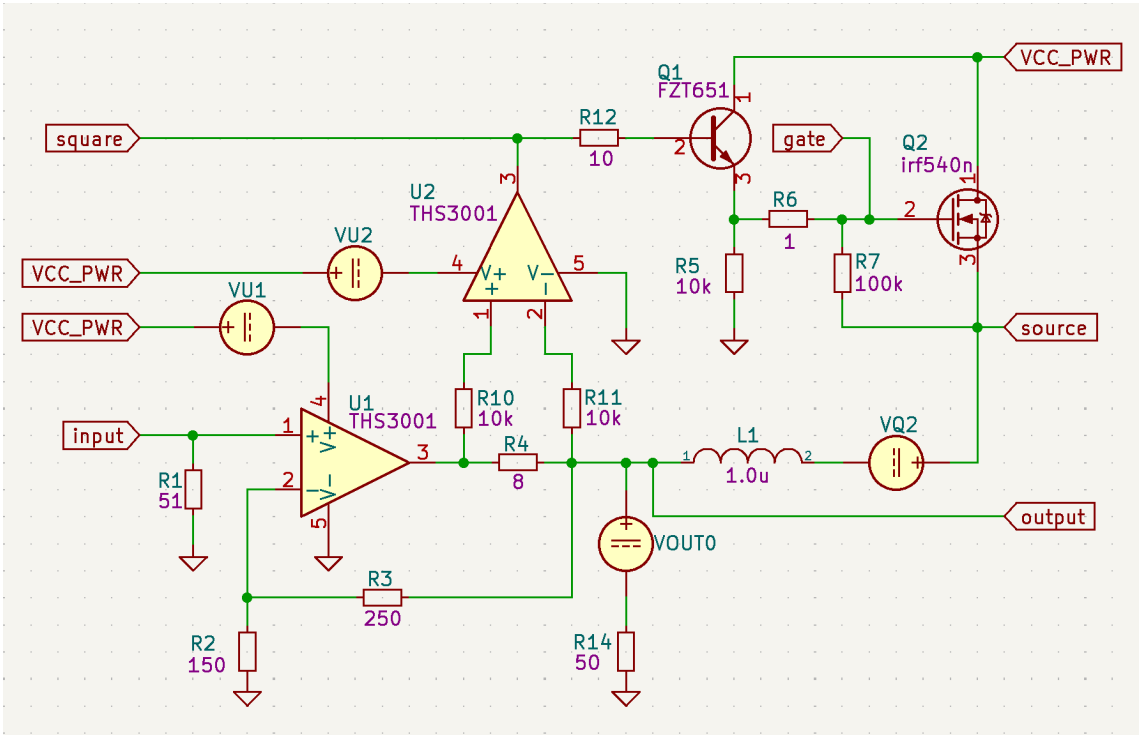


Figure 15: The tracker circuit in its entirety, is shown above with the non-inverting amplifier $U1$, open-loop current control signal $U2$, driver $Q2$, and the current switch $Q1$; the tracker output is at node "output", with its corresponding input at "input".

### 3.1.1 Prototype Design

$Tracker_{011}$, taken from [1], serves as the first prototype design for this investigation, where a printed circuit board (PCB) is fabricated, and soldered with purchased components. The natural starting point of this design phase is to decide on the active components of the system; this is namely the non-inverting OPAMP (U1), the open-loop OPMAP (U2), the gate-driver (Q1), and the current-switch (Q2). The active components selected to play the roles of the previously mentioned active devices are displayed in Table 7. Note that the following discussion is made with reference to Table 6 and Figure 15. The two devices of particular interest are U1,2 where there is a strong bandwidth requirement ($80MHz$), and voltage swing ($6V - 28V$). THS3001 is a current feedback amplifier that has a small-signal bandwidth of $420MHz$ for closed-loop unity gain, a supply voltage of $\pm 15V$, and a feedback resistor values of $1.0k\Omega$ making it ideal for the application of U1 in a closed-loop configuration, and for U2 in an open-loop configuration. FZT651 is a NPN BJT transistor that can receive a collector-emitter voltage of $60V$, can operate with $3A$ of continuous collector current, and has current gain of $\approx (80 - 100)\frac{V}{V}$, making it ideal for the emitter-follower configuration of Q1 seen in Figure 15. The final active component choice is the high-side current switch (Q2), where the N-channel MOSFET called STD40NF03LT4 is chosen for the task. This device may handle a drain-source voltage of $30V$, a sustained drain current of $40A$, while it has a low input gate capacitance of $1.4nF$, and a low threshold voltage of $\approx 1V$ making an ideally switch conducting current injection system for the hybrid tracker.

Table 7: $Tracker_{011}$ active component decisions for the first prototype.

| Device | Manufacturer Part Number | Company |
|---|---|---|
| U1 | THS3001 | Texas Instruments |
| U2 | THS3001 | Texas Instruments |
| Q1 | FZT651 | Diodes Incorporated |
| Q2 | STD40NF03LT4 | STMicroelectronics |
| D1 | BYG22D | Vishay Intertechnology |

The finished prototype is visually shown in Figure 16. The two SMA connectors disclose the input and output terminals, and the gold coloured large pads labelled "$GND$" and "$VCC - 34V$" are the ground and supply voltage thermal relief pads. Using Table 7, the location of the four active components are addressed. The blue cylinders are electrolytic capacitor that show the switch mode supply bank; the two-pin header represents the $34V$ supply connection. The following discussion iterates through the decisions made that resulted in this design. The two classes of active devices, OPAMP's and transistors, are discussed with respect to their relevant passive components, in the following two sections beginning with OPAMP's.

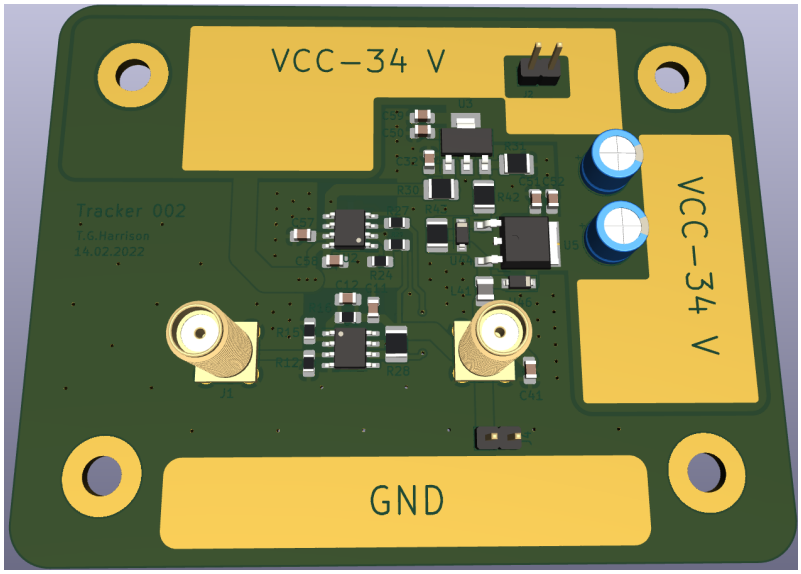


Figure 16: The 3D view of the final $Tracker_{011}$ prototype is presented here, showing the two SMA connectors for the input and output signals, the two OPAMP's, the two transistors, capacitor bank, and thermal pads.

### 3.1.2 Operational Amplifier Design

This section concerns both the sub-system component decisions, and the PCB fabrication design points associated with U1,2 (THS3001); U1 is discussed first followed by U2. According to [2], the bandwidth of the current feedback amplifier THS3001 is directly proportional to the value of its feedback resistor. To produce a gain of $\approx 3$, at a $30V$ supply, a feedback resistor between $560\Omega - 620\Omega$ is ideal; a value of $600\Omega$ is decided. The gain resistor (the feedback resistor to ground) has minimal impact on the circuits stability, and is decided at $350\Omega$ to keep the gain slightly below the specification. While on the topic of components related to the non-inverting amplifier (U1), it should be noted that there is a $50\Omega$ (R12) resistor at the input to the amplifier, and two capacitors (C12 and C11), that are not mounted; they are only needed in the case where the circuit turned out to be unstable. The PCB design of the OPAMPS is seen in Figure 17 where the two OPAMP devices are depicted with U1 and U2 respectively, the ground plane, and the $34V$ supply rails. There is an application note from [2], that emphasize the importance of grounding to allow a low inductive ground path, thermal management, and also the need to remove the placement of grounded copper plane away from the inverting terminal, and output node. The feedback path must also be free of copper; this is all on display in the presented figure. The feedback loop is routed as tightly between the output and the inverting terminal, the grounding plan surrounding the OPAMP's is stitched to the bottom place using vias for good continuity, and the $34V$ supply to the two devices is appropriately wide for $\approx 500mA$. The design decisions associated with the PCB's transistor population are discussed next.

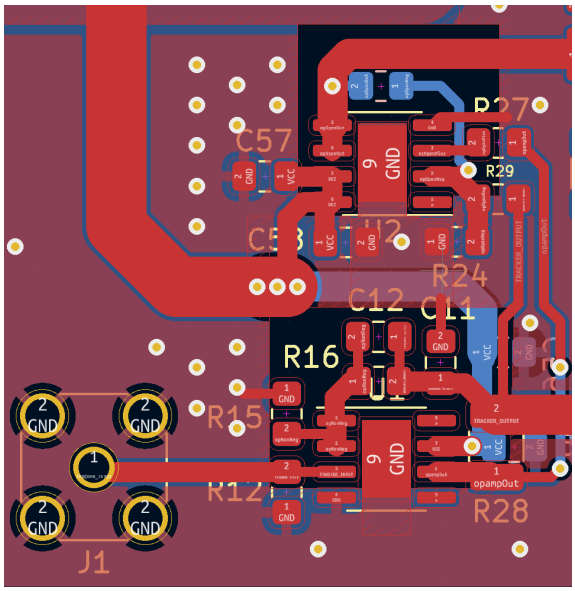


Figure 17: A close-up view of the two OPAMP's, the non-inverting (U1) and open-loop (U2), showing the removal of the ground plane near their node legs.

### 3.1.3 Transistor Design

The transistors populated on the prototype are the main current carrying devices, that introduce two PCB design points of particular concern, being namely impedance and thermal control; these are discussed with respect to Figure 18.

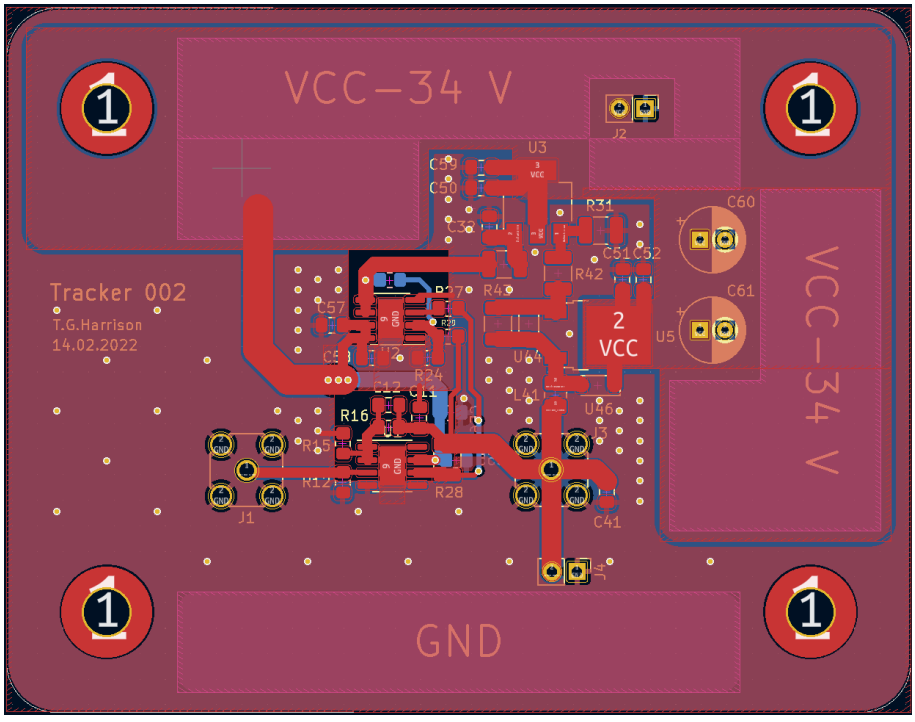


Figure 18: The board layer view of $Tracker_{011}$ is presented showing the relative track widths, grounding vias, and copper fills.

The relative resistivity of a copper track will increase with temperature, and thereby introducing the concept of thermal run-away. According to [7] a track width of $\approx 0.76$ is adequate for a

continuous current of $2.0A$, where the expected current load is not larger than $\approx 1.0A$. With this in consideration, a safe copper width between $1.5mm - 2.0mm$ is concluded. The high-side switch, and driving circuit is expected to draw the majority of the current load according to [1], sprouting cause for concern regarding thermal management. For this reason, the top and bottom ground planes are stitched together for low inductive current paths, and to distribute heat evenly. The supply plane on the other hand is not stitched to ground, however, it is expanded over a large area with exposed copper to encourage thermal expulsion via air-cooling; the top-overlay is removed over certain areas to expose bare copper to aid thermal cooling. It should also be noted that the current loop between the linear regulator's output and the switch-mode regulators output is kept as small as possible to limit propagation delay, and reactive loading [3]. Moving on from PCB development is second simulation involving the accurate component models.

### 3.1.4 Non-ideal Simulation

$Tracker_{011}$ is composed of four different active devices that are replaced by the following Pspice component models to produce $Tracker_{012}$, where the architecture is the same (architecture $01X$), however, there is a discrepancy from the new simulation data than that from the masters project [1] (simulation $XX2$). All of the active devices are readily available from their respective manufactures, however, the chosen N-channel MOSFET's (STD40NF03LT4) Pspice model proves to be inadequate for simulation purposes, and is exchanged for that of IRLML6346TRPBF's. The next hurtle to traverse is the limitations of LTspice that did not support Pspice model files; this gave way to ngspice that supports a greater breadth of component models. Excluding the difference in component models, the architecture of simulation one ($XX1$) and simulation two ($XX2$) are identical. This now concludes the engineering associated with architecture one ($01X$), where a summary proceeds to conclude the design discussion of architecture one.

Table 8: The component models for $Tracker_{012}$; the second simulation of the first tracker architecture.

| Device | Manufacturer Part Number | Company |
|---|---|---|
| Non-inverting OPAMP (U1) | THS3001 | Texas Instruments |
| Inverting OPAMP (U2) | THS3001 | Texas Instruments |
| NPN Transistor (Q1) | FZT651 | Diodes Incorporated |
| N-channel MOSFET (Q2) | IRLML6346TRPBF | Infineon |
| Fly-back Diode (D1) | BYG22D | Vishay Intertechnology |

### 3.1.5 Summary

$Tracker_{01X}$ is a prototype design derived from a previous masters project intended to serve as a path finder for future iterations. It is physically modelled using KiCad to produce a PCB with mounted components chosen to reflect the ideal components used in masters project. Following the physical design is a second simulation of the same tracker architecture that incorporates component models of real-world devices. In summary, $Tracker_{01X}$ is the proof of concept design to kick-start the proceeding innovation section that innovates on its shortcomings.

## 3.2 Tracker Innovation

The following section focuses on the areas of needed improvement with regard to $Tracker_{01X}$. Both the simulation results from [1], and the verification results from $Tracker_{011}$ presented in subsection 4.1. The following subsections cover the development of the current control feed, slew rate reduction via charge cycling, and improved linear current management.

### 3.2.1 Current Control Feedback

The purpose of the current control feedback signal is to allow the tracker to independently serve itself more current when needed, opposed to receiving a fixed frequency signal with fixed losses; the duty cycle will also change accordingly. The main area of focus in this section is to produce a square signal of high quality that travels between $0.0V$ and $5.0V$ in a clean and orderly fashion that does not wash out at high frequency. This is to prevent current commands that do not fully conduct the MOSFET, as this would cause higher losses, heat and potential damage to the device. Table 9 shows the system requirements of the current control signal. A $5V$ logic control voltage is chosen for two reasons. One is due to the slew limiting problems seen in [1], where the system's response is largely restricted to the opamp's slew rate when running in open-loop. With the system then powered with a $30V$ power rail, this causes the current control signal to be less responsive between control high, and control low. By using a $5V$ control signal the transition time between logic high, and logic low will be less; the rate, however, will still be limited to the open-loop opamp's gain bandwidth product. From subsection 2.3, the system is expected to utilise switch-mode regulation up to 1.0MHz, and therefore the bandwidth of the current control signal is placed one decade higher at 1MHz. The signal delay should be minimized as much as possible.

Table 9: Specification for the current control signal

| Parameter | Value | Unit |
|---|---|---|
| Input Voltage ($input$) | 3.3-5 | V |
| Voltage ($vcc_logic$) | 3.3-5 | V |
| Bandwidth ($BW$) | 1.0 | MHz |
| Delay ($T_{delay}$) | 10.0 | ns |

Figure 19 shows a two-phase non-overlapping clock generator that is used to control the logical state of the current control signal employed to drive the current injection switch at the tracker's output. This subsystem is referred to as the current control feedback block hereafter. The following break down of the logic-control block is carried out with reference to Figure 19, and the logic control units described in subsection 2.6. The nets are first described, where $vcc_{logic}$ is the $3.3V - 5V$ power supply to the subsystem, $input$ is the signal input, and $fb1, 2$ are the two feedback signals from the two corresponding outputs $out1, 2$. Note that $fb1, 2$ could be replaced with $out1, 2$, however, there would be less delay between logic events; this is not desirable. The nature of the logic-control block is that it is not possible for the outputs to share the same state; this is indicative of the NOR gate logic unit. The input signal drives in unison with $out2$, with $out1$ being inverted, and if $input$ is assumed to be high (3.3V), then $out1$ is low and $out2$ is high. As $input$ moves to low (0.0V), the NOR gate of $out1$ is set with one low input signal, and awaits the event change of the NOR gate of $out2$ supplied through feedback ($fb2$). $U4, 5, 6, 7$ provide the small delay between the event cycles that ensure the non-overlapping behaviour, and thereby ensuring the signal's integrity. The BJT transistors on the right-hand side of the figure (Q1,2) are the output buffer circuits, discussed in subsubsection 2.5.1, to enable the circuit to drive larger loads [3] [4].

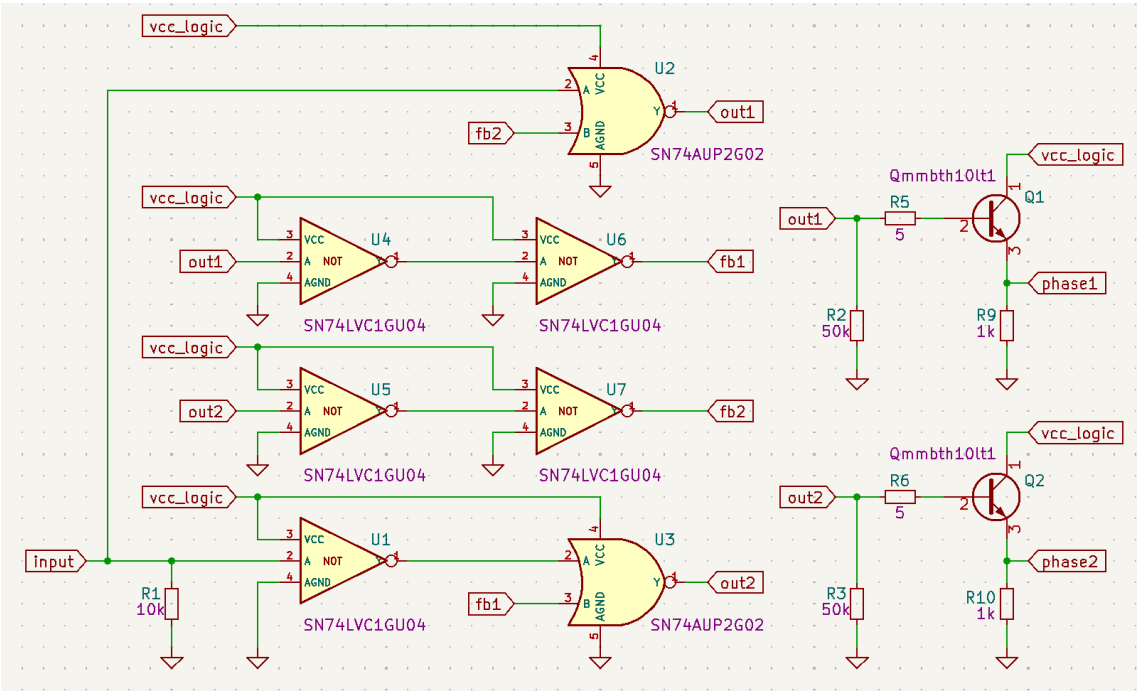


Figure 19: This circuit used logic feedback to produce non-overlapping lock pulses with a small delay between events. This is achieved using two NOR gates with five NOT gate, to create two inverted outputs; the concatenated NOT gates delay the feedback signal. The two BJT devices are buffer circuits.

The logic units, and their corresponding Pspice models, are produced by Texas Instruments, where the NOT gate device is called SN74LVC1GU04, and the NOR gate device is called SN74AUP2G02. The simulation results from this circuit are presented in subsubsection 4.3.1. Following this section is the practical application of the output signal from the above logic-control block to commutate a high-side n-channel switch.

### 3.2.2 Charge Pump

The circuit in Figure 20 is to replace the driver circuit from $Tracker_{010}$'s architecture that shows large efficiency degradation due to the voltage swing between 0.0V and 34.0V. Figure 20 shows the conceptual realisation of a manually driven charge pump that uses a boot-strap capacitor (C1), and a diode (D1), to shift the gate voltage of Q1 with respect to its source voltage ($vsine$). In doing this, the requirement of driving the gate of the high-side switch using an active device is eliminated, and instead the gate-source voltage of Q1 is placed on top of the voltage present on its source using the capacitor; this is described as a charge pump. Table 10 summarises the specification of the charge pump with respect to the tracker architecture requirements (subsection 2.3). The input control signal has a voltage range equal to that provided by the logic-control block, the driver supply voltage is 15.0V to account for high-speed operation, and the high-side switch (Q1) is powered by 30V.

Table 10: Specification for the tracker's charge pump

| Parameter | Value | Unit |
|---|---|---|
| Input Voltage ($input$) | 0.0-3.3 | V |
| Driver Voltage ($vcc_gate$) | 15.0 | V |
| Output Voltage ($vcc_power$) | 34.0 | V |
| Bandwidth ($BW$) | 10.0 | MHz |
| Delay ($T_{delay}$) | 10.0 | ns |
| Duty Cycle ($D$) | 100 | % |

Figure 20 is composed of three main units, the charge-pump circuit (D1 and C1), the push-pull amplifier (Q2, Q3, Q4, R7, R8), and the high-side switch (Q1, R1, R2, and R3); V2 is in practice an arbitrary voltage present at the source of Q1, and is here modelled as a sinusoidal voltage. Not that the placement of the load resistor on the drain of Q1, combined with the sinuous applied to Q1's source, is not representative of the tracker architecture and is purely used in this test bench as a proof of concept for the charge pump. With reference to Table 10 the three units are discussed in detail. As previously mentioned, the purpose of the circuit is to shift the gate voltage of Q1 by only what is necessary in order to fully conduct Q1. To achieve this in an effective manner, a capacitor (C1) is employed to sample the voltage present at the source of Q1, and then places the driver voltage on the left-hand side using the diode (D1). The second unit is the push-pull amplifier that is responsible for applying the shifted voltage reference to the gate of the high-side switch. Q4 operates as an inverted active device that drives the base of Q2 and Q3 with the shifted reference. When the input is low, Q2 (NPN) conducts and Q3 (PNP) is off since the shared gate net of Q2 and Q3 is pulled to "vcap". Q2 will initially push charge into the gate of Q1 since its gate voltage is at "vcap". Q2 will, however, turn itself of as the gate rises towards "vcap"; Q3 is off during this interval. When the input goes high, the common base of Q2 and Q3 is pulled to ground (0.0V), therefore forcing Q2 to remain in its current off-state, allowing Q3 to conduct, and pull the charge back out of Q1. The remaining unit is the high-side switch that merrily employs the driven voltage from the push-pull amplifier to draw current through the mock 500Ω load. R1 controls the charging time constant (RC) of the gate capacitance of Q1, and R2 regulates the relaxed (non-driven) state of Q1 where the its gate voltage will converge towards its emitter voltage ($vsine$) [3][4].

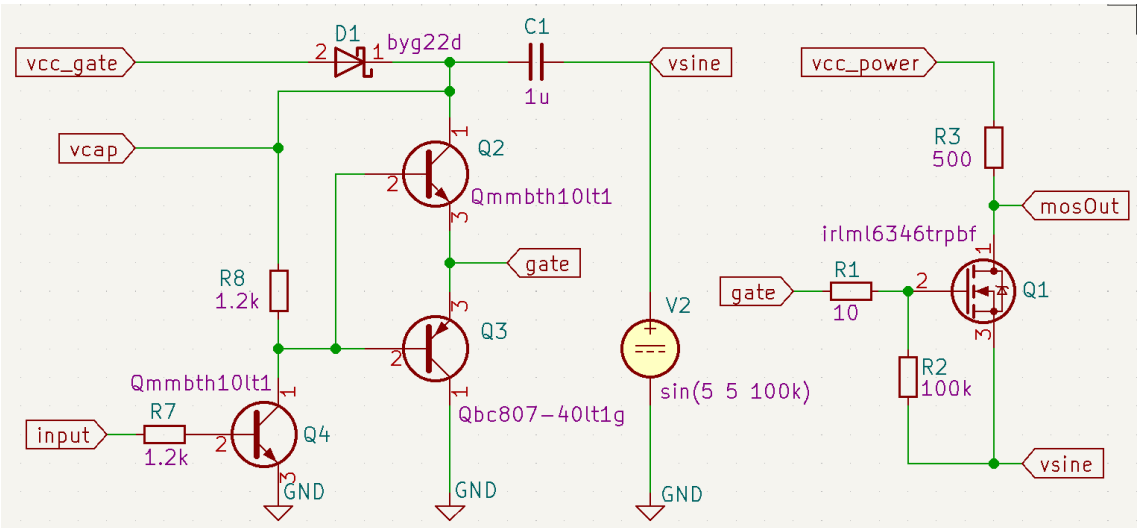


Figure 20: A manually commutated charge pump architecture is employed using one inverting transistor, a push-pull amplifier, a diode, and a capacitor. The capacitor is used to shift the gate voltage of Q1 above the voltage present at its source.

The NPN, and PNP BJT transistors (Q2,3,4) used in this design are produced from Onsemi along with their Pspice models. Care is taken to ensure that the current gain of the two transistors are similar so that shoot through is avoided. The N-channel MOSFET (Q1) is produced by Infineon as is its Pspice model; it has an adequate conduction resistance of $63m\Omega$, and an ideally low gate-source capacitance of $0.13nC$. The diode (D1) component choice is of importance due to speed requirements, and is produced by Vishay; the diode's Pspice model is sourced via their website. The diode is an ultra-fast avalanche diode for high-speed applications. Proceeding this section is the investigation of a ready-made IC high-side driver implementation.

### 3.2.3 High-side Driver & Charge Pump

The circuit presented in Figure 21, serves a similar purpose as of the manually commutated charge pump from subsubsection 3.2.2 with the added luxury of having the circuit architecture readily available as an integrated circuit (IC) package. While there is the benefit of having a working high-side driver within a short time-frame, there are potential problems with with regard to the application of a ready-made IC driver for the proposed tracking system. This is namely related to having a non-constant input control signal with regard to frequency and pulse width; and is the reasoning behind developing the two driver solutions in parallel with each other. The specification of for this IC is the same as for the manual charge pump, and is presented in Table 10. The high-side driver uses the same principles as subsubsection 3.2.2, where the IC has an internal charging diode, that deposits the driver's supply onto the capacitor that is referenced to the floating source of Q1.

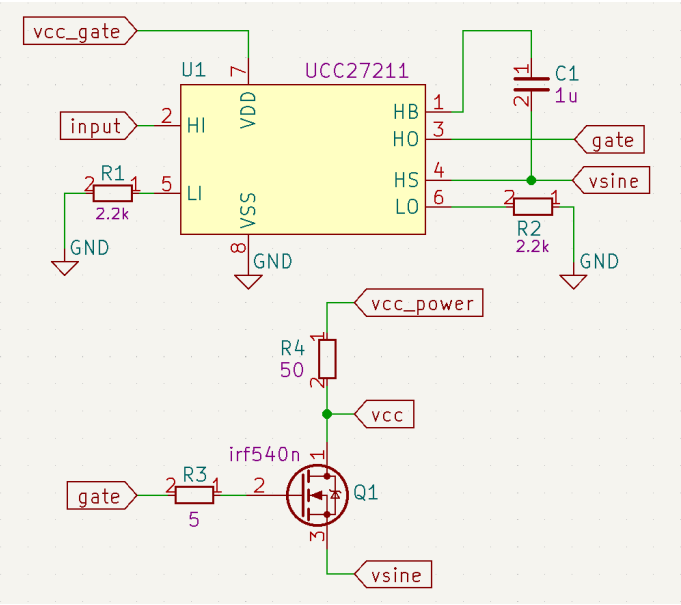


Figure 21: U1 is the high-side driver IC, where the high-side control input is connected to "input", powered by the gate supply, the high-side switch's floating source voltage ("vsine"), and the shifted high-side gate control signal that feeds the gate of Q1 ("gate").

The IC device used in this simulation (UCC27211) is from Texas Instruments; the Pspice model for this unit is sourced via their website. It is chosen as it is has very small propagation delay (typically 18ns), and is designed for both half-bridge and full-bridge converters. The following sections discusses the solution for linear current management to avoid pulling large loads through the non-inverting opamp that both sets the linear output reference, and actively filters the output node.

### 3.2.4 Linear Current Reference

One of the main problems of $Tracker_{010}$ is that the non-inverting OPAMP cannot drive the 50Ω load without the switch-mode regulator; this is dicussed in more detail in subsubsection 5.1.1. This is not ideal in the case where the switch-mode supply fails. The circuit shown in Figure 22 shows one method of decoupling the current load from the non-inverting opamp (U1 in Figure 15), and instead off-load it to a transistor (Q1). The information presented in Table 11 specifies the requirements of the linear regulator. The linear regulator is the starting point of the hybrid tracking system, and sets the reference signal for the switch-mode regulator to operate around. This circuit receives an input signal between 0.0V and 4.0V, the closed-loop gain is equal to $3.0\frac{V}{V}$ that when provided with a DC off-set of 6.0V, will output a sinusoidal waveform between 6.0V and 28.0V

centered about 18.0V. The non-inverting amplifier (U1) receives a 30.0V supply such that it can effectively drive the gate of the BJT (Q1). The phase margin and gain margin of 45.0° and 15.0dB are chosen to ensure stability over the 80.0MHz bandwidth [4].

Table 11: Specification for the linear regulator

| Parameter | Abbreviation | Value | Unit |
|---|---|---|---|
| Input Voltage | $input$ | 2-10 | V |
| DC Off-set | $(V_{DC})$ | 6.0 | V |
| Linear Regulator Supply | $(vcc_{power})$ | 30.0 | V |
| Closed-loop Gain | $A_V^{CL}$ | 3.0 | NA |
| Bandwidth | $BW$ | 80.0 | MHz |
| Loop-Gain Phase Margin | $(PM_{LG})$ | 45.0 | ° |
| Loop-Gain Gain Margin | $(GM_{LG})$ | 15.0 | dB |

The circuit is composed of three main units; the non-inverting amplifier (U1, R1,2 and C1), the emitter-follower NPN BJT (Q1), and the load (R4). It is worth noting the chosen active devices used prior to the break-down of the circuit to aid the rationality of the design decisions. The OPAMP (U1) is from Texas Instruments, it is a current feedback amplifier, and is called THS3001. The transistor (Q1) is an NPN BJT from DIODES Incorporated, and is called FZT651. The grounding principles of operation are relatable to the basic behaviour of the two standard circuit configurations, and are analysed accordingly for simplicity; the non-inverting amplifier is broken down first.

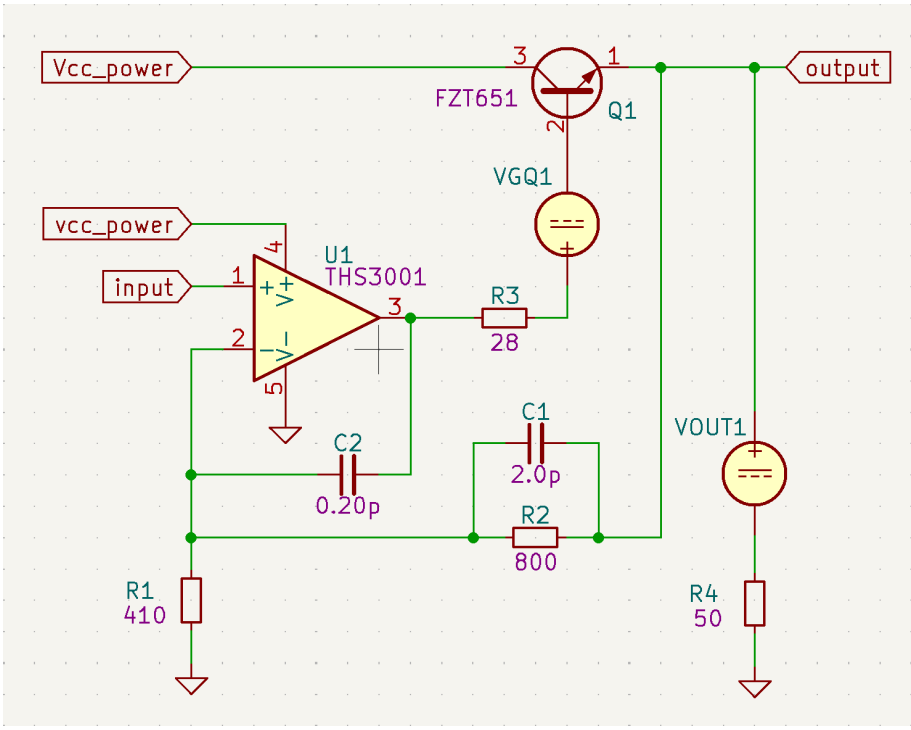


Figure 22: The circuit provides a linear reference proportional to the gain of the input signal via the feedback, where the BJT (Q1) is used to source the current for the output node leaving U1 unloaded.

The two feedback resistor (R1,2) set the closed loop DC voltage gain of the circuit as seen in Equation 12 where the BJT does not affect the circuit, and does not influence the gain equation since Q1 is incorporated into the feedback network.

$$A_V^{DC} = 1 + \frac{R2}{R1} \tag{12}$$

The capacitor (C1) is used in the AC voltage response to deplete the gain of the system at high frequencies, as seen in the closed loop AC voltage gain of Equation 19, where the feedback resistor R2 is short circuited as the frequency approaches infinity; this causes the gain to drop according to Equation 13. C1 produces one pole and one zero as seen in the transfer function.

$$A_V^{AC} = \frac{R1 + R2}{R1} \cdot \frac{1 + \frac{s}{(R1+R2)\cdot(R1\cdot R2\cdot C2)}}{1 + \frac{s}{R2\cdot C2}} \tag{13}$$

The next circuit is the emitter-follower, that is inherently known as a buffer circuit, and serves the purpose of decoupling the current requirements from the non-inverting amplifier. The following content relies highly on concepts presented in subsubsection 2.5.1. The DC voltage gain of the circuit is described in Equation 14, where gm is the transconductance of Q1, Ze is the impedance of the emitter node of Q1 with respect to ground, and $\beta$ is the current gain of Q1.

$$A_V^{DC} = \frac{Ze}{\frac{1}{gm} + Ze + \frac{R3}{\beta+1}} \tag{14}$$

The $\frac{R3}{\beta+1}$ term is very small, and is excluded from the analysis leaving $A_V^{DC} = \frac{Ze}{\frac{1}{gm}+Ze}$. The transconductance (gm) of the circuit is proportional to the collector current (ic), and the thermal voltage ($V_T$). Through the use of DC analysis, the values from the hybrid pi model described in subsubsection 2.5.1 can be defined. The output DC bias point is positioned at 18.0V with an output load of $\approx 50\Omega$ producing a collector current of $ic = \frac{18.0V}{50\Omega} = 280mA$. The inverse of the transconductance ($\frac{1}{gm}$) is therefore equal to $\frac{1}{gm} = \frac{V_T}{ic} = \frac{25mV}{280mA} \approx 90m\Omega$. This may be considered as being insignificant leaving the simplified voltage gain relation of $A_V^{DC} \approx \frac{Ze}{Ze} \approx 1$ or unity. Note that in reality the voltage gain will always be slightly less than unity, as it is impossible to produce a steady-state voltage at the emitter that is larger than the base voltage in this specific emitter-follower circuit configuration. The next phase of the analysis is to combine the the voltage gain equations to find the overall system response. The first stage of this process is to define the loop gain, that will also be used to check for stability. This is achieved by breaking the feedback connection to the inverting terminal of the opamp U1, grounding the input, applying a test signal (Vt) to the inverting signal of U1, and then observing the resulting divided voltage on the high-side of R1 where the feed-back node would normally be connected to the inverting terminal. The analysis of this process yields the loop gain of the circuit, and is presented in Equation 15 in its generic form with the more verbose version given in Equation 16.

$$LG_V^{AC} = A(s) \cdot \frac{R1}{R1 + R2||C1} \cdot \frac{Ze}{\frac{1}{gm} + Ze + \frac{R3}{\beta+1}} \tag{15}$$

$$LG_V^{AC} = A(s) \cdot \frac{R1}{R1 + R2} \cdot \frac{1 + s \cdot R2 \cdot C1}{1 + \frac{s\cdot R1\cdot R2\cdot C1}{R1+R2}} \cdot \frac{Ze}{\frac{1}{gm} + Ze + \frac{R3}{\beta+1}} \tag{16}$$

Inspecting Equation 16, yields one pole, and one zero shown by Equation 17, and Equation 18 respectively. These equations are used as tools to achieve the correct circuit performance.

$$w_{p1}^{LG} = \frac{R1 + R2}{R1 \cdot R2 \cdot C1} \rightarrow f_{p1} = \frac{R1 + R2}{2\pi \cdot R1 \cdot R2 \cdot C1} \tag{17}$$

$$w_{z1}^{LG} = \frac{1}{R2 \cdot C1} \rightarrow f_{z1} = \frac{1}{2\pi \cdot R2 \cdot C1} \tag{18}$$

The following design decisions are made with respect to Table 11, and the two data sheets of U1, and Q1. The feedback resistor values (R1,2) are set based on the desired closed-loop voltage gain ($3.0\frac{v}{v}$), and the characteristic response desired by the current feedback OPAMP. Since U1 is a current feedback OPAMP, feedback reistors (R2) at $1.0k\Omega$ produce a flattened response, where $400\Omega$ resistors over-shoot. Via simulation, a feedback resistor value of $800\Omega$ produces an adequate response. Using these values the capacitor value C1 is then solved for by setting the required pole 3dB corner frequency of 80MHz; the zero frequency is more of a byproduct rather than a design decision assuming the circuit is stable. Once the circuit is deemed stable by loop-gain analysis, it is then used to describe the closed loop response based off Equation 6 that suggest the closed-loop response is $\approx \frac{1}{\beta}$ assuming that $\beta >> 1.0$. The value of $\beta$ is in essence a voltage divider from the output of the circuit to the location of the feedback node; the closed-loop transfer function is presented in Equation 19.

$$A_V^{CL} = \frac{R1 + R2}{R1} \cdot \frac{1 + \frac{s \cdot R1 \cdot R2 \cdot C1}{R1 + R2}}{1 + s \cdot R2 \cdot C1} \cdot \frac{\frac{1}{gm} + Ze + \frac{R3}{\beta + 1}}{Ze} \tag{19}$$

By using the simplification of $\beta >> 1.0$ the closed-loop response becomes the inverse of the loop gain causing the loop's poles and zeros to switch to zeros and poles respectively. The closed-loop's poles and zeros are defined in Equation 20, and Equation 21 respectively. These two equations are used in subsubsection 5.2.1 to analyse the closed loop response of the system, which is in reality the response of the system in its functionally complete form [4].

$$w_{p1}^{CL} = \frac{1}{R2 \cdot C1} \rightarrow f_{z1} = \frac{1}{2\pi \cdot R2 \cdot C1} \tag{20}$$

$$w_{z1}^{CL} = \frac{R1 + R2}{R1 \cdot R2 \cdot C1} \rightarrow f_{p1} = \frac{R1 + R2}{2\pi \cdot R1 \cdot R2 \cdot C1} \tag{21}$$

### 3.2.5 Summary

This section begins with the introduction of a problem, that is to create a swift linear amplifier (BW $\approx 80MHz$) with the ability to drive a $50\Omega$ load; it must be be able to drive $\approx 1.5$A of continuous current (margin is accounted for). The proposed solution to this problem is to use an emitter follower in conjunction with the existing non-inverting amplifier. The design uses one NPN BJT (FZT651), and one current feedback OPAMP (THS3001). The loop gain is used to characterise the stability of the circuit, while the feedback resistor (R1,2) are selected based on the desired voltage gain, and the specific response of the OPAMP. By using the available information from the BJT's data sheet, the voltage gain of the emitter follower circuit along with the non-inverting amplifier's voltage gain equation, the loop-gain is defined. Analysis of this relation yields the systems stability, and by applying the loop-gain equation to Equation 6 results in the closed-loop response (assuming $\beta >> 1.0$). With the linear regulator now defined, the innovation design section is therefore concluded, and the report now move onto the next tracker architecture ($Tracker_{021}$).

## 3.3 Tracker Architecture Version Two

This chapter describes the second, and final RF envelope tracking architecture for this investigation ($Tracker_{021}$). This architecture combines the knowledge gained throughout the narrative of the project to produce the circuit shown in Figure 23. The only functional block that has not been covered is the differential comparator (U2) produced by STMicroelectronics (TS3011). The role of this unit is to amplify the small forward voltage drop across the shunt resistor (R5), which is the same concept from subsection 3.1, that is then pipped into the current control feedback circuit before the charge pump uses it to drive the high-side switch (Q5). The commutation of Q5 injects current into the output node via the inductor (L1) that helps to suppress the current ripple at the output. The shunt resistor (R5) then experiences a reverse in current direction (forward-bias to reverse-bias) thus forcing the comparator output (duty) to $\approx 0V$; this then prompts the charge

pump to discharge the gate of Q5 stopping the current flow to the output node. The two line resistors (R17,18) at the non-inverting/inverting terminal of U2 are arbitrary values posing little design significance, while the $100k\Omega$ resistor (R6) is used to pull the logic circuit low upon start up. The text now moves onto the specification of this new architecture presented in Table 12.

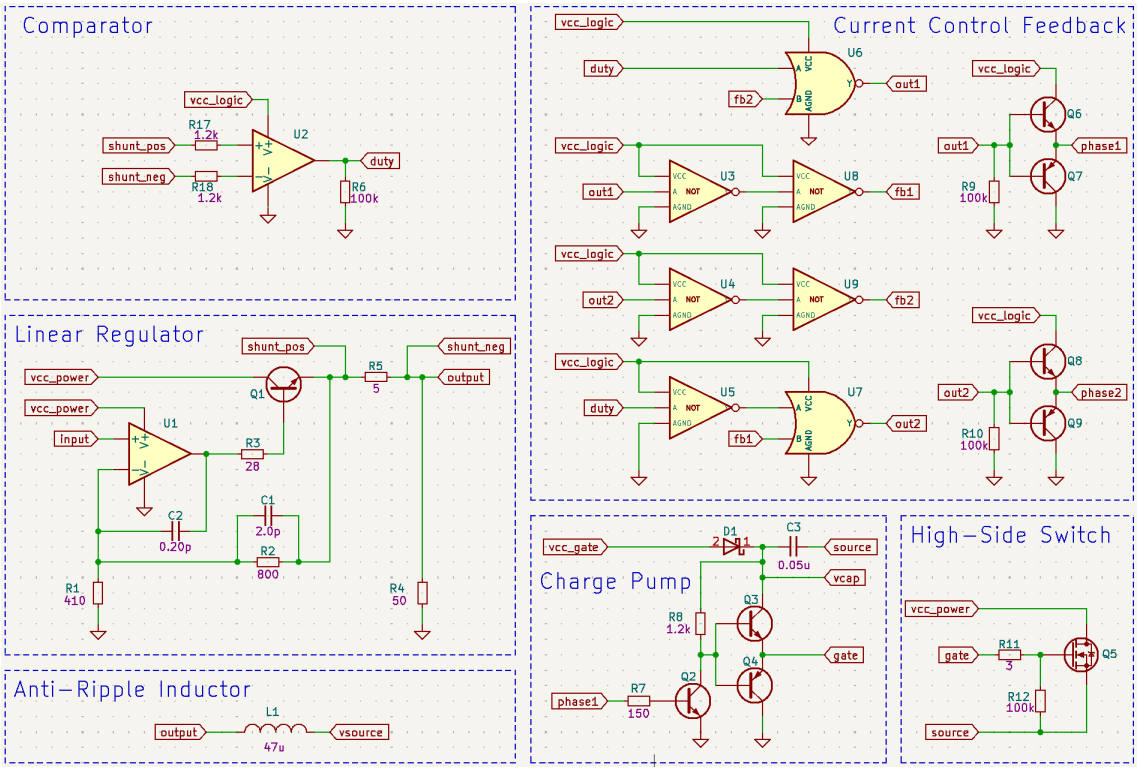


Figure 23: The second revision of the tracker architecture ($Tracker_{021}$) is shown in its entirety. The blue headings, together with the dashed-blue rectangles, specify the various sub-systems within the circuit.

Table 12 is constructed based on the theory from RF PA devices (subsection 2.1), and from the characteristics of mixed-signal modulation schemes (amplitude and frequency). The voltage is chosen accordingly due to a PA (transistor's) basic requirement of $\approx +6V$ at its drain to ensure that it does not go into cut off [8]. The $28V$ limit is an arbitrary output voltage common to low-voltage RF PA devices. The supply to the logic devices is intentionally kept as low as possible, as is for the gate voltage. The power supply is chosen to allow a $\approx 6V$ margin, the bandwidth requirements are as per subsection 2.2, and the efficiency must be as high as possible. The end of this passage marks the end of the design chapter, where the results take center stage from here onwards.

Table 12: Specification for $Tracker_{021}$

| Parameter | Abbreviation | Value | Unit |
|---|---|---|---|
| Input Voltage | $input$ | 2.0-10.0 | V |
| Output Voltage | $output$ | 0.6-28 | V |
| Logic Supply | $vcc_{logic}$ | 3.3.0-5.0 | V |
| Driver Supply | $vcc_{gate}$ | 12.0-15.0 | V |
| Power Supply | $vcc_{power}$ | 34 | V |
| Switching Bandwidth | $BW_{SWTCH}$ | 1.0 | MHz |
| Linear Bandwidth | $BW_{LINEAR}$ | 80.0 | MHz |
| Efficiency | $\mu$ | 70-100 | % |

# 4 Results

The results follow the narrative of the project where the results stemming from the proof-of-concept prototype ($Tracker_{011}$) are initially described followed by the second simulation of the same architecture using accurate component models ($Tracker_{012}$). The innovation section is hereafter presented showing the improved hardware performance driven by the preceding results. Finally, the second tracker architecture ($Tracker_{021}$) is derived based from the natural narrative of the project investigation. Data in this section may be from both lab verification using instruments, and simulation data from ngspice (subsection 2.7).

## 4.1 Tracker(011) Verification

This section covers the findings from the initial prototype $Tracker_{011}$ described in subsection 3.1 where the physical prototype is verified in a laboratory. Wile the prototype is designed to operate up to $34V$, the supply voltage is reduced to limit the expectations of the system and is instead increased over time. Table 13 shows the operating conditions for the laboratory work. There are two findings of significance that influence the future development of $Tracker_{021}$ through the innovation section in subsection 3.2; this is namely the current loading of U1 and the gate voltage of the high-side switch (Q2). The prototype PCB of $Tracker_{011}$ shown in Figure 16 is connected to $vcc_{power}$, the input signal generator ($input$), the output is connected with a 200Ω load ($R_{load}$), and the $output$ is measured using a vector-network analyser. While the prototype produced the correct gain for the larger load, problems arise when $R_{load}$ is reduced. U1 can not drive a 50Ω load resulting in the component failing; it is diagnosed through temperature (it became too hot to touch), visual inspection (smoke rose from the device), and an oscilloscope (there is no longer any gain). $R_{load}$ is reduced to 50Ω to test the switch-mode supply, as this causes a larger voltage drop across the shunt resistor (R4 in Figure 15). The high-side switch, including the gate driver, increases significantly in temperature over the duration of this process, and is ultimately terminated by the failure of U1 that cannot drive the smaller load.

Table 13: Laboratory test conditions for $Tracker_{011}$

| Parameter | Abbreviation | Value | Unit |
|---|---|---|---|
| Input Voltage DC | $input$ | 2.3-4.0 | V |
| Output Voltage DC | $output$ | 6.0-12.0 | V |
| Power Supply | $vcc_{power}$ | 15.0-20.0 | V |
| Load | $R_{load}$ | 50-200 | Ω |

## 4.2 Tracker(012) Simulation

The following section covers the second simulation of the first architecture ($Tracker_{012}$) using accurate component models in ngspice (subsection 2.7). The first subsection covers the DC current and power loading of the two OPAMP's (U1,2). Following is an investigation of the gate voltage driving the high-side switch (Q2). The next proceeding topic covers the data from the innovation section (subsection 3.2).

### 4.2.1 Operational Amplifiers

The following data presented in Figure 24 is sampled from the circuit in Figure 15 located in subsection 3.1. The graph is composed of time-domain data that describes both current, power and efficiency for the two OPAMP IC devices; the current (A) is on the y-axis, and the time (s) is on the x-axis. Both figures market "Instantaneous" current in green, "Average" current in purple, and "Maximum" current in red. The average, and maximum power corresponding to each current waveform from U1,2 respectively is provided for each sub-figure; the overall $Tracker_{012}$ DC efficiency (average and maximum) is given in the top sub-figure.

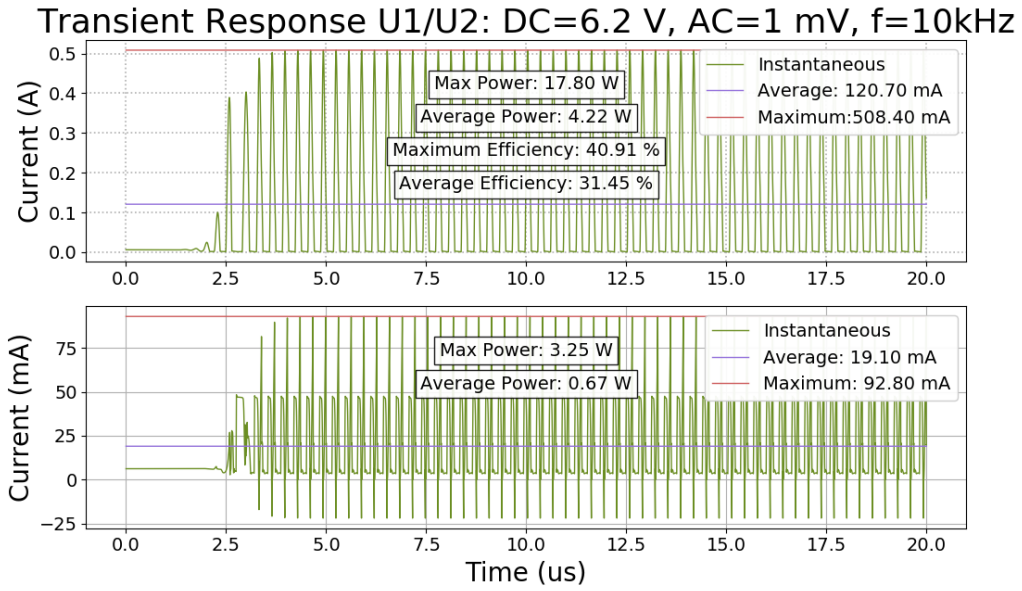


Figure 24: The transient response for $Tracker_{012}$ is presented in this figure showing current (A) on the y-axis, and time (s) on the x-axis. The load information corresponding to U1 and U2 is displayed in the top figure and bottom figure respectively. In both figures the "Instantaneous" current is in green, the "Average" current is in purple, and the "Maximum" is in red; the maximum, and average power derived from each instantaneous current signal is presented in text labels, with the top figure (U1) showing the overall system efficiency.

### 4.2.2 High-Side Switch

The following data presented in Figure 25 is sampled from the circuit in Figure 15 in subsection 3.1.

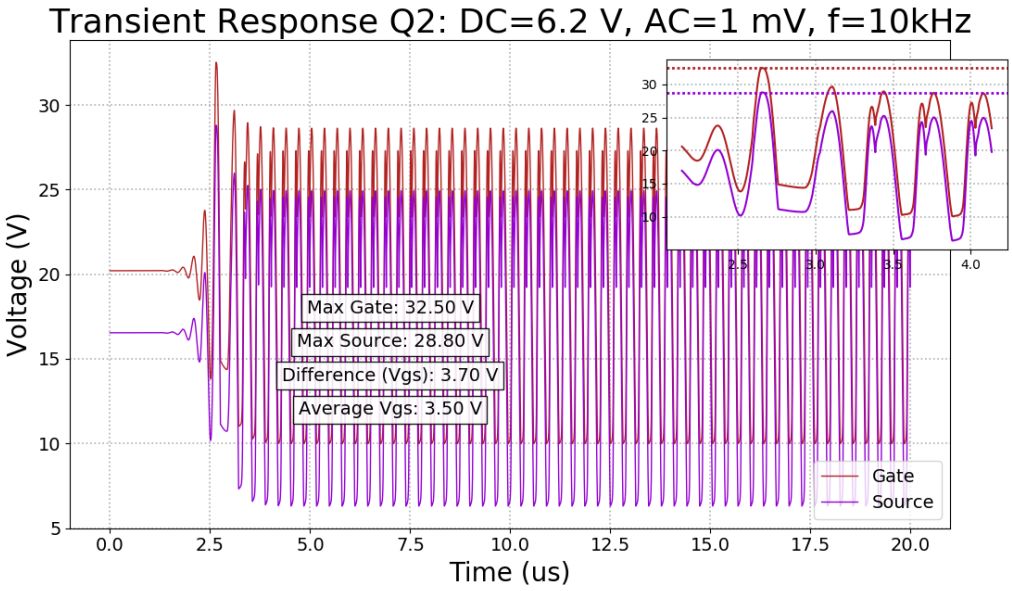


Figure 25: The time-domain response of the circuit from Figure 15 is presented in this figure, whith voltage (V) on the y-axis, and time (s) on the x-axis. The "Gate" voltage voltage is presented in red, while the "Source" voltage is in purple; there is also a small zoomed window in the top-right corner, and three text labels describing the gate-source voltage.

The two signals are "Gate" in red, and "Source" in purple; they are also displayed in a smaller, but zoomed window in the top-right corner. The "Max Gate" voltage, "Max Source", and "Difference" voltage values are inserted into the center of the figure. The next figure presented in Figure 26 is sampled from the circuit in Figure 15 in subsection 3.1, where the Fast-Fourier transform of the linearized gate voltage is displayed producing the voltage magnitude (V) on the y-axis against frequency (Hz) on the x-axis. The resulting "Gate" waveform is presented in red leaving a zoomed mini-window in the top-right corner.

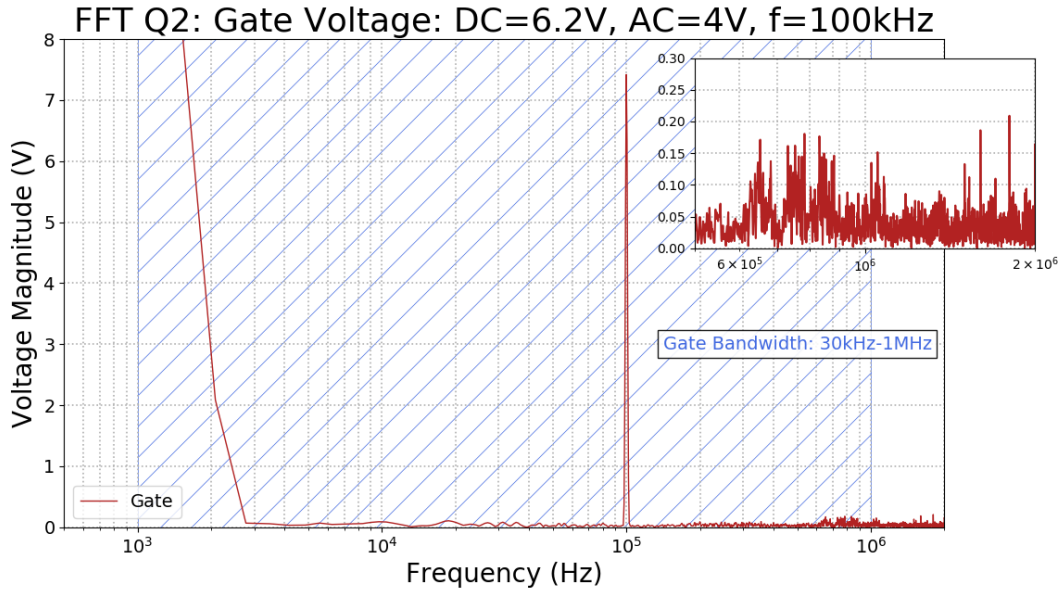


Figure 26: The fast Fourier transform of the transient response from Figure 25 is presented in this figure; see Figure 15 for the circuit. The "Gate" voltage's Fast-Fourier transform information is in red; note the zoomed window in the top-right corner.

## 4.3 Tracker Innovation Simulation

The information presented in this portion is the result from simulating the design decisions made in subsection 3.2. The structure of this segment of the report is in accordance with the design segment, where the digital current control data is presented, followed by the two differing charge pumps, and then finally the linear regulator.

### 4.3.1 Current Control Feedback

The following data presented in Figure 27 is sampled from the circuit in Figure 19 presented in subsubsection 3.2.1. The figure shows the time-domain information of the non-overlapping square wave control signals, where the voltage (V) is plotted on the y-axis, and the time (s) is plotted along the x-axis. The input signal to the circuit is $DC = 1.0V$, $AC = 0.8V$, and $f = 1MHz$. The "Input" is in red, while the "Phase1" and "Phase2" output control signals are denoted by dark-green and light-green respectively. There is a miniature window in the top-right corner showing the three wave-forms in greater detail. The "Maximum" power, and the "Average" power is amended to the figure via a text string.

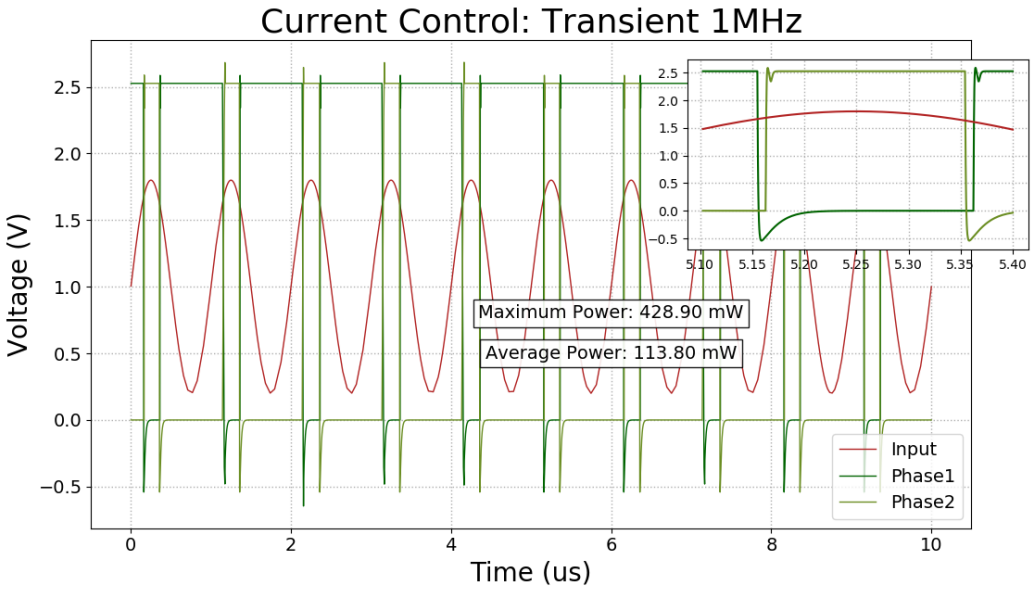


Figure 27: The figure plots the voltage (V) against time (s) on the y-axis and x-axis respectively; the data is produced by the current control feedback circuit from subsubsection 3.2.1. The "Input" (red) produces the two output signals names "Phase1" (dark green), and "Phase2" (light green). A detailed close up of the three signal is presented in the upper-right corner, with power consumption data presented using text strings.

### 4.3.2 Charge Pump

The following data presented in Figure 28 is sampled from the circuit in Figure 20 found in subsubsection 3.2.2, where the signals are composed of voltage (V) values located on the y-axis, that are plotted against time (s) on the x-axis.

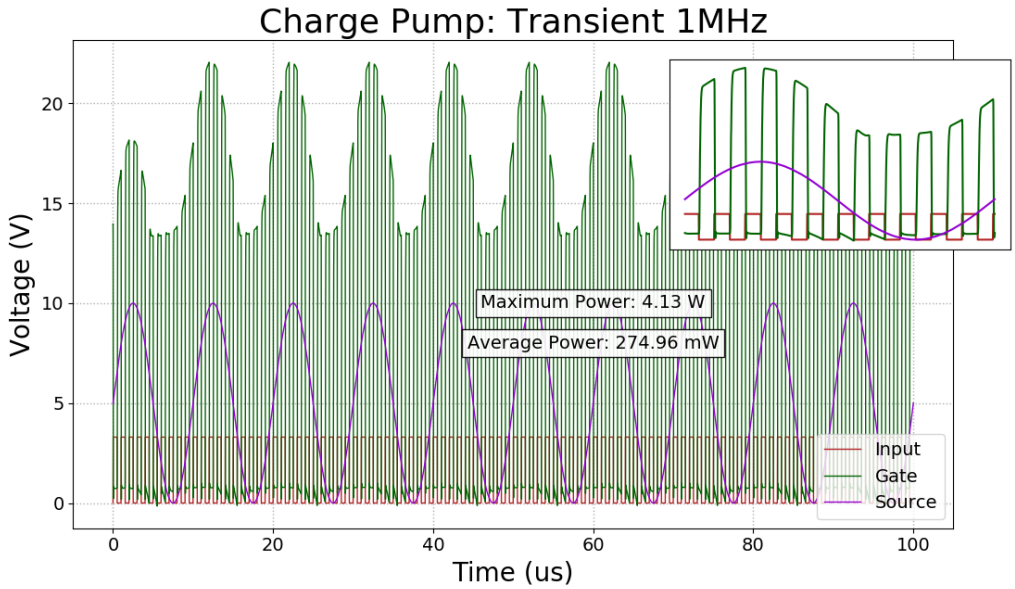


Figure 28: This is a charge pump. The circuit is controlled by a square "Input" (red), that pumps the "Gate" (green) voltage so that it is above $(12V - 15V)$ above the "Source" (purple); text strings define the power consumption.

The time-domain information is sampled using a $3.3V$ $f = 1MHz$ $50\%duty - cycle$ input square wave. The "Input" voltage in red produces the output voltage named "Gate" in green; this is placed on top of the "Source" voltage in purple. There is a zoomed portion of the waveform in a smaller window located in the top-right corner of the figure, and the "Maximum" and "Average" power consumption noted via text labels.

### 4.3.3 Integrated-Circuit High-side Driver

The following data presented in Figure 29 is sampled from the circuit in Figure 21 found in subsubsection 3.2.3, where the signals are composed of voltage (V) values located on the y-axis, that are plotted against time (s) on the x-axis. The time-domain information is sampled using a $3.3V$ $f = 1MHz$ $50\%duty - cycle$ input square wave. The "Input" voltage in red produces the output voltage named "Gate" in green; this is placed on top of the "Source" voltage in purple. There is a zoomed portion of the waveform in a smaller window located in the top-right corner of the figure with the "Maximum" and "Average" power consumption presented in text.

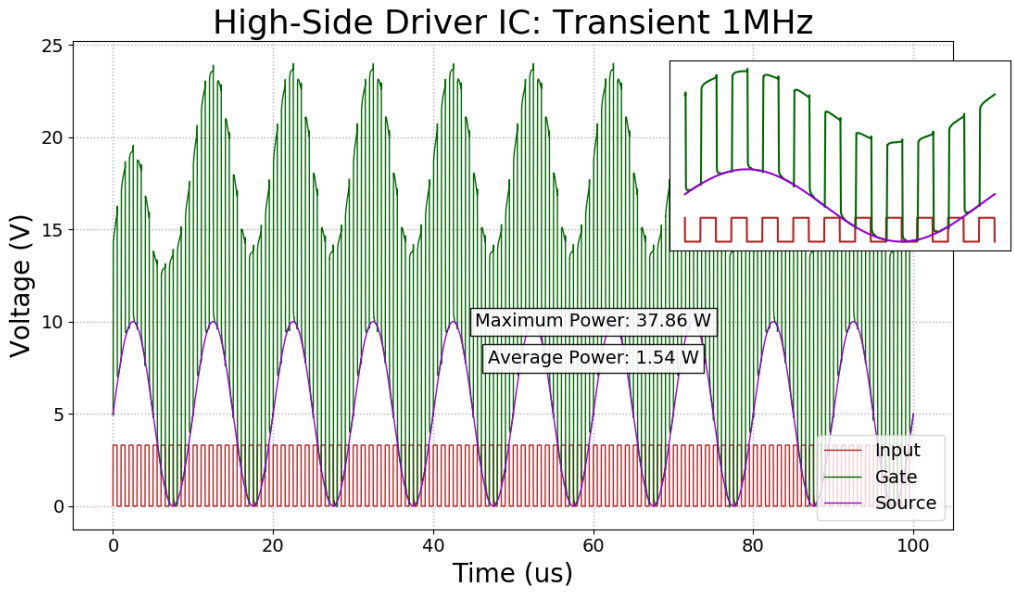


Figure 29: The change in voltage (V), on the y-axis with respect to time (s) on the x-axis, of the integrated circuit driver (transient waveform) is presented in this figure. The square "Input" (red) commutates the green "Gate" voltage that is pushed above the purple "Source" voltage using a boot-strap capacitor and a diode. Text strings define the power consumption.

### 4.3.4 Linear Regulator

There are a total of four different figures in this section derived from the circuit in Figure 22 located in subsubsection 3.2.4, where the first two are time-varying information, and the last two are frequency-varying information. Time-domain plot voltage (V) on the y-axis against time (s) along the x-axis, leaving frequency-varying information to plot magnitude (dB) and phase (degrees) on the y-axis against frequency (Hz) along the x-axis. The following data presented in Figure 30 showcases the varying "Output" voltage in purple in response to the "Input" voltage in red; the input and output variations respectively are $DC = 6V$, $AC = 4V$, and $17.5V$, $AC = 12V$ at $f = 1MHz$. The "Maximum" and "Average" drain efficiency of the circuit, along with the "Maximum" and "Minimum" output voltage is displayed using text stings.

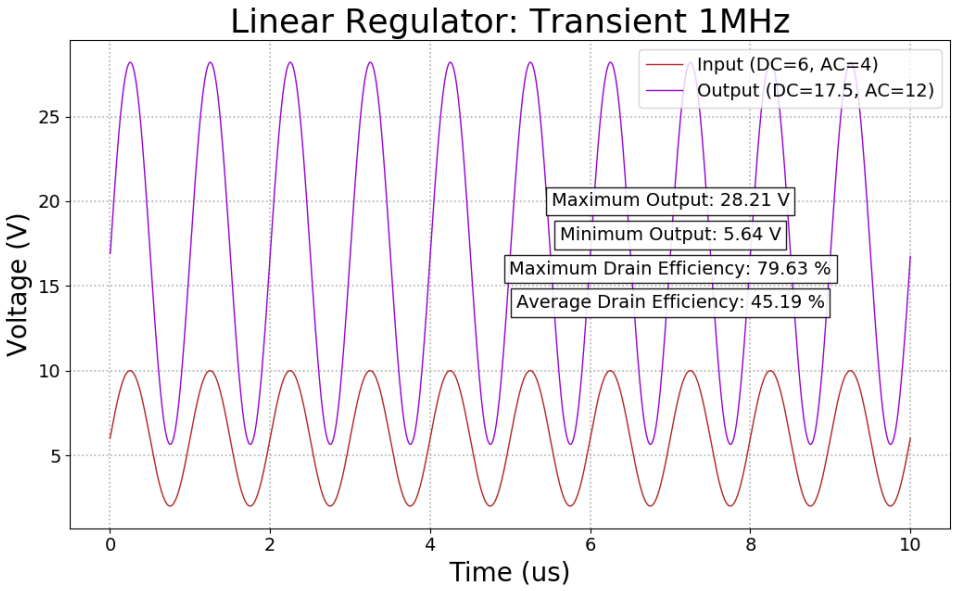


Figure 30: The transient waveform of the linear regulator, voltage (V) is on the y-axis and time (s) is on the x-axis, where the "Input" is displayed in red, and the corresponding output is in "Purple"; the circuit that produces this information is described in subsubsection 3.2.4. Particular details of the waveform is presented using text strings.

Moving on from time-domain analysis, is that of the frequency domain. The information embedded in Table 14 is the outcome of using the equations from subsubsection 3.2.4, where the indented $3dB$ corner frequency produces a C1 capacitor value of $2.5pF$. This is however, not reflected in the "Simulation" column where a smaller frequency is realised. $80MHz$ is the specified corner frequency, and Table 15 shows the new simulation adjusted parameters.

Table 14: The initial calculated closed-loop bode parameters for the linear regulator (C1=2.5pF)

| Parameter | Abbreviation | Calculated | Simulation | Unit |
|---|---|---|---|---|
| Dc Gain | $AV_{DC}$ | 9.4 | 9.4 | dB |
| 3dB Corner Frequency | $f_{3dB}$ | 80 | 68 | MHz |
| Unity-gain Frequency | $f_{0dB}$ | 117 | 140 | MHz |
| Phase Margin | $PM$ | - | 147 | ° |
| Gain Margin | $GM$ | - | 137 | dB |

The information in the table below is derived using a smaller C1 capacitor value of $2.0pF$, found by simulating the circuit (Figure 22) after the initial calculations described in the previous table; ideal performance parameters are obtained upon completion. The information from this table is visually depicted below.

Table 15: Simulation corrected closed-loop bode parameters for the linear regulator (C1=2.0pF)

| Parameter | Abbreviation | Calculated | Simulation | Unit |
|---|---|---|---|---|
| Dc Gain | $AV_{DC}$ | 9.4 | 9.4 | dB |
| 3dB Corner Frequency | $f_{3dB}$ | 99.5 | 79.1 | MHz |
| Unity-gain Frequency | $f_{0dB}$ | 146 | 137 | MHz |
| Phase Margin | $PM$ | - | 156 | ° |
| Gain Margin | $GM$ | - | 4.7 | dB |

Figure 31 shows the bode magnitude and phase information for the linear regulators closed-loop

frequency response. The upper sub-figure plots the "Magnitude" (dB) in red against frequency (Hz). The "Phase" is displayed in green in the lower sub-figure, with specifics of the figure displayed using text stings. The circuit responsible is constructed with the relations discussed in subsubsection 3.2.4; the following tables show the results of the design process.

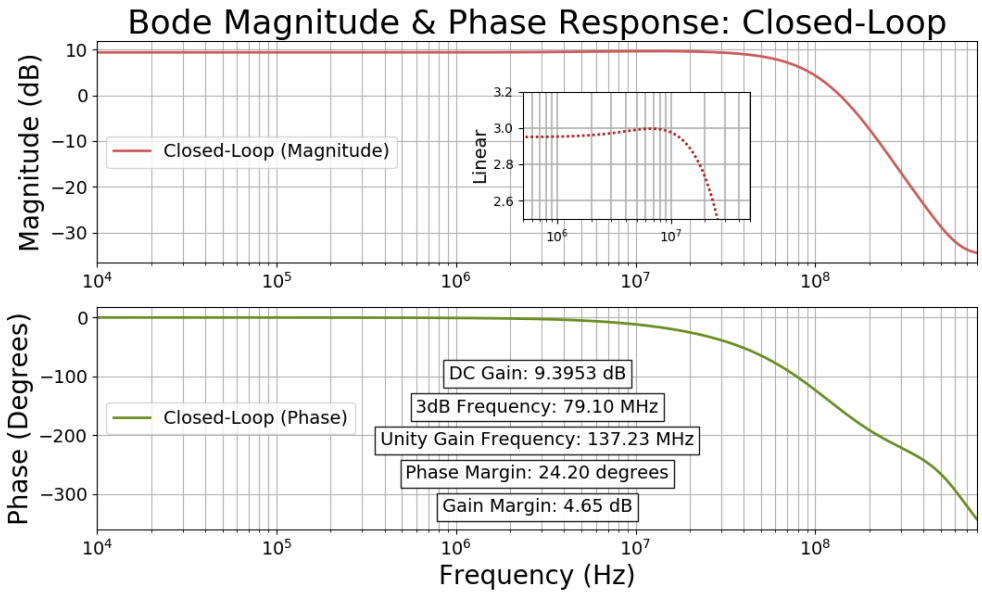


Figure 31: The closed-loop response of the circuit in subsubsection 3.2.4 is presented in this figure, where the top figure is the "Magnitude" in red, and the lower figure is the corresponding "Phase" in green. The top figure plots magnitude in decibels (dB) over frequency in hertz (Hz), while the lower figure plots the phase in degrees over frequency. Details regarding the gain margin, phase margin, corner frequency, unity gain frequency, and DC gain are presented in the upper figure. Note that the zoomed window in the top-right is in linear units.

The final figure markets the same category of information as the previous, however, the loop-gain response is displayed instead of that of the closed-loop; his information is needed to confidently state circuit stability. Moving on from the innovation section are the results from $Tracker_{021}$, where all the information investigated by this project is invested.

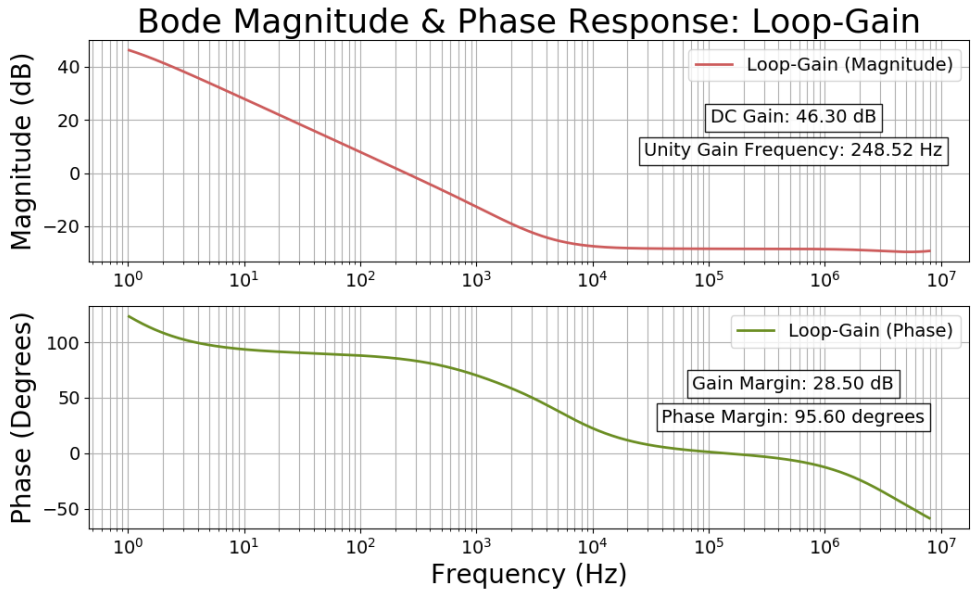


Figure 32: The bode plot used for the loop-gain stability analysis is presented in this figure, where the top figure is the "Magnitude" in red, and the lower figure is the corresponding "Phase" in green. The top figure plots magnitude in decibels (dB) over frequency in hertz (Hz), while the lower figure plots the phase in degrees over frequency. This circuit is found in subsubsection 3.2.4, and details regarding the gain margin, phase margin, unity gain frequency, and DC gain are presented in the upper figure.

## 4.4 Tracker(021) Simulation

Results from the final simulations of the second tracker architecture ($Tracker_{021}$) are presented in this section; the information is either pure transient or frequency information derived from transient analysis (Fourier analysis). The circuit under test is introduced in subsection 3.3, and the circuit is defined in Figure 23. The section begins with the input-output waveforms beginning from low to high frequency, followed by switch-mode control analysis, Fourier, and then concluding with sub-system power consumption.

### 4.4.1 Transient Analysis

The following section displays the varying time-domain responses of the circuit, where the input amplitude and frequency is adjusted to observe the differing output waveforms. The first figure excites the architecture with an input signal ($DC = 6V$, $AC = 4$, & $f = 100kHz$), that produces the following output seen in Figure 33; voltage (V) is on the y-axis, leaving time (s) on the x-axis. The "Input" is in red, the "Output" is in purple, the "Ideal" output is a dashed red line, the "Duty" signal from the comparator output is shown in green, leaving the "Phase1" signal, that is used by the charge pump, in blue. A close-up view is in the top-right corner, the appended date in the left-hand-side details the dynamic range (minimum, and maximum voltage), the average efficiency, and the average system gain in linear units. The proceeding figure shows the input-output relation for high frequencies.

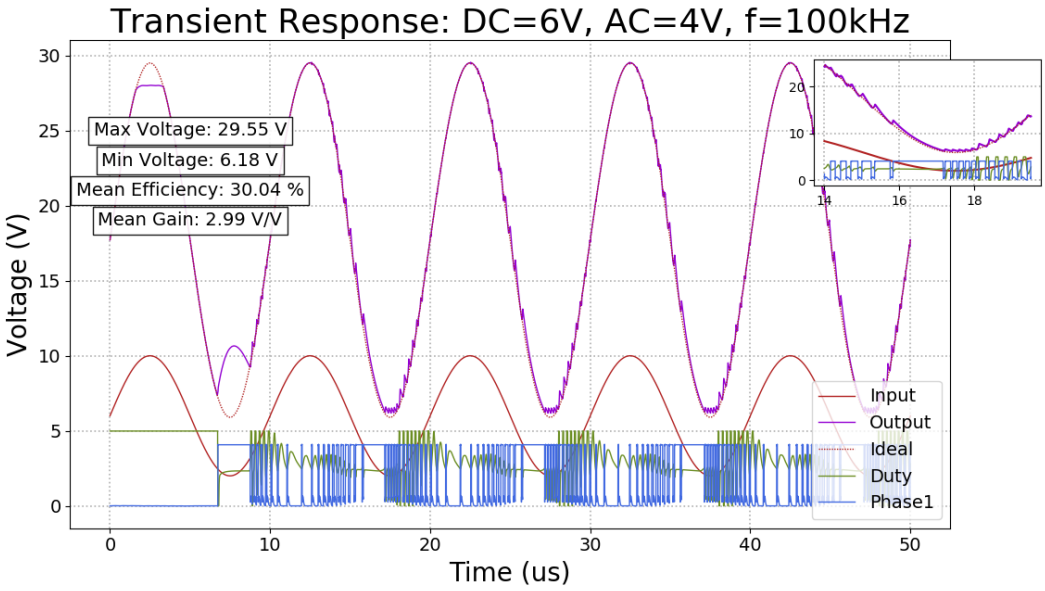


Figure 33: The time-domain response for the final tracker architecture is presented in this figure, where the "Input" is in red, the "Output" is in purple, the "Ideal" output is a dashed red line, the compactor's "Duty" output is in green and the "Phase1" control signal is in blue. A zoomed window in the top right corner, and text strings describing dynamic range and efficiency, aid the figure.

Figure 34 shows the same assortment of information as the preceding figure, however, the excitation is increase from $100kHz$ to $1MHz\&25MHz$ respectively. This figure concludes the input-output transient results, where the section now moves on to cover the switch-mode control signals.

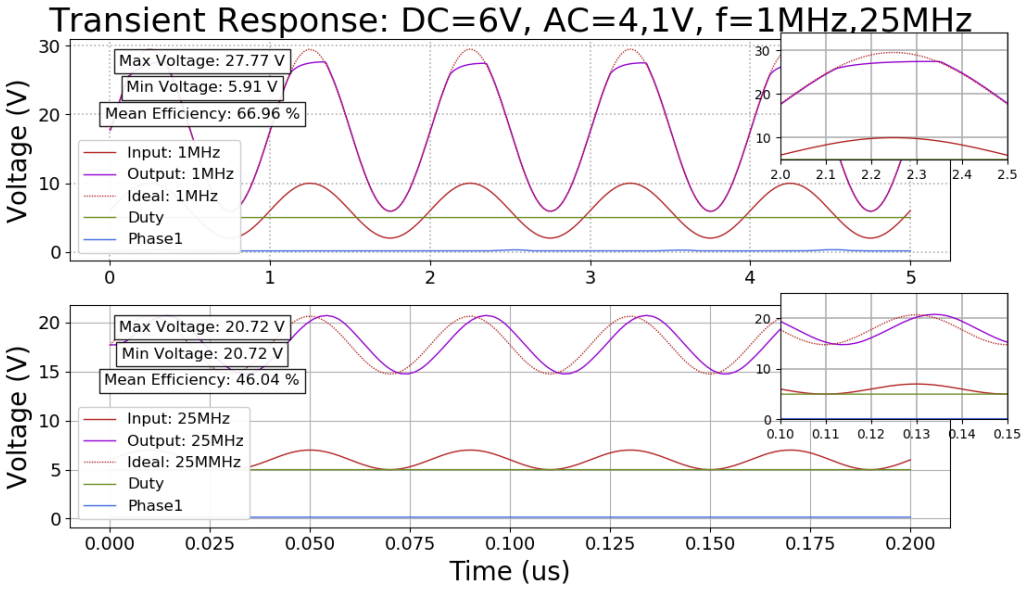


Figure 34: This figure shows the output, and input waveforms for $1MHz\&25MHz$ input frequencies. The "Input" is in red, while the "Output" is in purple, and the "Ideal" output is shown by the dashed-red line. There are also two control signals, "Duty" and "Phase1" that show the activity of the switch-mode regulator; information relevant to the waveforms are appended in the top left corner.

While the comparator output and charge pump control signals are shown in the previous two figures, they are broken down here for clarity purposes. Figure 35 shows the "Input", "Gate", "Source", and "Phase1" switch-mode control signals in red, purple, blue and green respectively. A magnified window in the top right corner shows the signal's in greater detail, leaving the general waveform information that is appended on the lefty-hand-side of the figure; namely the maximum gate voltage, the maximum source voltage, and the average power consumption of the charge pump. The transient solution used to plot this information is hereafter interpreted using Fourier analysis in the next figure.

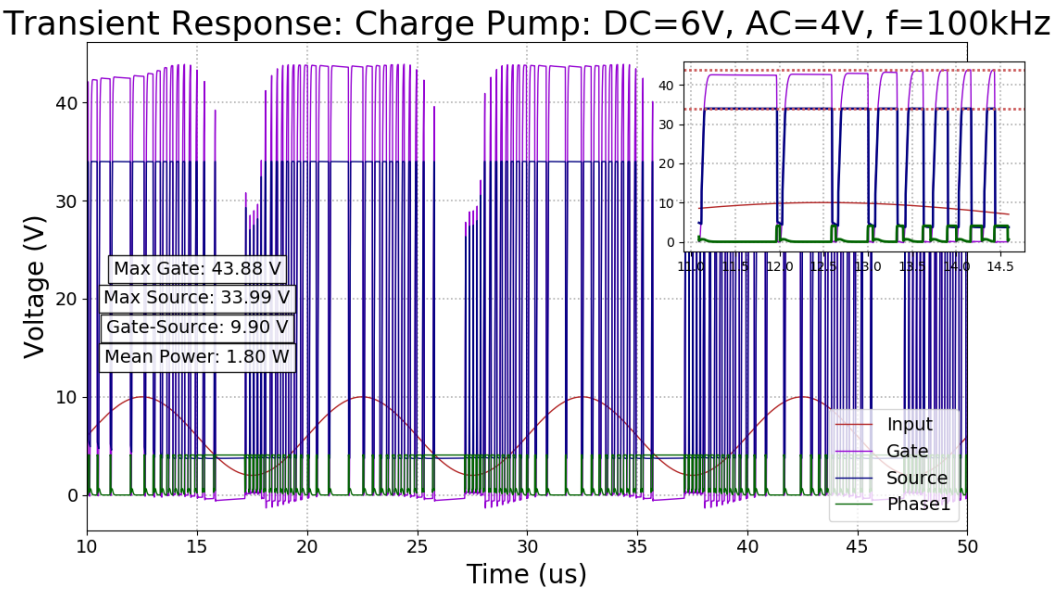


Figure 35: The control of the switch-mode regulator is introduced in this figure, where information regarding the data as a whole is appended on the left-hand side, the close-up view is in the top right corner, and the legend is in the bottom right. The "Input", "Gate", "Source", and "Phase1" signals are represented by red, purple, blue, and green respectively.

The following data presented in Figure 36 where the Fast-Fourier transform of the linearized gate voltage is displayed producing the voltage magnitude (V) on the y-axis against frequency (Hz) on the x-axis. The resulting "Gate" waveform is presented in red leaving a zoomed mini-window in the top-right corner; the blue hashed box shows the target bandwidth of the switch-mode gate control signal ($1kHz - 1MHz$). The power consumption of the various sub-systems of $Tracker_{021}$ are shown in the following figure (Figure 37). The 50Ω "Load" is in red while the "Power", "Logic" and "Gate" supplies are shown in purple, dashed-red, and green respectively; the power consumption of "U1,2" is given by light-blue and dark-blue respectively. A up-close window of the waveforms, excluding the logic supply's power consumption, is plotted in the top-right corner. Finer details such as the maximum power consumption of the logic supple, the maximum current of U1, and the average current of U1 are plastered on the left-hand-side of the figure. This figure now concludes the results section of this report, where it now moves onto the discussion that breaks down the finding made here with the design, and theory sections.

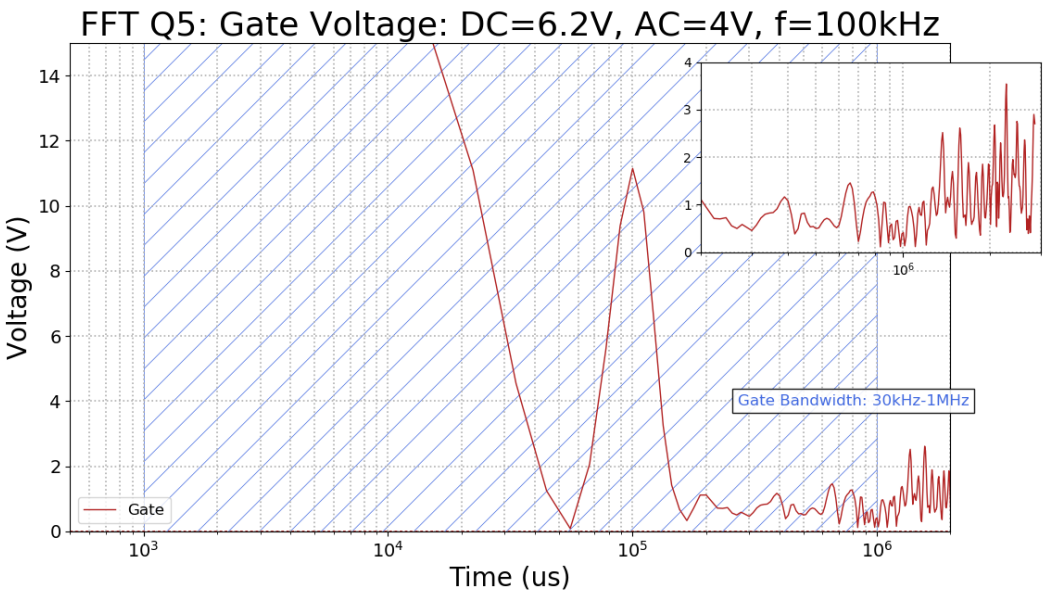


Figure 36: The Fast-Fourier Transform of the switch-mode regulator's "Gate" voltage is provided in this figure. A zoomed upper frequency portion is given in the top-right corner, and the blue hashed box designates the band-width of interest.

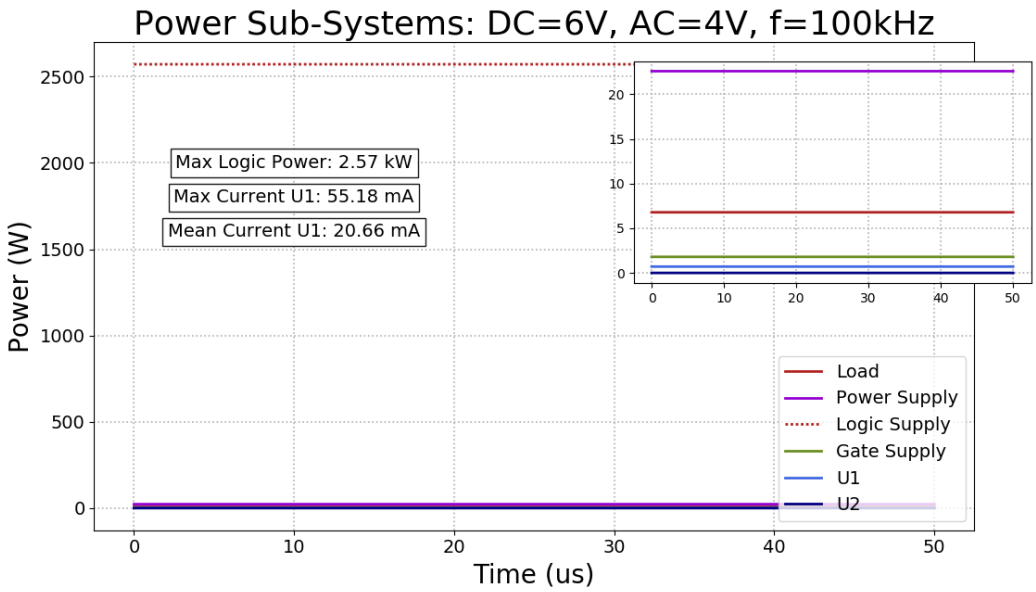


Figure 37: The differing average power consumption for the various subsystems ("Load" (red), "Power Supply" (purple), "Logic Supply" (dashed-red), "Gate Supply" (green), "U1" (navy-blue), and "U2" (dark-blue)) are depicted in this figure. Extra information regarding the data is appending to the upper-left-hand corner. A zoomed version is provided in the top-right corner that excludes the "Logic Supply".

# 5 Discussion

The results presented in the proceeding section are the results from the project narrative, where an initial prototype ($Tracker_{011}$) derived from the previous masters project ([1]) and designed in subsection 3.1, serves as a proof of concept based on the results from the master project's investigation; this is expected to reveal the physical imitations of the current understanding. The findings from the prototype then moves on to motivate the second simulation of the initial architecture ($Tracker_{012}$) described in subsubsection 3.1.4 to better understand architecture one. This information is then processed, and then used to create improved circuity in the innovation section (subsection 3.2). The project narrative hereafter employs the total understanding from all sections, and then composes the second architecture ($Tracker_{021}$). With the project's chronicle now clear, the discussion naturally begins at the start with $Tracker_{011}$. It should be noted that the following material is discussed with regard to the relevant sections mentioned prior to this division; consult the relevant sections for more information.

## 5.1 Tracker Architecture One

The following discussion section breaks down both the $Tracker_{011}$ prototype, and the $Tracker_{012}$ simulation to discuss architecture one ($Tracker_{01X}$) as a whole. The investigation of $Tracker_{01X}$ is carried out with the main goal of improving the efficiency with as little collateral damage to the other system parameters such as output ripple and bandwidth. To be clear, the objective of this entire investigation is to explore $Tracker_{01X}$ so that $Tracker_{02X}$ will be more efficient. Both architectures are composed of linear, and a switch-mode sub-system; the following two modules are discussed accordingly.

### 5.1.1 Linear Regulator

The linear regulator is denoted by U1, and is physically realised by the current feedback OPAMP $THS3001$ by Texas Instruments; see subsubsection 3.1.2 for more details. The main problem associated with this subsystem is its expected current loading that is plainly seen from the results. subsection 4.1 presents the initial problem where the prototype could not drive the expected 50Ω load resulting in the complete failure of U1. The demise of $Tracker_{011}$ motives the investigation of $Tracker_{012}$ in subsection 4.2, where the power and current loading of U1 is of particular interest. With reference to top sub-figure in Figure 24 and [2], the average current of $\approx 120mA$ is below the absolute rating of $175mA$, the instantaneous current is not; the maximum current output from U1 is $\approx 500mA$. The design therefore exceeds the capabilities of the active device causing it to fail. The average power output of $\approx 4.2W$ ($\approx 18W$ maximum) is far more than what the OPAMP's case (SOIC-8) can practically manage through means of thermal dissipation; the case's thermal power rating is $\approx 1W$. U2 on the other-hand has a peak current load of $\approx 93mA$ that is within specification, and an average power load of $\approx 0.67W$ ($3.25W$ maximum) making it also within specification. With the linear section concluded this discussion now moves onto the discussion surrounding the switch-mode operation.

### 5.1.2 High-Side Switch

The investigation of the gate of Q2 (Figure 15) is motivated by its apparent heating when driving the 50Ω load during laboratory verification. This is further confirmed by Figure 25 located in subsubsection 4.2.2, where the maximum gate voltage of $3.7V$, and average of $3.5V$ yield that the gate of Q2 is not being driven as a current "switch" and is instead more in-step to that of a linear regulator; a emitter-follower to be more precise. Q2 is represented by two separate MOSFETS, for the case of the prototype it is STD155N3LH6 ([9]), and simulation it is IRF540N ([10]); see subsubsection 3.1.1 for more details. While the first MOSFET has a smaller gate-threshold voltage of $2.5V$ (maximum), than the latter of $4.0V$ (maximum), the average gate-source voltage of $3.5V$ is potentially a hazardous design margin. It cannot ensure that the MOSFET is in hard saturation

thus reducing the resistance between its drain-source; thermal run-away is therefore a real issue. Moving onto the frequency composition of the gate signal shown in Figure 26, the majority of the power signal power appears to be located at or around DC($f \leq 20kHz$). This further supports the emitter-follower statement that the gate of the Q2 is not acting as a current switch and is instead acting as a buffer. The zoomed miniature window located in the same figure, however, shows a $\approx 3V - 5V$ spike at between $\approx 100MHz - 200MHz$. Frequencies of this magnitude are not intended to be placed at the gate due to the added losses caused by switching loss, as described in subsubsection 2.2.2. The aim of this project is have a varying gate control frequency in the range of the hashed blue box ($30kHz - 1MHz$). Note that the magnitude is not defined, and therefore extends beyond the scope of the graph. It is in-fact the gate-source ($V_{GS}$) voltage that is of importance, however, the gate voltage is investigated in this figure since it should be independent of the source voltage. Armed with the issues discussed in this section, the report moves onto the innovation section that acts as the solution space.

## 5.2 Tracker Innovation Simulation

In this section, the design decisions made in subsection 3.2 are discussed in contrast with the simulation data presented in subsection 4.3, to justify the solutions to the problems presented in the previous section (subsection 5.1). The current loading problems associated with U1 are initially addressed, followed by the control signal for the switch-mode regulator, and then finally the driver circuit for the high-side switch.

### 5.2.1 Linear Regulator

The linear regulator developed in subsubsection 3.2.4, presented in Figure 22, is one of the three main developments of the innovation section where its simulation performance results are shown in subsubsection 4.3.4; see Table 11 for the specification. The motivation for this circuit is to decouple the current load from U1 in the case of $Tracker_{01X}$, while maintaining the speed of the system. The time-varying simulation presented in Figure 30 shows a 0.74% error at a maximum output voltage of $28.21V$, and a 6% error for the smallest output voltage ($5.64V$); less than 1% for both extremes is the ideal scenario, however, it is good enough for the development of $Tracker_{021}$. The maximum, and average efficiency for the linear regulator is as expected, and while small increase are possible, there is no considerable increase in efficiency possible with this architecture. Moving onto the bode information, hand calculations from subsubsection 3.2.4 are used to rough-out the design; namely Equation 20 and Equation 12. The difference between the calculated and simulated AC-signal parameters of Table 14 and Table 15 are believed to be due to the simplification of the closed-loop transfer-function (Equation 19), where the emitter-follower Q1 is assumed to be an ideal buffer. In reality, the gate resistor (R3) and the impedance of Q1 itself will cause a change in the intended dominant pole design (R2 & C1). Once C1 is adjusted the closed-loop response in Figure 31 shows that the gain of the circuit dips off nicely providing the specified of $\approx 80MHz$. The linear DC voltage gain ($A_V^{DC}$) is equal to 2.95 while its specification states 3.0; 98% accuracy is considered acceptable. The closed-loop phase and gain margins are $24°\&4.65dB$ respectively, and while these values are an indication of stability, it is the equivalent loop-gain parameters that make or break the circuits stability; the loop-gain phase and gain margins are $95.6°\&28.5dB$ respectively denoting the circuit stable. With the linear regulator now defined, the discussion moves onto the first step in realising the switch-mode sub-system; current control feedback.

### 5.2.2 Current Control Feedback

The current control feedback circuit, employing digital logic devices to create two 180° non-overlapping control signals, displayed in Figure 19, acts to achieve two things. The first is to create a pulse modulated control signal at a low voltage, that can be used to control current injection. The last is to act as a comparator. These characteristics are best shown in Figure 27, where the input sinusoidal voltage is not square in nature, the logic circuit converts the varying input into a modulated output that is square in nature. The two non-overlapping control signals

(Phase1,2), exhibit an designed delay of $\approx 10ns$ that helps to maintain the integrity of the two signals, while the average power usage of the circuit is manageable at $114mW$. The next phase of the switch-mode regulator is to translate this control signal into something that can drive the gate of the high-side MOSFET.

### 5.2.3 Charge Pump

This report investigates two different charge pump methods in parallel, where one is designed from first principles, while the other is a marketed product; these two circuits are shown in Figure 20 and Figure 21 respectively. Both circuits exhibit excellent charge-pump behavior at $1MHz$, where the gate is pushed $12V - 15V$ above the the sinusoidal voltage at the source of the device, while maintaining a square waveform; this is important as Q1 should come all the way off when not in use. The high-side driver IC has the advantage of only dropping the gate voltage to that of the source voltage thus reducing the output swing of the circuit, and improving the slew-limiting load. It does, however, on average use more power than the engineered charge pump therefore removing it from the $Tracker_{021}$ revision. An observation is the relative smaller magnitude of gate voltage upon the start-up of both circuits. This is due to the the boot-strap capacitor (C1) being initially depleted of charge. One final point to discuss is the steady-state problem of this circuit. It relies on the reset of the input control signal, where a logically high signal over an extended duration of time will deplete the charge of C1, and therefore cause the voltage across it to drop; this will result in either the poor performance or total failure of Q1.

## 5.3 Tracker(021) Simulation

This investigation focus on the development of two differing circuit architectures for envelope tracking ($Tracker_{01X}$&$Tracker_{021}$), where the aim is to use a hybrid regulator aimed to meet the specifications in Table 2; output transient behaviour, regulation method, and efficiency are the prioritised investigation results and are naturally the start of discussion. The tracking architecture of interest is developed in subsection 3.3, and is presented visually in Figure 23. The concepts developed in the theory section (section 2), are used in the coming breakdown of $Tracker_{021}$, and should be consulted for finer details; see subsection 3.2, and subsection 3.3 for rationalisations for the design decisions made. The passage now moves onto the transient breakdown of the tracker architecture.

### 5.3.1 Low-Frequency Transient Analysis

The behaviour of the time-dependent waveforms presented in subsubsection 4.4.1 are discussed first. With reference to Figure 33, it is evident that the output responds well to maximum input signals ($6V - 10V$) at $f = 100kHz$ with a linear gain of $2.99\frac{V}{V}$; this is a 1.3% error compared with the gain from Table 15. The output produces roughly the intended dynamic range, however, this may be readily adjusted by tuning the DC offset, and the linear regulator's gain via R1 in Figure 23. The "Duty", and "Phase1" signals, the comparator and current control feedback output respectively, show that the switch-mode regulator is functioning as intended. How the output "Phase1" control signal changes in pulse duration of significance as it is wider when the output is high ($\approx 28V$), and then narrow when the output is low ($\approx 6V$). Note that "Phase1" drives an inverting BJT device that therefore requires it to be inverted from the actual current control signal ("Phase2" in this case). One interesting observation of these two signals is the reduction in the comparator output when the output node changes quickly or is at its maximum. The relative rise and fall of the green "Duty" comparator output is also faster on the rising and slower on the falling edge. This could suggest that the switch-mode supply cannot inject current into the output node fast enough thus causing a drop in comparator output resolution; the linear regulator can get current across the shunt resistor (R5) faster. Solutions could be to increase the gain of the comparator, decrease the inductor size, or increase the speed of the switch-mode regulator. The efficiency on the other-hand is, however, in need of some attention at an average of $\approx 30\%$; this is currently worse than a pure linear tracker variant. It should also be noted that this is not the overall efficiency, and is rather

the overall efficiency minus the consumption of the digital power supply. According to Figure 37 the logic supply uses a maximum of power rate of $\approx 2.6kW$, which is extremely high, and not in accordance with the results from Figure 27 that showed a maximum/average power consumption $\approx 429mW\&114mW$ respectively at $1MHz$. Power consumption of this magnitude corresponds to a load of $\approx 5m\Omega - 10m\Omega$; the contribution of the logic supply is therefore not accounted for in the efficiency calculation. There are two buffer circuits with in the current control feedback circuit, where only one is used, meaning that the buffer circuit for "Phase2" may be removed; this will only half the power consumption leaving a power value that is still of concern. There is something interesting regarding this information that may be resolved in the form of fixing a circuit bug, investigating the Pspice models used by the current control feedback block, or by changing the circuit entirely.

### 5.3.2 High-Frequency Transient Analysis

The $1MHz\&25MHz$ time-varying information presented in Figure 34, shows that the output is dominated by the linear regulator, where the switch-mode regulator appears to be dead apart from the output deviation in the top figure; this is believed to be the result of incorrect charge-pump operation. According to subsection 2.3, the switch-mode regulator is not need, and should not operate at frequencies over $1MHz$ due to the relative little amount of power in that section of the spectrum meaning that efficiency is less of a concern; this is instead left for the linear regulator. It should, however, operate at $1MHz$ where it currently does not. It can be seen that the comparator output ("Duty") is high meaning that the switch-mode regulator is instructed to drive the gate of Q5 ("Phase1" is low thus the push-pull gate should be pulled to "vcap" via R8); this, however, does not happen. One theory is that the circuit gets "stuck" in one state, where $vcc_{gate}$ must be set by pulling the gate of the push-pull circuit to ground via Q2, thus placing $vcc_{gate} - 0.7V$ ($0.7V diodedrop$) on the left-hand-side ($vcap$) of the boot-strap capacitor (C3). One solution is to use the inverted signal "Phase2" to reset the charge pump; this is discussed in more detail in the future work section (**??**). The $25MHz$ plot in the lower figure of Figure 34 show pure linear operation, that is an engineered design aspect of the hybrid tracker. The output shows a slight delay compared to the input, and decreased efficiency compared to the top figure that has a larger dynamic range; this is due to the DC offset placed at $\approx 18V$ causing a loss in efficiency with reduced dynamic range. This concludes the high frequency transient analysis, where the discussion moves onto further analysis of the switch-mode control system and further analysis of the high-side switch.

## 5.4 High-Side Switch

This section is formulated with respect to the results from subsubsection 4.2.2, that shows an insufficient gate-source voltage, and a fixed gate driving frequency proportional to the excitation frequency from Figure 26. The goal of the charge pump developed in this investigation is to efficiently "shift" the gate of Q5 adequately above the "source" voltage to effectively commutate the high-side switch (Q5). With reference to Figure 35, the charge pump achieves just that, where the average gate-source voltage is $\approx 9.9V$ opposed to $3.5V$ from $Tracker_{01X}$. This voltage is sufficient to commutate the MOSFET resulting in a much larger in-rush current, and is the reason for the larger inductor (L1) between the source and the output node compared to $Tracker_{01X}$. Figure 36 shows one other interesting point where the Fast-Fourier of the gate voltage to Q5 appears to spread over a greater bandwidth compared to Figure 26. This is supportive of a gate driving voltage that is less proportional to the excitation envelope signal, and is more independent. This is desired, since the hybrid-tracker is intended to switch current to its output when needed; this would cause varying switching frequency, and also a varying duty cycle. This method also has the added benefit of introducing switching frequencies that vary over a greater bandwidth, and therefore hopefully spreading the error introduced by the switching frequency over the output spectrum.

# 6 Future Work

Between $Tracker_{01X}$ and $Tracker_{021}$, positive momentum is created, however, there is work to be done with regard to controlling the self commutation of the switch-mode regulator. One area of focus is to work out an efficient method to reset the current control feedback signal ("Duty") so that the boot-strap capacitor can effectively sample, and then place $vcc_{gate}$ above the source voltage. One method is to increase the voltage gain of the comparator to make the feedback network more sensitive; the shunt resistor should ideally maintain a value no bigger than $5\Omega$ as increasing this will cause an unnecessary voltage divider for the linear regulator at high frequencies. With regard to power consumption, the logic circuity from the current control feedback circuit should be investigated to check the validity of the $2.6kW$ power consumption; the output buffer circuits are prime candidates for investigation. Methods for improving the overall system efficiency in the target switching bandwidth should also be investigated. One such method is to use parallel charge pump circuits driving parallel high-side switches that can be optimised for specific switching windows of a given output inductor. Finally, there are optimisation possibilities regarding the output inductor value with respect to ripple suppression. After an established architecture is verified, the next phase of the project is to test the architecture with an RF PA to investigate the practically of the concept.

# 7 Conclusion

The purpose of this project is to investigate the feasibility of creating a hybrid-envelope tracker that can take advantage of the efficiency benefits of switch-mode regulators at the lower-end of the envelope bandwidth ($0Hz - 1MHz$), where most of the spectrum's power is located, while using plain linear regulation at the remaining higher frequencies ($1MHz - 80MHz$).

The beginning of the report arms the reader with the relevant theoretical tools needed for the following design section, and discussion. A previous masters project ([1]) is employed to create a proof-of-concept prototype ($Tracker_{011}$) using KiCad, that reveals the need of decoupling the current load from the non-inverting OPAMP. This is thereafter verified using accurate component models (Pspice) in an open-source spice simulator called Ngspice; this iteration is called $Tracker_{012}$. $Tracker_{012}$ also reveals that there are problems with commutation of the high-side switch. Q2 from Figure 15 experiences an average gate-source voltage of $3.5V$, and its gate appears to track its source to emulate the behaviour of a source-follower. Fourier analysis also shows that the signal driving the gate is highly proportional to the input signal; this is to be avoided, as the switching frequency is to be variable. The lessons learned from prototype $Tracker_{011}$, simulation $Tracker_{012}$, and the masters project are compiled together to produce the three areas of the innovation section; a digital current control feedback circuit, a charge pump to drive the gate of the high-side switch, and an emitter follower architecture to decouple the current load from the non-inverting OPAMP (U1) from the first architecture ($Tracker_{01X}$). The circuits relevant to the switch-mode regulator are designed to combine a square digital control signal at a low voltage ($3.3V - 5V$) that is then used to drive a charge pump; the charge pumps act as the driver for the gate of the high-side switch. Both the current control feedback circuit, and the charge pump achieve correct operation at an excitation frequency, with both presenting an average power consumption under $300mW$. The linear regulator is thereafter the next success story of the innovation section, where signal amplification of $2.95\frac{V}{V}$ is achieved, correct output swing is established, and stability is ensured with a phase and gain margin of $\approx 96°$& $\approx 29dB$ respectively. The designs from the innovation section are then directly used to compose the final tracker architecture ($Tracker_{021}$); this circuit can be seen in Figure 23.

$Tracker_{021}$ shows ideal operation at low input frequencies ($100kHz$) with regard to the circuits intended fundamental regulation concept. This is namely described by the varying pulse width of the control signal driving the charge pump ("Phase1"), seen with the output signal in Figure 33. "Phase1" of varying duty cycle then goes onto drive the high-side switch that injects current into the output node via the anti-ripple inductor that thereafter emits the output waveform. One main point of interest is the relative slow reaction of the compactor's output ("Duty"). While it is intended that the switch-mode regulator shall operate up to $1MHz$, the circuit ultimately manages to stop operation at higher frequencies leaving the linear regulator to serve as the output regulator; efficiency at this point is as expected at $\approx 50\%$. While it is encouraging to see the system reacting as intended, the average efficiency of $\approx 30\%$ when the switch-mode regulator is operating is in need of attention. One observed problem associated with $Tracker_{01X}$ is the inadequate gate-source voltage (an average of $3.7V$); this is eradicated in the second revision ($Tracker_{021}$) with an average gate-source voltage of $9.9V$. The other point regarding the new commutation architecture, is that the frequency composition of the gate voltage is broader than $Tracker_{01X}$. This is ideal since the switching bandwidth is distributed over a greater spectrum, that hopefully divides the switching noise. The relative power consumption of the differing sub-systems is well dominated by the current control feedback circuit that consumes power at a maximum rate of $\approx 2.6kW$. This is not in accordance with the information from the innovation section where the developed current control feedback circuit demonstrates sub-watt power consumption; the contribution of the logic block is therefore excluded from the efficiency calculations. One final point for the final architecture is the complete reduction of current passed by U1. The maximum and average power consumption for U1 when utilizing the emitter follower configuration is now down to $55.2mA$&$21mA$ respectively. Future endeavors regarding $Tracker_{021}$ should initially focus on increasing the voltage gain of the comparator (U2), while also analysing the large currents associated with the current control feedback circuit. There is also the opportunity to explore using parallel high-side switches with a corresponding output inductor, and reset circuity that can effectively reset the charge pump.

In conclusion, two hybrid tracking architectures are investigated, using means of simulation and verification, to produce a report that breaks down the successes and short comings of the task. This project can now serve as a base for further investigation of hybrid-envelope tracking circuits in the intent of making wireless communication more energy efficient.

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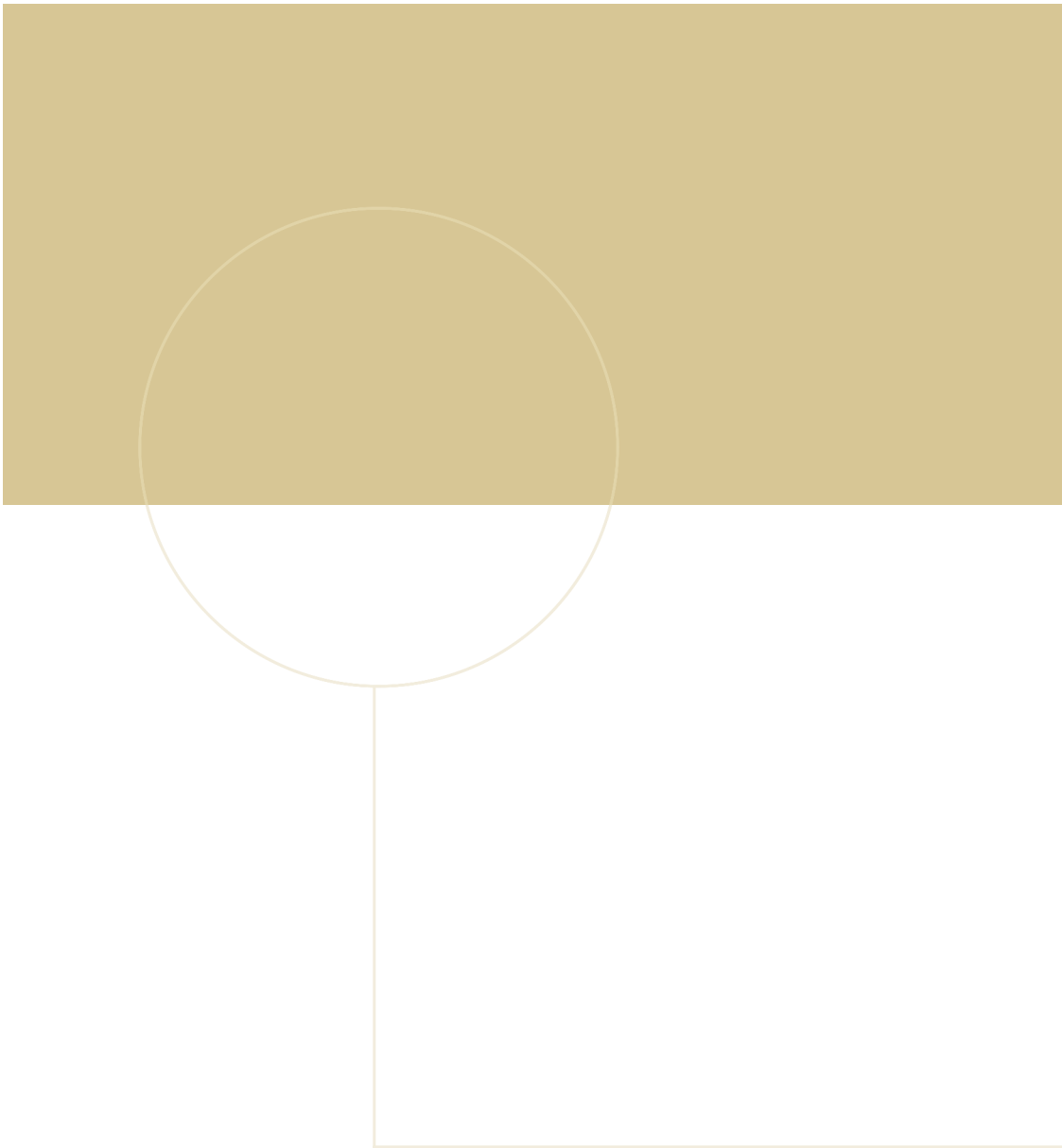

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