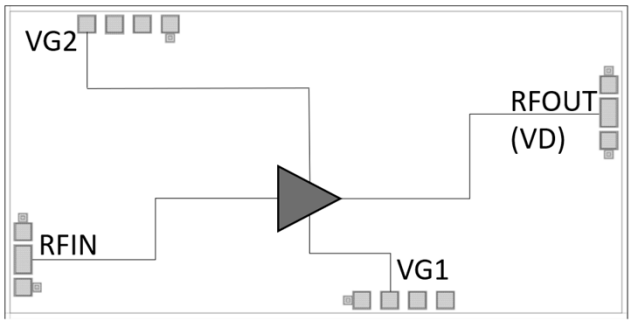
Features

- Frequency: DC - 40GHz
- Small Signal Gain: 16dB
- Gain Flatness: ≤±1.0dB
- Noise Figure 2-2.5dB typ. 2GHz – 20GHz
- P1dB: > 26dBm, 0.2GHz – 18GHz
- Power Supply: +7V/220mA
- Input/Output: 50Ω
- Die Size: 3.3 x 1.63 x 0.07 mm

Functional Block Diagram



Typical Applications

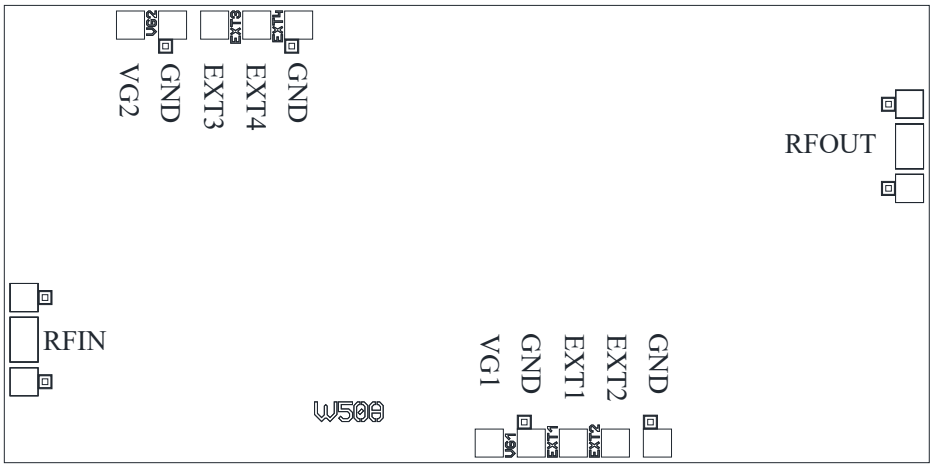
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Electrical Specifications

TA = +25°C, VD = +7V, VG1 = -0.25V, VG2 = 3.0V, ID = 220mA

Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency		0.2-6			6-18			18-40		GHz
Small Signal Gain		15			16			17		dB
Gain Flatness		±1			±1			±1		dB
Noise Figure		2.5		1.5	2.0			4.5		dB
Output 1dB Compression (P1dB)	24	26		22	25		16	21		dBm
Saturated Output Power (Psat)		27.5			26.5			22		dBm
Input Return Loss		> 12			> 13			> 15		dB
Output Return Loss		> 18			> 15			> 10		dB

* Adjust VG1, slightly to obtain device current of 220mA.

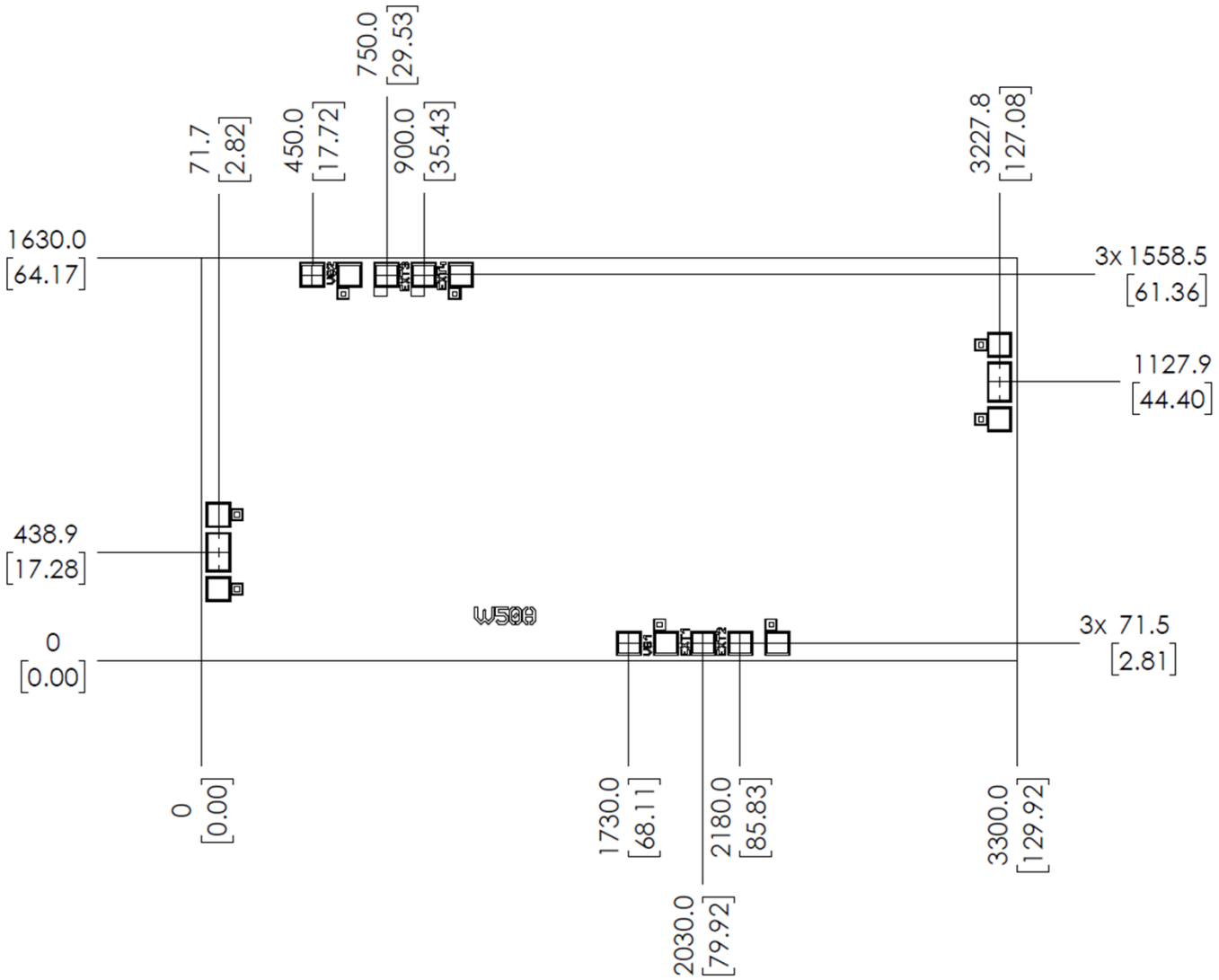


Pad Description

No	Function	Description
1	RF IN	Signal input terminal, connected to 50Ω circuit, DC Blocking capacitor inside.
2	RF OUT	Signal output terminal, connected to 50Ω circuit; blocking capacitor required; external DC biasing network required; drain current provided.
3	VG1	Amplifier 1st gate bias; connect to external 1000pF and 0.01uF bypass capacitors.
4	VG2	Amplifier 2nd gate bias; connect to external 1000pF and 0.01uF bypass capacitors.
5	EXT1	External bypass pad; connect to external 0.47uF bypass capacitor.
6	EXT2	External bypass pad; connect to external 1000pF bypass capacitor.
7	EXT3	External bypass pad; connect to external 1000pF bypass capacitor.
8	EXT4	External bypass pad; connect to external 0.47uF bypass capacitor.
9	GND1	Ground pad.
10	GND2	Ground pad.

Outline Drawing:

All Dimensions in µm [mil]



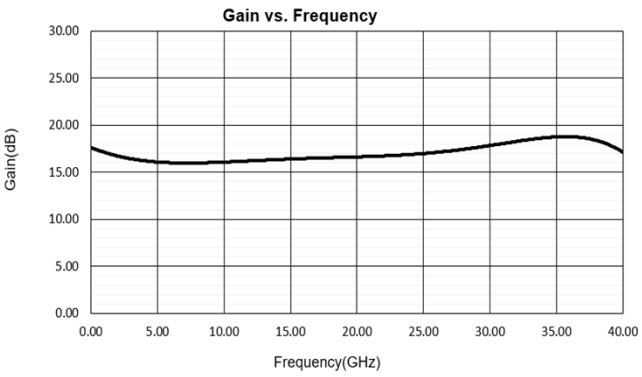
Notes:

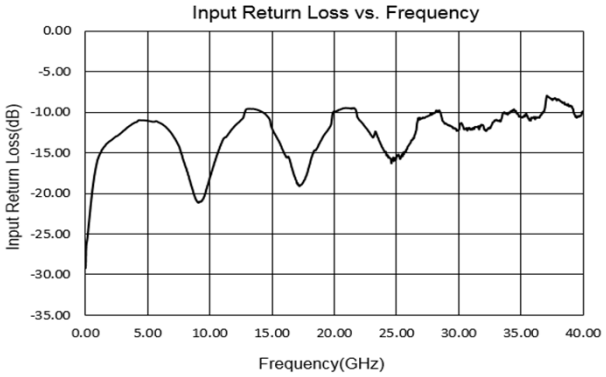
1. Die thickness: 70um
2. DC bond pad is 100 x 100 µm²
3. RF IN/OUT bond pad is 100 x 160 µm²
4. DC bond pad is 100 x 100 µm²
5. No DC Blocking Capacitor needed for RF input
6. External Bias-Tee network needed
7. Bond pad metalization: Gold
8. Backside metalization: Gold
9. Backside of the die (GND)

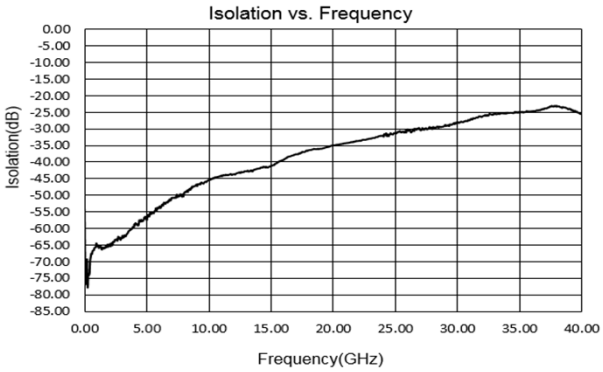
Maximum Ratings:

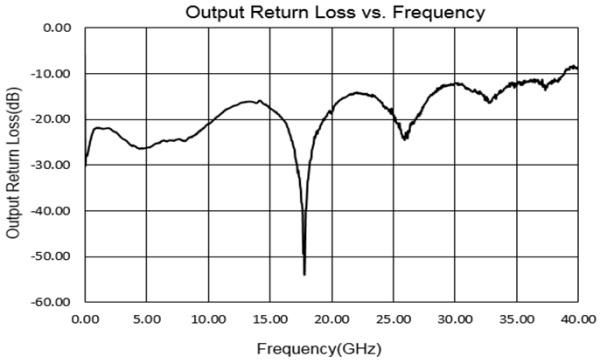
1. Maximum drain voltage: +7.5V
2. Maximum gate bias: -1.5V to -0.1V
3. Maximum input power: +15dBm
4. Operating temperature: -55℃ to +85℃
5. Storage temperature: -65℃ to +150℃

Measurement Plots: S-parameters

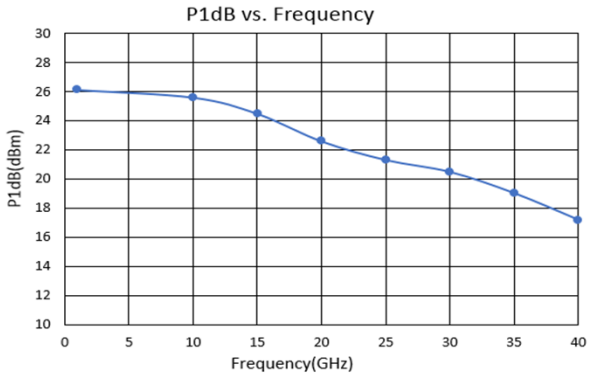




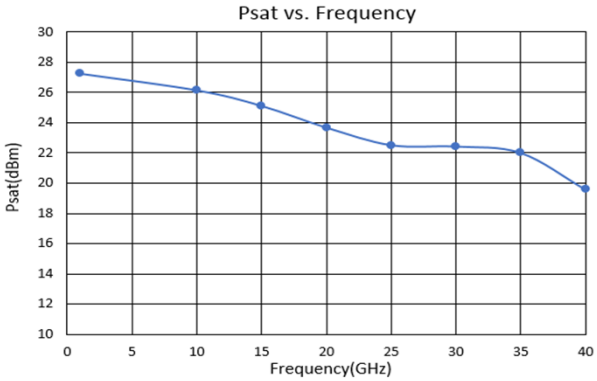




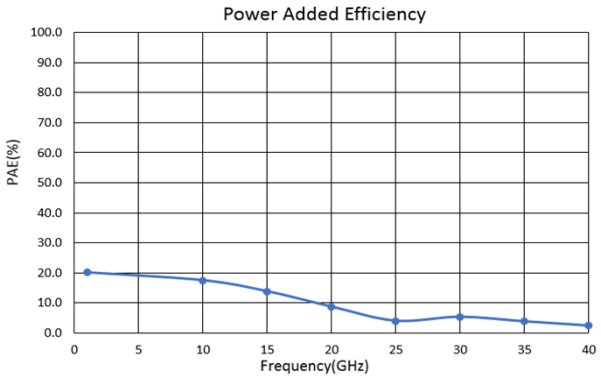
Measurement Plots: P1dB



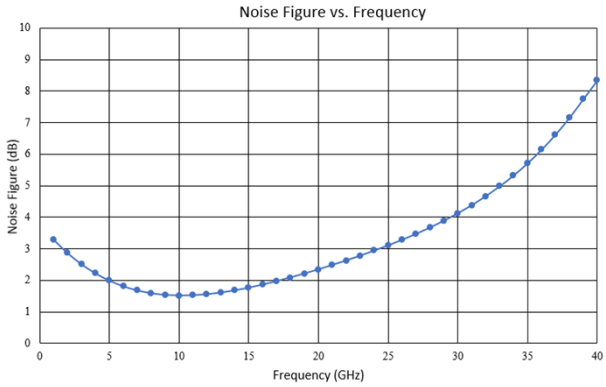
Measurement Plots: Psat



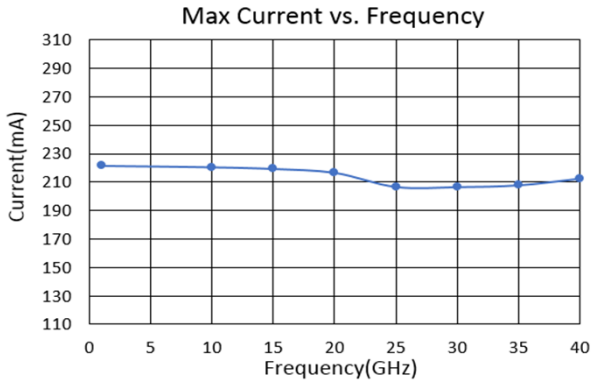
Measurement Plots: Power Added Efficiency



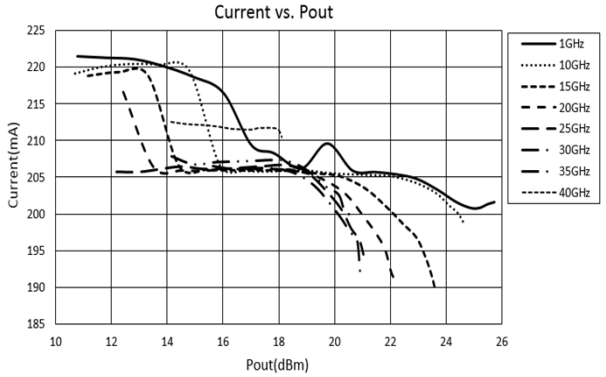
Measurement Plots: Noise Figure



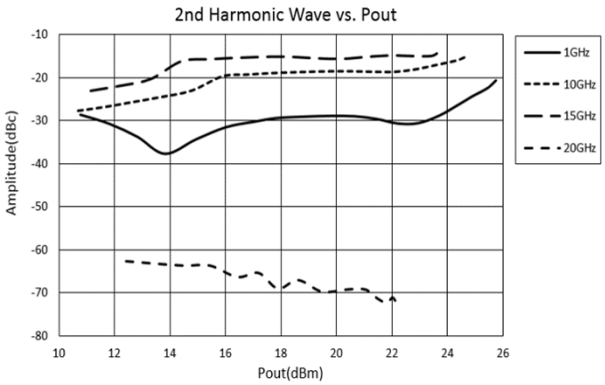
Measurement Plots: Max Current vs. Frequency

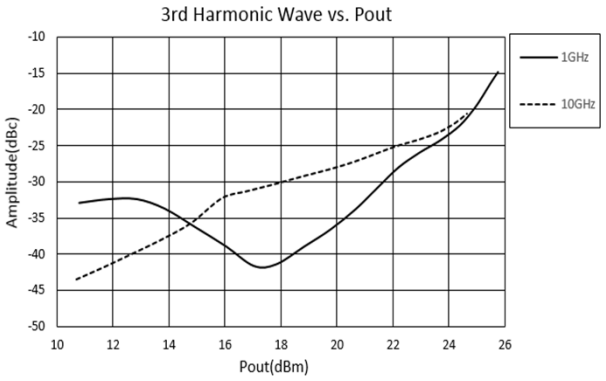


Measurement Plots: Current vs. Pout

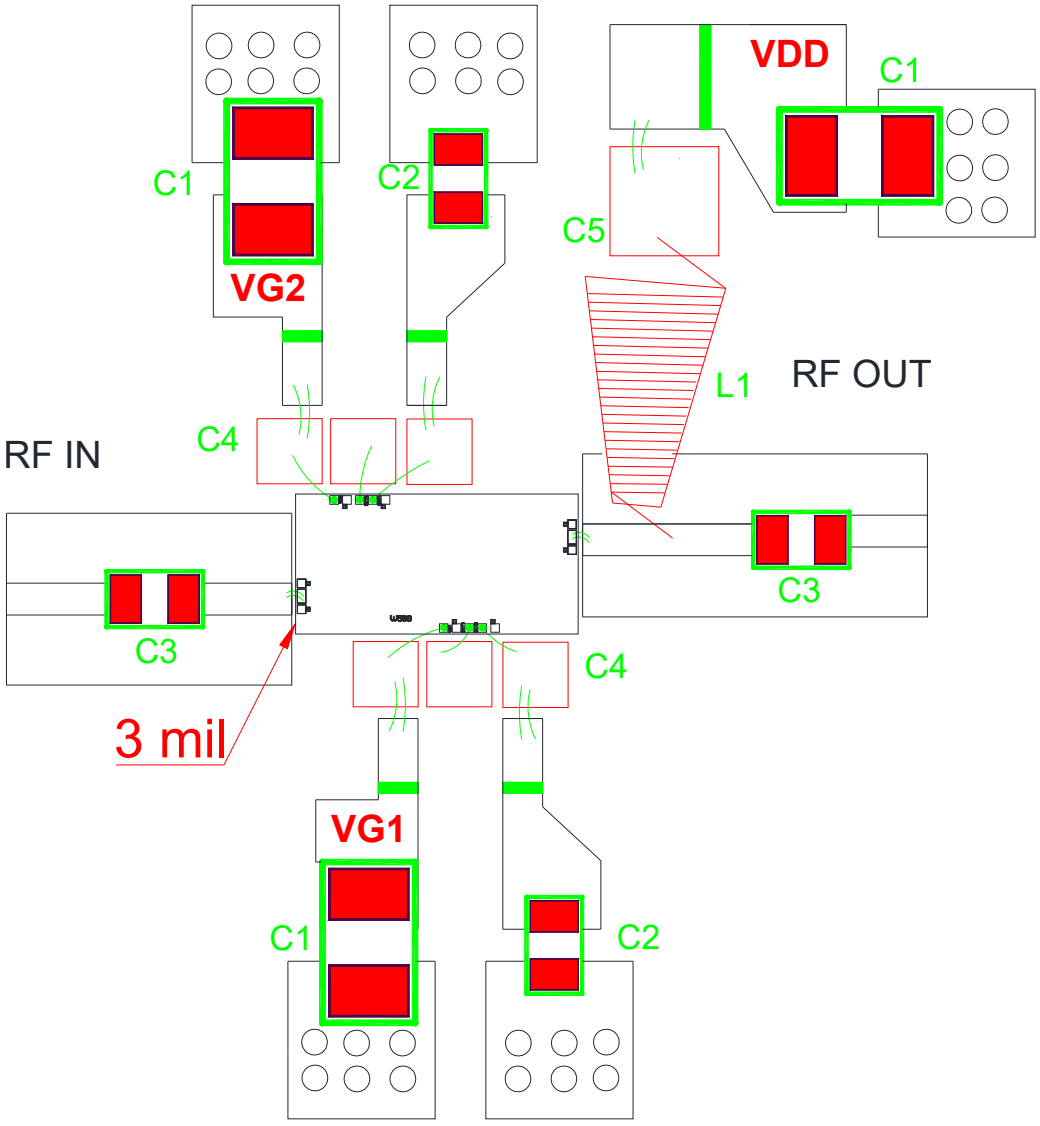


Measurement Plots: Harmonic Wave

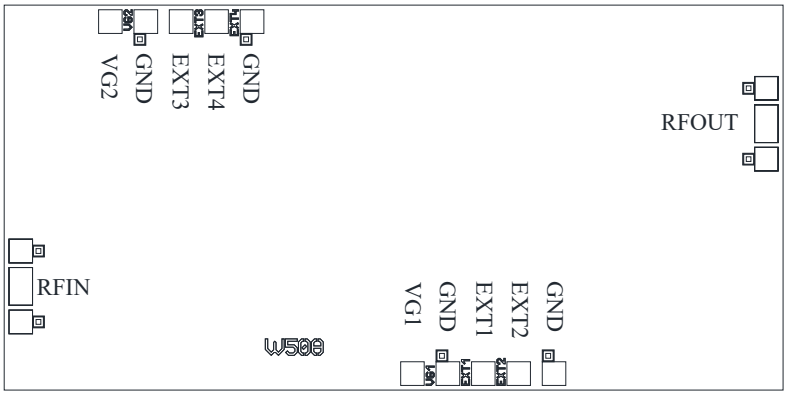




Assembly Drawing



Part	Value	Size	Part Number
C1	10uF	0603	C1608X5R1E106M080AC
C2	0.47uF	0402	C1005X5R0J474K050BB
C3	100pF // 0.01uF	30 * 30 mil	MVB3030X103M2H5C1C
C4	0.1uF	0402	0402BB104KW500
L1	0.425uH	135 mil	CC21T36K240G5



Biasing and Operation

Biasing is done with a positive VDD drain supply, a positive VG2 gate supply, and a negative VG1 gate supply. Performance is optimized when the drain voltage VDD is set to +7 V. The nominal gate voltage VG1 is -0.25V.

Turn ON procedure:

1. Connect Input and Output with 50 Ohm source/load.
2. Apply negative gate voltage VG1 and set to -0.9 V
3. Apply positive voltage VG2 and set to +3.0 V
4. Apply positive drain voltage VDD and set to +7.0 V
5. Increase VG1 (less negative) to achieve a drain current of 220 mA
6. Apply RF signal

Turn OFF procedure:

1. Turn off RF signal
2. Turn off positive drain voltage VDD
3. Turn off positive gate voltage VG2
4. Turn off negative gate voltage VG1