Process Change Notification

(Final-PCN)

- **Customer : All**
- **Subject : 512M DRAM Die Version Change (AS4C32M16MD1A-5BCN)**
- **Date : Mar. 21st 2016**

Alliance Memory Inc. 511 Taylor Way, San Carlos, CA 94070 TEL: (650) 610-6800 FAX: (650) 620-9211
Alliance Memory Inc. reserves the right to change products or specification without notice

1. Notification

This is to inform you that a design and/or process change will be made to the following product(s).
This notification is for your information and concurrence. This is a final PCN for notification.
Qualification is completed and data can meet the requirements

If you require data or samples to qualify this change, please contact Alliance Memory within 30 days of receipt of this notification.

2. Affected Products

AS4C32M16MD1A-5BCN : 512Mb x16bit Mobile DDR SDRAM, FBGA 60B 8 x 9 x 1.0mm

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3. Description of Change

These changes are to improve the performance of the product and keep supporting customer's demand. Alliance Memory decides to implement these changes for better customer support.

Category	Item	From	To
Major	Product Code	AS4C32M16MD1-5BCN	AS4C32M16MD1 A-5BCN
	Datasheet	AS4C32M16MD1-5BCN_rev0.4	AS4C32M16MD1A-5BCN_rev2.0
	Assembly Site	No Change (WINPAC in Korea)	
	Package Type	No Change (60 ball FBGA 8mm x 9mm)	
	Die	ELPIDA 512Mb (40nm tech)	JSC 512Mb (45nm tech)
	Substrate	SU-FBJS-06001W (MTG)	SU-FBJS-06004W (MTG)
	Die Attach Material	No Change	
	Wire	0.7 mil Au (HEESUNG)	0.7 mil AuAg (Heesung/MKE)
	Mold Compound	No Change	
	Solder Ball	No Change	
	Packing	No Change	
	Final Test Site	No Change	

Note : Alliance Memory's DRAM has been qualified by many other customers and it has been using for production in those customers.

4. Evaluation Plan

Item	Product	Requirements	Result
Product Qualification	AS4C32M16MD1 A-5BCN	a. Assembly Process Qualification b. Product Characterization for New DRAM c. Hazardous Substance Data	Qualified

5. Effective Date

Based on Alliance Memory's PCN rule, this change will be implemented for production by Q3 in Y2016.

Evaluation Result

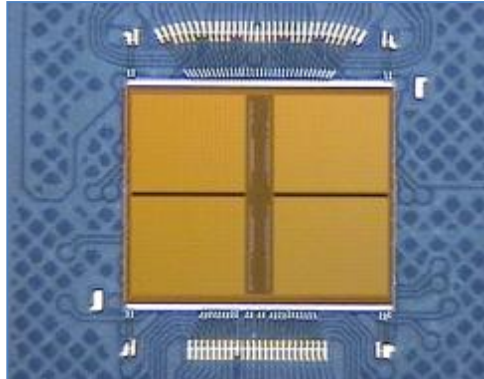
6-1. Assembly : Process Quality Control Data

All test items meet the requirements and shows Cpk > 1.33.

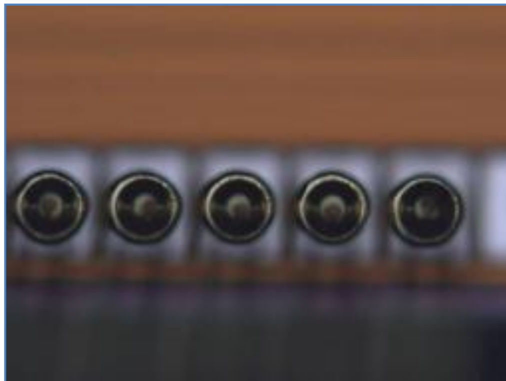
Product Code	Assembly						
	Test Item	Spec	Min	Max	Avg	Cpk	Result
AS4C32M16MD1A-5BCN	Wire Bond Pull	Min 2.0gf	4.09	5.51	4.70	3.04	Pass
	Bonded Ball Shear	Min 3.0gf	17.24	22.70	19.89	4.09	Pass
	Loop Height	Max 150um	96.00	119.00	110.05	2.18	Pass
	Solder Ball Shear	Min 400gf	698.60	886.00	801.67	2.97	Pass
	Solder Ball Pull	Min 400gf	612.99	713.14	657.15	2.87	Pass

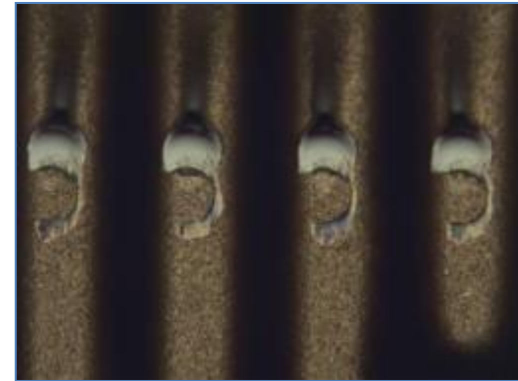
6-2. Assembly : Wire Bonding Image

All bonding results have no issue.



Wire Bonding





Ball

After Ball Shear Test

Stitch

6-3. Assembly : X-ray Image after mold

X-ray and molding results have no issue.

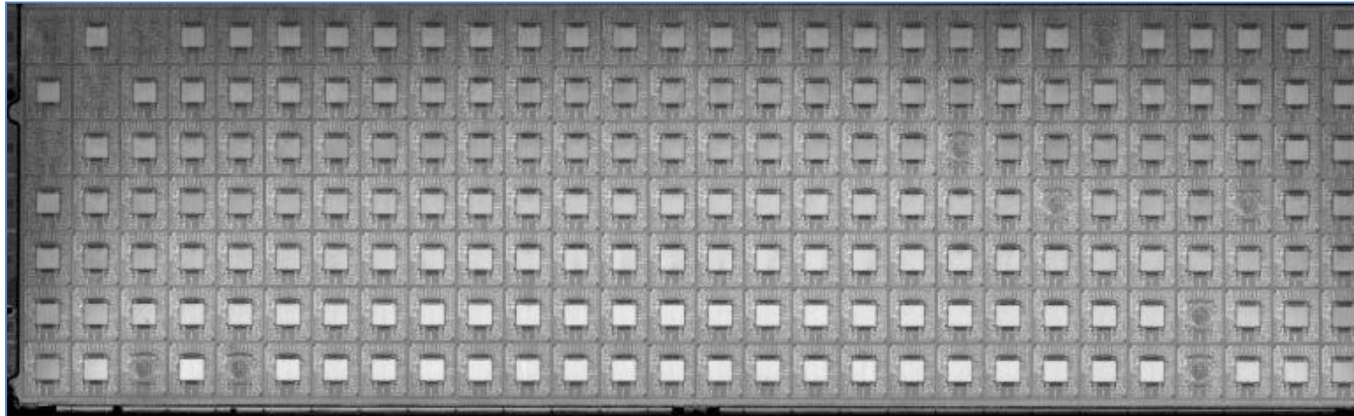
[Wire Sweeping Data]

Unit : %

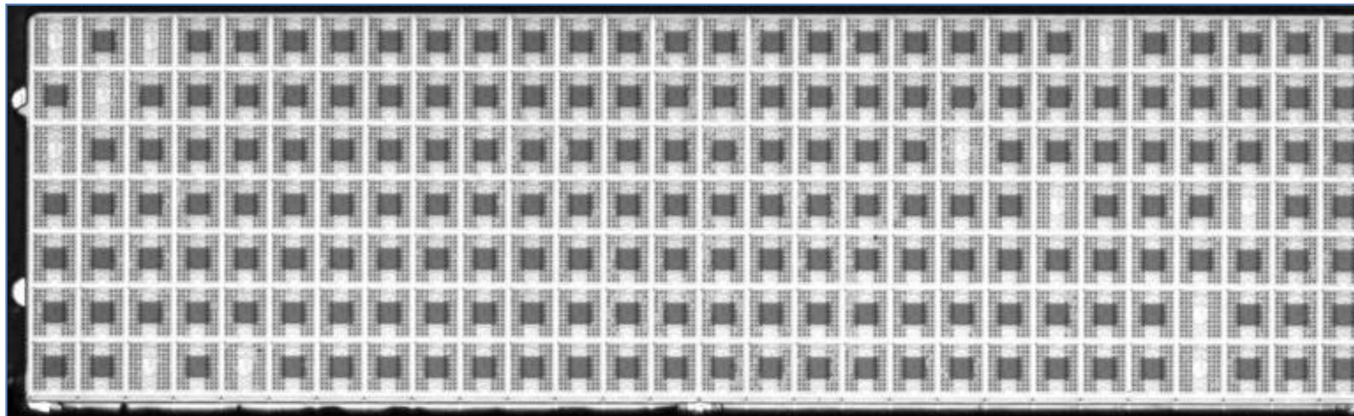
Spec	Min	Max	Avg	Result
Max 35%	2.62	3.51	2.99	Pass

6-4. Assembly : SAT Image after Mold

SAT results have no issue (no delamination).



C-SCAN

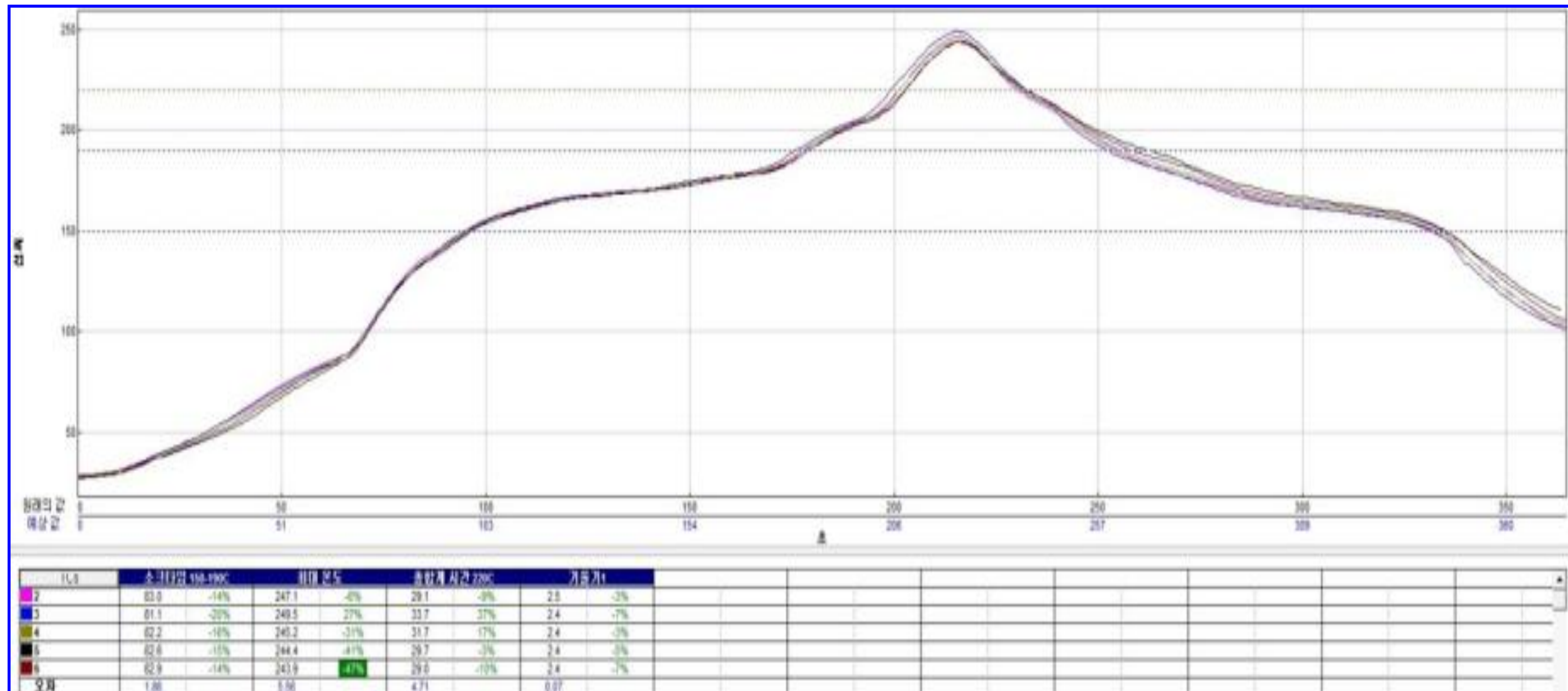


T-SCAN

6-5. Assembly : Reflow Profile for Solder Ball Attach

Below diagram is the reflow profile which is applied for solder ball attach.

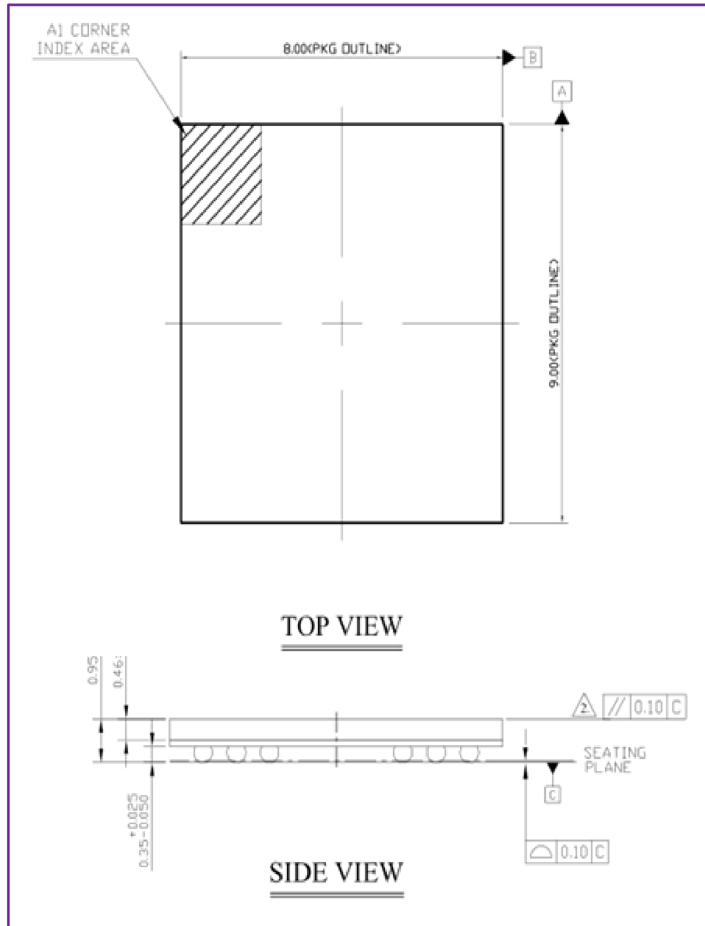
Item	Pre Dwell Time (sec)	Peak Temp. (℃)	Dwell Time (sec)
Parameter	83.0	247.1	29.1



6-6. Assembly : Package Dimension

All dimensions meet the spec.

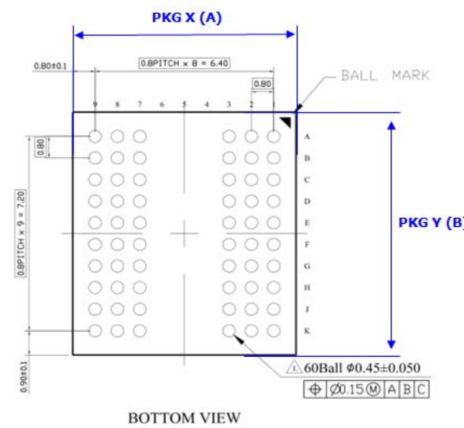
[Package Outline]

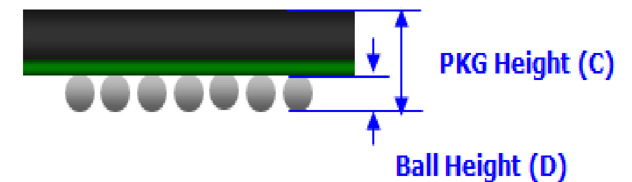


[Measuring Result]

Item	Spec	Min	Max	Avg	Cpk	Result
(A)	8.000 ± 0.10	7.983	8.006	7.996	5.21	Pass
(B)	9.000 ± 0.10	8.984	9.012	8.997	4.50	Pass
(C)	0.950 + 0.05/-0.1	0.904	0.918	0.912	4.80	Pass
(D)	0.350 ± 0.025	0.332	0.345	0.340	1.92	Pass
Coplanarity	Max 0.1	0.017	0.033	0.024	6.24	Pass

Unit : mm

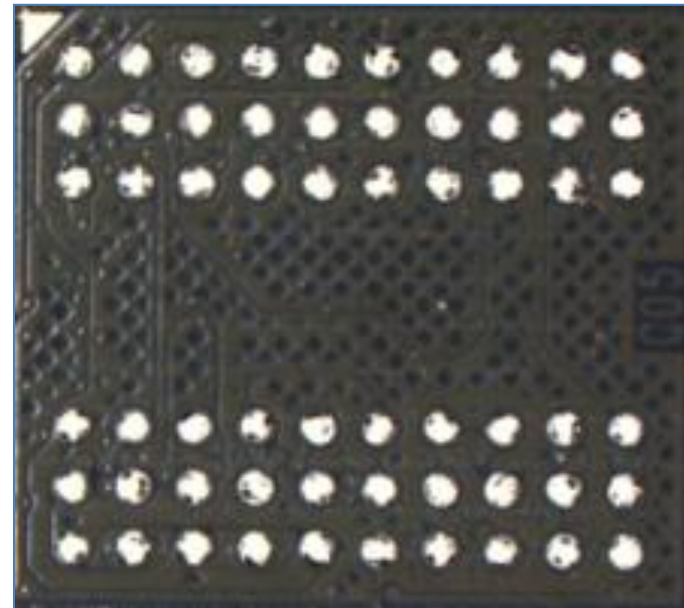




6-7. Assembly : Package Image

[Top View]

[Bottom View]



7-1. Final Test : Characterization Summary (DC Items, 1/2)

Below table shows the result to check parameters and there are enough margin.

Item	Description	Spec		Unit	Worst Case	Spec. Margin		Temp	VDD
		Min	Max			Value	Percent		
IDD0	Active-Precharge Current (One Bank)	-	40.00	mA	25.50	14.50	36.3%	Cold(-30℃)	2.00V
IDD2P	Precharge Standby Current (PDN)	-	0.30	mA	0.13	0.20	56.5%	Hot(87℃)	1.70V
IDD2PS	Precharge Standby Current (PDN CLK_L)	-	0.30	mA	0.13	0.20	56.5%	Hot(87℃)	1.70V
IDD2N	Precharge Standby Current (Non-PDN)	-	10.00	mA	5.60	4.40	44.0%	Cold(-30℃)	2.00V
IDD2NS	Precharge Standby Current (Non-PDN CLK_L)	-	3.00	mA	2.26	0.70	24.7%	Cold(-30℃)	2.00V
IDD3P	Active Standby Current (PDN)	-	3.00	mA	0.26	2.70	91.3%	Hot(87℃)	1.80V
IDD3PS	Active Standby Current (PDN CLK_L)	-	3.00	mA	0.26	2.70	91.3%	Hot(87℃)	1.80V
IDD3N	Active Standby Current (Non-PDN)	-	25.00	mA	10.00	15.00	59.9%	Cold(-30℃)	2.00V
IDD3NS	Active Standby Current (Non-PDN CLK_L)	-	15.00	mA	3.70	11.30	75.1%	Cold(-30℃)	2.00V
IDD4R	Read Burst Operating Current	-	85.00	mA	50.00	35.00	41.2%	Cold(-30℃)	2.00V
IDD4W	Write Burst Operating Current	-	65.00	mA	42.00	23.00	35.4%	Cold(-30℃)	2.00V

7-1. Final Test : Characterization Summary (DC Items, 2/2)

Below table shows the result to check parameters and there are enough margin.

Item	Description	Spec		Unit	Worst Case	Spec. Margin		Temp	VDD
		Min	Max			Value	Percent		
IDD5	Auto-Refresh Current	-	75.00	mA	53.00	22.00	29.3%	Cold(-30℃)	1.80V
IDD6 FULL	(Full Array) Self-Refresh Current	-	500.00	uA	394.00	106.00	21.2%	Hot(87℃)	1.70V
IDD6 1/2	(Half Array) Self-Refresh Current	-	450.00	uA	272.00	178.00	39.5%	Hot(87℃)	1.70V
IDD6 1/4	(Quarter Array) Self-Refresh Current	-	400.00	uA	209.00	191.00	47.8%	Hot(87℃)	1.70V
IDD8	Deep Power-Down Current	-	10.00	uA	1.86	8.14	81.4%	Hot(87℃)	2.00V
VIH_Max	Input High Voltage	-	VDDQ+0.3	V	2.50	0.25	11.1%	Hot(87℃)	1.95V
VIL_Min	Input Low Voltage	-0.30	-	V	-1.00	0.20	53.3%	Cold(-30℃)	1.70V
VIH_Min	Input High Voltage	VCCQ*0.8	-	V	1.10	0.38	24.4%	Hot(87℃)	1.95V
VIL_Max	Input Low Voltage	-	VCCQ*0.2	V	0.68	0.24	66.7%	Hot(87℃)	1.80V
VID	Input Differential Voltage	VDDQ*0.6	-	V	0.80	0.40	31.6%	Cold(-30℃)	1.95V
VOH	DC Output Hogh Voltage (Ioh=-100uA)	VDDQ*0.9	-	V	1.70	0.20	9.8%	Hot(87℃)	1.70V
VOL	DC Output Low Voltage (Iol=100uA)	-	VDDQ*0.1	V	0.00	0.20	94.1%	Hot(87℃)	1.70V

7-2. Final Test : Characterization Summary (AC Items, 1/4)

Below table shows the result to check parameters and there are enough margin.

Item	Description	Spec		Unit	Worst Case	Spec. Margin		Temp	VDD
		Min	Max			Value	Percent		
tAC (MAX)	DQ Output Access Time From CK	-	5.00	ns	4.55	0.45	9.0%	Hot(87℃)	1.70V
tAC (MIN)	DQ Output Access Time From CK	2.00	-	ns	2.95	0.95	47.5%	Hot(87℃)	1.95V
tDQSCK	DQS Output access time From CK	-	5.00	ns	4.50	0.50	10.0%	Hot(87℃)	1.70V
tCH (Min)	Clock High-Level Width	2.25	-	ns	1.35	0.65	28.9%	Cold(-30℃)	1.95V
tCH (MAX)	Clock High-Level Width	-	2.75	ns	3.50	0.45	16.4%	Hot(87℃)	1.70V
tCL (Min)	Clock Low-Level Width	2.25	-	ns	1.50	0.45	20.0%	Hot(87℃)	1.70V
tCL (MAX)	Clock Low-Level Width	-	2.75	ns	3.65	0.65	23.6%	Cold(-30℃)	1.95V
tCK	Clock Cycle Time	-	5.00	ns	4.20	0.80	16.0%	Hot(87℃)	1.95V
tDS	DQ Input Setup Time	0.58	-	ns	0.36	0.12	20.7%	Hot(87℃)	1.70V
tDH	DQ Input Hold Time	0.58	-	ns	0.40	0.14	24.1%	Hot(87℃)	1.95V
tDIPW	DQ Input Pulse Width	1.60	-	ns	1.40	0.20	12.5%	Hot(87℃)	1.95V

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7-2. Final Test : Characterization Summary (AC Items, 2/4)

Below table shows the result to check parameters and there are enough margin.

Item	Description	Spec		Unit	Worst Case	Spec. Margin		Temp	VDD
		Min	Max			Value	Percent		
tIS	Input Setup Time	0.90	-	ns	0.30	0.50	55.6%	Hot(87℃)	1.95V
tIH	Input Hold Time	0.90	-	ns	0.20	0.60	66.7%	Hot(87℃)	1.95V
tIPW	Input Pulse Width	2.30	-	ns	1.20	1.00	43.5%	Hot(87℃)	1.95V
tLZ	DQ Low-Impedance Time From CK	1.00	-	ns	3.90	2.10	210.0%	Cold(-30℃)	1.80V
tHZ	DQ High-Impedance Time From CK	-	5.00	ns	3.20	1.10	22.0%	Hot(87℃)	1.95V
tDQSS (MIN)	Write Command To 1st DQS Latching Transition	3.75	-	ns	0.00	1.25	33.3%	Hot(87℃)	1.95V
tDQSS (MAX)	Write Command To 1st DQS Latching Transition	-	6.25	ns	7.50	0.75	12.0%	Hot(87℃)	1.95V
tDQSH (MIN)	DQS Input High-Level Width	2.00	-	ns	1.50	0.50	25.0%	Hot(87℃)	1.95V
tDQSH (MAX)	DQS Input High-Level Width	-	3.00	ns	3.80	0.70	23.3%	Hot(87℃)	1.95V
tDQSL (Min)	DQS Input Low-Level Width	2.00	-	ns	1.70	0.20	10.0%	Cold(-30℃)	1.95V
tDQSL (MAX)	DQS Input Low-Level Width	-	3.00	ns	3.50	0.30	10.0%	Hot(87℃)	1.95V

7-2. Final Test : Characterization Summary (AC Items, 3/4)

Below table shows the result to check parameters and there are enough margin.

Item	Description	Spec		Unit	Worst Case	Spec. Margin		Temp	VDD
		Min	Max			Value	Percent		
tDSS	DQS Falling Edge To CK Setup Time	1.00	-	ns	0.00	0.50	50.0%	Hot(87℃)	1.95V
tDSH	DQS Falling Edge Hold Time From CK	1.00	-	ns	0.00	0.40	40.0%	Hot(87℃)	1.95V
tMRD	Mode Register Set Command Period	10.00	-	ns	8.00	2.00	20.0%	Hot(87℃)	1.95V
tWPST (MIN)	Write Postamble	2.00	-	ns	0.60	1.20	60.0%	Hot(87℃)	1.95V
tWPST (MAX)	Write Postamble	-	3.00	ns	4.00	1.00	33.3%	Hot(87℃)	1.95V
tWPRE	Write Preamble	1.25	-	ns	0.90	0.25	20.0%	Hot(87℃)	1.95V
tRPRE	Read Preamble	4.50	5.50	ns	4.80	0.30	5.5%	Hot(87℃)	1.70V
tRPST	Read Postamble	2.00	3.00	ns	2.10	0.40	13.3%	Hot(87℃)	1.95V
tRAS (MIN)	Active To Precharge Command Period	40.00	-	ns	15.00	25.00	62.5%	Hot(87℃)	1.95V
tRC	Active To Active Command Period	55.00	-	ns	24.00	27.40	49.8%	Room(25℃)	1.80V
tRFC	Auto Refresh To Active/Auto Refresh Command Period	72.00	-	ns	40.80	28.80	40.0%	Hot(87℃)	1.80V

7-2. Final Test : Characterization Summary (AC Items, 4/4)

Below table shows the result to check parameters and there are enough margin.

Item	Description	Spec		Unit	Worst Case	Spec. Margin		Temp	VDD
		Min	Max			Value	Percent		
tRCD	Active To Read Or Write Delay	15.00	-	ns	12.00	3.00	20.0%	Hot(87℃)	1.95V
tRP	Precharge Command Period	3*tCK	-	ns	5.60	8.20	54.7%	Hot(87℃)	1.95V
tRRD	Active Bank A To Active Bank B Delay	10.00	-	ns	5.60	4.00	40.0%	Hot(87℃)	1.95V
tWR	Write Recovery Time	15.00	-	ns	4.00	9.20	61.3%	Hot(87℃)	1.70V
tDAL	Auto Precharge Write Recovery + Precharge Time	6*tCK	-	ns	17.20	11.60	38.7%	Hot(87℃)	1.95V
tWTR	Internal Write To Read Command Delay	2*tCK	-	ns	5.80	4.20	42.0%	Hot(87℃)	1.95V
tXSR	Self Refresh Exit To Next Valid Command Delay	120.00	-	ns	38.00	80.00	66.7%	Hot(87℃)	1.95V
tXP	Exit Power Down To Next Valid Command Delay	2*tCK	-	ns	3.60	6.00	60.0%	Hot(87℃)	1.95V
tCKE	CKE Minimum Pulse Width (High And Low Pulse Width)	1*tCK	-	ns	4.70	0.30	6.0%	Hot(87℃)	1.95V
tREF	Refresh Period	64.00	-	ms	160.00	96.00	150.0%	Hot(87℃)	1.95V
tREFI	Average Periodic Refresh Interval	7.80	-	us	20.00	12.20	156.4%	Hot(87℃)	1.95V

8. RoHS Compliance (1/2)

All BOMs are compliant with the requirements of the European Union's Restriction on Use of Hazardous Substances("RoHS") and Halogen directive.

[Alliance Memory's ROHS & Halogen Free permissible limit]

Unit : PPM

Division	Cd	Pb	Hg	Cr6+	PBBs	PBDEs	Br	Cl	Sb
Organic	5	100	800	800	900	900	900	900	700
Inorganic	80	800	800	800	-	-	-	-	700

Organic : Substrate, WBL tape, Mold compound etc…

Inorganic : Wafer, Gold wire, Solder ball etc…

8. RoHS Compliance (2/2)

All BOMs are compliant with the requirements of the European Union's Restriction on Use of Hazardous Substances("RoHS") and Halogen directive.

Alliance Memory's ROHS & Halogen Free permissible limit]

Unit : PPM

Product Code	Assembly								
	Item	Vendor	Type	Cd	Pb	Cr6+	Hg	PBB	PBDE
AS4C32M16MD1A-5BC N	Silicon	ALLIANCE	512M LPDDR	ND	ND	ND	ND	ND	ND
	Substrate	MTG	SU-FBJS-06004W	ND	Cu : 5	ND	ND	ND	ND
	Epoxy	KCC	WA-330H-20T	ND	ND	ND	ND	ND	ND
	Wire	Heesung	AuAg wire	ND	ND	Negative	ND	ND	ND
		MKE	AuAg wire	ND	ND	Negative	ND	ND	ND
	Mold Compound	KCC	KTMC5900GL	ND	ND	ND	ND	ND	ND
	Solder Ball	Duksan	SAC 305	ND	142	Negative	ND	ND	ND
		MKE	SAC 305	ND	40.3	Negative	ND	ND	ND

Note : ND (Not Detected), Negative (Undetectable).