AU5424A1: HIGH PERFORMANCE 1:4 LVCMOS CLOCK BUFFER

General Description

The AU5424A1 is a high-performance LVCMOS clock buffer family of devices. It has an additive phase jitter of 50 fs RMS.

The AU5424A1 supports a synchronous glitch-free output enable (OE) function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It can operate from a 1.8 V to 3.3 V supply.

The AU5424A1 is available in an Automotive Grade 1, AEC-Q100 qualified version

Typical Applications:

- Automotive Applications

Features

- High-performance 1:4 Buffer
- LVCMOS clock buffer
- Very low pin-to-pin skew: <50 ps
- Very low additive jitter: <50 fs
- Supply voltage: 1.8 V to 3.3 V
- 3.3V tolerant input clock
- F_{MAX} = 200 MHz
- Integrated serial termination for 50 Ω channel
- Packaged in 8pin, 2 × 2 mm DFN packages
- AEC-Q100 qualified
- Automotive Grade 1 (-40 °C to +125 °C)

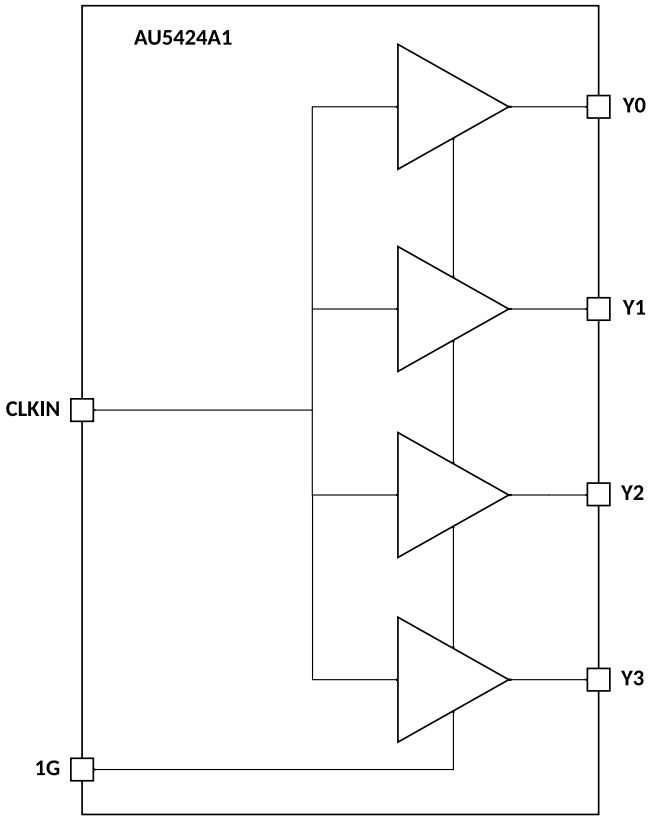

Figure 1 Functional Overview

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1 Pin Description

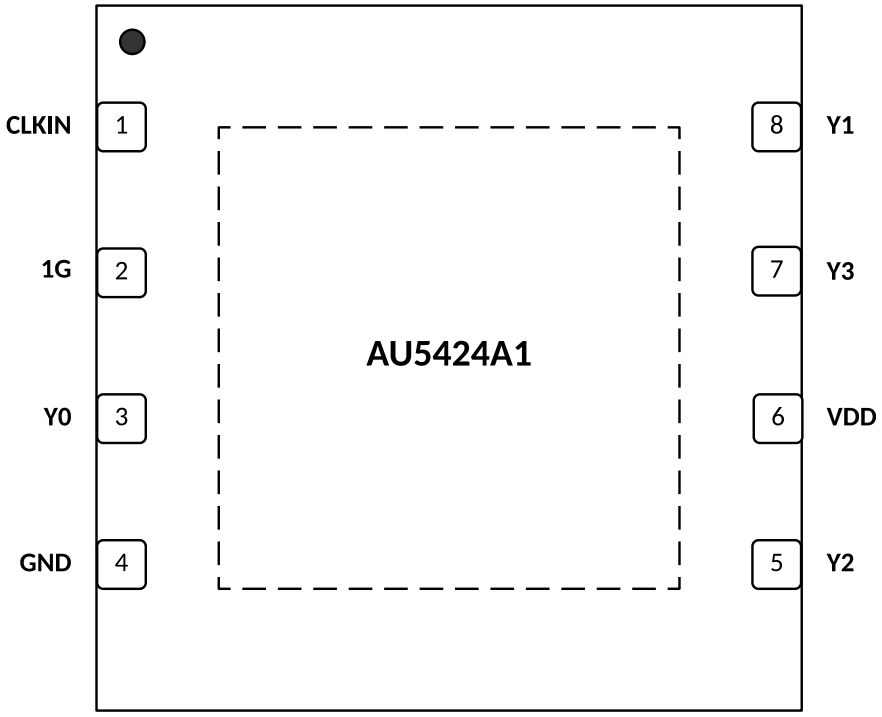

Figure 2 AU5424A1 Pin Configuration

Table 1 Detailed Pin Description

Pin Name	Pin Number	Functionality AU5424A1
Y0	3	LVCMOS output 0
Y1	8	LVCMOS output 1
Y2	5	LVCMOS output 2
Y3	7	LVCMOS output 3
CLKIN	1	Single Ended Input Clock
1G	2	All outputs enable/disable
VDD	6	Core Supply Voltage, VDD
GND	4	Ground

2 Functional Description

2.1Output Logic Tables

Table 2 Output Logic Tables

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

3 Typical Application Diagram

The following are the typical application diagram for Automotive applications .

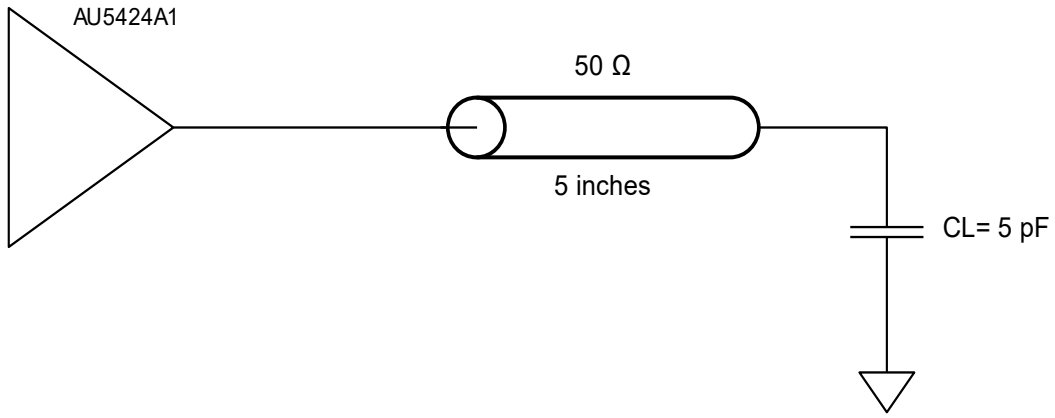

Figure 3 AU5424A1 Typical Application Load

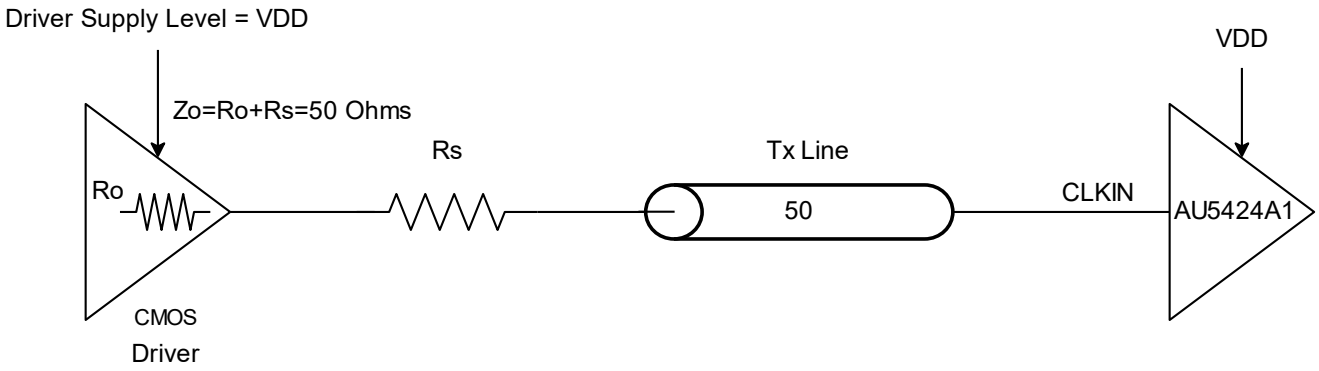

Figure 4 Recommended input clock configuration

4 Input Clock and Power Supply Sequencing

The input clock to the AU5424 buffer should come after the power supply ramp. Figure 5 shows the timing requirement of Input Clock start versus VDD ramp. However, for the supply rail of VDD = 1.8 V (±5%), the above timing requirement is not mandatory.

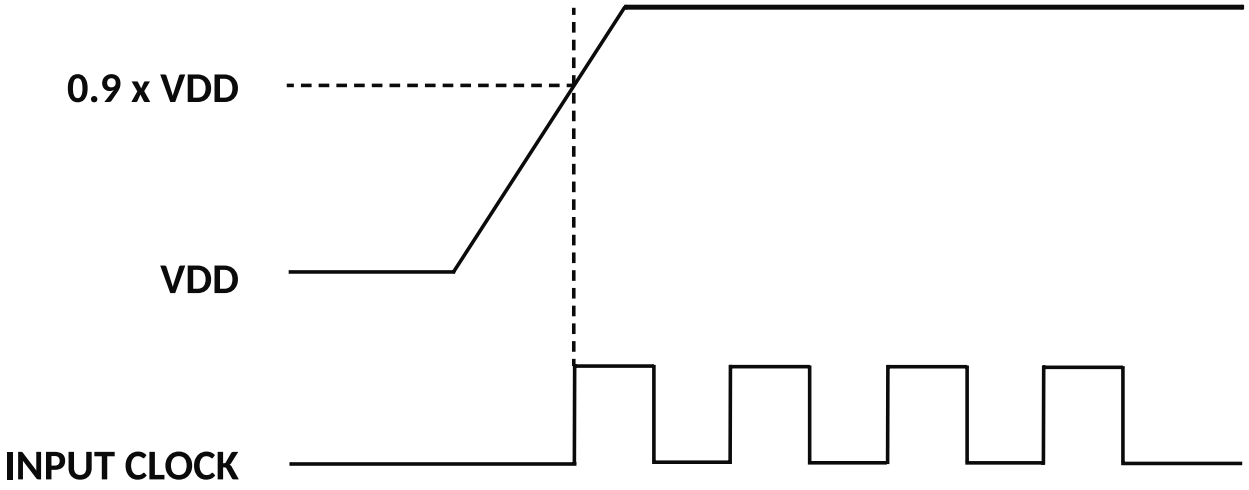

Figure 5 Input clock to VDD ramp timing requirement for AU5424A1

5 Electrical Specifications

Table 3 Absolute Maximum Ratings

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Supply Voltage, VDD					3.6	V
Output Enable and All Outputs			-0.4		VDD+0.3	V
Input voltage, CLKIN			-0.4		3.465	V
Ambient Operating Temperature, Automotive grade 1			-40		+125	°C
Storage Temperature			-65		+150	°C
Junction Temperature					+150	°C
Soldering Temperature					+260	°C
Moisture Sensitivity Level	8-DFN	MSL	3			

Notes:

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 4 Recommended Operating Supply and Temperature

Parameter	Symbol	Min	Typ	Max	Units
Ambient Operating Temperature (Automotive Grade 1)		-40		+125	°C
Power Supply Voltage (Measured in respect to GND)		+1.71		+3.465	V

Table 5 DC Electrical Characteristics V_{DD} = 1.8 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V_{DD}	1.71	1.8	1.89	V
Input High Voltage, CLKIN[1]		V_{IH}	0.7×V_{DD}			V
Input Low Voltage, CLKIN[1]		V_{IL}			0.3×V_{DD}	V
Input High Voltage, 1G		V_{IH}	1.6		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.6	V
Output High Voltage	I_{OH} = -5 mA.	V_{OH}	1.2			V
Output Low Voltage	I_{OL} = 5 mA.	V_{OL}			0.45	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin.	C_{IN}		5		pF
Operating Supply Current[2]	0.001 MHz, C_L = 5 pF.	I_{DD}		0.7	1.7	mA
	0.008 MHz, C_L = 5 pF.			0.7	1.7	
	40 MHz, C_L = 5 pF.			11	13	
	100 MHz, C_L = 5 pF.			25	30	
	156.25 MHz, C_L = 5 pF.			37	47	
	200 MHz, C_L = 5 pF.			39	57	

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +125 °C unless stated otherwise.

Table 6 DC Electrical Characteristics V_{DD} = 2.5 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V_{DD}	2.375	2.5	2.625	V
Input High Voltage, CLKIN[1]		V_{IH}	0.7×V_{DD}			V
Input Low Voltage, CLKIN[1]		V_{IL}			0.3×V_{DD}	V
Input High Voltage, 1G		V_{IH}	1.8		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.7	V
Output High Voltage	I_{OH} = -8 mA.	V_{OH}	1.6			V
Output Low Voltage	I_{OL} = 8 mA.	V_{OL}			0.625	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin.	C_{IN}		5		pF
Operating Supply Current[2]	0.001 MHz, C_L = 5 pF.	I_{DD}		0.9	2.0	mA
	0.008 MHz, C_L = 5 pF.			0.9	2.0	
	40 MHz, C_L = 5 pF.			15	17.2	
	100 MHz, C_L = 5 pF.			35	42	
	156.25 MHz, C_L = 5 pF.			52	67	
	200 MHz, C_L = 5 pF.			56	80	

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +125 °C unless stated otherwise.

Table 7 DC Electrical Characteristics - V_{DD} = 3.3 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Voltage		V_{DD}	3.135	3.3	3.465	V
Input High Voltage, CLKIN[1]		V_{IH}	0.7×V_{DD}			V
Input Low Voltage, CLKIN[1]		V_{IL}			0.3×V_{DD}	V
Input High Voltage, 1G		V_{IH}	2.1		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.8	V
Output High Voltage	I_{OH} = -12 mA.	V_{OH}	2.1			V
Output Low Voltage	I_{OL} = 12 mA.	V_{OL}			0.825	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin.	C_{IN}		5		pF
Operating Supply Current[2]	0.001 MHz, C_L = 5 pF.	I_{DD}		1.2	2.2	mA
	0.008 MHz, C_L = 5 pF.			1.2	2.2	
	40 MHz, C_L = 5 pF.			19	23.3	
Operating Supply Current[2]	100 MHz, C_L = 5pF.	I_{DD}		45	54	
	156.25 MHz, C_L = 5pF.			67	87	
	200 MHz, C_L = 5pF.			75	107	

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +125 °C unless stated otherwise.

Table 8 AC Electrical Characteristics - V_{DD} = 1.8 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Input Slew rate			2			V/ns
Output Rise Time (5 pF load)[2]	0.36 V to 1.44 V, C_L = 5 pF.	t_{OR}		0.65	1.2	ns
Output Fall Time (5 pF load)[2]	1.44 V to 0.36 V, C_L = 5 pF.	t_{OF}		0.65	1.2	ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up.	$t_{START-UP}$			3	ms
Propagation Delay[3]		t_{PD}	0.24		3.4	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t_{JIT}			0.06	ps
Output to Output Skew	Rising edges at VDD/2.[1]	t_{SK}		35	77	ps
Device to Device Skew	Rising edges at VDD/2.				200	ps
Output Enable Time	C_L ≤ 5 pF Frequency = 25Mhz	t_{EN}			3	cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{EN}			5	cycles
Output Disable Time	C_L ≤ 5 pF. Frequency = 25Mhz	t_{DIS}			3	cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{DIS}			5	cycles
Duty Cycle		t_{DC}		50		%

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +125 °C unless stated otherwise.
3. With rail to rail input clock

Table 9 AC Electrical Characteristics - V_{DD} = 2.5 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Input Slew rate			2			V/ns
Output Rise Time (5 pF load)[2]	0.5 V to 2.0 V, C_L = 5 pF.	t_{OR}		0.63	1.2	ns
Output Fall Time (5 pF load)[2]	2.0 V to 0.5 V, C_L = 5 pF.	t_{OF}		0.63	1.2	ns
Start-up Time	Part start-up time for valid outputs after V_{DD} ramp-up.	$t_{START-UP}$			3	ms
Propagation Delay[3]		t_{PD}	0.24		3.4	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t_{JIT}			0.06	ps
Output to Output Skew	Rising edges at V_{DD}/2[1]	t_{SK}		35	77	ps
Device to Device Skew	Rising edges at V_{DD}/2	t_{SKD}			200	ps
Output Enable Time	C_L ≤ 5 pF Frequency = 25Mhz	t_{EN}			3	cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{EN}			5	cycles

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Output Disable Time	$C_L \leq 5$ pF. Frequency = 25Mhz	t_{DIS}			3	cycles
	$C_L \leq 5$ pF Frequency = 200Mhz	t_{DIS}			5	cycles
Duty Cycle		t_{DS}		50		%

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +125 °C unless stated otherwise.
3. With rail to rail input clock

Table 10 AC Electrical Characteristics - V_{DD} = 3.3 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Input Slew rate			2			V/ns
Output Rise Time (5 pF load)[2]	0.66 V to 2.64 V, CL = 5 pF.	t_{OR}		0.61	1.2	ns
Output Fall Time (5 pF load)[2]	2.64 V to 0.66 V, CL = 5 pF.	t_{OF}		0.61	1.2	ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up.	$t_{START-UP}$			3	ms
Propagation Delay[3]		t_{PD}	0.24		3.4	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t_{JIT}			0.05	ps
Output to Output Skew	Rising edges at VDD/2[1]	t_{SK}		35	77	ps
Device to Device Skew	Rising edges at VDD/2.	t_{SKD}			200	ps
Output Enable Time	$C_L \leq 5$ pF Frequency = 25Mhz	t_{EN}			3	cycles
	$C_L \leq 5$ pF Frequency = 200Mhz	t_{EN}			5	cycles
Output Disable Time	$C_L \leq 5$ pF. Frequency = 25Mhz	t_{DIS}			3	cycles
	$C_L \leq 5$ pF Frequency = 200Mhz	t_{DIS}			5	cycles
Duty Cycle		t_{DC}		50		%

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +125 °C unless stated otherwise.
3. With rail to rail input clock

Table 11 ESD Ratings

Parameter	Conditions	Symbol	Min	Typ	Max	Units
ESD (Human Body Model)	AEC-Q100-002	ESD_{HBM}	-	2000	-	V
ESD(Charged Device Model)	AEC-Q100-011	ESD_{CDM}	-	500	-	V

Table 12 Thermal Characteristics

Package	ΘJA	Units
8-DFN	75	°C/W; still air

6 Package Information

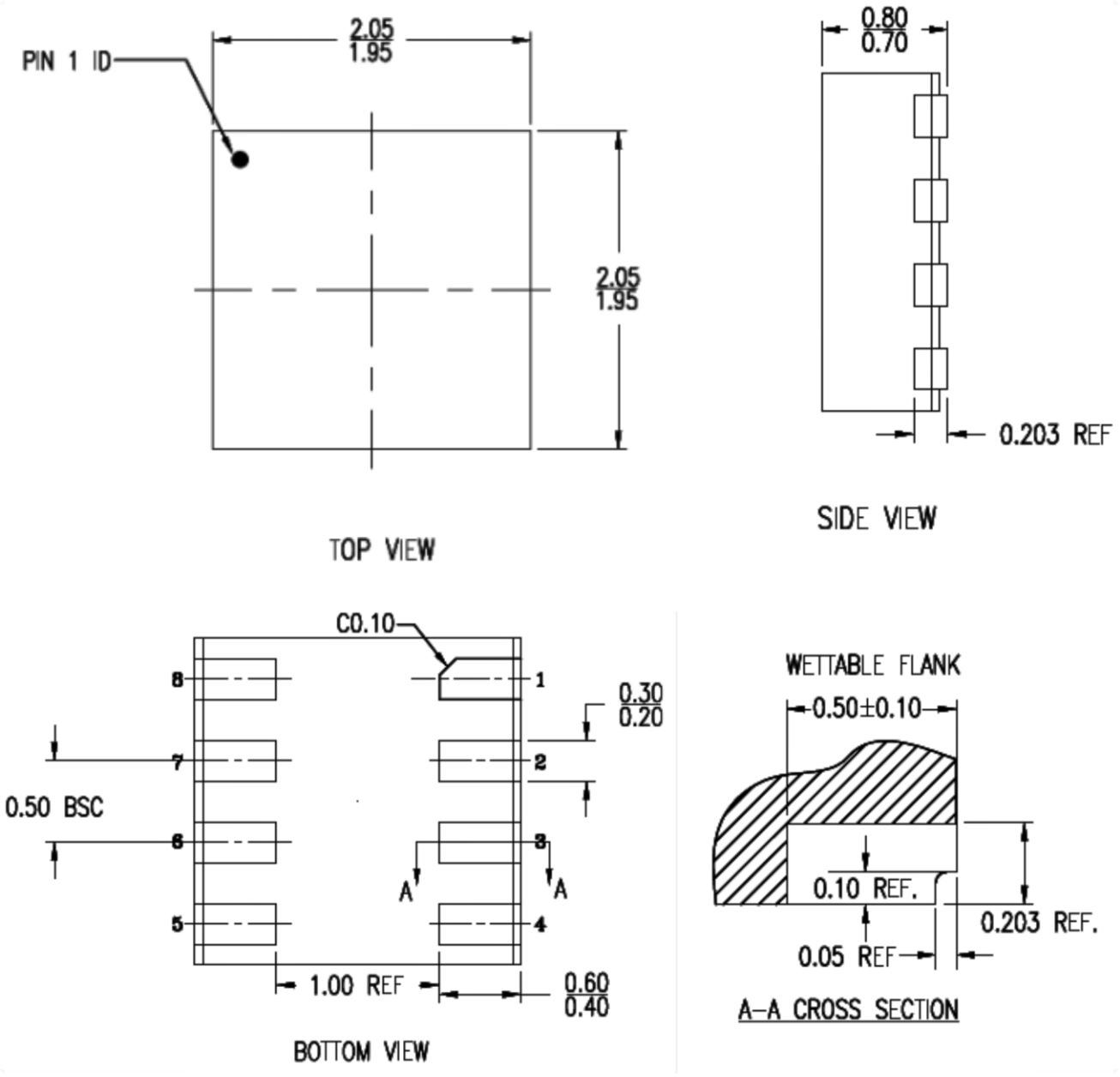

Figure 6 AU5424A1 Cross Sections

Note:

- All Dimensions and Tolerancing Conform to ANSI Y14.5M -1982
- All Dimensions are in Millimeters (mm)

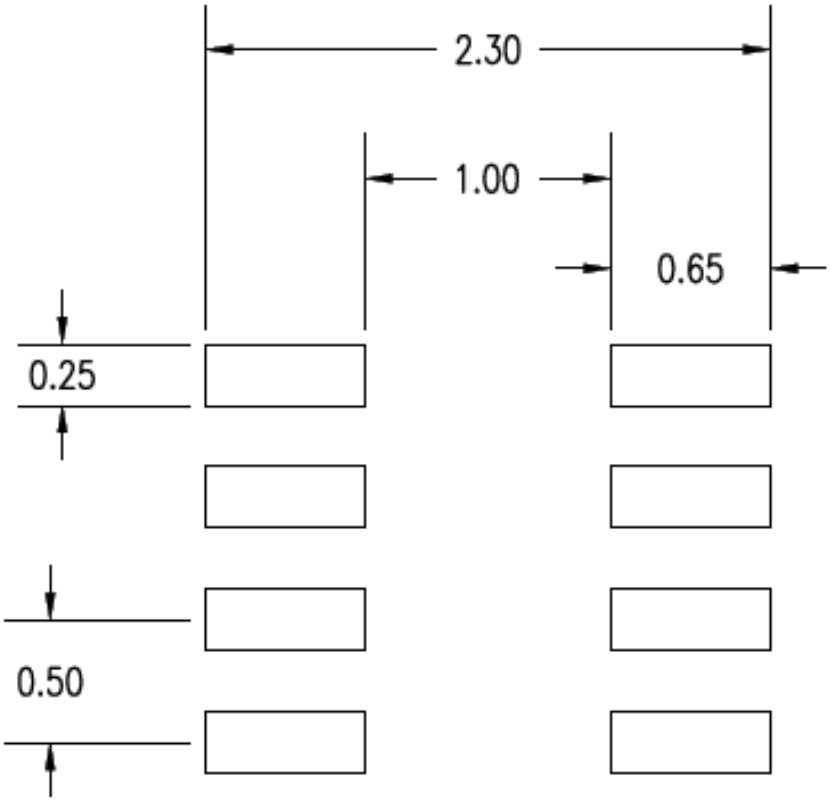

Figure 7 Recommended Land Pattern Dimension

Note:

- All Dimensions are in Millimeters (mm)
- All Angles are in Degrees
- Land Pattern Recommendation per IPC-7351B Generic Requirement for Mount Design and Land Pattern

7 Ordering Information

Table 13 Ordering Information for AU5424A1

Ordering Part Number (OPN)	Marking	Package	Shipping Package	Temp. Range
AU5424BA1-DAR[1]	24BA	8 Lead DFN 2 mm x 2 mm	Tape and Reel	–40 to 125 °C
AU5424A1-EVB	—	—	Evaluation Board	—

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering option. Add a T at the end of the OPN to denote a tray option.
2. This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU

8 Revision History

Table 14 Revision History

Version	Date	Description	Author
0.1	4th Jan 2021	AU5424A1 Data Sheet First Draft	Aurasemi
0.2	7th Feb 2021	Updated Table 13 Ordering Information Updated Conditions for Enable / Disable Delay Cycles	Aurasemi
0.3	8th Mar 2021	Updated Max Device Currents Format Changes	Aurasemi
0.4	9th April 2021	Corrected Propagation delay Specs Corrected Max Value of Output to Output Skew	Aurasemi
0.5	2nd July 2021	Table 13 changed to update the Ordering Part Number and Marking information.	Aurasemi
0.6	16th Aug 2021	Table 1 Pin Description added	Aurasemi
0.7	30th March 2022	Table 11 ESD Ratings added	Aurasemi
1.0	16th Aug 2022	AU5424A1 Datasheet: Production version released.	Aurasemi
1.1	13th Feb 2023	Section 4 : Input Clock and Power Supply Sequencing added	Aurasemi

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