

Article

Asymmetric Doherty Power Amplifier with Input Phase/Power Adjustment and Envelope Tracking

Fei Yang ¹, Jun Li ¹, Hongxi Yu ¹, Sen Yan ^{2,*}, Anxue Zhang ², Kaida Xu ² and Zhonghe Jin ³

¹ China Academy of Space Technology (Xi'an), Xi'an 710100, China; yfxjtu@163.com (F.Y.); liurz1388@163.com (J.L.); yuhongxi123@aliyun.com (H.Y.)

² School of Information and Communications Engineering, Xi'an Jiaotong University, Xi'an 710049, China; anxuezhang@mail.xjtu.edu.cn (A.Z.); kaidaxu@ieee.org (K.X.)

³ School of Aeronautics and Astronautics, Zhejiang University, Hangzhou 310027, China; jinzh@zju.edu.cn

* Correspondence: sen.yan@xjtu.edu.cn

Abstract: In this paper, the design and implementation of a Doherty power amplifier (DPA) are proposed using gallium nitride high electron mobility transistors (GaN HEMTs). Class-F and Class-C modes are combined to obtain an asymmetric DPA. The precise active load-pull controlling of fundamental and harmonic terminations of the DPA is simulated and analyzed, including the parasitics of the transistors. The measurements of the DPA with the phase difference, input power ratio adjustment, and envelope tracking of the auxiliary PA are discussed in detail in order to achieve a competitive performance. A greater than 63% drain efficiency is obtained within the 10-dB input power dynamic range at 2.1 GHz. The peak of the drain efficiency reaches 73%, with a corresponding output power of 46 dBm.

Keywords: Doherty; power amplifier; envelope tracking; Class-F; Class-C



check for updates

Citation: Yang, F.; Li, J.; Yu, H.; Yan, S.; Zhang, A.; Xu, K.; Jin, Z.

Asymmetric Doherty Power Amplifier with Input Phase/Power Adjustment and Envelope Tracking. *Electronics* **2021**, *10*, 2327. <https://doi.org/10.3390/electronics10192327>

Academic Editor: Esteban Telo-Cuautle

Received: 7 August 2021

Accepted: 15 September 2021

Published: 23 September 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

The high order modulations and the multi-carrier schemes, which are widely adopted to improve data rates and spectral efficiency in modern communication standards, have resulted in signal characteristics with large peak to average power ratios (PAPR). In order to meet the demand for minimized transmitter energy consumption, power control has become a key requirement in modern microwave frequency communication stations, and, thus, the power amplifier (PA) must provide a high efficiency when in the output power back-off (OPBO) condition [1].

The Doherty PA (DPA), first proposed in 1936, was primarily an efficiency enhancement technique, as shown in Figure 1a [1,2]. The interesting aspect of the Doherty configuration is the active load-pull technique, but the conventional DPA can provide only a 6-dB back-off level [3–7]. Owing to the requirement to operate at a power level of 10-dB back-off from the peak, several asymmetrical Doherty structures were introduced [8–12].

The quarter-wavelength transformer is normally utilized for the impedance matching of the main PA, which is also the main limitation of the bandwidth of the DPA, since the performances of the quarter-wavelength transformer is associated with the frequency. In order to extend the working bandwidth, some new techniques have been employed to the impedance transformers. As communication standards are currently spreading in different carrier frequencies, research efforts aiming to realize DPAs with ultra-wideband or multiband behaviors are urgently desired [13–22]. Multi-band DPAs allow the DPAs to optimize the performance in each carrier frequency, as demonstrated by both dual- and tri-band, which mainly focus on the optimization of the output combiners and the PAs [23–26].

Another important issue for Doherty matching is the non-negligible linear/nonlinear parasitic components of the high-power packaged devices, as shown in Figure 1b. The

active load-pull effect should be designed in the current source plane (I_{gen} plane), rather than the package plane. The most effective way for de-embedding the parasitics is by considering the output matching. In this paper, all of the parasitics will be de-embedded during the design procedure to accurately extract the performances of the fundamental and harmonic impedances at the I_{gen} plane.

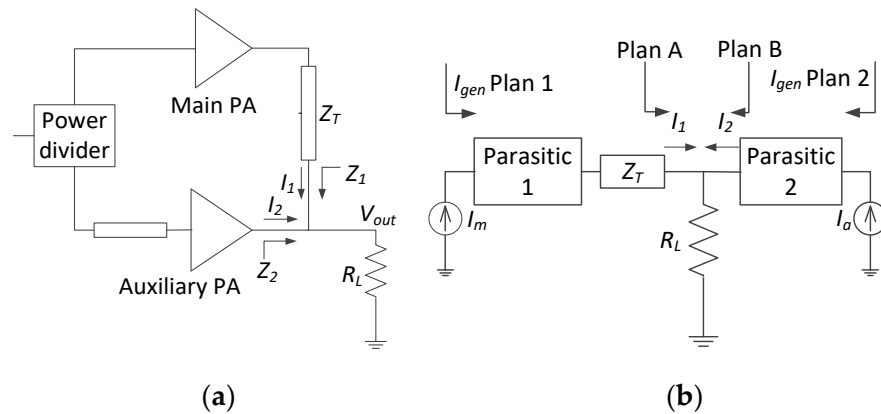


Figure 1. The schematic diagram of DPA: (a) schematic of Doherty; (b) equalized active load-pull effect.

Many works on DPAs have been carried out recently for both miniature and high frequencies. MMICs in GaAs, GaN, and CMOS processing are proposed in the recent literatures [27–31], which also show good performances by using some compact matching techniques.

To further enhance the efficiency of DPAs, the input power ratio and phase difference can be utilized to optimize the dynamic range efficiency performance and overcome the soft tune-on of the auxiliary PA [30,32]. Envelop tracking (ET) is also developed for main or auxiliary PA in order to significantly improve the efficiency during the wide input power range [33,34]. The turn-on time of the auxiliary amplifier can be controlled by the gate bias variation as well, which always cooperates with the power ratio adjustment method [35–37].

To mainly address the issue of the efficiency enhancement in the wide power dynamic range, we experimentally demonstrate an asymmetrical DPA with ET of the auxiliary amplifier in this paper, in order to keep a high efficiency over a wider range of output powers compared to classical Doherty designs. The paper is organized as follows. In Section 2, a DPA with a 10-W Class-F PA as the main amplifier and a 25-W Class-C PA as the auxiliary amplifier is proposed. The parasitics is included in the matching. The load-pull affection is carefully discussed, based on not only the fundamental termination, but also on the harmonic terminations. Then, the measurement of the DPA is discussed in Section 3. To further enhance the efficiency of the DPA, the adjustments of the input phase and the power ratio are utilized to optimize the efficiency performance during the dynamic range and overcome the soft tune-on of the auxiliary PA [2]. ET is also developed for the auxiliary PA to significantly improve the efficiency during the wide power range. A short conclusion is given in Section 4.

2. Doherty Amplifier Design

2.1. Asymmetrical DPA Theory

Figure 1 shows the basic structure of the proposed DPA and the corresponding equivalent circuit diagram. The characteristic impedance of the transformer and the resistance of the load can be carefully chosen to enable the main device to saturate at a point that corresponds to the maximum drain voltage waveform. This point is termed the transition point, and corresponds to an output power of nearly 10-dB less than the maximum output power in our design.

The currents in the common point are I_1 and I_2 , and the load resistor is R_L . To obtain the maximum output power point, $I_2 \approx 2 \times I_1$, so the voltage across R_L is:

$$V_{out} = (I_1 + I_2) \times R_L = 3I_1 \times R_L \quad (1)$$

The impedance seen from the plane A is:

$$Z_1 = V_{out} / I_1 = 3 \times R_L \quad (2)$$

At the 10-dB back-off point, i.e., $I_2 = 0$, the impedance seen from the plane A is:

$$Z_1 = R_L \quad (3)$$

Thus, the output matching network of the main PA should be used in order to make sure that Z_1 changes from R_L to $3 \times R_L$ as the power increases, which indicates that the efficiency can be maintained in the maximum level.

2.2. Class-F Main PA Design

The output and input matching networks of the Class-F mode PA are shown in Figure 2a. The substrate chooses Rogers RT5880, with a thickness of 0.254 mm and a relative permittivity of 2.2. The input matching is utilized to mainly consider the gain and the stability. The output matching is designed at the I_{gen} plane with parasitics de-embedded for three steps:

- Firstly, the open stubs ($Line_9$ and $Line_7$) are utilized in order to realize the second harmonic impedance short circuited and the third harmonic impedance open circuited, which are the harmonic suppression requirements of a third order Class-F mode PA, as shown in Figure 2b;
- Secondly, the fundamental matching for the optimum output power is designed as $R_{opt} = 33 \text{ Ohm}$ from the I_{gen} plane;
- Finally, the output impedance at the I_{gen} plane is also inverse to the load fundamental impedance in order to keep the maximum voltage sweep range and the maximum efficiency at the power back-off condition. This is the key part for the load-pull function to the main PA. With the variation of R_L , the impedance is seen from the I_{gen} plane at f_0 , and Z_1 , is inverted to the R_L . As shown in Figure 2b, as R_L shifts from 30 Ohm to 15 Ohm, Real (Z_1) @ f_0 changes from 33 Ohm to 64 Ohm, while the second harmonic impedance is kept in the nearly short condition (Real (Z_1) @ $2f_0 = 4 \text{ Ohm}$) during the load-pull process, and the third harmonic impedance is fixed to be closed to the open condition (Real (Z_1) @ $3f_0 = 830 \text{ Ohm}$).

The main PA is biased with a gate voltage (V_{gs}) of -3.2 V , corresponding to a class-B operation condition. The drain voltage (V_{ds}) is 28 V. The simulation results at the designed frequency of 2.1 GHz are summarized in Figure 2 as well. The drain waveform and the load-line are proposed in Figure 2c. The output power, gain, and efficiency are compared in Figure 2d at the back-off and the maximum output condition, respectively, corresponding to the load resistors R_L of 15 Ohm and 30 Ohm. The peak efficiency of the Class-F main PA is 72.5% at an output power of 40.8 dBm, corresponding to a power gain of 16.8 dB. At a 10-dB back-off condition, the voltage waveform at $R_L = 10 \text{ Ohm}$ is obviously higher than the condition of the no load-pull effect ($R_L = 30 \text{ Ohm}$). The drain efficiency increases from 34.4% to 49.2%, as the output power rises, as well as from 31.3 dBm to 31.7 dBm.

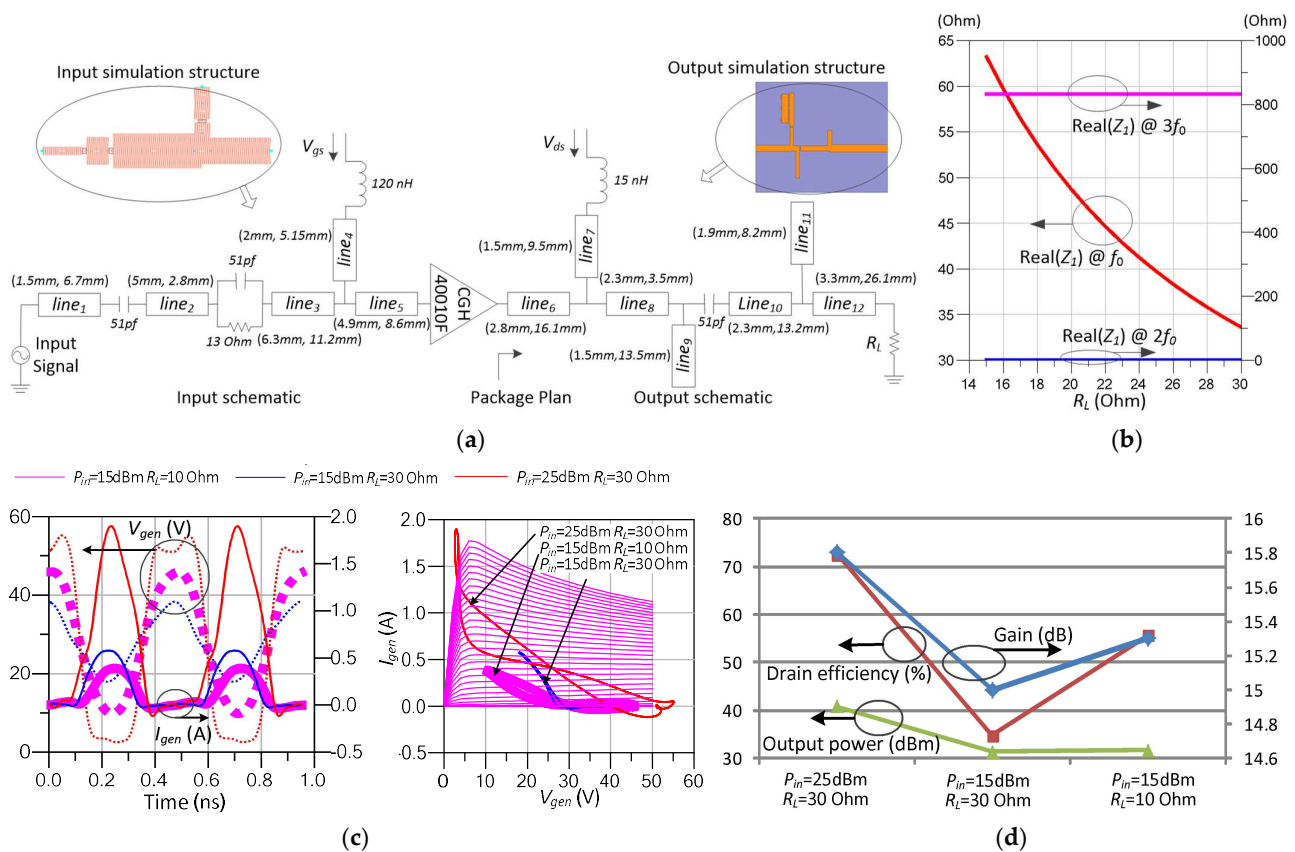


Figure 2. The simulation structure and results of Class-F PA: (a) simulation structure; (b) the real part of output impedances at I_{gen} plane $\text{Real}(Z_1)$ with the load impedance R_L shifting from 30 Ohm to 15 Ohm; (c) waveform and load-line, (d) gain, output power, and efficiency of the simulation results of Class-F PA with the load impedance R_L of 10 Ohm and 30 Ohm, respectively.

2.3. Class-C Auxiliary PA Design

The Class-C auxiliary amplifier is realized by the similar procedure. The matching structure and the simulation performance are shown in Figure 3. The bias of the proposed Class-C PA is $V_{gs} = -4$ V and $V_{ds} = 28$ V. The substrate also chooses Rogers RT5880, with a thickness of 0.254 mm and a relative permittivity of 2.2. Focusing on the frequency of 2.1 GHz, the simulation result of the Class-C PA delivers an efficiency greater than 78% at the maximum output power of 44 dBm, corresponding to a gain of 13 dB. As discussed in the Class-C PA bias condition, the gain drops quickly as the input power decreases, as shown in Figure 3c. This issue satisfies the requirement of the Doherty theory that the auxiliary PA is nearly tuned-off at the 10-dB back-off condition.

2.4. Doherty PA Realization

The DPA can then be designed by combining the Class-F 10-W and Class-C 25-W PAs. The two amplifiers' input ports are independent. By using separate coherent signal sources to drive the independent main and auxiliary inputs, it is possible to adjust the relative magnitudes and phases of the input ports. It will be shown later that the measured efficiency can be further enhanced at the power back-off condition.

Figure 4a shows the simulated waveform and the load-line of the main PA during the upper 10-dB dynamic range. Figure 4b summarizes the fundamental impedance variation and the corresponding output power according to the changing of the input power. Figure 4c shows the gain and the efficiency of the DPA in a 20-dB input power back-off range. All of the simulations by the CAD software are discussed in the I_{gen} plane to clearly show the variation characteristics of the waveform, the load-line, and the impedance.

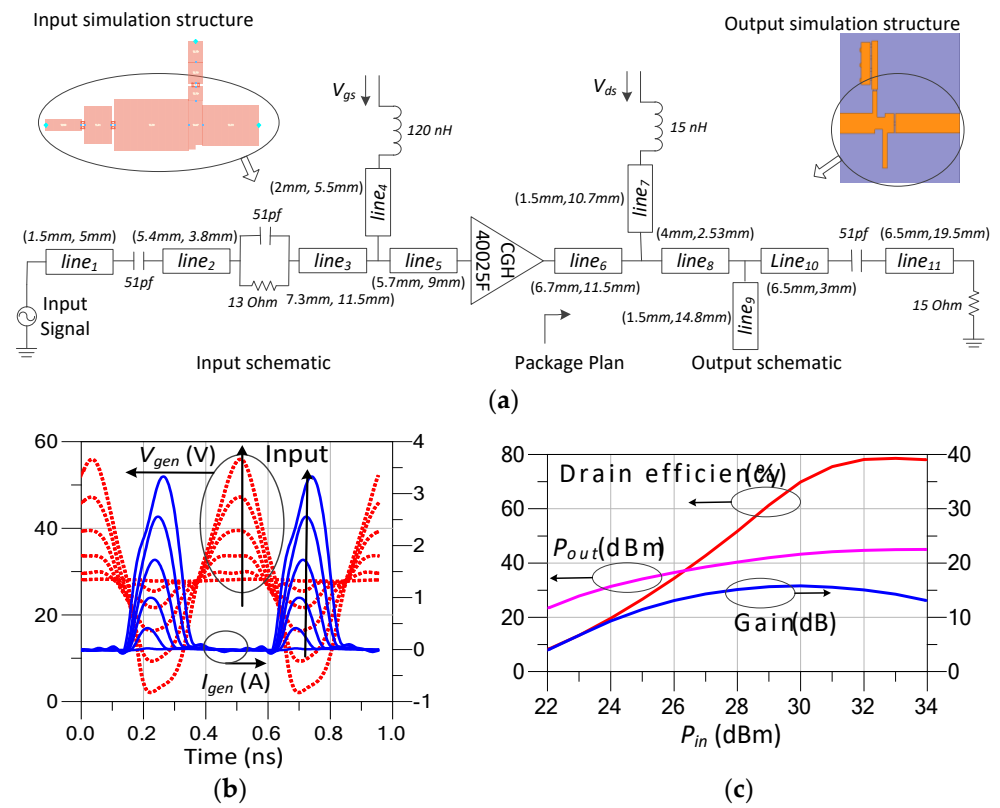


Figure 3. The simulation structure and results of the Class-C 25 watts auxiliary PA: (a) structure of Class-C PA; (b) waveform; (c) gain, output power, and drain efficiency.

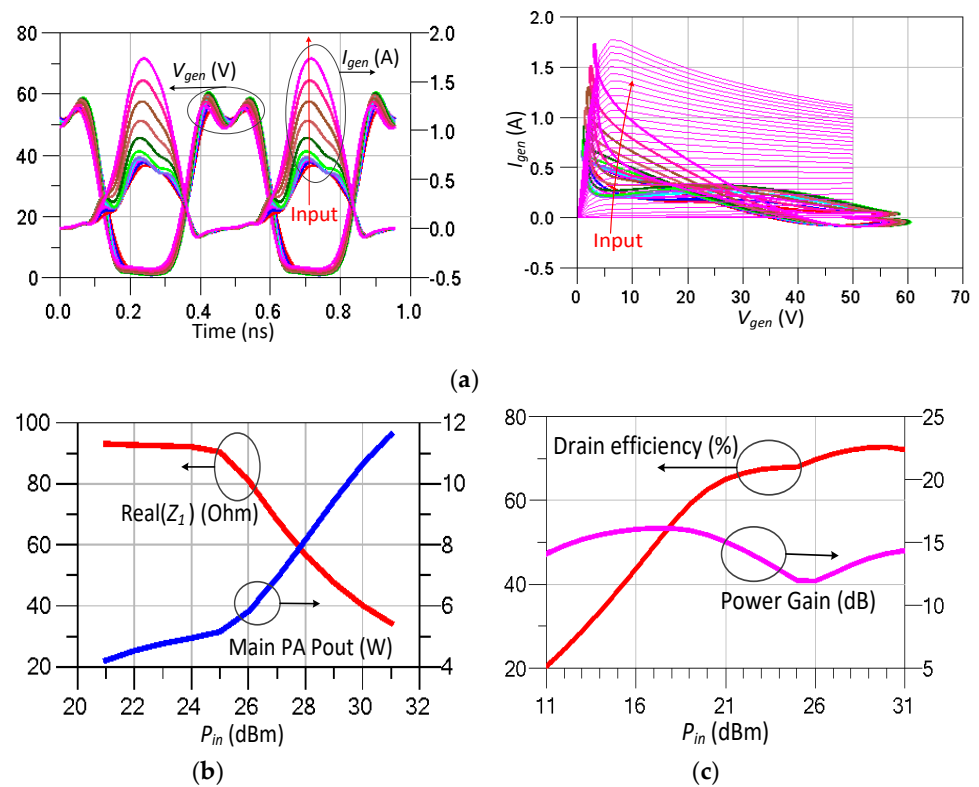


Figure 4. The simulation result of DPA: (a) the waveform and the load-line, (b) output power and fundamental impedance in the upper 10-dB input power range; (c) gain and efficiency of the DPA in 20-dB input back-off range.

From the simulation results, we can figure out that, as the input power P_{in} decreases from the maximum condition, the auxiliary amplifier's load-pull effect to the main amplifier makes the fundamental output impedance Z_1 change from 32 Ohm to 93 Ohm, i.e., almost three times the amount, (Figure 4c), and the voltage within the maximum sweep range is stable, as shown in Figure 4a. Correspondingly, the efficiency of the main amplifier is kept in the maximum condition.

3. Fabrication and Measurement

The photograph of the presented DPA is shown in Figure 5a. The inputs of the main and auxiliary PAs are independent in order for a more detailed measurement of the phase and the power ratio variation effect to search for the maximum efficiency. The optimum phase shift, the input power adjustment, and the V_{ds} of the auxiliary PA are depicted according to the input power level in Figure 5b, in order to obtain the efficiency enhancement. In this figure, the phase difference and the power ratio at the maximum output condition is termed as the reference point.

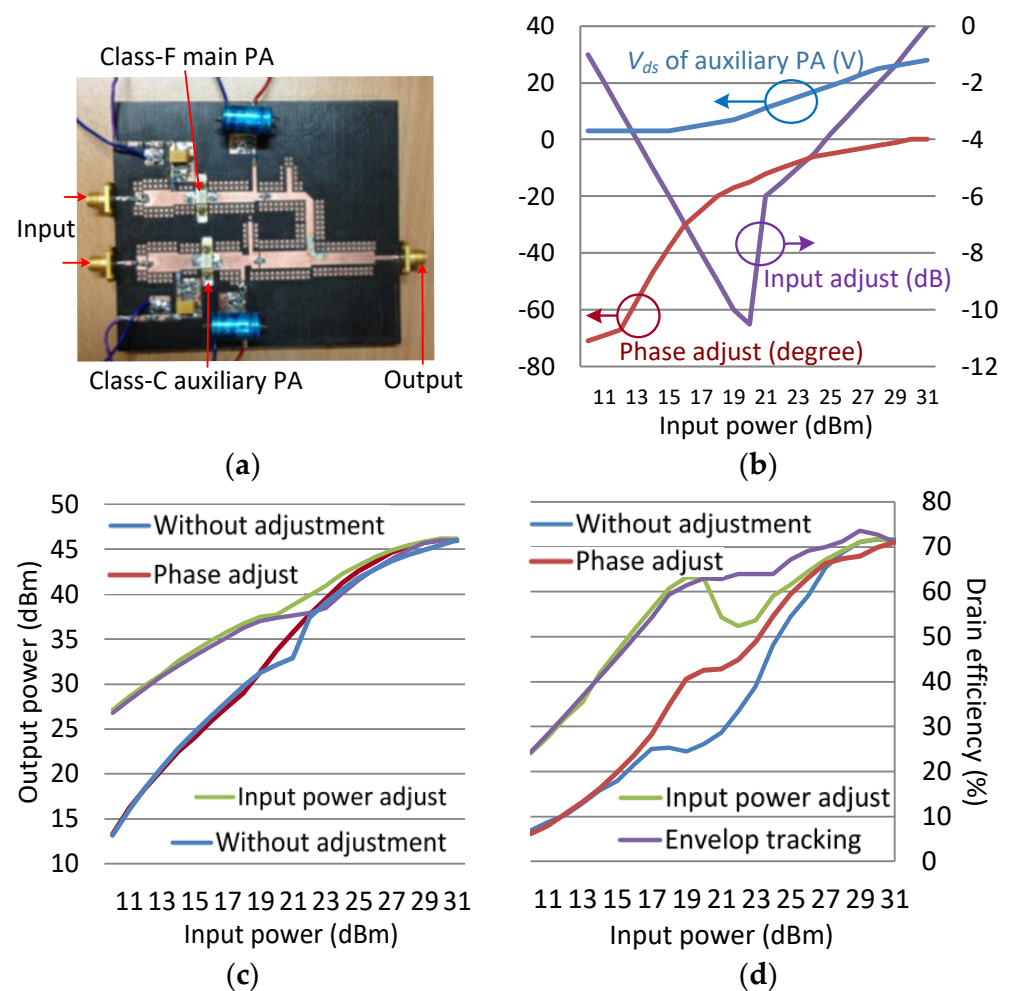


Figure 5. The measurement result of DPA: (a) photograph of the fabricated DPA; (b) phase and input power adjustment of auxiliary PA, V_{ds} of auxiliary PA for ET; measurement results of (c) output power and (d) drain efficiency.

Figure 5c,d depicts the measured output power, the gain, and the drain efficiency of the proposed DPA at a frequency of 2.1 GHz, when it is driven by a single continuous wave and over the 20-dB input power range. In Figure 5c,d, the blue lines show the measurement results without any adjustment. The red lines show the phase adjusted results. The green

lines show the input power adjusted results, and the purple lines show the envelope tracking results.

As depicted in Figure 5d, when the phase is defined at the maximum output power, an efficiency of over 71% can be attributed with an output power of 46 dBm. However, at the back-off range, the efficiency drops sharply. At the 10-dB input power back-off, the efficiency is only 28%. This means that the active load-pull between the main amplifier and the auxiliary amplifier is not fully effective. By tuning the phase difference between the two single-ended PAs, the efficiency can be significantly improved from 28% to nearly 42%, and the average efficiency is also enhanced within the 10-dB range. Thus, the phase deviation that is caused by the amplitude variation effect is an unneglected characteristic for the DPA, as the main and the auxiliary PAs are not biased at the same condition. However, this is unfortunately always true, especially considering the auto turn-on/off requirement of the auxiliary PA at the back-off condition.

The measurement results of the appropriate power adjustment are also depicted as a green line in Figure 5d, which shows the typical and excellent DPA performances. Within the input power range of 10-dB, the efficiency is higher than 52%. Due to the fact that more power is offered to the main PA during the dynamic range, the attribution to the DPA's efficiency and the output power from the auxiliary PA at the back-off condition are decreased, especially in the back range from 6-dB to 10-dB.

Figure 5d also includes the proposed DPA results with the ET of the auxiliary amplifier. By comparing with the power adjustment results, we can clearly see that the efficiency performance is improved when ET is used. Within the upper 10-dB operation range, the auxiliary PA's drain voltage decreases from 28 V to 10 V, which can ensure an efficiency higher than 60%. The main PA's efficiency is maintained in the maximum condition due to the active load-pull effect from the auxiliary PA. ET has been shown to be a powerful methodology of efficiency enhancement, in order to overcome the soft tune-on, and the efficiency drops in the middle of the input power dynamic range.

In our system, the efficiency is mainly enhanced by the DPA, and a digital processor is used to perform the predistortion, i.e., the input power assignment and also the phase controlling. As shown in Figure 6, the baseband signal is also pre-distorted to improve the linearity. The data of how to adjust the input power and phase to enhance the efficiency, as well as the drain voltage of the auxiliary PA, are stored in the digital processor.

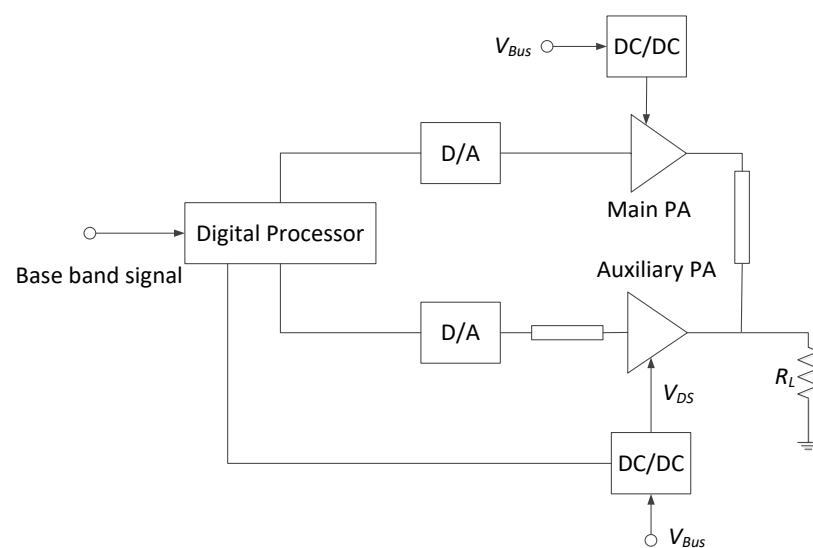


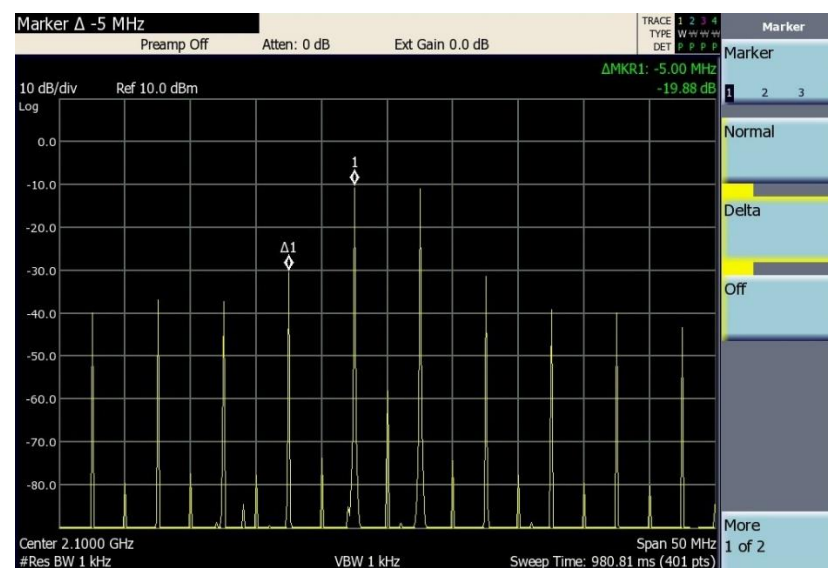
Figure 6. The system schematic with digital processor, D/A and DPA.

The third-order intermodulation (IM3) is measured at an input power of 30 dBm (1 dB's back-off from saturation point, corresponding to a single tone of 27 dBm, with 5 MHz interval). The IM3 is better than 19.88 dBc, which shows a very good linearity result.

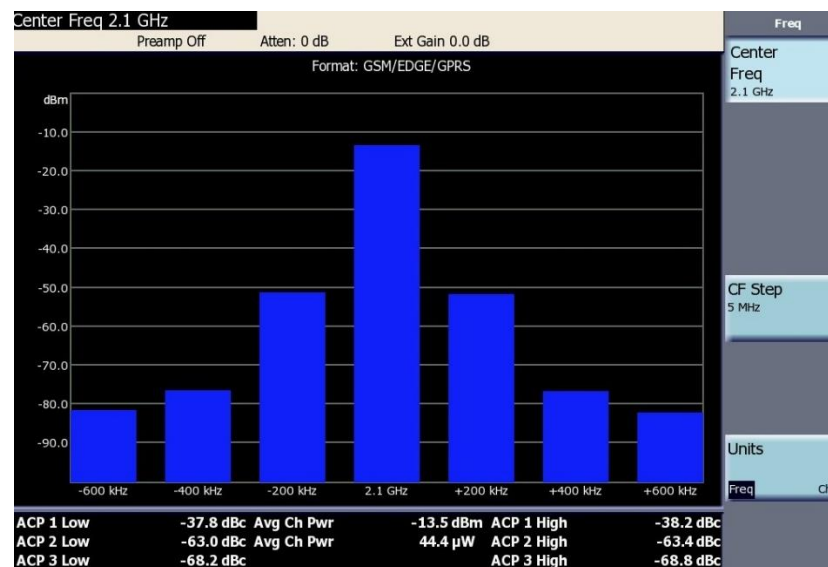
Furthermore, the adjacent channel power ratio (ACPR) is measured at the condition of the envelop peaking power at the saturation point (input power of 31 dBm). The input EDGE signal has a 200 KHz channel bandwidth and a 3.6 dB peak-to-average power ratio (PAPR). An ACPR of -37.8 dBc has been measured at 2.1 GHz. The IM3 and ACPR are summarized in Table 1 and displayed in Figure 7.

Table 1. Linearity measurement results.

Freq. (GHz)	2.1	Narrow-Band Designed
IM3 (dBc)	19.88	Two tones input power of 30 dBm (1-dB back-off from saturation point)
ACPR (dBc)	37.8	EDGE signal of 200 KHz channel bandwidth and 3.6 dB PAPR, envelop peak at saturation point



(a)



(b)

Figure 7. The linearity performance of DPA with DPD at 2.1 GHz: (a) IM3 measurement result of DPA with DPD at 30 dBm input power condition (two tones); (b) ACPR measurement result of DPA with DPD at peaking power of saturation condition.

4. Conclusions

In this paper, we have given the design, implementation, and experimental results of an asymmetric DPA using a Class-F main PA and Class-C auxiliary PA. The main and auxiliary PAs' design and the load-pull effect within the Doherty schematic are proposed by precisely controlling the harmonic impedances during the dynamic range. Then, detailed measurements and discussions have been taken to further enhance the efficiency by using the phase adjustment, input power ratio variation, and envelope tracking of the auxiliary PA. A greater than 63% efficiency within the upper 10-dB input power dynamic range is achieved. The peak efficiency reaches 73% with a corresponding output power of 46 dBm. Finally, in Table 2, the proposed PA is compared with other DPAs in terms of the operation frequency, dynamic range, output power, and efficiency. It can be seen that the presented DPA has a competitive efficiency performance within the 10-dB power range.

Table 2. Comparison with latest literatures.

Ref.	Frequency (GHz)	Dynamic Range (dB)	Output Power (dBm)	Drain Efficiency (%)
2021 [12]	1.9	9	46	54.6–75.5
2021 [10]	2.19	10	46.3	47–72.1
2021 [37]	3.5	10	41.6	51–63 (PAE)
This work	2.1	10	46	63–73

Author Contributions: Conceptualization, F.Y. and S.Y.; methodology, F.Y.; software design, F.Y.; validation, F.Y., S.Y. and K.X.; formal analysis, F.Y.; investigation, F.Y.; resources, J.L., H.Y. and Z.J.; data curation, K.X.; writing—original draft preparation, F.Y.; writing—review and editing, S.Y. and K.X.; supervision, A.Z. and Z.J.; project administration, F.Y.; funding acquisition, H.Y. All authors have read and agreed to the published version of the manuscript.

Funding: Innovation support program of Shaanxi Province, China: 2020KJXX-070.

Conflicts of Interest: The authors declare no conflict of interest.

References

- Doherty, W.H. A New High Efficiency Power Amplifier for Modulated Waves. *Proc. IRE* **1936**, *24*, 1163–1182. [\[CrossRef\]](#)
- Cripps, S. RF power amplifiers for wireless communications. *IEEE Microw. Mag.* **2000**, *1*, 64. [\[CrossRef\]](#)
- Tasker, P. Practical waveform engineering. *IEEE Microw. Mag.* **2009**, *10*, 65–76. [\[CrossRef\]](#)
- Musolff, C.; Kamper, M.; Abou-Chahine, Z.; Fischer, G. A Linear and Efficient Doherty PA at 3.5 GHz. *IEEE Microw. Mag.* **2012**, *14*, 95–101. [\[CrossRef\]](#)
- Giofre, R.; Colantonio, P.; Giannini, F.; Piazzon, L. New Output Combiner for Doherty Amplifiers. *IEEE Microw. Wirel. Compon. Lett.* **2013**, *23*, 31–33. [\[CrossRef\]](#)
- Modi, S.; Prakash, R.; Yanduru, N.; Balsara, P. A novel efficiency improvement technique for Doherty power amplifiers. In Proceedings of the Texas Symposium on Wireless and Microwave Circuits and Systems, Waco, TX, USA, 3–4 April 2014; pp. 1–4.
- Pang, J.; Li, Y.; Chu, C.; Peng, J.; Zhou, X.Y.; Zhu, A. Extend high efficiency range of Doherty power amplifier by modifying characteristic impedance of transmission lines in load modulation network. In Proceedings of the 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 18–27 June 2020; pp. 1–4.
- Kim, J.; Fehri, B.; Boumaiza, S.; Wood, J. Power Efficiency and Linearity Enhancement Using Optimized Asymmetrical Doherty Power Amplifiers. *IEEE Trans. Microw. Theory Tech.* **2010**, *59*, 425–434. [\[CrossRef\]](#)
- Ishikawa, R.; Takayama, Y.; Honjo, K. Fully Integrated Asymmetric Doherty Amplifier Based on Two-Power-Level Impedance Optimization. In Proceedings of the 13th European Microwave Integrated Circuits Conference, Madrid, Spain, 23–25 September 2018; pp. 253–256.
- Takagi, Y.; Hasegawa, N.; Ohta, Y.; Ishikawa, R.; Honjo, K. High-Efficiency Asymmetric Doherty Power Amplifier with Spurious Suppression Circuit. In Proceedings of the 50th European Microwave Conference, Utrecht, The Netherlands, 12–14 January 2021; pp. 308–311.
- Fang, X.H.; Cheng, K.-K.M. Extension of High-Efficiency Range of Doherty Amplifier by Using Complex Combining Load. *IEEE Trans. Microw. Theory Tech.* **2014**, *62*, 2038–2047. [\[CrossRef\]](#)
- Xu, Y.; Pang, J.; Wang, X.; Zhu, A. Enhancing Bandwidth and Back-Off Range of Doherty Power Amplifier with Modified Load Modulation Network. *IEEE Trans. Microw. Theory Tech.* **2021**, *69*, 2291–2303. [\[CrossRef\]](#)

13. Bathich, K.; Markos, A.Z.; Boeck, G. A Wideband GaN Doherty Amplifier with 35% Fractional Band-width. In Proceedings of the 40th European Microwave Conference, Paris, France, 28–30 September 2010; pp. 1006–1009.
14. Gustafsson, D.; Andersson, C.M.; Fager, C. A Modified Doherty Power Amplifier with Extended Bandwidth and Reconfigurable Efficiency. *IEEE Trans. Microw. Theory Tech.* **2013**, *61*, 533–542. [[CrossRef](#)]
15. Wu, T.Y.T.; Boumaiza, S. A Modified Doherty Configuration for Broadband Amplification Using Symmetrical Devices. *IEEE Trans. Microw. Theory Tech.* **2012**, *60*, 3201–3213. [[CrossRef](#)]
16. Giofre, R.; Piazzon, L.; Colantonio, P.; Giannini, F. An Ultra-Broadband GaN Doherty Amplifier, with 83% of Fractional Bandwidth. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *24*, 775–777. [[CrossRef](#)]
17. Fang, X.-H.; Cheng, K.-K.M. Improving Power Utilization Factor of Broadband Doherty Amplifier by Using Bandpass Auxiliary Transformer. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 2811–2820. [[CrossRef](#)]
18. Zhang, Z.; Cheng, Z.; Li, H.; Ke, H.; Guo, Y.J. A Broadband Doherty Power Amplifier with Hybrid Class-EFJ Mode. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 4270–4280. [[CrossRef](#)]
19. Kang, H.; Lee, W.; Oh, S.; Oh, H.; Choi, W.; Lee, H.; Hwang, K.C.; Lee, K.-Y.; Yang, Y. Optimized Broadband Load Network for Doherty Power Amplifier Based on Bandwidth Balancing. *IEEE Microw. Wirel. Compon. Lett.* **2020**, *31*, 280–283. [[CrossRef](#)]
20. Li, M.; Pang, J.; Li, Y.; Zhu, A. Bandwidth Enhancement of Doherty Power Amplifier Using Modified Load Modulation Network. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 1824–1834. [[CrossRef](#)]
21. Zhou, X.Y.; Zheng, S.Y.; Chan, W.S.; Chen, S.; Ho, D. Broadband Efficiency-Enhanced Mutually Coupled Harmonic Postmatching Doherty Power Amplifier. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 1758–1771. [[CrossRef](#)]
22. Naah, G.; Giofre, R. Empowering the Bandwidth of Continuous-Mode Symmetrical Doherty Amplifiers by Leveraging on Fuzzy Logic Techniques. *IEEE Trans. Microw. Theory Tech.* **2019**, *68*, 3134–3147. [[CrossRef](#)]
23. Chen, W.; Bassam, S.A.; Li, X.; Liu, Y.; Rawat, K.; Helou, M.; Ghannouchi, F.M.; Feng, Z. Design and Linearization of Concurrent Dual-Band Doherty Power Amplifier with Frequency-Dependent Power Ranges. *IEEE Trans. Microw. Theory Tech.* **2011**, *59*, 2537–2546. [[CrossRef](#)]
24. Saad, P.; Piazzon, L.; Colantonio, P.; Moon, J.; Giannini, F.; Andersson, K.; Kim, B.; Fager, C. Multi-band/multi-mode and efficient transmitter based on a Doherty Power Amplifier. In Proceedings of the 2012 7th European Microwave Integrated Circuit Conference, Amsterdam, The Netherlands, 29–30 October 2012; pp. 1031–1034.
25. Mohamed, A.M.M.; Boumaiza, S.; Mansour, R.R. Electronically Tunable Doherty Power Amplifier for Multi-Mode Multi-Band Base Stations. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2013**, *61*, 1229–1240. [[CrossRef](#)]
26. Rawat, K.; Ghannouchi, F.M. Design Methodology for Dual-Band Doherty Power Amplifier with Performance Enhancement Using Dual-Band Offset Lines. *IEEE Trans. Ind. Electron.* **2011**, *59*, 4831–4842. [[CrossRef](#)]
27. Gustafsson, D.; Cahuana, J.C.; Kuylenstierna, D.; Angelov, I.; Fager, C. A GaN MMIC Modified Doherty PA with Large Bandwidth and Reconfigurable Efficiency. *IEEE Trans. Microw. Theory Tech.* **2014**, *62*, 3006–3016. [[CrossRef](#)]
28. Jee, S.; Lee, J.; Son, J.; Kim, S.; Kim, C.H.; Moon, J.; Kim, B. Asymmetric Broadband Doherty Power Amplifier Using GaN MMIC for Femto-Cell Base-Station. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 2802–2810.
29. Carneiro, M.L.; Deltimple, N.; Carvalho, P.H.; Belot, D.; Kerhervé, E. Fully integrated CMOS Doherty power amplifier with network matching optimization for die size reduction. In Proceedings of the 2014 44th European Microwave Conference (EuMC), Rome, Italy, 6–9 October 2014; pp. 1269–1272.
30. Darraji, R.; Kwan, A.K.; Fadhel, M. Ghannouchi, and Mohamed Helou. Digitally Equalized Doherty RF Front-End Architecture for Broadband and Multi-standard Wireless Transmitters. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 1978–1988. [[CrossRef](#)]
31. Park, Y.; Lee, J.; Jee, S.; Kim, S.; Kim, C.H.; Park, B.; Kim, B. GaN HEMT MMIC Doherty Power Amplifier with High Gain and High PAE. *IEEE Microw. Wirel. Compon. Lett.* **2015**, *25*, 187–189. [[CrossRef](#)]
32. Fang, X.; Liu, H.; Cheng, K.M.; Boumaiza, S. Two-Way Doherty Power Amplifier Efficiency Enhancement by Incorporating Transistors' Nonlinear Phase Distortion. *IEEE Microw. Wirel. Compon. Lett.* **2018**, *28*, 168–170. [[CrossRef](#)]
33. Kim, I.; Kim, B. A 2.655 GHz 3-stage Doherty power amplifier using envelope tracking technique. In Proceedings of the 2010 IEEE MTT-S International Microwave Symposium, Anaheim, CA, USA, 23–28 May 2010; pp. 1496–1499.
34. Choi, J.; Kang, D.; Kim, D.; Kim, B. Optimized Envelope Tracking Operation of Doherty Power Amplifier for High Efficiency Over an Extended Dynamic Range. *IEEE Trans. Microw. Theory Tech.* **2009**, *57*, 1508–1515. [[CrossRef](#)]
35. Lees, J.; Goss, M.; Benedikt, J.; Tasker, P.J. Single-tone optimization of an adaptive-bias Doherty structure. In Proceedings of the IEEE MTT-S International Microwave Symposium Digest, Philadelphia, PA, USA, 8–13 June 2003; pp. 2213–2216.
36. Park, Y.; Lee, J.; Jee, S.; Kim, S.; Kim, B. Gate Bias Adaptation of Doherty Power Amplifier for High Efficiency and High Power. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *25*, 136–138. [[CrossRef](#)]
37. Fishler, D.; Popovic, Z.; Barton, T. Supply Modulation Behavior of a Doherty Power Amplifier. *IEEE J. Microw.* **2021**, *1*, 508–512. [[CrossRef](#)]