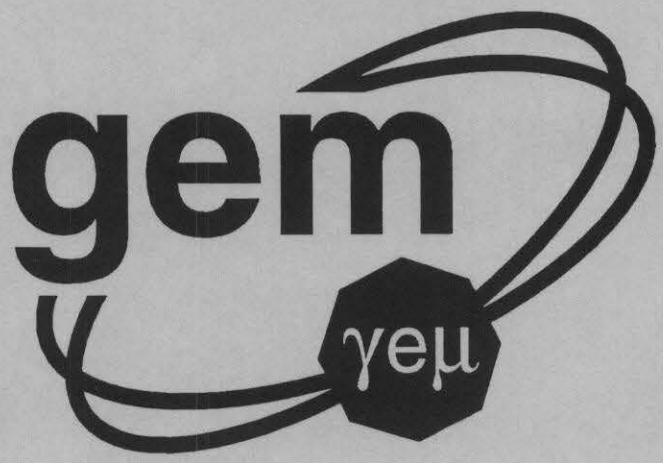
GEM TN-93-346



GEM Electronics Design Review - SSCL

February 24, 1993

Abstract:

Agenda, attendees, and presentations of the GEM Electronics Design Review Meeting held at the SSC Laboratory on February 24, 1993. Goals are to present the design requirements, conceptual design, R&D issues and preliminary cost, schedule and manpower/resource plans for the GEM electronics subsystem to GEM management and selected outside reviewers. The presentations and review should be a midcourse correction for the GEM TDR.

GEM ELECTRONICS DESIGN REVIEW

Wednesday, February 24, 1993

SSCL Room B125

GOALS: PRESENT THE DESIGN REQUIREMENTS, CONCEPTUAL DESIGN, R&D ISSUES AND PRELIMINARY COST, SCHEDULE AND MANPOWER/RESOURCE PLANS FOR THE GEM ELECTRONICS SUBSYSTEM TO GEM MANAGEMENT AND SELECTED OUTSIDE REVIEWERS. THE PRESENTATION AND REVIEW SHOULD BE A MIDCOURSE CORRECTION FOR THE GEM TDR.

Reviewers:
1. V. Radeka, BNL
2. P. Lecomte, ETH, Zurich (Outside reviewer)
3. Person from LeCroy Corp. (Farr/LeCroy) (Outside reviewer)

DRAFT AGENDA (see notes below)

9:00	Overview of GEM Electronics	Marlow
9:20	Silicon vertex front end	Mills/Hahn/Cooke
10:00	IPC front end	Musser/O'Connor*/Britton
11:00	Calorimeter front end	Parsons/Rescia/Sippach
12:00	Lunch	
13:00	Muon front end	Marlow/Wixted/Varner/Pinsky
14:00	Calorimeter trigger	Cleland/Crosetto
14:40	Muon trigger	Atiya/Liu
15:20	DAQ	Bowden
15:50	Rack Design and Placement	Freeman
16:10	Grounding and Shielding	Lau
16:30	Review committee executive session	
17:30	Committee and GEM management meet for preliminary findings and discussion. Electronics group principals may need to be present.	
18:00	Adjourn	

Notes: 1) First person listed after each each talk is responsible for time and topic assignments for the additional speakers.

2) *Paul O'Connor will cover all IPC and CSC preamp work in his talk.

Name	Institution	Phone	FAX / E-mail
Norman Lau	SSCL	214-708-6372	SSCVX1::LOU
Werner Farr	LeCroy	914-578-6027	914-578-5984
Pierre Lecomte	ETHZ	41 22 767 6028	41 22 782 8923
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Paul O'Connor	BNL	516 282 7577	"5773/ poc@bnl.gov
Igor Golutvin	Dubna	(214) 708-3064	6088/IGOLUTUIN@SSCVX1
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Sangkoo Hahn	LANL	(505)667-2507	(505)665-4657 HAHN@SANGKOO.LANL.G
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Gary Liu	@ Caltech	818-356-6681	CITHEX::GL
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V. Khabarov	Dubna JINR		
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GARY SMITH	LANL	505-667-2819	505-665-4657
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ALAN GARA	NEVIS	914 591-8100	GARA@NEVIS
GARY VARNER	BOSTON U.	617-353-4117	varner@buphy.bu.edu
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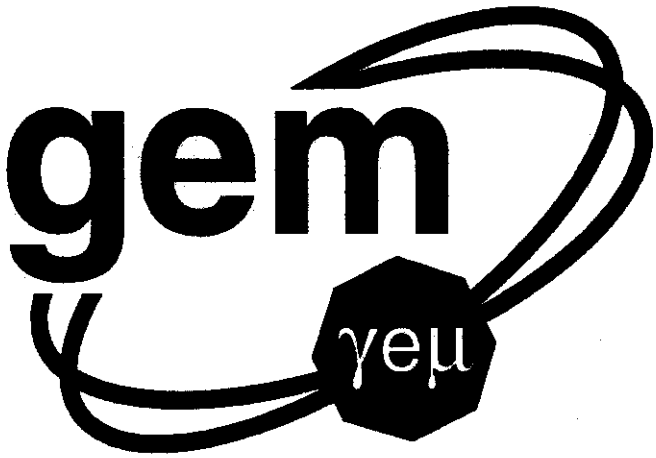
M. Baturitsky	Minsk, BSU	26-21-93	
M. Clemon	Univ. of Pittsburgh	412-624-9048	CLEMEN@PM2.CIS.PITT.ED
D. Crosetto	SSCL	3 412-708 6212	CROSETTO@SSCVX1.SSC.GOV

Name	Institution	Phone	FAX / E-MAIL
Brad Cooke	LANL	505-667-8512	cooke@sstlla.lanl.gov
Dan Marlow	Princeton	609 258 4383	PUPHEP::MARLOW
Paschal M. Kibuule	SSCL	(214)708-6172	PMK@sscig.ssc.gov
Rick Shypit	SSCL	(214)708-4465	Shypit@SSCVX1



Presentation by:

Sangkoo Hahn

Silicon Tracker Electronics

(Cost, Schedule, R&D Issues
+
Bipolar Chip Design)

2-22-93

Sangkoo Hahn

Los Alamos National Laboratory
Box 1663, MS-D448
Los Alamos, NM 87545
(505) 667-2507

Agenda:

1.	Sangkoo Hahn	20 min
	System Overview	
	Cost and Scheduling	
	Bipolar Chip Development	
2.	Bradley Cooke	15 min
	Systems Design	
	Digital Architecture	
3.	Gary Richardson	5 min
	Multi-Chip Module Development	

Siliicon Tracker Electronics Design Requirements

Operation in High Radiation Environment (5MRad total dose)

0.8 Tesla Magnetic Field

Single Bunch (16ns) Time Resolution

Single Sided Strip Detector Operation

Operation With 18cm Strip Length Detector

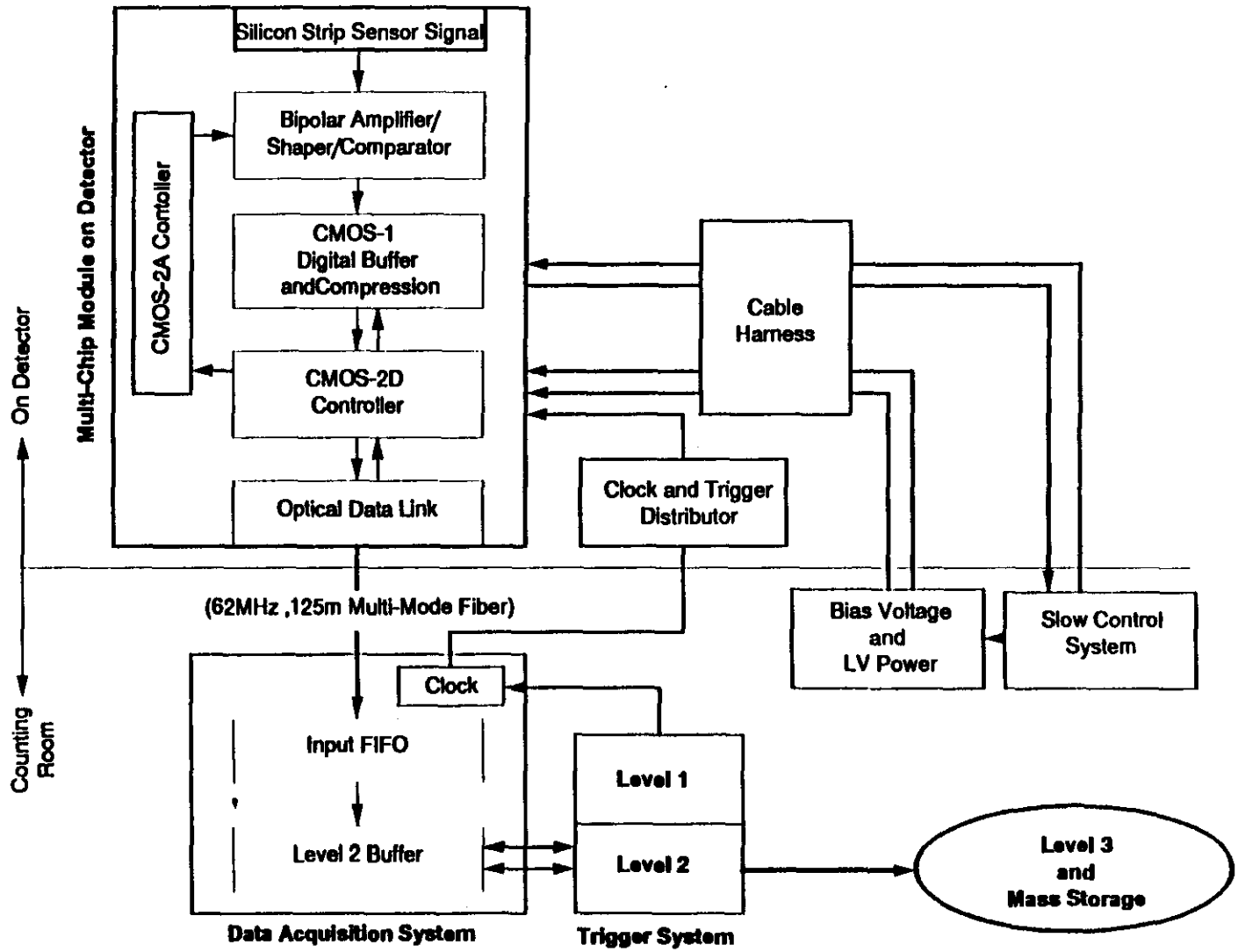
Digital Level 1 Buffer on Detector (up to 4 μs)

Single Channel Occupancy .001-.01 for 10^{33}-10^{34}

Electronics Noise Rate < Rate From True Hits

Power per Channel < 2 mW

Silicon Tracker Electronics System Architecture



System Components

Front End Electronics:

Multi Chip Module	(chip support and interconnect)
Bipolar Chip	(Analog amplifier and comparator)
CMOS-1	(Level 1 Buffering and Data Compression)
CMOS-2D	(Data Transmission and Housekeeping)
CMOS-2A	(Analog Housekeeping)
Optical Data Link	(Data Transmission to DAQ)

Data Acquisition:

Rack based system for receiving F/O data
Level 2 Buffer

Services

Cable Plant on and off detector
Bias and Low voltage Power Supplies
Slow Control System
Test Stations

SUBSYSTEM: Electronics

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS No.: 50.02. 2.1

WBS Descript.: Si-Tracker

WBS QTY: 2091 (incl. 5% spare)

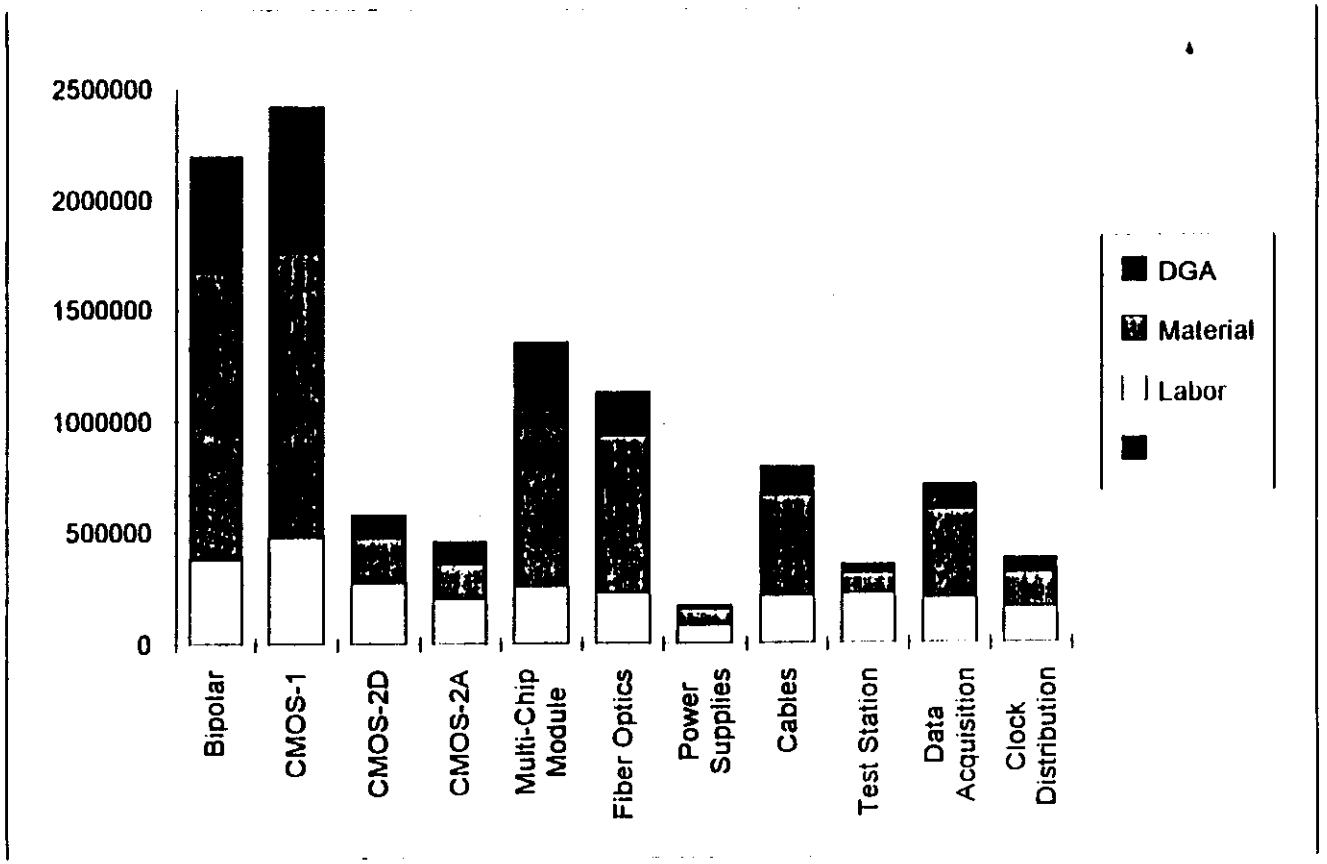
WBS UM: MCM

WBS No.	Item	Labor	Material	DGA	Item Total
50.02.2.1.0	Bipolar	375,753	1,291,860	533,636	**2,201,249**
50.02.2.1.1	CMOS-1	475,002	1,282,080	667,691	**2,424,774**
50.02.2.1.2.1	CMOS-2D	272,376	201,439	108,978	**582,793**
50.02.2.1.2.2	CMOS-2A	199,926	156,588	103,389	**459,903**
50.02.2.1.3	Multi-Chip Module	255,000	794,580	304,378	**1,353,958**
50.02.2.1.4	Fiber Optics	227,177	702,710	204,575	**1,134,462**
50.02.2.1.5	Power Supplies	80,039	72,000	21,285	**173,324**
50.02.2.1.6	Cables	211,178	450,465	132,329	**793,972**
50.02.2.1.7	Test Station	220,051	92,000	43,687	**355,739**
50.02.2.1.8	Data Acquisition	201,352	393,750	119,020	**714,123**
50.02.2.1.9	Clock Distribution	158,426	154,000	68,734	**381,159**
50.02.2.1.10	Slow Control	194,526	55,000	32,438	**281,964**
	Sub Total	**2,870,806**	**5,646,472**	**2,340,141**	
			TOTAL		**10,857,419**

SUBSYSTEM: Electronics

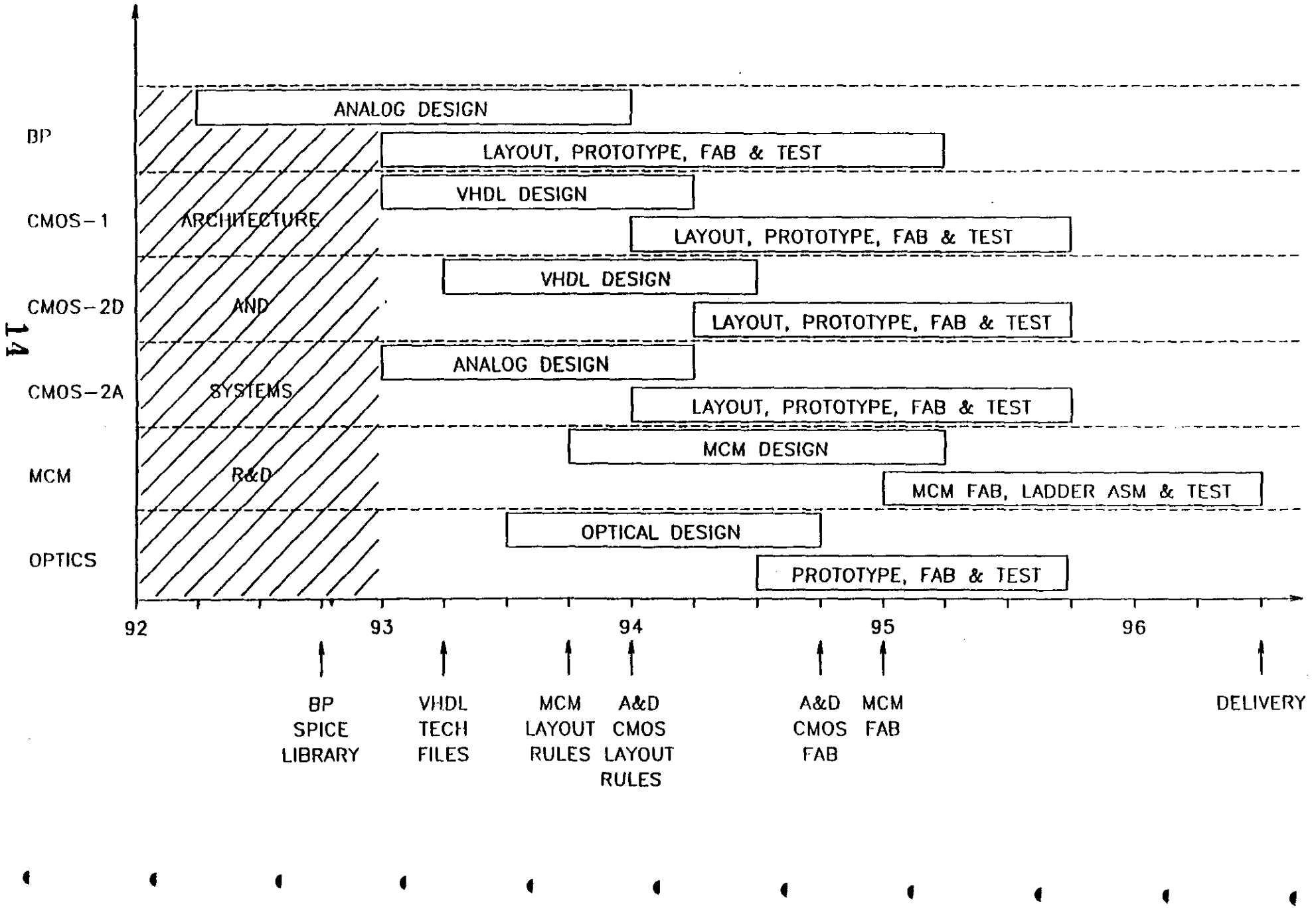
SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

(Note: These numbers were arrived at by using less than optimum labor quantities compared to the SSC9305 case. 2091 MCMs were used in the calculation.
This is the version given to Dave Lee on 2-11-93.)



SSC/GEM SILICON ELECTRONICS

MILESTONES



	SM 150		Tech 110			2/22/93
	Labor Cost			Procurement	Total	
	Man-Yr	Rate ($k)	Total ($k)		($k)	
Si-Tracker Electronics R&D Total	**5.75**		**713**	**169**	**870**	
Bipolar Development	**1**		**130**	**30**	**160**	
	0.5	150	75			
	0.5	110	55			
Purchase Order				30	30	Semi-custom foundry fabrication
CMOS-1 and 2D Development	**2.5**		**315**	**45**	**360**	
	1	150	150		150	
	1.5	110	165		165	
Purchase Oorder				45	45	VHDL design and layout service for CMOS-1, 2D
Fiber-Optics Development	**0.25**		**33**	**12**	**45**	
	0.125	150	19		19	
	0.125	110	14		14	
Purchase Order				12	12	Connectors, Transceivers hybrid
MCM proof-of-principle development	**0.75**		**83**	**43**	**126**	
		150				
	0.75	110	83		83	
Purchase Order				43	43	MCM order
CMOS-2A	**0.625**		**74**	**15**	**89**	
	0.125	150	19		19	
	0.5	110	55		55	
Purchase Order				15	15	Founry fabrication
Test Station and Cables	**0.625**		**79**	**12**	**91**	
	0.25	150	38		38	
	0.375	110	41		41	
Purchase Order				12	12	Control computer and software

Silicon Tracker Electronics R&D Budget for FY1994

2/22/93

	SM 150		Tech 110			
	Labor Cost			Procurement	Total	
	Man-Yr	Rate ($k)	Total ($k)		($k)	
SI-Tracker Electronics R&D Total	**3.75**		**610**	**313**	**911**	
Bipolar Proof-of-Principle Dev	**0.75**		**93**	**90**	**183**	
	0.25	150	38			
	0.5	110	55			
Purchase Order				90	90	*Foundry fabrication*
CMOS-1P-o-P Prototype Dev	**1.25**		**158**	**109**	**267**	
	0.5	150	75		75	
	0.75	110	83		83	
Purchase Oarder				109	109	Foundry fabrication of CMOS-1 and 2D
CMOS-2D P-o-P Prototype Dev	**0.75**		**93**		**93**	
	0.25	150	38		38	
	0.5	110	55		55	
Fiber-Optics Development	**0.375**		**46**	**12**	**58**	
	0.125	150	19		19	
	0.25	110	28		28	
Purchase Order				12	12	Connectors, Transceivers hybrid
MCM P-o-P Development	**0.875**		**101**	**50**	**151**	
	0.125	150	19		19	
	0.75	110	83		83	
Purchase Order				50	50	MCM fabrication
Cables	**0.375**		**46**	**35**	**81**	
	0.125	150	19		19	
	0.25	110	28		28	
Purchase Order				35	35	Aluminum Flex Cable Fabrication
Clock Distribution	**0.625**		**74**	**5**	**79**	
	0.125	150	19		19	
	0.5	110	55		55	
Purchase Order				5	5	Components

Si-Tracker Electronics Team at Los Alamos

Sangkoo Hahn:	Project Engineering, Bipolar, CMOS-2A
Brad Cooke:	Systems Engineering, Digital Architecture, MCM
Geoff Mills:	Requirements, Specifications, Integration, Test
Maureen Cafferty:	Bipolar, CMOS-2A, Cables
LeRoy Cope:	CMOS-2D, -1
Tony Rose:	CMOS-1, -2D
Gary Smith/Gary Richardson:	MCM, Hybrid
(Post Doctorate Associate):	Wafer/Chip Test, Beam Test Support
Ken Fuller:	Fiber Optics (consulting)

R&D Issues

Bipolar: Sangkoo Hahn, Maureen Cafferty

- Functional test of AT&T chips: FY93
- Beam test of AT&T chips for functional and radiation hardness: FY93
- Better simulation using realistic input charge waveforms and multiple strips: FY93
- Multi-channel (64 or 128) layout including cal injection and housekeeping: FY93,94
- Engineering proof-of-principle prototyping and testing: FY93
- Prototype fabrication, test: FY94

R&D Issues

CMOS-1, 2D: Brad Cooke, LeRoy Cope, Tony Rose

- Finalization of architecture: FY93
  (in collaboration with SSC Lab)
- Radiation hardness evaluation of various foundries: FY93
- VHDL-based design, synthesis, target layout, cost estimate: FY93
- FPGA implementation of functional blocks: FY93
- Engineering proof-of-principle prototyping and testing using FPGAs: FY93
- Prototype fabrication, test: FY94

R&D Issues

CMOS-2A: Maureen Cafferty, Sangkoo Hahn

- Prototype design: FY93
- Proof-of-principle prototyping support: FY93
- Fabrication and test of prototype: FY94

MCM: Brad Cooke, Gary Smith, Gary Richardson, Max Katko

- Cost estimate
- Proof-of-principle design, fab., possibly with SVX chip: FY93
- Prototype fabrication, test: FY94

R&D Issues

Fiber Optics: Brad Cooke, Ken Fuller

- Radiation hardness evaluation and testing: FY93
- Engineering proof-of-principle prototyping and testing using FPGAs: FY93
- Prototype fabrication, test: FY94

Cables: (TBD person)

- Low-Z design, layout, cost estimate: FY93
- Engineering proof-of-principle prototyping and testing using FPGAs: FY93

R&D Issues

Test Station, Slow Control: (Post-Doc Associate)

- Immediate need for AT&T chip tests
- Near-term use for proof-of-principle MCM tests
- Engineering proof-of-principle prototyping support: FY93

Clock Distribution: (TBD Person)

- GaAs-based design
- Proof-of-principle prototype support and testing: FY93
- Prototype development: FY94

Bipolar Chip

Design Baseline

- ~2.5M Channels of 50 u Pitch, Si-Strip Detectors
- 5 MRad (Si-equiv) Total Dose
- 18 cm and 16 cm Strip Lengths
- 25 ns charge integration time
- 150 ns double-pulse resolution
- 1.25 mW per channel
- Lowest achievable noise, time-walk

Bipolar Chip

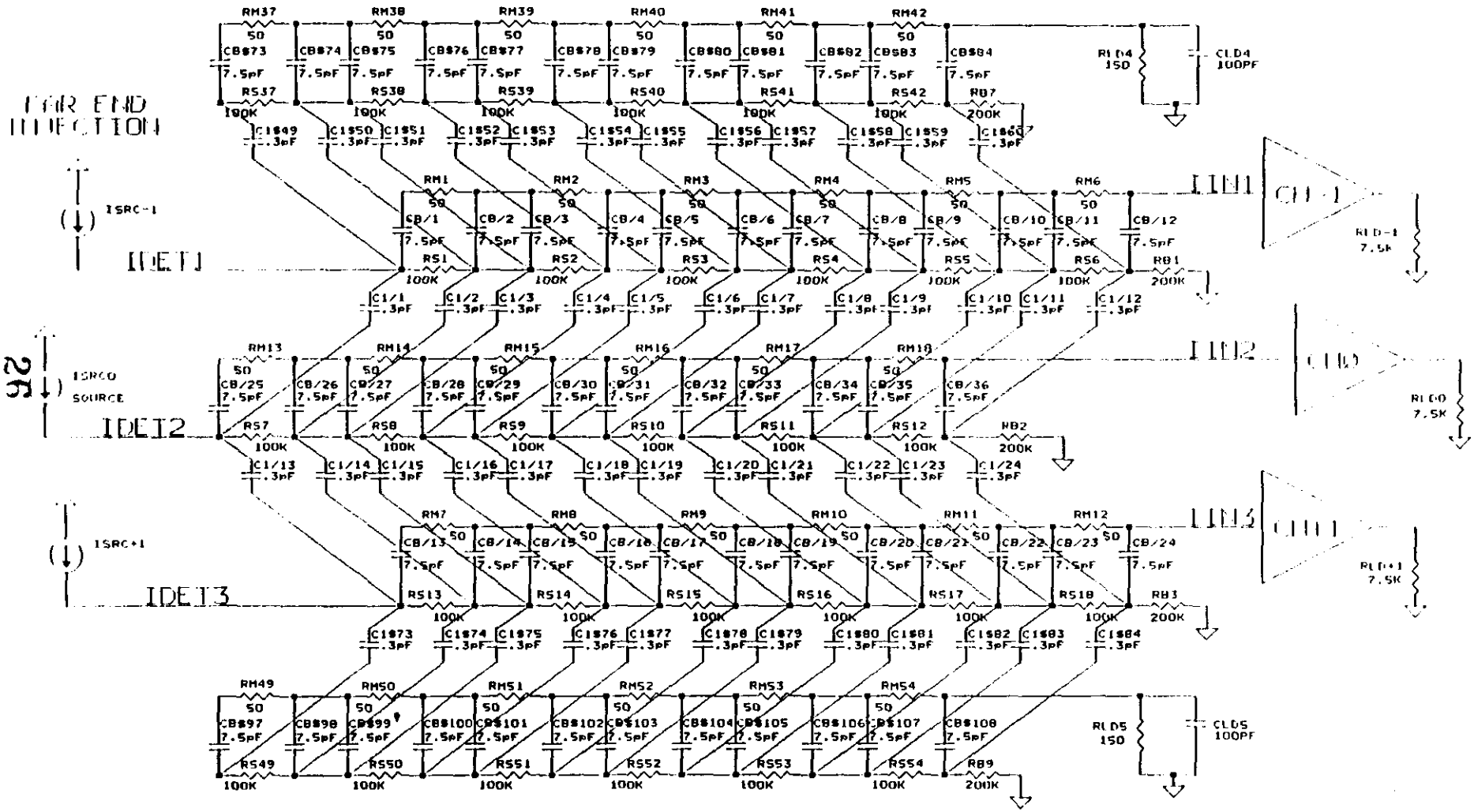
Development Status

- Single-Channel Amplifier Design Completed Based on AT&T-V series
- Proof-Reading of Layout Completed
- Design Release for Fab on Monday, February 22, '93
- 5-Channel/18 cm/Back-Annotated Circuit Simulation Started Incorporating Realistic Charge Waveforms from Oregon U (a set of ~200)

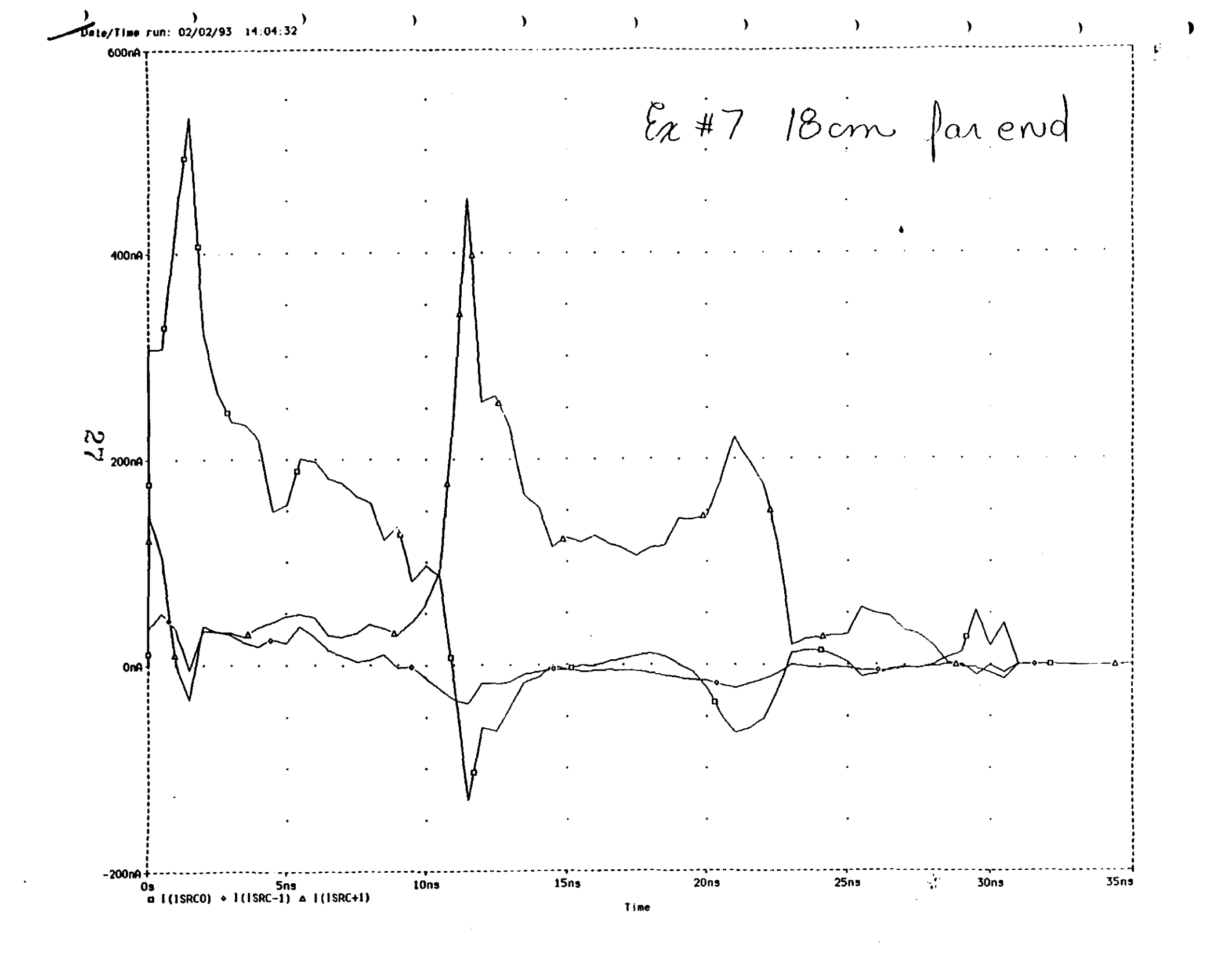
Bipolar Chip

Design Issues, Problems

18 cm Strip Length:	Noise Time Walk Power
Multiple Strip Effects:	1, 3 and 5 Strips for simulations
Realistic Charge Waveform:	Difference in Time-of-Arrival between channels
Radiation Hardness:	Harris, LBL, U Penn Data
Bias Stability:	Tough to achieve (State-of-Health Monitor: CMOS-2A)



REPRESENTATIVE OF ONE 6CM SECTION, 7.5PF DETECTOR CAPACITANCE
3--6CM SECTIONS USED FOR SIMULATIONS, 22.5PF DETECTOR CAPACITANCE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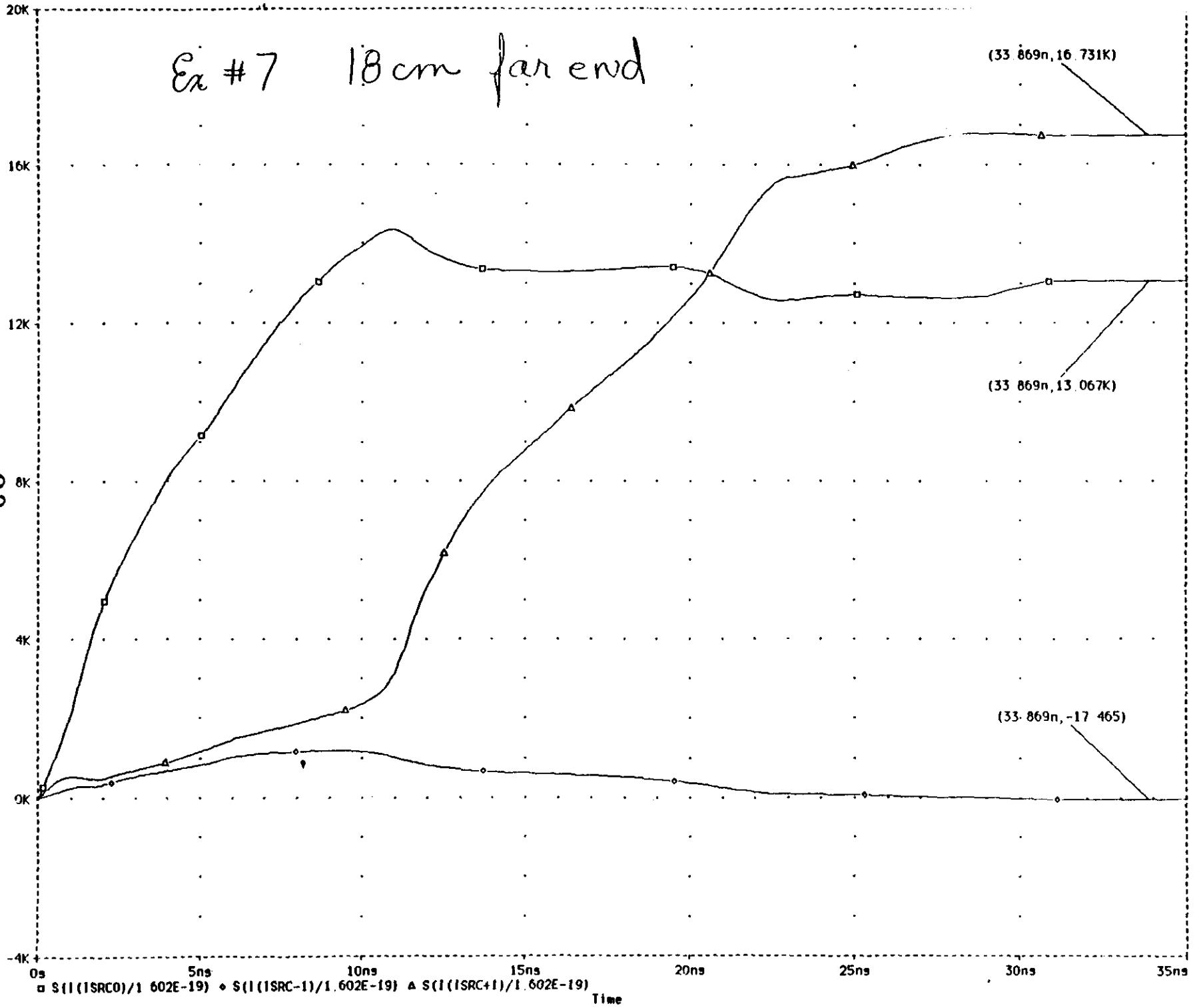
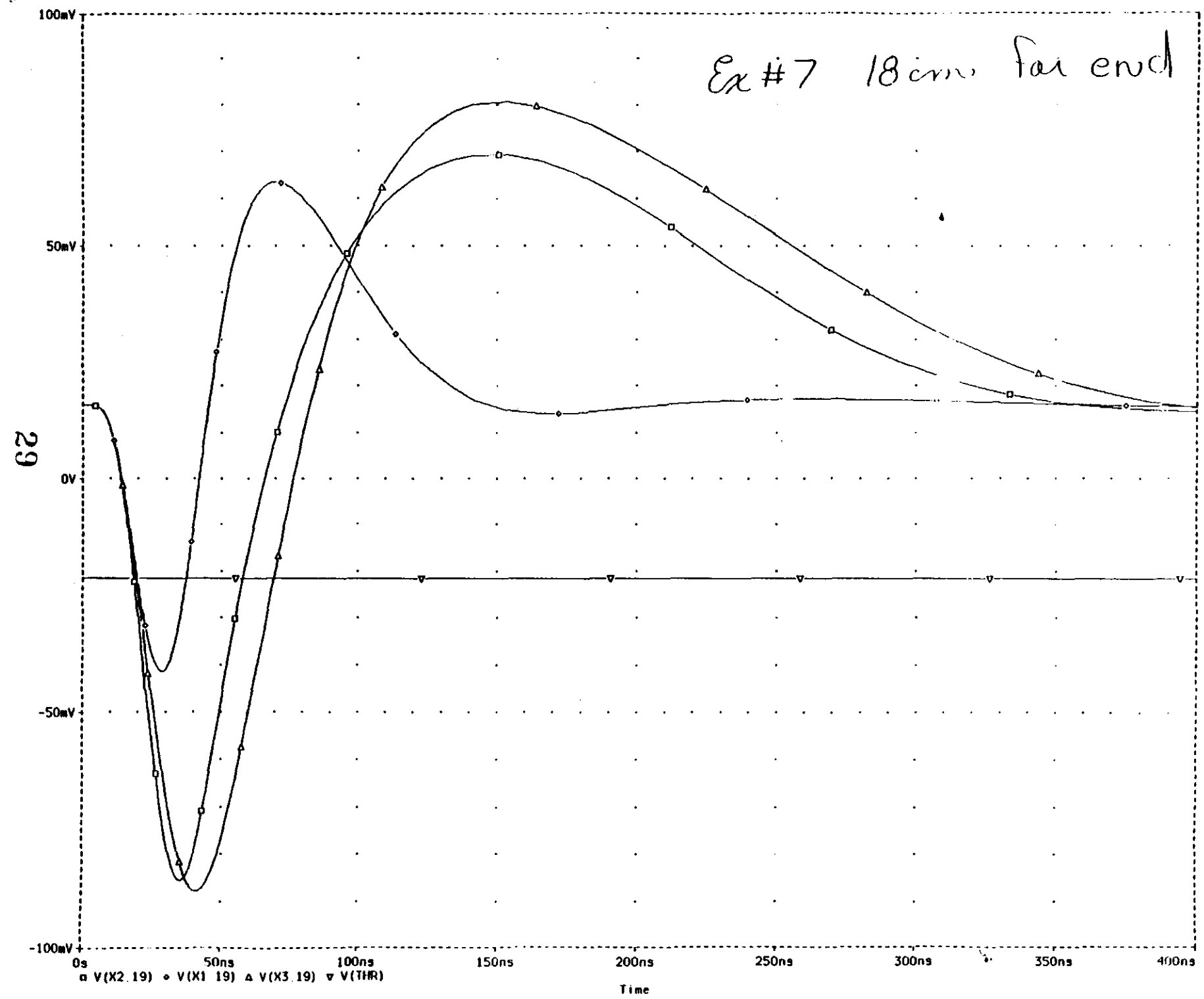
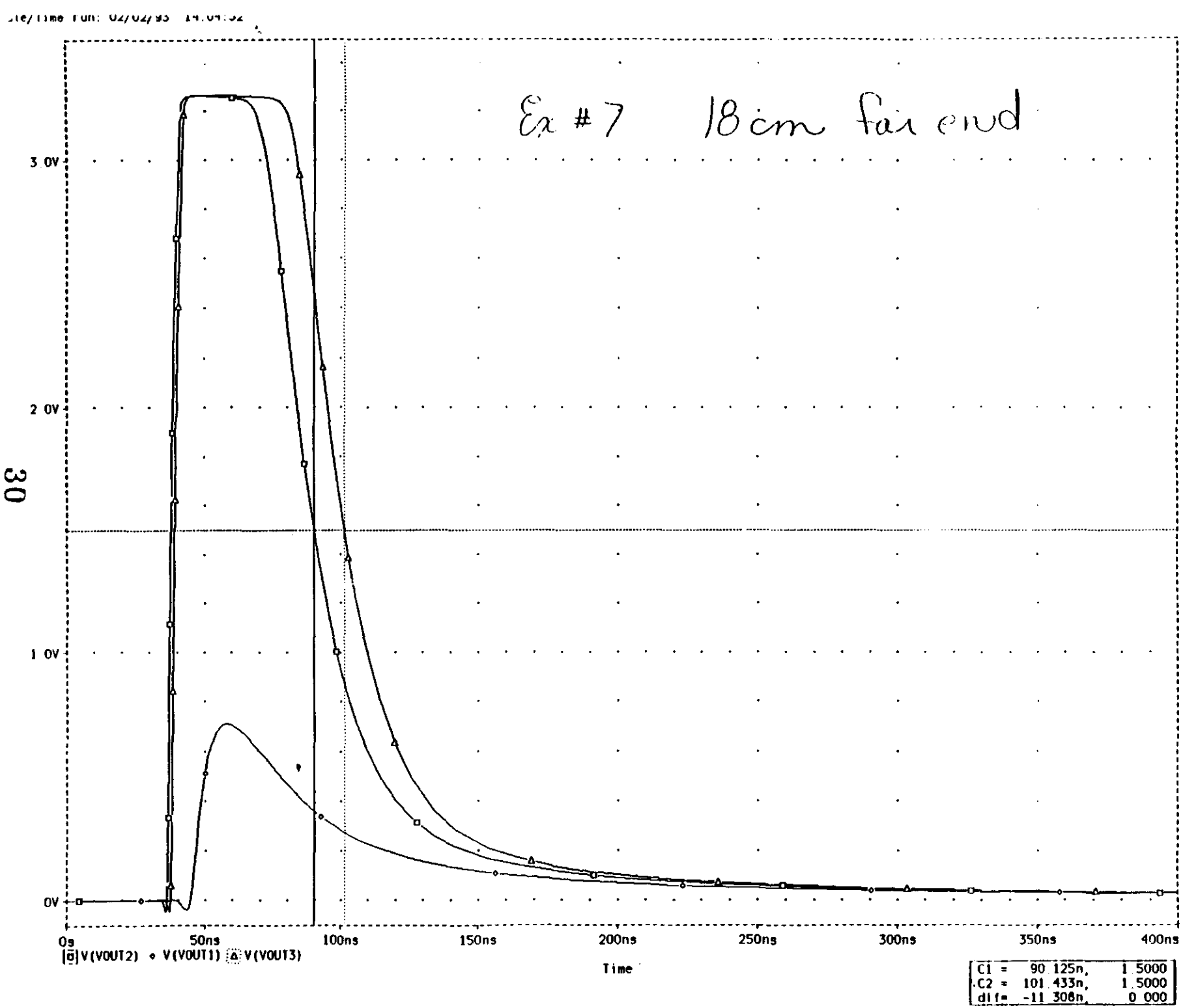
Ex #7 18cm far end
600nA
400nA
200nA
0nA
-200nA
I2
0s
5ns
10ns
15ns
20ns
25ns
30ns
35ns
Time
□ I(ISRC0) ◇ I(ISRC-1) △ I(ISRC+1)


Ex #7 18cm far end
(33.869n,16.731K)
(33.869n,13.067K)
(33.869n,-17.465)
20K
16K
12K
8K
4K
0K
-4K
0s
5ns
10ns
15ns
20ns
25ns
30ns
35ns
□ S(I(ISRC0)/1.602E-19) ◇ S(I(ISRC-1)/1.602E-19) △ S(I(ISRC+1)/1.602E-19)
Time


Ex #7 18cm far end
100mV
50mV
0V
-50mV
-100mV
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
Time
V(X2.19)
V(X1.19)
V(X3.19)
V(THR)


Ex #7 18cm far end
3.0V
2.0V
1.0V
0V
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
Time
V(VOUT2) V(VOUT1) V(VOUT3)
C1 = 90.125n, 1.5000
C2 = 101.433n, 1.5000
diff = -11.308n, 0.000

Bipolar Chip

Noise

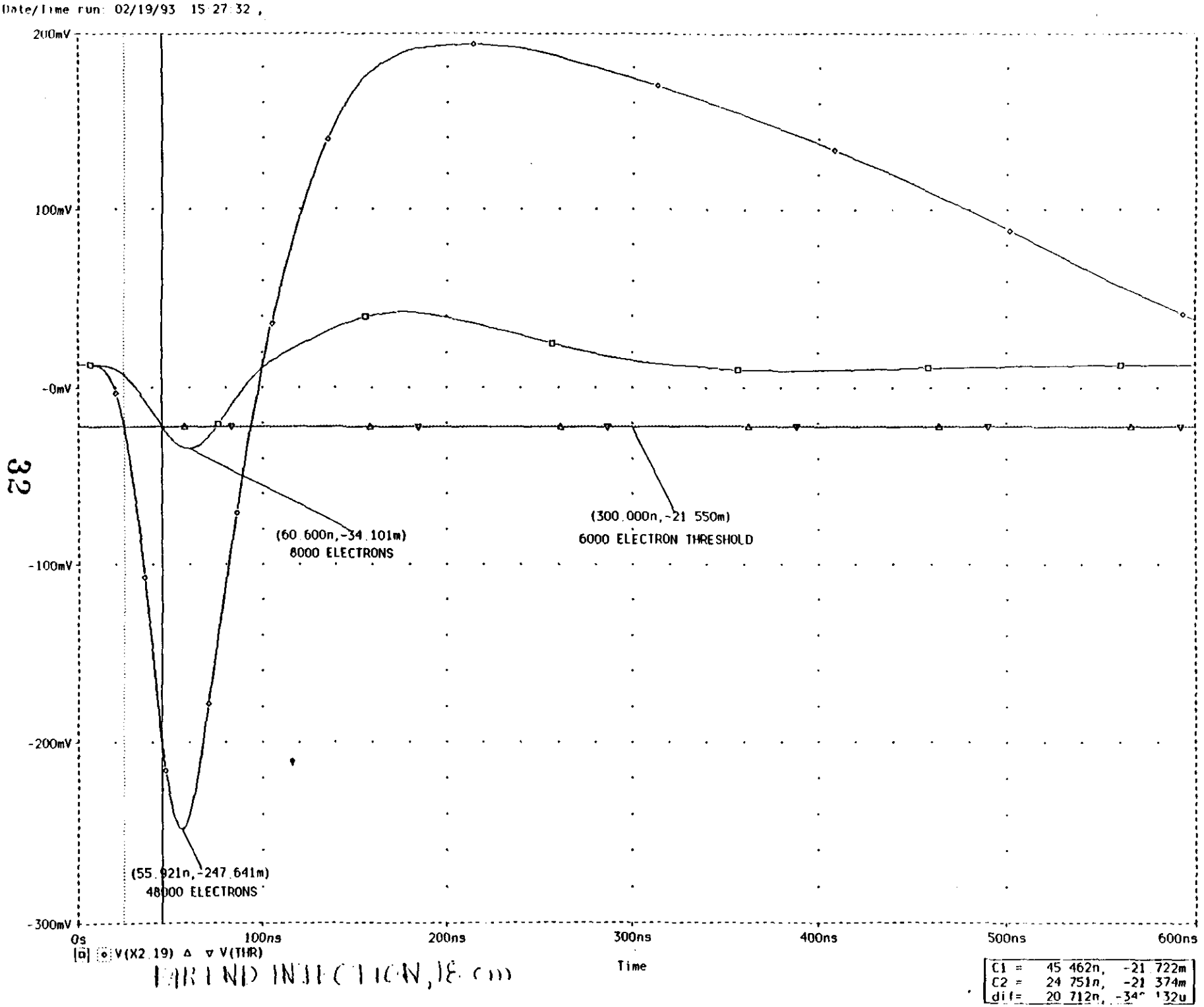
~2700 e^- RMS, near-end injection
~3000 e^- RMS, far-end injection

Interference, detector leakage current effects not considered
18 cm (1.2 pF, 50 ohms per cm), 5 strips

Time Walk

27 ns, near-end
34 ns, far-end

Leading edge trigger
8k (not 6k) to 48k electrons input range
6k equivalent threshold voltage (near-end injection charges)
5-strips



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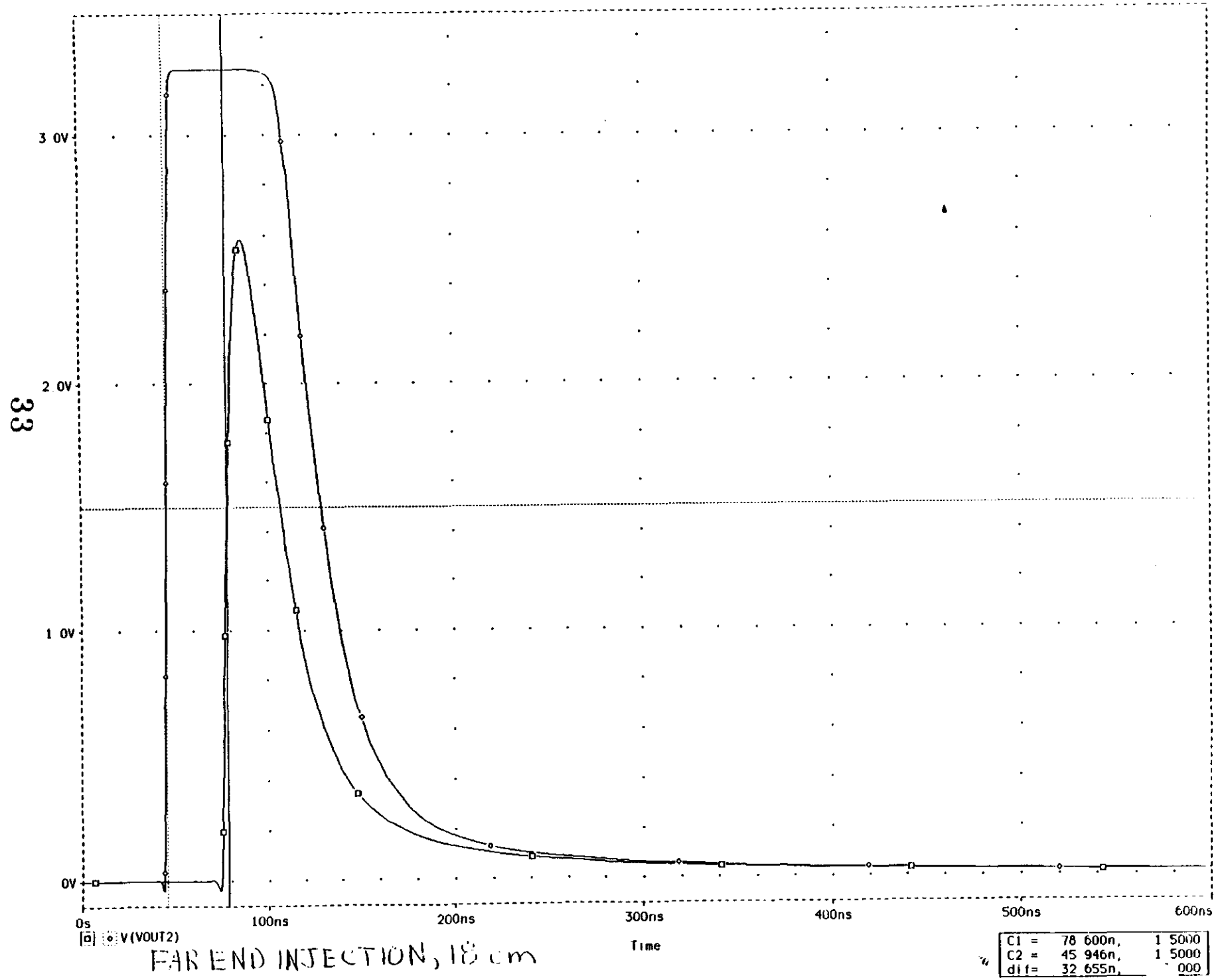


FAR END INJECTION, 18 cm

Bipolar

Time-of-Arrival Difference

~3 ns

Charge splitting between channels (boundary-crossing induced)
~10 ns difference in arrival of two wavefronts (Leading edge trigger preferred)

Radiation Hardness

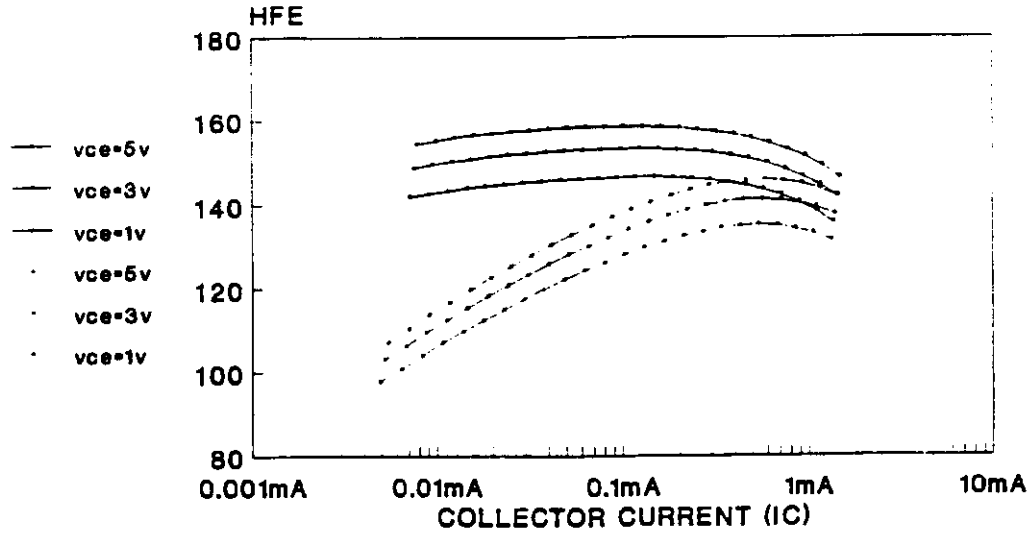
- LBL Data
  1/3 of original gain at Ic = 10uA for 1.2x10e14 protons/cm^2

- P-Base Resistance Change @1.2x10e14
  1 failure out of 8
  ~10 % reduction in resistance

HFE v.s. IC (NPN 1X)

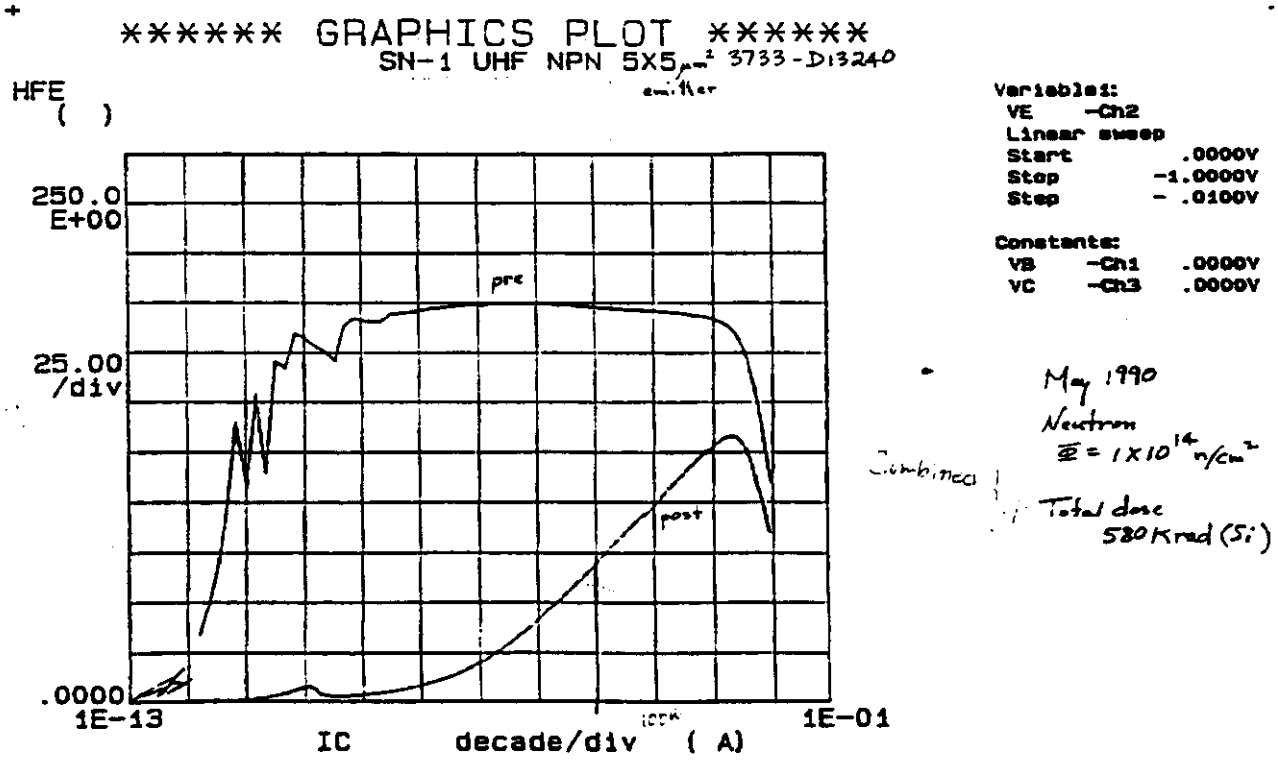
AT&T 2003 CHIP #1, TRANSISTOR #3

RADIATION LEVEL: 2M RAD (^{60}Cobalt)



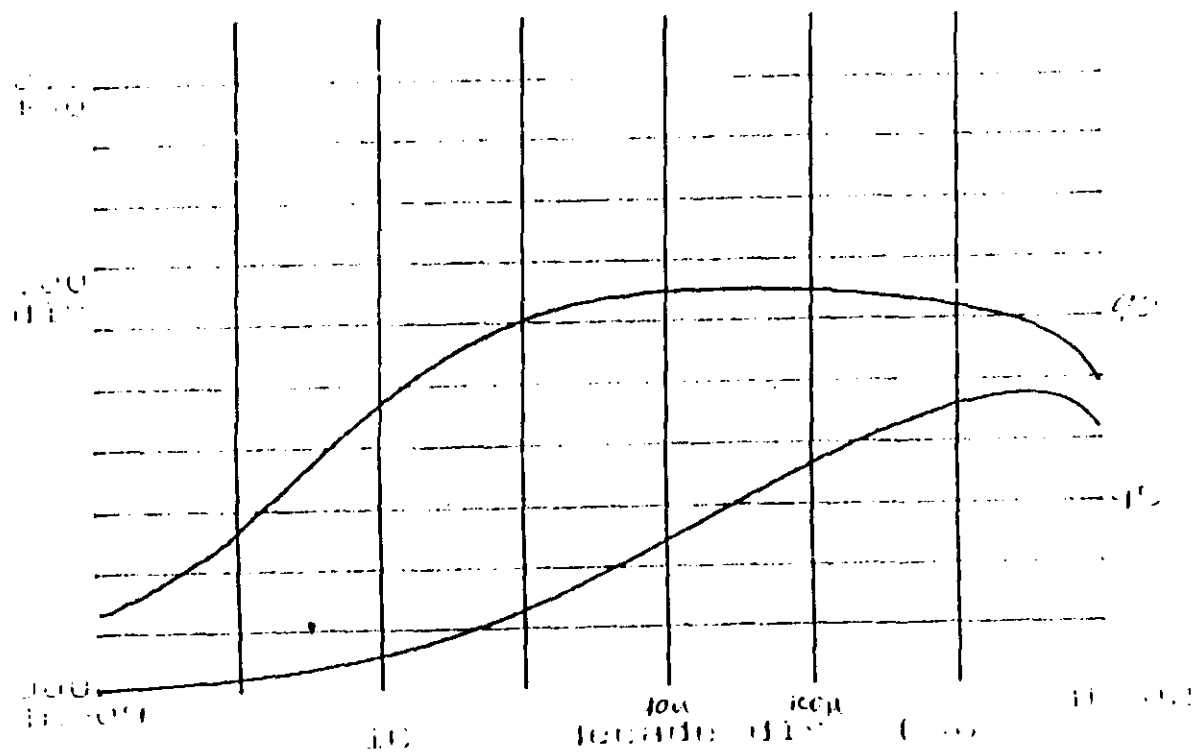
BLUE curve is BEFORE radiation
RED curve is AFTER radiation
VCE: collector & emitter volt difference

Pre- & Post-Radiation Gain vs. Ic
(One of a few AT&T Trs; Data from U. Penn)



Pre- & Post-Radiation Gain vs. Ic
(Harris Transistors)

AT&T CBIC-V npn NV231A01
$\Phi = 1.2 \times 10^{14}$ proton/cm^2



Variable1:
VE -Ch1
Linear sweep
Start .0000V
Stop -1.0000V
Step - .0050V

Constants:
VB -Ch2 .0000V
VCE -Ch3 .0000V

HFE ( ) = IC/IB

Bipolar

Bias Stability

Transistor gain change from radiaton damage (<50% for Ic=50uA, @EOL)

Toughest problem

Time-walk: worse

>10 mV DC shift of threshold @EOL

~20% drop in conversion gain @EOL (amplifier alone; worse at detector)

Need active monitoring for positive threshold setting

Bipolar

Conclusions

- Difficult to achieve noise performance better than 3000 e RMS (far-end)
- Hard to meet the (time walk) + (time difference) goal of <16ns
- EOL performance even worse
- *I can only strive for the best possible*

Future Direction

- Prototype design and layout for 64 or 128 channels with bias controls and charge injector
- Beam test of the AT&T chips for functions and radiation hardness
- More realistic simulations using charge waveforms from U Oregon and 5-strips

GEM SILICON-TRACKER READOUT ARCHITECTURE

SYSTEM OPTIMIZATION:

REQUIREMENTS

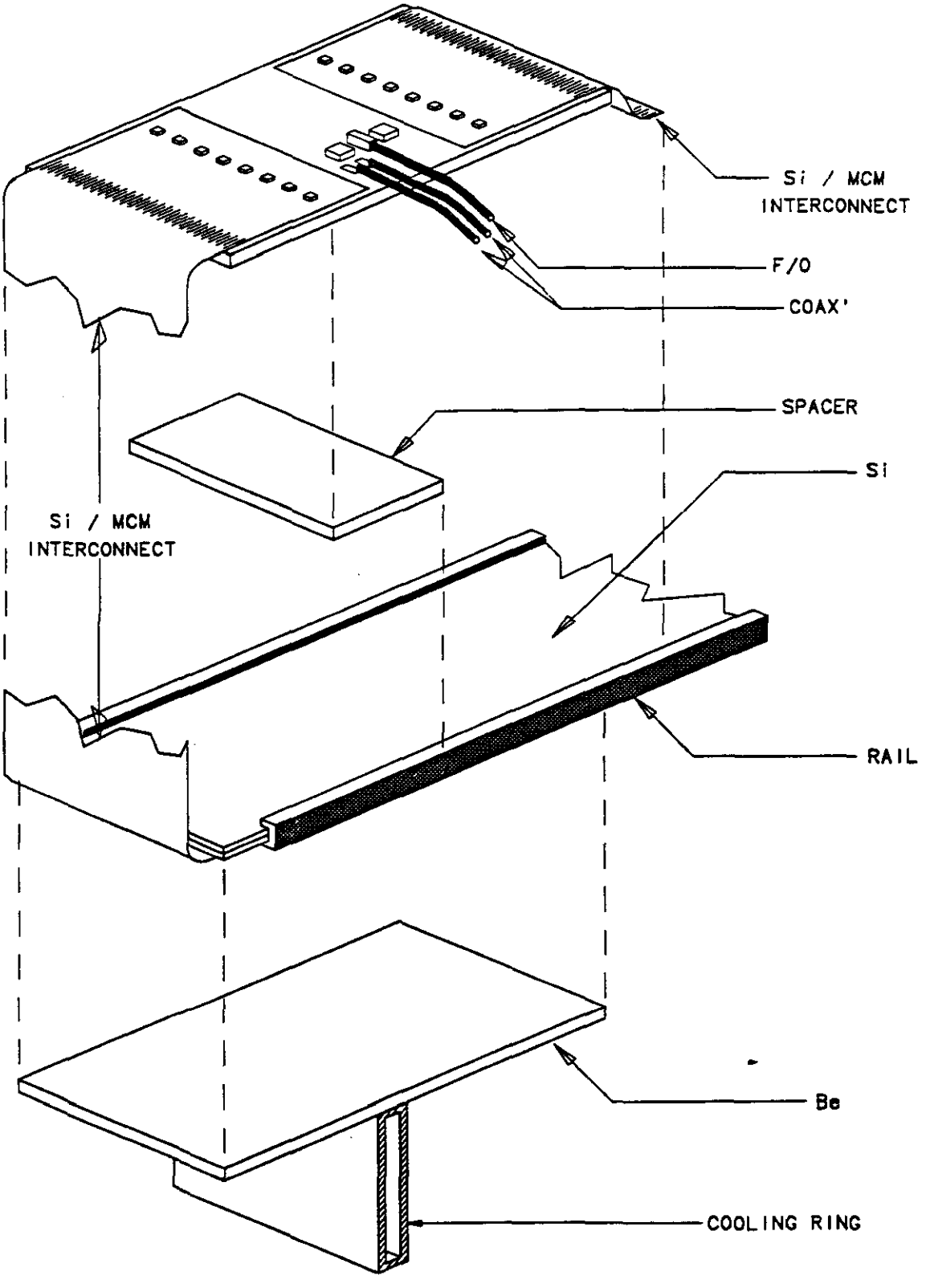
- COST
- SPEED
- RADIATION TOLERANCE
- POWER DISSIPATION
- RADIATION LENGTH
- LIFE CYCLE
- DELIVERY DATE

CONSTRAINTS

- BUILDABILITY
- TESTABILITY
- RELIABILITY
- MODULARITY

RESULTING SYSTEM FEATURES:

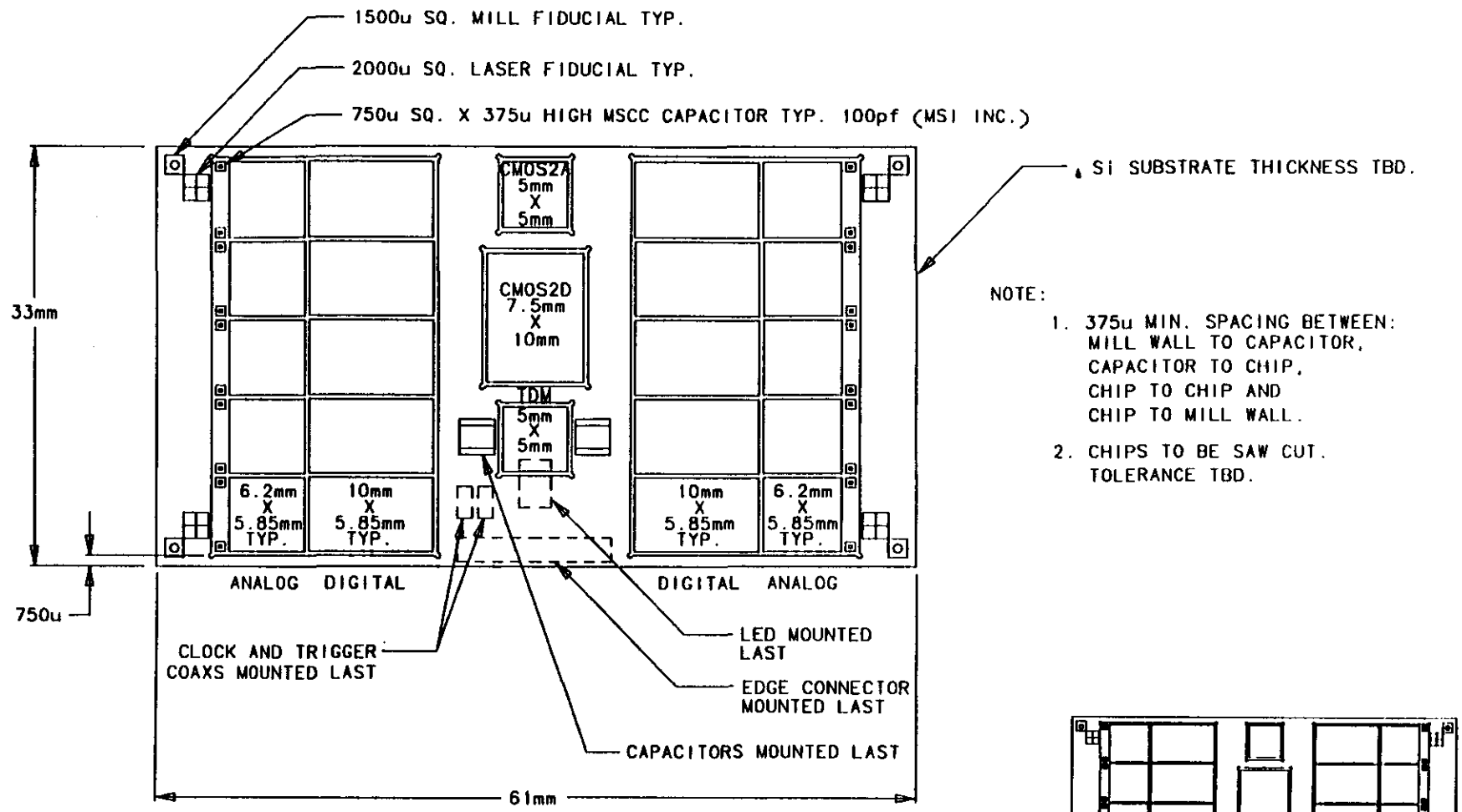
- EVENT DRIVEN CIRCUITRY (P_D PROPORTIONAL TO OCCUPANCY)
- RESET FREE ARCHITECTURE (SELF CORRECTING CIRCUITRY)
- PHASED CLOCK ARCHITECTURE (RELIABILITY)
- < 5% OF CMOS NEEDS TO RUN AT 60 MHz (YIELD, POWER & RELIABILITY)
- IN-SITU TESTABILITY AND CALIBRATION OF SYSTEM
- SELF-CONTAINED, SEGMENTED CIRCUITRY (RELIABILITY)
- RECONFIGURABLE (FO BW, TRIG. APERTURE, COMPRESSION, CIRCUIT BLOCKS)



GEM SILICON TRACKER. DETECTOR ASSEMBLY VER 11

B.C. / G.R. / M.J.K. MCDL, SST-11. GEML8

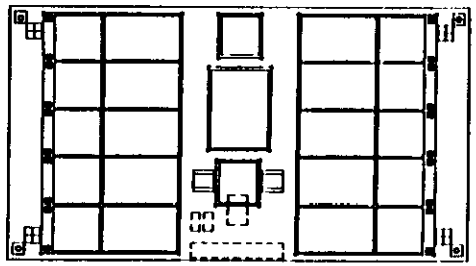
LOS ALAMOS NATIONAL LABORATORY, SST-11, MCDL, MSD448, PO BOX 1663, LOS ALAMOS, NM 87545. 2/9/92



APPROX. 2:1 SCALE

NOTE:

1. 375u MIN. SPACING BETWEEN:
   MILL WALL TO CAPACITOR,
   CAPACITOR TO CHIP,
   CHIP TO CHIP AND
   CHIP TO MILL WALL.
2. CHIPS TO BE SAW CUT.
   TOLERANCE TBD.

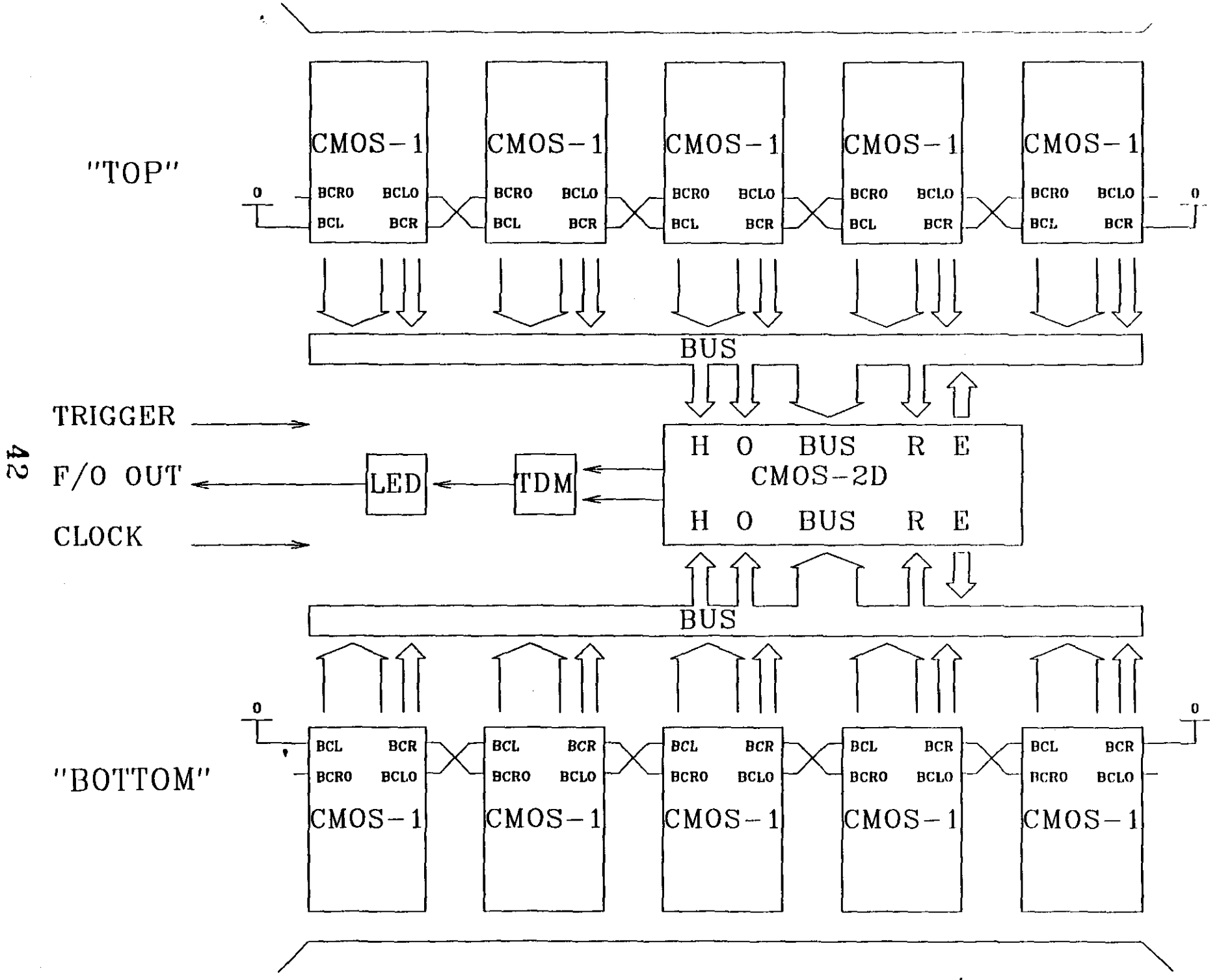


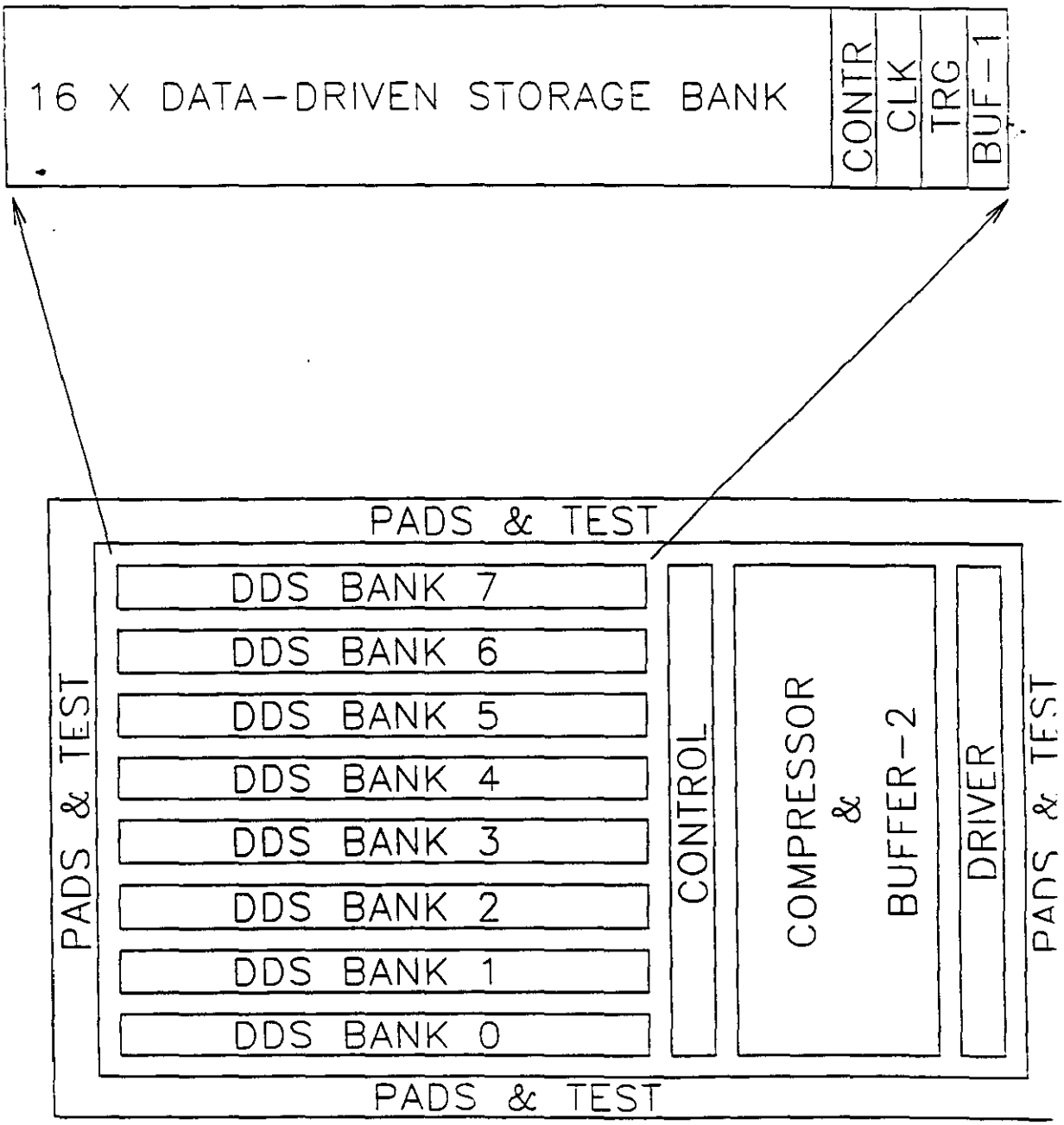
APPROX. 1:1 SCALE

GEM SILICON TRACKER. PRELIMINARY DESIGN LAYOUT.

B.C. / G.R. / M.J.K. MCDL, SST-11. GEML3.

LOS ALAMOS NATIONAL LABORATORY, SST-11, MCDL, MSD448, PO BOX 1663, LOS ALAMOS, NM 87545. 11/18/92


"TOP"
CMOS-1
BCRO
BCLO
BCL
BCR
0
BUS
TRIGGER
F/O OUT
CLOCK
LED
TDM
H O BUS R E
CMOS-2D
H O BUS R E
BUS
"BOTTOM"
640-CHANNEL ANALOG IN


16 X DATA-DRIVEN STORAGE BANK
CONTR
CLK
TRG
BUF-1
PADS & TEST
DDS BANK 7
DDS BANK 6
DDS BANK 5
DDS BANK 4
DDS BANK 3
DDS BANK 2
DDS BANK 1
DDS BANK 0
CONTROL
COMPRESSOR & BUFFER-2
DRIVER
PADS & TEST
PADS & TEST
PADS & TEST

DIGITAL STORAGE AND COMPRESSION

GENERAL SPECIFICATIONS:

- 60-62 MHz CLOCK

- RADIATION (PER YEAR) (LEE & WATERS)

  i) HADRONS: FLUX = 1.5 X 10^{13} / cm^2, 0.4 MRADS (Si) @ 10 cm
  ii) NEUTRONS (BACKSCATTER BORON-POLY): < 100 KeV FLUX = 3.3 x 10^{12} /cm^2,
  > 100 KeV FLUX = 1.9 X 10^{12} /cm^2
  iii) GAMMA: 0.1 - 0.5 MRADS

- SEU TOLERANT (CIRCUIT), LATCH-UP RESISTANT (DEVICE)

- NUMBER OF ASSEMBLIES (1/2 LADDERS) = ~ 2000

- STRIP-DETECTORS/ASSEMBLY/SIDE = 640/3.3 cm (PITCH = 50 microns)

- MEAN OCCUPANCY/ASSEMBLY/SIDE/16 ns = 0.2% @ 10^{33}, 2% @ 10^{34} (r=10 cm)

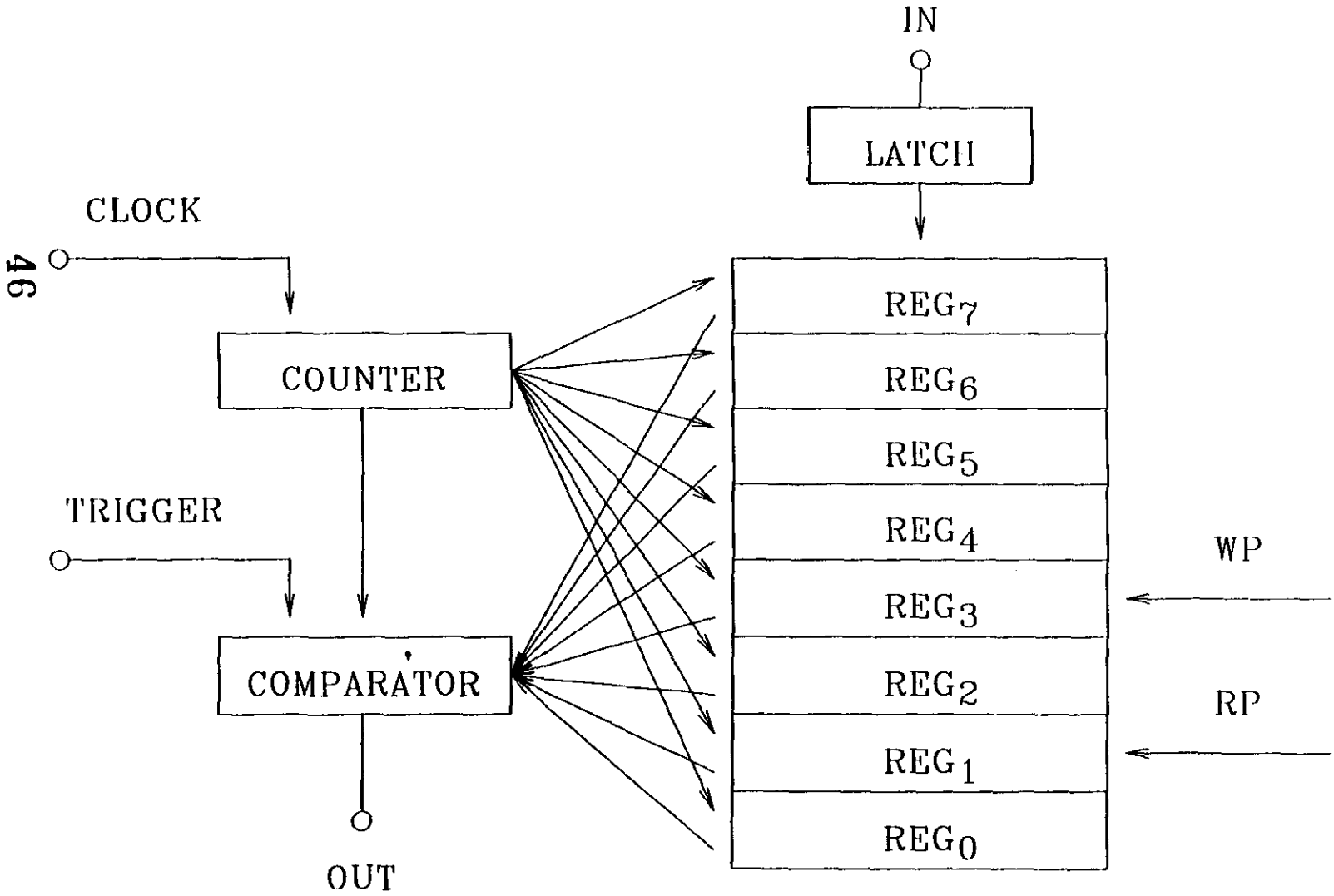
- MAXIMUM TRIGGER RATE (LEVEL 1) = 100 KHz

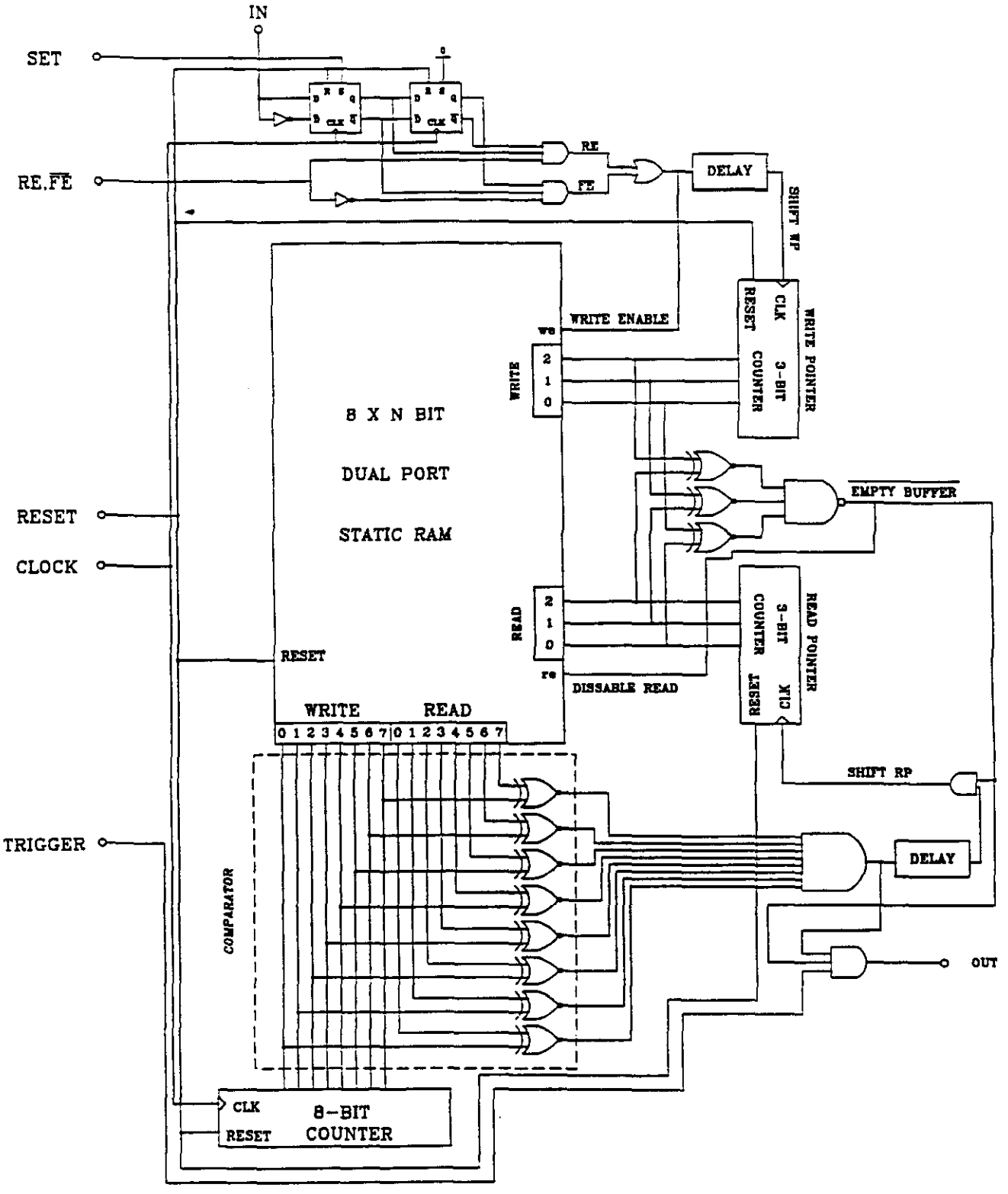
DIGITAL STORAGE AND COMPRESSION

FEATURES:

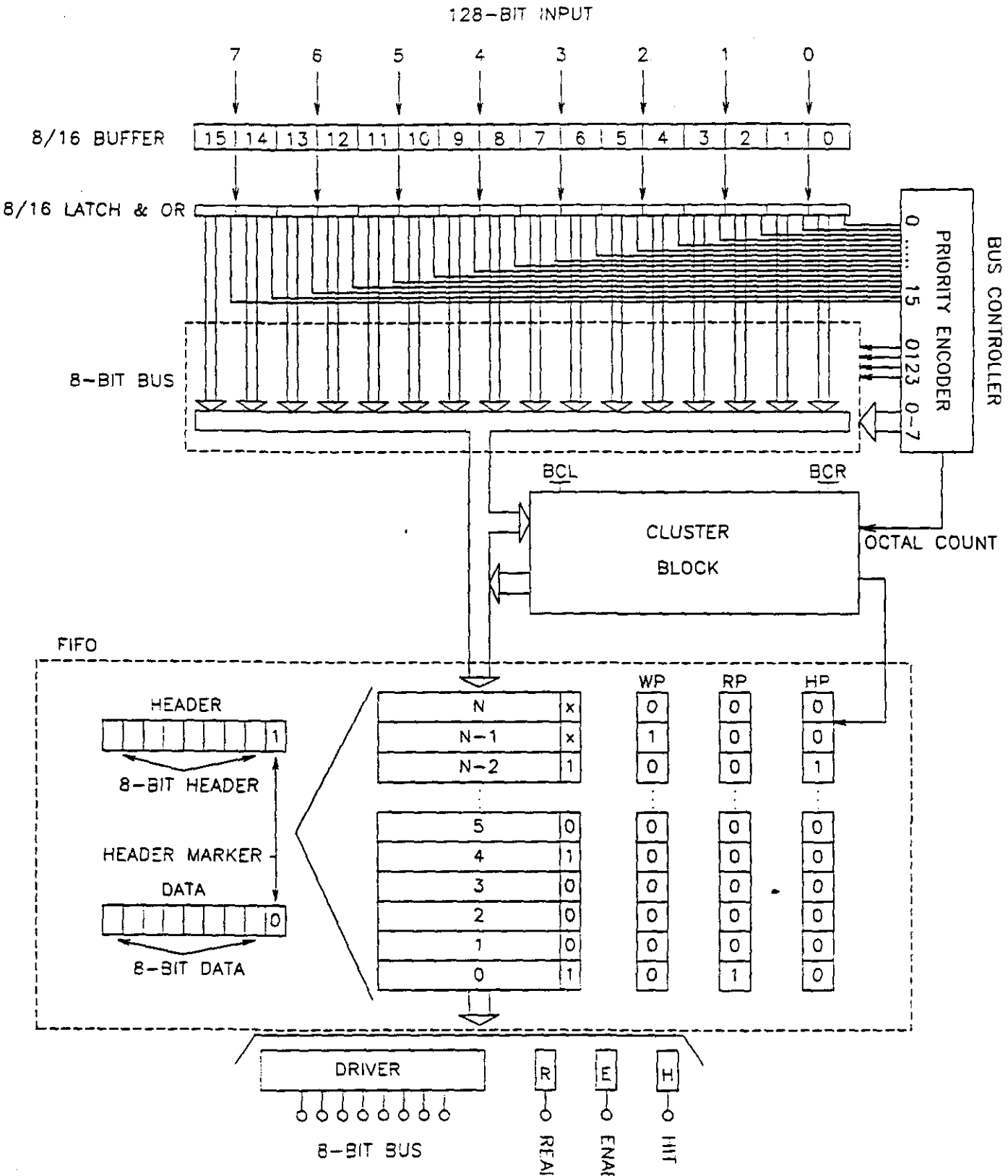
- LEVEL 1 TRIGGER (PROGRAMMABLE LATENCY 128-256 X CLOCK)
- EDGE TRIGGERED LATCH -- RISING OR FALLING EDGE (RELIABILITY)
- PROGRAMMABLE TRIGGER APERTURE (0 - 4 X CLOCK)
- CONSECUTIVE TRIGGERS = 2 - 4
- CONCURRENT POINTER DATA DRIVEN STORAGE (> 95% EFFICIENCY @ 1% OCCUPANCY, N_σ=3.0)
- MEAN CLUSTERING or 8/16 COMPRESSION (25X - 5X EFFICIENCY FOR 0.1% - 1% Occ.)
- MEAN COMPRESSION DELAY: CLUSTER = 1 μs, 8/16 =0.5 μs
- FO LINK BANDWIDTH = 60 MHz PER 1280 CHANNELS
- RESET FREE ARCHITECTURE
- PHASED CLOCK ARCHITECTURE
- SEGMENTED CIRCUITRY

CONCURRENT POINTER TRACKING DATA DRIVEN STORAGE

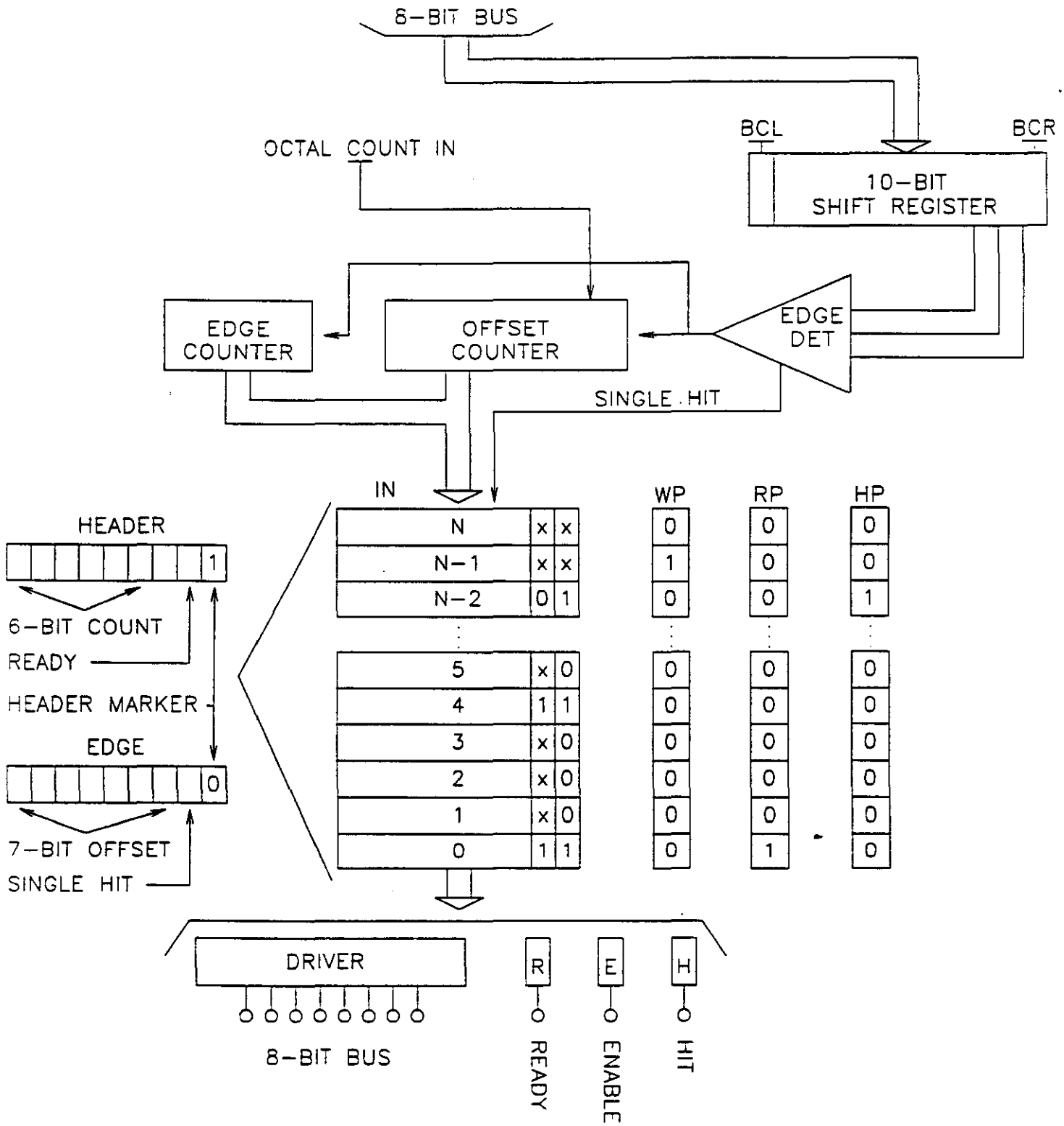


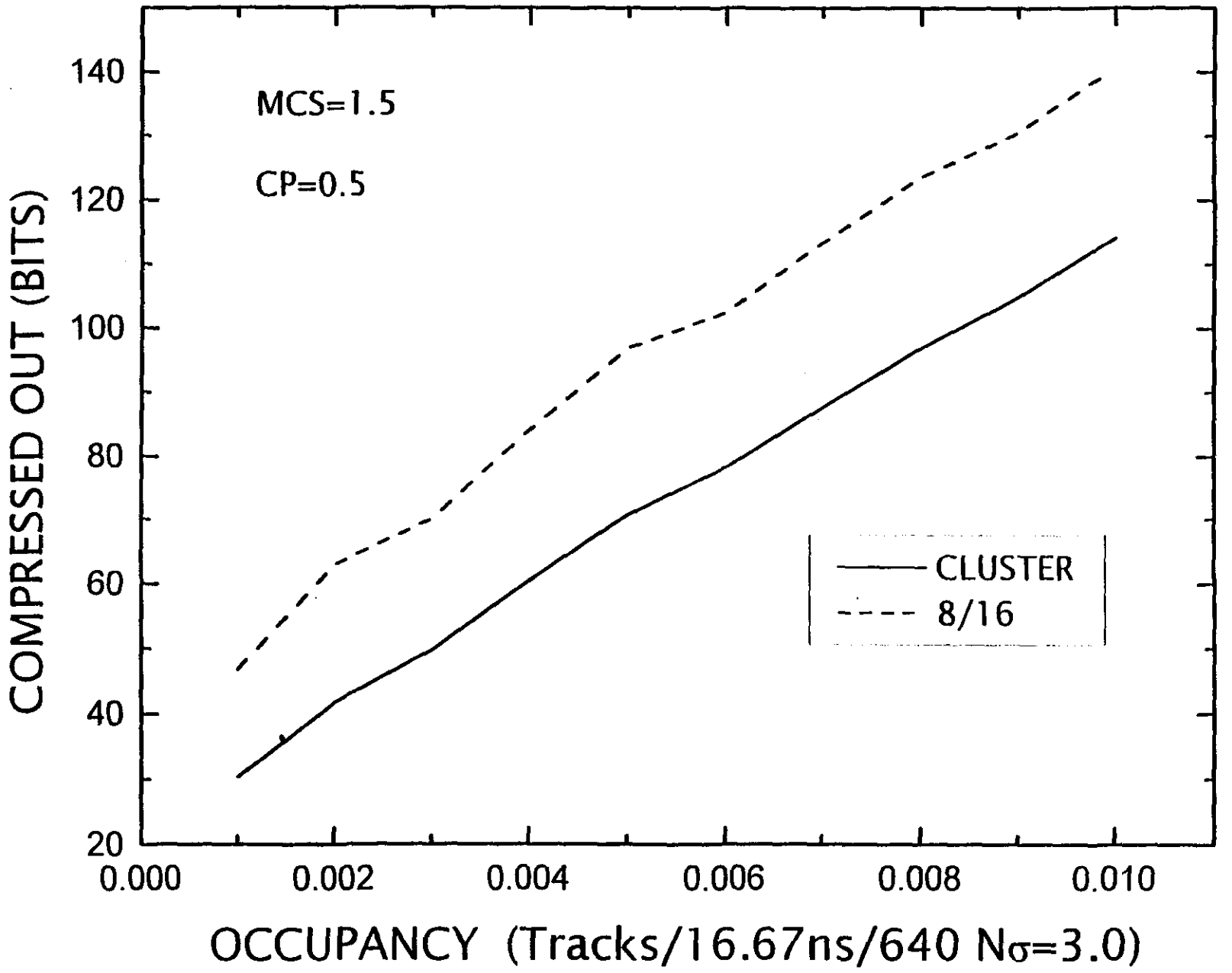

IN
SET
RE.FE
RESET
CLOCK
TRIGGER
RE
FE
DELAY
SHIFT WP
WRITE ENABLE
we
WRITE
2
1
0
CLK
RESET
3-BIT
COUNTER
WRITE POINTER
8 X N BIT
DUAL PORT
STATIC RAM
EMPTY BUFFER
READ
2
1
0
re
DISSABLE READ
RESET
WRITE
READ
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
READ POINTER
SHIFT RP
DELAY
COMPARATOR
OUT
CLK
RESET
8-BIT
COUNTER

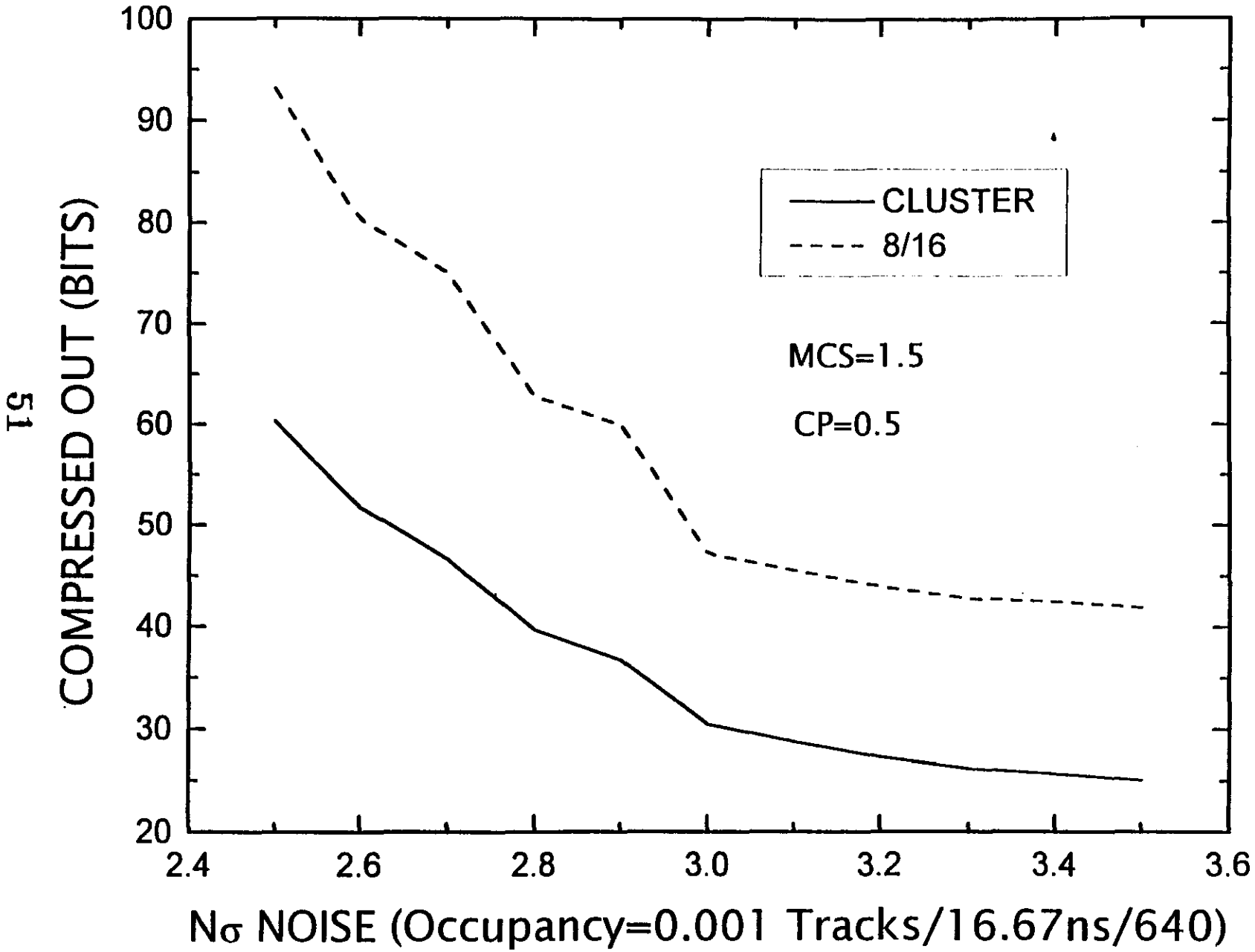
HYBRID 8_16/CLUSTER COMPRESSOR ARCHITECTURE



CLUSTER COMPRESSION BLOCK




MCS=1.5
CP=0.5
CLUSTER
8/16
COMPRESSED OUT (BITS)
OCCUPANCY (Tracks/16.67ns/640 Nσ=3.0)
20
40
60
80
100
120
140
0.000
0.002
0.004
0.006
0.008
0.010


100
90
80
70
60
50
40
30
20
COMPRESSED OUT (BITS)
CLUSTER
8/16
MCS=1.5
CP=0.5
2.4
2.6
2.8
3.0
3.2
3.4
3.6
Nσ NOISE (Occupancy=0.001 Tracks/16.67ns/640)

HDI MULTICHIP TECHNOLOGY

* PERFORMANCE - HIGHEST ELECTRICAL PERFORMANCE DUE TO SHORTEST INTERCONNECT DISTANCE, CONTROLLED IMPEDANCE.

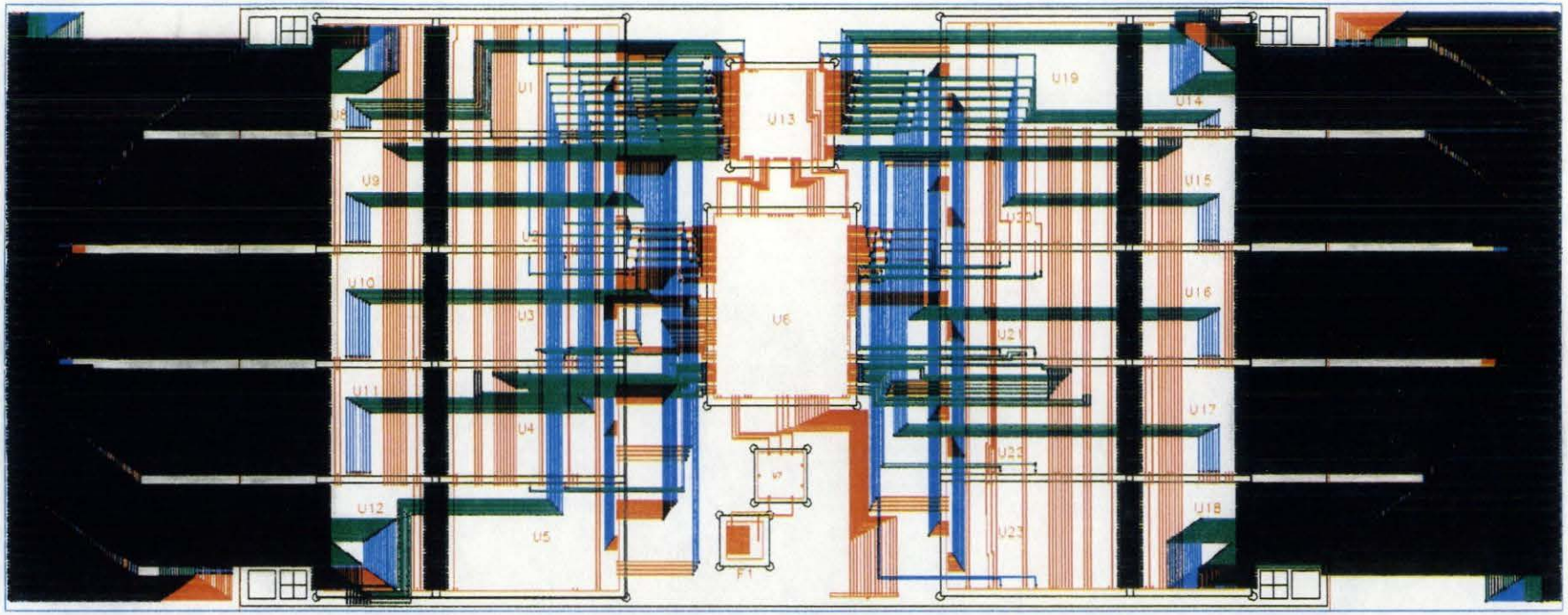
* THERMAL PERFORMANCE - PLACEMENT OF CHIPS UNDER THE POLYMER INTERCONNECT MINIMIZES THE THERMAL PATH AND SIMPLIFIES PACKAGING ISSUES.

* HIGH DENSITY - A CHIP PACKING DENSITY OF 90% CAN BE ACHIEVED, MINIMIZING SUBSTRATE SIZE. CIRCUITY ROUTING DENSITY, 50 MICRON PITCH.

* RELIABILITY -PASSED ALL MIL-STD-883 ENVIRONMENTAL, MECHANICAL AND RADIATION HARDENED SCREENS FOR CLASS "S" REQUIREMENTS.

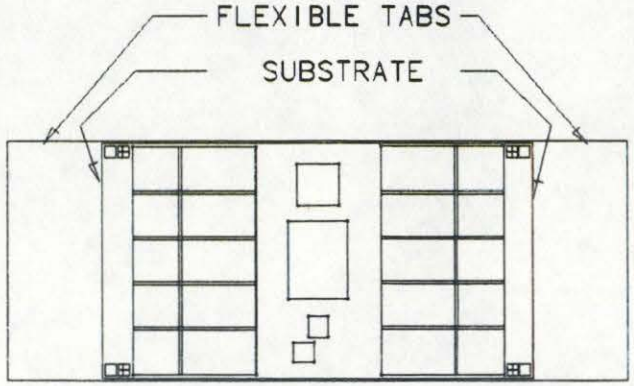
* REPAIRABILITY - MALFUNCTIONING CHIPS CAN BE REPLACED BY REMOVING THE HDI OVERLAY AND REPROCESSING.

* HIGH YIELD - THE LASER VIA AND PHOTO PATTERNING PROCESSES PROVIDE HIGH YIELDS.



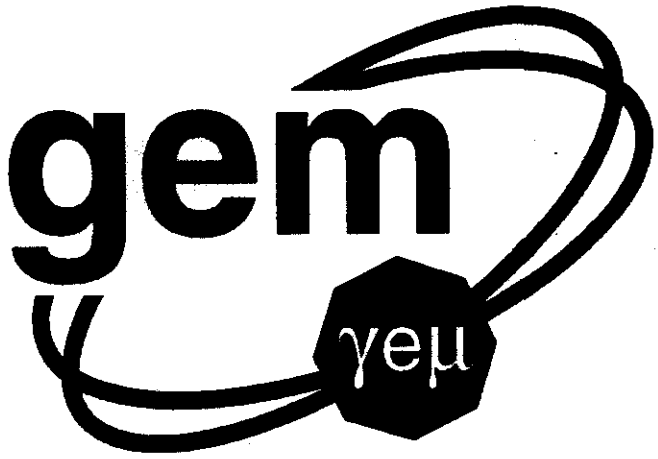
SUP-1 SUBSTRATE
61MM X 33MM

GEM HDI MCM



SCALE 1:1
SIZE: 61MM X 33MM

LOS ALAMOS NATIONAL LABORATORY, SST-11, MCDL, MSD448, P O BOX 1663, LOS ALAMOS, NM 87544 2/1/93



Presentation by:

P. O'Connor

MONOLITHIC FRONT END ICs FOR GEM IPC AND CSC

P. O'CONNOR BNL

IPC PAD PREAMP

J. Musser - I.U.
C.L. Britton } ORNL
L. Clonts }
T. Johnson Harris Semi.

CSC CATHODE READOUT IC

V. Polychronakos } BNL
M. Atiya }
V. Grachov PNPI
D. Skrzyniarz SUNY-SB Physics
M. Green } SUNY-SB E.E.
P. Walker }

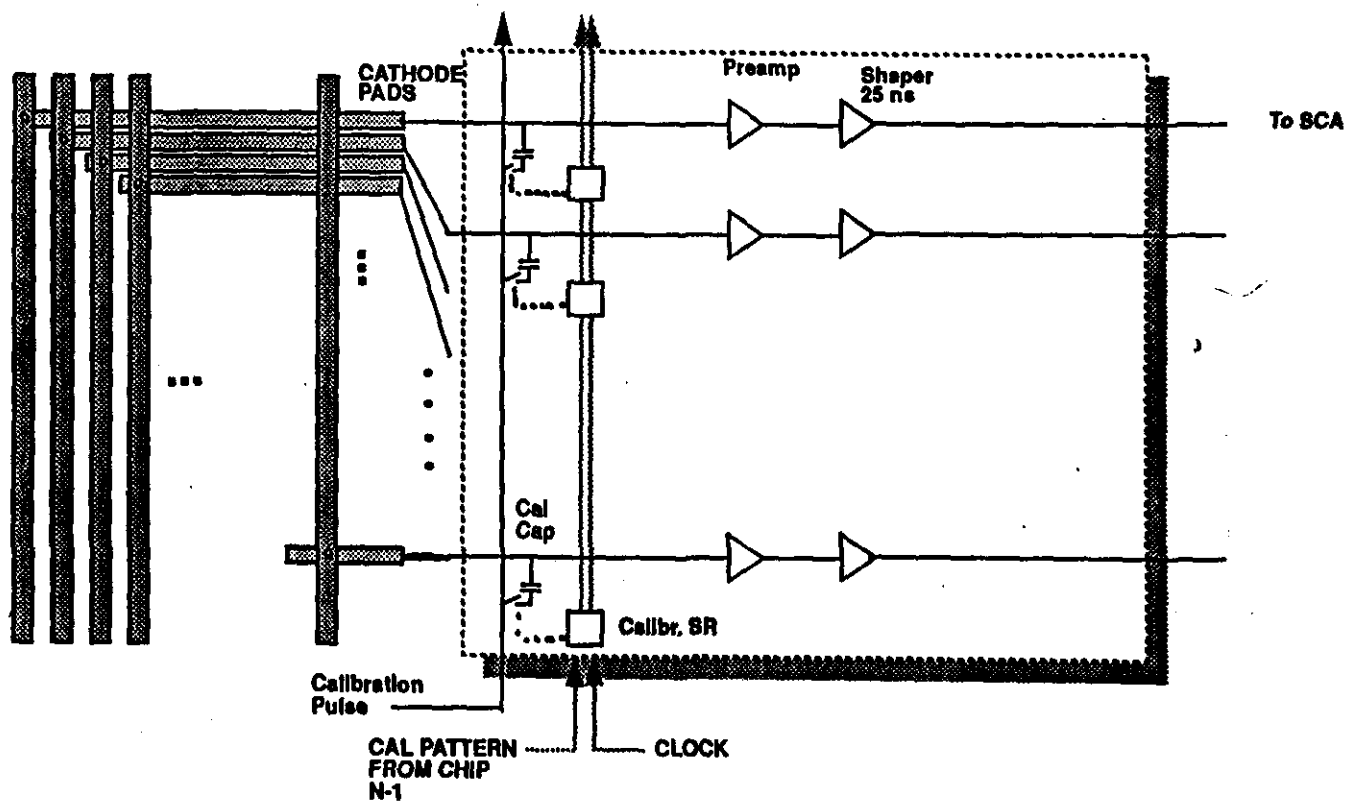
CSC ANODE PREAMP/SHAPER/DISCRIMINATOR

N. Bondar PNPI

ALL

V. Radeka, S. Rescia, D. Stephani, L. Rogers
B. Yu, G. Smith
J. Harder, R. Squires

Readout Chain for GEM IPC



IPC PREAMP/SHAPER DESIGN REQUIREMENTS

Input Capacitance (pad + readout line): 10 - 50 pF

Most probable Q_{pad}: ~ 30 fC (200,000 e^-)

Must produce voltage pulse into analog memory

Allow position interpolation accuracy of 2% of pad pitch

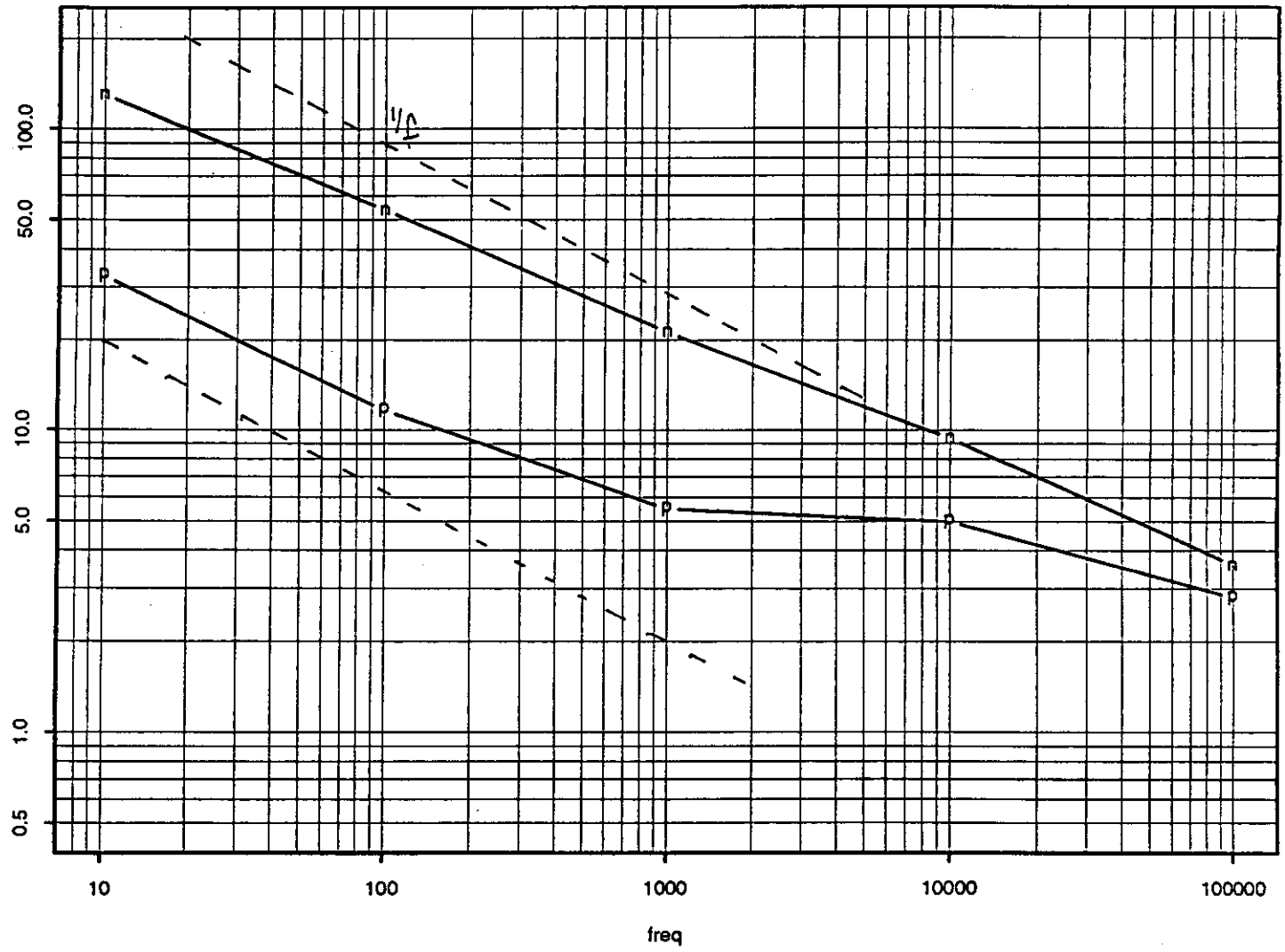
Keep occupancy within 2%

⇒ SPECIFICATIONS

1. Noise : < 2000 e^- r.m.s. equivalent input noise charge (ENC)
   [1000 desirable]
2. Voltage output: semi-Gaussian pulse with peaking time around 30 nsec.
3. Charge-to-voltage gain of about 10
4. Linear response to 150 fC input charge.
5. Survive 2 Mrad ionizing and $2 \cdot 10^{14}$ n/cm² radiation dose over several years of operation at the SSC.

10/30/92

IC5 MOSFET Noise vs. Frequency -- Id ~ 4mA



g_m ~ 24mS

K_f ~ 5.1×10^{-24} J nmos

3.2×10^{-25} J pmos

Noise

For $\sigma_x / x = .01$, need $\sigma_Q/Q = .006$

$\sigma_Q = (.006)$ (30 fC) = 0.17 fC = 1100 e^-

IPC:

For 1000 e^-, C_D= 40 pF,

$C_{FET} + C_{stray}$ = 15 pF, t_m = 25 ns (CR-RC^4)

$e_n < 0.46$ nV/$\sqrt{Hz}$

($R_{eq} < 15\ \Omega$)

Input device $g_m > 52$ ms (FET), 39 mS (BJT)

$I_C > 1.0$ mA (BJT) ... but need to consider parallel noise of ~ 10 uA I_B

I_d x W/L > 27A (I) for MOSFET in strong inversion

PLUS

30% - 50% from preamp other devices

noise of Rg, Rsub

2nd stage noise

CSC:

C_D = 120 pF

t_m = 500 ns

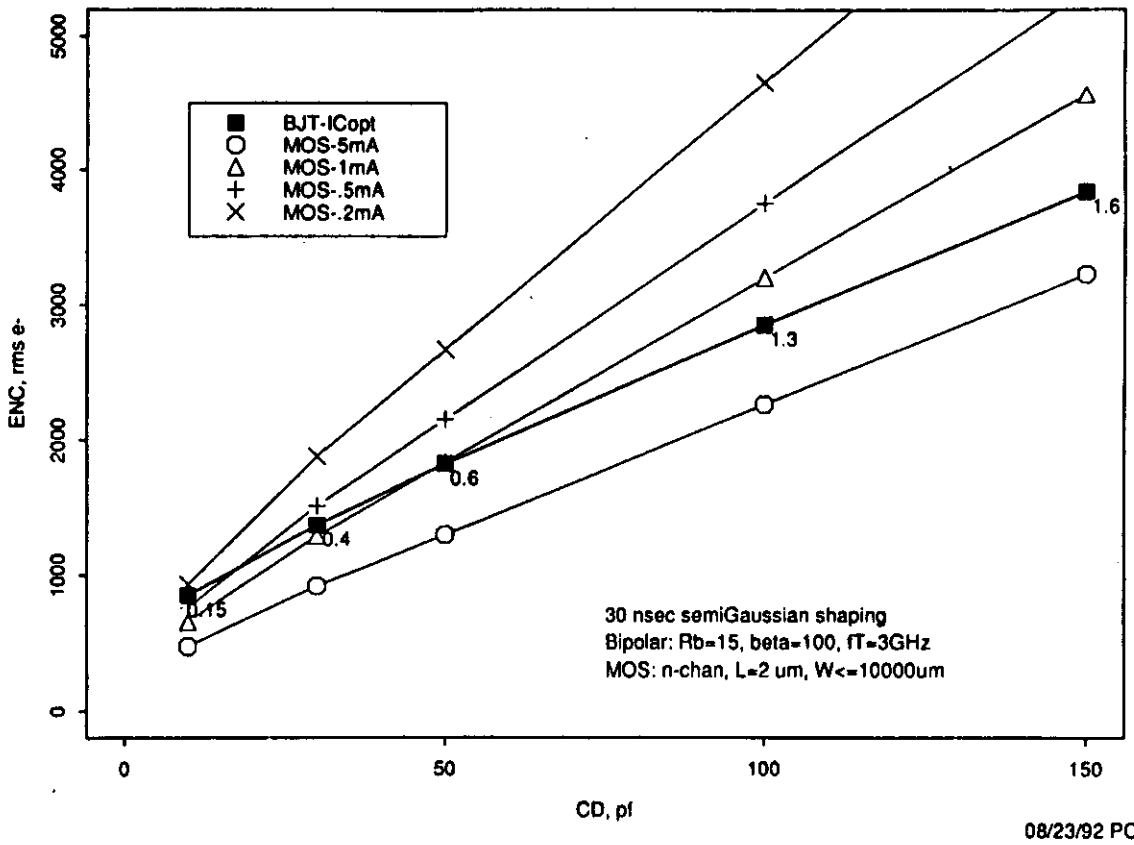
$e_n < 0.87$ nV/$\sqrt{Hz}$

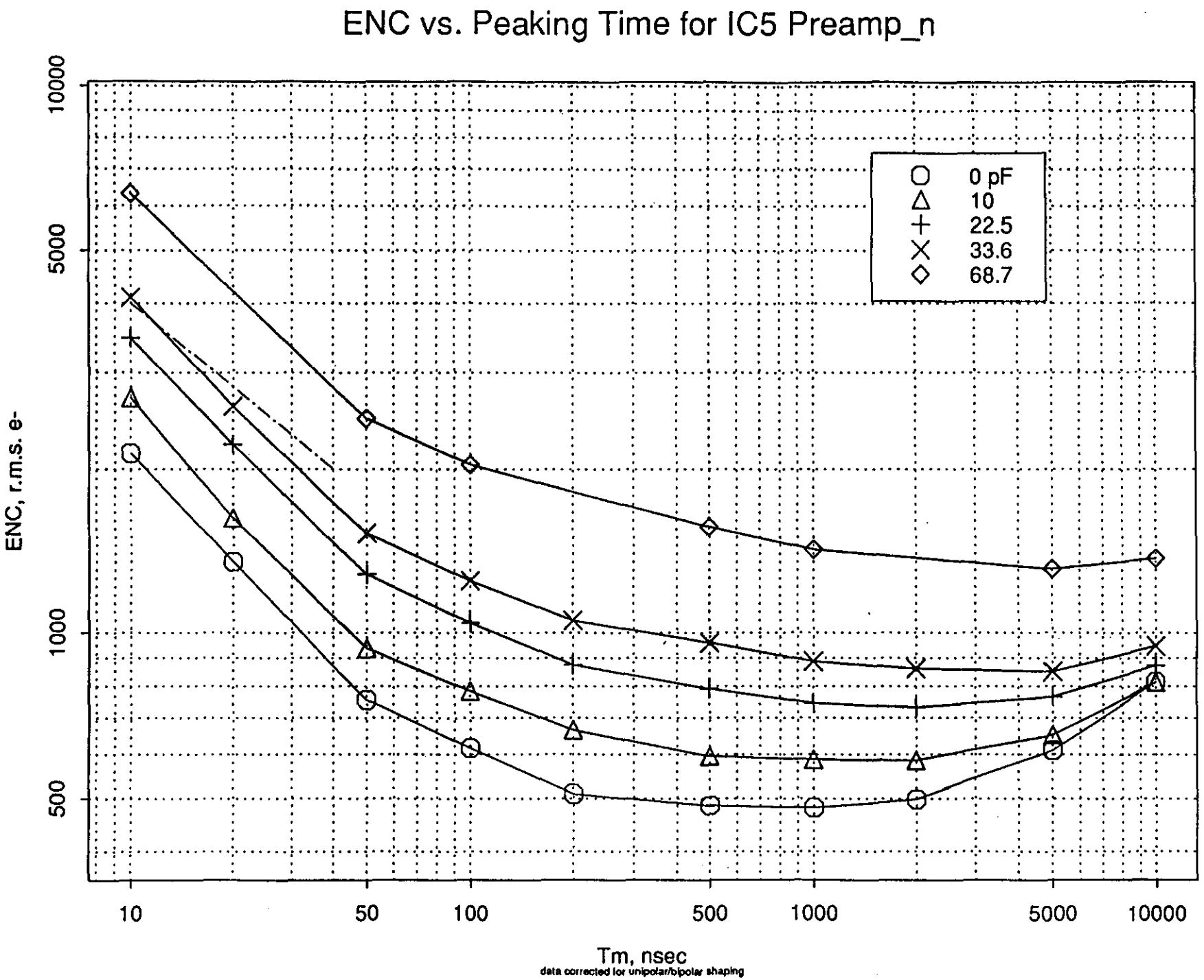
($R_{eq} < 48\ \Omega$)

g_m = 35 mS (FET)

I_d x W/L > 12 A

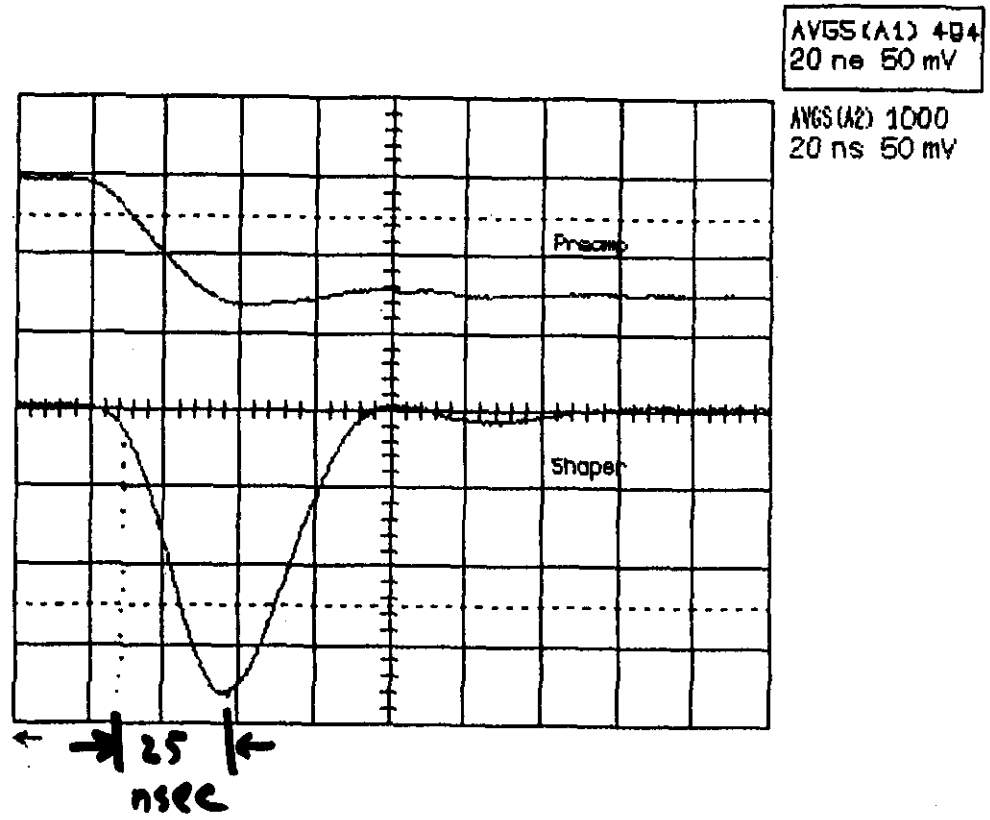
Comparison of BJT and MOS noise




ENC vs. Peaking Time for IC5 Preamp_n
ENC, r.m.s. e-
10000
5000
1000
500
10
50
100
500
1000
5000
10000
Tm, nsec
data corrected for unipolar/bipolar shaping
0 pF
10
22.5
33.6
68.7

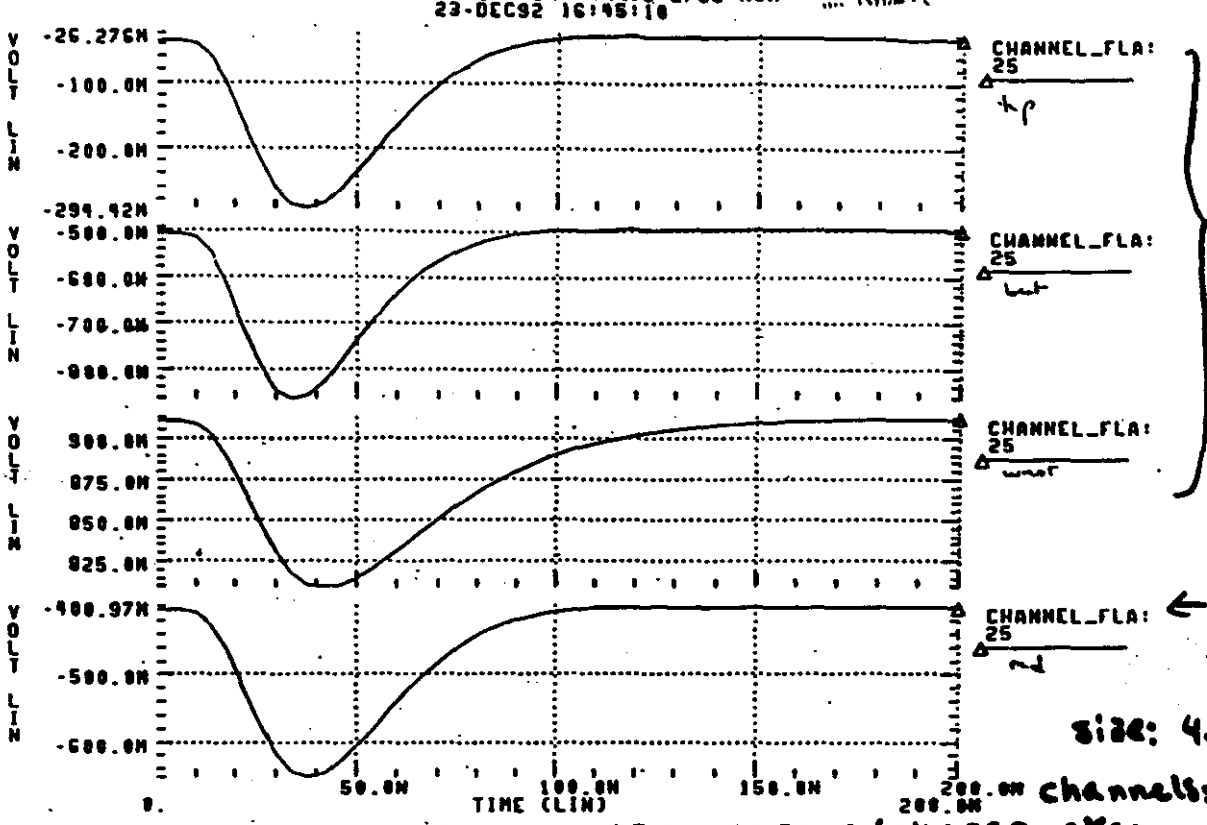
Results of Preamp/Shaper Test Chips Designed at BNL

8 channel preamp/shaper



HARRIS 1.2 μm CMOS AVLSI-RA

C_f = 10pF
C_d = 35pF



PRE-RAD PROCESS VARIATIONS

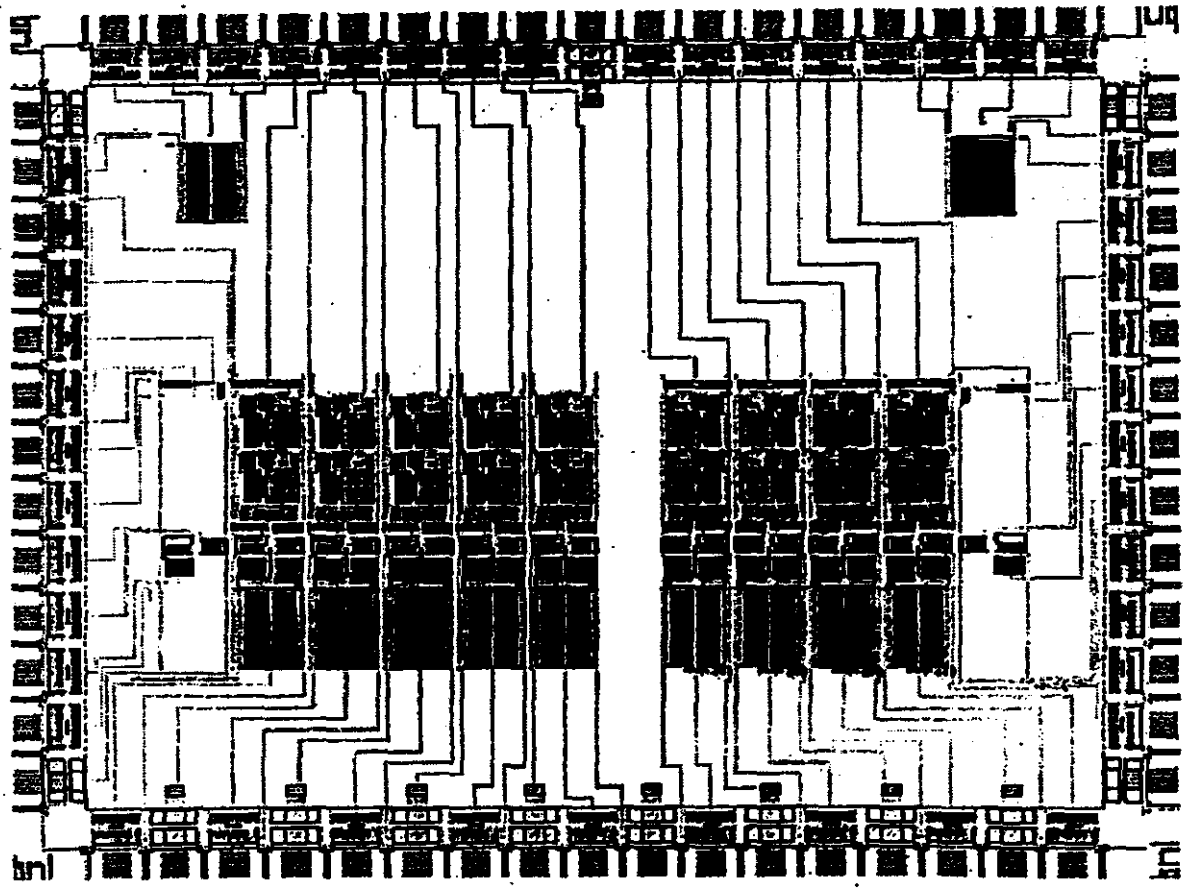
← AFTER 1 MRAD

size: 4.7 x 3.8 mm

channels: 9

HARRIS 1.2μm IPC PREAMP/SHAPER pkg: 68 LCC

power: 80 mW/chan



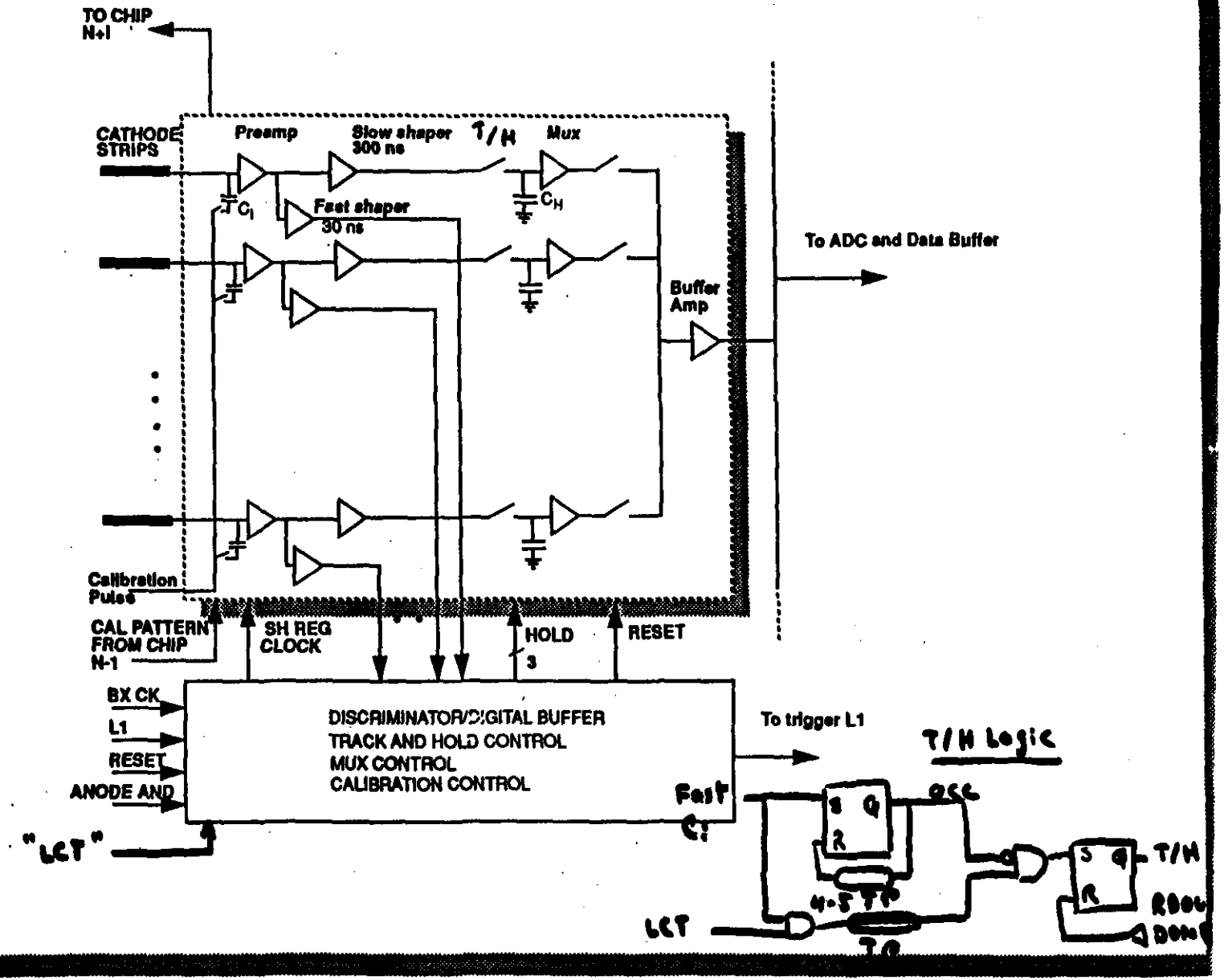
gain: 8 mV/fC

ENC:

1210 + 23.1 e⁻/pF (simulated)

Peaking Time: 25 ns ± 7 ns

Readout Chain for GEM Muon CSC Detector



CSC Cathode Readout Chip Design Requirements

Strip capacitance 80 - 120 pF

Most probable Q_{strip} ~ 36 fC

Track rate ~ 100 Hz/strip

Background rate < 50 KHz/strip ??

Interpolation accuracy 1% strip pitch

→

Slow (readout) channel

Noise: < 2000 e⁻ r.m.s. [1500 desirable]
Gain: ~ 10 mV/fC
Linear response to 150 - 250 fC
Voltage output: semi-Gaussian 300 - 500 nsec t_p
Track/hold: droop < 1 L.S.B. in longest hold time

Fast (timing) channel

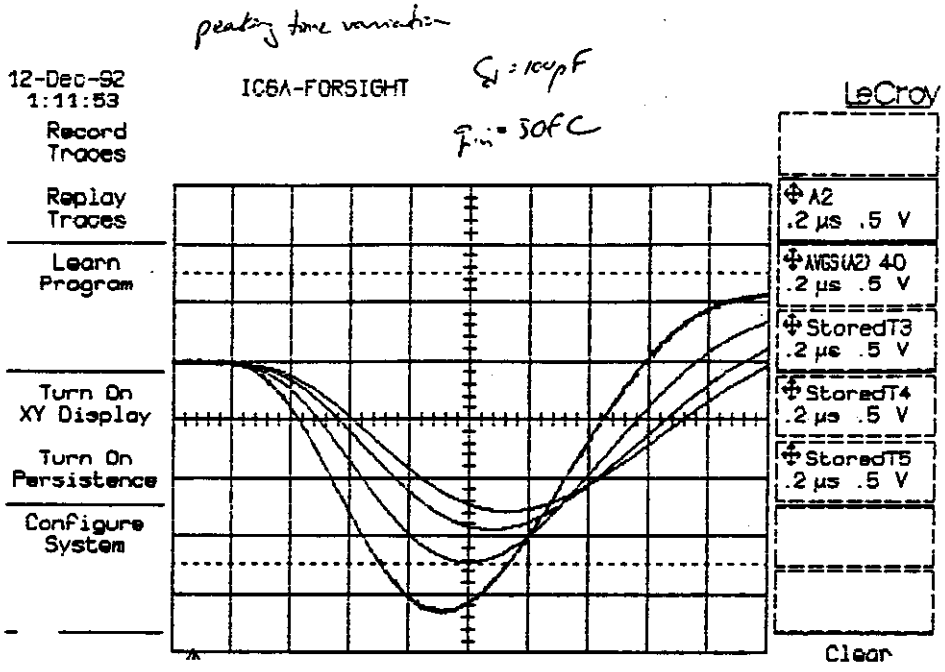
Noise < 5000 e⁻ [4000 desirable]
Risetime ≲ 30 nsec

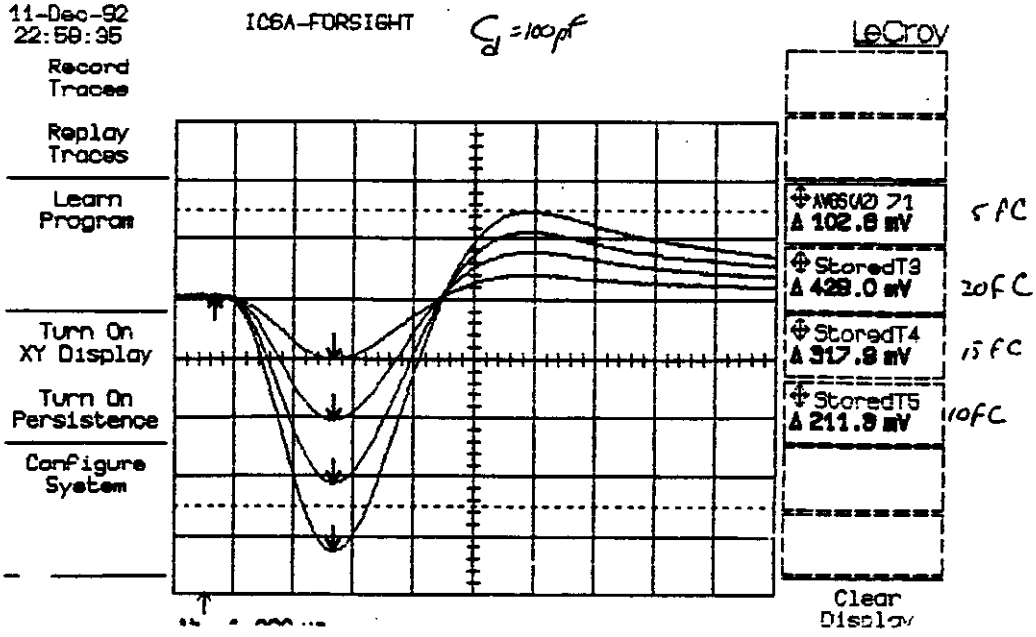
On-chip discriminator with adj. threshold - OPTIONAL

Fast analog sum - OPTIONAL

Output: either current or low voltage differential off-chip drive

Preamp + 1 μsec shaper & CSC



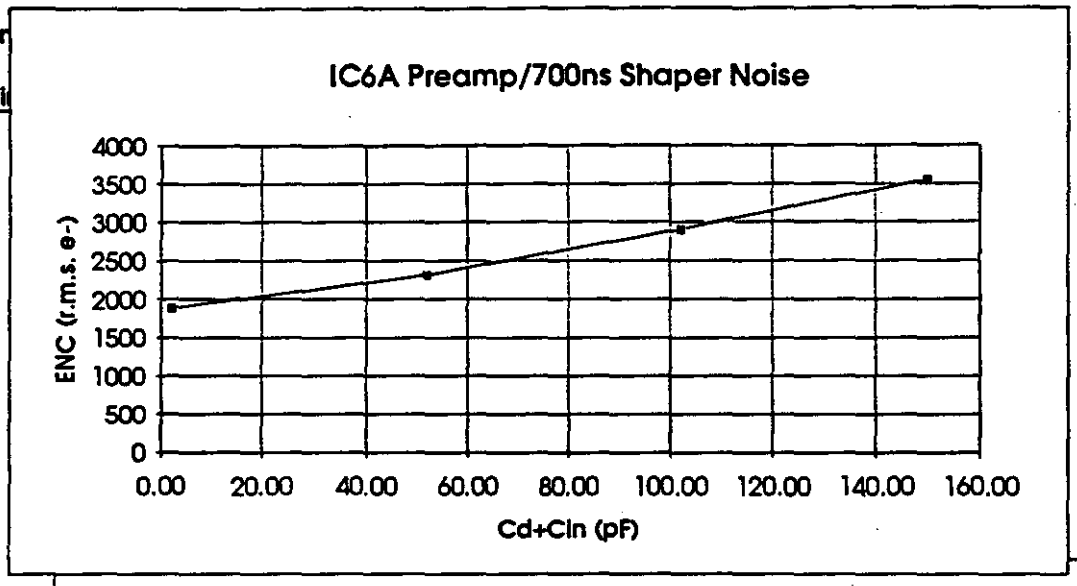


IC6A Device #7 PASH2 Cinj: 2.07E-12 2/20/93
Peaking time adjusted to 700nsec
Cinj=2pF Vin=15mV (1.50V through 40dB atten)
Peaking time adjusted to 700nsec Qin: 3.11E-14
Cinj=2.07pF Vin=15mV (1.50V through 40dB atten)
AD811 Op Amp Gain = 2

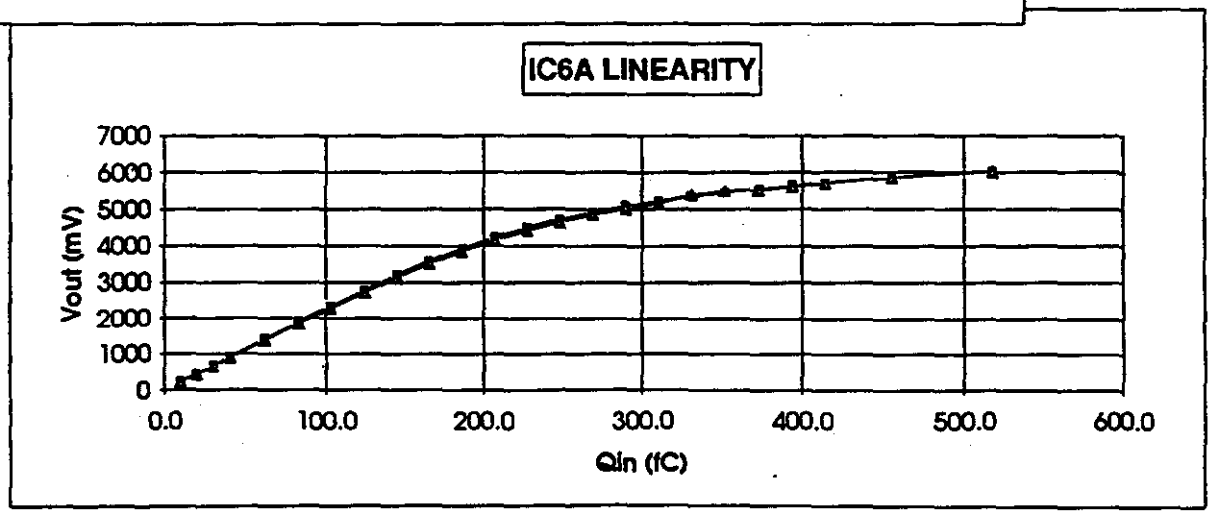
IB2:	.36m	V_PA:	-1.63	VB1:	0.903	VBIAS:	0.999
IB3:	5.36m	V_SH:	1.224	VB2:	-1.162		
IBIAS:	80u	V_IBIAS:	1.019	VB3:	-0.458		

Tp (5-100% 620 nsec

Cd	Cd + Cinj	Vout	Vnoise	System	SNR	Gain	ENC	ENC	Slope	Intercept
0	2.07	0.6765	6.6	0.54	103	21.79	3.02E-16	1884	11.32	1799.22
49.9	51.97	0.6696	8.02	0.54	84	21.57	3.71E-16	2316		
99.9	101.97	0.659	9.91	0.54	67	21.22	4.66E-16	2910		
147.7	149.77	0.6601	12.1	0.54	55	21.26	5.69E-16	3549		
pF	pF	V p-p	mV rms	mV rms	-	mV/fC	C	e-	e-/pF	e-



1800
+11 e-/pF



SCHEDULE

DESIGN OPEN ISSUES

4/93 | 7/93 | 10/93 | 4/94 | 7/94

IPC Front End

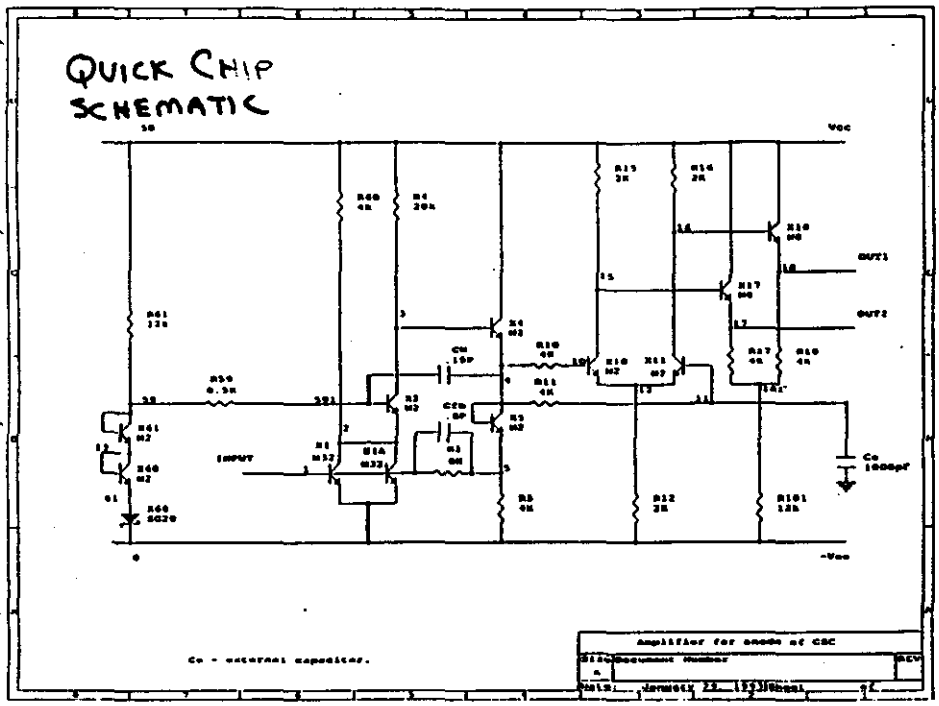
Test soft cmos preamp w/Yale chamber — PCB, TEST

AVLSI-RA hard cmos PA/SH

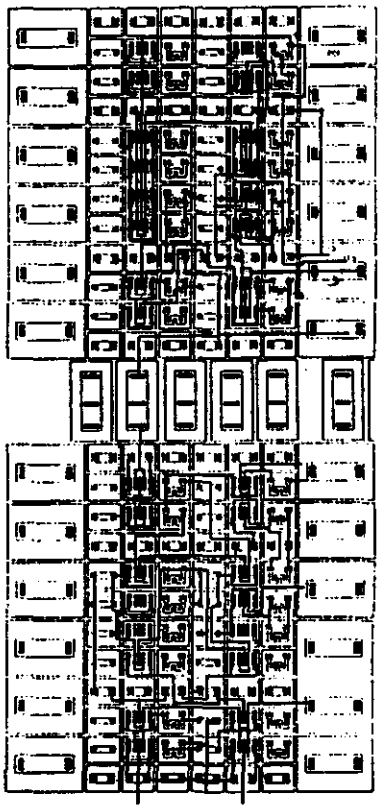
	IPC	CSC cathode	CSC anode
Preamp R_F control — DESIGN, FAB, PCB	-	x	-
Ion tail cancellation — TEST	x	x	x (?)
AVLSI-RA 2nd iteration — DESIGN, FAB (QUANT.), TEST	x	x	-
Shaper noise optimization			
Gain control	x	x	x
CSC cathode readout IC			
IC6a PA/SH/TH TEST — Comparator design	-	x	x
IC10 PA/SHS/SHF/TH/MUX — Low voltage I/O — DESIGN, FAB	-	x	?
ESD susceptibility — TEST JET/PCB, TEST	x	x	x
IC11 PA/SHS/SHF/TH/MUX/CAL + DIG ASIC ? — DC drift calibration — DESIGN, FAB (QUANT.), TEST	x	x	-
Line mismatch effects		x	xx
CSC Anode IC			
DELTA IC TEST — Crosstalk	xx	x	x
TEK PA/SH — Bipolar version of preamp — DESIGN, PCB, TEST SET, TEST (PNP)	x	-	-
TEK DISC — Packaging — DESIGN, FAB, TEST	x	x	x

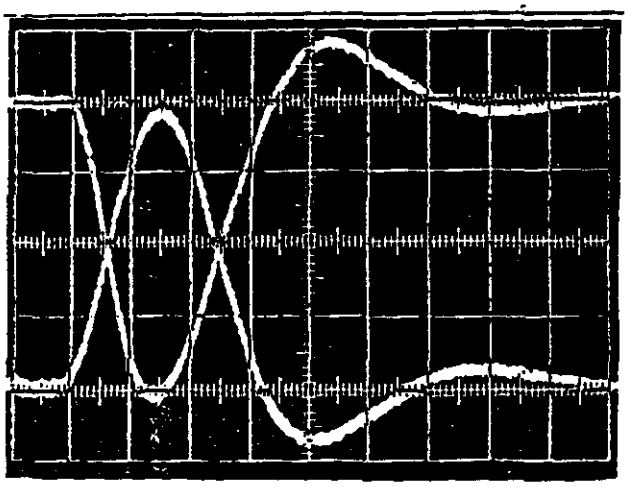
N. BONDAR

QUICK CHIP SCHEMATIC



DELTA LAYOUT





IMPULSE RESPONSE

PMT	DELTA	QUICK-CHIP	
NOISE	2K + 25e⁻/pF	1K + 40e⁻/pF	
GAIN	4	5	mV/fC
POWER	21	15	mW
RISE TIME, Cin = 300pF	25	< 7	ns
INPUT RESISTANCE	20	15 → 8	Ω
OUTPUT RANGE	.6	.6	V
RECOVERY	200	200	nS

Rad-Hard AMU Development at Oak Ridge National Laboratory

C. L. Britton, Jr.

L. C. Clonts

A. L. Wintenberg

K. F. Read

Presented at the February '93 GEM DAQ Meeting

SSC Laboratory

Dallas, TX

The Goals...

* Test the radiation hardness of the Harris AVLSI-RA process

* Make a memory good to 9 bits in this process

* Make the memory read-time <500ns

* Have power dissipation ~10mW/channel

* Have depth => 128 cells

What we are planning to submit...

"D" Chip

*** 8x128 memory chip with readout (interdigitated decode,**
4 channels VWVR, 4 channels VWCR,
5.049mm x 5.895mm)

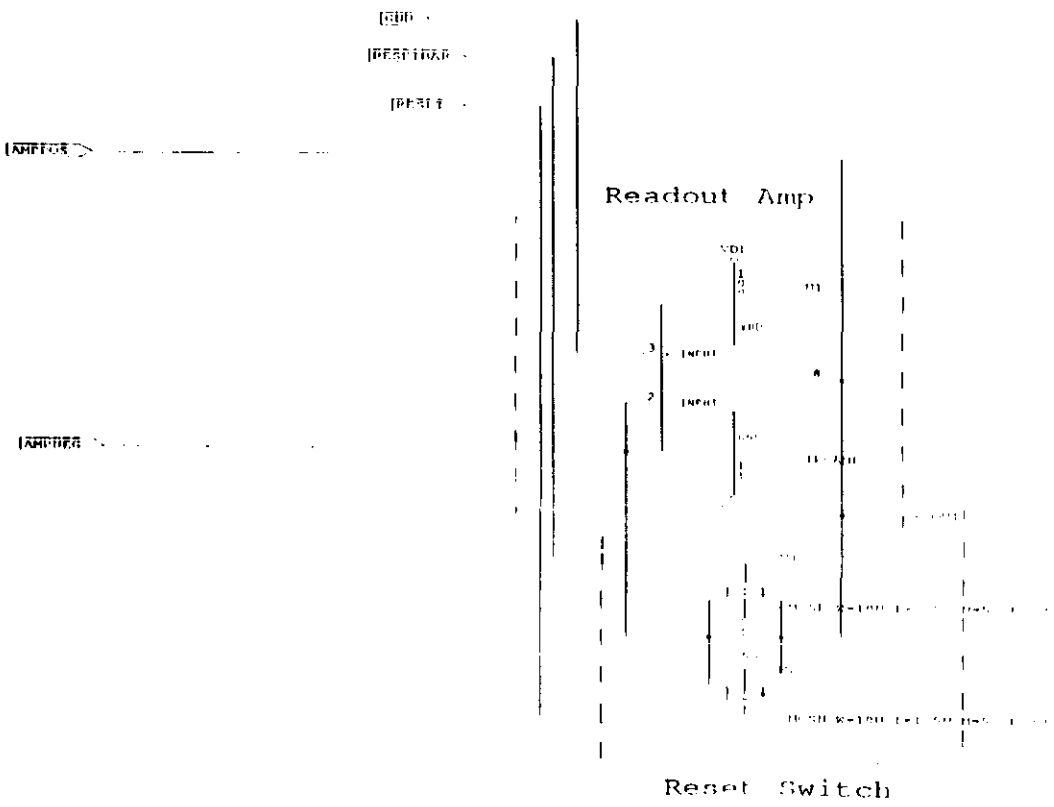
"S" Chip

*** 8x128 memory chip with readout (block decode,**
4 channel VWVR, 4 channels VWCR,
5.049mm x 5.895mm)

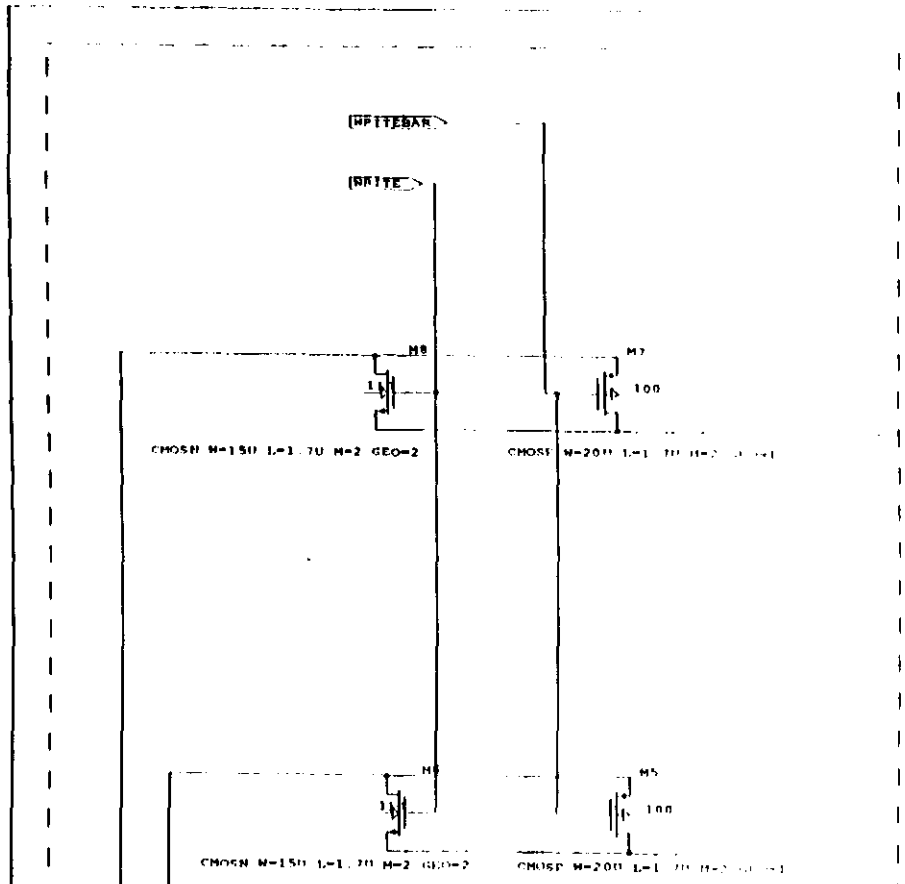
"T" Chip

*** Test pieces chip**

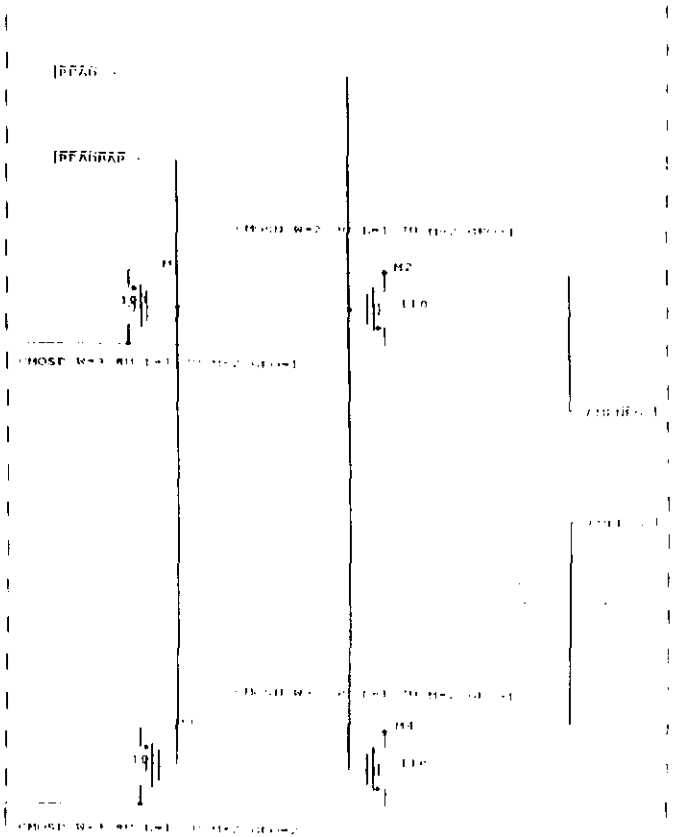
Read address (odd)
Read decoding
Read address (even)
Outputs
Inputs
Write address (odd)
Write decoding
Write address (even)



PRELIMINARY SCHEMATIC

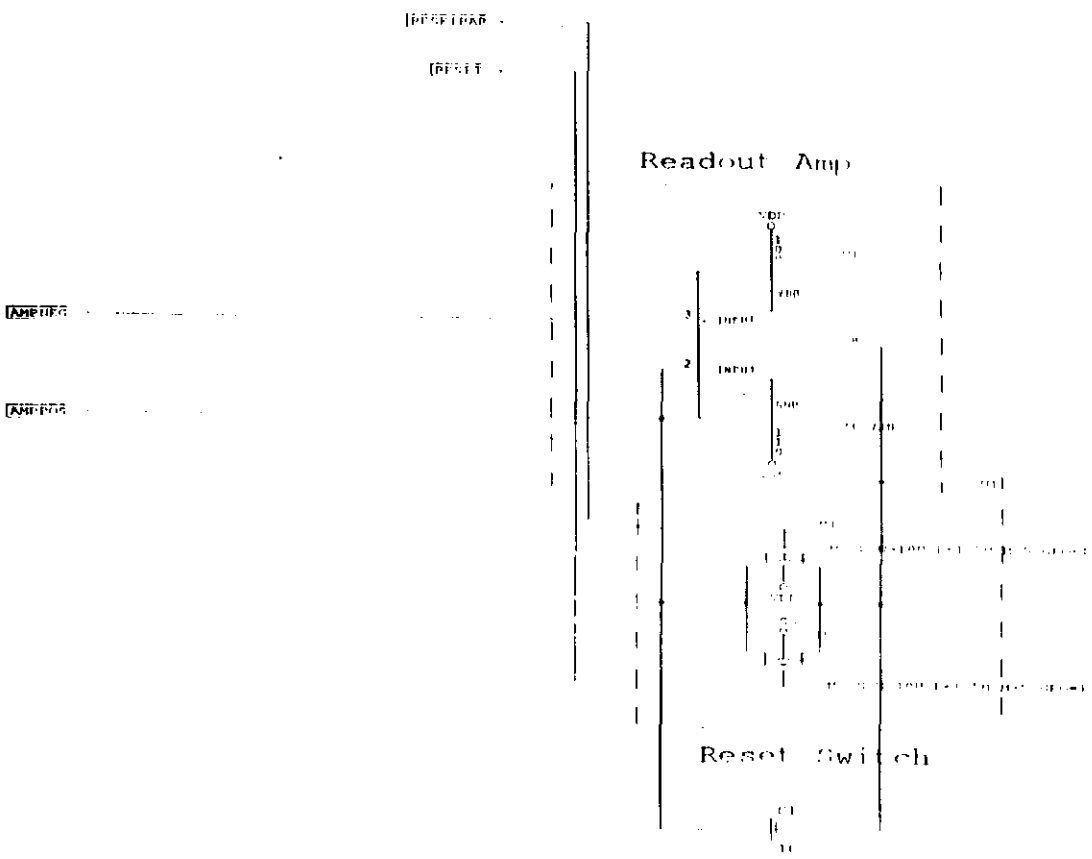


Write Cells

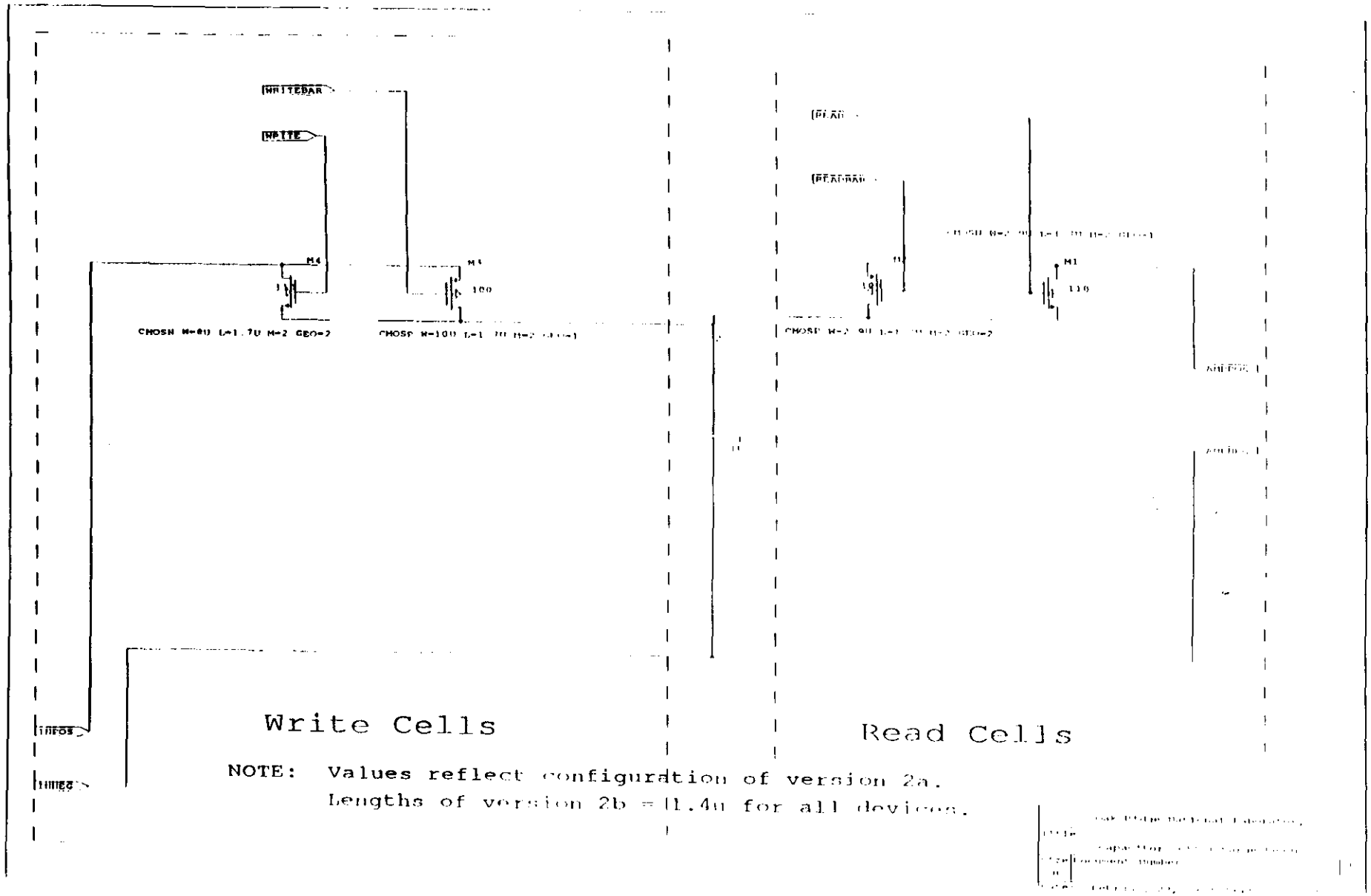


Read Cells

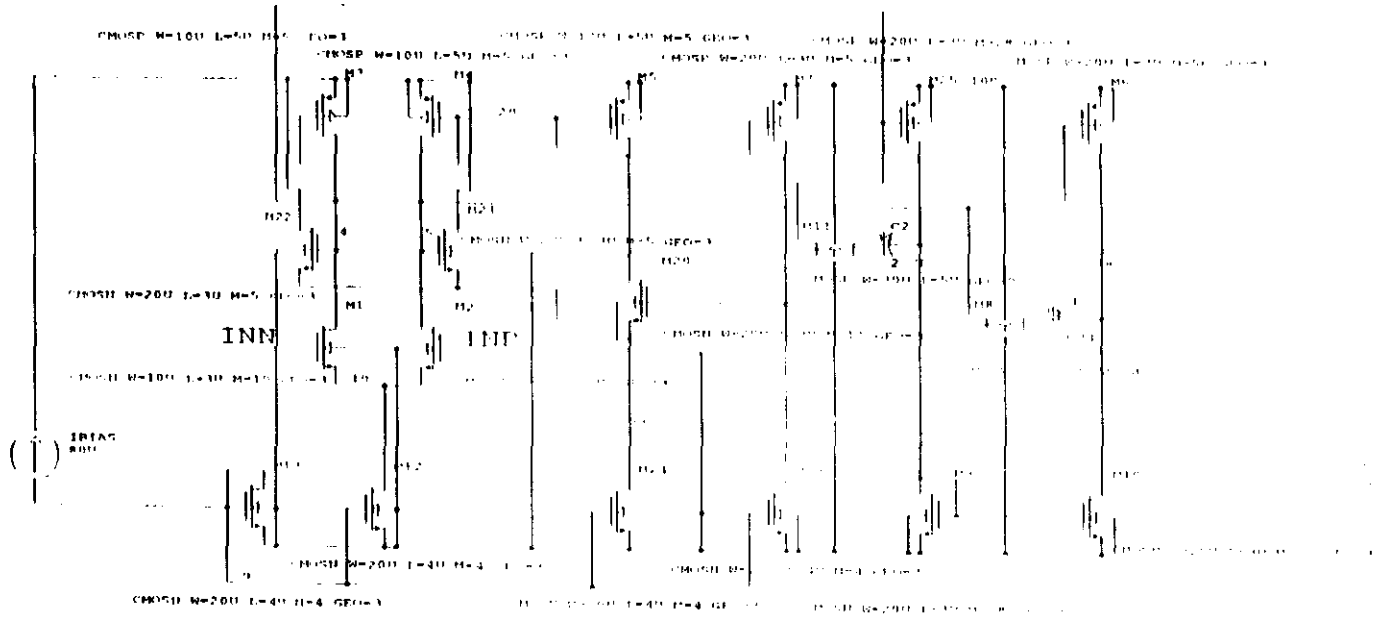
NOTE: Values reflect configuration of version 2a.
Lengths of version 2b = 1.4μ for all devices.



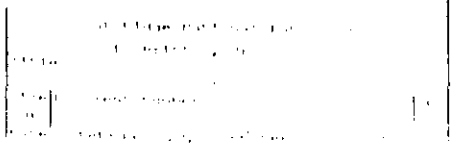
PRELIMINARY SCHEMATIC



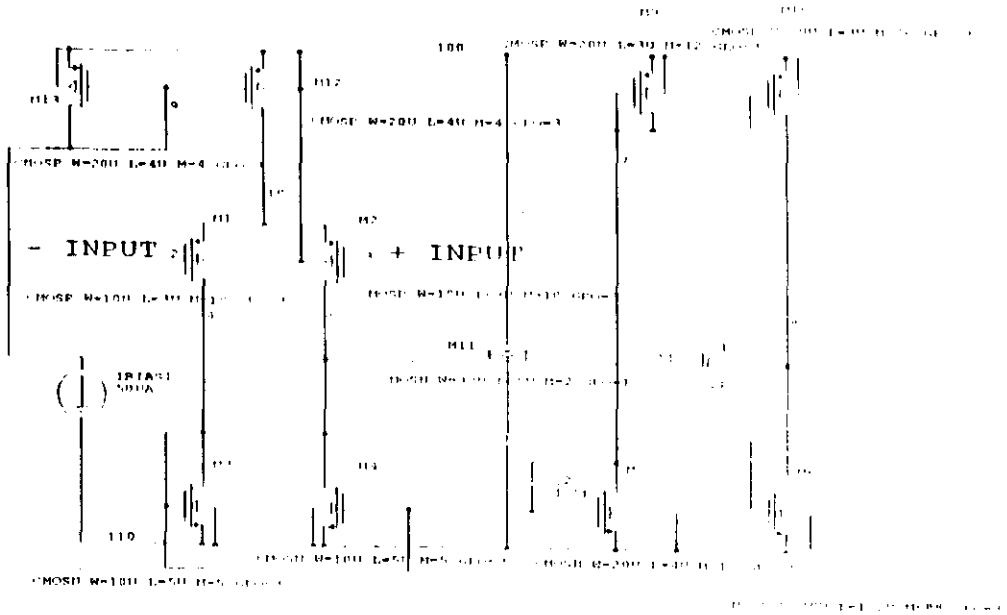
NOTE: Values reflect configuration of version 2a.
Lengths of version 2b = 1.4u for all devices.



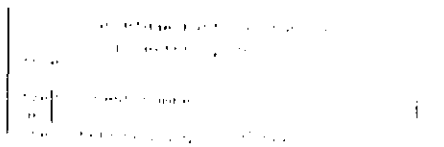
PRELIMINARY SCHEMATIC

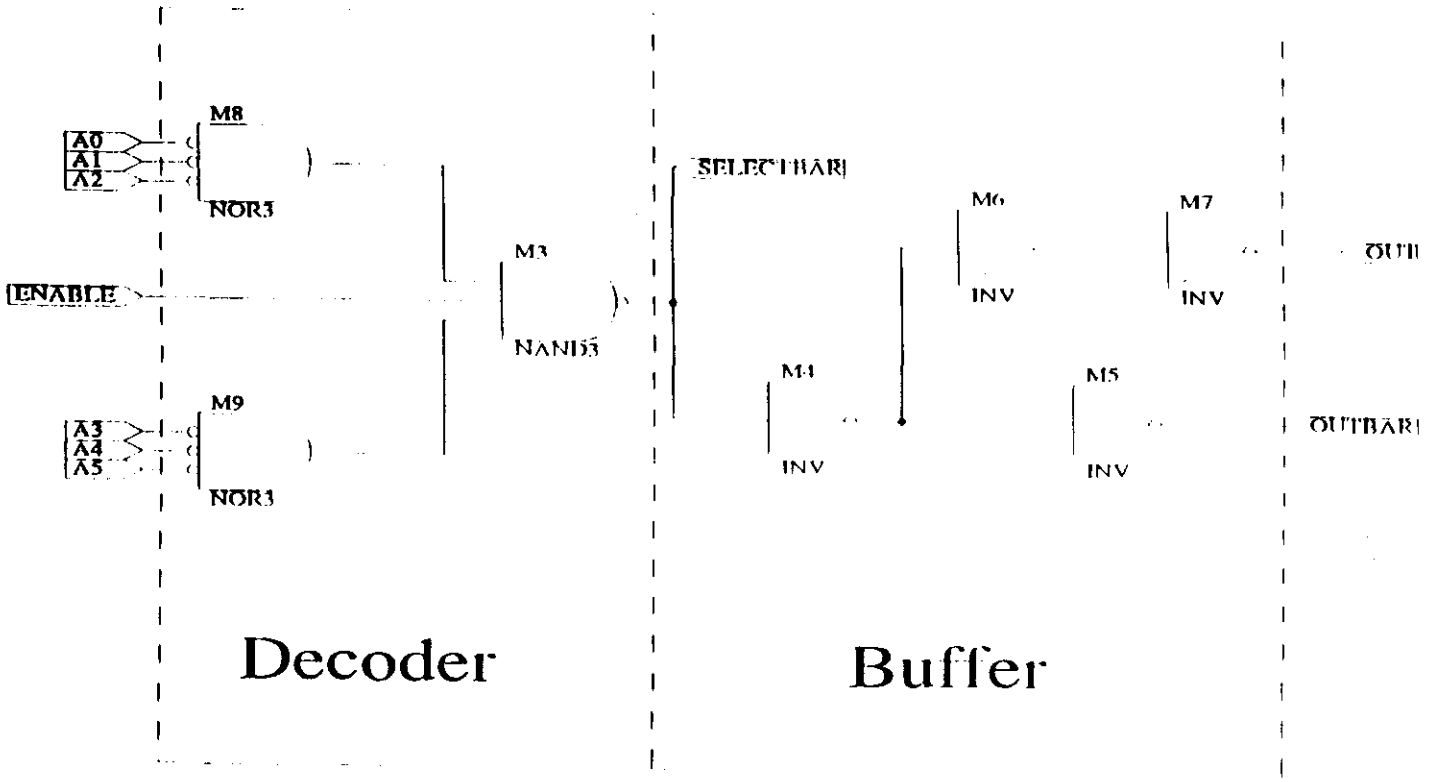


PRELIMINARY SCHEMATIC



PRELIMINARY SCHEMATIC





Oak Ridge National Laboratory

Title: IPC DECODER CELL

Size: A | Document Number | REV: C

Date: February 10, 1993 | Sheet 1 of 1

Parameters that affect read-time

* Frequency response, phase margin --> settling time
* Phase margin, slew rate --> reset time
* DC gain --> precision

For the topologies chosen..

* Settling time affected by output pole (high bus capacitance)
* Bandwidth determined by input g_m/C

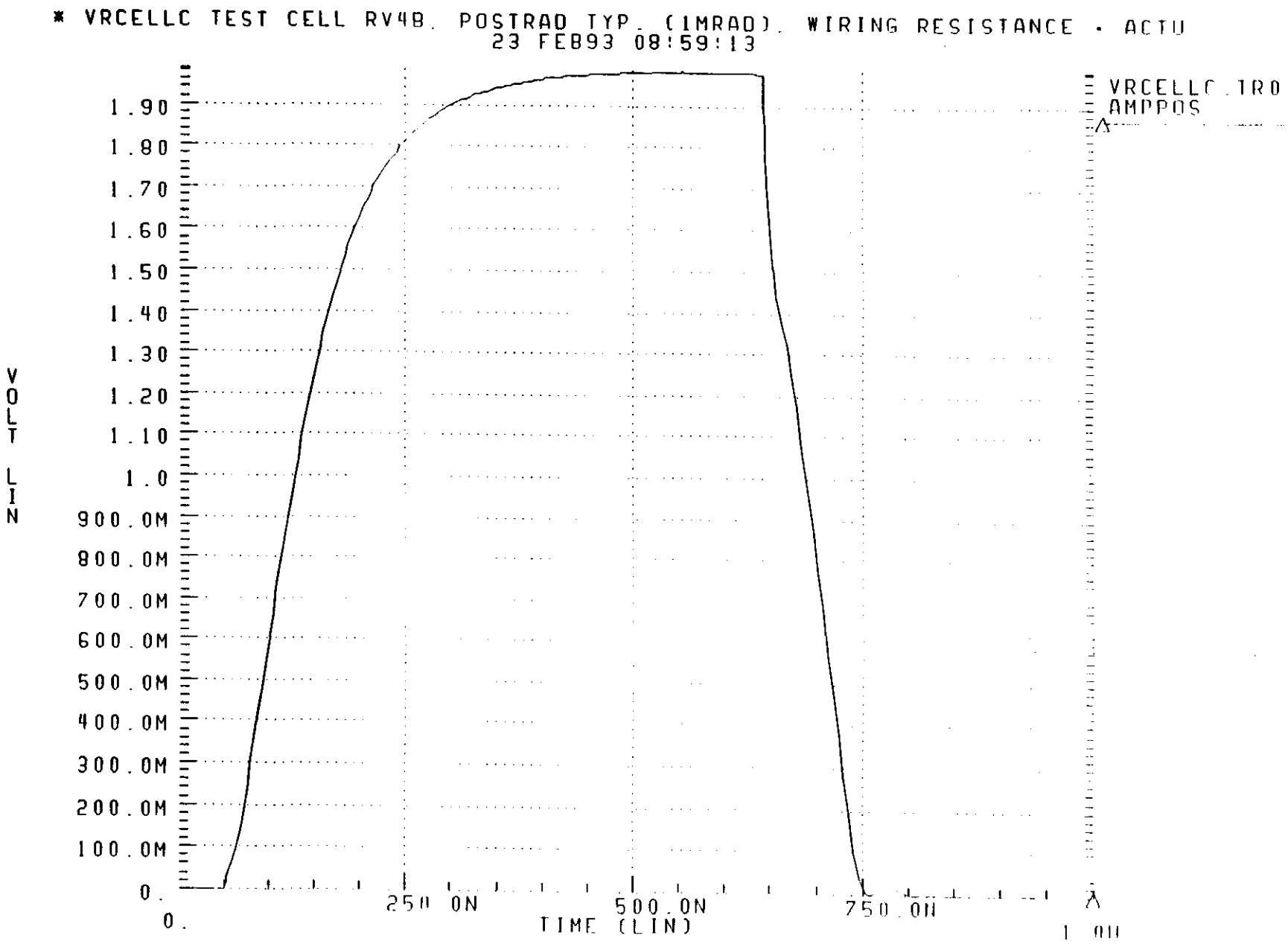
Some areas studied for optimization have included...

* Input bandwidth vs. switch size (process dependent)
* Droop rate vs. switch size and radiation dose
* Output bandwidth vs. bus loading
* Output stability vs. spatial location

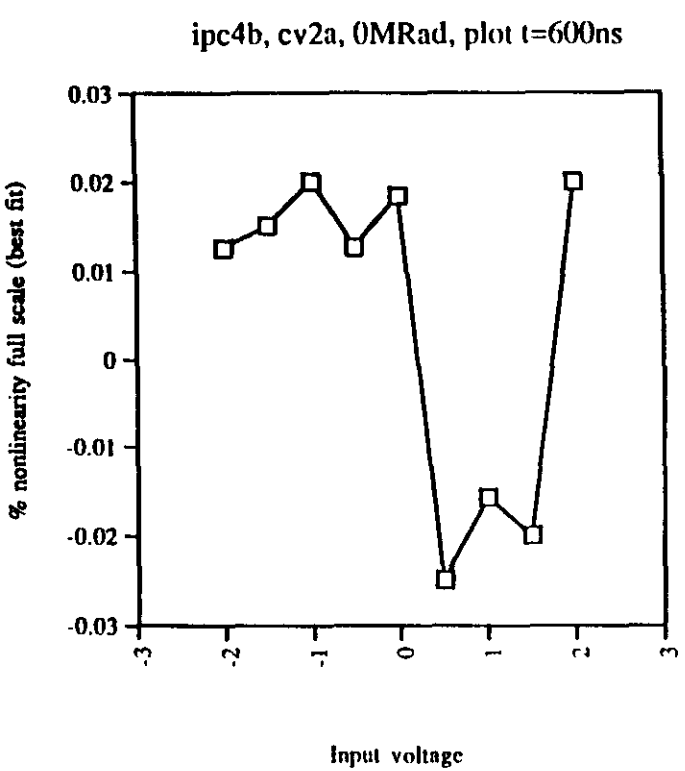
The opamp characteristics..

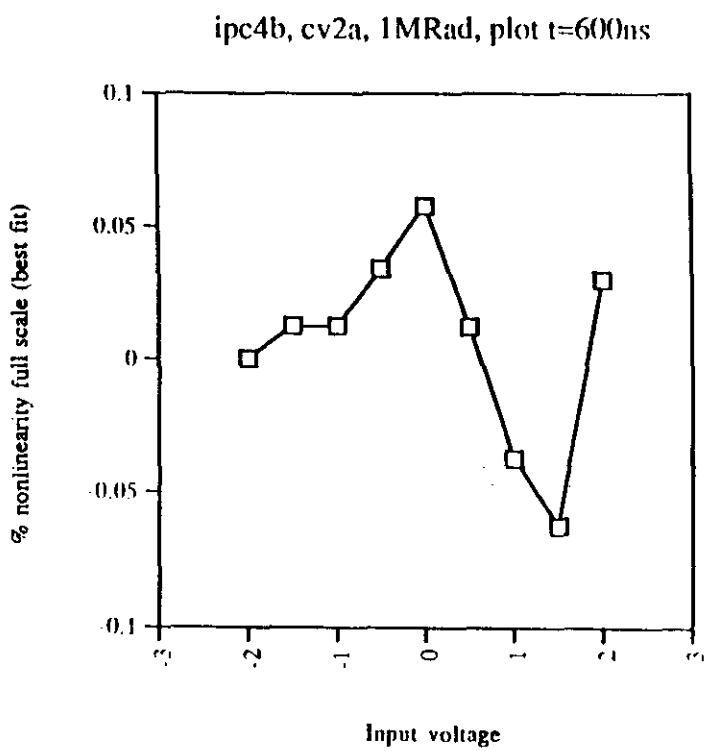
Amplifier	IPC4B	IPC5C
Bandwidth	11MHz	11MHz
Phase margin	~60°	~60°
Slew rate	> 20V/μs	>20V/μs
Power	9.4mW	6.7mW

(4B output stage similar to Babanezhad, Jour. Solid State Ckts. Dec '88 pp. 1414-1417)


* VRCELLC TEST CELL RV4B. POSTRAD TYP. (1MRAD). WIRING RESISTANCE - ACTU
23 FEB93 08:59:13
VRCELLC.TRO
AMPPOS
VOLT LIN
1.90
1.80
1.70
1.60
1.50
1.40
1.30
1.20
1.10
1.0
900.0M
800.0M
700.0M
600.0M
500.0M
400.0M
300.0M
200.0M
100.0M
0.
0.
250.0N
500.0N
750.0N
1.0U
TIME (LIN)

Integral nonlinearity simulations *(ipc4b, cv2a)*





We fabbed IPC4B in Orbit's 1.2μ nwell process....

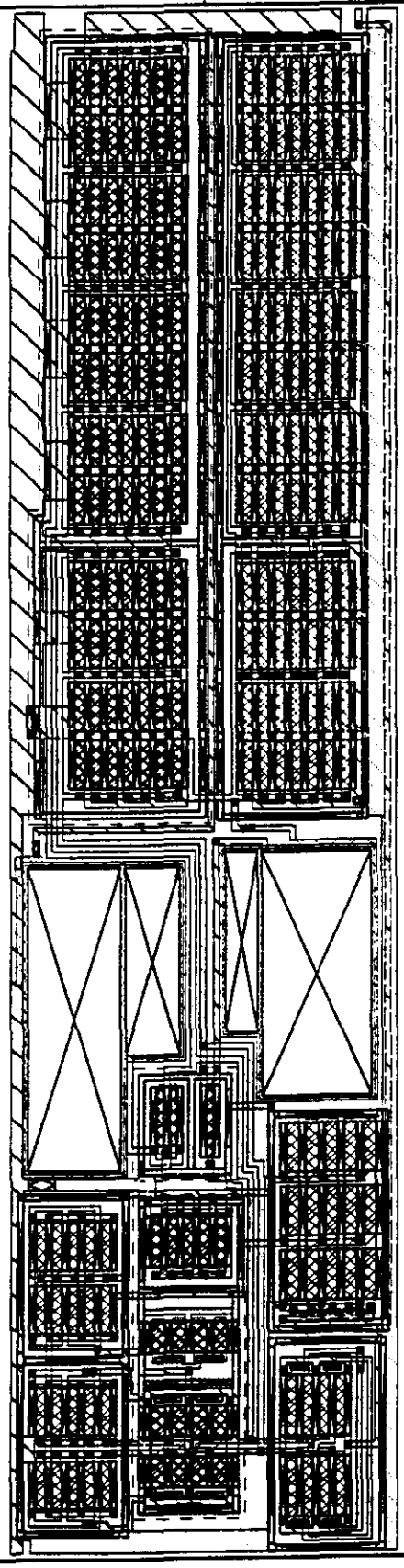
(5 units measured)

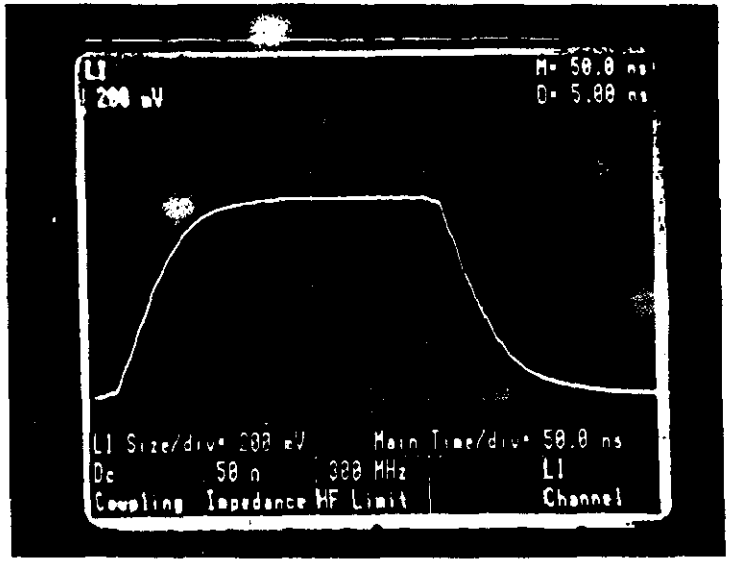
* Input offset = -0.366mV, σ = 1.42mV
* Unity gain risetime = 22ns
* Slew rate = 20V/μs
* Open loop DC gain = 10-15K

OAK RIDGE NATIONAL LABORATORY

Instrumentation and Controls Division

DATE: Feb 22, 1993	Scale: 120 lambda/inch
	User: clonts





'Scope photo of 4b, inverting gain of 3

To summarize the expected performance....

* Power dissipation ~ 10mW/channel

* We can make this 9-11 bit writing by adjusting the access time

* The 10-bit read time should be ~ 500-600ns

The status.....

* **We have finished both design reviews**

* **We are presently finalizing changes**
  (Includes modifying tech file and distributing to BNL)

* **The order has been placed**

* **We will get quotes on packages when the rest is done**

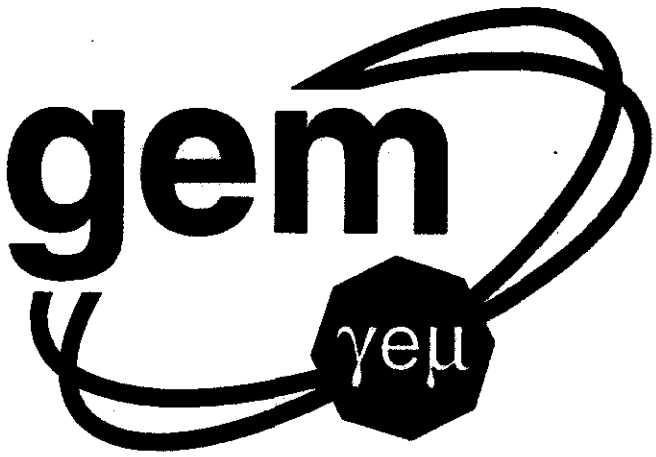
In summary

* We are almost ready to submit to Harris

* We have simulated out the wazoo, but continue
  (wazoo = 10^{bubba})

* The simulations appear to support a 10-bit memory

* We need to begin to converge towards a final configuration



Presentation by:

J. Parsons

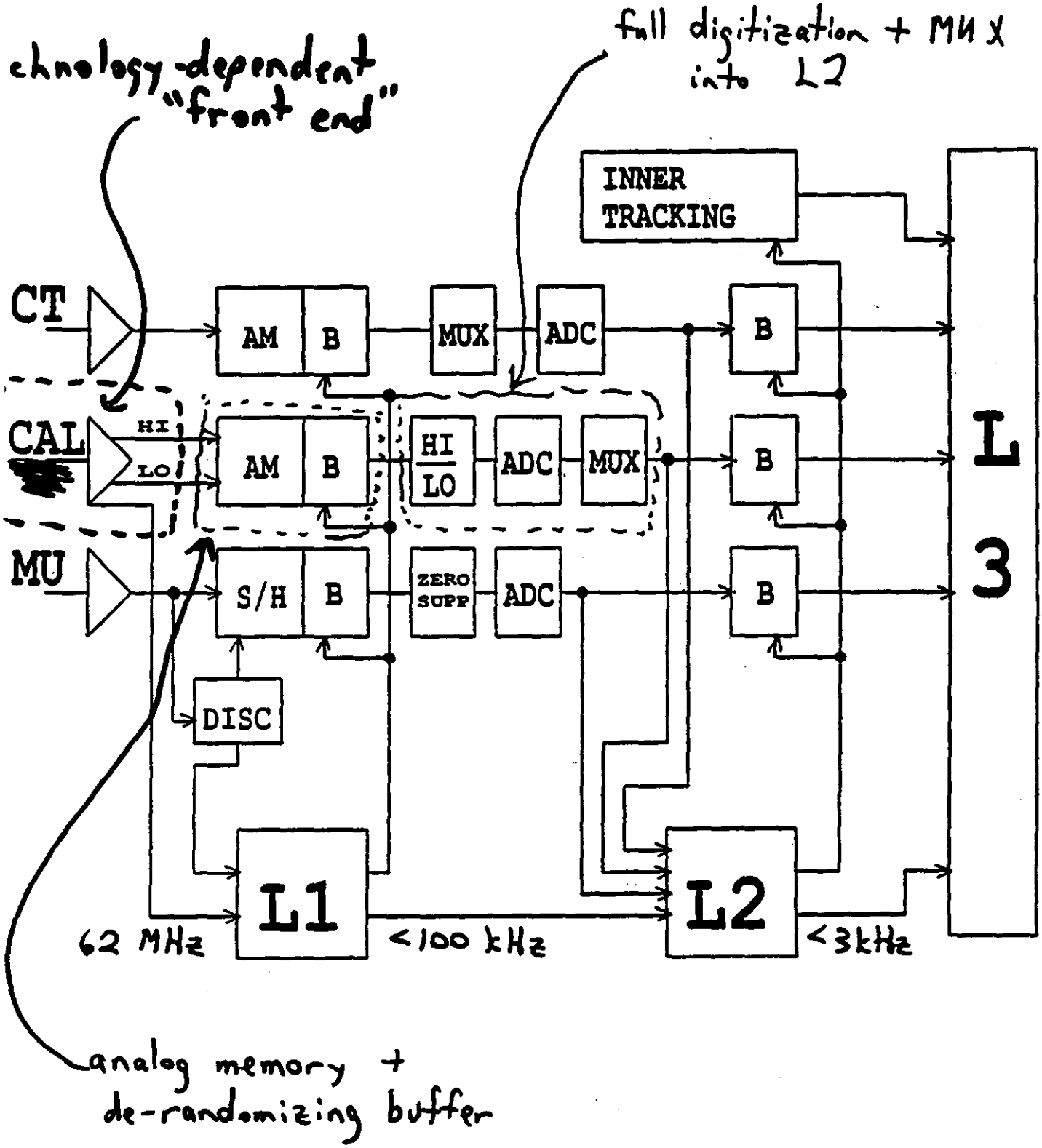
C. Parsons
Feb. 24/93

GEM CAL READOUT ELECTRONICS

System Requirements

- $\approx$ 120 k channels,
- $\geq$ 16 bits of dynamic range,
- contribution to constant term in $\sigma(E)/E$ of $< 0.2\%$,
- time resln sufficient to uniquely identify bunch crossing,
- storage of CAL signals during L1 latency of 2 μs,
- deadtimeless operation at max L1 rate of 100 kHz,
- transfer of fully digitized data (up to 5 samples / signal) to L2 at 100 kHz rate
- analog sums for L1 trigger
- LOW COST, LOW POWER !!

Overview of GEM Trigger/DAQ System

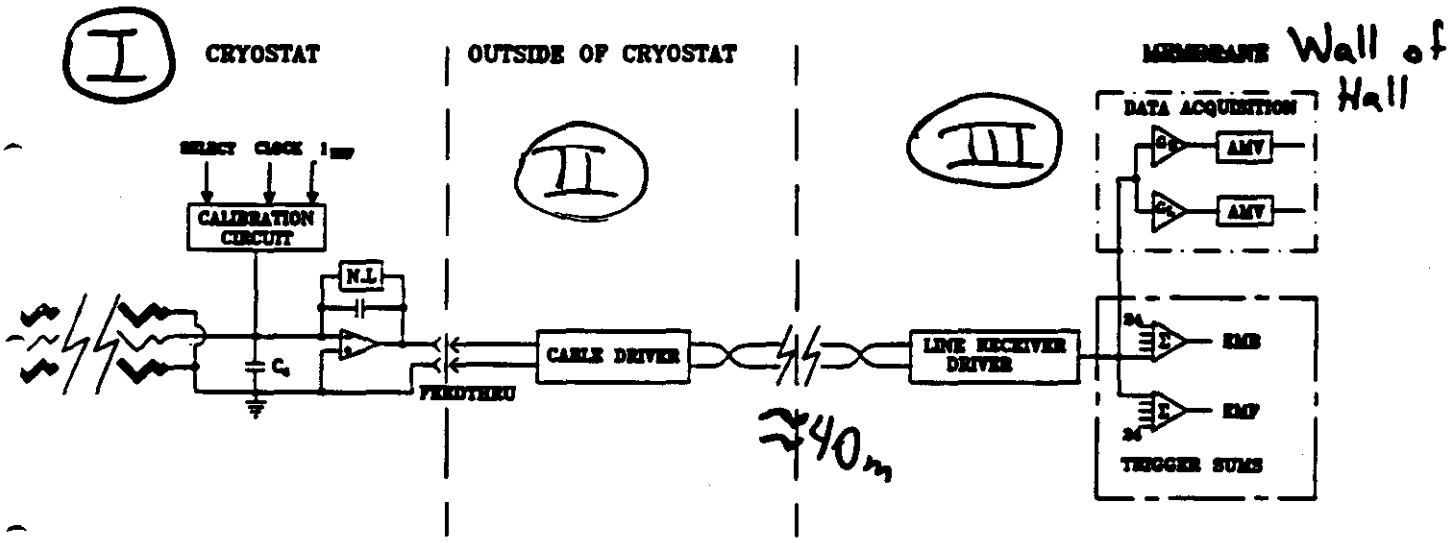


OVERVIEW OF THE READOUT

I) - cold JFET charge-integrating preamp
↳ nonlinear response above ≈ few hundred GeV

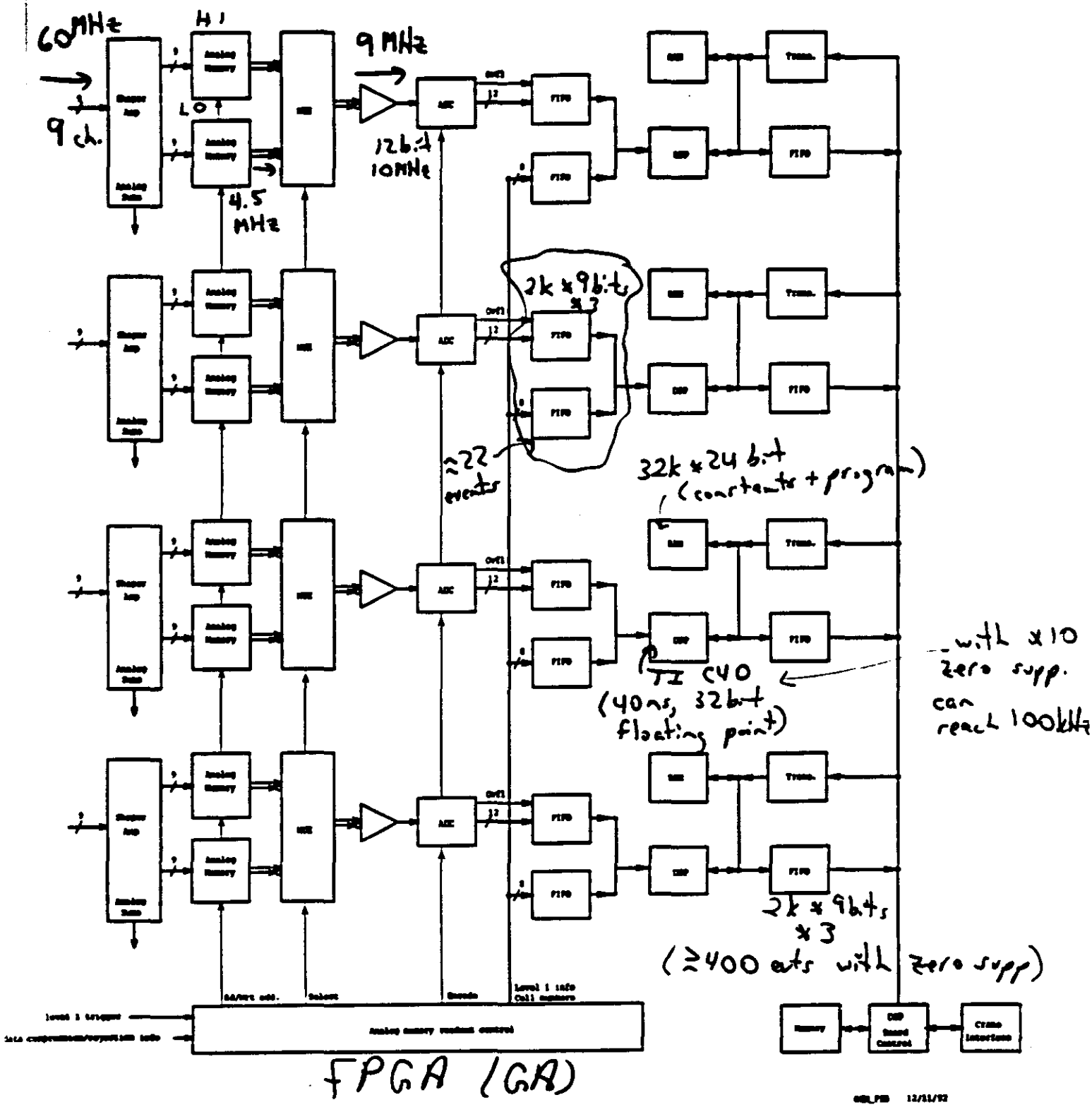
- precision calibration system

I) - cable drivers mounted on outside of cryo in "junction boxes"

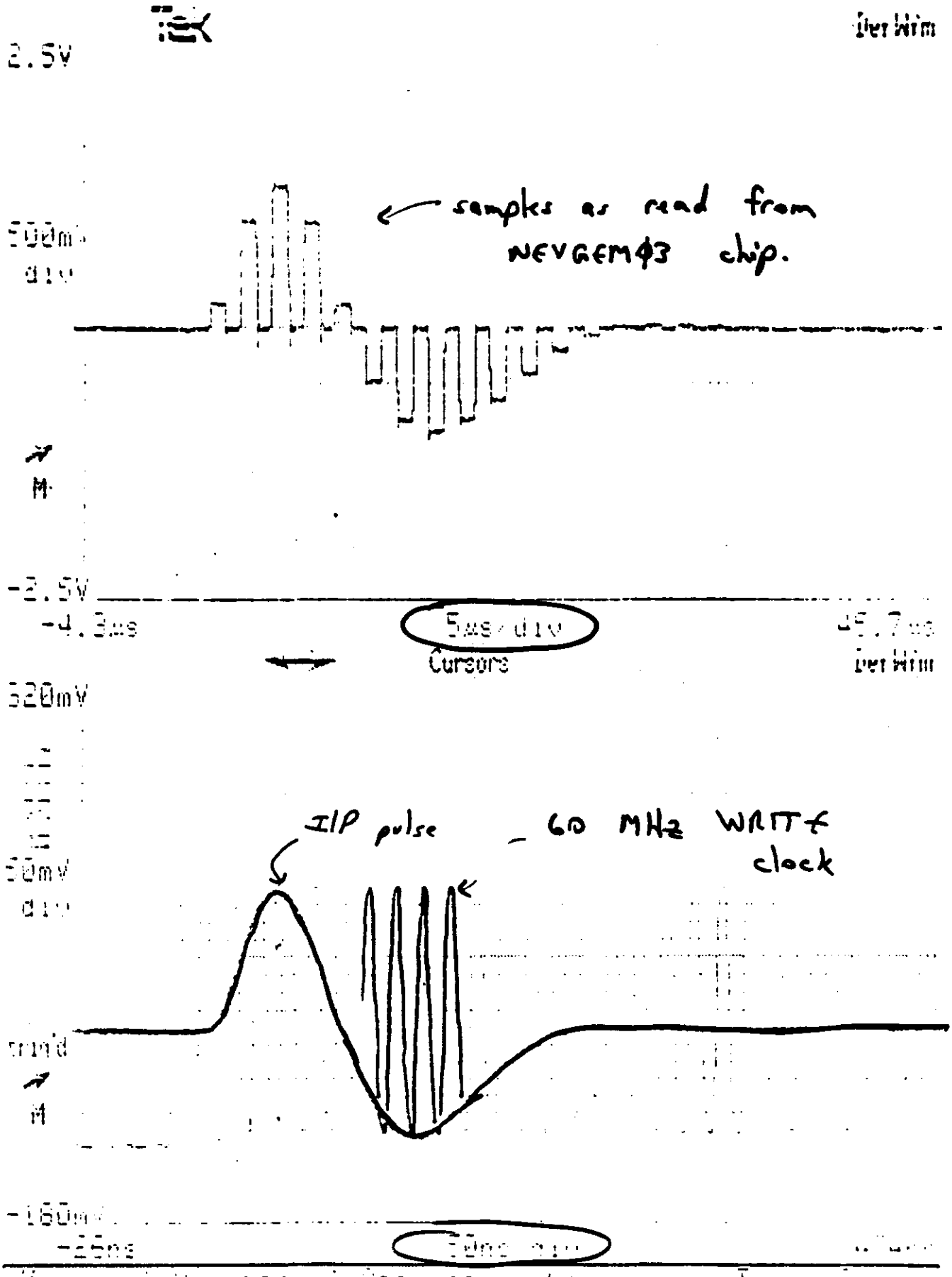


II) - racks of boards which:
- receive differential signals, and shape them
- sample @ 60 MHz
- store samples using SCA for 2μs latency
- buffer, digitize, process, format data for L1 triggered events
- form 1st level of analog summing for L1 trigger

36 Channel Readout Board



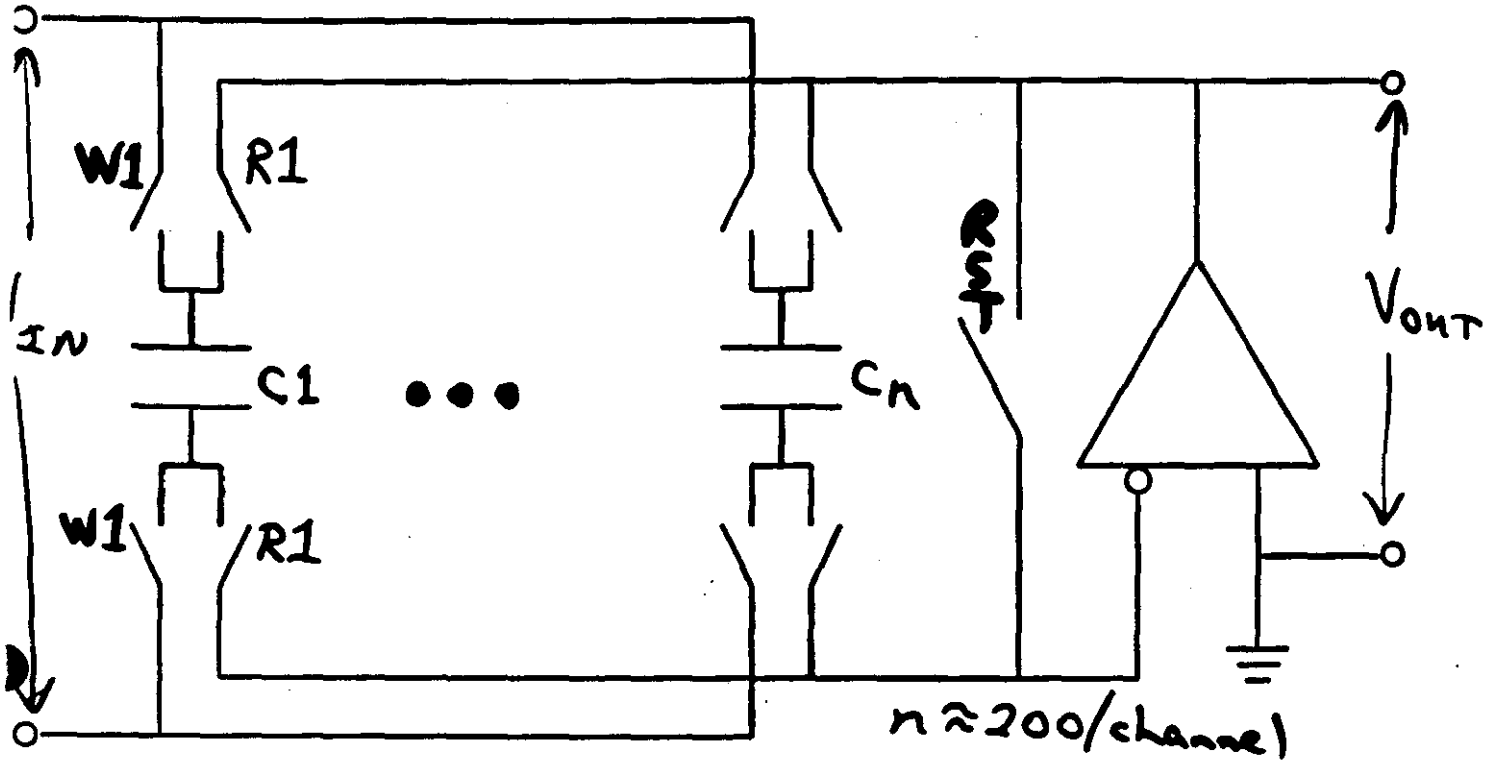
11402 DIGITIZING OSCILLOSCOPE [exp:3.7,dig:3.91,day:3.3]
date: 1-SEP-92 time: 8:50:58 Instrument ID# B010270



Vertical	Horizontal	Acquire	Lower	Trace dep
Desc	Desc	Desc	Graticule	
	Window		Linear	Trace dep

Switched-Capacitor Analog Memory

- sample voltage every 16ns and store in switched-cap. array awaiting L1 decision.



- **deadtimeless** through simultaneous R/W capability + virtual buffer
  - ↳ requires complicated address bookkeeping
- existence proof provided by LBL.
- can achieve 12-13 bits of dynamic range
  - ↳ need at least 2 gain scales
- may need to correct for cell-to-cell pedestal differences, especially when adding up large number of channels.

Analog Memory Control Requirements

- Use of virtual buffering and simultaneous Read/Write requires AM to be supplied with Addresses as well as Clocks.
- Addresses will be generated off the AM chip, with on-chip address decoders used to maintain the small SC pitch.
- The design philosophy for the AM Control stresses the desire to:

1 Minimize Noise Introduced into Analog Environment

- No on-chip communication between Read and Write logic; avoids crossing analog layout.
- Reduce number and rate of change of control lines:
  - Send Read Address bit serially (saves 6 lines).
  - Derive Write Address bit 0 from counter on AM chip (saves 1 line, reduces communication frequency to 30 MHz, simplifies external control).
  - Prevent significant randomizing in sequence of Write Addresses.
  - Use on-chip Write Address accumulate and send Incremental Address (saves 2 lines, provides reduction in rate of change of existing lines).

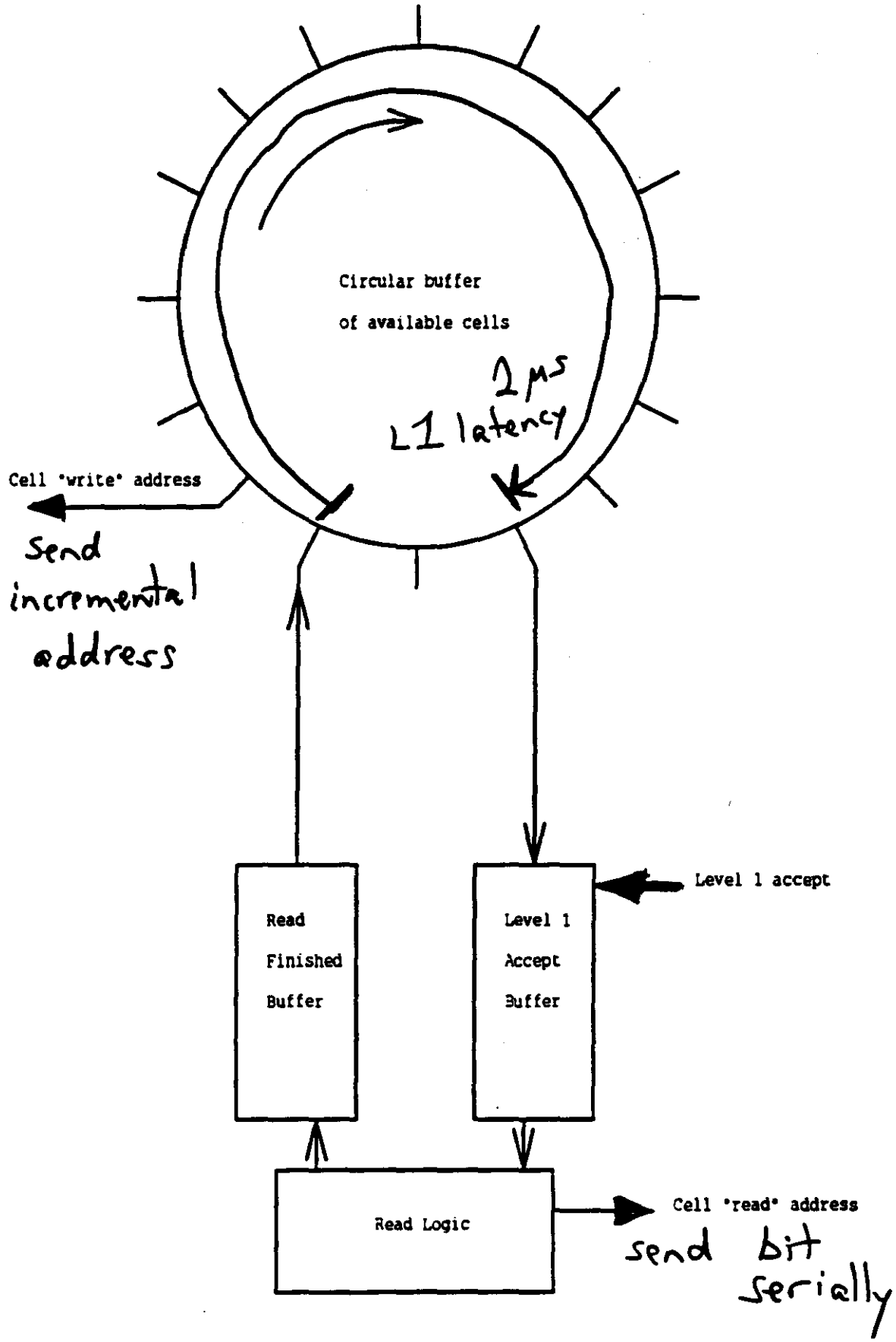
2 Maintain Fault Tolerance, Flexibility

- Programmable removal of dead AM cells.
- Programmable trigger sample pattern.

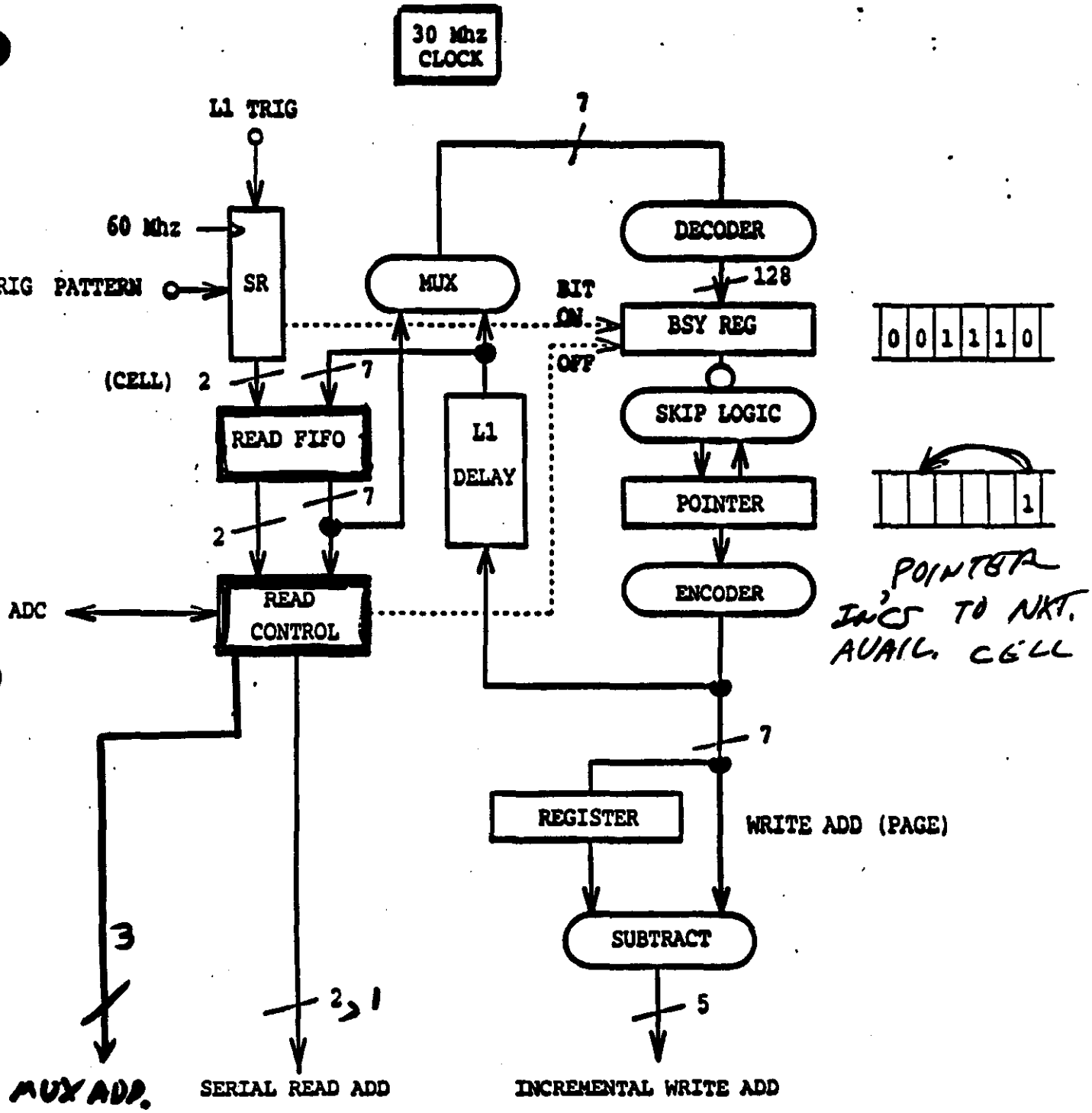
3 Use Commercially Available Technology

- Design AM Control with GA, FPGA.

Analog Memory Addressing

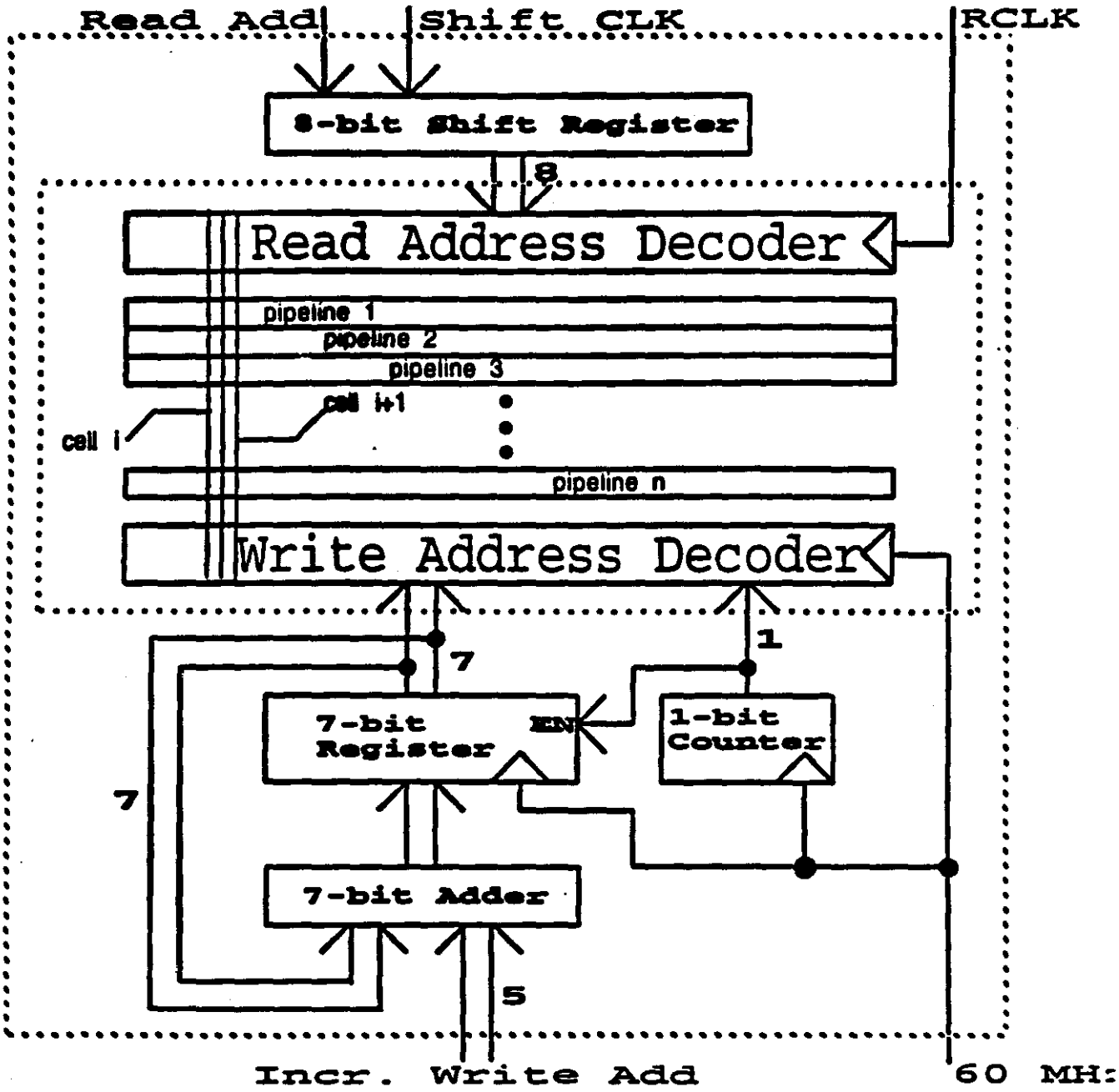


listgen



ANALOG MEMORY EXTERNAL CONTROL

ON CHIP DIGITAL CONTROL



1 SEPARATER RD., WR. STRUCTURES ON OPPOSITE SIDES OF CHIP.

2 ANALOG STRUCTURE IN MIDDLE WITH INPUTS, OUTPUTS AT OPPOSITE ENDS

3 ALL STRUCTURES ISOLATED WITH GUARD RINGS, AND HAVE PRIVATE VSS, VDD.

Output Board

- without zero suppression, each readout board produces data at rate of ≈ 28.8 MBytes/s (assuming 2 32-bit words / channel)

- assuming factor ≈ 10 suppression, crate produces $\lesssim 45$ MBytes/s

  ↳ need only one link to L2/crate

- Output Board collects & buffers data for crate, serves as interface to L1, control processes, provides local fan-out of clocks, etc,

  ⋮

L1 Sum Board

- form final trigger sums:

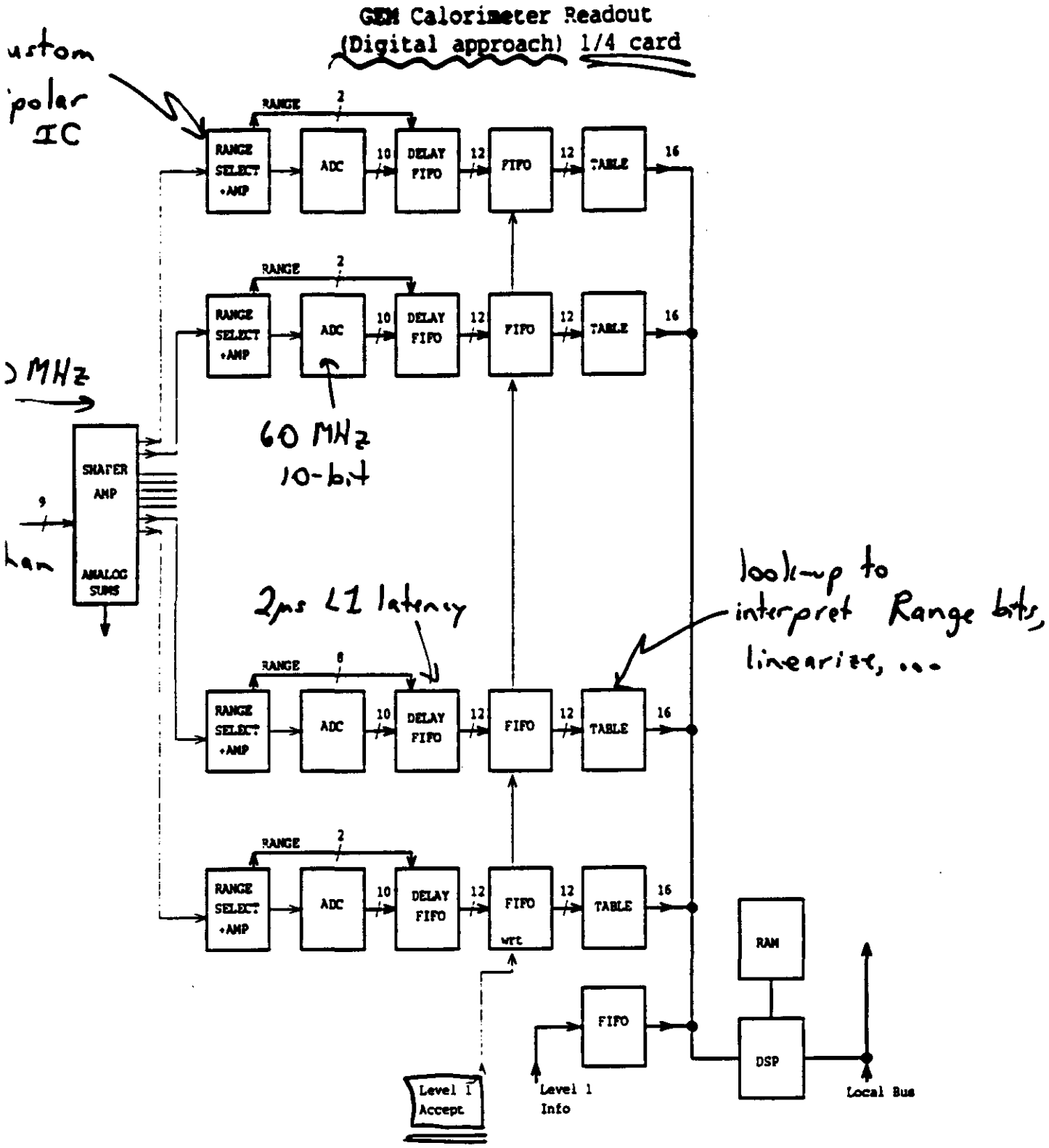
  [EMC .16 x .16] * 4

  HAC 1 .32 x .32 Isolation

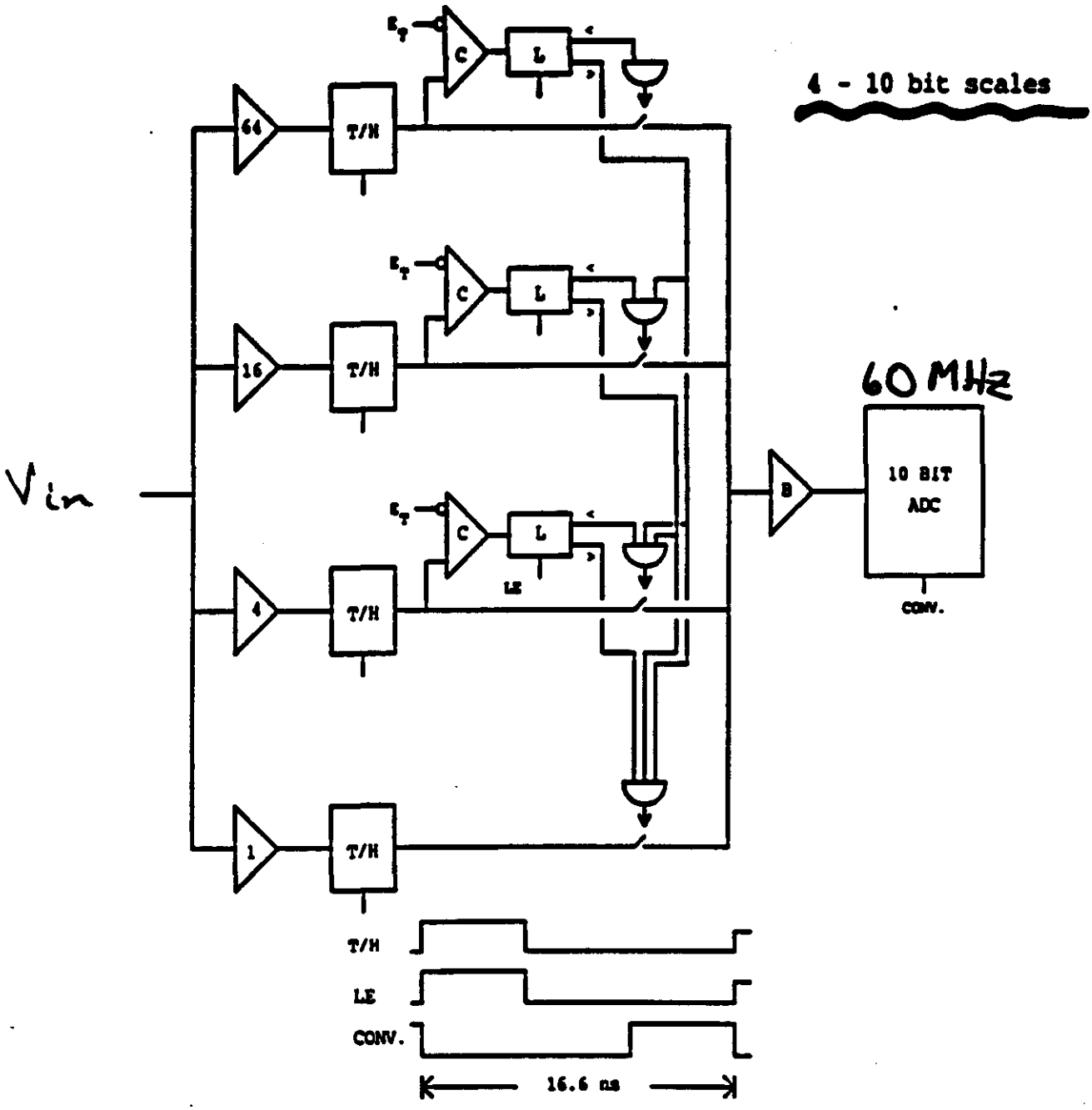
  HAC .32 x .32 Hadronic

- digitize and Xmit to Level 1 (6 links needed)

B: ONLY 1 VERSION OF READOUT BOARD, OUTPUT BOARD, L1 SUM BOARD NEEDED FOR ENTIRE SYSTEM!


GEM Calorimeter Readout
(Digital approach) 1/4 card
ustom
polar
IC
RANGE
2
RANGE SELECT +AMP
ADC
10
DELAY FIFO
12
FIFO
12
TABLE
16
) MHz
60 MHz
10-bit
SHAPER AMP
ANALOG SUMS
9
2μs L1 latency
look-up to interpret Range bits, linearize, ...
8
wrt
RAM
DSP
Local Bus
Level 1 Accept
Level 1 Info
GEM_FE6 1/13/93

ADC3


4 - 10 bit scales
60 MHz
Vin
64
16
4
1
T/H
C
L
LE
B
10 BIT
ADC
CONV.
T/H
LE
CONV.
16.6 ns

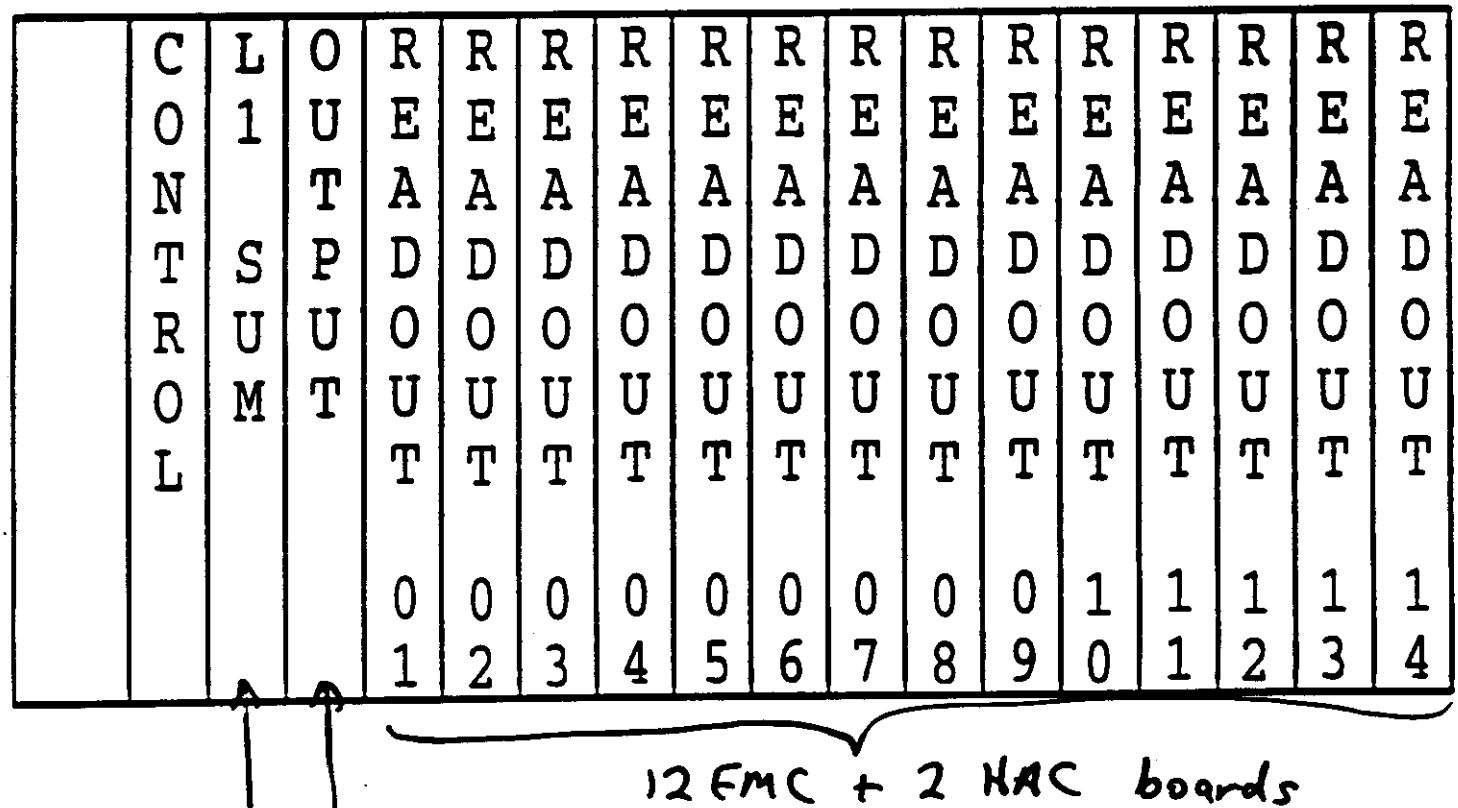
→ assume 36 ch/board, non-overlapping sums

→ .32 x .32 region of CAL maps onto 1 crate:

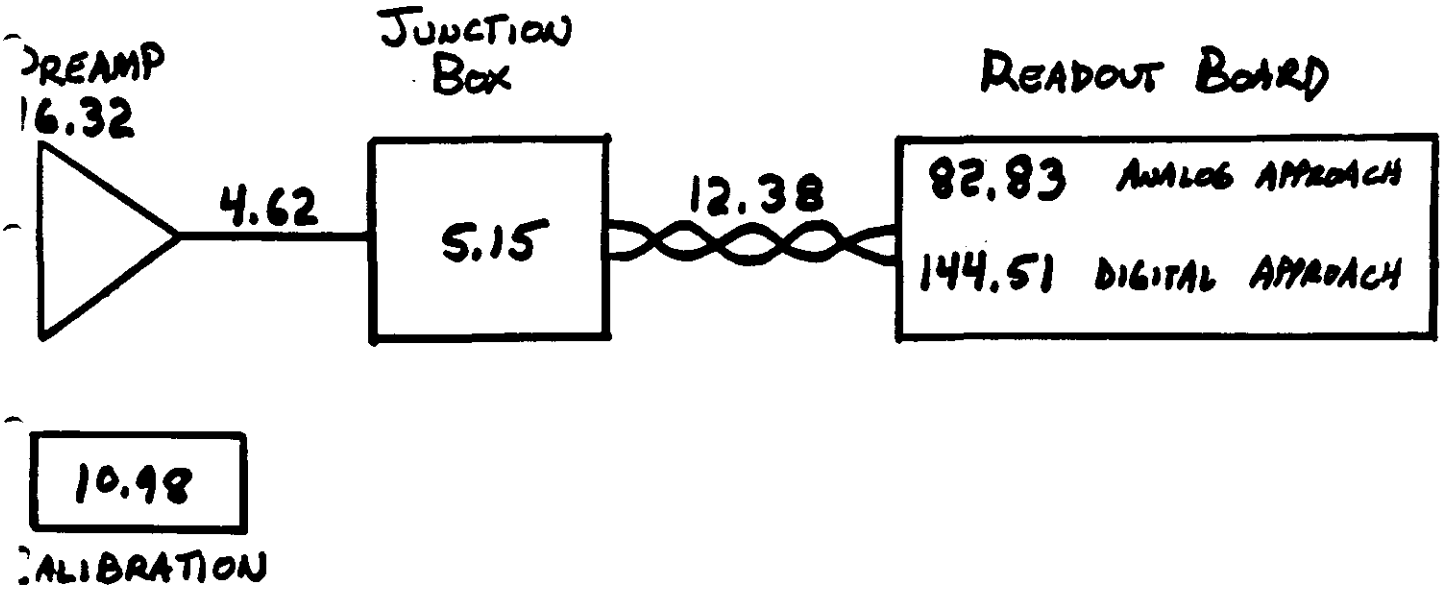
(i) 4 trigger towers (6 * 6 * 3) EMC
⇒ 4 * 3 = 12 boards

(ii) 1 trigger tower HAC (4 * 4 * 4)
⇒ 2 boards (using 32 ch each)

→ for EMC, add all 36 ch. for Level 1
→ for HAC, add top 16 & bottom 16 separately



Major Cost Breakdown



Readout Board Breakdown

Major Contributions

Analog Approach

Shaper	SCA	ADC	Mem	DSP	PCB
22.08	2.86	7.20	6.19	22.50	11.37

Digital Approach

Shaper	IC	ADC	Mem	DSP	PCB
22.08	5.69	50.00	24.00	22.50	11.37

GEM Calorimeter Readout Electronics

WBS #	Description	Subtotal	DGA	Total

Summary

WBS #	Description	Cost/Channel	Cost	DGA	Total	Total/Channel
50.02.3	Calorimeter Readout Electronics					
	Analog Pipeline Approach	179.37	21,524,197	5,242,472	26,766,668	223.06
	Digital Pipeline Approach	238.29	28,595,371	7,218,952	35,814,323	298.45
50.02.3.1	Design and Documentation	0.57	68,401	6,840	75,241	0.63
50.02.3.2	Prototype	20.96	2,515,621	575,436	3,091,057	25.76
50.02.3.3	Production					
	Analog Pipeline Approach	157.83	18,940,175	4,660,196	23,600,371	196.67
	Digital Pipeline Approach	216.76	26,011,349	6,636,676	32,648,025	272.07

Design of Low Noise Cable Driver

1. Introduction

In the GEM detector, liquid ionization will be the technology for the calorimeter. The signal from the calorimeter is amplified by a preamplifier inside the liquid and transmitted to the shaper and ADC via a long cable. Since the preamplifier can not drive a long cable, an IC cable driver is proposed to deliver the signal to the front end board. This report presents the initial results on the design of the driver done at the SSCL.

2. Low Noise Differential Cable Driver

Figure 1 is the block diagram of the electronics up to the front-end board, which is suggested by Dr. Veijko Radeka and Sergio Rescia from Brookhaven National Laboratory. The signal from the detector will be amplified by the preamplifier, which is located inside the detector. The output signal from the preamplifier will be passed on a 4 meters long 50 Ω cable to a linear cable driver just outside the calorimeter cryostat. The linear cable driver is responsible for transmitting the signal over a 30 meters long 100 Ω twisted pair cable to the front-end board for further processing. Both input and output of the driver are AC coupled. A 1 MΩ resistor connected from the input of the driver to its output is used to detect the proper DC offset of the preamplifier for diagnosis purpose. Based on the preliminary specifications of the calorimeter from BNL, the cable driver specifications are listed in Table 1.

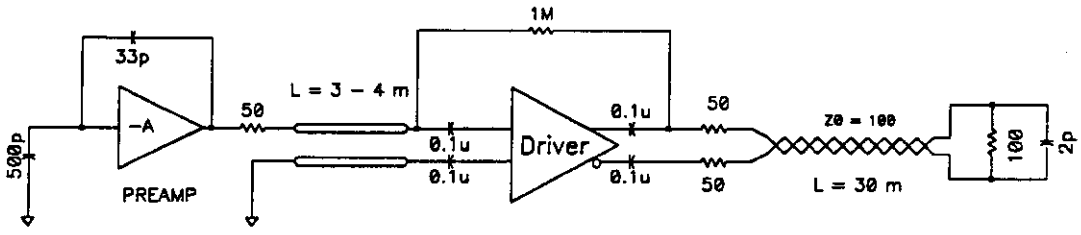


Figure 1. Block diagram of the preamplifier and driver electronics.

Table 1. Specifications for the Cable Driver

Parameters	Specifications
Input Impedance:	> 1 $K\Omega$
Output Impedance (differential):	100 Ω
Maximum Input Dynamic Range:	3 V
Rise Time at Input (10% ~ 90%):	< 15 ns
Maximum Differential Output:	±3 V
Equivalent Input Series Voltage Noise:	< 2 $nV/\sqrt{Hz}$
Integral Nonlinearity (±2 V):	< 0.02%
Fall Time at Output (10% ~ 90%):	< 400ns
Quiescent Power Consumption:	< 100 mW

From the specifications, we can derive the key circuit characteristics as follows:

1) The cable driver should have a small signal rise time less than 8 ns. This requires the small signal bandwidth to be in excess of 44 MHz. Since this circuit requires negative feedback, the bandwidth of the amplifier should be 3 to 5 times the above value to ensure the adequate transient response.
2) The large signal slew rate (for the rising edge) should be greater than 400 $V/\mu s$.
3) The driver is of single-ended input, differential output. Taking into account the line termination, actually a voltage divider, the gain of the cable driver should be ±2.

Because of the low noise requirement, the conventional 4-resistor feedback, in which a series resistor is inserted at the input, is not suitable for this application. Since its voltage noise directly contribute to the input noise, a resistor in series with the input should be avoided. A better performance can be expected from the circuit shown in

Figure 2, where VBB is the bias voltage for the gain stage. It uses a series-shunt feedback configuration, which is a good topology for achieving both fixed gain and low noise since the feedback signals are not directly applied to the input. It also provides the low output impedance needed to drive low resistance and capacitive loads. The gain of the driver will be determined by the ratio of the feedback resistance to the emitter degeneration resistance (*R11/R3* and *R12/R4*). The input differential pair achieves single-ended to differential conversion. The emitter degeneration resistance (*R3* and *R4*) of the input pair will determine the input dynamic range. High linearity can be achieved by increasing the loop gain of the feedback path, since the negative feedback will reduce the distortion by a factor equal to the loop gain. However, too much gain will decrease the bandwidth of the amplifier. Therefore a compromise has to be made to meet both linearity and bandwidth requirements. Following the differential input amplifier is the gain stage of the driver.

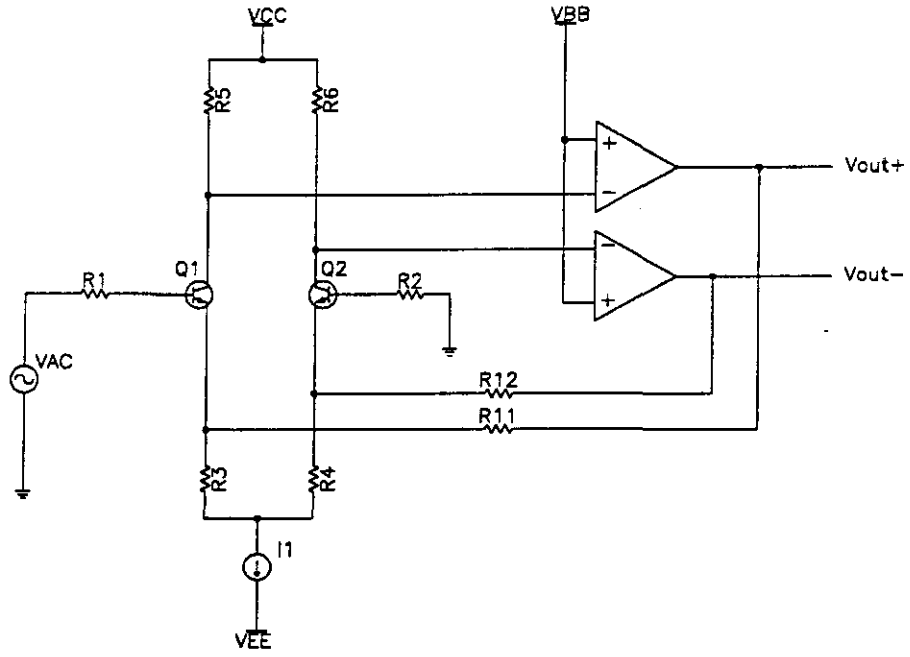


Figure 2. Simplified schematic of the cable driver circuit.

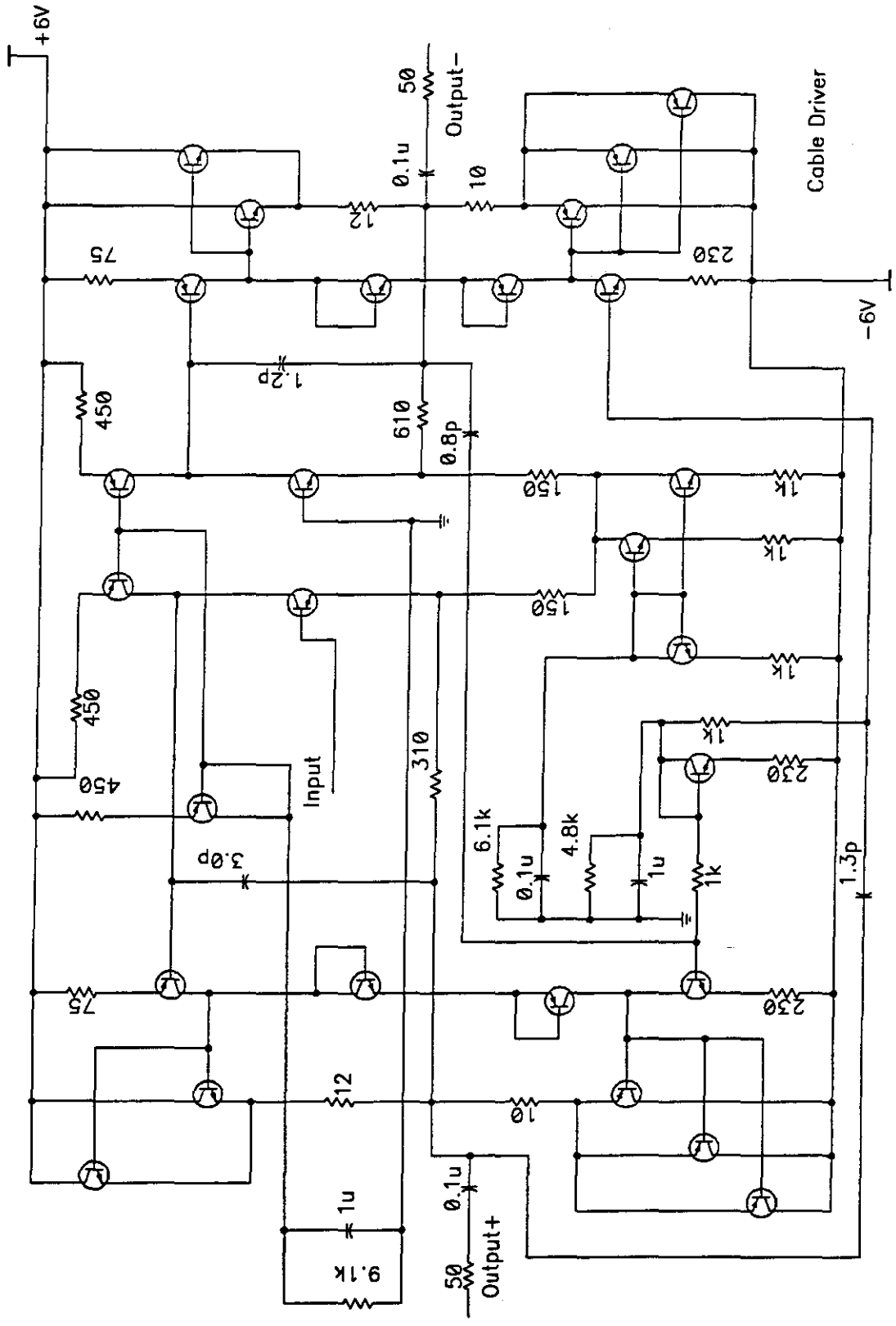


Figure 3. Schematic of the cable driver circuit.

3. Circuit Operation

The first step in implementing Figure 2 is to search for the appropriate process producing transistors with the desired characteristics. Since the source impedance is fixed to 50 Ω, bipolar transistors can be used in the input stage to achieve both low noise and high gain because the current noise is negligible compared to the voltage noise. For this application, we look for transistors which have high current gain β, low base resistance r_b and high cut off frequency f_T. The base resistance is in series with the input and it shows up as the voltage noise at the input. The high current gain will reduce the input base current, which in turn will reduce the input current noise. The reason for high f_T is that the high frequency noise will be far out of the operating frequency band because the upper frequency corner, where noise starts to increase with frequency, is proportional to $f_T/\sqrt{\beta}$. In addition, a high cut-off frequency is a requirement for high speed applications. For these reasons we picked Harris Semiconductor's HFA3XXX series transistor array as one of the preferred technologies to design this cable driver. We found that the Tektronix's QuickTile process does not supply pnp transistors that are good enough for this application.

Figure 3 shows the actual implementation of the simplified circuit in Figure 2. Instead of the resistive loads, the differential input stage uses active loads. This makes the whole input stage behave as current mode amplifier when the differential input stage is connected to the second stages, which are in common emitter configuration. Because the output nodes of the input stage have very small voltage swing, the Miller effect is minimized. This way the high frequency performance is improved. In constructing the current sources and current sinks, attention was paid to their noise contribution. The latter is decreased by using emitter degeneration. However, too much emitter degeneration deteriorates the high frequency performance of the active load. A tradeoff has to be made between low noise and speed. Following the input differential stage is the main gain stage, a the common emitter configuration. The output stages are of the

conventional push-pull type. Feedback is taken directly from the outputs and applied to the emitters of the input pair. Since the driver is operated under large feedback, circuit stability is obtained with Miller compensation. The capacitance of the compensation capacitors is chosen to result in a phase margin of 50°, which is the compromise of speed and power consumption. In order to reduce the DC power consumption and maintain adequate fast large signal response, dynamic biasing is utilized in the second gain stage. A small positive feedback is taken from the other polarity output through a small capacitor to the base of the active load of the second stage. It helps to remove the base storage charge when a signal transition is fast and large. When a very fast and large signal is applied to the circuit, one of the transistors in the second gain stage goes into cut-off. The base storage charge in the output npn transistors will need to be removed in order for it to switch off. In the mean time, the base of the output pnp transistor needs to source current to pull down the output. All these charges will have to flow through the second gain stage's active load. The injection of the charge into the base of the active load from the positive feedback will momentarily increase the flow of current in the collector and achieve faster switching. The amount of the feedback is determined by the size of the capacitor and the resistor connected to base of the active load.

One of the objectives in this design is to get the lowest noise possible. With the present circuit configuration, noise comes mainly from the input stage, the active loads and feedback resistors. In addition, the DC biasing of the input stage is also important. A large bias current will increase the transconductance of the first stage, therefore it will reduce the input referred noise voltage produced by the collector shot noise. However, this will also increase the power consumption. The biasing is chosen to guarantee an adequate slew rate combined with low power consumption. Decreasing the emitter degeneration resistance of the differential pair will increase the gain of the input stage and thus decrease the noise contribution from the active load and the feedback resistanors. However, the small value of the emitter degeneration will reduce the dynamic range of the

input stage. To maintain the gain of driver, the feedback resistance will also have to be reduce, which will load the output stage at both DC and transient operation. Too much DC loading will increase the power consumption of the circuit. This is another trade-off to be made and requires intensive computer optimization.

4. Simulation results

In the simulation, SPICE models for the high frequency transistor arrays from Harris Semiconductor are used. The npn and pnp transistors have a very low noise figure of about 1.7 dB. The designed circuit was intensively simulated and optimized to achieve the desired specifications. The final values for the individual components are shown in Figure 3.

The driver has an average gain of +1.9988 and -1.9920. Figure 4 gives the small signal frequency response of the driver. It has a bandwidth of about 210 *MHz* for the positive output and 200 *MHz* for the negative output. The low frequency roll-down is due to the DC blocking capacitors. Figure 5 is the output noise measured at the receiver. The input referred noise is about 2.9 $nV/\sqrt{Hz}$. An alternative configuration for the input stage is under exploration and could further reduce the input referred noise.

The open loop gain of the driver is of much interest. To simulate the loop gain of the driver, the loops are broken at the emitters of the input transistors. To account for the loading of feedback, the equivalents of the feedback resistors are placed at the points where feedback is broken. The circuit is then used to find out the loop gain. Figure 6 and Figure 7 show the simulation result for both the positive and negative outputs. The driver has a loop gain around 65 *dB* for the positive output and 60 *dB* for the negative output respectively. The phase margin is 62° for the positive output and 57° for the negative output. Therefore the circuit has the necessary stability.

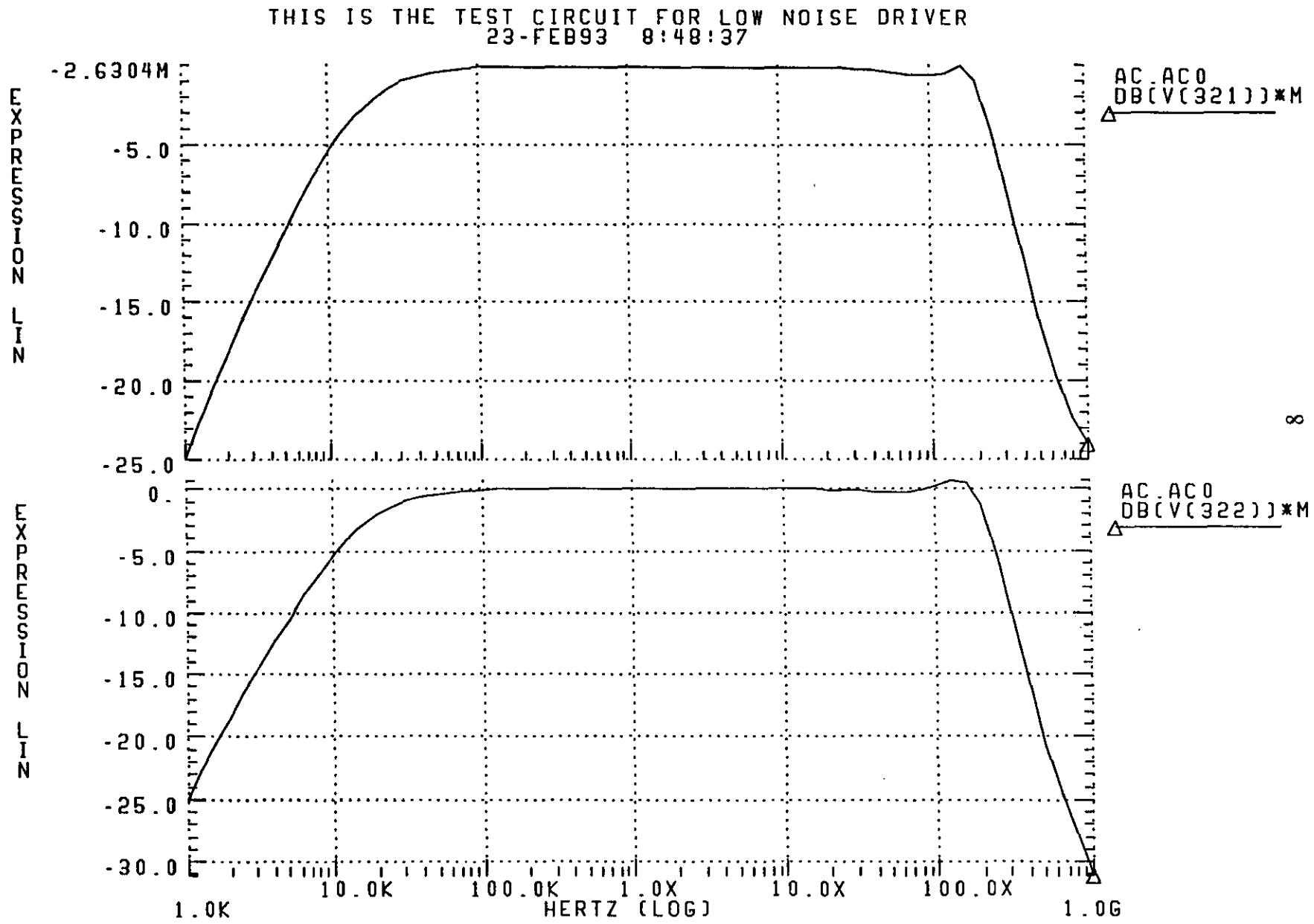


Figure 4. Frequency response of the cable driver.

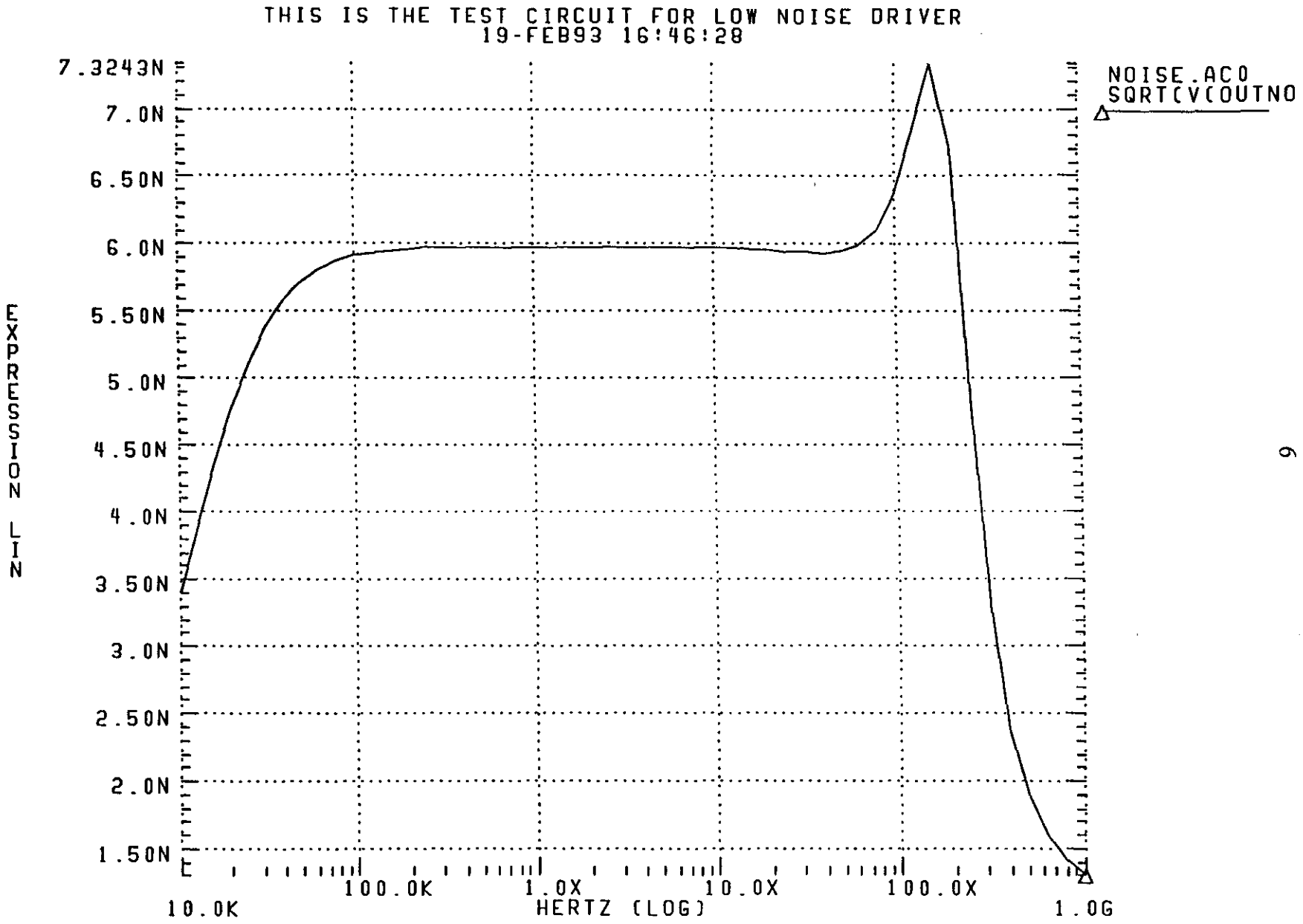


Figure 5. Output noise power spectra of the cable driver.

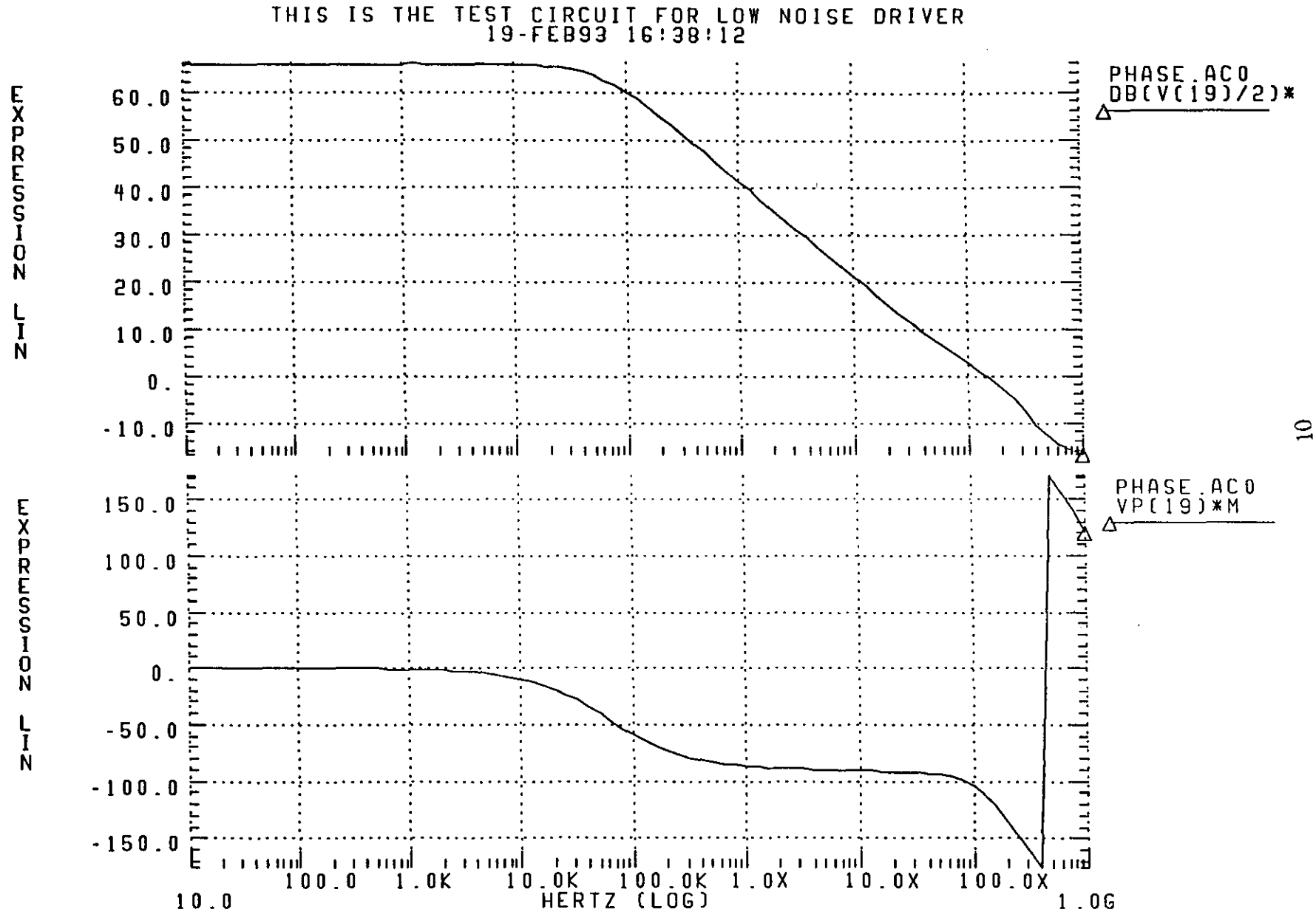


Figure 6. Loop gain and phase shift of the positive output of the driver.

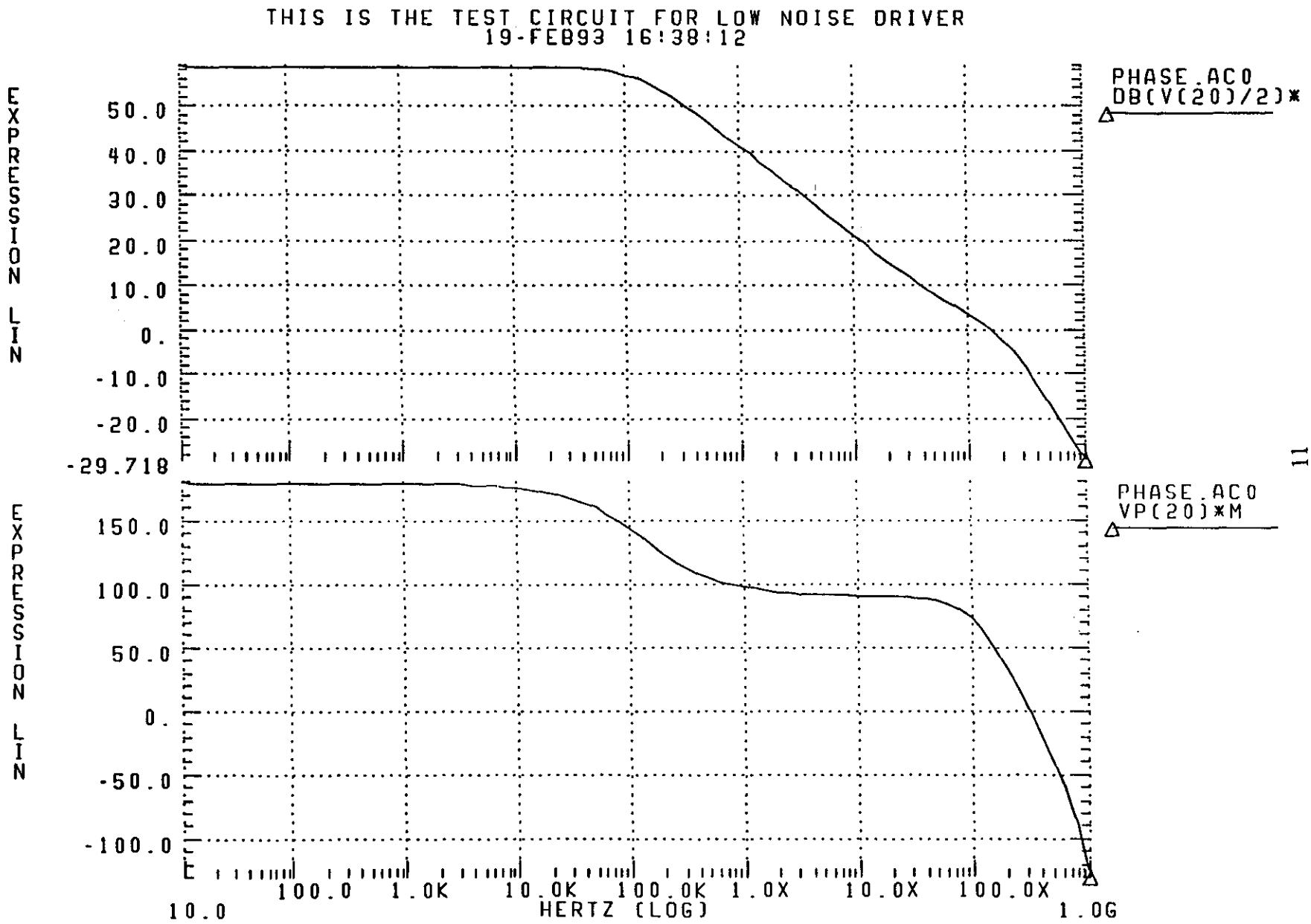


Figure 7. Loop gain and phase shift of the negative output of the driver.

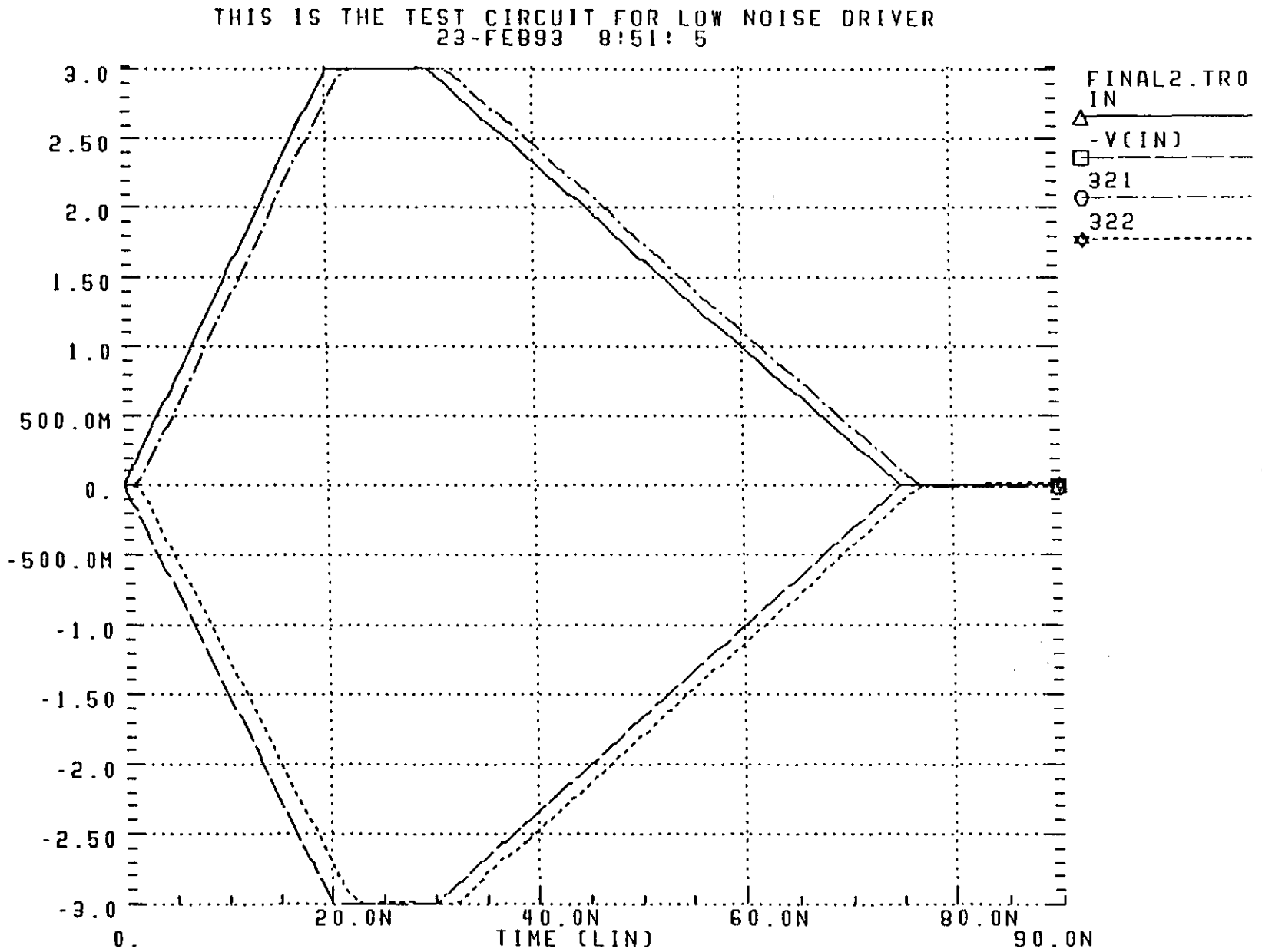


Figure 8. Transient response of the cable driver

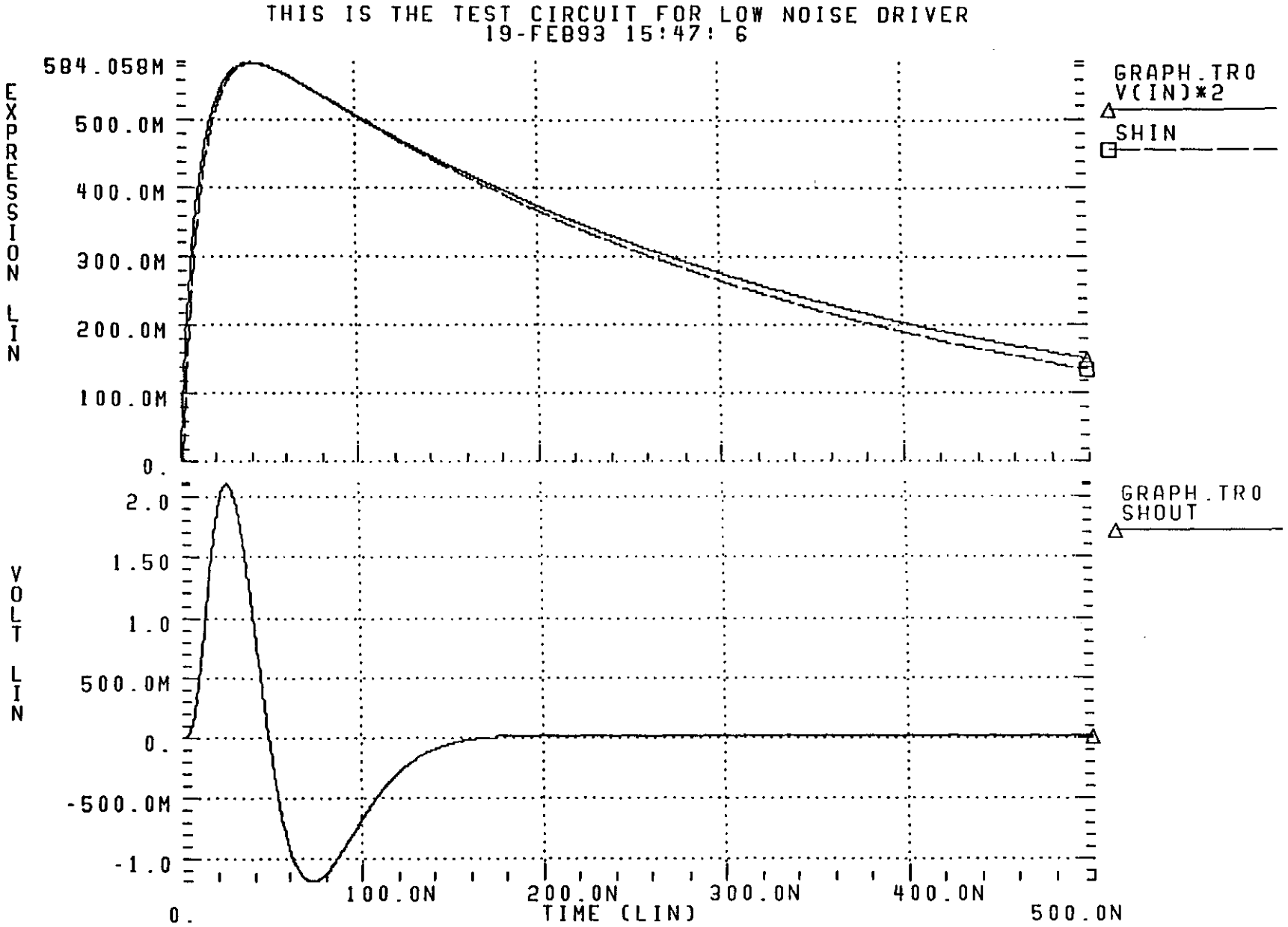


Figure 9. Typical δ response of the whole electronic chain including preamplifier, cable driver and shaper.

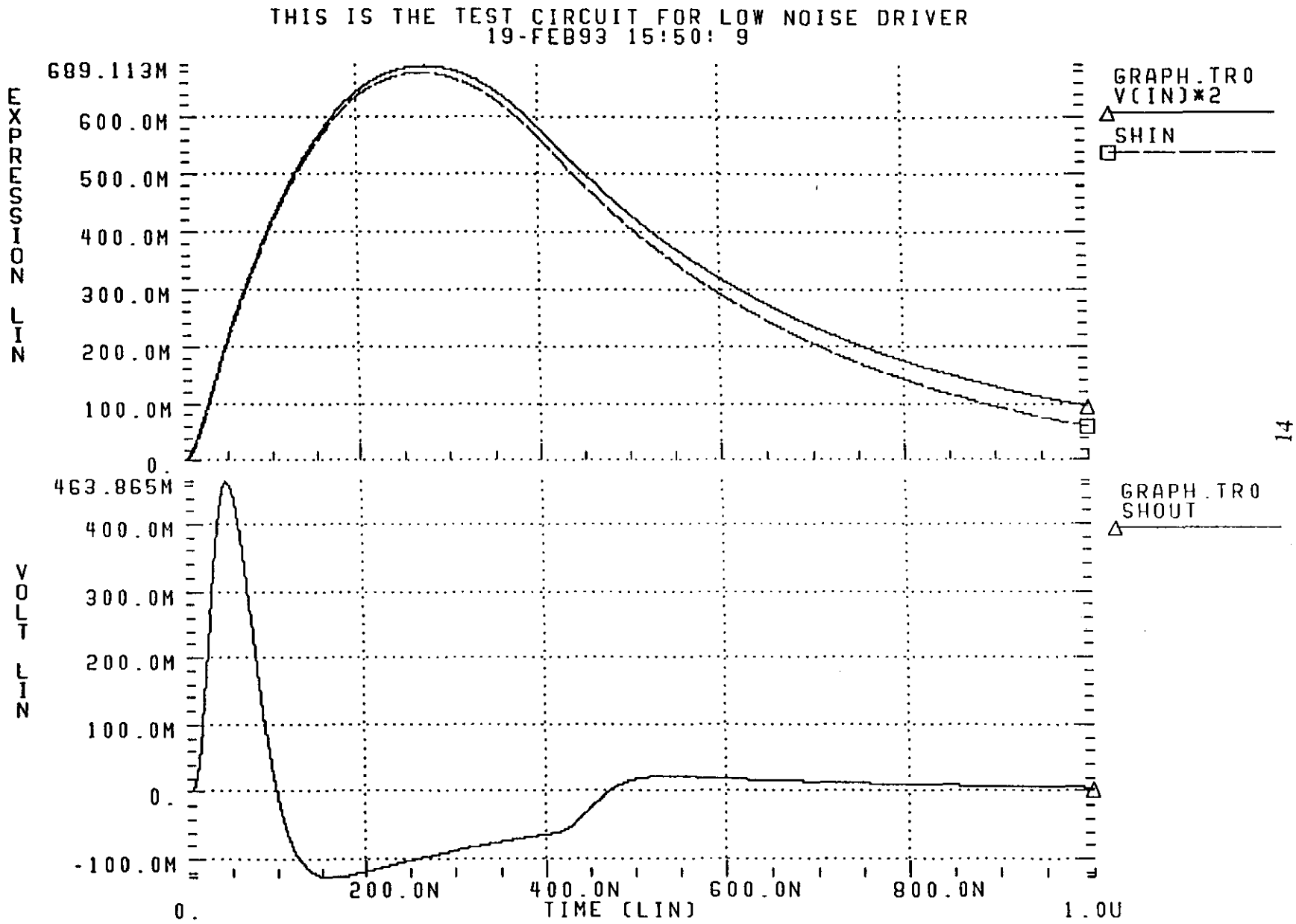


Figure 10. Typical waveform of the whole electronic chain including preamplifier, cable dirver and shaper when driven by a triangle current pulse with a drift time of 400 ns.

Although the driver circuit has a bandwidth around 210 MHz, its large signal behavior is mainly limited by the slew rate. The slew rate of the circuit is about 600 $V/\mu s$ for the rising edge and 200 $V/\mu s$ for the falling edge. This is the result of the compromise between power consumption and speed. If necessary, the speed can be improved by sacrificing the power consumption, or vice versus. Figure 8 shows the transient response of the driver circuit when driving it with a pulse of 3 V magnitude. The circuit has a delay of 1.25 ns for the positive output and 1.66 ns for the negative output. The output waveform has about the same rise time as the input.

To study integral nonlinearity, ideal models for the preamplifier and the shaper are used in the simulation. Therefore, the slewing effect of the shaper can be taken into account in the whole front electronics chain for the integral nonlinearity. The shaper is $CR^2 - RC^2$ S-G type with a peaking time around 24 ns for δ response. Figure 9 is a typical result of the wave form at the input and output of the driver as well as the output at the shaper response to δ impulse. Figure 10 is the response of the circuit to a triangle input current pulse assuming a drift time about 400 ns to simulate the real liquid ~~Krypton~~Ar detector signal. Examining the peaking at the output of the shaper, we found that the driver passes the input rising edge very faithfully from the input to the output. On the falling edge, there is some attenuation due to the DC blocking capacitors, which is inevitable. Therefore, the output peaking of the shaper is almost at the same time (only about 0.3 ns difference) for the input signal from 50 μV to about 3 V. The maximum output of the shaper is then measured for the calculation of integral nonlinearity, which is shown in Table 2. V_{in} is the voltage at the input of the driver, V_{shout} is the output at shaper which is located at the other end of the receiver. We assume an ideal receiver in this simulation. The integral nonlinearity is calculated as half of the maximum deviation from the line connecting the point of 10 mV and 2 V, divided by 2 V. The integral nonlinearity is found to be less than 0.013%.

One of the problems that needs to be addressed is the effect of process variation on the performance of the circuit. For a typical bipolar process, the process variation will be up to ±20% for resistors and ±10% for capacitors around their nominal values. To make sure the design will produce a working chip the first run, these variation should be taken into account in the simulation. Process variation information is provided by the ASIC vendor. For the UHF1 process from Harris Semiconductor, the variation is -21% to +37% for the resistors, and -13% to 17% for the capacitors. The variation in the transistors is not available for the moment so their contributions will not be accounted for this time. Since the driver circuit has very large feedback, variation in the transistor gain should not post a serious problem. In the design process, worst cases are studied for all the possible extremes. We then optimize the circuit so that it works for all the variations due to processing. The circuit now performs very well in the key characteristics, such as the slew rate, noise, and integral nonlinearity. Even for the largest simulated deviations maximum gain varies less than 0.68%. Variation of the phase margin is typically less than 5°. There is more than 45° safety margin in closed loop. However, this variation is constant once the chip is installed and it can be properly calibrated in the system. We also studied the variation of the delay of the driver. It varies up to ±0.4 *ns*. Fortunately, around the maximum of the shaper output, the pulse height changes slowly. Therefore delay variations do not introduce much difference in the magnitude if the signal is sampled right at peak. But this should still be corrected by some form of calibration in the system design.

The temperature variation is also considered. Since the SPICE model from Harris did not include the parasitic temperature effects, we only studied the temperature influence on the transistors and the resistance. The simulation was performed on the whole preamplifier, driver, and shaper chain. Since the preamplifier and shaper circuits are ideal models, they will not contribute any temperature drift. It is found that the change in the gain is less than 0.02% for temperatures ranging from 25°C to 85°C. As the temperature

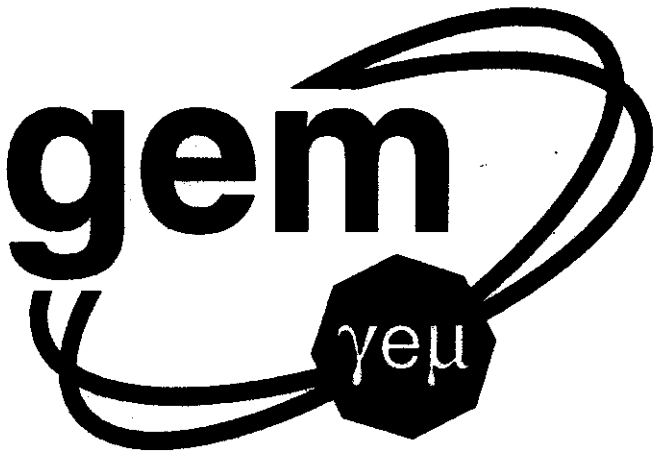
Table 3. Specifications and Simulation Results

Parameters	Specifications	Simulation
Input Impedance:	> 1 $K\Omega$	>50 $K\Omega$
Output Impedance (differential):	100 Ω	100 Ω
Input Dynamic Range:	3 V	3.1 V
Rise Time at Input (10% ~ 90%):	15 ns	15 ns
Maximum Differential Output:	±3 V	±3.1 V
Equivalent Input Series Voltage Noise:	< 2 $nV/\sqrt{Hz}$	2.9 $nV/\sqrt{Hz}$
Integral Nonlinearity (±2 V):	< 0.02%	< 0.013%
Fall Time at Output (10% ~ 90%):	< 400 ns	30 ns
Quiescent Power Consumption:	100 mW	140 mW

drift occurs very slowly, the blocking capacitors take care of DC drift and the output signal should not be affected. Further study on this problem will be done once we establish a proper process to obtain all the necessary information, such as the parasitic temperature variations of the transistors.

4.4 Summary

We have designed a differential low noise driver based on Harris Semiconductor's UHF1 process. The initial design shows a very promising circuit topology which is capable of achieving most of the specifications or being close to them. Table 3 is a summary of the cable driver's specifications and the simulation results. A refinement of the design will be carried out once a proper process is selected for fabrication. As for now, we are proceeding to make a prototype board using Harris Semiconductor's Array transistors to measure some of the key performance of the driver.



Presentation by:

Daniel Marlow

GEM Electronics Design Review

OVERVIEW of CSC Electronics

Presented by:
Daniel Marlow
Princeton University

SSC Laboratory
February 23, 1993

General CSC System Requirements

The CSC readout electronics must:

- Measure the charge on each strip with sufficient accuracy that the electronic contribution to the position resolution is rendered negligible.
- Measure single-hit times with a resolution that is better than one bunch crossing time (16.7) ns.
- Provide a reduced set of accurately timed signals as input to the Level 1 muon trigger.
- Identify and reject random backgrounds induced by neutrons and other debris not associated with the muon track of interest.
- Conform to the timing and readout-rate requirements of the GEM Trigger/DAQ system.
- Be suitable for chamber mounting.
- Be inexpensive on a per-channel basis.

Electrical Specifications for the CSC Readout

Sys. Section	Parameter	Value	Notes
Readout	Equivalent Input Noise	$< 1500\ e^-$ rms	1
	Pulse Peaking Time	400 ± 100 ns	2
	Overall System Gain	0.4 fC/Count	3
	Dynamic Range	10 bits	4
	Cross Talk	< -50 db	
	Readout Rate	100 kHz	5
	Readout Latency	$< 100\ \mu s$	6
Trigger	Input Threshold	16 fC	7
	Timing Jitter	< 4 ns rms	8
	Time Walk	< 4 ns	9
General	Temperature Range	20 ± 5 °C	10
	Power Per Channel	< 100 mW	11
	Rad. Hardness: Ionizing	tbd	12
	Rad. Hardness: Neutrons	10^{14}cm^{-2}	13

Notes:

1) A level of 2000 e^- (0.32 fC) equivalent input noise produces an ADC "pedestal width" of 0.8 counts. Noise level applies to 100 pf input capacitance and 400 ns shaping time.

2) Peaking time for "semi-gaussian" shaping. Transfer response of system is given by

$$H(s) = \frac{s\tau}{(1 + s\tau)^{n+1}}$$

where $n\tau$ = peaking time and n is the number of integrations. The most likely choice is $n = 4$, since $n = 2$ leads to a long uncancelled tail.

3) Ratio of input charge to ADC least count. This value depends on such things as the value of the feedback capacitor in the charge-sensitive preamplifier, the gain of the shaping amplifier, the ballistic deficit factor, and the least-count sensitivity of the readout ADC. For preamplifier-only designs, the required conversion gain is 5 mV/pC (10 mV/pC desirable).

4) Ten-bit range will keep a larger fraction of the Landau tail on scale and will allow operation over a wider range of chamber gas-gains.

5) This is maximum average rate of Level 1 accepts.

6) Maximum time between Level 1 accept and availability of data at readout output port. In data driven architectures, this drives the ADC conversion speed.

7) This will depend on the effective gain of the timing path and the input offset of the comparator used to generate the logic pulse.

8) Time jitter for fixed input amplitude of 40 fC.

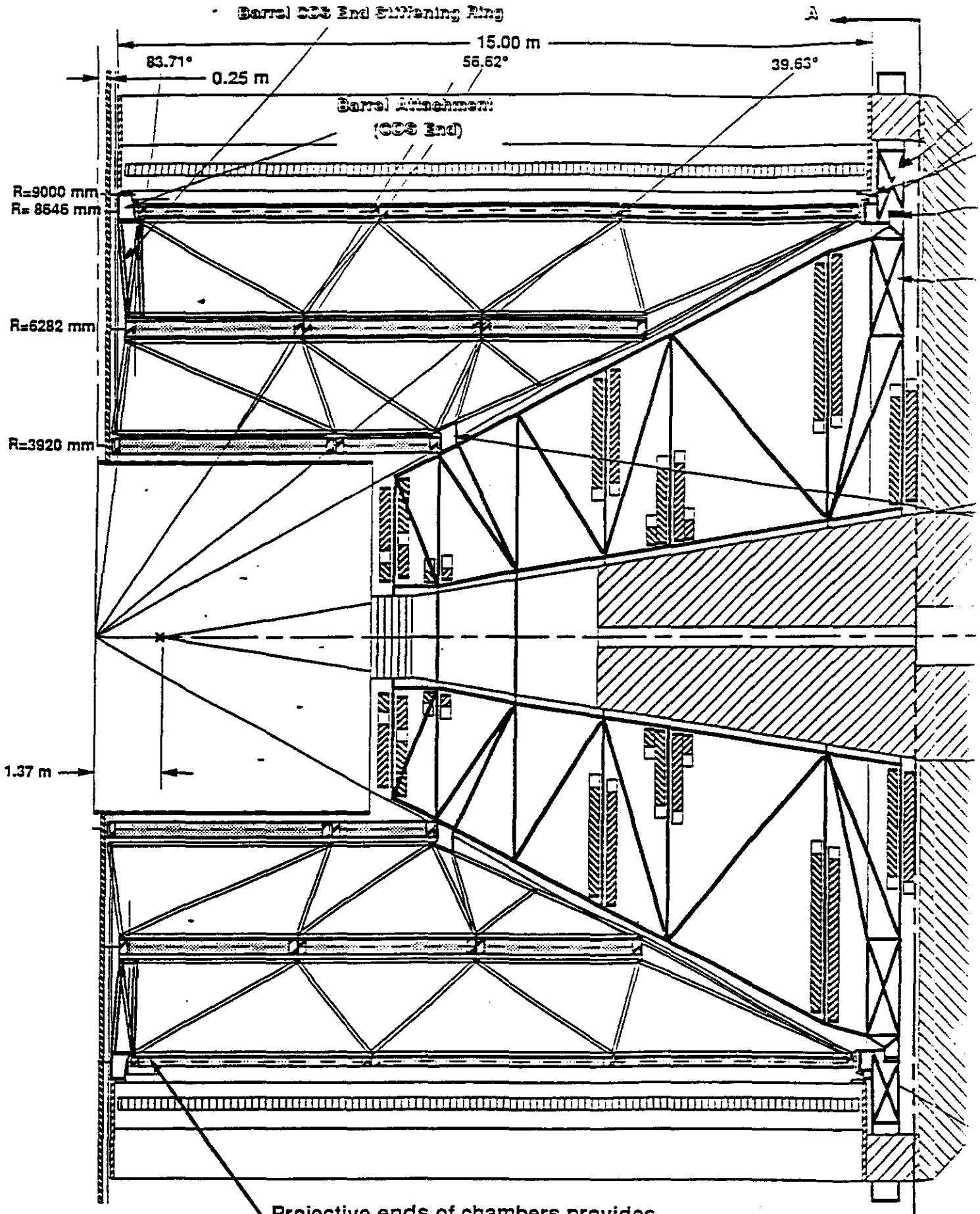
9) Variation in comparator firing time over a range of input pulses between threshold and 10 times threshold (20 times threshold if an 8 fC threshold is used).

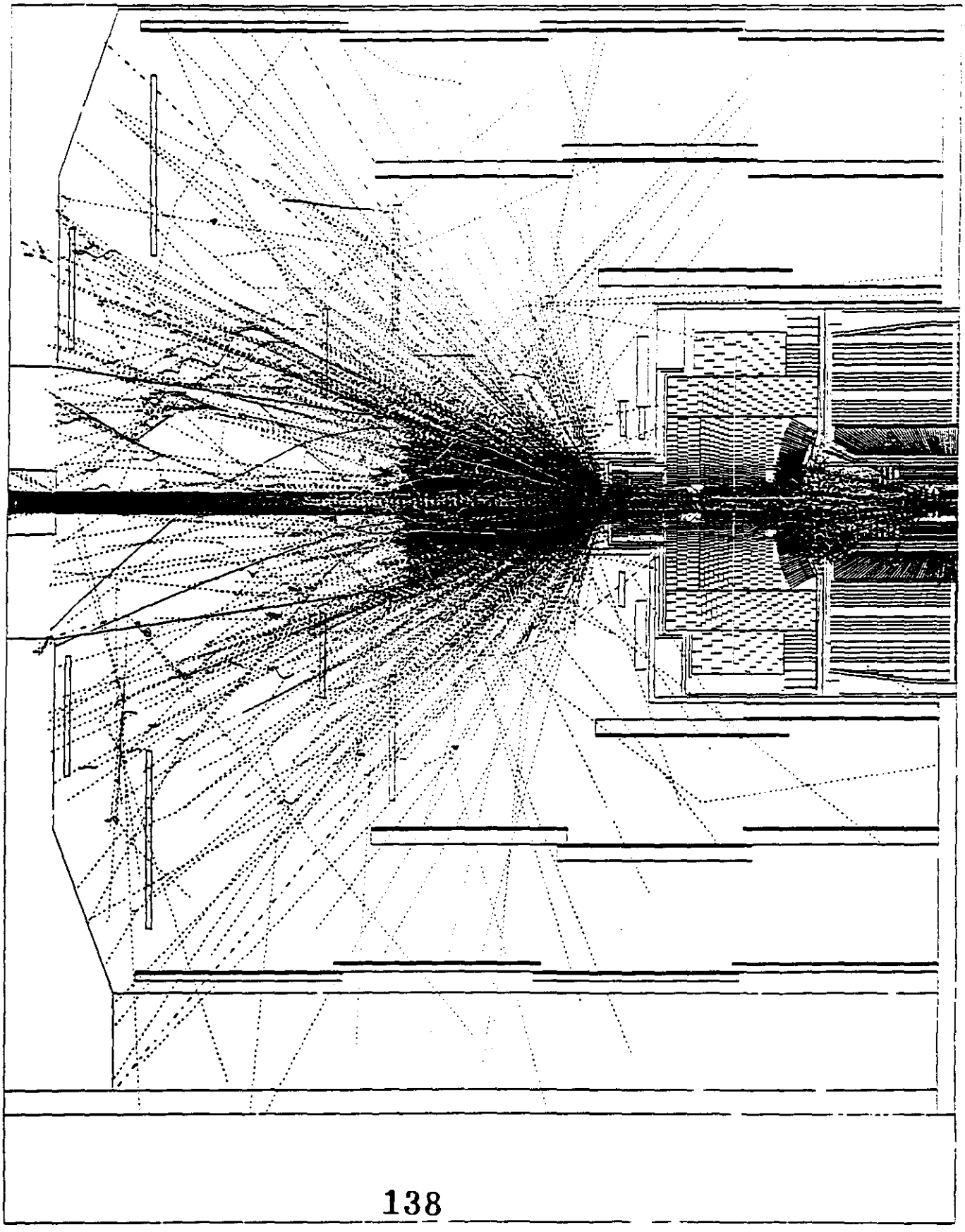
10) Ambient temperature range over which all other system specifications must be met.

11) Total power for on-chamber electronics divided by total number of channels. Includes on-chamber readout and trigger sections.

12) The muon electronics are situated outside of the calorimeter and therefore are expected to experience only low radiation levels. This remains to be verified.

13) Calculations are in progress. The stated value assumes a neutron fluence scenario of $F_n = 10^6 \mathrm{cm}^{-2}\mathrm{s}^{-1}$ at $\mathcal{L} = 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for ten SSC-years.


Barrel CSC End Stiffening Ring
A
15.00 m
83.71°
0.25 m
56.62°
39.63°
Barrel Attachment
(CSC End)
R=9000 mm
R= 8646 mm
R=6282 mm
R=3920 mm
1.37 m
Projective ends of chambers provides
necessary space for support structure



Neutron Rates

- Currently very uncertain
- Product of three factors

$$R = \varepsilon_n F_n A \equiv r_n A$$

where

ε_n = detection efficiency
F_n = fluence
A = strip area

The efficiency

measured ↙

calculated → $2 \times 10^{-4} < \varepsilon_n < 5 \times 10^{-3}$

the fluence (TN 92-91)

z = 575cm ↙

z = 235cm → $10^3 < F_n < 10^5$ cm^{-2}s^{-1}

the area

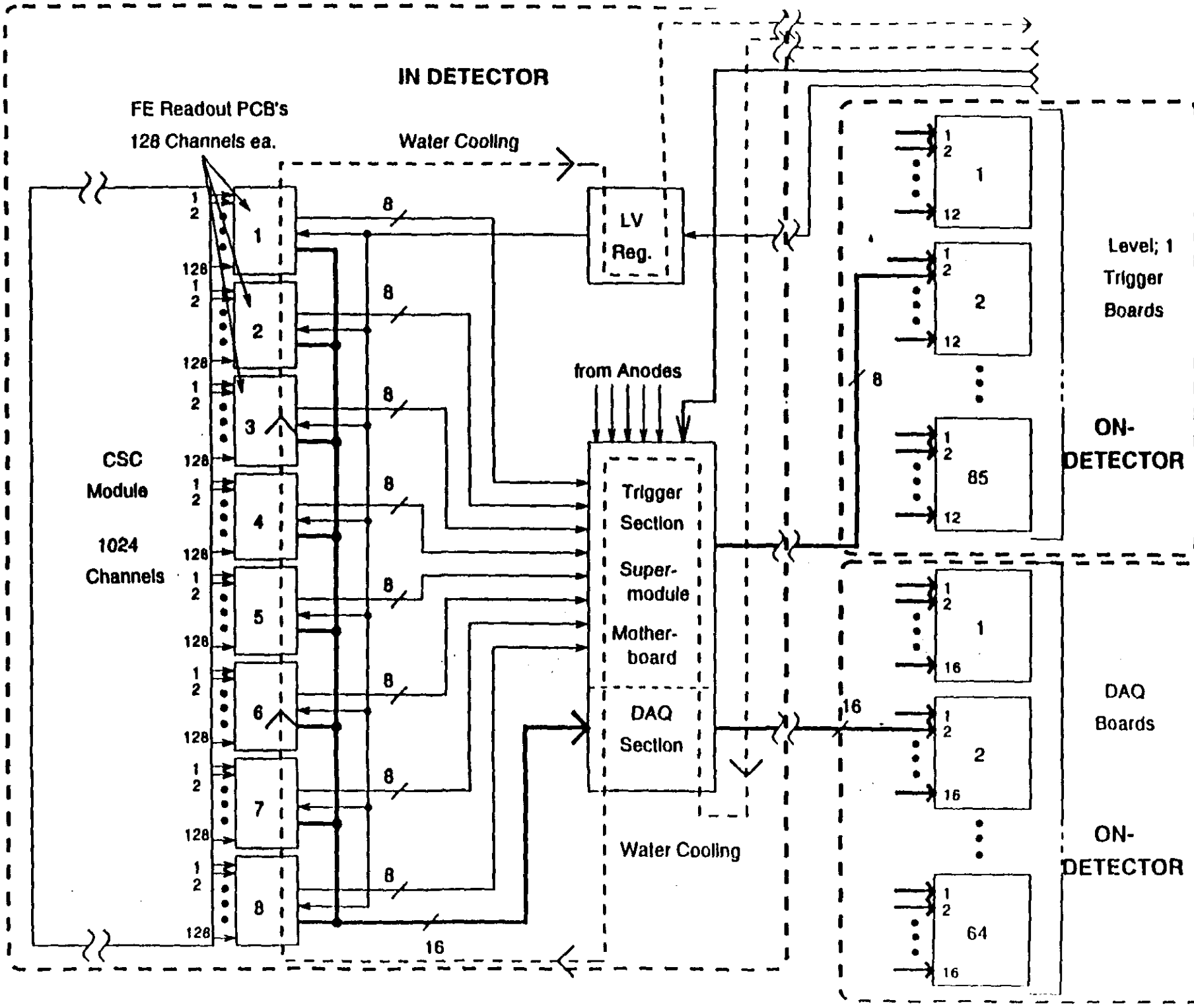
$$A = \ell w \simeq 300 \times 0.5 = 150 \text{ cm}^2$$

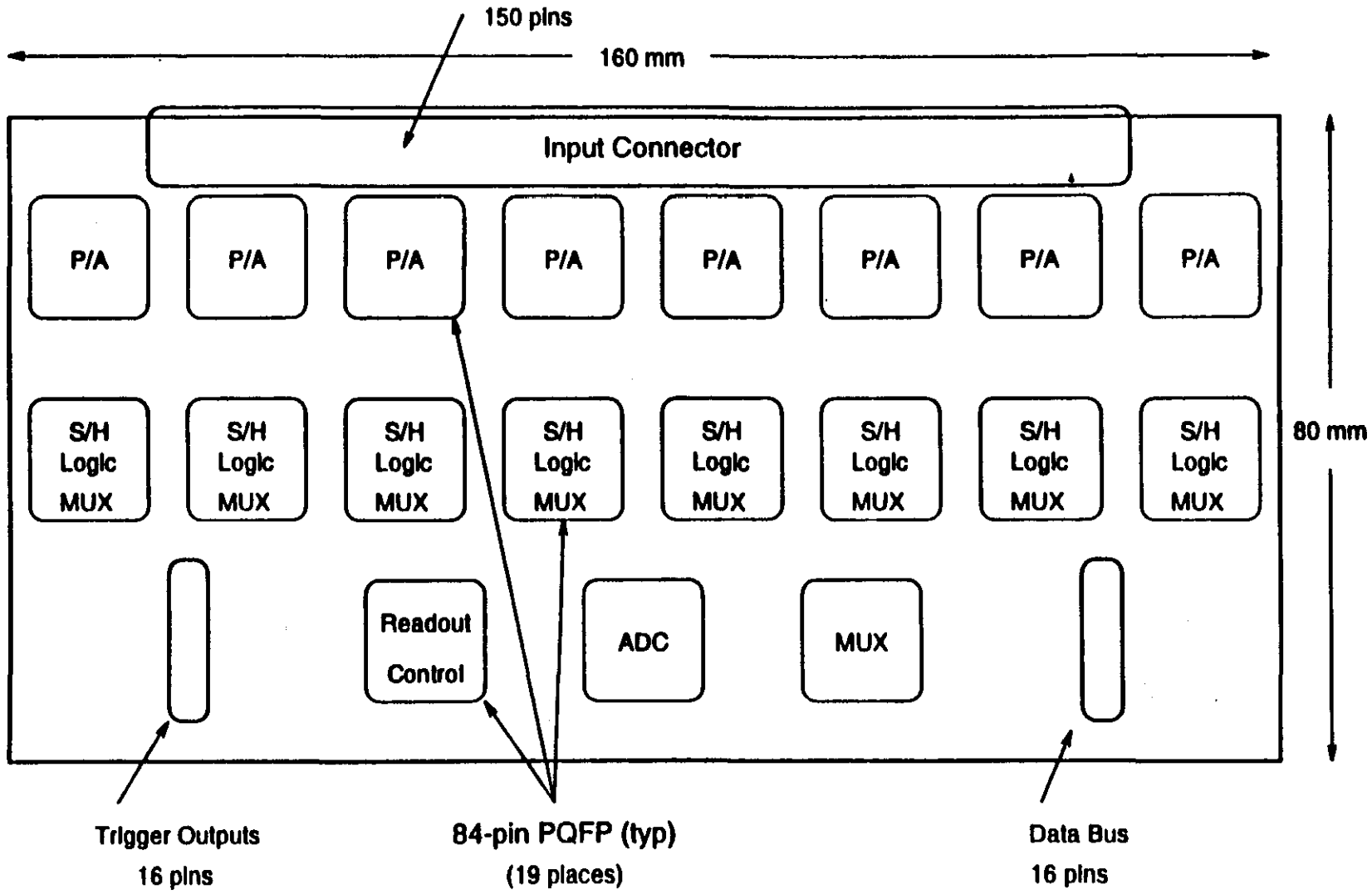
yielding a rate per strip (assuming $\varepsilon_n = 0.5\%$ of

$$0.75 < R < 75 \text{ kHz}$$

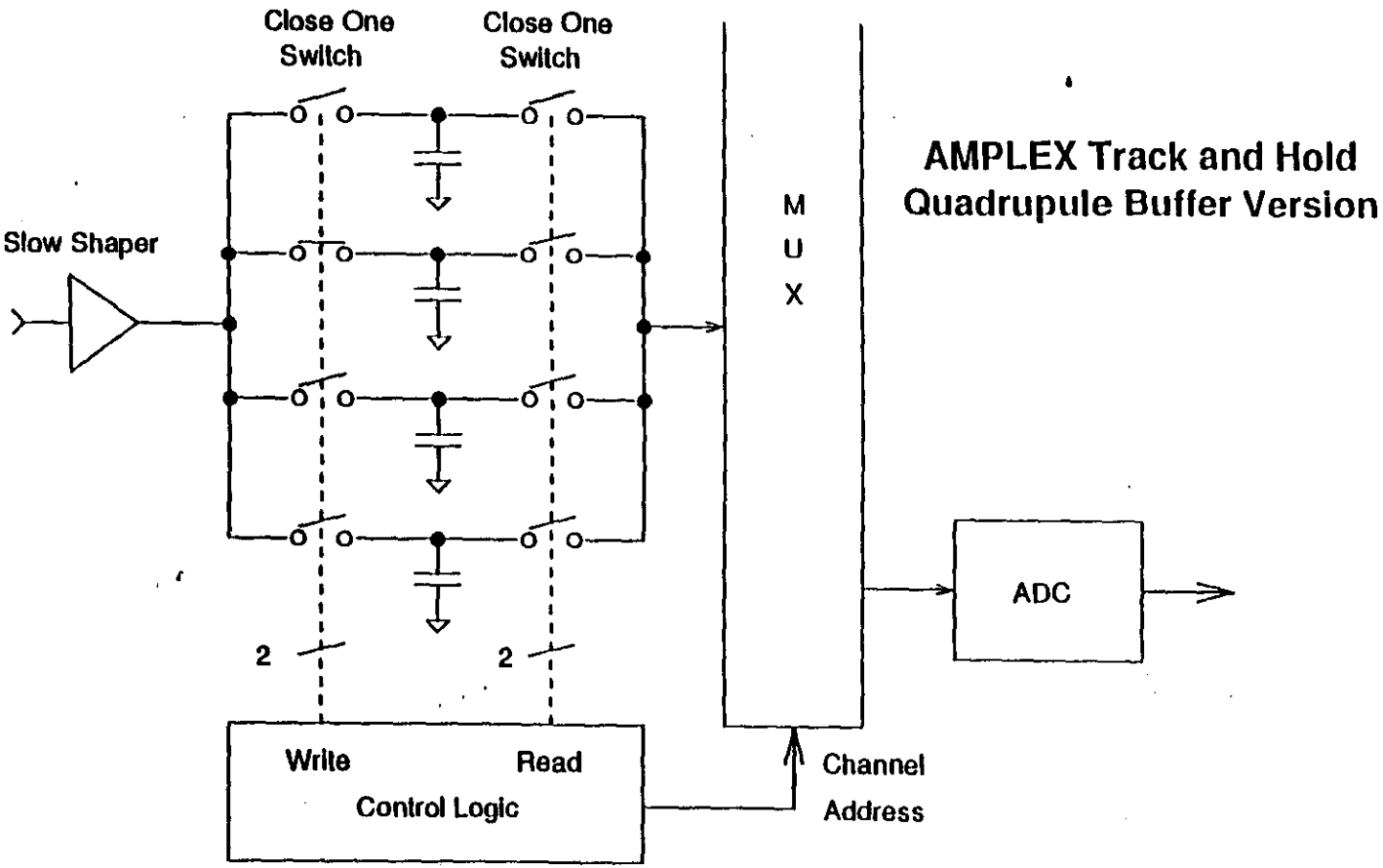
note that the corresponding rates per unit area are

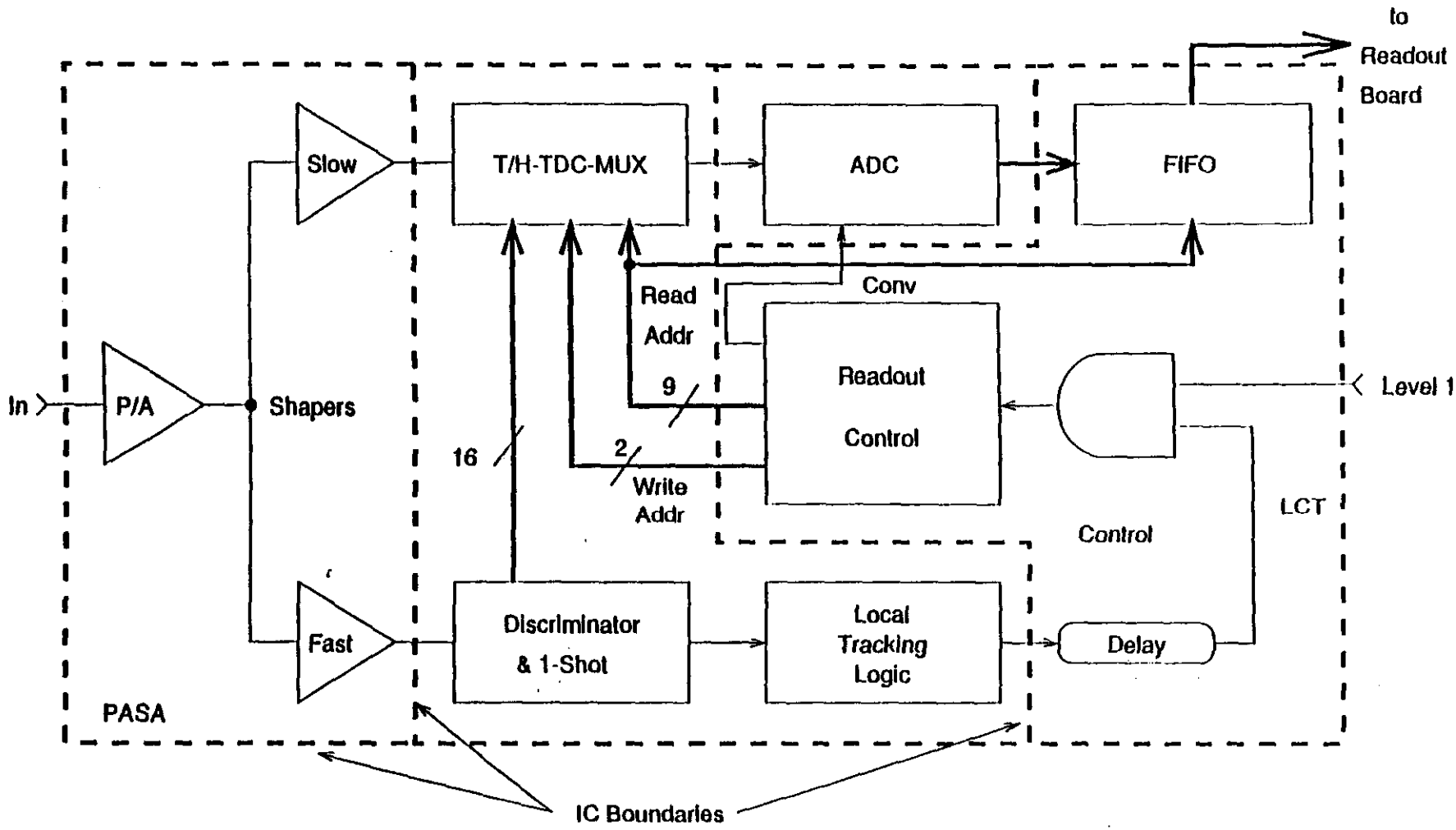
$$5 < r_n < 500 \text{ cm}^{-2}\text{s}^{-1}$$


IN DETECTOR
FE Readout PCB's
128 Channels ea.
Water Cooling
LV
Reg.
from Anodes
CSC
Module
1024
Channels
Trigger
Section
Super-
module
Mother-
board
DAQ
Section
Water Cooling
Level; 1
Trigger
Boards
ON-
DETECTOR
DAQ
Boards
ON-
DETECTOR
8
16
128
12
16
85
64

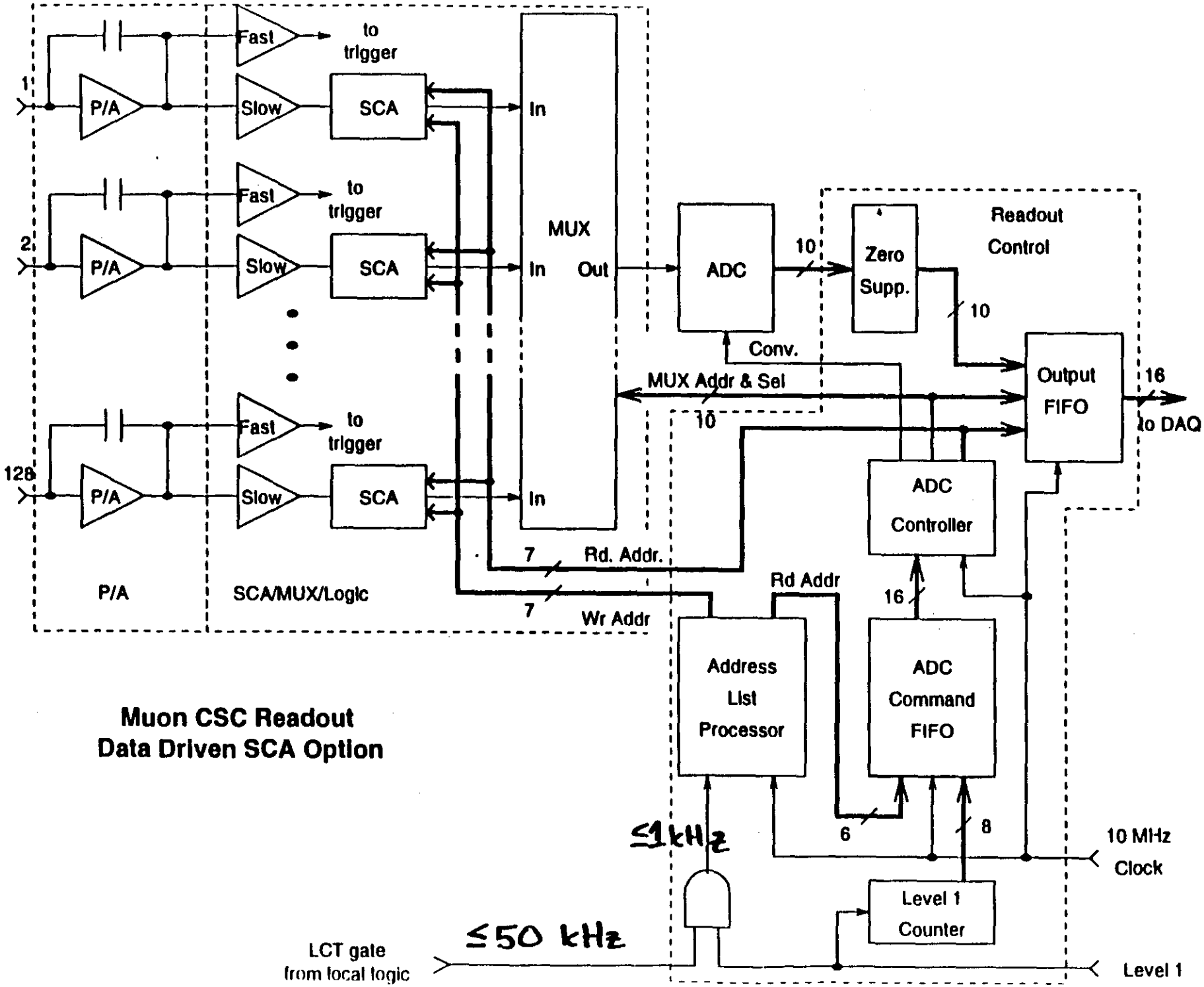


CSC Chamber Board Layout
128 Channel Version


AMPLEX Track and Hold
Quadrupule Buffer Version
Close One Switch
Close One Switch
Slow Shaper
M
U
X
ADC
2
2
Write
Read
Control Logic
Channel Address



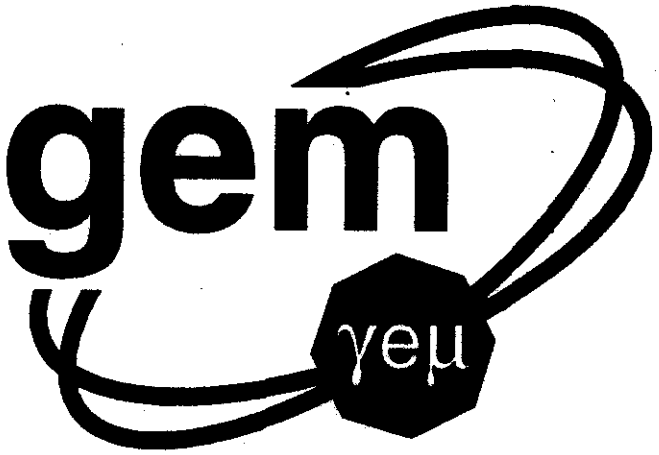
CSC Front End Board Block Diagram
Modified Amplex Version



Muon CSC Readout
Data Driven SCA Option

Muon CSC Readout R&D

BNL:	Low-noise CMOS preamp "Amplex"-like readout (0.5 FTE)	
Princeton:	S/H MUX-ADC Readout Architecture Studies (1.0 FTE)	
Boston Univ.:	Anode Readout (1.0 FTE)	
Univ. of Houston:	Readout Motherboard (0.5 FTE)	
Non-US	PNPI (St. Pete) INP (Minsk) JINR (Dubna) China (Beijing)	Anodes Preamps Readout Fab, Assy, Test



Presentation by:

R. L. Wixted

CSC Readout Electronics

R.L.Wixted

Princeton University

24 February 1993

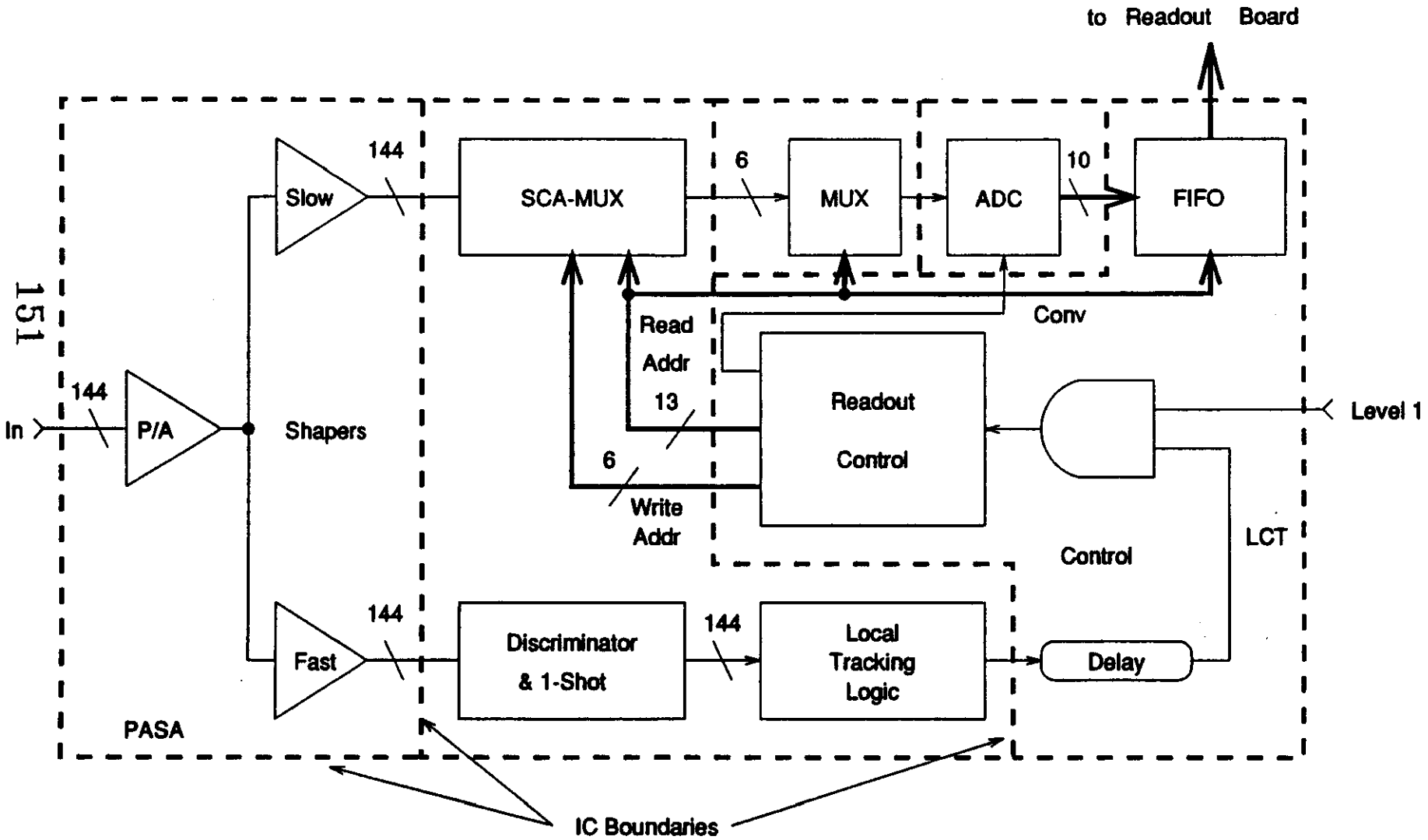
OUTLINE

Functional Block Diagram

Chip Floorplan

Local Charge Track Sub Circuits

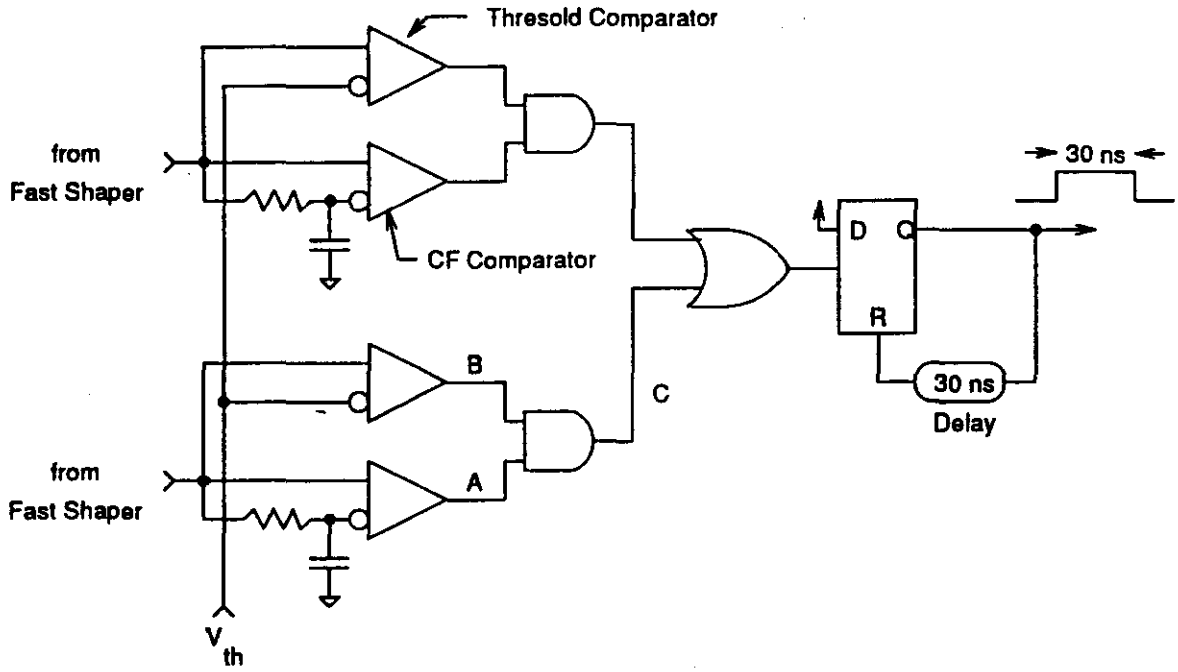
SCA-MUX Sub Circuits

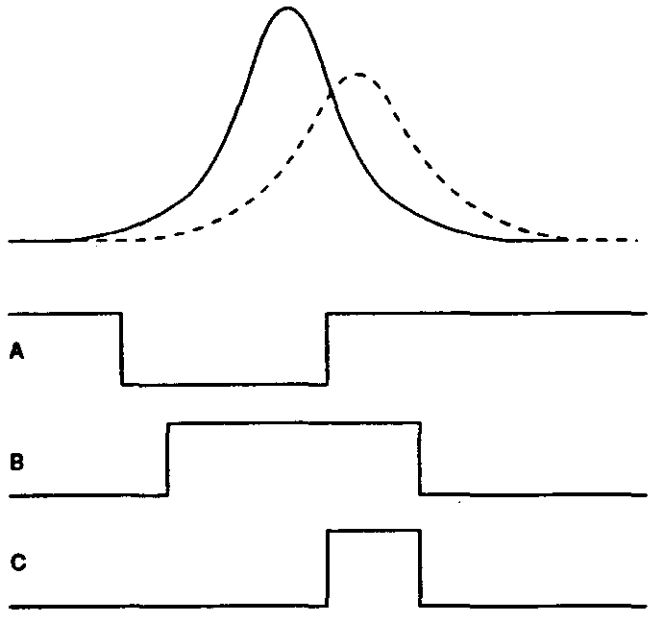


CSC Front End Board Block Diagram

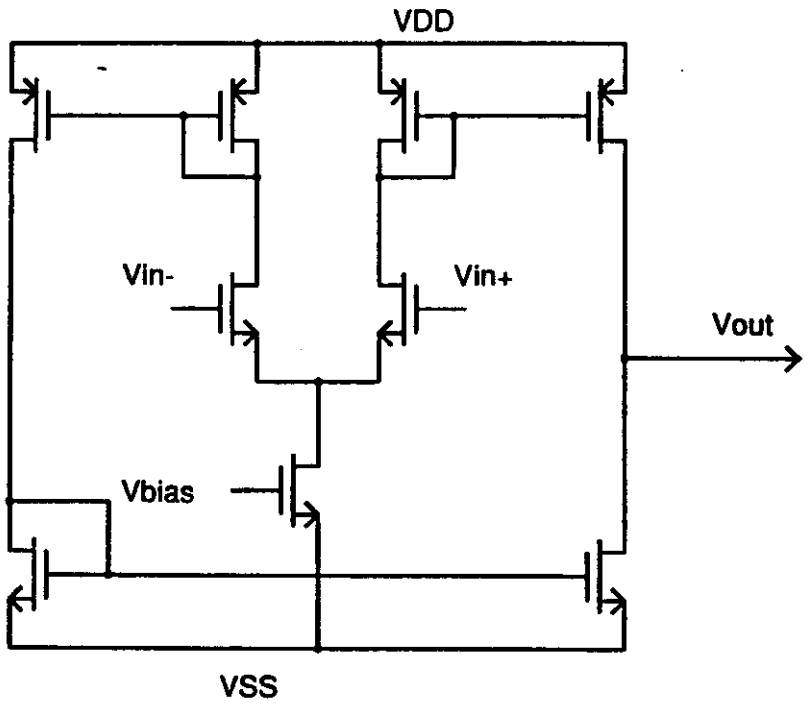
SCA Version

Timing Discriminator Schematic

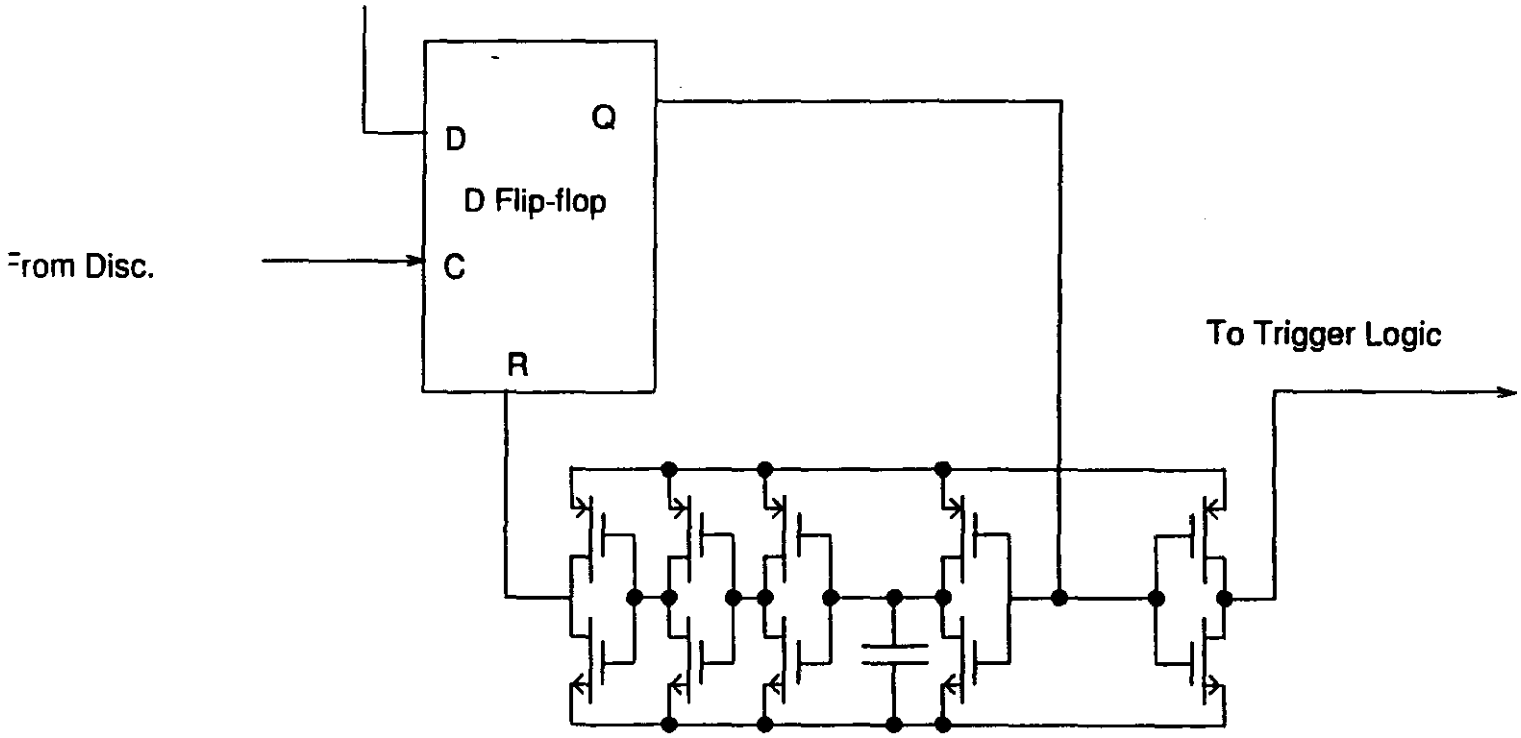




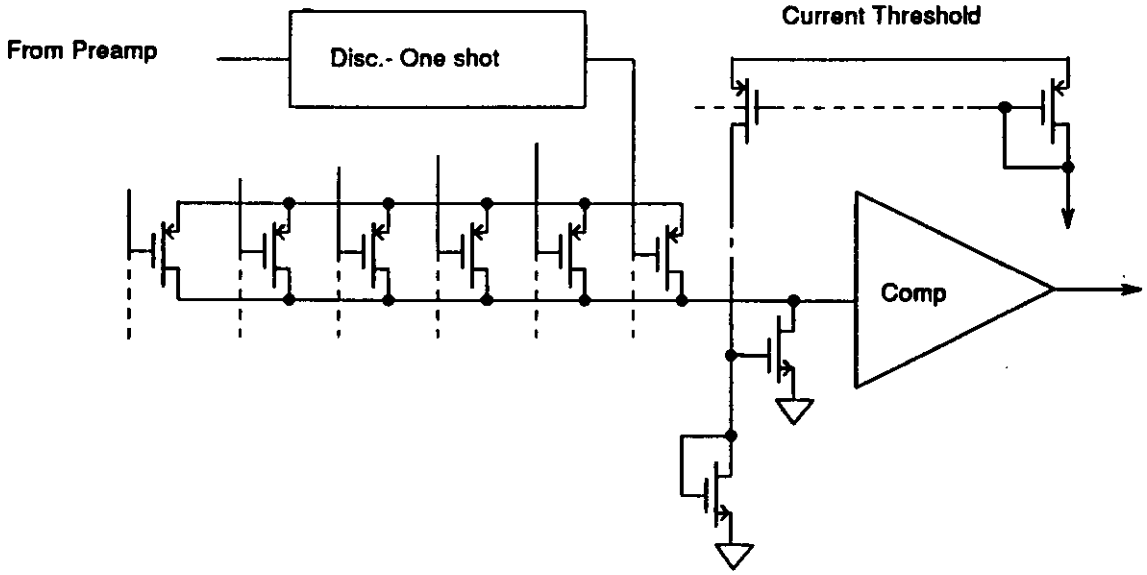
Discriminator Amplifier Schematic



Pulse Trigger Sub Circuit

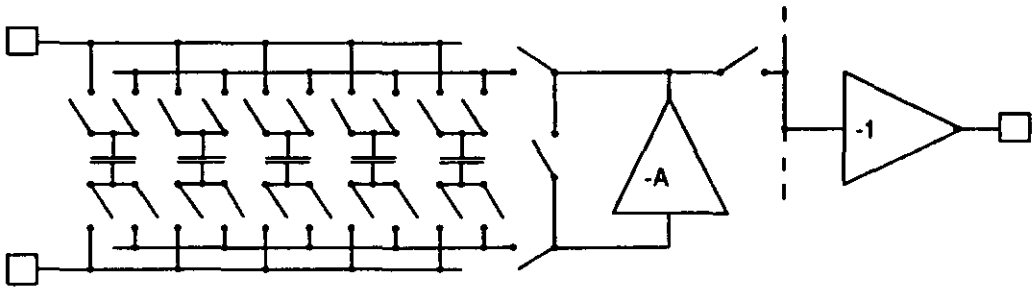


M out of 6 Trigger Schematic

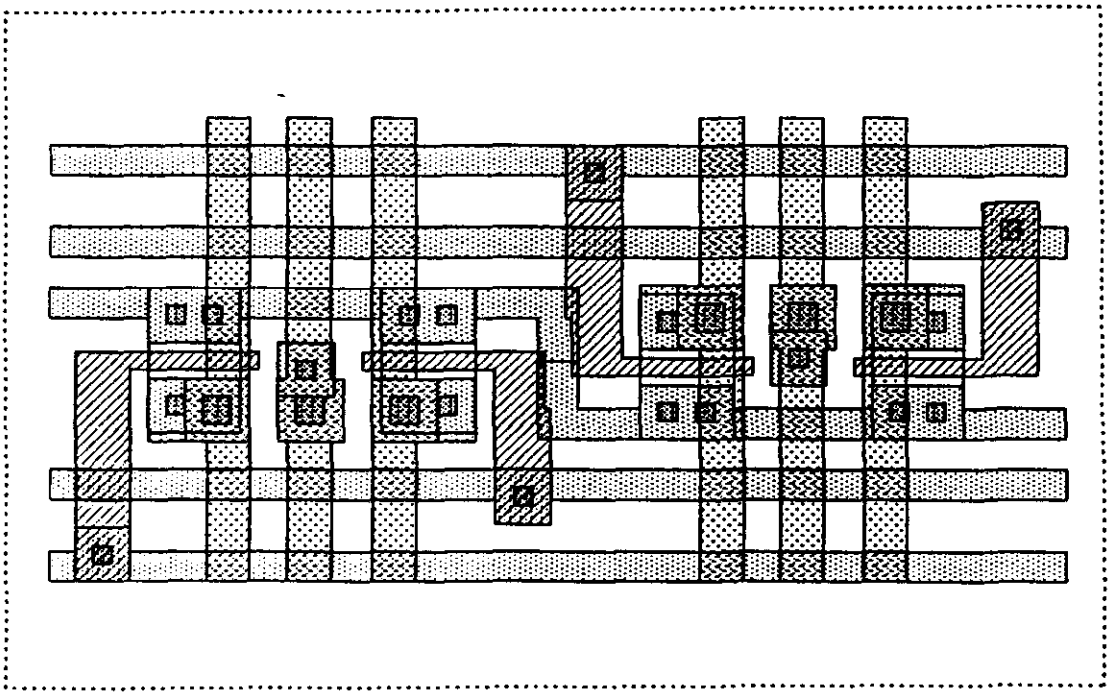


Thresh_sch.xfig

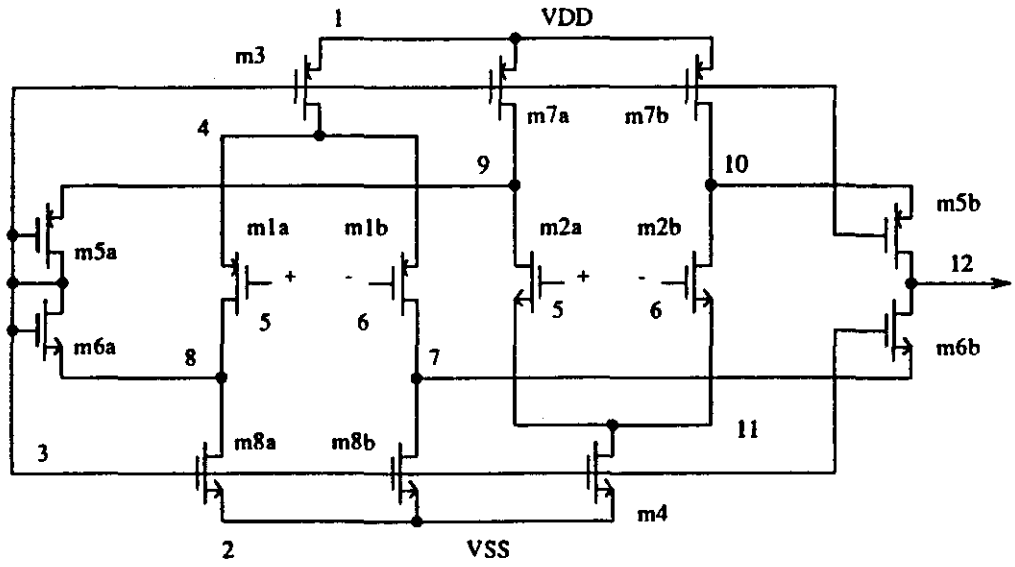
Switched Capacitor Array Schematic



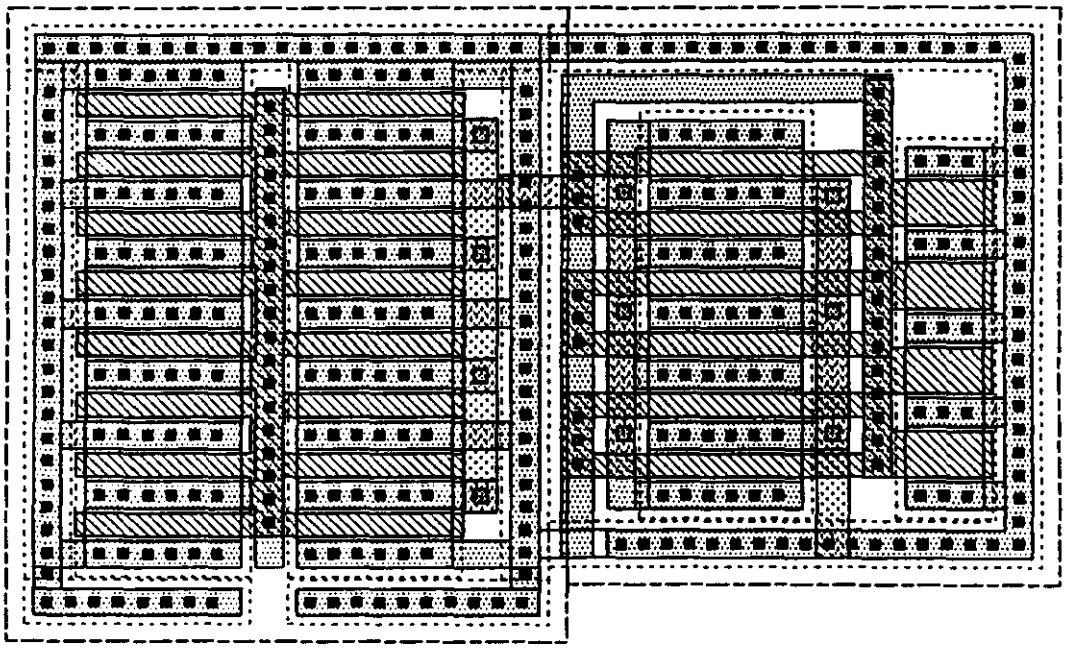
SCA CMOS Switch (SPDT)

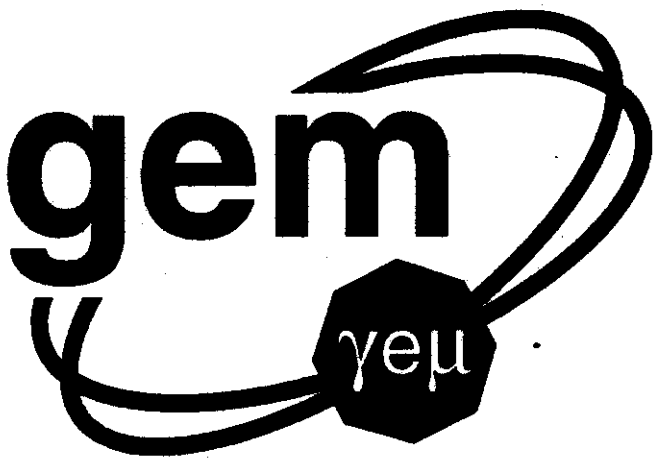


Switched Capacitor Readout Amplifier Schematic



Mirror, Cascode and Load Layout





Presentation by:

Gary S. Varner

CSC Anode Readout Electronics Update

Gary S. Varner
Boston University

Presented at the SSC Lab

24 February 93

List of Slides for 24 FEB 93 Elec. Rev. Talk

1. Introduction - Outline
2. Anode Electronics Requirements
3. Geometric Transition - Symmetry and Design Impact Discussion
4. 8/8/4 Barrel Mechanical Drawing
5. 8/8/4 Barrel Channel #'s PCB Summary
6. 8/4/4 Endcap Mechanical Drawing and Channel Count
7. 8/4/4 Endcap Channel and PCB Summary
8. 6/6/6 Barrel Mechanical Drawing (z-view)
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10. 6/6/6 Barrel Channel and PCB Count
11. 8/6/6 Endcap Mechanical and Channel Summary
12. 8/6/6 Endcap Channel and PCB Summary
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14. 6/6/6 and 8/6/6 Anode Electronics "Big Picture"
15. Mechanical Interface Drawing
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17. 3-of-4 AND/Fast, Flip-Flopped OR-of-6 (Scheme C1)
18. 3-of-4 AND/Fast, Simple OR-of-6 (Scheme C2)
19. Comparison Timing Diagram (Schemes C1 and C2)
20. Summary of RD-5 Timing Results
21. Conclusions

24 FEB 93
CSC Anode Electronics Design Review

1) Introduction to Baseline 2 for TDR

- Anode Electronics Requirements
- Comparison of New and Old CSC Configurations
- Summary of Anode Channel Counts

2) Anode Readout Architechture

- CSC Readout Overview and Chamber Interface
- Signal Processing and Readout Path
- BX Timing Discussion

3) Summary

- Administrative Schedule
- R and D Schedule
- Prototyping Schedule

Requirements for the GEM Muon System:

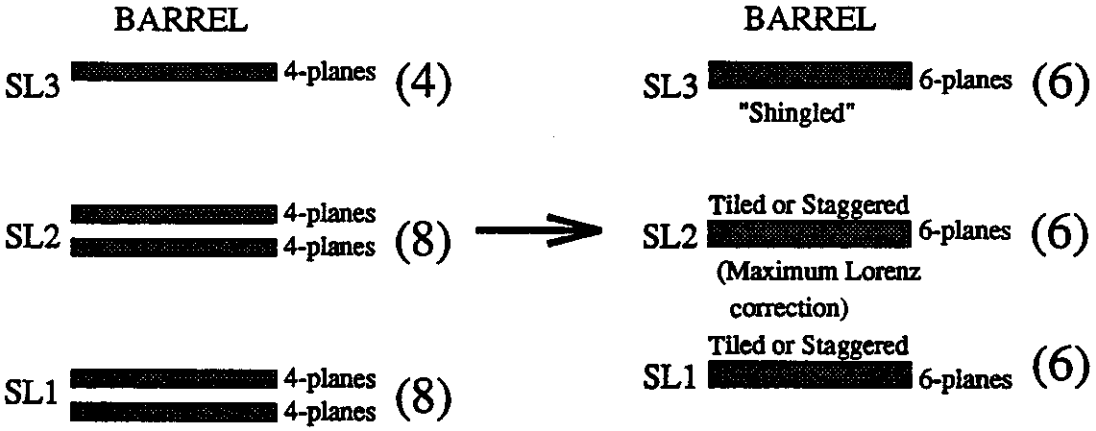
- Provide a precision coordinate measurement in the muon's bend direction with a precision of 100 μm in the barrel and 75 μm in the endcaps.
- Provide a mechanism for monitoring global alignment to a precision of 25 μm.
- Determine the non-bend coordinate (z in the barrel, r in the endcaps) with a resolution at the few cm level.
- Provide Level 1 trigger information with sufficiently fine spatial granularity to identify muons with transverse momenta up to 50 GeV/c and sufficiently good timing resolution to allow assignment of a given signal to the correct proton bunch crossing.
- Be of a design compatible with economical mass-production techniques.

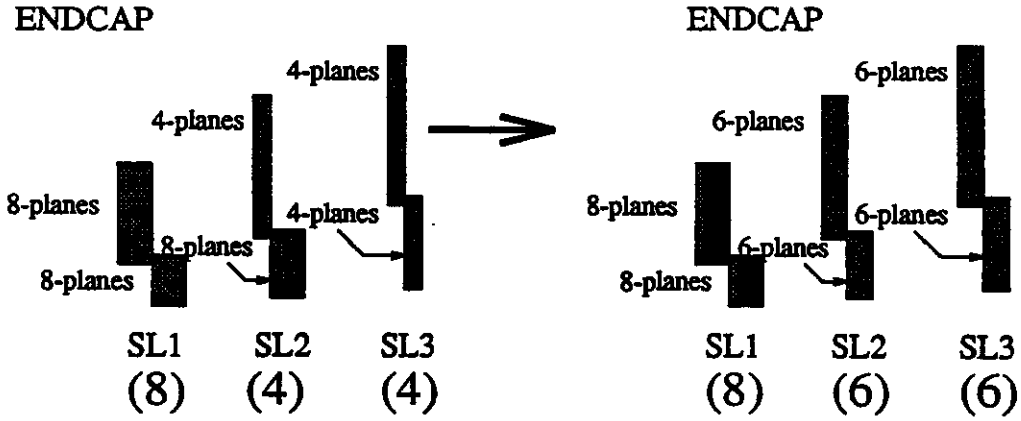
CSC Anode Readout Goals:

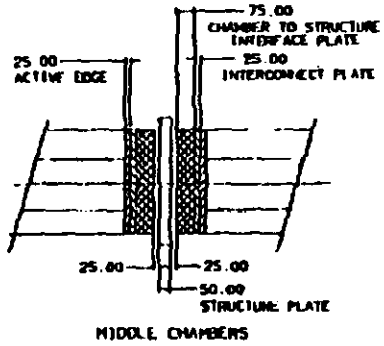
- Beam Crossing (BX) Timing
- Polar Angle Determination
- Local Anode Pattern Recognition, Background Supression
- Resolution of Multi-hit Ambiguity

Geometric Transition

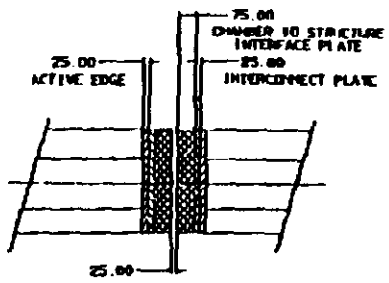
22 FEB 93 - GSV



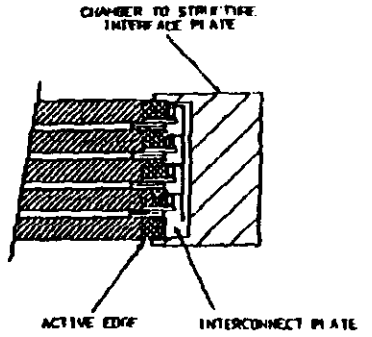


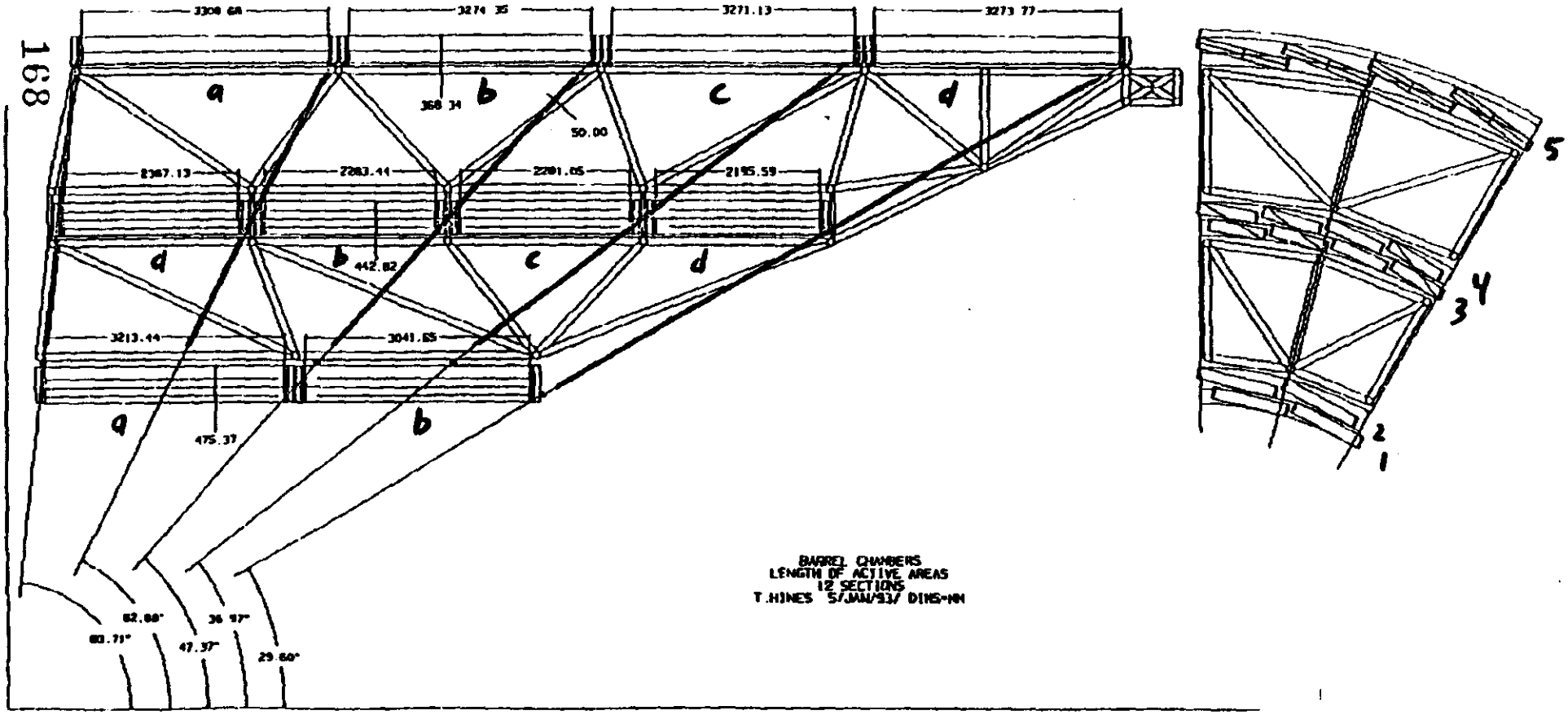


MIDDLE CHAMBERS



INNER AND OUTER CHAMBERS





BARREL CHAMBERS
LENGTH OF ACTIVE AREAS
12 SECTIONS
T.HINES 5/JAN/93/ DIMS=MM

CSC 2nd Coordinate Electronics Channel Summary

Barrel Channel/Board Count 18 FEB 93 - GSV

8/8/4 Geometry

	#mods /sec	mod. total	active edge(mm)	#z-ch /pl/s	#z-ch /sec	#PCB1 /sec.	total PCB1	#PCB2 /sec.	total #PCB2	total #z-ch	
1a)	1	48	3213.44	32	128	8	384	4	192	6144	
b)	1	48	3041.65	30	120	8	384	4	192	5760	
2a)	1	48	3213.44	32	128	8	384	4	192	6144	
b)	1	48	3041.65	30	120	8	384	4	192	5760	23808
3a)	2	96	2367.13	24	96	6	576	3	288	9216	
b)	2	96	2283.44	23	92	6	576	3	288	8832	
c)	2	96	2201.05	22	88	6	576	3	288	8448	
d)	2	96	2195.59	22	88	6	576	3	288	8448	
4a)	2	96	2367.13	24	92	6	576	3	288	9216	
b)	2	96	2283.44	23	92	6	576	3	288	8832	
c)	2	96	2201.05	22	88	6	576	3	288	8448	
d)	2	96	2195.59	22	88	6	576	3	288	8448	69888
5a)	2	96	3308.68	33	132	8	768	4	384	12672	
b)	2	96	3274.35	33	132	8	768	4	384	12672	
c)	2	96	3271.13	33	132	8	768	4	384	12672	
d)	2	96	3273.77	33	132	8	768	4	384	12672	50688
										======	
									TOTAL Channel Count:	144384	

NOTE: In Barrel all Supermodules 4 layers only, wires ganged in groups of 40 (10 cm).

TOTAL PCB Count:

PCB1	PCB2	Supermodule Layer
1536	768	Inner
4608	2304	Middle
3072	1536	Outer
9216	4608	

Definitions:

PCB1 - 2 layer signal carrying board with blocking caps. Spans 4 gangs on each of 4 anode planes. Right edge connector mates to PCB2 Dims.: ~12cm width (of tongue) x 20cm depth (width of 4 CSC layers).

PCB2 - 8 layer signal processing board. Handles 32 channels nominally. Dims.: see diagram (baseline 40 cm x ~10 cm)

CSC 2nd Coordinate Electronics Channel Summary
==========
Endcap Channel/Board Count 18 FEB 93 - GSV

8/4/4 Geometry

	# pl.	#r-ch /pl/s	# of secs.	#PCB1 /sec.	total PCB1	#PCB2 /sec.	total PCB2	#PCB3 /sec.	total PCB3	#r-ch /sec.	#r-ch	
1a)	8	17	24			5	120	5	120	136	3264	
1b)	8	19	24			5	120	5	120	152	3648	
2a)	8	29	24			8	192	8	192	232	5568	
2b)	8	32	24			8	192	8	192	256	6144	18624
3a)	8	30	24			8	192	8	192	240	5760	
3b)	8	31	24			8	192	8	192	248	5952	
4a)	4	23	48	6	288	3	144			92	4416	
4b)	4	24	48	6	288	3	144			96	4608	20736
5a)	4	21	48	6	288	3	144			84	4032	
5b)	4	22	48	6	288	3	144			88	4224	
6a)	4	34	48	9	432	5	240			136	6528	
6b)	4	35	48	9	432	5	240			140	6720	21504
									TOTAL Channel Count:		60864	

NOTE: Modules in layers 1-3 have wires ganged in groups of 20 (5 cm) and modules in layers 4-6 have wires ganged in groups of 40 (10 cm).

TOTAL PCB Count:

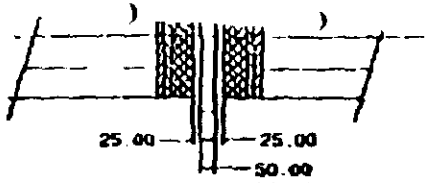
PCB1	PCB2	PCB3	Supermodule Layer
0	624	624	Inner
1200	1008	384	Middle
2736	1440	0	Outer
3936	3072	1008	

Definitions:

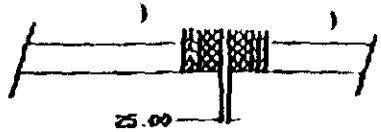
PCB1 - 2 layer signal carrying board with blocking caps. Spans 4 gangs on each of 4 anode planes. Right edge connector mates to PCB2
Dims.: ~12cm width (of tongue) x 20cm depth (width of 4 CSC layers).

PCB2 - 8 layer signal processing board. Handles 32 channels nominally.
Dims.: see diagram (baseline 40 cm x ~10 cm)

PCB3 - 4 layer signal carrying board with blocking caps. Same functionally as PCB1, except spans 8 anode planes and mates to two PCB2s.
Dims.: ~12 cm width x 50 cm depth.

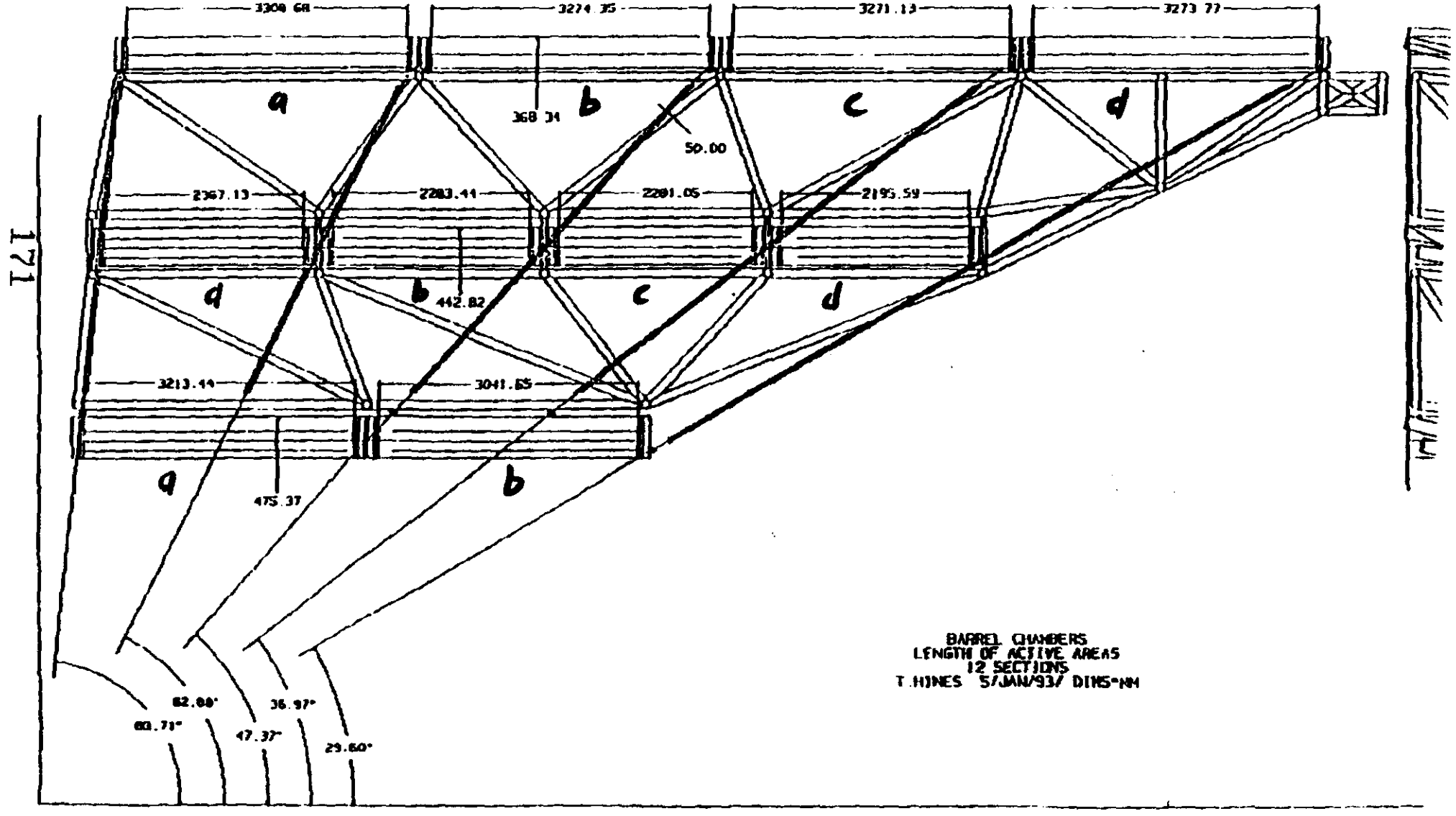


MIDDLE CHAMBERS



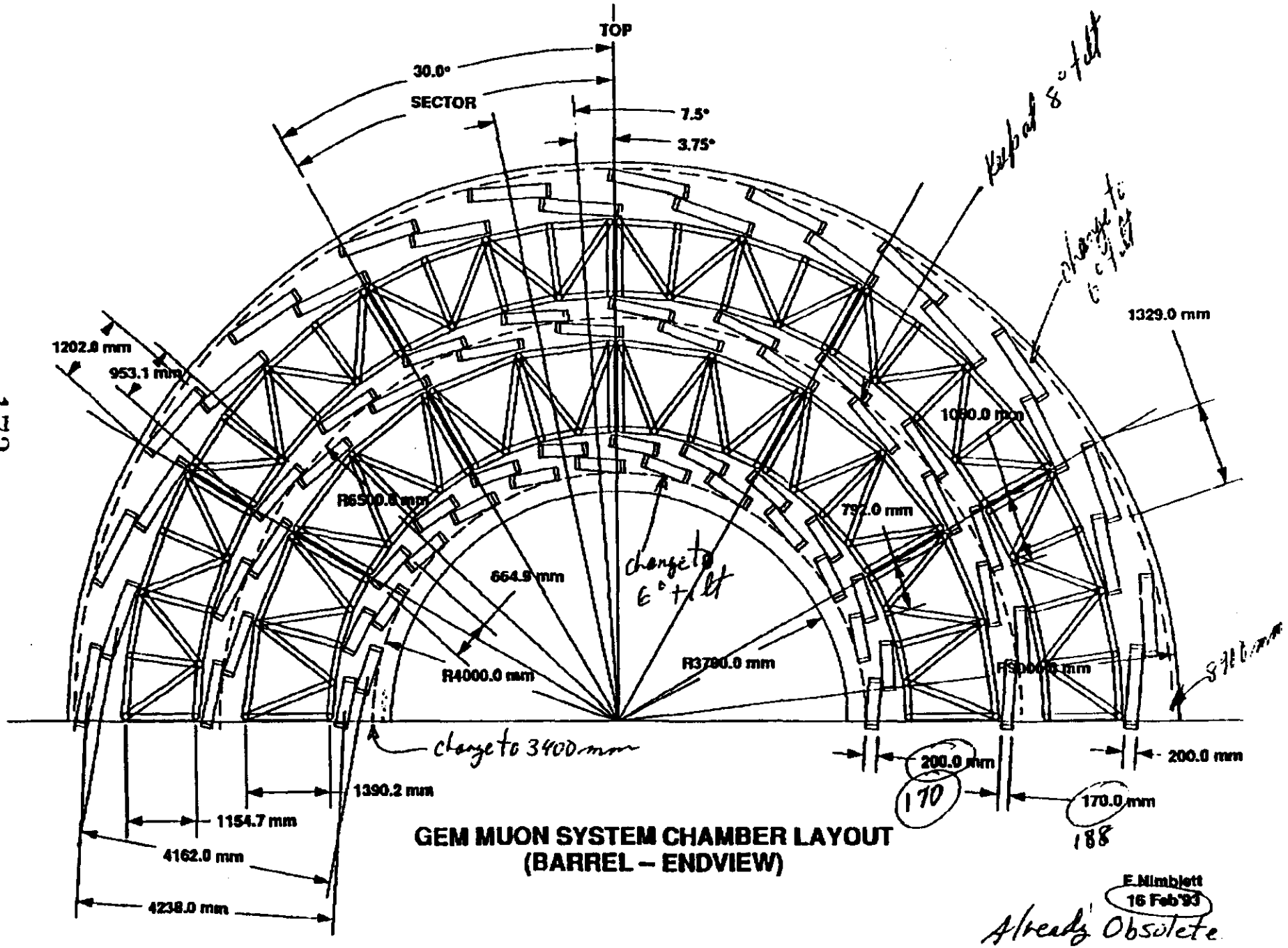
INNER AND OUTER CHAMBERS

ACTI



BARREL CHAMBERS
LENGTH OF ACTIVE AREAS
12 SECTIONS
T.HINES 5/JAN/93/ DIMS=MM

172

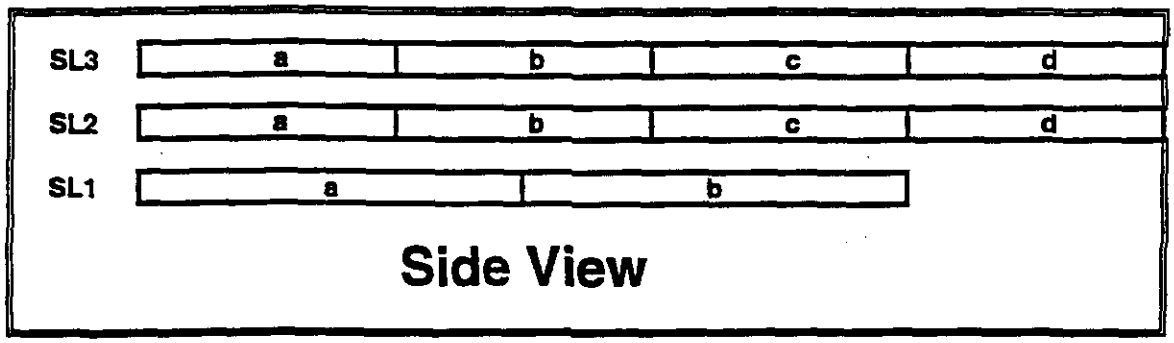


GEM MUON SYSTEM CHAMBER LAYOUT
(BARREL – ENDVIEW)

E.Nimblett
16 Feb'93

Already Obsolete

CSC 2nd Coordinate Electronics Channel Summary
Barrel Channel/Board Count 16 Feb 93 - GSV



SL/30deg phi	# modules /sector	#modules total	active edge(mm)	#z-Ch./ pl/sec	#z-Chan/ sector	#PCB1/ sector	total PCB1	#PCB2/ sector	total PCB2	total #z-Ch.
1a	4	96	3213.44	32	768	44	1,056	22	528	18432
1b	4	96	3041.65	30	720	40	960	20	480	17280
2a	4	96	2367.13	24	576	32	768	16	384	13824
2b	4	96	2283.44	23	552	32	768	16	384	13248
2c	4	96	2201.05	22	528	32	768	16	384	12672
2d	4	96	2195.59	22	528	32	768	16	384	12672
3a	4	96	3308.68	33	792	44	1,056	22	528	19008
3b	4	96	3274.35	33	792	44	1,056	22	528	19008
3c	4	96	3271.13	33	792	44	1,056	22	528	19008
3d	4	96	3273.77	33	792	44	1,056	22	528	19008
Total Modules		960					TOTAL Barrel Channels			164160

NOTE: In Barrel all Supermodules 6 layers only, wires ganged in groups of 40 (10cm).

Total PCB Count:

	PCB1	PCB2	SL#	
	2016	1008	1	(Inner)
	3072	1536	2	(Middle)
	4224	2112	3	(Outer)
TOTAL:	9312	4656		

Definitions:

PCB1: *PCB1 is a two layer signal carrying board with blocking caps. It spans 3 gangs of wires on each of 6 anode planes. A right-angle edge connector mates to PCB2.*
Dims.: ~8cm wide (width of tongue) x 20cm deep (depth of 6 planes).

PCB2: PCB2 is an 8-layer signal processing board. It handles 36 channels nominally (this corresponds to 2 PCB1 inputs) and spans 60cm of active chamber area.
Dims.: ~40cm wide (to allow 2 PCB1 matings) x 15cm deep (active area of signal processing).

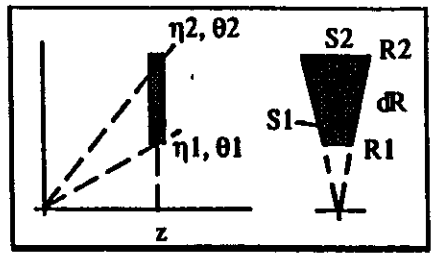
Endcap CSC Layout -- Baseline II Version h.4 -- Towers -- 8/6/6 24/48/48

SW 17-Feb-93

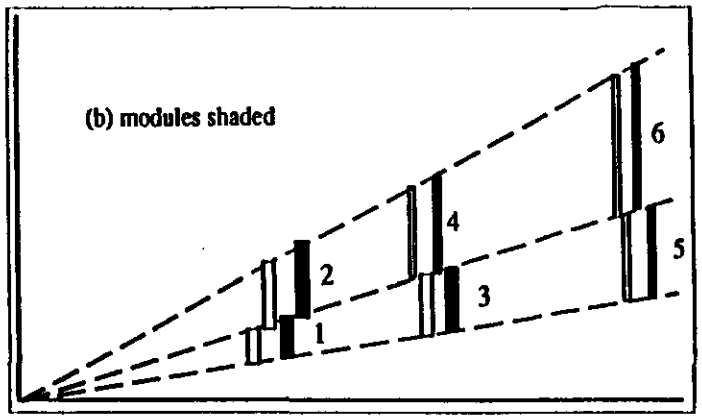
active coverage 9.75° to 27.71°

core thickness =	20.00	mm
in-tower intermodule space =	0.05	m
intertower space =	0.15	m
anode ch modularity =	3	
anode ch overlap =	1	
strip ch modularity =	16	
strip ch overlap =	3	
neutron flux (Hz/cm^2) =	10,000	
neutron efficiency =	0.005	

Nomenclature:



Layout:



Note: modules (a) occupy even-numbered sectors
modules (b) occupy odd-numbered sectors
Nsctrs/2 are type (a) and Nsctrs/2 are type (b)

	ngaps	gap= str wid mm	modth m	zfr m	zba m	zav m	Dz's	η1	θ1 deg	η2	θ2 deg	Nsctrs	R1 m	R2 m	dR m	S1 m	S2 m	# strips /pl/sctr	wire gp cm	Total ch counts: # r-ch /pl/sctr	# str ch	# r ch	single strip occ. ch. pl. /sec	neut. /sec
Inner modules																								
1a)	8	5.00	0.22	6.00	6.22	6.11		2.46	9.75	1.90	17.01	24	1.05	1.87	0.82	0.28	0.51	80	5.0	18	15,360	3,456	186	2,050
1b)	8	5.00	0.22	6.64	6.86	6.75		2.46	9.75	1.90	17.01	24	1.16	2.07	0.91	0.31	0.56	96	5.0	18	18,432	3,456	206	2,265
2a)	8	5.00	0.22	6.27	6.49	6.38		1.92	16.61	1.40	27.71	24	1.90	3.35	1.45	0.51	0.89	144	5.0	30	27,648	5,760	41	3,620
2b)	8	5.00	0.22	6.91	7.13	7.02		1.92	16.64	1.40	27.71	24	2.10	3.69	1.59	0.56	0.98	160	5.0	33	30,720	6,336	45	3,971
Middle modules																								
3a)	6	7.00	0.18	10.88	11.06	10.97	4.86	2.46	9.75	1.90	17.01	48	1.88	3.36	1.47	0.26	0.47	64	5.0	30	18,432	8,640	105	5,153
3b)	6	7.00	0.18	11.44	11.63	11.54	4.79	2.46	9.75	1.90	17.01	48	1.98	3.53	1.55	0.27	0.49	64	5.0	30	18,432	8,640	111	5,418
4a)	6	7.00	0.18	10.65	10.83	10.74	4.36	1.93	16.53	1.40	27.71	48	3.19	5.64	2.45	0.43	0.76	96	10.0	24	27,648	6,912	22	8,587
4b)	6	7.00	0.18	11.21	11.39	11.30	4.28	1.93	16.55	1.40	27.71	48	3.36	5.94	2.58	0.45	0.80	96	10.0	27	27,648	7,776	23	9,020
Outer modules																								
5a)	6	10.00	0.20	15.70	15.90	15.80	4.83	2.46	9.75	1.90	17.01	48	2.71	4.83	2.12	0.38	0.67	64	10.0	21	18,432	6,048	72	10,602
5b)	6	10.00	0.20	16.30	16.50	16.40	4.87	2.46	9.75	1.90	17.01	48	2.82	5.02	2.20	0.39	0.69	64	10.0	24	18,432	6,912	75	11,005
6a)	6	10.00	0.20	15.45	15.65	15.55	4.81	1.92	16.67	1.40	27.71	48	4.66	8.17	3.51	0.63	1.11	96	10.0	36	27,648	10,368	15	17,542
6b)	6	10.00	0.20	16.05	16.25	16.15	4.85	1.92	16.69	1.40	27.71	48	4.84	8.48	3.64	0.66	1.15	96	10.0	36	27,648	10,368	15	18,200

total area of strip cathodes (m^2)	4255
total volume of chambers (m^3)	21.3
Total number of modules	480

Total =: 276,480 84,672

CSC 2nd Coordinate Electronics Channel Summary
Endcap Channel/Board Count 19 Feb 93 - GSV

SL/phi	# of planes	# of sectors	active edge(mm)	#PCB1 /sector	total PCB1	#PCB2 /sector	total PCB2	#r-Ch. /sector	total #r-Ch.
1a	8	24	820	5	120	3	72	16	3072
1b	8	24	910	6	144	3	72	18	3456
2a	8	24	1,450	10	240	5	120	29	5568
2b	8	24	1,590	11	264	6	144	32	6144
3a	6	48	1,470	10	480	5	240	15	4320
3b	6	48	1,550	10	480	5	240	16	4608
4a	6	48	2,450	16	768	8	384	25	7200
4b	6	48	2,580	17	816	9	432	26	7488
5a	6	48	2,120	14	672	7	336	21	6048
5b	6	48	2,200	15	720	8	384	22	6336
6a	6	48	3,510	23	1,104	12	576	35	10080
6b	6	48	3,640	24	1,152	12	576	36	10368
						TOTAL Endcap Channels			74688

NOTE: In the Endcap SL1 contains 8-layer Supermodules with wires ganged in groups of 20 (5cm). In this case the PCB2's are overlapping. SL2 and SL3 (middle and outer SL's) are 6-layer Supermodules and have wire gangings of 40 (10cm).

Total PCB Count:

	PCB1	PCB2	SL#	
	768	408	1	(Inner)
	2544	1296	2	(Middle)
	3648	1872	3	(Outer)
TOTAL:	6960	3576		

Definitions:

PCB1: PCB1 is a two layer signal carrying board with blocking caps. It spans 3 gangs of wires on each of 6 anode planes. A right-angle edge connector mates to PCB2.
Dims.: ~8cm wide (width of tongue) x 20cm deep (depth of 6 planes).

PCB2: PCB2 is an 8-layer signal processing board. It handles 36 channels nominally (this corresponds to 2 PCB1 inputs) and spans 60cm of active chamber area.
Dims.: ~40cm wide (to permit 2 PCB1 matings) x 15cm deep (active area of signal processing).

Comparative

22 FEB 93 - GSV

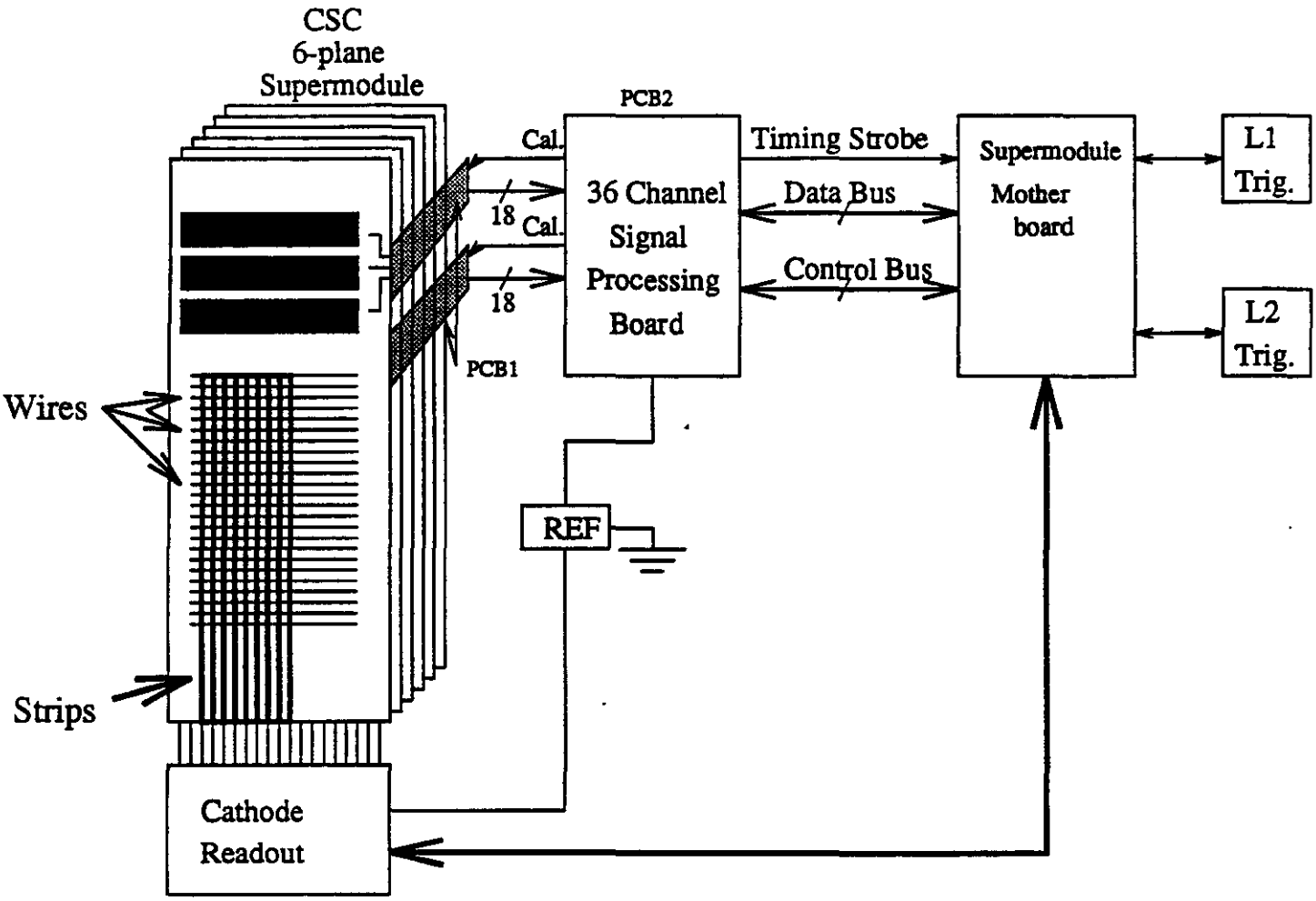
Channel and PCB Count Summary

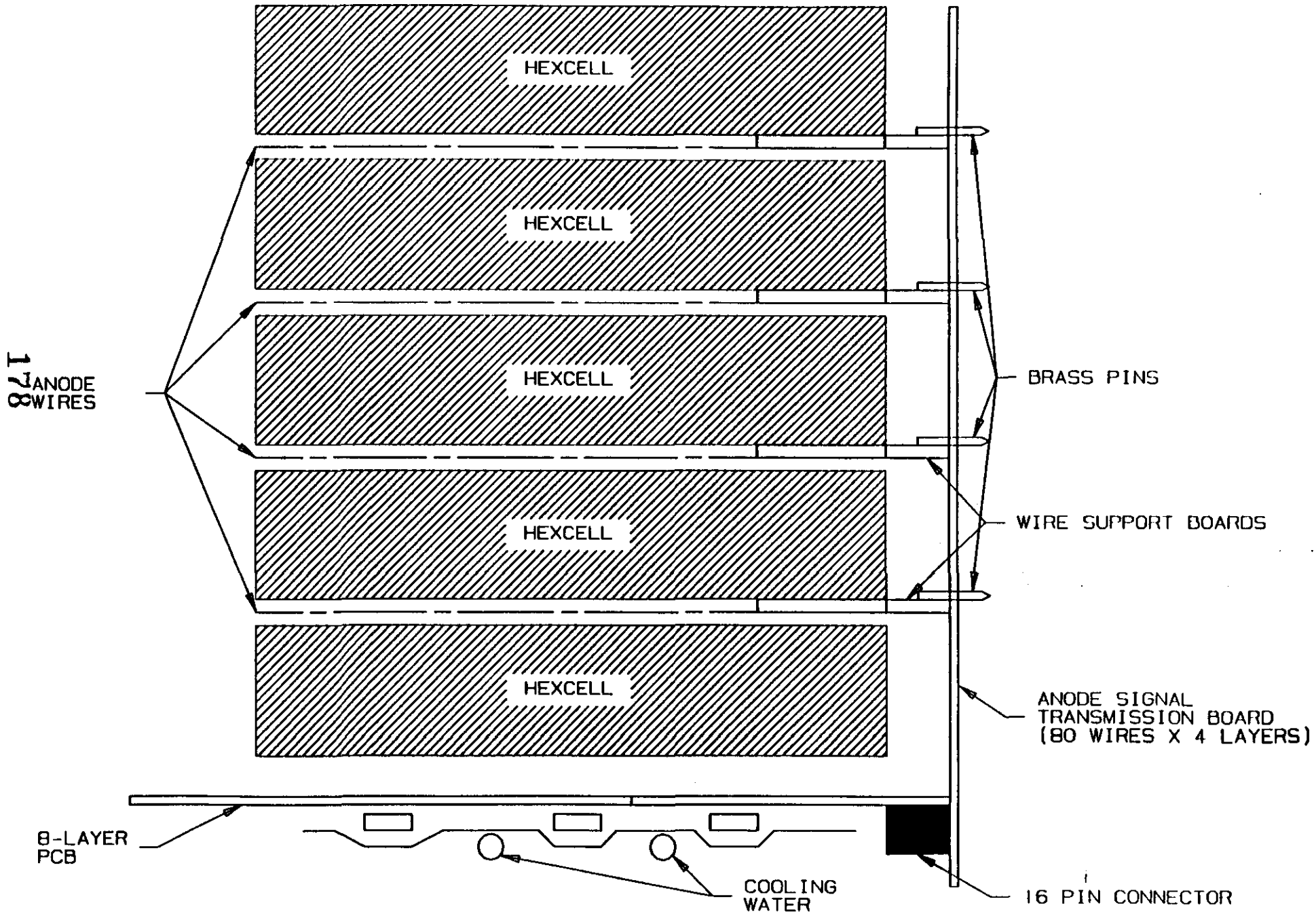
	Barrel 8/8/4	Endcap 8/4/4	TOTAL	Barrel 6/6/6	Endcap 8/6/6	TOTAL
Channels	144k	61k	205k	164k	75k	239k
PCB1	9216	4944	14160	9312	6960	16272
PCB2	4608	3072	7680	4656	3576	8232
Supermodules	1344	432	1776	960	480	1440

CSC 2nd Coord. Readout

20 FEB 93 - GSV

6/6/6 and 8/6/6 Geometries

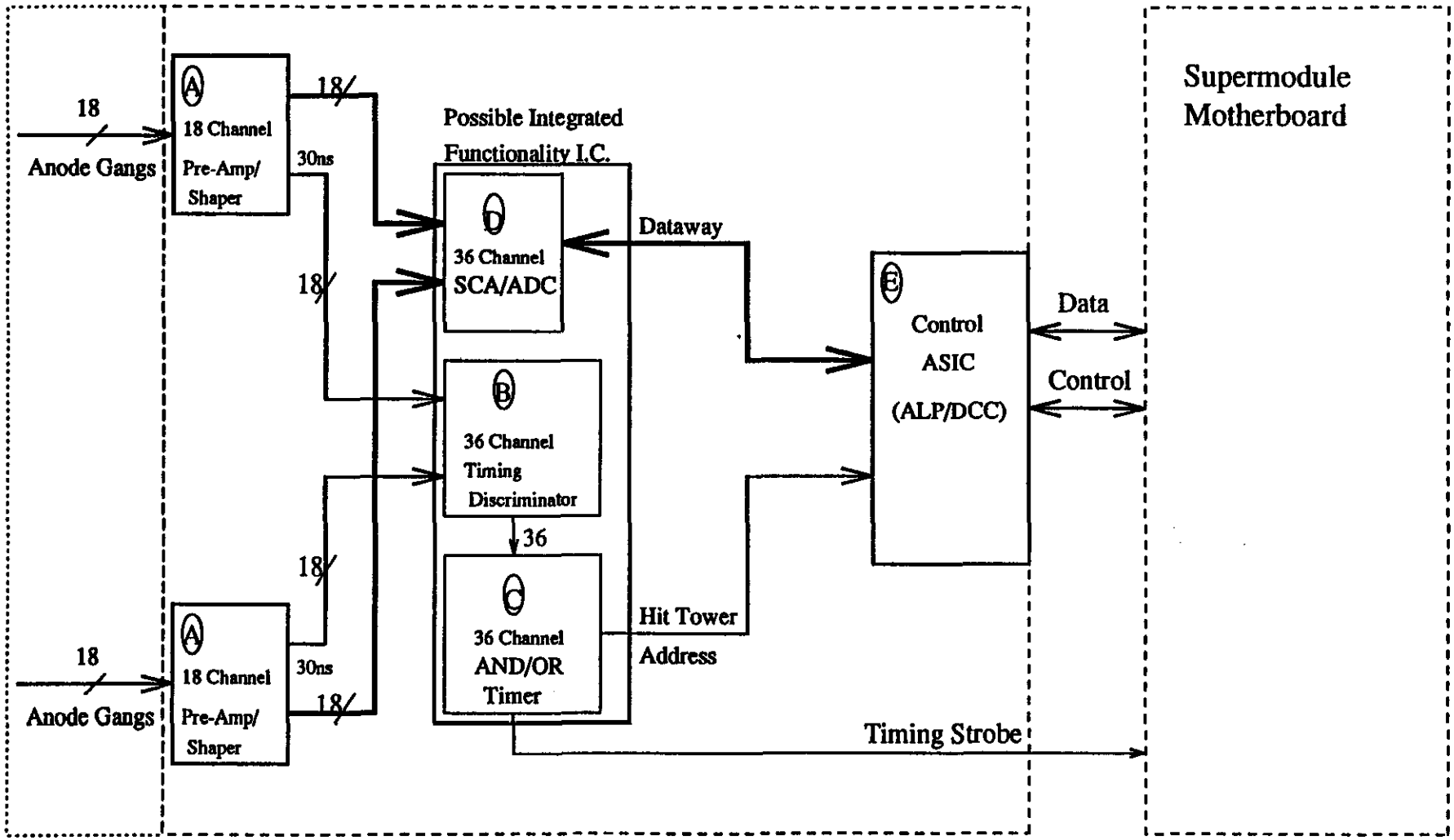



HEXCELL
HEXCELL
HEXCELL
HEXCELL
HEXCELL
178 ANODE WIRES
BRASS PINS
WIRE SUPPORT BOARDS
ANODE SIGNAL TRANSMISSION BOARD (80 WIRES X 4 LAYERS)
8-LAYER PCB
COOLING WATER
16 PIN CONNECTOR

Signal Processing Specifics

20 FEB 93 - GSV

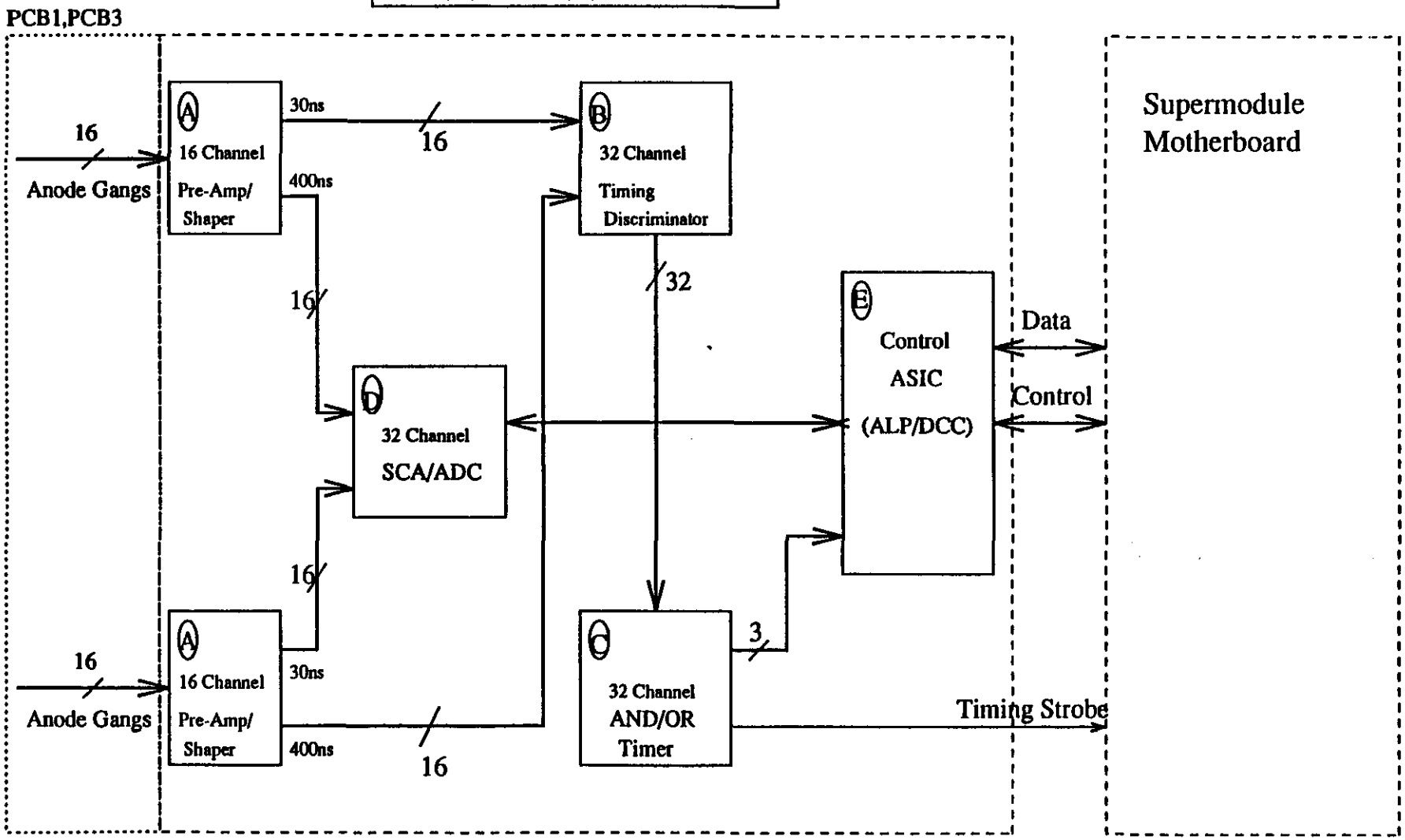
For 6/6/6 and 8/6/6 Geometries



Signal Processing Specifics

12 FEB 93 - GSV

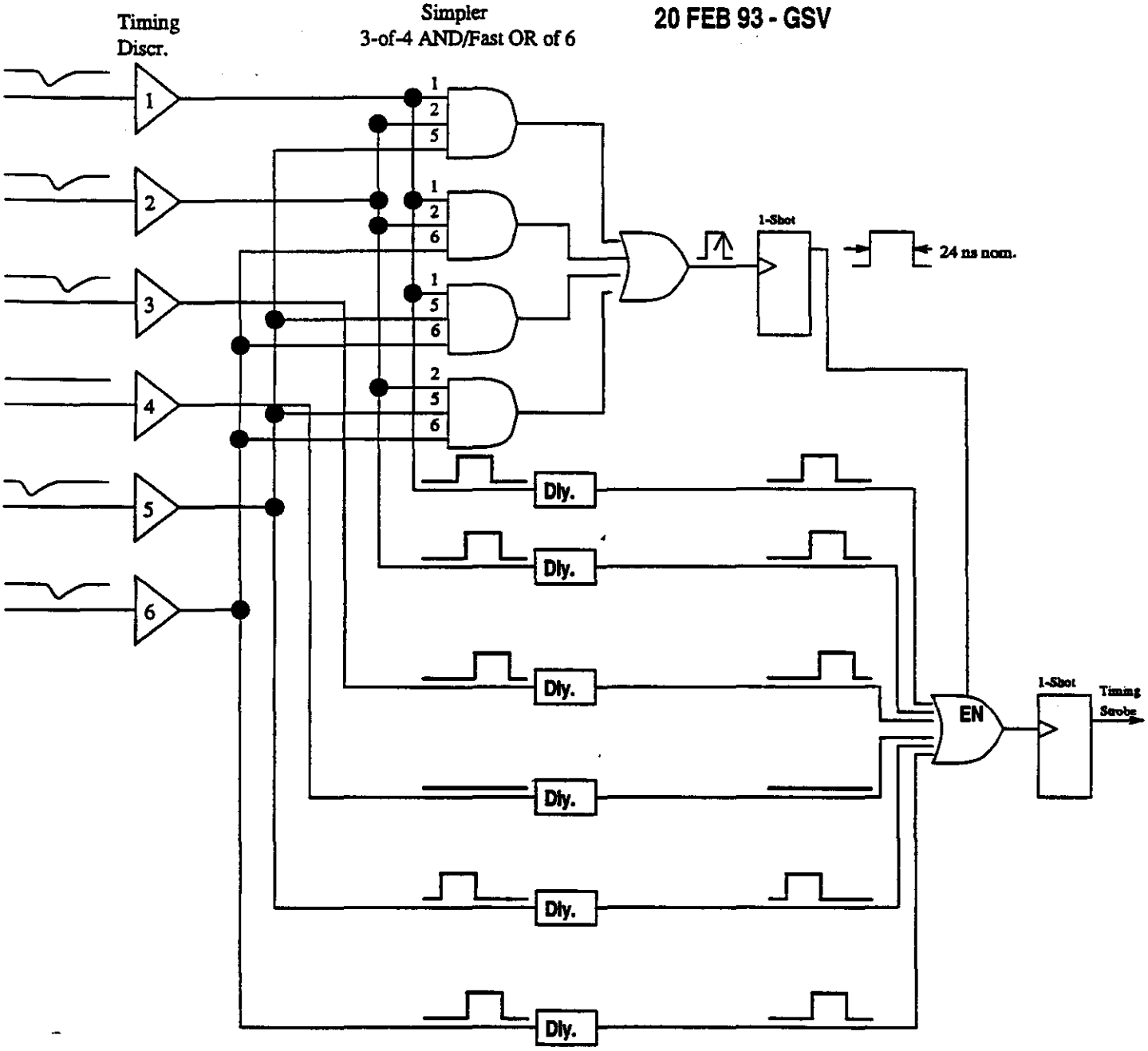
For 8/8/4 and 8/4/4 Geometries



Single Projective Tower

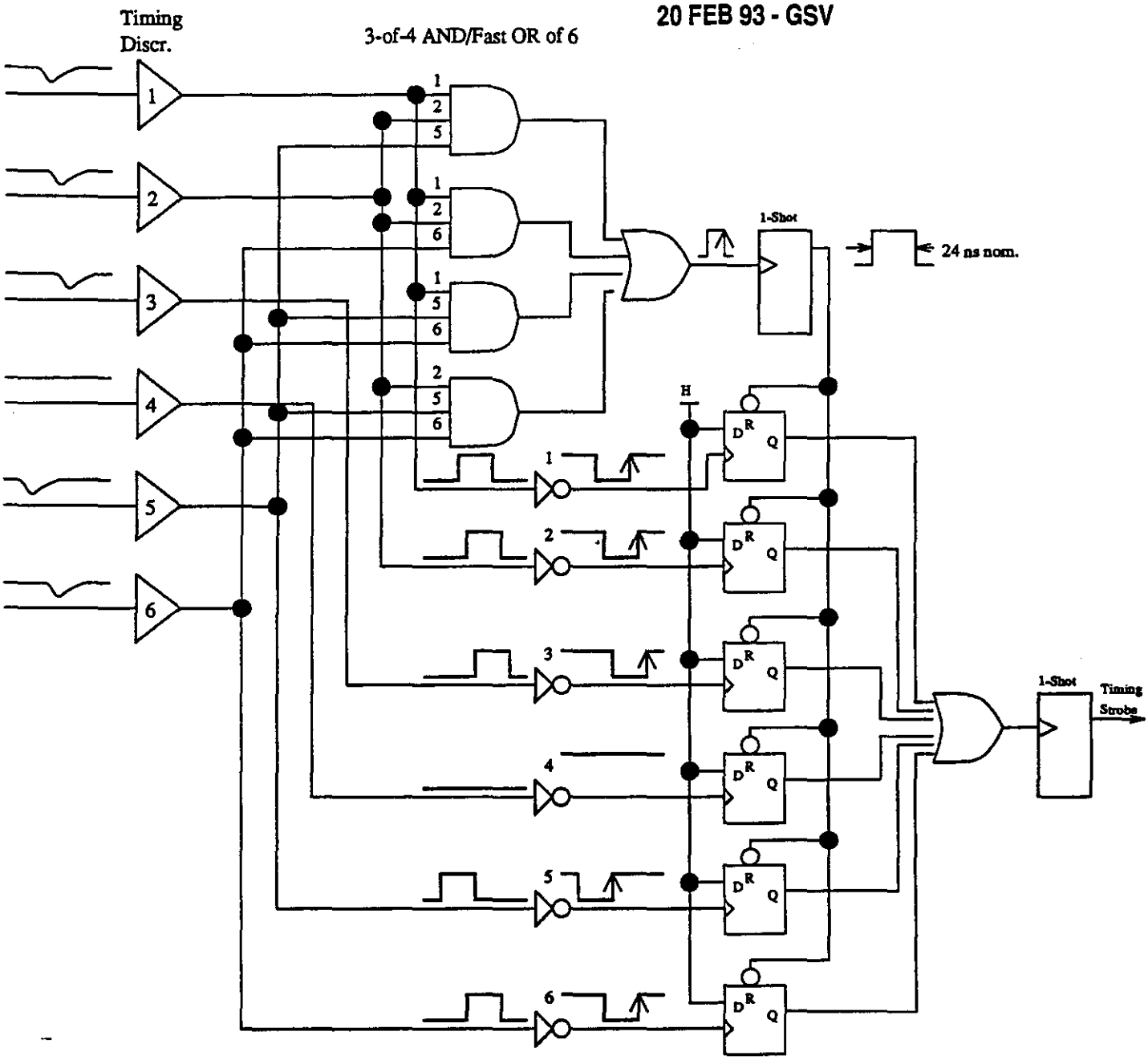
Simpler
3-of-4 AND/Fast OR of 6

20 FEB 93 - GSV



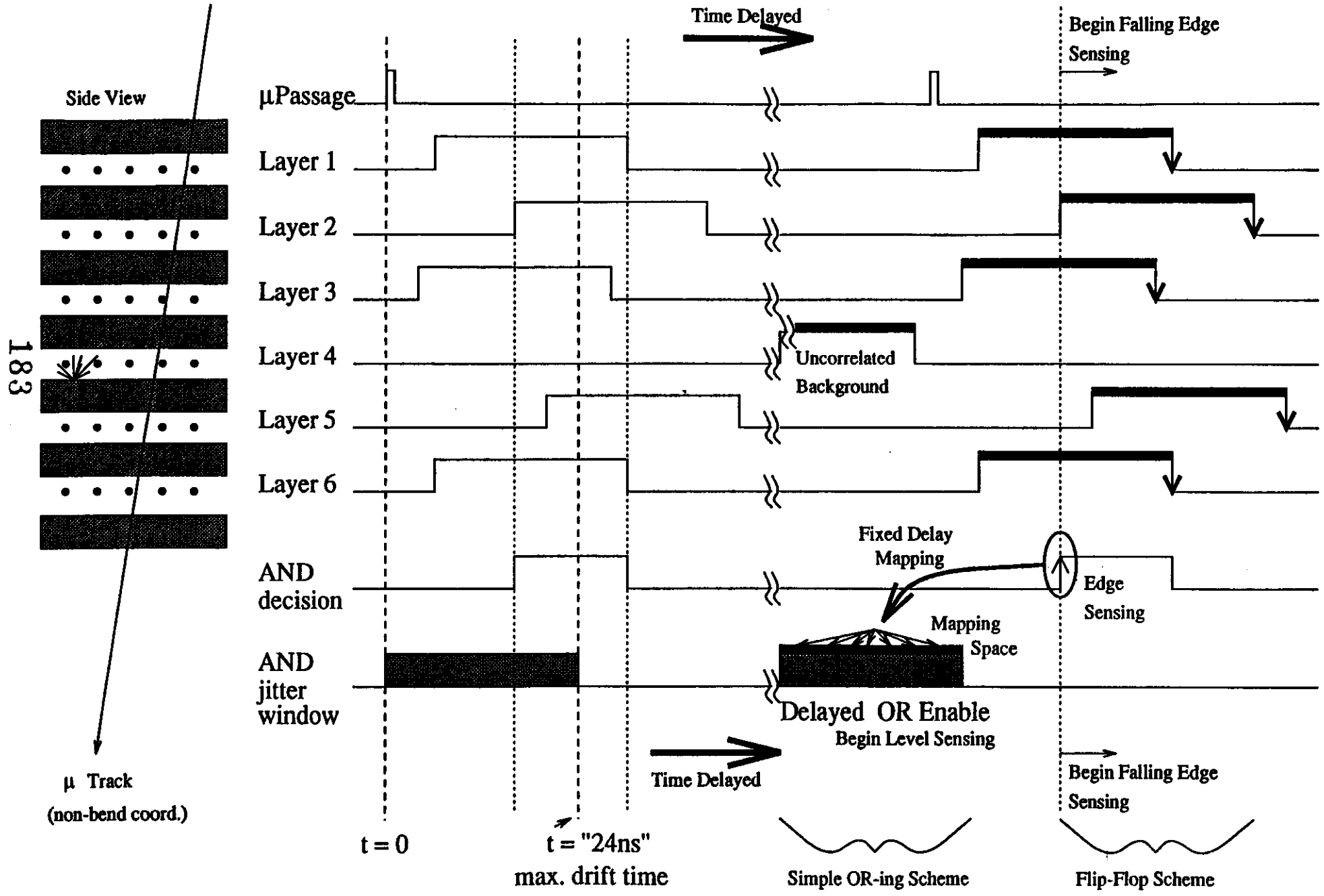
Single Projective Tower

20 FEB 93 - GSV



3-of-4 AND/Fast OR of 6 Timing Diagram

20 FEB 93 - GSV



RD-5 Timing Results

22 FEB 93 - GSV

- Leading edge disc. with fixed threshold - 150mV
  - 11ns rms per plane
  - 6.5ns rms for OR of 4 planes
  - Not the best possible:
    - → Improvement with higher HV
    - → Lab tests show 30%improvement with Constant Fraction Discrimination
- In terms of 16ns BX tagging, looks promising:
  - Building Prototype Electronics
  - Realistic Background Testing

CONCLUSIONS

Design Specifications

- Rapidly bringing this comparatively immature technology up to speed
- Outstanding Anode Electronics Design Issues:
  - Wire ganging
  - Noise tolerance
  - ADC resolution

R & D Issues

- **A LOT to be studied, A sampling:**
- Cost Efficient Multi-hit Resolution
- Optimal Timing Scheme
- Signal Fan-in Density issues

Preliminary Cost

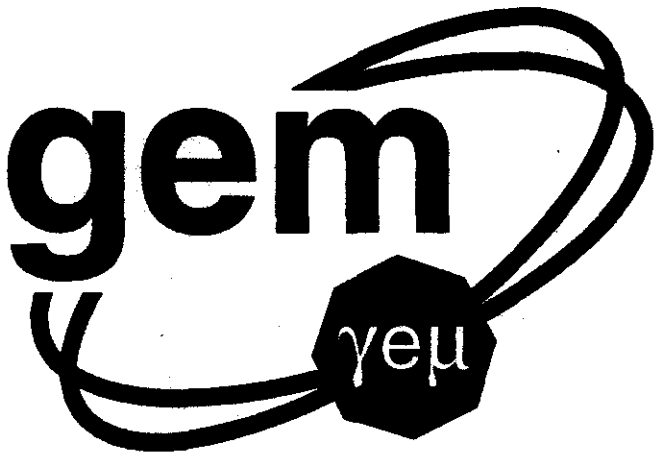
- Conservative estimate prior to Baseline 2
- Next iteration with Baseline 2 will be ready for 10 MAR meeting

Schedule

- Timing Electronics studies with RD-5 Chamber
- Summer 1993 Prototype Chamber Electronics
- Prototype Electronics — to be coordinated.
- Production Electronics — to be coordinated.

Man Power/Resources

- To be coordinated with rest of CSC Electronics Group: *BU,BNL,PNPI,PU,UH*,etc.



Presentation by:

L. Pinsky

2/24/93

GEM MUON READOUT

"MOTHERBOARD"

FUNCTIONS:

1. TRIGGER – PASS SIGNALS FROM ANODES TO LEVEL 1 DECISION MAKER (NOT DISCUSSED HERE)!

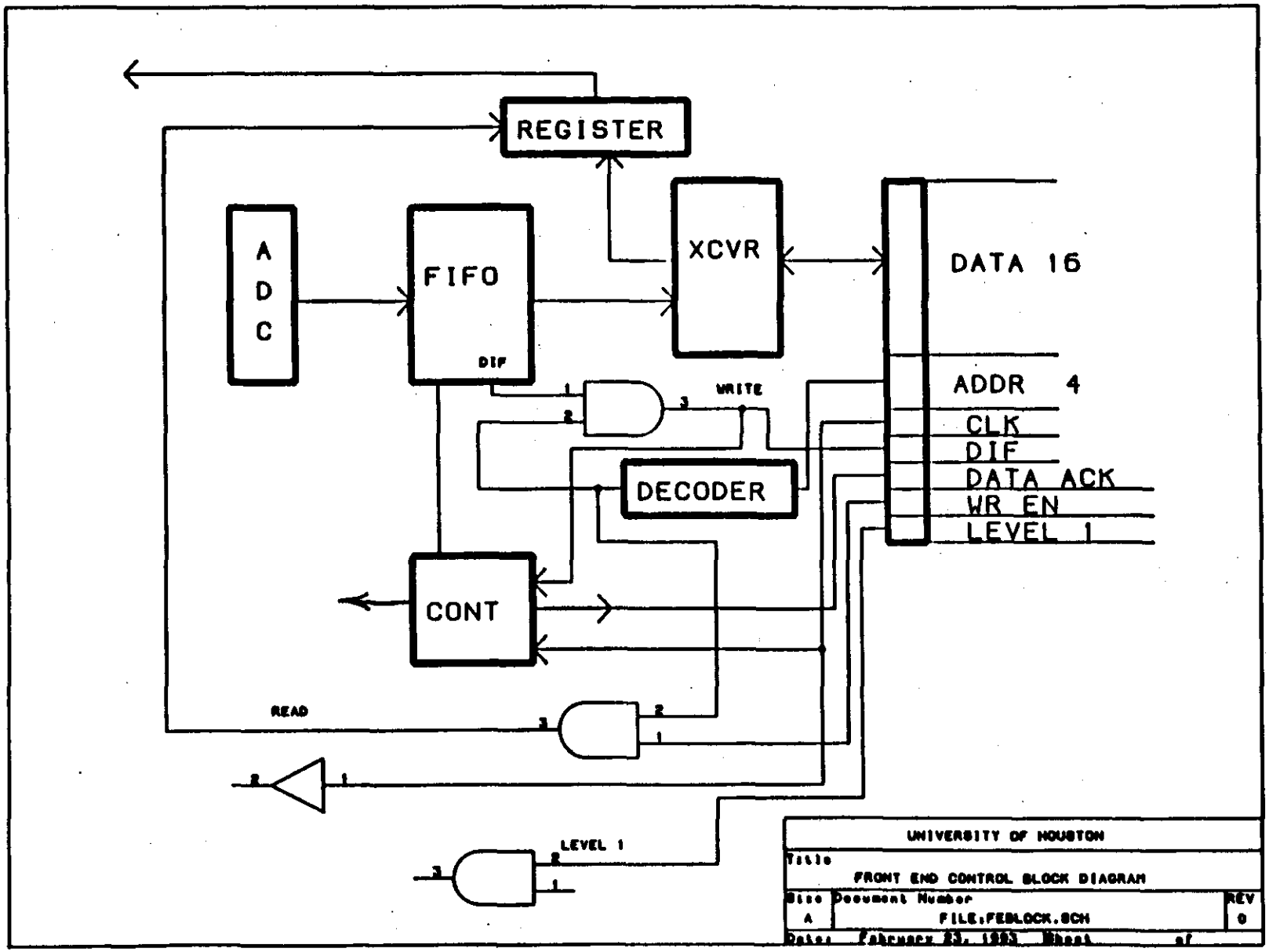
2. DAQ – COLLECT ADC & ANODE DATA FROM F.E. BOARDS AND PASS DATA VIA FIBER OPTIC LINK TO DAQ...

3. 10 MHZ CLOCK – PROVIDE A COMMON CLOCK

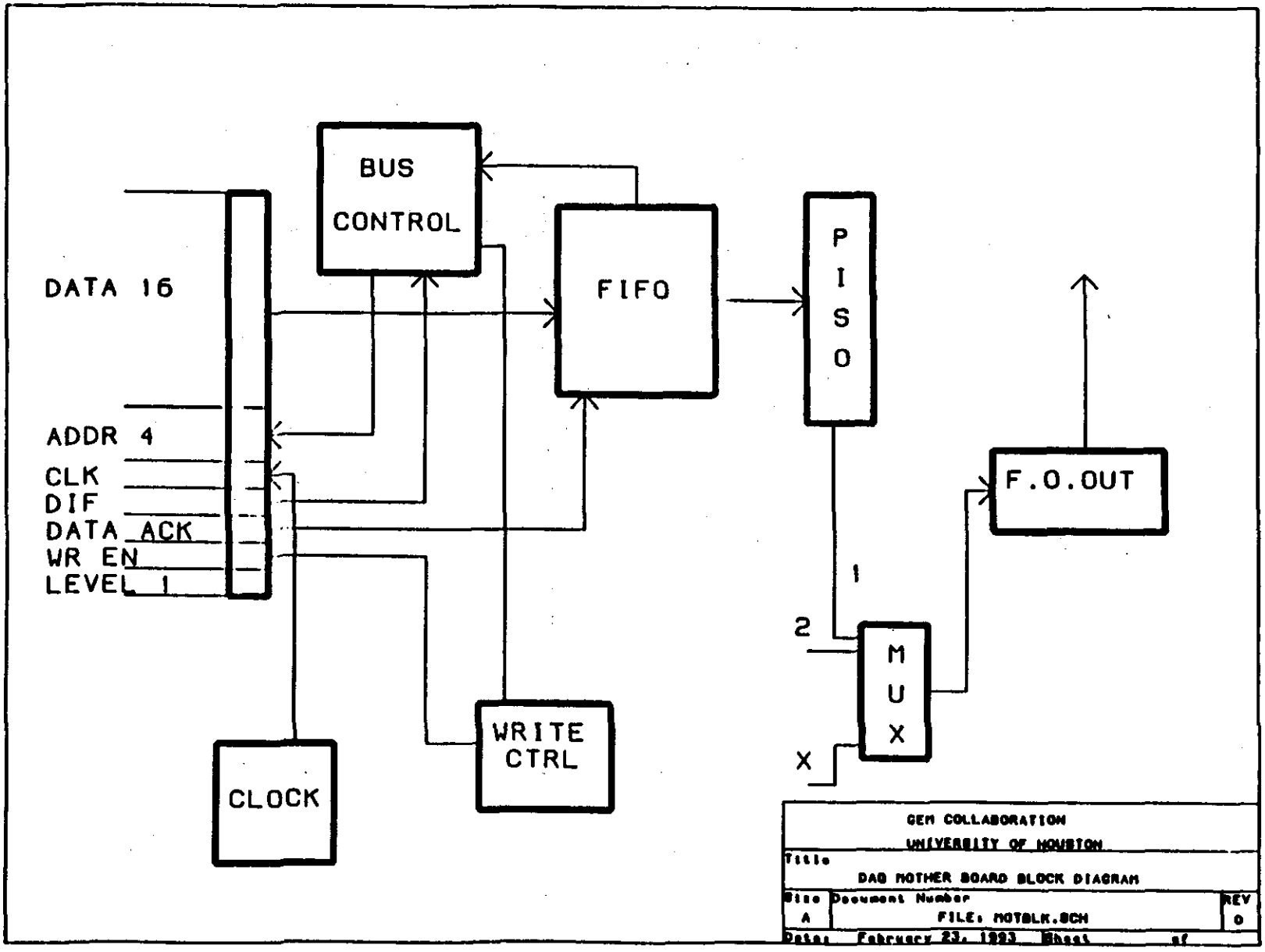
4. LEVEL 1 – DISTRIBUTE LEVEL 1 TRIGGER TO FE BOARDS

5. WRITE TO FE BOARDS – PROVIDE THE POSSIBILITY TO WRITE TO FE BOARDS (e.g. RESET LEVEL1 COUNTER

6. INTERMEDIATE BUFFER CAPACITY – ADD TO TOTAL DATA BUFFER CAP.


REGISTER
A
D
C
FIFO
DIF
XCVR
DATA 16
ADDR 4
CLK
DIF
DATA ACK
WR EN
LEVEL 1
WRITE
DECODER
CONT
READ
LEVEL 1
UNIVERSITY OF HOUSTON
Title
FRONT END CONTROL BLOCK DIAGRAM
Size
A
Document Number
FILE:FEBLOCK.SCH
REV
0
Date: February 23, 1993 Sheet of

2/24/93


BUS
CONTROL
FIFO
P
I
S
O
DATA 16
ADDR 4
CLK
DIF
DATA ACK
WR EN
LEVEL 1
F.O.OUT
1
2
M
U
X
X
WRITE
CTRL
CLOCK
GEM COLLABORATION
UNIVERSITY OF HOUSTON
Title
DAQ MOTHER BOARD BLOCK DIAGRAM
Size
A
Document Number
FILE: MOTBLK.SCH
REV
0
Date: February 23, 1993
Sheet
of

2/24/93

GEM MUON READOUT

"MOTHERBOARD"

CONSIDER THE VARIOUS LIMITING RATES

NO ZERO SUPPRESSION:

144 x 5 (SCA BINS/CH) x 10 (BITS) = 900 BYTES/EV/FE

w/ 16 BIT BUS @ 10 MHZ → 20 MBYTES/SEC

2000 BYTES / 100 μS LATENCY PERIOD!

→ ~ 2 FE BOARDS MAX!

WITH (FACTOR OF 2) ZERO SUPPRESSION:

~ 4 FE BOARDS MAX / 100 μS LATENCY PERIOD!

CONSIDER TRYING TO READOUT 10 FE BOARDS: (2 CSC MODULES)

2000 BYTES / 10 = 200 BYTES / MBD

$\frac{200}{900}$ → ~ 22% NON-ZERO MAX

↓

~ 5 NON-ZERO STRIPS / LAYER MAX!

USING 1 MBD / CSC MODULE → 10 NON-ZERO STRIPS/LAYER

2/24/9_

GEM MUON READOUT

"MOTHERBOARD"

CONSIDER THE VARIOUS LIMITING RATES

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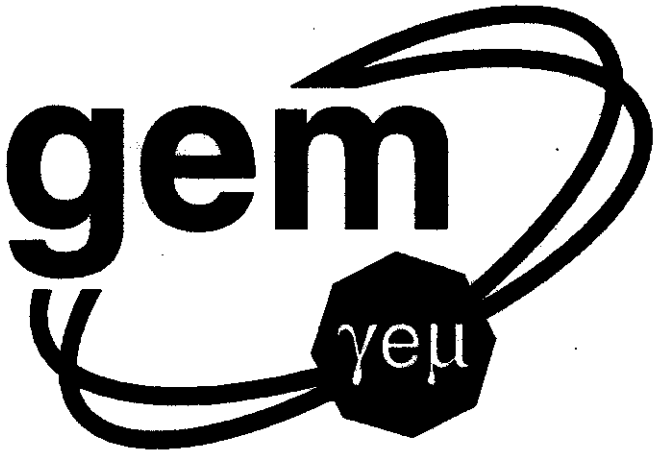


Presentation by:

W. Cleland

CALORIMETER LEVEL 1 TRIGGER

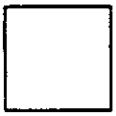
1. Specifications
2. Trigger Sums
3. Noise considerations
4. Discriminator performance
5. System description
   - Block diagam
   - Description of modules
   - Location of modules
6. Trigger latency

CALORIMETER LEVEL 1 TRIGGER SPECIFICATIONS

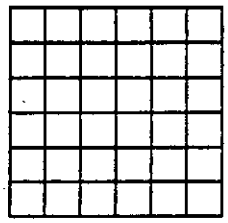
- Latency:
  - Total latency $\leq$ 2000 ns
  - Cable/fiber runs $\approx$ 1270 ns
  - Peaking time for hadronic shapers $\approx$ 150 ns
  - Assumption for ~~global~~ level 1 logic: 70 ns
- Synchronism: Level 1 trigger data must be made available for each bunch crossing (pipelined architecture).
- Minimal set of primitives:
  - Numbers of hits above several threshold values:
    - isolated EM clusters
    - isolated hadronic clusters
    - jet clusters
  - Global data, digital values:
    - Missing transverse energy
    - Total transverse energy
- Programmable.

EM cell
(.027x.027)

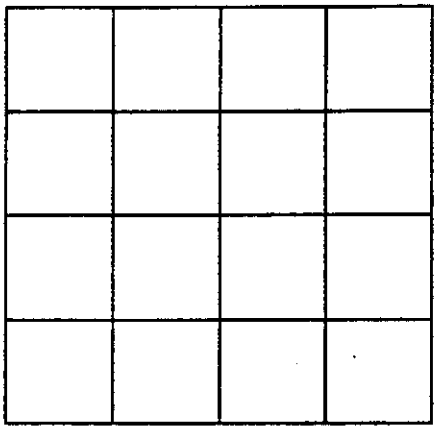
HAD cell
(.08x.08)



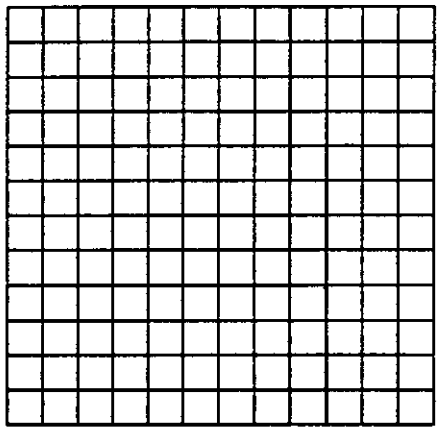
EM = 6X6 EM cells
(.16 x .16)



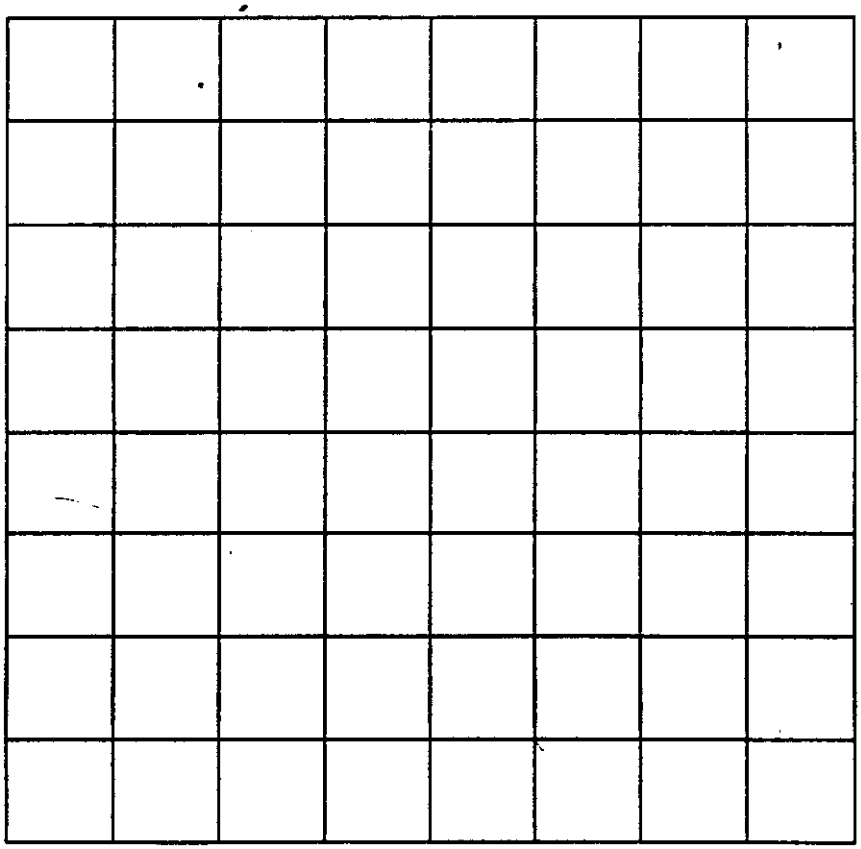
SP = 4x4 HAD
(.32 x .32)



SPEM = 2X2 EM
(.32 x .32)



JET = 2x2 SP
(.64 x .64)



LIMITATIONS DUE TO PILEUP AND THERMAL NOISE

- **Assumptions:**
  - **EM thermal noise from BNL test**
  - **Hadronic thermal noise from Kistinev estimates**
  - **Pileup noise density formula:**

$$\rho_p = 380(\Delta\eta\Delta\phi)^{0.76}(\frac{\mathcal{L}}{\mathcal{L}_0})^{\frac{1}{2}}\mathrm{MeV}/\sqrt{\mathrm{ns}}$$

- **Single sample amplitude resolution (t_m = 40 & 70 ns):**

4λ

Trigger tower		σ_{sample}(GeV)	
Type	$\Delta\eta\Delta\phi$	10^{33}	10^{34}
EM	0.16 × 0.16	0.19	0.56
SP	0.32 × 0.32	1.1	2.5
JET	0.64 ×0.64	2.6	7.0

- **Amplitude resolution from optimal filtering:**

4λ

Trigger tower		σ_E(GeV)	
Type	$\Delta\eta\Delta\phi$	10^{33}	10^{34}
EM	0.16 × 0.16	0.19	0.52
SP	0.32 × 0.32	1.0	2.4
JET	0.64 ×0.64	2.4	6.5

TIMING PERFORMANCE

- **Discriminator is Turko-Smith design**
- **Tested for calorimeter signals in BNL LKr test (7/90)**
- **Experimental timing resolution (before corrections): ≈1 ns for 15 GeV signals**
- **Timing resolution for discriminator for t_p=40 & 70 ns:**

4 λ

Trigger tower		E σ_t(GeV-ns)	
Type	$\Delta\eta\Delta\phi$	10^{33}	10^{34}
EM	0.16 × 0.16	11	33
SP	0.32 × 0.32	100	234
JET	0.64 ×0.64	248	656

- **Timing resolution from optimal filtering:**

4 λ

Trigger tower		Eσ_t(GeV-ns)	
Type	$\Delta\eta\Delta\phi$	10^{33}	10^{34}
EM	0.16 × 0.16	5.0	6.7
SP	0.32 × 0.32	60	80
JET	0.64 ×0.64	132	175

- **To achieve required timing accuracy for jets of ≈ 30 GeV, digital filter is required.**

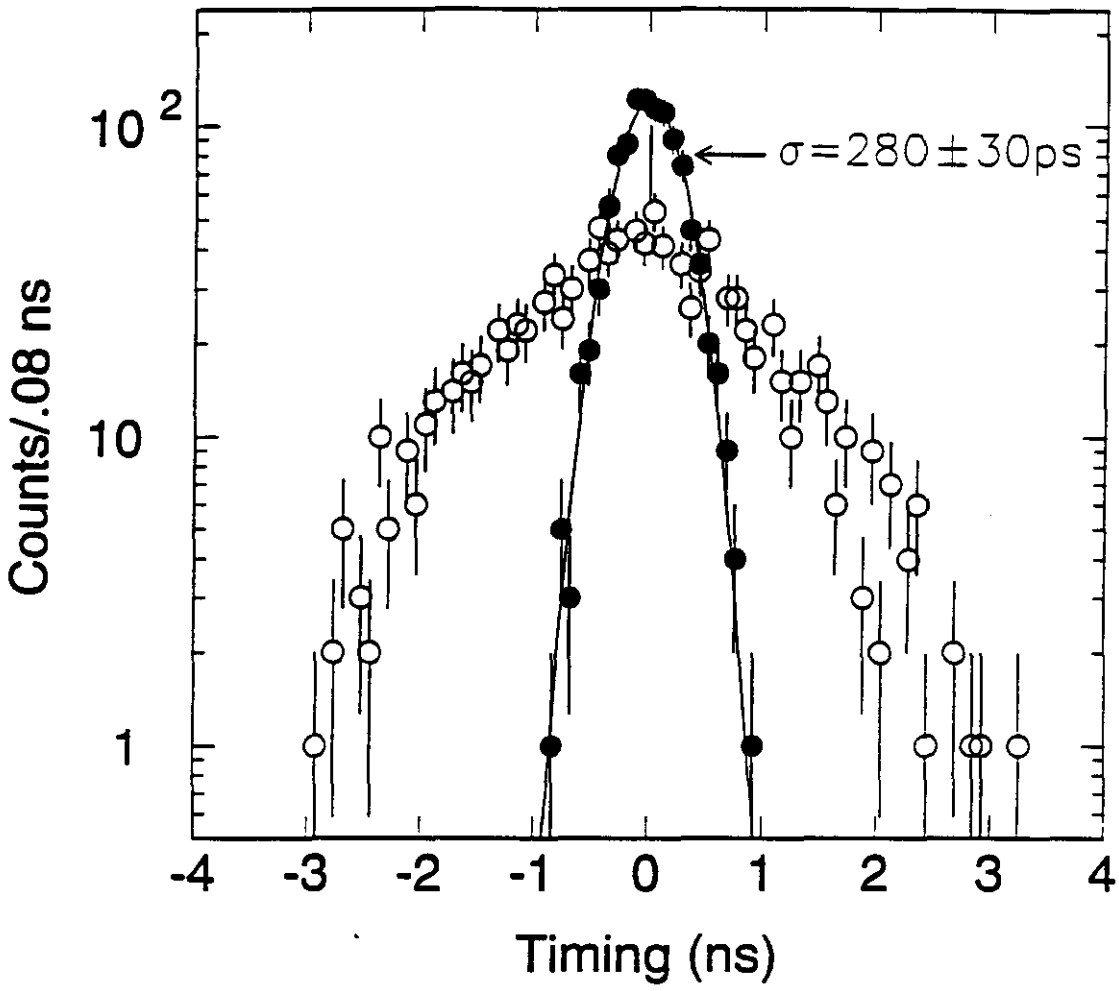


FIGURE 6

GLOBAL SUMS AND TIMING FILTER

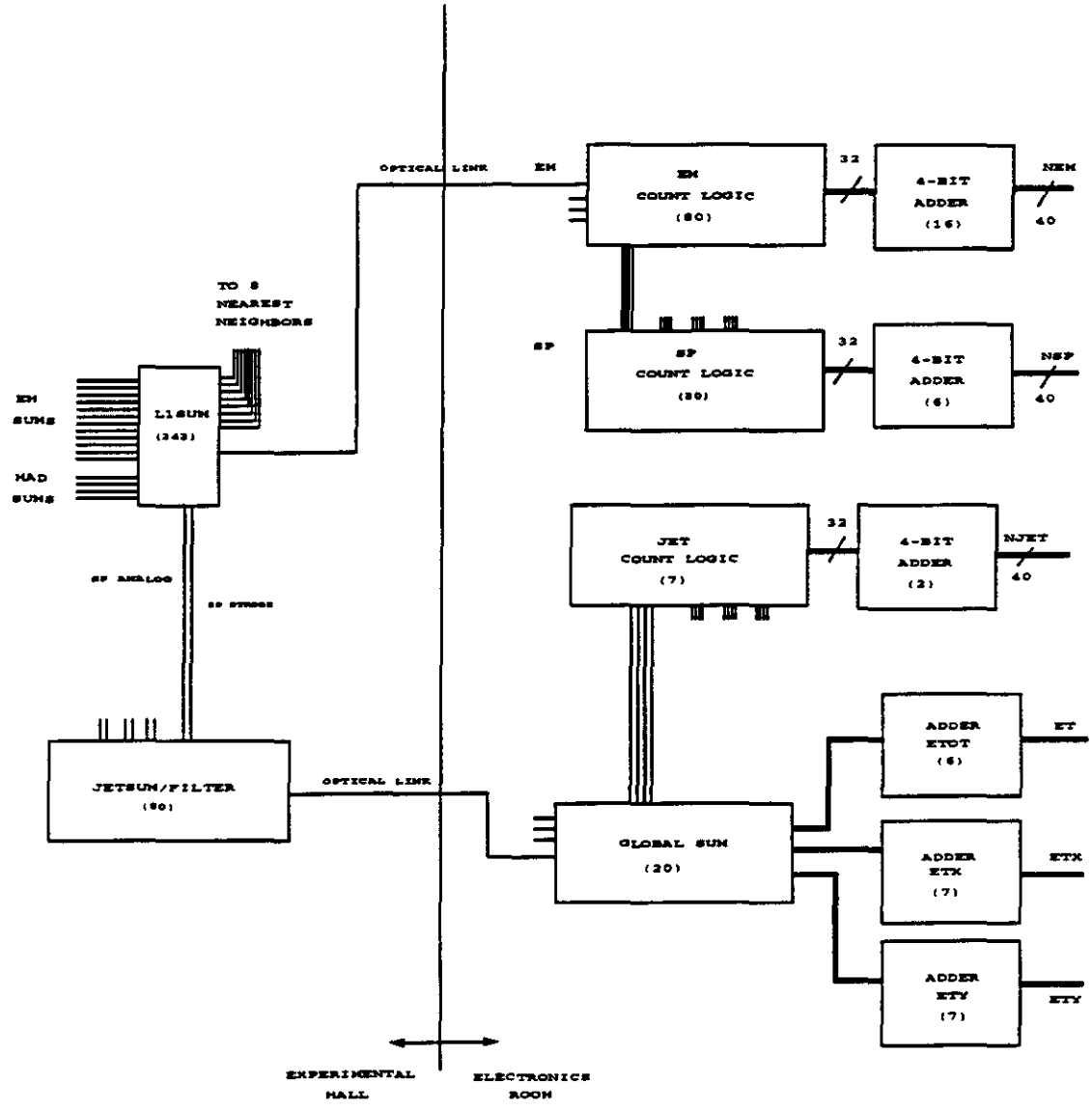
- **To establish crossing for a jet, require 25-30 GeV threshold**
- **Probability for an out-of-time jet in 400 ns $\approx$ 5**
- **Following suggestion of F. Paige (PN 91-1), sum only energy in jets.**
- **Errors introduced by jet filter:**

Source of error	$\sigma(E_T)$ (GeV)	$\sigma(E^{\text{miss}})$ (GeV)
Geometry	0	3.3
Threshold (25 GeV)	40	21
Pileup (5 Jet Sums)	13	10
Jet noise ($\overline{n} \approx 2$)	5.3	7.5
Total	42	25

- **Comparison of linear vs. filtered sum:**

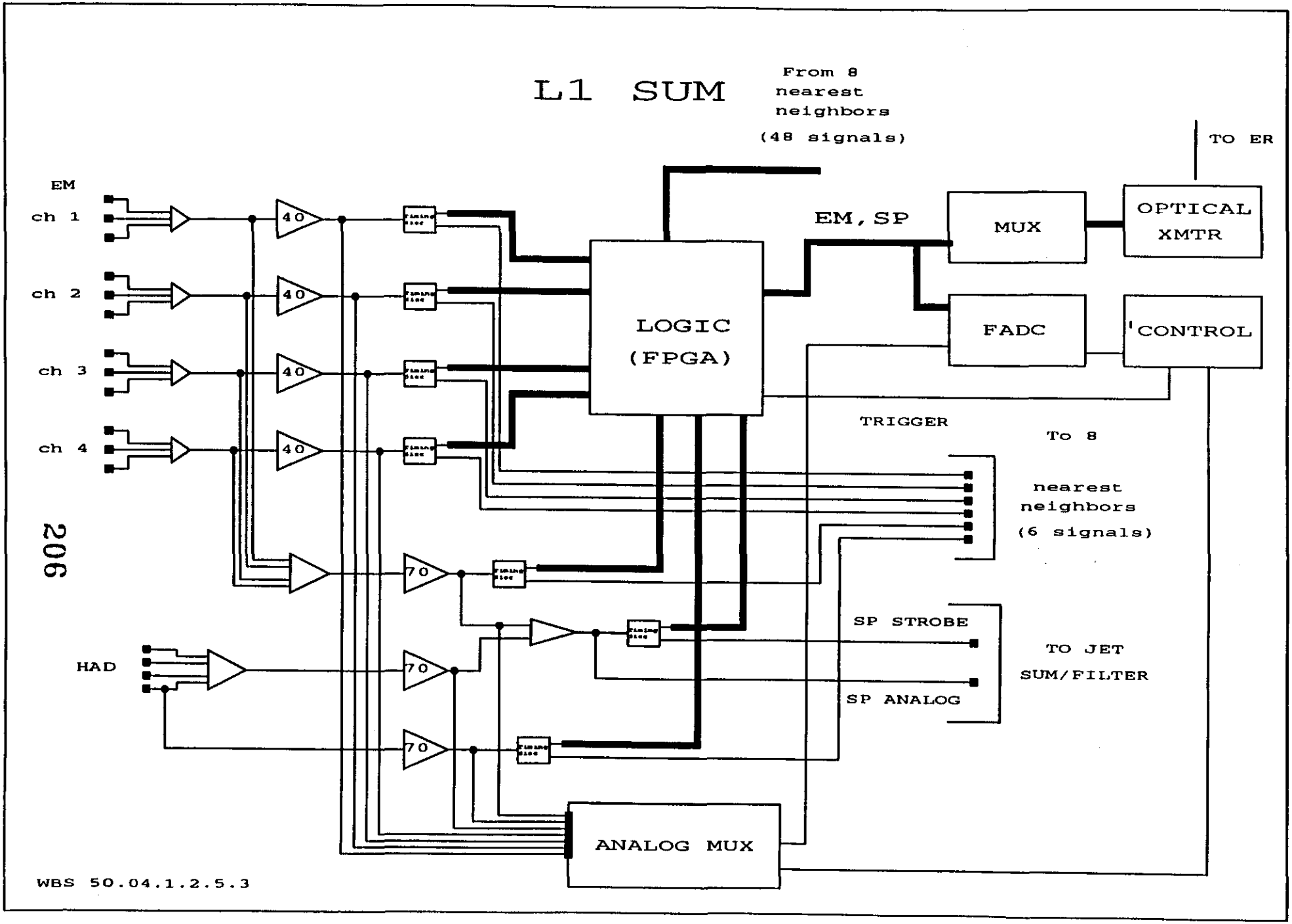
Condition	σ_E(GeV)		$E\sigma_t$(GeV-ns)	
	10^{33}	10^{34}	10^{33}	10^{34}
Linear sum (OF)	54	128	760	1000
Filtered sum	42	45	–	–

LEVEL 1 CALORIMETER TRIGGER



L1 SUM

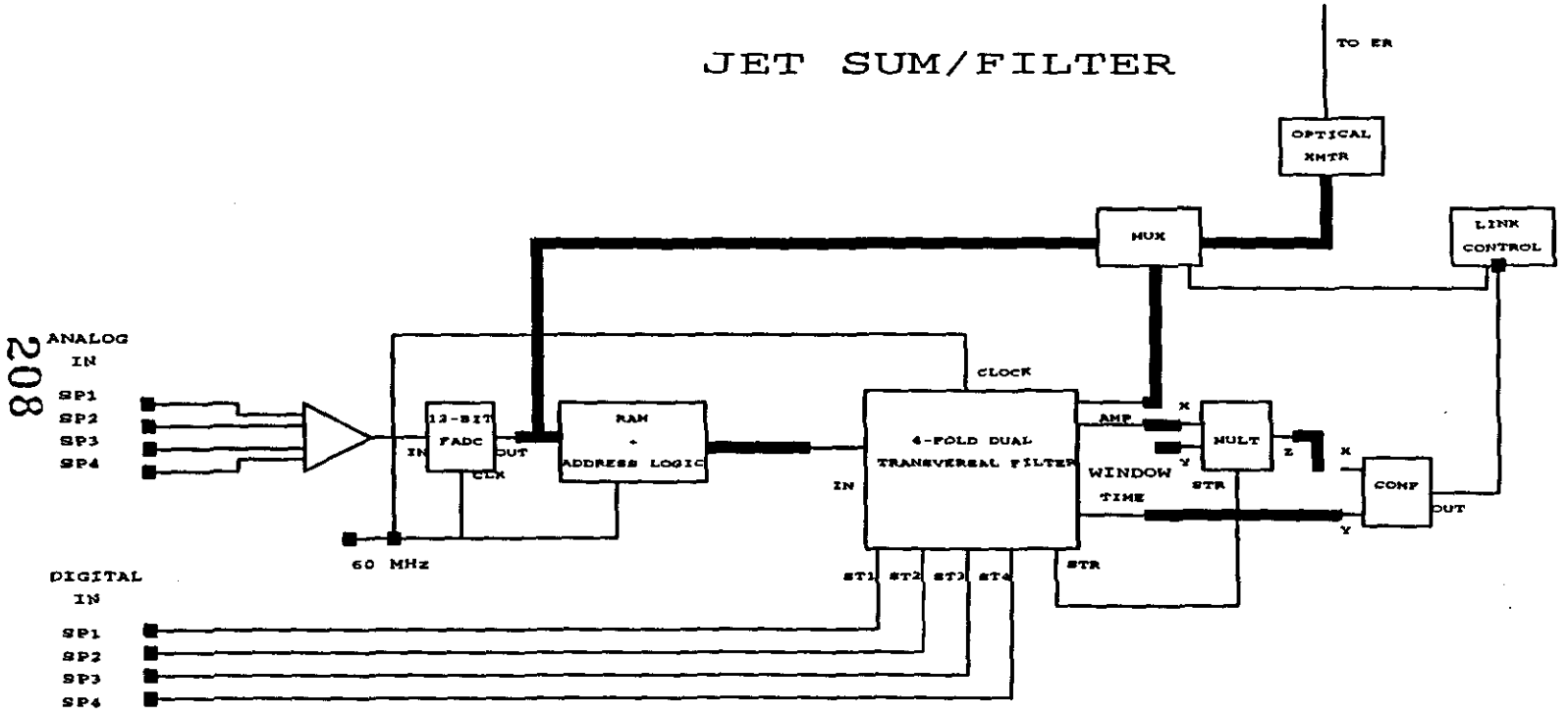
- **Location: Front end electronics racks (1 per crate)**
- **Functions:**
  1. **Form analog sums of different floors**
  2. **Equalize average gains**
  3. **Discriminate all sums (7 levels)**
  4. **Perform beam synchronization and nearest neighbor isolation logic (FPGA)**
  5. **Provide monitoring data for analog waveform**
- **Inputs**
  - **Analog sums from EM and hadronic front end boards**
  - **Discriminator signals from nearest neighbors**
- **Outputs**
  - **Discriminator signals to nearest neighbors**
  - **Analog/digital SP signals to Jet Sum boards**
  - **Isolation logic EM and SP signals to Edge Count logic (via optical link)**
  - **Analog waveform monitoring information (via optical link)**


L1 SUM
From 8 nearest neighbors (48 signals)
TO ER
EM
ch 1
ch 2
ch 3
ch 4
40
40
40
40
EM, SP
MUX
OPTICAL XMTR
LOGIC (FPGA)
FADC
CONTROL
TRIGGER
To 8 nearest neighbors (6 signals)
70
70
70
HAD
SP STROBE
SP ANALOG
TO JET SUM/FILTER
ANALOG MUX
206
WBS 50.04.1.2.5.3

JET SUM/FILTER

- **Location: Front end electronics racks (1 per 4 crates)**
- **Functions**
  1. **Perform analog addition of 4 SP signals**
  2. **Digitize and store samples each 16 ns**
  3. **Perform optimal filter algorithm to obtain Jet energy associated with crossing**
  4. **Provide monitoring of analog waveform**
- **Inputs**
  - **Analog signals from L1 Sum**
  - **Discriminator (timing) signals from L1 Sum**
- **Outputs**
  - **Jet energy and timing data (via optical link)**
  - **Analog waveform monitoring information (via optical link)**

JET SUM/FILTER

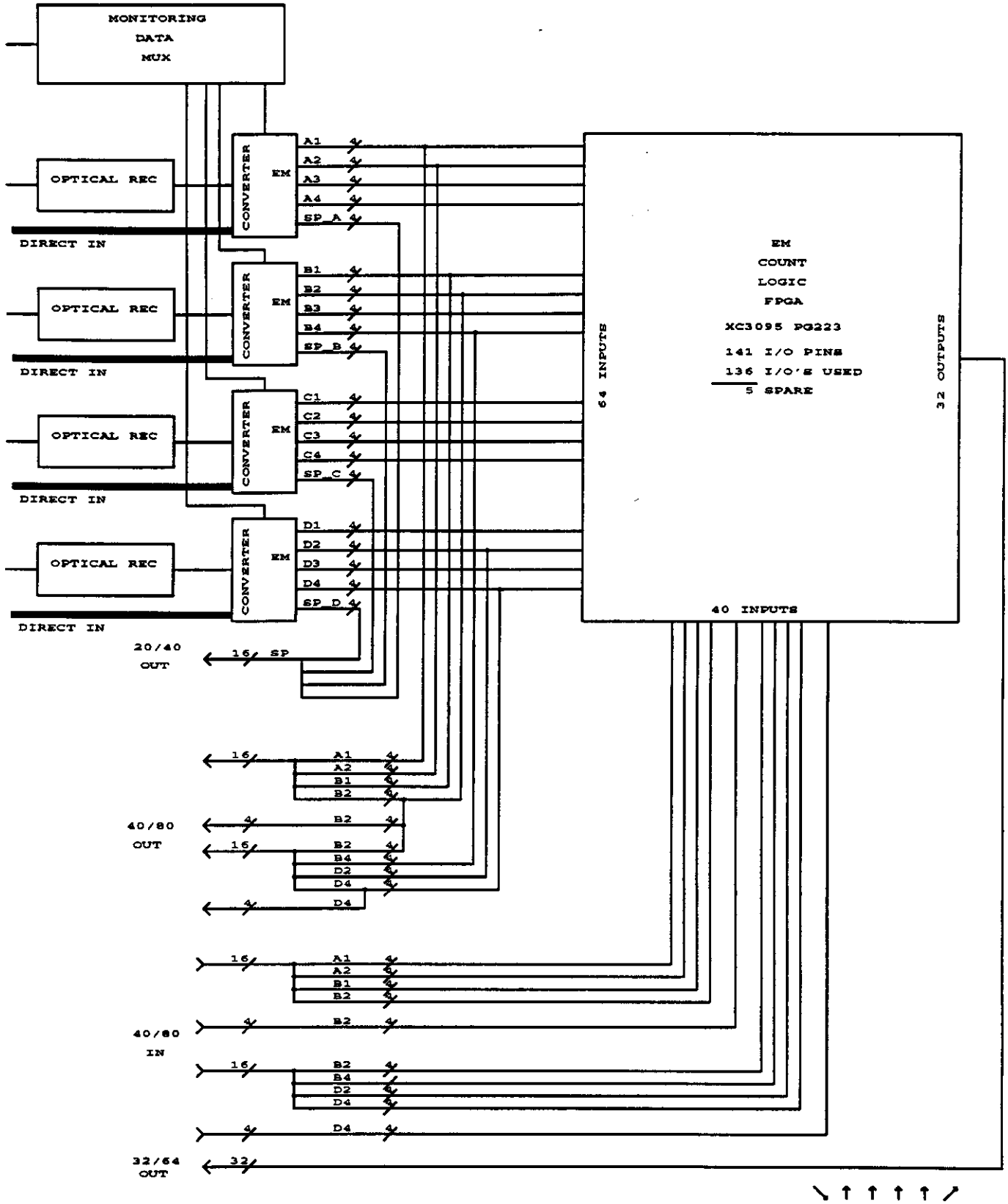


WBS 50.04.1.2.5.5

EM EDGE COUNT

- **Location: ER**
- **Functions**
  1. **Receive EM and SP isolation logic data over optical links**
  2. **Perform cluster counting for each of 8 categories of hits**
- **Inputs**
  - **Optical fibers from 4 L1 sum boards (5 channels, 4 bits/ch each 16 ns)**
  - **Data from neighbors for cluster counting (backplane)**
- **Outputs**
  - **Isolation logic SP data to SP Edge Count**
  - **Data to neighbors for cluster counting (backplane)**
  - **8 sums (cluster count) to adder**
  - **Digital signal for monitoring channel**

COUNT LOGIC

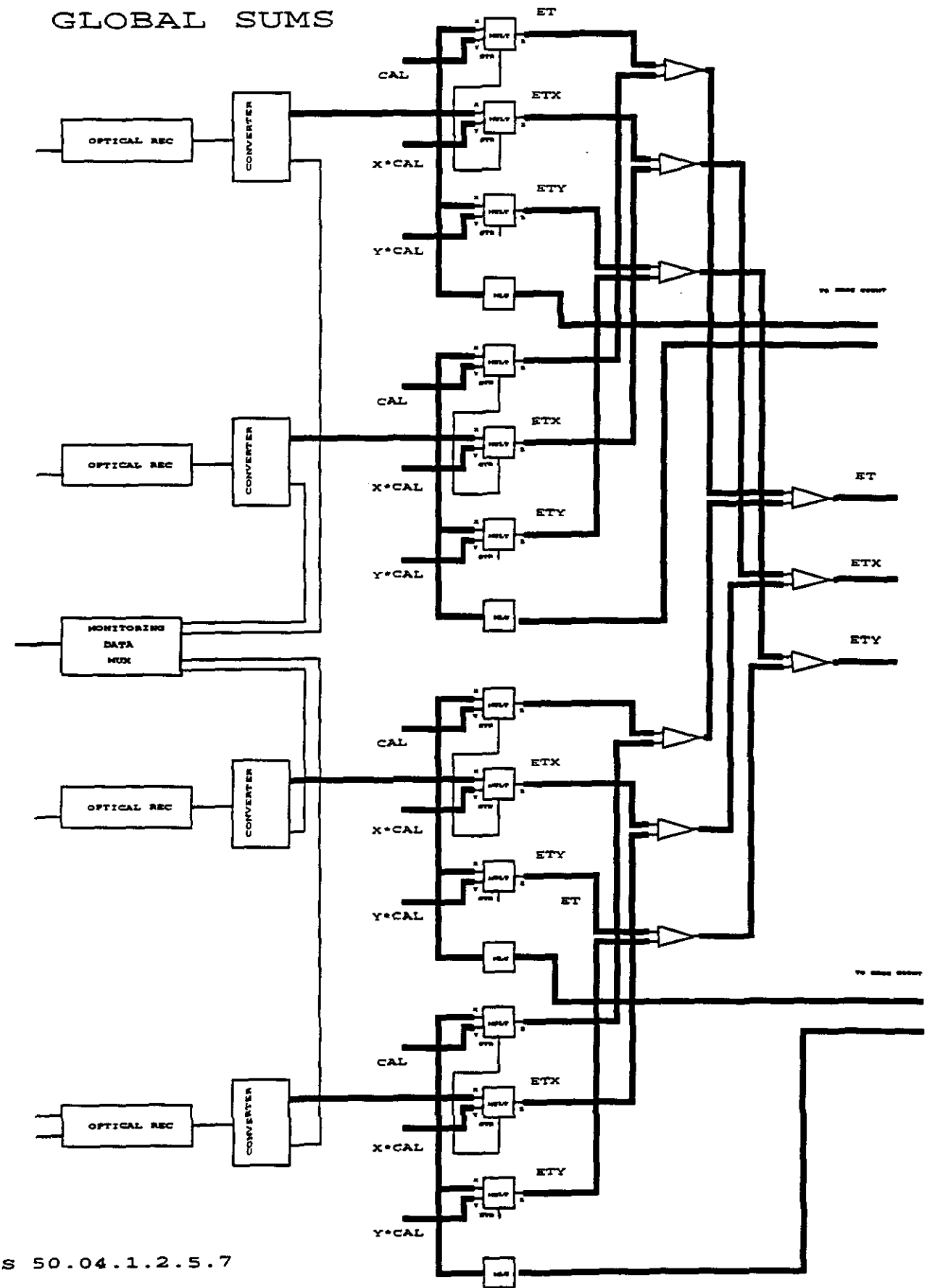


WBS 50.04.1.2.5.4

GLOBAL SUM

- **Location: ER**
- **Functions**
  1. **Receive Jet energy data over optical link**
  2. **Form Jet ET, ETX, ETY for global sums, and make board-level sums**
  3. **Provide "discriminator like" data for edge counting through table lookup**
- **Inputs**
  - **Optical fibers from 4 JET sum boards**
- **Outputs**
  - **Data to JET edge count modules**
  - **3 global sums (ET, ETX, and ETY) summed over 4 channels**
  - **Digital signal for monitoring channel**

GLOBAL SUMS



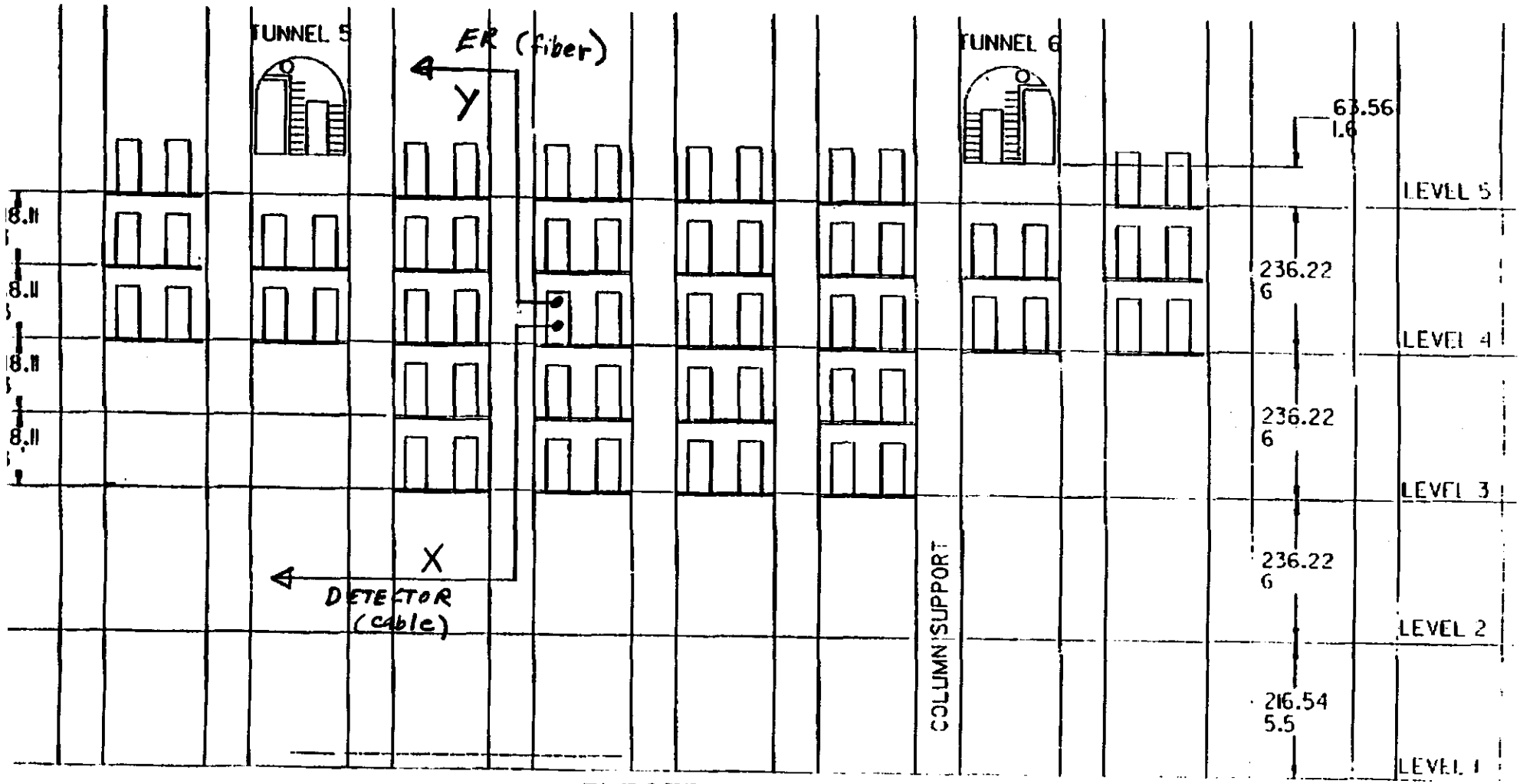
WBS 50.04.1.2.5.7

ADDER

- Functions
  1. Add digital data to form global sums (12 or 16 bit configuration)
  2. Add digital data to form EM, SP, or JET cluster sums (4 or 6 bit configuration)
- Inputs
  - Digital data from global sum, edge count or adder module
- Outputs
  - Digital sums to global level 1 module or follow-on adder

LOCATION OF LEVEL 1 LOGIC

- In experimental hall:
  - L1 Sum (1 per front end crate)
  - Jet Sum/Filter (1 per four front end crates)
- In electronics room:
  - Edge count logic
  - Global sums
  - Adders
- Features:
  - No copper connections between experimental hall and ER.
  - All analog signals are carried over cables $\leq$ 5 m in length.
  - All low level analog signals are discriminated in place.
  - Failures will remove only that particular segment from the trigger.
  - Remote monitoring of waveforms (at 16 ns sampling) available over trigger links.



ELECTRONIC RACK PLACEMENT

Constraint: $X + Y = \text{const}$

TIME BUDGET FOR LEVEL 1 CALORIMETER TRIGGER
ET ETX ETY

	CABLE		VME UNIT			TYP	
EVENT	METERS	ns/m		TYP pd		t	T
TOA at CH (5m @ 3ns/m)						15	15
Cable to Int Amp	12	6.6				79.2	94.2
Intermediate Amplifier *				5		5	99.2
Cable to Racks - Readout (X)	40	5				200	299.2
Readout Boards *				10		10	309.2
Cable to L1 Sum	0.5	5				2.5	311.7
L1 Sum Board (Sum+Shape+Disc+Drv)				216		216	527.7
Cable to Jet Sum/Filter	5	5				25	552.7
Jet Sum/Filter (Trans.Filter + Optical Xmit.)				152.5		152.5	705.2
Optical Fiber to ER (Global Sums) (Y)	80	5				400	1105.2
Global Sums (Logic + Adder Stage 1+2)				103		103	1208.2
Cable to 12-Bit Adder	1	5				5	1213.2
12_Bit Adder Board (Stage 3+4)				48		48	1261.2
Cable to 12-Bit Adder	0.5	5				2.5	1263.7
12_Bit Adder Board (Stage 5+6)				48		48	1311.7
Cable to Global Level 1 Logic	3	5				15	1326.7
Global Level 1 Logic *				100		100	1426.7
ER Xmit. Board (Optical Conv.+Xmit) *				10		10	1436.7
Optical Fiber from ER	120	5				600	2036.7
Optical Receiver (Rec.+ Elec.Conv.) *				10		10	2046.7
TOTAL							2046.7
* = Not Linked to another Worksheet							

TIME BUDGET FOR LEVEL 1 CALORIMETER TRIGGER
JET SUMS

	CABLE		VME UNIT			TYP	
EVENT	METERS	ns/m		TYP pd		t	T
TOA at CH (5m @ 3ns/m)						15	15
Cable to Int Amp	12	6.6				79.2	94.2
Intermediate Amplifier *				5		5	99.2
Cable to Racks - Readout (X)	40	5				200	299.2
Readout Boards *				10		10	309.2
Cable to L1 Sum	0.5	5				2.5	311.7
L1 Sum Board (Sum+Shape+Disc+Drv)				216		216	527.7
Cable to Jet Sum/Filter	5	5				25	552.7
Jet Sum/Filter (Trans.Filter + Optical Xmit.)				152.5		152.5	705.2
Optical Fiber to ER (Global Sums) (Y)	80	5				400	1105.2
Global Sums				55		55	1160.2
Cable to JET Count Logic	1	5				5	1165.2
Jet Count Logic				95		95	1260.2
Cable to Jet 4_Bit Adder	1	5				5	1265.2
JET 4_Bit Adder Board (Stage 1+2)				24		24	1289.2
Cable to JET 4_Bit Adder	0.5	5				2.5	1291.7
JET 4_Bit Adder Board (Stage 3+4)				24		24	1315.7
Cable to Global Level 1 Logic	3	5				15	1330.7
Global Level 1 Logic *				100		100	1430.7
ER Xmit. Board (Optical Conv.+Xmit) *				10		10	1440.7
Optical Fiber from ER	120	5				600	2040.7
Optical Receiver (Rec.+ Elec.Conv.) *				10		10	2050.7
TOTAL							2050.7
* = Not Linked to another Worksheet							

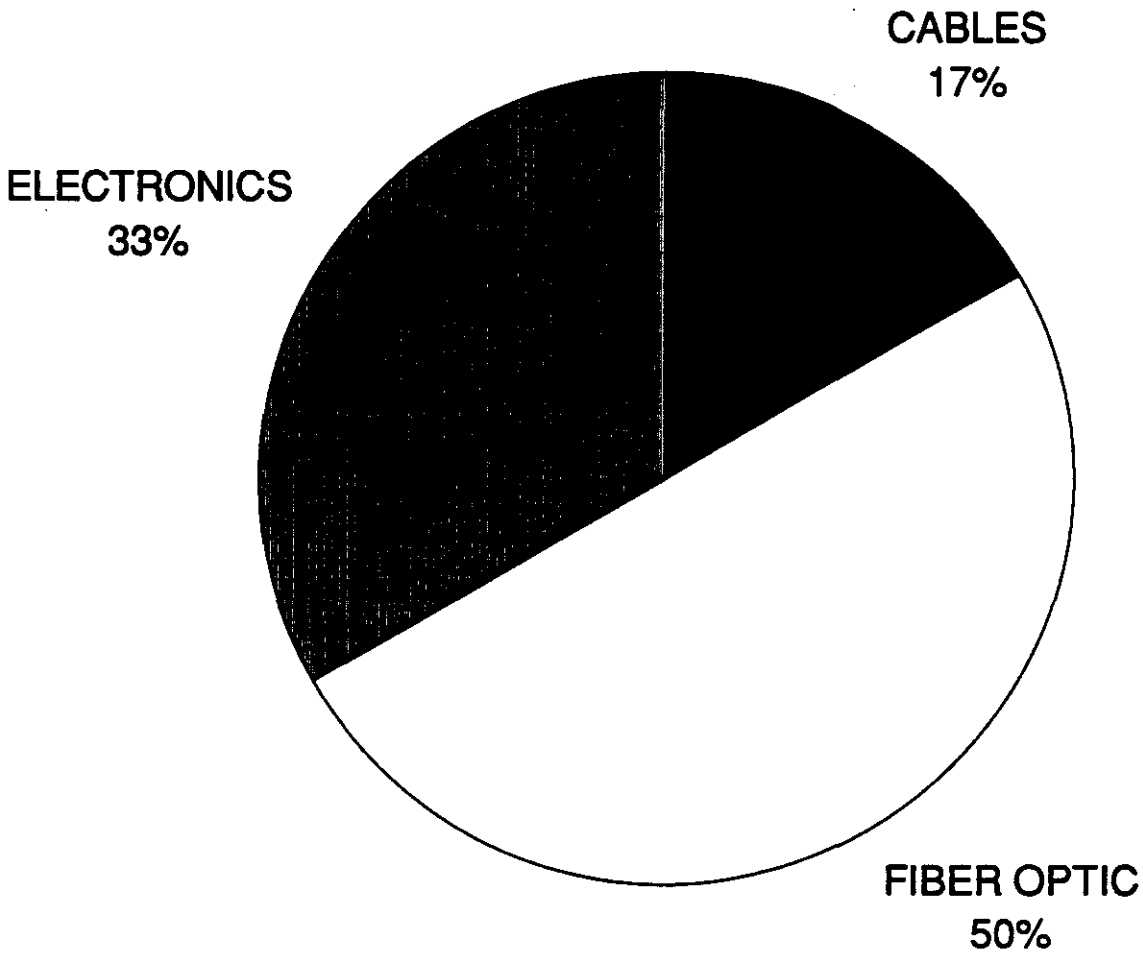
TIME BUDGET FOR LEVEL 1 CALORIMETER TRIGGER
SP SUMS

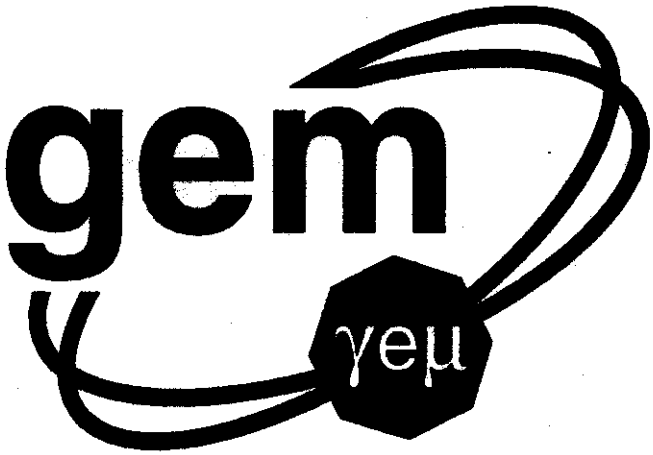
	CABLE		VME UNIT			TYP	
EVENT	METERS	ns/m		TYP pd		t	T
TOA at CH (5m @ 3ns/m)						15	15
Cable to Int Amp	12	6.6				79.2	94.2
Intermediate Amplifier *				5		5	99.2
Cable to Racks - Readout (X)	40	5				200	299.2
Readout Boards				10		10	309.2
Cable to L1 Sum	0.5	5				2.5	311.7
L1 Sum Board (Sum+Shape+Disc+Drv)				211		211	522.7
L1 Sum Transfer to Neighbors	5	5				25	547.7
L1 Sum Board (Logic + Optical Xmit)				105		105	652.7
Optical Fiber to ER (Count Logic) (Y)	80	5				400	1052.7
EM Count Logic * (Optical Rec.)				45		45	1097.7
Cable to SP Count Logic	1	5				5	1102.7
SP Count Logic				95		95	1197.7
Cable to SP 4-Bit Adder	1	5				5	1202.7
SP 4_Bit Adder Board (Stage 1+2)				24		24	1226.7
Cable to SP 4_Bit Adder	0.5	5				2.5	1229.2
SP 4_Bit Adder Board (Stage 3+4)				24		24	1253.2
Cable to SP 4-Bit Adder	0.5	5				2.5	1255.7
SP 4_Bit Adder Board (Stage 5+6)				24		24	1279.7
Cable to Global Level 1 Logic	3	5				15	1294.7
Global Level 1 Logic *				100		100	1394.7
ER Xmit. Board (Optical Conv.+Xmit) *				10		10	1404.7
Optical Fiber from ER	120	5				600	2004.7
Optical Receiver (Rec.+ Elec.Conv.) *				10		10	2014.7
TOTAL							2014.7
* = Not Linked to another Worksheet							

TIME BUDGET FOR LEVEL 1 CALORIMETER TRIGGER
EM SUMS

	CABLE		VME UNIT		TYP	
EVENT	METERS	ns/m	TYP pd		t	T
TOA at CH (5m @ 3ns/m)					15	15
Cable to Int Amp	12	6.6			79.2	94.2
Intermediate Amplifier *			5		5	99.2
Cable to Racks - Readout (X)	40	5			200	299.2
Readout Boards			10		10	309.2
Cable to L1 Sum	0.5	5			2.5	311.7
L1 Sum Board (Sum+Shape+Disc+Drv)			211		211	522.7
L1 Sum Transfer to Neighbors	5	5			25	547.7
L1 Sum Board (Logic + Optical Xmit)			105		105	652.7
Optical Fiber to ER (Count Logic) (Y)	80	5			400	1052.7
EM Count Logic			120		120	1172.7
Cable to EM 4-Bit Adder	1	5			5	1177.7
EM 4_Bit Adder Board (Stage 1+2)			24		24	1201.7
Cable to EM 4_Bit Adder	0.5	5			2.5	1204.2
EM 4_Bit Adder Board (Stage 3+4)			24		24	1228.2
Cable to EM 4-Bit Adder	0.5	5			2.5	1230.7
EM 4_Bit Adder Board (Stage 5+6)			24		24	1254.7
Cable to EM 4-Bit Adder	0.5	5			2.5	1257.2
EM 4_Bit Adder Board (Stage 7+8)			24		24	1281.2
Cable to Global Level 1 Logic	3	5			15	1296.2
Global Level 1 Logic *			100		100	1396.2
ER Xmit. Board (Optical Conv.+Xmit) *			10		10	1406.2
Optical Fiber from ER	120	5			600	2006.2
Optical Receiver (Rec.+ Elec.Conv.) *			10		10	2016.2
TOTAL						2016.2
* = Not Linked to another Worksheet						

TIME BUDGET FOR LEVEL 1 CALORIMETER TRIGGER
AVERAGE FOR SUBSYSTEM





Presentation by:

D. Crosetto

Programmable Digital Level-1 Trigger for Calorimeter

Cost estimate

with

Drawings

WBS No: 50.04.1

WBS number	Description	Engineering/Design			Material &	Inspection/Administrati			Proc/Fab	Assembly			Installation			Totals		
		Labor	Material	Total	Services	Labor	Material	Total	material	Labor	Materia	Total	Labor	Material	Total	SubTotal	DGA	Total
50.04	Trigger			0				0				0			0	0		0
50.04.1	Level 1 Calorimeter			0				0				0			0	0		0
50.04.1.1	**Design/documentation**	**17250**		**17250**				**0**				**0**			**0**	**17250**	**7935**	**25185**
50.04.1.2	**Prototype**	**203352**	**0**	**203352**	**61500**	**0**	**0**	**0**	**187000**	**0**	**0**	**0**	**0**	**21500**	**21500**	**473352**	**217742**	**691094**
50.04.1.2.2.2	Low voltage in-detector			0				0				0			0	0		0
50.04.1.2.2.2.1	Power Supply			0	10000			0				0			0	10000	4600	14600
50.04.1.2.3	Cables and optical fibers	2200		2200	2000			0				0			0	4200	1932	6132
50.04.1.2.4	Active components			0				0				0			0	0		0
50.04.1.2.4.1	3D-Flow chip	86252		86252	40000			0	150000			0		15000	15000	291252	133976	425228
50.04.1.2.5	Printed circuit board			0				0				0			0	0		0
50.04.1.2.5.1	3D-Flow board	11000		11000	500			0	2000			0			0	13500	6210	19710
50.04.1.2.5.2	Optical to electrical board	28250		28250	2000			0	6000			0		2000	2000	38250	17595	55845
50.04.1.2.5.3	Trig sum, ADC, elec - opt	30450		30450	2500			0	7000			0		2000	2000	41950	19297	61247
50.04.1.2.5.6	Energy sum board	28250		28250	500			0	2000			0		500	500	31250	14375	45625
50.04.1.2.6	On-detector crate complete	16950		16950	4000			0	20000			0		2000	2000	42950	19757	62707
50.04.1.3	**Production**	**44600**	**0**	**44600**	**346140**	**0**	**0**	**0**	**1745000**	**0**	**7000**	**7000**	**0**	**210500**	**210500**	**2353240**	**854458**	**3207698**
50.04.1.3.2	Low voltage in-detector			0				0				0			0	0		0
50.04.1.3.2.1	Power supply	6600		6600	5000			0				0			0	11600	5336	16936
50.04.1.3.3	Cables and Optical Fibers	4400		4400	110000			0				0			0	114400	29744	144144
50.04.1.3.4	Active components			0				0				0			0	0		0
50.04.1.3.4.1	3D-Flow chip			0				0	800000			0		20000	20000	820000	377200	1197200
50.04.1.3.5	Printed circuit board			0				0				0			0	0		0
50.04.1.3.5.1	3D-Flow board			0				0	15000		5000	5000			0	20000	9200	29200
50.04.1.3.5.2	Optical to electrical board			0				0	375000			0		62500	62500	437500	201250	638750
50.04.1.3.5.3	Trig sum, ADC, elec - op	20100		20100	125000			0	500000			0		125000	125000	770100	169422	939522
50.04.1.3.5.6	Energy sum board			0				0	30000			0		3000	3000	33000	15180	48180
50.04.1.3.6	On-detector crate complete	13500		13500	4500			0	25000		2000	2000			0	45000	20700	65700
50.04.1.3.7.3	Rack slot			0	101640			0				0			0	101640	26426	128066
50.04.1.4	**Installation & test**			**0**				**0**				**0**		**50000**	**50000**	**50000**	**13000**	**63000**
														Overall Totals:		**2893842**	**1093135**	**3986977**

224

SUBSYSTEM: Electronics
WBS No.: 50.04.1.1

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Design/documentation

WBS QTY: 1

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Engineer/Physicist-SSCL	BU	0.25	MY	SSC02	1,772	38.94		17,250	0	17,250

Notes: Place asterisk at the end of item descriptions if relational.

SUBTOTAL		17,250
DGA	46%	7,935
TOTAL		25,186

Estimated By: Dario Crosetto

Date Estimated: 1/19/93

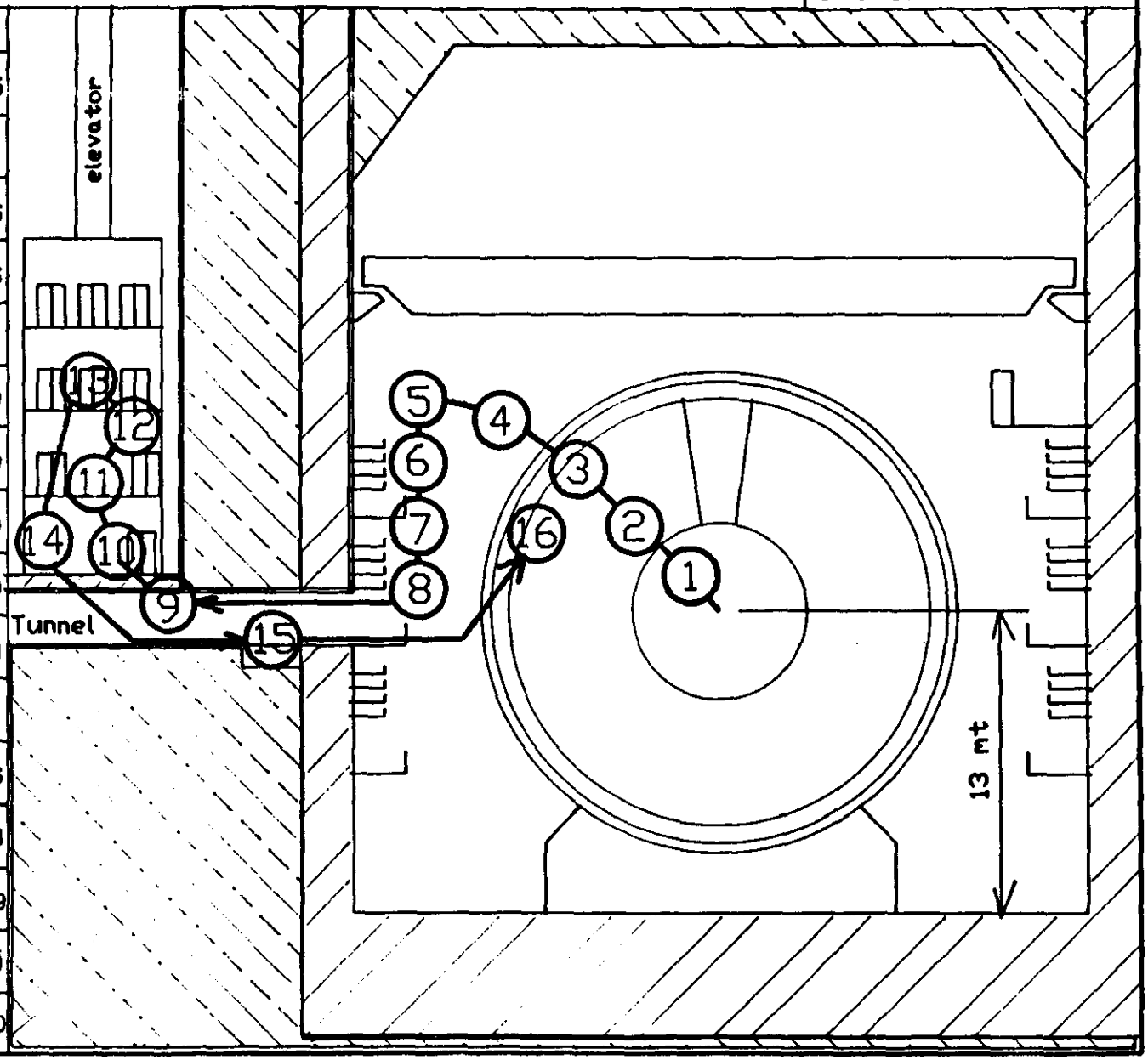
Sheet:

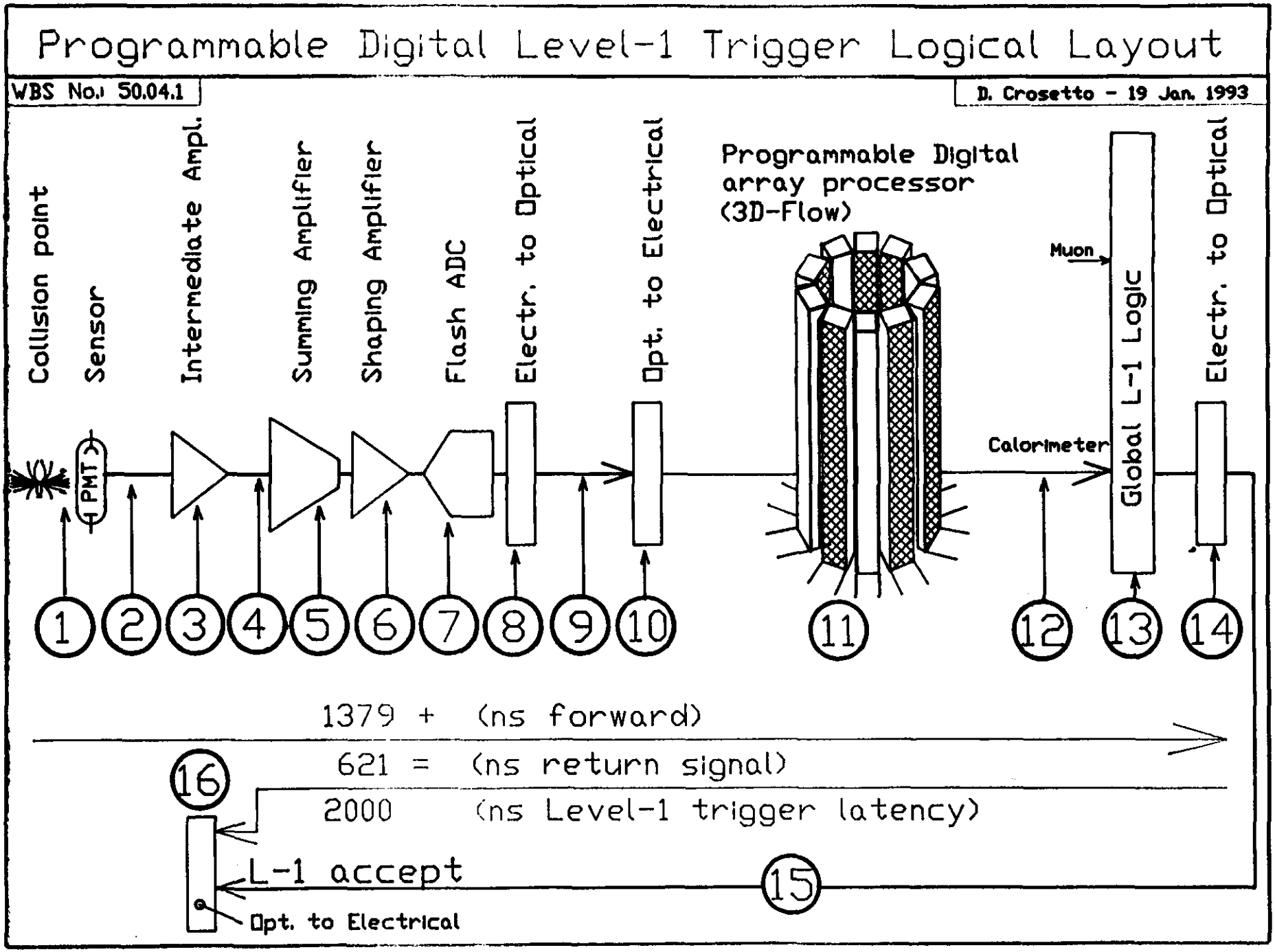
Programmable Digital Level-1 Trigger Physical Layout

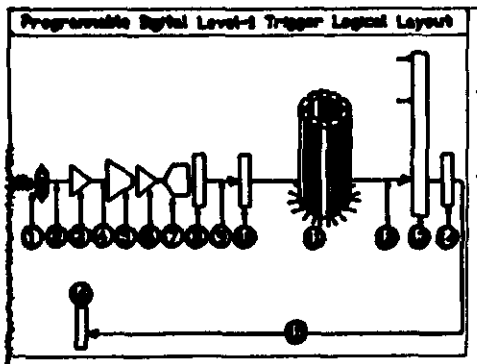
WBS No.: 50.04.1

D. C. SSC – 19 Jan. 1993

	Time (ns)	Δt	t
1	TOA at CH (max 5mt)	15	15
2	Cable to Int Amp (10 mt)	66	81
3	Inter. Ampl.	5	86
4	Cable to platf. (40 mt)	200	266
5	Sum Ampl.	5	271
6	Shape Ampl.	218	489
7	FADC out	20	509
8	Electr. to Optical	21	530
9	Optical Fiber (80 mt)	400	930
10	Optical to Electr.	21	951
11	Digital Proc. (3D–Flow)	500	1451
12	Cable to L–1 GI (5 mt)	25	1476
13	Global L–1 log.	182	1658
14	Electr. to Optical	21	1679
15	Optical Fiber (120 mt)	600	2279
16	Optical to Electr	21	2300




Programmable Digital Level-1 Trigger Logical Layout
WBS No.: 50.04.1
D. Crosetto - 19 Jan. 1993
Collision point
Sensor
Intermediate Ampl.
Summing Amplifier
Shaping Amplifier
Flash ADC
Electr. to Optical
Opt. to Electrical
Programmable Digital
array processor
(3D-Flow)
Muon
Global L-1 Logic
Electr. to Optical
Calorimeter
PMT
1
2
3
4
5
6
7
8
9
10
11
12
13
14
1379 + (ns forward)
621 = (ns return signal)
2000 (ns Level-1 trigger latency)
16
L-1 accept
15
Opt. to Electrical

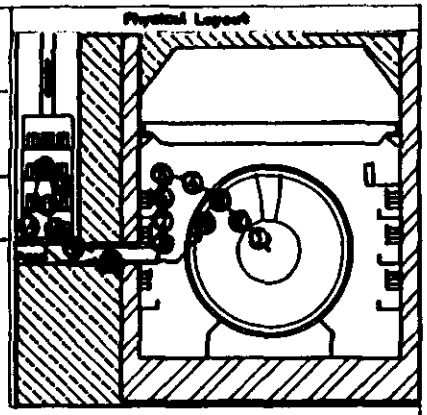


Programmable Digital Level-1 Trigger

SCHEDULE

WBS No.: 50.04.1

D. C. SSC - 19 Jan. 1993



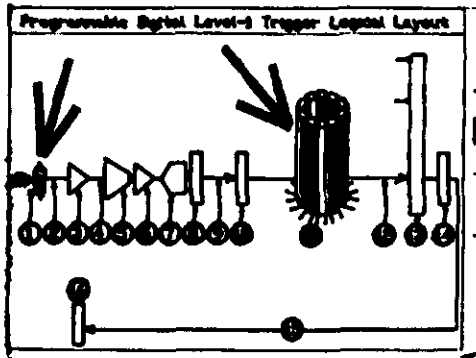
1/92	1/93	1/94	1/95	1/96	1/97	1/98	1/99
50.04.1 - L-1 Calorimeter Digital Trigger							
	Project Management						
	Develop Spec						
		Detail Design					
			Build & Test Prototype				
				Production			
					Assemble		
						Test	
							Install & Integrate

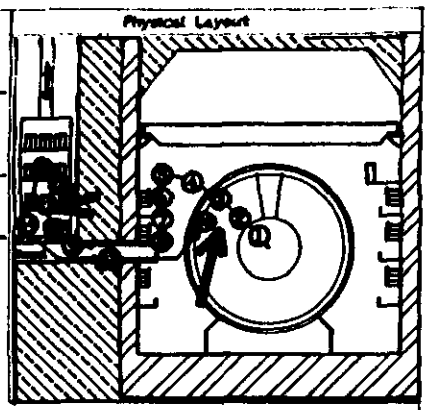
Programmable Digital Level-1 Trigger

Processor Array versus Calorimeter Array

WBS No.: 50.04.1

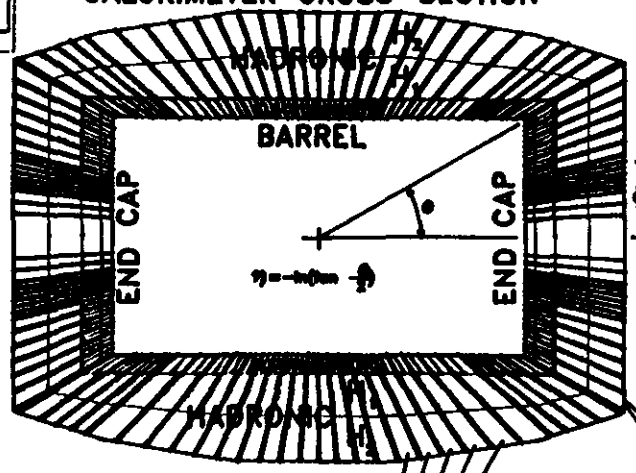
D. Crosetto - 19 Jan. 1993



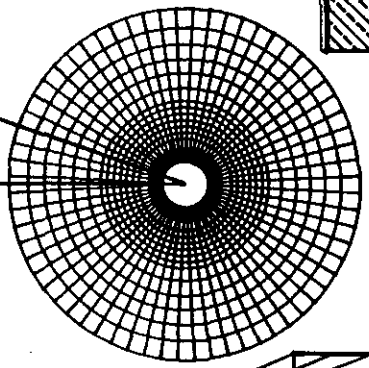


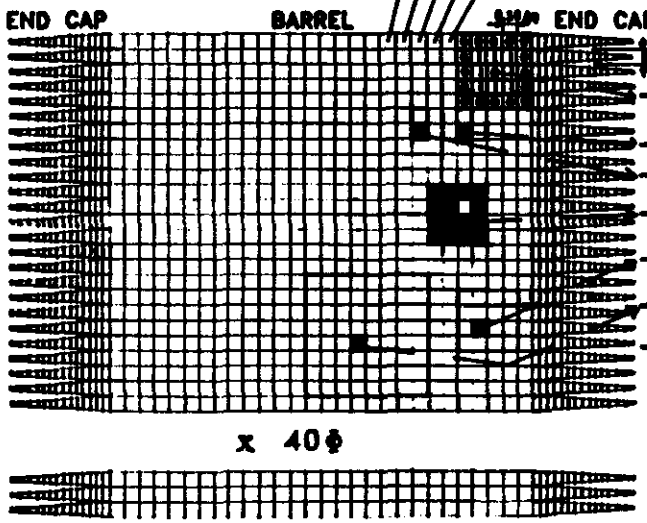
	Time (ns)	Δt	t
①	TOA at CH (max 5mt)	15	15
②	Cable to Int Amp (10 mt)	66	81
③	Inter. Ampl.	5	86
④	Cable to platf. (40 mt)	200	286
⑤	Sum Ampl.	5	271
⑥	Shape Ampl.	218	489
⑦	FADC out	20	509
⑧	Electr. to Optical	21	530
⑨	Optical Fiber (80 mt)	400	930
⑩	Optical to Electr.	21	951
⑪	Digital Proc. (3D-Flow)	282	1233
⑫	Cable to L-1 Gl (5 mt)	25	1258
⑬	Global L-1 log.	100	1358
⑭	Electr. to Optical	21	1379
⑮	Optical Fiber (120 mt)	600	1979
⑯	Optical to Electr.	21	2000

CALORIMETER CROSS-SECTION



END CAP





Unrolled "Barrel" + unfolded END CAP = Towers processor array

Simplified Tower for Level-1 trigger output.

1 level trigger granularity	examples	
Experiment	Δη Δφ	Number of processors
GEM	0.16 x 0.16	1500/stage

ONE TOWER = ONE PROCESSOR

SUBSYSTEM: Electronics
WBS No.: 50.04.1.2.2.2.1

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Power Supply

WBS QTY: 1

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
2-Power supply	BU	20.00	500 watt				500		10,000	10,000

Notes: Place asterisk at the end of item descriptions if relational.
Notes: Based on the cost of $1/watt

SUBTOTAL		**10,000**
DGA	**46%**	**4,600**
TOTAL		**14,600**

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.3.2.1

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Power Supply

WBS QTY: _____

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity: *Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.*

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Cost Basis:

1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Senior Technician-SSCL	BU	0.15	MY	SSC04	1,772	24.83		6,600	0	6,600
2-Material and services	BU	1.00					5,000		5,000	5,000

Notes: Place asterisk at the end of item descriptions if relational.
Notes: Based on the cost of $1/watt.

SUBTOTAL		**11,600**
DGA	**46%**	**5,336**
TOTAL		**16,936**

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.2.3

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Cables and Optical Fibers

WBS QTY: _____

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Senior Technician-SSCL	BU	0.05	MY	SSC04	1,772	24.83		2,200	0	2,200
2-Material and services	BU	1.00					2,000		2,000	2,000

Notes: Place asterisk at the end of item descriptions if relational.

SUBTOTAL		**4,200**
DGA	**46%**	**1,932**
TOTAL		**6,132**

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.3.3

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Cables and Optical Fibers

WBS QTY: _____

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	1%	5%
Cost	5	1%	5%
Schedule	8	2%	16%

Functional Activity:
Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Senior Technician-SSCL	BU	0.10	MY	SSC04	1,772	24.83		4,400	0	4,400
2-Material and services	BU	1.00					110,000		110,000	110,000

Notes: Place asterisk at the end of item descriptions if relational.
Notes: Based on the estimated cost of optical fibers provided by Antel of $.50/meter.

SUBTOTAL		**114,400**
DGA	**26%**	**29,744**
TOTAL		**144,144**

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.2.4.1

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: 3D-Flow Chip

WBS QTY: 10

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity: *Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.*

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Engineer/Physicist-SSCL	BU	1.25	MY	SSC02	1,772	38.94		86,252	0	86,252
2-EDIA Material	BU	1.00					40,000		40,000	40,000
4-Proc/Fab material	BU	1.00					150,000		150,000	150,000
6-Installation material	BU	1.00					15,000		15,000	15,000

Notes: Place asterisk at the end of item descriptions if relational.
Notes: Based on LeCroy cost estimate.

SUBTOTAL		**291,252**
DGA	**46%**	**133,976**
TOTAL		**425,228**

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.3.4.1

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: 3D-Flow Chip

WBS QTY: 4000

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

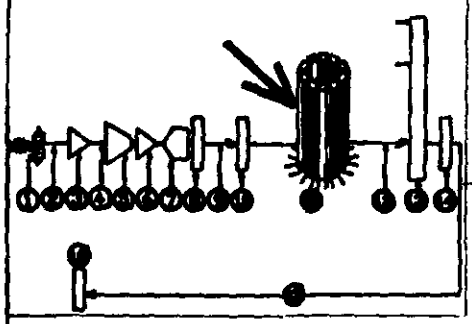
Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
4-Proc/Fab material	BU	4000.00					200		800,000	800,000
6-Installation material	BU	4000.00					5		20,000	20,000

Notes: Place asterisk at the end of item descriptions if relational.
Notes: The final bid among several companies has not yet been placed.

SUBTOTAL		**820,000**
DGA	**46%**	**377,200**
TOTAL		**1,197,200**

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

Logical Layout



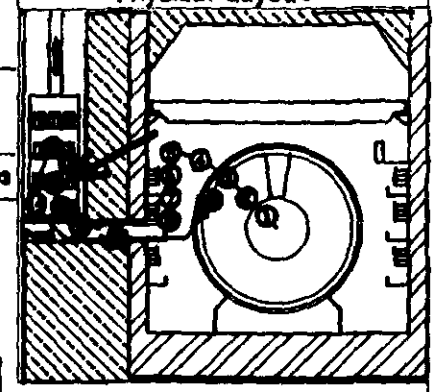
Programmable Digital Level-1 Trigger

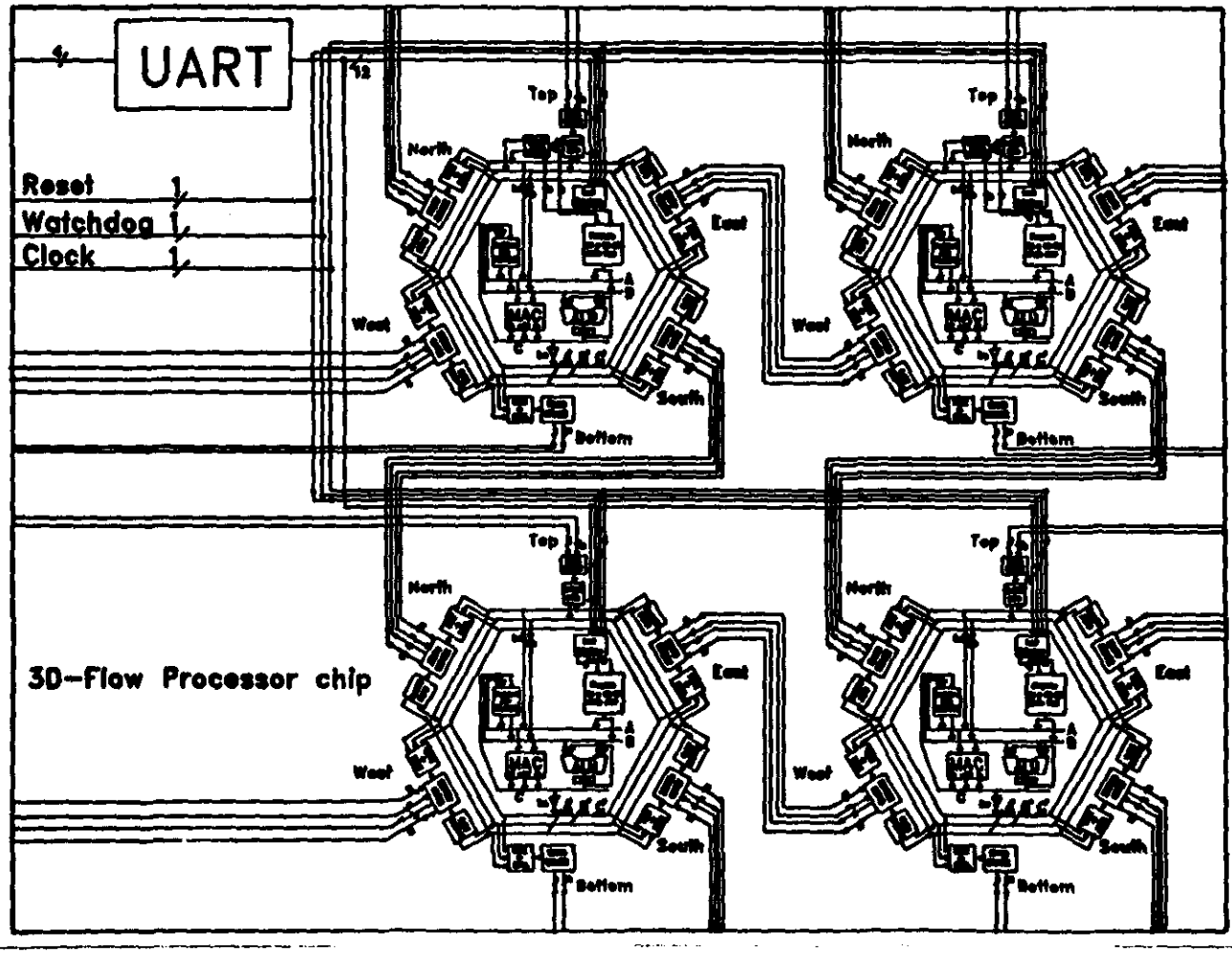
3D-Flow Processor chip

WBS No: 50.04.1.2.4.1

A. Cretaro - 19 Jan. 1998

Physical Layout





	Time (ns)	Δt	t
1	TOA at CH (max 5mt)	15	15
2	Cable to Int Amp (10 mt)	66	81
3	Inter. Ampl.	5	86
4	Cable to platf. (40 mt)	200	286
5	Sum Ampl.	5	271
6	Shape Ampl.	218	489
7	FADC out	20	509
8	Electr. to Optical	21	530
9	Optical Fiber (80 mt)	400	930
10	Optical to Electr.	21	951
11	Digital Proc. (3D-Flow)	282	1233
12	Cable to L-1 GI (5 mt)	25	1258
13	Global L-1 log.	100	1358
14	Electr. to Optical	21	1379
15	Optical Fiber (120 mt)	600	1979
16	Optical to Electr.	21	2000

SUBSYSTEM: Electronics
WBS No.: 50.04.1.2.5.1

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: 3D-Flow board

WBS QTY: 5

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity: *Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.*

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Cost Basis:

1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Senior Technician-SSCL	BU	0.25	MY	SSC04	1,772	24.83		11,000	0	11,000
2-EDIA materials	BU	1.00					500		500	500
4-Proc/Fab materials	BU	1.00					2,000		2,000	2,000

Notes: Place asterisk at the end of item descriptions if relational.

SUBTOTAL		13,500
DGA	46%	6,210
TOTAL		19,710

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.3.5.1

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: 3D-Flow board

WBS QTY: 1000

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
5-Assembly	BU	1000.00					5		5,000	5,000
4-Proc/Fab materials	BU	1000.00					15		15,000	15,000

Notes: Place asterisk at the end of item descriptions if relational.
Notes: Total shown is twice the estimated amount calculated from the guidelines provided.

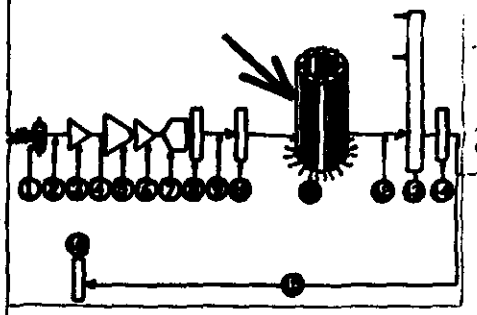
SUBTOTAL		20,000
DGA	46%	9,200
TOTAL		29,200

Estimated By: Dario Crosetto

Date Estimated: 1/19/93

Sheet:

Logical Layout



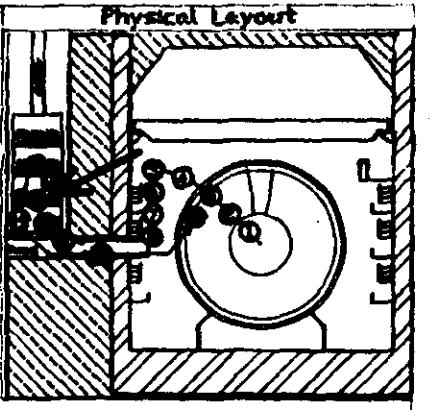
Programmable Digital Level-1 Trigger

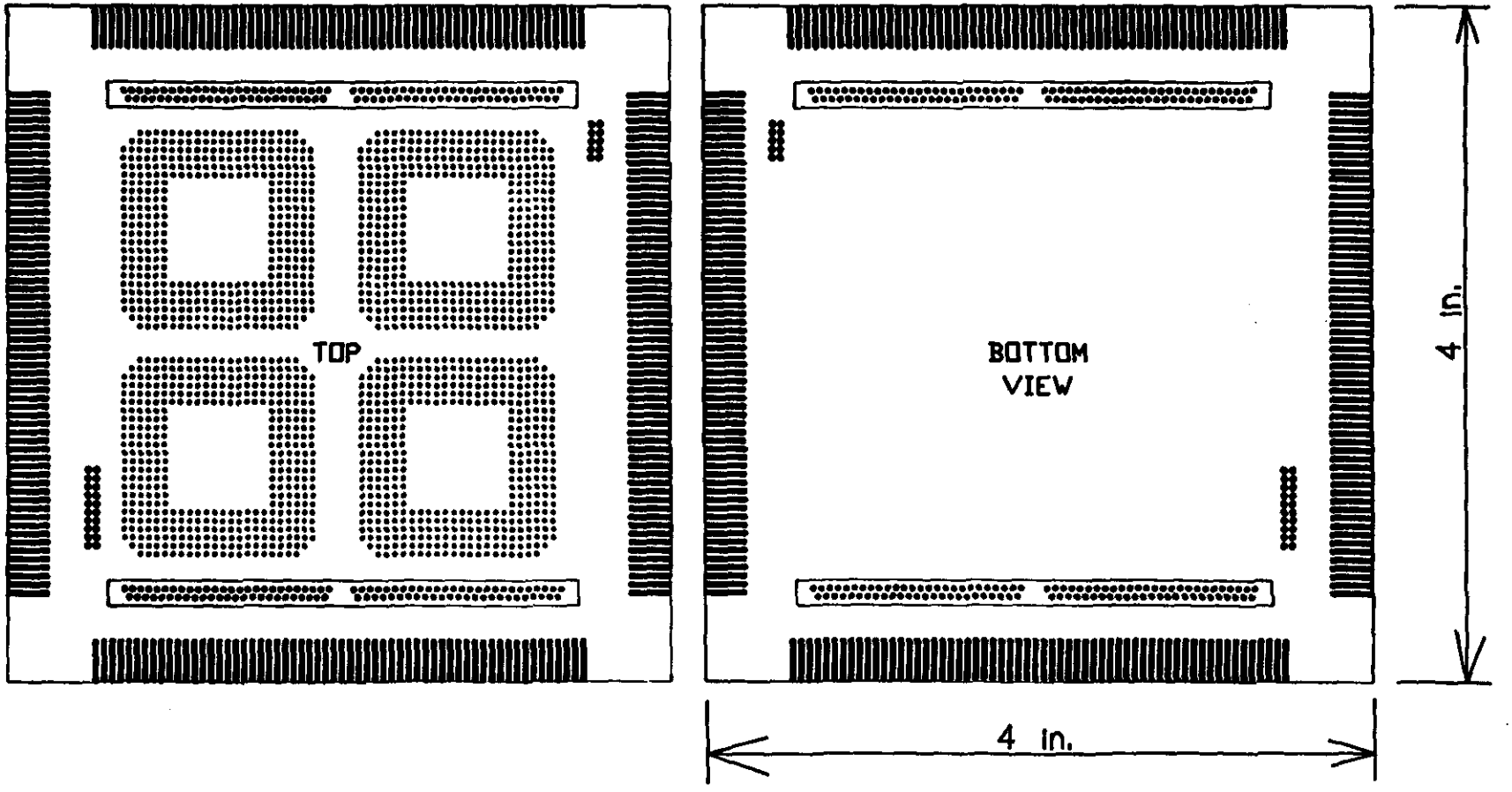
3D-Flow Processor board

VBS No: 50.04.1.2.5.1

A. Crastte - 19 Jan. 1998

Physical Layout





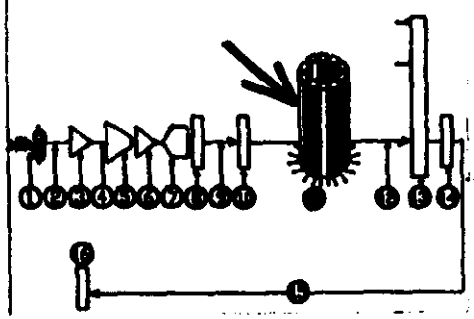
Programmable Digital Level-1 Trigger

3D-Flow boards assembly

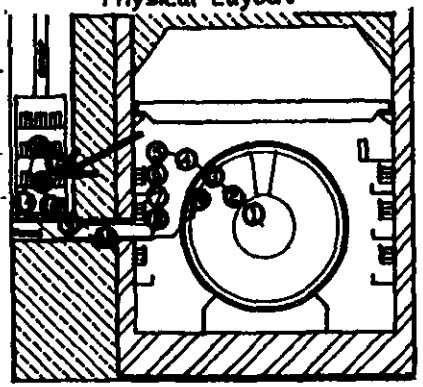
VBS No.: 50.04.1.2.6.1

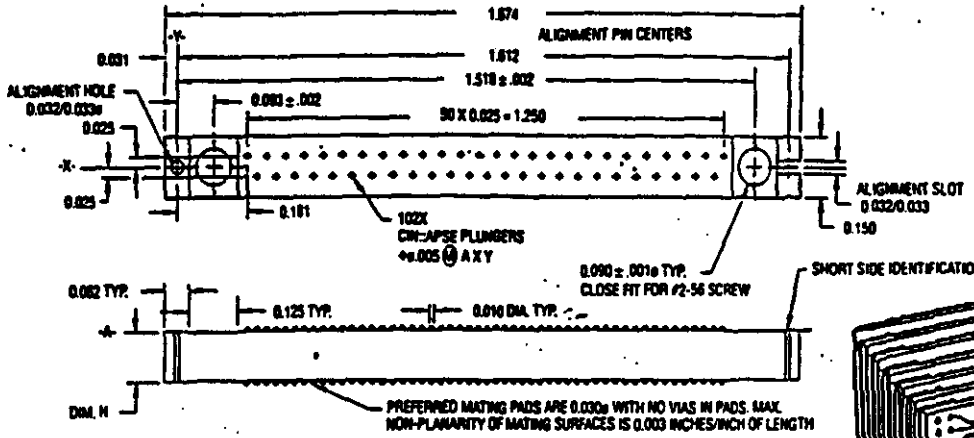
B. Crosetto - 19 Jan. 1993

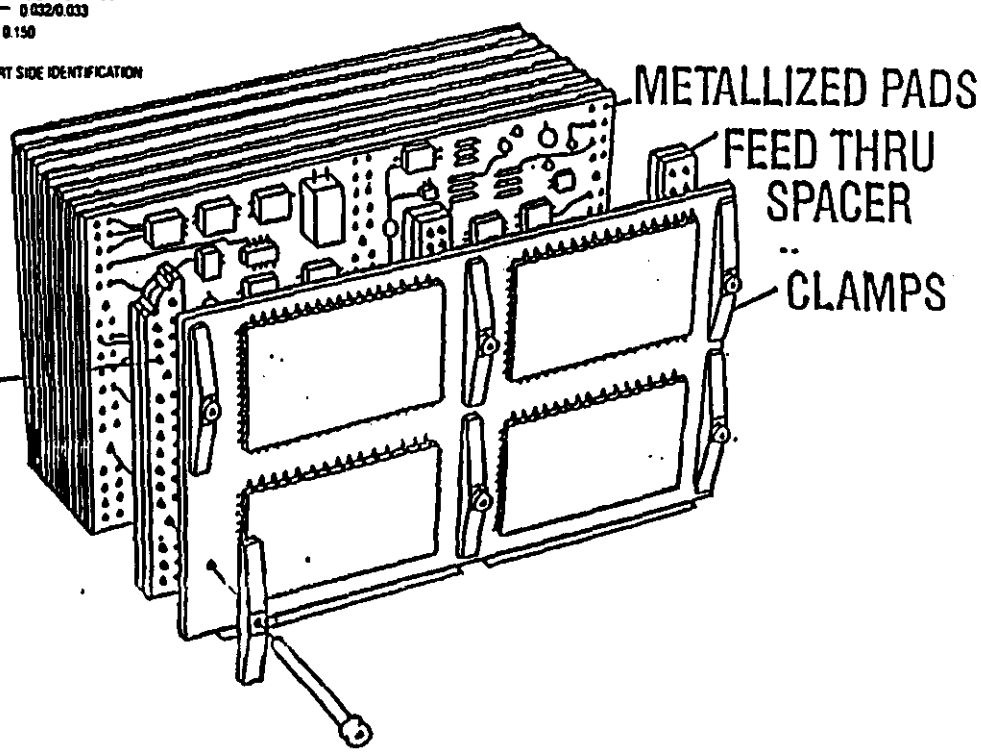
Logical Layout



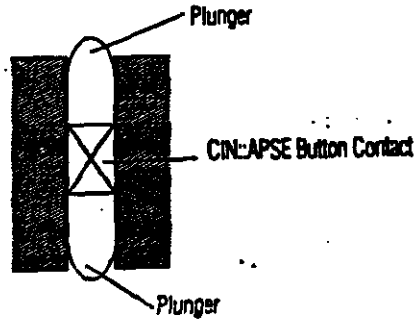
Physical Layout







Typical Cross-Section



SUBSYSTEM: Electronics
WBS No.: 50.04.1.3.7.3

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Rack slot

WBS QTY: 242

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	1.00%	5%
Cost	5	1.00%	5%
Schedule	8	2.00%	16%

Functional Activity:
Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
2-Material and services	BU	242.00					420		101,640	101,640

Notes: Place asterisk at the end of item descriptions if relational.
Notes: Based on the cost provided of $420/slot.

SUBTOTAL		**101,640**
DGA	**26%**	**26,426**
TOTAL		**128,066**

241

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.2.5.3

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Trigger sums , ADC, electrical to optical

WBS QTY: 5

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Engineer/Physicist-SSCL	BU	0.25	MY	SSC02	1,772	38.94		17,250	0	17,250
2-EDIA materials	BU	1.00					2,500		2,500	2,500
4-Proc/Fab materials	BU	1.00					7,000		7,000	7,000
6-Installation materials	BU	1.00					2,000		2,000	2,000
1-Senior Technician-SSCL	BU	0.30	MY	SSC04	1,772	24.83		13,200	0	13,200

242

Notes: Place asterisk at the end of item descriptions if relational.
Notes: Based on the cost of the DAC Motorola MC144111(4*6-bit DAC in 14 pin chip) cost of $5.70/chip, 6 chips/board used to control the offset of each analog input.
Based on the cost of the ADC from Analog Device (AD9012) or Sony cost $70/chip, 6 chips/board.
Based on the written quote from Antel: $500/transmitter.
Within 2-3 years the cost should be $100/transmitter.
The physical space on the board is estimated to be from 2 to 3 square inches/transmitter.

SUBTOTAL		41,950
DGA	46%	19,297
TOTAL		61,247

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.3.5.3

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Trigger sums , ADC, electrical to optical

WBS QTY: 250

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	1%	5%
Cost	1	1%	1%
Schedule	8	2%	16%

Functional Activity: *Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.*

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

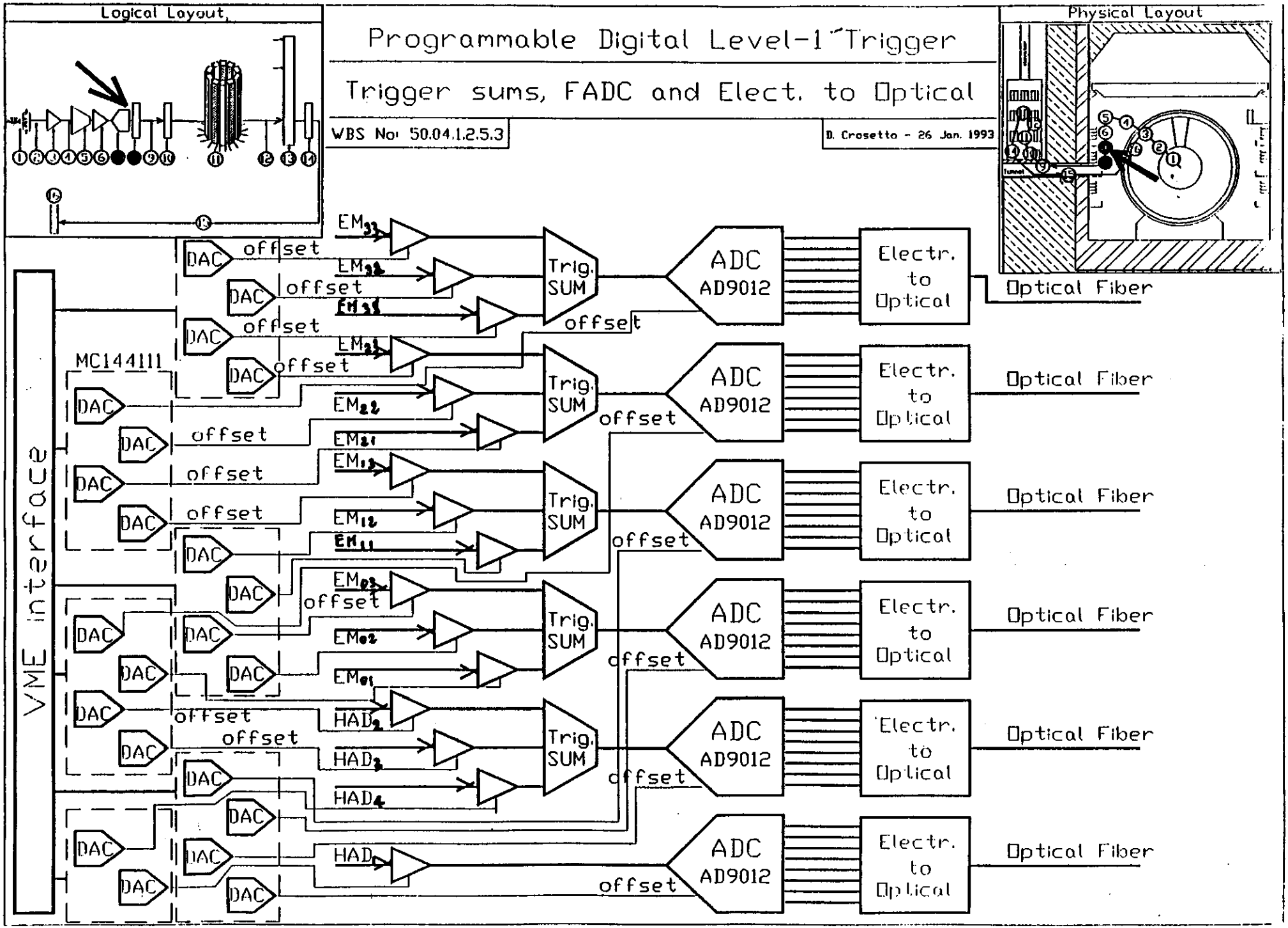
Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Engineer/Physicist-SSCL	BU	0.10	MY	SSC02	1,772	38.94		6,900	0	6,900
2-EDIA materials	BU	250.00					500		125,000	125,000
4-Proc/Fab materials	BU	250.00					2,000		500,000	500,000
6-Installation materials	BU	250.00					500		125,000	125,000
1-Senior Technician-SSCL	BU	0.30	MY	SSC04	1,772	24.83		13,200	0	13,200

Notes: Place asterisk at the end of item descriptions if relational.
Notes: Based on the cost of the DAC Motorola MC144111(4*6-bit DAC in 14 pin chip) cost of $2.70/chip, 6 chips/board used to control the offset of each analog input.
Based on the cost of the ADC from Analog Device (AD9012) or Sony cost $50/chip, 6 chips/board.
Based on the written quote from Antel: $500/transmitter.
Within 2-3 years the cost should be $100/transmitter.
The physical space on the board is estimated to be from 2 to 3 square inches/transmitter.

SUBTOTAL		770,100
DGA	22%	169,422
TOTAL		939,522

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:


Logical Layout
Physical Layout
Programmable Digital Level-1 Trigger
Trigger sums, FADC and Elect. to Optical
WBS No: 50.04.1.2.5.3
D. Crosetto - 26 Jan. 1993
VME interface
MC144111
DAC
offset
Trig. SUM
ADC AD9012
Electr. to Optical
Optical Fiber
EM31
EM32
EM33
EM21
EM22
EM23
EM11
EM12
EM13
EM01
EM02
EM03
HAD1
HAD2
HAD3
HAD4

SUBSYSTEM: Electronics
WBS No.: 50.04.1.2.5.6

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Energy sum board

WBS QTY: 5

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Engineer/Physicist-SSCL	BU	0.25	MY	SSC02	1,772	38.94		17,250	0	17,250
2-EDIA materials	BU	1.00					500		500	500
4-Proc/Fab materials	BU	1.00					2,000		2,000	2,000
6-Installation materials	BU	1.00					500		500	500
1-Senior Technician-SSCL	BU	0.25	MY	SSC04	1,772	24.83		11,000	0	11,000

Notes: Place asterisk at the end of item descriptions if relational.

SUBTOTAL		31,250
DGA	46%	14,375
TOTAL		45,625

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.3.5.6

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Energy sum board

WBS QTY: 20

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

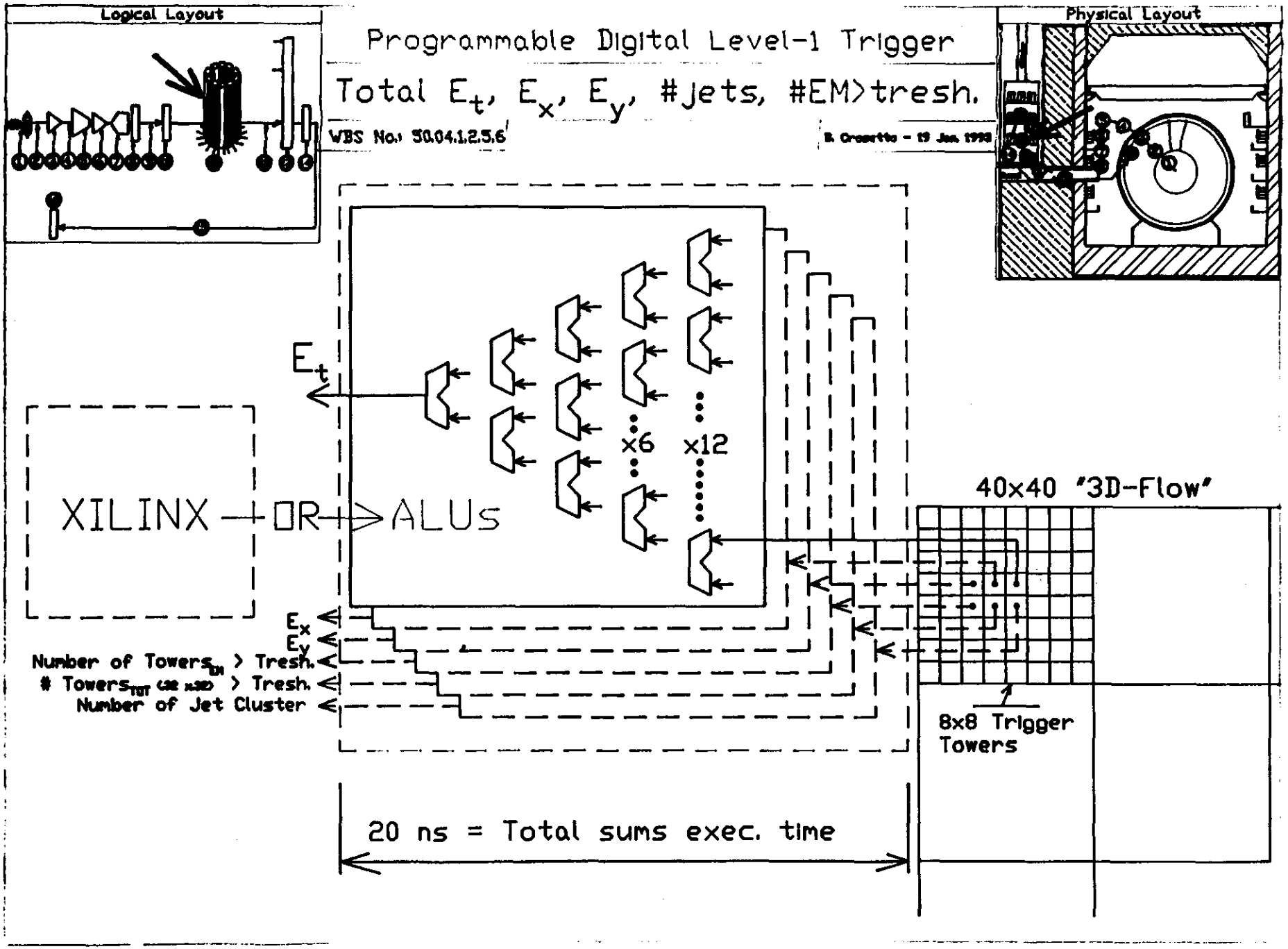
Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
4-Proc/Fab materials	BU	20.00					1,500		30,000	30,000
6-Installation materials	BU	20.00					150		3,000	3,000

Notes: Place asterisk at the end of item descriptions if relational.

SUBTOTAL		**33,000**
DGA	**46%**	**15,180**
TOTAL		**48,180**

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:


Logical Layout
Programmable Digital Level-1 Trigger
Total E_t, E_x, E_y, #jets, #EM>tresh.
WBS No.: 30.04.1.2.5.6
Physical Layout
E_t
x6
x12
XILINX
OR
ALUs
40x40 "3D-Flow"
E_x
E_y
Number of Towers$_{EM}$ > Tresh.
Towers$_{TOT}$ (2E x3D) > Tresh.
Number of Jet Cluster
8x8 Trigger Towers
20 ns = Total sums exec. time

SUBSYSTEM: Electronics
WBS No.: 50.04.1.2.6

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: On-detector crate complete

WBS QTY: _____

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Engineer/Physicist-SSCL	BU	0.15	MY	SSC02	1,772	38.94		10,350	0	10,350
2-EDIA material	BU	1.00					4,000		4,000	4,000
2-Boards and crate	BU	1.00					20,000		20,000	20,000
6-Installation materials	BU	1.00					2,000		2,000	2,000
1-Senior Tecnhnician-SSCL	BU	0.15	MY	SSC04	1,772	24.83		6,600	0	6,600

Notes: Place asterisk at the end of item descriptions if relational.
Notes: Based on the cost of VME crate with a MC68K CPU, memory board, and serial I/O boards to control the 3D-Flow processor array.

SUBTOTAL		42,950
DGA	46%	19,757
TOTAL		62,707

2488

Estimated By: Dario Crosetto

Date Estimated: 1/19/93

Sheet:

SUBSYSTEM: Electronics
WBS No.: 50.04.1.3.6

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: On-detector crate complete

WBS QTY: _____

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	4%	20%
Cost	10	1%	10%
Schedule	8	2%	16%

Functional Activity:
Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

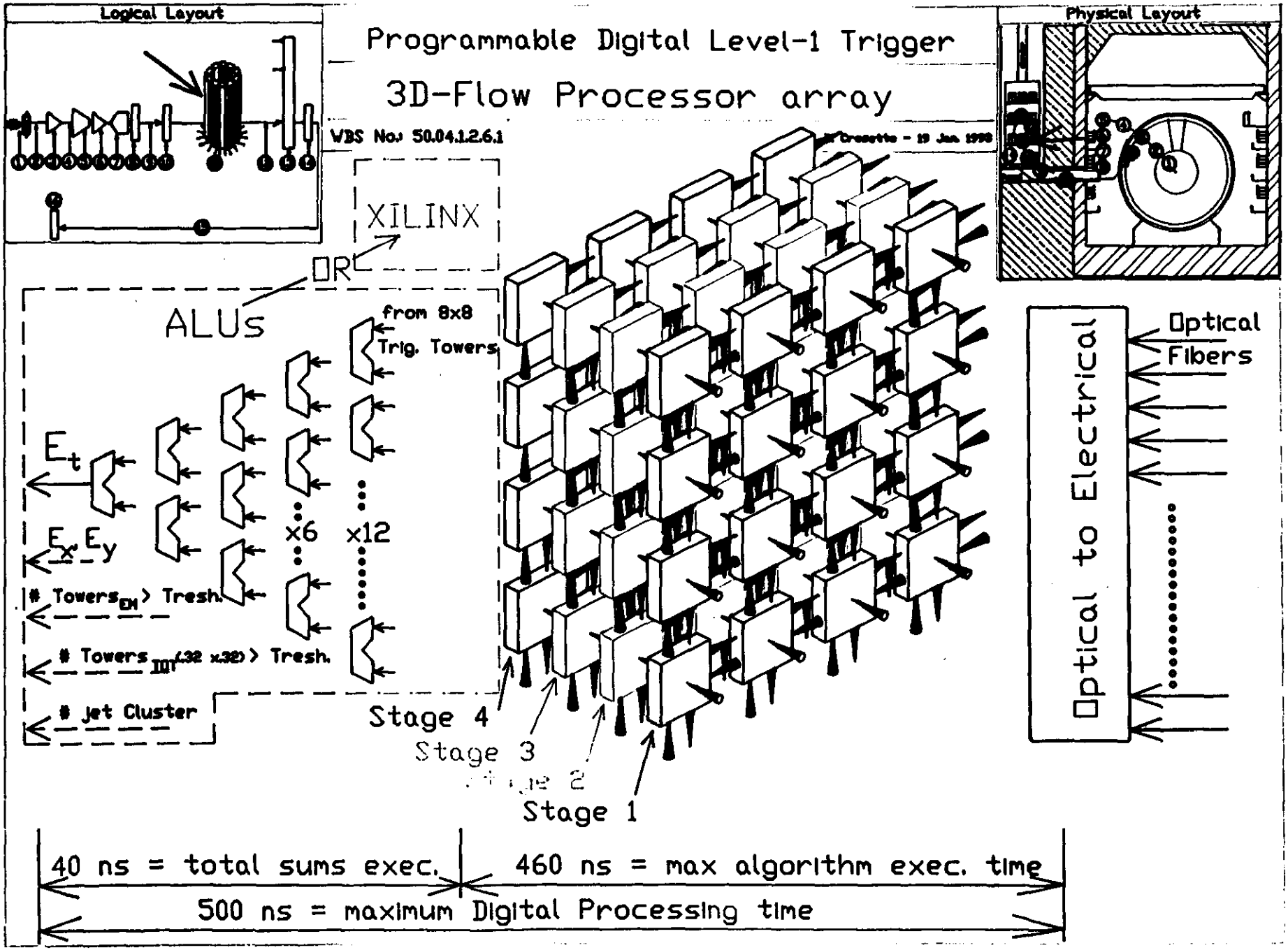
Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

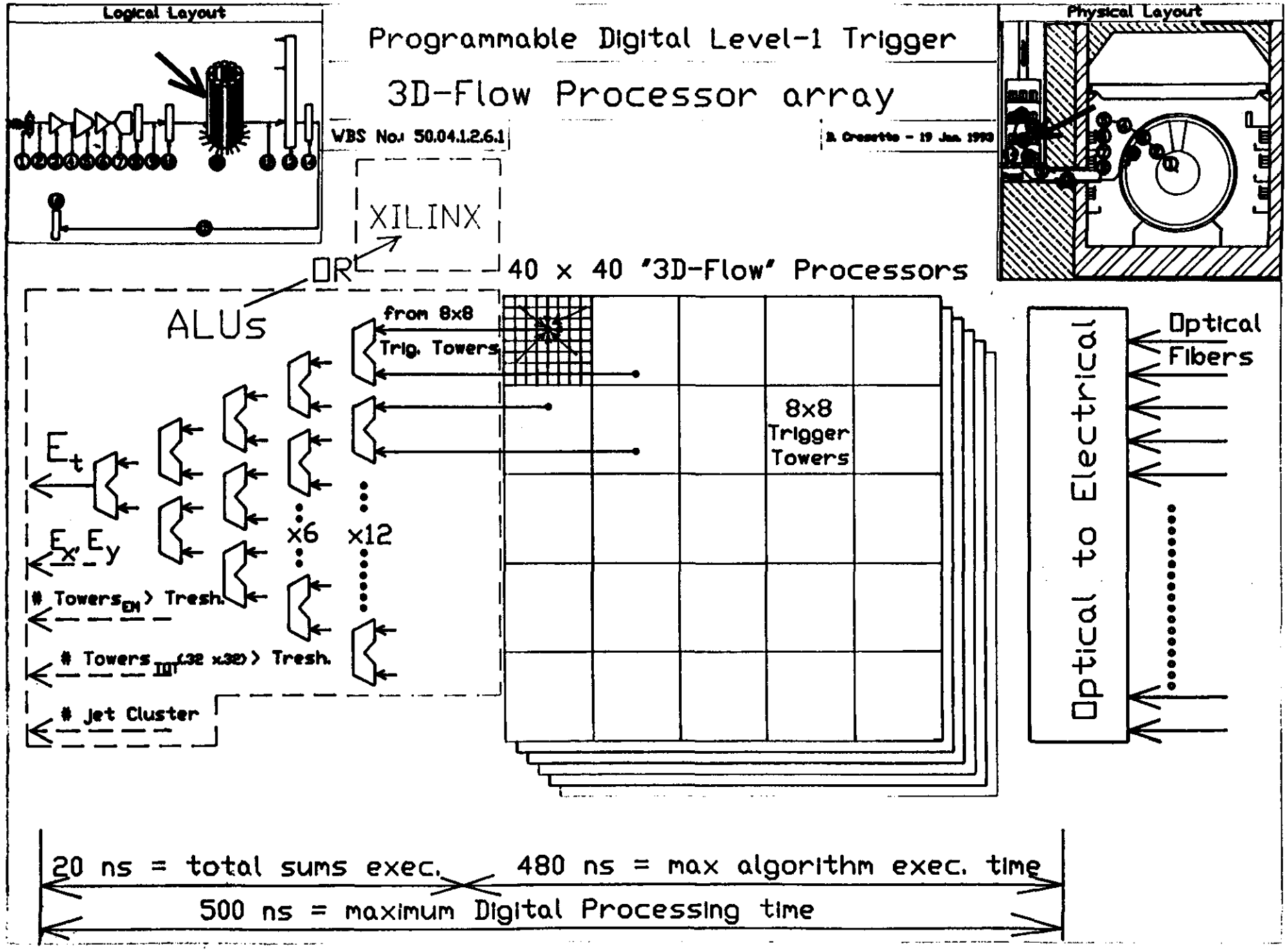
Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
1-Engineer/Physicist-SSCL	BU	0.10	MY	SSC02	1,772	38.94		6,900	0	6,900
2-EDIA material	BU	1.00					4,500		4,500	4,500
2-Boards and crate	BU	1.00					25,000		25,000	25,000
6-Installation materials	BU	1.00					2,000		2,000	2,000
1-Senior Tecnhnician-SSCL	BU	0.15	MY	SSC04	1,772	24.83		6,600	0	6,600

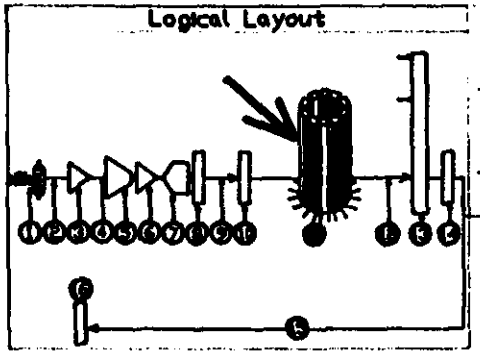
Notes: Place asterisk at the end of item descriptions if relational.
Notes: Based on the cost of additional VME memory and serial I/O boards, and the 3D-Flow cylinder rack.

SUBTOTAL		**45,000**
DGA	**46%**	**20,700**
TOTAL		**65,700**

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:


Logical Layout
Physical Layout
Programmable Digital Level-1 Trigger
3D-Flow Processor array
WBS No: 50.04.1.2.6.1
XILINX
OR
ALUs
from 8x8
Trig. Towers
E_t
E_x, E_y
x6
x12
Towers$_{EM}$ > Tresh.
Towers$_{HAD}$ (32 x32) > Tresh.
Jet Cluster
Stage 4
Stage 3
Stage 2
Stage 1
Optical to Electrical
Optical Fibers
40 ns = total sums exec.
460 ns = max algorithm exec. time
500 ns = maximum Digital Processing time


Logical Layout
Physical Layout
Programmable Digital Level-1 Trigger
3D-Flow Processor array
WBS No: 50.04.1.2.6.1
XILINX
OR
40 x 40 "3D-Flow" Processors
ALUs
from 8x8
Trig. Towers
8x8
Trigger
Towers
Optical
Fibers
Optical to Electrical
E_t
E_x E_y
x6
x12
Towers$_{EM}$ > Tresh.
Towers$_{HAD}$ (32 x32) > Tresh.
Jet Cluster
20 ns = total sums exec.
480 ns = max algorithm exec. time
500 ns = maximum Digital Processing time

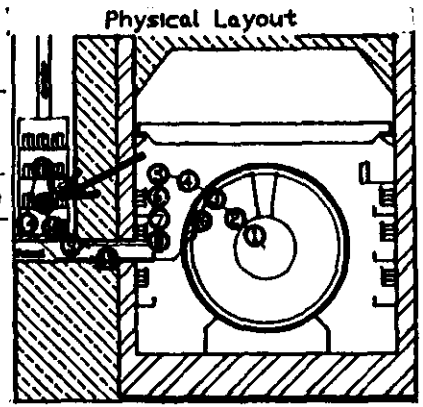


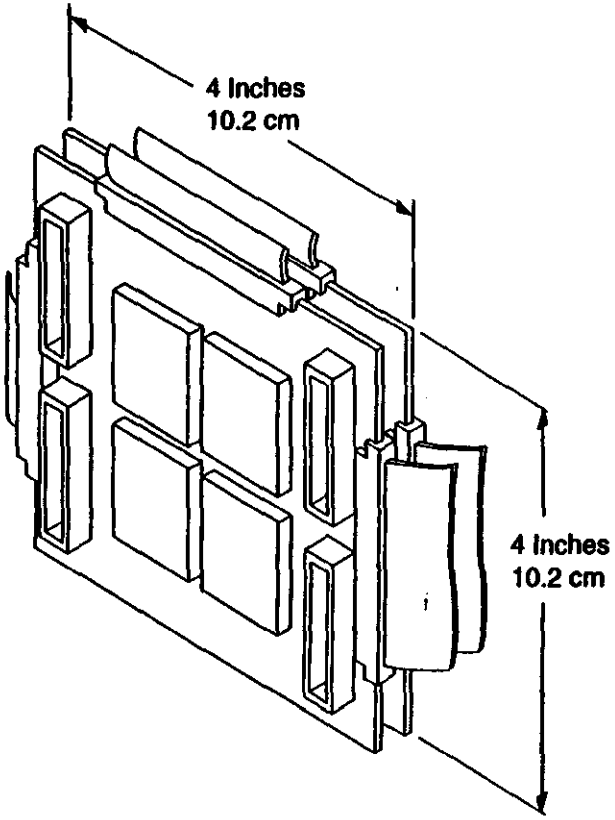
Programmable Digital Level-1 Trigger

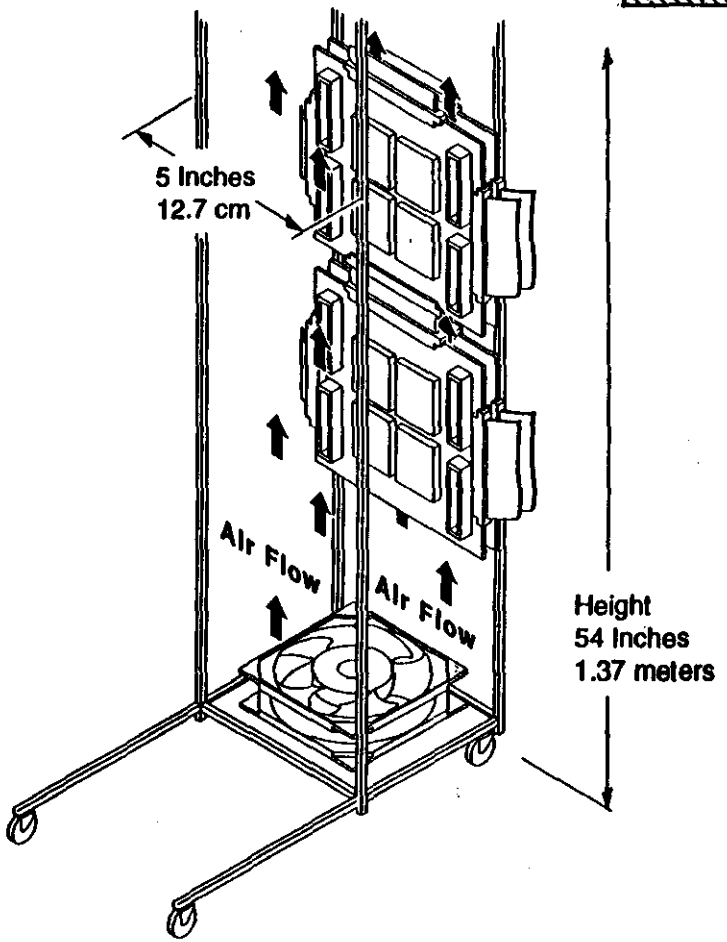
3D-Flow crate details

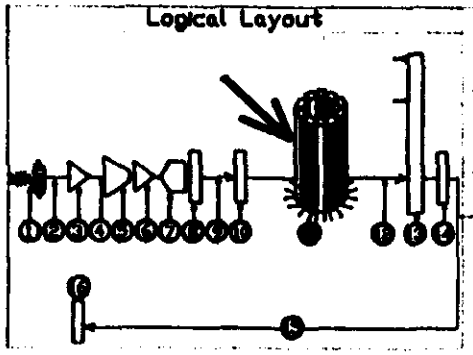
WBS No: 50.04.1.2.6.1

R. Crosetto - 19 Jun 1992







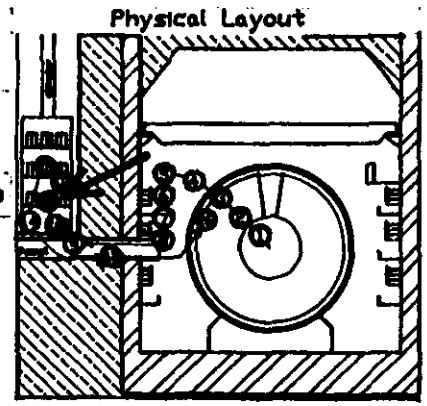


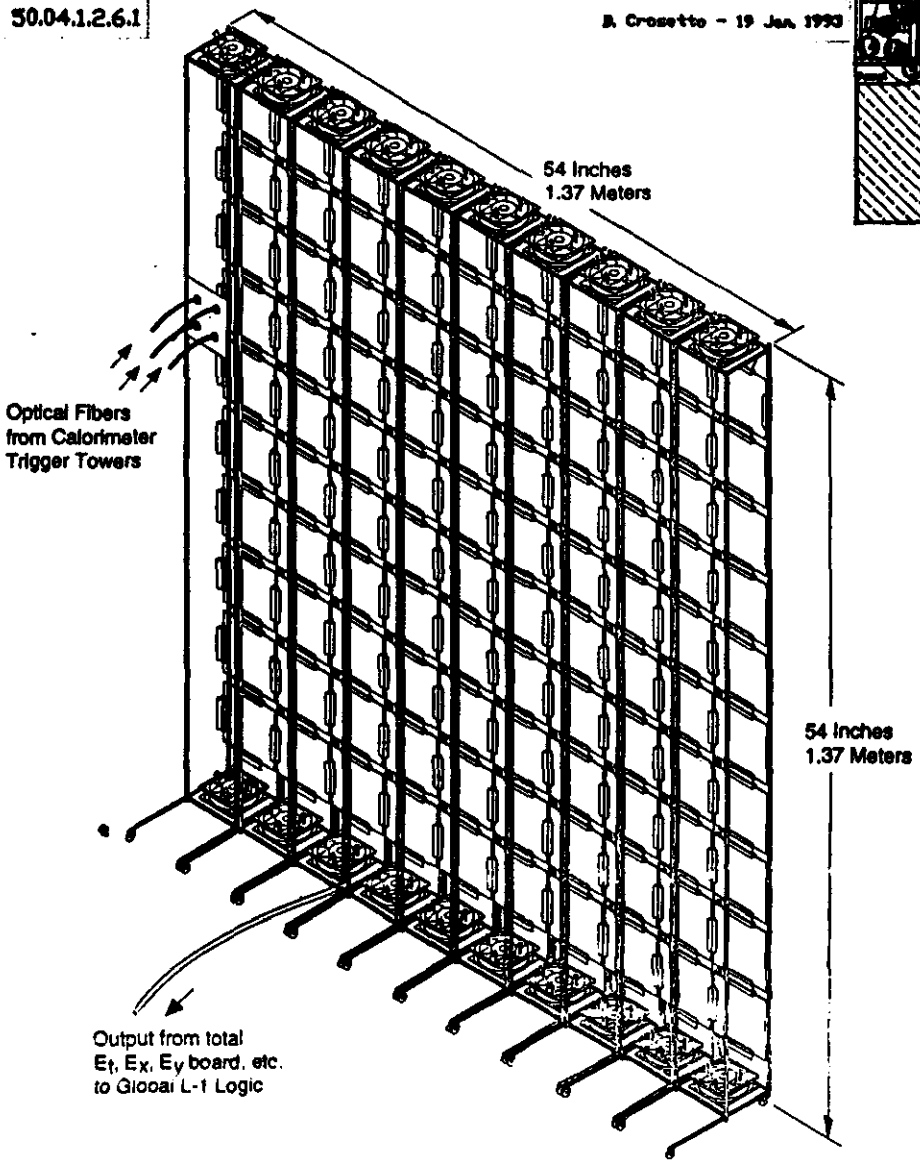
Programmable Digital Level-1 Trigger

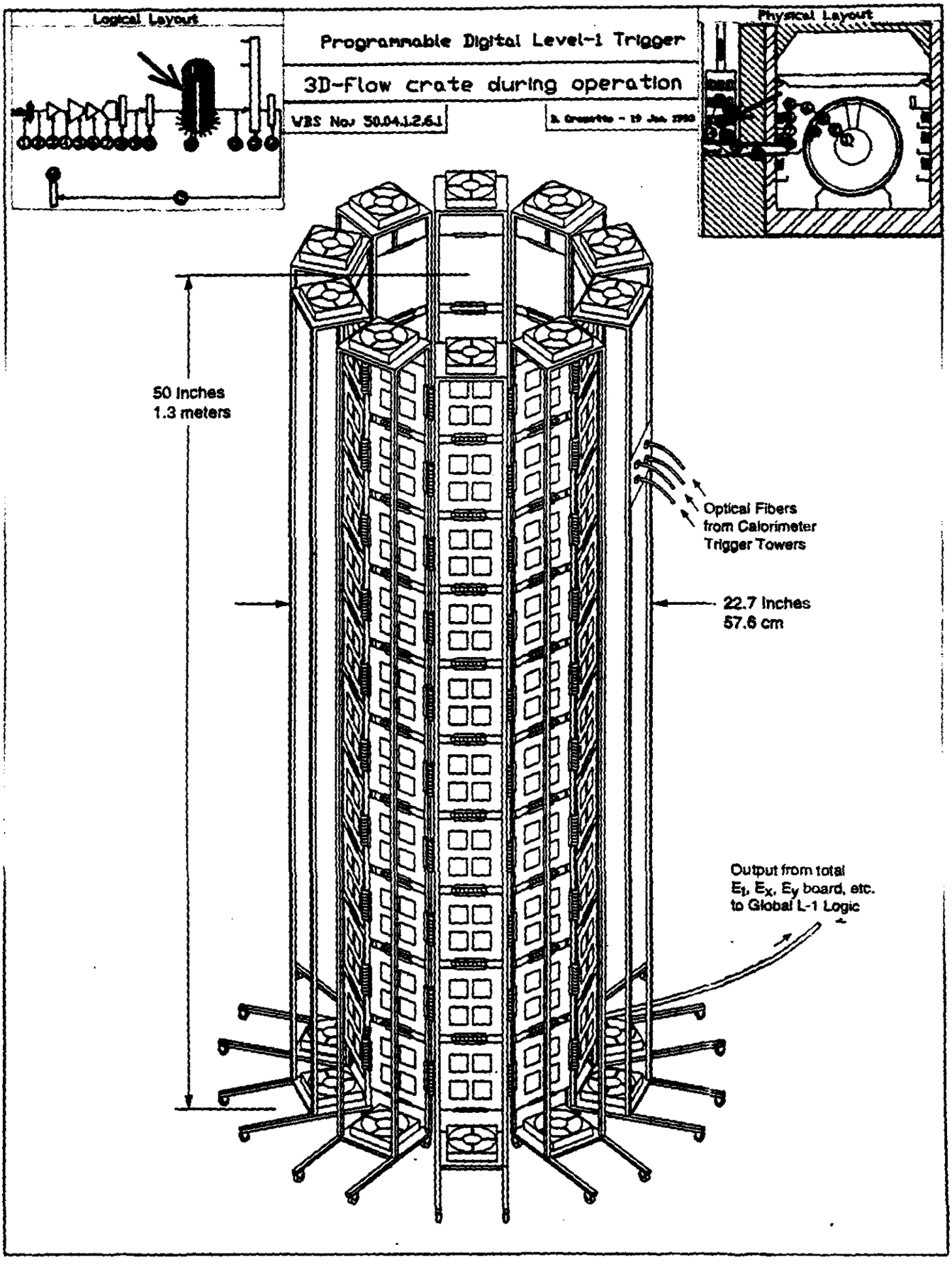
3D-Flow crate during assembly

WBS No.: 50.04.1.2.6.1

B. Crosetto - 19 Jan. 1999






Logical Layout
Programmable Digital Level-1 Trigger
3D-Flow crate during operation
WBS No: 50.04.1.2.6.1
Physical Layout
50 Inches
1.3 meters
Optical Fibers
from Calorimeter
Trigger Towers
22.7 Inches
57.6 cm
Output from total
E_t, E_x, E_y board, etc.
to Global L-1 Logic

SUBSYSTEM: Electronics
WBS No.: 50.04.1.4

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS Descript.: Installation & test

WBS QTY: _____

WBS UM: MY

	RISK		DGA
	Factors	Percentage	
Technical	5	1%	5%
Cost	5	1%	5%
Schedule	8	2%	16%

Functional Activity:
1 Engineering/Design
2 Material & Services
3 Inspection/Administration
4 Procurement/Fabrication
5 Assembly
6 Installation

Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

Cost Basis:
1. Bottom-Up (BU)
2. Specific Analogy (SA)
3. Parametric Study (PS)
4. Review and Update (RU)
5. Trend Analysis (TA)
6. Expert Opinion (EO)

Item Description	COST BASIS	Qty	Unit Meas (UM)	Craft/Team Resourse Code	* Unit Productivity MH/UM	Craft/ Team Rate/HR	Mat'l Unit Cost	Total Labor	Total Mat'l	Total Direct
6-Installation	BU	1.00					50,000		50,000	50,000

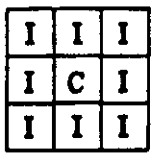
Notes: Place asterisk at the end of item descriptions if relational.

SUBTOTAL		50,000
DGA	26%	13,000
TOTAL		63,000

Estimated By: Dario Crosetto Date Estimated: 1/19/93 Sheet:

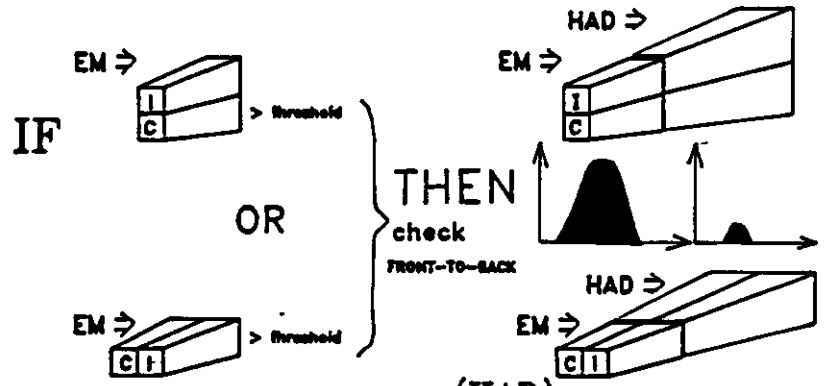
Algorithm example

Local maximum



$C > I_i$ for $i = 1, \ldots, 8$.

Threshold $< \sum_{i=1}^{8} I_i + C$.



Threshold $< C_{em} + I_{em}$; $\frac{(HAD)}{(EM)} <$ Threshold

15 steps

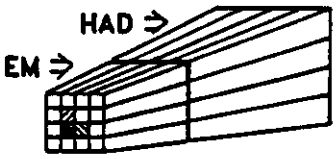
Any algorithm type and length

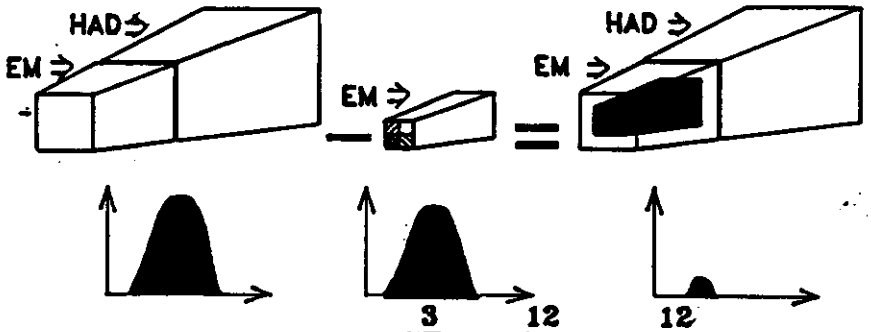
31 steps

THEN

Check for ISOLATION

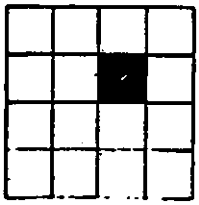
4 x 4 simplified trigger tower





Threshold $< C_H + \sum_{i=1}^{3} I_{H_i} + \sum_{i=1}^{12} O_{H_i} + \sum_{i=1}^{12} O_{EM_i}$

Jet finding



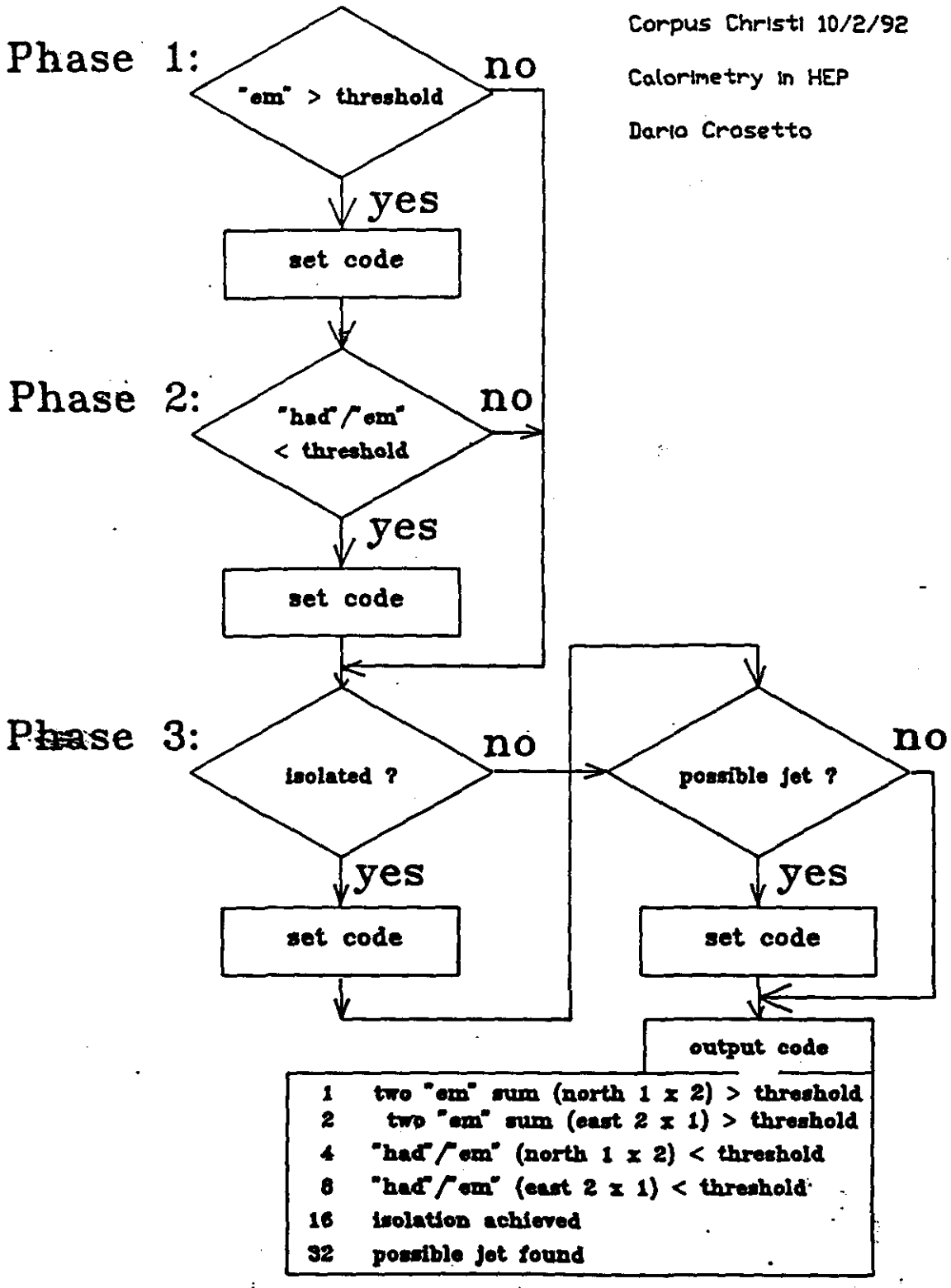
Threshold $< \sum_{i=1}^{16} E_{EM_i} + \sum_{i=1}^{16} E_{H_i}$

Algorithm flow-chart

Corpus Christi 10/2/92

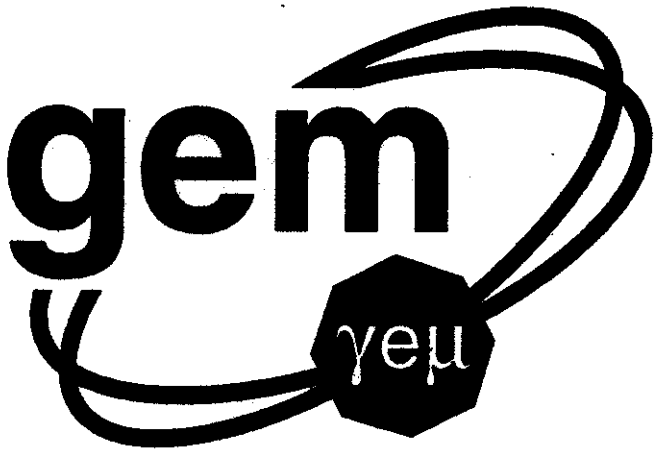
Calorimetry in HEP

Dario Crosetto



e.g. A "FEP" may return a code = 37 (1+4+32) stating:

- a possible electron was found,
- but it was not isolated from the sorrounding energy,
- and that cell may be part of a 4 x 4 jet.



Presentation by:

M. Atiya

GEM Muon Trigger

Purpose & Means:

- Identify "true" muons according to their P_t.
  - P_t range : 10-50 GeV/c
  - η range : -2.5 to 2.5 Units

  This is attained by purely geometrical means:
  Sagitta of a 10 GeV/c muon is 7.5 cm.
  Multiple scattering and non-uniform field are a potential complication.

- Identify the beam crossing responsible for the generated trigger.

  This is attained by using the short drift time of the Cathode Strip Chamber anode wire.

Objectives:

- Form the trigger in about 500 nsec.
- Reduce the number of connections.
- Allow programmability for P_t selection.
- Assist the DAQ in readout in order to reduce rate.

Trigger Numerology

Barrel

Superlayers	3		
Super Sectors	12		
Sectors	48		
Gaps/Superlayer	6	6	6
η Segments/Superlayer	4	8	8
Cathode Size (mm)	5.84	8.33	10.7
No Cathodes in trigger segment	2	2	2
No Channels/readout card	672	672	672
No trigger elements/readout card	336	336	336

EndCap

Superlayers	3		
Super Sectors	12		
Sectors	24	48	48
Gaps/Superlayer	8	6	6
η Segments/Superlayer	2x3	2x3	2x3
Cathode Size (mm) (radial)	5	5	5
No Cathodes in trigger segment	1	1	1

Associative Memory Scheme

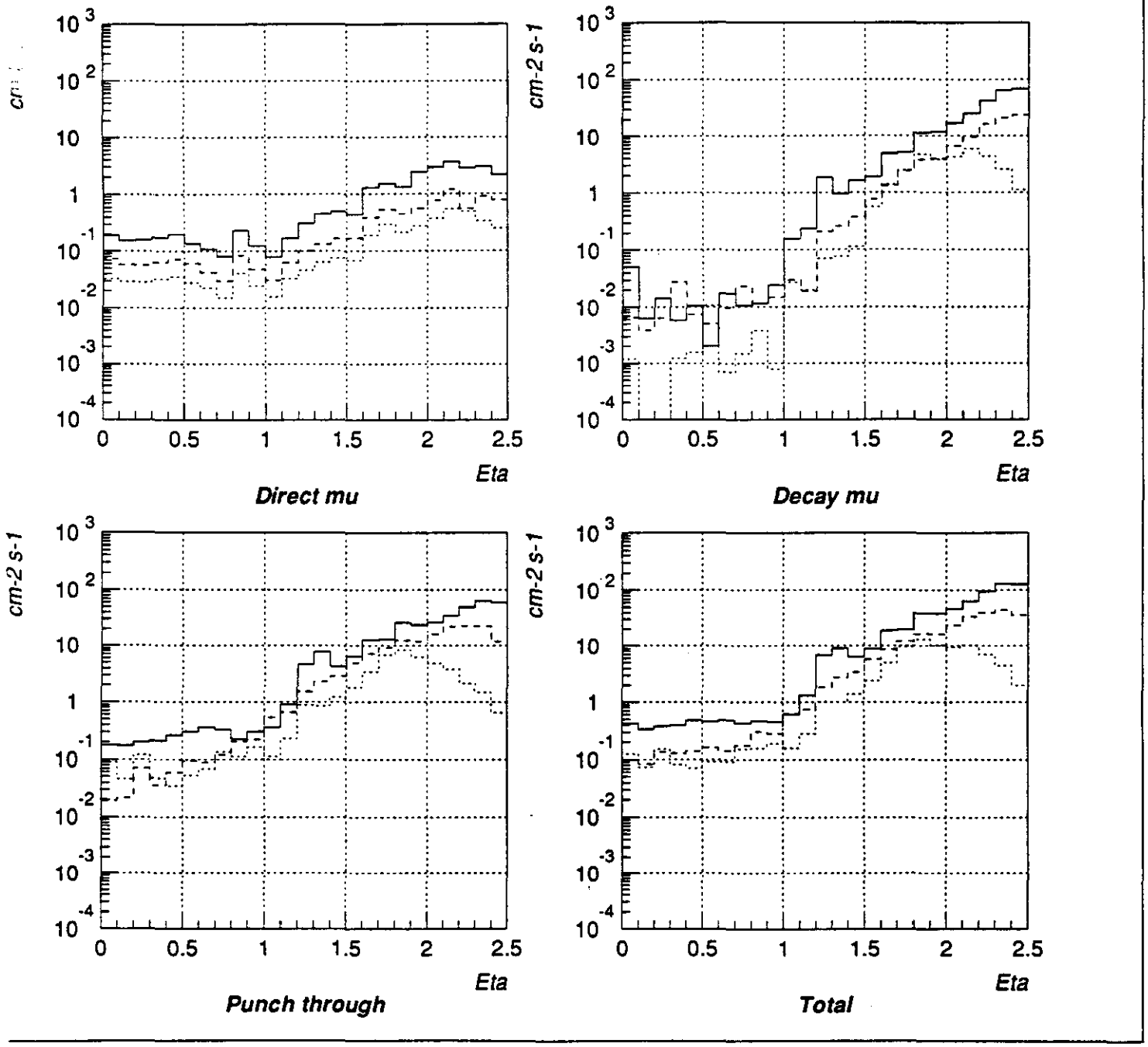
(Amendolia et. al., Dell'Orso et. al.)

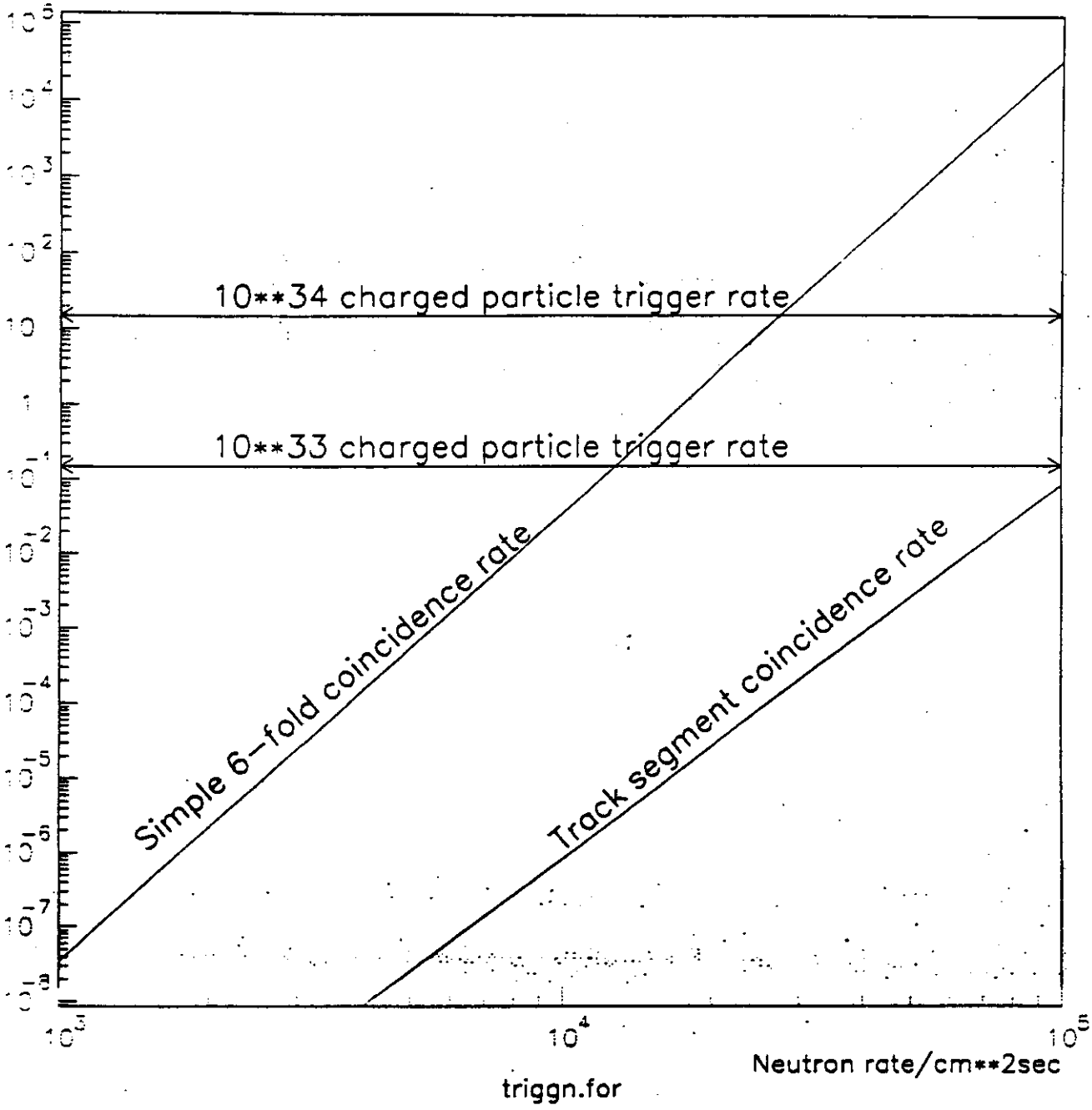
A content-addressable memory to recognize the appropriate trigger geometry patterns.

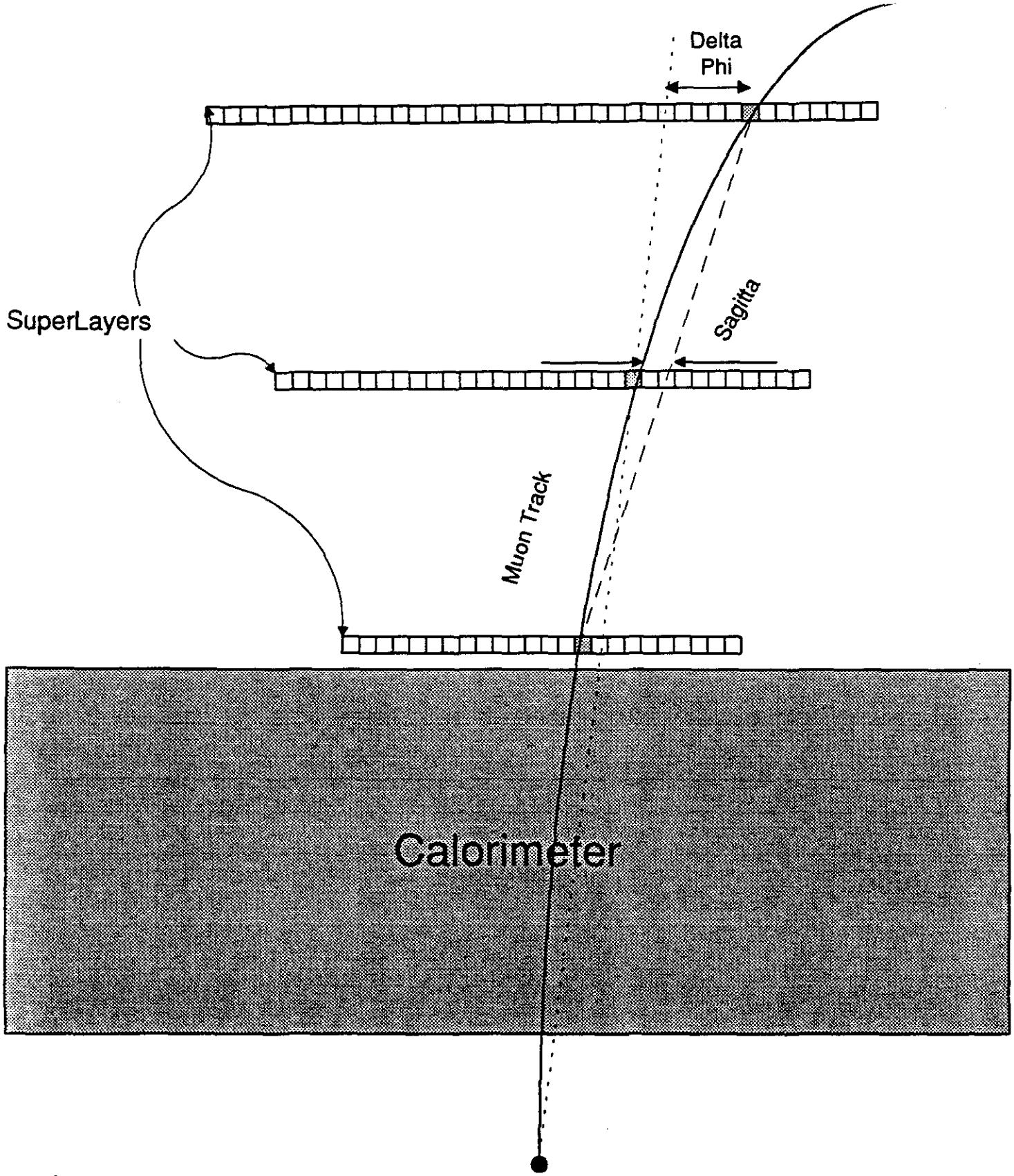
Pro	Con
Few Interconnects (encoded addressing)	Not "classically" pipe-lined
Programmable	Initial development necessary
Flexible	
Requires few services	

Number of patterns for baseline II

Minimum momentum Cut (GeV/c)	Number Patterns
10	1618
20	1090
30	793
40	610
50	503
60	448

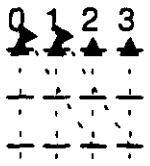

cm-2 s-1
Eta
Direct mu
Decay mu
Punch through
Total


10**34 charged particle trigger rate
10**33 charged particle trigger rate
Simple 6-fold coincidence rate
Track segment coincidence rate
Neutron rate/cm**2sec
triggn.for

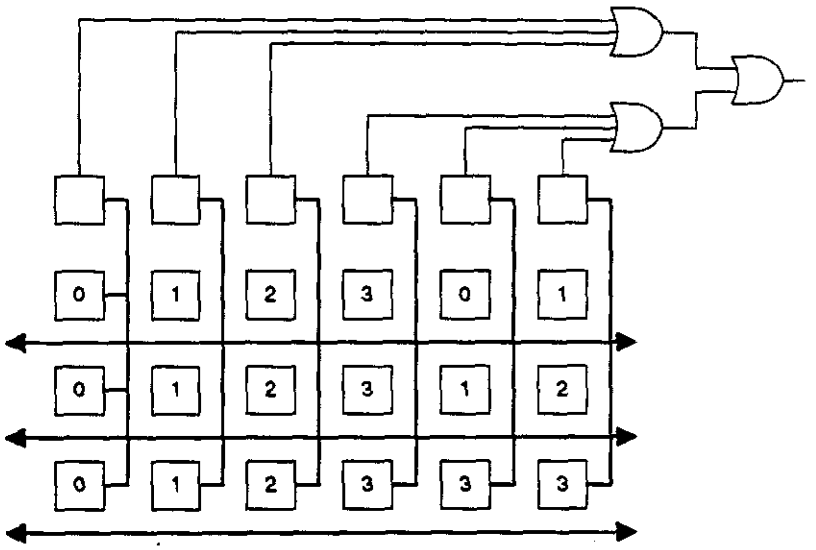


Delta Phi and Sagitta methods for level 1 trigger

Consider a situation with 6 allowable patterns

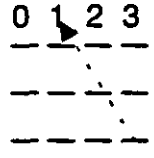


"Three out of Three" logic

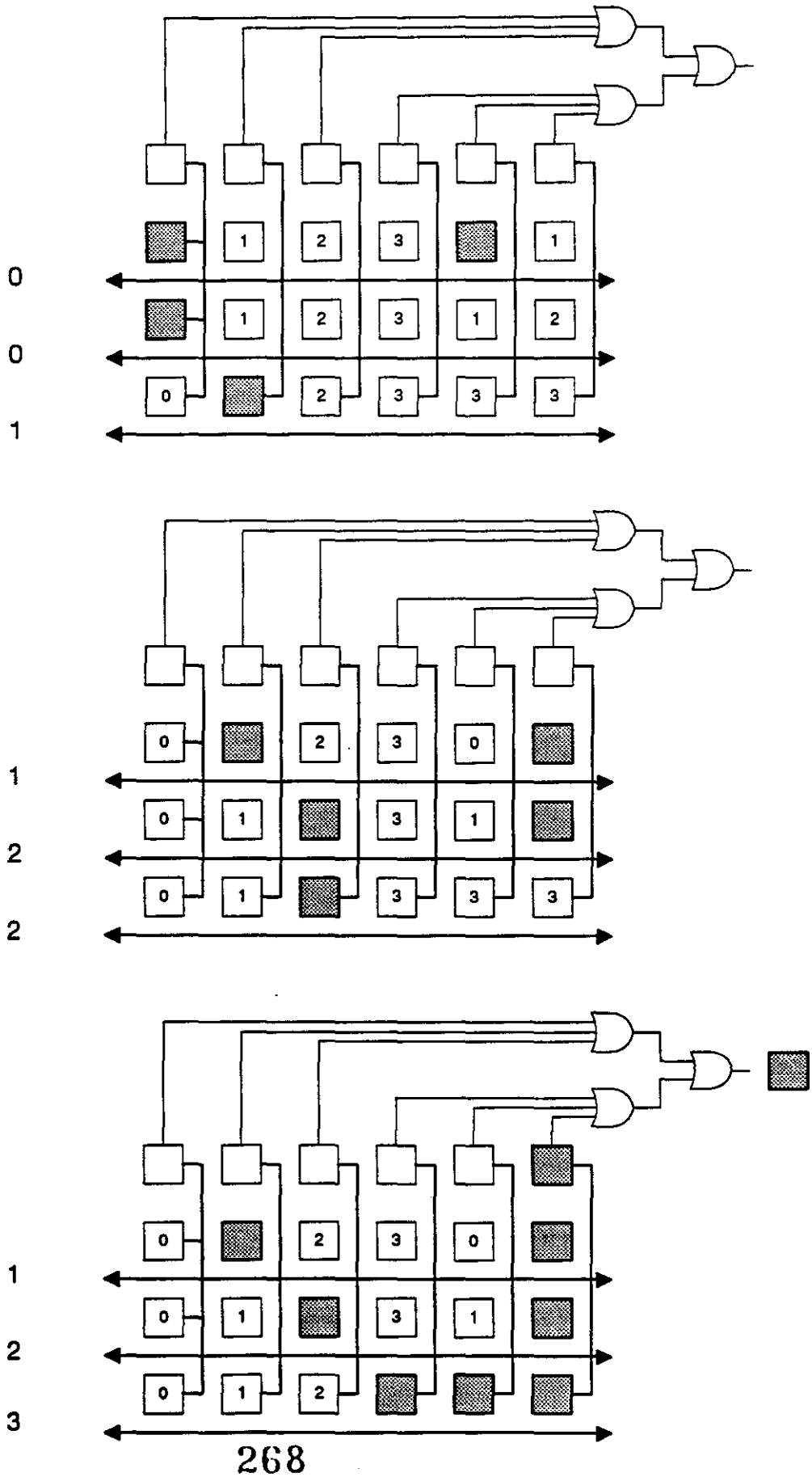


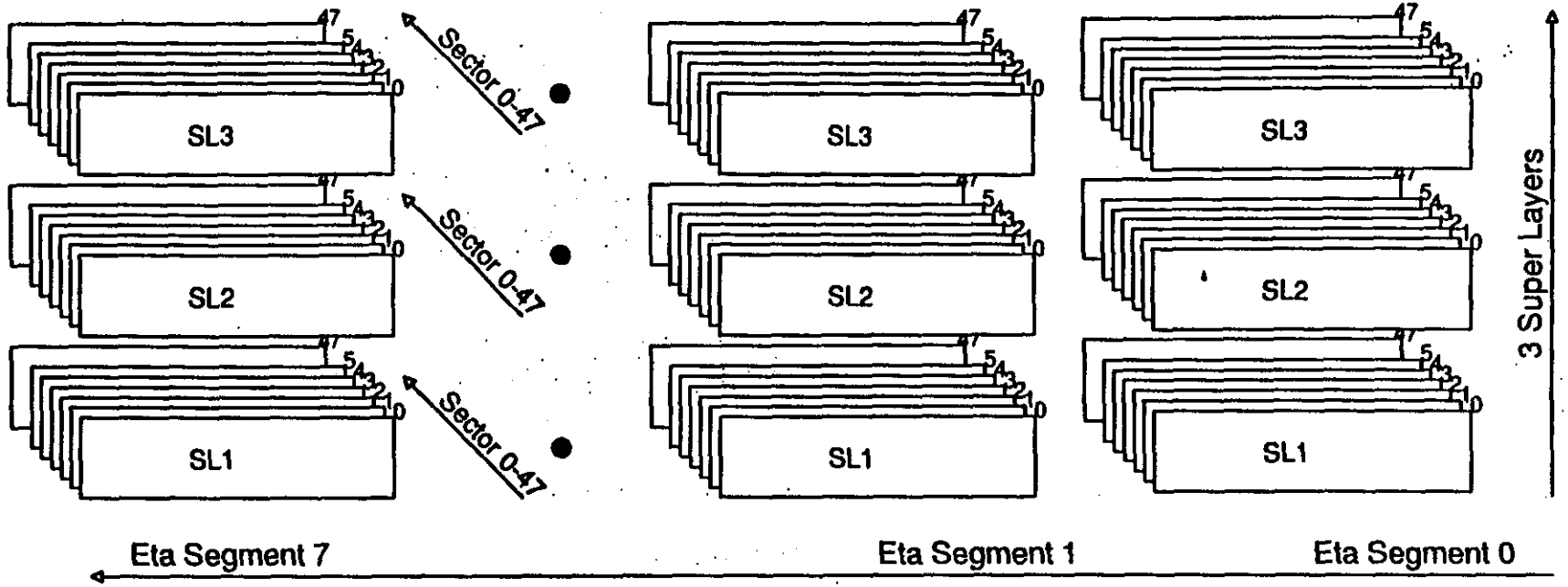
Data Buses

For Example:
A track with some extra hits

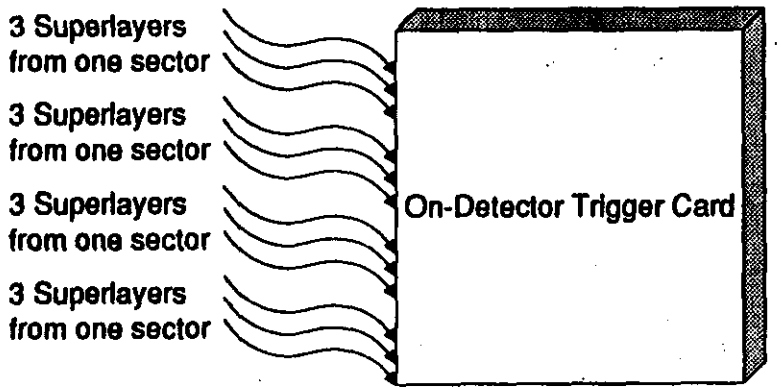


Hits
0,1
0,2
1,2,3


0
0
1
1
2
2
1
2
2
3



1152 Cables =
96 Cards x 12 Cables =
48 sectors x 3 SuperLayers x 8 Eta Segments



One Card per Super Sector

12 Super Sectors x 8 Eta Segments = 96 Cards

BROOKHAVEN NATIONAL LABORATORY	
Project: GEM-Muon-Level 1 Trigger	
Date: 2/9/93	**Drawn By:** M. Atiya

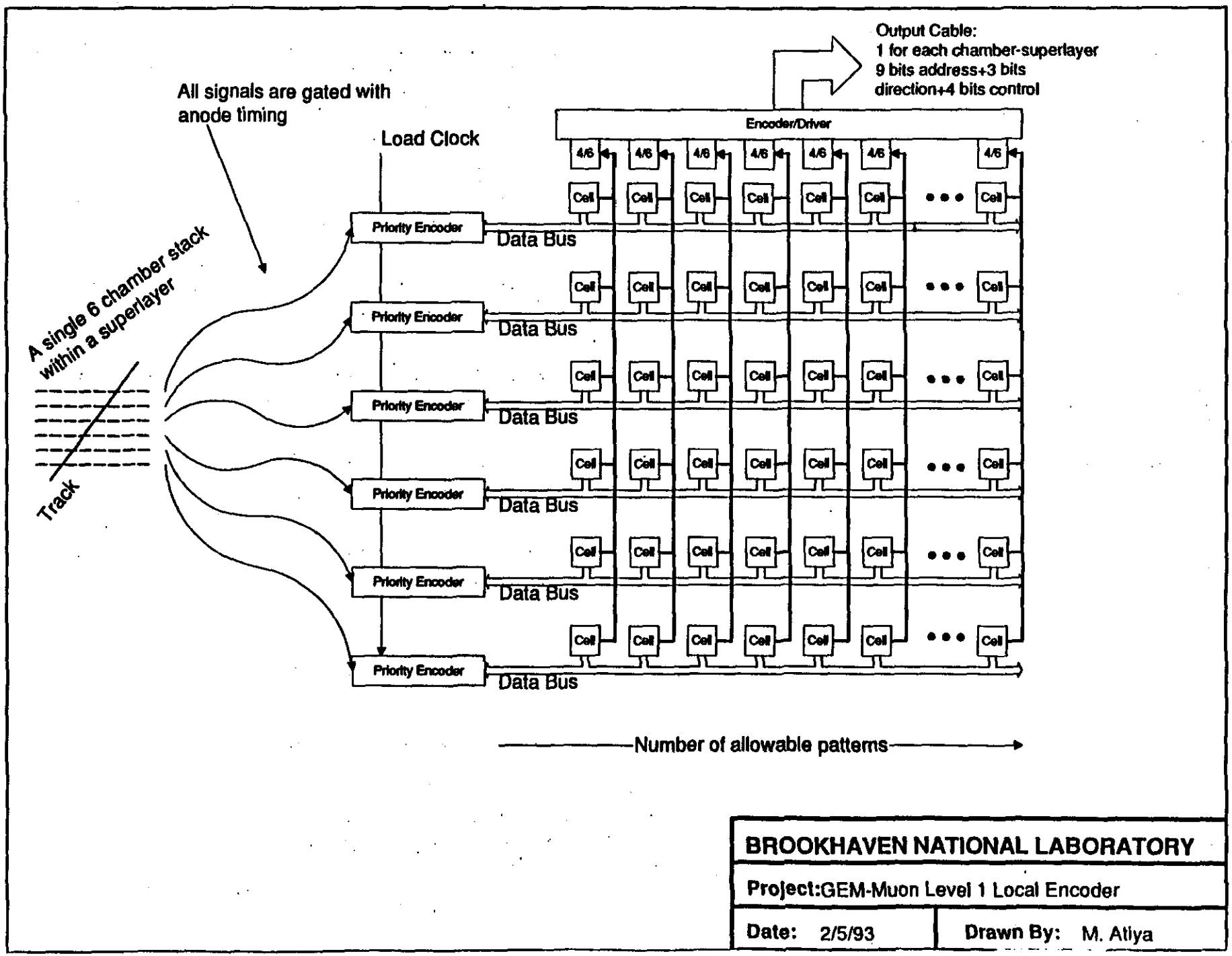
Structure (Barrel) of Muon Level 1 Trigger Hardware

BROOKHAVEN NATIONAL LABORATORY

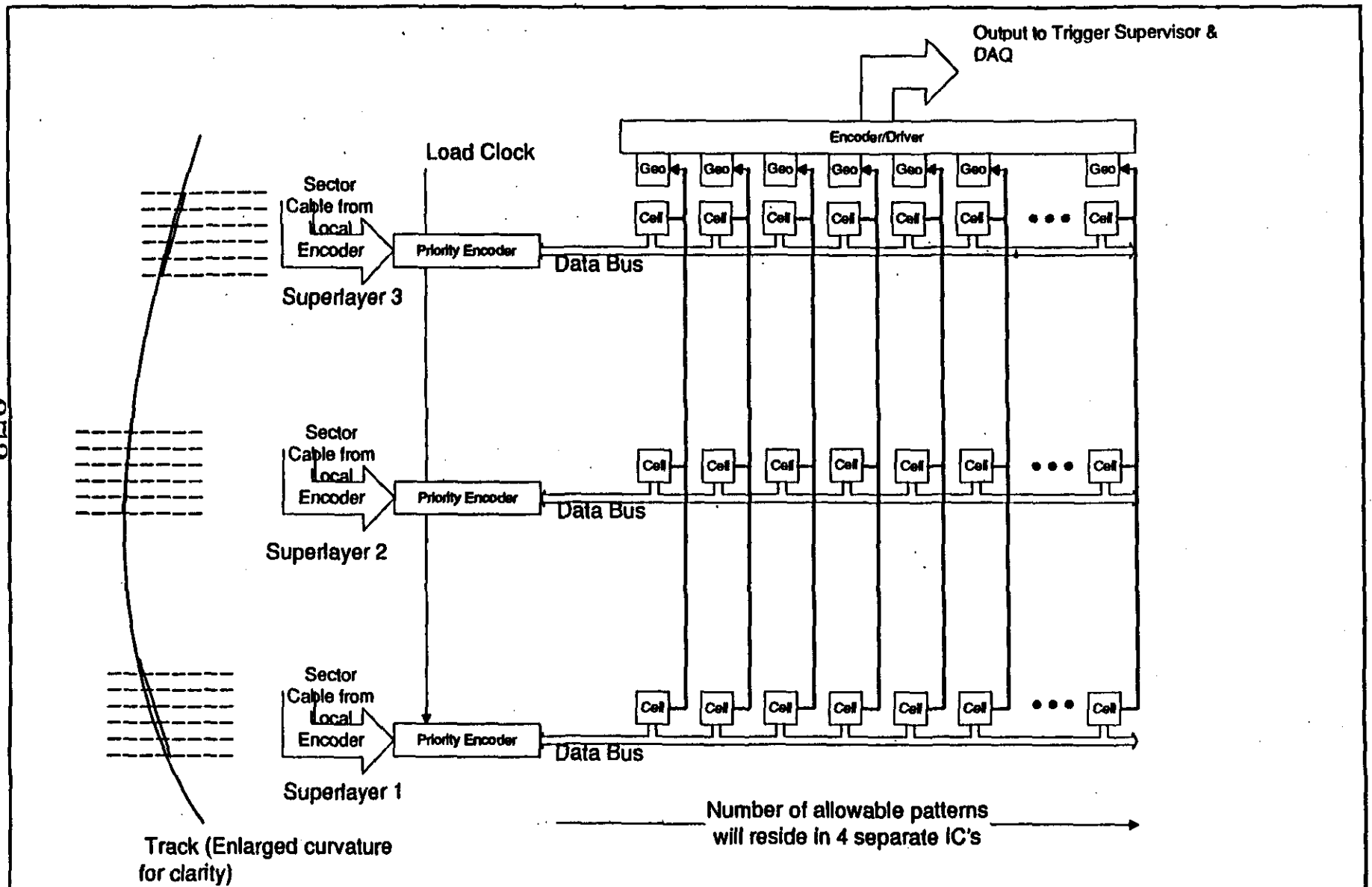
Project: GEM-Muon-Level 1 Trigger

Date: 2/9/93 **Drawn By:** M. Atiya

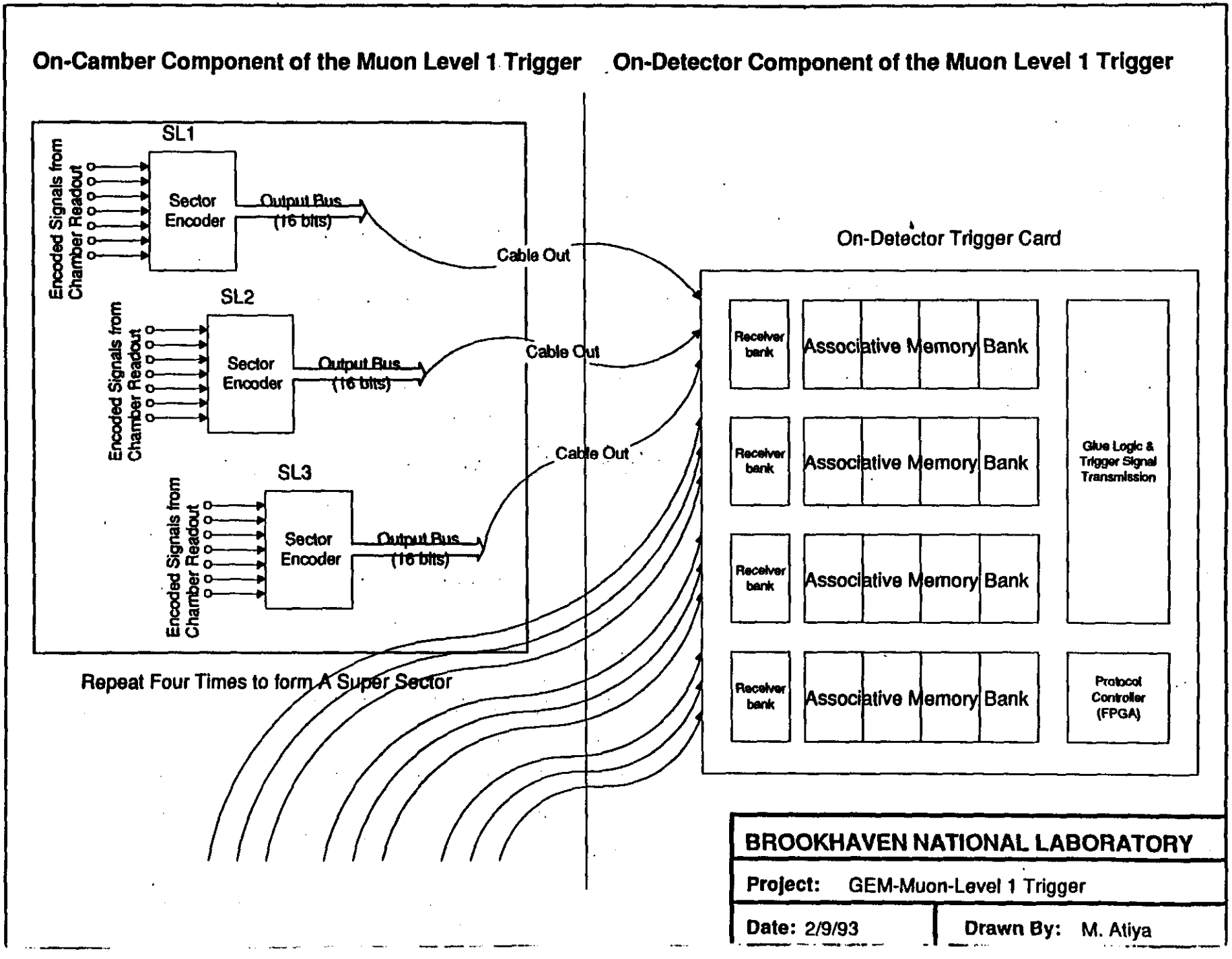
Structure (Endcap) of Muon Level 1 Trigger Hardware

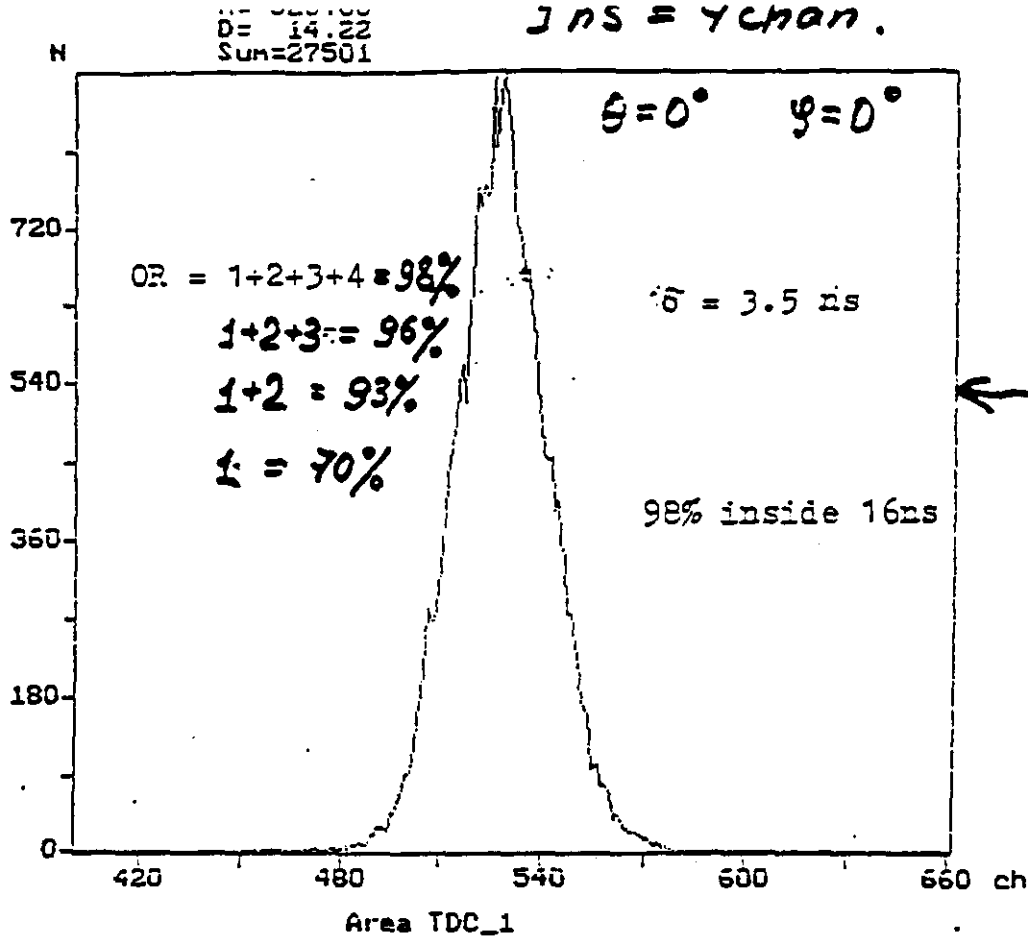


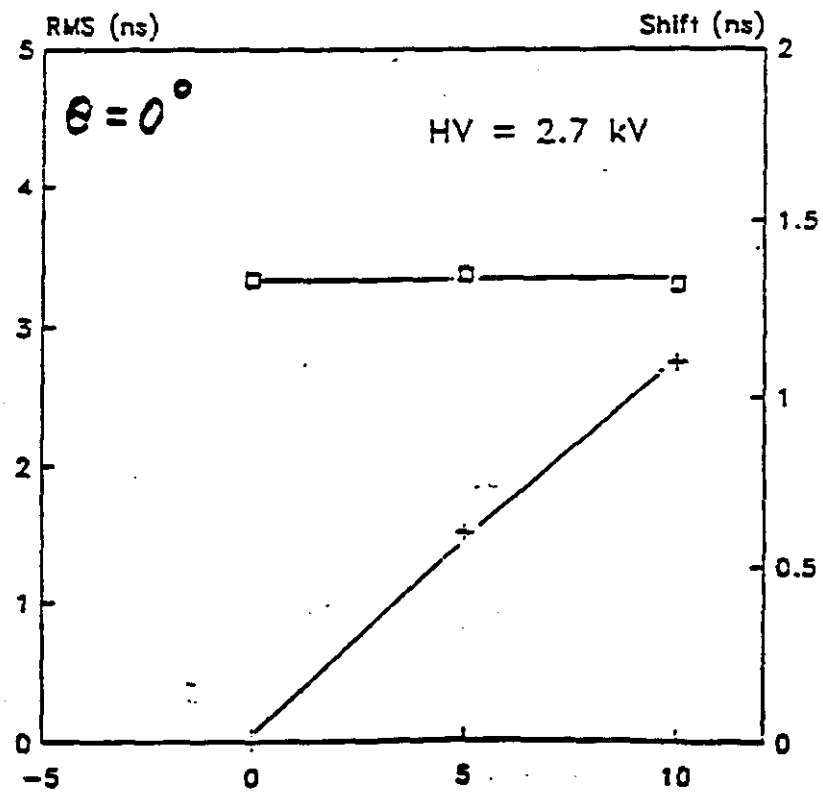
BROOKHAVEN NATIONAL LABORATORY	
Project: GEM-Muon Level 1 Local Encoder	
Date: 2/5/93	Drawn By: M. Atiya



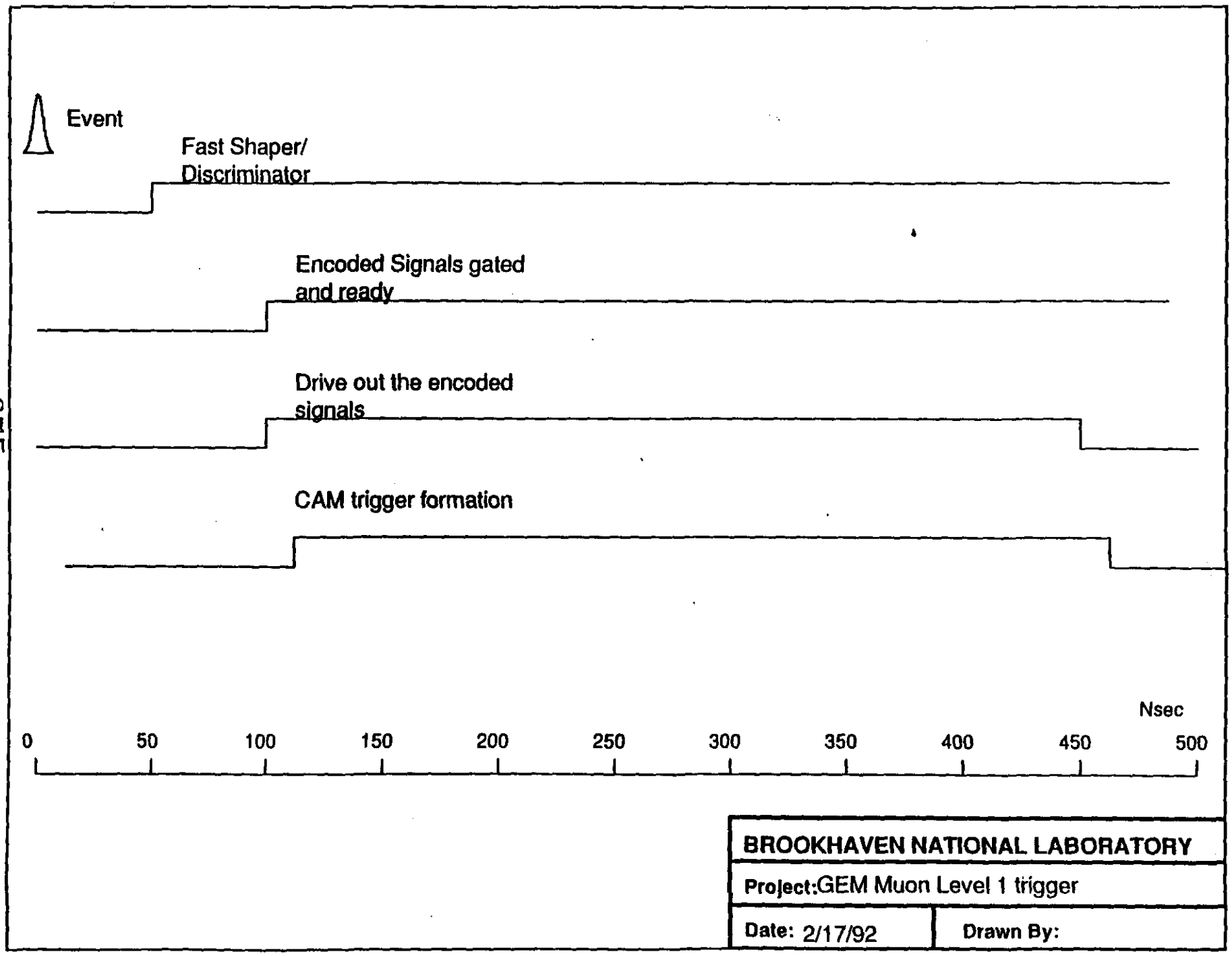
BROOKHAVEN NATIONAL LABORATORY	
Project: GEM-Muon Level 1 CAM & Encoder	
Date: 2/5/93	Drawn By: M. Atiya

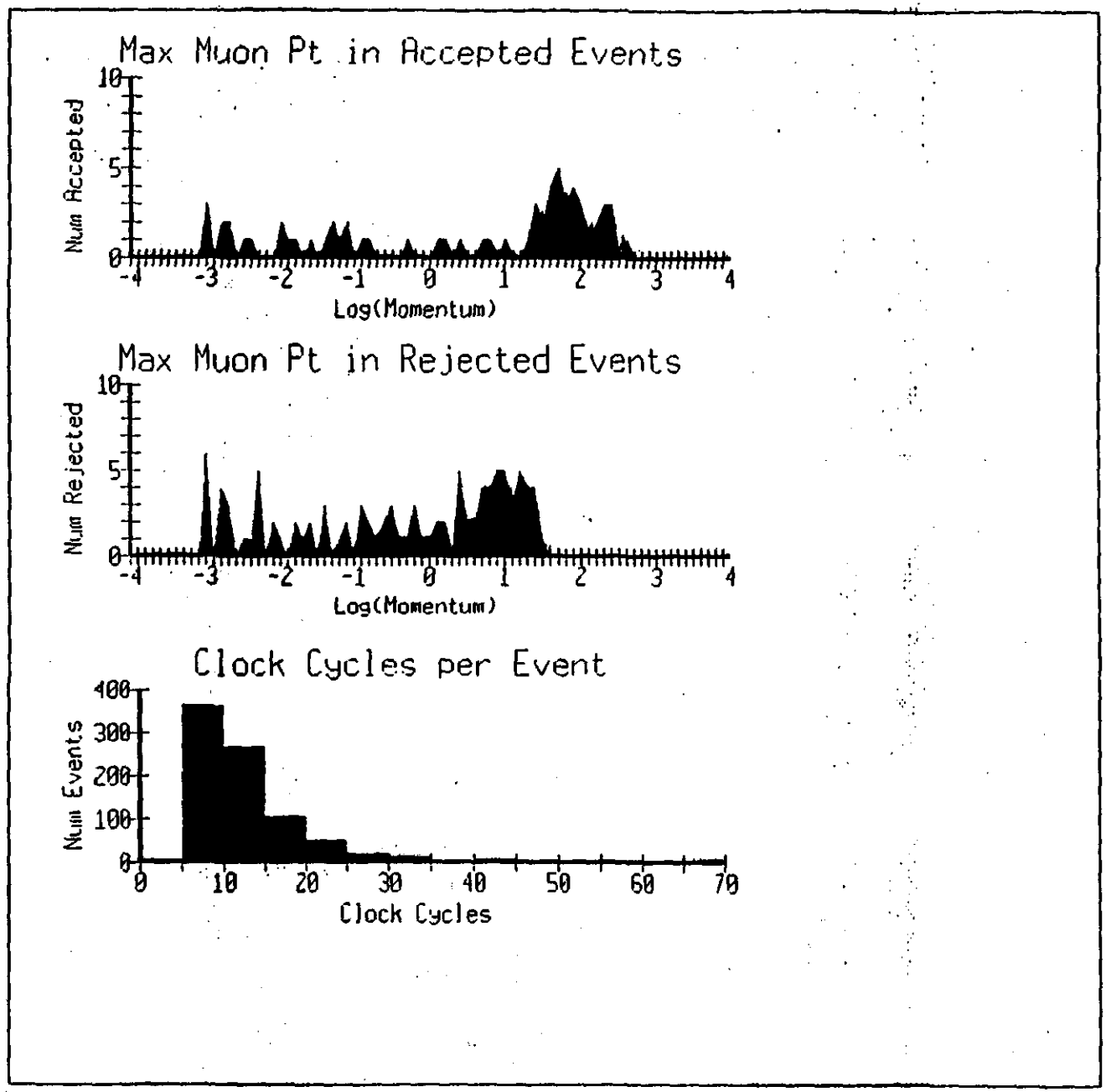

On-Camber Component of the Muon Level 1 Trigger
On-Detector Component of the Muon Level 1 Trigger
SL1
Encoded Signals from Chamber Readout
Sector Encoder
Output Bus (16 bits)
Cable Out
SL2
Encoded Signals from Chamber Readout
Sector Encoder
Output Bus (16 bits)
Cable Out
SL3
Encoded Signals from Chamber Readout
Sector Encoder
Output Bus (16 bits)
Cable Out
Repeat Four Times to form A Super Sector
On-Detector Trigger Card
Receiver bank
Associative Memory Bank
Receiver bank
Associative Memory Bank
Receiver bank
Associative Memory Bank
Receiver bank
Associative Memory Bank
Glue Logic & Trigger Signal Transmission
Protocol Controller (FPGA)
BROOKHAVEN NATIONAL LABORATORY
Project: GEM-Muon-Level 1 Trigger
Date: 2/9/93
Drawn By: M. Atiya

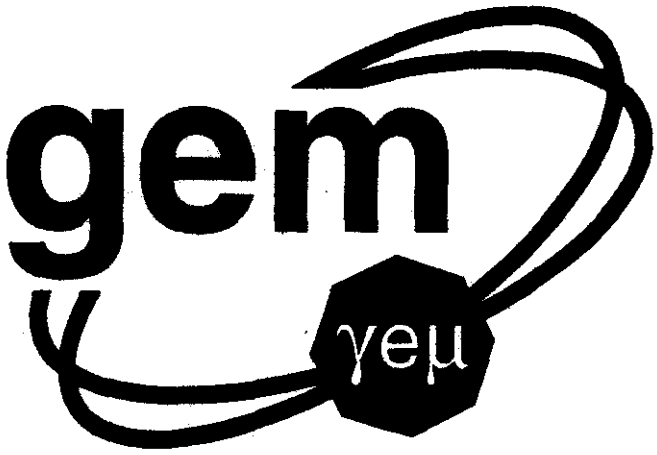




HV = 2.7 kV
σ = 3.5 ns


Event
Fast Shaper/
Discriminator
Encoded Signals gated
and ready
Drive out the encoded
signals
CAM trigger formation
Nsec
0
50
100
150
200
250
300
350
400
450
500
BROOKHAVEN NATIONAL LABORATORY
Project:GEM Muon Level 1 trigger
Date: 2/17/92
Drawn By:


Max Muon Pt in Accepted Events
Num Accepted
10
5
0
-4
-3
-2
-1
0
1
2
3
4
Log(Momentum)
Max Muon Pt in Rejected Events
Num Rejected
10
5
0
-4
-3
-2
-1
0
1
2
3
4
Log(Momentum)
Clock Cycles per Event
Num Events
400
300
200
100
0
0
10
20
30
40
50
60
70
Clock Cycles



Presentation by:

G. Liu

Combinatorial Approach for Muon Trigger

G. Lin

Advantages:

* Highly parallel
  → can handle high rate
* Simple, straight forward
* can be fully synchronized with the bunch crossing

Problems:

* number of signal cables ???
* programability ???

FPGA solve both problems.

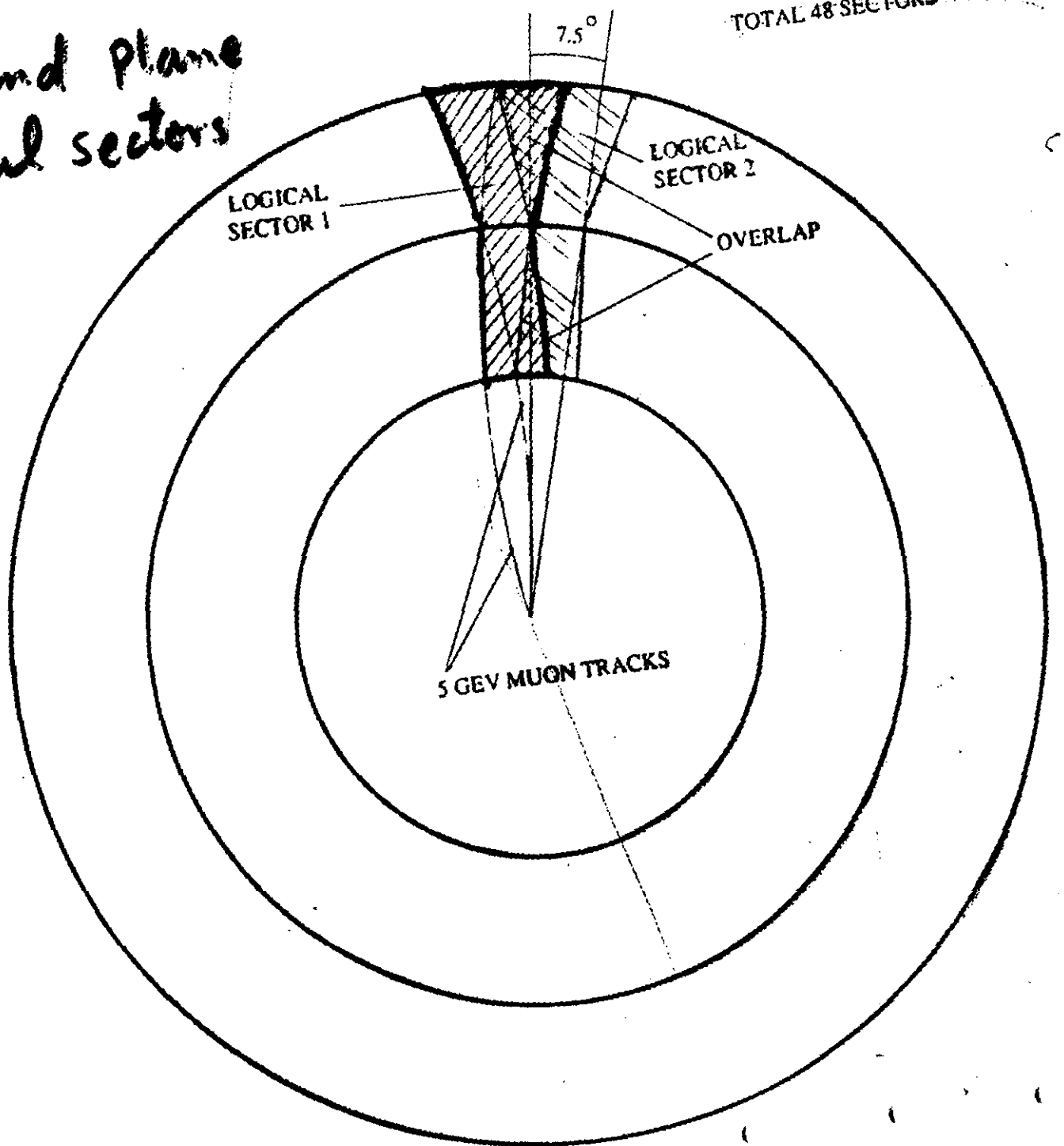
* "downloadable"
* physics can be programed inside detector
  → greatly reduce cables
* other advantages ....

Front End and Local Coincidence

(most conveniently implemented into the muon readout chip)

1) N out of 6 coincidence where $1 \leq N \leq 6$ programable.
2) Local vector should be brought out of the chip
3) OR signals so that each signal corresponds to a segment of 4 strips wide
   → 2cm for innerlayer
   3 cm for middle layer
   4 cm for outer layer
4) Maintain parallelism
   → DO NOT ENCODE

Barrel Bend plane
→ 48 Logical sectors



Each Logical Sector:

Ø signals:

Inner SL: 46 signals

middle SL: 25 signals

outer SL: 56 signals

Local vector signals:

11 signals each SL

→ Total 160 inputs

Logic Gates:

25 X 28 = 700 patterns

→ 700 AND Gates

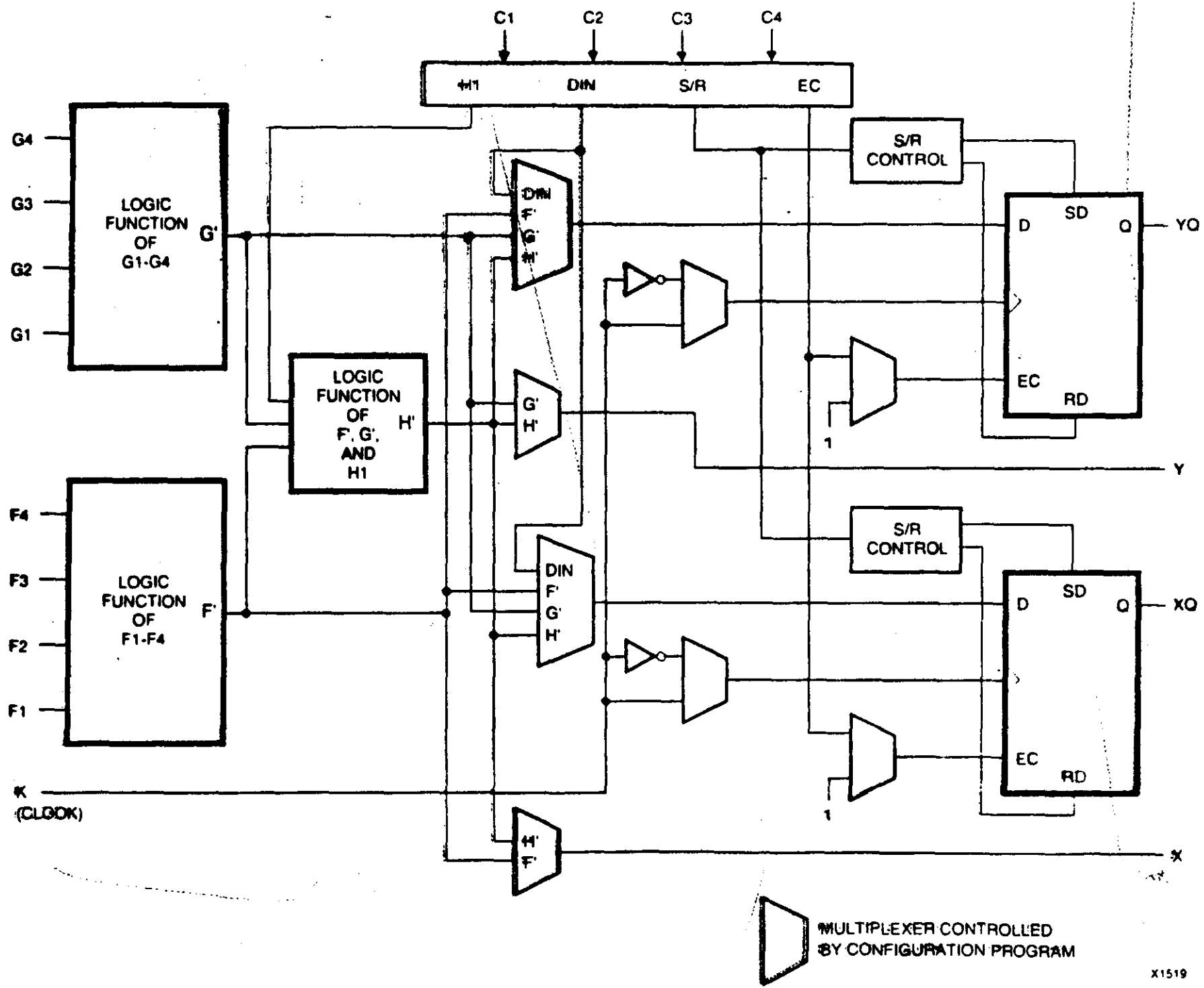
→ 350 Logic Blocks (CLBs)

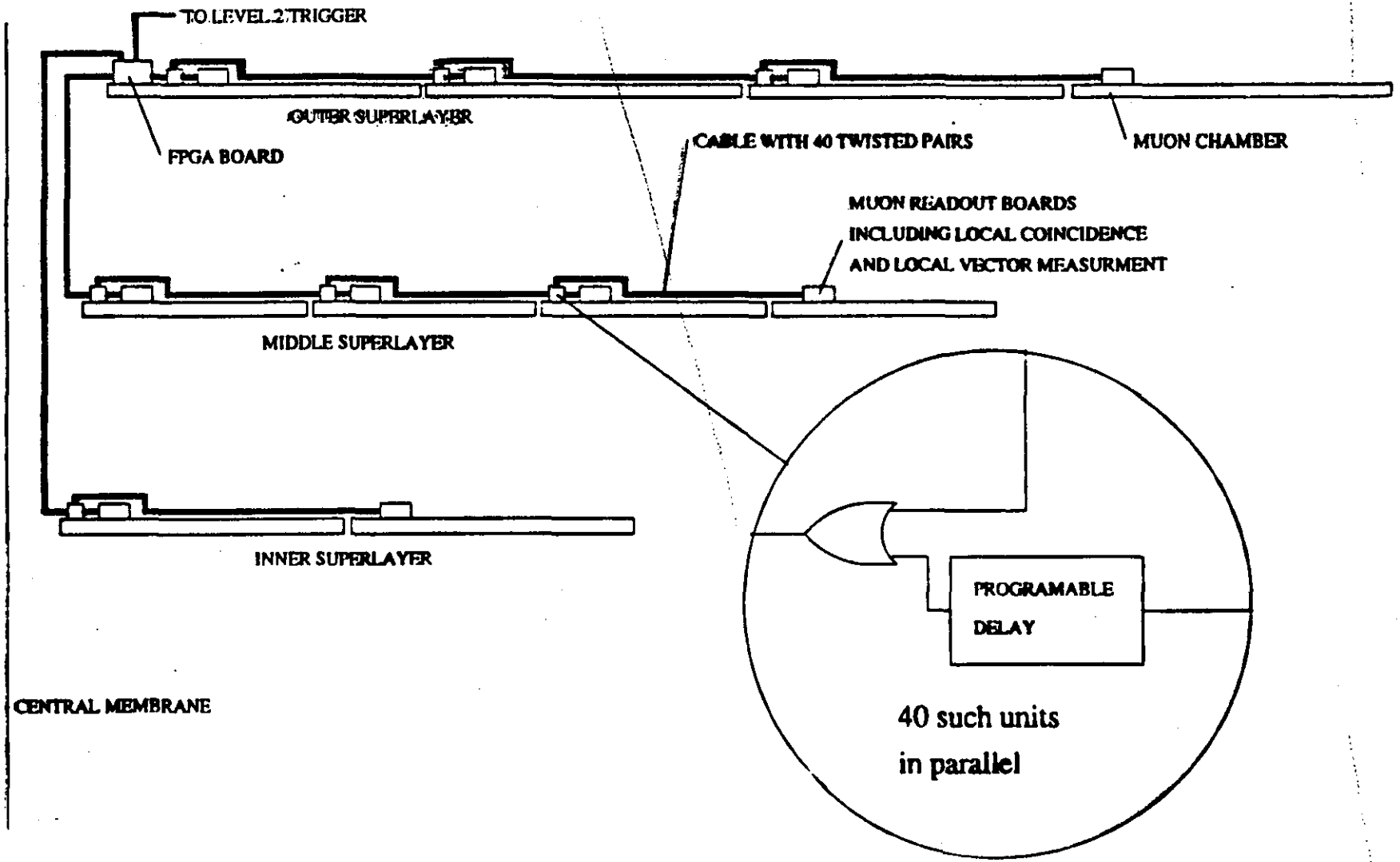
→ Several Choices:

			Available
XC4013	576 CLBs	192 I/Os	3093
XC4016	676 CLBs	208 I/Os	3093
XC4020	900 CLBs	240 I/Os	?
XC4125	Same as XC4020 but faster		2094

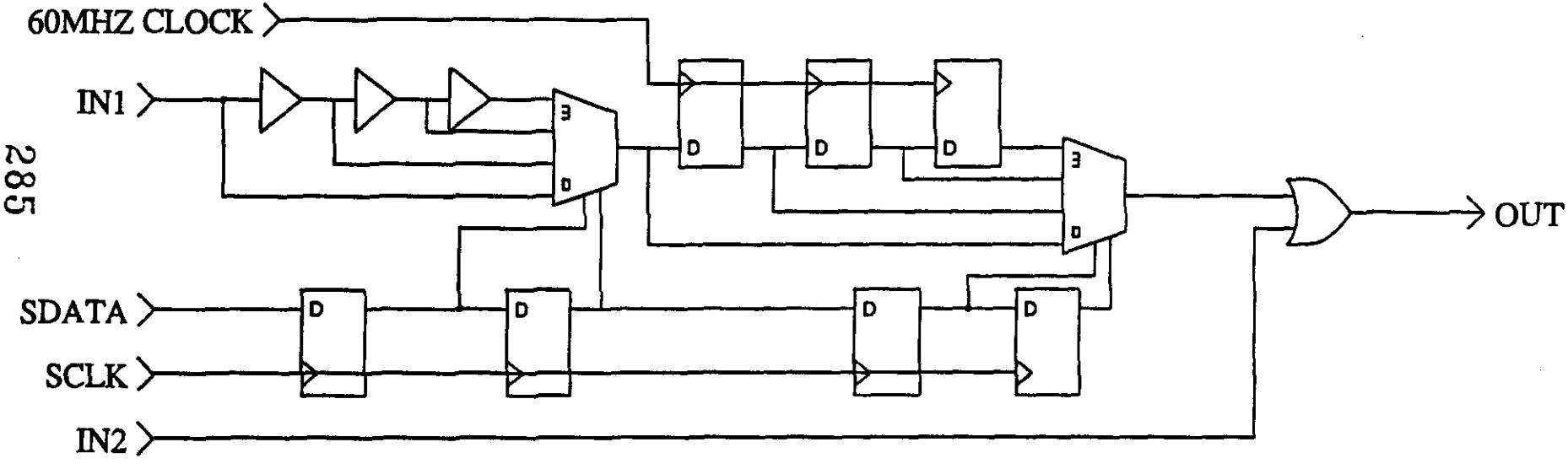
Or 3 XC4005H in parallel

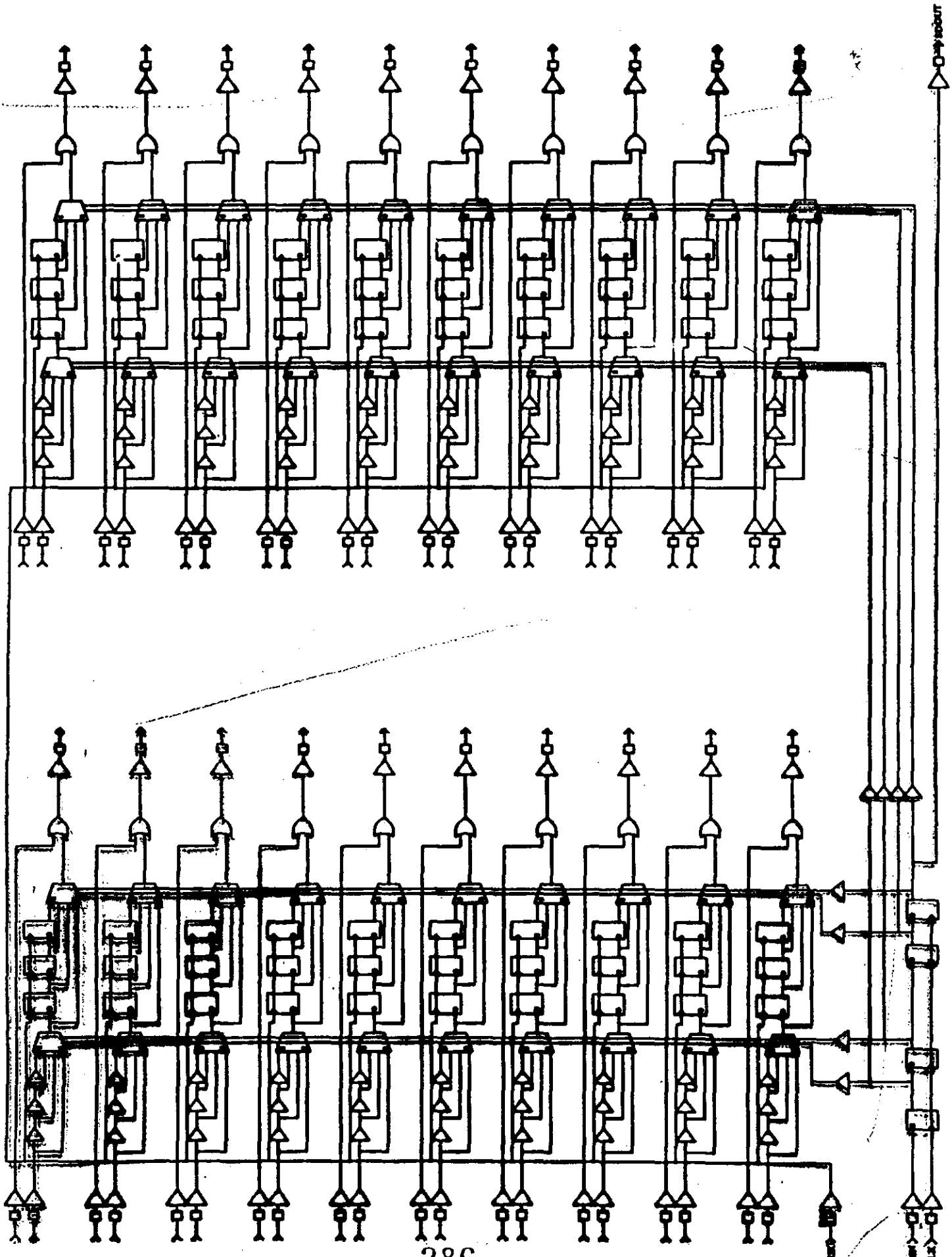
→ 588 CLBs 196 I/Os ——→ NOW ~$300

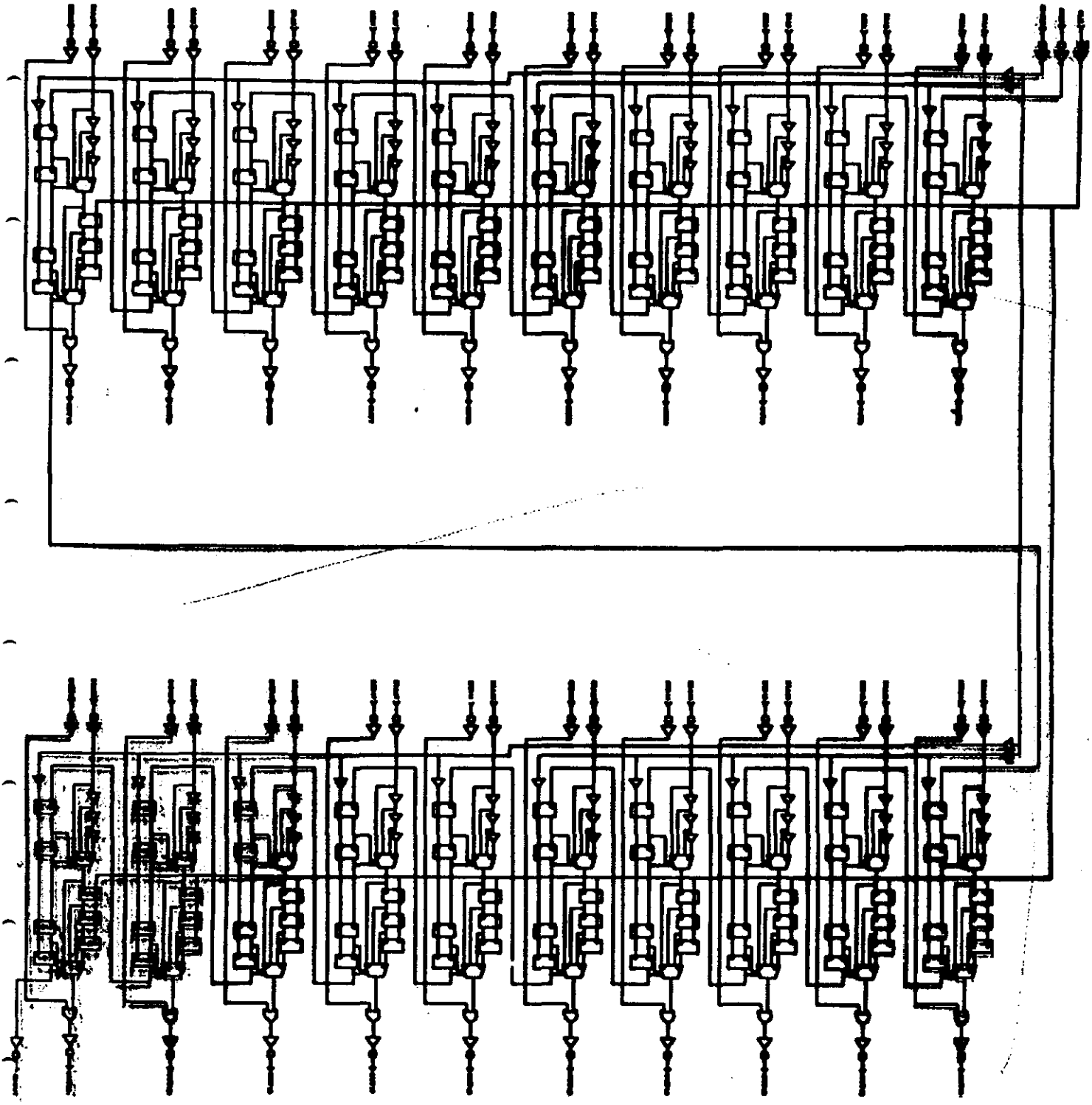

C1
C2
C3
C4
H1
DIN
S/R
EC
G4
G3
G2
G1
LOGIC FUNCTION OF G1-G4
G'
LOGIC FUNCTION OF F', G', AND H1
H'
F4
F3
F2
F1
LOGIC FUNCTION OF F1-F4
F'
K
(CLOCK)
DIN
F'
G'
H'
S/R CONTROL
D
SD
Q
EC
RD
YQ
Y
XQ
X
1
MULTIPLEXER CONTROLLED BY CONFIGURATION PROGRAM
X1519


TO LEVEL 2 TRIGGER
OUTER SUPERLAYER
FPGA BOARD
CABLE WITH 40 TWISTED PAIRS
MUON CHAMBER
MUON READOUT BOARDS
INCLUDING LOCAL COINCIDENCE
AND LOCAL VECTOR MEASURMENT
MIDDLE SUPERLAYER
INNER SUPERLAYER
PROGRAMABLE
DELAY
40 such units
in parallel
CENTRAL MEMBRANE

LOGIC ELEMENT OF THE OR BOARD







Cost Estimates (half a Barrel)

FPGAs: Bend: 48
NonBend: 4
Total: 52

$1000 each
(include board) → $52K

OR boards: Bend: 7×48=336
NonBend: 47×12=564
total: 900

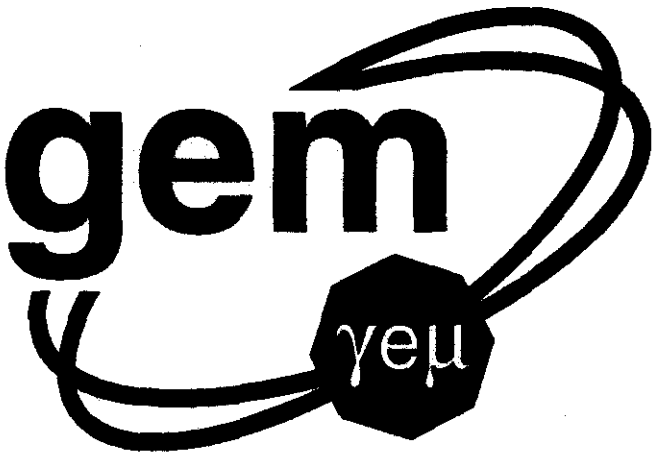
$60 each → $54K

Cables: Bend: 10×48=480
(40 Twisted pairs) NonBend: 48×12=576
total: 1056

$50 each → $52.8K
(includes connectors)

total: 158.8K

Whole detector: 4×158.8K = 635.2K



Presentation by:

M. Bowden

DAQ Overview

2/24/93

M. Bowden

System Requirements

- **Number of Input Channels**

Si	**2525**	**(may decrease)**
IPC	**3125**	
Cal	**3335**	**(may decrease)**
μ	**1270**	
Total	**~10,000**	

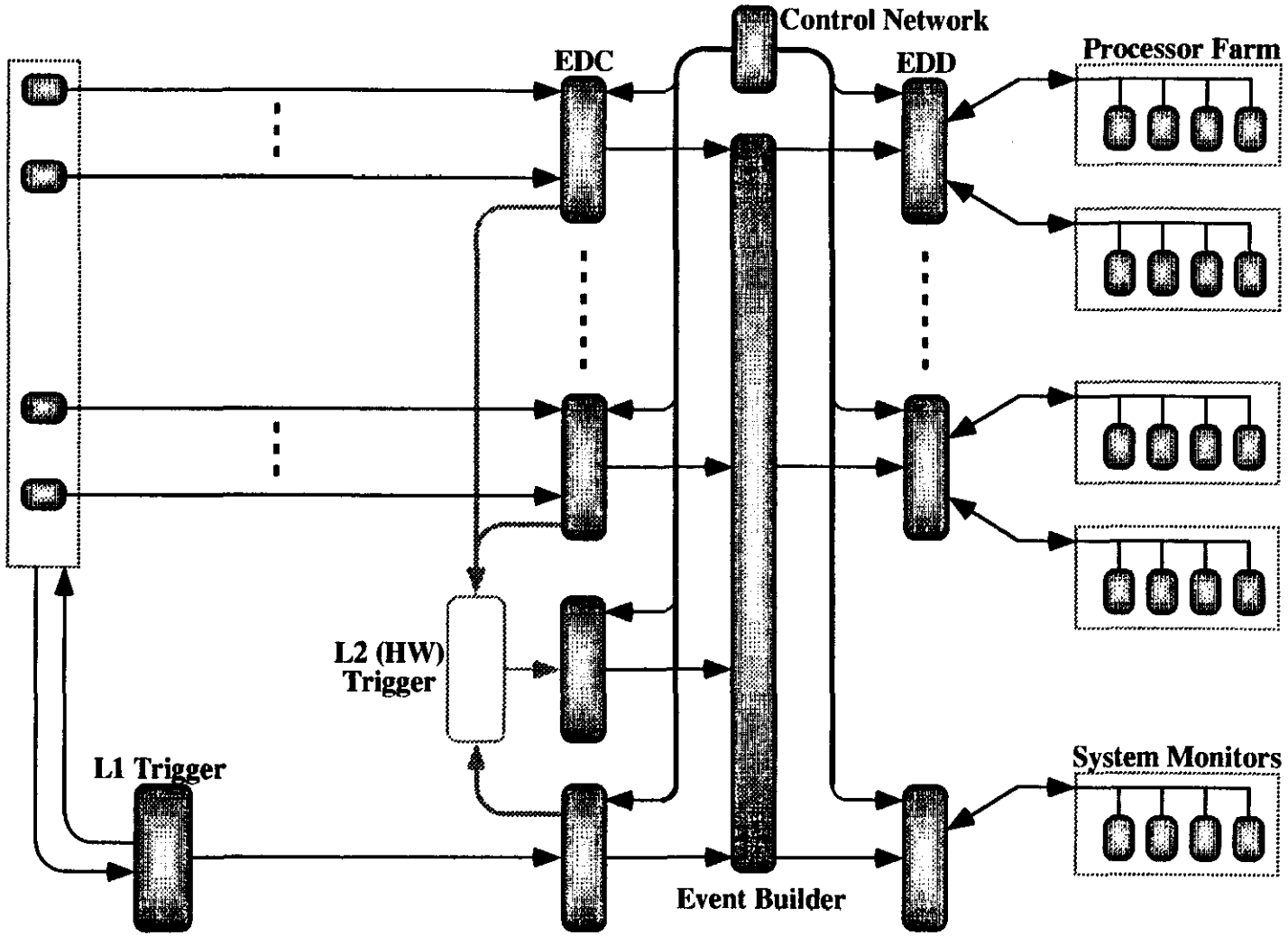
Up to12,200 channels supported

- **Data rate after Level 1 Trigger**

200-300 KBytes/event X 100 KHz => 20-30 GBytes/sec

Up to 60 GBytes/sec supported on input to Data Collectors

Up to 40 GBytes/sec supported by Event Builder
(scalable in 5 GByte/sec increments)


Control Network
EDC
EDD
Processor Farm
L2 (HW)
Trigger
L1 Trigger
System Monitors
Event Builder

Data and Control Flow

1) For each Level 1 Accept, trigger summary information is transmitted to the Level 1 Trigger EDC.

2) A Processor with a free event buffer issues a data request to the Level 1 Trigger EDC which returns the trigger summary.

3) The Processor then issues one or more requests to specific EDCs or EDC groups for data needed by the Level 2 Trigger.

4) If the event is accepted by the Level 2 Trigger, the Processor issues a request for all event data.

5) Level 3 processing continues in the same processor. When finished, a new event request is transmitted.

Note:

Multiple Level 2/3 processes execute on each Processor. A process is suspended during data requests, allowing a context switch to the next pending process. Data access times are comparable to disk access times (10-20 msec).

Selective Readout Option

Only the data needed by the Level 2 Trigger is transmitted to the Processor. Data requests are issued by the Processor via the Control Network. Requests may designate specific Event Data Collectors, or any pre-defined group of Event Data Collectors.

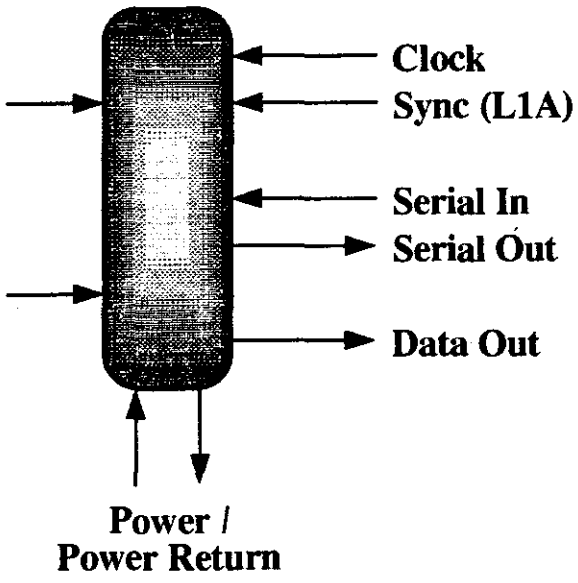
Advantages:

- Reduces bandwidth requirements and cost of Event Builder and Event Data Distributors (estimated savings...$3M).

Disadvantages:

- Increases latency.
- Increases complexity of Event Data Collectors and Event Data Distributors.
- Requires better modeling of Level 2 Trigger.
- Difficult to load balance data flow.
- Increase "real-time" requirements of Processor Farm.

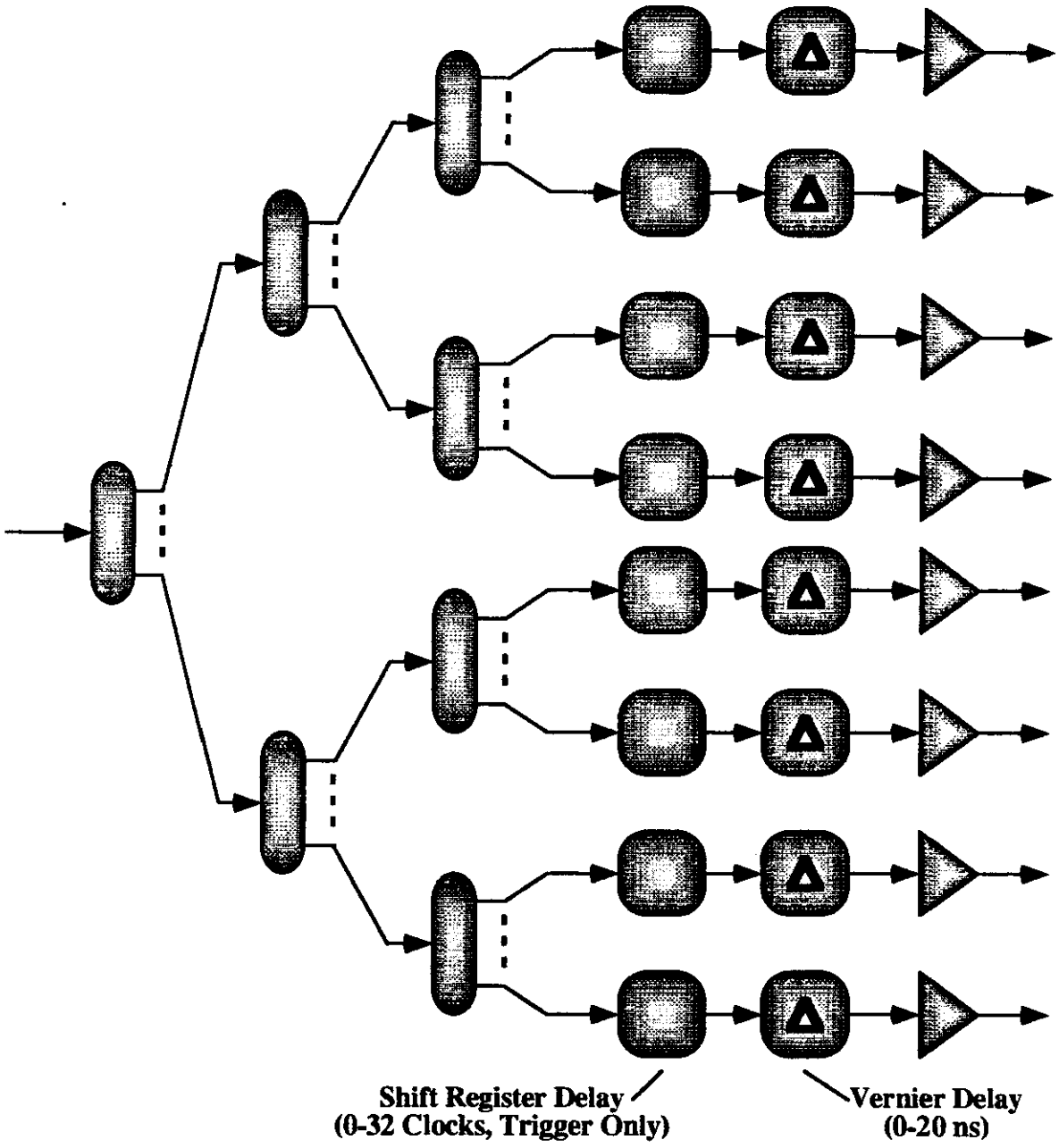
Minimal Front-end Interface



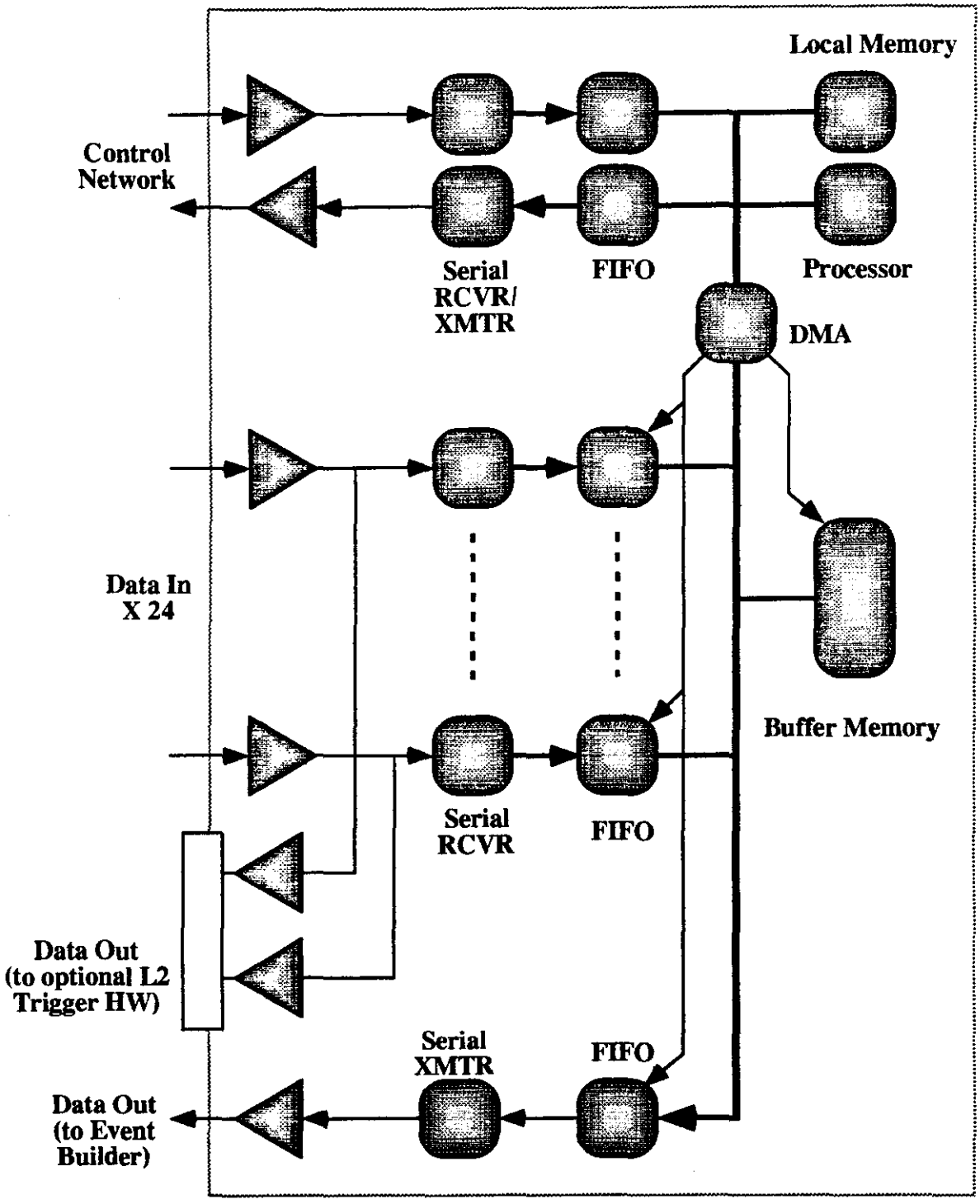
- Clock (62 MHz)
- Sync (62 Mbps, 31 MHz NRZ, clock synchronous)
- Serial I/O (20 Mbps, 10 MHz NRZ, asynchronous using 62 MHz clock for 3X oversampling, START bit + 16 data bits)
- Data Out (62 Mbps, 31 MHz NRZ, clock synchronous, START bit + 16 data bits)

Sync signal is interpreted as L1A unless alternate crossing synchronous command is sent on Serial In line.

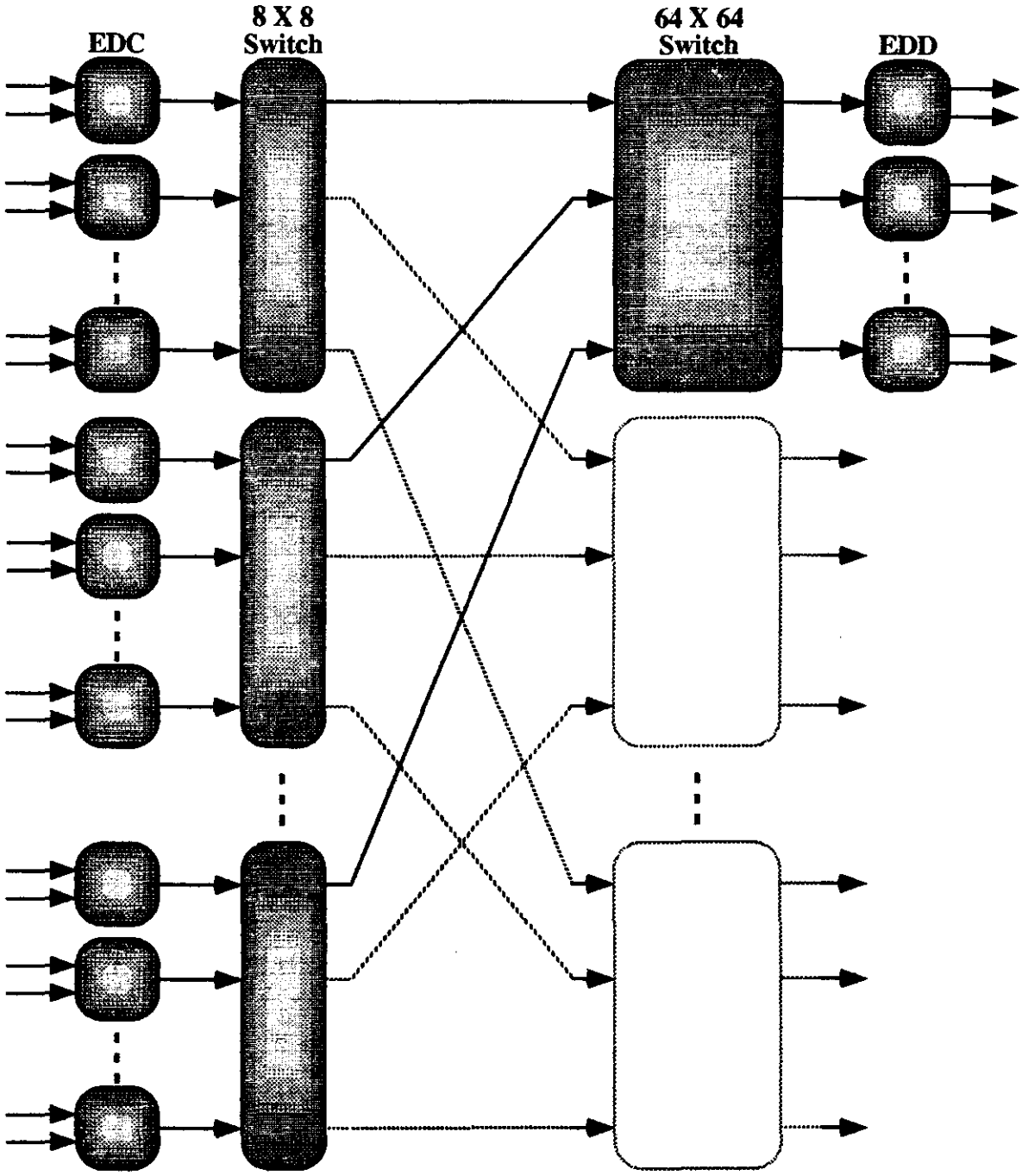
All signals (except Data Out) are differential copper to/from local fanout board which serves 24 front-end boards. Fanout board connects via fiber to clock, trigger and control network in Electronics Room. Data Out is fiber direct to EDCs in Electronics Room.



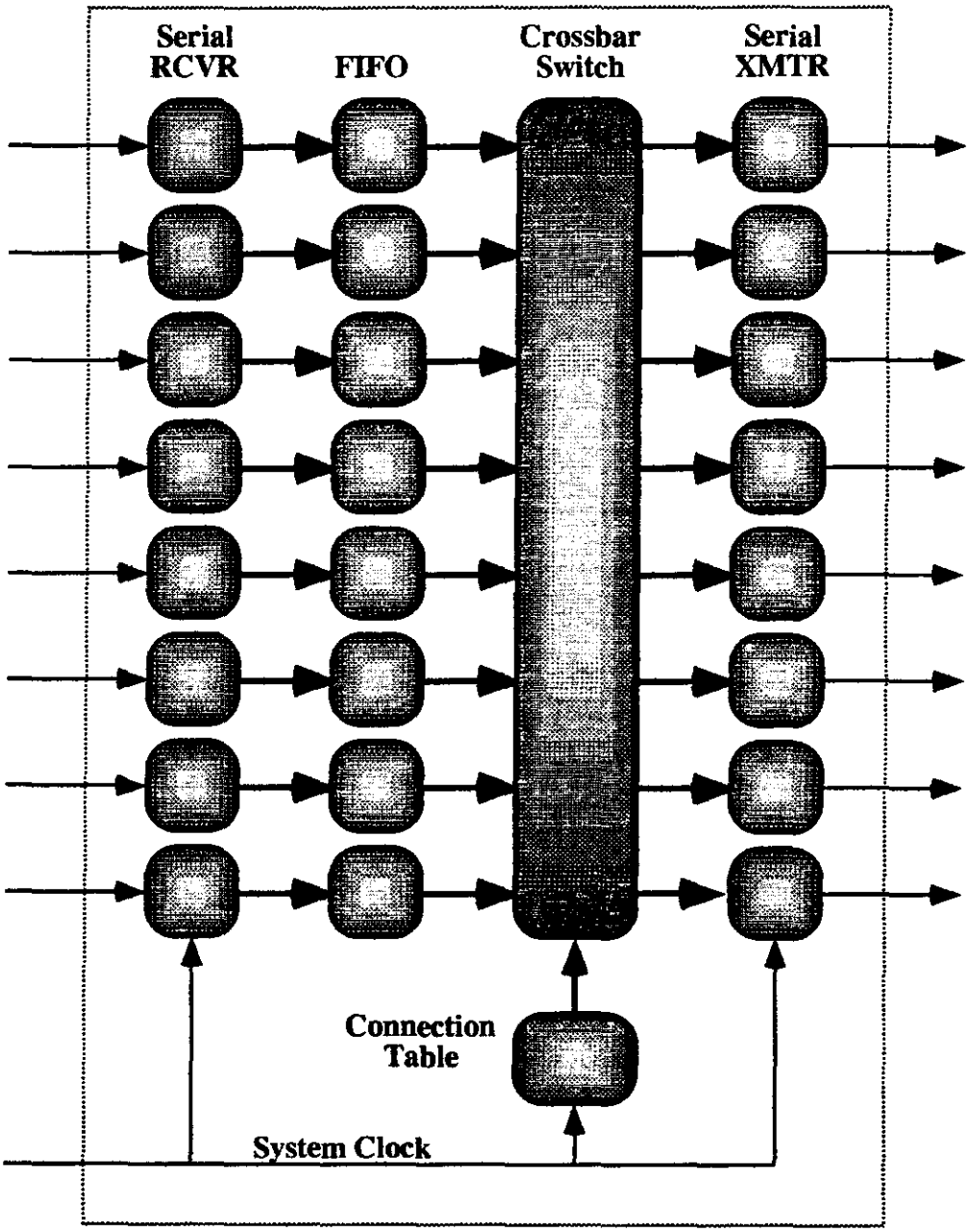
Clock / Trigger Distribution (Source)



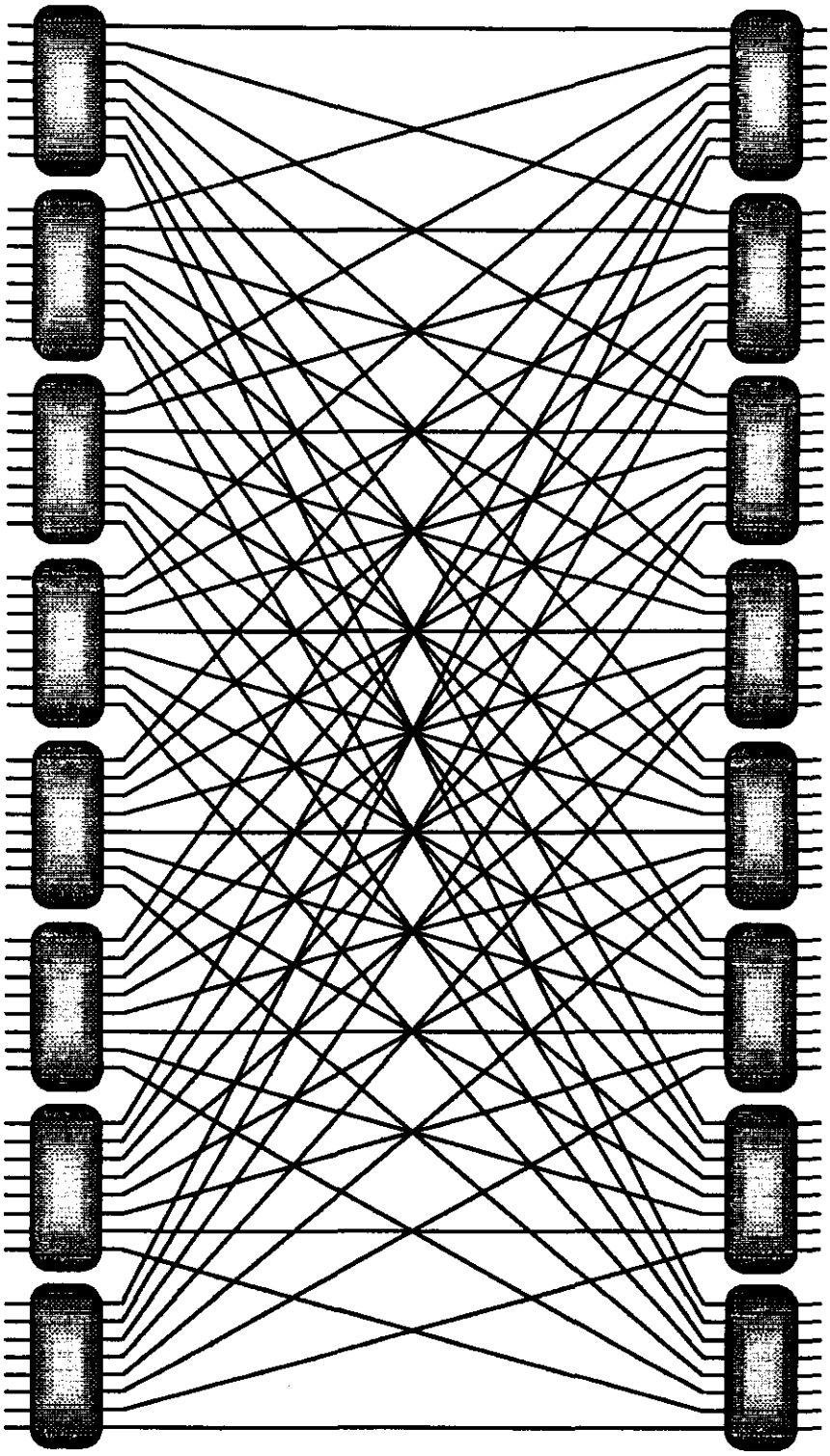
Event Data Collector



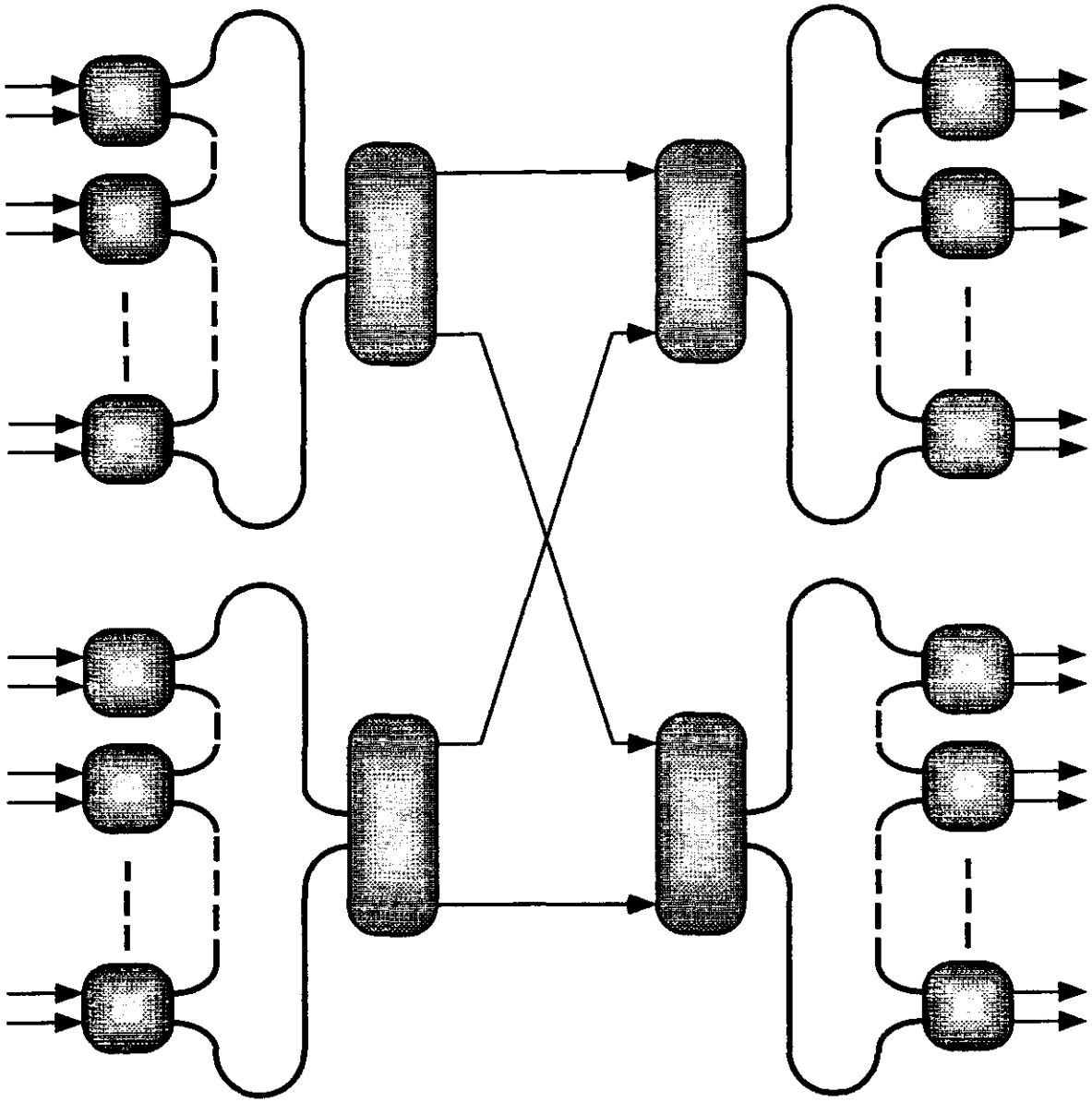
Event Builder

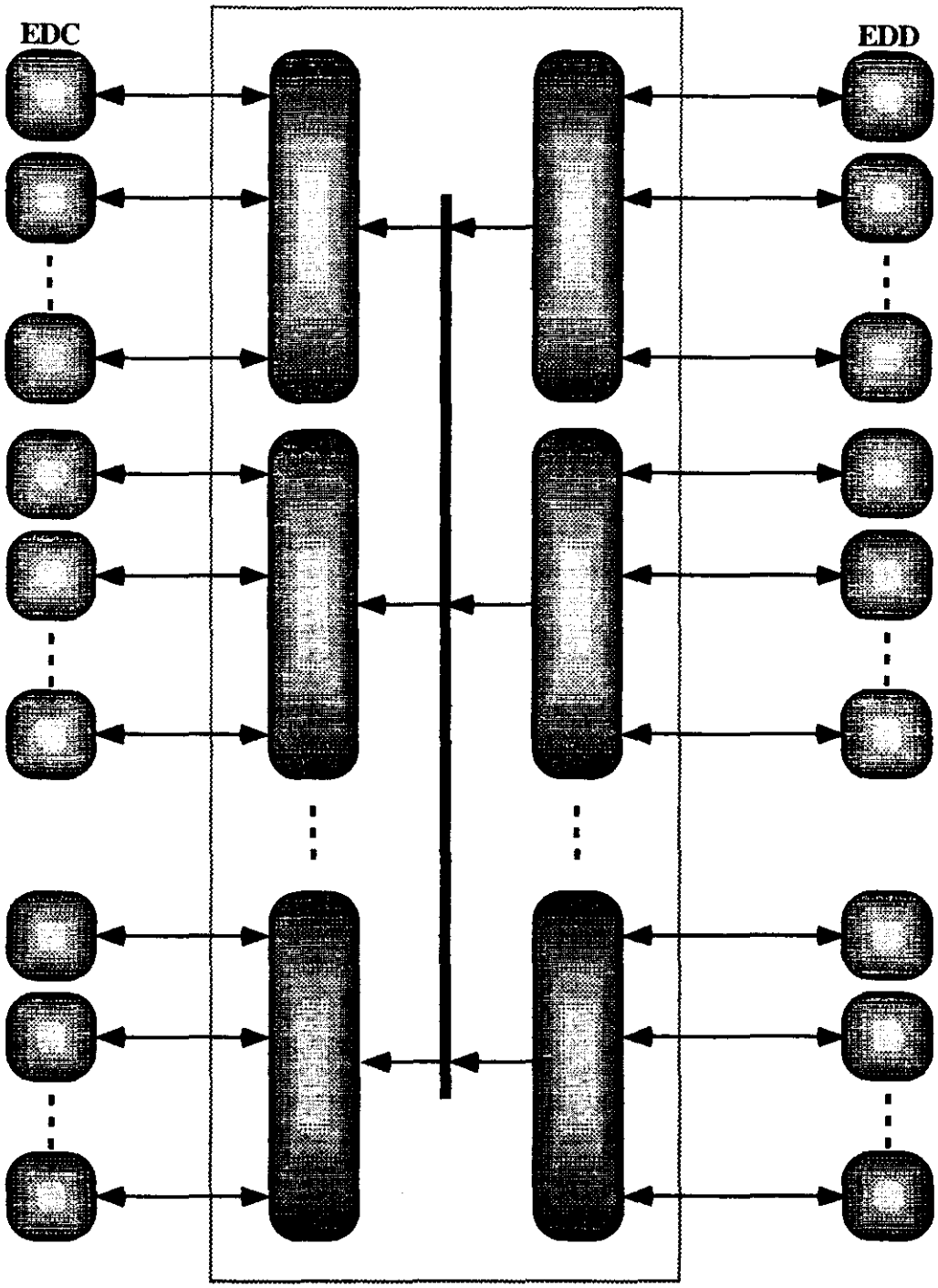


8 X 8 Switch Module

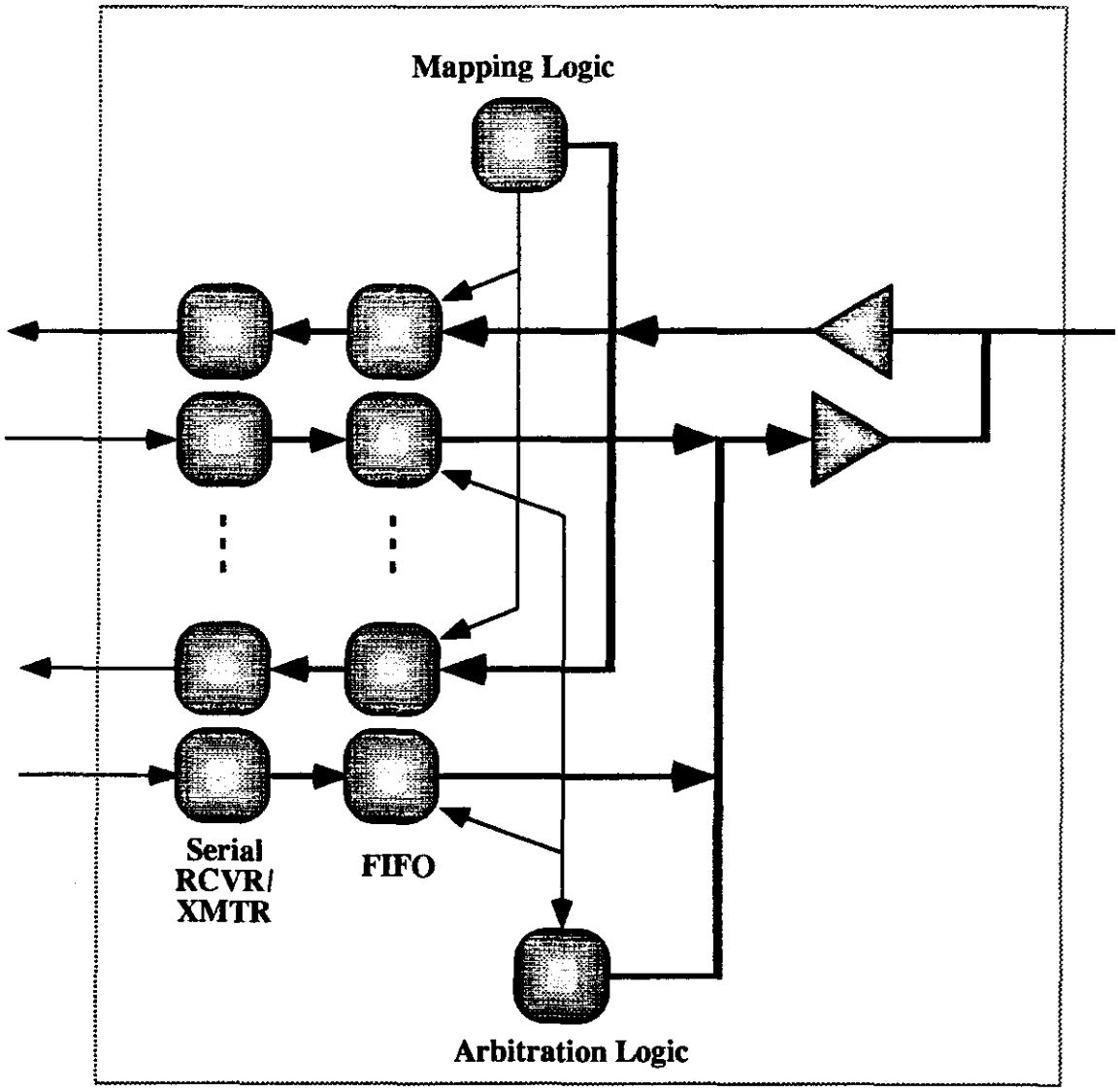


64 X 64 Switch (1 crate.....5 GBytes/sec)





Control Network



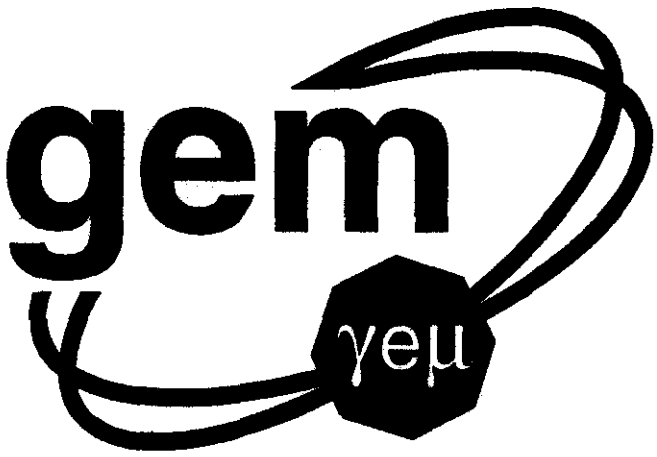
Control Network Module

Cost Summary

Development (NRE) Costs (Design, Prototype, Assembly, Installation, Test, Project Management)		$6.5M
Production Cost (Components only)		$7.5M
Event Data Collectors	($3.5M)	
Event Builder	($1.0M)	
Event Data Distributors	($1.0M)	
Control Network & Misc	($0.5M)	
Clock/Trigger Distribution	($1.5M)	
Total		**$14M**

By Activity:

Design and Document	$2.5M
Prototype	$2.0M
Production	$9.0M
Install and Test	$0.5M
Total	**$14M**



Presentation by:

N. Lau

GEM Grounding System

- Provides facility grounding system to meet National Electrical Code and Department of Energy standards.

- Adopts single point ground principle for establishing signal reference.

- Uses Faraday shield isolation transformers and fiber optic cables extensively for subsystem isolation and keeping conducted electrical noise coupling local.

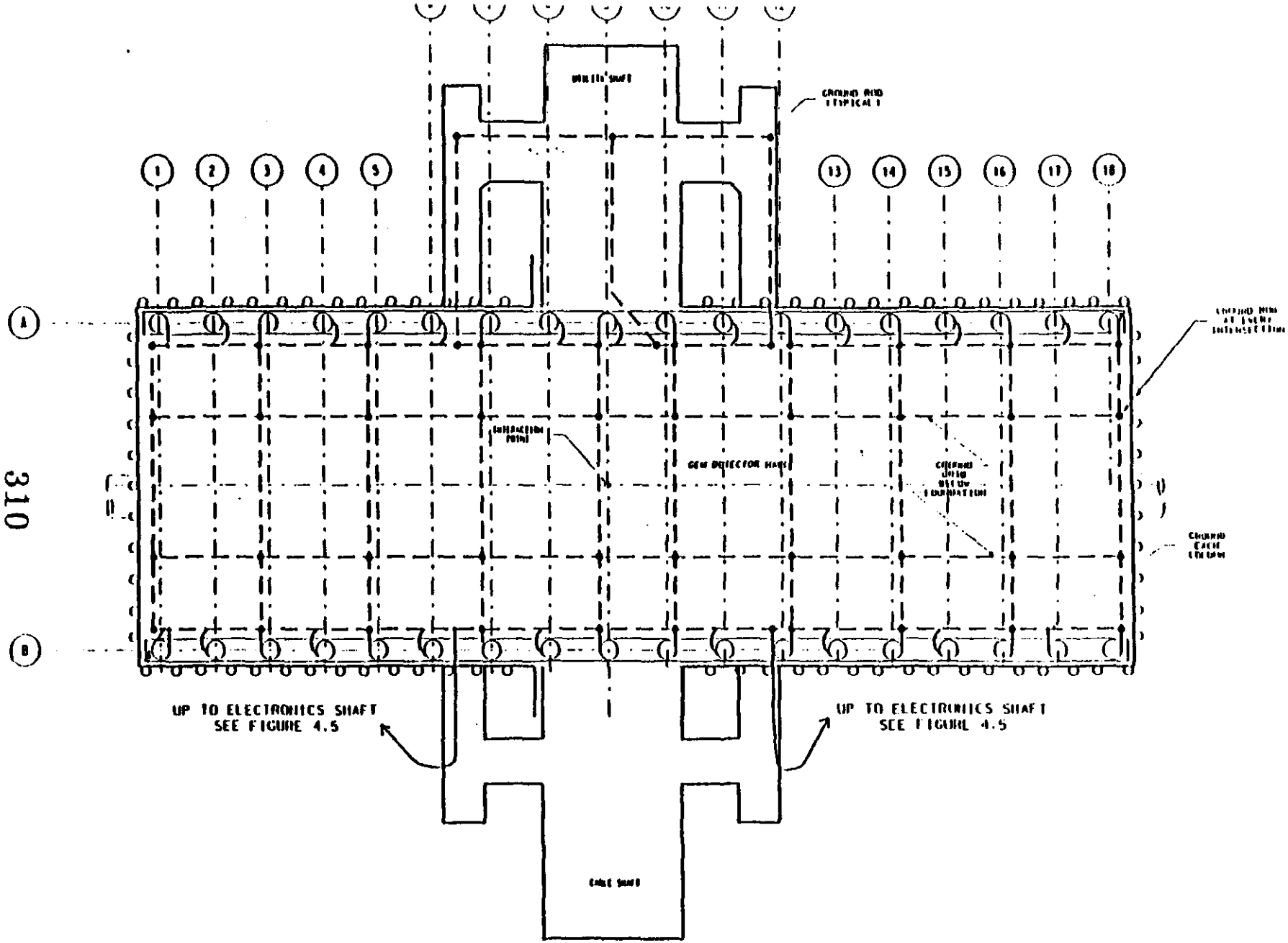
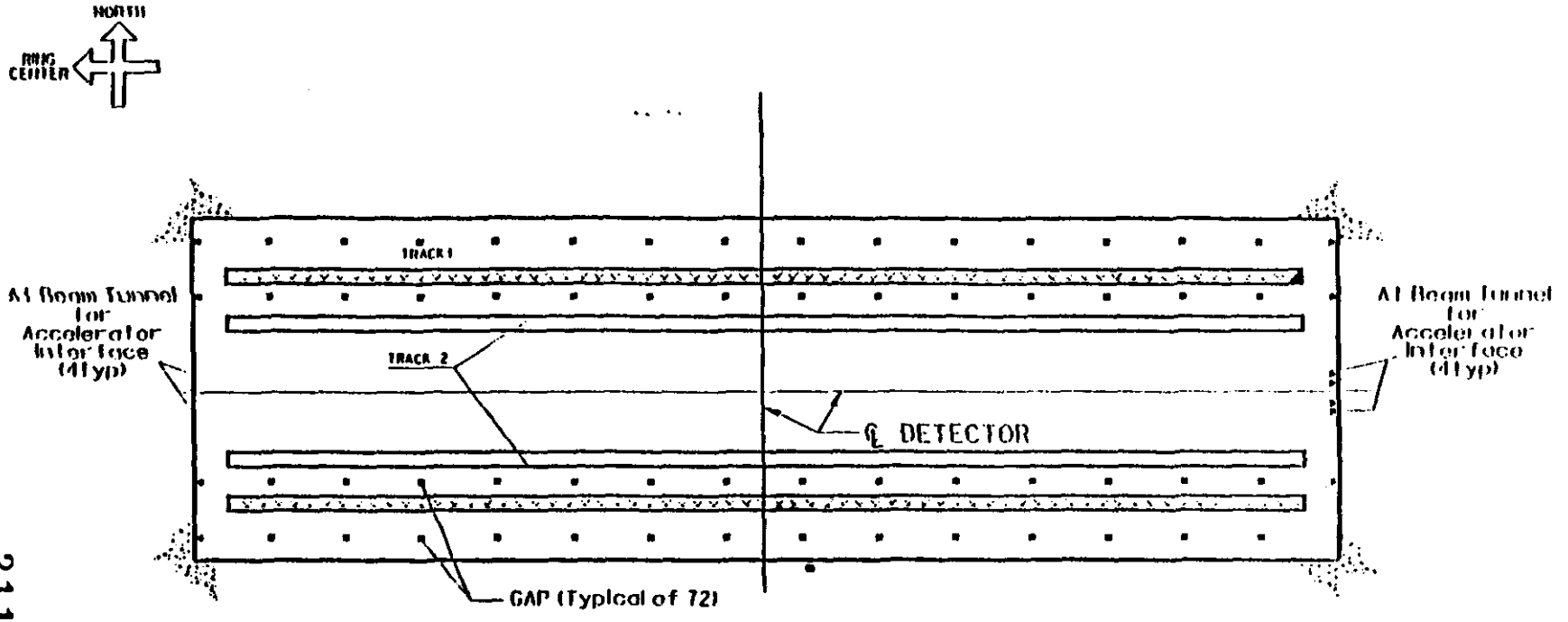


FIGURE 4.3
GEM HALL GROUNDING GRID

14 OCTOBER 1992
GDC/FK



See Fig 4-19 for the Location of Tracks 1 and 2

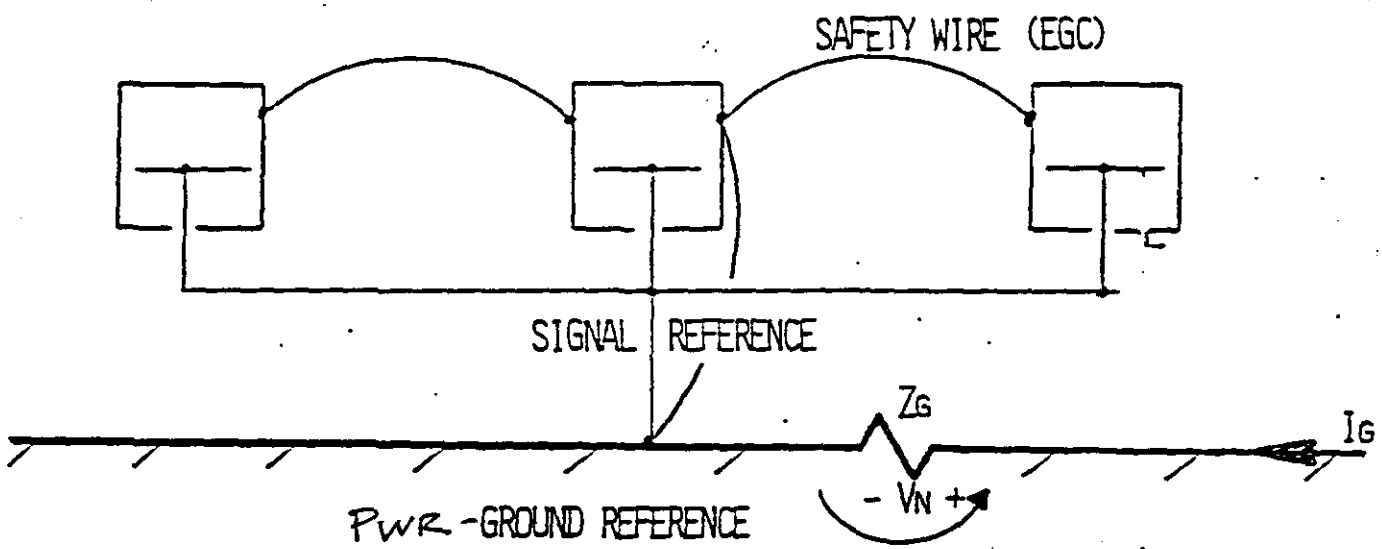
Symbol	Description
•	Symbol Indicates a Gounding Access Point (GAP) for connection to the Facility Ground Grid. Coordinate exact placement/location of GAPs with structural foundations/ columns, Detector/Beamline support structures, and Detector Load Paths.

gcd0000366
REF. FILEISh NONE
11-24-92
F.XDAT

Figure 18-5 GEM Grounding Access Points Locations

IDEAL SINGLE-POINT GROUND

SIGNAL



EXAMPLES: 1. 60 Hz POWER DISTRIBUTION SYSTEM.

2. TELEPHONE CO. C O GROUND.

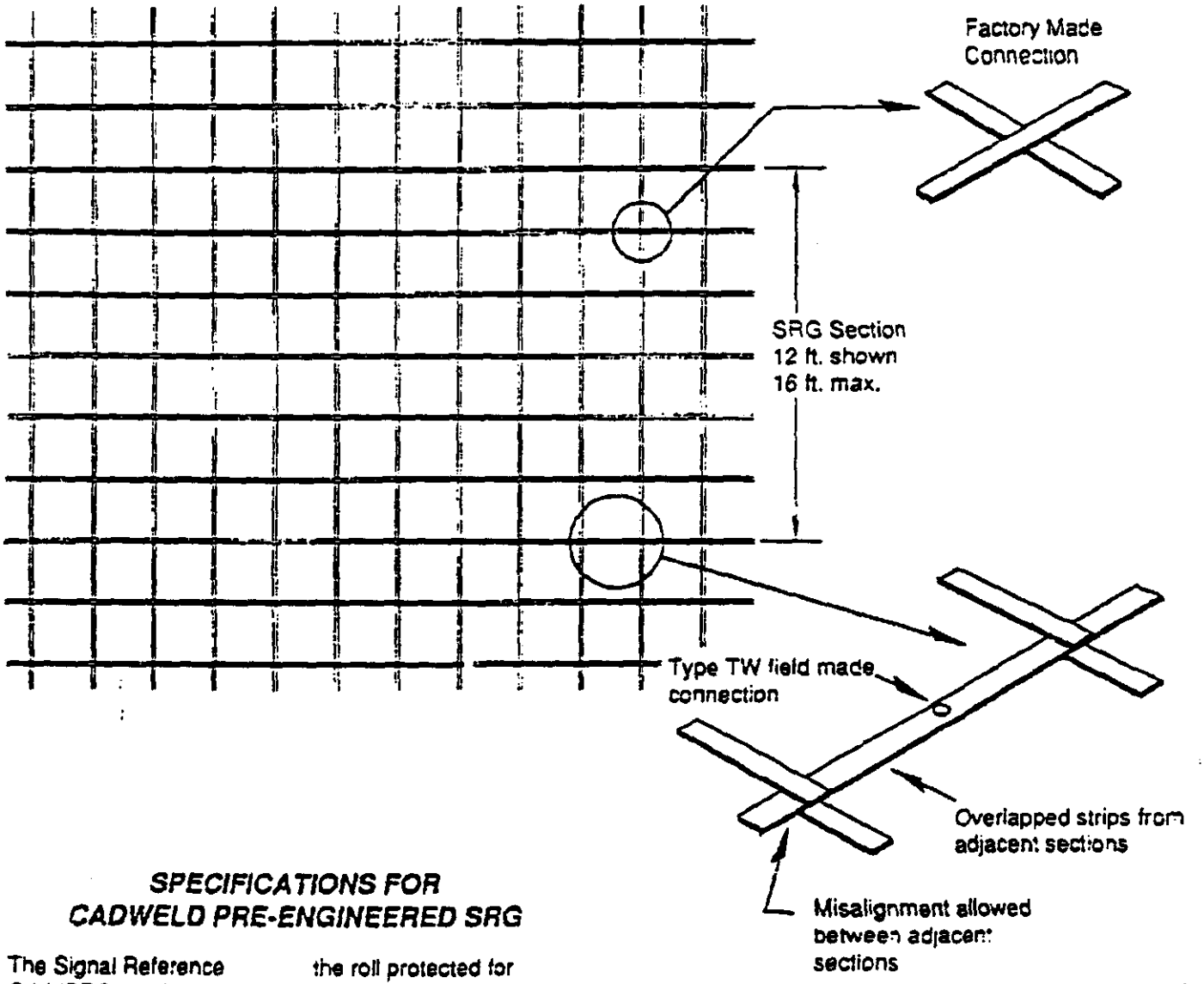
ADVANTAGES:

1. LOW FREQUENCY APPLICATIONS ONLY.
2. REDUCES CONDUCTIVELY-COUPLED NOISE BY ELIMINATING GROUND LOOPS (COMMON Z COUPLING).
3. No ESD Build-up

DISADVANTAGES:

1. LARGE NUMBER OF CONDUCTORS.
2. LONG CONDUCTORS.
3. BREAKS DOWN AT HIGH FREQUENCIES DUE TO ITEM 2.
4. CEASES TO EXIST AT HIGH FREQUENCIES DUE TO PARASITIC CAPACITANCE.
5. DIFFICULT TO MAINTAIN ONLY ONE CONNECTION.

SIGNAL REFERENCE GRID (SRG)



SPECIFICATIONS FOR CADWELD PRE-ENGINEERED SRG

The Signal Reference Grid (SRG) shall be manufactured from 2 inch wide by 26 AWG gage (0.0159 inch thick) copper strips on 2 foot centers. All crossovers shall be joined by welding. The SRG shall be furnished 4 to 16 feet wide. The sections shall be rolled on tubes with the outside of the roll protected for shipment.

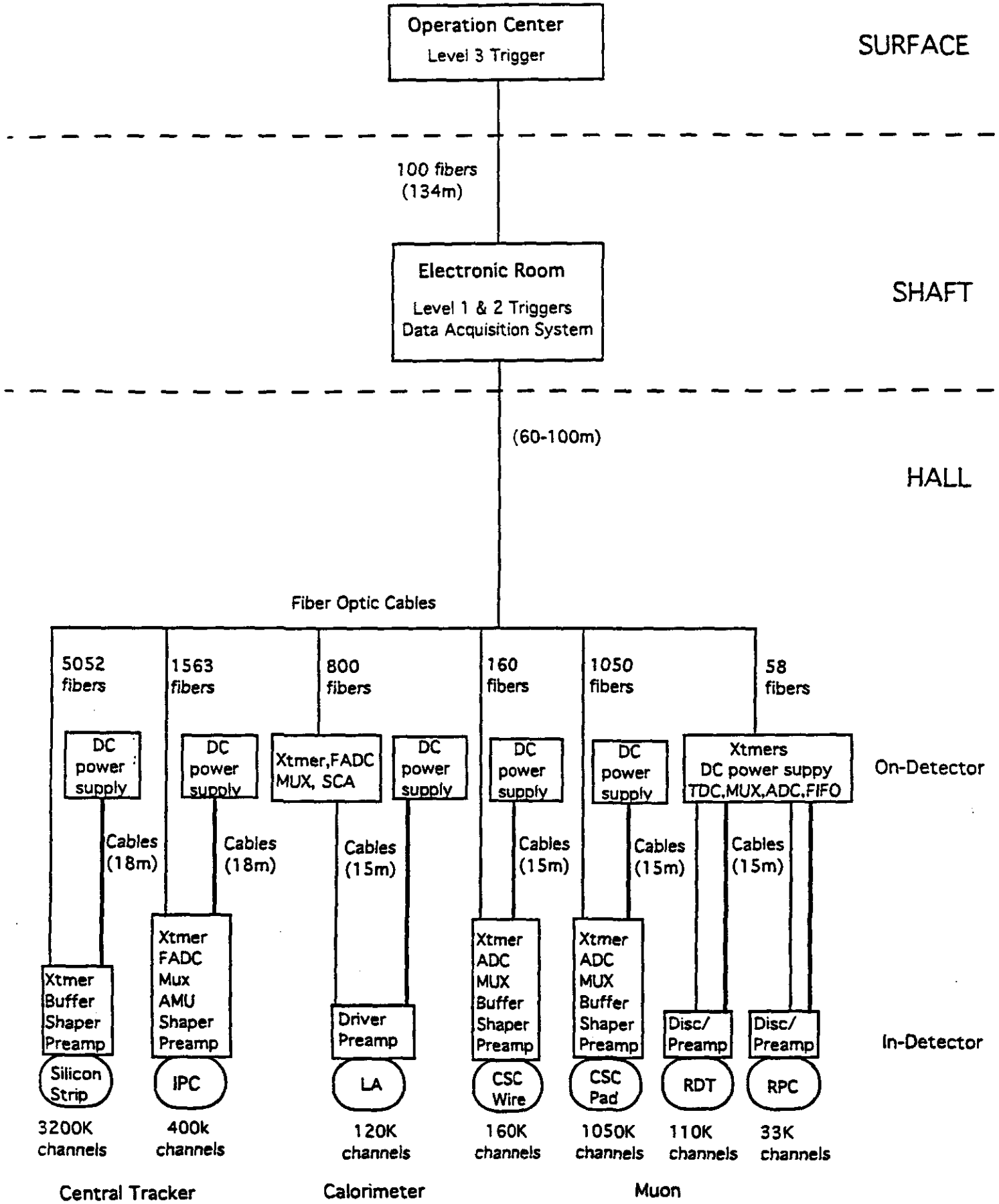
NOTES:

1. Other strip sizes are available.
2. Other spacing is available.
3. Roll weight usually limited to about 200 pounds gross weight for convenience (1200 sq. ft.).

ERICO® PRODUCTS INC
CLEVELAND, OHIO 44139

CADWELD®

1-800-248-WELD
FAX (800)462-4797



Electronics System Layout (November 18, 1992)

GEM/ELB1

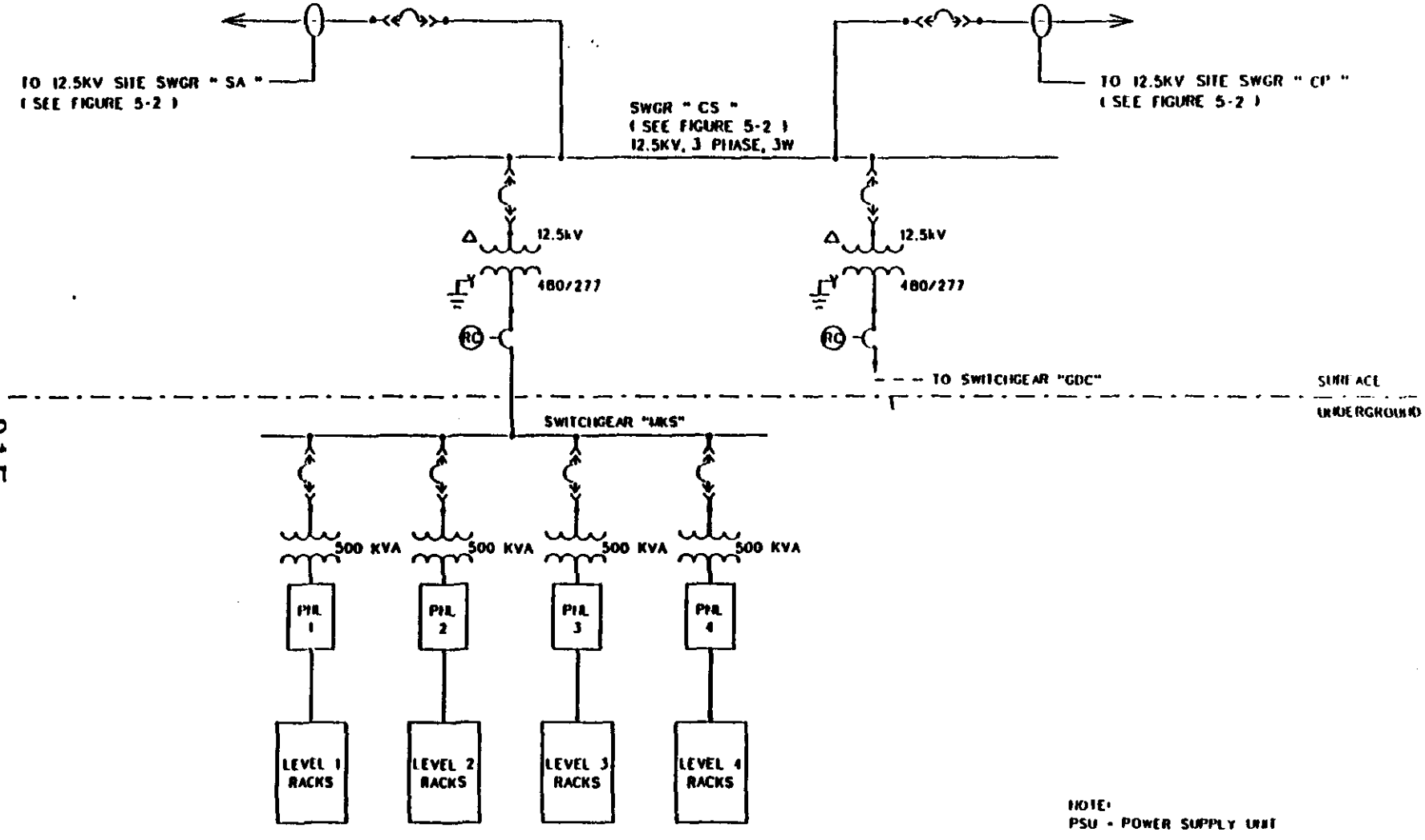
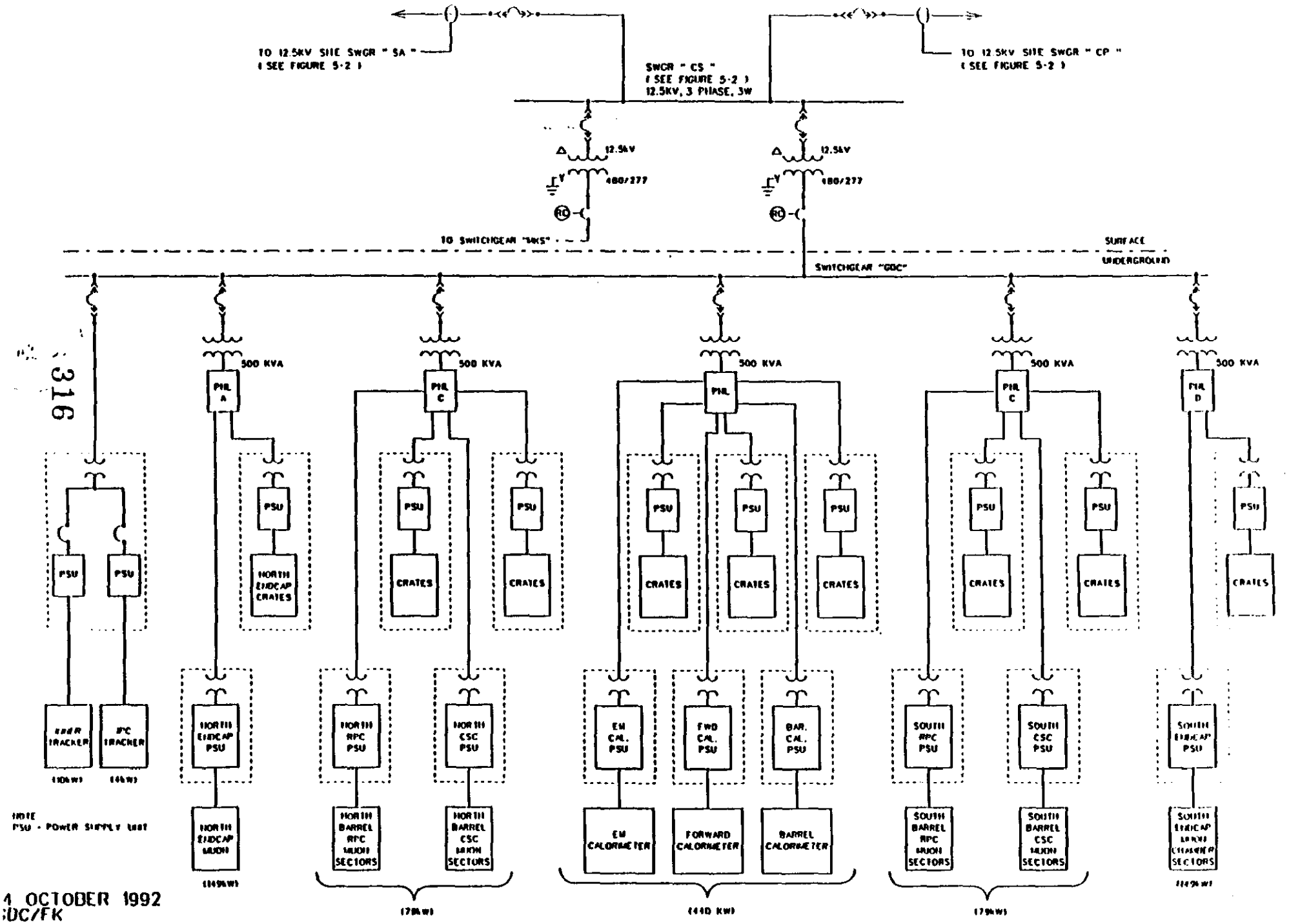


FIGURE 3.5
CABLE ELECTRONICS SHAFT POWER DISTRIBUTION



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:DC/FK

FIGURE 3.4
EXPERIMENTAL HALL ELECTRICAL DISTRIBUTION DIAGRAM

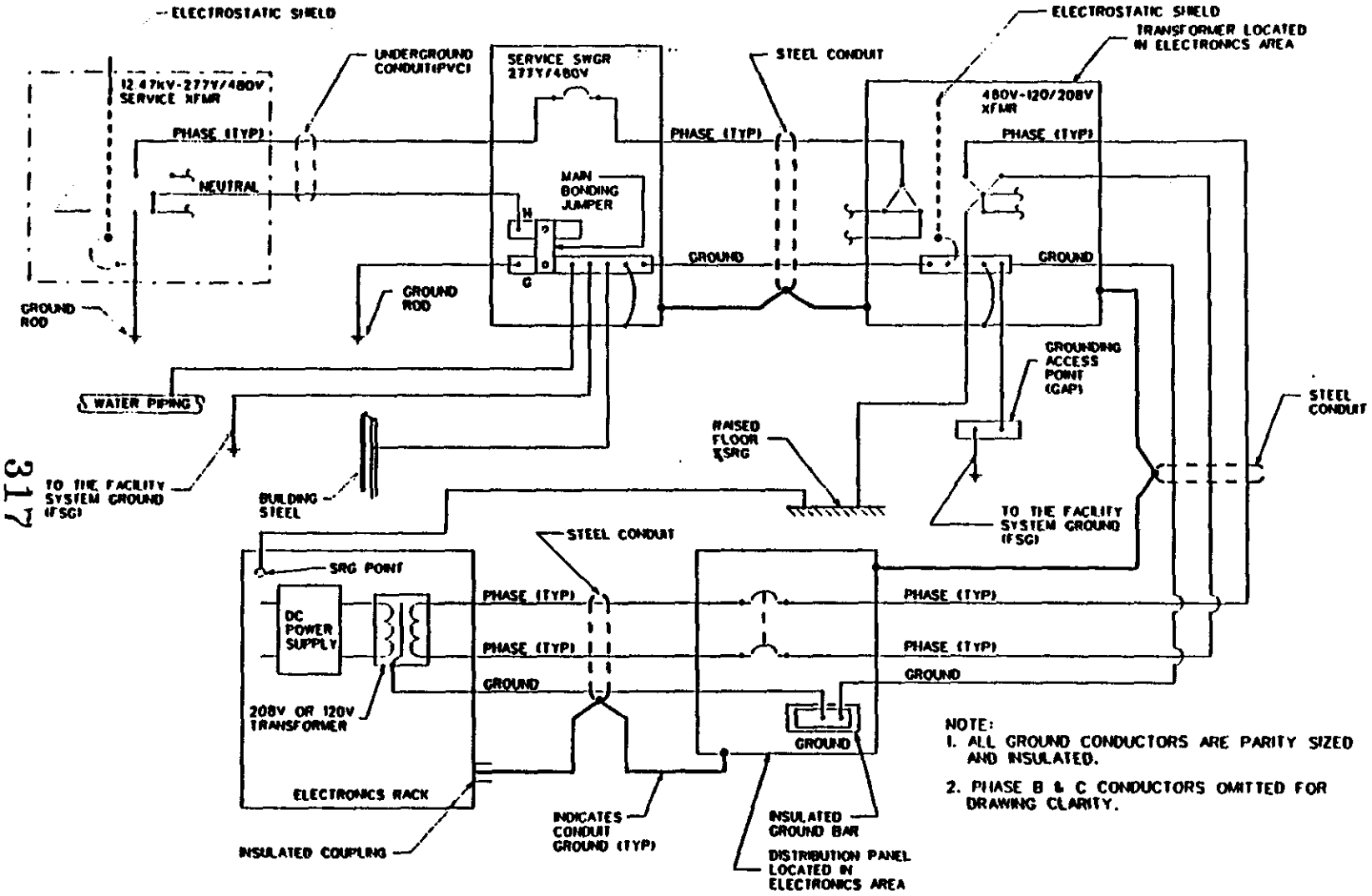
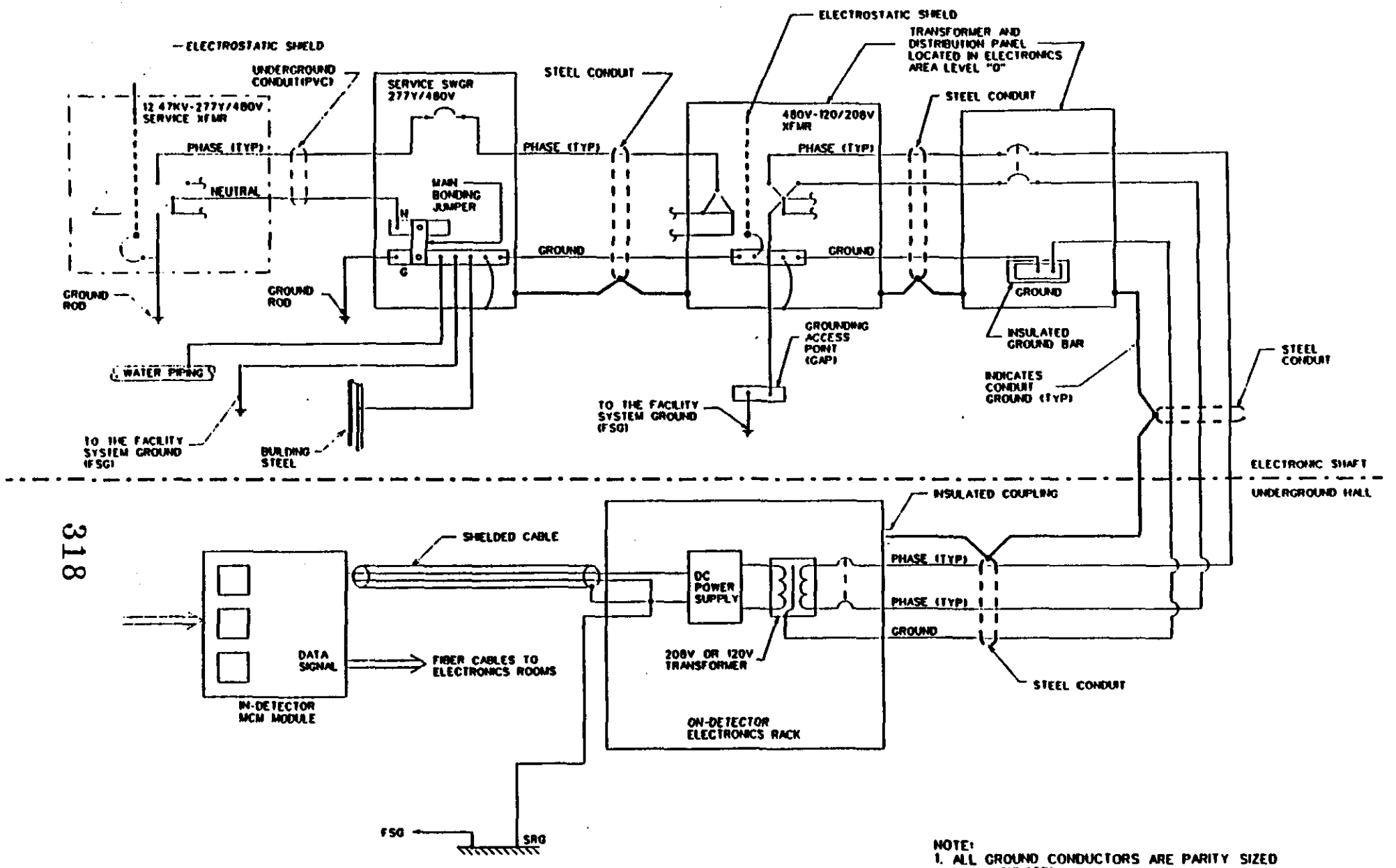


Figure 13.5 ELECTRONICS ROOM GROUNDING DIAGRAM



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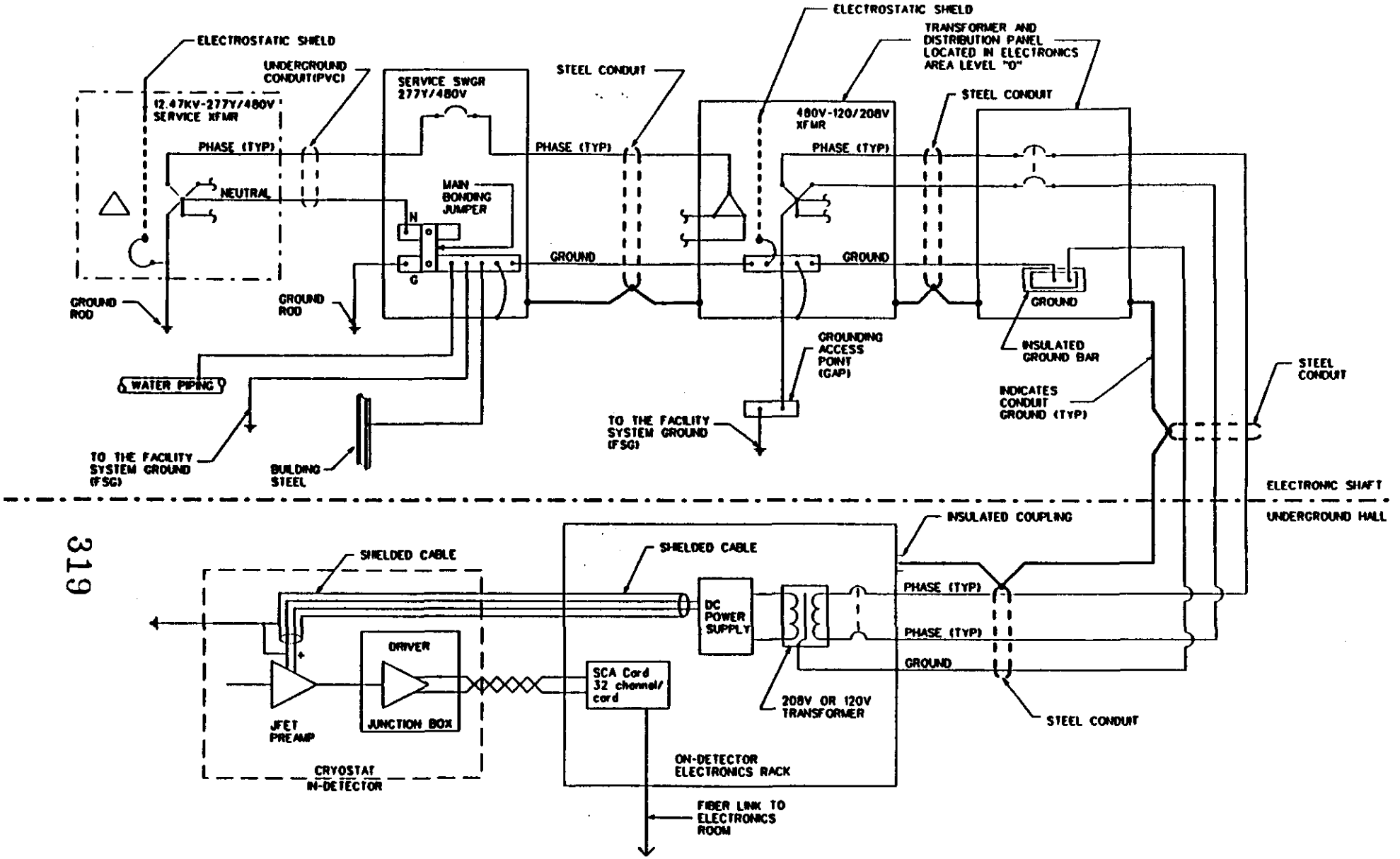
NOTE:
1. ALL GROUND CONDUCTORS ARE PARITY SIZED AND INSULATED.
2. PHASE B & C CONDUCTORS OMITTED FOR DRAWING CLARITY.

8 NOVEMBER 1992
K

gemERG

UNDERGROUND HALL GROUNDING DIAGRAM



NOTE:
1. ALL GROUND CONDUCTORS ARE PARITY SIZED AND INSULATED.
2. PHASE B & C CONDUCTORS OMITTED FOR DRAWING CLARITY.

18 NOVEMBER 1992
FK

gemERG

UNDERGROUND HALL GROUNDING DIAGRAM