FERMILAB-SLIDES-23-351-ETD-STUDENT



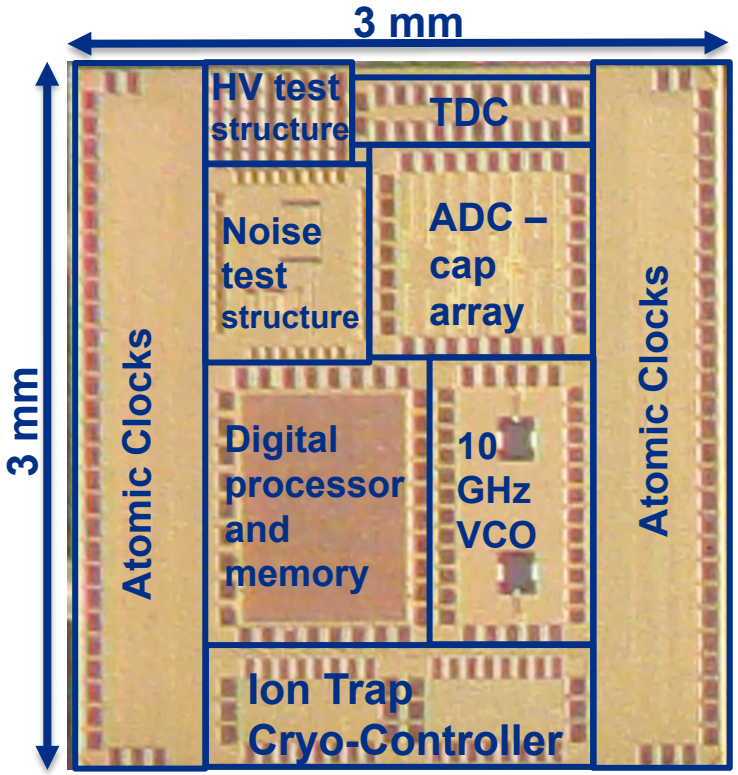
# 22FDX Cryogenic Modeling

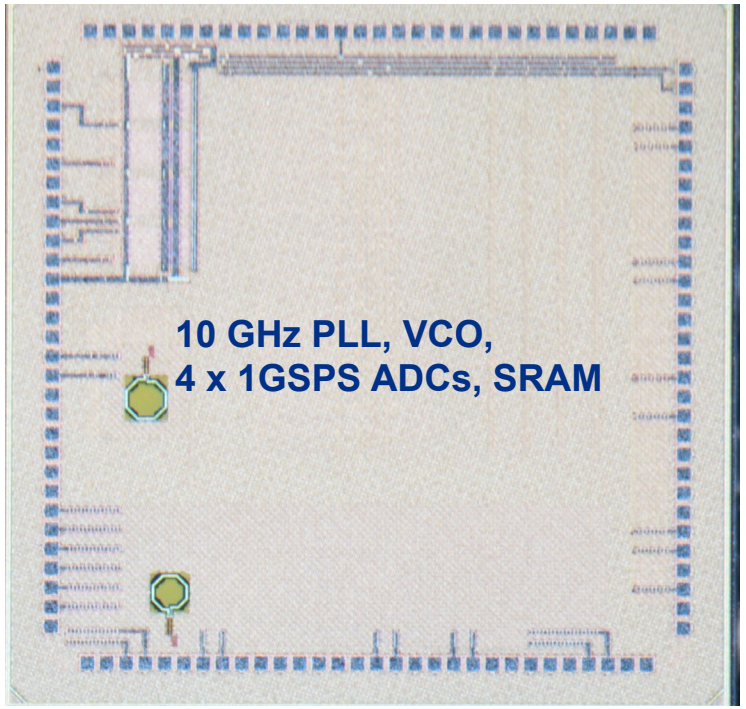
Olivia Seidel[1], Davide Braga[1], Andy Pender[2], Hung-Chi Han[3], Edoardo Charbon[3], Farah Fahim[1]

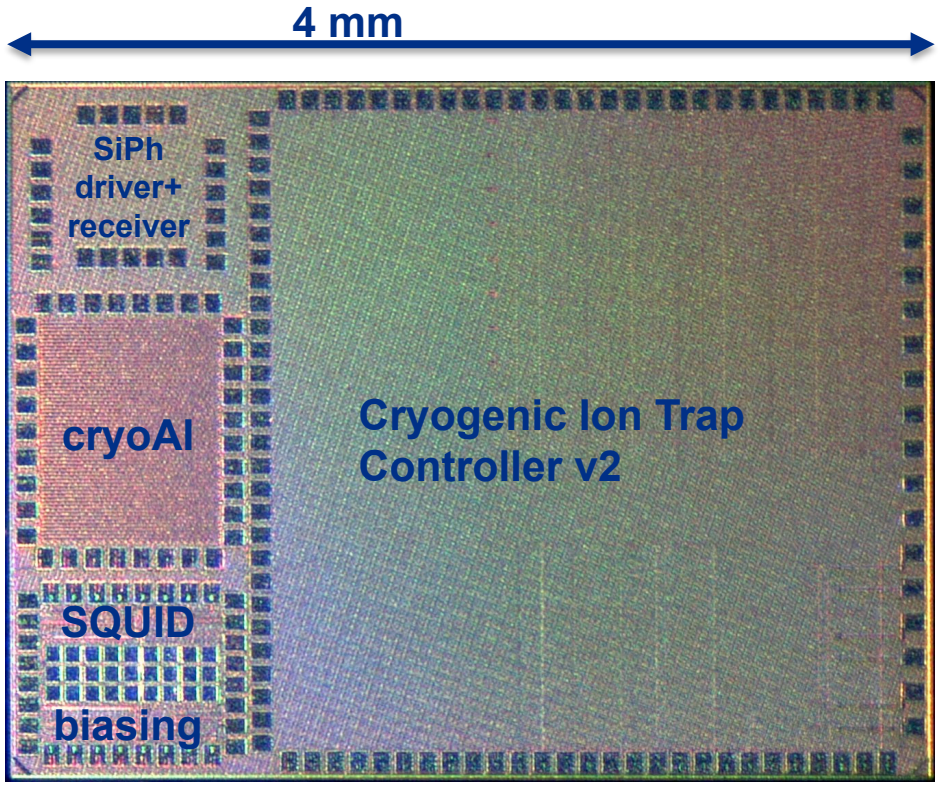
[1] Fermilab, [2] Synopsys, [3] EPFL

CPAD 2023

# 22nm FDSOI cryoChips at Fermilab




- **GF_test chip:** Submission Nov 21; Chips Received April 22: Various designs
- **Michigan :** Submission July 22; Chips Received Nov 22: 10 GHz PLL, VCO, 4 x 1GSPS ADCs, SRAM
- **Cryogenic Ion trap controller:** Submited Jan 2023, received May 2023: 16 channel Ion trap control chip;
- **Si Photonic driver/ receiver**; **cryoAI** ultrafast NN for anomaly detection; **SQUIDDAC**: SLUG_biasing; various level shifter test structures
- **Glebe:** (with Microsoft) 10 GSPS ADC (Dec23)
- **Sunrock:** 32 channel SNSPD () readout with ~ps time tagging (Dec23)

# Overview of Fermilab's 22FDX Cryo-CMOS modeling activities

Fermilab is leading several activities for the cryogenic characterization of 22FDX transistors:

GlobalFoundries™

In-house:

- Measurement and modeling of high voltage devices at 4K (BOXFET, LDMOS)

With EPFL:

EPFL

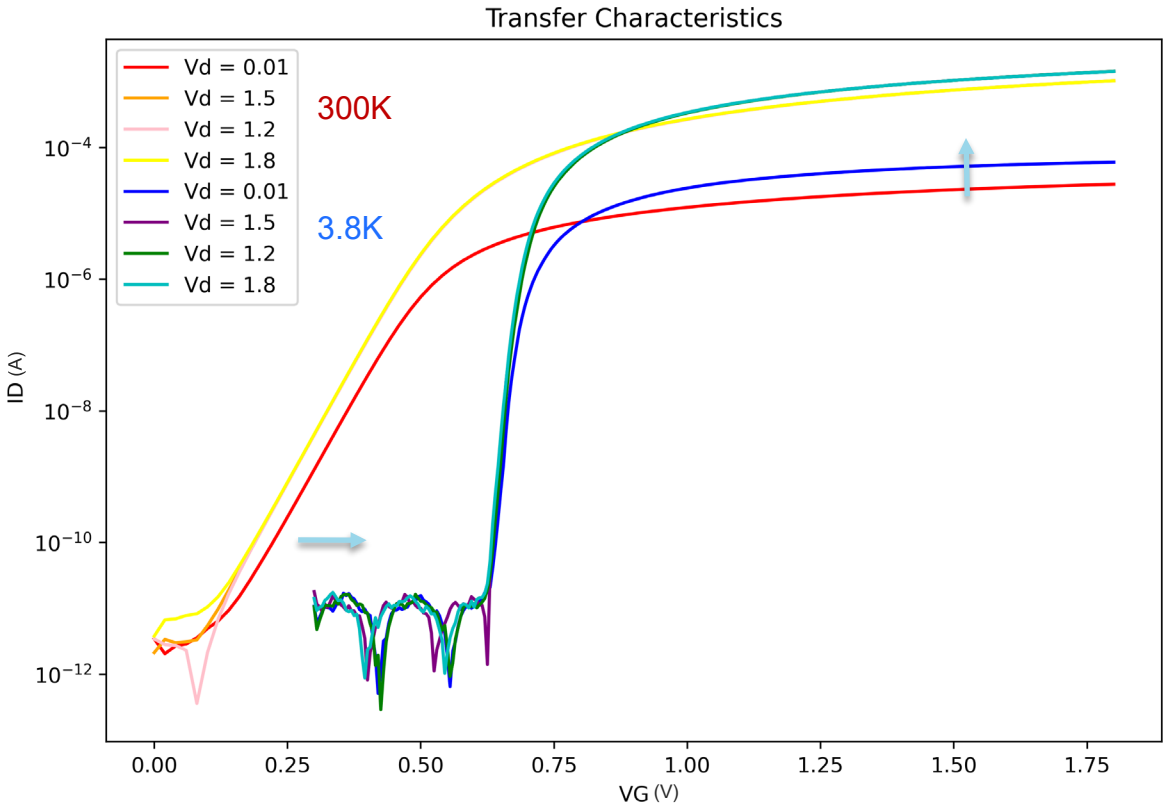
- Measurements of transistors at 4K
- Development of simplified EKV model for analog design
- Low noise test structure measurements

With Synopsys:

- PDK-compatible BSIM-IMG for 4K

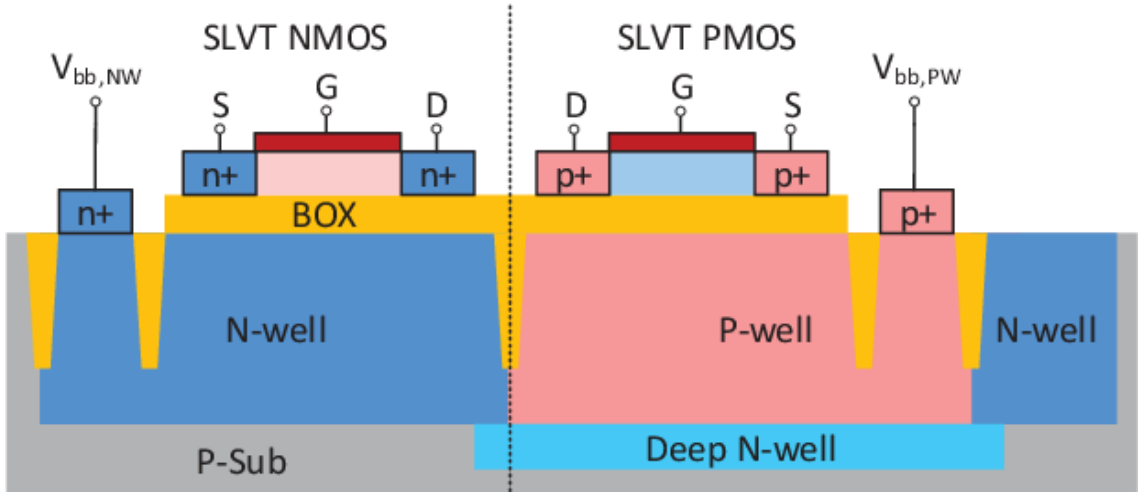
SYNOPSYS®
Silicon to Software™

# FDSOI for RF/Analog Design




IdVg for eglvt nfet l=0.2 um w=2um

- **Threshold Voltage increases** (due to substrate freezing)
- Availability of a **"back-gate"** in FDSOI technologies to lower the threshold and counter cryogenic increase
- Confined electrons in an undoped channel = less leakage, lower power, higher voltage, faster switching




[1]



Fermilab

# Behavior Changes at Cryogenic Temperatures

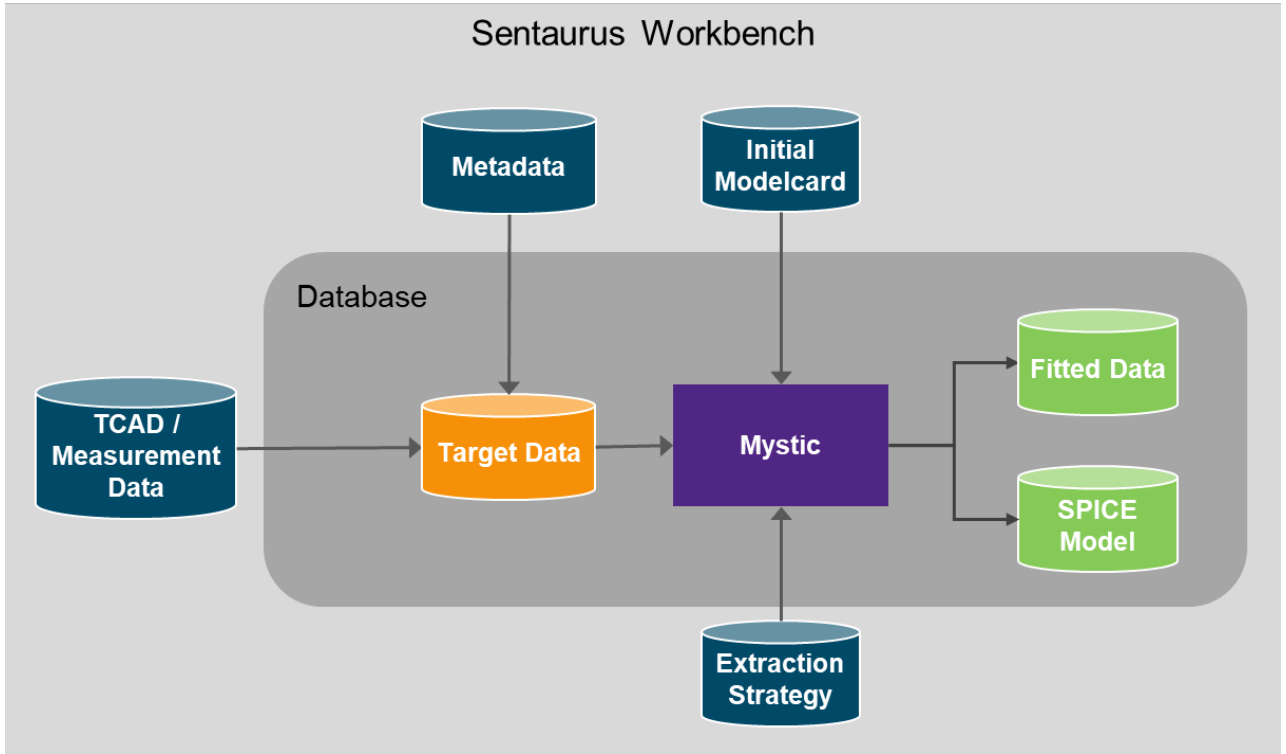
- Electron Mobility  [2]
- Phonon scattering, coulomb scattering [3]
- Capacitance effects [4]
- Resistance due to self-heating [5]
- Source drain extension resistance [6]
- Velocity saturation [7][8]
- Work function [7][9]
- Subthreshold slope [10]
- Drain induced barrier lowering [11]
- …etc

# Measurement data

- **300K, 3.8K** for various front gate and source/drain biases
- Gate **lengths**: 0.07um, 0.2 um, 2um
- Gate **widths** for each length: 0.16um, 0.5um, 2um
- For each IdVg we have Vd=0.01, 1.2, 1.5, 1.8V
- Starting with **eglvt** flavor

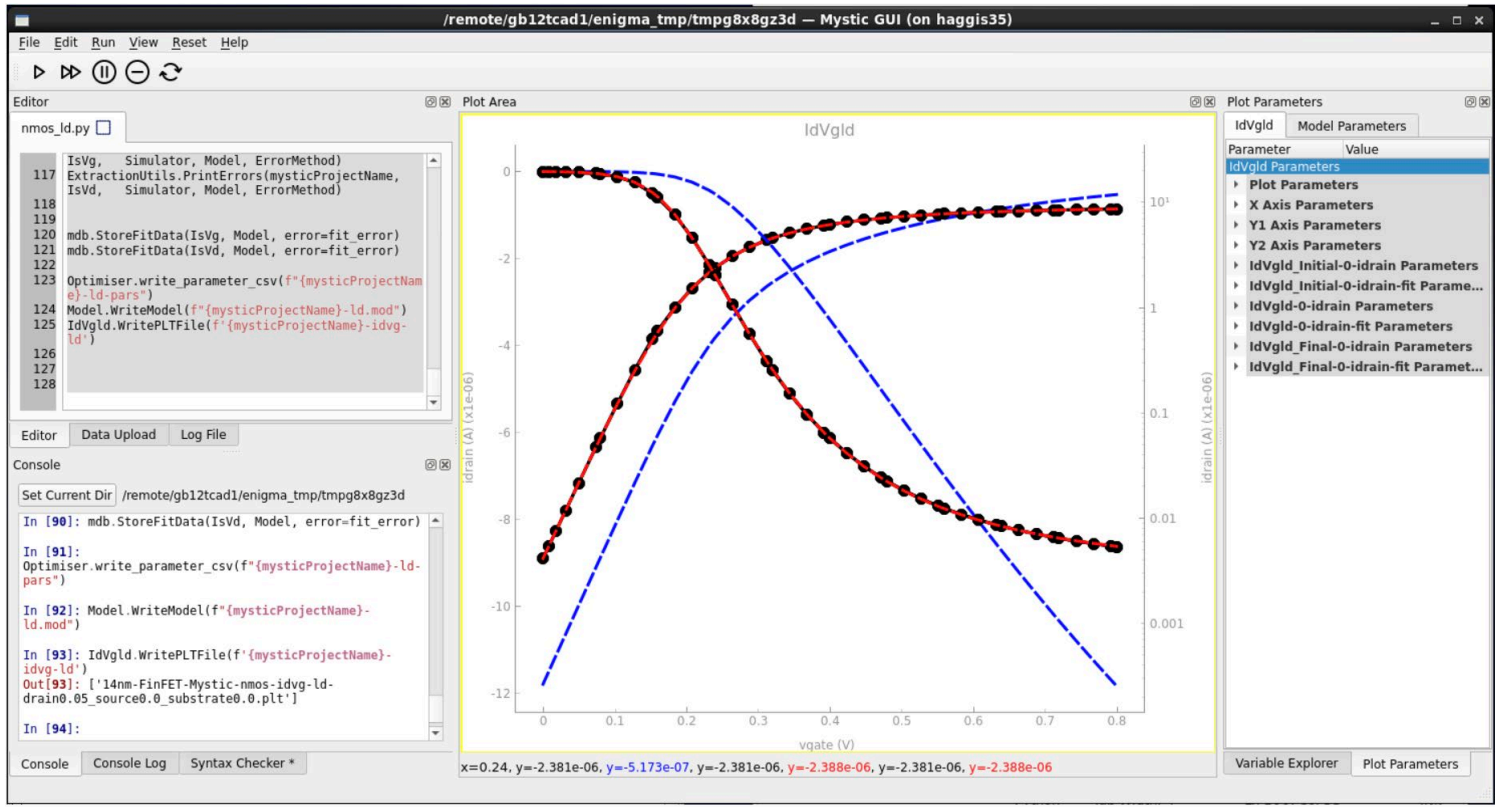
# Mystic Software

- Synopsys SPICE model extraction tool for creating **automated parameter extraction** methodologies for semiconductor applications
- Integrated in the Synopsys Sentaurus Workbench TCAD platform
- Use **Synopsys Primesim HSPICE** as a simulation backend



# Mystic Software

- Features an interactive GUI for real time extraction analysis, a custom **Python scripting environment** for flexible scripting and an extensive **optimization library** for finding the best parameter set for the selected SPICE model

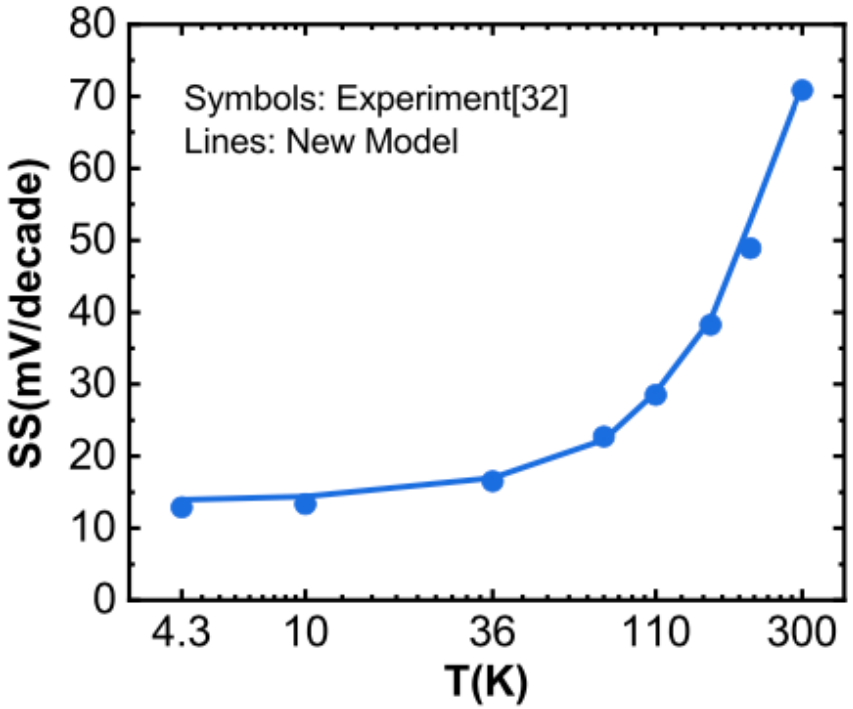





Fermilab

# Our Model Approach

- Take the 22nm PDK provided by global foundries for these devices and **re-extract** the parameters we think will change at cryo
- Keep a **basis in physics** by setting reasonable parameter ranges based on literature when applicable
- Change the input pdk:
  - BSIM-IMG 102.8 doesn't include effects like subthreshold slope saturation [14], we need to model that saturation by setting **temp=tnom** to the value where our **subthreshold slope saturates**
- **Isothermal** model
- We will then place these extracted values back into the PDK



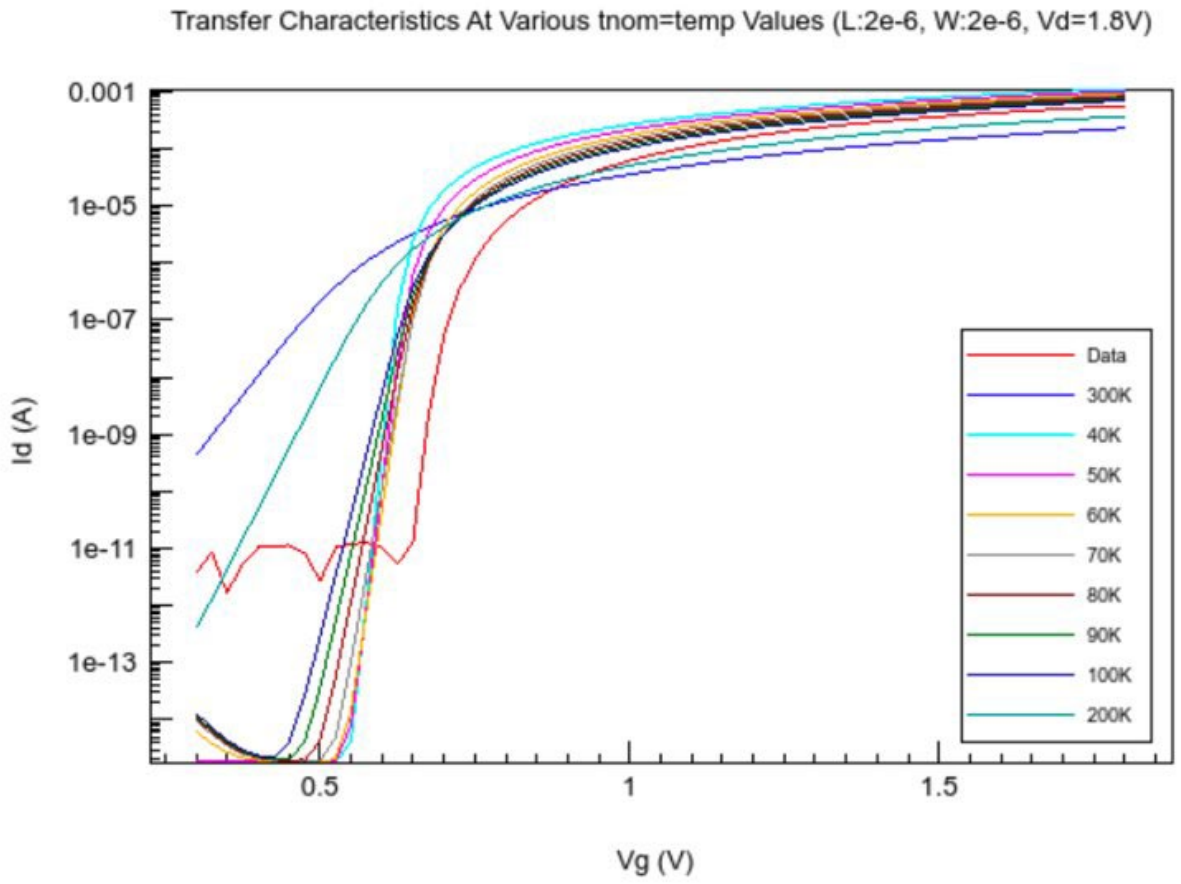

Subthreshold Slope Saturation as a function of Temperature [14]

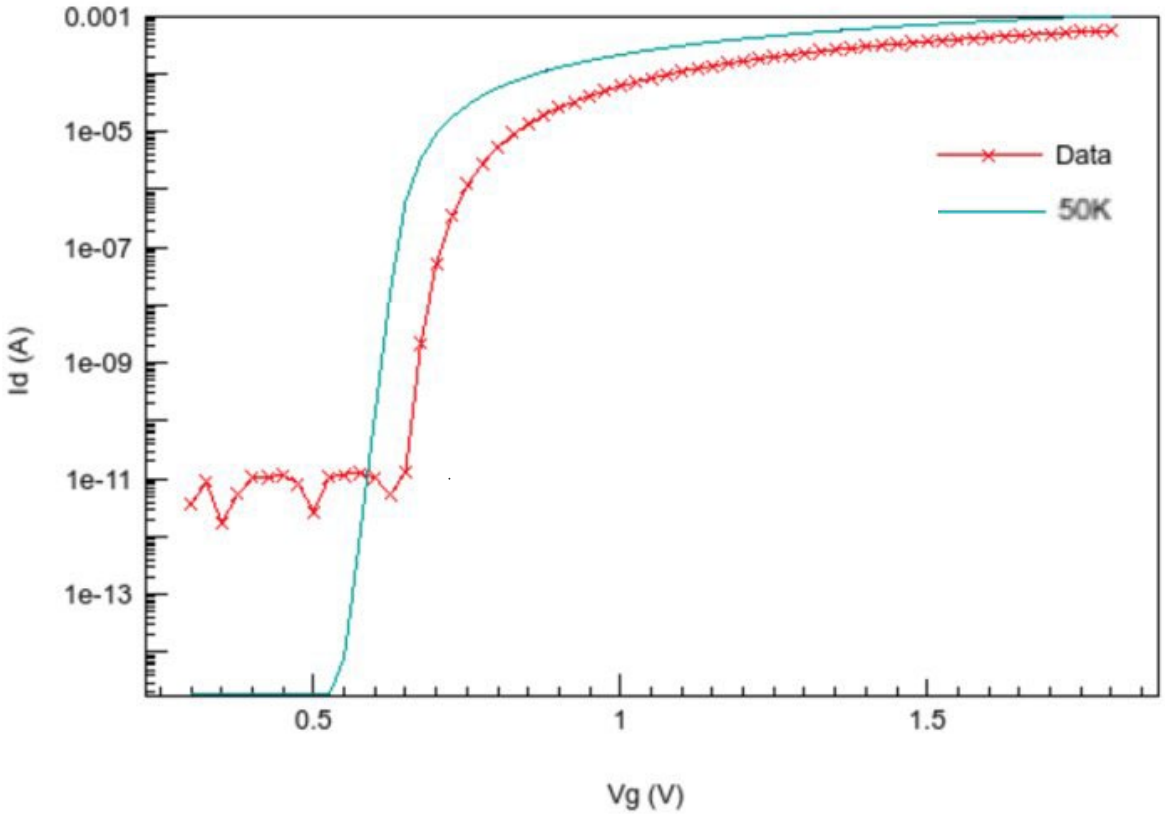


Fermilab

# Setting TNOM Value

Adjust temp=tnom and find where the subthreshold slope best fits:






Fermilab

# BSIM-IMG Recommended Strategy as a Basis

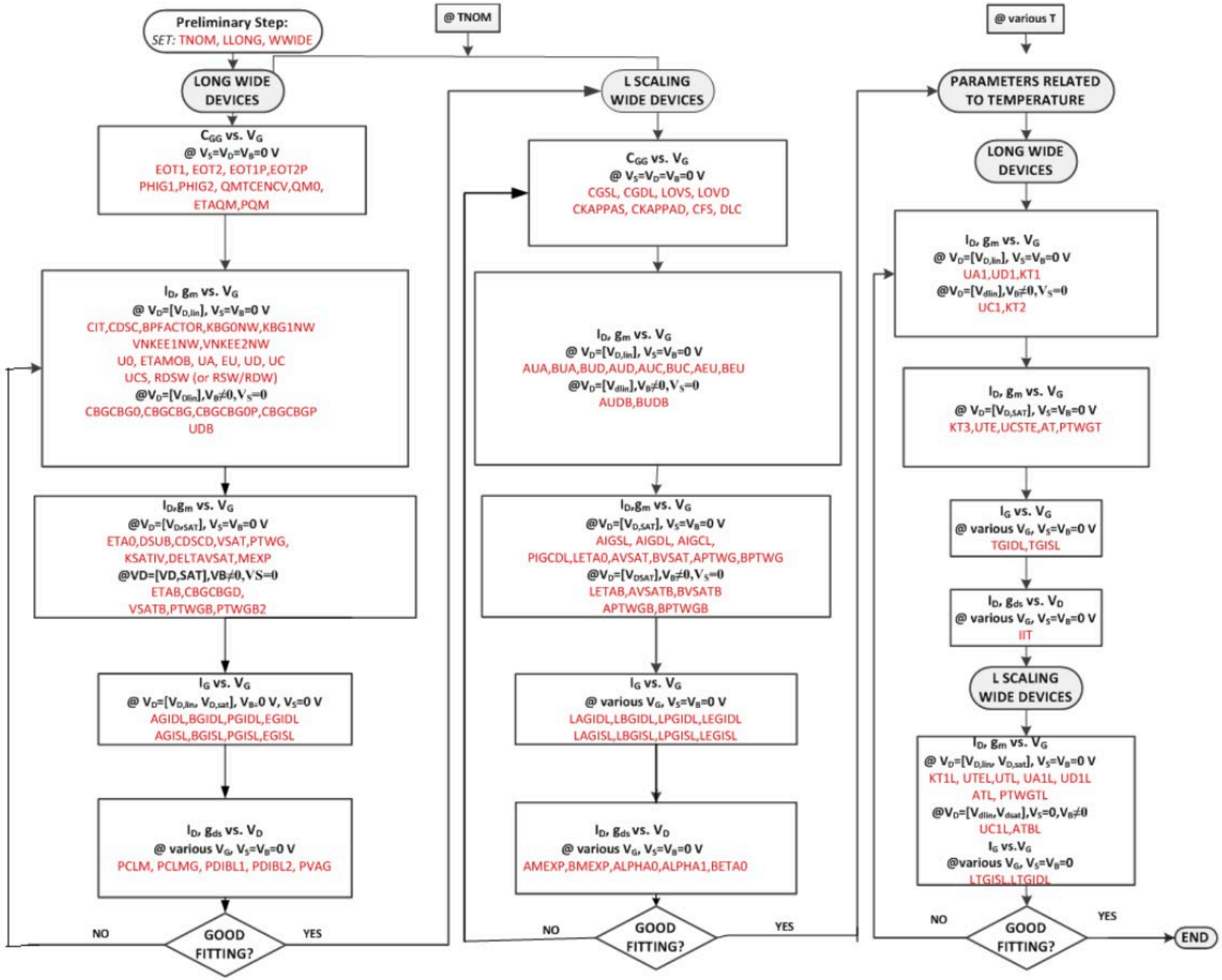



Figure 13: Parameters Extraction Procedure in BSIM-IMG Model.

# Building an Extraction Strategy

- Find **groups of isolated parameters** that influence each other but not the rest of the model and put in **“stages”**
- Within each group find subgroups or single parameters that impact **various target regions** of the curves and make a **series of steps**
- **Loop** until you get a good fit. If you never find a good fit, something is wrong with the strategy or parameter set and some changes need to be made

Example:

u0,ua,ud,rdw, rsw -> IDVG
Low drain

u0,ua,ud --> elbow/threshold voltage region

# Extraction Strategy

**Stage 1:** Extract **low drain** parameters for long/wide device

**Stage 2:** Extract **high drain** parameters for long/wide device

**Stage 3:** Extract **width** dependent parameters for long device at various widths

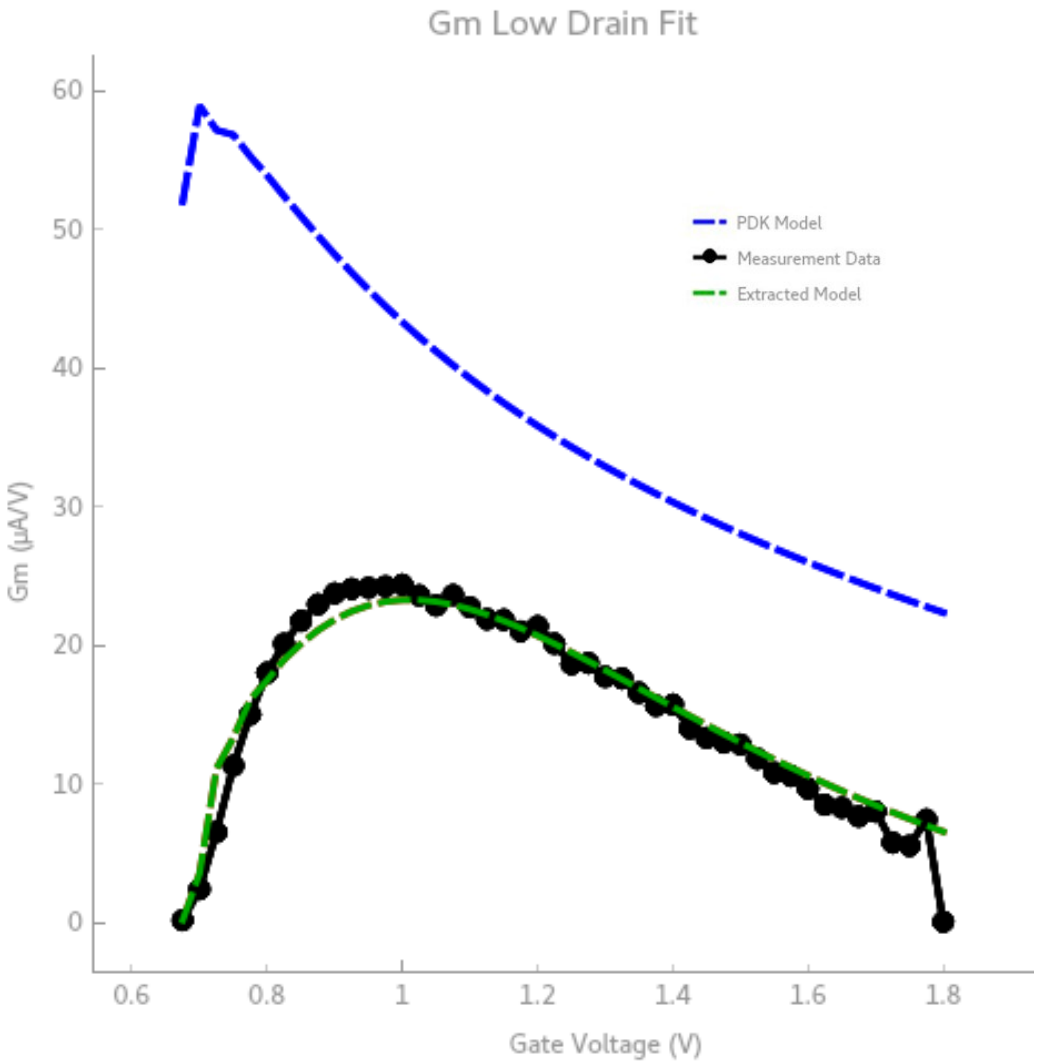
**Stage 4:** Extract **Low Drain length** dependent parameters

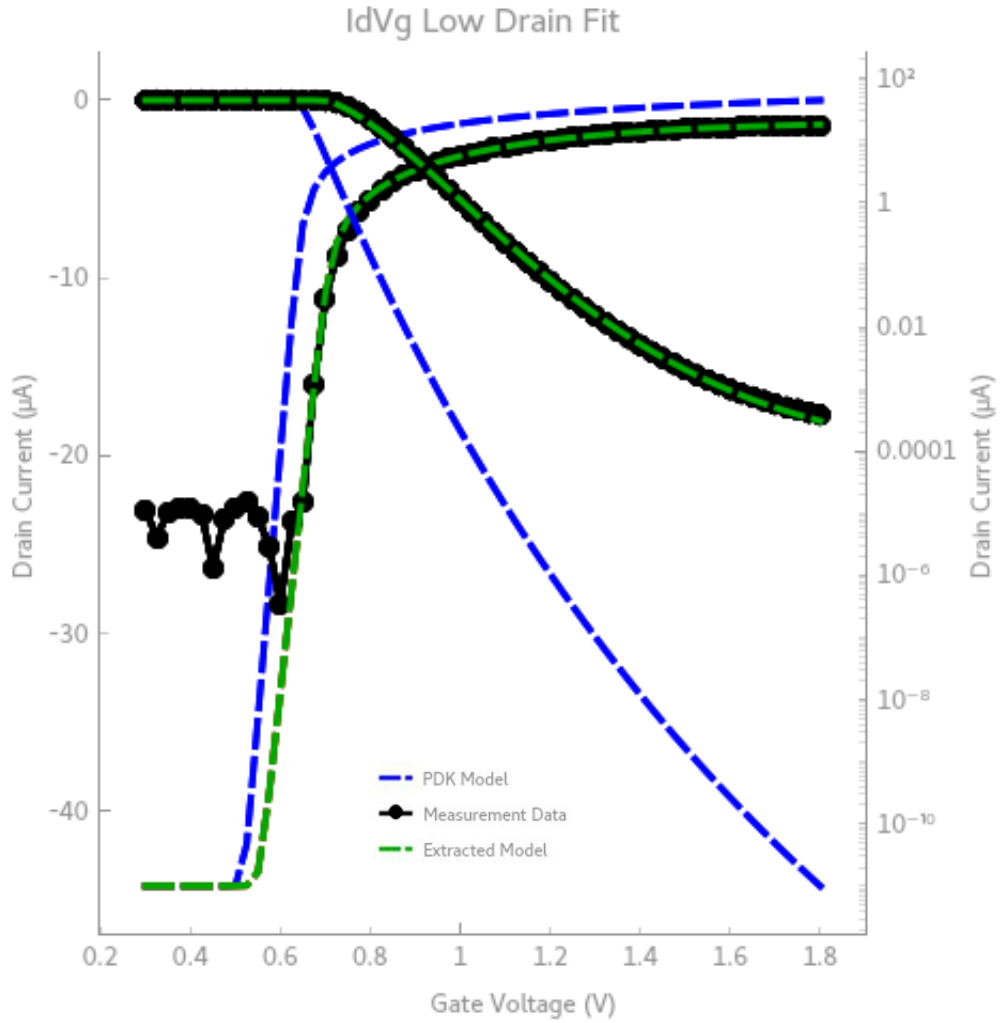
**Stage 5:** Extract **High Drain length** dependent parameters

**Stage 6:** Extract **Back gate** parameters

**Stage 7:** Extract **corner** cases (short length/short width)

# Stage 1 Low Drain extraction **PDK Model (with temp=tnom=50K) vs Extracted Model:**



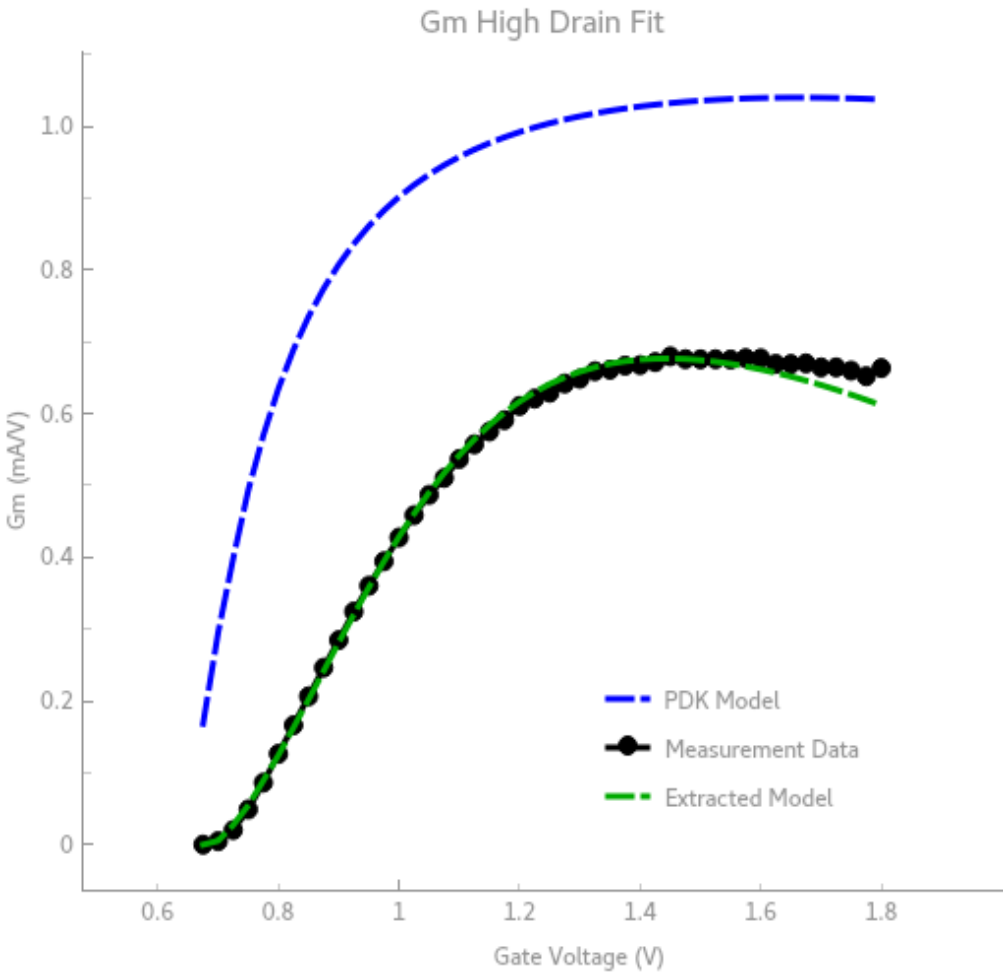



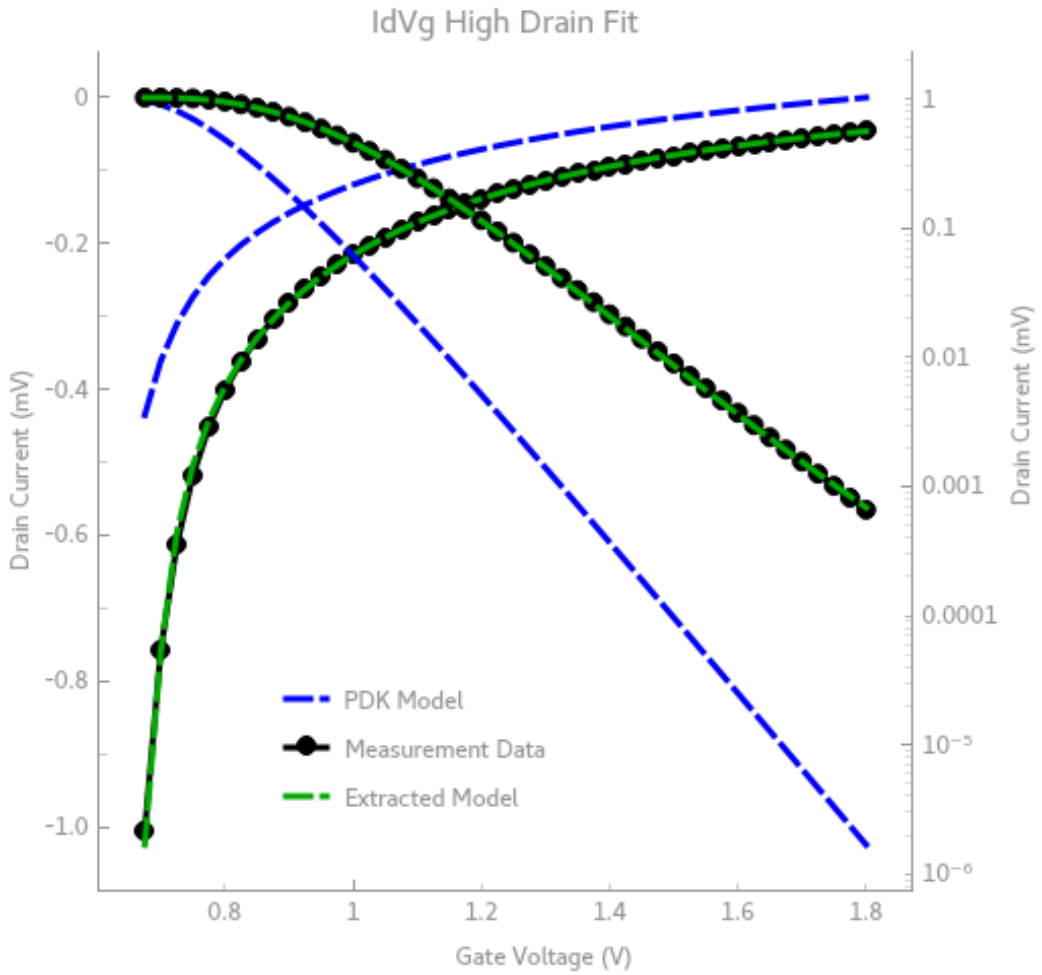



Fermilab

# Stage 2 High Drain extraction

## PDK Model (with temp=tnom=50K) vs Extracted Model:



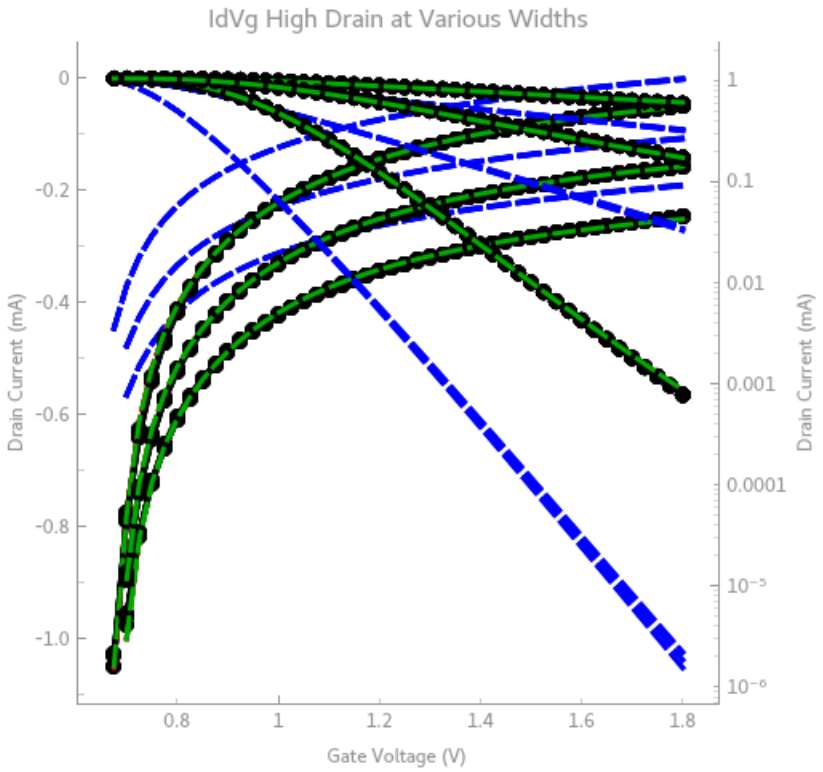



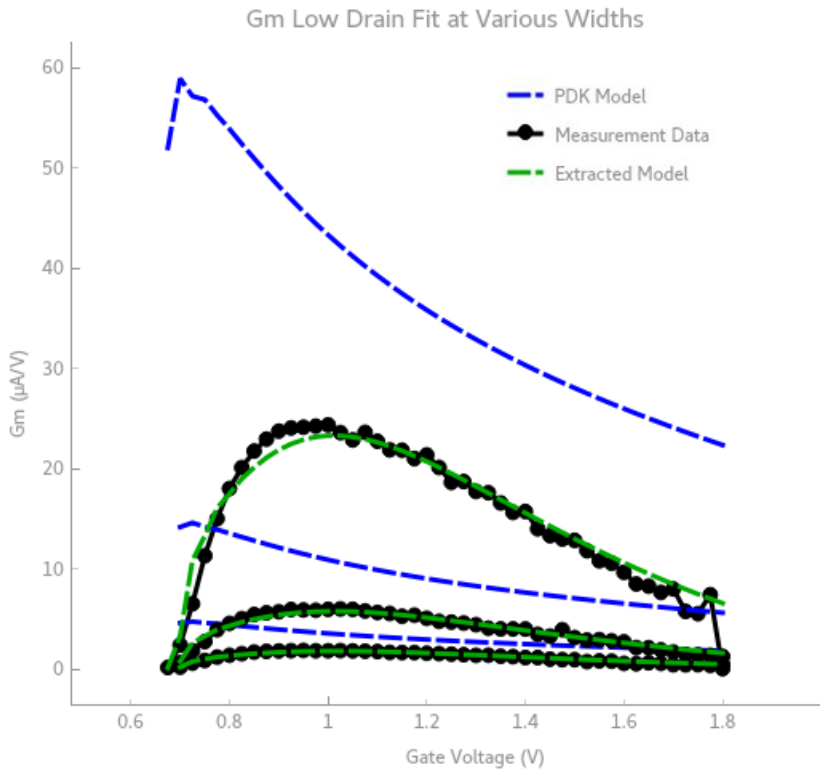


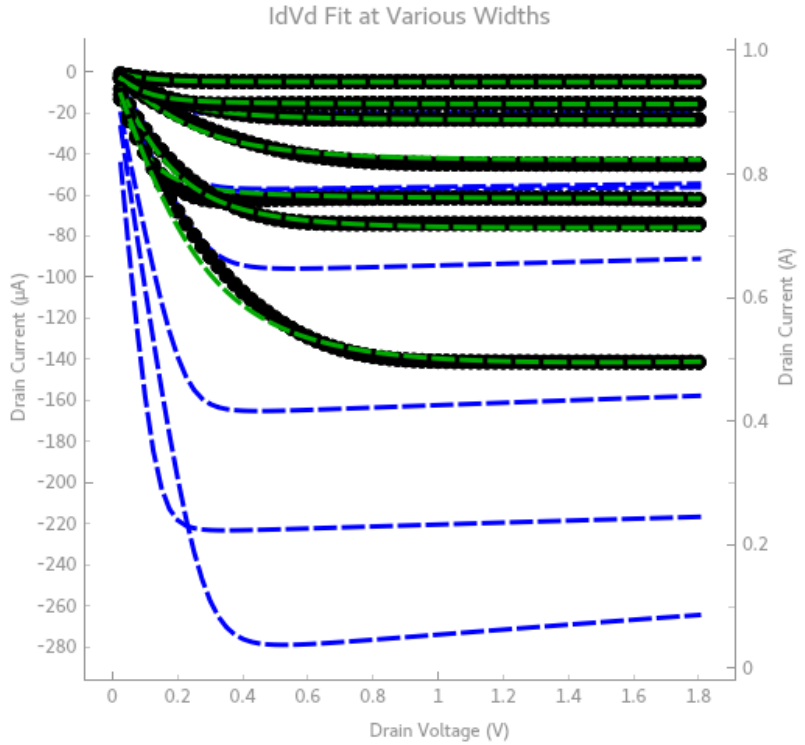

Fermilab

# Stage 3 Width extraction

## PDK Model (with temp=tnom=50K) vs Extracted Model:



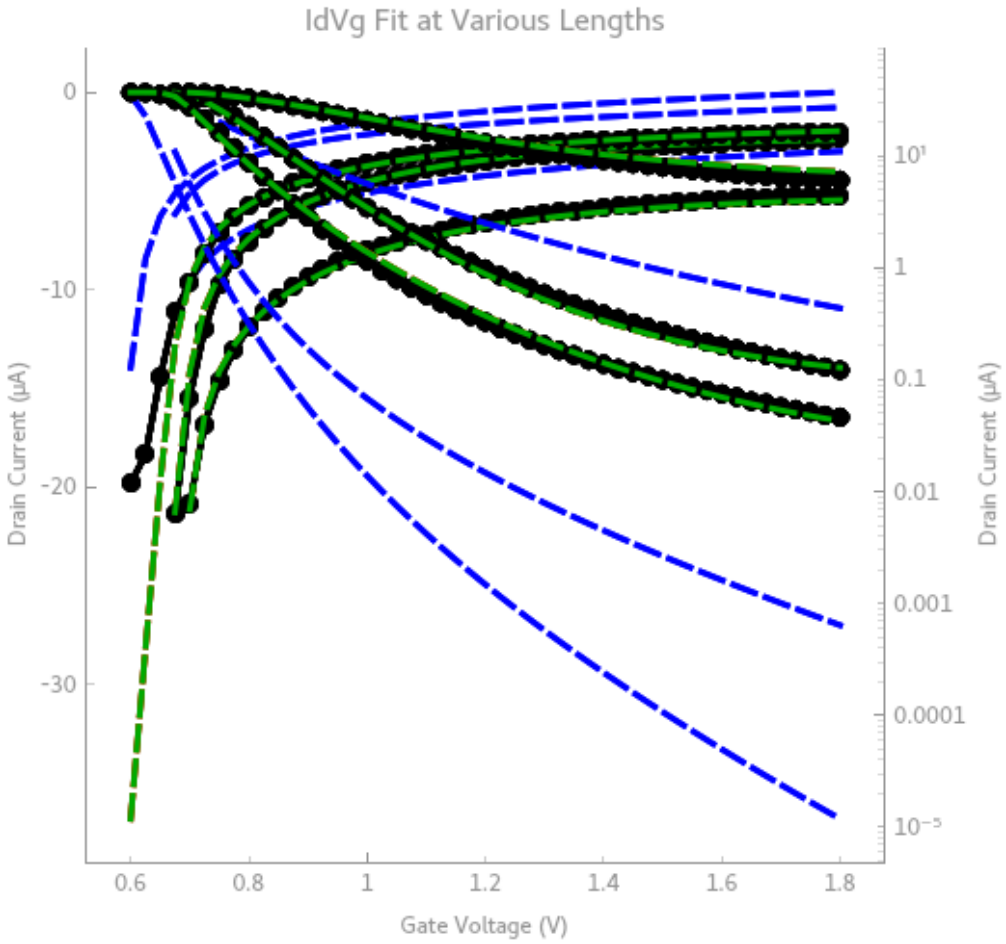


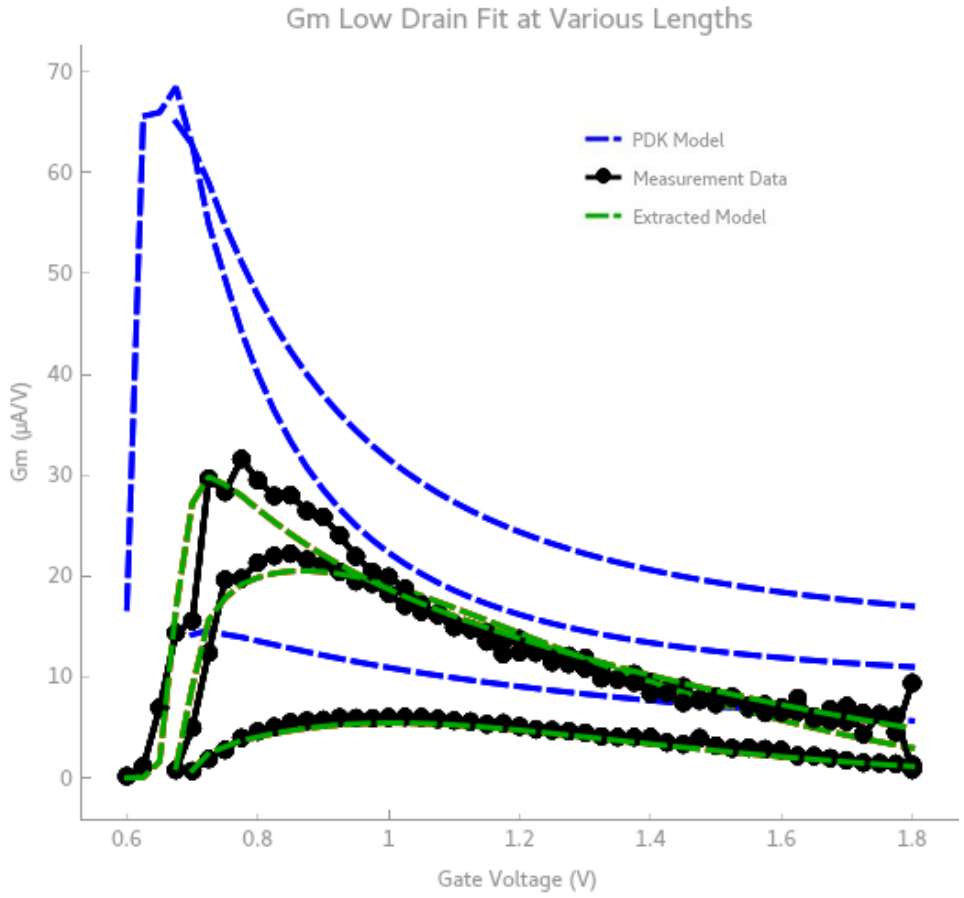

Fermilab

# Stage 4

Low Drain Length extraction

## PDK Model (with temp=tnom=50K) vs Extracted Model:



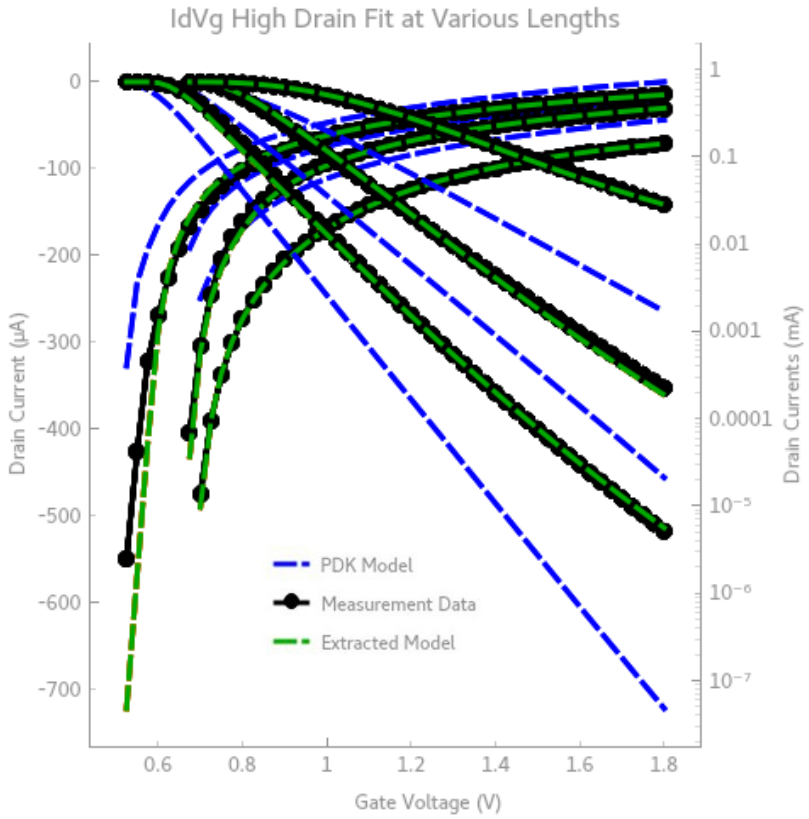



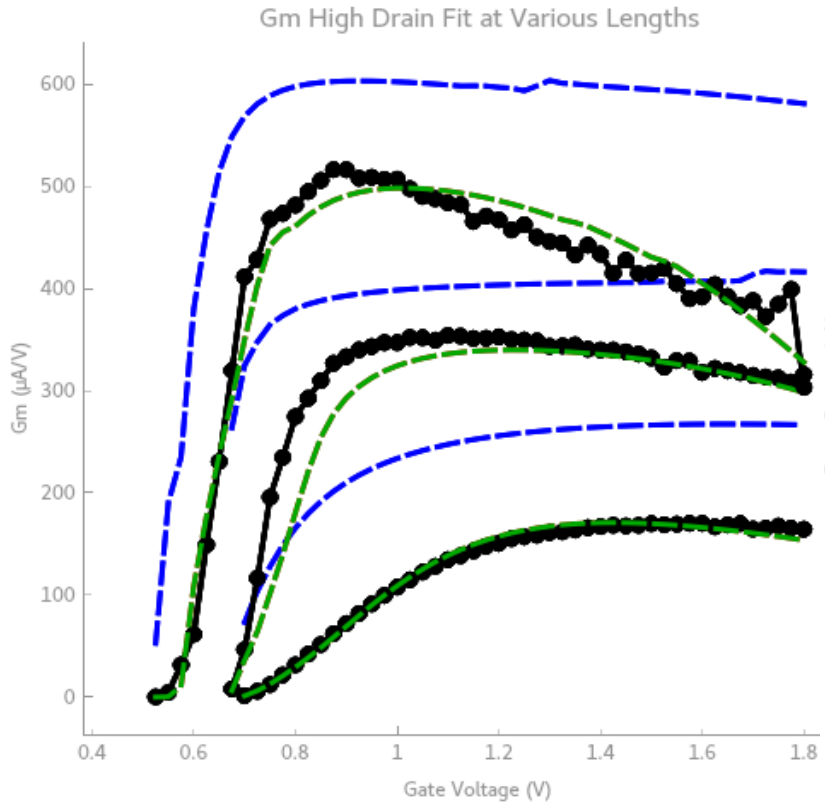


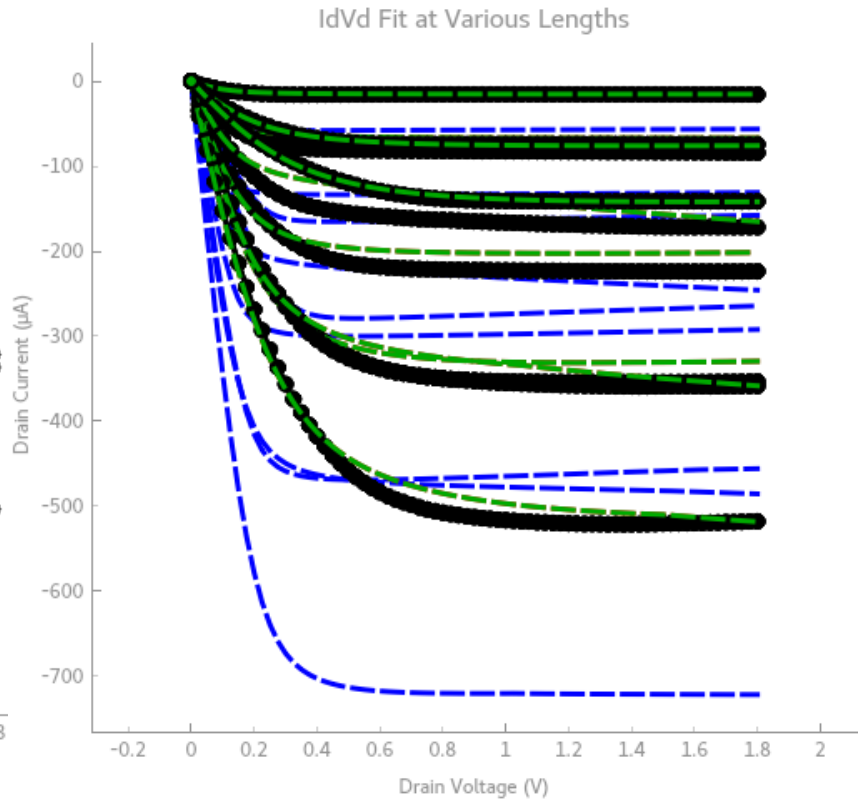

Fermilab

# Stage 5 High Drain Length extraction

## PDK Model (with temp=tnom=50K) vs Extracted Model:



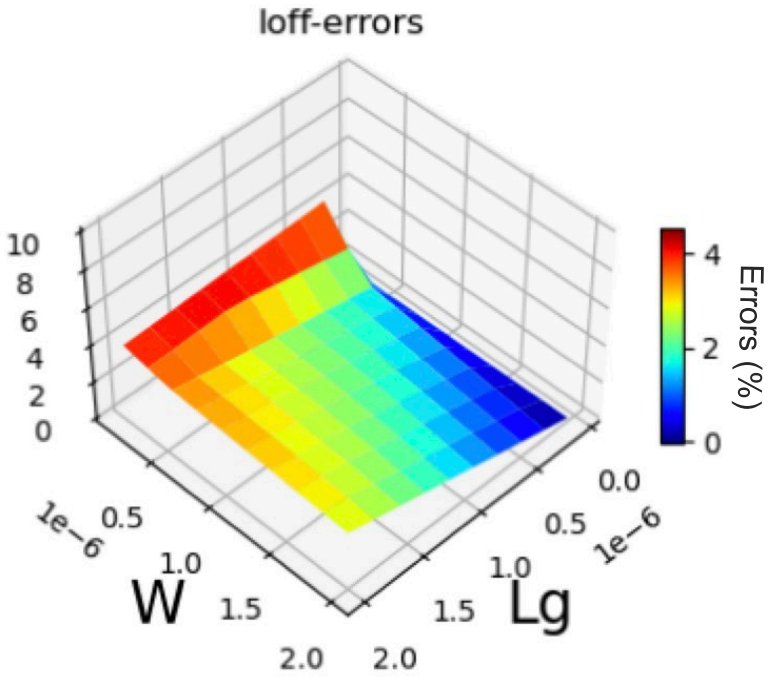



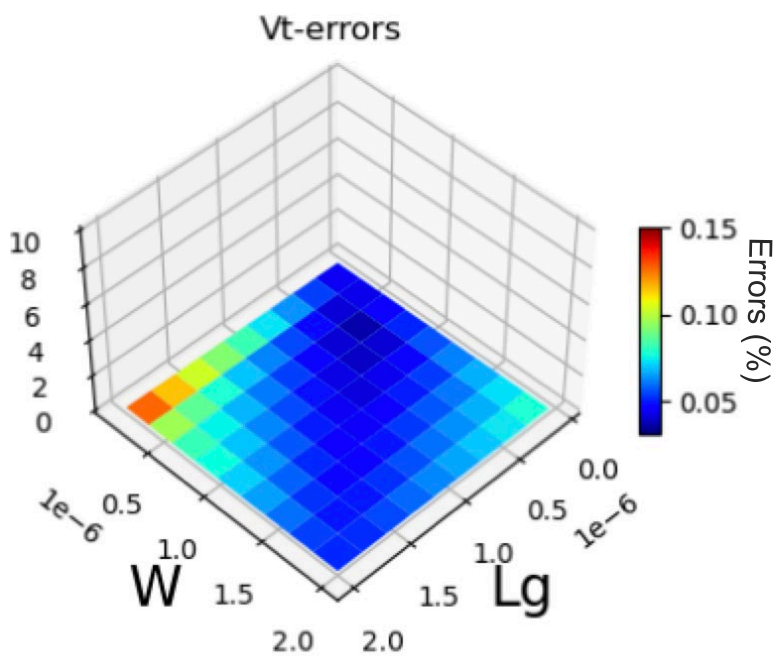


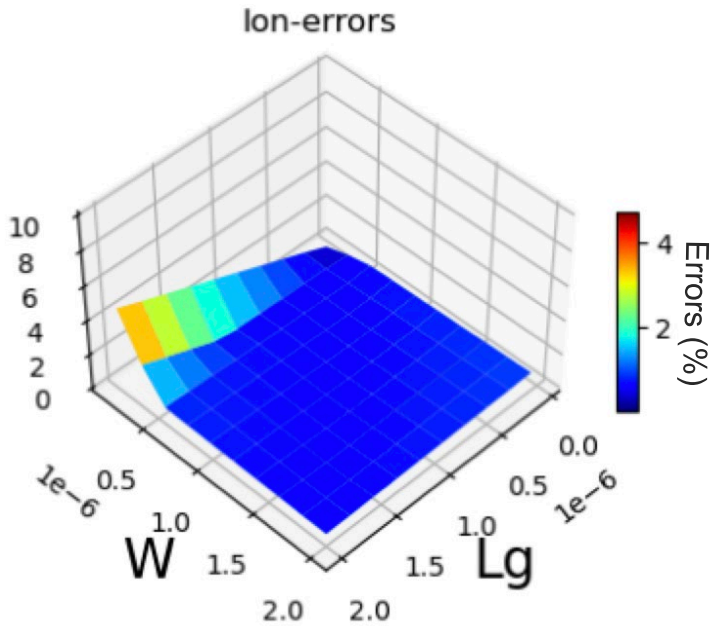

Fermilab

# Errors across Figures of Merit for all Lengths and Widths

Found by taking the percentage error between data simulated using the extracted model and the measurement data:



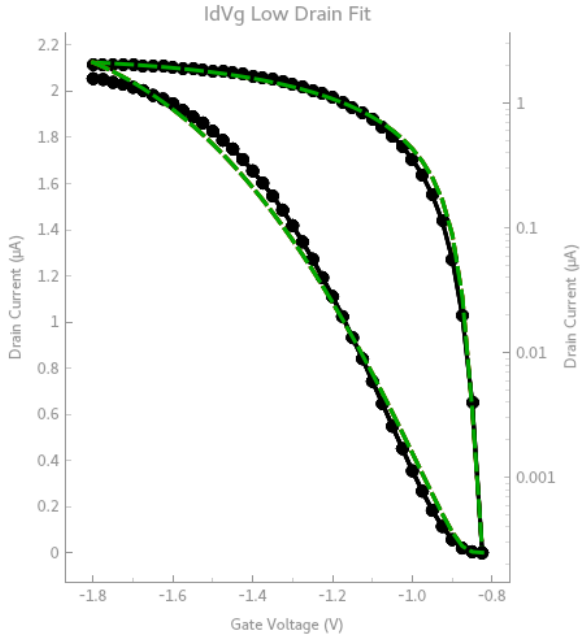



Fermilab

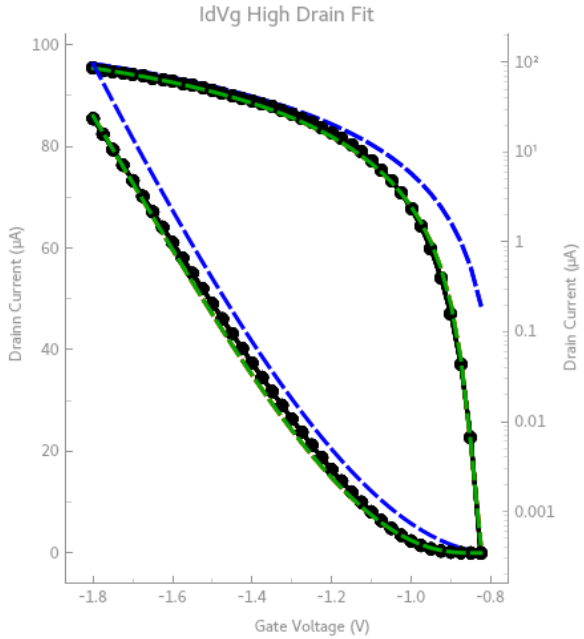
# PFETs

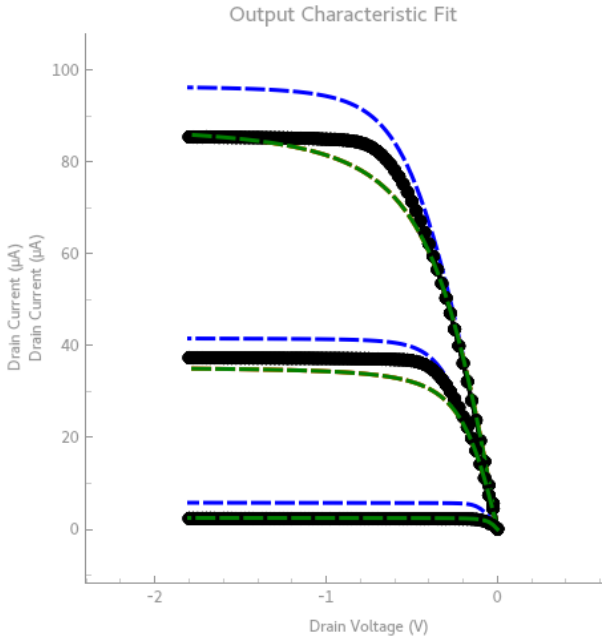
PDK Model
Measurement Data
Extracted Model

Stage 1:

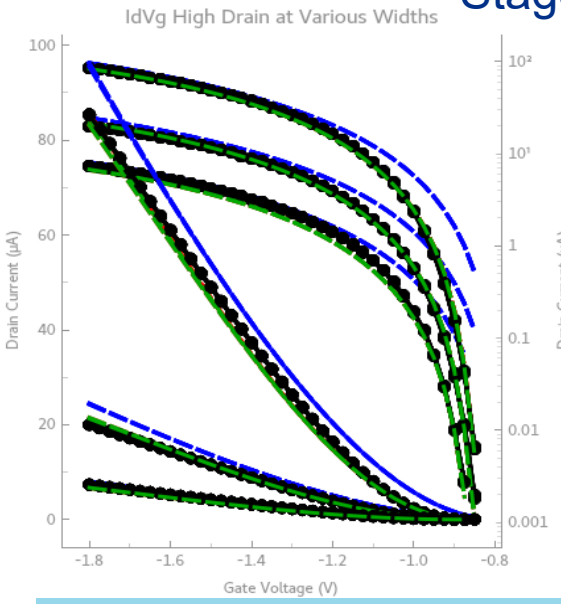


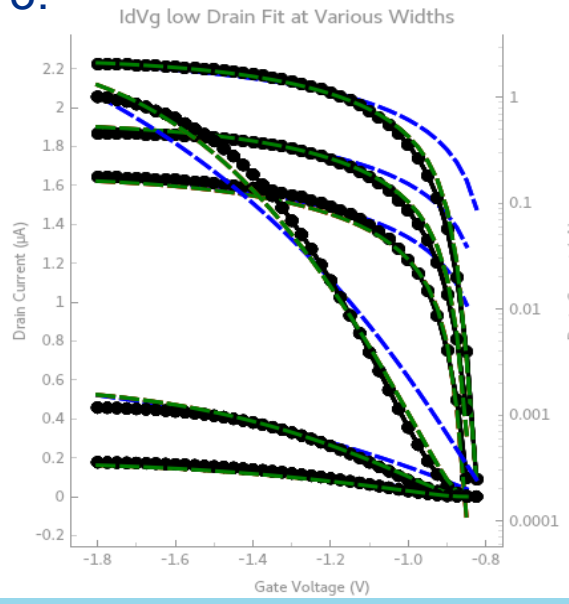

Stage 2:



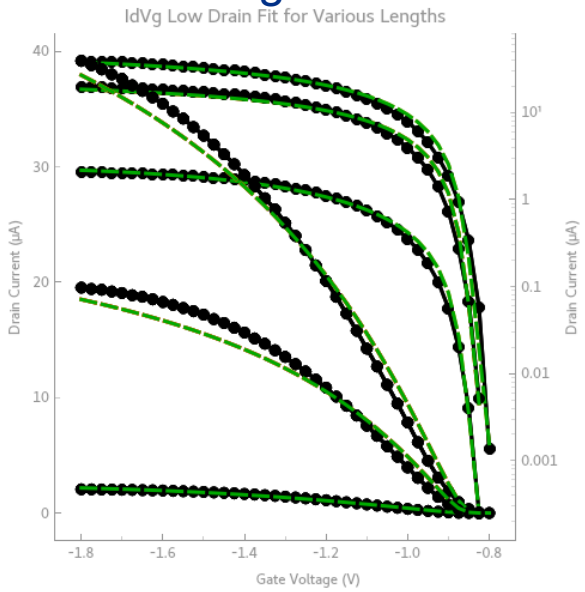




Stage 3:

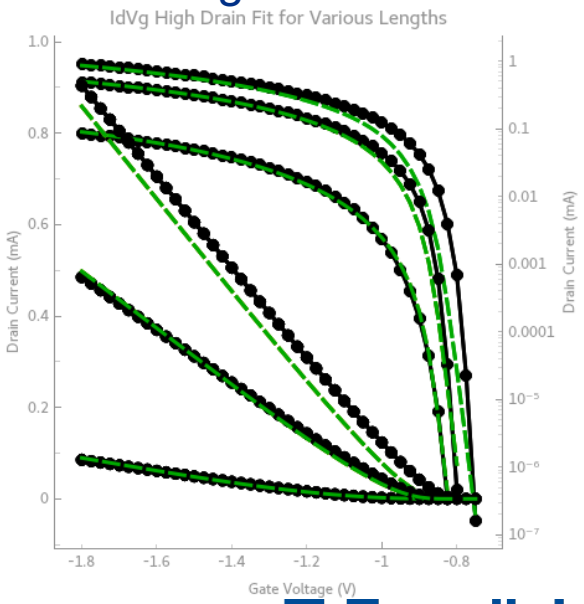



Stage 4:




Stage 5:






Fermilab

# Future work

**Complete 4K PDK-compatible models** for thin oxide devices and HV devices

Cryogenic **noise measurements**

Develop 4K **timing libraries** for standard cell library

Cryogenic radiation testing at Fermilab
- Evaluate radiation hardness at cryo
- If sufficient, create 4K radiation compact models and timing libraries

Quantify cryogenic **measurement error**

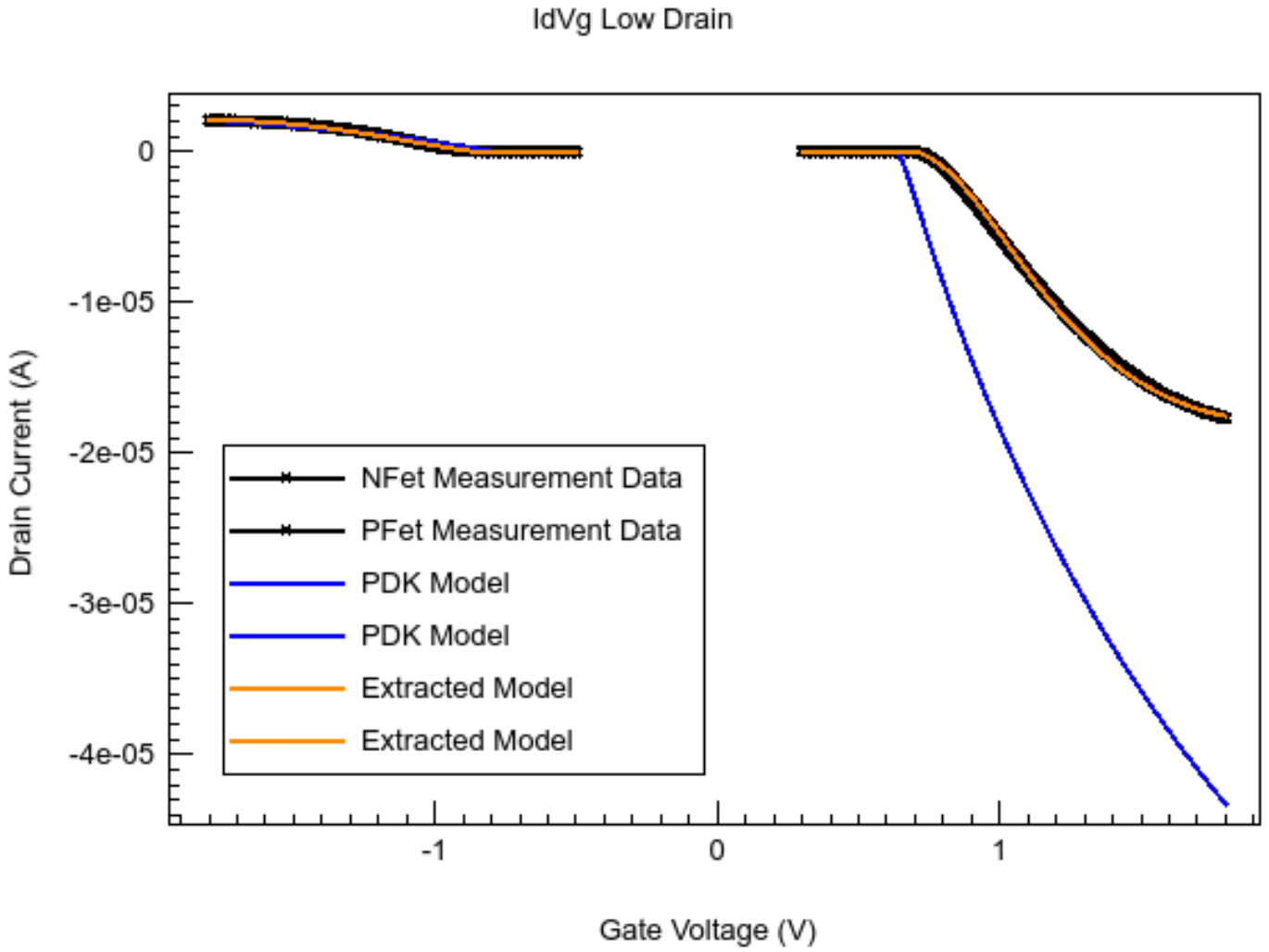
**AI/ML** based PDK development

Work supported by the U.S. Department of Energy, Office of Science (Microelectronics Codesign) and Fermilab LDRD.

# Works Cited

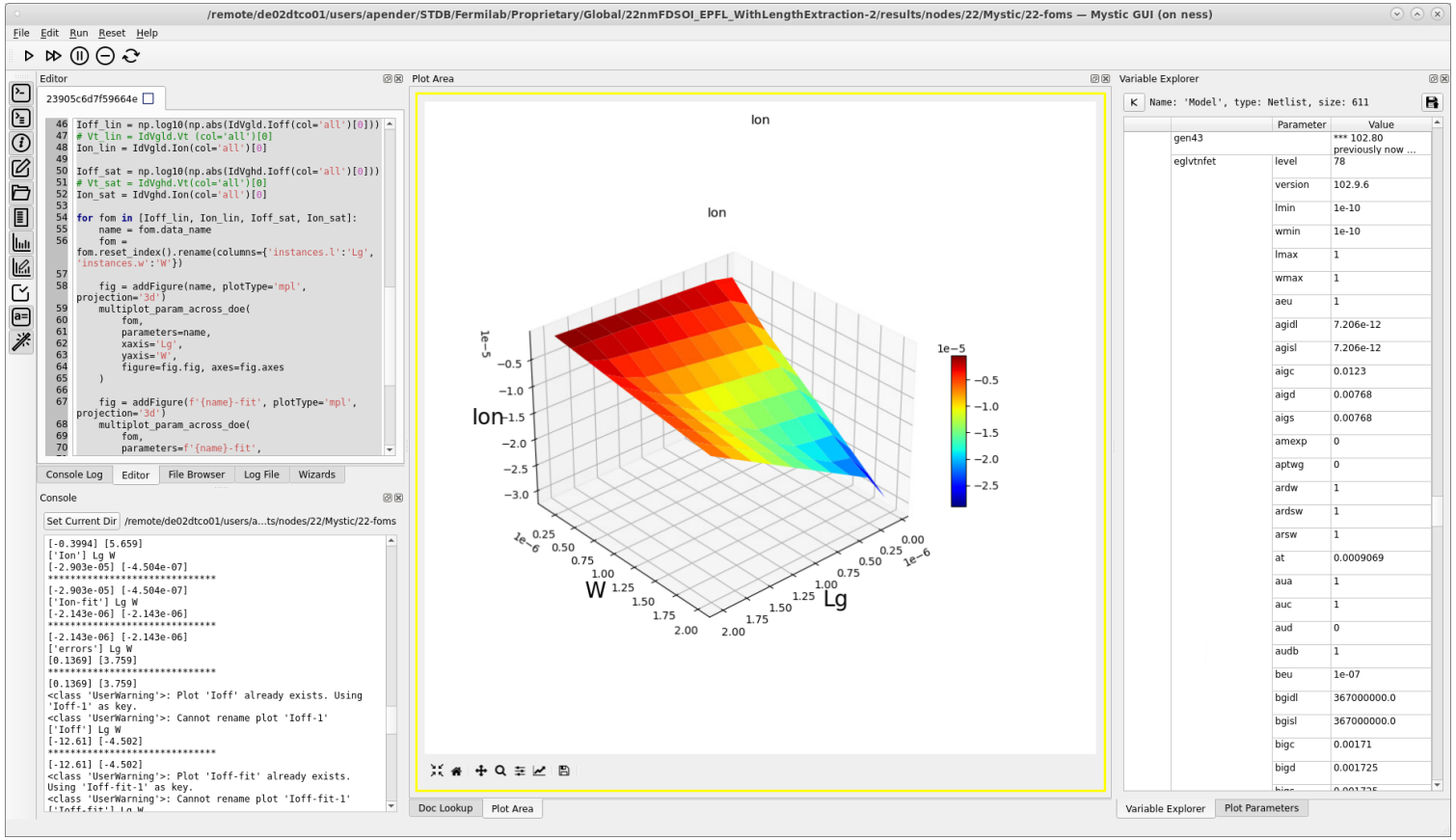

[1] Lotfi, Nima, et al. “A single-channel 18.5 GS/s 5-bit flash ADC using a body-biased comparator architecture in 22nm FD-soi.” *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, https://doi.org/10.1109/iscas.2019.8702505.
"A Single-Channel 18.5 GS/s 5-bit Flash ADC using a Body-Biased Comparator Architecture in 22nm FD-SOI""
[2] Tang, Zhidong, et al. “Cryogenic CMOS RF device modeling for Scalable Quantum Computer Design.” *IEEE Journal of the Electron Devices Society*, vol. 10, 2022, pp. 532–539, https://doi.org/10.1109/jeds.2022.3186979.
[3] Beckers, Arnout, Farzan Jazaeri, Heorhii Bohuslavskyi, et al. “Characterization and modeling of 28-NM FDSOI CMOS technology down to cryogenic temperatures.” *Solid-State Electronics*, vol. 159, 2019, pp. 106–115, https://doi.org/10.1016/j.sse.2019.03.033.
[4] Inaba, Takumi, et al. “Importance of source and drain extension design in cryogenic MOSFET operation: Causes of unexpected threshold voltage increases.” *Applied Physics Express*, vol. 15, no. 8, 2022, p. 084004, https://doi.org/10.35848/1882-0786/ac819b.
[5] Hart, P. A. ’t, Babaie, M., Vladimirescu, A., & Sebastiano, F. (2021, June 15). *Characterization and modeling of self-heating in nanometer bulk-CMOS at cryogenic temperatures*. arXiv.org. https://arxiv.org/abs/2106.07982
[6] Importance of source and drain extension design in ... - iopscience. (n.d.-a). https://iopscience.iop.org/article/10.35848/1882-0786/ac819b
[7] Beckers, Arnout, et al. “Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing.” *2017 47th European Solid-State Device Research Conference (ESSDERC)*, 2017, https://doi.org/10.1109/essderc.2017.8066592.
[8]Author links open overlay panelArnout Beckers a, et al. “Characterization and Modeling of 28-NM FDSOI CMOS Technology down to Cryogenic Temperatures.” *Solid-State Electronics*, Pergamon, 21 Mar. 2019, www.sciencedirect.com/science/article/pii/S0038110119301443.
[9] Beckers, Arnout, Farzan Jazaeri, and Christian Enz. “Cryogenic mos transistor model.” *IEEE Transactions on Electron Devices*, vol. 65, no. 9, 2018, pp. 3617–3625, https://doi.org/10.1109/ted.2018.2854701.
[10] Bohuslavskyi, H., et al. “Cryogenic subthreshold swing saturation in FD-soi mosfets described with band broadening.” *IEEE Electron Device Letters*, vol. 40, no. 5, 2019, pp. 784–787, https://doi.org/10.1109/led.2019.2903111.
[11] Chen, Zehua, et al. “Temperature dependences of threshold voltage and drain-induced barrier lowering in 60NM gate length MOS transistors.” *Microelectronics Reliability*, vol. 54, no. 6–7, 2014, pp. 1109–1114, https://doi.org/10.1016/j.microrel.2013.12.005.
[12] Bhardwaj, Anuj, et al. “Narrow-width effects in 28-nm FD-SOI transistors operating at cryogenic temperatures.” *IEEE Journal of the Electron Devices Society*, vol. 11, 2023, pp. 22–29, https://doi.org/10.1109/jeds.2022.3233302.
[13] Chakraborty, Wriddhi, et al. “Characterization and modeling of 22 nm FDSOI Cryogenic RF CMOS.” *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 7, no. 2, 2021, pp. 184–192, https://doi.org/10.1109/jxcdc.2021.3131144.
[14] G. Pahwa, P. Kushwaha, A. Dasgupta, S. Salahuddin, and C. Hu, “Compact modeling of temperature effects in fdsoi and finfet devices down to cryogenic temperatures,” *IEEE*, 2021.
[15] Han, Hung-Chi, et al. “Analytical modeling of source-to-drain tunneling current down to cryogenic temperatures.” *IEEE Electron Device Letters*, vol. 44, no. 5, 2023, pp. 717–720, https://doi.org/10.1109/led.2023.3254592.
[16] Tripathi, S. Pati, et al. "Characterization and modeling of quantum dot behavior in FDSOI devices." *IEEE Journal of the Electron Devices Society* 10 (2022): 600-610 https://doi.org/10.1109/JEDS.2022.3176205
[17] Braga, Davide, Shaorui Li, and Farah Fahim. "Cryogenic electronics development for high-energy physics: An overview of design considerations, benefits, and unique challenges." *IEEE Solid-State Circuits Magazine* 13.2 (2021): 36-45. https://doi.org/10.1109/MSSC.2021.3072804

# Backups


IdVg Low Drain
Drain Current (A)
0
-1e-05
-2e-05
-3e-05
-4e-05
-1
0
1
Gate Voltage (V)
NFet Measurement Data
PFet Measurement Data
PDK Model
PDK Model
Extracted Model
Extracted Model

# Mystic Software

- Interactive plotting environment allows for real-time visualization of model fits against target data on single 1D plots or higher dimensional spaces





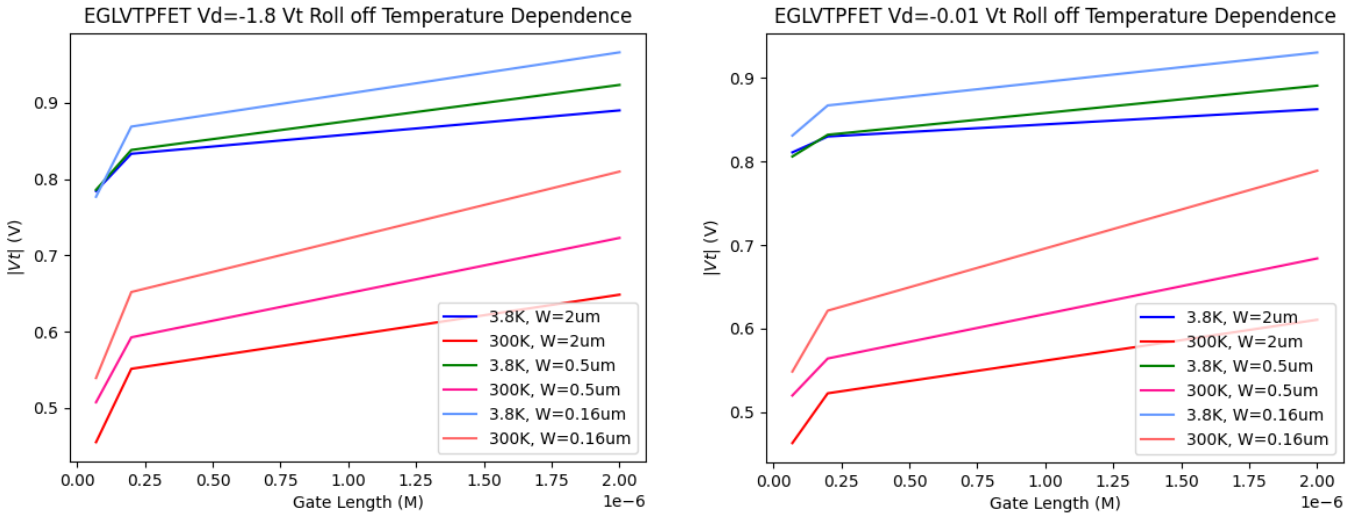

Fermilab

# BSIM-IMG Version 102.8

- Temperature range not made for deep-Cryo
- **Independent Multi-Gate (IMG)** models the **Back gate**
- We have shifted to **102.9.6 t**o use the most up to date version
- **Version 102.9.6**:
  - Includes cryogenic modeling, we tried running this version down to 4K with our PDK Model but it broke
  - If tnom=temp is kept at 50k and the cryomod function is disabled, the **PDK model stays the same**
  - **Same underlying equations as 102.8** so nothing should change if the new features are disabled

# Threshold Voltage Expectation at Cryogenic Temperatures

- Increase in Vt as temperature decreases seen in 28nm FDSOI [12]
- Our 22nm FDSOI data reflects this trend, with an average 250 mV difference in Vt across all lengths/widths:




Used **fixed current criteria** rather than GmMax to get a smoother roll off across geometries (GmMax method in backup slides)

**High drain** roll-off usually shows a **bigger difference in Vt because of DIBL**, at cryo we want Vt geometry dependence to be **more linear,** which is seen in the rightmost plot

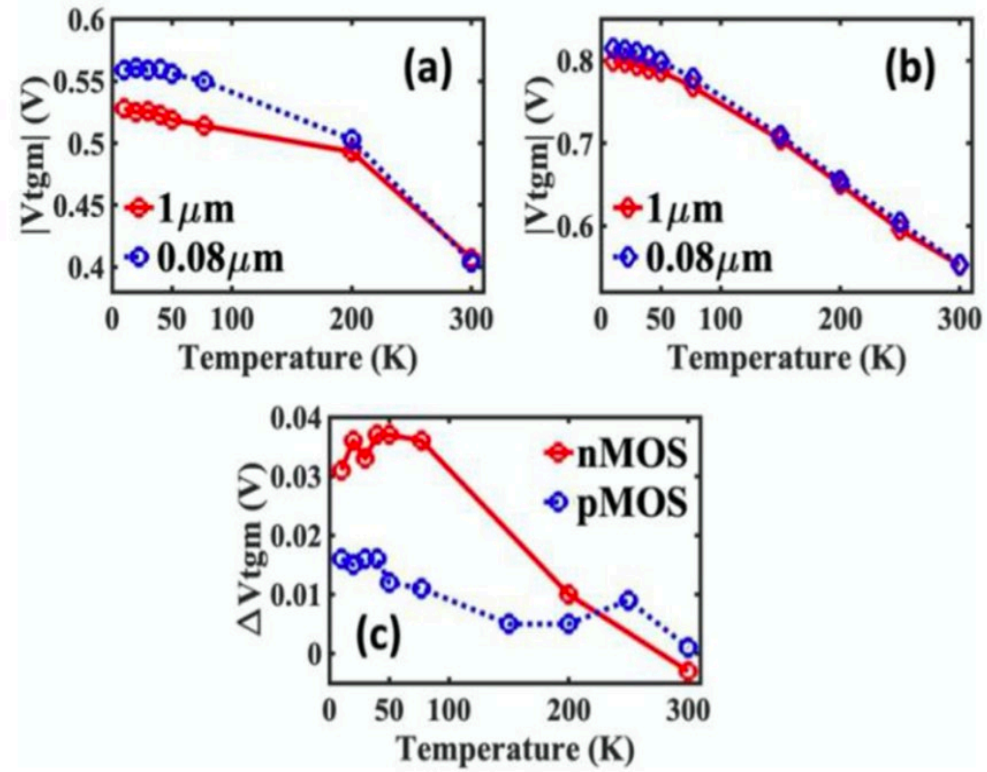


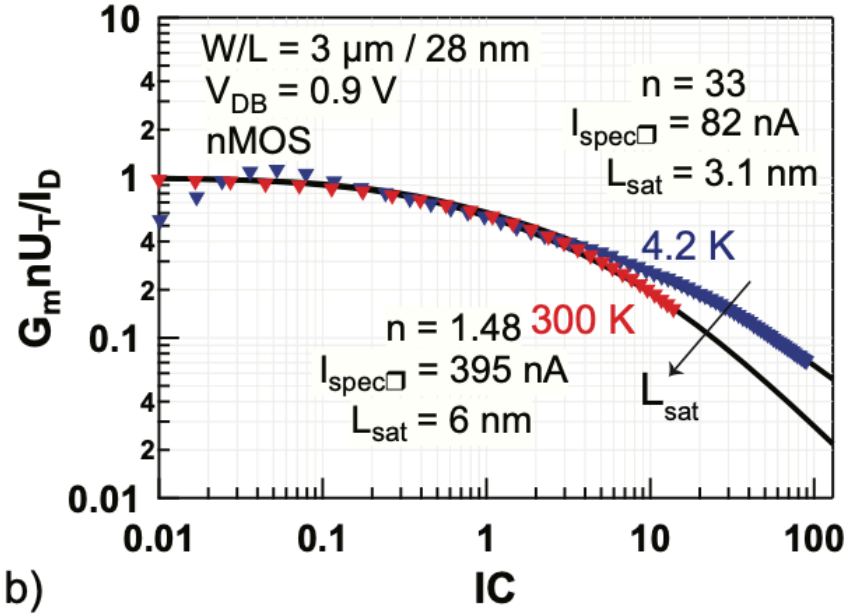

**FIGURE 4.** **|*Vt*| vs Temperature at |Vds|=50 mV using maximum transconductance method for (a) nMOS and (b) pMOS, (c) Δ*Vt* vs temperature using maximum transconductance method. The back-gate bias (*Vbs*) = 0 V.** [12]



Fermilab

# Velocity Saturation Expectation at Cryogenic Temperatures

Decrease in impact of velocity saturation seen in 28nm FDSOI [7][8]




b) Normalized transconductance efficiency versus the inversion coefficient for nMOS W/L = 3 µm / 28 nm, showing a decreased velocity saturation effect at 4.2 K. [7]

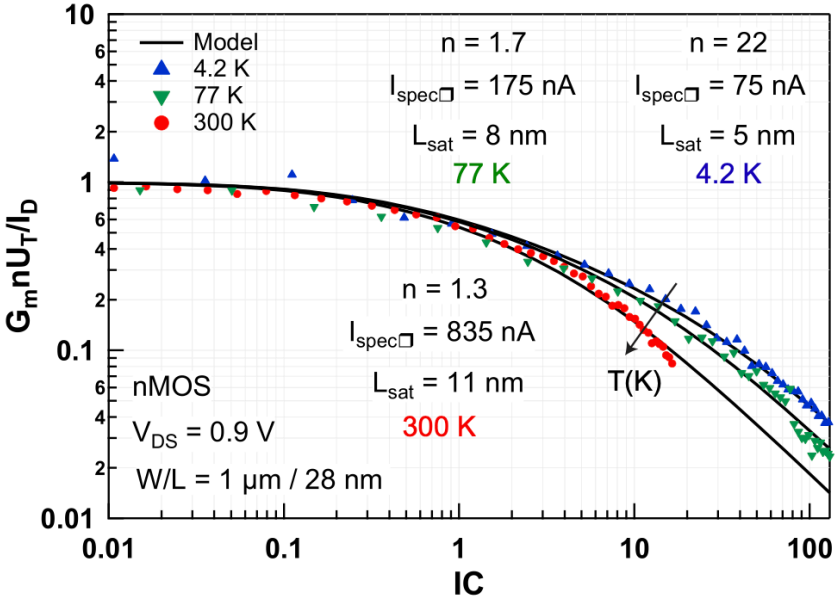



Figure 10: Modeling the normalized transconductance efficiency at 300, 77, and 4.2 K in a short 28-nm FDSOI nMOS in saturation. Model parameters are given in the figure. [8]



Fermilab

# Source/Drain Resistance Expectation at Cryogenic Temperatures

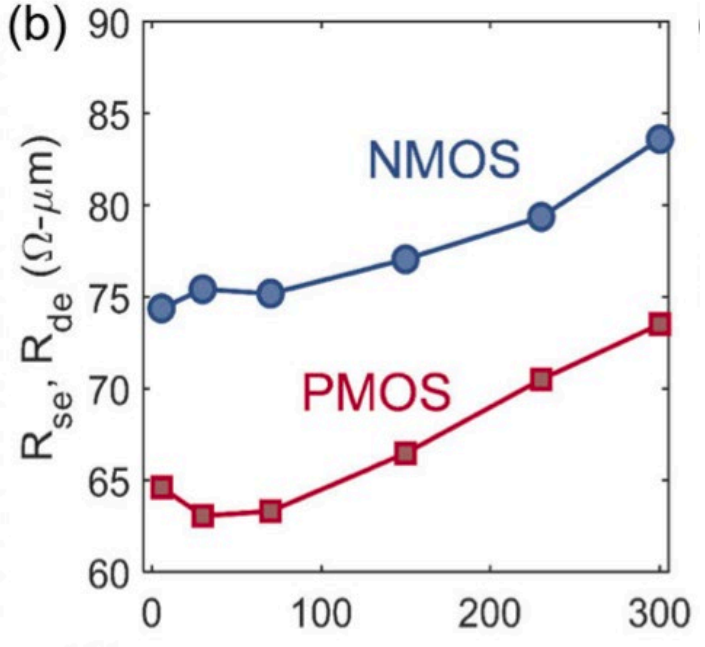
- In 22nm FDSOI a **11-15% decrease** seen in S/D resistance [13]

- Improvement in gate resistance:
  - **Prwg** models gate dependence of S/D resistance in BSIM 102.9.6, and as it **increases, overall resistance should decrease** (Our models reflect this)

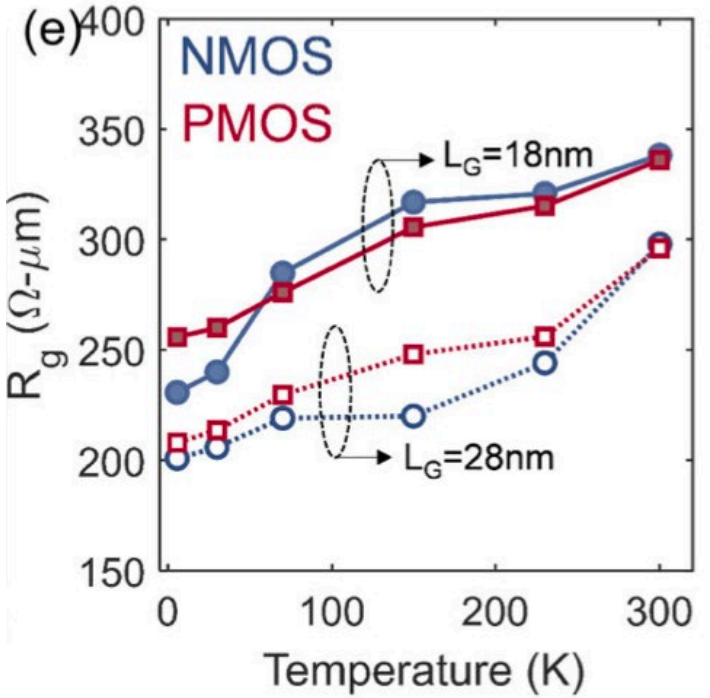
**From BSIM-IMG 102.9.6 Manual:**

$$R_{source} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left( RSWMIN(T) + \frac{RSW(T)}{1 + PRWG \cdot V_{gs,eff}} \right) + R_{s,geo}$$

$$R_{drain} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left( RDWMIN(T) + \frac{RDW(T)}{1 + PRWG \cdot V_{gd,eff}} \right) + R_{d,geo}$$




Source/drain series resistance (*R*se, *R*de) improve by 15% at 5.5 K [13]




Reduced resistivity of gate metal contact (NiSi) and poly-Si cause gate resistance (*R*ge) reduction at cryogenic temperature. [13]

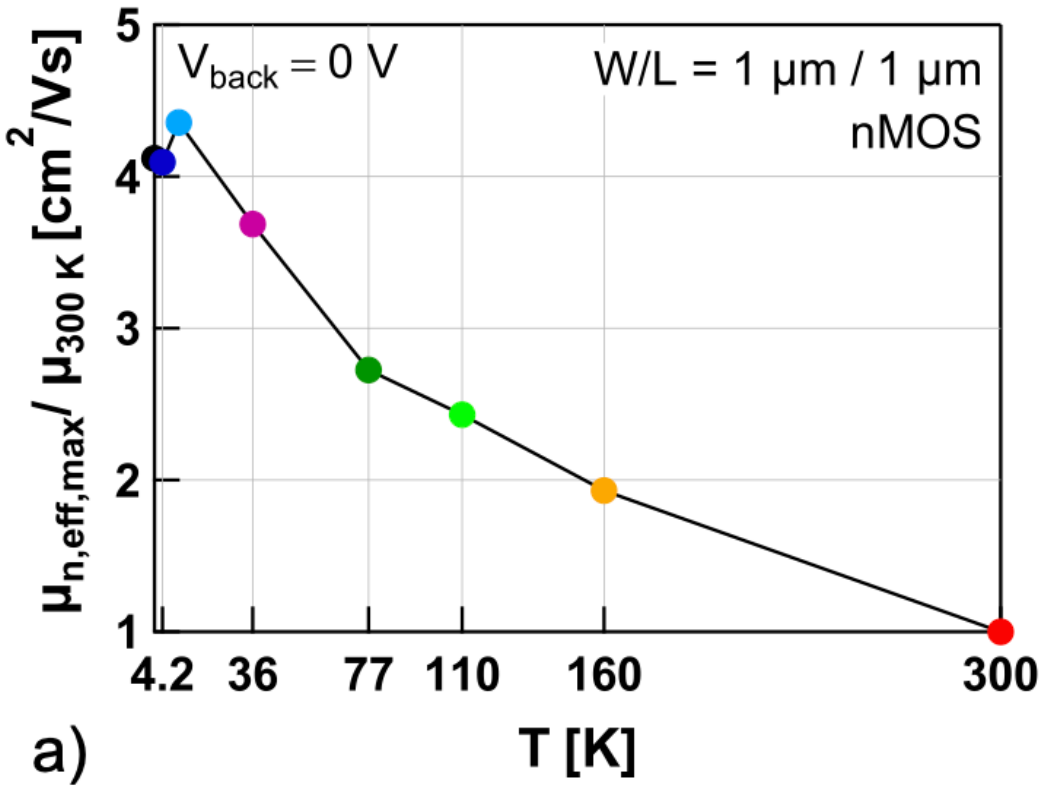


Fermilab

# Mobility Expectation at Cryogenic Temperatures

- Effective mobility is made of three main components:
  - Lattice vibration-induced scattering
  - Scattering on impurities (Coulomb and phonon scattering)
  - Surface Roughness Scattering

- At cryogenic temperatures Coulomb Scattering becomes more dominant increasing mobility [2]




Effective Mobility Temperature dependence in 28nm FDSOI [3]



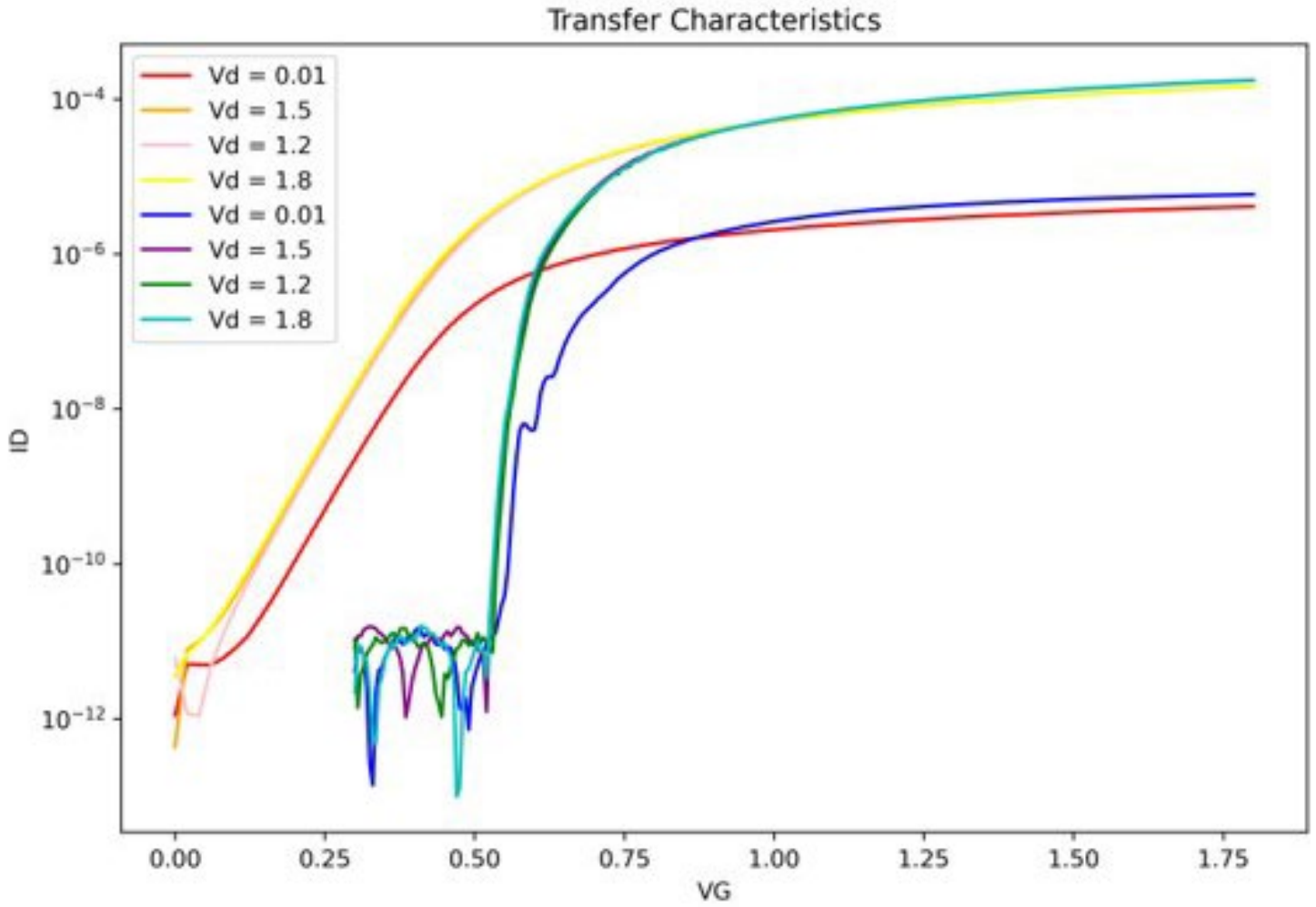
Fermilab

# Subthreshold Current Jumps

Most of our data doesn't have this effect, but a few curves do, like the one seen here.

This is caused by **source/drain tunneling** [15] [16]

We are not modeling this for now

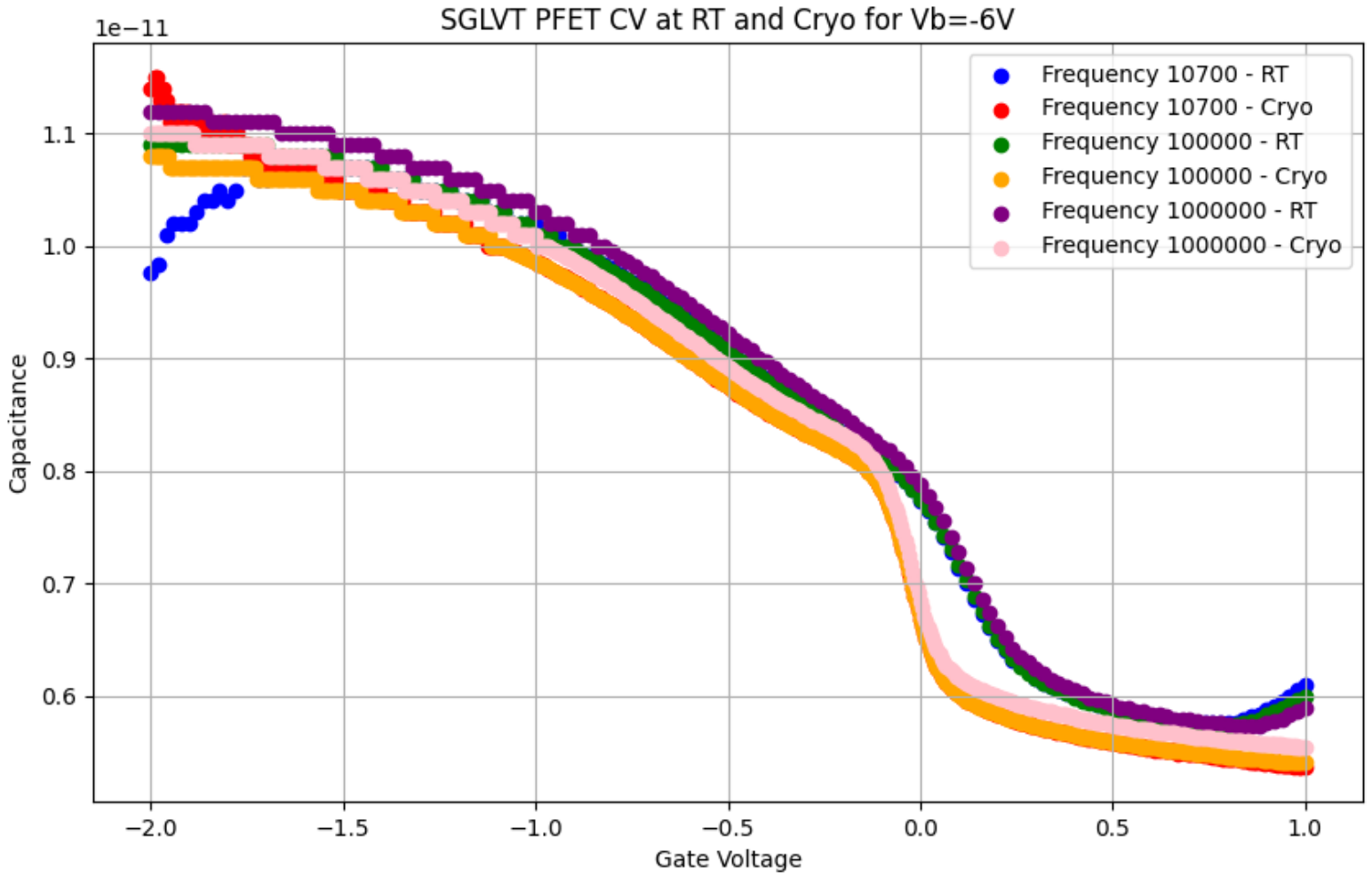





Fermilab

# CV Temperature Dependence

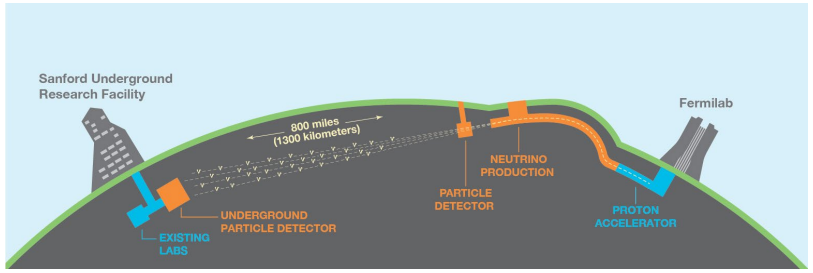
Not a significant change with temperature, so we are not modeling this for now

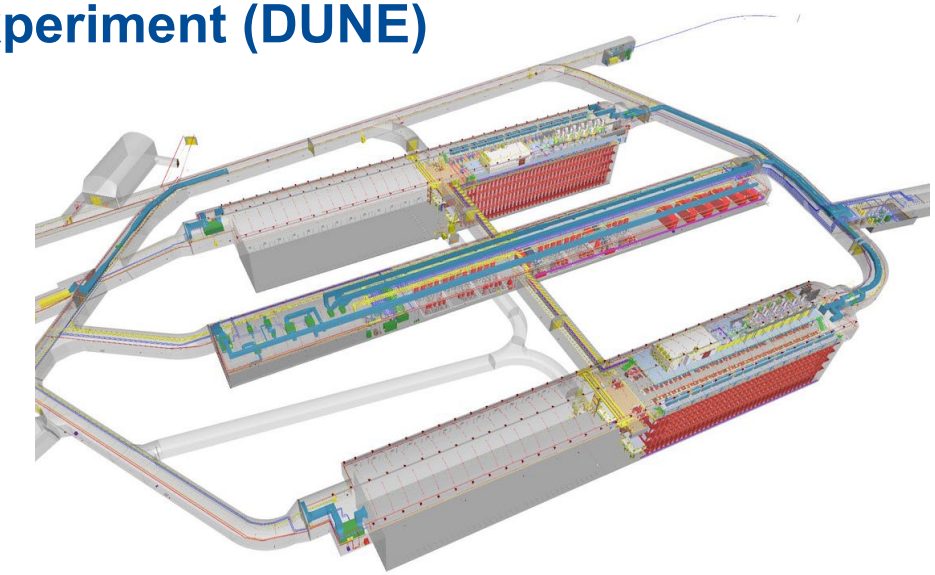


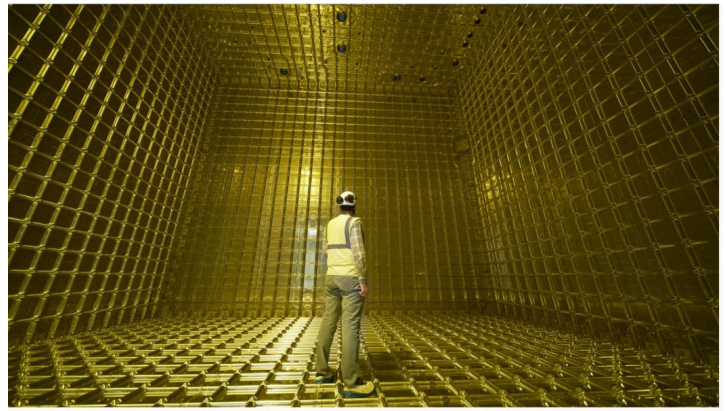


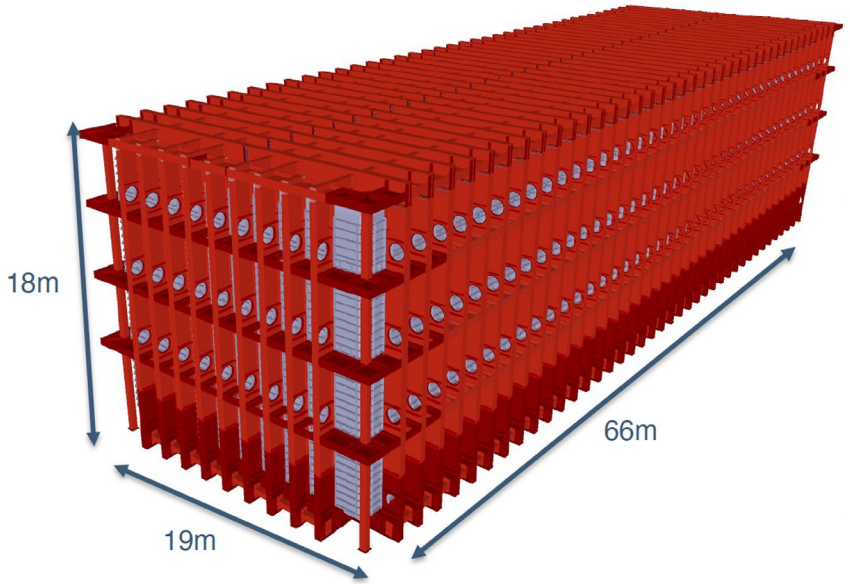

Fermilab

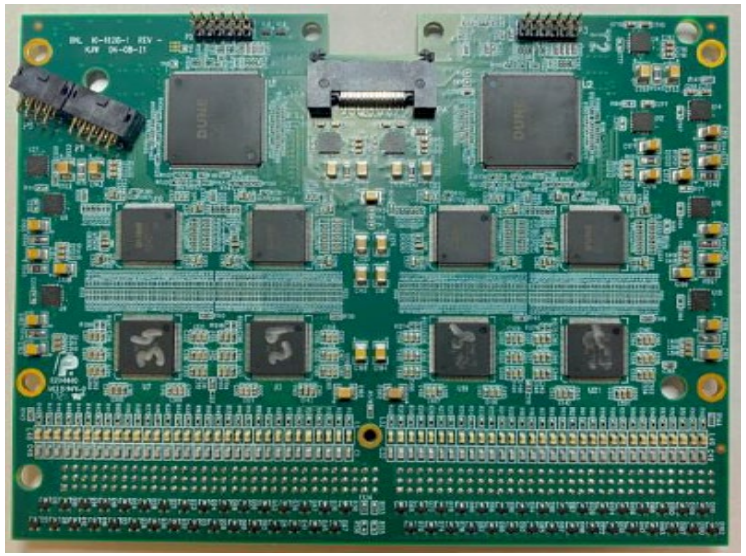
# Deep Underground Neutrino Experiment (DUNE)





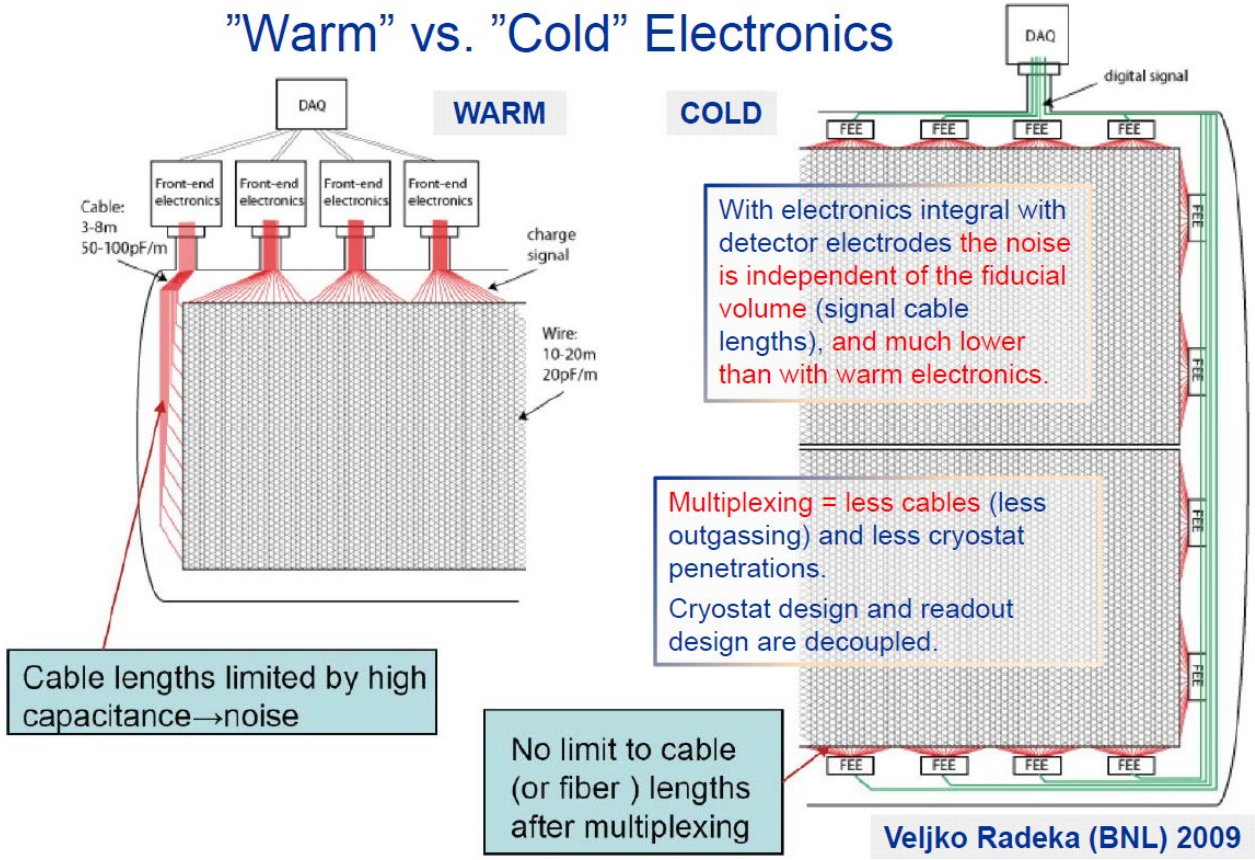


Fermilab

# Operation in liquid Argon

## Requirements

- Less than 0.7% channel failure in **30 years of operation**
- Total power consumption <50 mW/channel.
- Fully functional at 89 Kelvin



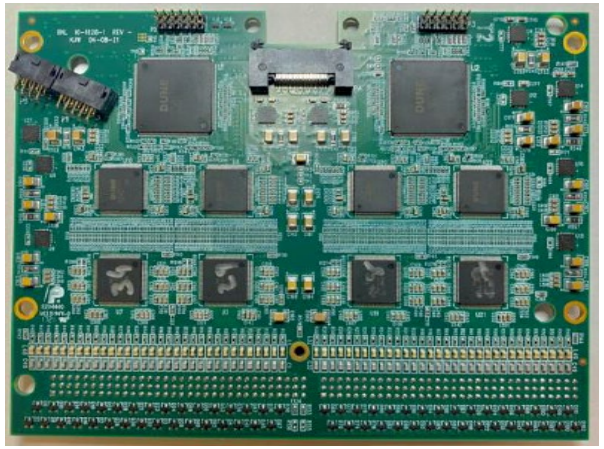

## Benefits of operating in liquid Argon:

- Increased **charge carrier mobility** --> **higher gain** and **lower noise** (by about a factor of two) at 89 Kelvin
- Mounting the front-end electronics on the anode plane array (APA) frames also **minimizes the input capacitance**.
- Placing the digitizing and multiplexing electronics inside of the cryostat allows for a **reduction in the total number of feed-throughs** into the cryostat

# DUNE cryogenic ASICs

- 16-channel front-end ASICs for amplification and pulse shaping (**LArASIC** - BNL);
- 16-channel 12-bit ADC ASICs operating at 2 MHz (**ColdADC** – LBNL+FNAL+BNL);
- 64-channel control and communications ASICs (**COLDATA** – FNAL+SMU)

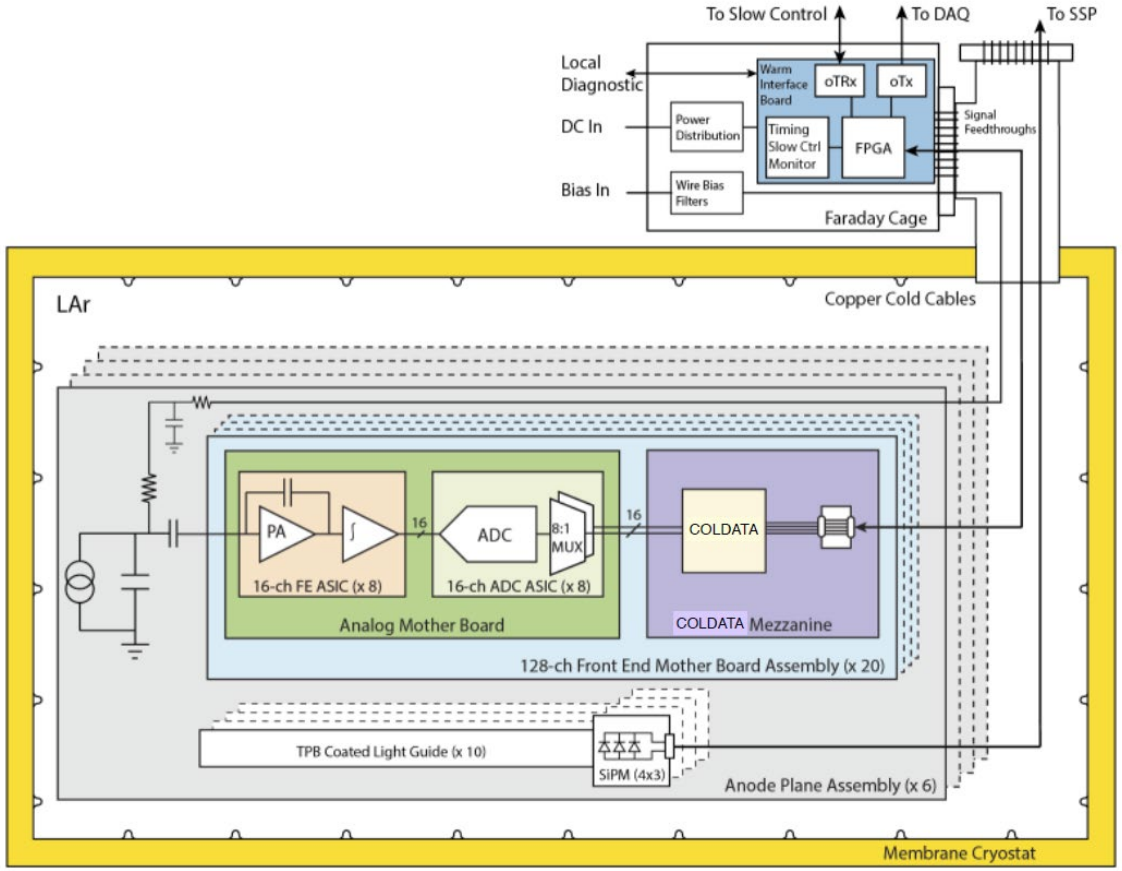
| Element | Quantity |
|---|---|
| TPC wires (channels) | 384K |
| Anode plane array (APA) | 150 |
| Front End Mother Board (FEMB) | 3000 |
| FE ASIC | **24000** |
| ADC ASIC | **24000** |
| COLDATA ASIC | **6000** |



- Large number of components requiring testing and qualification at both roomT and LAr
- Future proposed pixelated readout schemes with >100M channels (<100μW/channel), SiPh for readout and power delivery, chiplet-based or monolithic chips with integrated sensing, computing and communication

Large scientific experiments challenges and requirements:
- Performance (low noise, low power)
- Thermal and system constraints (e.g feedthroughs)
- Reliability (lifetime, SEE)
- Large # channels
- Radiopurity, etc.

… not too dissimilar to the challenges of scalable quantum computers

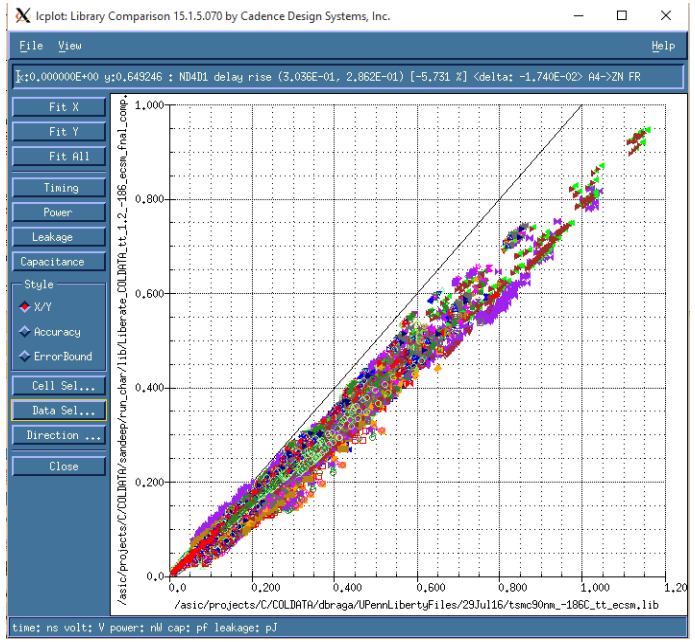


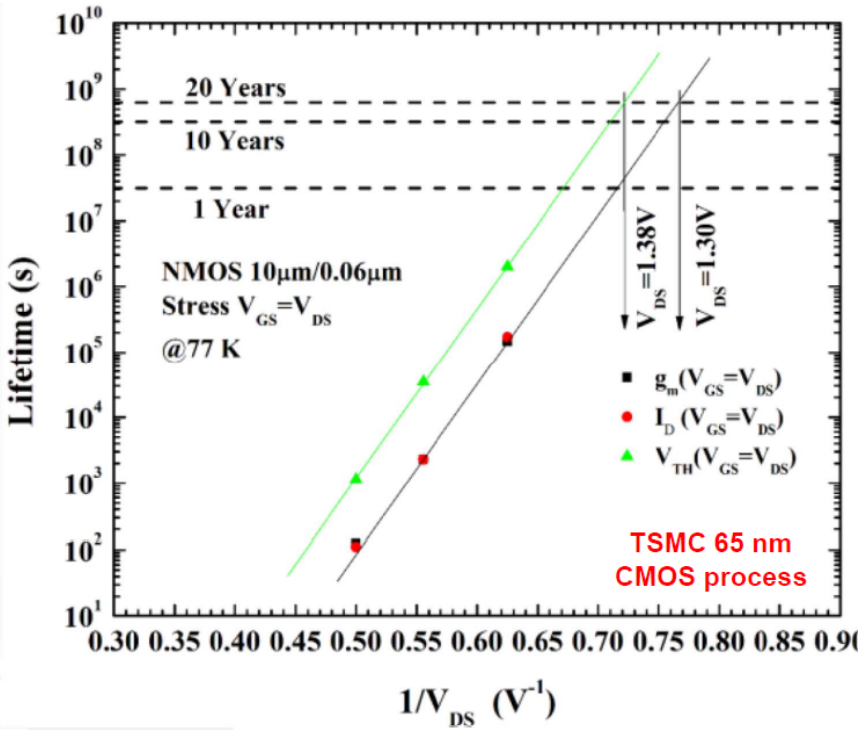
# Lifetime studies, modeling, and custom library development

Hot carrier induced lifetime degradation can be avoided by limiting Vds and/or increasing L

→ We derated the nominal supply by 10% and created a custom digital library with increased L (90nm)

The custom library (~230 cells) was characterized for static timing analysis (timing and power across corners) for digital synthesis and place and route.




The predicted lifetime for 130 nm nMOS devices reaches 20 years provided the drain voltages are reduced from the nominal, room temperature value of 1.5 V to a cryogenic temperature value of 1.49 V.

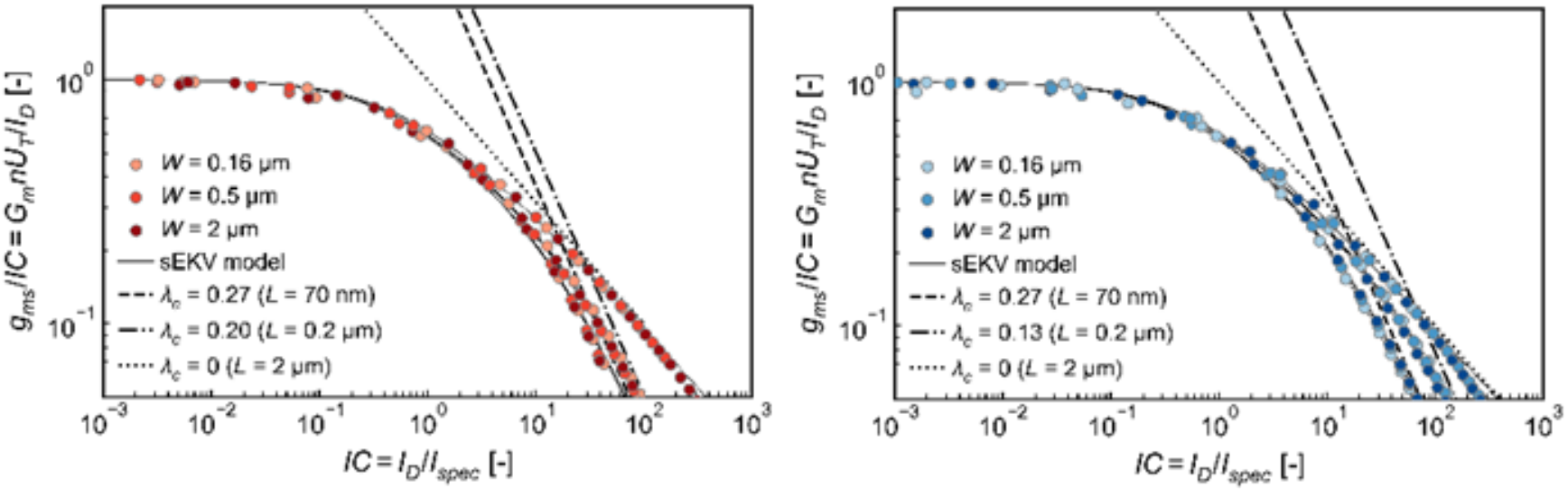
As noteworthy as this prediction is, the 65 nm nMOS device is even more resistant to cryogenic hot carrier degradation. Its nominal, room temperature voltage of 1.2 V is already lower than the maximum allowable cryogenic temperature voltage of 1.3 V.


**FERMILAB/SMU:** J. R. Hoff, et al., IEEE TRANS. ON NUCLEAR SCIENCE, VOL.59, NO.4, AUGUST 2012
**BNL:** Shaorui Li, et al., IEEE TRANS. ON NUCLEAR SCIENCE, VOL.60, NO.6, DECEMBER 2013
**FERMILAB/SMU:** Guoying Wu, et al., IEEE TRANS. ON DEV. AND MATERIALS RELIABILITY, VOL.14, NO.1, MARCH 2014
**FERMILAB/SMU:** J.R.Hoff, et al., „Cryogenic Lifetime Studies of 130nm and 65nm CMOS Technologies for High-Energy Physics Experiments, *in publishing in IEEE TRANS. ON NUCLEAR SCIENCE*

# 22FDX Cryogenic modeling - EKV

Collaboration with EPFL (Han, Enz, Charbon) for simplified EKV (sEKV) modeling for inversion coefficient design methodology (for analog design)

Data from GF's Basic FET Test Structures, measured at 3.8K at EPFL




The normalized transconductance efficiency with the application of simplified EKV model on EG FDSOI devices at room temperature; (left) nMOS, (right) pMOS.

| Oxide | Device | Type | # devices |
|---|---|---|---|
| EG | lvt | N | 9 |
| | | P | 9 |
| | slvt | N | 9 |
| | | P | 9 |
| SG | rvt | N | 7 |
| | | P | 5 |
| | slvt | P | 4 |
| | | N | in progress |



Fermilab

# 22FDX Cryogenic modeling - EKV

Collaboration with EPFL (Han, Enz, Charbon) for **Simplified EKV (S-EKV)** modeling for inversion coefficient design methodology (for analog design)

Data from GF's Basic FET Test Structures, measured with cryogenic probe station (3.8K) at EPFL

Length Scaling at Cryogenic Temperatures:

- effective mobility in terms of channel length and the temperature
- source-to-drain tunneling in subthreshold region

(Cryogenic RF characterization)

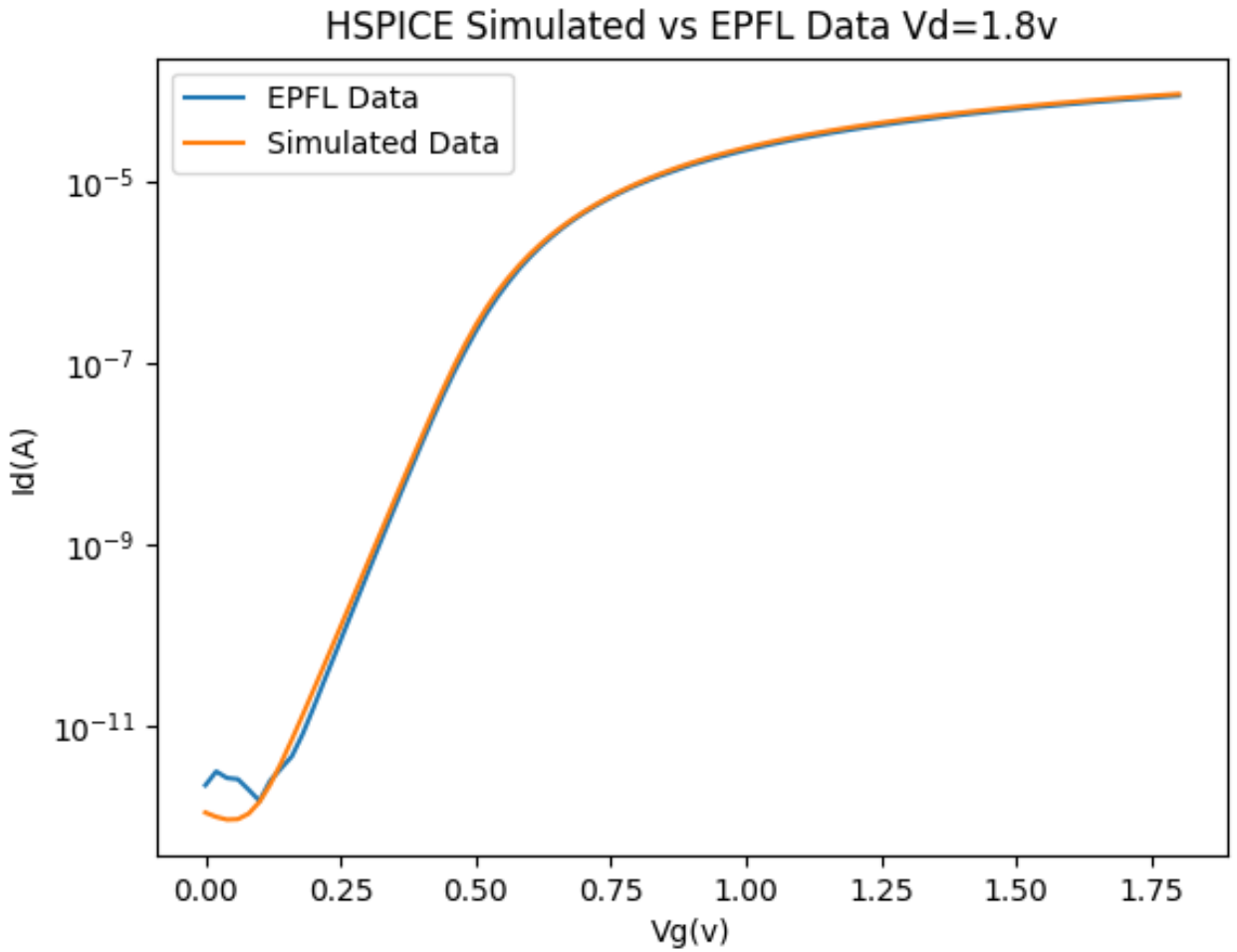
Open-source Python-based parameter extractor (SEKV-E) for the simplified EKV (sEKV) model https://gitlab.com/moscm/sekv-e

EPFL


- Han, Hung-Chi, Antonio D'Amico, and Christian Enz. "Comprehensive Design-oriented FDSOI EKV Model." *2022 29th International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*. IEEE, 2022.
- H.-C. Han, F. Jazaeri, Z. Zhao, S. Lehmann, C. Enz, "*An improved subthreshold swing expression accounting for back-gate bias in FDSOI FETs*", in *Solid-state Electronics*, vol. 202, 108608, April 2023. Doi: 10.1016/j.sse.2023.108608
- Han, Hung-Chi, et al. "In-depth cryogenic characterization of 22 nm FDSOI technology for quantum computation." *2021 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS)*. IEEE, 2021.
- Han, Hung-Chi, et al. "Cryogenic RF Characterization and Simple Modeling of a 22 nm FDSOI Technology." *ESSDERC 2022-IEEE 52nd European Solid-State Device Research Conference (ESSDERC)*. IEEE, 2022.
- H. -C. Han, A. D'Amico and C. Enz, "SEKV-E: Parameter Extractor of Simplified EKV I-V Model for Low-Power Analog Circuits," in IEEE Open Journal of Circuits and Systems, vol. 3, pp. 162-167, 2022, doi: 10.1109/OJCAS.2022.3179046.


Fermilab

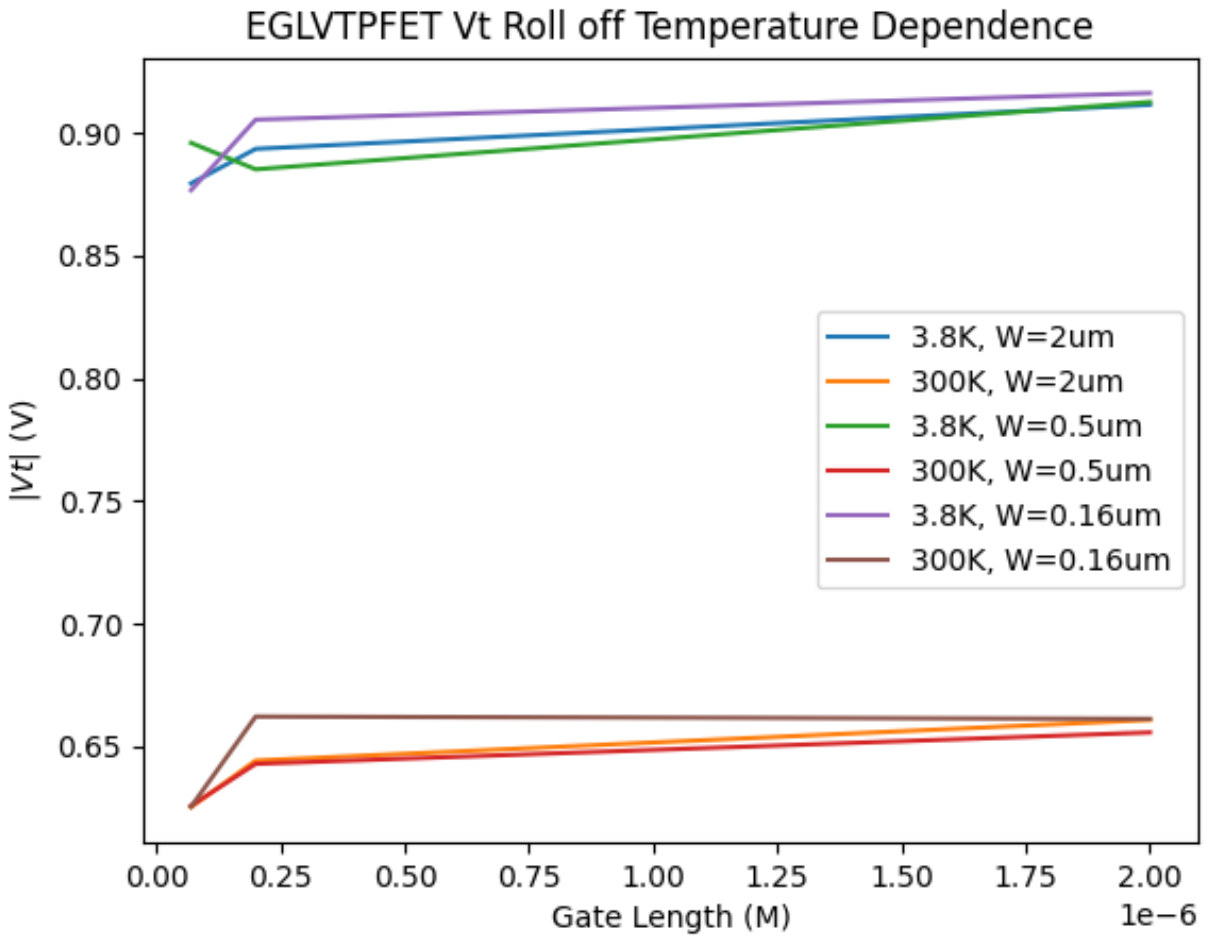
# PDK Validation at room temp






Fermilab

# Vt Rolloff using GmMax method

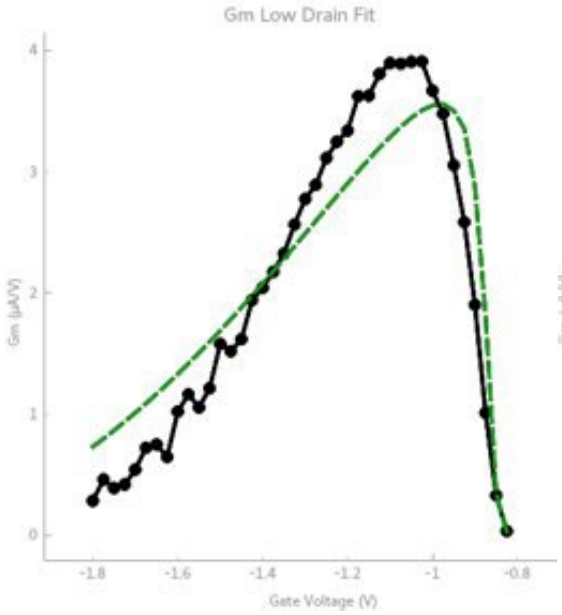


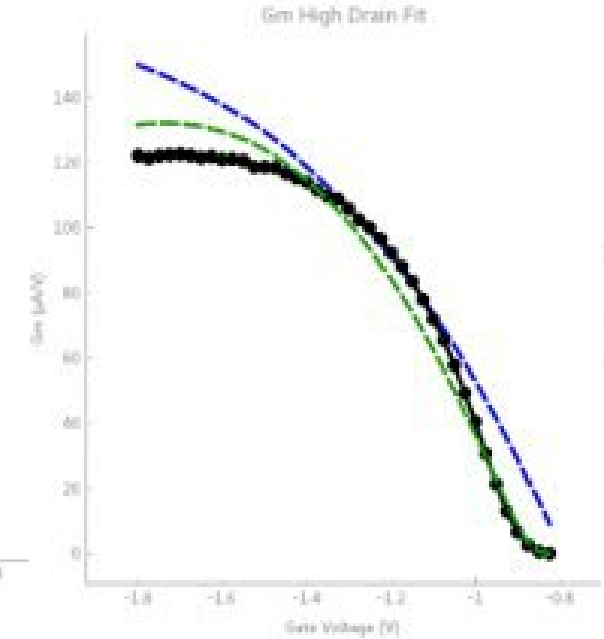

Temperature impact on Vt Roll Off for Vd=0.01V using maximum transconductance method from EPFL data

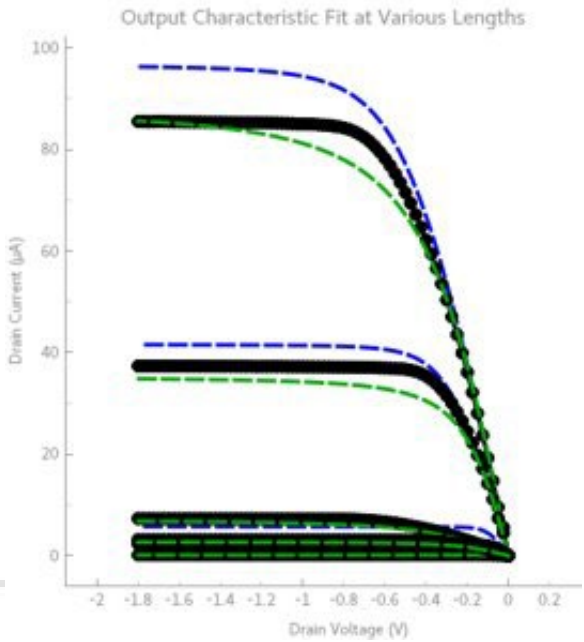


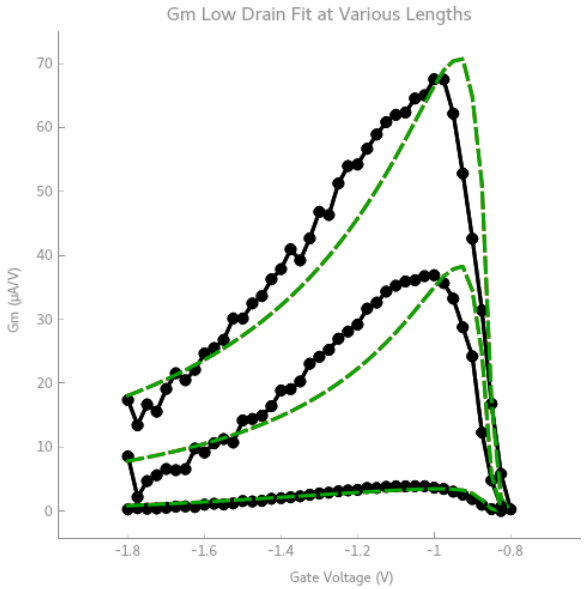
Fermilab

# Extra pfet plots



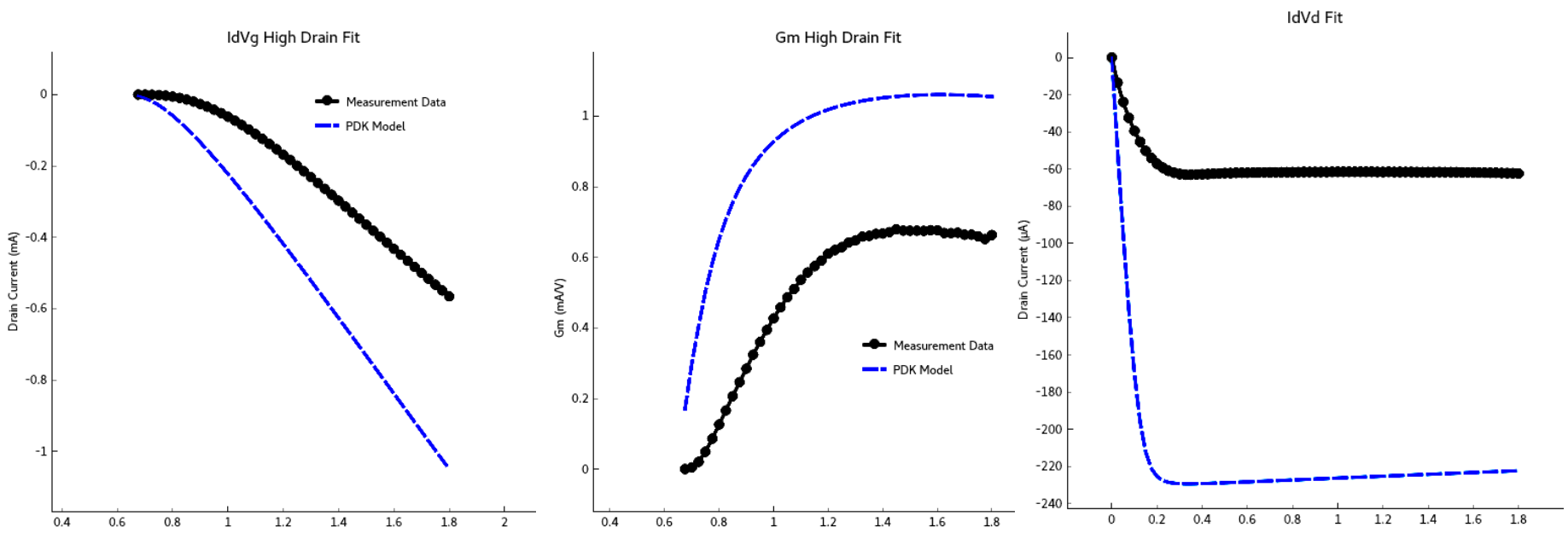





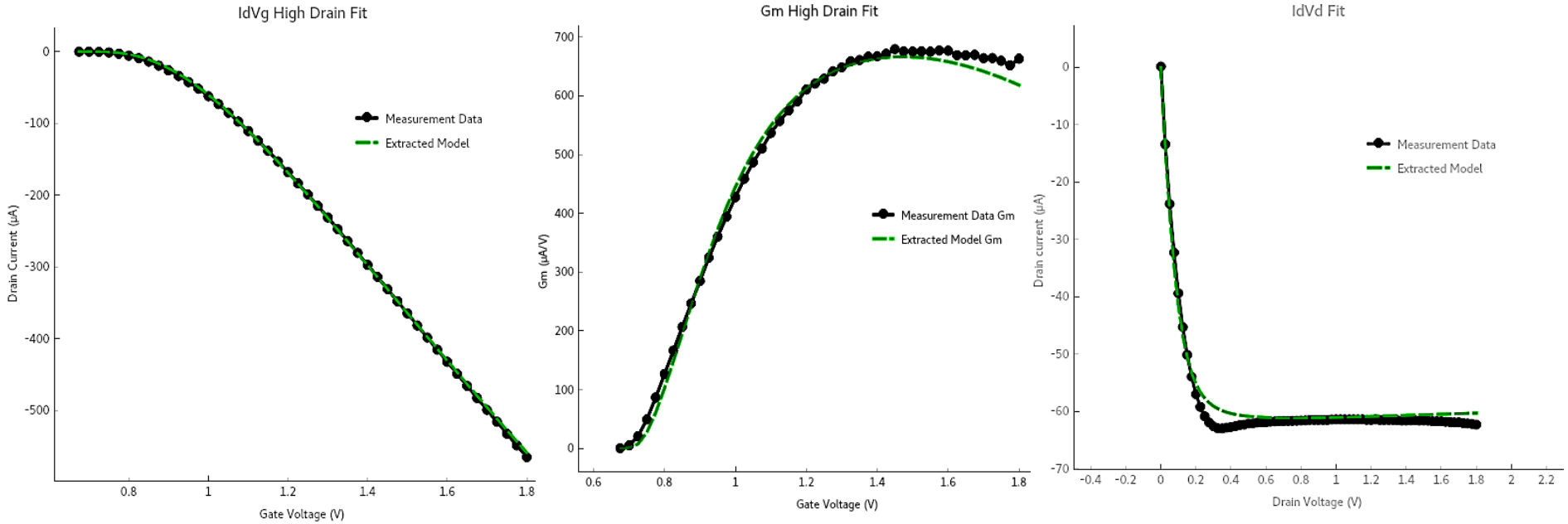

Fermilab

# Stage 2

PDK Model (with t=tnom=50K and rdw/rsw=130):




Our Model:

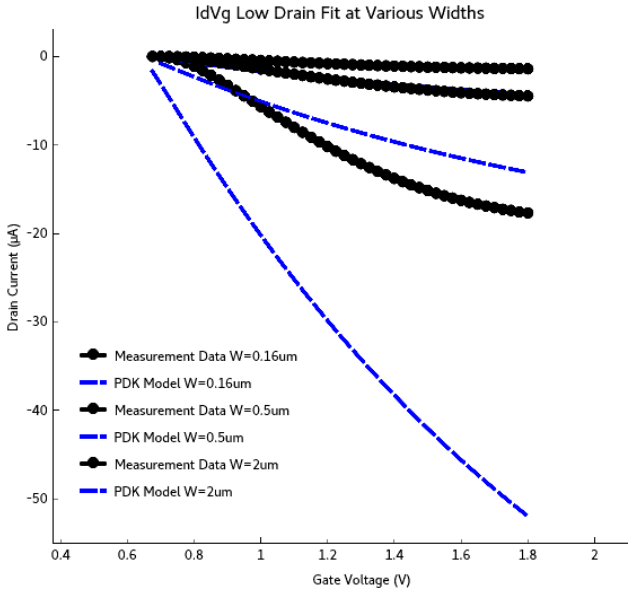


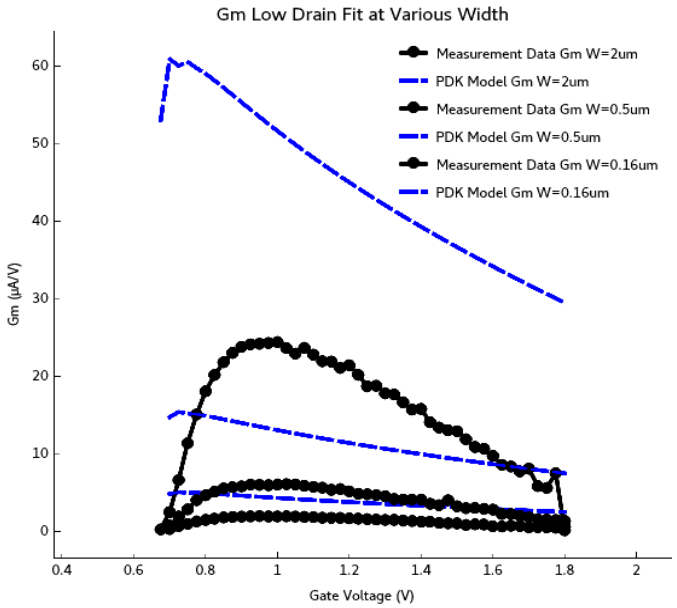



Fermilab

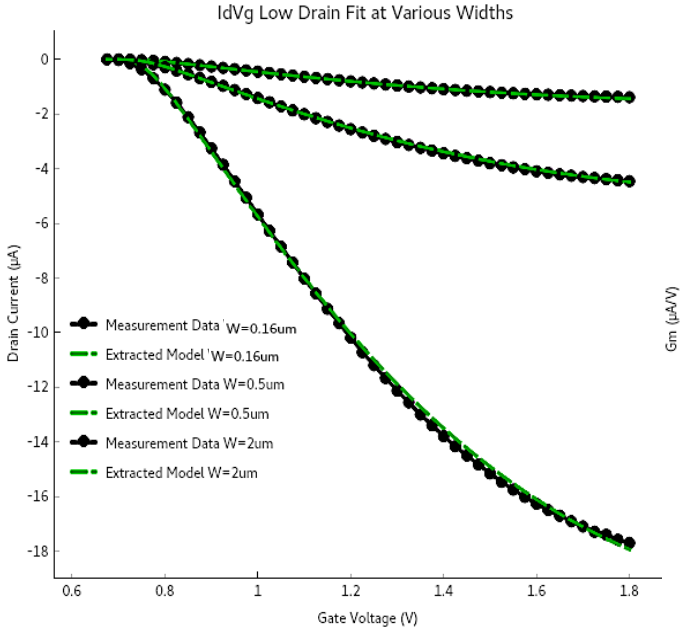
# Stage 3

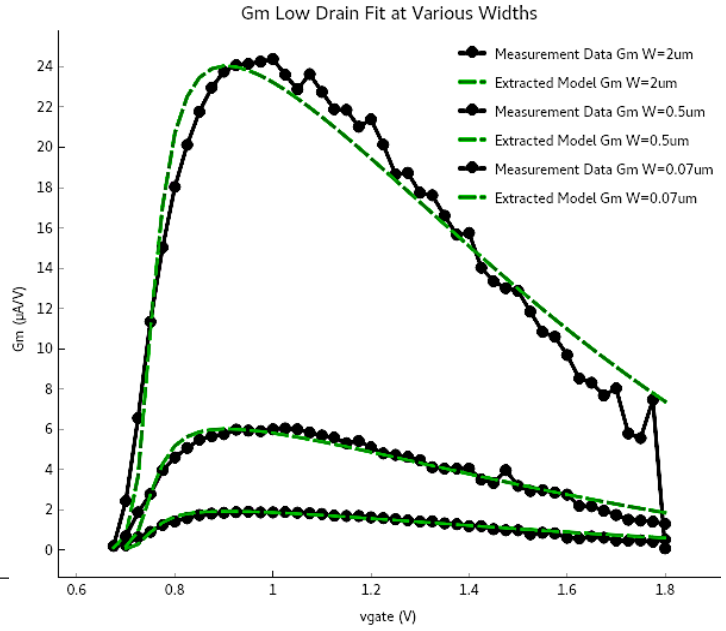
PDK Model (with t=tnom=50K and rdw/rsw=130):




Our Model:

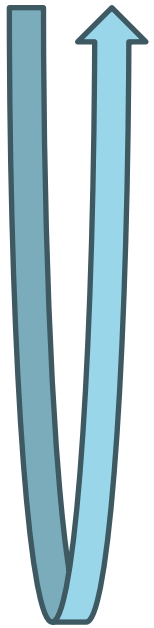




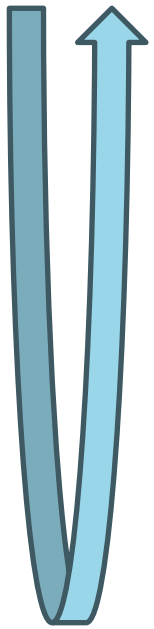

Fermilab

# Stage 1: Low Drain extraction



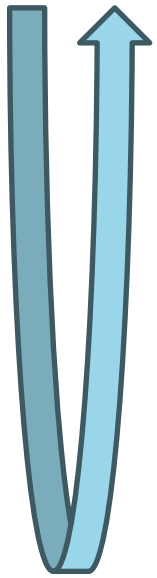
| | Parameters adjusted | Target Regions | Behavior modelled |
|---|---|---|---|
| Step 1 | Cit, phig1 | IdVg Below threshold voltage | Work function and Subthreshold slope |
| Step 2 | u0, ua | IdVg Mobility region | Mobility |
| Step 3 | u0,ua,eu,ud,rdw,rsw,ucs,prwg | IdVg Above Vth | Source/drain extension resistance, front gate bias dependence on s/d resistance, coulomb scattering, phonon/surface roughness scattering |
| Step 4 | phig1,ua,eu,ud,rdw,rsw,ucs,prwg | IdVg Below Vth, resistance region | All of the above |

# Stage 2: High Drain extraction



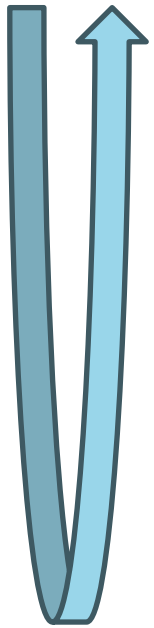
| | Parameters adjusted | Target Regions | Behavior modelled |
|---|---|---|---|
| Step 1 | Eta0, cdscd | IdVg Below Vt | Drain induced barrier lowering, drain bias sensitivity of cdsc (subthreshold slope) |
| Step 2 | Mexp, vsat | IdVg strong inversion | Smoothing for Vd saturation, Velocity saturation |
| Step 3 | vsat, vsat1, ptwg, pvag, ksativ | IdVg AboveVt, IdVd sat | Velocity saturation, Strong inversion Vd saturation, Vg dependence on early voltage |
| Step 4 | Mexp, vsat | IdVg strong inversion | Smoothing for Vd saturation, Velocity saturation |

# Stage 3: Width extraction



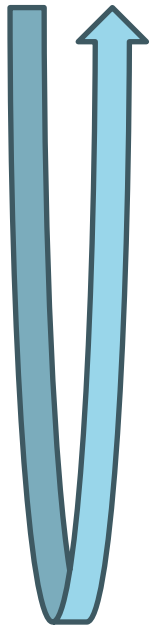
| | Parameters adjusted | Target Regions | Behavior modelled |
|---|---|---|---|
| Step 1 | wphig1 | Below Vt on all 3 low drain widths for our longest device | Width dependent work function |
| Step 2 | wu0 | Above Vt on all 3 low drain widths for our longest device | Width dependent mobility |
| Step 3 | wvsat | IdVg strong inversion region for high drain curves | Width dependent velocity saturation |

# Stage 4: Low Drain Length extraction



| | Parameters adjusted | Target Regions | Behavior modelled |
|---|---|---|---|
| **Step 1** | lphig1 | Below Vt on all 3 low drain lengths for longest width device | Work function length dependence |
| **Step 2** | Lu0 | All 3 low drain lengths for longest width device | Length dependent mobility |
| **Step 3** | leu, lua, lua1,lucs,lprwg, lrdw, lrsw | Mobility/resistance region on all 3 low drain lengths for medium width device | Length dependent Source/drain extension resistance, front gate bias dependence on s/d resistance, coulomb scattering, phonon/surface roughness scattering |
| **Step 4** | Lu0, leu, lua, lua1,lucs,lprwg, lrdw, lrsw | All 3 low drain lengths above Vt and transconductance for longest width device | Length dependent source/drain resistance, and length dependent series resistance coefficient |
| **Step 5** | Lu0, leu, lua, lua1,lucs,lprwg, lud | All 3 low drain lengths, Above Vt and Strong inversion region for our longest width device | All of the above |

# Stage 5: High Drain Length extraction



| | Parameters adjusted | Target Regions | Behavior modelled |
|---|---|---|---|
| **Step 1** | leta0 | IdVg for all 3 High drain lengths for longest width device below Vt | Length scaling for drain induced barrier lowering |
| **Step 2** | lvsat,lmexp | IdVg for all 3 High drain lengths for longest width device strong inversion | Length scaling for velocity saturation and Smoothing for Vd saturation |
| **Step 3** | lvsat,lmexp, lpvag, lptwg, lksativ | IdVg for all 3 High drain lengths for longest width device above Vt and IdVd saturation region | Above, and length scaling for Strong inversion Vd saturat ion, Vg dependence on early voltage |
| **Step 4** | lvsat,lmexp, lpvag, lptwg, lksativ, leta0 | All 3 High drain lengths for longest width device and transconductance | All of the above |

# Extracted Parameter change at 3.8K from PDK values at T = 50K (eglvtnfet)

| Param | Behavior Modeled | % Change | Value change |
|---|---|---|---|
| u0 | Mobility | 3.9 | 0.002 M^(2)/V −s |
| ua | Mobility | 1599 | 24.8 (cm/MV)^(EU) |
| phig1 | Work function | 1.4 | 0.13 mV |
| cit | Subthreshold slope | 32279 | 0.003228 F /m^(2) |
| rdw/rsw | S/D resistance | -11.4 | -21 Ω−μ^(WR) |
| prwg | Gate bias<br>S/D resistance Dependence | 128.8 | 0.58 1/v |
| vsat | Saturation velocity | 2.9 | 830 m/s |