NO. 27

Technical Manual

L109

UNINTERRUPTIBLE 1PPS MODULE

V. TORRES

June 1994

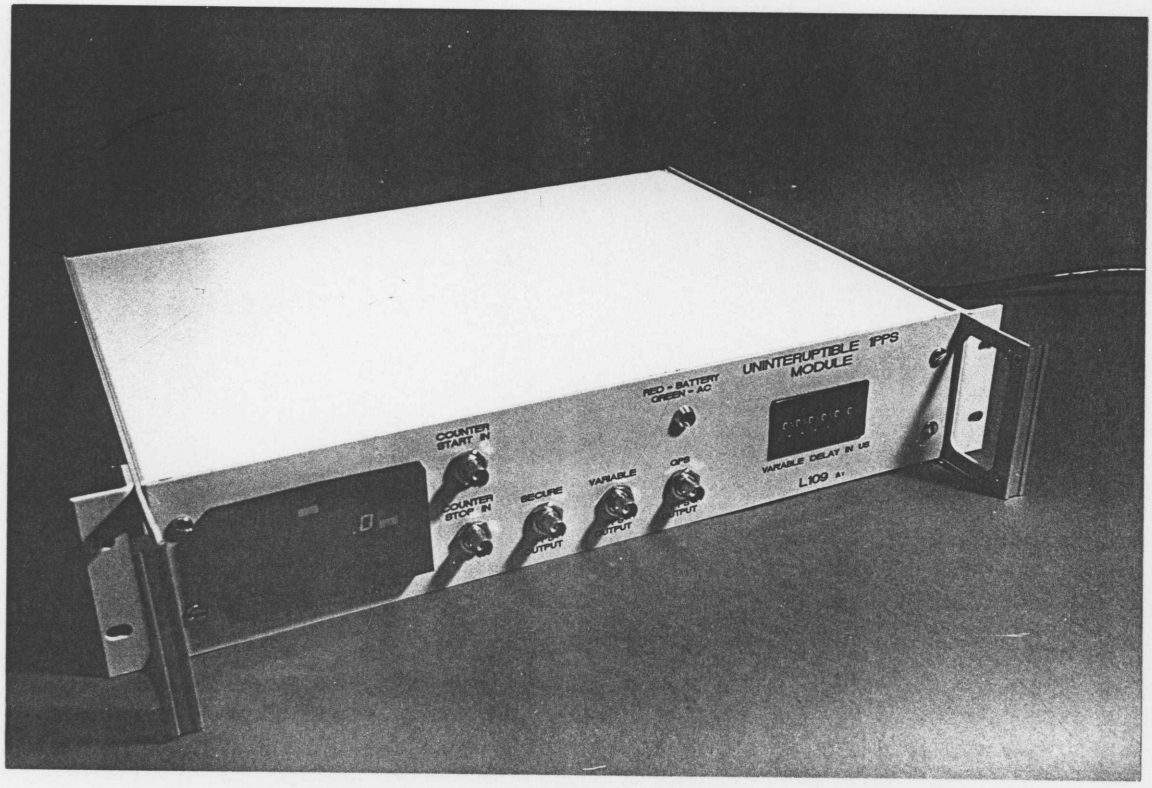


Table of Contents

I. General Description

The VLBA Uninterruptible 1PPS Module has four functions:

1. To provide a secure 1 Pulse Per Second (1PPS), 50 microsecond long timing pulse for synchronization purposes during power loss or other circumstances. The 1PPS output from the L109 is secure if and only if the MASER 5 MHz signal has not been interrupted and the L109 was previously in sync with the GPS. This is done by using the key switch on the rear panel to synchronize the L109 with the 1PPS output from the GPS. In case of power failure, the L109 has a battery backup which lasts about eighty hours, but the L109 is restricted to the six hour battery life of the MASER.

2. To provide a variable delay 1PPS output to be used with the counter to verify the L109 is in sync with the GPS 1PPS.

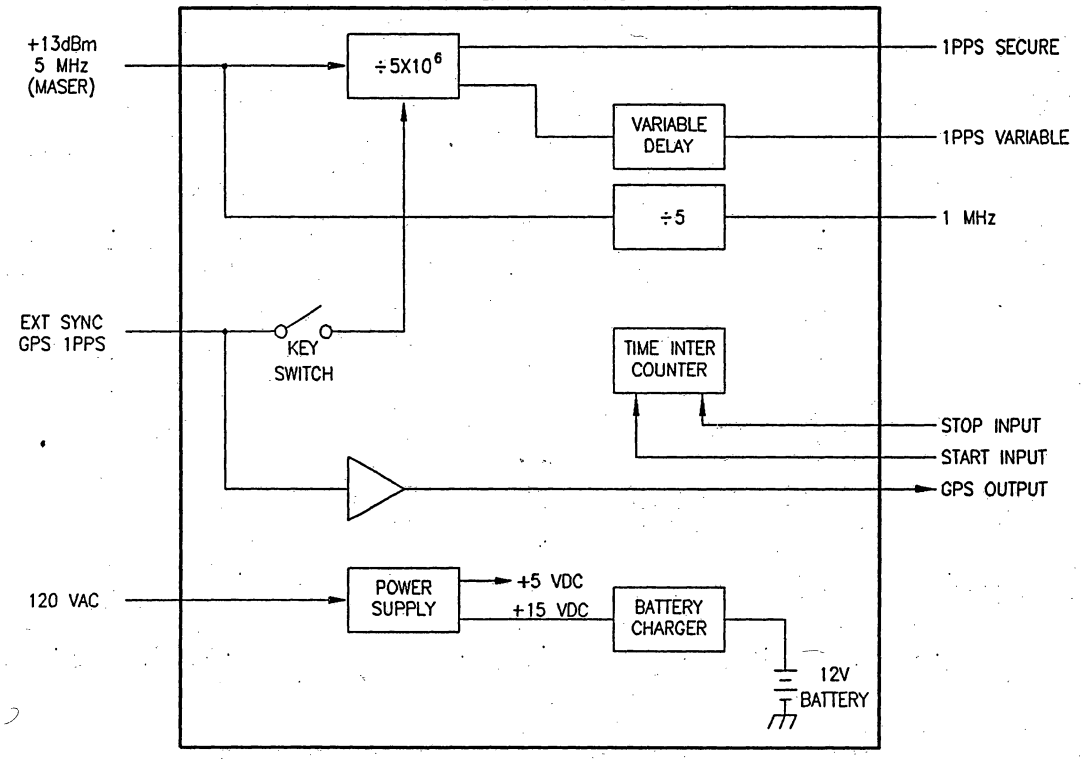
3. To provide a sample of the GPS 1PPS output.

4. To provide a 1 MHz output for use by any extra systems.

The L109 is a positive edge triggered device whose outputs consist of a Secure 1PPS (50 μs wide), a Variable 1PPS (50 μs wide), a GPS 1PPS Output (75 μs wide), and a 1 MHz output. The Secure and Variable 1PPS outputs appear on both the front and rear panels. The 1 MHz output appears on the rear panel and the GPS 1PPS output appears on the front panel. The inputs consist of a 5 MHz MASER and the GPS 1PPS rear panel inputs. The rear panel also has a Reset Secure Key Switch to sync the Secure 1PPS with the GPS 1PPS. The front panel has a universal counter-timer with inputs for start and stop times. A digital thumbwheel switch is also located on the front panel to control the variable delay in microseconds. The module also contains two 6 V batteries connected in series. In case of power loss, the batteries will guarantee the Secure 1PPS is still in sync with the GPS 1PPS, given that no interrupt from the MASER occurs. If power is lost, the counter will not be provided power and therefore cannot be used to verify the L109 has not lost sync.

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	7-94	K. TATE	L. BENO	ADDED 1 MHZ, GPS OUT

L109
UNINTERRUPTIBLE 1PPS



ACAD : 53311K01

D53311S002	SCHEMATIC
A53311B002	BOM
D53311A003	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLBA PROJECT: L109 UNINTERRUPTIBLE 1PPS MODULE

TITLE: L109 UNINTERRUPTIBLE 1PPS MODULE BLOCK DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	ANDREATTA	DATE 4-92
DESIGNED BY	BENO	DATE 4-92
APPROVED BY	BENO	DATE 4-92

SHEET NUMBER 1 OF 1 | DRAWING NUMBER B53311K001 | REV. A | SCALE NONE

II. Circuit Description

A. 1 MHz Output

The 5 MHz sine wave input from the MASER is first converted to a 5 MHz square wave. The 5 MHz square wave is then used as the clock for the divide by 2 and 5 counters (U9). A 1 MHz square wave is produced on pin 10 of U9 and is put through an inverter and used as the enable lines for two D Flip Flops, U11. The clock for the first F/F in U11 is the 5 MHz square wave. The first F/F in U11 produces a 1 MHz output, is inverted twice and is used as the clock for the second F/F in U11. The output of the second F/F in U11 is a 1 MHz signal with a 50% duty cycle. This signal is then sent through U4, a 50Ω line driver.

B. GPS 1PPS Out

The GPS 1PPS input is used as the clock for F/F, U12. The inverted output of U12 is sent through U4 (a 50 Ω line driver) resulting in a 4 V, 75 μs, GPS 1PPS output. This GPS 1PPS output is the same as the GPS 1PPS input with a delay of 94 ns.

C. Secure 1PPS Out

The 5 MHz signal is run into the divider chip, U9. The biquad output is then inverted and put through a NAND gate (U8) with the inverted 5 MHz square wave. The output of U8 is used as the clock of the first Flip Flop in U6 (pin 11). The output of the last of six decade counters (U13 pin 12) is a 1 Hz signal which is used to clock the second F/F in U6 (pin 3). The output of the first F/F in U6 (pin 5) is used as the data line for the second Flip Flop in U6 (pin 12). The inverted output of the first F/F in U6 (pin 8) is sent through a NOR gate (U3, a 50Ω line driver), which with the other input tied to ground, gives

a 50 μs pulse every second. Pin 1 of U3 goes to the rear panel while pin 4 of U3 goes to the front panel.

D. GPS/Secure Sync Circuit

The noninverted output, Q, of F/F U12 (pin 9) is used as the clock for the F/F U5 (pin 3). The noninverted output of U5 controls the clear line of the decade counters, U13-U18 and the divider chip, U9. These pins are active high, so the counters are not reset until the key is turned. When the key is turned, the counters (active low) are reset restarting the Secure and Variable 1PPS. The counters are then restarted when the key is released and the clock for second F/F in U5 (pin 3) receives a logic high from the GPS.

E. Variable 1PPS

The Digitran Digital Switch chooses the delay to be given to the variable 1PPS output. (from 1 μs to 999999 μs) The carry out bit of the SW7, SW6, SW5, and SW4 are sent through a NAND Gate (U7). The carry out bit of SW3 and SW2 along with the biquad output of the divider (U9) and the 5 MHz square wave are put through a NAND gate. The output of these two are sent through a NOR Gate (U8) resulting in a 100 ns wide 1 Hz pulse. This pulse is used as the clock for another D Flip Flop (U12). The inverted output of U12 is now a 1 Hz signal with 70 μs low pulse. This signal is then put through U4, a 50Ω line driver, to get a 50 μs positive pulse. The module can be expanded to include two more outputs of either Variable or Secure 1PPS by connecting the jumper to U3 pin 12. These outputs would be the same as the previous Variable or Secure 1PPS outputs.

F. Battery Charger

The battery charger circuitry is constructed in a constant voltage charger

configuration. The circuit allows for a small trickle current to charge the batteries at all times. The continuous trickle charge will balance all the cells equally. The power transistor regulates the amount of current going to the batteries. The circuit is designed to have a 200 mA, 14.4 V maximum. When AC power is lost, the batteries run the module. The diode D4 protects the power supplies from getting any back current from the batteries. The LEDs on the front panel verify whether the power supplies (green LED) or the batteries (red LED) are running the module.

G. Batteries

The batteries have a shelf life of 6-9 months at room temperature before they must be recharged. Two batteries are connected in series; each are 6 V, 2.0 Amp-hour batteries. The circuit (not including the counter) draws about 18 mA, so the batteries will last around 80 hours. However, the MASER batteries will only last six hours, so if power is lost for more than six hours the L109 will not receive the required 5 MHz signal to run the module and will not be able to produce the Secure 1PPS. Under the conditions of use in the L109, the batteries should be replaced every 5 years.

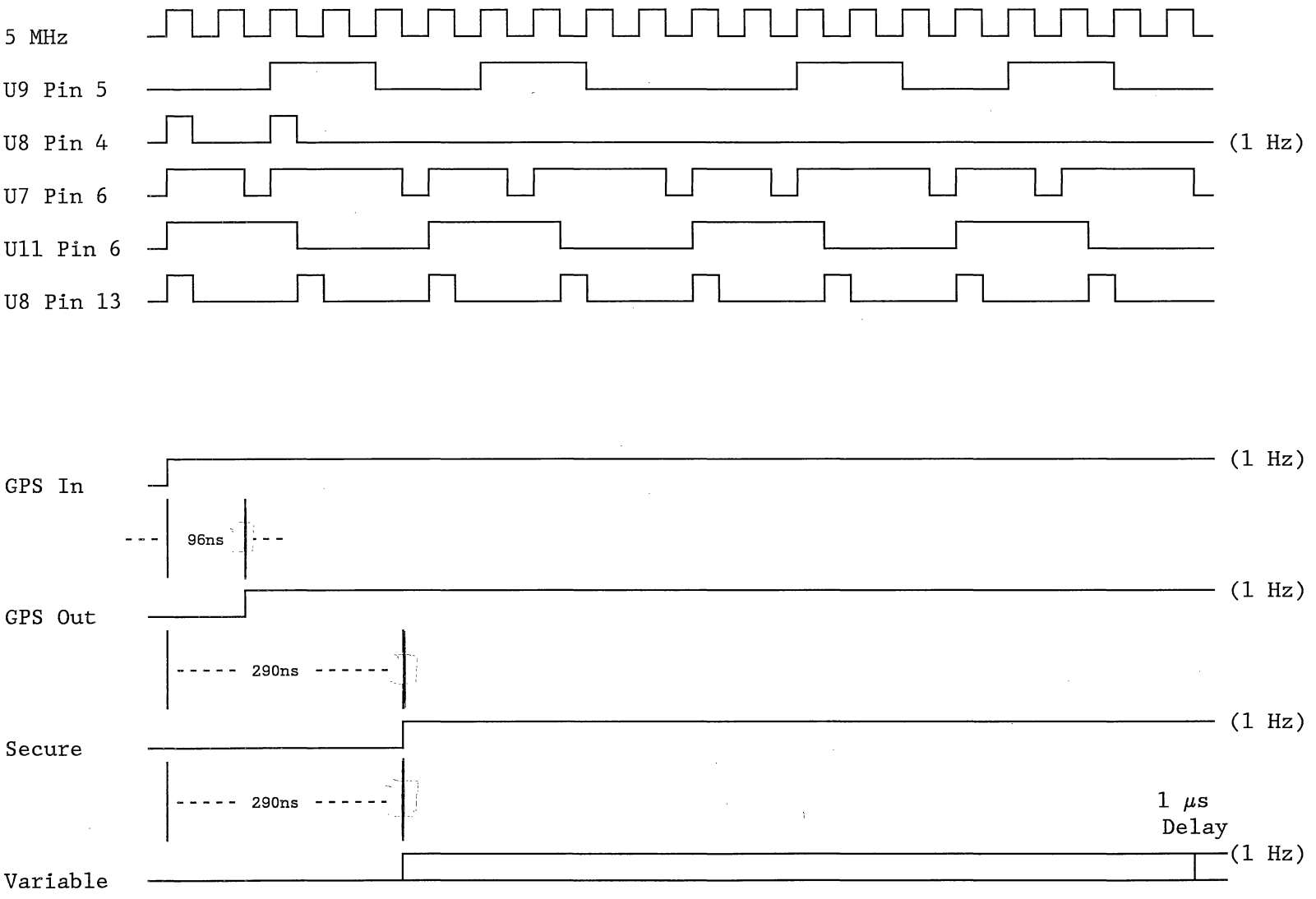


Figure 1: Waveforms of the L109

III. Test Procedure

REQUIREMENTS:

1. Oscilloscope. Storage capability is not required but makes measurement of the 50 microsecond pulse with repetition rate of once per second easier.

2. 1PPS from GPS or a function generator, capable of producing TTL-level square or pulse waveforms. If function generator is used, it should be set to a positive pulse or square wave at 1 Hz. The level should be TTL (0.2 V low, 4.0 V high).

3. MASER 5 MHz connection (4 to 13 dBm).

4. GPS 1PPS Output connected to the Counter Start In jack. Secure 1PPS or Variable 1PPS connected to the Counter Stop In jack.

The module is checked most easily while still in the C-rack, however, it can be checked on a bench by connecting appropriate inputs, and injecting a 5 MHz signal. Make sure the length of all pulses are as stated in this document.

I. Check that a positive TTL-level pulse appears at the front panel GPS 1PPS Output (75 μs), the Secure 1PPS Output (50 μs) and the Variable 1PPS Output (50 μs).

II. Check that a 1 MHz TTL signal appears at the 1 MHz Output jack on the rear panel.

III. Check the counter measurement.

Initially, the counter will read a very large number. Insert the key into the key switch located on the rear panel and turn and hold for about 3 seconds. Turn key back to original position and remove the key. The counter should now read a number ≤ .3 μs. If the number on the counter is any larger, insert key and repeat process. If the number is still large, reverse the Counter Start and Stop connections. If the counter still does not read a number ≤ 0.3 μs, return the Counter Start and Stop connections to their original position. The counter does not have nanosecond resolution, so the Variable 1PPS must be used. If it is not already connected, connect the Variable 1PPS Output to the Counter Stop jack. Using the Thumbwheel Switch, rotate the 1 μs wheel until it reads "1". The counter now will have a reading of "1._". A delay of 1 μs has just been put on the Variable 1PPS Output. The number located after the decimal is the delay of the Secure 1PPS Output and should still be ≤ 0.3 μs.

IV. Front Panel Connections

1. GPS 1PPS — (BNC Connector OUTPUT). Sample of the 1 Pulse Per Second Generated by the GPS. This can be hooked up to the Counter Start In or Counter Stop In and compared with the Secure 1PPS depending on which is leading.

2. Variable 1PPS — (BNC Connector OUTPUT) Variable 1 Pulse Per Second. If the comparison between the GPS 1PPS and the Secure 1PPS on the counter gives large numbers, this output should be connected to the counter as stated in the test procedures and the signal should be delayed by using the Thumbwheel Switch.

3. Secure 1PPS — (BNC Connector OUTPUT) Secure 1 Pulse Per Second. The circuit has a minimum delay of 280 ns. Once the L109 is synchronized with the GPS, the signal may have a slightly larger delay due to the MASER drifting or the GPS data being updated.

4. Counter Start In — (BNC Connector INPUT) Tells the counter where to begin its count. Counter is set up to begin count on the rising edge.

5. Counter Stop In — (BNC Connector INPUT) Tells counter where to end its count. Counter is set up to end count on the rising edge.

V. **Rear Panel Connections**

1. GPS 1PPS In — (BNC Connector INPUT) The 1 Pulse Per Second Output from the GPS should be connected.

2. 5 MHz Input — (BNC Connector INPUT) The 5 MHz signal from the MASER is to be connected.

3. 1 MHz Out — (BNC Connector OUTPUT) 1 MHz signal output.

4. Variable 1PPS — (BNC Connector OUTPUT) Variable 1 Pulse Per Second Output. Can be delayed from 1 μs to 999999 μs by using the Thumbwheel switch on the front panel.

5. Secure 1PPS — (BNC Connector OUTPUT) Secure 1 Pulse Per Second Output. Same as Secure 1PPS Output on front panel.

6. Reset Secure — (Key Lock) Key inserted and turned in order to synchronize GPS 1PPS input with Secure 1PPS output.

VI. Specifications

Primary clock input from MASER:	
Frequency	5 MHz
Wave form	Sine wave
Level	.353 to 1.0 VRMS (+4 to +13 dBm)
Input Impedance	50 Ω
1PPS input from GPS:	
Frequency	1 Hz
Signal Type	TTL, any duty cycle
Polarity	Positive
Rear Panel Outputs:	
Secure 1PPS (Frequency)	50 μs positive pulse (1 Hz) Minimum 280 ns delay from GPS 1PPS
Variable 1PPS (Frequency)	50 μs positive pulse (1 Hz) Minimum 280 ns delay from GPS 1PPS
1 MHz Output	50% Duty Cycle
Front Panel Outputs:	
Secure 1PPS	Same as above
Variable 1PPS	Same as above
GPS 1PPS	75 μs positive pulse (1 Hz) 96 ns delay from GPS 1PPS Input
Batteries:	
Type	6 V Sealed Rechargeable Lead Acid
Current	18 mA
Recharge Time	20 Hours typically
Shelf Life	6-9 Months
Service Life	5 Years
Power Supply:	
Voltage	5 V 15 V
Current Drain	5 V: 100 mA (When batteries charged) 78 mA (When batteries not charged) 15 V: 30 mA (When batteries charged) 100 mA (When batteries not charged)

VII. Bill of Materials

Item #	Ref Design	Manufacturer	MFG Part #	Description	Total Qty.
1	-	NRAO	DWG# D53311A003	L109 Module Assy	-
2	-	NRAO	DWG# D53311A003	L109 Module Assy BOM	-
3	-	NRAO	DWG# D53311S002	L109 Module Schematic	-
4	-	NRAO	DWG# D53311M004	L109 Module Drill Dwg.	-
5	-	NRAO	DWG# D53311I002	L109 Module Silkscreen	-
6	-	NRAO	DWG# D53311A004	Delay Circuit PCB Assy	-
7	-	NRAO	DWG# C13230M02-1	Battery Holder	1
8	-	NRAO	DWG# C13230M02-2	Battery Holder Post	3
9	-	BUD	HC-14101	Electronic Cabinet	1
10	SW2-SW7	DIGITRAN	23031-6	Switch Assembly	1
11	-	DATEL	PC-6	Universal Counter-Timer 10 MHz	1
12	-	CORCOM	3EPI (case EP1)	EMI Filter	1
13	PS1	LAMBDA	LSS-34-5	5 VDC Power Supply	1
14	PS2	LAMBDA	LSS-34-15	15 VDC Power Supply	1
15	B1,B2	POWER SONIC	PS-620	Battery Gel Cell	2
16	-	BELDEN	17612	Electronic Cord 18/3 AWG	1
17	-	SPC TECHNOLOGY	SRR-20	Cord Strain Relief	1
18	SW1	AUGAT ALCO SWITCH	SWK-13-1	Security Key Switch	1
19	-	AMPHENOL	31-318	BNC Connector	9
20	-	RADIO SHACK	276-025	Red/Green LED	1
21	-	OMNI SPECTRA	3004-7941-00	Type "N" Connector	1
22	-	LITTLE FUSE	345603A	Fuse Holder	1
23	-	LITTLE FUSE	36201.5	1.5A, 250V Fast Blow Fuse	1
24	-	3M	3302/14	4" Flat Cable Scotch Flex	6
25	J23-J28	3M	3385-6000	Connector Socket	6
26	-	KEYSTONE	1623-2	Electronic Standoff	4
27	-		#6-32 X ¼"	SS Pan Head Screw	12
28	-		#6-32 X ¼"	SS Flat Head Screw	4
29	-		#4-40 X ¼"	SS Pan Head Screw	4
30	-		#4-40 X ½"	SS Pan Head Screw	2
31	-	THERMALLOY INC.	#4880	Mounting Kit	1
32	-		#6-32	SS Hex Nut	6
33	-		#6	Ext. Tooth Lock Washer	6
34	-	SPC TECHNOLOGY	CFS-TO-1418-HT	Quick Disconnect Terminal	4
35	-	SPC TECHNOLOGY	CBS-DY-1806	Spade Terminal	10

Item #	Ref Design	Manufacturer	MFG Part #	Description	Total Qty.
36	-	ALPHA	FIT221V-¼	¼" Shrinkable Tubing	4
37	-	ALPHA	FIT221V-⅜	⅜" Shrinkable Tubing	1
38	-		RG188/U	Coax Wire	
39	-		RG402/U	Semi Ridged RF Cable	

VIII. Temperature Test

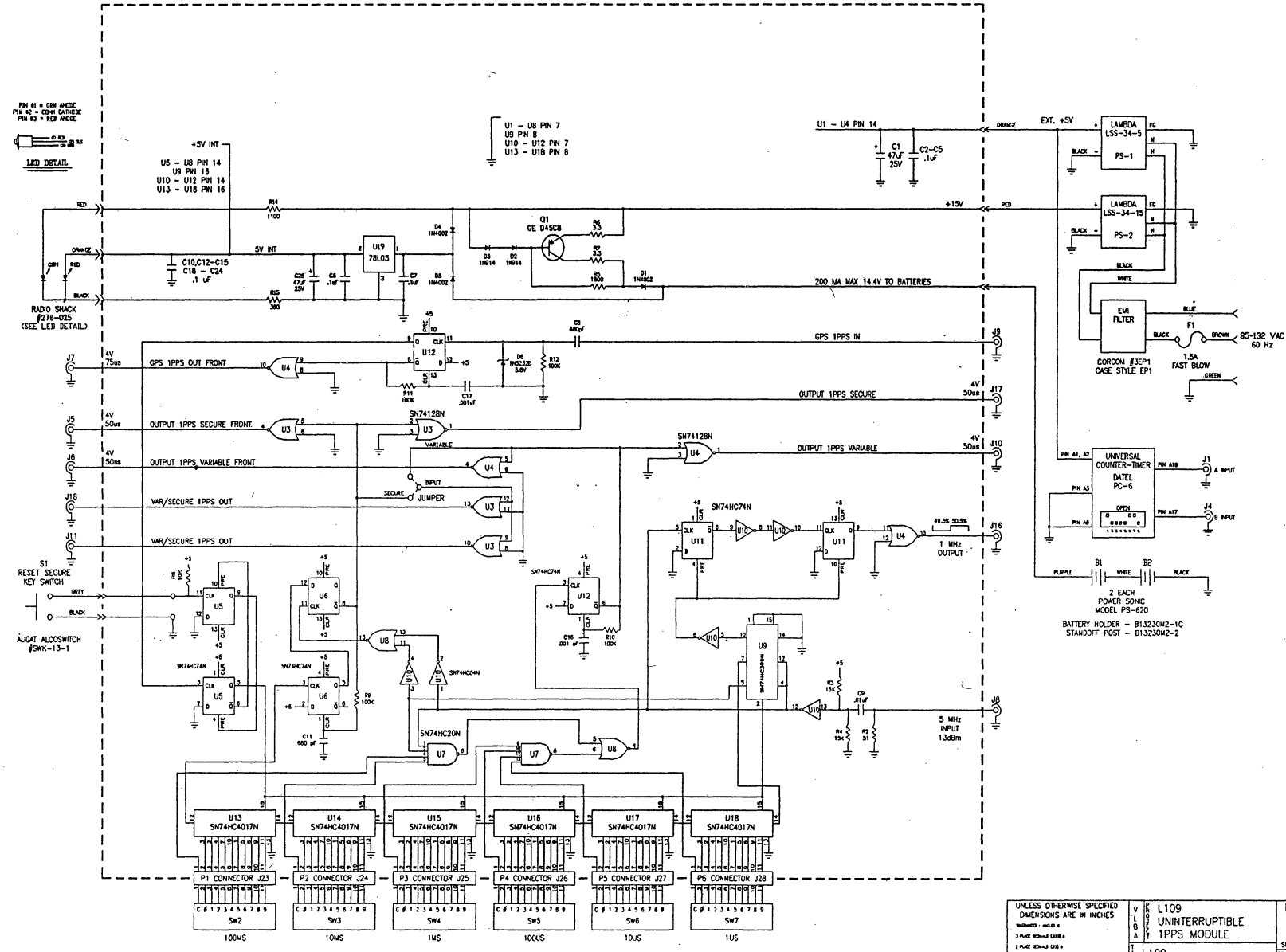
The L109 was subjected to a temperature test to see how much the temperature affected the Secure 1PPS and Variable 1PPS Outputs. The delay given is the delay between the Secure 1PPS output of an L109 at room temperature and the Secure and Variable 1PPS Outputs of an L109 in a temperature chamber. The L109 in the temperature chamber was started out at room temperature and then heated, cooled off to a low temperature and then heated and cooled again. The Variable 1PPS was only run through the same test (with the 10 μs switch set to 1) once because the delay change was the same. The initial delay at room temperature is due to the L109 not being synchronized exactly with the GPS and the internal delay of the L109. The change in delay (ns) versus the change in temperature (°C), $\Delta t / \Delta T \approx .15$ ns per °C.

Secure		**10 μs Variable**	
Temperature (°C)	**Delay (ns)**	**Temperature (°C)**	**Delay (μs)**
8.72	97	8.82	10.100
10.14	97	24.16	10.102
16.63	98	24.54	10.102
24.18	99	41.94	10.104
25.58	99		
26.31	99		
30.10	100		
42.00	101		
44.8	101		
48.32	102		

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	7-94	K. TATE	L. BENO	MINOR CORRECTIONS

NOTES :

1. ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED.
2. SW2 THRU SW7 ARE DIGITRAN DIGITAL SWITCH #23031-6.



ACAD : 53311S02

953311K001	BLOCK DIAG
±53311B002	BOM
053311A001	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

PROJECT: L109 UNINTERRUPTIBLE 1PPS MODULE

TITLE: L109 UNINTERRUPTIBLE 1PPS MODULE SCHEMATIC DIAGRAM

SHEET NUMBER 1 or 1

DRAWING NUMBER D53311S002

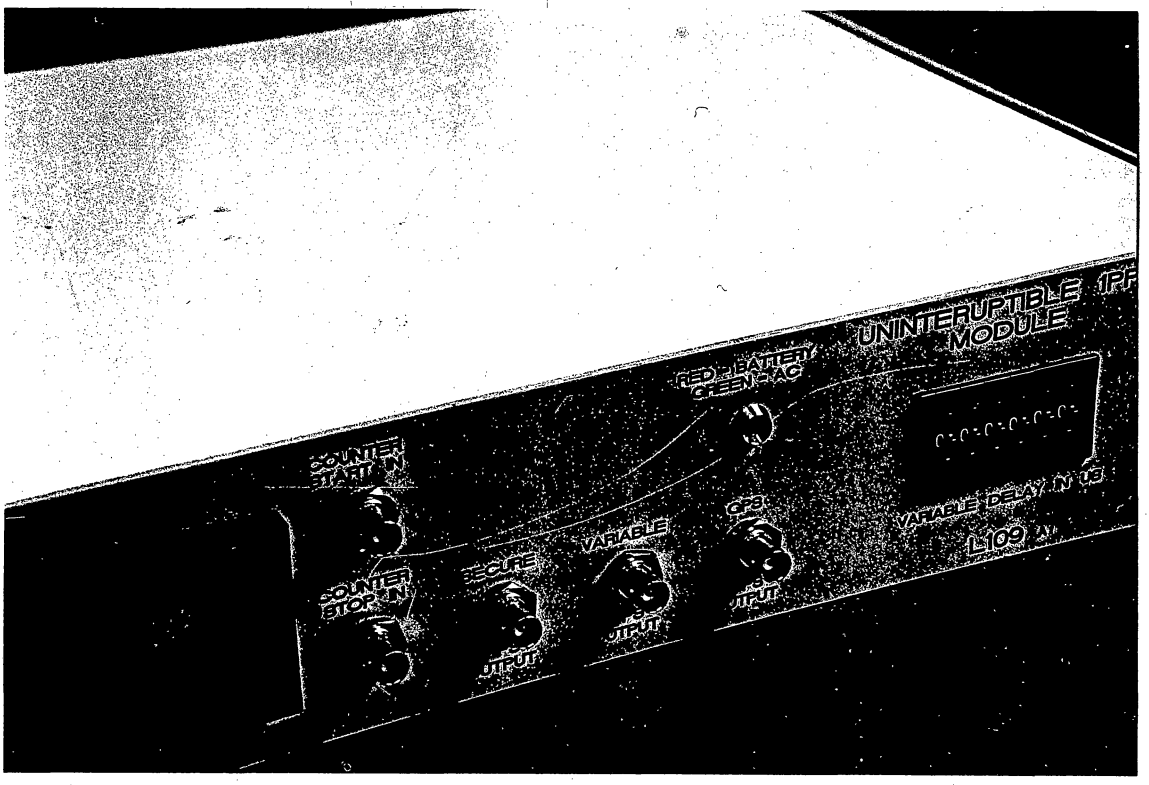
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	ANDREATTA	DATE 6-89
DESIGNED BY	HONEYWELL	DATE 5-89
APPROVED BY	L. BENO	DATE 6-89

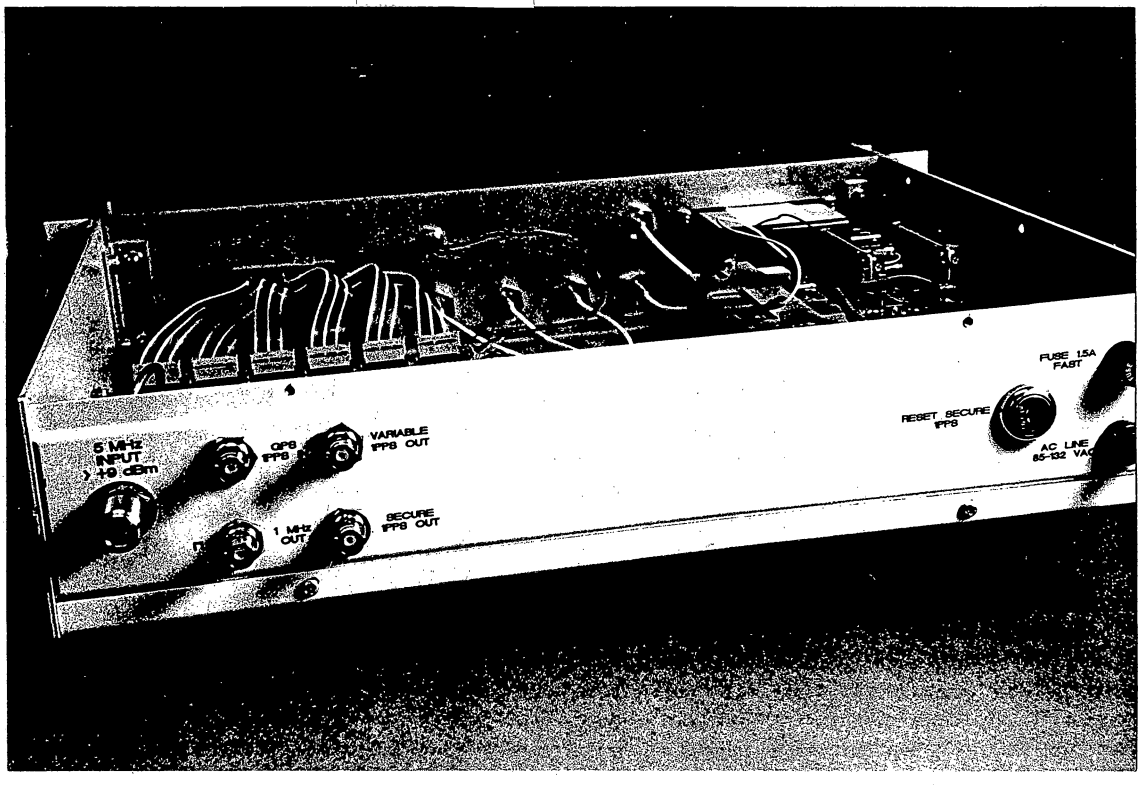
REV. A SCALE NONE

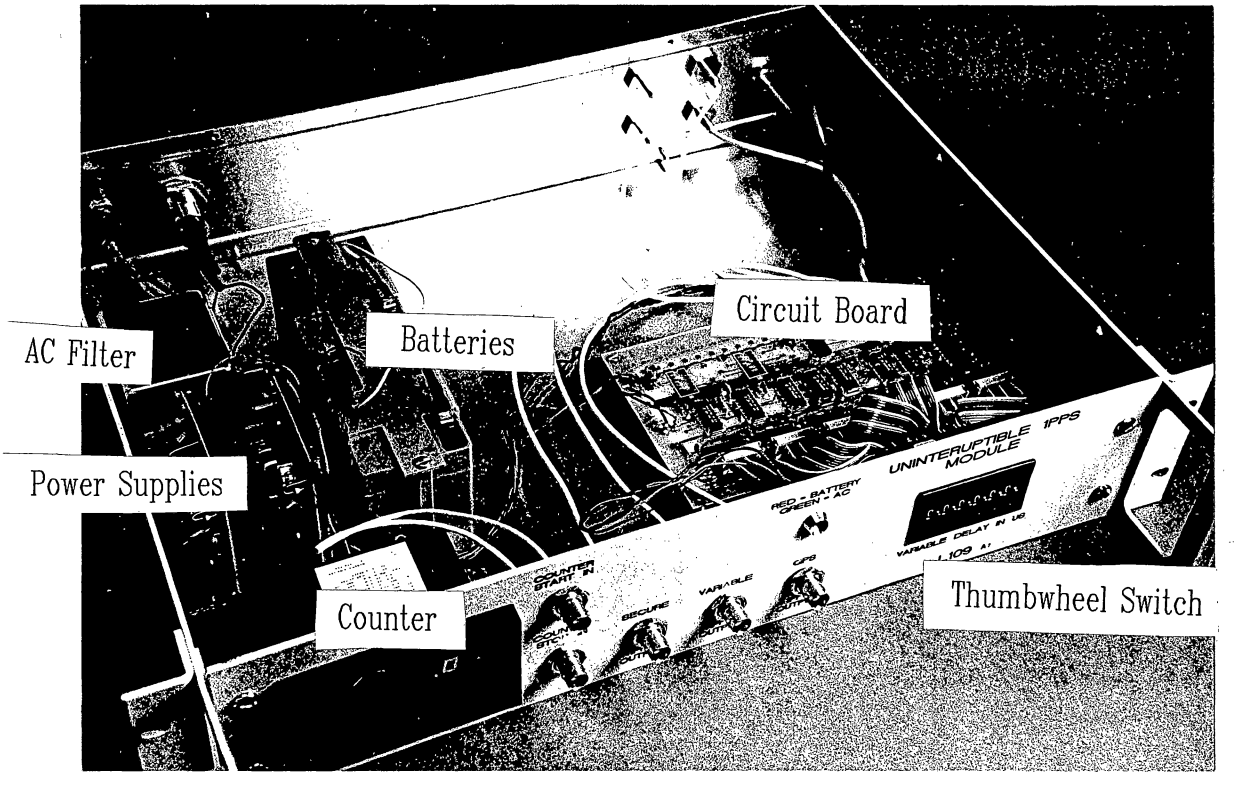
X. **Photos**

Front View



Back View





Internal View

XI. Module Drawing List

Description	Number
Module Assembly	D53311A003
Delay Circuit PCB Assembly	D53311A004
Bill of Materials	A53311B002
Silkscreen Front and Rear Panels	D53311I002
Delay Circuit PCB Silkscreen	D53311I003
Module Block Diagram	B53311K001
Module Drill Drawing	D53311M004
Delay Circuit PCB Drill Drawing	D53311P001
Delay Circuit PCB Artwork	D53311Q001
Module Schematic Diagram	D53311S002

XII. Data Sheets

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

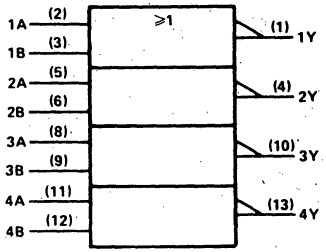
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A+B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54HC02 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC02 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

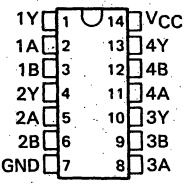
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

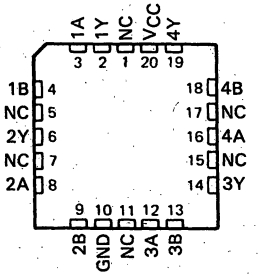


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HC02 . . . J PACKAGE
SN74HC02 . . . D OR N PACKAGE
(TOP VIEW)

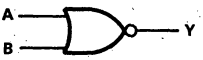


SN54HC02 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



D2953, JULY 1986—SEPTEMBER 1987

- Inputs are TTL-Voltage Compatible
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

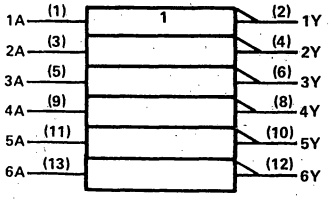
These devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$.

The SN54HCT04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT04 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

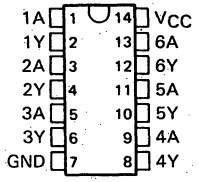
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†

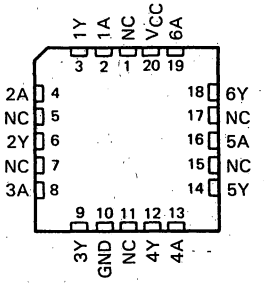


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

SN54HCT04 . . . J PACKAGE
SN74HCT04 . . . D OR N PACKAGE
(TOP VIEW)



SN54HCT04 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

D2684, DECEMBER 1982 – REVISED SEPTEMBER 1987

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

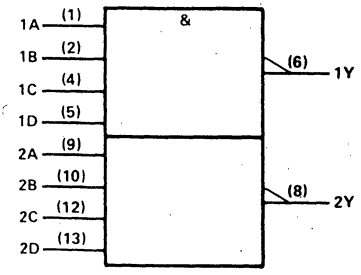
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54HC20 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC20 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

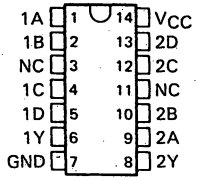
logic symbol†



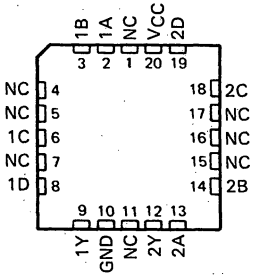
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54HC20 . . . J PACKAGE
SN74HC20 . . . D OR N PACKAGE
(TOP VIEW)

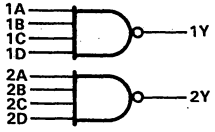


SN54HC20 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



- **Inputs are TTL-Voltage Compatible**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

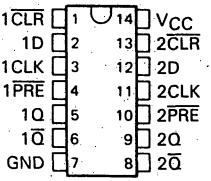
The SN54HCT74 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT74 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

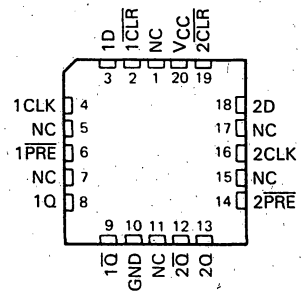
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when Preset or Clear returns to its inactive (high) level.

SN54HCT74 . . . J PACKAGE
SN74HCT74 . . . D OR N PACKAGE
(TOP VIEW)

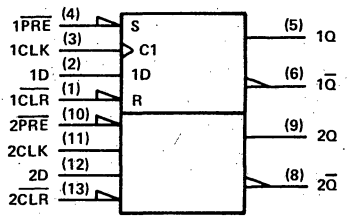


SN54HCT74 . . . FK PACKAGE
(TOP VIEW)



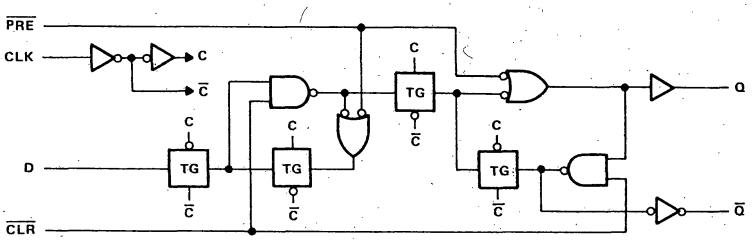
NC—No internal connection

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram, each flip-flop (positive logic)



D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

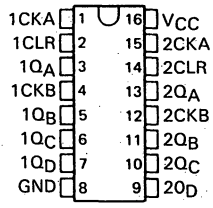
- 'HC390...Individual Clock for A and B Flip-Flops Provide Dual ÷ 2 and ÷ 5 Counters
- 'HC393...Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

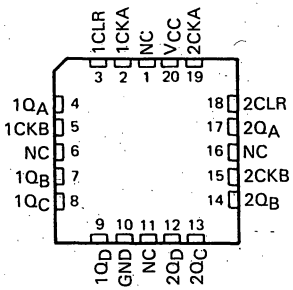
Each of these monolithic circuits contains eight flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'HC390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a biquinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'HC393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The 'HC390 and 'HC393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

The SN54HC390 and SN54HC393 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC390 and SN74HC393 are characterized for operation from −40°C to 85°C.

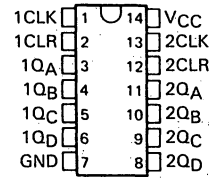
SN54HC390 . . . J PACKAGE
SN74HC390 . . . DW OR N PACKAGE
(TOP VIEW)



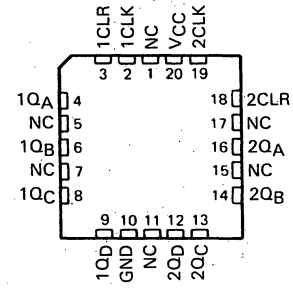
SN54HC390 . . . FK PACKAGE
(TOP VIEW)



SN54HC393 . . . J PACKAGE
SN74HC393 . . . N PACKAGE
(TOP VIEW)

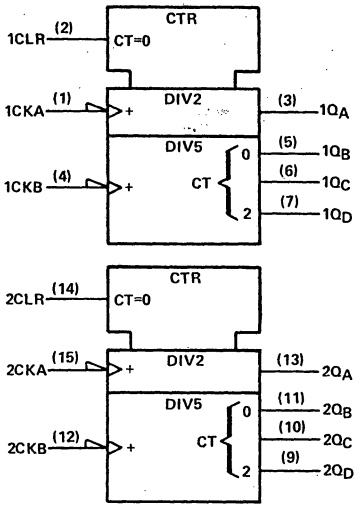


SN54HC393 . . . FK PACKAGE
(TOP VIEW)



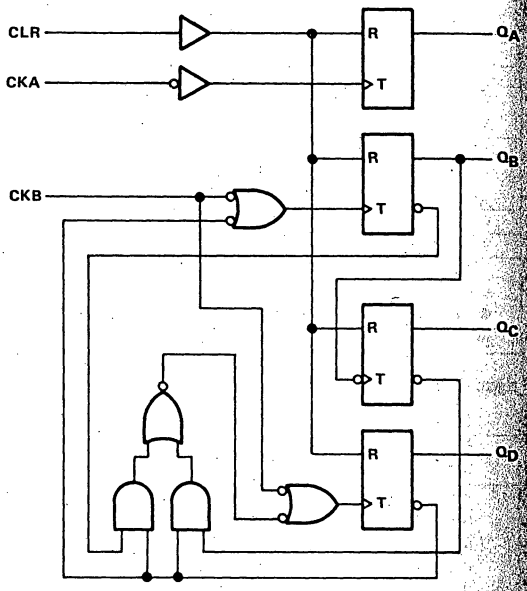
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram, each counter (positive logic)



FUNCTION TABLES

BCD COUNT SEQUENCE (EACH COUNTER) (See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BIQUINARY (5-2) (EACH COUNTER) (See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Notes: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for biquinary count.
H = high level, L = low level.

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D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- **Carry-Out Output for Cascading**
- **Divide-by-N Counting**
- **DC Clock Input Circuit Allows Slow Rise Times**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

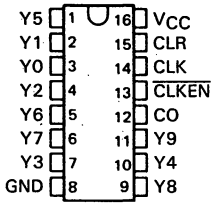
description

The 'HC4017 is a 5-stage divide-by-10 Johnson counter with ten decoded outputs and a carry-out bit. High-speed operation and spike-free outputs are obtained by use of the Johnson decade counter configuration.

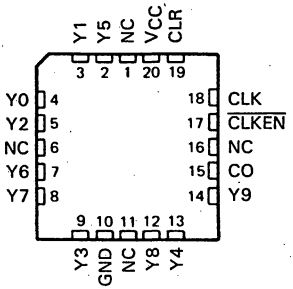
The ten decoded outputs are normally low and go high only at their respective decimal time periods. A high signal on CLR asynchronously clears the decade counter and sets the carry output and Y0 high. With $\overline{\text{CLKEN}}$ low, the count is advanced on a low-to-high transition at CLK. Alternatively, if CLK is high, the count is advanced on a high-to-low transition at $\overline{\text{CLKEN}}$. Each decoded output remains high for one full clock cycle. The carry output CO is high while Y0, Y1, Y2, Y3, or Y4 is high, then is low while Y5, Y6, Y7, Y8, or Y9 is high.

The SN54HC4017 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4017 is characterized for operation from −40°C to 85°C.

SN54HC4017 . . . J PACKAGE
SN74HC4017 . . . DW OR N PACKAGE
(TOP VIEW)

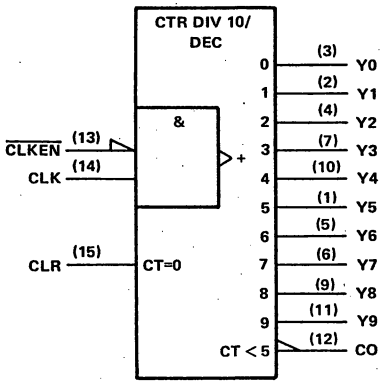


SN54HC4017 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

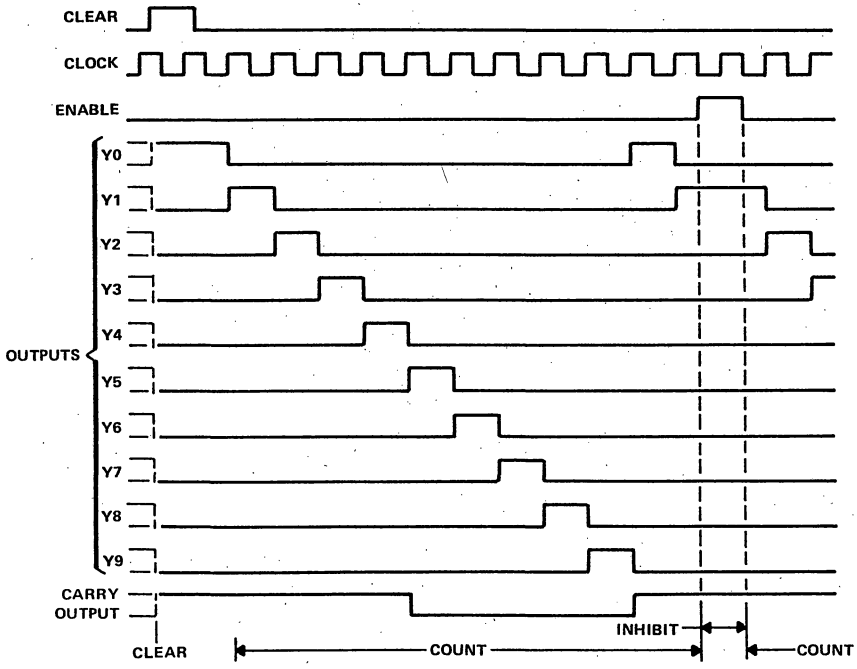
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

typical clear, count, and inhibit sequences



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

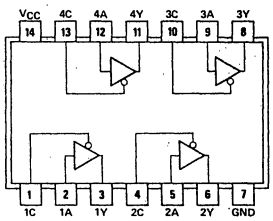
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

125

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

positive logic:
Y = A
Output is off (disabled) when C is high.

See page 142



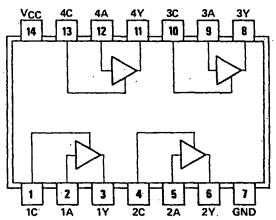
SN54125/SN74125(J, N, W)

126

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

positive logic:
Y = A
Output is off (disabled) when C is low.

See page 142



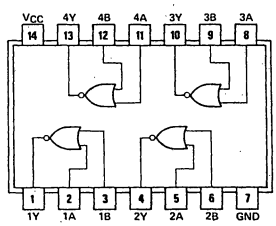
SN54126/SN74126(J, N, W)

128

SN54128 . . . 75-OHM LINE DRIVER
SN74128 . . . 50-OHM LINE DRIVER

positive logic:
$Y = \overline{A+B}$

See page 104



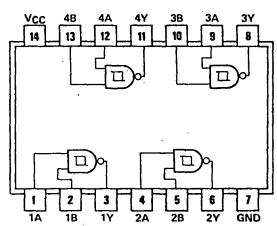
SN54128/SN74128(J, N, W)

132

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

positive logic:
$Y = \overline{AB}$

See page 98



SN54132/SN74132(J, N, W)
SN54S132/SN74S132(J, N, W)

TEXAS INSTRUMENTS
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recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '128 MIN	NOM	MAX	SERIES 54S / SERIES 74S 'S140 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−29			−40	mA
	74 Family			−42.4			−40	
Low-level output current, I_{OL}				48			60	mA
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 / SERIES 74 '128 MIN	TYP‡	MAX	SERIES 54S / SERIES 74S 'S140 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1, 2			2			2			V
V_{IL}	Low-level input voltage	1, 2					0.8			0.8	V
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §				−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −2.4 mA	54 Family	2.4	3.4					V
				74 Family	2.4	3.4					
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = −13.2 mA		2.4						
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = MAX		2						
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −3 mA	54 Family				2.5	3.4		
				74 Family				2.7	3.4		
			V_{CC} = MIN, V_{IL} = 0.5 V, R_O = 50 Ω to GND					2			
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX			0.26	0.4			0.5	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40				μA
				V_{IH} = 2.7 V						100	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6				mA
				V_{IL} = 0.5 V						−4	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		−70		−180	−50		−225	mA
I_{CC}	Supply current, Total, outputs high	7	V_{CC} = MAX			12	21		10	18	mA
	Supply current, Total, outputs low					33	57		25	44	
	Supply current, Average per gate		V_{CC} = 5 V, 50% duty cycle			5.63			8.75		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_I = −12 mA for '128 and −18 mA for 'S140.
♦Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second for '128 or 100 milliseconds for 'S140.

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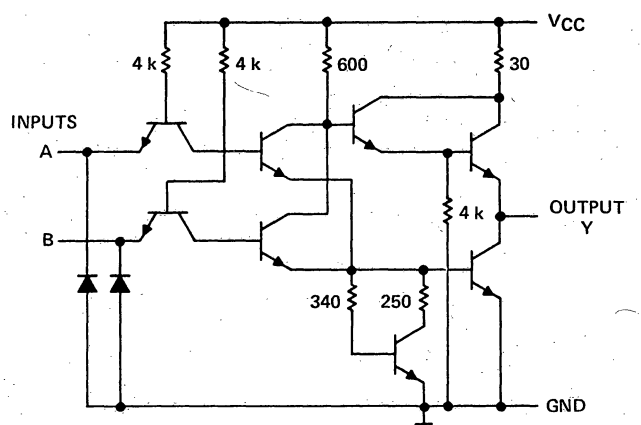
switching characteristics, V_{CC} = 5 V, T_A = 25°C

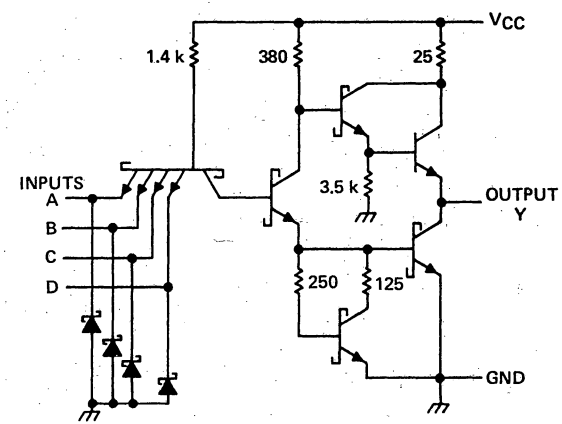
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'128	C_L = 50 pF, R_L = 133 Ω		6	9		8	12
	C_L = 150 pF, R_L = 133 Ω		10	15		12	18
'S140	C_L = 50 pF, R_L = 93 Ω	2	4	6.5	2	4	6.5
	C_L = 150 pF, R_L = 93 Ω		6			6	

#Load circuit and voltage waveforms are shown on page 148.

schematics (each driver)



'128 CIRCUITS



'S140 CIRCUITS

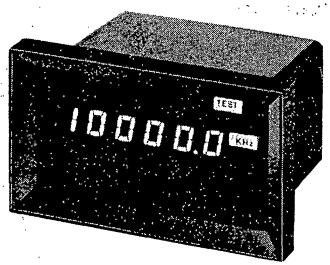
Resistor values shown are nominal and in ohms.

PC-6
Programmable 10 MHz Counter-Timer

DATEL

FEATURES

- **Performs five functions: unit counter, frequency counter, sub-second period counter, frequency ratio counter, and sub-second interval timer**
- **Offers four full-scale ranges to measure frequency and time (period and interval)**
- **All functions, ranges, and input slopes programmable using TTL-compatible inputs or front-access command switches**
- **6-digit LED display with descriptors**



GENERAL DESCRIPTION

The DATEL PC-6 is a low cost, ultra-compact, programmable 10 MHz Universal Counter-Timer. Frequency and time measurements are displayed on a 6-digit, .3" high Light Emitting Diode (LED) display. The counter is housed in a panel-mount polycarbonate short depth case.

Frequency measurements to 10 MHz can be made using an internal crystal timebase (Frequency Counter function, with the measured Frequency display in kHz), or with an external timebase (Frequency Ratio Counter where FA/FB is displayed). The PC-6 can also function as a Unit Counter, a Sub-Second Period Timer (single input, measuring the period of a single waveform), or a Sub-Second Interval Timer (dual input, measuring the time period from a start pulse on Input A to a stop pulse on Input B). Four ranges for each function permit resolution on frequency measurements to .1 Hz and resolution on time measurements to 100 pS.

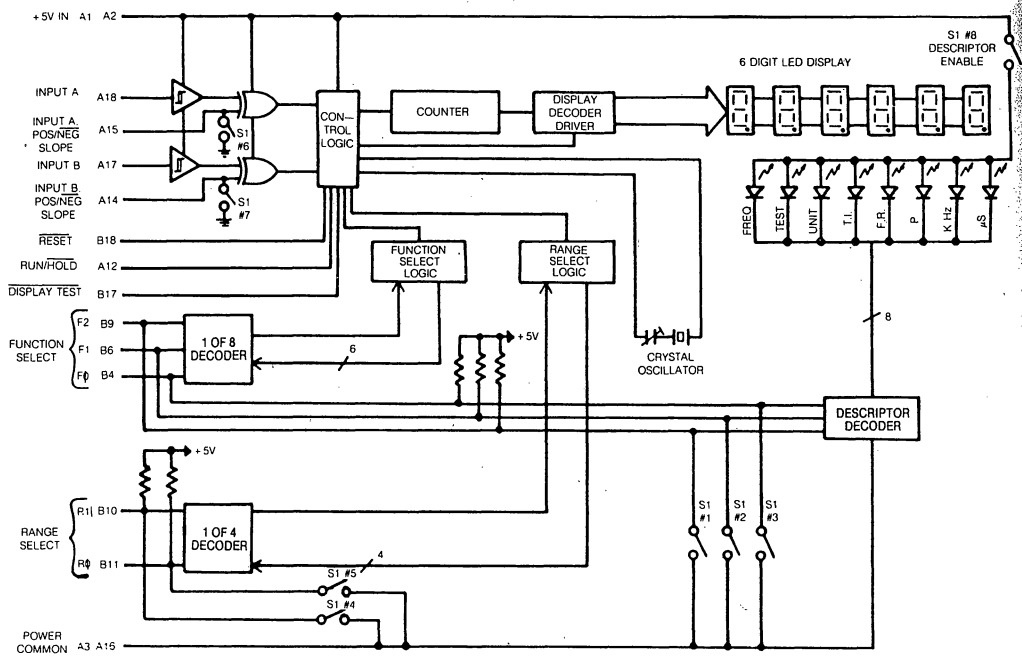
The PC-6 differs from many available Universal counter-timers in being programmable. Counter function, range, and input slope are selected by a binary code. The code is input either electrically on rear-panel, TTL-compatible digital inputs; or manually by setting a front-access Command DIP Switch.

ORDERING INFORMATION

To Order, Specify: PC-6

ACCESSORIES

Part Number	Description
58-2075010	Dual 18-pin edge connector
UPA-5/500	115V AC in, +5V dc (@ 500mA) out power adaptor



Simplified Block Diagram of a PC-6

SPECIFICATIONS

(Typical at +25°C unless noted)

FUNCTIONS

Unit (Event) Counter
Event counter dosplays total number of low-to-high transitions (or high-to-low, see Input Slope Selection Chart). Clears by RESET (Pin B-18).

Measurement Range....999,999 counts occuring at up to 10 MHz rate.

Frequency Counter

Measurement Range....10 MHz max. with 50 nS min. pulse width.
Full Scale Ranges.....10000.0 kHz, 9999.99 kHz, 999.999 kHz, 99.9999 kHz.
Gate Times.....User-selectable: 10mS, 100mS, 1S, 10S.
Timebase.....Internal.
Displayed Unit.....kHz.

Sub-Second Period Timer (Single Input)

Measurement Range....500 nS to .999999S.
Full Scale Ranges.....99999.9 µS, 9999.99 µS, 999.999 µS, 99.9999 µS.
Cycles Measured.....User-selectable: 1, 10, 100, 1000.
Displayed Unit.....µS.

Frequency Ratio Counter
Frequency Ratio Counter measures a frequency at Input A referenced to another frequency at Input B, and displays the unitless ratio FA/FB.

Full Scale Ranges.....99999.9:1, 9999.99:1, 999.999:1, 99.9999:1.
Frequency Range, Input A.....10 MHz maximum with 50% duty cycle square waves
Frequency Range, Input B.....2.0 MHz maximum
Cycles Measured.....User-selectable: 1, 10, 100, 1000.
Displayed Unit.....Pure ratio, FA/FB.

Sub-Second Interval Timer (Dual Input)
Time Interval Timer measures time period from a start pulse at Input A to a stop pulse at Input B.

Measurement Range....500 nS to .999999S.
Full Scale Ranges.....99999.9 µS, 9999.99 µS, 999.999 µS, 99.9999 µS.
Cycles Measured.....User-selectable: 1, 10, 100, 1000.
Displayed Unit.....µS.

Test
Test measures the PC-6 internal oscillator frequency (10 MHz nominally).
Resolution.....100 Hz, 10 Hz, 1 Hz, .1 Hz.
Gate Times.....User-selectable: 10 mS, 100 mS, 1S, 10S

Overall Accuracy
±1 count

Crystal Accuracy
10 ppm accuracy, total (typical) over full temperature range.

Display
Six self-illuminated red LED digits, .3" (7,6mm) high.

Decimal Point
A decimal point is automatically positioned to set display for units shown

Descriptors
Set of 8 LED lamps, which illuminate lenses to indicate Function and Displayed Unit. consists of: FREQ, TEST, UNIT, T.I. (Time Interval), F.R. (Frequency Ratio), P (Period), kHz, and µS. Descriptors are automatically selected with Function and Range Selection, or may be disabled by opening Command Switch #8.

Overrange
"Over" lamp on front panel lights: counting on displayed digits continues

Front-Access Control
Command Switch S1 can be used to select Function, Range, Input Slope, and to enable or disable Descriptors

Time Between Measurement Cycles
200mS, all Functions, all Ranges.

I/O SIGNAL FEATURES

+5V IN (Pins A-1, A-2)
POWER COMMON (Pins A-3, A-16)
Power to PC-6 is input here: +5V (regulated) @ 350 mA required. All logic inputs may be tied to +5V IN for Logic Hi; all inputs may be tied to POWER COMMON for Logic Lo. All inputs are returned at POWER COMMON.

INPUT A (Pin A-18)
INPUT B (Pin A-17)
Signals to be measured are input here (return at POWER COMMON). INPUT A is used for all functions except Test. INPUT B is used only in Frequency Ratio and Time Interval functions.

INPUT A: POS/$\overline{\text{NEG}}$ SLOPE IN (Pin A-15)
INPUT B: POS/$\overline{\text{NEG}}$ SLOPE IN (Pin A-14)
These logic inputs select positive or negative slopes for INPUT A and INPUT B (see "Input Slope Selection" Chart). Connecting either input to POWER COMMON sets that input for a negative slope; connecting either to +5V IN selects a posibite slope.

F2 (Pin B-9) FUNCTION
F1 (Pin B-6) INPUT
F0 (Pin B-4) CODE
R1 (Pin B-10) RANGE
R0 (Pin B-11) INPUT CODE
These five pins select all Functions and Ranges on the PC-6. See "PC-6 Function and Range Selection Chart" for details. Inputs are CMOS with 10kΩ pull-ups to +5V for compatibility with open collector logic.
1 = Logic HI (+3.5V < VH < +5V).
0 = Logic LO (0V < VL < +1.5V).

RESET INPUT (Pin B-18)

Connecting this pin to POWER COMMON stops any measurement in progress, resets the main counter, and displays all zeros. Tie to +5V IN for normal operation. Input is to a Schmitt Trigger (negative-going threshold = 1.5V typ; positive-going threshold is +0.8V typ).

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POWER REQUIREMENTS

+5V IN regulated at 350 mA typical between pins A1 / A2 (+5V IN) and A3 / A16 (POWER COMMON). Logic spikes must not exceed 50 mV. Current varies rapidly as digits switch so that unregulated supplies cannot be used.

PHYSICAL-ENVIRONMENTAL

Outline Dimensions Short-Depth Case, 3.00"W x 2.15"D x 1.76"H (76,2 x 54,6 x 47,7 mm)

Cutout Dimensions
1.812"H x 3.062"W (46,0 x 77,7 mm)

Mounting Method
See end of this section.

Weight
Approximately 7.4 ounces (210 g)

Operating Temperature Range
0° to +50°C (32° to 122°F)

Storage Temperature Range
-25°C to +85°C (-13° to +185°F)

Altitude
0 to 15,000 feet (4900m)

Relative Humidity
10% to 90% non-condensing

INPUT OUTPUT CONNECTIONS PC-6

BOTTOM A		TOP B
+5V PWR IN	1	NO CONNECTION
	2	NO CONNECTION
PWR COMMON	3	NO CONNECTION
NO CONNECTION	4	FUNCTION FØ
KEYWAY →		← KEYWAY
NO CONNECTION	5	NO CONNECTION
NO CONNECTION	6	FUNCTION F1
NO CONNECTION	7	NO CONNECTION
NO CONNECTION	8	NO CONNECTION
NO CONNECTION	9	FUNCTION F2
NO CONNECTION	10	RANGE R1
NO CONNECTION	11	RANGE RO
RUN/HOLD	12	NO CONNECTION
NO CONNECTION	13	NO CONNECTION
B SLOPE	14	NO CONNECTION
A SLOPE	15	NO CONNECTION
PWR COMMON	16	NO CONNECTION
INPUT B	17	DISPLAY TEST
INPUT A	18	RESET

THE WAVEFORMS BELOW INDICATE THE MINIMUM TIMES AN INPUT MUST BE HIGH OR LOW TO INCREMENT THE COUNTER CIRCUITRY IN THE PC-6.

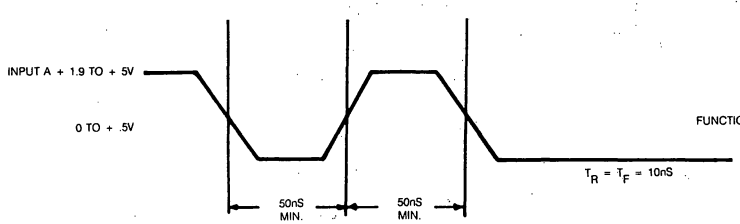


FIGURE 1
FUNCTION = FREQUENCY, FREQUENCY RATIO, UNIT COUNTER

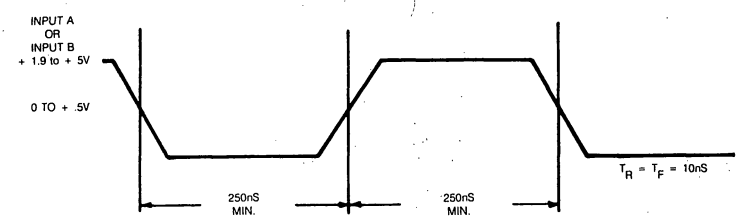


FIGURE 2
FUNCTION = PERIOD, TIME INTERVAL

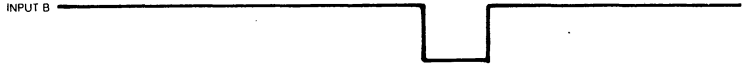


FIGURE 3
FUNCTION = TIME INTERVAL

* 200ms REQUIRED BETWEEN MEASUREMENTS FOR INTERNAL CIRCUITRY TO UPDATE.

PC-6 Input Waveforms

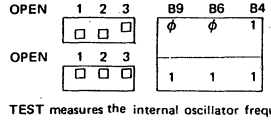
PC-6 FUNCTION AND RANGE SELECTION CHART

FUNCTION (8)	FULL SCALE DISPLAY RANGES	GATING TIMES/ CYCLES MEASURED	FUNCTION/RANGE SELECTION — S1 DIP SWITCH	Rear-Panel Logic Input (1) B9	B6	B4	B10	B11	TYPICAL INPUT WAVEFORM	SIGNAL (4) INPUT PIN(S)
UNIT (EVENT) COUNTER	999999 counts	N/A	OPEN 1 2 3 (2)	ϕ	1	1	-	-		A-18
FREQUENCY COUNTER (Internal Time-base)	10000.0 kHz	.01S	OPEN 1 2 3 4 5 (2)	ϕ	ϕ	ϕ	ϕ	ϕ		A-18 (7)
	9999.99 kHz	.1S GATING	OPEN 1 2 3 4 5	ϕ	ϕ	ϕ	ϕ	1		
	999.999 kHz	1S TIMES	OPEN 1 2 3 4 5	ϕ	ϕ	ϕ	1	ϕ		
	99.9999 kHz	10S	OPEN 1 2 3 4 5	ϕ	ϕ	ϕ	1	1		
SUB-SECOND PERIOD TIMER (single input)	99999.9 μS	1	OPEN 1 2 3 4 5	1	1	ϕ	ϕ	ϕ	T_A	A-18 (7)
	9999.99 μS	10 CYCLES	OPEN 1 2 3 4 5	1	1	ϕ	ϕ	1		
	999.999 μS	100 MEASURED	OPEN 1 2 3 4 5	1	1	ϕ	1	ϕ		
	99.9999 μS	1000	OPEN 1 2 3 4 5	1	1	ϕ	1	1		
FREQUENCY RATIO COUNTER (External Time-base)	99999.9:1	1	OPEN 1 2 3 4 5	1	ϕ	1	ϕ	ϕ	INPUT A	A-18 (INPUT A)
	9999.99:1	10 CYCLES	OPEN 1 2 3 4 5	1	ϕ	1	ϕ	1		
	999.999:1	100 MEASURED	OPEN 1 2 3 4 5	1	ϕ	1	1	ϕ	INPUT B	A-17 (INPUT B)
	99.9999:1	1000	OPEN 1 2 3 4 5	1	ϕ	1	1	1		
SUB-SECOND INTERVAL TIMER (dual input)	99999.9 μS	1 (6)	OPEN 1 2 3 4 5	1	ϕ	ϕ	ϕ	ϕ	$T_{A \to B}$	A-18 (INPUT A)
	9999.99 μS	10 CYCLES	OPEN 1 2 3 4 5	1	ϕ	ϕ	ϕ	1		
	999.999 μS	100 MEASURED	OPEN 1 2 3 4 5	1	ϕ	ϕ	1	ϕ		A-17 (INPUT B)
	99.9999 μS	1000	OPEN 1 2 3 4 5	1	ϕ	ϕ	1	1		
TEST	10000.0 kHz (3)	.01S	OPEN 1 2 3 4 5	ϕ	1	ϕ	ϕ	ϕ	N/A	N/A
	0000.00 kHz (3)	.1S GATING	OPEN 1 2 3 4 5	ϕ	1	ϕ	ϕ	1		
	000.000 kHz (3)	1S TIMES	OPEN 1 2 3 4 5	ϕ	1	ϕ	1	ϕ		
	00.0000 kHz (3)	10S	OPEN 1 2 3 4 5	ϕ	1	ϕ	1	1		

NOTES:

1) ϕ = Logic Low (0V< V_L <+1.5V)
   1 = Logic High (+3.5V< V_H <+5.0V)
   - = Don't care.

2) FREQUENCY COUNTER may identically be selected by:



Range Selection codes are those given in the above chart for ϕϕϕ Function Code.

3) TEST measures the internal oscillator frequency of the PC-6. This is nominally 10.0MHz (10000kHz). In the lower three ranges on TEST, the 10.0MHz frequency will be over-scale (Overrange light will turn on). The least significant digits on these ranges are accurately displayed to permit more accurate calibration of the PC-6.

4) All input signals are returned at A-16, POWER COMMON.

5) On the PC-6, Gating Times or Number of Cycles Measured is selected automatically with the Full Scale Display Range.

6) To measure a single cycle in the INTERVAL TIMER function, the PC-6 must be "primed," first by a single cycle preceding that to be measured. The first cycle sets the counter circuitry; the second cycle is measured.

7) In FREQUENCY and PERIOD functions, tie INPUT B (pin A-17) to POWER COMMON (pin A-16).

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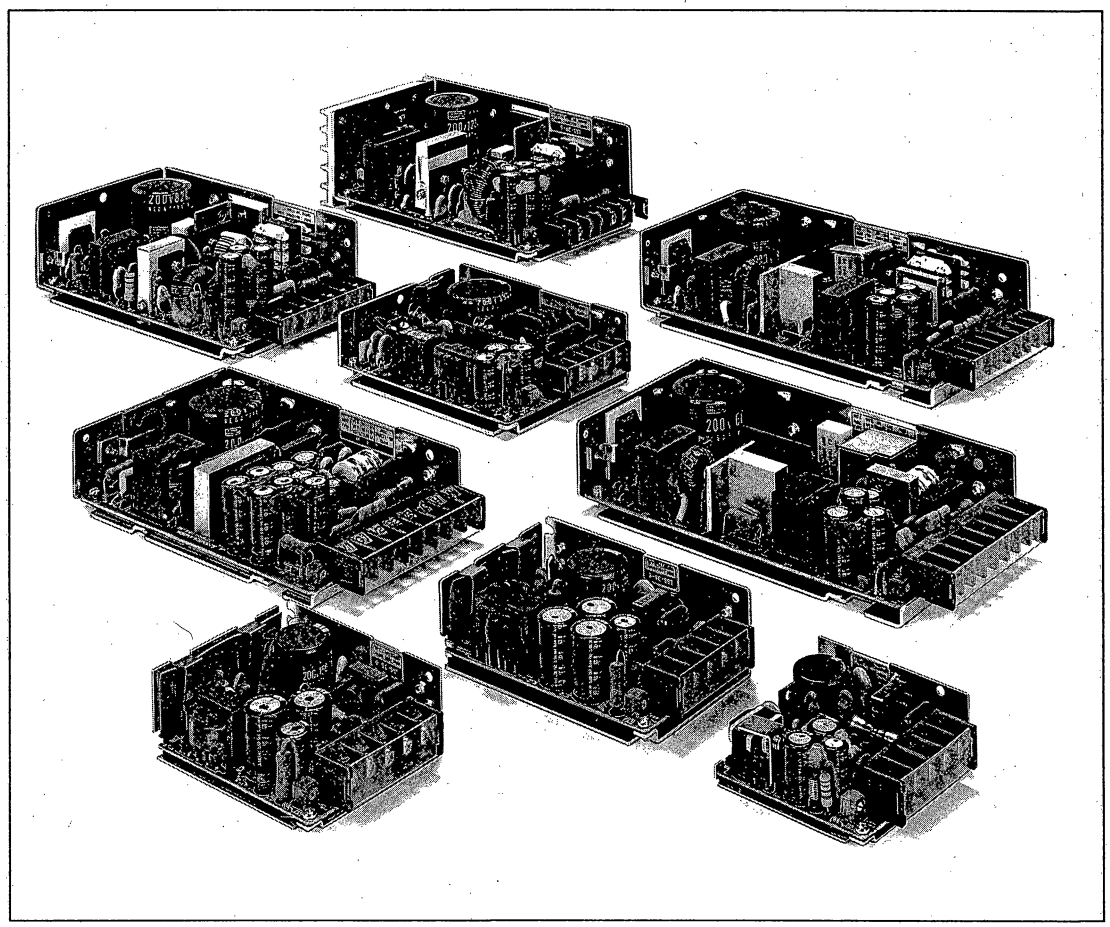
LAMBDA'S LS SERIES



High Density, Low Cost Power Supplies

Space is always at a premium in electronic applications, and form factor plays an important role in utilization of that space. Lambda's LS Series provides single and multiple output solutions in a modular form for the most efficient use of available space.

The LS Series features 10 single and triple output packages up to 48V, up to 30A, providing over 2.2W/in^3. All models are designed with built-in overvoltage protection, in-rush current limiting and 2000VAC input to output isolation.

Targeted for cost driven industrial applications in the US, Canadian and Far Eastern markets, the LS Series provides full output power from 85 to 132VAC. In addition, their thermal design allows for full rated power at 50°C ambient temperature in a convection cooled environment. Barrier strip connections provide ease of installation and replacement during equipment upgrading cycles.

LS SERIES SPECIFICATIONS

AC Input
line .....85 to 132VAC, 47-440Hz.

Efficiency
72% typical for 5V LSS models. 70% typical for LST models, and 12V and 15V LSS models. 82% typical on 24V through 48V LSS models.

DC Input
110 to 175VDC.

DC Output
Voltage range shown in tables.

Regulated Voltage
regulation, line .....0.4% for input variations from 85 to 132VAC or 132 to 85VAC.
regulation, load .....0.8% for load changes from zero to full load and from full load to zero on LSS models. 0.8% for load changes from 0.75A to full load on main output of LST-37; from 1.5A to full load on main output of LST-38, LST-39; from 3A to full load on LST-40. 150mV max from zero to full load and full load to zero on auxiliary outputs of LST-37, 38, 39, 40 with main output preloaded.
ripple and noise.
(20MHz Bandwidth) .....15mV RMS for all models;
120mV pk-pk for 5V and 6V models;
150mV pk-pk for 12V and 15V models;
200mV pk-pk for 24V and 28V models.
250mV pk-pk for 48V models.
temperature coefficient .....0.02%/°C.

Hold Up Time
5V and 6V LSS models, and all LST models will remain within regulation limits for at least 16.7 msec. after loss of AC power when operating at full load, nominal output voltage and 100VAC input voltage.

Overload Protection
External overload protection, automatic electronic current limiting circuit, limits output current to a safe, preset value, thereby protecting the load as well as the power supply. Avoid short circuit operation longer than 30 seconds.

Overvoltage Protection
Overvoltage protection is standard on all LSS models and on main output of LST Models. If output voltage increases above a preset level, inverter drive is removed.

Overshoot
No overshoot at turn-on, turn-off or power failure.

In-rush Current Limiting
The turn-on in-rush current will not exceed 15A typical on LSS-38, LSS-39, LST-37, LST-38, LST-39; 20A typical on LST-40; 24A typical for LSS-34; 30A typical for LSS-35, LSS-36, LSS-37.

Cooling
Convection cooled, no fans or blowers needed.

Operating Temperature Range
0-60°C with suitable derating above 50°C. (65°C operation on LST-40 is possible. Consult factory.)

Storage Temperature Range
−30°C to +85°C.

Remote Sensing
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation for LSS-38 and LSS-39.

Isolation Rating
2000V RMS input to output.

DC Output Controls
Simple screwdriver adjustment.

Input and Output Connections
All input and output connections are made via barrier strip terminals.

Output Status Indicator
LED indicates presence of output voltage on LSS models and 5V output of LST models.

Mounting
Two mounting surfaces, two mounting positions. One mounting surface and one mounting position for LSS-39. Some derating may be required in horizontal mounting position. Consult factory.

Finish
Aluminum.

Physical Data

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LSS-34	0.46	0.55	1.06 × 2.75 × 2.68
LSS-35	0.64	0.75	1.26 × 2.75 × 3.35
LSS-36	0.66	0.75	1.38 × 2.75 × 4.14
LSS-37	0.88	1.00	1.38 × 3.74 × 4.72
LST-37	0.93	1.10	1.42 × 3.74 × 6.10
LST-38	1.21	1.41	1.61 × 3.74 × 6.89
LST-39	1.54	1.79	1.93 × 3.74 × 7.48
LSS-38	1.54	1.85	2.00 × 3.74 × 6.30
LSS-39	2.31	2.50	2.40 × 3.74 × 7.09
LST-40	2.70	2.80	1.93 × 3.74 × 10.24

Accessories
For rack adapters and other accessories, see pages 151-152.

Safety Agency Approvals
All models are UL recognized and most are CSA certified. Consult factory.

Guarantee
One year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of one year.

POWER-SONIC Sealed Lead-Acid Batteries

FEATURES

Sealed/Maintenance-Free — The sealed construction of the Power-Sonic battery allows trouble-free, safe operation in any position. There is no need to add electrolyte, as gases generated during overcharge are recombined in a unique "Oxygen Cycle."

Easy Handling — No special handling precautions or shipping containers — surface or air — are required due to the leak-proof construction.

Economical — The high watt-hour per dollar value is made possible by the materials used in a sealed lead-acid battery; they are readily available and low in cost.

Long Service Life — Under normal operating conditions, four or five years of dependable service life can be expected in standby applications or between 200 and 1000 charge/discharge cycles depending upon depth of discharge.

Design Flexibility — Batteries may be used in series and/or parallel to give you choice of voltage and capacity. Due to recent design breakthroughs, the same battery may be used in either cyclic or standby applications without sacrificing life or performance. Furthermore, Power-Sonic offers over 30 basic model sizes.

Rugged Construction — The high-impact resistant battery case is made of non-conductive ABS plastic with superior resistance to shock, vibration, chemicals and heat.

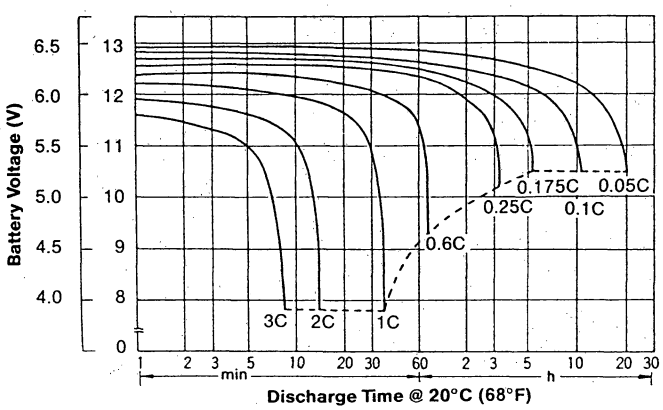
Compact — Power-Sonic batteries utilize state of the art design, highest grade materials, and a carefully controlled plate-making process to provide excellent output per cell. This high energy density results in superior power/volume and power/weight ratios.

High Discharge Rate — Low internal resistance allows discharge currents of over ten times the rated capacity of the battery. Therefore, a relatively smaller battery may be specified in applications requiring high peak currents.

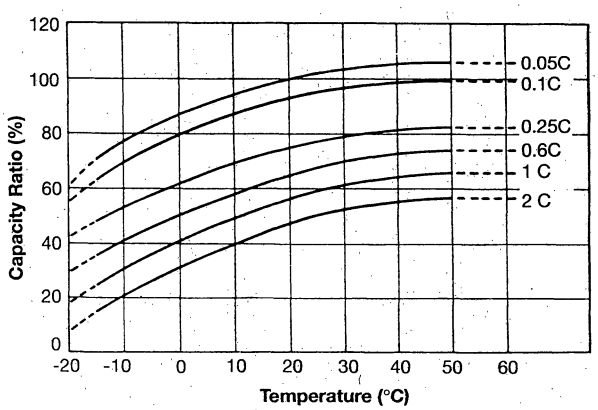
Long Shelf Life — A low self-discharge rate permits storage of fully charged batteries for up to a year at room temperature before charging is required. Lower storage temperatures enhance shelf life characteristics even further.

Wide Operating Temperature Range — Power-Sonic batteries may be used over a temperature range of -76°F to +140°F (-60°C to +60°C).

Deep Discharge Recovery — Special separators, advanced plate composition, and a carefully balanced electrolyte system have greatly improved the capability of recovering from deep discharge.



Characteristic Discharge Curves



Effect of Temperature on Capacity

CHARGING

Cycle Applications: Limit initial current to 0.20C (C is the nominal A.H. capacity of the battery). Charge until battery voltage (under charge) reaches 2.45 volts per cell at 68°F (20°C). Hold at 2.45 volts per cell until current drops to approximately 0.01C ampere. Battery is fully charged under these conditions, and charger should either be disconnected or switched to "float" voltage.

"Float" or "Stand-By" Service: Hold battery across constant voltage source of 2.25 to 2.30 volts per cell continuously. When held at this voltage, the battery will seek its own current level and maintain itself in a fully charged condition.

TERMINALS

Standard Terminals: Quick disconnect "FASTON" tabs 0.187″ × 0.032″; mate with AMP. INC. FASTON "187" series receptacles. Models: PS-445, 610, 612, 620, 630, 632, 640, 670, 682F, 6100, 1212, 1220, 1226, 1230, 1232, 1242, 1252, 1270, 1282.

"250" FASTON: Quick disconnect tabs 0.250″ × 0.032″; mate with AMP. INC. "250" series receptacle. Models: PS-490, 6100, 12100, 12120, 12170F, 12260F.

Polarized FASTON: Quick disconnect tabs; positive 0.250″ × 0.032″, negative 0.187″ × 0.032″. Models: PS-665, 695, 6120, 1295, 12120L.

Spring Type: PS-650L (lantern battery)

Wire Leads: C.U. insulated, stranded wire leads

a) terminated with AMP. INC. Mate-N-Lock connector housing P/N 1-480318-0 and female pin P/N 60619-1. Mates with connector housing P/N 1-480319 and male pin P/N 61116-1. Models: PS-640WL, PS-1207.
b) terminated with "250" female FASTON receptacles. Model: PS-682WL. c) terminated with MOLEX housing P/N 5264-02 and plug P/N 5263-PBT: Model PS-605.

Nut and Bolt: Post with nut and bolt terminals; 5mm ∅ for Models: PS-6200, 12170NB, 12260, 12280. 6mm ∅ for Model PS-12400.

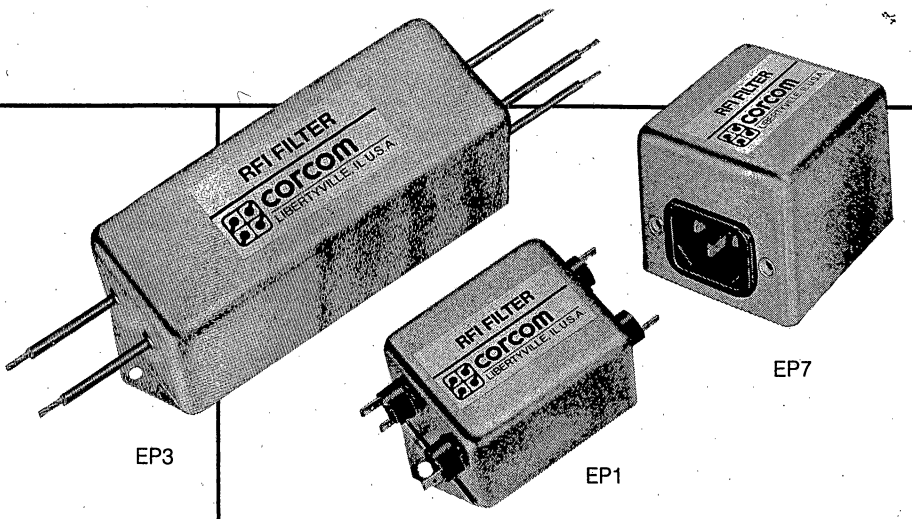
Heavy Duty Flag Terminals: Models: PS-12330, 12500, 12600, 12800.

SPECIFICATIONS

Model	Nominal Voltage V	Nominal Capacity @ 20 hr. rate A.H.	Discharge Capacity @ 20 hr. rate mA	DIMENSIONS								Weight	
				Length		Width		Height		Ht. Over Terminal			
				in.	mm	in.	mm	in.	mm	in.	mm.	lbs.	kg.
PS-445	4	4.5	225	1.93	49	2.09	53	3.70	94	3.86	98	1.5	0.7
PS-490	4	9.0	450	4.02	102	1.73	44	3.70	94	3.86	98	2.4	1.1
PS-605	6	0.5	25	2.24	57	0.55	14	1.97	50	1.97	50	.20	.09
PS-610	6	1.0	50	2.00	51	1.65	42	2.00	51	2.20	56	0.6	0.3
PS-612	6	1.2	60	3.82	97	0.94	24	2.00	51	2.13	54	0.6	0.3
PS-620	6	2.0	100	2.95	75	2.00	51	2.09	53	2.28	58	1.1	0.5
PS-630	6	3.0	150	5.28	134	1.34	34	2.35	60	2.56	65	1.5	0.7
PS-632	6	3.2	160	2.60	66	1.30	33	4.84	123	5.00	127	1.5	0.7
PS-640	6	4.0	200	2.76	70	1.89	48	4.02	102	4.25	108	1.8	0.8
PS-650L	6	5.0	250	2.63	67	2.63	67	3.78	96	4.28	109	2.0	0.9
PS-665	6	6.5	325	3.86	98	2.20	56	4.05	103	4.05	103	3.0	1.4
PS-670	6	7.0	350	5.95	151	1.34	34	3.70	94	3.86	98	3.0	1.4
PS-682	6	8.0	400	3.86	98	2.20	56	4.65	118	4.65	118	3.3	1.5
PS-695	6	9.5	475	4.26	108	2.75	70	5.54	141	5.54	141	4.9	2.2
PS-6100	6	10.0	500	5.95	151	2.00	51	3.70	94	3.86	98	4.6	2.1
PS-6120	6	12.0	600	4.26	108	2.75	70	5.54	141	5.54	141	5.5	2.5
PS-6200	6	20.0	1000	6.18	157	3.27	83	4.92	125	4.92	125	8.2	3.7
PS-1207	12	0.7	35	3.78	96	0.98	25	2.42	62	2.42	62	0.8	0.35
PS-1212	12	1.2	60	3.82	97	1.65	42	2.00	51	2.13	54	1.3	0.6
PS-1220	12	2.0	100	7.01	178	1.34	34	2.36	60	2.56	65	1.9	0.9
PS-1226	12	2.6	130	7.01	178	1.34	34	2.36	60	2.56	65	2.2	1.0
PS-1230	12	3.0	150	5.23	134	2.64	67	2.36	60	2.60	66	2.6	1.2
PS-1232	12	3.2	160	7.68	195	1.85	47	2.76	70	2.95	75	3.1	1.4
PS-1242	12	4.0	200	3.54	90	2.76	70	3.98	101	4.13	105	3.8	1.7
PS-1252	12	5.0	250	3.54	90	2.76	70	4.02	102	4.25	108	4.2	1.9
PS-1270	12	7.0	350	5.95	151	2.56	65	3.70	94	3.86	98	5.7	2.6
PS-1282	12	8.0	400	3.86	98	4.40	112	4.65	118	4.65	118	6.7	3.0
PS-1295	12	9.5	475	8.38	213	2.75	70	5.50	140	5.50	140	10.0	4.6
PS-12100	12	10.0	500	5.95	151	4.00	102	3.70	94	3.86	98	9.2	4.2
PS-12120	12	12.0	600	5.94	151	3.86	98	3.70	94	3.94	100	9.0	4.1
PS-12120L	12	12.0	600	8.38	213	2.75	70	5.50	140	5.50	140	11.0	5.0
PS-12170	12	17.0	850	7.13	181	2.99	76	6.57	167	6.57	167	12.8	5.8
PS-12260	12	26.0	1300	6.89	175	6.54	166	4.92	125	4.92	125	18.7	8.5
PS-12280	12	28.0	1400	6.54	166	4.92	125	6.89	175	6.89	175	19.4	8.8
PS-12330	12	33.0	1650	7.68	197	5.19	132	6.38	162	7.15	182	26.5	12.0
PS-12400	12	40.0	2000	7.75	197	6.50	165	6.69	170	6.69	170	30.9	14.0
PS-12500	12	50.0	2500	9.40	239	5.50	140	8.20	208	9.05	230	36.0	16.4
PS-12600	12	60.0	3000	10.25	260	6.60	168	8.20	208	9.45	240	46.0	20.9
PS-12800	12	80.0	4000	12.00	305	6.60	168	8.20	208	9.45	240	55.0	25.0

EP Series

For Switching Power Supply Noise Suppression



EP3

EP7

EP1

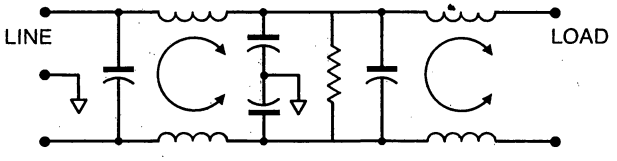
UL Recognized, CSA Certified, VDE Approved, and SEV Approved

EP Series

The EP series of RFI filters has been developed to reduce conducted noise to acceptable limits for equipment that must comply with the requirements of VDE 0871 in West Germany and the FCC specifications in the USA.

These filters provide high insertion loss for both line-to-ground and line-to-line emissions throughout the frequency range. They are particularly well suited for equipment that must meet both stringent emissions specifications (such as VDE 0871, A-level and FCC Part 15J, Class B) and very low leakage current requirements (such as SEV, VDE portable equipment, and (120 Volt) UL544 nonpatient medical equipment).

Electrical Schematic



Line Cord

Line Cord No. 80-1245:
7½ foot, 3-conductor line cord to mate with EP7 models.

Specifications

Maximum leakage current, each
line-to-ground @ 120 VAC 60 Hz: .25 mA
@ 250 VAC 50 Hz: .40 mA

Hipot rating (one minute):
line-to-ground 2250 VDC
line-to-line 1450 VDC

Operating frequency: 50/60 Hz

Rated voltage: 120/250 VAC

Rated current:	@ 120 VAC	@ 250 VAC	SEV @ 250 VAC
3EP	3A	3A	1.5A
6EP	6A	5A	4A
10EP	10A	8A	6A

Maximum rated current peaks:

3EP	10A
6EP	18A
10EP	30A

Minimum insertion loss in dB:
Line-to-ground in 50 ohm circuit

Current Rating	Frequency—MHz .01	.04	.05	.15	.5	1	5	10	30
3A	1	1	10	58	65	65	65	60	25
6A	1	1	10	58	65	65	65	60	25
10A	1	1	10	58	65	65	65	60	25

Line-to-line in 50 ohm circuit

Current Rating	Frequency—MHz .01	.09	.15	.5	1	5	10	20	30
EP1, EP3									
3A	1	5	36	65	65	65	65	58	58
6A	1	5	30	65	65	65	65	35	35
10A	1	5	30	65	65	65	65	35	35
EP7									
3A	1	5	36	55	55	54	53	51	50

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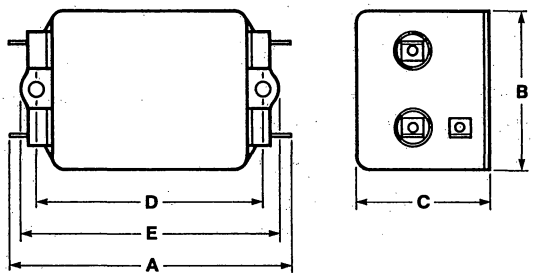
Case Styles

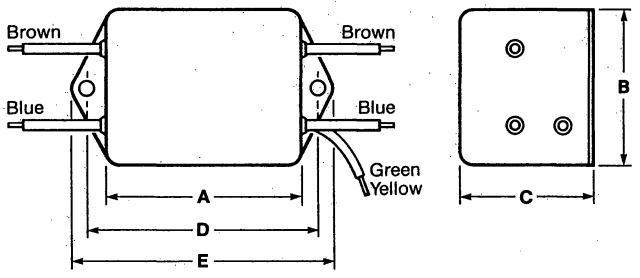
Metric shown in italics.

EP1



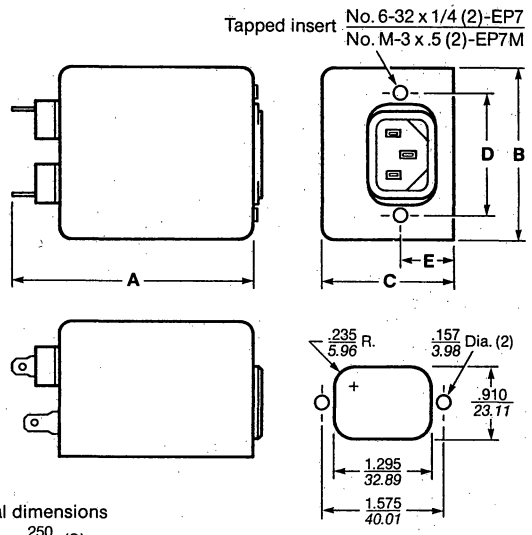
Typical dimensions
Fastons: .250 / 6.35 (5) Holes: .07 / 1.8 Dia. Mounting holes: .188 / 4.78 Dia. (2)

EP3



Typical dimensions
Wire leads: 4.0 / 101.6 Min. Mounting holes: .188 / 4.78 Dia. (2)

EP7 & EP7M (with metric insert)



Typical dimensions
Fastons: .250 / 6.35 (3)
Holes: .07 / 1.8 Dia.

Panel cutout (Back mount)
Tolerance ± .005 / 0.13

Case Dimensions

Metric shown in italics.

Part No.	A (max)	B (max)	C (max)	D ±.015 / ±.38	E (max)
3EP1	3.85 / *97.8*	2.07 / *52.6*	1.78 / *45.2*	2.938 / *74.63*	3.35 / *85.1*
3EP3	2.56 / *65.0*	2.07 / *52.6*	1.78 / *45.2*	2.938 / *74.63*	3.35 / *85.1*
3EP7	3.21 / *81.5*	2.25 / *57.2*	1.78 / *45.2*	1.575 / *40.01*	0.66 / *16.8* †
3EP7M	3.21 / *81.5*	2.25 / *57.2*	1.78 / *45.2*	1.575 / *40.01*	0.66 / *16.8* †
6EP1	6.62 / *168.1*	2.07 / *52.6*	2.28 / *57.9*	5.625 / *142.88*	6.03 / *153.2*
6EP3	5.33 / *135.4*	2.07 / *52.6*	2.28 / *57.9*	5.625 / *142.88*	6.03 / *153.2*
10EP1	6.62 / *168.1*	2.07 / *52.6*	2.78 / *70.6*	5.625 / *142.88*	6.03 / *153.2*
10EP3	5.33 / *135.4*	2.07 / *52.6*	2.78 / *70.6*	5.625 / *142.88*	6.03 / *153.2*

† ±.02 / ±.5

Price List

Part No.	Unit Price	Part No.	Unit Price
3EP1	$21.04	6EP1	$31.83
3EP3	21.04	6EP3	31.83
3EP7	22.93	10EP1	47.33
3EP7M	22.93	10EP3	47.33
Line Cord No. 80-1245			$ 6.07