VLBA Technical Report No. 8

VLBA FOCUS-ROTATION CONTROL SYSTEM

VOLUME IIA

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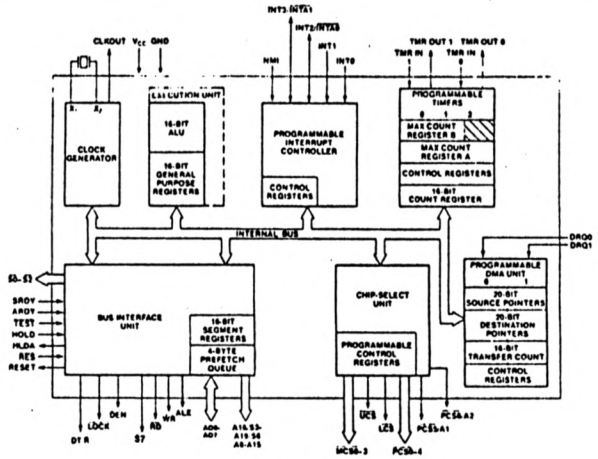
June 1990

80188
HIGH INTEGRATION 8-BIT MICROPROCESSOR

- Integrated Feature Set
  - — Enhanced 8086-2 CPU
  - — Clock Generator
  - — 2 Independent DMA Channels
  - — Programmable Interrupt Controller
  - — 3 Programmable 16-Bit Timers
  - — Programmable Memory and Peripheral Chip-Select Logic
  - — Programmable Wait State Generator
  - — Local Bus Controller
- 16-Bit Internal Architecture with 8-Bit Data Bus Interface
- High-Performance 8 MHz Processor
  - — At 8 MHz Provides 2 Times the Performance of the Standard 8088
  - — 2 MByte/Sec Bus Bandwidth Interface @8 MHz
- Direct Addressing Capability to 1 MByte of Memory and 64 KByte I/O
- Completely Object Code Compatible with All Existing 8086/8088 Software
  - — 10 New Instruction Types
- Complete System Development Support
  - — Development Software: ASM86 Assembler, PL/M-86, Pascal-86, Fortran-86, C-86, and System Utilities
  - — In-Circuit-Emulator (I²ICE™-186/188)
- High Performance Numerical Coprocessing Capability Through 8087 Interface
- Available in 68 Pin:
  - — Ceramic Leadless Chip Carrier (LCC)
  - — Ceramic Pin Grid Array (PGA)
  - — Plastic Leaded Chip Carrier (PLCC)

  (See Packaging Outlines and Dimensions, Order # 231369)
- Available in EXPRESS
  - — Standard Temperature with Burn-In
  - — Extended Temperature Range (−40°C to +85°C)



210706-1

Figure 1. 80188 Block Diagram

October 1988
Order Number: 210706-010

The Intel 80188 is a highly integrated microprocessor with an 8-bit data bus interface and a 16-bit internal architecture to give high performance. The 80188 effectively combines 15–20 of the most common 8088 system components onto one. The 80188 provides two times greater throughput than the standard 5 MHz 8088. The 80188 is upward compatible with 8086 and 8088 software and adds 10 new instruction types to the existing set.

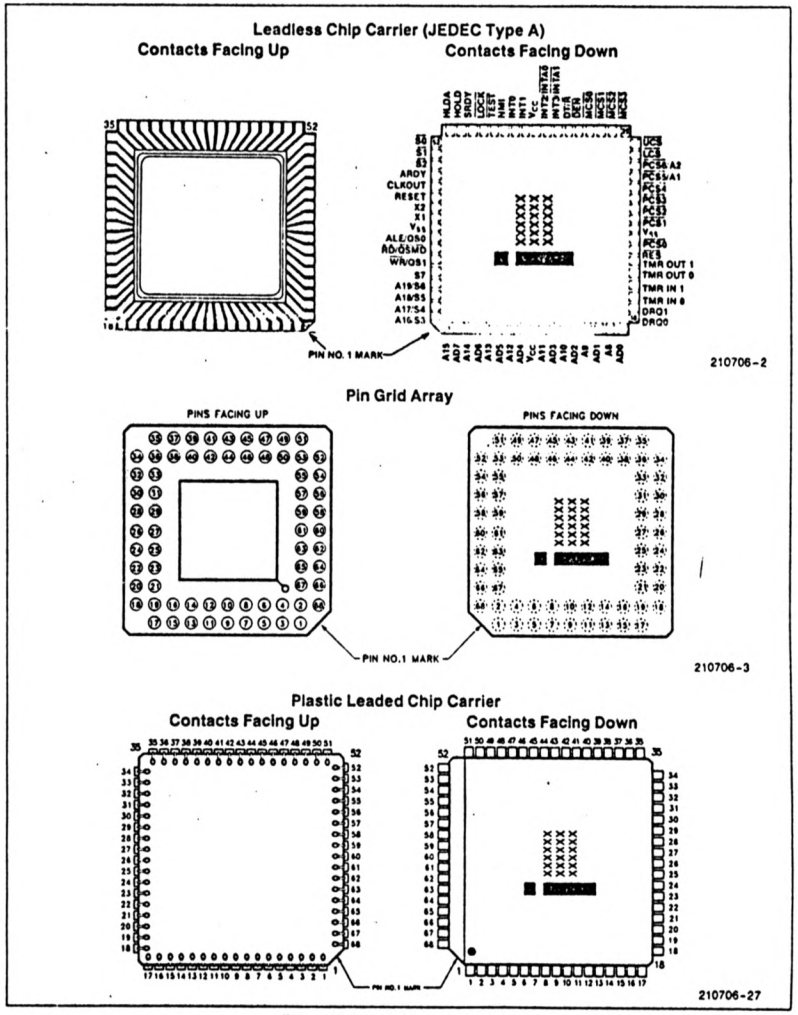


Figure 2. 80188 Pinout Diagram

Table 1. 80188 Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	9 43	I I	**SYSTEM POWER:** +5 volt power supply.
V_{SS}	26 60	I I	**SYSTEM GROUND**
RESET	57	O	**RESET OUTPUT:** Indicates that the 80188 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1 X2	59 58	I O	**CRYSTAL INPUTS:** X1 and X2 provide external connections for a fundamental mode parallel resonant crystal for the internal oscillator. Instead of using a crystal, an external clock may be applied to X1 while minimizing stray capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	**CLOCK OUTPUT:** Provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT.
$\overline{RES}$	24	I	**PROCESSOR RESET:** Causes the 80188 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80188 clock. The 80188 begins fetching instructions approximately 6½ clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held low. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network. When $\overline{RES}$ occurs, the 80188 will drive the status lines to an inactive level for one clock, and then float them.
$\overline{TEST}$	47	I	**$\overline{TEST}$:** Is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80188 is waiting for $\overline{TEST}$, interrupts will be serviced. This input is synchronized internally.
TMR IN 0 TMR IN 1	20 21	I I	**TIMER INPUTS:** Are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.
TMR OUT 0 TMR OUT 1	22 23	O O	**TIMER OUTPUTS:** Are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
DRQ0 DRQ1	18 19	I I	**DMA REQUEST:** Is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	46	I	**NON-MASKABLE INTERRUPT:** Causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one clock. The Non-Maskable interrupt cannot be avoided by programming.
INT0 INT1 INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$	45 44 42 41	I I I/O I/O	**MASKABLE INTERRUPT REQUESTS:** Can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When slave mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).

Table 1. 80188 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
A19/S6 A18/S5 A17/S4 A16/S3	65 66 67 68	O O O O	**ADDRESS BUS OUTPUTS (16–19) and BUS CYCLE STATUS (3–6):** Indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W, and T_4, status information is available on these lines as encoded below: S6: Low = Processor Cycle; High = DMA Cycle S3, S4, and S5 are defined as LOW during T_2–T_4. The status pins float during HOLD/HLDA.
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	2 4 6 8 11 13 15 17	I/O I/O I/O I/O I/O I/O I/O I/O	**ADDRESS/DATA BUS (0-7):** Signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active HIGH.
A15 A14 A13 A12 A11 A10 A9 A8	1 3 5 7 10 12 14 16	O O O O O O O O	**ADDRESS-ONLY BUS (8-15):** Containing valid address from T_1-T_4. The bus is active HIGH.
S7	64	O	This signal is HIGH to indicate that the 80188 has an 8-bit data bus. S7 floats during HOLD.
ALE/QS0	61	O	**ADDRESS LATCH ENABLE/QUEUE STATUS 0:** Is provided by the 80188 to latch the address. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T_1 of the associated bus cycle, effectively one-half clock cycle earlier than in the 8088. The trailing edge is generated off the CLKOUT rising edge in T_1 as in the 8088. Note that ALE is never floated.
$\overline{WR}$/QS1	63	O	**WRITE STROBE/QUEUE STATUS 1:** Indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW, and floats during HOLD. When the 80188 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction. QS1 / QS0 / Queue Operation: 0 / 0 / No Queue Operation 0 / 1 / First Opcode Byte Fetched from the Queue 1 / 1 / Subsequent Byte Fetched from the Queue 1 / 0 / Empty the Queue

Table 1. 80188 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RD}$/QSMD	62	I/O	**READ STROBE:** Is an active LOW signal which indicates that the 80188 is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the 80188 is to provide ALE, $\overline{RD}$, and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND. $\overline{RD}$ will float during bus hold.
ARDY	55	I	**ASYNCHRONOUS READY:** Informs the 80188 that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT and is active HIGH. The falling edge of ARDY must be synchronized to the 80188 clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.
SRDY	49	I	**SYNCHRONOUS READY:** Informs the 80188 that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchronize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.
$\overline{LOCK}$	48	O	**$\overline{LOCK}$:** Output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted. When executing more than one LOCK instruction, always make sure there are 6 bytes of code between the end of the first LOCK instruction and the start of the second LOCK instruction. $\overline{LOCK}$ is active LOW, is driven HIGH for one clock during RESET, and then floated.
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	52 53 54	O O O	**BUS CYCLE STATUS $\overline{S0}$–$\overline{S2}$:** Are encoded to provide bus-transaction information:

80188 Bus Cycle Status Information

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

The status pins float during "HOLD."
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.

Table 1. 80188 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
HOLD (input) HLDA (output)	50 51	I O	**HOLD:** Indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the 80188 clock. The 80188 will issue a HLDA in response to a HOLD request at the end of T_4 or T_i. Simultaneous with the issuance of HLDA, the 80188 will float the local bus and control lines. After HOLD is detected as being LOW, the 80188 will lower HLDA. When the 80188 needs to run another bus cycle, it will again drive the local bus and control lines.
$\overline{UCS}$	34	O	**UPPER MEMORY CHIP SELECT:** Is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{UCS}$ is software programmable.
$\overline{LCS}$	33	O	**LOWER MEMORY CHIP SELECT:** Is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{LCS}$ is software programmable.
$\overline{MCS0}$ $\overline{MCS1}$ $\overline{MCS2}$ $\overline{MCS3}$	38 37 36 35	O O O O	**MID-RANGE MEMORY CHIP SELECT SIGNALS:** Are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{MCS0}$–3 are software programmable.
$\overline{PCS0}$ $\overline{PCS1}$ $\overline{PCS2}$ $\overline{PCS3}$ $\overline{PCS4}$	25 27 28 29 30	O O O O O	**PERIPHERAL CHIP SELECT SIGNALS 0–4:** Are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{PCS0}$–4 are software programmable.
$\overline{PCS5}$/A1	31	O	**PERIPHERAL CHIP SELECT 5 or LATCHED A1:** May be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software programmable. When programmed to provide latched A1, rather than $\overline{PCS5}$, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active HIGH.
$\overline{PCS6}$/A2	32	O	**PERIPHERAL CHIP SELECT 6 or LATCHED A2:** May be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software programmable. When programmed to provide latched A2, rather than $\overline{PCS6}$, this pin will retain the previously latched value of A2 during a bus HOLD. A2 is active HIGH.
DT/$\overline{R}$	40	O	**DATA TRANSMIT/RECEIVE:** Controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the 80188. When HIGH the 80188 places write data on the data bus.
$\overline{DEN}$	39	O	**DATA ENABLE:** Is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access. $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state.

FUNCTIONAL DESCRIPTION

Introduction

The following Functional Description describes the base architecture of the 80188. The 80188 is a very high integration 8-bit microprocessor. It combines 15-20 of the most common microprocessor system components onto one chip while providing twice the performance of the standard 8088. The 80188 is object code compatible with the 8086, 8088 microprocessors and adds 10 new instruction types to the 8086, 8088 instruction set.

80188 BASE ARCHITECTURE

The 8086, 8088, 80186, 80188 and 80286 family all contain the same basic set of registers, instructions, and addressing modes. The 80188 processor is upward compatible with the 8086, 8088, 80186, and 80286 CPUs.

Register Set

The 80188 base architecture has fourteen registers as shown in Figures 3a and 3b. These registers are grouped into the following categories.

GENERAL REGISTERS

Eight 16-bit general purpose registers may be used for arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

SEGMENT REGISTERS

Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

BASE AND INDEX REGISTERS

Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

STATUS AND CONTROL REGISTERS

Two 16-bit special purpose registers record or alter certain aspects of the 80188 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Figures 3a and 3b).

STATUS WORD DESCRIPTION

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the 80188 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16 bits wide. The function of the Status Word bits is shown in Table 2.

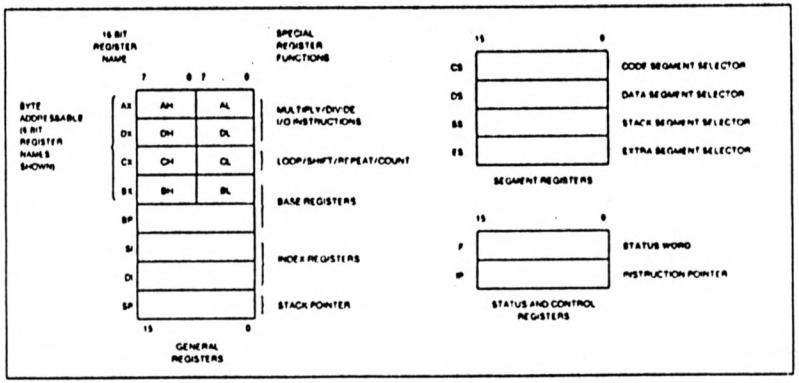


Figure 3a. 80188 Register Set

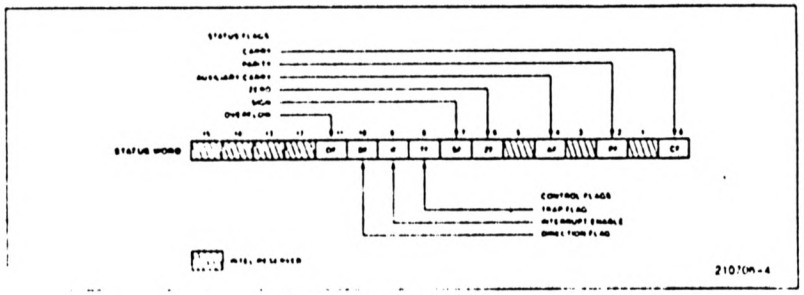


Figure 3b. Status Word Format

Table 2. Status Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag—Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag—Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag—Set if result is zero; cleared otherwise
7	SF	Sign Flag—Set equal to high-order bit of result (0 if positive, 1 if negative)
8	TF	Single Step Flag—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-Enable Flag—When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag—Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag—Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Figure 4.

An 80188 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory. Specific operand addressing modes are discussed later in this data sheet.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment registers (code, data, stack, extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 5). This allows for a 1 MByte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 3). These rules follow the way programs are written (see Figure 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack
ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero
LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word
FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for TEST pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Figure 4. 80188 Instruction Set

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign
JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign
UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

Figure 4. 80188 Instruction Set (Continued)

To access operands that do not reside in one of the four immediately available segments, a full 32-bit pointer can be used to reload both the base (segment) and offset values.

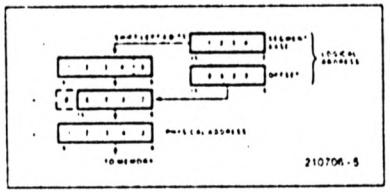


Figure 5. Two Component Address

Table 3. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references which use the DI register as an index.
Local Data	Data (DS)	All other data references.

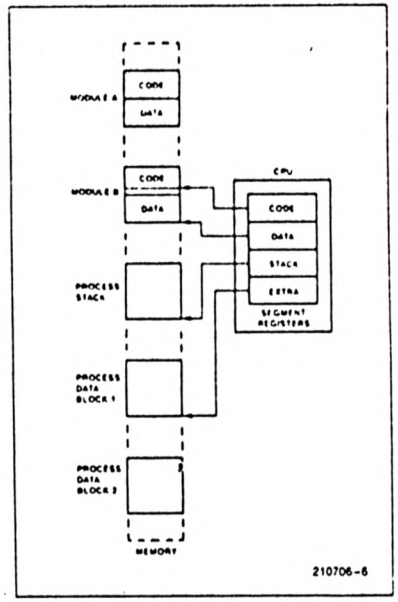


Figure 6. Segmented Memory Helps Structure Software

Addressing Modes

The 80188 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an index register.
- *Based Indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The 80188 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using an 8087 Numeric Data Coprocessor with the 80188.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.
- *Floating Point:* A signed 32-, 64-, or 80-bit real number representation. (Floating point operands are supported using an 8087 Numeric Data Coprocessor with the 80188.)

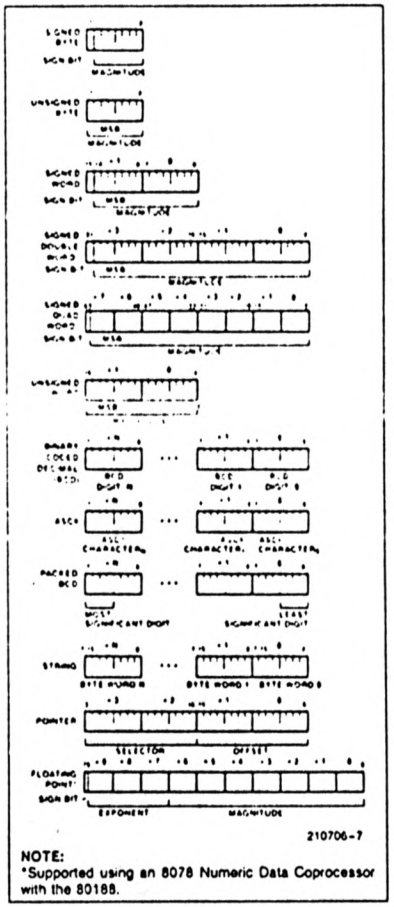
In general, individual data elements must fit within defined segment limits. Figure 7 graphically represents the data types supported by the 80188.

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A_{15}–A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.



NOTE:
*Supported using an 8078 Numeric Data Coprocessor with the 80188.

Figure 7. 80188 Supported Data Types

Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. If the exception was caused by executing an ESC instruction with the ESC trap bit set in the relocation register, the return instruction will point to the ESC instruction, or to the segment override prefix immediately preceding the ESC instruction if the prefix was present. In all other cases, the return address from an exception will point at the instruction immediately following the instruction causing the exception.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0–31, some of which are used for instruction exceptions, are reserved. Table 4 shows the 80188 predefined types and default priority levels. For each interrupt, an 8-bit vector must be supplied to the 80188 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. In addition, internal peripherals and noncascaded external interrupts will generate their own vectors through the internal interrupt controller. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Interrupt Sources

The 80188 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INTO, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type (Table 4), multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

The software generated 80188 interrupts are described below.

DIVIDE ERROR EXCEPTION (TYPE 0)

Generated when a DIV or IDIV instruction quotient cannot be expressed in the number of bits in the destination.

SINGLE-STEP INTERRUPT (TYPE 1)

Generated after most instructions if the TF flag is set. Interrupts will not be generated after prefix instructions (e.g., REP), instructions which modify segment registers (e.g., POP DS), or the WAIT instruction.

NON-MASKABLE INTERRUPT—NMI (TYPE 2)

An external interrupt source which cannot be masked.

Table 4. 80188 Interrupt Vectors

Interrupt Name	Vector Type	Vector Address	Default Priority	Related Instructions	Applicable Notes
Divide Error Exception	0	00H	1	DIV, IDIV	1
Single Step Interrupt	1	04H	1A	All	2
Non-Maskable Interrupt (NMI)	2	08H	1	All	
Breakpoint Interrupt	3	0CH	1	INT	1
INT0 Detected Overflow Exception	4	10H	1	INTO	1
Array Bounds Exception	5	14H	1	BOUND	1
Unused Opcode Exception	6	18H	1	Undefined Opcodes	1
ESC Opcode Exception	7	1CH	1	ESC Opcodes	1, 3
Timer 0 Interrupt	8	20H	2A		4
Timer 1 Interrupt	18	48H	2B		4
Timer 2 Interrupt	19	4CH	2C		4
Reserved	9	24H	3		
DMA 0 Interrupt	10	28H	4		
DMA 1 Interrupt	11	2CH	5		
INT0 Interrupt	12	30H	6		
INT1 Interrupt	13	34H	7		
INT2 Interrupt	14	38H	8		
INT3 Interrupt	15	3CH	9		
Reserved	16, 17	40H, 44H			
Reserved	20-31	50H . . . 7CH			

NOTES:
Default priorities for the interrupt sources are used only if the user does not program each source into a unique priority level.
1. Generated as a result of an instruction execution.
2. Performed in same manner as 8086.
3. An ESC opcode will cause a trap if the power-up bit is set in the peripheral control block relocation register.
4. All three timers constitute one source of request to the interrupt controller. As such, they share the same priority level with respect to other interrupt sources. However, the timers have a defined priority order among themselves (2A > 2B > 2C).

BREAKPOINT INTERRUPT (TYPE 3)

A one-byte version of the INT instruction. It uses 12 as an index into the service routine address table (because it is a type 3 interrupt).

INT0 DETECTED OVERFLOW EXCEPTION (TYPE 4)

Generated during an INT0 instruction if the OF bit is set.

ARRAY BOUNDS EXCEPTION (TYPE 5)

Generated during a BOUND instruction if the array index is outside the array bounds. The array bounds are located in memory at a location indicated by one of the instruction operands. The other operand indicates the value of the index to be checked.

UNUSED OPCODE EXCEPTION (TYPE 6)

Generated if execution is attempted on undefined opcodes.

ESCAPE OPCODE EXCEPTION (TYPE 7)

Generated if execution is attempted of ESC opcodes (D8H-DFH). This exception will only be generated if a bit in the relocation register is set. The return address of this exception will point to the ESC instruction causing the exception. If a segment override prefix preceded the ESC instruction, the return address will point to the segment override prefix.

Hardware-generated interrupts are divided into two groups: maskable interrupts and non-maskable interrupts. The 80188 provides maskable hardware interrupt request pins INT0-INT3. In addition, maskable interrupts may be generated by the 80188 integrated DMA controller and the integrated timer unit. The vector types for these interrupts are shown in Table 4. Software enables these inputs by setting the Interrupt Flag bit (IF) in the Status Word. The interrupt controller is discussed in the peripheral section of this data sheet.

Further maskable interrupts are disabled while servicing an interrupt because the IF bit is reset as part of the response to an interrupt or exception. The saved Status Word will reflect the enable status of the processor prior to the interrupt. The interrupt flag will remain zero unless specifically set. The interrupt return instruction restores the Status Word, thereby restoring the original status of IF bit. If the interrupt return re-enables interrupts, and another interrupt is pending, the 80188 will immediately service the highest-priority interrupt pending, i.e., no instructions of the main line program will be executed.

Non-Maskable Interrupt Request (NMI)

A non-maskable interrupt (NMI) is also provided. This interrupt is serviced regardless of the state of the IF bit. A typical use of NMI would be to activate a power failure routine. The activation of this input causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed. The IF bit is cleared at the beginning of an NMI interrupt to prevent maskable interrupts from being serviced.

Single-Step Interrupt

The 80188 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single-step interrupt and is controlled by the single-step flag bit (TF) in the Status Word. Once this bit is set, an internal single-step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single-stepped.

Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{RES}$ input pin LOW. $\overline{RES}$ forces the 80188 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the 80188 begins execution with the instruction at physical location FFFF0(H). $\overline{RES}$ also sets some registers to predefined values as shown in Table 5.

Table 5. 80188 Initial Register State after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

THE 80188 COMPARED TO THE 80186

The 80188 CPU is an 8-bit processor designed around the 80186 internal structure. Most internal functions of the 80188 are identical to the equivalent 80186 functions. The 80188 handles the external bus the same way the 80186 does with the distinction of handling only 8 bits at a time. Sixteen bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. The differences between the 80188 and the 80186 are outlined below. Internally, there are three differences between the 80188 and the 80186. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the 80188, whereas the 80186 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The 80188 BIU will fetch a new instruction to load into the queue each time there is a 1-byte hole (space available) in the queue. The 80186 waits until a 2-byte space is available.
- The internal execution time of the instruction is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU may also be limited by the speed of instruction fetches when a series of simple operations occur. When the more sophisticated instructions of the 80188 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

The 80188 and 80186 are completely software compatible by virtue of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally well on an 80188 or an 80186.

The hardware interface of the 80188 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes.

- A8–A15—These pins are only address outputs on the 80188. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.
- $\overline{BHE}$ has no meaning on the 80188 and has been eliminated.

80188 Clock Generator

The 80188 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

Oscillator

The oscillator circuit of the 80188 is designed to be used with a parallel resonant fundamental mode crystal. This is used as the time base for the 80188. The crystal frequency selected will be double the CPU clock frequency. Use of an LC or RC circuit is not recommended with this oscillator. If an external oscillator is used, it can be connected directly to input pin X1 in lieu of a crystal. The output of the oscillator is not directly available outside the 80188. The recommended crystal configuration is shown in Figure 8.

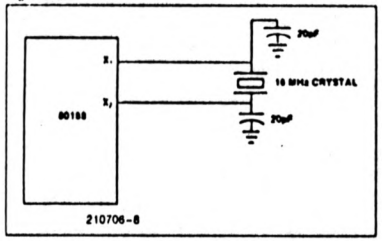


Figure 8. Recommended 80188 Crystal Configuration

The following parameters may be used for choosing a crystal:

Temperature Range:	0 to 70°C
ESR (Equivalent Series Resistance):	30Ω max
C_0 (Shunt Capacitance of Crystal):	7.0 pf max
C_L (Load Capacitance):	20 pf ± 2 pf
Drive Level:	1 mW max

Clock Generator

The 80188 clock generator provides the 50% duty cycle processor clock for the 80188. It does this by dividing the oscillator output by 2 forming the symmetrical clock. If an external oscillator is used, the state of the clock generator will change on the falling edge of the oscillator signal. The CLKOUT pin provides the processor clock signal for use outside the 80188. This may be used to drive other system components. All timings are referenced to the output clock.

READY Synchronization

The 80188 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T_2, T_3, and again in the middle of each T_W until ARDY is sampled HIGH. One-half CLKOUT cycle of resolution time is used for full synchronization of a rising ARDY signal. A high-to-low transition on ARDY may be used as an indication of the not ready condition but it must be performed synchronously to CLKOUT either in the middle of T_2, T_3, or T_W, or at the falling edge of T_3 or T_W.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T_2, T_3, and again at the end of each T_W until it is sampled HIGH. By using this input rather than the asynchronous ready input the half-clock cycle resolution time penalty is eliminated.

This input must satisfy set-up and hold times to guarantee proper operation of the circuit.

In addition, the 80188, as part of the integrated chip-select logic, has the capability to program WAIT states for memory and peripheral blocks. This is discussed in the Chip Select/Ready Logic description.

RESET Logic

The 80188 provides both a $\overline{RES}$ input pin and a synchronized RESET output pin for use with other system components. The $\overline{RES}$ input pin on the 80188 is provided with hysteresis in order to facilitate power-on Reset generation via an RC network. RESET is guaranteed to remain active for at least five clocks given a $\overline{RES}$ input of at least six clocks. RESET may be delayed up to approximately two and one-half clocks behind $\overline{RES}$.

Multiple 80188 processors may be synchronized through the $\overline{RES}$ input pin, since this input resets

both the processor and divide-by-two internal counter in the clock generator. In order to insure that the divide-by-two counters all begin counting at the same time, the active going edge of $\overline{RES}$ must satisfy a 25 ns setup time before the falling edge of the 80188 clock input. In addition, in order to insure that all CPUs begin executing in the same clock cycle, the reset must satisfy a 25 ns setup time before the rising edge of the CLKOUT signal of all the processors.

LOCAL BUS CONTROLLER

The 80188 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

Memory/Peripheral Control

The 80188 provides ALE, $\overline{RD}$, and $\overline{WR}$ bus control signals. The $\overline{RD}$ and $\overline{WR}$ signals are used to strobe data from memory or I/O to the 80188 or to strobe data from the 80188 to memory or I/O. The ALE line provides a strobe to latch the address when it is valid. The 80188 local bus controller does not provide a memory/$\overline{I/O}$ signal. If this is required, use the $\overline{S2}$ signal (which will require external latching), make the memory and I/O spaces nonoverlapping, or use only the integrated chip-select circuitry.

Transceiver Control

The 80188 generates two control signals for external transceiver chips. This capability allows the addition of transceivers for extra buffering without adding external logic. These control lines, DT/$\overline{R}$ and $\overline{DEN}$, are generated to control the flow of data through the transceivers. The operation of these signals is shown in Table 6.

Table 6. Transceiver Control Signals Description

Pin Name	Function
$\overline{DEN}$ (Data Enable)	Enables the output drivers of the transceivers. It is active LOW during memory, I/O, or INTA cycles.
DT/$\overline{R}$ (Data Transmit/Receive)	Determines the direction of travel through the transceivers. A HIGH level directs data away from the processor during write operations, while a LOW level directs data toward the processor during a read operation.

Local Bus Arbitration

The 80188 uses a HOLD/HLDA system of local bus exchange. This provides an asynchronous bus exchange mechanism. This means multiple masters utilizing the same bus can operate at separate clock frequencies. The 80188 provides a single HOLD/HLDA pair through which all other bus masters may gain control of the local bus. External circuitry must arbitrate which external device will gain control of the bus when there is more than one alternate local bus master. When the 80188 relinquishes control of the local bus, it floats $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S0}$–$\overline{S2}$, $\overline{LOCK}$, AD0–AD7, A8–A19, $\overline{S7}$, and DT/$\overline{R}$ to allow another master to drive these lines directly.

The 80188 HOLD latency time, i.e., the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is the highest-priority activity request which the processor may receive; higher than instruction fetching or internal DMA cycles. However, if a DMA cycle is in progress, the 80188 will complete the transfer before relinquishing the bus. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency time can be as great as 4 bus cycles. This will occur if a DMA word transfer operation is taking place from an odd address to an odd address. This is a total of 16 clocks or more, if WAIT states are required. In addition, if locked transfers are performed, the HOLD latency time will be increased by the length of the locked transfer.

Local Bus Controller and Reset

During RESET the local bus controller will perform the following actions:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ HIGH for one clock cycle, then float.

NOTE:
$\overline{RD}$ is also provided with an internal pull-up device to prevent the processor from inadvertently entering Queue Status mode during reset.

- Drive $\overline{S0}$–$\overline{S2}$ to the inactive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Three-state AD0–7, A8–19, S7, DT/$\overline{R}$.
- Drive ALE LOW (ALE is never floated).
- Drive HLDA LOW.

INTERNAL PERIPHERAL INTERFACE

All the 80188 integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D_{7-0}, SRDY, and ARDY will be ignored. The base address of the control block must be on an even 256-byte boundary (i.e., the lower 8 bits of the base address are all zeros). All of the defined registers within this control block may be read or written by the 80188 CPU at any time

The control block base address is programmed by a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block (see Figure 9). It provides the upper 12 bits of the base address of the control block. Note that mapping the control register block into an address range corresponding to a chip-select range is not recommended (the chip select circuitry is discussed later in this data sheet. In addition, bit 12 of this register determines whether the control block will be mapped into I/O or memory space. If this bit is 1, the control block will be located in memory space. If the bit is 0, the control block will be located in I/O space. If the control register block is mapped into I/O space, the upper 4 bits of the base address must be programmed as 0 (since I/O addresses are only 16 bits wide).

Whenever mapping the 188 peripheral control block to another location, the programming of the relocation register should be done with a byte write (i.e. OUT DX,AL). Any access to the control block is done 16 bits at a time. Thus, internally, the relocation register will get written with 16 bits of the AX register while externally, the BIU will run only one 8 bit bus cycle. If a word instruction is used (i.e. OUT DX,AX), the relocation register will be written on the first bus cycle. The BIU will then run a second bus cycle which is unnecessary. The address of the second bus cycle will no longer be within the control block (i.e. the control block was moved on the first cycle), and therefore, will require the generation of an external ready signal to complete the cycle. For this reason we recommend byte operations to the relocation register. Byte instructions may also be used for the other registers in the control block and will eliminate half of the bus cycles required if a word operation had been specified. Byte operations are only valid on even addresses though, and are undefined on odd addresses.

In addition to providing relocation information for the control block, the relocation register contains bits which place the interrupt controller into slave mode, and cause the CPU to interrupt upon encountering ESC instructions. At RESET, the relocation register is set to 20FFH which maps the control block to start at FF00H in I/O space. An offset map of the 256-byte control register block is shown in Figure 10.

CHIP-SELECT/READY GENERATION LOGIC

The 80188 contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The 80188 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address

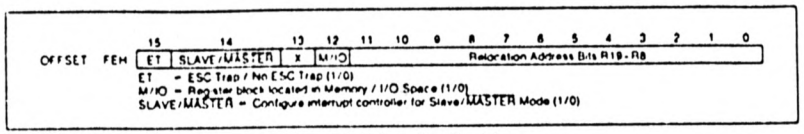


Figure 9. Relocation Register

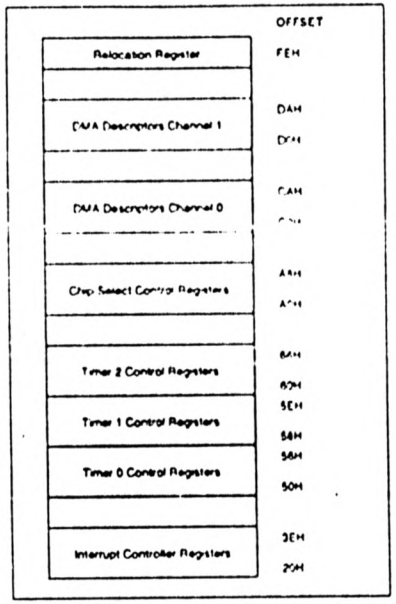


Figure 10. Internal Register Map

of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes.

Upper Memory $\overline{CS}$

The 80188 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the 80188 begins executing at memory location FFFF0H.

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 7 shows the relationship between the base address selected and the size of the memory block obtained.

Table 7. UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0 = R1 = R2 = 0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

The lower limit of this memory block is defined in the UMCS register (see Figure 11). This register is at offset A0H in the internal control block. The legal values for bits 6–13 and the resulting starting address and memory block sizes are given in Table 7. Any combination of bits 6–13 not shown in Table 7 will result in undefined operation. After reset, the UMCS register is programmed for a 1K area. It must be reprogrammed if a larger upper memory area is desired.

The internal generation of any 20-bit address whose upper 16 bits are equal to or greater than the UMCS value (with bits 0–5 as "0") asserts $\overline{UCS}$. UMCS bits R2–R0 specify the ready mode for the area of memory defined by the chip select register, as explained later.

Lower Memory $\overline{CS}$

The 80188 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The lower limit of memory defined by this chip select is always 0H, while the upper limit is programmable. By programming the upper limit, the size of the memory block is defined. Table 8 shows the relationship between the upper address selected and the size of the memory block obtained.

Table 8. LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0 = R1 = R2 = 0)
003FFH	1K	0038H
007FFH	2K	0078H
00FFFH	4K	00F8H
01FFFH	8K	01F8H
03FFFH	16K	03F8H
07FFFH	32K	07F8H
0FFFFH	64K	0FF8H
1FFFFH	128K	1FF8H
3FFFFH	256K	3FF8H

The upper limit of this memory block is defined in the LMCS register (see Figure 12) at offset A2H in the internal control block. The legal values for bits 6–15 and the resulting upper address and memory block sizes are given in Table 8. Any combination of bits 6–15 not shown in Table 8 will result in undefined operation. After reset, the LMCS register value is undefined. However, the $\overline{LCS}$ chip-select line will not become active until the LMCS register is accessed.

Any internally generated 20-bit address whose upper 16 bits are less than or equal to LMCS (with bits 0–5 "1") will assert $\overline{LCS}$. LMCS register bits R2–R0 specify the READY mode for the area of memory defined by this chip-select register.

Mid-Range Memory $\overline{CS}$

The 80188 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located within the 80188 1M byte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines, as shown in Table 9, is determined by bits 8–14 of the MPCS register (see Figure 13). This register is at location A8H in the internal control block. One and only one of bits 8–14 must be set at a time. Unpredictable operation of the $\overline{MCS}$ lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. If the total block size is 32K, each chip select is active for 8K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range.

The EX and MS in MPCS relate to peripheral functionality as described in a later section.

Table 9. MPCS Programming Values

Total Block Size	Individual Select Size	MPCS Bits 14–8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

The base address of the mid-range memory block is defined by bits 15–9 of the MMCS register (see Figure 14). This register is at offset A6H in the internal control block. These bits correspond to bits A19–A13 of the 20 bit memory address. Bits A12–A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the mid-range block size is 32K (or the size of the block for which each $\overline{MCS}$ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000H, 18000H, etc. After reset, the contents of both of these registers is undefined. However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

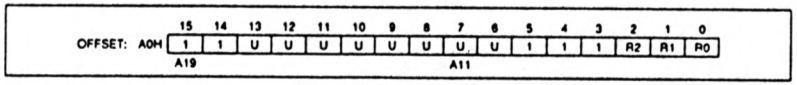


Figure 11. UMCS Register

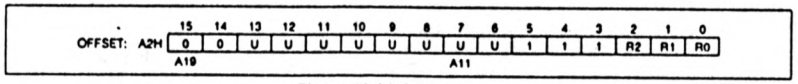


Figure 12. LMCS Register

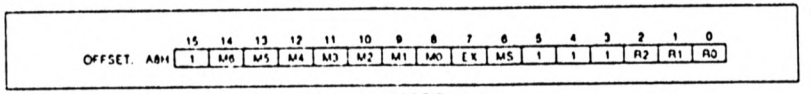


Figure 13. MPCS Register

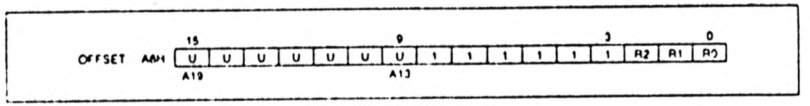


Figure 14. MMCS Register

MMCS bits R2–R0 specify READY mode of operation for all four mid-range chip selects.

The 512K block size for the mid-range memory chip selects is a special case. When using 512K, the base address would have to be at either locations 00000H or 80000H. If it were to be programmed at 00000H when the $\overline{LCS}$ line was programmed, there would be an internal conflict between the $\overline{LCS}$ ready generation logic and the $\overline{MCS}$ ready generation logic. Likewise, if the base address were programmed at 80000H, there would be a conflict with the $\overline{UCS}$ ready generation logic. Since the $\overline{LCS}$ chip-select line does not become active until programmed, while the $\overline{UCS}$ line is active at reset, the memory base can be set only at 00000H. If this base address is selected, however, the $\overline{LCS}$ range must not be programmed.

Peripheral Chip Selects

The 80188 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0}$–6 are generated by the 80188. The base address is user-programmable; however it can only be a multiple of 1K bytes, i.e., the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1 and A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0 and A1 pins used for selecting internal registers of 8-bit peripheral chips.

The starting address of the peripheral chip-select block is defined by the PACS register (see Figure 15). The register is located at offset A4H in the internal control block. Bits 15–6 of this register correspond to bits 19–10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9–0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12–15 must be programmed zero, since the I/O address is only 16 bits wide. Table 10 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

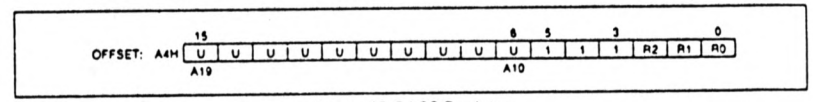


Figure 15. PACS Register

The user should program bits 15–6 to correspond to the desired peripheral base location. PACS bits 0–2 are used to specify READY mode for $\overline{PCS0}$–$\overline{PCS3}$.

Table 10. PCS Address Ranges

$\overline{PCS}$ Line	Active between Locations
$\overline{PCS0}$	PBA —PBA + 127
$\overline{PCS1}$	PBA + 128—PBA + 255
$\overline{PCS2}$	PBA + 256—PBA + 383
$\overline{PCS3}$	PBA + 384—PBA + 511
$\overline{PCS4}$	PBA + 512—PBA + 639
$\overline{PCS5}$	PBA + 640—PBA + 767
$\overline{PCS6}$	PBA + 768—PBA + 895

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the mid-range memory chip-select block, see Figure 13). The register is located at offset A8H in the internal control block. Bit 7 is used to select the function of $\overline{PCS5}$ and $\overline{PCS6}$, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 11 describes the programming of these bits. After reset, the contents of both the MPCS and the PACS registers are undefined, however none of the PCS lines will be active until both of the MPCS and PACS registers are accessed.

Table 11. MS, EX Programming Values

Bit	Description
MS	1 = Peripherals mapped into memory space.
	0 = Peripherals mapped into I/O space.
EX	0 = 5 $\overline{PCS}$ lines. A1, A2 provided.
	1 = 7 $\overline{PCS}$ lines. A1, A2 are not provided.

MPCS bits 0–2 specify the READY mode for $\overline{PCS4}$–$\overline{PCS6}$ as outlined below.

READY Generation Logic

The 80188 can generate a "READY" signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the 80188 may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

READY control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the 80188. The interpretation of the ready bits is shown in Table 12.

Table 12. READY Bits Programming

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external RDY also used.
0	0	1	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

The internal ready generator operates in parallel with external READY, not in series if the external READY is used (R2 = 0). For example, if the internal generator is set to insert two wait states, but activity on the external READY lines will insert four wait states, the processor will only insert four wait states, not six. This is because the two wait states generated by the internal generator overlapped the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2–R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2–R0 of PACS set the $\overline{PCS0}$–3 READY mode, R2–R0 of MPCS set the $\overline{PCS4}$–6 READY mode.

Chip Select/Ready Logic and Reset

Upon RESET, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

DMA Channels

The 80188 DMA controller provides two independent DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer. Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a data transfer rate of one MByte/sec at 8 MHz.

DMA Operation

Each channel has six registers in the control block which define each channel's operation. The control registers consist of a 20-bit Source pointer (2 words), a 20-bit Destination pointer (2 words), a 16-bit Transfer Count Register, and a 16-bit Control Word.

The format of the DMA Control Blocks is shown in Table 13. The Transfer Count Register (TC) specifies the number of DMA transfers to be performed. Up to 64K byte transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Figure 17). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 13. DMA Control Block Format

Register Name	Register Address	
	Ch. 0	Ch. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

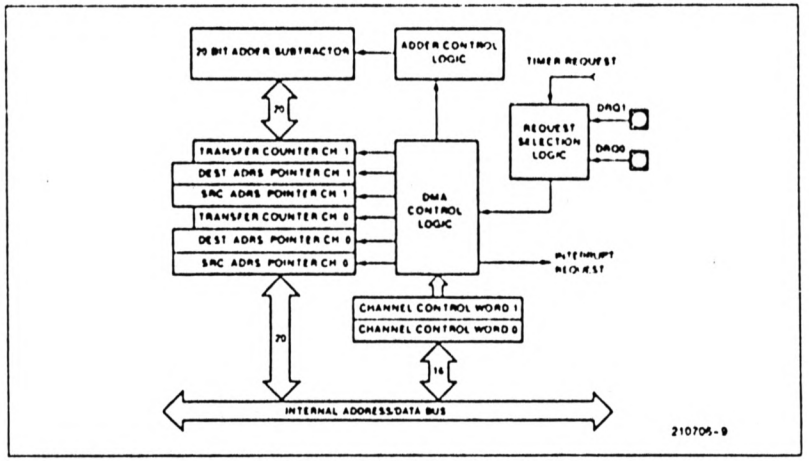


Figure 16. DMA Unit Block Diagram

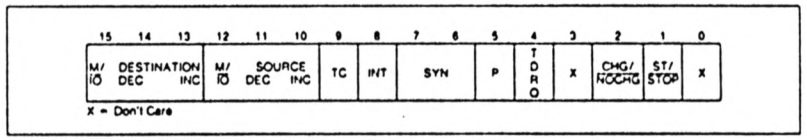


Figure 17. DMA Control Register

DMA Channel Control Word Register

Each DMA Channel Control Word determines the mode of operation for the particular 80188 DMA channel. This register specifies:

- the mode of synchronization;
- whether interrupts will be generated after the last transfer;
- whether DMA activity will cease after a programmed number of DMA cycles;
- the relative priority of the DMA channel with respect to the other DMA channel;
- whether the source pointer will be incremented, decremented, or maintained constant after each transfer;
- whether the source pointer addresses memory or I/O space;
- whether the destination pointer will be incremented, decremented, or maintained constant after each transfer; and
- whether the destination pointer will address memory or I/O space.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Control Word Bit Descriptions

DEST: M/$\overline{IO}$ Destination pointer is in memory (1) or I/O (0) space.

DEC Decrement destination pointer by 1 after each transfer.

INC Increment destination pointer by 1 after each transfer.

If both INC and DEC are specified, the pointer will not be changed after each cycle.

SOURCE: M/$\overline{IO}$ Source pointer is in memory (1) or I/O (0) space.

DEC Decrement source pointer by 1 after each transfer.

INC Increment source pointer by 1 after each transfer.

If both INC and DEC are specified, the pointer will not be changed after each cycle.

TC: If set, DMA will terminate when the contents of the transfer count register reach zero. The ST/$\overline{STOP}$ bit will also be reset at this point. If cleared, the DMA controller will decrement the transfer count register for each DMA cycle, but DMA transfers will not stop when the transfer count register reaches zero.

INT: Enable interrupts to CPU upon transfer count termination.

SYN: 00 No synchronization.

NOTE:

When unsynchronized transfers are specified, the TC bit will be ignored and the ST bit will be cleared upon the transfer count reaching zero, stopping the channel.

01 Source Synchronization.

10 Destination Synchronization.

11 Unused.

P: Channel priority relative to other channel.

0 Low priority.

1 High priority.

Channels will alternate cycles if both are set at the same priority level.

TDRQ: Enable/Disable (1/0) DMA requests from Timer 2.

CHG/$\overline{NOCHG}$: Change/Do Not Change (1/0) the ST/$\overline{STOP}$ bit. If this bit is set when writing the control word, the ST/$\overline{STOP}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{STOP}$ bit will not be altered. This bit is not stored; it will always be read as 0.

ST/$\overline{STOP}$: Start/Stop (1/0) Channel.

DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Figure 18). These pointers may be individually incremented or decremented after each transfer. Each pointer may point into either memory or I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on the values for the pointer registers.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). The register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set or if unsynchronized transfers are programmed, DMA activity will terminate when the transfer count register reaches zero.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming no wait states). When source synchronized or unsynchronized transfers are performed, data will not be fetched from the source address until the destination device signals that it is ready to receive it. Also, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another destination synchronized DMA cycle will begin after two processor clocks. This allows the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus, the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. Table 14 shows the maximum DMA transfer rates.

Table 14. Maximum DMA Transfer Rates @ 8 MHz

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	1.0 MBytes/sec	1.0 MBytes/sec
Source Synch	1.0 MBytes/sec	1.0 MBytes/sec
Destination Synch	0.67 MBytes/sec	0.80 MBytes/sec

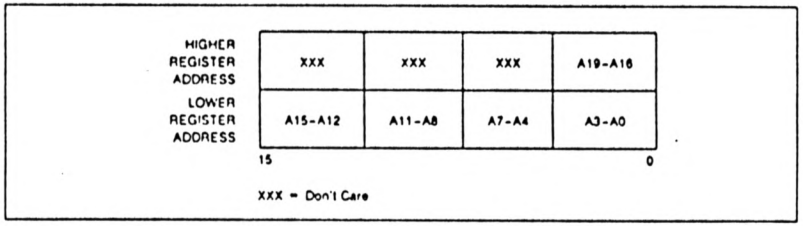


Figure 18. DMA Pointer Register Format

DMA Acknowledge

No explicit DMA acknowledge pulse is provided. Since both source and destination pointers are maintained, a read from a requesting source, or a write to a requesting destination, should be used as the DMA acknowledge signal. Since the chip-select lines can be programmed to be active for a given block of memory or I/O space, and the DMA pointers can be programmed to point to the same given block, a chip-select line could be used to indicate a DMA acknowledge.

DMA Priority

The DMA channels may be programmed to give one channel priority over the other, or they may be programmed to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses to odd memory locations; also, an external bus hold takes priority over an internal DMA cycle. Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time will suffer during sequences of continuous DMA cycles. An NMI request, however, will cause all internal DMA activity to halt. This allows the CPU to quickly respond to the NMI request.

DMA Programming

DMA cycles will occur whenever the ST/$\overline{\text{STOP}}$ bit of the Control Register is set. If synchronized transfers are programmed, a DRQ must also be generated. Therefore, the source and destination transfer pointers, and the transfer count register (if used) must be programmed before the ST/$\overline{\text{STOP}}$ bit is set.

Each DMA register may be modified while the channel is operating. If the CHG/$\overline{\text{NOCHG}}$ bit is cleared when the control register is written, the ST/$\overline{\text{STOP}}$ bit of the control register will not be modified by the write. If multiple channel registers are modified, it is recommended that a LOCKED string transfer be used to prevent a DMA transfer from occurring between updates to the channel registers.

DMA Channels and Reset

Upon RESET, the DMA channels will perform the following actions:

- The ST/$\overline{\text{STOP}}$ bit for each channel will be reset to STOP.
- Any transfer in progress is aborted.

TIMERS

The 80188 provides three internal 16-bit programmable timers (see Figure 19). Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

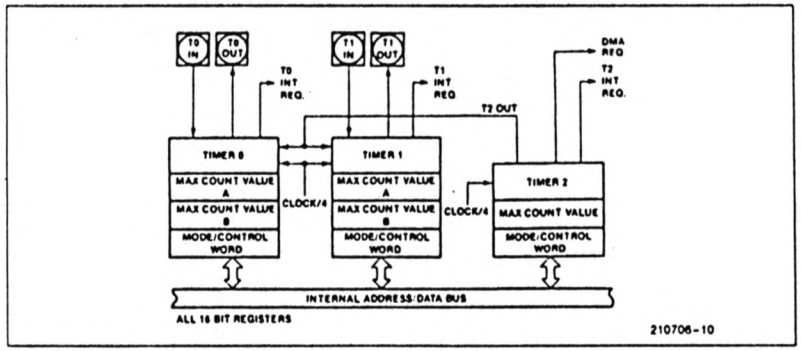


Figure 19. Timer Block Diagram

Timer Operation

The timers are controlled by 11 16-bit registers in the peripheral control block. The configuration of these registers is shown in Table 15. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a MAX COUNT register, which defines the maximum count the timer will reach. After reaching the MAX COUNT register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register itself. Timers 0 and 1 are, in addition, equipped with a second MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, 2 clocks after the maximum count value has been reached. In the dual MAX COUNT register mode, the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX COUNT registers, the RIU bit in the control register determines which is used for the comparison.

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate (2 MHz for an 8 MHz CPU clock). Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input.

Since the count registers and the maximum count registers are all 16 bits wide, 16 bits of resolution are provided. Any Read or Write access to the timers will add one wait state to the minimum four-clock bus cycle, however. This is needed to synchronize and coordinate the internal data flows between the internal timers and the internal bus.

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between MAX COUNT registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

These options are selectable via the timer mode/control word.

Timer Mode/Control Register

The mode/control register (see Figure 20) allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

Table 15. Timer Control Block Format

Register Name	Register Offset		
	Tmr. 0	Tmr. 1	Tmr. 2
Mode/Control Word	56H	5EH	66H
Max Count B	54H	5CH	not present
Max Count A	52H	5AH	62H
Count Register	50H	58H	60H

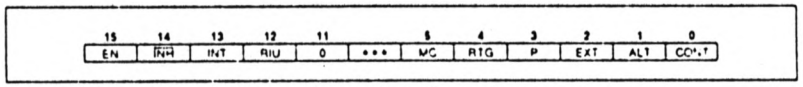


Figure 20. Timer Mode/Control Register

EN

The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transitions during the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

$\overline{INH}$

The inhibit bit allows for selective updating of the enable (EN) bit. If $\overline{INH}$ is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If $\overline{INH}$ is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT

When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual MAX COUNT register mode, an interrupt will be generated each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller.)

RIU

The Register In Use bit indicates which MAX COUNT register is currently being used for comparison to the timer count value. A zero value indicates register A. The RIU bit cannot be written, i.e., its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.

MC

The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts. Programmer intervention is required to clear this bit.

RTG

Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is HIGH, the timer will count; if the input pin is LOW, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the 80188 clock.

When RTG = 1, the input pin detects LOW-to-HIGH transitions. The first such transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

P

The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

EXT

The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the 80188 clock. If this bit is set, the timer will count LOW-to-HIGH transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

ALT

The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating non-repetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go LOW for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT

Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below.

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Count Registers

Each of the three timers has a 16-bit count register. The contents of this register may be read or written by the processor at any time. If the register is written while the timer is counting, the new value will take effect in the current count cycle.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two max count values whenever the current maximum count is reached. A timer resets when the timer count register equals the max count value being used. If the timer count register or the max count register is changed so that the max count is less than the timer count, the timer does not immediately reset. Instead, the timer counts up to 0FFFFH, "wraps around" to zero, counts up to the max count value, and then resets.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- For Timers 0 and 1, the RIU bits are reset to zero and the ALT bits are set to one. This results in the Timer Out pins going HIGH.

INTERRUPT CONTROLLER

The 80188 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80188 interrupt controller has its own control register that sets the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 21.

The 80188 has a special slave mode in which the internal interrupt controller acts as a slave to an external master. The controller is programmed into this mode by setting bit 14 in the peripheral control block relocation register. (See Slave Mode section.)

MASTER MODE OPERATION

Interrupt Controller External Interface

Five pins are provided for external interrupt sources. One of these pins is NMI, the non-maskable interrupt. NMI is generally used for unusual events such as power-fail interrupts. The other four pins may be configured in any of the following ways:

- As four interrupt input lines with internally generated interrupt vectors.
- As an interrupt line and interrupt acknowledge line pair (Cascade Mode) with externally generated interrupt vectors plus two interrupt input lines with internally generated vectors.
- As two pairs of interrupt/interrupt acknowledge lines (Cascade Mode) with externally generated interrupt vectors.

External sources in the cascade mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{INTA}$ cycles are initiated and the vector is read into the 80188 on the second cycle. The capability to interface to external 8259A programmable interrupt controllers is provided when the inputs are configured in cascade mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the 8259A. The interrupt controller responds indentically to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

FULLY NESTED MODE

When in the fully nested mode four pins are used as direct interrupt requests as in Figure 22. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in-service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate with interrupts enabled, yet be suspended only by interrupts of higher priority than the in-service interrupt.

When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register. This is required to allow subsequent interrupts from this interrupt source and to allow servicing of lower-priority interrupts. An EOI command is executed at the end of the service routine just before the return from interrupt instruction. If the fully nested structure has been upheld, the next highest-priority source with its IS bit set is then serviced.

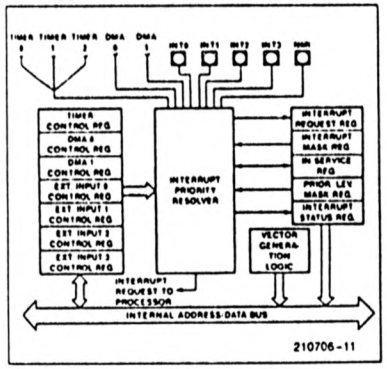


Figure 21. Interrupt Controller Block Diagram

CASCADE MODE

The 80188 has four interrupt pins and two of them have dual functions. In the fully nested mode the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In the cascade mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. The interconnection is shown in Figure 23. INT0 is an interrupt input interfaced to an 8259A, while INT2/$\overline{INTA0}$ serves as the dedicated interrupt acknowledge signal to that peripheral. The same is true for INT1 and INT3/$\overline{INTA1}$. Each pair can selectively be placed in the cascade or non-cascade mode by programming the proper value into INT0 and INT1 control registers. The use of the dedicated acknowledge signals eliminates the need for the use of external logic to generate $\overline{INTA}$ and device select signals.

The primary cascade mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave 8259As. Three levels of priority are created, requiring priority resolution in the 80188 interrupt controller, the master 8259As, and the slave 8259As. If an external interrupt is serviced, one IS bit is set at each of those levels. When the interrupt service routine is completed, up to three end-of-interrupt commands must be issued by the programmer.

SPECIAL FULLY NESTED MODE

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external 8259A masters. Normally, an interrupt request from an interrupt source will not be recognized unless the in-service bit for that source is reset. If more than one interrupt source is connected to an external interrupt controller, all of the interrupts will be funneled through the same 80188 interrupt request pin. As a result, if the external interrupt controller receives a higher-priority interrupt, its interrupt will not be recognized by the 80188 controller until the 80188 in-service bit is reset. In special fully nested mode, the 80188 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin. An in-service bit will continue to be

set, however, to inhibit interrupts from other lower-priority 80188 interrupt sources.

Special procedures should be followed when resetting IS bits at the end of interrupt service routines. Software polling of the IS register in the external master 8259A is required to determine if there is more than one bit set. If so, the IS bit in the 80188 remains active and the next interrupt service routine is entered.

Operation in a Polled Environment

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the Poll Word (Figure 32). Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service. Bits 0–4 indicate to the processor the type vector of the highest-priority source requesting service. Reading the Poll Word causes the In-Service bit of the highest priority source to be set.

It is desirable to be able to read the Poll Word information without guaranteeing service of any pending interrupt, i.e., not set the indicated in-service bit. The 80188 provides a Poll Status Word in addition to the conventional Poll Word to allow this to be done. Poll Word information is duplicated in the Poll Status Word, but reading the Poll Status Word does not set the associated in-service bit. These words are located in two adjacent memory locations in the register file.

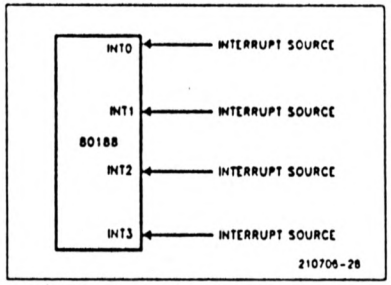


Figure 22. Fully Nested (Direct) Mode Interrupt Controller Connections

Master Mode Features

PROGRAMMABLE PRIORITY

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority). All interrupt sources have preprogrammed default priority levels (see Table 4).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 4 is used. If the serviced interrupt routine reenables interrupts, other interrupt requests can be serviced.

END-OF-INTERRUPT COMMAND

The end-of-interrupt (EOI) command is used by the programmer to reset the In-Service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The nonspecific command does not specify which IS bit is reset. When issued, the interrupt controller automatically resets the IS bit of the highest priority source with an active service routine. A specific EOI command requires that the programmer send the interrupt vector type to the interrupt controller indicating which source's IS bit is to be reset. This command is used when the fully nested structure has been disturbed or the highest priority IS bit that was set does not belong to the service routine in progress.

TRIGGER MODE

The four external interrupt pins can be programmed in either edge- or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active HIGH. In the edge sense mode or the level-trigger mode, the interrupt request must remain active (HIGH) until the interrupt request is acknowledged by the 80188 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go LOW for at least one clock cycle to reenable the input. In the level-trigger mode, no such provision is made: holding the interrupt input HIGH will cause continuous interrupt requests.

INTERRUPT VECTORING

The 80188 Interrupt Controller will generate interrupt vectors for the integrated DMA channels and the integrated Timers. In addition, the Interrupt Controller will generate interrupt vectors for the external interrupt lines if they are not configured in Cascade or Special Fully Nested Mode. The interrupt vectors generated are fixed and cannot be changed (see Table 4).

Interrupt Controller Registers

The Interrupt Controller register model is shown in Figure 24. It contains 15 registers. All registers can both be read or written unless specified otherwise.

IN-SERVICE REGISTER

This register can be read from or written into. The format is shown in Figure 25. It contains the In-Service bit for each of the interrupt sources. The In-Service bit is set to indicate that a source's service routine is in progress. When an In-Service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the In-Service bit for all three timers; the D0 and D1 bits are the In-Service bits for the two DMA channels; the I0–I3 are the In-Service bits for the external interrupt pins. The IS bit is set when the processor acknowledges an interrupt request either by an interrupt acknowledge or by reading the poll register. The IS bit is reset at the end of the interrupt service routine by an end-of-interrupt command.

INTERRUPT REQUEST REGISTER

The internal interrupt sources have interrupt request bits inside the interrupt controller. The format of this register is shown in Figure 25. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

The state of the external interrupt input pins is also indicated. The state of the external interrupt pins is not a stored condition inside the interrupt controller, therefore the external interrupt bits cannot be written. The external interrupt request bits are set when an interrupt request is given to the interrupt controller, so if edge-triggered mode is selected, the bit in the register will be HIGH only after an inactive-to-active transition. For internal interrupt sources, the register bits are set when a request arrives and are reset when the processor acknowledges the requests.

Writes to to the interrupt request register will affect the D0 and D1 interrupt request bits. Setting either bit will cause the corresponding interrupt request while clearing either bit will remove the corresponding interrupt request. All other bits in the register are read-only.

MASK REGISTER

This is a 16-bit register that contains a mask bit for each interrupt source. The format for this register is shown in Figure 25. A one in a bit position corresponding to a particular source masks the source from generating interrupts. These mask bits are the exact same bits which are used in the individual control registers; programming a mask bit using the mask register will also change this bit in the individual control registers, and vice versa.

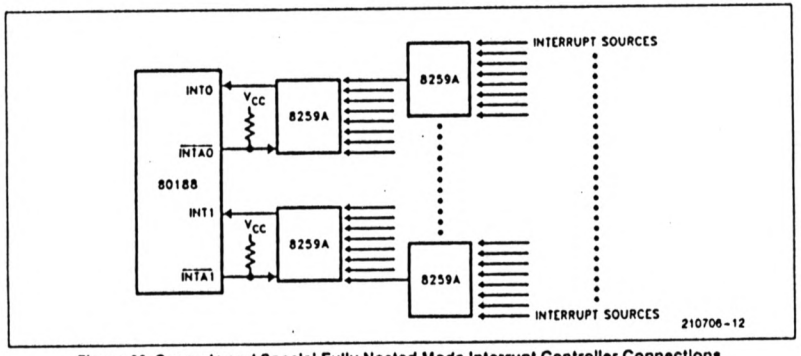


Figure 23. Cascade and Special Fully Nested Mode Interrupt Controller Connections

	OFFSET
INT3 CONTROL REGISTER	3EH
INT2 CONTROL REGISTER	3CH
INT1 CONTROL REGISTER	3AH
INT0 CONTROL REGISTER	38H
DMA 1 CONTROL REGISTER	36H
DMA 0 CONTROL REGISTER	34H
TIMER CONTROL REGISTER	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY MASK REGISTER	2AH
MASK REGISTER	28H
POLL STATUS REGISTER	26H
POLL REGISTER	24H
EOI REGISTER	22H

Figure 24. Interrupt Controller Registers (Master Mode)

PRIORITY MASK REGISTER

This register masks all interrupts below a particular interrupt priority level. The format of this register is shown in Figure 26. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified. For example, 100 written into this register masks interrupts of level five (101), six (110), and seven (111). The register is reset to seven (111) upon RESET so no interrupts are masked due to priority number.

INTERRUPT STATUS REGISTER

This register contains general interrupt controller status information. The format of this register is shown in Figure 27. The bits in the status register have the following functions:

DHLT: DMA Halt Transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed. This bit allows prompt service of all non-maskable interrupts. This bit may also be set by the programmer.

IRTx: These three bits represent the individual timer interrupt request bits. These bits differentiate between timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt requests. Note that setting any one of these three bits initiates an interrupt request to the interrupt controller.

15	14	•	•	•	10	9	8	7	6	5	4	3	2	1	0
0	0	•	•	•	0	0	0	I3	I2	I1	I0	D1	D0	0	TMR

Figure 25. In-Service, Interrupt Request, and Mask Register Formats

15	14	•	•	•	•	•	•	•	•	•	•	3	2	1	0
0	0	•	•	•	•	•	•	•	•	•	•	0	PRM2	PRM1	PRM0

Figure 26. Priority Mask Register Format

15	14	•	•	•	•	•	•	7	6	5	4	3	2	1	0
DHLT	0	•	•	•	•	•	•	0	0	0	0	0	IRT2	IRT1	IRT0

Figure 27. Interrupt Status Register Format (non-RMX Mode)

TIMER, DMA 0, 1; CONTROL REGISTERS

These registers are the control words for all the internal interrupt sources. The format for these registers is shown in Figure 28. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are the exact same bits as are in the Mask Register; modifying them in the individual control registers will also modify them in the Mask Register, and vice versa.

INT0-INT3 CONTROL REGISTERS

These registers are the control words for the four external input pins. Figure 29 shows the format of the INT0 and INT1 Control registers; Figure 30 shows the format of the INT2 and INT3 Control registers. In cascade mode or special fully nested mode, the control words for INT2 and INT3 are not used.

The bits in the various control registers are encoded as follows:

PR0-2: Priority programming information. Highest priority = 000, lowest priority = 111.

LTM: Level-triggor mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = non-mask.

C: Cascade mode bit, 1 = cascade; 0 = direct.

SFNM: Special fully nested mode bit, 1 = SFNM.

EOI REGISTER

The end of the interrupt register is a command register which can only be written into. The format of this register is shown in Figure 31. It initiates an EOI command when written to by the 80188 CPU.

The bits in the EOI register are encoded as follows:

S_x: Encoded information that specifies an interrupt source vector type as shown in Table 4. For example, to reset the In-Service bit for DMA channel 0, these bits should be set to 01010, since the vector type for DMA channel 0 is 10.

NOTE:
To reset the single In-Service bit for any of the three timers, the vector type for timer 0 (8) should be written in this register.

NSPEC/SPEC: A bit that determines the type of EOI command. Nonspecific = 1, Specific = 0.

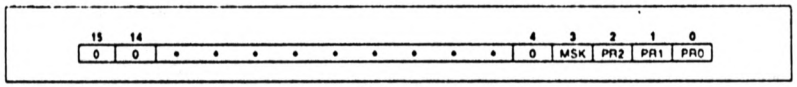


Figure 28. Timer/DMA Control Register Formats

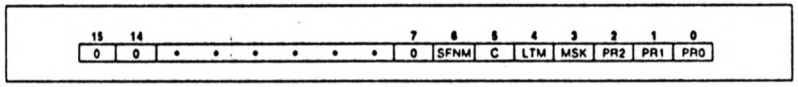


Figure 29. INT0/INT1 Control Register Formats

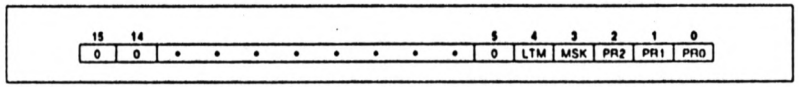


Figure 30. INT2/INT3 Control Register Formats

POLL AND POLL STATUS REGISTERS

These registers contain polling information. The format of these registers is shown in Figure 32. They can only be read. Reading the Poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt. Reading the poll status register will not set the IS bit of the highest priority pending interrupt; only the status of pending interrupts will be provided.

Encoding of the Poll and Poll Status register bits are as follows:

S_x: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt Request = 1, no Interrupt Request = 0.

SLAVE MODE OPERATION

When slave mode is used, the internal 80188 interrupt controller will be used as a slave controller to an external master interrupt controller. The internal 80188 resources will be monitored by the internal interrupt controller, while the external controller functions as the system master interrupt controller. Upon reset, the 80188 will be in master mode. To provide for slave mode operation bit 14 of the relocation register should be set.

Because of pin limitations caused by the need to interface to an external 8259A master, the internal interrupt controller will no longer accept external inputs. There are however, enough 80188 interrupt controller inputs (internally) to dedicate one to each timer. In this mode, each timer interrupt source has its own mask bit, IS bit, and control word.

In slave mode each peripheral must be assigned a unique priority to ensure proper interrupt controller operation. Therefore, it is the programmer's responsibility to assign correct priorities and initialize interrupt control registers before enable interrupts.

Slave Mode External Interface

The configuration of the 80188 with respect to an external 8259A master is shown in Figure 33. The INT0 (pin 45) input is used as the 80188 CPU interrupt input. INT3 (pin 41) functions as an output to send the 80188 slave-interrupt-request to one of the 8 master-PIC-inputs.

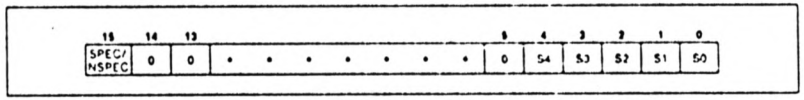


Figure 31. EOI Register Format

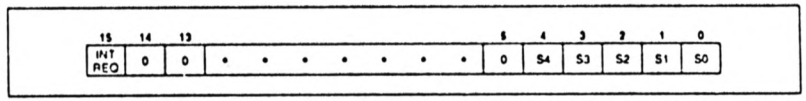


Figure 32. Poll and Poll Status Register Format

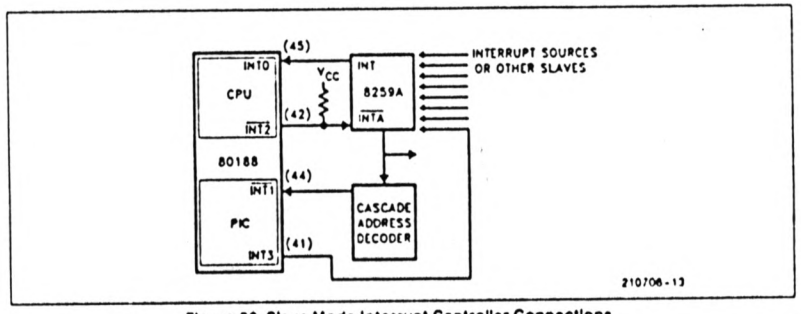


Figure 33. Slave Mode Interrupt Controller Connections

Correct master-slave interface requires decoding of the slave addresses (CAS0–2). Slave 8259As do this internally. Because of pin limitations, the 80188 slave address will have to be decoded externally. $\overline{INT1}$ (pin 44) is used as a slave-select input. Note that the slave vector address is transferred internally, but the READY input must be supplied externally.

$\overline{INT2}$ (pin 42) is used as an acknowledge output, suitable to drive the $\overline{INTA}$ input of an 8259A.

Interrupt Nesting

Slave mode operation allows nesting of interrupt requests. When an interrupt is acknowledged, the priority logic masks off all priority levels except those with equal or higher priority.

Vector Generation In the Slave Mode

Vector generation in slave mode is exactly like that of an 8259A slave. The interrupt controller generates an 8-bit vector which the CPU multiplies by four and uses as an address into a vector table. The significant five bits of the vector are user-programmable while the lower three bits are generated by the priority logic. These bits represent the encoding of the priority level requesting service. The significant five bits of the vector are programmed by writing to the Interrupt Vector register at offset 20H.

Specific End-of-Interrupt

In slave mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset. The command is executed by writing the correct value in the Specific EOI register at offset 22H.

Interrupt Controller Registers in the Slave Mode

All control and command registers are located inside the internal peripheral control block. Figure 34 shows the offsets of these registers.

END-OF-INTERRUPT REGISTER

The end-of-interrupt register is a command register which can only be written. The format of this register is shown in Figure 35. It initiates an EOI command when written by the 80188 CPU.

The bits in the EOI register are encoded as follows:

L_X: Encoded value indicating the priority of the IS bit to be reset.

IN-SERVICE REGISTER

This register can be read from or written into. It contains the in-service bit for each of the internal interrupt sources. The format for this register is shown in Figure 36. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers. The source's IS bit is set when the processor acknowledges its interrupt request.

INTERRUPT REQUEST REGISTER

This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Figure 36. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request. As in master mode, D0 and D1 are read/write, all other bits are read only.

MASK REGISTER

The register contains a mask bit for each interrupt source. The format for this register is shown in Figure 36. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bits are exactly the same bits which are used in the individual control registers, i.e., changing the state of a mask bit in this register will also change the state of the mask bit in the individual interrupt control register corresponding to the bit.

CONTROL REGISTERS

These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Figure 37. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are encoded as follows:

pr_x: 3-bit encoded field indicating a priority level for the source; note that each source must be programmed at specified levels.

msk: mask bit for the priority level indicated by pr_x bits.

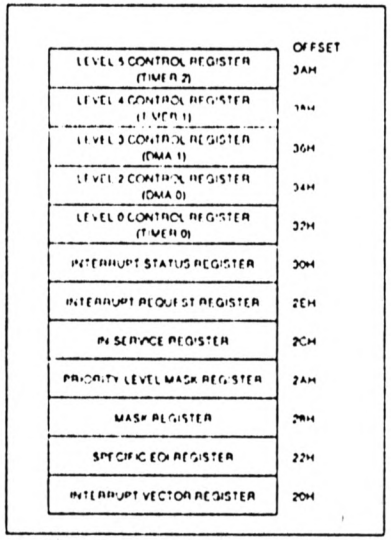


Figure 34. Interrupt Controller Registers (Slave Mode)

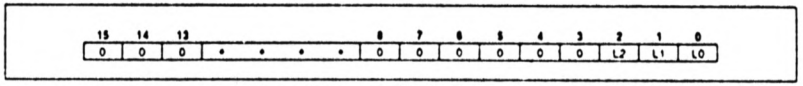


Figure 35. Specific EOI Register Format

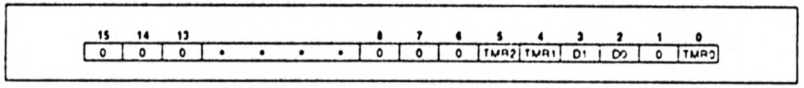


Figure 36. In-Service, Interrupt Request, and Mask Register Format

INTERRUPT VECTOR REGISTER

This register provides the upper five bits of the interrupt vector address. The format of this register is shown in Figure 38. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.

The format of the bits in this register is:

t_x: 5-bit field indicating the upper five bits of the vector address.

PRIORITY-LEVEL MASK REGISTER

This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:

m_x: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

INTERRUPT STATUS REGISTER

This register is defined as in master mode except that DHLT is not implemented. (See Figure 27).

Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Request bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to master mode.

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	0	0	MSK	PR2	PR1	PR0

Figure 37. Control Word Format

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	14	13	12	11	10	0	0	0

Figure 38. Interrupt Vector Register Format

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	0	0	0	m2	m1	m0

Figure 39. Priority Level Mask Register

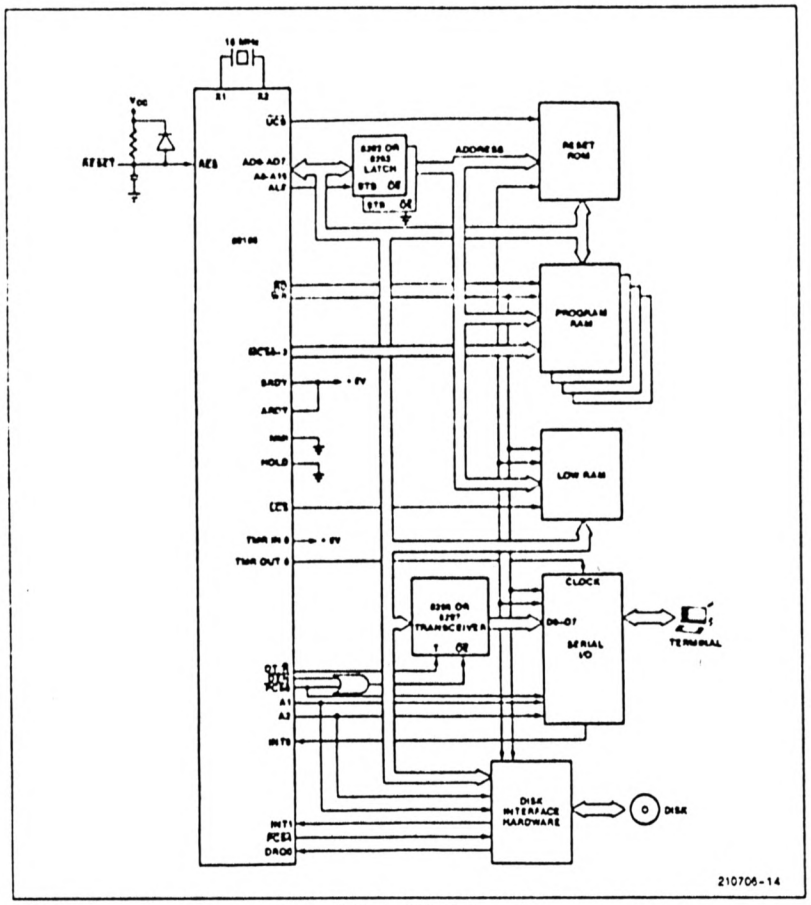


Figure 40. Typical 80188 Computer

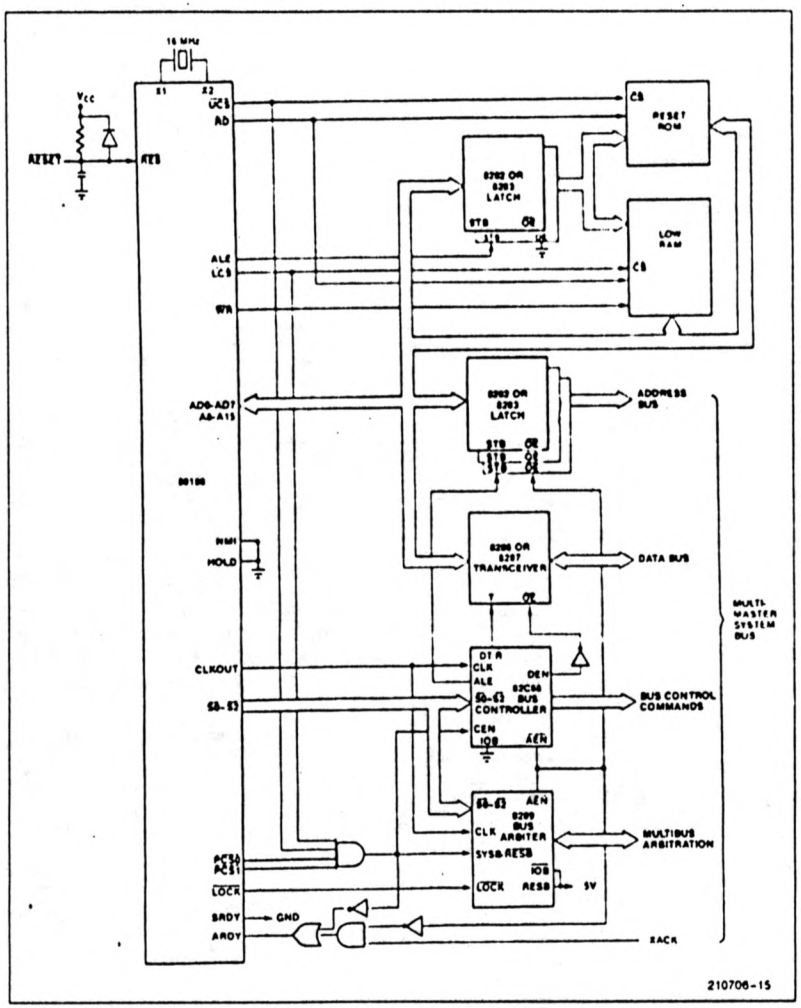


Figure 41. Typical 80188 Multi-Master Bus Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ....0°C to + 70°C
Storage Temperature .....−65°C to + 150°C
Voltage on any Pin with Respect to Ground.....−1.0V to + 7V
Power Dissipation .....3 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to + 70°C, V_{CC} = 5V ± 10%)

Applicable to 80188 (8 MHz)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage (All except X1 and RES)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (RES)	3.0	V_{CC} + 0.5	V	
V_{CLI}	X1 Input Low Voltage	−0.5	0.6	V	
V_{CHI}	X1 Input High Voltage	3.9	V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA for $\overline{S0}$-$\overline{S2}$ I_{OL} = 2.0 mA for all other outputs
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 µA
I_{CC}	Power Supply Current		600*	mA	T_A = −40°C
			550	mA	T_A = 0°C
			415	mA	T_A = +70°C
I_{LI}	Input Leakage Current		±10	µA	0V < V_{IN} < V_{CC}
I_{LO}	Output Leakage Current		±10	µA	0.45V < V_{OUT} < V_{CC}
V_{CLO}	Clock Output Low		0.6	V	I_{OL} = 4.0 mA
V_{CHO}	Clock Output High	4.0		V	I_{OH} = −200 µA
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		20	pF	

*For extended temperature parts only

PIN TIMINGS

A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

80188 Timing Requirements All Timings Measured At 1.5 Volts Unless Otherwise Noted

Symbol	Parameter	80188 (8 MHz) Min	80188 (8 MHz) Max	Units	Test Conditions
T_{DVCL}	Data in Setup (A/D)	20		ns	
T_{CLDX}	Data in Hold (A/D)	10		ns	
T_{ARYHCH}	Asynchronous Ready (ARDY) active setup time(1)	20		ns	
T_{ARYLCL}	ARDY inactive setup time	35		ns	
T_{CLARX}	ARDY hold time	15		ns	
T_{ARYCHL}	Asynchronous Ready inactive hold time	15		ns	
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(2)	20		ns	
T_{CLSRY}	SRDY Transition Hold Time(2)	15		ns	
T_{HVCL}	HOLD Setup(1)	25		ns	
T_{INVCH}	INTR, NMI, TEST, TMR IN, Setup(1)	25		ns	
T_{INVCL}	DRQ0, DRQ1, Setup(1)	25		ns	

80188 Master Interface Timing Responses

T_{CLAV}	Address Valid Delay	5	55	ns	C_L = 20–200 pF all outputs (except T_{CLTMV}) @ 8 MHz
T_{CLAX}	Address Hold	10		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	35	ns	
T_{CHCZ}	Command Lines Float Delay		45	ns	
T_{CHCV}	Command Lines Valid Delay (after float)		55	ns	
T_{LHLL}	ALE Width	T_{CLCL} – 35		ns	
T_{CHLH}	ALE Active Delay		35	ns	
T_{CHLL}	ALE Inactive Delay		35	ns	
T_{LLAX}	Address Hold to ALE Inactive	T_{CHCL} – 25		ns	
T_{CLDV}	Data Valid Delay	10	44	ns	
T_{CLDOX}	Data Hold Time	10		ns	
T_{WHDX}	Data Hold after WR	T_{CLCL} – 40		ns	
T_{CVCTV}	Control Active Delay 1	5	50	ns	
T_{CHCTV}	Control Active Delay 2	10	55	ns	
T_{CVCTX}	Control Inactive Delay	5	55	ns	
T_{CVDEX}	DEN Inactive Delay (Non-Write Cycle)	10	70	ns	

1. To guarantee recognition at next clock.
2. To guarantee proper operation.

PIN TIMINGS (Continued)

A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%) (Continued)

80188 Master Interface Timing Responses (Continued)

Symbol	Parameter	80188 (8 MHz) Min	80188 (8 MHz) Max	Units	Test Conditions
T_{AZRL}	Address Float to RD Active	0		ns	
T_{CLRL}	RD Active Delay	10	70	ns	
T_{CLRH}	RD Inactive Delay	10	55	ns	
T_{RHAV}	RD Inactive to Address Active	T_{CLCL} – 40		ns	
T_{CLHAV}	HLDA Valid Delay	5	50	ns	
T_{RLRH}	RD Width	$2T_{CLCL}$ – 50		ns	
T_{WLWH}	WR Width	$2T_{CLCL}$ – 40		ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} – 25		ns	
T_{CHSV}	Status Active Delay	10	55	ns	
T_{CLSH}	Status Inactive Delay	10	65	ns	
T_{CLTMV}	Timer Output Delay		60	ns	100 pF max
T_{CLRO}	Reset Delay		60	ns	
T_{CHQSV}	Queue Status Delay		35	ns	
T_{CHSX}	Status Hold Time	10		ns	
T_{AVCH}	Address Valid to Clock High	10		ns	
T_{CLLV}	LOCK Valid/Invalid Delay	5	65	ns	

80188 Chip-Select Timing Responses

T_{CLCSV}	Chip-Select Active Delay		60	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	35		ns	
T_{CHCSX}	Chip-Select Inactive Delay	5	35	ns	

80188 CLKIN Requirements

T_{CKIN}	CLKIN Period	62.5	250	ns	
T_{CKHL}	CLKIN Fall Time		10	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		10	ns	1.0 to 3.5V
T_{CLCK}	CLKIN Low Time	25		ns	1.5V
T_{CHCK}	CLKIN High Time	25		ns	1.5V

PIN TIMINGS (Continued)

A.C. CHARACTERISTICS (Continued)

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%) (Continued)

80188 CLKOUT Timing (200 pF load)

Symbol	Parameter	80188 (8 MHz)		Units	Test Conditions
		Min	Max		
T_{CICO}	CLKIN to CLKOUT Skew		50	ns	
T_{CLCL}	CLKOUT Period	125	500	ns	
T_{CLCH}	CLKOUT Low Time	$\frac{1}{2}T_{CLCL}-7.5$		ns	1.5V
T_{CHCL}	CLKOUT High Time	$\frac{1}{2}T_{CLCL}-7.5$		ns	1.5V
T_{CH1CH2}	CLKOUT Rise Time		15	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		15	ns	3.5 to 1.0V

Explanation of the AC Symbols

Each timing symbol has from 5 to 7 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

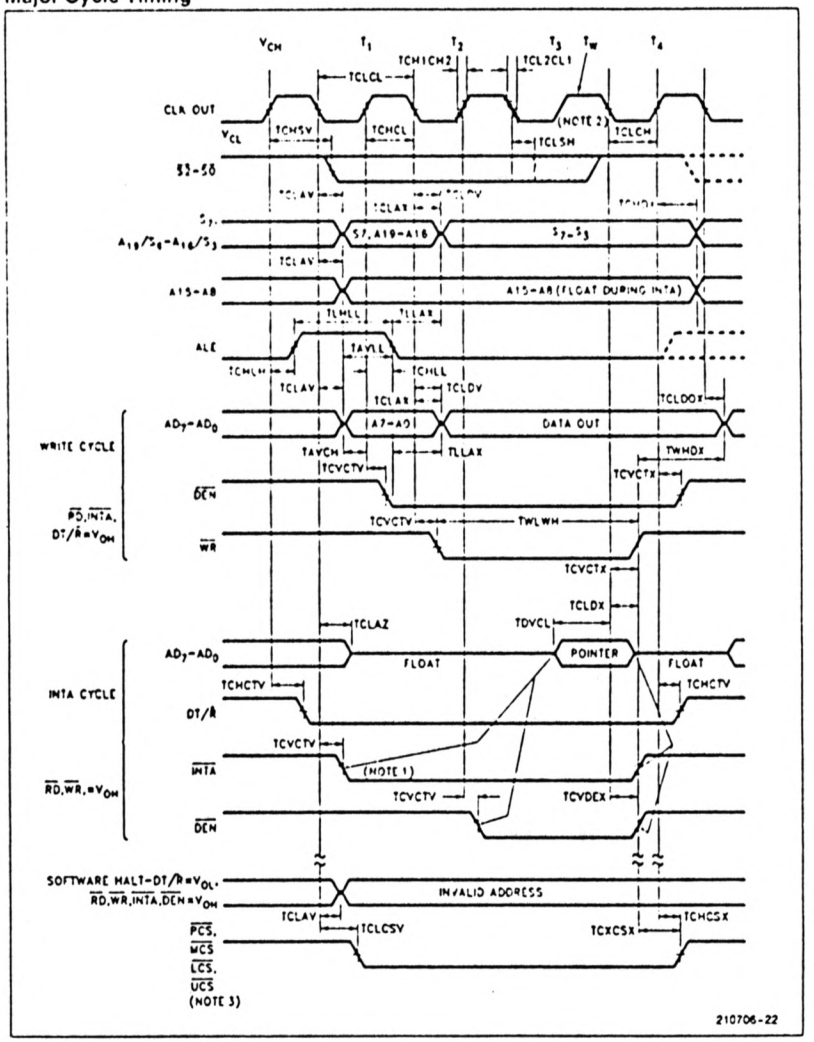
A: Address
ARY: Asynchronous Ready Input
C: Clock Output
CK: Clock Input
CS: Chip Select
CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)
D: Data Input
DE: $\overline{DEN}$
H: Logic Level High
IN: Input (DRQ0, TIM0, . . .)
L: Logic Level Low or ALE
O: Output
QS: Queue Status (QS1, QS2)
R: $\overline{RD}$ Signal, RESET Signal
S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)
SRY: Synchronous Ready Input
V: Valid
W: WR Signal
X: No Longer a Valid Logic Level
Z: Float

Examples:

T_{CLAV}— Time from Clock Low to Address Valid
T_{CHLH}— Time from Clock High to ALE High
T_{CLCSV}— Time from Clock LOW to Chp Select Valid

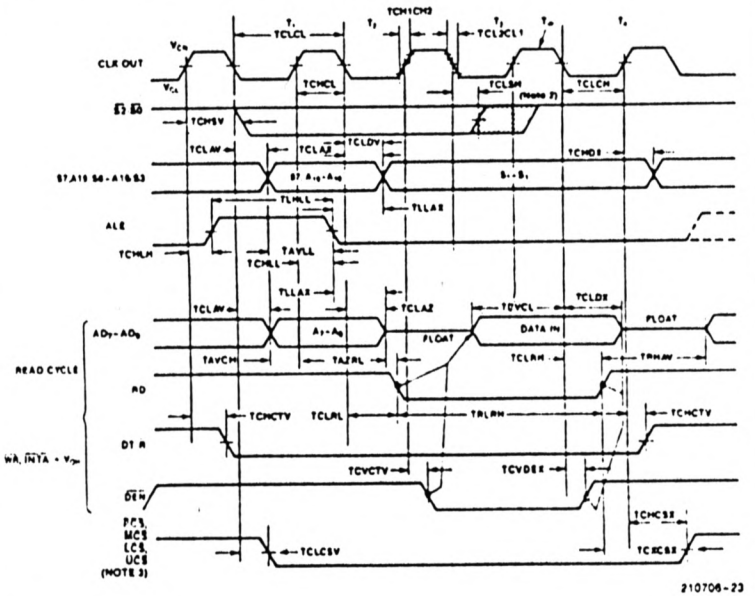
WAVEFORMS

Major Cycle Timing



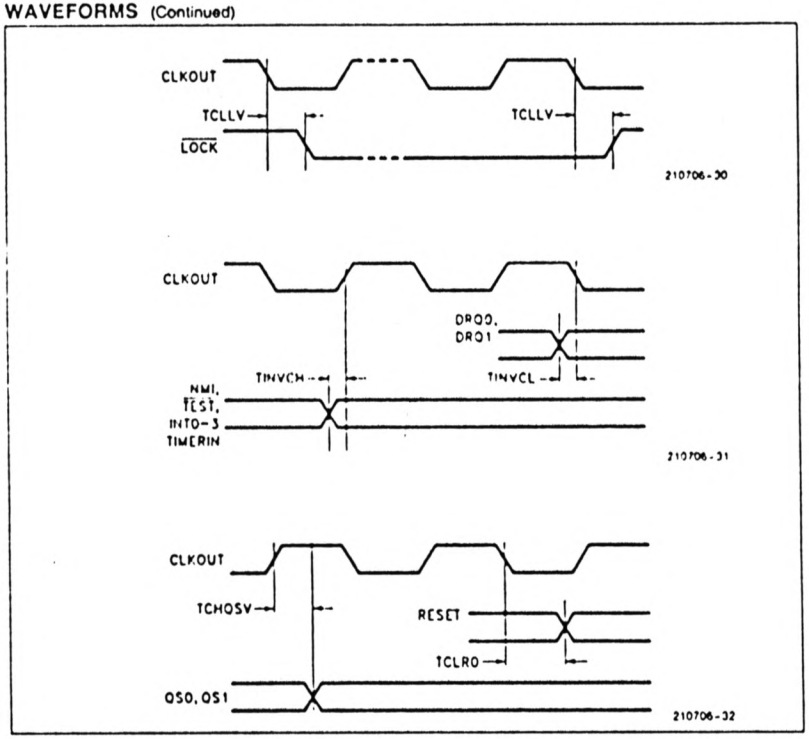
WAVEFORMS (Continued)

Major Cycle Timing (Continued)



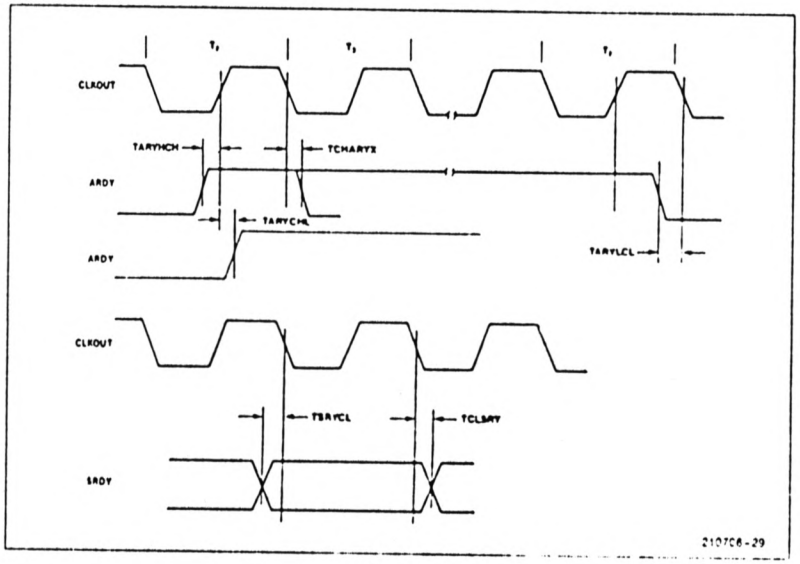
NOTES:
1. INTA occurs one clock later in Slave Mode.
2. Status inactive just prior to T_4.
3. Latched A1 and A2 have same timings as $\overline{PCS5}$ and $\overline{PCS6}$.

WAVEFORMS (Continued)

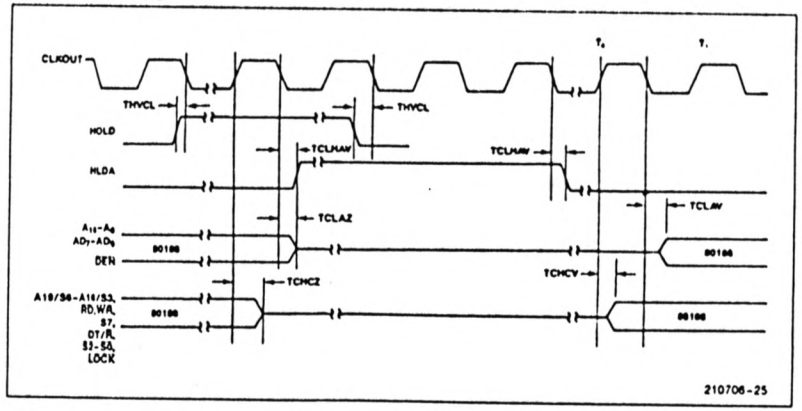


WAVEFORMS (Continued)

READY TIMING

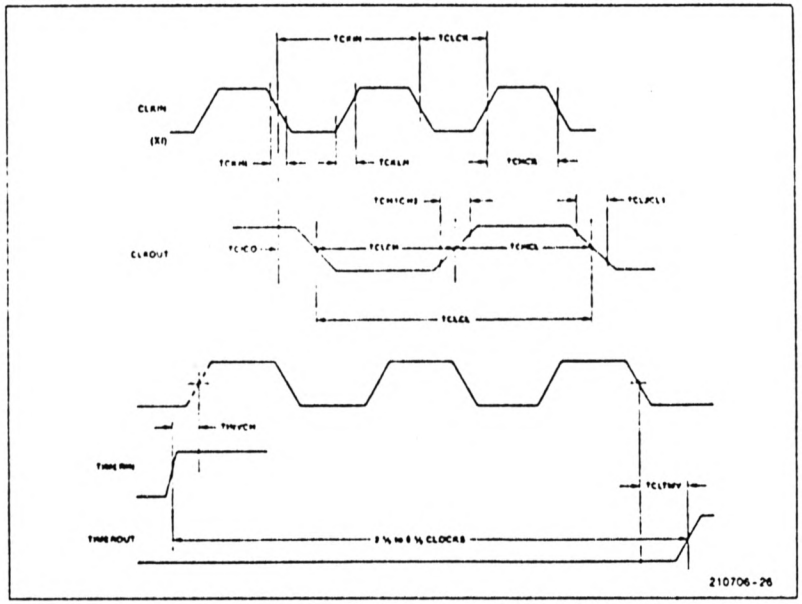


HOLD-HLDA TIMING



WAVEFORMS (Continued)

Timer On 80188



80188 EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the 80188 microprocessor. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic, for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one or two-letter prefix to the part number. The prefixes are listed in Table 16. All AC and DC specifications not mentioned in this section are the same for both commercial and EXPRESS parts.

Table 16. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
A	PGA	Commercial	No
N	PLCC	Commercial	No
R	LCC	Commercial	No
TA	PGA	Extended	No
OR	LCC	Commercial	Yes

NOTE:
Not all package/temperature range combinations are available.

80188 EXECUTION TIMINGS

Since the bus interface unit and execution unit operate independently, a determination of 80188 program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.

All instructions which involve memory accesses can also require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the BIU and execution unit.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

The 80188 8-bit BIU is noticeably limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue much of the time. Therefore, actual program execution time may be substantially greater than that derived from adding the instruction timings shown.

National Semiconductor Corporation

LM139/239/339, LM139A/239A/339A, LM2901, LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Wide single supply voltage range or dual supplies
  - LM139 series: 2 V_{DC} to 36 V_{DC} or
  - LM139A series, LM2901: ±1 V_{DC} to ±18 V_{DC}
  - LM3302: 2 V_{DC} to 28 V_{DC} or ±1 V_{DC} to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage (2 mW/comparator at +5 V_{DC})
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- and offset voltage: ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams

TL/H/5706-1

Dual-In-Line Package

TL/H/5706-2

Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
See NS Package Number J14A
Order Number LM339AM, LM339M or LM2901M
See NS Package Number M14A
Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 10)

	LM139/LM239/LM339	LM139A/LM239A/LM339A	LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	36 V_{DC} or ±18 V_{DC}	26 V_{DC} or ±13 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}	36 V_{DC}	26 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +26 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Power Dissipation (Note 1)				
Molded DIP	1050 mW	1050 mW	1050 mW	1050 mW
Cavity DIP	1190 mW	1190 mW	1190 mW	1190 mW
Small Outline Package	760 mW	760 mW	760 mW	760 mW
Output Short Circuit to GND (Note 2)	Continuous	Continuous	Continuous	Continuous
Input Current (V_{IN} < −0.3 V_{DC}) (Note 3)	50 mA	50 mA	50 mA	50 mA
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C	260°C	260°C
Operating Temperature Range				
LM339/LM339A	0°C to +70°C			
LM239/LM239A	−25°C to +85°C			
LM2901	−40°C to +85°C			
LM139/LM139A	−55°C to +125°C			
Soldering Information				
Dual-In-Line Package				
Soldering (10 seconds)	260°C			
Small Outline Package				
Vapor Phase (60 seconds)	215°C			
Infrared (15 seconds)	220°C			

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics (V^+ = 5 V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM139A		LM239A, LM339A		LM139		LM239, LM339		LM2901		LM3302		Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0	±3	±20	mV$_{DC}$
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, (Note 5), V_{CM} = 0V		25	100		25	250		25	100		25	250		25	500	nA$_{DC}$
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$, V_{CM} = 0V		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5	±50		±3	±100	nA$_{DC}$
Input Common-Mode Voltage Range	V^+ = 30 V_{DC} (LM3302, V^+ = 28 V_{DC}) (Note 6)	0		V^+ − 1.5	0		V^+ − 1.5	0		V^+ − 1.5	0		V^+ − 1.5	0		V^+ − 1.5	V_{DC}
Supply Current	R_L = ∞ on all Comparators, R_L = ∞, V^+ = 36V, (LM3302, V^+ = 28 V_{DC})		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0	mA$_{DC}$
			1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5	mA$_{DC}$
Voltage Gain	R_L ≥ 15 kΩ, V^+ = 15 V_{DC}, V_O = 1 V_{DC} to 11 V_{DC}	50	200		50	200		50	200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC}, V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ,		300			300			300			300			300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, (Note 7)		1.3			1.3			1.3			1.3			1.3		µs
Output Sink Current	$V_{IN}(-)$ = 1 V_{DC}, $V_{IN}(+)$ = 0, V_O = 1.5 V_{DC}	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA$_{DC}$

Electrical Characteristics ($V^+ = 5\ V_{DC}$, $T_A = 25°C$, unless otherwise stated) (Continued)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$		250	400		250	400		250	400		250	400		250	400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics ($V^+ = 5.0\ V_{DC}$, Note 4)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			± 4.0			± 4.0			± 9.0			± 9.0		± 9	± 15			± 40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			± 100			± 150			± 100			± 150		± 50	± 200			± 300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$ (LM3302, $V^+ = 28\ V_{DC}$) (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$			$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$, (LM3302, $V_O = 28\ V_{DC}$)			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			36			36			36			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100\ mW$), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: The input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to the diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to $+30\ V_{DC}$ without damage (25V for LM3302) independent of the magnitude of V^+.

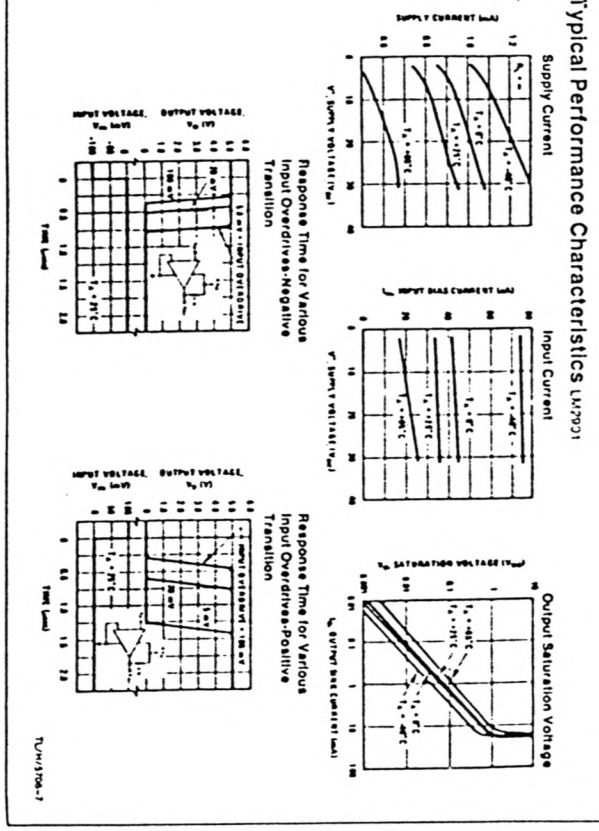
Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, $V_O = 1.4\ V_{DC}$, R_S = 0Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$) at 25°C. For LM3302, V^+ from 5 V_{DC} to 28 V_{DC}.

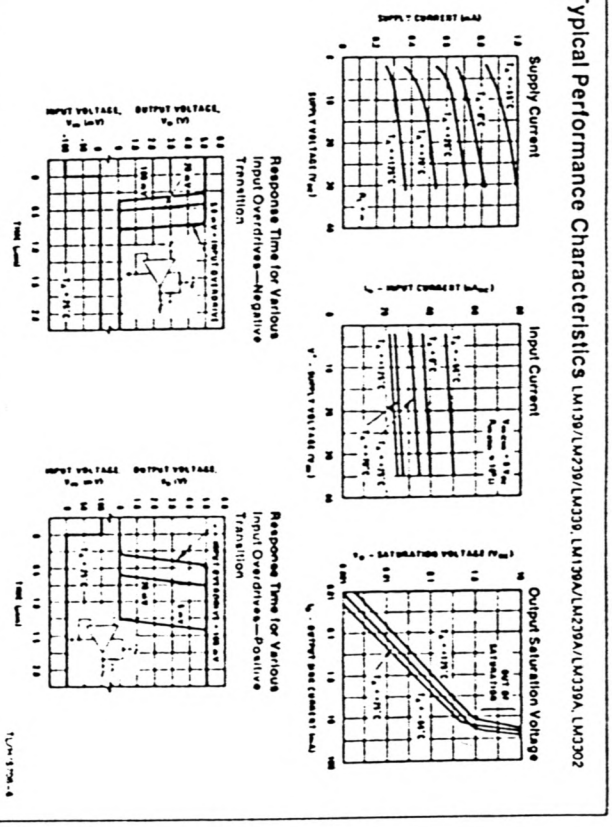
Note 10: Refer to RETS139AX for LM139AJ military specifications and to RETS139X for LM139J military specifications.

Typical Performance Characteristics LM2901



TL/H/5708-7

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302



TL/H/5708-8

Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output load is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

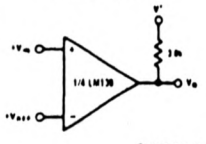
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

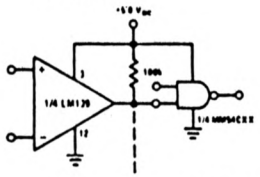
The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60 Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications (V^+ = 5.0 V_{DC})

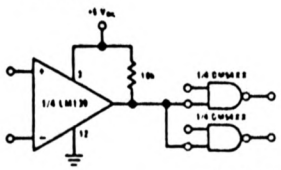
Basic Comparator



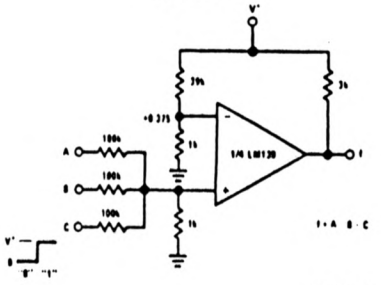
Driving CMOS



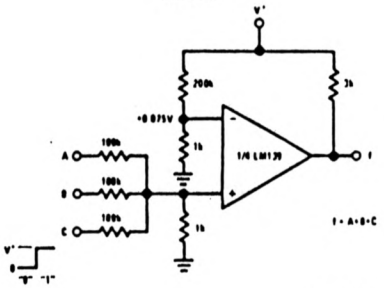
Driving TTL



AND Gate

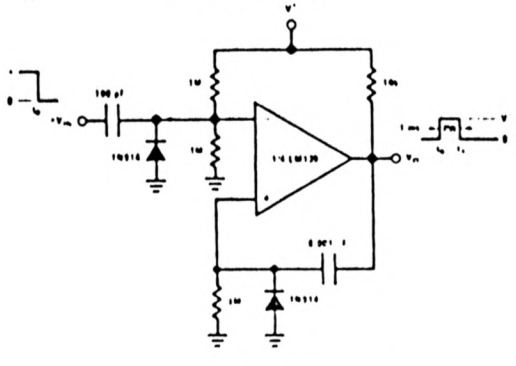


OR Gate

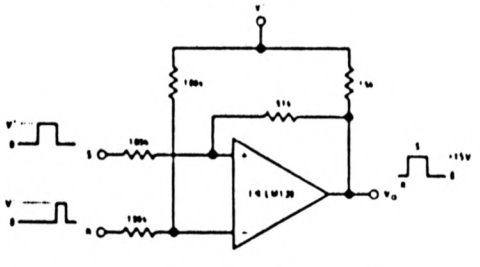


Typical Applications (V^+ = 15 V_{DC}) (Continued)

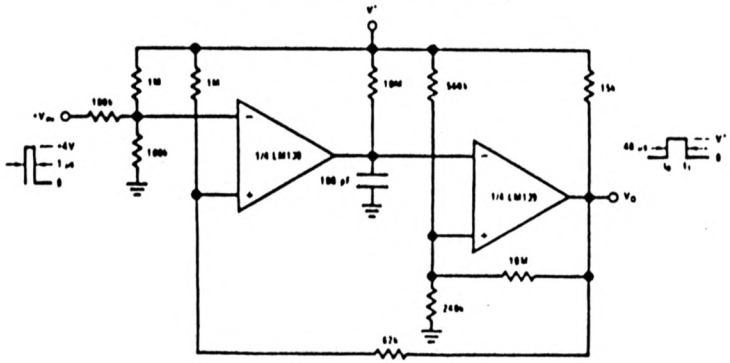
One-Shot Multivibrator



Bi-Stable Multivibrator

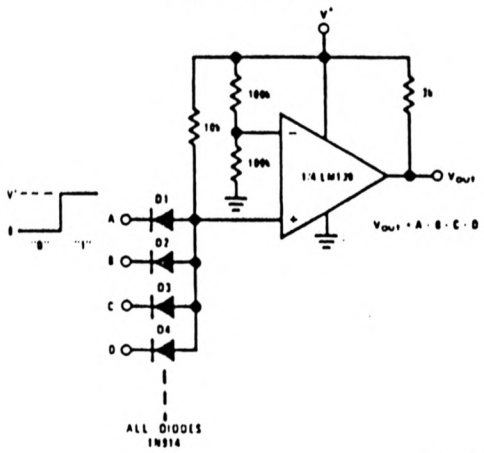


One-Shot Multivibrator with Input Lock Out

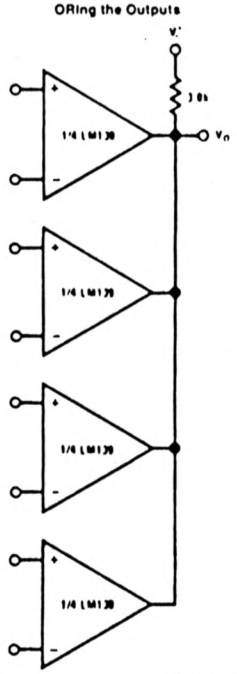


Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

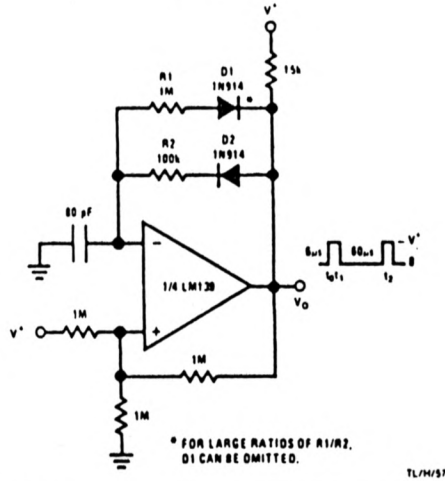
Large Fan-In AND Gate



ORing the Outputs

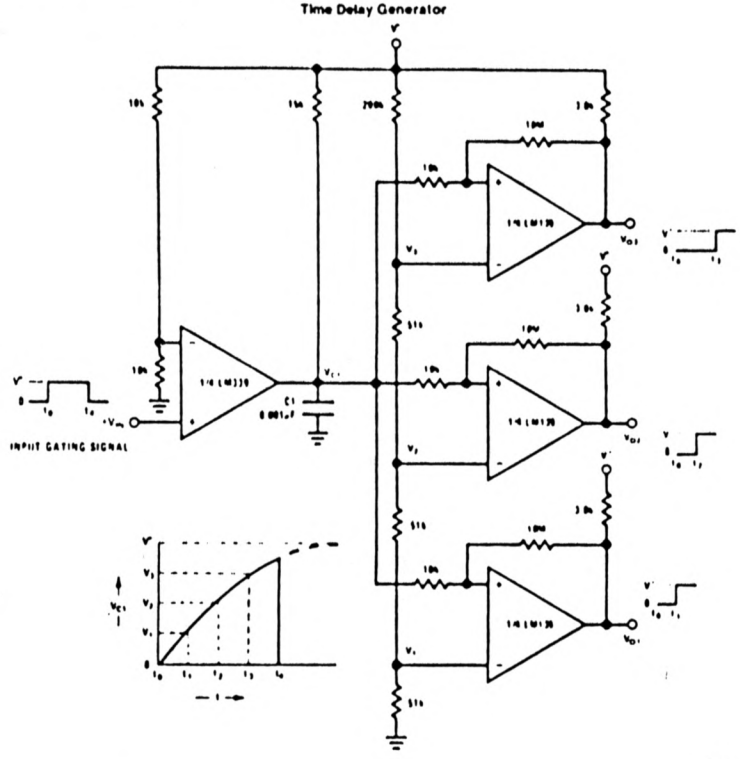


Pulse Generator

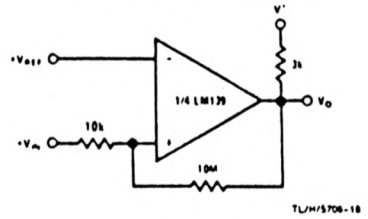


Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

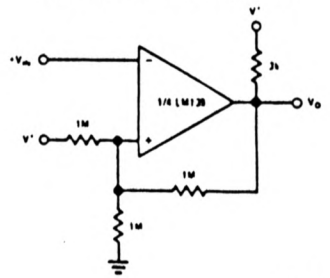
Time Delay Generator



Non-Inverting Comparator with Hysteresis



Inverting Comparator with Hysteresis



Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Squarewave Oscillator

Comparing Input Voltages of Opposite Polarity

Basic Comparator

Output Strobing

Limit Comparator

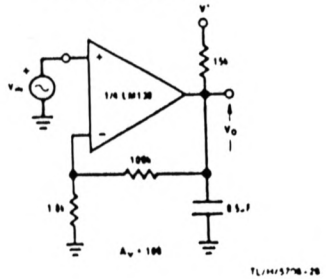
Crystal Controlled Oscillator

Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Two-Decade High-frequency VCO

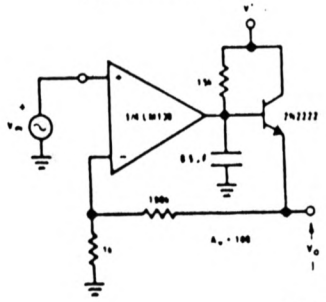
Typical Applications ($V^+ = 5\ V_{DC}$) (Continued)

Low Frequency Op Amp



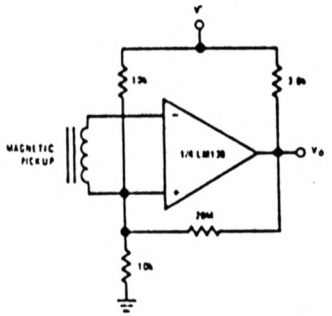
TL/H/5706-26

Low Frequency Op Amp
(V_o = 0V for V_{IN} = 0V)



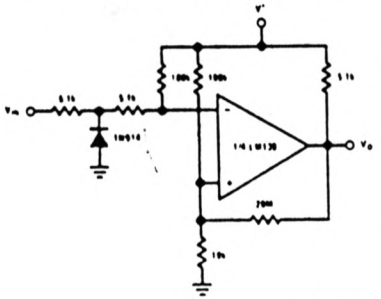
TL/H/5706-27

Transducer Amplifier



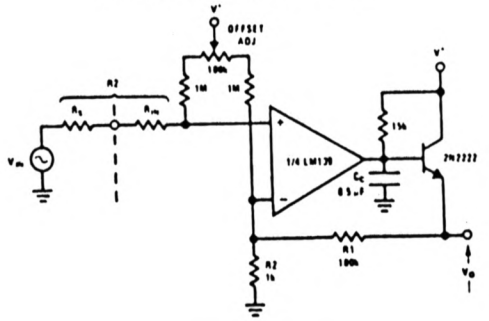
TL/H/5706-28

Zero Crossing Detector (Single Power Supply)



TL/H/5706-29

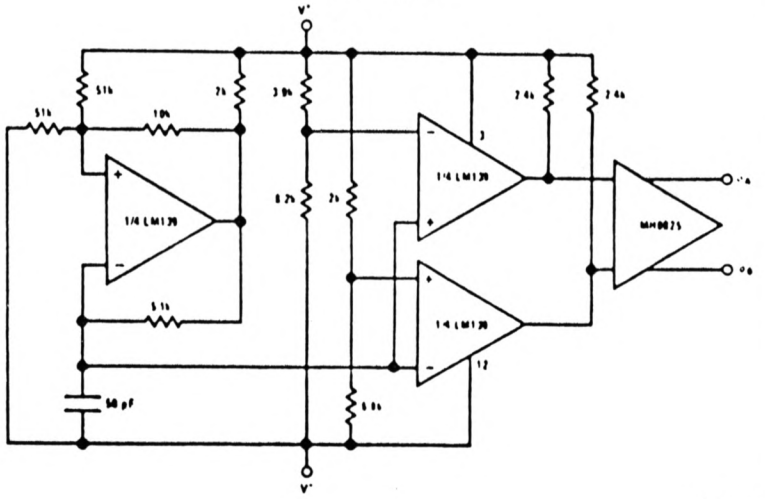
Low Frequency Op Amp with Offset Adjust



TL/H/5706-29

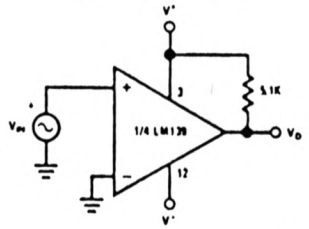
Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

MOS Clock Driver



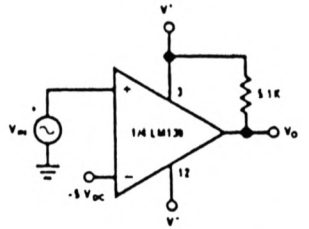
TL/H/5706-31

Zero Crossing Detector

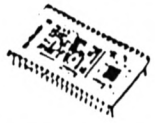


TL/H/5706-32

Comparator With a Negative Reference



TL/H/5706-33



10, 12, 14, OR 16 BIT INDUSTRIAL RESOLVER TO DIGITAL CONVERTERS

DESCRIPTION

The RDC-19200 Monobrid Series are versatile state-of-the-art resolver to digital converters featuring programmable resolution and bandwidth and a velocity output voltage.

Resolution programming allows selection of 10, 12, 14, or 16 bits and are available with commensurate accuracies up to 2 minutes + 1 LSB. Resolution programming combines the high tracking rate of a 10 bit converter with the precision of a 16 bit device in one package.

The velocity output (VEL) from the RDC-19200 is a ground based voltage of 0 to ±10VDC with a linearity of 2.0% or 0.7%. VEL may be scaled up by a single external resistor to provide up to ±10VDC for the required maximum tracking rate.

APPLICATIONS

The RDC-19200 Series converters are designed for use in modern high performance commercial and industrial control systems. Applications include motor control, theodolite, radar antenna position information, CNC machine tooling, robot axis control, and process control. With their low cost and superior performance, the RDC-19200 Series converters are ideal for motion control and position monitoring applications.

FEATURES

- *LOW COST*
- *IDEAL FOR MOTOR CONTROL*
- *BUILT-IN-TEST (BIT) AND LOSS-OF-SIGNAL (LOS) OUTPUTS*
- *VELOCITY OUTPUT ELIMINATES TACHOMETER*
- *PROGRAMMABLE RESOLUTION*
- *PROGRAMMABLE BANDWIDTH*
- *ACCURACY TO ±2.3 ARC MIN.*

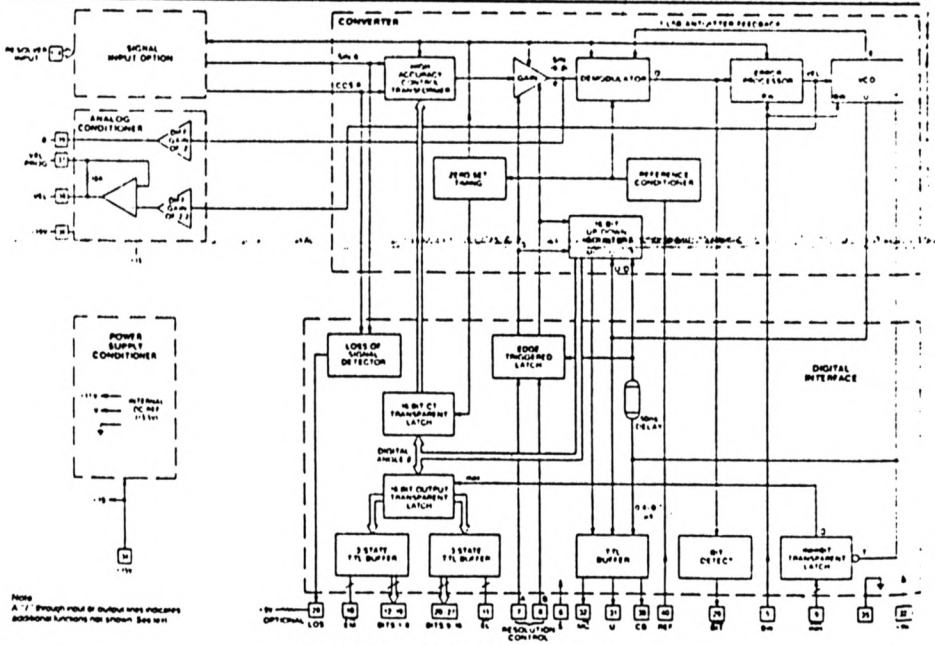


FIGURE 1. RDC-19200 BLOCK DIAGRAM

DDC ILC DATA DEVICE CORPORATION

RDC-19200* MONOBRID* SERIES

TABLE 1. RDC-19200 SPECIFICATIONS

These specifications apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE	DESCRIPTION
RESOLUTION	10, 12, 14, or 16 bits	Programmable
ACCURACY GRADES	10, 8, 4, 3, 2 minutes	Max ± 1 LSB of selected resolution, see Ordering Information
DIFFERENTIAL LINEARITY	16, 12, 8, or 4	LSBs in the 16th bit, see Ordering Information
REPEATABILITY	1 LSB max	
REF INPUT CHARACTERISTICS		
Voltage Range	4-50Vrms	
Single Ended Input Impedance	100K Ohm min, 110K Ohm nom	
Frequency Range	360Hz to 6KHz	See Table 4, Dynamic Characteristics
SIGNAL INPUT CHARACTERISTICS		Voltage options and minimum input impedance, balanced
Resolver	11.8VL-L	
Z_{in} Single Ended	70K Ohm	
Z_{in} Differential	140K Ohm	
Z_{in} Each line-ground	80K Ohm	
Common Mode Range	26V peak	
Max Voltage w/o damage	100V transient	
Direct	2.0VL-L	
Input Signal Type		Sin and Cos resolver signal referenced to converter's internal DC ref voltage of +5.5V
Sin Cos Voltage Range	2V nom, 2.3V max	
Max Voltage w/o Damage	15V continuous 110V peak transient	
Z_{in}	>20M ohm, <10pf voltage follower	
DIGITAL INPUT OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs	Logic 0 = 0.8V max Logic 1 = 2.0V min	
Max Voltage w/o Damage	-0.3 to 11V	
Loading	-10 µA max	Pull-up current source to +5V. 5pf max. CMOS transient protected
$\overline{INH}$ (Inhibit)		Logic 0 inhibits. Logic 1 enables. Data stable within 0.3 µs
$\overline{EM}$ (Enable bits 1-8)		Logic 0 enables, data valid within 150 ns. Logic 1 high Z within 100 ns
$\overline{EL}$ (Enable bits 9-16)		
$\overline{S}$ (Control Transformer)		Logic 0 for Control Transformer, Logic 1 for normal tracking
BW (Bandwidth)		Logic 1 = High BW (530 Hz), Logic 0 = Low BW (130 Hz)
Resolution Control		B (pin 8) / A (pin 7): 0/0, 0/1, 1/0, 1/1
10 Bit		
12 Bit		
14 Bit		
16 Bit		
		Unused output bits are at logic 0
OUTPUTS		
Parallel Data	10, 12, 14, or 16 bits	Natural binary angle, positive logic
CB (Converter Busy)		0.4 µs to 0.7 µs positive pulse; leading edge initiates counter update.
U (Direction)		Logic 1 counts up, Logic 0 counts down
$\overline{MC}$ (Major Carry)		Logic 0 at $\overline{MC}$
$\overline{BIT}$ (Built in Test)		Logic 0 for $\overline{BIT}$ condition.
LOS (Loss of Signal)		Logic 1 for LOS (1-3µA pull-up to +5V)
Drive Capability	Logic 0: 1 TTL Load Logic 1: 10 TTL Loads High Z: 10µA, 5pf max	-1.6mA at 0.4V max 0.4mA at 2.8V min
ANALOG OUTPUTS		
V (Internal DC ref)	+5.5V nom	
VEL (Velocity)		See Table 6, Velocity Characteristics
e (AC error)	50mVrms per LSB of error 25mVrms per LSB of error 12.5mVrms per LSB of error 6.3mVrms per LSB of error	10 bit mode 12 bit mode 14 bit mode 16 bit mode
Dynamic Characteristics		See Table 4, Dynamic Characteristics

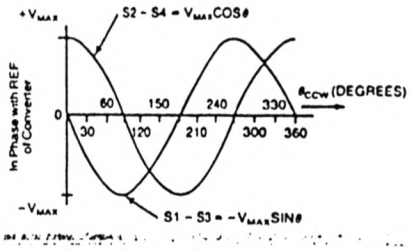
TABLE 1. RDC-19200 SPECIFICATIONS (Continued)

PARAMETER	VALUE			DESCRIPTION
POWER SUPPLY CHARACTERISTICS Nominal Voltage and Range	+15VDC ±5%	+5VDC ±10%	-15VDC ±5%	Note: When analog outputs are not required, ground -15V (pin 36)
Max Voltage w/o Damage Max Current	+18V 25mA	+8V 10mA	-18V 15mA	
TEMPERATURE RANGES Operating Storage	0°C to +70°C -40°C to +120°C			
PHYSICAL CHARACTERISTICS Size Weight	1.14 x 2.02 x 0.23 inches (28.96 x 51.3 x 5.84 mm) 0.46 oz (13 gm)			40 pin TDIP

TECHNICAL INFORMATION

INTRODUCTION

The RDC-19200 Series are small, 40 pin TDIP resolver to digital hybrid converters. As shown in the block diagram (figure 1), the RDC-19200 can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. RESOLVER SIGNALS

SIGNAL INPUT OPTIONS

In a resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The converter internal to the RDC-19200 operates with signals in resolver format, $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Figure 2 shows the resolver signals as a function of the angle θ. The RDC-19200 accepts solid state resolver (11.8Vrms) and direct (2Vrms) inputs. The reference is a single ended input with 100K ohm impedance.

2V DIRECT INPUT OPTION. The direct inputs are transient protected voltage followers which accept 2Vrms resolver inputs, as shown in figure 3. A 2V input from a resolver allows use of a lower reference voltage. This lowers oscillator cost and allows a lower power reference oscillator.

INTERNAL DC REFERENCE VOLTAGE (V). This internal voltage is not required externally for normal operation of the converter. It is used as the internal DC reference common with the direct input option. It is nominally +5.5V and is proportional to the +15VDC supply.

11.8V RESOLVER INPUT OPTION. The 11.8V resolver inputs are true differential inputs with high AC and DC common mode rejection (see figure 4). Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed 26V peak; maximum transient peak voltage should not exceed 100V.

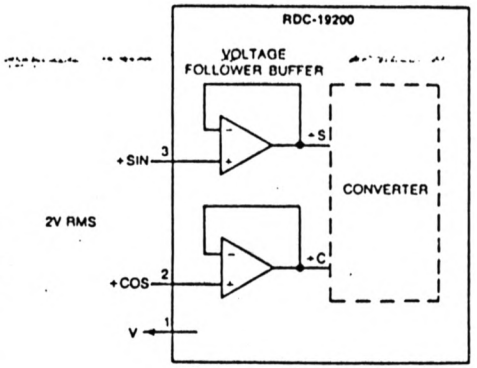


FIGURE 3. DIRECT INPUT OPTION - 2V

RESISTOR PROGRAMMING FOR NON-STANDARD INPUT VOLTAGES. When applying voltages greater than 2Vrms, a simple voltage divider can be used to attenuate both the sin and cos inputs. Since the converter inputs are voltage followers, there will be no loading on the resistor dividers (see figure 5).

The 11.8V resolver input conditioner consists of two differential amplifiers. The 11.8V input is scaled down to 2V. When applying resolver inputs greater than 11.8V, four resistors, one in series with each input line, can be used to scale down the voltage (see figure 6).

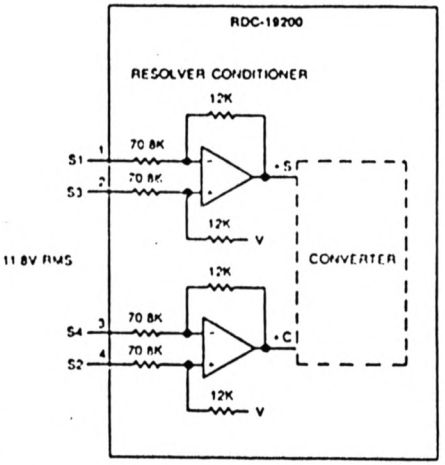
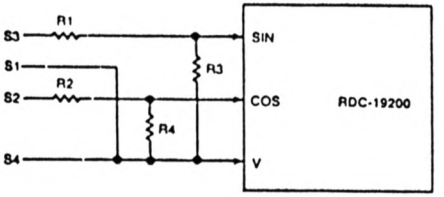


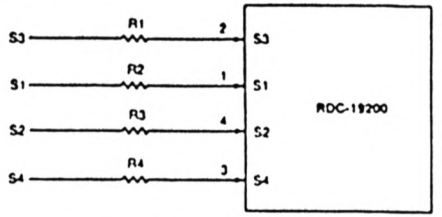
FIGURE 4. RESOLVER INPUT OPTION - 11.8V



$$\frac{\text{Input Voltage L-L}}{2V} = \frac{R1 + R3}{R3}$$

Notes:
(1) R1 = R2; R3 = R4 to 0.1% match.
(2) R1 + R3 and R2 + R4 should be as high as possible to minimize resolver loading.

FIGURE 5. INPUT RESISTOR SCALING - 2V



$$\frac{R + 70.8K}{70.8K} = \frac{\text{Input Voltage L-L}}{11.8V}$$

Notes
(1) Input Voltage L-L is greater than 11.8V
(2) R = R1 = R2 = R3 = R4 to 0.1% match

FIGURE 6. INPUT RESISTOR SCALING - 11.8V

CONVERTER OPERATION

As shown in figure 1, the converter section of the RDC-19200 contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO), up-down counter, zero-set timing, and reference conditioner. The converter produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the converter.

The control transformer performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

Where:

θ is angle theta, representing the resolver shaft position.
ϕ is digital angle phi, contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \to 0$, so that ϕ will repeat the shaft position θ.

The output of the demodulator is an analog DC level proportional to $\sin(\theta - \phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

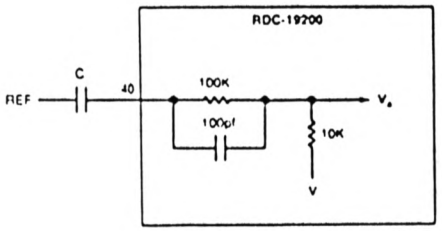
The RDC-19200 has unique **zero-set** timing circuits that cancel out all internal op-amp DC offsets. This zero-setting is done twice a reference input carrier cycle centered around the zero crossings. Each zero-setting cycle lasts for 18μs. During this time, the resolver input is disconnected and a zero input is switched in. The digital input to the control transformer is latched. The resultant DC error at the output of the demodulator is sampled and injected back in during the normal mode of operation.

The result is an effective way of simulating DC offset-free op-amps which ensure a converter whose actual dynamic and large signal performance is the same as its mathematical theoretical

performance. In a somewhat similar manner, the velocity op-amp integrator's DC offset voltage is also cancelled out with this zero-setting scheme.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. It is single ended ground based with an input Z of 100K ohms min, 110K ohms nom, resistive

MINIMIZING ERRORS DUE TO QUADRATURE. In those applications where highest accuracy is needed, the REF input can be phase shifted by adding a capacitor in series with the REF input (pin 40) to add a phase lead equal to the nominal phase lead of the resolver input. To determine the capacitor's value see figure 7.



Note
Choose C such that the V_a to REF phase lead is equal to the resolver to REF phase lead plus 9 μs

FIGURE 7. PHASE SHIFTING THE REF INPUT

QUADRATURE VOLTAGES. In a resolver, quadrature voltages are by definition the resulting 90° fundamental signal in the nulled out error voltage (ε) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error = (Quadrature Voltage/F.S. signal) • tan(α)

Where:

Magnitude of Error is in radians
Quadrature Voltage is in volts.
Full Scale signal is in volts.
α = signal to REF phase shift.

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8mV
Let: F.S. signal = 11.8V
Let: α = 6°
Then: Magnitude of Error = 0.35 min ≈ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage = (rotational speed/carrier freq) • F.S. signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the resolver.
Carrier frequency is the REF in Hz.

ANALOG CONDITIONER

The Analog Conditioner section performs three functions. It converts analog ground from 5.5V to 0V, provides a gain of 2 for AC Error (ε) and a gain of 2.2 for Velocity (VEL). The velocity scaling sensitivity can be increased with an external resistor. Refer to VEL PROGRAMMING section for more information.

POWER SUPPLY CONDITIONER

The power supply conditioner lowers the internal power supply voltage to the custom CMOS chip to +11V from the +15V supply. The +11V will track the +15V. Internal analog ground is one half of 11V or +5.5V, nom.

DIGITAL INTERFACE

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command, allowing stable data to be read out of the RDC-19200.
2. Furnishes parallel tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the RDC-19200, applying an Inhibit ($\overline{INH}$) command will lock the data in the output transparent latch without interfering with the continuous tracking of the converter's feedback loop. Therefore, the digital angle ϕ is always updated, and the $\overline{INH}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50ns delay are part of the inhibit circuitry. For further information, see the INHIBIT ($\overline{INH}$, PIN 9) paragraph.

The BIT detect circuitry monitors the error level (D) from the demodulator and the LOS (loss of signal) detector detects disconnected resolver inputs.

LOGIC INPUT/OUTPUT

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 10) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{EL}$ (pin 11) to a logic 0. The second byte will contain either bits 9-10 (10 bit resolution), bits 9-12 (12 bit resolution), bits 9-14 (14 bit resolution) or bits 9-16 (16 bit resolution). All unused LSBs will be at logic 0. Table 2 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{EM}$ or $\overline{EL}$ are activated with a logic 0 and are high impedance within 100 ns, max after $\overline{EL}$ and $\overline{EM}$ are set to logic 1. Both enables are internally pulled up to +5V by −10μA max current sources.

TABLE 2. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1 (MSB ALL MODES)	180	10 800
2	90	5 400
3	45	2,700
4	22 5	1.350
5	11 25	675
6	5 625	387 5
7	2 813	168 5
8	1 405	84 38
9	0 7031	42 19
10 (LSB 10 BIT MODE)	0 3516	21 09
11	0 1758	10 55
12 (LSB 12 BIT MODE)	0 879	5 27
13	0 439	2 64
14 (LSB 14 BIT MODE)	0 0220	1 32
15	0 0110	0 66
16 (LSB 16 BIT MODE)	0 0055	0 33

Note $\overline{EM}$ enables the 8 MSBs and $\overline{EL}$ enables the LSBs

DIGITAL ANGLE OUTPUT TIMING

The digital angle output is 10, 12, 14, or 16 parallel data bits. All logic outputs are short-circuit proof to ground and +5V. The CB output is a positive 0.4 to 0.7 μs pulse.

The digital output data changes approximately 50 ns after the leading edge of the CB pulse because of an internal delay (shown in figure 1). Data is valid 0.2 μs after the leading edge of CB (see figure 8). The angle is determined by the sum of the bits at logic 1.

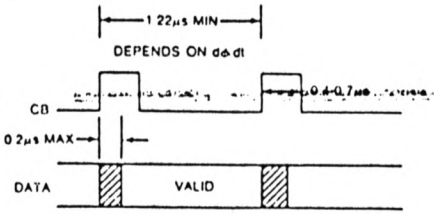


FIGURE 8. CB TIMING

INHIBIT ($\overline{INH}$, PIN 9)

When an Inhibit ($\overline{INH}$) input is applied to the RDC-19200, the Output Transparent Latch is locked, causing the output data bits to remain stable while data is being transferred (see figure 9). The output data bits are stable 0.3 μs after INH is driven to logic 0.

A logic 0 at the T input of the Inhibit Transparent Latch latches the data, and a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and INH. While the counter is not being updated, CB is at logic 0 and the INH latch is transparent; when CB goes to logic 1, the INH latch is locked. If CB occurs after INH has been applied, the latch will remain locked and its data will not change until CB returns to logic 0, if INH is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and INH where the up-down counter begins to change as an INH is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is:

(1) Apply $\overline{INH}$.
(2) Wait 0.3 μs, min.
(3) Transfer the data.
(4) Release $\overline{INH}$.

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 10 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

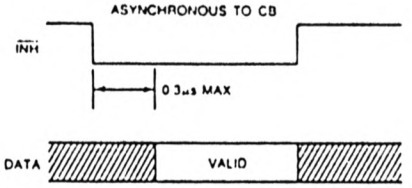


FIGURE 9. INHIBIT TIMING

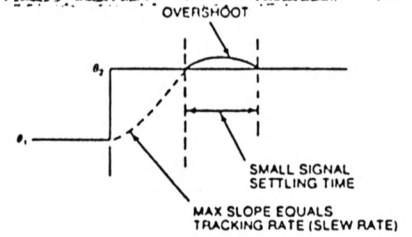


FIGURE 10. RESPONSE TO A STEP INPUT

DATA TRANSFERS

Digital output data from the RDC-19200 can be transferred to 8 bit and 16 bit bus systems. For 8 bit systems, the MSB and LSB bytes are transferred sequentially (see figures 11 and 12). For 16 bit systems, all bits are transferred at the same time (see figures 13 and 14).

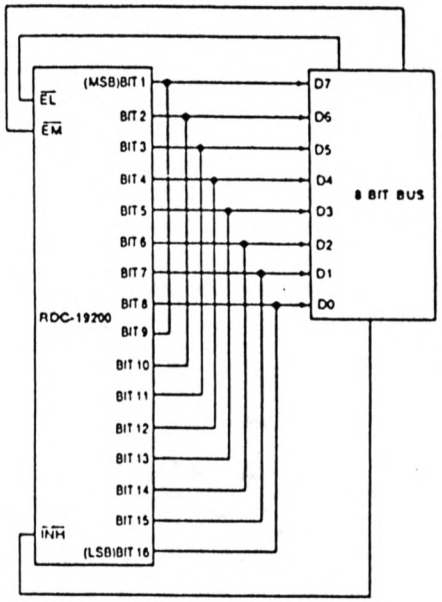


FIGURE 11. DATA TRANSFER TO 8 BIT BUS

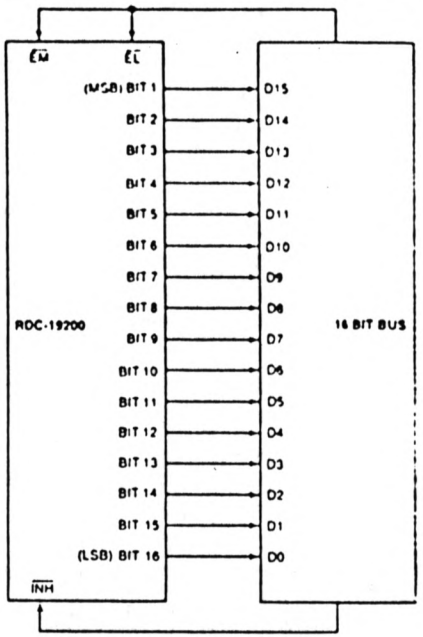


FIGURE 13. 16 BIT DATA TRANSFER

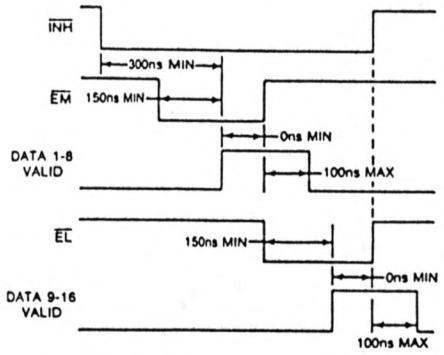


FIGURE 12. DATA TRANSFER TO 8 BIT BUS TIMING

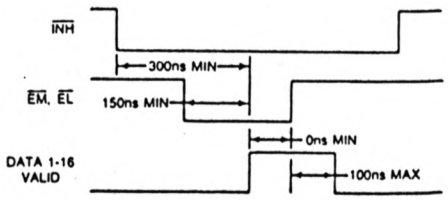


FIGURE 14. 16 BIT DATA TRANSFER TIMING

PROGRAMMABLE RESOLUTION

Resolution is controlled by two logic inputs, A and B (see table 3). The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, inputs A and B are transferred through the latch internally on the trailing edge of CB (see figure 15).

TABLE 3. RESOLUTION CONTROL

B (pin 7)	A (pin 8)	RESOLUTION
0	0	10 BIT
0	1	12 BIT
1	0	14 BIT
1	1	16 BIT

Note: All unused digital output data bits are at logic 0

FASTER SETTLING TIME USING BIT TO REDUCE RESOLUTION

Since the RDC-19200 has higher precision in the higher resolution mode and faster settling in the lower resolution modes, the $\overline{BIT}$ output can be used to program the RDC-19200 for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

When the resolution is changed, the VEL scaling is also changed. Since the VEL output is from an integrator with a capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth (see figure 22).

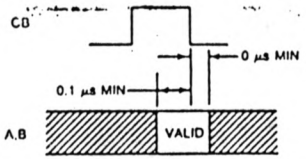


FIGURE 15. RESOLUTION CONTROL TIMING

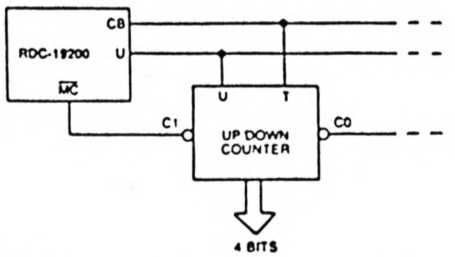
MAJOR CARRY ($\overline{MC}$, PIN 32)

Major Carry is used with Direction Output (U) for multi-turn applications. This signal is similar to the popular MSI four bit up-down counter CO (Carry Out), that is, it is normally high and goes low for all 1's when counting up or all 0's when counting down. See figure 16 for a typical interconnection.

DIRECTION OUTPUT (U, PIN 31)

Direction Output (U) is shown in figure 17. It is at logic 1 to count up and logic 0 for down. The logic level at (U) is valid at least 0.5µs before and at least 20ns after the leading edge of CB.

TURNS COUNTING



Notes:
(1) For the 4 bit up/down counter, use 74LS169B(TTL) or 4516 (CMOS).
(2) U = up down line, logic 1 counts up
(3) T = toggle line, counts on positive edge.

FIGURE 16. TURNS COUNTING CONNECTION DIAGRAM

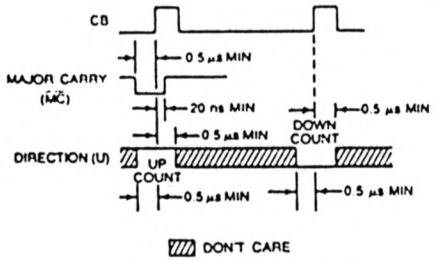


FIGURE 17. DIRECTION OUTPUT (U) TIMING

SYSTEM SELF-TEST

The RDC-19200 provides two useful logic outputs for systems self test, $\overline{BIT}$ and LOS.

BUILT-IN-TEST ($\overline{BIT}$, PIN 29)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 65 LSBs (of the selected resolution), the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an over-velocity condition because the converter loop cannot maintain input-output sync or if the converter malfunctions where it cannot maintain the loop at a null. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

LOSS OF SIGNAL (LOS, PIN 28)

The Loss of Signal (LOS) output is used for system safety. The LOS output changes from logic 0 to 1 if both resolver inputs are disconnected. With disconnected resolver inputs, unpredictable converter performance occurs.

If the LOS signal is used with the 2V Direct Input option, connect a 10M ohm resistor from +S to V and from +C to V. This will insure that if the input resolver signal opens, the input pin will go to V volts.

PROGRAMMABLE BANDWIDTH (BW, PIN 5)

Either low or high bandwidth can be selected by using the BW logic input. A logic 0 applied to BW selects low bandwidth (130 Hz nom), while a logic 1 selects high bandwidth (530 Hz nom). Bandwidth can be changed during converter operation.

Bandwidth and the acceleration constant (K_a) can be determined from the following formulas:

$$\text{Closed Loop Bandwidth (Hz)} = \sqrt{2}\,A/\pi$$

$$K_a = A^2$$

See Dynamic Characteristics Table 4 and figures 23 and 24 for values.

TABLE 4. DYNAMIC CHARACTERISTICS

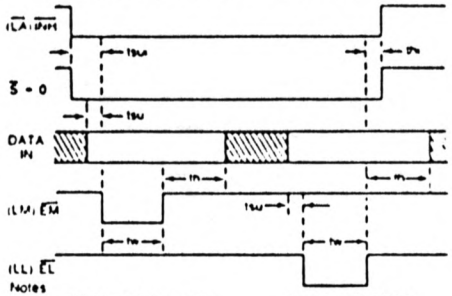
PARAMETER	UNITS	BANDWIDTH							
		HIGH				LOW			
RESOLUTION	BITS	10	12	14	16	10	12	14	16
Input Frequency	KHz	1-6	•	2-6	NR	36 6	•	•	2-6
Tracking Rate	RPS†	800	200	50	12 5	200	50	12 5	3 2
Bandwidth, CL	Hz	530	•	•	•	130	•	•	•
K_a	$1/sec^2$	1 4M	•	•	•	90K	•	•	•
A1**	1/sec	8	•	•	•	2	•	•	•
A2**	1/sec	178	•	•	•	45K	•	•	•
A**	1/sec	1200	•	•	•	300	•	•	•
B**	1/sec	600	•	•	•	150	•	•	•
acc-1 LSB lag	sec^2	512K	128K	32K	8K	32K	8K	2K	500
Settling time	msec	10	15	30	75	40	60	120	300

† RPS minimum
• Same as value to left
•• See figure 24 for definitions of A1, A2, A, and B

CONTROL TRANSFORMER MODE ($\overline{S}$, PIN 6)

The converter will function as a Control Transformer (CT) by placing $\overline{S}$ (pin 6) to logic 0. In the CT mode, the digital inputs are double buffered. $\overline{EM}$ is redefined as LM, $\overline{EL}$ is redefined as LL and $\overline{INH}$ becomes LA (see figures 19 and 27). Figure 18 shows CT mode timing for a two byte transfer.

The CT mode is used when the AC error (e) is needed to drive an external control loop by the difference angle of the resolver input and the digital input. It is also used for presetting the converter to a specific angle to reduce the step response time.



Notes
(1) tw = 100 ns min (pulse width)
th = 50 ns min (hold time)
thua = 0 ns min (hold time inhibit)
tsu = 0 ns min (setup time)
tsua = 300 ns min (setup inhibit)
(2) When $\overline{S}$ is low
(LM) $\overline{EM}$ is latch control for MSB byte.
(LL) $\overline{EL}$ is latch control for LSB byte.
1 = data held in latch.
0 = latch is transparent.
(3) (LA) $\overline{INH}$ is latch control for CT latch.
1 = latch is transparent.
0 = data held in latch.

FIGURE 18. CT MODE TIMING – TWO BYTE TRANSFER, DOUBLE BUFFERED

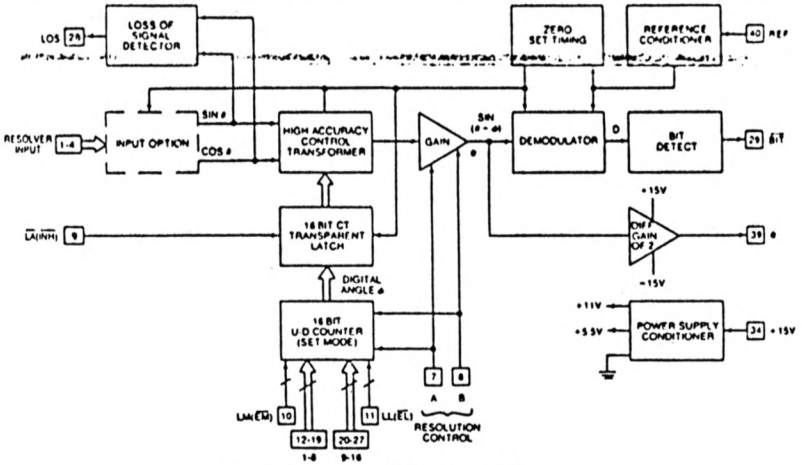


FIGURE 19. CONTROL TRANSFORMER BLOCK DIAGRAM

ANALOG OUTPUTS

The analog outputs are AC error (e) and velocity (VEL). If the analog outputs are not required, ground -15V (pin 36).

AC ERROR (e, PIN 39)

AC Error Out (e) is used in CT mode. The AC error is proportional to the difference between the resolver input angle θ and the digital input angle ϕ, ($\theta - \phi$), with a scaling of:

50mVrms LSB (10 bit mode)
25mVrms LSB (12 bit mode)
12 5mVrms LSB (14 bit mode)
6 3mVrms LSB (16 bit mode)

The error is positive if it is in phase with the reference and negative if it is out of phase with the reference.

The e output can swing ±10V peak min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level.

VELOCITY (VEL, PIN 38)

The velocity output (VEL, pin 38) is a DC voltage proportional to angular velocity $d\theta/dt$. The velocity is the input to the voltage controlled oscillator (VCO), as shown in figure 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO.

The maximum VEL output can swing ±10V min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level. The analog output VEL characteristics are listed in table 5.

The VEL output has DC tachometer quality specs such that it can be used as the velocity feedback in servo applications.

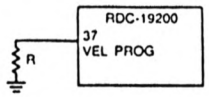
VELOCITY PROGRAMMING (VEL PROG, PIN 37)

The velocity output scale factor can be increased by connecting an external resistor (R) from VEL PROG, pin 37 to ground. By scaling up the output, the noise and offset will increase proportionally. The value of R can be determined by the following formula:

$$R = \frac{10 \times B/A}{1 - B/A}$$

Where:

R = external resistor in K Ohms
A = specified voltage scaling (RPS/VOLT)
B = desired voltage scaling (RPS/VOLT)



To determine A, refer to Table 6, Voltage Scaling.

TABLE 5. VELOCITY OUTPUT CHARACTERISTICS

PARAMETER	UNIT	RDC-19200, 19202		RDC-19201/19203	
		TYP	MAX	TYP	MAX
Polarity		(positive for increasing angle)			
Voltage scaling	RPS/V	See Voltage Scaling Table 6			
Scale Factor	%	5	10	5	10
Scale Factor TC	PPM/°C	100	200	100	200
Reversal Error	°e	1	2	0 5	0 7 overtemp
Linearity	°e output	1	2	0 5	0 7 overtemp
Zero Offset	mV	15	40	15	40
Zero Offset TC	µV/°C	25	50	25	50
Load	KOhms	-	3	-	3
Output Voltage	V	±13	±10 min	±13	±10 min

TABLE 6. VELOCITY OUTPUT VOLTAGE SCALING (RPS/VOLT)

BW	10 BIT	12 BIT	14 BIT	16 BIT
HIGH	80	20	5	1 25
LOW	20	5	1 25	0 32

DYNAMIC PERFORMANCE

A Type II servo loop ($K_v = \infty$) and very high acceleration constants give the RDC-19200 superior dynamic performance as listed in table 1.

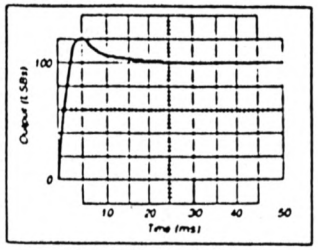
SMALL SIGNAL STEP RESPONSE. Figure 20 illustrates the Small Signal Step Response (100 LSB step) for low and high bandwidth for the four resolutions.

LARGE SIGNAL STEP RESPONSE. Figure 21 illustrates the Large Signal Step Response (179° step) for low and high bandwidth for the four resolutions.

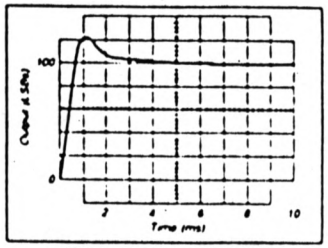
BIT OUTPUT REDUCES SETTLING TIME. By using the $\overline{BIT}$ output together with the A and B inputs, the Large Signal Settling Time may be significantly reduced. Figure 22 shows the connections required for $\overline{BIT}$, A, and B and the resultant settling for the different resolution modes.

VELOCITY RESPONSE

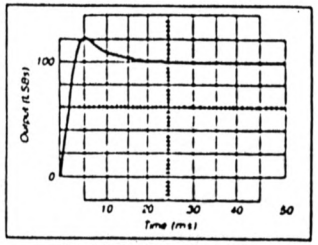
A filter on the VEL output will, for a step input in velocity, eliminate the velocity overshoot (normally critically damped) and filter carrier frequency ripple. Figure 23 shows the VEL output with and without a filter for low and high bandwidths. The VEL filter is shown in figure 24.



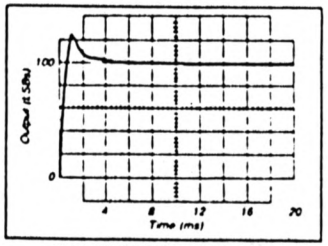
LOW BANDWIDTH – 10 BIT MODE



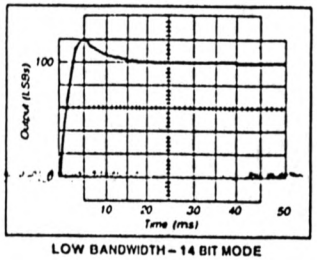
HIGH BANDWIDTH – 10 BIT MODE



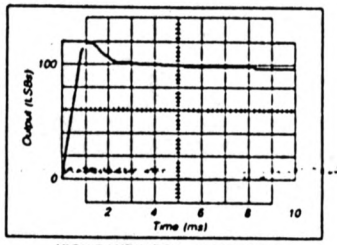
LOW BANDWIDTH – 12 BIT MODE



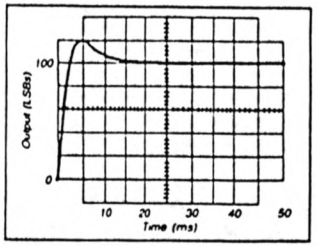
HIGH BANDWIDTH – 12 BIT MODE



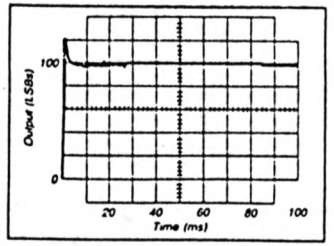
LOW BANDWIDTH – 14 BIT MODE



HIGH BANDWIDTH – 14 BIT MODE

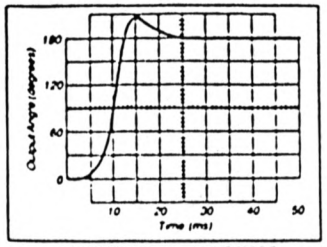


LOW BANDWIDTH – 16 BIT MODE

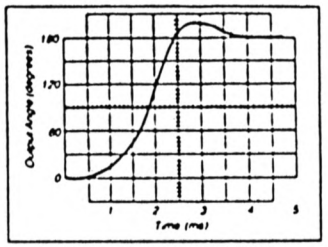


HIGH BANDWIDTH – 16 BIT MODE

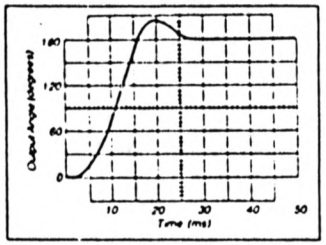
FIGURE 20. SMALL SIGNAL STEP RESPONSE (100 LSB STEP)



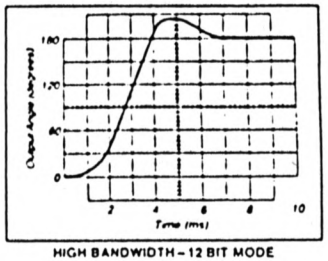
LOW BANDWIDTH – 10 BIT MODE



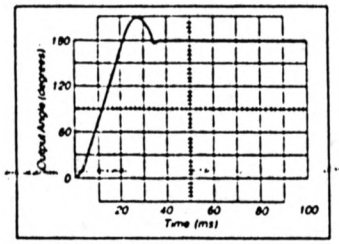
HIGH BANDWIDTH – 10 BIT MODE



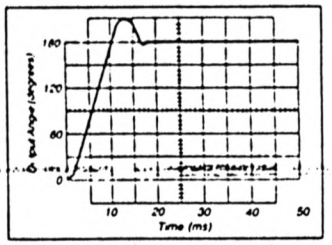
LOW BANDWIDTH – 12 BIT MODE



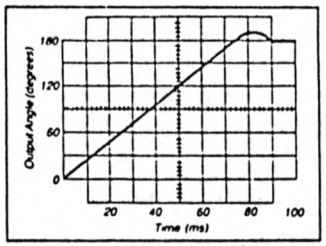
HIGH BANDWIDTH – 12 BIT MODE



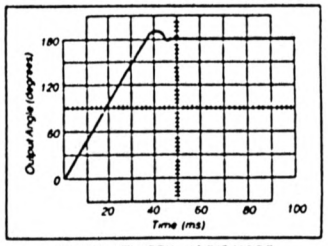
LOW BANDWIDTH – 14 BIT MODE



HIGH BANDWIDTH – 14 BIT MODE

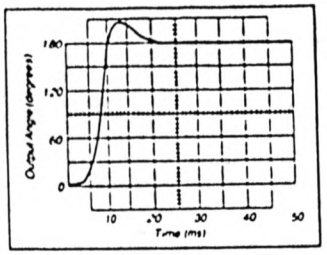


LOW BANDWIDTH – 16 BIT MODE

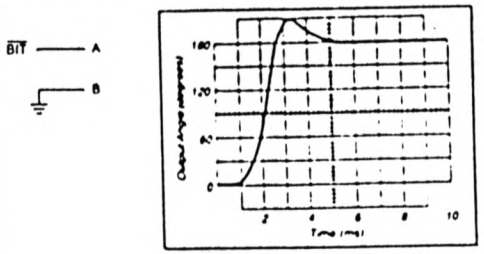


HIGH BANDWIDTH – 16 BIT MODE

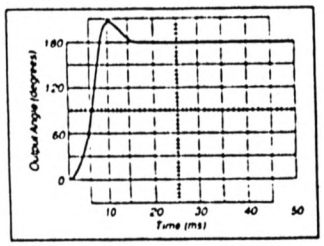
FIGURE 21. LARGE SIGNAL STEP RESPONSE (179° STEP)



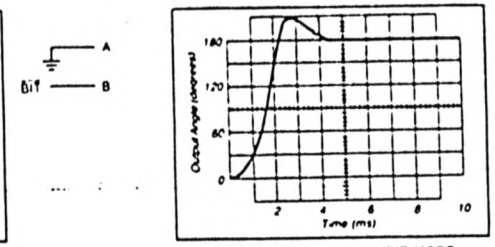
LOW BANDWIDTH 12-10 BIT MODE



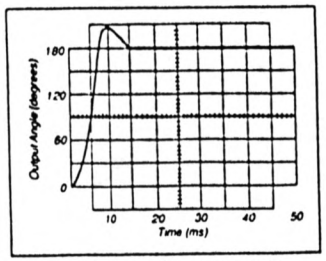
HIGH BANDWIDTH 12-10 BIT MODE



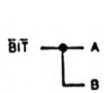
LOW BANDWIDTH 14-10 BIT MODE

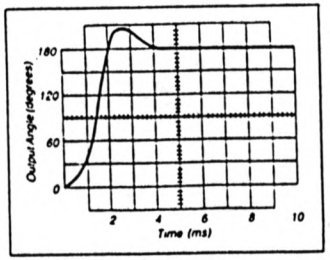


HIGH BANDWIDTH 14-10 BIT MODE



LOW BANDWIDTH 16-10 BIT MODE





HIGH BANDWIDTH 16-10 BIT MODE

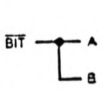
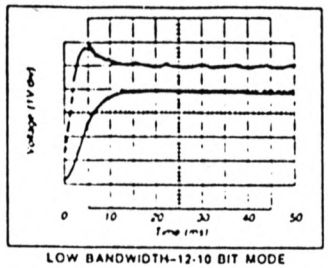
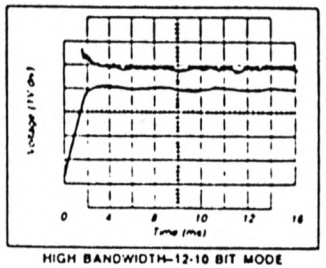


FIGURE 22. USING BIT TO REDUCE SETTLING TIME (179° STEP)



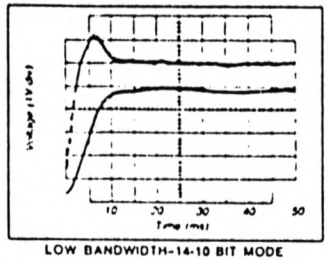
LOW BANDWIDTH-12-10 BIT MODE

BEFORE FILTER
AFTER FILTER



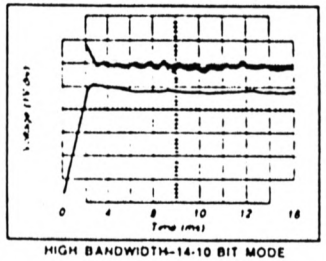
HIGH BANDWIDTH-12-10 BIT MODE

BEFORE FILTER
AFTER FILTER



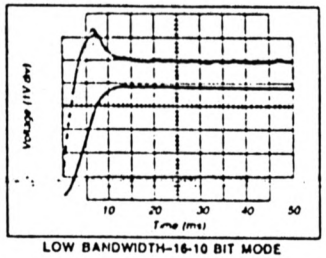
LOW BANDWIDTH-14-10 BIT MODE

BEFORE FILTER
AFTER FILTER



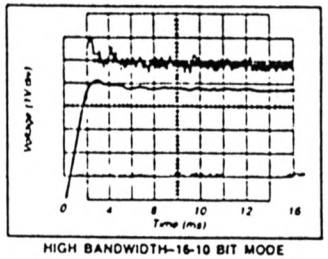
HIGH BANDWIDTH-14-10 BIT MODE

BEFORE FILTER
AFTER FILTER



LOW BANDWIDTH-16-10 BIT MODE

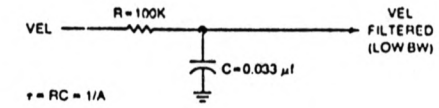
BEFORE FILTER
AFTER FILTER



HIGH BANDWIDTH-16-10 BIT MODE

BEFORE FILTER
AFTER FILTER

FIGURE 23. VEL OUTPUT WITH AND WITHOUT FILTER



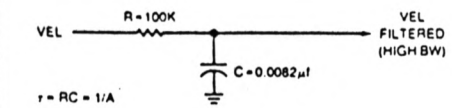
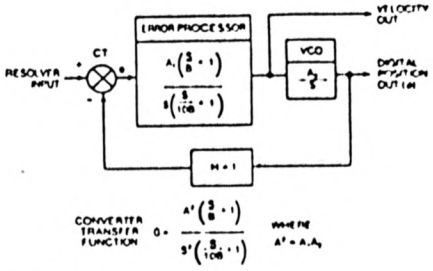


FIGURE 24. VEL OUTPUT FILTERS

TRANSFER FUNCTIONS

The dynamic performance of the converter can be determined from its transfer function block diagram (figure 25) and open and closed loop Bode plots (figures 26 and 27). Table 4 lists the parameters relating to the RDC-19200's dynamic characteristics for different resolution and bandwidth modes.



Note: See table 4 for values of A1, A2, and B

FIGURE 25. TRANSFER FUNCTION BLOCK DIAGRAM

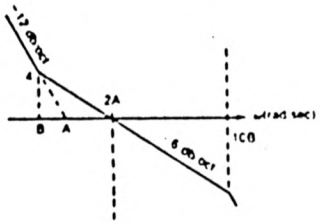


FIGURE 26. OPEN LOOP BODE PLOT

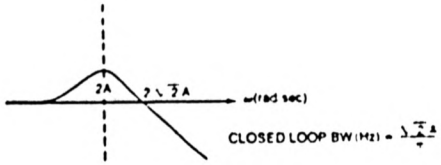


FIGURE 27. CLOSED LOOP BODE PLOT

ACCURACY AND RESOLUTION

Table 7 lists the total accuracy including quantization for the various resolution and accuracy grades.

TABLE 7. ACCURACY/RESOLUTION

RDC-19200 SERIES MODEL NO.	ACCURACY	10 BIT	12 BIT	14 BIT	16 BIT
RDC-1920X-304	2' + 1 LSB	23.1	7.3	3.3	2.3
RDC-1920X-303	3' + 1 LSB	24.1	8.3	4.3	3.3
RDC-1920X-302	4' + 1 LSB	25.1	9.3	5.3	4.3
RDC-1920X-301	8' + 1 LSB	29.1	13.3	9.3	8.3

RDC-19200 APPLICATIONS

USING THE RDC-19200 IN THE CT MODE

The CT mode can be applied in servo systems, as shown in figure 28. In this application, changes in position are commanded by the computer through signals fed to the CT. The CT then drives the motors through DC power amplifiers.

MULTI-TURN APPLICATIONS – USE OF MAJOR CARRY (MC, PIN 32)

Refer to Major Carry paragraph on page 8 for details.

USING THE RDC-19200 AS AN R/D WITH VEL TO STABILIZE POSITION LOOP

Figure 29 illustrates a typical use of a RDC-19200 connected as an R/D using the VEL output to stabilize the position loop.

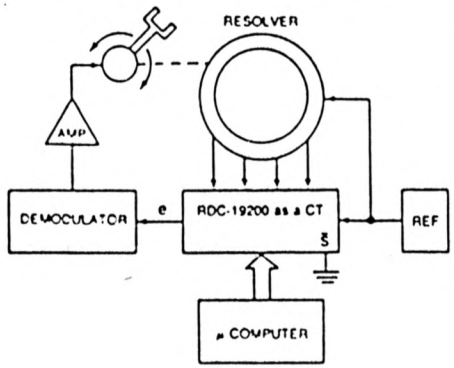


FIGURE 28. CT MODE APPLICATION

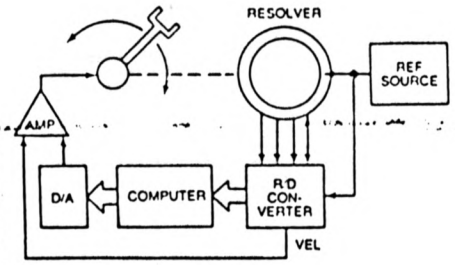


FIGURE 29. R/D WITH VEL TO STABILIZE POSITION

INTERFACING THE RDC-19200 WITH AN IBM PC/XT/AT®

The RDC-19200 can be connected to an IBM PC/XT/AT through the IBM PC Bus located at address HEX 300 through 303. This location is reserved by the PC for prototype cards. Figure 31 illustrates the connection to the IBM PC Bus; figure 30 illustrates the timing considerations for the interface.

RDC-19200 TO IBM PC/XT/AT THEORY OF OPERATION

1. The port address where the RDC-19200 is located is hard wired with jumpers into the 74LS688 address decoder. This address is HEX 300 through 303 and is reserved for prototype cards.

2. Address line A1 selects the upper or lower 8 bits of the RDC-19200 to be placed on the Bus. When A1 is high, bits 1-8 are selected.

3. Address line A0 sets and resets the RDC-19200 INHIBIT line. When A0 is low, the INHIBIT command ($\overline{INH}$) is invoked.

4. To read the output of the RDC-19200, perform the following:

   a. Send address HEX 302 to INHIBIT the RDC-19200 (hold data stable) and place bits 1-8 on the Bus. Read and store data on D0 to D7.

   b. Send address 300 HEX to keep the RDC-19200 in the INHIBIT mode and place bits 9-14 on the Bus. Read and store data on D0 to D7.

   c. Read address 301 HEX or 303 HEX to release the RDC-19200 from the INHIBIT mode and prepare for the next measurement. No valid data will be on the bus during this command.

5. Since the output data is not valid until 0.5 μs after the INHIBIT command is invoked, the I/O READY line is held low for this period of time. When I/O READY returns to the high level, the data on the bus is ready on the next negative clock edge.

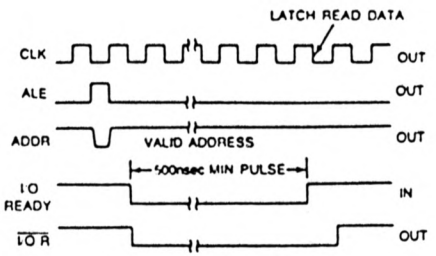


FIGURE 30. PC APPLICATION – I/O READ CYCLE TIMING

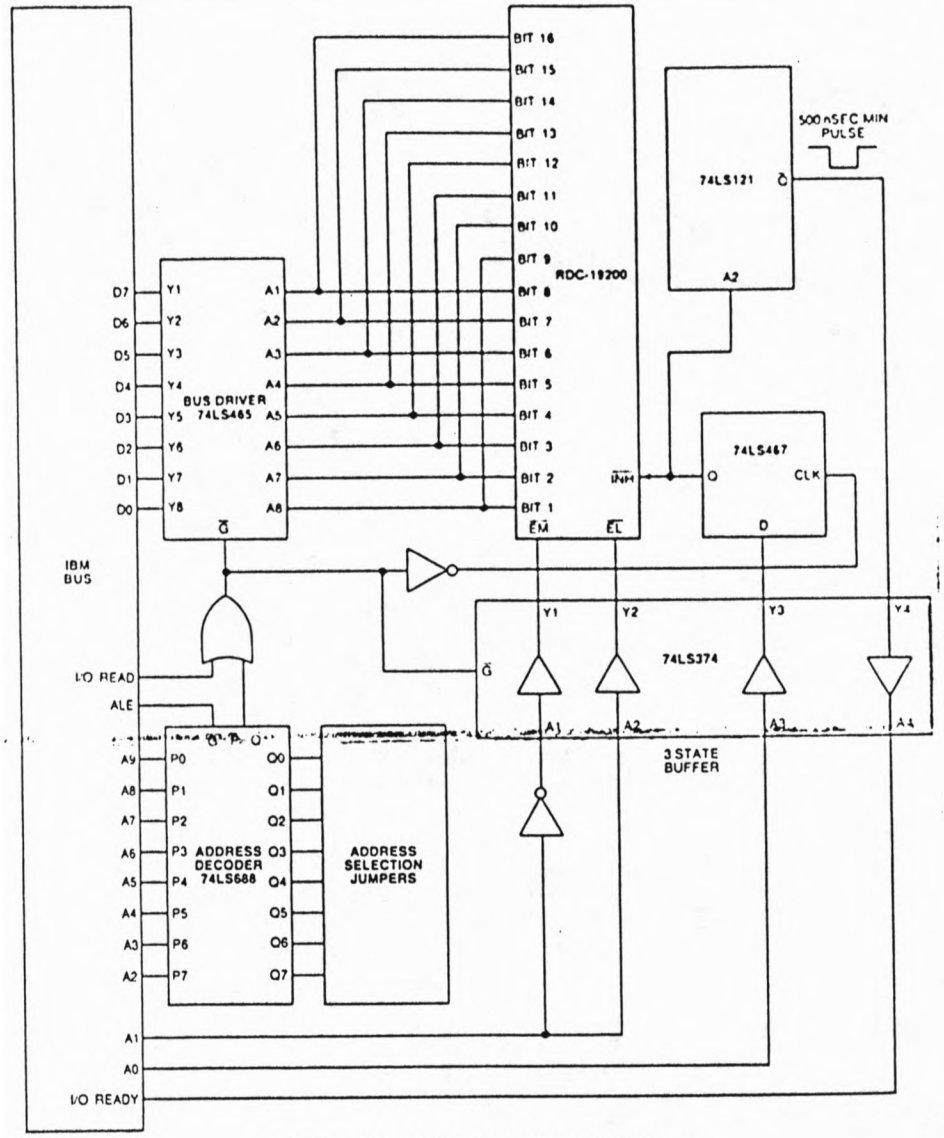


FIGURE 31. RDC-19200 TO PC CONNECTION DIAGRAM

TABLE 8. RDC-19200 PIN FUNCTIONS

PIN NO.	TITLE	I/O	FUNCTION
1	S1(R)/V(X)	I	(R) = 11.8V Resolver input, (X) = 2V Direct input
2	S2(R) - C(X)	I	(R) = 11.8V Resolver input, (X) = 2V Direct input
3	S3(R) - S(X)	I	(R) = 11.8V Resolver input, (X) = 2V Direct input
4	S4(R) -	I	(R) = 11.8V Resolver input
5	BW	I	Bandwidth. Logic 1 for high BW (530 Hz), logic 0 for low BW (130 Hz)
6	S	I	Control Transformer Set. Logic 1 for normal tracking, logic 0 for CT operation. Used when AC error (e) is needed to drive external control loop by the difference angle of the resolver input and the digital input, and for presetting the converter to a specific angle to reduce the step response time.
7	A	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bit, depending on logic level.
8	B		B A Resolution 0 0 10 BIT 0 1 12 BIT 1 0 14 BIT 1 1 16 BIT
9	$\overline{INH}$	I	Inhibit. Logic 0 prevents digital output bits from changing.
10	$\overline{EM}$	I	Enable MSBs. Logic 0 enables digital output bits 1-8. Logic 1 disables these bits.
11	$\overline{EL}$	I	Enable LSBs. Logic 0 enables digital output bits 9-16. Logic 1 disables these bits.
12	1	O	Digital Output Bit 1 (MSB all modes)
13	2	O	Digital Output Bit 2
14	3	O	Digital Output Bit 3
15	4	O	Digital Output Bit 4
16	5	O	Digital Output Bit 5
17	6	O	Digital Output Bit 6
18	7	O	Digital Output Bit 7
19	8	O	Digital Output Bit 8
20	9	O	Digital Output Bit 9
21	10	O	Digital Output Bit 10 (LSB-10 BIT MODE)
22	11	O	Digital Output Bit 11
23	12	O	Digital Output Bit 12 (LSB-12 BIT MODE)
24	13	O	Digital Output Bit 13
25	14	O	Digital Output Bit 14 (LSB-14 BIT MODE)
26	15	O	Digital Output Bit 15
27	16	O	Digital Output Bit 16 (LSB-16 BIT MODE)
28	LOS	O	Loss of signal. Used for system safety. The LOS output changes from logic 0 to 1 if both resolver inputs are disconnected.
29	BIT	O	Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds 65 bits, approx. Also logic 0 for an over-velocity condition.
30	CB	O	Converter Busy. Indicates digital output update.
31	U	O	Direction. Logic 1 to count up, logic 0 to count down.
32	MC	O	Major Carry. Used for forms counting [illegible]. Format: y high, goes low for all 1's when counting up or all 0's when counting down.
33	+5V	I	Supply Voltage
34	+15V	I	Supply Voltage
35	GND	-	Ground
36	-15V	I	Supply Voltage
37	VEL PROG	I	Velocity Programming. Increases output scale factor with external resistor (R) from VEL PROG. pin 37 to ground.
38	VEL	O	Velocity. DC voltage proportional to angular velocity.
39	e	O	AC Error. Used in CT mode. e is proportional to the difference between the resolver input angle θ and the digital output angle ϕ (θ - ϕ).
40	REF	I	AC Reference Input. Used to drive internal demodulator.

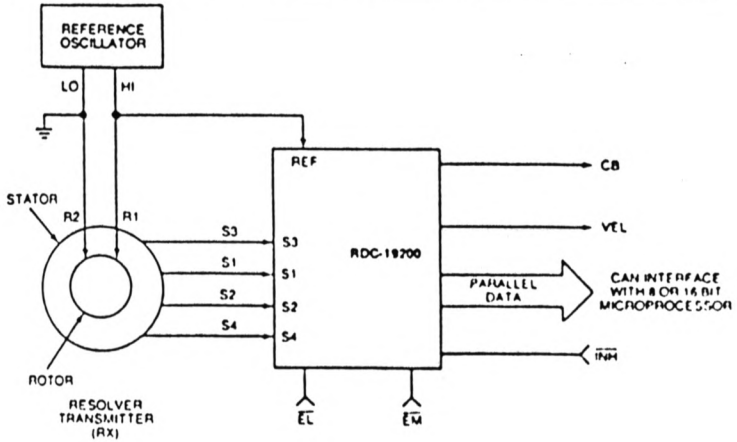


FIGURE 32. RESOLVER CONNECTION – 11.8V

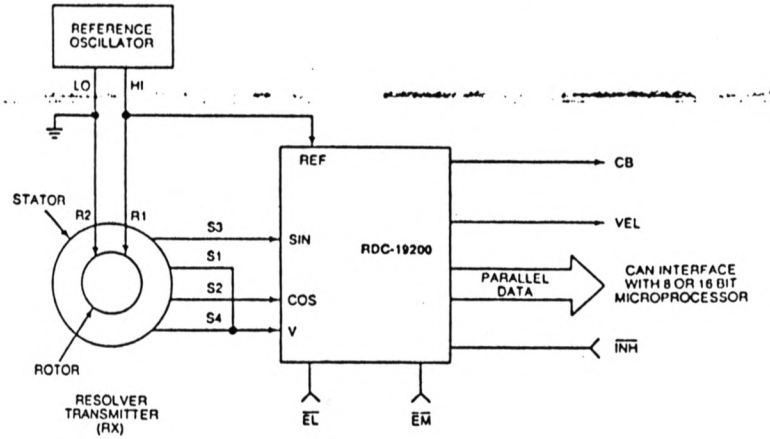


FIGURE 33. RESOLVER CONNECTION – 2V

SOURCES OF SOCKETS FOR THE RDC-19200

The following companies are sources of sockets for use with the RDC-19200 Series. Consult them for more information.

Aries Electronics, Inc.
P.O. Box 30
Frenchtown, NJ 08825
Tel: 1-201-996-6841

Single In-Line Socket
Strip-Line Socket
Part No. 20-05511-11

Circuit Assembly Corp
3169 Red Hill Avenue
Costa Mesa, CA 92626
Tel: 714-540-5490

Part No. CA-20-STL-XX XX-X

ORDERING INFORMATION

RDC-1920X-30X

Accuracy

- 0 = 10 min + 1 LSB (1) (16 LSBs Differential Linearity, RDC-19200 and RDC-19202 only)
- 1 = 8 min + 1 LSB (12 LSBs Differential Linearity)
- 2 = 4 min + 1 LSB (8 LSBs Differential Linearity)
- 3 = 3 min + 1 LSB (4 LSBs Differential Linearity)
- 4 = 2 min + 1 LSB (4 LSBs Differential Linearity)

Configuration:

- 0 = 11.8V, 2% Linearity
- 1 = 11.8V, 0.7% Linearity
- 2 = 2V, 2% Linearity
- 3 = 2V, 0.7% Linearity

Notes:
(1) Vel and e not characterized on models RDC-19200-300 and RDC-19202-300.
(2) Differential Linearity is x LSB in the 16th bit.

Dimensions are inches (mm)

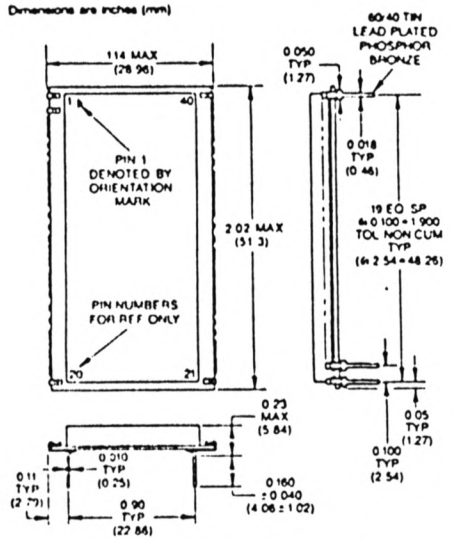


FIGURE 34. RDC-19200 MECHANICAL OUTLINE

CONNECTING THE RDC-19200

The RDC-19200 can be attached to a PC board using hand solder or wave soldering techniques. Limit exposure to 300°C (572°F) max. for 10 seconds maximum.

Do not use vapor phase soldering as this product contains SN60 or SN62 solder which melts at 180°C (356°F).

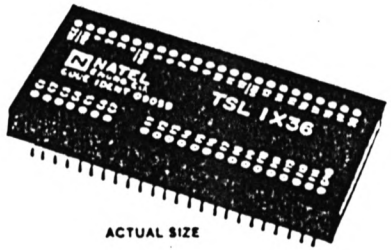
Since the RDC-19200 Series converters contain a CMOS device, standard CMOS handling procedures should be followed.

NATEL
TSL 1X36

TWO Speed Synchro Data Processor
3-State 20-bit Data Output

Features

- Small size
  (1.3 x 2.6 x 0.35 inch)
- High resolution
  (20 bits)
- High accuracy
  (21 bits or ±½ LSB)
- 3-state output
  (8 and 16-bit data-bus compatible)
- 36:1, 36:2, 18:1, 9:1 Ratios
  (With same module)
- No ambiguous output readings
- Fast parallel operation (250 ns)
- Automatic correction of misalignment
  between synchros
  (up to ±90° of fine synchro)
- Priced at $235/USA price
  (TSL 1X36-1S)



ACTUAL SIZE

Applications

Ordnance control
Radar tracking
Navigation
High accuracy industrial control systems

Description

Model TSL 1X36 accepts 2 binary word inputs from two synchro (or resolver)-to-digital converters in a mechanically or electrically geared coarse/fine system and provides a single unambiguous 20-bit binary output representing the coarse shaft angle. A new feature provided in the TSL 1X36 is its 3-state output, available in three bytes, which allows it to be compatible with an 8-bit data-bus. With a resolution of 20 bits, the TSL 1X36 processor provides an accuracy of ± ½ LSB . . . a factor of 4 improvement over existing units such as Natel's TSL1036.

In addition to high accuracy and 3-state output, the processor is less than half the size of existing designs. In spite of its size, the processor is not a hybrid, rather it employs a different design approach that allows it to cut size without increasing cost.

Although the unit described in this data sheet provides for ratios of 36:1 and its binary multiples, processors for speed ratios of 2:1 thru 72:1 are available on special order.

The inputs to the TSL 1X36 are up to 14 bits from the fine converter and 7 bits from the coarse converter. The two-speed processor may be used with any synchro (or resolver)-to-digital converters that produce a parallel binary output.

When used with Natel Hybrid converters of the 1000 series, a complete 2-speed converter occupies less space than the original processor . . . (3.1 x 2.6 x .42"), while providing a 20-bit, 3-state output.

Two-speed System

A two-speed synchro (or resolver) system consists of two synchros geared electrically or mechanically to a single shaft. One synchro provides coarse positioning of the angle and the second synchro, through gearings, provides fine positioning of the angle and improves the resolution and accuracy of the system by a multiple equal to the gear ratio (less gearing errors).

In order to convert the shaft angle information into a single unambiguous digital word, the two-speed processor TSL 1X36, together with two synchro (or resolver)-to-digital converters is used. A coarse converter of very low accuracy and a fine converter of moderate accuracy together with the TSL 1X36 logic combiner provide a very high accuracy 2-speed conversion system. The TSL 1X36 processor can accept data from any type of synchro converter that provides parallel binary outputs. This includes all tracking, sampling types or multiplexed . . . hybrid or discrete converters (for information on synchro converters request the Natel Synchro Conversion catalog).

Correction for Misalignment Error

In a 2-speed synchro system it is almost impossible to mechanically align the two synchros exactly. In addition there is a backlash error in the mechanical gearing of two synchros. These errors, called misalignment errors, are automatically corrected in the two-speed processor. The TSL 1X36 corrects misalignments of up to ± 90° of fine synchro shaft angle (±2.5° of coarse shaft angle for 36:1 system) by using the fine synchro converter input as the reference and continuously adjusting the data of the coarse synchro converter as required.

Theory of Operation

The operation of Model TSL 1X36 is illustrated in the block diagram of figure 1. The 7-bits of coarse digital word are multiplied by 36 to obtain coarse data rescaled to a binary multiple of the fine speed digital word. The 3 MSBs of fine speed data are compared with the corresponding bits of rescaled coarse data. If the two do not match the coarse data is modified to align it with the information contained in the fine data. The corrected coarse data together with 14-bits of fine data represent true angle free of any ambiguity or misalignment error. This data is divided by 36 to obtain the 20-bit digital word whose MSB is 180° and represents angular position of the coarse shaft of the two-speed system. This data is then supplied to three, independently controlled, 3-state buffers organized as a high byte of 4 MSBs, a middle byte of the next 8 bits and a low byte of 8 LSBs. Simultaneous parallel output of all 3 bytes is obtained by applying logic "0" (Ground) to the three enable control lines, $\overline{HBE}$, $\overline{MBE}$ and $\overline{LBE}$.

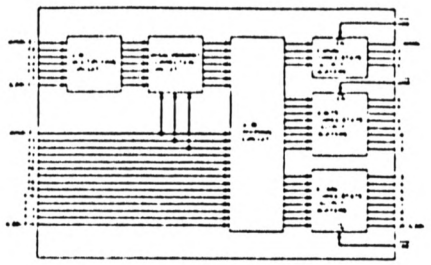


FIGURE 1. Block Diagram TSL 1X36

Specifications

PARAMETER	VALUE
Inputs	
Speed ratios Fine speed input Coarse speed input Logic levels Loading	36:1, 18:1, 9:1 Up to 14 bits parallel binary angle Up to 7 bits parallel binary angle DTL/TTL compatible (positive logic) 1 TTL load
Outputs	
Resolution Accuracy Logic levels Drive capability	Up to 20 bits parallel Binary Angle ± ½ LSB DTL/TTL compatible (positive logic) 5 TTL loads
Three State Outputs	
Low state OFF state current (I_{OZL}) High state OFF state current (I_{OZH}) Output short circuit current (I_{OS}) ENABLE CONTROLS ($\overline{HBE}$, $\overline{MBE}$, $\overline{LBE}$) Logic levels Loading	-100 µA MAX (V_O=0.5 V) +20 µA MAX (V_O=2.4 V) -50 mA typical DTL/TTL compatible 1 TTL load
Maximum mechanical misalignment between coarse and fine synchro	±90° of fine speed input e.g. ±2.5° of coarse shaft for 36:1 System
Conversion Time	250 ns typical, 370 ns max
Power Supply	
Voltage Current	5 V ±5% 500 mA typical, 650 mA max
Physical Characteristics	
Size	2.625 x 1.325 x 0.35 inch (66.7 x 33.7 x 8.9 mm)
Weight	2 oz (56 gms) max

Absolute Maximum Ratings

Supply voltage ..... -0.5 V-dc to 7.0 V-dc
Input voltage ..... -1.0 V-dc to 5.5 V-dc
Input current ..... -10 mA to 5mA
Output current ..... -50 mA to 50 mA
Storage temperature ..... -55°C to +135°C

Pin Designations

FIGURE 2. TSL 1X36 Pin Assignment

C1-C7	Coarse Angle Binary Input C1 is MSB, C7 is LSB
F1-F14	Fine Angle Binary Input F1 is MSB, F14 is LSB
GND	Power supply ground digital ground
5 V	Power supply voltage +5 V-dc
1-20	Combined Angle Binary Output 1=MSB, 20=LSB
$\overline{HBE}$	High Byte Enable ---- Output bits 1 through 4 are enabled (low impedance of 3-state output) when $\overline{HBE}$ is set to a logic "low." When $\overline{HBE}$ is set to a logic "high," the output bits 1 through 4 are disabled (high impedance state of 3-state output)
$\overline{MBE}$	Middle Byte Enable ---- A logic low on $\overline{MBE}$ enables output bits 5 through 12
$\overline{LBE}$	Low Byte Enable ---- A logic low on $\overline{LBE}$ enables output bits 13 through 20

Note: For simultaneous 20-bit parallel output $\overline{HBE}$, $\overline{MBE}$, and $\overline{LBE}$ should be connected to ground.

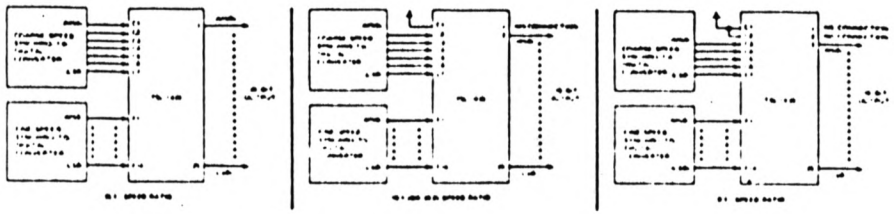


FIGURE 3 Connections for Different Speed Ratios

Input & Output Interface

Figure 3 shows input connections for different speed ratios. Note that for a speed ratio of 18:1 coarse input C1 is grounded and output MSB (180°) is the output labeled 2. For a speed ratio of 36:2, although input and output connections are same as that for 18:1, the MSB output (2) represents 90°. For a speed ratio of 9:1 inputs C1 and C2 are connected to ground and output bit 3 is the MSB (180°). For fine speed digital input of less than 14-bits unused LSB inputs must be connected to ground.

Depending upon the type of converters used -- sampling or tracking -- there are different methods of transferring data. The input data must be stable for the duration of conversion by the TSL 1X36.

The recommended method for data transfer from tracking converters is to combine converter busy outputs of both fine and coarse synchro converters with an OR gate to monitor when neither converter is updating. Apply an inhibit pulse to both converters simultaneously and when the data output from both converters is stable (as indicated by the combined busy output) transfer output data. The conversion time for the TSL 1X36 is 320 ns maximum.

Data transfer from sampling converters is accomplished by combining the DATA READY outputs of both fine and coarse synchro converters with an AND gate. When data is ready for both converters the input data may be transferred. If, instead of DATA READY, a CB (converter busy) signal is available, then an OR gate would be required to determine if the data is stable. For multiplexed systems storage registers would be required for fine and coarse data. Contact one of our applications engineers if you need assistance for your design.

OUTPUT DATA TRANSFER on an 8-bit data-bus is shown in figure 4. The timing diagram for data transfer is shown in figure 6. Access time and recovery time for enable controls is shown in the timing diagram of figure 5. The output data is available 320 ns after the input data is applied. When a logic low is applied to the enable controls, the corresponding data-bits are loaded on the 8-bit data bus. Enable control $\overline{LBE}$ transfers 8 LSBs, $\overline{MBE}$ transfers 8 middle data bits and $\overline{HBE}$ transfers 4 MSBs on the data bus.

Note that user should avoid having more than one register enabled on the bus at one time since the enabled outputs will deliver short circuit current into other enabled outputs wired together. While physical damage to the converter is unlikely, long-range affects of short circuit currents are unpredictable.

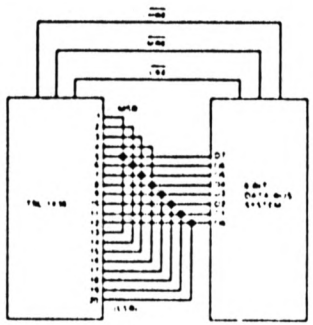


FIGURE 4 Output Connections for 8 Bit Data Bus

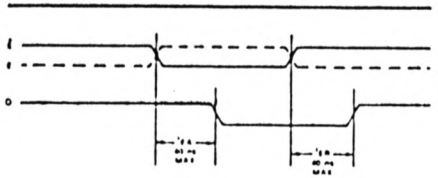


FIGURE 5 Enable Access Time and Recovery Time

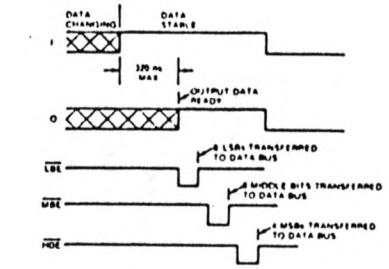
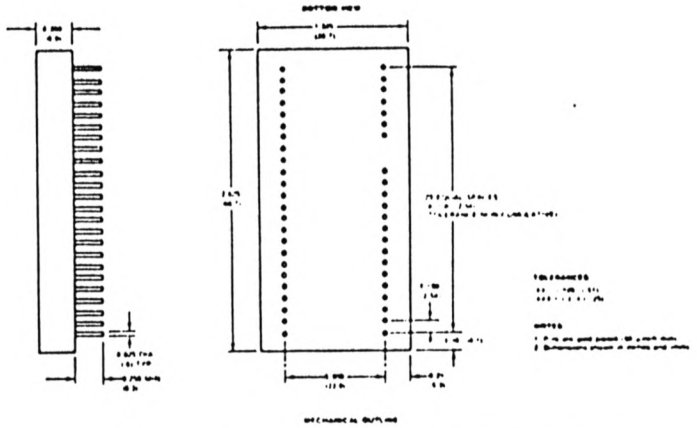


FIGURE 6 Data Transfer Timing Diagram



Ordering Information

TSL 1X36---T M

Temperature Range	Mil - specification
1=0°C to 70°C	S=standard
3=-55°C to +105°C	B=MIL-STD-883B
	C=MIL-STD-883C

For speed ratios other than 36:1, contact factory for part number.

Other products available from NATEL

- Hybrid (36-pin DDIP size) Synchro (Resolver)-to-Digital converters with 10 to 16-bit resolutions (1000 series)
- Hybrid (36-pin DDIP size) Digital-to-Synchro (Resolver) converter with 14 and 16-bit resolutions (2000 series)
- Two-speed Synchro (Resolver)-to-Digital converters with 18 and 20-bit resolutions in a single package. (Models 2SD402 and 2SD412)
- Multiplexed Synchro (Resolver)-to-Digital converters.
- Solid State control transformers (SSCT) and differential transmitters (SCDX).
- Angle position indicators and synchro instrumentation for one-speed and multi-speed applications.
- High Power synchro/resolver drivers.
- Code-converters.

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

Natel Engineering Co., Inc.
8954 Mason Ave.
Canoga Park, CA 91306 (USA)

Natel Hybrid Division
21602 Marilla Ave.
Chatsworth, CA 91311 (USA)

Phone: (213) 882-9620 • TWX: 910-494-1959

y=.54
y=1.54 525
-2.65

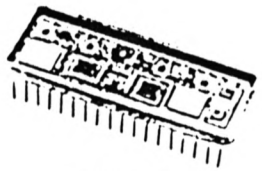
M103 - 2/81

NATEL
HSD/HRD1014

Synchro (Resolver)-to-Digital Converter Microprocessor Compatible 14-bit Hybrid

Features

- 3-state latched output (inhibit does not interrupt tracking)
- 8- and 16-bit microprocessor compatible
- 2.6 arc-minute accuracy
- Very high tracking rate (3600 degrees per second)
- High common-mode rejection (true differential inputs)
- High input impedance
- Programmable Gain Control
- TTL and CMOS compatible
- Analog velocity and error voltages outputs
- Single 36-pin hybrid DDIP package
- Hi-rel MIL-STD-883B processing
- Priced at $435/USA price (HSD1014-149S)



ACTUAL SIZE

Applications

Avionics systems
Antenna monitoring
Servo systems
Coordinate conversion
Fire control systems
Axis rotation
Engine controllers
Industrial control systems
Simulation
Robotics
Machine tool control systems
Solar panel control systems

Description

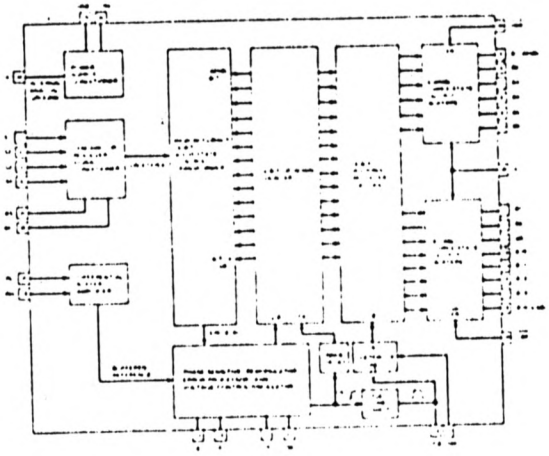
The HSD1014 (HRD1014), a 14-bit Synchro (Resolver)-to-Digital Converter, packaged in a 36-pin DDIP hybrid, offers high accuracy, microprocessor compatibility and excellent dynamic performance. Requiring only a single +15 V-dc main power supply for its operation, the converter maintains both static and dynamic accuracy over a wide range of power supply variations. The digital output voltage levels can be controlled independently by a logic voltage input V_L. The logic supply voltage V_L can range from 4.5 V-dc to the main power supply voltage. At 5 V-dc logic supply the output is CMOS/TTL compatible and can drive one 54/74 gate load or four 54LS/74LS gate loads.

Using a high-accuracy differential signal conditioner for the resolver input and a resistive scott-tee for the synchro-input, the converter provides common mode rejection in excess of 70 dB. The input impedance remains constant and balanced independent of dc power to the converter. This feature prevents loading of the synchro and reference input lines when the converter is not powered. This technique also permits resistor programming for non-standard input voltages.

Transferring data from the 1014 is facilitated by the use of a transparent latch with 3-state outputs, configured as two independently enabled bytes. Not only does this allow data to be read without interrupting converter tracking, it also permits memory-mapped data interface and control with the most popular 8- and 16-bit microprocessors and single-board computers.

Three analog outputs: velocity, unfiltered dc error and filtered dc error near null are made available from the 1014. A gain-control pin (Ge) is provided to allow user to program the converter for non-standard input voltages without degrading the accuracy of the converter.

Although pin-compatible Synchro (Resolver)-to-Digital converters are available, Natel's Model 1014 offers superior dynamic performance while maintaining its high accuracy. In addition, the Model 1014 uses established reliability (ER) components and is built in accordance with the requirements of MIL-STD-883B including 168 hours of active burn-in.



Theory of Operation

The operation of the Model HSD1014 is illustrated in the functional block diagram of figure 1. The HSD1014 is a high gain Type II tracking converter exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle (ϕ) and the Synchro (or Resolver) input angle (θ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. Once synchronized, the output angle tracks the input angle continuously and the data is always fresh and always available (except during transitions). The input signal conditioner accepts either a Synchro or Resolver input and converts it into low level signals $\sin\theta$ and $\cos\theta$. The feed-back loop consisting of an error processor, voltage-controlled oscillator and a 14-bit up-down counter produces a 14-bit digital angle (ϕ). The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage, (e) according to the following trigonometric identity:

$$"e" = \sin(\theta-\phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

When the error voltage goes to null, $\sin(\theta-\phi)$ is zero, which makes the angle ϕ equal to the angle θ. Thus, the digital output represents the input shaft angle. The error voltage (e) is an ac signal proportional to the instantaneous error between the input angle and the feed-back angle. This error voltage is synchronously demodulated with the buffered reference signal. The demodulated output is a dc signal proportional to the tracking error $(\theta-\phi)$. The dc error is integrated to produce a voltage proportional to the converter's tracking velocity. The velocity signal (available at pin 23) is the control input to a voltage-controlled oscillator. The VCO output changes the up-down counter, which contains the feed back angle, ϕ. The up-down counter functions as the second integrator in the tracking loop. The output of the counter is then supplied to a holding register and dual 3-state buffers for output interface.

Outputs Interface

The output interface circuit consists of a 14-bit holding register (latches) and dual three-state buffers. This not only imparts a versatile interface capability (data multiplexing on 8- or 16-bit data bus) to the HSD1014, but also enables the $\overline{INH}$ (inhibit) control to be used without opening the converter loop. This feature is important since synchro/resolver-to-digital converters typically disable the up-down counter during data transfer causing severe transients in the output data when the converter is re-enabled (inhibit removed) and the tracking loop is forced to re-synchronize.

When $\overline{INH}$ is at logic "high" or open, each clock pulse from the VCO changes the up-down counter and output by 1 LSB. When $\overline{INH}$ is at a logic low, the holding register is latched (within 3 μsec maximum) and although the up-down counter is updated continuously, the output data is stable. A 2μsec pulse is generated at CB (pin 24) every time up-down counter changes by 1 LSB.

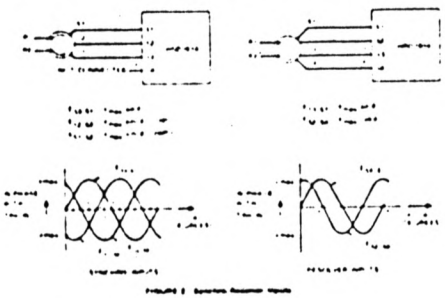
The outputs of the holding register are buffered with two three-state buffers with separate enable controls. When $\overline{HBE}$ is at logic "low," the 6MSBs (B1 through B6) are enabled. When $\overline{LBE}$ is at logic "low," the 8 LSBs (B7 through B14) are enabled. When $\overline{HBE}$ and/or $\overline{LBE}$ are at logic "high" the corresponding bits are in the high impedance state (disabled) and the data-bus sees an essentially open line.

Note that applying inhibit to the converter will latch the data in the 14-bit holding register (and will prevent it from being updated) . . . but will not interfere with the continuous operation of the conversion process.

Enable controls $\overline{HBE}$ and $\overline{LBE}$ operate only on three-state buffers and do not affect the converter loop.

Synchro/Resolver Connections and Phasing

The connections for synchro and resolver inputs are shown in figure 2. The input signal conditioner of the Model 1014 converter is designed to accept either synchro or resolver inputs. In addition it uses differential amplifiers and matched precision resistors to provide a high common-mode rejection ratio. This eliminates the need for external transformers for most applications. The input signal conditioner performs two functions. For both synchro and resolver format inputs it serves as a precision attenuator reducing the amplitude of high level ac input signals to levels which can be processed by the converter. For a synchro input, this network transforms three wire synchro information into resolver format (sin θ and cos θ).



Input Protection

Both signal and reference inputs are true differential inputs, and use precision thin-film resistors for signal attenuation. If input voltages exceed the absolute maximum ratings, the thin-film resistors may be destroyed. To prevent this from happening, it is recommended that transient voltage suppressors be installed on both signal and reference lines. Synchros and resolvers are highly inductive and can generate or couple transients many times greater than their normal signal voltages and can easily exceed the absolute maximum ratings. This situation is particularly likely to occur in cases where the excitation or source voltage for the synchro (resolver) is switched on or off. Transients can also occur by other equipment being turned on or off. Figures 3 and 4 show recommended methods of connecting synchro and resolver inputs. Transient voltage suppressor given in the tables (or equivalent) must be used to assure input protection.

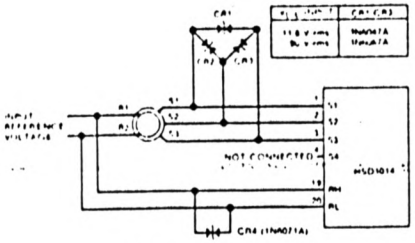


FIGURE 3 HSD1014 Input Protection

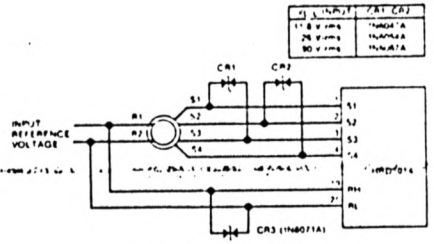


FIGURE 4 HRD 1014 Input Protection

Resistor Programming for Non-standard Input Voltages

Non-standard input signal voltages are accommodated with the addition of an external resistor connected between Gain control, Ge (pin 31), and Bias Voltage, V(pin 34). The circuit configuration for resistor programming is shown in figure 5. The formula for determining the value of external resistor R1 and the converter model to be used are shown in the table. The resistor R1 increases the gain of Voltage Control Oscillator (VCO), thereby compensating for lower input voltages. For input voltages greater than 90 V-rms line-to-line, the method described in Natel HSRD1006 data sheet can be used. Contact factory if you require assistance.

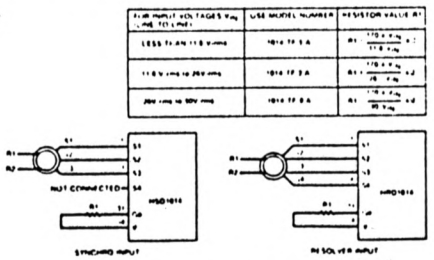
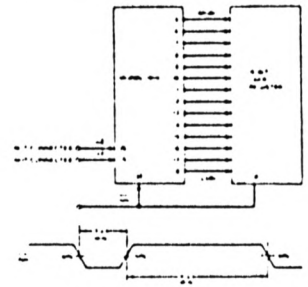


FIGURE 5 Resistor Programming for Non-standard Inputs

Asynchronous Data Transfer

Asynchronous data transfer from the 1014 Converter is shown in figure 6. Control functions $\overline{HBE}$ and $\overline{LBE}$ have internal pulldown circuitry, permitting these pins to be left open. The data is continuously available at the output pins, but it may be changing at any specific time. In order not to transfer data during transition times, the inhibit function should be used. There are two methods available for transferring data. One method is to monitor the CB output and transfer data at the trailing edge of the CB pulse. The preferred method is on command signal. Set the $\overline{INH}$ input to logic "low" for not less than 3 µsec. The 14-bits of output data may then be transferred.

Note that within 4µsec after the inhibit is removed, updated accurate data is available for the next cycle of data transfer. This is made possible as the $\overline{INH}$ does not interrupt the conversion process.



Two Byte Data Transfer Or 8-Bit Data Bus

The circuit configuration for transferring the 14-bit output of the Model 1014 to an 8-bit data-bus is shown in figure 7. Note that $\overline{INH}$ signal, a logic "low," is applied for the entire data transfer cycle to prevent updating of internal holding register (latches). After $\overline{INH}$ is applied, wait for 3µsec before transferring any data. When $\overline{HBE}$ is at logic "0," the 6 MSBs are transferred to the data-bus. When $\overline{LBE}$ is at logic "0" the 8 LSBs are transferred to data-bus. Note that for the data transfer, $\overline{HBE}$ and $\overline{LBE}$ can be applied in any order.

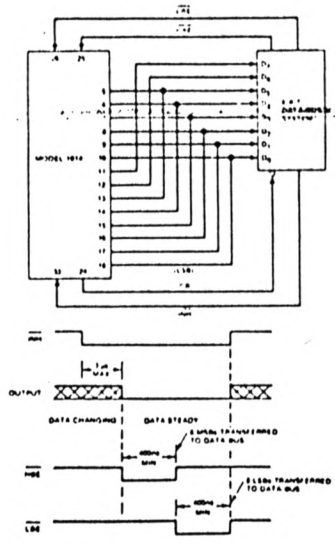


FIGURE 7 Digital Connections and Timing for Two-Byte Data Transfer

Single Byte Data Transfer

The circuit configuration for transferring the output of the Model 1014 to a 16-bit data-bus is shown in figure 8. Apply logic "low" to $\overline{INH}$ input. Wait for 3µsec and then apply a logic low to enable inputs ($\overline{HBE}$ and $\overline{LBE}$).

Note that within 4µsec after the inhibit is removed, updated accurate data is available for the next cycle of data transfer. This is made possible as the $\overline{INH}$ does not interrupt the conversion process. Only the holding register (latches) are prevented from updating during the time $\overline{INH}$ is at logic "low."

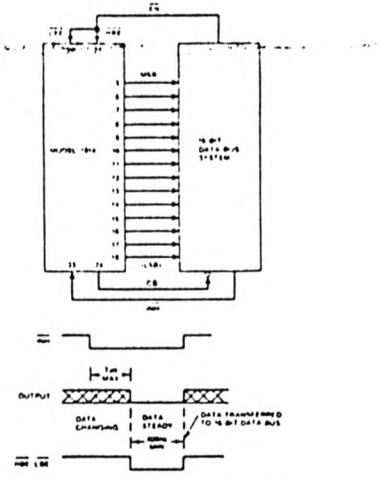


FIGURE 8 Digital Connections and Timing for Single-Byte Data Transfer

Dynamic Performance

The 1014 design incorporates the proven Type II tracking design (KV_{ff}) and has been configured to provide superior dynamic performance independent of power supply voltage over the range of 11 V-dc to 17 V-dc.

The converter will track the input angles up to specified tracking rates (see specifications, pages 6 and 7) with no lag error. The acceleration constant (K_A) for the converter is 48,000°/sec². Both small and large signal response for the Model 1014 are shown in figure 11.

The ***Large Signal*** transient response is dependent solely on the maximum velocity (ω_{max}) and the maximum acceleration (α_{max}) of which the converter is capable. The large signal parameters are defined in figure 9. The synchronizing time (t_{SYNC}) for large signals can be partitioned into three distinct intervals. Acceleration time (t_{ACC}) Slew time (t_{SLEW}) and Overshoot time (t_{OS}).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The ***Small Signal*** settling time (t_S) is specified for step inputs of less than 1.4 degrees. For small signal steps the settling time is a function of the transient response of the converter. The transfer functions for both 60 Hz and 400 Hz models are shown in figure 10.

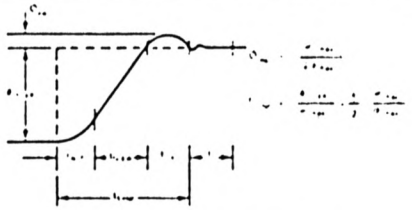


FIGURE 9 Large Signal (>1.4°) Response Parameters

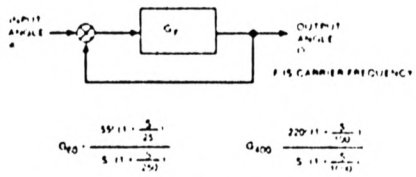


FIGURE 10 Transfer Functions for 1014

Small Signal Input Step = 0.7 Degrees

Large Signal Input Step = 179 Degrees

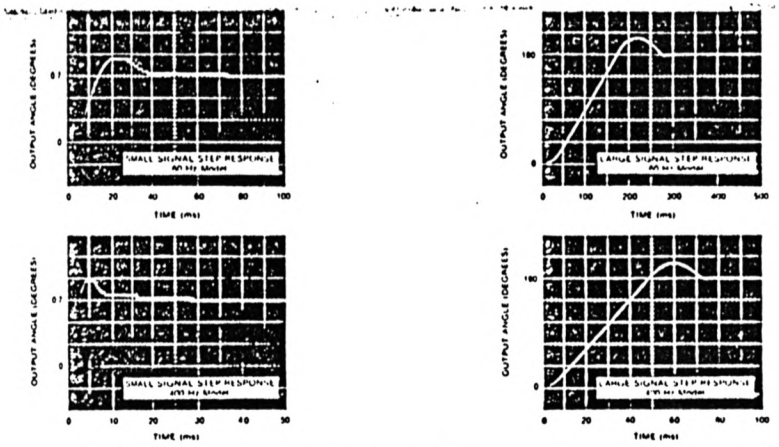


FIGURE 11 Dynamic Characteristics

Specifications

PARAMETER	VALUE		REMARKS
Digital Output Resolution	14-bits (1.32 arc-minutes)		
Accuracy	±5.2 arc-minutes (option S) ±2.6 arc-minutes (option H)		Accuracy applies over operating temperature range range and includes hysteresis
Reference Input			
Voltage	4 to 130 V-rms		
Frequency	360 to 1000 Hz 47 to 1000 Hz		400 Hz Models 60 Hz Models
Input Impedance	200 kΩ Single Ended 400 kΩ Differential		
Common Mode Range	±250 V peak maximum		dc plus recurrent ac peak
Synchro Resolver Inputs			
Input Voltages (Line-to-Line)	11.8 V-rms 26 V-rms 90 V-rms		Accuracy of the converter is maintained with ±10% variation in signal voltages
Input Impedance	Differential	Line-to-GND	
	60 kΩ 150 kΩ 500 kΩ	30 kΩ 75 kΩ 250 kΩ	11.8 V-rms L-L models 26 V-rms L-L models 90 V-rms L-L models
Impedance Unbalance	0.1% maximum		For all models
Common Mode Range	± 30 V peak ± 60 V peak ±180 V peak		11.8 V-rms models 26 V-rms models 90 V-rms models
Common Mode Rejection Ratio	70 dB minimum		dc to 1000 Hz
Harmonic Distortion	10% maximum		Without degradation in accuracy specification
Digital Inputs			CMOS transient protected
Voltage Levels Logic "0" Logic "1"	-0.3 V dc to 0.8 V dc 2.4 V dc		For V_L = 5 V dc
Logic "0" Logic "1"	-0.3 V dc to 0.3 V_L 0.7 V_L to V_L		For V_L = 15 V dc
Input Currents	-15 µA typical "active" pull-up to power supply (V_L)		When not used, may be left unconnected
$\overline{HBE}$, $\overline{LBE}$	15 µA typical "active" pull-down to ground (GND)		When not used may be left unconnected
Digital Input Controls			
$\overline{INH}$	Logic "1" Logic "0"		Digital output follows analog input signals Output data latched in holding register (Does not interrupt converter tracking-loop.)
$\overline{HBE}$	Logic "0" Logic "1"		6 MSBs are enabled 6 MSBs are in high impedance state of 3-state output
$\overline{LBE}$	Logic "0" Logic "1"		8 LSBs are enabled 8 LSBs are in high impedance state of 3-state output
Digital Outputs			
Logic Type	TTL/CMOS compatible		Depends on logic supply voltage (V_L)
Drive Capability			
Data Bits (B1-B14) CB	1 Standard TTL 1 Standard TTL		For 5 V-dc logic supply voltage (V_L)
Data Bits (B1-B14)	Natural Binary Angle		Positive Logic
CB	Logic "0" Logic "1" (2 µsec pulse for every LSB change)		Output angle not changing Output angle changing (Leading edge initiates output change)

PARAMETER	VALUE	REMARKS
Analog Outputs		Typical values unless otherwise specified
V (Bias Voltage)	(+15 V-0.7) ± 2	+7.15 V-dc for +15 V-dc main power supply
-D (Unfiltered Error)	±16 mV-dc per ±1 LSB	dc voltage referenced to V
-E (Buffered Error)	±1 V-dc per ±1 LSB	dc voltage referenced to V
$\dot{\theta}$ (Velocity Output)	0.48 V-dc per rps 1.85 V-dc per rps	400 Hz models 60 Hz models
BS (Buffered Sin θ) -BC (Buffered -Cos θ)	1 V-rms maximum Angular accuracy 1 arc minute	ac voltage referenced to V θ = input shaft angle
Drive Capability	1 mA maximum	All analog outputs
Analog Gain Control (Ge)		Gain programming pin
Gain Control Range	4 to 1	Without degradation of accuracy specification
Dynamic Characteristics		Typical values unless otherwise specified
Maximum Tracking Rate	±10 rps (3600° per sec) minimum ±2 rps (720° per sec) minimum	400 Hz models 60 Hz models
Maximum Acceleration	200,000° sec 15,000° sec	400 Hz models 60 Hz models
Acceleration for 1 LSB error	1,000° sec 65° sec	400 Hz models 60 Hz models
Settling Time to 1 LSB (for 179° step change)	150 msec 500 msec	400 Hz models 60 Hz models
Settling Time to 1 LSB (small signal step ≤ 1.4°)	20 msec 100 msec	400 Hz models 60 Hz models
Power Supplies		
Main Power Supply (+15 V)		
Voltage	11 V-dc to 17 V-dc	Without degradation in accuracy specification
Current	20 mA typical 30 mA maximum	For +15 V-dc power supply
Logic Voltage (V_L)		
Voltage	4.5 V-dc to main power supply	5 V-dc ± 10% for TTL compatible output
Current	1 mA maximum 3 mA maximum	For 5 V-dc logic supply For 15 V-dc logic supply
Physical Characteristics		
Type	36 PIN Double DIP	3 standoffs are added to the package to insulate it from printed circuit board traces (standoffs included in 0.21 inch height dimension)
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm)	
Weight	0.6 oz (17 g) max	

Model 1014 converter uses thin-film resistors (as compared to screened thick-film resistors), thereby allowing flexibility of design changes. Non-standard voltages, frequency, dynamic requirements, etc. can be accomodated with minor modifications, often, without any additional costs.

If your application requires non-standard input or output characteristics, contact a Natel Applications Engineer or sales department.

Pin Designations

+15 V	Main Power Supply - 11 V-dc to 17 V-dc
V_L	Logic Voltage - 5 V-dc (For TTL compatible output) 4.5 V-dc to +15 V supply (For CMOS compatible output)
GND	Power Supply Ground Digital Ground
B1 - B14	Parallel Output Data Bits - B1 is MSB = 180 degrees B14 is LSB = 0.022 degree
S1, S2, S3, S4	Input Analog Signals - Leave S4 unconnected for synchro-input
BS, -BC	Buffered Sinθ and -Cos θ outputs
RH, RL	Reference Voltage Input
TP1, TP2	Test points - (For future expansion to 16-bits) (For factory use only)
Ge	External Gain Control (see text for details)
-D	Unfiltered dc null error - Output is referenced to bias voltage (V) (see text for details)
-E	Amplified, filtered dc null voltage - Output is referenced to bias voltage (V) (see text for details)
$\dot{\theta}$	Velocity Output - dc analog voltage proportional to rotational speed of the input shaft angle Output is referenced to bias voltage (V)
V	Bias Voltage - Internally regulated reference voltage serves as reference ground for all analog outputs.
$\overline{INH}$	Inhibit Function - A logic "low" freezes the digital angular output. Internal loop keeps tracking the analog input. All other outputs keep following the input. For continuous operation this pin may be left unconnected. Internal active pull-up will apply V_L to the pin.

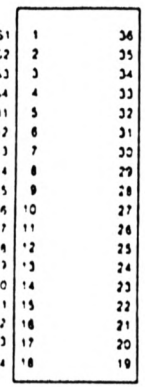


FIGURE 12 HSD1014/HRD1014 Pin Assignment

CB	Converter Busy - A 2µs pulse which occurs during updating of the holding register. Output data can be transferred at the trailing edge of the CB pulse. When converter output is not changing CB is at logic "low."
$\overline{HBE}$	High Byte Enable - Data bits B1 through B6 are enabled (low-impedance state of 3-state output) when $\overline{HBE}$ is set to a logic "low." When $\overline{HBE}$ is set to a logic "high," the data bits B1 through B6 are disabled (high-impedance state of 3-state output).
$\overline{LBE}$	Low Byte Enable - Data bits B7 through B14 are enabled when $\overline{LBE}$ is set to a logic "low." When $\overline{LBE}$ is set to a logic "high," the data bits B7 through B14 are disabled.
Note:	For continuous 14-bit parallel output $\overline{HBE}$ and $\overline{LBE}$ may be left open. Internal active pulldown to ground will apply logic "low" to these pins thus enabling all data bits B1 through B14.

Absolute Maximum Ratings

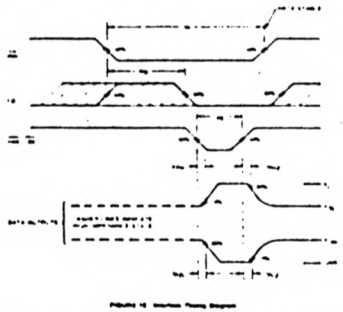
Signal Inputs ..... Twice Normal Voltage
Reference Input ..... 200 V-rms
Main Power Supply (+15 V) ..... +18 V-dc
Logic Voltage (V_L) ..... +4.5 V-dc to +15 V supply
Digital Inputs ..... -0.3 V-dc to V_L
Storage Temperature ..... -65°C to +135°C

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supplies and input signals be turned off. Decoupling capacitors are recommended on the main power supply (+15 V) as well as logic voltage (V_L). A 1 µF tantalum capacitor in parallel with 0.01 µF ceramic capacitor should be mounted as close to the supply pins (32 and 28) as possible.

Dynamic Electrical Characteristics

T_A = 25°C R_L = 200 kΩ Input t_r, t_f = 20 ns V_L = 5 V-dc C_L = 50 pF

CHARACTERISTIC	LIMITS			UNITS
	MIN	TYP	MAX	
[illegible] PULSE WIDTH t_{PA}	3	–	–	µs
BUSY PULSE WIDTH t_{PB}	1	2	4	µs
ENABLE PULSE WIDTH t_{PE} (HBE OR LBE)	400	–	–	ns
HIGH Z TO LOGIC '1' t_{PZH}	–	150	220	ns
HIGH Z TO LOGIC '0' t_{PZL}	–	200	300	ns
LOGIC '1' TO HIGH Z t_{PHZ}	–	150	220	ns
LOGIC '0' TO HIGH Z t_{PLZ}	–	200	300	ns
TRANSITION TIMES				
LOW TO HIGH t_{TLH}	–	250	375	ns
HIGH TO LOW t_{THL}	–	50	75	ns
INPUT CAPACITANCE C_{IN} (ANY INPUT)	–	5	7.5	pF



Analog Outputs

The outputs of the signal conditioner . . . resistive scott-tee for synchro-input and differential attenuator for resolver input . . . are the sine and cosine of the input shaft angle, θ. In the converter the sine and cosine outputs of signal conditioner are processed to obtain digital output. These outputs are also brought out on pin 35 (BS) and pin 36 (-BC) as buffered sine and cosine outputs. Nominal voltage for sine maximum and cosine maximum is 1 V-rms referred to bias voltage V (pin 34) . . . the internal analog ground. The ratio accuracy of sine and cosine outputs is better than 1 arc-minute.

Other analog outputs available from the 1014 converters are

-D ..... unfiltered dc error (pin 27)
-E ..... filtered dc error (pin 22)
$\dot{\theta}$ ..... velocity output (pin 23)

and are referenced to bias voltage (V)

The bias voltage V_B is equal to ½ (+15 V-0.7). For main power supply voltage of +15 V-dc, the bias voltage is 7.15 V-dc

-D is an unfiltered dc voltage proportional to error voltage sin (θ-ϕ), where θ is input angle and ϕ is the digital output angle. -16 mV-dc error voltage corresponds to an error of +1 LSB (0.022 degree).

-E is filtered dc voltage proportional to (θ-ϕ). A -1 V-dc voltage corresponds to an error of +1 LSB (0.022 degree).

$\dot{\theta}$ is a dc voltage proportional to the velocity of the input shaft angle (and output digital angle). The voltage goes positive for increasing digital angle and goes negative for decreasing digital angle. A +1 V-dc signal corresponds to +2 1 rps for 400 Hz models and +0 54 rps for 60 Hz models

Scaling of all analog outputs is independent of main-power supply voltage between 11 V-dc and 17 V-dc. Also all analog outputs are operational amplifier outputs and have a drive capability of 1 mA

The analog outputs -D, -E and $\dot{\theta}$ are by-products of the technique used in mechanizing the conversion process and are made available. They are not closely controlled or characterized functions

If a bipolar signal is required for any analog output a difference circuit, as shown in figure 14, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed

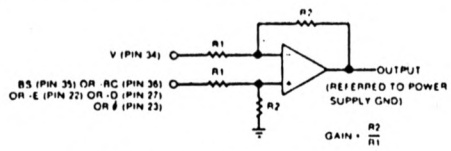


FIGURE 14 Difference Circuit for Bipolar Analog Outputs

Other Synchro Converters/Products Available from NATEL

- Two-speed logic combiner with 20-bit, 3-state output, in a 1.3 x 2.6 x .35 inch size (TSL1x36)
- 14 and 16-bit Digital to Synchro/Resolver converters, with internal power amplifiers (5012, 5112, 5116)
- High power Synchro/Resolver Drivers
- 10 to 20-bit single-speed Synchro-to-Digital converters
- Hybrid synchro converters - see page 12
- Low profile Digital-to-Synchro/Resolver converters
- Two-speed Synchro (Resolver)-to-Digital converters with 16 and 20-bit resolutions in a single package. (Models 2SD402 and 2SD412).
- Solid State control transformers (SSCT) and differential transmitters (SCDX).
- Angle position indicators and synchro instrumentation for one-speed and multi-speed applications.

Burn-in Circuit

As a standard practice all Natel hybrid synchro converters go through a power burn-in for 168 hours at maximum operating temperature. Although customer specifications in some cases, may not require it, we at Natel have found active power burn-in well worth the expense. Added initial costs save field failures and much higher system failure costs.

A burn-in circuit for Synchro (Resolver)-to-Digital Converter Model 1014 is shown in figure 15. An ac source provides the excitation voltage for the synchro (resolver) as well as a reference voltage for the 1014 converter. The frequency and voltage of the ac source are determined by the options of the unit under burn-in. A synchro (resolver) or a synchro (resolver) simulator e.g., a digital-to-synchro (resolver) converter may be used for signal input. To exercise a random digital pattern the synchro or synchro simulator may be rotated to apply a changing input shaft angle. Input S4 is left unconnected for synchro input models. The main power supply is set at +15 V-dc and the logic supply may be set at 5 V-dc or 15 V-dc. TP1, TP2 and Go are left unconnected. Control functions INH, LBE and HBE are randomly connected to GND or V_L. Analog outputs are connected to a 1 mA load. Data bits B1 - B14 and CB output are connected to 1 TTL load or left unconnected, depending on V_L.

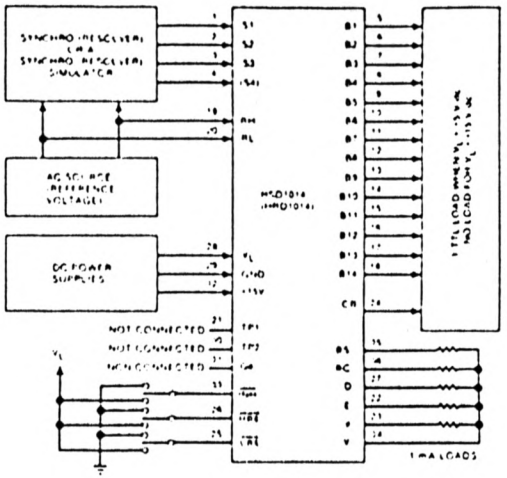


FIGURE 15 Burn-in Circuit

Testing Synchro (Resolver)-to-Digital Converters

All Model 1014 converters are guaranteed to meet the specifications described in the data sheet. All converters are 100% tested for their specifications (except for design parameters) at the factory. A copy of the data sheet with a record of the accuracy test is supplied with each unit.

Figure 16 shows a convenient test set-up for checking the static accuracy of the converter at incoming inspection. The synchro (resolver) input is set to "test angles." The output is monitored on a 6-digit numerical readout and compared with the standard angles for their accuracy.

Equipment described in figure 16 or equivalent may be used for testing. Synchro (Resolver) standard or simulator used must have an accuracy of at least 5 times (preferably 10 times) better than the unit under test. If the required equipment is not available arrangements may be made with Natel for source inspection at our facilities.

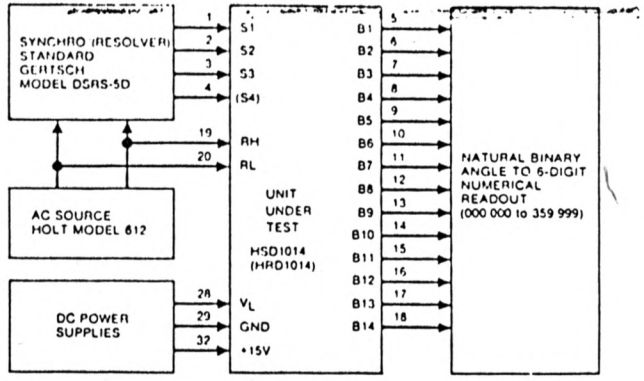
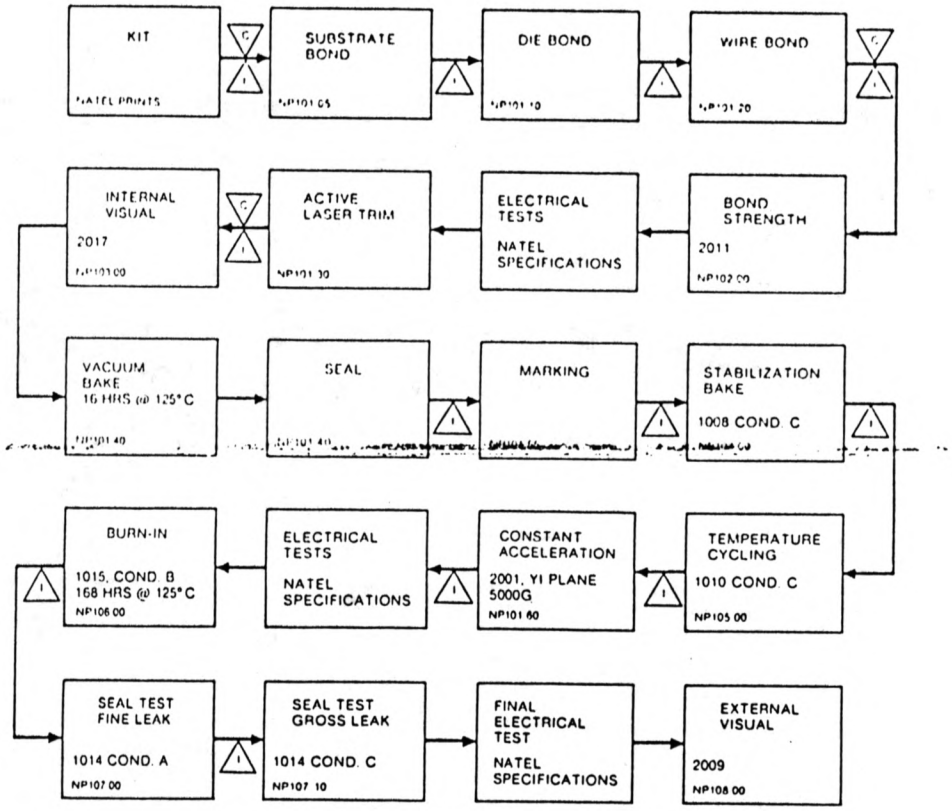


FIGURE 16 Static Accuracy Test Configuration

Hybrid Converter Assembly and Testing

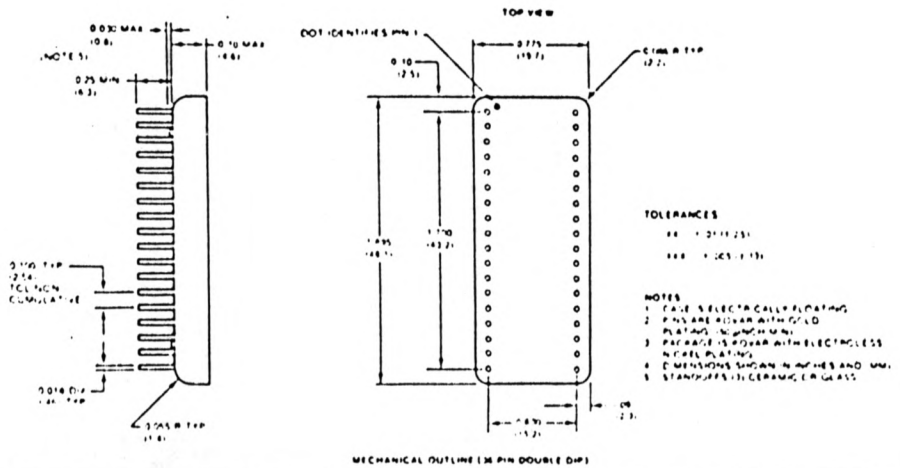
As a standard practice all Natel hybrid synchro converters are manufactured in accordance with the requirements of MIL-STD-883B method 5008. All active semiconductors and integrated circuit chips are 100% electrically probed at the vendor. All passive components used are established reliability (ER) type. Incoming inspection is per method 2010 of MIL-STD-883B. In addition, Natel may perform sample tests at incoming inspection to verify device performance. A hybrid assembly / test flow chart is shown in figure 17. Additional tests may be performed to assure long-term performance of converters.

All hybrid synchro converters have a traceability record to component level on a lot basis (lot consists of 20 or less converters). During manufacturing all work-in process and components are stored in controlled environment (dry boxes). All assembly and testing before sealing is performed in a class 100,000 clean-room. Each bonding machine/operator is evaluated at the start of every 4 hour shift by performing destructive pull-test on at least 10 wires consisting of chip to substrate bond, per paragraph 3.4.2 of method 5008. Final electrical tests are performed at room temperature as well as minimum and maximum operating temperatures.



C = CLEAN IF REQUIRED I = INSPECTION

FIGURE 17 Hybrid Assembly / Test Flow Chart



MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HSD1014 - T F I A

Temperature Range
1 = 0° C to +70° C
2 = -25° C to +85° C
3 = -55° C to +125° C

Frequency Range
4 = 360 Hz to 1000 Hz
6 = 47 Hz to 1000 Hz

Input Signal
1 = 11.8 V rms
2 = 26 V rms
9 = 90 V rms
0 = Ext. Signal at VIN/S
5 = Ext. Signal and Reference at VIN/S

Accuracy
S = ±5.2 arc minutes
H = ±2.6 arc minutes

SPECIFY HRD1014 FOR RESOLVER INPUT

As a standard practice, all converters are built in accordance with the requirements of MIL-STD-883B, including 168 hours of active burn-in.

Other Hybrid products in 36 pin DDIP size:

- 16-bit microprocessor-compatible synchro/resolver-to-digital converter, with 3 state output, operating from a single +5-V power supply (HSRD1006)
- 16-bit microprocessor-compatible digital to synchro/resolver converter with double buffered inputs and 1 arc-minute accuracy (HDSR2006)
- 14-bit digital-to-synchro/resolver converter that is pin-compatible with existing designs with transformation and angular accuracy improvement of a factor of 2 to 4 (HDSR2504)
- 10-bit synchro (resolver)-to-digital converters that are pin compatible with existing designs (HSD/HRD1510)
- 14/16-bit synchro (resolver) control transformer with 1 arc minute accuracy (HSCT/HRCT3006) ——— 10/81

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

Natel Engineering Co., Inc.
8954 Mason Ave.
Canoga Park, CA 91306 (USA)

Natel Hybrid Division
21602 Marilla Ave.
Chatsworth, CA 91311 (USA)

Phone: (213) 882-9620 • TWX: 910-494-1959

ANALOG DEVICES

High-Speed 12-Bit Monolithic D/A Converters

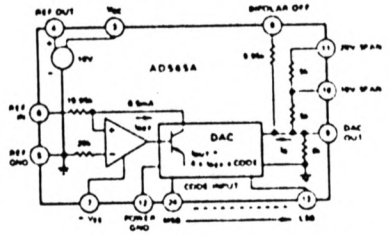
AD565A*/AD566A*

2

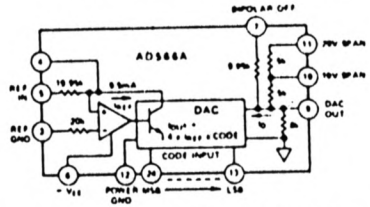
FEATURES

- Single Chip Construction
- Very High-Speed Settling to 1/2LSB
  - AD565A: 250ns max
  - AD566A: 350ns max
- Full-Scale Switching Time: 30ns
- Guaranteed for Operation with ±12V Supplies: AD565A with -12V Supply: AD566A
- Linearity Guaranteed Over Temperature: 1/2LSB max (K, T Grades)
- Monotonicity Guaranteed Over Temperature
- Low Power: AD566A = 180mW max; AD565A = 225mW max
- Use with On-Board High-Stability Reference (AD565A) or with External Reference (AD566A)
- Low Cost

AD565A FUNCTIONAL BLOCK DIAGRAM



AD566A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD565A and AD566A are fast 12-bit digital-to-analog converters which incorporate the latest advances in analog circuit design to achieve high speeds at low cost.

The AD565A and AD566A use 12 precision, high-speed bipolar current-steering switches, control amplifier and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The AD565A also includes a buried zener reference that features low-noise, long-term stability and temperature drift characteristics comparable to the best discrete reference diodes.

The combination of performance and flexibility in the AD565A and AD566A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565A and AD566A have a 10-90% full-scale transition time less than 35ns and settle to within ±1/2LSB in 250ns max (350ns for AD566A). Both are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD565A and AD566A the ideal choice for high-speed display drivers as well as fast analog-to-digital converters.

The laser trimming process which provides the excellent linearity is also used to trim both the absolute value and the temperature coefficient of the reference of the AD565A resulting in a typical full-scale gain TC of 10 ppm/°C. When tighter TC performance is required or when a system reference is available, the AD566A may be used with an external reference.

AD565A and AD566A are available in four performance grades. The J and K are specified for use over the 0 to +70°C temperature range while the S and T grades are specified for the -55°C to +125°C range. All are packaged in a 24-pin, hermetically sealed, ceramic, dual-in-line package.

PRODUCT HIGHLIGHTS

1. The wide output compliance range of the AD565A and AD566A are ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The devices incorporate a newly developed, fully differential, nonsaturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562/3 with very fast switching times and an optimally-damped settling characteristic.
3. The devices also contain SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, unless otherwise specified)

MODEL	AD565AJ MIN	AD565AJ TYP	AD565AJ MAX	AD565AK MIN	AD565AK TYP	AD565AK MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	µA
Bit OFF Logic "0"		+35	+100		+35	+100	µA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	1.0.8	1.1.0	1.1.2	1.0.8	1.1.0	1.1.2	mA
Resistance (exclusive of span resistor)	8k	8k	10k	8k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (adjustable to zero)			0.15		0.05	0.1	% of F.S. Range
Drift		15			25		ppm/°C
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (with internal reference)							
Unadjusted +25°C		±1.4 (0.11%)	±1.2 (0.012)		±1.8 (0.11%)	±1.4 (0.088)	LSB % of F.S. Range
T_{min} to T_{max}		±1.2 (0.012)	±1.4 (0.018)		±1.4 (0.088)	±1.2 (0.012)	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1.2	±1.4		±1.4	±1.2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS (with Internal Reference)							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON or OFF or OFF to ON		250	400		250	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		10	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}: +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}: -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE (see Figures 2, 3, 4)		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

NOTES

[1] The digital inputs are guaranteed but not tested over the operating temperature range.

[2] The power supply gain sensitivity is tested as referenced to a V_{CC}, V_{EE} of ±15V dc.

[3] For operation at elevated temperatures the reference current supply current for external loads is, therefore, should be buffered if additional loads are to be supplied

Specifications subject to change without notice.

MODEL	AD565AS MIN	AD565AS TYP	AD565AS MAX	AD565AT MIN	AD565AT TYP	AD565AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	µA
Bit OFF Logic "0"		+15	+100		+15	+100	µA
RESOLUTION		12			12		Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	8k	8k	10k	8k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S. Range
T_{min} to T_{max}		±1/2 (0.012)	±1/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±1/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	15	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB All Bits ON to OFF or OFF to ON		250	400		250	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (see Figures 2, 3, 4)		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications shown in boldface are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

SPECIFICATIONS (T_A = +25°C, V_{EE} = -15V, unless otherwise specified)

MODEL	AD566AJ MIN	AD566AJ TYP	AD566AJ MAX	AD566AR MIN	AD566AR TYP	AD566AR MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	µA
Bit OFF Logic "0"		+15	+100		+15	+100	µA
RESOLUTION		12			12		Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	8k	8k	10k	8k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S.R.
T_{min} to T_{max}		±1/2 (0.012)	±1/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of F.S.R.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±1/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB All Bits ON to OFF or OFF to ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE (see Figures 3, 4, 5)		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)

Quadrants	Two (2) Bipolar Operation or Digital Input Only
Reference Voltage	+3V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sine wave frequency for 1/2LSB [p-p] feedthrough)	40k Hz typ
Output Slew Rate 10%-90%	3mA/µs
90%-10%	3mA/µs
Output Settling Time (all bits on and a 0-10V step change in reference voltage)	1.5µs to 0.01% F.S.
CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

NOTES
[1] The digital input levels are guaranteed but not tested over the temperature range.
[2] The power supply gain sensitivity is tested in reference to a V_{EE} of -15V dc.
Specifications subject to change without notice.

MODEL	AD566AS MIN	AD566AS TYP	AD566AS MAX	AD566AT MIN	AD566AT TYP	AD566AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4, R_2 and R_3 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S.R.
T_{min} to T_{max}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % of F.S.R.
DIFFERENTIAL NONLINEARITY +25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB All Bits On to OFF or OFF to ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION 10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS V_{EE} -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2] V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S.%
PROGRAMMABLE OUTPUT RANGE (see Figures 1, 4, 5)		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%-90%	5mA/μs
90%-10%	1mA/μs
Output Settling Time (all bits on and a 0-10V step change in reference voltage)	1.5μs to 0.01% F.S.
CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small Signal Closed-Loop Bandwidth	1.8MHz

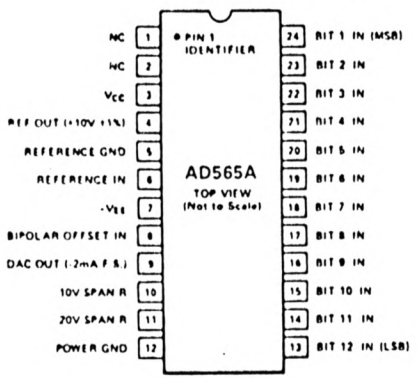
Specifications subject to change without notice.

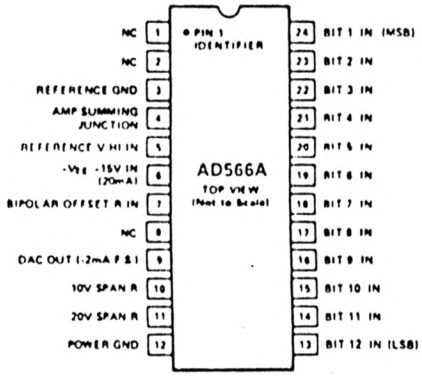
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . . 0V to +18V
V_{RR} to Power Ground (AD565A) . . . . . 0V to -18V
Voltage on DAC Output (Pin 9) . . . . . -3V to +12V
Digital Inputs (Pins 13 to 24) to
Power Ground . . . . . -1.0V to +7.0V
Ref in to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref out (AD565A) . . . . . Indefinite Short to Power Ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

PIN DESIGNATIONS





AD565A ORDERING GUIDE

Model	Package Option*	Temp. Range	Linearity Error Max @ 25°C	Max Gain T.C. (ppm of F.S./°C)
AD565AJD/BIN	Ceramic (D-24)	0 to +70°C	±1/2LSB	50
AD565AKD/BIN	Ceramic (D-24)	0 to +70°C	±1/4LSB	20
AD565ASD/BIN	Ceramic (D-24)	-55°C to +125°C	±1/2LSB	30
AD565ATD/BIN	Ceramic (D-24)	-55°C to 1125°C	±1/4LSB	15

*See Section 14 for package outline information.

AD566A ORDERING GUIDE

Model	Package Option*	Temp. Range	Linearity Error Max @ +25°C	Max Gain T.C. (ppm of F.S./°C)
AD566AJD/BIN	Ceramic (D-24)	0 to +70°C	±1/2LSB	10
AD566AKD/BIN	Ceramic (D-24)	0 to +70°C	±1/4LSB	3
AD566ASD/BIN	Ceramic (D-24)	-55°C to +125°C	±1/2LSB	10
AD566ATD/BIN	Ceramic (D-24)	-55°C to +125°C	±1/4LSB	3

*See Section 14 for package outline information.

GROUNDING RULES

The AD565A and AD566A bring out separate reference and power grounds to allow optimum connections for low noise and high-speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

CONNECTING THE AD565A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 1. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 2. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 3. OTHER VOLTAGE RANGES

The AD565A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 3.

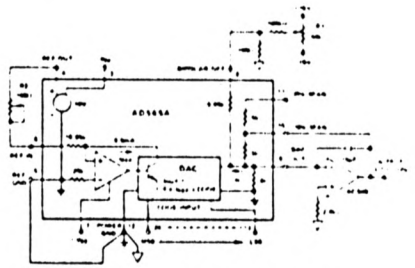


Figure 1. 0 to +10V Unipolar Voltage Output

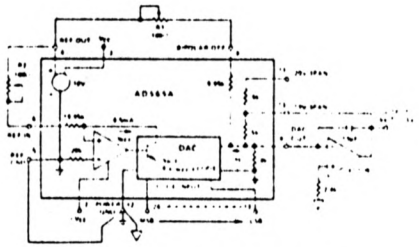


Figure 2. ±5V Bipolar Voltage Output

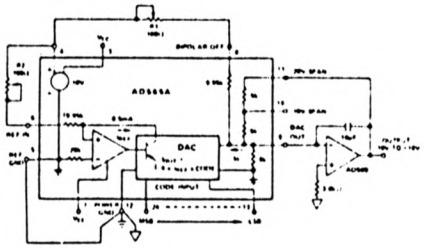


Figure 3. ±10V Voltage Output

CONNECTING THE AD566A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 4. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 5. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 output volts.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 6. OTHER VOLTAGE RANGES

The AD566A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF} for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 6.

DIGITAL INPUT		ANALOG OUTPUT		
MSB	LSB	Straight Binary	Offset Binary	Two's Compl.*
000000000000		Zero	-Full Scale	Zero
011111111111		Mid Scale -1LSB	Zero -1LSB	+5 -1LSB
100000000000		+1/2 FS	Zero	-5
111111111111		+FS -1LSB	+ Full Scale -1LSB	Zero -1LSB

*Invert the MSB of the offset binary code with an external inverter to obtain two's compl.

Table I. Digital Input Codes

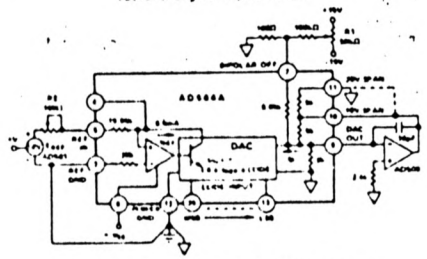


Figure 4. 0 to +10V Unipolar Voltage Output

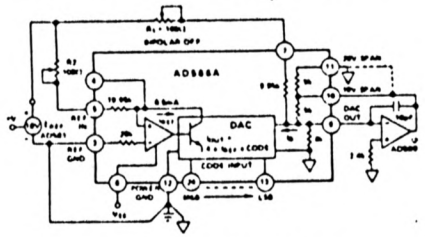


Figure 5. ±5V Bipolar Voltage Output

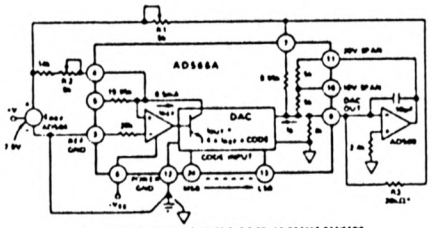


Figure 6. ±10V Voltage Output

intel

8755A/8755A-2
16,384-BIT EPROM WITH I/O

- 2048 Words × 8 Bits
- Single +5V Power Supply (V_{CC})
- Directly Compatible with 8085A and 8088 Microprocessors
- U.V. Erasable and Electrically Reprogrammable
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40-Pin DIP

The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the 8085A and 8088 microprocessor systems. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

The 8755A-2 is a high speed selected version of the 8755A compatible with the 5 MHz 8085A-2 and the full speed 5 MHz 8088.

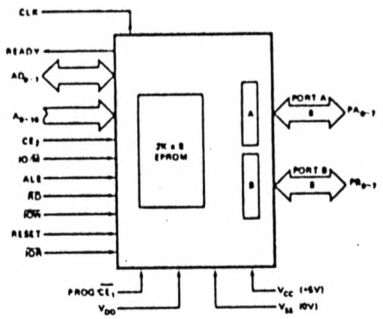


Figure 1. Block Diagram

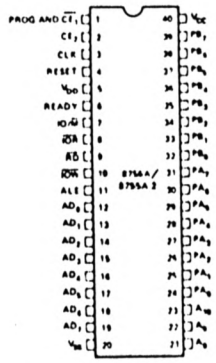


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
ALE	I	**Address Latch Enable:** When Address Latch Enable goes *high*, AD_{0-7}, IO/M, A_{8-10}, CE_2, and $\overline{CE_1}$ enter the address latches. The signals (AD, IO/M, A_{8-10}, CE) are latched in at the trailing edge of ALE
AD_{0-7}	I	**Bidirectional Address/Data Bus:** The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0 if $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	I	**Address:** These are the high order bits of the PROM address. They do not affect I/O operations.
PROG $\overline{CE_1}$ CE_2	I	**Chip Enable Inputs:** $\overline{CE_1}$ is active low and CE_2 is active high. The 8755A can be accessed only when *both* Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high impedance state. $\overline{CE_1}$ is also used as a programming pin. (See section on programming.)
IO/$\overline{M}$	I	**I/O Memory:** If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.
$\overline{RD}$	I	**Read:** If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected PROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-stated.
$\overline{IOW}$	I	**I/O Write:** If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.
CLK	I	**Clock:** The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE_1}$ low, CE_2 high, and ALE high.

Symbol	Type	Name and Function
READY	O	**Ready** is a 3-state output controlled by CE_2, $\overline{CE_1}$, ALE and CLK. READY is forced low when the Chip Enables are actove during the time ALE is high, and remains low until the rising edge of the next CLK. (See Figure 8.)
PA_{0-7}	I/O	**Port A:** These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0, AD_1. Read Operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 and AD_1 low or IO/$\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 and AD_1 low.
PB_{0-7}	I/O	**Port B:** This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0 and a 0 from AD_1.
RESET	I	**Reset:** In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$\overline{IOR}$	I	**I/O Read:** When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1").
V_{CC}		**Power:** +5 volt supply
V_{SS}		**Ground:** Reference.
V_{DD}		**Power Supply:** V_{DD} is a programming voltage, and must be tied to V_{CC} when the 8755A is being read. For programming, a high voltage is supplied with V_{DD} = 25V, typical. (See section on programming.)

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FUNCTIONAL DESCRIPTION

PROM Section

The 8755A contains an 8-bit address latch which allows it to interface directly to MCS-48, MCS-85 and iAPX 88/10 Microcomputers without additional hardware.

The PROM section of the chip is addressed by the 11-bit address and CE. The address, $\overline{CE}_1$ and CE_2 are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the PROM location addressed by the latched address are put out on the AD_{0-7} lines (provided that V_{DD} is tied to V_{CC}).

I/O Section

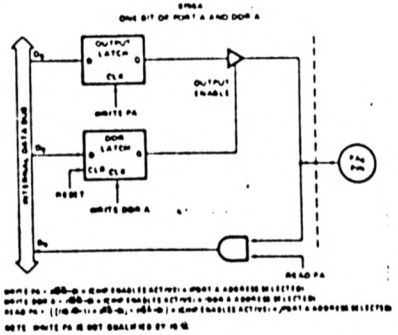
The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers (DDR) in 8755A determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the 8755A are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR's cannot be read.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD is written into I/O port selected by the latched value of AD_{0-1}. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high. (glitch free output)

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O Ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.



Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the Output Latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

TABLE 1. 8755A PROGRAMMING MODULE CROSS REFERENCE

MODULE NAME	USE WITH
UPP 955	UPP(4)
UPP UP2(2)	UPP 855
PROMPT 975	PROMPT 80/85(3)
PROMPT 475	PROMPT 48(1)

NOTES:
1. Described on p. 13-34 of 1978 Data Catalog.
2. Special adaptor socket.
3. Described on p. 13-39 of 1978 Data Catalog.
4. Described on p. 13-71 of 1978 Data Catalog.

ERASURE CHARACTERISTICS

The erasure characteristics of the 8755A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8755A in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755 window to prevent unintentional erasure.

The recommended erasure procedure for the 8755A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm² power rating. The 8755A should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

PROGRAMMING

Initially, and after each erasure, all bits of the EPROM portions of the 8755A are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 8755A can be programmed on the Intel® Universal PROM Programmer (UPP), and the PROMPT™ 80/85 and PROMPT-48™ design aids. The appropriate programming modules and adapters for use in programming both 8755A's and 8755's are shown in Table 1.

The program mode itself consists of programming a single address at a time, giving a single 50 msec pulse for every address. Generally, it is desirable to have a verify cycle after a program cycle for the same address as shown in the attached timing diagram. In the verify cycle (i.e., normal memory read cycle) V_{DD} should be at +5V.

Preliminary timing diagrams and parameter values pertaining to the 8755A programming operation are contained in Figure 7.

SYSTEM APPLICATIONS

System Interface with 8085A and 8088

A system using the 8755A can use either one of the two I/O interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE_2 and $\overline{CE}_1$. By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the 8085A system can use up to 5 each 8755A's without requiring a CE decoder. See Figure 2a and 2b.

If a memory mapped I/O approach is used the 8755A will be selected by the combination of both the Chip Enables and IO/$\overline{M}$ using the AD_{8-15} address lines. See Figure 1.

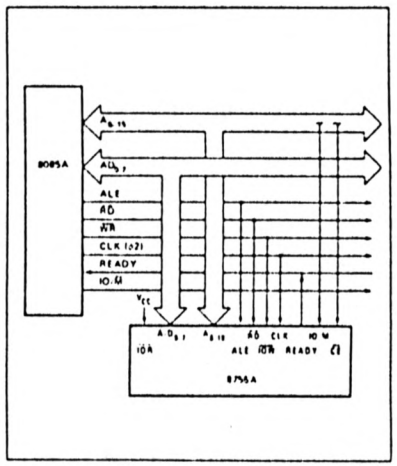


Figure 3. 8755A In 8085A System (Memory-Mapped I/O)

iAPX 88 FIVE CHIP SYSTEM

Figure 4 shows a five chip system containing:

- 1.25K Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 2 Interrupt Levels

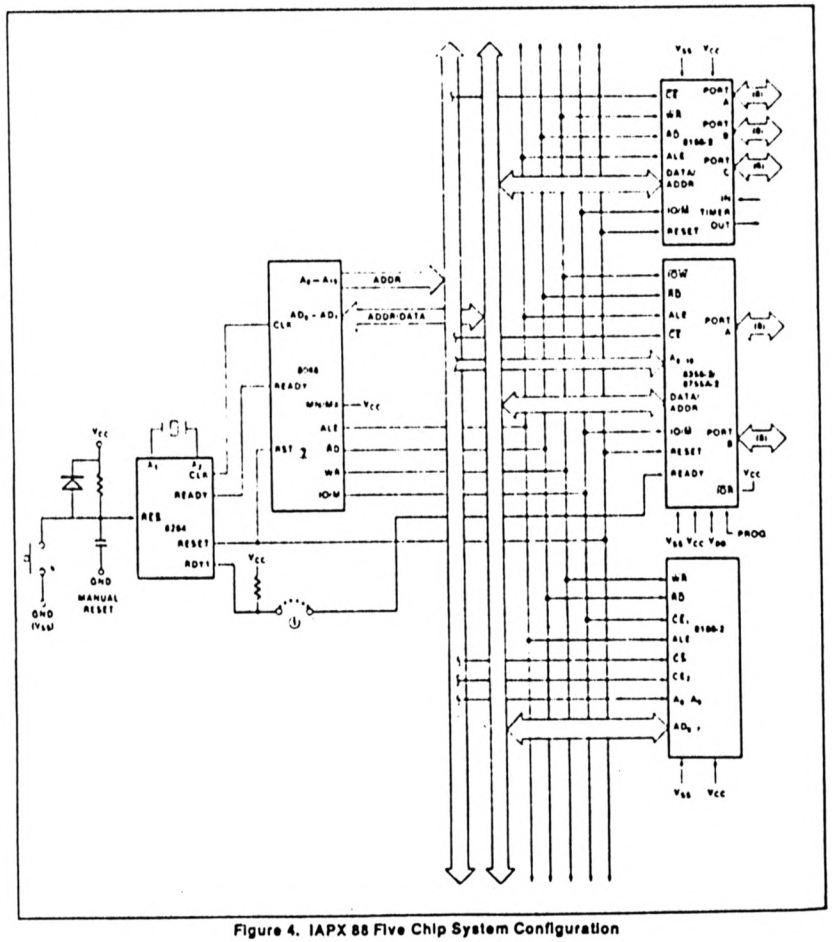


Figure 4. iAPX 88 Five Chip System Configuration

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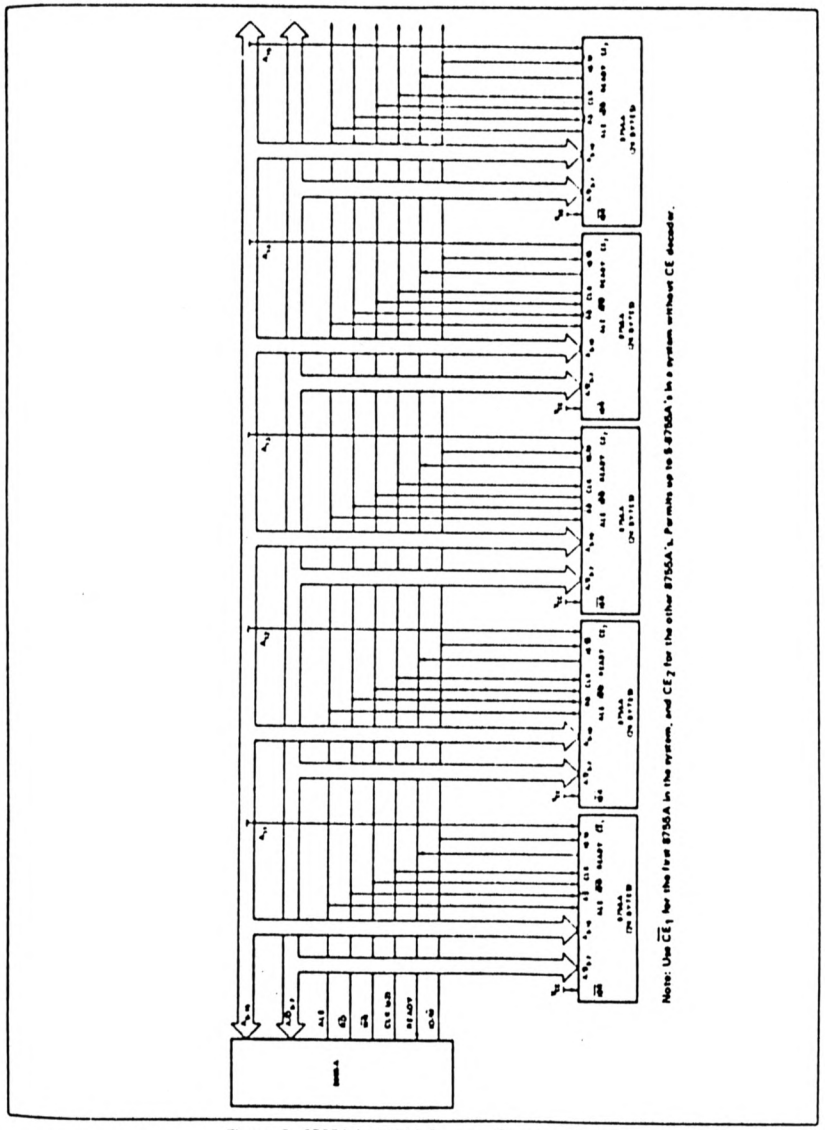


Figure 5. 8755A In 8085A System (Standard I/O)

AFN-01841B

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5W

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°, V_{CC} = V_{DD} = 5V ± 5%; V_{CC} = V_{DD} = 5V ± 10% for 8755A-2)

SYMBOL	PARAMETER	MIN	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	V_{CC} = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$V_{SS} \leq 0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	V_{CC} Supply Current		180	mA	
I_{DD}	V_{DD} Supply Current		30	mA	V_{DD} = V_{CC}
C_{IN}	Capacitance of Input Buffer		10	pF	f_C = 1μHz
$C_{I/O}$	Capacitance of I/O Buffer		15	pF	f_C = 1μHz

D.C. CHARACTERISTICS — PROGRAMMING (T_A = 0°C to 70°, V_{CC} = 5V ± 5%, V_{SS} = 0V, V_{DD} = 25V ± 1V; V_{CC} = V_{DD} = 5V ± 10% for 8755A-2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Programming Voltage (during Write to EPROM)	24	25	26	V
I_{DD}	Prog Supply Current		15	30	mA

intel 8755A/8755A-2

A.C. CHARACTERISTICS (T_A = 0°C to 70°, V_{CC} = 5V ± 5%, V_{CC} = V_{DD} = 5V ±10% for 8755A-2)

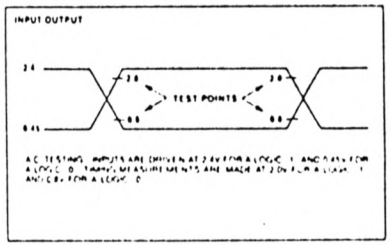
Symbol	Parameter	8755A		8755A-2 (Preliminary)		Units
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	320		200		ns
T_1	CLK Pulse Width	80		40		ns
T_2	CLK Pulse Width	120		70		ns
t_{r}, t_{f}	CLK Rise and Fall Time		30		30	ns
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		45		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170*		140*	ns
t_{AD}	Address Stable to Data Out Valid		450		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float after READ	0	100	0	85	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to Write Set Up Time	150		150		ns
t_{WD}	Data In Hold Time After WRITE	30		10		ns
t_{WP}	WRITE to Port Output		400		300	ns
t_{PR}	Port Input Set Up Time	50		50		ns
t_{RP}	Port Input Hold Time to Control	50		50		ns
t_{RYH}	READY HOLD Time to Control	0	160	0	160	ns
t_{ARY}	ADDRESS CE to READY		160		160	ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{RDE}	READ Control to Data Bus Enable	10		10		ns
t_{LD}	ALE to Data Out Valid		350		270	ns

NOTE:
C_{LOAD} = 150pF.
*Or T_{AD} = (T_{AL} + T_{LC}), whichever is greater.

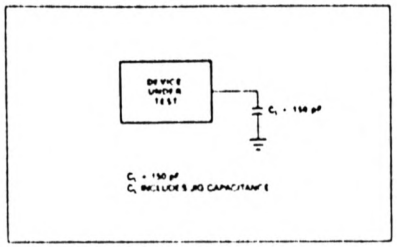
A.C. CHARACTERISTICS — PROGRAMMING (T_A = 0°C to 70°, V_{CC} = 5V ± 5%, V_{SS} = 0V, V_{DD} = 25V ± 1V; V_{CC} = V_{DD} = 5V ± 10% for 8755A-2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{DS}	Data Setup Time	10			ns
t_{DH}	Data Hold Time	0			ns
t_S	Prog Pulse Setup Time	2			μs
t_H	Prog Pulse Hold Time	2			μs
t_{PR}	Prog Pulse Rise Time	0.01	2		μs
t_{PF}	Prog Pulse Fall Time	0.01	2		μs
t_{PRG}	Prog Pulse Width	45	50		msec

A.C. TESTING INPUT, OUTPUT WAVEFORM

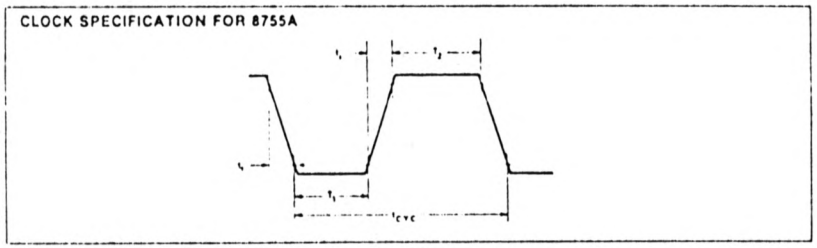


A.C. TESTING LOAD CIRCUIT

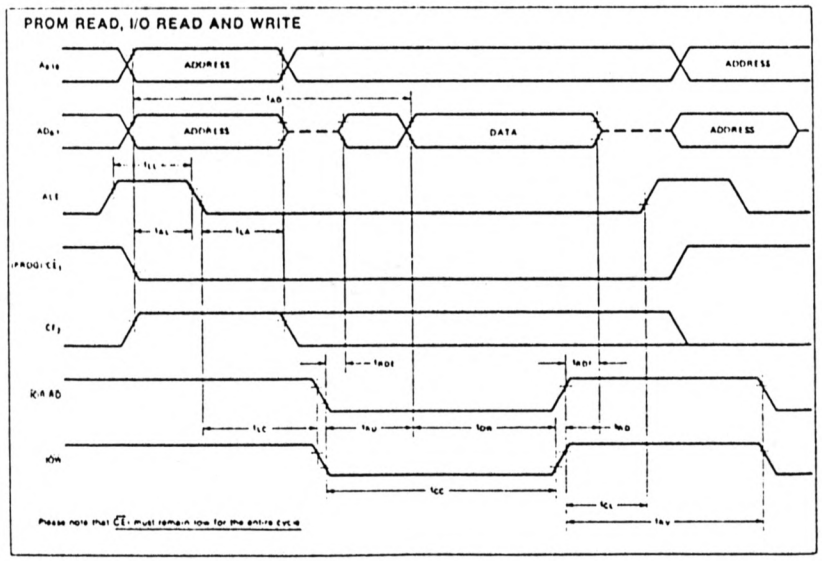


WAVEFORMS

CLOCK SPECIFICATION FOR 8755A



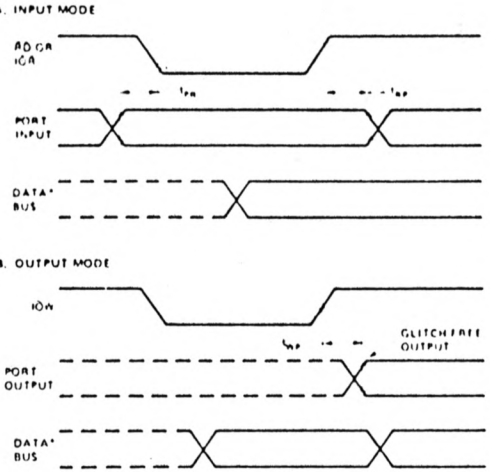
PROM READ, I/O READ AND WRITE



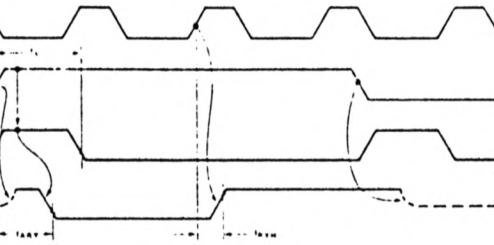
Please note that $\overline{CE}_1$ must remain low for the entire cycle

WAVEFORMS (Continued)

I/O PORT

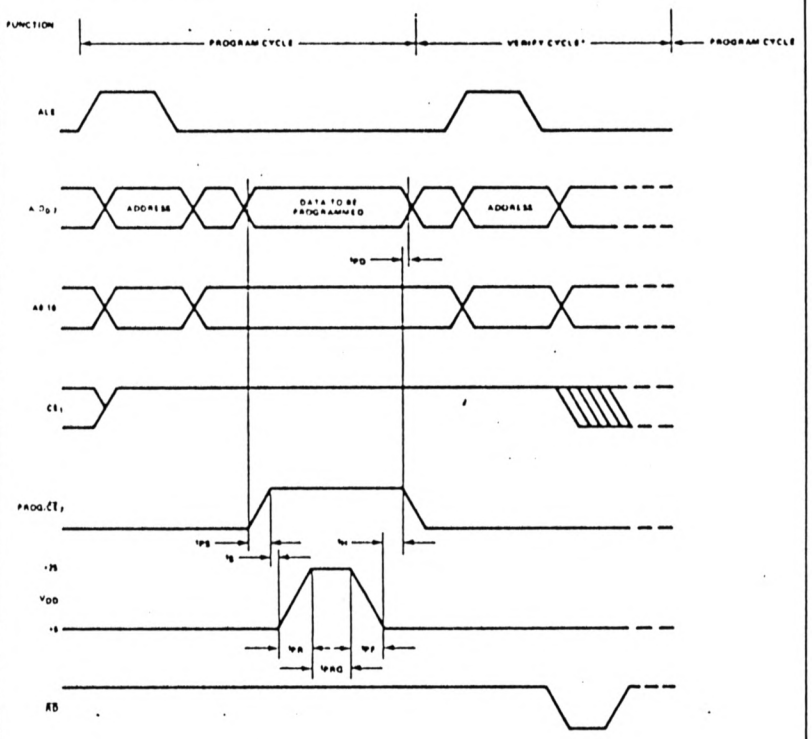


WAIT STATE (READY = 0)



WAVEFORMS (Continued)

8755A PROGRAM MODE



*VERIFY CYCLE IS A REGULAR MEMORY READ CYCLE (WITH V_{DD} = +5V FOR 8755A)

Installation and Service Manual

BDS3-208 AND BDS3-230 SERIES
Brushless Motor Controller

M-8507 ISSUE 8

NOTICE:

Upon receipt of the amplifier, closely inspect the components to ensure that no damage has occurred in shipment. If damage has occurred, notify the appropriate carrier at once.

> CAUTION:
>
> Dangerous voltages exist in this equipment. Do not attempt connecting or probing in this equipment with power on.
>
> Should any question arise regarding any step outlined in this manual please call the factory.

This product may be covered by one or more of the following U.S. Patents: 4447771, 4479078, 4490661 other (including foreign) patents pending.

INDUSTRIAL DRIVES
A
KOLLMORGEN
DIVISION
Radford, Virginia 24141
(703) 639-2495

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PREFACE

This Installation and Service Manual is a general document and is applicable to the entire BDS3 series product line. However, since these motor controllers are interfaced with motors of varying sizes having different operating characteristics such as internal resistance, inductance, rotor inertia, etc., the complete model number of these amplifiers will vary more or less with the motors they are made compatible with. Thus, after the BDS3 and a particular motor are connected together to form a complete Velocity Loop, the model number applied to the BDS3 nameplate may be understood to be the basic model number for the Velocity Loop; consisting of (1) BDS3, (2) PSR3, (3) motor, and (4) transformer. However, the PSR3 Main Bus power supply, the motor, and the transformer; will have nameplates bearing their specific Model Numbers.

The Test Limits and Modification Sheet (TL) is a specific document and is applicable only to individual systems. The TL Sheet contains such information as maximum operating speed, peak current limits, and the component compensation values which make the amplifier motor combination compatible. The compensation components are located on the compensation board. (See Figure 12) In addition, the microprocessor program will change from motor to motor. The proper microprocessor is also indicated by the TL Sheet. (See Figure 11)

With exception to the Comp Board, Microprocessor and continuous current rating, the brushless BDS3 motor controllers are identical. Options may be added by way of option board OPT 1, OPT2, OPT3, etc. Versatility can be enhanced by the addition of various OPTION BOARDS.

MODEL NUMBER SCHEME

Example: BDS3-208/20-01-100-4501AXX
A B C D E

BDS3 -	Brushless Drive Sine Wave Controller
A - 208, 230	Output L-L RMS Voltage
B - 12,20,30,40,55	Output RMS Current per Phase, Continous
C -	Mechanical Configuration
01	Standard, Fan Cooled, 4" Module
21	Standard Fan Cooled, 6" Module (55 A.)
D -	Option
100	No Option
101	Same As 100 W/Opt 2 Card
102	Same as 100 W/Opt 3 Card
105	Same as 100 W/Spindle Orient Card
123	Same as 100 W/Opt 8 Card
200	With Pigtail Harness and Bus Bars
201	Same as 200 W/Opt 2 Card
202	Same as 200 W/Opt 3 Card
203	Same as 201 W/14 Bit R/D Converter
204	Same as 201 W/10 Bit R/D Converter
205	Same as 200 W/Spindle Orient Card
206	Same as 205 but W/10-Bit R/D Converter
207	Same as 200 W/14 Bit R/D Converter
208	Same as 200 W/OPT5 Card
209	Same as 200 W/OPT6 Card

210	. . . . .	Same as 200 W/Notch Filter
211	. . . . .	Same as 201 W/Notch Filter
212	. . . . .	Same as 202 W/Notch Filter
213	. . . . .	Same as 203 W/Notch Filter
215	. . . . .	Same as 210 W/Spindle Orient Interface Card
221	. . . . .	Same as 200 W/OPT 7 Card
222	. . . . .	Same as 200 W/10 Bit R/D Converter
223	. . . . .	Same as 200 W/OPT 8 Card
224	. . . . .	Same as 200 W/OPT 9 Card
225	. . . . .	Same as 200 W/OPT 10 Card
229	. . . . .	Same as 200 W/OPT 6-01 Card
E -	. . . . .	Motor Compensation

NOTE:

ALL BDS3 MODELS REQUIRE A PSR3-208/25,50, or 75 POWER SUPPLY. -100 MODELS REQUIRE A BUS BAR AND CONNECTOR KIT, BDS3C-XXX. THE KIT IS CONFIGURED TO HAVE THE POWER SUPPLY LOCATED TO THE RIGHT OF THE CONTROLLER(S). A BDS3C-001 WOULD BE USED FOR A SINGLE AXIS SYSTEM; -002 FOR A TWO AXIS SYSTEM; ETC.

MOTOR CABLE ASSEMBLY B-82098 AND RESOLVER CABLE ASSEMBLY B-82096 ARE AVAILABLE IN 10' INCREMENTAL LENGTHS BUT MUST BE ORDERED SEPARATELY IF REQUIRED.

B82095 - SAME AS B82098 BUT WITH TWO EXTRA WIRES FOR THERMOSTAT.
B82097 - SAME AS B82096 BUT WITH TWO EXTRA WIRES FOR TACH.

Use Connector Kit BDS3-001 for a single axis system; BDS3-002 for a two axes system, etc.

A 12-Bit R/D Converter (Refer to Figure 11) is shipped in standard BDS3 motor controllers. Optional 10 and 14 Bit R/D units are available for providing position loop feedback information. R/D units other than the standard 12-Bit unit are identified in the BDS3 complete model number. (Refer to the model number breakdown scheme).

MODEL NUMBER SCHEME

Example: PSR3-208/50-01-002
A B C D

PSR3	Power Supply with Regen for BDS and ACS Systems
A - 208, 230	Amplifier (L-L) RMS Voltage When Using This Power Supply
B - 25, 50, 75	A.C. Line Current, RMS*
C -	Mechanical Configuration
01	Standard, Fan Cooled (4" Module)
21	Standard, Fan Cooled (6" Module) 75 A.
D -	Regen Capability
002	Regen, 7.5 Ohms, 300W (4" Module)
003	Remote Regen Resistor, (4" Module)
005	Regen, 15 Ohms, 150W (4" Module)
201 Thru 206	Remote Regen Resistor (6" Module) Refer to Drawing C-82260

NOTE: -003 MODEL REQUIRES PSR3-EXT/RES-202, REGEN RESISTOR KIT, 4.5 OHMS, 600W MAX. (COOLING DEPENDENT)

-201 THRU -206 MODELS REQUIRE ONE OF THE FOLLOWING REGEN RESISTOR KITS:

-201 PSR3-EXT/RES-201 (6.8 OHMS, 300W) O/L RELAY A-35026;HEATER-K-93034
-202 PSR3-EXT/RES-202 (4.5 OHMS, 600W) O/L RELAY A-35026;HEATER-K-93040
-203 PSR3-EXT/RES-203 (3.2 OHMS, 900W) O/L RELAY A-35026;HEATER-K-93043
-205 PSR3-EXT/RES-205 (2.31 OHMS,1500W) O/L RELAY A-35026;HEATER-K-93047
-206 PSR3-EXT/RES-206 (2.55 OHMS,2000W) O/L RELAY A-35026;HEATER-K-93049

*The PSR3 supply capability is the product of 208vac or 230vac 3 x RMS (L-L) current per phase.

Industrial Drives' BDS3 product lines are 3-phase sinewave brushless motor controllers. They are fully regenerative four-quadrant bi-directional velocity loop amplifiers designed to be used with Industrial Drives high performance permanent magnet brushless motors.

The I.D. brushless motors feature the latest in permanent magnet technology; utilizing high energy Samarium-Cobalt and Neodymium-Iron-Boron alloys. These brushless motors consist of permanent magnet rotors and three-phase Y stator windings. Being brushless motors, there are no commutators or associated brushes. These motors run as synchronous motors, meaning the rotor speed is the same as the speed (frequency) of the rotating stator magnetic field. A brushless resolver is utilized as the feedback device and is mounted internally as part of the overall motor construction. An integral brush tachometer is also available as an option.

An unregulated 300V DC bus for 208 Systems, 350V for 230 derived from full-wave rectification of a three-phase 208 AC line by the PSR3 Power Supply unit, is used to power the BDS3 motor controller. A shunt regulator, or "regen" module located within the PSR3 unit, is used to prevent the bus from being "pumped up" during periods of regeneration.

Benefits resulting from the BDS3 and brushless motor construction are:

1. Lower rotor inertia permits higher acceleration rates.

2. The motor is thermally more efficient since all heat is generated in the stator windings which are located in the outside shell.

3. Higher speed operation and high peak horsepower are achieved. There is no commutation limit.

4. Smaller physical motor size for a given H.P. rating.

5. Higher reliability and less motor maintenance. There is no commutator or brushes.

6. Smooth output torque.

7. The BDS3 sine-wave controller allows for a wider speed range because of the ability to electronically change the angle between the rotor flux and the stator flux . . . .commonly known as the "torque angle."*

*INDUSTRIAL DRIVES, DIVISION OF KOLLMORGEN CORPORATION PATENT NUMBERS 444771 AND 4490661

8. The BDS3 sine-wave controller has the capability to dynamically and adaptively change the torque angle as a function of speed and load, thus allowing the system to operate at the most efficient operating point.

1.1 Ratings

Input Power: 208 or 230 Volts RMS (L-L) 3-phase (±10%);

115 Volts AC 1-phase Control Power

Output Power: PSR3 Power Supply DC Bus; 300 Volts DC Nominal, No load.
BDS3: at rated load; 200 Volts RMS (L-L), Nominal ±10%.

Continuous Current (Amps RMS/Phase)	Intermittent Current (5 sec. max., 30% duty cycle) (Amps RMS/Phase)
12	20
20	35
30	53
40	70
55	96

NOTE: A MAXIMUM OF 6 AMPLIFIERS CAN BE DRIVEN BY A SINGLE POWER SUPPLY.

Ambient Operating Temperature: $0\text{-}55^{0}C$

Switching Frequency: 4Khz

Cooling: Fan, Convection (Cold Plate)

Options: Dynamic Braking, Regeneration (Power Dumping), Directional Limits, Brushless Tach/Brush Tach, Current Foldback Protection, 12/14 Bit encoder output.

Weight BDS3 ---------- 20 lbs.
PSR3 ---------- 21 lbs.

2.0 MOUNTING (Refer to the appropriate Outline and Dimension drawings listed in the Table of Contents)

It is recommended that the BDS3 and the PSR3 units be mounted in their "up-right" (vertical) positions; with the PSR3 mounted to the right of the BDS3 units.

CAUTION: Particular attention should be given to the notes on the Outline and Dimension drawings for information concerning mounting details.

3.0 WIRING (Refer to the notes on the appropriate System Wiring Diagram listed in the Table of Contents)

IN ORDER TO ADHERE TO SUITABLE ENGINEERING PRACTICES, IT IS STRONGLY RECOMMENDED THE 115 VAC CIRCUIT BE CONNECTED IN A MANNER THAT THE 115 VAC IS APPLIED FIRST IN ORDER TO ACTIVATE THE CONTROL AND FAULT CIRCUITS BEFORE APPLYING THE MAIN BUS VOLTAGE.

REMOVE THE PLASTIC FRONT COVERS FROM THE BDS3 AND PSR3 BY REMOVING THE FOUR #4 SCREWS. (Refer to Figures 1 and 2)

There are several types of package configurations offered as options therefore, reference to the NOTES on the appropriate System Wiring Diagram will aid in correctly "wiring the system up."

The following precautions are also recommended:

1. Twist all AC leads to minimize electromagnetic emissions and "noise".

2. Avoid running signal leads in close proximity to power leads, armature leads, or other sources of electromagnetic noise.

3. Minimize lead lengths as much as practical.

4. Double-check all interface wiring. Carefully inspect all connections.

5. DO NOT USE MAIN CONTACTOR FOR CONTROL FUNCTIONS.

IMPORTANT: Motor, tachometer (optional) and resolver phasing are critical for proper operation.

The method of connecting the motor is accomplished either one of two ways:

(1) By way of a connector; where the leads of the three phase motor stator are brought out to pins A, B, and C of the motor connector. Pin D is normally grounded at the BDS3. However, it may be grounded at the main ground point.

Simply wire pins A, B, C of the motor connector to the points of the power terminal block, mounted at the top of the BDS3 chassis, identified M_A, M_B, and M_C. (Refer to the System Wiring Diagram and Figures 7 and 8)

(2) By way of flying leads; where the leads of the three phase motor stator are color coded and are available directly out of the motor.

Notice the information on the System Wiring Diagram referring to the correct method of wiring the motor stator. The BROWN, GREEN, and ORANGE leads should be connected to the points identified as M_A, M_B, and M_C respectively on the power terminal block, mounted at the top of the BDS3 chassis. Connect the GREEN/YELLOW lead to the ground point of the same terminal block. (Refer to the System Wiring Diagram and Figures 7 & 8)

The three phase 208 input power, from the secondary of the three phase transformer, (Refer to Drawing A-M80421) should be brought through a customer supplied circuit breaker and connected to points identified as L_A, L_B, and L_C on the power terminal block mounted at the top of the PSR3 chassis. The system is not AC line phase sensitive (Refer to the System Wiring Diagram and Figures 9 and 10). Connect the 300V DC output, the 115V AC, and the regeneration circuit from the PSR3 to the BDS3 with the strapping bars and the small 115V AC and Regen cable.

CAUTION: Check to insure that the small cable is connected to the correct pins and that it is not offset to one side. (Refer to the System Wiring Diagram and Figures 3 and 4)

To access the 115V AC control terminal block within the PSR3, remove the plastic front cover by removing the four No. 4 screws. (Refer to Figures 1, 2, 9 and 10)

To access the control terminal strips to wire the BDS3, remove the plastic front cover by removing the four No.4 screws. (Refer to Figures 1,2,5,and 6) do the following:

1. It is recommended the signal wires be brought into the BDS3 from the bottom in order to keep them segregated from the power wires entering at the top of the unit. The wiring should be neatly dressed in order not to interfere with remounting the plastic front cover.

2. Unplug the 10 and 20 point terminal strips (97 and 210) from their connectors on the BDS3-Motor Control Board. (The board on the right-hand side) This will prevent over flexing the board when wiring up the connectors.

3. After removing the two terminal strips, wire them per the appropriate System Wiring Diagram. (Refer to Section 3.2)

4. Neatly dress the wire cable in a way that it will not interfere with securing the plastic front cover. Signal cables should be dressed separately. Not with the AC or power wiring.

5. Leave sufficient length in the wiring to allow the Motor Control Board to slide out enough to expose the small Compensation Board (Refer to Figures 5, 6, and 12). Insert the wired terminal strips back on to their connectors.

CAUTION: The motor thermostat is an AUTOMATIC RESETTING device and should be connected into a latched (LOCKED-OUT) power down type circuit.

CAUTION: The Motor Overload relay (customer furnished) is set to the AUTOMATIC MODE, should be used in a latched power down type ci it.

3.1 Grounding Scheme (Refer to the appropriate System Wiring Diagram)

It is important that the motor be grounded at the BDS3 motor terminal block as shown on the Wiring Diagram or at the main ground point. Connect shielded cables at one end only. Butt the other end.

3.2 Signal Inputs and Modes of Operation

The following descriptions are given to help the user decide what inputs and modes of operation to incorporate into the overall system and to identify the appropriate connecting points of connector 210. (Refer to Figures 5 and 6)

The Drive-Up contact closure (internally) is provided at Pins 1 and 2 and may be utilized one of two ways:

1) When jumper J3 is removed and J20 is installed on the ACS3-COMP1 Board, an internal contact will close when the Remote Inhibit circuit is closed (is pulled low) indicating to the "outside world" that the BDS3 is in the Drive-Up Mode. The intenral contact will open when the Remote Inhibit input circuit is opened (goes high) indicating that the BDS3 is in the Inhibit Mode.

   In the event that a fault occurs within the BDS3, as may be indicated by an illuminated red LED, the internal contact will remain open regardless of the state of the Remote Inhibit input circuit.

2) When J3 is installed on the ACS3-COMP1 Board, an O.K. to Enable function is introduced to the Drive-Up Mode of operation. When J20 is removed, J3 is installed, the Remote Inhibit circuit is open (is high), and

there are no fault LED's illuminated, the internal contact will remain closed indicating that the BDS3 is O.K. to enable. The Remote Inhibit circuit may then be pulled low to enable the BDS3. Otherwise, the internal contact will remain open indicating that the BDS3 is in a fault mode.

The Drive-Up contact is reated at 115VAC at 2 amps.

The Sum 1 and Sum 2 inputs, at Pins 4 and 5, are auxiliary inputs. These inputs are normally used in conjunction with various optional interfacing schemes; such as special situations requiring two BDS3 systems working together in an Antibacklash or any one of several other types of Master-Slave applications.

The V Error (Velocity Error Signal) is brought out at Pin 6. This signal is the difference between the commanded speed and actual motor speed. The V Error output, like Sum 1 and Sum 2 above, is optional and generally needed when the BDS3 is used in master slave applications.

The Torque Hold mode allows the amplifier to be put into a low gain or torque mode by closing a contact or installing a jumper between either Sum 1 or Sum 2 and V Error.

The External Current Limit (when provided) may be utilized, when external control of motor torque is desired, by opening a contact between Pins 7 and 11 (D-common). Refer to the T.L. Sheet for reduced current limit value. Normal operation requires a contact closure or jumper between these two points.

The Remote Inhibit allows a means by which the BDS3 may be disabled without removing the main power. When a contact is closed between Pins 8 and 11 (D-common) the BDS3 will be put into the "Drive-Up" mode. Opening the contact will put the BDS3 into the "Inhibit" mode.

The A-Common points at Pin 9 and 10 are shield and signal commons. These points provide commons (returns) between external equipment (Numerical Controls etc.) and the BDS3.

The D-Common point at Pin 11 is utilized with the External Current Limit and Remote Inhibit modes of operation.

The I Offset, (an option) at Pin 13 is an input provided for injecting voltage levels into the BDS3 when used in antibacklash and other special types of applications.

The Input Reference Signal (not to exceed ± 8 volts) is applied to the BDS3 at Pin 14 with respect to 15.

-12 Volts is available at Pin 17 and +12 Volts is available at Pin 20 and may be used as a signal source for manual and semi-automatic machines. (Maximum available current is 12 ma from each supply).

The I Mon Current Monitor signal may be observed at Pin 18. There is a direct relationship between this voltage and the actual motor currents. A D.C. voltmeter placed between Pins 18 and Pins 9 or 10 can serve as a means to monitor motor current.

The current scale factor at the Current Monitor test point above may be determined by the following chart:

BDS3 Continuous Current Rating (RMS/Phase)	Amps RMS/D.C. Volt (per phase)
12	2.625
20	4.375
30	6.625
40	8.75
55	12.031

The Tach Out at Pin 19 is a signal which represents speed. A D. C. voltmeter placed between Pin 19 and Pins 9 or 10 (calibrated in R.P.M.) can serve as a means by which speeds may be monitored. Refer to the T.L. sheet for the system, for the scale factor in volts/R.P.M. (8 volts = maximum rated motor speed)

4.0 PRELIMINARY CHECKS (Refer to the appropriate System Wiring Diagram)

Once the BDS3 system has been installed and wired in, follow the Preliminary Check-Out procedure to ensure proper operation before the Main Power is applied.

4.1 Checking the AC Input Voltage

Open the circuit breaker or remove the fuses in the secondary of the large 3-phase isolation transformer.

Apply power. With an AC voltmeter, check the 3-phase secondary line-to-line voltage. The voltage should be approximately 208 volts RMS ±10%. Remove power. Close the circuit breaker or replace the fuses in the secondary of the large 3-phase isolation transformer.

4.2 Checking the PSR3 D. C. Output Voltage

DO NOT APPLY THE 115 VOLT AC. Apply power to the large 3-phase transformer only.

With a DC voltmeter, monitor the 300 volt DC bus bars at the bottom of the PSR3 and BDS3 units. The bus bar on the outside should be positive with respect to the inner bus bar.

The voltage from the PSR3 should be approximately +300 volts DC. ±10%. Remove power.

4.3 Checking the Brushless Motor Phasing

If the motor stator is wired according to the system Wiring Diagram, the phase sequence will automatically be correct.

Remove the motors' 3-phase stator connector from the motor. Check continuity between the pins of the motor stator connector and the terminal block of the BDS3 unit; as identified by the System Wiring Diagram. Note the color code of the stator wires in the flying lead series.

4.4 Checking the Brush Tach Phasing (When Used)

With a DC voltmeter (on a sensitive VDC scale), monitor input connector 210-19 with respect to 210-9. Have an assistant rotate the motor shaft C.W. The voltmeter should read positive. (Pin R on the motor connector should connect to Connector 210-19). Pin 5 on the motor connector should connect to Connector 210-9).

4.5 Checking the Resolver Phasing

If the resolver is wired according to the System Wiring Diagram, the resolver phase sequence will automatically be correct. Remove the motors' system resolver connector at the motor. Remove connector 97 from the BDS3 unit. (Refer to Figures 5 and 6). Check continuity between pins of the resolver connector and pins of connector 97 at the BDS3 unit per the System Wiring Diagram.

5.0 CONNECTING THE INPUT SIGNAL SOURCE (N/C, C/N/C, ETC.)

CAUTION: INCORRECT SERVO TO POSITION LOOP PHASING CAN CAUSE LARGE EXCURSION OSCILLATIONS OR RUNAWAYS.

Appropriate precautions should be taken to stop the machine if necessary. Slides, etc. should be moved a reasonable distance away from hard stops or motor drive belt removed, etc., before applying power.

Apply power, enable the BDS3. Observe the action of the machine. If it is determined that the direction of rotation of the motor is reversed (slide moves in the wrong direction, etc.) do the following:

1. Remove all power. Remove the front cover from the BDS3.

2. Slide the Motor Control Board out and remove the small Compensation Board. (Refer to Figures 5, 6, and 12)

3. Notice the NON-INVERTING and INVERTING jumpers 10 and 11. Only one of the two will be installed. (Refer to Drawing C-81506-1)

4. Remove the jumper installed. Add the jumper presently missing.

4. Replace the Compensation Board. Slide the Motor Control Board back into the amplifier chassis.

6.0 ADJUSTMENTS

Remove power. Remove the front cover from the BDS3 chassis by removing the four no. 4 screws. The adjustment pots are located on the front edge of the boards. (Refer to Figures 5, 6, 7, 8, 9, and 10)

6.1 ZERO Adjustment

For N/C or C/N/C machines:

If the "Following Error" is displayed by way of read-out,

simply adjust the Zero Pot 30 (located on the Compensation Board) for zero "Following Error" at zero speed.

Optional: Monitor "INPUT HI" with respect to "INPUT LO" at 14 and 15 (screw heads of terminal strip 151) with a DC voltmeter. Command zero speed from the N/C or C/N/C. Adjust the Zero Pot 30 for zero volts.

For Manually Operated Machines:

With the input signal at zero volts, simply adjust Pot 30 for zero speed.

6.2 SPEED SCALE FACTOR Adjustment (With N/C or C/N/C)

If the "Following Error" is displayed by way of read-out, command an appropriate speed (preferably a slow feed rate) and adjust Pot 31 (located on the ACS3-COMP1 Board) for the proper amount of "Following Error".

6.3 SPEED SCALE FACTOR Adjustment (Manually Operated Machines)

Turn the Speed Scale Factor Pot (31) fully CCW. Apply input signal level which equals desired motor speed in R.P.M.

Adjust Pot 31 CW until motor obtains desired speed in R.P.M. (Normally done with a manual input signal level).

6.4 GAIN Adjustment

In many cases, Pot 32 (located on the Compensation Board) will not need to be adjusted. However, if necessary, the Gain Pot can be used to improve the dynamic response of the servo loop. To increase the "AC Gain", monitor the internal "tach" signal at Terminal Strip 210-19 with respect to 210-9 with an oscilloscope. Turn Pot 32 fully CCW. Apply a step input command signal while accelerating and decelerating the motor at approximately 25% of maximum speed. Adjust the Gain Pot 32 CW and notice the tach signal response. Watch for indication of instability in the tach waveform. Turn Pot 32 CCW until the tendency to go unstable diminishes.

CAUTION: INCREASING THE GAIN TOO MUCH MAY CAUSE THE SYSTEM TO GO UNSTABLE.

6.5 RESOLVER EXCITATION Adjustment

If the resolver lead lengths are in excess of 100 ft., the Resolver Excitation Voltage adjustment may have to be adjusted. To make this adjustment, refer to Figures 5, 6, and 11. Do the following:

(1) Inhibit the BDS3.

With an oscilloscope, monitor the sine functions at the resolver connector 97, terminal 1, with respect to 2.

This signal will peak twice in one mechanical revolution of the motor.

(2) Have an assistant rotate the motor shaft manually until a maximum peak voltage is obtained. Adjust Pot 24 for 2.8 Volts Peak as shown below:

6.6. HALL EFFECT CURRENT SENSOR ZERO Adjustments

WARNING: DO NOT ADJUST THE CURRENT FEEDBACK GAIN POTS ON THE BASE DRIVE BOARD. POTS 50 AND 55 ARE FACTORY SET AND SEALED ADJUSTMENTS ONLY. IF ONE OF THESE SEALS IS EVER BROKEN, RETURN THE COMPLETE BDS3 AMPLIFIER TO THE FACTORY FOR ALIGNMENT.

Inhibit the BDS3. With a D.C. voltmeter, monitor TP386 on the motor control board with respect to TP350 (Common). Adjust Pot 54 on the base drive board for 0 volts ±10 mv. Monitor TP348 on the motor control board with respect to TP350 (Common). Adjust Pot 49 on the base drive board for 0 volts ±10 mv.

6.7 REGEN LEVEL Adjustment (Refer to Figures 9 and 10)

Inhibit the BDS3. For BDS3-208 Volt Amplifiers:

With a D.C. voltmeter, monitor TP22 on the Regen Board (BDS3-REG 1) within the PSR3 unit. Adjust Pot 17 for 8.20 volts.

For BDS3-230 Volt Amplifiers With a D.C. voltmeter, monitor TP22 on the Regen Board (BDS3-REG 1) within the PSR3 unit. Adjust Pot 17 for 7.40 volts.

6.8 OVERVOLTS Adjustment (Refer to Figures 9 and 10)

Inhibit the BDS3. For BDS3-208 Volt Amplifiers:

With a D.C. voltmeter, monitor TP20 on the Regen Board (BDS3-REG 1) within the PSR3 unit. Adjust Pot 19 for 6.15 volts.

For BDS3-230 Volt Amplifiers: With a D.C. voltmeter, monitor TP20 on the Regen Board (BDS3-REG 1) within the PSR3 unit. Adjust Pot 19 for 5.68 volts.

6.9 BDS3 SYSTEM RESOLVER ZERO

The BDS3 System Resolver Zero has been factory set and secured. The following procedure is given only in the event the resolver becomes misaligned during motor repair, etc. (Refer to Figures 15, 16, 17, and Page 36).

PLEASE USE CAUTION

-1 Remove Power

-2 Place a jumper between TP95 and TP96 on the ACS3-MC2 Control Board.

-3 Place a jumper between Connector 210-4 and 6.

-4 Disconnect the A phase motor lead from the amplifier.

-5 Connect a digital DC voltmeter to TP219, with respect to common (TP348).

-6 Remove the screws which hold the end plate to the rear end bell of the motor. Remove the end plate. The shaft mounted frameless resolver should be in sight.

-7 The frameless resolver rotor is slid forward onto the motor shaft and secured by a large lock nut. This part of the resolver need not be disturbed unless it is to secure the lock nut. It does not matter where the resolver rotor is in respect to the motor shaft, just as long as it remains secure.

-8 Apply power, but inhibit the BDS3 by opening the circuit at connector 210-8. Rotate the motor shaft C.W. by hand until the zeroing LED (Refer to Section 7.2 point 3) is on continuously.

-9 Enable the BDS3 by closing the circuit at connector 210-8. Input a reference voltage until the DVM (connected to TP219) reads -1.5±100mv. The motor should be locked into one of the three low torque points located 120 mechanical degrees apart, around the motor stator. The ZEROING LED should still be on continuously (not blinking). If the LED remains illuminated continuously, no further action is necessary. The system resolver is correctly set. Remove jumpers, DVM, and reconnect the motor lead. If blinking, please proceed.

-10 If the LED is blinking and the motor <u>does not</u> have an <u>application resolver</u> (Refer to Figures 15 and 16), continue to Step 11. If the motor also has an application resolver (Refer to Figure 17, continue to Step 11, but keep in mind; this procedure is for the SYSTEM RESOLVER, not the APPLICATION RESOLVER.

-11 Loosen, but do not remove the two servo clamp screws holding the resolver stator secure and continue from Step 9, above. Rotate the resolver stator (outside portion). As the zero position is approached, the LED should blink increasingly faster. If this cannot be achieved, rotate the motor shaft to another one of the three "locked" positions (approximately 120 mechanical degrees) from where the motor shaft is at present. The LED should blink. Once again, adjust the resolver stator for a steady illuminated LED. Tighten the two servo clamp screws to secure the resolver stator.

Remove power. Remove the jumper between TP95 and TP96 on the Motor Control Board.

Remove the jumper between Connector 210-4 and 6.

Reconnect the A phase motor lead to the BD83.

Remove the DVM.

7.0 PSR3 POWER SUPPLY MODULE

PSR3 is available in three current ratings: 25,50, and 75 amps. Each PSR3 incorporates control circuitry, that limits the D.C. bus voltage to a safe level during periods of regeneration. All units have this resistor internal to the module. (Refer to model breakdown scheme in the front of manual and Figures 9 and 10). For those units that require an external regen power ressistor, IT MUST BE INSURED THAT ITS INSTALLATION IS NOT CLOSE TO ANY FLAMMABLE MATERIALS.

PSR3-208-25
This model is available with an internal regen power resistor of 15 ohms, fused for 10 amps. There is no option for an external power resistor. (Refer to Drawing C-81543)

PSR3-208/50
This model is available with an internal regen power resistor of 7.5 ohms, (two 15 ohm res. in parallel) fused for 15 amps. There is an option for an external power resistor of 4.5 ohms, fused with 30 amps. (Refer to Drawing C-81543)

PSR3-208/75
This model is available with only an external regen power resistor. Protection for this circuit is accomplished by an internal thermal overload relay. THE CONTACT FROM THIS RELAY MUST BE WIRED IN SUCH A MANNER THAT THE THREE PHASE POWER TO THE PSR3 IS REMOVED IF AN OVERLOAD IS DETECTED. (Refer to the appropriate System Wiring Diagram and Drawing C-82182)

8.0 TROUBLESHOOTING HINTS

The BDS3 and PSR3 are designed to promote minimum down time situations. Due to the smaller package size, these units are to be replaced if they cease to function properly. Therefore, the best defense against down time is to keep on hand one or more complete spare BDS3 and PSR3 units. Since the BDS3 units are downward compatible (units of larger capacity may be used to replace units of smaller capacity), they are directly interchangeable provided:

1. The package dimensions are accommodating.

2. The Motor Control Card contains the proper microprocessor unit, per the TL Sheet.

3. The Compensation (Personality) Card is matched with the motor.

Some recommended equipment for troubleshooting the BDS3 and PSR3:

(1) Adjustable signal source 0-±8V DC (small 9V DC battery with input reversing switch will do).

(2) Dual trace oscilloscope

(3) D.C. voltmeter

Before beginning the troubleshooting process, consider the following points:

I. There are five (5) distinct areas within which a fault may occur:

1. External Interface

(1) circuitry external to, but connecting to, the BDS3 and PSR3.

2. BDS3 Control Stage (Refer to Figures 5, 6, 11, and 12).

(1) ACS3-MC2, Motor Control Board, containing the following:

a. ACS3-Comp 1(Compensation) Board (Refer to TL Sheet)
b. OPT1, OPT2, OPT3, OPT4, OPT5, etc.(Refer to Figures 13, 14, 15 and 16). OPT1 not shown in Figures)
c. Microprocessor Unit (Refer to TL Sheet)
d. R/D Converter Unit

3. BDS3 Power Stage (Refer to Figures 7 and 8)

(1) Heat Sink, containing the following:

a. BDS3-BD1, Base Drive Board- Control Power Supplies
b. Fuse (115vac, 1 1/2 amp MDL) refer to parts list
c. Power Transistor Paks
d. Thermostat

4. PSR3 Control Stage (Refer to Figures 9 and 10)

(1) BDS3-Reg 1, Regeneration Board

5. PSR3 Power Stage (Refer to Figures 9 and 10)

(1) Heat Sink, containing the following:

a. Power Transistor (Regeneration)
b. Resistive Load (Regeneration on Chassis)
c. Rectifier Paks (Main D.C. Bus)
d. Large Filter Capacitors (Main D.C. Bus)
e. Fuse 1 1/2 amp AGC (115V AC on Chassis) Refer to parts list
f. Fuse according to the following:
PSR3-208/25-XX-005=10 amp
PSR3-208/50-XX-003=30 amp
With external regen resistor.
PSR3-208/50-XX-002=15 amp
With internal regen resistor
(Regeneration fuse, on chassis)
Refer to Parts List
PSR3/75-XX-Overload relay with proper heater element (Refer to PSR3 MODEL NUMBER SYSTEM in front of Manual)

II. There are only two basic fault characteristics to be considered:

1. The motor exhibits very low torque or is totally inoperative.

2. The motor is erratic or exhibits an improper mode of operation.

8.1 The Motor Exhibits Very Low Torque or is Totally Inoperative

Prerequisites for motor movement:

1) All power must be present.

2) The BDS3 must be in the enable mode, as indicated by the Bar Graph DRIVE UP LED.(Refer to Figure 1)

3) A command signal(other than zero) must be present at the input of the BDS3.

4) The BDS3 and PSR3 must be wired correctly, per the appropriate System Wiring Diagram. Also, check the External Current Limit input circuit and confirm that it is pulled low (tied to common). If this input is not tied to common, the motor torque will be restricted to approximately one third of its peak rating. Refer to Section 3.2

5) Fault circuits must not be activated. Fault modes are identified by diagnostic bar-graph indicators. (Refer to Figure 1 and Section 7.2)

Five of the 10 LED INDICATORS are latched fault modes. To reset any of the faults identified as a latched condition, by Section 7.2, simply remove the power, wait 60 seconds, then reapply it.

8.2 LED Status, Diagnostics Bar Graph

1. BUS FAULT (RED)

(a) The Main Bus should be 300V DC ±10% for BDS3-208 and 325V DC ±10% for BDS3-230 units.

The LED will become illuminated if the Main D.C. Bus rises above 415V. The BDS3 will become latched in the inhibit mode. (May happen if the PSR3 unit does not have a BDS3-Reg 1 Board or if this board malfunctions) (Refer to Figures 9 and 10).

(b) This LED will also become illuminated if the Main Bus is insufficient or absent. See Figures 3 and 4.

(c) This LED will also become illuminated if the Regen Fuse blows. Usually means the Regeneration load resistor bank is insufficient.

This resistor load is utilized with a shunt regulator power transistor switch and BDS3-Reg 1 Board located within the PSR3 unit. The circuit is used to prevent the Main Bus from being "pumped up" during deceleration periods by overhauling motor loads. (Refer to Figures 9, 10, and Drawing C-82260)

2. OVERSPEED (RED)

In the event the motor obtains an excessive speed, the OVERSPEED fault circuit will activate, latch the BDS3 in the inhibit mode, and the LED will become illuminated.

3. ZEROING (YELLOW)

This LED is not a fault indicator but, is used to help set the BDS3 system resolver zero point. (Refer to Section 6.9-8)

4. REMOTE INHIBIT (YELLOW)

This LED is not a fault indicator. When the LED is illuminated, it simply means the BDS3 is in the inhibit mode. This LED will always take the opposite state to that of the DRIVE UP LED when J20 is installed on the ACS3-COMP1 Board.

5. DIRECTION (GREEN)

This LED is not a fault indicator. It indicates direction of rotation of the motor shaft. It will be illuminated to indicate C.W., extinguished to indicate C.C.W.

6. DRIVE UP (GREEN)

This LED is not a fault indicator. When the LED is illuminated, it simply means the BDS3 is in the enable mode. The LED will always take the opposite state to that of the REMOTE INHIBIT LED when J20 is installed on the ACS3-COMP1 Board. There will be no motor movement until this LED becomes illumianted.

7. FOLDBACK (YELLOW)

When the LED becomes illuminated, it is an indication that the motor peak current is remaining at a high level too long or the duty cycle is too severe. In either case, the peak current will be reduced automatically to the continuous current rating of the BDS3 until the load demand is removed.

8. POWER LOSS (YELLOW)

When the LED becomes illuminated, it is an indication that the +5 volt logic supply is not functioning properly, usually because the 115V AC has been momentarily interrupted. In this event, the BDS3 will become latched in the inhibit mode.

9. OVERTEMP (RED)

In the event the transistor power stage overheats a thermostat (mounted on the power stage heat sink) will open, the LED will become illuminated, and the BDS3 will become latched in the inhibit mode. (Refer to Figures 7 and 8)

10. OVERCURRENT (RED)

When this LED becomes illuminated, it indicates an overcurrent condition usually due to a shorted load (motor) or a shorted power transistor (BDS3). The BDS3 will become latched in the inhibit mode. If this LED becomes illuminated, remove the power and disconnect the motor. Reapply power. If the BDS3 comes up without this LED becoming illuminated, suspect a faulty motor. If the BDS3 comes up with the LED illuminated, suspect a faulty BDS3 power stage.

8.3 The Motor is Erratic or Exhibits an Improper Mode of Operation

Prerequisites for proper motor operation:

1) Proper grounding scheme. The motor ground wire should be grounded as shown by the appropriate System Wiring Diagram or grounded to the main ground point.

2) Motor armature leads must not be run in conduit or wire ducts with any signal carrying conductors.

3) The resolver leads and motor armature leads must be wired according to the appropriate System Wiring Diagram.

4) The tachometer leads (when used) must be connected so that a clock-wise turn of the motor shaft will produce a positive voltage at Connector 210-19 with respect to 210-9.

5) The motor system resolver must be set at its zero point. (Refer to Section 6.9)

6) The motor should be loaded; otherwise, the system may become unstable.

9.0 OPTION BOARDS

Option boards are brought into existence from time to time to satisfy specific needs and to add versatility to the product.

9.1 ACS3-OPT2

The ACS3-OPT2 is an encoder board. The main function of this board is to convert the binary (motor shaft) position information from the R/D converter (mounted on the ACS3-MC2 Board) into an encoder output format. An L.E.D. display of the signals is provided. (Refer to Drawing C-81991-1 and Figure 13)

Each BDS3 Amplifier has a R/D (Resolver to Digital) converter mounted on its ACS3-MC2 Board. The R/D may be a 10, 12, or 14 Bit unit. The ACS3-MC2 Board works in conjunction with the R/D to generate the Encoder output lines. The Standard 100, 101, 200, 201, and 202 Series BDS3 Amplifiers have 12 Bit R/D units. Refer to the Model Number Scheme in the front of the manual to determine what R/D your BDS3 amplifier may have.

Also, there are two types of R/D units currently in use; the Open Housed unit and the Encapsulated unit. Refer to Chart 1 for information concerning restrictions in motor speed in RPM for the two different types of R/D units. All jumpers and switches on the OPT2 Board have been previously set at the factory.

The ACS3-OPT2 Board in conjunction with the R/D unit generates two line quadrature channels of information with a third channel of marker pulses. The two line quadrature channel options are as follows:

1. With a 10-Bit R/D unit (mounted on the ACS3-MC2 Board) the ACS3-OPT2 converts 10 bits of R/D (Resolver to Digital) information into two 256 line quadrature channels.

2. With a 12-Bit R/D (configured as an 11-Bit unit) the ACS3-OPT2 converts 11 bits of R/D information into two 512 line quadrature channels.

3. With a 12-Bit R/D (Standard) the ACS3-OPT2 converts 12 bits of R/D information into two 1024 line quadrature channels.

4. With a 14-Bit R/D (configured as a 13-Bit unit) the ACS3-OPT2 converts 13 bits of R/D information into two 2048 line quadrature channels.

5. With a 14-Bit R/D the ACS3-OPT2 converts 14 bits of R/D information into two 4096 line quadrature channels.

If you have ordered the ACS3-OPT2 Board option as a separate item to add to your BDS3 amplifier, please refer to Chart 1 for information concerning the ACS3-OPT2 jumper and switch configurations.

signal that represents the RMS phase current to the motor. The signal after entering the ACS3-OPT6 Board is normally scaled for +8.0 volts and represents the maximum RMS amplifier phase current at TP-40. However, this signal may be scaled over a limited range for an external load meter. To scale this signal for an external load meter, connect a DVM to TP-40. Adjust Pot 39, Load Meter Scaling for the desired value in amps/volt.

9.4.7 RAMP ADJUSTMENT

The Ramp circuit alters the speed reference signal. For a step input reference voltage, adjust Pot 71 fully counter clockwise for command signals of 1.525 seconds per volt or fully clockwise for 0.025 seconds per volt ramps. The adjustment range is linear between the extremes.

10.0 SPARE PARTS LIST

The BDS3 and PSR3 are designed to promote minimum down time situations. Their design features promote change out if they cease to function properly. Therefore, the best defense against down time is to keep on hand one or more complete spare BDS3 and PSR3 units.

BDS3

Description	I.D. Model Number
Motor Control Board	BDS3-MC1 (Discontinued)
Motor Control Board	ACS3-MC2 (Must have ACS3-MC2 micro to replace with BDS3-MC1)
F65	1 1/2A. Slo-Blo 3AE 250V
Microprocessor	Refer to TL Sheet for System
R/D Converter	A-80994-002
Compensation (Personality) Board	ACS3-Comp 1
Encoder Option Board (When Used)	ACS3-OPT2
Thermostat	A-80078

BDS3-208/12

Base Drive Board	BDS3-BD1-12
Power Stage Transistor 50A/450V	A-80121

BDS3-208/20

Base Drive Board	BDS3-BD1-20
Power Stage Transistor 75A/450V	A-79957

BDS3-208/30

Base Drive Board	BDS3-BD1-30
Power Stage Transistor 100A/450V	A-80641

BDS3-208/40

Base Drive Board	BDS3-BD1-40
Power Stage Transistor 150A/450V	A-80504

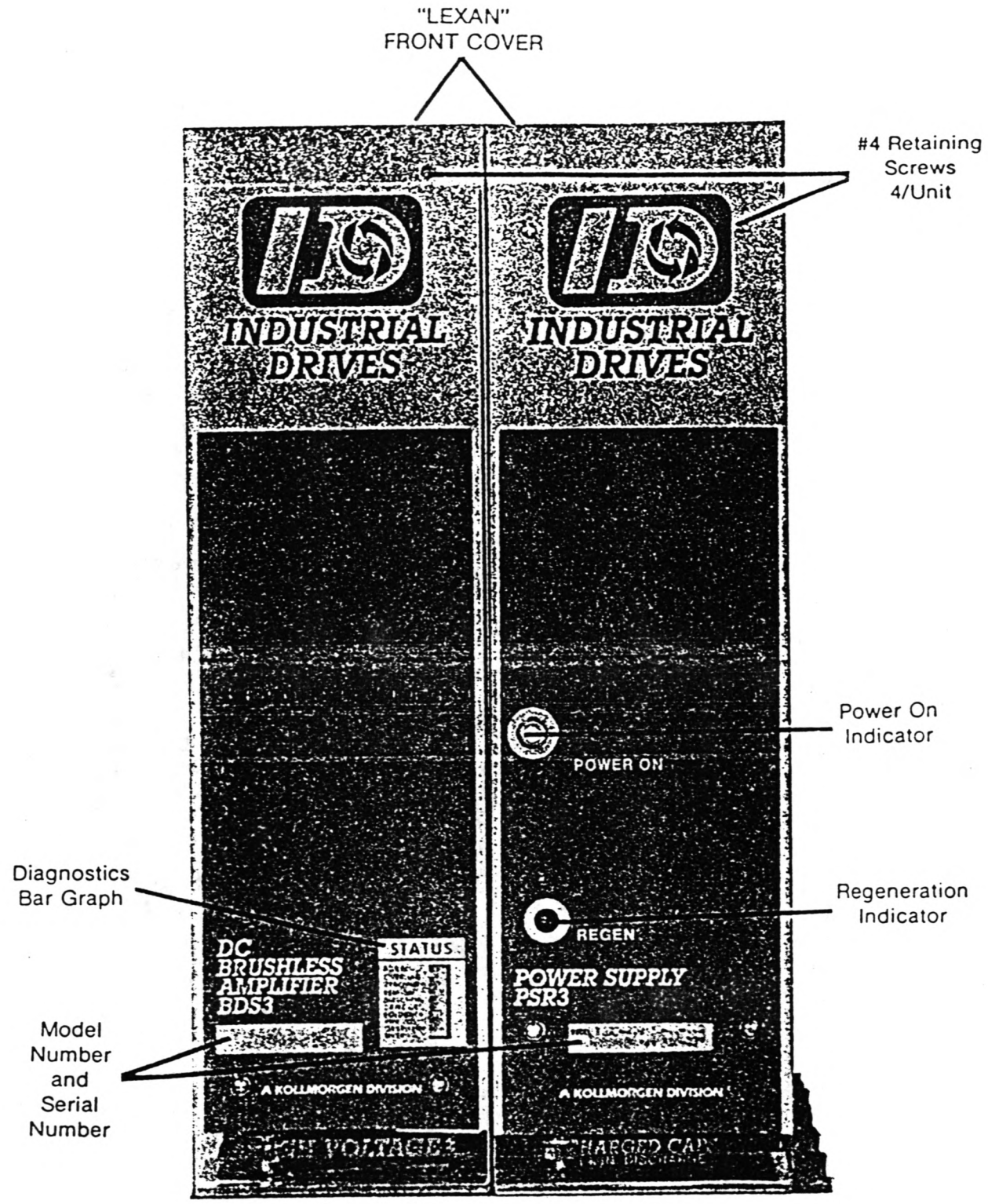
BDS3-208/55

Base Drive Board	BDS3-BD1-55
Power Stage Transistor 150A/550V	A-81707

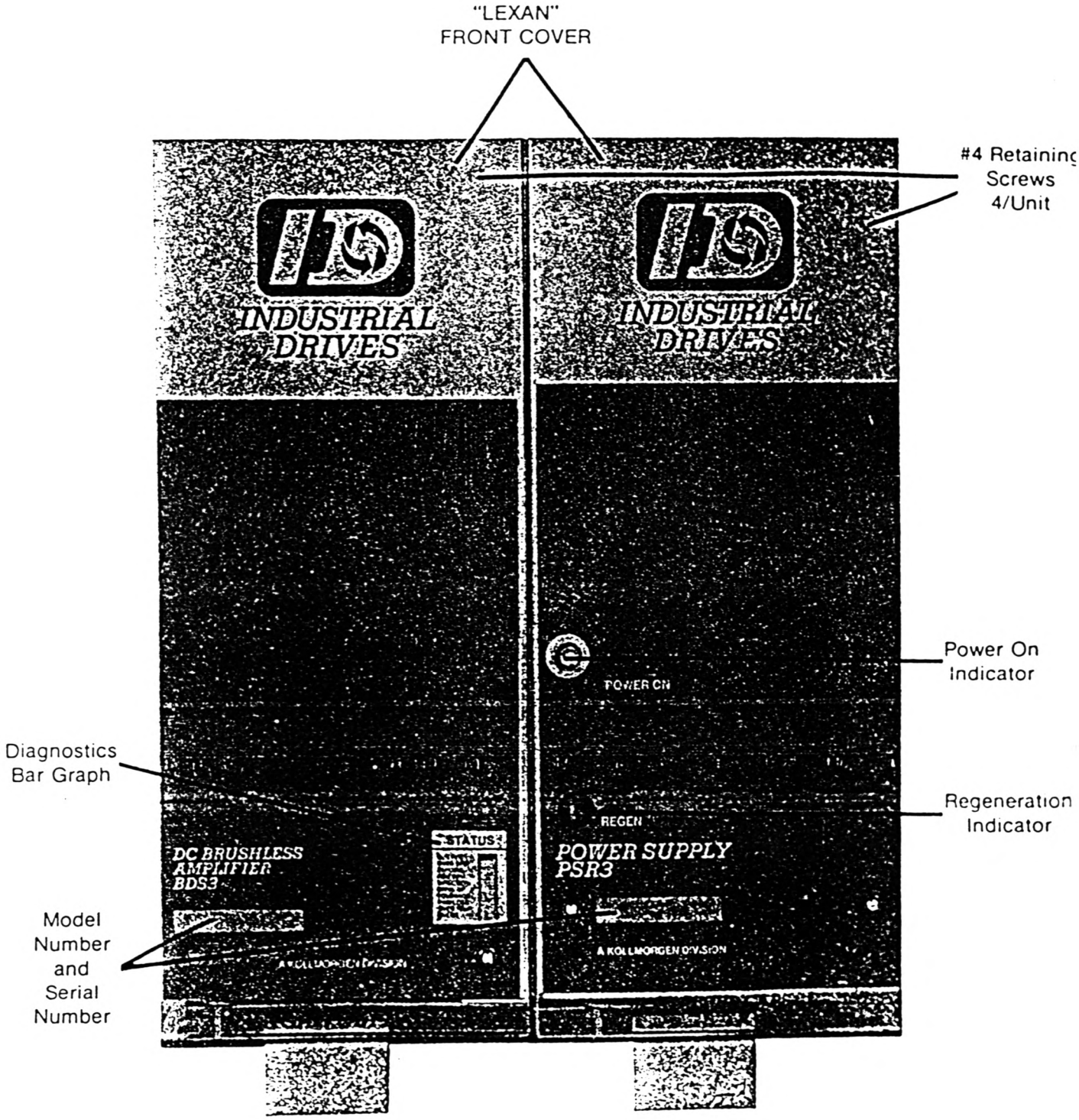
PSR3

Regeneration Board	BDS3-REG 1
Regeneration Resistor Load (Internal) 15 ohm 280W	A-81162
Regeneration Fuse	**
Regeneration Power Transistor Module 100 amp.	A-81080
F54 5 amp/250V	A-78896-013

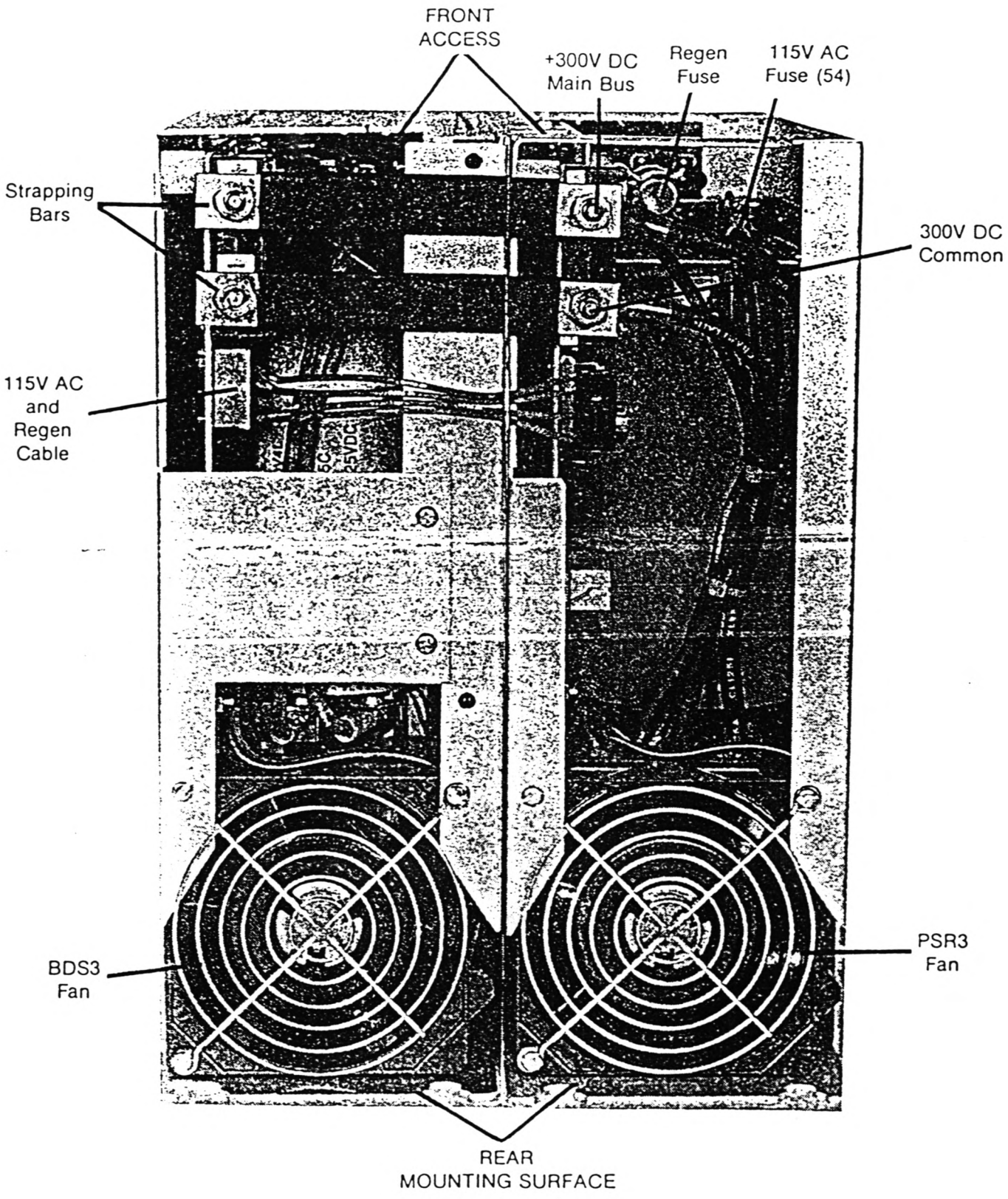
**	PSR3-208/25-XX-005	10 amp	A-79787-001
	PSR3-208/50-XX-002	15 amp	A-79787-002
	PSR3-208/50-XX-003	30 amp	A-79787-005
	PSR3-208/75-XX-XXX	(Overload relay/heater)	Refer to PSR3 MODEL NUMBER SYSTEM in front of Manual



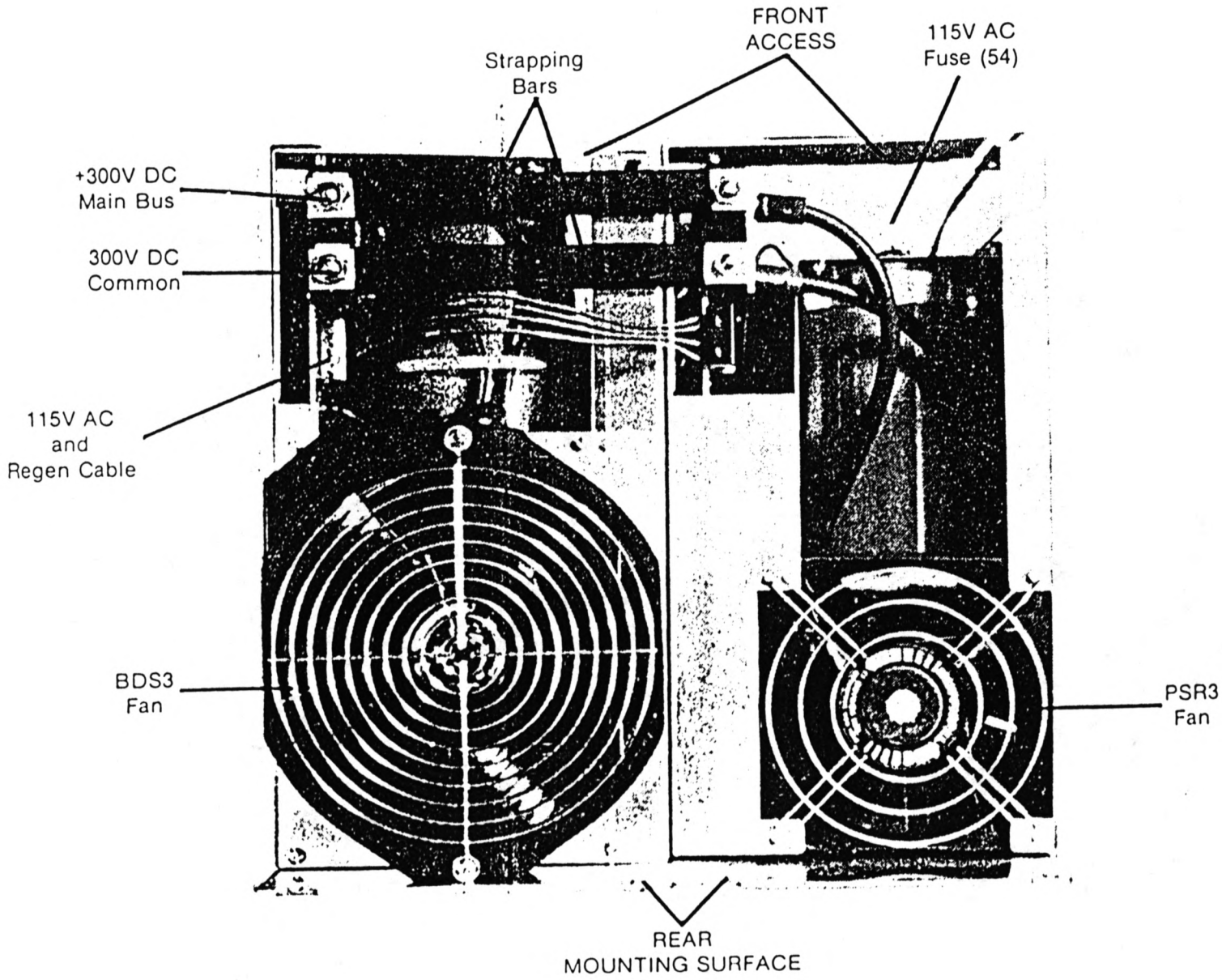
BDS3 - 12/20/30/40 AMP AND PSR3 - 25/50 AMP
(FRONT VIEW)
FIGURE 1



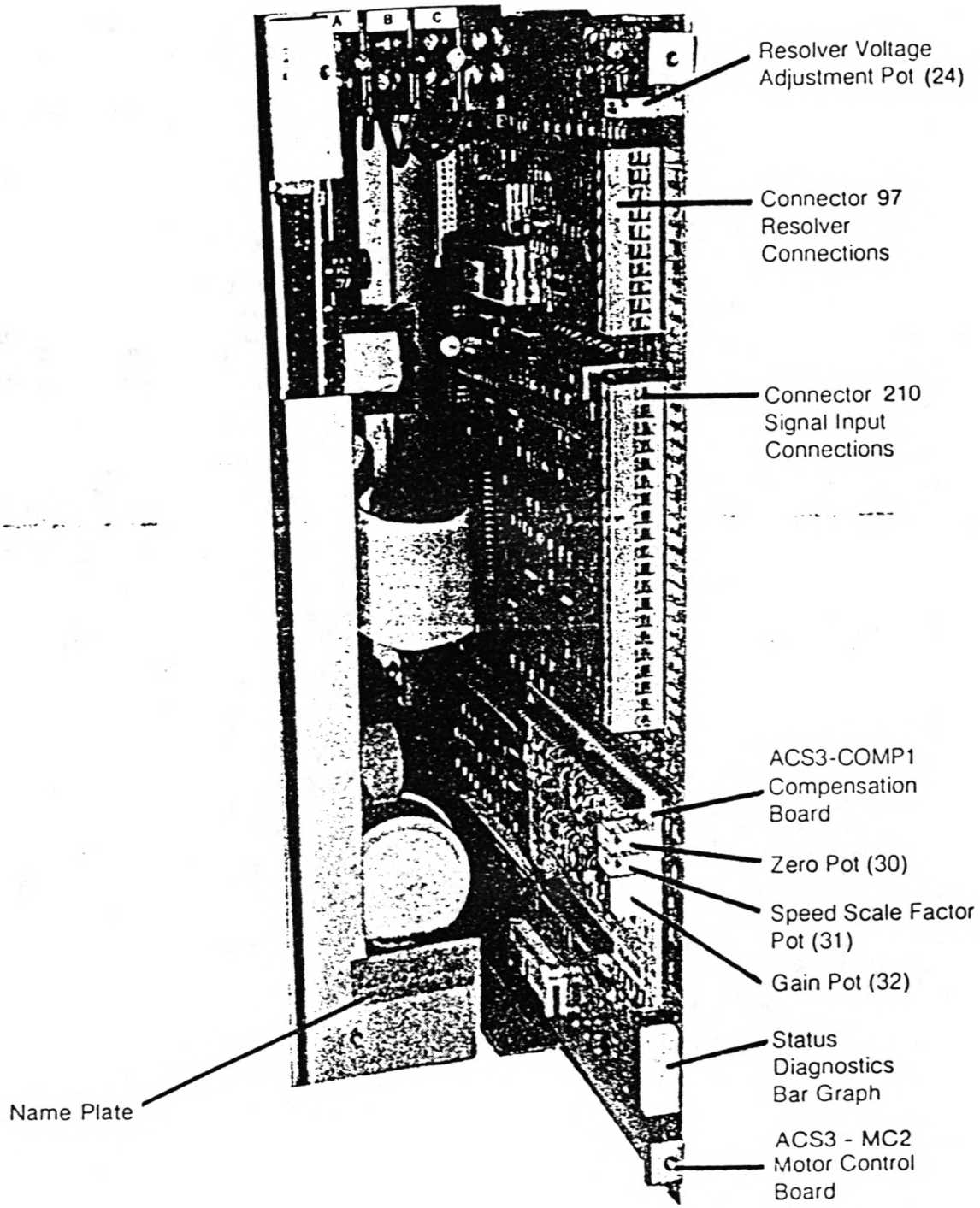
BDS3 - 55 AMP AND PSR3 - 75 AMP
(FRONT VIEW)
FIGURE 2



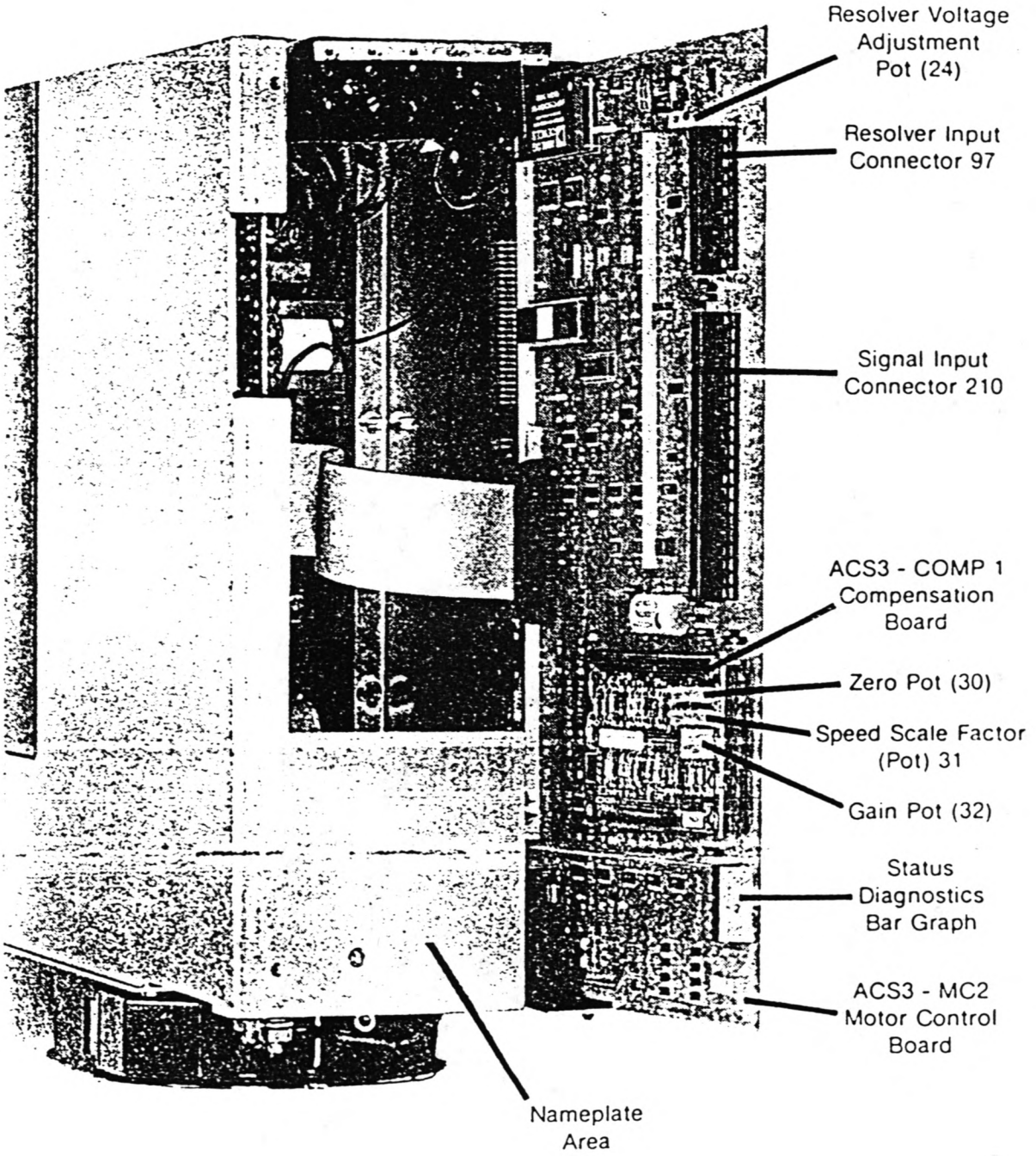
BDS3 - 12/20/30/40 AMP AND PSR3 - 25/50 AMP
(BOTTOM VIEW)
FIGURE 3



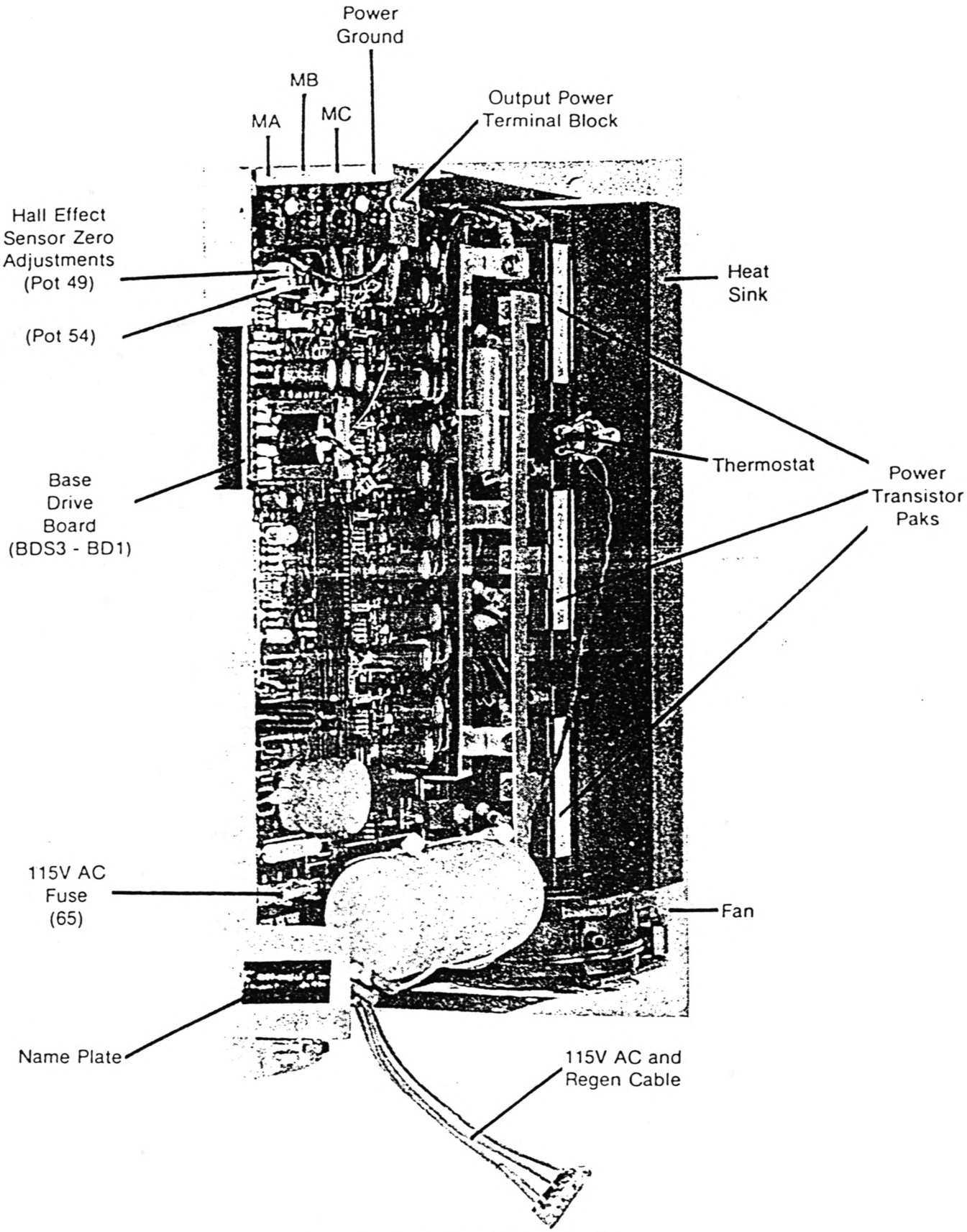
BDS3 - 55 AMP AND PSR3 - 75 AMP
(BOTTOM VIEW)
FIGURE 4



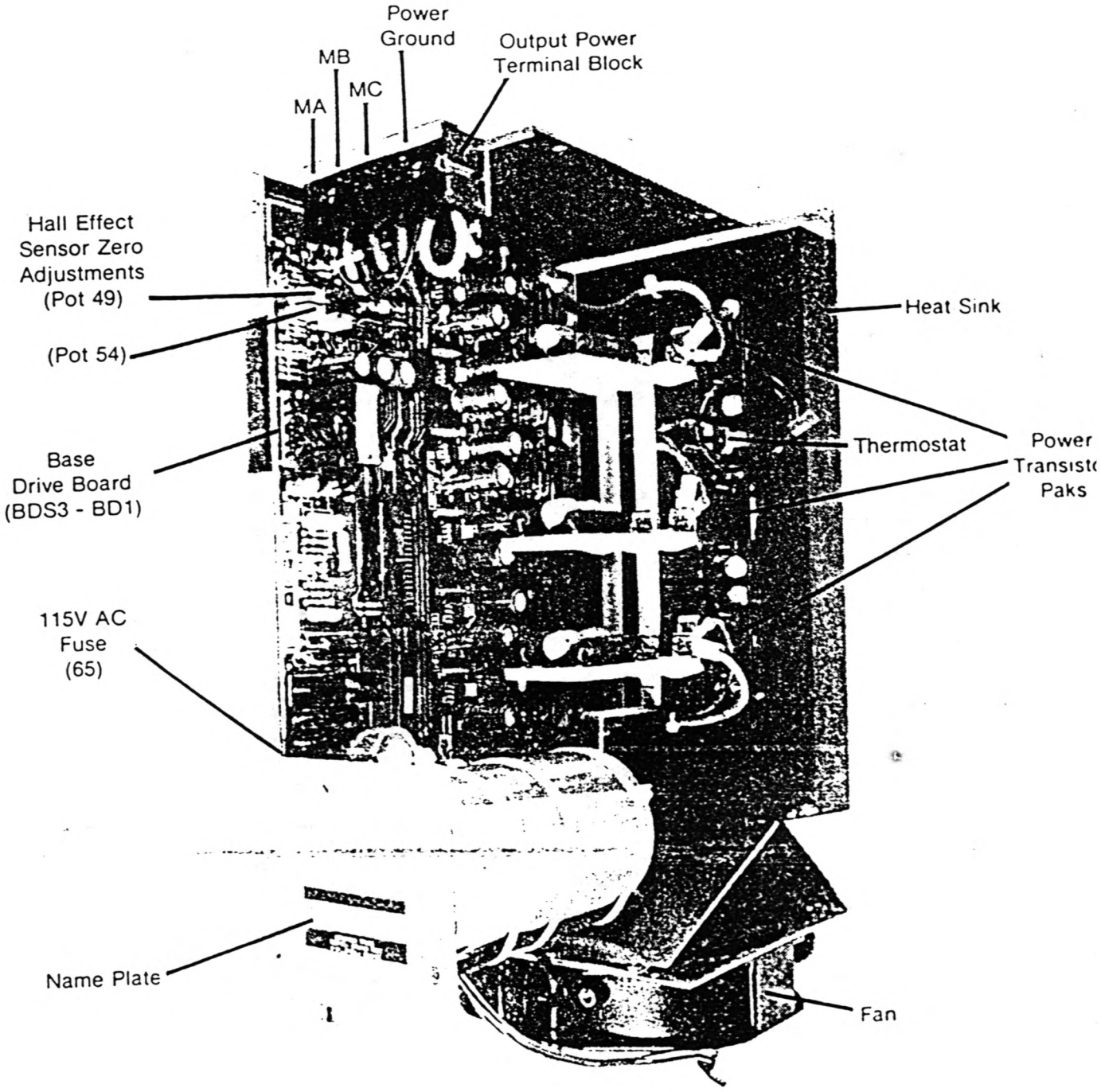
BDS3 - 12/20/30/40 AMP (RIGHT SIDE)
SHOWING ACS3 - MC2
MOTOR CONTROL BOARD
FIGURE 5



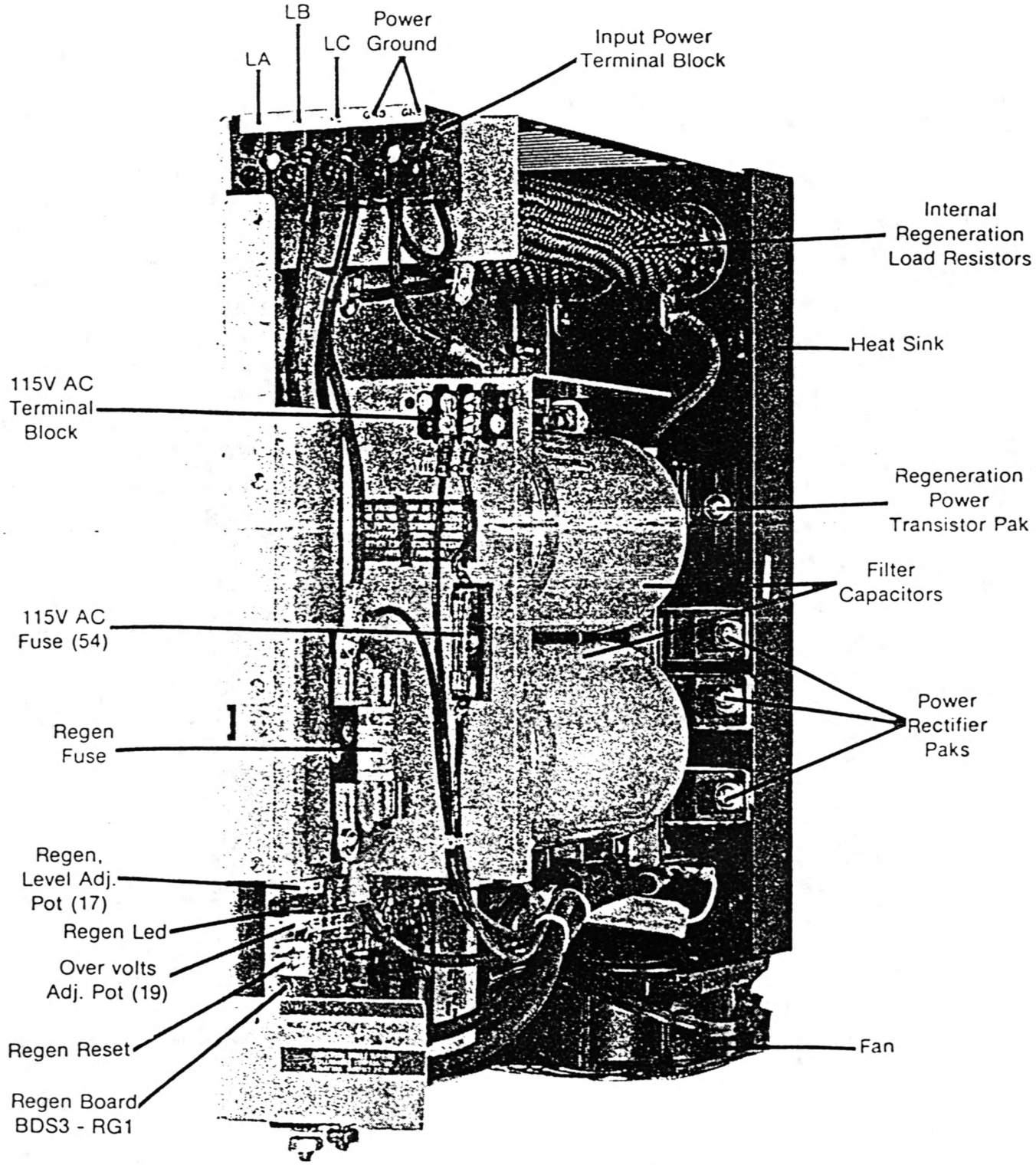
BDS3 - 55 AMP (RIGHT SIDE)
SHOWING ACS3 - MC2
MOTOR CONTROL BOARD
FIGURE 6



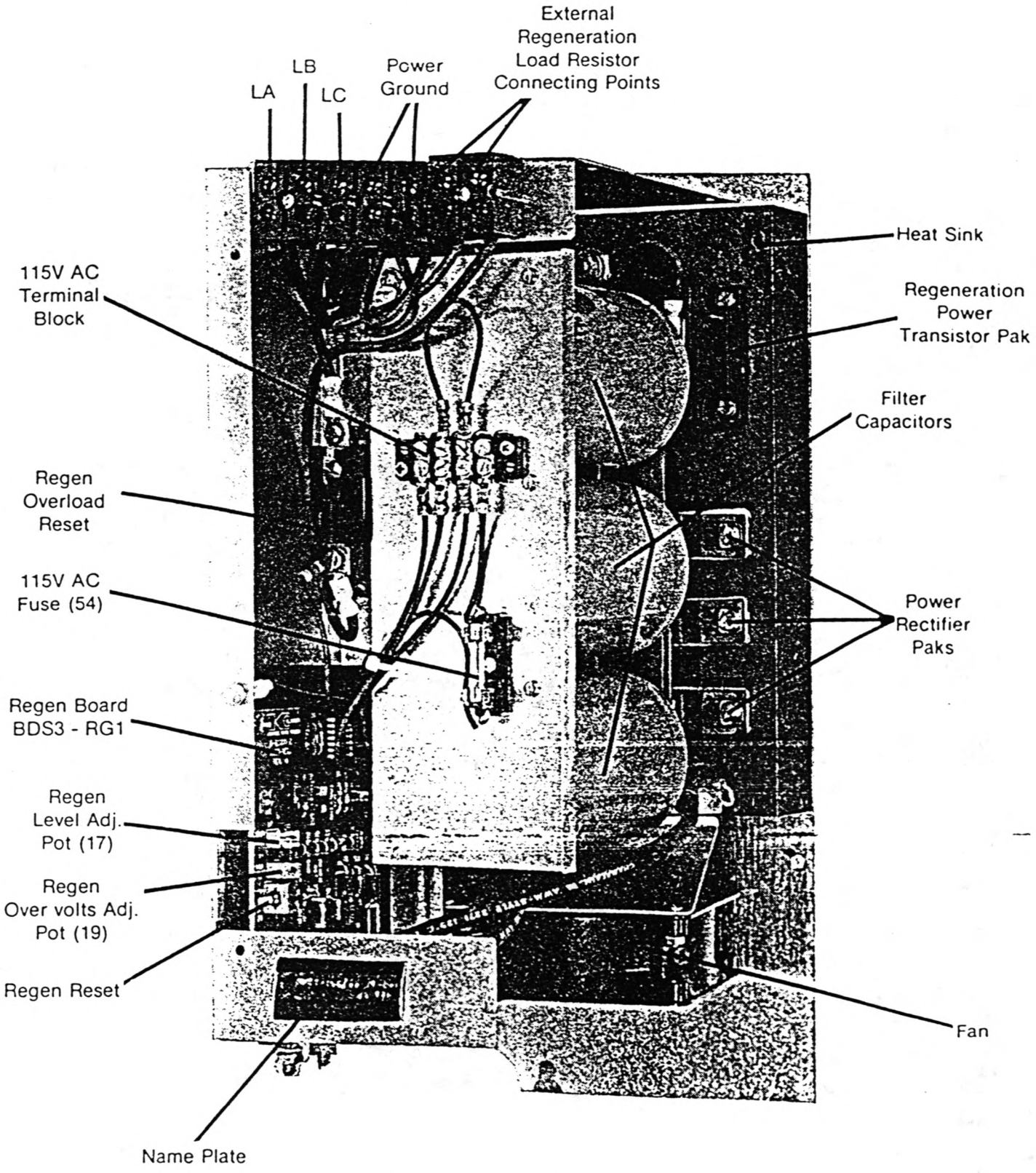
BDS3 - 12/20/30/40 AMP (LEFT SIDE)
SHOWING POWER STAGE WITH
BASE DRIVE BOARD
BDS3 - BD1
FIGURE 7



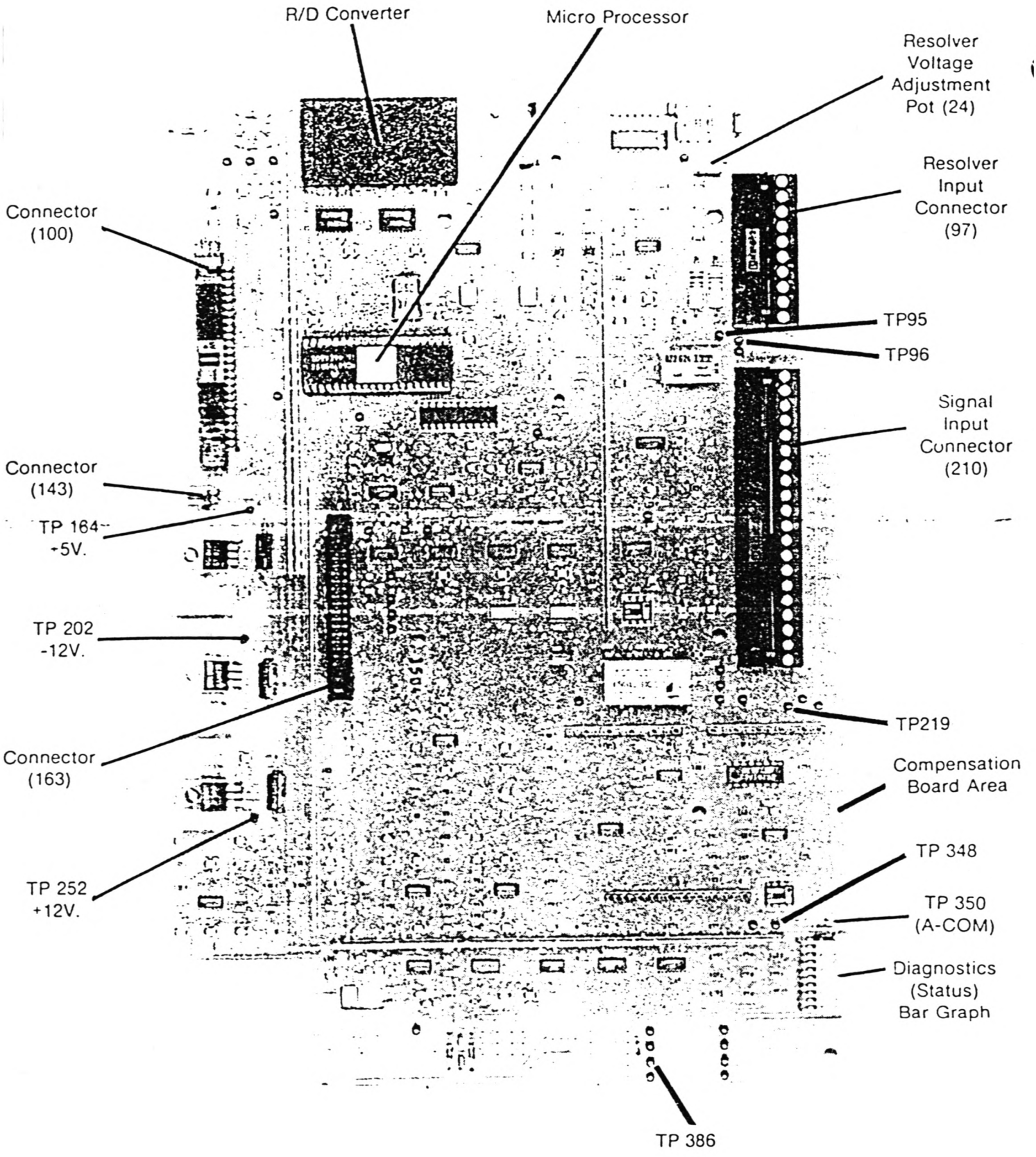
BDS3 - 55 AMP (LEFT SIDE)
SHOWING POWER STAGE WITH
BASE DRIVE BOARD
BDS3 - BD1
FIGURE 8



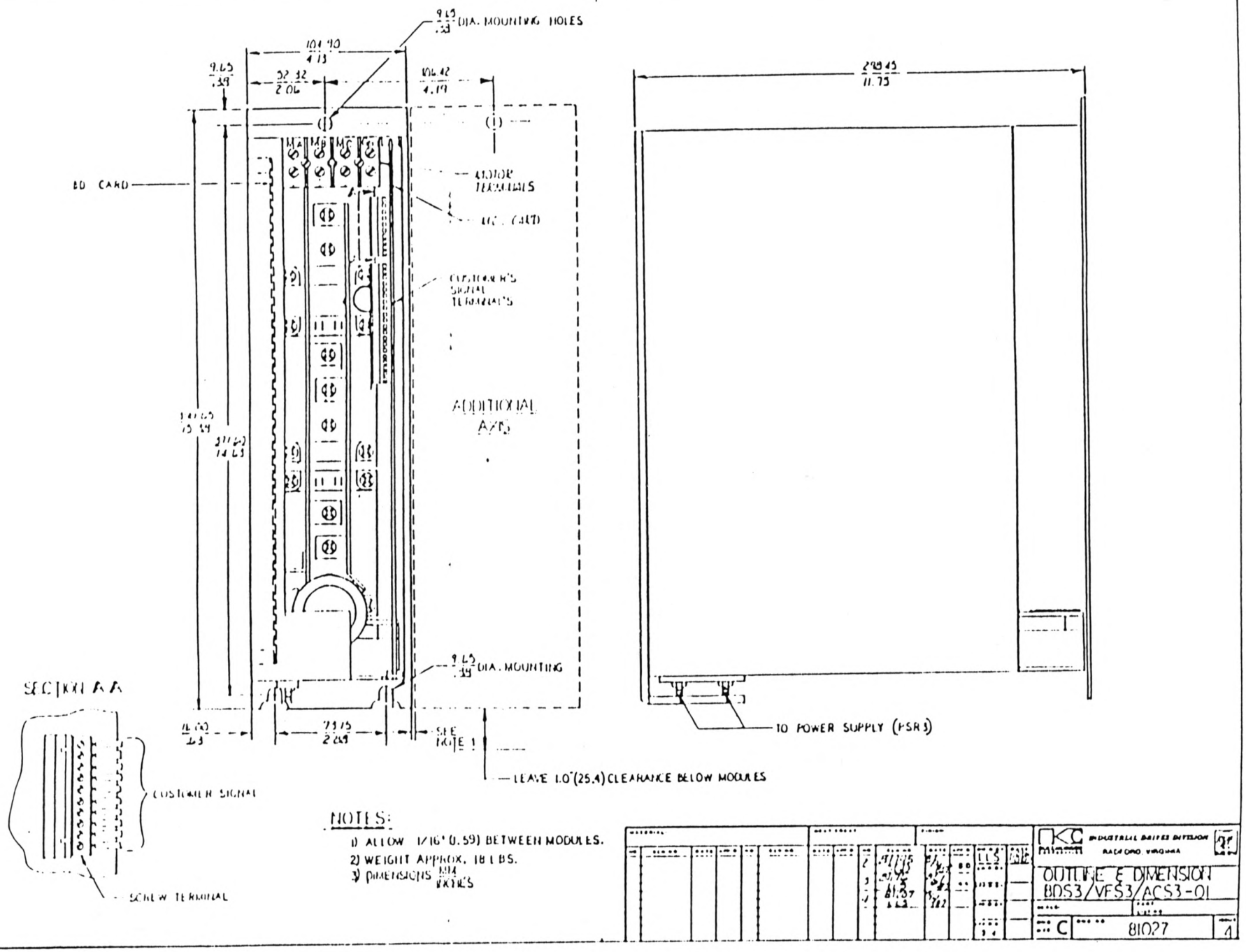
PSR3 - 25/50 AMP
POWER SUPPLY
(LEFT SIDE)
FIGURE 9

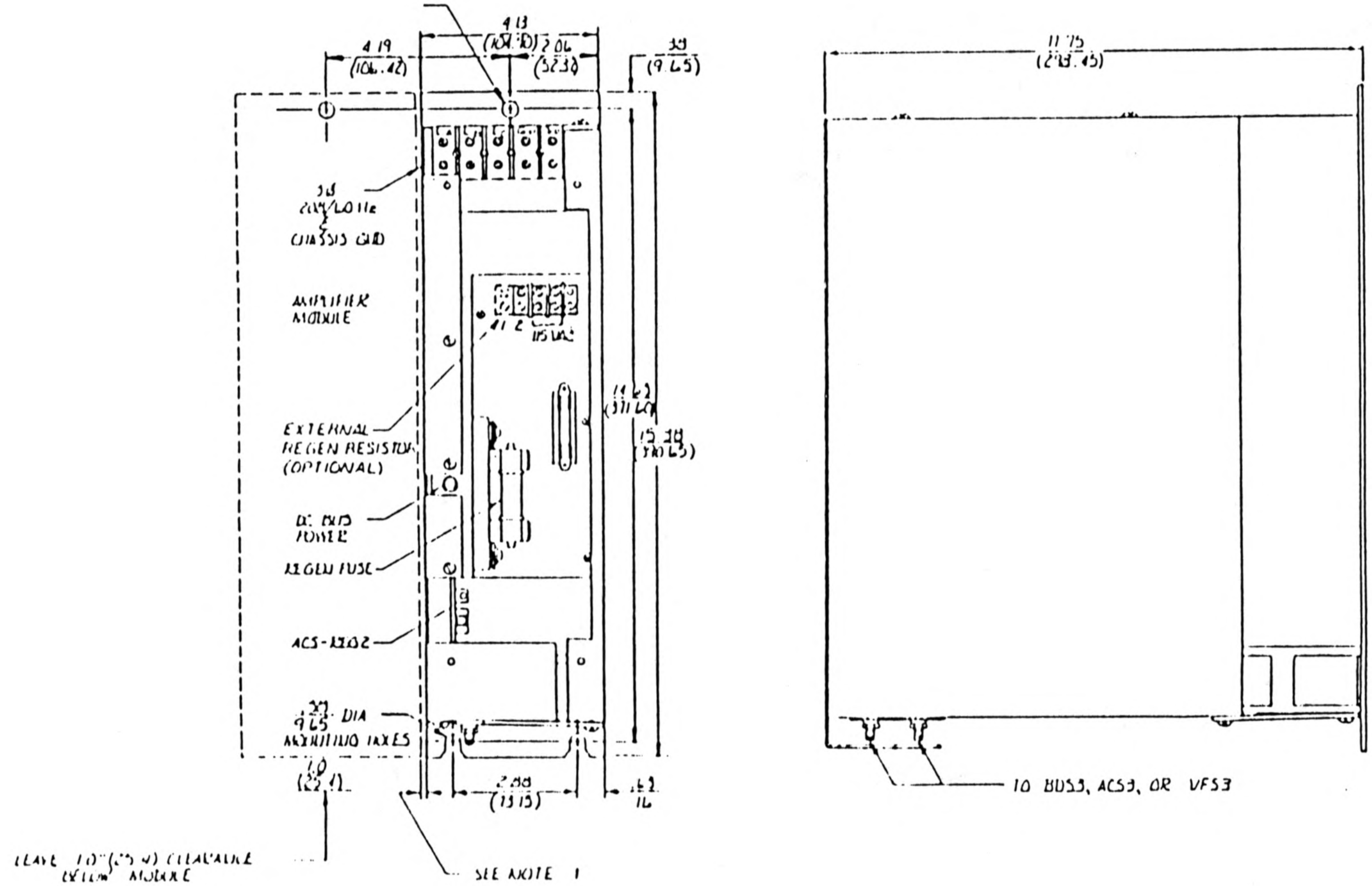


PSR3 - 75 AMP
POWER SUPPLY
(LEFT SIDE)
FIGURE 10



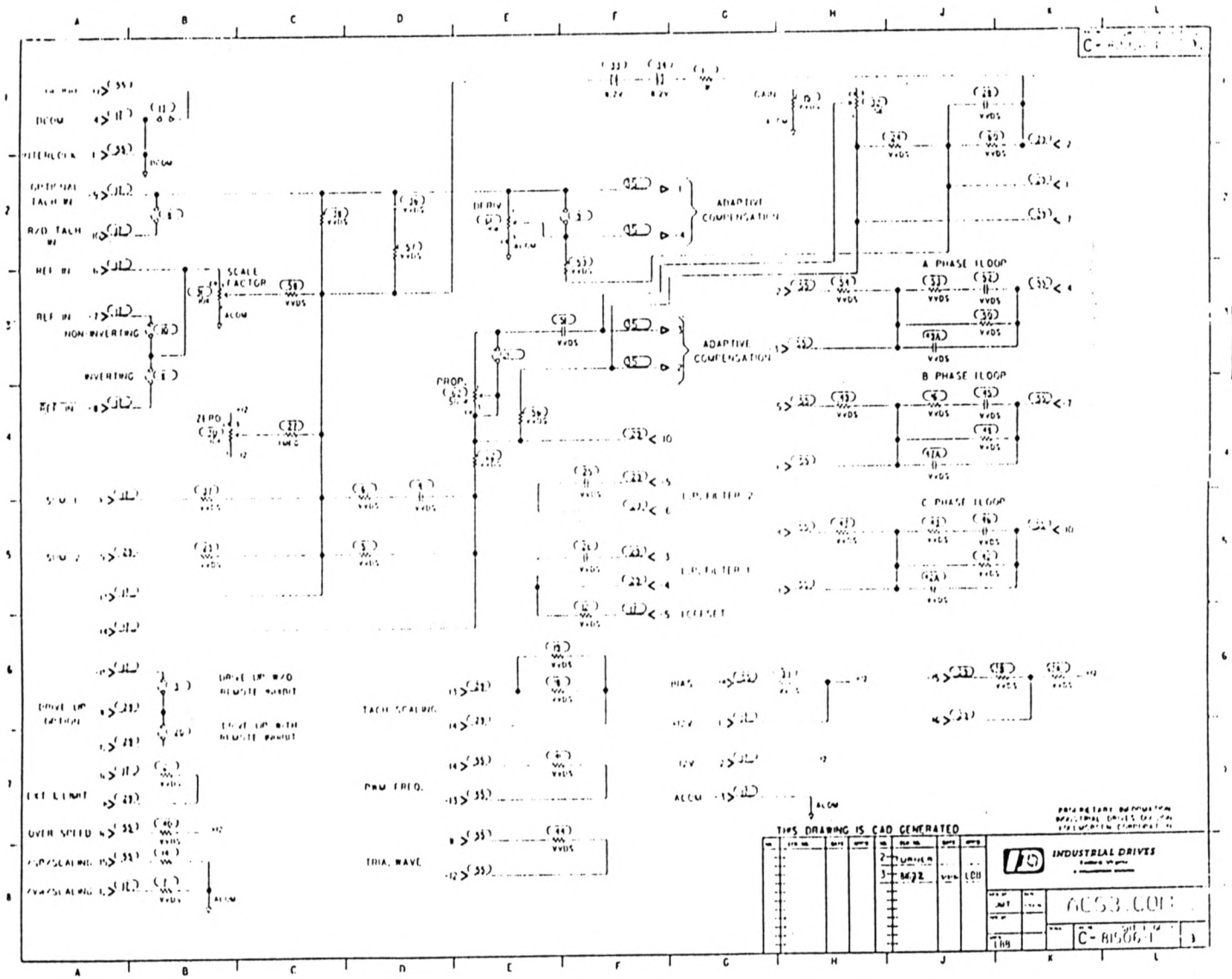
ACS3 - MC2
MOTOR CONTROL BOARD
FIGURE 11

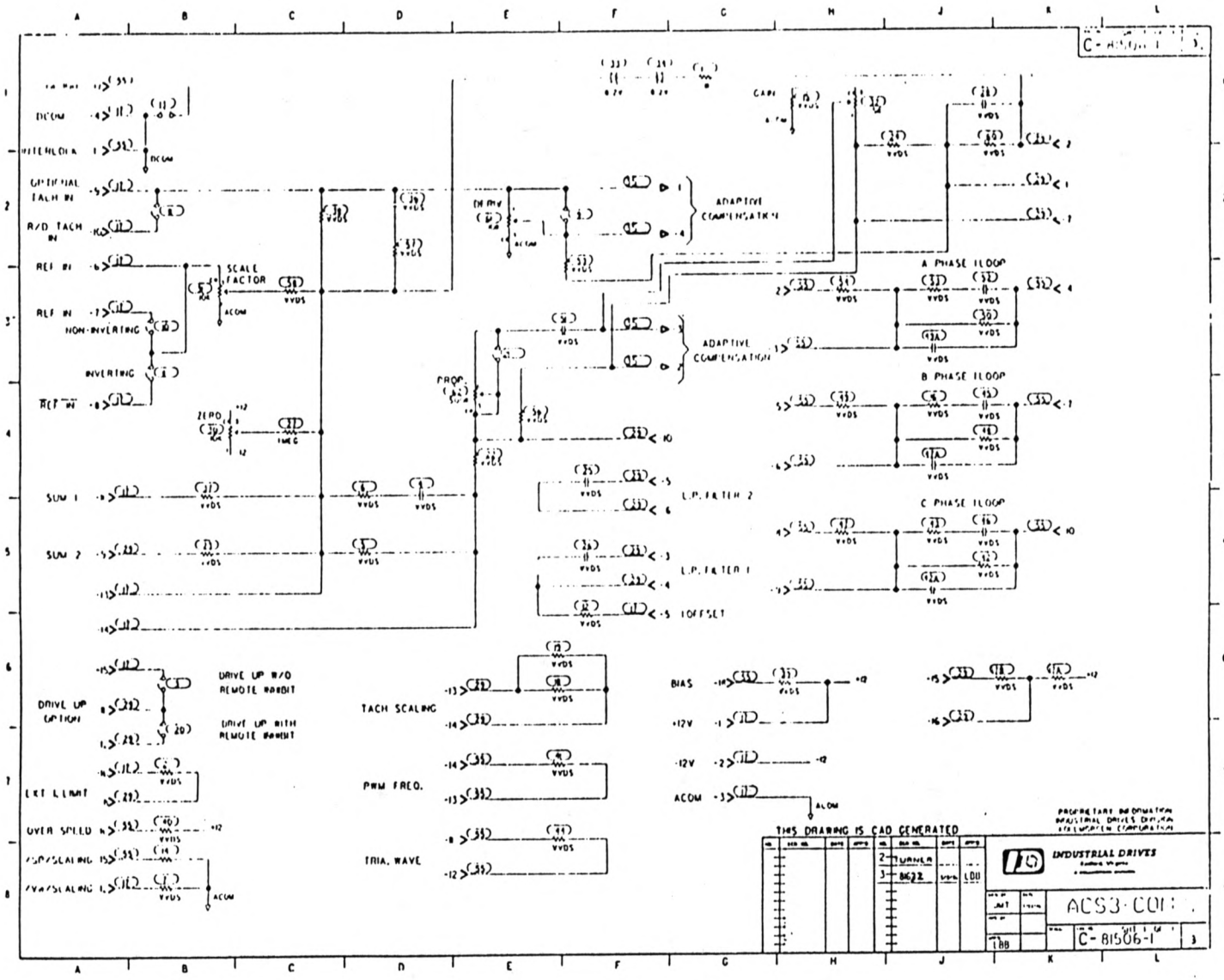

9.65 DIA. MOUNTING HOLES
BD CARD
ADDITIONAL AXES
9.65 DIA. MOUNTING
TO POWER SUPPLY (PSR3)
LEAVE 1.0"(25.4) CLEARANCE BELOW MODULES
SECTION A-A
CUSTOMER SIGNAL
SCREW TERMINAL
NOTES:
1) ALLOW 1/16" (1.59) BETWEEN MODULES.
2) WEIGHT APPROX. 18 LBS.
3) DIMENSIONS IN MM (INCHES)
OUTLINE & DIMENSION
BDS3/VFS3/ACS3-01
81027

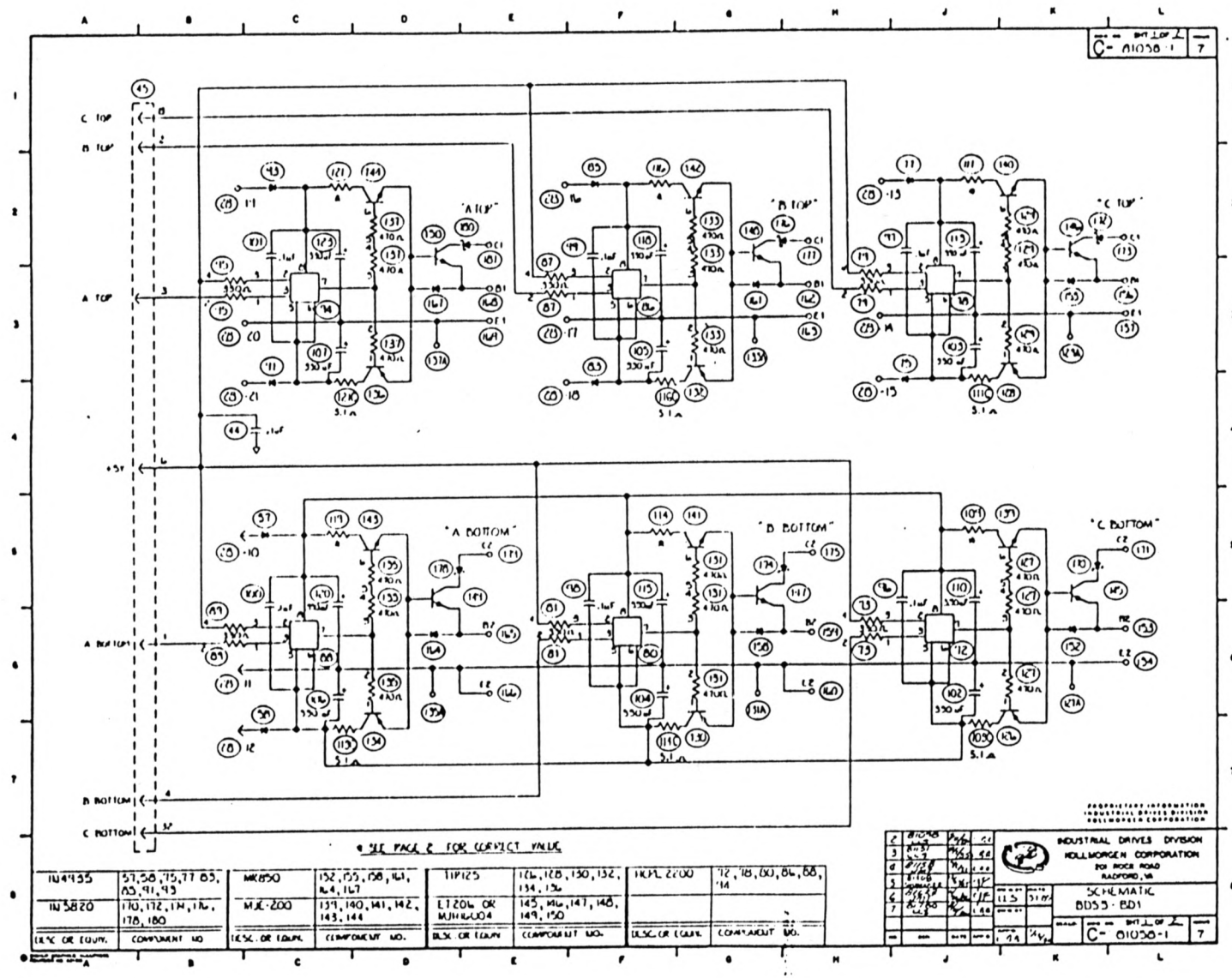


NOTES
1 ALLOW 1/16" (1.59) BETWEEN MODULES
2 WEIGHT APPROX. 21 LBS.
3 DIMENSIONS : INCHES (MM)

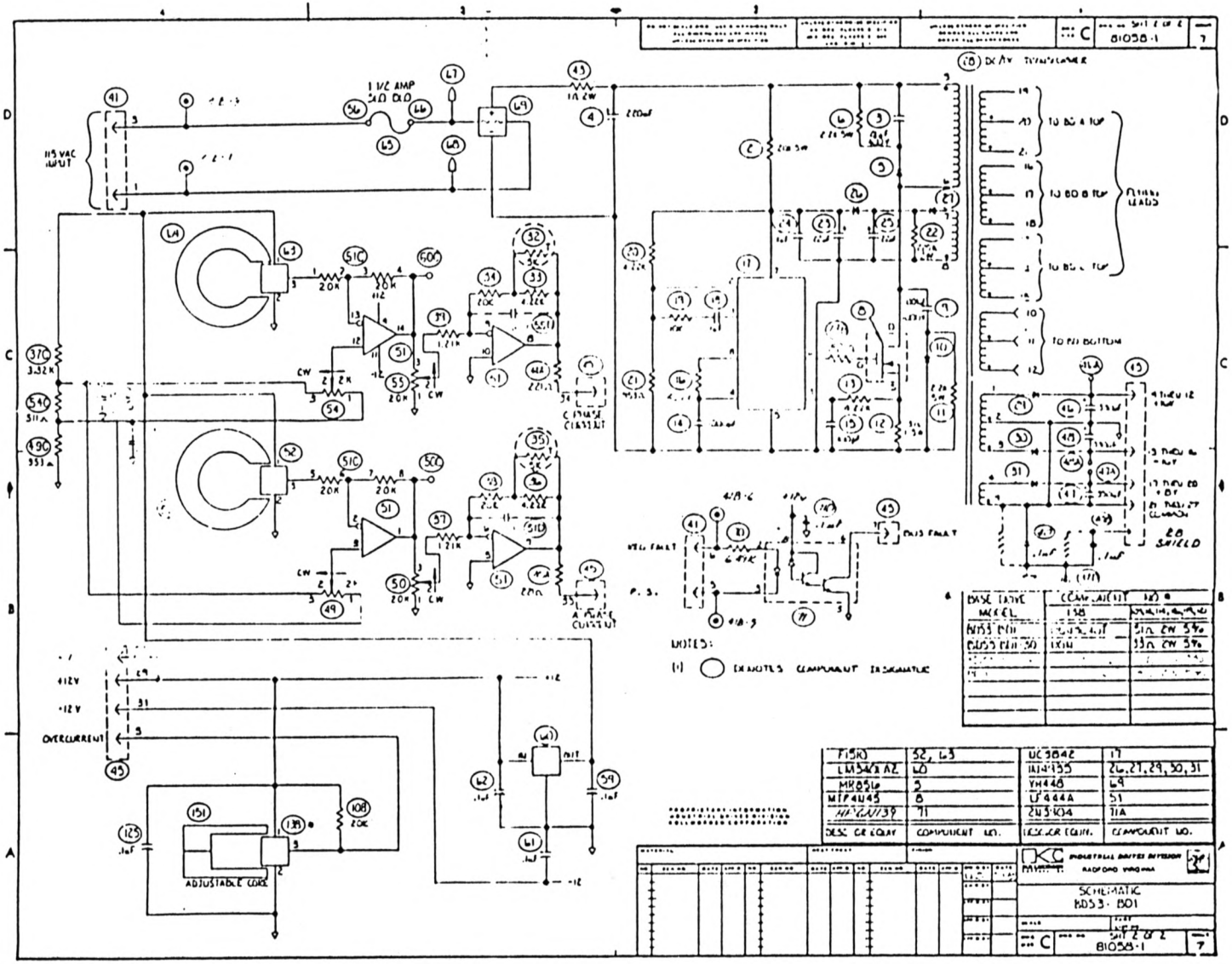
OUTLINE & DIMENSION
PSR 3-01
C 81056


SCALE FACTOR
ADAPTIVE COMPENSATION
ADAPTIVE COMPENSATION
A PHASE LOOP
B PHASE LOOP
C PHASE LOOP
INTEGRATOR 2
INTEGRATOR 1
OFFSET
DRIVE UP W/O REMOTE PERMIT
DRIVE UP WITH REMOTE PERMIT
TACH SCALING
PWM FREQ.
TRIA. WAVE
THIS DRAWING IS CAD GENERATED
INDUSTRIAL DRIVES
AC53.COM

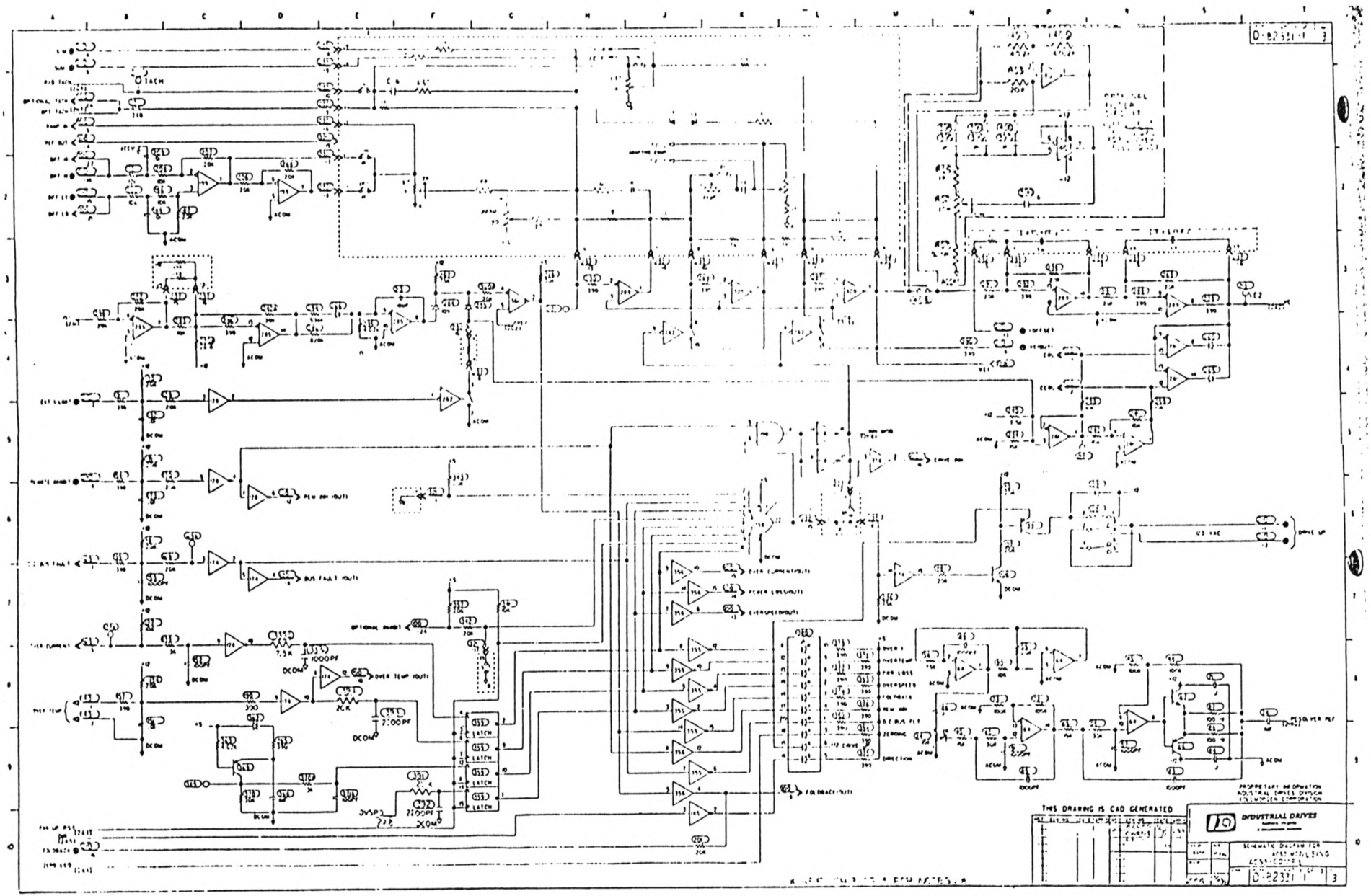

DCOM
INTERLOCK
OPTICAL TACH IN
R/D TACH IN
REF IN
REF IN
NON-INVERTING
INVERTING
REF IN
SCALE FACTOR
ACOM
ZERO
SUM 1
SUM 2
PROP
ADAPTIVE COMPENSATION
ADAPTIVE COMPENSATION
L.P. FILTER 2
L.P. FILTER 1
OFFSET
A PHASE LOOP
B PHASE LOOP
C PHASE LOOP
DRIVE UP OPTION
DRIVE UP W/O REMOTE PANEL
DRIVE UP WITH REMOTE PANEL
TACH SCALING
PWM FREQ.
TRIA. WAVE
BIAS
+12V
-12V
ACOM
THIS DRAWING IS CAD GENERATED
INDUSTRIAL DRIVES
ACS3-CON
C-81506-1

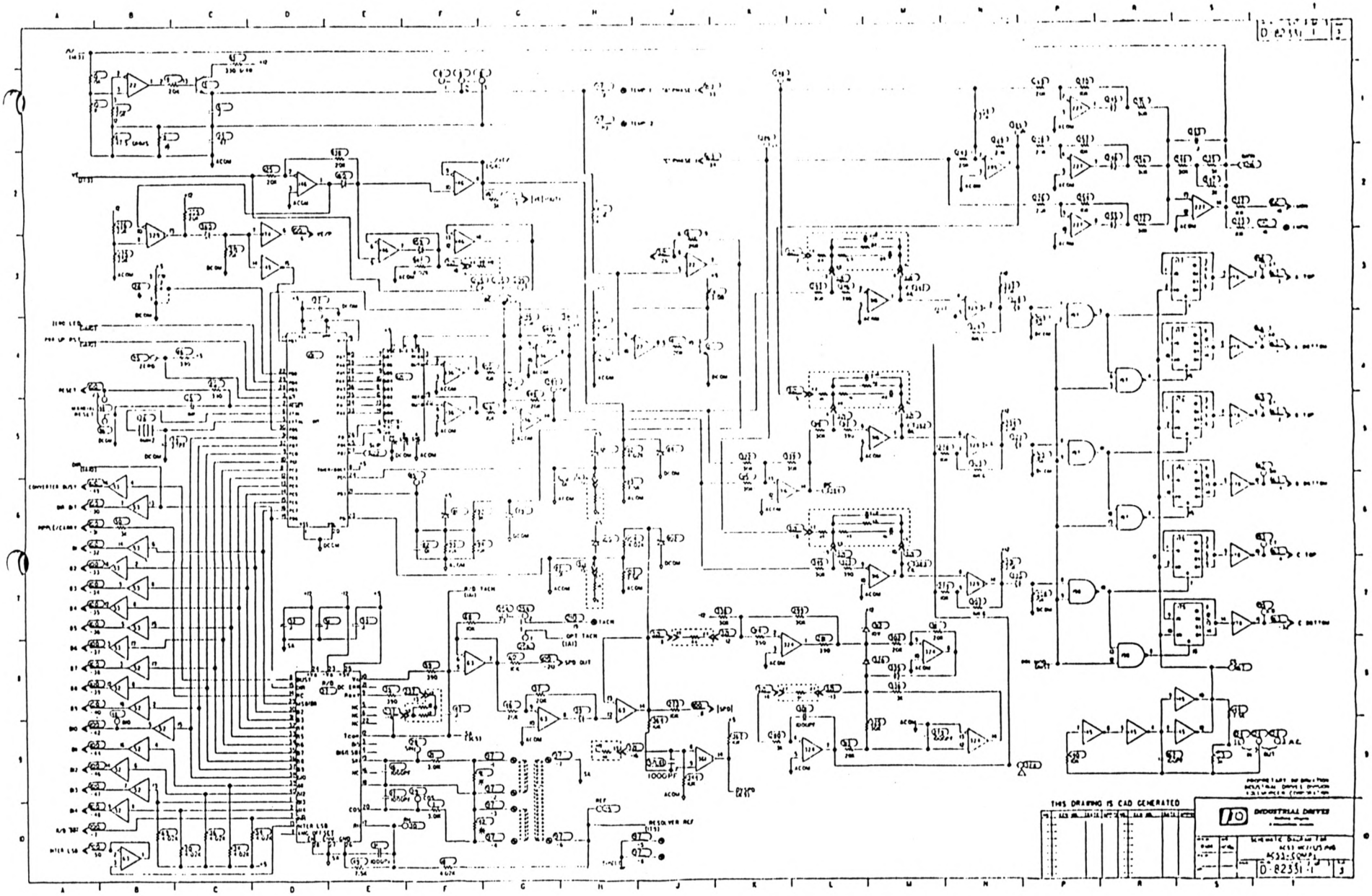


IN4935	57,58,75,77 83, 85,91,93	MR850	152,155,158,161, 164,167	TIP125	126,128,130,132, 134,136	TRPL 2200	72,78,80,84,88, 114
IN5820	170,172,174,176, 178,180	MJE-200	139,140,141,142, 143,144	LT204 OR MJH6004	145,146,147,148, 149,150		
DESC OR EQUIV.	COMPONENT NO	DESC. OR EQUIV.	COMPONENT NO.	DESC OR EQUIV.	COMPONENT NO.	DESC OR EQUIV.	COMPONENT NO.



FISRD	52, 63	UC3842	17
LM3403AZ	60	IRF9135	26, 27, 29, 30, 31
MR856	3	YH448	69
MTP4N45	8	LF444A	51
MMBZ5239	71	2N3904	114
DESC OR EQUIV	COMPONENT NO.	DESC OR EQUIV.	COMPONENT NO.




THIS DRAWING IS CAD GENERATED

NOTES:
1. COMPONENTS IN DOTTED LINES ARE ON ACSS-COMPI BOARD. P1.
* - NOT USED UNLESS CALLED FOR ON T.L.

THIS DRAWING IS CAD GENERATED

PROPRIETARY INFORMATION
INDUSTRIAL DRIVES DIVISION
EMERSON ELECTRIC CORPORATION

INDUSTRIAL DRIVES

SCHEMATIC DIAGRAM FOR
ACSS WITH USING
ACSS-COMPI

D-82[illegible]-1

3

INDUSTRIAL DRIVES
TEST LIMITS AND MODIFICATION DATA
BDS3-208/20

TL BDS3-208/20-3105A2
ISSUE 2 SH 1 OF 3
WRITTEN BY L. LESTER 12/3/86
APPROVED BY

MOTOR DATA:

MODEL BR-3105A
RATED SPEED 1450 RPM
RATED TORQUE 9.5 LB.FT
RATED CURRENT 6.5 AMPS RMS/PHASE
ROTOR INERTIA .00233 $lb.ft.sec^2$
LOAD INERTIA 0 - .012 $lb.ft.sec^2$

AMPLIFIER DATA:

CURRENT LIMIT SET FOR 35 AMPS RMS/PHASE (42 - 52 A. PK.)
EXTERNAL CURRENT LIMIT SET FOR 20 AMPS RMS/PHASE (26 - 30A. PK.)
OVERSPEED SET FOR 1875 RPM
TACH SCALED FOR 1800 RPM @ ±8 VOLTS
PWM FREQ. 4 KHZ
CURRENT MONITOR SET FOR 8V @ 35 AMPS RMS/PHASE (42 - 52A. PK.)
4.6V @ 20 AMPS RMS/PHASE (23 - 30A. PK.)

AMPLIFIER COMPENSATION: ACS3-COMP1

CURRENT LOOP COMP.

FEEDBACK R47,R49,R54 30.1K

A PHASE:	R50 2.7M5%	R53 499K	C52 330pf	C49A 100pf *
B PHASE:	R48 2.7M5%	R16 499K	C45 330pf	C47A 100pf *
C PHASE:	R42 2.7M5%	R43 499K	C46 330pf	C42A 100pf *

*SEE SPECIAL INSTRUCTIONS

VELOCITY LOOP COMP:

TACH INPUT SELECTION:	J8 IN			
TACH SCALING:	R18 2.74K	R19 18.2K		
REFERENCE INPUT POLARITY:	J10 IN	J11 OPEN		
SUM 1 INPUT:	R37 15K	SUM 2 INPUT:	R23 20K	
REFERENCE INPUT:	R58 15K			
ADJUST SCALE FACTOR POT:	P31 FOR -0- OHMS BETWEEN 17-6 AND WIPER OF POT.			
SUM STAGE:	R38 20K	R57 OPEN	C36 OPEN	
	R5 20K	R6 OPEN	C4 OPEN	
PROPORTIONAL STAGE:	R22 82.5K	R56 OPEN	J21 IN	
		C51 0.1mf		

NOTE: ALL RESISTORS 1/8W, 1% AND CAPS 5% UNLESS OTHERWISE SPECIFIED. 1/4W, 1% MAY BE SUBSTITUTED IF 1/8W, 1% NOT AVAILABLE.

ECN: (2) 81917 12/3/86 LDL:

INDUSTRIAL DRIVES
TEST LIMITS AND MODIFICATION DATA
BDS3-208/20

TL BDS3-208/20-3105A2
ISSUE 2 SH 2 OF 3

GAIN STAGE: R15 511 OHMS
ADJUST GAIN POT P32 FOR 2.5K OHMS BETWEEN 35-2 & 35-3.

DERIVATIVE STAGE: R59 22.1K J9 IN R24 20K
R60 150K C28 220pf

LOW PASS FILTER: C25 .015mf C26 .015mf

DRIVE UP OPTION: J3 OPEN J20 IN

EXTERNAL CURRENT LIMIT: R2 6.49K

OVERSPEED: R40 3.74K

|SPEED| SCALING: R14 6.81K

|VELOCITY ERROR| SCALING: R7 ZERO OHMS

PWM FREQUENCY: R41 75K

TRIANGLE WAVE REDUCTION: R44 OPEN

I OFFSET: R12 10K

OPT. INHIBIT: J13 IN

BIAS: R39 OPEN

FOLDBACK: R17A OPEN R17B 5.62K

BDS3-MC1 COMPENSATION VALUES:

MICROPROCESSOR, IC54, PROGRAM A79776- 18 -LATEST REVISION

ACS3-MC2 COMPENSATION VALUES:

MICROPROCESSOR, IC101, PROGRAM A79776-26-LATEST REVISION

TEMPERATURE COMPENSATION R9 OPEN J8 2 - 3

OPTIONAL TACH SELECT J25A 2 - 3

CLOCK FREQUENCY J124 2 - 3

ACS OR BDS J205 1 - 2

FILTER: J408 IN J398 OUT
J399 OUT J400 OUT

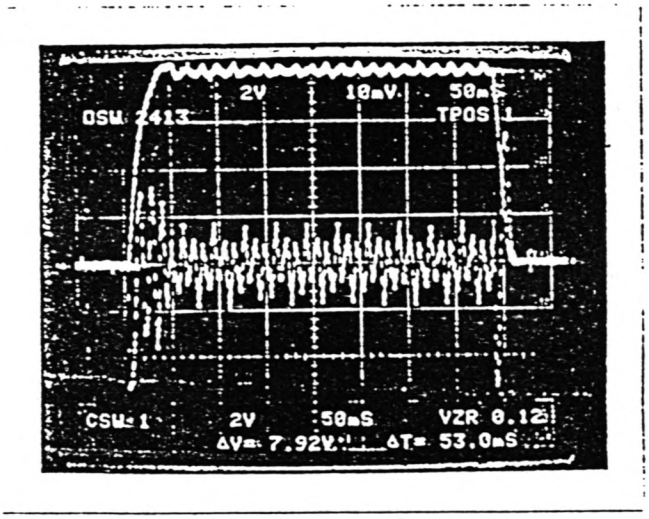
SPECIAL INSTRUCTIONS AND COMMENTS:

*WHEN ACS3-COMP1; REV. 2 BOARDS ARE USED, C49A, C47A & C43A WILL BE INSTALLED IN PARALLEL WITH R42, R48, & R50.

ACCEL/DECEL
@ 1800 RPM

LOAD INERTIA
0.00233 LB.FT.SEC^2

20 A/DIV.



Stamp ACS3-COMP1 Card, in box provided, with amplifier current rating and motor compensation.

Example: 20-3105A2-2

INDUSTRIAL DRIVES
TEST LIMITS AND MODIFICATION DATA

TL BDS3-208/12-2102A22
ISSUE 1 SH 1 OP 3
WRITTEN BY L. LESTER 12/15/86
APPROVED BY

MOTOR DATA:

MODEL BR-2102A
RATED SPEED 6260 RPM
RATED TORQUE 2.6 LB.FT
RATED CURRENT 4.2 AMPS RMS/PHASE
ROTOR INERTIA 0.000236 $lb.ft.sec^2$
LOAD INERTIA 0.10 $lb.ft.sec^2$

AMPLIFIER DATA:

CURRENT LIMIT SET FOR 21 AMPS RMS/PHASE (28 - 32 A. PK.)
EXTERNAL CURRENT LIMIT SET FOR 12 AMPS RMS/PHASE (16 - 18A. PK.)
OVERSPEED SET FOR 560 RPM
TACH SCALED FOR 500 RPM @ ±8 VOLTS
PWM FREQ. 4 KHZ
CURRENT MONITOR SET FOR 8V @ 21 AMPS RMS/PHASE (28 - 32 A. PK.)
4.6V @ 12 AMPS RMS/PHASE (16 - 18 A. PK.)

AMPLIFIER COMPENSATION: ACS3-COMP1

CURRENT LOOP COMP.

FEEDBACK R47,R49,R54 30.1K

A PHASE:	R50 2.7M,5%	R53 332K	C52 4700pf	C49A 100pf *
B PHASE:	R48 2.7M,5%	R16 332K	C45 4700pf	C47A 100pf *
C PHASE:	R42 2.7M,5%	R43 332K	C46 4700pf	C42A 100pf *

*SEE SPECIAL INSTRUCTIONS

VELOCITY LOOP COMP:

TACH INPUT SELECTION:	J8 IN			
TACH SCALING:	R18 249 OHMS	R19 OPEN		
REFERENCE INPUT POLARITY:	J10 IN	J11 OUT		
SUM 1 INPUT:	R37 15K	SUM 2 INPUT:	R23 20K	
REFERENCE INPUT:	R58 15K			
ADJUST SCALE FACTOR POT:	P31 FOR ZERO OHMS BETWEEN 17-6 AND WIPER OF POT.			
SUM STAGE:	R38 20K	R57 OPEN	C36 OPEN	
	R5 20K	R6 OPEN	C4 OPEN	
PROPORTIONAL STAGE:	R22 475K	R56 OPEN	J21 IN	
		C51 0.1 mf		

NOTE: ALL RESISTORS 1/8W, 1% AND CAPS 5% UNLESS OTHERWISE SPECIFIED. 1/4W, 1% MAY BE SUBSTITUTED IF 1/8W, 1% IS NOT AVAILABLE.

ECN: _____

INDUSTRIAL DRIVES
TEST LIMITS AND MODIFICATION DATA

TL BDS3-208/12-2102A22
ISSUE 1 SH 2 OF 3

GAIN STAGE: R15 511 OHMS
ADJUST GAIN POT P32 FOR 2.5K OHMS BETWEEN 35-2 & 35-3.

DERIVATIVE STAGE: R59 22.1K J9 IN R24 20K
R60 1.5 MEG C28 560pf

LOW PASS FILTER: C25 0.068mf C26 0.068mf

DRIVE UP OPTION: J3 OUT J20 IN

EXTERNAL CURRENT LIMIT: R2 6.49K

OVERSPEED: R40 3.32K

|SPEED| SCALING: R14 182 OHMS

|VELOCITY ERROR| SCALING: R7 1.0K

PWM FREQUENCY: R41 75K

TRIANGLE WAVE REDUCTION: R44 OPEN

I OFFSET: R12 10K

OPT. INHIBIT: J13 IN

BIAS: R39 OPEN

FOLDBACK: R17A OPEN R17B 13K

BDS3-MC1 COMPENSATION VALUES:

MICROPROCESSOR, IC54, PROGRAM A79776- 15 LATEST REVISION

ACS3-MC2 COMPENSATION VALUES:

MICROPROCESSOR, IC101, PROGRAM A79776- 24 LATEST REVISION

TEMPERATURE COMPENSATION R9 OPEN J8 2 - 3

OPTIONAL TACH SELECT J25A 2 - 3

CLOCK FREQUENCY J124 2 - 3

ACS OR BDS J205 1 - 2

FILTER: J408 IN J398 OUT
J399 OUT J400 OUT

INDUSTRIAL DRIVES
TEST LIMITS AND MODIFICATION DATA

TL BDS3-208/12-2102A22
ISSUE 1 SH 3 OF 3

SPECIAL INSTRUCTIONS AND COMMENTS:

*WHEN ACS3-COMP1; REV.2 BOARDS ARE USED, C49A, C47A, & C43A WILL BE INSTALLED IN PARALLEL WITH R42, R48, & R50.

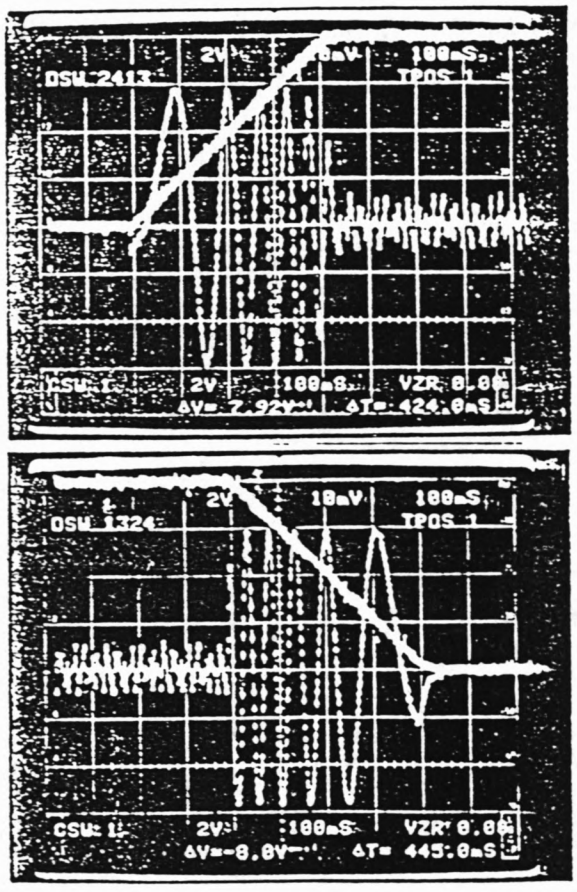
NOTE: **This system will be unstable without the stated load inertia.**

ACCEL
@ 500 RPM

LOAD INERTIA
0.1 LB.FT.SEC^2

10 A/DIV.

DECEL
@ 500 RPM



100 MS./DIV.

Stamp ACS3-COMP1 Card, in box provided, with amplifier current rating and motor compensation.

Example: 12-2102A22-1

INDUSTRIAL DRIVES
Radford, Virginia
A KOLLMORGEN DIVISION

CD 25712 ISSUE 4
WRITTEN REV 4-96 APPROVED 12RF4/96
SHEET 1 OF 2

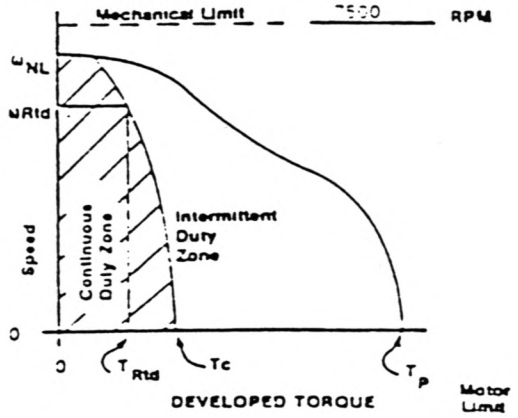
BRUSHLESS SERVO MOTOR 2102 SERIES

MOTOR PARAMETERS / **WINDING DATA**

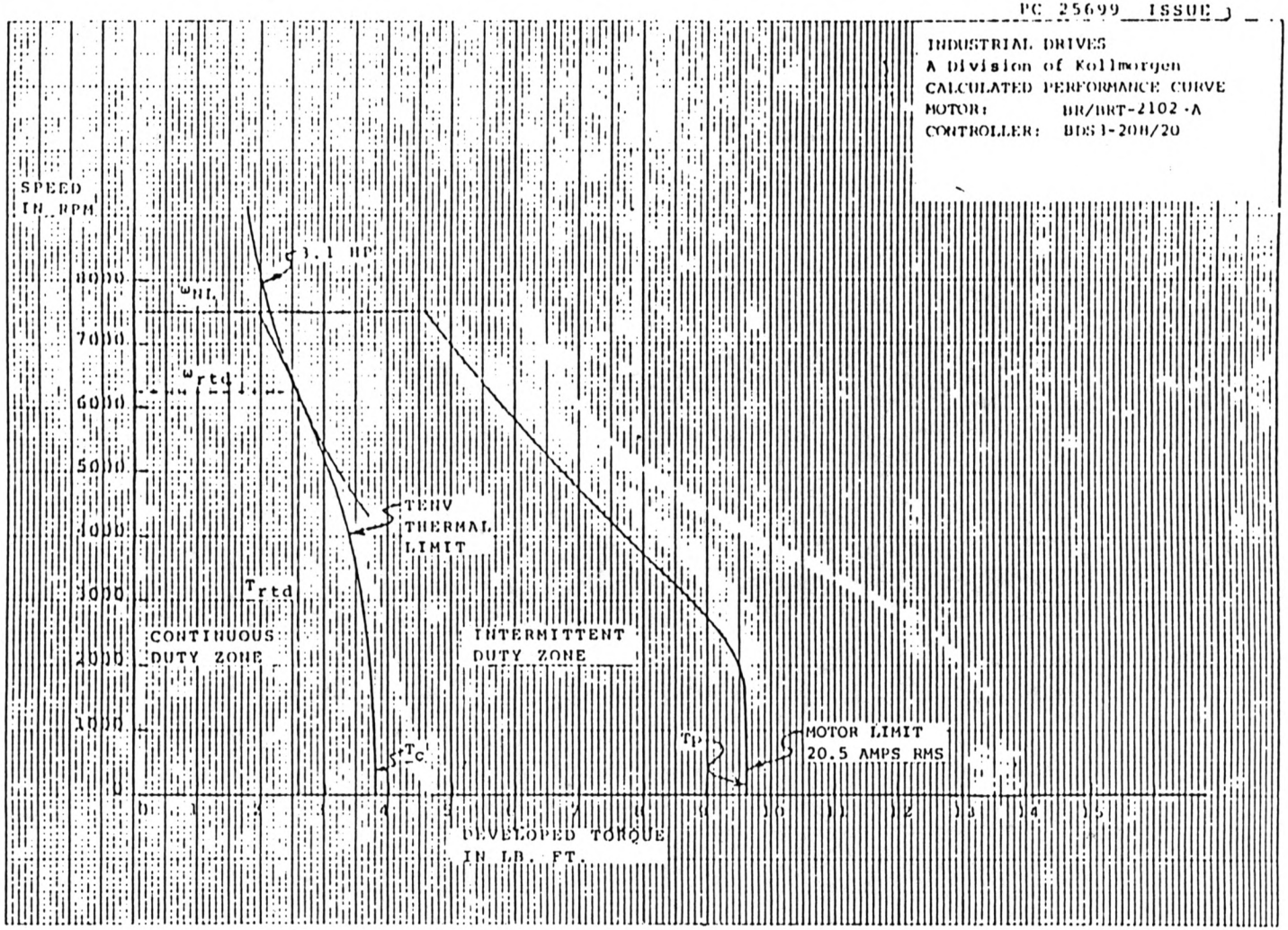
	Tol.	Symbol	Units	A	B	C	D	E
Horsepower	Rated	Hp Rtd	HP	3.1	4.0	4.7		
Speed	Rated	ω Rtd	RPM	6260	7500	7500		
Torque	Rated	T Rtd	lb • ft / N • m	2.6 / 3.5	2.8 / 3.8	3.3 / 4.5		
Line Current	Rated	I Rtd	amps RMS	4.2	7.6	13.7		
Volts (line to line)	Rated	V Rtd	Volts RMS	210	210	210		
Continuous Torque (Stall) @ 40° C Ambient	Nom.	TC	lb • ft / N • m	3.8 / 5.2	3.9 / 5.3	3.9 / 5.3		
Cont. Line Current	Nom.	IC	amps RMS	6.3	10.5	16.2		
Peak Torque	Nom.	Tp	lb • ft / N • m	9.6 / 13.0	9.4 / 12.8	9.7 / 13.2		
Peak Line Current	Nom.	Ip	amps RMS	20.5	33.0	52.5		
Theoretical Acceleration	Nom.	α m	rad/sec²	40750	39750	41000		
Torque Sensitivity	± 10%	Kt	lb • ft/amp RMS / N • m/amp RMS	0.60 / 0.82	0.37 / 0.51	0.24 / 0.32		
Back EMF (line-to-line)	± 10%	KB	V/KRPM	29.2	20.3	19.7		
No Load Operating Speed	Nom.	ω NL	RPM	7500	7500	7500		
Max Line to Line Volts	Max	V Max	Volts RMS	250	250	250		
DC Res @ 25°C (line-to-line)	± 10%	RM	Ohms	1.9	0.75	0.30		
Inductance (line-to-line)	± 30%	LM	mH	17.3	6.9	2.9		
Time Constant Mech @ 25° C Elec	Nom	TM	msec	1.4	1.4	1.4		
	Nom	TE	msec	9.1	9.1	9.1		
Motor Operating Characteristics Curve			PC-					
Motor Cycle Curve for Intermittent Operation			PC-					
Motor Temperature Rise Curve			PC-					
System Performance Curve			PC-	25699	25700	25701		

	Symbol	Units	Value
Rotor Inertia	JM	lb • ft • sec² / kg • m²	0.000236 / 0.000320
Weight	Wt	lb / kg	20.5 / 9.3
Static Friction	TF	lb • ft / N • m	0.020 / 0.027
Thermal Time Constant	TCT	minutes	130
Viscous Damping ∞ Z Source	FI	lb • ft/KRPM / N • m/KRPM	0.0083 / 0.0110

ISS.	ECN #	DATE	APP'D	ISS.	ECN #	DATE	APP'D
2	ADD PC #'s	8/21/85					
3	24283	3/5/86					
4	24693	12/12/86					



PC 25699 ISSUE



Leon Reiss 8/6/84

INDUSTRIAL DRIVES

A KOLLMORGEN DIVISION

CD 25993 ISSUE 2

WRITTEN J.S. 9-85 APPROVED [illegible] 55

SHEET 1 OF 2

BRUSHLESS SERVO MOTOR BR-3105

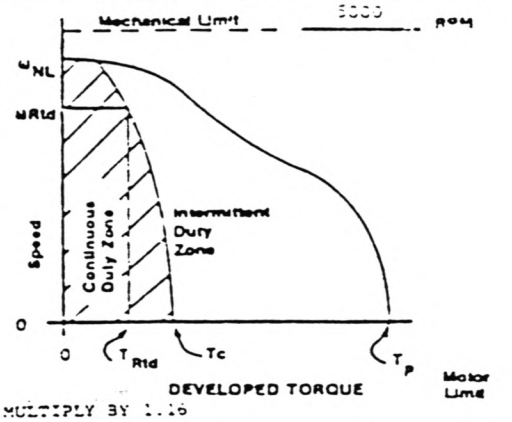
MOTOR PARAMETERS — **WINDING DATA**

		Tol.	Symbol	Units	A	B	C	D	E
*Horsepower		Rated	Ho Rtd	HP	2.6	4.7	3.5		
Speed		Rated	ω Rtd	RPM	1450	2900	2150		
*Torque		Rated	T Rtd	lb • ft	9.5	8.5	8.5		
				N • m	12.88	11.531	11.531		
Line Current		Rated	I Rtd	amps RMS	6.5	11.6	9.0		
Volts (line to line)		Rated	V Rtd	Volts RMS	210	210	210		
*Continuous Torque (Stall) @ 40° C Ambient		Nom.	TC	lb • ft	10.4	10.4	10.4		
				N • m	14.1	14.1	14.1		
Cont. Line Current		Nom.	IC	amps RMS	7.2	14.3	11.1		
Peak Torque		Nom.	Tp	lb • ft	50	50	50		
				N • m	68	68	68		
Peak Line Current		Nom.	Ip	amps RMS	35	70	54		
Theoretical Acceleration		Nom.	α m	rad/sec²	21,460	21,460	21,460		
*Torque Sensitivity		± 10%	Kt	lb • ft/amp RMS	1.46	0.73	.84		
				N • m/amp RMS	1.98	0.99	1.14		
*Back EMF (line-to-line)		± 10%	KB	V/KRPM	119	59.5	76.5		
No Load Operating Speed		Nom.	ω NL	RPM	1850	3600	2600		
Max Line to Line Volts		Max	V Max	Volts RMS	250	250	250		
DC Res @ 25°C (line-to-line)		± 10%	RM	Ohms	4.0	1.00	1.7		
Inductance (line-to-line)		± 30%	LM	mH	5.6	1.40	2.3		
Time Constant @ 25° C	Mech	Nom	TM	msec	4.9	4.9	4.9		
	Elec	Nom	TE	msec	1.4	1.4	1.4		

Motor Operating Characteristics Curve	PC-	
Motor Cycle Curve for Intermittent Operation	PC-	
Motor Temperature Rise Curve	PC-	
System Performance Curve	PC-	25994 25823

	Symbol	Units	value
Rotor Inertia	JM	lb • ft • sec²	[illegible]
		kg • m²	[illegible]
Weight	Wt	lb	24.5
		kg	[illegible]
Static Friction	TF	lb • ft	0.1
		N • m	[illegible]
Thermal Time Constant	TCT	minutes	50
Viscous Damping ∞ Z Source	Fl	lb • ft/KRPM	0.05
		N • m/KRPM	[illegible]

ISS:	ECN #	DATE	APP'D	ISS:	ECN #	DATE	APP'D
2	74730	12/5/86	[illegible]				



*AT ULTIMATE WINDING TEMPERATURE...FOR AMBIENT DATA MULTIPLY BY 1.16

INDUSTRIAL DRIVES

A KOLLMORGEN DIVISION

CD 25993 ISSUE 2
WRITTEN J.S. 12/85 APPROVED 2/86
SHEET 2 OF 2

Optional Brushless Tachometer Parameter **Tach Winding Data**

	Tol.	Symbol	Units	1	2	3	4	5
Voltage Sensitivity L-N	± 10%	KG	V/KRPM	10				
Voltage Ripple @12 cv/R	Max.	VR	% Avg-pk	2				
DC Resistance/ Phase	±12.5%	RT	ohms	32.7				
Load Resistance/ Phase	Min.	RL	ohms	3.5				
Inductance/ Phase	±30%	LG	mH	25				

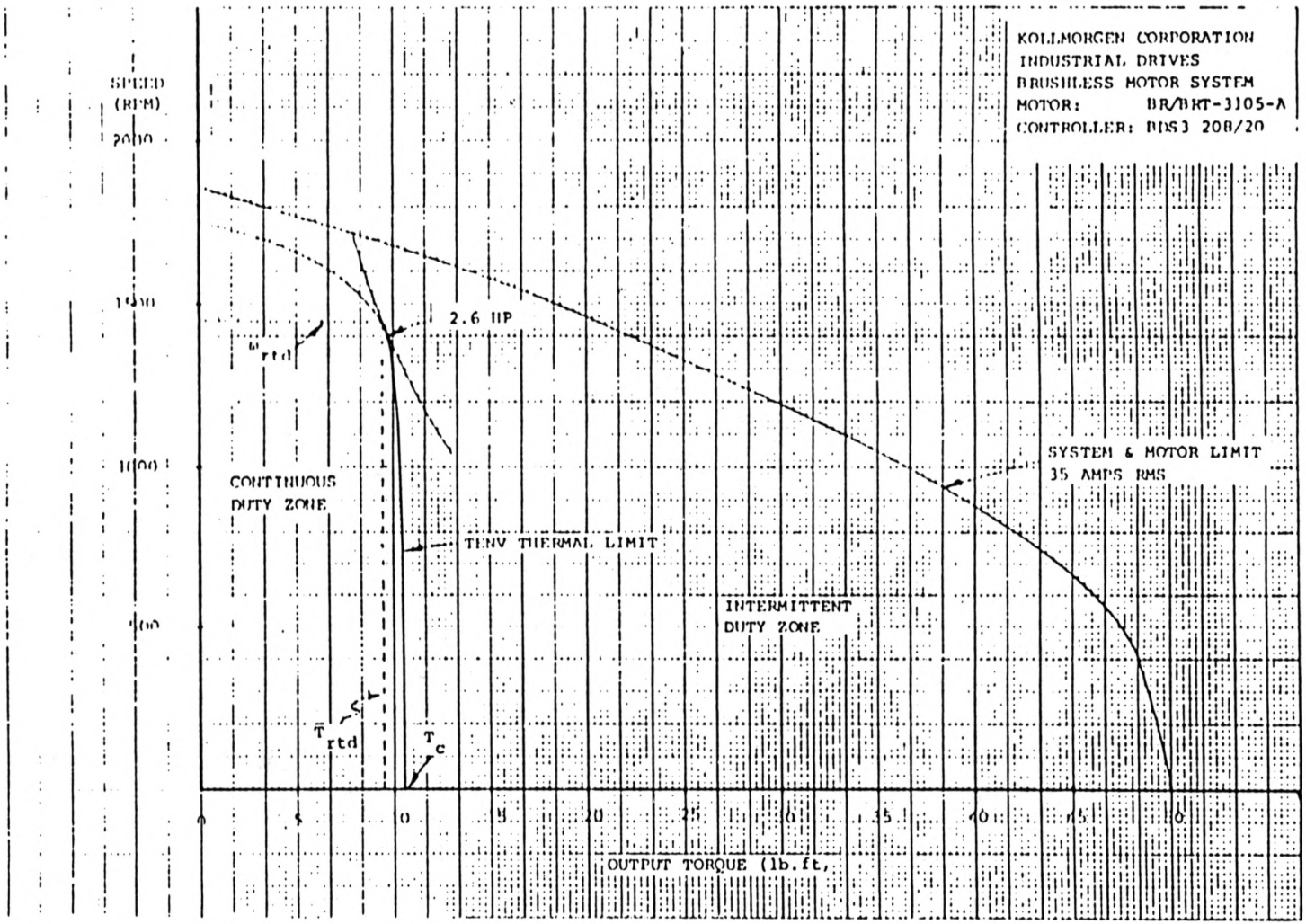
Optional Brush-Type Tachometer Parameter **Tach Winding Data**

	Tol.	Symbol	Units	1	2	3	4	5
Voltage Sensitivity	± 10%	KG	V/KRPM		19	17		
Voltage Ripple @ 66 cv/R	Max.	VR	% Avg-pk		1	0.1		
DC Resistance	±12.5%	RT	ohms		26	26		
Load Resistance	Min.	RL	ohms		2.6K	2.6K		
Inductance	± 30%	LG	mH		24	24		

Option Adders

	Length(in.)	Weight(lbs)	Inertia (lb-ft-sec²)
Brake	2.91	8.7	.0000934
Brushless 1713 Tachometer	1.12	2.0	.0000260
Brush-Type 2030 Tachometer	1.93	3.3	.0000469

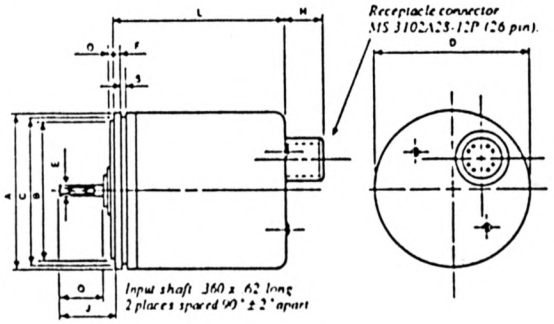
PC- 25996 ISSUE 2



APPROVED BY: TRE DATE: 11/2/88

MICRON® FEEDBACK TRANSDUCER 50-306-532

ABSOLUTE - FOUR SWITCH - Multi-turn, dual brushless resolvers - Fine/Coarse geared system with four integral limit switches. 3.5" dia. instrument housing (NEMA 12).



All dimensions are in inches

A	3.50 Dia.
B	3.000 / 2.997 Dia.
C	3.25 Dia.
D	3.50 Dia.
E	.3748 / .3743 Dia.
F	.125
H	.60
J	.84
L	6.05 max.
O	.04
Q	.71
S	.12

Aluminum alloy housing provides NEMA Type 12 enclosure for two (2) geared, servo size 11, brushless resolvers and four integral limit switches. Maximum absolute measurement range equals 128 turns of input shaft. Programmable, maintained contact limit switches are infinitely adjustable from 1 to 500 turns without changing components.

Internal precision anti-backlash gearing system provides two separate functions :

1 / Ratio between input shaft and fine resolver which is determined by system resolution.

2 / Ratio between input shaft and coarse resolver, which is determined by absolute measurement range required by system.

Unit is mounted with hold-down clamps and flexible coupling.

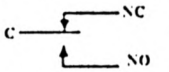
SPECIFICATIONS :

For use with 3105° motor
To use # 73-205-144 Resolvers

MATERIAL	Base	Aluminum alloy casting
	Cover	Aluminum alloy with anodize finish. O-ring seal at base.
	Shaft	Stainless steel.
	Gearing (Resolver)	Stainless steel, AGMA quality 14, spring loaded anti-backlash.
	Ball bearings	Stainless steel, shielded, lubricated with grease.
	Hardware	Corrosion resistant.
RESOLVERS	Brushless, servo size 11 (see Rotating Components 73-Series for standard resolvers).	
RATIOS	(Input shaft turns to fine resolver shaft turns) 1:1, 1:2, 1:2.5, 1:4, 1:5, 1:8, 1:10. (Input shaft turns to coarse resolver shaft turns) 8:1, 10:1, 16:1, 32:1, 36:1, 64:1, 100:1, 128:1. 145:1 - special order	

(over)

MICRO-SWITCH "SM" series, single pole, double throw. 5 Amps resistive, 3 AMPS inductive at 28 VDC. 5 Amps at 125 or 250 VAC.



C : Common
NO : Normally open when actuator is in free position
NC : Normally closed when actuator is in free position

SWITCHES #1 and #2 (closest to input shaft) maintained contact (Type A). At switching point, when viewing unit from input shaft, clockwise shaft rotation will depress micro-switch plunger (forced actuation).

SWITCHES #3 and #4 (closest to connector) maintained contact (Type B). At switching point, when viewing unit from input shaft, counterclockwise shaft rotation will depress micro-switch plunger (forced actuation).

SHAFT LOADING 10 lbs axial and 10 lbs radial at .5" from mounting surface.

OPERATING SPEED 5000 RPM maximum at fine resolver shaft. 5000 RPM maximum at unit input shaft for switches.

OPERATING TEMPERATURE -20° to +90° C.

MOUNTING Flexible coupling (see 41-2 Series)
Hold-down clamps (see 01-505-940-3)

MATING CONNECTOR Plug with clamp and bushing. Straight : 13-902-076-11
90° angle : 13-902-076-12

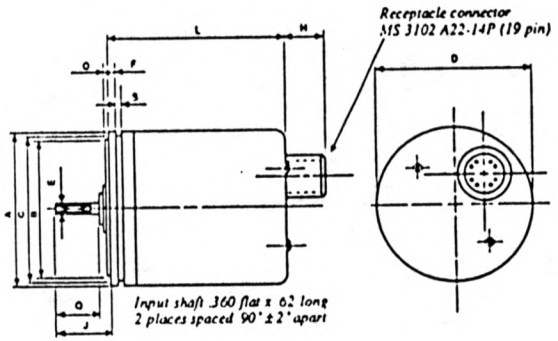
CAM ADJUSTING WRENCH For setting of switching points : 75-103-891

WIRING SCHEMATIC

Wire color	Component	Function	Connector pin number
Red / White	Fine resolver	R1 Rotor	A
Yellow (Black) White	"	R2 Rotor	B
Red	"	S1 Stator	C
Yellow	"	S2 Stator	D
Black	"	S3 Stator	E
Blue	"	S4 Stator	F
Red / White	Coarse resolver	R1 Rotor	G
Yellow (Black) / White	"	R2 Rotor	H
Red	"	S1 Stator	J
Yellow	"	S2 Stator	K
Black	"	S3 Stator	L
Blue	"	S4 Stator	M
Red	Switch #1	C	N
Yellow	"	NO	P
Black	"	NC	R
Orange	Switch #2	C	S
Brown	"	NO	T
White	"	NC	U
Gray	Switch #3	C	V
Purple	"	NO	W
Green	"	NC	X
White / Red	Switch #4	C	Y
White / Yellow	"	NO	Z
White / Black	"	NC	a

MICRON® FEEDBACK TRANSDUCER 50-306-520

ABSOLUTE - TWO SWITCH - Multi-turn, dual brushless resolvers - Fine/Coarse geared system with two integral limit switches, 3.5" diameter instrument housing (NEMA Type 12).



All dimensions are in inches

A =	3.50 Dia.
B =	3.000 / 2.997 Dia.
C =	3.25 Dia.
D =	3.50 Dia.
E =	.3748 / .3743 Dia
F =	.125
H =	.60
J =	.84
L =	5.00 max.
O =	.04
Q =	.71
S =	.12

Aluminum alloy housing provides NEMA type 12 enclosure for two (2) geared, servo size 11, brushless resolvers and two integral limit switches. Maximum absolute measurement range equals 128 turns of input shaft. Programmable, maintained contact limit switches are infinitely adjustable from 1 to 500 turns without changing components.

Internal precision anti-backlash gearing system provides two separate functions :

1/ Ratio between input shaft and fine resolver, which is determined by system resolution.

2/ Ratio between input shaft and coarse resolver, which is determined by absolute measurement range required by system.

Unit is mounted with hold-down clamps and flexible coupling.

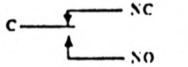
FOR USE WITH 2102 ...

SPECIFICATIONS :

MATERIAL	Base	Aluminum alloy casting.
	Cover	Aluminum alloy with anodize finish. O-ring seal at base.
	Shaft	Stainless steel.
	Gearing (Resolver)	Stainless steel, AGMA quality class 14, spring loaded anti-backlash.
	Ball bearings	Stainless steel, shielded, lubricated with grease.
	Hardware	Corrosion resistant.
RESOLVERS		Brushless, servo size 11 (see Rotating Components 73-Series for standard resolvers).
RATIOS		(Input shaft turns to fine resolver shaft turns) 1:1, 1:2, 1:2.5, 1:4, 1:5, 1:8, 1:10. (Input shaft turns to coarse resolver shaft turns) 8:1, 10:1, 16:1, 32:1, 36:1, 64:1, 100:1, 128:1.

(over)

MICRO-SWITCH	"SM" series, single pole, double throw. 5 Amps resistive, 3 Amps inductive at 28 VDC. 5 Amps at 125 or 250 VAC.



C : Common
NO : Normally open when actuator is in free position
NC : Normally closed when actuator is in free position.

BOTTOM SWITCH (closest to input shaft) maintained contact (Type A). At switching point, when viewing unit from input shaft, clockwise shaft rotation will depress micro-switch plunger (forced actuation).

TOP SWITCH (closest to connector) maintained contact (Type B). At switching point, when viewing unit from input shaft, counterclockwise shaft rotation will depress micro-switch plunger (forced actuation).

SHAFT LOADING	10 lbs. axial and 10 lbs. radial at .5" from mounting surface.
OPERATING SPEED	5000 RPM maximum at fine resolver shaft. 5000 RPM maximum at unit shaft for switches.

OPERATING TEMPERATURE -20° to +90° C.

MOUNTING — Flexible coupling (see 41-2 Series)
Hold-down clamps (see 01-505-940-3)

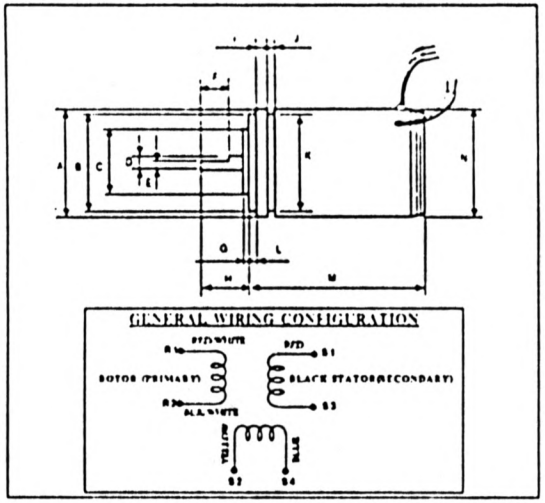
MATING CONNECTOR Plug with clamp and bushing. Straight : 13-902-076-09
90° angle : 13-902-076-10

CAM ADJUSTING WRENCH For setting of switching points : 75-103-891.

WIRING SCHEMATIC

Wire color	Component	Function	Connector pin number
Red / White	Fine resolver	R1 Rotor	A
Yellow (Black) / White	"	R2 Rotor	B
Red	"	S1 Stator	C
Yellow	"	S2 Stator	D
Black	"	S3 Stator	E
Blue	"	S4 Stator	F
Red / White	Coarse resolver	R1 Rotor	G
Yellow (Black) / White	"	R2 Rotor	H
Red	"	S1 Stator	J
Yellow	"	S2 Stator	K
Black	"	S3 Stator	L
Blue	"	S4 Stator	M
Red	Bottom switch	C	N
Yellow	"	NO	P
Black	"	NC	R
Orange	Top switch	C	S
Brown	"	NO	T
White	"	NC	U

MICRON® ROTATING COMPONENTS - 72-204-688, 73-205-144 - Resolvers (brushless) Servo size 11 - Control Transmitter



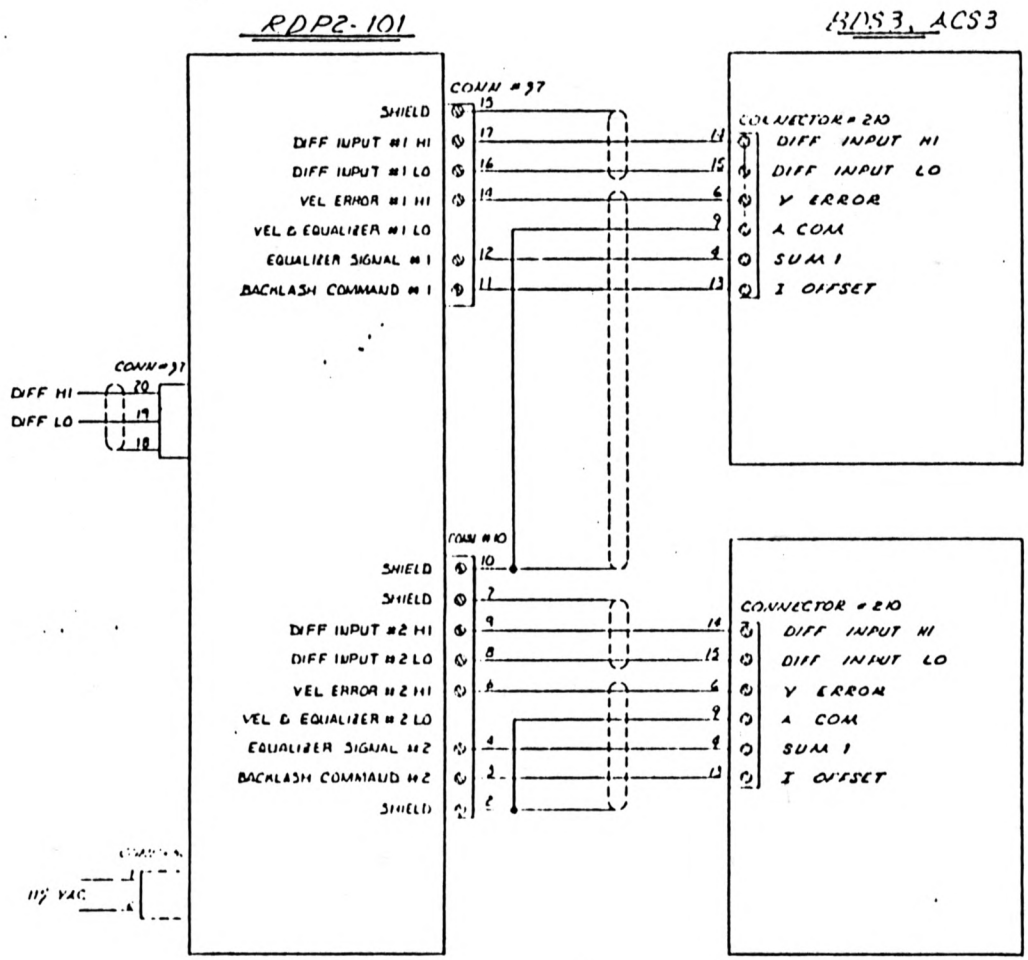
All dimensions are in inches

A	=	1.059/1.062 Dia.
B	=	.9995/1.0000 Dia.
C	=	.6245/.6250 Dia.
D	=	.1195/.1200 Dia.
E	=	.099/.105 Flat
F	=	.437
G	=	.059/.065
H	=	.562
I	=	.090/.096
J	=	.047/.053
K	=	.980 max.
L	=	.059/.065
M	=	1.590 max.
N	=	1.065 Dia. max.

TYPICAL ELECTRICAL DATA		73-204-688 2 speed (4-pole)	73-205-144 Single speed (2-pole)
Input Voltage	Volts	7.0	26
Transformation ratio		.9500 ± 5%	.454
Output Voltage	Volts	6.65	11.8
DC Rotor Resistance	OHMS	9.5	38
DC Stator Resistance	OHMS	114	130
Sensitivity	mV/Deg	116	206
Maximum Error	Minutes	12 spread	± 3
		5000 Hz	400 Hz
Input Current Maximum	mA.	10.9	40
Input power Nominal	WATTS	.039	.56
Impedance ZSO	OHMS	692 + j1250	330 + j315
Impedance ZRO	OHMS	410 + j594	450 + j580
Impedance ZRS	OHMS	150 + j350	440 + j330
Phase shift (Open circuit) lead	DEG	-3.0	10
Null Voltage (Total) RMS	mV	15	30
Phasing equation		E(S1-S3)=KE(R1-R2)cos A E(S2-S4)=KE(R1-R2)sin A	E(S1-S3)=KE(R1-R2)cos A E(S2-S4)=KE(R1-R2)sin A

73-01-3305/3-2

310 EXPRESS ST., PLAINVIEW, N.Y. 11803
516-349-1100 TWX 510 221 2194 USA



REV	ECN NUMBER	INITIALS	DATE	APP'D
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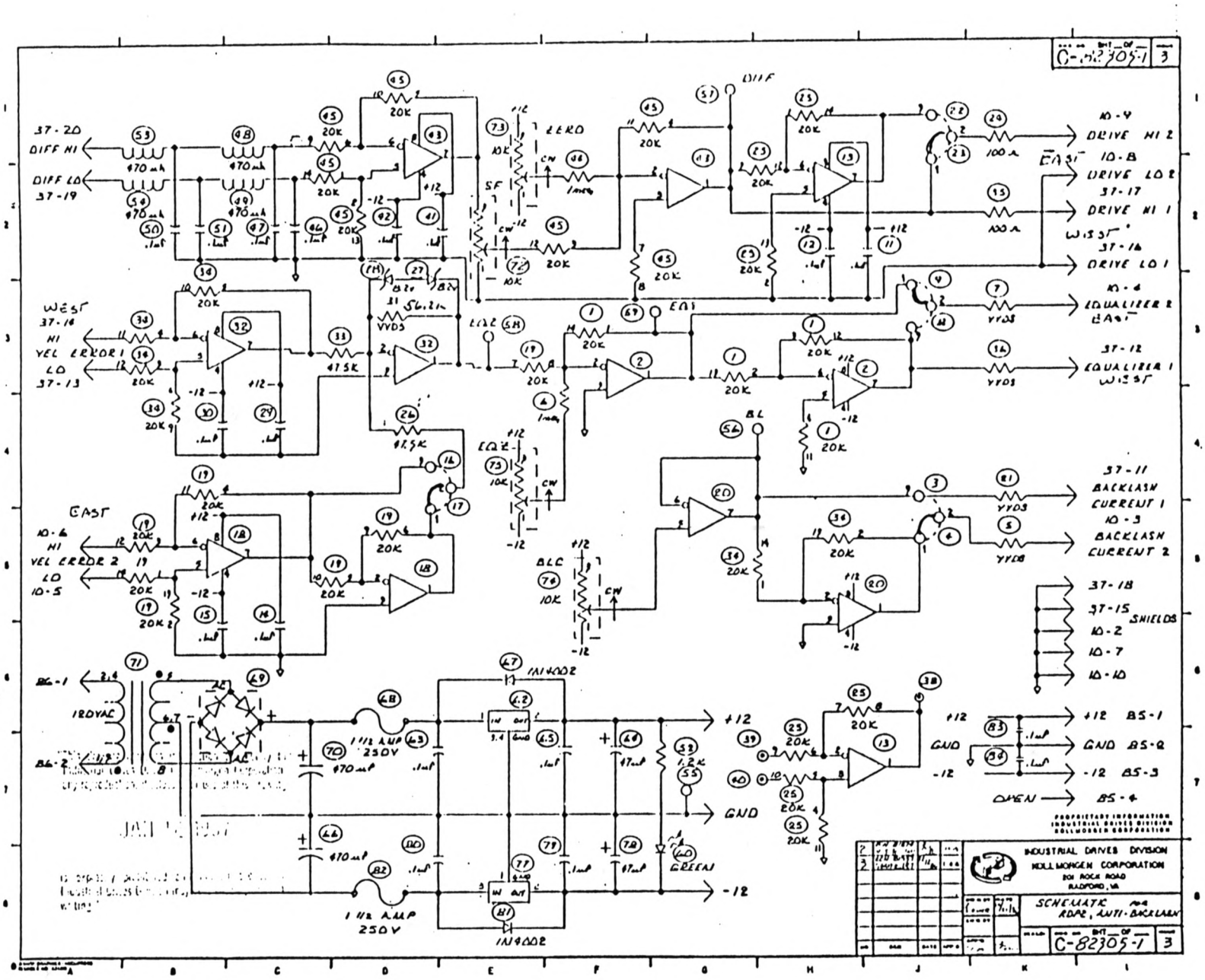
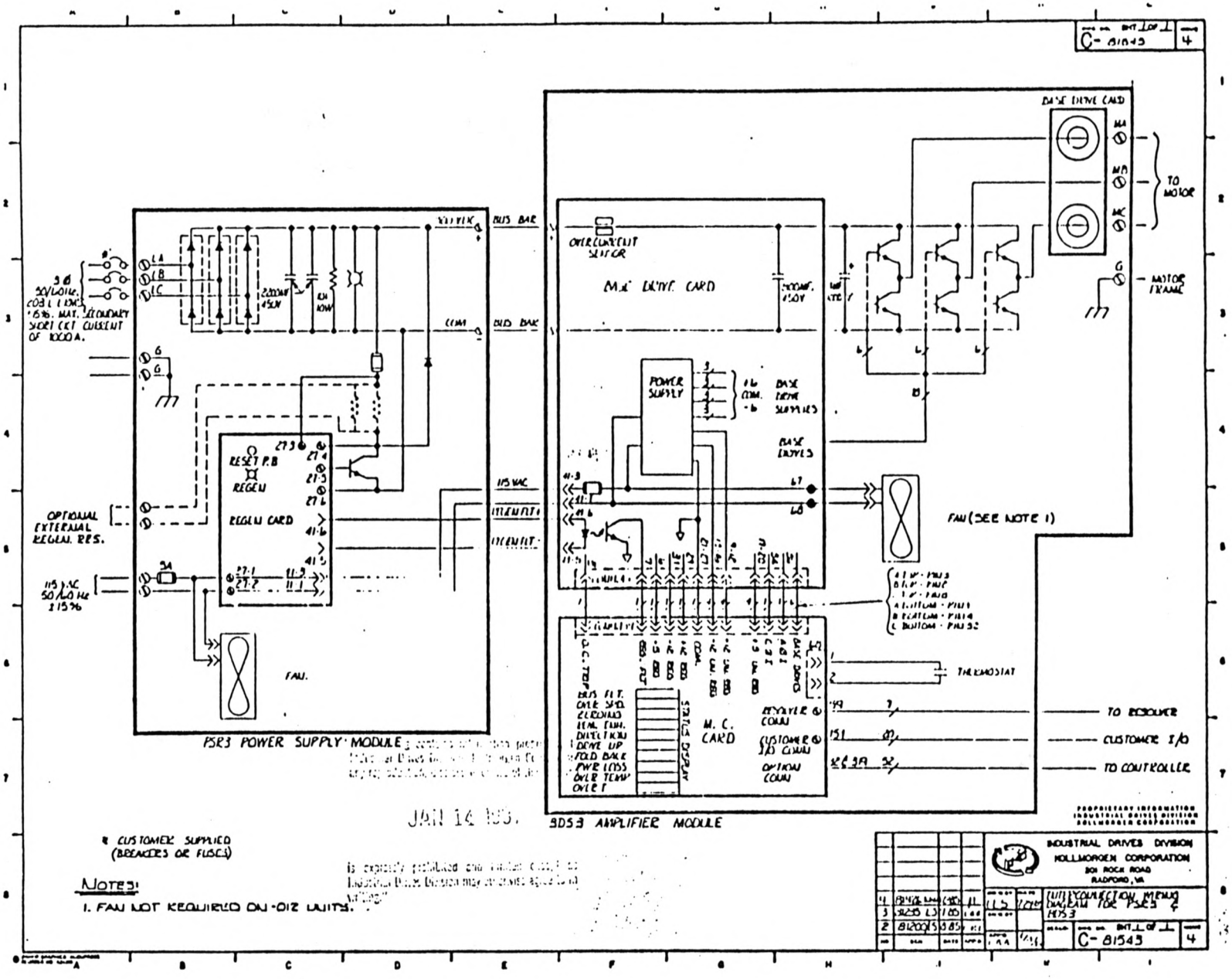
INLAND MOTOR
INDUSTRIAL DRIVE DIVISION

RDP2 INTERCONNECT DIAGRAM
FOR ACS3, BDS3

C-82317 | 2


C-82305-1
3
37-20
DIFF HI
DIFF LO
37-19
470 mh
ZERO
DIFF
SF
10K
20K
100 A
10-4
DRIVE HI 2
EAST
10-8
DRIVE LO 2
37-17
DRIVE HI 1
WEST
37-16
DRIVE LO 1
10-6
EQUALIZER 2
EAST
37-12
EQUALIZER 1
WEST
WEST
37-16
HI
YEL ERROR 1
LO
37-13
47.5K
EQU
BL
37-11
BACKLASH
CURRENT 1
10-3
BACKLASH
CURRENT 2
EAST
10-6
HI
YEL ERROR 2
LO
10-5
BLC
37-18
37-15
SHIELDS
10-2
10-7
10-10
BG-1
BG-2
120VAC
1N4002
1 1/2 AMP
250V
470 mf
+12
GND
-12
1.2K
GREEN
+12 BS-1
GND BS-2
-12 BS-3
OPEN
BS-4
PROPRIETARY INFORMATION
INDUSTRIAL DRIVES DIVISION
KOLLMORGEN CORPORATION
INDUSTRIAL DRIVES DIVISION
KOLLMORGEN CORPORATION
301 ROCK ROAD
RADFORD, VA
SCHEMATIC
ADAPT, ANTI-BACKLASH
C-82305-1
3



* CUSTOMER SUPPLIED (BREAKERS OR FUSES)

NOTES:

1. FAN NOT REQUIRED ON -012 UNITS.

INDUSTRIAL DRIVES DIVISION
KOLLMORGEN CORPORATION
801 ROCK ROAD
RADFORD, VA

WIRING CONNECTION MENU DIAGRAM FOR PSR3 & SD53

C-81543 4

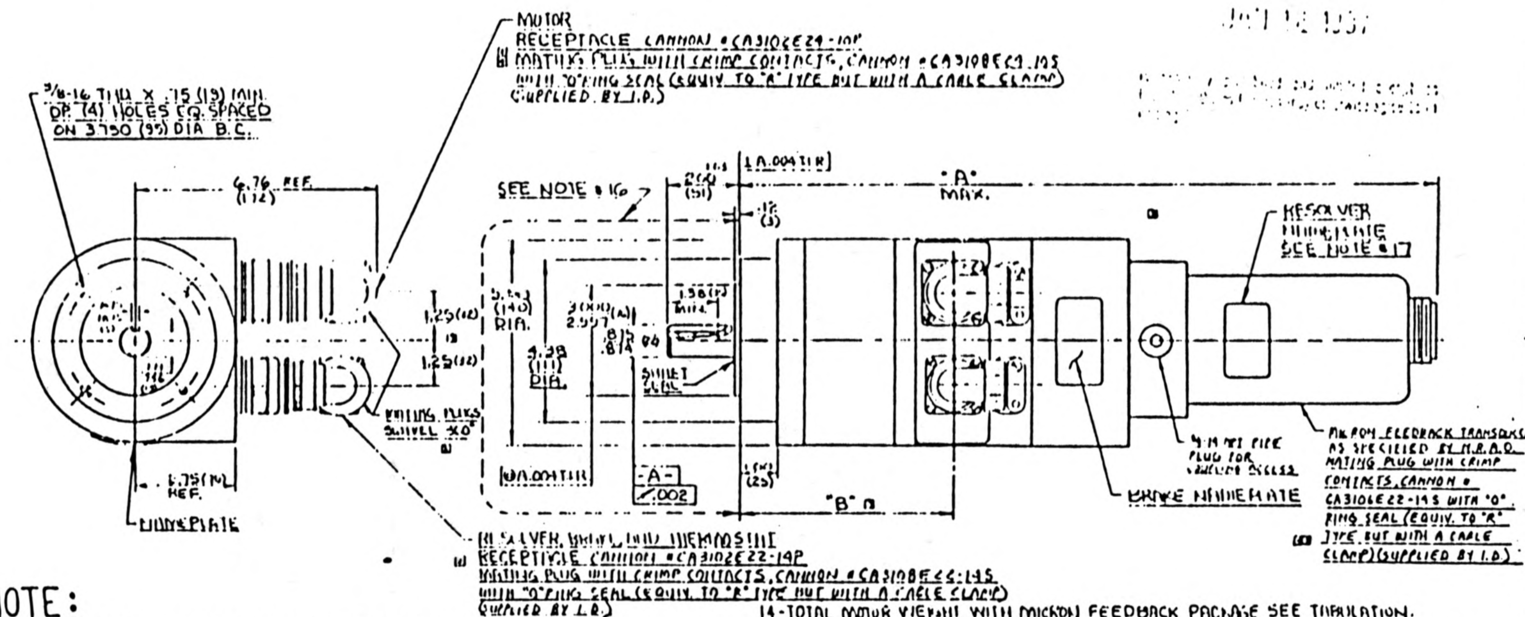
			C	40639	4

HOLDING CURRENT	BRAKE VOLTAGE	MODEL
.39 AMPS	90 V.D.C	BRB8R
1.27 AMPS	24 V.D.C.	BRB9R

MOTOR CONNECTION

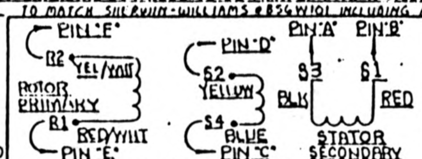
GROUND - GRN/YEL LEAD - PIN "D"
PHASE A - BROWN LEAD - PIN "A"
PHASE B - GREEN LEAD - PIN "B"
PHASE C - ORANGE LEAD - PIN "C"

SINGLE VOLTAGE



NOTE:

1. WITH A PHASE SEQUENCE A.C.B. MOTOR ROTATION SHALL BE CW FACING MOUNTING END.
2. ALL DIMENSIONS IN INCHES WITH METRIC EQUIVALENTS IN PARENTHESIS.
3. MOTOR CAN BE MOUNTED IN ANY POSITION.
4. BRAKE DUTY: CONTINUOUS STATIC HOLDING & EMERGENCY DYNAMIC STOPPING. TYPE - POWER ON BRAKE OFF, HOLDING NOM. STATIC 22 LB-FT, BRAKE ELECT. LEADS IN PINS "N" & "P".
5. SHAFT MATERIAL - 17-4PH STAINLESS STEEL.
6. ALL RETAINING RINGS, KEYS, PINS, NUTS, BOLTS, SCREWS, WASHERS AND SPRINGWASHERS WILL BE 300 SERIES STAINLESS STEEL OR ZINC PLATED.
7. MOTOR SHALL USE A SIX POLE RARE EARTH PERMANENT MAGNET.
8. FRONT END BELL, RESOLVER HOUS. WITH BRG LINER, BRAKE HOUS & STATOR WILL BE YELLOW CHROMATED.
9. UNPROTECTED SURFACES OF ROTOR STACK TO BE PAINTED BLACK PRIMER.
10. PRESSURE ON SHAFT SEAL NOT TO EXCEED 5 P.S.I.
11. MOTOR WILL BE TOTALLY ENCLOSED FOR DIRT AND MOISTURE RESISTANCE. "O" RINGS WILL BE USED BETWEEN ALL EXTERNAL JOINTS. LOCTITE 515 SEALING COMPOUND WILL BE USED TO SEAL, AS NEEDED.
12. MOTOR SUPPLIED WITH LIFE LUBRICATED BEARINGS RATED AT -55°C TO 85°C.
13. THERMOSTAT PRESET TO OPEN AT 230°F ±6°F AND CLOSE AT 194°F ±10°F FALLING. NORMALLY CLOSED CONTACTS RATED TO 15 AMPS., 120 V.A.C. PINS "T" + "U".
14. TOTAL MOTOR WEIGHT WITH MICRON FEEDBACK PACKAGE SEE TABULATION.
15. MOUNTING SURFACES, SHAFT EXT. & CONNECTOR THREADS SHALL BE FREE OF PAINT AND PRIMER.
16. MASK OFF RESOLVER NAMEPLATE BEFORE PAINTING.
17. EXTERNAL SURFACES TO BE PAINTED WITH A BRILLIANT HIGH GLOSS WHITE EPOXY PAINT TO MATCH SHERWIN-WILLIAMS #B56W101 INCLUDING A BASE PRIMER PER IM-15 TO MEET MIL-STD-810.



RESOLVER CONNECTION DIAGRAM

"B"	LBS MIN	"A" mm	MODEL NO.
9.86	50	20.78 (528)	BRB( )R-2105-3007
8.76	46	19.68 (500)	BRB( )R-2104-3007
7.66	42	18.58 (472)	BRB( )R-2103-3007
6.56	38	17.48 (444)	BRB( )R-2102-3007
5.46	34	16.38 (416)	BRB( )R-2101-3007

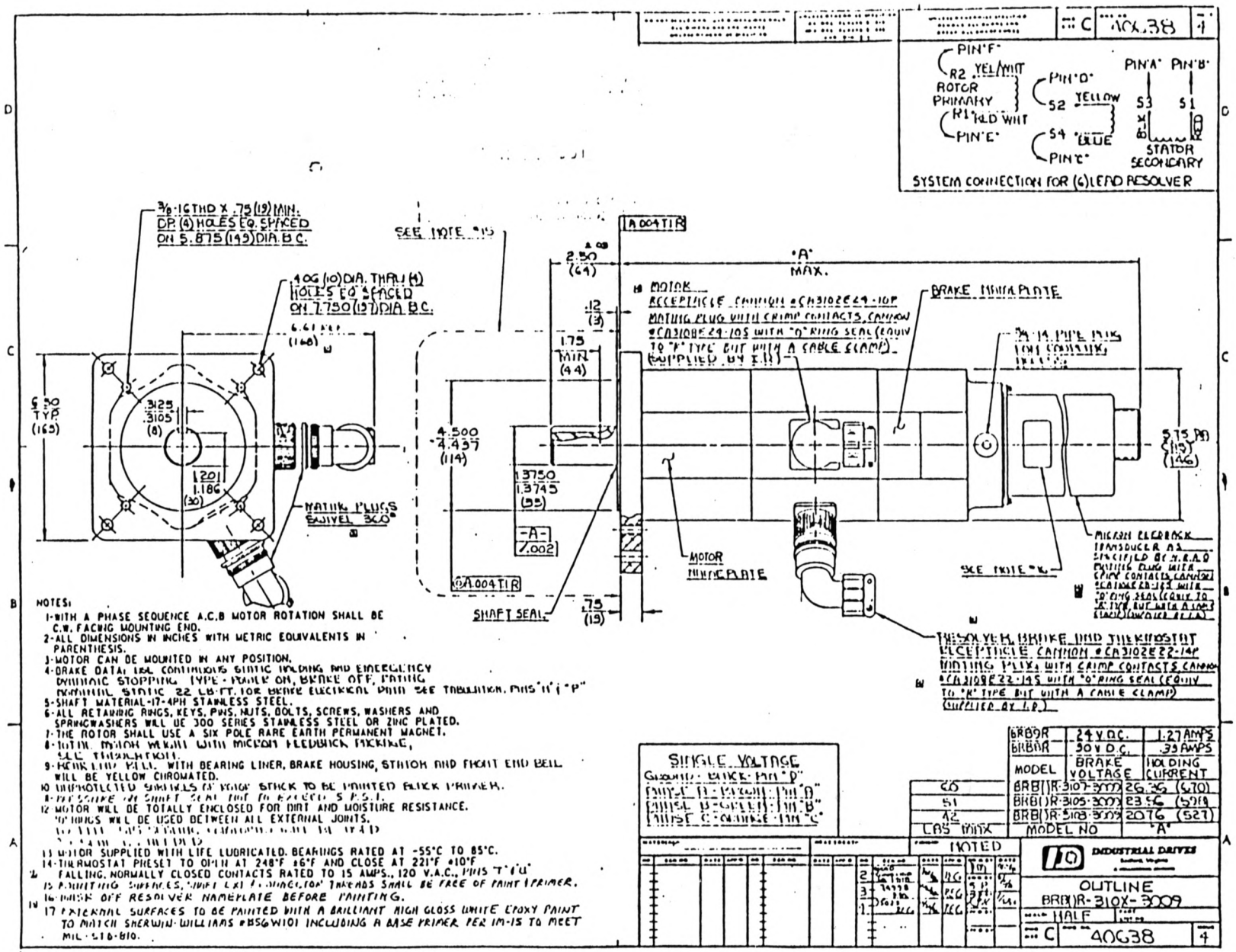
NOTED

INDUSTRIAL DRIVES

OUTLINE
BRB( )R-210X-3007

NONE

C 40639 4



NOTES:
1. WITH A PHASE SEQUENCE A,C,B MOTOR ROTATION SHALL BE C.W. FACING MOUNTING END.
2. ALL DIMENSIONS IN INCHES WITH METRIC EQUIVALENTS IN PARENTHESIS.
3. MOTOR CAN BE MOUNTED IN ANY POSITION.
4. BRAKE DATA: 16A CONTINUOUS STATIC HOLDING AND EMERGENCY DYNAMIC STOPPING. TYPE - POWER ON, BRAKE OFF, FAIL SAFE. MINIMUM STATIC 22 LB-FT. FOR BRAKE ELECTRICAL PINS SEE TABULATION. PINS "H" & "P"
5. SHAFT MATERIAL-17-4PH STAINLESS STEEL.
6. ALL RETAINING RINGS, KEYS, PINS, NUTS, BOLTS, SCREWS, WASHERS AND SPRINGWASHERS WILL BE 300 SERIES STAINLESS STEEL OR ZINC PLATED.
7. THE ROTOR SHALL USE A SIX POLE RARE EARTH PERMANENT MAGNET.
8. MOTOR MOUNT WEIGHT WITH MICRON FEEDBACK PACKAGE, SEE TABULATION.
9. REAR END BELL WITH BEARING LINER, BRAKE HOUSING, STATOR AND FRONT END BELL WILL BE YELLOW CHROMATED.
10. UNPROTECTED SURFACES OF ROTOR STACK TO BE PAINTED BLACK PRIMER.
11. PRESSURE ON SHAFT SEAL NOT TO EXCEED 5 P.S.I.
12. MOTOR WILL BE TOTALLY ENCLOSED FOR DIRT AND MOISTURE RESISTANCE. O-RINGS WILL BE USED BETWEEN ALL EXTERNAL JOINTS.
13. MOTOR SUPPLIED WITH LIFE LUBRICATED BEARINGS RATED AT -55°C TO 85°C.
14. THERMOSTAT PRESET TO OPEN AT 248°F ±6°F AND CLOSE AT 221°F ±10°F FALLING. NORMALLY CLOSED CONTACTS RATED TO 15 AMPS., 120 V.A.C., PINS "T" & "U"
15. PAINTING SURFACES, SHAFT EXTENSION AND THREADS SHALL BE FREE OF PAINT & PRIMER.
16. MASK OFF RESOLVER NAMEPLATE BEFORE PAINTING.
17. EXTERNAL SURFACES TO BE PAINTED WITH A BRILLIANT HIGH GLOSS WHITE EPOXY PAINT TO MATCH SHERWIN-WILLIAMS #B56W101 INCLUDING A BASE PRIMER PER IM-15 TO MEET MIL-S-18-870.

SINGLE VOLTAGE
CONNECTOR: BRAKE: PIN "P"
PHASE B: RESOLVER: PIN "B"
PHASE A: RESOLVER: PIN "A"
THERMOSTAT: PIN "C"

C6		
S1		
R2		
LBS MAX	MODEL NO	"A"

MODEL	BRAKE VOLTAGE	HOLDING CURRENT
BRB(1)R-3107-3009	26.36	1.27 AMPS (670)
BRB(1)R-3105-3009	83.56	.33 AMPS (509)
BRB(1)R-5103-3009	207.6	(527)

BRB9R 24 V.D.C. 1.27 AMPS
BRB8R 90 V.D.C. .33 AMPS

NOTED

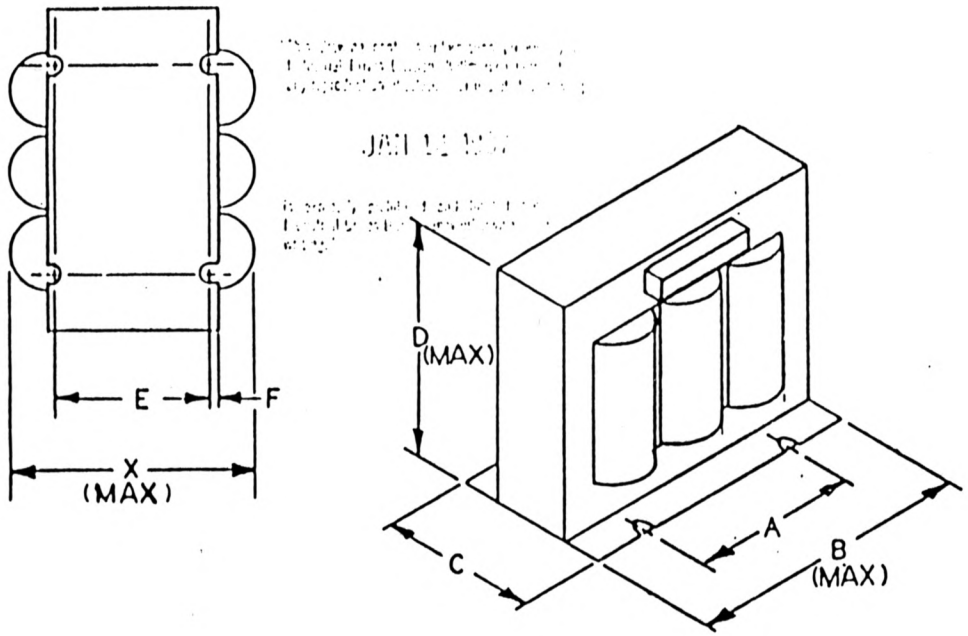
INDUSTRIAL DRIVES

OUTLINE
BRB(1)R-310X-3009

HALF

C 40638 4

DWG NO	SH	REV
A-80421	2 OF 3	8



DASH	X	A	B	C	D	E	F
001		8.5	12.5	6.5	7.0	4.88	
002							
003							
004		10.75	15.88	9.75	9.06	7.50	1.13
005							
[8] 006	9½	12	15.25	8.5	13.5	7.0	5/8
[7] 007	13½	14	20¾	8¼	13	7¾	3/32
008		12.0	16.0	8.5	15.5	6.87	.782
009							
010							
011		19.0	21	8.25	16.5	6.5	.87
012							
013							
014							

EXAMPLE: TR3 – 230 / 7.5 – 16 – 00 — OPEN CONSTRUCTION
- 240/480 PRIMARY
- IRMS
- 230 VRMS SECONDARY
- 3 PHASE TRANSFORMER 240/480 VAC RMS PRIMARY

BOSE MORGEN CORPORATION — INDUSTRIAL DRIVES DIVISION — RADFORD, VIRGINIA

UNLESS OTHERWISE SPECIFIED
XX DEC PLACES ± .01
XXX DEC PLACES ± .005
ANG DIM ± 1°

DO NOT SCALE DWG. USE DIMENSIONS ONLY
ALL DIMENSIONS ARE INCHES
UNLESS OTHERWISE SPECIFIED

NO	ECN NO.	DATE	APP'D.
8	81717 OWENS	11/18/93	

DW'N BY LLS — DATE 11/18/93
CH'K BY
APP'D BY — DATE 11/22/93

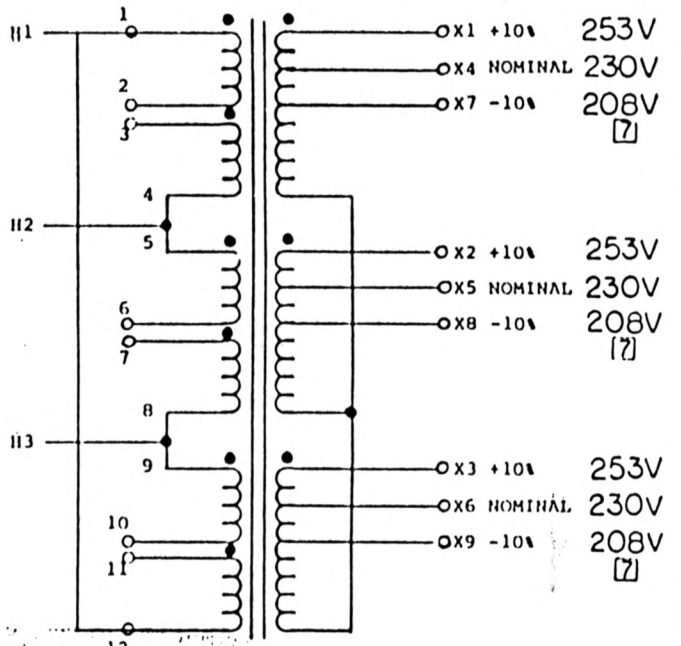
SPEC
3 PHASE POWER TRANS.

SCALE: NONE — DWG NO. A-80421 SH 2 OF 3 — REV 8

THIS INFO MUST BE ON A LABEL & AFFIXED TO UNIT!

VOLTS	CONNECTION	LINES
240	1-3, 2-4, 5-7, 6-8, 9-11, 10-12	H1-H2-H3
480	2-3, 6-7, 10-11	H1-H2-H3
253		X1-X2-X3
230		X4-X5-X6
208		X7-X8-X9

DASH NO.	IDD MODEL NUMBER	IRMS	VRMS (NOMI) SEC. VOLT.	CONST.
001	TR3-230/75-16-00	7.5	230	OPEN
002	/013	13		
003	/020	20		
004	/030	30		
005	/038	38		
006	/058	58		
007	/075	75		
008	/095	95		
010	/113	113		
011	/151	151		
012	/188	188		
013	/289	289		
014	/377	377		



DWG NO SH 3 OF 3
A- 80421
REV 8

ROCKWELL INTERNATIONAL
INDUSTRIAL DRIVES DIVISION
RADFORD, VIRGINIA

UNLESS OTHERWISE SPECIFIED
XX DEC PLACES ± .01
XXX DEC PLACES ± .005
ANG DIM ±1°

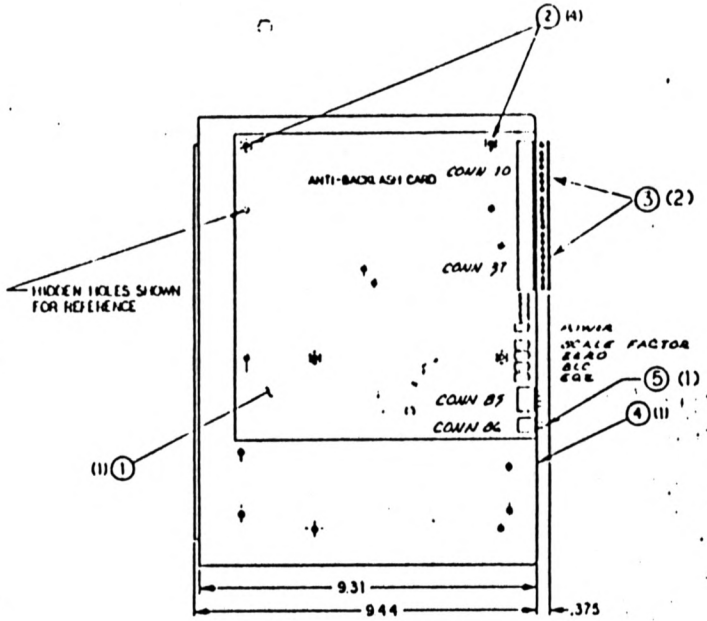
DO NOT SCALE DWG USE DIMENSIONS ONLY
ALL DIMENSIONS ARE INCHES
UNLESS OTHERWISE SPECIFIED

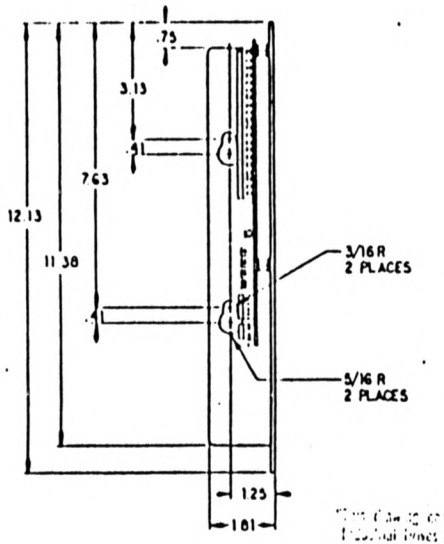
NO	ECN NO	DATE	APP'D	NO	ECN NO.	DATE	APP'D.

DWN BY LLS DATE 11/21/85
CHK'D BY
APP'D [illegible] 11/23/85

SPEC
3 PHASE POWER TRANS

SCALE: NONE
DWG NO SH 3 OF 3
A-80421
REV 8





KC INDUSTRIAL CONTROL DIVISION RADFORD, VIRGINIA

RDPH-101 MOUNTING PLATE ASSY
& OUTLINE & DIMENSION

SCALE 1/2 SHEET [illegible]

C 82318 T

SPARE PARTS LIST

(Board & Component Level)

National Radio Astronomy Observatory S.O. 59266

I. BRB8R-2102-3007-A-401-22 Motor

1. P/N C-40619 Antibacklash brake
2. P/N B-40664 Micron feedback package

II. BRB8R-3105-3009-A-401-2

1. P/N C-40619 Brake
2. P/N B-40613 Micro feedback package

III. BDS3-208/12-01-200 Servo amplifier
BDS3-208/20-01-200 Servo amplifier

1. P/N ACS3-MC2 Motor control card
2. P/N A-80121 Power transistor 12 amp unit
3. P/N A-79957 Power transistor 20 amp unit
4. P/N A-80294-001 Microprocessor
5. P/N A-78899-008 Fuse

IV. PSR3-208/50-01-002

1. P/N BDS3-REG1 Regenerative card
2. P/N A-79787-001 Fuse 10 amps
3. P/N A-78896-013 Fuse 5 amp glass tube
4. P/N A-79787-005 Fuse semi cond. 30 amps SDDV
5. P/N A-81080 Transistor power module, 100 amp 450V
6. P/N A-80934 Transistor switching module

V. Heaters for overload relays

P/N H-15952 for use with BRB8R-2102
P/N K-93037 for use with BRB8R-3105

National Semiconductor Corporation

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard + 5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ± 15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

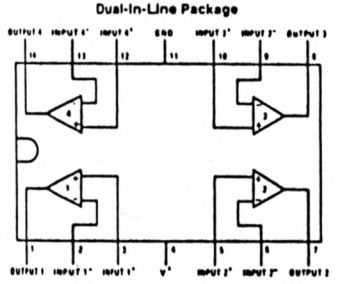
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
  (temperature compensated)
- Wide power supply range:
  Single supply 3 V_{DC} to 32 V_{DC}
  or dual supplies ± 1.5 V_{DC} to ± 16 V_{DC}
- Very low supply current drain (800 μA)—essentially independent of supply voltage (1 mW/op amp at + 5 V_{DC})
- Low input biasing current 45 nA_{DC}
  (temperature compensated)
- Low input offset voltage 2 mV_{DC}
  and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagram

Dual-In-Line Package

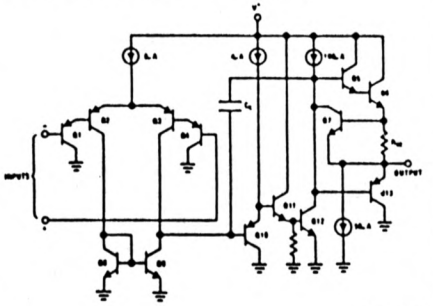


TL/H/9298–1

Top View

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ, LM324M, LM324AM, LM2902M, LM324N, LM324AN or LM2902N
See NS Package Number J14A, M14A or N14A

Schematic Diagram (Each Amplifier)



TL/H/9298–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 9)

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ± 16 V_{DC}	26 V_{DC} or ± 13 V_{DC}	Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Differential Input Voltage	32 V_{DC}	26 V_{DC}	Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}	Soldering Information		
Power Dissipation (Note 1)			Dual-in-Line Package		
Molded DIP	1130 mW	1130 mW	Soldering (10 seconds)	260°C	260°C
Cavity DIP	1260 mW	1260 mW	Small Outline Package		
Small Outline Package	800 mW	800 mW	Vapor Phase (60 seconds)	215°C	215°C
Output Short-Circuit to GND			Infrared (15 seconds)	220°C	220°C
(One Amplifier) (Note 2)			See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
$V^+ \leq 15$ V_{DC} and $T_A = 25°C$	Continuous	Continuous			
Input Current			ESD rating to be determined.		
($V_{IN} < -0.3$ V_{DC}) (Note 3)	50 mA	50 mA			
Operating Temperature Range		−40°C to +85°C			
LM324/LM324A	0°C to +70°C				
LM224/LM224A	−25°C to +85°C				
LM124/LM124A	−55°C to +125°C				

Electrical Characteristics $V^+ = +5.0$ V_{DC} (Note 4), unless otherwise stated

Parameter	Conditions	LM124A		LM224A		LM324A		LM124/LM224		LM324		LM2902		Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5)		±1	±2		±1	±3		±2	±5		±2	±7		±2	±7	mV$_{DC}$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ $V_{CM} = 0V$		20	50		40	80		45	100		45	150		45	250	nA$_{DC}$
(Note 6)																	
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$ $V_{CM} = 0V$		±2	±10		±2	±15		±3	±30		±5	±30		±5	±50	nA$_{DC}$
Input Common-Mode	$V^+ = 30$ V_{DC}	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V$_{DC}$
Voltage Range (Note 7)	(LM2902, $V^+ = 26$ V_{DC})																
Supply Current	$R_L = \infty$, $V^+ = 30V$,		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA$_{DC}$
	(LM2902 $V^+ = 26V$)																
	$R_L = \infty$ On All Op Amps		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	
	Over Full Temperature Range																
Large Signal	$V^+ = 15$ V_{DC}, $R_L \geq 2$ kΩ,	50	100		50	100		25	100		50	100		25	100		V/mV
Voltage Gain	($V_O = 1$ V_{DC} to 11 V_{DC})																
Common-Mode	DC, $V_{CM} = 0V$ to $V^+ - 1.5$ V_{DC}	70	85		70	85		65	85		70	85		65	85		dB
Rejection Ratio																	
Power Supply	DC, $V^+ = 5$ V_{DC} to 30 V_{DC}	65	100		65	100		65	100		65	100		50	100		dB
Rejection Ratio	(LM2902, $V^+ = 5$ V_{DC} to 26 V_{DC})																

Electrical Characteristics $V^+ = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Amplifier-to-Amplifier Coupling (Note 8)		f = 1 kHz to 20 kHz, (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
	Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		
		$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 200\ mV_{DC}$	12	50		12	50		12	50		12	50		12	50		12	50		μA_{DC}
Short Circuit to Ground		(Note 2) $V^+ = 15\ V_{DC}$, $T_A = 25°C$		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage		(Note 5)			±4			±4			±5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift		$R_S = 0\Omega$		±7	±20		±7	±20		±7	±30		±7			±7			±7		$\mu V/°C$
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			±30			±30			±75			±100			±150		±45	±200	nA_{DC}
Input Offset Current Drift		$R_S = 0\Omega$		±10	±200		±10	±200		±10	±200		±10			±10			±10		$pA_{DC}/°C$
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)		$V^+ = +30\ V_{DC}$ (LM2902, $V^+ = 26\ V_{DC}$)	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V_{DC}
Large Signal Voltage Gain		$V^+ = +15\ V_{DC}$ (V_O Swing = 1 V_{DC} to 11 V_{DC}) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
		$R_L \geq 10\ k\Omega$ (LM2902, $V^+ = 26\ V_{DC}$)	27	28		27	28		27	28		27	28		27	28		23	24		
	V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \geq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}

Electrical Characteristics $V^+ = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions		LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Current	Source	$V_O = 2\ V_{DC}$	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	Sink		$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2902 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O = 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$) at 25°C, for LM2902, V^+ from 5 V_{DC} to 26 V_{DC}.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

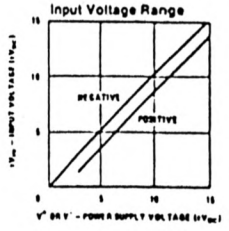
Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902), independent of the magnitude of V^+.

Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

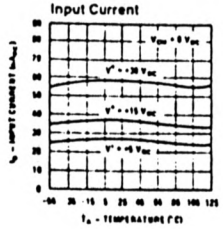
Note 9: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

Typical Performance Characteristics

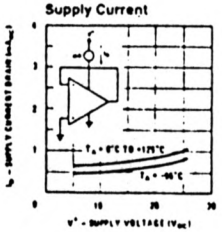
Input Voltage Range



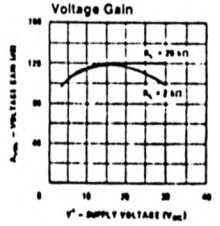
Input Current



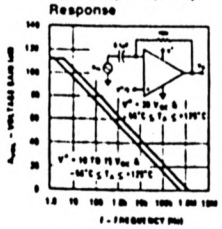
Supply Current



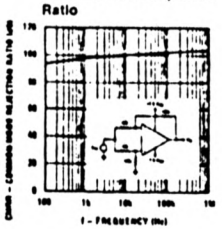
Voltage Gain



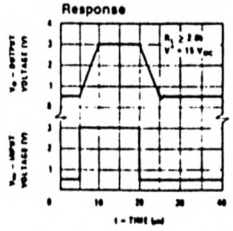
Open Loop Frequency Response



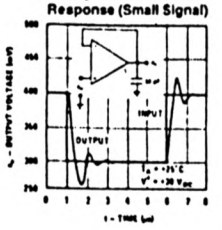
Common Mode Rejection Ratio



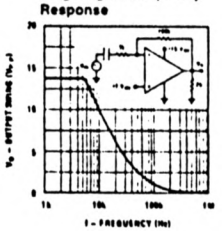
Voltage Follower Pulse Response



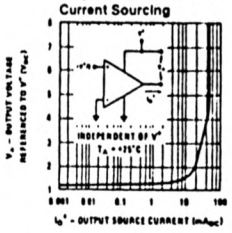
Voltage Follower Pulse Response (Small Signal)



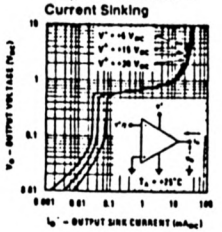
Large Signal Frequency Response



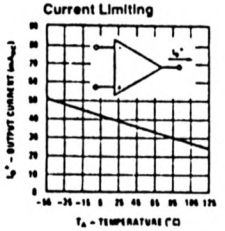
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



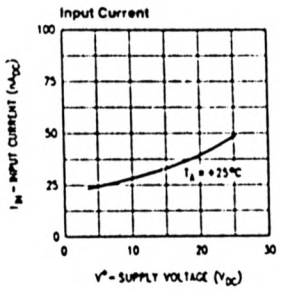
Current Limiting



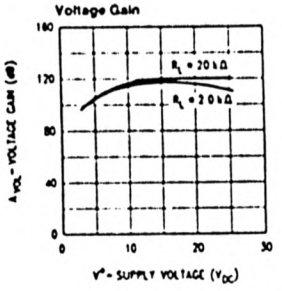
TL/H/9299-3

Typical Performance Characteristics (LM2902 only)

Input Current



Voltage Gain



TL/H/9299-4

Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

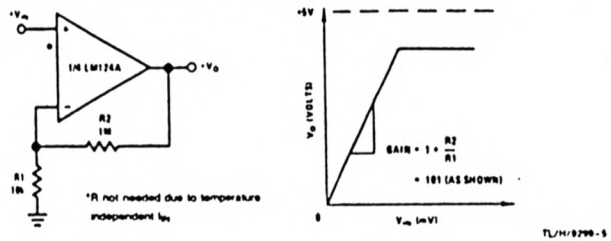
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

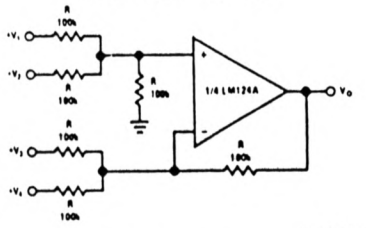
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)



TL/H/9299-5

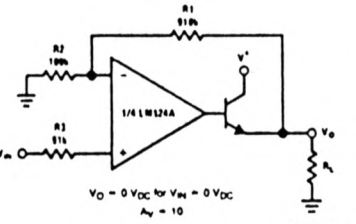
DC Summing Amplifier (V_{IN}'s ≥ 0 V_{DC} and V_O ≥ V_{DC})



TL/H/9299-6

Where $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O \geq 0\ V_{DC}$

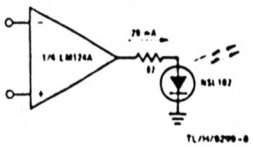
Power Amplifier



$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$

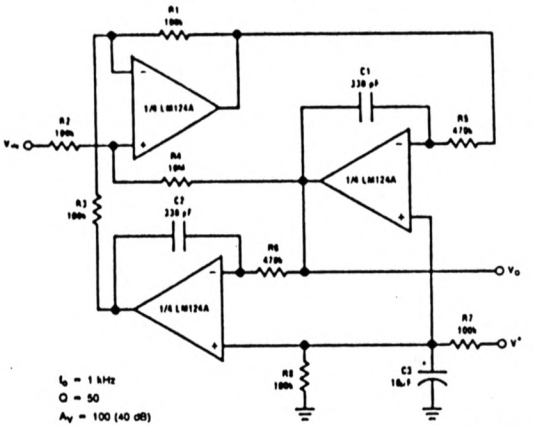
TL/H/9299-7

LED Driver



TL/H/9299-8

"BI-QUAD" RC Active Bandpass Filter

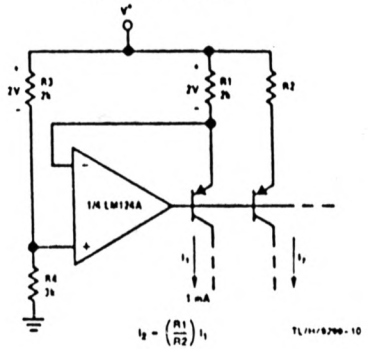


f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

TL/H/9299-9

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

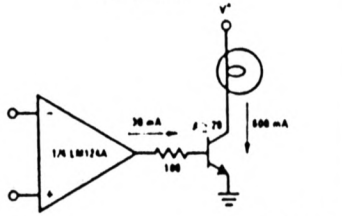
Fixed Current Sources



$I_2 = \left(\frac{R1}{R2}\right) I_1$

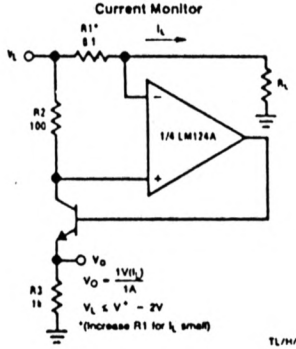
TL/H/9299-10

Lamp Driver



TL/H/9299-11

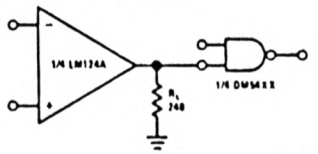
Current Monitor



$V_O = \frac{1V(I_L)}{1A}$
$V_L \leq V^+ - 2V$
*(Increase R1 for I_L small)

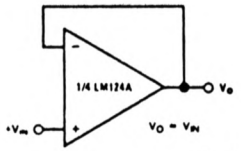
TL/H/9299-12

Driving TTL



TL/H/9299-13

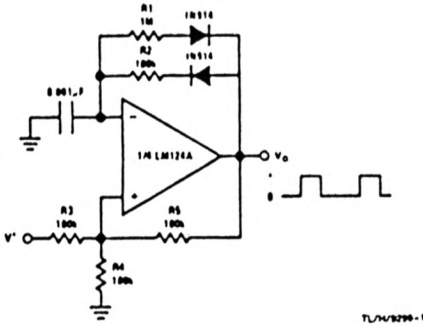
Voltage Follower



$V_O = V_{IN}$

TL/H/9299-14

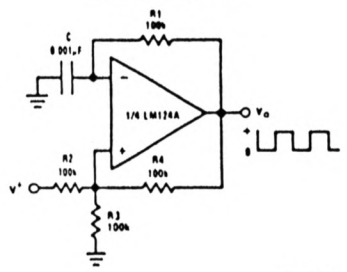
Pulse Generator



TL/H/9299-15

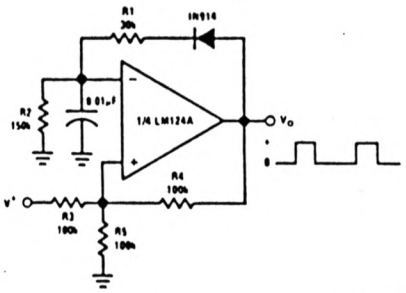
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Squarewave Oscillator



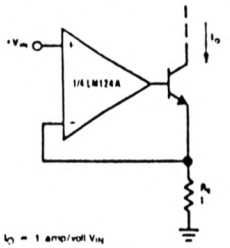
TL/H/9299-16

Pulse Generator



TL/H/9299-17

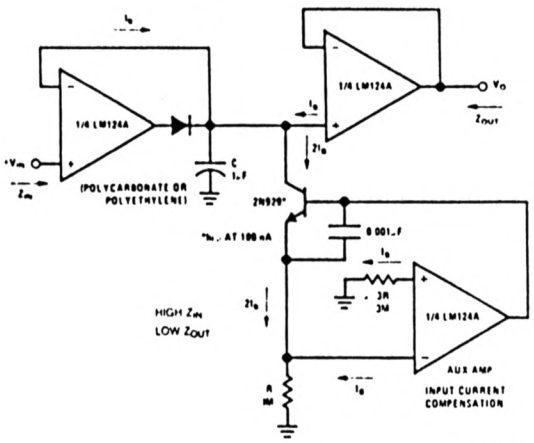
High Compliance Current Sink



I_O = 1 amp/volt V_{IN}
(Increase R_L for I_O small)

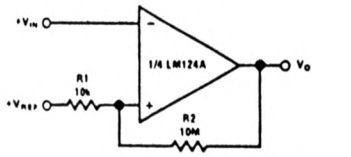
TL/H/9299-18

Low Drift Peak Detector



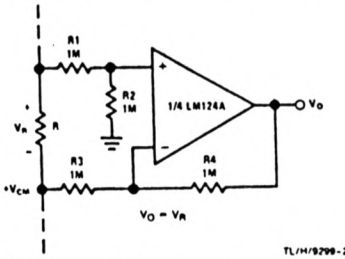
TL/H/9299-19

Comparator with Hysteresis



TL/H/9299-20

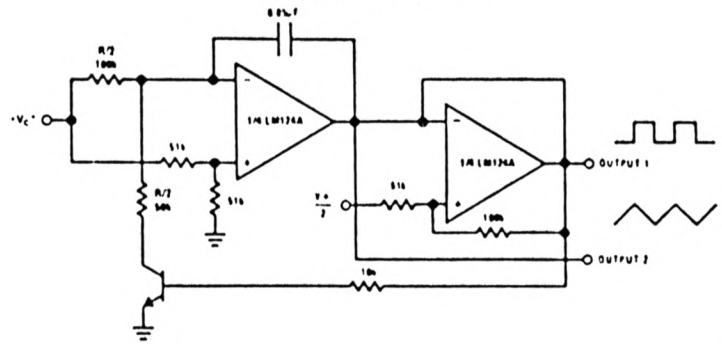
Ground Referencing a Differential Input Signal



TL/H/9299-21

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

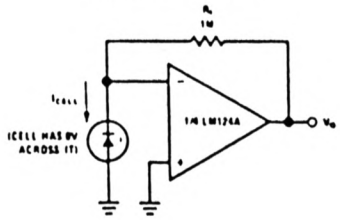
Voltage Controlled Oscillator Circuit



TL/H/9299-22

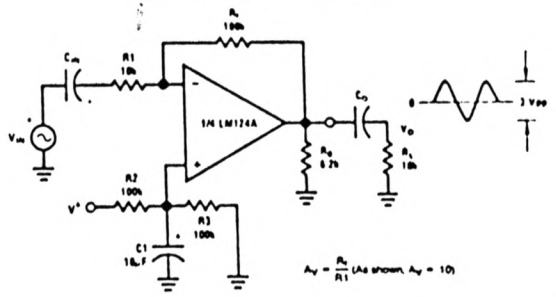
*Wide control voltage range $0\ V_{DC} \leq V_C \leq 2\ (V^+ - 1.5\ V_{(C)})$

Photo Voltaic-Cell Amplifier



TL/H/9299-23

AC Coupled Inverting Amplifier

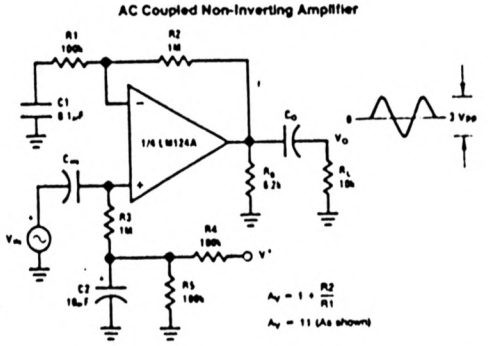


$A_V = \frac{R_L}{R1}$ (As shown, $A_V = 10$)

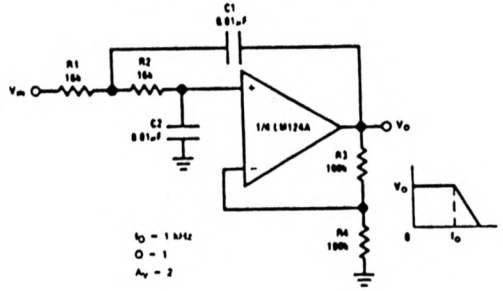
TL/H/9299-24

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

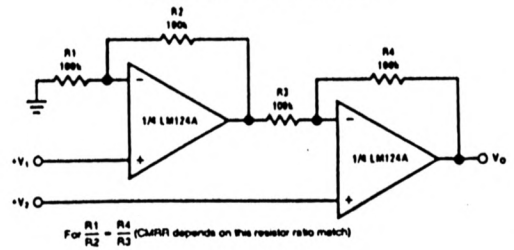
AC Coupled Non-Inverting Amplifier



DC Coupled Low-Pass RC Active Filter



High Input Z, DC Differential Amplifier



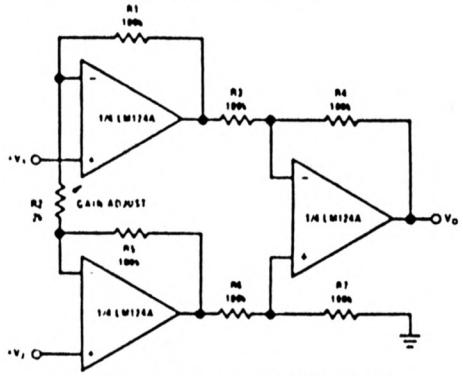
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown $V_O = 2(V_2 - V_1)$

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

High Input Z Adjustable-Gain DC Instrumentation Amplifier

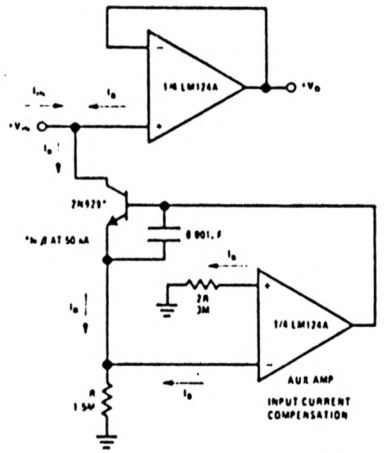


If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

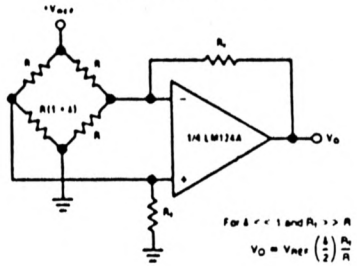
$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$

As shown $V_O = 101(V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



Bridge Current Amplifier

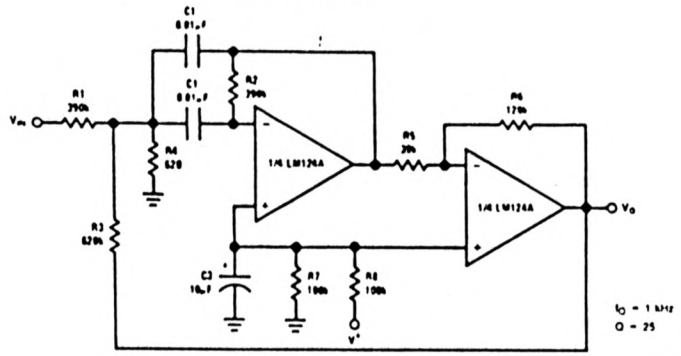


For $\delta << 1$ and $R_f >> R$

$V_O = V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Bandpass Active Filter



TL/H/9299-31

ANALOG DEVICES

12- and 14-Bit Hybrid Synchro/ Resolver-to-Digital Converters

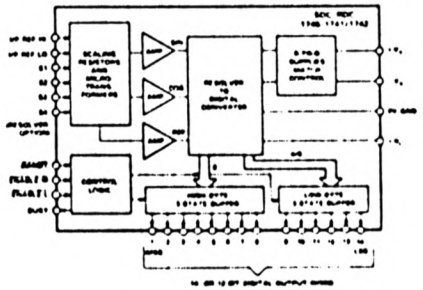
SDC/RDC1740/1741/1742

FEATURES
Internal Isolating Transformers
Military Temperature Range
Three Accuracy Options
14-Bit or 12-Bit Resolution
High, Continuous Tracking Rate
32-Pin Welded Metal Package
Hermetically Sealed
Ratiometric Conversion
Laser Trimmed – No External Adjustment
Three-State Latched Outputs

APPLICATIONS
Flight Instrumentation Systems
Military Servo Control Systems
Artillery Fire Control Systems
Avionic Systems
Antenna Monitoring
Robotics
Engine Controllers
Coordinate Conversion
Axis Transformation
CNC Machine Tooling
Process Control

GENERAL DESCRIPTION
The SDC/RDC1740/1741/1742 are hybrid 14- or 12-bit continuous tracking synchro or resolver to digital converters contained in 32-pin welded metal packages. In the core of this hybrid the conversion process is performed by a monolithic IC manufactured in Analog Devices proprietary BiMOS II process that combines the advantages of CMOS logic and bipolar high accuracy linear circuits on the same chip. Internal isolating microtransformers are used to provide true isolation of the signal and reference inputs. The 14- or 12-bit digital word is in a three-state digital form available in two bytes. Using separate ENABLE inputs for the most significant 8 bits and the least significant 6 or 4 bits not only simplifies multiplexing of more than one device onto a single data bus, but also enables the INHIBIT input to be used without interrupting the operation of the tracking loop. The converters are hermetically sealed in a 32-pin welded metal package.

SDC/RDC1740/1741/1742 FUNCTIONAL BLOCK DIAGRAM



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MODELS AVAILABLE
The three synchro/resolver-to-digital converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1740XYZ is a 14-bit converter with an overall accuracy of ±5.3 arc minutes and a resolution of 1.3 arc minutes

Model SDC1741XYZ is a 12-bit converter with an overall accuracy of ±15.3 arc minutes and a resolution of 5.3 arc minutes.

Model SDC1742XYZ is a 12-bit converter with an overall accuracy of ±8.5 arc minutes and a resolution of 5.3 arc minutes.

Each model has two operating temperature range versions, those covering the industrial temperature range (0 to +70°C) and the military temperature range (−55°C to +125°C). The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage whether it will accept synchro or resolver format. To ensure a high level of reliability each converter receives stringent precap visual inspection, environmental screening and final electrical test.

Military temperature range devices and those processed to high reliability screening standards (suffix B) receive further levels of testing and screening to ensure high levels of reliability. More information about the option codes is given under the heading Ordering Information.

SPECIFICATIONS (typical at 25°C unless otherwise specified)

Parameter	SDC/RDC1740	SDC/RDC1741	SDC/RDC1742	Units	Comments	Notes
CONVERTER PERFORMANCE						
Accuracy	±5.3 max	±15.3 max	±8.5 max	arc min		1, 3
Tracking Rate	27 min	18 min	**	revs		4
Resolution	14	12	**	Bits	Output Coding Parallel Natural Binary	
	(1 LSB = 1.3 arc min)	(1 LSB = 5.3 arc min)	**			
Signal & Reference Frequency	400	*	*	Hz	Option X1Z	
	2.6	*	*	kHz	Option X4Z	
Repeatability of Position Output	1	*	*	LSB		4
Bandwidth	180	150	**	Hz		4
SIGNAL INPUT IMPEDANCE						
90V Signal	200	*	*	kΩ	Resistive Tolerance ±2%	4
26V Signal	57.7	*	*	kΩ		4
11.8V Signal	26	*	*	kΩ		4
REFERENCE INPUTS						
Reference Voltage	11.8, 26, 115	*	*	V rms	See Ordering Information	
Reference Impedance						
115V Ref	120	*	*	kΩ	Resistive Tolerance ±5%	4
26V Ref	27	*	*	kΩ		4
11.8V Ref	12.3	*	*	kΩ		4
ACCELERATION CONSTANT	56000	11000	**	sec^{-2}	Symbol K_v	4
LARGE STEP RESPONSE	85 typ	60 typ	**	ms	179° Step for Settling to	1, 3
	100 max	75 max	**	ms	1 LSB of Error	
POWER LINES						
$+V_S$ = +15V	28 typ 35 max	*	*	mA	Quiescent Condition	1, 3
$-V_S$ = −15V	28 typ 35 max	*	*	mA	Quiescent Condition	1, 3
V_L = +5V	35 typ 56 max	*	*	mA	Quiescent Condition	1, 3
Power Dissipation	1.4 max	*	*	W		
DIGITAL INPUTS (INHIBIT, ENABLE L, ENABLE M)						
V (Input High)	2 min	*	*	V dc	V_L = +5V	1, 3
V (Input Low)	0.7 max	*	*	V dc	V_L = +5V	1, 3
I (Input High)	20 max	*	*	μA	V_{IH} = 2.4V	1, 3
I (Input Low)	−400 max	*	*	μA	V_{IL} = 0.4V	1, 3
ENABLE AND DISABLE TIME	80 max	*	*	ns		2, 4
INHIBIT						
Sense	Logic Low to INHIBIT	*	*			
		*	*			
Time to Data Stable (after Negative-Going Edge of INHIBIT)	640 max	*	*	ns		4
BUSY OUTPUT						
Sense	Active Logic High when converter position output changing.					
Timing	Positive going edge 50ns before change in position output.					
Width	400 typ	*	*	ns		1, 3
	200 min	*	*	ns		1, 3
	600 max	*	*	ns		1, 3
Load	2 min	*	*	TTL		4
DIGITAL OUTPUTS						
Voltage Levels						
Logic High	2.4 min	*	*	V dc	V_L = +5V, I_{OH} = −240μA	1, 3
Logic Low	0.4 max	*	*	V dc	V_L = +5V I_{OL} = 9.6mA	1, 3
Load	6 max	*	*	TTL		

Parameter	SDC/RDC1740	SDC/RDC1741	SDC/RDC1742	Units	Comments	Notes
OPERATING TEMPERATURE RANGE						
Option 5YZ	0 to + 70	*	*	°C		
Option 4YZ	−55 to +125	*	*	°C		
DIMENSIONS	1.74 × 1.14 × 0.28	*	*	Inch	See Package	4
	(44.2 × 28.9 × 7.1)	*	*	mm	Information	
WEIGHT	0.86 max	*	*	oz		4
	25 max	*	*	grams		

NOTES
[1]Specified over the appropriate operating temperature range and for: (a) ± 10% signal and reference amplitude variation; (b) ± 10% signal and reference harmonic distortion; (c) ±5% power supply variation; (d) ± 10% variation in reference frequency.
[2]$\overline{\text{ENABLE M}}$ enables most significant 8 bits.
$\overline{\text{ENABLE L}}$ enables least significant 4 bits (or 6 bits for SDC/RDC1740).
[3]100% tested at nominal values of power supplies, input signal voltages and operating frequency.
[4]Guaranteed by design.

*Specifications same as SDC/RDC1740.
**Specifications same as SDC/RDC1741.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

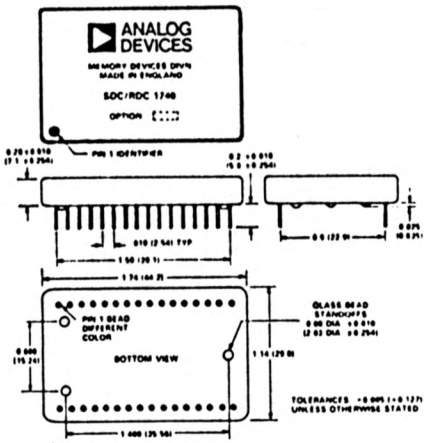
$+V_S$[1] to GND . . . . . +17.25V dc
$-V_S$ to GND . . . . . −17.25V dc
$+V_L$[2] to GND . . . . . +7V dc
Reference Input HI to GND . . . . . ±350V dc
Reference Input LO to GND . . . . . ±350V dc
Common Mode Range . . . . . 175V rms
S1, S2, S3, S4 to GND . . . . . ±350V dc
Any Logical Input to GND . . . . . −0.4V to $+V_L$
Case to GND . . . . . ±20V dc
Storage Temperature Range . . . . . −65°C to +150°C

CAUTION:
[1]Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
[2]The +5V power supply must never go below GND potential.

NOTE
Absolute maximum ratings are those values beyond which damage to the device may occur.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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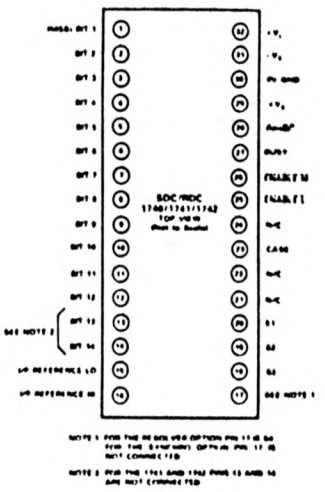
PIN CONFIGURATION



Bit Number	Weight in Degrees
1 (MSB)	180 0000
2	90 0000
3	45 0000
4	22 5000
5	11 2500
6	5 6250
7	2 8125
8	1 4063
9	0 7031
10	0 3516
11	0 1758
12 (LSB for 1741/1742)	0 0879
13	0 0439
14 (LSB for 1740)	0 0220

Table I. Bit Weight Table

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1-14	Bit 1-14 (1740)	Parallel output data bits.
1-12	Bit 1-12 (1741/1742)	
15	REF LO	Input pins for the reference signal.
16	REF HI	
17	S4 OR N/C	S4 signal input for Resolver option. N/C for Synchro option.
18	S3	
19	S2	Synchro/Resolver input signals.
20	S1	
21	N/C	No Connection.
22	N/C	No Connection.
23	CASE	Should be connected to 0V GND.
24	N/C	No Connection.
25	$\overline{\text{ENABLE L}}$	$\overline{\text{ENABLE L}}$ enables the 6 or 4 least significant bits.
26	$\overline{\text{ENABLE M}}$	$\overline{\text{ENABLE M}}$ enables the 8 most significant bits. Logic High sets the output data bits to a high impedance state; a Logic Low presents the data in the latches to the output pins.
27	BUSY	Converter busy. A Logic High output indicates that the output latches are being updated and data should not be transferred.
28	INHIBIT	Logic Low inhibits the data transfer from the counter to the output latches.
29	$+V_S$	Main positive power supply.
30	0V GND	Power supply ground.
31	$-V_S$	Main negative power supply.
32	$+V_L$	Logic power supply.

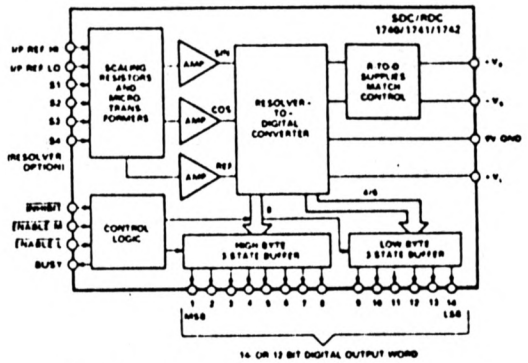


Figure 1. Functional Diagram of the SDC/RDC1740/1741/1742

THEORY OF OPERATION

In the synchro-to-digital converter configuration, the 3-wire synchro output should be connected to S1, S2 and S3 on the unit and the Scott T transformer pair will convert these signals into resolver format, i.e.,

$V_1 = K E_0 \sin \omega t \sin \theta$ (SIN)
$V_2 = K E_0 \sin \omega t \cos \theta$ (COS)

where θ is the angle of the synchro shaft.

In the resolver-to-digital converter configuration, the 4-wire resolver output should be connected to S1, S2, S3 and S4 on the unit and the transformers will act purely as isolators.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

V_1 is multiplied by COSϕ and V_2 is multiplied by SINϕ to give:

$K E_0 \sin \omega t \sin \theta \cos \phi$
and $K E_0 \sin \omega t \cos \theta \sin \phi$.

These signals are subtracted by the error amplifier to give:

$K E_0 \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$
or $K E_0 \sin \omega t \sin (\theta - \phi)$.

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null $\sin (\theta - \phi)$. The digital output (counter ϕ), then represents the synchro/resolver shaft angle θ within the specified accuracy of the converter.

$\overline{\text{INHIBIT}}$ INPUT

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a busy pulse to refresh the output data.

$\overline{\text{ENABLE}}$ INPUTS

The $\overline{\text{ENABLE}}$ inputs determine the state of the output data. A Logic High maintains the output data pins in the high impedance condition, and application of a Logic Low presents the data in the latches to the output pins. $\overline{\text{ENABLE}}$ M enables the most significant 8 bits, while $\overline{\text{ENABLE}}$ L, enables the least significant 4 bits (6 bits in the SDC/RDC1740). The operation of the $\overline{\text{ENABLE}}$ inputs has no effect on the conversion process.

DATA TRANSFER

Data transfer can be accomplished using either the $\overline{\text{INHIBIT}}$ input or the trailing edge, positive to negative transition of the BUSY pulse output.

The data will be valid 640ns after the application of a Logic Lo to the $\overline{\text{INHIBIT}}$ input. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied and allows time for an active busy pulse to clear. By using the $\overline{\text{ENABLE}}$ M and $\overline{\text{ENABLE}}$ L inputs the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a Logic Hi state to enable the output latches to be updated.

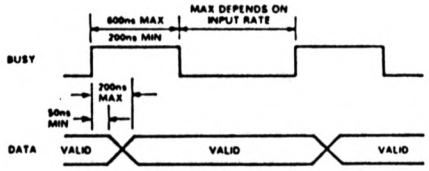


Figure 2. Timing Diagram

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STANDARD PROCESSING (5YZ OPTION)

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Conditions
1. Preseal Burn In	64 hrs at +125°C
2. Precap Visual Inspection	In-house criteria
3. Seal Test, Fine and Gross	In-house criteria
4. Final Electrical Test	Performed at +25°C
Extended temperature range versions receive additional processing as follows:	
Final Electrical Test	Performed at max and min operating temperatures

PROCESSING FOR HIGH RELIABILITY

Process	Conditions
1. Preseal Burn In	64 hrs at +125°C
2. Precap Visual Inspection	2017
3. Temperature Cycling	10 Cycles, −65°C to +150°C
4. Constant Acceleration	5000G, Y1 Plane
5. Interim Electrical Tests	
6. Operating Burn In	96 hours @ +125°C
7. Seal Test, Fine and Gross	1014
8. Final Electrical Testing (Group A)	Performed at T_{max}, $T_{ambient}$ and T_{min}
9. External Visual Inspection	2009

NOTE
Test and screening data can be supplied. Further information on request.

OTHER PRODUCTS

Many other hybrid products concerned with the conversion of synchro data are manufactured by Analog Devices, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

The *SDC/RDC1767* and SDC/RDC1768 are hybrid synchro-to-digital converters with isolating microtransformers similar to the SDC/RDC1740/41/42 described on this data sheet with the additional features of analog velocity output and dc error output.

The *OSC1758* is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts, over a frequency range of 0 to 10kHz.

The *DRC1745* and *DRC1746* are 14- and 16-bit natural binary latched output hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc mins, and the outputs can supply 2VA at 7V rms.

ORDERING INFORMATION

For full definition, the converter part number should be suffixed by an option code. All the standard options and their option codes are shown below. For options not shown, please consult Analog Devices.

SDC 174A X Y Z B

B = High-Rel Processing

Z = 1 Signal 11.8V Reference 26V Synchro
Z = 2 Signal 90V Reference 115V Synchro
Z = 3 Signal 11.8V Reference 11.8V Resolver
Z = 4 Signal 26V Reference 26V Resolver
Z = 8 Signal 11.8V Reference 26V Resolver

SDC = Synchro-to-Digital Converter
RDC = Resolver-to-Digital Converter

1740 = 14-Bit Resolution, ±5.3 arc min Accuracy
1741 = 12-Bit Resolution, ±15.3 arc min Accuracy
1742 = 12-Bit Resolution, ±8.5 arc min Accuracy

Y = 1 400Hz Reference Frequency
Y = 4 2.6kHz Reference Frequency

X = 4 −55°C to +125°C Operating Temperature Range
X = 5 0 to +70°C Operating Temperature Range

ANALOG DEVICES

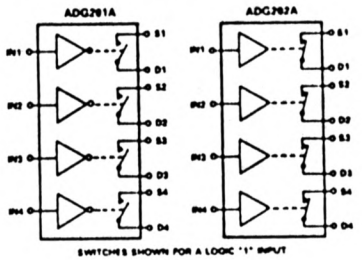
CMOS Quad SPST Switches

ADG201A/ADG202A

FEATURES

44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (60Ω)
Low Leakage (0.5nA)
Extended Plastic Temperature Range (−40°C to +85°C)
Low Power Dissipation (33mW)
Standard 16-Pin Dips and 20-Terminal Surface Mount Packages
Superior Second Source:
ADG201A Replaces DG201A, HI-201
ADG202A Replaces DG202

ADG201A/ADG202A FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

ORDERING INFORMATION[1]

Temperature Range and Package Options[2, 3]		
−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
Plastic DIP (N-16)	Hermetic (Q-16)	Hermetic (Q-16)
ADG201AKN ADG202AKN	ADG201ABQ ADG202ABQ	ADG201ATQ ADG202ATQ
PLCC[4] (P-20A)		LCCC[5] (E-20A)
ADG201AKP ADG202AKP		ADG201ATE ADG202ATE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. See Analog Devices Military Products Data Book (1987) for military data sheet.
[2]See Section 14 for package outline information.
[3]Also available in SOIC packages (ADG201AKR, ADG202AKR)
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

PRODUCT HIGHLIGHTS

1. Extended Signal Range:
These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.

2. Single Supply Operation:
For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.

3. Low Leakage:
Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

ADG201A IN	ADG202A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table I. Truth Table

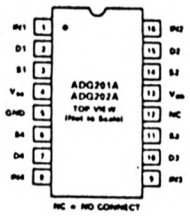
SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, unless otherwise noted)

Parameter	K Version 25°C	K Version −40°C to +85°C	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}	60		60		60		Ω typ	$-10V \le V_S \le +10V$
	90	145	90	145	90	145	Ω max	$I_{DS} = 1.0mA$
								Test Circuit 1
R_{ON} vs. V_D (V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	$V_S = 0V, I_{DS} = 1mA$
I_S (OFF)	0.5		0.5		0.5		nA typ	$V_D = \pm 14V, V_S \mp 14V$, Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)	0.5		0.5		0.5		nA typ	$V_D = \pm 14V, V_S \mp 14V$, Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)	0.5		0.5		0.5		nA typ	$V_D = \pm 14V$, Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{TRANS}	30		30		30		ns typ	
t_{ON}	300		300		300		ns max	Test Circuit 4
t_{OFF}	250		250		250		ns max	Test Circuit 4
OFF Isolation	80		80		80		dB typ	$V_S = 10V_{p\text{-}p}$, f = 100kHz
								$R_L = 75\Omega$, Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_D, C_S (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	$R_S = 0\Omega, C_L = 1000pF, V_S = 0V$
								Test Circuit 5
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}		2		2		2	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}		0.2		0.2		0.2	mA max	
Power Dissipation		33		33		33	mW max	

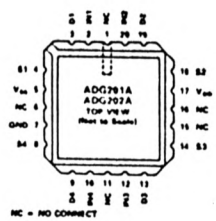
NOTES
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice

PIN CONFIGURATIONS

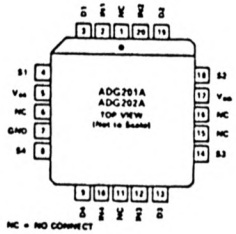
DIP



LCCC



PLCC



ABSOLUTE MAXIMUM RATINGS*
(T_A = + 25°C unless otherwise stated)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	– 25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} – 0.3V to V_{DD} + 0.3V
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs[1]	
Voltage at IN	V_{SS} – 2V to V_{DD} + 2V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to + 75°C	470mW
Derates above + 75°C by	6mW/°C
Operating Temperature	
Commercial (K Version)	– 40°C to + 85°C
Industrial (B Version)	– 40°C to + 85°C
Extended (T Version)	– 55°C to + 125°C
Storage Temperature Range	– 65°C to + 150°C
Lead Temperature (Soldering 10sec)	+ 300°C

NOTE
[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

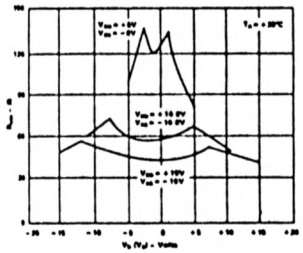
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

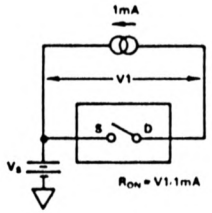
7

Typical Performance Characteristics and Test Circuits

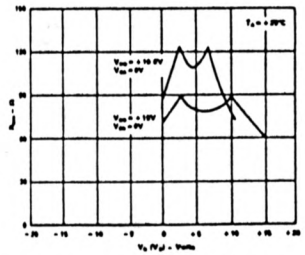
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



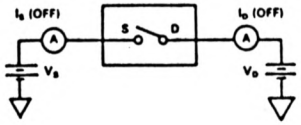
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



Test Circuit 1



R_{ON} as a Function of V_D (V_S): Single Supply Voltage



Test Circuit 2

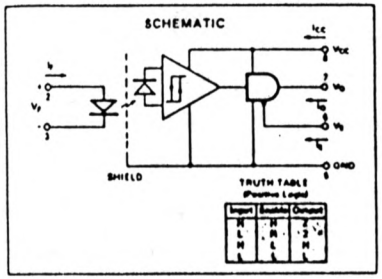
HEWLETT PACKARD

LOW INPUT CURRENT LOGIC GATE OPTOCOUPLER

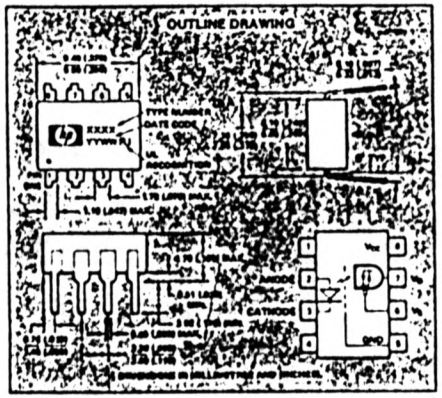
HCPL-2200

TECHNICAL DATA JANUARY 1986

SCHEMATIC



OUTLINE DRAWING



Features

- COMPATIBLE WITH LSTTL, TTL, AND CMOS LOGIC
- 2.5 MBAUD GUARANTEED OVER TEMPERATURE
- LOW INPUT CURRENT (1.6 mA)
- WIDE V_{CC} RANGE (4.5 TO 20 VOLTS)
- THREE STATE OUTPUT (NO PULLUP RESISTOR REQUIRED)
- GUARANTEED PERFORMANCE FROM 0° C TO +85° C
- INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Applications

- Isolation of High Speed Logic Systems
- Computer-Peripheral Interfaces
- Microprocessor System Interfaces
- Ground Loop Elimination
- Pulse Transformer Replacement
- Isolated Buss Driver
- High Speed Line Receiver

Description

The HCPL-2200 is an optically coupled logic gate that combines a GaAsP LED and an integrated high gain photon detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides typically 0.1 mA of differential mode noise immunity and eliminates the potential for output signal chatter. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1,000 volts/μsec. Higher CMR specifications are available upon request. Improved power supply rejection eliminates the need for special power supply bypassing precautions.

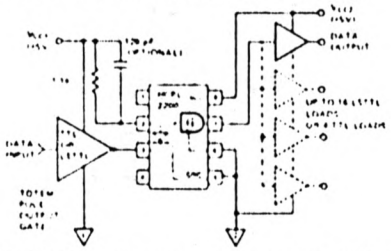
The Electrical and Switching Characteristics of the HCPL-2200 are guaranteed over the temperature range of 0° C to 85° C. The HCPL-2200 is guaranteed to operate over a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic. Low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 160 nsec when a 120 pF peaking capacitor is used in parallel with the 1.1KΩ current limiting resistor.

The HCPL-2200 is useful for isolating high speed logic interfaces, buffering of input and output lines, and implementing isolated line receivers in high noise environments.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	+20	Volts
Enable Voltage High	V_{EH}	2.0	20	Volts
Enable Voltage Low	V_{EL}	0.0	0.8	Volts
Forward Input Current	$I_{F(ON)}$	1.6	5	mA
Forward Input Current	$I_{F(OFF)}$	—	0.1	mA
Operating Temperature	T_A	0	85	°C
Fan Out	N	—	4	TTL Loads

Recommended Circuit Design



The 120 pF capacitor may be omitted in applications where 50 ns propagation delay is sufficient.

Figure 1. Recommended LSTTL to LSTTL Circuit.

Absolute Maximum Ratings

No Derating Required up to 70° C

Storage Temperature ..... -55° C to +125° C
Operating Temperature ..... -40° C to +85° C [1]
Lead Solder Temperature ..... 260° C for 10 s
1.6 mm below seating plane
Average Forward Input Current — I_F ..... 10 mA
Peak Transient Input Current — I_F 1A
(≤ 1 μs Pulse Width, 300 pps)
Reverse Input Voltage 5V
Supply Voltage — V_{CC} ..... 0.0V min., 20V max.
Three State Enable Voltage
— V_E ..... -0.5V min., 20V max.
Output Voltage — V_O ..... -0.5V min., 20V max.
Total Package Power
Dissipation — P_T ..... 210 mW [1]
Average Output Current — I_O ..... 25 mA

Electrical Characteristics

For 0° C < T_A < +85° C, 4.5 V < V_{CC} < 20 V, 1.6 mA < $I_{F(ON)}$ < 5 mA, 2.0 V < V_{EH} < 20 V, 0.0 V < V_{EL} < 0.8 V, 0 mA < I_F (off) < 0.1 mA. All Typicals at T_A = 25° C, V_{CC} = 5V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 0.4 mA, 4 TTL Loads		4	
Logic High Output Voltage	V_{OH}	2.4	*		Volts	I_{OH} = -2.6 mA, V_{OH} = V_{CC} - 2.1V		3	
Output Leakage Current (V_{OUT} = V_{CC})	I_{OHH}			100	μA	V_O = 5.5V	I_F = 5 mA		
				500	μA	V_O = 20V	V_{CC} = 4.5V		
Logic High Enable Voltage	V_{EH}	2.0			Volts				
Logic Low Enable Voltage	V_{EL}			0.8	Volts				
Logic High Enable Current	I_{EH}			-20	μA	V_{EN} = 2.7V			
				-100	μA	V_{EN} = 5.5V			
			-0.04	-250	μA	V_{EN} = 20V			
Logic Low Enable Current	I_{EL}			-0.32	mA	V_{EN} = 0.4V			
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5V	I_F = 0 mA		
			5.25	7.5	mA	V_{CC} = 20V	V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5V	I_F = 5 mA,		
			3.1	6.0	mA	V_{CC} = 20V	V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			-20	μA	V_O = 0.4V	V_{EN} = 2V, I_F = 5 mA		
	I_{OZH}			20	μA	V_O = 2.4V	V_{EN} = 2V, I_F = 0		
				100	μA	V_O = 5.5V			
				500	μA	V_O = 20V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = V_{CC} = 5.5V	I_F = 0 mA		2
		40			mA	V_O = V_{CC} = 20V			
Logic High Short Circuit Output Current	I_{OSH}	-10			mA	V_{CC} = 5.5V	I_F = 5 mA,		2
		-25			mA	V_{CC} = 20V	V_O = GND		
Input Current Hysteresis	I_{HYS}		0.12		mA	V_{CC} = 5V		4	
Input Forward Voltage	V_F		1.5	1.70	Volts	I_F = 5 mA, T_A = 25° C		5	
Input Reverse Breakdown Voltage	V_R	5			Volts	I_R = 10 μA at T_A = 25° C			
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.7		mV/° C	I_F = 5 mA			
Input-Output Insulation	I_{I-O}*			1	μA	45% RH, t = 5s, V_{I-O} = 3kV dc, T_A = 25° C			3, 7
OPT. 010	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min.			8
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		90		pF	f = 1 MHz, V_F = 0V, Pins 2 and 3			

*For JEDEC registered parts

Switching Characteristics

For $0°C \le T_A^{[1]} \le 85°C$, $4.5V \le V_{CC} \le 20V$, $1.6\ mA \le I_{F(ON)} \le 5\ mA$, $0.0\ mA \le I_{F(OFF)} \le 0.1\ mA$. All Typicals at $T_A = 25°C$, $V_{CC} = 5V$, $I_{F(ON)} = 3\ mA$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		110	300	ns	Without Peaking Capacitor	6,7,8	4,5
			160	300	ns	With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		170	300	ns	Without Peaking Capacitor	6,7,8	4,5
			115	300	ns	With Peaking Capacitor		
Output Enable Time to Logic High	t_{PZH}		25		ns		8,10	
Output Enable Time to Logic Low	t_{PZL}		28		ns		8,9	
Output Disable Time from Logic High	t_{PHZ}		105		ns		8,10	
Output Disable Time from Logic Low	t_{PLZ}		80		ns		8,9	
Output Rise Time (10-90%)	t_r		55		ns		6,11	
Output Fall Time (90-10%)	t_f		15		ns		6,11	
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$	1000	10,000		V/μs	$T_A = 25°C$, $I_F = 1.6\ mA$, $V_{CM} = 50\ V$	12,13	6
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$	1000	10,000		V/μs	$T_A = 25°C$, $I_F = 0$, $V_{CM} = 50\ V$	12,13	6

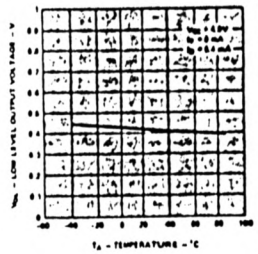


Figure 2. Typical Logic Low Output Voltage vs. Temperature

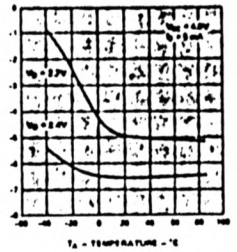


Figure 3. Typical Logic High Output Current vs. Temperature

Figure 4. Output Voltage vs. Forward Input Current

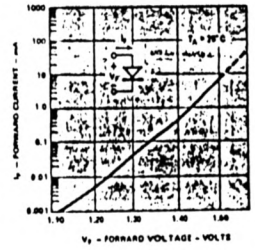


Figure 5. Typical Input Diode Forward Characteristic

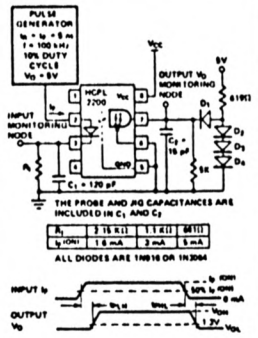


Figure 6. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

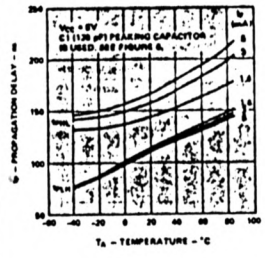


Figure 7. Typical Propagation Delays vs. Temperature

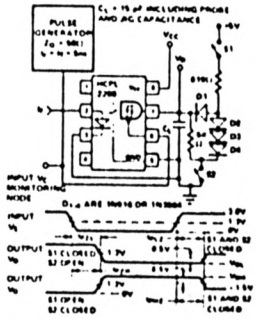


Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

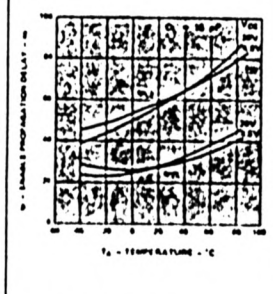


Figure 9. Typical Logic Low Enable Propagation Delay vs. Temperature

Figure 10. Typical Logic High Enable Propagation Delay vs. Temperature

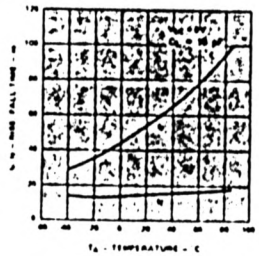


Figure 11. Typical Rise, Fall Time vs. Temperature

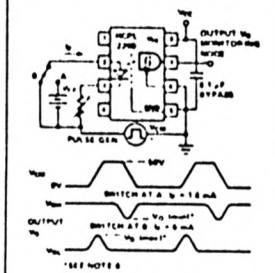


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

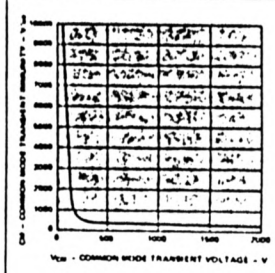


Figure 13. Typical Common Mode Transient Immunity vs. Common Mode Transient Amplitude

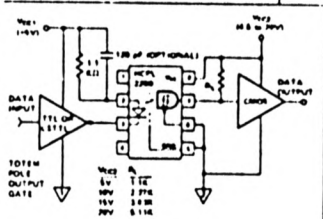


Figure 14. LSTTL to CMOS Interface Circuit

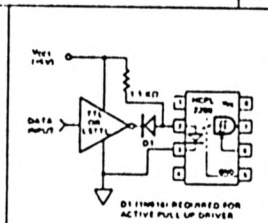


Figure 15. Recommended LED Drive Circuit

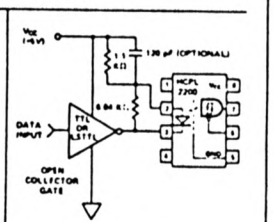


Figure 16. Series LED Drive with Open Collector Gate (6.04 kΩ Resistor Shunts I_{OH} from the LED)

The 120 pF capacitor may be omitted in applications where 500 ns propagation delay is sufficient.

Notes:

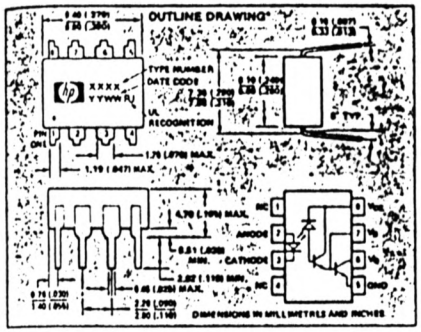
1. Derate total package power dissipation, P, linearly above 70° C free air temperature at a rate of 4.5 mW/° C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.
5. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
6. $|CM_L|$ is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8V$). $|CM_H|$ is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0V$).
7. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec test.
8. See Option 010 data sheet for more information.

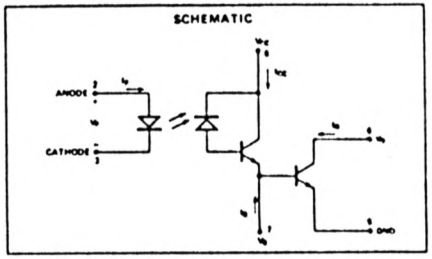
HEWLETT PACKARD

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

6N138
6N139

TECHNICAL DATA JANUARY 1986





OPTOCOUPLERS

Features

- HIGH CURRENT TRANSFER RATIO—2000% TYPICAL
- LOW INPUT CURRENT REQUIREMENT — 0.5 mA
- TTL COMPATIBLE OUTPUT — 0.1 V V_{OL} TYPICAL
- HIGH COMMON MODE REJECTION — 500 V/μs
- PERFORMANCE GUARANTEED OVER TEMPERATURE 0° C to 70° C
- BASE ACCESS ALLOWS GAIN BANDWIDTH ADJUSTMENT
- HIGH OUTPUT CURRENT — 60 mA
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF U.L. (FILE NO. E55361) FOR DIELECTRIC WITHSTAND PROOF TEST VOLTAGES OF 1440 Vac, 1 MINUTE AND 2500 Vac, 1 MINUTE (OPTION 010).

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photon detector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the Vcc and Vo terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70° C operating range for only 0.5 mA of LED current.

The 6N138 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70° C for an LED current of 1.6 mA (1 TTL Unit load (U.L.)). A 300% minimum CTR enables operation with 1 U.L. out with a 2.2 kμ pull-up resistor.

Applications

- Ground Isolate Most Logic Families – TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL
- Low Input Current Line Receiver – Long Line or Party line
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator – Low Input Power Dissipation
- Low Power Systems – Ground Isolation

Absolute Maximum Ratings*

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Average Input Current – I_F ..... 20mA [1]
Peak Input Current – I_F 40mA
(50% duty cycle, 1ms pulse width)
Peak Transient Input Current – I_F 1.0A
(≤ 1μs pulse width, 300 pps)
Reverse Input Voltage – V_R 5V
Input Power Dissipation ..... 35mW [2]
Output Current – I_O (Pin 6) ..... 60mA [3]
Emitter-Base Reverse Voltage (Pin 5-7) 0.5V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)
6N138 .....−0.5 to 7V
6N139 .....−0.5 to 18V
Output Power Dissipation ..... 100mW [4]

See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

*JEDEC Registered Data.

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C to 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N139	400	3000		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V	3	5,6
			500	1600			I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
		6N138	300	1600		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}	6N139		0.1	0.4	V	I_F = 1.6mA, I_O = 6.4mA, V_{CC} = 4.5V	1,2	6
				0.1	0.4		I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V		
				0.2	0.4		I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V		
		6N138		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}*	6N139		0.05	100	μA	I_F = 0mA, V_O = V_{CC} = 18V		6
		6N138		0.1	250	μA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}			0.4		mA	I_F = 1.6mA, V_O = Open, V_{CC} = 5V		6
Logic High Supply Current	I_{CCH}			10		nA	I_F = 0mA, V_O = Open, V_{CC} = 5V		6
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	4	
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10μA, T_A = 25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			−1.9		mV/°C	I_F = 1.6mA		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation	I_{I-O}*				1	μA	45% RH, t = 5s, V_{I-O} = 3kV dc, T_A = 25°C		7,11
Option 010	V_{ISO}	2500				Vrms	RH = 50%, t = 1 min		12
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7

*JEDEC registered data.

**All typicals at T_A = 25°C and V_{CC} = 5V, unless otherwise noted.

Switching Specifications

AT T_A = 25°C, V_{CC} = 5V

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}*	6N139		5	25	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	6,8
				0.2	1		I_F = 12mA, R_L = 270Ω		
		6N138		1.6	10	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}*	6N139		18	60	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	6,8
				2	7		I_F = 12mA, R_L = 270Ω		
		6N138		10	35	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Common Mode Transient Immunity at Logic High Level Output	$\lvert CM_H \rvert$			500		V/μs	I_F = 0mA, R_L = 2.2kΩ, R_{CC} = 0 V_{cm} = 10V_{p-p}	10	9,10
Common Mode Transient Immunity at Logic Low Level Output	$\lvert CM_L \rvert$			500		V/μs	I_F = 1.6mA, R_L = 2.2kΩ, R_{CC} = 0 V_{cm} = 10V_{p-p}	10	9,10

NOTES

1. Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C
2. Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C
3. Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C
4. Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 7 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951.1 for more details.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
10. In applications where dV/dt may exceed 50,000V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} = \frac{1V}{0.15\ I_F\ (mA)}$ kΩ.
11. This is a proof test. This rating is equally validated by a 2500 Vac, 1 sec. test.
12. See Opt. 010 data sheet for more information.

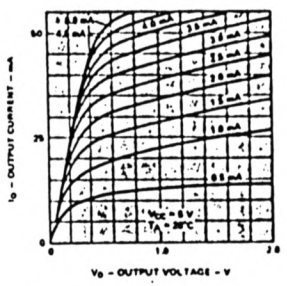


Figure 1. 6N138/6N139 DC Transfer Characteristics

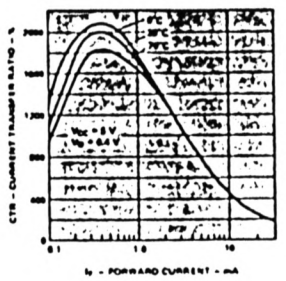


Figure 2. Current Transfer Ratio vs Forward Current 6N138/6N139

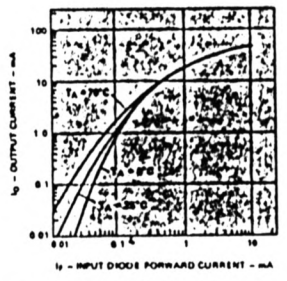


Figure 3. 6N138/6N139 Output Current vs Input Diode Forward Current

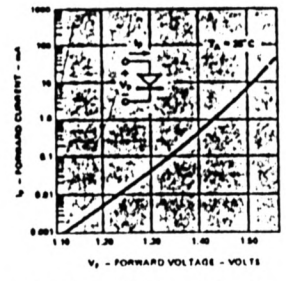


Figure 4. Input Diode Forward Current vs. Forward Voltage.

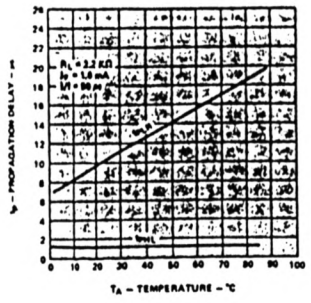


Figure 5. Propagation Delay vs. Temperature.

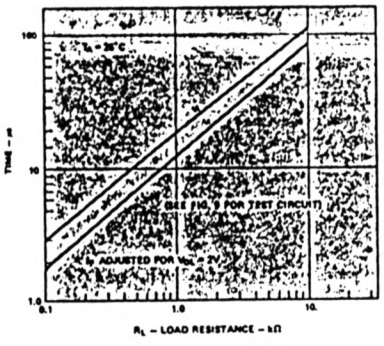


Figure 6. Non Saturated Rise and Fall Times vs. Load Resistance.

D2393, SEPTEMBER 1978 - REVISED JANUARY 1989

19 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- Common-Mode Input Voltage Range Includes V_{CC+}
- Low Noise . . . V_n = 18 nV/$\sqrt{Hz}$ Typ
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL070, TL070A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ

description

The JFET-input operational amplifiers in the TL07__ series are designed as low-noise versions of the TL08__ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07__ series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

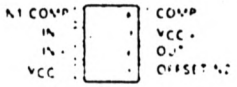
The M suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I suffix devices are characterized for operation from −40°C to 85°C, and the C suffix devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

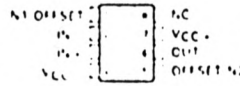
T_A	V_{IO} MAX AT 25°C	PACKAGE							
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (N)	PLASTIC DIP (P)	FLAT PACK (W)
0°C to 70°C	10 mV	TL070CD			TL070CJG			TL070CP	
	6 mV	TL070ACD			TL070ACJG			TL070ACP	
	10 mV	TL071CD			TL071CJG			TL071CP	
	6 mV	TL071ACD			TL071ACJG			TL071ACP	
	3 mV	TL071BCD			TL071BCJG			TL071BCP	
	10 mV	TL072CD			TL072CJG			TL072CP	
	6 mV	TL072ACD			TL072ACJG			TL072ACP	
	3 mV	TL072BCD			TL072BCJG			TL072BCP	
	10 mV	TL074CD		TL074CJ			TL074CN		
	6 mV	TL074ACD		TL074ACJ			TL074ACN		
	3 mV	TL074BCD		TL074BCJ			TL074BCN		
	10 mV						TL075CN		
−40°C to 85°C	6 mV	TL070ID			TL070IJG			TL070IP	
	6 mV	TL071ID			TL071IJG			TL071IP	
	6 mV	TL072ID			TL072IJG			TL072IP	
	6 mV	TL074ID		TL074IJ			TL074IN		
−55°C to 125°C	6 mV		TL071MFK		TL071MJG	TL071ML			
	6 mV		TL072MFK		TL072MJG	TL072ML			
	9 mV		TL074MFK	TL074MJ					TL074MW

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR).

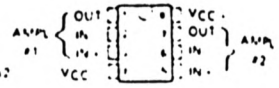
TL070, TL070A
D, JG, OR P PACKAGE
(TOP VIEW)



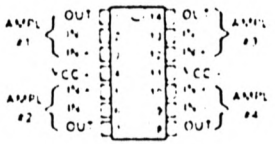
TL071, TL071A, TL071B
D, JG, OR P PACKAGE
(TOP VIEW)



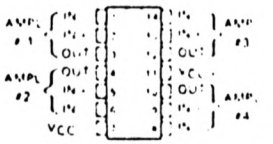
TL072, TL072A, TL072B
D, JG, OR P PACKAGE
(TOP VIEW)



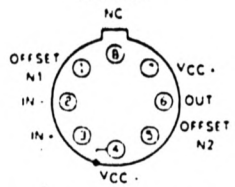
TL074, TL074A, TL074B
D, J, OR N PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



TL075
N PACKAGE
(TOP VIEW)

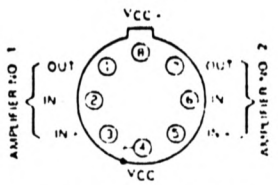


TL071 . . . L PACKAGE
(TOP VIEW)



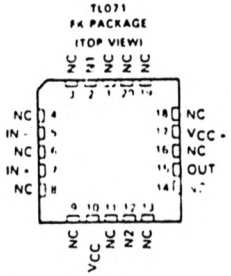
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TL072 . . . L PACKAGE
(TOP VIEW)

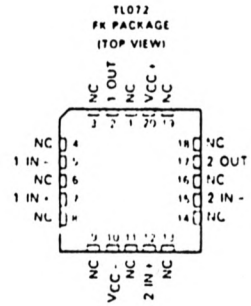


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

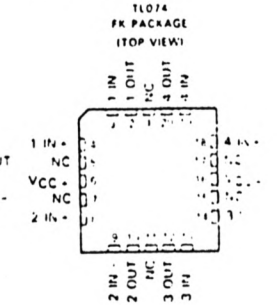
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)

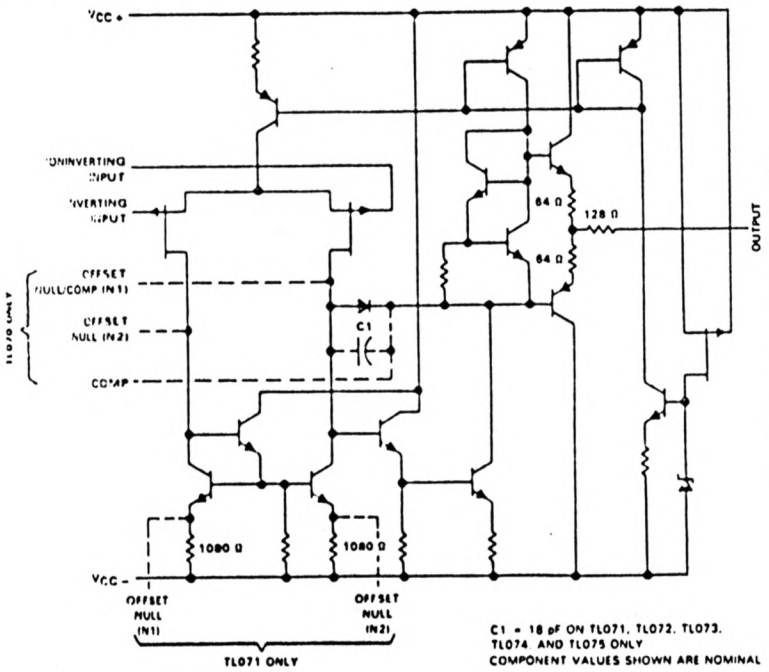


TL074
FK PACKAGE
(TOP VIEW)



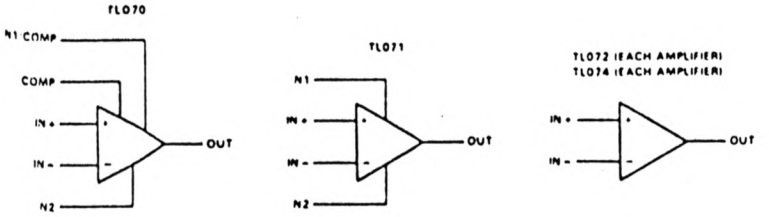
NC – No internal connection.

schematic (each amplifier)



C1 = 18 pF ON TL071, TL072, TL073, TL074 AND TL075 ONLY
COMPONENT VALUES SHOWN ARE NOMINAL

symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL07_M	TL07_I	TL07_C TL07_AC TL07_BC	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	18	V
Supply voltage V_{CC-} (see Note 1)		–18	–18	–18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		–55 to 125	–40 to 85	0 to 70	°C
Storage temperature range		–65 to 150	–65 to 150	–65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J, JG, or W package	300	300	300	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, N, or P package		260	260	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	L package	300			°C

NOTES 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8-pin)	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
D (14-pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (TL07_M)	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (all others)	680 mW	8.2 mW/°C	67°C	656 mW	533 mW	N/A
JG (TL07_M)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (all others)	680 mW	5.6 mW/°C	47°C	528 mW	429 mW	N/A
L	680 mW	6.6 mW/°C	25°C	528 mW	429 mW	165 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

National Semiconductor Corporation

LF444A/LF444 Quad Low Power JFET Input Operational Amplifier

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

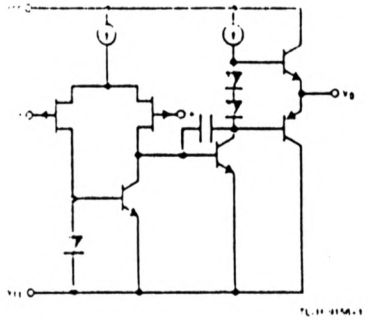
The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

- ¼ supply current of a LM148 — 200 μA/Amplifier (max)
- Low input bias current — 50 pA (max)
- High gain bandwidth — 1 MHz
- High slew rate — 1 V/μs
- Low noise voltage for low power — 35 nV/√Hz
- Low input noise current — 0.01 pA/√Hz
- High input impedance — $10^{12}\Omega$
- High gain V_O = ±10V, R_L = 10k — 50k (min)

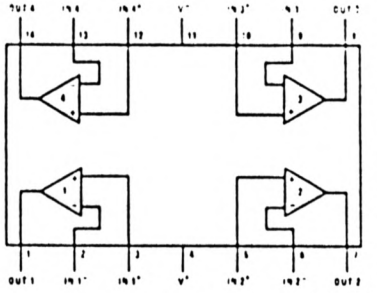
Simplified Schematic

¼ Quad



Connection Diagram

LF444AMD/LF444CD/LF444ACN/LF444CN
Dual-In-Line Package



Top View

Order Number LF444AMD, LF444CD, LF444CJ, LF444CM, LF444CWM, LF444ACN or LF444CN
See NS Package Number D14E, J14A, M14A, M14B or N14A

Ordering Information

LF444XYZ

X indicates electrical grade

Y indicates temperature range

"M" for military, "C" for commercial

Z indicates package type "D", "M" or "N"

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF444A	LF444
Supply Voltage	±22 V	±18V
Differential Input Voltage	±38 V	±30 V
Input Voltage Range (Note 1)	±15 V	±15 V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	D Package	N Package
Power Dissipation (Notes 3 and 11)	500 mW	670 mW
T_J max	150°C	115°C
θ_{JA} (Typical)	100°C/W	85°C/W

	D Package (Note 4)	N Package (Note 4)
Operating Temperature Range	−65°C ≤ T_A ≤ 150°C	
Lead Temperature DIP (Soldering, 10 sec.)	260°C	260°C
ESD rating to be determined		
Soldering Information		
Dual-In-Line Package (Soldering, 10 sec.)	260°C	260°C
Small Outline Package		
Vapor Phase (60 sec.)	215°C	215°C
Infrared (15 sec.)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF444A Min	LF444A Typ	LF444A Max	LF444 Min	LF444 Typ	LF444 Max	Units
V_{OS}	Input Offset Voltage	R_S = 10k, T_A = 25°C			2	5		3	10	mV
		0°C ≤ T_A ≤ +70°C				6.5			12	mV
		−55°C ≤ T_A ≤ +125°C				8				mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ			10			10		μV/°C
I_{OS}	Input Offset Current	V_S = ±15V (Notes 5, 6)	T_j = 25°C		5	25		5	50	pA
			T_j = 70°C			1.5			1.5	nA
			T_j = 125°C			10				nA
I_B	Input Bias Current	V_S = ±15V (Notes 5, 6)	T_j = 25°C		10	50		10	100	pA
			T_j = 70°C			3			3	nA
			T_j = 125°C			20				nA
R_{IN}	Input Resistance	T_j = 25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, V_O = ±10V, R_L = 10 kΩ, T_A = 25°C		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V
CMRR	Common-Mode Rejection Ratio	R_S = 10 kΩ		80	100		70	90		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				0.6	0.8		0.8	1.0	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF444A			LF444			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier-to-Amplifier Coupling			−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C		1			1		V/μs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		1			1		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1 kHz		35			35		nV/√Hz
i_n	Equivalent Input Noise Current	T_A = 25°C, f = 1 kHz		0.01			0.01		pA/√Hz

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely. However, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF444A is available in both the commercial temperature range 0°C ≤ T_A ≤ 70°C and the military temperature range −55°C ≤ T_A ≤ 125°C. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A 'C' indicates the commercial temperature range and an 'M' indicates the military temperature range. The military temperature range is available in 'D' (CERDIP) package only.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for V_S = ±20V for the LF444A and for V_S = ±15V for the LF444. I_B, I_{OS} and I_{CS} are measured at V_{CM} = 0.

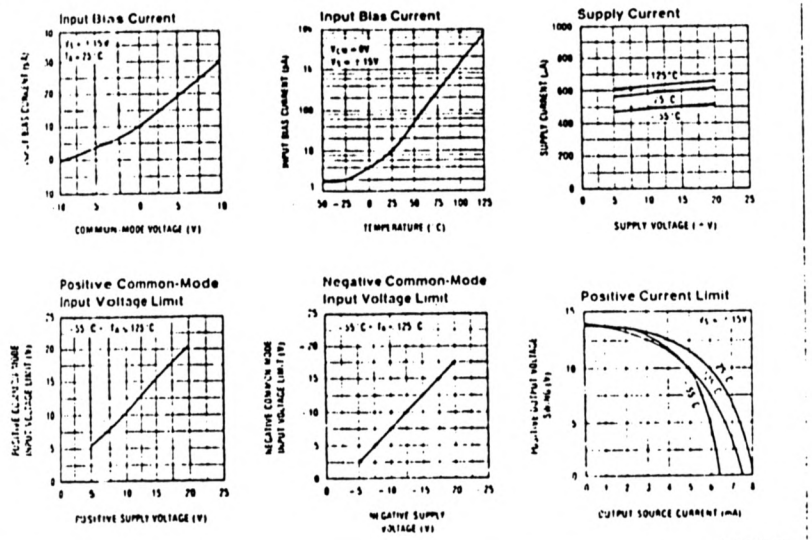
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_j. Due to limited production test time the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation. P_D. T_j = T_A + $\theta_{jA}P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±5V to ±15V for the LF444 and from ±20V to ±5V for the LF444A.

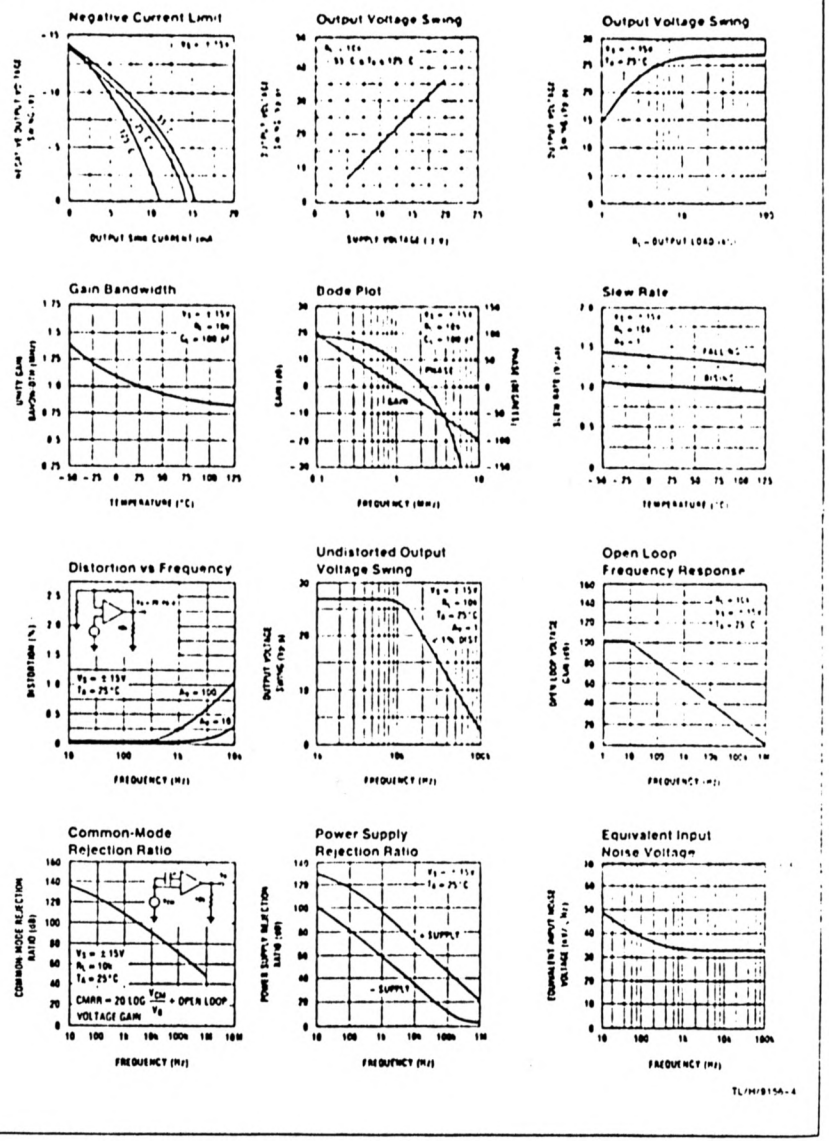
Note 8: Refer to RETS444AX for LF444AMJ military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

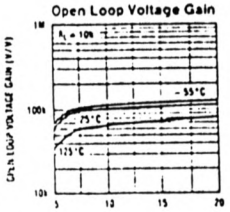


Typical Performance Characteristics (Continued)

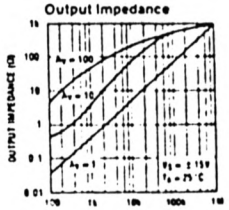


Typical Performance Characteristics (Continued)

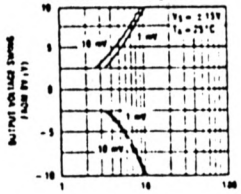
Open Loop Voltage Gain



Output Impedance

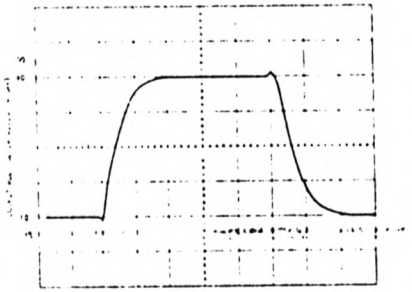


Inverter Settling Time

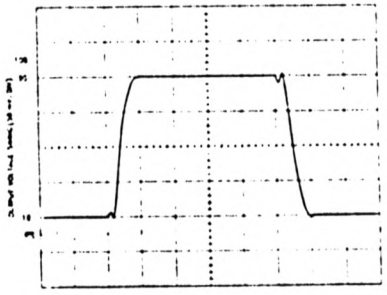


Pulse Response R_L = 10 kΩ, C_L = 10 pF

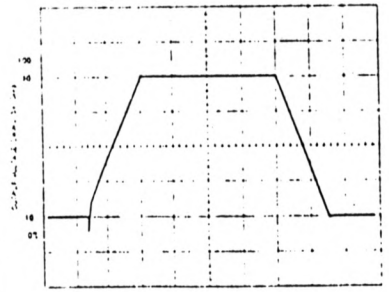
Small Signal Inverting



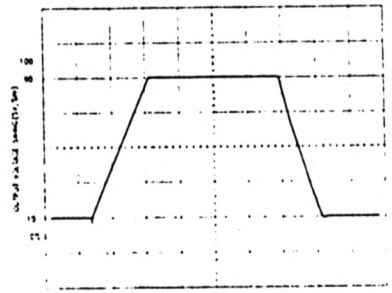
Small Signal Non-Inverting



Large Signal Inverting



Large Signal Non-Inverting



Application Hints

This device is a quad low power op amp with JFET input devices (BIFET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

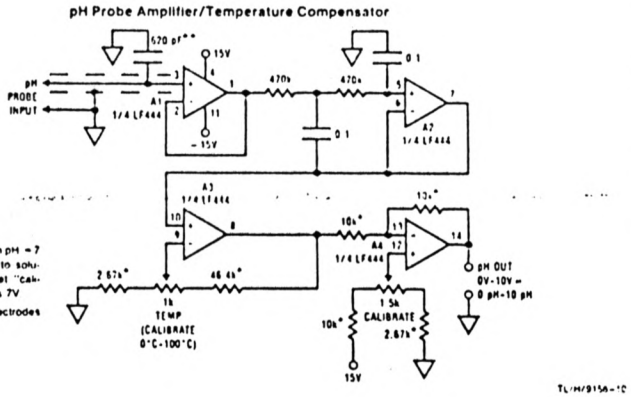
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

pH Probe Amplifier/Temperature Compensator



**Polystyrene

*Film resistor type RN60C

To calibrate, insert probe in pH = 7 solution. Set "temp" dial to solution temperature, then, set "calibrate" dial so output reads 7V.

Typical probe = Ingold Electrodes #465-35

Detailed Schematic

¼ Quad

TL/H/9154–11

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE520

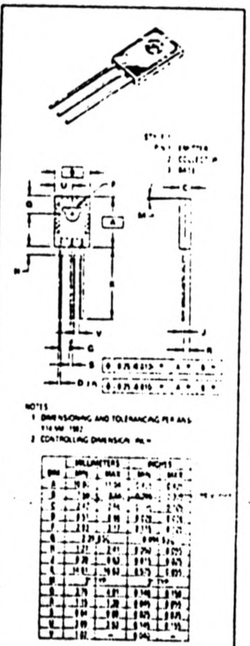
PLASTIC MEDIUM POWER NPN SILICON TRANSISTOR

. . . designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain — h_{FE} = 25 (Min) @ I_C = 1.0 Adc
- Complementary to PNP MJE370

3 AMPERE POWER TRANSISTOR NPN SILICON

30 VOLTS 25 WATTS



CASE 77-06 TO-225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	3.0	Adc
— Peak		7.0	
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.2	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

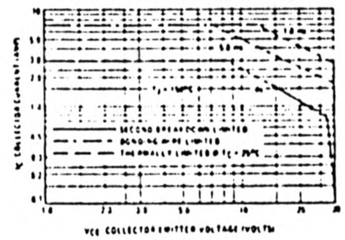
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	30		Vdc
Collector-Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	100	µAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	µAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	25	—	—

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

FIGURE 1 — ACTIVE REGION SAFE OPERATING AREA



The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

FIGURE 2 — DC CURRENT GAIN

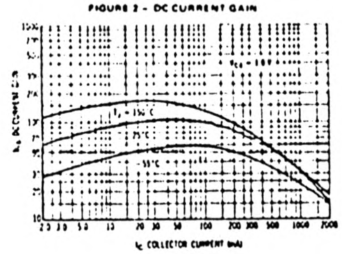


FIGURE 3 — "ON" VOLTAGE

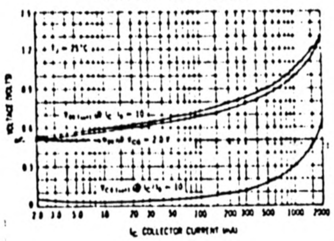
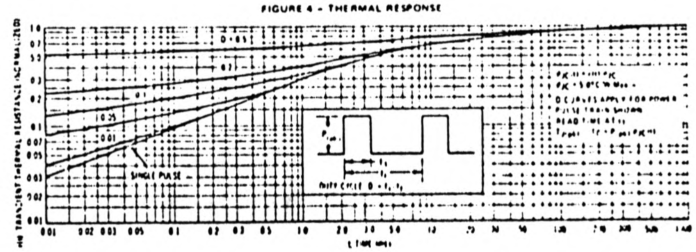


FIGURE 4 — THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM4N45
MTM4N50
MTP4N45
MTP4N50

Designer's Data Sheet

Power Field Effect Transistor

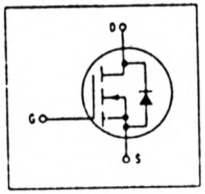
N-Channel Enhancement Mode Silicon Gate TMOS

TMOS

TMOS POWER FETs
4 AMPERES
$r_{DS(on)}$ = 1.5 OHMS
450 and 500 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM4N45 / MTP4N45	MTM4N50 / MTP4N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	4 10		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

MTM4N45
MTM4N50
CASE 1-05
TO-204AA
(TO-3)

MTP4N45
MTP4N50
CASE 221A-02
TO-220AB

THERMAL CHARACTERISTICS

				Unit
Thermal Resistance — Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTM4N45 MTM4N50	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	— —	0.25 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2 Adc)		$r_{DS(on)}$	—	1.5	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) I_D = 4 Adc I_D = 2 Adc, T_J = 100°C		$V_{DS(on)}$	— —	7.5 6	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2 A)		g_{FS}	1.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	27 (Typ)	37	nC
Gate-Source Charge		Q_{gs}	17 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	210 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

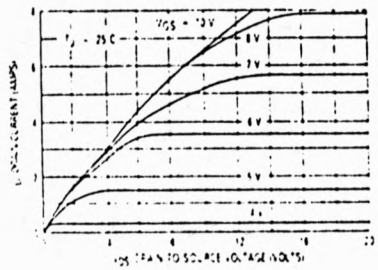


Figure 1. On-Region Characteristics

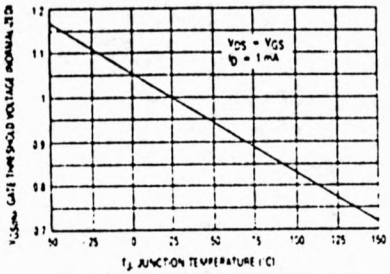


Figure 2. Gate-Threshold Voltage Variation With Temperature

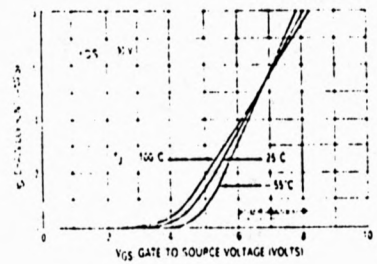


Figure 3. Transfer Characteristics

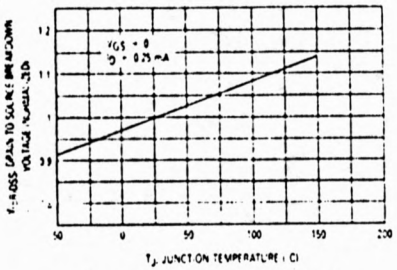


Figure 4. Breakdown Voltage Variation With Temperature

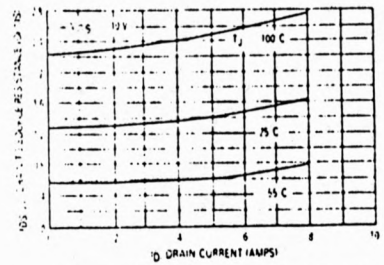


Figure 5. On-Resistance versus Drain Current

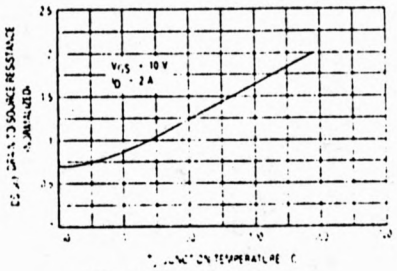


Figure 6. On Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

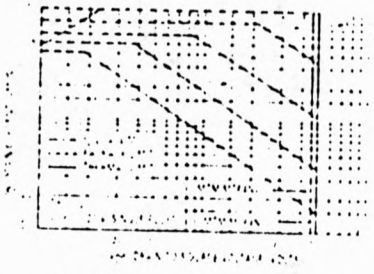


Figure 7. Maximum Rated Forward Biased Safe Operating Area

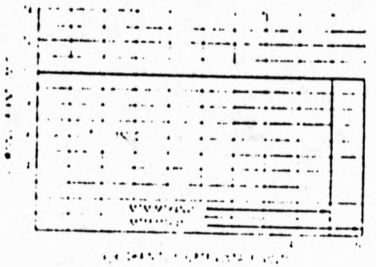


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain to source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25 C and a maximum junction temperature of 150 C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

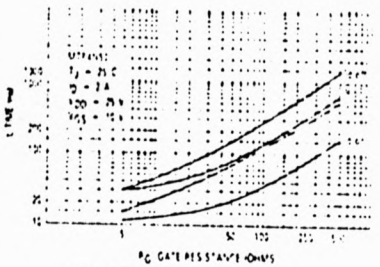


Figure 9. Resistive Switching Time Variation versus Gate Resistance

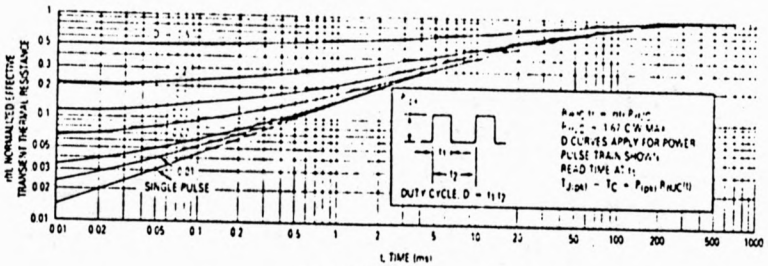


Figure 10. Thermal Response

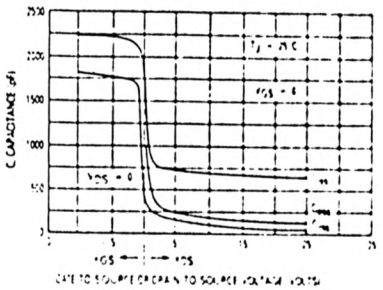


Figure 11 Capacitance Variation

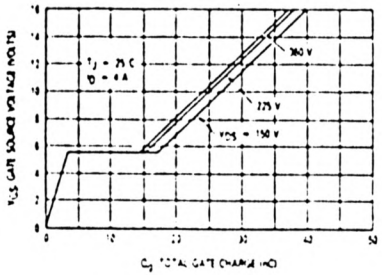


Figure 12 Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

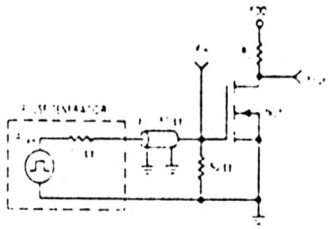


Figure 13. Switching Test Circuit

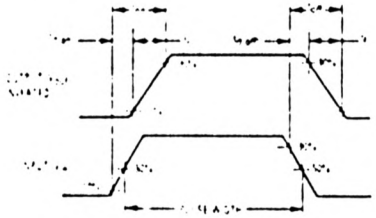
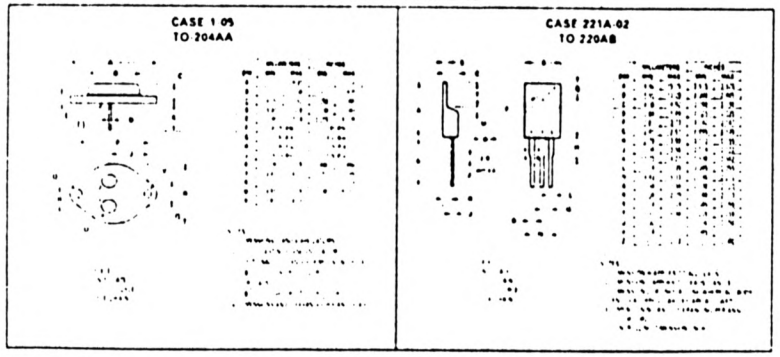


Figure 14 Switching Waveforms

OUTLINE DIMENSIONS



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN	PNP
TIP120	TIP125
TIP121	TIP126
TIP122	TIP127

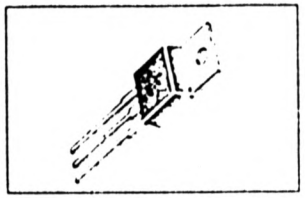
PLASTIC MEDIUM POWER COMPLEMENTARY SILICON TRANSISTORS

... designed for general purpose amplifier and low speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) – TIP120, TIP125
  = 80 Vdc (Min) – TIP121, TIP126
  = 100 Vdc (Min) – TIP122, TIP127
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON 5 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60, 80, 100 VOLTS
65 WATTS



*MAXIMUM RATINGS

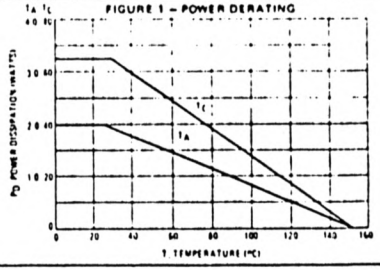
Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous / Peak	I_C	5.0 / 8.0			Adc
Base Current	I_B	120			mAdc
Total Power Dissipation @ T_C = 25°C / Derate above 25°C	P_D	65 / 0.52			Watts / W/°C
Total Power Dissipation @ T_A = 25°C / Derate above 25°C	P_D	2.0 / 0.016			Watts / W/°C
Unclamped Inductive Load Energy (1)	E	50			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

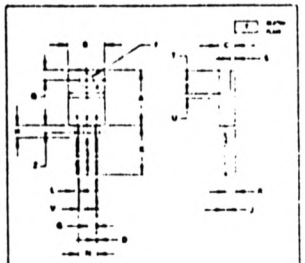
THERMAL CHARACTERISTICS

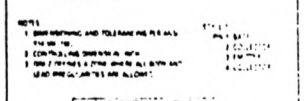
Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1 A, L = 100 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

FIGURE 1 – POWER DERATING







CASE 221A-04
TO-220AB

3-1100

FIGURE 4 – THERMAL RESPONSE

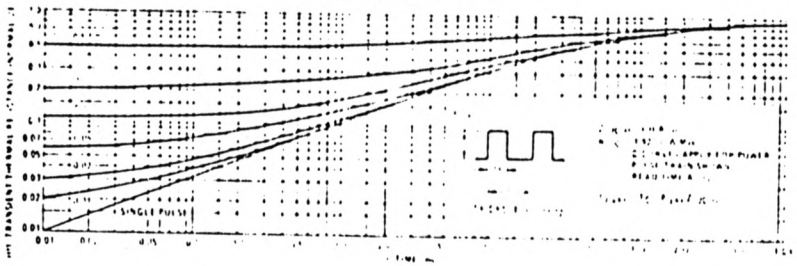


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

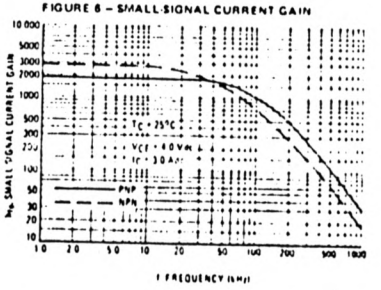
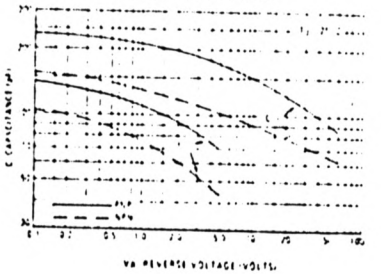


FIGURE 7 – CAPACITANCE



3-1102

NPN
TIP120, TIP121, TIP122

PNP
TIP125, TIP126, TIP127

FIGURE 8 – DC CURRENT GAIN

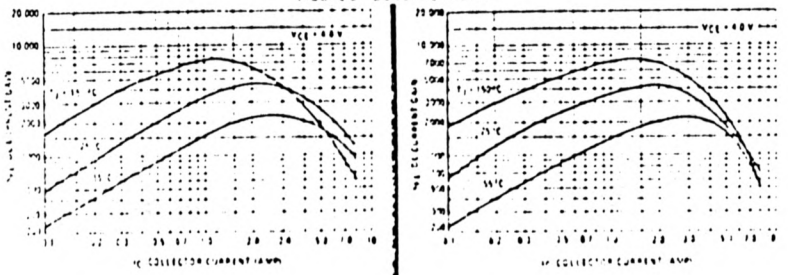


FIGURE 9 – COLLECTOR SATURATION REGION

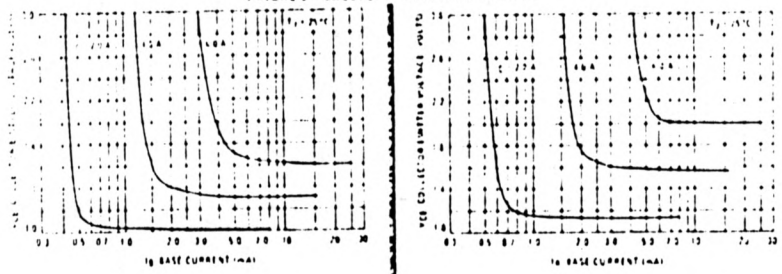
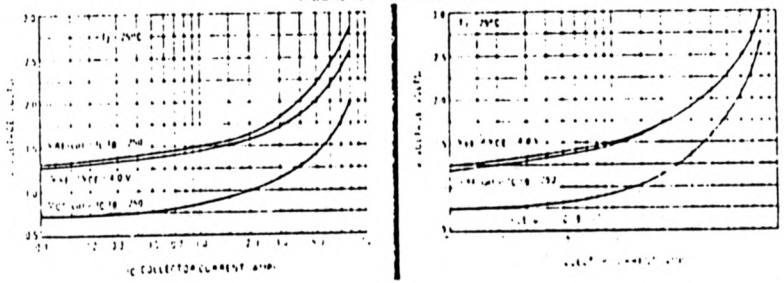


FIGURE 10 – "ON" VOLTAGES



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
MJE200
PNP
MJE210

COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

designed for low voltage, low-power, high-gain audio amplifier applications

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 5.0 Adc
  = 750 (Typ) @ I_C = 2.0 Adc
  = 70 (Min) @ I_C = 0.5 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mA
  = 0.75 Vdc (Max) @ I_C = 2.0 A
- High Current-Gain — Bandwidth Product
  f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage — I_{CBO} 100 nAdc @ Rated V_{CB}

5 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
25 VOLTS
15 WATTS

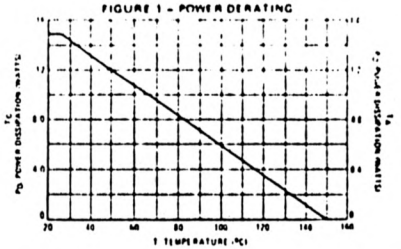
MAXIMUM RATINGS

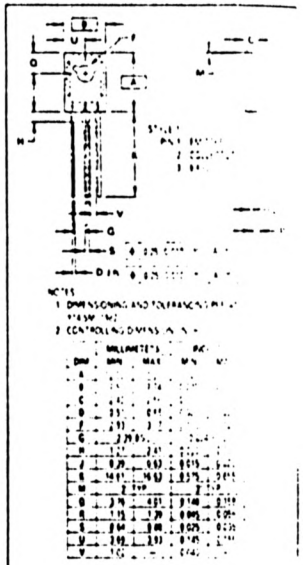
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CE}	25	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	8.34	°C/W
Thermal Resistance — Junction to Ambient	$R_{\theta JA}$	83.4	°C/W

FIGURE 1 – POWER DERATING





CASE 77-05
TO-225AA TYPE

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}		100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)	I_{EBO}		100	nAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	70 45 10	 180 	
Collector-Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$		0.3 0.75 1.9	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$		2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJE200 MJE210	C_{ob}		80 120	pF

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

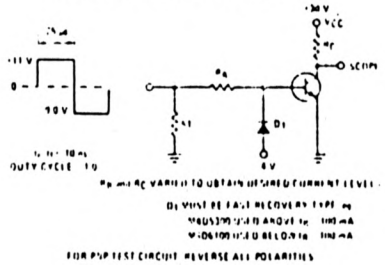


FIGURE 3 – TURN-ON TIME

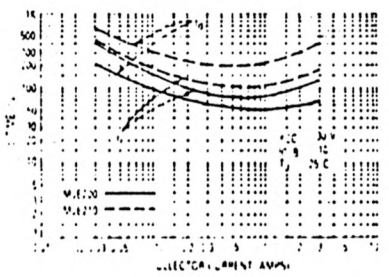


FIGURE 4 – THERMAL RESPONSE

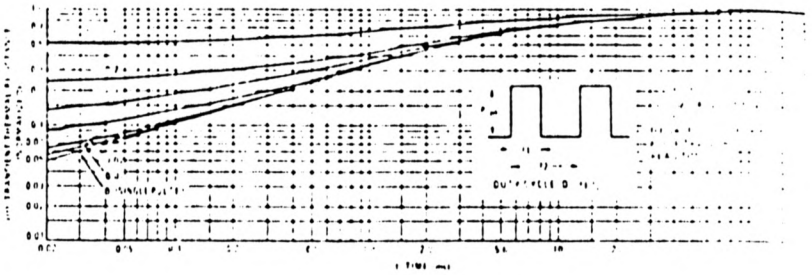
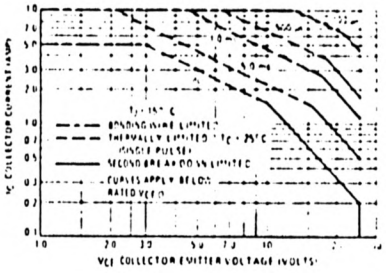


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C or T_A is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN OFF TIME

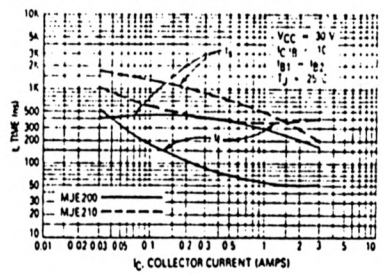
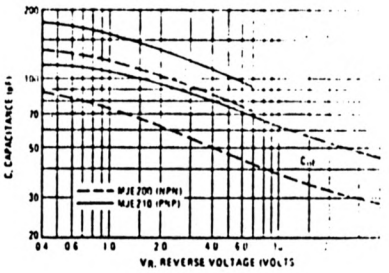


FIGURE 7 – CAPACITANCE



NPN
MJE200

PNP
MJE210

FIGURE 8 – DC CURRENT GAIN

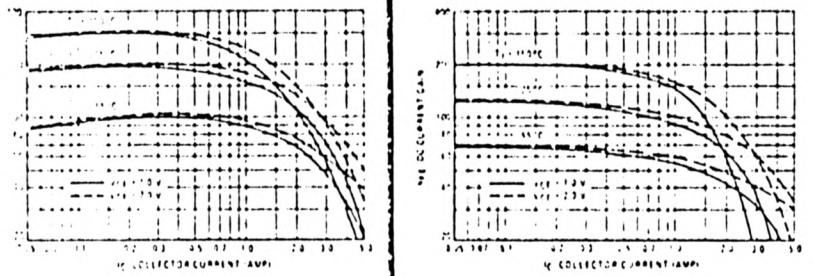


FIGURE 9 – ON VOLTAGE

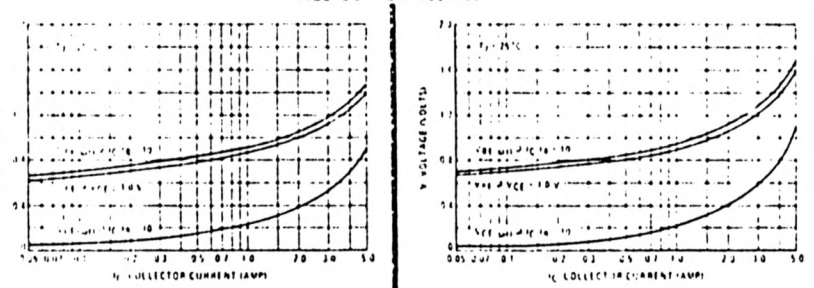
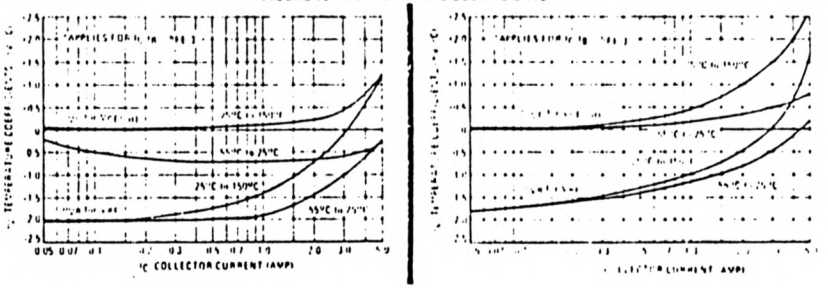


FIGURE 10 – TEMPERATURE COEFFICIENTS



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE16002
MJE16004
MJH16002
MJH16004

Designer's Data Sheet

SWITCHMODE III SERIES
NPN SILICON POWER TRANSISTORS

8.0 AMPERE

NPN SILICON POWER TRANSISTORS

450 VOLTS
80 and 100 WATTS

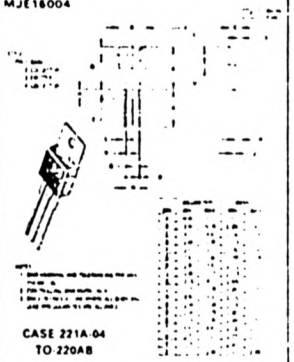
These transistors are designed for high voltage, high-speed switching of inductive circuits where fall time and RBSOA are critical. They are particularly well suited for line-operated switch mode applications.

The MJE16004 and MJH16004 are high gain versions of the MJE16002 and MJH16002 for applications where drive current is limited.

Typical Applications

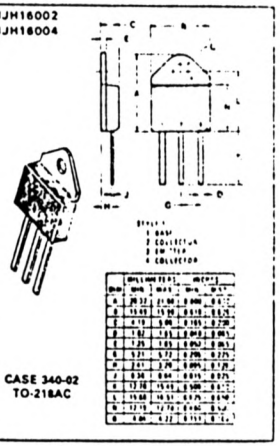
- Switching Regulators
- High Resolution Deflection Circuits
- Inverters
- Motor Drives
- Fast Switching Speeds
  - 50 ns Inductive Fall Time @ 75°C (Typ)
  - 70 ns Crossover Time @ 75°C (Typ)
- 100°C Performance Specified for
  - Reverse-Biased SOA
  - Inductive Switching Times
  - Saturation Voltages
  - Leakage Currents

MJE16002
MJE16004



CASE 221A-04
TO-220AB

MJH16002
MJH16004



CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MJE16002 / MJH16002 MJE16004 / MJH16004		Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450		Vdc
Collector-Emitter Voltage	V_{CEV}	850		Vdc
Emitter-Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	80 32 0.64	100 40 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	1.25	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	–	–	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 650 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	– –	– –	0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{s/b}$		See Figure 17 or 18		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 19		
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 0.2 Adc) MJE16002, MJH16002 (I_C = 1.5 Adc, I_B = 0.15 Adc) MJE16004, MJH16004 (I_C = 3.0 Adc, I_B = 0.4 Adc) MJE16002, MJH16002 (I_C = 3.0 Adc, I_B = 0.3 Adc) MJE16004, MJH16004 (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C) MJE16002 / MJH16002 (I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C) MJE16004 / MJH16004	$V_{CE(sat)}$	– – – – – –	– – – – – –	1.0 1.0 2.5 2.5 2.5 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.4 Adc) MJE16002 / MJH16002 (I_C = 1.0 Adc, I_B = 0.3 Adc) MJE16004 / MJH16004 (I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C) MJE16002 / MJH16002 (I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C) MJE16004 / MJH16004	$V_{BE(sat)}$	– – – –	– – – –	1.5 1.5 1.5 1.5	Vdc
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc) MJE16002 / MJH16002 MJE16004 / MJH16004	h_{FE}	5.0 7.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	–	–	200	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1) MJE16002 / MJH16002						
Delay Time	I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%	I_{B2} = 0.8 Adc, R_{B2} = 8.0 (1)	t_d	–	30	100 (1)	ns
Rise Time			t_r	–	100	300	
Storage Time			t_s	–	1000	1800	
Fall Time			t_f	–	60	300	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	–	400	–	
Fall Time			t_f	–	130	–	
Resistive Load (Table 1) MJE16004 / MJH16004						
Delay Time	I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.3 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%	I_{B2} = 0.6 Adc, R_{B2} = 8.0 (1)	t_d	–	30	100	ns
Rise Time			t_r	–	130	300	
Storage Time			t_s	–	800	2700	
Fall Time			t_f	–	80	350	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	–	250	–	
Fall Time			t_f	–	60	–	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%

*$A_I = \frac{I_C}{I_{B1}}$

SWITCHING CHARACTERISTICS (continued)

Characteristics			Symbol	Min	Typ	Max	Unit
Inductive Load (Table 2)	**MJE16002 / MJH16002**						
Storage Time	I_C = 3.0 Adc I_{B1} = 0.4 Adc $V_{BE(off)}$ = 5.0 Vdc $V_{CE(pk)}$ = 400 Vdc	(T_J = 100°C)	t_{sv}	–	500	1600	
Fall Time			t_{fi}	–	101	200	
Crossover Time			t_c	–	120	250	
Storage Time		(T_J = 150°C)	t_{sv}	–	600	–	
Fall Time			t_{fi}	–	120	–	
Crossover Time			t_c	–	160	–	
Inductive Load (Table 2)	**MJE16004 / MJH16004**						
Storage Time	I_C = 3.0 Adc I_{B1} = 0.3 Adc $V_{BE(off)}$ = 5.0 Vdc $V_{CE(pk)}$ = 400 Vdc	(T_J = 100°C)	t_{sv}	–	400	1300	
Fall Time			t_{fi}	–	80	150	
Crossover Time			t_c	–	90	200	
Storage Time		(T_J = 150°C)	t_{sv}	–	450	–	
Fall Time			t_{fi}	–	100	–	
Crossover Time			t_c	–	110	–	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$$\beta_f = \frac{I_C}{I_{B1}}$$

FIGURE 1 – DC CURRENT GAIN

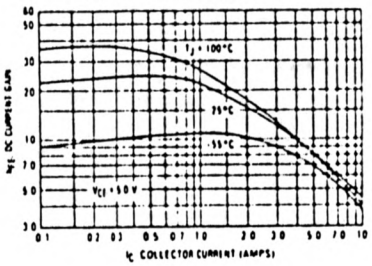


FIGURE 2 – COLLECTOR SATURATION REGION

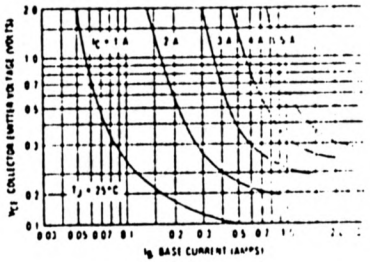


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

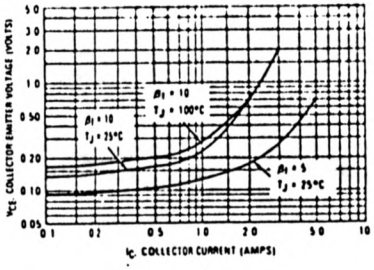
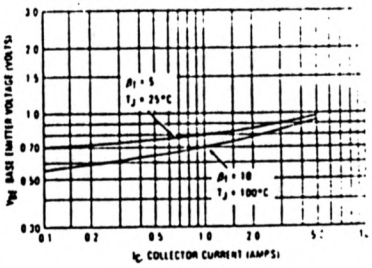


FIGURE 4 – BASE-EMITTER VOLTAGE



TYPICAL STATIC CHARACTERISTICS (continued)

FIGURE 5 – COLLECTOR CUTOFF REGION

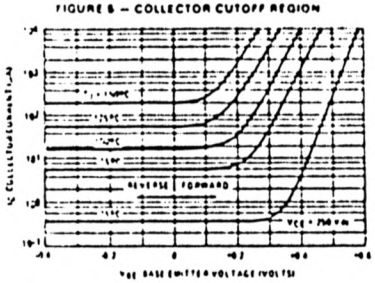
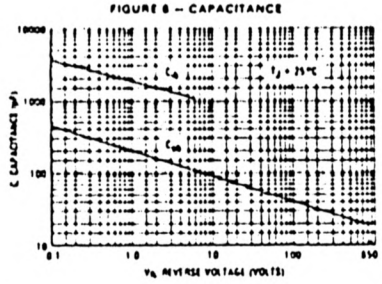


FIGURE 6 – CAPACITANCE



TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 7 – STORAGE TIME

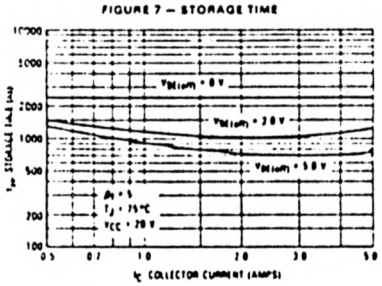


FIGURE 8 – STORAGE TIME

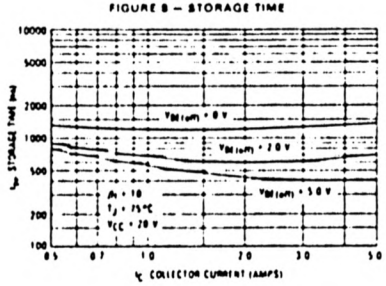


FIGURE 9 – COLLECTOR CURRENT FALL TIME

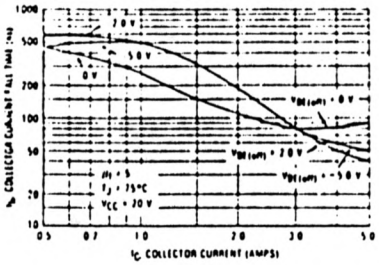
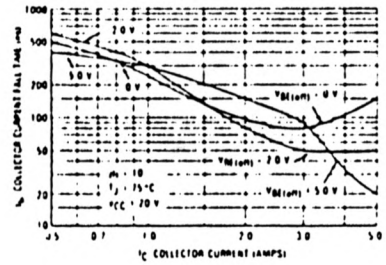


FIGURE 10 – COLLECTOR CURRENT FALL TIME



TYPICAL DYNAMIC CHARACTERISTICS (continued)

FIGURE 11 — CROSSOVER TIME

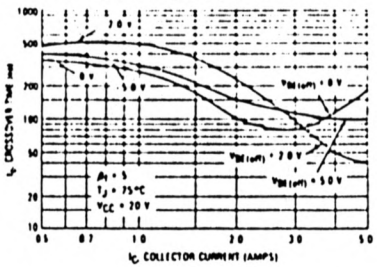
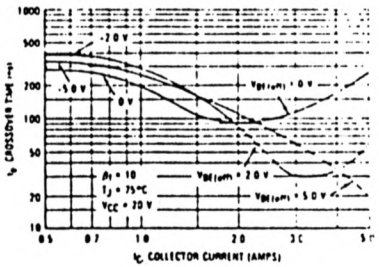


FIGURE 12 — CROSSOVER TIME



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 13 — INDUCTIVE SWITCHING MEASUREMENTS

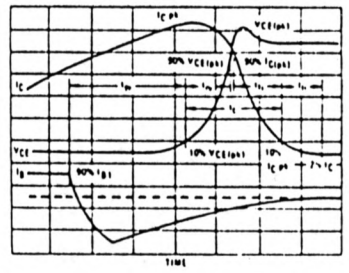


FIGURE 14 — PEAK REVERSE BASE CURRENT

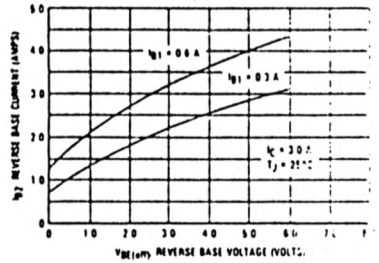
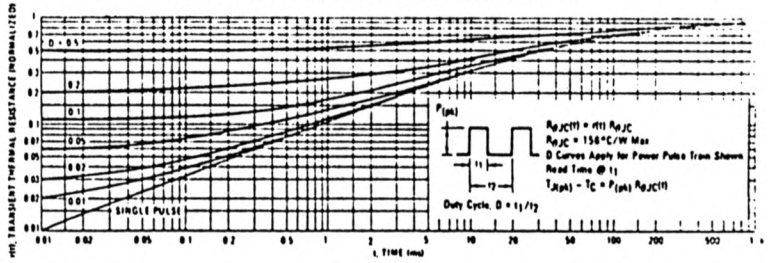
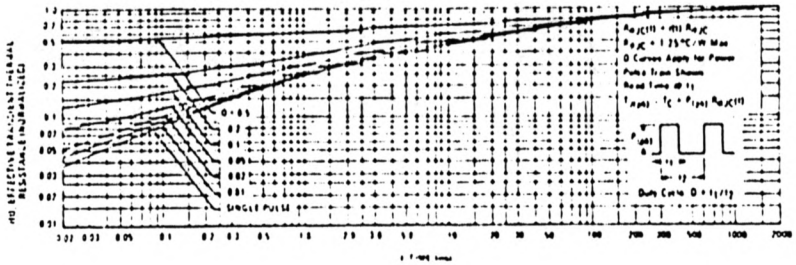


FIGURE 15 — THERMAL RESPONSE (MJE16002 and MJE16004)



TYPICAL ELECTRICAL CHARACTERISTICS (continued)

FIGURE 16 — THERMAL RESPONSE (MJH16002 and MJH16004)



SAFE OPERATING AREA INFORMATION

FIGURE 17 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (MJE16002 and MJE16004)

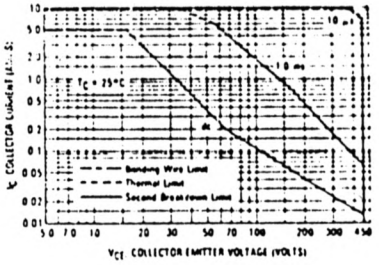


FIGURE 18 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (MJH16002 and MJH16004)

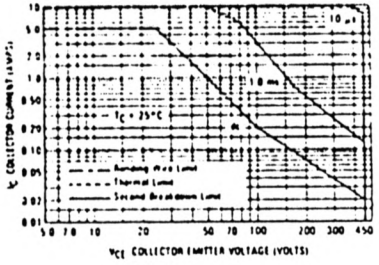


FIGURE 19 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA

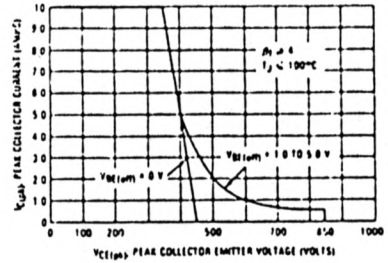
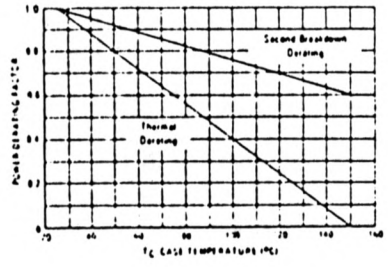


FIGURE 20 — POWER DERATING



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 17 and 18 are based on $T_C = 25°C$. $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 17 and 18 may be found at any case temperature by using the appropriate curve on Figure 20.

$T_{J(pk)}$ may be calculated from the data in Figures 15 or 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 19 gives the RBSOA characteristics.

TABLE 1 – RESISTIVE LOAD SWITCHING

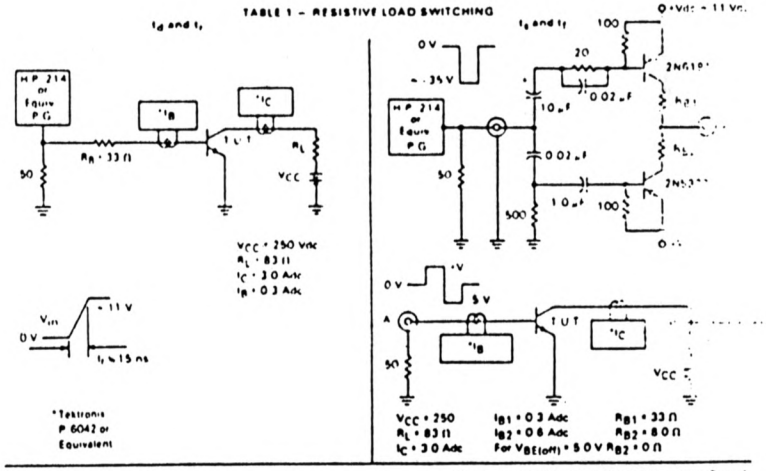
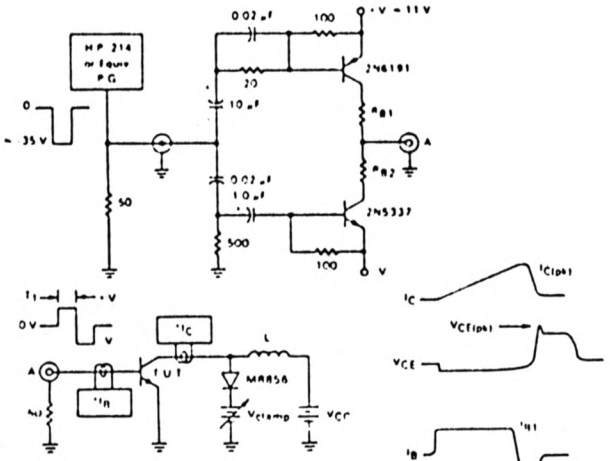
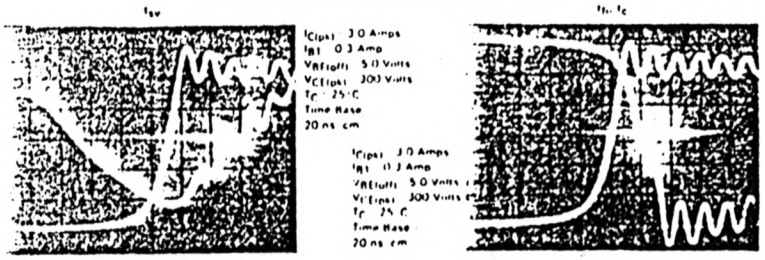


TABLE 2 – INDUCTIVE LOAD SWITCHING



TYPICAL INDUCTIVE SWITCHING WAVEFORMS



LINEAR INTEGRATED CIRCUITS

Off-Line Current Mode PWM Controller

UC184x
UC284x
UC384x

FEATURES

- Optimized for off-line control
- Low start up current (< 1mA)
- Automatic feed forward compensation
- Pulse by pulse current limiting
- Enhanced load response characteristics
- Under voltage lockout with hysteresis
- Double pulse suppression
- High current totem pole output
- Internally trimmed bandgap reference
- 500kHz operation

DESCRIPTION

The UC1842 family of control ICs provides on an eight pin mini dip the necessary features to implement off line, fixed frequency current mode control schemes with a minimal external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse by pulse current limiting.

Protection circuitry includes built in under-voltage lockout and current limiting. Other features include fully latched operation, a 1% trimmed bandgap reference, and start up current less than 1mA.

These devices feature a totem pole output designed to source and sink high peak current from a capacitive load, such as the gate of a power MOSFET. Consistent with N-Channel power devices, the output is low in the OFF state.

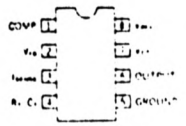
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (I_{CC} < 30mA) ..... Self Limiting
Supply Voltage (Low Impedence Source) 30V
Output Current ..... ±1A
Output Energy (Capacitive Load) 5μJ
Analog Inputs (Pin 2, Pin 3) ..... -0.3V to V_{CC}
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 70°C$ 1W
Derate 12.5mW/°C for $T_A > 70°C$
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

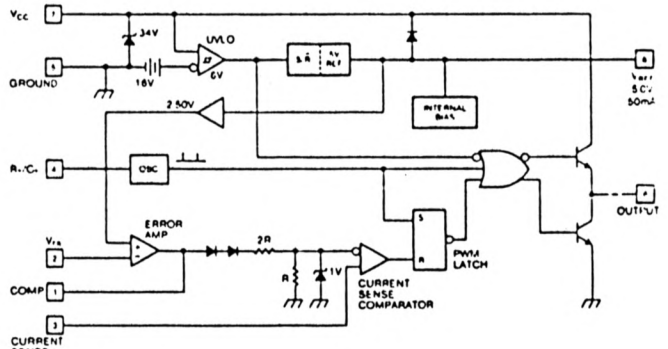
Note 1: All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.

CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE

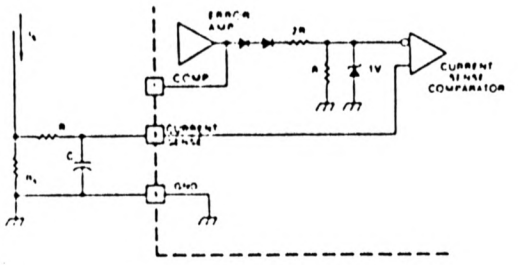


BLOCK DIAGRAM



UNITRODE

CURRENT SENSE CIRCUIT

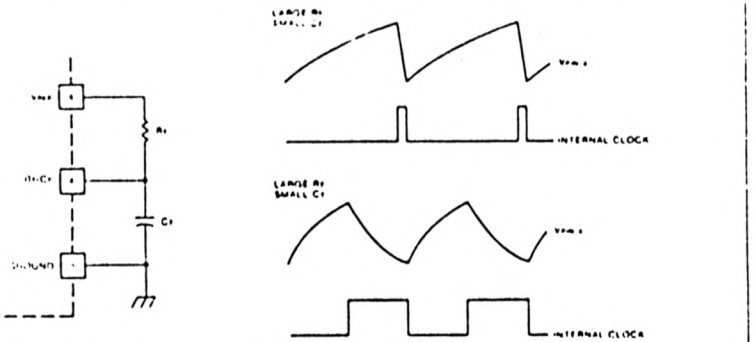


PEAK CURRENT I_S IS DETERMINED BY THE FORMULA

$$I_{S\,MAX} \approx \frac{1.0V}{R_S}$$

A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS.

OSCILLATOR WAVEFORMS AND MAXIMUM DUTY CYCLE



For the timing capacitor, C_T is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of R_T and C_T therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulas:

$$t_C = 0.55\,R_TC_T$$

$$t_d = R_TC_T\,\ln\left(\frac{6.3\,R_T - 2.7}{6.3\,R_T - 4}\right) \quad (R_T \text{ in } k\Omega)$$

Frequency, then, is $f = (t_C + t_d)^{-1}$

For $R_T > 5k$, $f \approx \dfrac{1.8}{R_TC_T}$

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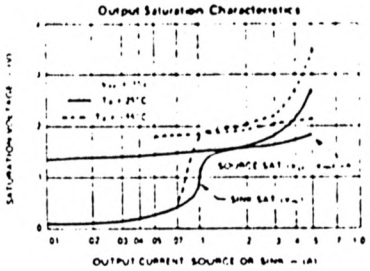
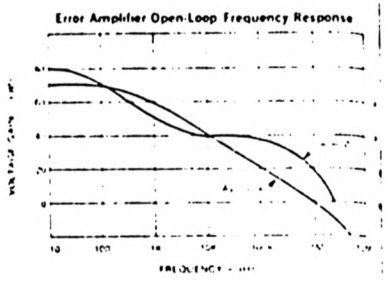
TWX (710) 326-6509 • TELEX 95-1064

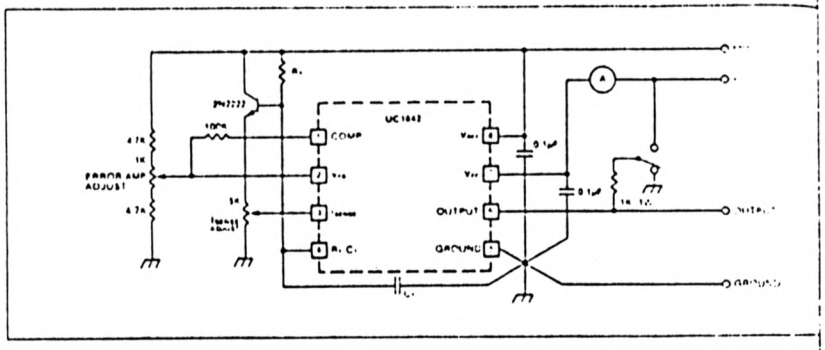
Output Saturation Characteristics



Error Amplifier Open-Loop Frequency Response



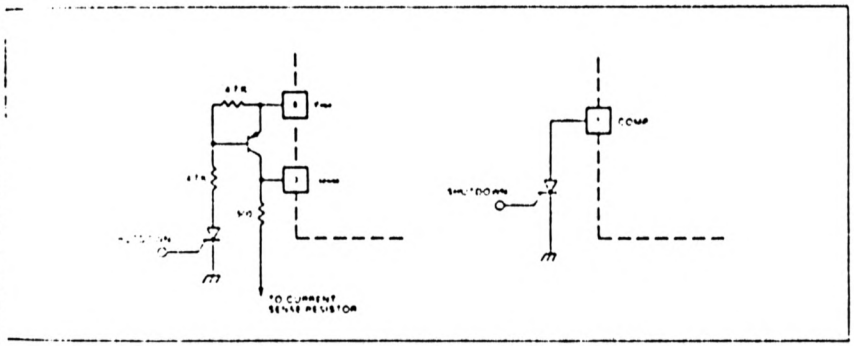
OPEN-LOOP LABORATORY TEST FIXTURE



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

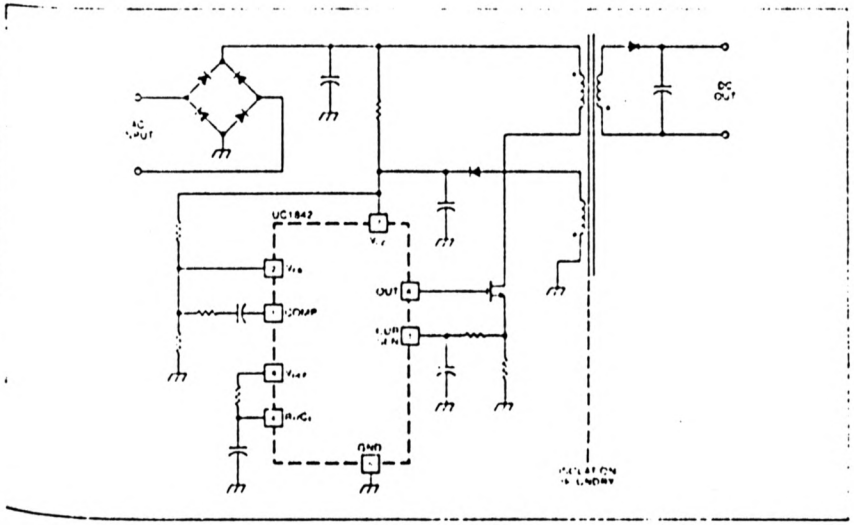
The transistor and 5K potentiometer are used to s[ ] oscillator waveform and apply an adjustable ramp to pin 3.

SHUTDOWN TECHNIQUES



[ ]ation of the UC1842 can be accomplished by two methods [ ]ither raising pin 3 above 1V or pull pin 1 below a voltage two diode [ ] Either method causes the output of the PWM [ ] to zero (refer to block diagram). The PWM latch is [ ] so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In the examples shown, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{in} below the lower UVLO threshold (10V). At this point all internal bias is removed allowing the SCR to reset.

OFF LINE FLYBACK REGULATOR



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJE520

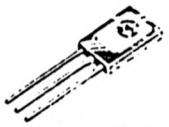
PLASTIC MEDIUM POWER NPN
SILICON TRANSISTOR

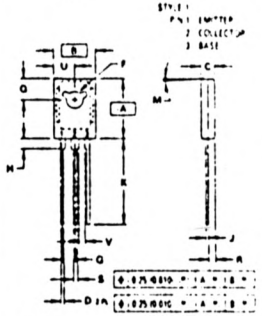
... designed for use in general purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain – h_{FE} = 25 (Min) @ I_C = 1.0 Adc
- Complementary to PNP MJE370

3 AMPERE
POWER TRANSISTOR
NPN SILICON

30 VOLTS
25 WATTS





NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.16	11.04	0.400	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.17	0.115	0.125
G	2.29 BSC		0.090 BSC	
H	1.27	2.41	0.050	0.095
J	0.29	0.52	0.015	0.020
K	14.61	16.62	0.575	0.655
M	5° TYP		5° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.94	0.98	0.037	0.039
U	3.93	3.93	0.155	0.155
V	1.02	–	0.040	–

CASE 77-06
TO-225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	30	Vdc
Collector Base Voltage	V_{CB}	30	Vdc
Emitter Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous – Peak	I_C	3.0 7.0	Adc
Base Current – Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 .02	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

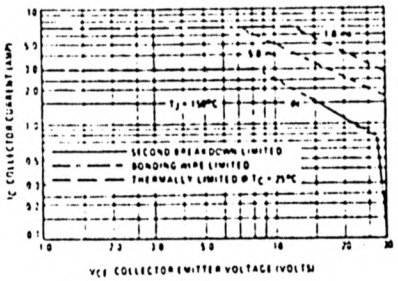
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	25	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 ACTIVE REGION SAFE OPERATING AREA



The data of Figure 1 based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

FIGURE 2 – DC CURRENT GAIN

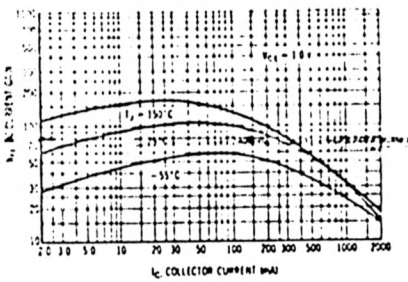


FIGURE 3 – "ON" VOLTAGE

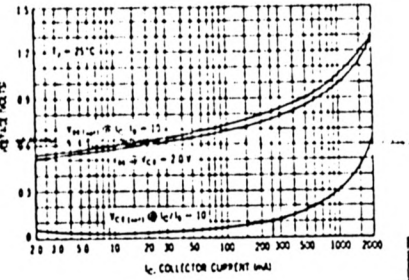
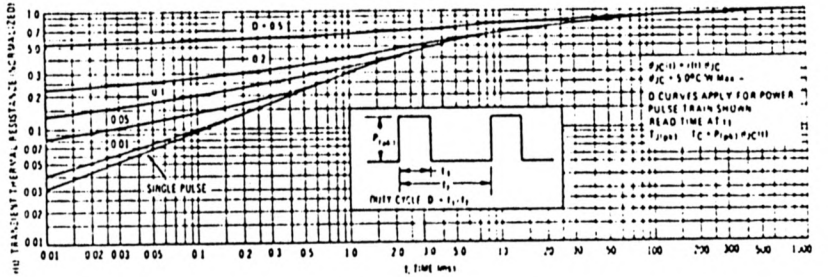


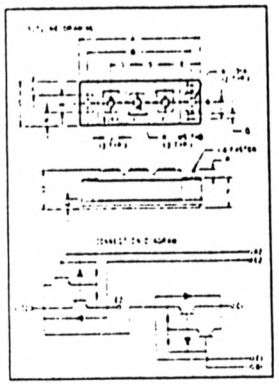
FIGURE 4 – THERMAL RESPONSE



Powerex, Inc., Hillis Street, Youngwood, Pennsylvania 15697 (412) 925-7272

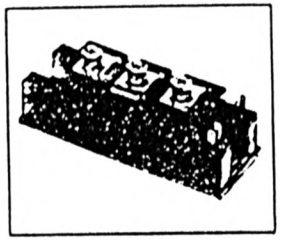
Dual Darlington Transistor Module

75 Amperes/600 Volts



600 Volt KD224575
Outline Drawing

Dimension	Inches	Millimeters
A	3.701 Max	94 Max
B	3.150 ± .010	80 ± 0.25
C	1.339 Max	34 Max
D	1.181 Max	30 Max
E	1.063	27
F	.906	23
G	.787	20
H	.512	13
J	.472	12
K	.413	10.5
L	.344	8.75
M	.315	8
N	.256 Dia	6.5 Dia
P	.256 Min	6.5 Min
Q	.157	4
R	M5 Metric	M5



KD224575
Dual Darlington
Transistor Module
75 Amperes/600 Volts

Description
Powerex Dual Darlington Transistor Modules are medium power devices which are designed for use in switching applications. The modules are isolated consisting of two Darlington Transistors with each transistor having a reverse parallel connected high speed diode.

Features:
- ☐ Isolated Mounting
- ☐ Planar Chips
- ☐ Discrete Fast Recovery Feed Back Diode
- ☐ High Gain (h_{FE})
- ☐ 110 Fast On Base Emitter Signal Connections
- ☐ Base Emitter Speed Up Diode

Applications:
- ☐ Inverters
- ☐ DC Motor Control
- ☐ Switching Power Supplies
- ☐ AC Motor Control

Ordering Information
Example: Select the complete eight digit module part number you desire from the table - i.e. KD224575 is a 450 $V_{CEO(sus)}$ (600 V_{CEV}), 75 Ampere Dual Darlington Module.

Type	$V_{CEO(sus)}$ Volts (x 10)	Current Rating Amperes (75)
KD22	45	75

POWEREX

Powerex, Inc., Hillis Street, Youngwood, Pennsylvania 15697 (412) 925-7272

KD224575
Dual Darlington Transistor Module
75 Amperes/600 Volts

Maximum Ratings T_j = 25°C unless otherwise specified

	Symbol	KD224575	Units
Junction Temperature	T_j	-40 to 150	°C
Storage Temperature	T_{stg}	-40 to 125	°C
Collector-Emitter Sustaining Voltage	$V_{CEO(sus)}$	450	Volts
Collector-Emitter Sustaining Voltage for t_{ps} = 2V	$V_{CEV(sus)}$	600	Volts
Collector-Base Voltage	V_{CBO}	600	Volts
Emitter-Base Voltage	V_{EB}	7	Volts
Collector-Emitter Voltage t_{ps} = 2V	V_{CEV}	600	Volts
Continuous Collector Current	I_C	75	Amperes
Diode Forward Current	I_{DF}	75	Amperes
Continuous Base Current	I_B	4.5	Amperes
Diode Surge Current	I_{DFM}	750	Amperes
Power Dissipation, Each Transistor	P_C	350	Watts
Max. Mounting Torque, M5 Terminal Screw	—	17	in-lb
Max. Mounting Torque, M6 Mounting Screw	—	26	in-lb
Module Weight	—	7	Oz.
Module Weight	—	210	Grams
Isolation	V_{ISOL}	2500	Volts

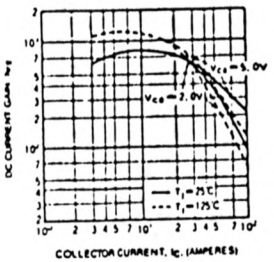
Electrical and Mechanical Characteristics T_j = 25°C unless otherwise specified

Characteristics		Symbol	Test Conditions	KD224575 Min	Typ	Max	Units
Collector Cutoff Current		I_{CEV}	V_{CE} = 600V, V_{BE} = -2V	—	—	1	mA
Collector Cutoff Current		I_{CEV}	V_{CE} = 600V, V_{BE} = -2V, T_j = 125°C	—	—	10	mA
DC Current Gain		h_{FE}	I_C = 75A, V_{CE} = 2V	75	—	—	—
DC Current Gain		h_{FE}	I_C = 75A, V_{CE} = 5V	100	—	—	—
Diode Forward Voltage		V_{FM}	I_{FM} = 75A	—	—	1.85	V
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	I_C = 75A, I_B = 1A	—	—	2.0	V
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	I_C = 75A, I_B = 1A	—	—	2.5	V
Resistive Load Switch Times	Turn On	t_{on}	V_{CC} = 300V, I_C = 75A, I_{B1} = 1.5A, I_{B2} = -1.5A	—	—	2.5	µs
	Storage Time	t_s		—	—	12	µs
	Fall Time	t_f		—	—	3.0	µs
Thermal Resistance, Case to Sink Lubricated		R_{thCS}	Per Half Module	—	—	0.15	°C/W
Thermal Resistance, Junction to Case		R_{thJC}	Transistor Parts	—	—	0.35	°C/W
Thermal Resistance, Junction to Case		R_{thJC}	Diode Part	—	—	1.3	°C/W

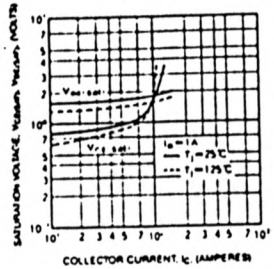
Powerex, Inc., Hillis Street, Youngwood, Pennsylvania 15697 (412) 925-7272

KD224575
Dual Darlington Transistor Module
75 Amperes/600 Volts

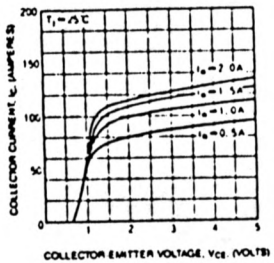
DC CURRENT GAIN (TYPICAL)



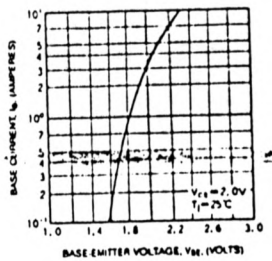
SATURATION VOLTAGE (TYPICAL)



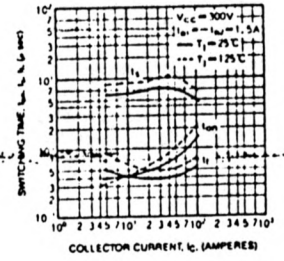
COMMON EMITTER OUTPUT CHARACTERISTICS (TYPICAL)



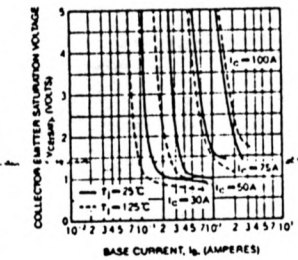
COMMON EMITTER INPUT CHARACTERISTICS (TYPICAL)



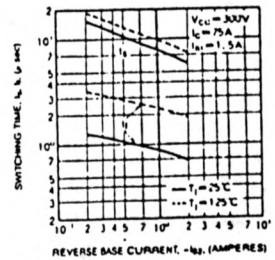
SWITCHING CHARACTERISTICS (TYPICAL)



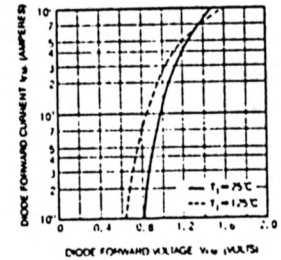
COLLECTOR-EMITTER SATURATION VOLTAGE (TYPICAL)



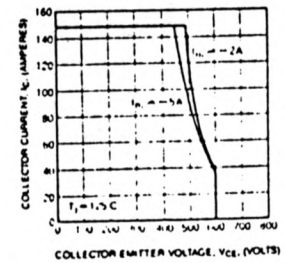
SWITCHING TIME VS. BASE CURRENT (TYPICAL)



DIODE CHARACTERISTICS (TYPICAL)



REVERSE BIAS SAFE OPERATING AREA (R.B.S.O.A.)

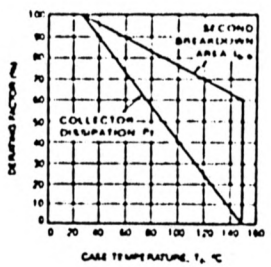


Powerex, Inc., Hillis Street, Youngwood, Pennsylvania 15697 (412) 925-7272

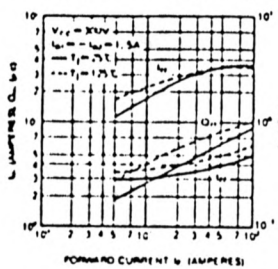
KD224575
Dual Darlington Transistor Module
75 Amperes/600 Volts

FORWARD BIAS SAFE OPERATING AREA (S.O.A.)

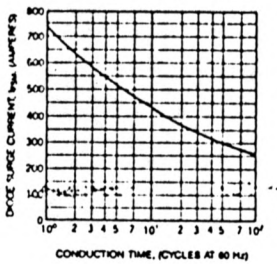
DERATING FACTOR OF SAFE OPERATING AREA (S.O.A.)



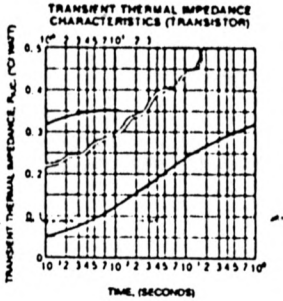
REVERSE RECOVERY CHARACTERISTICS OF FREE-WHEEL DIODE (TYPICAL)



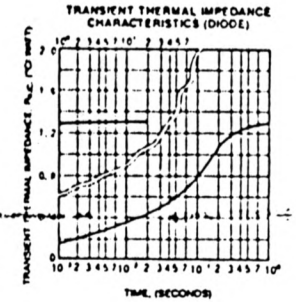
DIODE FORWARD SURGE CURRENT



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (TRANSISTOR)



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (DIODE)



National Semiconductor

CD4518BM/CD4518BC, CD4520BM/CD4520BC
Dual Synchronous Up Counters

General Description

The CD4518BM/CD4518BC dual BCD counter and the CD4520BM/CD4520BC dual binary counter are implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors.

Each counter consists of two identical, independent, synchronous, 4-stage counters. The counter stages are toggle flip-flops which increment on either the positive-edge of CLOCK or negative-edge of ENABLE, simplifying cascading of multiple stages. Each counter can be asynchronously cleared by a high level on the RESET line. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 6MHz counting rate (typ.) at V_{DD} = 10V

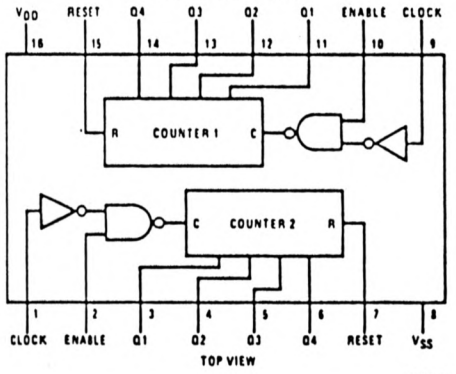
Truth Table

CLOCK	ENABLE	RESET	ACTION
⌐	1	0	Increment counter
0	⌐	0	Increment counter
⌐	X	0	No change
X	⌐	0	No change
⌐	0	0	No change
1	⌐	0	No change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

Connection Diagram

Dual-In-Line and Flat Package



Order Number CD4518BMJ, CD4518BCJ, CD4520BMJ or CD4520BCJ
See NS Package J16A

Order Number CD4518BMN, CD4518BCN, CD4520BMN or CD4520BCN
See NS Package N16E

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4518BM, CD4520BM	−55°C to +125°C
CD4518BC, CD4520BC	−40°C to +85°C

DC Electrical Characteristics CD4518BM/CD4520BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C MIN	−55°C MAX	25°C MIN	25°C TYP	25°C MAX	125°C MIN	125°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.01	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	|I_O| < 1 μA, V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	|I_O| < 1 μA, V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	|I_O| < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	|I_O| < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		10^{-5}	0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4518BC/CD4520BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C MIN	−40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	|I_O| < 1 μA, V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	|I_O| < 1 μA, V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd) CD4518BC/CD4520BC (Note 2)

SYM	PARAMETER	CONDITIONS	-40°C MIN	-40°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS
V_{IL}	Low Level Input Voltage	I_O = 1 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	I_O = 1 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IN} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IN} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 9.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 13.5V	3.6		3.0	8.8		2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		-0.3		-10^{-5}	-0.3		-1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, $t_r = t_f$ = 20 ns, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock → Q	V_{DD} = 5V		325	650	ns
		V_{DD} = 10V		110	225	ns
		V_{DD} = 15V		85	170	ns
t_{PHL}	Propagation Delay Time Reset → Q	V_{DD} = 5V		220	560	ns
		V_{DD} = 10V		90	230	ns
		V_{DD} = 15V		65	160	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5V	1.5	3		MHz
		V_{DD} = 10V	3.0	6		MHz
		V_{DD} = 15V	4.0	8		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		35	70	ns
t_{RCL}, t_{FC}	Maximum Clock or Enable Rise and Fall Time	V_{DD} = 5V	15			µs
		V_{DD} = 10V	10			µs
		V_{DD} = 15V	5			µs
t_{WH}, t_{WL}	Minimum Enable Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		55	110	ns
		V_{DD} = 15V		40	80	ns
t_{WH}	Minimum Reset Pulse Width	V_{DD} = 5V		180	375	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	130	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Either Counter, (Note 4)		50		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

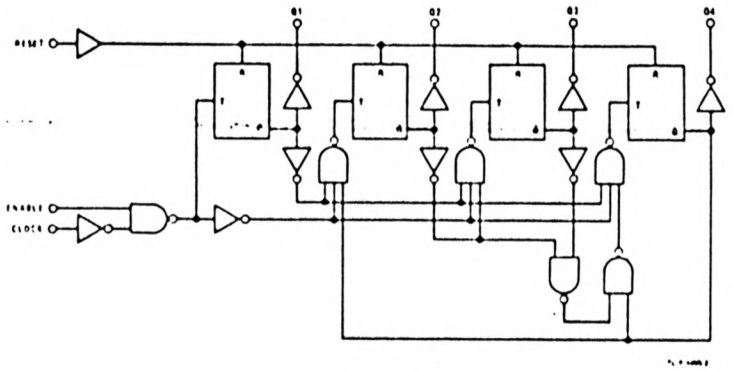
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

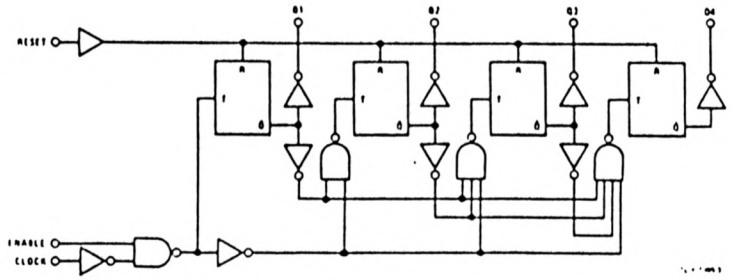
Note 4: C_{PD} determines the no load ac power consumption of a CMOS device. For a complete explanation, see "54C/74C Family Characteristics," application note AN-90.

Logic Diagrams

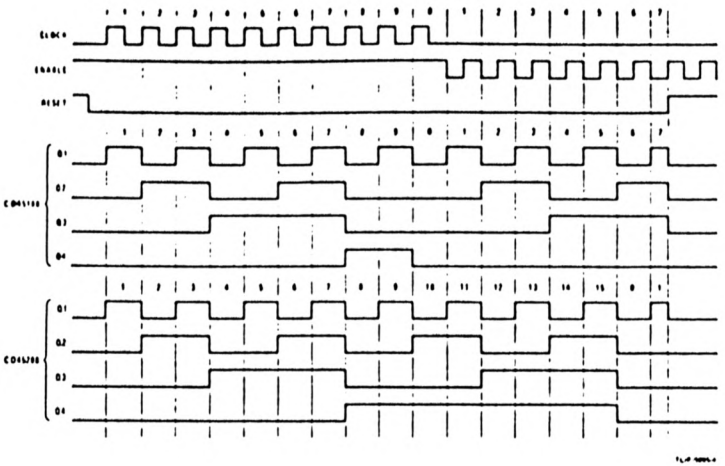
Decade Counter (CD4518BI) 1/2 Device Shown



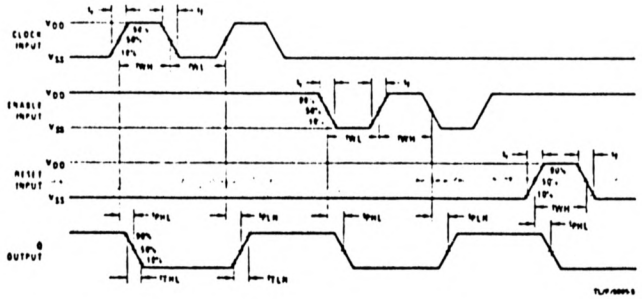
Binary Counter (CD4520BI) 1/2 Device Shown



Timing Diagrams



Switching Time Waveforms



HARRIS HI-508A/509A

Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection.....70 Vpp
- No Channel Interaction During Overvoltage
- ESD Resistant.....>4,000 Volts
- 44 V Maximum Power Supply
- Fail Safe with Power Loss (No Latchup)
- Break-Before-Make Switching
- Analog Signal range.....±15 V
- Access Time (Typical).....500 ns
- Standby Power (Typical).....7.5 mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

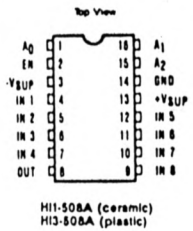
Description

The HI-508A and 509A are analog multiplexers with Active Overvoltage Protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The 508A is an 8 channel device and the 509A is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508 and HI-509 multiplexers are recommended. For further information see Application Notes 520 and 521.

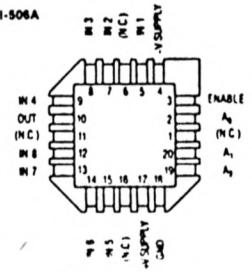
Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC package.

The HI-508A/509A are offered in both commercial and military grades. Addition HI-Rel screening including 160 hour burn-in is specified by the "-8" suffix.

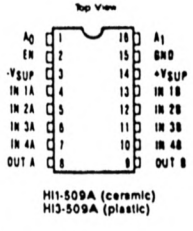
Pinouts



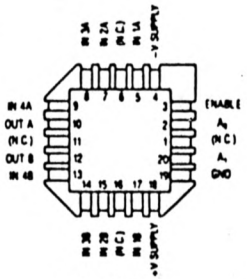
HI1-508A (ceramic)
HI3-508A (plastic)



HI4-508A (LCC)

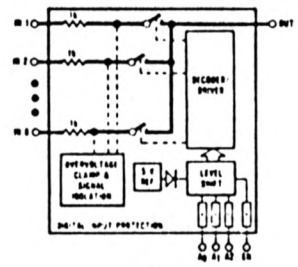


HI1-509A (ceramic)
HI3-509A (plastic)

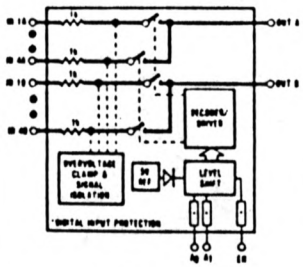


HI4-509A (LCC)

Functional Diagrams



HI-508A



HI-509A

4 MULTIPLEXERS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between Supply Pins 44 V
V+ to Ground 22 V
V- to Ground 25 V
Digital Input Overvoltage:
V_{EN}, V_A { $V_{Supply(+)}$ +4 V; $V_{Supply(-)}$ -4 V }
or 20 mA, whichever occurs first.
Analog Input Overvoltage:
V_S { $V_{Supply(+)}$ +20 V; $V_{Supply(-)}$ -20 V }

Continuous Current, S or D: 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max): 40 mA
Power Dissipation* (CERDIP) 1.28 W
Operating Temperature Range:
HI-508A/509A-2,-8 -55°C to +125°C
HI-508A/509A-5 0°C to +75°C
Storage Temperature Range -65°C to +150°C

*Derate 12.8 mW/°C above T_A=75°C

ELECTRICAL CHARACTERISTICS

Supplies = +15 V, -15 V; V_{AH} (Logic Level High) = +4.0 V, V_{AL}(Logic Level Low) = +0.8 V (unless otherwise specified).
For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508A/HI-509A -2, -8 MIN.	TYP.	MAX.	HI-508A/509A -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON} On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				µA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
I_{DIFF} Differential Off Output Leakage Current (HI-509A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold (Note 8)	Full			0.8			0.8	V
*V_{AH}, Input High Threshold	Full	4.0			4.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		µs
	Full			1.0			1.0	µs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		µs
(0.01%)	+25°C		3.5			3.5		µs
"OFF Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I_+, Current (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I_-, Current (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at +55°C.

NOTES: 1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100µA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33 V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
6. V_{EN} = 0.8 V, R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 100 kHz. Worst Case detection occurs on channel 4 due to proximity of the output pins.
7. V_{EN}, V_A = 0 V or 4.0 V.
8. To drive from DTL/TTL Circuits, 1kΩ pull up resistors to +5.0 V supply are recommended.

TRUTH TABLES

HI-508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

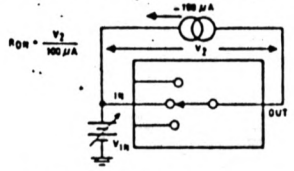
A_1	A_0	EN	ON CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Performance Characteristics and Test Circuits

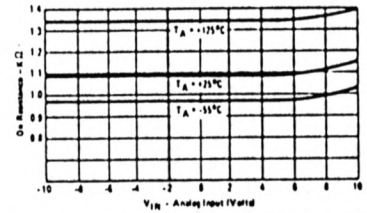
Unless Otherwise Specified T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

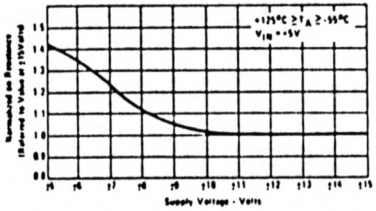
TEST CIRCUIT NO. 1



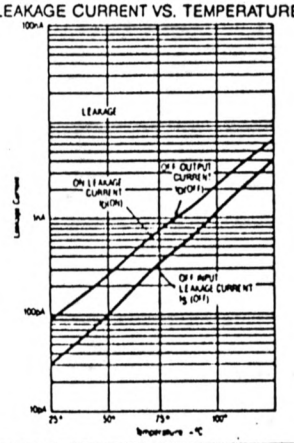
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



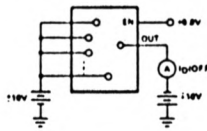
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



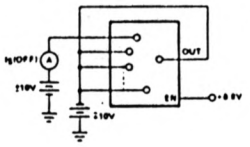
LEAKAGE CURRENT VS. TEMPERATURE



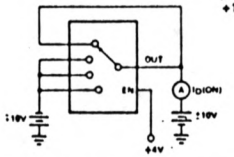
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

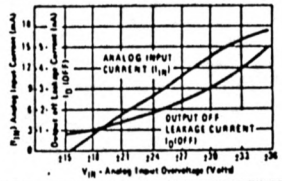


TEST CIRCUIT NO. 4*



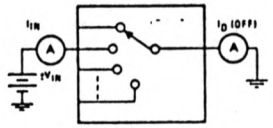
*Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



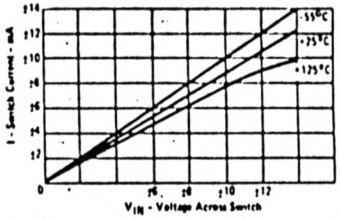
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



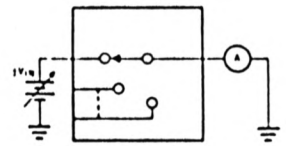
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

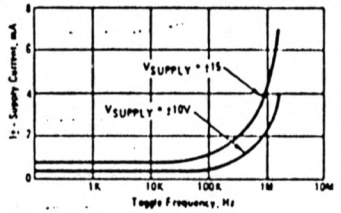


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

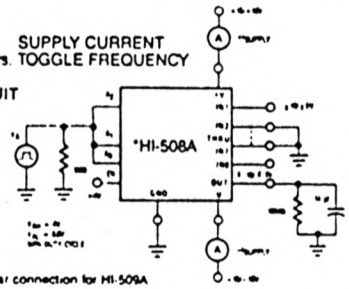


SUPPLY CURRENT vs. TOGGLE FREQUENCY



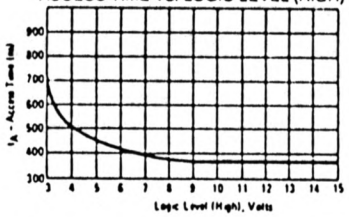
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



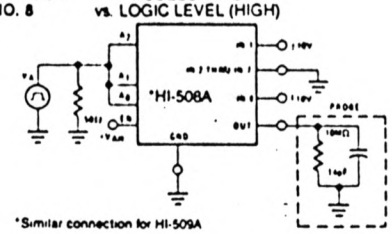
*Similar connection for HI-509A

ACCESS TIME VS. LOGIC LEVEL (HIGH)



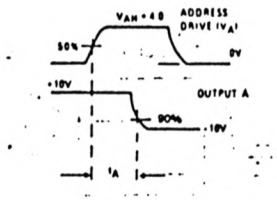
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL (HIGH)

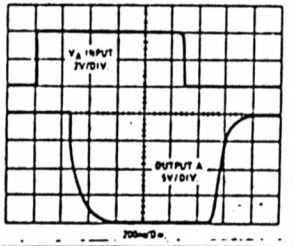


*Similar connection for HI-509A

Switching Waveforms



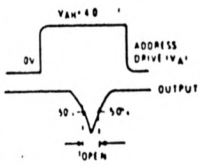
ACCESS TIME

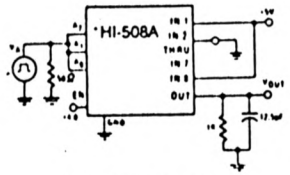


Switching Waveforms (continued)

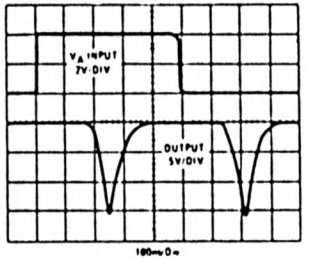
TEST CIRCUIT NO. 9

BREAK-BEFORE-MAKE DELAY (tOPEN)



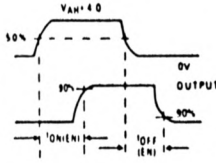


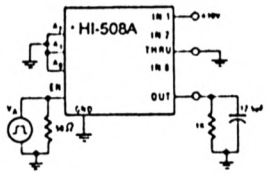
*Similar connection for HI-509A



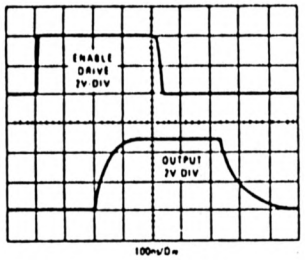
TEST CIRCUIT NO. 10

ENABLE DELAY (tON(EN), tOFF(EN))

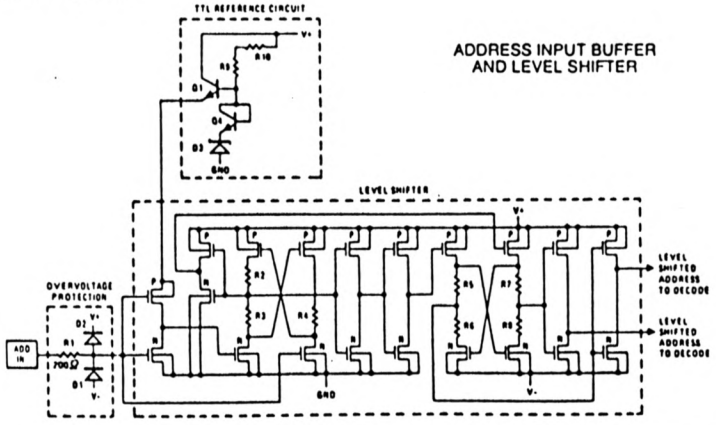




*Similar connection for HI-509A

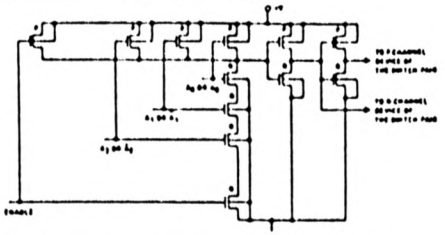


Schematic Diagrams

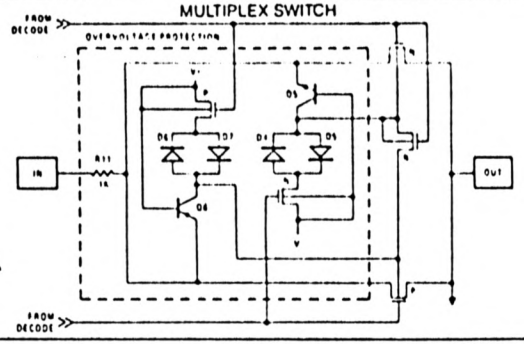


Schematic Diagrams (continued)

ADDRESS DECODER



MULTIPLEX SWITCH



Die Characteristics

Transistor Count		253
Die Size		116 x 79 mil
Thermal Constants	θ_{ja}	78°C/W } For Ceramic Dip
	θ_{jc}	25°C/W } For Ceramic Dip
Tie Substrate to:		-VSupply
Process:		CMOS - DI

National Semiconductor

CD4518BM/CD4518BC, CD4520BM/CD4520BC
Dual Synchronous Up Counters

General Description

The CD4518BM/CD4518BC dual BCD counter and the CD4520BM/CD4520BC dual binary counter are implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors.

Each counter consists of two identical, independent, synchronous, 4-stage counters. The counter stages are toggle flip-flops which increment on either the positive-edge of CLOCK or negative-edge of ENABLE, simplifying cascading of multiple stages. Each counter can be asynchronously cleared by a high level on the RESET line. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ 6MHz counting rate (typ.) at V_{DD} = 10V	

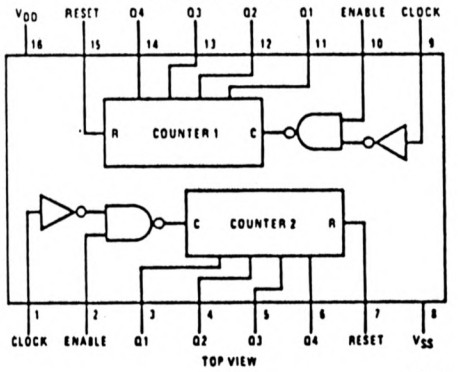
Truth Table

CLOCK	ENABLE	RESET	ACTION
↓	1	0	Increment counter
0	↓	0	Increment counter
↓	X	0	No change
X	↓	0	No change
↓	0	0	No change
1	↓	0	No change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Order Number CD4518BMJ, CD4518BCJ, CD4520BMJ or CD4520BCJ
See NS Package J16A

Order Number CD4518BMN, CD4518BCN, CD4520BMN or CD4520BCN
See NS Package N16E

CD4518BM/CD4518BC, CD4520BM/CD4520BC

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4518BM, CD4520BM	−55°C to +125°C
CD4518BC, CD4520BC	−40°C to +85°C

DC Electrical Characteristics CD4518BM/CD4520BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.01	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	|I_O| < 1 μA, V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	|I_O| < 1 μA, V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	|I_O| < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	|I_O| < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4518BC/CD4520BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	|I_O| < 1 μA, V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	|I_O| < 1 μA, V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd) CD4518BC/CD4520BC (Note 2)

SYM	PARAMETER	CONDITIONS	-40°C MIN	-40°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS
V_{IL}	Low Level Input Voltage	I_O = 1 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.75	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	I_O = 1 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.75		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 9.5V	1.3		1.1	2.75		0.9		mA
		V_{DD} = 15V, V_O = 13.5V	3.6		3.0	8.8		2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		0.3		-10^{-5}	-0.3		-1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, t_r = t_f = 20 ns, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock → Q	V_{DD} = 5V		325	650	ns
		V_{DD} = 10V		110	225	ns
		V_{DD} = 15V		85	170	ns
t_{PHL}	Propagation Delay Time Reset → Q	V_{DD} = 5V		220	560	ns
		V_{DD} = 10V		90	230	ns
		V_{DD} = 15V		65	160	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5V	1.5	3		MHz
		V_{DD} = 10V	3.0	6		MHz
		V_{DD} = 15V	4.0	8		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		35	70	ns
t_{RCL}, t_{FC}	Maximum Clock or Enable Rise and Fall Time	V_{DD} = 5V	15			µs
		V_{DD} = 10V	10			µs
		V_{DD} = 15V	5			µs
t_{WH}, t_{WL}	Minimum Enable Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		55	110	ns
		V_{DD} = 15V		40	80	ns
t_{WH}	Minimum Reset Pulse Width	V_{DD} = 5V		180	375	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	130	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Either Counter (Note 4)		50		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

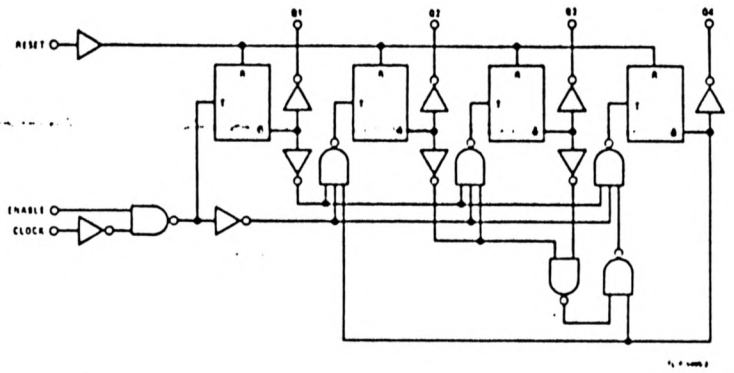
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

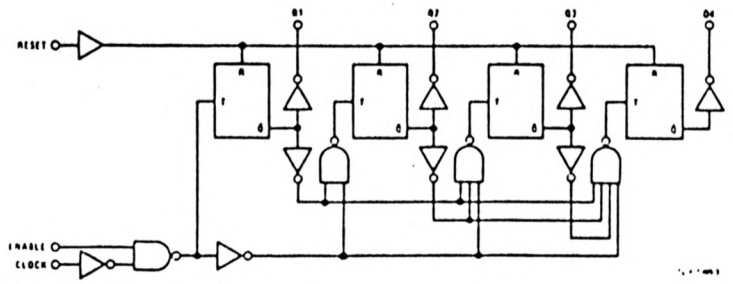
Note 4: C_{PD} determines the no load ac power consumption of a CMOS device. For a complete explanation, see "54C/74C Family Characteristics," application note AN-90.

Logic Diagrams

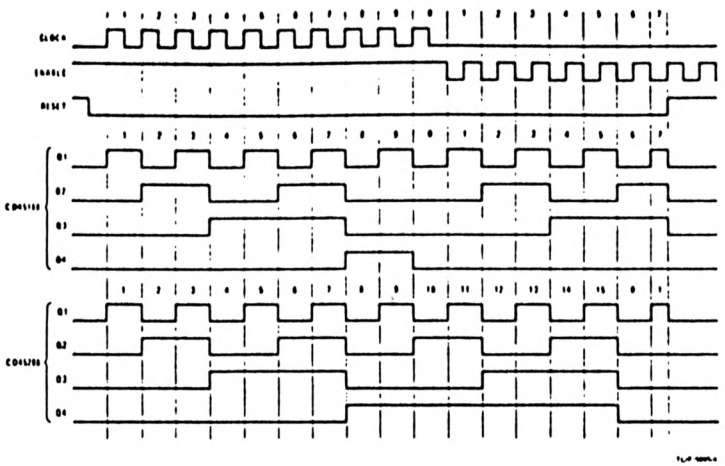
Decade Counter (CD4518B) 1/2 Device Shown



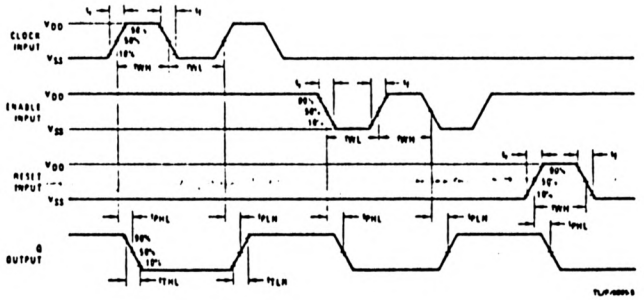
Binary Counter (CD4520B) 1/2 Device Shown



Timing Diagrams



Switching Time Waveforms



ANALOG DEVICES

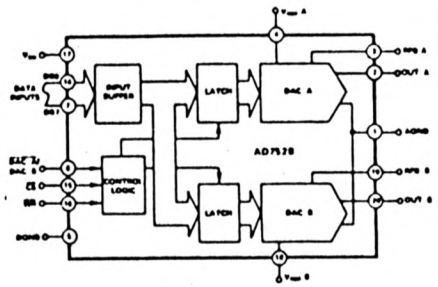
CMOS Dual 8-Bit Buffered Multiplying DAC

AD7528

FEATURES
On-Chip Latches for Both DACs
+5V to +15V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible
Latch Free (Protection Schottkys not Required)

APPLICATIONS
Digital Control of:
Gain/Attenuation
Filter Parameters
Stereo Audio Circuits
X–Y Graphics

AD7528 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{DAC\ A}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5V to +15V power supply, dissipating only 20mW of power.

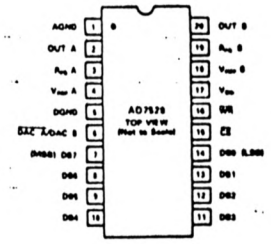
Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

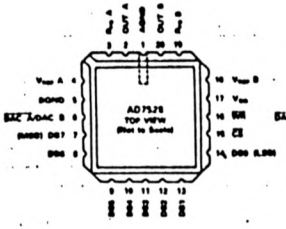
1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{DAC\ A}$/DAC B select line has allowed the AD7528 to be packaged in either a small 20-pin 0.3" wide DIP or in 20-terminal surface mount packages.

PIN CONFIGURATIONS

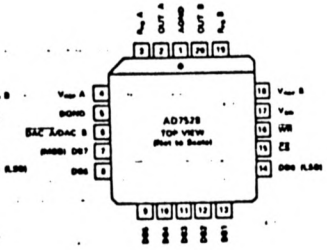
DIP



LCCC



PLCC



SPECIFICATIONS (V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}–T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}–T_{max}	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, E	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±1/2	±1/2	±1/2	±1/2	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, E	±4	±6	±4	±5	LSB max	Measured Using Internal R FB A and R FB B.
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 1 and 2.
Gain Temperature Coefficient[3]							
ΔGain/ΔTemperature	All	±0.002	±0.002	±0.0001	±0.0001	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±10	±400	±10	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±30	±400	±10	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	All	8	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A-V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[4]							
Input High Voltage V_{IH}	All	2.4	2.4	11.5	11.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
D80–D87	All	10	10	10	10	pF max	
$\overline{WR}$, $\overline{CS}$, DAC A, DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[5]							See Timing Diagram
Chip Select to Write Set Up Time t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time t_{DS}	All	130	130	30	40	ns min	
Data Valid to Write Hold Time t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended P.C. Board Layout and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}–T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}–T_{max}	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV$_{DD}$)	All	0.02	0.04	0.01	0.02	% per % max	ΔV$_{DD}$ = ±1%
CURRENT SETTLING TIME[5]	All	350	400	180	200	ns max	To 1/2 LSB. Out A/Out B load = 100Ω. $\overline{WR}$ = $\overline{CS}$ = 0V. DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10V. OUT A, OUT B Load = 100Ω C$_{EXT}$ = 13pF. $\overline{WR}$, $\overline{CS}$ = 0V DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL TO ANALOG GLITCH IMPULSE	All	160	-	640	-	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C$_{OUT}$ A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C$_{OUT}$ B		50	50	50	50	pF max	
C$_{OUT}$ A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C$_{OUT}$ B		120	120	120	120	pF max	
AC FEEDTHROUGH							
V_{REF} A to OUT A	All	−70	−65	−70	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave @ 100kHz
V_{REF} B to OUT B		−70	−65	−70	−65	dB max	
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	All	−77	-	−77	-	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz. V_{REF} B = 0V.
V_{REF} B to OUT A		−77	-	−77	-	dB typ	V_{REF} B = 20V p-p Sine Wave @ 100kHz. V_{REF} A = 0V.
DIGITAL CROSSTALK	All	30	-	60	-	nV sec typ	Measured for Code Transitions 00000000 to 11111111
HARMONIC DISTORTION	All	−85	-	−85	-	dB typ	V_{REF} = 6V rms @ 1kHz

NOTES
[1]Temperature Ranges are: J, K, L Versions, −40°C to +85°C; A, B, C Versions, −40°C to +85°C; S, T, U Versions, −55°C to +125°C.
[2]Specifications applies to both DACs in AD7528.
[3]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.
[4]Guaranteed by design but not production tested.
[5]These characteristics are for design guidance only and are not subject to test. Specifications subject to change without notice.

INTERFACE LOGIC INFORMATION

DAC Selection:
Both DAC latches share a common 8-bit input port. The control input $\overline{DAC\ A}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:
Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:
When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{DAC\ A}$/ DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

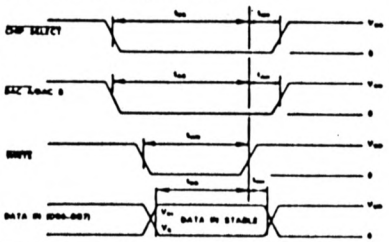
L = Low State H = High State X = Don't Care

Mode Selection Table

CAUTION:

1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

WRITE CYCLE TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

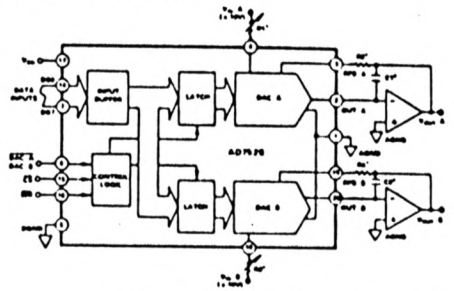
V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, L) Grades	−40°C to +85°C
Industrial (A, B, C) Grades	−40°C to +85°C
Extended (S, T, U) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300 C

ORDERING INFORMATION[1]

Relative Accuracy	Gain Error T_A = +25°C	Temperature Range and Package Options[2,3] −40°C to +85°C	−40°C to +85°C	−55°C to +125°C
		Plastic DIP (N-20)	Hermetic (Q-20)	Hermetic (Q-20)
±1LSB	±4LSB	AD7528JN	AD7528AQ	AD7528SQ
±1/2LSB	±2LSB	AD7528KN	AD7528BQ	AD7528TQ
±1/2LSB	±1LSB	AD7528LN	AD7528CQ	AD7528UQ
		PLCC[4] (P-20A)		LCCC[5] (E-20A)
±1LSB	±4LSB	AD7528JP		AD7528SE
±1/2LSB	±2LSB	AD7528KP		AD7528TE
±1/2LSB	±1LSB	AD7528LP		AD7528UE

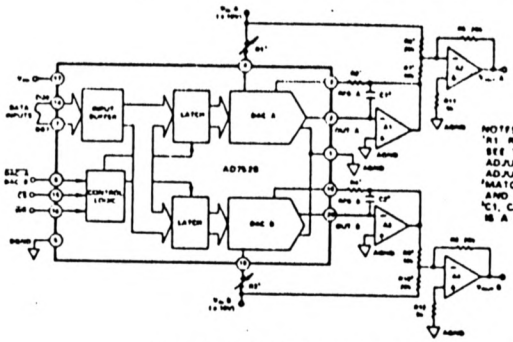
NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-87701.
[2]See Section 14 for package outline information.
[3]Also available in SOIC package (AD7528KR, AD7528LR).
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

Applying the AD7528



NOTES
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES
[2]C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION

Figure 1. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table I.



NOTES
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES
ADJUST R1 FOR V_{OUT} A = 0V WITH CODE 10000000 IN DAC A LATCH.
ADJUST R3 FOR V_{OUT} B = 0V WITH CODE 10000000 IN DAC B LATCH.
[2]MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
[3]C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BE REQUIRED IF A1/A2 IS A HIGH SPEED AMPLIFIER

Figure 2. Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table II.

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$-V_{IN}\left(\frac{255}{256}\right)$
10000001	$-V_{IN}\left(\frac{129}{256}\right)$
10000000	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
01111111	$-V_{IN}\left(\frac{127}{256}\right)$
00000001	$-V_{IN}\left(\frac{1}{256}\right)$
00000000	$-V_{IN}\left(\frac{0}{256}\right) = 0$

Note 1LSB = $(2^{-8} \times V_{IN}) = \frac{1}{256}(V_{IN})$

Table I. Unipolar Binary Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$+V_{IN}\left(\frac{127}{128}\right)$
10000001	$+V_{IN}\left(\frac{1}{128}\right)$
10000000	0
01111111	$-V_{IN}\left(\frac{1}{128}\right)$
00000001	$-V_{IN}\left(\frac{127}{128}\right)$
00000000	$-V_{IN}\left(\frac{128}{128}\right)$

Note 1LSB = $(2^{-7} \times V_{IN}) = \frac{1}{128}(V_{IN})$

Table II. Bipolar (Offset Binary) Code Table

Trim Resistor	J/A/S	K/B/T	L/C/U
R1;R3	1k	500	200
R2;R4	330	150	82

Table III. Recommended Trim Resistor Values vs. Grade