VLA Technical Report No. 70
X-BAND LOCAL OSCILLATOR-MIXER
Module Type F12

Larry Beno and David Weber
9/25/92

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1.0 INTRODUCTION

This manual describes the VLA 12-15 GHz (X-Band) Local Oscillator-Mixer, module type F12. The emphasis of this manual is on the F12 theory of operation (Section 2) and Alignment and Bench Tests (Section 3). Construction details are not included but all drawings used in F12 fabrication are listed in the BOM (Bill of Materials) drawing. Section 4 contains the drawings and Section 5 contains the Data Sheets for the special-purpose components used in F12. The Appendix (Section 6) lists VLA Technical Reports and other reference data which are relevant to the operation of F12.

1.1 F12 ROLE IN THE VLA

The VLA is equipped to receive seven bands consisting of P (400 cm and 90 cm), L (1.4 cm), S (13 cm), C (6 cm), X (4 cm), U (2 cm), K (1.3 cm) and is being outfitted for the Q (0.7 cm) band. F12 is one of the components of the X-Band implementation.

The VLA receiving system uses the superhetrodyne principle. In a superhetrodyne receiver, a local oscillator signal (LO) is mixed with the Received Signal (RF) from a tuned pre-amplifier to create two signals that are the sum and difference of the RF and LO frequencies; these signals are sometimes called side-bands. The lower (difference frequency) side-band is usually amplified as an Intermediate Frequency (IF) signal and is then detected to produce a base-band output. The function of converting an RF signal to another frequency by the superhetrodyne process is sometimes called frequency conversion.

VLA receiver implementation details vary between bands but all bands conform to the superhetrodyne scheme outlined above. In the VLA, the preamplifiers are the older A-Rack receivers, uncooled P-Band receivers and the newer generation, Single-Band, Front End Receivers. The Single-Band, Front End Receiver is typically a Dewar assembly containing cooled, tuned amplifiers and power calibration circuitry. Each band has a dedicated front end and mixer that produces an IF signal which (through a coaxial selector switch) drives the IF system. The IF and Transmission systems in the B-Rack transmit the IF (and other signals) down the waveguide to the Central Control Building where the IF (and the other) signals are detected and processed. Implementation details of the other bands, IF and Transmission systems are beyond the scope of this manual and therefore will not be described; interested readers are referred to the VLA Technical Reports listed in the Apppendix.

The incoming astronomical signal is split into two components (LCP for Left Circular and RCP for Right Circular Polarization) by a polarization transducer between the antenna feeds (usually a feed horn) and the front end receiver. In the A-Rack F4's, the LCP and RCP IF signals are separated into four IF paths (A, B, C and D) for further amplification and processing. These four signals have independant (but identical) paths through the IF, transmission and detector systems. The F12 drawings use the A/B and C/D nomenclature to designate the RCP and LCP signals, respectively.

The local oscillator signals used in the signal conversions at all of the antennas must be coherent in phase to preserve the correletion of the received signals. The 5 Mhz antenna oscillators (L1) in each of the antennas are therefore phase-locked to a 5 Mhz Master Oscillator in the Control Building. [1] In the F12, the 12-15 GHz local oscillator is phase-locked to a harmonic of the antenna oscillator by the use of 200 MHz and 600 MHz reference signals derived from the 5 MHz antenna oscillator.

The two F12 IF output signals A/B and C/D cover the band of 4.5 to 5.0 GHz and are fed to module F9 in the A-Rack where they are selected for input to the IF system by the coaxial selector switch.

[1] VLA Technical Report No. 29, page I-2

1.2 F12 FUNCTIONS AND CONTROL MODES

Drawing C13165B01 is a block diagram of the F12 module. F12 performs two functions: 1) Synthesis of a 12 - 15 GHz, phase-coherent LO signal and 2) Mixing this LO signal with the RF signal from the X-Band front end to produce the two 4.5 to 5.0 GHz IF signals.

The local oscillator is an Avantek AV-71251 YIG (Yttrium/Iron/Garnet) microwave oscillator module purchased as a commercial component. The YIG oscillator uses a YIG sphere as a magnetically tunable resonant cavity; a GaAs FET or Bipolar transistor provides the power to sustain oscillations and drive the LO load. YIG oscillators exhibit high spectral purity and tuning linearity. YIG oscillation frequency is determined by the cavity size and an external magnetic field created by currents through a Tuning coil and an FM coil. The magnetic field results from the composite sum of the two currents. In the F12 application, current through the Tuning coil sets the approximate oscillation frequency and current through the FM coil is used to phase-lock the oscillator to the reference frequencies. YIG frequency control is an important concern in the design of the F12.

The F12 YIG oscillator must be settable to twelve standard frequencies over a 12 to 15 Ghz band. These frequencies are tabulated below. Using the 200 MHz and 600 MHz reference frequencies, the loop control circuit phase-locks the YIG to harmonics of the antenna 5 MHz oscillator. The standard lock frequencies are given by:

F_o = (N x 600) +/- 200 MHz, where N is an integer ranging from 20 to 25. When the YIG is locked to a + 200 MHz case, the YIG is defined to be in High Lock. The converse case is defined as Low Lock.

Using the + (High lock) and - (Low lock) symbols as a suffix, YIG lock frequencies are:

11.8 GHz-	12.4 GHz-	13.0 GHz-	13.6 GHz-	14.2 GHz-	14.8 GHz-
12.2 GHz+	12.8 GHz+	13.4 GHz+	14.0 GHz+	14.6 GHz+	15.2 GHz+

Note that the frequency intervals are alternately 400 MHz and 200 MHz.

In commanding F12 to operate at one of the standard frequencies, the Tuning coil current is set to the N value; the FM coil current will be at about a mid-range level. These two currents will cause the YIG to oscillate at a frequency which is approximately N x 600 MHz + or - 200 MHz. The phase-lock control circuit then initiates a linear current ramp drive to the FM coil. When the FM coil current reaches the level at which the loop can lock (i.e. a current corresponding to the + or - 200 MHz offset frequency), the current ramp is stopped at the lock value and the FM coil current is controlled by the phase-driven loop control circuitry. The "A1" board contains the Tuning current and phase-lock control circuits; these are described in Section 2.4 below.

The YIG Tuning coil current can be set by two means: 1) A front-panel thumbwheel switch or 2) a digital command value from the central control computers via the Monitor and Control system and the Data Set. Controlling the current in the Tuning coil is sometimes referred to as coarse tuning. The front panel thumbwheel control mode is typically used on the test bench for alignment and in the antenna, it is used to verify proper operation of the oscillator and control circuity. Digital control logic on the "A2" board selects either the thumbwheel digital code or a value in a Data Set-controlled command register. The digital logic board contains the Data Set interface, command register and thumbwheel/command register selector logic. This circuitry is described in Section 2.8 below.

The Tuning control argument format is a two digit (eight-bit), BCD code digital value specifying the units and tenth's digit of the commanded YIG frequency in Ghz. This format is common to both

AUTO (central computer) and MAN (thumbwheel) control modes and is described in Section 2.8.

The YIG oscillator output drives two sets of mixers that convert the RCP and LCP RF signals from the X-Band front end to IF signals A/B and C/D that are connected to F9 in the A-Rack. A power divider, band-pass filters and isolators are used in this circuitry which is described in Section 2.6.

The "A2" digital board also contains digital and analog circuitry to monitor the states of F12 control discretes and critical analog signals. The F12 frequency set-point command from the Data Set is read out as command echo monitor data to the Data Set to verify the proper operation of the command path. The command echo and digital monitor data formats and analog signal multiplexing are described in Section 2.9.

1.3 FRONT PANEL CONTROLS AND INDICATORS

F12 has front panel manual controls to select the YIG frequency and to display the FM coil voltage and IF level values. An AUTO/MAN YIG frequency control switch selects either frequency control via the Data Set (AUTO) or frequency control via the two-digit thumbwheel switch (MAN). The thumbwheel setting indicates the one's and tenth's digit (in Ghz) of the selected YIG frequency; the tens digit is implied.

A momentary-action, IF LEV/CONT VOLT toggle switch permits the IF level or YIG FM control voltage levels to be displayed on a front panel, bipolar bar-graph LED display.

A three-digit, numeric LED display shows the state of the command register which contains the computer or manually-commanded YIG frequency. The ten's digit is hard-wired to display "1".

Front Panel discrete LED's show the state of the H LOCK (High Lock) and L LOCK (Low Lock) phase-lock control circuit and the AUTO/MAN switch.

The YIG and phase-locked IF (200 MHz) signal spectrums may be monitored on the front panel LO MON (SMA) and IF MON (BNC) connectors.

1.4 F12 PHYSICAL DESCRIPTION

F12 is a two-wide module with the control and RF components mounted on a center component plate. The control PC board ("A1") and digital logic board ("A2") are mounted on the right side of the plate (viewed from the front of F12) and the RF components are mounted on the left side. Figures 1 and 2 (next two pages) show the two sides of F12 with the covers removed. Figure 3 (following page) shows the front and rear panel views.

A front panel PC board ("A3") contains the display components and circuitry.

The rear panel has an AMP 42 pin (P1) control and power connector and six "OSP" RF connectors (J7 through J12). These connectors are all blind-mating connectors physically referenced to the module guide blocks.

The YIG oscillator module is mounted on long spacers in front of the component plate. The spacers provide some thermal isolation for the YIG module, which has an internal heater and temperature control system to stabilize the YIG element dimensions.

The YIG Tuning and FM coils are electrically isolated from each other and the YIG internal oscillator circuitry. The oscillator circuitry is powered by +15 Volt power and the heater and temperature control circuitry is powered by +28 Volt power.

In some cases, the commercial modular RF components were ordered with connectors that permit them to be directly connected; this eliminates several semi-rigid coax cable runs. Reducing the number of semi-rigid cables makes the RF circuitry more compact and simplifies fabrication by reducing the number of semi-rigid interconnect cables to be fabricated. The part numbers listed on the BOM are those used in F12. The data sheets contained in Section 5 cover all the normal options for these devices. When additional parts are ordered, the BOM part numbers should be used.

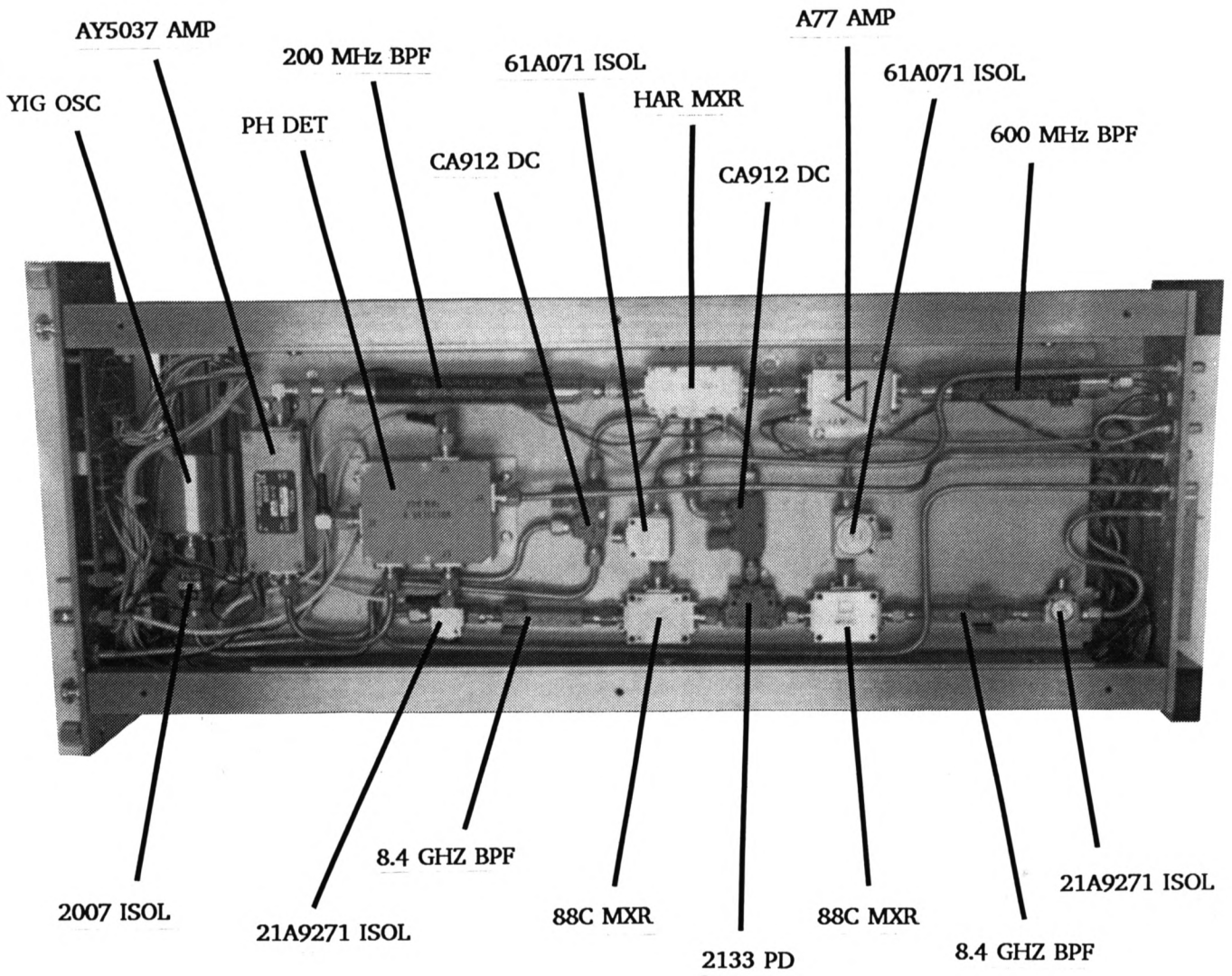


FIGURE 1, F12
RIGHT SIDE VIEW

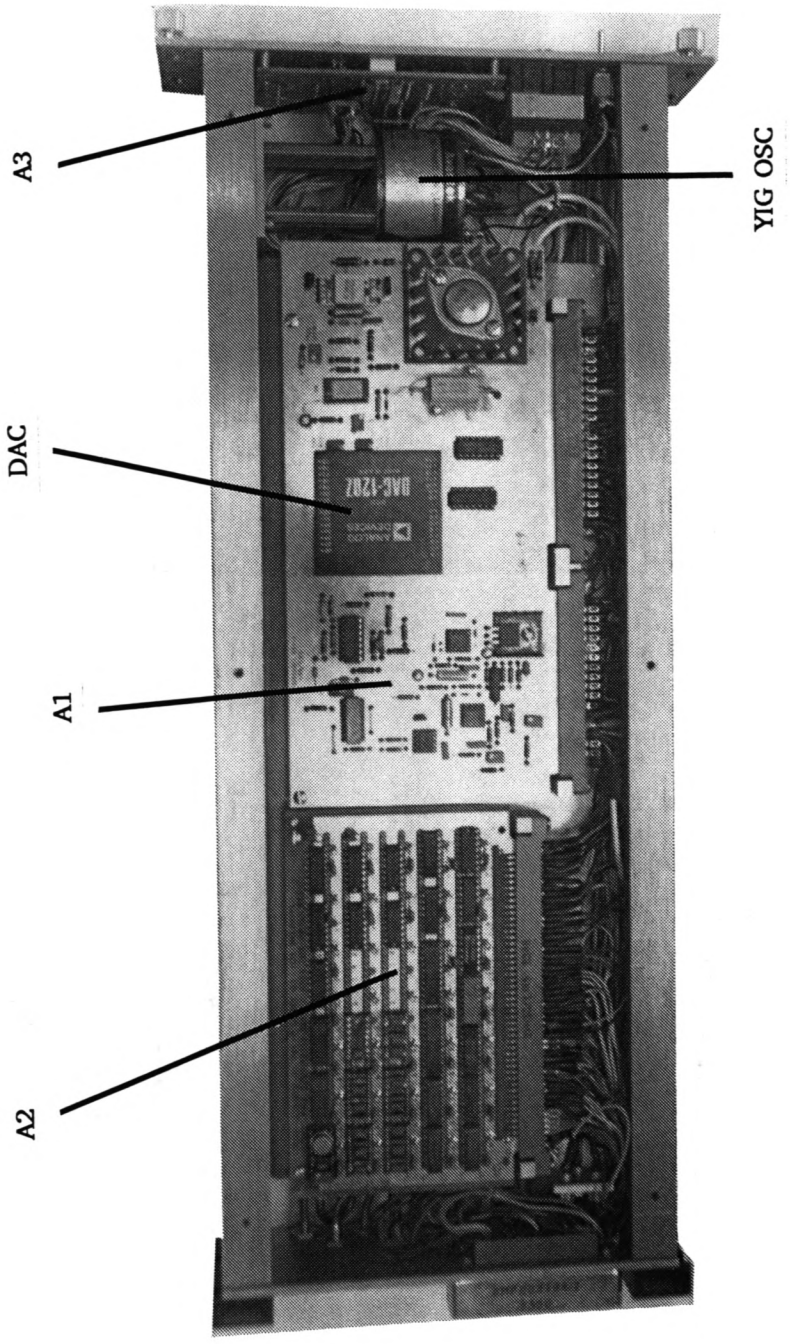
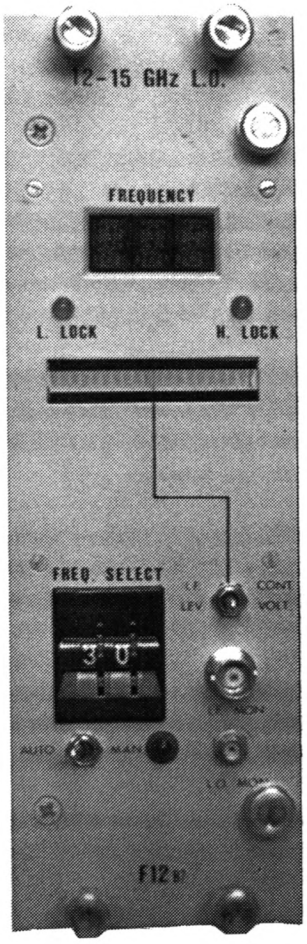


FIGURE 2, F12
LEFT SIDE VIEW



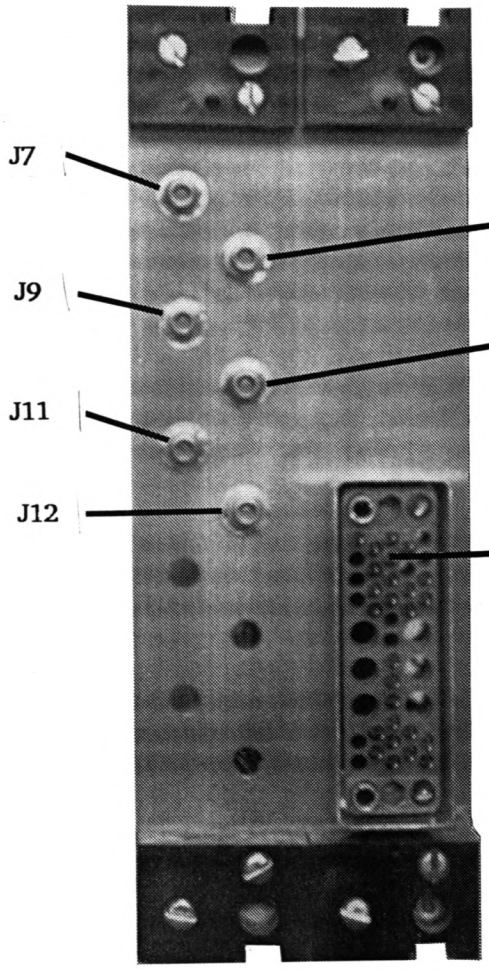


FIGURE 3, F12 FRONT AND REAR PANEL VIEWS

2.0 THEORY OF OPERATION

This section describes the F12 theory of operation. The YIG oscillator characteristics (Section, 2.1) and its frequency control circuitry (Sections 2.2 through 2.5) are the most important aspects of this manual. The RF to IF conversion description (Section 2.6) follows the YIG control circuitry description. Section 2.7 describes F12 power levels and spectrums. Section 2.8 describes the "A3" front panel display board. Section 2.9 describes the "A2" Monitor and Control board. Section 2.10 describes the commercial RF components used in F12; these consist of RF amplifiers, mixers, isolators, directional couplers, splitters and attenuators.

Drawings of interest in the following discussion are the F12 Block Diagram, the Module Wiring Diagram, the "A1" Control Board Schematic, the Harmonic Mixer Schematic, the 200 Mhz Phase Detector Schematic, the Front Panel Meter Circuit Schematic and the M&C ("A2") Board Logic Diagram. These drawings are found in Section 4.0. Section 5 Data Sheets are also important references.

YIG frequency control is a major emphasis of this manual. The YIG frequency control circuitry consists of three functional blocks: the "A1" control board, the 200 MHz Phase Detector and the Harmonic Mixer. The commercial RF components (amplifiers, filters, attenuators, etc.) used in the frequency control circuitry are important but straightforward elements; these components are briefly described in the context of their function in the YIG frequency control circuitry. They are more completely described in Section 2.10.

The "A1" Control Board (Section 2.2) is described first (after the YIG description) because it contains the Tuning coil and FM coil drive circuitry and the mode control logic. This circuitry sets the Tuning coil current level, determines the FM coil control modes (Search/Track), and drives the FM coil in both modes.

The 200 MHz Phase Detector (Section 2.3) is described next because the two output signals determine the operation of the FM coil control circuitry. The Quadrature-Phase signal determines the FM coil control modes (Search/Track). The phase-lock circuitry uses the In-Phase signal to control the FM coil current in the Track mode.

The Harmonic Mixer description (Section 2.4) follows the phase detector description. The Harmonic Mixer mixes the YIG output (11.8 to 15.2 GHz) with the 600 MHz reference to produce a 200 MHz signal which is the YIG signal N x 600 MHz + or - 200 MHz, where N = 20, ... 25.

Following these three descriptions, Section 2.5 describes the operation of the phase-locked frequency control loop.

2.1 YIG TUNING AND SPECIFICATIONS

The Avantek AV-71251 YIG oscillator operates over a 12 to 18 GHz range; the upper 3 Ghz of this range is not used in the F12 application. At this point the reader should review the AV-71251 Specification and Data Sheets in Section 5.

Although the AV-71251 data sheet does not specifically cite the oscillator's Q, the Avantek catalog states that Avantek YIG oscillators have a Q ranging between 1000 and 8000. This high Q provides a high frequency stability and the output has very low AM and FM noise components.

Avantek Data Sheets for each YIG characterize the YIG's Tuning current at frequencies of 12.0 GHz and 18.0 GHz. From the YIG Specification Sheet, typical Tuning coil sensitivity is 18 MHz/mA and linearity is +/- 0.1%. For the 12.0 to 15.2 GHz (3200 MHz) tuning range, the current span is thus 3200/18 = 177.77 mA. Average values of Tuning coil current for three randomly selected YIG's are 625.33 mA @ 12.0 MHz, 947 mA @ 18.0 GHz and the average sensitivity is 18.65 MHz/mA, in reasonable agreement with the Specification Sheet.

From the YIG Specification Sheet, typical FM coil sensivity is 450 kHz/mA. This parameter is not characterized on the individual YIG Data Sheets.

The YIG Tuning coil has a 5 KHz, 3dB bandwidth; that is, when the Tuning coil current is changed, the YIG output frequency cannot change faster than permitted by this bandwidth. This response is not a concern because after a commanded frequency change, the YIG Tuning coil is a DC drive.

The YIG FM coil has a 400 kHz bandwidth and is analagous to the Tuning bandwidth described above. Since the FM coil is driven by the phase-lock circuitry, this response is a concern in the phase-lock loop dynamics. This concern is discussed in Section 2.5.

The YIG has a Pulling Figure of 1.0 MHz with a return loss of 12 dB. This means that a VSWR of 1.7:1 on the YIG output resulting from an impedance mis-match can shift the YIG frequency by 1.0 MHz. An isolator on the YIG output reduces the YIG sensitivity to output mismatches.

The Magnetic Susceptability (sensitivity to influence by external magnetic fields) at 60 Hz is 50 kHz/Gauss. The earth's magnetic field flux density is about 1 Gauss, so variations in the orientation of the YIG relative to the earth's field could change the frequency by about 50 kHz. The steel walls of the Vertex Room provide some magnetic shielding from the earth's magnetic field. The intensity of the 60 Hz magnetic fields in the Vertex room has probably never been measured but the bandwidth of the phase-lock control circuit is adequate to remove this perturbation.

The YIG output 2nd harmonic is specified to be 12 dB below the output frequency; bench tests show that it is typically 20 dB below the output.

Over the 11.8 to 18.0 GHz operating frequency range, the YIG output power is 40 mW (+16 dBm) and the output varies no more than +/- 3 dB over this range.

2.2 "A1" CONTROL BOARD

The main functions of the "A1" board are to control the YIG Tuning and FM coil currents. The two coil drive circuits are described below. The Tuning coil is driven by an open-loop driver that has scaling and offset controls to scale the frequency to the commanded digital values. This circuit is described first. The FM coil is driven by a phase-locked, closed-loop controller which is described after the Tuning description.

YIG Tuning Coil Drive Circuit

The Tuning coil drive circuit consists of a DAC (U3), an operational amplifier (U4) to scale and offset the DAC drive, and a current source consisting of a non-inverting power operational amplifier (U5) which drives a power buffer transistor (Q1). Q1 is inside the U5 feedback loop and provides a current-sourcing drive to the Tuning coil.

The DAC is a three-digit, Binary-Coded Decimal, Digital-to-Analog converter which converts the BCD Tuning coil command to an analog value. The DAC is an Analog Devices DAC-12QZ/CDB, a complementary code, unipolar 12-bit unit that is jumpered to operate over an output range of 0.00 to +10.00 Volts. The two-digit BCD command value is converted to a high-true, 1's complement code by the eight 74L04 inverters on the two upper DAC inputs. The lower digit is not used and the four LSD lines float. This usage scales the units (MSD) digit to 1.00 Volt/count and the tenth's digit to 0.10 Volt/count. Since the DAC uses a complementary code, the four floating LSD lines are all logical "0's"; the resultant converted LSD value is thus 0.00 Volts. Settling time is 5 usec and a load strobe is not required. Two 20 kOhm potentiometers (R42 "Offset Adj" and R43 "Gain Adj") trim the DAC offset and scaling.

With this scaling, the DAC outputs are +2.00 Volts for a 12.0 GHz frequency setting and + 5.00 Volts for a 15.0 Ghz frequency setting. The YIG tuning is a linear function of Tuning coil current with an offset current. Therefore, the DAC output must be scaled and offset to properly drive the Tuning coil. U4 is a FET-input, operational amplifier (LH0022CD) that performs this function.

Potentiometer R45 is the "Frequency Slope" adjustment for the Tuning coil; this pot adjusts amplifier U4's gain to match the individual YIG's Tuning coil GHz/Ampere scaling. U4's gain is determined by (R6 + R45)/R2. Taking into account resistance tolerances and the setting of R45, the gain may be adjusted over a range of 0.238 to 0.301. These gains thus scale the 3.2 Volt DAC range (12.0 to 15.2 GHz) to -0.762 and -0.963 Volts, respectively.

Potentiometer R44 is the "Frequency Offset" adjustment that offsets the output of amplifier U4. At a frequency setting of 12.0 GHz, the DAC output is +2.000 Volts. It is necessary to offset the Tuning coil drive so that at 12.0 GHz, the YIG is driven with the appropriate current. Each YIG requires a slightly different Tuning current at 12.0 GHz; R44 is adjusted to set the drive to the Data Sheet value.

Tuning coil offset is provided by biasing the U4 + input to a value of about -2.0 volts. This pulls the U4 output negative because the U4 negative input (the summing junction) will be driven to this negative value by the feedback. The offset voltage is determined by a resistive voltage divider (R44, R3, and R4) driven by a 6.2 Volt precision voltage reference diode (D1, a Motorola 1N827A). R44 (500 Ohms) is the offset adjustment. Taking into account resistance tolerances and extreme settings of R44, the amplifier offset may be adjusted between about -2.1 to -1.9 Volts.

U5, an LH0041, is a 0.200 Amp power operational amplifier with overload protection features on

both the inputs and output. U5 is configured as a voltage follower with PNP power transistor Q1 (2N3792) inside the feedback loop.

Capacitor C2 (3.3 nF) is a frequency compensation capacitor to eliminate oscillations. With this capacitor and the 150 Ohm load (R8), U5 is capable of a signal swing of about 14 volts at 12 kHz.

The YIG Tuning coil current path is: (1) from (+/-15 Volt) common, (2) through R10 (5 Ohms) to the emitter of Q1 (2N3972), (3) out the collector to the Tuning coil + terminal, (4) through the coil and out the - terminal, (5) off the "A1" board via J1-D and through R11 (5 Ohms) to - 15 volts. If Q1 was a short, the Tuning coil current would be limited to 0.937 Amp by the 16 Ohms series path resistance (e.g. coil resistance is 6 Ohms and R11 and R10 are each 5 Ohms). The maximum Tuning coil current is about 800 mA @ 15.2 GHz (about 620 mA @ 12.0 GHz, linearly increasing by about 180 mA to 800 mA @ 15.2 GHz). The YIG tuning coil is thus inherently protected from overcurrent drive.

The 2N3972 data sheet shows a Beta ranging between a minimum of 50 to about 100 at a collector current of 1 Amp and a junction temperature of 25 degrees C. Beta increases slightly at a Junction temperature of +175 C. With the 2N3972 minimum Beta, the LH0041 must drive (i.e. sink) the 2N3972 base with 16 mA to cause a collector current of 800 Ma, the required 15.2 GHz Tuning current. The Base-to-Emitter voltage will be about -0.7 volts so the LH0041 output will be 1.5 Volts more negative than the Emitter. Since the 2N3972 is inside the LH0041 feedback loop, the Base-to-Emitter bias is not a value of great concern.

Consider the safety features of the Tuning coil drive circuit. Current limiting was covered above.

When the thumbwheel switches are being actuated, switch transitions and contact bounce can cause transient erratic digital values which will be fed through the DAC to the Tuning coil analog circuits. Single-pole RC filter R7-C1 has a time-constant of about 30 mS to reduce the effects of these transients. Capacitor C5 from the Q1 collector to ground also limits these transients.

Diode D2 inhibits the U4 output from going more positive than about +0.6 Volts. Zener diode D3 (V_Z = 6.8 Volts) clamps the U5 + input to -6.8 volts in the event of an over-range U4 output. Diode D4 (1N4007) clamps the Q1 base to about +0.6 volts in the event of a positive output malfunction of U5. Zener diode D5 (V_Z = 20 Volts) limits Tuning coil current in the event that Q1 fails open and the -15 Volt supply exceeds -20 Volts (e.g. a power supply failure).

The Tuning coil circuit has two analog monitor readout signals, Tuning Voltage and Tuning Current (octal mux addresses 50 and 53, respectively). The Tuning Voltage monitor is the output of U4 (LH0022) and the Tuning Current is the Emitter of Q1 through 10 kOhm isolation resistors. The 10 kOhm resistors reduce the effect of charge transfers caused by analog multiplexer switching. This effect is described in Section 2.8.

Section 5 contains data sheets for the DAC-12QZ/CBD, LH0022, LH0041 and 2N3792.

YIG FM Coil Drive Circuit

FM coil current is controlled by a phase-locked control loop (described in Section 2.5); the FM coil driver circuit is a major component of the control loop. The FM coil drive circuitry is similar to the Tuning coil drive circuit in that it uses an operational amplifier (configured as an integrator) for phase-tracking control and a current source to drive the FM coil. Unlike the Tuning coil, which operates at a fixed current level, the FM coil drive circuit must provide a varying current as a function of the two operating modes. The Quadrature-Phase signal from the 200 MHz Phase Detector determines the operating mode.

The two modes are Search and Track. In the Search mode the control circuit generates an FM Coil linear current ramp that causes the YIG oscillating frequency to increase in a corresponding manner. When the YIG frequency reaches a Low or High lock point, logic in the control circuit stops the current ramp and the FM coil current is controlled by the phase-lock loop which tracks the phase of the 200 MHz reference frequency. This is the Track mode. If the phase lock is lost, the control logic reverts to the Search mode to re-acquire phase-lock.

The 200 MHz Phase Detector signals are described in Section 2.4. Briefly, as a function of phase error, the In-Phase signal is a sine wave with an axis crossing at a phase error of zero degrees and the Quadrature-Phase signal is a cosine wave with a peak at zero phase error. The Quadrature-Phase signal can have either a plus or minus polarity depending upon the selection of either the + or - 200 MHz frequency case in the F_0 = (N x 600) +/- 200 MHz equation. The sine-cosine relationship of the In-Phase and Quadrature-Phase signals are shown on Figure 4, above.

When the loop is locked, the FM coil is driven by the In-Phase signal and integrated by U9.

Referring to Figure 4, it is evident that if the control loop is opened so that the phase error is free to drift, the error would probably increase in either a positive or negative direction. This is the usual behavior of control loops that lose their feedback. As the error increases, the In-Phase signal increases. Also, the Quadrature-Phase signal decreases from either a + or - maximum at zero error. When the phase error is + or - 90°, the Quadrature-Phase signal becomes zero. The FM coil mode control circuitry has threshold comparators that sense a low-level condition (at a phase error of about +/-77 degrees). When the Quadrature-Phase signal diminishes to this threshold, the loop is considered to be out of lock and the FM coil control circuitry is set to the Search mode.

Operational amplifier U6 (RC4136DC, a quad 741) functions as a high-gain threshold comparator operating on the Quadrature-Phase signal. The first stage is an inverting amplifier with a gain of 19.6. It also functions as a low pass filter with a 1 mS time constant.

The first U6 stage drives two other stages of U6 configured as threshold comparators (no feedback resistors, hence open loop operation) with reference voltages of + and - 1.07 Volts. The comparator outputs drive five 7406 open-collector buffers through a 1 kOhm resistor and a 4.7 volt Zener diode. Three of the buffer's outputs are wire-Or'ed with a common pull-up resistor. (Ignore the U7-9 output for the moment; the functions of the two other buffers are described below.) The reference voltages are + and - 55 mV, referred to the first stage of U6 (i.e. 1.07/19.6 = 0.055 V). If the Quadrature-Phase signal is **outside** the + or - 55 mV threshold window, one of the comparator outputs will swing largely positive, which puts a logic low on the 7406 wired-Or output. This low holds the sweep oscillator U8 reset.

If the Quadrature-Phase signal is **inside** the + or - 55 mV threshold window, the U7 wired-Or goes to +5 volts, which lifts the reset from U8 so that it can oscillate. The square-wave output of the 555 drives inverting operational amplifier U9 (OP27EP) which is an integrator. The integrator output is a voltage ramp that provides a frequency sweeping drive to the FM coil. This ramping drive in the Search mode is described below.

The two paragraphs above describe the **logic** of the comparator-555 reset circuit. A high Quadrature-Phase signal does

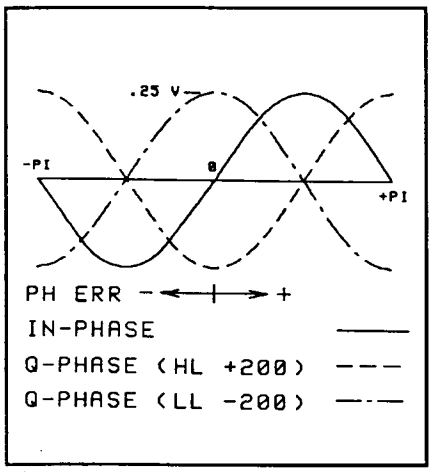


Figure 4, Quadrature and In-Phase Signals

not guarantee that the loop is locked but it is an indication that it **could** be locked. (Phase-lock acquisition is described in Section 2.5.) The integrator is **always** driven by the In-Phase signal; the comparator-555 reset logic enables the 555 square-wave drive to be injected into the integrator summing junction. This square-wave drive (ignoring the In-Phase drive for the moment) induces a voltage ramp on the integrator output.

If the 1 kOhm resistors and Zener diodes were not present, the comparator outputs would swing to either the + or - rail, typically about + or - 13 Volts. The amplifier output resistance (about 100 ohms), 1 kOhm resistor and Zener diode load the outputs which reduce the swing to about 10 Volts; the level is not critical. When a comparator output is positive, it sources current to the 1 kOhm resistor and 4.7 Volt Zener diode so the 7406 (U7) sees a logic high input. When a comparator output is negative, the Zener diode is forward biased (about 0.6 volts) and the 7406 input (emitter) sinks current to the Zener. The - 0.6 volt level is a logic low input to the 7406; if all three of the wired-Or 7406 inputs are low, the open-collector outputs rise to +5 volts via the pull-up resistor.

The third 7406 (U7 9-8) is used to force the wired-Or low to inhibit the sweep oscillator (U8) for bench alignment purposes. When S1 ("Sweep" switch) is set to "Off", the U7 9-8 input goes to +5 V through the pull-up resistor which forces the wired-Or low, holding the oscillator reset.

Two other U7 buffers are used to sink current to front panel H LOCK (High Lock) and L LOCK (Low Lock) LED's. If the Quadrature-Phase signal is more negative than the - 55 mV threshold, the H LOCK LED is powered. If the Quadrature-Phase signal is more positive than the + 55 mV threshold, the L LOCK LED is powered.

The sweep oscillator U7 is an LM555CN timer configured as an astable oscillator with a TTL logic level output. The period of the oscillator is given by $T = 0.693(R_{28} + 2R_{29})C_6$ and is about 37.7 mS. In this configuration, the capacitor charges to 2/3 V_{cc} at which point the Threshold input is triggered and the capacitor begins to discharge. When it reaches 1/3 V_{cc}, it activates the Discharge input which causes the capacitor to resume charging. The 555 output is high during the charge period and low during the discharge period. Charge time is given by $T_{CH} = 0.693(R_{28} + R_{29})C_6$ and is 19 mS. Discharge time is given by $T_{DIS} = 0.693(R_{28})C_6$ and is 18.7 mS. C7 is connected to the Control Voltage input. This input can be used to modulate the 555 frequency and in this application, should not be allowed to float. The capacitor charges to 2/3 V_{CC}. The 0.01 uf value is recommended by the 555 data sheet. For additional details on the 555, see the LM555CN data sheet in Section 5.

When the 555 is oscillating, the output is a 3.3 Volt, 27 Hz square-wave. When the 555 output is a logic low (during the reset state or low periods when it is oscillating), the level is less than +0.01 volts under the conditions imposed by the integrator drive.

When the Reset input is raised high, the 555 is enabled to oscillate and the output immediately jumps to a logic high; when it is set low, the output reverts to logic low within about 500 nS.

The FM coil drive circuit consists of the integrator U9 (OP27EP) that drives a second operational amplifier U10 (OP27EP) which functions as a current source. U10 is configured as a voltage follower with a power Darlington transistor Q2 (D44C8) inside the feedback loop.

Setting aside for the moment the In-Phase drive, consider the integrator response to the 555 square wave drive. In this mode, the integrator has two time constants, T_{RD1} and T_{RD2}; the first time constant is the dominant factor in ramping as is shown below. T_{RD1} is 3.0 mS ($T_{RD1} = R_{31} \times C_9$) where R_A is the resistance of R30 paralleled with R31. The second time constant T_{RD2} is 4.5 uS ($T_{RD2} = R_{36} \times C_9$).

The 3.3 Volt 555 output is AC-coupled to the integrator via capacitor C8. C8 will be charged to about +0.010 volts (a negligible value) when the oscillation starts because the 555 output will have been low for an indefinite period. Since R31's low side is connected to the summing junction of U9, it is effectively in parallel with R30. Taking this paralleled resistor shunting effect into account, the C8 x R30||R31 time-constant is 0.424 Seconds. Time-constant arithmetic shows that during the first 19 mS high output period, the voltage at the C8-R31 junction droops about 90 mV (from the initial 3.3 Volts) because C8 is slowly charging. During the next 19 mS low period, C8 discharges slightly so the C8-R31 junction voltage rises slightly. If the 555 were to continue to oscillate (it doesn't), C8 would charge to +1.65 volts in about 75 cycles of oscillation. The effect of the small droop and rise on the integrator operation is negligible.

The most important aspect of this AC coupling is that when the 555 starts to oscillate, its output immediately jumps from a logic low to logic high (about +3.3 volts) because C8 is not charged. The initial input to the integrator is a 3.3 Volt high signal with a duration of 19 mS. Following this high level is a low level (about +0.01 volts) of about 19 mS duration. As will be shown below, during the 19 mS low period, the integrator output ramps positively, sweeping the FM coil through the 63 MHz lock point range.

If the input to a simple (first order) integrator is a **constant** voltage, the integrator output is given by: $V_{out} = - (V_{in}/T) \times t$, a constant slope ramp voltage where T is the time constant. The U9 integrator is a second-order integrator which has two time constants, $T_{RD1} = R_{31}C_9$ (3mS) and $T_{RD2} = R_{36}C_9$ (4.5 uS). If the input to this second order integrator is a **constant** voltage, the integrator output is given by: $V_{out} = - V_{in}(t/T_1 + T_2/T_1)$. The T_{RD2}/T_{RD1} ratio is 0.0015, so that (for the ramping function) the second time constant is negligible and the integrator can be considered to be of first order.

If diode D10 is not in the circuit, U9's output is (for the initial high period output of the 555) a negative-going linear ramp having a slope of -1.1 V/mS. At 3 mS after ramp start, the output is -3.3 volts and at 19 mS (the end of the high period), the output would be -20.9 volts but the operational amplifier will be limited at about -13 volts. Now consider the effect of D10. D10 limits the integrator output when it tries to go more negative than -0.6 volts; the circuit then stops being an integrator and becomes a simple diode-limited operational amplifier. The amplifier output remains in this limited state for about 18.5 mS, the balance of the 19 mS period.

During the 555 low period following the 555 high output period, the integrator ramps positively with a +1.1 V/mS slope from the -0.6 volt level. The integrator output rises linearly to about +13 volts, the positive limit of output. This limit is reached about 12.4 mS after the ramp starts. Zener diode D13 and R37 limit the drive to U10 (another OP27EP) to +12 volts. If the phase-lock circuit did not manage to capture lock during this positive ramp, at the end of the 19 mS low period, the integrator would ramp negatively to the -0.6 level and the cycle would repeat. The integrator output signal (at TP2) is depicted in Figure 5.

During the positive slope current ramp, the YIG FM coil is swept to the lock-point frequency; it would continue through the 63 MHz range if the loop fails to lock. Since the FM coil is rapidly driven to the lockpoint by ramping, the acquisition is faster and more certain than would be the case if the lock circuitry had to do a long range frequency slew. Bench tests show that phase lock is acquired during the first 555 cycle.

Operational amplifier U10 (OP27EP) and transistor Q2 are the current source for the FM coil. U10 is configured as a voltage follower and Q2 is included inside the feedback loop of U10. Q2 is a D44C8, a NPN power Darlington transistor having a minimum Beta of 1000 and a low Collector-Emitter saturation voltage. $V_{CE(sat)}$ voltage = 2.0 V @ 10 A. With a collector current of 1 Amp and at a Junction Temperature of 25 C, typical Beta is 10,000. This high Beta enables U10 to comfortably provide the

fraction of a milliamp required to drive Q2's base.

Diode D14 limits the U10 drive to Q2 to about -0.6 volts, the lowest level from the integrator when it is sweeping. Zener diode D15 (1N4747A, V_Z = 20 volts) limits the FM coil current in the event that Q2 fails open and the + 15 volt power exceeds about 20 volts (e.g. a power supply failure). Capacitor C14 (0.001 uF) is used to prevent oscillation of the driving circuit.

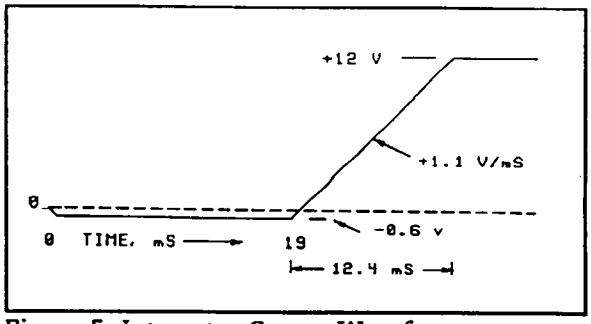


Figure 5, Integrator Sweep Waveform

The FM coil current path is from the +15 V power supply to the FM coil + terminal, through the coil, out the - terminal, and through Q2 to common via R39. R39 limits the FM coil current to about 150 mA. The FM tuning drop across R39 is divided by 10 kOhm resistors R25-R26 and the output drives the front panel bar-graph display.

From the above description, the drive to the unity-gain voltage-follower is first a -0.6 volt level followed by a positive ramp with a +1.1 V/mS slope ramps from -0.6 volts to +12 volts. We now consider the frequency sweep caused by the ramp. During the -0.6V portion of the Q2 input, no FM coil current flows because Q2 is negative biased; when the positive-going ramp reaches about +1 volts, Q2 begins to sink current through the FM coil. The Q2 Collector-to-Emitter voltage is about 1 volt over the current range of the ramp drive. 10 volts is the nominal voltage sweep range above the Q2 conduction threshold. The FM coil resistance is 1 Ohm so resistor R39 (100 Ohms) limits the FM coil current. Considering the series resistance of the FM coil, the Q2 Collector-Emitter drop and the 100 Ohms of R39, the maximum FM coil current is about 140 mA and zero mA is the mimimum. The typical YIG FM sensitivity (from the Specification Sheet) is 450 kHz/mA so the frequency sweep caused by the integrator ramp is about 63 MHz. This is about a 5 MHz/mS sweep rate.

Figure 5 depicts the integrator sweep waveform.

Remember that the lock-point frequency intervals are alternate 200 MHz and 400 MHz; since the frequency sweep is 63 MHz, the phase-lock circuitry cannot lock on an undesired lock point.

R46 ("Bal") is the integrator zero offset adjustment. The potentiometer is connected across two 10 Ohm resistors on the lower side of two voltage dividers to +15 volts. The potentiometer ends are connected to +0.003 and -0.003 volts, providing a 6 mV range of offset adjustment.

The operation of the integrator in the Track mode is described in Section 2.5.

Section 5 has data sheets for the OP27EP, D44C8, LM555CN and RC4136DC.

2.3 HARMONIC MIXER

The Harmonic Mixer is an important component of the phase-lock loop and is a micro-strip-discrete components PC board circuit housed in an NRAO-designed enclosure (listed in the Drawing List in Section 4). The reader should refer to the schematic diagram (in Section 4) during the following description.

The Harmonic Mixer mixes harmonics of the 600 MHz reference signal with the YIG output to produce a 200 MHz signal, which is **either** a N x 600 + **200** (High Lock) case **or** a N x 600 - **200** (Low Lock) case. After filtering and amplification, the 200 MHz IF signal drives the 200 MHz Phase Detector (described in Section 2.4). If there is a phase difference between the 200 MHz reference signal and the 200 MHz signal from the Harmonic Mixer, the phase control circuitry on board "A1" adjusts the drive to the FM coil which shifts the YIG frequency so as to minimize the phase error.

Following the usual mixer conventions, the 600 MHz signal is input via the LO port, the YIG is input via the RF port and the 200 MHz sum and difference output is fed out the IF port. The mixer is biased by a DC bias signal from the +15 volt power supply. The "A1" board has a 5 kOhm potentiometer (R47) that is used as an adjustable bias source; R1 is a current limiter for the bias input.

D1 is Schottky high barrier mixer diode (sometimes called a "Hot Carrier" diode) that is the non-linear element that mixes the 600 MHz and 12 - 15 GHz YIG signals. Schottky diodes have a low forward drop, fast recovery, a low junction capacitance and a low noise figure. D1 has a forward drop of about 0.5 volts at 1 mA, a junction capacitance of 0.10 pF, a noise figure of 6.5 dB and is tested at 16 GHz. Section 5 contains a data sheet for the TRW A2S124 Schottky mixer diode.

The schematic diagram shows a number of frequency-dependent components such as micro-strip stubs and parallel-resonant traps. These provide isolation between inputs and outputs and to suppress unwanted harmonic outputs. Mixer circuits have both the input frequencies, the sum and difference frequencies of the inputs, and can also have frequencies that are harmonics of the sum and difference frequencies. Proper operation of the phase-lock loop requires that unwanted signals be suppressed on the Harmonic Mixer inputs and output. The function of these frequency-dependent elements is described below.

Parallel-resonant traps are placed in the 600 MHz LO input and IF output paths. The left-most trap is tuned to about 200 MHz to keep 200 MHz out of the 600 MHz LO input port. The right-most trap is tuned to about 600 MHz to keep 600 MHz out of the IF output port.

Capacitors C1 and C5 are DC blocks to keep the mixer DC bias out of the LO and IF ports. The RF port (YIG) input is isolated by an external 10 dB attenuator that is unaffected by the DC bias.

In the LO input-to-mixer diode path, three series 50 Ohm micro-strip lines interconnect the LO input (J1), the blocking capacitor (C1), the 200 MHz parallel-resonant tank circuit (L1 and C2) and two 1/4 wave (at 13.5 GHz) micro-strip stubs. (The 1/4 wave micro-strip stubs are designated Lambda/4 on the schematic diagram.) The first 1/4 wave stub (shown vertically on the drawing) is open at the bottom which forces a short circuit at the junction of the two 1/4 wave stubs and the microstrip line from the tank. The short-circuit at this junction forces an open-circuit condition at the junction of D1 and the three 1/4 wave stubs. The IF output-to-mixer diode path is identical to the LO input-to-mixer path with a 600 MHz parallel resonant tank. The 1/4 wave stubs and the parallel-resonant tank circuits isolate the YIG signal from the LO input and IF output.

A series micro-strip line is also placed in the RF port-to-mixer diode path to isolate the RF port from the mixer products. A stub with a shorted end is tapped onto this stub to provide a DC path for the diode bias current.

The 200 MHz IF signal level from the Harmonic Mixer varies as a function of the set-up of the bias on the mixer diode and the 600 MHz reference signal level. The 200 MHz IF level should be between - 50 and -60 dbm. During F12 alignment, this level should be measured at all the standard frequencies.

Although it is not a Harmonic Mixer component, the function performed by the 600 MHz K&L bandpass filter should be mentioned in this section. The Antenna LO system 600 MHz reference signal that drives the LO input of the Harmonic Mixer also carries other LO system signals at low levels, 50 MHz being particularly prominant. If these other signals were input to the Harmonic Mixer, the resultant IF output spectrum would be much more complex which would complicate the design of the 200 MHz phase-lock control circuitry.

2.4 200 MHz PHASE DETECTOR

The 200 MHz Phase Detector is a subassembly consisting of a Directional Coupler, a two-way Power Splitter, two Double-Balanced Mixers and a 90 Degree Power Divider. The reader should review the schematic in Section 5. These five components are commercial units manufactured by Mini-Circuits and are installed on an NRAO-designed micro-strip PC board. The micro-strip PC board and board I/O OSM connectors are housed in an NRAO custom enclosure (listed in the Drawing List in Section 4). Data Sheets for these components are included in Section 5 and the components are described in Section 2.10.

The phase detector inputs are the 200 MHz reference frequency from the Antenna Local Oscillator System and the 200 MHz signal from the Harmonic Mixer, filtered by a 16 MHz-wide 200 MHz bandpass filter and amplified by a 66 dB gain amplifier. The 200 MHz input from the Harmonic Mixer is at a + 3 dbm level and the 200 MHz reference signal is at a + 10 dbm level. The phase detector outputs are the Quadrature-Phase and In-Phase signals mentioned in Section 2.2 above. The directional coupler on the phase detector input taps off a low-level sample (at - 9 dbm) of the Harmonic Mixer input for front panel spectrum monitoring.

The two-way power splitter equally divides the +3 dbm 200 MHz signal from the Harmonic Mixer into two signals which drive the RF ports of the two double-balanced mixers. The power splitter loss is less than 1/2 dbm and the two outputs have the same phase. Phase angle is important in the following discussion and the phase angle of the splitter outputs are defined as zero phase.

Conventional mixers form the product of two signals in a nonlinear circuit. The outputs contain both the input's sum and difference signals, the two input signals, and may also include harmonics of the input signals resulting from the action of the mixer's nonlinear elements. In contrast, a properly constructed, double-balanced mixer output contains only the sum and difference terms; the input signals are about 30 dB below the sum and difference signals. The double-balanced mixer is constructed of transformers and a diode bridge. Review the description of the Double-Balanced Mixers in the Data Sheets of Section 5.

The 200 MHz reference signal from the antenna LO system drives the 90 Degree Power Divider. One port is terminated by a 51 Ohm resistor. Two output ports drive the double-balanced mixers at a power level of +7 dbm. A very important property of the 90 Degree Power Divider is that one of the outputs leads the 200 MHz input by 45 degrees (relative to the 200 MHz reference signal) and the other lags by 45 degrees. The net effect is a 90 degrees phase difference between the outputs. The leading-phase output drives the In-Phase double-balanced mixer and the lagging-phase output drives the Quadrature-Phase double-balanced mixer. The mixer output signals are the **sum** and **difference** of the two 200 MHz inputs. The sum signal is about 400MHz and the difference signal is a low frequency signal that converges to a DC value when the difference frequency is zero. The sum signal is not used in the phase lock circuitry and the level is reduced by low-pass filters between the mixers and the output ports.

When the loop is **out of lock**, the difference signals of **both** the In-Phase and Quadrature-Phase mixers are AC signals, which is the frequency difference of the two 200 MHz inputs.

When the loop is **in lock**, the In-Phase and Quadrature-Phase mixer difference signals are a DC value which is a function of the phase difference between the two inputs.

Although the above difference signals sound identical, the functional relationships differ. **When the loop is locked**, the difference component of the In-Phase output is a **Sine function of phase difference** and the difference component of the Quadrature-Phase output is a **Cosine function of phase difference.**

The Cosine output can have two polarities, depending upon whether lock frequency is a + 200 MHz or - 200 MHz case. The sine and cosine relalationship is the result of the two mixer outputs being 90 degrees out of phase (+ and - 45 degrees) relative to the mixer RF port inputs. Figure 4 has been repeated to show the relationships of these two signals.

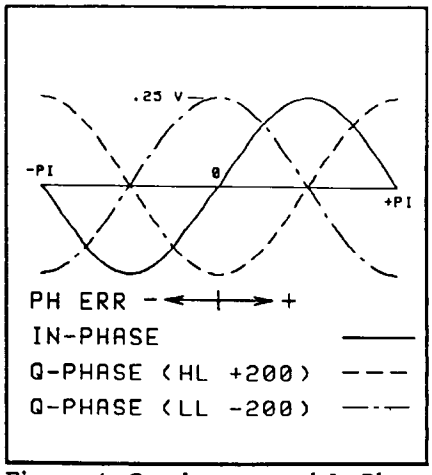


Figure 4, Quadrature and In-Phase Signals

The 400 MHz mixer sum signals are reduced by two sections of cascaded low-pass RC filters. The cut-off frequency of the In-Phase filter is about 1 MHz and the cut-off frequency of the Quadrature-Phase filter is about 300 kHz. The difference components of these two signals drive the "A1" board phase-lock control circuits described in Section 2.2.

Note Figure 4. As a result of the Cosine character of the Quadrature-Phase signal, when the phase error is low (or near zero), the Quadrature-Phase signal is at a positive or negative peak. When the phase error increases, the level decreases to zero at + or - 90 degrees of phase angle. This behavior provides a convenient way of determining when the loop is out of lock. The Quadrature-Phase input to board "A1" drives a comparator (U6) that operates upon both the level and polarity of this signal as described in Section 2.2. The comparator first stage amplifier also acts as a single-pole, low-pass filter with a -3 dB cutoff frequency of 1000Hz. This filter further reduces the AC component of the Quadrature-Phase mixer output. Note from Figure 4 that it is not desirable to permit the threshold voltage values to be very close to zero volts; component tolerance effects could introduce ambiguities in the logic decisions.

Note also from Figure 4 that as a result of the Sine character of the In-Phase signal, the signal level is zero (or low) when the phase error is zero. The signal increases positively or negatively as the error increases and the slope of the sine function is high (at small angles) so that small phase errors are indicated by a relatively large change in the signal. This portion of the sine function is an approximately linear function of the angle so that the magnitude and polarity of the signal are a convenient measure of the phase error. The linear behavior, high slope and phase-polarity detection of the In-Phase signal provide a convenient way to control the frequency of an oscillator in a closed-loop system. The closed-loop system alters the frequency of the oscillator so as to null the phase error.

The 200 MHz IF signal level from the Harmonic Mixer varies as a function of the set-up of the bias on the mixer diode and the 600 MHz reference signal level. The 200 MHz IF level should be between - 50 and -60 dbm.

V_p, the peak level of the In-Phase and Quadrature-Phase signals at the output ports, is about 250 mV.

K_p, the phase detector gain, is V_p/radian and is a parameter important in the phase lock control loop. A conservative value of K_p is 0.2V/rad. The phase gain is discussed in Section 2.5.

Section 5 has data sheets for the Directional Coupler (MCL PDC-10-1), the Power Divider (MCL PSC-2-1), the Mixer (MCL SRA-1) and the 90 Degree Power Divider (MCL PSCQ-2-250).

2.5 PHASE-LOCKED CONTROL LOOP

This section describes the operation of the YIG oscillator frequency control circuitry in the Track mode. In this mode, the YIG frequency is controlled by adjusting the current in the FM coil so as to null the phase error between the 200 MHz reference signal and the 200 MHz output of the Harmonic Mixer.

Phase-Locked Loop Properties

In a phase-locked loop, phase error is measured but frequency is adjusted. Phase is the time-integral of frequency. Integrator U9 integrates phase error to correct the VCO control voltage.

YIG frequency is controlled by a second-order phase-locked loop. Compared to a first order loop, a second order loop has additional low-pass filtering which reduces instabilities. This additional filtering provides "fly-wheel action" (analogous to inertial behavior) and the ability to smooth out fluctuations and noise on the inputs. Also, relative to the first order loop, the second-order loop reduces capture range and increases capture time. Capture means that the control loop has sensed and nulled the phase error and is in control of frequency. Second order loops also permit high loop gain at low frequencies; this is directly analagous to the effects of negative feedback in operational amplifier circuits.

Figure 5 is a block diagram of a phase-locked loop with the VCO (voltage-controlled oscillator) output phase fed back to the phase detector. The phase detector converts phase error to voltage and the VCO converts voltage to the time-derivative of phase (i.e. frequency). K_p is the phase detector constant mentioned in 2.4 above. K_{VCO} is the VCO constant.

The filter smooths variations in the phase error voltage.

The YIG oscillator is a form of VCO in that the output frequency is a linear function of FM coil current. K_{VCO}, the VCO constant, is 36×10^6 rad/Sec-volt.

The lock points are alternately 400 MHz and 200 MHz along the operating range of the F12. In setting the YIG to a new operating frequency, the Tuning and FM coil currents are set to a value close to the desired lock frequency. The mid-range value of FM coil current in conjunction with the Tuning coil current will produce a frequency close to the lock frequency. Since the sweep range is only 63 MHz (from 2.2 above), it is not possible for the loop to lock onto an undesired frequency.

Convergence to the Lock Frequency

In the Search mode, the integrator ramp slope is about 1.1 V/mS which produces a frequency sweep range of 63 MHz in about 12 mS. The frequency sweep rate is thus 63 MHz/12 mS or about 5 MHz/mS.

Since the FM coil produces a frequency sweep through the desired lock frequency, it is not necessary for the phase-lock circuitry to search for lock over a large frequency range but when the swept frequency approaches the lock frequency, the phase lock circuitry must capture phase lock by assuming control of the FM coil current. The time-response of the

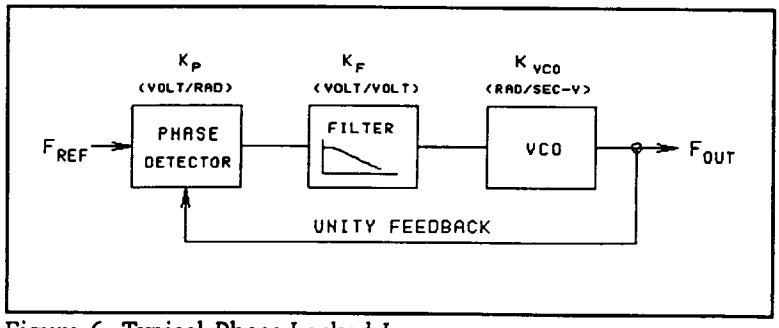


Figure 6, Typical Phase-Locked Loop

threshold comparators and response of the 555 reset (about 500 nS) must be fast enough to shut off the current ramping within the capture range of the phase-locked loop. During the sweep, as the sweep frequency approaches the lock frequency, the frequency difference decreases and then becomes zero. At a zero difference frequency, the Quadrature-Phase signal goes through zero volts and then begins to increase, either negatively or positively, following the cosine function. When the Quadrature-Phase signal reaches the + or - 55 mV threshold, one of the comparators resets the 555 and the output drops to a logic low within about 500 nS. This stops the current ramping. The comparator circuit is an AM detector; thus it performs a **logic** function and is not a factor in the phase-lock loop operation.

Since the 555 output is at a low level, the 555 reset has a minimal effect upon the integrator. If there is no time delay in the comparator circuitry, the 555 would be reset at the + or - 55 mV threshold. The first stage of the comparator is a combination amplifier-low pass filter with a -3 dB cutoff frequency of 159 KHz. The amplifier functions as a simple lag circuit that adds about 0.8 mS time lag to the comparator time response.

Consider the current drive to the summing junction from the two signal sources. The 3.3 volt drive from the 555 is input through a 200 kOhm resistor and the 225 mV drive from the In-Phase port is input through a 3.3 kOhm resistor. The ratio of In-Phase current span to ramping current span is about 4.5; thus the In-Phase signal is the dominant input to the integrator.

Until the difference frequency is zero, the two mixer's difference signal outputs are AC signals. The integrator's response to this AC signal is zero because it simply averages the input AC.

Loop Parameters

The performance of the phase-locked loop is a function of W_N (the loop natural frequency), K_O, K_P, T_1, T_2, D (the Damping Factor) and P_E (the maximum permissable phase error response to loop perturbations).

K_P, the phase detector constant, is determined by the characteristics of 200 MHz phase detector and is 0.2 rad/volt. K_O, the VCO constant, is determined by the characteristics of the FM coil drive circuit and YIG FM sensitivity. K_O is 56.5×10^6 rad/sec.

The loop should have high gain at the natural frequency W_N; this determines the loop's time-response to phase errors. A W_N of 314×10^3 rad/sec (50 KHz) was chosen. The OP27 has a gain-bandwidth product of 8 MHz. The switching characteristics of the current driver (D44C8) are a rise and delay time of 0.6 uSec, a storage time of 2.0 uSec and a fall time of 0.5 uSec. The characteristics of these two devices suggest that they are capable of operation at a loop bandwidth well over 100 KHz.

Using the selected W_N, T_1 was calculated from $W_N = (K_O K_P / T_1)^{1/2}$. T_1 = 49.5 uSec.

T_2 was calculated from $T_2 = 2D/W_N$. D was chosen to be 1.1 which made T_2 = 4.5 uSec.

Stability is a concern in any closed-loop system. Horowitz [2] states that if the loop gain falls off at -20 dB/decade in the neigborhood of unity gain, the loop will be stable. The integrator has two time constants. T_1 is 49.5 uS and is a pole. T_2 is 4.5 uSec and is a zero. T_2 alters the integrator's frequency response by reducing the rolloff near unity gain; this improves the phase margin, the difference between 180 degrees and the phase shift around the loop at unity-gain frequency.

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[2] Art of Electronics, Horowitz and Hill, page 648

Plotting open-loop gain (the composite of the OP27 open-loop gain vs frequency and the frequency response of T_1 and T_2) shows a unity-gain frequency of about 90 kHz and the slope is -20 dB/decade at unity gain.

W_N may be calculated from the phase stability specification, P_E. A basic VLA specification is that the LO system phase error should be no greater than 1 degree/GHz of the observing frequency. F12 is the X-Band Local Oscillator (8.4 GHz).

Since the YIG and driving circuitry are a VCO, the phase error induced by perturbations is a concern. 120 Hz power supply ripple is probably the most dominant perturbation. If the YIG were not controlled by a phase-locked loop, the phase error induced by power supply (and other) perturbations would be excessive.

A specification of 1 degree was used in the design of the L6 phase-locked loop. Estimating the 120 Hz ripple of the +15 power supply to be 15 mV (0.1%) and using Thompson's model [3], W_N may be calculated using a P_E of 1 degree (pi/180) in the following formula from Gardner.

$$P_E = D_w W_m / (W_N)^2$$

W_m is 120 Hz (754 rad/sec). $D_w = K_O$ x 0.015 V and is 0.834 x 10^6 rad/sec. Using pi/180 as the phase specification in this equation, W_N is found to be 3.59 x 10^5 rad/sec (F_N = 114 kHz) which is a bit higher than the 76 kHz chosen. This estimate is perhaps unduly pessimistic but does illustrate the loop bandwidth concern. Careful spectral analysis of the F12 LO signal shows no discernable phase error. For comparison, an F_N of 140 kHz was chosen for the L104 which is the VLBA 2 - 16 GHz Synthesizer. [4]

F12 has RFI feedthrough filters on the +5 and 15 volt power to reduce high-frequency noise on these lines.

Phase Locked Loop Configuration

Figure 7 (next page) is a block diagram of the YIG phase-locked loop. The YIG Tuning control circuits (described in Section 2.2) have been been included for completeness.

The loop contains several RF components (amplifiers, isolator, directional couplers and attenuators) which are vital but essentially transparent elements in the loop performance. These components establish the proper RF operating conditions for the phase-locked loop. For example: the two amplifiers (WJ A77-1 and Aydin-Vector AY-5037-4) raise the 600 MHz and 200 MHz signals to the levels required by the mixers in the Harmonic Mixer and 200 MHz Phase Detector. The Midwest 263 attenuator isolates the Harmonic Mixer from cable and connector reflections on the line to the Triangle Microwave directional coupler that samples the YIG output.

The 200 MHz and 600 MHz bandpass filters are important to the operation of the phase-locked loop. Since the loop operates upon the frequency and phase relationships between the 200 MHz LO reference signal and the 200 MHz IF output of the Harmonic Mixer, it is desirable to remove signals that could obscure the operation of the control loop.

The 600 MHz K&L bandpass filter in the 600 MHz reference signal line remove other (B-Rack)

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[3] VLA Technical Report No. 8, page 5-2

[4] VLBA Technical Report No. 4, page 15

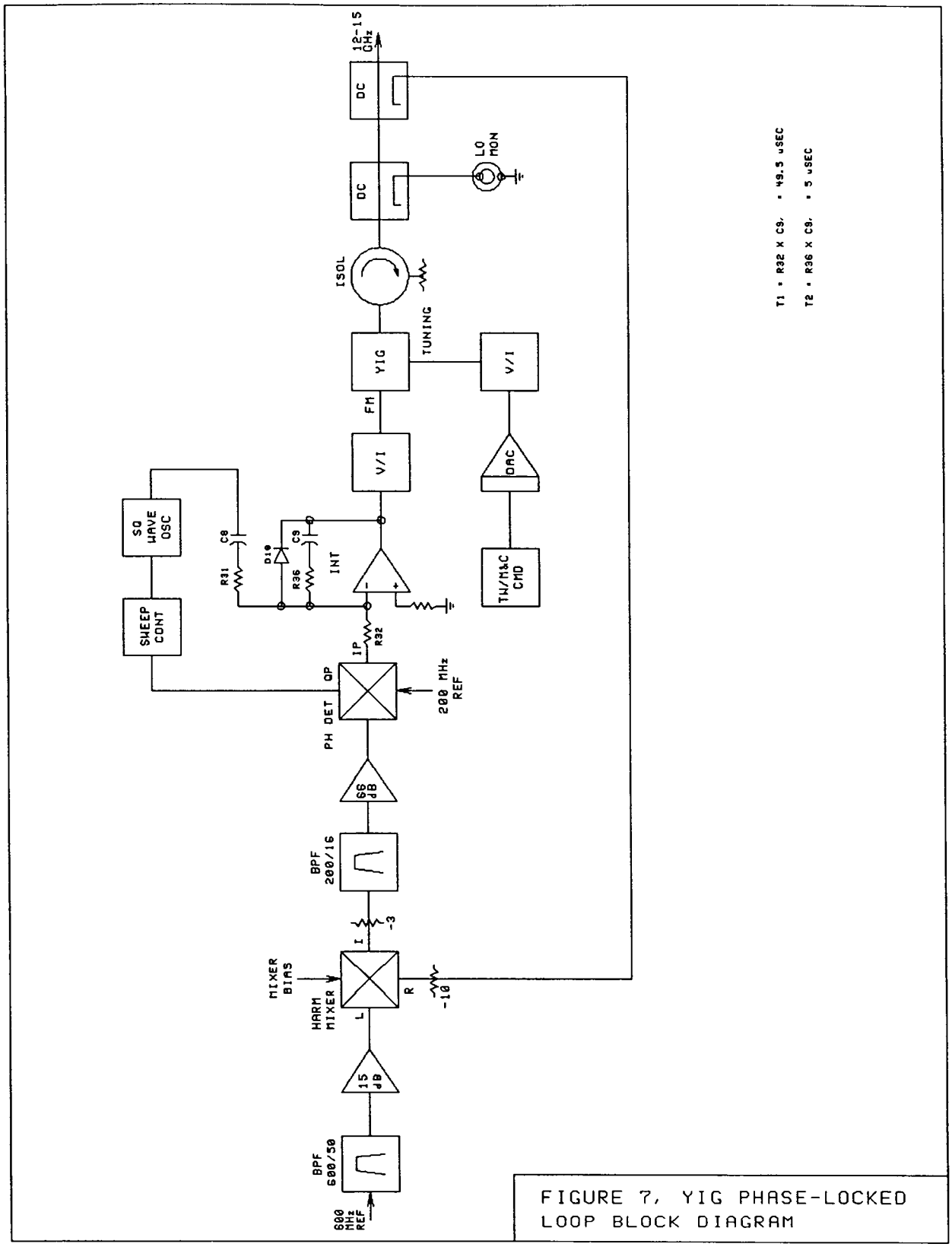


FIGURE 7, YIG PHASE-LOCKED LOOP BLOCK DIAGRAM

LO signals which are present on the 600 MHz line at residual levels. A notable example is 50 MHz which is extensively used in the B-Rack. The presence of these other signals (e.g. 50 MHz) on the Harmonic Mixer's RF port would complicate the Harmonic Mixer's IF spectrum and add 200 MHz components which are unrelated to the operation of the 200 MHz phase-locked loop.

The K&L 200/16 bandpass filter is used to filter the 200 MHz output of the Harmonic Mixer. The Harmonic Mixer mixes the YIG output with the 600 MHz reference signal; this generates an IF which may have a number of complex sum and difference terms, **one** of which is the 200 MHz signal. Since the phase-locked loop operates upon the phase relationship between this 200 MHz signal and the LO system 200 MHz reference signal, it is important that the Harmonic Mixer's 200 MHz output be filtered to remove these other unwanted signals before it is input to the 200 MHz Phase Detector.

A Triangle Microwave CA-912 Directional Coupler on the YIG output line picks off a low level signal (-20 dB below the line level) for input to the RF port of the Harmonic Mixer. A second CA-912 DC picks of a sample which is connected to the front panel LO MON connector. The isolation provided by these directional couplers minimizes the effect of cable and connector reflections between the YIG and the mixer and connector.

These RF components are described in Section 2.10 and their data sheets are included in Section 5.

2.6 X-BAND RF TO IF FREQUENCY CONVERSION

This section describes the second function of F12, which is the conversion of the two RF (A/B and C/D) signals from the X-Band Front End Receiver to two (A/B and C/D) IF signals that are routed to the F9 module for further amplification and conversion to the A, B, C and D IF signals.

The Local Oscillator is the YIG Oscillator that (with its frequency control circuitry) was described above. The YIG oscillator tunes over the range of 11.8 to 15.2 GHz and has an output power of +13 dbm. The power splitter separates the LO signal into two +10 dbm signals that drive the LO port on the mixers. The RF inputs from the Front End covers an 8.0 to 8.8 GHz band and have a power level of -47 dbm/GHz. The IF outputs are two 4.5 to 5.0 GHz signals (A/B and C/D) at a power level of -57 dbm/GHz.

A 16 GHz low-pass filter is shown on the Module Wiring Diagram (D13165S09). This filter was not used in the production versions of F12.

The mixer components are the following commercial modules:

A Passive Microwave PTB2007 isolator that minimizes reflections from the mixer back into the YIG. The Module Wiring Diagram shows a PTB 1091 isolator on the YIG output; the PTB 2007 is actually used because it has a more convenient connector configuration than the PTB 1091.

A Triangle Microwave YL-2133 two-way power divider that provides two isolated LO signals to the mixers. The YL-2133 splits the LO signal into two +10 dbm signals that drive the two mixers (W-J M88C). The YL-2133 has excellent amplitude and phase balance; both are important considerations in the VLA system which must maintain the integrity of two independent RF signal paths.

Two Watkins-Johnson M88C double-balanced mixers that mix the two RF signals with the LO signal to produce two IF signals.

Two Trak 61A6071 isolators that minimize the effect of reflections caused by discontinuities in the cables and connectors between the mixers and the F6 inputs.

Two isolator-bandpass filter combinations (Trak 21A9271 Isolator and Reactel 4CO-8400-1000-S12, 8.4 GHz bandpass filter) that reject out-of-band outputs of the broadband Front End and minimize the effect of reflections caused by discontinuities in the cables and connectors.

Section 5 has data sheets for these components and Section 2.10 describes their important characteristics.

The configuration of these components is depicted in the Module Wiring Diagram (D13165S09). Figure 1 provides a photographic view of the RF side of the module. Note that the mixer components occupy a major portion of the F12 RF space.

Important considerations in frequency conversion are isolation, conversion loss, VSWR, the noise content of the mixer output, compression, and rejection of out-of-band signals.

Isolation

Isolation is a measure of the circuit balance within a mixer. When the isolation is high, the amount of "leakage" or "feed through" between the mixer ports will be small. The Isolation vs Frequency

charts on page 558 of the M88C data sheet show that at an LO level of +13 dbm, an RF of 8 GHz and an IF of 5 GHz, the LO to IF isolation is about 37 dB and the LO to RF isolation is about 23 dB. The RF to IF isolation is not plotted for an IF of 5 GHz but is typically about 23 dB.

In Section 2.1, the YIG Pulling Figure was described and is a measure of the influence of output mismatches upon the YIG frequency. The AV-71251 has a Pulling Figure of 5MHz for a return loss of 12 dB (a VSWR of 1.7:1). The PTB-2007 isolator has a max VSWR of 1.15:1 and an isolation of 23 dB which protects the YIG from cable and connector mismatches.

Conversion Loss

A mixer's conversion loss is the ratio of the mixer's IF power (in an upper or lower sidebnd) to RF input power and is normally expressed in dB.

The Watkins-Johnson M88C mixer is a double-balanced mixer and page 557 of the data sheets shows that the typical conversion loss is about 7.5 dB and the max is 10.0 dB. Page 559 of the data sheet shows plots of conversion loss versus LO power for four combinations of LO and RF frequencies. The third plot (down) shows that conversion loss is essentially constant for LO levels above 10 dbm.

A manufacturer's test data sheet (in Section 5) shows a Conversion Loss is typically of about 7 dB for IF's of 4 to 6 GHz.

VSWR

Page 559 of the M88C data sheet shows that with an RF of 8 GHz and an IF of 5 GHz, the RF port VSWR is about 1.5:1. Page 560 shows that the LO port VSWR is about 2:1 for an LO level of +13 dbm and a frequency of about 13 GHz.

Intermodulation

Ideal mixers generate only the desired IF output of F_{LO} +/- F_{RF}. Practical diode mixers generate harmonics of the LO and RF input signals which mix and cause the harmonic modulation products NF_{RF} +/- MF_{LO} in the output frequency spectrum.

The double-balanced mixer (DBM) is a circuit that theoretically has only the sum and difference signals to the output. Practical double-balanced mixers have a 20 to 30 dB suppression of internally generated, even-order harmonic products compared to a single diode mixer.

Page 558 of the M88C data sheet shows that the intermodulation product levels for low-order combinations of RF and LO frequencies are more than 45 dB below the 1 x 1 product level. This data is for an LO of 18 GHz at a level of +13 dbm and an RF of 10.1 GHz.

Noise

Noise Figure is a measure of the noise content of a device's output. For a mixer, the Noise Figure is the ratio (in dB) of the signal-to-noise ratio at the mixer's RF input divided by the signal-to-noise ratio of one mixer IF sideband output.

Page 557 of the M88C data sheets shows that the mixer's typical Noise Figure (NF) is 8.0 dB and the maximum is 10.5 dB for an RF of 10 to 18 GHz and an LO of 10 to 18 GHz.

Compression

The M88C data sheet cites a 1 dB compression specification for an RF level of +7 dbm and an LO level of +13 dbm. Compression is a measure of a Double-Balanced Mixer's dynamic range. In a DBM, as the RF level is increased, the IF output should correspondingly increase in a linear manner. At some point, IF outputs begin to depart from this linear behavior; further increases in RF input produce smaller increases in IF output and eventually the IF output becomes fairly constant. Additional increases in RF input do not produce additional IF output. The 1 dB compression point is where the IF output cannot linearly follow the input RF and deviates from linearity by 1 dB.

In the F12 mixer, LO power is about +10 dbm but RF power is about -47 dbm/GHz so the mixer is operating far below the RF +7 dbm compression point.

Out-of-Band Signal Rejection

In the F12, out-of-Band signals from the Front-Ends are rejected by the 8.4 GHz Reactel 4CO-8400-1000-S12 Bandpass filters.

The M88C mixer's outputs contain RF and LO sum and difference signals. The difference signal (a band covering 4.5 to 5.0 GHz) is the signal used by the LO system for amplification and further frequency processing. The sum signal (about 21 GHz) is present in the mixer's outputs but are rejected by the 4750 GHz (4750/795) bandpass filter in F4.

2.7 F12 SIGNAL LEVELS AND SPECTRUMS

This section lists F12 signal levels. A photograph of the typical YIG spectrum at the front panel LO MON connector is shown below.

Reference Signal Inputs

The level of the 200 MHz Reference Signal at J10 is +10 dbm.

The level of the 600 MHz Reference Signal at J9 is -3 dbm.

RF to IF Mixer

The level of the LO input to the (M88C) mixer is +13 dbm.

The levels of the X-band Front-End outputs at J11 and J12 are -47 dbm/GHz.

The levels of the (M88C) Mixer outputs at J7 and J8 are -57 dbm/GHz.

Harmonic Mixer

The level of the RF input to the Harmonic Mixer is -14 dbm.

The level of the 200 MHz IF output of the Harmonic Mixer is - 50 to -60 dbm.

The level of the RF input (YIG LO signal) to the Harmonic Mixer is -14 dbm.

200 MHz Phase Detector

The 200 MHz level at the IF input is +3 dbm.

The 200 MHz level at the LO input is +10 dbm.

The level of the In-Phase and Quad-Phase outputs of the 200 MHz Phase Detector is 250 mV.

The MCL PSCQ-2-250 Quad Power Splitter output level is +7 dbm.

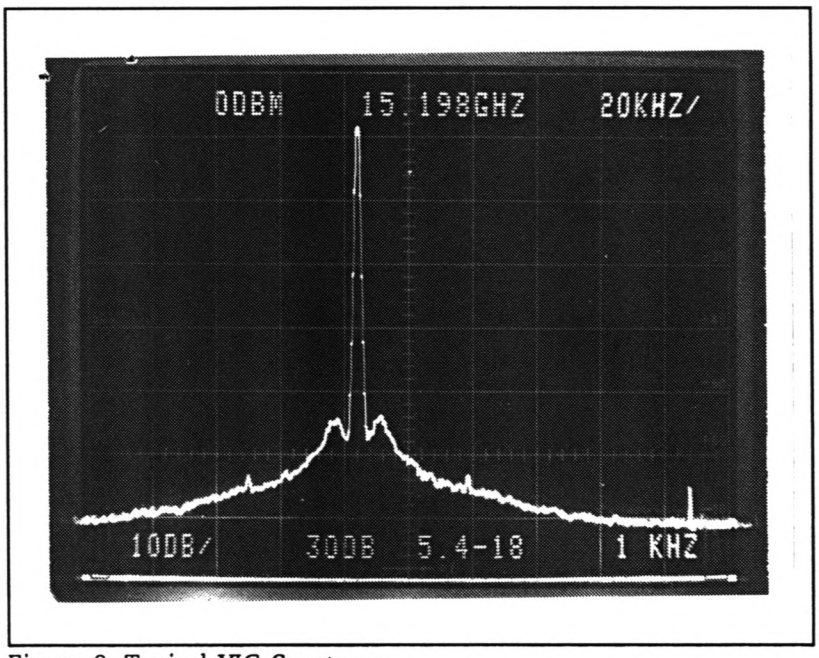


Figure 8, Typical YIG Spectrum

2.8 FRONT PANEL LED DISPLAY BOARD

This section describes the operation of the front panel display circuitry that is contained on board "A3". This board contains an alphanumeric display of the commanded YIG frequency and a bar-graph display that indicates the level of bipolar analog signals. A center-off, momentary-action, front panel switch selects either the CONT VOLT (YIG FM coil drive voltage) or the IF LEV (YIG output) level for the bargraph display. The L LOCK and H LOCK display LED's are also installed on this board.

The YIG frequency display shows the YIG frequency command selected by the command select multiplexer on "A2", the digital control board. When the front panel mode switch is in the AUTO position, the display shows the Data Set frequency command from the central control computers. When the switch is in the MAN position, the display shows the Thumbwheel switch frequency command.

The YIG frequency display uses three Hewlett-Packard 5082-7300 numeric BCD-code LED display chips with an internal decoder/driver and memory. The display chips show digits 0 through 9 plus a right-hand decimal point. The BCD input lines are high-true TTL levels. The state on the four inputs is loaded into the chip memory by dropping pin 5 to ground and then raising it high. If pin 5 is held low, the four input states drive the display decoder to indicate the input state. Pin 5 is hard-wired low on this diplay board so the display continuously reflects the BCD command value.

The ten's digit is hardwired to show the "1" digit; this digit is not commanded and is implicit in the command argument. The decimal point input on the units digit is hard-wired to logic ground to illuminate this LED. The units digit is driven by the command argument units nibble (MSD) and the tenth's digit is driven by the command argument tenth's nibble (LSD).

The bargraph display uses two National Semiconductor LM3914 Dot/Bar Display Driver chips connected to drive two side-by side, 10-element Bar Graph LED array chips (Hewlett-Packard HDSP-4820). The display forms a twenty-state bargraph that indicates the level of the selected bipolar analog signal.

A data sheet for the LM3914 driver chip is contained in Section 5.

Figure 9 shows a simplified block diagram of the LM3914. This device has ten analog comparators to perform parallel comparisons of the input analog signal with taps on a ten-element voltage divider powered by an internal +1.25 reference supply connected to the top of the voltage divider (R_{HI}). The low (-, Ref Adj) side of the supply is connected to ground. When the analog signal is more positive than a tap point, the associated comparator output will switch low and sink current from an external LED. Comparators with tap voltages less than the input signal will power LED's; those that exceed the signal will not. If the LED's are a linear array as is the case in the F12 display, the display is a bargraph representation of the analog signal with 125 mV increments. This simple configuration provides a bargraph for an input signal ranging from 0.0 to +1.25 volts.

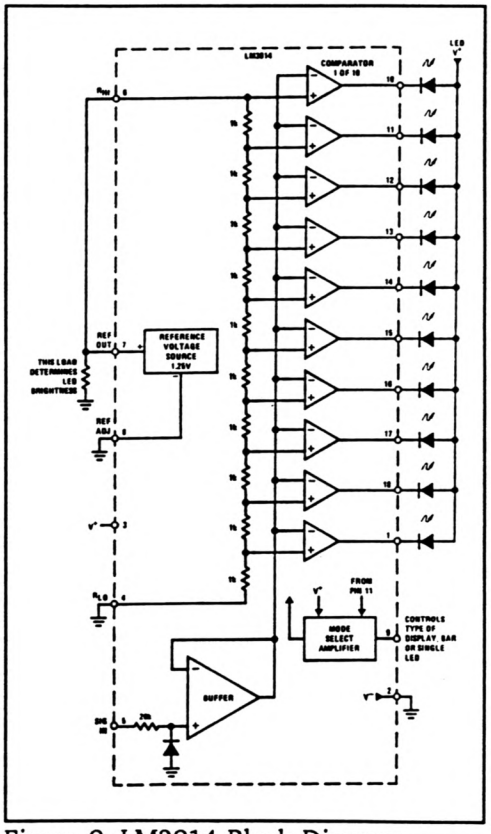


Figure 9, LM3914 Block Diagram

A voltage-follower buffers the input signal to provide a high input impedance.

A second 3914 may be added to provide a 20-element bipolar display of an analog signal level ranging from -1.25 to + 1.25 volts. This is the configuration used in the F12 display. The display driver chips are connected to power the LED's in a left-to-right right manner; as the signal increases positively, LED's will be incrementally illuminated in a right-ward direction. If the signal is more negative than -1.25 volts, none of the LED's will be powered. If the signal is slightly more positive than -1.25 volts, the left-most LED will be powered. If the signal is more positive than -1.125 volts, the two left-most LED's will be powered, etc. If the signal is more positive than +1.25 volts, all LED's will be powered.

Drawing B13165S04 shows the bargraph display circuitry. Data Sheet page 9-170 shows this configuration. Note that a voltage divider reduces the signal level by 0.247. An LM337T voltage regulator provides a -1.3 volt reference level which is connected to R_{LO}, Ref Adj and to R_{HI} and Ref Out through a 750 Ohm resistor. These connections translate the top of the voltage divider to ground potential and the bottom to -1.3 volts. Potentiometer R12 is used to adjust the regulator to a -1.3 volt output.

The negative voltage LED drivers sink current through a resistor to +5 V; this steals current from the LED's because the driver output levels are below the LED's minimum forward voltage. When the outputs rise, the associated LED's are powered by +5 volts through the current-limiting resistors. The positive voltage LED current is controlled by R16. The LM3914 data sheet describes this current control scheme.

The "A3" BOM is included in Section 4.

2.9 "A2" MONITOR AND CONTROL BOARD

Data Set Interface

This section describes the operation of the "A2" board which interfaces the F12 circuitry to the Data Set.

All F12 monitor data operations are a response to monitor data message stimulus signals from the Data Set. In **both** the AUTO and MAN modes, the Data Set command stimulus signals can store a frequency command value in the "A2" Command Storage Register. In the AUTO mode, the YIG frequency is determined by this value. In the MAN mode, the YIG frequency is determined by the setting of the front panel Thumbwheel switches but the Command Storage Register value is not altered. When the AUTO/MAN switch is returned to AUTO, YIG frequency control will revert to the state stored in the Command Storage Register.

The Data Set interface signals are described first since they control the operation of the "A2" board.

Multiplex Address

The Multiplex Address is conveyed by the state of four (SMA-0, ... SMA-3), low-true, TTL logic signals having binary weights of 2^0 through 2^3. These lines permit sixteen command and data addresses to be decoded; one command and two monitor enables are decoded by the "A2" board logic. SMA-0, .. SMA-3 are the lower portion of the eight-bit address byte of Data Set command and data messages. The Data Set decodes the upper four bits to select a Data Set digital output or input to/from a device controlled by the Data Set.

The SMA-0, ... SMA-3 lines also control the channel selection logic of the "A2" analog multiplexers.

Between command or data operations, the Multiplex Address lines are quiescent high (logic "0" state).

Two low-true enables (EN0 and EN1) from decoder L21 are used by the command and digital monitor logic. EN0 is used to enable commands (address 320_8) to be loaded into the Command Register and to enable the Command Echo data (address 220_8) to be read out to the Data Set. EN1 (address 221_8) is used to enable digital monitor data to be read out to the Data Set.

Digital Command Output, DIGI-0

The Data Set digital command output used by F12 is DIGO-0, which consists of three low-true lines: DIGO-0, CLKO-0 and STRO-0. The DIGO-0 signal is a serial data line, clocked into an F12 serial input command register by CLKO-0. After 24 shift clocks, the data is parallel-loaded into a static storage register by the STRO-0 signal. In the interval between command messages directed to DIGO-0, the Data Sets sets the DIGO-0 lines high. DIGO-0 addresses are 320_8 - 337_8.

Digital Monitor Data Input, DIGI-1

The Data Set digital monitor data input used by F12 is DIGI-1, which consists of three low-true lines: DIGI-1, CLKI-1 and STRI-1. The STRI-1 signal parallel-loads an F12 monitor register. The DIGI-1 signal is a serial data line, the output of a serial monitor data register. The DIGI-1 line is clocked into the Data Set monitor register by CLKI. In the interval between monitor messages evoked from DIGI-1, the Data Set sets the DIGI-1 lines high. DIGI-1 addresses are 220_8 - 237_8.

Analog Monitor Inputs, ALGI-2

F12 analog data is connected to the Data Set ALGI-2 analog multiplexer input. The associated addresses range from 40_8 through 57_8.

The Data Set analog multiplexer is a differential multiplexer and accepts differential or single-ended signals from up to eight sources. The multiplexer has a common-mode noise rejection ratio > 80 db. Input impedance is greater than 10^{10} ohms. Settling time to less than one bit error is less than 18 microseconds but the Data Set provides 30 microseconds of settling time. 30 microseconds after the start of an analog to digital conversion sequence, the Analog to Digital converter sample/hold is set to the hold mode and the conversion sequence is started.

Analog inputs from single-ended sources **must** have a low (-) signal return line connected to analog common at the signal source. Since the Data Set is a differential multiplexer, the low signal returns from different devices are isolated from each other and common-mode noise rejection is not reduced.

Command and Monitor Enable Decode Logic (Sheet 1)

The four (low-true) Mux address bits (SMA0- through SMA3-) are inverted to high-true format by open-collector buffer C01. The buffer output levels swing between 0 and +5 volts. A 7406 buffer and pull-up resistors are used in place of a simple inverter in the event that it becomes necessary to use analog multiplexer chips with overvoltage protection (typically an HI 508A). These multiplexers require a logic 1 greater than 4.0 volts.

The Command and Digital Monitor enables are decoded by a 1-of-eight decoder L21, a 74LS138. (See a TTL data book for details on the operation of the 74LS138.) The low-true EN0 and EN1 outputs are decodes of mux addresses 00_8 and 01_8, respectively.

Enable EN0 permits the CLKO-0 clock to load the DIGO-0 command data into the Command Storage Register as described below.

Enables EN0 and EN1 permit the CLKI-1 clock to unload the Command Echo and Monitor Data registers to the Data Set DIGI-1 input as described below.

The Command Echo address 220_8 is 100_8 less than the command address 320_8. This assignment is for convenience in remembering the Command Echo address.

The Data Set Command format is shown below.

Data Set Command Format

	LSD																MSD							
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Funct	CB0	CB1	CB1	CB3	CB4	CB5	CB6	CB7	SB0	SB1	SB2	SB3	SB4	SB5	SB6	SB7	NU	NU	NU	NU	NU	NU	NU	NU
Weight	.1	.2	.4	.8	1	2	4	8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

CB0, CB1, etc. are Command Bits 0, 1, etc. SB0, etc. denotes spare, unassigned command bits. NU denotes unused command bits. - denotes that the bit has no weighted value.

Command Register Logic

The command register logic consists of two serial-in parallel-out shift registers and two parallel-input storage registers. Three sets of gates, enabled by EN0 (described above), load the registers under control of the Data Set DIGO-0 lines. Two 74LS02 low-true AND-gates (C9-10 and C9-4) enable the low-true serial data (DIGO-0) and the low-true clock (CLKO-0) to serially shift the 24 command argument bits into 74LS164's E41 and E49. The DIGO-0 state on the A-B inputs and the contents of the 74LS164's are shifted to the right on the rising (trailing) edge of the register clock. The command MSD shifts completely through the register and is not used.

5 microseconds after the serial loading has been completed, the trailing edge of the 5 microsecond low-true strobe STRO-0 parallel-loads the 16-bit contents of the serial register (E41 and E49) into the static storage registers E30 and E19. Figure 10 (next page), depicts the digital command timing operations.

Command Select Multiplexer

Two quad, 2:1 parallel multiplexers (E10 and E01, 74LS157's) select either the Command Storage Register value or the Thumbwheel command value for control of the F12 Tuning Coil current.

When the Select input to these multiplexers is low, the 1A, 2A, 3A and 4A inputs (Command Register bits) are selected for output to the 1Y, 2Y, 3Y and 4Y outputs. A high on the Select input selects the B1, B2, B3 and B4 (Thumbwheel switch) inputs. The front panel AUTO/MAN switch provides a logic ground to the 74LS157's Sel inputs (pin 1) when the switch is in the AUTO position. The multiplexer STRB (strobe) input is tied to logic ground to continuously enable the multiplexers. The state of the Command Select Multiplexer output is read back to the control computers on the MSD of the Command Echo data. The Command Echo format is described below.

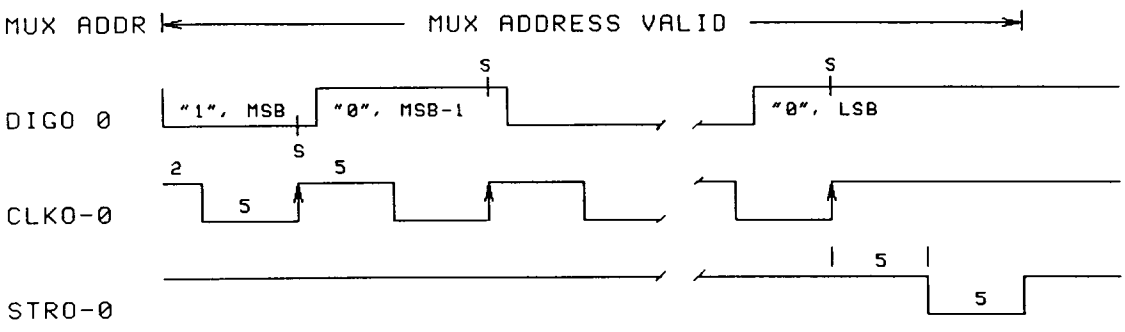
Digital Monitor Logic

Two types of Digital Data are read from the "A2" board by the Data Set, Command Echo and Digital Monitor data.

The lowest two bytes of the Command Echo are readouts of the contents of the command storage registers, E10 and E01 (E01's contents are spare command bits). The upper byte (MSB) is the output of the Command Select Multiplexer described above. This byte reflects the actual command applied to the YIG Tuning coil circuit and will be either the (Data Set) Command Register or Thumbwheel Switch value, depending upon the state of the AUTO/MAN switch. The Command Echo readout provides a confirmation to the central control computers that the command issued by the control computers is correctly loaded into the command register.

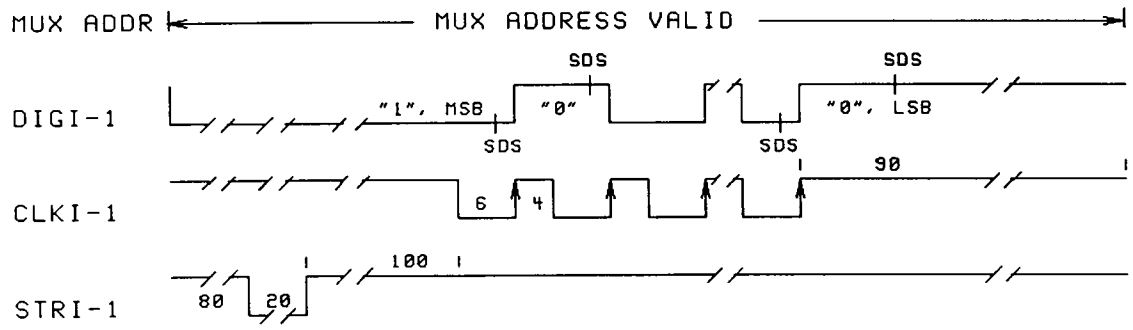
Digital Monitor Data is read out of the F12 to indicate the status of the Phase Lock loop and the state of the AUTO/MAN switch. This data is indicated by three discretes: LOW LOCK WARN, HIGH LOCK WARN and A/M (the state of front panel AUTO/MAN switch). The balance of the digital monitor bits are available for future use but at present are not used.

DIGO-0 TIMING



NOTE: S DENOTES F12 SAMPLING POINT

DIGI-1 TIMING



NOTE: SDS DENOTES DATA SET SAMPLING POINT

NOTES:
1 SIGNALS SHOWN AT INPUT TO F12 LOGIC
2 TIME IN MICROSECONDS
3 UP ARROWS DENOTE CLOCKING EDGE

FIGURE 10, DIGO-0 AND DIGI-1 TIMING

The Data Set Digital Monitor Data and Command Echo formats are shown below.

Data Set Digital Monitor Data Format

	LSD																MSD							
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Funct	M0	M1	M2	M3	M4	M5	M6	M7	M10	M11	M12	M13	M14	M15	M16	M17	M20	M21	M22	M23	M24	LLW	HLW	A/M
Weight	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DM	DM	DM

M0, M1, etc., are spare Monitor Data Bits 0, 1, ... 24, not assigned to any functions.
DM denotes discrete monitor bits as follows: LLW = Low Lock Warn, 1 = Warn, HLW denotes High Lock Warn, 1 = Warn, A/M denotes AUTO/MAN switch mode, 1 = Manual mode.

Command Echo Monitor Data Format

	LSD																MSD							
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Funct	CB0	CB1	CB1	CB3	CB4	CB5	CB6	CB7	SB0	SB1	SB2	SB3	SB4	SB5	SB6	SB7	CS0	CS1	CS1	CS3	CS4	CS5	CS6	CS7
Weight	.1	.2	.4	.8	1	2	4	8	-	-	-	-	-	-	-	-	.1	.2	.4	.8	1	2	4	8

CB0, CB1, etc. are Data Set Command Bits 0, 1, etc. SB0, etc. denotes spare command bits, no assigned function. CS0, CS1, etc. denotes the Command Select Multiplexer output bits.

The Command Echo and Digital Monitor data readout logic are identical except for the enables; Command Echo is enabled by EN0 and Digital Monitor data is enabled by EN1.

The monitor data readout logic is similar to the digital command logic - a set of three serial shift registers. Three parallel-input, serial-output shift registers (74LS165's) are parallel-loaded and serially unloaded to the Data Set under control of the Data Set DIGI-0 input lines. Three gates, enabled by EN0 or EN1, permit the low-true STRI-1, DIGI-1 and CLKI-1 signals to read the selected digital data. If enabled by EN0 (or EN1), Gate C17-1 (or C17-13) impresses the 20 microsecond STRI-1 strobe on either of the two sets of 74LS165 Shift/Load (S/L) inputs. This loads the register with the state on the three register's A through H inputs. 100 microseconds after the rise of STRI-1, the CLKI-1 shift clocks on gate C9-13 (or C17-4) start the serial unload of the 24 monitor data bits in the register to the Data Set DIGI-1 input via gate C49-3 (or C49-6).

Since 21 of the 24 bits of the Digital Monitor data register (L12, J12 and G12, Mux 221_8) are not tied to ground or to a pull-up resistor, they may be either a high or low, but will probably be read out as 1's.

Figure 10 (previous page) shows the timing of the digital monitor data logic.

The DIGI line is driven by open-collector buffers (7406's) that are driven by gates C49-6 or C49-3) which are enabled by EN0 or EN1. The buffer pull-up resistor is in the Data Set and all the other monitor data sources (e.g. F-Rack F14's) on the DIGI-1 line sink current through this resistor as they input digital monitor data to the Data Set. The 74LS165 Clock Inhibit inputs are tied to logic ground which permits the shift clocks to unload the register. The LSB serial inputs L3-10 and L12-10 are connected to ground so that the registers fill with zero's during unload. This would not be a problem as the shift register is always parallel-loaded by STRI-1 at the start of a new shift sequence.

If the CLKI-1 signal is viewed on an oscilloscope, a curious feature will be seen: there are two pauses in the clock train. These have a duration of one bit period and occur after eight shift clocks. This pause is an artifact of the Data Set monitor shift logic. The monitor data is not stored in a register in the Data Set. The serial stream of data from the F14 is merged directly into the Data Set's message output logic. The pause is used to inject the Data Set's serial parity bit into the message data stream.

A natural question is: is there a possibility of time contention between Data Set command and monitor operations which could obscure the readout of the command echo monitor data? The answer is "no"; the Data Set command and monitor operations are widely separated in time so there is no possibility of conflict.

Analog Signal Multiplexing and Conditioning (Sheet 2)

The "A2" board has sixteen channels of analog signal conditioning and multiplexing that are read out as analog monitor data by the Data Set. This data is indicative of the performance of the F12 module. The following is a description of the signal conditioning and multiplexing. The analog signals are tabulated at the end of this section.

The Data Set uses a dual-stage analog multiplexing scheme; an 8-input Data Set analog multiplexer selects analog data from up to 8 analog multiplexers in modules such as F12. The upper four (of 8) address bits enable one of the eight Data Set analog multiplexer inputs and the SMA-0, ... SMA-3 lines control the selection logic of the "A2" analog multiplexers.

Analog Signal Conditioning

Each analog multiplexer channel has an RC filter that provides charge-transfer isolation to reduce perturbations to signal sources during sampling. The multiplexer chips (HI-508's) have break-before-make properties but circuit wiring and chip capacitances (although small) can retain charges between actuation of the multiplexer channels. The Data Set defaults the four multiplex address lines to address 15_{10} (Hex F) between command or monitor operations; the stored charge associated with this address state is the charge that exists on this capacitance when an analog signal is selected. The 0.1 uF capacitors in the RC filter will be charged to the signal source voltage; this capacitor must charge the multiplexer-wiring capacitances. The worst-case scenario would be to assume that a channel filter capacitor is charged to +10 volts and the multiplexer default address (F_{16}) had selected a -7.5 volts source; the worst case signal swing on a multiplexer output is thus 17.5 volts. Estimating 50 pF for the HI-508 chip and wiring capacitances and using a Data Set multiplexer "on" capacitance of 100 pF, the filter capacitor charge is reduced by about 2.5 mV, about a 1/2 count error in the converted value. This (worst case) 2.5 mV charge must be replaced by the signal source through the 1000 ohm filter resistor. The charge time constant is about 50 ns so the output, wiring and Data Set input capacitance is charged within about 1 uS. The Data Set A/D shifts to the "Hold" mode 30 us after the multiplex address goes true; thus there is more than adequate time for analog settling before A/D conversion is initiated.

It is particularly important to protect the YIG frequency control circuitry from multiplexer charge-transfer perturbations.

Voltages greater than 10 volts are divided by a resistive divider across the filter capacitor. These are 15 and 28 volt power supply voltages.

Clamping diodes on the HI-508 inputs and outputs clamp over-range inputs or outputs to the +15V or -15V chip inputs. Chip damage under these conditions is unlikely because the 1000 ohms (or 5110) ohm resistors in the RC filter circuits will limit "On" channel current to less than the 20 mA limit.

Analog Signal Multiplexing

The "A2" board has two 8-channel, single-ended, analog multiplexer chips which sample sixteen F12 analog signals. One multiplexer chip selects one of the lower eight signals and the second selects one of the upper eight signals. The multiplexer chips have internal one-of-eight decoders which drive the analog switches. The decoder has an enable input which permits the decoder outputs to drive the analog switches. The three lower Multiplex Address bits SMA-0, SMA-1 and SMA-2, respectively activate (via the one-of-eight decoder) one of the channels on each multiplexer and the most significant bit SMA-3, enables either the lower or upper multiplexer decoder as a function of the logic level. The two multiplexer outputs are tied together and drive the + (signal high) input of the Data Set multiplexer.

The negative (signal low) input to the Data Set multiplexer is connected to the F12 +/- 15 V Common. Since the Data Set is located in another slot, there is probably a small common-mode difference between the F12 and Data Set analog common. Since the Data Set analog inputs are differential and have a high common-mode rejection (about 80 db), the use of the F12 analog common signal for the signal low input to the Data Set multiplexer has a negligable effect upon the converted values. An HI-508 data sheet is included in Section 5.

10 Volt Reference

A precision +10 volt reference on the "A2" board provides a means of checking the Data Set A/D converter gain drift. The Harris HA1608 +10 volt reference and trim circuitry are installed on dip header L48. The +10 volt output is connected to the Channel 2 input of multiplexer L30. Analog ground is connected to channel 1 of L30. The signal levels read via these two channels provide a means of checking the Data Set A/D converter gain and zero drifts.

F12 Analog Signals

Mux Address$_8$	Function	Normal Value	Data Range
40	Analog Gnd.	0.000 Volts	+/- 20 mV
41	+10 Volt Ref.	+10.000	+/- 20 mV
42	+5 Volt PS	+5.000	+/- 100 mV
43	+15 Volt PS (+15/2)	+7.500 Volts	+/- 200 mV
44	-15 Volt PS (-15/2)	-7.500 Volts	+/- 200 mV
45	+28 Volt PS (+28/4)	+7.000 Volts	+/- 400 mV
46	Not used, Gnd.	0.000 Volts	
47	IF Level	+/- 3 Volts	+/- 1 to +/- 5 Volts
50	YIG Tuning Voltage	-3 to - 4 Volts	
51	FM Coil Control Voltage	+ 5 Volts	0 to +10 Volts
52	Phase detector In-Phase	0.0 Volts	+/- 20 mV
53	YIG Tuning Current (V/5)	-3 to -4 Volts	
54	Spare		
55	Spare		
56	Spare		
57	Spare		

Two data overlay print-outs (next page) show typical F12 analog and digital values. The TST overlay shows IF level, YIG Tuning Voltage and current, FM Voltage and 200 MHz Phase Detector In-Phase level.

The Monitor Word 1 DCS=01 DS=4 overlay (next page) shows all analog and digital monitor data from Data Set 4 which controls the F12 and F14 modules. The (decimal) level of the F12 analog data is listed in rows A040 and A050. Unassigned multiplexer channels are not printed. Rows D220 are Hexadecimal values of the Command Echo (D220) and Monitor data (221).

```
TST SDT ZZZ DB DWR CAL CRYO FEX FRO LOX PA SYSTMP
KILL:<CR> clears the screen and returns to the Menu List.      92.239  19h46m10s
                  JPL X-BAND ANTENNA  1   DCS   5   MODE  XFER  SW      CAL
             A          B          C          D       00040093  OFF        NORM
 CAL         4.04       4.06       3.39       3.37                    AB    CD
 GTP         2.98       2.98       2.98       2.98      BAND SEL.     C  C  C  C
 ALC         2.03       2.22       3.35       3.20      BAND SET.     C     C
 PK.DET.     0.54       0.46       0.66       0.43      FIRST LO  13.0 AUTO LO LOCK
 SYS/CAL.    11.14      11.08      13.27      13.33
                                              VACUUM    10.00      -0.02
                                              DEWAR     17  K      55  K    306  K
 8GHz    GND        +5V        +15V       +28V       -15V       +10V.REF
  FE   -0.70      -1.08      -2.090     -4.820      2.060         -0.93
  LO    0.00       4.96      14.990     27.700    -15.010          9.99
            STAGE 1             OTHER          ______I   NOISE SOURCE   V_____
 AB BIAS      -0.28               -0.80            0.850   NORMAL     -4.520 _
 CD BIAS      -0.31               -0.70            0.400   SOLAR      -4.740 _
         LED VOLTAGE      5.225                 ---------------- LO ------------
 CRITICAL  +15V.    0.600  -15V.      0.610          IF LEVEL         -1.57  _
 CURRENTL  PUMP     0.01 REFRIG.       6.95     TUNING VOLTAGE        -3.52  _
                                              CONTROL VOLTAGE         3.30  _
 K ANTENNA = 1                                 PHASE DETECTOR         -0.00  _
                                                  YIG CURRENT        -0.704  _
WORD B = NORM WORD C = MAN                    ---------------------------------

                                                                      00040091

                      MONITOR WORD  1  DCS=05  DS=4
 (A000)
 (A010)
 (A020)
 (A030)
 (A040)       -0.005    9.995    4.960    7.495   -7.505    6.925   -0.005   -1.575
 (A050)       -3.520    3.295   -0.005   -3.520
 (A060)       10.005   -0.020    0.170    0.550    3.060    6.945   -0.280   -0.800
 (A070)       -0.310   -0.700    5.225    0.010    0.015    0.000    0.090    0.045
 (A100)       -0.710   -0.930   -1.185   -1.130   -1.045    1.025   -1.080   -1.205
 (A110)       -1.075   -1.350   -0.330   -0.005   -0.005    0.000    9.880    0.015
 (A120)        0.570    0.700   -0.050    0.170    0.450    3.390    0.535    0.405
 (A130)        0.650    0.090    0.470    0.000    0.000    0.000    0.020    0.015
 (A140)        0.000    9.980   -9.975   -0.020    7.480   -7.475    4.960    6.915
 (A150)        7.525   -7.500   -0.005   -0.160   -0.265    0.000    0.000    0.000
 (A160)
 (A170)
 (D200)     FFFFFF
 (D210)
 (D220)     300030  5FFFFF  666666  000000  050B07  1F3FFF  1F3FFF
 (D230)
 (D240)
 (D250)
 (D260)
 (D270)
```

Figure 11, TST and MW1, DS4 Overlays

2.10 COMMERCIAL RF COMPONENTS

Data Sheets for the commercial RF components used in F12 are included in Section 5. This section summarizes the important characteristics of these components. Internal circuit details are not described; interested readers should refer to the manufacturer's catalogs and application notes.

AVANTEK AV-71251 YIG OSCILLATOR

The Avantek AV-71251 characteristics were described in Section 2.1.

ISOLATORS

Trak PTB2007

The YIG output is isolated by a Passive Microwave PTB2007 Isolator. The PTB2007 isolator is specified to operate over a frequency band of 12.4 to 18.0 GHz and have a minimum isolation of 23 dB. The isolator's maximum insertion loss (loss caused by its loading of the input) is 0.3 dB and the maximum VSWR is 1.15. From Section 2.1 remember that the YIG has a Pulling Figure of 1.0 MHz with a return loss of 12 dB (i.e. a VSWR of 1.7:1). This is the frequency sensitivity of the YIG to mismatches on its output. The 23 dB of isolation and low VSWR provided by the PTB2007 eliminates this perturbation of YIG frequency. PAMTEK's test data sheets for eleven PTB2007's in the Data Sheet Section (5) show input and output VSWR's ranging from 1.06 to 1.15 and an isolation ranging from 24 to 30 dB. NRAO lab tests of eleven PTB2007's (not all units were from the same lot as above) show an isolation > 30 dB and an insertion loss < 0.3 dB.

Trak 21A9271

The 21A9271 Isolator is characterized over a frequency range of 8.0 to 12.4 GHz. This isolator is used between the J11 and J12 inputs from the X-Band receiver and the mixer's RF inputs. The X-Band receiver's outputs cover the 8.0 to 8.8 GHz. The 21A9271 impedance is 50 Ohms. Maximum insertion loss is specified to be 0.5 dB and isolation is specified to be 20 dB, minimum. VSWR is specified to be 1.3:1, maximum. A manufacturer's test data sheet (in Section 5) for 3 units shows an insertion loss of 0.45 dB, an isolation of 21 dB and input and output VSWR's of 1.25:1.

Trak 61A6071

The 61A6071 Isolator is characterized over a frequency range of 4.0 to 8.0 GHz. The 61A6071 impedance is 50 Ohms. Maximum insertion loss is specified to be 0.5 dB and isolation is specified to be 18 dB, minimum. VSWR is specified to be 1.3:1, maximum. A manufacturer's test data sheet (in Section 5) for 22 units shows an insertion loss of 0.5 dB, an isolation of 18 dB and a VSWR 1.30:1.

POWER DIVIDERS

Triangle YL-2133

The YL-2133 two-way power divider is characterized over the 12.0 to 18.0 GHz frequency range and has excellent amplitude and phase balance - important considerations in the VLA system which must retain the integrity of two independent RF signal paths. The YL-2133 uses stripline construction and the resistive element is a ceramic pad. The YL-2133 impedance is 50 Ohms. The maximum input and output VSWR are specified to be 1.50 and 1.40, respectively. The maximum insertion loss is specified to be 0.6 dB and the minimum isolation is specified to be 20 dB. Phase and amplitude balance are specified to be within +/- 6 degrees and 0.3 dB, respectively.

A YL-2133 manufacturer's test data sheet (in Section 5) for eight YL-2133's shows that these unit's VSWR's were less than 1.5:1, the insertion loss was less than 0.5 dB and the isolation was greater than 19 dB. Amplitude balance was +/- 0.2 dB and the maximum phase unbalance (for one unit) was +/- 5 degrees with an average of +/- 3.6 degrees.

MCL PSC-2-1

The Mini-Circuit PSC-1 is a two-way, 0-degrees power splitter that is used to generate the In-Phase signal in the 200MHz Phase Detector module. The PSC-1 is characterized over a frequency range of 0.1 to 400 MHz. At an input power level of 0 dbm and frequency of 200 MHz, the insertion loss is specified to be 3.3 and 3.1 dB, input to outputs 1 and 2, respectively. The amplitude unbalance (between outputs 1 and 2) is 0.02 dB. Isolation (output to output) is 29 dB. Input VSWR is 1.15:1 and outputs 1 and 2 output VSWR's are each 1.09:1.

In the 200 MHz Phase Detector, the PSC-2-1 input level is +3 dbm.

MCL PSCQ-2-250

The Mini-Circuits PSCQ-2-250 is a two-way, 90 degrees power splitter that is used to generate the Quadrature-Phase signal in the 200 MHz Phase Detector module. The PSCQ-2-250 is characterized over a frequency range of 150 to 250 MHz. At an input power level of 0 dbm and frequency of 200 MHz, the insertion loss is specified to be 2.89 and 3.46, input to outputs 1 and 2, respectively. The amplitude unbalance (between outputs 1 and 2) is 0.57 dB and isolation (output to output) is 38 dB. Output 1-2 phase is 89.60 degrees.

In the 200 MHz Phase Detector, the PSCQ-2-250 input level is +10 dbm and the output levels to the MCL SRA-1 mixers are +7 dbm.

The PSCQ-2-250 is packaged in a small case with projecting pins, suitable for installation on a PC board.

ATTENUATORS

Midwest 263 Attenuator (10 dB)

The Midwest 263 attenuator is characterized for frequencies up to 18 GHz. The attenuation is 10 dB, +/- 0.3 dB. Maximum VSWR is 1.15:1 for frequencies up to 4.0 GHz.

Midwest 294 Attenuator (3 dB)

The Midwest 294 attenuator is characterized for frequencies up to 2.0 GHz. The attenuation is 3 dB, +/- 0.3 dB. Maximum VSWR is 1.15:1 for frequencies up to 2.0 GHz.

AMPLIFIERS

Aydin-Vector AY5037-4

The Aydin-Vector AY5037-4 amplifier is used to amplify the 200 MHz IF signal from the Harmonic Mixer. The amplifier is specified to have a gain between 62 and 70 dB gain at 200 MHz, deliver an output power of +9 dbm and have maximum input and output VSWR's of 1.6:1 and a maximum noise figure of 5 dB.

A typical manufacturer's test data sheet (in Section 5) shows a gain of 67.9 dB and an output power of +10.6 dbm. The input VSWR is 1.17:1 and the output VSWR is 1.60:1. Noise figure is 4.5 dB.

Watkins-Johnson A77-1

The Watkins-Johnson A77-1 amplifier is used to drive the LO input of the Harmonic Mixer. The guaranteed specifications cover operation over a 2 to 700 MHz frequency range. The small signal gain is 16.0 dB, with a gain flatness of +/- 0.3 dB. Power output is rated at +16.5 dbm with 1 dB of compression. Max input and output VSWR is less than 1.5:1.

The A77-1 is packaged in a TO-8 can that is installed on an Avantek TB1 printed circuit board mounted in an Avantek TC2 case.

BANDPASS FILTERS

Reactel 4CO-8400-1000-S12

The Reactel 4CO-8400-1000-S12 filter is used in the RF input paths from the X-Band receivers and is used to reject out-of-band signals from the wide-band receivers.

The Reactel 4CO-8400-1000-S12 bandpass filters are specified to have a center frequency of 8.4 GHz, a bandwidth of 1.0 GHz (at +/- 1 dB response frequencies), and a VSWR less than 1.5:1 over this band. The insertion loss is specified to be 1 dB at the center frequency. The filter's impedance is 50 Ohms.

A manufacturer's test data sheet for twenty-four units shows a +/- 1 dB bandwidth of 7.9 to 8.9 GHz and a VSWR less than 1.5:1 over a bandwidth of 7.93 to 8.84 GHz. Section 5 contains this data sheet and an associated plot of frequency response and VSWR.

K&L 4B120-600/50-OP

The K&L 4B120-600/50-OP Bandpass Filter is used to filter the 600 MHz reference signal from the Local Oscillator system to insure that this signal is free from residual components that might affect the Harmonic Mixer's output spectrum.

The Manufacturer's specifications for this filter are: a center frequency of 600 MHz, a 3 dB bandwidth of 574 to 625 MHz and a VSWR of 1.5:1. Manufacturer's test data for two units show an average bandwidth of 581 to 618 MHz and an insertion loss of 0.85 dB. A Data Sheet and frequency response plot for these two filters are included in the Data Sheet Section (5).

K&L 4B120-200/16-OP

The K&L 4B120-200/16-OP Bandpass Filter is used to filter the 200 MHz output of the Harmonic Mixer. In addition to the 200 MHz IF signal, the Harmonic Mixer may generate a number of complex signals that must be removed by filtering so that the 200 MHz Phase Detector input is only this single mixing product.

The Manufacturer's specifications for this filter are: a center frequency of 200 MHz, a 3 dB bandwidth of 192 to 208 MHz and a VSWR of 1.5:1. Manufacturer's test data for two units show an average bandwidth of 189.5 to 209.5 MHz and an insertion loss of 1.2 dB. A Data Sheet and frequency response plot for these two filters are included in the Data Sheet Section (5).

DIRECTIONAL COUPLERS

MCL PDC-10-1

The Mini-Circuit MCL PDC-10-1 Directional Coupler is used in the 200 MHz Phase Detector module to provide a sample of the 200 MHz signal from the Harmonic Mixer for monitoring on the front panel IF MON connector.

The PDC-10-1 is characterized over a 0.5 to 500 MHz frequency range. Coupling to the CPL output is -11.5 +/- 0.5 dB with a flatness of +/- 0.6 dB. Directivity is 32 dB typical and 25 dB, minimum. Typical VSWR is 1.2. The PDC-10-1 is packaged in an extremely small metal case with pin connections to the phase detector PC board.

In the 200 MHz Phase Detector, the PDC-10-1 input level is +3 dbm.

The PDC-10-1 is packaged in a small case with projecting pins, suitable for installation on a PC board.

Triangle Microwave CA-912

Two Triangle Microwave CA-912 Directional Couplers are used to sample the YIG oscillator outputs to drive the Harmonic Mixer and the front-panel LO MON OSM connector.

CA-912 Directional Couplers are sub-miniature stripline components featuring a high directivity and low VSWR. The impedance is 50 Ohms. The CA-912 is specified to operate over a 12.4 to 18.0 GHz frequency band and has a -20 dB +/- 0.8 dB coupling of the input to the CPL output, a minimum directivity of 15 dB, a maximum VSWR of 1.40:1 and a maximum insertion loss of 0.4 dB.

MIXERS

MCL SRA-1 Double Balanced Mixer

The Mini-Circuits SRA-1 double-balanced mixer is used in the 200 MHz Phase Detector to generate the In-Phase and Quadrature-Phase signals.

The SRA-1 is characterized over a 0.5 to 500 MHz frequency range at an LO input level of up to +7 dbm and an RF input of up to +1 dbm. The conversion loss is 5.5 dB, typical and 7 dB, maximum. The LO-RF isolation is 50 dB, typical and 30 dB, minimum. The LO-IF isolation is 40 dB, typical and 25 db, mimimum. With a 200 MHz RF input at a 4 dbm level, the RF port VSWR is 1.28:1, the LO port VSWR is 1.35:1 and the IF port VSWR is 1.86:1. The maximum DC output is 261 mV with an offset of 0.13 mV.

The SRA-1 is packaged in a small case with projecting pins, suitable for installation on a PC board.

Watkins-Johnson M88-C

The Watkins-Johnson M88C double-balanced mixers are used to convert the two front end RF signals to IF signals using the YIG signal as an LO.

Since the M88C mixers are double-balanced mixers, the RF-LO sum and difference frequencies are the dominant outputs. The RF and LO signals and products of combinations of these two signals are

present at minimal levels. (See the double-balanced-mixer discussion in Section 2.4) The M88C is specified to operate over an IF range of 1 to 8 GHz, an LO up to 18 GHz and an RF up to 18 GHz. The M88C may operate as an up-converter or a down-converter. The YIG 11.8 to 15.2 GHz LO drive to the M88C is a +10 dbm level. The resultant IF signal is a 4.5 to 5.0 GHz signal. Referring to the M88C data sheets for up-conversion under these conditions, the typical conversion loss is 8.0 dB and the max conversion loss is 10.0 dB. The typical noise figure for these conditions is 8.0 dB and the maximum noise figure is 10.5 dB. The minimum LO to RF isolation is 15 dB and the typical is 28 dB. The minimum LO to IF isolation is 16 dB and the typical is 32 dB.

The RF port VSWR is about 2.5:1 and the LO port VSWR ranges from about 2:1 at an LO of 12 GHz to 3.3:1 at an LO of 15 GHz.

At the frequencies cited above, the second harmonic of the LO at the RF port is about -29 dbm with an LO signal level of +13 dbm.

There are many combinations of RF and LO frequency combinations that may be considered for intermodulation effects. From the bottom table on data sheet page 558, intermodulation products are seen to be below 58 dB relative to the 1 x 1 (RF x LO) at an RF level of -10 dbm and an LO level of +13 dbm. These minute intermodulation products are probably of no concern as they would probably be removed by filters further down the LO system path.

TRW/AERTECH A2S124 Mixer Diode

The TRW/AERTECH AS124 mixer diode is a Schottky high barrier mixer diode (sometimes called a "Hot Carrier" diode) that is the non-linear element in the Harmonic Mixer which mixes the 600 MHz and 12 - 15 GHz YIG signals. Schottky diodes have a low forward drop, fast recovery, a low junction capacitance and a low noise figure. The AS124 has a forward drop of about 0.5 volts at 1 mA, a junction capacitance of 0.10 pF, a noise figure of 6.5 dB and is tested at 16 GHz.

3.0 F12 ALIGNMENT AND BENCH TESTS

This section describes the bench alignment tests that are principally concerned with the "A1" board and the RF components.

Check the power wiring before applying power to the module. The YIG and other components are expensive.

Apply DC power to the module and verify that it is within the F-Rack tolerances.

"A2" Control Board Tests

Before testing the "A1" board, it is necessary to verify that the digital board is functioning properly. Malfunctions in the digital board could confuse tests of the "A1" board and module.

Testing the digital board entails verifying that the command, address and monitor data data circuitry are functioning properly.

1) All eight outputs of the address decoder outputs should be tested (even though some of them are not used) by setting address states which range over all eight addresses. Testing all eight states verifies that the address wiring is correct and that the decoder chip internal logic is functioning correctly.

2) The command register should be checked to verify that the Data Set commands are correct. All command register bits should be exercised to verify that there are no stuck bits, etc. Suggested arguments are all 1's, all 0's, alternate 1's and 0's and the complement of the alternate 1's and 0's.

3) The digital monitor data outputs should be checked for proper operation. Since the command argument is output as an echo on the two LSB's, this data should be checked in conjunction with the command argument tests above.

4) The command select multiplexer should be checked by verifying that both the command register and Thumbwheel states are properly selected. Verify that the Auto/Man switch selects the designated command source. This verifies module and switch wiring. The command select multiplexer should be tested with the command register arguments suggested above. Verify that all Thumbwheel states are properly routed through the multiplexer.

The command select multiplexer outputs are read out as digital monitor data on the MSB of the command echo. Verify that these eight bits are correct.

5) Verify that the states of the Man/Auto, High Lock Warn and Low Lock Warn discretes are correct on the digital monitor data output.

6) Set the +10 volt reference to +10.000 by adjusting the 100 kOhm potentiometer on Dip Header L48.

7) Verify that all sixteen channels of analog monitor data are properly read out by the analog multiplexer. After setting up the RF circuitry, check the multiplexer again to verify that the IF Level, YIG Tuning coil voltage and current, the FM voltage and In-Phase level are correctly multiplexed.

"A1" Control Board Tests

Verify the 200 MHz and 600MHz reference signal levels. The 200 MHz level should be -3 dbm and the 600 MHz level should be +10 dbm.

1) Set the AUTO/MAN switch to Manual.

2) Monitor the TP1 voltage with a DVM. Set the Thumbwheel switches to 0.0 (i.e. the setting for a command of 10.0 GHz). Adjust the "OFFSET ADJ" potentiometer (R42) for 0.000 Volts, +/- 0.001 volts.

3) Set the Thumbwheel switches to 5.0 (i.e. the setting for a command of 15.0 GHz). Adjust the "GAIN ADJ" potentiometer (R43) for +5.000 volts +/- 0.001 volts at TP1.

4) Connect a frequency counter to the front panel LO MON connector. Set the Thumbwheel switches to 2.0 (i.e. the setting for a command of 12.0 GHz) and turn off the ON/OFF sweep select switch on the PC board.

Adjust the "FREQ OFFSET" control (potentiomenter R44) for a 12.0 GHz reading on the frequency counter.

Set the Thumbwheel switches to 5.0 (i.e. the setting for a command of 15.0 GHz).

Adjust the "FREQ SLOPE" control (potentiometer R45) for a 15.0 GHz reading on the frequency counter.

Repeat the "FREQ OFFSET" and "FREQ SLOPE" adjustments until the two frequencies are within +/- 5.0 MHz of the commanded values.

5) Monitor TP3 with an oscilloscope (5VDC/div, 10 mS/div). Turn on the PC board ON/OFF sweep select switch.

Set the Thumbwheel to 5.1 (i.e. the setting for a command of 15.1 GHz, not a standard frequency).

Adjust the "BAL" control (potentiometer R46) for a symmetrical ramping waveform on the oscilloscope.

6) Verify that the frequency counter is still connected to the LO MON connector.

Set the Thumbwheel switches to 1.8 (i.e. the setting for a command of 18 GHz, not a standard frequency but within the YIG operating range).

Adjust "H.M. BIAS" potentiometer (R47) for a LOW LOCK indication on the front panel. If the loop does not lock, adjust "FREQ OFFSET" potentiometer (R44) plus or minus 1/2 turn for a proper lock.

Adjust "FREQ OFFSET" (R44) for a middle scale reading on the bargraph display while holding the I.F. LEV/CONT VOLT switch in the CONT VOLT position.

Adjust the H.M. BIAS potentiometer (R47) for a maximum scale reading while holding the I.F. LEV/CONT VOLT switch in the I.F. LEV position.

7) Check all the standard frequencies listed below for correct High or Low Lock.

Adjust the H.M. BIAS control (R47) for an optimum IF level at all the frequencies. It may be necessary to repeat the sequence through the frequency list to determine the best H.M. BIAS setting.

8) With a power meter, check the power level at the LO MON connector at all the frequencies listed below. The power level should be -3 dbm over these standard frequencies. This test measures the YIG output level over the operating frequency range.

9) With a power meter, check the power level at the IF MON connector at all frequencies listed below. The power level should be -13 dbm. This test measures the 200 MHz level input to the 200 MHz Phase Detector over the operating frequency range.

F12 Standard Lock Frequencies

Using the + (High Lock) and - (Low Lock) symbols as a suffix, YIG lock frequencies are:

11.8 GHz-	12.4 GHz-	13.0 GHz-	13.6 GHz-	14.2 GHz-	14.8 GHz-
12.2 GHz+	12.8 GHz+	13.4 GHz+	14.0 GHz+	14.6 GHz+	15.2 GHz+

F12 output Frequency (in MHz) = N x 600 +/- 200, where N = 20, 21, 22, 23, 24 and 25.

10) The following alignment procedure adjusts the YIG drive circuitry so that all F12's have similar tuning-frequency characteristics. This procedure normalizes the individual YIG's characteristics to a uniform operating range.

With the side plate covers installed and at a stabilized operating temperature, plot the FM coil control voltage against YIG frequency for the standard frequencies listed above. The FM coil control voltage is read from the analog monitor data (address 51_8).

Plot the FM coil voltage values as a function of YIG frequency on linear graph paper. Frequency is plotted along the horizontal axis and control voltage along the vertical axis. Draw a curve through each of the data points; the curve may not be smooth and in some cases may be concave or convex. Draw a best-fit (by eye) straight line through the above curve. Since the circuits that drive the Tuning and FM coils are very linear, the curve represents the tuning characteristics of the YIG oscillator.

The straight line drawn above represents the average value of YIG frequency versus FM coil current. Ideally, this straight line should have a zero slope and should be + 5 Volts +/- 1 Volt.

11) If the straight line in 10) above exceeds the + 5 Volt +/- 1 Volt tolerance, the potentiometer settings described above may have to be readjusted.

A) Remove the module left plate for access to the "A1" control PC board. First attempt to reduce the slope of the straight line by adjusting R43 ("Gain Adjust"). If the straight line slopes up with increasing frequency, it indicates that the YIG's differential sensitivity to the applied magnetic field (delta frequency/delta magnetic field) is less than the nominal value. U4's gain is thus too low and increasing amounts of current drive are required as frequency is increased. If the straight line slopes down with increasing frequency, the YIG's differential sensitivity is greater than the nominal value. Slightly increase (or decrease depending upon the slope) U4's gain by adjusting R43 and record a new set of FM coil voltage versus frequency values. Plot them on a new piece of graph paper and construct a new curve and best straight line through the curve. Repeat the procedure until the straight line slope is small.

B) After reducing the straight line slope, adjust R44 ("Freq Offset") to move the straight line up or down so that all frequency versus FM coil voltages are within the + 5 Volt +/- 1 Volt tolerance band.

C) After completing A) and B) above, install the module left plate. To verify the settings at the operating temperature, after the module temperature has stablized, repeat the measurements of 10) above and plot the curve and straight line. Save this data in the module maintenance files.

4.0 DRAWINGS

This section contains F12 functional drawings such as the module block diagram, module wiring diagram, PC board schematics, BOM's, etc. These drawings are listed below. For convenience, C and D size drawings have been reduced to B-size, foldout sheets. A-size drawings have not been reduced.

A list of F12 fabrication drawings follows the list of functional drawings. Fabrication drawings are not included in this manual.

X-Band system drawings are listed in Section 6.

F12 Functional Drawings

C13165B01	12-15 GHz L.O. Module Block Diagram
D13165S09	12-15 GHz L.O. Module Wiring Diagram
A13165Z05	12-15 GHz Module BOM
C13165S01	12-15 GHz L.O. Cont. P.C. Schematic
C13165P01	12-15 GHz L.O. Control P.C. Assembly
A13165Z04	12-15 GHz L.O. Control PCB BOM
B13165S06	12-15 GHz L.O. Harmonic Mixer Schematic
A13165Z07	12-15 GHz L.O. Harmonic Mixer BOM
B13165S03	12-15 GHz L.O. 200 MHz Phase Detector Schematic
A13165Z06	12-15 GHz L.O. 200 MHz Phase Detector BOM
B13165S04	12-15 GHz L.O. Front Panel Meter Schematic
B13165P04	12-15 GHz L.O. Front Panel Assembly
A13165Z03	12-15 GHz L.O. Front Panel Meter BOM
D13165L02	12-15 GHz L.O. M and C Board Logic Diagram
C13165P02	12-15 GHz L.O. M and C Board Wire Wrap Assembly
A13165P11	12-15 GHz Dip Header Assembly

F12 Fabrication Drawings

B13165AB02	12-15 GHz L.O. Front Panel PCB Artwork
B13165M06	12-15 GHz L.O. Front Panel Drill Drawing
B13165M38	12-15 GHz L.O. Front Panel Meter Lens Drawing
C13165AA06	12-15 GHz L.O. Front Panel Silkscreen
C13165A0B7	12-15 GHz L.O. Front Panel Silkscreen Dimensions
B13165P05	12-15 GHz L.O. 200 MHz Phase Detector Assembly Drawing
B13165AB05	12-15 GHz L.O. 200 MHz Phase Detector Artwork
B13165M10	12-15 GHz L.O. 200 MHz Phase Detector Drill Drawing
B13165AA20	12-15 GHz L.O. 200 MHz Phase Detector Decal
C13165M08	12-15 GHz L.O. 200 Mhz Phase Detector Chassis, Lids
B13165M07	12-15 GHz L.O. Harmonic Mixer Chassis Chassis and Lid
B13165AB03	12-15 GHz L.O. Harmonic Mixer P.C. Artwork

D13165AB01	12-15 GHz L.O. Control P.C.B Artwork
C13165M05	12-15 GHz L.O. Control P.C. Board Drill Drawing
B13165M04	12-15 GHz L.O. OSP Rear Module Panel
B13165M30	12-15 GHz L.O. Wire Wrap Support Block
B13050M18	Module Side Plates
B13165M15	12-15 GHz L.O., Ay-Vector Mounting Bracket
B13165M14	12-15 GHz L.O., P.C. Card Brackets
B13165M16	12-15 GHz L.O., YIG Osc Mount Bracket
C13050M22-1	Module Cover, Perforated
C13165M17	12-15 GHz L.O., Module Center Plate
D13165M09	12-15 GHz L.O., Front Panel Mech Drawing
D13165M18	12-15 GHz L.O., Module Bar Supports
C13165M70	Module Pull
B13165M03	12-15 GHz L.O., OSP Bin Panel

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	6/4/84	SPAULDING		DESIGN CHGS.
B	11/85	SPAULDING		CHG. PART MFGS.
C	4-88	ANOREATTA		DESIGN CHGS.

THUMB-WHEEL SWITCHES (FRONT PANEL)

DIGITAL DISPLAY "A3" BD (FRONT PANEL)

D/A CONVERTER "A1" BD

OFFSET/ SLOPE CONTROL "A1" BD

-3/-4V

TUNING DRIVER VIN "A1" BD

TWISTED PR. TUNING I

YIG OSC. AVANTEK AV-71251

8.4 GHZ FROM DEWAR

OSP CONN.

4.5-5 GHZ TO F9

TRAK 21A9271

50Ω

TRAK 61A6071

8.4/1.0 B.P. FILTER

RF IN

IF OUT 4.5-5GHZ

MIXER W-J M88C

LO IN 12-15 GHZ

PASSIVE MICRO TECH #PTB2007 50Ω

TRIANGLE MICROWAVE #CA-912 -20db

12-15GHZ OUT +14 dbm

12-15GHZ OUT

POWER DIVIDER TRIANGLE MICROWAVE #YL-2133

12-15GHZ IN +14dbm

TRIANGLE MICROWAVE #CA-2014 912

F.P. SMA

DIG. COMMAND MONITOR & ANALOG "A2" BOARD

TUNING V MON.

FM V MON.

TWISTED PAIR

FM I

FM DRIVER "A1" BD. VIN

FM I

+METER

0-+10V

+5V

F.P. LED

AUTO

S2

MAN

600MHZ INPUT -3 dBm (COUPLED FROM "B" RACK 600)

OSP CONN.

600MHZ BANDPASS FILTER K&L 4B120-600/50-0

WJ A77-1 +15db

+10dBm LO IN 600 MHZ

NRAO HARMONIC MIXER

-14 dBm RF IN 12-15GHZ

10db MIDWEST #263

-60 dBm IF OUT 200 MHZ

3db MIDWEST #294

200MHZ BANDPASS FILTER K&L 4B120-200/16-0

AYDIN VECTOR 9AY5037-4 +66db

+3dBm 200MHZ IN

IF MON. OUT

NRAO 0° PHASE DETECTOR

QUAD. 90°

REF.

+10dBm 200MHZ

PHASELOCK LOOP "A1" BD.

SWEEP LOCK "A1" BD.

HIGH LOCK

LOW LOCK

S1

ALCO MTA 106-F MOM. CON.

N.C.

METER +

N.O.

200 MHZ IF MON. (FRONT PANEL)

BNC CONN.

DIG. HIGH LOCK MON "A2" BD

HIGH LOCK (FRONT PANEL LED)

"A3" BD.

DIG. LOW LOCK MON. "A2" BD.

LOW LOCK (FRONT PANEL LED)

+5V

200MHZ INPUT +10 dBm (2-WAY SPLITTER FROM "B" RACK 200)

FM/IF METER (FRONT PANEL) "A3" BD.

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

PROJECT: F12 12-15GHZ L.O.

TITLE: MODULE BLOCK DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY GENE SPAULDING	DATE 3-22-84	
DESIGNED BY LARRY BENO	DATE 3-22-84	
APPROVED BY LB	DATE 3-22-84	

SHEET NUMBER 1 of 1 | DRAWING NUMBER C13165B01 | REV. C | SCALE —

BRUNING 44-231 44427

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	7/13/84	SPAULDING	LAB	DESIGN CH6S.
B	7/26/84	SPAULDING	LAB	CH6 MONITOR, MINOR RELABEL
C	4/1/85	SPAULDING	LAB	ADD TUNING & I MON./RELABEL
D	8/20/87	BENO	LAB	ADD GND'S
E	11-2-87	ANDREATTA	LAB	ADDED NOTES 3 + 4 ADDED R50 + C16 ADDED J2-A + J2-5

CONTROL P.C. CARD
"A1" BOARD D13165AB01 REV A

M&C P.C. CARD
"A2" BOARD

AUTO/MAN ALCO MTA 106-D SPDT

MAN WARN LED HP3082-4860

IF/FM MON C&K MOD. 7105SYCBE MOM. CON.

METER CIRCUIT P.C. CARD "A3" BOARD D13165AB02 REV. A

DIGITRAN #23102 THUMB-WHEEL SWITCH

BACK PANEL

AMP # 204186-5 CONNECTOR (42 PIN)

P1

FL1 FL2 FL3

OSP CONN.

J10 (200MHZ IN, +10dbm)
OSM #4503-7941-00 TYP. (6 CONN.)

J9 (600MHZ IN, -3dbm)

J11 (A/B RF INPUT)

J7 (A/B IF OUTPUT)

J8 (C/D IF OUTPUT)

J12 (C/D RF INPUT)

LO MON. OSM #210-1 SMA

IF MON KING'S KC19-152 BNC

FRONT PANEL

AVANTEK AV71251 YIG OSC.

ASTROLAB #29519 SMA ELBOW

NOTE 3

NOTE 4

NOTES:

1. R11 = DALE #RH-10, 5Ω, 1%
2. FL1 = FL2 = FL3 = ERIE #1201-054, 1500pf
3. INSTALLED IN A_1 AND B_2 ONLY.
4. SELECTED FOR OPTIMUM HARM MIXER PERFORMANCE.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

VLA PROJECT: F12 12-15GHZ LO

TITLE: MODULE WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY GENE SPAULDING DATE 6-12-84
DESIGNED BY L.A. BENO DATE 6-12-84
APPROVED BY DATE 6/11/84

SHEET NUMBER 1 of 1 | DRAWING NUMBER D13165509 | REV. E | SCALE ~

BRUNING 44231 44427-1

REVISIONS				
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

DRAWN BY K. TATE	DATE 09-09-92			
DESIGNED BY L. BENO	DATE 04-20-88			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT F12

TITLE 12-15 GHZ MODULE BOM

DWG NO. A13165Z05 SHEET 1 OF 4

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13165Z05 REV - DATE 09-10-92 PAGE 2 OF 4

MODULE F12 NAME 12-15 GHZ MODULE DWG# _____ SUB ASSY _____ DWG# _____

SCHEM. DWG# D13165S09 LOCATION _____ QUA/SYS. _____ PREPRD BY K. TATE APPRVD BY _____

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1		K&L MICROWAVE	4B120-600/50-0/OP	BANDPASS FILTER, 600 MHZ	1
2		WATKINS JOHNSON	A77-1	AMPLIFIER, L.O.	1
3		AVANTEK	TC2 & TB1	CASE & P.C.B. FOR A77-1	1
4		OMNI SPECTRA	OSM-218	ADAPTER, SMA	2
5		NRAO	DWG #B13165S06	MIXER, HARMONIC	1
6		MIDWEST	294-3	ATTENUATOR, 3db	1
7		K&L MICROWAVE	4B120-200/16/0/OP	BANDPASS FILTER, 200 MHZ	1
8		OMNI SPECTRA	OSM-219	ADAPTER, SMA	1
9		AYDIN VECTOR	AY-5037-4	AMPLIFIER, I.F.	1
10		NRAO	DWG #B13165S03	PHASE DETECTOR, 200 MHZ	1
11		MIDWEST	263-10	ATTENUATOR, 10db	1
12		TRIANGLE MICROWAVE	CA-912	DIR. COUPLER , 12-18 GHZ	2
13		ASTROLAB	29519	ADAPTER, RIGHT ANGLE SMA	1
14		TRAK MICROWAVE	61A6071	ISOLATOR, 4-8 GHZ	2
15		TRAK MICROWAVE	21A9271	ISOLATOR, 8-12 GHZ	2
16		REACTEL	4CO-8.4G-1GS12	BANDPASS FILTER, 8.4 GHZ	2
17		WATKINS JOHNSON	M88C	MIXER	2
18		TRIANGLE MICROWAVE	YL-2133	POWER SPLITTER, 12-15 GHZ	1
19		PAMTECH	PTB2007	ISOLATOR, 12-15 GHZ (INPUT SMA MALE, OUTPUT SMA FEM.)	1
20		AVANTEK	AV-71251	YIG OSCILLATOR, 12-18 GHZ	1

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13165Z05 REV - DATE 09-10-92 PAGE 3 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
21		OMNI SPECTRA	OSM 201-1	CONNECTOR, SMA	12
22		OMNI SPECTRA	OSM 210-1	CONNECTOR, SMA	1
23		OMNI SPECTRA	OSM 531-3	CONNECTOR, SMA	3
24		KINGS	KC-152-19	CONNECTOR, BNC	1
25		ALCO	MTA-106D	SWITCH (F.P.)	1
26		C&K	7105SYCBE	SWITCH (F.P.)	1
27		HEWLETT-PACKARD	HP-5082-4860	LED (F.P.)	1
28		DIGITRAN	23102-2	SWITCH, DECADE (F.P.)	1
29		NRAO	DWG #B13165AB02	PCB, DISPLAY	1
30		OMNI SPECTRA	OSP-4503-7941-00	CONNECTOR, OSP	6
31		OMNI SPECTRA	OSP-4506-7941-02	CONNECTOR, OSP	6
32		NRAO	DWG #D13165AB01, REV. A	PCB, CONTROL	1
33		TRW/CINCH	50-36A-30	CONNECTOR, PCB EDGE	1
34		TRW/CINCH	50-44A-30	CONNECTOR, PCB EDGE	1
35		NRAO	DWG #D13165L02	BOARD, M&C	1
36		VIKING	3VH50/1JN5	CONNECTOR, PCB EDGE	1
37		K&L MICROWAVE	M12-A	CLIP, R.F. FILTER	4
38		ERIE	1201-054	FILTER, FEED THRU	1
39		H&H SMITH	8260	STANDOFF, YIG MOUNT, 1.75"L	4
40		H&H SMITH	8325	STANDOFF, M&C BOARD, .75"L	2
41		H&H SMITH	8324	STANDOFF, CONTR. PCB, .63"L	2
42		SOUTHCO	445-12-204-10	FASTENER	4

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13165Z05 REV - DATE 09-10-92 PAGE 4 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
43		OMNI SPECTRA	RG-402/U	CABLE, SEMI-RIGID COAXIAL	8 FT.
44		AMP	200833-4	PIN, GUIDE	2
45		AMP	203964-6	SOCKET, GUIDE	2
46		AMP	204186-5	BLOCK, 42-PIN	1
47		AMP	202394-2	HOOD	1
48		AMP	201578-1	PIN, CRIMP	25
49		AMP	201334-1	PIN, CRIMP	1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	5/27/84	SPAULDING		DESIGN CHGS.
B	4/5/84	SPAULDING		ADD TP3
C	3/10/84	SPAULDING		LABEL POTS
D	4/1/85	SPAULDING		ADD R48, R49, DEL D11, D12
E	13 JAN 88	BENO		CHANGED U9, U10
F	11-2-87	ANDREATTA		ADDED C17

NOTES:

1. "OFFSET ADJ" (DAC) SET A 0 B 0 C 0 D 0 E 0 F 0 G 0 H 0
   (ADJ. FOR 0.00V)
   "GAIN ADJ" (DAC) SET A 0 B 1 C 0 D 1 E 0 F 1 G 0 H 1
   (ADJ FOR 5.500V
2. R11, D8 & D9 ARE LOCATED OFF BOARD
3. ALL RESISTORS ARE 1/4W, 5%, RC07 TYPE UNLESS SPECIFIED
4. LAST R=49, LAST C=17, LAST D=15, LAST U=10, LAST Q=2
5. TERM. J1 = 44 PIN EDGE CONN #50-44A-30
   TERM J2 = 36 PIN EDGE CONN. #50-36A-30

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA PROJECT: F12 12-15 GHz L.O.

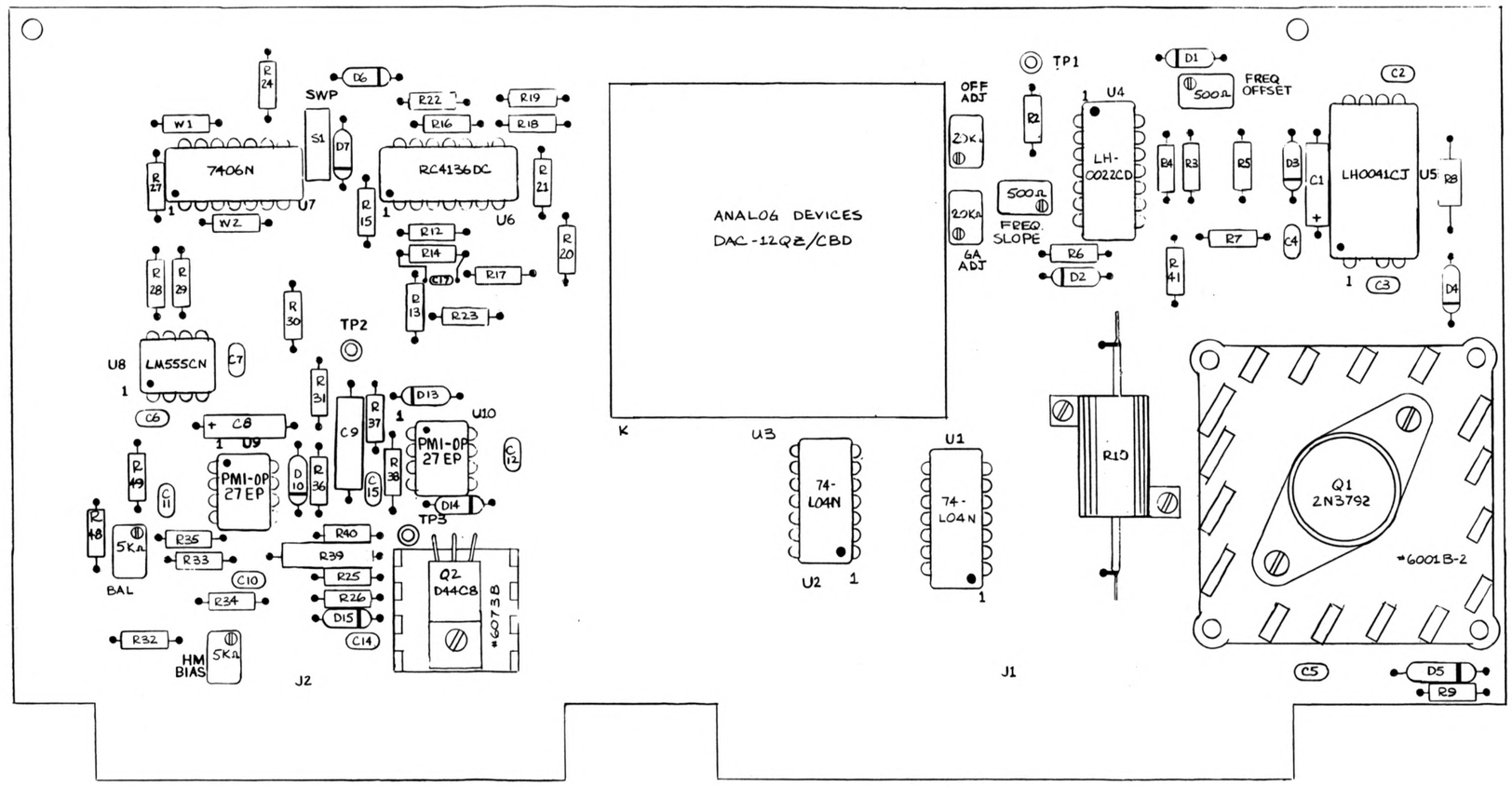
TITLE: CONTROL P.C. CARD
SCHEMATIC
A1 - BOARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY GENE SPAULDING	DATE 4-8-84	
DESIGNED BY L.A. BENO	DATE 4-8-84	
APPROVED BY [signature]	DATE 4-19-84	
SHEET NUMBER 1 of 1	DRAWING NUMBER C13165501	REV. F
		SCALE ~

BRUNING 44-231 44427

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	4/4/84	SPAULDING	LaB	ADD R10, TP3
B	4/28/84	SPAULDING	LaB	DRAWING CORRECTIONS
C	4/1/85	SPAULDING	LaB	REPL. D11 & D12 W/R48 & R49
D	12-3-87	J.M.R.	LaB.	ADDED C17 REPLACED U9 AND U10 WITH OP 27EP REPLACED Q1 WITH 2N3792



NOTES:
1. Q1, Q2, & R10 REQUIRE THERMAL COMPOUND WHEN MOUNTING COMPONENTS.

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA PROJECT: F12 12-15GHZ L.O

TITLE: CONTROL P.C. CARD ASSEMBLY DWG

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY GENE SPAULDING	DATE 4-20-84	
DESIGNED BY GENE SPAULDING	DATE 4-20-84	
APPROVED BY [signature]	DATE 4-20-84	
SHEET NUMBER 1 of 1	DRAWING NUMBER C13165P01	REV. D
		SCALE 2X

BRUNING 44-231 44427

REVISIONS				
REV	DATE	DRAWN BY	APPR'V'D BY	DESCRIPTION

DRAWN BY K. TATE	DATE 09-09-92			
DESIGNED BY L. BENO	DATE 04-20-88			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT F12

TITLE 12-15 GHZ L.O. CONTROL PCB BOM

DWG NO. A13165Z04 SHEET 1 OF 4

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL _____ MECHANICAL BOM # A13165Z04 REV - DATE 09-10-92 PAGE 2 OF 4

MODULE F12 NAME 12-15GHZ LO CONT. PCB DWG# _____ SUB ASSY _____ DWG# _____

SCHEM. DWG# C13165S01 LOCATION _____ QUA/SYS. _____ PREPRD BY K. TATE APPRVD BY _____

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1	R2	TRW	RN-55C	RESISTOR, 10K, 1/8W, 1%	1
2	R3	TRW	RN-55C	RESISTOR, 4020, 1/8W, 1%	1
3	R4	TRW	RN-55C	RESISTOR, 2.1K, 1/8W, 1%	1
4	R5,R22,R23,R50	ALLEN-BRADLEY	RC07GF102J	RESISTOR, 1K, 1/4W, 5%	4
5	R6	TRW	RN-55C	RESISTOR, 2430, 1/8W, 1%	1
6	R7,R24,R33,R37	ALLEN-BRADLEY	RC07GF202J	RESISTOR, 2K, 1/4W, 5%	4
7	R8	ALLEN-BRADLEY	RC20GF151J	RESISTOR, 150, 1/2W, 5%	1
8	R9,R15-R18,R21, R25,R26,R38,R40,R41	ALLEN-BRADLEY	RC07GF103J	RESISTOR, 10K, 1/4W, 5%	11
9	R10,R11	DALE	RH-10	RESISTOR, 5.0, 10W, 1%	2
10	R12,27,R28	ALLEN-BRADLEY	RC07GF512J	RESISTOR, 5.1K, 1/4W, 5%	3
11	R13	ALLEN-BRADLEY	RC07GF472J	RESISTOR, 4.7K, 1/4W, 5%	1
12	R14	ALLEN-BRADLEY	RC07GF104J	RESISTOR, 100K, 1/4W, 5%	1
13	R19,R20	ALLEN-BRADLEY	RC07GF134J	RESISTOR, 130K, 1/4W, 5%	2
14	R29	ALLEN-BRADLEY	RC07GF274J	RESISTOR, 270K, 1/4W, 5%	1
15	R30	ALLEN-BRADLEY	RC07GF333J	RESISTOR, 33K, 1/4W, 5%	1
16	R31	ALLEN-BRADLEY	RC07GF204J	RESISTOR, 200K, 1/4W, 5%	1
17	R32	ALLEN-BRADLEY	RC07GF332J	RESISTOR, 3.3K, 1/4W, 5%	1
18	R34,R35	ALLEN-BRADLEY	RC07GF302J	RESISTOR, 3K, 1/4W, 5%	2
19	R36	ALLEN-BRADLEY	RC07GF301J	RESISTOR, 300, 1/4W, 5%	1
20	R42,R43	BOURNS	3262W	TRIM POT, 20K, 1/4W, 10%	2

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL _____ MECHANICAL BOM # A13165Z04 REV - DATE 09-10-92 PAGE 3 OF 4

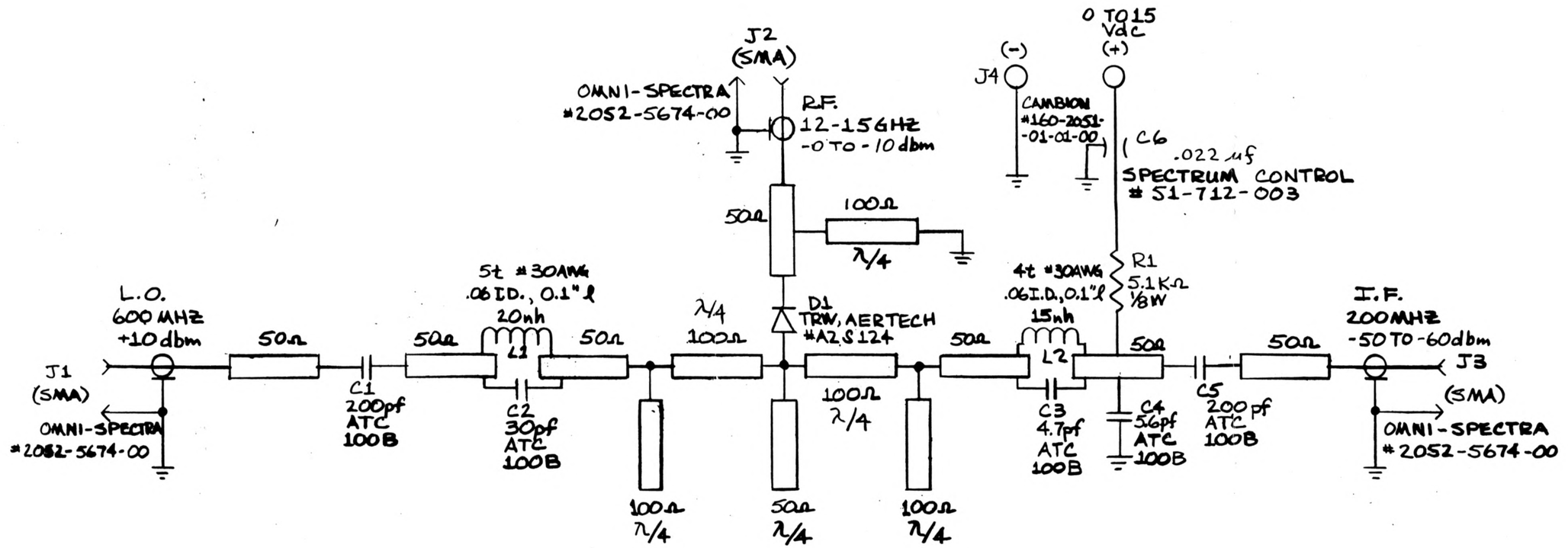
ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
21	R44,R45	BOURNS	3262W	TRIM POT, 500, 1/4W, 10%	2
22	R46,R47	BOURNS	3262W	TRIM POT, 5K, 1/4W, 10%	2
23	R48, R49	ALLEN-BRADLEY	RC07GF100J	RESISTOR, 10, 1/4W, 5%	2
24	C1,C8	SPRAGUE	CSR-13, 2289	CAPACITOR, 15μf, 20 VDC	2
25	C2	MALLORY	CK05BX332K	CAPACITOR, .0033μf	1
26	C3,C4,C6,C10-C12,C15	MALLORY	CK05BX104K	CAPACITOR, 0.1μf	7
27	C5,C7,C17	MALLORY	CK05BX103K	CAPACITOR, .01μf	3
28	C9	C.D.E.	WMF1S15	CAPACITOR, .015μf, 100 VDC	1
29	C14	MALLORY	CK05BX102K	CAPACITOR, .001μf	1
30	C16	SPRAGUE	CSR13E106KL	CAPACITOR, 10μf, 25 VDC	1
31	D1	MOTOROLA	1N827A	DIODE, REFERENCE, 6.2V	1
32	D2,D10	G.E.	1N4148	DIODE	2
33	D3	MOTOROLA	1N5235B	DIODE, ZENER, 6.8V	1
34	D4	MOTOROLA	1N4005	DIODE, ZENER, 6.8V	1
35	D5	MOTOROLA	1N5357B	DIODE, ZENER, 20V	1
36	D6,D7	MOTOROLA	1N5230B	DIODE, ZENER, 4.7V	2
37	D13	MOTOROLA	1N5242B	DIODE, ZENER, 12V	1
38	D14	G.E.	1N456	DIODE	1
39	D15	MOTOROLA	1N4747A	DIODE, ZENER, 20V	1
40	Q1	THERMALLOY	6001B-2	HEAT SINK	1
41	Q2	THERMALLOY	6073B	HEAT SINK	1
42	Q1	MOTOROLA	2N3792	TRANSISTOR	1

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL _____ MECHANICAL BOM # A13165Z04 REV - DATE 09-10-92 PAGE 4 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
43	Q2	G.E.	D44C8	TRANSISTOR	1
44	U1,U2	T.I.	SN74L04N	INTEGRATED CIRCUIT	2
45	U3	ANALOG DEVICES	DAC-12Q2/CBD	HYBRID MODULE	1
46	U4	NATIONAL	LH002CD	INTEGRATED CIRCUIT	1
47	U5	NATIONAL	LH0041CJ	INTEGRATED CIRCUIT	1
48	U6	RAYTHEON	RC4136DC	INTEGRATED CIRCUIT	1
49	U7	FAIRCHILD	F-7406PC	INTEGRATED CIRCUIT	1
50	U8	NATIONAL	LM555CN	INTEGRATED CIRCUIT	1
51	U9,U10	P.M.I.	OP-27EP	INTEGRATED CIRCUIT	2
52	TP1,TP2,TP3	KEYSTONE ELEC.	1559-2	TERMINAL	3
53	S1	ALCO SWITCH	DSS-101	SWITCH	1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	850719	BENO	LaB	MINOR CORR.



NOTES:

1. REF. DWG. # B13165AB03

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA PROJECT: F12 12-15GHZ L.O.

TITLE: HARMONIC MIXER SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY GENE SPAULDING	DATE 5-23-85	
DESIGNED BY L.A. BENO	DATE 5-23-85	
APPROVED BY L. A. Beno	DATE 5/23/85	

SHEET NUMBER 1 OF 1 | DRAWING NUMBER B13165506 | REV. A | SCALE NTS

REVISIONS				
REV	DATE	DRAWN BY	APPR'V'D BY	DESCRIPTION

DRAWN BY K. TATE	DATE 09-09-92			
DESIGNED BY L. BENO	DATE 04-20-88			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT F12

TITLE 12-15 GHZ L.O. HARMONIC MIXER BOM

DWG NO. A13165Z07 SHEET 1 OF 2

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

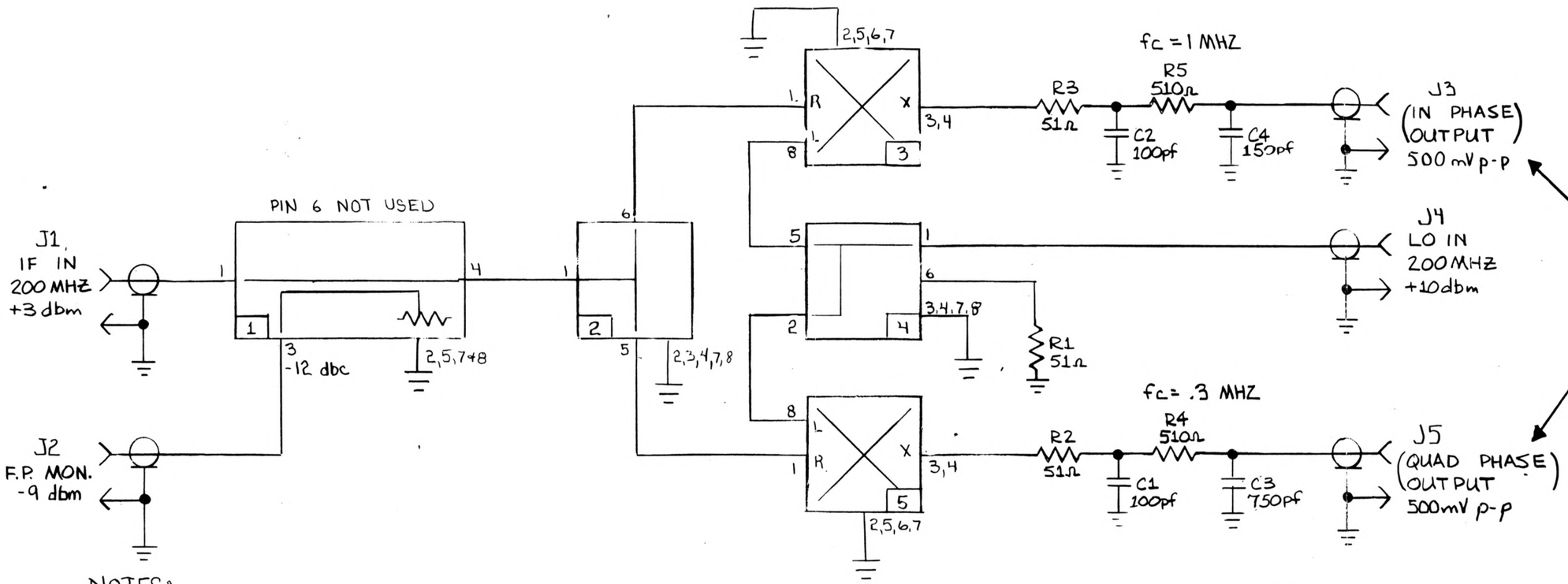
X ELECTRICAL X MECHANICAL BOM # A13165Z07 REV - DATE 09-10-92 PAGE 2 OF 2

MODULE F12 NAME HARMONIC MIXER DWG# _____ SUB ASSY _____ DWG# _____

SCHEM. DWG# B13165S06 LOCATION _____ QUA/SYS. _____ PREPRD BY K. TATE APPRVD BY _____

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1	C1,C5	AMERICAN TECHNICAL CERAMICS	ATC-100B-201-JP300X	CAPACITOR	2
2	C2	AMERICAN TECHNICAL CERAMICS	ATC-100B-200-JP300X	CAPACITOR	1
3	C3	AMERICAN TECHNICAL CERAMICS	ATC-100B-4R7	CAPACITOR	1
4	C4	AMERICAN TECHNICAL CERAMICS	ATC-100B-5R6	CAPACITOR	1
5	C6	SPECTRUM CONTROL	51-712-003	CAPACITOR, FEED THRU	1
6	D1	TRW/AERTECH	A2S124	DIODE, MIXER	1
7	J1-J3	OMNI SPECTRA	2052-5674-00	CONNECTOR, SMA	3
8	J4	CAMBION	160-2051-01-01-00	TERMINAL	1
9	L1	NRAO		INDUCTOR, 20nh, 5 TURNS, #30, .06" ID, 0.1" LONG	1
10	L2	NRAO		INDUCTOR, 15nh, 4 TURNS, #30, .06" ID, 0.1" LONG	1
11	R1	ALLEN-BRADLEY	RC05GF512J	RESISTOR, 5.1K, 1/8W, 5%	1
12		RODGERS RT/DUROID	5870	PCB, 1 OZ. CU. BOTH SIDES ROLLED, .020" THK, 1" X 2"	1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	840719	Dennis	RQR	REDESIGNED



NOTES:

1. J1-J5 OMNI SPECTRA, OSM 244-2
2. C1-C4 ATC-100B SERIES
3. R1-R5 RC05 1/8 WATT 5%

[1] MCL PDC-10-1
[2] MCL PSC-2-1
[3] MCL SRA-1
[4] MCL PSCQ-2-250
[5] MCL SRA-1

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA PROJECT: F12 12-15GHZ LO

TITLE: 200 MHZ Ø DETECTOR SCHEMATIC

SHEET NUMBER 1 of 1 | DRAWING NUMBER B13165503 | REV. A | SCALE ~

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY GENE SPAULDING	DATE 4-25-84
DESIGNED BY L.A. BENO	DATE 4-25-84
APPROVED BY L.A. Beno	DATE 4-25-84

REVISIONS				
REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION

DRAWN BY K. TATE	DATE 09-09-92			
DESIGNED BY L. BENO	DATE 05-11-88			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT F12

TITLE 12-15 GHZ L.O.
200 MHZ PHASE DETECTOR BOM

DWG NO. A13165Z06 SHEET 1 OF 2

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

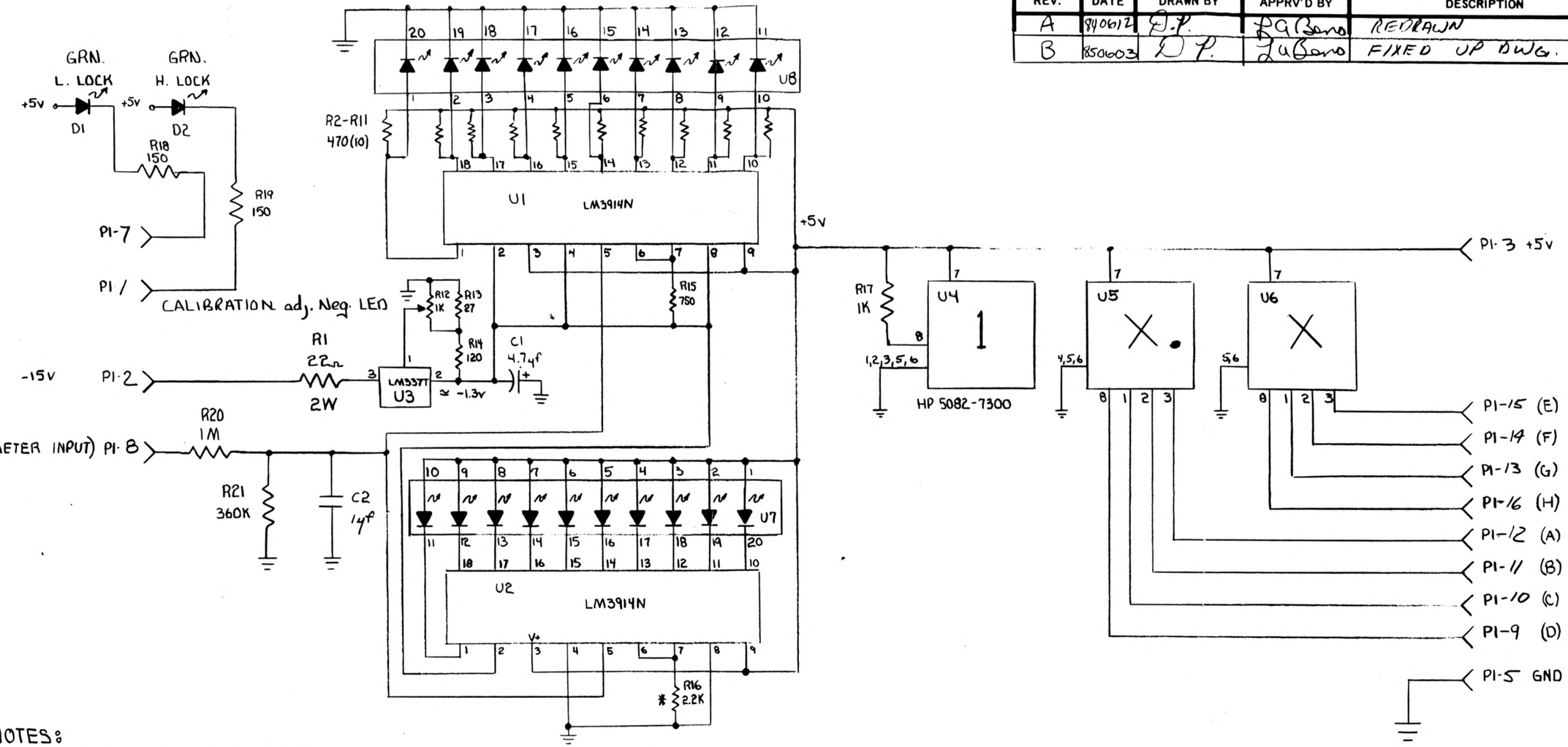
X ELECTRICAL X MECHANICAL BOM # A13165Z06 REV - DATE 09-10-92 PAGE 2 OF 2

MODULE F12 NAME 200 MHZ PHASE DETECT. DWG# _____ SUB ASSY _____ DWG# _____

SCHEM. DWG# B13165S03 LOCATION _____ QUA/SYS. _____ PREPRD BY K. TATE APPRVD BY _____

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1		MINI-CIRCUITS LAB	PDC-10-1	COUPLER, DIRECTIONAL	1
2		MINI-CIRCUITS LAB	PSC-2-1	DIVIDER, POWER	1
3		MINI-CIRCUITS LAB	SRA-1	MIXER	2
4		MINI-CIRCUITS LAB	PSCQ-2-250	DIVIDER, POWER, 90°	1
5	J1,J5	OMNI SPECTRA	OSM-244-2	CONNECTOR, SMA	5
6	R1-R3	ALLEN-BRADLEY	RC05GF510J	RESISTOR, 51, 1/8W, 5%	3
7	R4,R5	ALLEN-BRADLEY	RC05GF511J	RESISTOR, 510, 1/8W, 5%	2
8	C1,C2	AMERICAN TECHNICAL CERAMICS	ATC-100B-101-JP300X	CAPACITOR, CHIP	2
9	C4	AMERICAN TECHNICAL CERAMICS	ATC-100B-151-JP300X	CAPACITOR, CHIP	1
10	C5	AMERICAN TECHNICAL CERAMICS	ATC-100B-751-JP50X	CAPACITOR, CHIP	1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	840612	D.P.	LGBorn	REDRAWN
B	850603	D.P.	LGBorn	FIXED UP DWG.



NOTES:

1. P1 IS 16 PIN DIP SOCKET
2. ALL RESISTORS 1/4 WATT 5% IF NOT SPECIFIED

* LOWER RESISTANCE FOR BRIGHTER LED'S U7 (POS. LED)

3. U6 & U7 IS GENERAL INST. MV-54164 (GRN.)
4. R12 BOURNS P/N 3339P-1-102

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

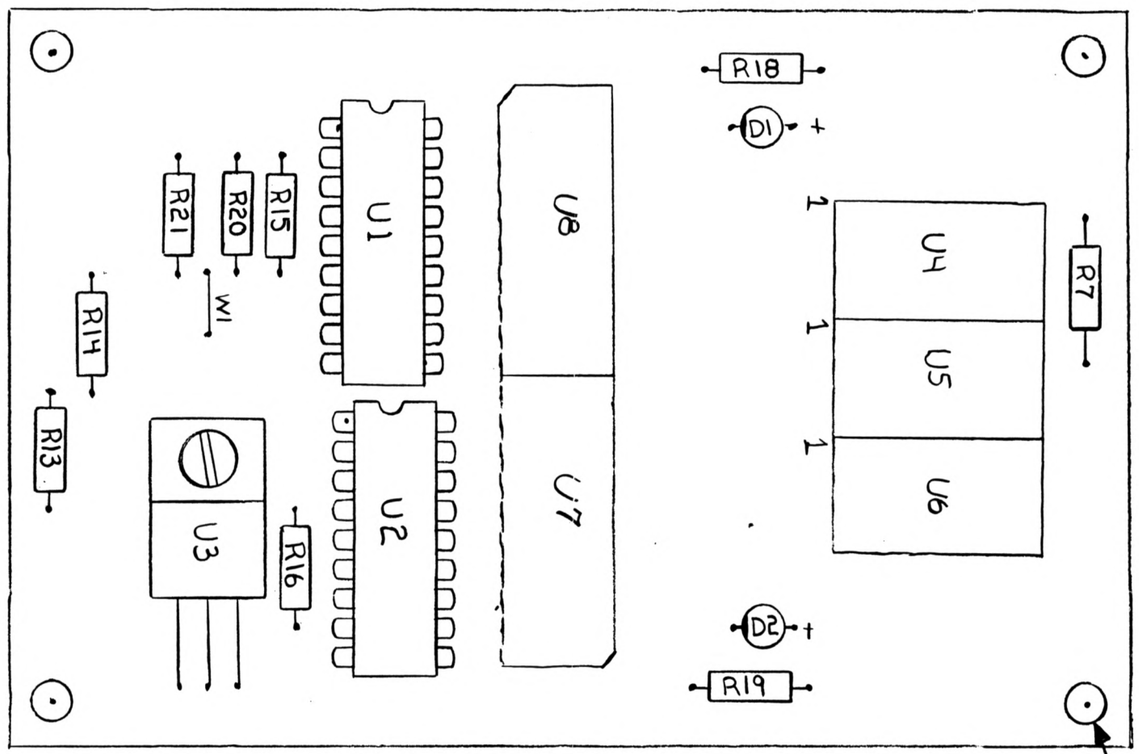
PROJECT: F12 12-15 GHZ L.O.

TITLE: F.P. METER CIRCUIT SCHEMATIC DWG.

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY Dennis Polyard	DATE 840424	
DESIGNED BY Dennis Polyard	DATE 840424	
APPROVED BY LG Born	DATE 840424	
SHEET NUMBER	DRAWING NUMBER B13165504	REV. B
		SCALE

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
B	850602	DP		FIXED DWG.



KEYSTONE STANDOFF P/N 1591-2 (4 PL)

NOTE:
1. INSULATOR INBETWEEN U3 & BOARD

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

PROJECT: F12 12-15 GHZ L.O.

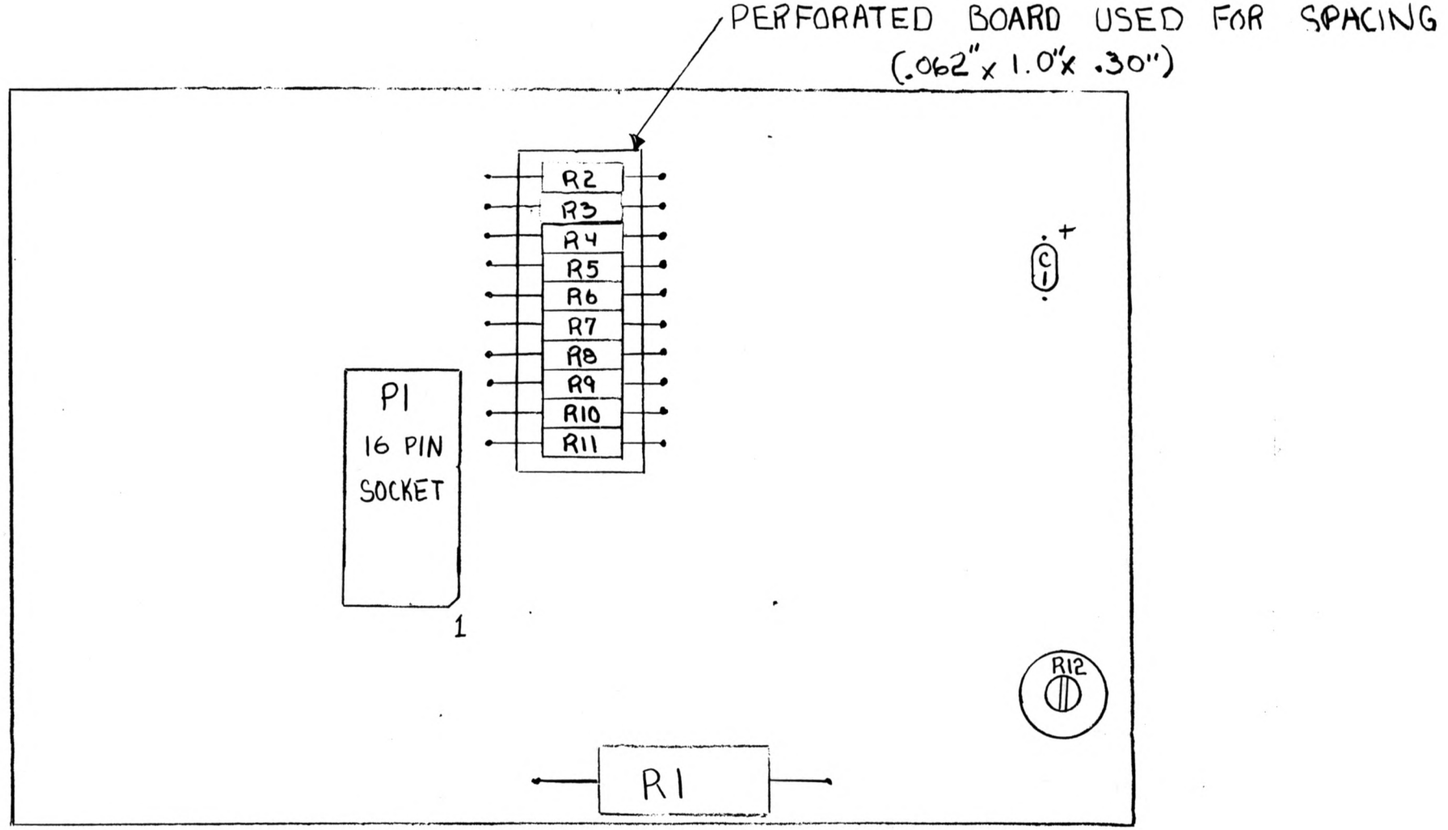
TITLE: F.P. METER CIRCUIT ASSEMBLY DWG FRONT SIDE

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY Dennis Polyard	DATE 840606	
DESIGNED BY Dennis Polyard	DATE 840606	
APPROVED BY LG Bayo	DATE 840606	

SHEET NUMBER 1/2 | DRAWING NUMBER B13165P04 | REV. | SCALE 2/1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

PROJECT: F12 12-15 GHZ L.O.

TITLE: F.P. METER CIRCUIT ASSEMBLY DWG BACK SIDE

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	Dennis Polyard	DATE 840606
DESIGNED BY	Dennis Polyard	DATE 840606
APPROVED BY	L.C. Bono	DATE 840606

SHEET NUMBER 2/2 | DRAWING NUMBER B13165 P04 | REV. | SCALE 2/1

REVISIONS

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	09-09-92	K. TATE	D. POLYARD	REDRAWN WITH ACAD; CORRECTED SCHEMATIC NUMBER ON SHT 2

DRAWN BY K. TATE	DATE 09-09-92			
DESIGNED BY D. POLYARD	DATE 05-31-85			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT F12

TITLE 12-15 GHZ L.O.
FRONT PANEL METER PCB BOM

DWG NO. A13165Z03 SHEET 1 OF 3

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13165Z03 REV A DATE 09-09-92 PAGE 2 OF 3

MODULE F12 NAME FRONT PANEL METER DWG# _____ SUB ASSY _____ DWG# _____

SCHEM. DWG# B13165S04 LOCATION _____ QUA/SYS. _____ PREPRD BY K. TATE APPRVD BY _____

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1	C1	SPRAGUE	196D47SX9035JA1	CAPACITOR, 4.7uf TANTALUM	1
2	C2	CENTRALAB	CZ TYPE 30C105M	CAPACITOR, 1uf MONOLITHIC	1
3	D1,D2	DIALIGHT	521-9250	LED, GREEN DIF	2
4	P1	TEXAS INSTRUMENTS	C931602	IC SOCKET, 16-PIN, LW PROF	1
5	R1	ALLEN-BRADLEY	RC42GF200J	RESISTOR, 22, 2W, 5%	1
6	R2-R11	ALLEN-BRADLEY	RC07GF471J	RESISTOR, 470, 1/4W, 5%	10
7	R12	BOURNS	3339P-1-102	TRIM POT, 1K	1
8	R13	ALLEN-BRADLEY	RC07GF270J	RESISTOR, 27, 1/4W, 5%	1
9	R14	ALLEN-BRADLEY	RC07GF121J	RESISTOR, 120, 1/42, 5%	1
10	R15	ALLEN-BRADLEY	RC07GF751J	RESISTOR, 750, 1/4W, 5%	1
11	R16	ALLEN-BRADLEY	RC07GF222J	RESISTOR, 2.2K, 1/4W, 5%	1
12	R17	ALLEN-BRADLEY	RC07GF102J	RESISTOR, 1K, 1/4W, 5%	1
13	R18,R19	ALLEN-BRADLEY	RC07GF151J	RESISTOR, 150, 1/4W, 5%	2
14	R20	ALLEN-BRADLEY	RC07GF105J	RESISTOR, 1M, 1/4W, 5%	1
15	R21	ALLEN-BRADLEY	RC07GF364J	RESISTOR, 360, 1/4W, 5%	1
16	U1,U2	NATIONAL	LM3914N	LED BAR GRAPH DRIVER	2
17	U3	NATIONAL	LM337T	NEG. VARIABLE REG.	1
18	U4-U6	HEWLETT PACKARD	5082-7300	DISPLAY, MULT. SEGMENT	3
19	U7,U8	GENERAL INSTRUMENT	MV54164	IO SEGMENT LED BARD GRAPH	2
20	P2	ROBINSON NUGENT	ICA-246-S-G	SOCKET, 24-PIN, ICA SERIES	1

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13165Z03 REV A DATE 09-09-92 PAGE 3 OF 3

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
21		KEYSTONE	1591-2	STANDOFF, THREADED	4
22	U3	THERMALLOY, INC.	43-77-2	SPACER, INSULATOR	1
23		KEYSTONE	3053	SPACER, INSULATOR FOR SCREW	1

REV.	DATE	DRAWN BY	APPR'D BY	DESCRIPTION

CMD. INPUT REG, 16 BIT CMD STORAGE

ADDR = 320 8

CMP/MAN MUX

COMMAND ECHO READOUT

ADDR= 220$_8$, 24 BITS

BINARY MONITOR DATA READOUT

ADDR= 221$_8$

SEE ASSY. DWG., # C13165 P02

ADDRESS DECODER

74LS 138

SMA 2 (L23) SMA 1 (L22) SMA Ø (L21)

(L26) SMA-3

(L24) (L25)

Y7 EN7 · Y6 EN6 · Y5 EN5 · Y4 EN4 · Y3 EN3 · Y2 EN2 · Y1 EN1 (K23) · Y0 EN0 (K22)

SMA-3 SMA-2 SMA-1 SMA-Ø

7406 TYP.

LOGIC GND PLANE

+5 PWR PLANE

-15 DIST

+15 DIST

+15V COMM 58 KJ-39

74LS164 SER IN/PAR OUT E41

74LS165 PAR IN/SER OUT L3 · J3 · Q3

74LS165 PAR IN/SER OUT SA L12 · J12 · G12

74LS374 8 BIT LATCH E30 · E19

74LS157 QUAD 2:1 MUX E10 · E01

74LS02 · 74LS04 · 74LS08 · 74LS20 · 74LS202 · 74LS06

DIGO-X · CLKO-X · STRO-X · CMD BN E.N Ø · MCT

THUMB WHEEL CMD INPUTS

MC7 MC6 MC5 MC4 MC3 MC2 MC1 MCØ

(PULL-UP RES NETWORK INSTALLED IN LOC C28)

MAN/CMP SEL LOW=COMP HI= MAN (LOCAL CONTROL)

MAN/CMP

CMD BIT Ø · CMD BIT 1 · CMD BIT 2 · CMD BIT 3 · CMD BIT 4 · CMD BIT 5 · CMD BIT 6 · CMD BIT 7

CB10 CB11 CB12 CB13 CB14 CB15 CB16 CB17

8 SPARE CMD BITS

CLKI-X · CMD ECHO EN Ø · STAI-X · CMD ECHO

MON-Ø 8 BIOP (K17) · MON-1 · MON-2 · MON-3 · MON-4 · MON-5 · MON-6 · MON-7

MON 8 · MON 9 · MON 10 · MON 11 · MON 12 · MON 13 · MON 14 · MON 15 · MON 16 · MON 17

MON 20 · MON 21 · MON 22 · MON 23 · MON 24 · LO LOCK WARN · HI LOCK WARN · MAN/CMP

CLKI-X · SYEI-X · MON ENABLE EN1 · CMD ECHO · MON DATA OUT TO DATA BUS · DIGI-X

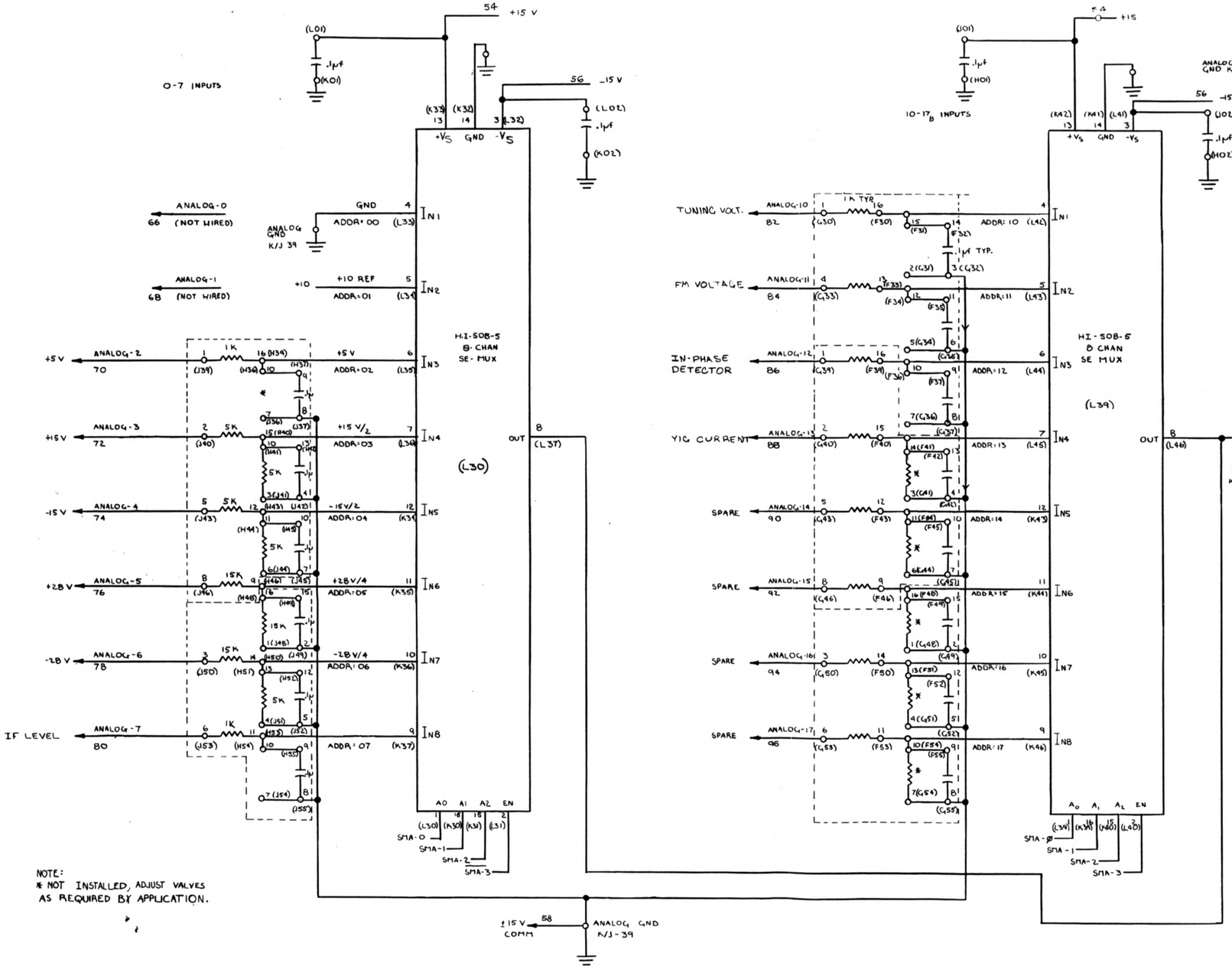
NOTES:

1. NUMBERS IN PARENTHESIS ARE X & Y CORDINATES OF LOGIC BOARD. EX. (A17)
2. DEVICE PIN NUMBERS DO NOT HAVE PARENTHESIS.
3. INSTALL 0.01 CERAMIC CAPACITORS FROM VCC TO GND ACROSS ALL I.C.'S.
4. VCC & GND PINS ON CHIPS TO BE TO ADJACENT VCC & GND PINS.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	12-15 GHz L.O. MODULE	NATIONAL RADIO ASTRONOMY OBSERVATORY
TOLERANCES: ANGLES ± · 3 PLACE DECIMALS (.XXX): ± · 2 PLACE DECIMALS (.XX): ± · 1 PLACE DECIMALS (.X): ±		SOCORRO, NEW MEXICO 87801
MATERIAL:	M&C BOARD LOGIC DIAGRAM	DRAWN BY JEFF CoLe · DATE 4-30-84
FINISH:		DESIGNED BY · DATE
NEXT ASSY · USED ON		APPROVED BY D. WEBBER · DATE 5/3/84
	SHEET NUMBER 1 of 2 · DRAWING NUMBER D13165L02 · REV. · SCALE	

BRUNING 44-231 44427-1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	850601	BENO		MINOR CHGS.



NEXT ASSY	USED ON		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:

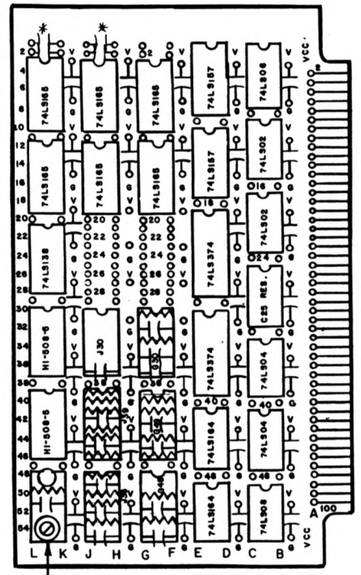
PROJECT: VLA
TITLE: 12-15 GHz LO MODULE
M&C BOARD
A2-BOARD

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	Jeff Cole	DATE	5/2-84
DESIGNED BY		DATE	
APPROVED BY	D. Wilbish	DATE	5/3/84
SCALE		REV.	A
SHEET NUMBER	2 of 2	DRAWING NUMBER	013165102

BRUNING 44-231 44427-1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



NOTE:
1. ALL CAPACITORS ARE .1μf *

SEE LOGIC DWG. # D13165L02

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

PROJECT: 12-15 GHz LO MODULE

TITLE: WIRE WRAP CARD, ASSY. DWG.

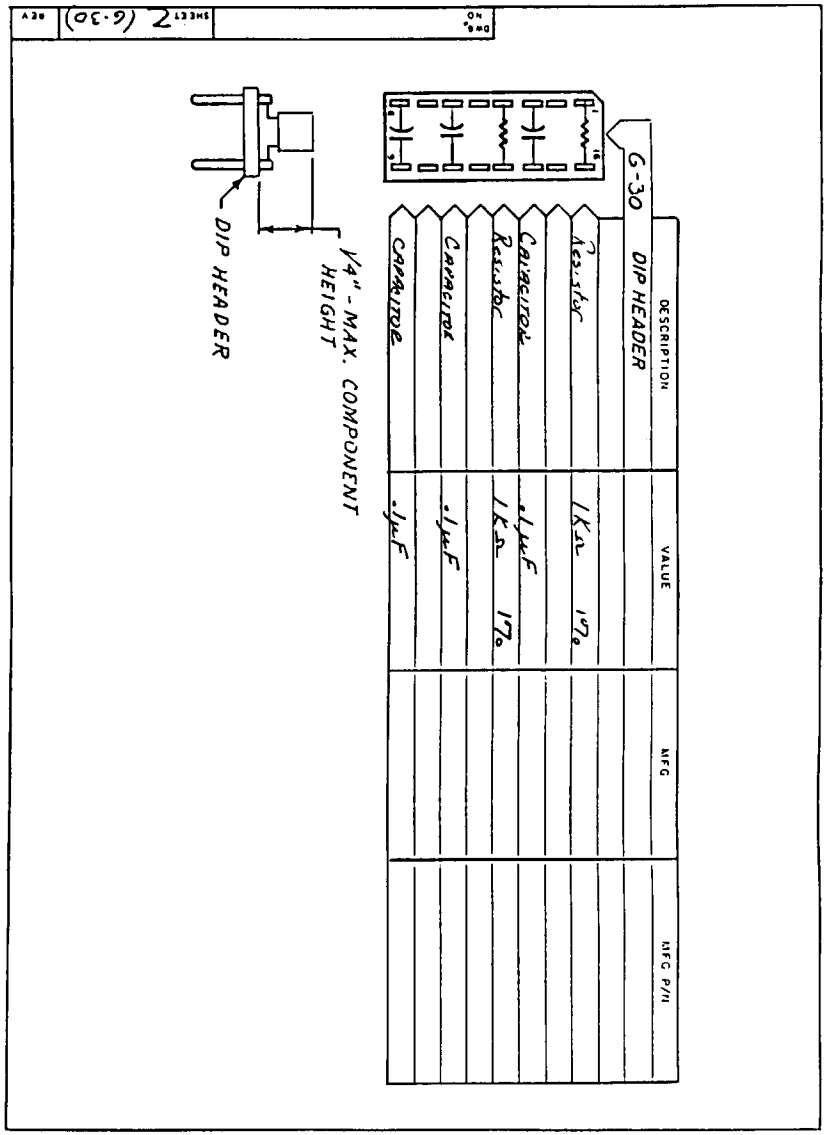
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY JEFF COLE	DATE 5-2-84
DESIGNED BY	DATE
APPROVED BY D. WEBSTER	DATE 5/3/84
SHEET NUMBER 1 of 1	DRAWING NUMBER D13165P02
REV.	SCALE

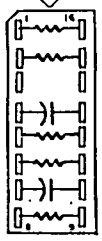
BRUNING 44-231 44427

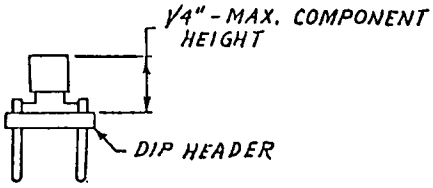
MAY 15 1992

NATIONAL RADIO ASTRONOMY OBSERVATORY (VERY LARGE ARRAY) SOCORRO, NEW MEXICO 87801	V L A	PROJECT F12 TITLE 12-15GHz DIP HEADER ASSY DWG NO A13165P11 SHEET 1 OF 8



DESCRIPTION	VALUE	MFG	MFG P/N
G-39 DIP HEADER			
Resistor	1KΩ 1%		
Resistor	1KΩ 1%		
Capacitor	.1μF		
Resistor	1KΩ 1%		
Resistor	5KΩ 1%		
Capacitor	.1μF		
Resistor	1KΩ 1%		



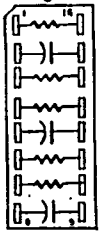


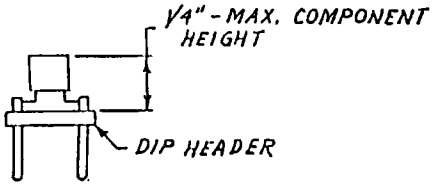
DWG. NO.

SHEET 3 (G-39)

REV.

DESCRIPTION	VALUE	MFG	MFG P/N
G-48 DIP HEADER			
Resistor	5KΩ 1%		
Capacitor	.1μF		
Resistor	1KΩ 1%		
Resistor	5KΩ 1%		
Capacitor	.1μF		
Resistor	1KΩ 1%		
Resistor	5KΩ 1%		
Capacitor	.1μF		



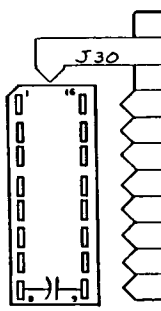


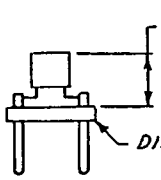
DWG. NO.

SHEET 4 (G-48)

REV.

DESCRIPTION	VALUE	MFG	MFG P/N
J30 DIP HEADER			
CAPACITOR	.1 μF		



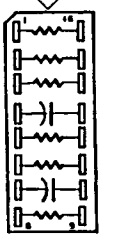


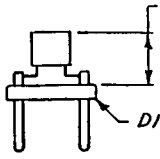
DWG NO -

SHEET 5 (J-30)

REV

DESCRIPTION	VALUE	MFG	MFG P/N
J-39 DIP HEADER			
Resistor	1 KΩ 1%		
Resistor	5 KΩ 1%		
Resistor	5 KΩ 1%		
CAPACITOR	.1 μF		
Resistor	5 KΩ 1%		
Resistor	5 KΩ 1%		
Capacitor	.1 μF		
Resistor	15 KΩ 1%		



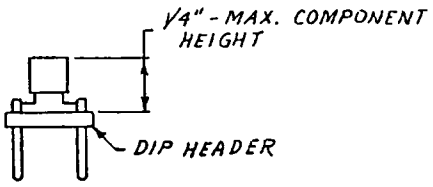


DWG NO -

SHEET 6 (J-39)

REV

J-48	DESCRIPTION	VALUE	MFG	MFG P/N
	DIP HEADER			
	Resistor	5000Ω 1%		
	Capacitor	.1μF		
	Resistor	15KΩ 1%		
	Resistor	5KΩ 1%		
	Capacitor	.1μF		
	Resistor	1KΩ 1%		
	Capacitor	.1μF		

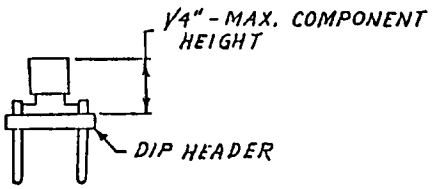


DWG NO.

SHEET 7 J-48

REV

L-48	DESCRIPTION	VALUE	MFG	MFG P/N
	DIP HEADER			
	HI-1608-5			
	Resistor	100KΩ		
	Capacitor	.1μF		
	Potentiometer	100KΩ		
	"			



DWG NO.

SHEET 8 L-48

REV

5.0 DATA SHEETS

This section contains Data Sheets for specialized components. For convenience, the data sheets are grouped into major sub-assembly sets as follows: Control Board ("A1"), Monitor and Control Interface ("A2"), Front Panel Meter Board ("A3"), 200 MHz Phase Detector, Module Plate RF Components and Harmonic Mixer. Each set is headed by a cover sheet which lists the sub-assembly data sheets.

"A1" Board

DAC-12QZ/CBD D/A Converter, Analog Devices
LH0022CD High Performance FET Op Amp, National
RC4136DC, Quad 741 General Purpose Operational Amplifier, Raytheon
LH0041CJ Power Operational Amplifier, National
2N3792 Silicon PNP Power Transistor, Motorola
LM555CN Timer, National
OP27EP, Precision Operational Amplifier, Precision Monolithics
D44C8 Power Darlington Transistors, NPN Silicon, Motorola

ANALOG DEVICES

Low Cost General Purpose Digital to Analog Converter

DAC-12QZ

FEATURES
- Low Cost
- 12-Bit Resolution
- ½LSB Linearity
- ±30ppm/°C TC
- 20ppm/% Power Supply Rejection
- Programmable Output Ranges
- Small Size – 2" x 2" x 0.4"

GENERAL DESCRIPTION

The DAC-12QZ is a low-cost/high performance 12-bit digital-to-analog converter designed for general purpose OEM applications. The completely self-contained module includes weighted resistor networks, monolithic current switches, temperature compensated reference and an externally programmable output amplifier. Performance specifications include 1/2LSB linearity error, 5μs settling time for full scale conversion 30ppm/°C temperature coefficient and 20ppm/% power supply rejection.

INPUT CODING

The internal switches of the complementary binary and complementary BCD models are driven directly without need of a strobe. The complementary codes for each model are:

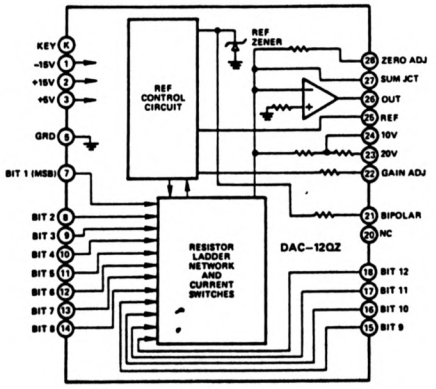
MODEL	-F.S.	Zero	+F.S.
DAC-12QZ/CB	1111 1111 1111	0111 1111 1111	0000 0000 0000
	1111 1111 1111	0111 1111 1111	0000 0000 0000
DAC-12QZ/CBD	1111 1111 1111	1010 1111 1111	0110 0110 0110
	1111 1111 1111	1010 1111 1111	0110 0110 0110

OUTPUT PROGRAMMING

The scale factor is programmed by connecting external jumpers between module pins. With either model, the user can select any one of five output ranges, including bipolar outputs. The choices are:

Unipolar	0 to +5V, 0 to +10V
Bipolar	±2.5V, ±5V, ±10V

The external jumpers at the module pins determine the output amplifier feedback resistance, allowing use of one 5k resistor, or both, either in series to provide 10k, or parallel to provide 2.5k. Offset of exactly one-half full scale for bipolar applications is provided by connecting another jumper to the summing junction of the output amplifier. To maintain constant load on the reference zener, the bipolar offset output should be grounded when using the module in a unipolar mode.



DAC-12QZ Block Diagram

SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

RESOLUTION	12 Bits
DIGITAL INPUTS	TTL Compatible
'0' E <+0.8V	@ –0.1mA
'1' +2V<E<+6V	@ +1.0mA (open input equivalent to digital "1")
INPUT CODES	
Unipolar	Complementary Binary (CB)
	Complementary BCD (CBD)
Bipolar	Complementary Offset Binary
	Complementary Offset BCD
OUTPUT RANGES	0 to +5V @ 10mA
	0 to +10V @ 5mA
(User Programmable; See Figure 1)	±2.5V, ±5V @ 10mA
	±10V @ 5mA
OUTPUT IMPEDANCE	0.02Ω
CONVERSION SPEED	5μs to 0.01% (for 10V step)
Slewing Rate	15V/μs
LINEARITY ERROR	±½LSB
TEMPERATURE COEFFICIENT	
Gain	±30ppm/°C of Reading, max
Zero	±50μV/°C (Unipolar), max
	±100μV/°C (Bipolar), max
Differential Linearity	±10ppm/°C F.S., max
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +125°C
POWER REQUIREMENTS	+15V ±5% @ 20mA
	-15V ±5% @ 30mA
	+5V ±10% @ 20mA
POWER SUPPLY SENSITIVITY	
Gain	±20ppm/% } ±15V only;
Zero	±5ppm/% } tracking supplies
ADJUSTMENTS (USER PROVIDED)	
Gain (20k, 20 turn pot)	±0.3% F.S.
Zero (20k, 20 turn pot)	±30mV
OUTLINE DIMENSIONS	2" x 2" x 0.4"

[1] Recommended Power Supply: Analog Devices model 923.

Specifications subject to change without notice.

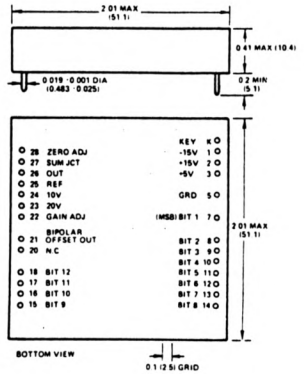
ORDERING GUIDE:

Model DAC-12QZ/XXX

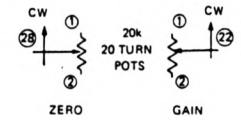
- CB
- CBD

OUTLINE DIMENSIONS AND PIN CONNECTIONS

Dimensions shown in inches and (mm).



POTENTIOMETER CONNECTIONS



OUTPUT PROGRAMMING

Output Range	External Pin Connections		
±2.5V	21, 23, & 27	24 & 26	
±5V	21 & 27	24 & 26	
±10V	21 & 27	23 & 26	
+5V	23 & 27	24 & 26	21 & 5
+10V	24 & 26	21 & 5	

Connect pins as indicated for selected output.

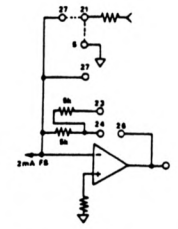


Figure 1. Output Amplifier

P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Tel: 617/329-4700 TWX: 710/394-6577
Telex: 924491 Cables: ANALOG NORWOOD MASS

National Semiconductor

Operational Amplifiers/Buffers

LH0022/LH0022C High Performance FET Op Amp
LH0042/LH0042C Low Cost FET Op Amp
LH0052/LH0052C Precision FET Op Amp

General Description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 500 microvolts maximum offset and 5 μV/°C offset drift. Input offset current is less than 500 femtoamps at room temperature and 500 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with neglible effect in CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the −55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the −25°C to +85°C temperature range.

Features

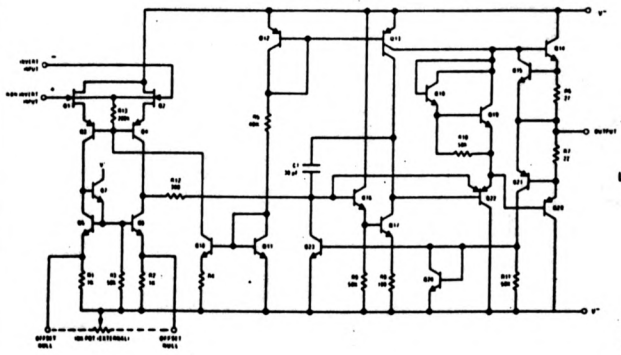
- Low input offset current—500 femtoamps max. (LH0052)
- Low input offset drift—5 μV/°C max (LH0052)
- Low input offset voltage — 100 microvolts-typ.
- High open loop gain — 100 dB typ.
- Excellent slew rate — 3.0 V/μs typ.
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

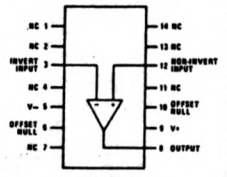
Special electrical parameter selection and custom built circuits are available on special request.

For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

Schematic and Connection Diagrams



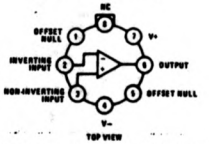
Dual-In-Line Package



TOP VIEW

Order Number LH0022D, LH0022CD, LH0042D, LH0042CD, LH0052D or LH0052CD
See Package D14E

Metal Can Package



TOP VIEW

Order Number LH0022H, LH0022CH, LH0042H, LH0042CH, LH0052H or LH0052CH
See Package H08A

*Previously Called NH0022/NH0022C

Absolute Maximum Ratings

Supply Voltage	±22V
Power Dissipation (see graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V⁻	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, LH0042, LH0052	−55°C to +125°C
LH0022C, LH0042C, LH0052C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

DC Electrical Characteristics for LH0022/LH0022C (Note 3)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022			LH0022C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 100$ kΩ; $T_A = 25°C$, $V_S = \pm 15V$		2.0	4.0		3.5	6.0	mV
	$R_S \leq 100$ kΩ, $V_S = \pm 15V$			5.0			7.0	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100$ kΩ		5	10		5	15	μV/°C
Offset Voltage Drift with Time			3			4		μV/week
Input Offset Current	(Note 4)		0.2	2.0		1.0	5.0	pA
				2.0			0.5	nA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		5	10		10	25	pA
				10			2.5	nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ, $V_{IN} = \pm 10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ, $\pm 5V \leq V_S \leq \pm 15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2$ kΩ, $V_{OUT} = \pm 10V$, $T_A = 25°C$, $V_S = \pm 15V$	100	200		75	160		V/mV
	$R_L = 2$ kΩ, $V_{OUT} = \pm 10V$, $V_S = \pm 15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1$ kΩ, $T_A = 25°C$, $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2$ kΩ, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		2.0	2.5		2.4	2.8	mA
Power Consumption	$V_S = \pm 15V$			75			85	mW

DC Electrical Characteristics for LH0042/LH0042C (Note 3)

Parameter	Conditions	Limits						Units
		LH0042			LH0042C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$R_S \leq 100k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100k\Omega$		5.0			10		µV/°C
Offset Voltage Drift with Time			7.0			10		µV/week
Input Offset Current	(Note 4)		1.0	5.0		2.0	10	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		10	25		15	50	pA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 19°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$, $V_{IN} = \pm 10V$	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	70	86		70	80		dB
Large Signal Voltage Gain	$R_S \leq 2k\Omega$, $V_{OUT} = \pm 10V$	50	150		25	100		V/mV
Output Voltage Swing	$R_L = 1k\Omega$, $T_A = 25°C$ $R_L = 2k\Omega$	±10 ±10	±12.5		±10 ±10	±12		V V
Output Current Swing	$V_{OUT} = \pm 10V$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption				105			120	mW

DC Electrical Characteristics For LH0052/LH0052C (Note 3)

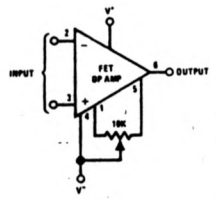
Parameter	Conditions	Limits						Units
		LH0052			LH0052C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$R_S < 100k\Omega$, $V_S = +15V$ $T_A = 25°C$		0.1	0.5		0.2	1.0	mV
	$R_S < 100k\Omega$, $V_S = \pm 15V$			1.0			1.5	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100k\Omega$, $V_S = \pm 15V$		2.0	5.0		5.0	10	µV/°C
Offset Voltage Drift with Time			2.0			4.0		µV/week
Input Offset Current	(Note 4)		0.01	5.0 500		0.02	1.0 100	pA pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time		<0.1			<0.1			pA/week
Input Bias Current	(Note 4)		0.5	2.5 2.5		1.0	5.0 0.5	pA nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S < 10k\Omega$, $V_{IN} = \pm 10V$	74	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S < 10k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	74	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2K\Omega$, $V_{OUT} = \pm 10V$ $V_S = \pm 15V$, $T_A = 25°C$	100	200		75	160		V/mV
	$R_L = 2k\Omega$, $V_{OUT} = \pm 10V$ $V_S = \pm 15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $t_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		3.0	3.5		3.0	3.8	mA
Power Consumption	$V_S = \pm 15V$			105			114	mW

AC Electrical Characteristics For all amplifiers ($T_A = 25°C$, $V_S = \pm 15V$)

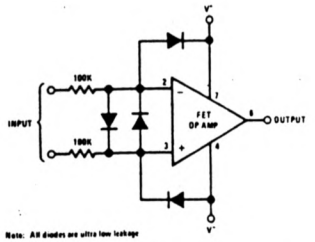
PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0022/42/52			LH0022C/42C/52C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/µs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	µs
Overshoot			10	30		15	40	%
Settling Time (0.1 %)	$\Delta V_{IN} = 10V$		4.5			4.5		µs
Overload Recovery			4.0			4.0		µs
Input Noise Voltage	$R_S = 10k\Omega$, $f_o = 10$ Hz		150			150		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10k\Omega$, $f_o = 100$ Hz		55			55		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10k\Omega$, $f_o = 1$ kHz		35			35		$nV/\sqrt{Hz}$
Input Noise Voltage	$R_S = 10k\Omega$, $f_o = 10$ kHz		30			30		$nV/\sqrt{Hz}$
Input Noise Voltage	BW = 10 Hz to 10 kHz, $R_S = 10k\Omega$		12			12		µVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 2: Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.
Note 3: Unless otherwise specified, these specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ for the LH0022 and LH0052 and $-25°C \leq T_A \leq +85°C$ for the LH0022C and LH0052C Typical values are given for $T_A = 25°C$.
Note 4: Input currents are a strong function of temperature. Due to high speed testing they are specified a junction temperature $T_j = 25°C$, self heating will cause an increase in current in manual tests.

Auxiliary Circuits (Shown for TO-5 pin out)

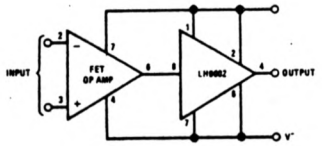


Offset Null



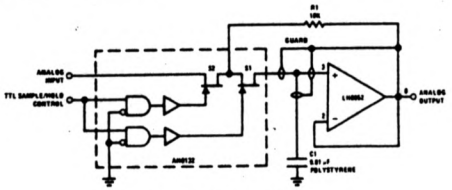
Note: All diodes are ultra low leakage

Protecting Inputs From ± 150V Transients

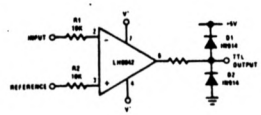


Boosting Output Drive to ± 100 mA

Typical Applications

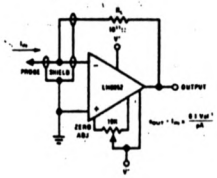


Low Drift Sample and Hold

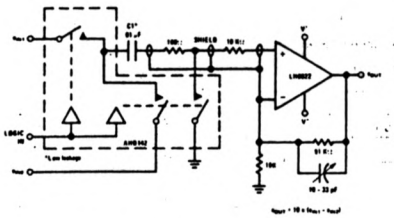


Precision Voltage Comparator

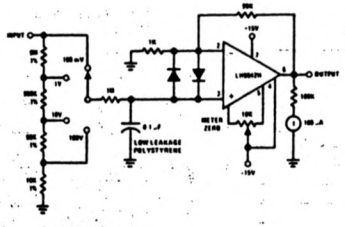
Typical Applications (Cont'd)



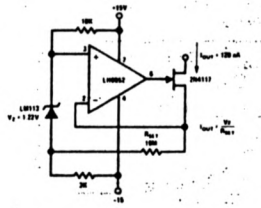
Picoamp Amplifier for pH Meters and Radiation Detectors



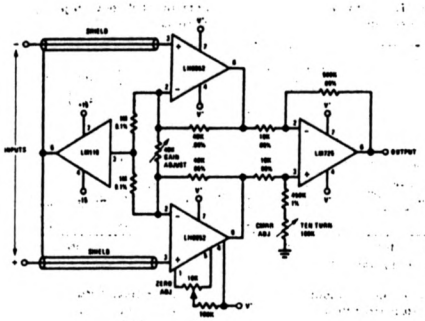
Precision Subtractor for Automatic Test Gear



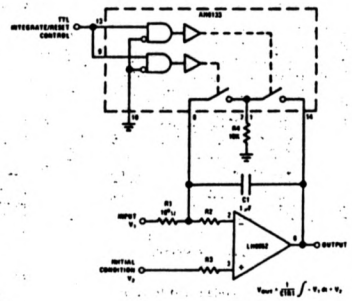
Sensitive Low Cost "VTVM"



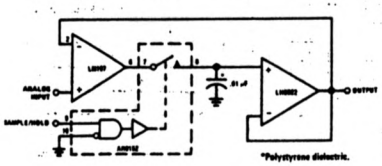
Ultra Low Level Current Source



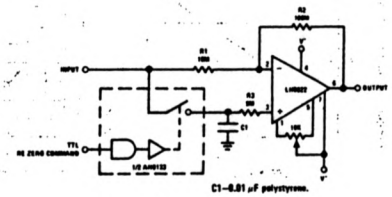
True Instrumentation Amplifier



Precision Integrator

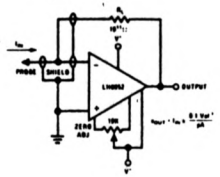


Precision Sample and Hold

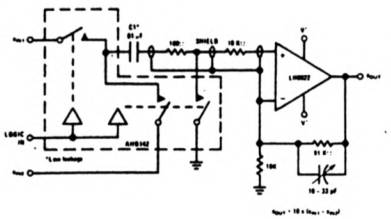


Re-Zeroing Amplifier

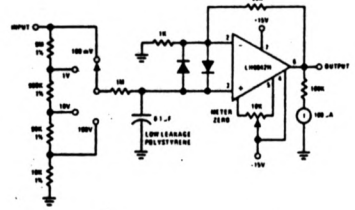
Typical Applications (Cont'd)



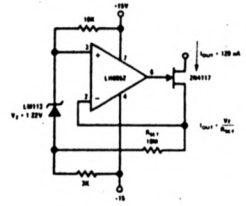
Picoamp Amplifier for pH Meters and Radiation Detectors



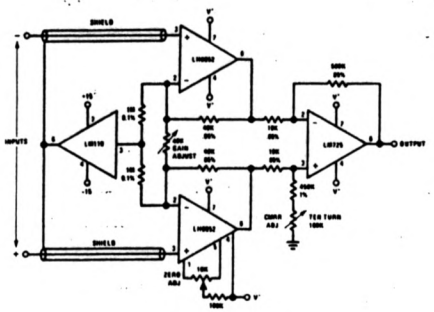
Precision Subtractor for Automatic Test Gear



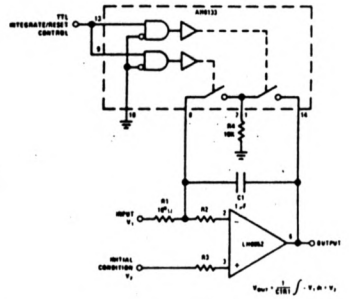
Sensitive Low Cost "VTVM"



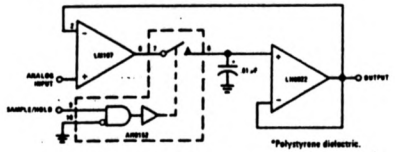
Ultra Low Level Current Source



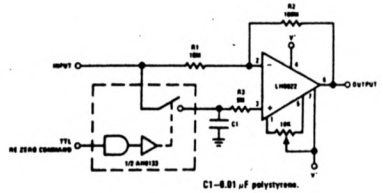
True Instrumentation Amplifier



Precision Integrator



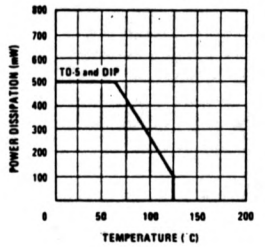
Precision Sample and Hold



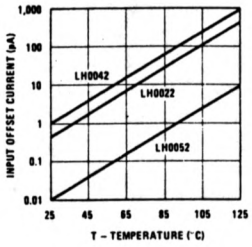
Re-Zeroing Amplifier

Typical Performance Characteristics

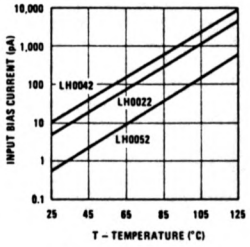
Maximum Power Dissipation



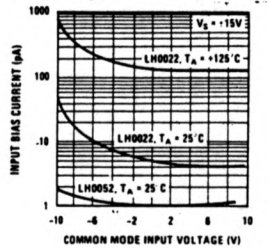
Input Offset Current vs Temperature



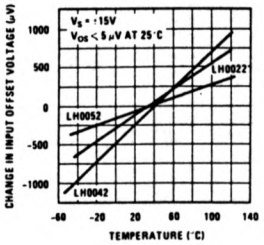
Input Bias Current vs Temperature



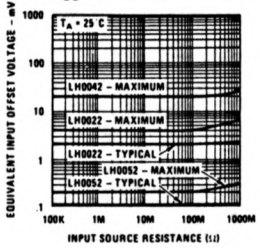
Input Bias Current vs Input Voltage



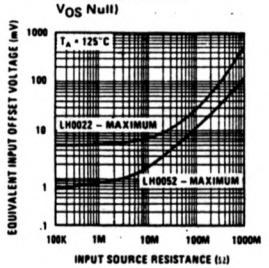
Input Offset Voltage vs Temperature



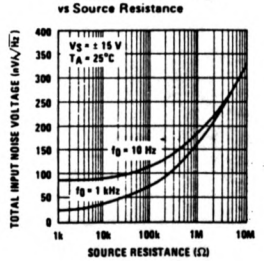
Offset Error (Without V_{OS} Null)



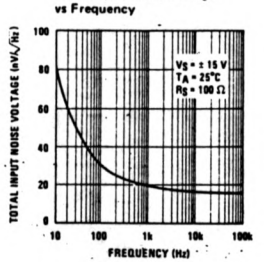
Offset Error (Without V_{OS} Null)



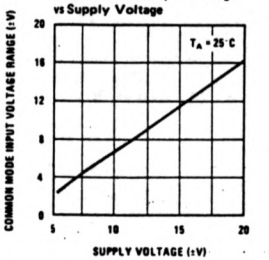
Total Input Noise Voltage* vs Source Resistance



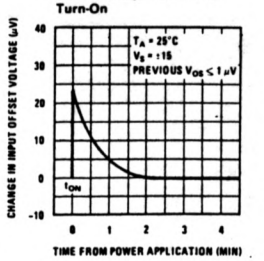
Total Input Noise Voltage* vs Frequency



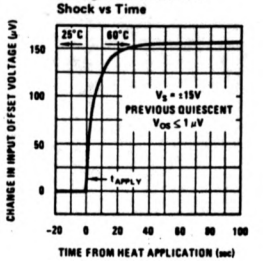
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On



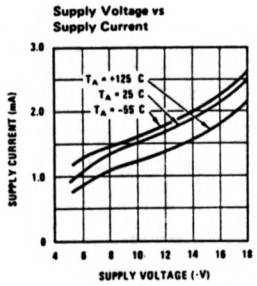
Change in Input Offset Voltage Due to Thermal Shock vs Time



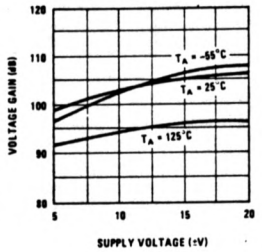
*Noise Voltage Includes Contribution from Source Resistance

Typical Performance Characteristics (Cont'd)

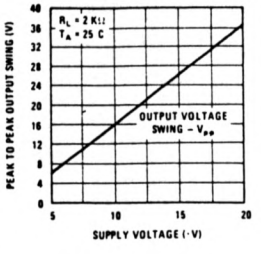
Supply Voltage vs Supply Current



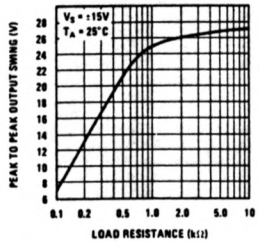
Voltage Gain



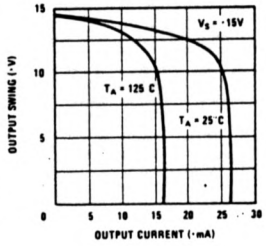
Output Swing vs Supply Voltage



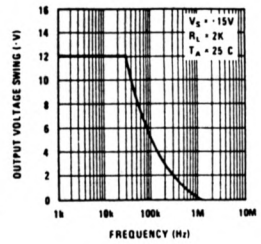
Output Voltage Swing vs Load Resistance



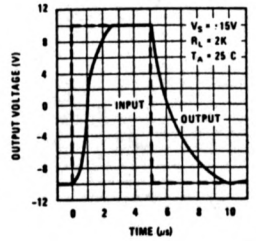
Current Limiting



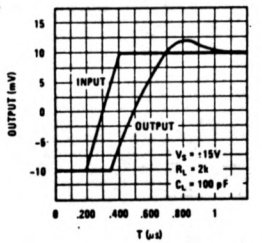
Output Voltage Swing vs Frequency



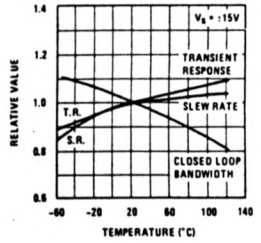
Voltage Follower Large Signal Response



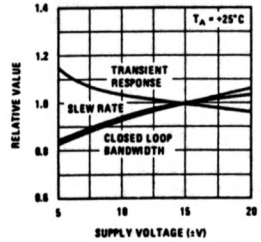
Transient Response



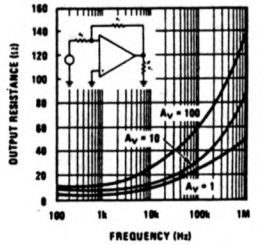
Frequency Characteristics vs Ambient Temperature



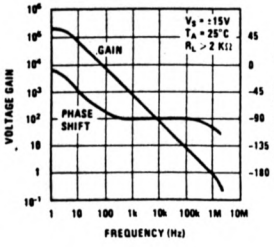
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



Open Loop Transfer Characteristics vs Frequency



GENERAL DESCRIPTION

The RM4136 and RC4136 include four independent high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial processes.

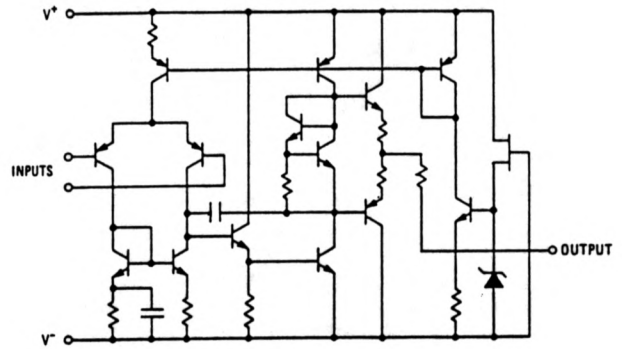
These amplifiers meet or exceed all specifications for 741 type amplifiers. Excellent channel separation allows the use of the 4136 quad amplifier in all 741 operational amplifier applications providing the highest possible packaging density.

The specially designed low noise input transistors allow the 4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners.

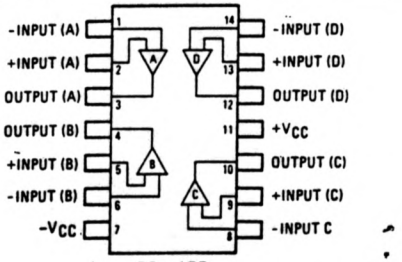
DESIGN FEATURES

- Unity Gain Bandwidth, 3MHz
- Continuous Short Circuit Protection
- No Frequency Compensation Required
- No Latch-up
- Large Common Mode and Differential Voltage Ranges
- Low Power Consumption
- Parameter Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers

SCHEMATIC DIAGRAM



CONNECTION INFORMATION



DC and DB
Dual In-line Packages
(Top View)

Order Part Nos.:
RM4136DC, RV4136 DB,
RC4136DC, RC4136DC

ABSOLUTE MAXIMUM RATINGS

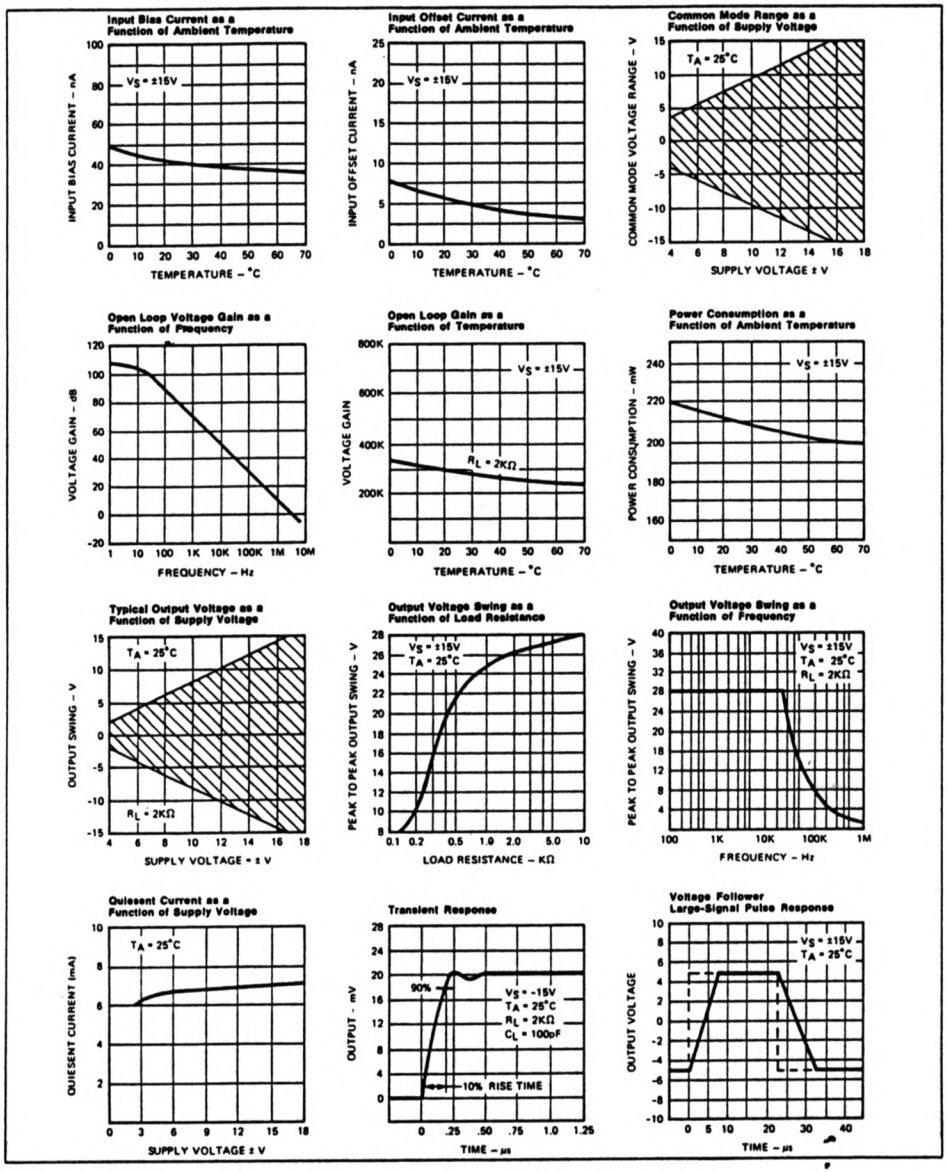
Supply Voltage	RM4136: ±22V	Storage Temperature Range	−65°C to +150°C
	RV4136, RC4136: ±18V	Operating Temperature Range	RM4136: −55°C to +125°C
Internal Power Dissipation (Note 1)	800mW		RC4136: 0°C to +70°C
Differential Input Voltage	±30V		RV4136: −40°C to +85°C
Input Voltage (Note 2)	±15V	Lead Temperature (Soldering, 60s)	300°C
		Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_A = +25°C unless otherwise noted.)

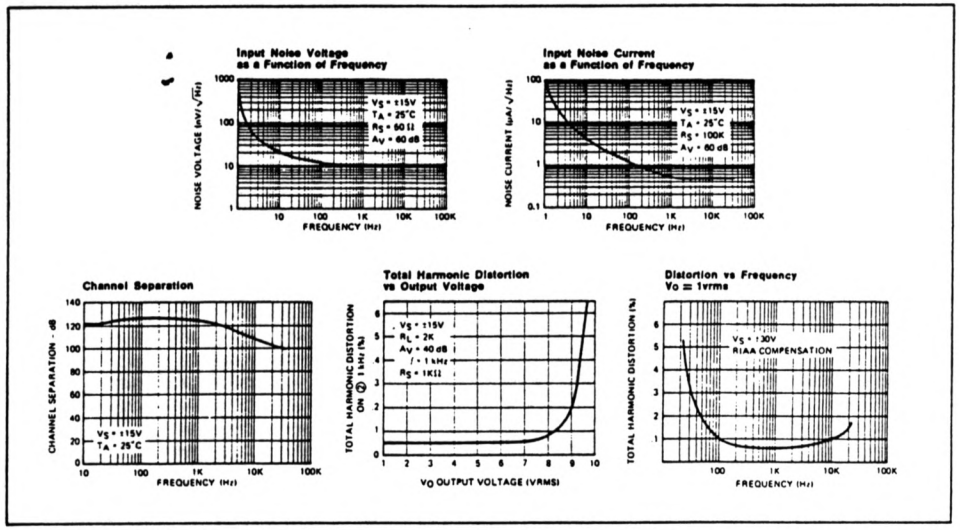
PARAMETER	CONDITIONS	RM4136			RV4136, RC4136			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{out} = \pm 10V$	50,000	300,000		20,000	300,000		V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	100		70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		10	150		10	150	μV/V
Power Consumption	$R_L = \infty$, All Outputs		210	340		210	340	mW
Transient Response (unity gain)	V_{in} = 20 mV, R_L = 2 kΩ, $C_L \leq 100$ pF							
Risetime			0.13			0.13		μs
Overshoot			5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate (unity gain)	$R_L \geq 2\ k\Omega$		1.5			1.0		V/μs
Channel Separation (open loop)	f = 10 kHz, R_S = 1 kΩ		105			105		dB
(Gain = 100)	f = 10 kHz, R_S = 1 kΩ		105			105		dB
The following specifications apply for −55°C ≤ T_A ≤ +125°C for RM4136; 0°C ≤ T_A ≤ +70°C for RC4136.								
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{out} = \pm 10V$	25,000			15,000			V/V
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±10			±10			V
Power Consumption	T_A = High		180	300		180	300	mW
	T_A = Low		240	400		240	400	mW

NOTES:
1. Rating applies for case temperature to +25°C; derate linearly at 6.4 mW/°C for ambient temperatures above +25°C.
2. For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or one amplifier only. I_{CC} = 45mA (typical).

TYPICAL ELECTRICAL DATA



TYPICAL ELECTRICAL DATA



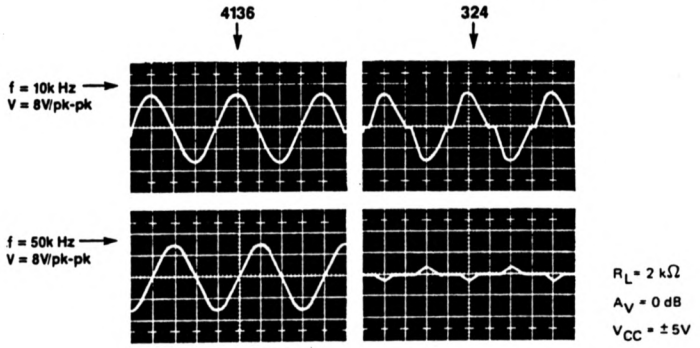
ELECTRICAL CHARACTERISTICS COMPARISON (V_{CC} = ±15V, T_A = +25°C)

PARAMETER		RC4136 (typ)	RC741 (typ)	LM324 (typ)	UNIT
Input Offset Voltage		0.5	2.0	2	mV
Input Offset Current		5	10	5	nA
Input Bias Current		40	80	55	nA
Input Resistance		5	2		MΩ
Large-Signal Voltage Gain (R_L = 2 kΩ)		300,000	200,000	100,000	V/V
Output Voltage Swing (R_L = 2 kΩ)		±13V	±13V	$\lvert+V_{CC} - 1.2V\rvert$ to $-V_{CC}$	V
Input Voltage Range		±14V	±13V	$\lvert+V_{CC} - 1.5V\rvert$ to $-V_{CC}$	V
Common-Mode Rejection Ratio		100	90	85	dB
Supply Voltage Rejection Ratio		10	30	10	µV/V
Transient Response (gain = 1)	Risetime	0.13	0.3		µs
	Overshoot	5	5		%
Unity-Gain Bandwidth		3	0.8	0.8	MHz
Unity-Gain Slew Rate		1.0	0.5	0.5	V/µs
Input Noise Voltage (f_O = 1 kHz)		10	22.5		$nV/\sqrt{Hz}$
Output Short-Circuit Current		±45	±25		mA

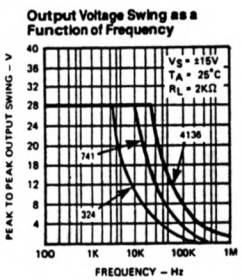
4136 vs. 741

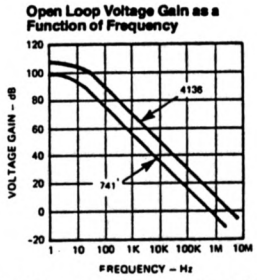
Although the 324 is an excellent device for single-supply applications where ground-sensing is important, it is a poor substitute for four 741's in split-supply circuits.

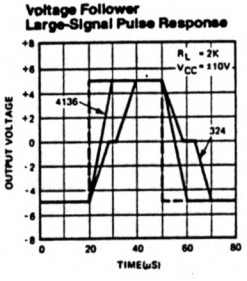
The simplified input circuit of the 4136 exhibits much lower noise than that of the 324 and exhibits no crossover distortion as compared with the 324 (see illustration). The 324 shows serious crossover distortion and pulse delay in attempting to handle a large-signal input pulse.



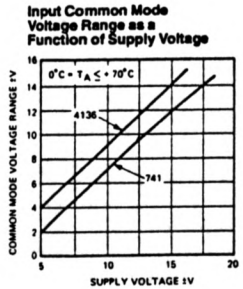
Comparative Cross-over Distortion

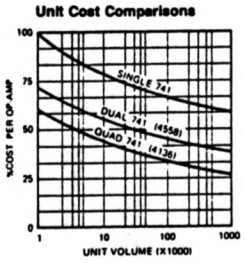






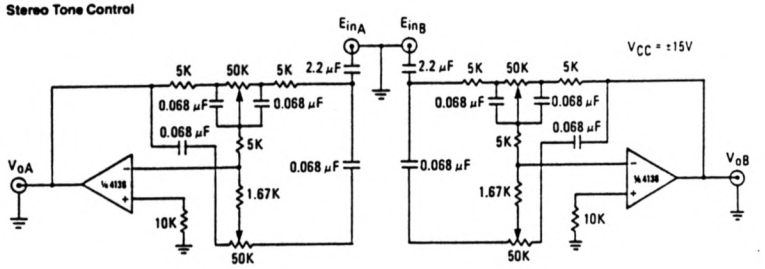
Typical Characteristics Curves Comparison



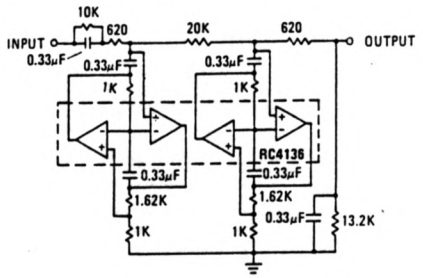


4136 TYPICAL APPLICATIONS

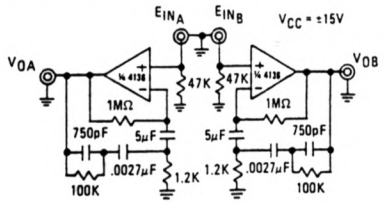
Stereo Tone Control



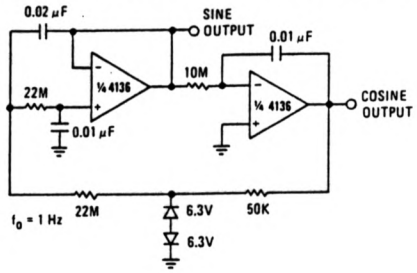
400 Hz Lowpass Butterworth Active Filter



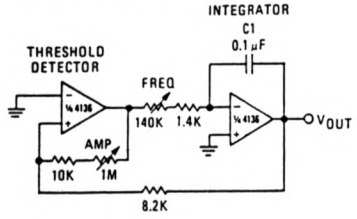
RIAA Preamplifier



Low Frequency Sine Wave Generator with Quadrature Output

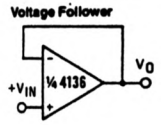


Triangular-Wave Generator

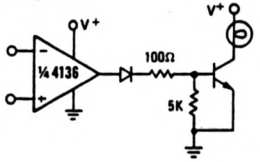


4136 TYPICAL APPLICATIONS

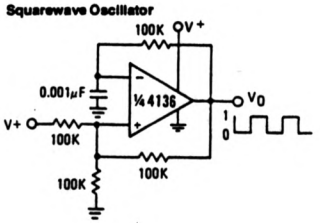
Voltage Follower



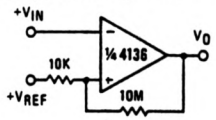
Lamp Driver



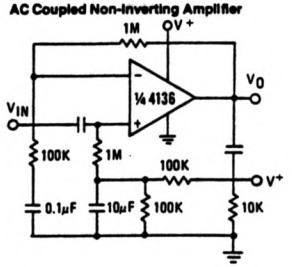
Squarewave Oscillator



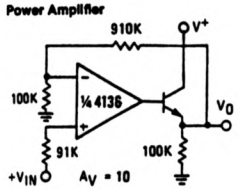
Comparator With Hysteresis



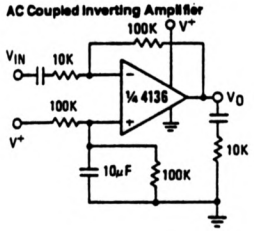
AC Coupled Non-Inverting Amplifier



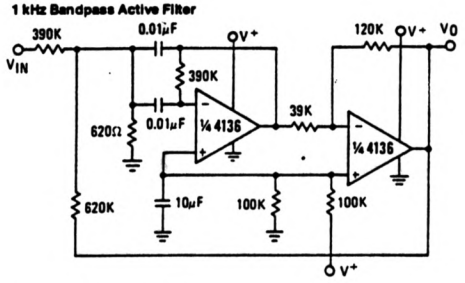
Power Amplifier



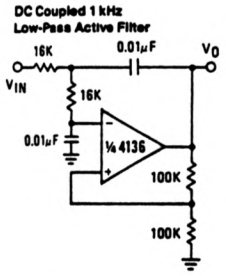
AC Coupled Inverting Amplifier



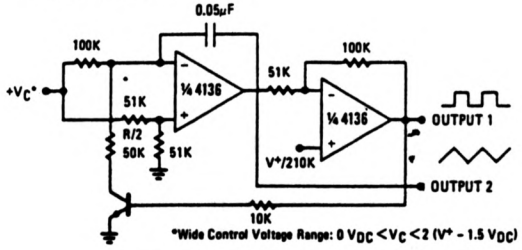
1 kHz Bandpass Active Filter



DC Coupled 1 kHz Low-Pass Active Filter

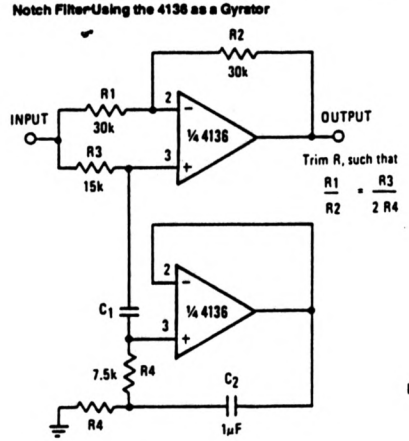


Voltage Controlled Oscillator (VCO)

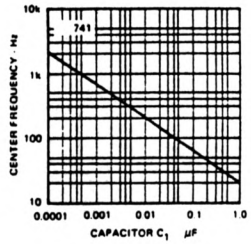


4136 TYPICAL APPLICATIONS

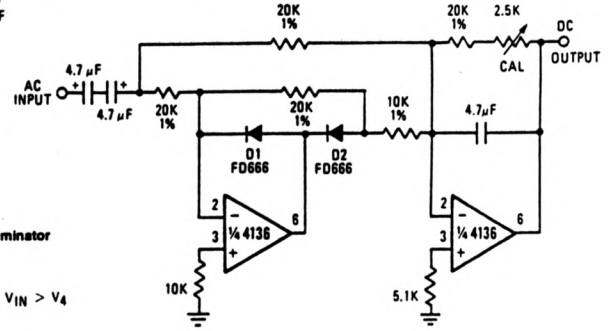
Notch Filter Using the 4136 as a Gyrator



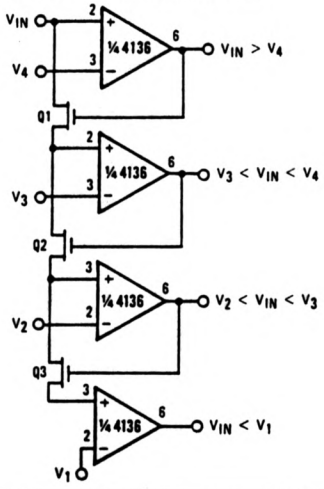
Notch Frequency as a Function of C1



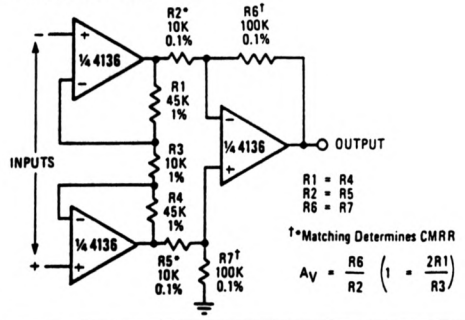
Full-Wave Rectifier and Averaging Filter



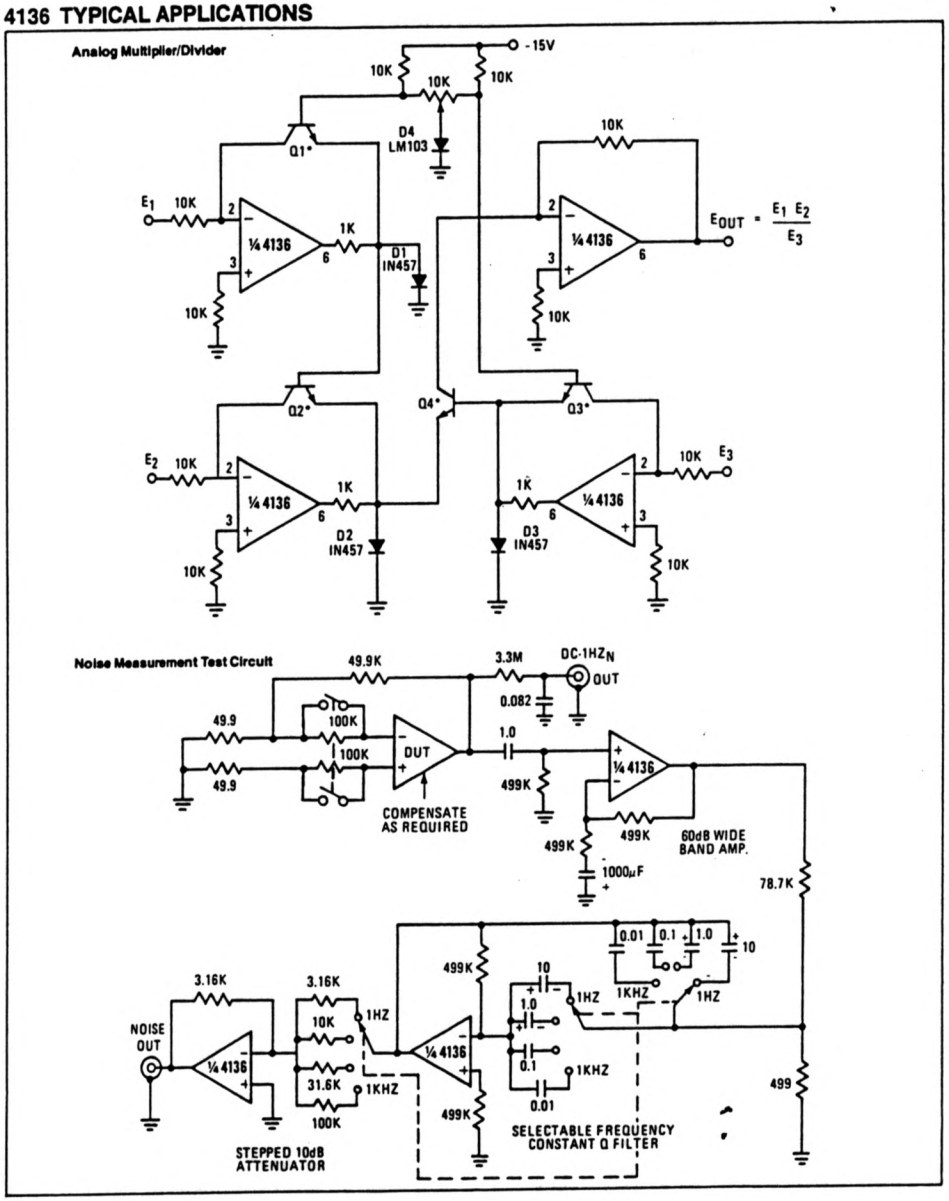
Multiple Aperture Window Discriminator



Differential Input Instrumentation Amplifier with High Common Mode Rejection



4136 TYPICAL APPLICATIONS



National Semiconductor

Operational Amplifiers/Buffers

LH0021/LH0021C 1.0 Amp Power Operational Amplifier
LH0041/LH0041C 0.2 Amp Power Operational Amplifier

General Description

The LH0021/LH0021C and LH0041/LH0041C are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH0021 will provide output currents in excess of one ampere at voltage levels of ±12V; the LH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

Features

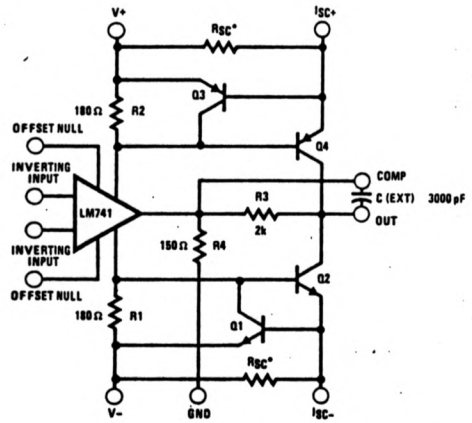
- Output current 1.0 Amp (LH0021)
  0.2 Amp (LH0041)
- Output voltage swing ±12V into 10Ω (LH0021)
  ±14V into 100Ω (LH0041)
- Wide full power bandwidth 15 kHz
- Low standby power 100 mW at ±15V
- Low input offset voltage and current 1 mV and 20 nA
- High slew rate 3.0V/μs
- High open loop gain 100 dB

The excellent input characteristics and high output capability of the LH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

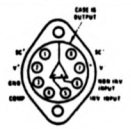
The LH0041 is particularly suited for applications such as torque driver for inertial guidance systems, diddle yoke driver for alpha-numeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

The LH0021 is supplied in a 8 pin TO-3 package rated at 20 watts with suitable heatsink. The LH0041 is supplied in both 12 pin TO-8 (2.5 watts with clip on heatsink) and a power 8 pin ceramic DIP (2 watts with suitable heatsink). The LH0021 and LH0041 are guaranteed over the temperature range of −55°C to +125°C while the LH0021C and LH0041C are guaranteed from −25°C to +85°C

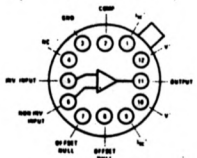
Schematic and Connection Diagrams



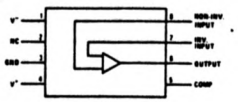
*RSC external on "G" and "K" packages. RSC internal on "J" package. Offset Null connections available only on "G" package.



Order Number
LH0021K or LH0021CK
See Package K08A



Order Number
LH0041G or LH0041CG
See Package H12B



Order Number
LH0041CJ
See Package HY08A

Absolute Maximum Ratings

Supply Voltage		±18V
Power Dissipation		See curves
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Peak Output Current (Note 2)	LH0021/LH0021C	2.0 Amps
	LH0041/LH0041C	0.5 Amps
Output Short Circuit Duration (Note 3)		Continuous
Operating Temperature Range	LH0021/LH0041	−55°C to +125°C
	LH0021C/LH0041C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

DC Electrical Characteristics for LH0021/LH0021C (Note 4)

PARAMETER	CONDITIONS	LIMITS LH0021 MIN	LH0021 TYP	LH0021 MAX	LH0021C MIN	LH0021C TYP	LH0021C MAX	UNITS
Input Offset Voltage	$R_S < 100\Omega$, $T_C = 25°C$		1.0	3.0		3.0	6.0	mV
	$R_S < 100\Omega$			5.0			7.5	mV
Voltage Drift with Temperature	$R_S < 100\Omega$		3	25		5	30	μV/°C
Offset Voltage Drift with Time			5			5		μV/week
Offset Voltage Change with Output Power			5	15		5	20	μV/watt
Input Offset Current	$T_C = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_C = 25°C$		100	300		200	500	nA
				1.0			1.0	μA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S < 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S < 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 1 k\Omega$, $T_C = 25°C$	100	200		100	200		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 100\Omega$,	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13.5	14		±13	±14		V
	$V_S = \pm 15V$, $R_L = 10\Omega$, $T_C = 25°C$	±11.0	±12		±10	±12		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 0.5\Omega$	0.8	1.2	1.6	0.8	1.2	1.6	Amps
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0021/LH0021C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000 pF$)

Slew Rate	$A_V = +1$, $R_L = 100\Omega$	0.8	3.0		1.0	3.0		V/μs
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	μs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		μs
Overload Recovery Time			3			3		μs
Harmonic Distortion	$f = 1 kHz$, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		μV rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA rms

DC Electrical Characteristics for LH0041/LH0041C (Note 4)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0041			LH0041C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S < 100\Omega$, $T_A = 25°C$		1.0	3.0		3.0	6.0	mV
	$R_S < 100\Omega$			5.0			7.5	mV
Voltage Drift with Temperature	$R_S < 100\Omega$		3			5		µV/°C
Offset Voltage Drift with Time			5			5		µV/week
Offset Voltage Change with Output Power			15			15		µV/watt
Offset Voltage Adjustment Range	(Note 5)		20			20		mV
Input Offset Current	$T_A = 25°C$		30	100		50	200	nA
				300			500	nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_A = 25°C$		100	300		200	500	nA
				1.0			1.0	µA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S < 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 1 k\Omega$, $T_A = 25°C$	100	200		100	200		V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13.0	14.0		±13.0	±14.0		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_A = 25°C$ (Note 6)		200	300		200	300	mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0041/LH0041C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000 pF$)

Slew Rate	$A_V = +1$, $R_L = 100\Omega$	1.5	3.0		1.0	3.0		V/µs
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	µs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		µs
Overload Recovery Time			3			3		µs
Harmonic Distortion	f = 1 kHz, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		µV/rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA/rms

Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.

Note 2: Rating applies for LH0041G and LH0021K with $R_{SC} = 0\Omega$.

Note 3: Rating applies as long as package power rating is not exceeded.

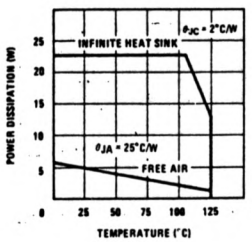
Note 4: Specifications apply for $\pm 5V \leq V_S \leq \pm 18V$, and $-55°C \leq T_C = \leq 125°C$ for LH0021K and LH0041G, and $-25°C \leq T_C \leq +85°C$ for LH0021CK, LH0041CG and LH0041CJ unless otherwise specified. Typical values are for 25°C only.

Note 5: TO-8 "G" packages only.

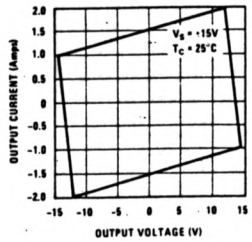
Note 6: Rating applies for "J" DIP package and for TO-8 "G" package with $R_{SC} = 3.3$ ohms.

Typical Performance Characteristics

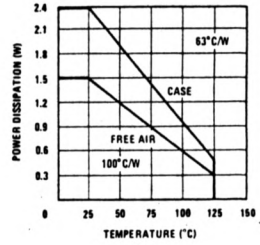
Power Derating-LH0021



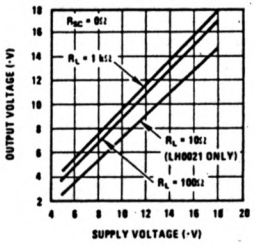
Safe Operating Area – LH0021



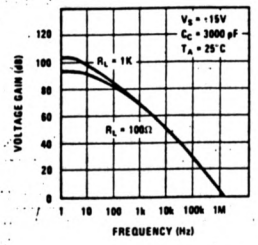
Package Power Dissipation LH0041/LH0041C



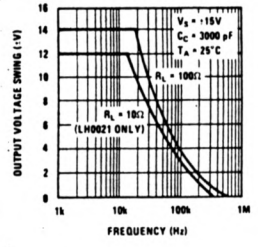
Output Voltage Swing



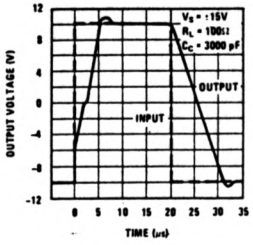
Open Loop Frequency Response



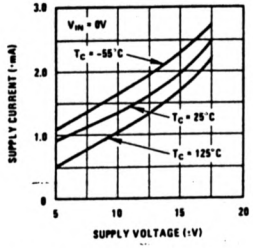
Large Signal Frequency Response



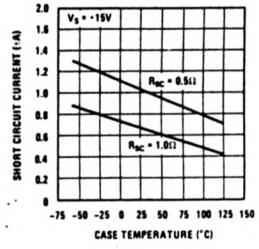
Voltage Follower Pulse Response



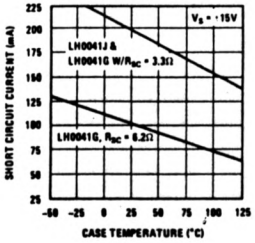
No Load Supply Current



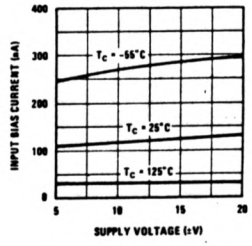
Short Circuit Current vs Temperature LH0021/LH0021C



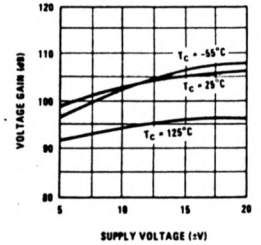
Short Circuit Current vs Temperature LH0041/LH0041C



Input Bias Current

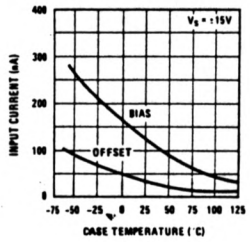


Voltage Gain

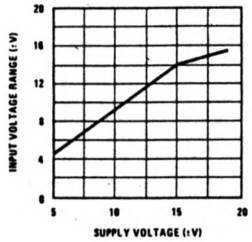


Typical Performance Characteristics (Cont'd)

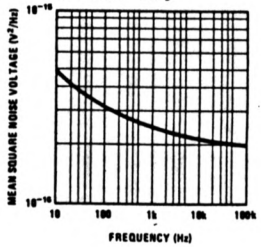
Input Current



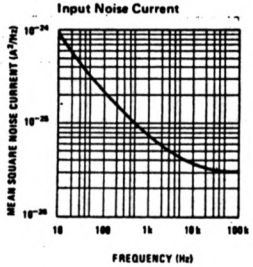
Input Voltage Range



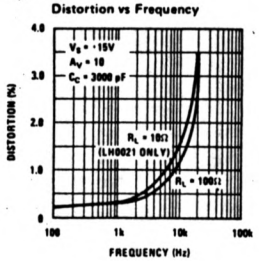
Input Noise Voltage



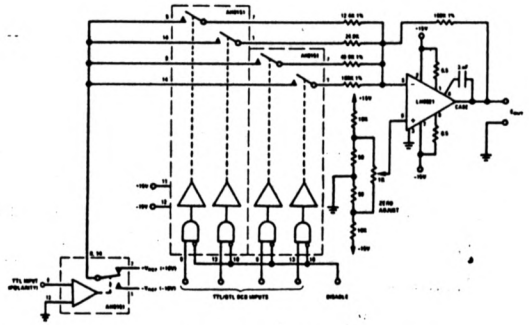
Input Noise Current



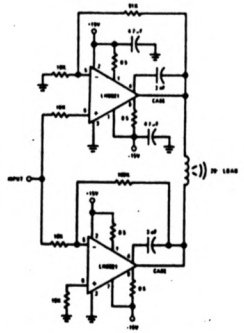
Distortion vs Frequency



Typical Applications

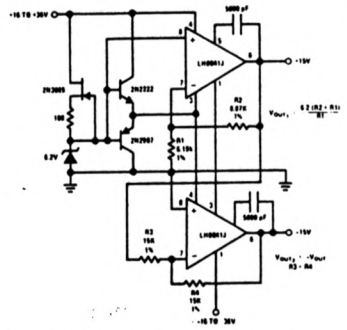


Programmable One Amp Power Supply

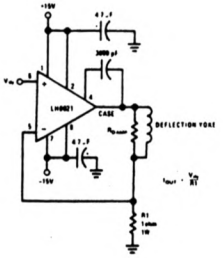


10 WATT (rms) Audio Amplifier

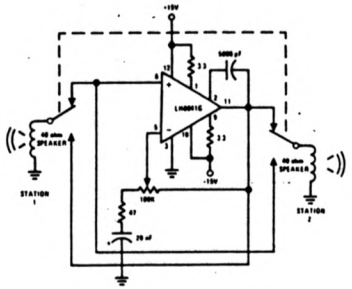
Typical Applications (Cont'd)



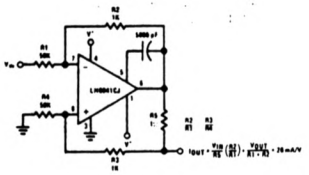
Dual Tracking One Amp Power Supply



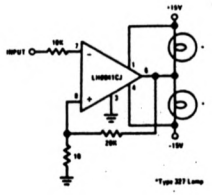
CRT Deflection Yoke Driver



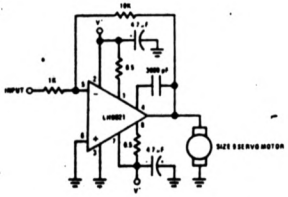
Two Way Intercom



Programmable High Current Source/Sink

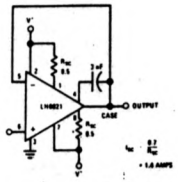


Power Comparator

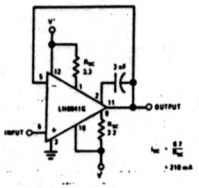


DC Servo Amplifier

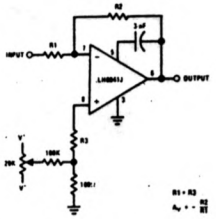
Auxiliary Circuits



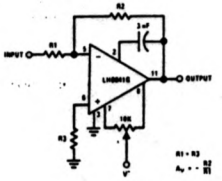
LH0021 Unity Gain Circuit with Short Circuit Limiting



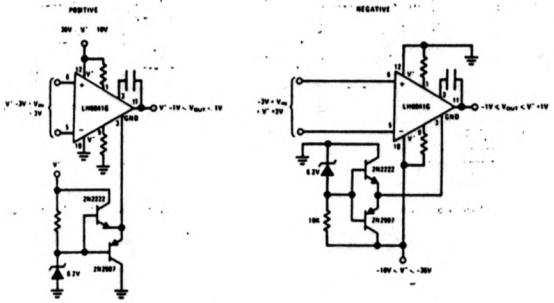
LH0041G Unity Gain with Short Circuit Limiting



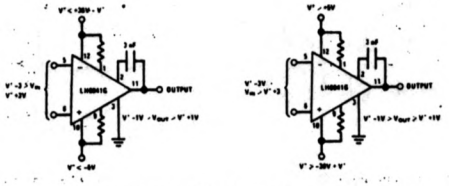
LH0041/LH0021 Offset Voltage Null Circuit (LH0041CJ Pin Connections Shown)*



LH0041G Offset Voltage Null Circuit *



Operation from Single Supplies



Operation from Non-Symmetrical Supplies

*For additional offset null circuit techniques see National Linear Applications Handbook.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3789 thru 2N3792

SILICON PNP POWER TRANSISTORS

. . . designed for medium-speed switching and amplifier applications. These devices feature:

- Total Switching Time @ 3 A ≈ 1 μs (typ)
- Two Gain Ranges:
  - h_{FE} (min) = 15 and 30 @ 3 A (2N3789, 2N3790)
  - 25 and 50 @ 1 A (2N3791, 2N3792)
- Low $V_{CE(sat)}$ = 0.5 V (typ) @ I_C = 4.0 A, I_B = 0.4 A
- Excellent Safe Area Limits
- Complementary NPN types available – 2N3713 thru 2N3716

10 AMPERE

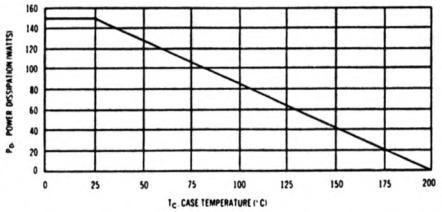
POWER TRANSISTORS
PNP SILICON

60-80 VOLTS
150 WATTS

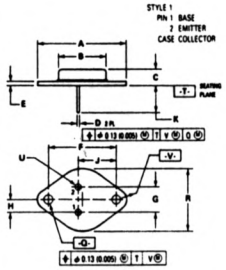
MAXIMUM RATINGS

Characteristic	Symbol	2N3789 2N3791	2N3790 2N3792	Unit
Collector-Base Voltage	V_{CB}	60	80	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current (Continuous)	I_C	10	10	Amps
Base Current (Continuous)	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resistance	θ_{JC}	1.17	1.17	°C/W
Junction Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +200		°C

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Limits are indicated by Figures 15, 16. Both limits are applicable and must be observed.



NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	--	39.37	--	1.550
B	--	21.08	--	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
R	3.84	4.19	0.151	0.165
S	--	26.67	--	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

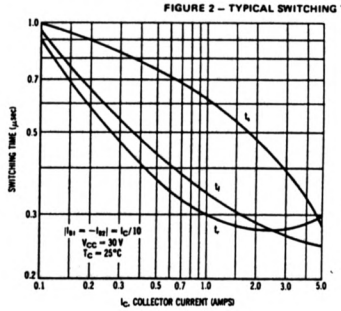
CASE 1-06
TO-204AA
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 200 mAdc, I_B = 0)	2N3789, 2N3791	$V_{CEO(sus)}$*	60	–	Vdc
	2N3790, 2N3792		80	–	
Collector-Emmiter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc)	2N3789, 2N3791		–	1	
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc)	2N3790, 2N3792		–	1	
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3789, 2N3791		–	5	
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3790, 2N3792		–	5	
Emitter-Base Cutoff Current (V_{EB} = 7 Vdc)	All Types	I_{EBO}	–	5	mAdc
DC Current Gain*		h_{FE}*			–
(I_C = 1 Adc, V_{CE} = 2 Vdc)	2N3789, 2N3790		25	90	
	2N3791, 2N3792		50	180	
(I_C = 3 Adc, V_{CE} = 2 Vdc)	2N3789, 2N3790		15	–	
	2N3791, 2N3792		30	–	
Collector-Emitter Saturation Voltage*		$V_{CE(sat)}$*			Vdc
(I_C = 4 Adc, I_B = 0.4 Adc)	2N3789, 2N3790		–	1.0	
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3791, 2N3792		–	1.0	
Base-Emitter On Voltage*		$V_{BE(on)}$*			Vdc
(I_C = 5 A, V_{CE} = 2 Vdc)	2N3789, 2N3790		–	2.0	
	2N3791, 2N3792		–	1.8	
(I_C = 10 Adc, V_{CE} = 4 Vdc)	All Types		–	4.0	
Current Gain – Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 MHz)	All Types	f_T	4		MHz

*Sweep Test: 1/2 sine wave cycle @ 60 cps.

FIGURE 2 – TYPICAL SWITCHING TIMES AND TEST CIRCUIT



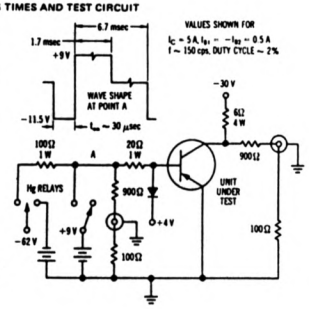


FIGURE 3 – CURRENT GAIN VARIATIONS

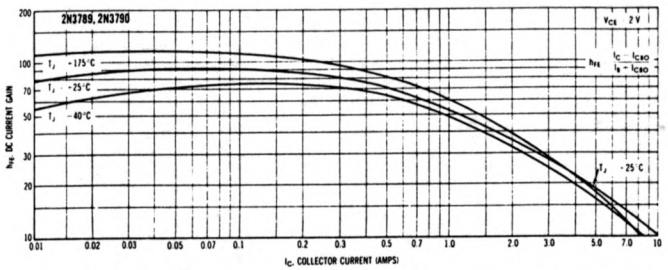


FIGURE 4 – CURRENT GAIN VARIATIONS

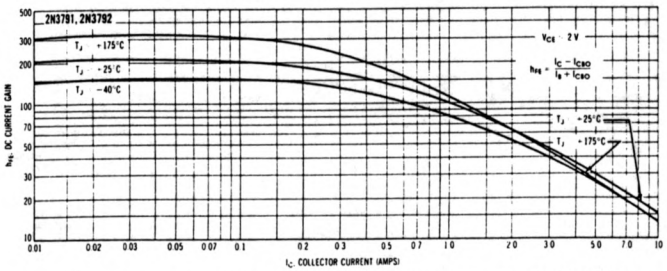


FIGURE 5 – SATURATION VOLTAGES

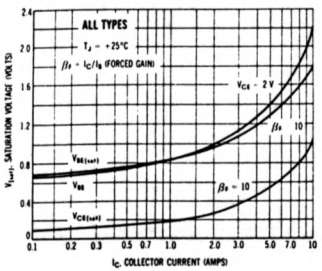
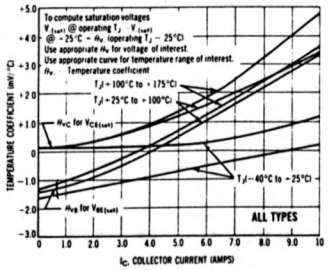


FIGURE 6 – TEMPERATURE COEFFICIENTS



SAFE OPERATING AREAS

FIGURE 7 – 2N3789, 2N3791

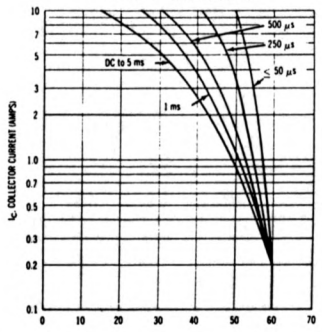
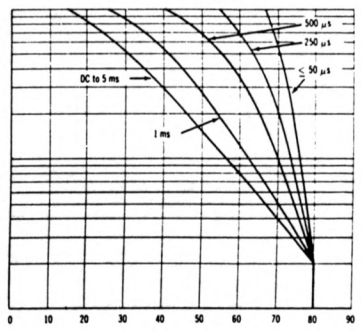


FIGURE 8 – 2N3790, 2N3792



V_{CE}, COLLECTOR EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

FIGURE 9 – CUT-OFF REGION TRANSCONDUCTANCE

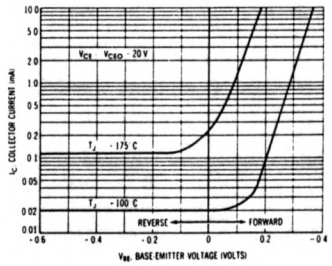
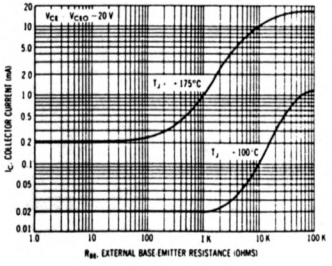


FIGURE 10 – COLLECTOR CUT-OFF CURRENT versus BASE-EMITTER RESISTANCE



National Semiconductor

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

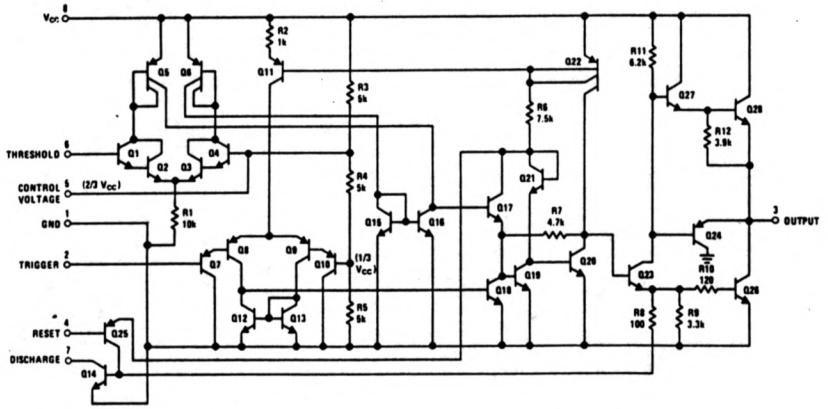
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

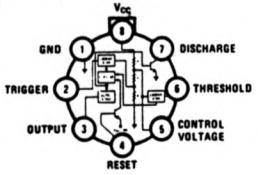
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagrams

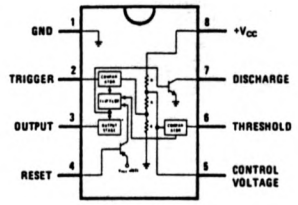
Metal Can Package



TOP VIEW

Order Number LM555H, LM555CH
See NS Package H08C

Dual-In-Line Package



TOP VIEW

Order Number LM555CN
See NS Package N08B
Order Number LM555J or LM555CJ
See NS Package J08A

Absolute Maximum Ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A, R_B = 1k to 100 k, C = 0.1μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

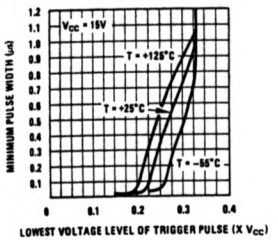
Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

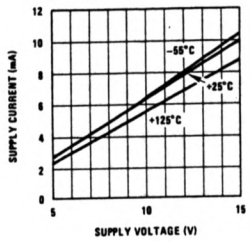
Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Typical Performance Characteristics

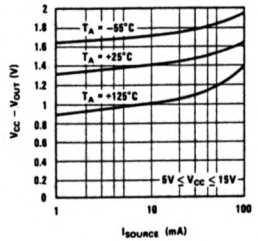
Minimum Pulse Width Required for Triggering



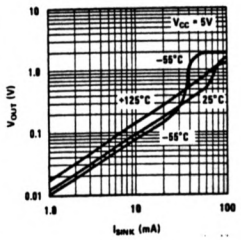
Supply Current vs Supply Voltage



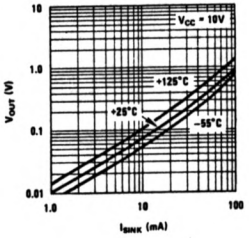
High Output Voltage vs Output Source Current



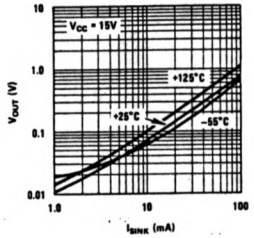
Low Output Voltage vs Output Sink Current



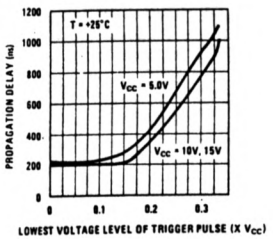
Low Output Voltage vs Output Sink Current



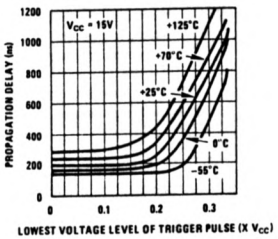
Low Output Voltage vs Output Sink Current



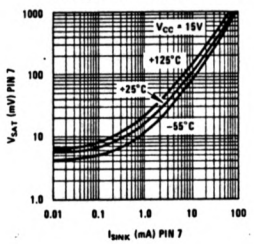
Output Propagation Delay vs Voltage Level of Trigger Pulse



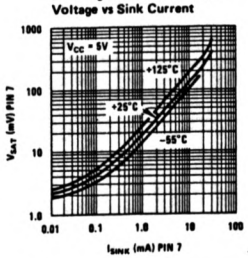
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

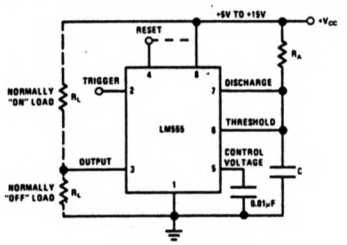


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_AC, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

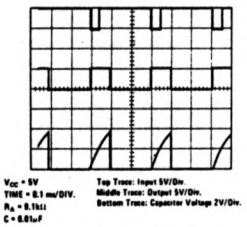


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a

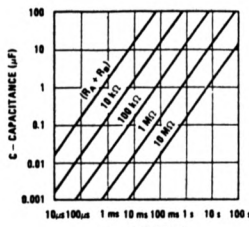


FIGURE 3. Time Delay

multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

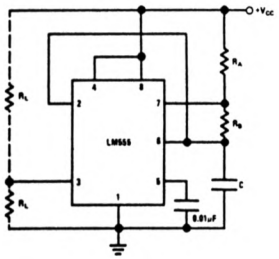


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

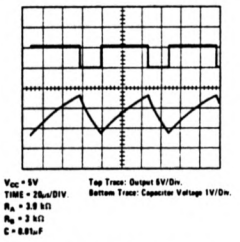


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

Applications Information (Continued)

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is: $D = \frac{R_B}{R_A + 2R_B}$

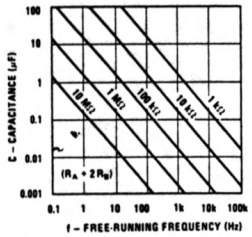


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

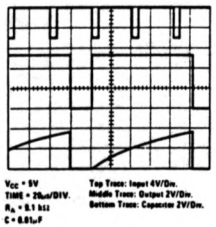


FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

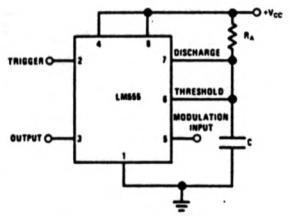


FIGURE 8. Pulse Width Modulator

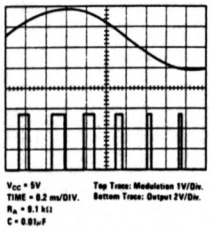


FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

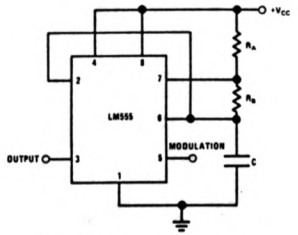


FIGURE 10. Pulse Position Modulator

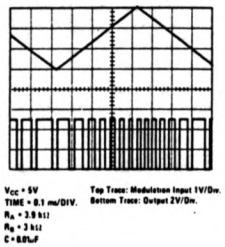


FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is

Applications Information (Continued)

generated. *Figure 12* shows a circuit configuration that will perform this function.

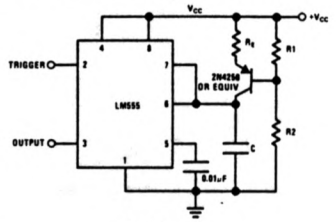


FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$V_{BE} \simeq 0.6V$

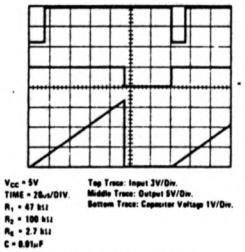


FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$[(R_A\ R_B)/(R_A + R_B)]\ \text{CLn}\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

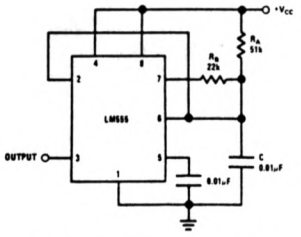


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

LOW-NOISE PRECISION OPERATIONAL AMPLIFIER — OP-27

FEATURES

- **Low Noise** ..... 80nV$_{p-p}$ (0.1Hz to 10Hz); 3nV/$\sqrt{Hz}$
- **Low Drift** ..... 0.2μV/°C
- **High Speed** ..... 2.8V/μs Slew Rate; 8MHz Gain Bandwidth
- **Low V_{OS}** 10μV
- **Excellent CMRR** ..... 126dB at V_{CM} of ±11V
- **High Open-Loop Gain** ..... 1.8 Million
- **Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets**

GENERAL DESCRIPTION

The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high-speed and low-noise. Offsets down to 25μV and drift of 0.6μV/° C maximim make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, e_n = 3.5nV/$\sqrt{Hz}$, at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8MHz and a 2.8V/μsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of ±10nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

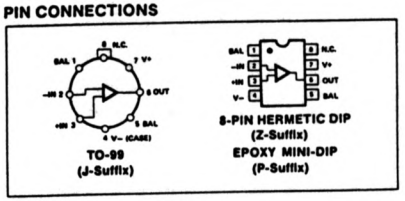
ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE HERMETIC TO-99 8-PIN	PACKAGE HERMETIC DIP 8-PIN	PACKAGE PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
25	OP27AJ*	OP27AZ*		MIL
25	OP27EJ	OP27EZ	OP27EP	IND/COM
60	OP27BJ*	OP27BZ*		MIL
60	OP27FJ	OP27FZ	OP27FP	IND/COM
100	OP27CJ*	OP27CZ*		MIL
100	OP27GJ	OP27GZ	OP27GP	IND/COM

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. See Section 3 for screening procedure.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. See Ordering Information, Section 2.

PIN CONNECTIONS

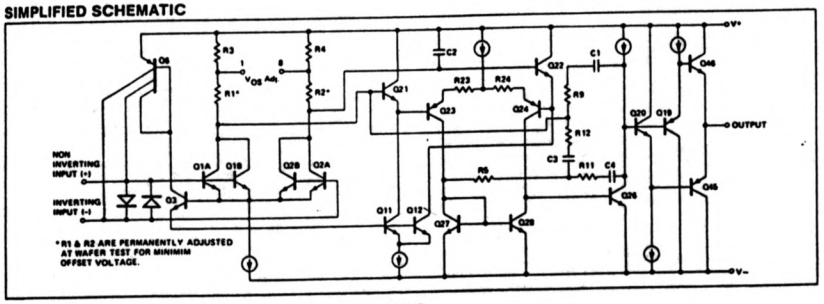


TO-99 (J-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

EPOXY MINI-DIP (P-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 3) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-27A, OP-27B, OP-27C (J, Z) ..... −55°C to +125°C
OP-27E, OP-27F, OP-27G (J, Z) ..... −25°C to +85°C
OP-27E, OP-27F, OP-27G (P) ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature ..... −65°C to +150°C

NOTES:
1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

2. The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

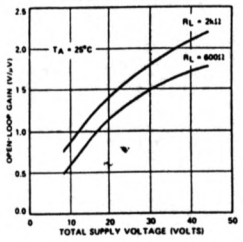
ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E MIN	OP-27A/E TYP	OP-27A/E MAX	OP-27B/F MIN	OP-27B/F TYP	OP-27B/F MAX	OP-27C/G MIN	OP-27C/G TYP	OP-27C/G MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	nV/$\sqrt{Hz}$
		f_O = 30Hz (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		f_O = 1000Hz (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3,6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	pA/$\sqrt{Hz}$
		f_O = 30Hz (Notes 3,6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	1.5	6	—	1.2	5	—	0.8	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		R_L ≥ 600Ω, V_O = ±10V	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		R_L ≥ 600Ω	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	R_L ≥ 2kΩ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/μs
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	V_O	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		R_P = 10kΩ	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

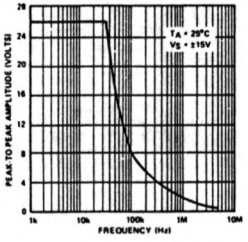
NOTES:
1. Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.

TYPICAL PERFORMANCE CHARACTERISTICS

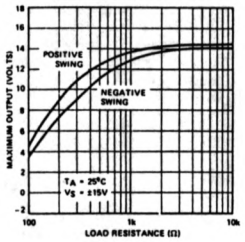
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



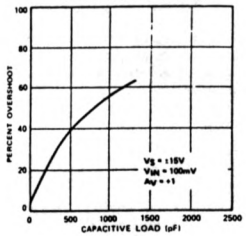
MAXIMUM OUTPUT SWING vs FREQUENCY



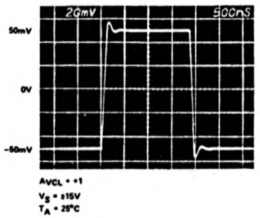
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



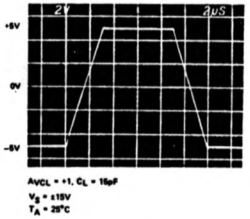
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



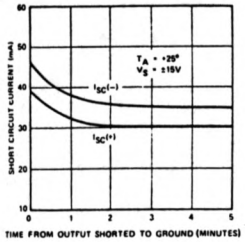
SMALL-SIGNAL TRANSIENT RESPONSE



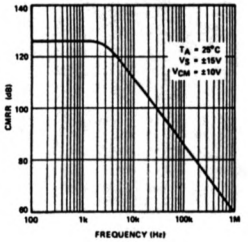
LARGE-SIGNAL TRANSIENT RESPONSE



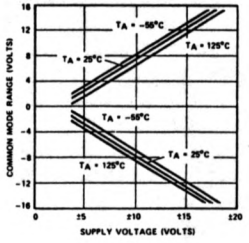
SHORT-CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

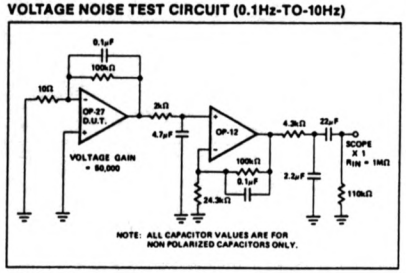


COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

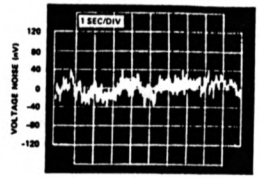


TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz)

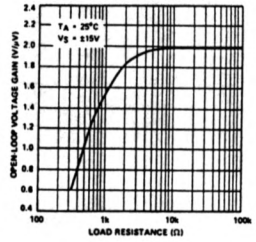


LOW-FREQUENCY NOISE

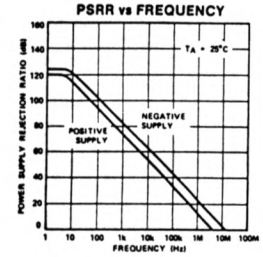


NOTE:
Observation time limited to 10 seconds.

OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



PSRR vs FREQUENCY



APPLICATIONS INFORMATION

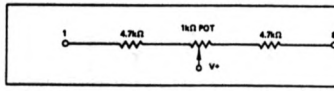
OP-27 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-27 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-27 operation. OP-27 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see Offset Nulling Circuit).

The OP-27 provides stable operation with load capacitances of up to 2000pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. The OP-27 is unity-gain stable.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-27 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see Offset Nulling Circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/°C. For example, the change in TCV_{OS} will be 0.33μV/°C if V_{OS} is adjusted to 100μV. The offset-voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjuction with fixed resistors. For example, the network below will have a ±280μV adjustment range.



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-27 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

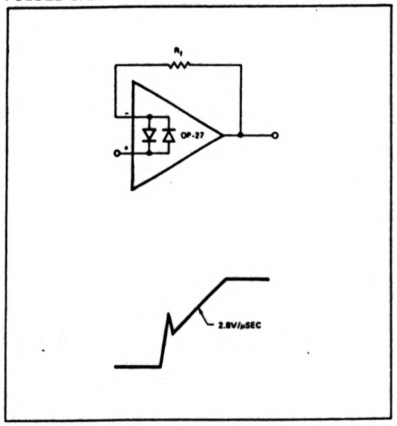
UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram below.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance (8pF) that creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f will eliminate this problem.

PULSED OPERATION



COMMENTS ON NOISE

The OP-27 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-27 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-27A/E has I_B and I_{OS} of only ±40nA and 35nA respectively at 25°C. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers prefer to use direct coupling. The high I_B, V_{OS}, TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-27's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-27 observed total noise with the noise performance of other devices in different circuit applications.

Total noise = $[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

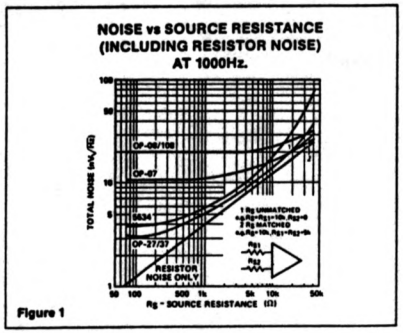


Figure 1

At $R_S < 1k\Omega$, the OP-27's low voltage noise is maintained. With $R_S > 1k\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of 20kΩ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-27 and OP-07 and OP-08 noise occurs in the 15-to-40kΩ region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to-5kΩ range depending on whether balanced or unbalanced source resistors are used (at 3kΩ the I_B, I_{OS} error also can be three times the V_{OS} spec.).

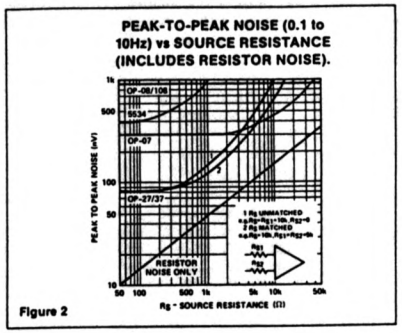


Figure 2

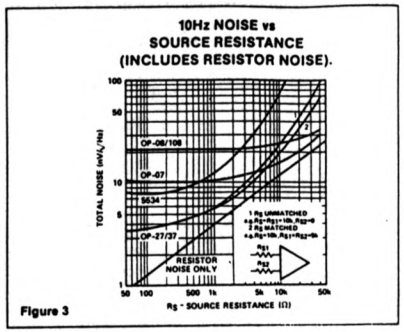


Figure 3

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-27 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-27 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

OPEN-LOOP GAIN

FREQUENCY AT:	OP-07	OP-27	OP-37
3Hz	100dB	124dB	125dB
10Hz	100dB	120dB	125dB
30Hz	90dB	110dB	124dB

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values.)

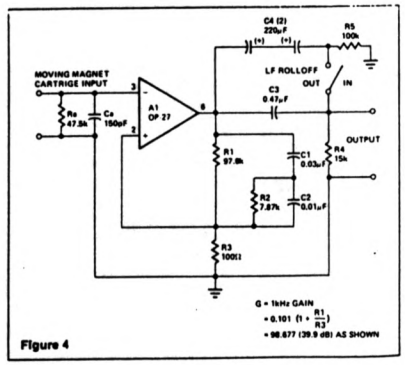


Figure 4

The OP-27 brings a 3.2nV/$\sqrt{Hz}$ voltage noise and 0.45 pA/$\sqrt{Hz}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω, which generates a voltage noise of 1.3nV/$\sqrt{Hz}$. The noise increases the 3.2nV/$\sqrt{Hz}$ of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101\ (1 + \frac{R_1}{R_3})$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C_3 and resistor R_4 form a simple −6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

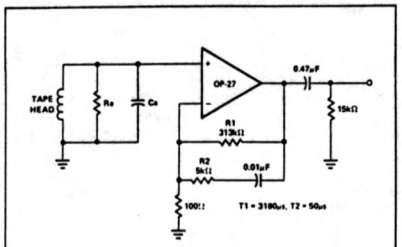


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz (T_2 = 50μs), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 80nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 100μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a 4nV/$\sqrt{Hz}$ noise, while the op amp generates a 3.2nV/$\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about 6nV/$\sqrt{Hz}$, equivalent to 0.9μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

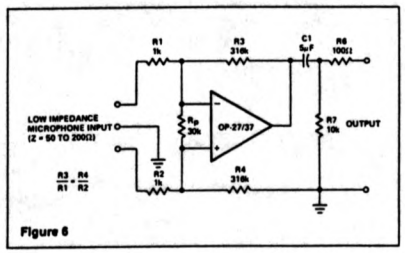


Figure 6

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally-compensated OP-27. T_1 is a JE-115K-E 150Ω/15kΩ transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

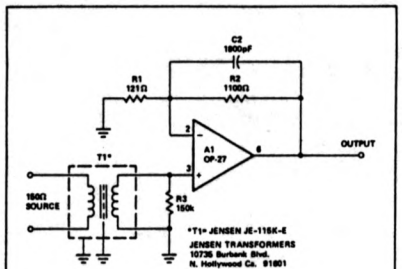


Figure 7

Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1. Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a 40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

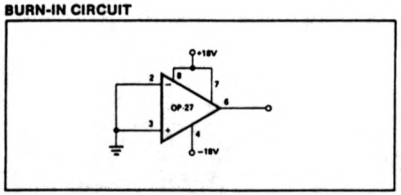
Capacitor C_2 and resistor R_2 form a 2μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2μs time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or −69.5 referenced to 1mV).

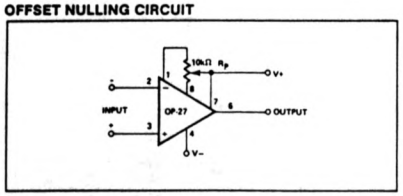
References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

D44E Series

POWER DARLINGTON TRANSISTORS NPN SILICON

. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.0 V (Max) @ 10 A
- High DC Current Gain — 1000 (Min) @ 5.0 Adc
- Complementary Pairs Simplifies Designs

DARLINGTON
10 AMPERE
POWER TRANSISTORS NPN SILICON
40-80 VOLTS
50 WATTS

MAXIMUM RATINGS

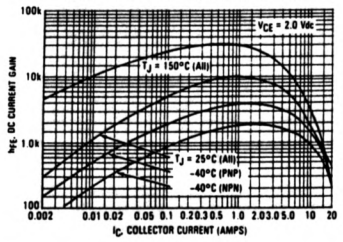
Rating	Symbol	D44E 1	D44E 3	Unit
Collector-Emitter Voltage	V_{CEO}	40	80	Vdc
Emitter Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak (1)	I_C	10 20		Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	50 1.67		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150		°C

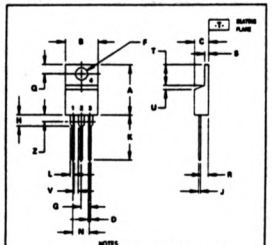
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 8.0 ms, Duty Cycle ≤ 50%

FIGURE 1 — TYPICAL DC CURRENT GAIN





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.71	0.018	0.028
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.05	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

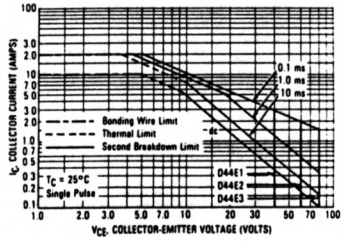
CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)	I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 7.0 Vdc)	I_{EBO}	—	—	1.0	μA
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	1000	—	—	—
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 10 mAdc) (I_C = 10 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	— —	— —	1.5 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 10 mAdc)	$V_{BE(sat)}$	—	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1.0 MHz)	C_{CBO}	—	—	130	pF
SWITCHING CHARACTERISTICS					
Delay and Rise Times (I_C = 10 Adc, I_{B1} = 20 mAdc)	$t_d + t_r$	—	0.6	—	μs
Storage Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_s	—	2.0	—	μs
Fall Time (I_C = 10 Adc, I_{B1} = I_{B2} = 20 mAdc)	t_f	—	0.5	—	μs

SAFE OPERATING AREA INFORMATION

FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA (NPN)



"A2" Board

HI-508-5 8-Channel CMOS Analog Multiplexer, Harris
HA-1608 + 10V Adjustable Voltage Reference

HARRIS

HI-508/509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

Features

- R_{ON} 180Ω
- Wide Analog Signal Range ..... ±15 V
- TTL/CMOS Compatible .....2.4 V (Logic "1")
- Fast Access .....250 ns
- Fast Settling (0.01%) .....600 ns
- 44V Maximum Power Supply
- Break-Before-Make Switching
- No Latch-Up
- Replaces DG508A/DG508AA and DG509A/DG509AA

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

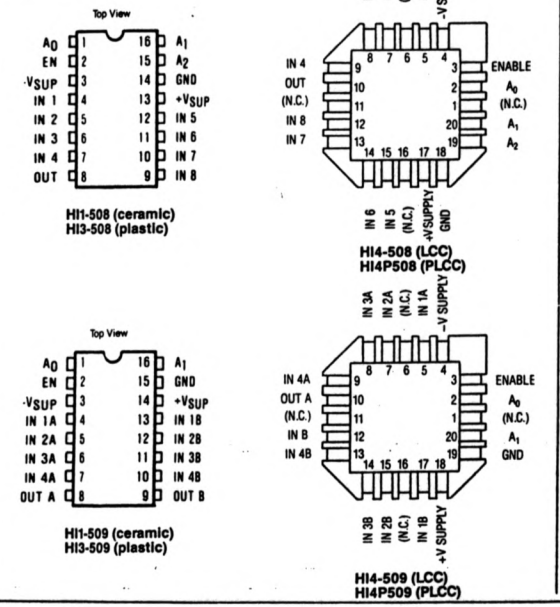
Switches are guaranteed to break-before-make, so that two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4 V for "1" and Maximum 0.8 V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

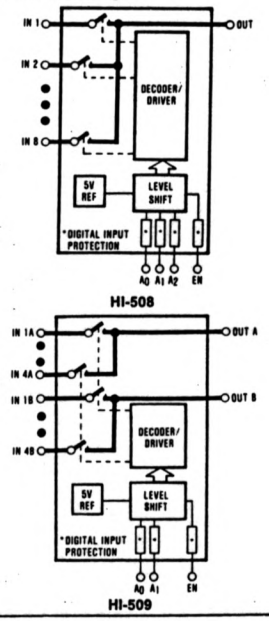
The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. The recommended supply voltage is ±15 V; however, reasonable performance is available down to ±7 V. Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC or 20 pin plastic LCC (PLCC) package. If input overvoltage protection is needed, the HI-508A/509A multiplexers are recommended. For further information, see Application Notes 520 and 521.

The HI-508/509 is offered in both commercial and military grades, suitable for spacecraft/military applications. For additional HI-Rel screening including 160 hour burn-in, specify the "–8" suffix. For further information see Application Notes 520 and 521. For MIL-STD-883 compliant parts, request the 508/883 or 509/883 data sheet.

Pinouts



Functional Diagrams



ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{Supply}(+)$ to $V_{Supply}(-)$	44 V
$V_{Supply}(+)$ to GND	22 V
$V_{Supply}(-)$ to GND	25 V
Digital Input Overvoltage:	
V_{EN}, V_A { $V_{Supply}(+)$	+4 V
$V_{Supply}(-)$ }	−4 V
or 20 mA, whichever occurs first.	
Analog Signal Overvoltage (Note 7)	
V_D, V_S { $V_{Supply}(+)$	+2 V
$V_{Supply}(-)$ }	−2 V

Continuous Current, S or D:	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max):	40 mA
Power Dissipation* (Cerdip)	1.09 W
Operating Temperature Range:	
HI-508/509-2,-8	−55°C to +125°C
HI-508/509-4	−25°C to +85°C
HI-508/509-5	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

*Derate 10.9 mW/°C above T_A = 75°C

ELECTRICAL CHARACTERISTICS Unless Otherwise Specified:

Supplies = +15 V, −15 V; V_{AH} (Logic Level High) = +2.4 V, V_{AL} (Logic Level Low) = +0.8 V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508/HI-509 −2, −8 MIN.	TYP.	MAX.	HI-508/509 −4, −5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		180	300		180	400	Ω
	Full			400			500	Ω
ΔR_{ON}, Any Two Channels	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold	Full			0.8			0.8	V
*V_{AH}, Input High Threshold	Full	2.4			2.4			V
*I_A, Input Leakage Current (High or Low) (Note 4)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OPEN}, Break-Before-Make Interval	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Turn-On	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Turn-Off	+25°C		250	500		250		ns
	Full			1000			1000	ns
t_S, Settling Time to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
"Off Isolation" (Note 5)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508	+25°C		22			22		pF
HI-509	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
*I+, Positive Supply Current (Note 6)	Full		1.5	2		1.5	2	mA
*I−, Negative Supply Current (Note 6))	Full		0.4	1		0.4	1	mA
P_D, Power Dissipation	Full			45			45	mW

*100% tested for Dash 8. Leakage currents not tested at −55°C.

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = −1 mA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
5. V_{EN} = 0.8 V, R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 100 kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
6. V_{EN}, V_A = 0 V or 2.4 V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the HARRIS HI-508A/509A multiplexers are recommended.

TRUTH TABLES

HI-508

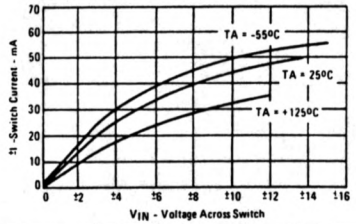
A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

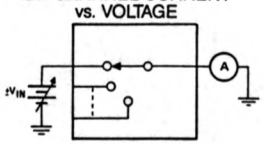
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

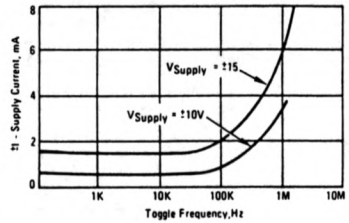


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

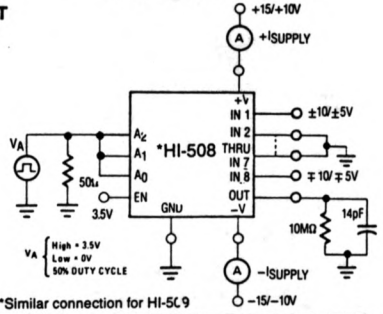


SUPPLY CURRENT vs. TOGGLE FREQUENCY



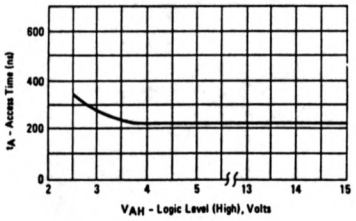
TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY



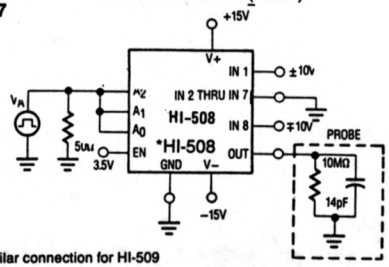
*Similar connection for HI-509

ACCESS TIME vs. LOGIC LEVEL (HIGH)



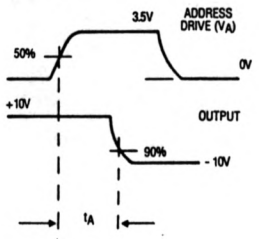
TEST CIRCUIT NO. 7

ACCESS TIME vs. LOGIC LEVEL (HIGH)

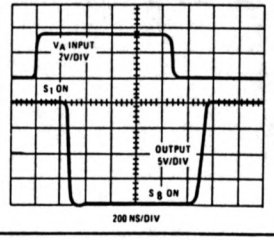


*Similar connection for HI-509

Switching Wav



ACCESS TIME

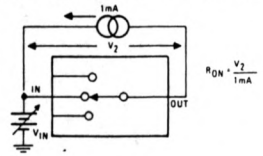


Performance Characteristics and Test Circuits

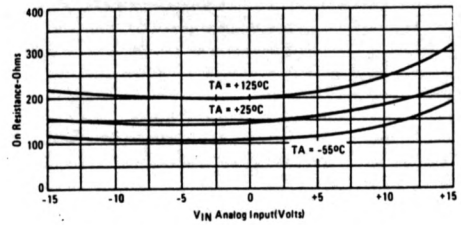
Unless Otherwise Specified; T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

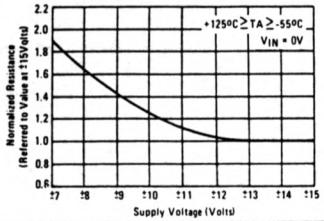
TEST CIRCUIT NO. 1



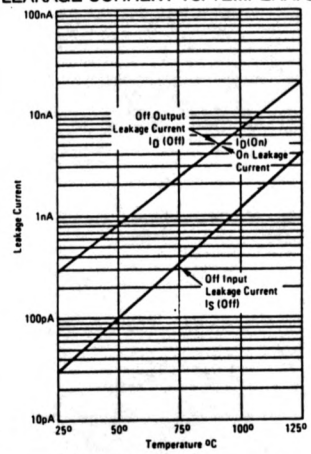
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



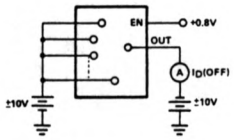
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



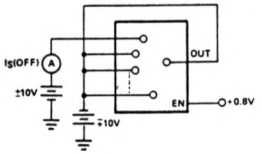
LEAKAGE CURRENT VS. TEMPERATURE



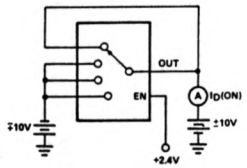
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 4*

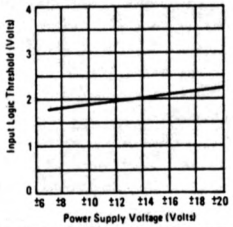


TEST CIRCUIT NO. 3*

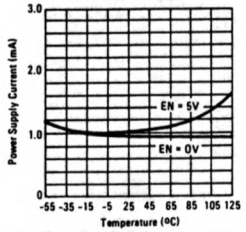


*Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)

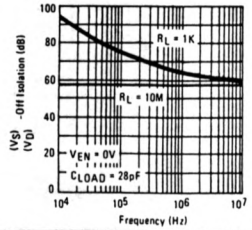
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE



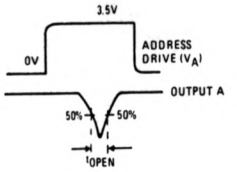
OFF ISOLATION vs. FREQUENCY



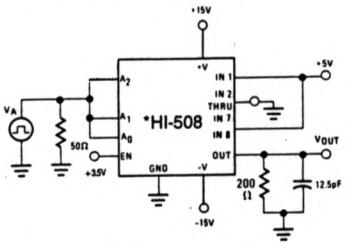
Switching Waveforms (continued)

TEST CIRCUIT NO. 8

ADDRESS DRIVE

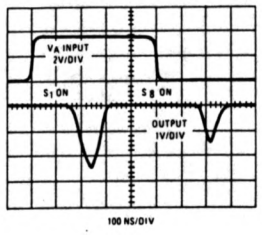


BREAK-BEFORE-MAKE DELAY (tOPEN)



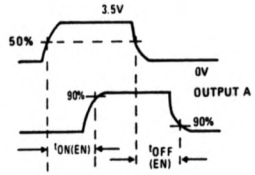
*Similar connection for HI-509

BREAK-BEFORE-MAKE DELAY(tOPEN)

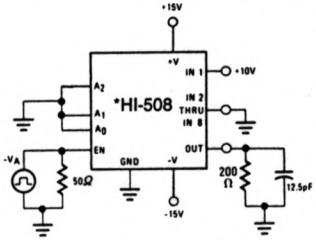


TEST CIRCUIT NO. 9

ENABLE DRIVE

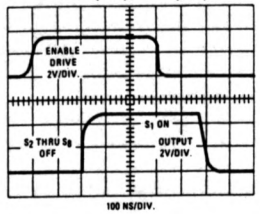


ENABLE DELAY (tON(EN),tOFF(EN)



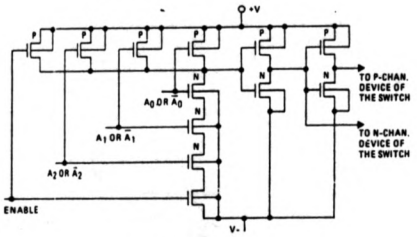
*Similar connection for HI-509

ENABLE DELAY (tON(EN),tOFF(EN))



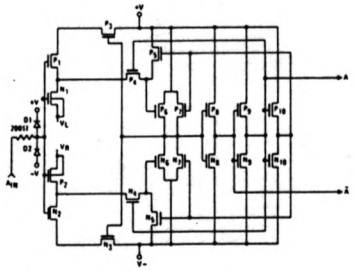
Schematic Diagrams

ADDRESS DECODER



Delete A_2 or $\overline{A_2}$ Input for HI-509

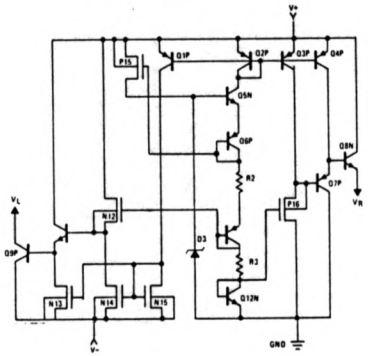
ADDRESS INPUT BUFFER LEVER SHIFTER



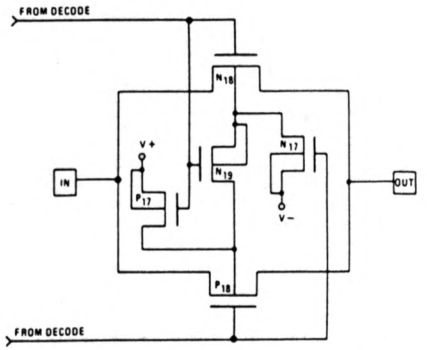
All N-Channel Bodies to V–
All P-Channel Bodies to V+ Unless Otherwise Indicated

Schematic Diagrams (continued)

TTL REFERENCE CIRCUIT

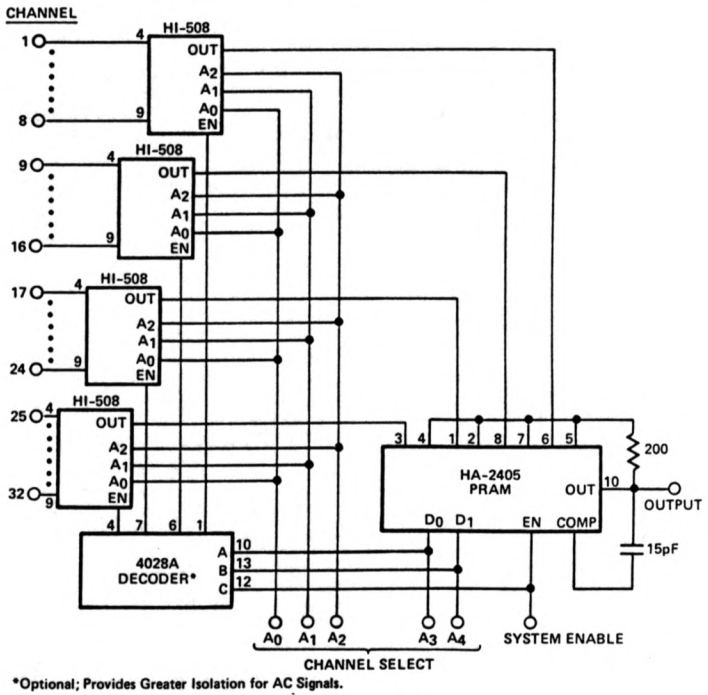


MULTIPLEX SWITCH



Applications

32 CHANNEL BUFFERED MULTIPLEXER



*Optional; Provides Greater Isolation for AC Signals.

HARRIS

HA-1608

+10V Adjustable Voltage Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- INITIAL ACCURACY +10V ± 0.010V
- OUTPUT VOLTAGE ERROR, TOTAL ±1/4 LSB
- LOW NOISE $20\mu V_{p-p}$
- WIDE INPUT RANGE 12V TO 30V
- LOW POWER DISSIPATION 30mW
- OUTPUT SHORT CIRCUIT PROTECTION
- ADJUSTABLE OUTPUT

APPLICATIONS

- AN ECONOMICAL EXTERNAL REFERENCE FOR: HI-5608; DAC 08; AD1408; AD559
- VOLTAGE REGULATOR REFERENCE
- PORTABLE BATTERY OPERATED EQUIPMENT
- NEGATIVE 10V REFERENCE

DESCRIPTION

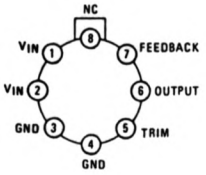
HA-1608 is a monolithic +10V adjustable voltage reference featuring accuracy and temperature stability specifications detailed exclusively for 8 bit data conversion systems. A stable +10V output is provided by a reference zener and buffer amplifier coupled with laser trimmed feedback and zener bias resistors. Long term stability is ensured through integration of all reference components into a monolithic design. Flexibility of HA-1608 is provided through an external trim control which allows the user to adjust the output voltage for binary or BCD applications without affecting overall performance.

These devices provide a total output voltage error of ± 1/4 LSB for 8 bit D/A or A/D converters. Low standby power (0.3mW) makes HA-1608 a natural selection for portable battery operated equipment, comparator references, and reference stacking circuits. These devices can also be used on -10V references.

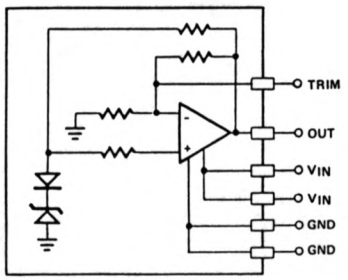
HA-1608 is packaged in 8 pin metal cans (TO-99) and the pinout is arranged for convenient replacement of other less accurate regulators in applications demanding minimal change with temperature and time. HA-1608-2 is specified for -55°C to +125°C operation while the HA-1608-5 operates from 0°C to +75°C.

PINOUT

TOP VIEW



FUNCTIONAL SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage	40V	Operating Temperature Range	
Output Short Circuit Duration	Indefinitely	HA-1608-2	-55°C to +125°C
Power Dissipation	500mW	HA-1608-5	0°C to +75°C
Storage Temperature Range	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS (Note 2) (V_{IN} = +15V, I_L = 0mA, unless otherwise specified)

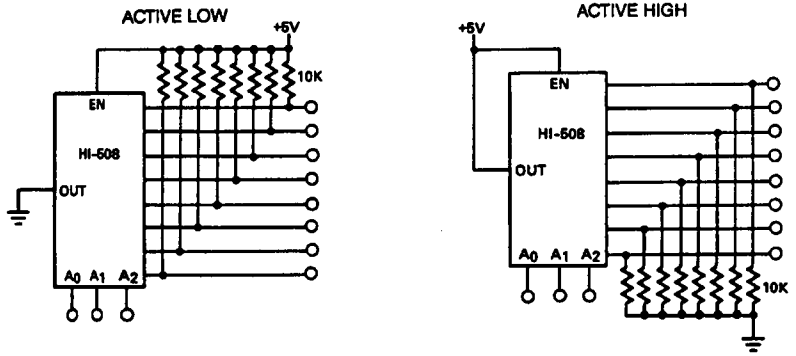
PARAMETER	TEMP	HA-1608-2 -55°C to +125°C MIN	TYP	MAX	HA-1608-5 0°C to +75°C MIN	TYP	MAX	UNITS
POWER INPUT CHARACTERISTICS								
Input Voltage Range, V_{IN}	Full	12	15	30	12	15	30	V
Quiescent Current, I_Q	25°C		1.9			1.9		mA
	Full			3.0			3.0	
REGULATED OUTPUT CHARA.'S								
Output Voltage, V_O	25°C	9.990	10.00	10.010	9.990	10.00	10.010	V
Output Load Current, I_L	Full	10	20		10	20		mA
Line Regulation (V_{IN} = 12V to 30V)	25°C		0.006			0.006		%/V
	Full			0.015			0.015	
Load Regulation (I_L = Open to 10mA)	25°C		0.006			0.006		%/mA
	Full			0.015			0.015	
Output Voltage Error Total I_L = 0mA (Relative to 8-bit accuracy, see Definition #3)	Full			±1/4 LSB			±1/4 LSB	
Output Noise Voltage, EN 0.1Hz to 10Hz	Full		35			35		μV_{p-p}
Dynamic Load Settling Time to ± 0.1%	25°C		2.5			2.5		µs
to ± 0.01%	25°C		5			5		
Warm-up Time (to ± 0.01%)	25°C		1			1		sec
	Full		3			3		

NOTES:

1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The specified electrical characteristics apply to suggested hook-up only.

Applications (continued)

ONE OF 8 DECODER



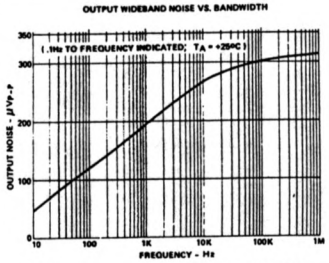
Die Characteristics

Transistor Count		243
Die Size		86 x 79 mils
Thermal Constants	θ_{ja}	92°C/W } For Ceramic Dip
	θ_{jc}	37°C/W }
Tie Substrate to:		−VSupply
Process:		CMOS - DI

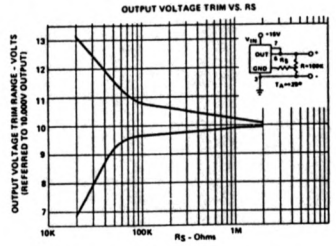
DEFINITIONS

1. Output Noise Voltage - the output noise voltage in a specified frequency band.
2. Quiescent Current, I_Q - the current required from the supply to operate the device at no load condition after the device is warmed-up.
3. Output Voltage Error Total - Includes effects of Noise Voltage, Line Regulation, and ΔV_0TC relative to 8-bit (10V output) resolution where: 1 LSB = one part in 256 or 39mV for a +10V output.
4. Line Regulation (%/V) - the ratio of the change in output voltage to the change in line voltage producing it; line regulation (%/V) = $[(\Delta V_0/10V) \times 100]/\Delta V_{IN}$.
5. Load Regulation (%/mA) - the ratio of the change in output voltage to the change in load current producing it; load regulation (%/mA) = $[(\Delta V_0/10V) \times 100]/\Delta mA$.
6. Dynamic Load Settling Time - the time required for the output to settle to within the specified error band for a change in the load current of 1mA.

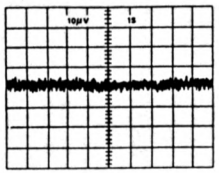
PERFORMANCE CURVES



OUTPUT WIDEBAND NOISE VS. BANDWIDTH



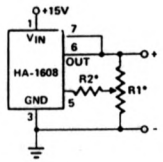
OUTPUT VOLTAGE TRIM VS. R_S



OUTPUT NOISE (0.1Hz TO 10Hz)

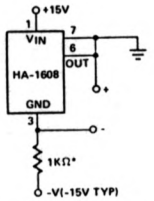
APPLICATIONS

TYPICAL HOOK-UP WITH OUTPUT TRIM



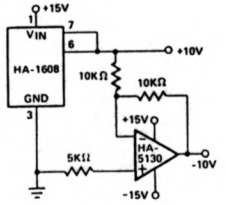
*NOTE: R_1 potentiometer value can be 10K to 100K R_2 can range from 10K to 2M .

NEGATIVE 10 VOLT REFERENCE



*NOTE: The value of R may reduce the output current available to less than that specified on the data sheet.

±10V REFERENCE



"A3" Board and Front Panel

LM3914N Dot/Bar Display Driver, National
HP 5082-7300 Numeric Indicator, Hewlett-Packard
HDSP-4820 10 Element Bar Graph Array, Hewlett-Packard
23102-2 Decade Switch, Digitran

National Semiconductor

LM3914 Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to 1/2%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

Features

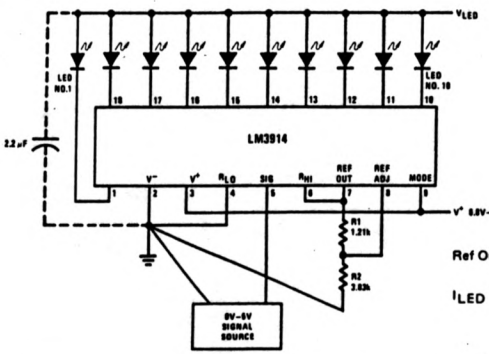
- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N is available in an 18-lead molded (N) package and the LM3914J comes in the 18-lead ceramic DIP.

The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Typical Applications

0V to 5V Bar Graph Meter



Note 1: Grounding method is typical of *all* uses. The 2.2 µF tantalum or 10 µF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} \simeq \frac{12.5}{R1}$$

Absolute Maximum Ratings

Power Dissipation (Note 5)		Input Signal Overvoltage (Note 3)	±35V
Ceramic DIP (J)	1W	Divider Voltage	−100 mV to V^+
Molded DIP (N)	625 mW	Reference Load Current	10 mA
Supply Voltage	25V	Storage Temperature Range	−55°C to +150°C
Voltage on Output Drivers	25V	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS (Note 1)	MIN	TYP	MAX	UNITS
COMPARATOR					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, I_{LED} = 1 mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)}$ = 2 mA, I_{LED} = 10 mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le V^+ - 1.5V$		10	50	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
VOLTAGE-DIVIDER					
Divider Resistance	Total, Pin 6 to 4	6.5	10	15	kΩ
Accuracy	(Note 2)		0.5	2	%
VOLTAGE REFERENCE					
Output Voltage	$0.1\ mA \le I_{L(REF)} \le 4\ mA$, $V^+ = V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$		0.01	0.03	%/V
Load Regulation	$0.1\ mA \le I_{L(REF)} \le 4\ mA$, $V^+ = V_{LED} = 5V$		0.4	2	%
Output Voltage Change With Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)}$ = 1 mA, V^+ = 5V		1		%
Adjust Pin Current			75	120	µA
OUTPUT DRIVERS					
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)}$ = 1 mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	V_{LED} = 5V, I_{LED} = 2 mA		0.12	0.4	mA
	V_{LED} = 5V, I_{LED} = 20 mA		1.2	3	mA
LED Current Regulation	$2V \le V_{LED} \le 17V$ I_{LED} = 2 mA		0.1	0.25	mA
	I_{LED} = 20 mA		1	3	mA
Dropout Voltage	$I_{LED(ON)}$ = 20 mA, V_{LED} = 5V, ΔI_{LED} = 2 mA			1.5	V
Saturation Voltage	I_{LED} = 2.0 mA, $I_{L(REF)}$ = 0.4 mA		0.15	0.4	V
Output Leakage, Each Collector	(Bar Mode) (Note 4)		0.1	10	µA
Output Leakage	(Dot Mode) (Note 4)				
Pins 10–18			0.1	10	µA
Pin 1		60	150	450	µA
SUPPLY CURRENT					
Standby Supply Current (All Outputs Off)	V^+ = 5V, $I_{L(REF)}$ = 0.2 mA		2.4	4.2	mA
	V^+ = 20V, $I_{L(REF)}$ = 1.0 mA		6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \le V^+ \le 20\ V_{DC}$
$3\ V_{DC} \le V_{LED} \le V^+$
$-0.015V \le V_{RLO} \le 12\ V_{DC}$
$-0.015V \le V_{RHI} \le 12\ V_{DC}$
$V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$
$0V \le V_{IN} \le V^+ - 1.5V$
T_A = +25°C, $I_{L(REF)}$ = 0.2 mA, V_{LED} = 3.0V, pin 9 connected to pin 3 (Bar Mode).

For higher power dissipations, pulse testing is used.

Note 2: Accuracy is measured referred to +10.000 V_{DC} at pin 6, with 0.000 V_{DC} at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+ or left open circuit. LED No. 10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

Note 5: The maximum junction temperature of the LM3914 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 75°C/W for the ceramic DIP (J package) and 120°C/W for the molded DIP (N package).

Definition of Terms

Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

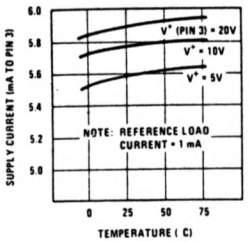
Line Regulation: The average change in reference output voltage over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage (V_{REF}) over the specified range of load current ($I_{L(REF)}$).

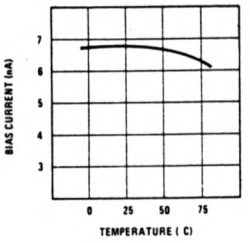
Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Typical Performance Characteristics

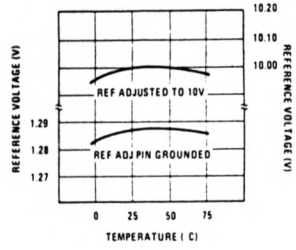
Supply Current vs Temperature



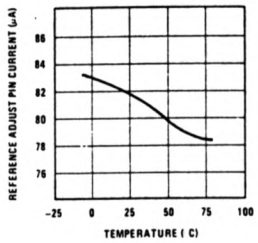
Operating Input Bias Current vs Temperature



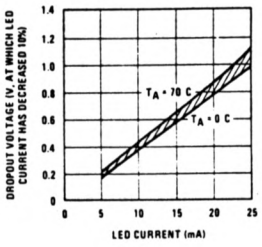
Reference Voltage vs Temperature



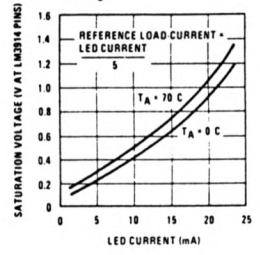
Reference Adjust Pin Current vs Temperature



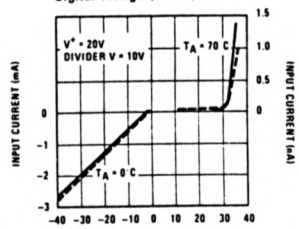
LED Current-Regulation Dropout



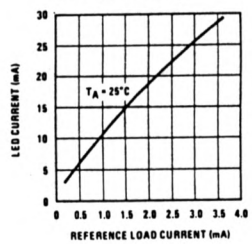
LED Driver Saturation Voltage



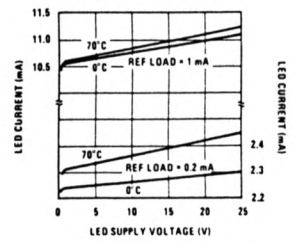
Input Current Beyond Signal Range (Pin 5)



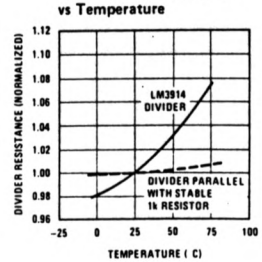
LED Current vs Reference Loading



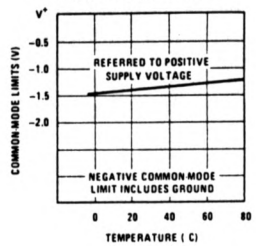
LED Driver Current Regulation



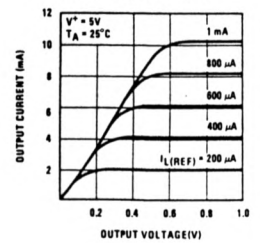
Total Divider Resistance vs Temperature



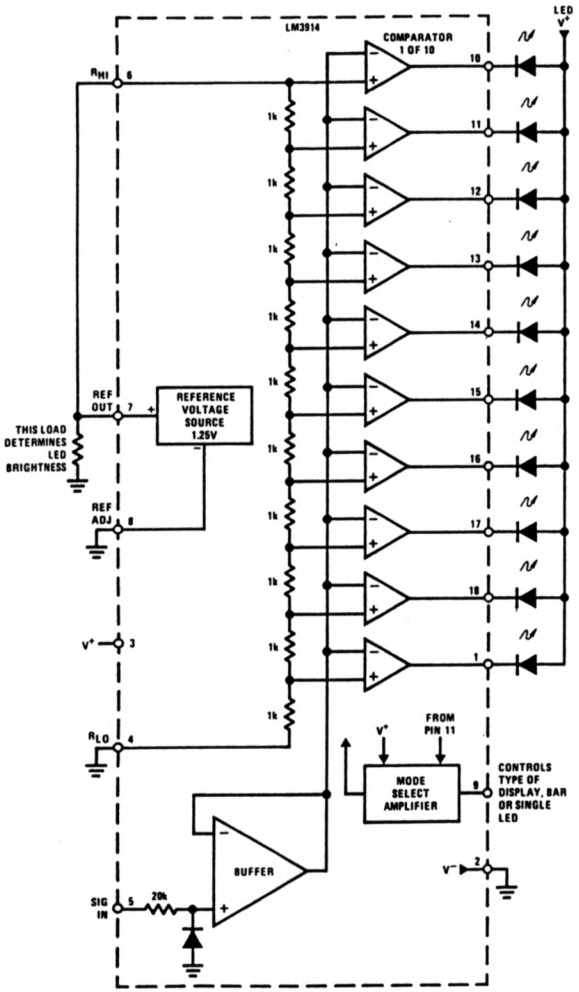
Common-Mode Limits



Output Characteristics



Block Diagram (Showing Simplest Application)



Functional Description

The simplified LM3914 block diagram is to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 125 mV that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are 1.5V below V^+ and no less than V^-. If an expanded scale meter display is desired, the total divider voltage can be as little as 200 mV. Expanded-scale meter displays are more accurate and the segments light uniformly only if bar mode is used. At 50 mV or more per step, dot mode is usable.

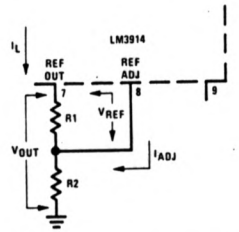
Internal Voltage Reference

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and

Functional Description (Continued)

REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes.

Current Programming

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

Mode Pin Use

Pin 9, the Mode Select input controls chaining of multiple LM3914s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

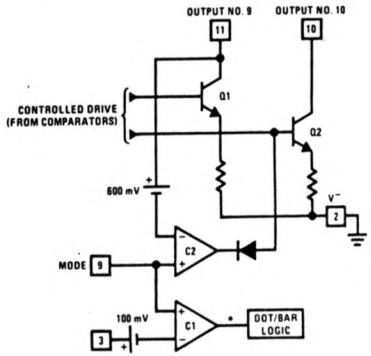
Dot Display, Single LM3914 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3914 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30, 40, or more LED displays. The last LM3914 driver in the chain will have pin 9 wired to pin 11. All previous drivers should have a 20k resistor in parallel with LED No. 9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



*High for bar

Dot or Bar Mode Selection

The voltage at pin 9 is sensed by comparator C1, nominally referenced to (V^+−100 mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

Dot Mode Carry

In order for the display to make sense when multiple LM3914s are cascaded in dot mode, special circuitry has been included to shut off LED No. 10 of the first device when LED No. 1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted on the following page.

As long as the input signal voltage is below the threshold of the second LM3914, LED No. 11 is off. Pin 9 of LM3914 No. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED No. 11, pin 9 of LM3914 No. 1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED No. 10.

Mode Pin Functional Description (Continued)

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED No. 9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED No. 11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3914 No. 1 is held low enough to force LED No. 10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED No. 11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED No. 10 yet small enough that LED No. 11 does not conduct significantly.

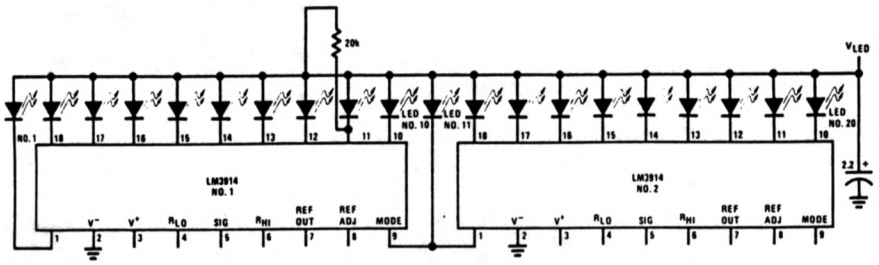
Other Device Characteristics

The LM3914 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA (2.5 mA max). However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3914 with a 1 mA reference pin load (1.3k), would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time between segments are all LEDs completely OFF in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range (Note 2). The change may be much more rapid between LED No. 10 of one device and LED No. 1 of a *second* device "chained" to the first.

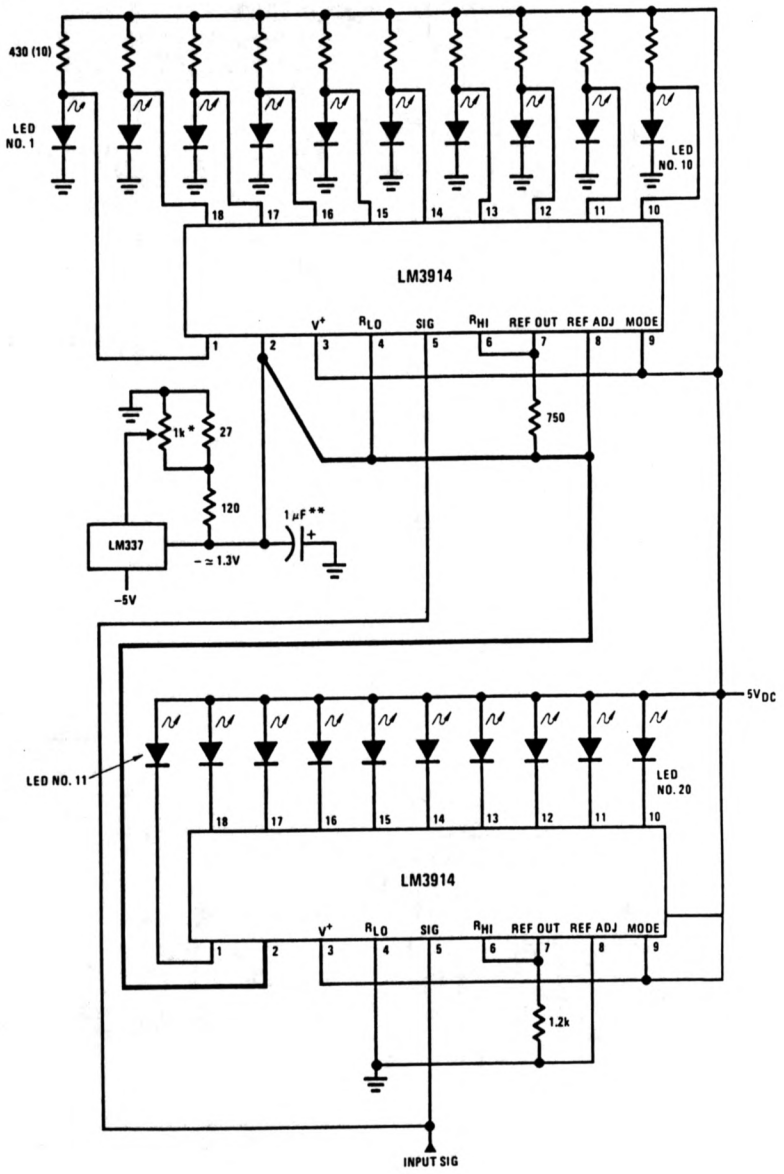
The LM3914 features individually current regulated LED driver transistors. Further internal circuitry detects when any driver transistor goes into saturation, and prevents other circuitry from drawing excess current. This results in the ability of the LM3914 to drive and regulate LEDs powered from a pulsating DC power source, i.e., largely unfiltered. (Due to possible oscillations at low voltages a nominal bypass capacitor consisting of a 2.2 μF solid tantalum connected from the pulsating LED supply to pin 2 of the LM3914 is recommended.) This ability to operate with low or fluctuating voltages also allows the display driver to interface with logic circuitry, opto-coupled solid-state relays, and low-current incandescent lamps.

Cascading LM3914s in Dot Mode



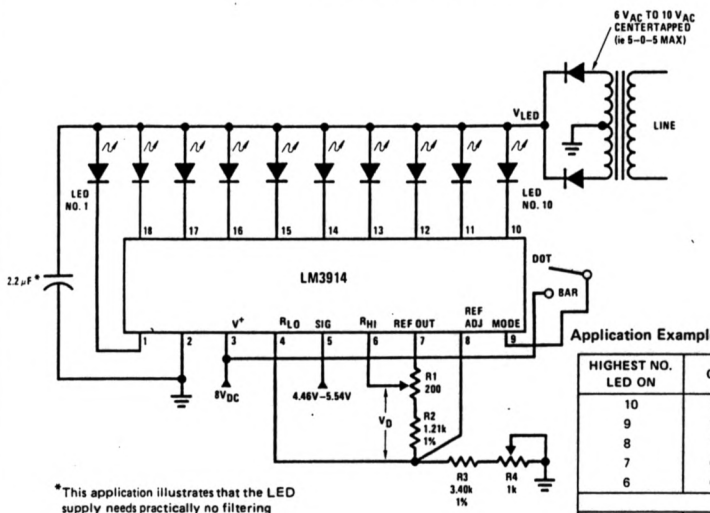
Typical Applications (Continued)

Zero-Center Meter, 20-Segment



Typical Applications (Continued)

Expanded Scale Meter, Dot or Bar



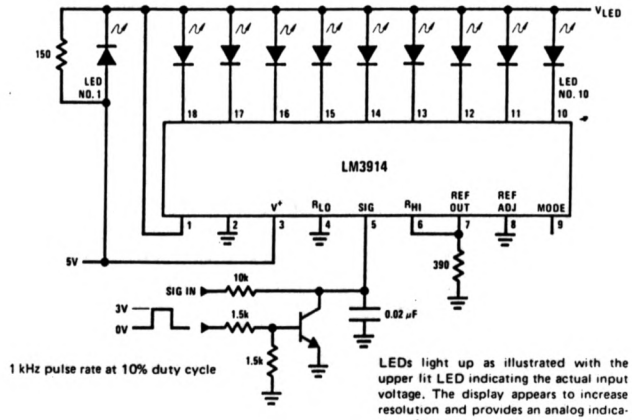
*This application illustrates that the LED supply needs practically no filtering

Calibration: With a precision meter between pins 4 and 6 adjust R1 for voltage V_D of 1.20V. Apply 4.94V to pin 5, and adjust R4 until LED No. 5 just lights. The adjustments are non-interacting.

Application Example: Grading 5V Regulators

HIGHEST NO. LED ON	COLOR	VOUT(MIN)
10	Red	5.54
9	Red	5.42
8	Yellow	5.30
7	Green	5.18
6	Green	5.06
5V		
5	Green	4.94
4	Green	4.82
3	Yellow	4.7
2	Red	4.58
1	Red	4.46

"Exclamation Point" Display

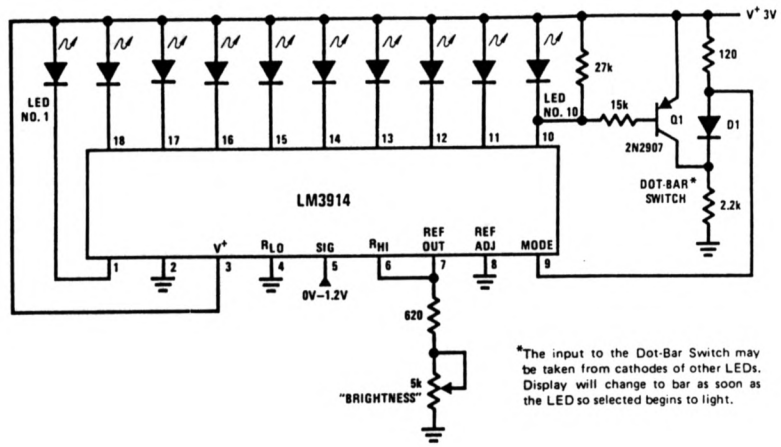


1 kHz pulse rate at 10% duty cycle

LEDs light up as illustrated with the upper lit LED indicating the actual input voltage. The display appears to increase resolution and provides an analog indication of overrange.

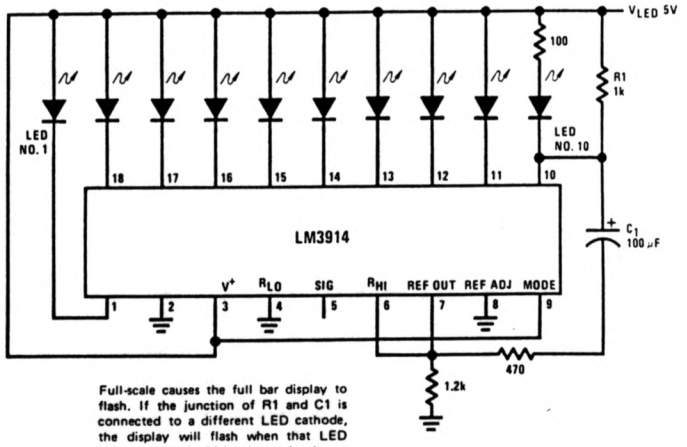
Typical Applications (Continued)

Indicator and Alarm, Full-Scale Changes Display From Dot to Bar



*The input to the Dot-Bar Switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

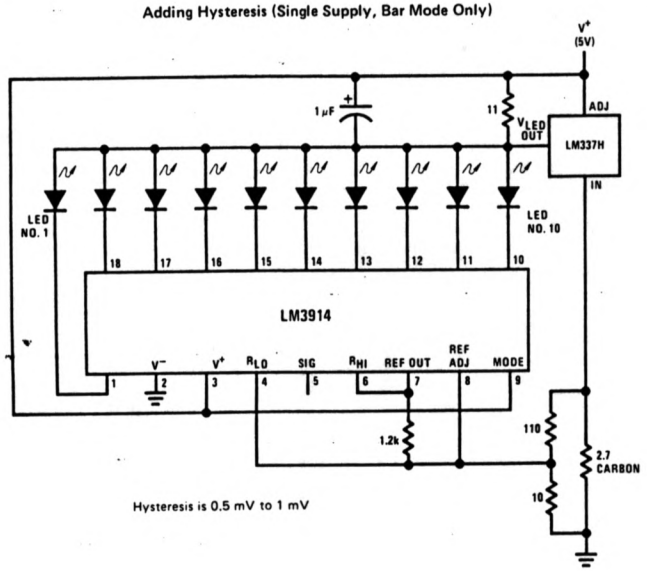
Bar Display with Alarm Flasher



Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

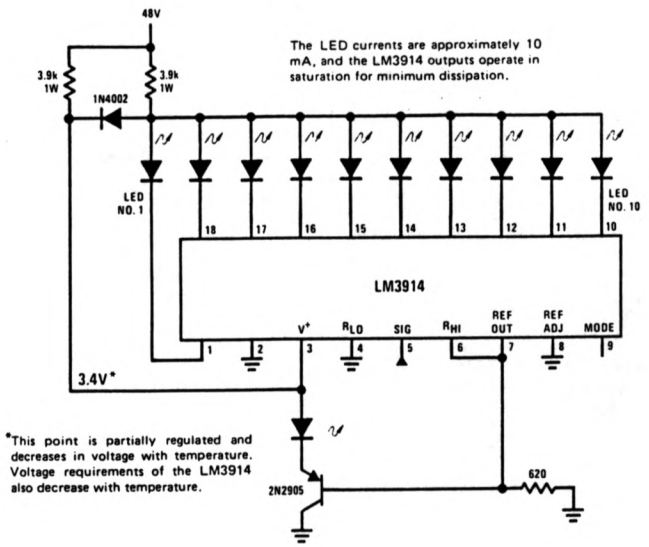
Typical Applications (Continued)

Adding Hysteresis (Single Supply, Bar Mode Only)



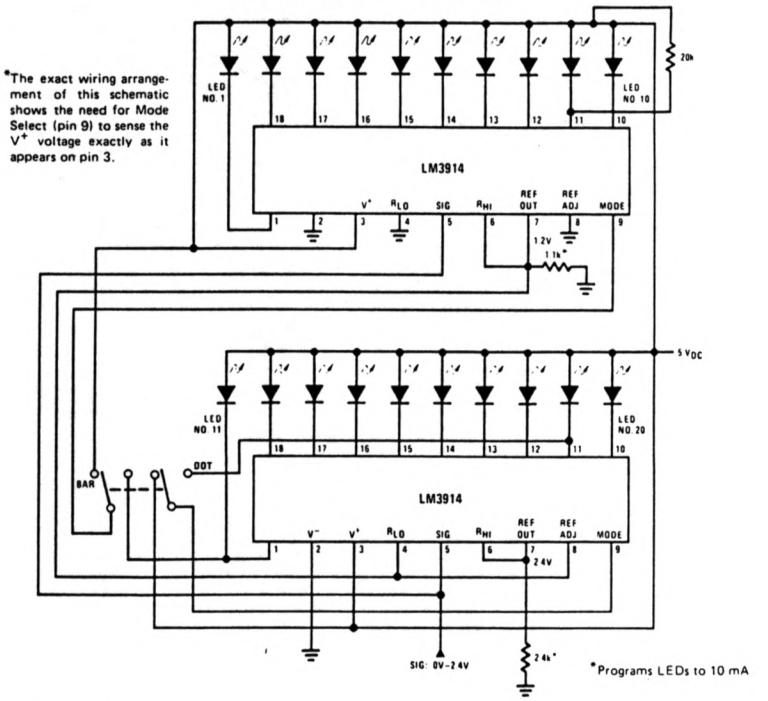
Hysteresis is 0.5 mV to 1 mV

Operating with a High Voltage Supply (Dot Mode Only)



Typical Applications (Continued)

20-Segment Meter with Mode Switch



Application Hints

Three of the most commonly needed precautions for using the LM3914 are shown in the first typical application drawing (see page 9-108) showing a 0V–5V bar graph meter. The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string (as illustrated) to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 µF to 2.2 µF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits (see Note 2, page 9-108). Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 µF capacitor, or up to 0.1 µF in noisy environments.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 µF solid tantalum capacitor to pin 2 of the LM3914.

Turning OFF of most of the internal current sources is accomplished by pulling positive on the reference with a current source or resistance supplying 100 µA or so. Alternately, the input signal can be gated OFF with a transistor switch.

Other special features and applications characteristics will be illustrated in the following applications schematics. Notes have been added in many cases, attempting to cover any special procedures or unusual characteristics of these applications. A special section called "Application Tips for the LM3914 Adjustable Reference" has been included with these schematics.

Application Hints (Continued)

APPLICATION TIPS FOR THE LM3914s ADJUSTABLE REFERENCE

Greatly Expanded Scale (Bar Mode Only)

Placing the LM3914s internal resistor divider in parallel with a section (≃230Ω) of a stable, low resistance divider greatly reduces voltage changes due to IC resistor value changes with temperature. Voltage V_1 should be trimmed to 1.1V first by use of R2. Then the voltage V_2 across the IC divider string can be adjusted to 200 mV, using R5 without affecting V_1. LED current will be approximately 10 mA.

Non-Interacting Adjustments for Expanded Scale Meter (4.5V to 5V, Bar *or* Dot Mode)

This arrangement allows independent adjustment of LED brightness regardless of meter span and zero adjustments.

First, V_1 is adjusted to 5V, using R2. Then the span (voltage across R4) can be adjusted to exactly 0.5V using R6 without affecting the previous adjustment.

R9 programs LED currents within a range of 2.2 mA to 20 mA after the above settings are made.

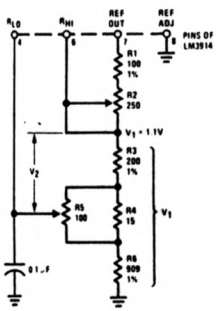
Adjusting Linearity of Several Stacked Dividers

Three internal voltage dividers are shown connected in series to provide a 30-step display. If the resulting analog meter is to be accurate and linear the voltage on each divider must be adjusted, preferably without affecting any other adjustments. To do this, adjust R2 first, so that the voltage across R5 is exactly 1V. Then the voltages across R3 and R4 can be independently adjusted by shunting each with selected resistors of 6 kΩ or higher resistance. This is possible because the reference of LM3914 No. 3 is acting as a constant current source.

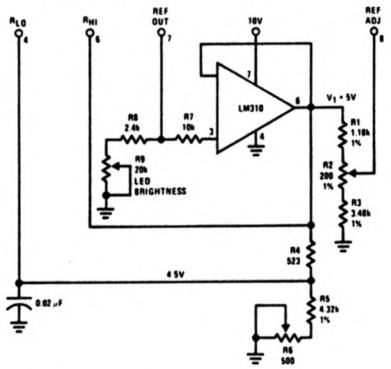
The references associated with LM3914s No. 1 and No. 2 should have their Ref Adj pins (pin 8) wired to ground, and their Ref Outputs loaded by a 620Ω resistor to ground. This makes available similar 20 mA current outputs to all the LEDs in the system.

If an independent LED brightness control is desired (as in the previous application), a unity gain buffer, such as the LM310, should be placed between pin 7 and R1, similar to the previous application.

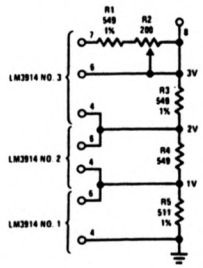
Greatly Expanded Scale (Bar Mode Only)



Non-Interacting Adjustments for Expanded Scale Meter (4.5V to 5V, Bar *or* Dot Mode)



Adjusting Linearity of Several Stacked Dividers

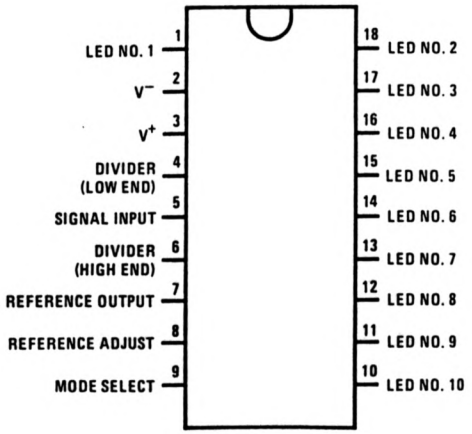


Other Applications

- "Slow" – fade bar or dot display (doubles resolution)
- 20-step meter with single pot brightness control
- 10-step (or multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Direction and rate indicator (to add to DVMs)
- Exclamation point display for power saving
- Graduations can be added to dot displays. Dimly light every other LED using a resistor to ground
- Electronic "meter-relay"–display could be circle or semi-circle
- Moving "hole" display–indicator LED is dark, rest of bar lit
- Drives vacuum-fluorescent and LCDs using added passive parts

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number 3914J
See NS Package J18A
Order Number LM3914N
See NS Package N18A

HEWLETT PACKARD

HEXADECIMAL AND NUMERIC INDICATORS

5082-7300
5082-7302
5082-7304
5082-7340

TECHNICAL DATA JANUARY 1986

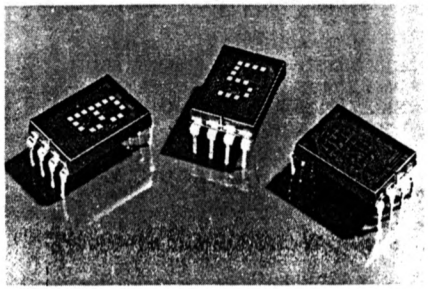
Features

- **NUMERIC 5082-7300/-7302**
  - 0-9, Test State, Minus Sign, Blank States
  - Decimal Point
    - 7300 Right Hand D.P.
    - 7302 Left Hand D.P.
- **HEXADECIMAL 5082-7340**
  - 0-9, A-F, Base 16 Operation
  - Blanking Control, Conserves Power
  - No Decimal Point
- **DTL/TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH 5-BIT MEMORY**
  - 8421 Positive Logic Input
- **4 x 7 DOT MATRIX ARRAY**
  - Shaped Character, Excellent Readibility
- **STANDARD DUAL-IN-LINE PACKAGE INCLUDING CONTRAST FILTER**
  - 15.2 mm x 10.2 mm (0.6 inch x 0.4 inch)
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  - Assures Uniformity of Light Output from Unit to Unit within a Single Category

Description

The HP 5082-7300 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide 7.4 mm (0.29 inch) displays for reliable, low-cost methods of displaying digital information.

The 5082-7300 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a "—" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point.



The 5082-7302 is the same as the 5082-7300, except that the decimal point is located on the left-hand side of the digit.

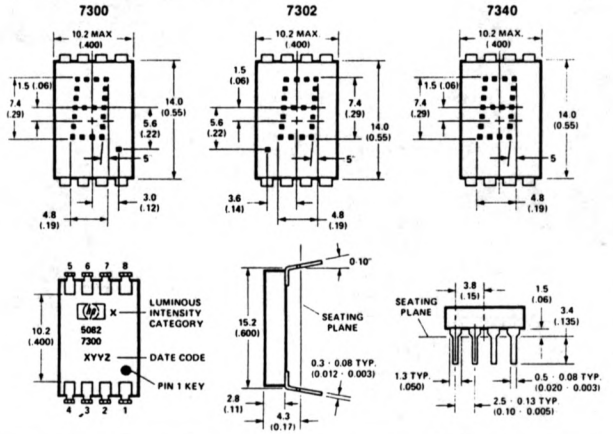
The 5082-7340 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7304 is a (±1) overrange display including a right-hand decimal point.

Applications

Typical applications include point-of-sale terminals, instrumentation, and computer system.

Package Dimensions



Pin	Function	
	5082-7300 and 7302 Numeric	5082-7340 Hexadecimal
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal Point	Blanking Control
5	Latch Enable	Latch Enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

Notes:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±0.38 mm (±0.015 inch).
3. Digit center line is ±0.25 mm (±0.01 inch) from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−40	+100	°C
Operating temperature, case [1,2]	T_C	−20	+85	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			230	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, case	T_C	-20		+85	°C
Enable Pulse Width	t_w	120			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_C = -20°C to +85°C, unless otherwise specified).

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral 5 and dp lighted)		112	170	mA
Power dissipation	P_T			560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_C=25°C	32	70		µcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			20	µA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			2.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+250	µA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+250	µA
Peak wavelength	λ_{PEAK}	T_C=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_C=25°C		640		nm
Weight				0.8		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: θ_{JA}=50°C/W; θ_{JC}=15°C/W; 2. θ_{C_A} of a mounted display should not exceed 35°C/W for operation up to T_C = +85°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_C=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific case temperature, $I_v(T_C)$ may be calculated from this relationship: $I_v(T_C)=I_v\ (25°C)\ e^{[-.0188/°C\ (T_C-25°C)]}$ 7. Applies only to 7340. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

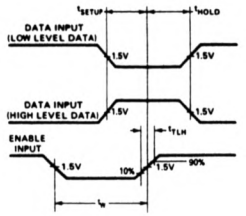


Figure 1. Timing Diagram of 5082-7300 Series Logic.

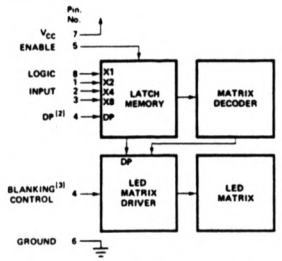


Figure 2. Block Diagram of 5082-7300 Series Logic.

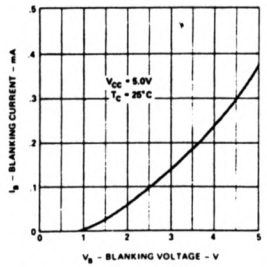


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7340.

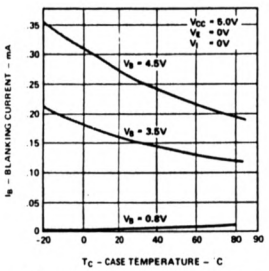


Figure 4. Typical Blanking Control Input Current vs. Temperature 5082-7340.

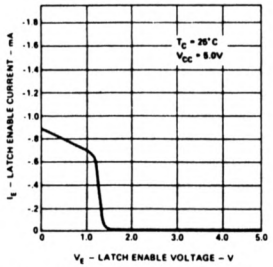


Figure 5. Typical Latch Enable Input Current vs. Voltage for the 5082-7300 Series Devices.

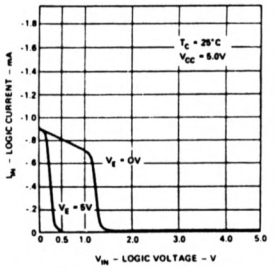


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage for the 5082-7300 Series Devices. Decimal Point Applies to 5082-7300 and -7302 Only.

TRUTH TABLE

BCD DATA[1]				5082-7300/7302	5082-7340
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	A	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	-	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F

DECIMAL PT.[2]	ON	V_{DP} = L
	OFF	V_{DP} = H
ENABLE[1]	LOAD DATA	V_E = L
	LATCH DATA	V_E = H
BLANKING[3]	DISPLAY-ON	V_B = L
	DISPLAY-OFF	V_B = H

Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7300 and 5082-7302 displays.
3. The blanking control input, B, pertains only to the 5082-7340 hexadecimal display. Blanking input has no effect upon display memory.

HEWLETT PACKARD

10-ELEMENT BAR GRAPH ARRAY

RED HDSP-4820
HIGH-EFFICIENCY RED HDSP-4830
YELLOW HDSP-4840
HIGH PERFORMANCE GREEN HDSP-4850
EMERALD GREEN HDSP-4890
MULTICOLOR HDSP-4832
MULTICOLOR HDSP-4836

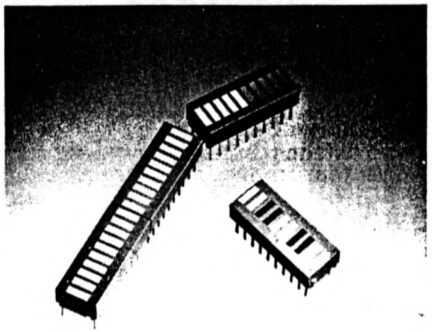
TECHNICAL DATA JANUARY 1986

Features

- CUSTOM MULTICOLOR ARRAY CAPABILITY
- MATCHED LEDs FOR UNIFORM APPEARANCE
- END STACKABLE
- PACKAGE INTERLOCK ENSURES CORRECT ALIGNMENT
- LOW PROFILE PACKAGE
- RUGGED CONSTRUCTION— RELIABILITY DATA SHEETS AVAILABLE
- LARGE, EASILY RECOGNIZABLE SEGMENTS
- HIGH ON-OFF CONTRAST, SEGMENT TO SEGMENT
- WIDE VIEWING ANGLE
- CATEGORIZED FOR LUMINOUS INTENSITY
- HDSP-4832/-4836/-4840/-4850/-4890 CATEGORIZED FOR DOMINANT WAVELENGTH

Applications

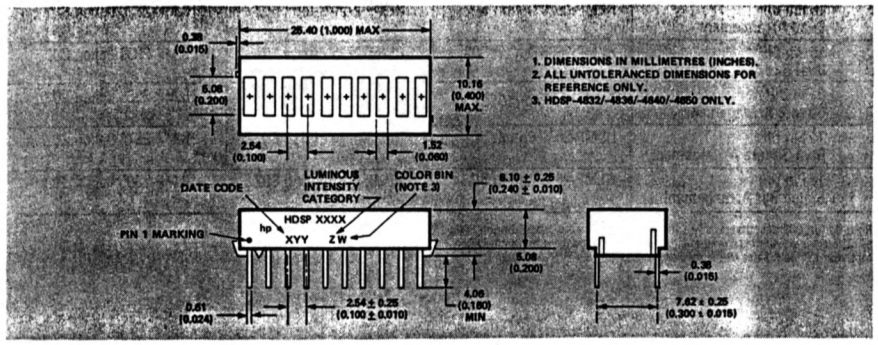
- INDUSTRIAL CONTROLS
- INSTRUMENTATION
- OFFICE EQUIPMENT
- COMPUTER PERIPHERALS
- CONSUMER PRODUCTS



Description

These 10-element LED arrays are designed to display information in easily recognizable bar graph form. The packages are end stackable and therefore capable of displaying long strings of information. Use of these bar graph arrays eliminates the alignment, intensity, and color matching problems associated with discrete LEDs. The HDSP-4820/-4830/-4840/-4850/-4890 each contain LEDs of just one color. The HDSP-4832/-4836 are multicolor arrays with High-Efficiency Red, Yellow, and Green LEDs in a single package. CUSTOM MULTICOLOR ARRAYS ARE AVAILABLE WITH MINIMUM DELIVERY REQUIREMENTS. CONTACT YOUR LOCAL DISTRIBUTOR OR HP SALES OFFICE FOR DETAILS.

Package Dimensions

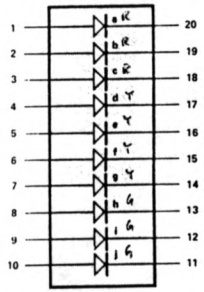


Absolute Maximum Ratings[9]

Parameter	HDSP-4820	HDSP-4830	HDSP-4840	HDSP-4850	HDSP-4890
Average Power Dissipation per LED (T = 25° C)[1]	125 mW	125 mW	125 mW	125 mW	125 mW
Peak Forward Current per LED	150 mA[2]	90 mA[3]	60 mA[3]	90 mA[3]	90 mA[3]
DC Forward Current per LED	30 mA[4]	30 mA[5]	30 mA[6]	30 mA[7]	30 mA[7]
Operating Temperature Range	−40° C to +85° C			−20° C to +85° C	
Storage Temperature Range	−40° C to +85° C				
Reverse Voltage per LED	3.0 V				
Lead Soldering Temperature (1.59 mm (1/16 inch) below seating plane[8]	260° C for 3 sec				

NOTES:
1. Derate maximum average power above T_A = 25° C at 1.67 mW/° C. This derating assumes worst case $R_{\theta J-A}$ = 600° C/W/LED.
2. See Figure 1 to establish pulsed operating conditions.
3. See Figure 6 to establish pulsed operating conditions.
4. Derate maximum DC current above T_A = 63° C at 0.81 mA/° C per LED. This derating assumes worst case $R_{\theta J-A}$ = 600° C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 2.
5. Derate maximum DC current above T_A = 50° C at 0.6 mA/° C per LED. This derating assumes worst case $R_{\theta J-A}$ = 600° C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 7.
6. Derate maximum DC current above T_A = 70° C at 0.67 mA/° C per LED. This derating assumes worst case $R_{\theta J-A}$ = 600° C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 8.
7. Derate maximum DC current above T_A = 37° C at 0.48 mA/° C per LED. This derating assumes worst case $R_{\theta J-A}$ = 600° C/W/LED. With an improved thermal design, operation at higher temperatures without derating is possible. See Figure 9.
8. Clean only in water, Isopropanol, Ethanol, Freon TF or TE (or equivalent) and Genesolve DI-15 (or equivalent).
9. Absolute maximum ratings for the HER, Yellow, and Green elements of the multicolor arrays are identical to the HDSP-4830/-4840/-4850 maximum ratings.

Internal Circuit Diagram



PIN	FUNCTION	PIN	FUNCTION
1	ANODE-a	11	CATHODE-j
2	ANODE-b	12	CATHODE-i
3	ANODE-c	13	CATHODE-h
4	ANODE-d	14	CATHODE-g
5	ANODE-e	15	CATHODE-f
6	ANODE-f	16	CATHODE-e
7	ANODE-g	17	CATHODE-d
8	ANODE-h	18	CATHODE-c
9	ANODE-i	19	CATHODE-b
10	ANODE-j	20	CATHODE-a

Multicolor Array Segment Colors

Segment	HDSP-4832 Segment Color	HDSP-4836 Segment Color
a	HER	HER
b	HER	HER
c	HER	Yellow
d	Yellow	Yellow
e	Yellow	Green
f	Yellow	Green
g	Yellow	Yellow
h	Green	Yellow
i	Green	HER
j	Green	HER

Electrical/Optical Characteristics at T_A = 25° C[4]

RED HDSP-4820

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[11]	I_F	I_F = 20 mA	610	1250		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[12]	λ_d			645		nm
Forward Voltage per LED	V_F	I_F = 20 mA		1.6	2.0	V
Reverse Voltage per LED	V_R	I_R = 100 μA	3	12[5]		V
Temperature Coefficient V_F per LED	ΔV_F/° C			-2.0		mV/° C
Thermal Resistance LED Junction-to-Pin	$R_{\theta J-PIN}$			300		° C/W/ LED

HIGH-EFFICIENCY RED HDSP-4830

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	I_F = 10 mA	900	3500		µcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[2]	λ_d			626		nm
Forward Voltage per LED	V_F	I_F = 20 mA		2.1	2.5	V
Reverse Voltage per LED	V_R	I_R = 100 µA	3	30[5]		V
Temperature Coefficient V_F per LED	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R_{\theta J-PIN}$			300		°C/W/ LED

YELLOW HDSP-4840

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	I_F = 10 mA	600	1900		µcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[2,3]	λ_d		581	585	592	nm
Forward Voltage per LED	V_F	I_F = 20 mA		2.2	2.5	V
Reverse Voltage per LED	V_R	I_R = 100 µA	3	40[5]		V
Temperature Coefficient V_F per LED	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R_{\theta J-PIN}$			300		°C/W/ LED

GREEN HDSP-4850

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity per LED (Unit Average)[1]	I_V	I_F = 10 mA	600	1900		µcd
Peak Wavelength	λ_{PEAK}			566		nm
Dominant Wavelength[2,3]	λ_d			571	577	nm
Forward Voltage per LED	V_F	I_F = 10 mA		2.1	2.5	V
Reverse Voltage per LED	V_R	I_R = 100 µA	3	50[5]		V
Temperature Coefficient V_F per LED	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R_{\theta J-PIN}$			300		°C/W/ LED

EMERALD GREEN HDSP-4890

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity Per LED (Unit Average)[1]	I_V	I_F = 10 mA	250	1600		µcd
Peak Wavelength	λ_{PEAK}			556		nm
Dominant Wavelength[2,3]	λ_d			558		nm
Forward Voltage Per LED	V_F	I_F = 10 mA		2.2	2.5	V
Reverse Voltage Per LED	V_R	I_R = 100 µA	3	50[5]		
Temperature Coefficient V_F Per LED	ΔV_F/°C			-2.0		mV/°C
Thermal Resistance LED Junction-to-Pin	$R\theta_{J-PIN}$			300		°C/W/LED

NOTES:
1. The bar graph arrays are categorized for luminous intensity. The category is designated by a letter located on the side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
3. The HDSP-4832/-4836/-4840/-4850/-4890 bar graph arrays are categorized by dominant wavelength with the category designated by a number adjacent to the intensity category letter. Only the yellow elements of the HDSP-4832/-4836 are categorized for color.
4. Electrical/optical characteristics of the High-Efficiency Red elements of the HDSP-4832/-4836 are identical to the HDSP-4830 characteristics. Characteristics of Yellow elements of the HDSP-4832/-4836 are identical to the HDSP-4840. Characteristics of Green elements of the HDSP-4832/-4836 are identical to the HDSP-4850.
5. Reverse voltage per LED should be limited to 3.0 V Max.

HDSP-4820

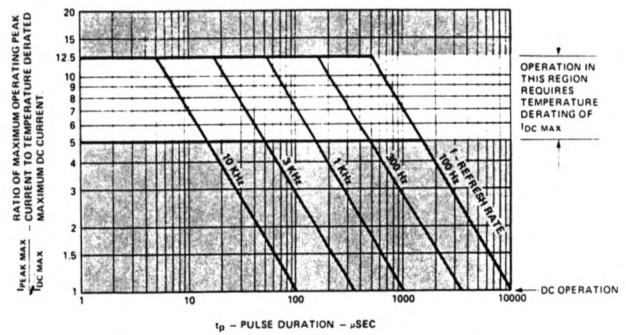


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

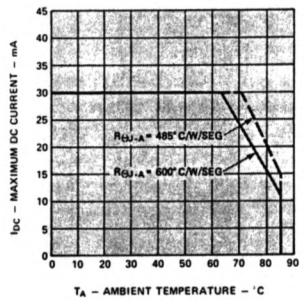


Figure 2. Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings based on Maximum Allowable Thermal Resistance, LED Junction-to-Ambient on a per LED basis. T_{JMAX} = 100° C

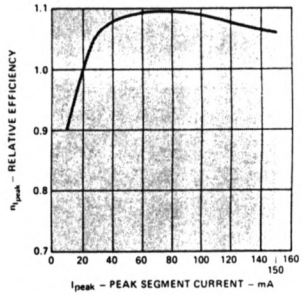


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

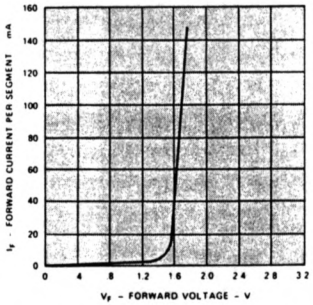


Figure 4. Forward Current vs. Forward Voltage

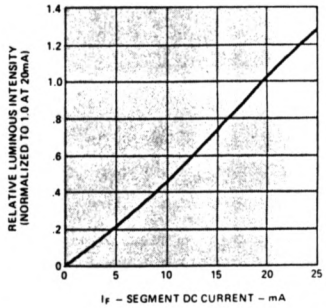


Figure 5. Relative Luminous Intensity vs. D.C. Forward Current

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

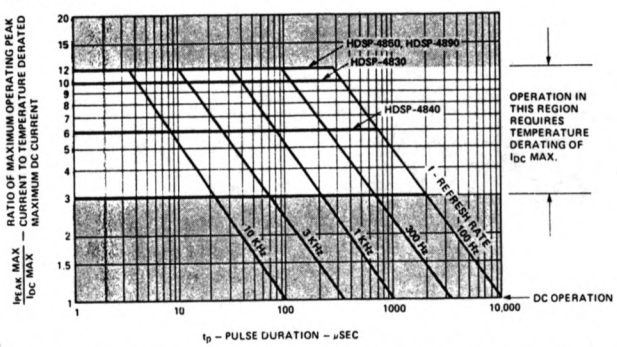


Figure 6. HDSP-4830/-4840/-4850/-4890 Maximum Tolerable Peak Current vs. Pulse Duration

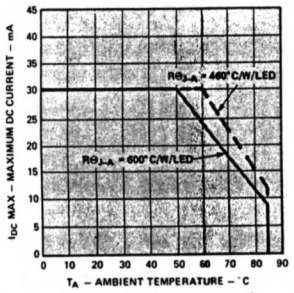


Figure 7. HDSP-4830 Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED basis. $T_{J\ MAX}$ = 100° C.

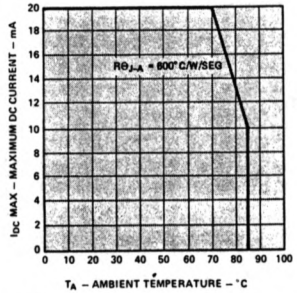


Figure 8. HDSP-4840 Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED basis. $T_{J\ MAX}$ = 100° C.

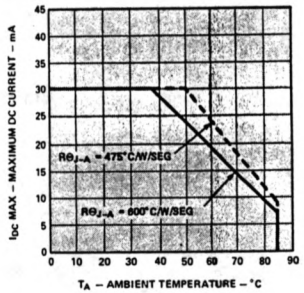


Figure 9. HDSP-4850/-4890 Maximum Allowable D.C. Current per LED vs. Ambient Temperature. Deratings Based on Maximum Allowable Thermal Resistance Values, LED Junction-to-Ambient on a per LED basis. $T_{J\ MAX}$ = 100° C.

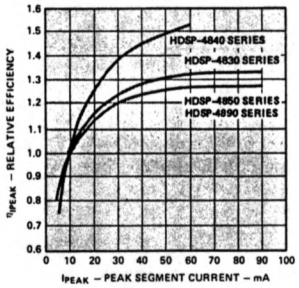


Figure 10. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current

For a Detailed Explanation on the Use of Data Sheet Information and Recommended Soldering Procedures, See Application Note 1005.

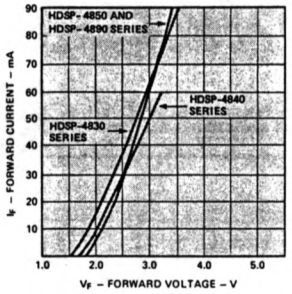


Figure 11. Forward Current vs. Forward Voltage

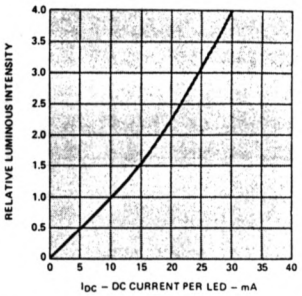


Figure 12. HDSP-4830/-4840/-4850/-4890 Relative Luminous Intensity vs. D.C. Forward Current

Electrical

These versatile bar graph arrays are composed of ten light emitting diodes. The light from each LED is optically stretched to form individual elements. The diodes in the HDSP-4820 bar graph utilize a Gallium Arsenide Phosphide (GaAsP) epitaxial layer on a Gallium Arsenide (GaAs) Substrate. The HDSP-4830/-4840 bar graphs utilize a GaAsP epitaxial layer on a GaP substrate to produce the brighter high-efficiency red and yellow displays. The HDSP-4850/-4890 bar graph arrays utilize a GaP epitaxial layer on a GaP substrate. The HDSP-4832/-4836 multicolor arrays have high efficiency red, yellow, and green LEDs in one package.

These display devices are designed to allow strobed operation. The typical forward voltage values, scaled from Figure 4 or 11, should be used for calculating the current limiting resistor value and typical power dissipation. Expected maximum V_F values, for the purpose of driver circuit design and maximum power dissipation, may be calculated using the following $V_{F\ MAX}$ models.

HDSP-4820 (Red)

$V_{F\ MAX} = 1.75\ V + I_{PEAK}\ (12.5\Omega)$

For: $I_{PEAK} \geq 5$ mA

HDSP-4830/-4840 (High Efficiency Red/Yellow)

$V_{F\ MAX} = 1.75V + I_{PEAK}\ (38\Omega)$

For $I_{PEAK} \geq 20$ mA

$V_{F\ MAX} = 1.6V + I_{DC}\ (45\Omega)$

For: 5 mA ≤ I_{DC} ≤ 20 mA

HDSP-4850/-4890 (Green/Emerald)

$V_{F\ MAX} = 2.0V + I_{PEAK}\ (50\Omega)$

For: $I_{PEAK} > 5$ mA

Refresh rates of 1 KHz or faster provide the most efficient operation resulting in the maximum possible time averaged luminous intensity.

The time averaged luminous intensity may be calculated using the relative efficiency characteristic shown in Figures 3 and 10. The time averaged luminous intensity at T_A = 25°C is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{F\ AVG}}{I_{F\ SPEC\ AVG}}\right] \eta_{IPEAK}\ (I_{V\ SPEC})$$

Example: For HDSP-4830 operating at I_{PEAK} = 50 mA, 1 of 4 Duty Factor

$\eta_{IPEAK} = 1.35$ (at I_{PEAK} = 50 mA)

$$I_{V\ TIME\ AVG} = \left[\frac{12.5\ mA}{10\ mA}\right] (1.35)\ 2280\ \mu cd = 3847\ \mu cd$$

For Further Information Concerning Bar Graph Arrays and Suggested Drive Circuits, Consult HP Application Note 1007 Entitled "Bar Graph Array Applications".

SERIES 23000 "SNAP-IN" SLIMSWITCH

The unit that costs less to buy, less to install and less to maintain.

10 STANDARD DIAL POSITIONS

Series 23000 SLIMSWITCHES are especially made for applications where cost is the primary consideration in selecting a control component. They are also ideal for use where maximum panel density, good reliability, error-proof positive setting action and large (.170 high) easily read in-line characters are desired.

Series 23000 SLIMSWITCHES are not recommended for use in applications where high temperature, high humidity or contaminated environments exist.

Series 23000 SLIMSWITCHES are truly the state-of-the-art economy leaders of the "thumbwheel" switch industry.

Their high package density saves on precious panel space...Snap-in mounting saves on installation and replacement costs...Exclusive, self-locking stainless steel snap-on assembly strap minimizes assembly and module replacement time...

And the purchase price is our lowest ever... Check our price list and you will see what we mean!

Stack as many modules of the same or different output code configurations together as you wish. Put an end bracket on each end of the assembly and snap-on the assembly strap. Snap the entire assembly into a precut hole in your control panel. All without the use of a single tool. That's simplicity and economy!

Or...

If you do not want to set up your own modularized system of assembling switches to meet all of your digital switch requirements yourself, just tell us what your requirements are and we will assemble them for you.

Series 23000 SLIMSWITCHES are available from local stock at your nearest Digitran distributor or from the factory.

Specifications

Mechanical & Electrical:

Number of standard dial positions: 10

Operating Force: 4 to 8 ounces

Life: Over 1,000,000 detent operations at 25°C. (77°F.)

Weight: 1/4 ounce per module (approximately)

Dial character height: .170 (4.32) for standard dials

Standard finish and color: Case, wheel and end brackets, black unless otherwise specified. Dial markings, white on black

Rated electrical loads: 28VAC or 28VDC at 50 milliamps resistive at 25°C. (77°F.). Non-switching current: 2 amps

Contact resistance: Less than 100 milliohms original value between common and output terminal(s)

Insulation resistance: 1000 megohms minimum per MIL-STD-202, Method 302, Test Condition A, between any two non-connected terminals

Dielectric withstanding: 500 VRMS

Terminations: Solder connections standard. Connector compatability on some types

Environmental:

Operating temperature: −20°C. to 65°C.

Shock: 100 G's, 6 miliseconds duration, sawtooth

Vibration: 5G's at 70—2000 cps. 10—70 cps: .06 inches double amplitude (Ref: MIL-STD-202, Method 204, Test Condition B.)

Materials:

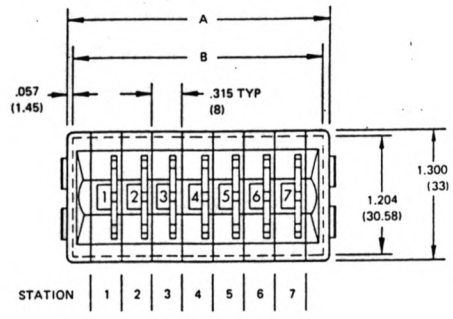
Printed circuit board: Laminate per MIL-P-13949, type GF or GE, plated with nickel

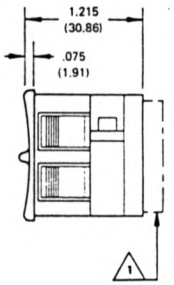
Contacts: Precious metal alloy

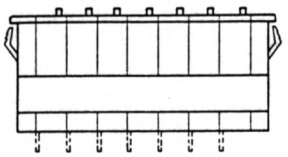
Structural parts: ABS thermoplastic

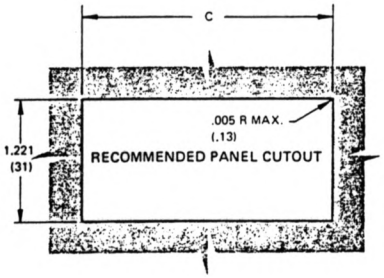
Important Notice:

Do not allow flux or cleaning agent to enter switch. Use only 40% isopropyl alcohol in distilled water for cleaning agents. For additional information about recommended cleaning method, contact Digitran.









NUMBER OF MODULES	A	B	C
1	.745 (19)	.649 (16.5)	.669 (17)
2	1.060 (27)	.964 (24.5)	.984 (25)
3	1.375 (35)	1.279 (32.5)	1.299 (33)
4	1.690 (43)	1.594 (40.5)	1.614 (41)
5	2.005 (51)	1.909 (48.5)	1.929 (49)
6	2.320 (59)	2.224 (56.5)	2.244 (57)
7	2.635 (67)	2.539 (64.5)	2.559 (65)
8	2.950 (75)	2.854 (72.5)	2.874 (73)
9	3.265 (83)	3.169 (80.5)	3.189 (81)
10	3.580 (91)	3.484 (88.5)	3.504 (89)
N	N × .315 + .430 N × (8) + (11)	N × .315 + .334 N × (8) + (8.5)	N × .315 + .354 N × (8) + (9)

Notes:

1. For details of printed circuit board, terminals and electrical output, see drawing of specific module.
2. Dimensions in parenthesis are in millimeters.
3. Assembly will accept panel thickness of .062 (1.58), .079 (2), .118 (3), .125 (3.2), .158 (4).

TRUTH TABLE 14 (continued from page 8).

Series	Symbol	Part Number	Terminations	List Price
700		710	S	12.00
		710/107	S	14.00
		721	S	13.00
	*	721/107	S	16.00
8000		8010	S	6.50
	*	8021	S	7.50
9000		9010	S or DC1	13.00
	*	9021	S or DC1	14.00
12000		12010	S	16.00
13000		13010	S or DC1	9.00
		1302	S or DC1	8.00
19000		19010	S or DC1	10.00
		19021	S or DC1	11.00
23000		23010	S	3.75
		2302	S	.25
28000		28010	S or DC35	7.00
		2851D	S or DC	7.00
29000		29010	S	4.50
		2902	S	5.00

* With provision for components (Diodes, Resistors, etc.)

Truth Table 15

	COMMON C CONNECTED TO:							
DIAL	1	2	4	8	1	2	4	8
0		●		●	●		●	
1	●					●	●	●
2		●			●		●	●
3	●	●					●	●
4			●		●	●		●
5	●		●			●		●
6		●	●		●			●
7	●	●	●					●
8				●	●	●	●	
9	●			●			●	

BINARY CODED DECIMAL, PLUS COMPLEMENT, WITH BINARY 10 AT ZERO, ONE COMMON

Standard Dial: 0-9

10 Positions

Series	Symbol	Part Number	Terminations	List Price
300		3069	S	14.00
9000	*	9069	S or DC1	18.00
13000		1306	S or DC1	11.00
19000	*	19069	S or DC1	15.00

* With provision for components (Diodes, Resistors, etc.)

Truth Table 16

	COMMON C CONNECTED TO:			
DIAL	1	2	4	8
0	●	●	●	●
1		●	●	●
2	●		●	●
3			●	●
4	●	●		●
5		●		●
6	●			●
7				●
8	●	●	●	
9		●	●	

COMPLEMENT OF BINARY CODED DECIMAL, ONE COMMON

Standard Dial: 0-9

10 Positions

Series	Symbol	Part Number	Terminations	List Price
300		3129	S	7.00
	*	368	S	9.00
700		7635	S or DC27	10.00
		7635/107	S or DC27	12.00
		761	S	12.00
	*	7616/107	S	14.00
8000		79	S or DC8	5.50
9000		9129	S	11.00
		906	S	13.00
12000		12628	S or DC27	16.00
13000		1306	S	9.00
		13129	S	7.00
19000		1912	S	8.00
	*	19068	S	10.00
23000		2310	S	.25
28000		28115	S or DC8	6.00
		2861	S or DC8	7.00
29000		29102	S	4.00
		2911	S or WW	4.50

* With provision for components (Diodes, Resistors, etc.)

1. Terminals available where indicated: S=direct solder only, DCXX=connector only, S or DCXX=direct solder or connector, WW=wire wrap, P=pin, WL=wire leads only. 2. See pages 20 through 22 for "Additional Pricing Information". 3. See page 22 for Quantity Discount Schedule. 4. See pages 1 and 2 for "How To Order", "How To Use The Price List" and "Our Assembly Part Numbering System".

200 MHz Phase Detector

MCL PDC-10-1 Broadband Directional Coupler, Mini-Circuits
MCL PSC-2-1 Power Divider, Mini-Circuits
MCL SRA-1 Mixer, Mini-Circuits
MCL PSCQ-2-250 90 Degree Power Divider, Mini-Circuits

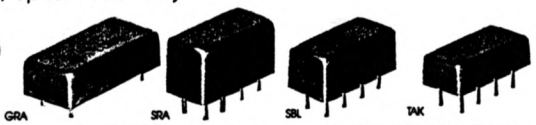
most widely-used

Frequency Mixers

LEVEL 7 (+7 dBm LO, up to +1 dBm RF)

case style selection

outline drawings see pages 4-9



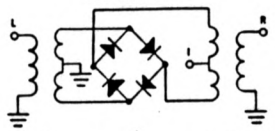
	MODEL NO.	FREQUENCY MHz LO/RF f_L-f_U	IF	CONVERSION LOSS dB Mid-Band m Typ.	Mid-Band m Max.	Total Range Typ.	Total Range Max.	LO-RF ISOLATION, dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	LO-IF ISOLATION, dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	PRICE, $ Ea.	Qty.
GRA case D09	GRA-1	5-500	DC-500	5.5	7.0	6.5	8.5	50	45	45	30	35	25	45	35	40	25	30	20	12.95	(6-49)
	GRA-3	025-200	DC-200	5.5	7.5	6.5	8.5	60	50	45	35	35	25	45	35	40	30	30	20	15.95	(6-49)
	GRA-6	003-100	DC-100	5.5	7.5	6.5	8.5	60	50	45	30	35	25	60	45	40	25	30	20	22.95	(5-24)
	GRA-8	0005-10	DC-10	6.5	7.5	7.0	8.5	60	50	50	40	45	35	60	50	50	40	45	35	25.95	(5-24)
SRA case A01	•SRA-1	5-500	DC-500	5.5	7.0	6.5	8.5	50	45	45	30	35	25	45	35	40	25	30	20	11.95	(1-49)
	SRA-1TX	5-500	DC-500	5.5	7.0	6.5	8.5	50	45	45	30	35	25	45	35	40	25	30	20	49.95	(1-49)
	SRA-1W	1-750	DC-750	5.5	7.5	6.5	8.5	50	45	45	30	35	25	45	30	40	25	30	20	14.95	(5-24)
	SRA-1-1	1-500	DC-500	5.5	7.5	6.5	8.5	50	45	45	30	35	25	45	30	40	25	30	20	13.95	(5-24)
	SRA-2	1-1000	5-500	5.5	7.5	6.5	8.5	45	30	35	20	30	20	45	30	30	20	30	20	14.95	(5-24)
	SRA-2CM	5-1000	DC-1000	6.0	7.0	6.5	8.5	60	50	35	30	30	25	50	45	30	25	25	20	14.95	(1-49)
	SRA-3	025-200	DC-200	5.5	7.5	6.5	8.5	60	50	45	35	35	25	45	35	40	30	30	20	14.95	(5-24)
	SRA-4	5-1250	5-500	5.5	7.5	6.5	8.5	50	40	40	20	30	20	50	40	40	20	30	20	16.95	(5-24)
	•SRA-5	5-1500	10-600	7.0	8.0	7.5	8.5	50	45	35	30	30	20	45	40	30	25	25	15	21.95	(5-24)
	SRA-6	003-100	DC-100	5.5	7.5	6.5	8.5	60	50	45	30	35	25	60	45	40	25	30	20	21.95	(5-24)
	SRA-8	0005-10	DC-10	6.5	7.5	7.0	8.5	60	50	50	40	45	35	60	50	50	40	45	35	26.95	(5-24)
case A06	SRA-11	5-2000	10-600	7.0	8.5	7.5	9.0	50	45	35	25	30	20	45	40	30	20	25	15	26.95	(5-24)
	SRA-12	800-1250	50-90	—	—	6.0	7.5	32	25	35	25	35	25	30	20	30	20	30	20	24.95	(5-24)
	SRA-2000	100-2000	DC-600	6.0	9.5	7.0	9.5	—	—	37	20	—	—	—	—	—	—	30	20	31.95	(1-24)
	SRA-2400 WW	750-2400	DC-400	—	—	6.7	9.0	30	20	30	20	30	20	30	8	30	8	30	8	19.95	(1-24)
	SRA-3500 WW	500-3500	DC-1000	—	—	7.5	9.5	30	17	30	17	30	17	20	8	20	8	20	8	34.95	(1-24)
□ SBL case A06	SBL-1	1-500	DC-500	5.5	7.0	6.5	8.0	60	45	45	35	40	25	45	35	40	25	30	20	4.50	(10-49)
	SBL-1X	10-1000	5-500	6.0	7.5	7.0	8.0	50	40	40	30	30	20	50	45	40	35	35	25	5.95	(10-49)
	SBL-1Z	10-1000	DC-500	6.5	7.5	7.0	9.0	50	40	35	25	25	20	40	25	25	18	19	15	6.95	(10-49)
	SBL-1-1	0.1-400	DC-400	5.5	7.0	6.0	8.0	58	45	45	30	35	25	45	30	40	25	30	20	6.50	(10-49)
	SBL-3	025-200	DC-200	5.5	7.5	6.0	8.5	55	50	45	30	35	25	45	35	40	30	30	20	7.50	(10-49)
	SBL-11 WW	5-2000	10-600	7.0	8.5	7.5	9.0	50	45	35	25	30	20	45	40	30	20	25	15	16.95	(5-49)
TAK case A04	TAK-5	01-250	DC-250	5.5	7.0	6.5	8.5	60	50	50	35	40	35	55	45	45	30	35	25	18.95	(1-4)
	TAK-5R	05-200	DC-200	5.5	6.5	6.5	8.0	55	50	45	35	45	35	50	45	40	30	40	30	15.95	(5-24)
	TAK-6	5-600	DC-600	5.5	7.5	6.5	8.5	60	50	50	30	40	25	55	45	45	30	30	20	18.95	(1-4)
	TAK-6R	5-600	DC-600	6.0	7.0	6.5	8.0	55	50	45	40	35	30	45	40	40	25	30	25	15.95	(5-24)
	TAK-7	2-1000	5-500	5.5	7.5	6.5	8.5	45	30	35	20	30	20	45	30	35	20	30	20	20.95	(1-4)

L = low range (f_L to 10 f_L) M = mid range (10f_L to f_U/2) U = upper range (f_U/2 to f_U)

m = mid band (2f_L to f_U/2)

• SRA-5 case style is A06.
e HTRB tested. 3 year guarantee
□ NON-HERMETIC
1 For quality control procedures, environmental specifications, and Hi-Rel, MIL and TX description see Table of Contents.
2 Absolute Maximum Ratings:
RF power 50 mW, peak IF current 40 mA, see Table of Contents.
3 PAM-42 protected under patent 4,430,758.
4 Prices and specifications subject to change without notice.

schematic



pin connections

see case style outline drawing

Series	GRA	SRA					SBL				TAK			
models	all models	-1 -1TX -1-1 -3	-2 -4	-6 -8	-1W -2CM	-5 -11 -12 -2000 -2400† -3500†	-1 -1-1 -3	-1X	-1Z	-11	-5 -6	-7	-5R	-6R
LO	1	8	8	8	8	8	8	8	1	8	8	8	8	1
RF	6	1	3,4	1	1	1	1	3,4	8	1	1	3,4	1	8
IF	4	3,4*	1	3,4*	3,4*	3	3,4*	1	3	3	3,4*	1	3,4*	5,6*
GND	2,3,5	2,5,6,7	2,5,6,7	2,5,6,7	2,5,6,7	2,5,6,7	2,5,6,7	2,5,6,7	2,5,6,7		2,5,6,7	2,5,6,7	2,5,6,7	3,4,7
CASE GND	—	2	2,5,6,7	—	2,5,6,7	2,5,6,7	—	2,5,6,7	2,5,6,7		2	2,5,6,7	—	3,4,7

*pins must be connected together externally † (LO = 4, RF = 8)

Mini-Circuits P.O. BOX 350166, Brooklyn, New York 11235-0003 (718) 934-4500
FAX (718) 332-4661 TELEX 6852844 or 620156

mixer harmonic intermodulation

(relative to desired IF output)

RF CAL	1	2	3	4	5	6	7	8	9	10
0	>94	-	36	51	42	61	42	60	58	62	54	72
1	>94	23	-	39	12	46	22	51	35	56	48	72
2	74	68	54	71	55	73	55	74	55	64	50	77
3	81	47	41	49	40	53	42	55	42	56	44	64
4	>94	73	75	76	71	77	67	76	66	76	62	75
5	>94	70	66	67	52	71	49	66	49	71	52	65
6	>94	84	77	>86	>86	>86	81	>86	82	84	82	83
7	>94	83	65	79	65	78	75	76	60	77	55	73
8	>94	86	85	>88	81	>86	>86	>86	>86	>86	84	>86
9	93	87	84	86	80	82	73	85	75	86	84	78
10	>93	>87	>87	86	>87	>88	>88	>86	>86	>86	>86	>86

RF ORDER HARMONIC

Harmonic LO Order

test conditions RF = 185.100 MHZ INPUT P = +0.00DBM
LO = 155.010 MHZ INPUT P = +6.92DBM
IF = 30.090 MHZ IF AMPLIT. = -6.18 DBM

RF CAL	1	2	3	4	5	6	7	8	9	10
0	>84	-	28	42	28	52	27	43	30	48	35	48
1	>84	22	-	36	13	40	21	47	30	44	36	49
2	82	75	60	76	60	73	59	73	58	69	49	69
3	>84	65	62	67	66	69	56	73	55	69	53	68
4	>84	>76	>76	>76	>76	>76	>76	>76	>76	>76	>76	>76
5	>84	>76	>76	>76	>76	>76	>76	>76	>76	>76	>76	>76
6	>84	>78	>76	>76	>76	>76	>76	>76	>76	>76	>76	>76
7	84	>78	>78	>76	>76	>76	>76	>76	>76	>76	>76	>76
8	>84	>78	>78	78	>78	>76	>76	>76	>76	>76	>76	>76
9	82	77	>78	>78	>78	>78	>76	>76	>76	>76	>76	>76
10	>82	>76	78	78	>78	78	>78	>76	>76	>76	>76	>76

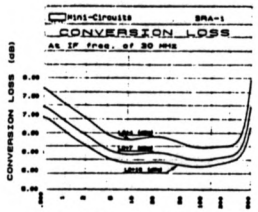
RF ORDER HARMONIC

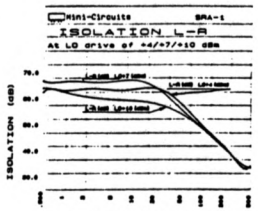
Harmonic LO Order

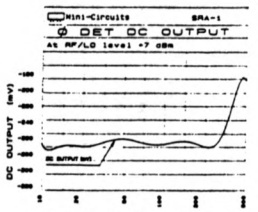
test conditions RF = 185.100 MHZ INPUT P = -9.90DBM
LO = 155.010 MHZ INPUT P = +6.92DBM
IF = 30.090 MHZ IF AMPLIT. = -15.97 DBM

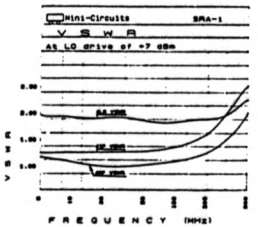
typical performance curves

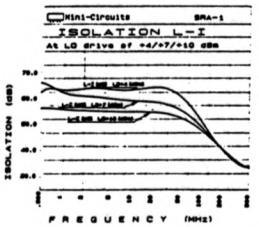
(production unit)

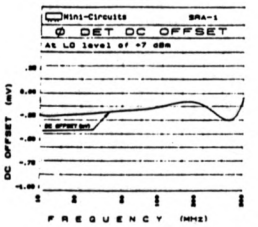












very broadband

Directional Couplers

6 to 30dB

10KHz to 2000 MHz

case style selection

outline drawings see pages 4-9


TDC


PDC


TODC

	MODEL NO.	FREQUENCY MHz f_L-f_U	COUPLING dB Nom.	COUPLING dB Flatness	MAINLINE LOSS* dB L typ.	L max.	M typ.	M max.	U typ.	U max.	DIRECTIVITY dB L typ.	L min.	M typ.	M min.	U typ.	U min.	VSWR typ.	POWER INPUT, W L max.	POWER INPUT, W M,U max.	PRICE, $ ea.	PRICE, $ qty.
TDC case B02	TDC-6-1	10-400	6.3±0.4	±0.4	2.0	2.4	2.0	2.4	2.0	2.5	36	30	30	25	20	15	1.5	1	2	19.95	(5-49)
	TDC-10-1	1-400	10.0±0.5	±0.5	1.2	1.5	1.0	1.3	1.2	1.5	35	25	30	20	20	15	1.5	1	2	15.95	(5-49)
	TDC-10-2 NEW	5-1000	11 ± 0.5	±0.6	1.4	1.8	1.5	1.8	1.6	2.0	50	35	25	20	20	15	1.5	0.5	0.5	21.95	(5-49)
PDC case A01	PDC-10-1	0.5-500	11.5±0.5	±0.6	0.85	1.3	0.65	1.0	0.85	1.3	32	25	32	25	22	15	1.2	1.5	3	11.95	(5-49)
	△PDC-10-2	250-1000	10.5±0.5	±0.6	1.4	1.6	—	—	1.6	2.0	30	25	30	20	25	15	1.5	—	5	27.95	(5-49)
	PDC-10-5 NEW	1-2000	10.5 ± 0.5	±1.0	1.2	1.9	1.3	1.9	2.0	2.5	38	25	30	18	22	18	1.3	0.5	0.5	34.95	(5-49)
	PDC-10-6	0.005-20	11±0.5	±0.5	0.4	1.2	0.4	0.8	0.4	1.0	40	30	40	30	35	25	1.3	1.5	3	19.95	(5-49)
	▲PDC-10-21	1-1000	11±0.5	±0.5	1.2	1.7	1.2	1.7	1.6	2	40	30	25	20	25	20	1.2	1	2	24.95	(5-49)
	PDC-10-22	5-750	11±0.5	±0.5	1.1	1.6	1.2	1.7	1.6	1.9	35	30	25	20	25	20	1.25	1	2	19.95	(5-49)
	PDC-10-54 NEW	10-1500	10.5 ± 0.5	±0.7	1.2	1.8	1.3	1.9	1.6	2.3	35	25	28	23	28	23	1.3	0.5	0.5	29.95	(5-49)
	PDC-15-6	0.01-35	15±0.5	±0.5	0.3	0.6	0.2	0.4	0.3	0.6	38	30	35	25	28	20	1.15	2	4	19.95	(5-49)
	PDC-15-21	1-500	14.7±0.5	±0.6	0.7	1.1	0.7	1.1	0.8	1.2	35	30	35	30	30	23	1.4	1	2	19.95	(5-49)
	†PDC-20-1	25-400	21±0.75	±0.5	0.2	0.25	0.3	0.35	0.35	0.5	25	20	35	25	25	20	1.25	3	5	19.95	(5-49)
	PDC-20-1W	10-700	19.2±0.5	±0.5	0.25	0.5	0.4	0.7	0.7	1.1	34	30	27	23	23	20	1.4	1	2	19.95	(5-49)
	PDC-20-3	0.2-250	19.5±0.5	±0.5	0.35	0.6	0.25	0.5	0.35	0.6	36	30	33	25	25	20	1.2	1.5	4	13.95	(5-49)
	◊◊PDC-20-3B NEW	0.2-250	19.5 ± 0.5	±0.5	0.3	0.6	0.25	0.5	0.35	0.6	47	40	40	25	30	20	1.1	1.5	4	15.95	(5-49)
	▪PDC-10-1-75	1-250	10.5±0.5	±0.75	1.1	1.5	1.1	1.5	1.1	1.5	30	20	30	20	30	20	2	2	4	12.95	(5-49)
	▪PDC-10-4-75	0.2-100	10.0±0.5	±0.2	1.2	1.6	0.9	1.2	0.9	1.3	50	30	40	25	37	25	1.5	1	2	14.95	(5-49)
	▪PDC-15-6-75	0.02-35	14.5±0.5	±0.5	0.3	0.7	0.3	0.7	0.3	0.7	35	20	35	20	35	20	1.3	1.5	4	20.95	(5-49)
	▪PDC-20-3-75	1-150	19.5±0.5	±0.75	0.35	0.8	0.35	0.8	0.35	0.8	25	20	25	20	25	20	2	2	4	12.95	(5-49)
TODC case 0096	TODC-10-1	10-400	11.5±0.5	±0.5	1.2	1.5	1.0	1.3	1.2	1.5	35	25	30	20	25	20	1.5	0.5	1	15.95	(5-49)

L = low range (f_L to 10 f_L) M = mid range (10f_L to f_U/2) U = upper range (f_U/2 to f_U)

NOTES:

△ L = f_L – 2f_L, M=0

* Includes theoretical power loss at coupled port.

▪ Denotes 75 ohm models, available only with 75 ohm BNC

◊ bi directional, L = 30 to 100 MHz

◊◊ bi directional

† Models PDC-20-1, ZDC-20-1, ZMDC-20-1:
L = 25-50 MHz, M = 50-300 MHz, U = 300-400 MHz

▪ Model ZFDC-20-5: above 1000 MHz, coupling flatness ± 1.5dB

▲ Models PDC-10-21, ZFDC-10-21: Upper range coupling ± 0.75dB

1. For quality control procedures, see Table of Contents.
2. For environmental specifications, see Table of Contents.
3. For connector types and case mounting options, see case style outline drawing.
4. Prices and specifications subject to change without notice.
5. All models are licensed under U.S. Patent 3,426,298.
6. For Model PDC-20-3B, bidirectional

MIL-C-15370/18, NSN GUIDE

MCL NO.	NSN	MIL-C-15370/18*
PDC-10-1	5985-01-178-4406	002
PDC-10-2		008
PDC-10-21	5985-01-130-0177	003
PDC-10-22	5985-01-190-7738	
PDC-15-6	5985-01-147-0160	
PDC-20-3	5985-01-076-8477	001
TDC-10-1	5985-01-226-3428	
ZDC-10-1-BNC	5985-01-125-3467	
ZDC-20-1	5985-01-178-4405	
ZDC-20-3-BNC	5985-01-096-5007	
ZFDC-10-1	5985-01-179-5122	
ZFDC-10-2	5985-01-208-5694	
ZFDC-20-3	5985-01-146-0478	
ZFDC-20-5	5985-01-097-2192	
ZMDC-20-3	5985-01-193-8515	

*units are not QPL listed

pin and coaxial connections

see case style outline drawing

Series	In	Out	Cpl_{in}	NOTE 6 Cpl_{out}	Case Ground	Not Used
TODC	5	8	2	—	all others	11
PDC	1	4	3	6	2,5,7,8	6
TDC	1	2	4	—	3	—
ZFDC	1	2	3	—	—	—
ZMDC	3	2	1	—	—	—
ZDC	3	2	1	—	—	—
ZFDC (except 20-4, -5)	1	2	3	—	—	—
ZFDC 20-4, -5	3	1	2	—	—	—

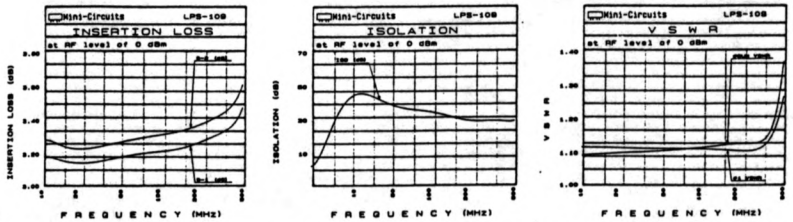
Mini-Circuits P.O. BOX 350166, Brooklyn, New York 11235-0003 (718) 934-4500
FAX (718) 332-4661 TELEX 6852844 or 620156

2WAY-0°

Power Splitter/Combiners 50 ohms

LPS-109

10 to 500MHz

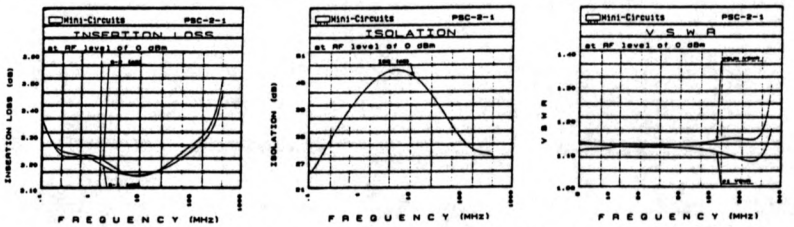


FREQUENCY (MHz)	INSERTION LOSS (dB) S-1	INSERTION LOSS (dB) S-2	AMPLITUDE UNBALANCE (dB) 1-2	ISOLATION (dB)
10.0	3.19	3.29	0.10	49.87
34.5	3.16	3.25	0.09	42.08
59.0	3.19	3.28	0.09	37.67
83.5	3.20	3.29	0.09	35.19
108.0	3.21	3.30	0.09	33.43
132.5	3.22	3.33	0.11	32.10
157.0	3.24	3.34	0.10	31.06
206.0	3.27	3.36	0.09	29.55
255.0	3.28	3.39	0.11	28.67
304.0	3.31	3.42	0.11	28.29
353.0	3.34	3.46	0.12	28.41
402.0	3.36	3.48	0.12	28.79
426.5	3.36	3.48	0.12	28.93
451.0	3.40	3.52	0.12	28.84
500.0	3.49	3.63	0.14	27.07

FREQUENCY (MHz)	VSWR S	VSWR 1	VSWR 2
10.0	1.09	1.12	1.14
34.5	1.10	1.11	1.13
59.0	1.11	1.11	1.13
83.5	1.11	1.11	1.13
108.0	1.11	1.11	1.13
132.5	1.12	1.11	1.13
157.0	1.12	1.11	1.13
206.0	1.12	1.10	1.12
255.0	1.12	1.10	1.12
304.0	1.13	1.11	1.11
353.0	1.14	1.12	1.12
402.0	1.18	1.15	1.13
426.5	1.21	1.17	1.14
451.0	1.25	1.20	1.16
500.0	1.37	1.26	1.20

PSC-2-1

0.1 to 400MHz



FREQUENCY (MHz)	INSERTION LOSS (dB) S-1	INSERTION LOSS (dB) S-2	AMPLITUDE UNBALANCE (dB) 1-2	ISOLATION (dB)
0.1	3.37	3.38	0.01	24.33
0.2	3.26	3.25	0.01	29.63
0.5	3.24	3.23	0.01	37.19
1.0	3.22	3.22	0.00	41.80
10.0	3.16	3.16	0.00	47.10
20.0	3.18	3.18	0.00	43.53
50.0	3.20	3.20	0.00	37.27
100.0	3.24	3.24	0.00	32.42
148.2	3.27	3.29	0.02	30.09
200.0	3.31	3.33	0.02	28.94
251.9	3.32	3.35	0.03	28.80
296.3	3.34	3.39	0.05	29.45
340.8	3.40	3.45	0.05	29.74
370.4	3.42	3.48	0.06	28.61
400.0	3.48	3.53	0.05	26.04

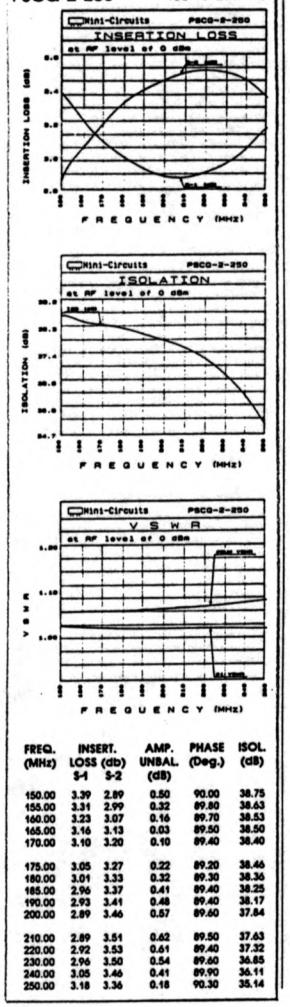
FREQUENCY (MHz)	VSWR S	VSWR 1	VSWR 2
5.0	1.12	1.14	1.14
10.0	1.12	1.13	1.13
17.3	1.13	1.12	1.12
20.0	1.13	1.12	1.12
50.0	1.13	1.12	1.12
66.7	1.13	1.12	1.12
100.0	1.14	1.11	1.11
140.8	1.14	1.10	1.1
190.2	1.15	1.09	1.09
227.2	1.14	1.08	1.08
276.6	1.15	1.08	1.08
313.6	1.16	1.09	1.09
350.6	1.20	1.12	1.11
375.3	1.24	1.14	1.13
400.0	1.30	1.17	1.16

Mini-Circuits P.O. BOX 350166, Brooklyn, New York 11235-0003 (718) 934-4500
FAX (718) 332-4661 TELEX 6852844 or 620156

Mini-Circuits

PSCQ-2-250

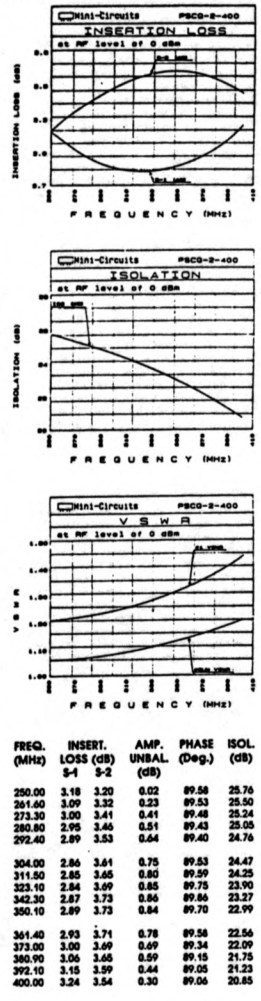
150 to 250MHz



FREQ. (MHz)	INSERT. LOSS (db) S-1	INSERT. LOSS (db) S-2	AMP. UNBAL. (dB)	PHASE (Deg.)	ISOL. (dB)
150.00	3.39	2.89	0.50	90.00	38.75
155.00	3.31	2.99	0.32	89.80	38.63
160.00	3.23	3.07	0.16	89.70	38.53
165.00	3.16	3.13	0.03	89.50	38.50
170.00	3.10	3.20	0.10	89.40	38.40
175.00	3.05	3.27	0.22	89.20	38.46
180.00	3.01	3.33	0.32	89.30	38.36
185.00	2.96	3.37	0.41	89.40	38.25
190.00	2.93	3.41	0.48	89.40	38.17
200.00	2.89	3.46	0.57	89.60	37.84
210.00	2.89	3.51	0.62	89.50	37.63
220.00	2.92	3.53	0.61	89.40	37.32
230.00	2.96	3.50	0.54	89.60	36.85
240.00	3.05	3.46	0.41	89.90	36.11
250.00	3.18	3.36	0.18	90.30	35.14

PSCQ-2-400

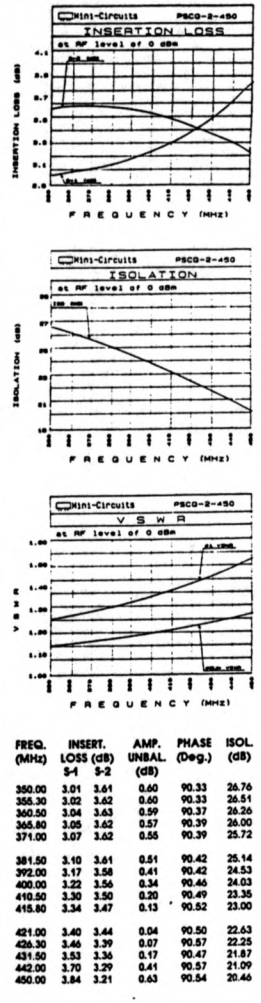
250 to 400MHz



FREQ. (MHz)	INSERT. LOSS (dB) S-1	INSERT. LOSS (dB) S-2	AMP. UNBAL. (dB)	PHASE (Deg.)	ISOL. (dB)
250.00	3.18	3.20	0.02	89.58	25.76
261.60	3.09	3.32	0.23	89.53	25.50
273.30	3.00	3.41	0.41	89.48	25.24
280.80	2.95	3.46	0.51	89.43	25.05
292.40	2.89	3.53	0.64	89.40	24.76
304.00	2.86	3.61	0.75	89.53	24.47
311.50	2.85	3.65	0.80	89.59	24.25
323.10	2.84	3.69	0.85	89.75	23.90
342.30	2.87	3.73	0.86	89.86	23.27
350.10	2.89	3.73	0.84	89.70	22.99
361.40	2.93	3.71	0.78	89.58	22.56
373.00	3.00	3.69	0.69	89.34	22.09
380.90	3.06	3.65	0.59	89.15	21.75
392.10	3.15	3.59	0.44	89.05	21.23
400.00	3.24	3.54	0.30	89.06	20.85

PSCQ-2-450

350 to 450MHz



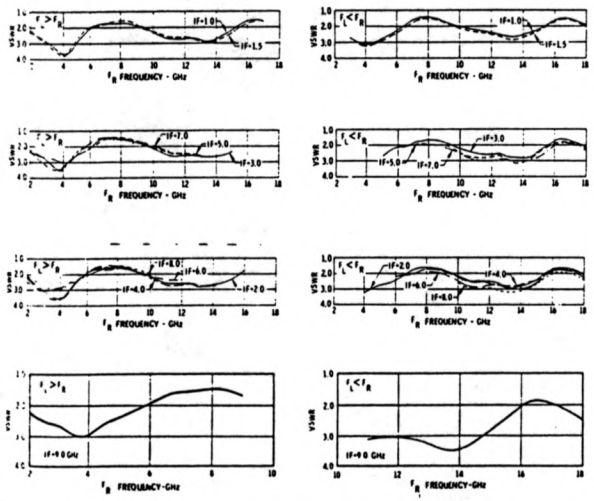
FREQ. (MHz)	INSERT. LOSS (dB) S-1	INSERT. LOSS (dB) S-2	AMP. UNBAL. (dB)	PHASE (Deg.)	ISOL. (dB)
350.00	3.01	3.61	0.60	90.33	26.76
355.30	3.02	3.62	0.60	90.33	26.51
360.50	3.04	3.63	0.59	90.37	26.26
365.80	3.05	3.62	0.57	90.39	26.00
371.00	3.07	3.62	0.55	90.39	25.72
381.50	3.10	3.61	0.51	90.42	25.14
392.00	3.17	3.58	0.41	90.42	24.53
400.00	3.22	3.56	0.34	90.46	24.03
410.50	3.30	3.50	0.20	90.49	23.35
415.80	3.34	3.47	0.13	90.52	23.00
421.00	3.40	3.44	0.04	90.50	22.63
426.30	3.46	3.39	0.07	90.57	22.25
431.50	3.53	3.36	0.17	90.47	21.87
442.00	3.70	3.29	0.41	90.57	21.09
450.00	3.84	3.21	0.63	90.54	20.46

In Stock...Immediate Delivery

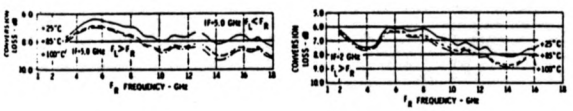
Typical Performance at 25°C (Cont.)

Characteristics	Output Power		Test Conditions
Harmonics of f_L	R-Port	I-Port	
f_L	-10 dBm	-12 dBm	f_L = 2 GHz at +13 dBm
2 f_L	-18 dBm	-15 dBm	
3 f_L	-24 dBm	-21 dBm	
4 f_L	-30 dBm	-31 dBm	
5 f_L	-36 dBm	—	
f_L	-18 dBm		f_L = 4.5 GHz at +13 dBm
2 f_L	-22 dBm		
3 f_L	-34 dBm		
4 f_L	-37 dBm		
f_L	-9 dBm		f_L = 9 GHz at +13 dBm
2 f_L	-29 dBm		
f_L		-21 dBm	f_L = 4 GHz at +13 dBm
2 f_L		-21 dBm	

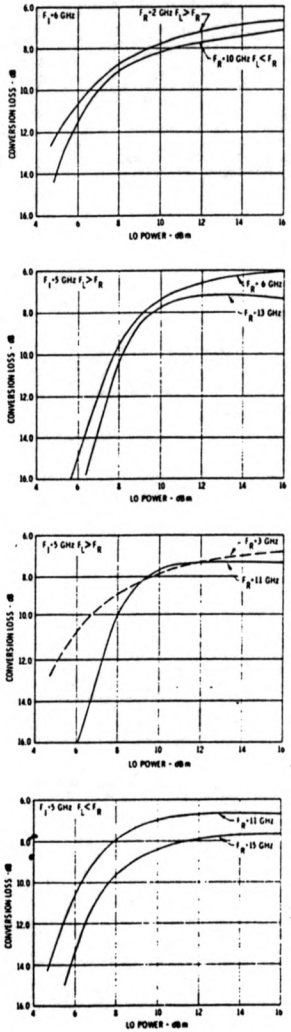
R-PORT VSWR LO @ +13 dBm



CONVERSION LOSS vs FREQUENCY & TEMPERATURE LO @ +13 dBm

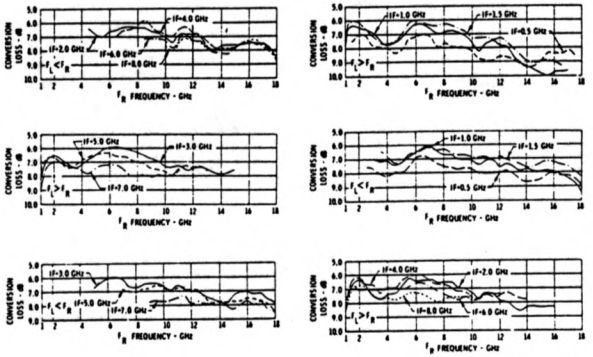


Drive Level: The maximum recommended drive level is +20 dBm.

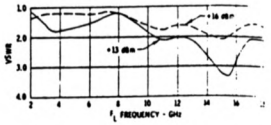


Typical Performance at 25°C (Cont.)

CONVERSION LOSS vs FREQUENCY LO @ + 13 dBm



L-PORT VSWR



JHNSON CO.
, CA, USA

FINAL TEST RESULTS
FOR WJ FM8B MIXER
SERIAL NO. 32018

PASS

CONVERSION LOSS(dB) (LO AT +13dBm)

RF+/-IF=LO(NOT SHOWN) IF(MHz)= RF(MHz)	1000	2000	4000	6000	8000
2000-	----	----	----	----	----
+	6.2	----	6.5	7.4	7.0
3000-	6.8	----	----	----	----
+	6.6	6.7	7.2	7.8	8.8
4000-	6.9	----	----	----	----
+	7.4	7.4	----	8.3	9.2
5000-	7.6	6.5	----	----	----
+	7.7	6.7	7.4	8.3	8.3
6000-	6.2	6.5	2.2	----	----
+	6.2	5.7	6.3	----	8.8
7000-	5.7	5.5	6.1	----	----
+	6.2	5.5	5.9	8.6	7.9
8000-	6.0	5.5	----	5.1	----
+	6.5	5.8	6.7	8.3	----
9000-	6.3	5.6	6.0	4.7	----
+	6.7	6.9	6.5	8.2	8.0
10000-	6.9	5.9	6.3	7.3	7.6
+	7.7	7.2	6.8	8.3	7.9
11000-	----	6.7	6.3	7.1	6.9
+	----	7.2	6.9	8.4	----
12000-	----	6.3	7.1	----	4.3
+	----	7.1	6.9	8.1	----
13000-	----	6.0	6.4	7.7	6.4
+	----	7.0	6.6	----	----
14000-	----	6.1	6.5	7.1	6.6
+	----	7.4	6.6	----	----
15000-	----	6.3	6.7	7.3	7.0
+	----	7.9	----	----	----
16000-	----	6.6	6.7	7.5	----
+	----	8.0	----	----	----
17000-	----	7.8	7.8	8.8	8.6
+	----	----	----	----	----
18000-	----	9.1	8.9	10.3	10.1
+	----	----	----	----	----

ISOLATIONS (dB) (LO AT +13dBm)

LO(MHz)	L-I	L-R
2000	22	21
3000	26	25
4000	30	30
5000	31	33
6000	30	32
7000	29	35
8000	29	38
9000	33	39
10000	39	32
11000	40	30
12000	36	30
13000	43	26
14000	43	27
15000	38	28
16000	33	27
17000	31	26
18000	31	24

DATE:101486
DATE: _____ FM8B S/N 320

C BAND — 4.0 GHz - 8.0 GHz

Model No. Isolator	Model No. Circulator	Frequency GHz	Isolation dB Min.	Loss dB Max.	VSWR Max.	Length x Width x Height Inches
STANDARD BANDWIDTHS						
CTD2011	CTD2012	4.00-6.00	20	.4	1.20	1.00 x 1.00 x .50
CTA2013	CTA2014	4.20-4.40	23	.3	1.15	.75 x .75 x .50
CTC2015	CTC2016	4.40-5.00	23	.3	1.15	.75 x .75 x .50
CTB2017	CTB2018	5.40-5.90	23	.3	1.15	.63 x .63 x .50
CTB2019	CTB2020	5.90-6.40	23	.3	1.15	.63 x .63 x .50
CTF2029	CTF2030	6.20-8.40	20	.4	1.25	1.00 x 1.00 x .50
CTF2031	CTF2032	6.00-8.00	23	.4	1.15	1.00 x 1.00 x .50
CTF2033	CTF2034	7.05-10.00	23	.4	1.15	1.00 x 1.00 x .50
BROADBAND AND OCTAVE BANDWIDTHS						
CTH2035	CTH2036	4.00-8.00	18	.4	1.28	1.00 x 1.00 x .50
CTH2037	CTH2038	4.30-8.30	18	.4	1.28	1.00 x 1.00 x .50
CTH2039	CTH2040	4.30-9.30	17	.5	1.35	1.00 x 1.00 x .50
CTH2041	CTH2042	5.2-10.2	17	.5	1.35	1.00 x 1.00 x .50

X BAND — 8.0 GHz - 12.4 GHz

Model No. Isolator	Model No. Circulator	Frequency GHz	Isolation dB Min.	Loss dB Max.	VSWR Max.	Length x Width x Height Inches
XTD2009	XTD2010	7.0-10.0	20	.4	1.25	.75 x .75 x .55
XTG2011	XTG2012	7.0-11.0	20	.4	1.25	1.00 x 1.00 x .50
XTB2013	XTB2014	7.2- 7.8	23	.3	1.15	.75 x .75 x .55
XTE2015	XTE2016	7.5-10.0	20	.4	1.25	.75 x .75 x .55
XTB2017	XTB2018	7.9- 8.4	23	.3	1.15	.75 x .75 x .55
XTE2019	XTE2020	8.2-10.2	23	.3	1.15	.75 x .75 x .55
XTE2021	XTE2022	8.0-12.4	20	.4	1.25	.75 x .75 x .55
XTC2023	XTC2024	8.5- 9.6	23	.3	1.15	.75 x .75 x .55
XTB2025	XTB2026	10.7-11.7	23	.3	1.15	.75 x .75 x .55
XTC2027	XTC2028	11.7-13.2	20	.4	1.25	.75 x .75 x .55
XTE2029	XTE2030	11.8-14.8	20	.4	1.25	.75 x .75 x .55

P BAND — 12.4 GHz - 18.0 GHz

Model No. Isolator	Model No. Circulator	Frequency GHz	Isolation dB Min.	Loss dB Max.	VSWR Max.	Length x Width x Height Inches
PTB2007	PTB2008	12.0-14.0	23	.3	1.15	.55 x .55 x .55
PTB2009	PTB2010	13.0-15.0	23	.3	1.15	.55 x .55 x .55
PTH2011	PTH2012	11.0-18.0	18	.5	1.30	.63 x .75 x .55
PTE2013	PTE2014	12.0-15.2	20	.4	1.25	.63 x .75 x .55
PTE2015	PTE2016	12.4-16.0	20	.4	1.25	.63 x .75 x .55
PTG2017	PTG2018	12.4-18.0	20	.5	1.25	.63 x .75 x .55
PTA2019	PTA2020	14.0-14.5	23	.3	1.15	.55 x .55 x .55
PTC2021	PTC2022	14.4-16.4	23	.3	1.15	.55 x .55 x .55
PTC2023	PTC2024	16.0-18.0	23	.3	1.15	.55 x .55 x .55
PTC2025	PTC2026	16.4-18.4	23	.4	1.15	.55 x .55 x .55
PTB2027	PTB2028	17.0-18.0	23	.4	1.15	.55 x .55 x .55
PTB2029	PTB2030	18.0-19.0	23	.4	1.15	.55 x .55 x .55

PAssive Microwave TECHnology
CANOGA PARK, CALIFORNIA

ENGINEER: Guy Hayes — CUST. P/N:
DATE: 2/20/97 — CUST. P/O:
TEMPERATURE: Amb — WORK ORDER 2398
QA: (PANTECH ENG)

ISOLATOR TEST DATA

MODEL NO. PTB2007 — SERIAL NO. 123 - 133

FREQUENCY (GHZ) 12 / 14	INPUT VSWR	OUTPUT VSWR	INSERTION LOSS	ISOLATION
12.177	≥ 1.10	≥ 1.13	≤ 0.30	> 27
124	≥ 1.15	≥ 1.13	≤ 0.30	≥ 25
125	≥ 1.15	≥ 1.08	≤ 0.30	> 27
126	≥ 1.10	≥ 1.10	≤ 0.30	≥ 29
127	≥ 1.13	≥ 1.12	≤ 0.30	≥ 28
128	≥ 1.09	≥ 1.13	≤ 0.30	≥ 25
129	≥ 1.12	≥ 1.12	≤ 0.30	≥ 30
130	≥ 1.13	≥ 1.11	≤ 0.25	≥ 23
131	≥ 1.13	≥ 1.08	≤ 0.25	≥ 30
132	≥ 1.09	≥ 1.10	≤ 0.38	> 27.5
133	≥ 1.13	≥ 1.12	≤ 0.30	≥ 25
SPECIFICATION LIMITS	1.15 :1 MAX	1.15 :1 MAX	0.30 db MAX	23 db MIN

ISOLATOR TEST 3-4-87

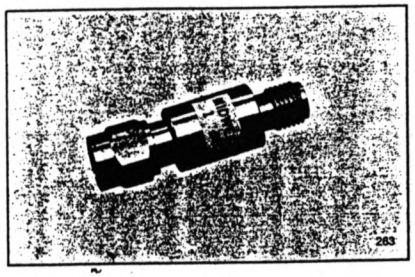
Model # PTB2007 Ser# 123 — 133

Frequency 15 GHz

S/N	INPUT R/L	OUTPUT R/L	ISOLATION R/L	F/LOSS
125	≥ 30 dB	30 dB	26 dB	0.20 dB
129	> 30 dB	30	≥ 29	0.25
124	> 30 dB	30	24	0.30
123	> 30 dB	30	28	0.15
133	> 30 dB	30	27.5	0.32
131	> 30 dB	30	> 30	0.20
132	> 30 dB	30	28	0.23
127	> 30 dB	30	29	0.32
130	> 30 dB	30	26	0.3
126	> 30 dB	30	27	0.25
128	> 30 dB	30	30	0.1

FIXED ATTENUATORS
SMA

MINIATURE*



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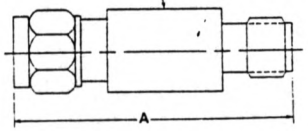
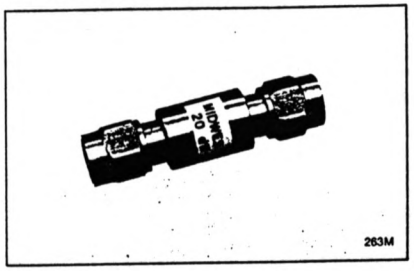


ATTENUATION VALUE	LENGTH A
1-20 dB	1.20
21-60 dB	1.49

MINIATURE DOUBLE MALE



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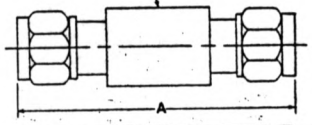
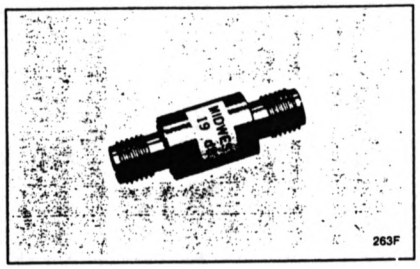


ATTENUATION VALUE	LENGTH A
1-20 dB	1.33
21-60 dB	1.62

MINIATURE DOUBLE FEMALE



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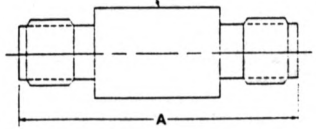


ATTENUATION VALUE	LENGTH A
1-20 dB	1.07
21-60 dB	1.36

DC TO 18 GHz HIGH PERFORMANCE SPECIFICATIONS

MODELS 263, 263M AND 263F
FREQUENCY RANGE: DC TO 18GHz
CONNECTOR TYPE: STAINLESS STEEL SMA PER MIL-C-39012
ATTENUATION VALUES: 1 THRU 60dB IN 1dB INCREMENTS
ATTENUATION ACCURACY: 1 - 10dB ±0.3dB ■ 11 - 20dB ±0.5dB ■ 21 - 40dB ±1.0dB ■ 41 - 60dB ±1.5dB
MAXIMUM VSWR: DC TO 4.0 GHz **1.15** ■ 4.0 TO 12.4 GHz **1.25** ■ 12.4 TO 18 GHz **1.35**
MAXIMUM INPUT POWER: 2 WATTS AVERAGE AT +25°C DERATED LINEARLY TO 0.5 WATTS AT +125°C
OPERATING TEMPERATURE RANGE: -65°C TO +125°C

DC TO 8.0 GHz HIGH PERFORMANCE SPECIFICATIONS

MODELS 292, 292M AND 292F
FREQUENCY RANGE: DC TO 8.0 GHz
CONNECTOR TYPE: STAINLESS STEEL SMA PER MIL-C-39012
ATTENUATION VALUES: 1 THRU 30dB IN 1dB INCREMENTS
ATTENUATION ACCURACY: 1 - 10dB ±0.3dB ■ 11 - 20dB ±0.5dB ■ 21 - 30 dB ±1.0dB
MAXIMUM VSWR: 1.07 +0.015fGHz
MAXIMUM INPUT POWER: 2 WATTS AVERAGE AT +25°C DERATED LINEARLY TO 0.5 WATTS AT +125°C
OPERATING TEMPERATURE RANGE: -65°C TO +125°C

DC TO 2.0 GHz HIGH PERFORMANCE SPECIFICATIONS

MODELS 294, 294M AND 294F
FREQUENCY RANGE: DC TO 2.0 GHz
CONNECTOR TYPE: STAINLESS STEEL SMA PER MIL-C-39012
ATTENUATION VALUES: 1 THRU 30dB IN 1dB INCREMENTS
ATTENUATION ACCURACY: 1 - 20dB ±0.3dB ■ 21 - 30dB ±0.5dB
MAXIMUM VSWR: 1.15
MAXIMUM INPUT POWER: 2 WATTS AVERAGE AT +25°C DERATED LINEARLY TO 0.5 WATTS AT +125°C
OPERATING TEMPERATURE RANGE: -65°C TO +125°C

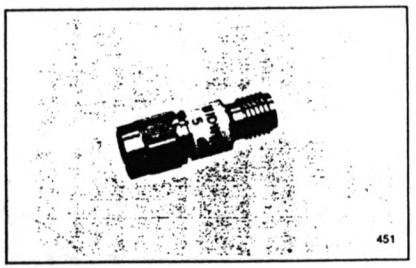
DC TO 18 GHz INEXPENSIVE SPECIFICATIONS

MODELS 444, 444M AND 444F
FREQUENCY RANGE: DC TO 18 GHz
CONNECTOR TYPE: STAINLESS STEEL SMA PER MIL-C-39012
ATTENUATION VALUES: 1 THRU 30dB IN 1dB INCREMENTS
ATTENUATION ACCURACY:

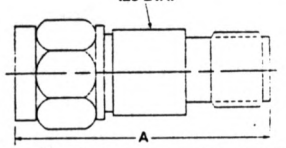
DC TO 12.4 GHz		12.4 TO 18 GHz	
1-4dB	±0.75dB	1-4dB	±0.75dB
5-8dB	±0.75dB	5-8dB	±1.00dB
9-12dB	±1.00dB	9-12dB	±1.25dB
13-20dB	±1.50dB	13-20dB	±1.50dB
21-30dB	±2.0dB	21-30dB	±2.0dB

MAXIMUM VSWR: DC TO 4.0 GHz **1.25** ■ 4.0 TO 12.4 GHz **1.45** ■ 12.4 TO 18 GHz **1.65**
MAXIMUM INPUT POWER: 2 WATTS AVERAGE AT +25°C DERATED LINEARLY TO 0.5 WATTS AT +125°C
OPERATING TEMPERATURE RANGE: -65°C TO +125°C

TYPE II*



.28 DIA.



ATTENUATION VALUE	LENGTH A
1-10 dB	.86
20 dB	1.02

DC TO 18 GHz SPECIFICATIONS

MODELS 451, 451M AND 451F
FREQUENCY RANGE: DC TO 18 GHz
CONNECTOR TYPE: STAINLESS STEEL SMA PER MIL-C-39012
ATTENUATION VALUES: 1 THRU 10dB IN 1dB INCREMENTS AND 20dB
ATTENUATION ACCURACY: 1 - 6dB ±0.3dB ■ 7 - 10dB AND 20dB ±0.5dB
MAXIMUM VSWR: DC TO 4.0 GHz **1.12** ■ 4.0 TO 8.0 GHz **1.15** ■ 8.0 TO 18 GHz **1.20**
MAXIMUM INPUT POWER: 2 WATTS AVERAGE AT +25°C DERATED LINEARLY TO 0.5 WATTS AT +125°C

DC TO 12.4 GHz SPECIFICATIONS

MODELS 452, 452M AND 452F
FREQUENCY RANGE: DC TO 12.4 GHz
CONNECTOR TYPE: STAINLESS STEEL SMA PER MIL-C-39012
ATTENUATION VALUES: 1 THRU 10dB in 1dB INCREMENTS AND 20dB
ATTENUATION ACCURACY: 1 - 6dB ±0.3dB ■ 7 - 10dB AND 20dB ±0.5dB
MAXIMUM VSWR: DC TO 4.0 GHz **1.12** ■ 4.0 TO 8.0 GHz **1.15** ■ 8.0 TO 12.4 GHz **1.20**
MAXIMUM INPUT POWER: 2 WATTS AVERAGE AT +25°C DERATED LINEARLY TO 0.5 WATTS AT +125°C
OPERATING TEMPERATURE RANGE: -65°C TO +125°C

* U.S. Patent number 3,824,506 applies to all Type II Fixed Attenuators.

* U.S. Patent numbe. 3,824,506

OCTAVE AND BROAD BANDWIDTH CIRCULATORS AND ISOLATORS

TRAK octave and broad bandwidth circulators and isolators represent the state-of-the-art in miniaturization of broadband ferrite components. These devices are enclosed in steel cases to provide magnetic shielding and to make them extremely rugged.

Only distributed parameter matching is used to assure greater stability and more uniform characteristics than units designed with lumped-constant matching. Miniaturization of TRAK units has been accomplished while maintaining microwave characteristics equal to or better than those of other manufacturers. Use of ferrite materials from TRAK's own ferrite lab helps assure high quality and on-time delivery. TRAK's unique designs provide the utmost in phase linearity, repeatability and freedom from "glitches."

Applications include EW systems, radar systems, microwave landing systems, communications systems, navigation equipment, missiles, telemetry systems and transponders.

CIRCULATORS

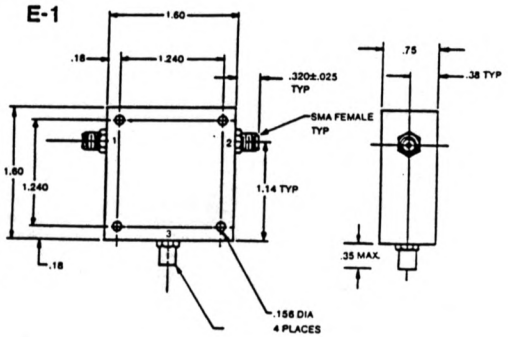
FREQ. RANGE (GHz)	MODEL #	ISOLATION dB min.	INSERTION LOSS dB max.	VSWR max.	OPERATING TEMP. °C	POWER RATING: PEAK POWER KW	POWER RATING: AVERAGE POWER WATTS	POWER RATING: HEAT SINK TEMP. °C	OUTLINE Pg. F-7
1.0-2.0	50A1101	15	0.6	1.40	0 to +50	0.2	100	+35	E-1
2.0-4.0	50A3001	18	0.5	1.30	-10 to +70	0.6	125	+40	F-1
2.6-5.2	50A3011	18	0.5	1.30	-25 to +80	1.0	125	+45	F-1
3.0-6.0	50A6301	18	0.5	1.40	-45 to +85	1.0	125	+50	G-1
4.0-8.0	50A6001	18	0.5	1.30	-45 to +95	2.0	125	+50	G-1
5.0-10.0	50A6071	18	0.5	1.30	-55 to +95	0.5	125	+50	G-1
6.0-12.0	50A9201	16	0.7	1.35	-55 to +95	0.5	75	+50	G-1
8.0-12.4	10B9201	20	0.5	1.30	-55 to +110	0.5	75	+50	H-1
8.0-16.0	50A2001	17	0.5	1.35	-40 to +95	0.5	65	+50	H-1
12.0-18.0	10B2201	18	0.5	1.30	-55 to +110	2.0	50	+50	H-1
8.0-18.0	50A2051	14	0.6	1.50	-54 to +95	0.5	65	+50	H-1
18.0-22.0	10A8101	18	0.7	1.30	-54 to +95	0.5	65	+50	H-1

ISOLATORS

FREQ. RANGE (GHz)	MODEL #	ISOLATION dB min.	INSERTION LOSS dB max.	VSWR max.	OPERATING TEMP. °C	POWER RATING: PEAK POWER KW	POWER RATING: AVERAGE POWER WATTS	POWER RATING: HEAT SINK TEMP. °C	OUTLINE Pg. F-7
1.0-2.0	60A1101	15	0.6	1.40	0 to +50	0.2	1.0	+35	E-1
2.0-4.0	60A3001	18	0.5	1.30	-10 to +70	0.6	1.0	+40	F-1
2.6-5.2	60A3011	18	0.5	1.30	-25 to +80	1.0	1.0	+45	F-1
3.0-6.0	60A6301	18	0.5	1.40	-45 to +85	0.1	1.0	+50	G-1
4.0-8.0	60A6001	18	0.5	1.30	-45 to +95	2.0	1.0	+50	G-1
5.0-10.0	60A6071	18	0.5	1.30	-55 to +95	0.5	2.0	+50	G-1
6.0-12.0	60A9201	16	0.7	1.35	-55 to +95	0.1	1.0	+50	G-1
8.0-12.4	20B9201	20	0.5	1.30	-55 to +110	0.5	3.0	+50	H-1
8.0-16.0	60A2001	17	0.5	1.35	-40 to +95	0.5	3.0	+50	H-1
7.5-18.0	60C2051	14	0.9	1.50	-54 to +95	0.5	3.0	+50	H-1
12.0-18.0	20B2201	18	0.5	1.30	-55 to +110	2.0	3.0	+50	H-1
8.0-18.0	60A2051	14	0.6	1.50	-54 to +95	0.5	3.0	+50	H-1
18.0-22.0	20A8101	18	0.7	1.30	-54 to +95	0.5	3.0	+50	H-1

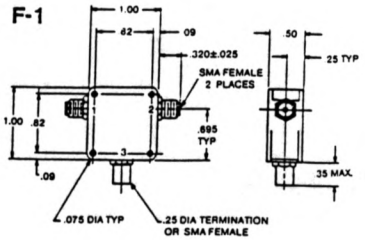
weight
11.5 oz. (nominal)

E-1



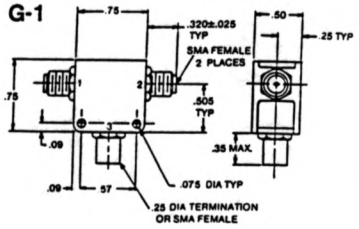
weight
1.4 oz. (nominal)

F-1



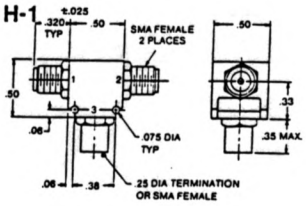
weight
1.0 oz. (nominal)

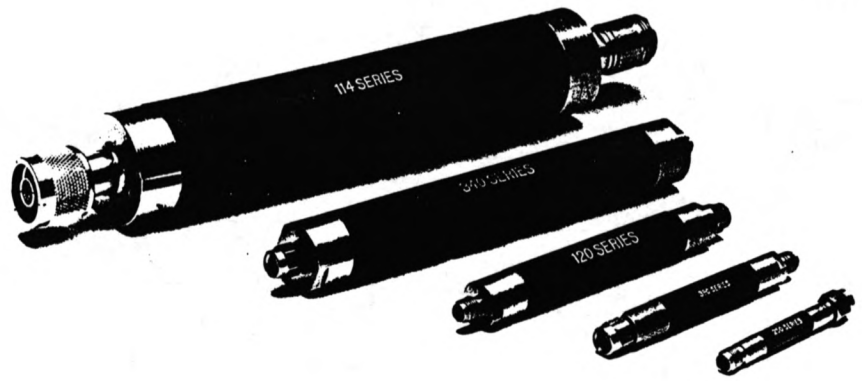
G-1



weight
0.5 oz. (nominal)

H-1





Features

K&L tubular bandpass filters are available in five different series ranging in size from ¼ inch diameter to 1¼ inch diameter to cover the frequency range of 15 MHz to 5.0GHz. K&L uses a .05 Chebychev design to yield low insertion loss in the passband and high attenuation levels in the stopband. The tubular filter design is made up of small resonating sections. These sections are capacitively coupled to provide the specified passband response and selectivity required. This coupling structure provides a DC block.

In choosing the best tubular filter to meet the user's needs, K&L recommends the use of the ½ inch diameter, model B120. This series has convenient size, broad frequency range, versatility of design, and is the most economical.

The two larger series, ¾ inch diameter and 1¼ inch diameter, offer the user lower insertion loss, lower frequency operation, and higher power capabilities. The two smaller diameter filter series, ⅜ inch diameter and ¼ inch diameter, offer the user miniature size and volume, higher frequency operations and less weight.

Mechanical

For sizes and connectors, see page 66.

NOTE:

For a detailed explanation of changes to K&L's part numbering system, see page 32

To Order

5	B121	–	500/T80	–	O/O
1	2 3 4		5 6 7		8 9

1. Number of sections
2. B—Bandpass
3. Size designation
   - 250 — .250″
   - 380 — .375″
   - 120 — .500″
   - 340 — .750″
   - 110 — 1.250″
4. Circuit Indicator
5. Center Frequency
6. Supplemental codes. (See page 32)
7. Bandwidth
8. Input connector
9. Output connector

Specifications

Model	Diameter Inches	Frequency Range (MHz)	3dB BW (% of Center Freq.)	VSWR	No. of Sections	Impedance (Ohms (2))	Avg. Power (Watts)	Shock	Vibration	Humidity	Temp. Range
B250	1/4	200–6,000(3)	3–70%(1)	1.5:1 or Less	2–8	50 75	2	30G. 11ms	10 G 5–2,000 Hz	0–95%	– 55°C to + 85°C
B380	3/8	200–4,000	3–70%(1)	1.5:1 or Less	2–8	50 75	5	30G. 11ms	10 G 5–2,000 Hz	0–95%	– 55°C to + 85°C
B120*	1/2	50–3,900	1–70%	1.5:1 or Less	2–12	50 75	18	30G. 11ms	10 G 5–2,000 Hz	0–95%	– 55°C to + 85°C
B340	3/4	25–1,700	1–80%	1.5:1 or Less	2–12	50 75	40	30G. 11ms	10 G. 5–2,000 Hz	0–95%	– 55°C to + 85°C
B110	1-1/4	15–1,000	1–80%	1.5:1 or Less	2–12	50 75	200	30G. 11ms	10 G 5–2,000 Hz	0–95%	– 55°C to + 85°C

***Most versatile • Fits most applications • Immediate delivery**

(1) For frequency below 400MHz. %3dB Bandwidth range from 3% to 40%
(2) 50 Ohms standard
(3) For frequency above 6,000MHz, combline and interdigital filters are better suited

Insertion Loss / Loss Constant

LOSS CONSTANT VS. FREQUENCY VS. MODEL

	Center Frequency (MHz)										
Model	15 25	26 40	41 50	51 65	66 100	101 200	201 400	401 1,000	1,001 2,000	2,001 4,000	4,001 6,000
B250						5.0	5.0	4.0	3.5	3.0	2.5
380						4.0	3.0	2.5	2.0	1.8	
B120				4.0	3.5	3.0	2.5	2.0	1.8	1.6	
B340		3.5	3.0	2.5	2.2	2.0	1.6	1.4	1.2		
B110	2.6	2.5	2.4	2.2	1.8	1.6	1.3	1.2			

To determine the maximum insertion loss of the tubular filter at center frequency the following formula is used:

Insertion loss at Center frequency =

$$\frac{(\text{Loss constant})(\text{No. of sections} + \frac{1}{2})}{\%3\text{dB BW}} + 0.2$$

EXAMPLE:

Center frequency = 500MHz
3dB Bandwidth = 80MHz
Number of sections = 5
Filter model: B120
Find the insertion loss at Center frequency
From the table the Loss constant is shown to be 2.0
Number of sections = 5
The percent 3dB bandwidth is:

$$\frac{3\text{dB BW}(100)}{\text{Center freq.}} = \frac{(80)(100)}{500} = 16\%$$

By substituting in the formula we find the insertion loss =

$$\frac{(2)(5 + \frac{1}{2})}{16} + 0.2 = 0.88\text{dB}$$

Phone 301 749-2424 • TWX 710 864 9683 • FAX 301 749 5725

REACTEL, INC.

687-D LOFSTRAND LANE, ROCKVILLE, MD 20850. TEL: ~~(301)~~ 702 279-5535

TEST DATA

Date: 3/6/1987

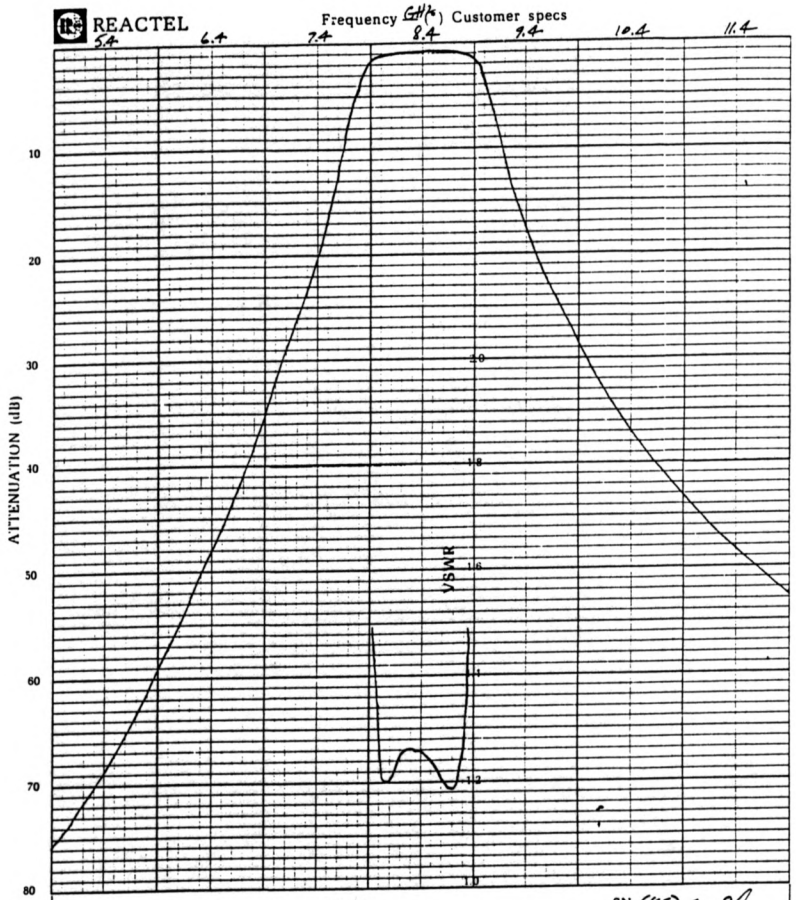
REACTEL'S P/N. 4CO-8400-1000S12 TEST ENGINEER: C. Hashiguri

SERIAL NO'S (85) 21-44 VERIFIED BY:

CUSTOMER'S P/N. Q.C. INSPECTOR:

TEST RESULTS

SERIAL NUMBERS	21-44									
SPEC'S										
1.0: Center freq.: 8.4 GHz	8.46									
2.0: Insertion Loss at: fo = 1dB	1dB									
RELATIVE B.W.										
3.0: 3 dB BW ..... to										
3.1: 1dB BW 7900 to 8900MHz	✓									
REJECTIONS										
4.0: > ..... dB at										
4.1: > ..... dB at										
4.2: > ..... dB at										
VSWR (R.L.)										
5.0 < 1.5:1 at 7.93 to 8.84GHz nom	✓									
PHASE										
6.0: ± ..... degrees at										
GROUP DELAY										
7.0: ± ..... at										
CONNECTORS										
8.0: SMA female, SMA male	✓									
9.0: Size 1/4" x 0.375 x 2.6" T.T.	✓									
10.0: Others										
.....										



P.N. 4CO-8400-1000 S12 Job No. SN-(85) 3-18

Q.C. Inspection Mechanical by: EE Electrical by:

Tested by: R-H Date: 9-30-85 Impedance: 50Ω nom.

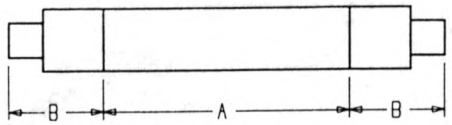
VSWR ≤ 1.5:1 over 7.93 - 8.84 GHz nom. BW 1dB = 7.86 - 8.94GHz, 3dB = 7.78 - 9.05 GHz fo 8.4GHz

Insertion loss = 1dB @ f_o Rejections TYPICAL 4 POLE RESPONSE

Linearity Time delay Power

The length of a tubular filter is determined by adding the "A" and "B" dimensions. The "B" dimension is obtained from the table below and the "A" dimension is obtained from Length vs. Frequency tables on the following page.

Example: A 4-section bandpass filter Model B120 with a center frequency of 1,200MHz and with SMA connectors has an "A" dimension of 2 inches, and a "B" dimension of .08 inches. The total length is 3.6 inches since there is a connector at each end of the filter.



Connector Length Table

CONNECTOR STYLE	Connector Code	"B" DIMENSION (Inches) 1/4 Dia.	3/8 Dia.	1/2 Dia.	3/4 Dia.	1¼ Dia.	Fig.	Frequency Range
"N" Female	N	NR*	1.28	1.28	1.4	1.7		* *
"N" Male	NP	NR*	1.23	1.23	1.31	1.65		* *
BNC Female	B	NR*	1.0	1.0	1.35	1.42		DC-1 GHz
BNC Male	BP	NR*	.93	.93	1.45	1.35		DC-1 GHz
TNC Female	T	NR*	1.0	1.0	1.35	1.42		DC-10 GHz
TNC Male	TP	NR*	.93	.93	1.45	1.35		DC-10 GHz
SMC Female (Screw On)	S	.6	.73	.73	.73	.73		DC-4 GHz
SMC Male (Screw On)	SP	NR*	.81	.81	.81	.81		DC-4 GHz
SMB Female (Snap On)	A	.6	.73	.73	.73	.73		DC-4 GHz
SMB Male (Snap On)	AP	NR*	.81	.81	.81	.81		DC-4 GHz
"F" Female	F	NR*	NR*	1.05	1.05	1.05		DC-800 MHz
SMA Female (Standard)	O	.6	.8	.8	.8	.8		DC-20 GHz
SMA Female (Right Angle)	DO	NR*	.6	.6	.6	.6	2	DC-3 GHz
SMA Female (Right Angle Square)	EO	.55	.65	.65	.65	.65	5	DC-3 GHz
SMA Male (Standard)	OP	.73	.85	.85	.85	.85		DC-20 GHz
SMA Male (Right Angle)	DP	NR*	.6	.6	.6	.6	2	DC-3 GHz
SMA Male (Right Angle Square)	EP	.55	.65	.65	.65	.65	5	DC-3 GHz
Cable, RG 188 (Right Angle Standard)	C	.45	.5	.5	.5	.5	1	DC-3 GHz
Cable, RG 188 (Straight)	CS	.45	.55	.55	.55	.55	4	DC-3 GHz
Solder Lug	L	.40	.45	.45	.45	.45	6	DC-20 GHz
PC Mount (Right Angle)	P	*	*	*	*	*	*	*

RT. ANGLE CABLE 6" RG-188/U

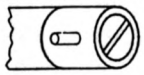


FIGURE 1

RT. ANGLE SMA-FEMALE OR MALE

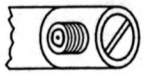


FIGURE 2

STRAIGHT CABLE

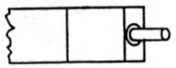


FIGURE 4

RT. ANGLE FLUSH MOUNT

FIGURE 5

SOLDER LUG

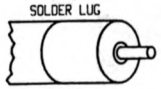


FIGURE 6

NR* = Not Recommended

* For PC Mount, contact factory.

Phone 301-749-2424 • TWX 710-864-9683 • FAX 301-749-5725

Tubular Filters

Approximate* Dimension "A" - Length vs. Frequency

*If dimensions are critical, contact factory for exact dimensions

B250

No. of Sections	Frequency (MHz) 150-200	201-300	301-400	401-3,000	3,001-6,000
2	1¾	1½	1½	1	
3	2¾	2¼	2½	1½	⅜
4	3¾	3½	3¼	2	1½
5	4¾	4¼	3¾	2½	1½
6	5¾	5	4¼	3	1½
7	6¾	5¾	4¾	3½	2
8	7¾	6½	5¼	4	2½
9	8¾	7¾	5¾	4½	
10	9¾	8	6¼	5	

B380

No. of Sections	Frequency (MHz) 160-200	201-800	801-1,200	1,201-2,000	2,001-4,000
2	3		1¼	1½	1
3	4¼	3½	2	1¾	1¼
4	5	2¾	2½	2	1½
5	5½	3¼	3	2½	2
6	6¼	4	3½	2¾	2¼
7	6¾	4¾	4	3¼	
8	7½	5½	4½	3¾	
9	8	6¼	5	4	
10	8½	7	5½	4½	

B120

No. of Sections	Frequency (MHz) 50-65	66-90	91-130	131-180	181-350	351-700	701-2,000	2,001-3,900
2	5	3	2½	2	1¾	1	1	¼
3	7¼	4	3¼	2¾	2¼	1¼	1¼	1
4	9½	5½	4½	3¾	3	2	2	1½
5	11¾	7¼	5¾	4¾	3¾	2¾	2½	2
6	14	9¼	7	5¾	4½	3½	3	2½
7	16¼	11¼	8¼	6¾	5¼	4¼	3½	3
8	18½	13¼	9½	7¾	6	5	4	3½
9	20¾	15¼	10¾	8¼	6¾	5¼	4½	4
10	23	17¼	12	9¾	7½	6½	5	4½

B340

No. of Sections	Frequency (MHz) 25-35	36-50	51-75	76-140	141-230	231-500	501-1,700
2	6¼	5	4½	3	2¼	1½	1½
3	9	7	6½	3½	3	2	2
4	11¾	9½	8	4	3½	2½	2½
5	13½	12	9½	5½	4¼	3¼	3¼
6	16¼	14½	12	7	5	4	3¼
7	19	17	13½	8½	5¾	4¾	4¼
8	21¾	19½	15	9½	6½	5½	4¾
9	24¼	22	16½	10½	7¼	6¼	5¼
10	27¼	24½	18	11½	8	7	5¾

B110

No. of Sections	Frequency (MHz) 15-22	23-40	41-55	56-80	81-200	201-400	401-1,000
2	10	4	4	3¾	3½	3	2
3	13	7	5	4½	4	3½	2½
4	17	9	7	6	5	4	3
5	21	11	9	7½	6¼	5	3¼
6	25	14	11	9	7½	6	4½
7	29	17	13	10½	8¾	7	5¼
8	33	20	15	12	10	8	6
9	37	23	17	13½	11¼	9	6¾
10	41	26	19	15	12¼	10	7½

WEIGHT (ounces)

	B380	B120	B340	B110
	¼ oz. per inch	½ oz. per inch	¼ oz. per inch	¼ oz. per inch	½ oz. per inch

L250

No. of Sections	Frequency (MHz) 100-200	201-300	301-800	801-2,000	2,001-4,000	4,001-7,000	7,001-11,000	11,001-20,000
2	1¾	1½	1	1	½			
3	2½	1¾	1½	1½	¾	1	5/8	
4	3¼	2¼	1½	1¾	1	1	¾	1/4‡
5	4	2¾	2	2	1¼	1½	7/8	3/8‡
6	4¾	3½	2¼	2¼	1½	1	1	1/2‡
7	5½	3¾	2½	2½				
8	7¼	4¼	3	2¾				
9	8	4¾	3½	3½				
10	8¾	5¼	4	3¾				

L380

No. of Sections	Frequency (MHz) 100-210	211-350	351-600	601-1,200	1,201-4,000
2	2½	1¾	1	1½	¾
3	3½	2	1½	2¼	1½
4	4½	2¾	2	3	1¾
5	5½	3½	2½	3½	2¼
6	6½	4¼	3	4	2½
7	7½	5	3½	4½	
8	8½	5¾	4	5	
9	9½	6½	4½	5½	
10	10½	7¼	5	6	

L120

No. of Sections	Frequency (MHz) 40-60	61-70	71-90	91-150	151-210	211-600	601-1,900	1,901-4,000
2	4	3	2½	2	1½	1¼	1	¾
3	7	5	4	3½	2¼	2	1¼	1¼
4	9	7	5½	4½	3	2½	1½	1½
5	11	9	7	5½	3¾	3	1¾	2
6	13	11	8½	6½	4¼	3½	2¼	2½
7	16	13	10	7½	5¼	4	2¾	3
8	18	15	11½	8½	6	4¾	4½	3½
9	20	17	13	9½	6¾	5	4¾	4
10	22	19	14½	10½	7½	5½	5	4½

L340

No. of Sections	Frequency (MHz) 25-40	41-50	51-80	81-140	141-400	401-1,000	1,001-2,000
2	5	2¾	2½	2	1½	1½	1½
3	8½	5½	4½	3½	2¾	3½	2¼
4	12	7¾	6½	4	3	4	2¾
5	15	10	8½	4½	3¾	4½	3¼
6	18	12¾	10	5¾	4½	5¾	3¾
7	21	15¾	11	6½	5¾	6½	4½
8	24	18	12½	7¼	6	7¼	5¼
9	27	20¾	14	8	6¾	8	6
10	30	23½	15½	8¾	7½	8¾	6½

L110

No. of Sections	Frequency (MHz) 10-15	16-30	31-100	101-200	201-1,000
2	7	5	4	2½	2¼
3	11	7½	5½	3½	3
4	14	10	7	4½	3¾
5	17	12½	8½	5½	4½
6	20	15	10	6½	5¼
7	23	17½	11½	7½	6
8	26	20	13	8½	6¾
9	29	22½	14½	9½	7½
10	32	25	16	10½	8¼

WEIGHT (ounces)

L250	L380	L120	L340	L110
¼ oz. per inch	½ oz. per inch	¼ oz. per inch	¼ oz. per inch	1½ oz. per inch

Length shown above is less connectors. Dimensions and weight are approximate.

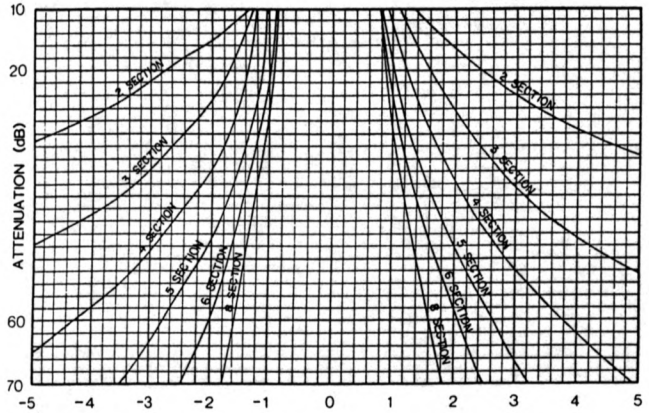
‡Occasionally a transmission line design may be indicated necessitating a longer body length

Phone 301-749-2424 • TWX 710-864-9683 • FAX 301-749-5725

The following curves are used in determining the out-of-band attenuation for K&L's five series of tubular filters. The curves show minimum stopband in dB, as multiples of 3dB bandwidth for filters with 2 through 8 sections.

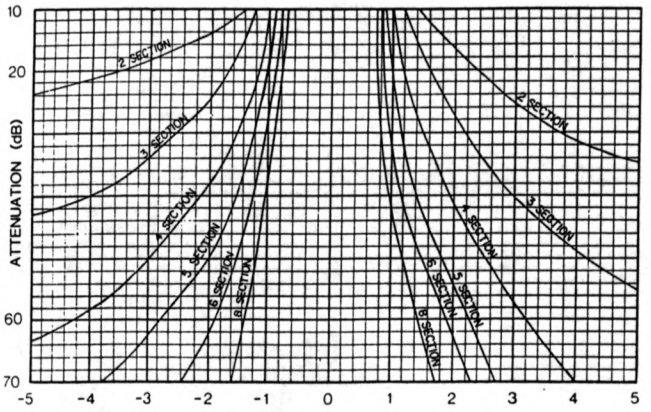
For the most part, K&L filters are free of spurious responses. However due to case moding or when resonance develops, spurious responses can occur. It is therefore advisable that the user specify the frequency which is to be spurious-free. By doing so, K&L can incorporate compensating networks to eliminate the spurious responses at no degradation in the passband frequencies.

2-5% BANDPASS



Important Note: The stopband attenuation curves shown are for specific schematics shown as figures 1 and 2 respectively on page 10. As this series is computer designed, necessitating unique component values, other schematics may be utilized which will yield different attenuation characteristics (e.g., steeper on the high frequency side of the passband and shallower on the low frequency side). Filter types such as elliptic function, linear phase, Butterworth of Gaussian may also be specified. For special requirements, consult the factory for specifications meeting your particular needs.

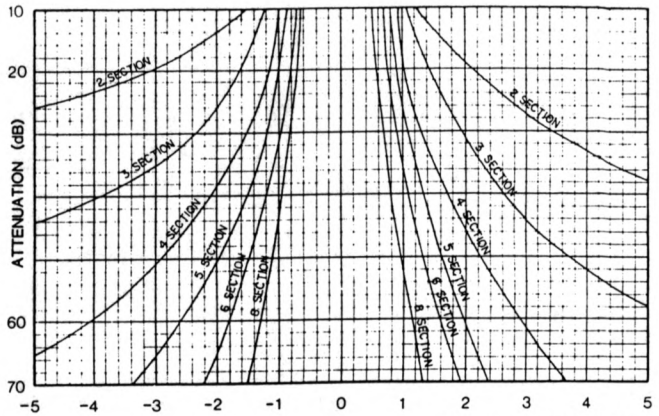
5-15% BANDPASS



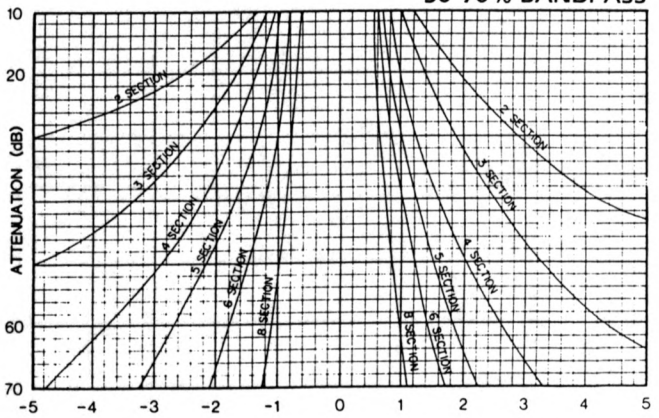
Phone 301 749-2424 • TWX 710 864 9683 • FAX 301 749 5725

Tubular Filters

15-30% BANDPASS



30-70% BANDPASS



To determine which series of curves to use, first calculate the percentage 3dB bandwidth from the formula:

$$\%BW = \frac{\text{3db BW}}{\text{Center freq.}} \times 100$$

To determine the number of bandwidths (3dB) from center frequency, use the following formula:

$$\text{3dB BW} = \frac{\text{Reject freq.} - \text{Center freq.}}{\text{93dB BW}}$$

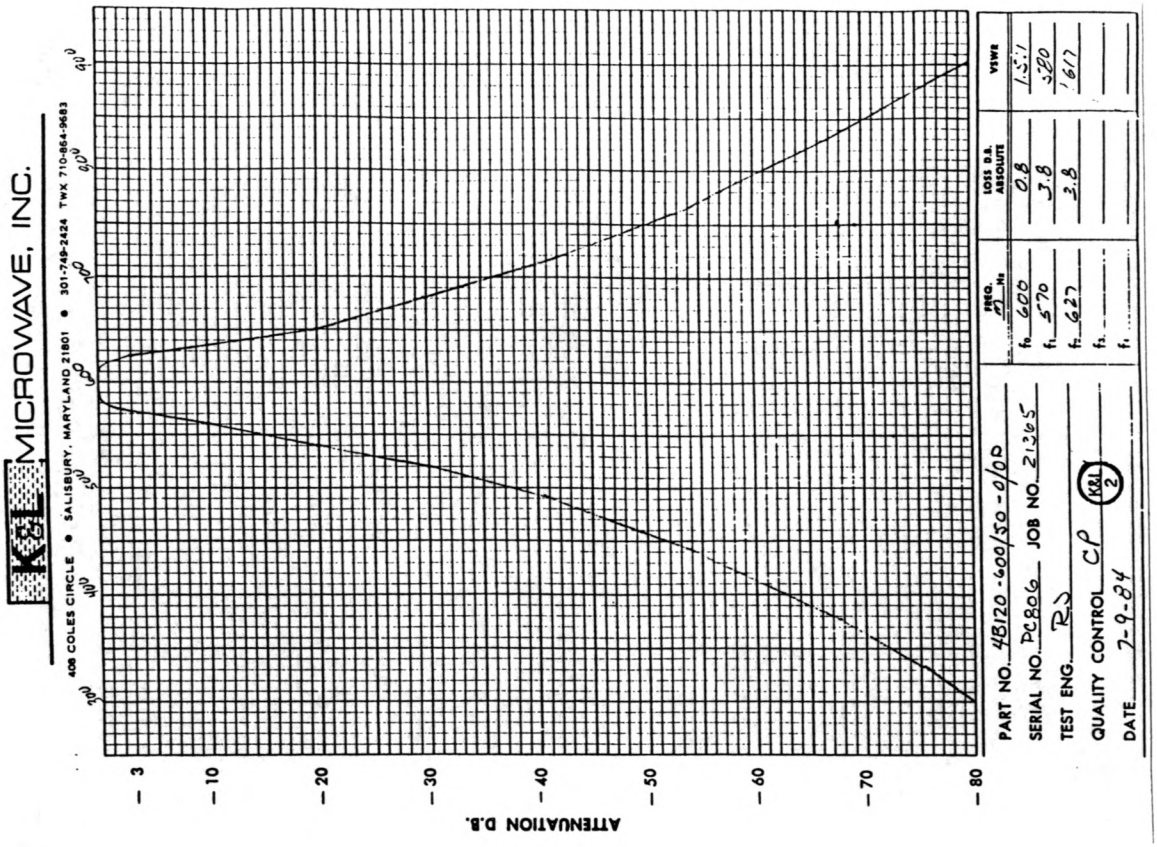
EXAMPLE:

Center frequency = 300MHz
3dB Bandwidth = 50MHz
Number of sections = 6
Determine attenuation at 200MHz and 400 MHz

1. Calculate % BW = $\frac{50 \times 100}{300}$ = 17%
2. −3dB BW = $\frac{200-300}{50}$ = −2 BW
3. +3dB BW = $\frac{400-500}{50}$ = +2 BW

Referring to the curve for 15%-30%, a 6-section response −2 BW yields 64dB, and +2 BW yields greater than 70dB.

Phone 301 749-2424 • TWX 710 864 9683 • FAX 301 749 5725



K&L MICROWAVE INCORPORATED
A DOVER TECHNOLOGIES COMPANY

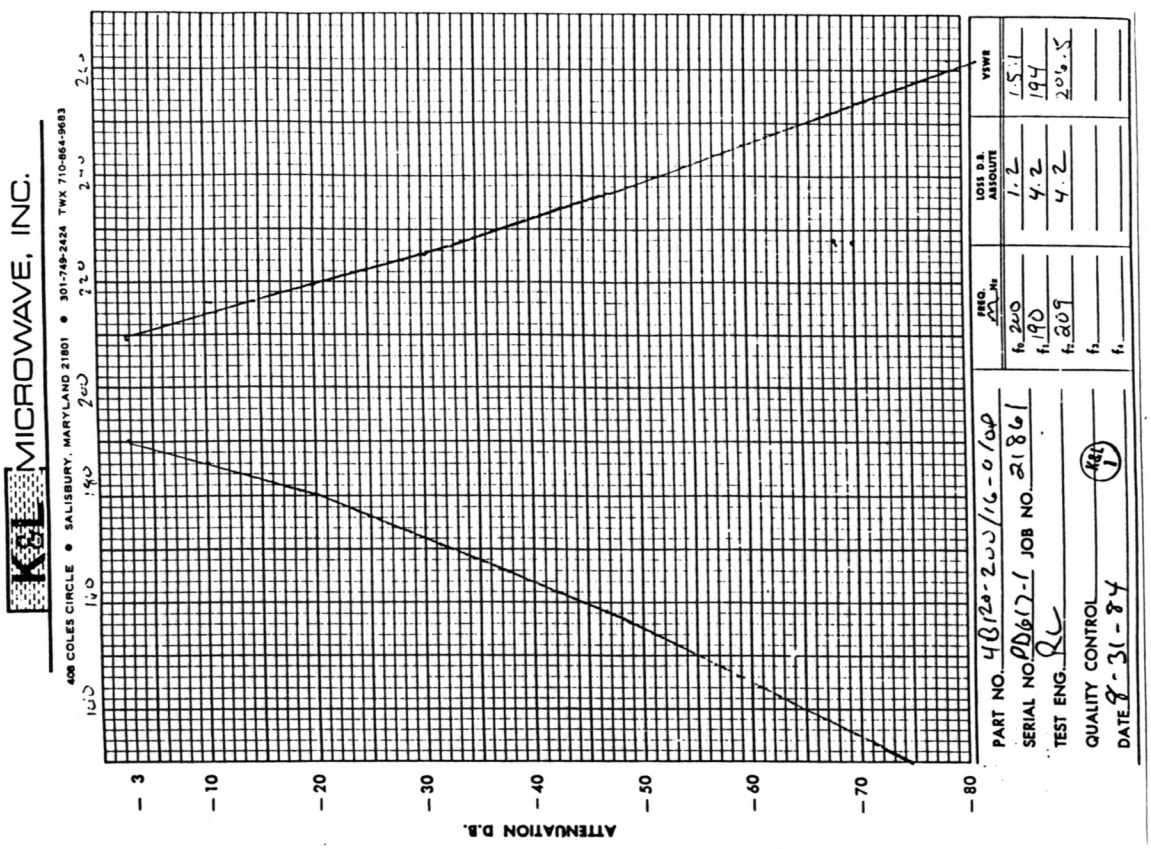
TEST DATA

K & L P/N 4B120-600/50-0/0P
CUSTOMER PART NO. _____
SERIAL NO. SG362-1 thru 11
PER ATP _____

K & L ORDER NO. 30952
TEST ENGINEER DD
Q.C. INSPECTOR mjh
DATE 2-12-87
(K&L 8)

TEST RESULTS

SPECIFICATIONS / SERIAL NO.	1	2	3	4	5	6	7	8	9	10	11
1.0 CENTER FREQUENCY 600 MHz											
2.0 RELATIVE BANDWIDTH											
2.1 ____ 3dB BW 575 MHz	572.2	570.3	572	571.5	572.2	572.1	571.3	571.6	571.2	571.1	571.2
625 MHz	625.6	626.9	626.9	627.8	626.1	626.1	627.2	627.4	626.3	626	626.4
____ BW ____ MHz											
____ MHz											
3.0 INSERTION LOSS											
600 MHz ____ dB	1.1	.9	1.0	1.0	1.0	1.3	.95	.9	1.0	.9	.9
____ MHz ____ dB											
4.0 VSWR 1.5:1											
Typ. MHz	578.3	577	578.2	577.4	577	576.6	576.7	577.5	577	576.3	577.3
____ MHz	621.3	622.1	622.2	622.8	621.9	623.1	621.7	622.8	621.4	621.7	621.9
5.0 PHASE ____ MHz											
____ MHz											
6.0 GROUP DELAY ____ MHz											
____ MHz											
7.0 STOPBAND REJECTION											
Curve MHz ____ dB											
____ MHz ____ dB											
____ MHz ____ dB											
____ MHz ____ dB											
8.0 OTHER ____											
9.0 MECHANICAL & MARKING											



K&L TEST DATA

K & L P/N 4B120-200/16-0/0P
CUSTOMER PART NO. /
SERIAL NO. RE139-1,8
PER ATP

K & L ORDER NO. 25882
TEST ENGINEER GV
Q.C. INSPECTOR RPT
DATE 9/6/85

K&L 9

SPECIFICATIONS SERIAL NO.	TEST RESULTS 1	2	3	4	5	6	7	8
1.0 CENTER FREQUENCY 200 MHz								
2.0 RELATIVE BANDWIDTH								
2.1 ____ 3dB BW 192 MHz	191.4	191.0	191.5	191.1	191.9	191.7	191.5	190.8
208 MHz	208.3	208.5	208.5	208.9	208.1	208.2	208.8	208.6
____ BW ____ MHz								
____ MHz								
3.0 INSERTION LOSS								
200 MHz 1.89 dB	1.3	1.3	1.3	1.3	1.7	1.3	1.4	1.3
____ MHz ____ dB								
4.0 VSWR 1.5:1								
typ MHz	194.0	193.2	193.0	193.1	193.0	193.4	193.7	193.0
____ MHz	209.4	209.0	206.3	206.9	206.6	206.8	209.0	206.1
5.0 PHASE ____ MHz								
____ ____ MHz								
6.0 GROUP DELAY ____ MHz								
____ ____ MHz								
7.0 STOPBAND REJECTION								
Curve MHz ____ dB								
____ MHz ____ dB								
____ MHz ____ dB								
____ MHz ____ dB								
8.0 OTHER								
9.0 MECHANICAL & MARKING								

Rev. 9/82

TECHNICAL DATA

WATKINS-JOHNSON

5 TO 600 MHz CASCADABLE AMPLIFIER WJ-A77-1

- HIGH OUTPUT LEVEL: +15 dBm (MIN)
- HIGH THIRD ORDER I.P.: +30 dBm (TYP)
- EXTENDED BANDWIDTH: 5-600 MHz
- WIDE POWER SUPPLY RANGE: +8 TO +15 VOLTS
- SMALL SIZE: TO-8

GUARANTEED SPECIFICATIONS*

Characteristic	Typical	0°-50°C	-54°C-+85°C
Frequency (Min.)	2-700 MHz	5-600 MHz	5-600 MHz
Small Signal Gain (Min.)	16.0 dB	15.0 dB	14.5 dB
Gain Flatness (Max.)	±0.3 dB	±0.7 dB	±1.0 dB
Noise Figure (Max.)	5.0 dB	6.5 dB	7.0 dB
Power Output at 1dB Compression (Min.)	+16.5 dBm	+15.0 dBm	+14.5 dBm
VSWR (Max.) Input/Output	<1.5:1	1.8:1	2.0:1
DC Current at 15 Volts (Max.)	50 mA	53 mA	56 mA

Second Order Harmonic Intercept Point: +49 dBm (Typ.)
Second Order Two Tone Intercept Point: +43 dBm (Typ.)
Third Order Two Tone Intercept Point: +30 dBm (Typ.)

*Measured in a 50 ohm system, at +15 Vdc Nominal

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature .....-54°C to +100°C
Storage Temperature .....-62°C to +125°C
Maximum Case Temperature .....105°C
Maximum DC Voltage .....+17 Volts

Maximum Continuous R.F. Input Power .....+13 dBm
Maximum Short Term R.F. Input Power (1 minute Maximum) ...+100 Milliwatts
Maximum Peak Power 0.5 Watt (3 μsec maximum)
"S" Series Burn-In Temperature ..100°C

*Supersedes WJ-A77-1 Technical Data Sheet dated Oct. 1978

NOTE: All testing per applicable internal Watkins-Johnson test procedures which are available upon request and are also subject to change without notice.

WATKINS-JOHNSON COMPANY
3333 Hillview Avenue, Palo Alto, California 94304
(415) 493-4141, TWX: 910-373-1253, TELEX: 348-415, CABLE: WJPLA

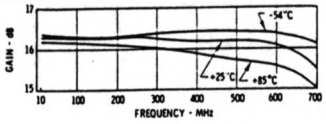
192A

JUNE 1980*

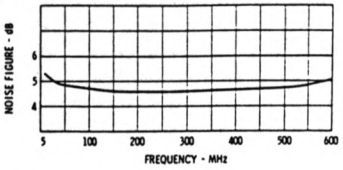
Specifications subject to change without notice

TYPICAL PERFORMANCE AT 25°C

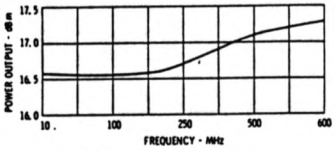
GAIN



NOISE FIGURE

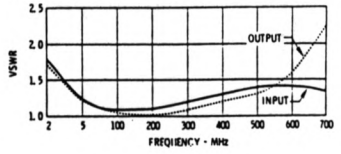


POWER OUTPUT*

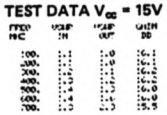


*at 1 dB Gain Compression

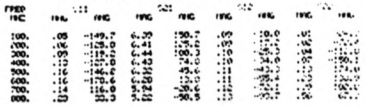
VSWR



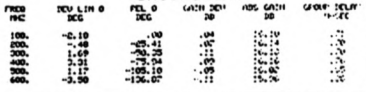
TYPICAL AUTOMATIC TEST DATA V_{DC} = 15V



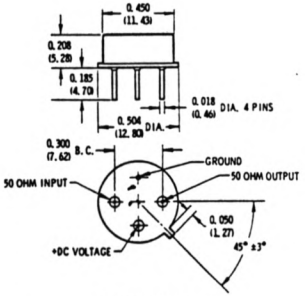
LINEAR S-PARAMETERS



DEVIATION FROM LINEAR PHASE, GAIN AND GROUP DELAY



OUTLINE DRAWING



WEIGHT 2.1 GRAMS
DIMENSIONS ARE IN INCHES (MILLIMETERS)

JUNE 1980

PRINTED IN U.S.A.

INPUT POWER = -11 dBm

A77-1 AMPLIFIER

600 MHz

NOTES:
1. S11 INPUT RETURN LOSS
2. S12 ISOLATION
3. S21 GAIN
4. S22 OUTPUT RETURN LOSS
5. Is SOURCE CURRENT

	S11	S12	S21	S22	Is @ +
S.1	-17	-20	15	-19	50 mA
S.2	-17	-18	17	-15	50mA
S.3	-17	-18	16	-15	48mA
S.4	-18	-18	17	-15	50mA
S5	-13	-18	16	-14	50 mA
S6	-16	-18	17	-13	50mA
S7	-16	-18	17	-14	50mA
S8	-17	-20	15	-15	48mA
S9			17.5		48 mA
S10	-16	-17.5	+16	-16	49 mA
S11	-15	-17	+16	-22	50mA
S12	-14.5	-17	+15	-19	48 mA
S13	-16	-17.5	+15.5	-17	48mA
S14	-15	-17	+16.5	-15.5	48 mA
S15	-13.5	-17.5	+16	-17	48mA
S16	-13.8	-18	+15	-20	46 mA
S17	-15	-17	+16	-16	49 mA
S18	-16.5	-17.5	+16	-15	50mA
S19	-15	-17	+16	-15.5	50mA
S20	-15	-17	+16	-16	50mA
S21	-13.5	-17.5	+16	-19	49mA
S22					
S.23					
S.24					
S.25					
S.26					
S.27					
S.28					
S.29					
S.30					

RF HYBRID AMPLIFIER ASSEMBLY
AY 5029-X

AYDIN VECTOR *DIVISION*

-4
367[00]

- Guaranteed Specifications
- Quality Product
- Wide Bandwidth 5 - 250 MHz
- Gain 65 dB
- 1 dB Gain Compression +12 dBm.
- Temperature Stability -55°C to 100°C
- Choice Of Connector

GENERAL DESCRIPTION:
The AY series of amplifier assemblies consists of multiple modular amplifiers. The hermetically sealed TO-8 packages and DIP are directly inserted into a microstrip circuit board which is enclosed in the aluminum housing. A choice of connector is available.

QUALITY ASSURANCE:
The Quality system is approved to MIL-Q-9858A. Units are designed to meet environmental requirements of MIL-STD-883B.

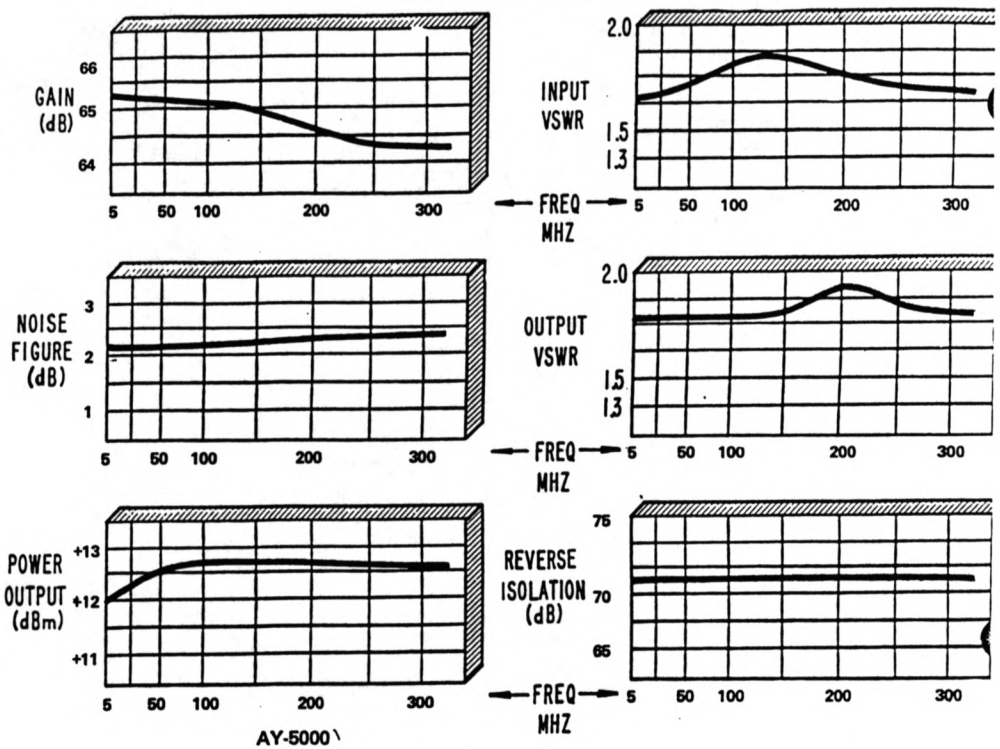
APPLICATIONS:
RF Preamplifiers, IF Gain Building Blocks, Isolation Amplifier, LO Buffer Amplifiers.
Used in Phased Arrays, ECM Receivers, Satellite Communications IF's, Direction Finding Systems, Instrumentation, Radar Receivers, Transceivers.

ENVIRONMENTAL:
All standard products are screened to MIL-STD-883B, Class B with the exception of burn-in. Tests such as, Temperature Cycling, Acceleration, Hermeticity Centrifuge and Fine/Gross Leak. Burn-in (168 hrs.) will be performed upon request.

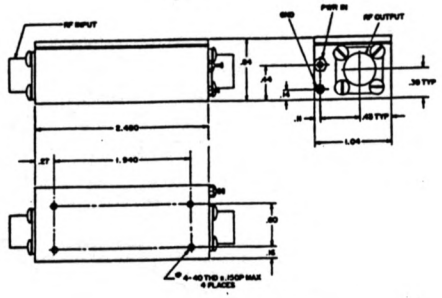
GUARANTEED:	5 MHz to 250 MHz							
ELECTRICAL SPECIFICATIONS	GAIN dB	FLATNESS ±dB	NOISE FIGURE (dB)	IMP_3 dBm	POWER OUTPUT dBm	INPUT/ OUTPUT VSWR	REVERSE ISOLATION (dB)	VDC / IM
Maximum						2.1 / 2.0		
Typical	65	±1	2.2	+31	+12	1.7 / 1.7	70	+15 / 130mA
Minimum								

AYDIN VECTOR division / P.O. Box 328, Newtown, PA 18940
Main Offices & Plant: Newtown Industrial Commons, Newtown, PA

TYPICAL TEST DATA



AY-5000



Assemblies available with BNC, TNC, N or SMA connectors.

TNC Connectors	AY5029	-1
BNC Connectors		-2
N Connectors		-3
SMA Connectors		-4

NOTE: ALL DIMENSIONS IN INCHES.

Bulletin No.: 16005029/6-82-1M/Printed in USA.

Data Acquisition and Reduction Systems and Components

AYDIN VECTOR division
Friends Lane, P.O. Box 328
Newtown, Pa. 18940
Phone: (215) 968-4271
TWX: 510-667-2320

Ruggedized Airborne Components & Systems
Transmitters....Commutators....PCM Encoders
Subcarrier Oscillators....Telemetry Systems

AYDIN MONITOR systems
401 Commerce Drive
Fort Washington, Pa. 19034
Phone: (215) 646-8100
TWX: 510-661-1520

Ground Based Components & Systems
PAM/PDM/PCM Simulators & Synchronizers
PCM Decommutators...Computer Interface

AYDIN VECTOR division

TEST DATA

Unit Nomenclature: RF Amplifier Date: 8-29-84

Unit Part Number: AV-5037-4 Serial No.: 190

Description of Test: Final Tested By: 2156

Project Number: 8888 ATP No.: 65000855

Temp. +25°C

Paragraph	Parameter	Limits	Reading	500 Mhz Frequency MHz	High Gain	Low Gain	MHz
6.2	Gain	62 To 70 db	67.9db				
	Flatness	N/A	N/A				
6.5	Power Out	+9 dBm Min.	+10.6dbm	@ 200 Mhz			
6.6	IMP-3	N/A dBm Min.	—	MHz			
6.4	N.F.	5.0 dB Max.	4.5db	200 @	MHz Worst Case		
6.1	Dc Power @ +~~15~~ 12 Vdc	120mA ~~Max.~~ Typ	127.3mA				
	VSWR IN	1.3-1.6	1.17	to	MHz Worse Case		
6.3	VSWR OUT	1.3-1.6	1.60	to	MHz Worse Case		
7.0	Reverse Iso	N/A dB Min.	—	to	MHz Worse Case		

Remarks: GSI

Q.A.

Form No. 110-E-173

Model Number AY-5037
P/N 160005037-504

TEST DATA
RF HYBRIDS
Lot Number A1

Job Number 20864
Tested By [illegible]
Date 4/15/87

PROCEDURE PARAGRAPH NUMBER	PARAMETER DESCRIPTION	LIMITS	UNITS	QTY IN	QTY OUT
1.0	Small Signal Gain (typ)	65	dB	2	—
2.0	Gain Flatness (max)	±1.5	dB	2	—
3.0	Total Current @ +15Vdc (typ)	165	mA	2	—
4.0	VSWR in/out (max)	2.0:1	—	2	—
5.0	Noise Figure (max)	6.0	dB	2	—
6.0	Power Output @ 1dB Comp. (min.)	10	dBm	2	—

Note: Quantity of the units passed the final testing is shown in "QTY IN" column.

AY 5037 AR 16 MT

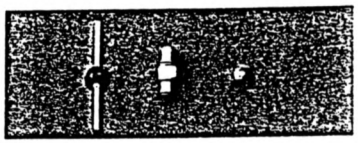
AYDIN VECTOR DIVISION | CODE 13927 | Size A | DRAWING NO.: | Revision | Sheet Of

Harmonic Mixer

A2S124 Mixer Diode, TRW-Aertech

Schottky High Barrier Mixer Diodes

Series A2S100



Features

- Lowest Available Noise Figure
- Low Intermod Distortion
- High Peak Power Handling Capability
- High Reliability (Space Qualifiable)

Description

The TRW Microwave A2S100 series of diodes employs a relatively high barrier metal/silicon Schottky junction. This produces diodes which have very low noise figures and are capable of operation over a broad range of local oscillator power. Hi-Rel versions are available upon request.

Environmental Ratings (Maximum)

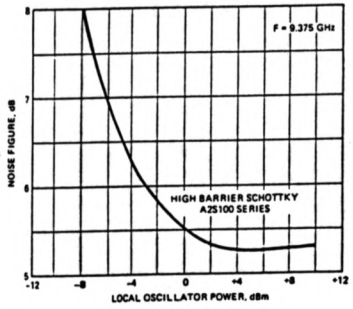
Operating Temperature . . . . . -65°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Power Dissipation @ 25°C. . . . . 200 mW. Derate linearly to zero at 150°C
Soldering Temperature . . . . . 230°C for 5 seconds

Electrical Specifications @ 25°C — High Turn-on (V_F = 530 mV Typ. @ 1mA)

Part[3] Number	Test[4] Frequency (GHz)	Case Style[1]	Noise Figure[2] Typ (dB)	Noise Figure[2] Max (dB)	Max[2] VSWR	Z_{IF}[2] (Ohms)	Typical Parameters[4] C_{jo} (pF)	Typical Parameters[4] V_{BR} (Volts)
A2S101	9.375	P	5.6	6.0	1.5	200-400	0.12	3.0
A2S103	9.375	P	6.5	7.0	2.0	200-400	0.12	3.0
A2S106	9.375	L	5.6	6.0	1.5	200-400	0.12	3.0
A2S108	9.375	L	6.5	7.0	2.0	200-400	0.12	3.0
A2S121	16.0	P	6.0	6.5	1.5	175-350	0.10	2.0
A2S124	16.0	P	6.5	7.0	2.0	175-350	0.10	2.0
A2S122	16.0	L	6.0	6.5	1.5	175-350	0.10	2.0
A2S123	16.0	L	6.5	7.0	2.0	175-350	0.10	2.0
A2S120	9.375	U4	6.0	–	1.5 (typ)	300 (typ)	0.12	3.0
A2S029	9.375	N6	6.0	–	1.5 (typ)	300 (typ)	0.12	3.0
A2S130	3.0	H	5.5	–	1.5 (typ)	300 (typ)	0.40	5.0

Notes:
1. Heat sink is the cathode.
2. Single sideband overall noise figure, resistive image termination:
   P_{LO} = 1 mW
   N_{IF} = 1.5 dB @ 30 MHz
   R_L < 10 ohms
3. Single diodes are available as matched pairs or quads.
   Suffix "M" denotes a pair; "Q" denotes a quad.
   ΔNF_o < 0.3 dB
   ΔZ_{IF} < 25 ohms
4. C_{jo} - Junction capacitance @ V_R = 0 volt.
   V_{BR} - Measured at I_R = 10 μA.
5. Available tested at 2 or 3 GHz.

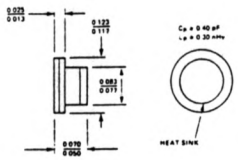
Typical Performance Data @ 25°C



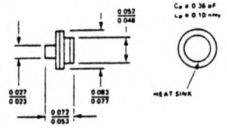
TRW Microwave

Diode Outline Dimensions

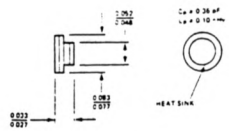
CASE STYLE "A"



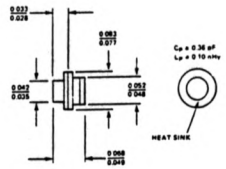
CASE STYLE "C"



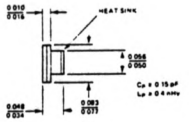
CASE STYLE "D"



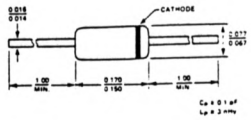
CASE STYLE "E"



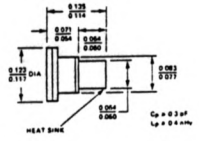
CASE STYLE "G"



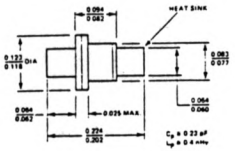
CASE STYLE "H"
(Glass axial lead—similar to DO34)



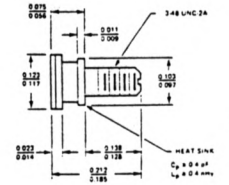
CASE STYLE "I"



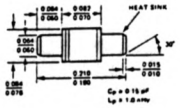
CASE STYLE "J"



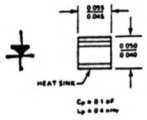
CASE STYLE "K"



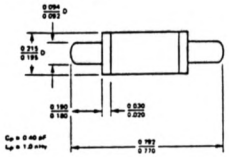
CASE STYLE "L"



CASE STYLE "P"



CASE STYLE "S2"



Note: Packages are not necessarily drawn to the same scale.

6.0 APPENDIX

List of Relevant NRAO Technical Reports and Data

NRAO Technical Reports

VLA Technical Report No. 29, An Introduction to the VLA Electronic System A. R. Thompson 3/77
VLA Technical Report No. 8, Module L6 The 2-4 GHz Synthesizer A. R. Thompson February 1976
VLA Technical Report No. 7, Module F4 Frequency Converter, S. Weinreb July 1975
VLBA Technical Report No. 4, 2 - 16 GHz Synthesizer, L104 Robert I. Mauzy June 11, 1987

VLA System Drawings

D16000B03	VLA System RF Block Diagram

X-Band System Drawings

A13050P20	Bin/Module OSP Connector Interface
C13165B02	8 - 10 GHz Receiver Block Diagram
B13030M21	F-Rack to B-Rack Cables
B13030M17	Connector/Pin Mod. UG-603A/U
B13030M58	B-Rack Connector Bracket
B13050M56	B Rack Support Bracket
C13030M30	F-Rack to B-Rack Cable Support
C13030P11	Cable Support Assembly
C13600M01	D-Rack Filter Bracket
C13165B02	8 - 10 GHz Receiver