OTA-Free 1-1 MASH ADC Using Fully Passive Noise-Shaping SAR & VCO ADC

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Abstract—We present an OTA-free 1-1 multi-stage noise-shaping (MASH) analog-to-digital converter (ADC) utilizing a fully passive noise-shaping successive approximation register (NS-SAR) as the first stage and an open-loop ring voltage-controlled oscillator (VCO) as the second stage. The key contribution of this work is to address the challenge of driving large sampling capacitors for high-resolution NS-SAR. The proposed architecture allows a low-resolution NS-SAR stage and leverages residue attenuation due to passive charge sharing in the NS-SAR to linearize the VCO. The MASH architecture suppresses quantization noise and SAR comparator noise at the ADC output, and the high pass shapes VCO thermal noise. In addition, we demonstrate a computationally inexpensive foreground inter-stage gain calibration algorithm for the proposed ADC architecture. The prototype ADC consumes 0.16 mW while achieving an SNDR/DR of 71.5/75.8 dB over a 1.1-MHz bandwidth and Walden FoM of 23.3 fJ/step, which is the lowest in 65-nm technology.

Index Terms—Multi-stage noise-shaping (MASH), noise-shaping successive approximation register, oversampling analog-to-digital converter (ADC), passive integrator, ring voltage-controlled oscillator (VCO).

I. Introduction

NOISE-SHAPING successive approximation register (NS-SAR) [1]–[11] is a hybrid oversampling analog-to-digital converter (ADC) architecture that combines the advantages of both SAR and $\Delta\Sigma$ ADCs. SAR ADC is very energy efficient at medium resolution, but energy efficiency of high-resolution SAR ADC is limited by thermal noise. While recent works have introduced correlated double sampling in SAR ADC to break the limit set by kT/C sampling noise [12], [13], comparator thermal noise is still a limiting factor. On the other hand, $\Delta\Sigma$ ADC can achieve high resolution by reducing kT/C noise through oversampling and comparator thermal noise through noise-shaping. However, designing high-resolution $\Delta\Sigma$ ADC with high-gain OTA is challenging in advanced CMOS processes.

NS-SAR combines the merits of SAR and $\Delta\Sigma$ architecture by embedding a filter inside the SAR loop that integrates the residue from prior conversion. Thus, the NS-SAR essentially implements a feedforward $\Delta\Sigma$ with SAR quantizer. Three different loop filter architectures have been demonstrated so far: 1) closed-loop active integrator [1]; 2) passive integrator [2], [11]; and 3) open-loop amplifier followed by passive integrator [7], [8]. Closed-loop active integrator architecture can provide large gain and strong in-band noise suppression. However, the loop filter requires high-gain amplifiers, which limits energy efficiency. In contrast, passive integrators use only switches and capacitors, and are scaling friendly. However, passive integrators attenuate the signal during integration, which results in inadequate in-band noise suppression performance. In addition, a multiple-input comparator is used to provide relative gain between integration and input-feedforward paths, which is noisier than a single input comparator. Open-loop amplification followed by passive integration offers a good tradeoff between active and passive integrator architectures, but open-loop amplifiers can make the NS-SAR loop unstable due to large variations in open-loop gain and require calibration, which increases design complexity [9]. A recent work [14] presents a high-resolution NS-SAR that uses a closed-loop dynamic amplifier for residue integration. The dynamic amplifier consumes less power than OTA, and the closed-loop implementation ensures robustness against PVT variations. Despite the recent advancements in NS-SAR architectures, state-of-the-art NS-SAR ADCs require 9–11-bit DAC to achieve >12-bit resolution, which brings the additional challenge of driving large sampling capacitors. As an example, the NS-SAR in [14] uses 10-bit DAC with one additional bit for redundancy and a 2-pF single-ended DAC capacitor.

In this work, we try to address the challenges posed by passive integrator-based NS-SAR architectures, as well as driving requirements by adopting a multi-stage noise-shaping (MASH) architecture in which the first stage is an NS-SAR and the second stage is a ring voltage-controlled oscillator (VCO). The VCO stage is driven by the output of the passive integrator in the NS-SAR stage. Since the MASH architecture suppresses quantization error and comparator noise from the SAR stage, the weak in-band noise suppression of passive NS-SAR is readily addressed. Signal attenuation by the passive integrator in NS-SAR proves advantageous to the proposed architecture since the small-signal swing linearizes the VCO. The VCO performs inherent amplification during

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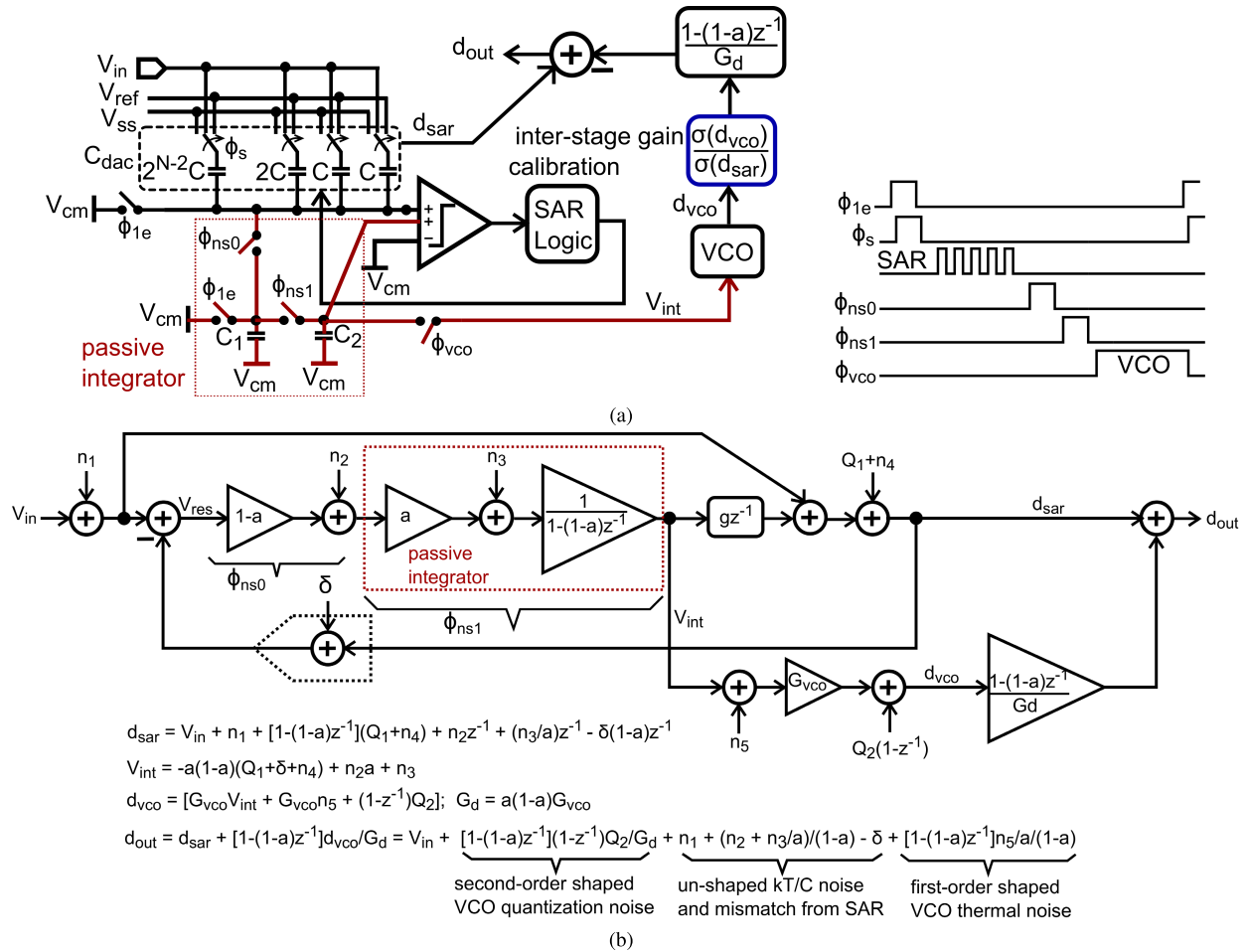
Fig. 1. (a) Circuit diagram of the proposed NS-SAR + VCO ADC. (b) Simplified mathematical model.

phase-domain integration by integrating its input over time and does not require an explicit amplifier as in conventional MASH architecture. While a multi-input comparator in the NS-SAR stage increases noise, comparator noise is suppressed in the overall ADC output and is not a limiting factor. The overall architecture does not use any operational amplifier and is highly digital and scaling friendly. Due to MASH architecture, the NS-SAR stage can be low resolution, and the total input capacitor that needs to be driven is also small. A recent work [15] uses a similar MASH architecture and cascades two NS-SAR ADCs. However, an active amplifier is still needed to amplify residue of the first stage, unlike the proposed work in which no active amplifier is used. To address inter-stage gain mismatch, a simple foreground calibration technique is proposed, which extracts the inter-stage gain through ratios of standard deviations of digital outputs from the two stages in the absence of input signal. The proposed calibration technique does not inject any additional signal to the VCO stage for calibration, such as pseudorandom sequence in [16], which improves the dynamic range of the VCO and ADC energy efficiency.

The rest of this article is organized as follows. Section II presents the proposed architecture and detailed discussion on design optimization. Section III presents measurement

results on test chips fabricated in the 65-nm CMOS process. Section IV brings up the conclusion.

II. NS-SAR + VCO ADC DESIGN

A. Architecture

Fig. 1(a) shows the proposed NS-SAR + VCO ADC with a timing diagram. A single-ended architecture is shown for sake of simplicity even though the circuit realization uses differential architecture. A 5-bit passive noise-shaping SAR is used as first stage, and a VCO is used as second stage. The input signal is sampled during ϕ_s phase, and the SAR performs normal conversion over the next five cycles. During ϕ_{ns0}, the SAR residue is passively shared with a capacitor C_1, where $C_1 = ac_{dac}/(1 - a)$ and C_{dac} is the capacitance of SAR DAC. The charge on C_1 is dumped across another capacitor $C_2 = C_{dac}$ during the next cycle, ϕ_{ns1}, thus effectively realizing passive integration. The capacitor C_1 is discharged at the start of every SAR conversion. The voltage integrated on C_2 [labeled as V_{int} in Fig. 1(a)] is sent to the SAR comparator input. Thus, the SAR ADC effectively behaves as a feedforward $\Delta\Sigma$ modulator with first-order noise-shaping with a signal transfer function (STF) of 1 and NTF of $[1 - (1 - a)z^{-1}]$.

The passive integrator output, V_{int}, is sent to the VCO for fine, time-domain quantization during the phase ϕ_{vco}.

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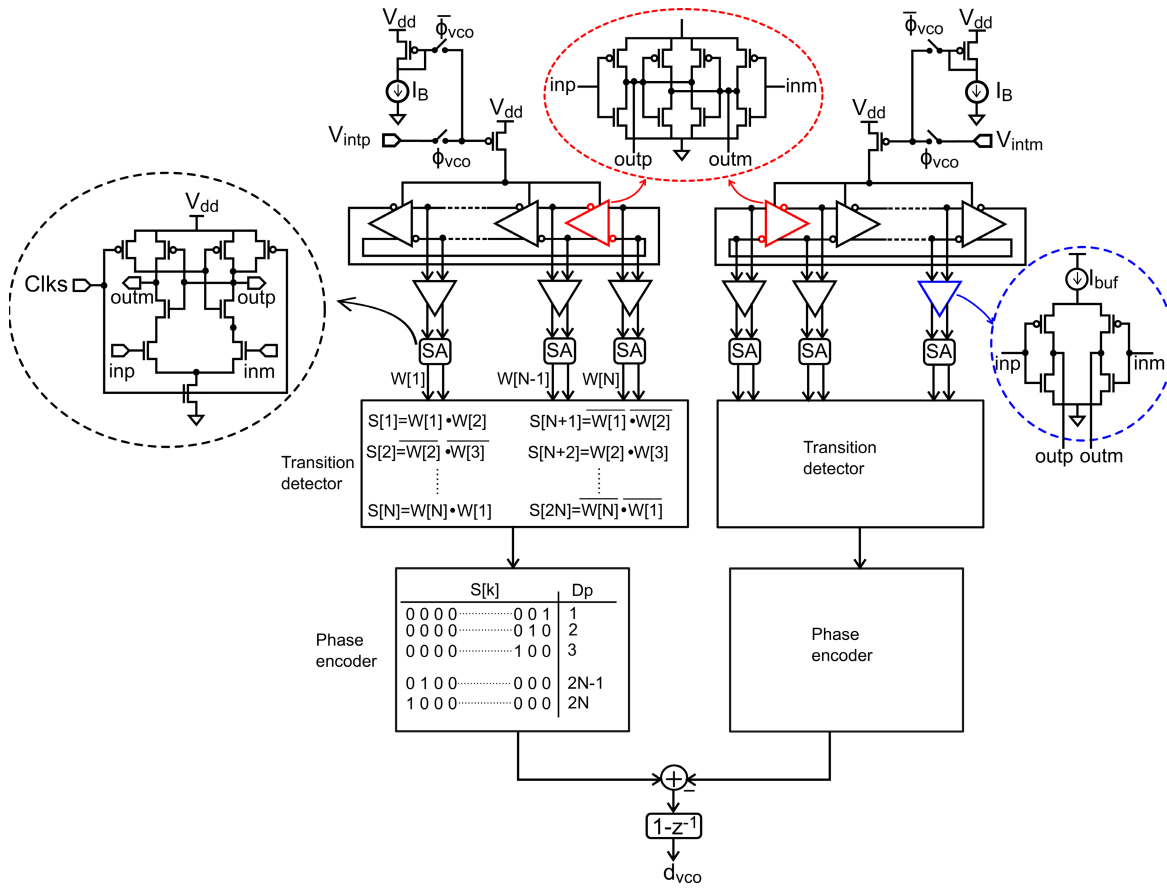

Fig. 2.   Circuit schematic for second-stage VCO.

Passive integration of SAR residue attenuates the signal swing seen by the VCO and linearizes it. The VCO, in turn, absorbs errors in the SAR stage due to comparator thermal noise, which allows a reduction in SAR power. Calibration is performed to suppress inter-stage gain mismatch. The ADC parameter optimizations are discussed in detail in the following.

Fig. 1(b) shows a simplified mathematical model of the proposed NS-SAR + VCO ADC. While the model is not mathematically rigorous since it does not model anti-aliasing in the continuous-time (CT) VCO, it still provides key insights into the architecture. The effect of anti-aliasing in the VCO stage is discussed separately in Section II-B. n_1 is the kT/C sampling noise in the SAR DAC, which directly adds to the input, n_2 is the noise voltage on C_1 at the end of ϕ_{ns0}, n_3 is the noise voltage on C_2 at the end of ϕ_{ns1}, n_4 is the thermal noise from SAR comparator, Q_1 is the quantization noise of the SAR stage, δ is the mismatch in the SAR DAC, n_5 is the input-referred thermal noise of the VCO stage, and Q_2 is the quantization noise of VCO. The comparator in the SAR stage has two paths with the passive integration path having a gain of $g = 1/a$, which is realized in circuit by relative scaling of input transistor sizes. The VCO output is passed through a differentiator before adding with SAR output. As shown in Fig. 1(b), the ADC output has the following components: 1) second-order shaped VCO quantization noise; 2) first-order shaped VCO thermal noise; 3) kT/C sampling

noise and capacitor mismatch from SAR DAC; and 4) kT/C noise components from the passive integrator. Thermal noise from the comparator and quantization noise from the first stage is canceled at the ADC output with the degree of cancellation being limited by the inter-stage gain mismatch.

Fig. 2 shows the circuit schematic for the second-stage VCO. A seven-stage current-starved ring inverter chain is used as the VCO. The choice of the number of inverters in the VCO is explained in Section II-C. PMOS tail current source is used to reduce flicker noise. The VCO phase output is captured by sense amplifiers (SAs) on the positive edges of the sampling clock. Current starved buffers are used to isolate the VCO cells from the SAs to reduce kickback noise. At any given time, only one of the seven inverters in each VCO stage is undergoing transition, rising or falling. Thus, the seven-stage VCO quantizes the phase interval $(0, 2\pi)$ into 14 levels. A rising transition occurs when the positive input of an inverter cell is greater than the switching threshold of the buffer, and the positive output is less than the switching threshold of the buffer. Similarly, a falling transition occurs when the positive input of an inverter cell is less than the switching threshold of the buffer, and the positive output is greater than the switching threshold of the buffer. Since each transition state depends on both rising and falling edges of the inverters, nonuniform quantization of phase is avoided, which would otherwise lead to significant distortion in the

ADC output [17]. The VCO phase is sampled by the SAs, and a transition detector identifies which inverter was transitioning and the type of transition when the phase is sampled. Thus, the transition detector quantizes the sampled phase into 14 levels. The quantized phase is in one-hot form, which is encoded into a digital word and differentiated digitally to form the second-stage output, d_{vco}. During the SAR conversion phase, the differential VCOs are not shut down but rather run with a current I_B. This is done to avoid phase errors due to charge leakage if the VCOs are stopped completely [18]. By running the VCOs from the same current source, the differential phase accumulated by the VCOs is zero during the SAR conversion phase. The value of I_B is kept low to save power and reduce phase noise of the VCOs during their idle phase.

B. Inter-Stage Gain Mismatch

Inter-stage gain mismatch in the proposed architecture comes from the following sources: 1) parasitic capacitors in the passive integration path in the SAR stage, which attenuates signal swing for VCO stage; 2) variations in VCO tuning gain; and 3) re-construction error introduced during the combination of discrete-time (DT) SAR output with CT VCO output. Calibration techniques can be used to correct for inter-stage gain mismatch due to parasitic capacitors in the passive integration path and variations in VCO tuning gain. However, correcting for reconstruction error due to the DT-CT interface is non-trivial, and its effect is illustrated in Fig. 3. Fig. 3(a) shows a simplified signal-flow diagram of the DT-CT interface. The VCO is assumed to be an ideal back-end quantizer with no thermal noise and infinitely many quantization levels and is modeled by a sinc-filter and sampler. The passive integrator output from the SAR stage effectively passes through a mixer before reaching the VCO stage since the VCO only performs quantization after SAR conversion is complete. In Fig. 3(a), $X_n(t)$ denotes the DT output of passive integrator, which consists of noise contributions from the SAR stage, as shown in Fig. 1(b). $X_n(t)$ passes through a passive mixer controlled by a pulse train $p(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(2\pi n f_s t)$, where $a_0 = d$ is the duty cycle of $p(t)$ given by ratio of VCO integration time to sampling period of the ADC, and $a_n = (2/n\pi) \sin(nd\pi/2)$. The passive mixing creates multiple copies of $X_n(f)$ around harmonics of sampling frequency f_s with different scaling factors and spreads out its spectrum. The VCO acts as a CT filter with transfer function given by $H(f) = K_{\text{vco}} e^{-j\pi T_s f} \cdot (\sin(\pi T_s f)/\pi f)$. Thus, the mixer output is sinc-filtered due to inherent anti-aliasing in the CT VCO stage, which attenuates the mixer output in the higher Nyquist bands. The output of the sinc-filter, $X_h(t)$, is sampled to produce VCO output, $X_s(t)$. Even with an ideal VCO quantizer, the reconstructed signal $X_s(t)$ will not be identical to $X_n(t)$ due to anti-aliasing in the VCO, which performs frequency dependent attenuation of the mixer output. The normalized power spectral density (PSD) for each signal is shown in Fig. 3(a). For simplicity, it is assumed that $X_n(f)$ has a uniform PSD. Frequency selectivity of since-filter results in frequency-dependent gain for the sampled VCO output, $X_s(f)$, as shown in Fig. 3(a). Thus, even though input to the
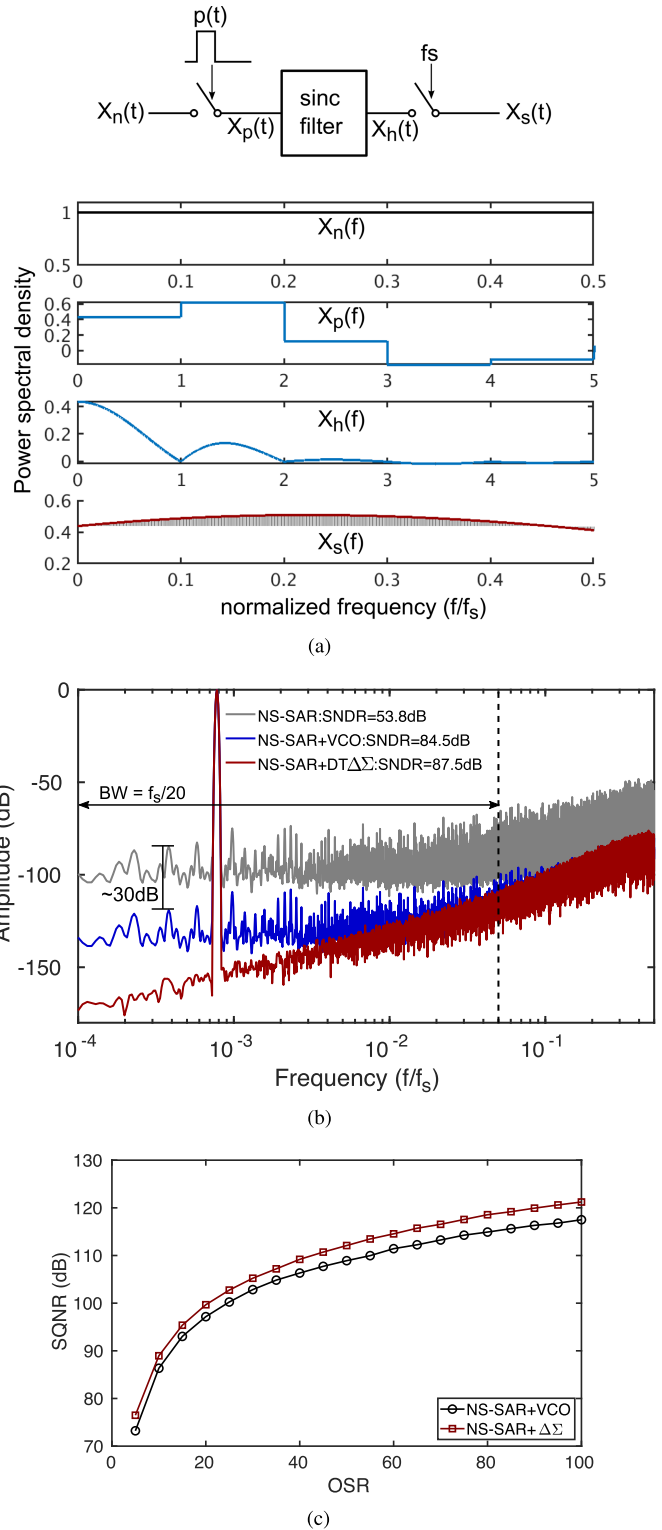

(a)

(b)

(c)

Fig. 3. (a) Illustration of reconstruction error due to CT second stage. (b) 2^{17} point simulated FFT plot showing effect of interstage gain mismatch due to reconstruction error introduced by the VCO stage. (c) Comparison of SQNR with DT $\Delta\Sigma$ second stage as a function of OSR.

VCO stage has a uniform PSD, the sampled VCO output has a frequency-variant PSD, which makes the interstage gain a function of frequency. Thus, it is not trivial to match interstage gain at all frequencies in the signal band using time-domain interstage gain extraction.

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Fig. 3(b) shows the effect of interstage gain mismatch due to DT-CT interface through FFT plots from behavioral simulations with an NS-SAR + VCO and an NS-SAR + DT $\Delta\Sigma$ with both the second stages having the same SQNR. Thermal noise is not included in the simulation. The NTF zero for the SAR stage is set to $z = 0.75$, which corresponds to $a = 0.25$. The 5-bit NS-SAR has an SNDR of 53.8 dB at an OSR of 10, while the NS-SAR + VCO and NS-SAR + DT $\Delta\Sigma$ have SNDR of 84.5 and 87.5 dB, respectively. As seen from Fig. 3(b), the NS-SAR + DT $\Delta\Sigma$ significantly suppresses quantization noise from the SAR stage, while the NS-SAR + VCO attenuates in-band noise from the SAR stage by 30 dB. As shown in Fig. 3(c), NS-SAR + DT $\Delta\Sigma$ results in better SNDR than NS-SAR + VCO with increase in OSR. In practice, kT/C noise from the SAR stage sets the in-band noise floor of the overall ADC and limits the advantage of NS-SAR + DT $\Delta\Sigma$ over NS-SAR + VCO in terms of SNDR. In addition, VCO architecture offers a highly digital and scaling-friendly design compared to conventional DT $\Delta\Sigma$ requiring high-gain amplifiers.

C. Design Space Exploration

There are several design parameters to tune for optimizing the energy efficiency of the NS-SAR + VCO ADC: 1) SAR resolution; 2) comparator noise; 3) NTF zero location in the NS-SAR stage; and 4) VCO resolution. The design parameter optimizations are performed assuming a supply voltage of 1.2 V and OSR of 11. VCO thermal noise is not included in the design optimization since: 1) the in-band thermal noise floor is set by kT/C noise from the SAR stage and 2) VCO thermal noise is independent of the number of delay cells in the VCO and can be set to the desired value by tuning transconductance of tail current source [19]. During SAR resolution optimization, the VCO resolution is adjusted such that the overall ADC maintains a 12–13-b resolution. The NTF zero for the NS-SAR stage is set to $z = 0.75$ for the simulations. Resolution of the SAR stage is swept from 3 to 8 b keeping the total DAC capacitance, C_{dac}, constant, and the simulation results are plotted in Fig. 4(a). The Walden FoM increases with the increase in the SAR resolution since the comparator power increases by $4\times$ for every 1-bit increase in SAR resolution. While the SAR comparator noise is suppressed in the overall ADC output and does not affect ADC resolution to the first order, the comparator noise has to be adequately small so as not to over-range the second-stage VCO. At the same time, reducing the comparator noise too much increases ADC power without improving its resolution. As shown in Fig. 4(a), the ADC achieves the best Walden FoM for SAR resolution in the range of 3–5 b. A 5-b SAR resolution is selected for this design to linearize the VCO by reducing its signal swing. Fig. 4(b) shows the simulated ADC Walden FoM versus standard deviation of comparator noise. The ADC resolution drops for large comparator noise, which increases Walden FoM, whereas, for very low comparator noise, the Walden FoM rises again due to an exponential increase in comparator power. For this design, the comparator
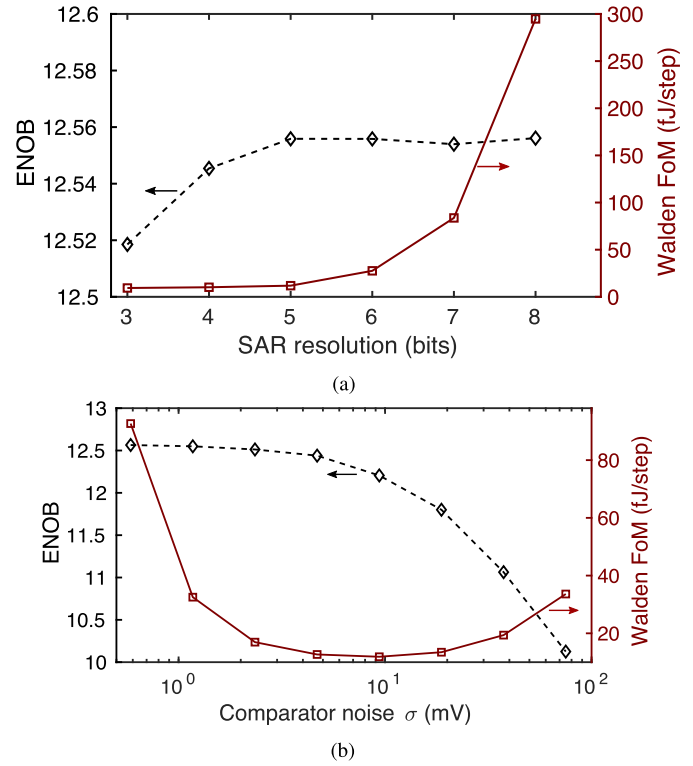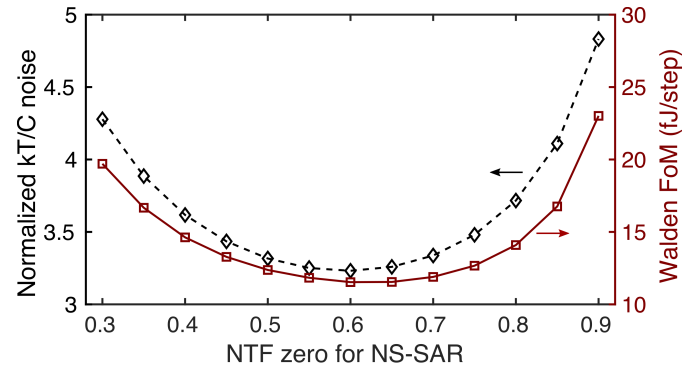

Fig. 4. (a) Simulated ADC ENOB and Walden FoM as a function of SAR resolution. (b) Walden FoM versus comparator noise.

$$\overline{n_1^2} = \frac{kT}{C_{dac}}; \quad \overline{n_2^2} = \frac{(1-a)^2 kT}{a C_{dac}}; \quad \overline{n_3^2} = \frac{akT}{C_{dac}}$$

$$\overline{n_{ADC}^2} = \overline{n_1^2} + \frac{1}{(1-a)^2}\overline{n_2^2} + \frac{\overline{n_3^2}}{a^2(1-a)^2}$$

$$\frac{\overline{n_{ADC}^2}}{kT/C_{dac}} = \left[1 + \frac{1}{a} + \frac{1}{a(1-a)^2}\right]$$

Fig. 5. Simulated kT/C noise in NS-SAR stage and Walden FoM.

noise standard deviation is selected to be $\Delta/8$, where Δ is the LSB size of SAR.

The NTF zero in the NS-SAR stage plays an important role in ADC energy efficiency in two ways: 1) contribution of kT/C noise sampled on C_1 and C_2 at the ADC output changes with SAR NTF zero and 2) VCO input swing changes with SAR NTF zero. Fig. 5 shows simulated kT/C noise in the
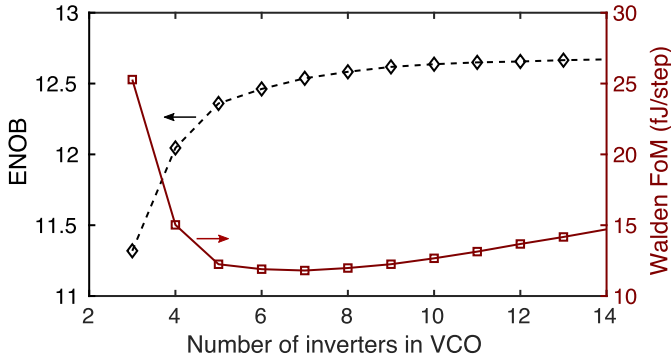
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Fig. 6. Simulated ADC ENOB and Walden FoM as a function of number of inverters in the VCO stage.

Fig. 7. Simulated ADC ENOB versus capacitor standard deviation.

Fig. 8. Simulated SNDR versus integrator path gain.

NS-SAR stage and Walden FoM as a function of NTF zero in the NS-SAR stage. The change in VCO input swing with SAR NTF zero location can be remedied by tuning the VCO gain, and hence, the VCO input swing is kept constant for the simulations. Interested readers are referred to [2] for derivation of kT/C noise equations shown in Fig. 5. The kT/C noise at the ADC output is dominated by noise sampled on C_2 at the end of ϕ_{ns1}, n_3. The kT/C noise increases as the NTF zero is pushed closer to dc or toward $f_s/4$ and has a shallow local minimum between $z = 0.5$ to $z = 0.8$, which results in shallow optimum for Walden FoM in the same range. The NTF zero in the NS-SAR stage is set to $z = 0.75$ in this design.

Fig. 6 shows the result of optimization of the VCO stage. The number of inverters in the VCO stage, N, is swept while keeping VCO tuning gain constant. For low N, the VCO quantization noise limits ADC resolution and Walden FoM, while, for large N, the ADC resolution is limited by in-band kT/C noise from the SAR stage. Thus, at large N, increasing N does not improve ADC resolution while increasing VCO power, which increases Walden FoM. The optimum Walden FoM is achieved for $N = 5$–8. A seven-stage ring VCO is selected for this design for optimizing ADC resolution and Walden FoM.

Capacitance mismatch in the SAR stage is an important non-ideality that can limit ADC resolution. The capacitance matching requirement is made more stringent by the fact that the unit capacitor in the 5-bit DAC needs to be matched with 13-bit accuracy, which is more difficult than matching unit capacitors in a 13-bit DAC with the same accuracy. For a differential B-bit binary DAC, the standard deviation of worst case DNL corresponding to mid-scale transition is given by

$$\sigma_{\text{DNL,mid}} = \sqrt{\frac{2^B - 1}{2}} \sigma_u \cdot \frac{1}{2^B} \tag{1}$$

where σ_u is the standard deviation of unit capacitor [20]. The requirement for capacitor matching is to set $3\sigma_{\text{DNL,mid}}$ to less than 0.5 LSB of the overall ADC resolution. For a 5-bit DAC ($B = 5$) and 13-bit ADC, $\sigma_u < 0.05\%$. Based on foundry mismatch data, 204-fF unit capacitors will be required to achieve $\sigma_u = 0.05\%$. Hence, achieving 13-bit uncalibrated matching with the SAR DAC is challenging and will require a large area and power consumption. Instead of selecting the
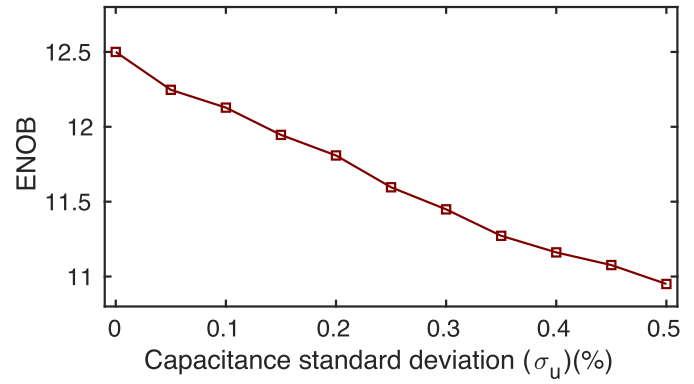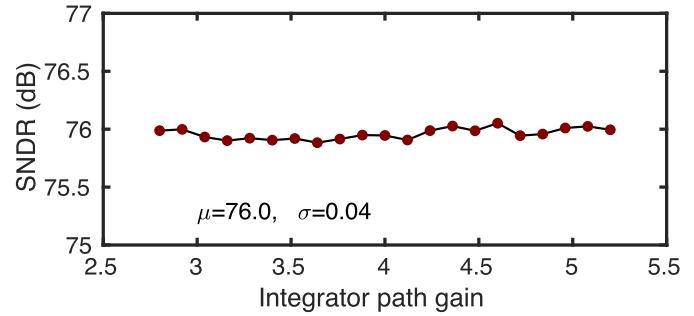
unit capacitor value based on matching requirements, we have selected a unit capacitor value of 18 fF based on in-band thermal noise requirements. An 18-fF unit capacitor results in $\sigma_u = 0.16\%$, which will degrade ADC SNDR at large input amplitudes. Fig. 7 plots ADC ENOB versus σ_u. The ADC SNDR is expected to reduce to 73.2 dB, and the Walden FoM is expected to increase by $1.5\times$ compared to the ideal case with no capacitor mismatch as a result of our choice of a unit capacitor.

The integrator path in the NS-SAR stage has a gain of $g = 1/a$, and deviations in the value of g from $1/a$ add a pole to the NTF in the NS-SAR stage. The integrator path gain is set by relative ratios of the sizes of input transistors in the multi-input comparator and is subject to variations. As shown in [2], $1/(1 - a) < g < (2 - a)/a/(1 - a)$ for the NS-SAR loop to remain stable. For this design, $g = 4$, which is far from the upper and lower boundaries of $28/3$ and $4/3$, respectively, making the design robust to variations in g. Fig. 8 plots simulated SNDR as g is varied by $\pm 30\%$ around 4. The SNDR does not vary significantly showing the ADC robust against variations in integrator path gain in the NS-SAR stage.

D. Inter-Stage Gain Calibration

As discussed earlier, the inter-stage gain is a function of frequency, and it is not trivial to correct for inter-stage gain variation. The proposed inter-stage gain calibration tries to extract the inter-stage gain at low frequencies to sufficiently suppress quantization noise and comparator thermal noise from the SAR stage in the signal band. Fig. 9(a) shows

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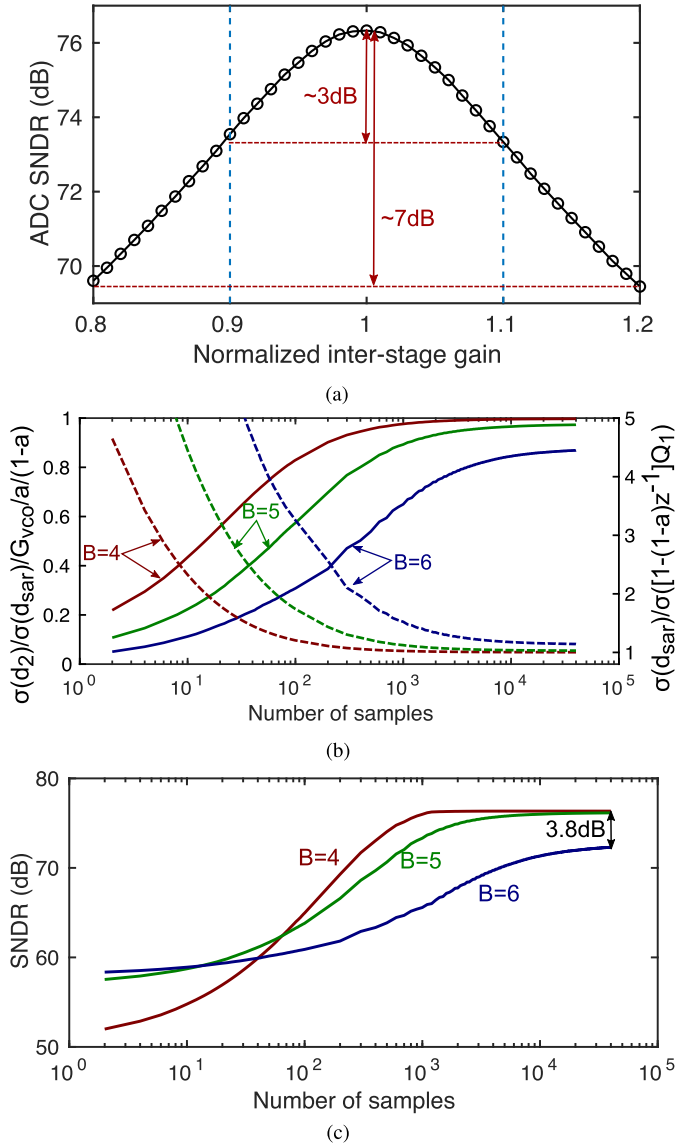
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Fig. 9. (a) Simulated ADC ENOB with variation in inter-stage gain. (b) Normalized inter-stage gain and ratio of standard deviation of d_{sar} and shaped Q_1 versus number of samples for 4-/5-/6-bit SAR. (c) Calibrated SNDR versus number of samples for 4-/5-/6-bit SAR.

the simulated ADC SNDR versus inter-stage gain mismatch. Capacitor mismatch is not considered for this simulation. The SNDR reduces by 3 dB for $\pm 10\%$ variation in interstage gain and 7 dB for $\pm 20\%$ variation in the inter-stage gain.

To extract the inter-stage gain, the input signal is set to "0." The NS-SAR is a feedforward $\Delta\Sigma$, and in the absence of signal, its output oscillates between "1" and "−1" deterministically such that the long-term average is "0." Using $\sigma^2(\cdot)$ as the notation for variance, the variance of SAR output can be written as

$$\sigma^2(d_{sar}) = \sigma^2\big(\{1 - (1-a)z^{-1}\}Q_1\big) + \sigma^2(n_1) + \sigma^2(n_2)$$
$$+ \sigma^2\big(\{1 - (1-a)z^{-1}\}n_4\big) + \sigma^2(n_3)/a^2$$
$$\approx \sigma^2\big(\{1 - (1-a)z^{-1}\}Q_1\big) \quad (2)$$

where the in-band quantization noise power of SAR stage dominates the thermal noise sources. Similarly, variance of

VCO output after passing through $[1 - (1-a)z^{-1}]$ filter, $d_2 = [1 - (1-a)z^{-1}]d_{vco}$, can be written as

$$\sigma^2(d_2) = [G_{vco}a(1-a)]^2\sigma^2\big(\{1-(1-a)z^{-1}\}Q_1\big)$$
$$+ [G_{vco}a(1-a)]^2\sigma^2\big(\{1-(1-a)z^{-1}\}n_4\big)$$
$$+ G_{vco}^2\sigma^2\big(\{1-(1-a)z^{-1}\}n_5\big)$$
$$+ [G_{vco}a]^2\sigma^2\big(\{1-(1-a)z^{-1}\}n_2\big)$$
$$+ G_{vco}^2\sigma^2\big(\{1-(1-a)z^{-1}\}n_3\big)$$
$$+ \sigma^2\big(\{1-(1-a)z^{-1}\}\{1-z^{-1}\}Q_2\big). \quad (3)$$

Variance of quantization noise from the SAR is much higher than thermal noise and VCO quantization noise. Thus, $\sigma^2(d_2)$ can be approximated as

$$\sigma^2(d_2) \approx [G_{vco}a(1-a)]^2\sigma^2\big(\{1-(1-a)z^{-1}\}Q_1\big). \quad (4)$$

The ratio of $\{\sigma^2(d_2)/\sigma^2(d_{sar})\}$ yields the square of inter-stage gain. The proposed inter-stage gain extraction technique is computationally simple and can be implemented by using digital outputs from the two stages. The variance of d_{sar} is calculated from n samples as

$$\sigma^2(d_{sar}) = \frac{1}{n}\sum_{k=1}^{n}(d_{sar}[k] - \mu)^2, \quad \mu = \frac{1}{n}\sum_{k=1}^{n}d_{sar}[k] \quad (5)$$

where μ is the sample mean of d_{sar}. The variance of d_2 is also calculated similarly from n samples. The variance estimation above is biased since the sample mean is not the same as the actual mean. The bias rolls off with n, i.e., the variance estimates converge to their correct values as more samples are considered [21]. This results in finite convergence time for the proposed calibration technique. A key factor in accuracy of the proposed inter-stage calibration technique is the relative ratio between variance of Q_1 and other noise terms. Since the SAR stage has relatively low resolution compared to the overall ADC resolution, Q_1 is the dominant term in (2) and (3), which allows accurate estimation of the inter-stage gain. Fig. 9(b) and (c) illustrates this graphically. The SAR stage resolution, B, is swept from 4 to 6 bit while keeping the ADC resolution unchanged at 13 bit. Fig. 9(b) shows the extracted normalized inter-stage gain and ratio between standard deviation of d_{sar} to $\{1 - (1-a)z^{-1}\}Q_1$ as a function of number of samples. The normalized inter-stage gain converges quickly for 4-bit SAR and asymptotically for 5-bit SAR to within 3% of the correct value. However, for 6-bit SAR, the normalized inter-stage gain has 13% error and longer convergence time. This is also seen in Fig. 9(c) in which the calibrated SNDR is 3.8 dB lower for 6-bit SAR case than that of 4-/5-bit SAR.

The key to this inter-stage gain extraction technique is that the input signal amplitude has to be much smaller than SAR quantization noise. Fig. 10 plots the ENOB of the ADC after calibration and the extracted inter-stage gain normalized by the actual inter-stage gain as a function of the input amplitude. At low signal amplitudes, the ENOB remains close to 12.5-bit after calibration, and the extracted inter-stage gain is close to the ideal value. At input amplitudes above −40 dB, the extracted inter-stage gain starts to deviate from the ideal value significantly, and the ADC ENOB drops.
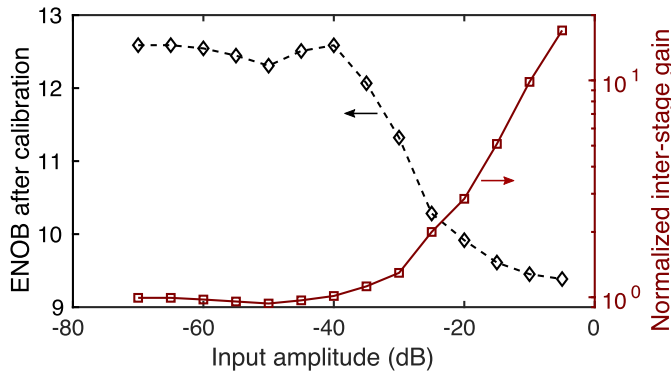
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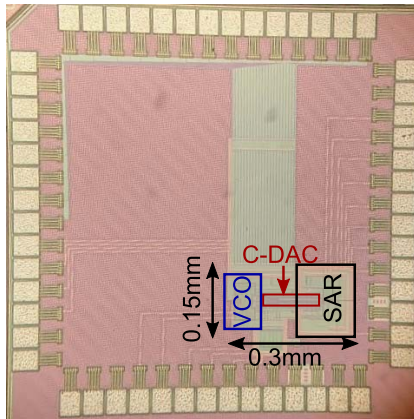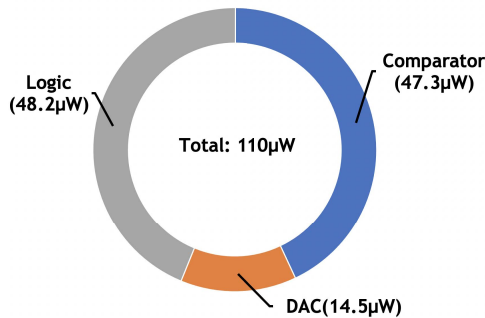Fig. 10.   Simulated ADC ENOB and extracted normalized inter-stage gain versus input amplitude.

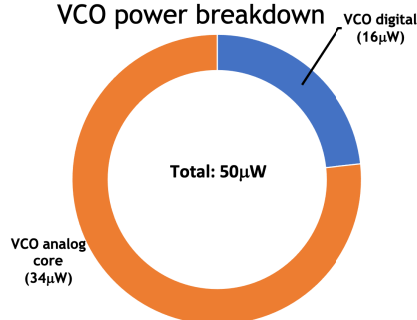Fig. 11.   Die micro-photograph.

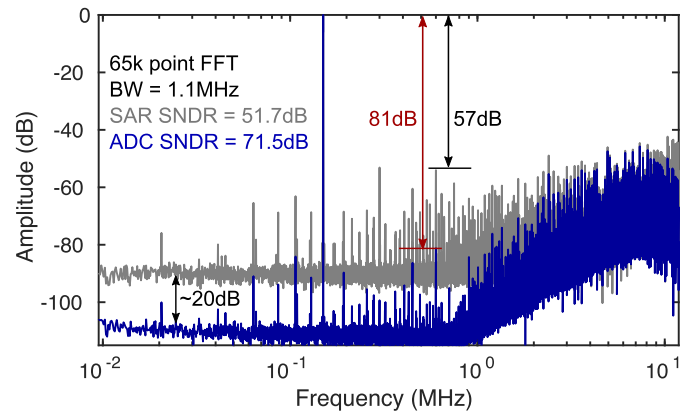Fig. 12.   Breakdown of power consumption in SAR and VCO stages.

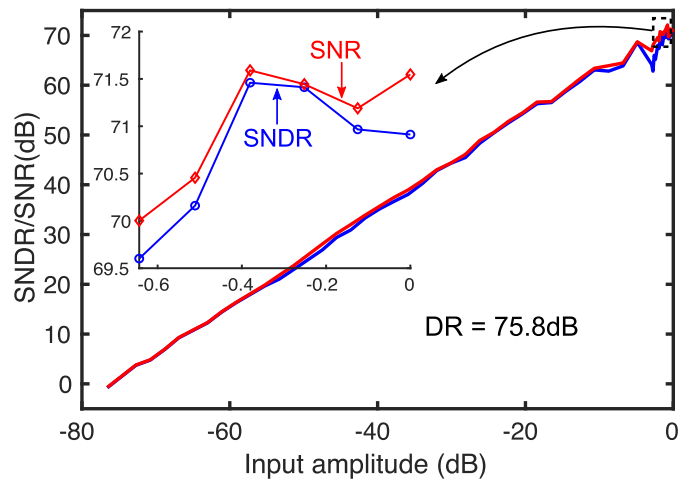Fig. 13.   Measured FFT of NS-SAR and overall ADC.

Fig. 14.   Measured ADC dynamic range.

on calibration as necessary. Another option for on-chip voltage and temperature monitoring is to measure the free-running frequency of the ring oscillator in the second stage. This can be realized by using the output of the delay cell from each VCO to run counters with sufficient depth. The moving average of the two counter outputs is the VCO free-running frequency, and variations in the average value are an indicator of changes in operating conditions, which can trigger the inter-stage gain calibration.

III. MEASUREMENT RESULTS

The proposed ADC is fabricated in the 65-nm CMOS process, and the die photograph is shown in Fig. 11. The ADC has a core area of 0.045 mm^2 and consumes 160 μW from 1.1-V supply at the 24-MHz sampling frequency. Out of 160-μW power, the NS-SAR stage consumes 110-μW power, and the VCO consumes 50-μW power. Fig. 12 shows the breakdown of power consumption in SAR and VCO stages.

Fig. 13 shows the measured 65k point FFT of the NS-SAR and overall ADC. The NS-SAR stage has an SNDR of 51.7 dB and SFDR of 57 dB at an OSR of 11. After the combination of output from the VCO stage, the ADC SNDR improves to 71.5 dB, and SFDR improves to 81 dB. The quantization noise tones in the NS-SAR output are suppressed by more than 20 B

While the proposed calibration technique is foreground in nature, it can be combined with digital on-chip monitors [22] that can continuously check voltage and temperature and turn

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TABLE I
COMPARISON WITH STATE-OF-THE-ART OVERSAMPLING ADCS

	This	**[15]**	**[3]**	**[23]**	**[24]**	**[11]**	**[25]**	**[26]**	**[27]**	**[28]**
	work	**CICC'20**	**CICC'19**	**VLSI'19**	**JSSC'20**	**JSSC'19**	**CICC'19**	**ASSCC'18**	**VLSI'18**	**JSSC'19**
Architecture	NS-SAR	NS-SAR	NS-SAR	SAR	NS-SAR	NS-SAR	CTDSM	NS-SAR	NS-SAR	CTDSM
	VCO (1-1)	pipelined	pipelined	pipelined			+NS-SAR		pipelined	+NS-SAR
Process(nm)	65	65	65	40	28	40	65	28	65	40
Input cap(pF)	0.55	-	0.8	1	7.65	4.2	-	-	-	-
Area(mm^2)	0.04	0.11	0.08	0.06	0.02	0.04	0.22	0.06	0.01	0.03
OTA?	No	Yes	No	Yes	Yes	No	Yes	No	Yes	Yes
Fs(MHz)	24	83.3	80	100	2	8.4	600	0.32	200	500
BW(MHz)	1.1	6	2	12.5	0.1	0.26	12	0.1	12.5	12.5
SNDR(dB)	71.5	73.7	73.8	75.8	87.6	78.4	80	69.3	77.1	70.4
Power(mW)	0.16	3.5	0.87	1.5	0.12	0.14	16.5	0.12	4.5	1.2
FoM$_w$(fJ/step)[1]	23.3	71.7	52.8	11.5	29.6	38.5	84	245	30	17
FoM$_s$(dB)[2]	169.9	166	167.4	175	176.8	171	168.6	158.5	171.5	170.7

[1] FoM$_w$ = Power/2^{ENOB}/2/BW
[2] FoM$_s$ = SNDR + $10\log_{10}$(BW/Power)
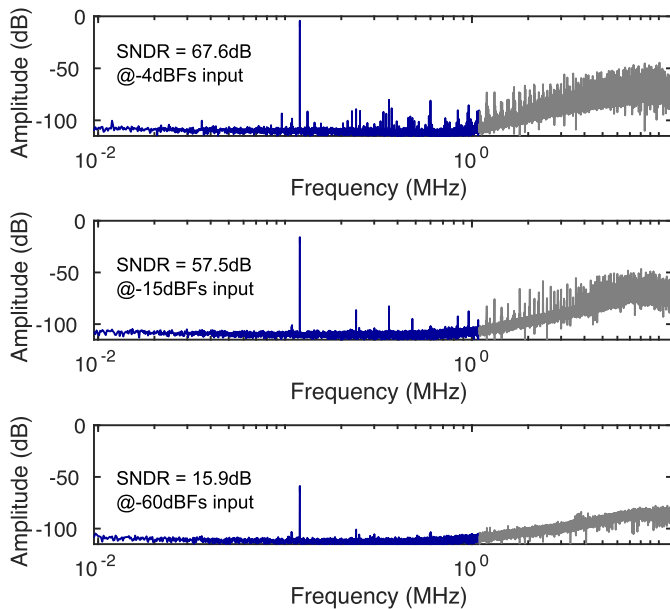
Fig. 15. 65k point FFT of ADC for different input amplitudes.

Fig. 16. Schreier and Walden FoMs versus OSR.
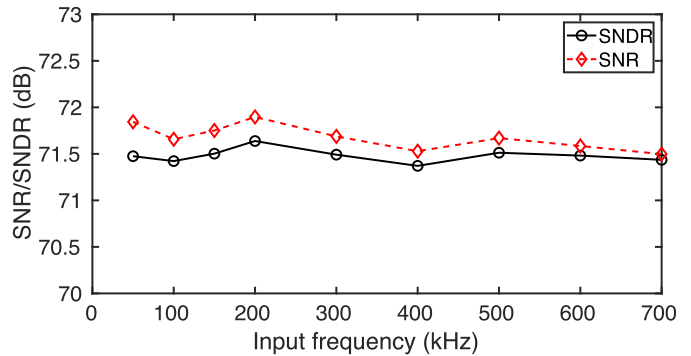
Fig. 17. Measured SNR and SNDR versus input frequency.

by the VCO stage. The tones in the ADC output are due to imperfect inter-stage gain matching arising out of the DT-CT interface and capacitor mismatch in the SAR DAC. Fig. 14 shows the measured SNR/SNDR as a function of the input amplitude. The ADC has a dynamic range of 75.8 dB, and the upper limit on SNR/SNDR is due to capacitor mismatch. Capacitor mismatch is not calibrated in this work. Fig. 15 shows the measured FFT for the ADC at input amplitudes of -4, -15, and -60 dBFs.

Fig. 16 shows the measured Schreier and Walden FoMs as a function of OSR. The best Walden FoM of 23.3 fJ/step is achieved at an OSR of 11. At small OSR values, the ADC SNDR is limited by second-order quantization noise from the
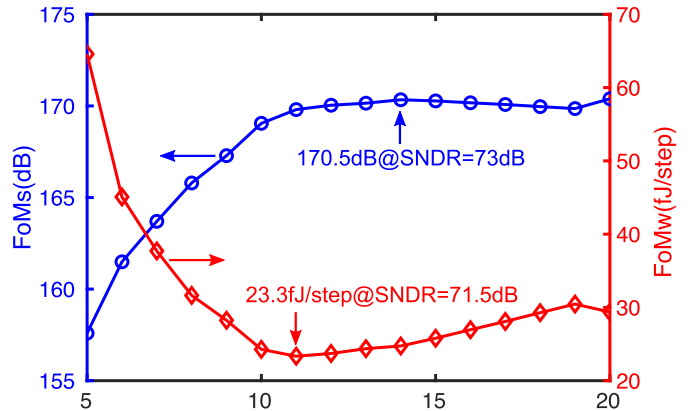
VCO stage, while the ADC SNDR is limited by kT/C noise from the SAR stage at large OSR values. The Schreier FoM is limited by quantization noise from the VCO stage at small OSR values and flattens out for large OSR values in the kT/C noise limited regime. Fig. 17 shows the measured SNR and SNDR as a function of the input frequency.

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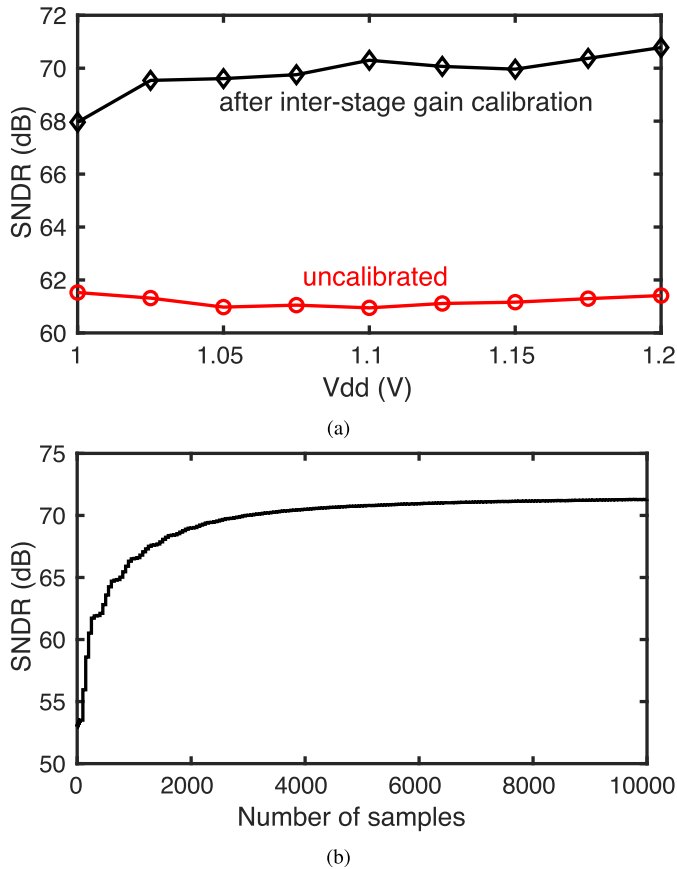

(a)

(b)

Fig. 18.   (a) SNDR with supply variation with and without inter-stage gain calibration. (b) Convergence speed of inter-stage gain calibration.
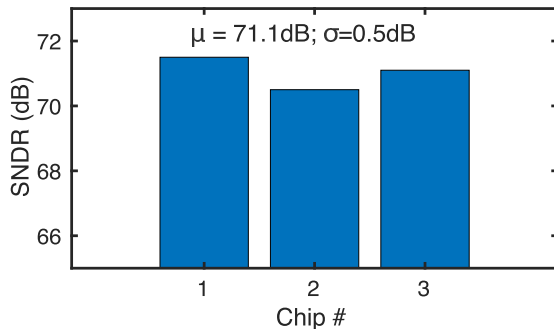

Fig. 19.   SNDR variation for different chips.

Fig. 18(a) shows the measured results as the supply voltage is varied by ±10%. Without the proposed inter-stage gain calibration, the ADC SNDR is around 62 dB. Inter-stage gain calibration improves the SNDR by 6–9 dB over the supply voltage range. The inter-stage gain extraction is performed without applying any input signal. Fig. 18(b) shows the convergence speed of the inter-stage gain calibration technique. The gain calibration requires 5000 samples (or 0.21 ms) for convergence.

Fig. 19 shows the measured SNDR for three test chips with a mean SNDR of 71.1 dB and a standard deviation of 0.5 dB. Table I compares this work with state-of-the-art oversampling ADCs across technology. The proposed ADC
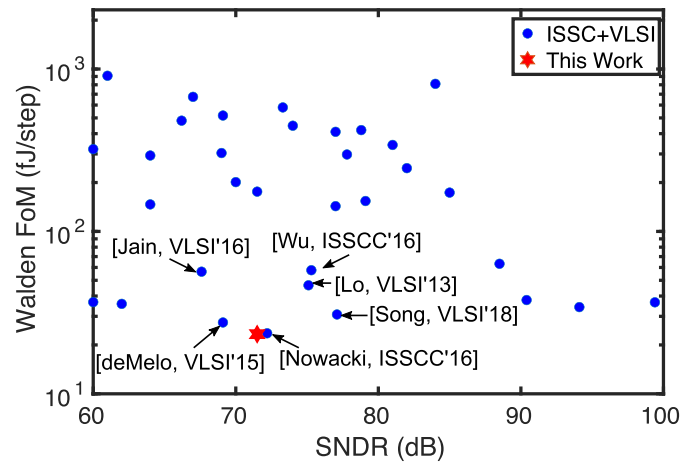

Fig. 20.   Comparison with state-of-the-art oversampling ADCs in 65 nm.

achieves competitive Walden and Schreier FoMs compared to state of the art. Since the proposed ADC is highly digital, its energy efficiency is expected to improve further with technology scaling. The input capacitance of the NS-SAR stage in the proposed ADC is less than the input capacitance of state-of-the-art works. Fig. 20 graphically compares the proposed work with state-of-the-art oversampling ADCs in 65 nm. The proposed ADC achieves the lowest Walden FoM among oversampling ADCs in the 65-nm process.

IV. Conclusion

This work has presented a 1-1 MASH ADC with passive noise-shaping SAR as the first stage and a ring VCO as the second stage. The proposed architecture addresses the challenge of driving large input capacitors for high-resolution NS-SAR ADCs. The second-stage VCO addresses the limitations of passive NS-SAR: 1) signal attenuation and 2) increased comparator noise by leveraging signal attenuation to linearize the VCO stage and suppressing comparator noise at the overall ADC output. The proposed architecture is highly digital and scaling friendly, and will benefit from technology scaling.

Appendix

To theoretically analyze the effect of frequency dependence of inter-stage gain in the proposed ADC, let us compare the SQNR of the proposed architecture with that of a NS-SAR+ DT $\Delta\Sigma$ ADC with the same quantization levels in DT $\Delta\Sigma$ as in the VCO stage. Thermal noise is not considered in this calculation, and the output of the SAR stage going into the second stage is given by $V_{\text{int}} = -a(1 - a)Q_1$. Referring to Fig. 3, the frequency response of $X_p(f)$ at $f = f_o$ can be written as

$$X_p(f_o) = A\left\{a_o\delta(f - f_o) + \sum_{n=1} a_n\delta(f - nf_s \pm f_o)\right\} \quad (6)$$

where A is the amplitude of $X_n(t)$ and PSD of $X_n(t)$ is given by $\text{PSD}_{Q1} = \{a(1 - a)\}^2 \cdot (\Delta^2/12) \cdot (2/f_s)$ with Δ being

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quantization step size of the SAR stage. After X_p is quantized by the VCO stage, the sampled output can be written as

$$X_s(f_o) = A \left\{ a_o H(f_o) + \sum_{n=1} a_n H(nf_s + f_o) \right\} \delta(f - f_o) \quad (7)$$

where

$$H(f) = (K_{\text{vco}} T_s) \cdot e^{-j\pi T_s f} \cdot \frac{\sin(\pi T_s f)}{\pi T_s f}.$$

The sampled output is filtered by $G(z) = [1 - (1 - a)z^{-1}]/G_d$ before combining with SAR output, and the filtered output is given by

$$X_d(f_o) = AG(f_o)$$
$$\times \left[a_o H(f_o) + \sum_{n=1} a_n H(nf_s + f_o) \right] \delta(f - f_o) \quad (8)$$

where $B(f_o) = 1 - (1 - a)e^{-j2\pi f_o T_s}$. For obtaining closed-form solution, we make the simplifying assumption that $f_o \ll f_s$. Hence,

$$H(f_o) \approx K_{\text{vco}} T_s$$
$$H(nf_s + f_o) \approx K_{\text{vco}} T_s \cdot \left(\frac{f_o}{nf_s} \right)$$
$$\left| 1 - (1-a)e^{-j2\pi f_o T_s} \right|^2 \approx 1 + (1-a)^2 - 2(1-a). \quad (9)$$

Plugging the approximations in (9) into (8), $X_d(f_o)$ can be written as

$$X_d(f_o)$$
$$= A[1 + (1-a)^2 - 2(1-a)]a_o \frac{K_{\text{vco}} T_s}{G_d}$$
$$+ A[1 + (1-a)^2 - 2(1-a)] \cdot \frac{K_{\text{vco}} T_s}{G_d} \left(\sum_{n=1} \frac{a_n}{n} \right) \frac{f_o}{f_s}.$$
$$(10)$$

The first term in (10) is frequency-independent and is canceled after combining VCO and SAR outputs, while the second term is due to the frequency dependence of interstage gain and is not canceled. The in-band power of the second term in (10) can be written as

$$P_s = \text{PSD}_{Q1}(K_{\text{vco}} T_s)^2 \cdot \frac{[1 + (1-a)^2 - 2(1-a)]}{G_d^2}$$
$$\times \int_{f=0}^{f_B} \left[\sum_{n=1} a_n \left(\frac{f}{nf_s} \right) \right]^2 df$$
$$= [1 + (1-a)^2 - 2(1-a)] \frac{\Delta^2}{12} \left(\sum_{n=1} \frac{a_n}{n} \right)^2 \frac{1}{12(\text{OSR})^3}.$$
$$(11)$$

In-band quantization noise power of the second stage can be written as

$$P_q = [1 + (1-a)^2 - 2(1-a)] \frac{\Delta_{\text{adc}}^2}{12} \frac{\pi^2}{3} \frac{1}{(\text{OSR})^3} \quad (12)$$
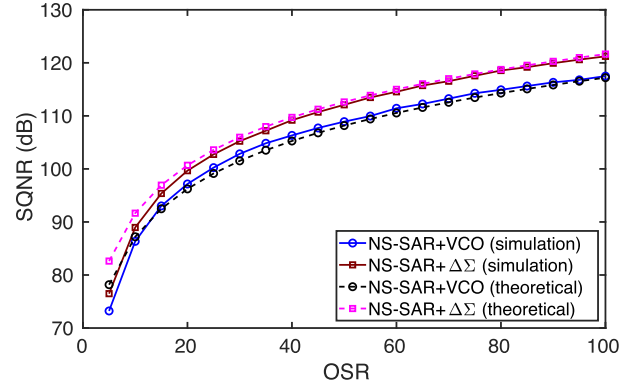

Fig. 21. SQNR of NS-SAR + VCO and NS-SAR + DT $\Delta\Sigma$ as a function of OSR calculated using theoretical equations and simulation.

where Δ_{adc} is the quantization step of the combined ADC without oversampling. The VCO uses seven-stage ring oscillator that quantizes the phase interval $[0, 2\pi]$ into 14 levels. Hence, the VCO quantizer has 3.8-bit resolution, and the combined ADC is an 8.8-bit quantizer without oversampling. The in-band noise power of the NS-SAR + VCO stage, without considering thermal noise, is given by $P_s + P_q$, while the in-band noise power of an equivalent NS-SAR + DT $\Delta\Sigma$ stage is given by P_q since the contribution of quantization noise from the first stage is completely canceled at the output of NS-SAR + DT $\Delta\Sigma$ stage. Fig. 21 shows the SQNR as a function of OSR for NS-SAR + VCO and NS-SAR + DT $\Delta\Sigma$ derived using (11) and (12) and obtained through simulations. The theoretically derived SQNR values match closely those obtained through simulation, except at low OSR where the simplifying assumptions in (9) are not accurate.

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