DATA SHEET

M8132A – 640 Gb/s Digital Signal Processor

Version 0.2

M8132A at a glance

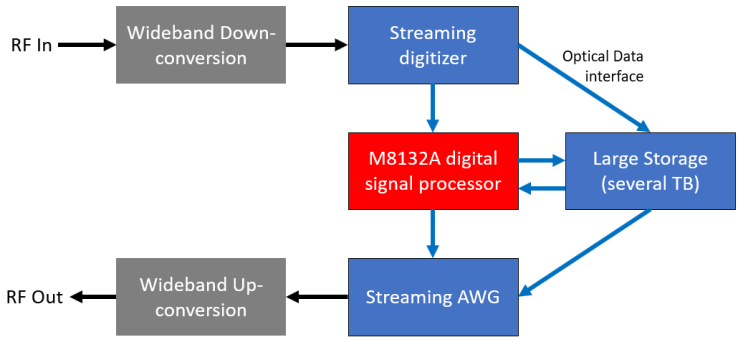
Key features

- Two large Xilinx Ultrascale+ VU9P FPGAs fully usable for custom processing functions
- 4 x 160 Gb/s bidirectional optical data interfaces (ODI)
- Aggregate throughput 640 Gb/s input + 640 Gb/s output
- PCIe backplane interface up to Gen3 x8
- 2 GBytes of HMC memory[1]
- Deterministic latency between Digitizer, DSP module and AWG
- 2-slot AXIe module
- Part of Keysight's Wideband Solution Platform (WSP)

KEYSIGHT TECHNOLOGIES

Wideband Solution Platform

The M8132A is part of Keysight's Wideband Solution Platform that consists of a portfolio of compatible instruments, including digitizer, arbitrary waveform generator, digital signal processor and storage modules. The interconnect between these products is based on a high-speed optical data interface.



Optical Data Interface

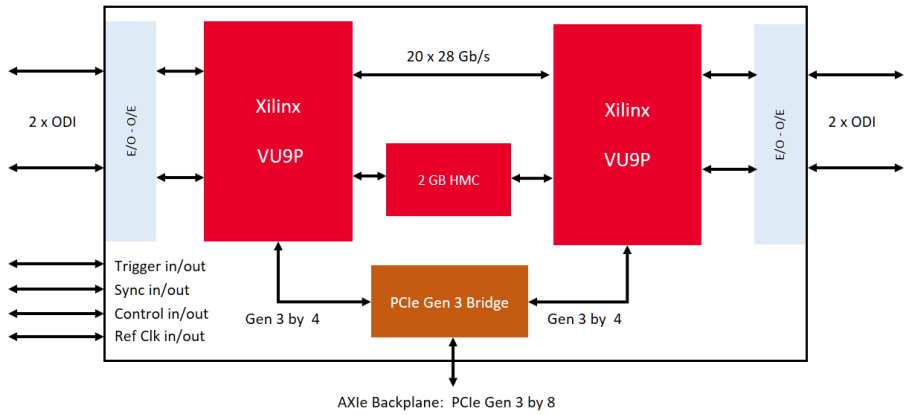
The AXIe Consortium has standardized a high-speed optical data interface (ODI) for advanced instrumentation and embedded systems (http://www.axiestandard.org/odispecifications.html).

The M8132A has four ODI ports on the front panel, each of which allows digital data to be transmitted and received at up to 160 Gb/s per direction.

The optical data interface serves as a backbone between wideband digitizers, AWGs, digital signal processing modules, mass storage devices or custom hardware. Due to the modular structure, different system configurations can be realized. A few examples are shown in the Applications section below.

System Block diagram

The M8132A is a powerful digital signal processing engine consisting of two Xilinx Ultrascale+ VU9P FPGAs, 2 GByte of HMC memory[1] that can be accessed from both FPGAs, four ODI interfaces running at up to 160 Gb/s in+out each, a 560 Gb/s inter-FPGA link[1] and a PCIe Gen3 x8 link to the AXIe backplane. In addition, the module provides a trigger input and output, synchronization input and outputs for deterministic latency between compatible digitizers and AWG modules as well as a 10-general purpose I/Os.



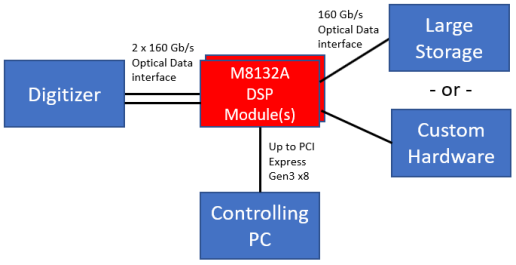
[1] Access to HMC memory and inter-FPGA link is not supported by the PathWaveFPGA software in the initial software release. Please contact Keysight for further details

Applications

Two large FPGAs provide endless signal processing and generation possibilities. Here are a few examples.

Real-time processing of captured data

In many cases, captured data from a digitizer needs to be post-processed in real-time. This can be accomplished in one or more M8132A DSP modules. Possible applications include:

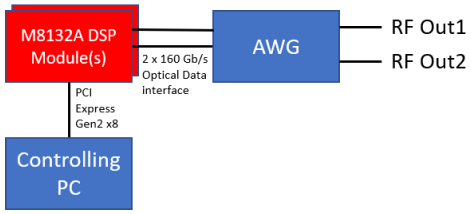


- Demodulation of a communications signal
- Protocol analysis
- Pulse-descriptor-word extraction from a received radar signal
- Real-time spectrum analysis
- Determination of the angle-of-arrival in a phased array antenna
- Custom digital signal processing

Depending on the bandwidth of the post-processed data, it can be streamed into a compatible storage device, into other custom hardware or into the controlling PC through PCI Express.

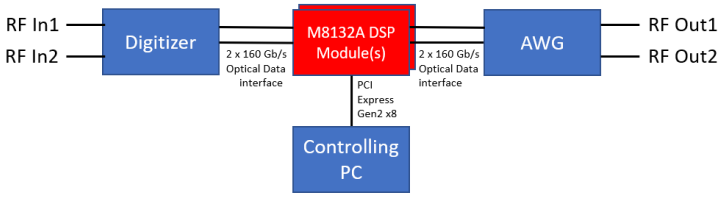
Realtime signal generation

In some AWG applications, waveforms and sequences are too complex to store them in the memory of a conventional AWG. The M8132A can offer a possibility to calculate the AWG waveform in real-time, e.g. radar pulses based on pulse descriptor words or a radio signal based on the digital content



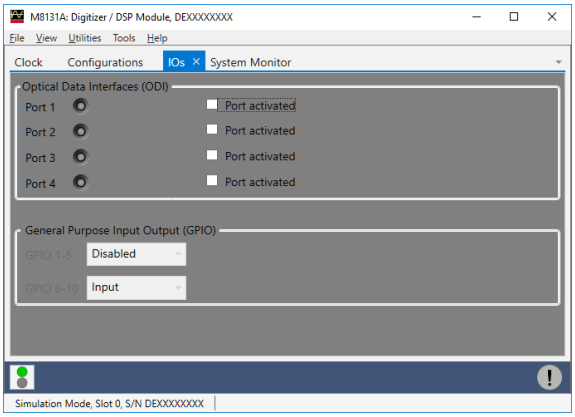
Record and Playback

In combination with a compatible AWG and digitizer, the M8132A can perform real-time processing in a wideband record and playback system. Depending on the amount of processing required, one or more M8132A modules can be cascaded.



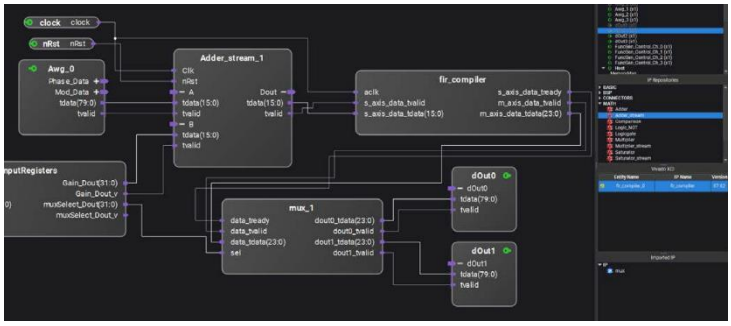
Software

The M8132A is controlled from a windows-based PC through PCI Express or USB. A soft front panel application contains the necessary functions for configuring the ODI ports and loading FPGA images.



FPGA Design and Configuration

Keysight plans to offer the KF9000A PathWave FPGA Programming Environment to allow users to design and configure the FPGAs inside the M8132A. Until this software is available for the M8132A, customers will be supported on an individual basis to develop the desired functionality. Please contact a Keysight representative to discuss details.



Product Structure

Description	Product #	Comment
640 GSa/s digital signal processor module, 2 user accessible FPGAs	M8132A-002	
AXIe infrastructure:		
2-slot AXIe chassis with USB option	M9502A-U20	
5-slot AXIe chassis with USB option	M9505A-U20	
PCIe desktop card adapter Gen 2 x8	M9048A	
x4 – x8 PCIe cable	Y1200B	
x8 – x8 PCIe cable	Y1202A	
Embedded AXIe controller	M9537A	

Performance Characteristics

User accessible FPGAs

FPGA type	2 x Xilinx Ultrascale+ VU9P, speed grade 2
System logic elements	5172k
Registers	4728k
DSP slices	13680

Memory

Memory size	2 GByte, shared amongst all channels

Optical Data Interface

Number of ODI ports	4 (2 ODI ports per FPGA)
Lane rate	12 x 14.1 Gb/s per direction per ODI connector
Supported data formats	User defined
Supported packet formats	User defined
Supported burst sizes	User defined
Flow control	User defined
Connector type	MPO 24

Trigger In

A trigger input is provided on the front panel. The LED next to the Trigger In connector indicates that an externally applied signal matches the adjusted threshold to be used as a Trigger event.

Input range	-4 to +4 V
Threshold	
Range	-4 to +4 V
Resolution	10 mV (nom.)
Sensitivity	100 mV (typ.)
Polarity	Selectable: positive or negative
Input impedance	50Ω (nom.), DC coupled
Max toggle frequency	t.b.d.
Minimum pulse width	t.b.d.
Trigger Delay	t.b.d.
Delay uncertainty	t.b.d.
Connector	SMA

Trigger Out

Output voltage	
High Level	1.1 V (typ.), terminate externally with 50Ω to GND
Low Level	0.5 V (typ.), terminate externally with 50Ω to GND
Rise / fall time (20% / 80%)	55 ps (nom.)
Output impedance	50Ω (nom.)
Connector	SMA

Reference Clock Input

Input frequency	100 MHz
Lock range	±50 ppm (typ.)
Input level	632 mV_{pp} (0 dBm) to 3.1 V_{pp} (14 dBm) ±1 dB (typ.)
Input impedance	50Ω (nom.), AC coupled
Connector Type	SMA

Reference Clock Output

Reference Clock Source: Internal Reference Clock Oscillator	
Output frequency	100 MHz
Frequency accuracy	±3 ppm initial accuracy (nom.), aging less than 20 ppm in 10 years (typ.)
Phase Noise	< -125 dBc/Hz at 10 kHz offset (meas.)
Output amplitude	850 mV ±50 mV (typ.) Terminate externally with 50Ω to GND
Reference Clock Source: External Reference Clock Input	
Output frequency	100 MHz
Frequency accuracy	Same as applied at Reference Clock Input
Phase Noise	determined by phase noise at Reference Clock Input
Output amplitude	850 mV ±50 mV (typ.) Terminate externally with 50Ω to GND
Source impedance	50Ω (nom.), AC coupled
Connector type	SMA

Control Input/Output

A bidirectional parallel port with 10 digital signals is provided on the front panel. This connector is reserved for future use

FPGA Config Connector

An FPGA configuration connector is provided on the front panel to load custom FPGA contents. This connector is reserved for future use.

System Requirements

Operating System	Windows 7, 8, 8.1, 10, 64-bit
Connection to AXIe hardware	PCIe or USB

General Characteristics

Power consumption	280 W (nom.)
Operating temperature	0°C to +40°C
Operating humidity	5% to 80% relative humidity, non-condensing
Operating altitude	Up to 3000 m
Storage temperature	-40°C to +70°C
Stored states	User Configuration and factory default
Power on state	Default
Interface to controlling PC	PCIe or USB (see AXIe specification)
Form factor	2-slot AXIe module
Dimensions (H x W x D)	60 mm x 322.5 mm x 281.5 mm
Weight	5 kg
Safety designed to	IEC61010-1, UL61010, CSA22.2 61010.1 certified
EMC tested to	IEC61326
Warm-up time	30 min
Calibration interval	n/a
Cooling requirements	Choose a location that provides at least 80 mm of clearance at rear, and at least 30 mm of clearance at each side.

Definitions

Specification (spec.)

The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0°C to 40°C and a 30-minute warm up period. Within +/- 10°C after auto calibration. All specifications include measurement uncertainty and were created in compliance with ISO-17025 methods. Data published in this document are specifications (spec) only where specifically indicated.

Typical (typ.)

The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23°C).

Nominal (nom.)

The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and is measured at room temperature (approximately 23°C).

Measured (meas.)

An attribute measured during development for purposes of communicating the expected performance. This data is not warranted and is measured at room temperature (approximately 23°C).

Accuracy

Represents the traceable accuracy of a specified parameter. Includes measurement error and time base error, and calibration source uncertainty.

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