GSTP 6 Element 2: Competitiveness Multi-Purpose Interface Platform

Final Presentation

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1. Introduction

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I. Objectives and Challenges

- The **Objective** was to develop a generic EGSE platform that can be easily expanded to support different electrical interfaces, allow for protocol and interface customization and implement industry standard back-end interfaces.

The **Multi-Purpose Interface Platform** (MPIP)

- The nature of the design is intended to allow for a product delivery with **Quick and Low-Cost** adaptation possibility to ever changing project requirements.
- The main **Challenges** of the activity was the integration of many different spacecraft EGSE interfaces within a single product architecture.
- All the designs and developments were from **Scratch**, inhouse at C-STS.
- This to position a **Competitive** and **Cost Efficient** product on the market

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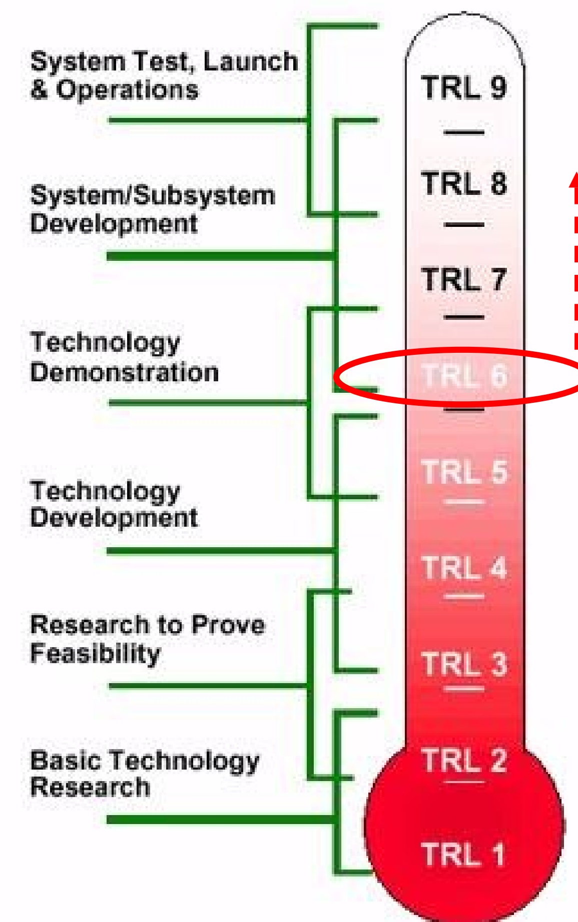
II. Target versus Achievement

- The target was to develop MPIP to **Model** or **Prototype Demonstration (TRL 6)**

- During the early development phases, it was decided to target a **higher TRL** to answer the increasing market demand

- The MPIP consists of various elements, where the table below shows the Target TRL versus Achieved TRL

MPIP Element	Target TRL Level	Achieved TRL Level
Hardware	6	8
Firmware	6	7
Embedded Software	6	7
Application Software	6	6



Source: ESA

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2. EGSE, a Quick Introduction

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I. Satellite Platform Elements

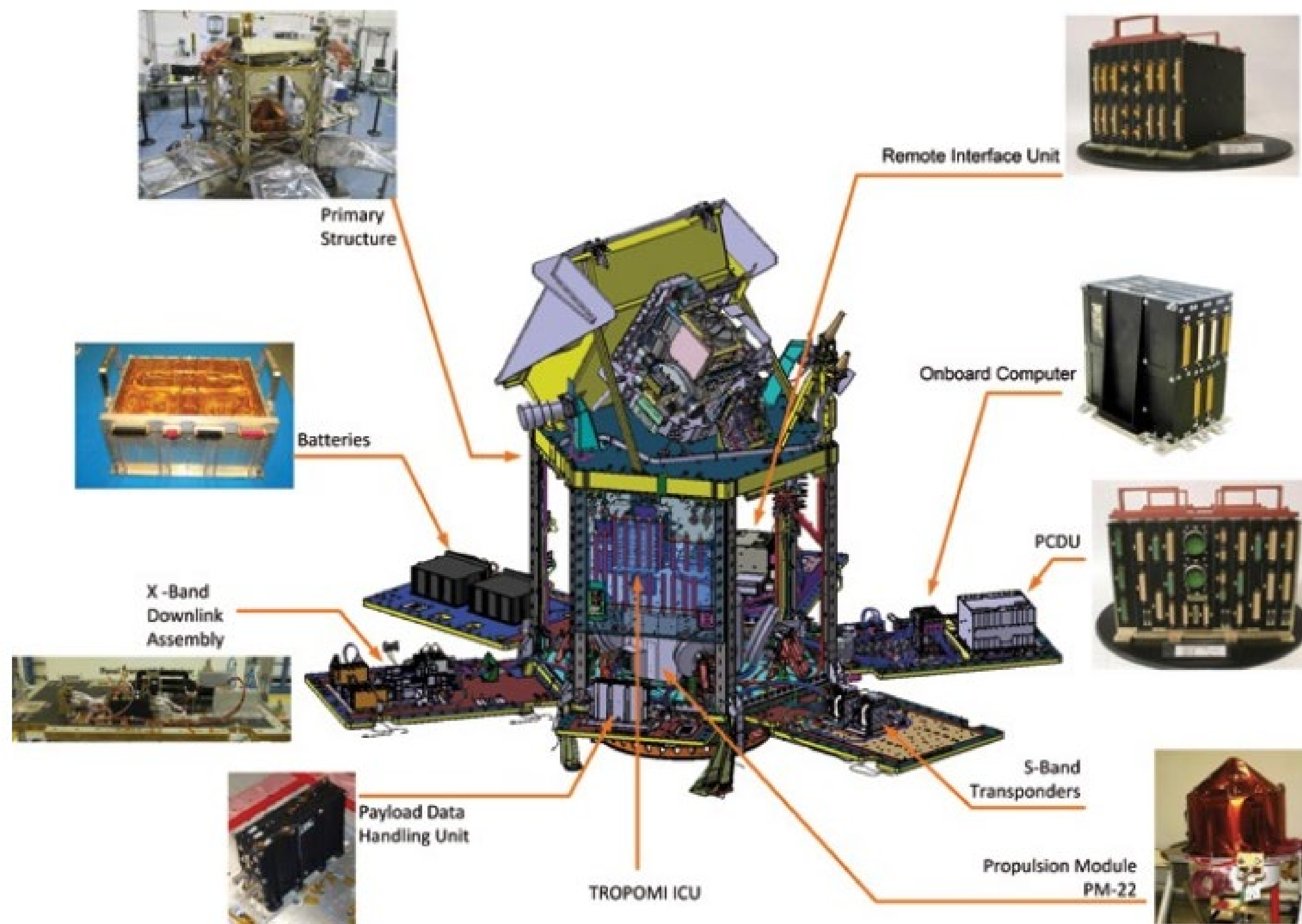

Image: Airbus Defence and Space

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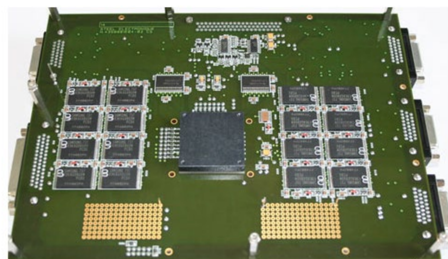
II. Testing on Different Levels

Module Level Testing



Source: Steel Electronique

Unit Level Testing

Source: ESA

Payload Level Testing

Source: SSTL

Satellite Level Testing

Source: ESA

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III. Sub-System Interface Types

Discrete Interface
(Thermistors, Analog, Pulses, switches, etc...)

MPIP

Onboard TM/TC
(MIL1553, CAN, SpW, etc...)

MPIP

Power
(LCL's, Heaters, Pyro, etc...)

Source: ESA

Space-to-Ground TM/TC
(RS422/LVDS Bypass)

Payload Data
(SpF, Parallel LVDS, WzL, etc...)

Modulated IF
(Subcarrier, Carrier, etc...)

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3. Design Concept, Evaluation and Testing

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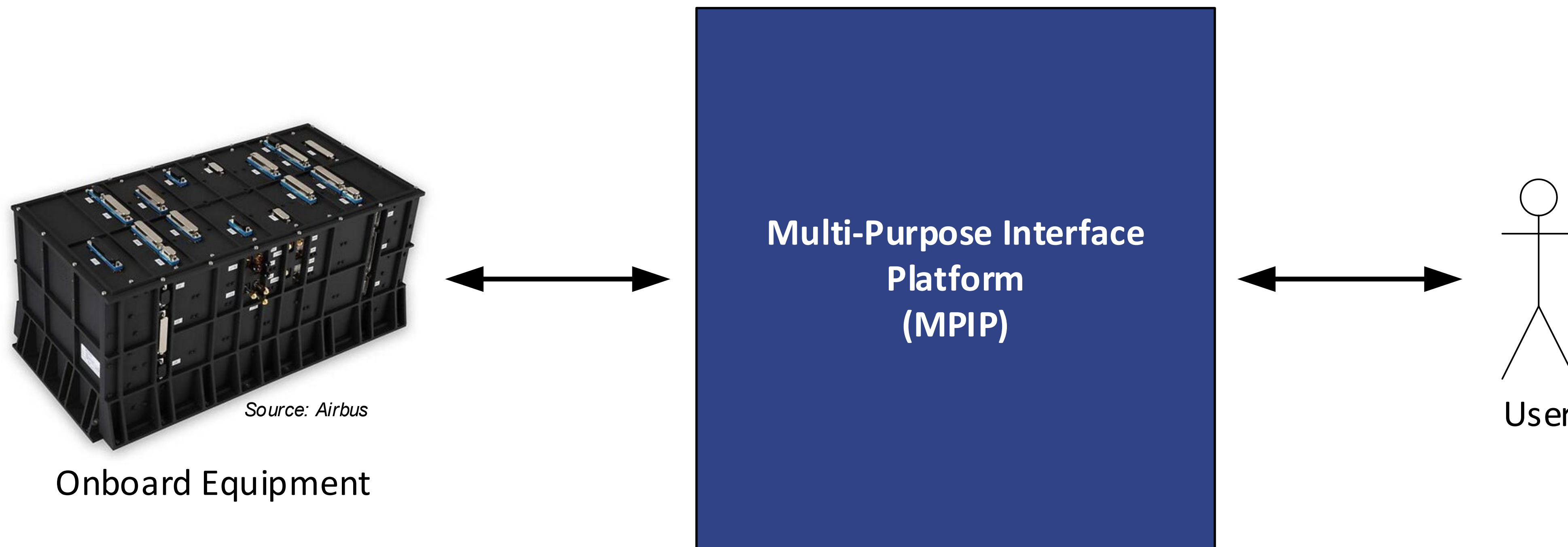
I. MPIP Context



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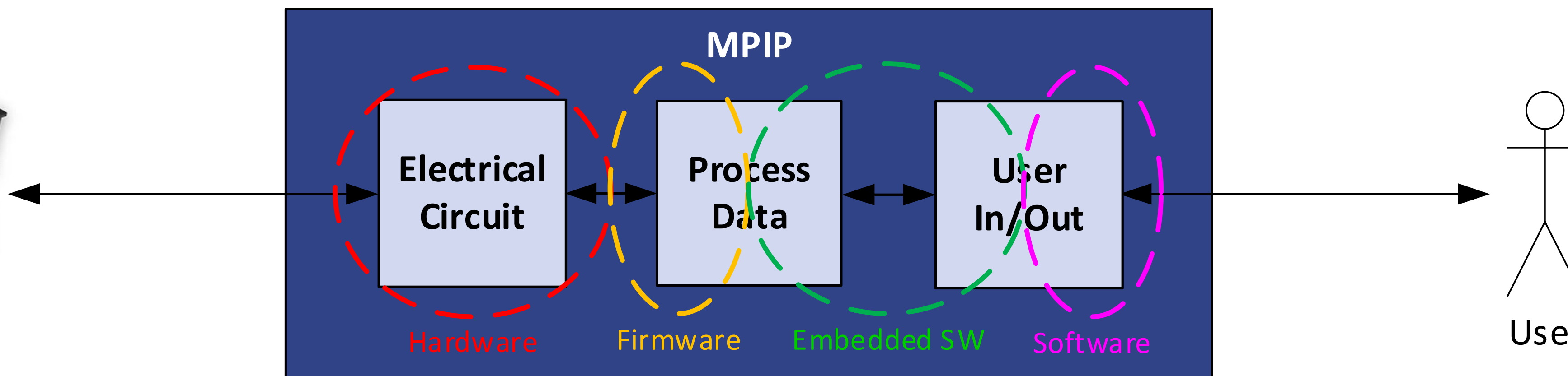
II. MPIP Breakdown

Onboard Equipment



III. MPIP Interface Support (phase-1)

Supported Interfaces Type(s)	Purpose	MPIP Direction
Custom Digital Interface (RS-422 and/or LVDS)	For custom digital interfaces, implemented in firmware	Input & Output
SpaceWire (LVDS)	Transportation of TM/TC or Science Data via SpW Protocol	Input & Output
Latching Current Limiter	To provide a protected voltage and current to power the UUT	Output
Heater Latching Current Limiter	To provide protected voltage to dump resistor to heat the UUT	Output
Analogue Signal Monitor (ASM) Simulation	Analogue voltage (0 to +5V) simulation representing a value	Output
Bi-Level Discrete Monitor (BDM) Simulation	Static state simulation (‘0’ or ‘1’) by analogue voltage level	Output
Analogue Signal Monitor (ASM) Acquisition	Analogue voltage (0 to +5.12V) acquisition of a represented value	Input
Bi-Level Discrete Monitor (BDM) Acquisition	Static state acquisition (‘0’ or ‘1’) by analogue voltage level	Input
Temperature Sensor Monitor (TSM) Acquisition	Resistive temperature sensor acquisition by voltage division	Input
Bi-Level Switch Monitor (BSM) Acquisition	Monitoring of Open/Close State of a switch or relay	Input
Thermistor Sensor Monitor (TSM) Simulation	Temperature simulation by selectable Impedance (resistor)	Output
Bi-Level Switch Monitor (BSM) Simulation	Simulation of Open/Close State of a switch or relay	Output
Low-Power Command (LPC) Simulation	Low-Voltage Pulse generation to drive opto-coupler channels	Output
High-Power Command (HPC) Simulation	High-Voltage Pulse generation to switch relays (load driving)	Output
High-Power Command (HPC) Acquisition	High-Voltage Pulse acquisition of switch relay drivers (load driving)	Input
Low-Power Command (LPC) Acquisition	Low-Voltage Pulse acquisition of opto-coupler drive channels	Input

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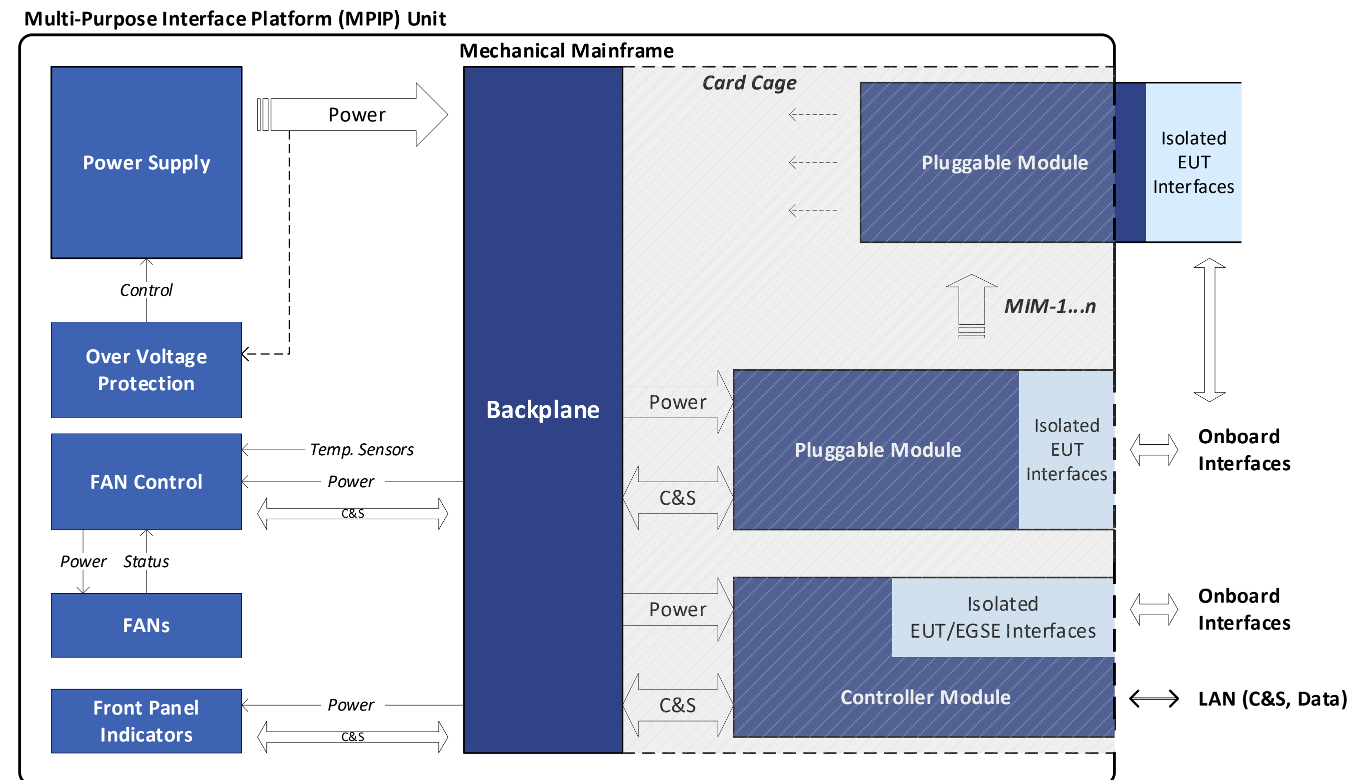
IV: MPIP Architectural Concept

- Depending on the project or program the type and number of interfaces will vary
- To support this flexibility and scalability at the architecture is based on **modules**, both a hardware and software levels
- The **hardware modules** provide the interfaces towards the onboard equipment
- The **firmware and software modules** control the hardware and provide the user interface
- Using **pluggable modules** allows for the required flexibility
- This allows for a combination of **any interface type** in a single mainframe



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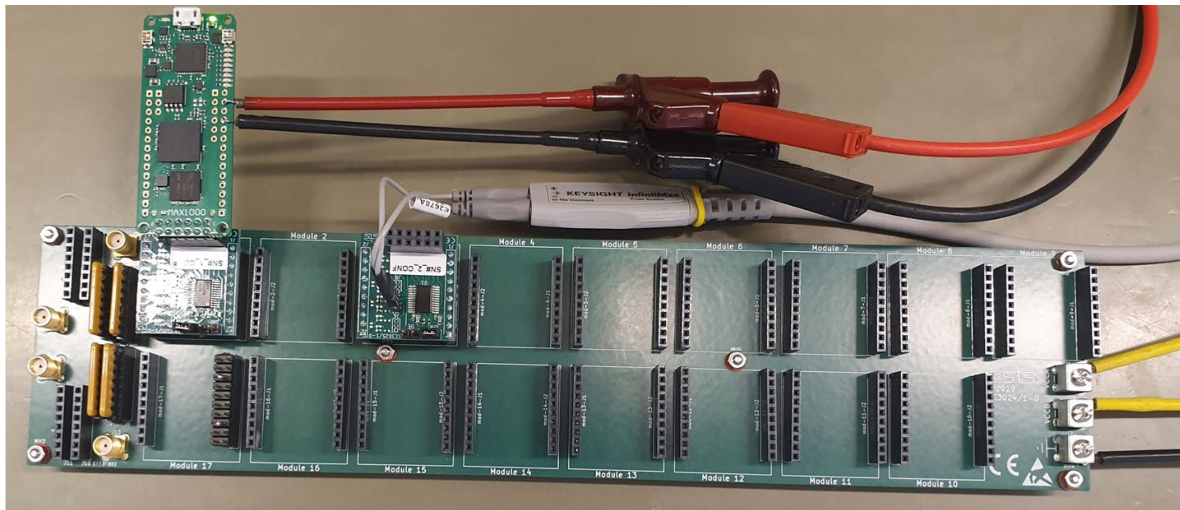
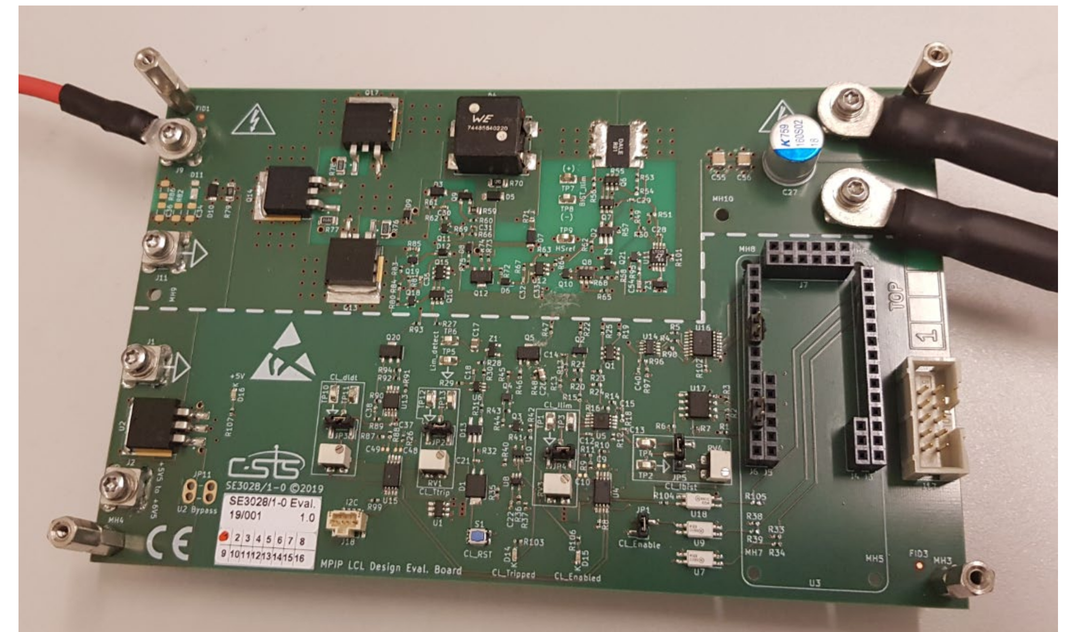
V: Early Proof of Concept

- With a higher TRL target, early proof of concept for various elements was required
- Various Printed Circuit Boards (PCBs) were developed to allow this
- Some examples are:



Backplane Test Setup (testing various electrical standards)



Programmable Latching Current Limiter Evaluation

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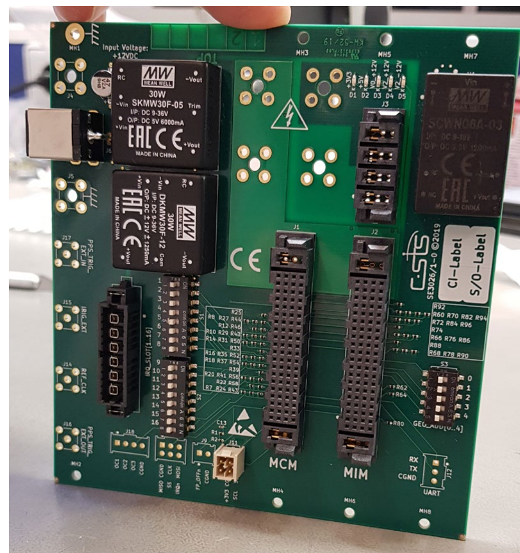
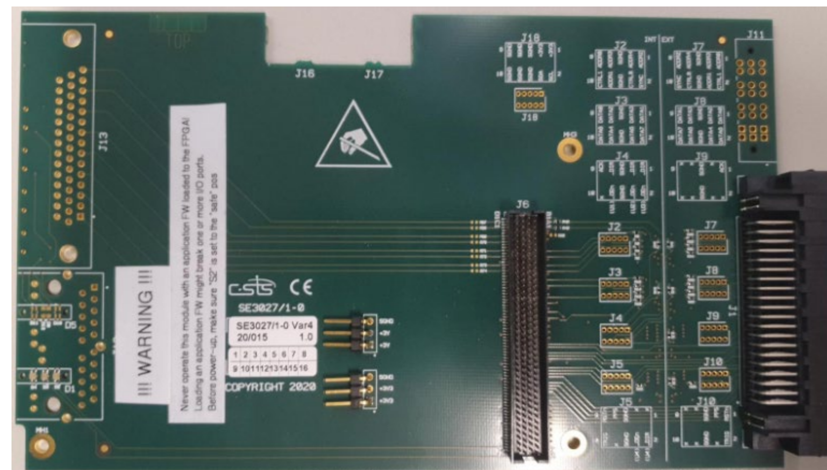
VI: Integration, Test and Verification Aids (I)

- The MPIP development consisted of hardware, firmware, embedded software and application software
- To support the integration, test and verification on all levels, various tools were developed to support these activities early in the project
- Some hardware test and verification tools:



2-slot backplane for on-bench testing



Backplane monitoring board for in system debug communication

Programming and monitoring point access on modules

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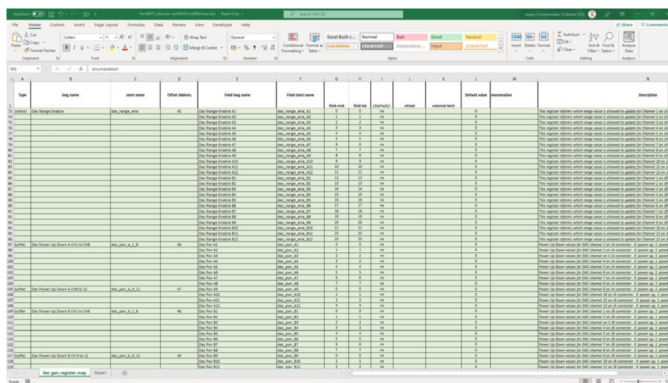
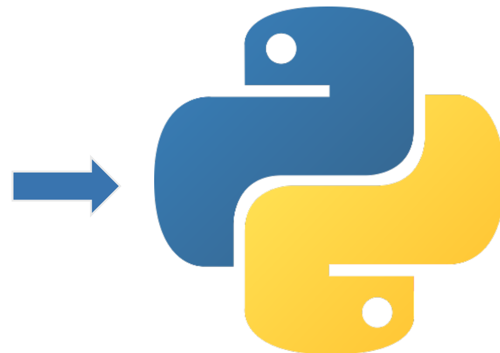
VI: Integration, Test and Verification Aids (II)

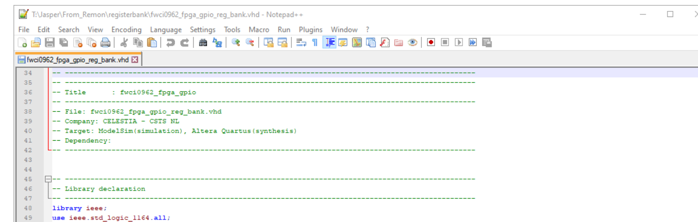
- In addition, various software tools were developed to for example speed up repetitive work
- Example: **Python Code Generator** for register maps, from an **Excel file** automatic **VHDL register code** and **JSON definition file** used by embedded SW to generate the command line interface (CLI) functions



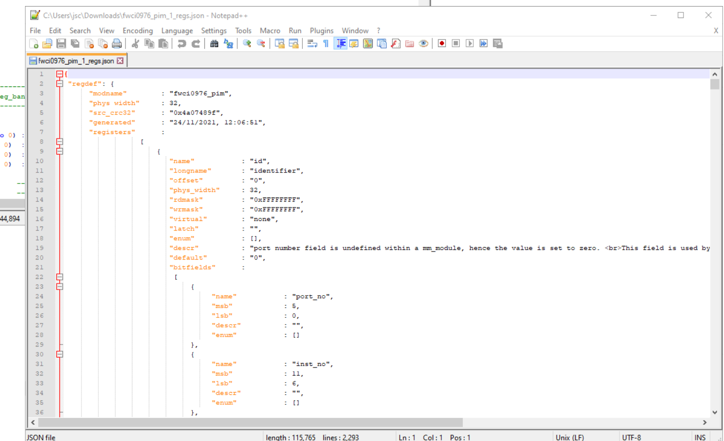
Module Register Map in Excel



Python Script



VHDL Code



JSON Definition

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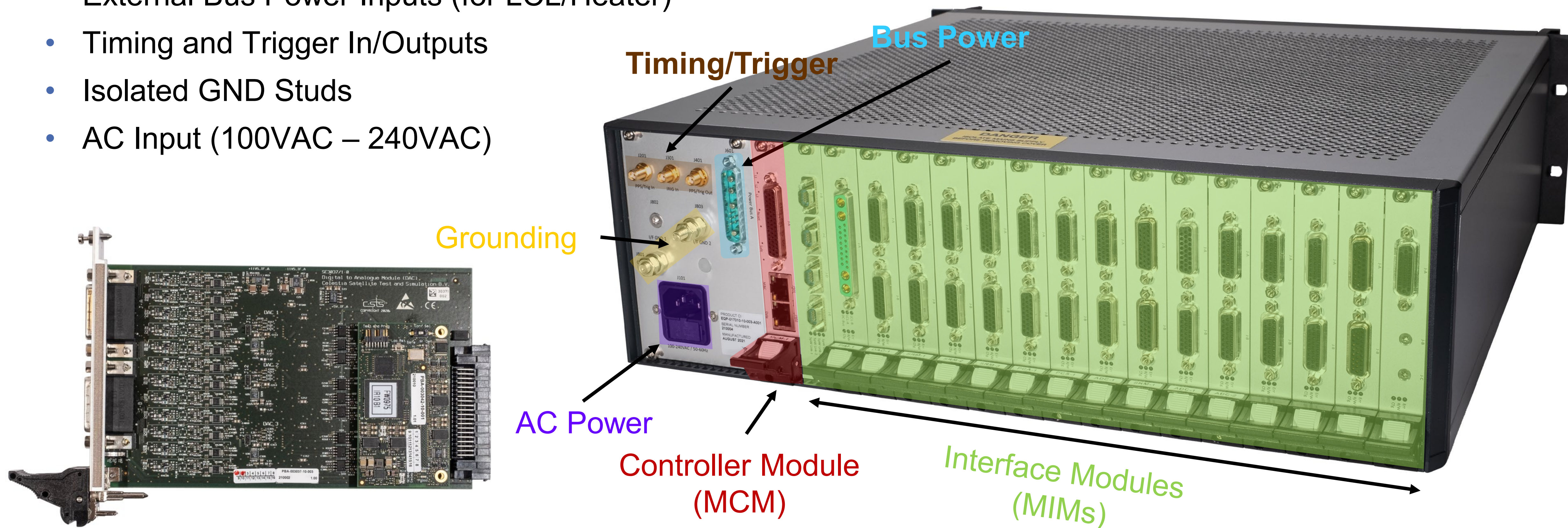
4. Development Results

The actual product that has been developed

I. MPIP Platform

- 3U 19” Rack Mountable Chassis supporting **up to 17 module** slots
- Eurocard (3U) **Pluggable Modules** (100mm × 160mm)
- 1 x MPIP Controller Module (MCM) – **dedicated slot**
- Up to 16 x MPIP Interface Module (MIM)
- External Bus Power Inputs (for LCL/Heater)
- Timing and Trigger In/Outputs
- Isolated GND Studs
- AC Input (100VAC – 240VAC)

Parameter	Characteristic
Height	132.55mm (3U)
Width	448.90mm (19” rack mountable)
Depth	435.50mm (excluding handles)
Empty Weight	9kg (excluding Interface Modules)
Full Weight	13kg (including 16 Interface Modules)



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II. MPIP Interface Modules (1)

- **MPIP Controller Module** (MCM)
  - Provides all Platform Control and Monitoring functions
  - Standard Interface Type Support (20 x RS-422/LVDS)
  - Interface Expansion with up to 2 **Plug-on Boards:**
    - 20 x RS422/LVDS In/Outputs
    - 4 x SpaceWire Interfaces (up to 200Mbps)
  - All interfaces are galvanically isolated
  - Science interfaces supported up to 800Mbps
  - Dedicated 1G TCP/IP Ethernet for External M&C
  - Dedicated 1G TCP/IP Streaming Hardstack for Data Up/Offload
  - Custom Firmware support for project specific functions
  - Compliant with ECSS-E-ST-50-14C (RS422)
  - Compliant with ECSS-E-ST-50-12C (SpW/LVDS)

MCM + RS422/LVDS Plug-on

MCM + SpaceWire Plug-on

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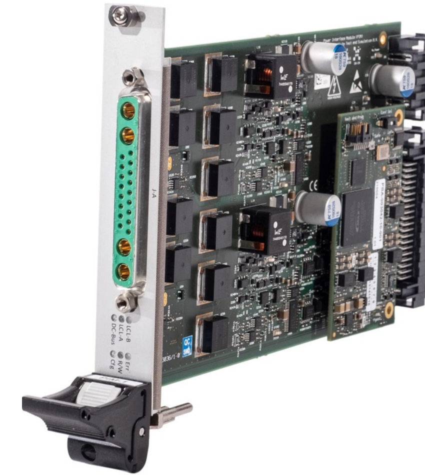
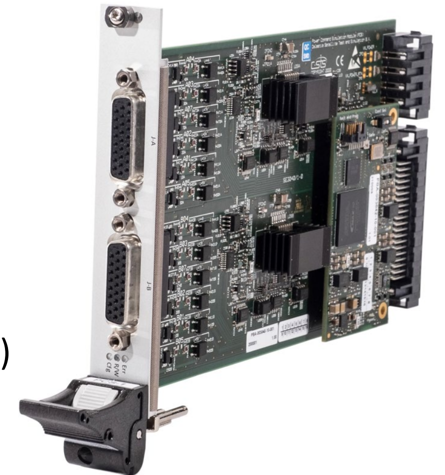
II. MPIP Interface Modules (2)

- **Power Interface Module** (PIM)
  - Up to 2 × Latching Current Limiters or 4 × Heater LCL Outputs
  - Bus Voltages 28V, 50V and 100V
  - Current Classes 0.5A to 20A
  - Configurable UVP, OVP and OCP Levels
  - Configurable Current Change (dI/dt) and Switch-off Time
  - Compliant with ECSS-E-ST-20-20
- **Power Command Simulation Module** (PCS)
  - Up to 24 outputs:
    - Low-Voltage High Power Pulse Command (LV-HPC) Source
    - High-Voltage High Power Pulse Command (HV-HPC) Source
    - High-Current High Power Pulse Command (HC-HPC) Source
  - Compliant with ECSS-E-ST-50-14C (section 7.1)
- **Power Command Acquisition Module** (PCA)
  - Up to 24 outputs:
    - Low-Voltage High Power Pulse Command (LV-HPC) Receiver
    - High-Voltage High Power Pulse Command (HV-HPC) Receiver
    - High-Current High Power Pulse Command (HC-HPC) Receiver
  - Compliant with ECSS-E-ST-50-14C (section 7.1)

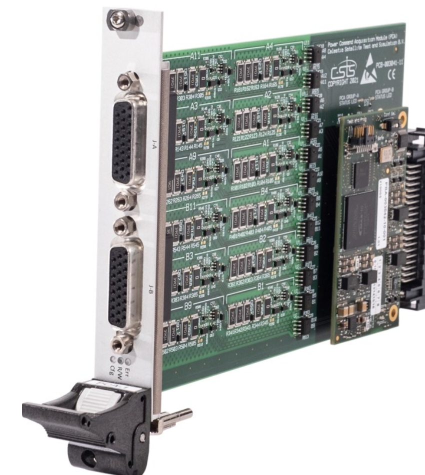
Power Interface Module (PIM)



Power Command Simulator (PCS)



Power Command Acquisition (PCA)



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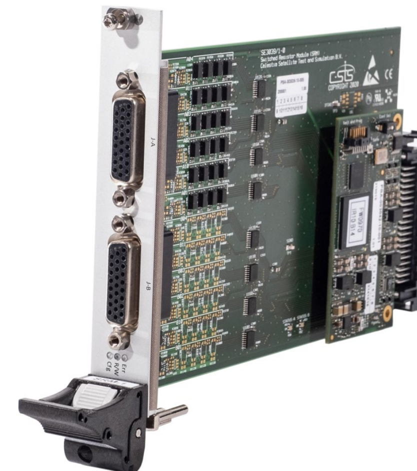
II. MPIP Interface Modules (3)

- **Digital to Analog Module** (DAC)
  - Up to 24 outputs:
    - Analogue Signal Monitor (ASM) Source
    - Bi-Level Discrete Monitor (BDM) Source
  - Compliant with ECSS-E-ST-50-14C (section 5.2 and 6.2)
- **Analog to Digital Module** (ADC)
  - Up to 24 outputs:
    - Analogue Signal Monitor (ASM) Receiver
    - Temperature Sensors Monitor (TSM) Receiver
    - Bi-Level Discrete Monitor (BDM) Receiver
    - Bi-Level Switch Monitor (BSM) Receiver
  - Compliant with ECSS-E-ST-50-14C (section 5.2, 5.3, 6.1 and 6.2)
- **Switched Resistor Module (SRM)**
- Up to 24 outputs:
    - Temperature Sensors Monitor (TSM) Source
    - Bi-Level Switch Monitor (BSM) Source
    - Low-Power Command (LPC) Source
  - Compliant with ECSS-E-ST-50-14C (section 5.3, 6.2 and 7.2)

Digital to Analog Module (DAC)

Analog to Digital Module (ADC)

Switched Resistor Module (SRM)



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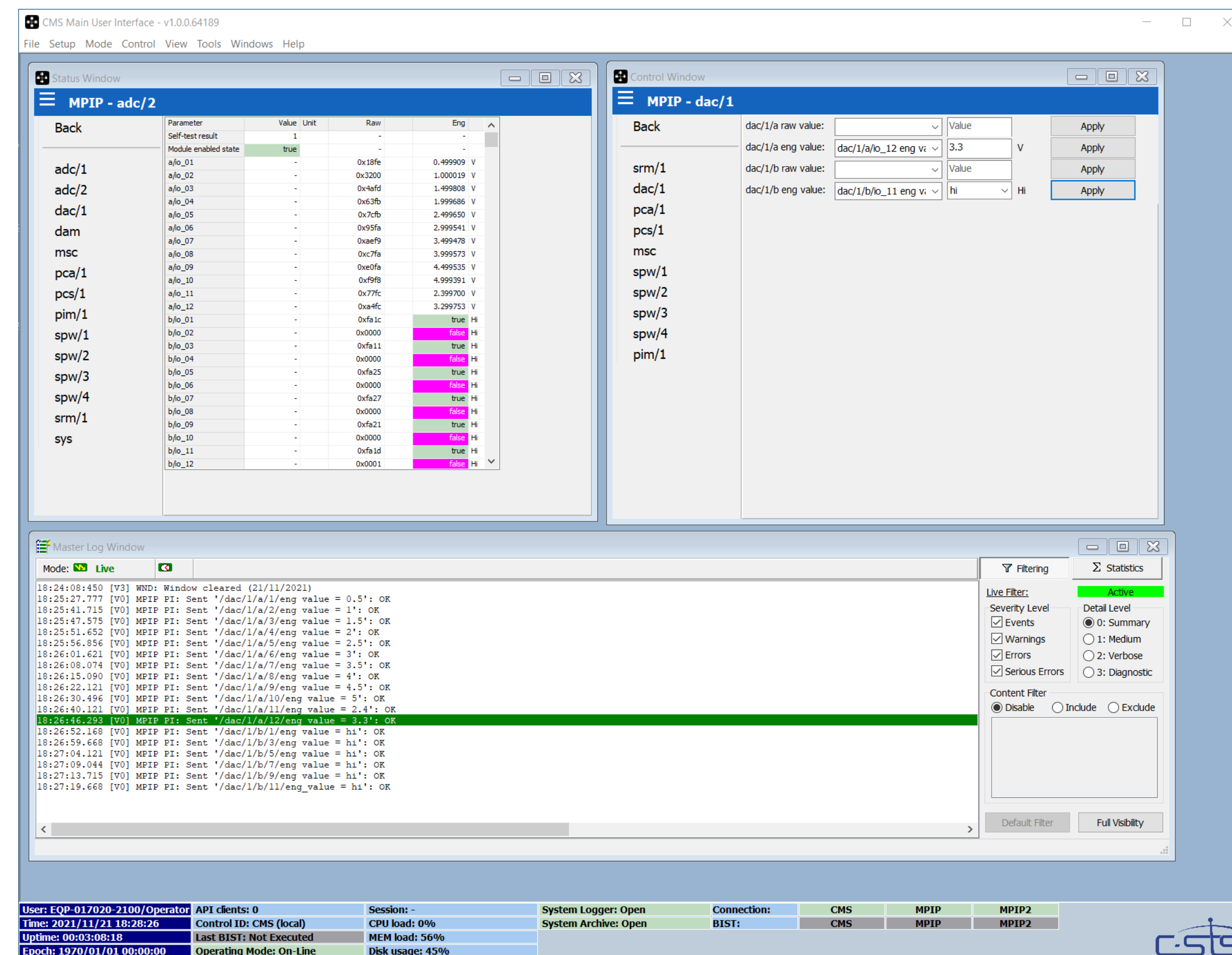
III. MPIP Application Software

- Provides control and status interface to the User
- Plugin based architecture:
  - Supports any combination of interfaces
  - Interfaces to one or more MPIP's in parallel
  - Interfaces with other Front-Ends or Equipment (e.g. MIL-1553, Power Supply, etc.)
- Single Interface to a larger EGSE/SCOE
- Dynamic GUI that automatically adapts to the MPIP configuration (e.g. modules, channels, types, amounts)
- Archiving of data exchange (e.g. SpW Packets, Science Data, etc.)
- Displaying of the system log
- API for system operation by custom SW or Scripting (e.g. Python)



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IV. Development Metrics

- **Printed Circuit Boards**: 18
  - Proof of Concept Boards 3
  - Test and Verification Boards 4
  - Final Product Boards: 11
  - Re-spin Boards: 1
- **Firmware Designs** (VHDL): 7
- **Embedded Software** (C++): 18
  - Software Framework: 1
  - Services and Drivers: 17
- **Application Software** (C++): 17
  - Applications (executables): 3
  - Plugins and Drivers: 14
- **Documents** 159

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5. Changes and Lessons Learnt

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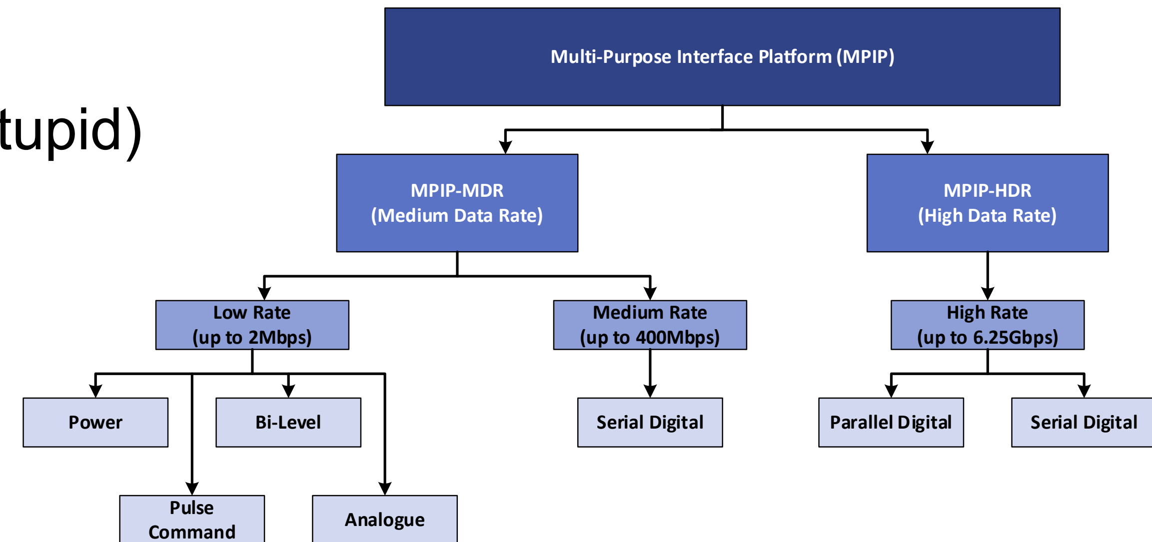
I. Technical

- **Changes during project**:
  - Split-off high-speed from low/medium speed to allow usage of low-cost components making the MPIP more cost affective.
  - Shrinking mechanical form-factor from 6U horizontal modules to 3U vertical modules for efficient use of footprint and allow higher integration in a small package

- **Lessons Learned**:
  - Use the **KISS** principle (**K**eep **I**t **S**imple **S**tupid)
  - The early design evaluation allowed for first-time-right results
  - Consider test and integration needs from the start of the design



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II. Programmatic & Commercial

- **Required effort** significantly **underestimated** at the time of the proposal, especially for software & firmware.
- **Deliverables** defined were in fact still **too many** to fit in the frame of this contract.
- **Required inputs** for certain developments were **not mature** enough at the right stage of the project i.e., EGS-CC.
- **Certain elements** were deemed **less interesting** from commercial point of view i.e., SpaceFibre I/F.

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6. Further Technical Evolution

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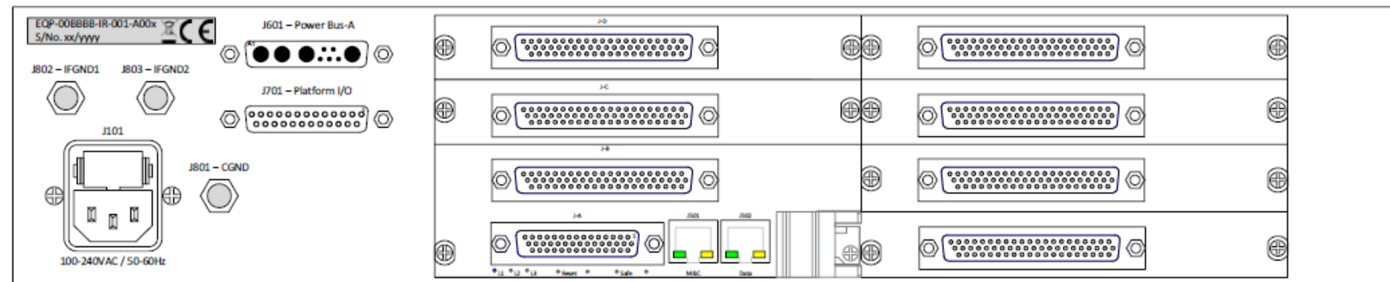
I. CCN & Phase-II Developments

- Successfully implementing the **MPIP Contract Change Notice (CCN)**
  - Implementation of the *SpaceWire RMAP* functionality
  - Enabling *parallelization of LCL* module outputs
  - The development of the *Secondary Level Protection Module (SLP)*
  - The development of the *Power Switch Module (PSM)*
- Phase-II Developments:
  - Develop a **2U MPIP unit** where up to 8 modules can be mounted **horizontally.**



  - To integrate **Baseband TM/TC Processing** into the MPIP architecture.

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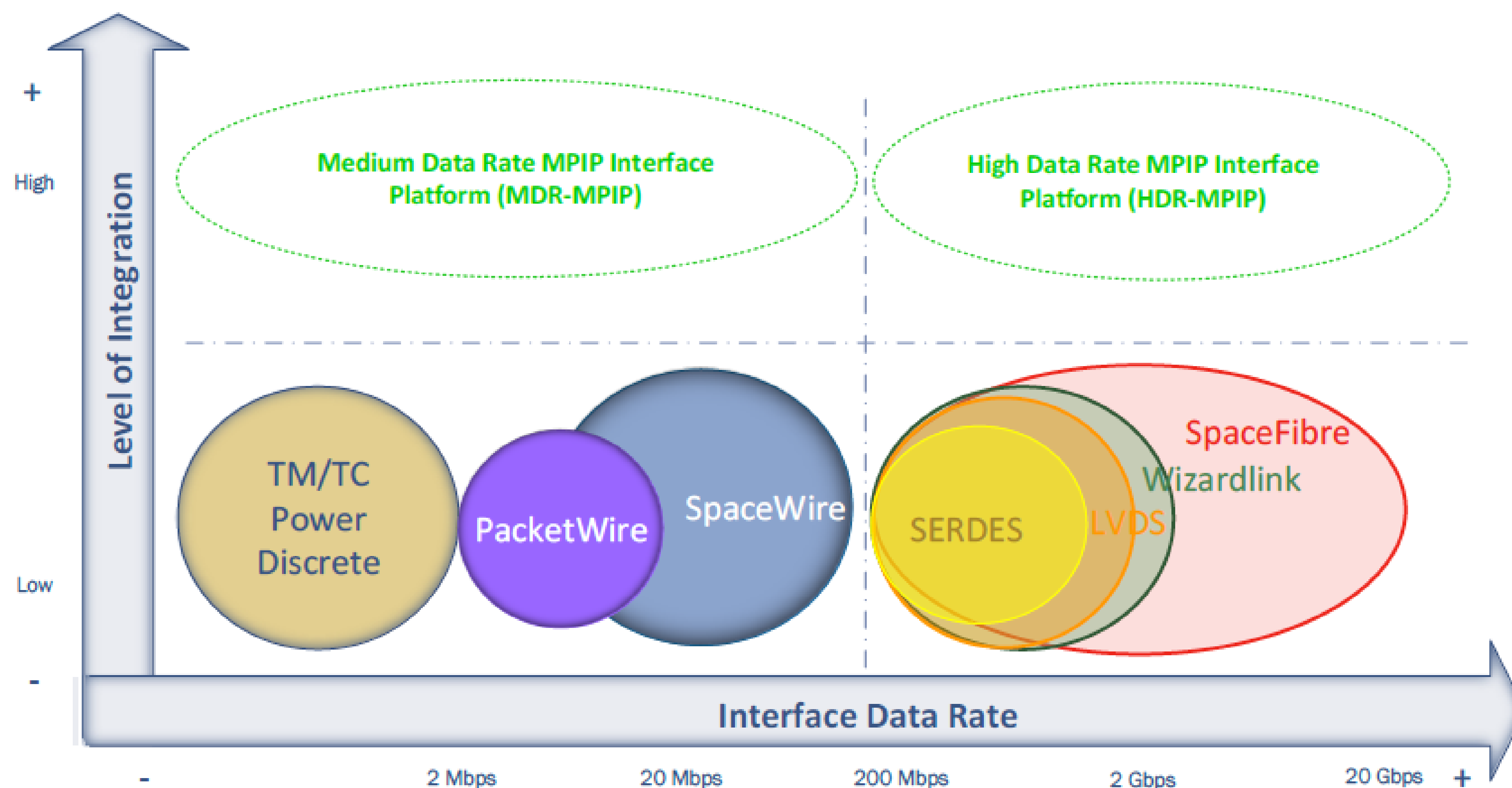
II. MPIP High Data Rate

Further develop **MPIP High Date Rate** modules, like:

- SpaceFibre



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7. Further Commercial Evolution

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I. MPIP as a Market Defender

- During 2019-2021 the MPIP proposal value **>€29M**
- Bids for **major ESA mission** EGSEs:
  - Copernicus
  - Galileo
  - PLATO
  - Space Rider
  - Mars Sample Return
  - Etc..
- MPIP acted as **capability expander**

ID	EGSE Type	Before MPIP	After MPIP
1	Solar Array Simulator (SAS) SCOE		
2	Battery Simulator (BS) SCOE		
3	Battery Conditioning Equipment (BCE)		
4	Umbilical (UMB) SCOE		
5	Pyro/NEA Simulator		X
6	RF SCOE		
7	RF Suitcase	X	X
8	Spacecraft Interface Simulator		X
9	Payload/Instrument SCOE		X
10	PCDU Simulator		X
11	TMTC SCOE	X	X
12	SpaceWire SCOE		(partially)
13	Data Handling (DH) SCOE	X	X
14	SpaceFibre FE		X
15	WizardLink FE	X	X
16	LVDS FE	X	X
17	CAN FE	X	X
18	MIL1553 FE	X	X

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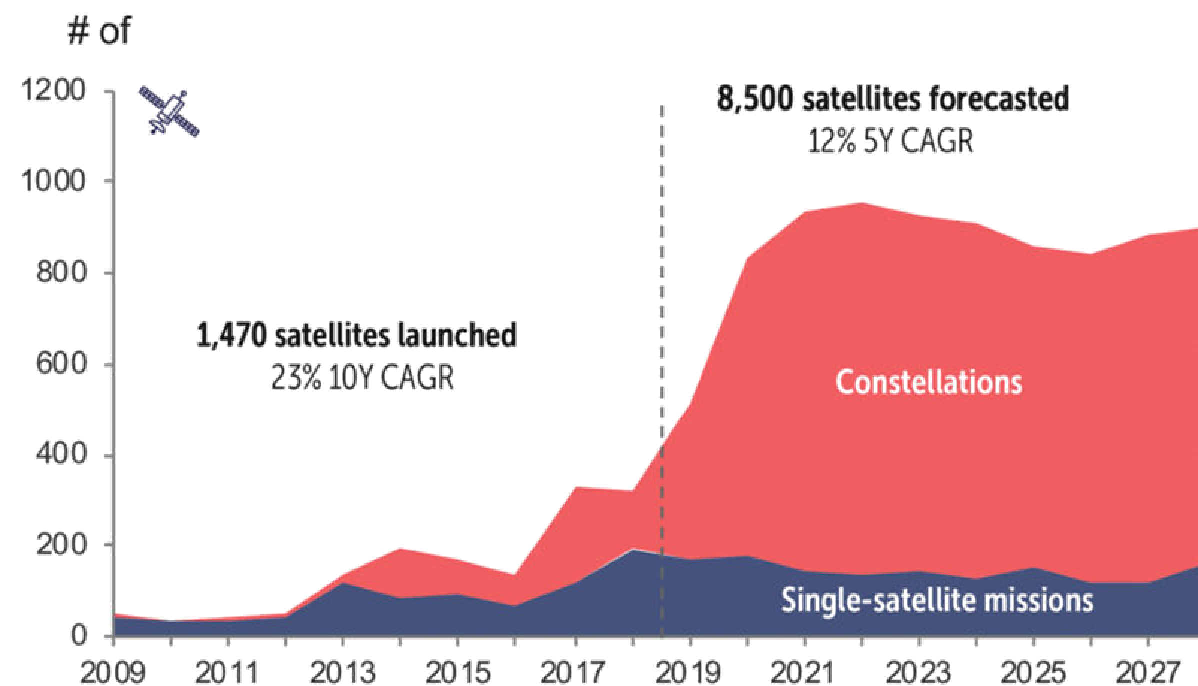
II. MPIP as a Market Enabler

- **8,500 small satellites** to be launched in 2019-2028
- Small satellite market value **$51B by 2029**
- ~70% of market value goes to **manufacturing**
- **~$33B** for manufacturing



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III. Already Secured Contracts

- C-STS have been awarded with **two commercial contracts** for MPIP based EGSE systems.

- In total **5 systems** will be supplied in the scope of a non-ESA mission dedicated to climate monitoring.

- The total value is approximately **€800k.**

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Positive result

Deputy Director NSO, Mr. N Van Putten (right) and J Schoenmaker (left) holding MPIP Unit at Space Tech Expo 2021, Bremen.

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