AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Multi-channel 10b SAR ADCs in 130 nm/65nm

Marek Idzik AGH-UST

M. Firlej, T. Fiutowski, Sz. Kulis(CERN), J. Moron, K. Swientek

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Outline

- Introduction
- Design of SAR ADC in CMOS 130 nm
  - –Architecture
  - –Capacitance switching schemes
  - –Split DAC architecture
  - –From single channel to multi-channel
- Performance of prototype ADCs in 130nm
  - –Measurement setup
  - –Results of static and dynamic measurements for process A and B
- Results on radiation hardness
- Summary

Introduction
ADC Figure Of Merit (FOM)

- Various features/parameters are important in ADC design/applications: effective resolution (ENOB), power, sampling frequency, area, etc... and can be used to create the “Figure Of Merit” (FOM) for ADC
- The first and most commonly used in publications is the so called Walden FOM:

$$FOMW = \frac{Power}{f_{sample} * 2^{ENOB}} \left[J / conv. - step \right]$$

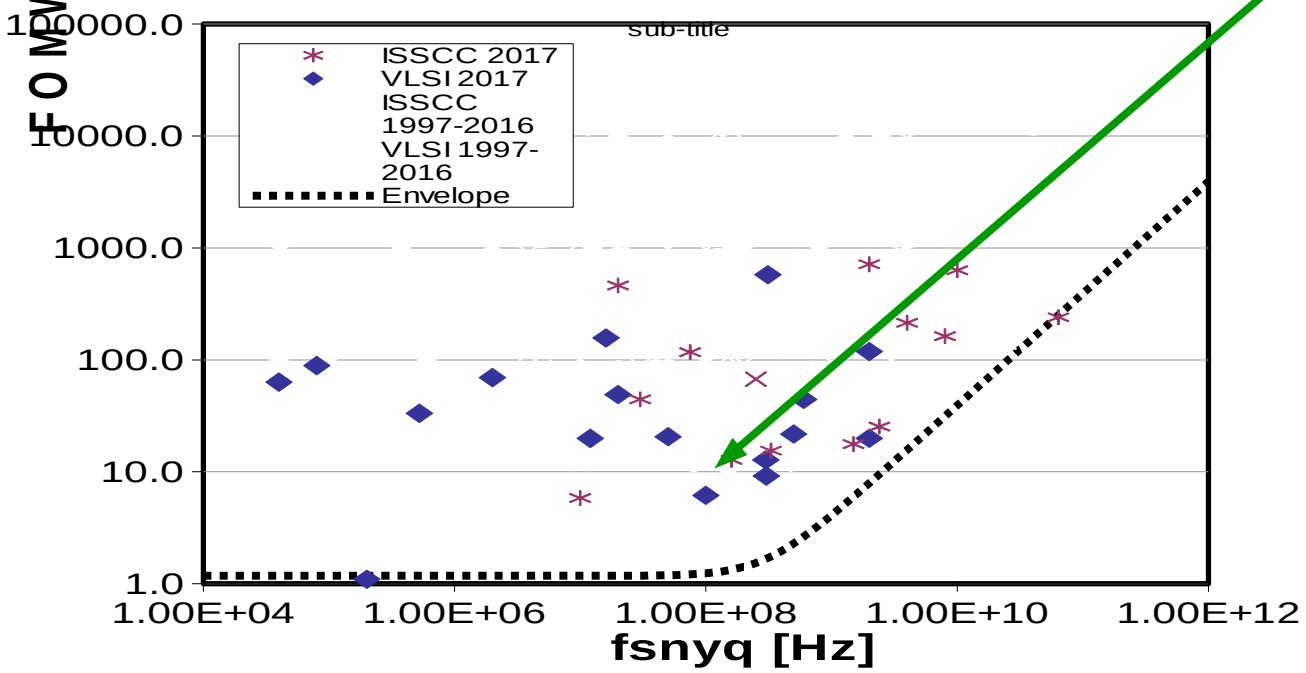
$$ENOB = \frac{SNDR\left[dB \right] - 1.76}{6.02}$$

- FOMW is often given as FOMW_hf (measured at Nyquist input) or FOMW_lf (at lower input frequency)
- Since it is not “perfect”, there are also other FOMs (particularly for higher resolutions), but this one is most commonly used

R. H. Walden, “Analog-to-digital converter technology comparison,” in Proc. of GaAs IC Symp., pp. 228–231, Oct., 1994.
R. H. Walden, “Analog-to-digital converter survey and analysis,” IEEE J. Selected Areas in Communications, no. 4, pp. 539–550, Apr. 1999.

Introduction
Murmann ADC State of Art

Since low power is crucial feature for multichannel readout ASIC the FOM is among the most important ADC parameters

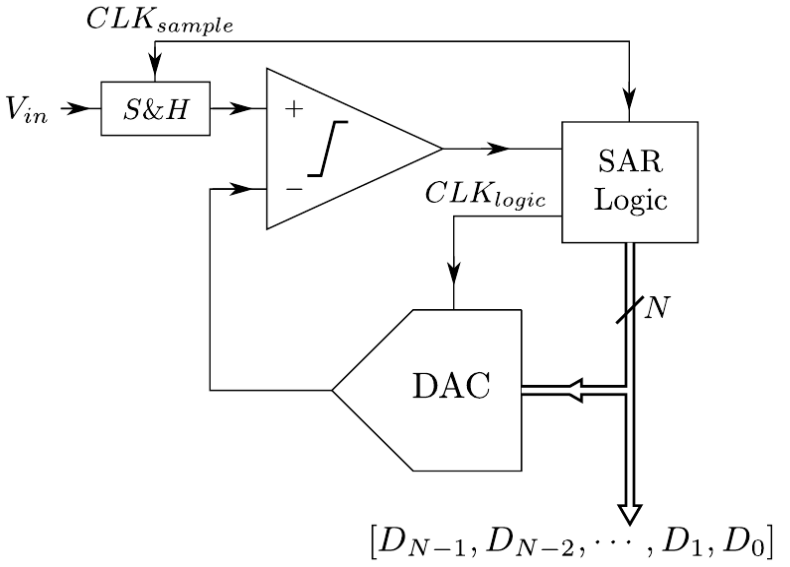


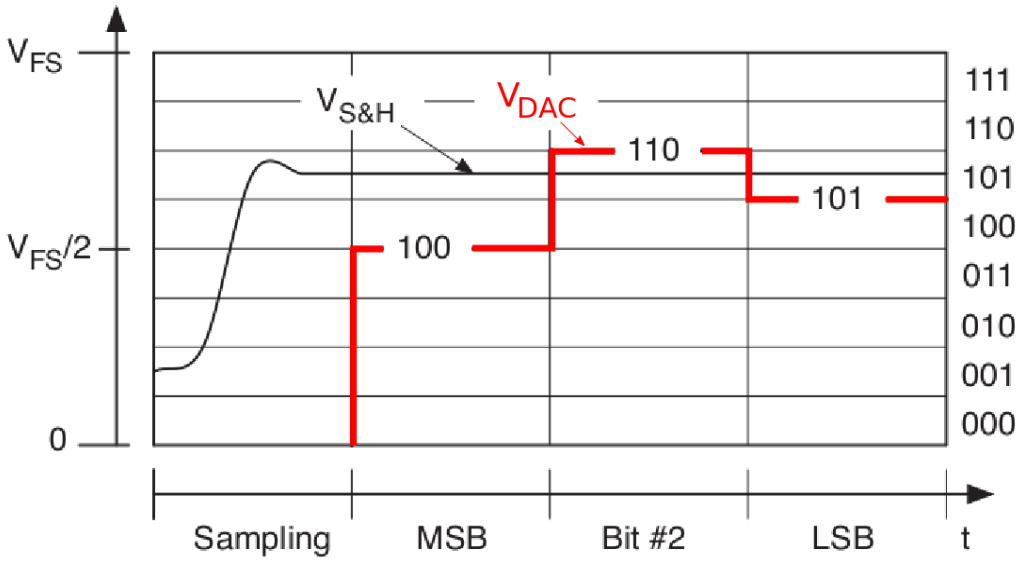
What does it mean in practise ?

- An ADC consuming 0.73mW and achieaving ENOB=9.5 @100MSps (with Nyquist input 50MHz sine) would sit in this point (10fJ/conv.-step @100MHz)
- Designs with FOMW below 20-30 fJ/conv.-step are done in ⩽65nm CMOS

B. Murmann, "ADC Performance Survey 1997-2017", http://www.stanford.edu/~murmann/adcsurvey.html

SAR ADC architecture and features





- Comparison between sampled input voltage and DAC output voltage
- Comparison result → changes DAC output voltage closer to the input sample
- Each consecutive voltage change is half of the previous one
- Operation repeated N times for N-bit ADC

\+ Power and area-efficient architecture – *same circuitry used in loop N-times*

\+ Contains: one comparator, two DACs (differential) and SAR logic – *fits well to modern digital CMOS*

\+ DAC network usually capacitive - *no static power, serves also as S/H circuit*

– Limited conv. rates – *but with modern CMOS (~20nm) >300MSps 10-bit ADCs are reported*

Design of SAR ADC in CMOS 130 nm

Design of SAR ADC in CMOS 130nm
Specifications for 10-bit SAR

Design specifications:

- Variable sampling rate up to ~50 Msps and power consumption scaling with rate
- Ultra-low power consumption <1 mW at 40 MS/s
- Good ENOB > 9.?
- Good linearity INL,DNL ~ 0.5LSB
- Made as IP block
- Ready for multichannel implementation (e.g. small pitch <200um, No clk distribution)

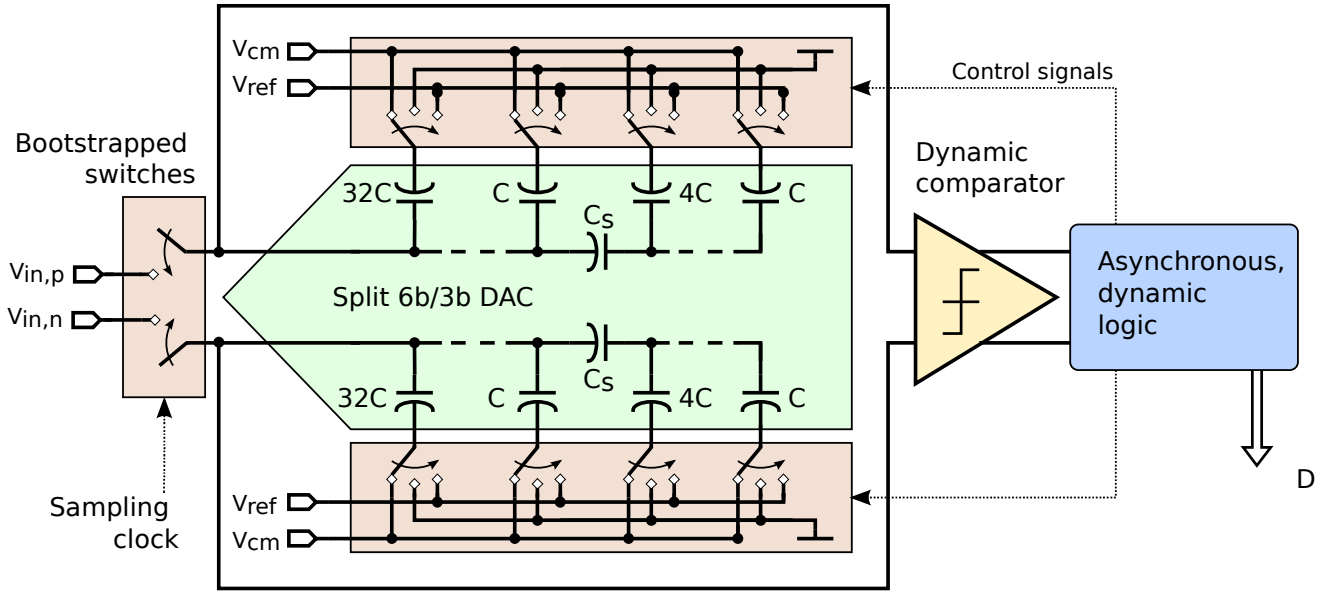
These specifications were based on excellent paper about SAR ADC:

- *Ch. Ch. Liu, S-J. Chang, G-Y.Huang, Y-Z. Lin, "A 10-bit 50MS/s SAR ADC with a monotonic capacitor switching procedure" , IEEE Journal of Solid-State Circuits v.45 p.731-740 2010.*

which presented the design in CMOS 130nm featuring:

- Sampling rate 50 MSps
- Power 826uW@50MSps
- INL<1.36, DNL<0.91
- ENOB ~9 bit, ENOB_lf 9.18
- FOMW_hf ~32-35 fJ/conv.-step, FOMW_lf 29 fJ/conv.-step

Design of SAR ADC in CMOS 130nm
Chosen architecture of 10-bit SAR



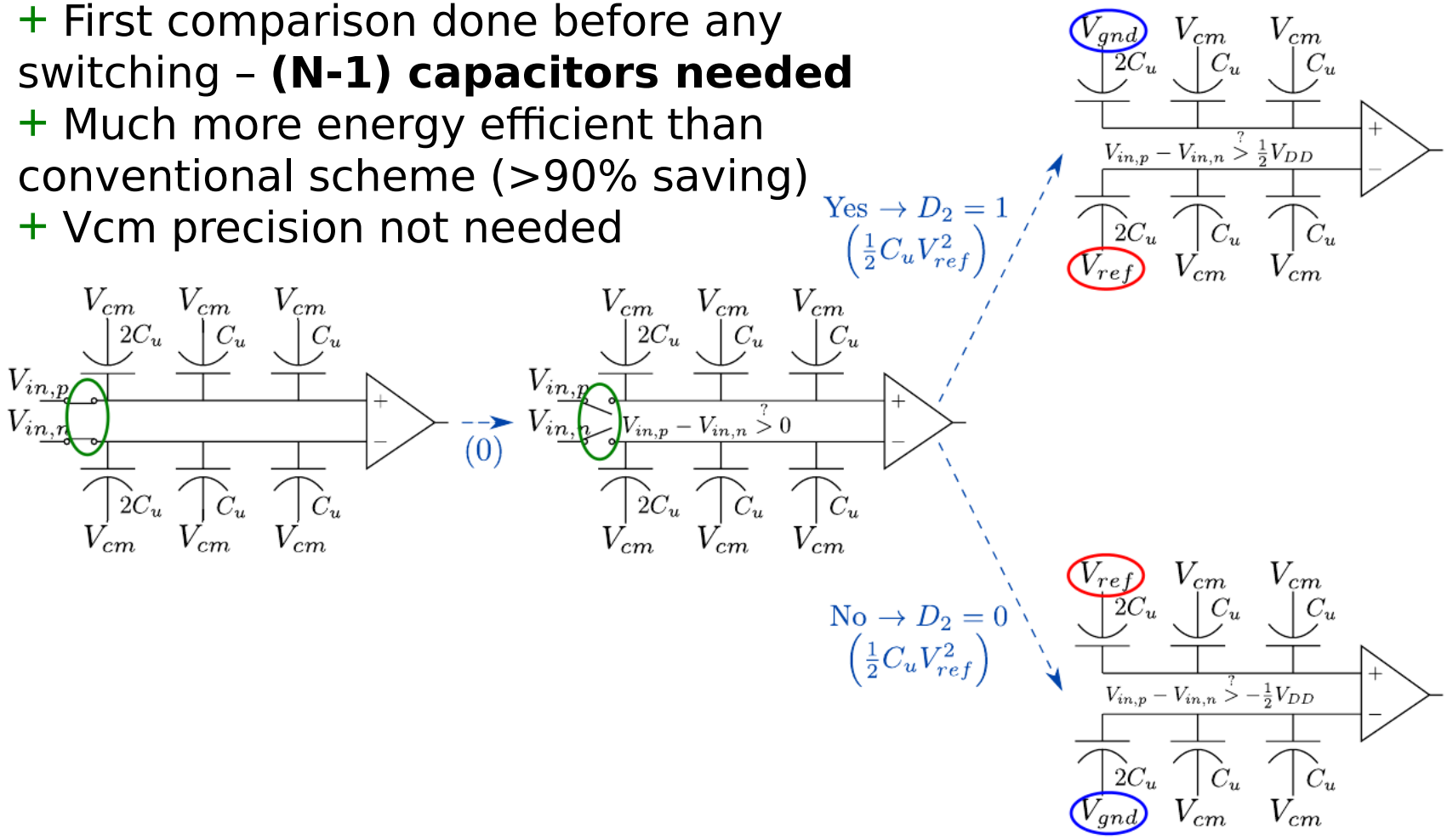
Main features:

- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption***
- Asynchronous and dynamic logic – no clock tree – ***power saving, allows asynchronous sampling***
- Bootstrapped sampling switch for good linearity

M. Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, J. Moroń, K. Świentek "A fast, ultra-low and frequency-scalable power consumption, 10-bit SAR ADC for particle physics detectors", JINST 10 (2015) P11012

Design of SAR ADC in CMOS 130nm
Merged Capacitor Switching (MCS) scheme

+ First comparison done before any switching – **(N-1) capacitors needed**
+ Much more energy efficient than conventional scheme (>90% saving)
+ Vcm precision not needed



Design of SAR ADC in CMOS 130nm
DAC Capacitance Mismatch and Noise

Noise

- Thermal switch noise of sampling circuit – kT/C

$$\frac{kT}{C} < \frac{\sigma^2}{12}, \sigma = \frac{V_{ref}}{2^N}$$

$$C > 12\,kT\left(\frac{2^N}{V_{ref}}\right)$$

- For V_{ref}=1 V:

N=6 bits	C >	0.2 fF
N=8 bits	C >	3.3 fF
N=10 bits	C >	52.0 fF
N=12 bits	C >	830.0 fF

For 10-bit ADC switch noise is negligible

Matching

For a design without digital error correction or digital calibration, the capacitance matching limits the resolution.

Minimum capacitance C_u

$$C_u \sim K_\sigma^2 K_C$$

For process A C_{min}=46 fF (MIMCAP)

K_σ=4.12 %µm K_C=2.05 fF/µm^2

$K_\sigma = 4.12\,\%\mu m \quad K_C = 2.05\,fF/\mu m^2$

$C_{min} \sim K_\sigma^2 K_C$

For process B C_{min}=26.2 fF (MIMCAP)

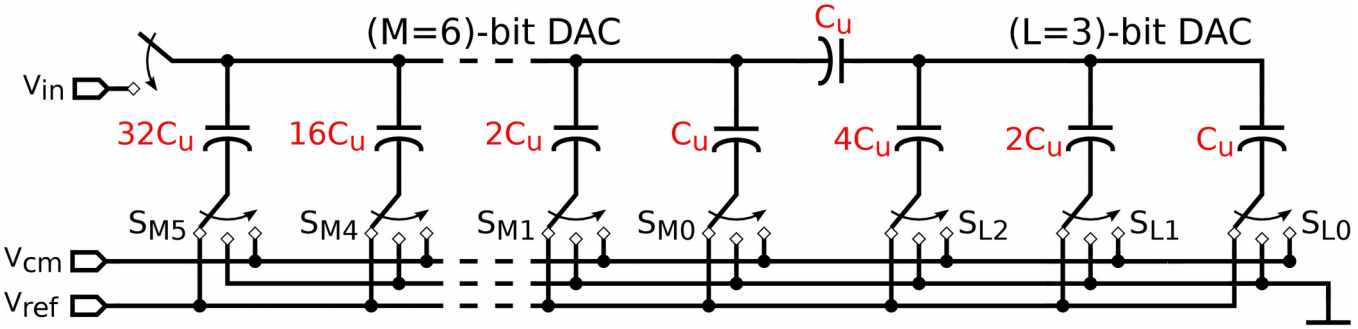
K_σ=1.44 %µm K_C=1.55 fF/µm^2

$K_\sigma = 1.44\,\%\mu m \quad K_C = 1.55\,\frac{fF}{\mu m^2}$

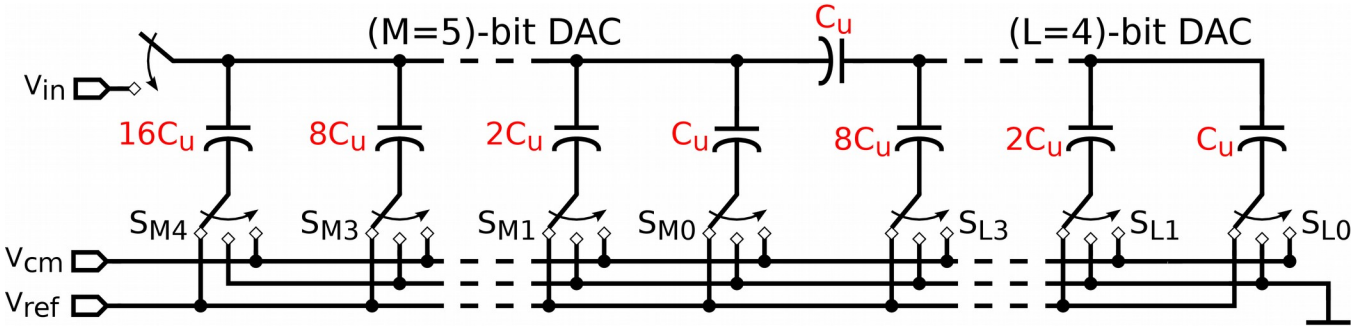
Good matching in process B, but C_{min} still high...

Design of SAR ADC in CMOS 130nm
Applied DAC splits (in process B)

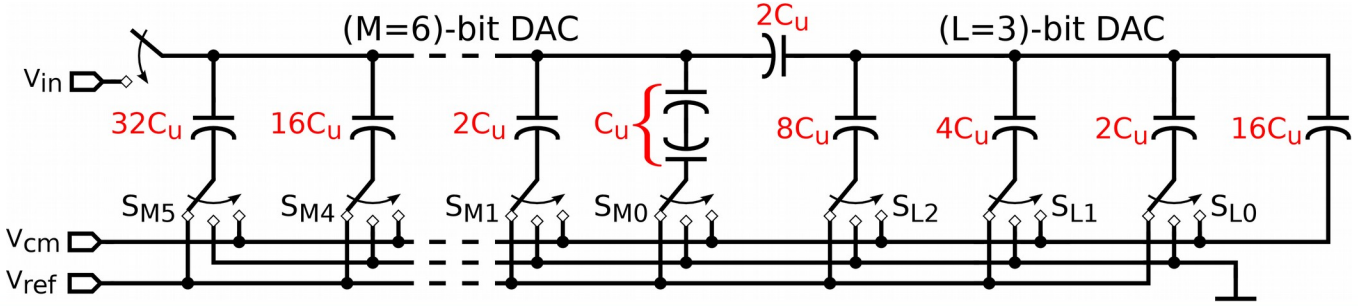
- **DAC 613**
- C_{in} = 1.68 pF
- C_{tot} = 1.86 pF



- **DAC 514**
- C_{in} = 0.84 pF
- C_{tot} = 1.23 pF



- **DAC 623**
- C_{in} = 0.83 pF
- C_{tot} = 1.04 pF



C_u=26.2fF

Design of SAR ADC in CMOS 130nm
Dynamic comparator

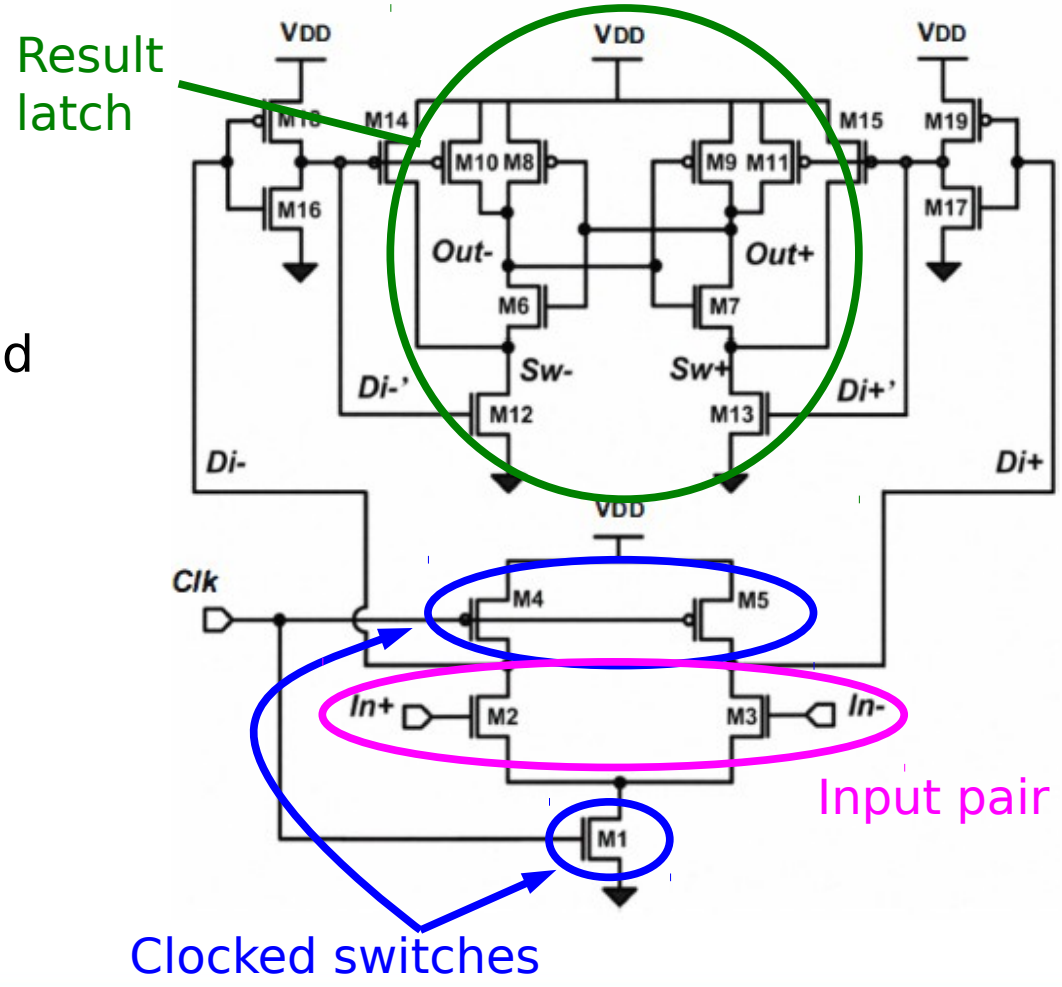
H.J. Jeon, Y-B. Kim, M. Choi "Offset voltage analysis of dynamic latched comparator", IEEE 54th Int. Midwest Symp. On Circuits and Systems, 2011

Dynamic comparator

- Comparison performed on rising edge of clock signal
- Reset (low clock level) needed before next comparison

Pros and cons:

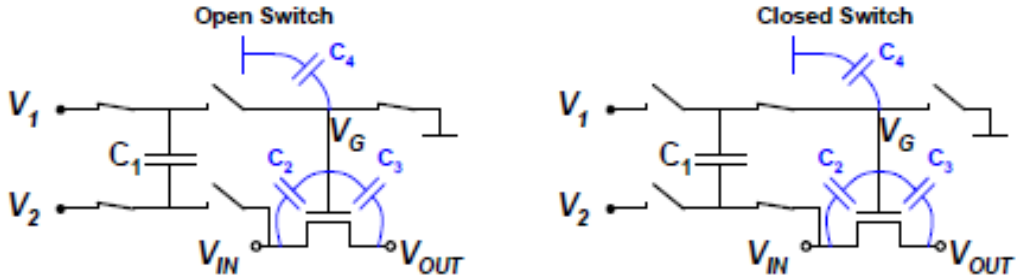
\+ No direct path current
\+ Low power consumption
– Dead time needed for reset



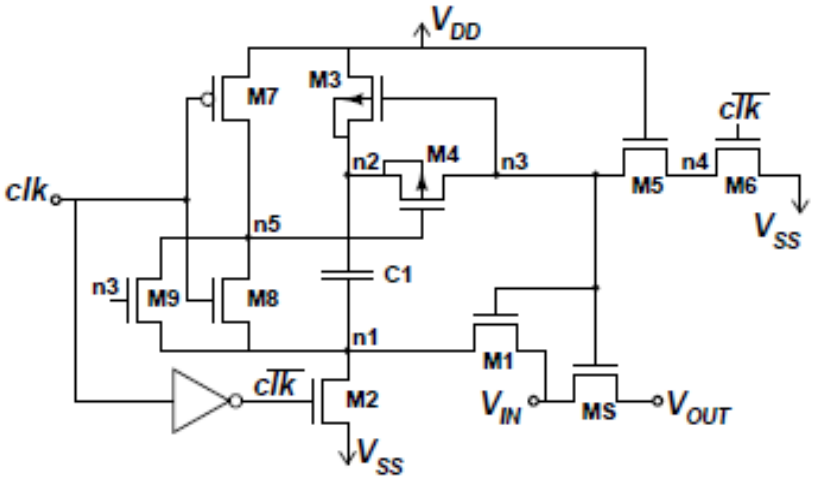
Design of SAR ADC in CMOS 130nm
Bootstrap S/H switch

How to minimize signal distortion during sampling phase ?

Idea



Implementation



M. Dessouky, A. Kaiser, "Input switch configuration for rail-to-rail operation of switched opamp circuits",Electronics Letters vol. 35 no. 1 pp. 8-10 January 1999

Design of SAR ADC in CMOS 130nm
Asynchronous logic

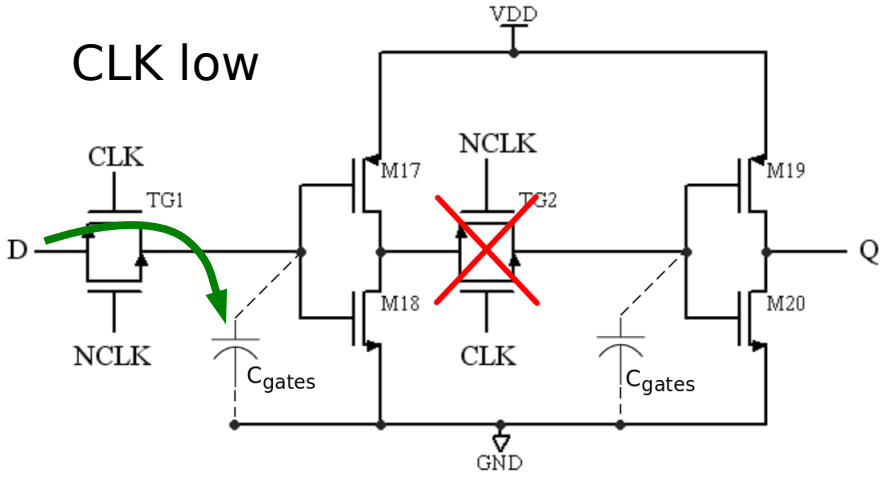
Dynamic D-type flip-flop:

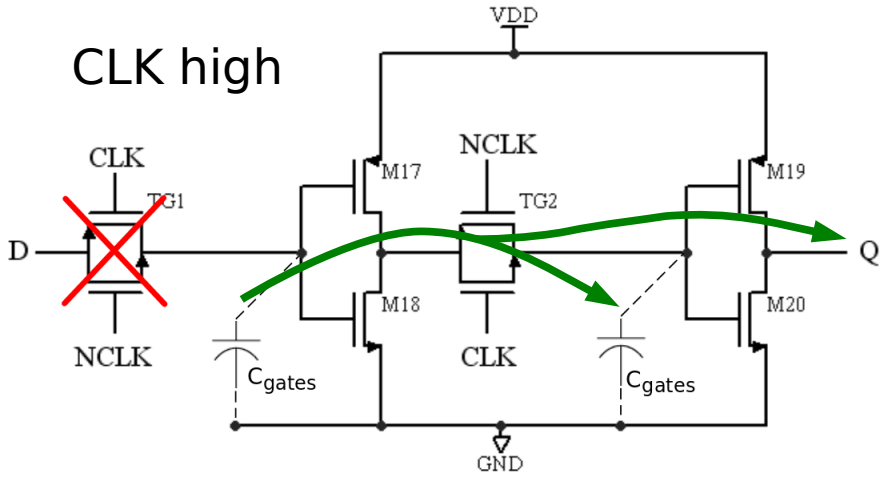
- Bit (voltage level) stored on inverter gate capacitance

+ Very fast - only two small transistor gates need to be recharged on each clock slope

– Clock needs to run continuously (or static reset is needed)

– Manual layout



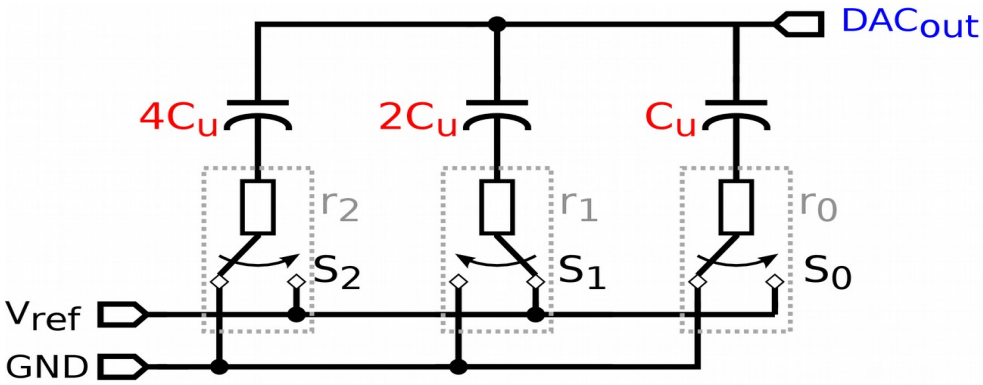


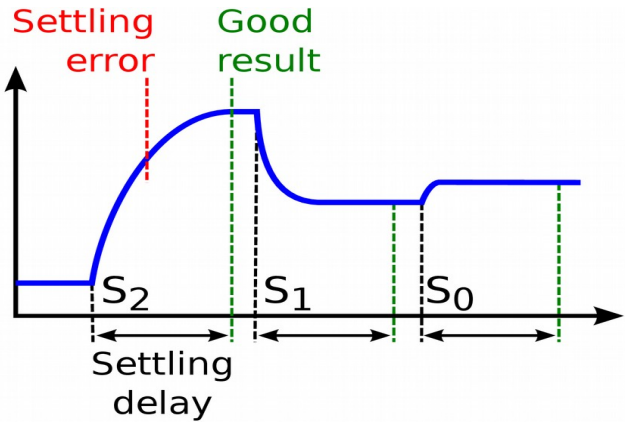
Flip-flop Architecture Process A	Signal propagation time [ps]	Power consumption [µW/clk cycle]
Static	155	2.62
Dynamic	**50**	**2.58**

Process B – dynamic only a bit faster than static
But consumes only ~50% power

Dynamic flip-flop is much more power efficient

Design of SAR ADC in CMOS 130nm
Asynchronous logic

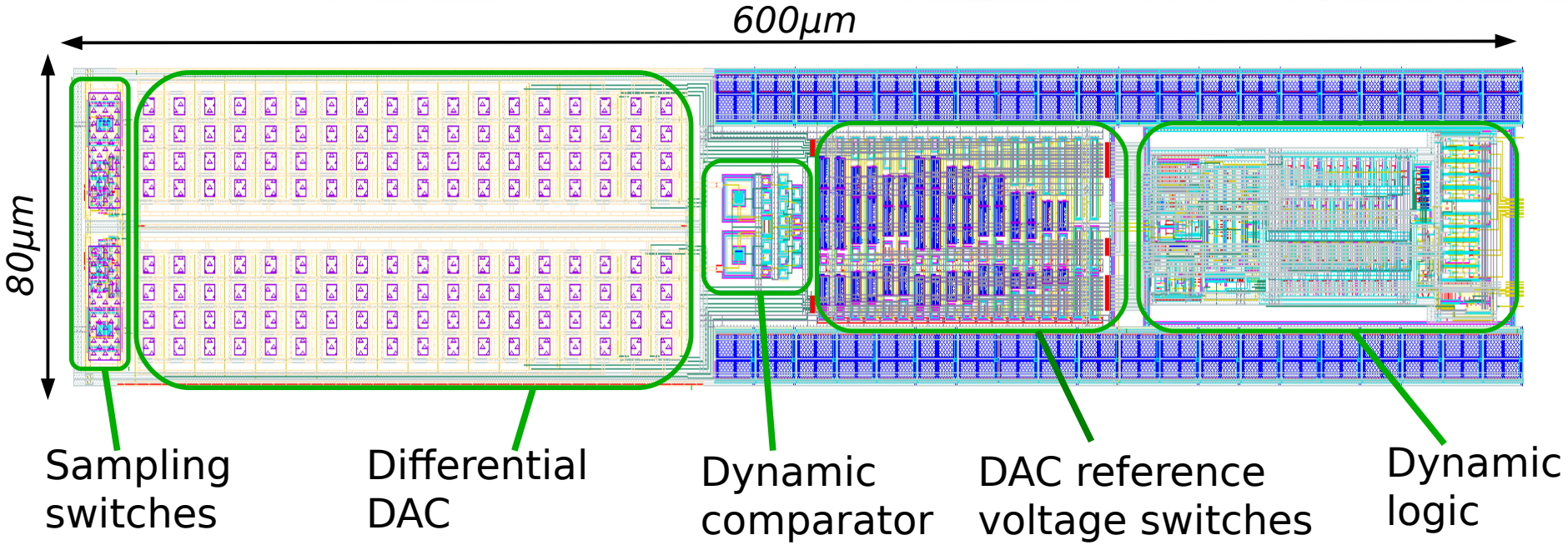




- Making settling time equal for each bit practically impossible
- Constant settling delay for each bit → a lot of time wasted...
- Two versions of variable settling delay implemented

Logic	Bit no.	9	8	7	6	5	4	3	2	1
v1	Group	A [9-8]		B [7-5]			C [4-1]			
	Delay	$t_C+\Delta t_A$ (fixed)		$t_C+\Delta t_B$ (fixed)			Adjustable t_C			
v2	Group	A [9]	B [8-7]		C [6-5]		D [4-1]			
	Delay	Adjustable t_A	Adjustable t_B		Adjustable t_C		Adjustable t_D			

Design of SAR ADC in CMOS 130nm Layout



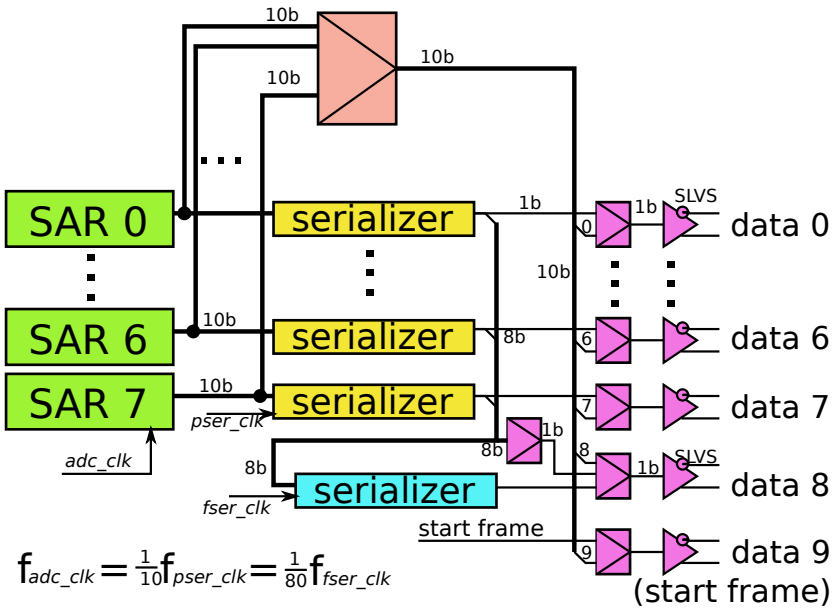
- Pitch of ADC core 80µm ADC core, some more area needed for decoupling

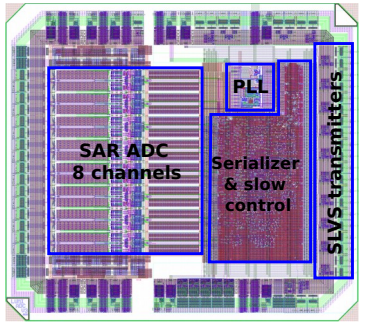
Layout ready for multichannel implementation

Design of SAR ADC in CMOS 130nm
Development of multi-channel ADC

Specifications & main features:

- 8 channels of 10/12-bit SAR ADC
- Versions with MIM and MOM(65nm) caps designed
- Multimode multiplexer/serializer:
  - Single ADC mode: single channnel output
  - Parallel mode: one output per channel (10/12-bit serialization with faster clock)
  - Serial mode: one output per all channels (double serialization: 10/12-bit x 8 channels)
- Additional test modes, with counters/pseudo-random data instead of ADC output, to verify serialization/transmission
- PLL for data serialization
- High speed SLVS interface (~1GHz)





This architecture is mainly to test multi-channel ADC because its data serialization and transmission is not power-optimized.

Sz. Bugiel, R. Dasgupta, M. Firlej, T. Fiutowski, M. Idzik, M. Kopeć, J. Moroń, K. Świentek "Ultra-low power fast multi-channel 10-bit ADC ASIC for readout of particle physics detectors", IEEE TNS vol 63 no 5 pp. 2622-2631 2016

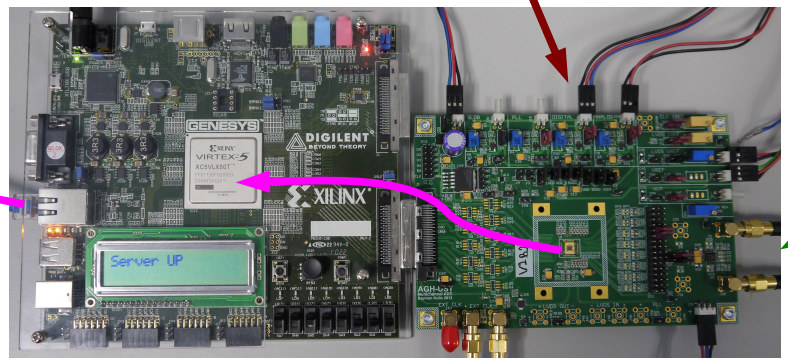
Performance of prototype ADCs in 130nm

Performance of prototype ADCs in 130nm
Measurement setup

DFT and data analysis – custom software

Power supply

Differential function generator – Agilent 81160A

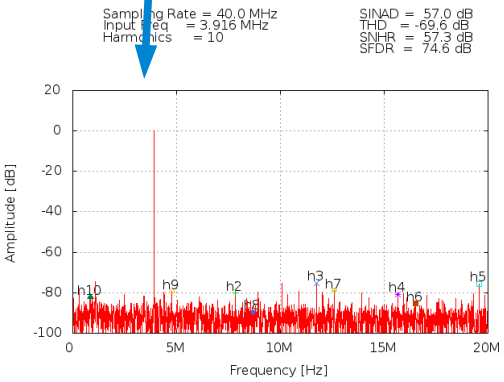


Input sine

Sample clock

Results

Sampled data (**low bitrate**)

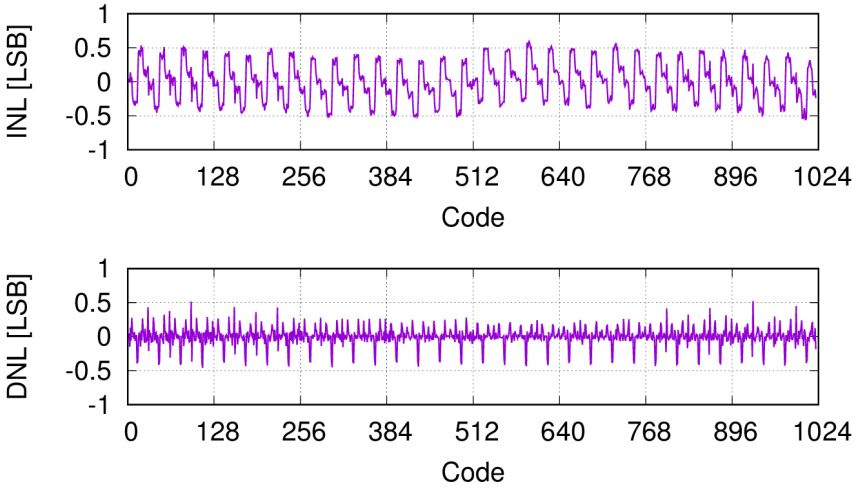


Sampled data (**high bitrate**)

DAQ – receive fast transmission from ADC (up to 500Mb/s), store the assumed amount of data (ie. 4096 samples) and sends to PC via Ethernet for offline analysis.

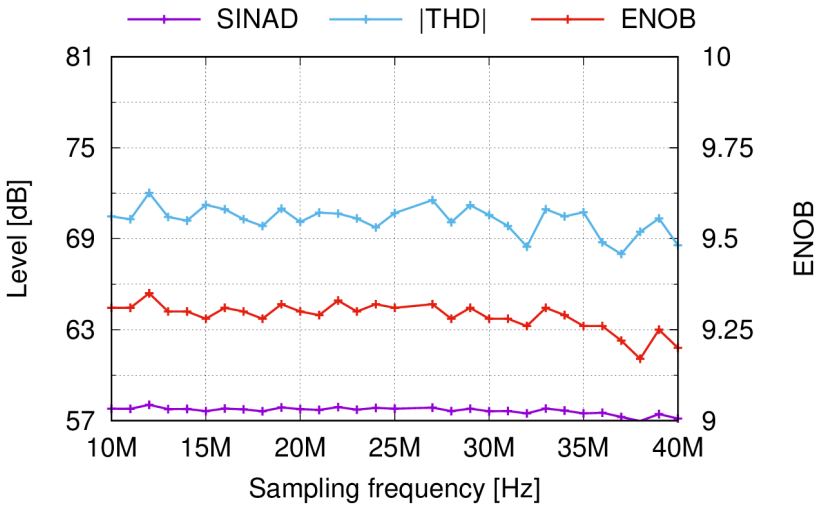
Performance of prototype ADCs in 130nm Process A, with DAC 613

Static measurements



- **INL,DNL≦0.5 LSB**

Dynamic measurements at 0.1Nyquist



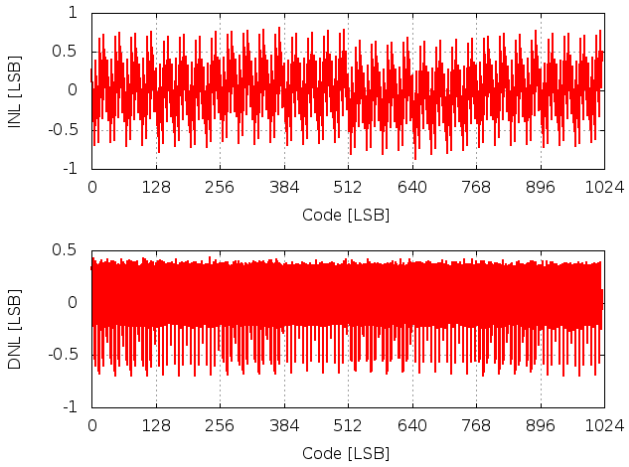
ENOB ~ 9.2-9.3,

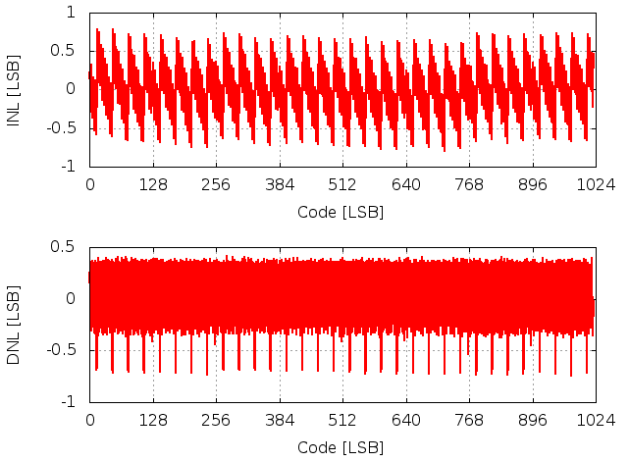
- Max sampling rate ~ **40** Msps
- Power consumption @40MSps 880uW

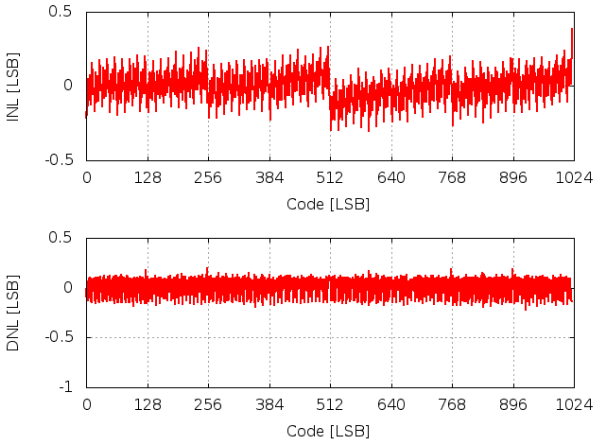
Good performance of ADC in process A

Performance of prototype ADCs in 130nm Process B

Static performance







- **DAC 514 v2**
- -0.70 < **DNL** < 0.44
- -0.87 < **INL** < 0.81
- Static **ENOB** = 9.37
- Sampling rate ≤ 50 MSps

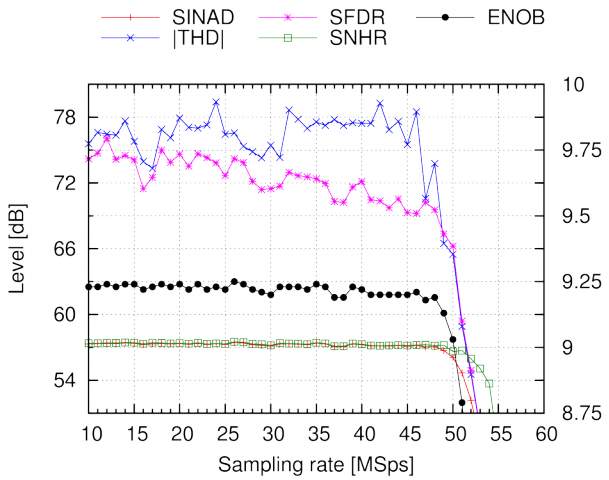
- **DAC 623 v2**
- -0.75 < **DNL** < 0.42
- -0.80 < **INL** < 0.78
- Static **ENOB** = 9.37
- Sampling rate ≤ 50 MSps

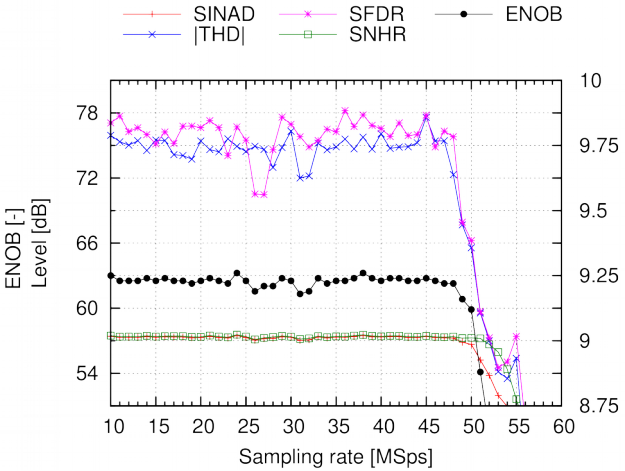
- **DAC 613 v2**
- -0.22 < **DNL** < 0.20
- -0.30 < **INL** < 0.40
- Static **ENOB** = 9.92
- Sampling rate ≤ 55 MSps

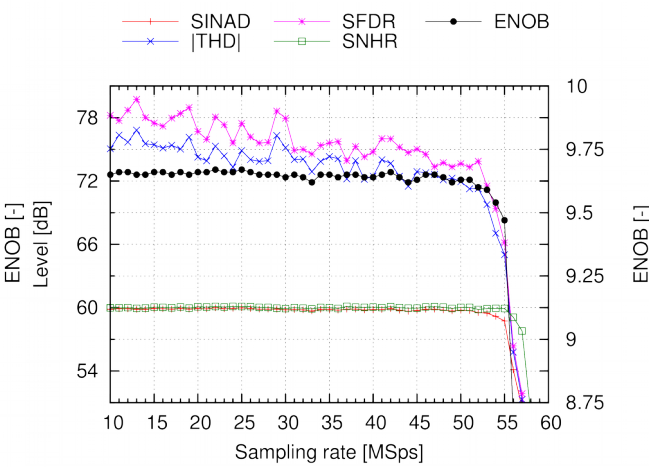
All good but for DAC 613 excellent!

Performance of prototype ADCs in 130nm Process B

Dynamic performance (fin=0.1 Nyquist)







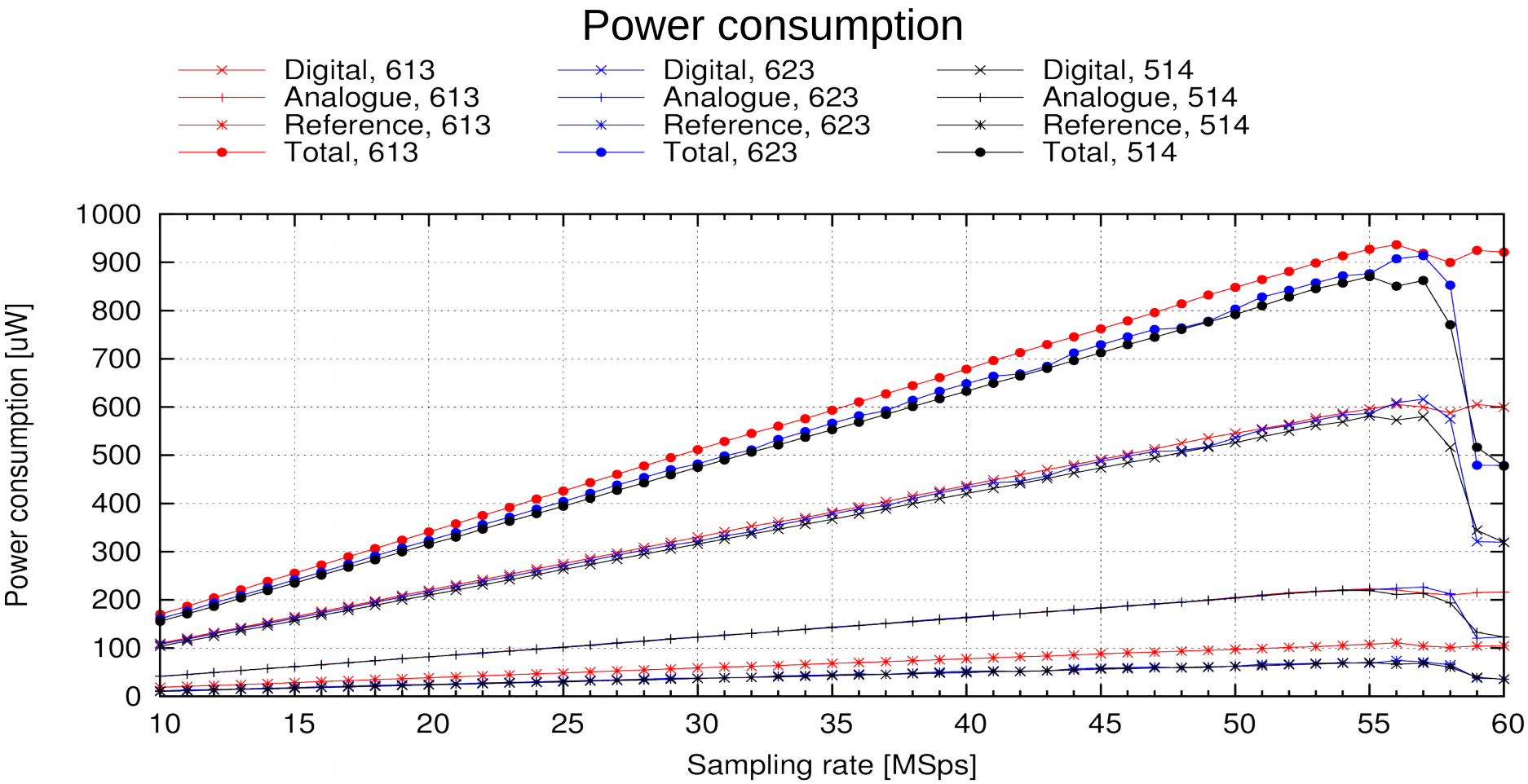
- **DAC 514 v2**
- ENOB ~ **9.2** up to 45 MSps
  > **9.0** up to 50 MSps
- Sampling rate ≤ 50 MSps

- **DAC 623 v2**
- ENOB ~ **9.2** up to 45 MSps
  > **9.0** up to 50 MSps
- Sampling rate ≤ 50 MSps

- **DAC 613 v2**
- ENOB ~ **9.65** up to 50 MSps
  > **9.5** up to 55 MSps
- Sampling rate ~ **55** MSps

All good but for DAC 613 excellent!

Performance of prototype ADCs in 130nm Process B

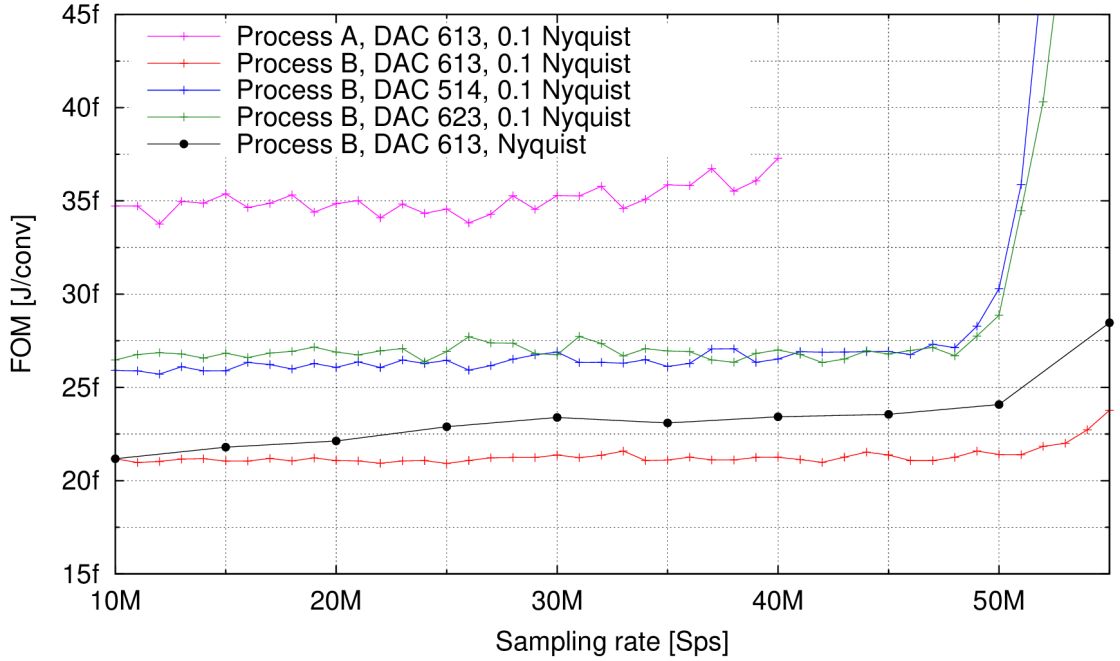


Ultra-low power consumption !

Highest contribution from Digital power

Performance of prototype ADCs in 130nm Figure Of Merit

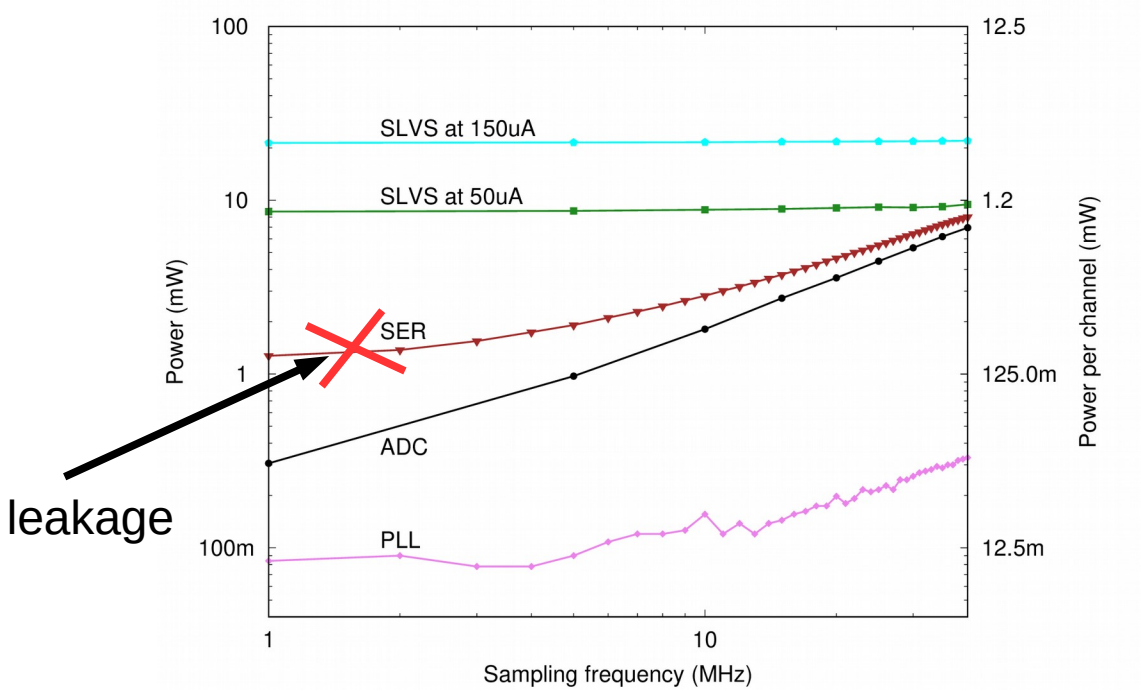
FOMW for process A and process B

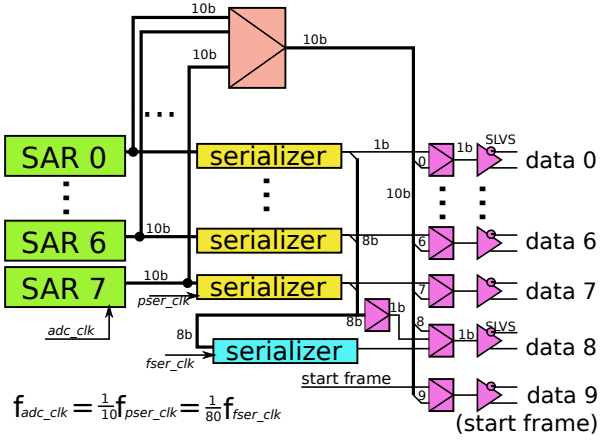


FOMW_hf/FOMW_lf for process B DAC 613 ~ 24/22 fJ/conv.-step @50MSps !

Performance of prototype ADCs in 130nm
Power efficiency of multi-channel ADC

Power consumption of prototype 8-channel ADC ASIC
without optimization of serializer and data transmission

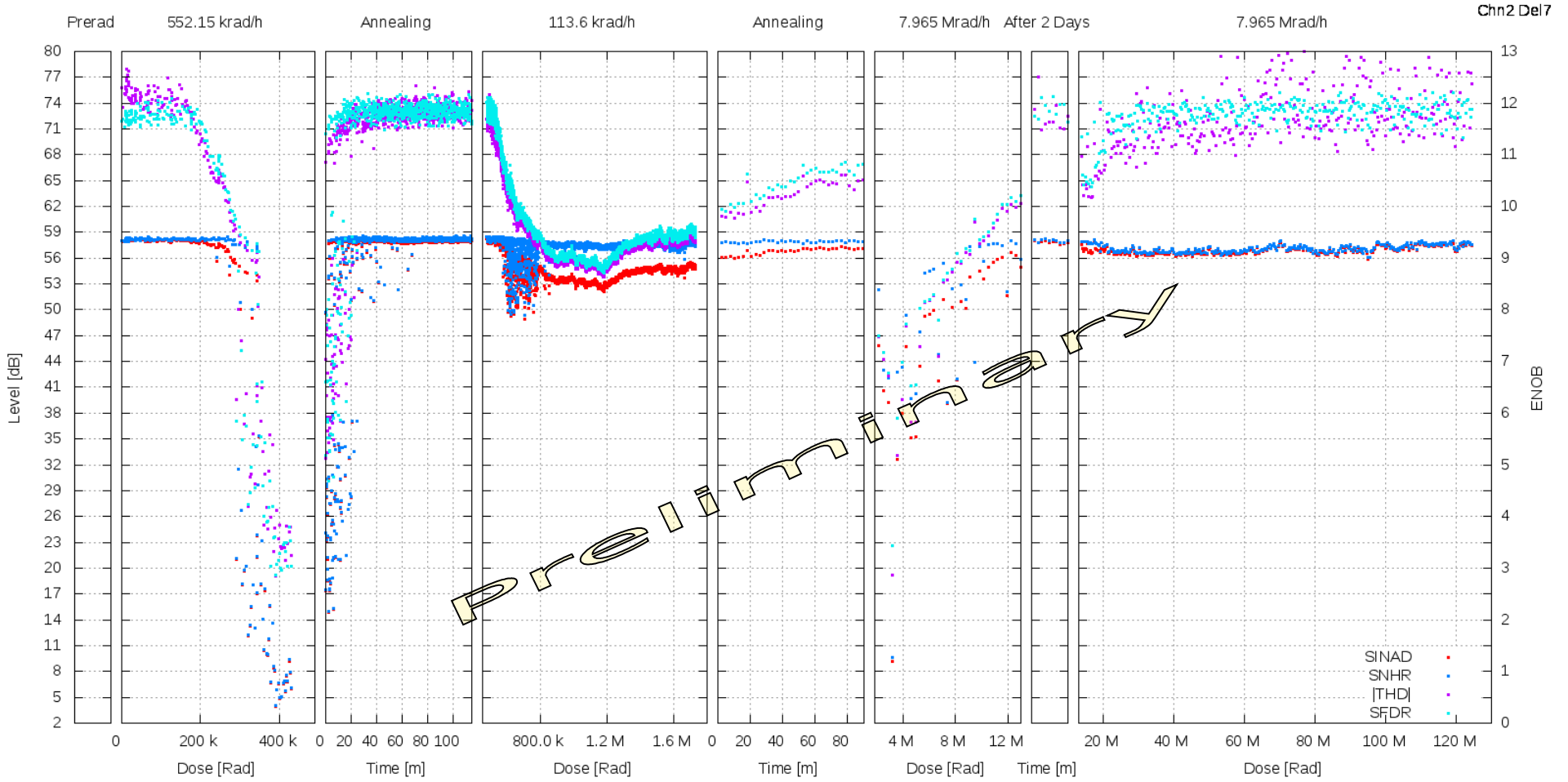




To keep power efficiency power-efficient serializer and transmitter are needed !

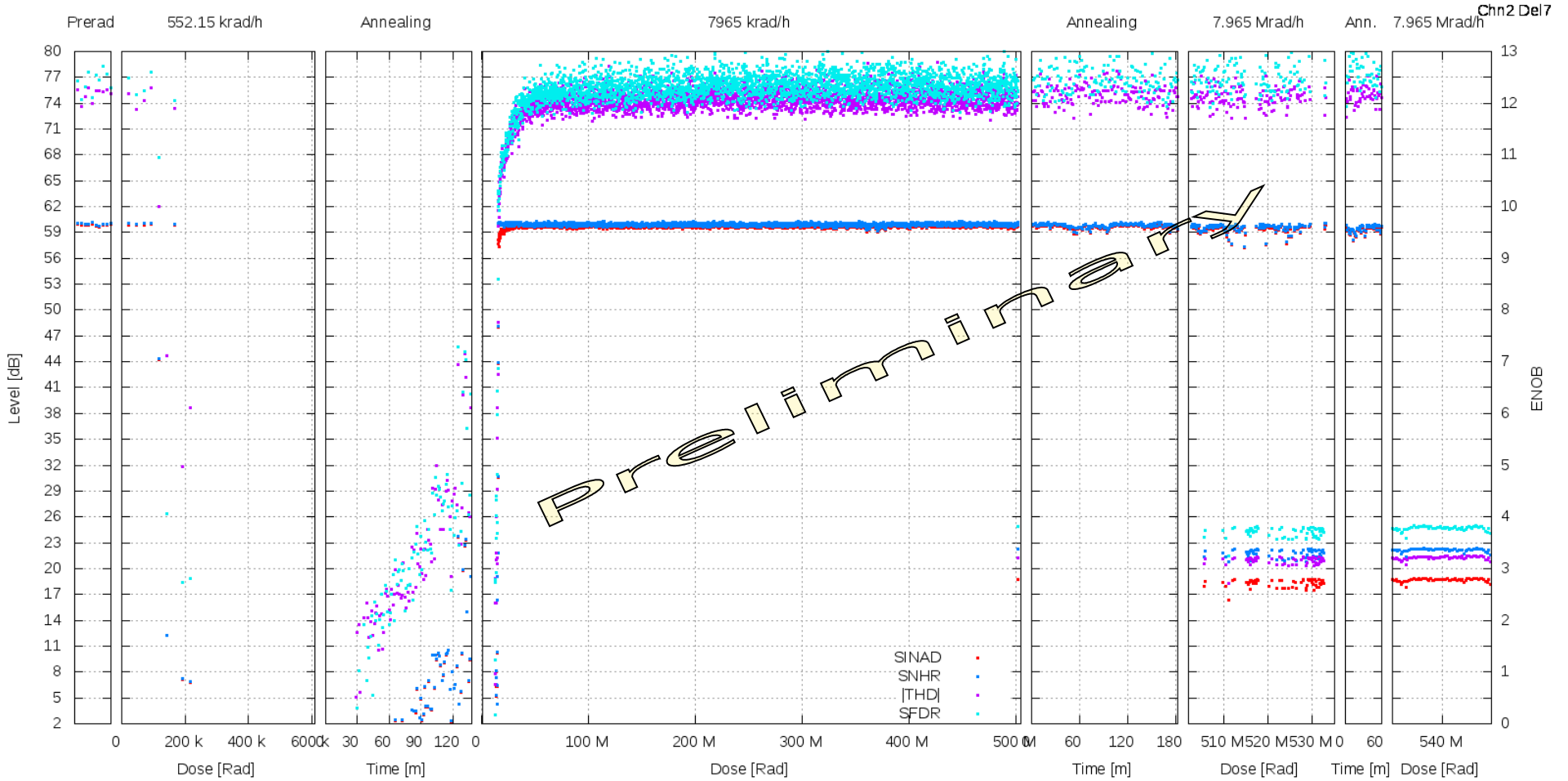
Radiation hardness

Radiation hardness
Process A



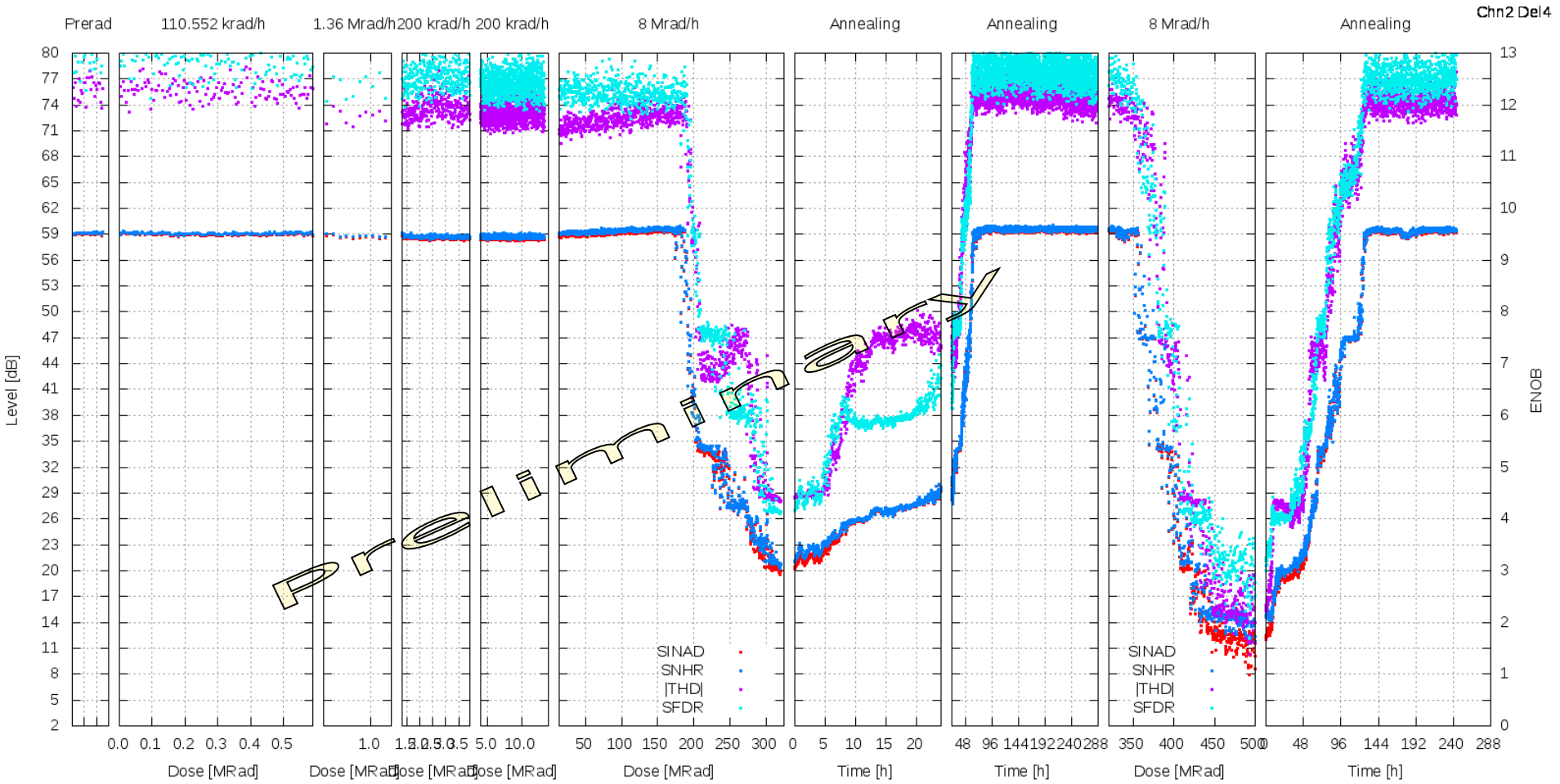
Resolution degrades after few hundred krads but recovers in few days and stays good up to above 100 Mrad

Radiation hardness
Process B, 12 inch



Resolution degrades after few hundred krads but recovers in few days and stays good up to ~500 Mrad

Radiation hardness
Process B, 8 inch wafer



Below ~200 Mrad no effect. Above the resolution start to degrade (at high dose intensity) but recovers with few days of annealing, even above 500 Mrad

Summary

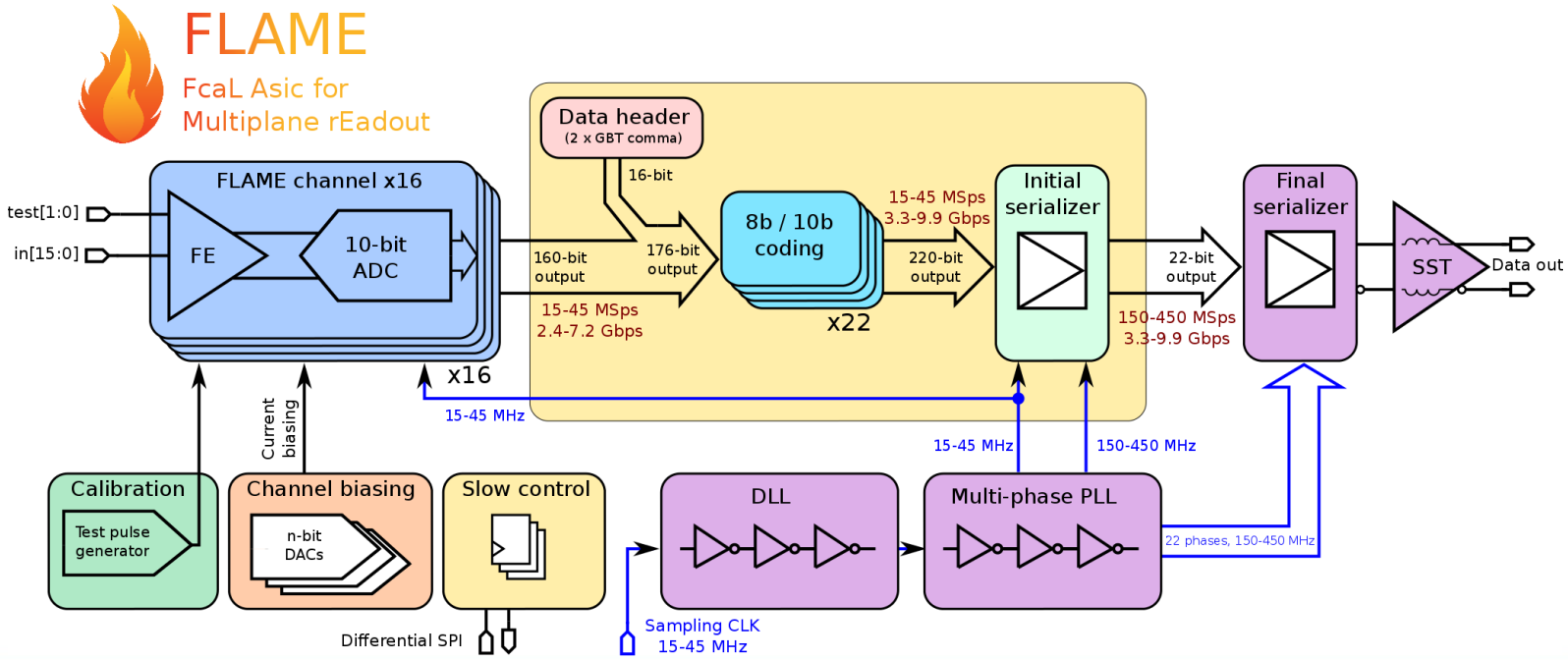
- SAR ADCs have become ultra-low power and quite fast during last decade
- Our recent prototypes in CMOS 130nm show that even at moderately high sampling rate (~40MSps) 10-bit ADC may consume less than typical front-end
- In CMOS 130nm with well optimized analog part the digital power is dominant
- I have not discussed here 65nm designs because various prototypes of 10/12 bit SAR ADCs with MIMCAP and MOM capacitive DACs are still waiting to be tested, but we hope to get even better results than with 130nm
- With present ultra-low power SAR ADC the main power bottleneck is in serialization and data transmission

Thank you for attention

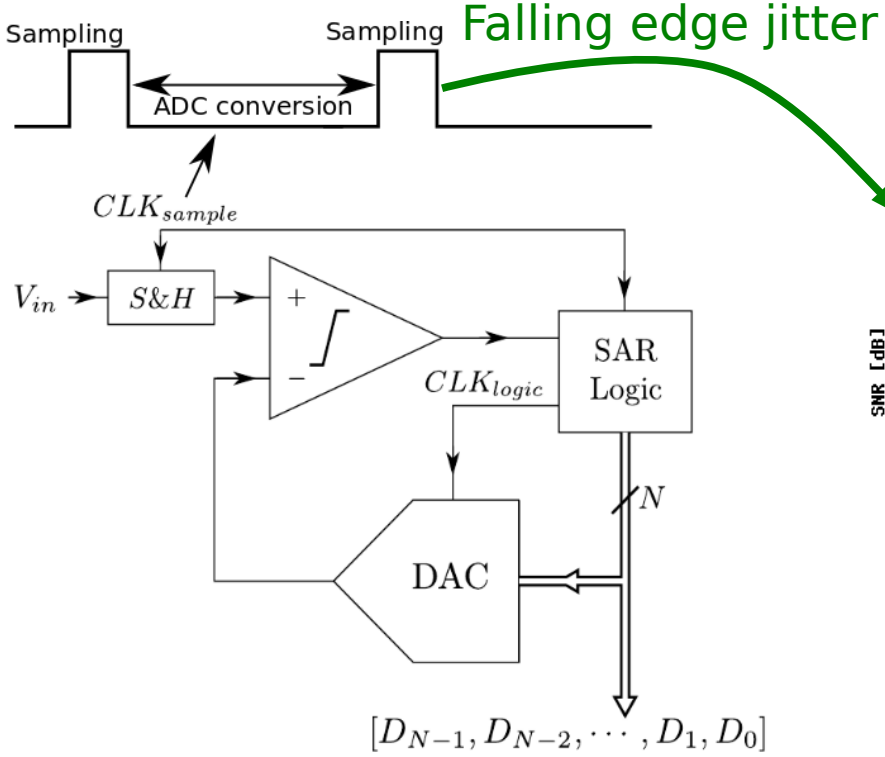
Backup

Example applications ? (HGCAL, LPGBT, VFAT)
FLAME – dedicated readout ASIC for ILC in TSMC CMOS 130

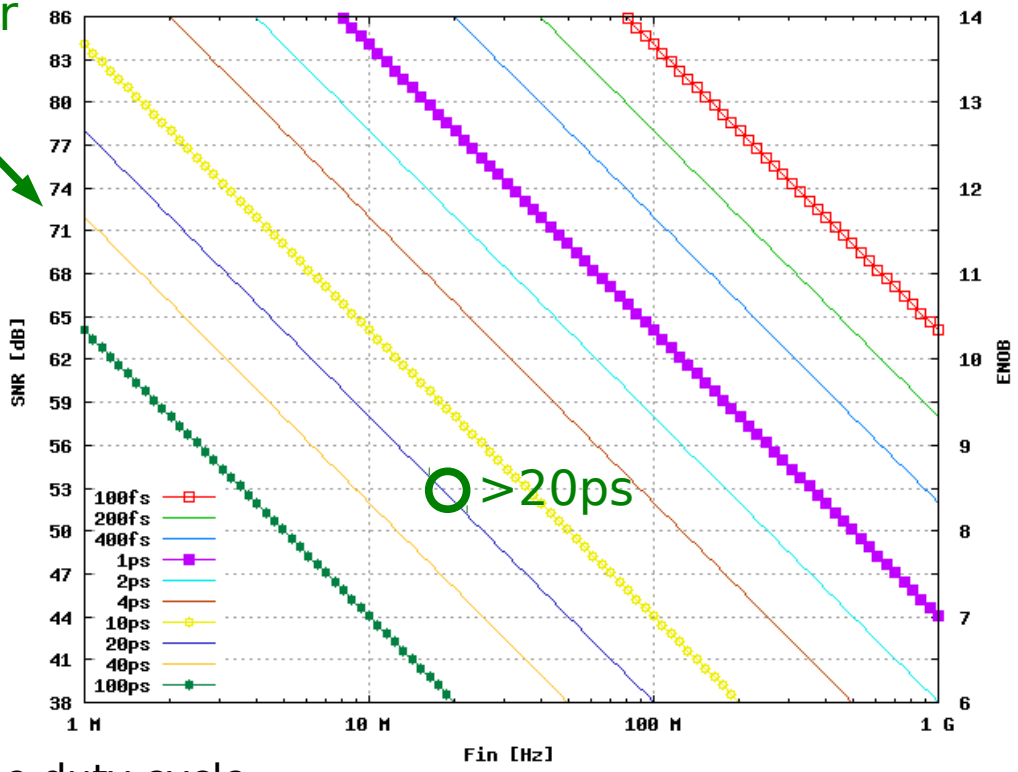
- For **very compact** calorimeter we need an ultra-low power, SoC type (all functionalities on chip) readout ASIC
- FLAME: 16(changed to 32) -channel ultra-low power readout ASIC in CMOS 130 nm, FE&ADC in ech channel, fast serialization and data transmission, all functionalities in single ASIC



Sampling clock jitter



Falling edge jitter

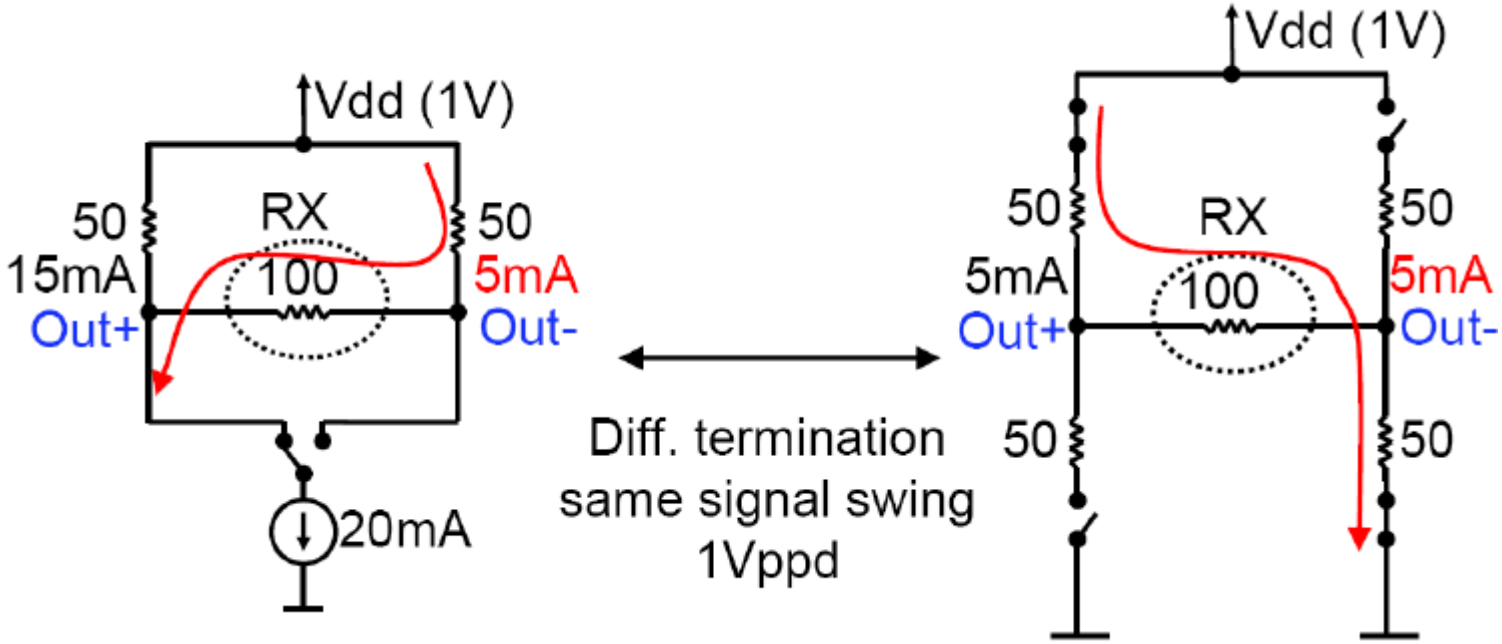


- Sampling time steered by triggering pulse duty cycle
- Non-50% duty cycle triggering pulse generated by internal circuit → introducing jitter – although post-layout simulations showed very small jitter, in reality it was larger than expected → it caused worsening of the ENOB

\+ Temporary solution – use 50% duty cycle external clock (low jitter) as triggering pulse

– Max. ADC sampling frequency dropped below 25 MHz

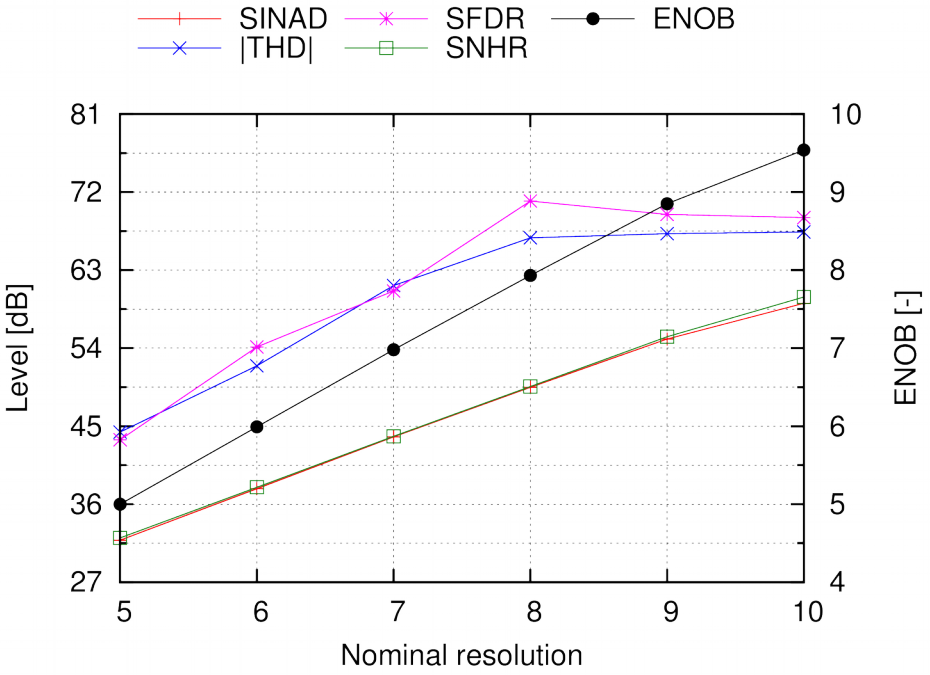
Drivers for higher speed

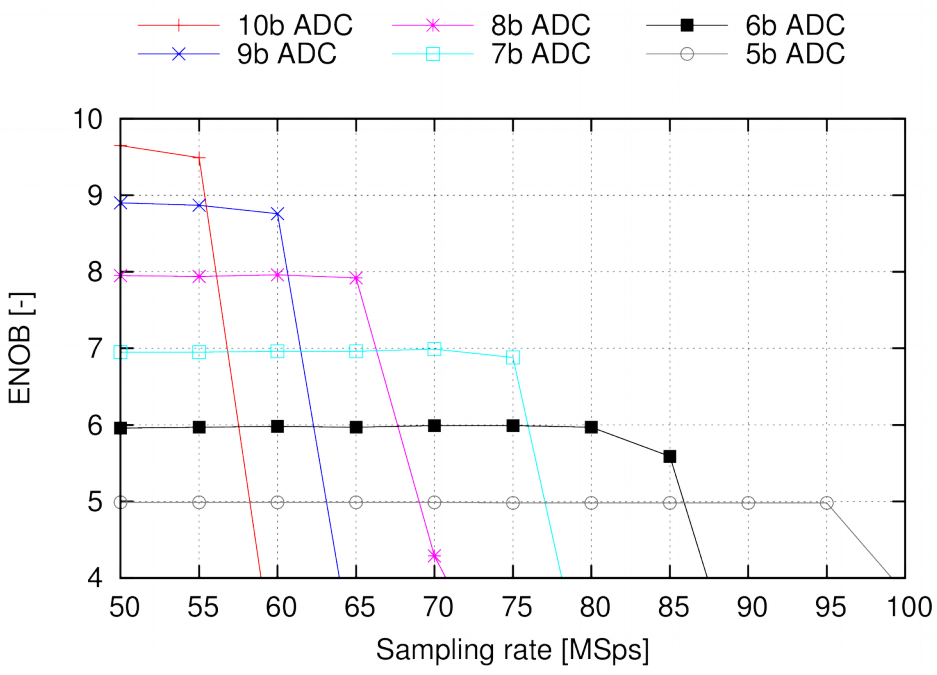


CML - Current mode logic
Total current 20 mA

SST - Source-Series Terminated
Total current 5 mA

Performance of SAR ADCs in 130nm
Programmable resolution



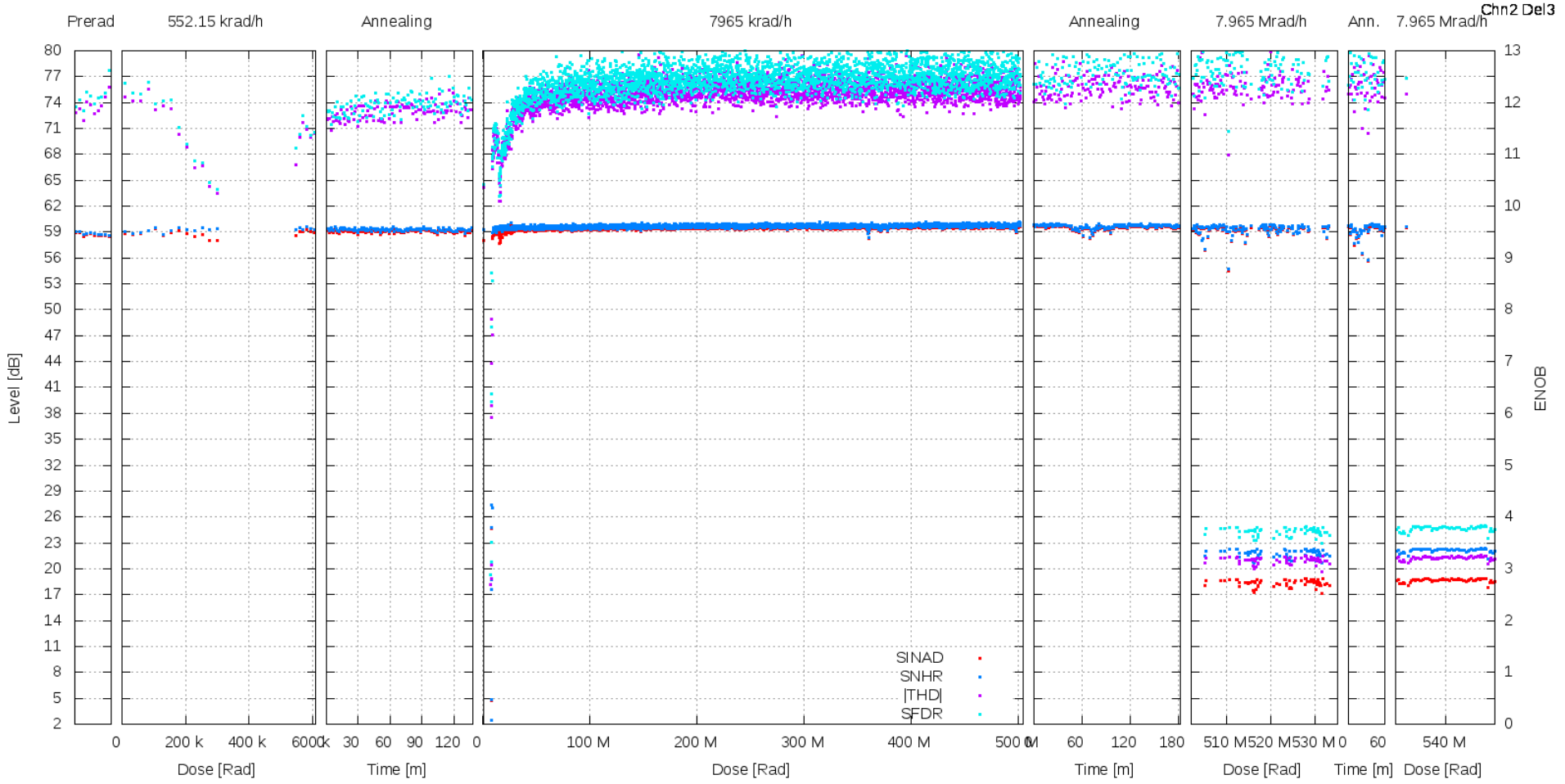


- **DAC 613 v2 – programmable resolution**

- For resolution below nominal dynamic metrics are almost ideal
- For 6-bit ENOB=**6.0** for 0.1 Nyquist of input frequency

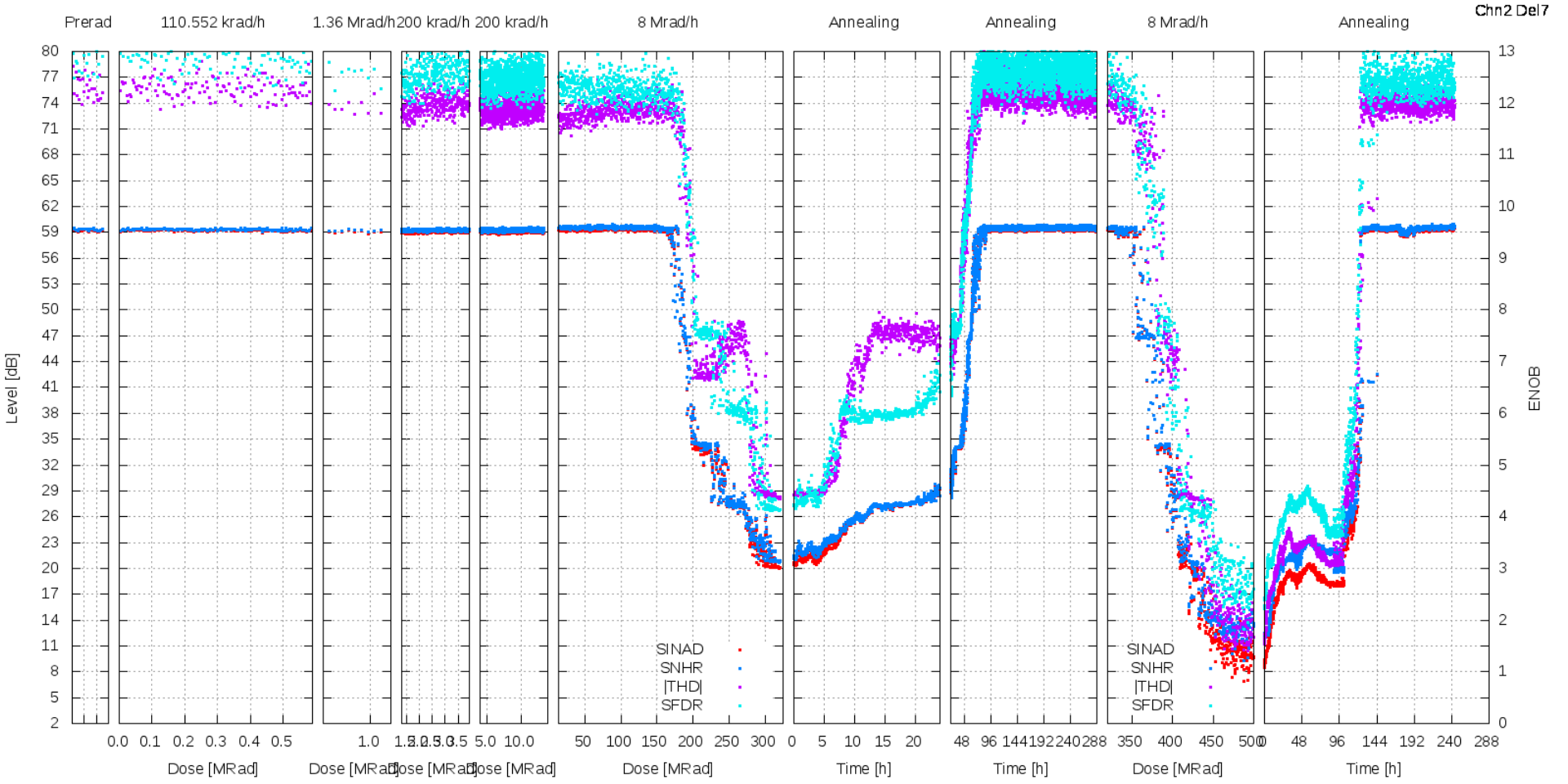
- Maximal sampling rate increases with reduced resolution
- <**85** MSps for 6-bit

Radiation hardness
Process B, 12 inch ?

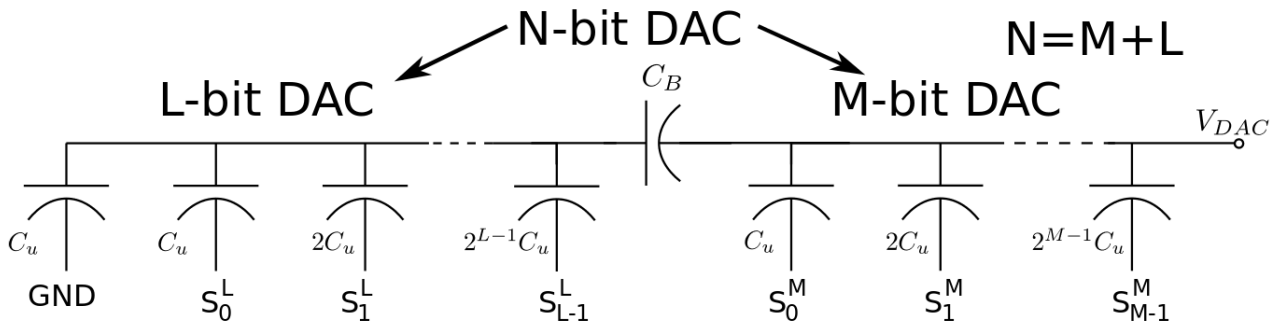


Resolution degrades after few hundred krads but recovers in few days and stays good up to ~500 Mrad

Radiation hardness
Process B, 8 inch ?



Design of SAR ADC in CMOS 130nm
Split of the DAC



- N-bit DAC splitted into two DACs connected via series unit capacitor

$$C_u > \frac{36}{2\sqrt{2}} 2^{2L}\left(2^M - 1\right) K_\sigma^2 K_C \qquad K_\sigma \sim 1.44\%\,\mu m \qquad K_C = 1.55\,\frac{fF}{\mu m^2}$$

M	L	C_u [fF]	No. of C_u	C_{in} [pF]	C_{total} [pF]
9	0	2.09 → 26.2	512	13.41	13.41
8	1	4.17 → 26.2	257	6.71	6.73
7	2	8.31 → 26.2	131	3.35	3.43
6	**3**	**16.49 → 26.2**	**71**	**1.68**	**1.86**
5	4	32.47	47	1.04	1.53
5	**4**	**32.47 → 26.2**	**47**	**0.84**	**1.23**

- C_u – minimal unit capacitance ensuring 3σ of DNL < 0.5 LSB
- Technology limit – 26.2fF
- For 514 split with reduced C_u 3σ of DNL < 1.5 LSB expected

D. Zhang, Design of Ultra-Low-Power Analog-to-Digital Converters. Linköping University, 2012