ADCs Approaching 100GSamples/s

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Outlines

- Application of high-speed high-sampling-rate ADCs
- The challenges and design techniques in high-speed ADC design
- Examples of State-of-the-art high-speed ADCs
- Conclusions

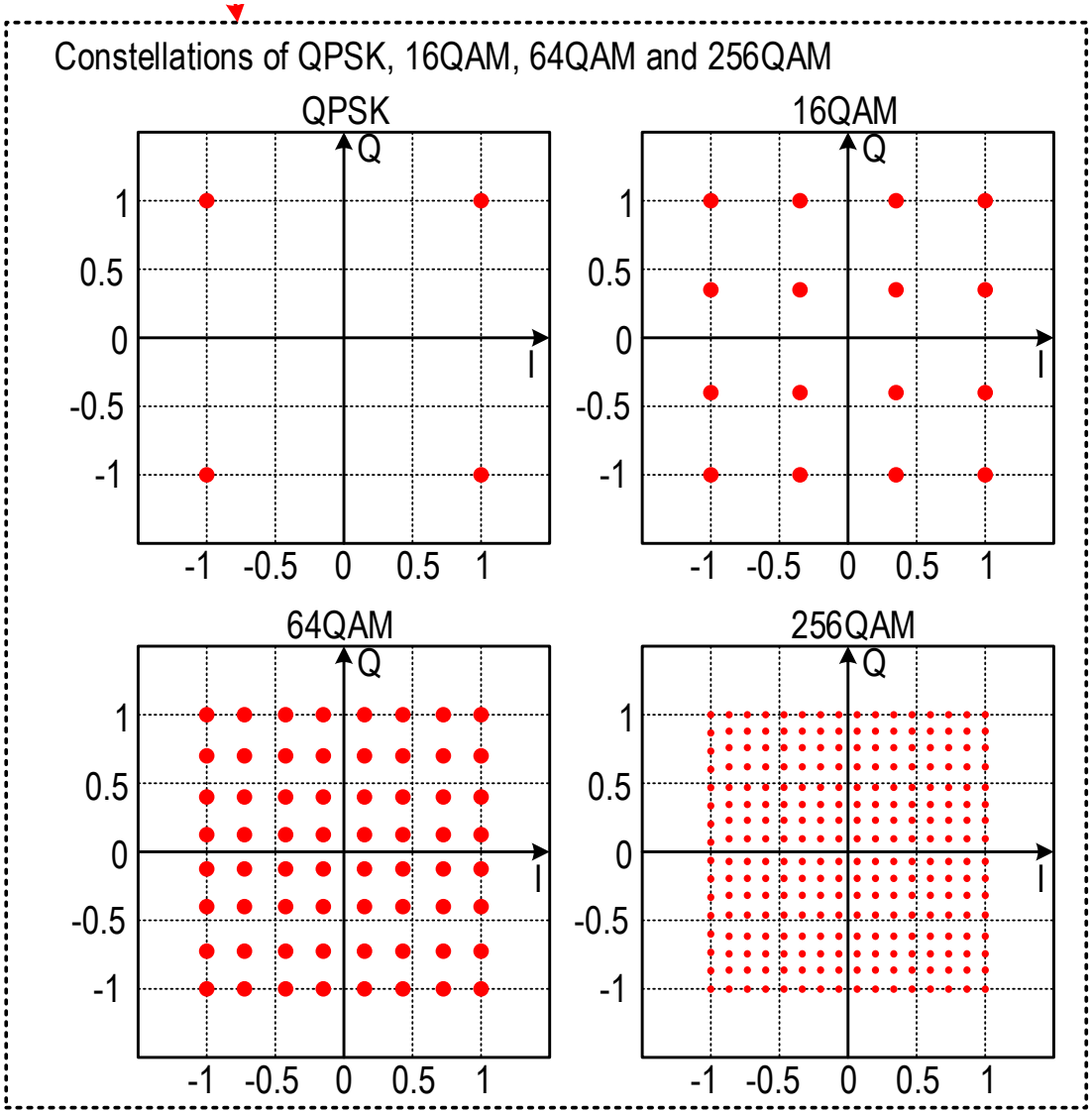
The Demand for High-Speed ADCs

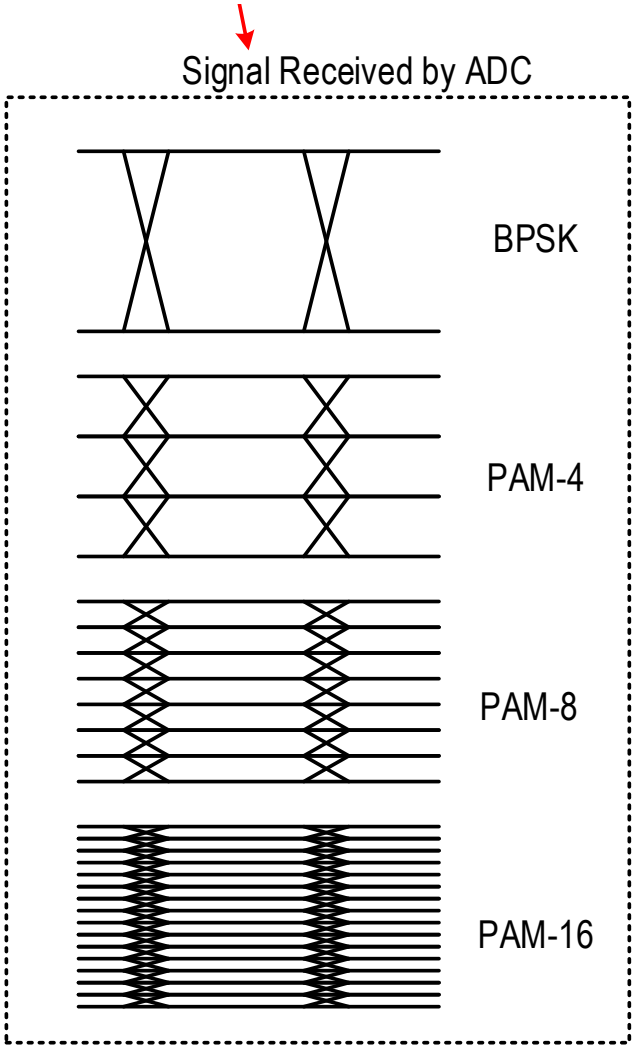
- Applications
  - High-bandwidth oscilloscopes
  - 100/400Gb/s optical and backplane data links
  - 5G Wireless communications
  - Phased array systems for RADAR
  - HEP experiments

- High sampling rate: GS/s to 100 GS/s
  - Double (Nyquist rate) sampling (sampling rate being twice the bandwidth) allows for robust CDR, and equalization and spectrum engineering in DSP
- High bandwidth to accommodate high symbol rate
- ENOB: > 6 bit, SNDR > 37.8 dB
- Power consumption manageable

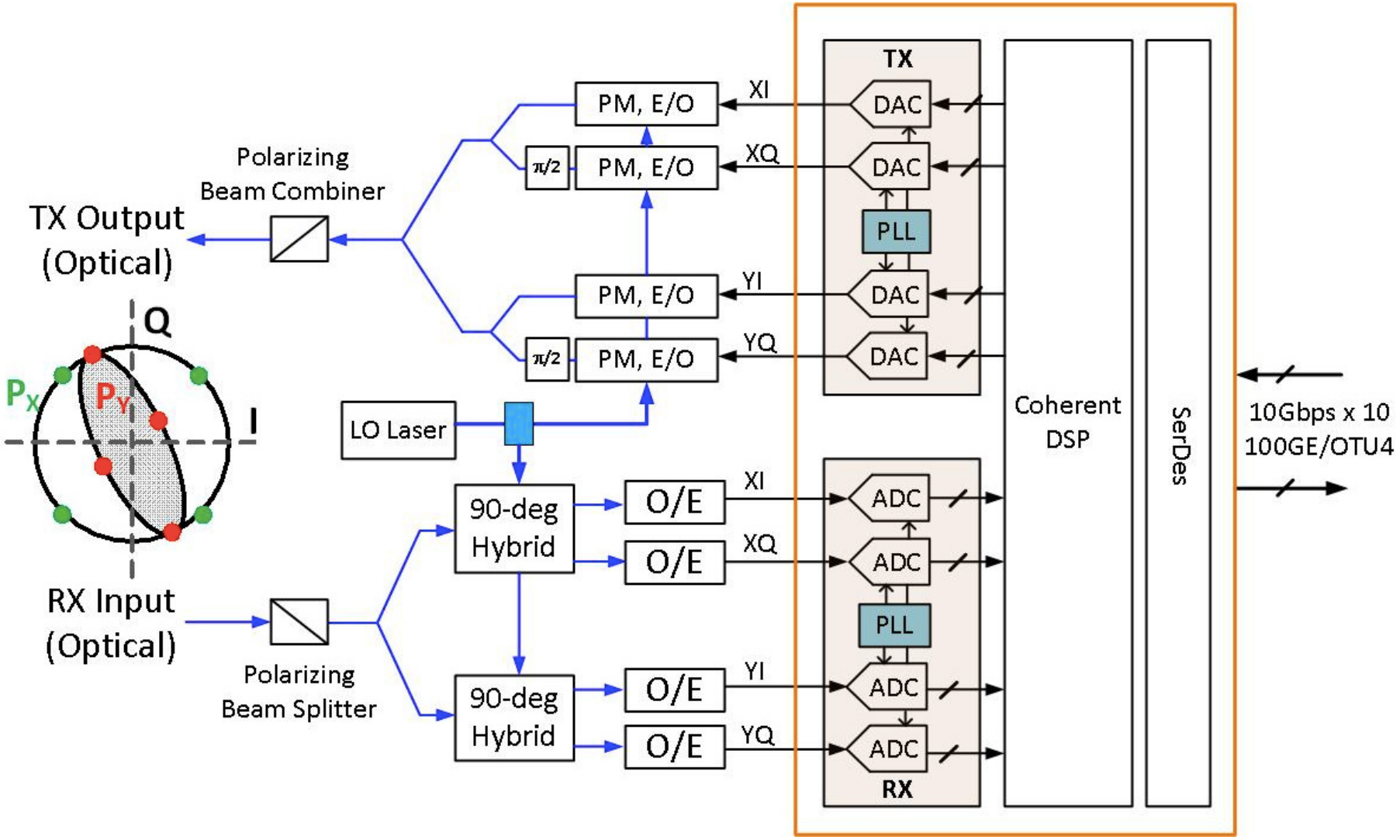
$$\text{ENOB}=\frac{\text{SNDR(dB)-1.76dB}}{6.02\text{dB}}$$

PAM or QAM-based High-Speed Data Links





ADC/DAC Based Coherent Optical Transceiver



[Image from Broadcom, ISSCC 2017]

Design Specifications and Challenges

Analog-to-Digital Converter Requirements for 112 Gb/s Transmission

Constellation	ADC bandwidth	ADC sampling rate	ADC Effective number of bits (ENOB)
4-QAM	25GHz	50 Gsamples/s	> 3.8
16-QAM	12.5GHz	25 Gsamples/s	> 4.9
64-QAM	8.33 GHz	16.67 Gsamples/s	> 5.7
256-QAM	6.25 GHz	12.5 Gsamples/s	> 7.0

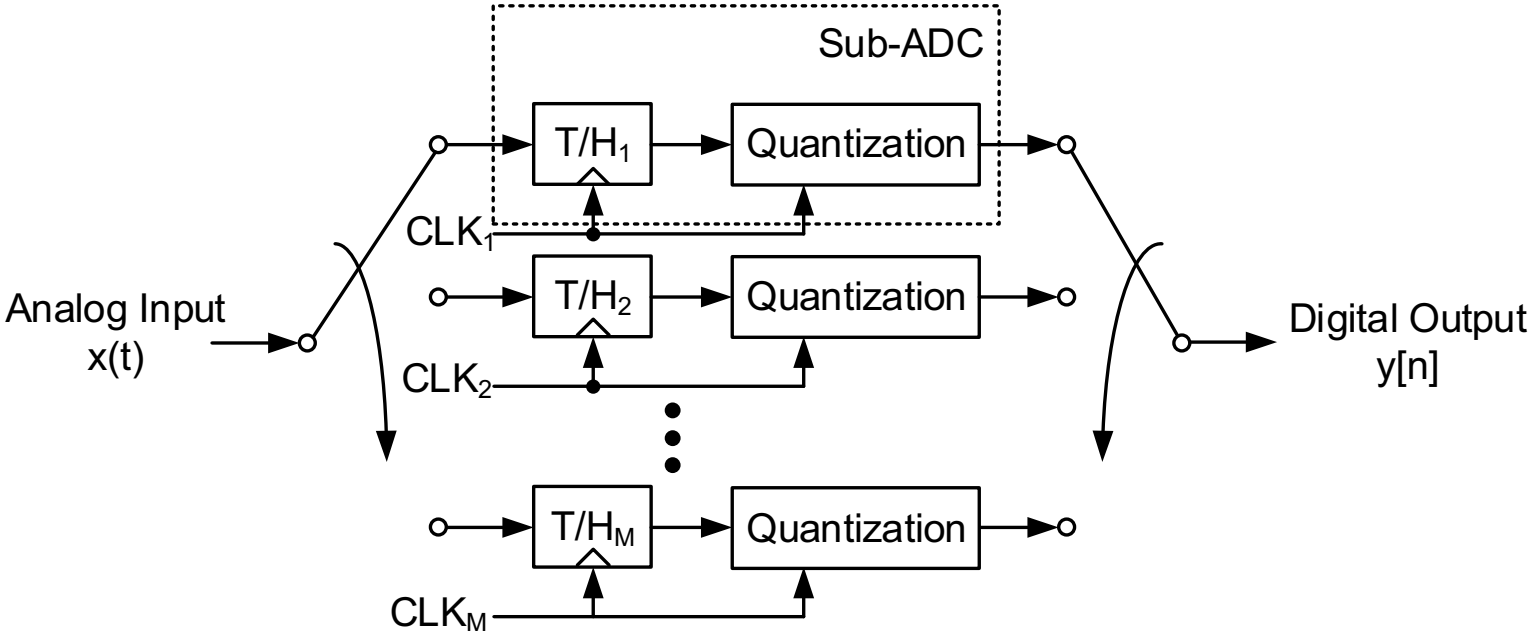
Analog-to-Digital Converter Requirements for 448 Gb/s Transmission

Constellation	ADC bandwidth	ADC sampling rate	ADC Effective number of bits (ENOB)
4-QAM	112GHz	224 Gsamples/s	> 3.8
16-QAM	56GHz	112 Gsamples/s	> 4.9
64-QAM	37 GHz	74 Gsamples/s	> 5.7
256-QAM	28 GHz	56 Gsamples/s	> 7.0

[Timo Pfau, Journal of Lightwave Technology, 2009]

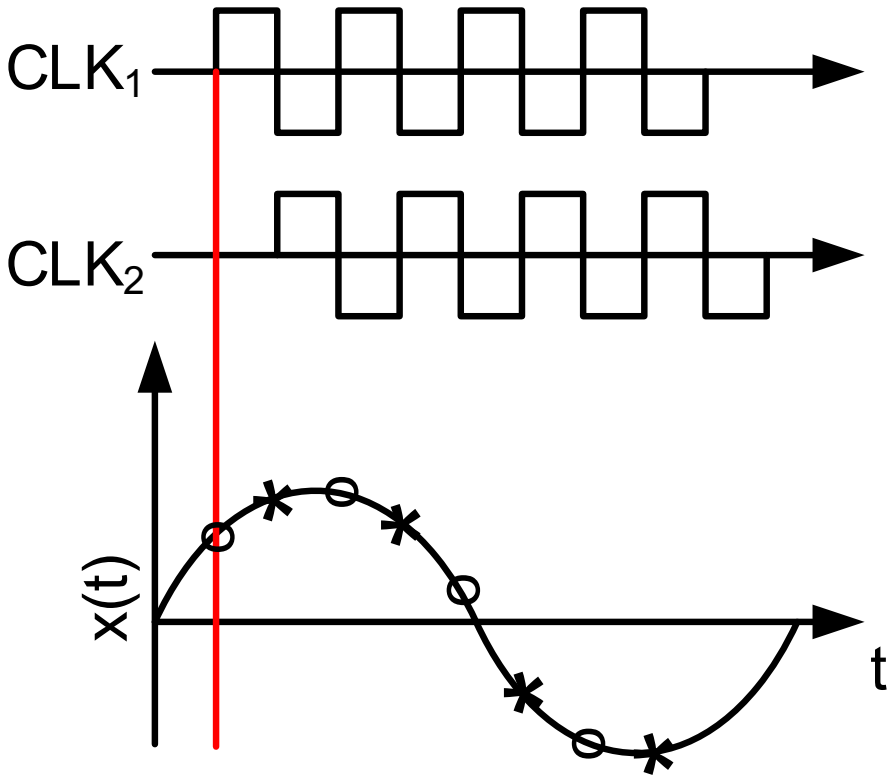
How to Achieve such a High Sampling Rate

- Increasing f_s in a single ADC will hit a technological wall and make the power dissipation prohibitively high
- Time-interleaved ADC is an effective method to increase sampling frequency f_s.
  - Cycle through a set of M identical sub-ADCs
  - Aggregate sample-rate is M times the sample-rate of the individual sub-ADCs



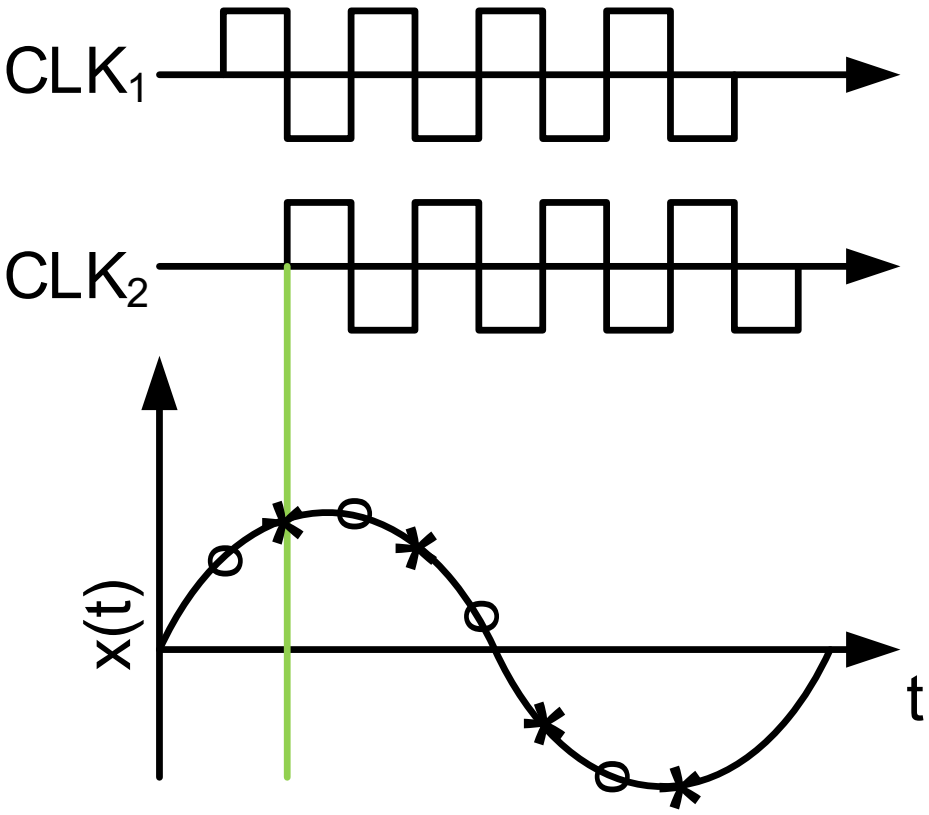
Introduction of Time-Interleaved ADCs

- Scenario of first sub-ADC sampling the signal



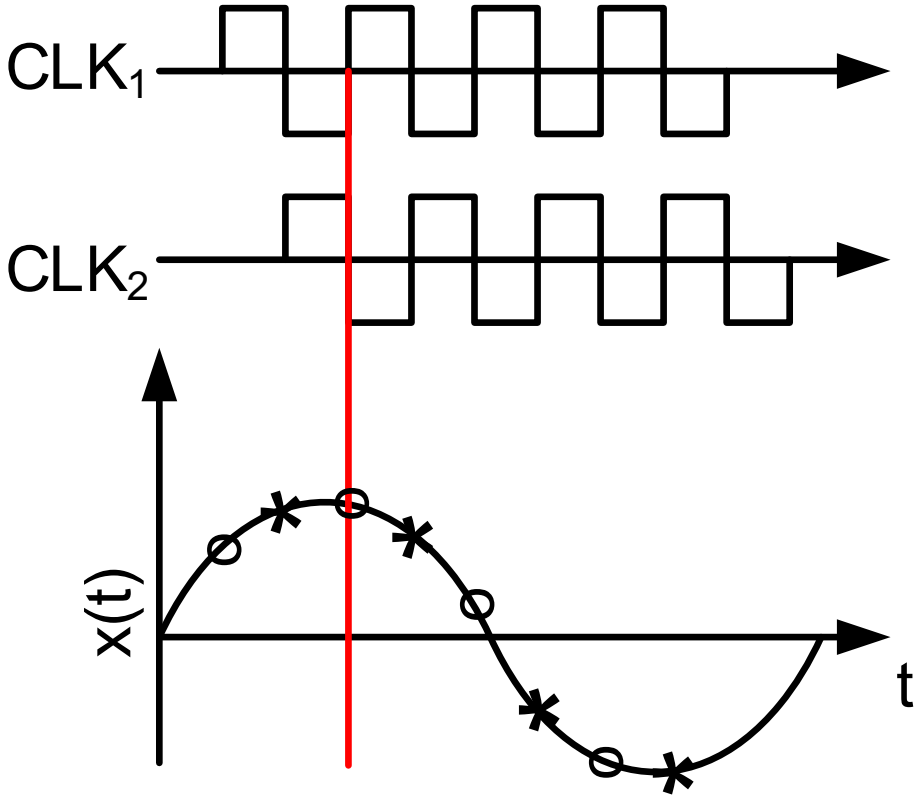
Introduction of Time-Interleaved ADCs

- Scenario of second sub-ADC sampling the signal



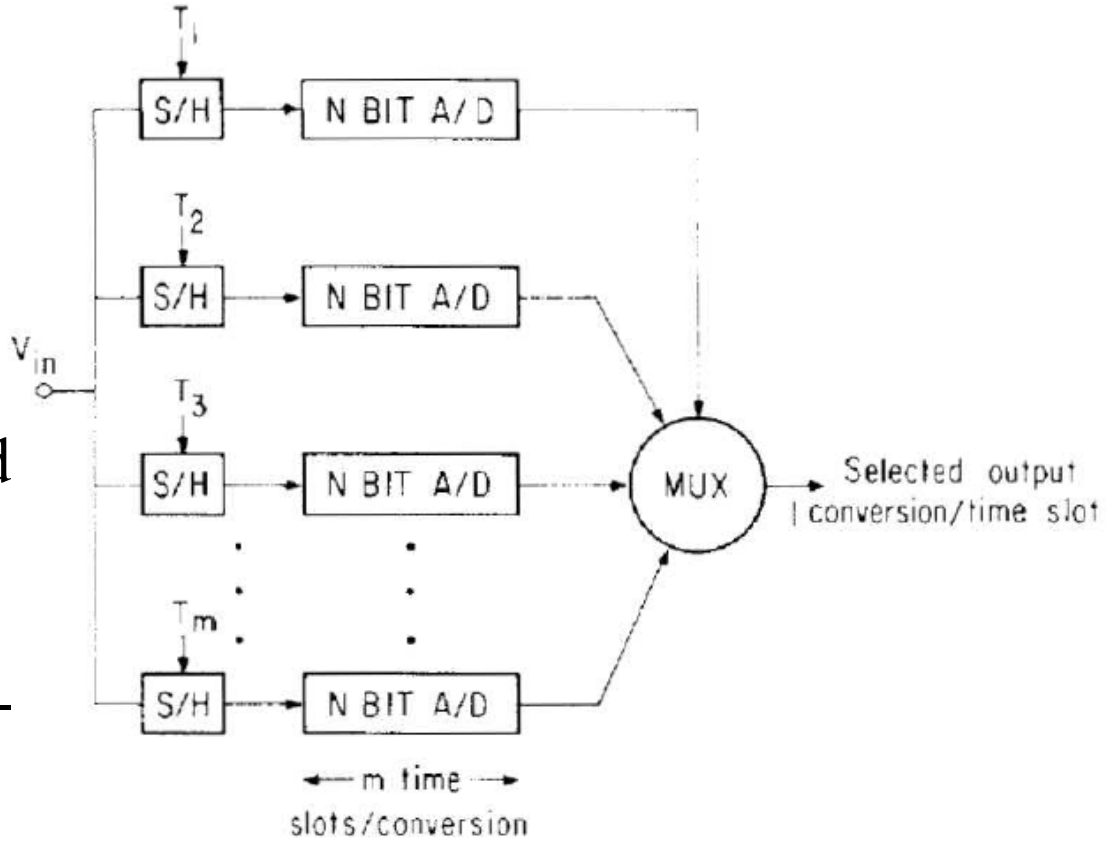
Introduction of Time-Interleaved ADCs

- And again, first sub-ADC samples the signal



Back in 1980s…

- William Black, Ph.D. Dissertation, "High-Speed CMOS A/D Conversion Techniques"
- Published time-interleaved conversion array
- This technique was for a 7-bit 2.5MHz ADC

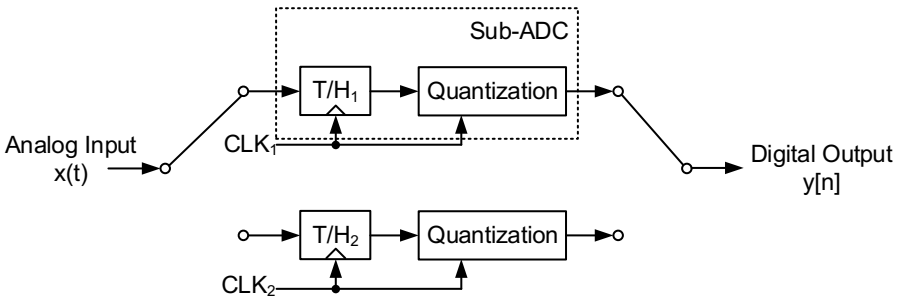


30 Years Later

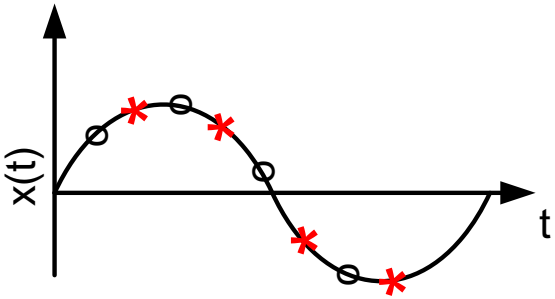
- Time-interleaved ADCs is still an active research area

- High-sampling rate ADCs
  - Agilent 2003: 80-way interleaved 20 GS/s
  - Fujitsu 2009: 4-way interleaved 56 GS/s
  - Nortel 2010: 16-way interleaved 40 GS/s
  - IBM 2014: 64-way interleaved 90 GS/s
  - Broadcom 2017, 64-way interleaved 4 x 64GS/s
  - ….

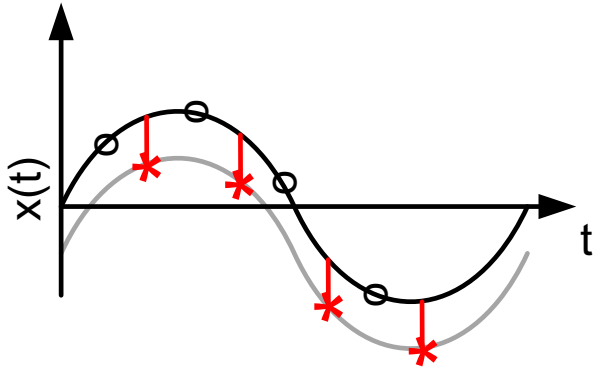
Inter-Channel Mismatches



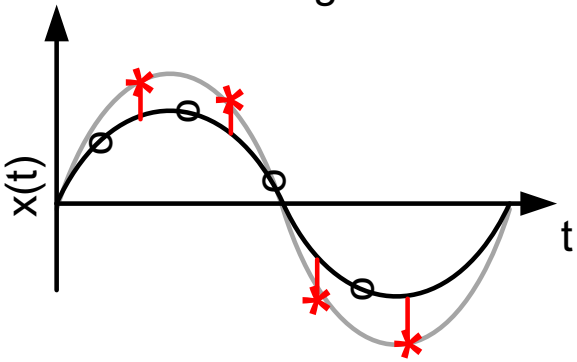
Ideal



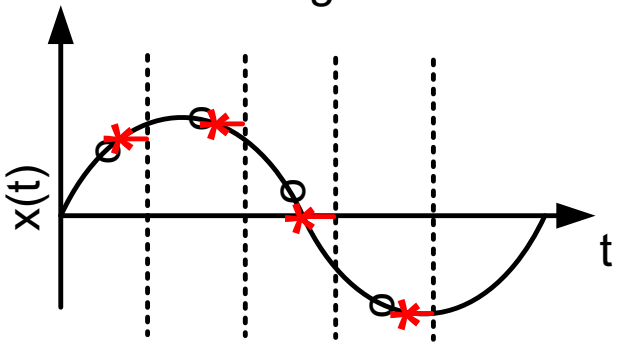
Inter-channel offset mismatch



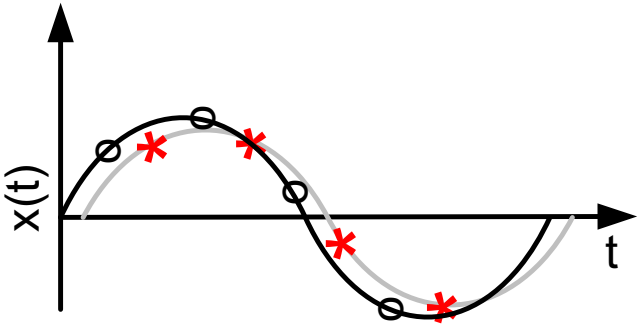
Inter-channel gain mismatch



Inter-channel timing skew mismatch



Inter-channel BW mismatch

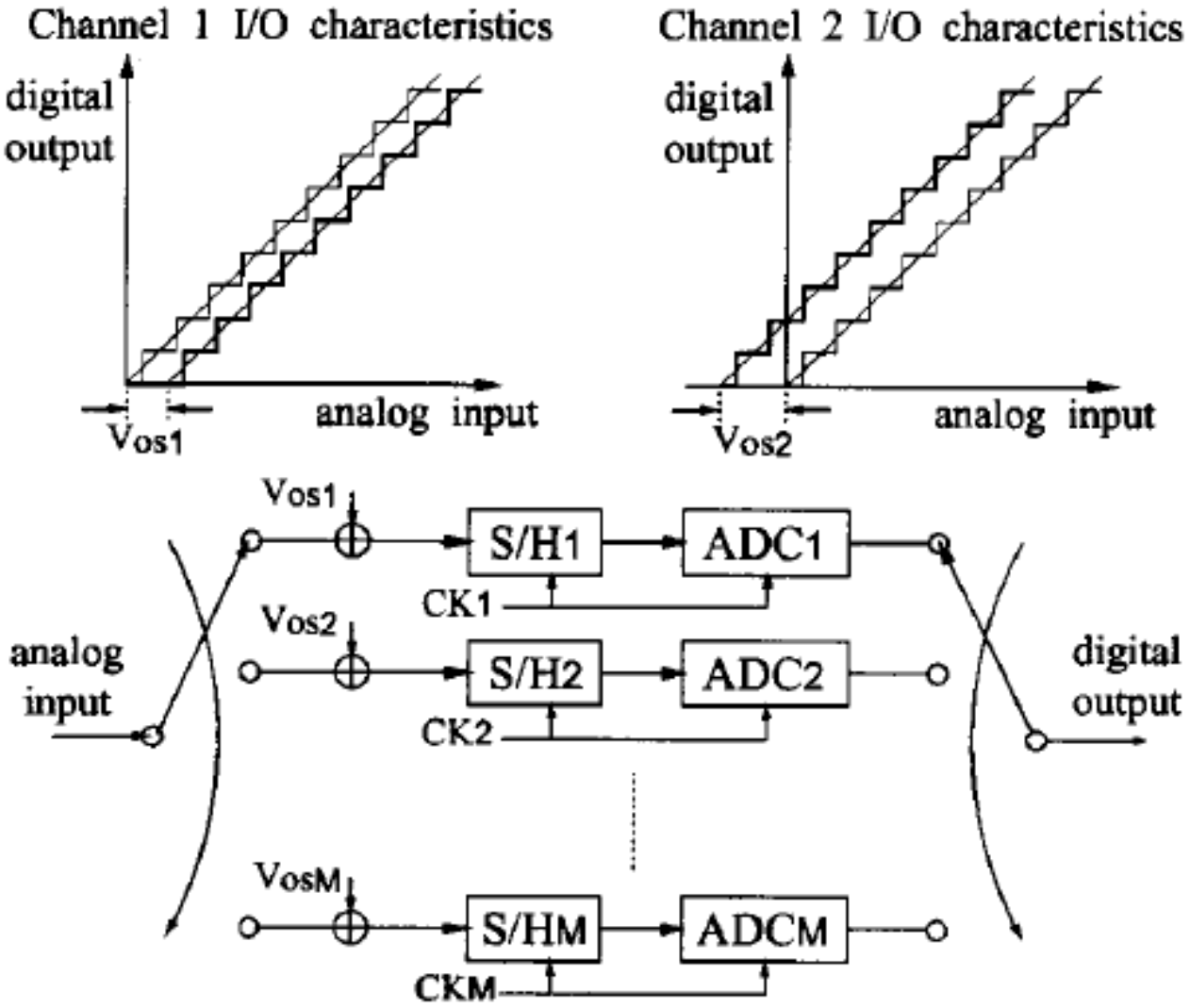


Challenges in High-Speed ADC Design

- Inter-channel mismatches calibration
  - Gain, Offset, Timing skew, Bandwidth, (nonlinearity)
- High-speed front-end Track/Hold (T/H)
- Low-power and high-speed of sub-ADC channels

- **Inter-channel Mismatches**

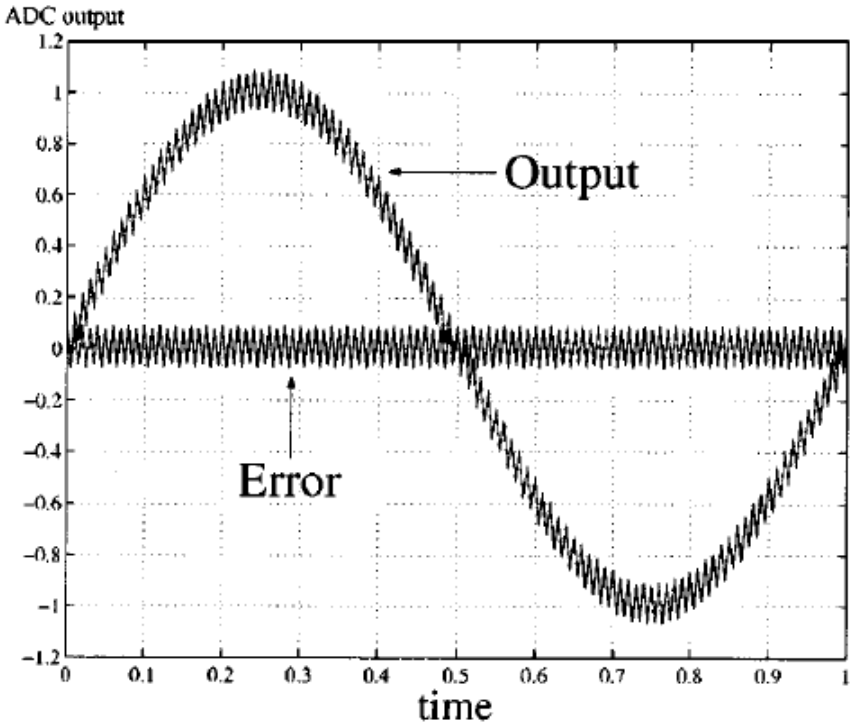
Offset Mismatch Effect

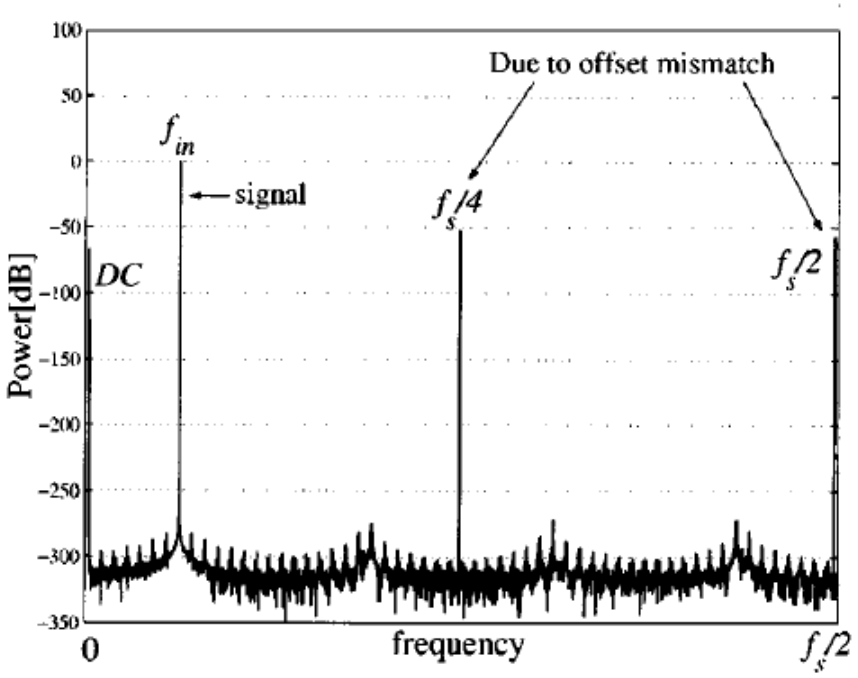


[Kurosawa, TCAS-I 2001]

M Channels interleaved together

Offset Mismatch Effect





Spurious tone frequencies:

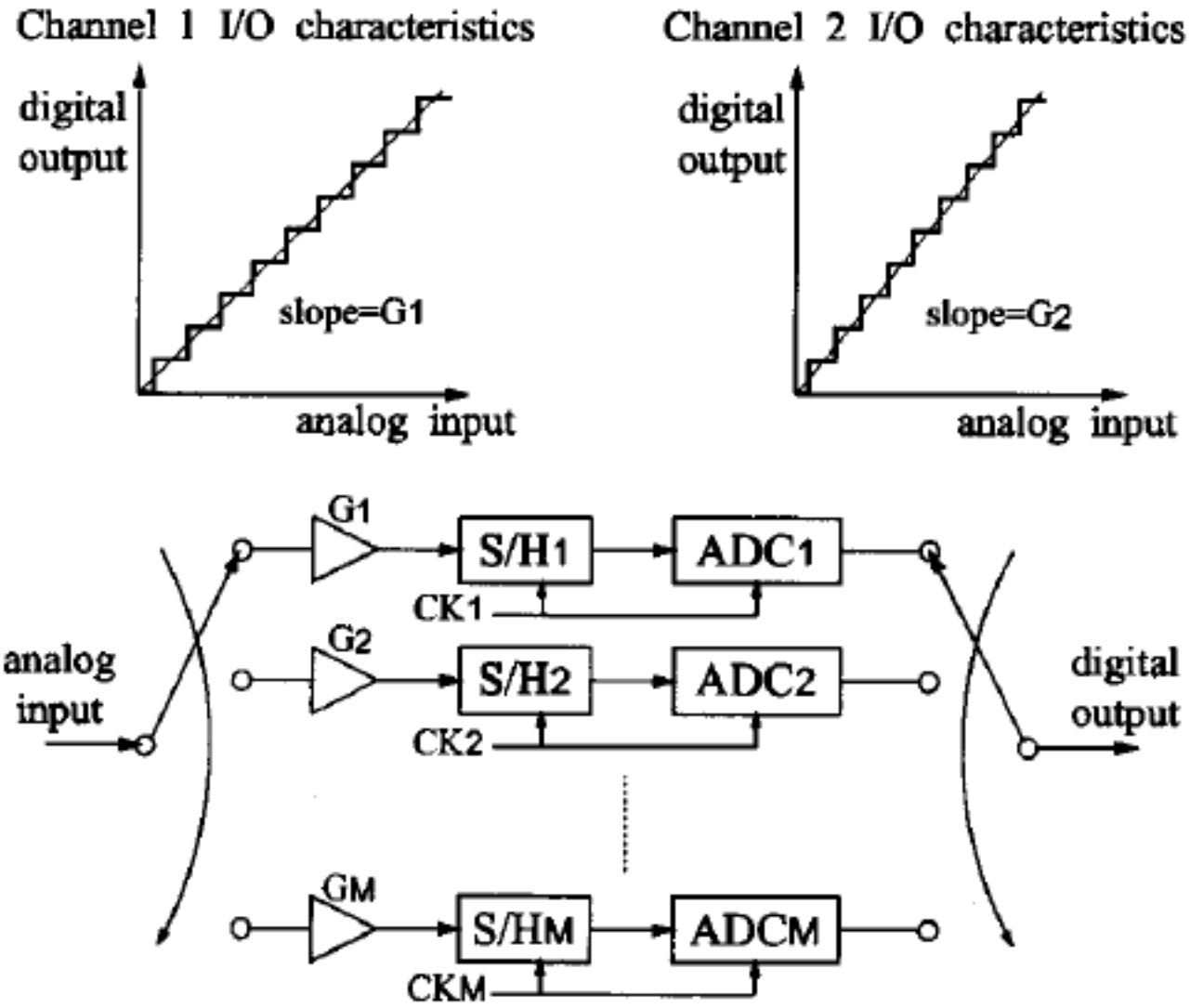
$$f_{noise} = k \times \frac{f_s}{M}$$

M= $number\ of\ channels$, e.g. 4

$k = 1,2,3,\ldots$

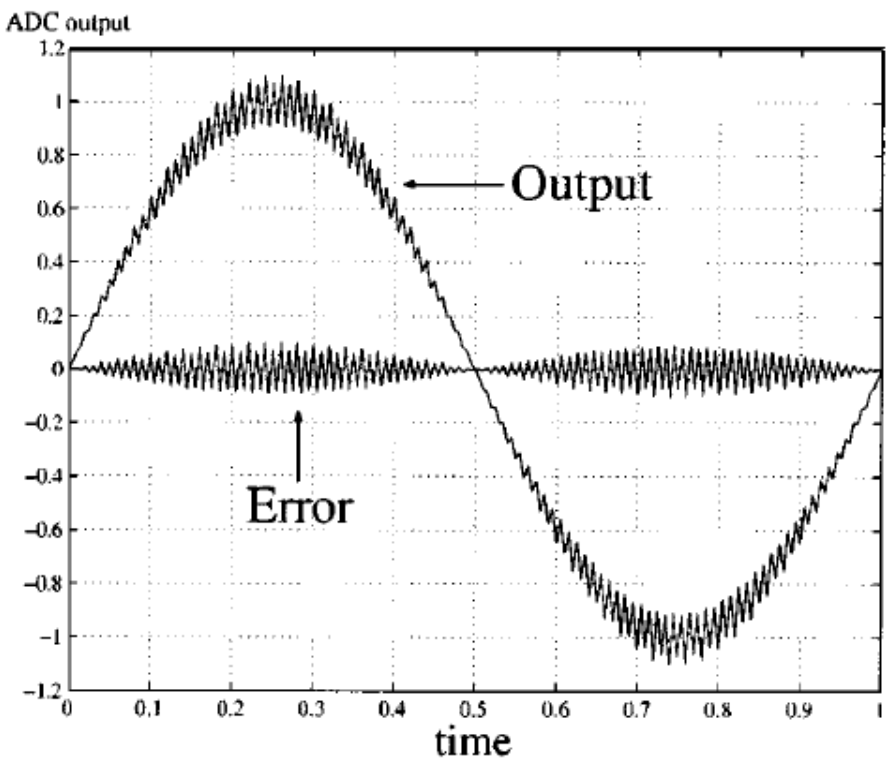
[Kurosawa, TCAS-I 2001]

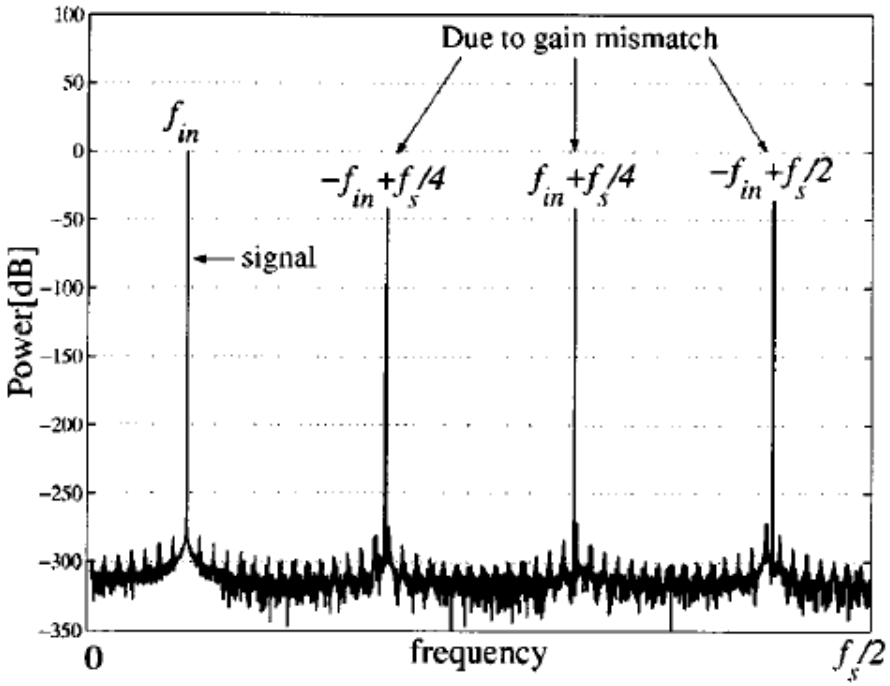
Gain Mismatch Effect



[Kurosawa, TCAS-I 2001]

Gain Mismatch Effect





Spurious tone frequencies:

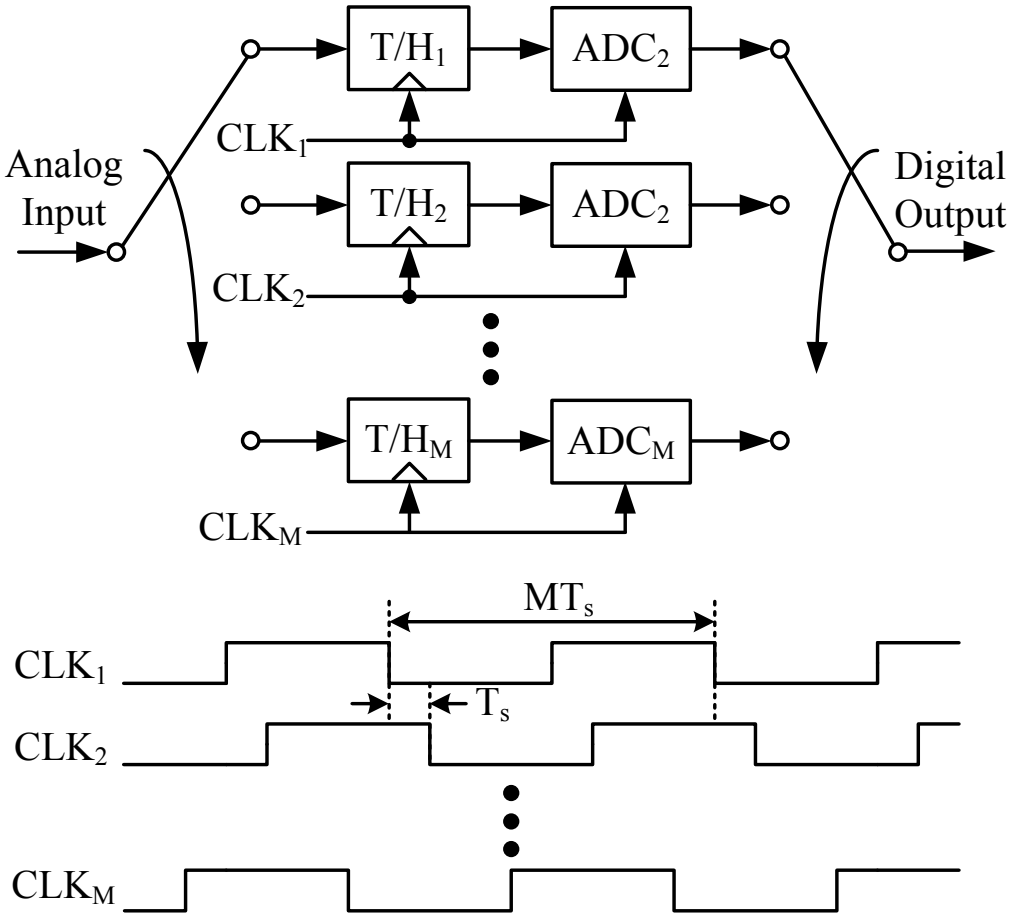
$$f_{noise} = \pm f_{in} + k \times \frac{f_s}{M}$$

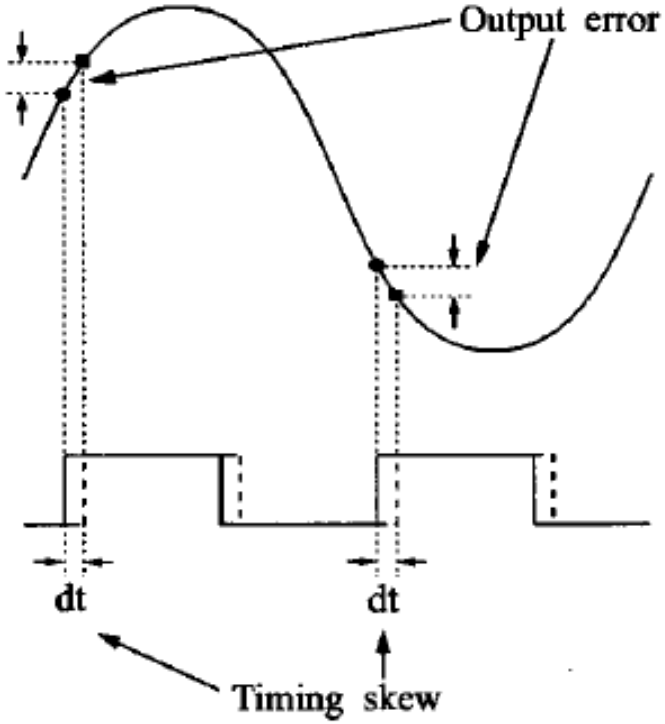
M= *number of channels*, e.g. 4

$$k = 1,2,3,\ldots$$

[Kurosawa, TCAS-I 2001]

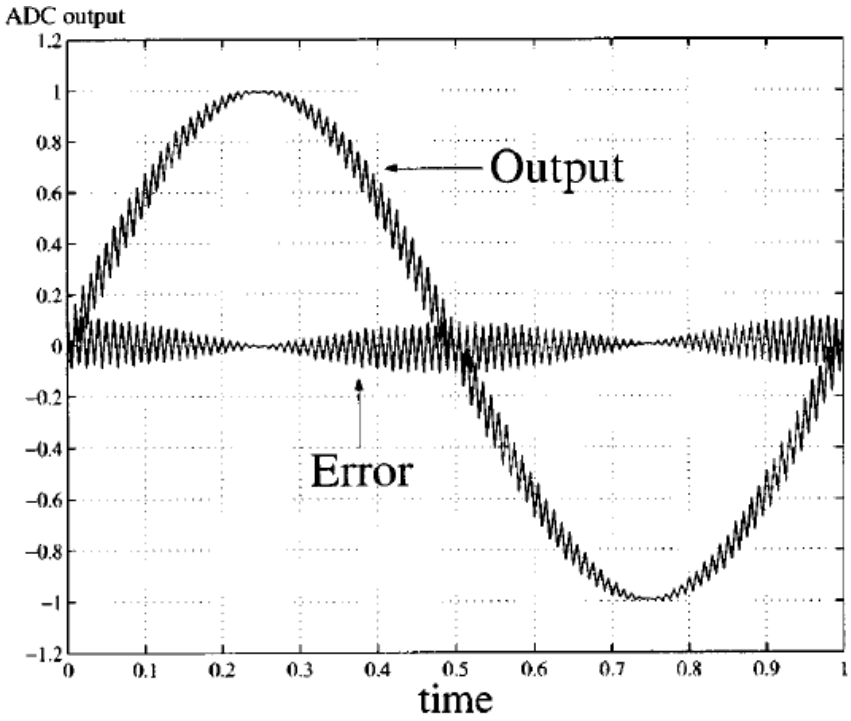
Timing Skew Error Effect

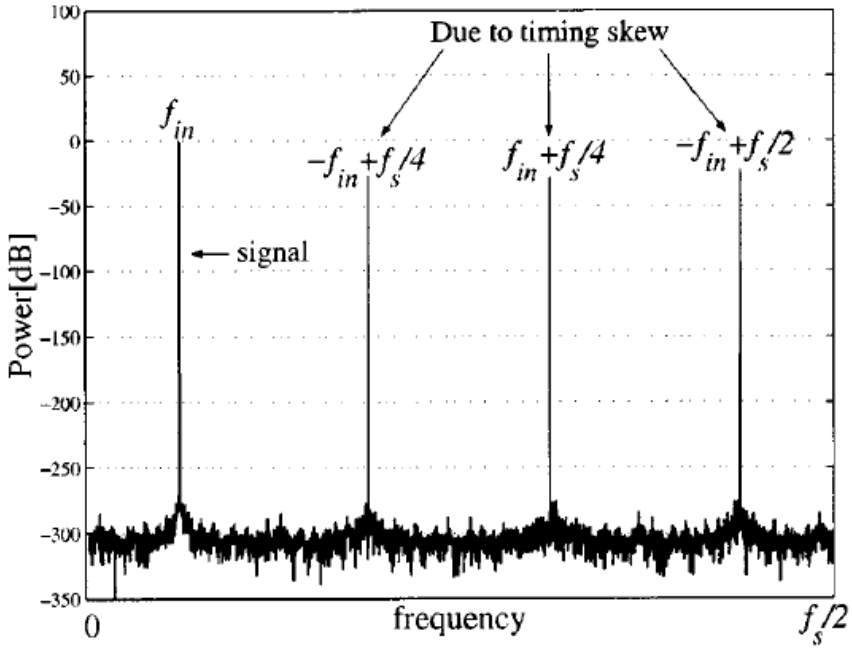




[Kurosawa, TCAS-I 2001]

Timing Skew Error Effect





$$f_{noise} = \pm f_{in} + k \times \frac{f_s}{M} \qquad k = 1, 2, 3, \ldots$$

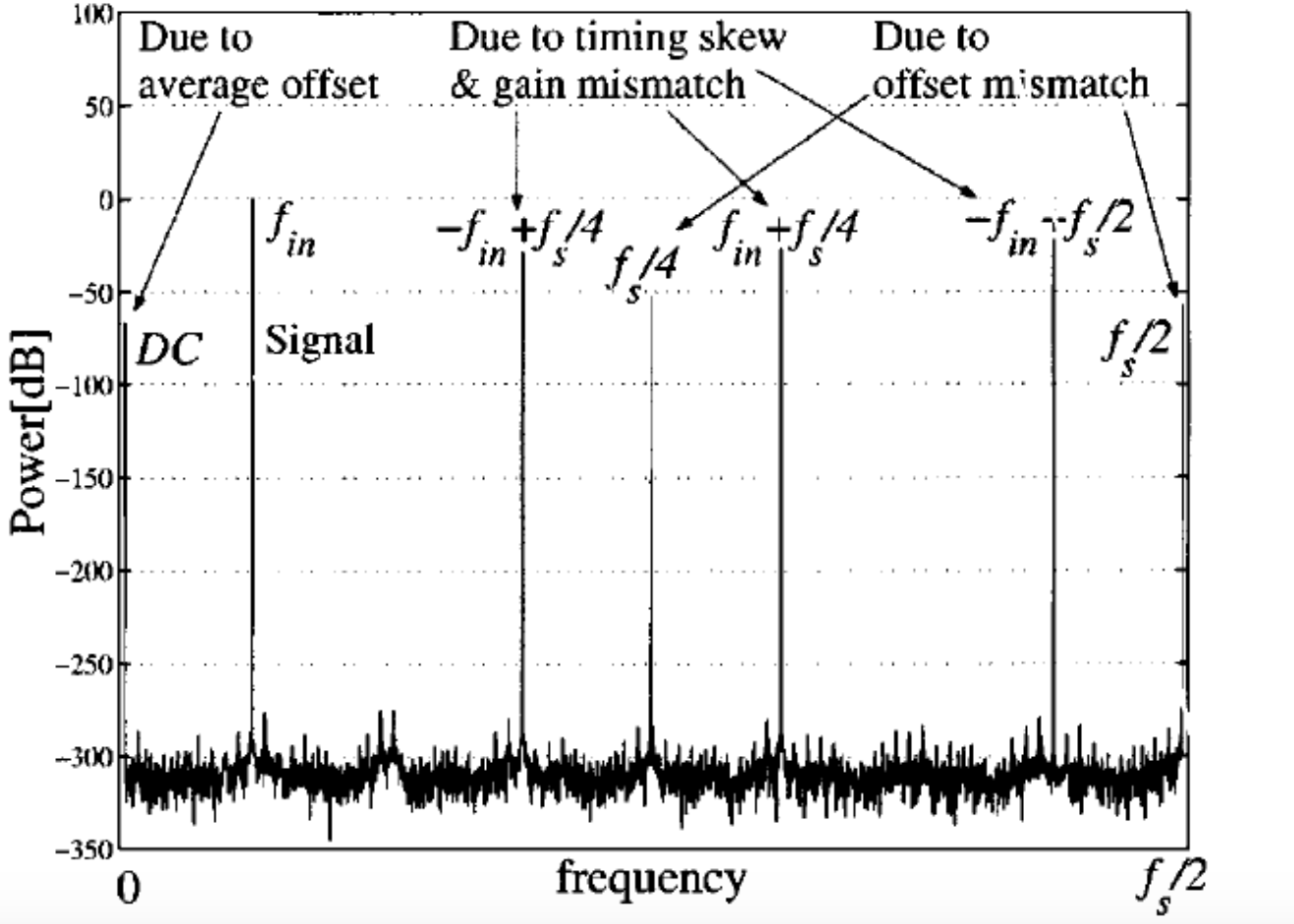
The same as that of gain mismatches

[Kurosawa, TCAS-I 2001]

What about Bandwidth Mismatches Effects

- The effect of BW mismatches are similar to that caused by the combination of
  - Gain mismatch effects
  - Timing skew (Phase) error effects

Aggregate Mismatches Effects



- All these will limit ADC performance

[Kurosawa, TCAS-I 2001]

Mismatches Calibrations

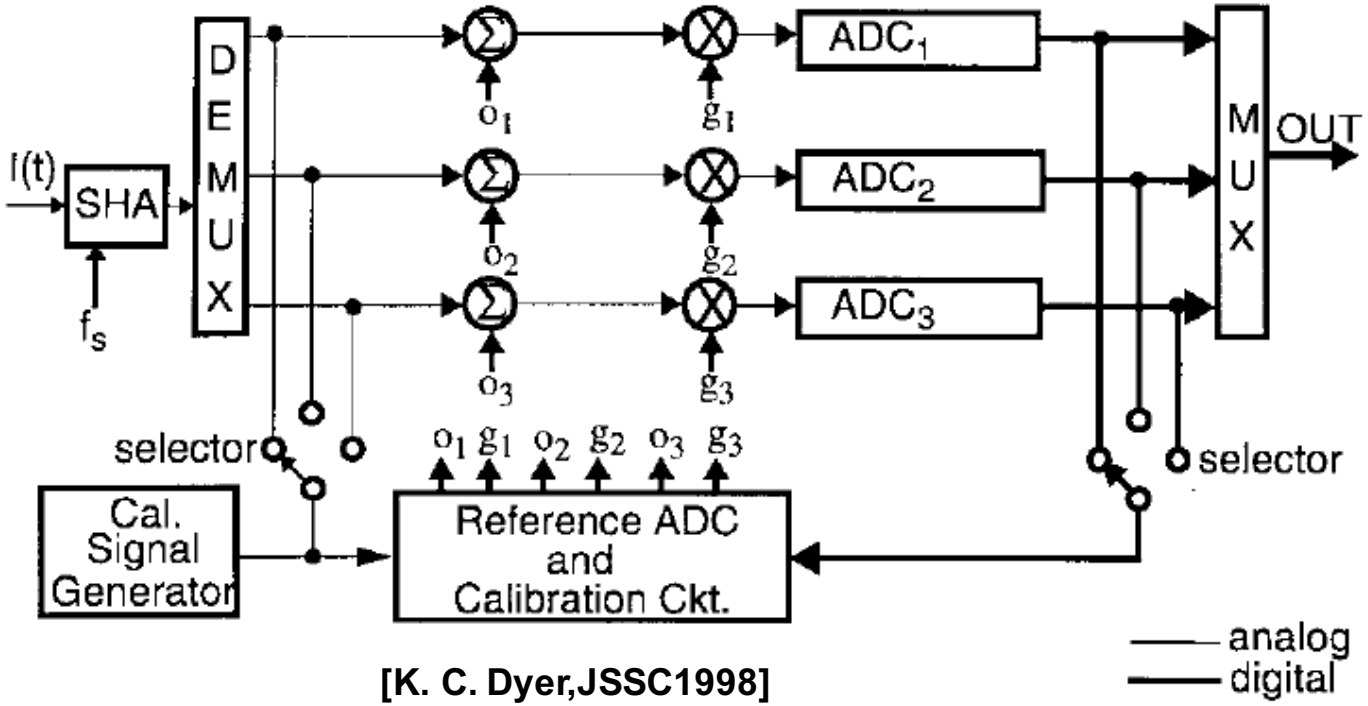
- Careful design and layout
- Mismatches always exist due to PVT variations, clock distribution networks, stray capacitance, etc.

- Calibration
  - Analog calibration
  - Digital calibration
  - Foreground calibration
  - Background calibration (can track PVT variations)

- Offset, Gain, Timing skew mismatches (analog and digital)
- BW mismatches (digital domain)

Analog Calibration for Gain/Offset Mismatches

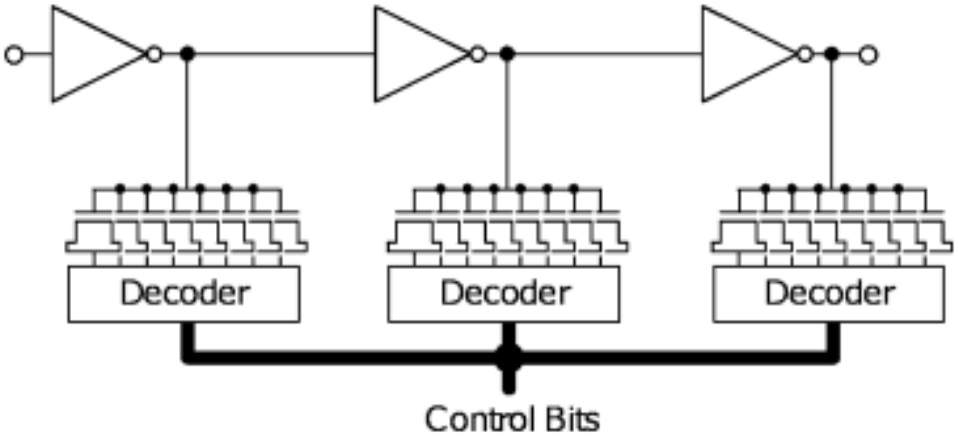
- A reference ADC is used to convert the same input
- Comparing selected ADC channel result with reference ADC result
- Estimate offset and gain mismatch by LMS algorithm
- Offset error can be calibrated by adjusting the comparator offset of each channel
- Gain error can be calibrated by adjusting the reference voltage



[K. C. Dyer,JSSC1998]

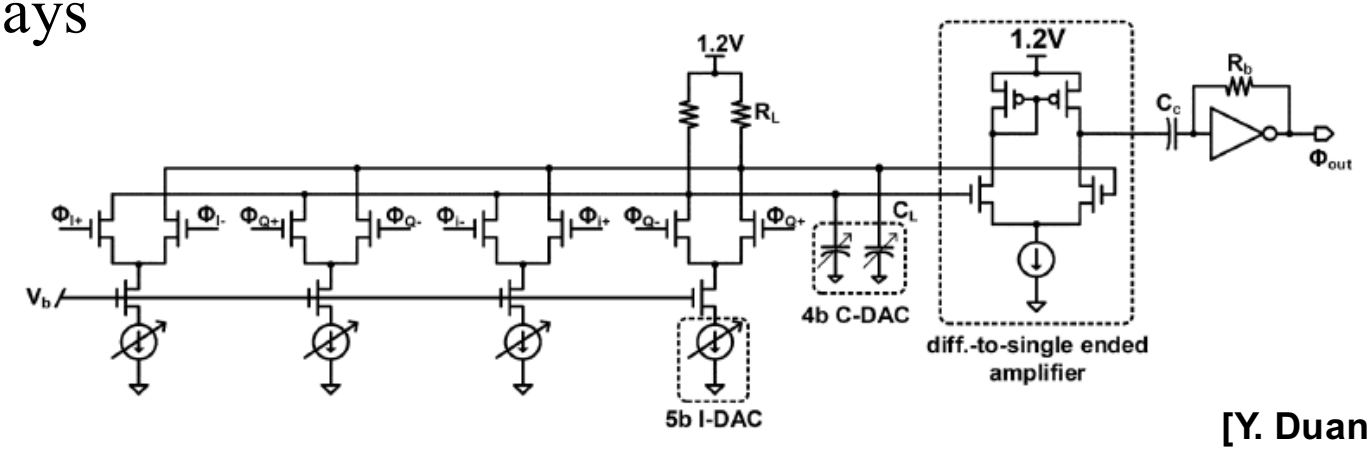
Analog Calibration for Timing Skew Mismatch

- Digital controlled capacitor bank to control the delay



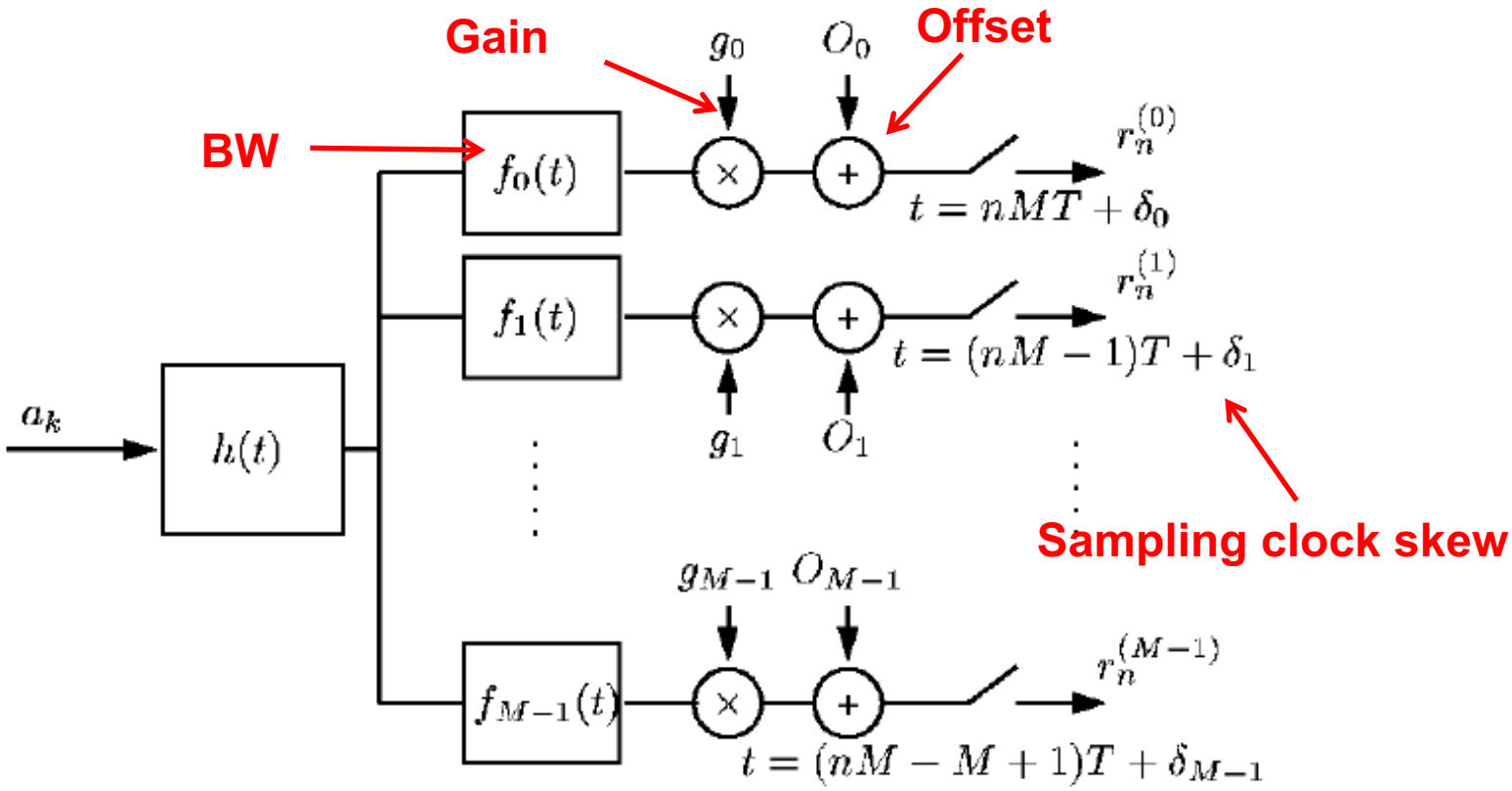
[M. E.-Chammas, JSSC2011]

- Phase Interpolator or DLLs to produce clocks with different delays



[Y. Duan, JSSC2014]

Digital Calibration for Inter-Channel Mismatches

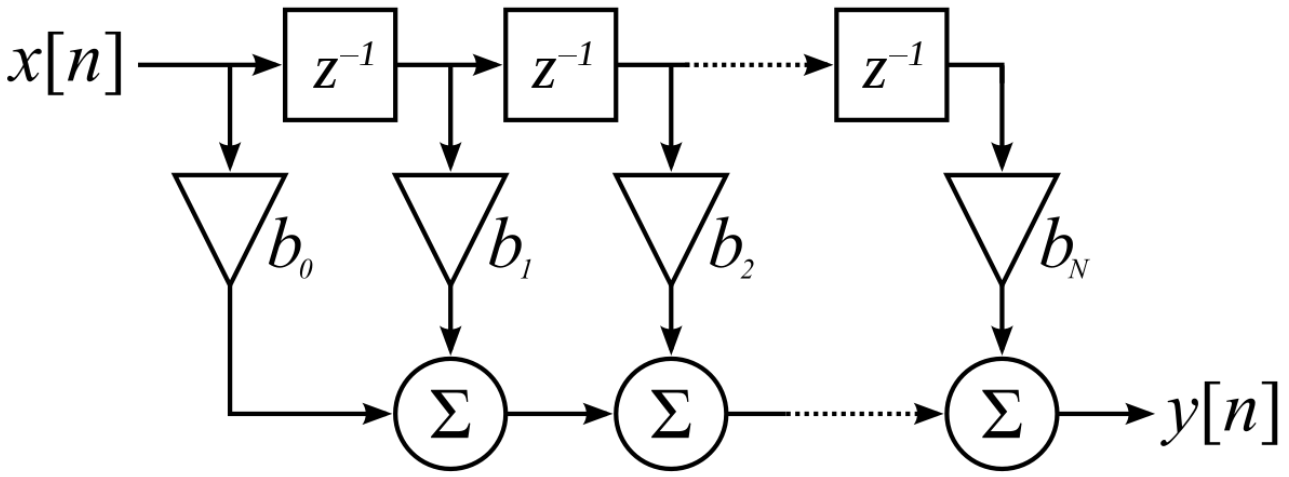


- h(t): channel response at input, i.e. input buffer and etc.
- f_0(t): frequency response of T/H
- g_0: gain error; O_0:offsets; δ_0:sampling time error

[Clariphy, ISCAS 2006]

Digital Calibration for Inter-Channel Mismatches

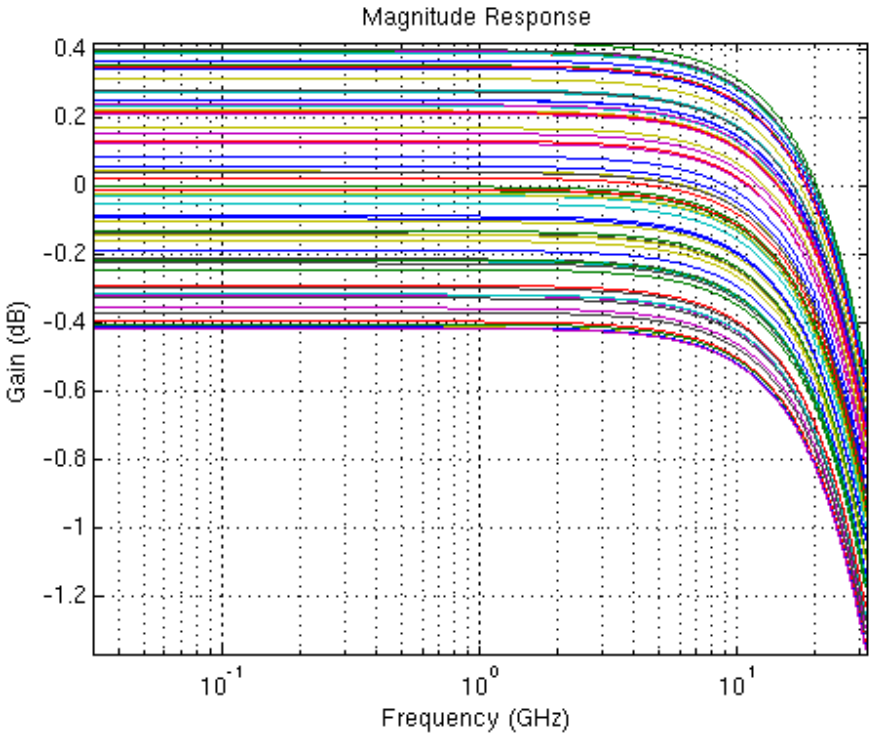
- Mismatches calibration can be formulated as equalization problem for M-input-M-output
- Offset, gain, timing skew, and bandwidth mismatches are compensated by FFE (FIR filters) or DFE
- Coefficients of FIR filters are estimated by collecting the conversion results of single-tone training signals of frequencies and best curve fitting.



FFE (FIR filters)

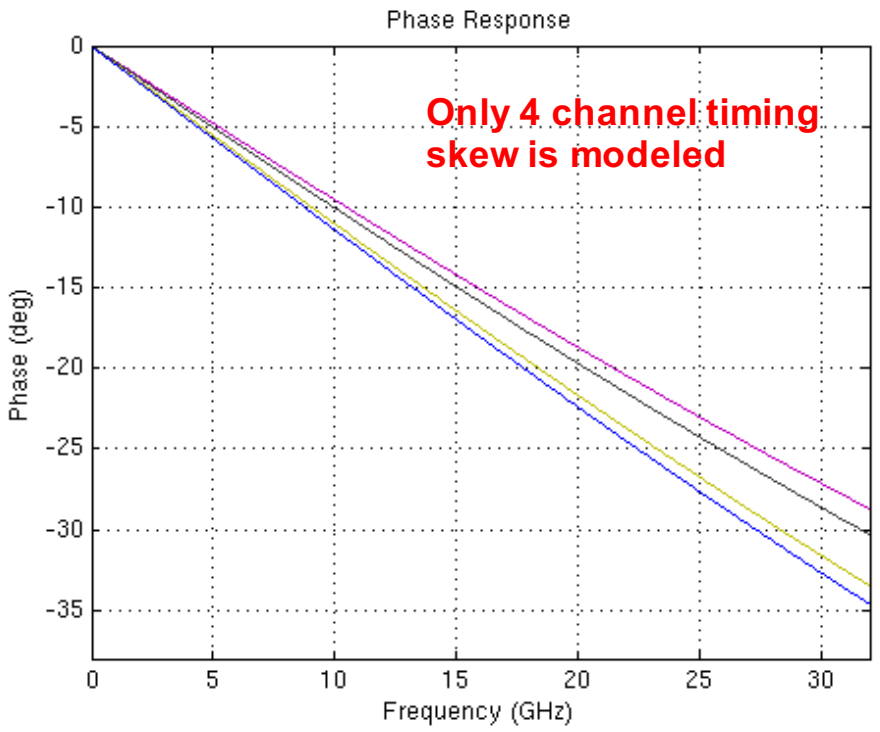
Digital Calibration for Inter-Channel Mismatches

- Transfer function of M channels



(a)

(a) Magnitude response

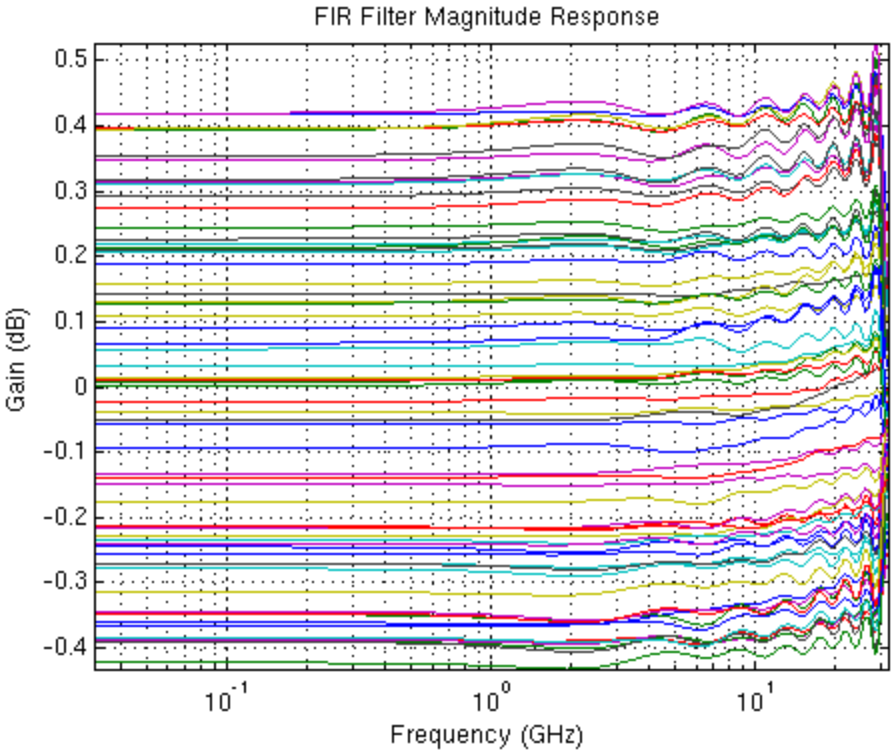


(b)

(b) Phase response

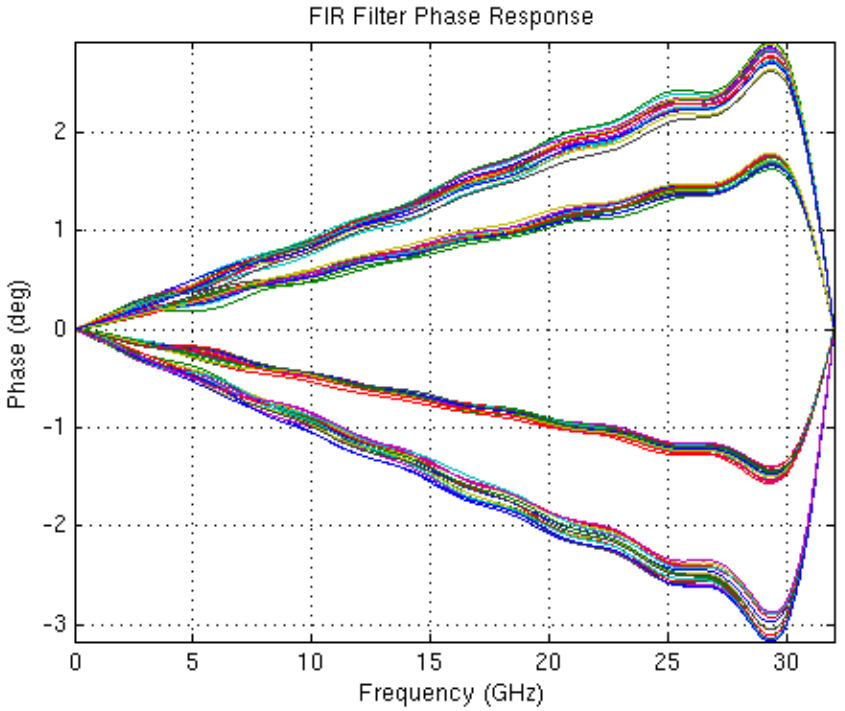
Digital Calibration for Inter-Channel Mismatches

- Transfer function Equalizer (FIR) of each channel



(a)

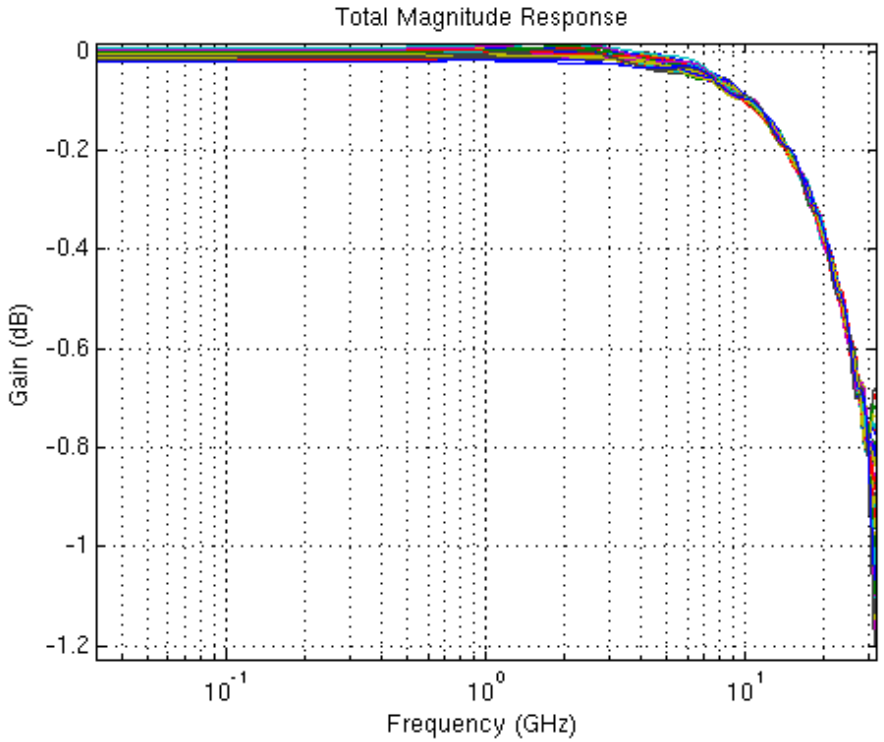
(a)Magnitude response



(b)

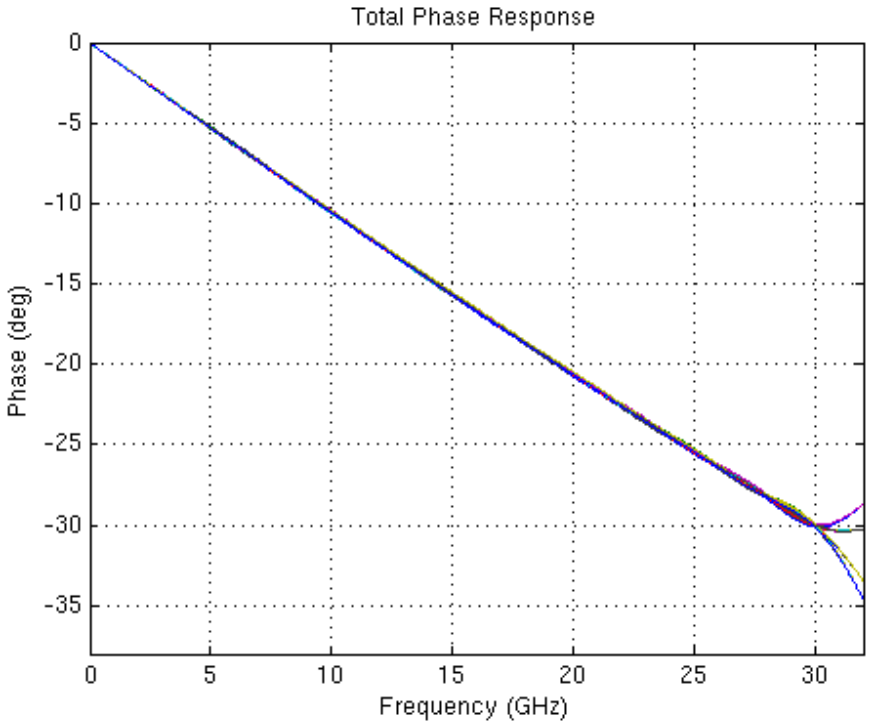
(b) Phase response

- M-Channel + Equalizer



(a)

(a) Magnitude response



(b)

(b) Phase response

- **Front-end High-Speed T/H**

Challenges in Front-End High-Speed T/H

- Front-end high-speed T/H
  - Even with interleaving, the front-end T/Hs still need to operate at multi-GHz frequency
  - Input bandwidth needs to be high
  - Other T/H non-idealities

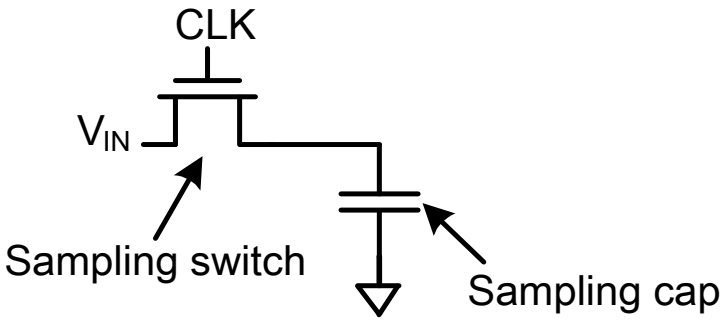
Sources of Non-idealities in T/H

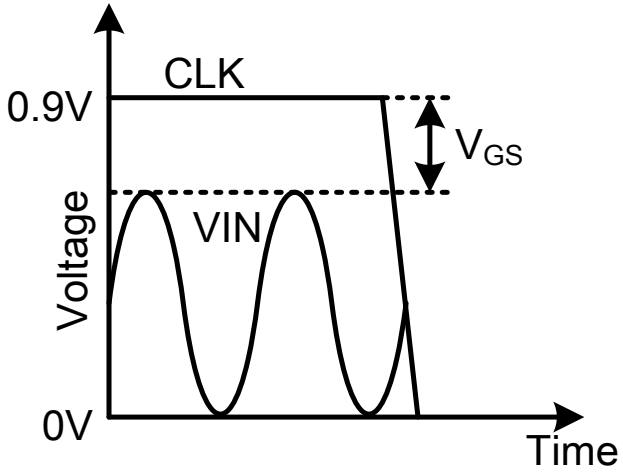
- kT/C noise
- Finite acquisition time (RC constant of the switches)
- Track mode nonlinearity, $R=f(V_{in})$
- Signal dependent sampling instant
- Sampling aperture uncertainty
- Clock feedthrough and charge injection
- …..

Track Mode Nonlinearity

- Problem: R_{on} is modulated by V_{IN}

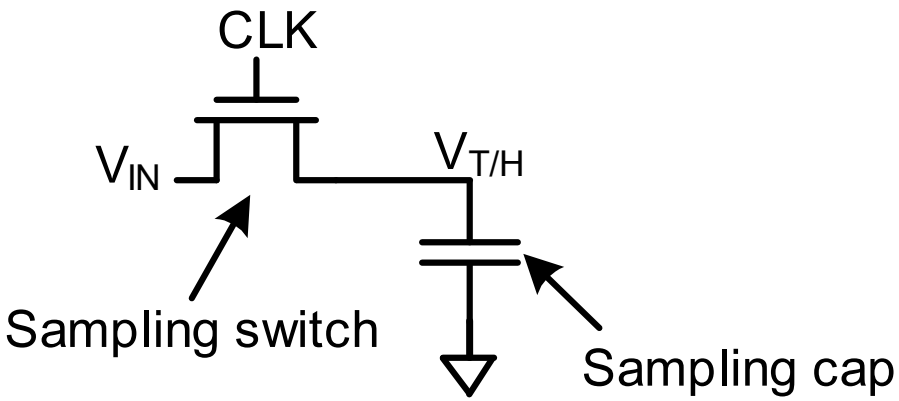
$$R_{on,NMOS} = \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)} = \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{DD} - V_{IN} - V_{TH}\right)}$$

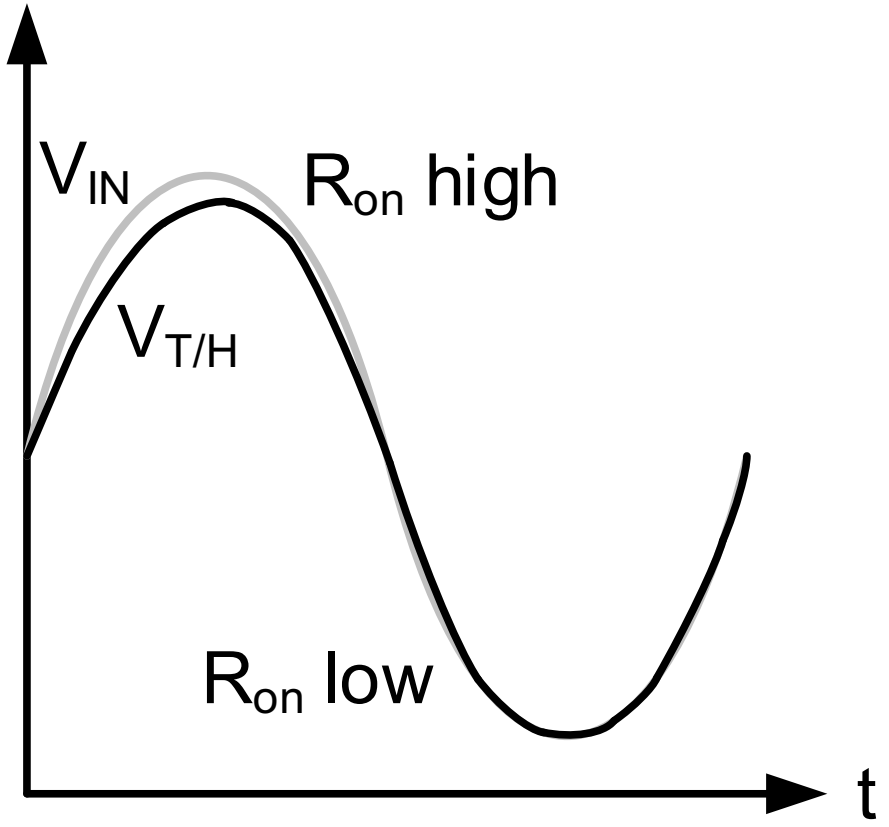




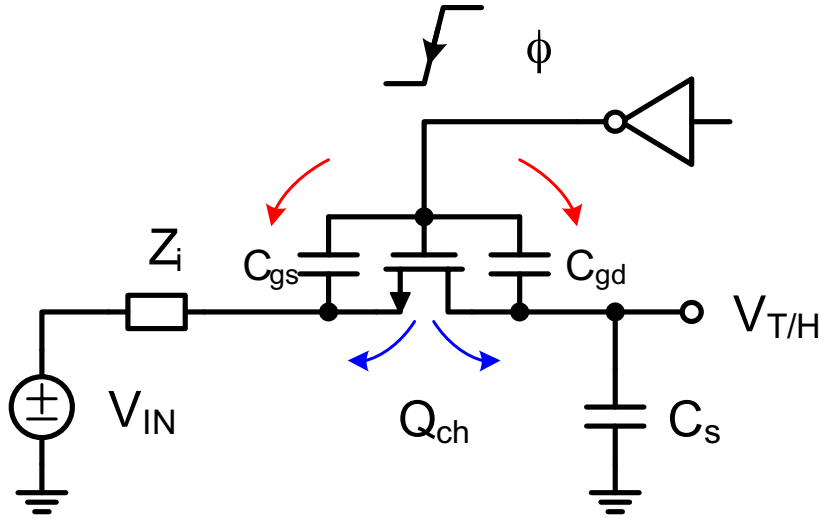
Track Mode Nonlinearity

- Output tracks well when input voltage level is low
- It gets distorted when voltage is high due to increase in R_{on}

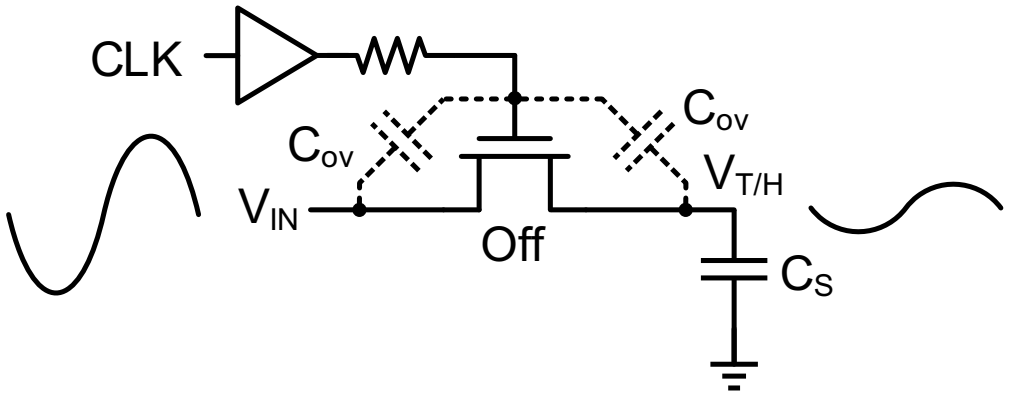




Clock Feedthrough and Charge Injection

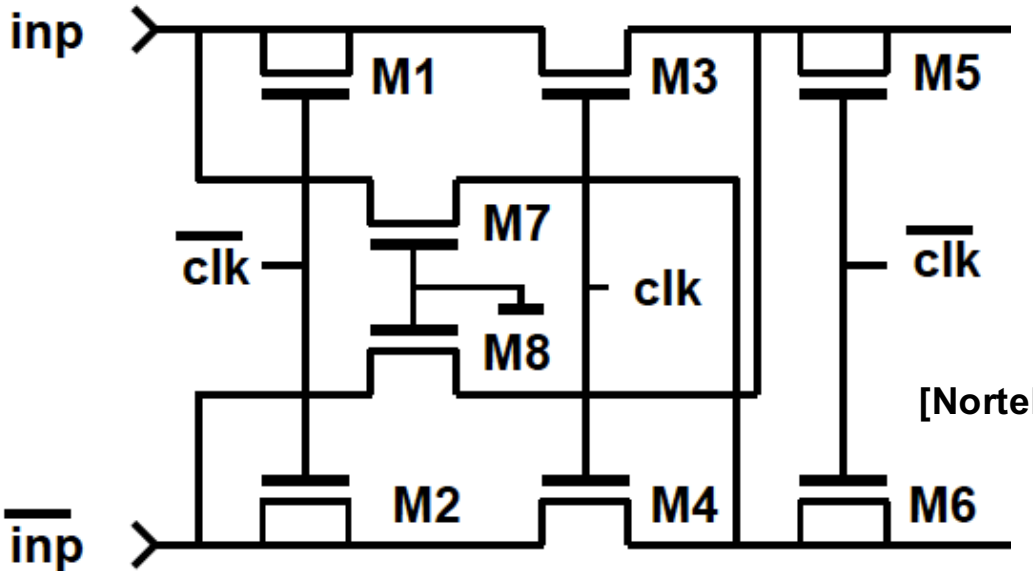


Track Mode



Hold Mode

A Basic Front-End T/H

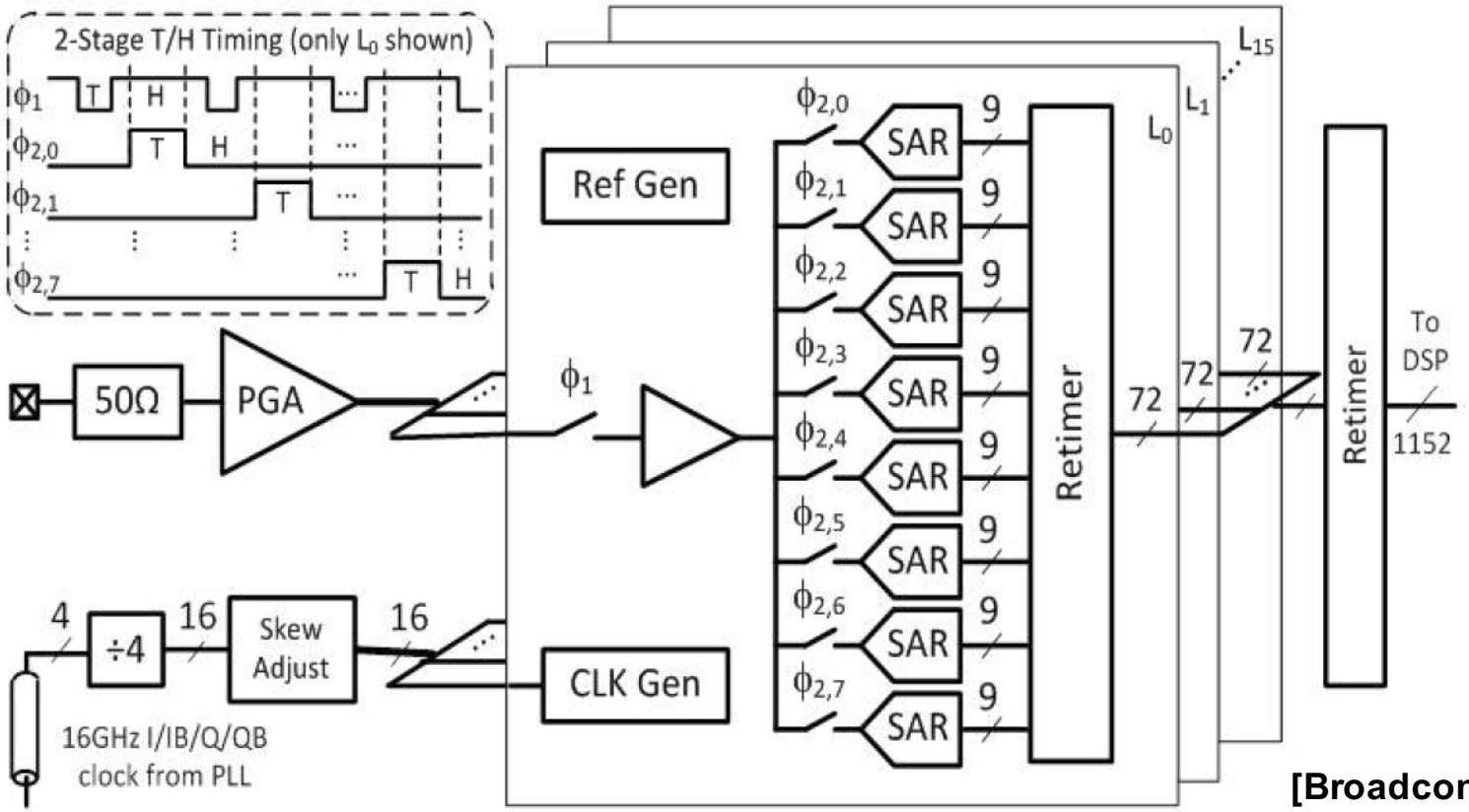


[Nortel, A 40GS/s 6b ADC, ISSCC 2010]

- M3 & M4: sampling switch
- M1 & M2: clock feedthrough and charge injection cancellation
- M5 & M6: clock feedthrough and charge injection cancellation
- M7 & M8: signal feedthrough cancellation
- Differential structure to cancel HD2 and some offset

Front-End T/H: Achieving High BW

- Hierarchical sampling architecture for a high degree of interleaving
  - BW limited by the heavy load from all of parallel sub-ADCs
  - Large amount of power on distributing low jitter clocks to all parallel sampling switches
  - Two-stage interleaving to improve the bandwidth and keep the jitter low



[Broadcom, ISSCC 2017]

64 GS/s ADC in 2-stage (16 x 8) T.H with 128 unit-SARs

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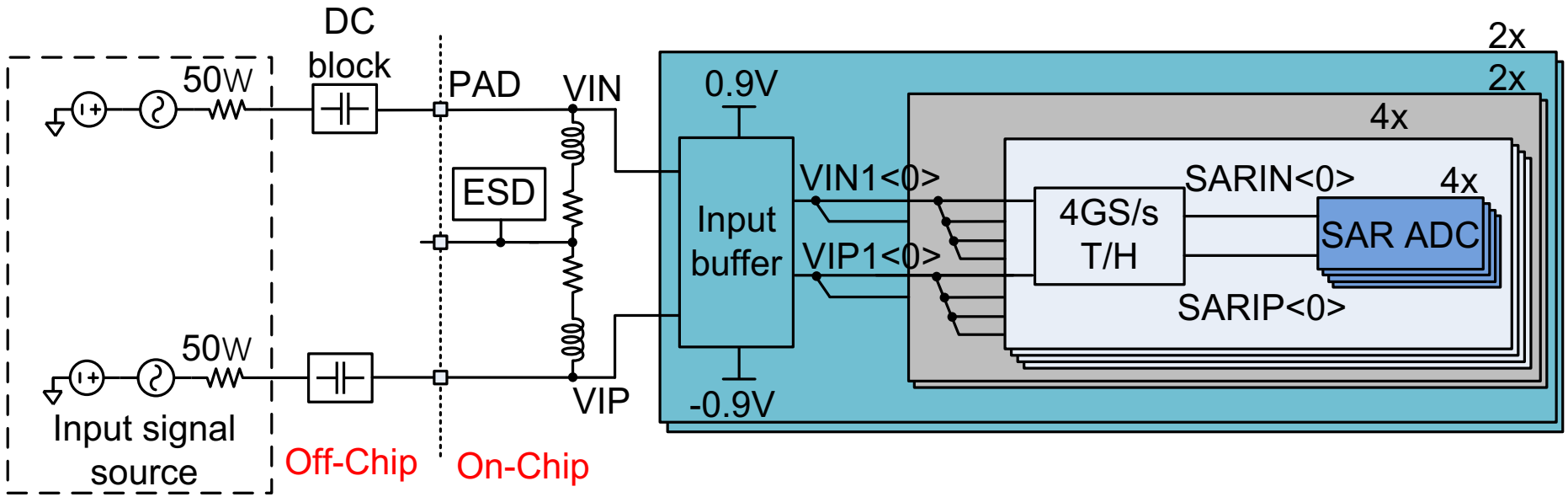
Front-End T/H: Achieving High BW

- High BW techniques:
  - Parasitic capacitance of multi-GS/s T/H circuits used as sampling capacitor
  - Input buffer to present low impedance to the sampling switches
  - Inductive peaking added at the inputs to extend the bandwidth
  - ESD-diodes at the common-mode node to reduce input parasitic capacitance

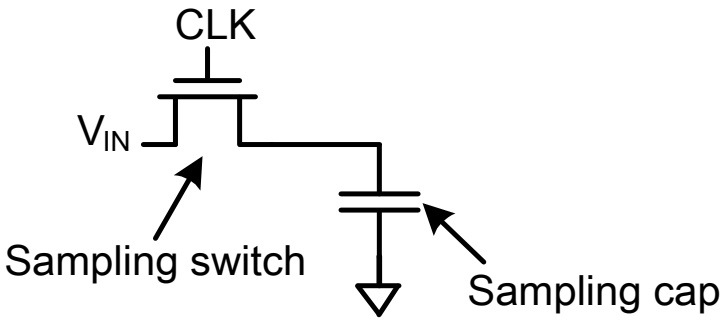


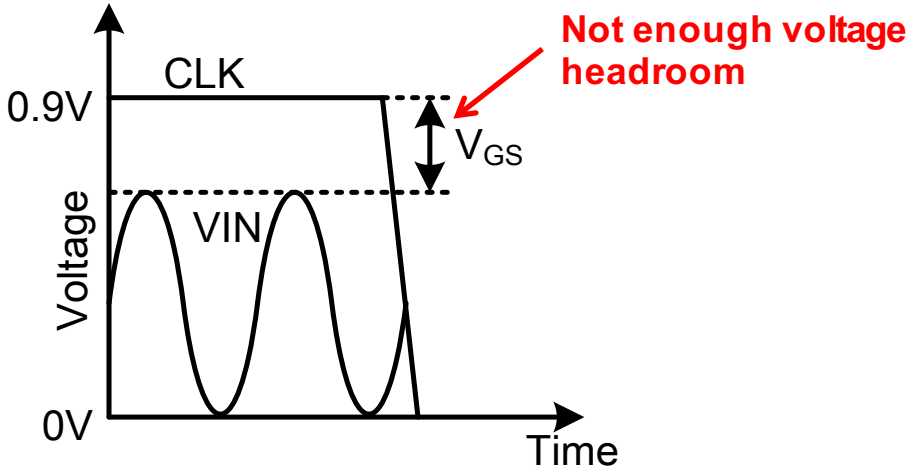
Challenge in Obtaining Good SNR

- Not enough voltage headroom to turn on switch
  - Limiting the input signal swing and affecting the SNR

- Large signal swing would cause large variations in the on-resistance of the switch, resulting in nonlinearity.
  - Turned-on resistance can be expressed as

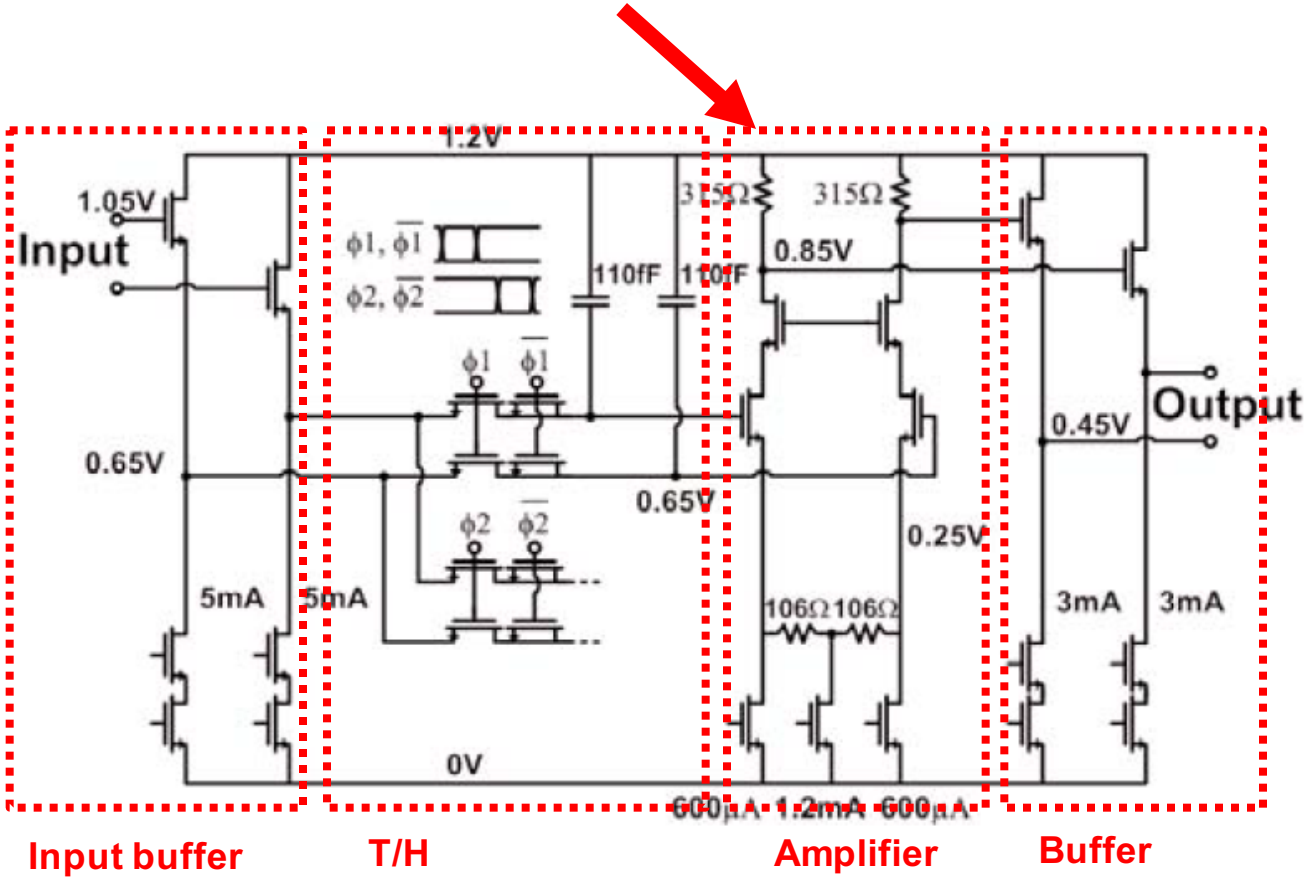
$$R_{on,NMOS} = \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)} = \frac{1}{\mu C_{ox}\frac{W}{L}\left(V_{DD} - V_{IN} - V_{TH}\right)}$$





Solution to the SNR Challenge

- Sampled signal is amplified before being sent to sub-channel ADCs

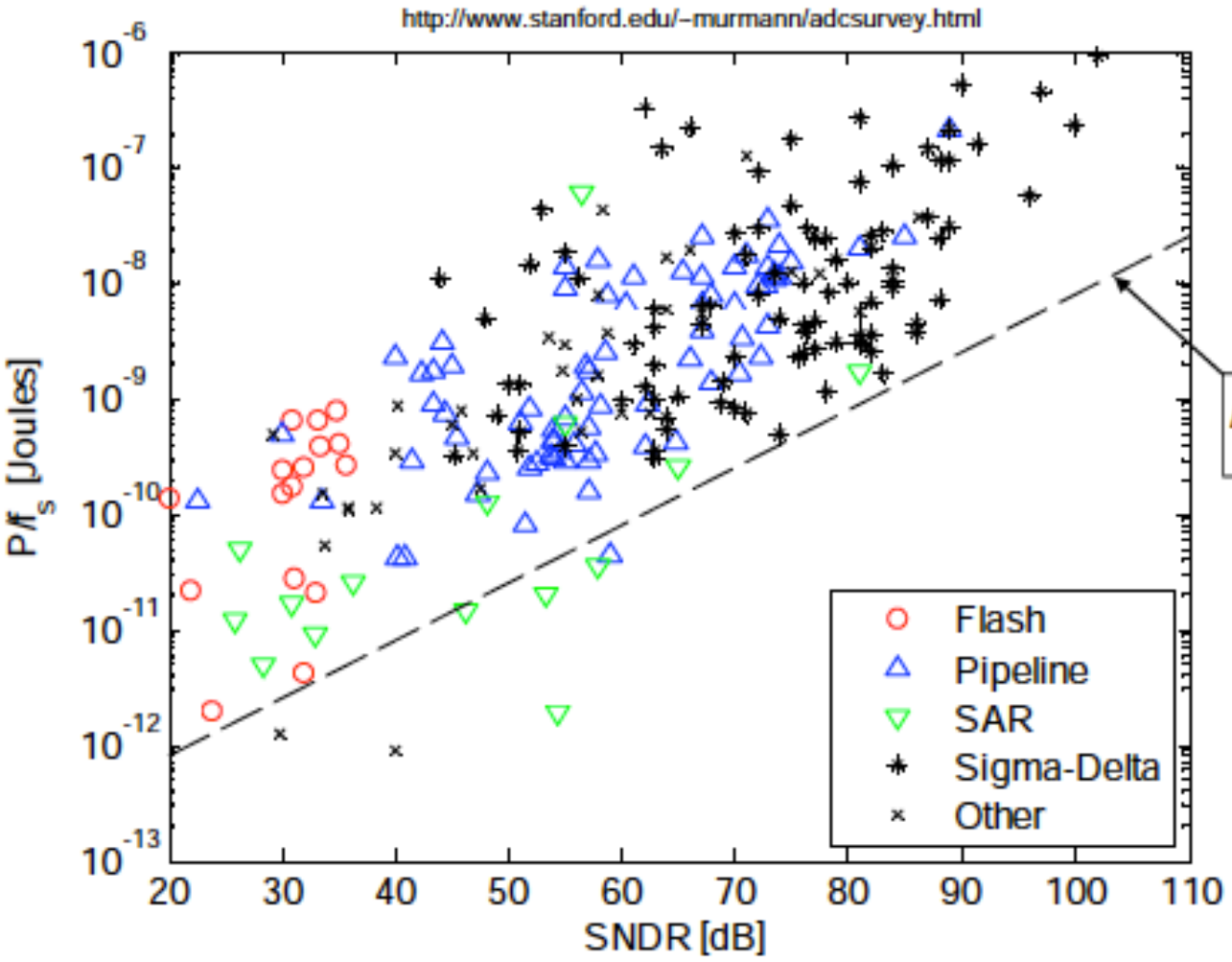


[Clariphy's 20GS/s 6b ADC]

[Clariphy, a 50Gb/s DP-QPSK/BPSK transceiver, ISSCC 2012]

- **Sub-ADC Design**

Sub-ADC Architectures



$$FOM = \frac{P}{f_s \cdot 2^{ENOB}} = 100 \frac{\text{fJ}}{\text{conv-step}}$$

$$ENOB = \frac{SNDR[dB] - 1.76}{6.02}$$

[Image from B. Murmann notes]

Sub-ADC Architectures

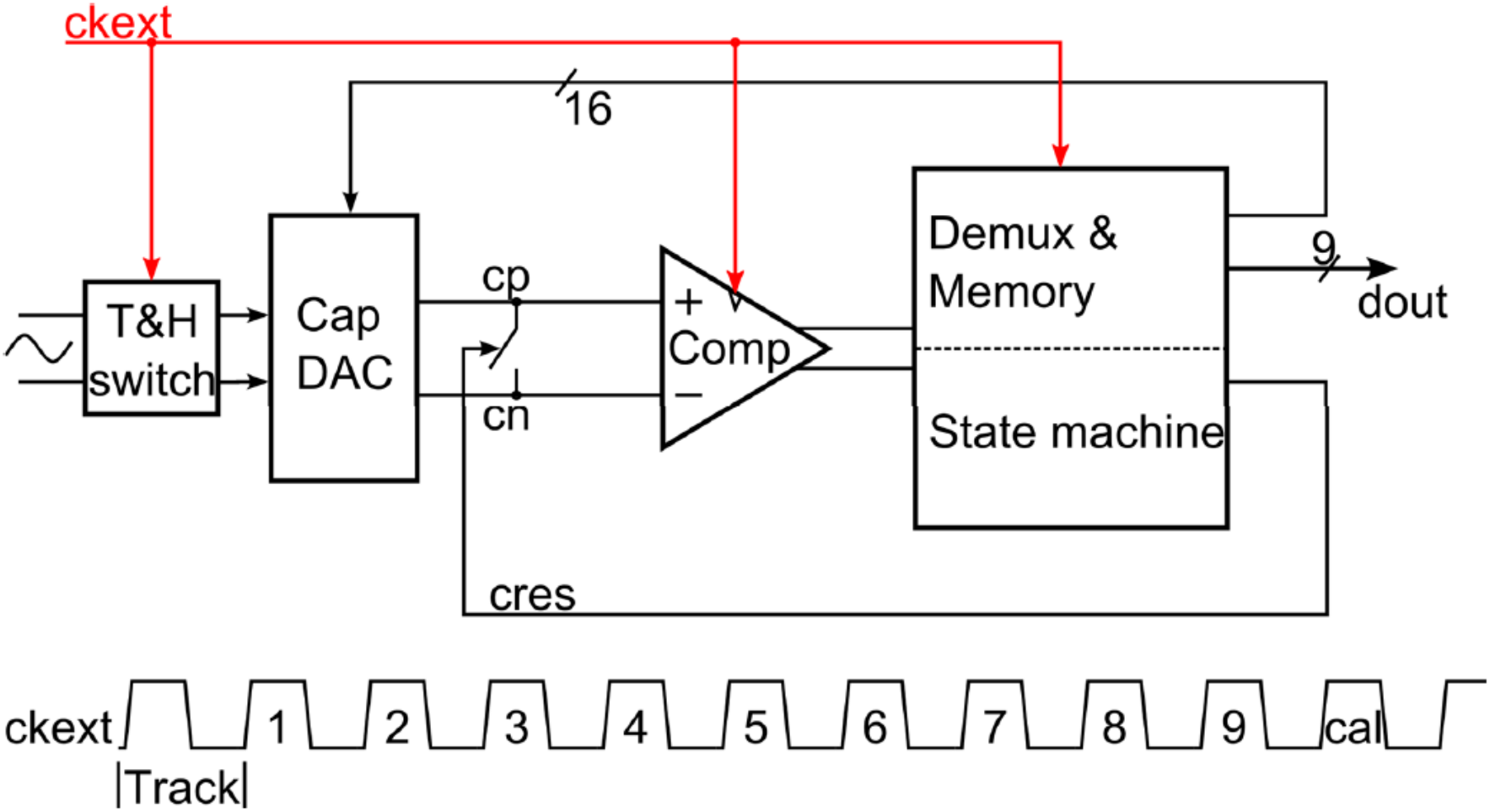
- Low power operation and small silicon area are the key factors since there are many channels of them

- SAR is the choice as sub-ADC
  - Pros
    - Power efficient, no static current consumption
    - Compatible with technology scaling
    - Can handle rail to rail signal swing, relaxing noise requirement.
    - Device nonlinearity is not of concern
  - Cons
    - Sequential operation tends to limit the conversion speed
    - Capacitor and comparator mismatch could lead to distortion.

Design of SAR ADCs

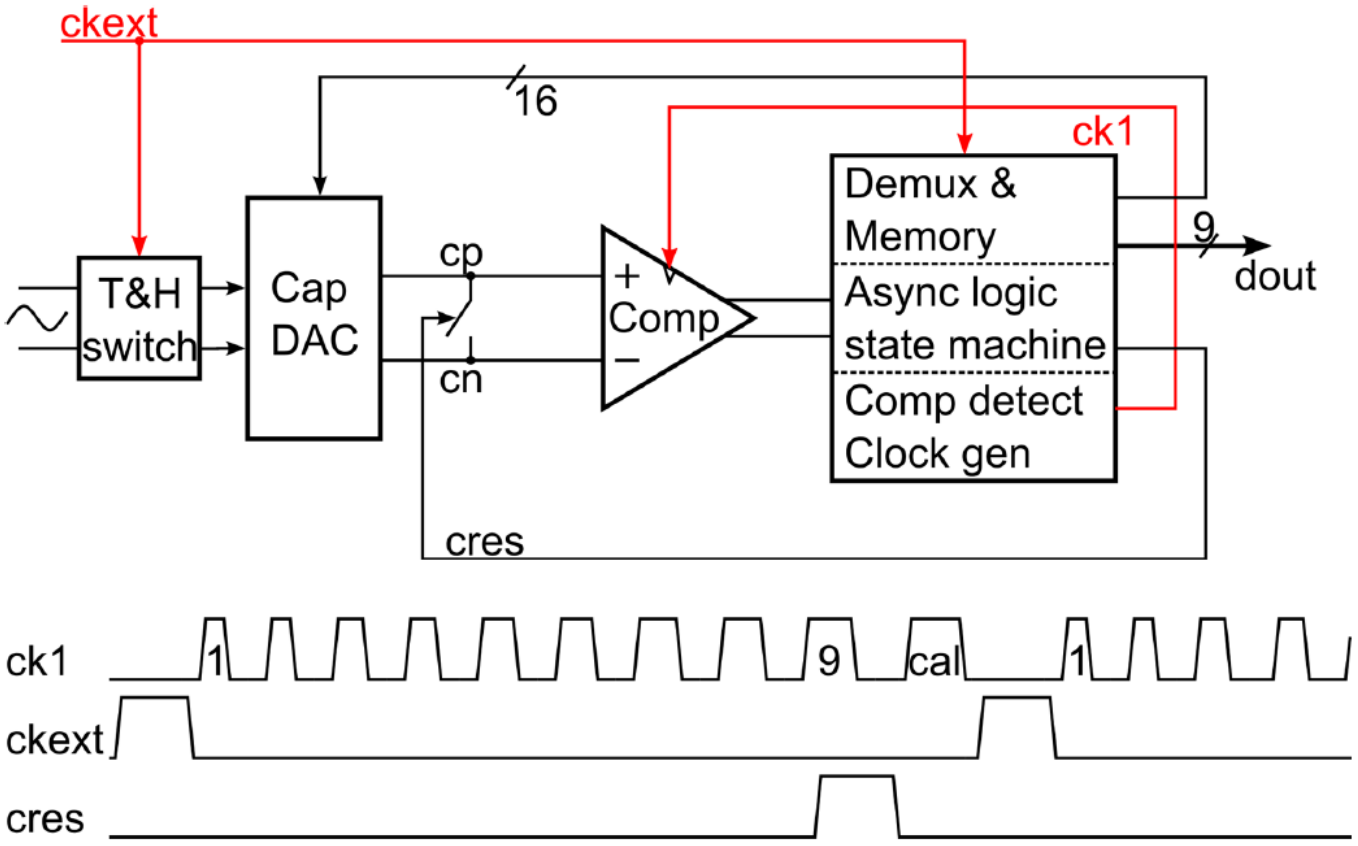
- Further improving the SAR speed
- Further optimizing the power dissipation of SAR
- Comparator offset calibration
  - Optional for SAR ADCs with single comparator
  - Most advanced design employs multiple comparators, then comparator offset calibration is necessary
- DAC capacitor calibration
  - Low-power and high-speed operation requires capacitor to be small
  - Capacitor mismatch arise due to small size

Conventional Synchronous SAR



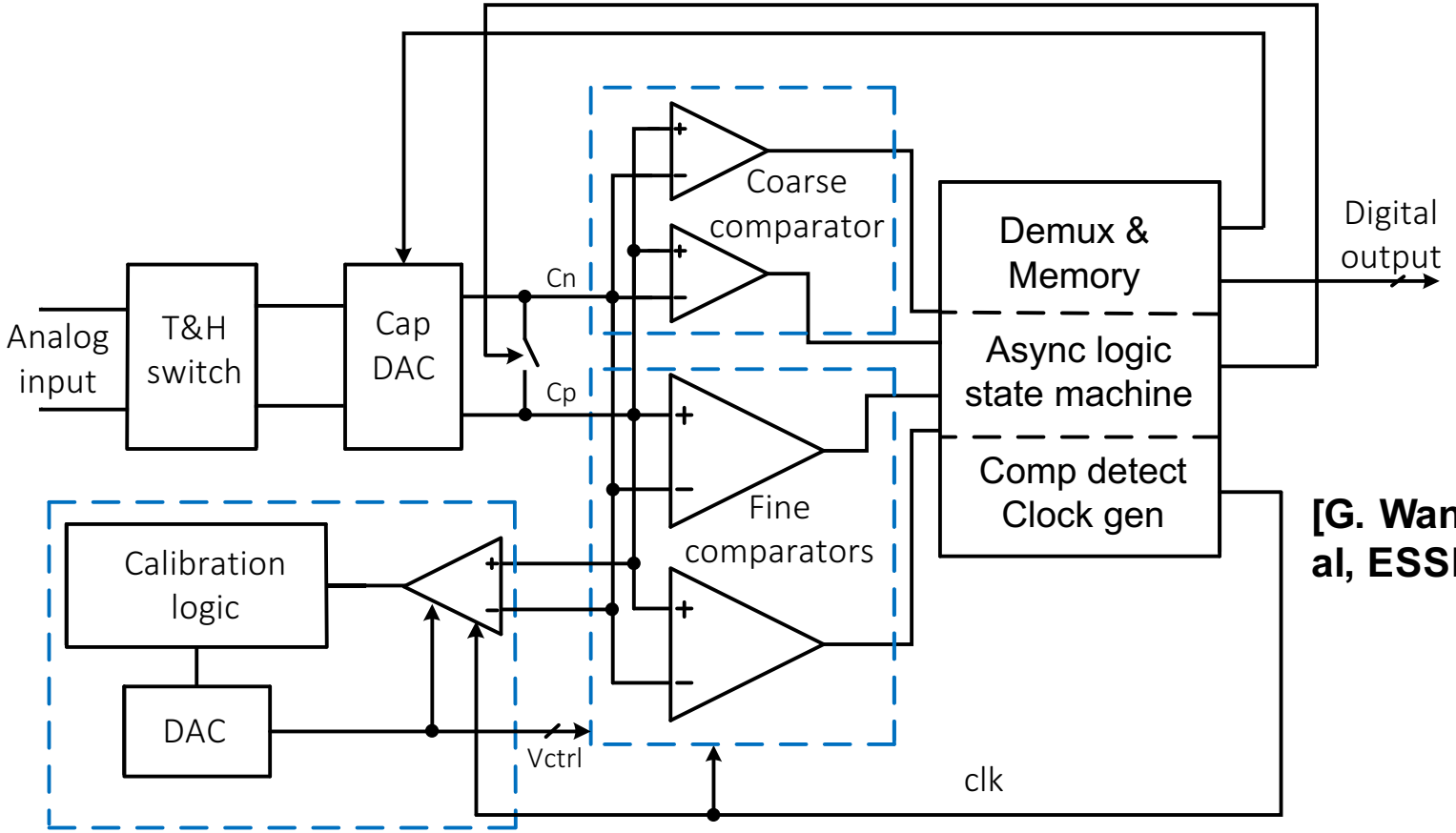
- A high speed external clock, Fs*(N+1), controls operation of every bit
- The duration of every bit conversion is determined by the slowest bit

Asynchronous SAR



- Improving speed and reducing power dissipation of clocks
- No external high-speed clock.
- The operation of every bit is determined by the completion of the previous bit

Asynchronous SAR with Improved Speed and Optimized Power

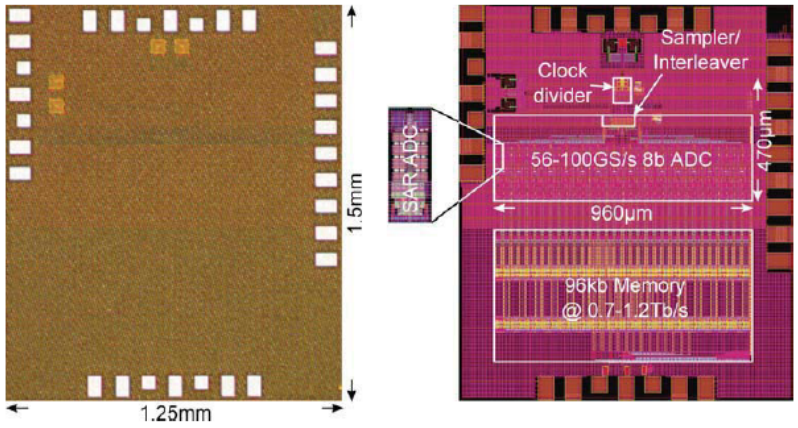


[G. Wang, P. Gui, et. al, ESSRIC 2017]

- Alternating comparators for speed improvement
- Coarse and fine comparators for power optimization
- Sub-binary DAC to improve error tolerance
- Offsets between the comparators are calibrated in background
- 1G/s 8-bit 3.2mW/channel, 43.6db in SNDR, 6.95b ENOB

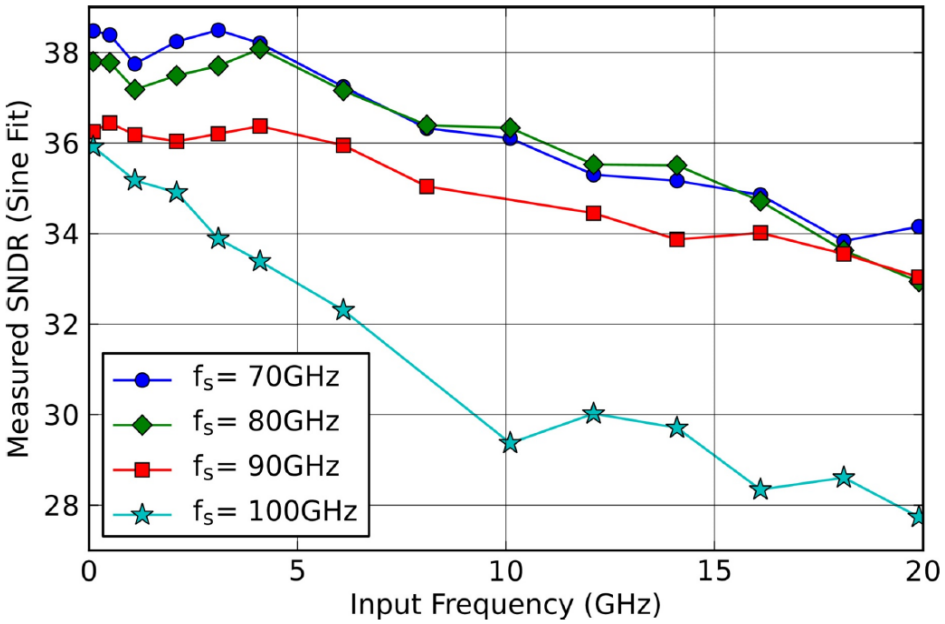
IBM 90GS/S 8-bit ADC in 32nm SOI

- BW: 22GHz
- 5.7b ENOB@6.1GHz
- 5.2b ENOB@19.9GHz
- Power dissipation: 667mW
- 64 ADC channels operating at 1.4GS/s



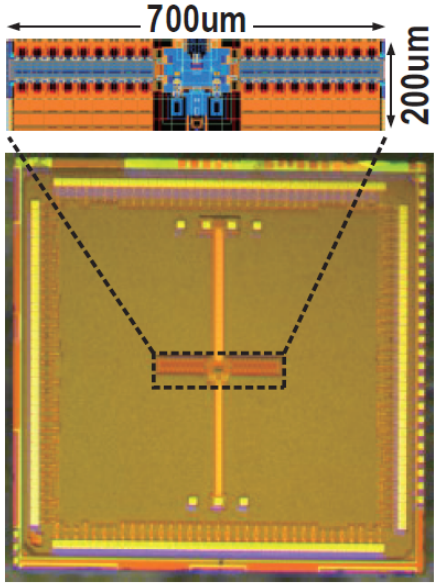
[IBM, a 90GS/s 8b ADC, ISSCC 2014]

- Foreground analog calibration
- Offset mismatch
  - Subtracted from digital conversion results
- Gain mismatch
  - Tuning the associated reference voltage of sub-channel ADCs
- Timing skew mismatch
  - Tuning the sampling clock skew
- Bandwidth mismatch is not calibrated.



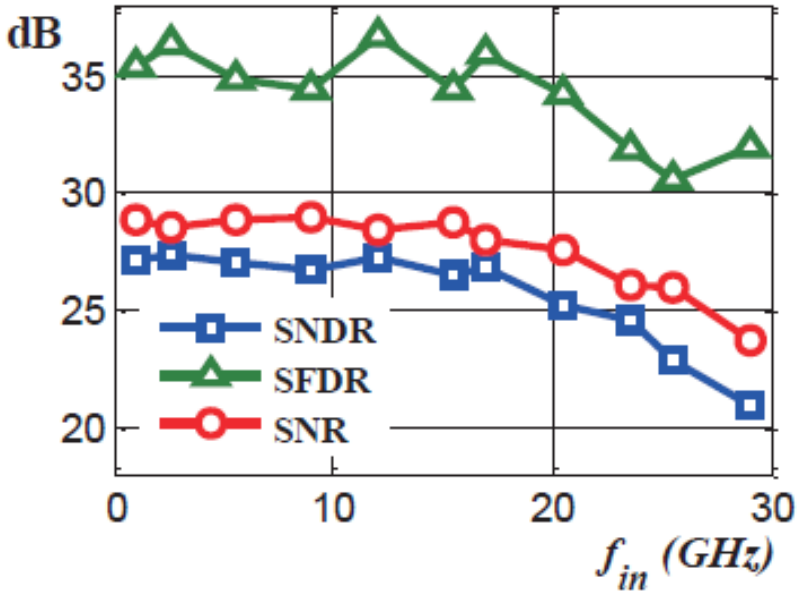
UC Berkeley's 46GS/s 6-bit ADC in 28nm FDSOI

- BW: 23 GHz
- 4.2b ENOB @ low frequency
- 3.9b ENOB @ 23.5GHz
- Power dissipation: 381mW
- 72 ADC channels operating at 0.64GS/s



[UC Berkeley, VLSI 2015]

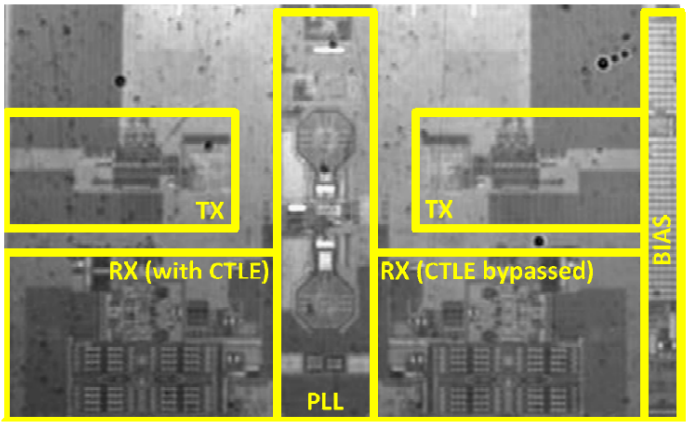
- Foreground inter-channel mismatch calibration
- Offset mismatch
  - Adjusting comparator offset
- Gain mismatch
  - Adjusting the reference voltage of sub-channel ADCs
- Timing skew mismatch
  - Using variable delay lines
- Bandwidth mismatch not calibrated



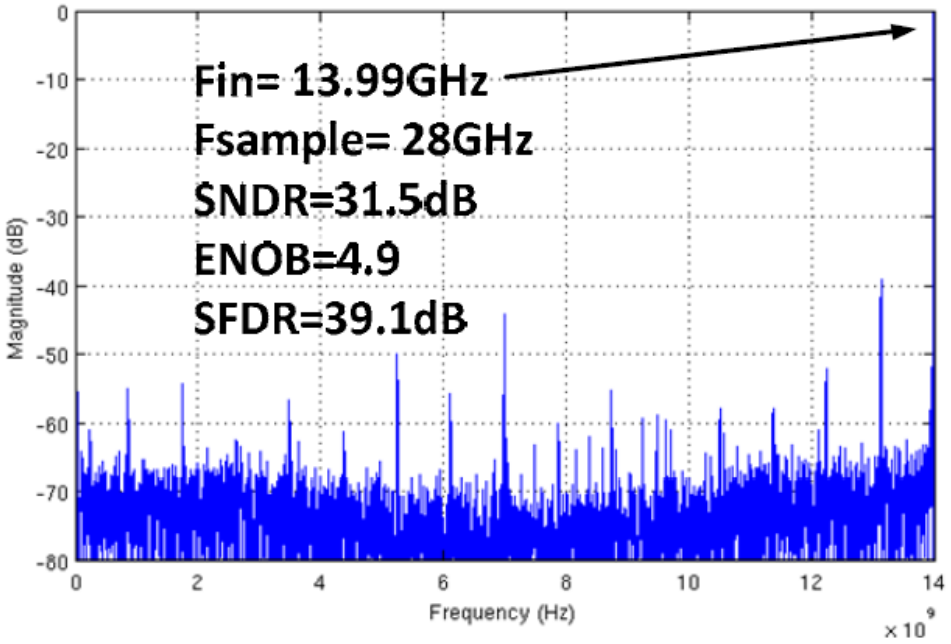
Xilinx's 28 GS/s 8-bit ADC in 16nm FinFET

- BW: 14 GHz
- 5.5b ENOB @ 0.18GHz
- 4.9b ENOB @ 14GHz
- Power dissipation: 280mW
- 32 ADC channels operating at 0.875GS/s

- Background and foreground calibration
- On-chip calibration of timing skew, gain and offset



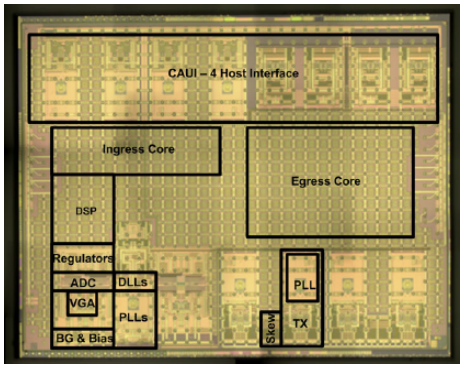
[Xilinx, VLSI 2016]



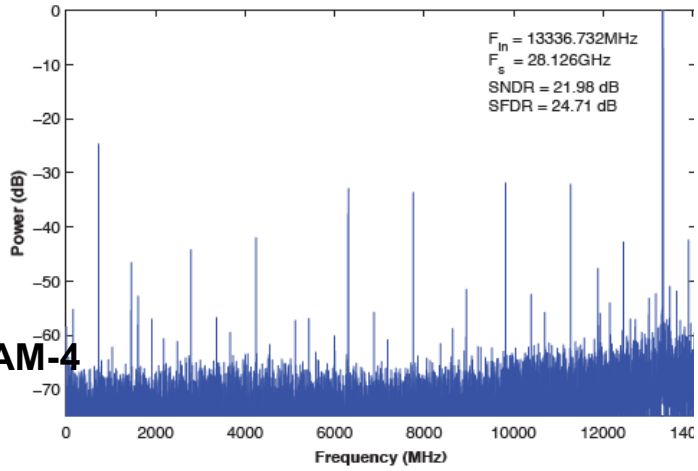
Inphy 28 GS/s 8-bit ADC in 28nm CMOS

- BW: 18GHz
- 5.8b ENOB@1GHz
- 5.0b ENOB@13.3GHz
- Power dissipation:165mW
- 32 ADC channels each operating at 0.875GS/s

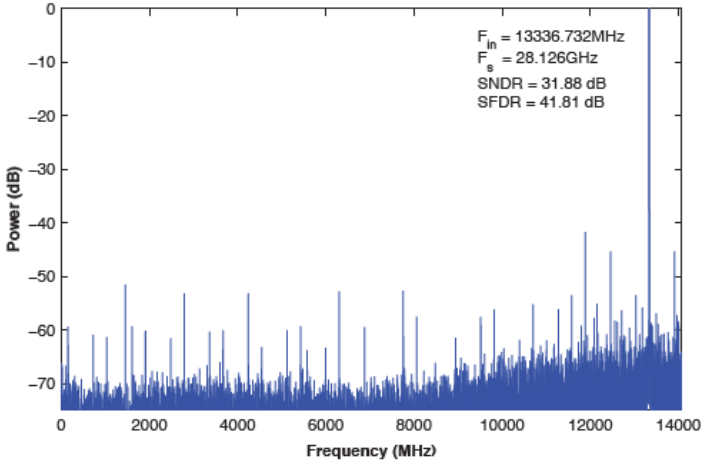
- Background & foreground calibration
  - Offset mismatch
    - Estimated by computing the average of single channel results and corrected in DSP
  - Gain mismatch
    - Envelop detection of the gain error and calibrated by tuning the gain of sub-channel ADCs
    - Residual gain mismatch is corrected in DSP
  - Timing skew mismatch
    - Tuning the delay cell in side the CLK w/ 200fs res.
  - Bandwidth mismatch corrected by FFE in DSP



[Inphy, a 40/50/100Gb/s PAM-4 transceiver, ISSCC 2016]



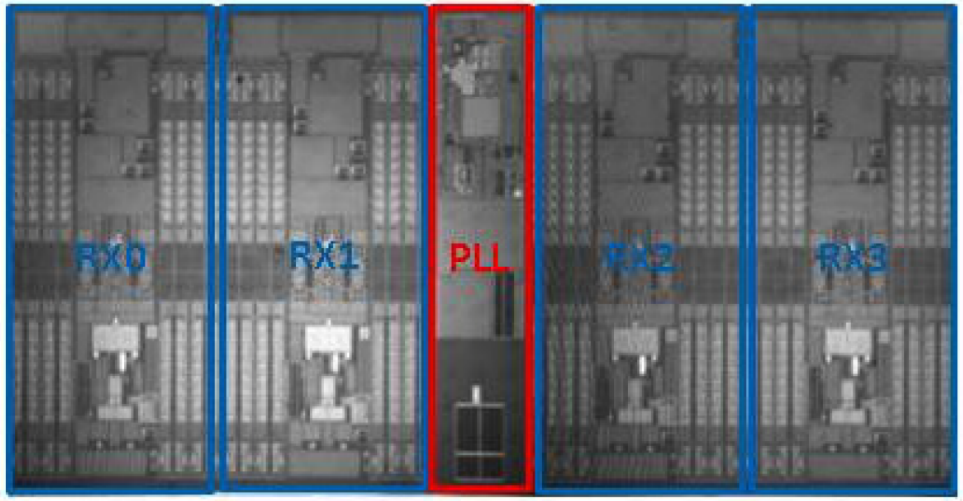
Before Calibration



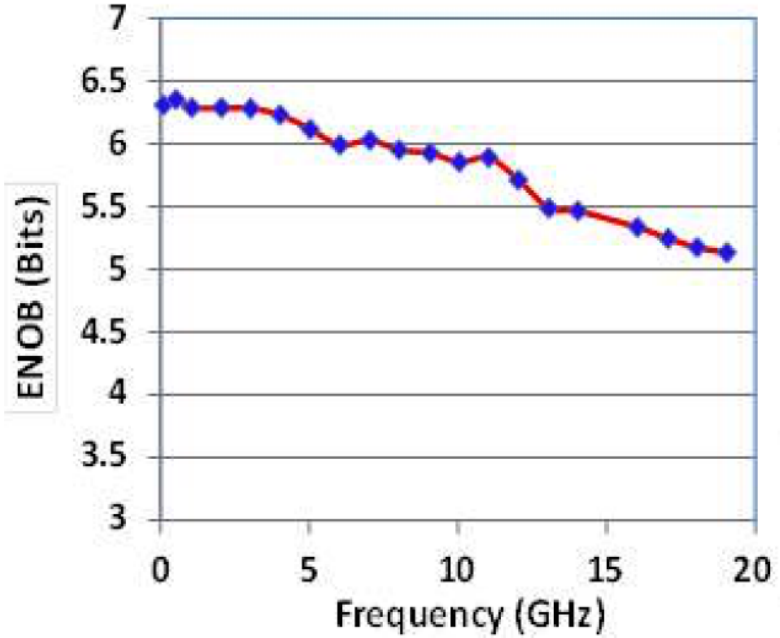
After Calibration

Broadcom 4 x 64GS/s 8-bit ADC in 20nm CMOS

- 5.95b ENOB @ 8GHz,
- 5.3b ENOB @ 16GHz
- Power dissipation of each 64GS/s ADC : 950mW
- 128 ADC interleaved
  - Each operating 500 MS/s
- Timing skew adjustment circuit with coarse and fine tuning
- On-chip calibration loops are used to cancel the gain, offset, and timing skew
- Foreground calibration of comparator offset
- Bandwidth mismatches not calibrated



[Broadcom, ISSCC 2017]



Conclusions

- Time-interleaving is an effective way to design high-sampling-rate ADCs
- ADCs have been design in CMOS with sampling rate approaching 100GS/s
  - Analog and Digital Calibration for inter-channel mismatches calibration
  - Front-end high-speed T/H
  - Sub-ADCs operating at low power and GS/s

Acknowledgement

- Thank You!

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