SÜSS MicroTec

Lithography for Wafer Level Packaging for LED Manufacturing

Tim McCrone
Applications Engineer

SUSS MicroTec
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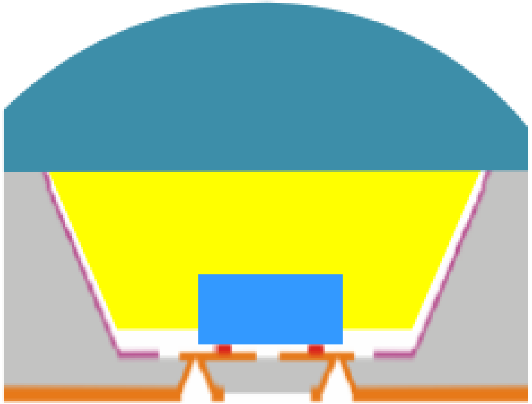

INTRODUCTION

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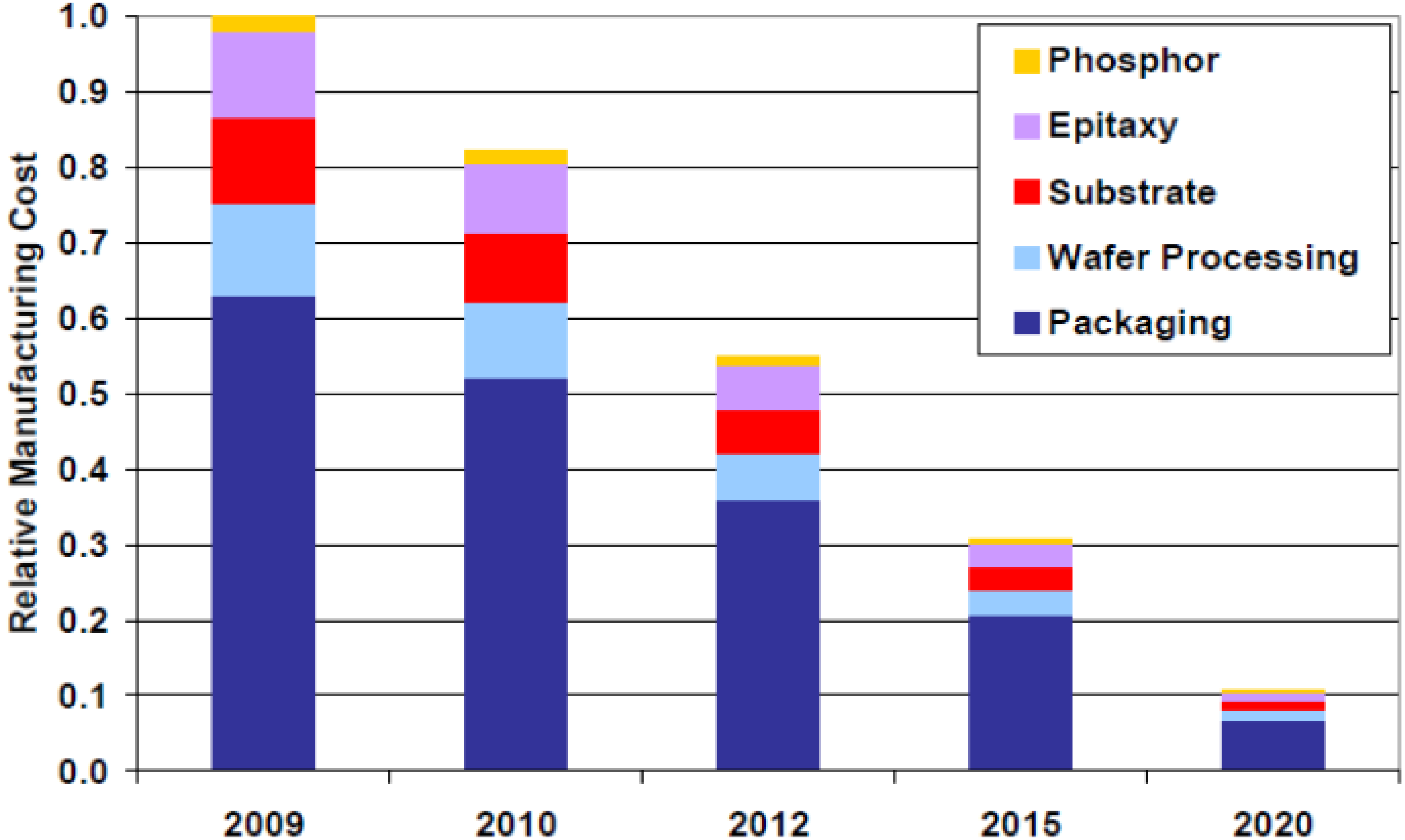
LED designs trends toward higher efficiency and brightness at a lower cost.

The primary cost of LED electronics is found in the packaging of the material.



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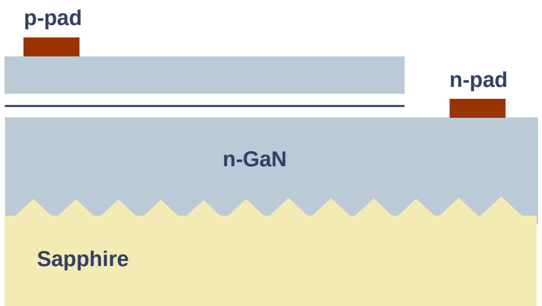


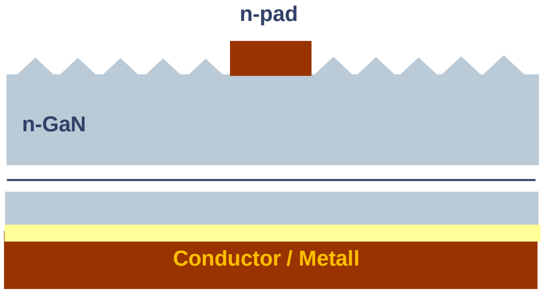
Conventional LED device with patterend sapphire substrate (PSS) (essentially all LED chip makers)

+ Relatively inexpensive

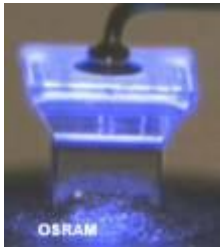
- Up to 30% active surface lost to the Mesa

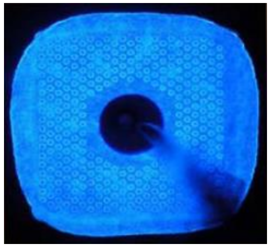
- Transparent or small contact needed on the p-side

- Current crowding due to poor conductivity of n-GaN increase total resistance



Thin-film vertical LED device with n-GaN texturing with substrate removal (Osram, Lumileds, Semileds, Cree, Luminus)





- Complexity and Cost

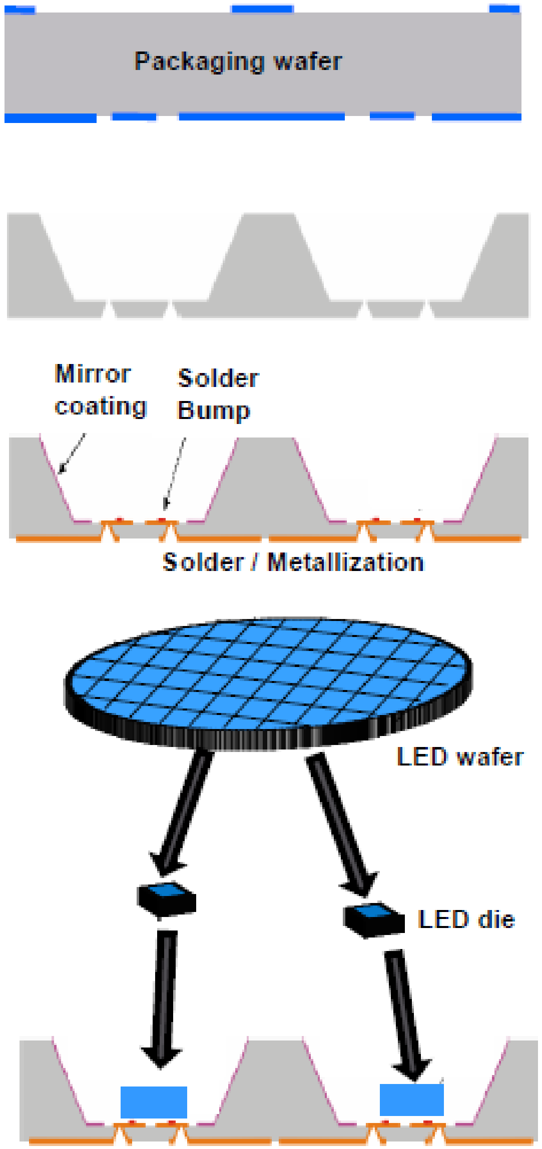
+ Good thermal properties

+ Larger active area (no MESA)

+ n-GaN can be thinned down to bring active layer close to the surface and improve light extraction (surface emitter)

+ Lower resistance

INTRODUCTION

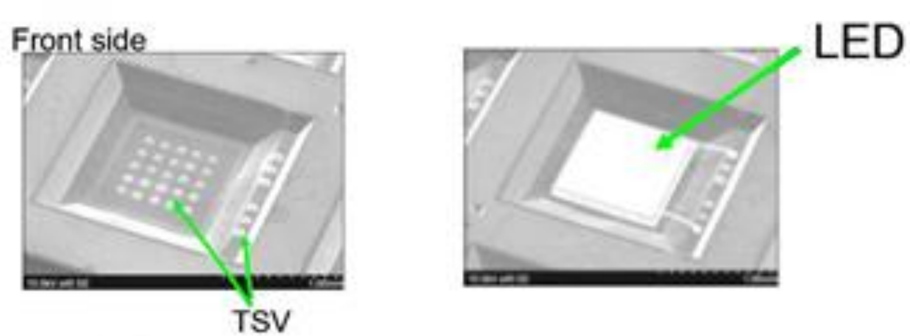


Advantages of wafer level packaging:

Small form factors
Excellent scalability to larger wafer sizes

Challenges with wafer level packaging:

Conformal coating
Exposure in deep vias and grooves
TSV creation and isolation



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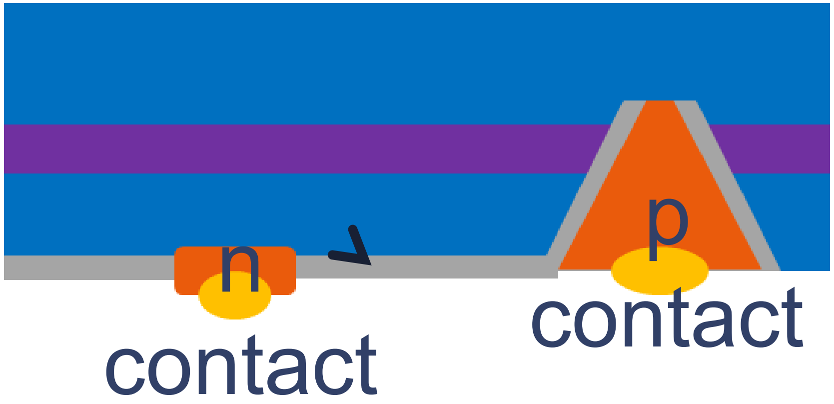
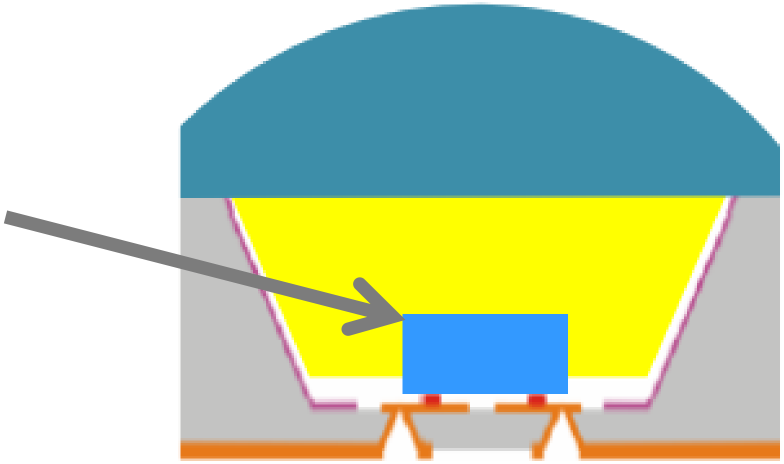
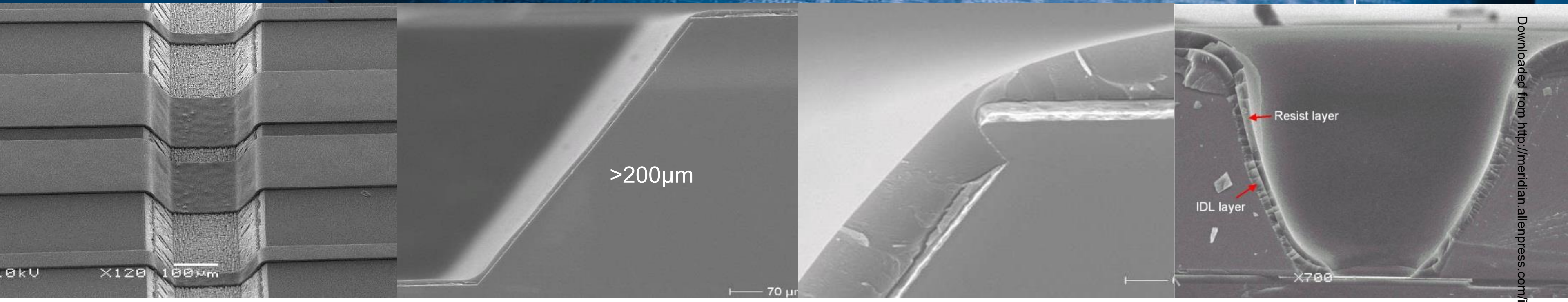
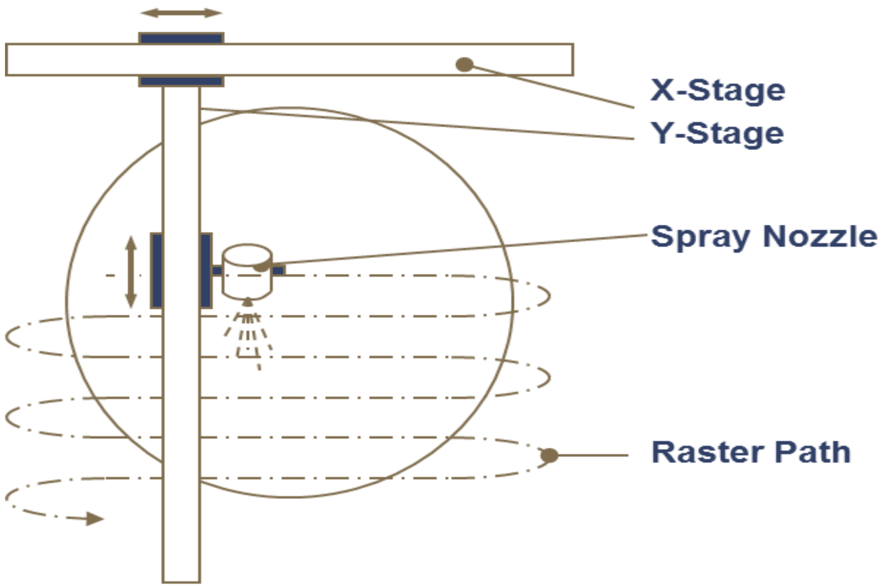
Using vias in LED device structure and packaging introduces the challenge of being able to coat and pattern in high aspect ratio structures

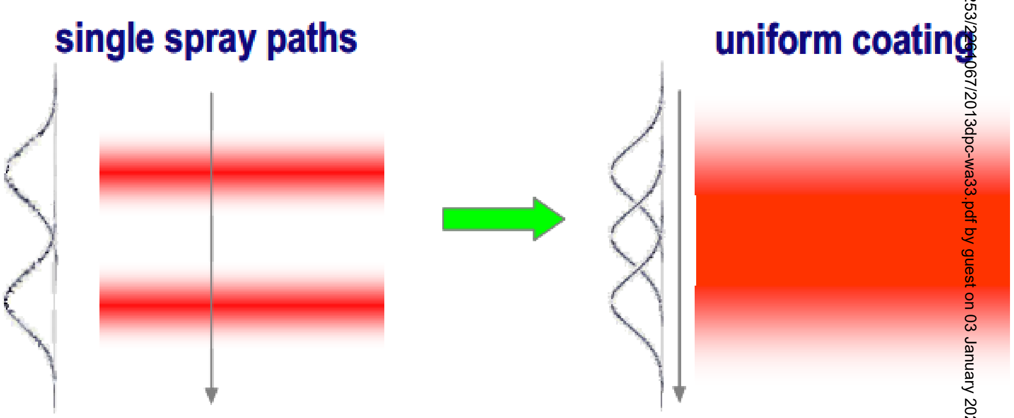




SPRAY COATING







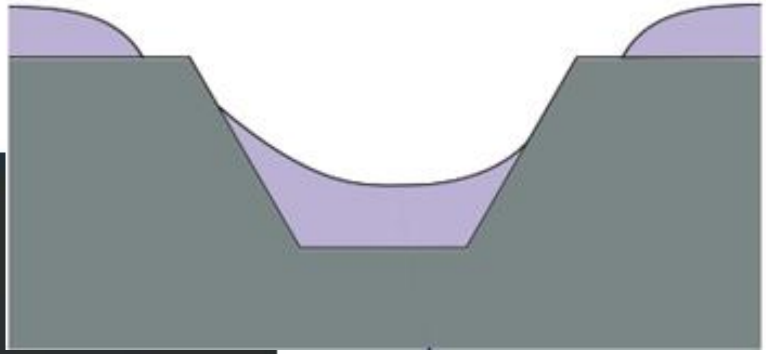
SPRAY COATING: COMPARISONS

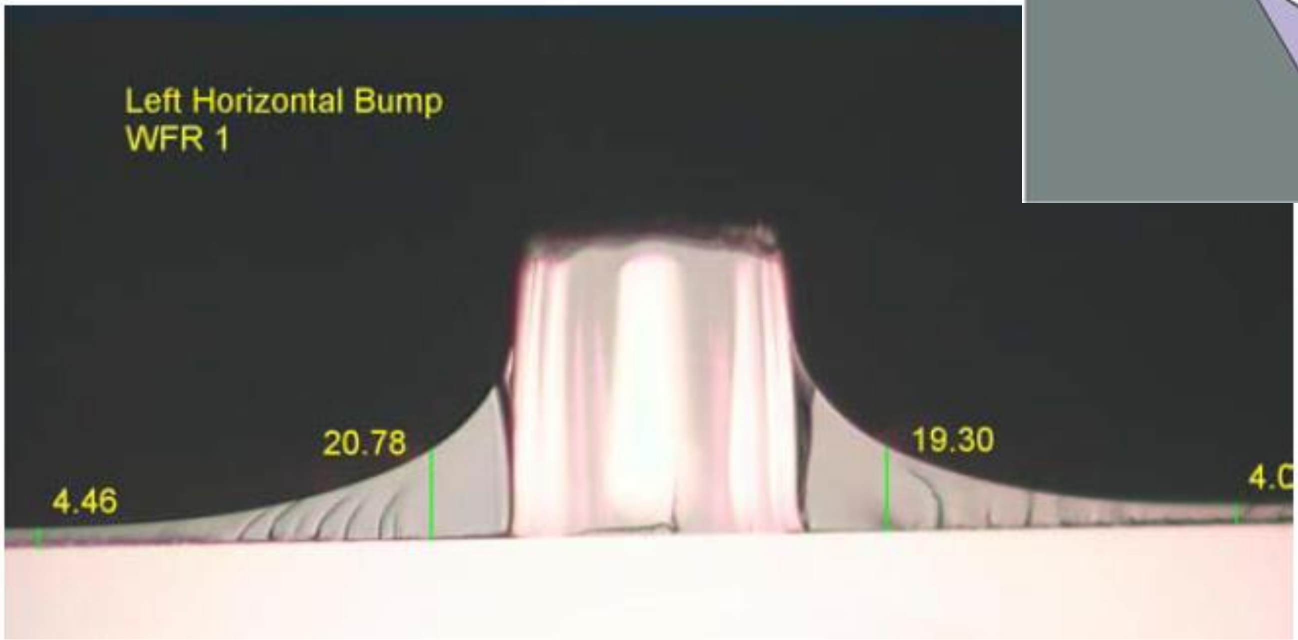
Spin Coating over Topography:

Easy to set up for small topography steps

Higher throughput

High aspect ratio structures cannot be coated due to gravity and surface tension





SPRAY COATING: COMPARISONS

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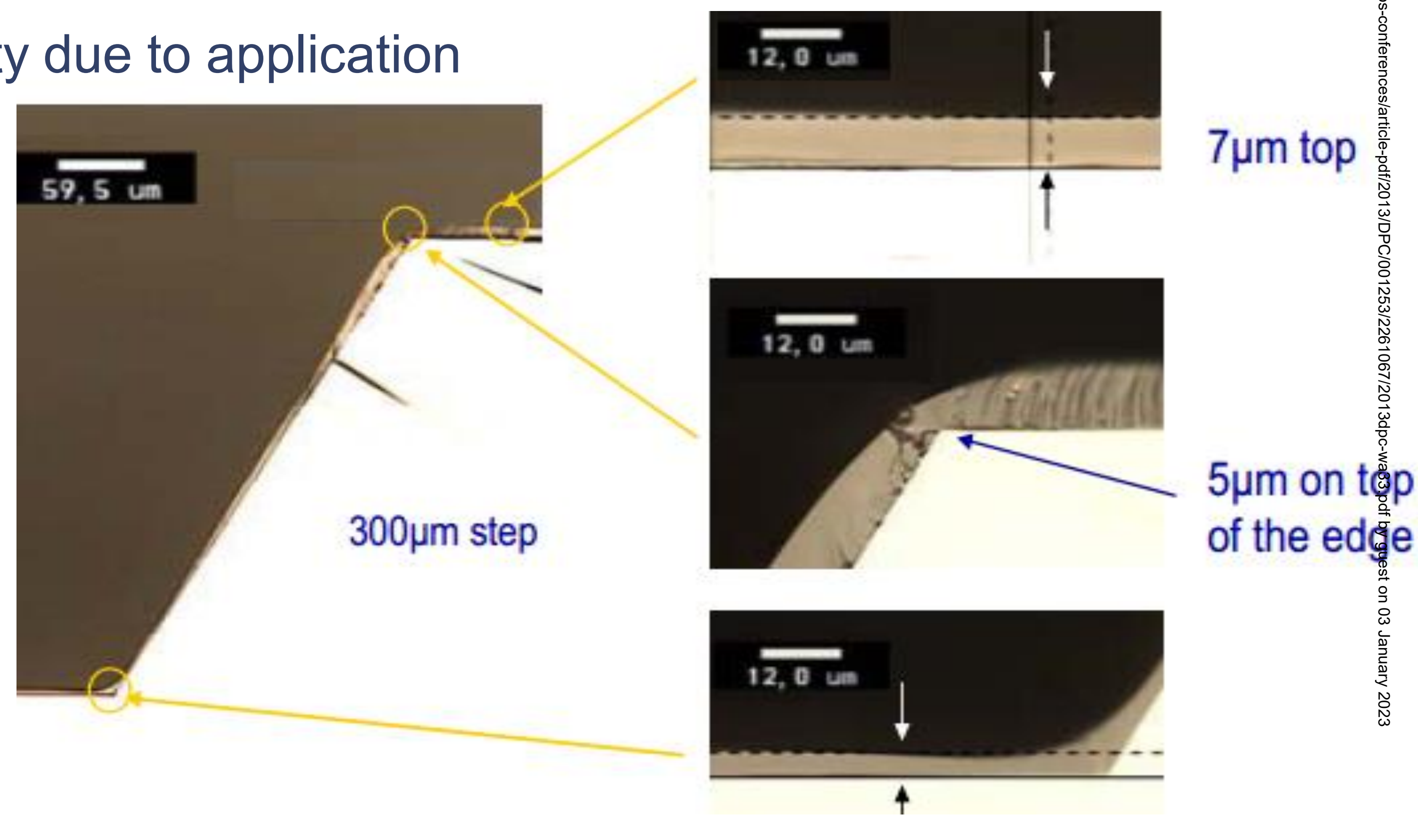
Spray Coating over Topography:
Reliable coverage at corners, in trenches and grooves

Higher material utilization fraction than spin coating

Great film uniformity due to application method



SPRAY COATING: AZ4999 DNQ/NOVOLAK

SPRAY COATING NEGATIVE RESISTS: SU8-3050

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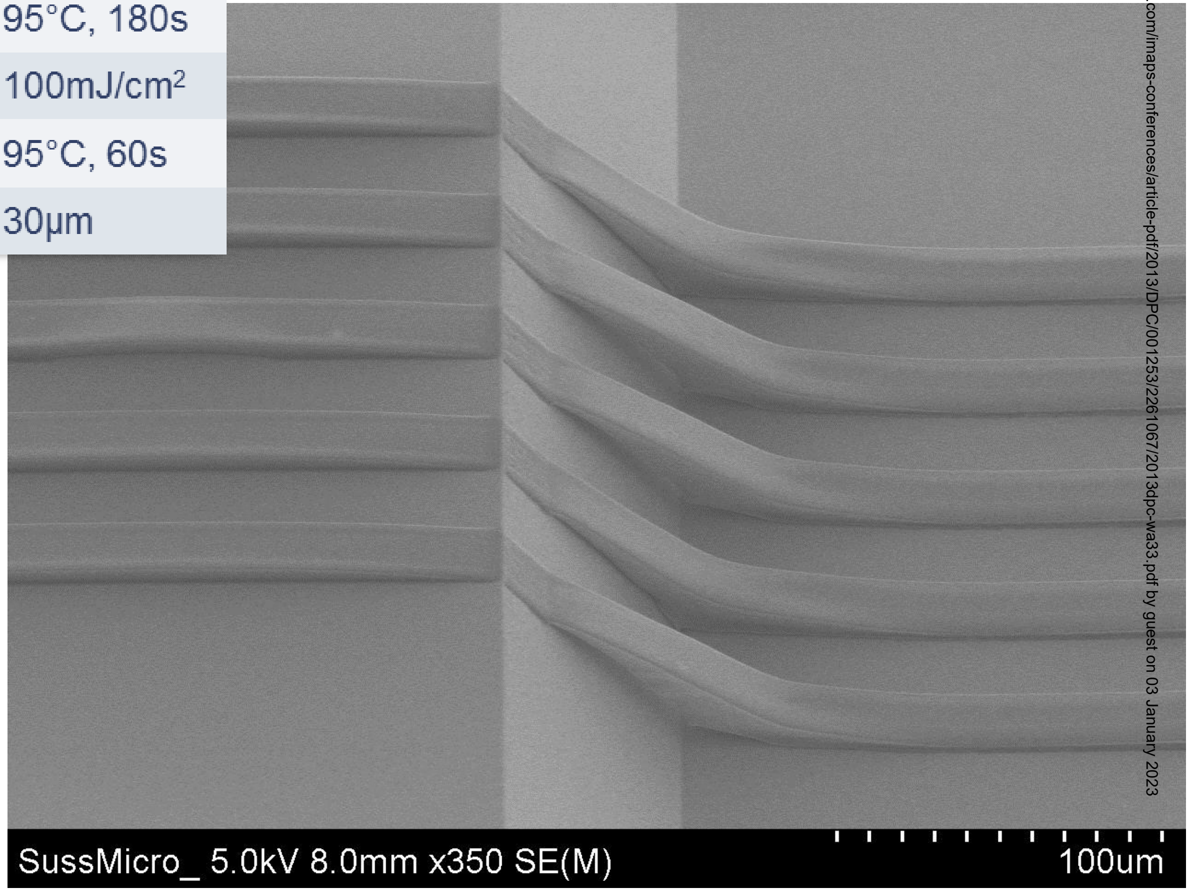
SU8-3050 (diluted)	
Cavity depth (KOH etched):	100µm
Cavity width / length:	4,000µm
Film Thickness (top / bottom):	5µm
Softbake:	95°C, 180s
Exposure Dose:	100mJ/cm^2
Post Exposure Bake (PEB):	95°C, 60s
CD of L/S Resolution Pattern:	30µm



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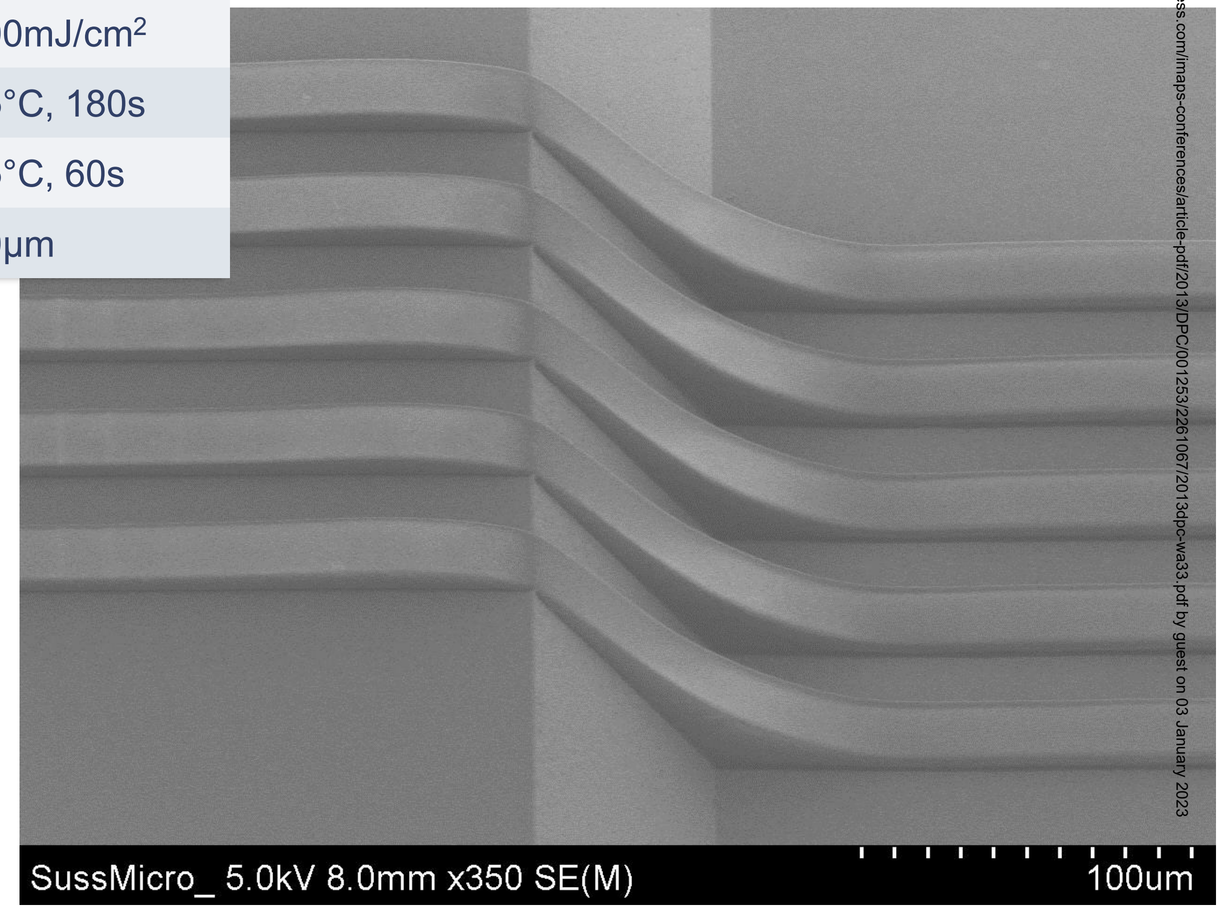
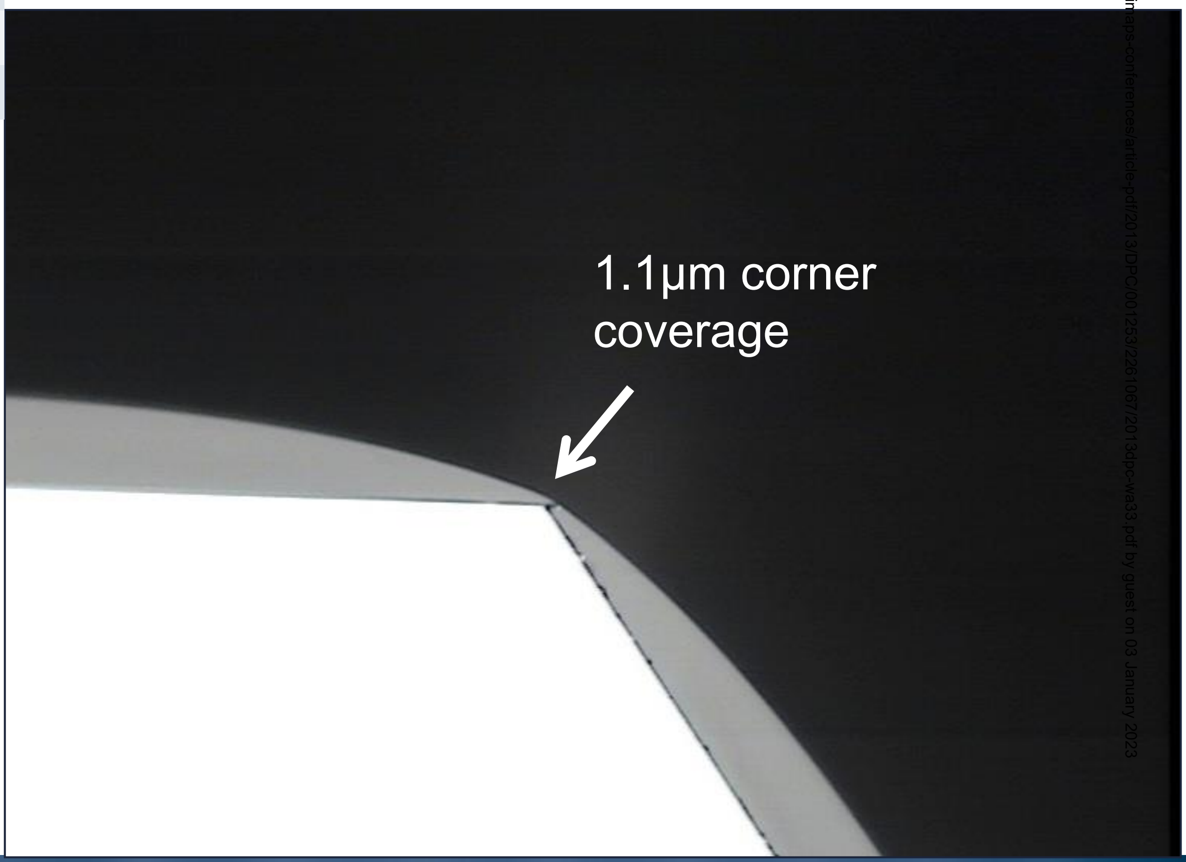


SPRAY COATING NEGATIVE RESISTS: SU8-3050

SU8-3050 (diluted)	
Cavity depth (KOH etched):	100µm
Trench width:	800µm
Film Thickness (top / bottom):	5µm
Exposure Dose:	250mJ/cm^2
Softbake (after exposure):	95°C, 180s
Post Exposure Bake (PEB)	95°C, 60s
CD of L/S Resolution Pattern:	Flood Exp.



SPRAY COATING: EXAMPLE WHY NEGATIVE SPRAY RESIST IS IMPORTANT

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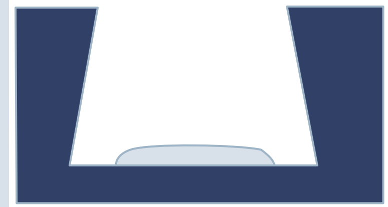
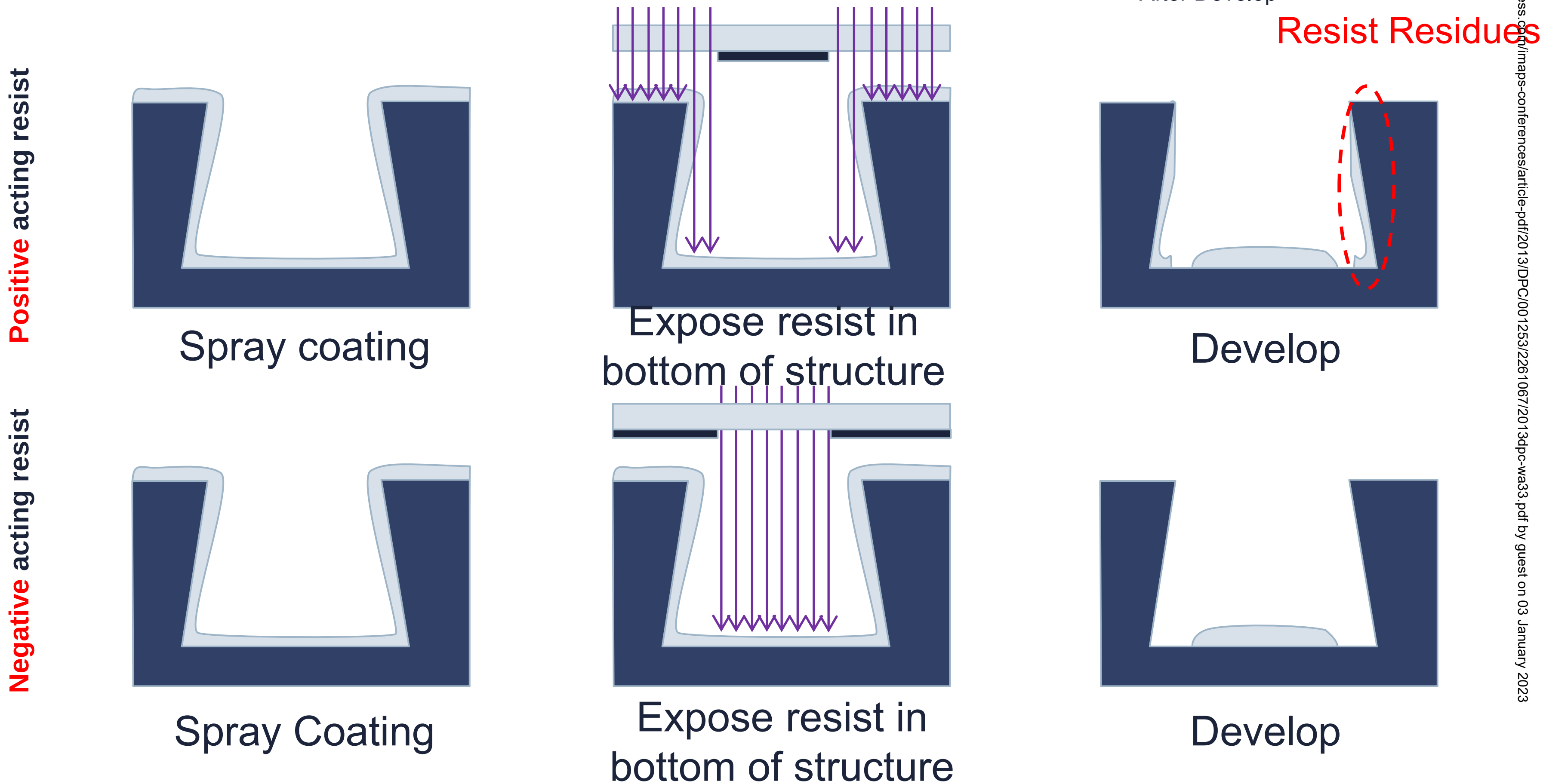
Goal:

Topography: Negative slope

Resist structures: Only in the bottom of cavity





SPRAY COATING: SPIN-ON DIELECTRICS

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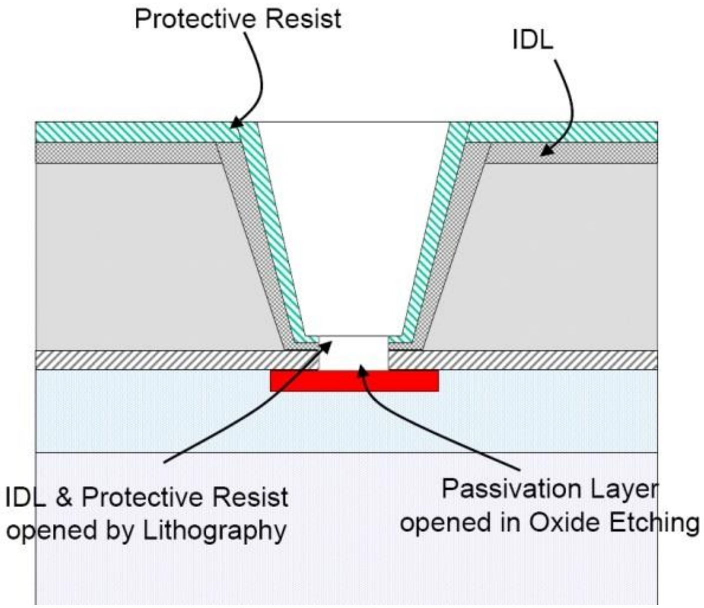
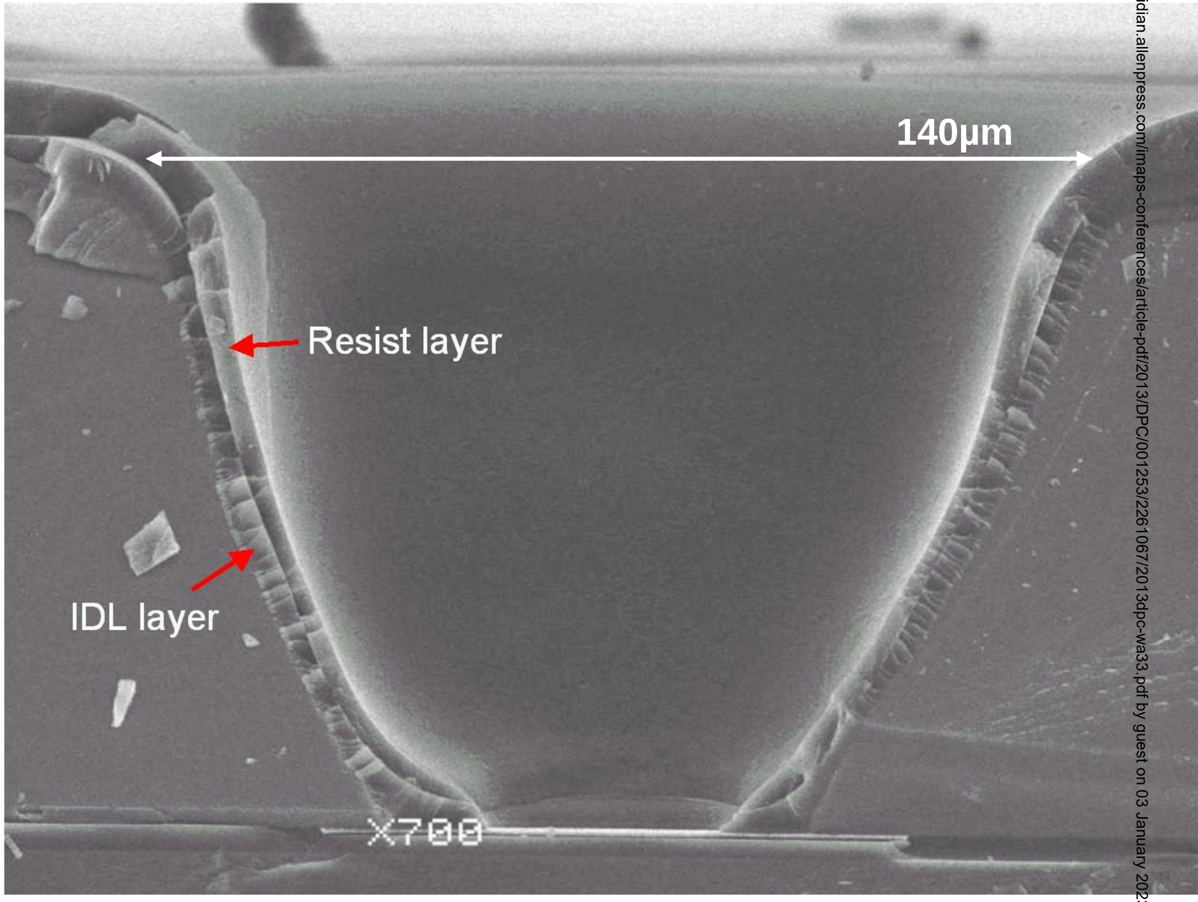
Material	Supplier	Polymer Type	Developer
HD 4100	HD Microsystems	Polyimide	Org. Developer
Durimide 7005	Fujifilm	Polyimide	Org. Developer
Cyclotene 4024-40	Dow Chemical	BCB	Org. Developer
Intervia 8023	Rohm & Haas	Epoxy / Novolak	TMAH (aq)

Material	Supplier	Polymer Type	Developer
WPR-5200	JSR Micro	Phenolic Resin	TMAH (aq)
HD8820	HD Microsystems	PBO	TMAH (aq)
CRC-8600	Sumitomo Bakelite	PBO	TMAH (aq)
PW-1200	Toray Industries	Polyimide	TMAH (aq)
Cyclotene P6505	Dow Chemical	BCB	TMAH (aq)

Generally, positive-acting passivation materials are more suitable for spray coating.

SPRAY COATING: COATING IN VIAS





Source: Schott OPTO WLP

EXPOSURE

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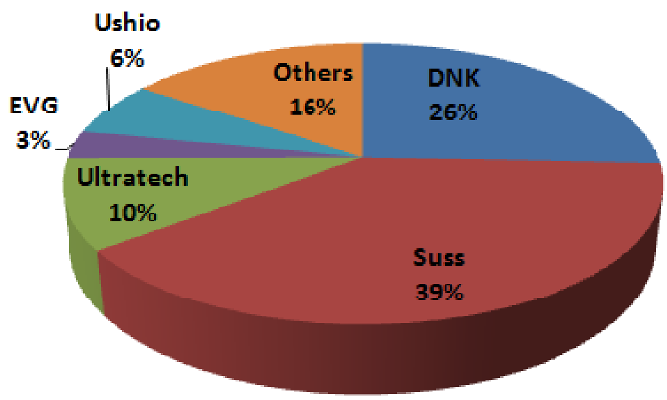
Proximity printing is a well established and cost efficient process in LED device manufacturing with more than 70% share

WLP generally has low pin counts with larger pads.

Aligners are optimized for resolution at specific proximities or contact

To achieve the highest resolution over a range of gaps in a device the light source must be shaped to achieve the best results

Relative Share of Installed LED Systems



Relative share of installed LED systems (over a total estimate of ~ 465 tools)

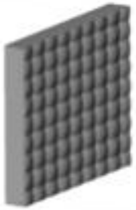
YOLE Développement July 2012

MO EXPOSURE OPTICS

Diffraction Reduction

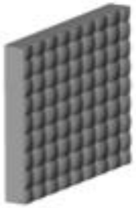
+Defines illumination settings by Illumination Filter Plate (IFP)

„Angle defining element“



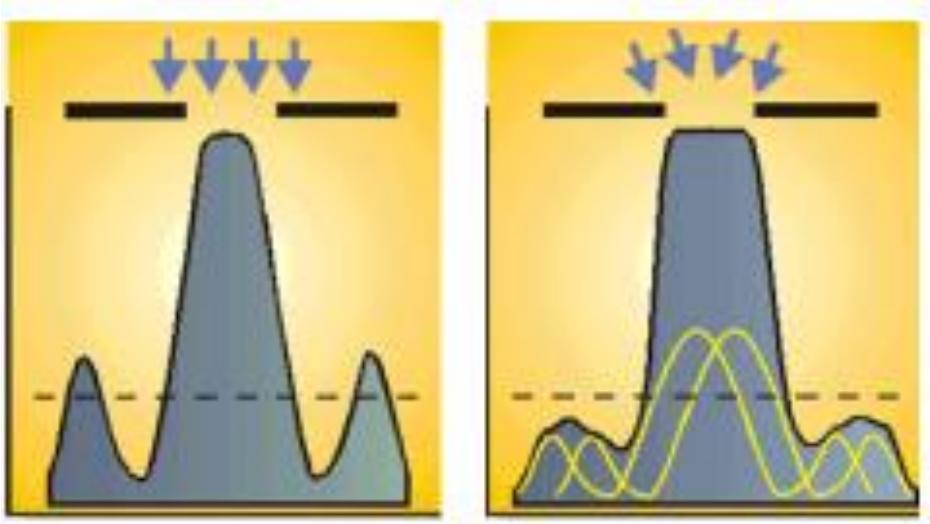
MO Integrator (1)

+Decouples illumination from lamp position



MO Integrator (2)

+Ensures uniform illumination of mask field



Parallel illumination causes high intensity second order effects

Using illumination from multiple angles at equal intensities reduces diffraction effects

MO EXPOSURE OPTICS

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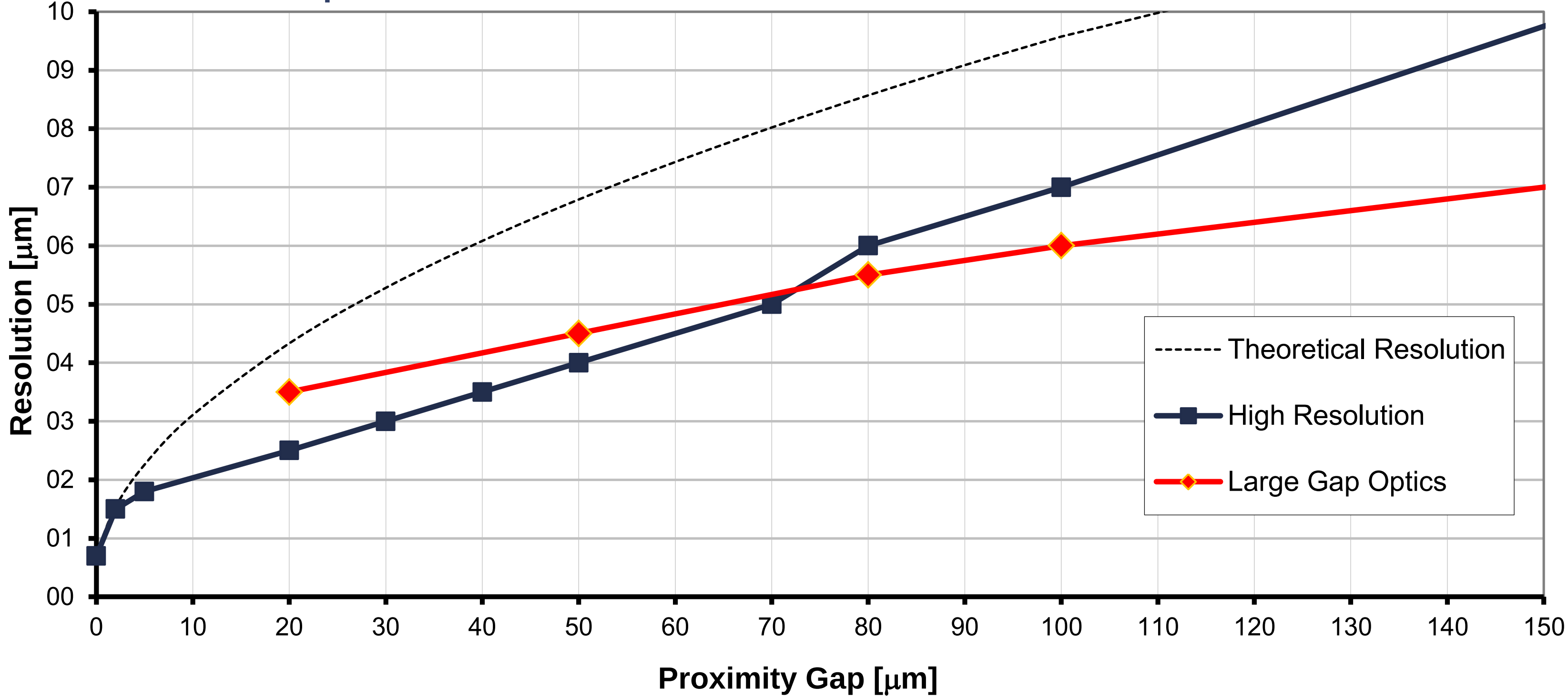
High stability of resolution over a larger depth of field allows for large exposure gaps, leading to fewer mask contamination defects

Diffraction limiting effects limits resolution loss over the depth of a device

Conventional optics are unable to do this



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CUSTOMIZED ILLUMINATION: CHANGING SOURCE SHAPE TO OPTIMIZE A PROCESS

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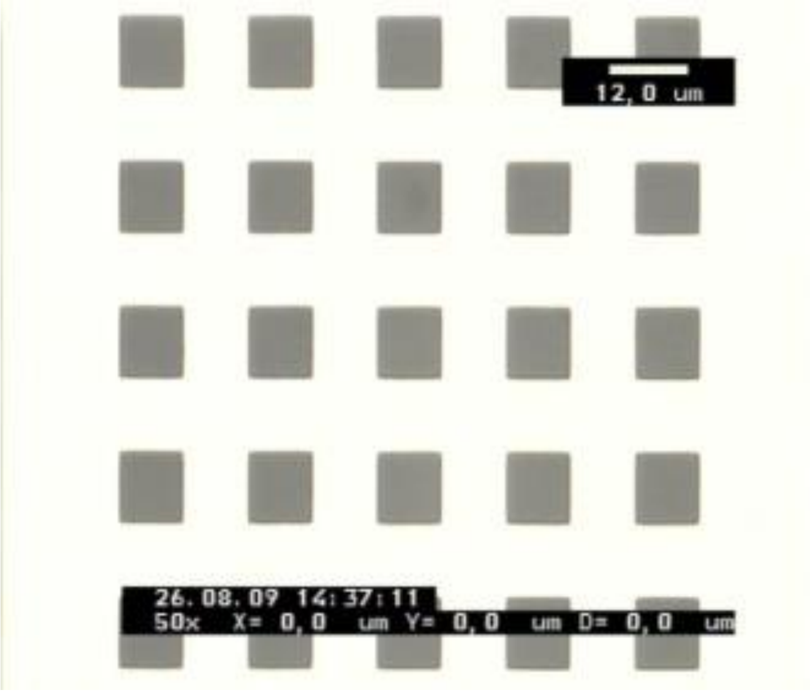
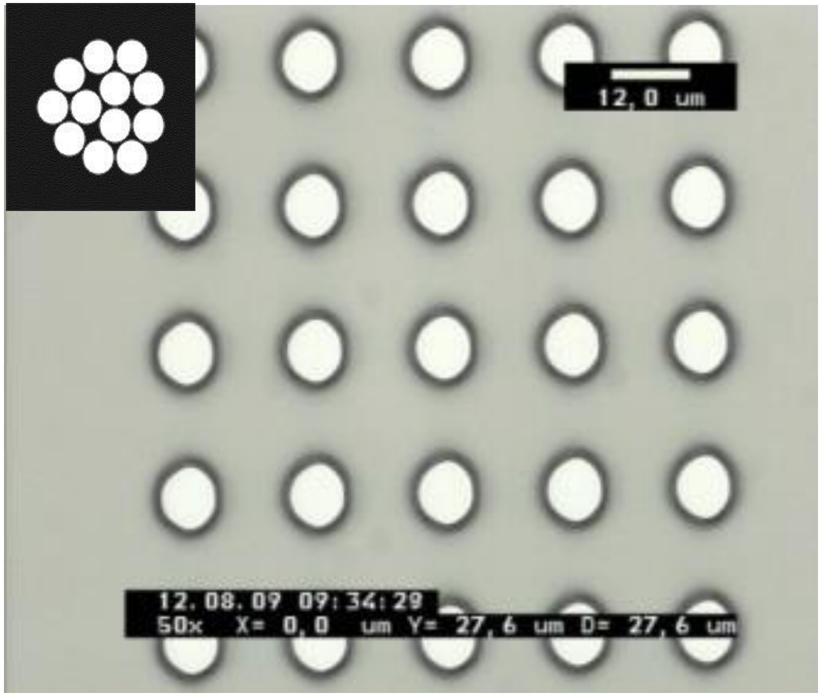
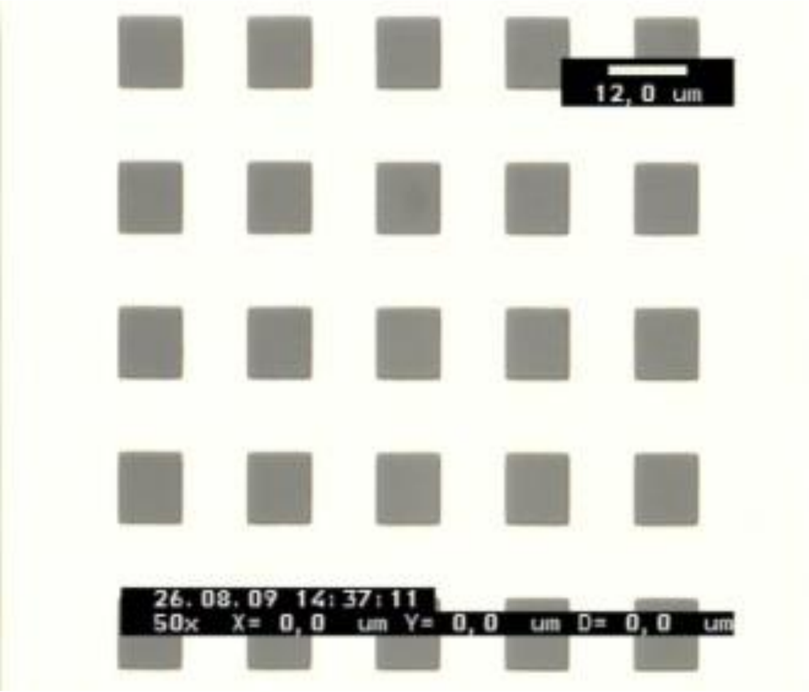


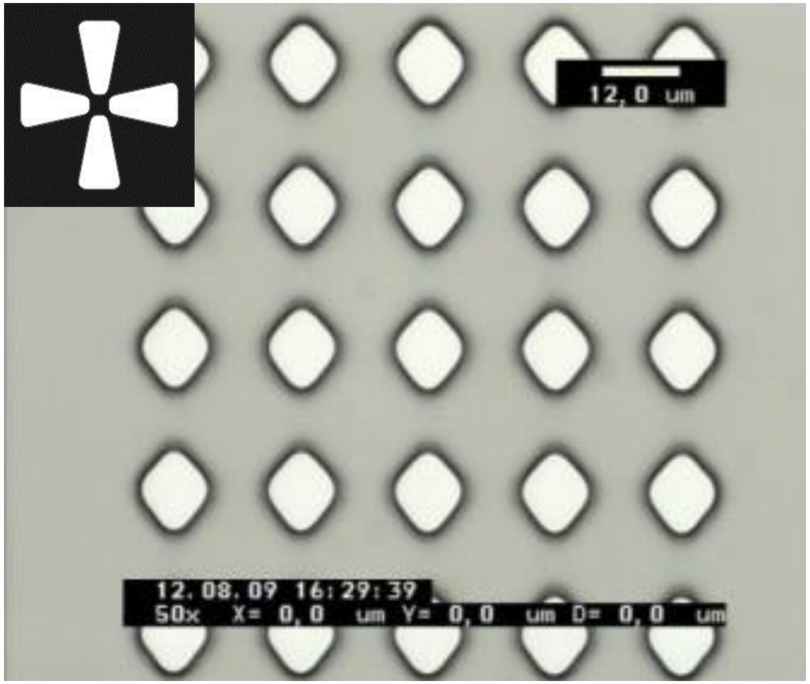


1.2µm thick resist (AZ 4110), 100µm Proximity Gap, SUSS MA8

IMAPS 9th International Conference & Exhibition on Device Packaging | March 11-14, 2013 | Fountain Hills, AZ

CUSTOMIZED ILLUMINATION: CHANGING SOURCE SHAPE TO OPTIMIZE A PROCESS





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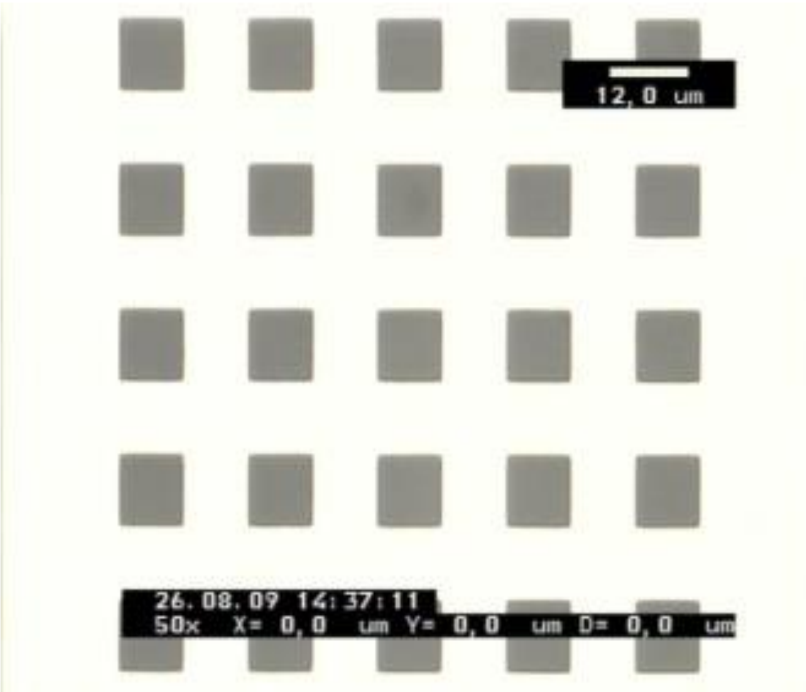
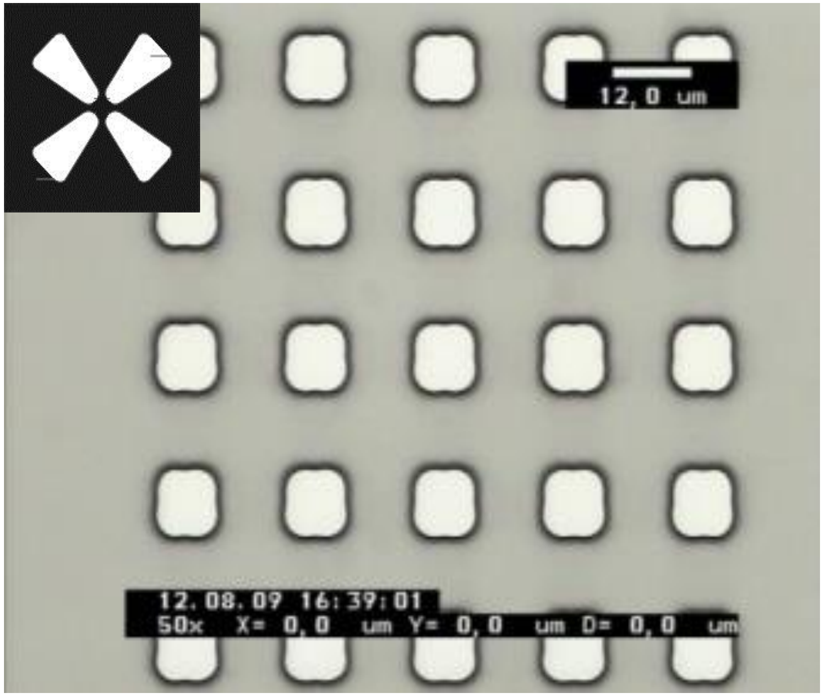
SÜSS MicroTec





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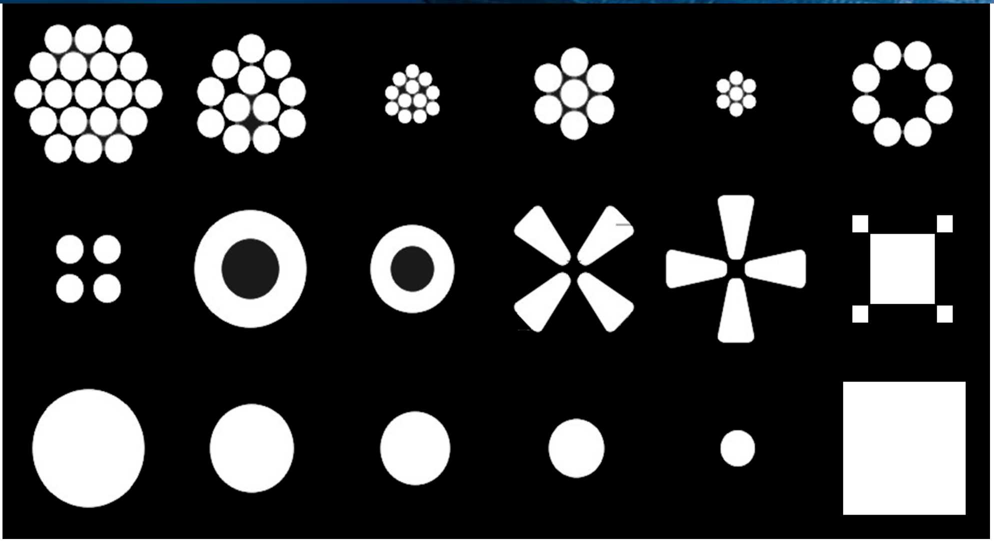
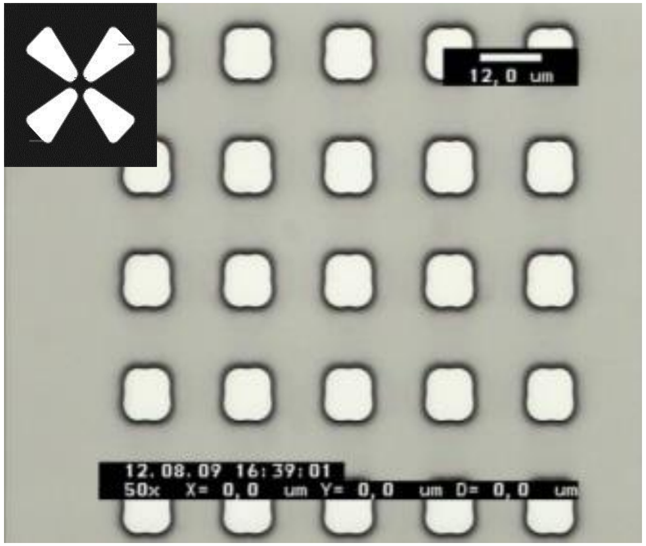
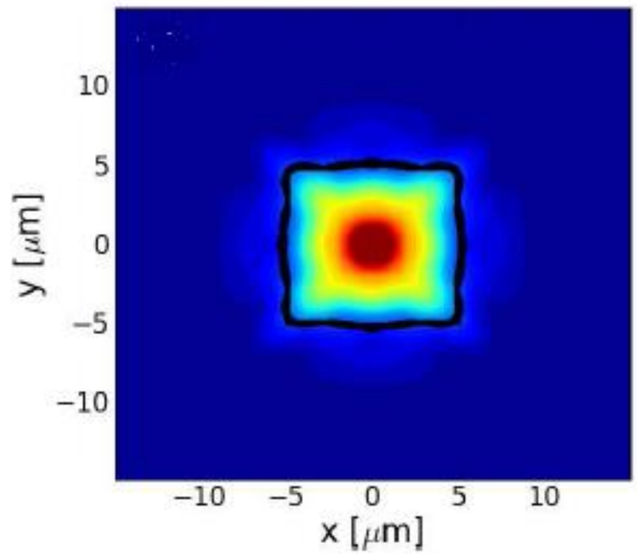


Large selection of illumination filter plates to optimize specific structures

GenISys is a powerful tool to help optimize the illumination source for a process





GENISYS SOFTWARE

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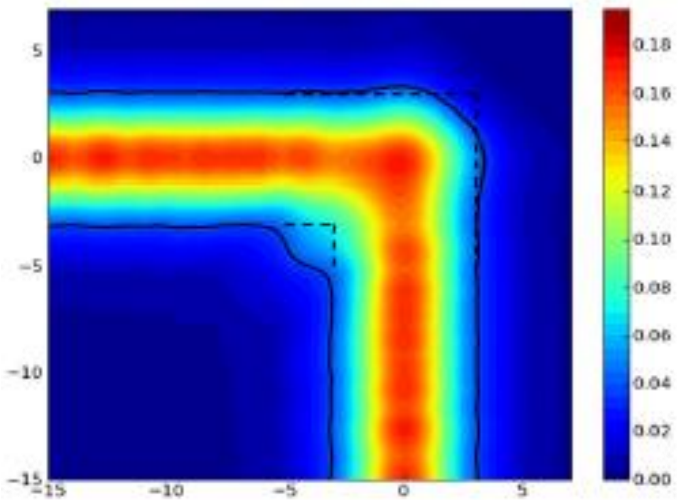
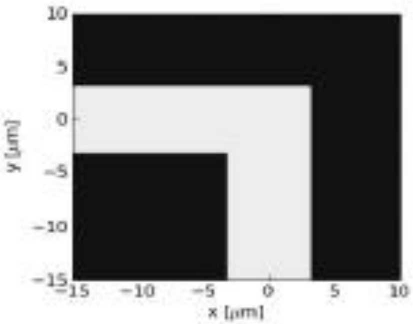
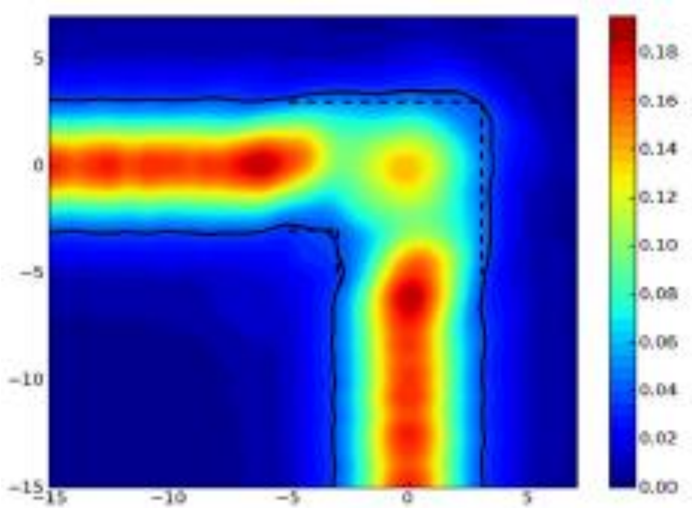
Aerial image (simulation)

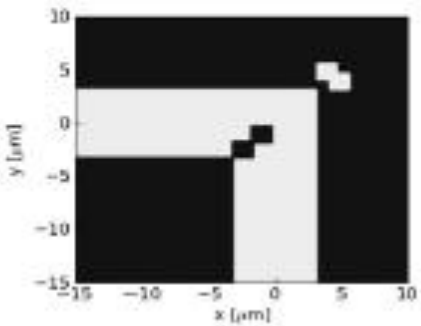




Mask pattern

GenISys also assists with corrective features in mask design





OPC assist features

SUMMARY

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Spray coating of both negative and positive acting dielectrics and photoresists allows for the patterning of 3D structures on a wafer and the isolation of TSVs.

Aligners can be used for patterning of packaging wafers and for creation of LEDs.

GenISys software quickly optimizes processes without use of lab time or trial masks