Chiplets Heterogeneous Integration on High-Density Hybrid Substrate Using an Interconnect-Layer

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Abstract
In this study, a high-density organic hybrid substrate for chiplets heterogeneous integration is investigated. Emphasis is placed on the design, materials, process, fabrication, and characterization of the hybrid substrate with an interconnect-layer. A non-linear finite element analysis is performed to show the state of stress at the vias filled with a conductive paste of the interconnect-layer.

Key words
Chiplets, heterogenous integration, hybrid substrate, interconnect-layer, Fan-out panel-level chip-last

I. Introduction

For 2.1D IC integration, thin film layers (the coreless substrate) with fine metal line width (L) and spacing (S) are fabricated on the top-layer of a build-up package substrate and become a hybrid substrate [1-5]. In this case, the yield loss of the hybrid substrate, especially the fine metal L/S coreless substrate is difficult to control and can be very large. For 2.3D IC integration, the fine metal L/S substrate (or interposer) and the build-up package substrate are fabricated separately [6-15]. After that, the fine metal L/S substrate and the build-up package substrate are interconnected into a hybrid substrate through the solder joints which are enhanced with underfill. In this case, the yield loss of the hybrid substrate especially the fine metal L/S coreless substrate is easier to control and smaller.

In this study, the fine metal L/S substrate and the build-up package substrate or high-density interconnect (HDI) are also fabricated separately, and then they are combined through an interconnect-layer. This is very similar to 2.3D IC integration except the solder joint and underfill are eliminated, which are replaced by an interconnect-layer.

The interconnect-layer is about 60μm-thick, which consists of the prepreg and vias (100μm-diameter on top and 80μm-diameter at the bottom) filled with conductive paste and are in β-stage. The fine metal L/S coreless substrate (37μm-thickness) is fabricated by a PID (photoimageable dielectric), LDI (laser direct imaging) and development, PVD (physical vapor deposition), photoresist and LDI, Cu-plating, etc. on a temporary glass carrier. The minimum metal L/S, pad pitch, and pad diameter for the chips are respectively, 2/2μm, 60μm, and 35μm. The HDI is an 8-layer substrate with 1mm-thickness. The pad pitch and pad diameter are respectively 350μm and 300μm. The final assembly of these 3 separate substrates is by thermal compression and the interconnect-layer is then fully cured (C- stage).

Characterizations such as continuity check is performed to make sure at least the design and fabrication are correct. Optical microscope (OM), x-ray, and scanning electron microscope (SEM) of the cross-section of the hybrid substrate is performed to check the quality of metal and dielectric layers of the fine metal L/S coreless substrate, the integrity of the conductive paste in the vias, and the delamination of the interconnect-layer. A non-linear finite element analysis is performed to show the state of stress at the vias filled with the conductive paste.

II. High-Density Hybrid Substrate for Chiplets Heterogeneous Integration

Figure 1 schematically shows the top-view and cross-section view of a heterogeneous integration on a high-density organic hybrid substrate. It consists of four major parts: (a) the chips with microbumps, (b) the fine metal L/S redistribution-layer (RDL) substrate or interposer (~37μm), (c) the interconnect-layer (~60μm), and (d) the high-density interconnect (HDI) printed circuit board (PCB) (~1mm) as shown in Figure 2.

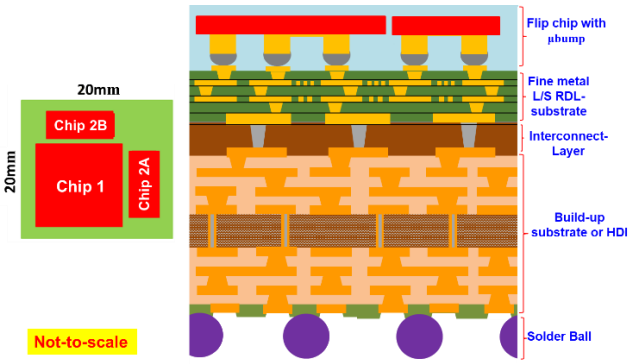


Fig. 1 Top-view and cross-section view of chiplets heterogeneous integration on hybrid substrate.

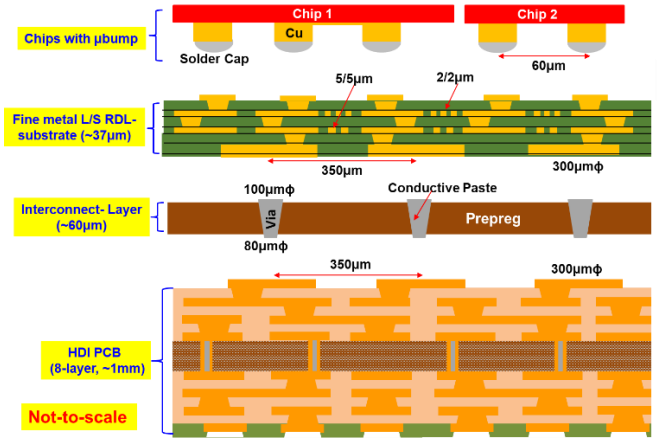


Fig. 2 Key parts of the test package.

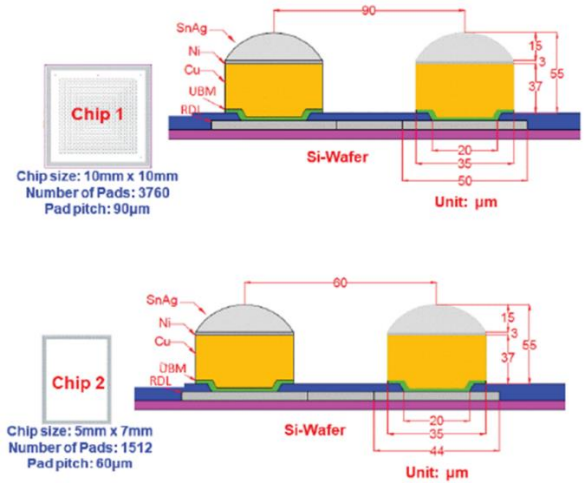
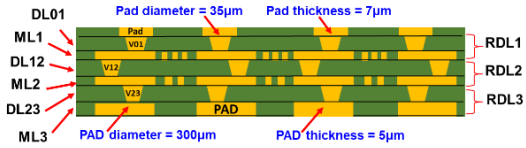


Fig. 3 Schematic of the test chips.

II(a) Test Chips

The test chips for this study are shown in Figure 3. It can be seen that the size of the large chip (Chip 1) is 10mm x 10mm with 3,760 area array pads on 90µm-pitch and are daisy chained. The Cu pad size is 50µm x 50µm. The size of the small chips (Chip 2A and Chip 2B) is 7mm x 5mm with



RDLs	Key Elements of RDL	Line width/ Spacing (L/S)	Thickness (H)	Via Dia. (T/B)
RDL1	ML1 (Metal layer 1)	2/2µm	2.5µm	NA
	DL01 (Dielectric layer between Pad and ML1)	NA	7.5µm	NA
	V01 (Via opening between contact Pad and ML1)	NA	NA	17/10µm
RDL2	ML2 (Metal layer 2)	5/5µm	3.5µm	NA
	DL12 (Dielectric layer between ML1 and ML2)	NA	6.5µm	NA
	V12 (Via opening between ML1 and ML2)	NA	NA	32/25µm
RDL3	ML3 (Metal layer 3) (PAD)	NA	5µm	NA
	DL23 (Dielectric layer between ML2 and ML3)	NA	5µm	NA
	V23 (Via opening between ML2 and ML3)	NA	NA	32/25µm

Fig. 4 Fine metal L/S 3-layer RDL-substrate.

1,512 area array daisy chained pads on 60µm-pitch and the Cu pad size is 44µm x 44µm. For all the chips, the Ti/Cu (0.1/0.2µm) UBM (under bump metallurgy) pad size is 35µm-diameter, the passivation (PI2) opening is 20µm-diameter, the Cu-pillar is 35µm-diameter and 37µm-tall, the SnAg solder cap is 15µm with a barrier (Ni = 3µm).

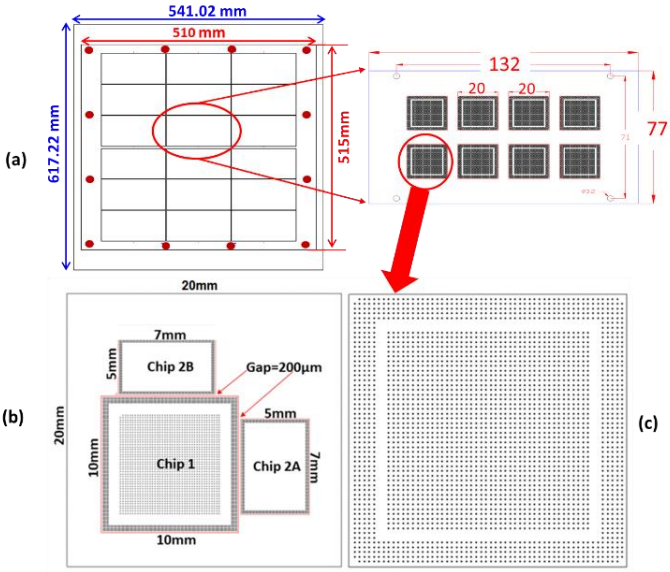


Fig. 5 (a) Panel for making the RDL-substrates. RDL-substrate: (b) Top-view and (c) Bottom-view.

II(b) Fine Metal L/S RDL-Interposer

There are three RDLs in the RDL-substrate and each RDL consists of one metal layer (ML) and one dielectric layer (DL). Figure 4 shows the definition and value of RDLx, MLx, DLxy, Vxy, and L/S/H. It can be seen that the L/S/H of ML1 are 2/2/2.5µm and ML2 are 5/5/3.5µm. ML3 is the contact PAD with a diameter = 300µm and a thickness = 5µm. The thickness of dielectric layers DL01, DL12, and DL23 are respectively 7.5µm, 6.5µm, and 5µm.

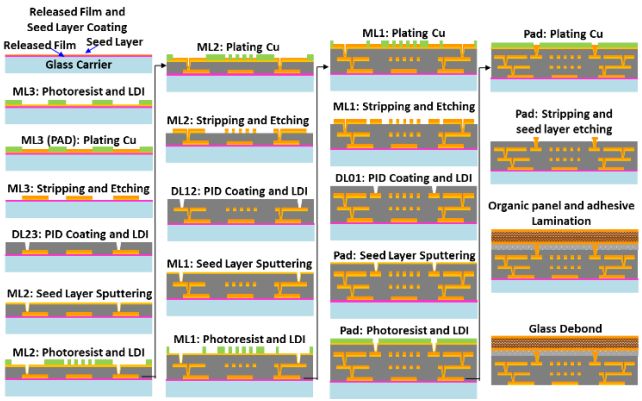


Fig. 6 **Key process steps in making the RDL-substrate.**

The temporary panel for fabricating the RDL-substrate is shown in Figure 5(a). It can be seen that the panel size is 515mm x 510mm x 1.1mm and is made of glass with a coefficient of thermal expansion (CTE) equals to $8.5x10^{-6}$/ºC. The panel is divided into 18 strips and each strip (132mm x 77mm) has 8 (20mm x 20mm) RDL-substrates. Thus, in one shot, it can make RDL-substrates for 432 chips in 144 heterogeneous integration packages. Figures 5(b) and (c) show the top-side and bottom-side of an individual hybrid substrate. On the top-side, there are 2 x 1,512 + 3,760 = 6,784 pads, Figure 5(b), which are for bonding the chips to the fine metal L/S RDL-substrate. On the bottom-side, there are 2,780 Cu pads (300µm-diameter) on 350µm-pitch, Figure 5(c). These pads are for the interconnection of the interconnect-layer.

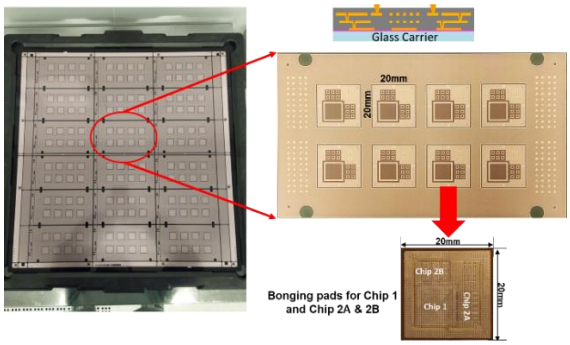


Fig. 7 **Glass panel for making the RDL-substrate.**

The key process steps in fabricating the fine metal L/S RDL-substrate are shown in Figure 6. First, a released film (sacrificial layer) is slit coated on a temporary glass carrier (515mm x 510mm) and then a Ti/Cu seed layer is formed by PVD. It is followed by photoresist, LDI and development. Then, ECD (electrochemical deposition) Cu and strip off the photoresist and etch off the Ti/Cu to obtain the metal layer (ML3 or PAD) of RDL3. It is followed by slit coating a PID and LDI to get the dielectric layer DL23 of RDL3. Then, sputter the Ti/Cu, photoresist, LDI and develop, and ECD the Cu. It is followed by stripping off the photoresist and

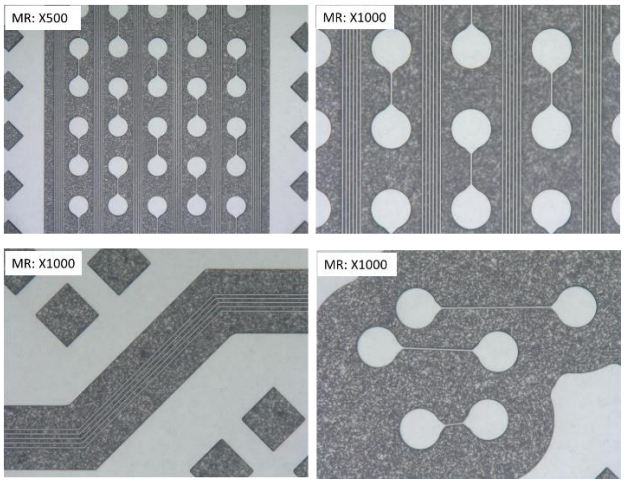


Fig. 8 OM images of the RDL-substrate (top-side).

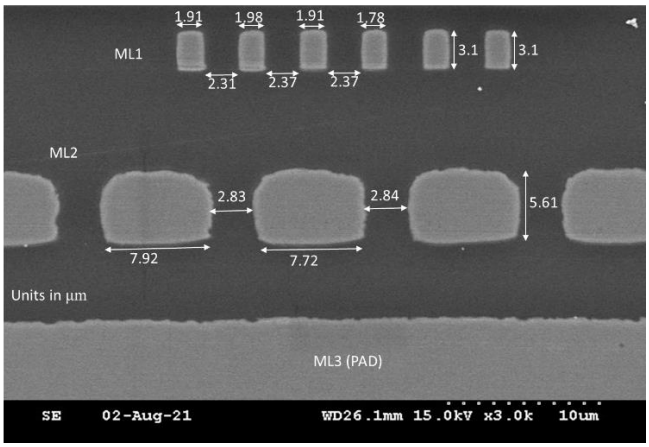


Fig. 9 Cross section SEM image of the RDL-substrate.

etching off the TiCu to get the metal layer ML2 of RDL2. Repeat the same process steps to obtain the metal layer ML1 of RDL1 and dielectric layers DL12 and DL01 of RDL2 and RDL1, respectively. Then, sputter the Ti/Cu, photoresist, LDI, and develop, and ECD the Cu. It is followed by stripping off the photoresist and etching off the TiCu to get the bonding pad (lead) for the chips. Figure 7 shows the panel with 144 3-layer (20mm x 20mm) RDL-substrates.

Figure 8 shows the OM images of the top-side of the (L/S = 2/2µm) RDL-substrate at 500 and 1000 times of magnifications. Figure 9 shows a typical SEM image of the cross section of the RDL-substrate. It can be seen that (a) for ML1, the line widths (L) are 1.91µm, 1.98µm, 1.91µm, and 1.78µm, which are close to the target (2µm), the line spacing (S) are 2.31µm, 2.37µm, and 2.37µm, which are reasonably close to the target (2µm), and the thicknesses (H) are 3.1µm and 3.1µm, which are close to the target (2.5µm), (b) for ML2, the L are 7.92µm and 7.92µm, which are not close to the target (5µm), the S are 2.83µm and 2.84µm, which are far from the target (5µm), and the H is 5.61, which is far from

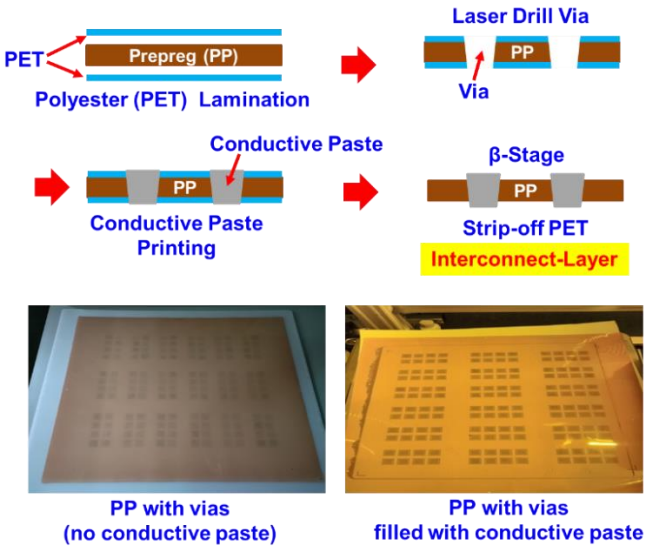


Fig. 10 Interconnect-layer (PP and paste are in β-stage).

the target (3.5μm), and (c) for ML3, the H is 8.31μm, which is also far from the target (5μm). Thus, there are rooms for improvements, e.g., a better estimation of the compensation of photoresist, LDI, ECD Cu, Cu etching, etc.

II(c) Interconnect-Layer

Figure 10 shows the interconnect-layer. First, laminate a polyester (PET) on both sides of a prepreg (PP). Then, laser drill vias and print conductive paste into vias. It is followed by stripping off the PET. Both the paste and PP of the interconnect-layer are in β-stage.

TABLE 1 HDI PCB MATERIALS AND SPEC.

Category	Layer	Material	Item	Diameter/ Width (μm)	Thickness (μm)
HDI	L1	Cu	Pad Dia.	300	22
		PP 1067	Bottom Dia.	100	55
	L2	Cu	Pad Dia.	200/400	25
		PP 1067	Bottom Dia.	250	60
	L3	Cu	Pad Dia.	400	17
		Core	MTH Dia.	250	254
	L4	Cu	Pad Dia.	400	17
		PP 1067	Bottom Dia.	250	55
	L5	Cu	Pad Dia.	400	17
		Core	MTH Dia.	250	254
	L6	Cu	Pad Dia.	400	17
		PP 1067	Bottom Dia.	250	60
	L7	Cu	Pad Dia.	200/400	25
		PP 1067	Bottom Dia.	100	55
	L8	Cu	Pad Dia.	200	22
		SR	Bottom Dia.	600	20
	HDI Total Thickness				975

II(d) HDI PCB

The 975mm-thick HDI PCB has eight layers (Figure 2 and Table 1) and is fabricated by the conventional process.

II(e) Final Assembly of the Hybrid Interposer

First, attach the fabricated RDL-substrate with the glass carrier to an organic panel with an adhesive, and then debond the glass carrier as shown in Figure 11. The key final assembly process steps (Figure 12) of these 3 substrates are by thermal compression. The alignments and correct positions of these three substrates are fixed by more than 10 nails around the four sides of these three panel substrates. After thermal compression (lamination), the PP and conductive paste of the interconnect-layer are fully cured (C-stage) and the nails are removed.

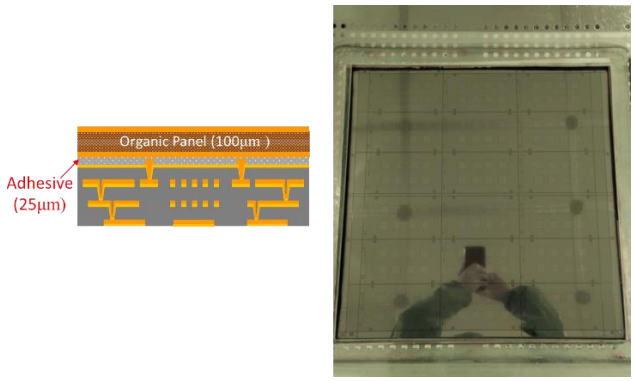


Fig. 11 Attach an organic panel to the RDL-interposer and debond the temporary glass carrier.

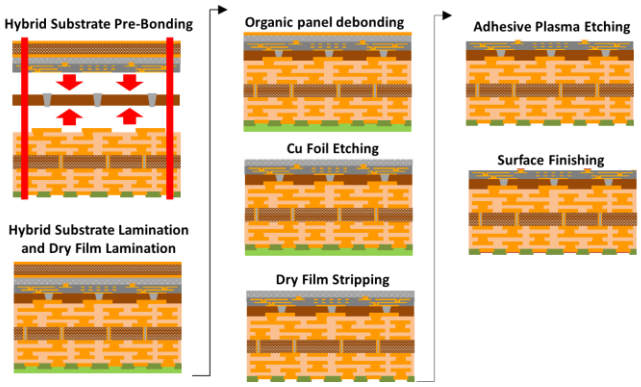


Fig. 12 Process steps in making the hybrid substrate.

It is followed by dry film lamination at the bottom of the hybrid substrate and then organic panel debonding. It is followed by dry film stripping, adhesive plasma etching, seed layer etching, and surface finishing.

III. Characterizations of the Hybrid Substrate

III(a) X-Ray and OM

Figures 13 and 14 show the OM and x-ray images of the fabricated hybrid substrate. Figure 13 shows a typical cross section of the hybrid substrate which consists of the fine metal L/S RDL-substrate, the interconnect-layer, and the HDI PCB. Figure 13 also shows the vias filled with the conductive paste nicely and there are not any obvious large void and delamination. The thickness of the interconnect-layer is 60μm, which is thinner than the C4 solder joint (usually 100μm) of the 2.3D IC integration.

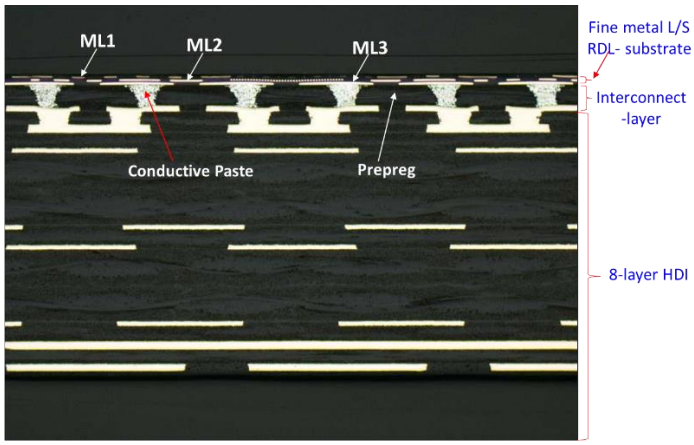


Fig. 13 A typical cross section of the hybrid substrate.

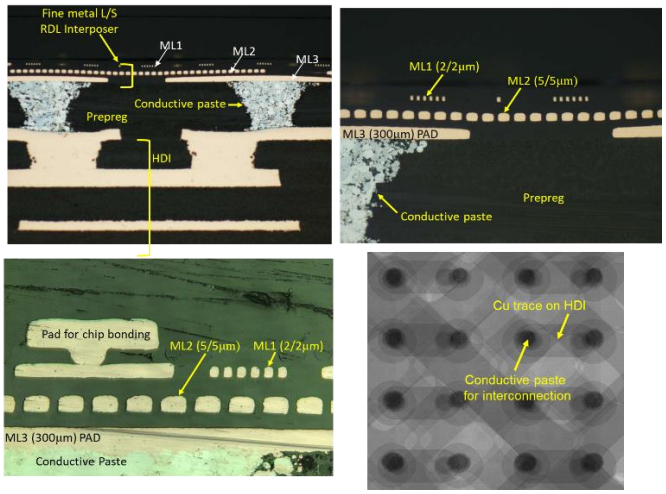


Fig. 14 Close-up views of the hybrid substrate.

Figure 14 shows the pad for chip bonding, the pads for interconnect-layer, the conductive paste, and ML1, ML2, and ML3 with their targets. Figure 14 also shows the x-ray image of the conductive paste, the contact pads, and the daisy-chain on PCB. All these demonstrated the assembly is properly done.

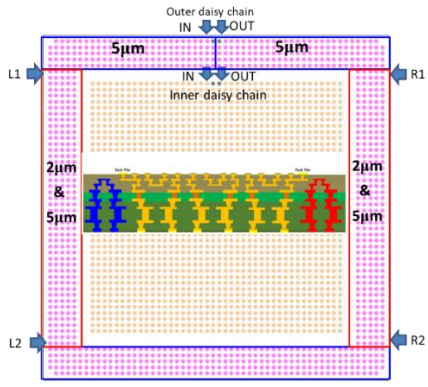


Fig. 15 Schematic nets for continuity measurements.

III(b) Continuity Check

Figure 13 shows the schematic nets for continuity checks. There are 21 hybrid substrates passed all the nets.

III(c) Finite Element Analysis

The structural elements and their dimensions of the hybrid substrate are shown in Figure 16 and their finite element model is shown in Figure 17. Since the conductive paste filled via is the focus point of interest, much finer meshes are used in the paste filled via and around areas. Due to symmetry about the AA'- axes only half of the structure is modelled.

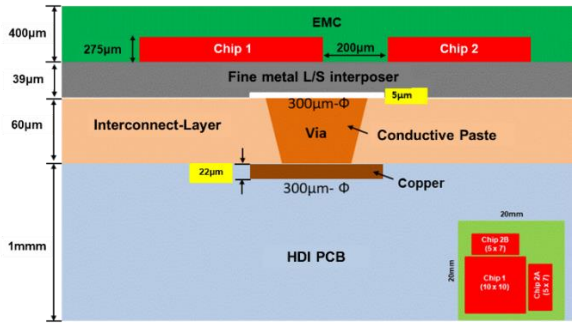


Fig. 16 Structural elements for finite element modelling.

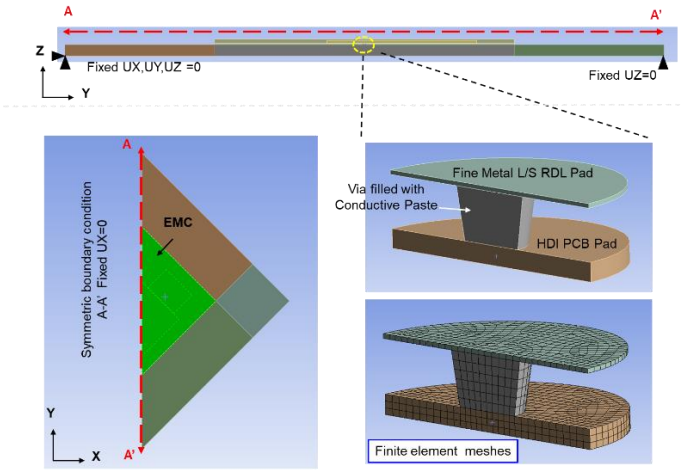


Fig. 17 Finite element modelling.

The material properties of the structural elements are shown in Table 2. The electroplated Cu is assumed as an elastic-plastic (bilinear kinematic hardening) material with the stress-strain relation shown in Figure 18 (first Young's modulus = 121Gpa, second Young's modulus = 1.2Gpa, and yield strength = 173MPa).

The temperature boundary condition is shown in Figure 19. It can be seen that the temperatures are -40°C ⇆ 85°C, and the dwell-time at hot, dwell-time at cold, ramp-up time, and ramp-down time are 15 minutes each. Stress free is at room temperature.

TABLE 2 MATERIAL PROPERTIES

Materials	CTE (10^{-6}/°C)	Young's Modulus (GPa)	Poison's Ratio
Copper	16.3	121	0.34
HDI (PCB)	$\alpha_x = \alpha_y = 18$ $\alpha_z = 70$	$E_x = E_y = 22$ $E_z = 10$	0.28
Silicon(Chip)	2.8	131	0.278
EMC	10 (< 150°C)	19	0.25
RDL package	27.9	47.8	0.3
Conductive Paste	19.01	20.33	0.3
Prepreg	15	26	0.39
Underfill	50	4.5	0.35

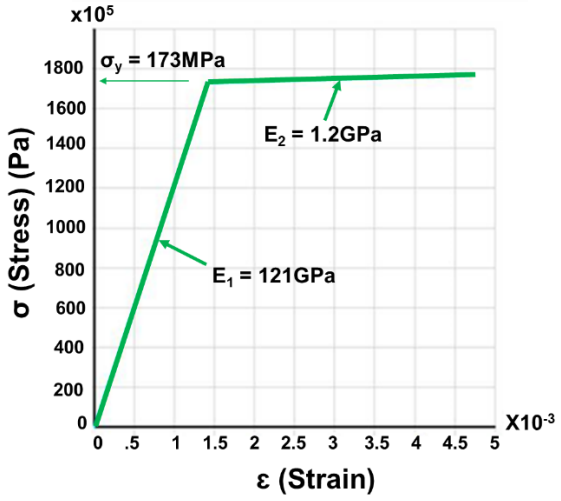


Fig. 18 Stress-strain relation for electroplated Cu.

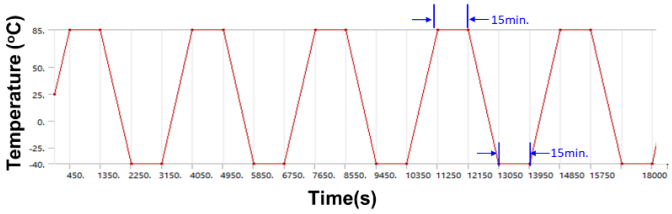


Fig. 19 Temperature boundary condition for simulation.

Figure 20 shows the Mises (equivalent) stress [16] acting at the via filled with conductive paste. Figure 20(a) shows the Mises contours at 85°C (450s), while Figure 20(b) at -40°C (2250s). It can be seen that: (a) for both times (or temperatures) the maximum Mises stress occurs near the interface between the interconnect-layer and the fine metal L/S RDL-interposer (this is due to the expansion mismatch between the RDL-interposer and the interconnect-layer is larger than that between the interconnect-layer and the HDI PCB) and (b) the Mises stress contour at both times is not much different, and (c) the maximum Mises stress (~20MPa) is very small to create reliability issues such as cracking and delamination.

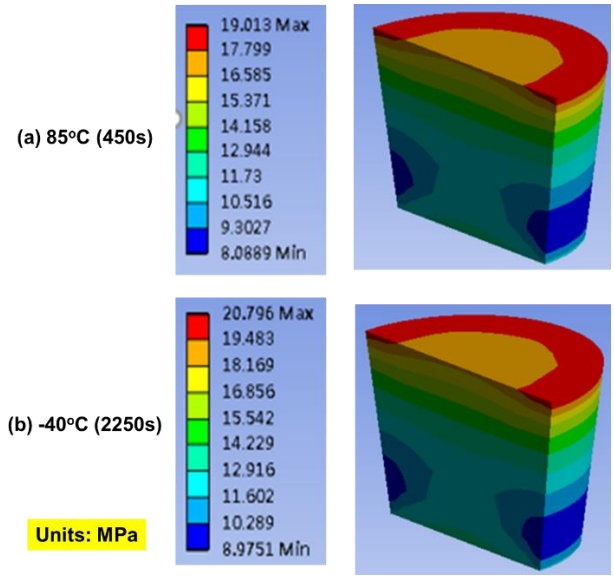


Fig. 20 Equivalent (Mises) stress at the via filled with conductive paste. (a) 85°C (450s). (b) -40°C (2250s).

IV. Summary

Some important results are summarized as follows.

- A high-density organic hybrid substrate for chiplets heterogeneous integration has been developed. This hybrid substrate consists of three major parts, namely the fine metal L/S RDL-interposer, the interconnect-layer, and the HDI PCB.
- The fine metal L/S RDL-interposer with a minimum L/S = 2μm has been fabricated by a fan-out panel-level RDL-first process.
- The interconnect-layer has been fabricated by the PP and vias filled with conductive paste in β-stage.
- The 8-layer HDI PCB has been fabricated by the conventional process.
- The hybrid substrate has been formed by thermocompression and the interconnect-layer become in C-stage.
- Hybrid substrate characterizations such as OM, x-ray, and SEM demonstrated that the interconnect-layer (both conductive paste and prepreg), MLs, pad for chip bonding, daisy-chains on PCB, etc. are properly fabricated. Continuity checks of the hybrid substrate have been passed.
- Nonlinear finite element analysis and result show that the stress state acting at the conductive paste filled via and the surrounding structural elements is very small to create reliability issues such as delamination and cracking.

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