COMPAL CONFIDENTIAL

MODEL NAME : Loki15/17

PCB NO : DA8001BS000

BOM P/N : 431A7Y31L01

KBL-U+MEC1416 board

2017-07-28

REV : 1.0 (A00)

PCB R1

ZZZ

DA8001BS000

PCB@

PCB 21C LA-F115P REV0 M/B 3

PCB R3

ZZZ

DAZ21C00101

PCB_R3@

PCB CAL50 LA-F115P LS-F111P GOLD A31 !

KBL R1

UC1 SA0000AWC0L i7KBLR_1.8G_QS@ S IC A31 FJ8067703281816 QNBF Y0 1.8G

UC1 SA0000A370L i5KBLU_2.5G_R1@ S IC FJ8067702739739 SR2ZU H0 2.5G A31!

UC1 SA0000AWB1L i5KBLR_1.6G_QS@ S IC A31 FJ8067703282221 QNEG Y0 1.6G

UC1 SA0000AQZ0L i7KBLR_1.8G_ES@ S IC A31 FJ8067703281813 QN5C Y0 1.8G

UC1 SA0000A344L i7KBLU_2.7G@ S IC FJ8067702739740 SR2ZV H0 2.7G A31!

UC1 SA0000ACL0L i3SKL_2.0G_SMB0@ S IC FJ8066201931106 SR2UW D1 2G A31!

KBL R3

UC1 SA0000AWC2L i7KBLR_R3@ S IC FJ8067703281816 SR3LC Y0 1.8G A31!

UC1 SA0000AWB3L i5KBLR_R3@ S IC FJ8067703282221 SR3LB Y0 1.6G A31!

UC1 SA0000B2Y1L i3KBLU_R3@ S IC FJ8067702739765 SR3JY H0 2.7G A31!

UC1 SA0000ADV3L KBLU_Pentium_R3@ S IC FJ8067702739932 SR348 H0 2.3G A31!

UC1 SA0000ADL3L KBLU_Celeron_R3@ S IC FJ8067702739933 SR349 H0 1.8G A31!

UC1 SA0000ACL1L i3SKL_SMB0_R3@ S IC FJ8066201931106 SR2UW D1 2G A31!

@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
U22@/U42@ : KBL U/KBL U-R
SKL@/KBL@:SKL/KBL
EC@ : EC
JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
TYPEC@EMI@/TYPEC@ESD@/TYPEC@RF@:EMI, ESD ,RFTYPEC Component
MAD@RF@:RF MAD Component
LOKI@EMI@/LOKI@ESD@:EMI/ESD LOKI Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
TPM@/FTPM@ : HW TPM/SW TPM
MMC@ : eMMC
FFS@ : Free Fall Sensor
TYPEC@/LOKI@TYPEC@ : typeC
DSX@ : Deep sleep
GEN8@/GEN9@:RTC GEN8/9
ODD@:ODD Component
FP@:Finger Printer

M2_50@ : GPU R17M_2_50
2G@/2G_H@/2G_S@/2G_M@ : VRAM type
4G@/4G_H@/4G_S@/4G_M@ : VRAM type

Layout Dell logo

REV: X00
PWB: 9HTP8

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

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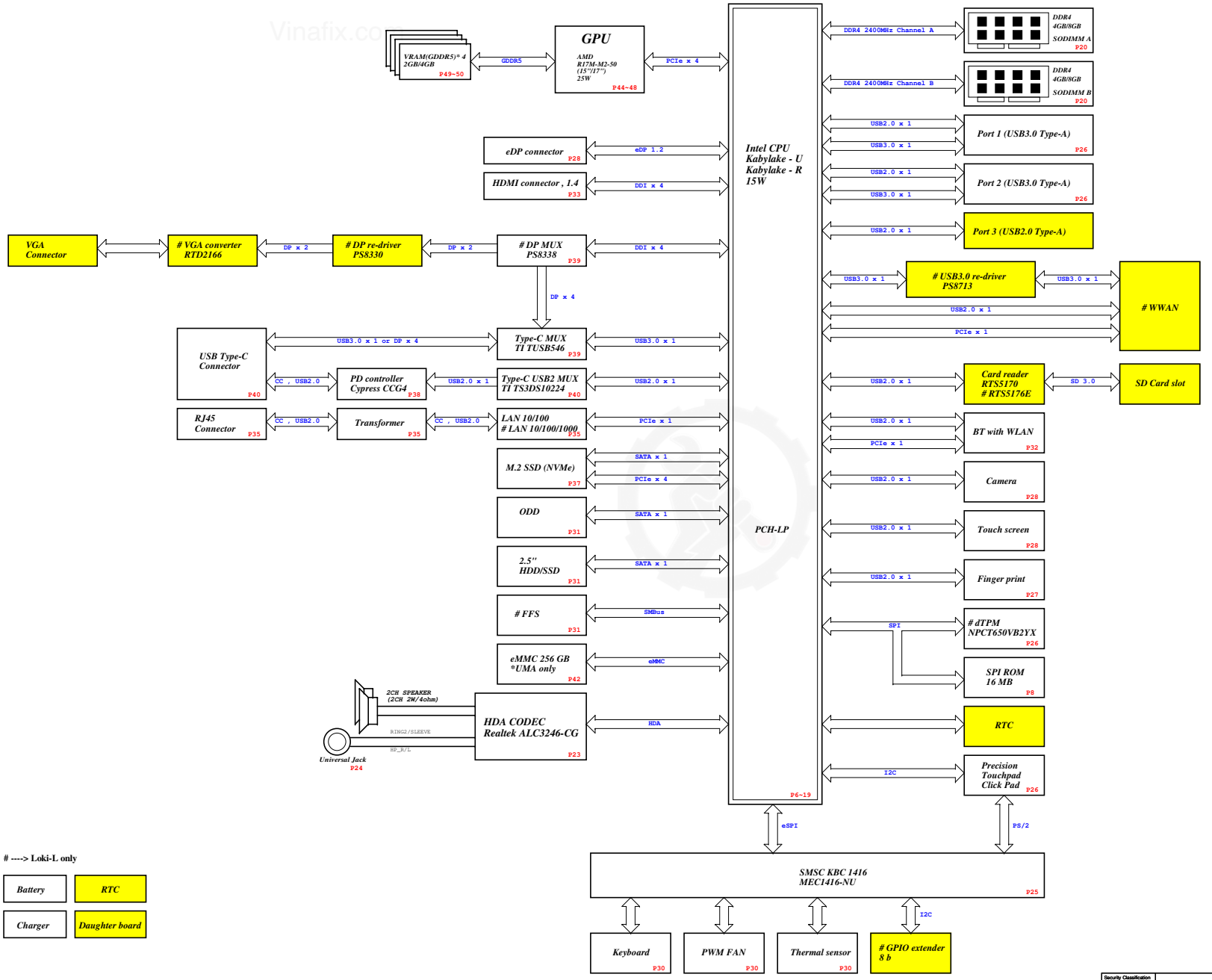
Title: Cover Page

Size | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 1 of 65

Loki/Loki-L Block Diagram



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Issued Date	2016/12/01	Deciphered Date	2017/12/01
Title	Block Diagram		
Size	Document Number		Rev
	LA-F115P		0.1
Date: Friday, July 06, 2017	Sheet 3 of 65		

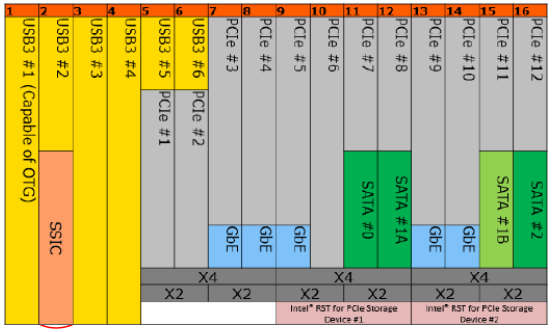
POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	LOW	HIGH	HIGH	ON	ON	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	DS3	S4/S5	M3
+SDC_IN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+1.0V_PRIM	System +1.0V power rail	ON	ON	OFF	ON*	ON
+1.0VS_VCCIO	+1.0VS IO power rail	ON	OFF	OFF	OFF	OFF
+1.0V_MPHYPLL	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	OFF	ON/OFF	ON
+0.95VSDGPU	+0.9VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.35V_MEM_GFX	+1.35VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.2V_DDR	DDR4/L-RS +1.2V power rail	ON	ON	ON	OFF	ON
+2.5V_MEM	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	OFF	ON*	ON
+1.8VS	System +1.8VS power rail	ON	OFF	OFF	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3.3V_ALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	OFF	ON*	ON
+3VS	System +3VS power rail	ON	OFF	OFF	OFF	ON
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	OFF	OFF	OFF	ON
+RTC_CELL	RTC power	ON	ON	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.						

High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

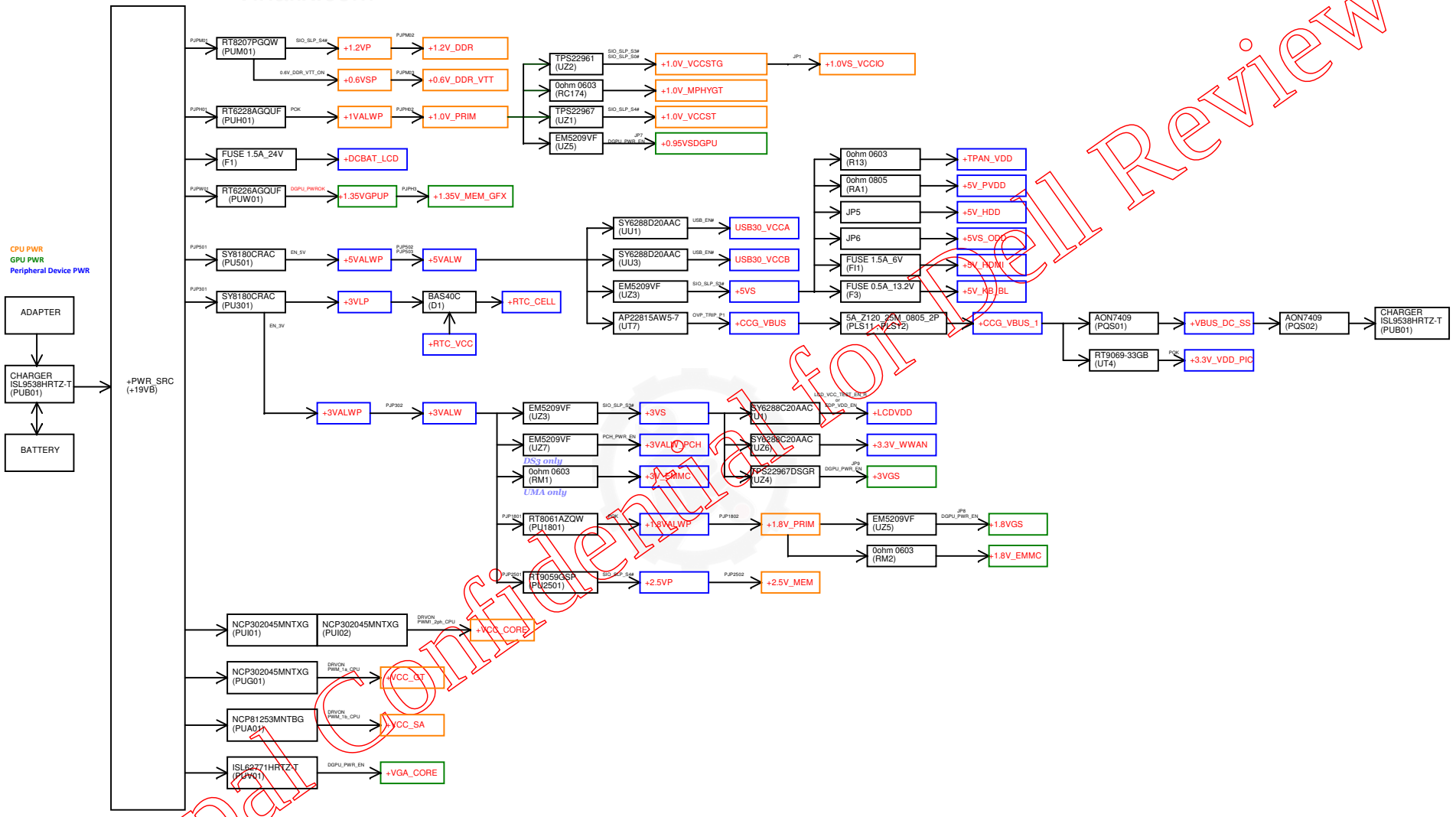


USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 port3 , IO/B
3	USB2.0 Port2
4	TypeC
5	Camera
6	Card reader , IO/B
7	BT
8	Touch screen
9	Finger printer
10	WWAN , IO/B

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1			USB3.0 port1
USB3.0-2			WWAN , IO/B
USB3.0-3			USB3.0 port2
USB3.0-4			TypeC
USB3.0-5	PCIE-1		GPU
USB3.0-6	PCIE-2		GPU
	PCIE-3		GPU
	PCIE-4		GPU
	PCIE-5		10/100 LAN
	PCIE-6		WLAN
	PCIE-7	SATA-0	SATA HDD
	PCIE-8	SATA-1	SATA ODD
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-1*	NVME SSD
	PCIE-12	SATA-2	NVME SSD

Board ID & Model ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT
2	100	13.7	2.902	
3	100	17.8	2.801	DVT1
4	100	22.1	2.703	
5	100	27.0	2.598	DVT2
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	Pilot
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	
15	100	120.0	1.500	
16	100	137.0	1.392	
17	100	154.0	1.299	
18	100	200.0	1.100	
19	100	232.0	0.994	



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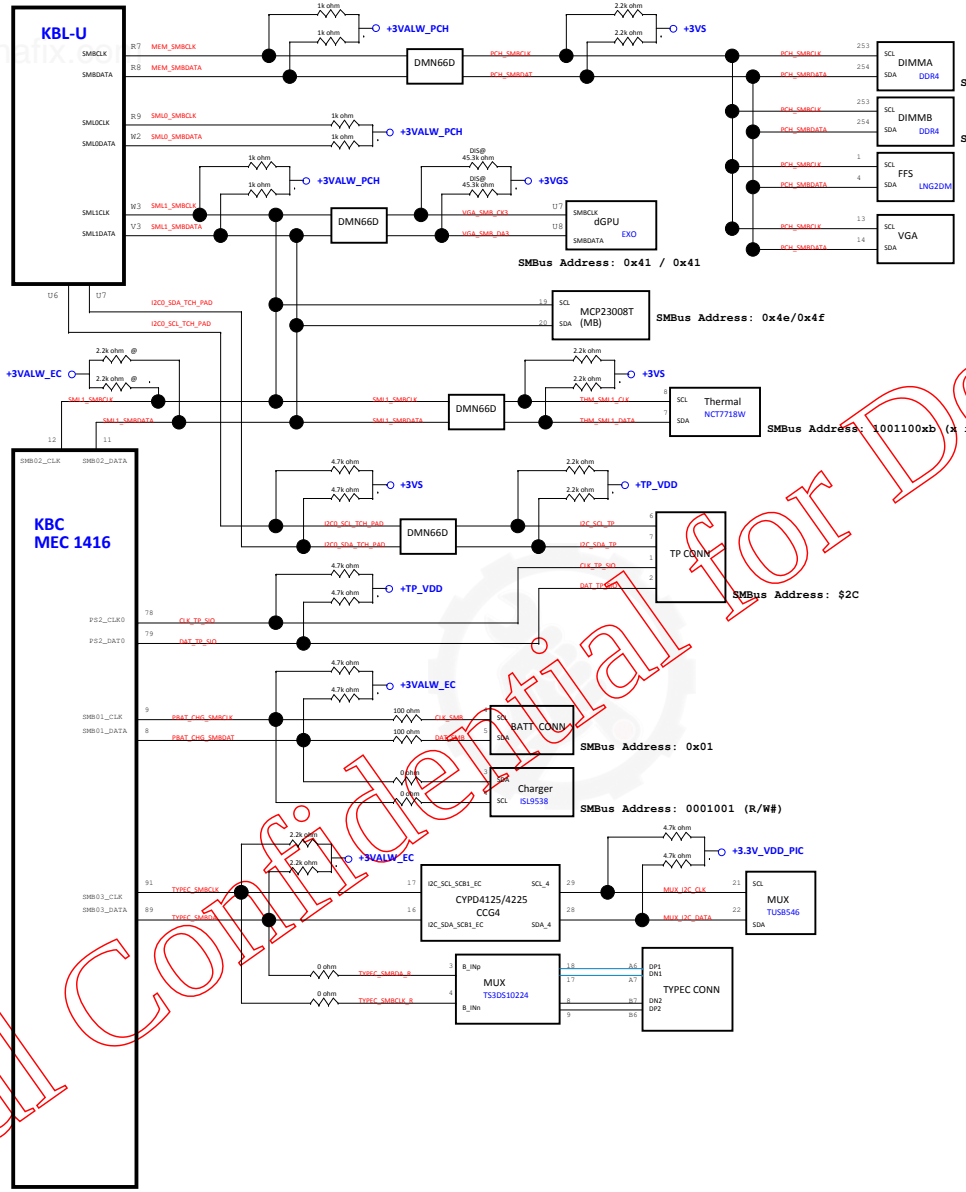
			Size: Document Number: LA-F115P Rev: 0.1
			Date: Friday, July 28, 2017 Sheet 4 of 65



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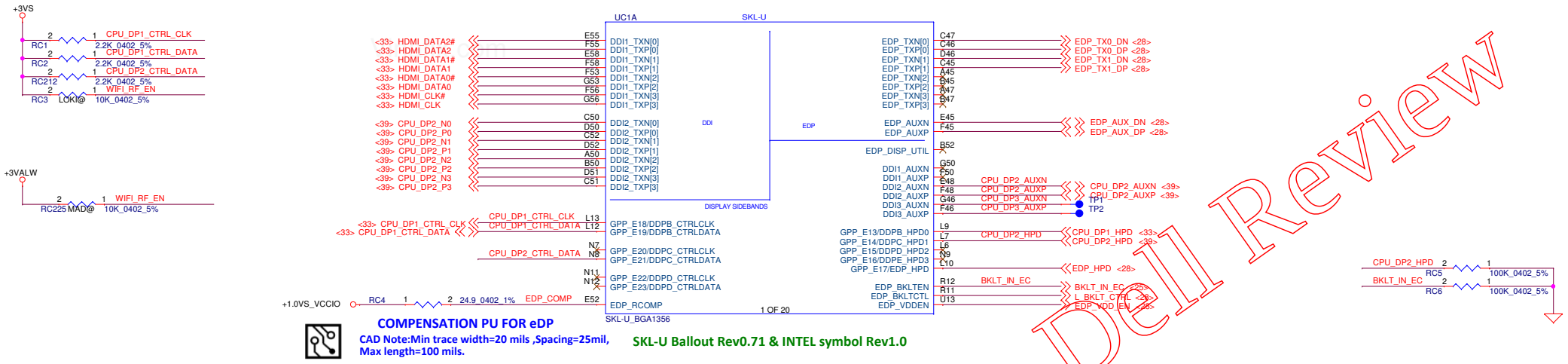
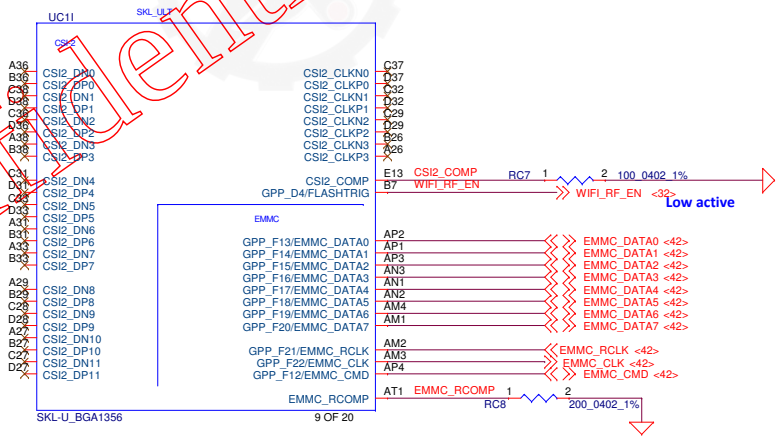
Issued Date	2016/12/01	Deciphered Date	2017/12/01
Title	SMbus Block Diagram		
Size	Document Number		Rev
	LA-F115P		0.1
Date: Friday, July 28, 2017	Sheet 5 of 65		

Main Func = CPU





Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	MCP(1/14)DDI,EDP,CSI2,EMMC		
Size	Document Number LA-F115P		Rev 0.1
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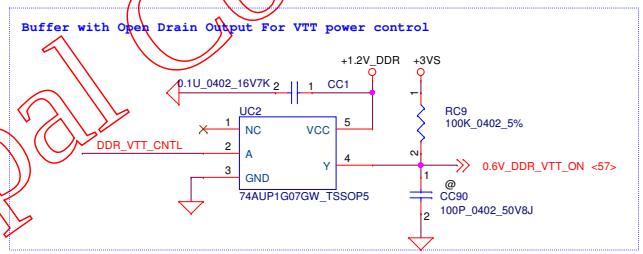
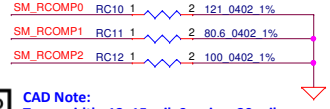
Main Func = CPU

DDR4 Interleaved Memory



DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: MCP(2/14)DDR4			
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017	Sheet 7 of 65		

Main Func = CPU

SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

UC1E — SKL-U — SPI - FLASH / SPI - TOUCH / C LINK / SMBUS, SMLINK / LPC

SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2, SPI0_IO3, SPI0_CS0#, SPI0_CS1#, SPI0_CS2#

GPP_D1/SPI1_CLK, GPP_D2/SPI1_MISO, GPP_D3/SPI1_MOSI, GPP_D21/SPI1_IO2, GPP_D22/SPI1_IO3, GPP_D0/SPI1_CS#

CL_CLK, CL_DATA, CL_RST#

GPP_A0/RCIN#, GPP_A6/SERIRQ

GPP_C0/SMBCLK, GPP_C1/SMBDATA, GPP_C2/SMBALERT#, GPP_C3/SML0CLK, GPP_C4/SML0DATA, GPP_C5/SML0ALERT#, GPP_C6/SML1CLK, GPP_C7/SML1DATA, GPP_B23/SML1ALERT#/PCHHOT#

GPP_A1/LAD0/ESPI_IO0, GPP_A2/LAD1/ESPI_IO1, GPP_A3/LAD2/ESPI_IO2, GPP_A4/LAD3/ESPI_IO3, GPP_A5/LFRAME#/ESPI_CS#, GPP_A14/SUS_STAT#/ESPI_RESET#

GPP_A9/CLKOUT_LPC0/ESPI_CLK, GPP_A10/CLKOUT_LPC1, GPP_A8/CLKRUN#

SKL-U_BGA1356 — 5 OF 20

SML1_SMBCLK <25,30,34,45> / SML1_SMBDATA <25,30,34,45> — SML1 -> EC, DGPU, THM

QC1A DMN66D0LDW-7_SOT363-6 / QC1B DMN66D0LDW-7_SOT363-6 — MEM_SMBCLK, MEM_SMBDATA — PCH_SMBCLK <20,21,31,34>, PCH_SMBDATA <20,21,31,34> — SMB -> DDR4, FFS

RPC2 15_0804_8P4R_5%

CLOSE TO UC1

TLS CONFIDENTIALITY

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

Modify Value to 150k for WW52 MOW 2015/03/03 Jason

EXI BOOT STALL BYPASS

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

RC40/41 place to within 1100 mil of SPI0_MOSI/SPI0_IO2 pin for XDP

MOW 2015WW06

UC3 W25Q128FVSIQ_SO8 — 128Mb Flash ROM

RC178,RC179,RC180 place colse to UC1

UC3 place colse to UX1

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

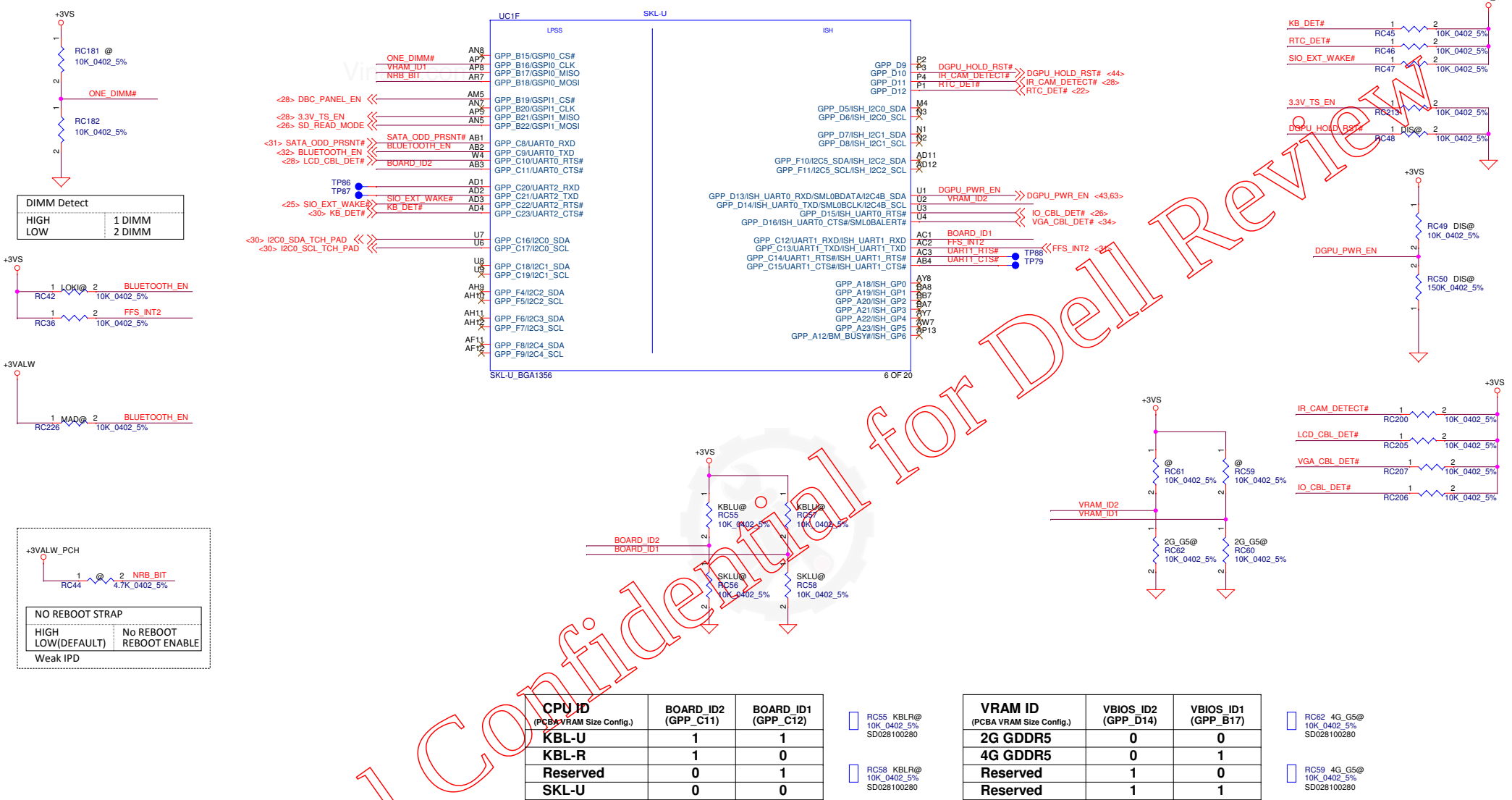
Compal Electronics, Inc.

Title: MCP(3/14)SPI,SMB,LPC

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 8 of 65

Main Func = CPU



CPU ID (PCBA VRAM Size Config.)	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
KBL-U	1	1
KBL-R	1	0
Reserved	0	1
SKL-U	0	0

RC55 KBLR@ 10K_0402_5% SD028100280

RC58 KBLR@ 10K_0402_5% SD028100280

VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_D14)	VBIOS_ID1 (GPP_B17)
2G GDDR5	0	0
4G GDDR5	0	1
Reserved	1	0
Reserved	1	1

RC62 4G_G5@ 10K_0402_5% SD028100280

RC59 4G_G5@ 10K_0402_5% SD028100280

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

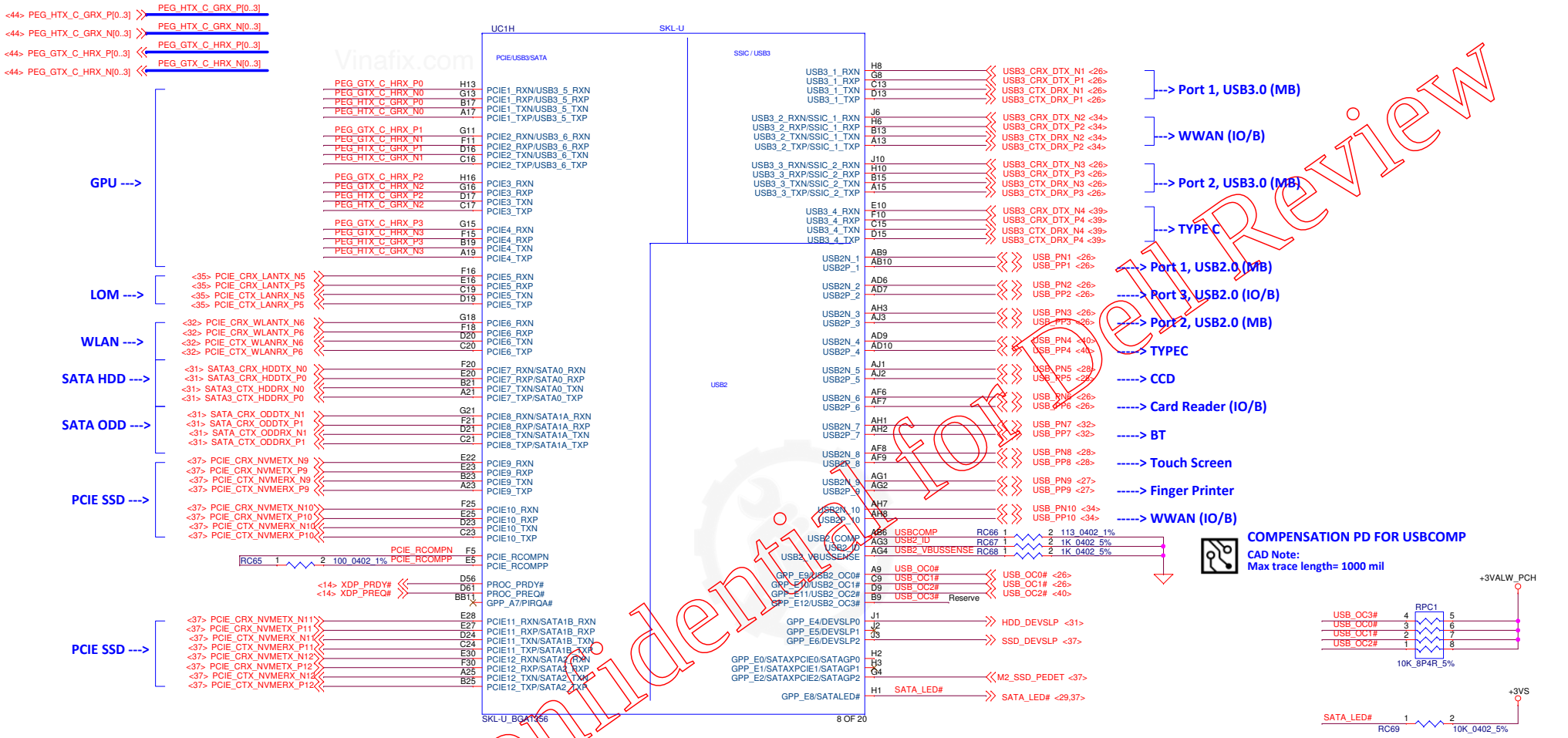
Compal Electronics, Inc.

Title: MCP(4/14)GSPI,I2C,UART,ISH

Size: C | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 9 of 65

Main Func = CPU

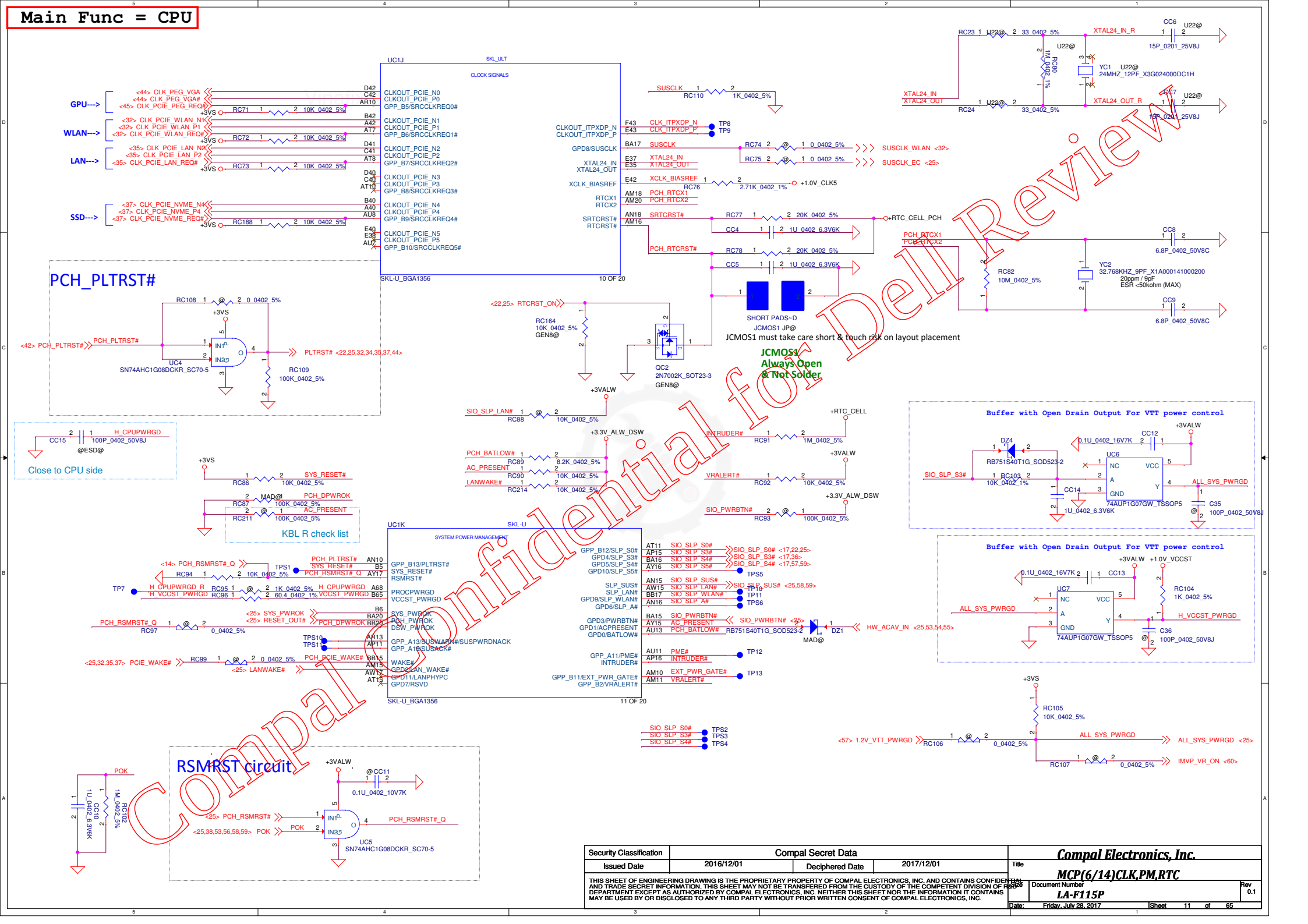


GPIO	Device Control
USB_OC0#	USB Port 1
USB_OC1#	WWAN
USB_OC2#	USB Port 4 (Type-C)
USB_OC3#	NA

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: MCP(5/14)PCIE,USB,SATA			
Size:	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017	Sheet 10 of 65		

Main Func = CPU



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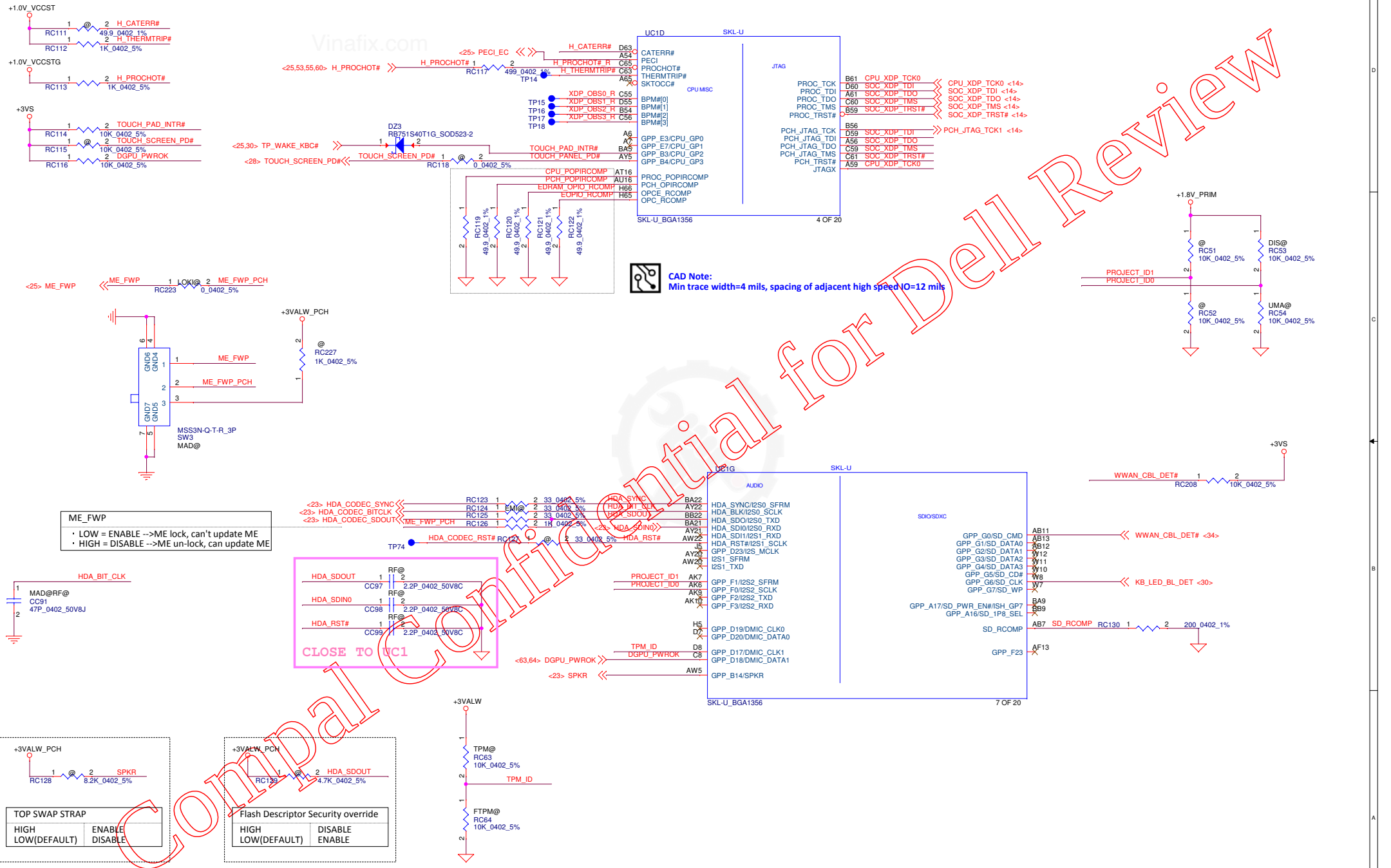
Compal Electronics, Inc.			
Title: MCP(6/14)CLK,PM,RTC			
Size: C	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017		Sheet 11 of 65	

Main Func = CPU



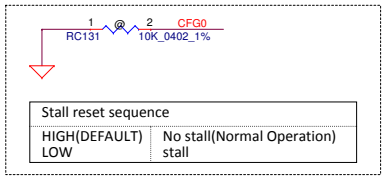
ME_FWP

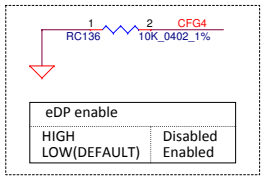
- LOW = ENABLE -->ME lock, can't update ME
- HIGH = DISABLE -->ME un-lock, can update ME

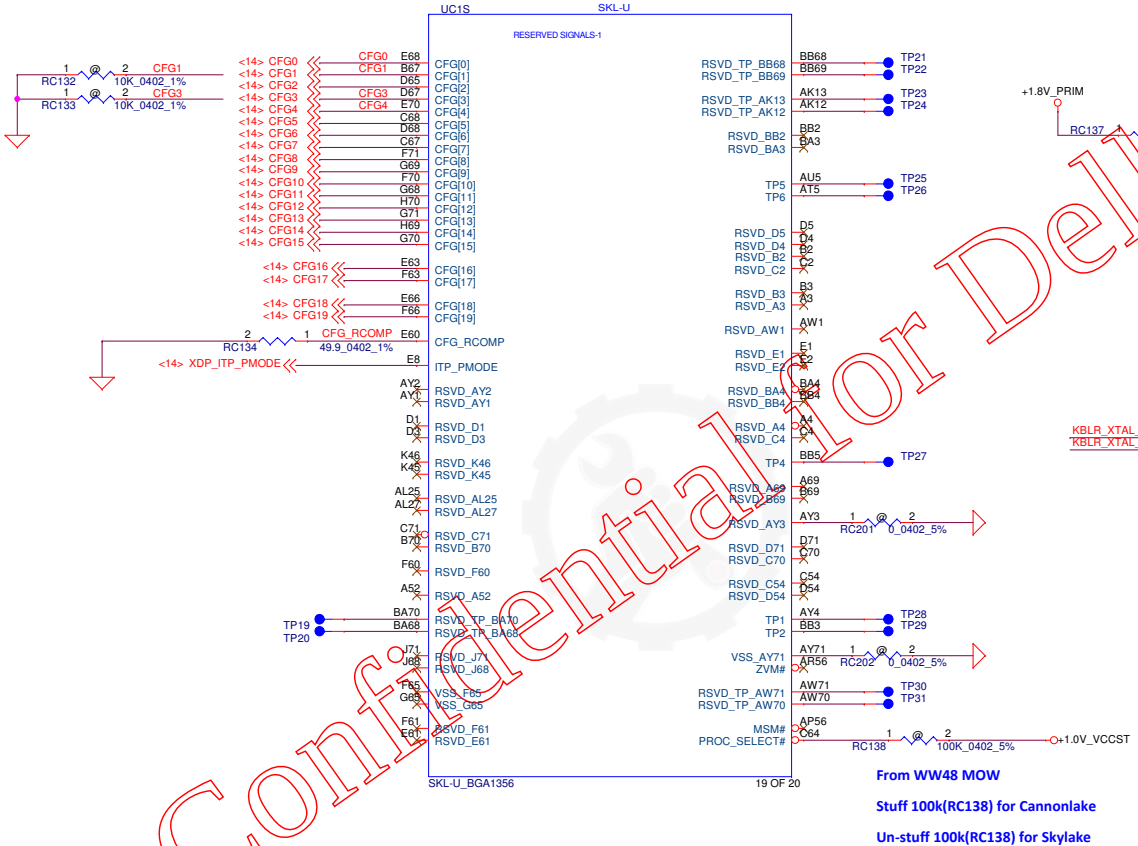
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

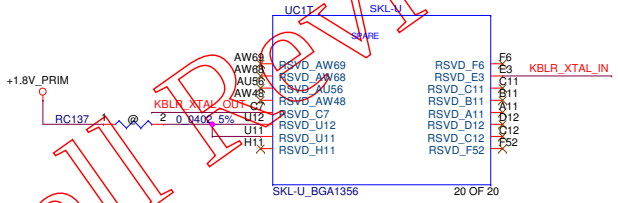
Compal Electronics, Inc.			
Title	MCP(7/14)MISC,JTAG,HDA,SDIO		
Size	Document Number		Rev
	LA-F115P		0.1
Date: Friday, July 28, 2017		Sheet 12 of 65	

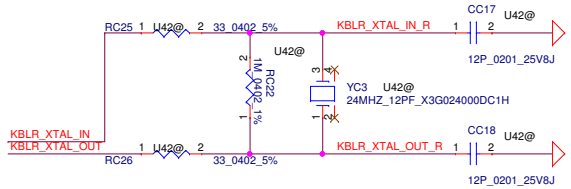
Main Func = CPU











Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	MCP(8/14)CFG,RSVD		
Size	Document Number		Rev
	LA-F115P		0.1
Date: Friday, July 28, 2017	Sheet 13 of 65		

Main Func = CPU

Connector Less Routing Topology

DCI Link
RC142 need POP
RC146 need POP

+3.3V_SPI
RC139 1 CMC@ 2 1K_0402_5% XDP_SPI_SI

Place to CPU side

+1.0V_VCCSTG
RC140 2 CMC@ 1 51_0402_5% SOC_XDP_TMS
RC141 2 CMC@ 1 51_0402_5% SOC_XDP_TDI
RC142 2 CMC@ 1 51_0402_5% SOC_XDP_TDO

+1.0V_XDP
RC143 1 CMC@ 2 1K_0402_5% XDP_ITP_PMODE
RC144 2 @ 1 0_0402_5% XDP_PRSENT_CPU
RC145 2 @ 1 0_0402_5% XDP_SPI_IO2

Place to CPU side

RC146 2 CMC@ 1 51_0402_1% CPU_XDP_TCK0
RC147 2 @ 1 51_0402_5% PCH_JTAG_TCK1

<12> SOC_XDP_TDO → TPC1
<12> CPU_XDP_TCK0 → TPC2
<12> PCH_JTAG_TCK1 → TPC3
<12> SOC_XDP_TMS → TPC4

<12> SOC_XDP_TDI → TPC5
<12> SOC_XDP_TRST# → TPC6
<13> XDP_ITP_PMODE → TPC7

<8> XDP_SPI_SI → TPC8
<8> XDP_SPI_IO2 → TPC9

CFG3 — RC175 1 CMC@ 2 0_0402_5% — XDP_PRSENT_CPU

<11> PCH_RSMRST#_O — RC148 1 CMC@ 2 1K_0402_5% — XDP_HOOK0

<13> CFG0 → TPC10
<13> CFG1 → TPC11
<13> CFG2 → TPC12
<13> CFG3 → TPC13
<13> CFG4 → TPC14
<13> CFG5 → TPC15
<13> CFG6 → TPC16
<13> CFG7 → TPC17

<13> CFG17 → TPC18
<13> CFG16 → TPC19

<13> CFG8 → TPC20
<13> CFG9 → TPC21
<13> CFG10 → TPC22
<13> CFG11 → TPC23
<13> CFG12 → TPC24
<13> CFG13 → TPC25
<13> CFG14 → TPC26
<13> CFG15 → TPC27

<13> CFG19 → TPC28
<13> CFG18 → TPC29

PRIMARY CMC CONN

+1.0V_PRIM — RC149 1 CMC@ 2 0_0603_5% — +1.0V_XDP

TPC30 → XDP_PREQ# <10>
TPC31 → XDP_PRDY# <10>
TPC32 → XDP_HOOK0
TPC33 → XDP_PRSENT_CPU

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: MCP(9/14)XDP			
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017		Sheet 14 of 65	

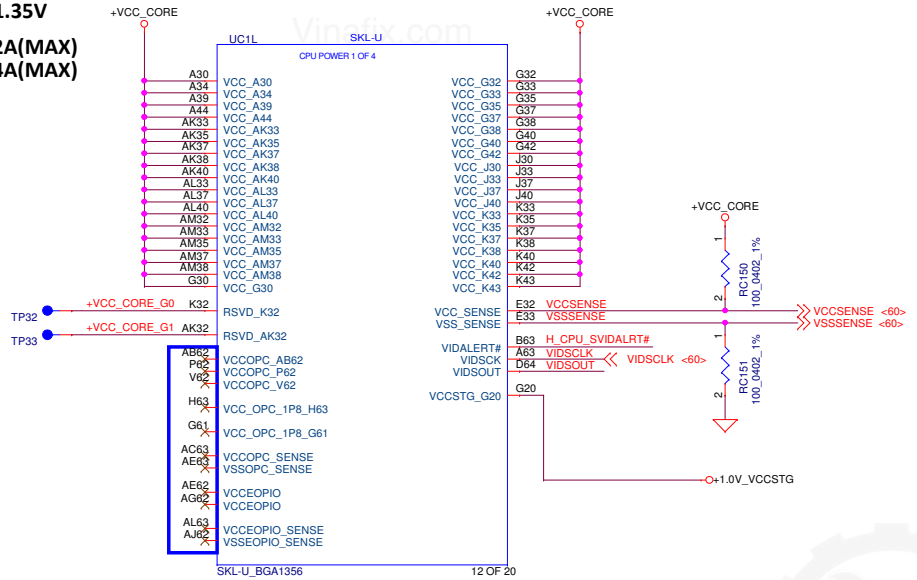
Main Func = CPU

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

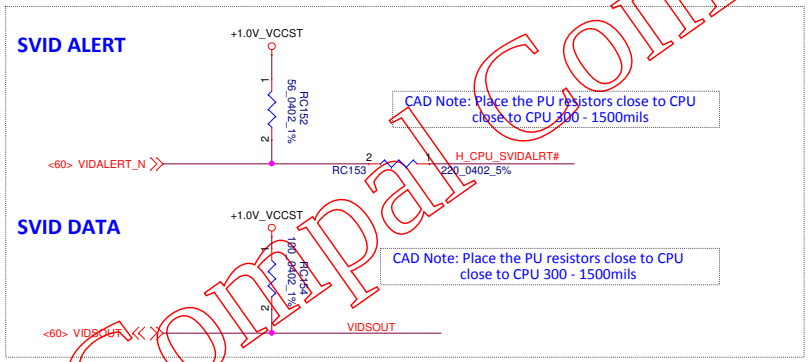
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

+VCC_CORE: 0.3~1.35V

+VCC_CORE(U22): 32A(MAX)
+VCC_CORE(U42): 64A(MAX)



VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



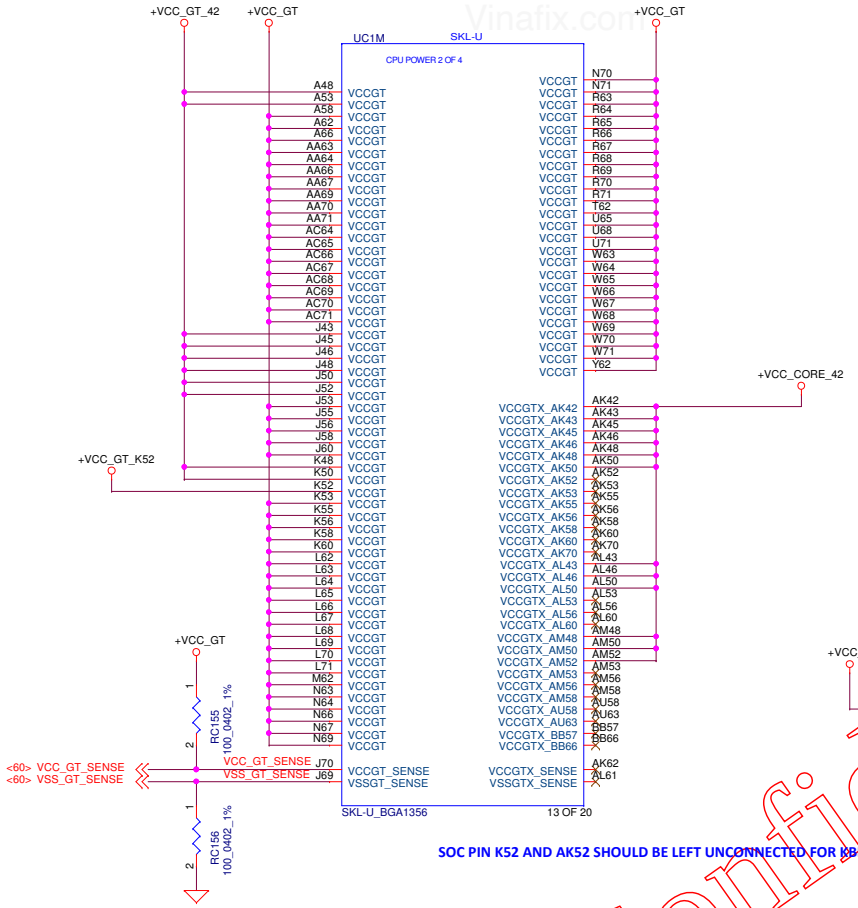
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

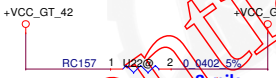
Compal Electronics, Inc.			
Title	MCP(10/14)PWR-VCC CORE		
Size	Document Number		Rev
	LA-F115P		0.1
Date:	Friday, July 28, 2017	Sheet 15 of 65	

Main Func = CPU

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

+VCC_GT(U22): 31A(MAX)
+VCC_GT(U42): 28A(MAX)





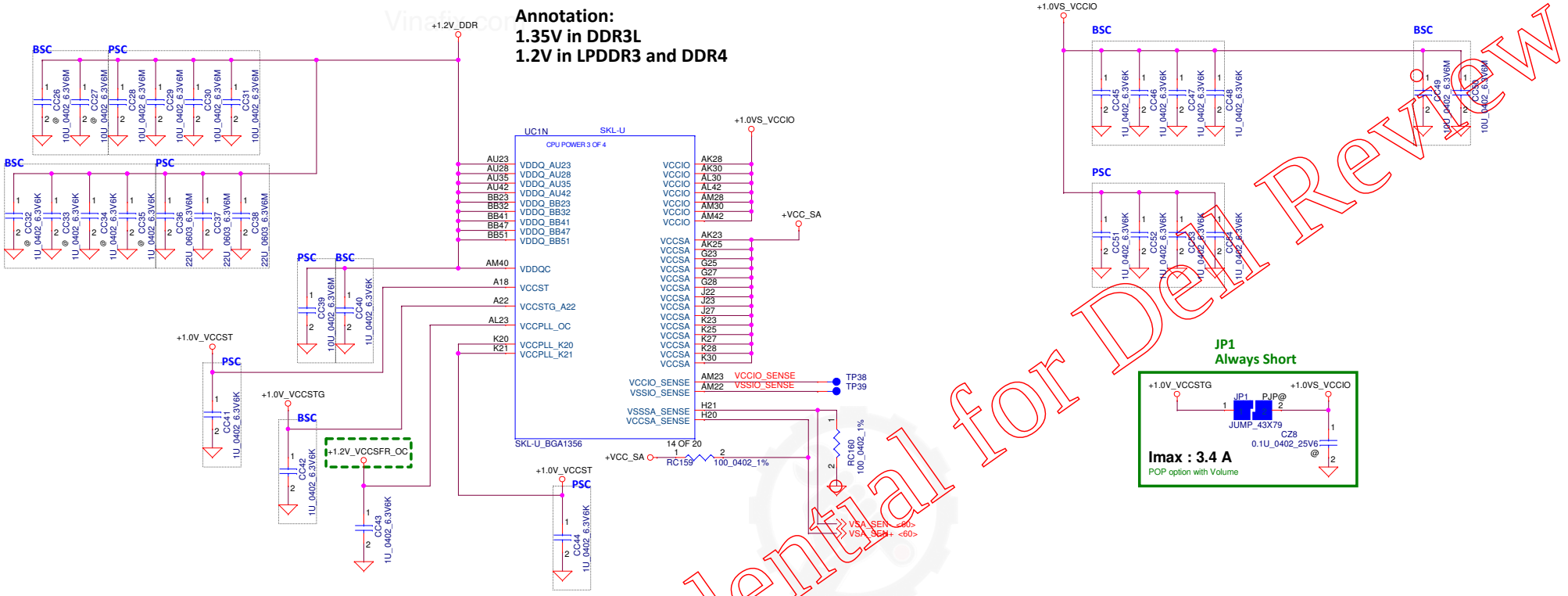
SOC PIN K52 AND AK52 SHOULD BE LEFT UNCONNECTED FOR KBL R U42 DESIGNS

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.		
Title: MCP(11/14)PWR-VCCGT		
Size	Document Number: LA-F115P	Rev: 0.1
Date: Friday, July 28, 2017	Sheet 16 of 65	

Main Func = CPU

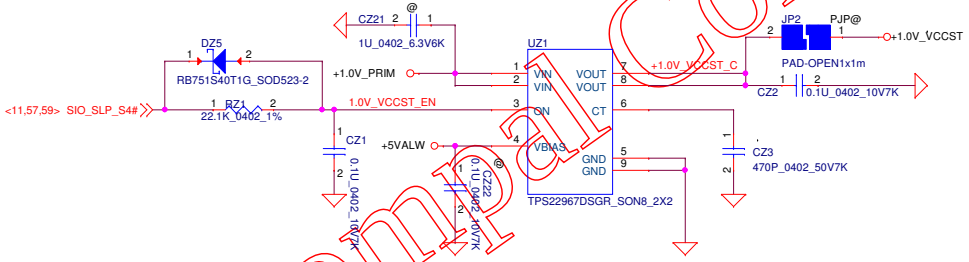
Annotation:
1.35V in DDR3L
1.2V in LPDDR3 and DDR4



+1.0V_VCCST source

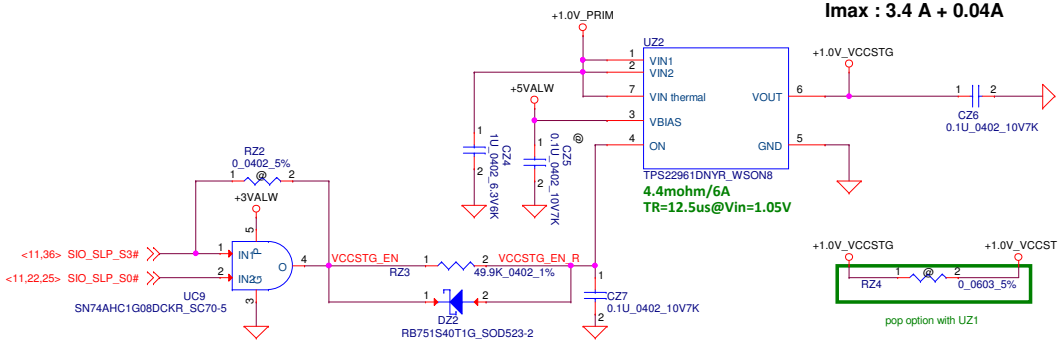
Imax : 0.24 A

JP2
Always Short



+1.0V_VCCSTG source

Imax : 3.4 A + 0.04A



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	MCP(12/14)PWR-VCCIO,MEM		
Size	Document Number	LA-F115P	Rev 0.1
Date: Friday, July 28, 2017	Sheet 17 of 65		

Main Func = CPU

+1.0V_MPHYGT source

+1.0V_PRIM — RC174 1 @ 2 0_0603_5% — +1.0V_MPHYGT

Imax : 2.8 A

PCH PWR

UC1O — SKL-U — CPU POWER 4 OF 4

AB19	VCCPRIM_1P0	close UC1.AL1 and <120mil
AB20	VCCPRIM_1P0	
P18	VCCPRIM_1P0	
AF18	VCCPRIM_CORE	close UC1.AF18 and <400mil
AF19	VCCPRIM_CORE	
V20	VCCPRIM_CORE	
V21	VCCPRIM_CORE	
AL1	DCPDSW_1P0	
K17	VCCMPHYAON_1P0	close UC1.K17 and <120mil
L1	VCCMPHYAON_1P0	
N15	VCCMPHYGT_1P0_N15	
N16	VCCMPHYGT_1P0_N16	
N17	VCCMPHYGT_1P0_N17	
P15	VCCMPHYGT_1P0_P15	
P16	VCCMPHYGT_1P0_P16	
K15	VCCAMPHYPLL_1P0	+1.0V_AMPHYPLL
L15	VCCAMPHYPLL_1P0	
V15	VCCAPLL_1P0	+1.0V_APLL
AB17	VCCPRIM_1P0_AB17	+1.0V_PRIM
Y18	VCCPRIM_1P0_Y18	
AD17	VCCDSW_3P3_AD17	+3.3V_ALW_DSW
AD18	VCCDSW_3P3_AD18	
AJ17	VCCDSW_3P3_AJ17	
AJ19	VCCHDA	+3.3V_HDA
AJ16	VCCSPI	+3.3V_SPI
AF20	VCCSRAM_1P0	close UC1.AF20 and <400mil
AF21	VCCSRAM_1P0	
T19	VCCSRAM_1P0	
T20	VCCSRAM_1P0	
AJ21	VCCPRIM_3P3_AJ21	+3VALW_PCH
AK20	VCCPRIM_1P0_AK20	+1.0V_PRIM
N18	VCCAPLLEBB	+1.0V_APLLEBB, close UC1.N18 and <120mil

AK15	VCCPGPPA	+1.8V_PRIM
AG15	VCCPGPPB	close UC1.AG15 and <120mil
Y16	VCCPGPPC	close UC1.Y16 and <400mil
Y15	VCCPGPPD	+3VALW_PCH
T16	VCCPGPPE	close UC1.T16 and <400mil
AF16	VCCPGPPF	+1.8V_PRIM
AD15	VCCPGPPG	+3VALW_PCH
V19	VCCPRIM_3P3_V19	+3VALW_PCH, close UC1.V19 and <120mil
T1	VCCPRIM_1P0_T1	+1.0V_PRIM
AA1	VCCATS_1P8	close UC1.AA1 and <400mil
AK17	VCCRTCPRIM_3P3	+3VALW_PCH
AK19	VCCRTC_AK19	close UC1.AK19 and <120mil
BB14	VCCRTC_BB14	
BB10	DCPRTC	close UC1.BB10 and <120mil
A14	VCCCLK1	+1.0V_PRIM
K19	VCCCLK2	+1.0V_CLK2
L21	VCCCLK3	
N20	VCCCLK4	+1.0V_CLK4
L19	VCCCLK5	+1.0V_CLK5
A10	VCCCLK6	+1.0V_PRIM, close UC1.A10 and <120mil
AN11	GPP_B0/CORE_VID0	TP76
AN13	GPP_B1/CORE_VID1	TP77

SKL-U_BGA1356 — 15 OF 20

+1.0V_PRIM — RC161 1 2 0_0603_5% — +1.0V_SRAM

+1.0V_PRIM — RC162 1 2 0_0603_5% — +1.0V_APLLEBB

+3VALW_PCH — RC199 1 GEN8@ 2 0_0402_5% — +RTC_CELL_PCH — +RTC_CELL

+3VALW_PCH — close UC1.AJ19 and <100mil — L2 BLM15BD601SN1D_2P — CC100 0.5P_0402_50V8 RF@ — CC61 0.5P_0402_50V8 @RF@ — +3.3V_HDA

+1.0V_MPHYGT — close UC1.K15, UC1.L15 and <100mil — RC169 1 @ 2 0_0603_5% — close UC1.K15 and <120mil — +1.0V_AMPHYPLL

+1.0V_PRIM — RC170 1 @ 2 0_0603_5% — close UC1.K19 and <100mil — +1.0V_CLK2

+1.0V_PRIM — RC171 1 @ 2 0_0603_5% — close UC1.L19 and <100mil — +1.0V_CLK5

+3VALW_PCH — close UC1.AK17 and <120mil

+3VALW — RC163 1 GEN8@ 2 0_0402_5% — +3.3V_ALW_DSW

+1.0V_PRIM — close UC1.V15 and <100mil — L1 BLM15BD601SN1D_2P — CC83 0.5P_0402_50V8 RF@ — CC82 0.5P_0402_50V8 @RF@ — +1.0V_APLL

+1.0V_PRIM — RC173 1 @ 2 0_0603_5% — close UC1.N20 and <100mil — +1.0V_CLK4

+3VALW — +1.8V_PRIM — +1.0V_PRIM

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

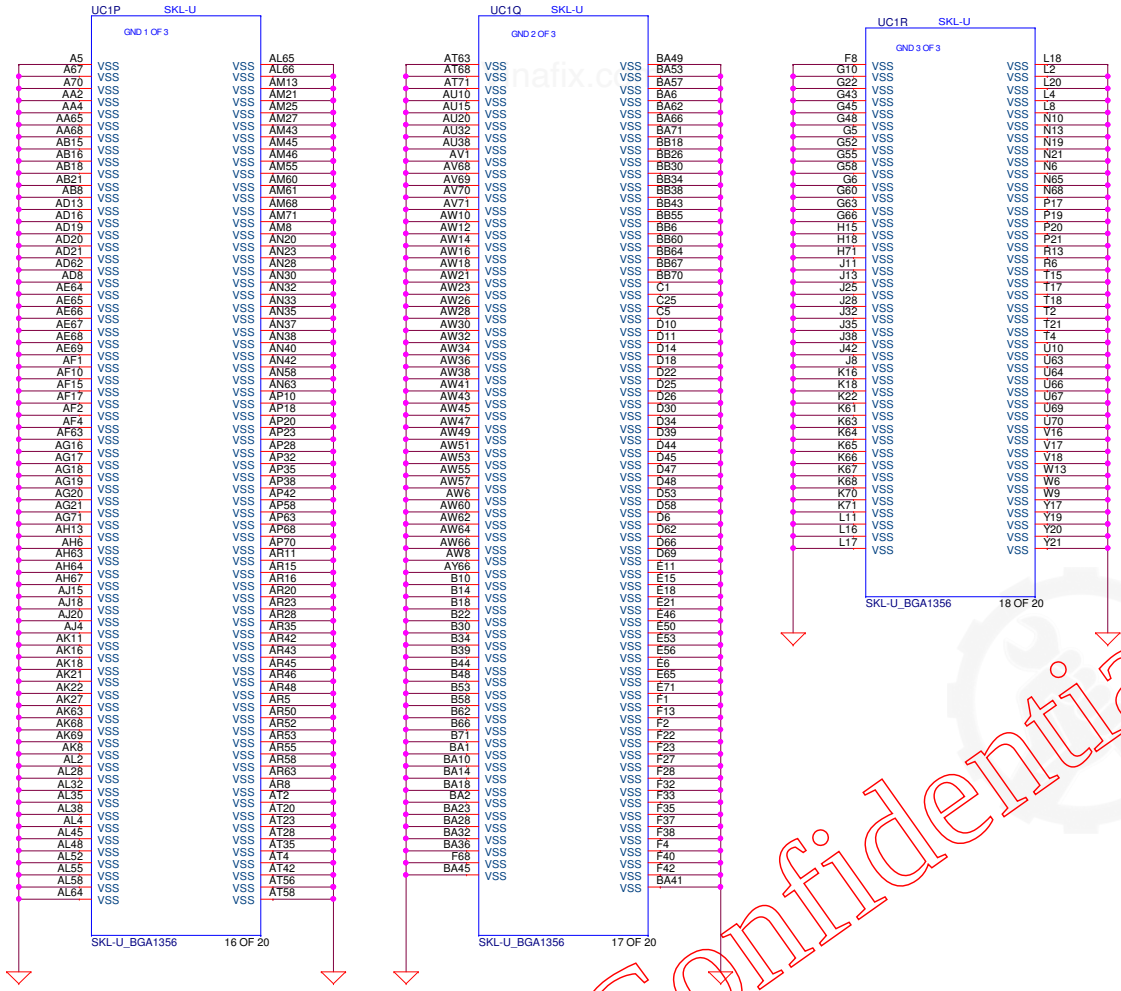
Compal Electronics, Inc.

Title: MCP(13/14)PCH PWR

Size | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 18 of 65

Main Func = CPU



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MCP(14/14)VSS

Size: C | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 19 of 65

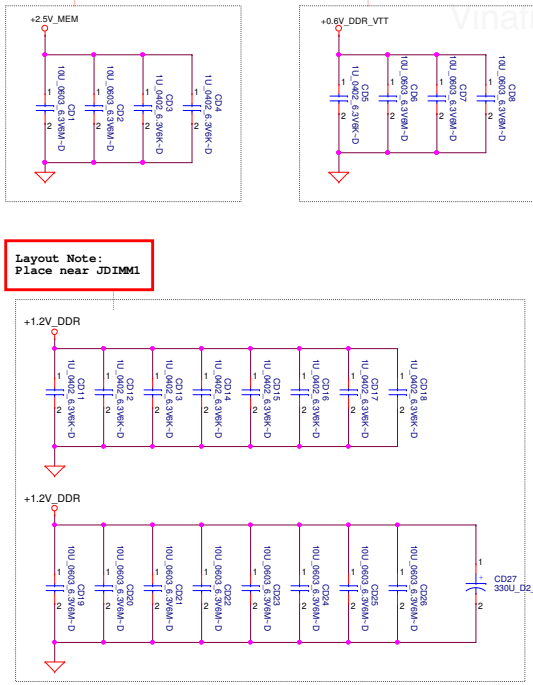
Main Func = DDR

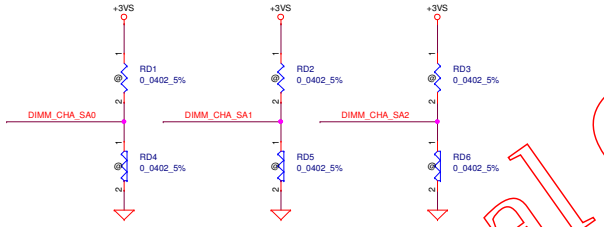
Layout Note:
Place near JDIMM1.257,259

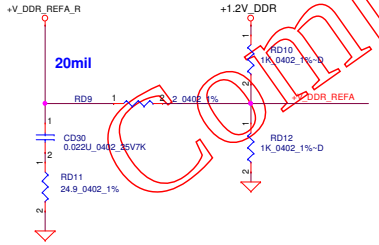
Layout Note:
Place near JDIMM1.258

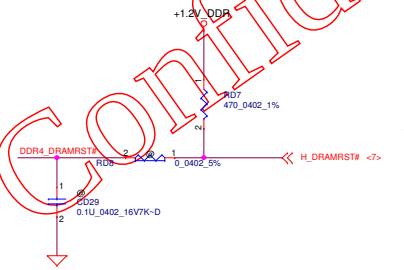
Layout Note:
Place near JDIMM1.255

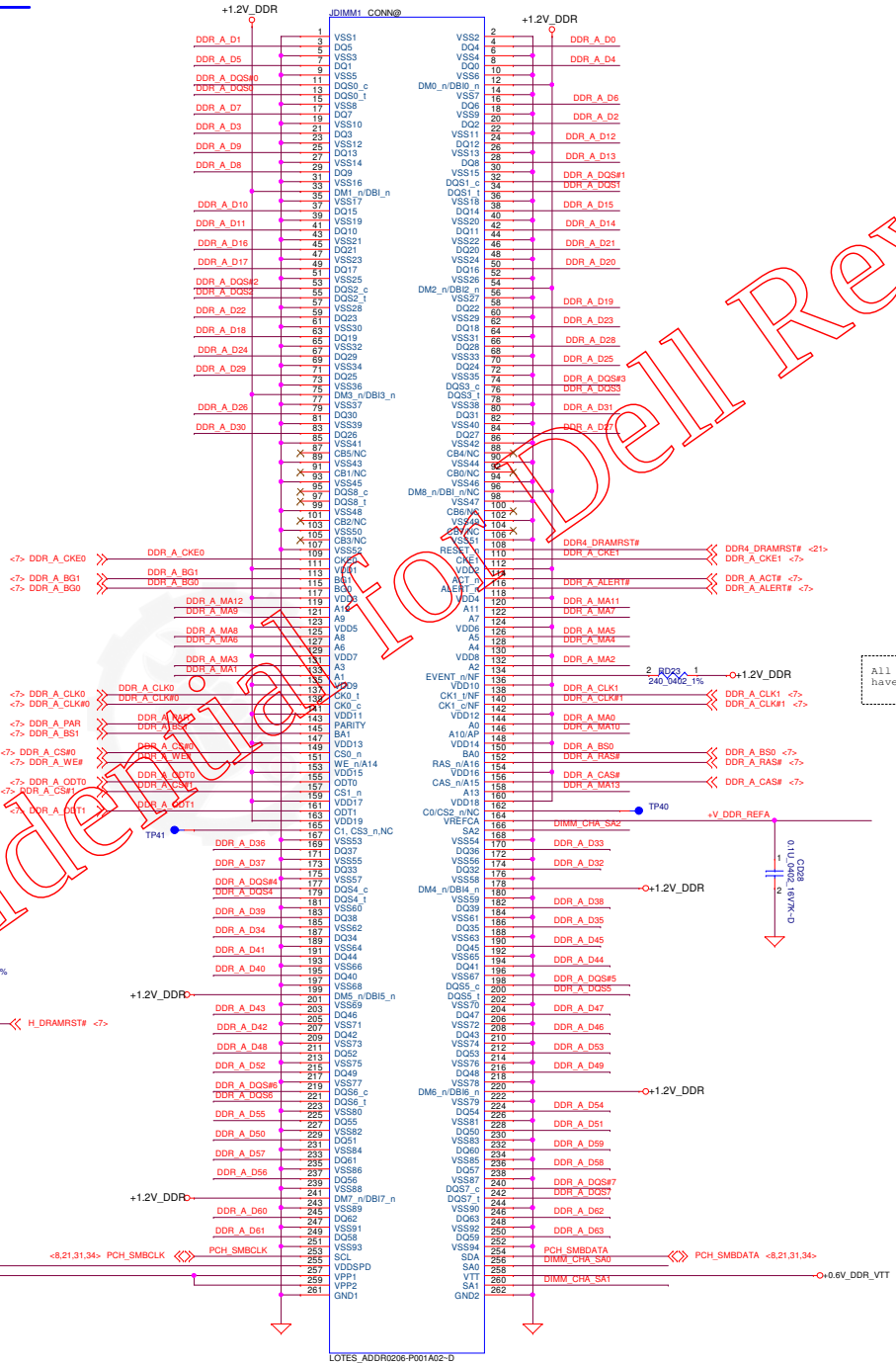
Layout Note:
Place near JDIMM1











All VREF traces should have 10 mil trace width

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: DDR4 DIMMA_RVS			
Size	Document Number: LA-F111P		Rev: 0.1
Date: Friday, July 28, 2017	Sheet 20 of 65		

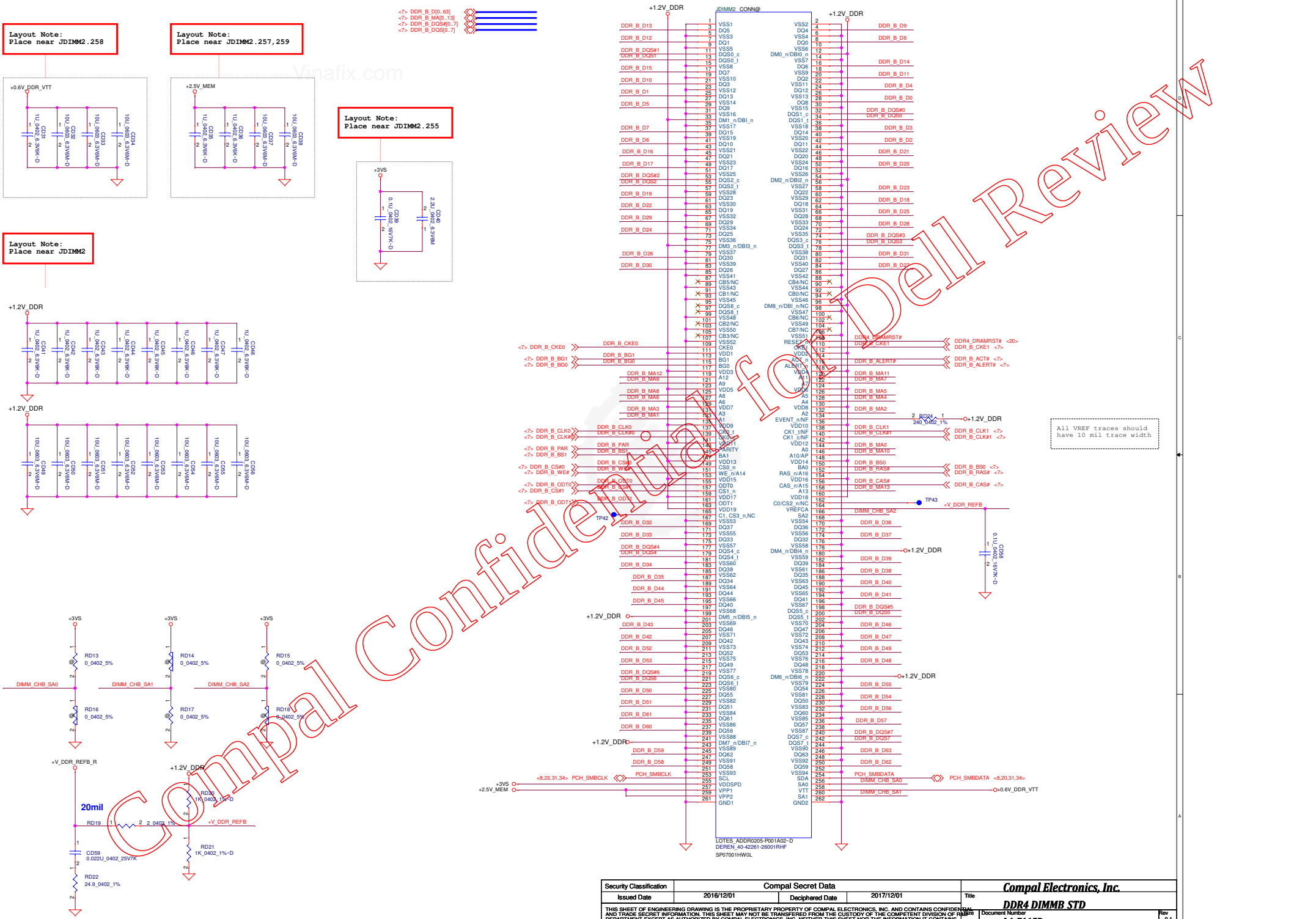
Main Func = DDR

Layout Note:
Place near JDIMM2.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMM2



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	DDR4 DIMMB STD		
Size	Document Number		Rev
	LA-F115P		0.1
Date:	Friday, July 28, 2017	Sheet	21 of 65

Main Func = TPM

Screw hole/FD

H1 HOLEA H_3P0
H3 HOLEA H_5P0
H4 HOLEA H_3P0
H5 HOLEA H_3P0-G
H6 HOLEA H_3P0-G
H7 HOLEA H_3P0
H8 HOLEA H_3P3-G
H9 HOLEA H_3P5
H10 HOLEA H_3P5
H11 HOLEA H_3P2
H12 HOLEA H_3P2-G
H13 HOLEA H_3P0X4P0
H14 HOLEA H_5P6N
HCPU1 HOLEA H_4P0X3P7
HCPU2 HOLEA H_3P7
HCPU3 HOLEA H_4P0
HCPU4 HOLEA H_3P7X4P0
FD1
FD2
FD3
FD4

NPCT650:TPM@/650@/650@750@
NPCT750:TPM@/750@/650@750@
ChinaTPM:TPM@/cTPM@
SW TPM:fTPM@

UX1 SA0000AQ200 750@
S IC NPCT750JAAYX QFN 32P TPM

+3.3V_SPI — RX4 1 TPM@ 2 TPM_SPI_IRQ# 10K_0402_5%

UX1 NPCT650VB2YX_QFN32_5X5 650@
GPIO0/SDA, GPIO1/SCL, GPIO2/GPX, GPIO3/BADD
LAD0/MISO, LAD1/MOSI, LAD2/SPI_IRQ#, LAD3
LCLK/SCLK, LFRAME#/SCS#, LRESET#/SPI_RST#/SRESET#, SERIRQ, CLKRUN#/GPIO4/SINT#, LPCPD#, PP, TEST
VSB, VDD1, VHIO1, VHIO2, NC1–NC7, GND1–GND4, PGND, Reserved

<11,17,25> SIO_SLP_S0# — RX9 650@ / RX10 750@ 0_0402_5%
<8> PCH_SPI_D1 — RX1 TPM@ 33_0402_5% PCH_SPI_D1_TPM
<8> PCH_SPI_D0 — RX2 TPM@ 33_0402_5% PCH_SPI_D0_TPM
<8> TPM_SPI_IRQ# — TPM_SPI_IRQ#
<8> PCH_SPI_CLK — RX3 TPM@ 33_0402_5% PCH_SPI_CLK_TPM
<8> PCH_SPI_CS#2
<11,25,32,34,35,37,44> PLTRST#
RX5 10K_0402_5% 650@750@
RX8 0_0402_5% cTPM@

+3VALW
CX1 10U_0402_6.3V6M TPM@, CX2 0.1U_0402_10V7K TPM@ — CX1, CX2: colse to Pin1
+3VS
CX3 0.1U_0402_10V7K TPM@, CX4 10U_0402_6.3V6M TPM@ — CX3, CX4: colse to Pin8
RX5 0_0402_5% cTPM@ +3VS
RX7 0_0402_5% 650@750@ +3.3V_SPI
CX7 0.1U_0402_10V7K TPM@, CX6 0.1U_0402_10V7K TPM@, CX5 10U_0402_6.3V6M TPM@ — CX5, CX6: colse to Pin14; CX7: colse to Pin22

UX1 place colse to UC3

Main Func = RTC

+RTC_VCC, +3VLP, +RTC_CELL
R1 1K_0402_5% RTC_PWR
D1 BAS40C_SOT23-3 (anode, cathode, anode)
C1 0.47U_0402_6.3V6K @
R2 10M_0402_5%
Q1 2N7002K_SOT23-3
RTC_DET# <9>

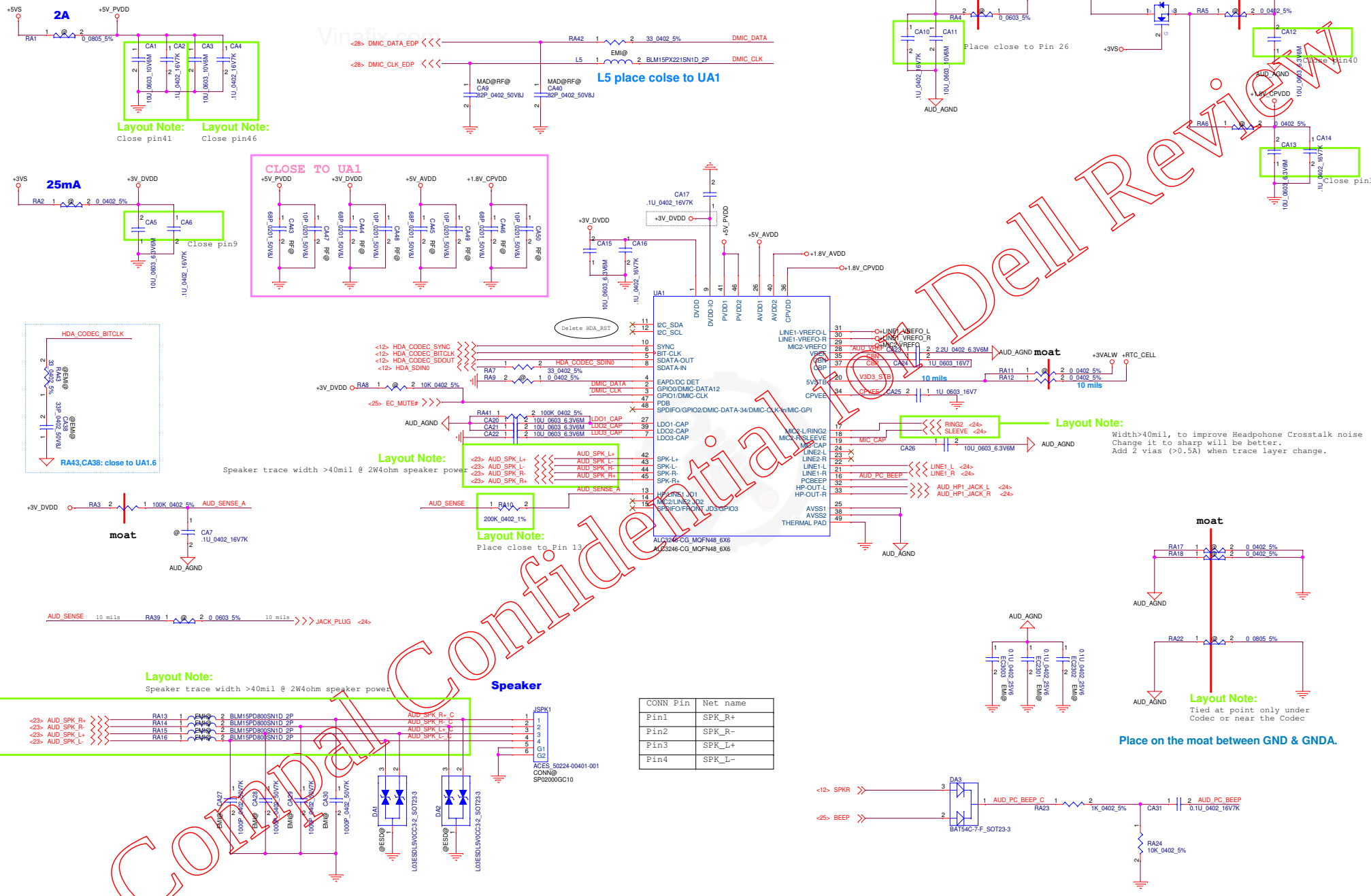
+RTC_CELL_PCH, +RTC_CELL
Q23 GEN9@ LP2301ALT1G_SOT23-3
C59 GEN9@ 1U_0402_6.3V6K
R73 GEN9@ 10K_0402_5%
D7 GEN9@ RB751S40T1G_SOD523-2
Q24 GEN9@ L2N7002WT1G_SC-70-3
R78 GEN9@ 1M_0402_5%
RTCRST_ON, RTCRST_ON <11,25>
C60 GEN9@ 22P_0402_50V8J
R79 GEN9@ 100K_0402_5%
C61 @ 0.1U_0402_25V6

+3VALW_PCH, +3.3V_ALW_DSW, +3VALW
R84 GEN9@ 0_0402_5%
Q15 LP2301ALT1G 1P SOT-23-3 DSX@
R65 499K_0402_1% DSX@
R66 GEN9@ 100K_0402_5%
VCCDSW_ON <25>
R67 DSX@ 49.9K_0402_1%
Q4 DSX@ L2N7002WT1G_SC-70-3

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.
Title: TPM/RTC/Screw hole
Size: B2 | Document Number: LA-F115P | Rev: 0.1
Date: Friday, July 28, 2017 | Sheet 22 of 65

Main Func = Audio

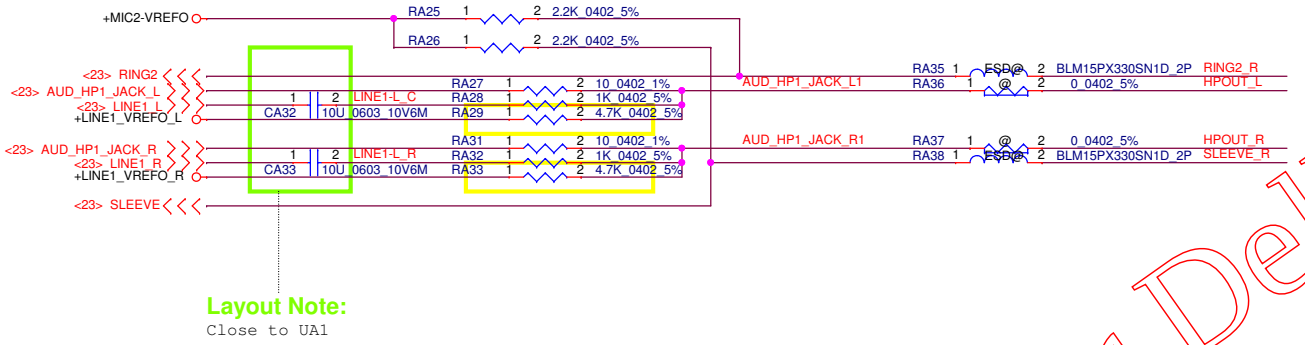


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	Audio Codec ALC3246		
Size	Document Number LA-F115P		Rev 0.1
Date: Friday, July 28, 2017		Sheet 23 of 65	

Main Func = Audio Jack



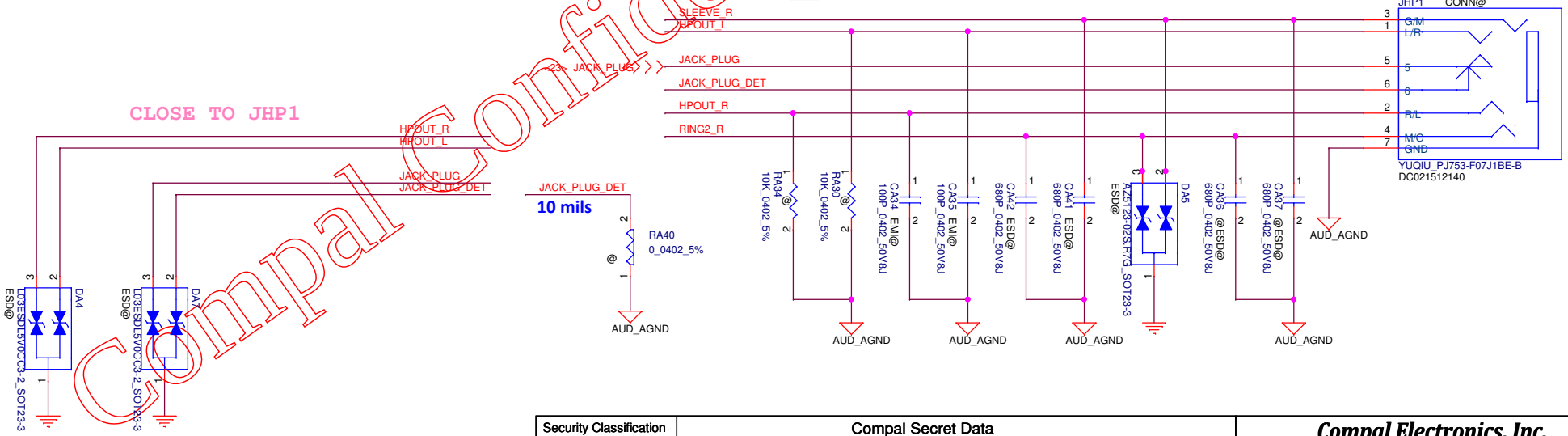
Layout Note:
Close to UA1

Universal Jack
(Global Headset Jack + mic phone in + line in support)

Main Func = Audio Jack

Universal Jack
(Global Headset Jack + mic phone in + line in support)

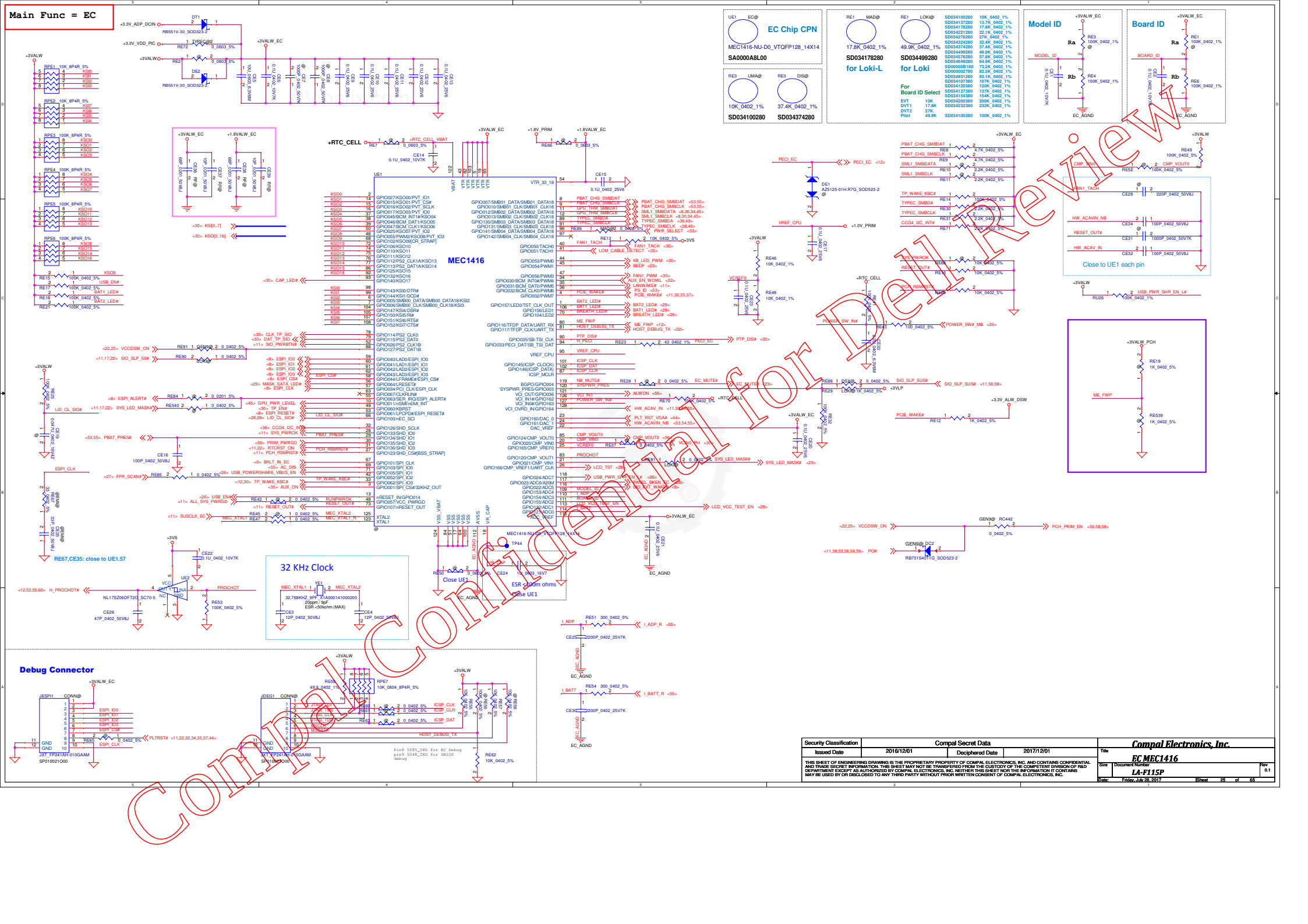
CLOSE TO JHP1



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.		
Title: Audio JACK		
Size	Document Number: LA-F115P	Rev: 0.1
Date: Friday, July 28, 2017	Sheet 24 of 65	

Main Func = EC



Security Classification	Compal Secret Data	
Issued Date	2016/12/01	Deciphered Date 2017/12/01

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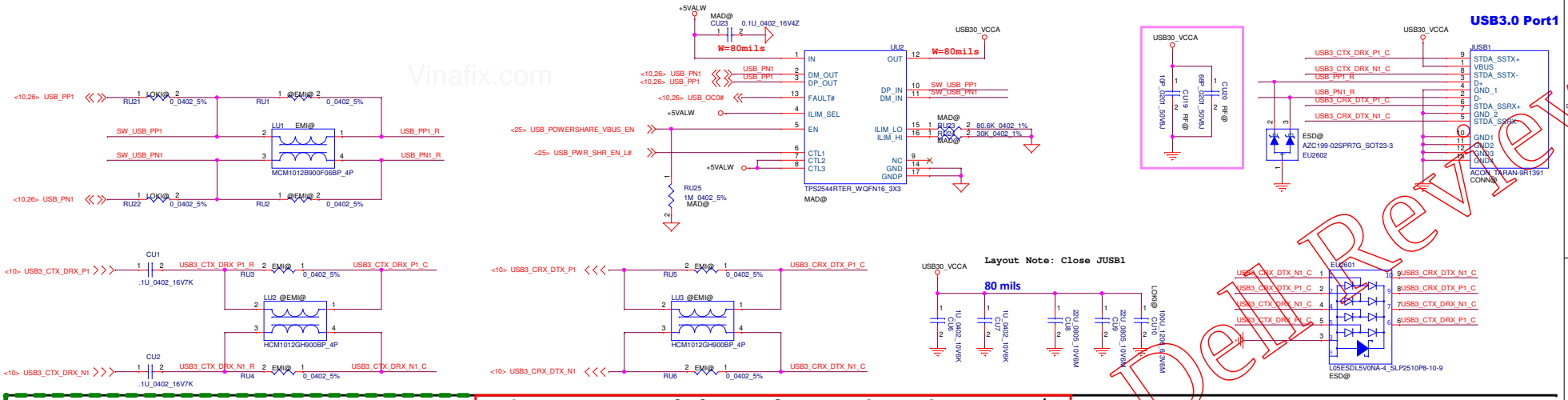
Compal Electronics, Inc.

Title: EC MEC1416

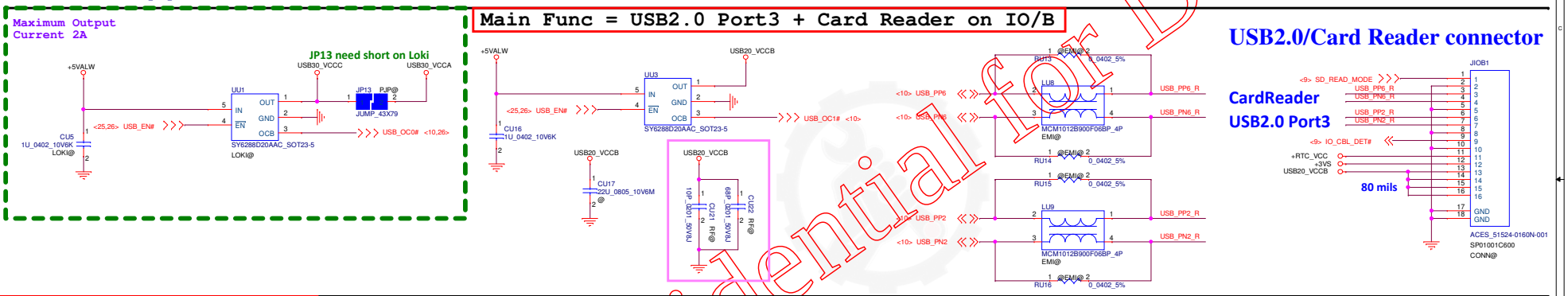
Size: LA-F115P | Document Number | Rev 0.1

Date: Friday, July 28, 2017 | Sheet 25 of 65

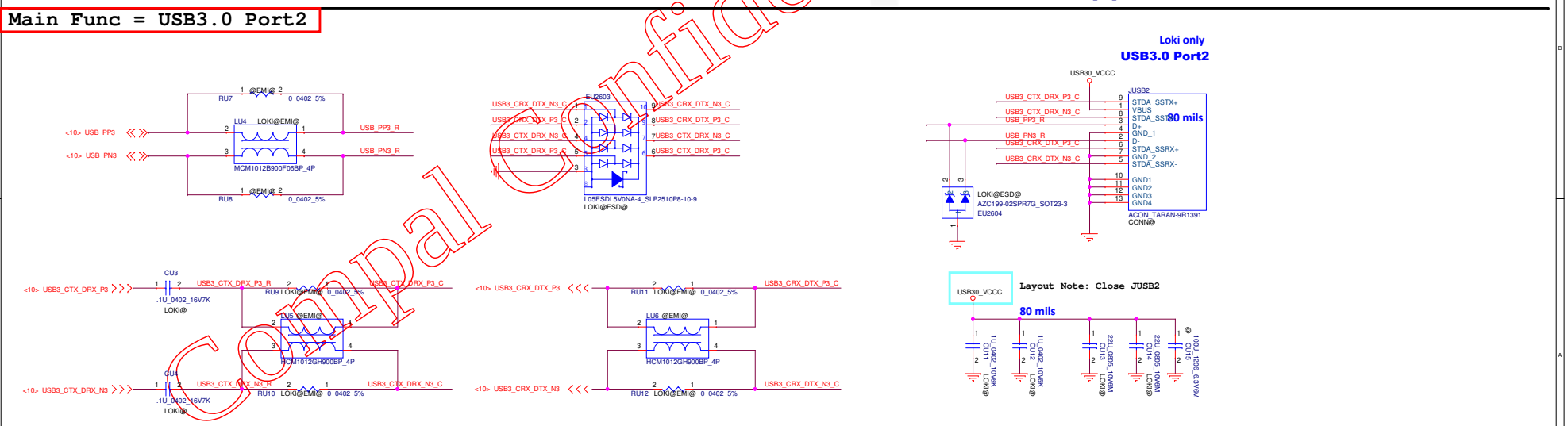
Main Func = USB3.0 Port1



Main Func = USB2.0 Port3 + Card Reader on IO/B



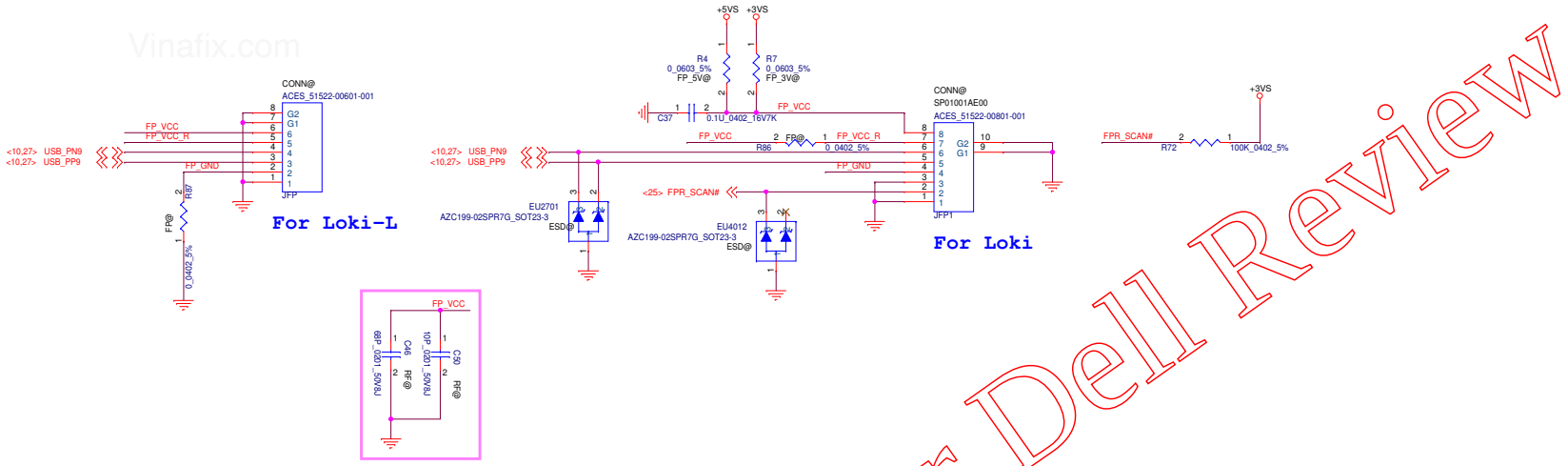
Main Func = USB3.0 Port2



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.	
Title	USB3.0 & I/O
Size	Document Number: LA-F115P
Rev	0.1
Date: Friday, July 28, 2017	Sheet 26 of 65

Main Func = Finger Printer

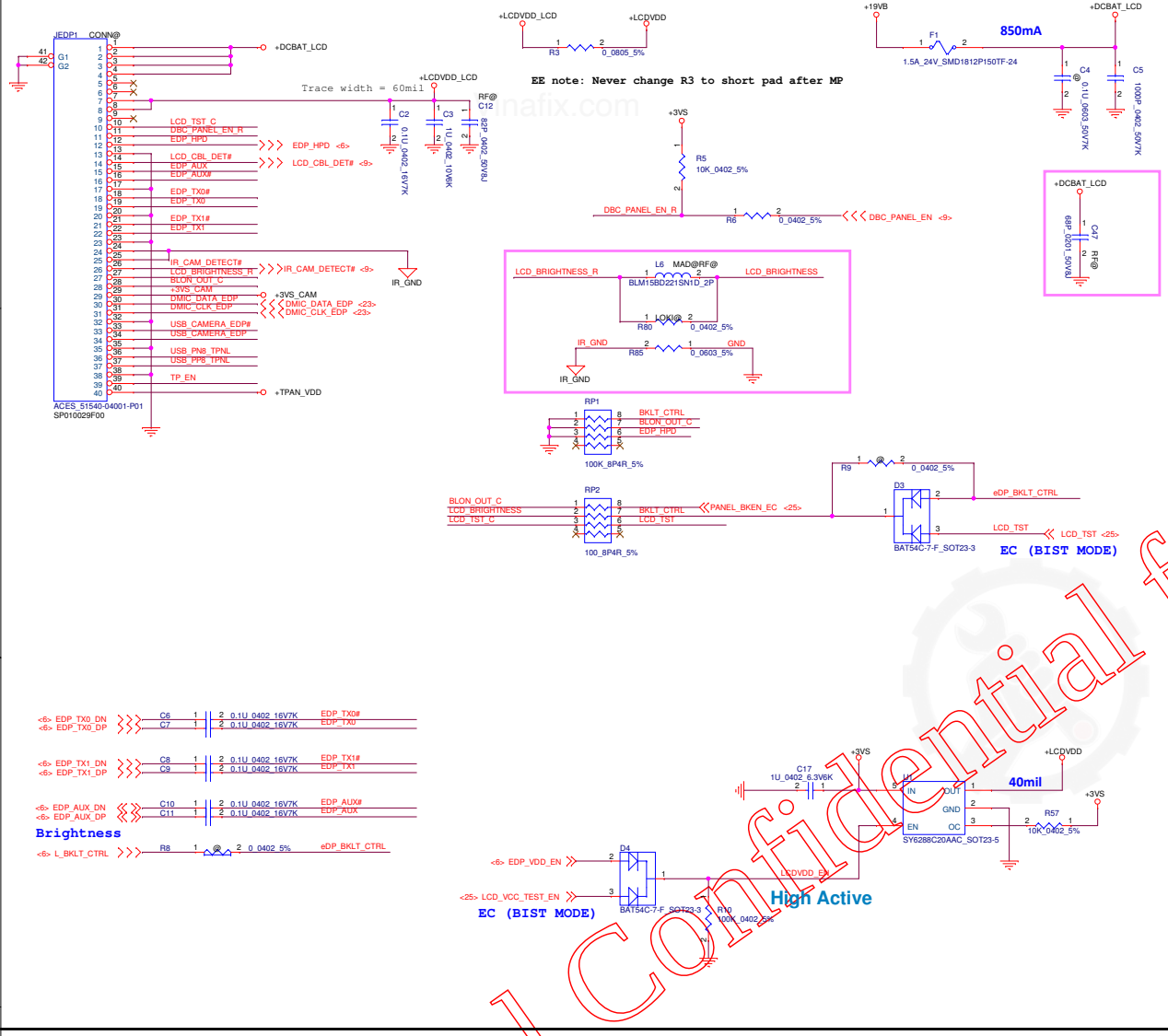


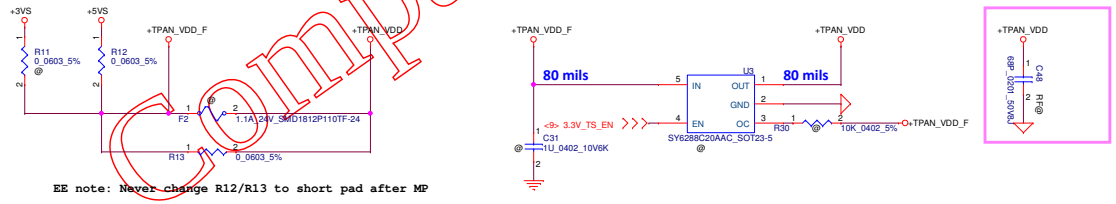
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: Finger Print			
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017		Sheet 27 of 65	

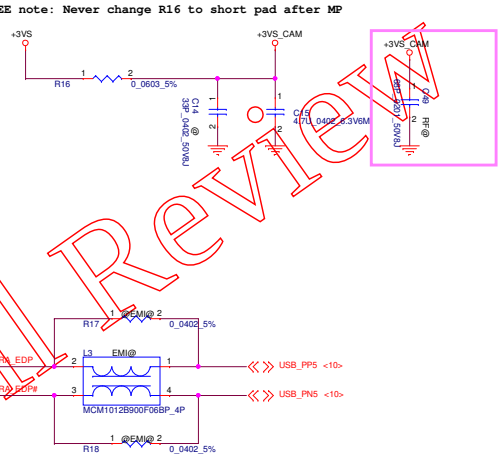
Main Func = LCD

INVERTER POWER

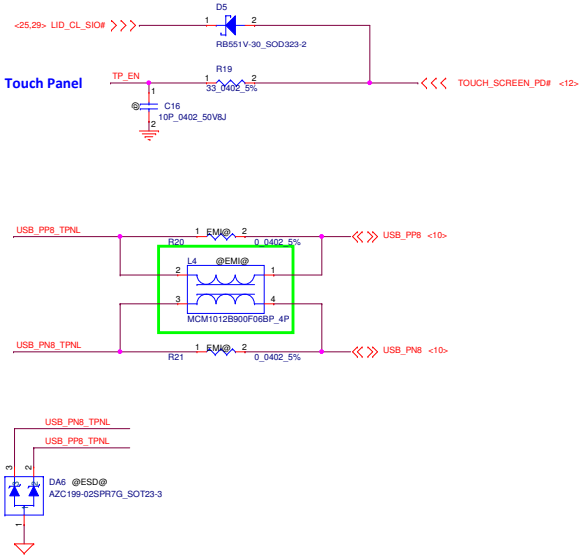




Main Func = CAM



Main Func = TS



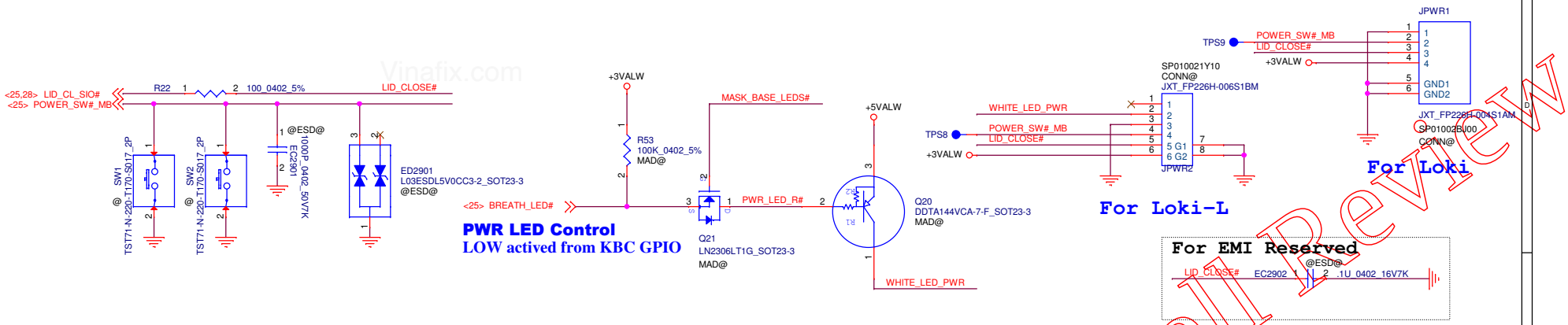
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	LCD/Cam/MIC/T.Panel		
Size	Document Number	LA-F115P	Rev 0.1
Date: Friday, July 28, 2017	Sheet 28 of 65		

Main Func = Power BTN

Main Func = PWR LED

Low actived from KBC GPIO

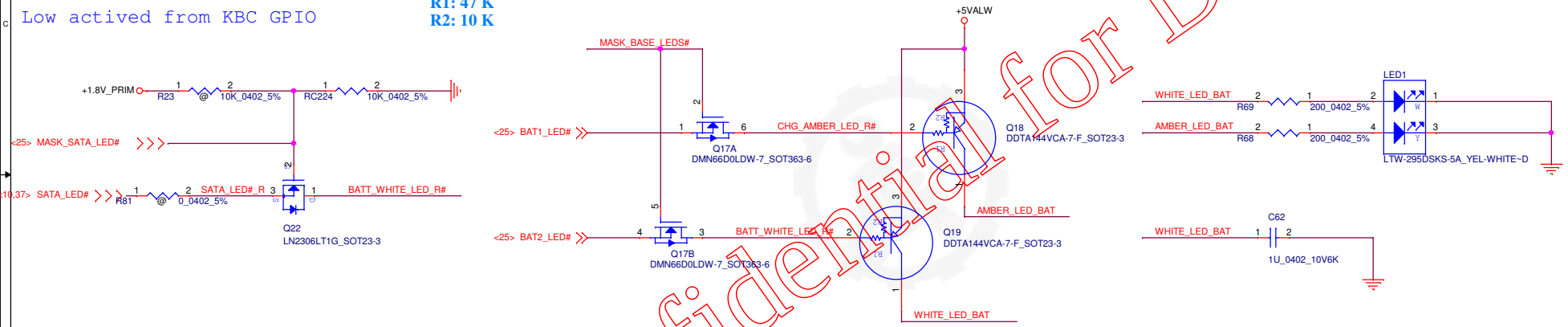


PWR LED Control
LOW actived from KBC GPIO

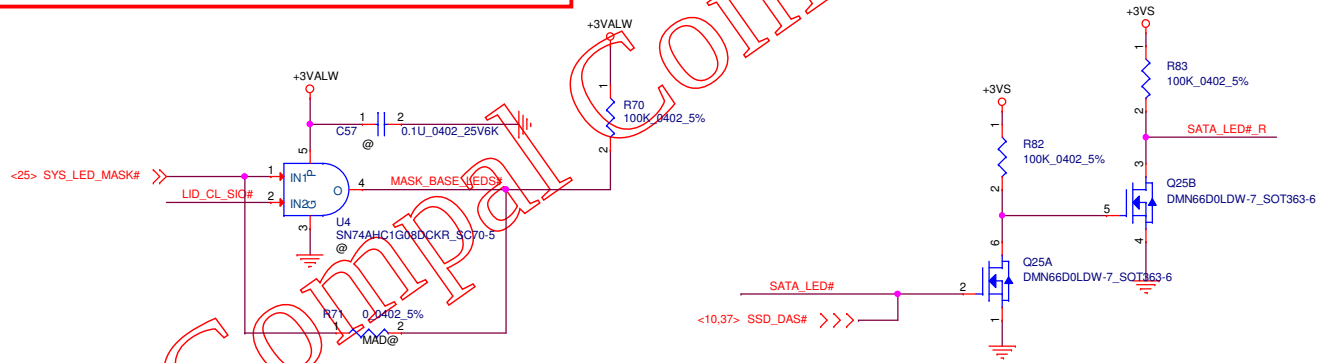
Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



Main Func = Unobtrusive Mode



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: LED Board/Power Button			
Size	Document Number: LA-F115P		Rev: 0.1
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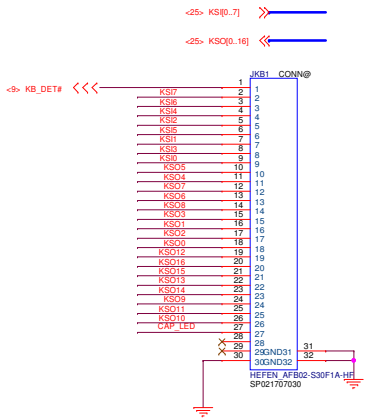
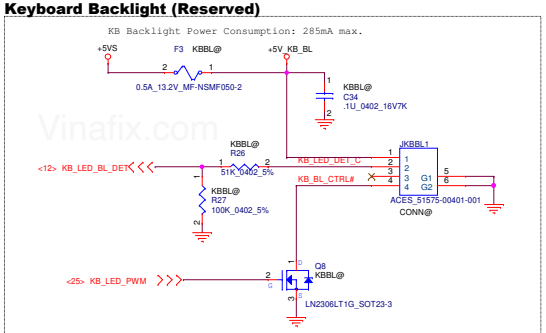
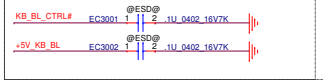
Main Func = KB



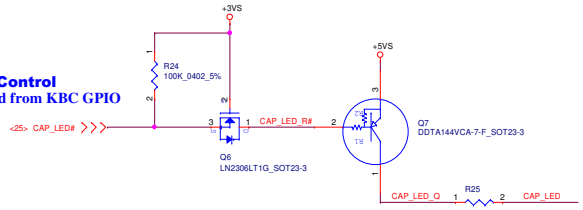
Keyboard Backlight (Reserved)

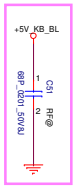


For EMI Reserved

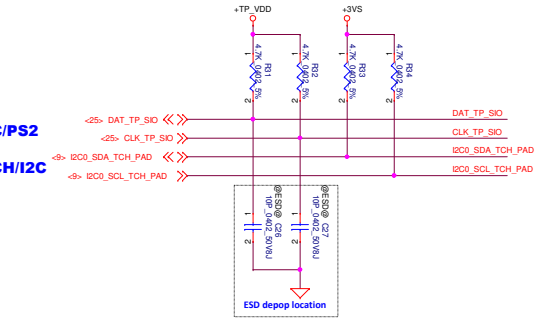


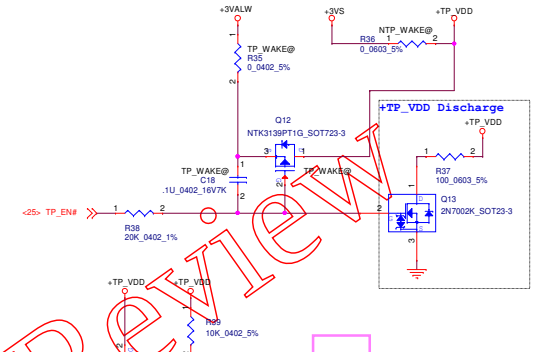
CAP LED Control
LOW actived from KBC GPIO

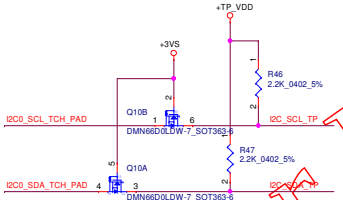




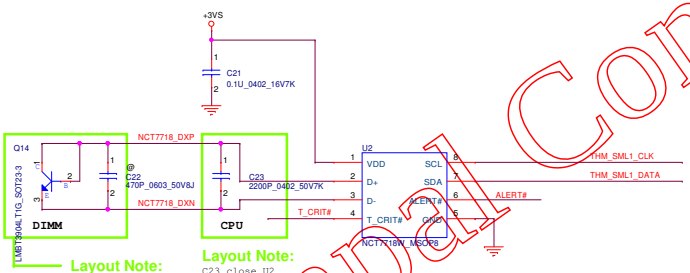
Main Func = TPAD





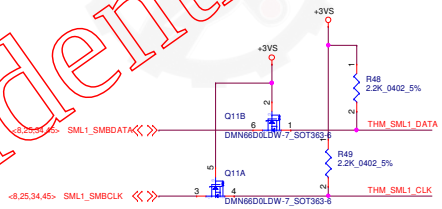


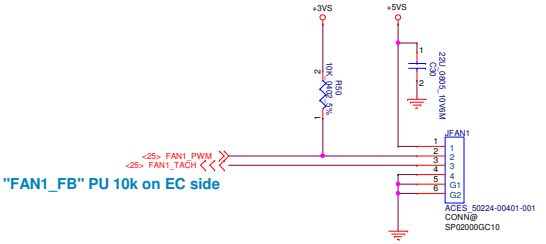
Main Func = Thermal



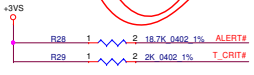
Layout Note:
DXN and DXP routing width and spacing is 10 mil / 10 mil.

Layout Note:
C23 close U2





"FAN1_FB" PU 10k on EC side

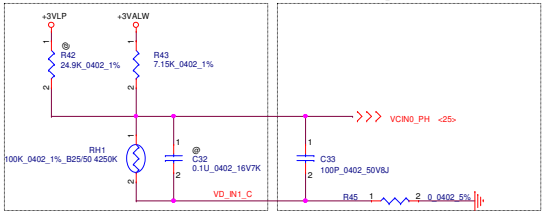


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Main Func = OTP

Close to Thermal sensor

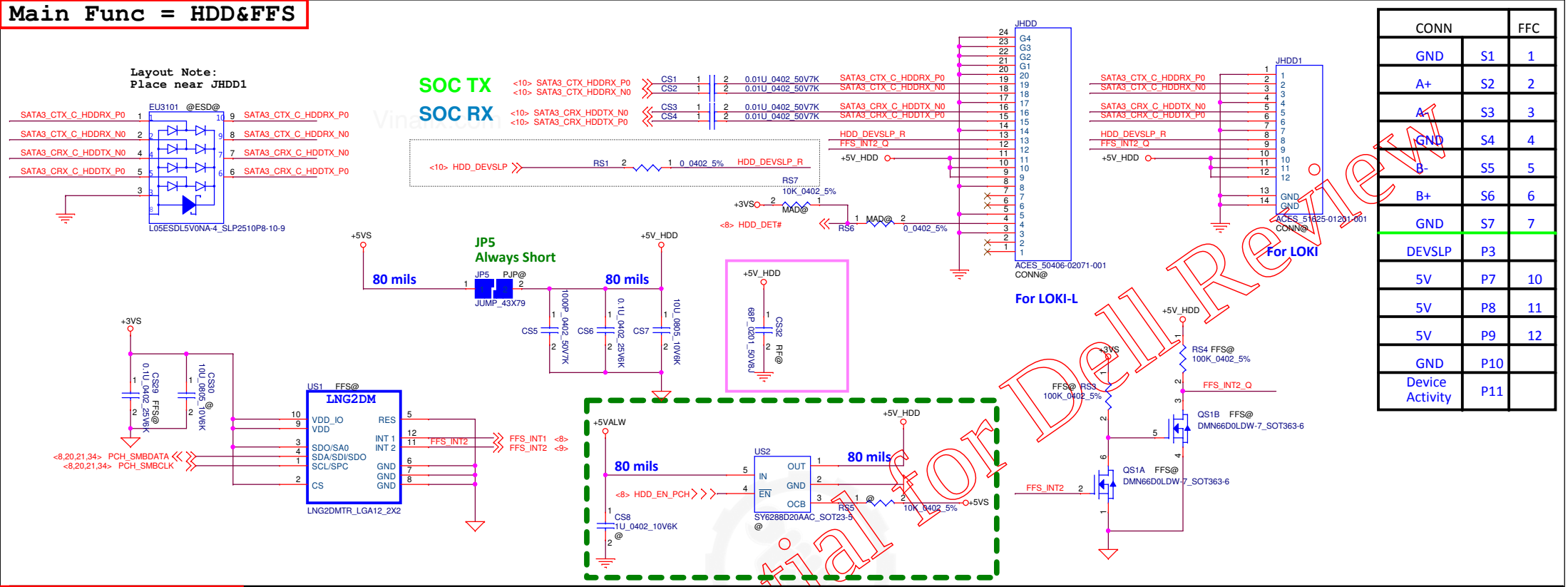
Close to KBC
VD_IN1 for system thermal sensor



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

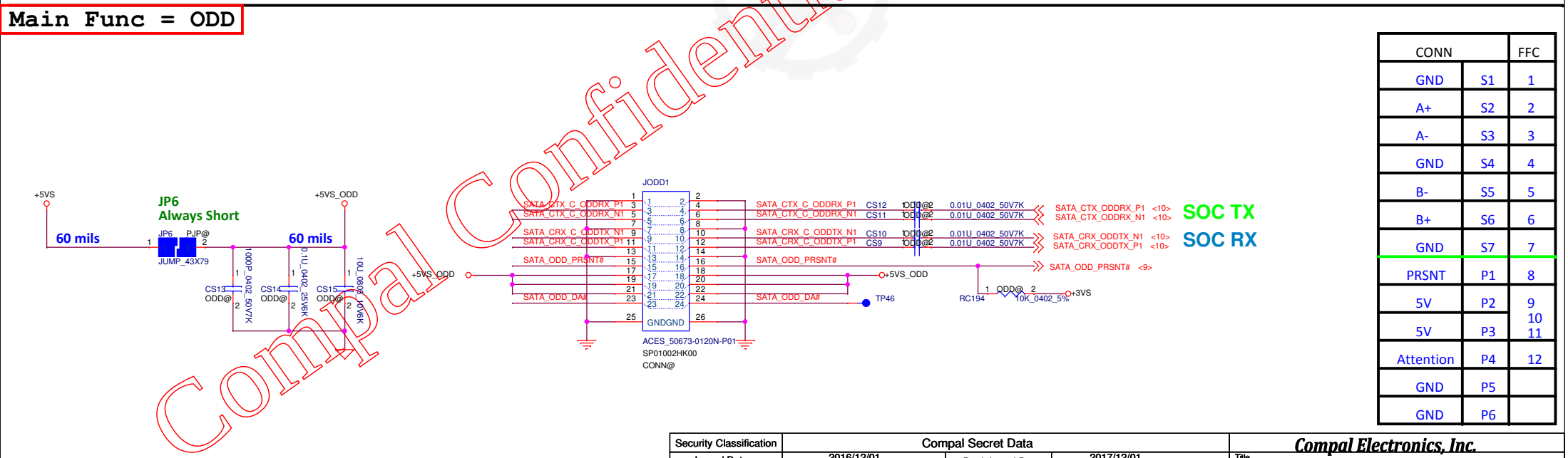
Compal Electronics, Inc.			
Title	Keyboard/Touch Pad/Thermal/FAN		
Size	Document Number	Rev	
	LA-F115P	0.1	
Date: Friday, July 28, 2017	Sheet 30 of 65		

Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	

Main Func = ODD



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSNT	P1	8
5V	P2	9
5V	P3	10 11
Attention	P4	12
GND	P5	
GND	P6	

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

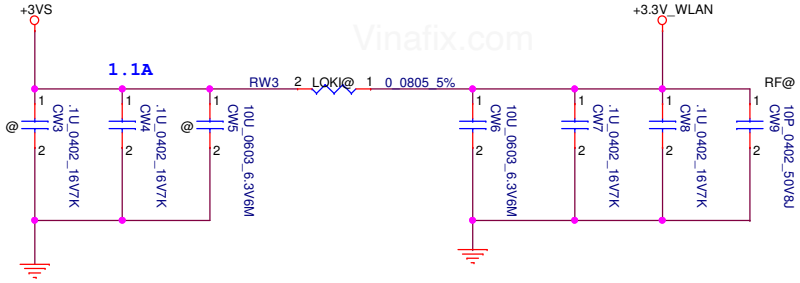
Title: HDD/FFS/ODD

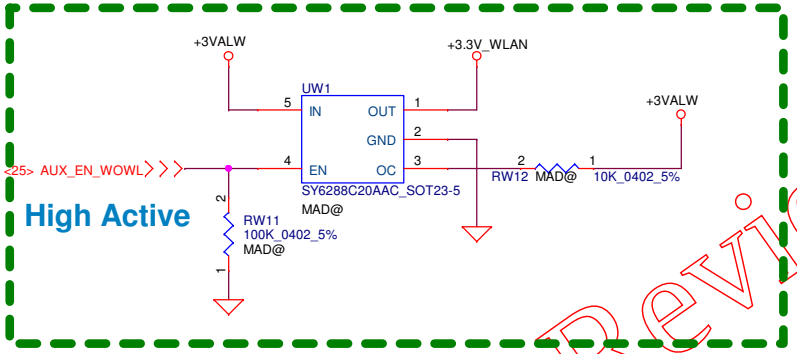
Size: Custom | Document Number: LA-F115P | Rev: 0.1

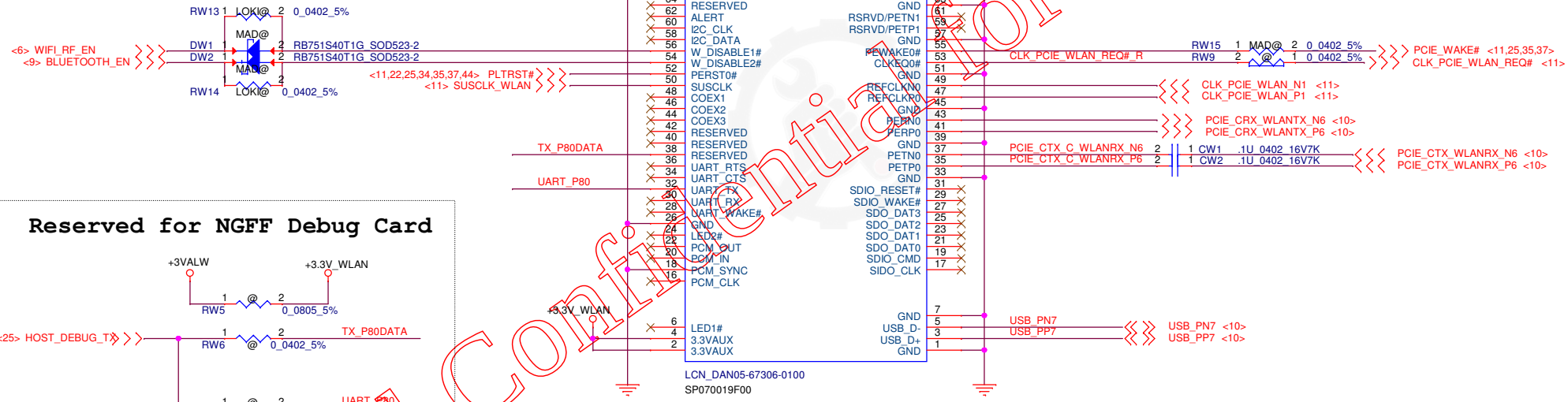
Date: Friday, July 28, 2017 | Sheet 31 of 65

Main Func = WLAN

A Key CONN





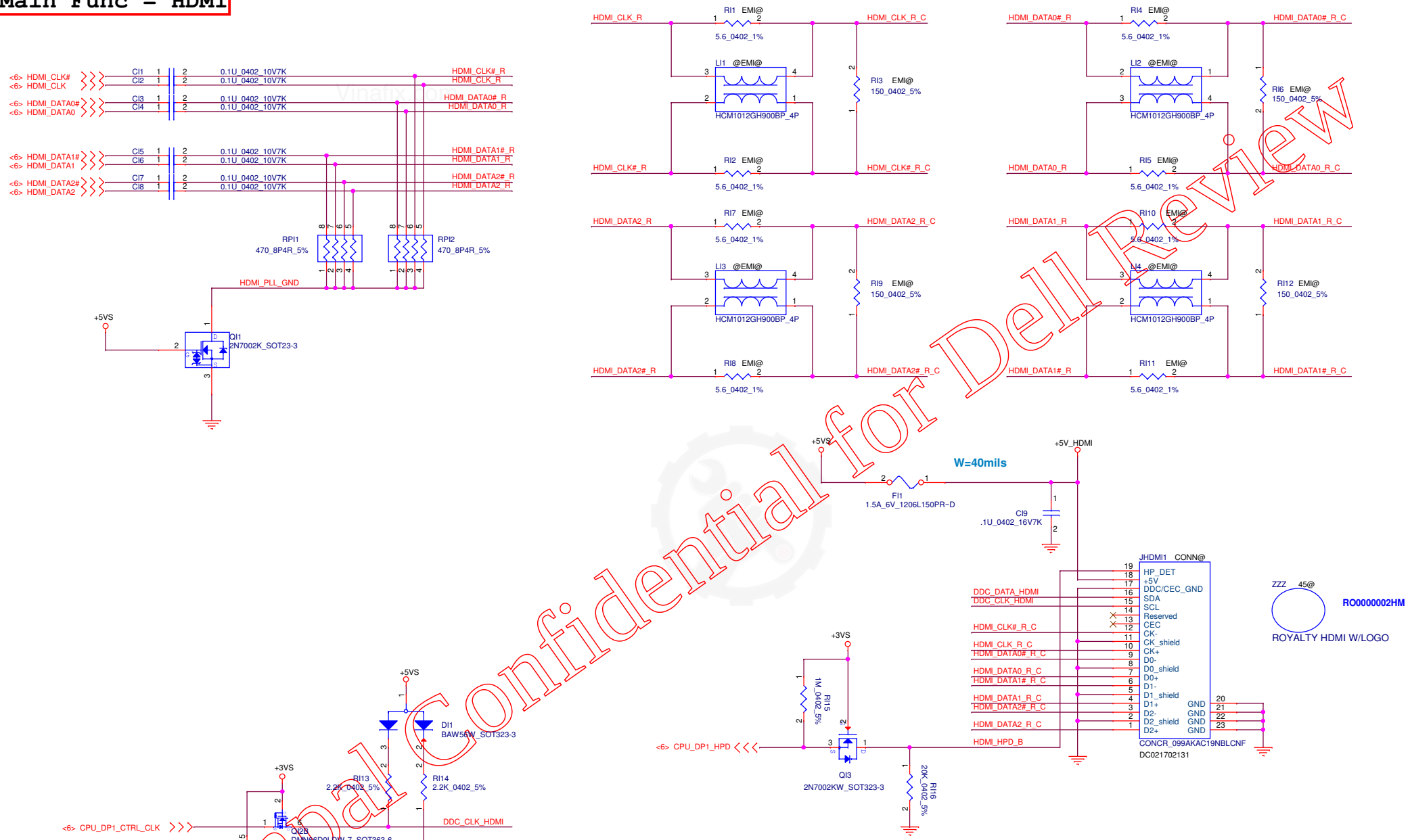


Reserved for NGFF Debug Card

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	NGFF_WLAN CONN		
Size	Document Number		Rev
	LA-F115P		0.1
Date: Friday, July 28, 2017	Sheet 32 of 65		

Main Func = HDMI



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **HDMI L.Shifter/Conn**

Size	Document Number	Rev
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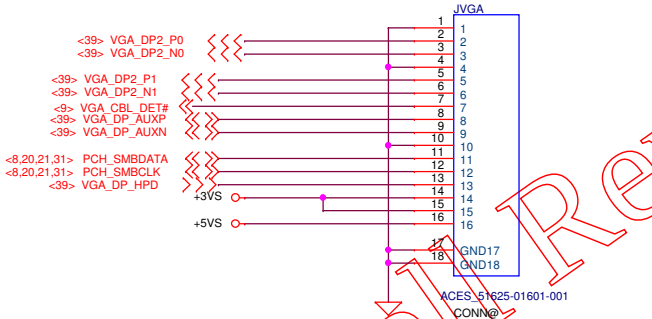
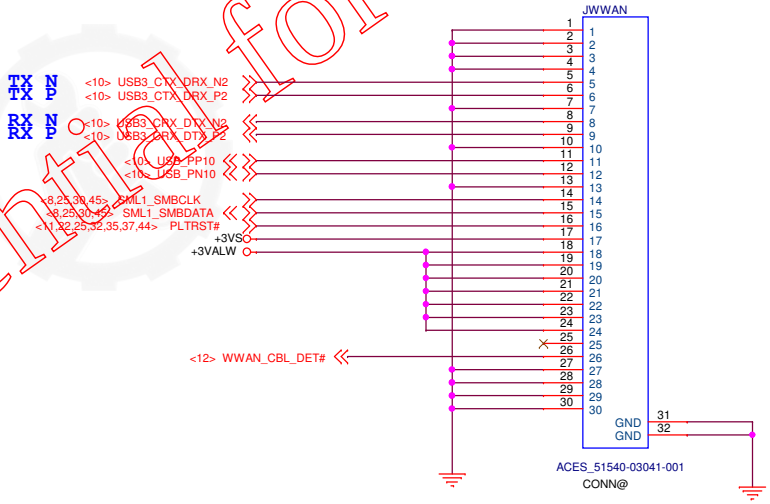
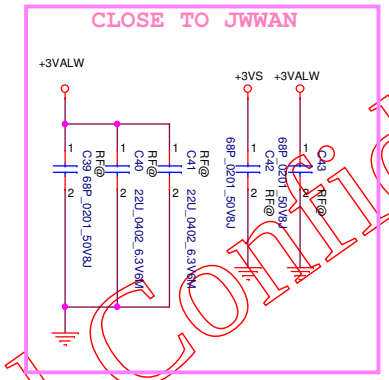
Date: Friday, July 28, 2017 Sheet 33 of 65

Main Func = WWAN/B & VGA/B







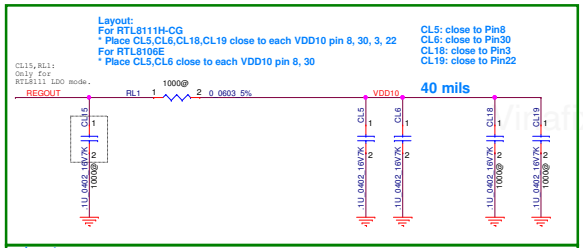
RTL8111G-CGT (71.08111.U03/LDO Mode): 10/100/1000M < 252 mW.
RTL8106E-CG (071.08106.0003): 10/100M <70mW.

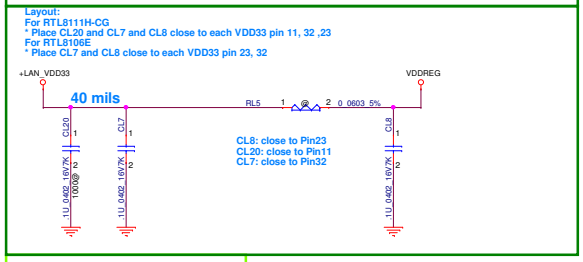
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

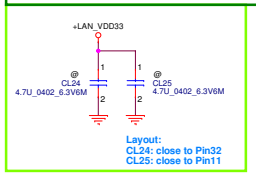
Compal Electronics, Inc.			
Title: IO DB(WWAN/VGA)			
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017	Sheet 34 of 65		

Main Func = LAN

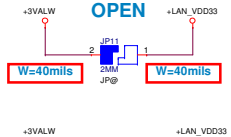
LAN Chip (10/100/1000M & 10/100M co-layout)

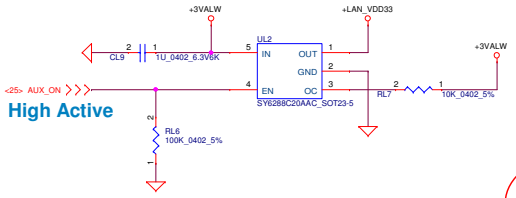


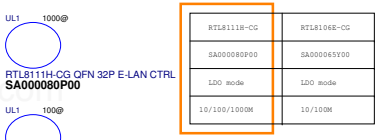


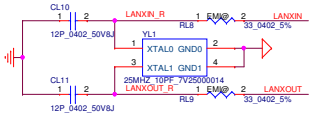


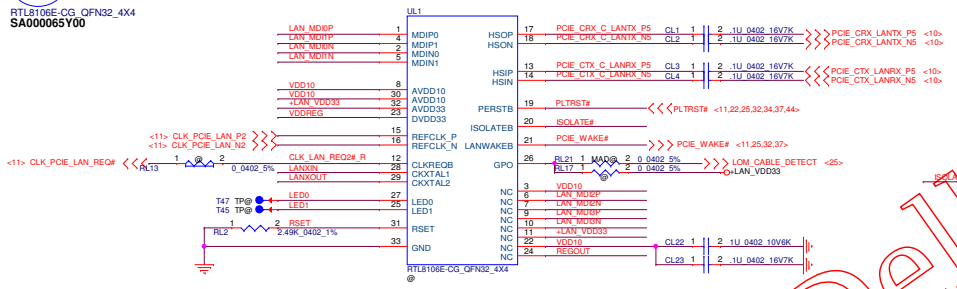
+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



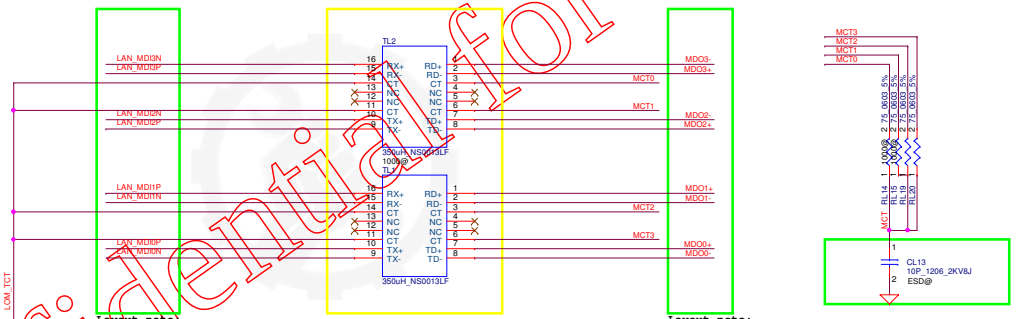






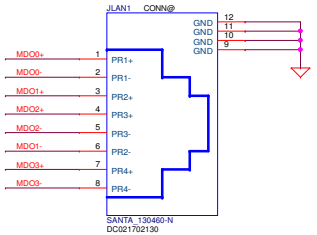


LAN TransFormer (10/100/1000M & 10/100M co-layout)



Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.



	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date 2017/12/01	Title: P35-LAN RTL8111/RTL8106
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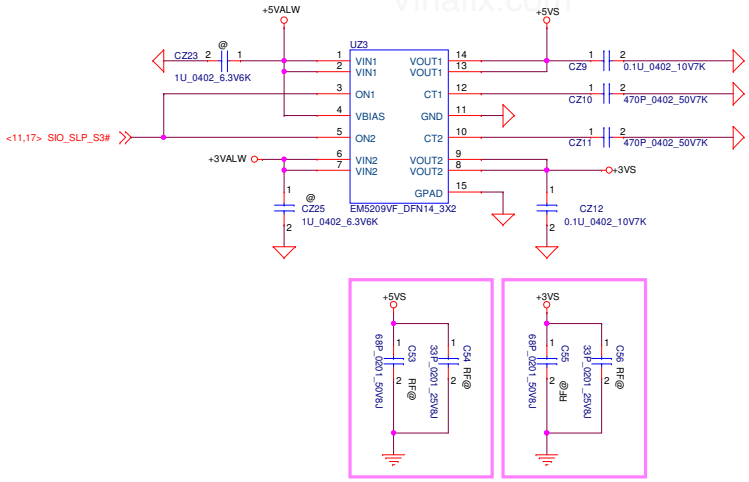
			Date: Friday, July 28, 2017 Sheet 35 of 65

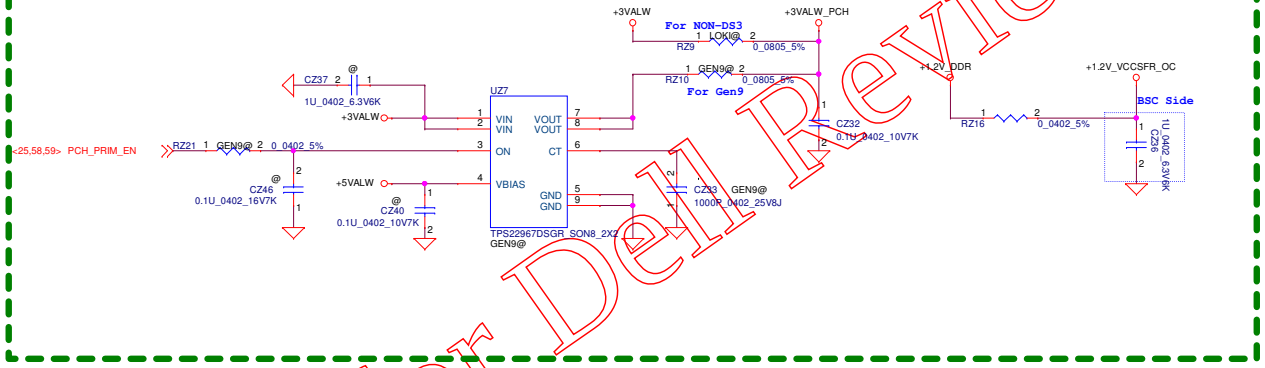
Main Func = DC/DC

+5VS/+3VS for System



+3VALW_PCH for System
+1.2V_DDR TO +1.2V_VCCSFR_OC

NON-DSX(LOKI)
DSX(LOKI-L)



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: DC/DC

Size | Document Number: LA-F115P | Rev: 0.1

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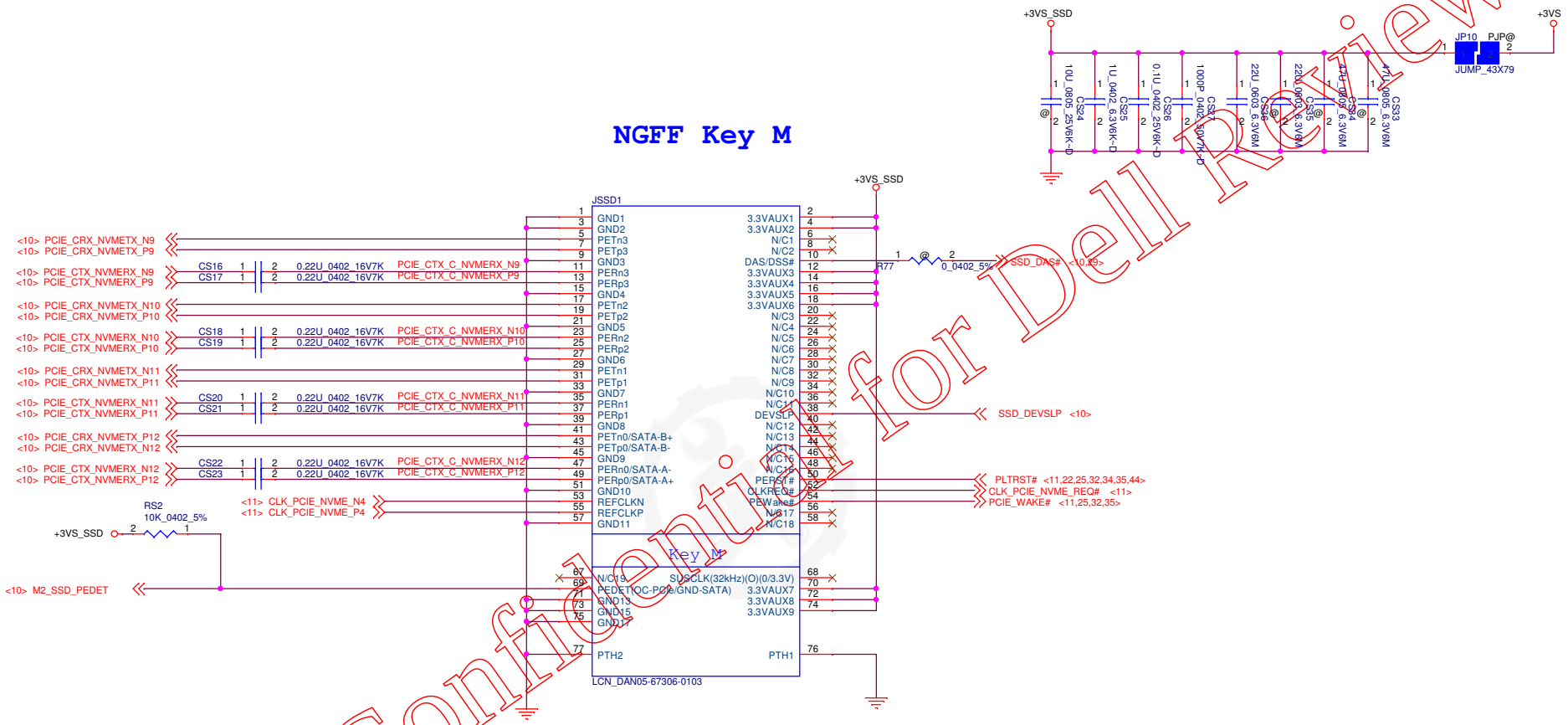
Main Func = SSD

M Key CONN

NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: NVME SSD			
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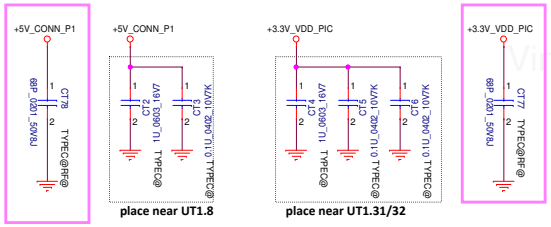
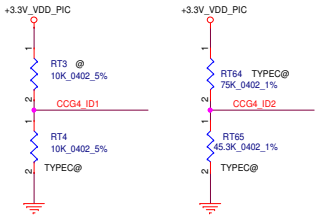
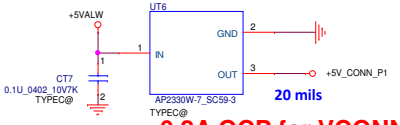
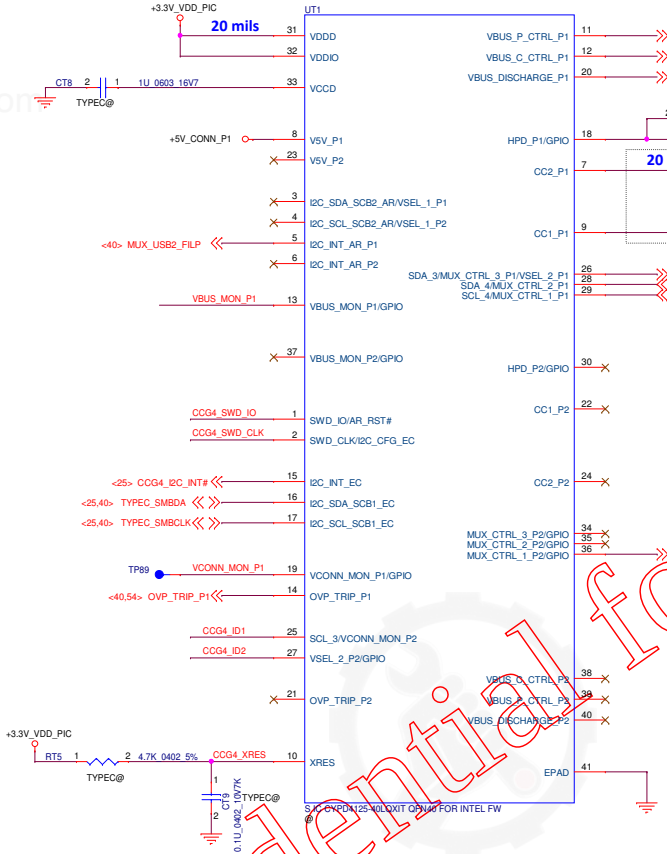
Main Func = CCG4

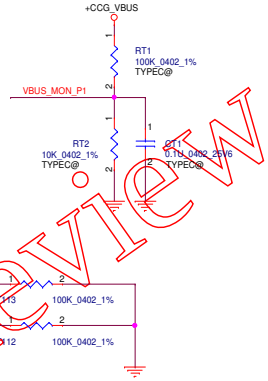


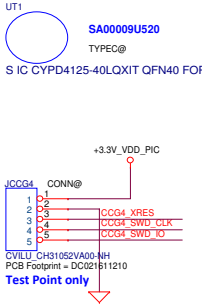


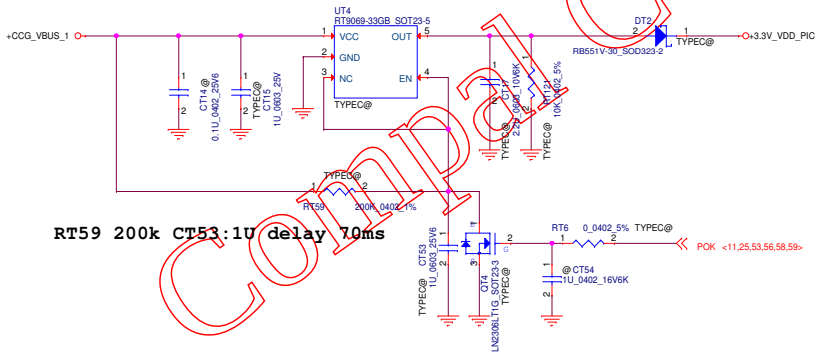


0.2A OCP for VCONN!









Voltages for various platform on "CCG4_ID_1" pin and "CCG4_ID_2" pin

#	Platform	Voltage on CCG4_ID_1	Voltage on CCG4_ID_2
1	Single Port - Intel - DDM support - Armani 13" & 14"	L0	L7
2	Single Port - Intel - DDM support - Kyloren	L0	L6
3	Single Port - Intel - DDM support - Miyake	L0	L5
4	Single Port - Intel - DDM support - Loki 13"	L0	L4
5	Single Port - Intel - DDM support - Loki 15" & 17" (Motherboard is same)	L0	L3
6	Single Port - Intel - DDM support - StarLord KBL - R	L0	L2
7	Single Port - AMD - DDM not supported - Loki 15" & 17" (Motherboard is same)	L4	L0

Voltage level	Voltage value
L0	0V
L1	3.3V
L2	3.3V/2
L3	3.3V/3
L4	3.3V/4
L5	3.3V/5
L6	3.3V/6
L7	3.3V/7

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Compal Electronics, Inc.			
Title	Cypress PD Control		
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Main Func = typec MUX & DP MUX

Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.		
Title: Dual Role Mux		
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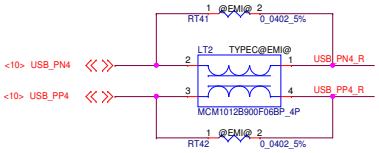
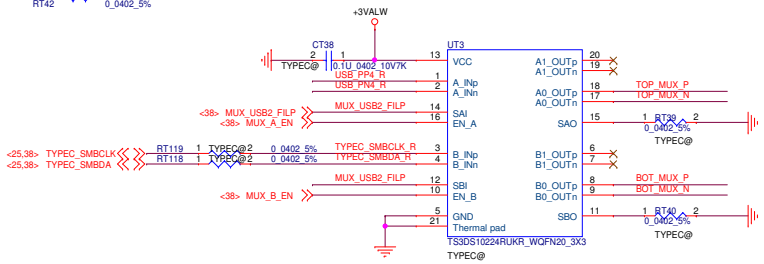
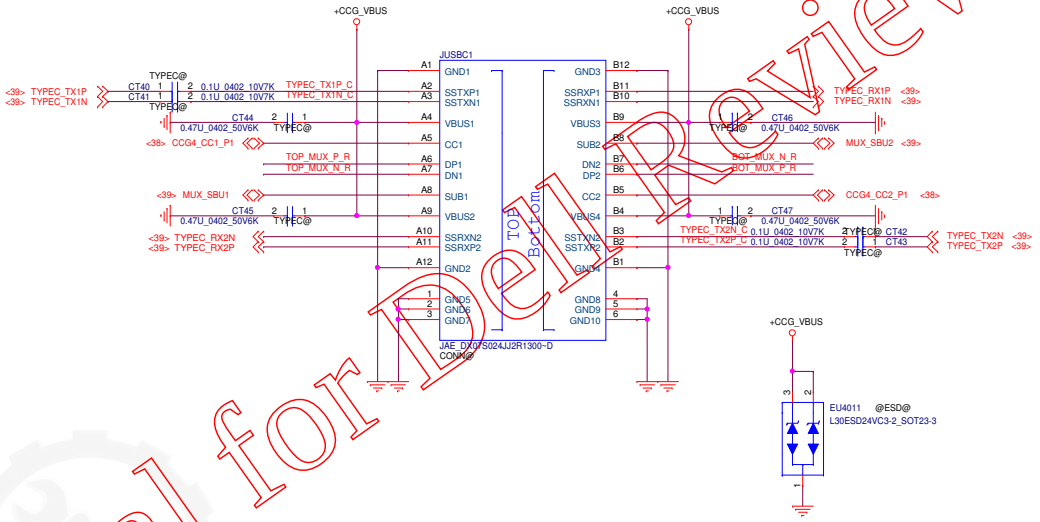
Main Func = USB2/I2C Mux

Close to JUSBC1 <500mil

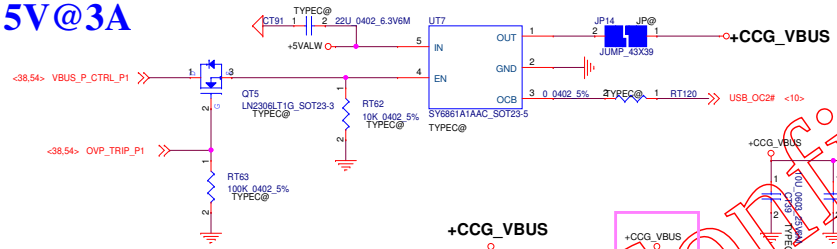


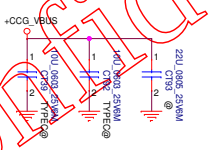


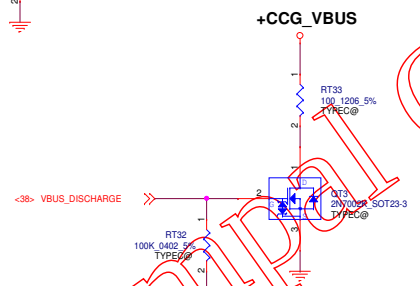
MUX_USB2_FILP	MUX_A_EN	MUX_B_EN	A0_OUT	B0_OUT
0	0	1	--	USB2
0	1	1	I2C	USB2
1	1	0	USB2	--
1	1	1	USB2	I2C

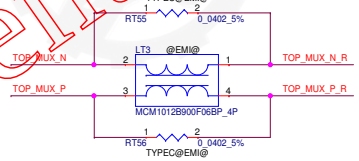


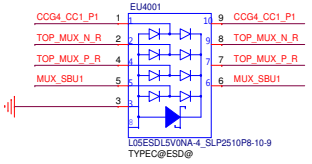
5V@3A

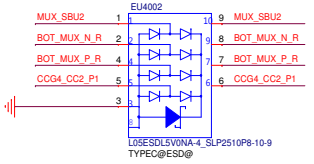


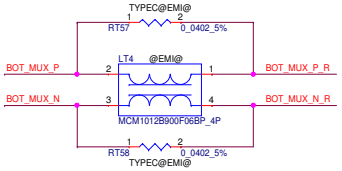


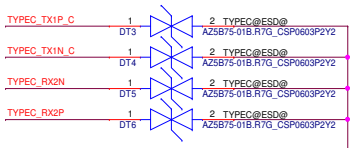


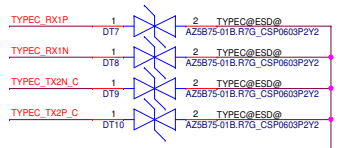












Type-C 5V Provide Path Control

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Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: TYPE-C			
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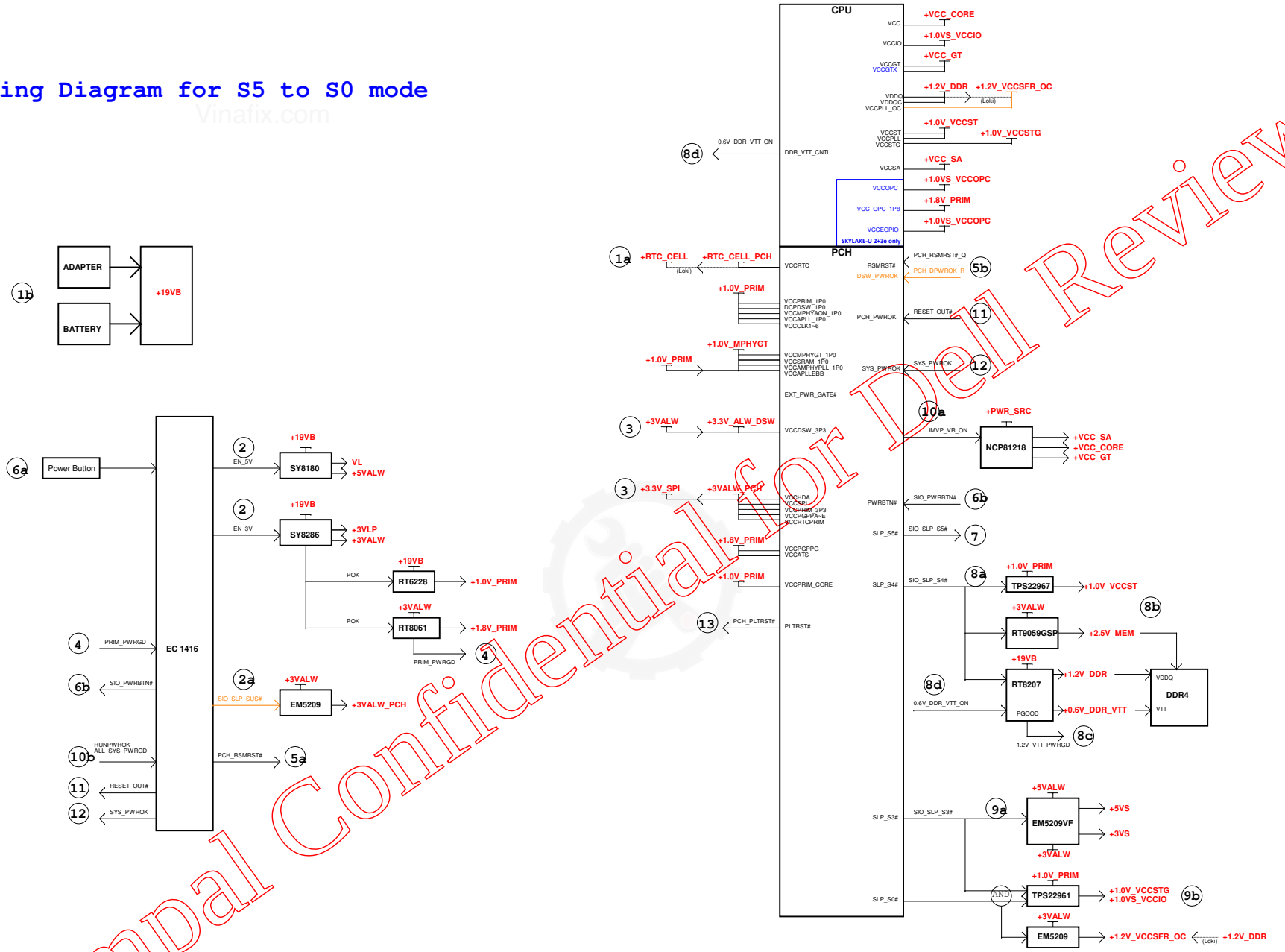
Timing Diagram for S5 to S0 mode



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date	2017/12/01
Title	Platform Power Sequence		
Size	Document Number		Rev
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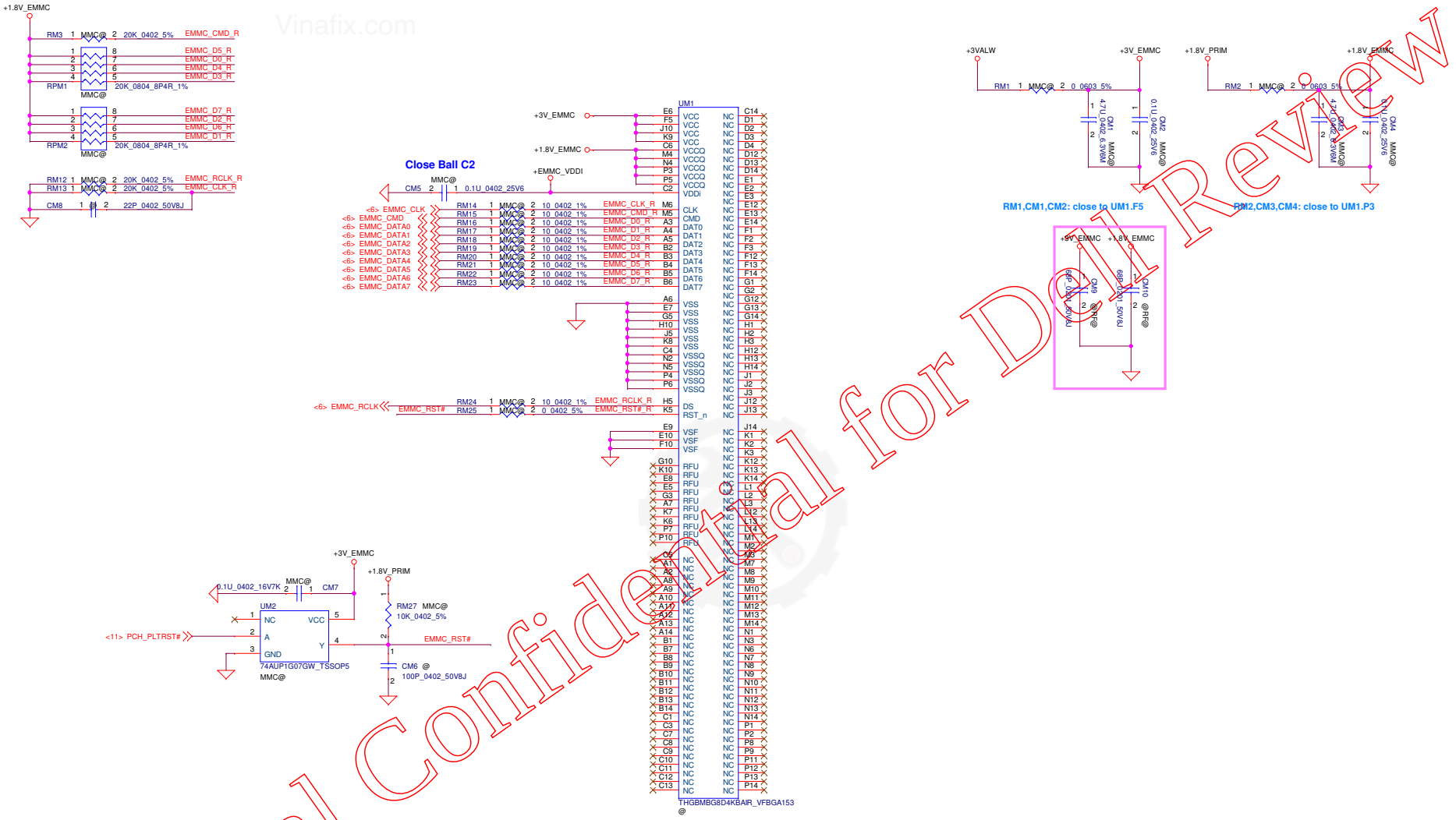
Main Func = eMMC



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Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	RAV for eMMC		
Size	Document Number		Rev
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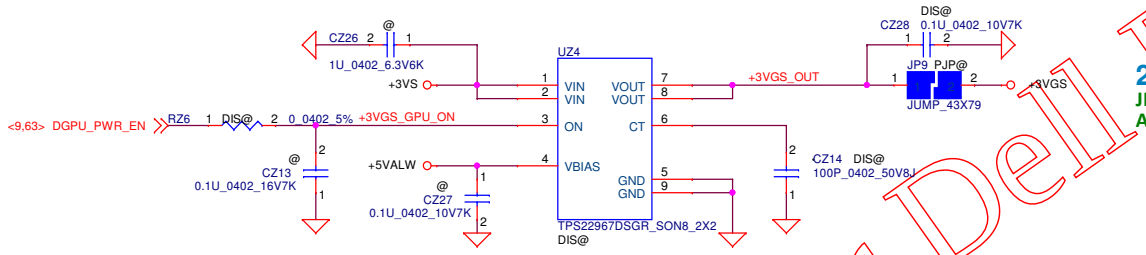
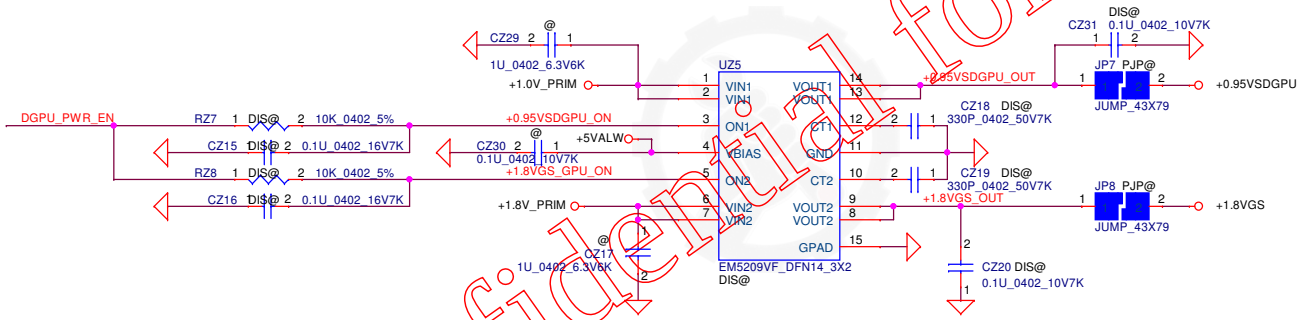
Main Func = GPU

+3V/+0.95V/+1.8V for GPU

Maximum Output Current 4A



250mA
JP9
Always Short



2300mA
JP7
Always Short

500mA
JP8
Always Short

Maximum Output Current 6A

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: GPU Power			
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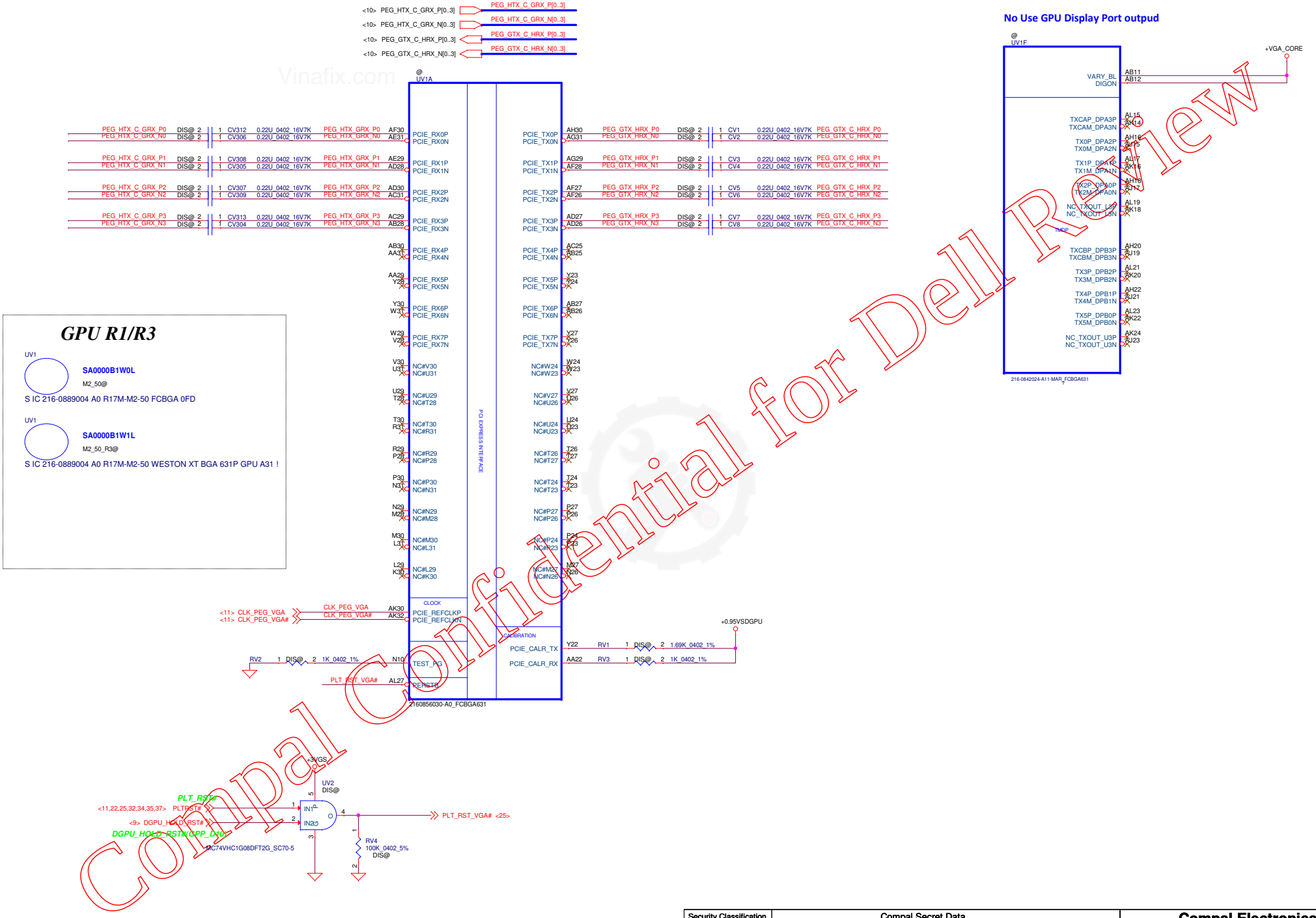
Main Func = GPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MESO_(1/5)_PCIE/DP

Size: | Document Number: LA-F115P | Rev: 0.1

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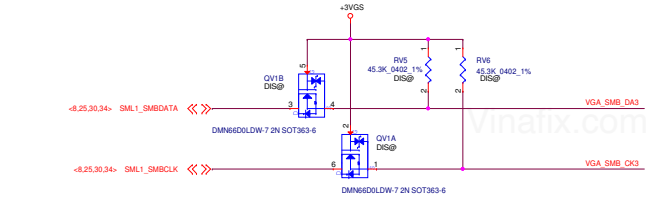
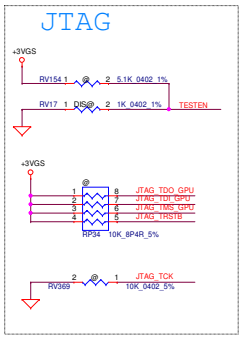
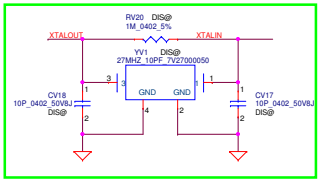
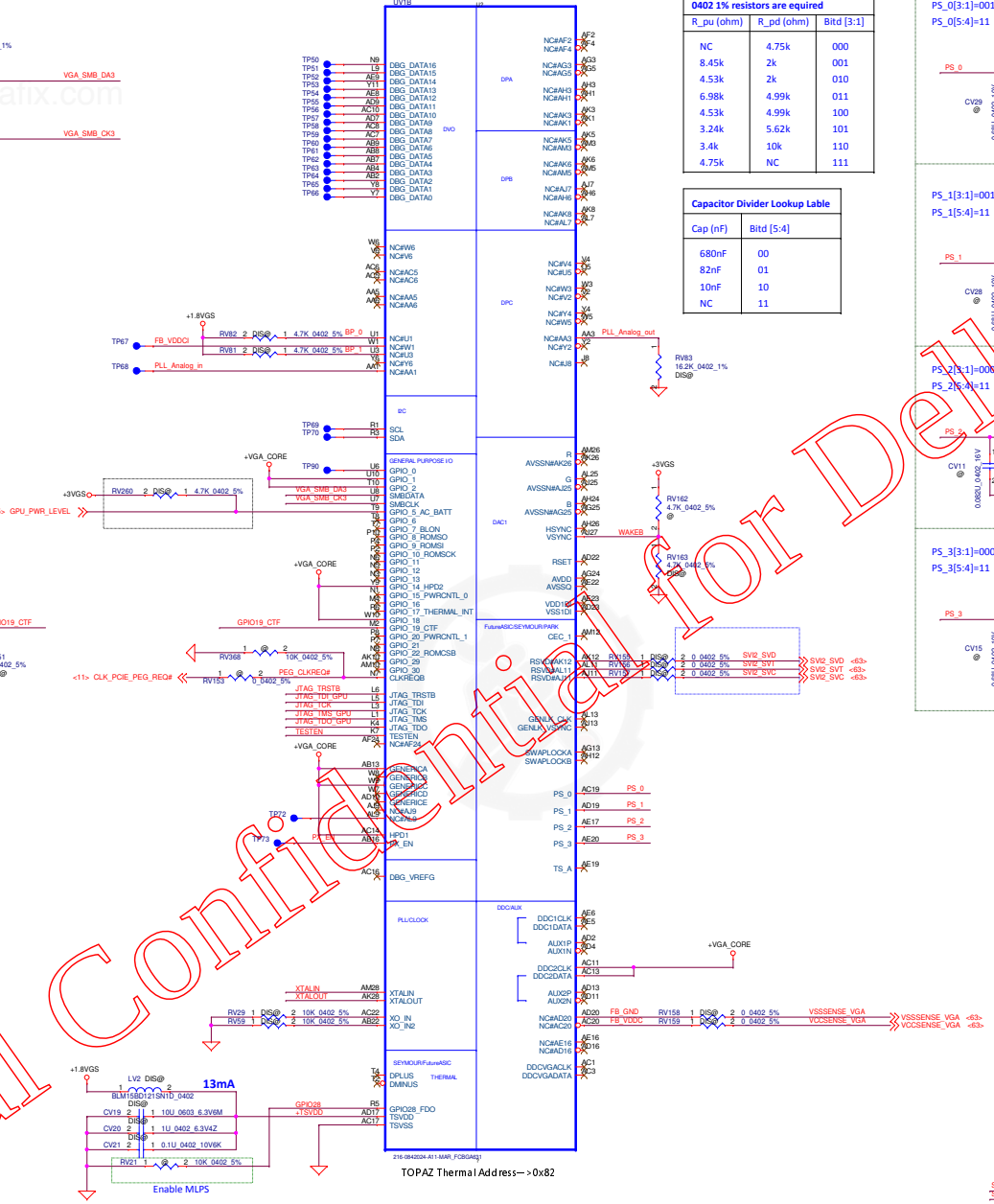
Main Func = GPU



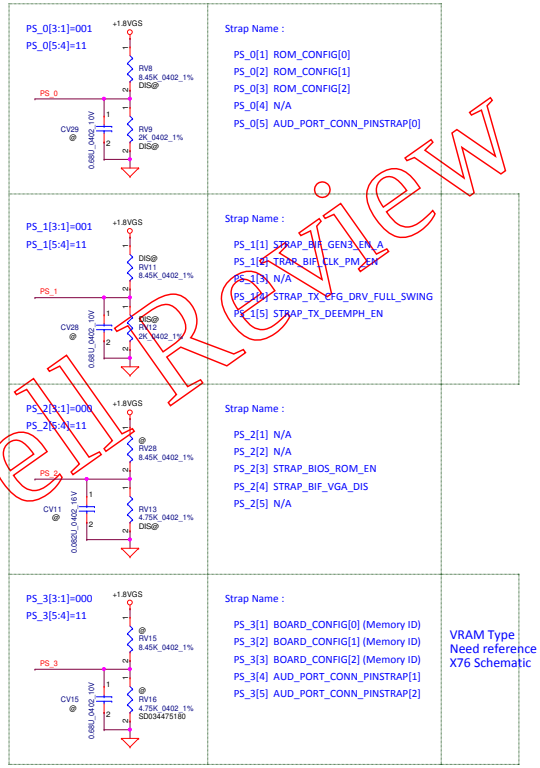


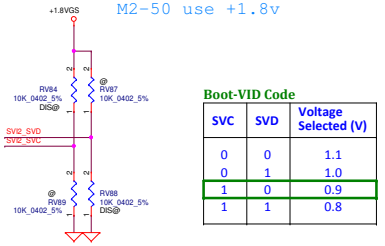




Resistor Divider Lookup Lable		
0402 1% resistors are equired		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Lable	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11





Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

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Title	MESO_(2/5)_MSIC
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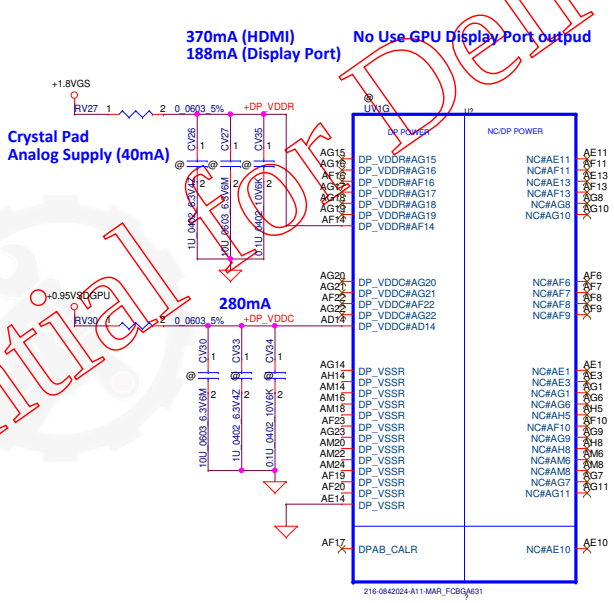
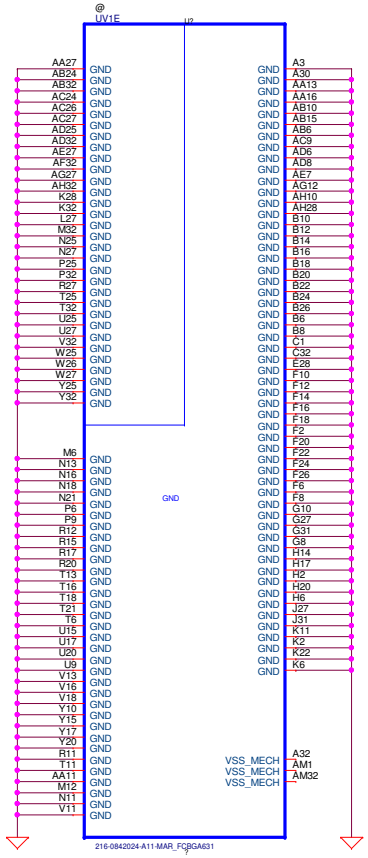
Main Func = GPU





Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MESO_(3/5)_Power/GND

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Main Func = GPU

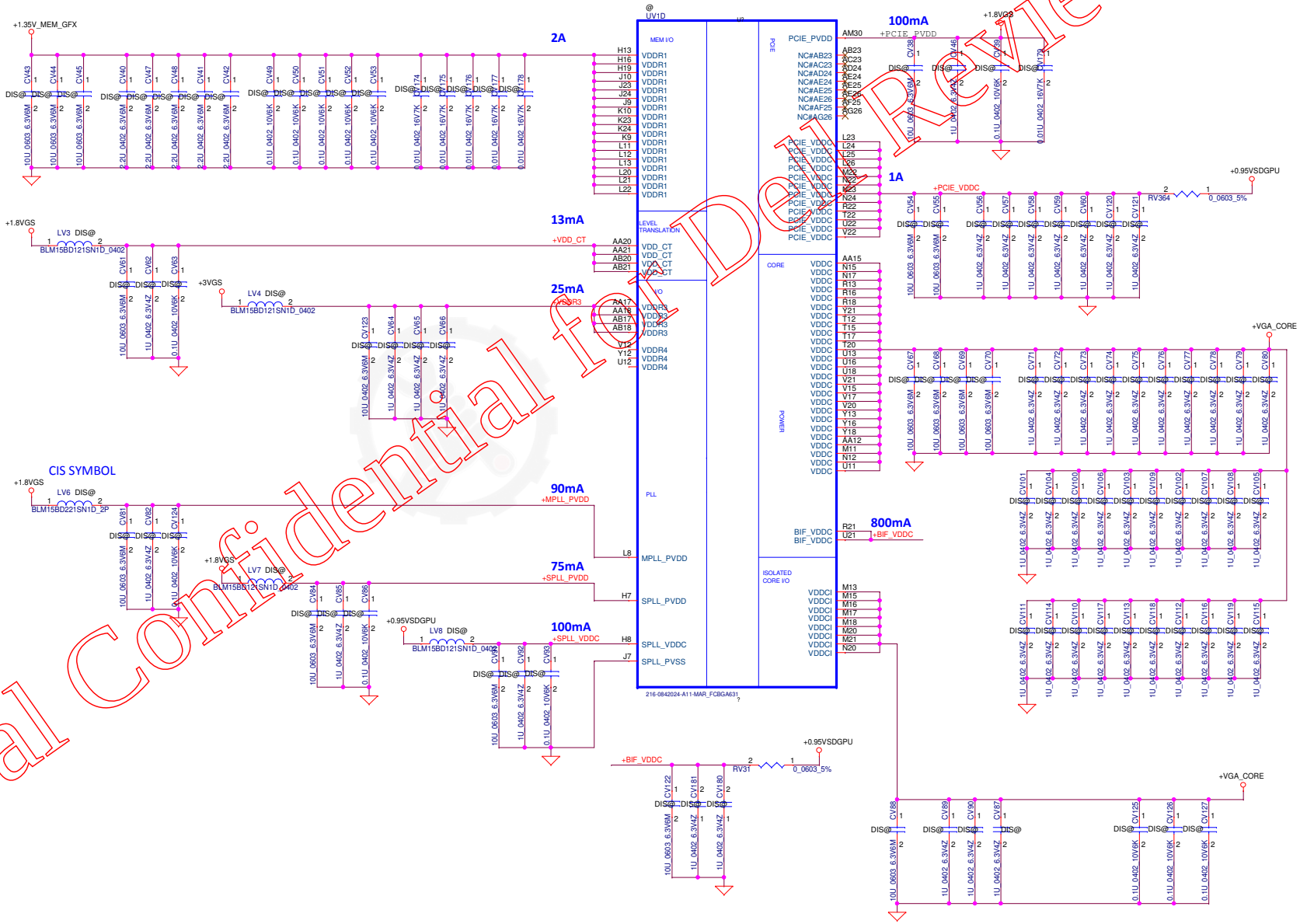
+VGA_CORE	10uF	1uF	0.1uF
VDDC	4	30	0
VDDCI	1	3	3

+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC	2	7	0
BIF_VDDC	1	2	0
SPLL_VDDC	1	1	1
+DP_VDDC	0	0	0

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1	3	5	5	5

+1.8VGS	10uF	1uF	0.1uF
PCIE_PVDD	1	1	1
MPLL_PVDD	1	1	1
SPLL_PVDD	1	1	1
VDDR4 (NC)	0	0	0
VDD_CT	1	1	1
+TSVDD	1	1	1
+DP_VDDR	0	0	0

+3VGS	10uF	1uF	0.1uF
VDDR3	1	3	0



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MESO_(4/5)_Power

Size	Document Number	Rev
Custom	LA-F115P	0.1

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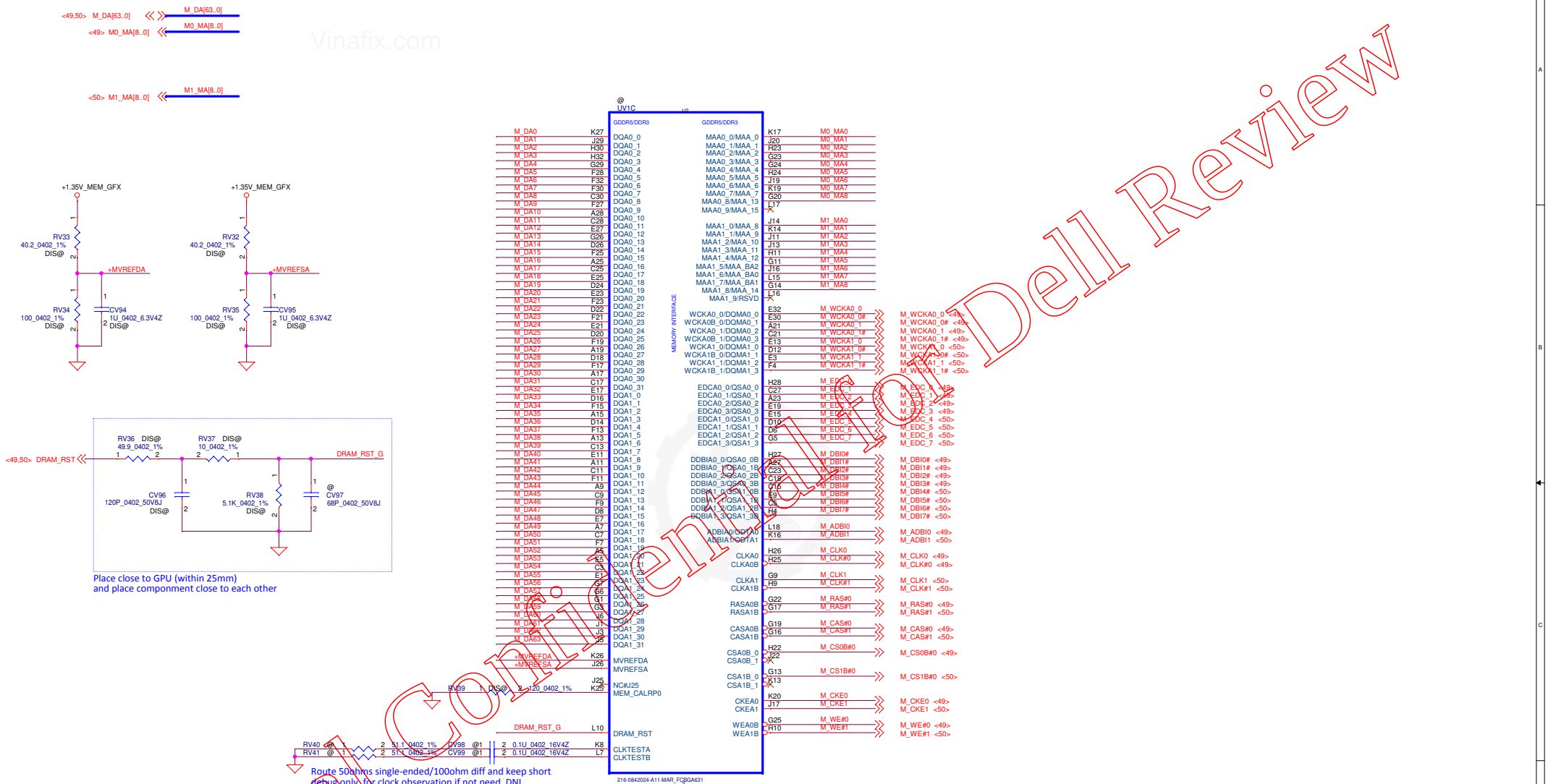
Main Func = GPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **MESO_(5/5)_MEM**

Size	Document Number	Rev
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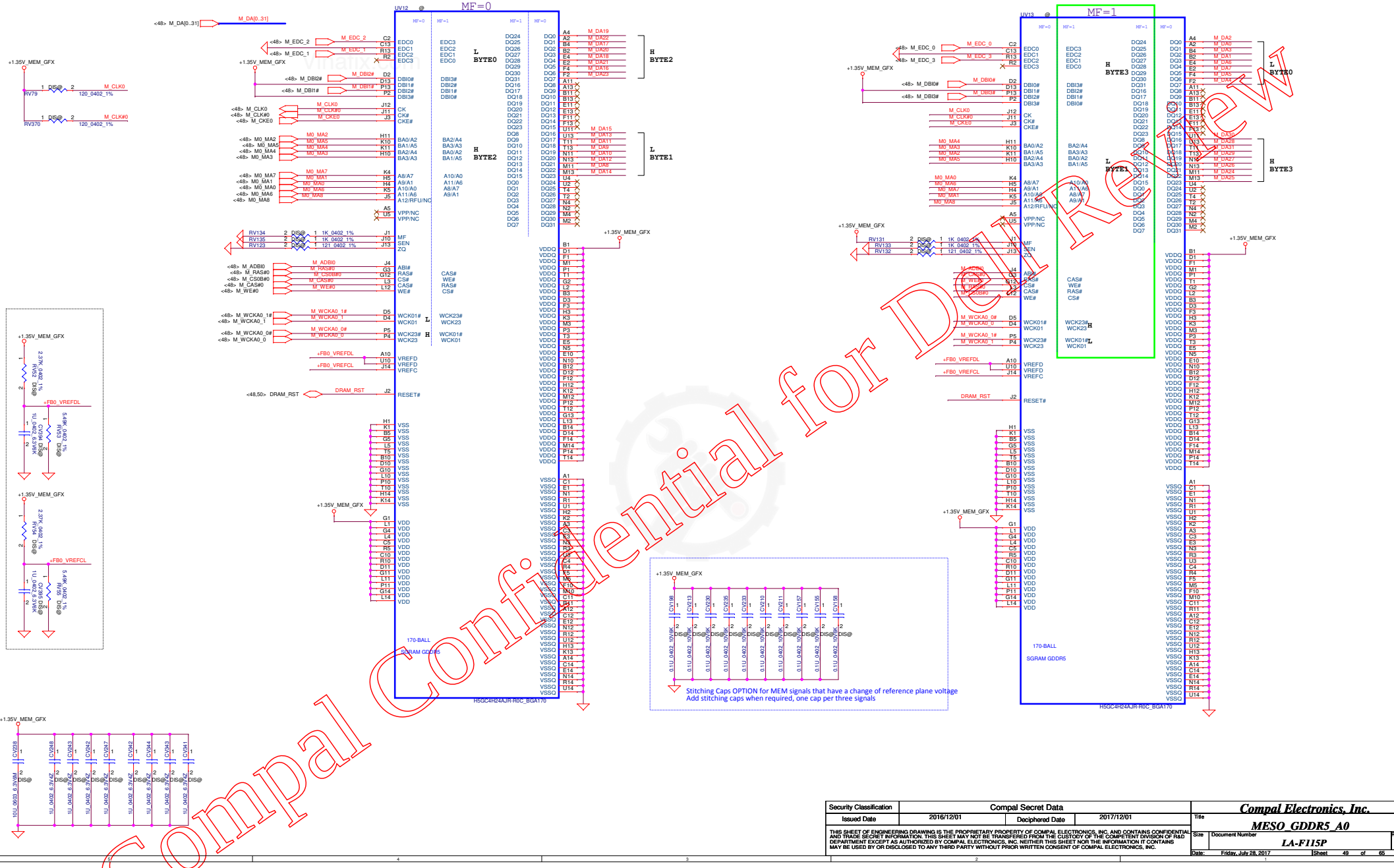
Main Func = GDDR5



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Issued Date	2016/12/01	Deciphered Date	2017/12/01

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Compal Electronics, Inc.	
Title	MESO_GDDR5_A0
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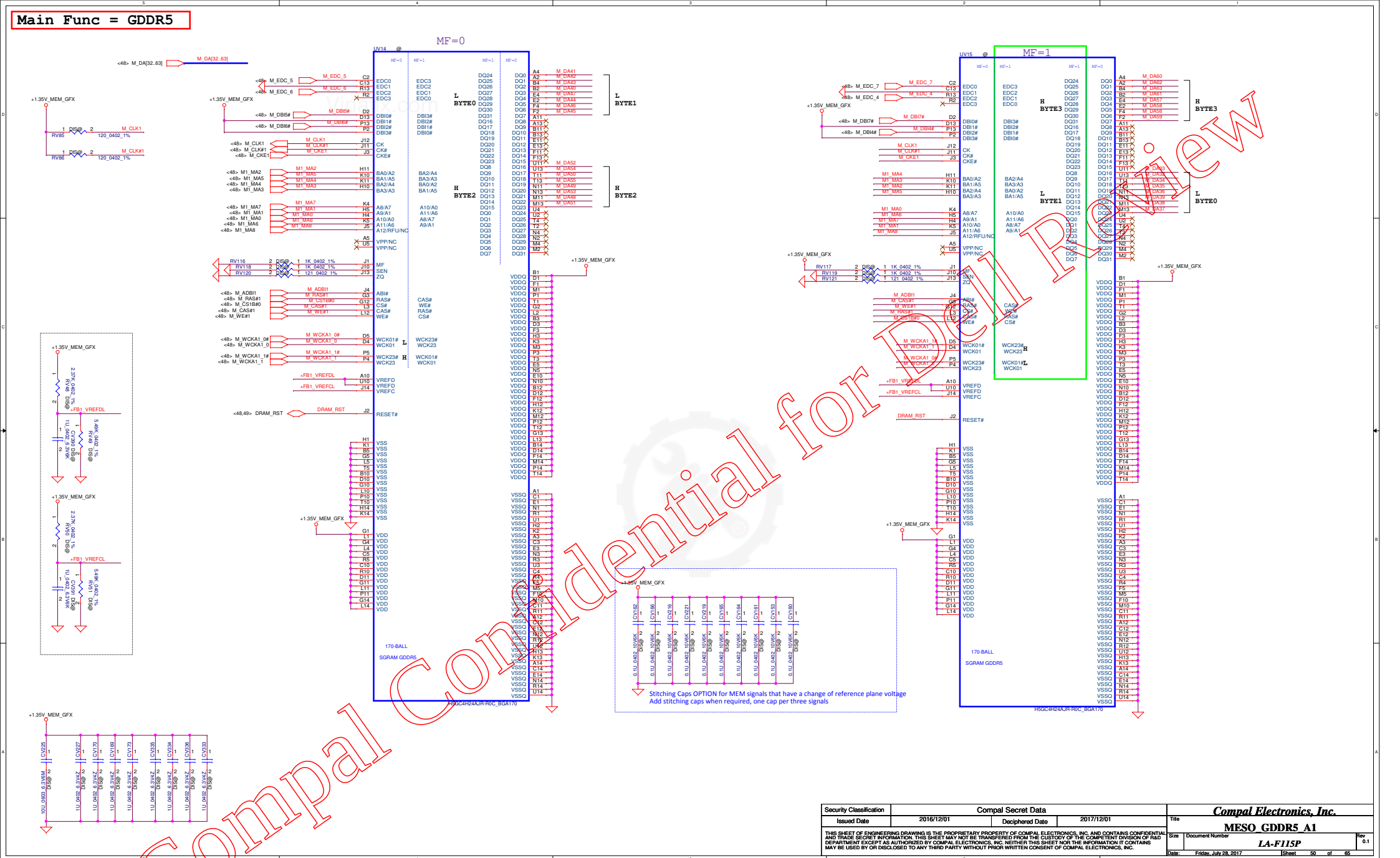
Main Func = GDDR5



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Compal Electronics, Inc.			
Title	MESO_GDDR5_A1		
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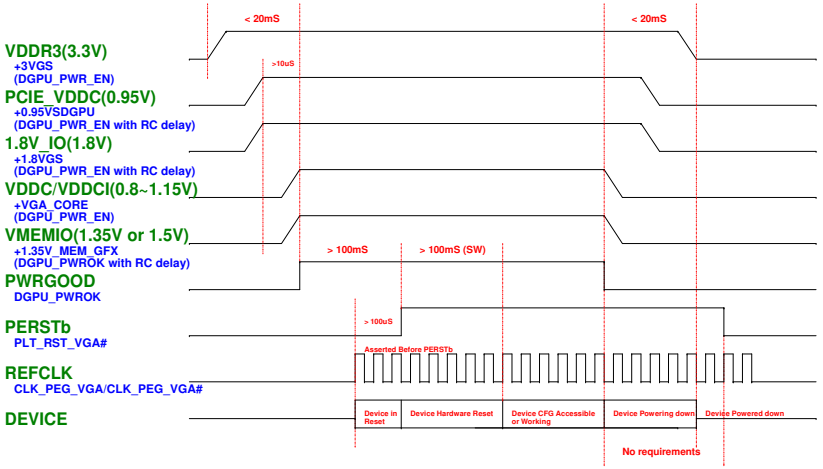
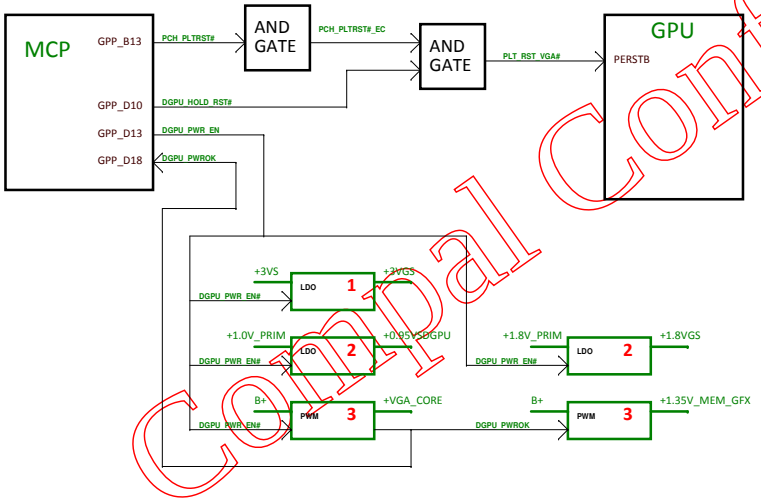
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/µs).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.





samsung 4G

UV12	SA000092D1L S4G_R3@ S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	UV14	SA000092D1L S4G_R3@ S IC D5 256M32 K4G80325FB-HC28 FBGA A31!
UV13	SA000092D1L S4G_R3@ S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	UV15	SA000092D1L S4G_R3@ S IC D5 256M32 K4G80325FB-HC28 FBGA A31!

samsung 2G

UV12	SA00009TT1L S2G_R3@ S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	UV14	SA00009TT1L S2G_R3@ S IC D5 128M32 K4G41325FE-HC28 FBGA A31!
UV13	SA00009TT1L S2G_R3@ S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	UV15	SA00009TT1L S2G_R3@ S IC D5 128M32 K4G41325FE-HC28 FBGA A31!

Hynix 4G

UV12	SA00009U11L H4G_R3@ S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	UV14	SA00009U11L H4G_R3@ S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!
UV13	SA00009U11L H4G_R3@ S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	UV15	SA00009U11L H4G_R3@ S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!

Hynix 2G

UV12	SA00008HQ1L H2G_R3@ S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	UV14	SA00008HQ1L H2G_R3@ S IC D5 128M32/3G H5GC4H24AJR-R0C A31!
UV13	SA00008HQ1L H2G_R3@ S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	UV15	SA00008HQ1L H2G_R3@ S IC D5 128M32/3G H5GC4H24AJR-R0C A31!

Micron 4G

UV12	SA00009TV1L M4G_R3@ S IC D5 256M32 MT51J256M32HF-70:A A31!	UV14	SA00009TV1L M4G_R3@ S IC D5 256M32 MT51J256M32HF-70:A A31!
UV13	SA00009TV1L M4G_R3@ S IC D5 256M32 MT51J256M32HF-70:A A31!	UV15	SA00009TV1L M4G_R3@ S IC D5 256M32 MT51J256M32HF-70:A A31!

Micron 2G

UV12	SA00009E31L M2G_R3@ S IC D5 128M32 EDW4032BABG-70-F-R A31!	UV14	SA00009E31L M2G_R3@ S IC D5 128M32 EDW4032BABG-70-F-R A31!
UV13	SA00009E31L M2G_R3@ S IC D5 128M32 EDW4032BABG-70-F-R A31!	UV15	SA00009E31L M2G_R3@ S IC D5 128M32 EDW4032BABG-70-F-R A31!

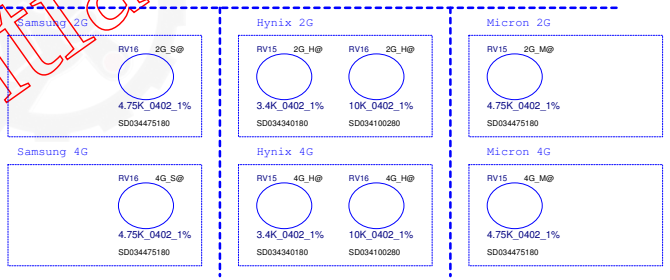


Table 3–21 Resistor Divider Lookup T

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R17M-M2-50 VRAM Only

Memory ID	4Gb R3 P/N	Vendor	Configuration	Size
000	SA00009TT1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BABG-70-F-R A31!	2GB

Memory ID	8Gb R3 P/N	Vendor	Configuration	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	4GB
110	SA00009U11L	Hynix	S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	4GB
111	SA00009TV1L	Micron	S IC D5 256M32 MT51J256M32HF-70:A A31!	4GB

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

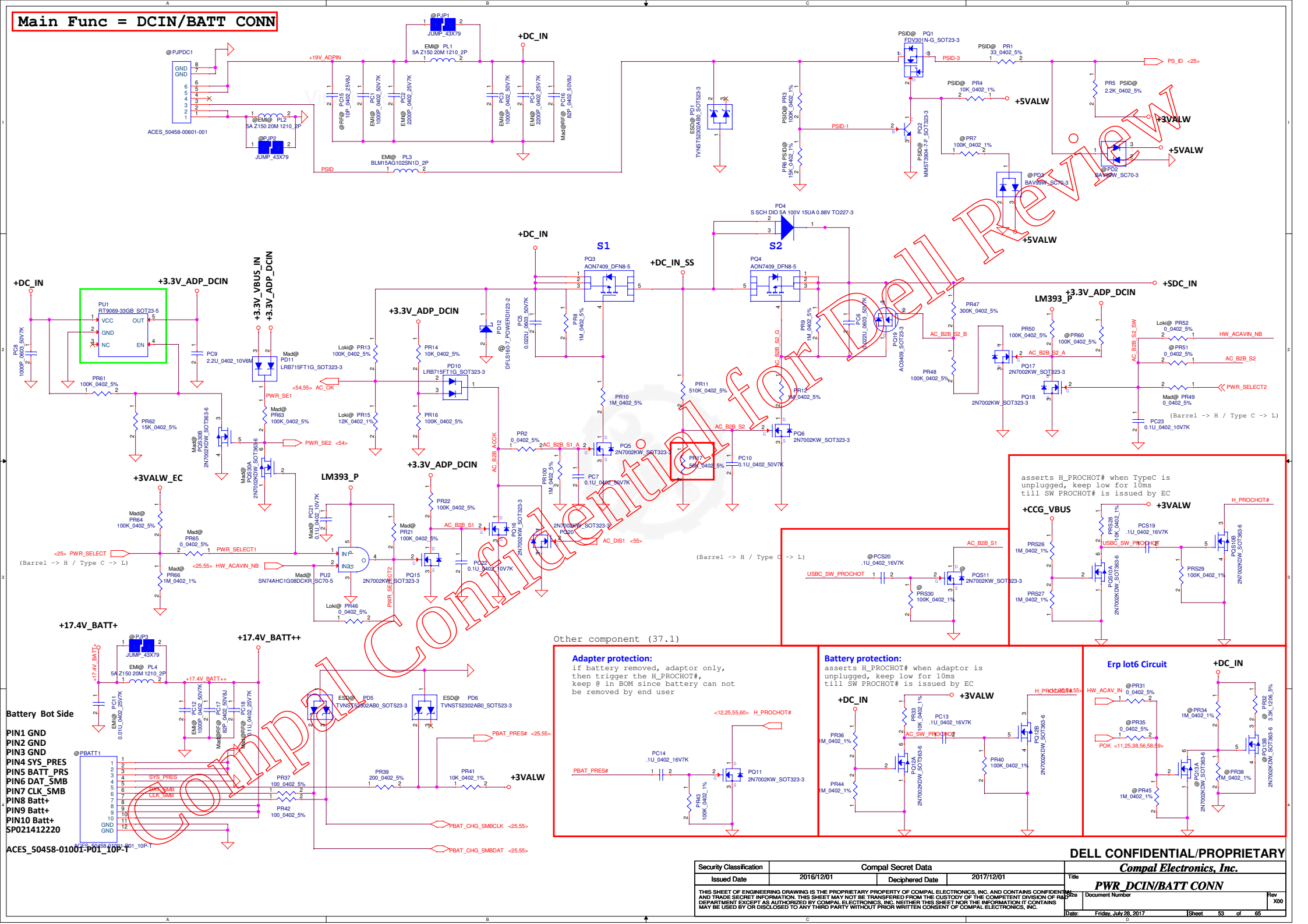
Compal Electronics, Inc.			
Title	MESO_Note		
Size	Document Number		Rev
	LA-F115P		0.1
Date:	Friday, July 28, 2017	Sheet	51 of 65

Version Change List (P. I. R. List)

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.		
Title: EE Change list		
Size	Document Number: LA-F115P	Rev: 0.1
Date: Friday, July 28, 2017	Sheet 52 of 85	

Main Func = DCIN/BATT CONN



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: PWR_DCIN/BATT CONN			
Size	Document Number		Rev X00
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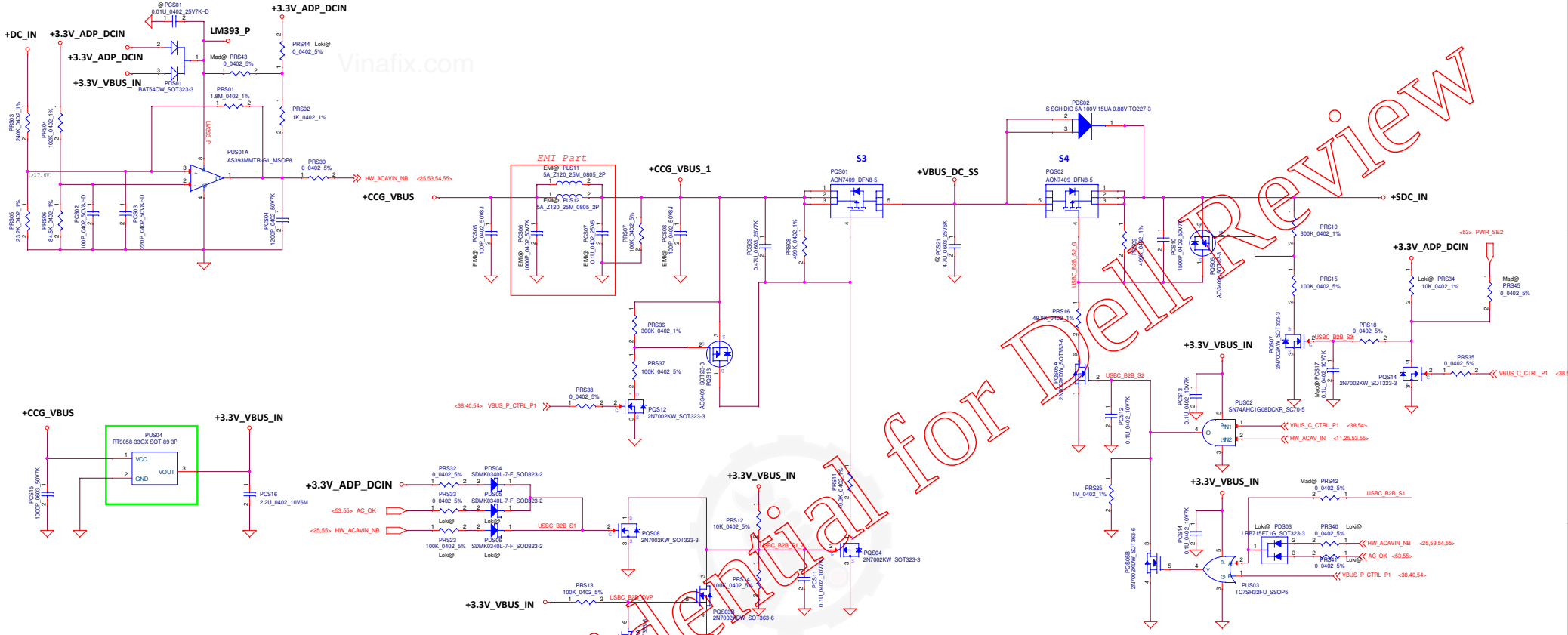
Main Func = Type-C PD Selector

DCIN_AC_Detector



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Issued Date	2016/12/01	Deciphered Date 2017/12/01	Title: PWR_Type-C PD Selector
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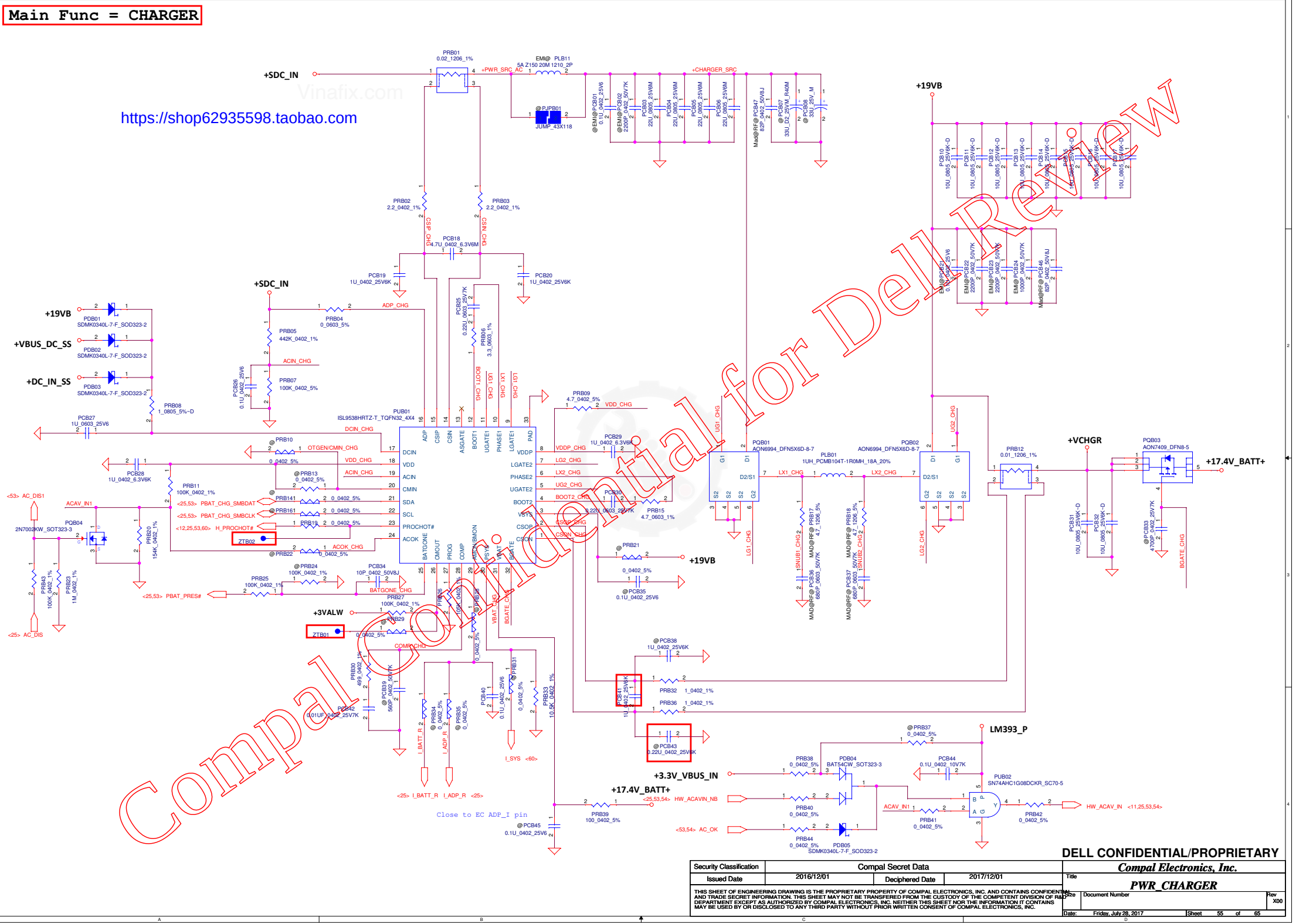
			Date: Friday, July 28, 2017 Sheet 54 of 65

Main Func = CHARGER



Security Classification	Compal Secret Data		
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DELL CONFIDENTIAL/PROPRIETARY

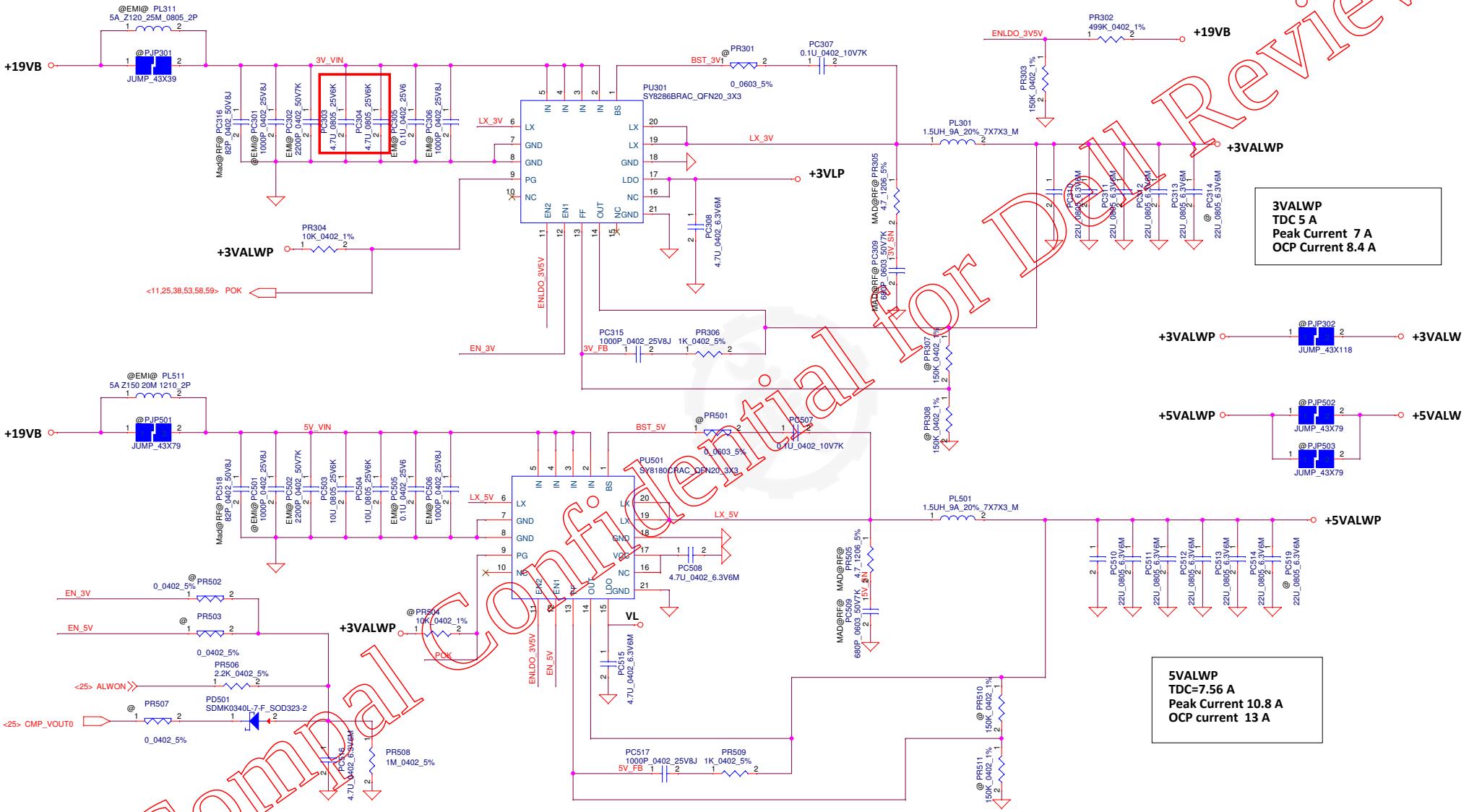
Compal Electronics, Inc.

Title: PWR_CHARGER

Size | Document Number | Rev X00

Date: Friday, July 28, 2017 | Sheet 55 of 65

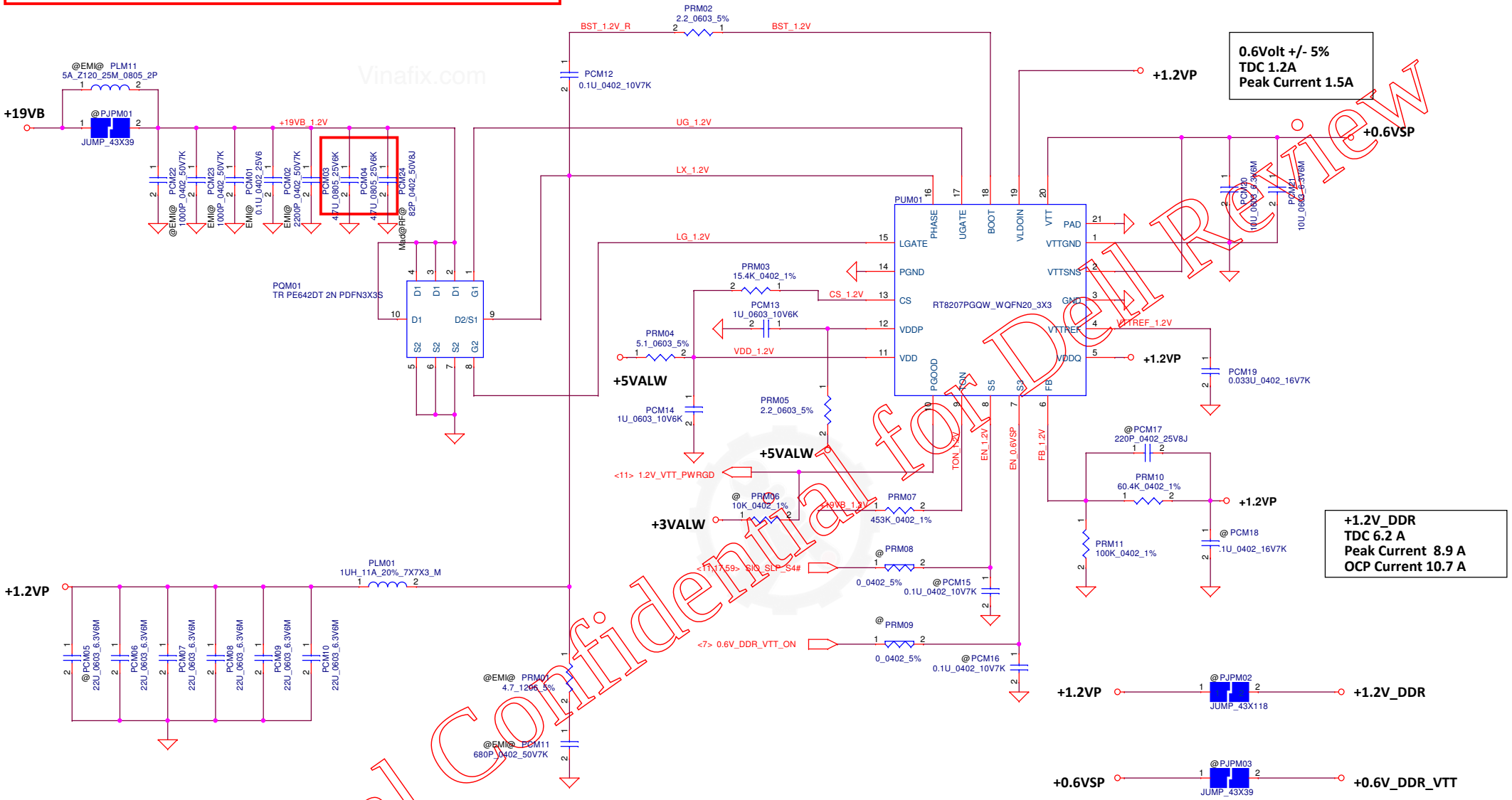
Main Func = 3.3VALWP/5VALWP



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	PWR_3.3VALWP/5VALWP		
Document Number			Rev 0.1 (X00)
Date: Friday, July 28, 2017	Sheet 56 of 65		

Main Func = +1.2V_DDR/+0.6V_DDR_VTT



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

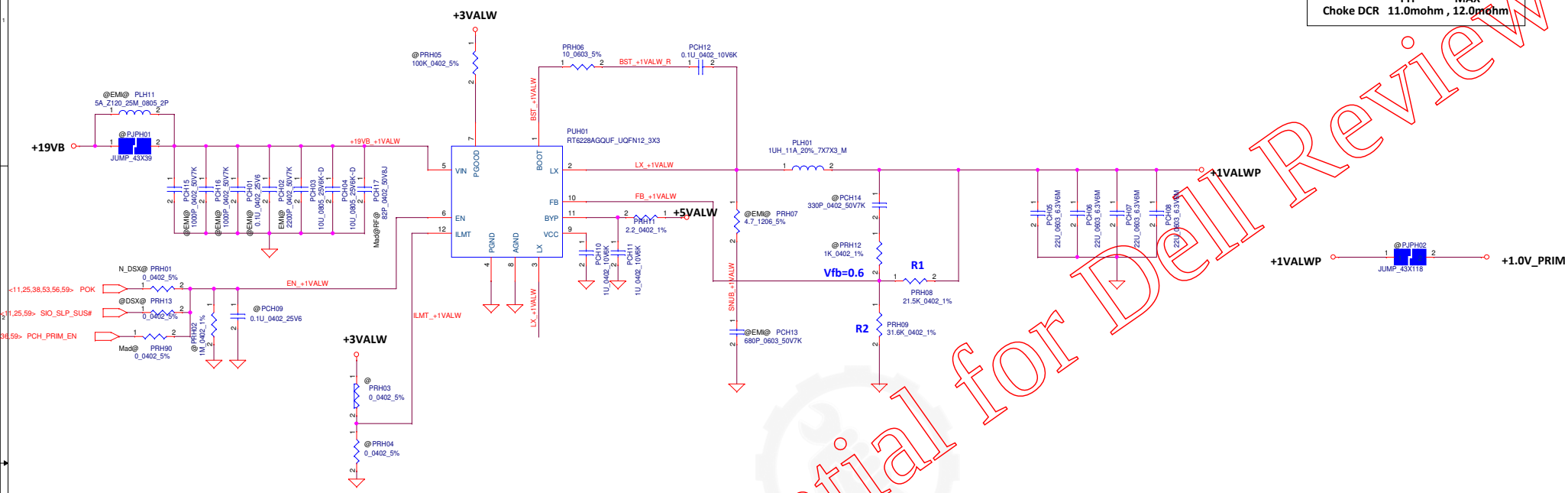
Title: PWR_+1.2V_MEN/+0.6V_DDR_VTT

Size	Document Number	Rev
Custom		X00

Date: Friday, July 28, 2017 | Sheet 57 of 65

Main Func = +1VALWP

+1.0V_PRIM
TDC 7.6 A
Peak Current 10.8 A
OCP Current 12 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: PWR_+1VALWP

Size	Document Number	Rev
C		X00

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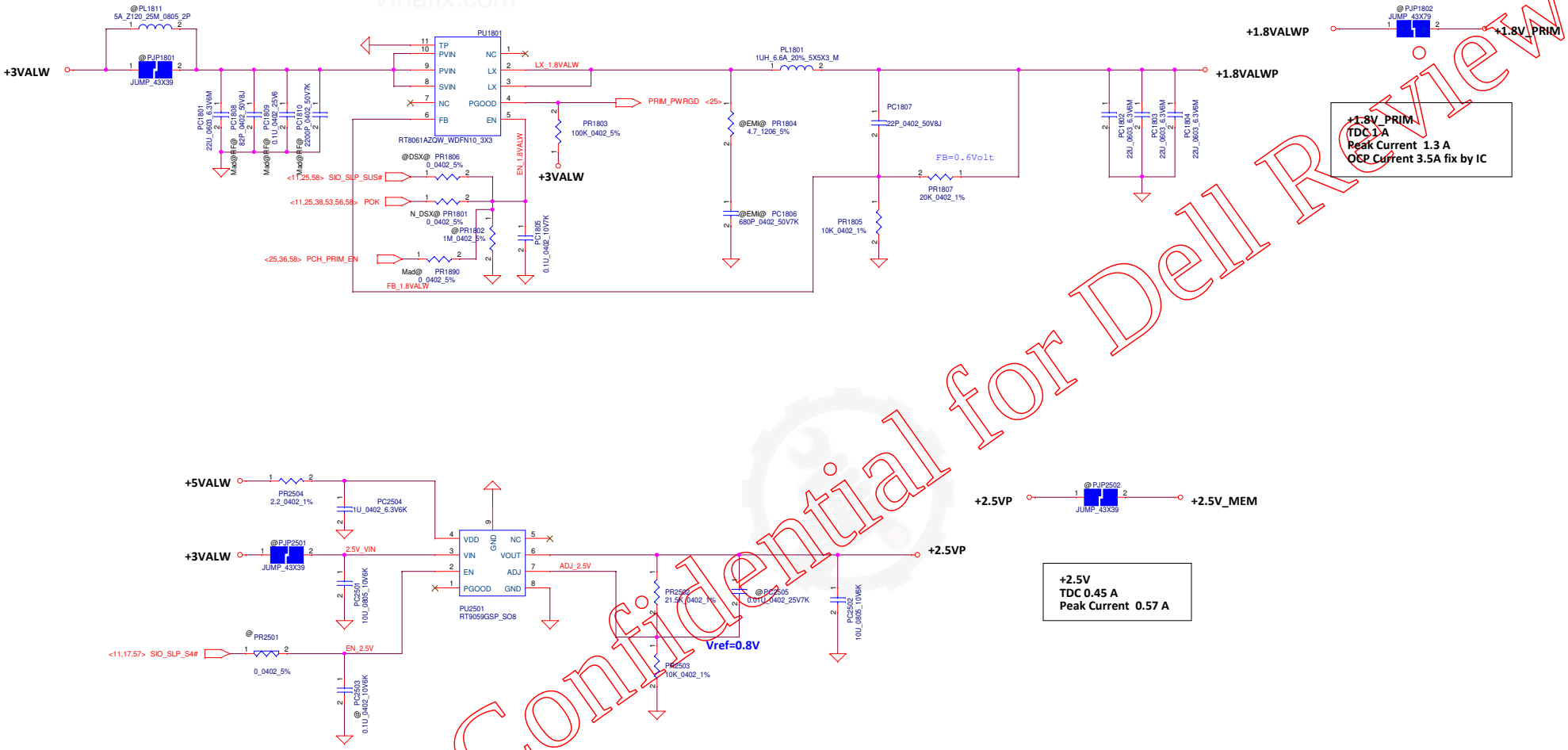
Main Func = +1.8VALWP / +2.5VP



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	PWR_+1.8VALWP / +2.5VP		
Size C	Document Number		Rev X00
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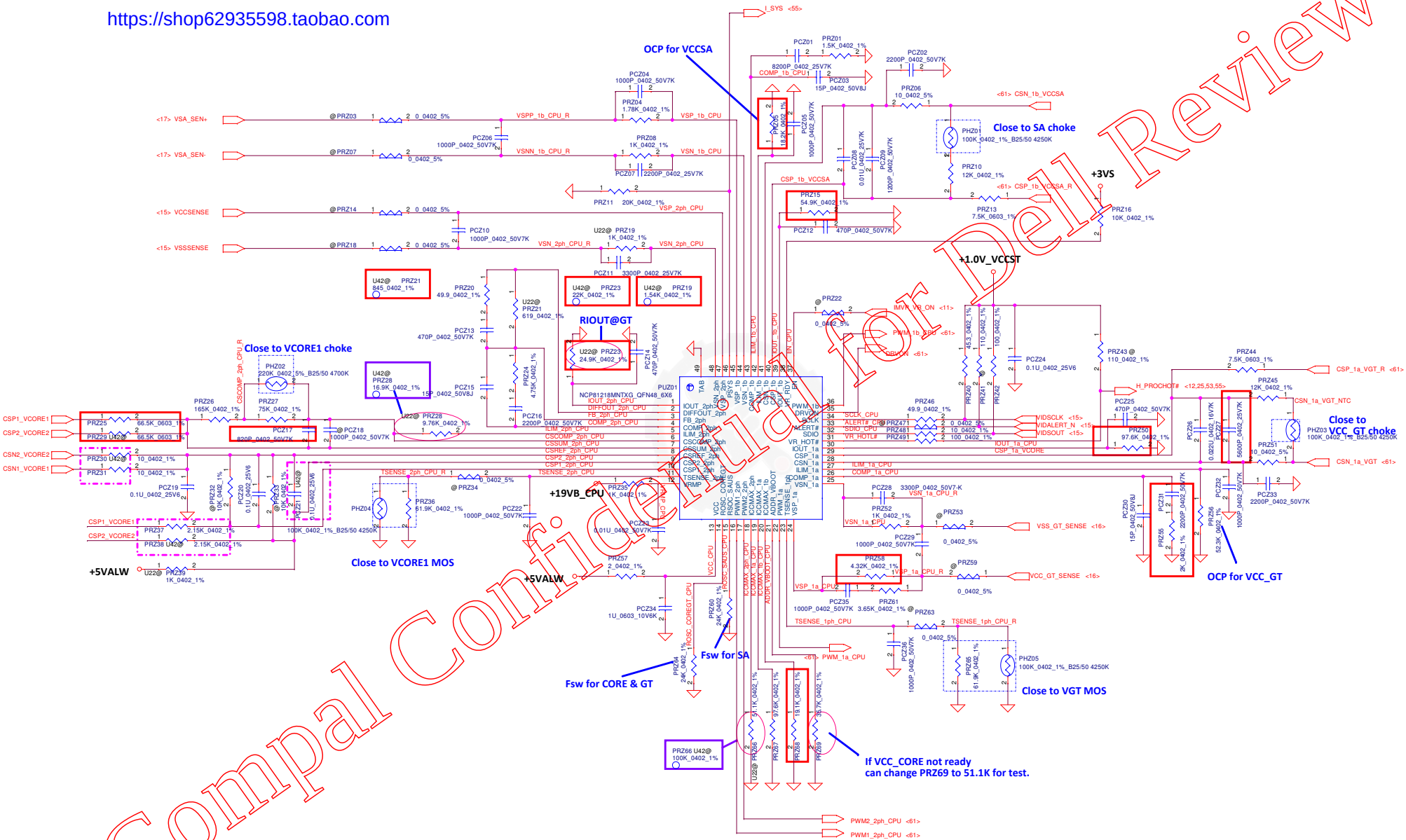
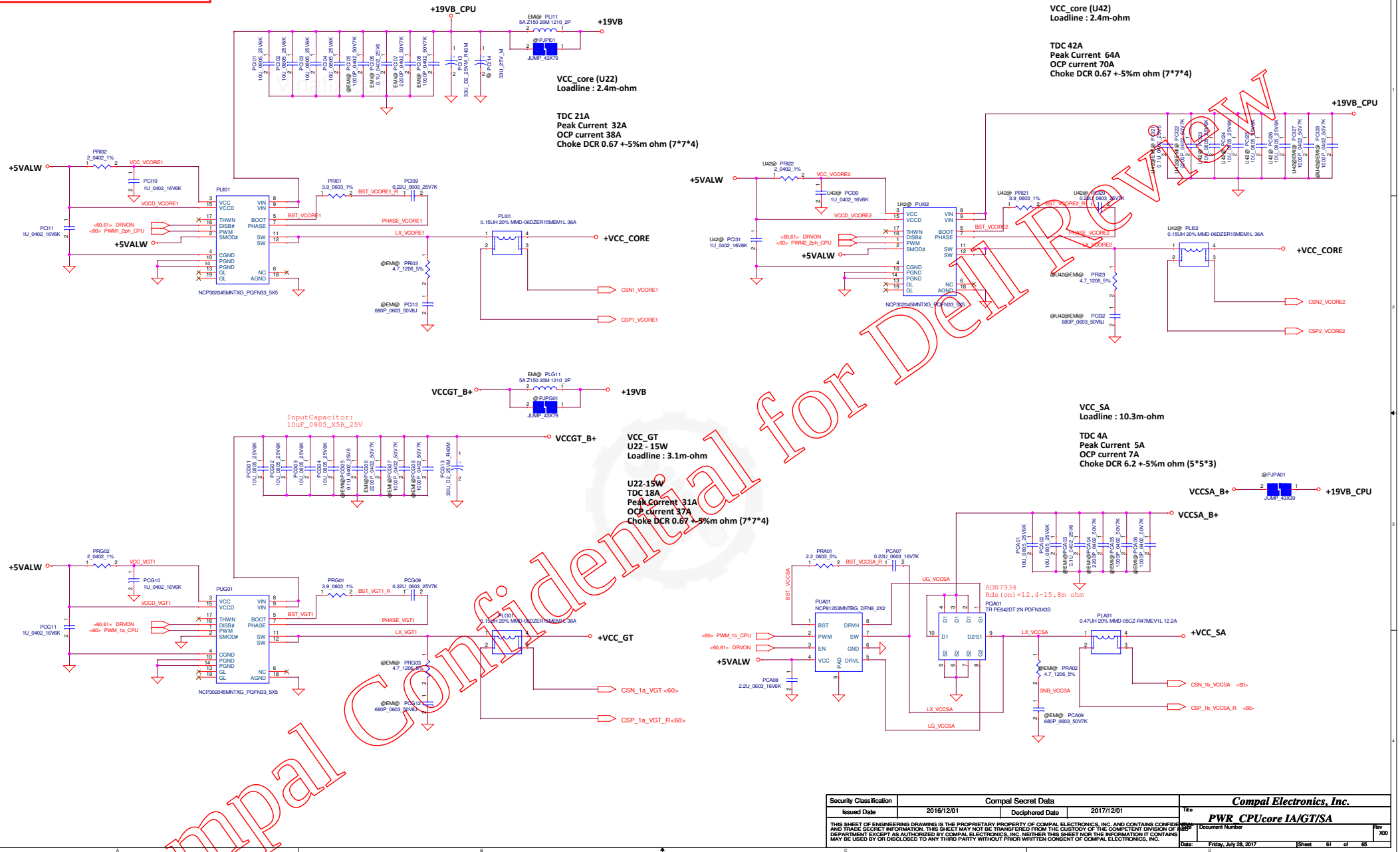
Main Func = CPU



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date 2017/12/01	Title: PWR_CPU
Size	Document Number		Rev: X00
Date: Friday, July 28, 2017	Sheet 60 of 65		

Main Func = CPUcore IA/GT/SA



Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Title	PWR_CPUcore IA/GT/SA		
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Main Func = CPU/ VGA / SA MLCC

Total VCORE Output Capacitor:
3 X 330uF_D2==>U42
2 X 220uF_D2==>U22
32 X 22uF_0603==>U42
20 X 22uF_0603==>U22
30 X 1uF_0201==>U42
35 X 1uF_0201==>U22

Total VCCGT Output Capacitor:
1 X 220uF_D2
35X 22uF_0603_X5R==>U22
33X 22uF_0603_X5R==>U42
4X0.47uF_0201
9X 1uF_0201

Total VCCSA Output Capacitor:
7 X 22uF_0603
7 X 1uF_0201

+VCC_CORE
+VCC_GT
+VCC_SA
+VCC_CORE_42
+VCC_GT_42
+VGA_CORE

For VGACORE

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **PWR_CPU / VGA / SA MLCC**

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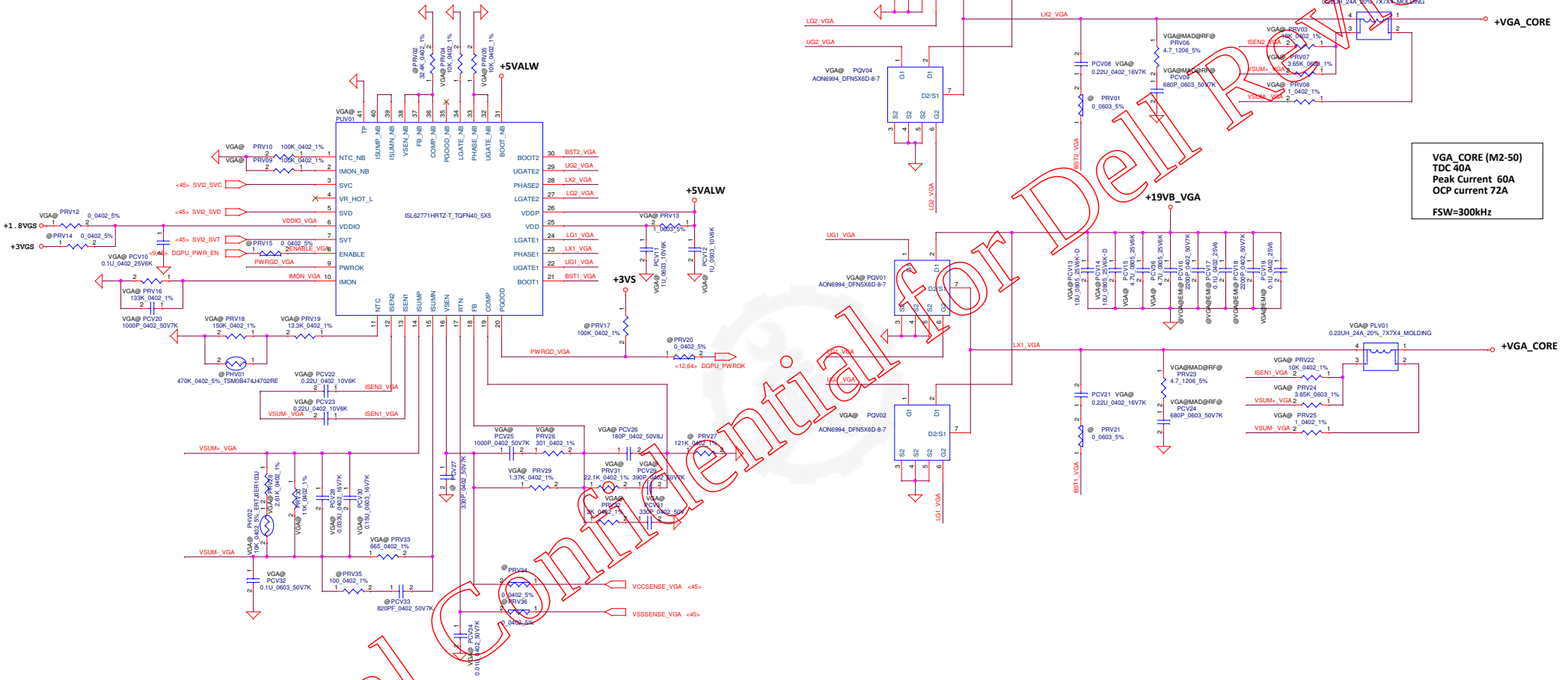
Main Func = VGA CORE



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.	
Title	PWR_VGA_CORE
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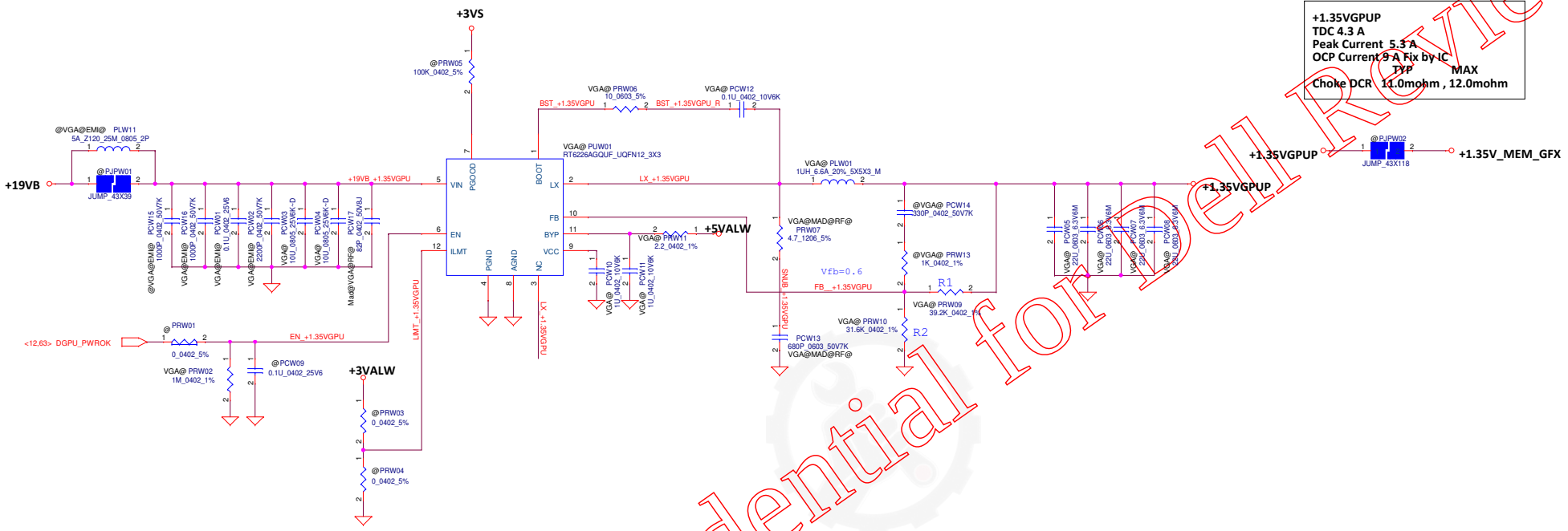
Main Func = +1.35VGPUP



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	PWR_+1.35VGPUP		
Size	Document Number		Rev X00
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P51	PWR	20160321	COMPAL			0.1(X00)
2	P56	PWR	20160321	COMPAL			0.1(X00)
3							
4							
5							
6							
7							
8							

Security Classification	Compal Secret Data		
Issued Date	2015/12/22	Deciphered Date	2017/01/31

Compal Electronics, Inc.			
Title	Changed-List PWR History		
Size	Document Number		Rev X00
Date:	Friday, July 28, 2017	Sheet	65 of 65