Introducing 2-nm/20Å Nano-Sheet FET technology with Buried Power Rails and nano Through-Silicon-Vias in Microwind

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Abstract: This paper describes the implementation of the novel Nano-sheet FET (NS-FET) for the 2-nm/20Å technology node in Microwind. After a general presentation of the electronic market and the roadmap to the atomic scale, we present design rules and basic metrics for the 2-nm node. Concepts related to the design of NS-FET using novel buried power rails are also described. Lastly, we analyze the performance of a ring oscillator, basic cells, sequential cells, and a 6-transistor RAM memory.

Keywords: Nano-Sheet, NSFET, Buried Power Rails, BPR, Through-Silicon-Via, nTSV, 2-nm, 20A, Ring oscillator, interconnects, SRAM, logic gates

Introduction

The structural growth of the semiconductor industry can be attributed to the soaring demand for electronic equipment, ranging from smartphones & laptops to electric cars, renewable energy systems, high-end servers, and high-performance computing associated to Artificial Intelligence (AI). Giant IC foundries such as TSMC, Samsung and Intel have shown an outstanding ability to propose new technology nodes every two years (Table 1). This trend should slow down to three years for the upcoming 2 nm and 1.5 nm nodes.

Technology node	Year of introduction	Key innovations	Application note
180 nm	2000	Cu interconnect, MOS options, 6 metal layers	
130 nm	2002	Low-k dielectric, 8 metal layers	
90 nm	2003	SOI substrate	[Sicard2005]
65 nm	2004	Strain silicon	[Sicard2006]
45 nm	2008	2nd generation strain, 10 metal layers	[Sicard2008]
32 nm	2010	High-K metal gate	[Sicard2010]
20 nm	2013	Double patterning, 12 metal layers	[Sicard2014]
14 nm	2015	FinFET	[Sicard2017]
10 nm	2017	FinFET, double patterning	[Sicard2017]
7 nm	2019	FinFET, quadruple patterning	[Sicard2017]
5 nm	2020	FinFET enhancement, EUV	[Sicard&Trojman2021]
3 nm	2021	Nano-Sheet FET, EUV	[Sicard&Trojman2021b]
2 nm /20A	2024	Buried power rail, nano Through-Silicon-Via	This application note
1.5 nm /15A	2027	Complementary FET	
1 nm /10A	2030	Stacked Complementary FET	

Table 1: Most significant technology nodes introduced over the past 20 years and prospective vision for 2030.

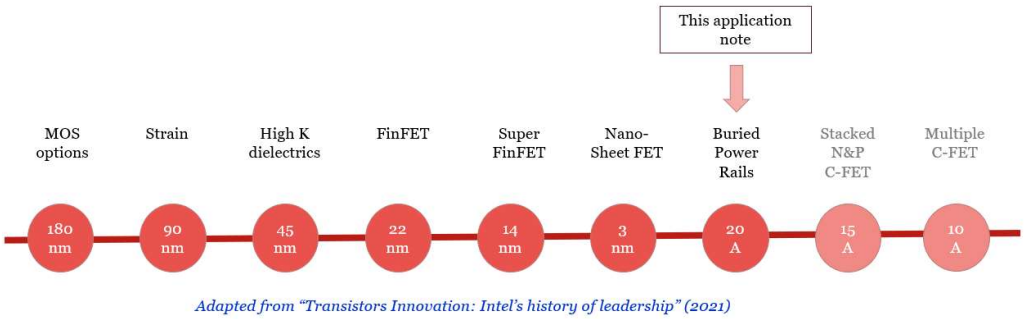


Figure 1: Technological innovation from 180 nm to 10Å technology, adapted from [Intel 2021].

Continuous advances in process fabrication are enabling a vision of future nodes such as 2 nm/20Å and 1.5 nm/15Å for the next decade, reinforced by prospective roadmaps from giant semiconductor foundries [Intel 2021][Anandtech 2022]. Through 10 application notes in open access on HAL [HAL 2022], we have tried to illustrate the increased performance of devices, specifically for the 14-nm and 7-nm nodes [Sicard 2017], and more recently the 5-nm & 3-nm nodes [Sicard & Trojman 2021] [Sicard & Trojman 2021b]. The key innovations of each technology node are summarized in Figure 1.

Three major silicon foundries, namely TSMC from Taiwan, Samsung from South-Korea and Intel from USA, are planning to introduce 2-nm/20A technologies in 2025. Samsung expects to have 2 nm chips based on gate-all-around (GAA) transistor architecture in mass production by 2025, and 1.4 nm process available as early as 2027 [Samsung 2021].

TSMC is expecting to start production of integrated circuits (ICs) using its 2 nm technology by the end of 2024, about three years after the introduction of its 3-nm technology. Chips fabricated using TSMC's 2 nm technology should be introduced in consumer devices around 2026 according to [Anandtech 2022]. Intel announced in 2021 that its 20Å process (Å for "Angstrom", 0.1 nm) would use its own version of nano-sheet FET named RibbonFET starting 2024 [Intel 2021].

In this application note, we describe the main characteristics of the 2-nm/20Å node by making use of available scientific literature and information released by semiconductor manufacturers, with focus on the Nano-Sheet FET, the buried power rails (BPR) and the Through-Silicon-Vias (TSV). We review the basic design rules, describe the transistor characteristics and the changes induced by buried power rail on the cell design. The implementation and performance of basic cells such as the inverter, the ring oscillator, the static RAM (SRAM) memory and basic logic circuits are presented. We conclude this document by discussing the switching performances of the node.

What the technology node represents

For more than 50 years, Moore's Law [Moore 2020] has described and predicted the shrinkage of transistors and the doubling of the number of transistors in the same silicon surface, roughly every two years. Until 1995, we used a simple rule that stated that the minimum feature size was equal to the node. For example, in 0.35-µm technology, the minimum reachable feature size by the process is around 0.35 µm. In Microwind, the "lambda" parameter used for designing cells was simply half of the minimum feature size. For decades, the minimum gate length was simply fixed to 2 λ. As shown in Figure 2, the gate length became even smaller than the technology node from 1995 to 2010.

Starting in 2010, the reduction of minimum feature size slowed down, and became more and more disconnected from the node name, mostly due to fundamental physical limitations linked to lithography. In nano-scale technology, we are facing a confusion between the "brands" (e.g. 7 nm, 5 nm, 3 nm and 2 nm nodes) and the physical reality of minimum dimensions, which are physically

limited to higher values, despite small lithography improvements. For example, in a 2-nm node, the minimum feature size is in the order of 10 nm, 5 times more than the “commercial” denomination of the node.

To solve this issue, the semiconductor industry decided to switch from "Planar" to "3D" architecture. As a result, the smallest feature size remains much larger than the brand name. As the distribution of the device onto the Si surface is no more planar, we get on an equivalent silicon surface a transistor density and an amount of current equivalent to the technology node.

For example, the 7-nm technology using FinFET devices has a minimum feature size larger than 7nm but in term of transistor integration, it offers the same performance as a 7nm gate length planar MOSFET on the same silicon area (Figure 4).

As the limits of lithography have been reached, progress has been made at the device level through the introduction of more efficient switches (FinFET, Nano-Sheet FET, Complementary FET) and at the design level with new strategies for supplying the cells by means of buried power rails, nano-through silicon vias and back-side power delivery.

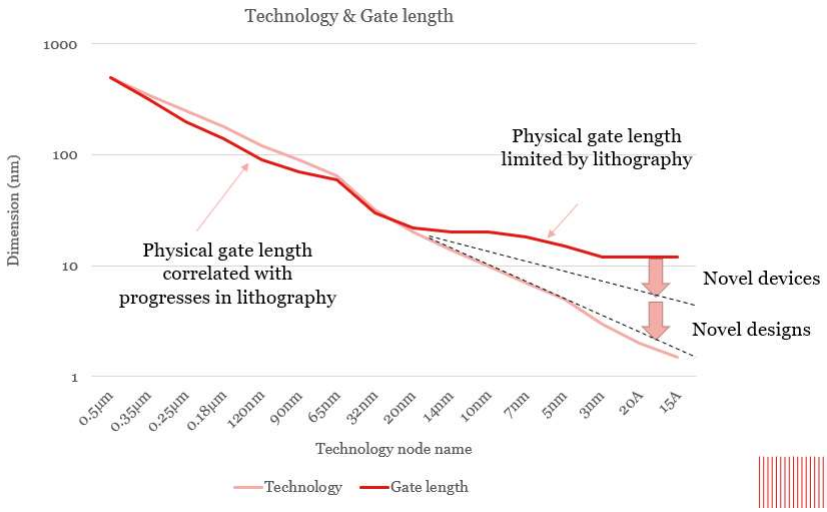


Figure 2: Link between technology nodes and device gate length: from 20 nm, the node name started being uncorrelated to the gate length. Adapted from [Moore 2020].

The Nano-Sheet era

The adoption of nano-sheet FET has followed the adoption of FinFET with a 10-year difference [Samsung 2021]. The 3-nm node has signaled the start of a migration process from FinFET to NSFET, so as to enable further gains in current drive while reducing the device surface, leading to smaller, faster and more energy-efficient chips (Figure 3). The 2-nm node should be using NSFET devices and introduce buried power rails (BPR). Three different categories of applications can be distinguished: high-performance (severs, data centers), general-purpose (laptops, gaming), and low-power computing (mobile, IoT) with significant differences in terms of acceptable leakage current (IOFF).

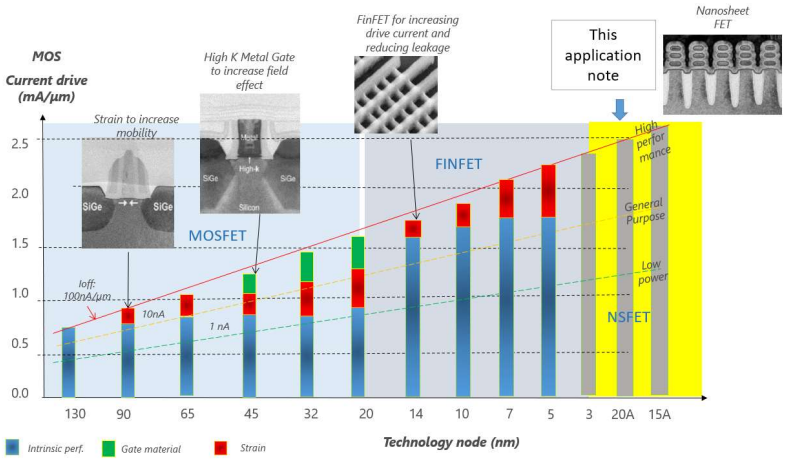


Figure 3: Increased current drive over 13 technology nodes including MosFET, FinFET & Nano-Sheet FET.

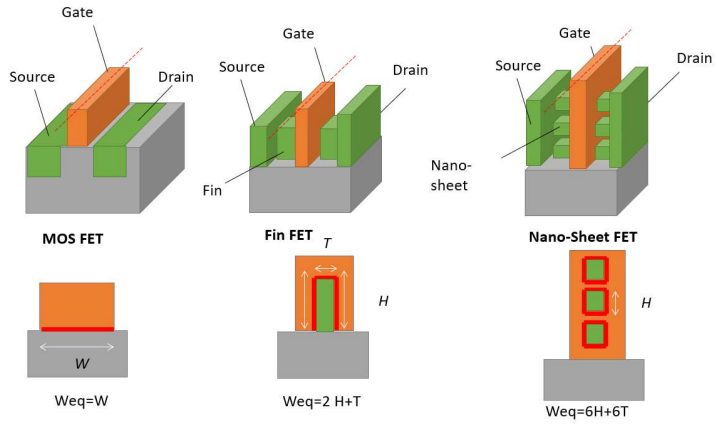


Figure 4: MosFET, FinFET & Nano-Sheet FET, with their corresponding equivalent channel width.

Within a reduced silicon surface, process engineers have been able to fabricate much more efficient devices than the original planar MosFET enabling to increase the device density. Stacking nano-sheets results in an equivalent channel width three times more area-efficient than for a planar MosFET, in its 3-stacked nano-sheet configuration. More details about the NSFET may be found in [Sicard & Trojman 2021b].

Parameter	*Code*	*[Choi 2020]*	*[Jeong 2020]*	*[Yoon 2022]*	*[Yang 2022]*	*[Mertens 2021]*	*Microwind*
Nano-Sheet thickness	TNS	5	5	5	5	5	5
Nano-Sheet Spacing	TSP	7.4	10	10	15	10	10
Number of Nano-Sheets	NS	4	3	2,3,4	3	4	3*

Table 2: Characteristics of NSFET extracted from a selection of publications; (*) in Microwind, the number of NS can be changed from 2 to 4.

We have fused key elements found in literature, without any knowledge of the process-design-kit (PDK) proposed by the foundries, due to severe non-disclosure agreements (NDA) restricting access to detailed technology specifications. The industrial process usually results from a careful approach

known as design technology co-optimization (DTCO), as well as a precise evaluation of power, performance area and cost (PPAC). In our implementation of the 2-nm technology in Microwind, we keep the same thickness (called TNS, TCH, or TSH depending on the authors) and spacing (TSP) as those of the 3-nm node [Sicard & Trojman 2021b] (Table 2).

Key metrics

We present in this section three key metrics: the gate pitch, the metal pitch, and the "track" design unit.

Gate pitch

The gate pitch, also called the Contacted-Gate-Pitch (CGP), refers to the minimum distance between active gates (vertical red lines in Fig. 5). In Microwind, you may generate vertical gates at regular CGP using the command `Edit > Generate > Tracks (MP) and Gates (CGP)`. Unselect metal tracks and click OK; four vertical gates will be drawn, with a CGP of 40 nm (10 λ). In Microwind, the gate pitch has remained constant at 40 nm in the 5, 3 and 2 nm nodes. Roadmaps such as described in [Ahmed 2020] indicate a slight reduction of this parameter (typically 48 nm down to 40 nm).

Figure 5: Generating gates with the 40 nm (10 λ) contacted gate pitch (CGP-4gates.MSK).

Metal pitch

Using the command `Edit > Generate > Tracks (MP) and Gates (CGP)`, we may select metal tracks that will be routed using the associated metal pitch, i.e. the sum of the minimum metal width (r501) and the metal 1 spacing (r502). In our implementation of the 2 nm in Microwind, the minimum metal width is 3 λ (12 nm) and the spacing is 2 λ (8 nm), which yields a metal pitch (MP) of 5 λ (20 nm), as illustrated in Figure 6. This value is smaller than those of the 5 and 3 nm nodes (3 + 3 λ, or 24 nm), accounting for the decrease of MP according to most roadmaps [Prasad 2019][Ahmed 2020] [Radosavljevic 2021].

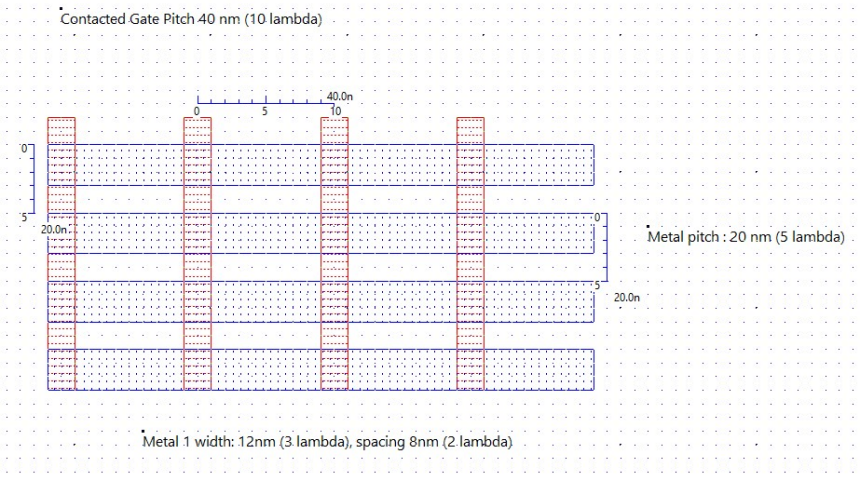


Figure 6: Generating gates with the 40-nm (10 λ) contacted gate pitch (cgp-mp-bpr-4x4.MSK).

T-Track unit

Most publications related to 2-nm design including buried power rails refer to the so-called 5T design (where T stands for "horizontal metal tracks"). The higher the number of T, the taller the cell. The value of T is the same as the metal pitch Metal Pitch (MP), i.e. around 20 nm in 2-nm technology (3 λ minimum metal width, 2 λ minimum spacing). The "T" concept is illustrated in Figure 7.

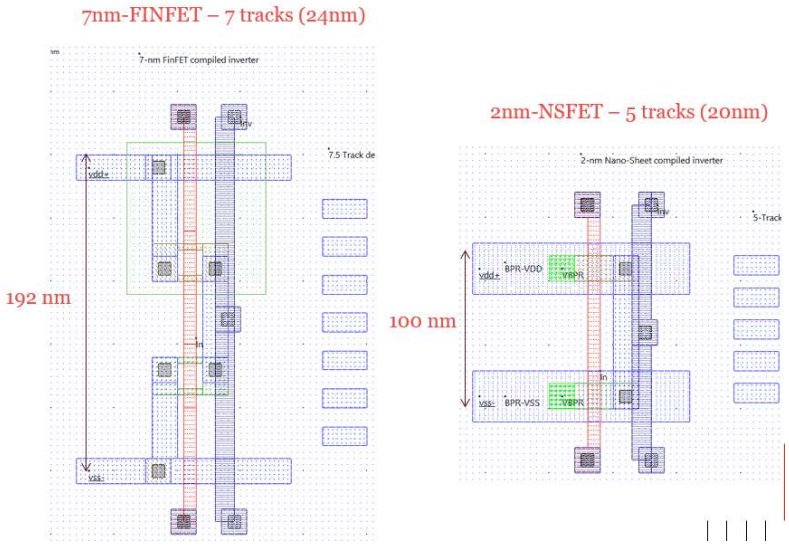


Figure 7: comparing the design of a 7-nm Inverter with 7 tracks, 192nm height and the 2-nm INV with 5T, 100 nm height (inv5Tracks vs inv7Tracks.MSK).

In 7-nm (Figure 7, left), the VDD and VSS tracks are routed horizontally in metal 1. The VSS is routed at the bottom, the VDD on top of the cell. The remaining routing area is between these two horizontal tracks. The metal pitch MP is 6 λ, that is 24 nm. In 2-nm (Figure 7, right), the VDD and VSS tracks are routed using the buried power rail, leaving more space for routing. The layout uses the 5-track design with a metal pitch MP, which is a little smaller (5 λ, 20 nm) due to a 2 λ spacing instead of the 3 λ in previous nodes. The cell height is nearly divided by 2 (100 nm instead of 192 nm), while the cell width remains comparable due to similar contacted gate pitch, which is consistent with Figure 2.

Voltage supply

We usually make a distinction between internal and external voltage supply. The internal supply (VDD) is the lowest and is mostly used for the core of the IC. The external supply (VDDH), around twice as high as the internal supply, is reserved for I/Os and specific analog or power devices.

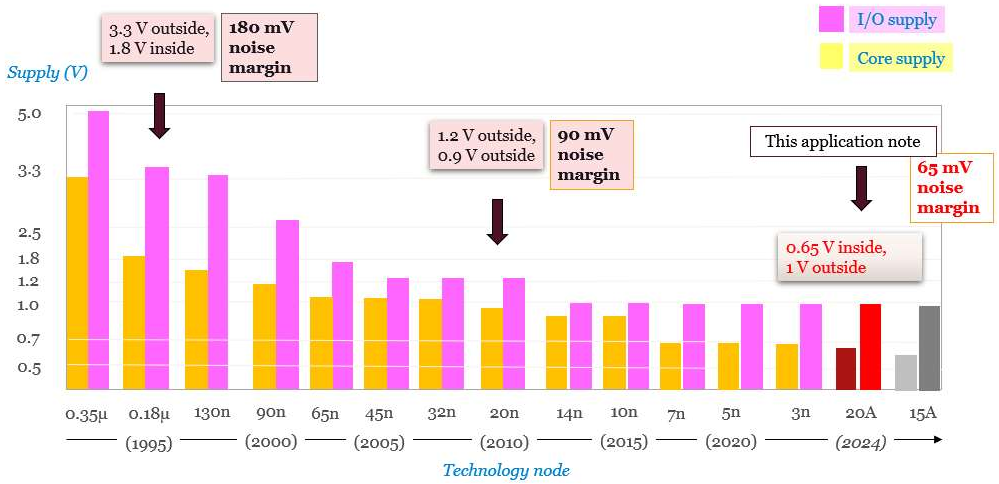


Figure 8: The reduction of the internal (VDD) and external supply voltages (VDDH) with the technology nodes. In nano-CMOS technologies, the most common value for VDD is around 0.65V.

Although a rapid decrease of the supply has been observed from 0.35 µm to 90 nm technologies, the reduction of VDD has considerably slowed down. An internal supply voltage around 0.6-0.7 V is considered to be the norm for most nano-scale technologies (Figure 8).

Most of the gates implemented in the IC are supplied at low voltage, around 0.65 V in the 5, 3 and 2 nm nodes, as shown in Figure 8. We usually consider 10% of VSS as the "noise margin" that can be tolerated for logic signals. For a 0.65 V supply, this means that 65 mV is the maximum acceptable amplitude for power and signal noise.

Introducing the buried power rail

For decades, the lowest part of the die (i.e. the substrate) has been virtually empty, serving as ground polarization for the safe operation of n-type & p-type devices. In order to supply ICs, we used to connect the uppermost layer of metal to solder balls which make the link to the package and then to the electronic board (Figure 9, left). The two last layers were usually dedicated to VDD (0.65 V) and VSS (0.0 V) for power grids, with thick and tall upper metal layers implemented as a grid to reduce resistive losses (Metal7 & Metal8 in Microwind) and limit voltage fluctuations during current switching.

These supplies are implemented through a complex stack of metal layers and vias between upper power grid and lower layers before they reach their target (the devices, situated above the substrate). This very complex and resistive path is far from being optimal [Cline 2021]. At the cell level, the VDD/VSS supply lines are routed using the lowest metal layer (called M1 in Microwind) which feature a very high serial resistance, in the order of 200-1KΩ/µm, depending on the width, thickness, and metallization material (Copper, Cobalt, Ruthenium) as discussed in [Chava 2018]. This supply strategy is called the "Front-Side" approach (Figure 9, left).

Buried power rails are one of the key scaling enablers beyond the 3 nm node [Gupta 2021]. This approach consists of burying the power rails into the substrate below the active devices. The BPR is part of the "Back-Side" supply strategy, with numerous advantages: it serves to reduce the cell size,

the VDD/VSS access resistance, and the supply noise, while increasing the switching speed and enhancing the memory performance.

Reorienting the supply to the back side of the substrate instead of the front side is a major challenge for the IC industry [Prasad 2019]. The new design constraints of BPR entail the re-design and restructuring of all basic cells.

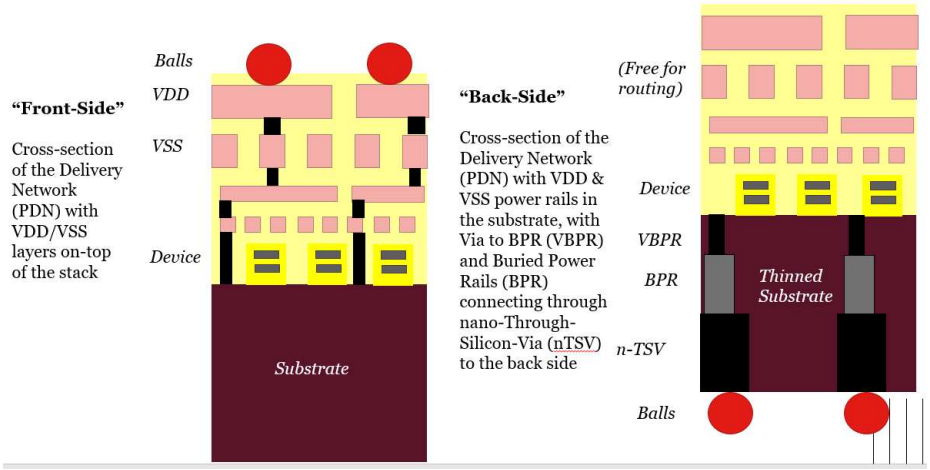


Figure 9: Front-side approach (left) vs back-side approach (right). Buried power rails are used to supply the devices from the back-side of the IC starting 2nm/20Å node.

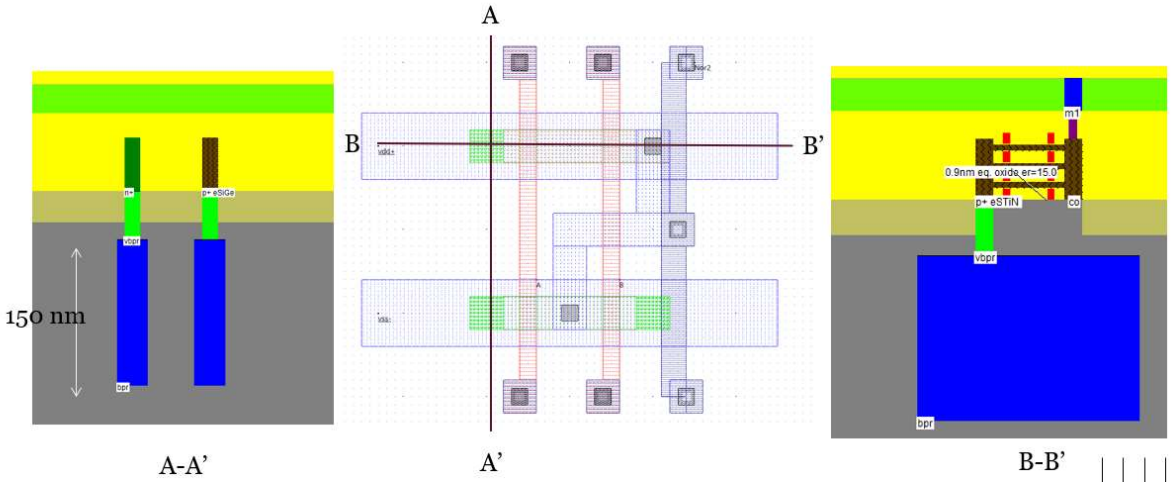


Figure 10: Implementation of the via-to-BPR and BPR in Microwind (Technology cmos20a.rul).

Thinned substrate, nano-Through-Silicon-Vias (nTSV) and specific back-side metal layers should also be added to ensure an optimum VDD/VSS supply [Nibhanupudi 2022]. Intel has announced its intentio to introduce power delivery from the backside of the chip using "PowerVias" [Intel 2021].

The effects of the CPU design with back-side power delivery coupled with buried power layers has been benchmarked by [Prasad 2019] using the Arm Cortex-A53 CPU. The authors have shown that buried rails with back-side power delivery can reduce the power noise nearly by a factor of 7. Details about the structure of the BPV & BPR may be found in [Gupta 2020], with discussions about the BPR resistance as a function of different materials such as Tungsten (W), Ruthenium (Ru) or Molybdenum (Mo).

The approach described in [Jourdain 2022] is based on wafer thinning to less than 1 µm (from the initial 300-400 µm thickness), combined with an nTSV build using low-resistivity metals such as Tungsten, Cobalt or Ruthenium, which make the internal connection between the buried power rails and the back-side Power Delivery Network. The buried power rails are 32 nm wide and 105 nm pitch according to [Jourdain 2022], with a total height within the range of 150-200 nm.

The BPR appear in blue (Figure 10) in the 2D process section proposed by Microwind. The BPR described in [Gupta 2020] is fabricated in Tungsten, surrounded by a thin TiN liner (4 nm), and isolated from the substrate by a thin film of SiO2 deposited with atomic layer precision. Some important characteristics related to the design rules implemented in Microwind for 7 nm, 5 nm, 3 nm and 2 nm nodes are reported in Table 3.

Parameter	***7nm***	***5nm***	***3nm***	***2nm/20A***	***1.5nm/15A***
Device	FinFET	FinFET	Nano-Sheet	Nano-Sheet	Stacked NS
λ (nm)	4	4	4	4	3.5
Metal 1 pitch (λ)	6	6	6	5	4
Metal 1 pitch (nm)	24	24	24	20	17
Contacted gate pitch (CGP)	40	40	40	40	35
Routing tracks	7	7	5	3	2
Buried Power Rail	No	No	No	Yes	Yes
Cell height (nm)	192	192	160	100	50

Table 3: Design rules implemented in Microwind for 7nm down to 1.5nm technology nodes.

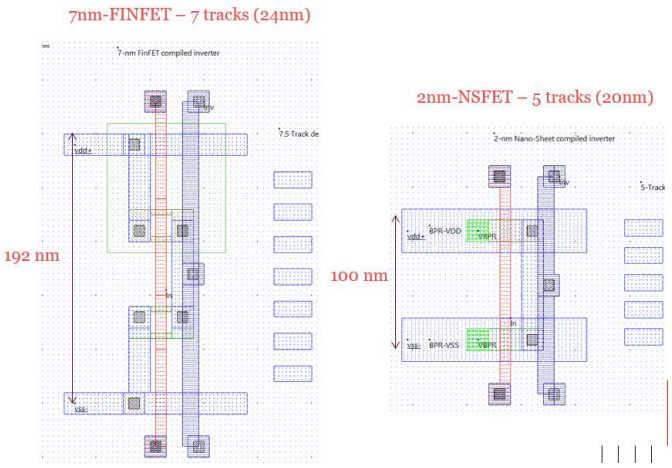


Figure 11: Comparing a 2-input NOR cell compiled by Microwind in 7-nm technology and 2-nm technology (inv5Tracks vs inv7Tracks.MSK).

The gate pitch remains the same and the metal pitch is slowly decreased, while the cell height is drastically reduced due to the adoption of Nano-sheet devices in the 3 nm node, buried power rails in 2 nm and stacked Nano-sheet in 1.5 nm. As seen previously, the cell height has been divided by two between the 7 nm node (Figure 11, left) and the 2 nm node (Figure 11, right) while the contacted gate pitch remains unchanged (40 nm). Therefore, the total cell surface is divided by two.

Although impressive gains are observed in terms of cell height, the overall benefits in terms of silicon area at IC level may not be as high as expected. While the BPR routed in the substrate underneath the cell leaves reasonable space for internal routing, the limited cell height (around 100 nm as illustrated for an inverter in Figure 12) may require upper or lower routing wires when implementing gates that

include routing difficulties such as D-Flip Flops (DFF) or multiple-input AND-OR-Invert (AOI) due to the limited horizontal routing capabilities within the cell, as studied by [Chidambaram 2021].

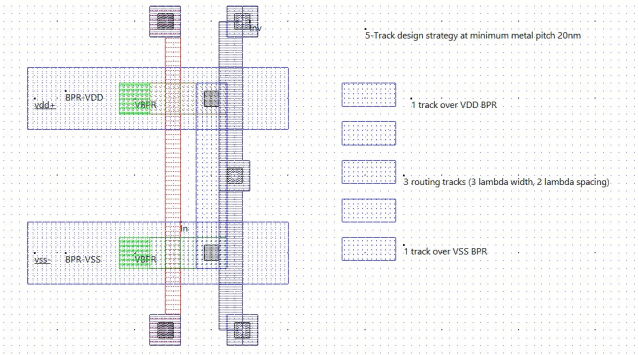


Figure 12: Compiled inverter with 5-Track strategy at minimum metal pitch 5 λ, 20 nm (inv-5tracks.MSK).

Electrical properties of the buried power rail

Thanks to the BPR, the cell area is reduced, all vertical tracks are shorter, including gates and input/outputs. The delay may be decreased by 10% as shown by [Yoon 2022]. The target BPR resistance is around 50 Ω/µm [Prasad 2019][Gupta 2020b], and the via to BPR around 50 Ω/via. Considering a BPR width of 32 nm and a resistivity of 25 µΩ.cm for tungsten and 15 µΩ.cm for ruthenium, the 50 Ω/µm target requires a BPR thickness of 85 nm (Ru) to 175 nm (W) [Chen 2022]. Molybdenum BPR proposed by [Gupta 2021] features a 12 µΩ.cm resistivity with a performance close to ruthenium.

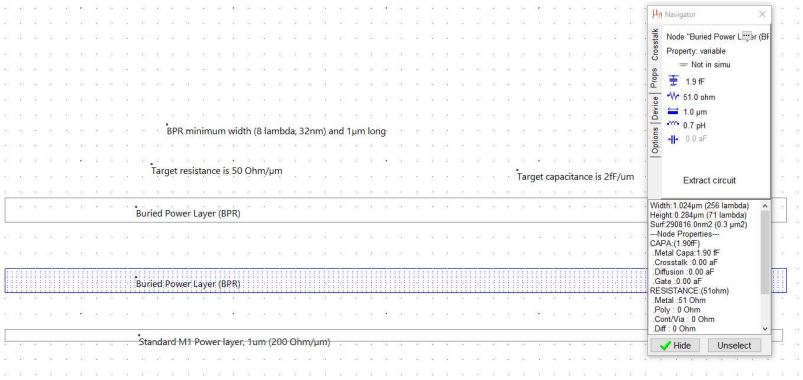


Figure 13: Design of a 32 nm (8 λ) wide, 1000 nm long BPR and extraction of its resistance (bpr-1um.MSk).

We fixed the BPR thickness to 150 nm in our own implementation of the 2 nm/20Å technology, as shown in the cross section of Figure 10. The resistance is tuned using specific parameters of the design rules, namely `rebp` = 1.6 Ω/square (square resistance of BPR), and `revb` = 50 Ω/via-BPR. Concerning the capacitance, the very tall geometry of the BPR leads to values as high as 2 fF/µm that is approximately 10 times the upper metal capacitance (Fig. 13).

Nano-through-silicon-vias (nTSV)

The companion device for back-side power delivery is the Through-Silicon-Via (TSV), in its nano-scale version called nTSV (typically 50-100 nm diameter), one order of magnitude smaller than the µTSV which has a diameter within the range 1-10 µm [Milojevic 2021]. As demonstrated by [Jourdain 2022],

the nTSV nicely connects the BPR to the back side of the die (Figure 14) by aligning the BPR and the nTSV. This study considers a nTSV BPR pitch around 200 nm and a nTSV diameter of around 100 nm. In [Hossein 2020], the nTSV diameter is as low as 50 nm and its 500 nm height corresponds to the ultra-thin substrate.

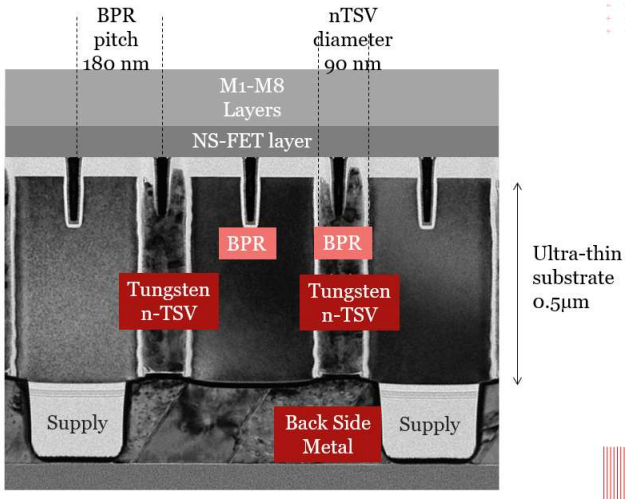


Figure 14: Ultra-thin substrate (0.5 µm), buried power layer (BPR), nano-Through-Silicon-Vias (nTSV) connecting to back side VSS/VDD supply; adapted from [Jourdain 2022].

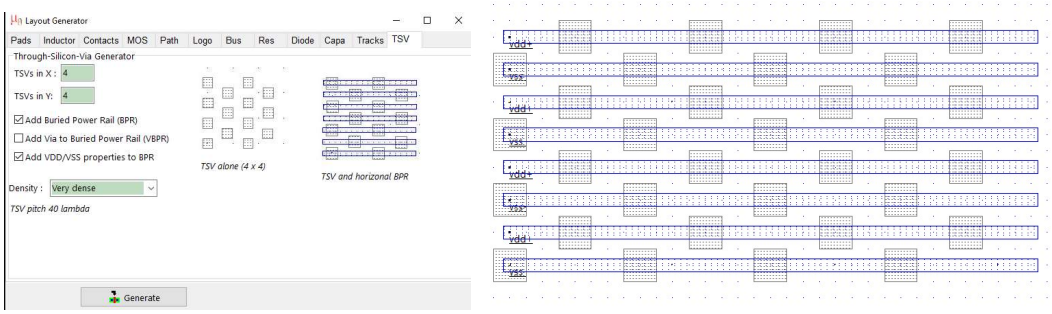


Figure 15: TSV generator and BPR aligned to the TSV grid in Microwind, and associated nTSV array in very dense mode (tsv-4x4-very-dense.MSK).

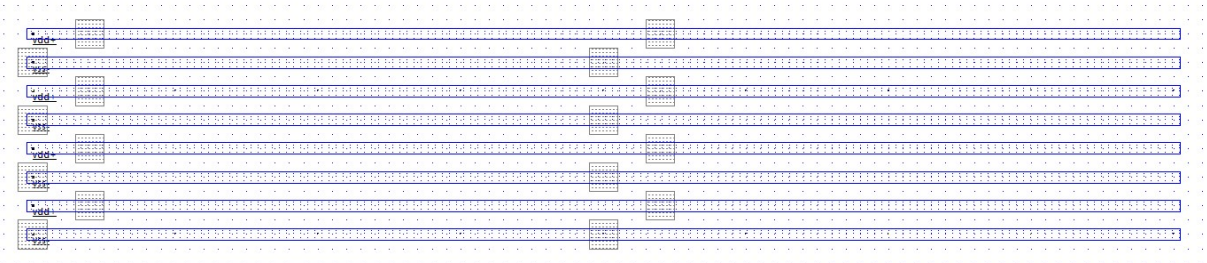


Figure 16: nTSV array in relaxed mode (tsv-4x2-relaxed.MSK).

In its smallest form, the nTSV has a resistance of around 5-15 Ω [Nibhanupudi 2022] [Sisto 2021] and a capacitance of 200 fF when travelling through an ultra-thin substrate of 0.5 µm [Chen 2021]. The total resistance of the supply path including vias, BPR and nTSV is estimated to be 200 Ω/µm [Jourdain 2022]. This value may vary according to the material used to fill the BPR and nTSV.

The TSV array with associated BPR can be generated in Microwind using the screen shown in Figure 15. In very dense designs, vias are generated according to the nTSV pitch, controlled by design rule

`rt02` (40 λ, 160 nm by default). The BPR used to supply the VDD and VSS of logic cells are routed horizontally. All nTSV placed on the same line correspond to the same supply, either VDD or VSS. In relaxed mode (Figure 16), the spacing between nTSV is increased.

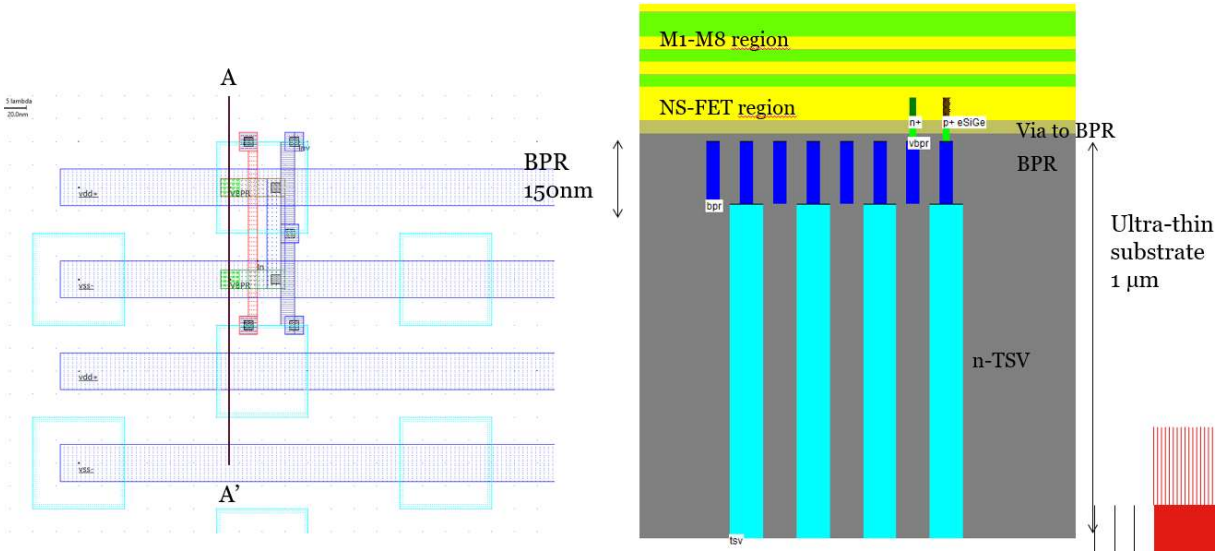


Figure 17: One inverter connected to the VDD/VSS BPR & nTSV array (inv-bpr-tsv.MSK).

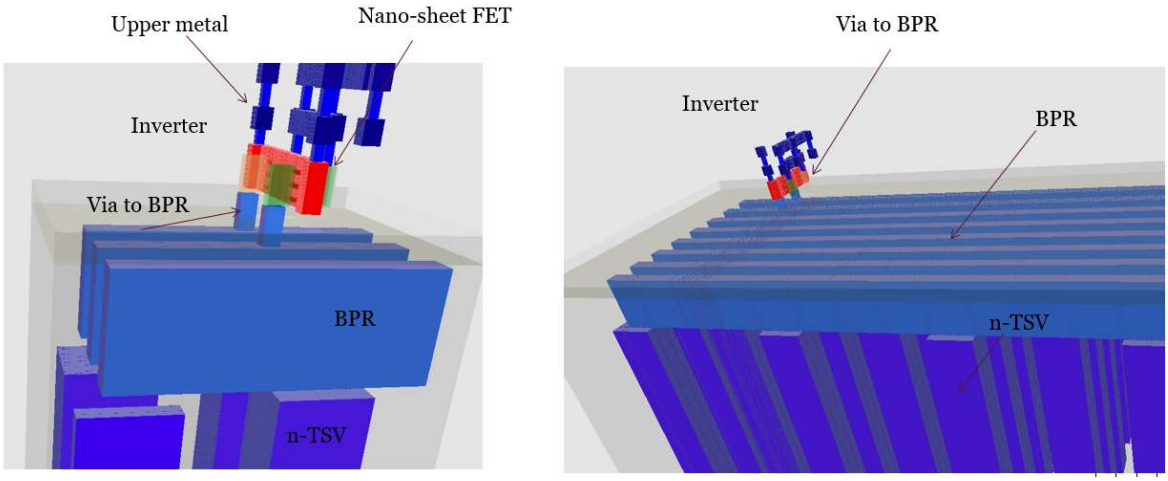


Figure 18: 3D views of the connection from the logic cell to the back-side power delivery including the via to buried power layer and the nano-Though-Silicon-Via (inv-bpr-tsv.MSK).

As the TSV and BPR rails are aligned to the cell size, we can place an inverter on the power grid and observe the cross-section at the contact location between the logic devices and the supply. The later starts by a vertical via to BPR (VBPR), followed by the BPR (150 nm height) and finally the nTSV at regular intervals. The VDD and VSS supplies are applied from the back side of the thinned substrate, i.e. on the bottom side of the nTSV (Figures 17 and 18).

DESIGN PARAMETER	***UNIT***	***CODE***	***NAME IN RULE FILE***	***VALUE IN 2-NM PROCESS***
LAMBDA	nm	λ	lambda	4.0
CORE SUPPLY	V	VDD	Vdd	0.65
DEVICE TYPE		NanoSheet	nsfet	3
WIDTH FAST	λ	WF	nswhp	8
WIDTH SLOW	λ	WS	nswlp	4
DEVICE HEIGHT	nm	HNS	thpoly	55

THICKNESS NS	nm	TNS	tns	5
SPACING NS	nm	TSP	tsp	10
NUMBER OF NS		NS	nsfet	3*
GATE LENGTH	λ	GL	R302	2
GATE PITCH	nm	CGP	cgp	40
SPACER WIDTH	nm	SW		10
CONTACT SIZE	λ	CS	R401	2
EOT	nm	EOT	b4toxe	0.95
M1 WIDTH	λ		R501	3
M1 SPACING	λ		R502	2
METAL PITCH	nm	MP	R501+R502	20
METAL TRACKS		5T	tracks	2
WIDTH BPR	λ		RK01	8
SPACING BPR	λ		RK02	12
VIA BPR	λ		RK03	4
DIE THICKNESS	µm		THDI	1.0
RULE FILE				Cmos20a.rul

Table 4: Basic parameters of the 3-nm process implemented in Microwind (cmos20a.RUL); (*) the number of nano-sheets (three by default) can be changed from two to four.

Along the parasitic components we must consider the IR drop in the supply rails linked to the supply current peak (I) passing through the supply network resistance (R). According to [Ryckaert 2019], the BPR/nTSV approach demonstrates lower IR drop and overall lower performance losses.

As the current peak is mostly related to the switching current of the nFET and pFET, it can be moderated by low-power design strategies, but its reduction is usually limited. On the other side, R is strongly dependent on the VDD and VSS supply networks, namely the geometry and the interconnect material. In this case, specific care is dedicated to the choice of these parameter to enable a global resistance of the back-side nTSV and internal BPR significantly lower than the traditional front side resistance.

Summary of design rules

Table 4 summarizes the main characteristics of the 2-nm/20Å technology design rules implemented in Microwind. The lambda unit (λ) is the same as for the 7-nm, 5-nm and 3-nm technology nodes. The supply voltage VDD also remains at 0.65 V. The number of nanosheets is defined as three stacked layers, with 5 nm thickness (TNS) and 10 nm spacing (TSP). These values are the same as for 3 nm devices. The total device height is around 60 nm. The number of nanosheets is defined in `cmos20a.rul` using parameter *nsfet*. It can also be reconfigured in the compiler menu. We use three nanosheets by default.

Nano-Sheet implementation in Microwind

Layout design in Microwind uses integer units called lambda (λ). This strategy is not optimal in terms of silicon area but its great benefit is that it makes the layout nearly independent of the technology. Design rules have remained nearly the same for the past 30 years. In our 2-nm implementation, λ is kept at 4 nm, the same value as for the 7-nm, 5-nm & 3-nm nodes. In other words, no scale down is required – the space, speed and consumption benefits stem from design and device innovations.

The minimum channel length is 2 λ as usual, the contacted gate pitch (CGP) is 10 λ (quite similar to FinFET & MosFET nodes), and the metal pitch (MP) is 5 λ (3 λ width +2 λ spacing) – a small gain compared to 7-5-3 nm (3 λ width + 3 λ spacing). This small improvement enables to rout five horizontal metal tracks within a reduced vertical cell height. Dummy gates are activated by default and added on both sides of the active device, with a gate pitch of around 10 λ (40 nm, see Figure 19). Note that the default NSFET width is 4 λ (16 nm), which corresponds to the slow speed design strategy. It is worth

noting that the effective width *Weff* is much larger than the W footprint, as the effective channel is more than six times higher, according to Figure 4.

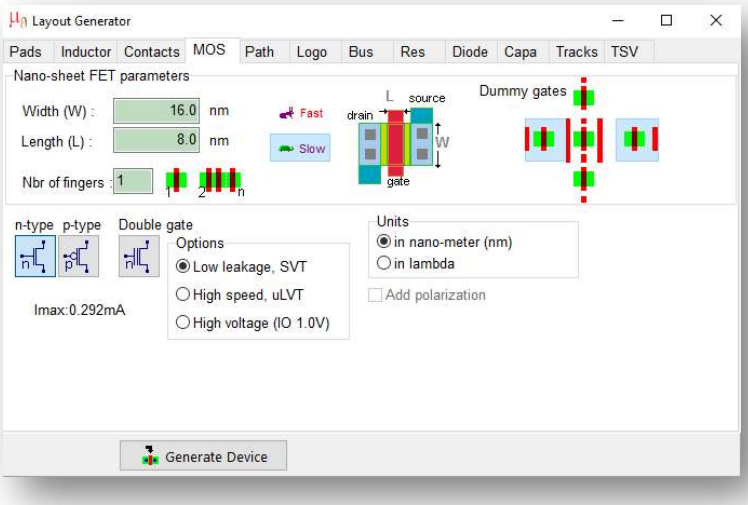


Figure 19: In 2-nm nano-sheet technology, dummy gates are selected, and the default width is 16 nm (the Weff being more than 6 times larger than W).

Basic Inverter

The layout of a basic inverter is shown in Figure 20 (left). The cross-section (Figure 20, right) follows the vertical axis A-A'. The NSFET devices have three stacked nano-sheets, with each nano-sheet being isolated from the gate by a thin oxide (Al_2O_3,ZrO_2, HfO_2..). A review of publications regarding the NSFET devices & technology is proposed by [Valasa 2022].

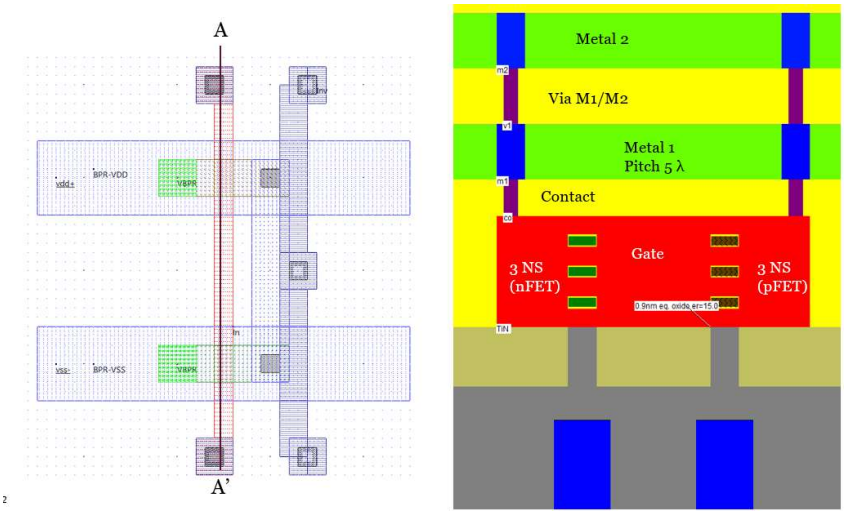


Figure 20: Basic inverter with BPR supply and slow mode (inv5Tracks.MSK).

Two versions of the NSFET are considered in Microwind, one called "slow" mode (W=4 λ), the other called "fast" mode (W= 8λ); both are shown in Figure 21 along with the associated cross-section showing the three stacked nano-sheets. The hand-made design of the NSFET can use any channel width larger than or equal to the minimum width (4 λ).

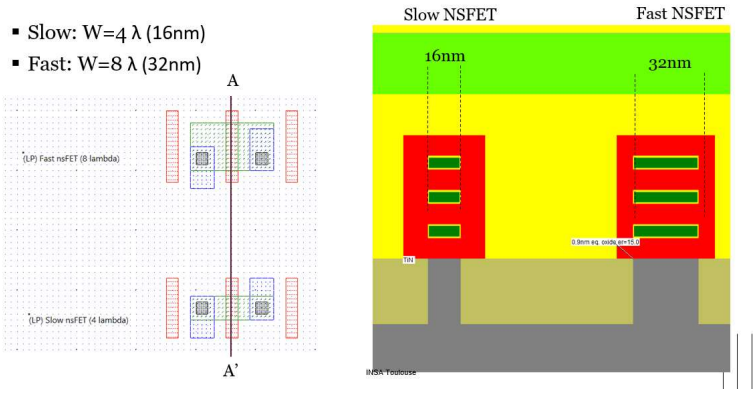


Figure 21: Slow and fast devices, layout view, cross-section and 3D view (nsFETs.msk).

NS-FET Performances

The published results concerning the ION/IOFF currents for nano-sheet devices show important variations among the authors. One reason pointed out by [Chu 2018] is the manner of evaluating the effective width Weff in order to normalize the current to a unit per µm – some authors opt for the NS footprint and others the NS perimeter. Some authors like [Chu 2018] and [Huang 2020] have measured the single device, while [Yoon 2022] and [Jeong 2020] have relied on simulation (Table 5).

Parameter	*Unit*	*[Huang 2020]*	*[Yoon 2022]*	*[Jeong 2020]*	*[Chu 2018]*	*[Ahmed 2020]*	*Microwind*
Ion nFET	µA/µm	406	660	1410	1510	900-2500	1500
Ion pFET	µA/µm	180	660	1130	1650	900-2500	1280
Ioff	nA/µm	100	5	1	20	2	10
Sub-Vt Slope	mV/dec	68		75	140	65	65
VDD	V	0.65	0.70	0.70	1.00	0.70	0.65
Method		Meas	Simu	Simu	Meas	Simu	Simu

Table 5: Nano-sheet ION & IOFF currents from a selection of publications.

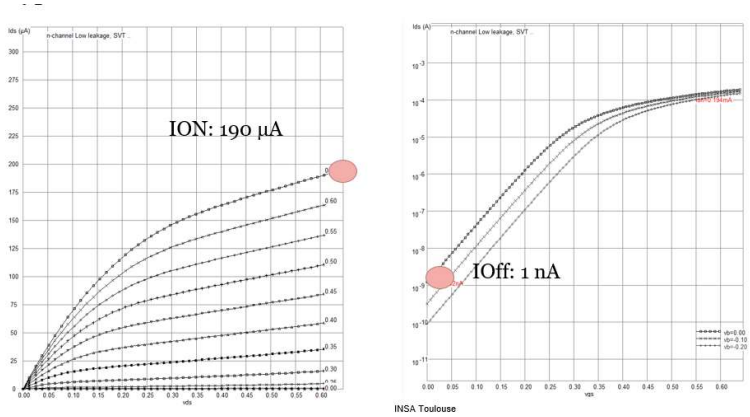


Figure 22: ION/IOFF for the slow NSFET, n-type @ 0.65 V.

The ION current for the slow n-type device is around 190 µA for total channel width of 128 nm (Figure 22) and corresponds to the maximum available current for this device at nominal voltage (VDD=0.65 V). The IOFF current corresponds to VG=0, which is around 1 nA. As for the slow p-type device, ION is 160 µA and IOFF is around 1 nA (Figure 23). The subthreshold slope is around 65 mV/decade.

The ID/VD curves of the slow and fast devices show an ION current that is nearly double. Using the option layer, we can turn the device to high-performance mode for a supplementary boost of around 25%, but at the cost of an IOFF multiplied by 10 (Figure 24). The use of such a device should be restricted to situations where the speed is critical (clock tree, critical logic path, needs for highest performance) and power saving is no more the priority.

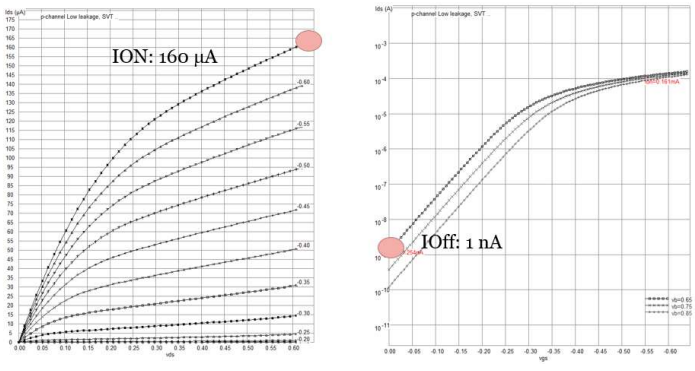


Figure 23: ION/IOFF for the slow NSFET, p-type @ 0.65 V.

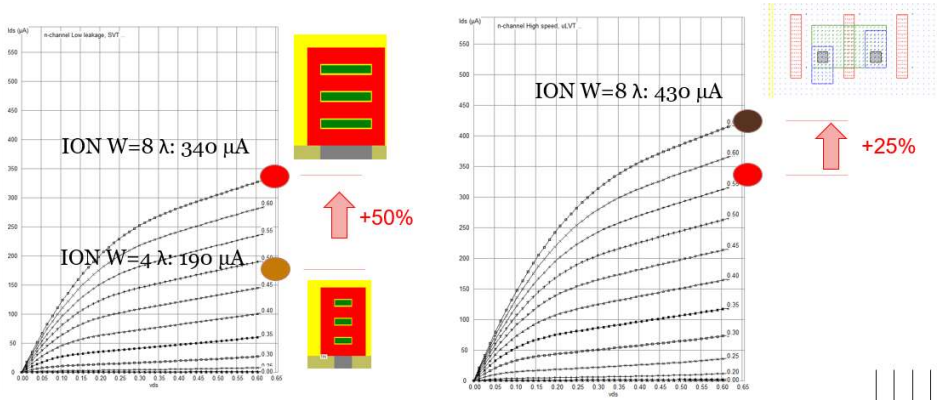


Figure 24: Comparing the ION of the slow & fast nFET (left), and the supplementary ION boost using the high-speed device option.

In our implementation of the 2-nm NSFET, the low-leakage default device has a threshold voltage around 0.30 V, while the high-performance device has a low Vt around 0.25 V. The Vt adjustment is achieved by modulating the effective work function (EWF) of the gate through the introduction of specific metallic material or modifying the oxide properties, as described in [Chen 2022b].

NS-FET Booster

An approach for increasing the ION current furthermore is to increase the number of nano-sheets. Authors like [Ahmed 2021] [Ryckaert 2021][Schuddinck 2022] have analyzed the performances of four stacked nano-sheet devices. In Microwind, the parameter `nsfet` (3 by default) controls the number of nano-sheets. It can be changed from 2 to 4 NS using a selection in the compiler menu, as illustrated in Figure 25. Low power devices such as smartphones may require only 2 NS, general purpose devices such as laptops 3 NS, and high-performance devices such as servers 4 NS.

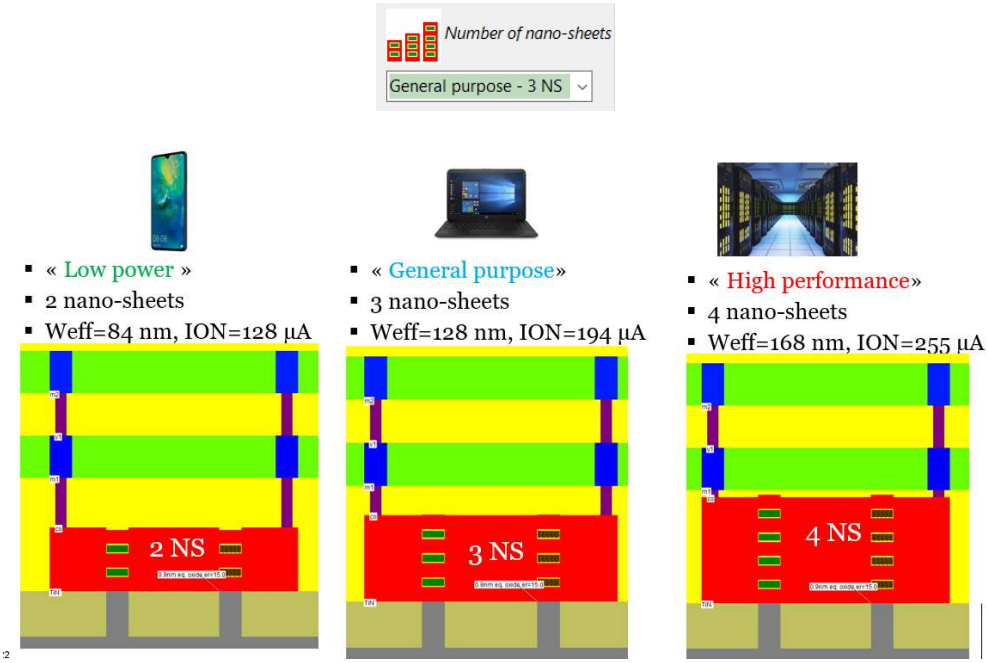


Figure 25: The number of nano sheets has a direct influence on the ION current and may be a booster to match high performance computing requirements (4 NS) or meet the low power requirements (2 NS).

NS-FET Capacitance

The value of the total gate capacitance *Cgg* for a slow device (channel footprint: 16 nm) is tuned to 100 aF, while the fast device (32 nm) is around 200 aF. The input capacitance of the inverter is the sum of nFET *Cgg*, pFET *Cgg* and the extra metal and gate connection. Its value is around 250 aF. The output capacitance is smaller, around 50 aF per device. Some values found in a selection of publications are reported in Table 6.

	[Ahmed 2020]	*[Jeong 2020]*	*[Yoon 2022]*	*[Choi 2020]*	*Microwind Slow (W=4 λ)*	*Microwind Fast (W=8 λ)*
Number of NS	4	3	4	3	3	3
Weff (nm)	144	300	120	116	128	224
Gate capacitance (aF)	110	130	328	130	100	200
VDD (V)	0.70	0.70	0.70	0.70	0.65	0.65

Table 6: Gate capacitance according to a selection of publications.

Modelling the NSFET

The reference model for simulating the Nano-Sheet FET is the Berkeley BSIM-CMG, which stands for Common-Multi-Gate [BSIM-CMG 2022]. At the time of writing, BSIM-CMG 111.2 was not open source but BSIM-CMG 111.1 was available for download. Some details about the model can be found in [Dasgupta 2020].

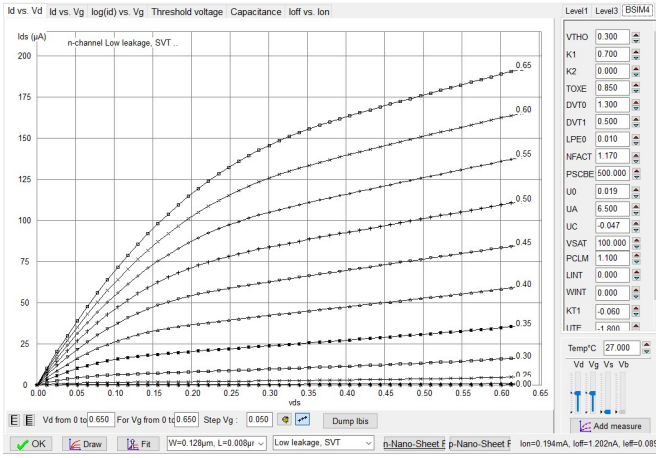


Figure 26: Simplified BSIM4 model implementation in Microwind used to simulate the 2-nm nano-sheet devices.

For the sake of simplicity, Microwind uses a simplified version of the BSIM4 model for simulating the Nanosheet FET (Figure 26). This version of BSIM4 follows the main equations detailed in the book [Liu 2001]. The BSIM4 model was not initially targeted to FinFET nor double-gate/nano-sheet devices. However, it can fit in first order the I/V characteristics of advanced devices. Using the BSIM4 model instead of BSIM-CMG may lead to significant mismatch between simulations and measurements, specifically for analog and radio-frequency designs. As the BSIM4 suffers from some non-symmetrical equations, it does not handle self-heating (corrected in late versions, e.g. BSIM6 [Agarwal 2013] and BSIM-CMG). Quantum effects are also ignored in BSIM4 models.

Getting started with the 2nm design

Hand-made design of an inverter

1. Select the “NsFET Gate” layer in the palette window (Red).
2. Fix the first corner of the box with the mouse. While keeping the mouse button pressed, move the mouse to the opposite corner of the box. Release the button. This creates a narrow gate. The box width should not be inferior to 2 λ, which is the minimum and optimal thickness of the gate.
3. Select “N+ diffusion” by clicking on the palette of the N+ Diffusion (Green).
4. Draw a n-diffusion box at the bottom of the drawing as in Figure 27. The N+ diffusion should have a minimum of 4 λ height and extension at both sides of the polysilicon gate. The intersection between the N+ diffusion and gate corresponds to the channel of the N-device.
5. Select “P+ diffusion” by clicking on the palette of the N+ Diffusion (Brown).
6. Draw a P+ diffusion box, as shown in Figure 27. The intersection between diffusion and gate creates the channel of the P-device.
7. Select “Metal 1” and draw a box over the N+ & P+ area. The minimum width is 3 λ.
8. Select the icon “Connect layers”  , click on the intersection N+/metal, and again on the intersection P+/metal.
9. Add VDD and VSS properties.
10. Add a clock to the input gate.
11. Add a “visible” property to the output (“Visible node”).
12. Click “Simulate”. Click “More” until you reach 1 ns.

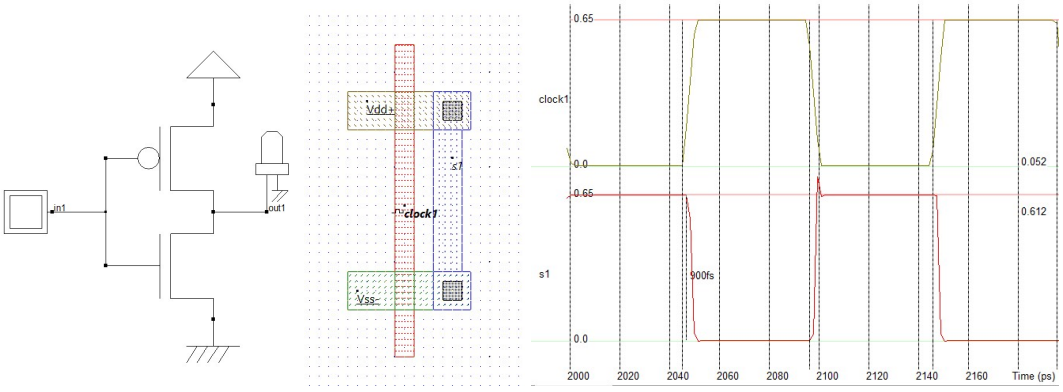
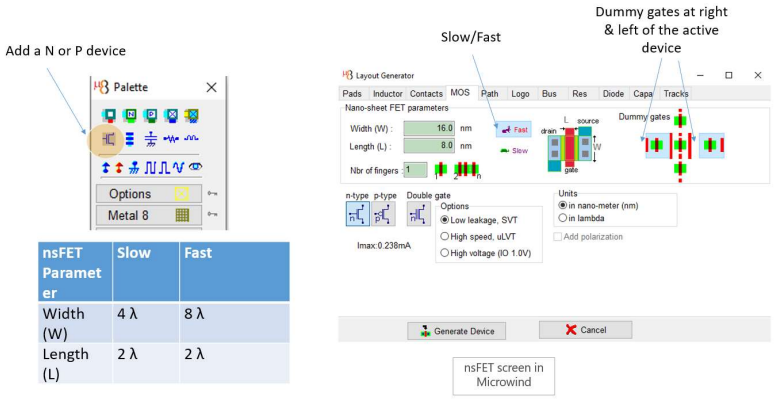


Figure 27: Steps to draw a simple inverter (mySimpleInverter.MSK).

Another approach to avoid design rule errors is to instantiate the n & p devices directly using the layout generator. Just click the device icon on the palette (“Generate Device”), place the component on the layout. Click the same icon, this time selecting “p-type”, and place the component on top of the n-type device. Dummy gates are added by default for manufacturability purpose. The devices should be aligned. The minimum distance between N+ and P+ diffusions is 6 λ. All gates should touch together in order to merge vertical layers in a regular way, as illustrated in Figure 28.



nsFET Parameter	Slow	Fast
Width (W)	4 λ	8 λ
Length (L)	2 λ	2 λ

Figure 28: Select a n-channel or p-channel NSFET.

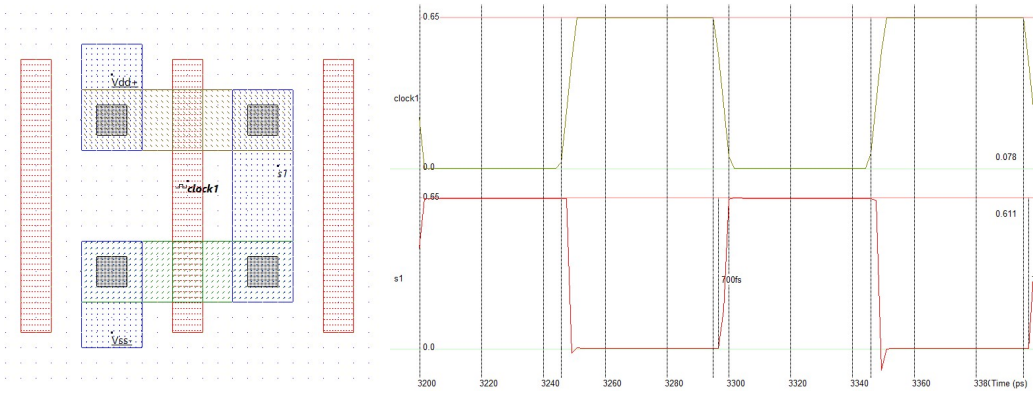


Figure 29: Creating an inverter with n-channel or p-channel NSFET generated by Microwind.

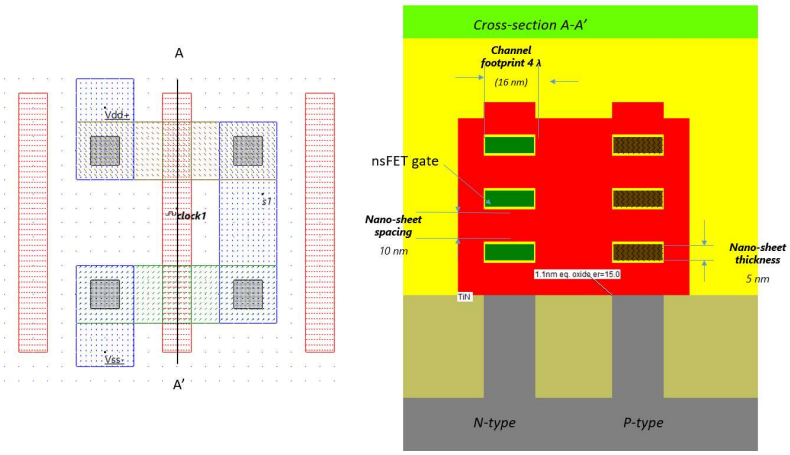


Figure 30: Cross-section of the n-channel or p-channel NSFET generated by Microwind.

The N & P devices use a 4 λ channel footprint, which corresponds to the "slow" design style. The nano-sheet cross section can be displayed using the icon  , with the vertical selection corresponding to the active gate (A-A'). The three stacked nano-sheets are shown (Figure 30), each with a thickness of 5 nm and spacing of 10 nm. The equivalent channel width *Weff* is

$$W_{eff} = ns \times (2W + 2TNS) = 3 \times (2 \times 16 + 2 \times 5) = 128\,nm$$

where *ns* is the number of nano-sheets, *W* is the channel footprint and *TNS* the nano-sheet thickness.

Compile one inverter, 5T

Microwind includes a specific tool to handle the generation of a complete inverter. Other simple logic cells such as NAND, NOR, AND, OR can also be generated using this tool. The cell height corresponds to the “5T” approach, with the supply wires VDD and VSS routed by means of buried power rails. The link between BPR and diffusions is established using the “Via to BPR” (vbpr). The device width can be either “Slow” (4 λ footprint) or “Fast” (8 λ). An example of compiled inverter is shown in Figure 31. The performances correspond to 3-NS devices (default configuration). If you run the Design Rule Checker (DRC), the layout should be error-free.

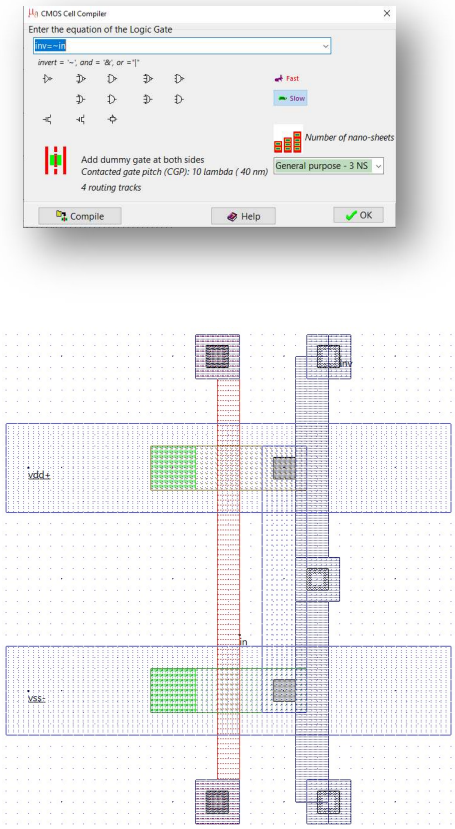


Figure 31: Compiling basic gates with the Microwind cell compiler.

Logic Design with Nano-Sheet

Ring Oscillator

Building a ring oscillator is possible by compiling three successive inverters; such a device oscillates freely without any external stimulation. The only required work is to build the interconnections according to the schematic diagram shown below and to add the VSS and VDD supplies. The loading condition corresponds to the shortest possible wire and one single gate (the next input stage).

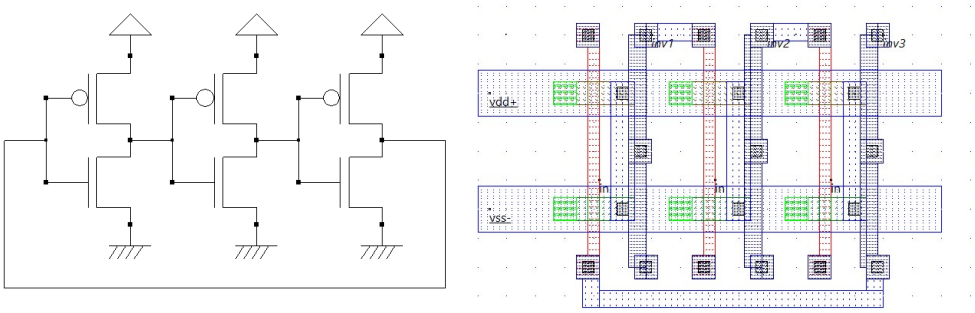


Figure 32: A simple 3-stage ring oscillator based on compiled inverters "Fast" mode (RO3-FO1.MSK).

The design corresponds to minimum parasitic resistance and capacitance, which corresponds to maximum performance. The observed frequency is approaching 90 GHz. A further boost can be obtained by further increasing the device width or by using the "high-speed" option, which is accessible using the option layer. Instead of the default "low leakage" option, we surround all six devices by an option layer and change the device option to "high speed". The resulting simulation shows an oscillating frequency of 140 GHz, that is about a 2.4 ps/stage delay (Figure 33).

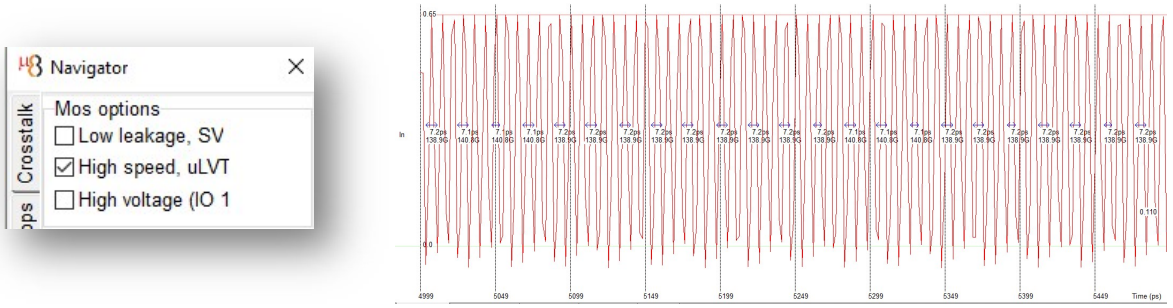


Figure 33: Turning the device option to "High-speed" increases the oscillating frequency to 140 GHz (RO3-FO1-Fast.MSK).

Ring Oscillator with Fan-Out

Many scientific publications include simulations of ring oscillators, including [Wang 2020], [Ahmed 2020], [Na 2021] and [Ryckaert 2021]. As the number of stages and operating conditions significantly vary among publications, direct comparison of the published results is not always possible. For example, [Na 201] uses 19 stages, each stage connected to M1 to M6 and then back to M1. In [Wang 2020], a 3-stage ring oscillator is used, each stage loaded by a metal track with a length corresponding to 25 × (CGP + MP), where CGP is the contacted gate pitch (48 nm) and MP is the metal pitch (28 nm), which intends to represent typical loading conditions. Comparison is possible only if similar operating conditions are used (VDD, loading, options, device size) and if power and frequency per stage is evaluated, instead of the whole ring oscillator performance.

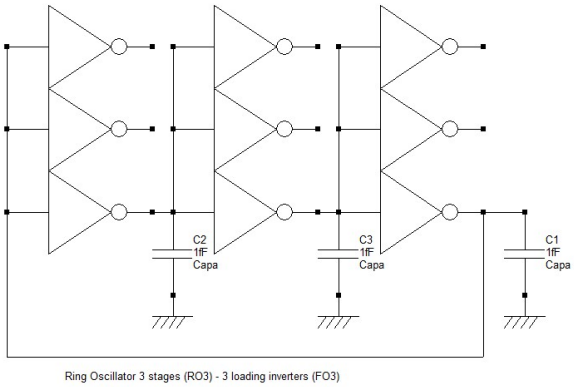


Figure 34: Each inverter output is connected to three inputs to emulate a significant load.

We use the following strategy for simulation: we consider a 3-stage RO with a 3-input load. The corresponding layout is shown in Figure 35. The capacitance load of each stage is around 1 fF, a value very close to the effective capacitance *Ceff* evaluated by [Jung 2021] mostly consisting of three total gate capacitance *Cgg*. In contrast to [Na 2021], the upper metal layers are not used and the routing of interconnects only uses the lower metal layer *metal1*. The value of *Cgg* is estimated to around 250 aF/gate.

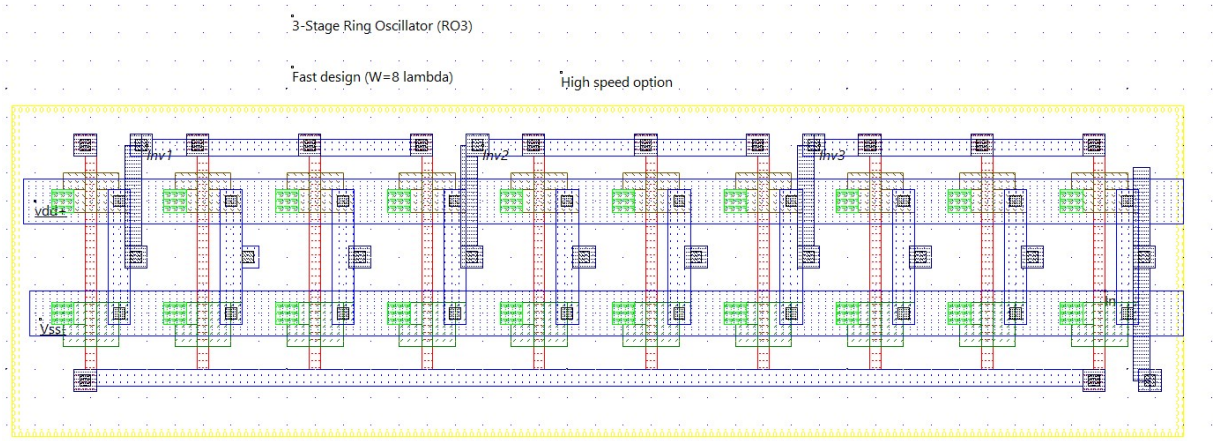


Figure 35: RO3, FO3 with fast design and supplementary boost using high speed device option (RO3FO3-Fast.MSK).

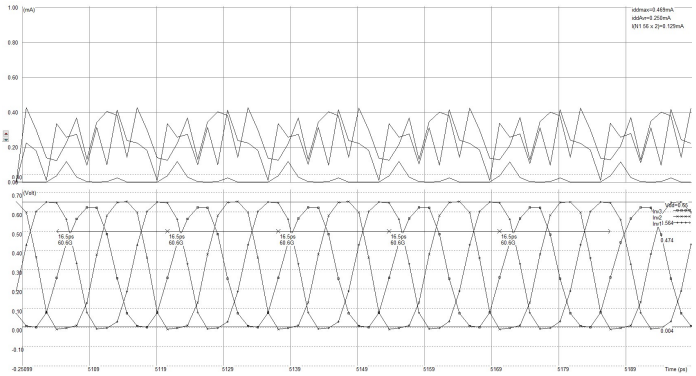


Figure 36: The 60 GHz oscillating frequency f0 and 160 µW total power consumption Ptot for three inverters is converted into a frequency of 3.f0 & Ptot/3 for one inverter stage (RO3FO3-Fast.MSK).

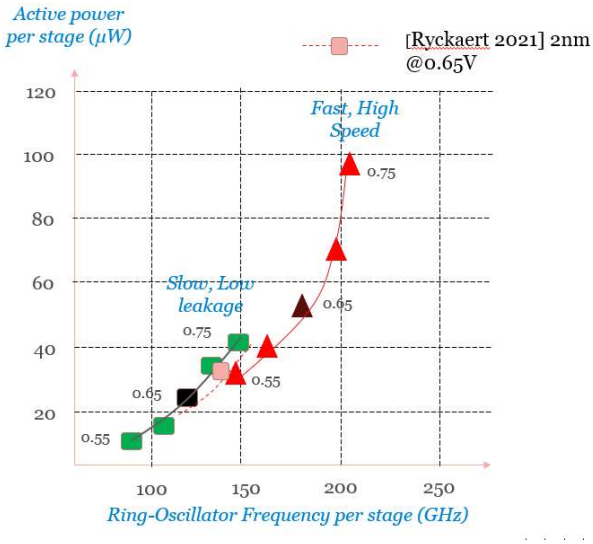


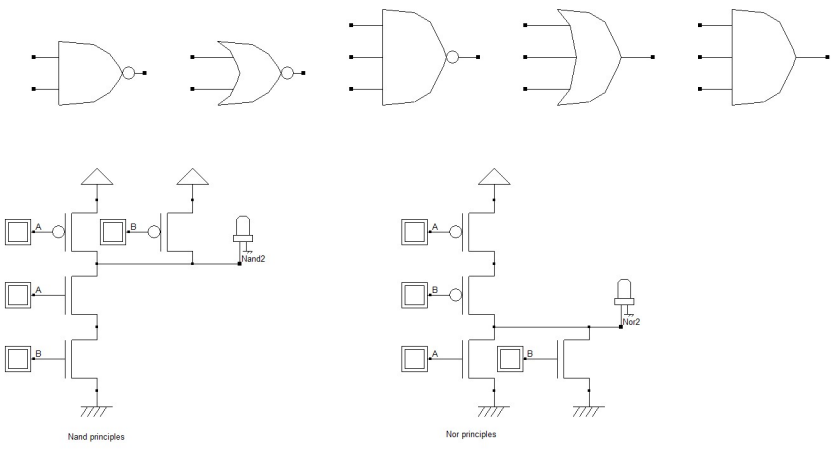
Figure 37: Performance of the ring oscillator in the Power/Frequency domain (RO3FO3-Slow.MSK, RO3FO3-Fast.MSK).

We extract the frequency per stage by multiplying the RO frequency by three (Figure 37). We can also extract the power per stage by dividing per 3 the total power consumption. In the simulation, we used "fast" design approach and considered high-performance devices instead of the default low power, so as to maximize the oscillating speed. Then, we iterate the simulation for VDD ranging from 0.55 to 0.75 V, by steps of 50 mV.

Figure 37 compares the performances of the slow, low-power device (in green) and the fast, high-performance devices (in red) for VDD varying from 0.55 to 0.75 V. At nominal voltage 0.65 V, the frequency per stage is around 120 GHz for slow-LP, and 180 GHz for fast-HP inverters. The performances are comparable to the results published in [Ryckaert 2021] (130 GHz @ 0.65 V).

Basic cells

We use again the cell compiler to generate basic cells, namely the NAND, NOR, NAND3, OR3 and AND3 gates. The cells are placed horizontally with a regular CGP and share the same VDD (top of the cells) and VSS (bottom of the cells, Figure 38). The A, B and C inputs were merged to simulate the gate inputs simultaneously, by means of M1/M2 routing and appropriate vias on the bottom. The simulation shows a delay ranging from 1 to 2 ps for unloaded Nand & Nor gates, and increased to 3-4 ps for unloaded AND & Or gates, due to the supplementary inverter stage (Figure 38).



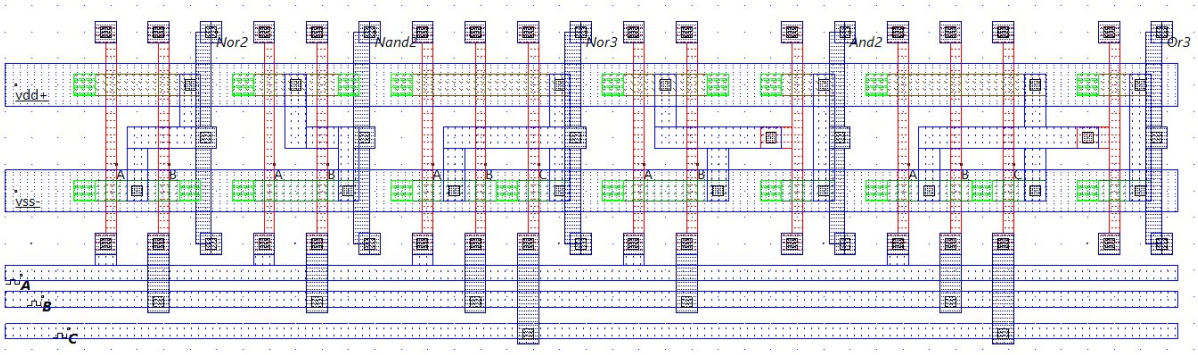


Figure 38: Compiled basic gates using the cell compiler in 2-nm NSFET technology, with 5T strategy (basicgates.MSK).

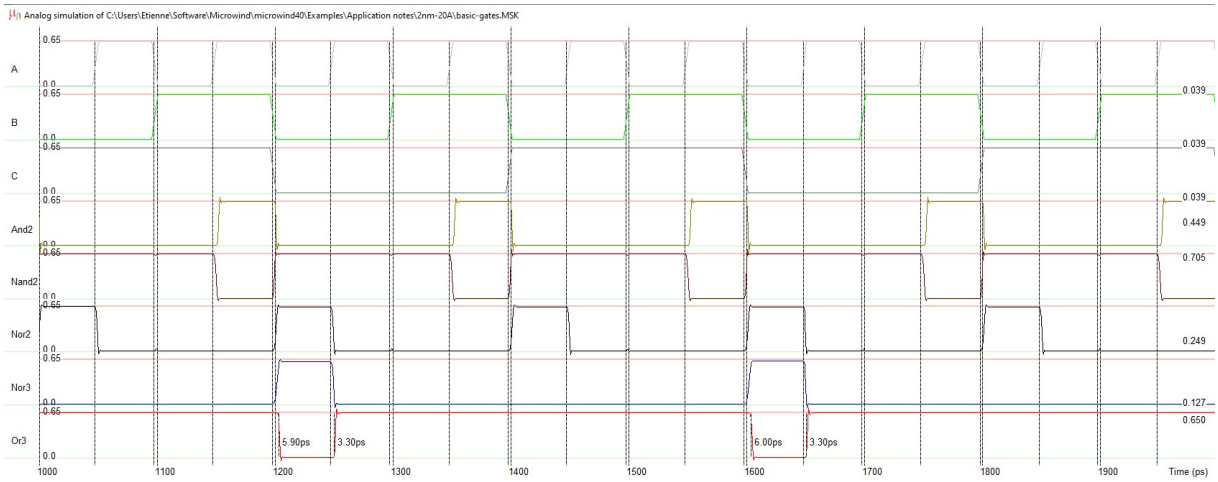


Figure 39: Simulation of Nor2 in 3-nm NSFET technology. The largest delay is observed for multiple-input AND & OR gates due to an inverter stage (basicgates.MSK).

Interconnect delay

All these intrinsic delays are optimistic as no load has been connected to the floating outputs. This corresponds to an open output circuit or minimum-load configuration. The connection of the outputs input gates through interconnects are equivalent to a significant RC delay, which slows down the propagation. Although the intrinsic delay is dominant for short and medium interconnects (Figure 40), the interconnect delay has a strong impact on the total switching delay for long interconnects. The resistance of lower metal layers used for intra-cell routing ranges between 100 Ω/µm and 1 KΩ/µm [Prasad 2019] [Wang 2020] [Seon 2021].

Lower metal layers have high resistance due their small section, as shown in Figure 40. Higher metal layers are thick and wide, with lineic resistance around 10 Ω/µm. The lower metal capacitance is around 100-500 aF/µm. Interconnects with small pitch and large thickness have significant lateral capacitance (crosstalk capacitance).

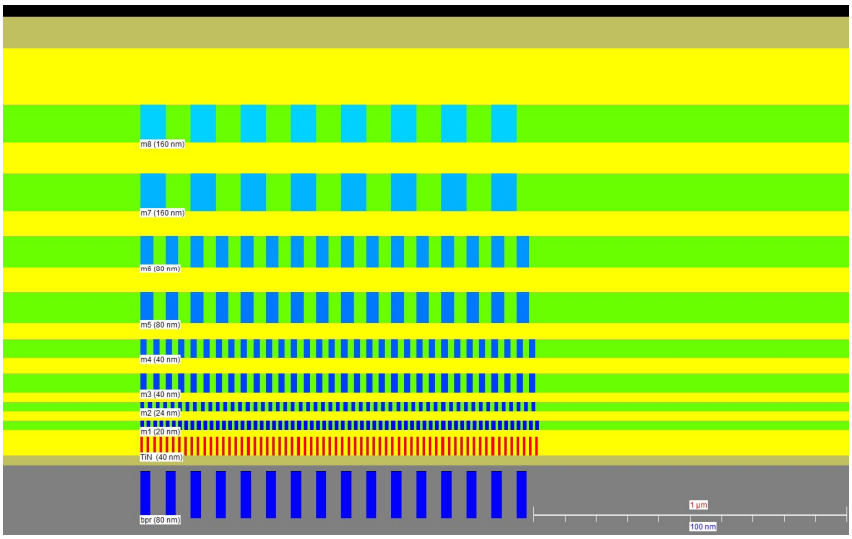


Figure 40: Vertical cross-section of metal layers including the buried power rail, with the associated pitch in nm (all-metal-layers.msk).

Although no significant gain is observed between fast and slow inverter designs for short and medium interconnects, fast inverters limit the overall delay as compared to slow inverters when long metal wires (4 µm and above) are used.

The pitch, width, spacing, thickness and associated capacitance and resistance per µm for each metal layer (including the buried power rail) is reported in Figure 42. For the BPR via and TSV, the resistance is expressed in Ω/via; for all other metal layers, we assume a 1 µm width and compute the associated resistance and capacitance per µm from the square and lineic parameters declared in the technology rule file `cmos20a.rul`.

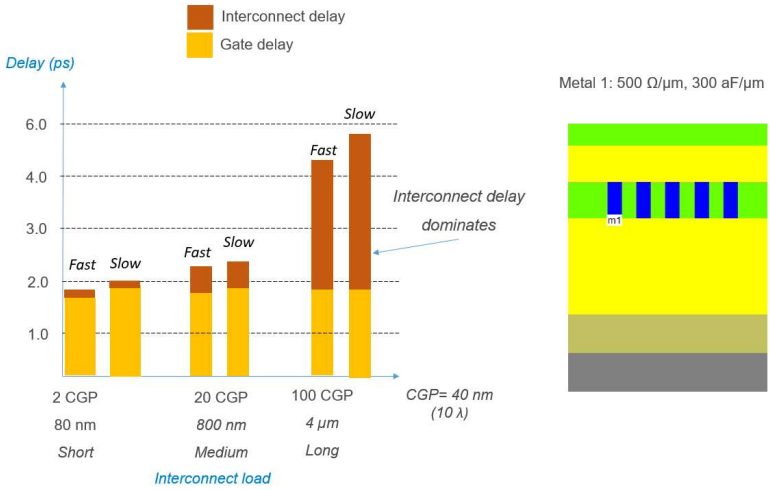


Figure 41: The interconnect delay has a strong impact on the total switching delay for medium to long interconnects.

Design rules and electrical parameters

Layer	Pitch	Width	Spacing	Thickness	Capa	Res
	nm	nm	nm	nm	af/µm	ohm/µm
metal8	160	80	80	120	130	3
metal7	160	80	80	120	130	3
metal6	80	40	40	100	180	25
metal5	80	40	40	100	180	25
metal4	40	20	20	60	240	100
metal3	40	20	20	60	240	100
metal2	24	12	12	30	310	249
metal	20	12	8	30	250	249
TiN Gate	40	8	12	60	300	6250
vbpr	80	16	48	50	0	50
bpr	80	32	48	150	1900	50
tsv	80	32	48	1000	0	3

Figure 42: Metal pitch, width, spacing, thickness and associated capacitance and resistance per µm. For the BPR via and TSV, the resistance is expressed in Ω/via.

SRAM design with BPR

The 6-transistor static memory (also called 6T-SRAM) consists of a 2-inverter stable loop that stores the data and two access transistors to either import or export the logic data through so-called bit lines. When the data is imported from the outside to the cell (the data through BL, its opposite through ~BL), we speak of the write cycle; when the data is exported, it is called the read cycle. The cell structure is optimized for multiplication in X, Y in order to create a matrix of cells, typically 1000 x 1000, leading to a 1 Mega-bit memory plane.

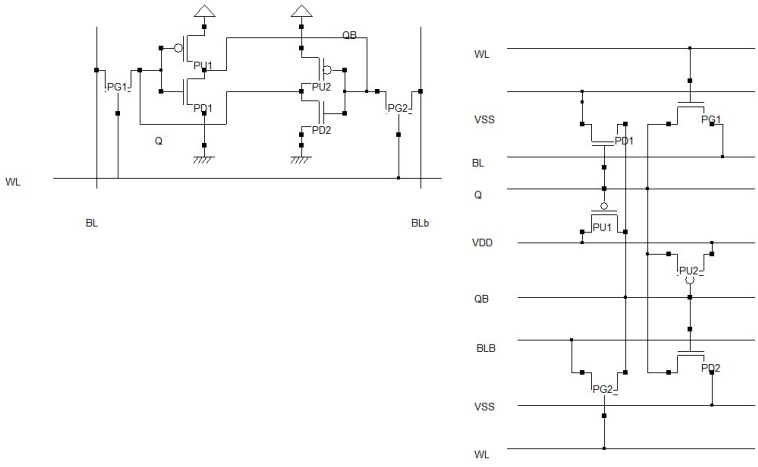


Figure 43: Proposed implementation of the 6T-SRAM adapted from [Gupta 2021c].

The schematic of a six-transistor SRAM bit-cell is shown in Figure 43 (left). A possible implementation with all signals routed horizontally is proposed in Figure 43 (right) [Gupta 2021c]. The cell consists of two pairs of inverters (*PU1-PD1, PU2-PD2*) and two pass gates (*PG1 and PG2*). The *bitline* signals *BL* and *BLb* are significantly enlarged by the introduction of the buried power rails (Figure 44), decreasing its serial resistance and thereby significantly enhancing the write margin and overall performances, without any silicon area penalty, as the SRAM area remains the same [Salahuddin 2019][Salahuddin 2020][Gupta 2021c].

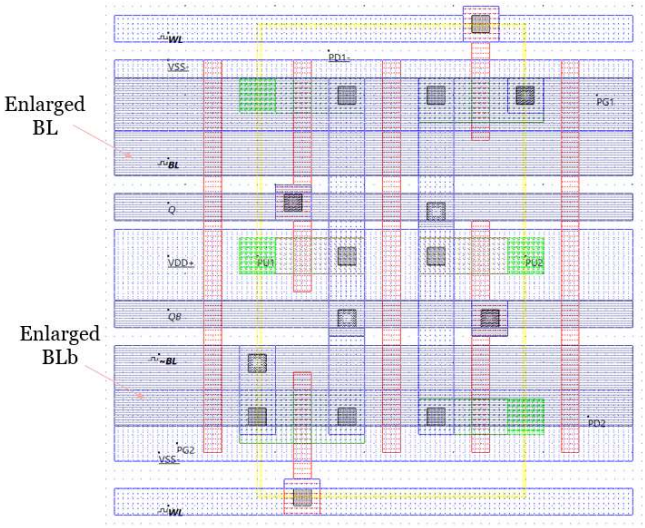


Figure 44: Proposed implementation of the 6T-SRAM with enlarged BL and BLb (SRAM-6T-2nm.MSK).

Conclusion

This application note describes the implementation of the 2-nm/20A technology in the educational tool Microwind, which the introduction of buried power rails and nano-Through-Silicon-Vias. In this paper, we discussed the NSFET characteristics, the performance tradeoff, the interconnect parasitic effects and the performances of basic cells such as logic gates, ring oscillators and memory cells.

Although limited gains are observed in terms of geometrical scale down, the NSFET efficiency—combined with back-side power delivery using BPR—leads to significant gains in terms of silicon area and the shrinkage of the logic cell height. Further improvements are forecast by introducing stacked P-FET and N-FET—also called Complementary FET (C-FET)—in future technology nodes [Sicard & Trojman 2023].

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