Rev. 1.0 Jan. 2018

MZQLB960HAJR-00007
MZQLB1T9HAJR-00007
MZQLB3T8HALS-00007
MZQLB7T6HMLA-00007

2.5"NVMe PCIe SSD Specification (PM983)

datasheet

SAMSUNG

Revision History

Revision No.	History	Draft Date	Remark	Editor by	Review by
1.0	1. Initial issue.	Jan. 08, 2018	Final	H.I. Choi	Y.H. Kim

Part Number	Capacity[1)]	LBA (512 Bytes size)
MZQLB960HAJR-00007	960GB	1,875,385,008
MZQLB1T9HAJR-00007	1.92TB	3,750,748,848
MZQLB3T8HALS-00007	3.84TB	7,501,476,528
MZQLB7T6HMLA-00007	7.68TB	15,002,931,888

FEATURES

· PCI Express Gen3
  - Single port X4 lanes
· Compliant with PCI Express CEM Specification Rev. 3.0
. Compliant with PCI Express Base Specification Rev. 3.1
· Compliant with NVM Express Specification Rev. 1.2a
· Enhanced Power-Loss Data Protection
· End-to-End Data Protection
· Support SSD Enhanced S.M.A.R.T. Feature Set
· Hardware based AES-XTS 256-bit Encryption Engine
· Static and Dynamic Wear Leveling
· RoHS / Halogen-Free Compliant
. TCG Opal Compliant

DRIVE CONFIGURATION

· Form Factor	2.5"
· Interface	PCI Express Gen3 x4
· Bytes per Sector	512, 4096 Bytes

PERFORMANCE SPECIFICATIONS[2)]

· Data Transfer Rate (128KB data size)

- Sequential Read	(7.68TB) Up to TBD MB/s[3]
	(3.84/1.92TB/960GB) Up to 3000 MB/s[3]
- Sequential Write	(7.68TB) Up to TBD MB/s[3]
	(3.84/1.92TB) Up to 1900 MB/s[3]
	(960GB) Up to 1050 MB/s[3]

· Data I/O Speed (4KB data size, Sustained)

- Random Read	(7.68TB) Up to TBDK IOPS
	(3.84/1.92TB) Up to 540K IOPS
	(960GB) Up to 400K IOPS
- Random Write	(7.68TB) Up to TBDK IOPS
	(3.84/1.92TB) Up to 50K IOPS
	(960GB) Up to 40K IOPS

· Latency (Sustained workload)

- Random Read/ Write (typical)[4]	(7.68TB) TBD us
	(3.84/1.92TB/960GB) 85/50 us
- Sequential Read/ Write (typical)[5]	(7.68TB) TBD us
	(3.84/1.92TB/960GB)15/15 us
- Drive Ready Time (typical)	(7.68TB) TBD s
	(3.84/1.92TB/960GB) 10 s

RELIABILITY SPECIFICATIONS

· Uncorrectable Bit Error Rate	1 sector per 10^{17} bits read
· MTBF	2,000,000 hours
· Component Design Life	3 years
· Endurance	
- 3.84/1.92TB/960GB	1.3 DWPD
· TBW (@4KB Random Write)	
- 3.84TB	5466 TB
- 1.92TB	2733 TB
- 960GB	1366 TB
· Data Retention	3 months

ENVIRONMENTAL SPECIFICATIONS

· Temperature, Case (Tc[6])	
- Operating	0 ~ 70 °C
- Non-operating	-40 ~ 85 °C
· Humidity (non-condensing)	5 ~ 95%
· Linear Shock (0.5ms duration with 1/2 sine wave)	
- Non-operating	1,500 G
· Vibration	
- Non-operating (10 ~ 2,000 Hz, Sinusoidal)	20 G

POWER REQUIREMENTS

· Supply Voltage / Tolerance	12V±8%
· Active[7] (max. RMS)	10.6 W
· Idle (typ.)	4.0 W

PHYSICAL DIMENSION

· Width	69.85 ± 0.25 mm
· Length	100.20 ± 0.25 mm
· Height	6.80 ± 0.20 mmT
· Weight	Up to 70 g

OPERATING SYSTEMS

Windows Server 2012R2/2016
RHEL 6.6/7.2
CentOS 6.7/7.3
Ubuntu 14.10/15.10
SLES 11SP3/12
Oracle Linux 6.6/7.2

NOTE: *Specifications are subject to change without notice.*

1) 1MB = 1,000,000 Bytes, 1GB = 1,000,000,000 Bytes, unformatted Capacity. User accessible capacity may vary depending on operating environment and formatting.
2) Based on PCI Express Gen3 x4, Random performance measured using FIO 2.1.3 in Linux RHEL 6.6(Kernel 3.14.29) with 4KB (4,096 bytes) of data transfer size in queue depth 32 by 4 workers and Sequential performance with 128KB (131,072 bytes) of data transfer size in queue depth 32 by 1 worker. Actual performance may vary depending on use conditions and environment.
3) 1 MB/sec = 1,000,000 bytes/sec was used in sequential performance.
4) The random latency is measured by using FIO 2.1.3 in Linux RHEL 6.6(Kernel 3.14.29) and 4KB (4,096 bytes) transfer size with queue depth 1 by 1 worker.
5) The Sequential latency is measured by using FIO 2.1.3 in Linux RHEL 6.6(Kernel 3.14.29) and 4KB (4,096 bytes) transfer size with queue depth 1 by 1 worker.
6) Tc is measured at the hottest point on the case. Sufficient airflow is recommended to be operated properly on heavier workloads wthin device operating temperature.
7) Active power is measured using IOMeter2006 on Windows Server 2012.

Table Of Contents

1.0 Introduction

1.1 General Description

This document describes the specifications of the Samsung SSD PM983, which is a native-PCIe SSD for enterprise application.

The Samsung SSD PM983 presents outstanding performance with instant responsiveness to the host system, by applying the Peripheral Component Interconnect Express (PCIe) 3.0 interface standard, as well as highly efficient Non-Volatile Memory Express (NVMe) Protocol.

The Samsung SSD PM983 delivers wide bandwidth of up to 3,000MB/s for sequential read speed and up to 1,900MB/s for sequential write speed under up to 10.6W power. With the help of Toggle 2.0 NAND Flash interface, the Samsung SSD PM983 delivers random performance of up to 540KIOPS for random 4KB read and up to 50KIOPS for random 4KB write in the sustained state.

By combining the enhanced reliability Samsung NAND Flash memory silicon with NAND Flash management technologies, the Samsung SSD PM983 delivers the extended endurance of up to 1.3 drive writes per day over 3 years, which is suitable for enterprise applications, in 2.5" form factor lineups: 960GB, 1.92TB, 3.84TB and 7.68TB.

In addition, the Samsung SSD PM983 supports Power Loss Protection (PLP). PLP solution can guarantee that data issued by the host system are written to the storage media without any loss in the event of sudden power off or sudden power failure.

1.2 Product List

[Table 1] Product List

Type	Capacity	Part Number
2.5"[1)]	960GB	MZQLB960HAJR-00007
	1.92TB	MZQLB1T9HAJR-00007
	3.84TB	MZQLB3T8HALS-00007
	7.68TB	MZQLB7T6HMLA-00007

NOTE:
1) 69.85 ± 0.25 x 100.20 ± 0.25 x 6.80 ± 0.20

1.3 Ordering Information

M Z X X X X X X X X X X - X X X X X

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Memory (M)

2. Module Classification
Z: SSD

3. Form Factor
Q: PCIe2.5 inch 7mmt

4. Line-Up
L: Client/SV (VNAND 3bit MLC)

5. SSD CTRL
B: Phoenix,S.LSI

6~8. SSD Density
960: 960GB
1T9: 1.92TB
3T8: 3.84TB
7T6: 7.68TB

9. NAND PKG + NAND Voltage
H: BGA (LF,HF)

10. Flash Generation
M: 1st Generation
A: 2st Generation

11~12. NAND Density
JR: 2T ODP 2CE
LS: 4T HDP 2CE(FBI)
LA: 8T HDP 2CE(FBI)

13. "-"

14. Default
"0"

15. HW revision
0: No revision

16. Packaging type
0: Bulk

17~18. Customer
07: General TCG

2.0 PRODUCT SPECIFICATIONS

2.1 Capacity

[Table 2] User Capacity and Addressable Sectors

Capacity[2)]	Max LBA[3)]
960GB	1,875,385,008
1.92TB	3,750,748,848
3.84TB	7,501,476,528
7.68TB	15,002,931,888

NOTE:
1) Gigabyte (GB) = 1,000,000,000 Bytes, 1 Sector = 512Bytes
2) Capacity shown in Table 1 represents the total usable capacity of the SSD which may be less than the total physical capacity. A certain area in physical capacity, not in the area shown to the user, might be used for the purpose of NAND flash management.
3) Max. LBA shown in Table 1 represents the total user addressable sectors in LBA mode and calculated by IDEMA rule.

2.2 Performance

[Table 3] Sustained Random Read/Write Performance (IOPS)

Maximum Performance[1)]	Unit	960GB	1.92TB	3.84TB	7.68TB
Random 4KB Read (Up to)	IOPS	400K	540K	540K	TBD
Random 4KB Write (Up to)	IOPS	40K	50K	50K	TBD

NOTE:
1) Random performance in Table 3 was measured by using FIO 2.1.3 in Linux RHEL 6.5 with 4KB (4,096 bytes) of data transfer size in Queue Depth=32 by 4 workers. Measurements were performed on a full Logical Block Address (LBA) span of the drive in sustained state. The actual performance may vary depending on use conditions and environment.

[Table 4] Sequential Read/Write Performance

Maximum Performance[1)]	Unit	960GB	1.92TB	3.84TB	7.68TB
Sequential 128KB Read (Up to)	MB/s	3,000	3,000	3,000	TBD
Sequential 128KB Write (Up to)	MB/s	1,050	1,900	1,900	TBD

NOTE:
1)Sequential performance in Table 4 was measured by using FIO 2.1.3 in Linux RHEL 6.5 with 128KB (131,072 bytes) of data transfer size in Queue Depth=32 by 1 worker.

[Table 5] IOPS Consistency

Maximum Performance[1)]	960GB	1.92TB	3.84TB	7.68TB
Random Read (4 KB)	99%	99%	99%	TBD
Random Write (4 KB)	96%	95%	97%	TBD

NOTE:
1) IOPS consistency measured using FIO with queue depth 32.
2) IOPS Consistency (%) = (99.9% IOPS) / (Average IOPS) x 100.

2.3 Latency

[Table 6] Latency[1] (sustained state)

Queue Depth = 1	Unit	960GB	1.92TB	3.84TB	7.68TB
Random Read/Write[2]	us	85 / 50	85 / 50	85 / 50	TBD
Sequential Read/Write[3]	us	15 / 15	15 / 15	15 / 15	TBD
Drive Ready Time[4]	sec	10	10	10	TBD

NOTE:
1) Typical values
2) The random latency is measured by using FIO 2.1.3 in Linux RHEL 7.0(Kernel 3.10.0) and 4KB transfer size with queue depth 1 by 1 worker.
3) The sequential latency is measured by using FIO 2.1.3 in Linux RHEL 7.0(Kernel 3.10.0) and 4KB transfer size with queue depth 1 by 1 worker.
4) The maximum taking time to be ready for receiving commands after power-up (CSTS.Ready=1). It is expected that I/O commands may not be completed at this point.

2.4 Quality of Service (QoS)

[Table 7] Quality of Service (QoS)

Quality of Service (99%)	Unit	QD=1	QD=32
Read(4KB)	ms	0.1	0.3
Write(4KB)	ms	0.06	1.5

Quality of Service (99.99%)	Unit	QD=1	QD=32
Read(4KB)	ms	0.2	0.6
Write(4KB)	ms	0.09	1.5

NOTE:
1. QoS is measured using Fio 2.1.3 (99 and 99.99%) in Linux RHEL 7.0(Kernel 3.10.0) with queue depth 1, 32 on 4KB random read and write.
2. QoS is measured as the maximum round-trip time taken for 99 and 99.99% of commands to host.

2.5 Power

The Samsung SSD PM983 is implemented in standardized 2.5" form factor and gets primary 12V power t from the host system.
For 12V, the allowable voltage tolerance and noise level in SSD are described in chapter 2.4.1, the power consumption in 2.4.2 and the inrush current in 2.4.3.

2.5.1 Maximum Voltage Ratings (12V)

[Table 8] Allowable Voltage Tolerance[1]

Operating Voltage	960GB	1.92TB	3.84TB	7.68TB
Allowable Voltage	12V±8%			
Allowable noise/ripple	DC to 100Khz : 960 mVp-p Max 100Khz to 20Mhz : 150 mVp-p Max			

NOTE:
1) The components inside SSD were designed to endure the range of voltage fluctuations, which might be induced by the host system, in Table 6.

2.5.2 Power Consumption (12V)

In enterprise server and storage system, the Samsung SSD PM983 is designed for the specific usage, which means that SSD will be always operated by the host system during the entire life. Hence, the Samsung SSD PM983 does not manage any low power modes except for the Active/Idle and Off mode.

[Table 9] Power Consumption (12V Supply Voltage)[1]

Power Mode		960GB	1.92TB	3.84TB	7.68TB
Active[2]	Read	8.6W	8.7W	8.7W	TBD
	Write	8.1W	10.6W	10.6W	TBD
Idle[3]		4.0W	4.0W	4.0W	TBD
Off		0W	0W	0W	0W

NOTE:
1) Power consumption was measured in the 12V power pins of the connector plug in SSD. The active and idle power is defined as the highest averaged power value, which is the maximum RMS average value over 100 ms duration.
2) The measurement condition for active power is assumed for 100% sequential read and write.
3) The idle state is defined as the state that the host system can issue any commands into SSD at any time.

2.5.3 Inrush Current

[Table 10] Inrush Current

Inrush Current	960GB	1.92TB	3.84TB	7.68TB
12V	1.5A[1]			

NOTE:
1) The measurement value of inrush current is also compatible with the standard specification of “Enterprise SSD Form Factor Version 1.0a” released by SSD Form Factor Working Group

2.5.4 Power Loss Protection

By using internal back-up power technology, the Samsung SSD PM983 supports power loss protection (PLP) feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

2.6 Reliability

The reliability specification of the Samsung SSD PM983 follows JEDEC standard, which are included in JESD218A and JESD219A documents

2.6.1 Mean Time Between Failures

By definition, Mean Time between Failures (MTBF) is the estimated time between failures occurring during SSD operation.

[Table 11] MTBF Specifications

Parameter	960GB	1.92TB	3.84TB	7.68TB(target)
MTBF	2,000,000 Hours			

2.6.2 Uncorrectable Bit Error Rate

By definition, Uncorrectable Bit Error Rate (UBER) is a metric for the rate of occurrence of data errors, equal to the number of data errors per bits read as specified in the JESD218 document of JEDEC standard.

[Table 12] UBER Specifications

Parameter	960GB	1.92TB	3.84TB	7.68TB(target)
UBER	1 sector per 10^{17} bits read			

2.6.3 Data Retention

By definition, data retention is the expected time period for retaining data in the SSD at the maximum rated endurance in power-off state as specified in the JESD218 document of JEDEC standard.

[Table 13] Data Retention

Parameter	960GB	1.92TB	3.84TB	7.68TB(target)
Data Retention[1]	3 months			

NOTE:
1) Data retention was measured by assuming that SSD reaches the maximum rated endurance at 40C in power-off state.

2.6.4 Endurance

By definition, the endurance of SSD in enterprise application is defined as the maximum number of drive writes per day that can meet the requirements specified in the JESD218 document of JEDEC standard.

[Table 14] Drive Write Per Day (DWPD)

Parameter	960GB	1.92TB	3.84TB	7.68TB(target)
DWPD	1.3 drive writes per day over 3 years			

[Table 15] TBW (Tera Bytes Written) Specifications

Parameter	Unit	960GB	1.92TB	3.84TB	7.68TB(target)
TBW	TB	1366	2733	5466	10932

2.7 Environmental Specification

2.7.1 Temperature

[Table 16] Temperature, Case (Tc[1])

Parameter		960GB	1.92TB	3.84TB	7.68TB
Temperature[1]	Operating	0 to 70°C			
	Non-operating	-40 to 85°C			

NOTE:
1) Tc is measured at the hottest point on the case. Sufficient airflow is recommended to be operated properly on heavier workloads wthin device operating temperature.

2.7.2 Humidity

[Table 17] Humidity

Parameter		960GB	1.92TB	3.84TB	7.68TB
Humidity[1]	Non-operating	5% to 95%			

NOTE:
1) Humidity is measured in non-condensing state.

2.7.3 Shock and Vibration

[Table 18] Shock and Vibration

Parameter		960GB	1.92TB	3.84TB	7.68TB
Shock[1]	Non-operating	1,500 G			
Vibration[2]	Non-operating	20 G			

NOTE:
1) Test condition for shock: 0.5ms duration with half sine wave.
2) Test condition for vibration: 10Hz to 2000Hz.

3.0 Mechanical Specifications

3.1 Physical Information

The physical case of the Samsung SSD PM983 in 2.5 form factor follows the standardized dimensions defined by SSD Form Factor Work Group.

[Table 19] Physical Dimensions and Weight

Parameter	Unit	960GB	1.92TB	3.84TB	7.68TB
Width	mm	69.85 ± 0.25			
Length	mm	100.20 ± 0.25			
Thickness	mm	6.80 ± 0.20			
Weight	g	Up to 70g			

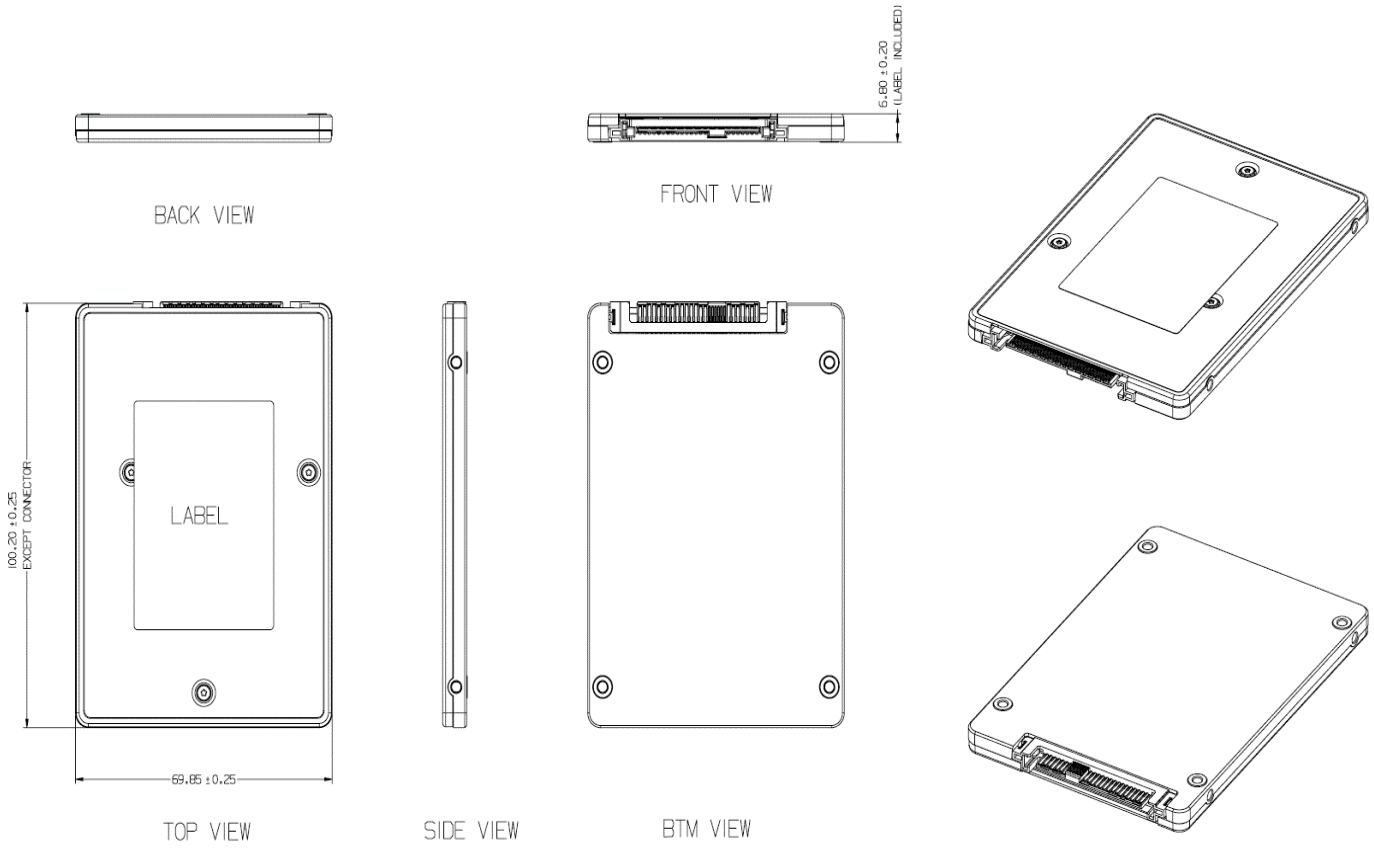
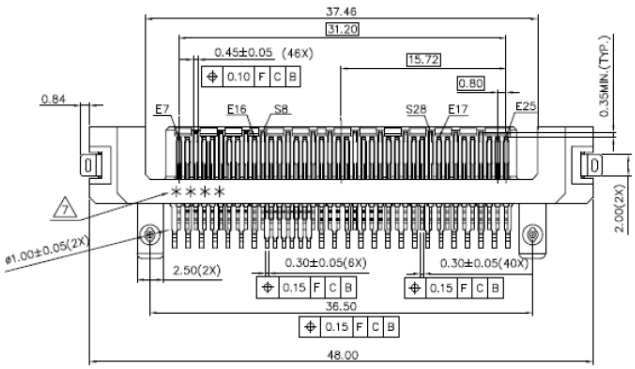


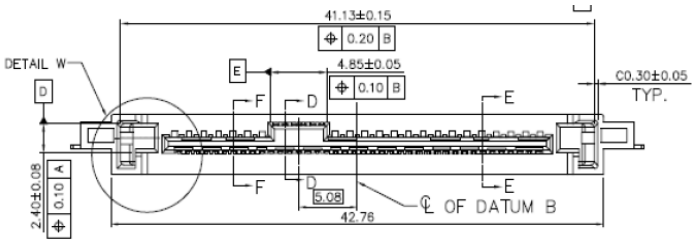
Figure 1. Mechanical Outline

4.0 Interface Specification

4.1 Connector Dimensions

Drive Connector: FOXCONN





4.2 Connector Pin Assignments

[Table 20] Certifications and Declarations

Pin #	Assignment	Description	Pin #	Assignment	Description
S1	GND	Ground	E7	RefClk0+	PCIe Reference Clock +
S2	Not Used	Floated	E8	RefClk0-	PCIe Reference Clock -
S3	Not Used		E9	GND	Ground
S4	GND	Ground	E10	PETp0	PCIe Transmit+ (lane 0)
S5	Not Used		E11	PETn0	PCIe Transmit- (lane 0)
S6	Not Used		E12	GND	Ground
S7	GND	Ground	E13	PERn0	PCIe Receive- (lane 0)
E1	REFCLK1+	Grounded	E14	PERp0	PCIe Receive+ (lane 0)
E2	REFCLK1-	Grounded	E15	GND	Ground
E3	3.3V AUX		E16	Not Used	
E4	ePERST1#	Floated	S8	GND	Ground
E5	ePERST0#		S9	Not Used	
E6	RSVD		S10	Not Used	
P1	Not Used		S11	GND	Ground
P2	Not Used		S12	Not Used	
P3	Not Used		S13	Not Used	
P4	IfDet #	Grounded	S14	GND	Ground
P5	GND	Ground	S15	Not Used	
P6	GND	Ground	S16	GND	Ground
P7	Not Used		S17	PETp1	PCIe Transmit+ (lane 1)
P8	Not Used		S18	PETn1	PCIe Transmit- (lane 1)
P9	Not Used		S19	GND	Ground
P10	PRSNT #	Presence	S20	PERn1	PCIe Receive- (lane 1)
P11	Activity	Drive Active	S21	PERp1	PCIe Receive+ (lane 1)
P12	GND	Ground	S22	GND	Ground
P13	12 V	Primary Power	S23	PETp2	PCIe Transmit+ (lane 2)
P14	12 V	Primary Power	S24	PETn2	PCIe Transmit- (lane 2)
P15	12 V	Primary Power	S25	GND	Ground
			S26	PERn2	PCIe Receive- (lane 2)

			S27	PERp2	PCIe Receive+ (lane 2)
			S28	GND	Ground
			E17	PETp3	PCIe Transmit+ (lane 3)
			E18	PETn3	PCIe Transmit- (lane 3)
			E19	GND	Ground
			E20	PERn3	PCIe Receive- (lane 3)
			E21	PERp3	PCIe Receive+ (lane 3)
			E22	GND	Ground
			E23	SMClk	SMBus Clock
			E24	SMDat	SMBus Data
			E25	DualPortEn#	

5.0 PCI and NVM Express Registers

5.1 PCI Express Registers

5.1.1 PCI Register Summary

[Table 21] PCI Register Summary

Start Address	End Address	Name	Type
00h	3Fh	PCI Header	PCI Capability
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting Capability	PCI Capability
148h	153h	Device Serial No Capability	PCI Capability
158h	167h	Power Budgeting Capability	PCI Capability
168h	17Bh	Secondary PCI Express Header	PCI Capability
188h	18Fh	Latency Tolerance Reporting (LTR)	PCI Capability
190h	19Fh	L1 Substates Capability Register	PCI Capability

5.1.2 PCI Header Registers

[Table 22] PCI Header Register Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)
14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Index/Data Pair Register Base Address
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	RO	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

[Table 23] Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A808h	Device ID
0:15	RO	144Dh	Vendor ID

[Table 24] Command Register

Bits	Type	Default Value	Description
15:11	RO	0h	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back Enable (N/A)
8	RW	0	SERR# Enable (N/A)
7	RO	0	IDSEL Stepping/Wait Cycle Control (N/A)
6	RW	0	Parity Error Response Enable
5	RO	0	VGA Palette Snooping Enable (N/A)
4	RO	0	Memory Write and Invalidate Enable (N/A)
3	RO	0	Special Cycle Enable (N/A)
2	RW	0	Bus Master Enable
1	RW	0	Memory Space Enable
0	RW	0	I/O Space Enable

[Table 25] Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Detected Parity Error
14	RW1C	0	Signaled System Error
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort (N/A)
10:9	RO	0h	DEVSEL Timing (N/A)
8	RW1C	0	Master Data Parity Error Detected
7	RO	0	Fast Back-to-Back Transaction Capable (N/A)
6	RsvdP	0	Reserved
5	RO	0	66MHz Capable (N/A)
4	RO	1	Capabilities List
3	RO	0	Interrupt Status
2:1	RO	0h	Reserved
0	RO	0	Reserved

[Table 26] Revision ID Register

Bits	Type	Default Value	Description
7:0	RO	00h	Controller Hardware Revision ID

[Table 27] Class Code Register

Bits	Type	Default Value	Description
23:16	RO	01h	Base Class Code
15:8	RO	08h	Sub Class Code
7:0	RO	02h	Programming Interface

[Table 28] Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0h	Cache Line Size (N/A)

[Table 29] Master Latency Timer Register

Bits	Type	Default Value	Description
7:0	RO	0h	Master Latency Timer (N/A)

[Table 30] Header Type Register

Bits	Type	Default Value	Description
7	RO	0	Multi-Function Device (N/A)
6:0	RO	0h	Reserved

[Table 31] Built In Self Test Register

Bits	Type	Default Value	Description
7:0	RO	0h	Built In Self Test (N/A)

[Table 32] Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:14	RW	0h	Base Address
13:4	RO	0h	Reserved
3	RO	0	Pre-Fetchable
2:1	RO	2h	Address Type (64-bit)
0	RO	0	Memory Space Indicator (MEMSI)

[Table 33] Memory Register Base Address Upper 32-bits (BAR1)

Bits	Type	Default Value	Description
31:0	RO	0h	Base Address

[Table 34] Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 35] BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 36] Vendor Specific BAR4 Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 37] Vendor Specific BAR5 Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 38] Cardbus CIS Pointer Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

[Table 39] Subsystem Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A801h	Subsystem ID
15:0	RO	144Dh	Subsystem Vendor ID

[Table 40] Expansion ROM Register

Bits	Type	Default Value	Description
31:17	RW	0h	Expansion ROM Base Address
16:1	RO	0h	Reserved
0	RW	0	Expansion ROM Enable/Disable

[Table 41] Capabilities Pointer Register

Bits	Type	Default Value	Description
7:0	RO	40h	Capability Pointer (Points to PCI Power Management Capability Offset)

[Table 42] Interrupt Information Register

Bits	Type	Default Value	Description
15:8	RO	01h	Interrupt Pin
7:0	RW	FFh	Interrupt Line

[Table 43] Minimum Grant Register

Bits	Type	Default Value	Description
7:0	RO	0h	Minimum Grant

[Table 44] Maximum Latency Register

Bits	Type	Default Value	Description
7:0	RO	0h	Maximum Latency

5.1.3 PCI Power Management Registers

[Table 45] PCI Power Management Capability Register Summary

Start Address	End Address	Symbol	Description
40h	40h	PCIPM_ID	PCI Power Management Capability ID
41h	41h	NEXTCAP	Next Capability Pointer
42h	43h	PCIPM_CAP	PC Power Management Capabilities
44h	45h	PCIPM_CS	PCI Power Management Control and Status
46h	46h	PCIPM_CSR_BSE	PMCSR_BSE Bridge Extensions
47h	47h	PCIEPM_DATA	Data

[Table 46] PCI Power Management Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	50h	Next Capability
7:0	RO	1h	Capability ID

[Table 47] PCI Power Management Capability Register

Bits	Type	Default Value	Description
15:11	RO	0h	PME Support (N/A)
10	RO	0	D2 Support (N/A)
9	RO	0	D1 Support (N/A)
8:6	RO	0h	AUX Current (N/A)
5	RO	0	Device Specific Initialization (N/A)
4	RsvdP	0	Reserved
3	RO	0	PME Clock (N/A)
2:0	RO	3h	Version (Support for PCI Bus Power Management Interface Spec R1.2)

[Table 48] PCI Power Management Control and Status Register

Bits	Type	Default Value	Description
31:24	RsvdP	0h	Data register (N/A)
23	RO	0	Bus Power/Clock Enable (N/A)
22	RO	0	B2 , B3 support (N/A)
21:16	RsvdP	0h	Reserved
15	RO	0	PME_Status (N/A)
14:13	RO	0h	Data Scale (N/A)
12:9	RO	0h	Data Select (N/A)
8	RWS	0	PME enable (N/A)
7:4	RsvdP	0h	Reserved
3	RO	1	No Soft Reset
2	RsvdP	0	Reserved
1:0	RW	0h	Power State

5.1.4 Message Signaled Interrupt Registers

[Table 49] Message Signaled Interrupt Capability Register Summary

Start Address	End Address	Symbol	Description
50h	51h	MSI_ID	Message Signaled Interrupt Capability ID
52h	53h	MSI_MC	Message Signaled Interrupt Message Control
54h	57h	MSI_MA	Message Signaled Interrupt Message Address
58h	5Bh	MSI_MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MSI_MDATA	Message Signaled Interrupt Message Data
60h	63h	MSI_MMASK	Message Signaled Interrupt Mask Bits
64h	67h	MSI_MPEND	Message Signaled Interrupt Pending Bits

[Table 50] Message Signaled Interrupt Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	70h	Next Capability
7:0	RO	05h	Capability ID

[Table 51] Message Signaled Interrupt Control Register

Bits	Type	Default Value	Description
15:9	RsvdP	0h	Reserved
8	RO	0	Per Vector Masking Capable (N/A)
7	RO	1h	64-bit Address Capable
6:4	RW	0h	Multiple Message Enable
3:1	RO	5h	Multiple Message Capable
0	RW	0	MSI Enable

[Table 52] Message Signaled Interrupt Lower Address Register

Bits	Type	Default Value	Description
31:2	RW	0h	Address
1:0	RO	0h	Reserved

[Table 53] Message Signaled Interrupt Upper Address Register

Bits	Type	Default Value	Description
31:0	RW	0h	Upper Address

[Table 54] Message Signaled Interrupt Message Data Register

Bits	Type	Default Value	Description
31:16	RsvdP	0h	Reserved
0:15	RW	0h	Data

[Table 55] Message Signaled Interrupt Mask Bits Register

Bits	Type	Default Value	Description
31:0	RW	0h	Mask Bits

[Table 56] Message Signaled Interrupt Pending Bits Register

Bits	Type	Default Value	Description
31:0	RO	0h	Pending Bits

5.1.5 MSI-X Registers

[Table 57] MSI-X Capability Register Summary

Start Address	End Address	Symbol	Description
B0h	B1h	MSIX_ID	MSI-X Capability ID
B2h	B3h	MSIX_CAP	MSI-X Message Control
B4h	B7h	MSIX_TBL	MSI-X Table Offset and Table BIR
B8h	BBh	MSIX_PBA	MSI-X PBA Offset and PBA BIR

[Table 58] MSI-X Identifier Register

Bits	Type	Default Value	Description
15:8	RO	00h	Next Capability
7:0	RO	11h	Capability ID

[Table 59] MSI-X Control Register

Bits	Type	Default Value	Description
15	RW	0	MSI-X Enable
14	RW	0	Function Mask
13:11	RsvdP	0h	Reserved
10:0	RO	20h	Table Size

[Table 60] MSI-X Table Offset Register

Bits	Type	Default Value	Description
31:3	RO	600h	Table Offset
2:0	RO	0	Table BIR

[Table 61] MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value	Description
31:3	RO	400h	Pending Bit Array Offset
2:0	RO	0	Pending Bit Array BIR

5.1.6 PCI Express Capability Registers

[Table 62] PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
70h	71h	PCIE_ID	PCI Express Capability ID
72h	73h	PCIE_CAP	PCI Express Capabilities
74h	77h	PCIE_DCAP	PCI Express Device Capabilities
78h	79h	PCIE_DC	PCI Express Device Control
7Ah	7Bh	PCIE_DS	PCI Express Device Status
7Ch	7Fh	PCIE_LCAP	PCI Express Link Capabilities
80h	81h	PCIE_LC	PCI Express Link Control
82h	83h	PCIE_LS	PCI Express Link Status
94h	97h	PCIE_DCAP2	PCI Express Device Capabilities 2
98h	99h	PCIE_DC2	PCI Express Device Control 2
9Ah	9Bh	PCIE_DS2	PCI Express Device Status 2
9Ch	9Fh	PCIE_LCAP2	PCI Express Link Capabilities 2
A0h	A1h	PCIE_LC2	PCI Express Link Control 2
A2h	A3h	PCIE_LS2	PCI Express Link Status 2

[Table 63] PCI Express Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	B0h	Next Pointer (MSI-X Capability)
7:0	RO	10h	Capability ID

[Table 64] PCI Express Capabilities Register

Bits	Type	Default Value	Description
15:14	RsvdP	0h	Reserved
13:9	RO	0h	Interrupt Message Number
8	HwInit	0	Slot Implementation (N/A)
7:4	RO	0h	Device/Port Type
3:0	RO	2h	Capability Version

[Table 65] PCI Express Device Capabilities Register

Bits	Type	Default Value	Description
31:29	RsvdP	0h	Reserved
28	RO	1	Function Level Reset Capability
27:26	RO	0h	Captured Slot Power Limit Scale
25:18	RO	0h	Captured Slot Power Limit Value
17:16	RsvdP	0h	Reserved
15	RO	1	Role-based Error Reporting
14:12	RO	0h	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	0	Extended Tag Field Supported
4:3	RO	0h	Phantom Functions Supported
2:0	RO	1h	Max Payload Size Supported (256 byte payload)

[Table 66] PCI Express Device Control Register

Bits	Type	Default Value	Description
15	RW	0	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	1	Enable No Snoop
10	RWS	0	Aux Power PM Enable (N/A)
9	RW	0	Phantom Functions Enable (N/A)
8	RW	0	Extended Tag Enable
7:5	RW	0h	Max Payload Size
4	RW	1	Enable Relaxed Ordering
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

[Table 67] PCI Express Device Status Register

Bits	Type	Default Value	Description
15:6	RsvdZ	0h	Reserved
5	RO	0	Transactions Pending
4	RO	0	Aux Power Detected
3	RW1C	0	Unsupported Request Detected
2	RW1C	0	Fatal Error Detected
1	RW1C	0	Non-Fatal Error Detected
0	RW1C	0	Correctable Error Detected

[Table 68] PCI Express Link Capabilities Register

Bits	Type	Default Value	Description
31:24	HwInit	0 (Port 0)	Port Number
23	RsvdP	0	Reserved
22	HwInit	1	ASPM Optionality Compliance
21	RO	0	Link Bandwidth Notification Capability (N/A)
20	RO	0	Data Link Layer Link Active Reporting Capable (N/A)
19	RO	0	Surprise Down Error Reporting Capable (N/A)
18	RO	1	Clock Power Management
17:15	RO	6h	L1 Exit Latency
14:12	RO	7h	L0s Exit Latency
11:10	RO	2h	Active State Power Management Support
9:4	RO	4h (x4 link)	Maximum Link Width
3:0	RO	3h	Supported Link Speeds

[Table 69] PCI Express Link Control Register

Bits	Type	Default Value	Description
15:14	RW/RsvdP	0h	Reserved
13:12	RsvdP	0h	Reserved
11	RsvdP	0	Link Autonomous Bandwidth Interrupt Enable (N/A)
10	RsvdP	0	Link Bandwidth Management Interrupt Enable (N/A)
9	RsvdP	0	Hardware Autonomous Width Disable
8	RW	0	Enable Clock Power Management
7	RW	0	Extended Sync
6	RW	0	Common Clock Configuration
5	RsvdP	0	Retrain Link (N/A)
4	RsvdP	0	Link Disable (N/A)
3	RW	0	Read Completion Boundary (N/A)
2	RsvdP	0	Reserved
1:0	RW	0h	Active State Power Management Control

[Table 70] PCI Express Link Status Register

Bits	Type	Default Value	Description
15	RW1C	0h	Link Autonomous Bandwidth Status (N/A)
14	RW1C	0	Link Bandwidth Management Status (N/A)
13	RO	0	Data Link Layer Link Active
12	HwInit	1	Slot Clock Configuration
11	RO	0	Link Training (N/A)
10	RO	0	Reserved
9:4	RO	1h	Negotiated Link Width
3:0	RO	1h	Current Link Speed

[Table 71] PCI Express Device Capabilities 2 Register

Bits	Type	Default Value	Description
31	HwInit	0	FRS Supported (N/A)
30:24	RsvdP	0h	Reserved
23:22	HwInit	0h	Max End-End TLP Prefixes (N/A)
21	HwInit	0	End-End TLP Prefix Supported (N/A)
20	RO	0	Extended Format Field Supported (N/A)
19:18	HwInit	0h	OBFF Supported (N/A)
17:16	RsvdP	0h	Reserved
15:14	HwInit	0h	LN System CLS (N/A)
13:12	RO	0h	TPH Completer Supported (N/A)
11	RO	1	Latency Tolerance Reporting Supported
10	HwInit	0	No RO-enabled PR-PR Passing (N/A)
9	RO	0	128-bit CAS Completer Supported (N/A)
8	RO	0	64-bit Atomic Op Completer Supported (N/A)
7	RO	0	32-bit Atomic Op Completer Supported (N/A)
6	RO	0	Atomic Op Routing Supported (N/A)
5	RO	0	ARI Forwarding Supported (N/A)
4	RO	1	Completion Timeout Disable Supported
3:0	HwInit	Fh	Completion Timeout Ranges Supported

[Table 72] PCI Express Device Control 2 Register

Bits	Type	Default Value	Description
15	RsvdP	0	End-to-end TLP Prefix Blocking (N/A)
14:13	RW/RsvdP	0h	OBFF Enable (N/A)
12:11	RsvdP	0h	Reserved
10	RW	0	Latency Tolerance Reporting Mechanism Enable
9	RW	0	IDO Completion Enable (N/A)
8	RW	0	IDO Request Enable (N/A)
7	RW	0	AtomicOp Egress Blocking (N/A)
6	RW	0	AtomicOp Requester Enable (N/A)
5	RW	0	ARI Forwarding Enable (N/A)
4	RW	0	Completion Timeout Disable
3:0	RW	0h	Completion Timeout Value

[Table 73] PCI Express Device Status 2 Register

Bits	Type	Default Value	Description
15:0	RsvdZ	0h	Reserved

[Table 74] PCI Express Link Capabilities 2 Register

Bits	Type	Default Value	Description
31:9	RO	0	Reserved
30:24	RsvdP	0h	Reserved
23	HWinit	0	Reserved
22:16	HWinit	0h	Lower SKP OS Reception Supported Speed Vector (N/A)
15:9	HWinit	0h	Lower SKP OS Generation Supported Speed Vector (N/A)
8	RO	0	Cross-Link Supported (N/A)
7:1	RO	7h	Supported Speeds Vector
0	RsvdP	0	Reserved

[Table 75] PCI Express Link Control 2 Register

Bits	Type	Default Value	Description
15:12	RWS/RsvdP	0h	Compliance De-emphasis
11	RWS/RsvdP	0	Compliance SOS
10	RWS/RsvdP	0	Enter Modified Compliance
9:7	RWS/RsvdP	0h	Transmit Margin
6	HwInit	0	Selectable De-Emphasis (N/A)
5	RWS/RsvdP	0	Hardware Autonomous Speed Disable
4	RWS/RsvdP	0	Enter Compliance
3:0	RWS/RsvdP	3h	Target Link Speed 1h: 2.5 GT/s (Gen 1) 2h: 5.0 GT/s (Gen 2) 3h: 8 GT/s (Gen 3) 4h: 16 GT/s(Gen 4)

[Table 76] PCI Express Link Status 2 Register

Bits	Type	Default Value	Description
15:6	RsvdP	0	Reserved
5	RW1CS	0	Link Equalization Request
4	ROS	0	Equalization Phase 3 Successful
3	ROS	0	Equalization Phase 2 Successful
2	ROS	0	Equalization Phase 1 Successful
1	ROS	0	Equalization Complete
0	RO	1	Current De-Emphasis

5.1.7 Advanced Error Reporting Registers

[Table 77] Advanced Error Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
100h	103h	AER_ID	AER Capability ID
104h	107h	AER_UCES	AER Uncorrectable Error Status
108h	10Bh	AER_UCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AER_UCESEV	AER Uncorrectable Error Severity
110h	113h	AER_CES	AER Correctable Error Status
114h	117h	AER_CEM	AER Correctable Error Mask
118h	11Bh	AER_CC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AER_HL	AER Header Log

[Table 78] AER Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	148h	Next Pointer (Points to Secondary PCI Express Extended Capability Header Offset)
19:16	RO	2h	Capability Version
15:0	RO	1h	Capability ID

[Table 79] AER Uncorrectable Error Status Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0h	Reserved
26	RW1CS	0	Poisoned TLP Egress Blocked Status (N/A)
25	RW1CS	0	TLP Prefix Blocked Error Status (N/A)
24	RW1CS	0	Atomic Op Egress Blocked Status (N/A)
23	RW1CS	0	MC Blocked TLP Status (N/A)
22	RW1CS	0	Uncorrectable Internal Error Status (N/A)
21	RW1CS	0	ACS Violation Status (N/A)
20	RW1CS	0	Unsupported Request Error Status
19	RW1CS	0	ECRC Error Status
18	RW1CS	0	Malformed TLP Status
17	RW1CS	0	Receiver Overflow Status
16	RW1CS	0	Unexpected Completion Status
15	RW1CS	0	Completer Abort Status
14	RW1CS	0	Completion Timeout Status
13	RW1CS	0	Flow Control Protocol Error Status
12	RW1CS	0	Poisoned TLP Status
11:6	RsvdZ	0h	Reserved
5	RW1CS	0	Surprise Down Error Status (N/A)
4	RW1CS	0	Data Link Protocol Error Status
3:1	RsvdZ	0h	Reserved
0	Undefined	0	Undefined

[Table 80] AER Uncorrectable Error Mask Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0h	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Mask (N/A)
25	RWS	0	TLP Prefix Blocked Error Mask (N/A)
24	RWS	0	Atomic Op Egress Blocked Mask (N/A)
23	RWS	0	MC Blocked TLP Mask (N/A)
22	RWS	1	Uncorrectable Internal Error Mask
21	RWS	0	ACS Violation Mask (N/A)
20	RWS	0	Unsupported Request Error Mask
19	RWS	0	ECRC Error Mask
18	RWS	0	Malformed TLP Mask
17	RWS	0	Receiver Overflow Mask
16	RWS	0	Unexpected Completion Mask
15	RWS	0	Completer Abort Mask
14	RWS	0	Completion Timeout Mask

13	RWS	0	Flow Control Protocol Error Mask
12	RWS	0	Poisoned TLP Mask
11:6	RsvdZ	0h	Reserved
5	RWS	0	Surprise Down Error Mask (N/A)
4	RWS	0	Data Link Protocol Error Mask
3:1	RsvdZ	0h	Reserved
0	Undefined	0	Undefined

[Table 81] AER Uncorrectable Error Severity Register

Bits	Type	Default Value	Description
31:27	RsvdP	0h	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Severity (N/A)
25	RWS	0	TLP Prefix Blocked Error Severity (N/A)
24	RWS	0	Atomic Op Egress Blocked Severity (N/A)
23	RWS	0	MC Blocked TLP Severity (N/A)
22	RWS	1	Uncorrectable Internal Error Severity (N/A)
21	RWS	0	ACS Violation Severity (N/A)
20	RWS	0	Unsupported Request Error Severity
19	RWS	0	ECRC Error Severity
18	RWS	1	Malformed TLP Severity
17	RWS	1	Receiver Overflow Severity
16	RWS	0	Unexpected Completion Severity
15	RWS	0	Completer Abort Severity
14	RWS	0	Completion Timeout Severity
13	RWS	1	Flow Control Protocol Error Severity
12	RWS	0	Poisoned TLP Severity
11:6	RsvdP	0h	Reserved
5	RWS	1	Surprise Down Error Severity (N/A)
4	RWS	1	Data Link Protocol Error Severity
3:1	RsvdP	0h	Reserved
0	Undefined	0	Undefined

[Table 82] AER Correctable Error Status Register

Bits	Type	Default Value	Description
31:16	RsvdZ	0h	Reserved
15	RW1CS	0	Header Log Overflow Status
14	RW1CS	0	Corrected Internal Error Status
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status
11:9	RsvdZ	0h	Reserved
8	RW1CS	0	Replay Number Rollover Status
7	RW1CS	0	Bad DLLP Status
6	RW1CS	0	Bad TLP Status
5:1	RsvdZ	0h	Reserved
0	RW1CS	0	Received Error Status

[Table 83] AER Correctable Error Mask Register

Bits	Type	Default Value	Description
31:16	RsvdP	0h	Reserved
15	RWS	1	Header Log Overflow Status
14	RWS	1	Corrected Internal Error Mask
13	RWS	1	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask
11:9	RsvdP	0h	Reserved
8	RWS	0	Replay Number Rollover Mask
7	RWS	0	Bad DLLP Mask
6	RWS	0	Bad TLP Mask
5:1	RsvdP	0h	Reserved
0	RWS	0	Received Error Mask

[Table 84] AER Capabilities and Control Register

Bits	Type	Default Value	Description
31:13	RsvdP	0h	Reserved
12	RO	0	Completion Timeout Prefix/Header Log Capable (N/A)
11	ROS	0	TLP Prefix Log Present (N/A)
10	RWS	0	Multiple Header Recording Enable
9	RO	0	Multiple Header Recording Capable
8	RWS	0	ECRC Check Enable
7	RO	1	ECRC Check Capable
6	RWS	0	ECRC Generation Enable
5	RO	1	ECRC Generation Capable
4:0	ROS	0h	First Error Pointer

[Table 85] AER Header Log Register

Bits	Type	Default Value	Description
127:120	ROS	0h	Header Byte 0
119:112	ROS	0h	Header Byte 1
111:104	ROS	0h	Header Byte 2
103:96	ROS	0h	Header Byte 3
95:88	ROS	0h	Header Byte 4
87:80	ROS	0h	Header Byte 5
79:72	ROS	0h	Header Byte 6
71:64	ROS	0h	Header Byte 7
63:56	ROS	0h	Header Byte 8
55:48	ROS	0h	Header Byte 9
47:40	ROS	0h	Header Byte 10
39:32	ROS	0h	Header Byte 11
31:24	ROS	0h	Header Byte 12
23:16	ROS	0h	Header Byte 13
15:8	ROS	0h	Header Byte 14
7:0	ROS	0h	Header Byte 15

[Table 86] Secondary PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
168h	16Bh	SPE_ID	Secondary PCI Express Capability
16Ch	16Fh	PCIE_LC3	PCI Express Link Control 3
170h	173h	PCIE_LE	PCI Express Lane Error Status
174h	175h	PCIE_L0EC	PCI Express Lane 0 Equalization Control
176h	177h	PCIE_L1EC	PCI Express Lane 1 Equalization Control
178h	179h	PCIE_L2EC	PCI Express Lane 2 Equalization Control
17Ah	17Bh	PCIE_L3EC	PCI Express Lane 3 Equalization Control

[Table 87] Secondary PCI Express Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	188h	Next Pointer
19:16	RO	1h	Capability Version
15:0	RO	19h	Capability ID (Secondary PCI Express Extended capability)

[Table 88] PCI Express Link Control 3 Register

Bits	Type	Default Value	Description
31:16	Rsvdp	0h	Reserved
15:9	RW	0h	Enable Lower SKP OS Generation Vector (N/A)
8:2	RsvdP	0h	Reserved
1	Rsvdp	0	Link Equalization Request Interrupt Enable (N/A)
0	Rsvdp	0	Perform Equalization (N/A)

[Table 89] PCI Express Lane Error Status Register

Bits	Type	Default Value	Description
31:4	Rsvdp	0h	Reserved
3:0	RW1CS	0h	Lane Error Status Bits

[Table 90] PCI Express Lane 0 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 91] PCI Express Lane 1 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 92] PCI Express Lane 2 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

[Table 93] PCI Express Lane 3 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

5.1.8 Device Serial Number Capability Register

[Table 94] Device Serial Number Capability Summary

Start Address	End Address	Symbol	Description
148h	14Bh	DSN_ID	Device Serial Number Capability ID
14Ch	14Fh	DSN_LR	Serial Number Register (Lower DW)
150h	153h	DSN_UR	Serial Number Register (Upper DW)

[Table 95] Device Serial Number Capability Register Header

Bits	Type	Default Value	Description
31:20	RO	158h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	3h	PCI Express Extended Capability ID

[Table 96] Serial Number Register Header (Lower DW)

Bits	Type	Default Value	Description
31:0	RO	0h	Serial Number register (Lower DW)

[Table 97] Serial Number Register Header (Upper DW)

Bits	Type	Default Value	Description
31:0	RO	0h	Serial Number register (Upper DW)

5.1.9 Power Budgeting Extended Capability

[Table 98] Power Budgeting Extended Capability Register Summary

Start Address	End Address	Symbol	Description
158h	15Bh	PB_ID	Power Budgeting Extended Capability ID
15Ch	15Fh	PB_SR	Data Select Register
160h	163h	PB_DR	Data Register
164h	167h	PB_BCR	Power Budget Capability Register

[Table 99] Power Budgeting Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	168h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	4h	PCI Express Extended Capability ID

[Table 100] Data Select Register

Bits	Type	Default Value	Description
31:8	RsvdP	0h	Reserved
7:0	RW	0h	Data Select

[Table 101] Data Register

Bits	Type	Default Value	Description
31:21	RsvdP	0h	Reserved
20:18	RO	0h	Power Rail
17:15	RO	0h	Type
14:13	RO	0h	PM State
12:10	RO	0h	PM Sub State
9:8	RO	0h	Data Scale
7:0	RO	0h	Base Power

[Table 102] Power Budget Capability Register

Bits	Type	Default Value	Description
7:1	RsvdP	0h	Reserved
0	HwInit	1h	System Allocated

5.1.10 Latency Tolerance Reporting Capability Registers

[Table 103] Latency Tolerance Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
188h	18Bh	LTR_ID	Latency Tolerance Reporting(LTR) Capability ID
18Ch	18Dh	LTR_SLR	LTR Max Snoop Latency Register
18Eh	18Fh	LTR_NSLR	LTR Max No-Snoop Latency Register

[Table 104] LTR Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	190h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	18h	PCI Express Extended Capability ID

[Table 105] LTR Max Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0h	Reserved
12:10	RW	0h	Max Snoop latency Scale
9:0	RW	0h	Max Snoop latency Value

[Table 106] LTR Max No Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0h	Reserved
12:10	RW	0h	Max No Snoop latency Scale
9:0	RW	0h	Max No Snoop latency Value

5.1.11 L1 Substates Capability Registers

[Table 107] L1 Substates Capability Register Summary

Start Address	End Address	Symbol	Description
190h	193h	L1S_CID	L1 Substate Capability ID
194h	197h	L1S_CR	L1 Substate Capability Register
198h	19Bh	L1S_C1R	L1 Substate Control 1 Register
19Ch	19Fh	L1S_C2R	L1 Substate Control 2 Register

[Table 108] L1 Substates Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	0h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	1Eh	PCI Express Extended Capability ID

[Table 109] L1 Substates Capability Register

Bits	Type	Default Value	Description
31:24	RsvdP	0h	Reserved
23:19	HwInit	5h	Port Power on value
18	RsvdP	0	Reserved
17:16	HwInit	0h	Port T_Power_on scale
15:8	HwInit	Ah	Port Common_mode_restore_time
7:5	RsvdP	0h	Reserved
4	HwInit	1	L1 PM Substates Supported
3	HwInit	1	ASPM PM L1.1 Supported
2	HwInit	1	ASPM PM L1.2 Supported
1	HwInit	1	PCI PM L1.1 Supported
0	HwInit	1	PCI PM L1.2 Supported

[Table 110] L1 Substates Control1 Register

Bits	Type	Default Value	Description
31:29	RW	0h	LTR L1.2 Threshold Scale
28:26	RsvdP	0h	Reserved
25:16	RW	0h	LTR L1.2 Threshold value
15:8	RsvdP	0h	Common_mode_restore_time (N/A)
7:4	RsvdP	0h	Reserved
3	RW	0	ASPM PM L1.1 Supported
2	RW	0	ASPM PM L1.2 Supported
1	RW	0	PCI PM L1.1 Supported
0	RW	0	PCI PM L1.2 Supported

[Table 111] L1 Substates Control2 Register

Bits	Type	Default Value	Description
31:8	RsvdP	0h	Reserved
7:3	RW	5h	T_POWER_ON Value
2	RsvdP	0	Reserved
1:0	RW	0h	T_POWER_ON Scale

5.2 NVM Express Registers

5.2.1 Register Summary

[Table 112] Register Summary

Start Address	End Address	Name	Type
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	Reserved	Reserved
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	EFFh	Reserved	Reserved
F00h	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
...			
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDVL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQYHDBL	Completion Queue y Head Doorbell

5.2.2 Controller Registers

[Table 113] Controller Capabilities

Bits	Type	Name	Default Value	Description
63:56:00	RO	-	0h	Reserved
55:52:00	RO	MPSMAX	0h	Memory Page Size Maximum (Maximum is 4KB)
51:48:00	RO	MPSMIN	0	Memory Page Size Minimum (Minimum is 4KB)
47:45:00	RO	-	0	Reserved
44:37:00	RO	CSS	1h	Command Sets Supported 1h: NVM command set
36	RO	NSSRS	1h	NVM Subsystem Reset Supported
35:32:00	RO	DSTRD	0	Doorbell Stride 0: Stride of 4 bytes
31:24:00	RO	TO	3Ch	Timeout 3Ch: 30 seconds
23:19	RO	-	0	Reserved
18:17	RO	AMS	1h	Arbitration Mechanism Supported (Weighted Round Robin with Urgent supported)
16	RO	CQR	1	Contiguous Queues Required
15:00	RO	MQES	3FFFh	Maximum Queue Entries Supported (16384 entries supported)

[Table 114] Version

Bits	Type	Name	Default Value	Description
31:16	RO	MJR	1h	Major Version Number
15:0	RO	MNR	200h	Minor Version Number

NOTE:
The PM983 supports NVM Express version 1.2 (partially).

[Table 115] Interrupt Mask Set

Bits	Type	Name	Default Value	Description
31:0	RW1S	IVMS	0	Interrupt Vector Mask Set

[Table 116] Interrupt Mask Clear

Bits	Type	Name	Default Value	Description
31:00	RW1C	IVMC	0	Interrupt Vector Mask Clear

[Table 117] Controller Configuration

Bits	Type	Name	Default Value	Description
31:24	RO	-	0	Reserved
23:20	RW	IOCQES	0	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16 byte entry size)
19:16	RW	IOSQES	0	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64 byte entry size)
15:14	RW	SHN	0	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0	Reserved
0	RW	EN	0	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

[Table 118] Controller Status

Bits	Type	Name	Default Value	Description
31:6	RO	-	0	Reserved
5	RW	PP	0	Processing Paused
4	RW1C	NSSRO	0	NVM Subsystem Reset Occurred
3:2	RO	SHST	0	Shutdown Status 0h: Normal operation, no shutdown requested 1h: Shutdown processing occurring 2h: Shutdown processing complete 3h: Reserved
1	RO	CFS	0	Controller Fatal Status
0	RO	RDY	0	1h: Controller ready to process commands 0h: Controller shall not process commands.

[Table 119] Admin Queue Attributes

Bits	Type	Name	Default Value	Description
31:28	RO	-	0	Reserved
27:16	RW	ACQS	0	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's based value)
15:12	RO	-	0	Reserved
11:0	RW	ASQS	0	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's based value)

[Table 120] Admin Submission Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ASQB	0	Admin Submission Queue Base Address
11:0	RO	-	0	Reserved

[Table 121] Admin Completion Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ACQB	0	Admin Completion Queue Base Address
11:0	RO	-	0	Reserved

[Table 122] Submission Queue Tail y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	SQT	0	Submission Queue Tail

[Table 123] Completion Queue Head y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	CQH	0	Completion Queue Head

6.0 Supported Command Set

The Admin command sets and NVM I/O command sets of Samsung SSD PM963 are defined in compliant with NVM Express specification revision 1.2a

6.1 Admin Command Set

The Admin command set is the commands that are submitted to the Admin Submission Queues. The detailed specifications are described in NVM Express specification document.

[Table 124] Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature
0Ah	Get Feature
0Ch	Asynchronous Event Request
0Dh	Namespace Management
10h	Firmware Activate
11h	Firmware Image Download
15h	Namespace Attachment
19h	Directive Send (Not support)
1Ah	Directive Receive (Not support)
80h – BFh	I/O Command Set Specific
C0h – FFh	Vendor Specific

6.1.1 Identify Command

The Identify Command returns the data described below.

[Table 125] Identify Controller Data Structure

Bytes	O/M	Default Value	Description
1:0	M	144Dh	PCI Vendor ID
3:2	M	144Dh	PCI Subsystem Vendor ID
23:4	M	S##############	Serial Number (ASCII), #:Variables
63:24	M	960GB : SAMSUNG MZQLB960HAJR-00007 1.92TB : SAMSUNG MZQLB1T9HAJR-00007 3.84TB : SAMSUNG MZQLB3T8HALS-00007 7.68TB : SAMSUNG MZQLB7T6HMLA-00007	Model Number (ASCII)
71:64	M	########	Firmware Revision, #:Variables
72	M	2h	Recommended Arbitration Burst
75:73	M	002538h	IEEE OUI
76	O	0	Multi-Interface Capabilties and Namespace Sharing Capability Bit 2: 1h - Controller is associated with an SR-IOV Virtual Function 0h - Controller is associated with a PCI Function. Bit 1: 1h - Device has Two or More controller 0h - Device has One Controller Bit 0: 1h - Device has Two or More physical PCI Express ports 0h - Device has One PCI Express port

77	M	9h	Maximum Data Transfer Size 9h: 2MB
79:78	M	04h	Controller ID (CNTLID)
83:80	M	0x10200	Controller Version
87:84	M	0x7a1200	RTD3 Resume Latency
91:88	M	0x7a1200	RTD3 Entry Latency
95:92	M	0h	OAES_Reserved
239:96	-	0h	Reserved
255:240	M	-	NVMe Management Interface Specification for Definition
257:256	M	Fh	Optional Admin Command Support Bits 15:6 - Reserved Bit 5 if set to '1' then the controller supports Directives. If cleared to '0' then the controller does not support Directives. A controller that supports Directives shall support the Directive Send and Directive Receive commands. Refer to section 9. Bit 4 if set to '1' then the controller supports the Device Self-test command. If cleared to '0' then the controller does not support the Device Self-test command. Bit 3: 1h - Namespace Management and Namespace Attachment Commands Supported (PM963 conditionally supports the Namespace Management and Namespace Attachment command(NVMe v1.2 specification) for reconfigurable overprovisioning) Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 0 Security Send and Security Receive Not Supported
258	M	7h	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)
259	M	3h	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)
260	M	17h	FirmwareUpdates Bits7:5–Reserved Bits4– 1h Controller supports firmware activation without a reset 0h Controller requires a reset for firmware to be activated Bits3:1–Numbeorffirmwareslots Bit 0 – 1h Slot 1 is read only
261	M	3h	Log Page Attributes Bits 7:1 – Reserved Bit 0: 0h SMART data is global for all namespaces
262	M	3Fh	Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)
263	M	0h	Number of Power States Support (0's based value)
264	M	1h	Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in Admin and NVM Vendor Specific Commands (Optional) table of NVM Express spec.
265	O	0h	Autonomous Power State Transition Attributes (APSTA)
267:266	M	168h	Warning Composite Temperature Threshold

269:268	M	169h	Critical Composite Temperature Threshold
271:270	O	0h	Maximum Time for Firmware Activation
275:272	O	0h	Host Memory Buffer Preferred Size
279:276	O	0h	Host Memory Buffer Minimum Size
295:280	O	6FC81AB0h * 512 (960GB) DF8FE2B0h * 512 (1920GB) 1BF1F72B0h * 512 (3840GB) 37E3E92B0 * 512 (7680GB)	Total NVM Capacity
311:296	O	0h	Unallocated NVM Capacity
315:132	O	0h	RPMBS_NUMBER_RPMB_UNITS
315:132	O	0h	RPMBS_AUTHENTICATION_METHOD
315:132	O	0h	RPMBS_RESERVED
315:132	O	0h	RPMBS_TOTAL_SIZE
315:132	O	0h	RPMBS_ACCESS_SIZE
511:316	-	-	Reserved
512	M	66h	Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)
513	M	44h	Completion Queue Entry Size Bits 7:4 – 4h Max SQES (16 bytes) Bits 3:0 – 4h Required SQES (16 bytes)
515:514		0h	Reserved
519:516	M	1h	Number of Namespaces
521:520	M	1Fh	Optional NVM Command Support Bits 15:6 – Reserved Bit 5 – 1h Reservations Supported 0h Not support Reservations Bit 4 – 1h Save field in Set Feature & Select field in Get Feature Supported 0h Not support Save field in Set Feature & Select field in Get Feature Bit 3 – 1h Write Zeros Supported 0h Not support Write Zeros Bit 2 – 1h Dataset Management Supported 0h Not support Dataset Management Bit 1 – 1h Write Uncorrectable Supported 0h Not support Write Uncorrectable Bit 0 – 1h Compare Supported 0h Not support Compare
523:522	M	0h	Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported
524	M	4h	Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase Bit 1 – 1h Secure Erase Per Namespace Bit 0 – 0h Format Per Namespace
525	M	0h	Volatile Write Cache 0h – No VWC present
527:526	M	3Fh	Atomic Write Unit Normal
529:528	M	0h	Atomic Write Unit Power Fail (0's based value)
530	M	1h	NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express specification

531	M	0h	Reserved
533:532	O	0h	ACWU
534:533	M	0h	Reserved
539:536	O	0h	No SGL support
703:540	-	0h	Reserved
I/O Command Set Attributes			
2047:704	-	0h	Reserved
Power State Descriptors			
2079:2048	M	refer to 'Identify Power State Descriptor Data Structure'	Power State 0 Descriptor
2111:2080	O	0h	N/A
2143:2112	O	0h	N/A
...	-	0h	N/A
3071:3040	O	0h	Power State 31 Descriptor (N/A)
Vendor Specific			
4095:3072	-	-	Samsung Reserved

[Table 126] Identify Power State Descriptor Data Structure

Bits	Power State 0	Description
255:184	0h	Reserved
183:182	0h	Active Power Scale(APS)
181:179	0h	Reserved
178:176	0h	Active Power Workload(APW)
175:160	0h	Active Power(ACTP)
159:152	0h	Reserved
151:150	0h	Idle Power Scale(IPS)
149:144	0h	Reserverd
143:128	0h	Idle Power(IDLP)
127:125	0h	Reserved
124:120	0h	Relative Write Latency
119:117	0h	Reserved
116:112	0h	RelativeWriteThroughput
111:109	0h	Reserved
108:104	0h	RelativeReadLatency
103:101	0h	Reserved
100:96	0h	RelativeReadThroughput
95:64	5h	Exit Latency
63:32:00	5h	EntryLatency (100us)
31:26:00	0h	Reserved
25	0h	Non-Operational State
24	0h	Max Power Scale
23:16	0h	Reserved
15:00	3FCh	Maximum Power

[Table 127] Identify Namespace Data Structure

Bytes	O/M	Default Value		Description
7:0	M	960GB 1920GB 3840GB 7680GB	6FC81AB0h (512B) DF8FE2B0h (512B) 1BF1F72B0h (512B) 37E3E92B0 (512B)	Namespace Size
15:8	M	960GB 1920GB 3840GB 7680GB	6FC81AB0h (512B) DF8FE2B0h (512B) 1BF1F72B0h (512B) 37E3E92B0 (512B)	Namespace Capacity
23:16	M	-		Namespace Utilization A device may report Namespace Utilization equal to Namespace Capacity at all times if the product is not targeted for thin provisioning environments
24	M	2h		Namespace Features Bits 7:1 Reserved Bit 0: Thin provisioning not supported
25	M	1h		Number of LBA Formats
26	M	0h		Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format
27	M	0h		Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA
28	M	0h		End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information
29	M	0h		End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bit 3 – 1: Protection information transferred as first 8 bytes of metadata Bit 3 – 0: Protection information transferred as last 8 bytes of metadata Bit 2:0 – 000b: Protection information disabled Bit 2:0 – 1h: Protection type 1 enabled Bit 2:0 – 2h: Protection type 2 enabled Bit 2:0 – 3h: Protection type 3 enabled
30	O	0h		Namespace Multi-path I/O and Namespace sharing Capabilities (NMIC) Bits 7:1 - Reserved Bit 0 - 1 : Accessible by two or more controllers Bit 0 - 0 : Private namespace

31	O	0h	Reservation Capabilities (RESCAP) Bits 7 - Reserved Bits 6 - 1: Namespace supports the Exclusive Access (All Registrants reservation type) Bit 5 - 1 : Namespace supports the Write Exclusive (All Registrants reservation type) Bit 4 - 1 : Namespace supports the Exclusive Access (Registrants only reservation type) Bit 3 - 1 : Namespace supports the Write Exclusive (Registrants only reservation type) Bit 2 - 1 : Namespace supports the Exclusive Access Reservation type Bit 1 - 1 : Namespace supports the Write Exclusive Reservation type Bit 0 - 1 : Namespace supports the Persist Through Power Loss capability
32	O	80h	Format Progress Indicator(FPI)
33	-	Reserved	
35:34	O	3FFh	Namespace Atomic Write Unit Normal
37:36	O	7h	Namespace Atomic Write Unit Power Fail
39:38	O	0h	Namespace Atomic Compare & Write Unit
41:40	O	3FFh	Namespace Atomic Boundary Size Normal
43:42	O	0h	Namespace Atomic Boundary Offset
45:44	O	7h	Namespace Atomic Boundary Size Power Fail
47:46	-	Reserved	
63:48	O	6FC81AB0h * 512 (960GB) DF8FE2B0h * 512 (1920GB) 1BF1F72B0h * 512 (3840GB) 37E3E92B0 * 512 (7680GB)	NVM Capacity (NVMCAP)
103:64	-	0h	Reserved
119:104	O	################002538##########h	Namespace Globally Unique Identifier (NGUID) #:Variables *NGUID specifies data in a big endian format.
127:120	O	0h	IEEE Extended Unique Identifier(EUI64) #:Variables *EUI64 specifies data in a big endian format.
131:128	M	refer to 'LBA Format 0 Data Structure'	LBA Format 0 Support
135:132	O	refer to 'LBA Format 1 Data Structure'	LBA Format 1 Support
139:136	O	0h	LBA Format 2 Support
143:140	O	0h	LBA Format 3 Support
147:144	O	0h	LBA Format 4 Support (N/A)
…			
191:188	O	0h	LBA Format 15 Support (N/A)
383:192	-	0h	Reserved
Vendor Specific			
4095:384	-	-	Samsung Reserved

[Table 128] LBA Format 0 Data Structure

Bits	Name	Default Value	Description
31:26		0	Reserved
25:24	RP	0	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	0	Metadata Size

[Table 129] LBA Format 1 Data Structure

Bits	Name	Default Value	Description
31:26		0	Reserved
25:24	RP	0	Relative Performance
23:16	LBADS	Ch	LBA Data Size
15:00	MS	0	Meta data Size

6.2 NVM Express I/O Command Set

[Table 130] Opcode for NVM Express I/O Commands

Opcode (Hex)	Command Name
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

NOTE:
1) Deallocate feature in Dataset Management command is only supported in the Samsung SSD PM983.

6.3 SMART/Health Information

[Table 131] SMART/Health Information Log

Bytes	Default Value	Attribute Description
0	0	Critical Warning Bit 7:5 – Reserved Bit 4 – 1h: the volatile memory backup device has failed. (only valid if the controller has a volatile memory backup solution) Bit 3 – 1h: the media has been placed in read only mode Bit 2 – 1h: the device reliability has been degraded due to significant media related errors or any internal error that degrades device reliability Bit 1 – 1h: the temperature has exceeded a critical threshold Bit 0 – 1h: the available spare space has fallen below the threshold
2:1	current temp.	Temperature
3	100	Available Spare
4	10	Available Spare Threshold
5	0	Percentage Used
31:6	-	Reserved
47:32	0	Data Units Read
63:48	0	Data Units Written
79:64	0	Host Read Commands
95:80	0	Host Write Commands
111:96	0	Controller Busy Time
127:112	0	Power Cycles
143:128	0	Power On Hours
159:144	0	Unsafe Shutdowns
175:160	0	Media Errors
191:176	0	Number of Error Information Log Entries
511:192	-	Reserved
195:192	0	Warning Composite Temperature Time
199:196	0	Critical Composite Temperature Time
201:200	0	Temperature Sensor 1
203:202	0	Temperature Sensor 2
205:204	0	Temperature Sensor 3
207:206	0	Temperature Sensor 4
209:208	0	Temperature Sensor 5
211:210	0	Temperature Sensor 6
213:212	0	Temperature Sensor 7
215:213	0	Temperature Sensor 8
511:216	-	Reserved

6.4 Extended SMART Information (LID : 0xCA)

[Table 132] Extended SMARTInformation Log

Bytes	Default Value	Attribute Description
11:00	ID:0xAB Normalized Value:100 Current Value:0	Lifetime Program Fail Count
23:12	ID:0xAC Normalized Value:100 Current Value:0	Lifetime Erase Fail Count
35:24	ID:0xAD Normalized Value:100 Current Value:0	Lifetime Wear Level Count
47:36	ID:0xB8 Normalized Value:100 Current Value:0	Lifetime E2E Error Count
59:48	ID:0xC7 Normalized Value:100 Current Value:0	Lifetime CRC Error Count
71:60	ID:0xE2 Normalized Value:100 Current Value:0	Media Wear Pctg
83:72	ID:0xE3 Normalized Value:100 Current Value:0	Host Read Pctg
95:84	ID:0xE4 Normalized Value:100 Current Value:0	Workload Timer
107:96	ID:0xEA Normalized Value:100 Current Value:0	Lifetime Thermal Throttle Status
131:108	-	Reserved
143:132	ID:0xF4 Normalized Value:100 Current Value:0	Lifetime Phy Pages Written Count
155:144	ID:0xF5 Normalized Value:100 Current Value:0	Lifetime Data Units Written
255:156	-	Reserved
259:256	0	Lifetime Write Amplification Factor
263:260	0	Trailing Hour Write Amplification Factor
279:264	0	Lifetime User Writes
295:280	0	Lifetime NAND Writes
311:296	0	Lifetime User Reads
315:312	0	Lifetime Retired Block Count
317:316	current temp.	Current Temperature
319:318	100	Capacitor Health
323:320	reserved block count	Lifetime Unused Reserved Block
331:324	0	Read Reclaim Count
339:332	0	Lifetime UECC Count
343:340	0	Lifetime Used Reserved Block
359:344	0	Power on Hours
375:360	0	NPO Count
391:376	0	SPO Count
395:392	0	Perf Indicator

7.0 SPOR Specification (Sudden Power Off and Recovery)

7.1 Data Recovery in Sudden Power off

If power interruption is detected, SSD dumps all cached user data and meta data to NAND Flash. SSD could protect even the user data in DRAM from sudden power off while SSD is used with cache on. Commonly, data is protected all of the operation period.

7.2 Time to Ready Sequence

In normal power-off recovery status, SSD needs less than 8 seconds to reach operating mode where SSD works perfectly with cache-on state. SSD is ready to respond identify Device command during FTL OPEN. When the sudden power-off occurs, the user data in DRAM will be dumped into the NAND Flash using the stored power in the capacitor. In sudden power-off recovery condition, mapping data will be loaded or the FTL meta data be rebuilt perfectly for initial max. 20 seconds in 3.84TB. During this period, Identify Device command is still supported. It is called SPOR. (Sudden Power Off and Recovery)

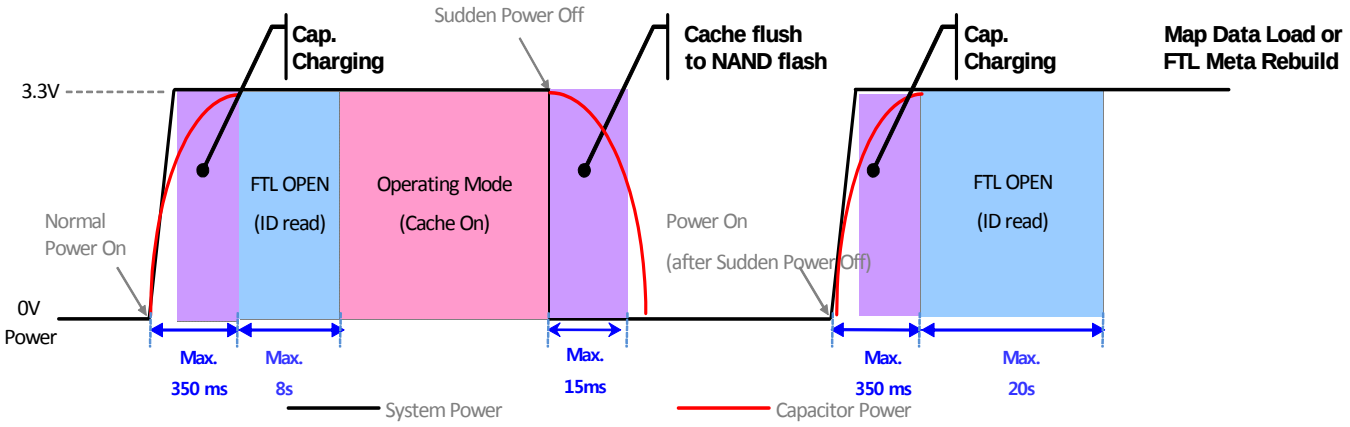


Figure 2. Sudden Power on-off operation

[Table 133] Device Ready Time for Normal Read / Write Operation after Sudden Power Off

	960GB	1.92TB	3.84TB	7.68TB
Max. Open Time (sec)	10s	10s	20s	TBD

8.0 SMBUS RESOURCES

The expansion ROM integrated in Samsung SSD PM983 supports booting UEFI operating system installed on the drive, it complies to UEFI standard, which is specified in UEFI v2.4 Specification.

This section listed data structures and registers accessible through SMBus interface.
Vital Product Data (VPD) is stored in SM-Bus slave address of 0xA6 (bits 7-1 correspond to 1010_011 on the SM-Bus). Temperature sensor is stored in SM-Bus slave address of 0x36 (bits 7-1 correspond to 0011_011).

8.1 Vital Product Data (VPD) Structure

VPD listed device specific information for Enterprise PCIe SSD discovery and power allocation.

Bytes	Name	Default Value	Description
02:00	Class Code	010802h	Device Type & Programming Interface
04:03	ID	144Dh	PCI-SIG Vendor ID
24:05	ID	S##############	Serial Number(Vendor Unique, ASCII String), # :Variables
64:25	ID	960GB : SAMSUNG MZQLB960HAJR-00007 1.92TB : SAMSUNG MZQLB1T9HAJR-00007 3.84TB : SAMSUNG MZQLB3T8HALS-00007 7.68TB : SAMSUNG MZQLB7T6HMLA-00007	Model Number (ASCII String)
65:65	PCIe Port 0 Capabilities	03h	Maximum Link Speed (PCIe Gen3)
66:66	PCIe Port 0 Capabilities	04h	Maximum Link Width (x8)
67:67	-	0h	-
68:68	-	0h	-
69:69	Inital Power Requirements	04h	12V Power rail initial power requirement (4 W)
71:70	Inital Power Requirements	0h	Reserved
72:72	Max power Requirement	0Bh	12V Power rail maximum power requirement (11W)
74:73	Max power Requirement	0h	Reserved
76:75	Cap List Pointer	0050h	Start Cap Address Pointer (0x50)
79:77	-	0h	-
81:80	-	00A2h	VU Cap ID
83:82	-	0h	Next Cap Address (NULL)
84:84	Sensor Type	0h	JC-42.4 TSE2004av compliant temperature sensor on 3.3Vaux
85:85	Sensor Address	36h	-
87:86	-	0h	Reserved
88:88	Warning Thresh - LSB	70h	"DTT state" engaging temperature (Refer to the Note)
89:89	Warning Thresh - MSB	05h	"DTT state" engaging temperature (Refer to the Note)
90:90	OverTemp Thresh - LSB	80h	"Critical state" engaging temperature (Refer to the Note)
91:91	OverTemp Thresh - MSB	05h	"Critical state" engaging temperature (Refer to the Note)
254:92	-	FFh	Reserved
255:255	-	FFh	

NOTE: TSE2004av temperature encoding:

B15/B07	B14/B06	B13/B05	B12/B04	B11/B03	B10/B02	B09/B01	B08/B00
N/A	N/A	N/A	Sign	128	64	32	16
8	4	2	1	N/A	N/A	N/A	N/A

The 16-bit value is 2s complement representation of a temperature with the Bit 4 equal to the minimum granularity of 1 °C. Bit 12 is the sign bit.
For example:
1. a value of 0190h represents 25 °C,
2. a value of 07C0 h represents 124 °C, and
3. a value of 1E80 h represents –24 °C

By choosing the starting of the lowest bit the resolution of the temperature sensor can be defined. For SMBus temperature capability support PM983's temperature sensor is at resolution of 1°C (8-bit)

8.2 Temperature Sensor Register Summary

Offset	Type	Name	Description	Default
00	RO	Capabilities	Capability register	0x00EF
01	RW	Configuration	Configuration register (CONFIG)	0x0000
02	RW	TUPPER	Event Temperature Upper-Boundary Trip register	0x0000
03	RW	TLOWER	Event Temperature Lower-Boundary Trip register	0x0000
04	RW	TCRIT	Critical Temperature Trip register	0x0000
05	RO	TA	Ambient Temperature	0x0000
06	RO	Manufacture ID	Manufacturer ID register	0x0054
07	RO	Reserved	Reserved	0x0601
08	RO	Device/Revision	Device ID/Revision register	0x0601
09	RW	Resolution register	Resolution register	0x0001

8.2.1 Capability register

Bits	Type	Default Value	Description
15:8	RO	0	Unimplemented: Read as '0'
7	RO	1	Event Output Status During Shutdown (SHDN Status): 0 = Event output remains in previous state. If the output asserts before shutdown command, it remains asserted during shutdown. 1 = Event output deasserts during shutdown. After shutdown, it takes tCONV to reassert the event output (power-up default)
6	RO	1	I2C Bus Time-Out (tOUT Range): 0 = Bus time-out range is 10 ms to 60 ms 1 = Bus time-out range is 25 ms to 35 ms (power-up default)
5	RO	1	Unimplemented: Read as '1'
4:3	RO	01	Resolution: 00 = 0.5°C 01 = 0.25? (power-up default) 10 = 0.125°C 11 = 0.0625°C
2	RO	1	Temperature Measurement Range (Meas. Range): 0 = TA=0 (decimal) for temperature below 0°C 1 = The part can measure temperature below 0°C (power-up default)
1	RO	1	Accuracy: 0 = Accuracy → ±2°C from +75°C to +95°C (Active Range) and ±3°C from +40°C to +125°C (Monitor Range) 1 = Accuracy → ±1°C from +75°C to +95°C (Active Range) and ±2°C from +40°C to +125°C (Monitor Range)
0	RO	1	Temperature Alarm: 0 = No defined function (This bit will never be cleared or set to '0') 1 = The part has temperature boundary trip limits (TUPPER/TLOWER/TCRIT registers) and a temperature event output (JC 42.4 required feature)

8.2.2 Configuration register (CONFIG)

Bits	Type	Default Value	Description
15:11	RW	0	Unimplemented: Read as '0'
10:09	RW	00	TUPPER and TLOWER Limit Hysteresis (THYST): 00 = 0? (power-up default) 01 = 1.5°C 10 = 3.0°C 11 = 6.0°C
8	RW	0	Shutdown Mode (SHDN): 0 = Continuous Conversion (power-up default) 1 = Shutdown (Low-Power mode)
7	RW	0	TCRIT Lock Bit (Crit. Lock): 0 = Unlocked. TCRIT register can be written. (power-up default) 1 = Locked. TCRIT register can not be written
6	RW	0	TUPPER and TLOWER Window Lock Bit (Win. Lock): 0 = Unlocked. TUPPER and TLOWER registers can be written. (power-up default) 1 = Locked. TUPPER and TLOWER registers can not be written
5	RW	0	Interrupt Clear (Int. Clear) Bit: 0 = No effect (power-up default) 1 = Clear interrupt output. When read this bit returns '0'
4	RW	0	Event Output Status (Event Stat.) Bit: 0 = Event output is not asserted by the device (power-up default) 1 = Event output is asserted as a comparator/Interrupt or critical temperature output
3	RW	0	Event Output Control (Event Cnt.) Bit: 0 = Event output Disabled (power-up default) 1 = Event output Enabled
2	RW	0	Event Output Select (Event Sel.) Bit: 0 = Event output for TUPPER, TLOWER and TCRIT (power-up default) 1 = TA ≥ TCRIT only. (TUPPER and TLOWER temperature boundaries are disabled.)
1	RW	0	Event Output Polarity (Event Pol.) Bit: 0 = Active-low (power-up default. Pull-up resistor required) 1 = Active-high
0	RW	0	Event Output Mode (Event Mod.) Bit: 0 = Comparator output (power-up default) 1 = Interrupt output

8.2.3 Event Temperature, Critical Temperature Trip register

Bits	Type	Default Value	Description	Remark
15:13	RW	0	Unimplemented: Read as '0'	
12	RW	0	Sign: 0 = TA ≥ 0°C 1 = TA < 0°C	
11	RW	0	2^{7}°C	TUPPER/TLOWER/TCRIT:Temperature boundary trip data in two's complement format
10	RW	0	2^{6}°C	
09	RW	0	2^{5}°C	
08	RW	0	2^{4}°C	
07	RW	0	2^{3}°C	
06	RW	0	2^{2}°C	
05	RW	0	2^{1}°C	
04	RW	0	2^{0}°C	
03	RW	0	2^{-1}°C	
02	RW	0	2^{-2}°C	
1:0	RW	0	Unimplemented: Read as '0'	

8.2.4 Ambient Temperature Register

Bits	Type	Default Value	Description
15	RO	0	TA vs. TCRIT Bit: 0 = TA < TCRIT°C 1 = TA ≥ TCRIT°C
14	RO	0	TA vs. TUPPER Bit: 0 = TA ≤ TUPPER°C 1 = TA > TUPPER°C
13	RO	0	TA vs. TLOWER Bit: 0 = TA ≥ TLOWER°C 1 = TA < TLOWER°C
12	RO	0	Sign: 0 = TA ≥ 0°C 1 = TA < 0°C
11	RO	0	2^{7}°C
10	RO	0	2^{6}°C
09	RO	0	2^{5}°C
08	RO	0	2^{4}°C
07	RO	0	2^{3}°C
06	RO	0	2^{2}°C
05	RO	0	2^{1}°C
04	RO	0	2^{0}°C
03	RO	0	2^{-1}°C
2	RO	0	2^{-2}°C
1	RO	0	2^{-3}°C
0	RO	0	2^{-4}°C

8.2.5 Manufacture ID Register

Bits	Type	Default Value	Description
15:0	RO	0x0054	Device Manufacturer Identification Number

8.2.6 Device/Revision Register

Bits	Type	Default Value	Description
15:0	RO	0x0601	Device ID / Revision Register

8.2.7 Resolution Register

Bits	Type	Default Value	Description
15	RW	0	Unimplemented: Read as '0'
14:2	RO	0	Unimplemented: Read as '0'
1:0	RW	01	Resolution: 00 = LSb = 0.5°C (tCONV = 30 ms, typical) 01 = LSb = 0.25°C (power-up default, tCONV = 65 ms, typical) 10 = LSb = 0.125°C (tCONV = 130 ms, typical) 11 = LSb = 0.0625°C (tCONV = 260 ms, typical)

9.0 UEFI EXPANSION ROM

The expansion ROM integrated in Samsung SSD PM983 supports booting UEFI operating system installed on the drive, it complies to UEFI standard, which is specified in UEFI v2.4 Specification.

9.1 Basic Information

- IA32/x64 architecture support: x64 only
- Binary executable size is exactly equal to 64KB
- Platform BIOS requirement: EFI Specification Revision 2.31+, EFI Shell Version 1.0
- Number of Admin Submission Queue/Admin Completion Queue entries: 2
- Number of IO Queue entries: 2
- Maximum number of IO queues supported: 2
- Interrupt used: None

9.1.1 General Features

- Supports various operating systems booting in UEFI mode
- Ability to boot from large partition (over 2TB) with GUID Partition Table (GPT)
- Provides drive information via UEFI user interface (HII) in pre-boot environment (such as model number, firmware revision and drive capacity)
- Supports Secure Boot
- UEFI standard APIs supporting followings in pre-boot environment (EFI Shell):
. Basic block read/write access (produced API: EfiBlockIoProtocol)
. Driver health information (produced API: EfiDriverHealthProtocol)
. Drive diagnostic function (produced API: EfiDriverDiagnostics2Protocol)
. NVMHCI functions: GetLogPage, Firmware Download/Activate and Format (produced API: EfiFirmwareManagementProtocol and NvmExpressPassThruProtocol)

9.2 Supported Operating Systems

Index	Operating Systems bootable on PM983 drive
1	Windows Server 2016
2	Windows Server 2012 R2 64-bit
3	RHEL 7.2 (Kernel 2.6.32)
4	RHEL 6.6 (Kernel 2.6.32)
5	CentOS 6.7
6	CentOS 7.3
7	Ubuntu 14.10
8	Ubuntu 15.10
9	SLES 11 SP3 (Kernel 3.0.13)
10	SLES 12 (Kernel 3.12.28)
11	Oracle Linux 6.6
12	Oracle Linux 7.2

10.0 PRODUCT COMPLIANCE

10.1 Product regulatory compliance and Certifications

[Table 134] Certifications and Declarations

Category	Certifications
Safety	c-UL-us
	CE
	TUV
	CB
EMC	CE (EU)
	BSMI (Taiwan)
	KCC (South Korea)
	VCCI (Japan)
	RCM (Australia)
	FCC (USA)
	IC (CANADA)

The three existing compliance marks (C-Tick, A-Tick and RCM) are consolidated into a single compliance mark - the RCM.

Caution: Any changes or modifications in construction of this device which are not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications, However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
Modifications not expressly approved by the manufacturer could void the user's authority to operated the equipment under FCC rules.

1. 기자재 명칭 : SSD (Solid State Drive)
2. 모델명(Model): 라벨 별도 표기
3. 제조연월 : 라벨 별도 표기
4. 제조자 : 삼성전자(주)
5. 제조국가 : 대한민국
6. 상호명 : 삼성전자(주)

Industry Canada ICES-003 Compliance Label:
CAN ICES-3 (B)/NMB-3(B)

11.0 References

[Table 135] Standards References

Item	Website
PCI Express Base Specification Revision 3.1	http://www.pcisig.com/specifications/pciexpress/base3/
PCI Express CEM Specification Revision 3.0	http://www.pcisig.com/specifications/
NVM Express Specification Rev. 1.2	http://www.nvmexpress.org/
Enterprise SSD Form Factor Version 1.0a	http://www.ssdformfactor.org/
Solid-State Drive Requirements and Endurance Test Method (JESD218A)	http://www.jedec.org/standards-documents/docs/jesd218a
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a