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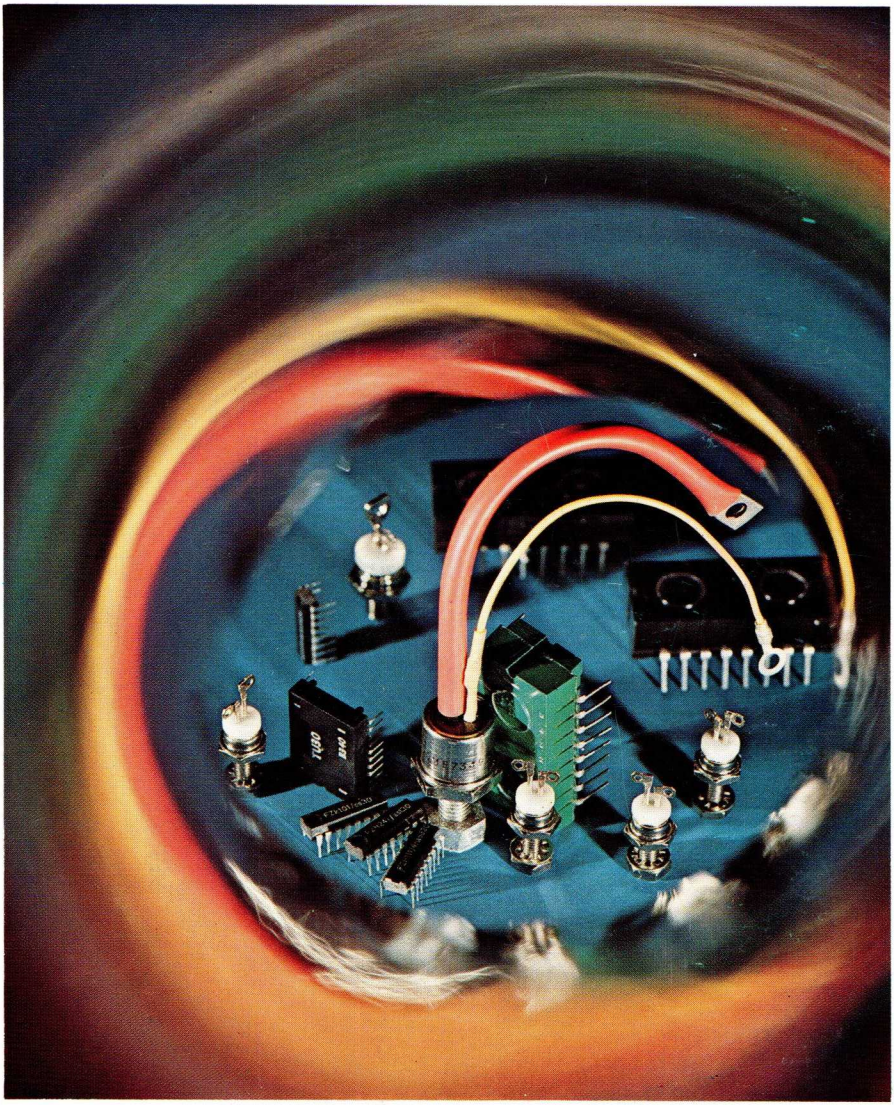
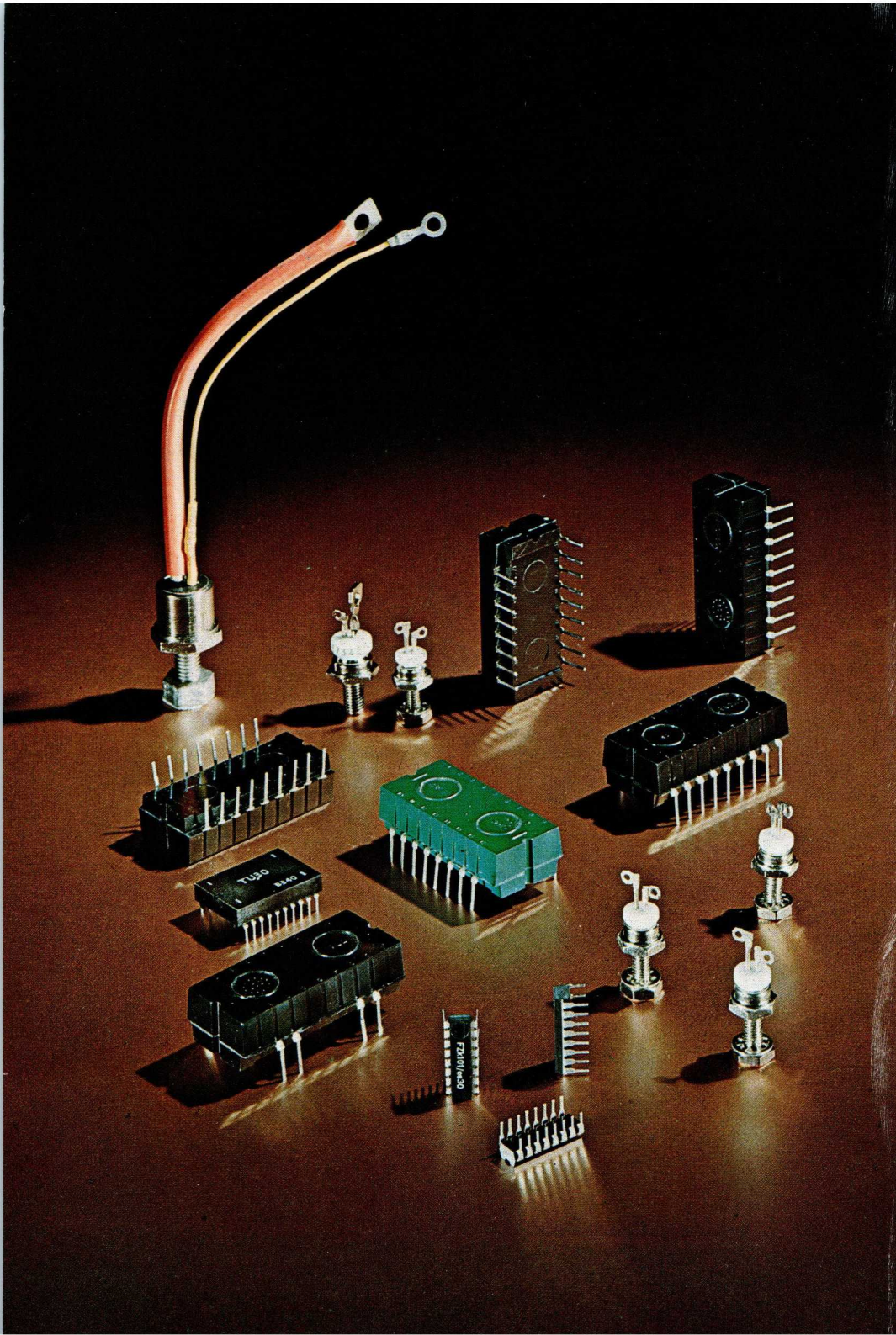
Industrial triacs and their applications



Industrial triacs and their applications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Industrial triacs and their applications

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ELECTRONIC COMPONENTS AND MATERIALS DIVISION

Contents

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Foreword

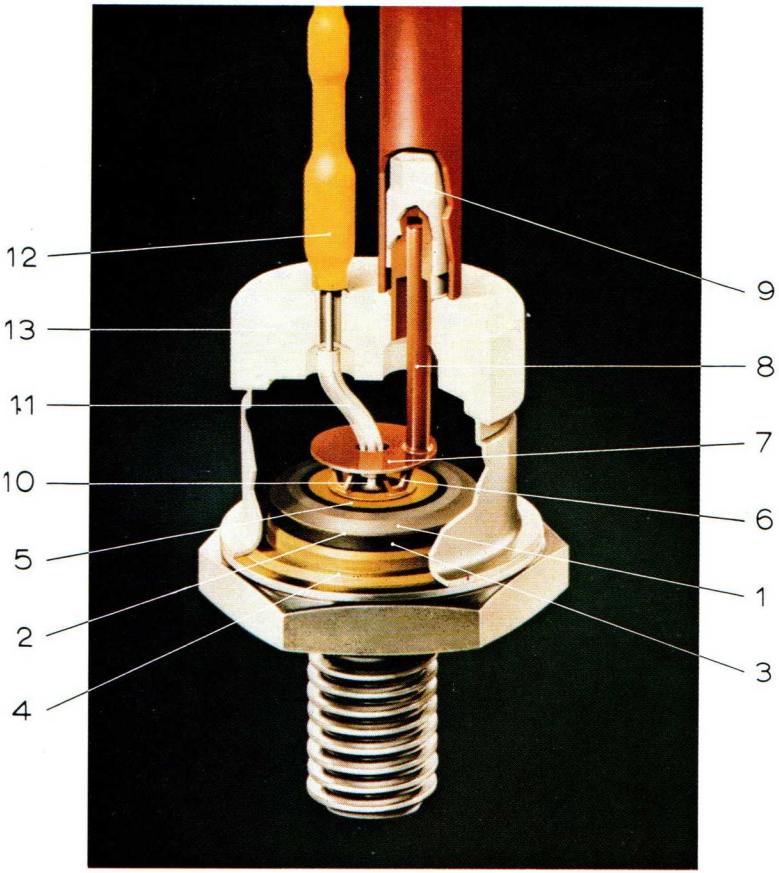
The past few years have seen unprecedented growth in semiconductor technology. Its frontiers have not only advanced but expanded so rapidly that systems and equipment design engineers have been increasingly hard put to keep up with developments that affect their own fields of interest. As this accelerating trend continues, one aspect of that technology which is sure to be in the forefront is the development and application of power control devices — especially four-layer devices such as thyristors and triacs.

Thyristors are already well established. They have been extensively dealt with in the literature and most engineers are by now well acquainted with their use. Triacs, however, have not fared so well. The literature concerning them is scanty, and early disappointments, due either to shortcomings of the devices themselves or improper understanding of how to apply them, have made many prospective users shy of them. One aim of this book is to break down that barrier — an aim that is the more challenging in that the barrier is, admittedly, not without some historical basis. For all their promise, the first generation of triacs unquestionably left something to be desired, particularly as regards commutation behaviour and voltage capability.

But recent advances in semiconductor technology have now swept those limitations aside. Dramatic improvements in commutation behaviour enable the present generation of triacs to give completely reliable service in nearly all mains applications. Similar improvements in voltage capability make it possible to recommend many of them for use even on 380 V mains.

Circuit technology too has undergone comparable development. The circuits presented in this book enable the design engineer to take full advantage of what today's generation of triacs can do. Not only that, but by mastering the few simple principles that underly those circuits, he will also prepare himself to take similar advantage of the still more advanced devices that will emerge from the development laboratories in the years to come.

H. D. Gräve



Cut-away view of BTW34 Triac.

1 = double-bevel silicon crystal
2 = fatigue-free hard-solder connection
3 = molybdenum disc for thermal-expansion equalization
4 = gold-plated copper contact block (terminal 2)
5 = terminal 1 metallization
6 = coronet washer for thermal expansion equalization
7 = current collector ring
8 = terminal 1 connection
9 = terminal attachment for braiding
10 = gate metallization
11 = heat-resistant gate-lead insulation
12 = gate connection
13 = ceramic envelope

1 Triac vs. anti-parallel thyristor pair

The triac, passing current bidirectionally, is an *a.c. power* control device. Its control performance is that of a pair of thyristors in anti-parallel and the following comparisons can be made:

- the triac needs only one heatsink, but this must be large enough to remove the heat caused by the passage of current in both directions
- the triac constitutes a *single* element for a.c. power control
- the triac fuse arrangement is simpler (compare Fig. 1-1*b* with Fig. 1-1*a*)
- the triac has a single gate electrode and can be triggered by a positive or negative signal
- the triac trigger circuit must be designed with care: because the triac can conduct with either polarity of a.c. input voltage, unwanted conduction, i.e. loss of control, results when triggering lasts too long.

Table 1-1 shows the available triac types.

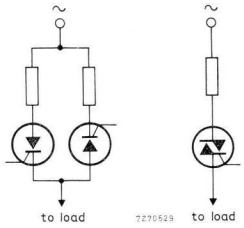


Fig.1-1 Fuse arrangement: (a) anti-parallel thyristors, (b) triacs.

Table 1-1 Available triac types

series	current rating at 85 °C mounting-base temperature	repetitive peak voltage rating
BTW43	12 A r.m.s.	600 V to 1200 V
BTX94	25 A r.m.s.	400 V to 1200 V
BTW34	45 A r.m.s.	600 V to 1600 V

2 Build-up

2.1. Basic structure

A triac can be considered, in most respects, to be similar to an anti-parallel pair of thyristors, so the basic crystal structure without gate is as shown in Fig. 2-1. (The equivalent thyristor circuit is shown for comparison.) The lower metal plate covers the entire lower surface of the crystal but the upper plate covers only about half of the top surface (Fig. 2-2; crystal seen from above) to leave room for a gate electrode.

If a metal electrode is placed directly on the exposed portion of the upper p-region to form a gate, it becomes difficult to trigger the device because there is a low-resistance path between gate and upper electrode. For triggering to occur, the current I_{gate} flowing along this path must be sufficient to develop the forward voltage (about 0,8 V) required for current flow to the upper cathode. Such a gate current is prohibitively large.

However, by diffusing a further n region into the p region, as shown in Fig. 2-3, the gate can be so placed that the path of I_{gate} is long enough for reasonable values of I_{gate} to develop 0,8 V along it and thus bring about gate-to-cathode conduction. To allow positive and negative triggering in both quadrants (Section 3.2.1), the gate metallization is extended over the additional n region. Fig. 2-4 shows one possible triac structure.

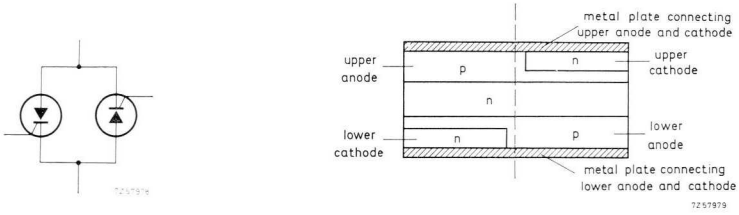


Fig. 2.1 Basic structure without gate.

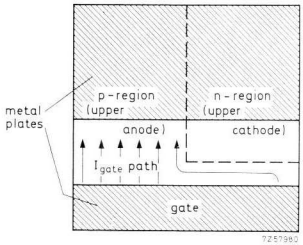


Fig.2-2 Plan view showing almost untriggerable gate arrangement.

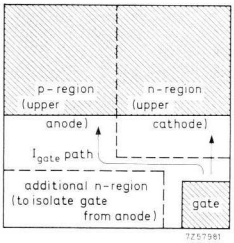


Fig.2-3 Triggerable gate arrangement.

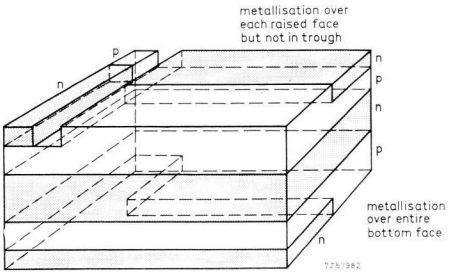


Fig.2-4 Practical structure (square crystal).

2.2 BTX94 and BTW34 construction

The BTX94 and BTW34 have a double-bevel crystal allowing them to withstand up to 1200 V and 1600 V repetitive peak voltage, respectively. Their shorted-emitter structure gives two important advantages: (a) because of the more powerful gate drive required there is better immunity to interference, (b) dv/dt capability (Section 3.2.3) is much increased.

Fig. 2-5 shows the crystal build-up. With *main terminal 2 the more positive*, conduction will be initiated in the gate/cathode area and the triac current after triggering will flow through layers $p_2\ n_2\ p_1\ n_1$ (*right-hand crystal-half conducting*). When the triac voltage reverses, *main terminal 1 becomes the more positive*; conduction will start again in the gate/cathode area, and, when triggering is completed, triac current will flow through layers $p_1\ n_2\ p_2\ n_3$ (*left-hand crystal-half conducting*).

Fig. 2-6 is useful for investigating the turn-on behaviour of a triac with a so-called central gate. The central gate in a thyristor ensures a uniform spread of current over a large portion of the crystal area, so that a high turn-on di/dt causes no damage. Although the gate in the triac is geometrically central, it is eccentric to each of the crystal halves, which alternately conduct during successive half cyces. Fig. 2-7 shows the upper-anode configuration. The p channel establishes direct contact of the gate metallization with the anode region. The restriction (gate resistance) between the n regions ensures triggering at a moderate gate current — see Section 2.1. Triggering can occur with positive as well as negative gate drive.

With positive gate drive — Fig. 2-6*a* — hole current is passed from the p channel to the upper anode via the gate resistance; see arrows. When a sufficient voltage drop (about 0,8 V) is developed across this resistance, the shaded part of the upper-cathode junction becomes forward biased and injects electrons, which triggers the device. The turn-on zone (shown shaded) is near the p channel and will be wider when the p channel is wedge-shaped, as in the case of the BTW34, thus improving the dI_T/dt-capability (Section 3.3.2); see Fig. 2-6*c*.

With negative gate drive — Fig. 2-6*b* — the hole current through the gate resistance reverses, so that, when a sufficient bias is established, it is the gate region that conducts and injects electrons rather than the cathode. Since the gate resistance consists of two parallel sections joined near the p channel

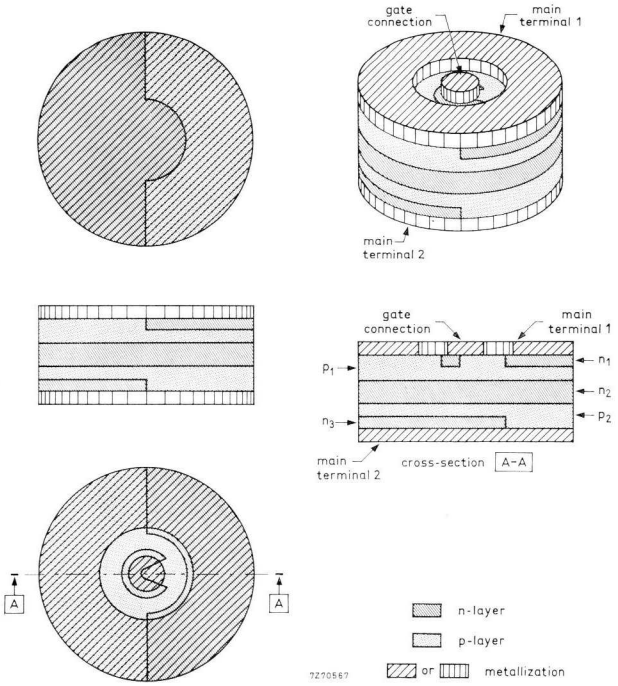


Fig.2-5 BTX94/BTW34 crystal structure (ratio of crystal thickness to diameter much exaggerated).

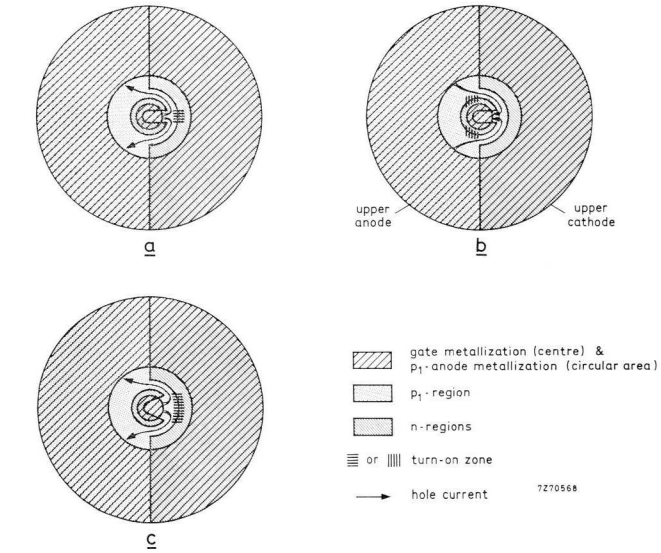


Fig.2-6 Triggering of triac with (a) gate positive, (b) gate negative, (c) gate positive and wedge-shaped *p* channel.

(Fig. 2-7), electron injection, and thus triggering occurs at two points remote from the channel and shown shaded in Fig. 2-6*b*. The device geometry is such that a low gate current suffices for triggering and dv/dt capability is good.

Fig. 2-8*a* illustrates the effect of the thyristor voltage assuming reverse-biasing polarity. Injected charge carriers are attracted back to the cathode, so that the charge is recovered and the thyristor turns off. In the triac — Fig. 2-8*b* — the charge can diffuse from the right-hand thyristor into the base region of the left-hand thyristor. When the triac voltage polarity reverses, some of this charge, as well as some of the charge from the perimeter of the right-hand thyristor, is attracted to the upper anode and can switch on the left-hand thyristor if the voltage rises rapidly. Loss of control will then result. By selecting an optimum geometry, reliable turn-off is obtained for up to 50 A/ms decay rate of commutation current followed by max. 30 V/μs rise rate of re-applied voltage. (Uncontrolled triac turn-on is discussed in Section 3.2.3.)

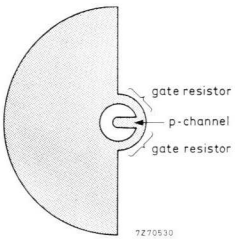


Fig.2-7 Upper-anode configuration (p_1 region). Overall gate resistance is parallel combination of both gate resistors.

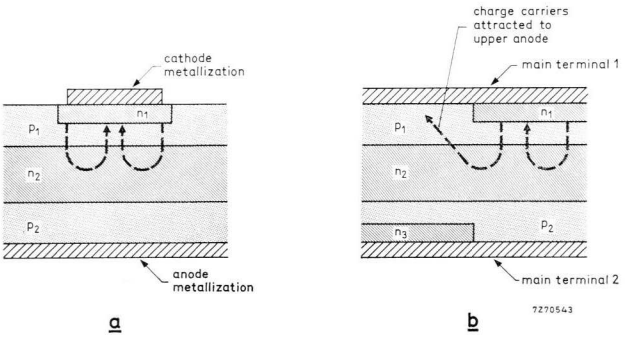


Fig.2-8 Movement of residual charge carriers in (a) thyristor (b) triac.

2.3 BTW43 construction

The BTW43 triac series has the same successful shorted-emitter structure. The crest working voltage rating of up to 800 V makes the BTW43 suitable for all mains-supplied control systems, and the repetitive peak rating of 1200 V ensures ample margin for voltage surges. Fig. 2-9 is a cross section of the unit.

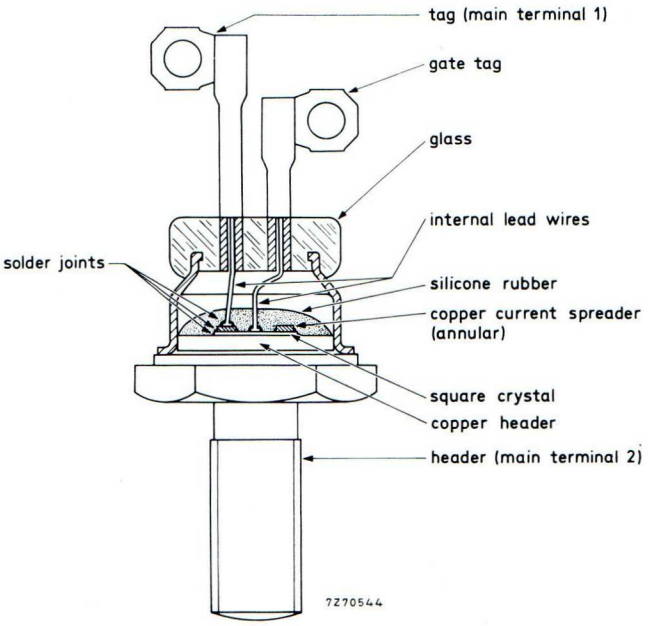
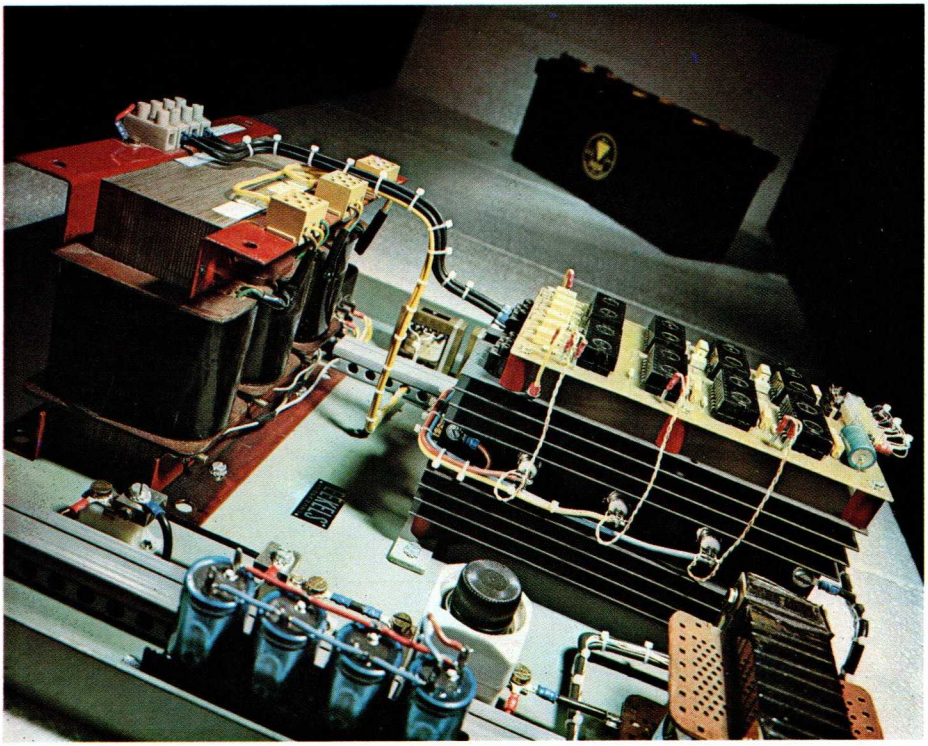


Fig.2-9 BTW43 construction.



2 kVA, 12 V to 120 V traction battery charger.
Courtesy of Messrs. Eekels, Hoogezand, The Netherlands.

100-ton press driven by variable-speed 10 h. p. motor, supplied from a three-phase 12 kVA inverter.

3 Characteristics and ratings

3.1 General

This Section explains characteristics and ratings that require special attention where triacs are concerned. Characteristics and ratings are expressed by the symbols designated in Table 3-1.

Table 3-1 Symbol letter designation code

quantity symbol	1st subscript	2nd subscript	3rd subscript
I = current	(BO) = breakover value	(AV) = average value	M = peak value
P = power	D = off-state (forward blocking)	D = value that will not trigger any device	(RMS) = root-mean-square value
T = temperature	F = forward-biased state (only for gate)	M = peak value	
V = voltage	G = gate	R = repetitive value	
	H = holding value	(RMS) = root-mean-square value	
	j = junction	S = non-repetitive (surge) value	
	L = latching value	T = value that will trigger all devices	
	R = reverse-biased state (only for gate)	W = working value (excluding repetitive and non-repetitive transients)	
	stg = storage condition (non-operational)		
	T = on-state		

3.2 Characteristics

3.2.1 Static current/voltage characteristic

Fig. 3-1 shows the current/voltage relationship and the symbol of the triac. The device has two main terminals: terminal 1 adjacent to the gate electrode, and terminal 2 on the other side of the crystal. Operation in quadrant 1 occurs

when main terminal 2 has the higher potential, and operation in quadrant 3 occurs when main terminal 1 has the higher potential. Note that operation is possible only in quadrants 1 and 3. The single gate electrode controls the conduction in both directions, and triggering occurs with a gate signal of sufficient magnitude and of either polarity.

The triac characteristic is that of two thyristors in anti-parallel. Without a gate signal, the triac is in the off-state and a low current — *leakage* current — flows through the device. With a gate signal, the triac voltage collapses (see dotted characteristics) and turn-on follows as soon as the triac current, flowing in either direction, exceeds the *latching* (*pick-up*) level I_{L1} or I_{L3}. (The values of latching current occurring in quadrants 1 and 3 are not necessarily equal, they depend on the polarity of the gate signal.) The triac turns off when its current falls below the *holding* level I_{H1} or I_{H3} (lower than latching level), that is, the on-state characteristics terminate at the holding current value.

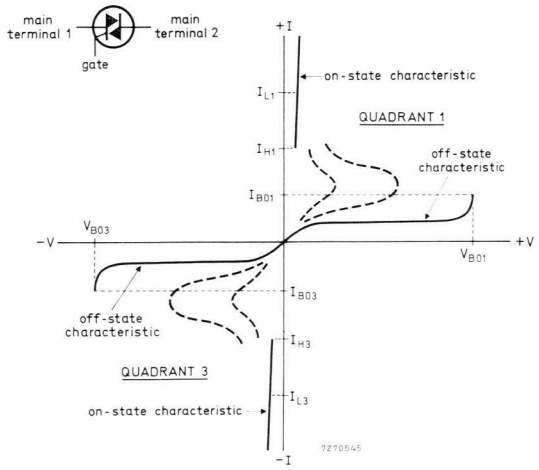


Fig.3-1 Static current/voltage characteristic and triac symbol. Dotted curves show the gradual collapse of triac voltage as a result of a positive or negative gate drive.
$V_{BO1,3}$ = breakover voltages
$I_{BO,13}$ = breakover currents
$I_{L1,3}$ = latching currents
$I_{H1,3}$ = holding currents.

The triac can also be made to turn on by excessive voltage between its main terminals. This phenomenon is called *breakover*. The voltages and currents at which breakover occurs are respectively labelled V_{BO1} V_{BO3} and I_{BO1} I_{BO3} in the diagram.

3.2.2 THERMAL RESISTANCE[1])

$R_{th\ j-mb}$ is the junction-to-mounting base or device thermal resistance. Because only half of the triac crystal conducts in the case of uni-directional operation (controlled rectification), the value of the device thermal resistance is twice that for bi-directional operation (a.c. power control). Normally, $R_{th\ j-mb}$ is specified for uni-directional as well as bi-directional operation.

$Z_{th\ j-mb}$ is the junction-to-mounting base thermal impedance. This quantity is of importance for pulsed loading (intermittent flow of load current). Fig. 3-2 shows the transient thermal impedance as a function of time. For a very short power pulse, $Z_{th\ j-mb}$ is low, and the junction temperature of the triac therefore hardly rises. For a long pulse, $Z_{th\ j-mb}$ approaches the static value $R_{th\ j-mb}$. As in the case of thermal resistance, the transient thermal impedance for uni-directional operation is twice that for bi-directional operation.

3.2.3 VOLTAGE

$\mathrm{d}V_D/\mathrm{d}t$ is the rise rate of voltage (either polarity) across the non-conducting device. When the voltage rise rate is high, uncontrolled turn-on can result. Distinction is made between $\mathrm{d}V_D/\mathrm{d}t$ applied to a device in the off-state (not conducting previously) and a turned-off device (conducting previously). The voltage ramp function applied to a *device in the off-state* causes the junction capacitance C_j to be charged by a current equal to C_j $(\mathrm{d}V_D/\mathrm{d}t)$. If the charge current is high enough, the triac is triggered into conduction. In a *turned-off device*, there are still charge carriers unrecombined after previous conduction. Their number is large if the decay rate of commutation current is high, and a small value of $\mathrm{d}V_D/\mathrm{d}t$ can then induce a high current in the triac. To prevent uncontrolled turn-on, the decay rate of commutation current and the rise rate of re-applied voltage must both be held below specified limits. Owing to the

[1]) Application Book: Rectifier Diodes, Chapter 3; ordering code 9399 256 01001.

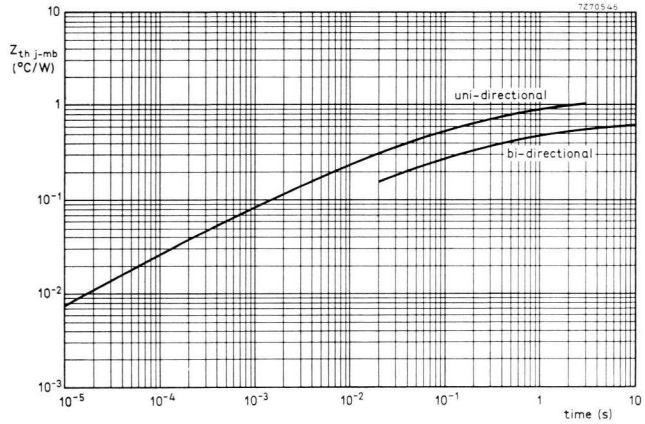


Fig.3-2 Transient thermal impedance of BTW34.

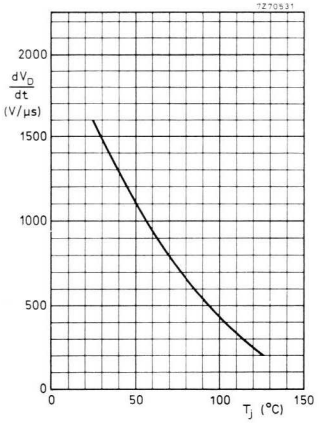


Fig.3-3 dV_D/dt capability of BTW34 in the off-state.

presence of the charge carriers, the maximum non-triggering voltage rise rate is lower for a turned-off device than for a device in the off-state. For the BTW34 having 125 °C junction temperature, the maximum non-triggering rise rate of off-state voltage is 200 V/μs for any device; the maximum non-triggering rise rate of voltage re-applied after turn-off is 30 V/μs for a 50 A/ms current decay rate. The dV_D/dt capability depends on the junction temperature — see Fig. 3-3.

V_{GT}, $-V_{GT}$ are the minimum gate voltages for reliably triggering any device in the series. V_{GT} refers to a signal that makes the gate positive with respect to terminal 1 and $-V_{GT}$ refers to a signal that makes the gate negative with respect to terminal 1. Because the values of V_{GT} and $-V_{GT}$ increase when the junction temperature falls, a lower junction temperature necessitates more powerful triggering.

3.2.4 Current

I_L is the latching current, that is, the minimum current that will cause the device to conduct. Gate drive must be sustained until the triac current has reached this level, otherwise turn-off will occur. The expected maximum latching current is specified for a positive and a negative gate drive and for the first and third quadrant.

I_H is the holding current. Conduction ceases if the triac current falls below this level. The expected maximum holding current (positive or negative gate drive) is specified for the first and third quadrants.

I_{GT}, $-I_{GT}$ are the minimum gate currents that will reliably trigger any device in the series; I_{GT} refers to the current fed into the gate, and $-I_{GT}$ to the current extracted from the gate. Because the values of I_{GT} and $-I_{GT}$ increase when the junction temperature falls, a lower junction temperature necessitates more powerful triggering.

3.2.5 Power dissipation

Power dissipation is due to the on-state voltage loss, gate losses, leakage in the off-state and switching losses. The power dissipation is a function of r.m.s. on-state current and conduction angle. Fig. 3-4 is a plot of the *expected maximum* power dissipation P versus r.m.s. current $I_{T(RMS)}$ (a.c. operation). The power dissipation raises the junction temperature; the right-hand section in the graph is used for calculating the heatsink thermal resistance required to limit the junction temperature to the rated value of 125 °C (temperature of mounting base related to that of junction). Section 8.2 gives an example of calculation. Plots similar to Fig. 3-4 are published for half-wave operation.

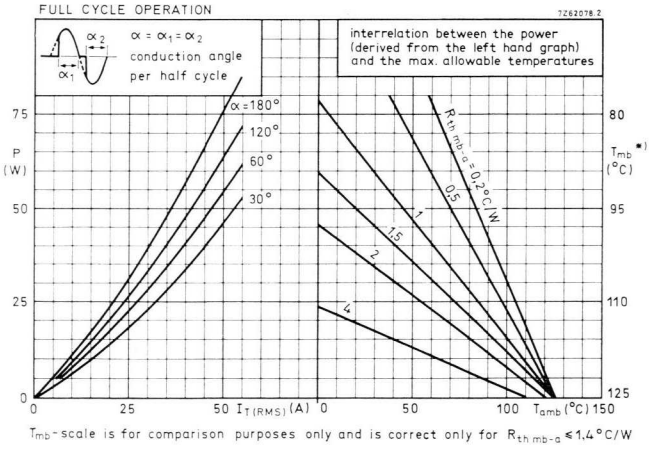


Fig.3-4 Power dissipation in BTW34 for full-cycle 50 Hz operation.

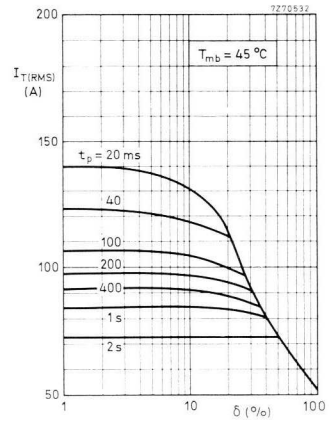
3.3 Ratings

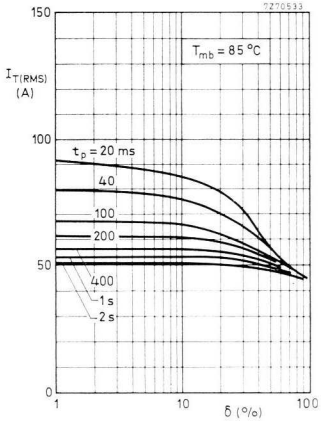
3.3.1 Voltage

The triac has no reverse voltage rating because it can conduct with either polarity of voltage applied. Like thyristors, triacs are classified according to their *repetitive peak* voltage rating.

3.3.2 CURRENT

$I_{T(RMS)\ max}$ (r.m.s. on-state current) refers to the r.m.s. value of a sinusoidal current under continuous load. Fig. 3-5 shows the BTW34 intermittent current rating for the mounting-base temperature T_{mb} equal to 45 °C or 85 °C. Fig. 3-6 gives the BTW34 inrush current rating, important for a motor or incandescent lamp load. The inrush current time function must lie below the illustrated plot. For instance, for 85 °C mounting-base temperature, the first-cycle r.m.s. current may amount to 113 A, but at the end of the fifth cycle (0,1 s) it must have fallen to 82 A. The allowable steady-state r.m.s. current read from the plot is 45 A, quite in accordance with the continuous r.m.s. current rating. The plot is valid for a "*cooled down*" device (junction temperature T_j equal to mounting-base temperature T_{mb}), that is, the current must not start to flow until a few seconds after previous conduction.





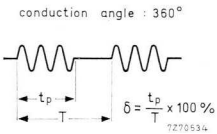


Fig.3-5 BTW34 current rating for intermittent loading.
δ = duty cycle,
t_p = conduction period.

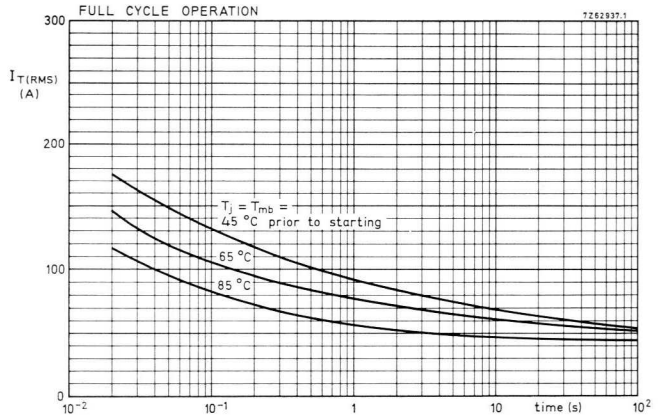
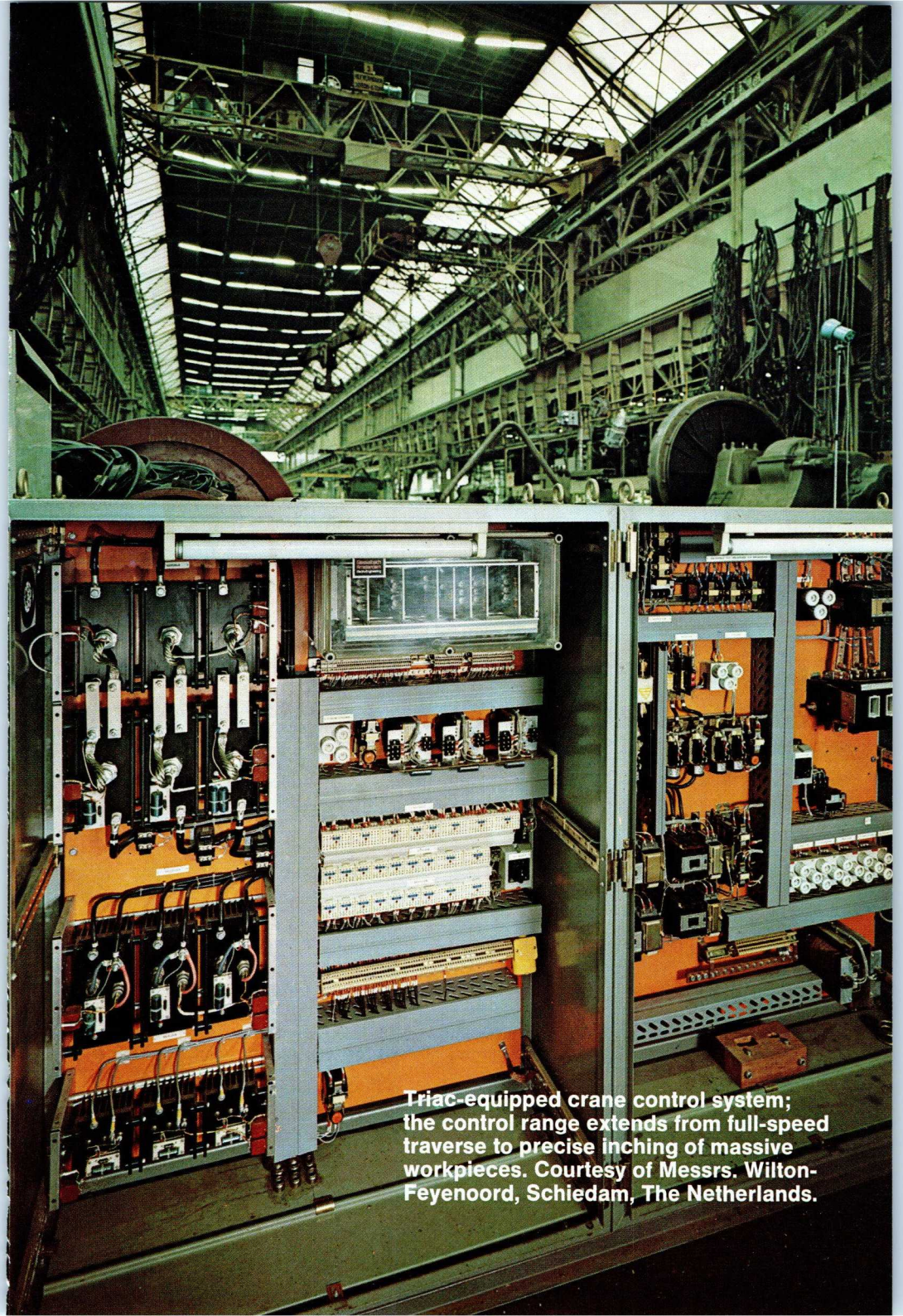


Fig.3-6 BTW34 inrush (starting) current rating for full-cycle, 50 Hz operation.

$I_{TSM\ max}$ (peak surge or non-repetitive peak on-state current) refers to the peak value of a semi-sinusoidal or sinusoidal overload current. The rating curve of Fig. 3-7 shows the allowed non-repetitive *r.m.s.* surge current $I_{TS(RMS)}$ integrated over *one-half sinusoid* of current. For a surge duration of less than 10 ms (operation from a 50 Hz mains), a single semi-sinusoid of current lasting less than one-half cycle is assumed to flow. For surge duration t between 10 ms and 20 ms, an opposite half-sinusoid of current flowing through the other half of the triac crystal is added, but the overload on the crystal-half already in conduction does not change; consequently, that particular part of the overload rating curve is horizontal. For any surge duration longer than 10 ms, equal-amplitude current pulses are assumed — see inset. It should be noted that temporary loss of power control may occur after an overload. The non-repetitive rating is important for protection by means of fuses.



Triac-equipped crane control system; the control range extends from full-speed traverse to precise inching of massive workpieces. Courtesy of Messrs. Wilton-Feyenoord, Schiedam, The Netherlands.

$(dI_T/dt)_{max}$ refers to the rise rate of on-state current. Because the current spreads with finite velocity from the gate area across the entire crystal cross section, hot spots would occur locally if the current rise rate were excessive. The dI_T/dt rating is established for protection against this type of overload. The spreading velocity, and so the dI_T/dt capability, increases with the rate of rise and the level of gate current; the dI_T/dt rating is given for specified values of gate current I_G, on-state current I_T, and often rise rate of gate current. If the device is turned on by breakover, the permitted dI_T/dt is generally lower.

Series chokes are usually needed to reduce the decay rate, $-dI/dt$, of the commutation current to a value allowing safe turn-off (see Section 3.2.3); this value is a few orders of magnitude smaller than the turn-on dI_T/dt rating.

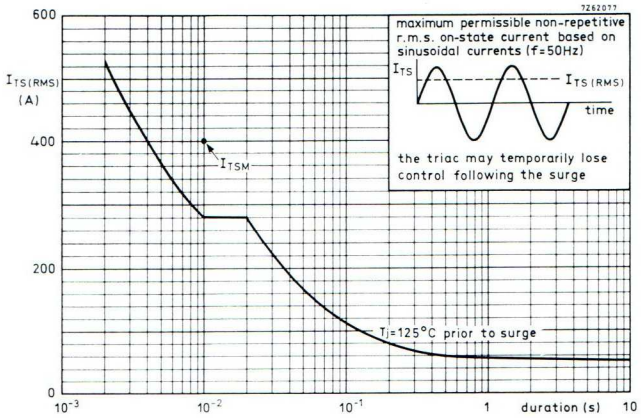


Fig.3-7 BTW34 non-repetitive current rating for sinusoidal, 50 Hz operation (equal sinusoids for any overload duration). I_{TSM} = peak value allowed for semi-sinusoidal current lasting 10 ms.

4 Triggering

4.1 Trigger modes

The figures in this chapter illustrate the four trigger modes and show an appropriate cross section of the triac crystal (either through the p region or the n region of the gate). Reverse or forward bias at junctions is shown by the letters R and F, and polarity of gate signals is shown by plus, or minus signs.

First quadrant, positive triggering (Fig. 4-1). The gate-cathode junction p_1n_3 is forward biased and electrons from n_3 are collected by the n_1 region. These lower the potential of the n_1 region thus providing more forward bias for the p_2n_1 junction. Holes from p_2 reach the n_1 region and are collected by p_1, and the triac switches on as a normal thyristor.

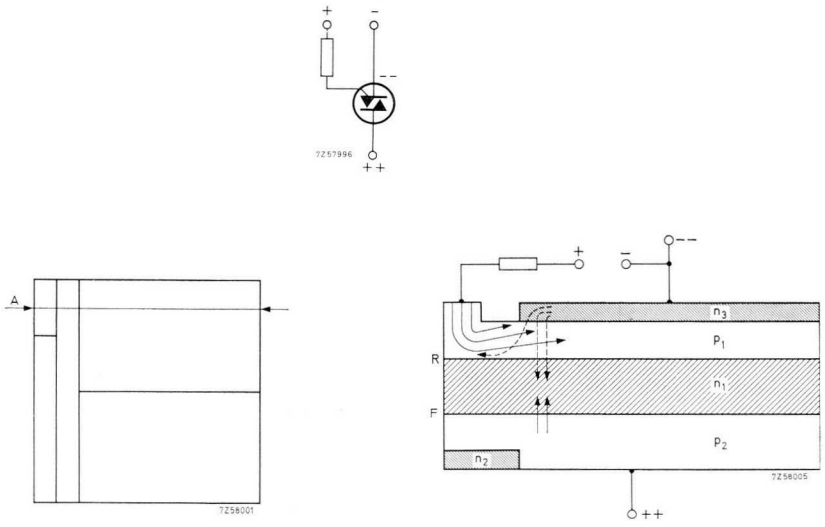


Fig.4-1 First-quadrant positive triggering.

First quadrant, negative triggering (Fig. 4-2). Forward bias is applied to the gate-cathode junction p_1n_4. Electrons from n_4 are collected by the n_1 region and lower the potential there. Thus, the p_2n_1 junction becomes more forward biased. Holes from p_2 reach the n_1 region and are collected by p_1. Junction p_1n_3 becomes forward biased and the triac switches on (as a thyristor with a junction gate).

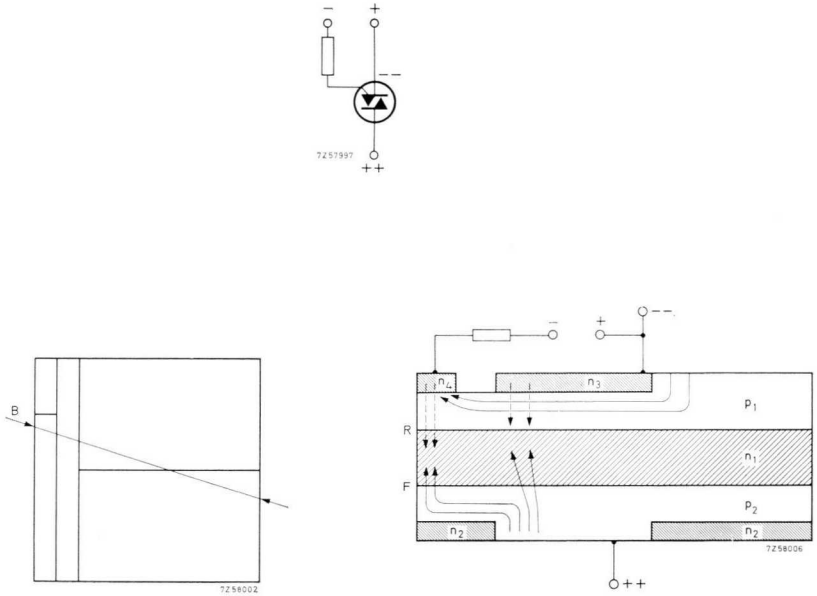


Fig.4-2 First-quadrant negative triggering.

Third quadrant, positive triggering (Fig. 4-3). The gate-cathode junction p_1n_3 is forward biased. Electrons reach n_1, which becomes more negative. Hole current from to p_1 to n_1 increases and the holes in n_1 are collected by p_2; this hole flow causes n_2 to emit electrons (p_2n_2 junction forward biased) and these are collected by n_1. Current flows down the left-hand side of the crystal, and, if sufficient current can flow in the main circuit, the right-hand side then switches on (triac switching on as a thyristor with a remote gate).

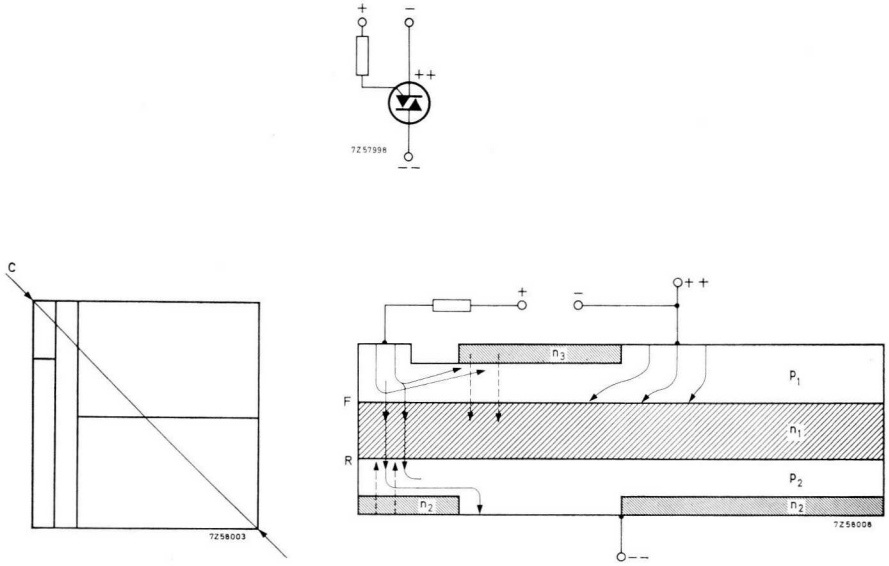


Fig.4-3 Third-quadrant positive triggering.

Third quadrant, negative triggering (Fig. 4-4). The gate-cathode junction p_1n_4 is forward biased and electrons reach n_1, lowering the potential there. The flow of holes from p_1 to n_1 increases and the holes in n_1 are collected by p_2. Electrons are emitted by n_2 as a result of the flow of holes and are collected by n_1. Current flows down the left-hand side of the crystal, and, if sufficient current can flow in the main circuit, the triac switches on (as a thyristor with a remote gate).

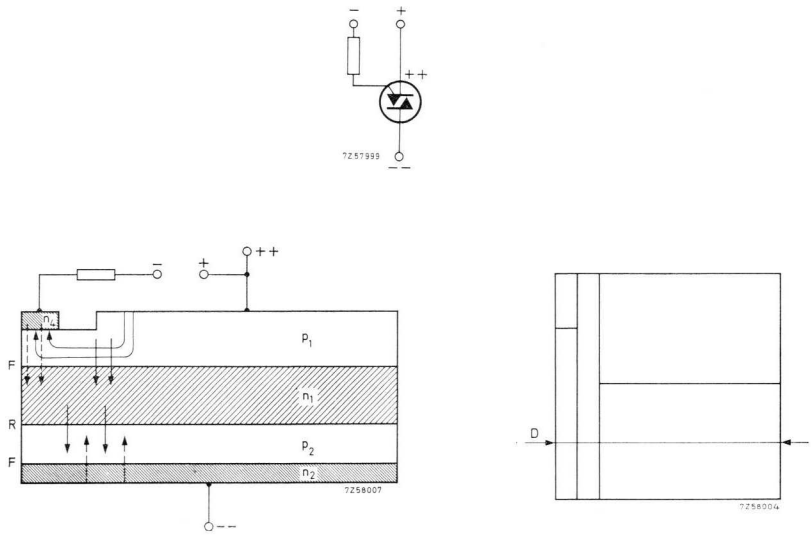


Fig.4-4 Third-quadrant negative triggering.

4.2 Gate forward characteristic

Fig. 4-5 illustrates the boundary curves of the spread in gate forward characteristic for the BTX94 (25 °C junction temperature). The triac can be triggered by either a positive or a negative gate signal (polarity of gate signal referred to terminal 1). The areas of certain triggering (shown hatched) are given for both cases, i.e. $+I_G + V_G$ and $-I_G - V_G$, and for operation in the first quadrant ("terminal 2 positive") and in the third quadrant ("terminal 2 negative"). To ensure turn-on, operation must occur outside the areas of uncertain triggering.

It follows that triggering with a *negative* signal is preferable when the trigger power is limited. Another motive for favouring a negative signal is explained in Section 4.3.

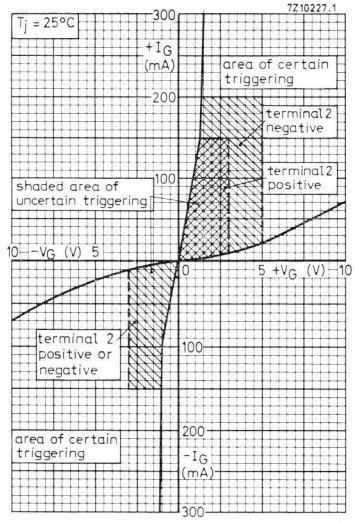


Fig.4-5 BTX94 gate characteristics.

4.3 Trigger signal

Magnitude. This was discussed in the previous Section.

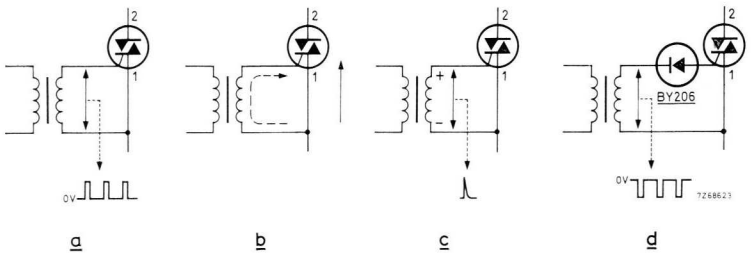


Fig.4-6 Gate coupling to (a)(b)(c) positive trigger source (d) negative trigger source.

Polarity. The gate can be driven by a positive or a negative signal. Fig. 4-6*a* illustrates the former case. With the main current flowing into terminal 1 (solid arrow in Fig. 4-6*b*), a parallel gate current can occur (see dashed arrow). The parallel gate current has two undesirable effects. Firstly, it can saturate the trigger transformer. Secondly, during turn-off the parallel current will cease fairly abruptly; the induced voltage spike (Fig. 4-6*c*) re-triggers the triac, and uncontrolled conduction results. These deficiencies are overcome by using a negative gate drive; see Fig. 4-6*d*. The BY206 blocks the parallel current. (The diode would, of course, pass any opposite parallel gate current, but this current cannot flow because, when the main current flows from terminal 2 to terminal 1, there is a very high main path-to-gate path isolation resistance.)

Duration. Like thyristors, it is advantageous to trigger triacs with a pulsating signal. To ensure bi-directional conduction, even with a very inductive load, the trigger pulses must continue until the end of the half cycles. If single trigger pulses are used, one-way conduction (rectification) results when the trigger angle is smaller than the load phase angle. See Fig. 4-7, waveform *A*. The triac is triggered at times t_1 t_3, and the pulses occurring at times t_2 t_4 have no effect because the triac is still conducting. Thus, one-way current pulses flow saturating the load inductance. When using a trigger pulse train (waveform *B*), a sinusoidal current flows with a phase delay equal to that of the load phase angle, even if the trigger pulses start at zero degrees. A trigger source producing pulse trains that continue until the end of the half cycles will also cope with inrush conditions (Figs 4-8 and 4-9); single pulses cause rectification. The trigger pulse train must cease *before* the mains voltage passes through zero; otherwise the triac will continue to conduct (loss of control). It must be noted that a continuous pulse (so called *d.c. triggering*) causes more gate dissipation than a pulse train).

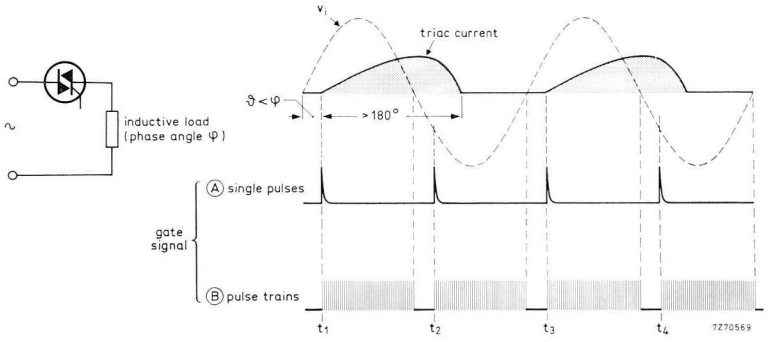


Fig.4-7 Rectification in a.c. controller;
ϑ = trigger angle, φ = load phase angle.

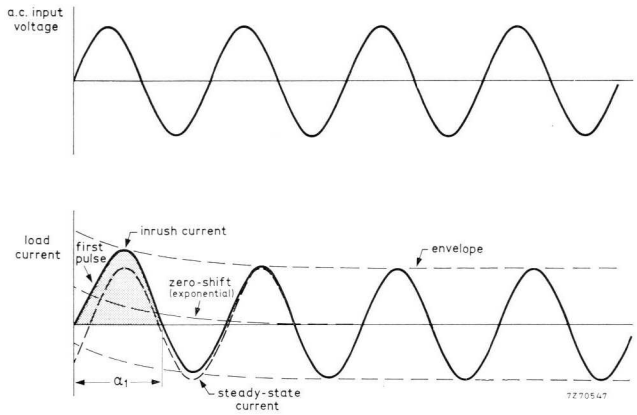


Fig.4-8 Inrush phenomenon in a.c. controller (zero trigger angle); for α_1 see Fig.4-9.

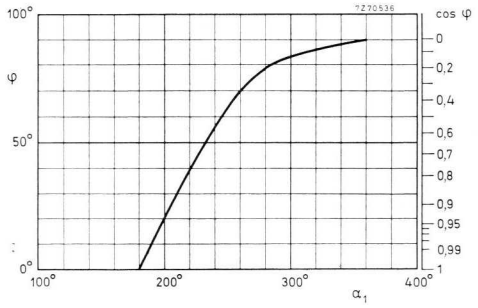


Fig.4-9 First-pulse length α_1 (Fig.4-8) vs. load phase angle φ.

5 How to obtain reliable turn-off

5.1 Chokes needed to "soften" commutation

Unlike the thyristor, the triac can conduct irrespective of the polarity of the applied voltage. That is, the triac experiences no circuit-imposed turn-off time allowing its recovery before voltage is re-applied. Triac-controlled circuits therefore require careful design.

Triac control of a transformer supplying an inductively-loaded diode bridge is notorious for the problems it can cause[2]). Fig. 5-1 shows the situation. The load inductance forces the rectifier diodes into conduction as soon as the instantaneous d.c. output voltage becomes negative. So the transformer secondary is shorted for some time after the zero transition of the mains voltage and a reversed voltage is applied to the triac, turning it off. Because of the transformer leakage inductance, the triac does not turn off immediately, but continues to conduct over what is called the *commutation interval* (see i_T-waveform). During this interval, a high decay rate, $(di/dt)_{com}$, of current results for two reasons.

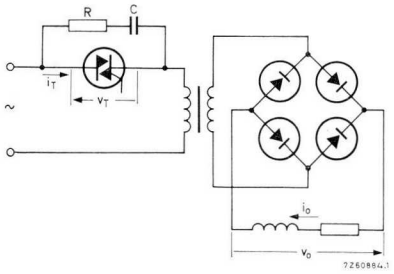
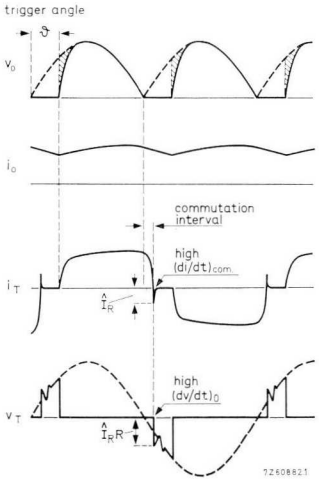


Fig.5-1 "Hard" commutation.



[2]) AN No. 127: Triac Control of D.C. Inductive Loads; ordering code 9399 250 62701.

Firstly, the transformer leakage inductances is low. (This is necessary for minimum d.c. output voltage loss — see the hatched areas in the waveform for v_o.) Secondly, with an inductive rectifier load, a substantial current flows when commutation starts. Because the current decays rapidly, the peak reverse recovery current $\hat{I}_R$ is fairly large. At turn-off, $\hat{I}_R$ is abruptly transferred to the transient suppression elements R and C, so the voltage suddenly rises to the level $I_R \times R$ (C uncharged initially). Owing to the high value of both $(\mathrm{d}i/\mathrm{d}t)_{com}$ and $(\mathrm{d}v/\mathrm{d}t)_0$, turn-on causing loss of control can ensue (see Section 3.2.3, "$\mathrm{d}V_D/\mathrm{d}t$").

A saturable choke in series with the transformer primary reduces $(\mathrm{d}i/\mathrm{d}t)_{com}$, thus preventing uncontrolled turn-on. See Fig. 5-2. Saturation must occur at a fraction of the rated load current so that there is little loss in the output voltage of the rectifier (hatched v_o-areas). Another advantage of the saturable choke is that it has little effect on the power factor. At low current, a high inductance is available that "softens" commutation. The choke delays the voltage rise so a quiescent period of a few tens of microseconds is interposed during which the triac can recover[3]). The inductance of the choke is calculated from the formulae in Section 5.2.

The decay rate of the commutation current depends on the mains frequency, d.c. output current, trigger angle, rectifier constant[4]) and transformer fractional reactance. The three-phase bridge has the lowest rectifier constant and causes the "hardest" commutation. Fig. 5-3*a* is the circuit, and Fig. 5-3*b* is a plot of the decay rate of commutation current $(\mathrm{d}i/\mathrm{d}t)_{com}$ versus total angle $\vartheta + \gamma_c$. For $0° < \vartheta + \gamma_c < 60°$, current commutates between triacs and $(\mathrm{d}i/\mathrm{d}t)_{com}$ is part of a sine function. For $\vartheta + \gamma_c > 60°$, the d.c. output voltage becomes intermittent and the current is transferred from the triac in conduction to one pair of bridge diodes whenever the instantaneous bridge output voltage becomes zero. The instants of current transfer do not shift with the trigger angle, the

[3]) Elektronik 1970, Heft 5, pp. 161 to 164, K. Brückmüller — Steuerung induktiver Verbraucher mit Triacs.

[4]) Application Book: Rectifier Diodes, Chapter 9; ordering code 9399 256 01001.

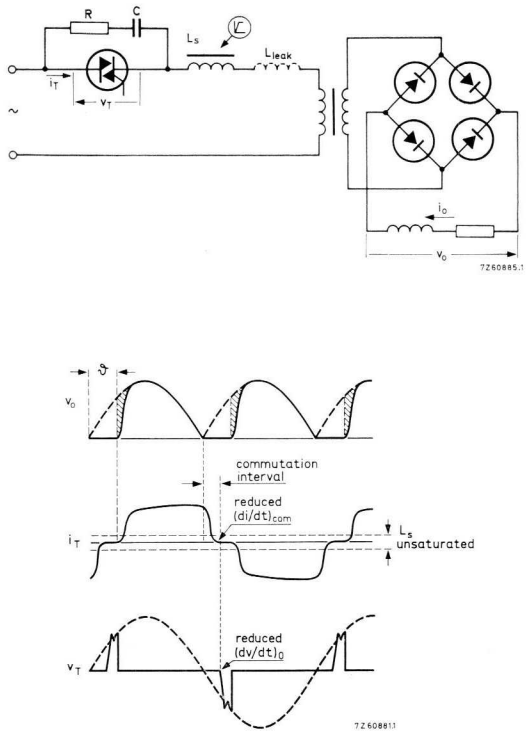


Fig.5-2 Use of saturable choke to "soften" commutation.

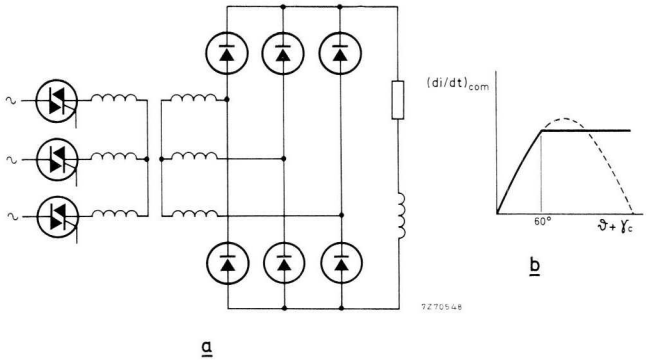


Fig.5-3 Circuit causing the "hardest" commutation. ϑ = trigger angle, γ_c = angle of commutation interval; (a) circuit diagram, (b) plot of commutation current decay rate.

commutation voltage remains the same and the function $(di/dt)_{com}$ vs. $\vartheta + \gamma_c$ becomes a horizontal line: maximum $(di/dt)_{com}$. Fig. 5-4 is a plot of the ratio of maximum $(di/dt)_{com}$ to r.m.s. triac current $I_{T(RMS)}$ versus transformer fractional reactance x. Series inductance is generally required to reduce $(di/dt)_{com}$ to an acceptable level — see Section 5.2.

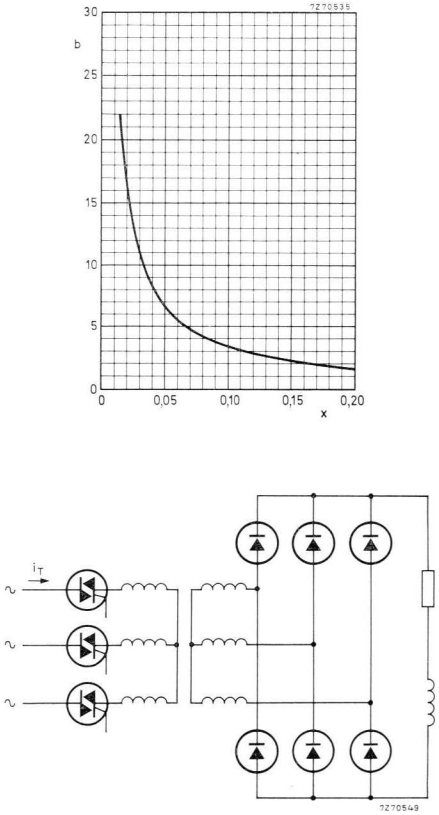


Fig.5-4 $b = \max (di/dt)_{com}/I_{T(RMS)}$ (ms^{-1}) vs. transformer fractional reactance x for circuit shown in diagram.

5.2 Formulae for choke calculation

The inductance of the saturable series choke L_s required for reliable turn-off is derived from the formulae given here for a few practical circuits. The nomenclature, together with the units recommended for ease of calculation, is:

L_s = inductance of series choke (mH)
L_t = total series inductance (mH)
L_{leak} = transformer leakage inductance (mH)
L_m = motor inductance (mH)
L_{add} = series inductance to be added (mH)
$(-\mathrm{d}I_T/\mathrm{d}t)_{max}$ = recommended maximum decay rate of commutation current for ensuring reliable turn-off (mA/s)
x = transformer reactance (fractional)
kVA_{rated} = transformer rating (kVA)
ω = $2\pi \times$ mains frequency (Hz)
V_{LL} = r.m.s. line-line voltage (V)

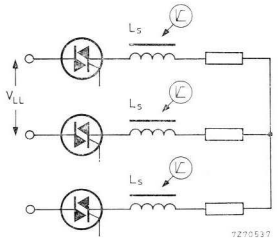


Fig.5-5 Three-phase controller with resistive load (star or delta).

Three-phase controller with resistive load (Fig. 5-5)

$$L_s \geqslant \frac{V_{LL}}{(-\mathrm{d}I_T/\mathrm{d}t)_{max} \cdot \sqrt{6}}. \tag{5-1}$$

Three-phase controller with transformer and resistive load (Fig. 5-6)

$$L_{leak} = \frac{x\, V_{LL}^2}{\omega \cdot kVA_{rated}}, \tag{5-2}$$

$$L_t \geqslant \frac{V_{LL}}{(-\mathrm{d}I_T/\mathrm{d}t)_{max} \cdot \sqrt{6}}, \tag{5-3}$$

$$L_{add} = L_t - L_{leak}. \tag{5-4}$$

To prevent saturation of the transformer core, the transformer must be preloaded to about 10% of full load; this also eliminates the necessity for RC elements across the transformer primary windings to promote triac turn-on[5]).

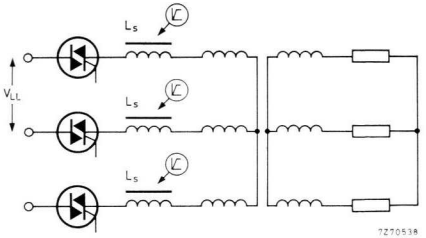


Fig.5-6 Three-phase controller with transformer (star- or delta-connected) and resistive load.

Three-phase controller with transformer and inductively-loaded bridge rectifier (Fig. 5-7)

$$L_{leak} = \frac{x\, V_{LL}^2}{\omega \cdot kVA_{rated}}. \tag{5-5}$$

[5]) AI No. 336: Thyristors and Triacs in Temperature Control Systems; ordering code 9399 214 33601.

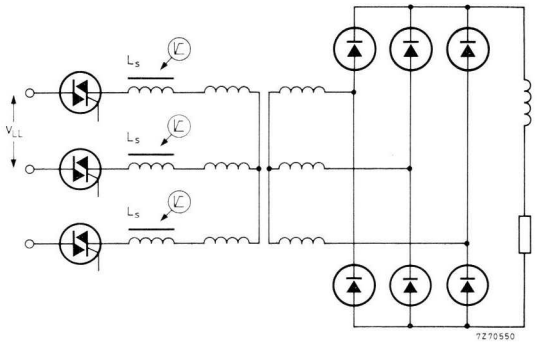


Fig.5-7 Three-phase controller with transformer (star- or delta-connected) and inductively loaded bridge rectifier.

For triac-triac commutation ($0° < \vartheta < 60°$):

$$L_{t1} \geqslant \frac{3\,V_{LL}}{(-\mathrm{d}I_T/\mathrm{d}t)_{max} \cdot 2\sqrt{6}}, \tag{5-6}$$

$$L_{add1} = L_{t1} - L_{leak}. \tag{5-7}$$

For triac-diode commutation ($\vartheta > 60°$):

$$L_{t2} \geqslant \frac{\omega \cdot kVA_{rated}}{(-\mathrm{d}I_T/\mathrm{d}t)_{max}{}^2}, \tag{5-8}$$

$$L_{add2} = L_{t2} - L_{leak}. \tag{5-9}$$

Use the larger of the two values calculated.

To prevent saturation of the transformer core, the rectifier must be pre-loaded to about 10% of full load; RC-elements across the transformer windings are omitted.

Three-phase motor load

$$L_t \geqslant \frac{V_{LL}}{(-\mathrm{d}I_T/\mathrm{d}t)_{max} \cdot \sqrt{6}}, \tag{5-10}$$

$$L_{add} = L_t - L_m. \tag{5-11}$$

Triac control is suitable for motors driving a load that is some exponential function of motor speed (fan, centrifugal pump, etc.). The d.c. control voltage is applied via an RC network, so that it can only change slowly and motor saturation is avoided.

Calculation example

A 10 kVA three-phase transformer, with a fractional reactance of 0,06, supplies a diode bridge; the phase-phase input voltage is 380 V, 50 Hz. Calculate the inductance of the series chokes.

$$\text{Eq. (5-5):}\quad L_{leak} = \frac{0{,}06 \times 380^2}{314 \times 10} = 2{,}75 \text{ mH}.$$

The phase current at full output is:

$$I_L = \frac{VA_{rated}}{V_{LL}\sqrt{3}} = \frac{10\,000}{380\sqrt{3}} = 15{,}2 \text{ A}.$$

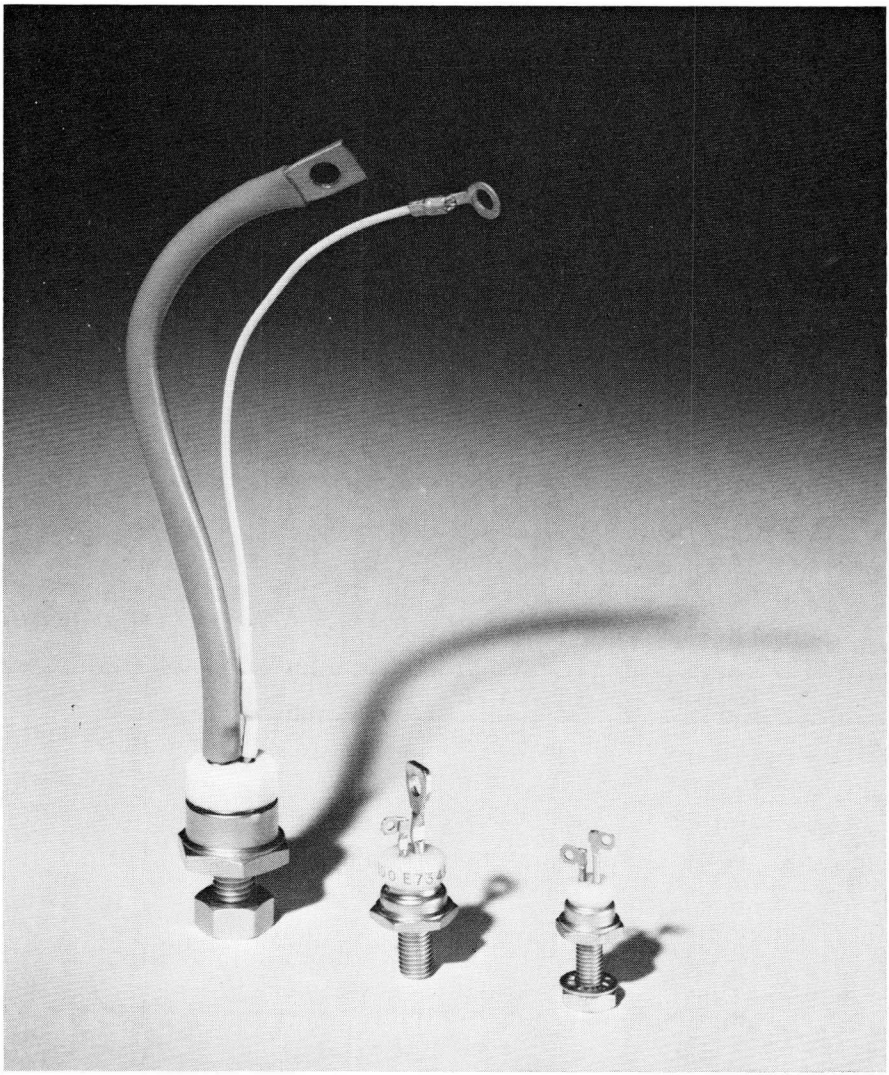
BTX94 triacs will suffice; the recommended value of $(-\mathrm{d}I_T/\mathrm{d}t)_{max}$ is 50 A/ms.

$$\text{Eq. (5-6):}\quad L_{t1} \geqslant \frac{3 \times 380}{50 \times 2\sqrt{6}} = 4{,}65 \text{ mH}$$

$$\text{Eq. (5-8):}\quad L_{t2} \geqslant \frac{314 \times 10}{50^2} = 1{,}26 \text{ mH}$$

The larger value must be taken, so the inductance of the series chokes is calculated from eq. (5-7):

$$L_{add} = 4{,}65 - 2{,}75 = 1{,}9 \text{ mH}.$$



The triac family. From left to right: BTW 34, BTX 94, BTW 43.

6 Voltage transient protection

Transients on the mains voltage cause undesirable triggering when the break-over voltage or the recommended maximum rate of voltage rise is exceeded. With an incandescent lamp or motor load the resulting inrush current can be dangerous.

Transients originate from lightning flashes, switching in adjacent circuitry, etc. or they can be caused by the contactor, which is included in the triac controller itself for safe isolation. When the contactor closes, the triac voltage can rise at a rate of 1000 V/μs! Transients can be suppressed by an *LC* input filter, diode clippers, surge arresting diodes, voltage dependent resistors, etc.

The circuits of Figs 6-1 and 6-2 (compare with Table 6-1) use a diode bridge for transient clipping. When a transient occurs, the diodes conduct and the transient energy is stored in the polarized capacitor; the 10 nF by-pass capacitor handles high-frequency components in the transient. Resistor R_1 limits the capacitor charge current to a value less than the repetitive current rating.

Tabel 6-1 Suggested components for transient suppression; available type numbers specified in last column.

fig.	component	specification	type number
6-1	R_1	10 Ω, 2 W, 10%	2322 215 13109
	R_2	27 kΩ, 4 W, 10%	2322 330 32273
	R_3	33 Ω, 2 W, 10%	2322 215 13339
	C_1	5 μF, 350 V d.c., −10%/+30%	2222 040 15508
	C_2	10 nF, 400 V, 20%	2222 341 58103
	C_3	0,15 μF, 1000 V, 20%	2222 341 70154
	L_1	see Section 5.2	
	D_1 to D_4		BYX45-800R
6-2	R_1	22 Ω, 4 W, 10%	2322 325 36229
	$R_{2a} = R_{2b}$	18 kΩ, 4 W, 10%	2322 330 32183
	R_3	33 Ω, 2 W, 10%	2322 215 13339
	$C_{1a} = C_{1b}$	20 μF, 350 V d.c., −10%/+30%	2222 040 15209
	C_2	10 nF, 1000 V, 20%	2222 341 70103
	C_3	0,15 μF, 1000 V, 20%	2222 341 70154
	L_1	see Section 5.2	
	D_1 to D_6		BYX45-1000R

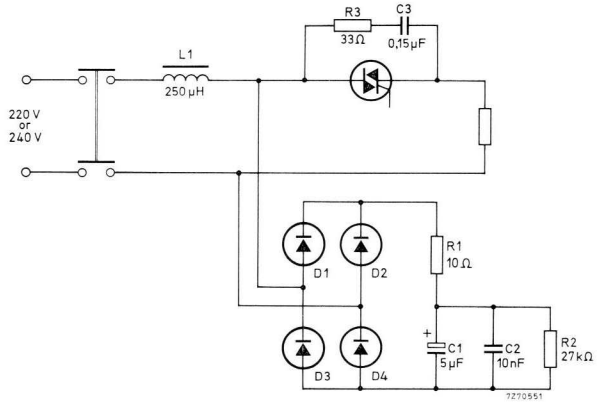


Fig.6-1 Single-phase transient suppression scheme (see Table 6-1) using transient clipper.

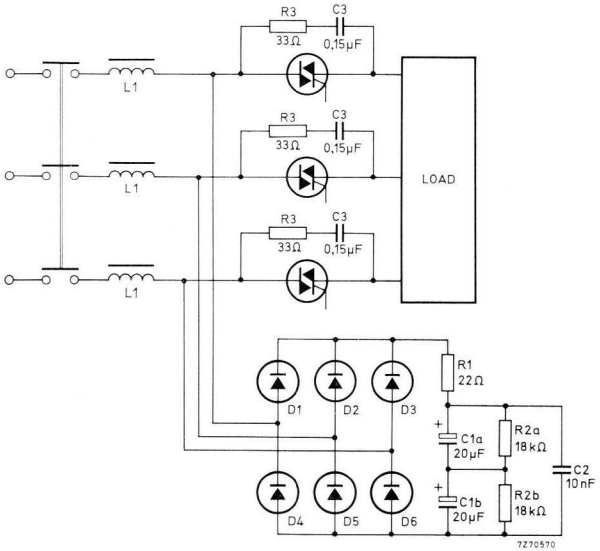


Fig.6-2 Three-phase transient suppression scheme (see Table 6-1) using transient clipper.

7 Overcurrent protection

Like all other semiconductor devices, triacs have an infinite life if they are used within their ratings. However, they rapidly overheat when passing excessive current because the thermal capacitance of their junction is small. Overcurrent protective devices (circuit breakers, fuses) must, therefore, be fast-acting.

7.1 Inrush condition

Motor, incandescent lamp or transformer loads give rise to an inrush condition. Lamp and motor inrush currents are avoided by starting the control at a large trigger angle. Transformer inrush currents are avoided by adjusting the initial trigger angle to a value roughly equal to the load phase angle. Smaller and larger trigger angles cause inrush effects. No damage occurs when the inrush current time function is below the inrush current rating curve (Section 3.3.2). Circuits catering for a transformer load are presented in Section 9.3.

Turn-on di/dt under inrush condition seldom exceeds the rated level. For instance, a 220 V a.c. supply with 20 μH source inductance causes a maximum di/dt of $(220\sqrt{2})/20 = 16$ A/μs (50 A/μs rating). Chokes to soften commutation should preferably be saturable so as to maintain regulation and avoid deterioration of the power factor; because their impedance reduces at low current, they have very little effect on the inrush current.

7.2 Short-circuit condition

Fuses for protecting triacs should be fast acting, and the amount of fuse I^2t to clear the circuit must be less than the I^2t rating of the triac. Because the fuses open the circuit rapidly, they have a current limiting action in the event of a short-circuit — see Fig. 7-1[6]). High-voltage fuses exhibit low clearing I^2t but the fuse arc voltage will be dangerous unless triacs with a sufficiently high voltage rating are used.

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[6]) Application Book: Rectifier Diodes, Chapter 7; ordering code 9399 256 01001.

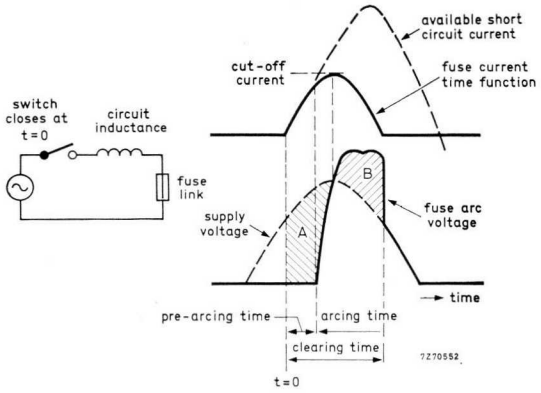


Fig.7-1 Action of a rapid fuse. Upper curve shows fuse current and lower curve fuse voltage; areas *A* and *B* are equal.

Fuses suitable for the BTW43, BTX94 and BTW34 are listed in Table 7-1. The table shows that higher-voltage fuses may require current derating; for instance, the NGH00 uFF63, intended for use with up to 240 V a.c. input, allows the BTW34 to operate at its full current rating (45 A or 55 A) but for the NGH00 uFF40, intended for use with an a.c. input that may exceed 240 V, the load current must be restricted to 40 A.

Table 7-1 Fast acting fuses for triac protection

triac	$V_{rms\ max}$[a])	fuse → Amp trap form 101	Bogenschütz	English Electric	Ferraz	Jean Müller
		I_{max}[b]) → 200 kA	150 kA	110 kA	100 kA	100 kA
BTW43	240	A25×10	—	GSG 1000/16	621 CP URE 14-12	M00 üF2 10
	380	A60×20	—	GSG 1000/16[c])	621 CP URE 14-10	M00 üF2 10
	415	A60×20	—	—	621 CP URE 14-10	M00 üF2 10
BTX94	240	A25×30 A70P40[d])	NHG00 uFF40	GSG 1000/35	621 CP YRE 14-32	N00 üF2 36
	415	A60×30	NHG00 uFF32	GSG 1000/30	621 CP URE 14-25	M00 üF2 25
BTW34	220	A25×40 A70P70[d])	NGH00 uFF63	GSG 1000/55	621 CP URE 22-50	M00 üF2 50
	240	A25×40 A70P70[d])	NHG00 uFF63	GSG 1000/55	621 CP URE 22-50	M00 üF2 36
	415	A60×30 A70P50[d])	NHG00 uFF50	GSG 1000/40 GSG 1000/45[e])	621 CP URE 14-40	M00 üF2 36
	500	A60×30 A70P50[d])	NHG00 uFF40	GSG 1000/35 GSG 1000/40[f])	621 CP URE 14-32	M00 üF2 36

[a]) R.M.S. mains voltage (max. value).
[b]) Symmetrical prospective current breaking capacity.
[c]) Symmetrical prospective current must not exceed 20 kA.
[d]) For high repetitive current.
[e]) Symmetrical prospective current must not exceed 5 kA.
[f]) Symmetrical prospective current must not exceed 8 kA.

USE OF TABLE: The "$V_{rms\ max}$" column gives the nominal input voltage *up to which* a fuse can operate. For instance, the A60×20 may be used for any voltage up to 415 V, but the use of the A25×10 is restricted to 240 V max.
The last two digits in the fuse type numbers denote rated fuse current, e.g. A25×10 is a 10 A fuse, A70P70 is a 70 A fuse, NHG00 uFF40 is a 40 A fuse, GSG 1000/45 is a 45 A fuse, 621 CP URE 14-32 is a 32 A fuse and M00 üF2 36 is a 36 A fuse.

8 Triac choice and heatsink calculation

8.1 Triac choice

The choice of the triac depends on:

1. a.c. input voltage
2. nominal load current
3. inrush current
4. cooling.

1. To allow for transients, the triac voltage classification (repetitive peak rating) is taken to be *about three times* the r.m.s. input voltage. Transient suppression is still necessary, but the size of the required transient suppression elements (Chapter 6) is moderate.

2. The r.m.s. current rating must be at least equal to the maximum load current.

3. Inrush currents occur when the load is a motor, a transformer or an incandescent lamp. It is generally safe to use a triac the r.m.s. current rating of which is 50% to 100% higher than the nominal load current. The lamp or transformer inrush current can be 10 to 15 times the nominal load current. In most cases the repetitive current rating can be chosen to accord with the inrush current because the inrush condition lasts for only a few cycles. Always check the inrush current with the inrush current rating curve (Section 3.3.2). Section 7.1 discusses how inrush currents can be avoided.

4. The cooling method (free convection, forced-air cooling, water cooling) determines the loading capability of the triac.

8.2 Heatsink calculation

The heat generated in a triac must be transferred to the surrounding air at a sufficient rate to prevent overheating of the junction. This can be achieved by mounting the triac on a heatsink; the thermal resistance between the junction and ambient is much too high to cause significant cooling. Fig. 8-1 is a simplified heat flow diagram for the triac mounted on a heatsink. The temperature difference $T_j - T_{amb}$ is the thermal e.m.f. driving the heat P generated in the junction area through the chain of thermal resistances. Applying Ohm's law, the required heatsink thermal resistance follows from:

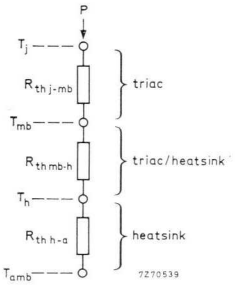


Fig.8-1 Simplified heat flow diagram.
T_h = heatsink temperature
$R_{th\,h-a}$ = heatsink thermal resistance
T_{amb} = ambient temperature.

$$R_{th\,h-a} \leqslant \frac{T_{j\,max} - T_{amb}}{P} - (R_{th\,j-mb} + R_{th\,mb-h})$$

where: $T_{j\,max}$ = rated junction temperature (125 °C)

T_{amb} = ambient temperature

P = power dissipated in the device

$R_{th\,j-mb}$ is defined in Section 3.2.2

$R_{th\,mb-h}$ is the mounting base-to-heatsink thermal resistance (0,2 °C/W to 0,5 °C/W).

Calculation example

A triac must control 25 A motor current at 35 °C ambient temperature. Select a triac and calculate its heatsink.

According to Section 8.1, the triac r.m.s. current rating must be twice the nominal motor current, so the BTW34 (55 A r.m.s. current rating) can be used. For BTW34: $T_{j\ max} = 125$ °C. $R_{th\ j-mb} = 0{,}6$ °C/W (full-wave operation), $R_{th\ mb-h} = 0{,}2$ °C/W. Consulting Fig. 8-2: $P = 32$ W at $I_{T(RMS)} = 25$ A. For $T_{amb} = 35$ °C from the equation given above:

$$R_{th\ h-a} \leqslant \frac{125 - 35}{32} - (0{,}6 + 0{,}2) = 2{,}0\ \text{°C/W}.$$

From Fig. 8-2, by drawing lines shown dotted, we find: $R_{th\ mb-a} \approx 2{,}2$ °C/W. Whence: $R_{th\ h-a} = R_{th\ mb-a} - R_{th\ mb-h} \approx 2{,}2 - 0{,}2 = 2{,}0$ °C/W, which is the value found above. Entering $R_{th\ h-a} = 2{,}0$ °C/W into the 56290 extruded heatsink plot of Fig. 8-3, we read for $P = 31{,}5$ W and free convection: heatsink length = 7,5 cm.

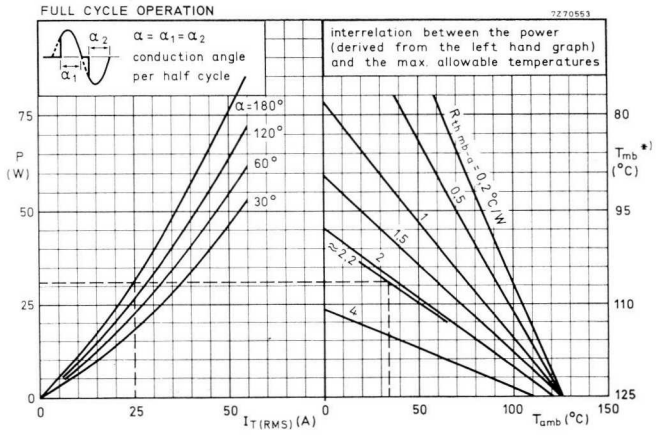


Fig.8-2 Use of BTW34 power dissipation curves; compare with Fig.3-4.

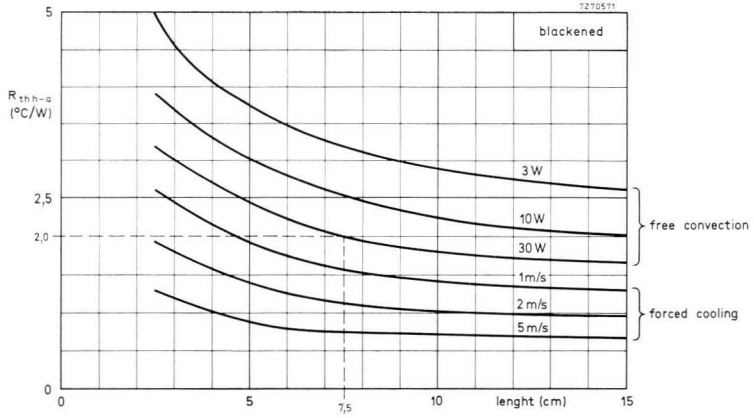


Fig.8-3 Plot of 56290 blackened aluminium heatsink extrusion.

8.3 Diecast heatsinks

Diecast heatsinks are readily available and provide efficient cooling. Those in Table 8-1 ensure thermal stability[7]). (For bi-directional operation, the maximum thermal resistance allowed between junction and ambient is 6 °C/W, 3,5 °C/W and 2 °C/W for BTW43, BTX94 and BTW34, respectively.) The stated current values must not be exceeded at the highest expected a.c. input voltage.

Table 8-1 Triacs and associated diecast heatsinks.

triac	diecast heatsink	allowed r.m.s. current for *free convection* with ambient temperature of: 35 °C	45 °C
BTW43	56348	10 A	9 A
BTX94	56278	23 A	20 A
BTW34	56314	33 A	30 A
BTW34	56318	42 A	38 A

[7]) Application Book: Rectifier Diodes, Chapter 3; ordering code 9399 256 01001.

9 Applications

9.1 General

Triacs are used in:

- on/off switches
- time-proportional controllers
- continuous controllers.

Several examples of these circuits are treated in this Section and a few general notes are important here.

On/off switches. Whereas in an asynchronous switch the triac is randomly triggered, triggering in a synchronous switch is made to coincide with the zero cross-over points of the mains voltage. This results in:

- slightly higher circuit complexity because synchronization must be included
- better power factor (equal to that of the load) because of sinusoidal current
- reduced r.f.i. because during turn-on there is no step rise in triac current or an abrupt drop of triac voltage.
- high inrush current in the case of an iron-cored load
- low turn-on di/dt
- to obtain reliable triac switch-on under inductive load, the trigger pulses must be maintained during 100 μs to 200 μs minimum; this time is needed for the triac current to reach latching level as the device must start to conduct at a very low instantaneous mains voltage.

Compared with contactors, triac switches have an infinite life (when used within their ratings) and do not require provision for operation in explosive atmospheres. Unlike a contactor, a triac switch can easily be made to operate synchroneously. Soft start (no inrush effect) is simply obtained by initially using an increased trigger angle; this is of importance for weaving machines to prevent breaking of delicate yarns. Short-circuit currents are rapidly interrupted (within 10 ms as against 30 ms for a contactor). Disadvantages of triacs are: the triac/heatsink combination takes more space; the triac/heatsink/trigger circuit is more expensive; triac losses are higher (but still below 1% of full output power).

There are single-phase and three-phase switches; the single-phase types are limited in power because of unbalanced loading of the mains.

Sections 9.2 and 9.3 discuss circuits of on/off switches.

Time-proportional controllers. Fig. 9-1 shows the principle of time-proportional control. It is on/off control with a fixed repetition period t_o; the triac is triggered synchronously to reduce r.f.i. and turn-on di/dt, and to obtain the best power factor (sinusoidal load current). The average power in the load is proportional to t_{on}/t_o (linear behaviour) and stepless variation occurs by changing t_{on}, the conduction time of the triac: *quasi*-proportional control. Time-proportional control is mostly used to control temperature, and period t_o is adjusted to suit the controlled process: there is no temperature ripple when t_o is made much smaller than the thermal time constant.

Triac switching rates must, if possible, be outside the 0,1 Hz to 30 Hz range to avoid irritation to the eye caused by light flicker where weak mains supplies are concerned.

Examples of time-proportional control are given in an earlier publication[8]) and in Section 9.3.

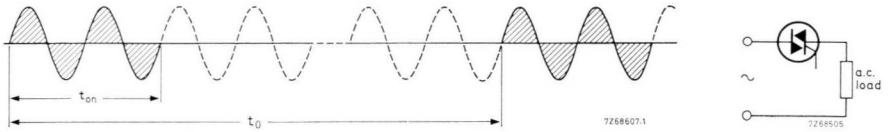


Fig.9-1 Time-proportional control principle.

Continuous controllers (*as distinct from* on/off controllers). There are single-phase and three-phase controllers. Three-phase controllers may be half-controlled (i.e. diode and thyristor in anti-parallel in each phase) or full-controlled (i.e. two thyristors in anti-parallel or one triac in each phase). Full-controlled controllers require more careful design of the trigger circuit, but their symmetrical output has a lower harmonic content because there are no even harmonics; this means less dissipation in motor control as clearly illustrated by Fig. 9-2. Another advantage over half-controlled controllers is that saturation

[8]) Application Book: Thyristor and Triac Power Control Using 61-series Modules, Chapter 4; ordering code 9399 266 02601.

of an inductive load is more easily avoided. It is sufficient that the trigger angles for the positive and negative half cycles be matched to within a few degrees for each phase; different trigger angles in different phases (and equally different phase voltages) do not produce a d.c. component in the load.

Because in a full-controlled controller two triacs turn on simultaneously, conduction can only ensue *when the trigger pulses fed to all gates coincide*; a *central trigger pulse generator* is, therefore, essential. A.C. controllers are now frequently used for motor control[8]).

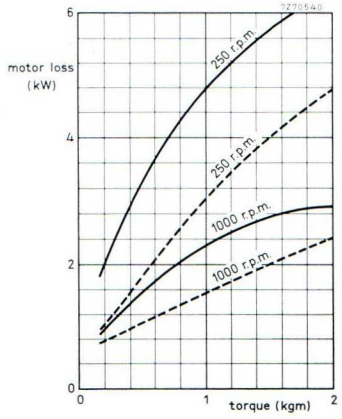


Fig.9-2 Motor loss (kW) vs. torque (kgm) for triac controller (- - - -) and thyristor/diode controller (———). Three-phase, 5 h.p., 1500 r.p.m. motor.

Note 1. Switchable powers depend on the allowed triac current — see Table 8-1. For a motor load the current must be taken as half the tabulated value because of the inrush effect.

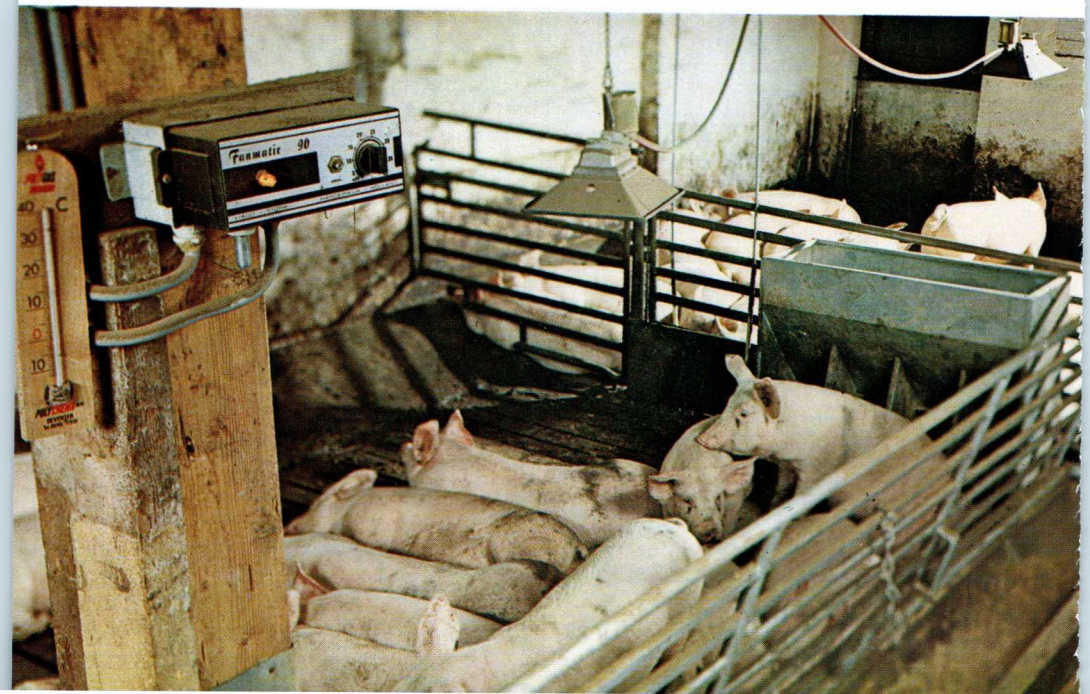
Note 2. *Controlled load current must exceed specified latching current*, otherwise the triac may not stay in conduction. This condition determines minimum controllable power (50 W at 240 V for BTW43).

Note 3. *Gate leads must be twisted* to prevent spurious triggering by interference; spurious triggering would cause a short-circuit in motor reversing switches.

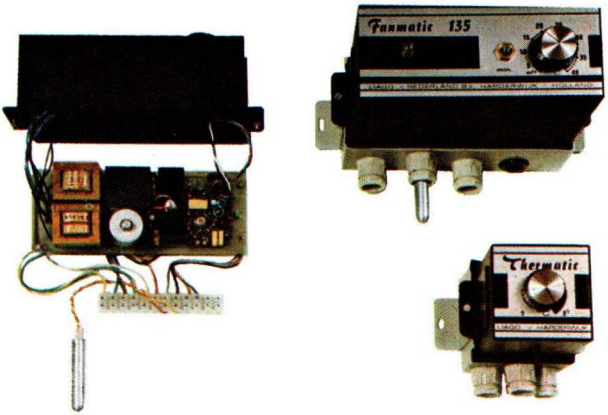
Note 4. A 0,1 μF, 1000 V d.c. capacitor and a 33 Ω, 2 W resistor are connected in series across *each* triac to reduce transients.

[8]) Application Book: Thyristor and Triac Power Control using 61-series Modules, Chapter 4; ordering code 9399 266 02601.

„Kooylust" farm uses conditioned pigsties (controlled temperature, humidity and light) to breed strong and healthy pigs.



In the pink of condition thanks to triac-controlled heating and ventilating system.
Courtesy of Messrs. Mitra, Waarder, The Netherlands.



9.2 Solid-state motor switches

9.2.1 Circuit survey

The switches presented here are suitable for squirrel-cage motors. Some are reversing and, where motor inrush currents are intolerable, the solid-state star/delta switches are useful; in all circuits, the star-position time is adjustable to suit the particular application. All three-phase switches cater for both star-connected and delta-connected loads. The motor load must be shunted by an *RC*-network to promote triac turn-on — Fig. 9-5 in Section 9.2.3 gives the necessary particulars. Table 9-1 lists the circuits discussed.

Tabel 9-1 Solid-state motor switches

section	circuit	features	number of triacs used
9.2.2	single-phase switch	asynchronous	1
9.2.3	three-phase switch	asynchronous	2
9.2.4	three-phase soft-start switch	starting torque adjustable to limit inrush current or prevent damage to sensitive load	1
9.2.5	single/three-phase reversing switch	asynchronous	2/4
9.2.6	three-phase rapid-stop-and-reversing switch	asynchronous rapid stop and reversing by "plugging"	4
9.2.7	star/delta	"star position" obtained through phase control (reduced motor voltage)	3
9.2.8	star/delta and reversing switch	asynchronous	11

9.2.2 Single-phase switch[9])

The circuit of Fig. 9-3 is asynchronous because triac TH_1 is triggered as soon as S_1 closes. The UPA61 trigger pulse generator functions as follows. Capacitor C_1 charges on closure of S_1 until Schmitt trigger ST trips on; inverting

[9]) AN No. 131: A.C. Static Switch; ordering code 9399 260 63101.

amplifier A_1 saturates and C_1 discharges rapidly through regenerative feedback path D_1 R_2. Discharging stops when ST trips off because then A_1 no longer conducts; C_1 charges again to repeat the process. The 10 kHz, 10 μs wide trigger pulses are coupled to the triac gate via a TT61 trigger transformer.

Variants of the circuit are a switch or the output of a 60- or 61-series circuit module in parallel with C_1 (pins 14/17 connected direct to +12 V). Also, pins 14/17 of the UPA61 can be connected to a NOR gate of the 60- or 61-series for logic control (S_1 omitted). In all cases, trigger pulses only occur when C_1 can charge.

The wiring diagram is given in Fig. 9-4.

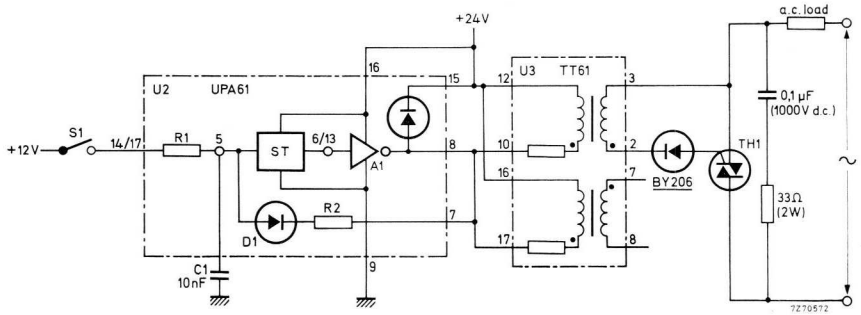


Fig.9-3 Single-phase asynchronous switch.

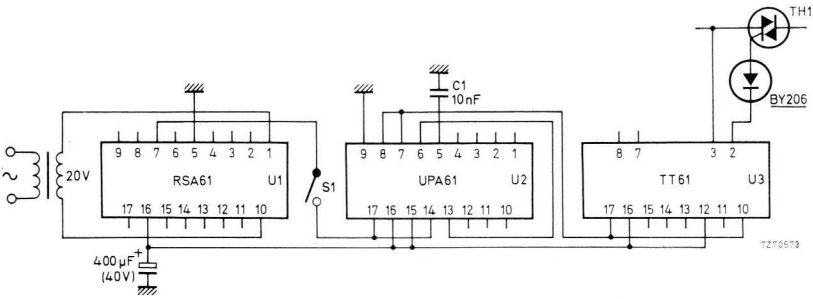


Fig.9-4 Wiring diagram of single-phase asynchronous switch.

9.2.3 THREE-PHASE SWITCH

The three-phase switch, Figs 9-5 and 9-6, is very simple. The 40 kHz trigger pulse source functions as described in the previous Section; pulse inversion is required because the pulse amplifier must deliver negative-going output pulses. With S_1 closed, C_2 cannot charge, the pulse generator is inhibited, and so TH_1 TH_2 do not conduct. A logic output can replace S_1. Because the load is a motor, components R and C in Fig. 9-5 are recommended for promoting triac turn-on.

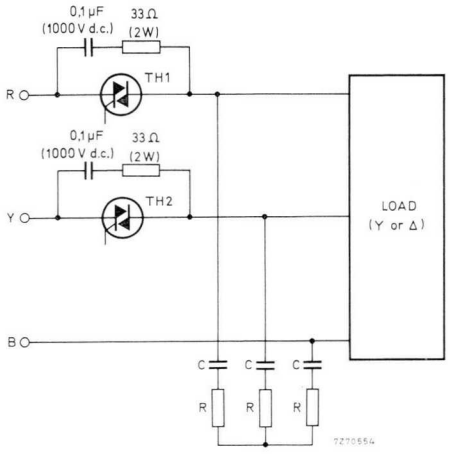


Fig.9-5 Power circuit of three-phase switch
R = 22 Ω, 9,5 W, 2322 325 17229
C = 1,5 µF, 220 V a.c., 2222 326 50155.

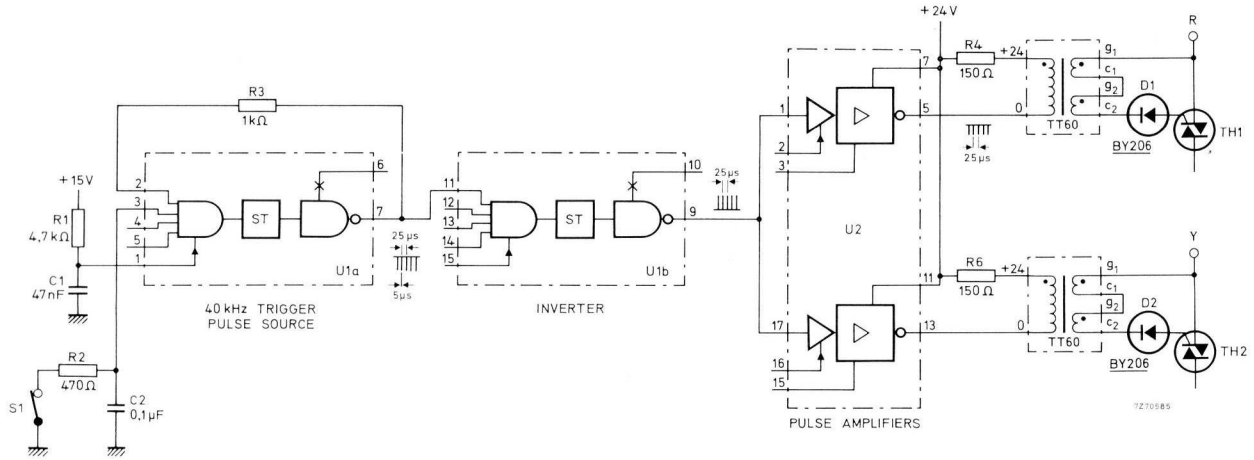


Fig.9-6 Circuit diagram of three-phase switch.
$U_{1a,b}$ = FZH241/2.AST30, U_2 = 2.LRD30.

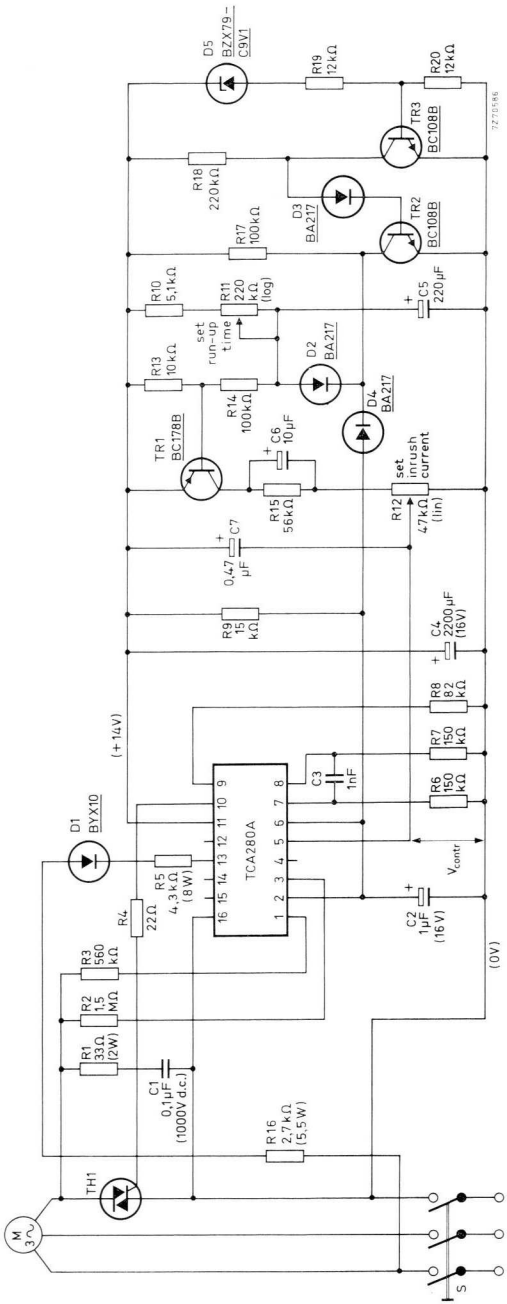


Fig.9-7 Soft-start switch with lock-out.

9.2.4 THREE-PHASE SOFT-START SWITCH[10])

The circuit in Fig. 9-7 provides "soft" motor speed run-up by delayed triggering of a triac connected in one of the phase leads. The advantage is that the circuit is simple, but the motor dissipation increases because the uncontrolled windings have to carry inrush current over a prolonged run-up period.

The trigger angle of TH_1 depends on the instantaneous value of V_{contr}. Lock-out excludes spurious triggering, that is, the TCA280A is inhibited until its d.c. voltage has reached the steady-state level. After closure of motor switch S, while the +14 V TCA280A supply is still below steady-state level and D_5 is not conducting, TR_3 is off and TR_2 on. With pins 2/6 at low potential (because D_4 and TR_2 conduct), and pin 5 at high potential (because TR_1 conducts), the TCA280A cannot produce trigger pulses. When the +14 V supply has reached its steady-state level, D_5 avalanches, TR_3 switches on and TR_2 switches off, diode D_2 becomes reverse-biased and C_5 can charge. When C_5 has charged to a predetermined level, TR_1 switches off. Thus, the time function of V_{contr} is according to Fig. 9-8. Initially, V_{contr} is high because C_6 and C_7 are uncharged.

Adjustment (Fig. 9-7):

1. *Set the starting torque with R_{12} (higher R_{12} resistance lowers the starting torque).*
2. *Adjust R_{11} so that, during run-up, motor current remains approximately equal to the initial value (observe with oscilloscope). Check with triac inrush current rating; if necessary increase, the resistance of R_{11} and R_{12}.*

[10]) AN No. 200: Smooth Start Circuits for Squirrel Cage Motors; ordering code 9399 320 70001.

Fig. 9-8 shows also the sawtooth voltage across C_2 which is used for phase control[11]). The triac trigger angle during run-up, and so the inrush current in the controlled phase, is set with R_{12}. The run-up time depends on the charging rate of C_5 and is adjusted with R_{11}. Because V_{contr} is initially high, a gradual build-up of the starting torque is ensured.

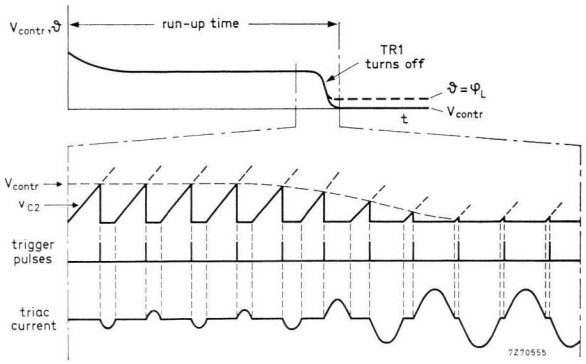


Fig.9-8 Waveforms of soft-start switch; lower waveforms on expanded scale: ϑ is the triac trigger angle and φ_L is the load phase angle.

9.2.5 Single/three-phase reversing switch

Figs 9-9, 9-10 and 9-11 show a circuit suitable for reversing a single- or three-phase motor. It was originally designed to steer a computer-controlled telescope drive but it also provides manual control. The circuit uses TTL silicon monolithic integrated-circuits from the FJ series for logic operations and for interfacing with the UPA61 high-power trigger sources; 10 kHz, 20 μs wide trigger pulses occur when a logic "1" (HIGH) level is applied to the input (pin 14) of the UPA61.

[11]) AN No. 214: Single phase control using TCA280A trigger IC; ordering code 9399 120 71401.

The truth tables and the subsequent motor functions are given in Tables 9-2 and 9-3. If CCW- and CW-rotation commands are given simultaneously (S_2 S_3 closed), output E of the anti-coincidence gate assumes "0" (LOW) level, outputs H and K become "0", trigger pulses are not produced, and the motor is not energized. Voltage regulator diodes D_1 D_2 restrict the collector voltage of the output transistors in U_3 to a value less than the rated level (15 V). Networks R_7 C_1, R_8 C_2 provide dead intervals of longer than a half-cycle during which no triggering occurs when a *CW*-command is followed by a *CCW*-command. It is thus ensured that the *CW*-control triac(s) will turn off *before* the *CCW*-control triac(s) will turn on, thereby preventing a short-circuit.

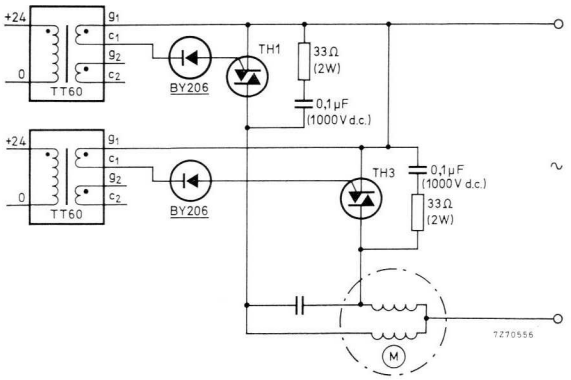
Table 9-2 Logic operation for automatic (computer) control; S_1 S_2 S_3 open

computer output to		outputs									motor rotation
U1-13	U1-1	*A*	*B*	*C*	*D*	*E*	*F*	*G*	*H*	*K*	
1 (CCW)	1 (start)	0	1	1	0	1	0	1	1	0	CCW
1 (CCW)	0 (stop)	1	1	0	0	1	1	1	0	0	—
0 (CW)	1 (start)	1	0	0	1	1	1	0	0	1	CW
0 (CW)	0 (stop)	1	1	0	0	1	1	1	0	0	—

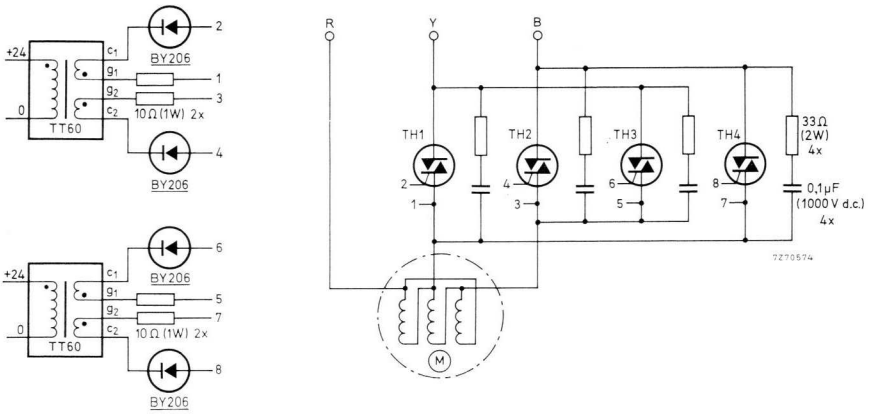
Table 9-3 Logic operation for manual control S_1 closed

S_2	S_3	outputs							motor rotation
		C	*D*	*E*	*F*	*G*	*H*	*K*	
open	open	0	0	1	1	1	0	0	—
closed	open	1	0	1	0	1	1	0	CCW
open	closed	0	1	1	1	0	0	1	CW
closed*	closed*	1	1	0	1	1	0	0	—

* conflicting commands



(*a*)



(*b*)

Fig.9-9 Motor reversing switch: (a) single-phase (b) three-phase.

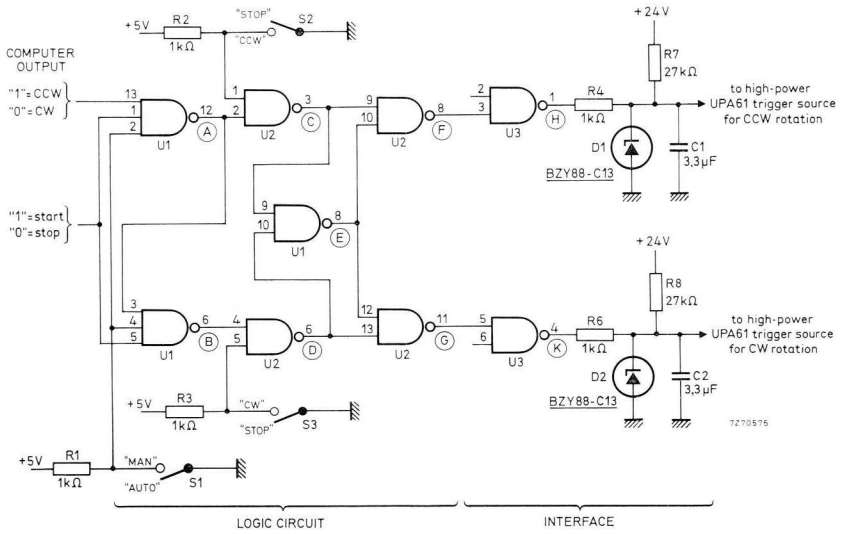


Fig.9-10 Logic circuit and interface of motor reversing switch.

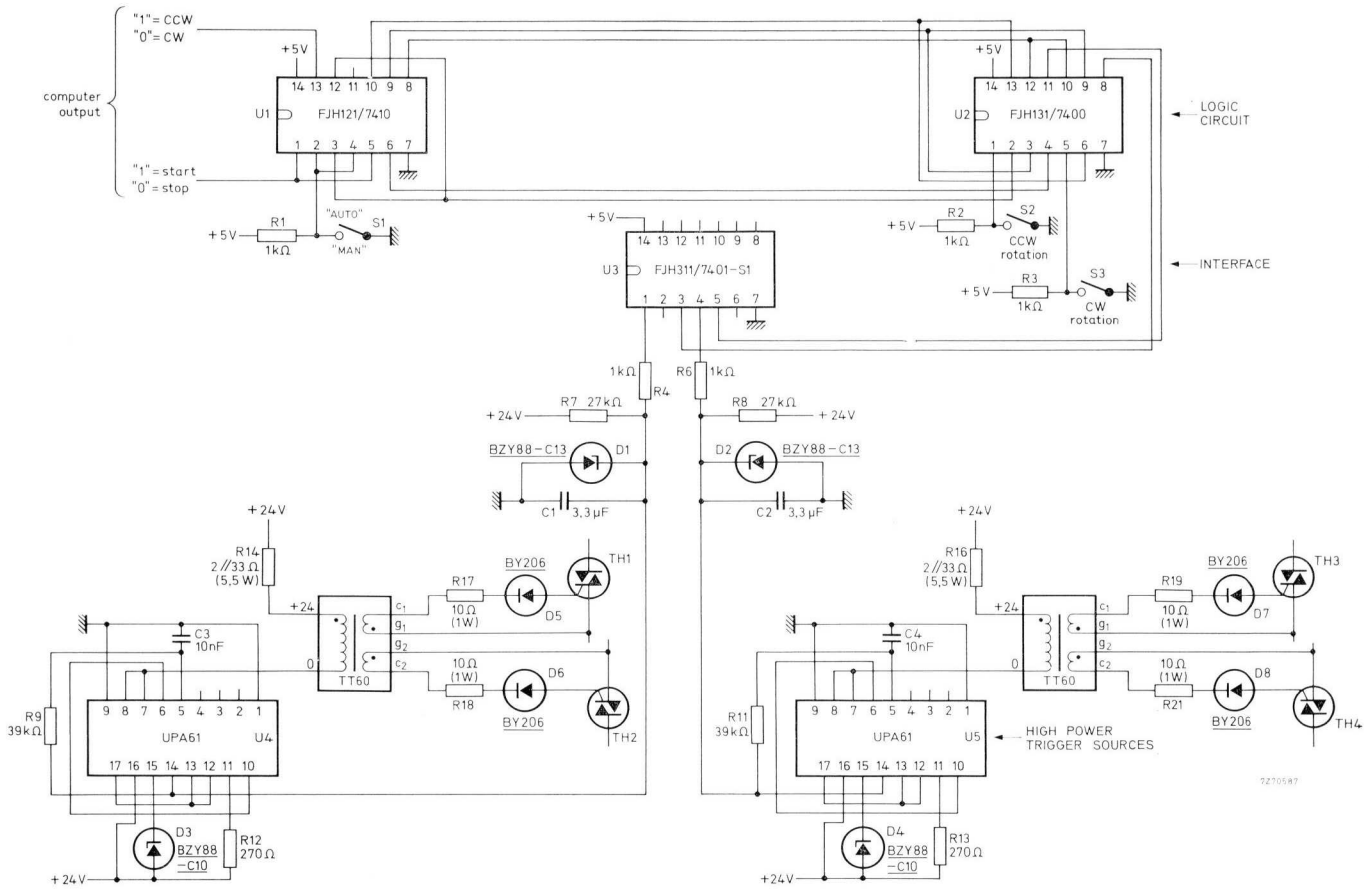
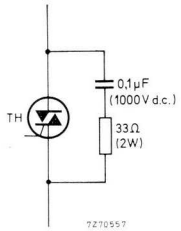


Fig.9-11 Wiring diagram of motor reversing switch arranged for three-phase circuit.

9.2.6 THREE-PHASE RAPID-STOP-AND-REVERSING SWITCH

The switch treated here provides rapid motor braking and reversal by so-called *plugging*. Plugging occurs when interchanging two phase leads so that the stator field reverses and rotates in a direction opposite to the rotor. Consequently, a high current is caused in the motor, and the resulting high torque causes abrupt braking owing to high acceleration in the opposite direction. To achieve braking, the motor is plugged for a preset period. The proposed system is only suitable for a motor with a constant load.

Fig. 9-12 and 9-13 show the circuit in which the 60-series and 61-series[12]) NORbits are used for triac control. Fig. 9-12 is the power circuit. The trigger circuit (Fig. 9-13) includes exclusive-OR interlocking stages U_{3b} U_{4b} for protection against simultaneous conduction of all four triacs owing to conflicting commands. That is, triggering only occurs if either $F \,.\, \bar{R} = 1$ or $\bar{F} \,.\, R = 1$; this condition is fulfilled for $F = 1$ ("Forward" command) *or* $R = 1$ ("Reverse" command). Networks $D_1\ R_1\ C_1$ and $D_2\ R_2\ C_2$ provide a non-triggering period of about 30 ms for safe switching from forward to reverse rotation.



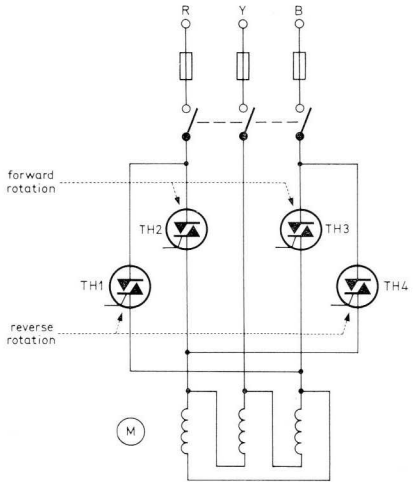


Fig.9-12 Three-phase reversing switch: (a) power circuit, (b) triac arrangement.

[12]) Application Book: Thyristor and Triac Power Control Using 61-series Modules, Chapter 2; ordering code 9399 266 02601.

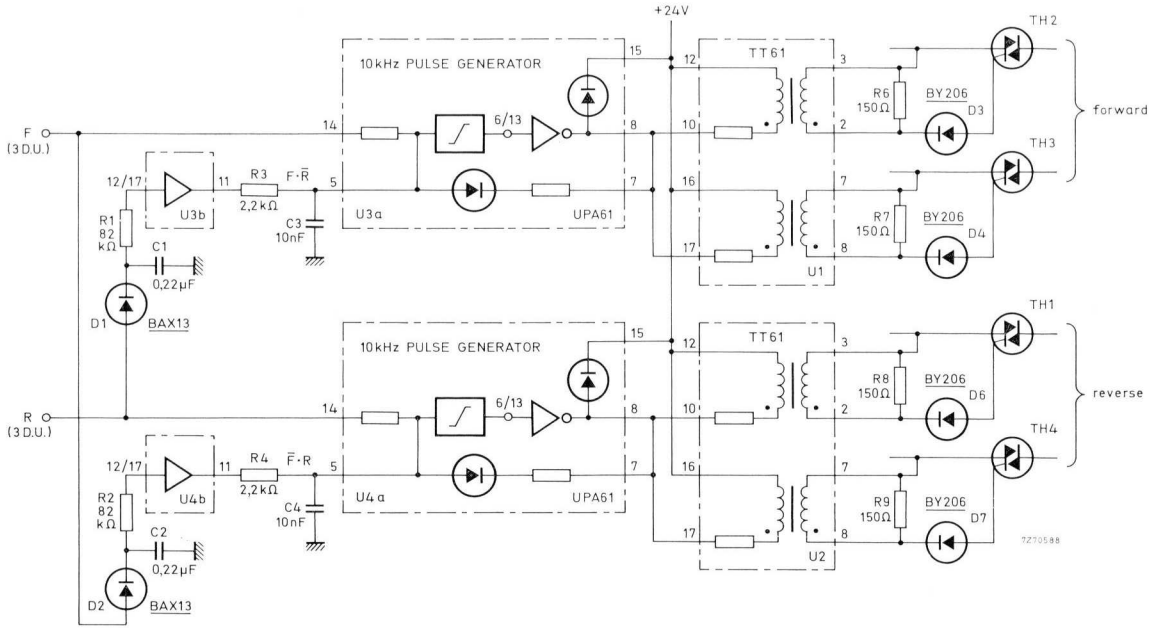


Fig.9-13 Trigger circuit for three-phase reversing switch.

In the plugging circuit of Fig. 9-14, U_{6a} U_{6b} act as a bistable memory whose state is determined by input commands R' and F'. Suppose $R' = 1$ (reverse rotation) and consequently $F' = 0$. Memory output $U_{6a} - 13$ is at "0". When "R" becomes "0", the TU60 output remains at "0" for a period approximately equal to C_{11} $(R_{11} + R_{12})$, gate U_{6c} has no input drive and its output becomes "1"; an "F" (forward) command is issued causing motor braking by plugging. The value for C_{11} depends on the motor type and its load. The required input drive is 6 D.U. (an input resistance of about 16 kΩ)[12]).

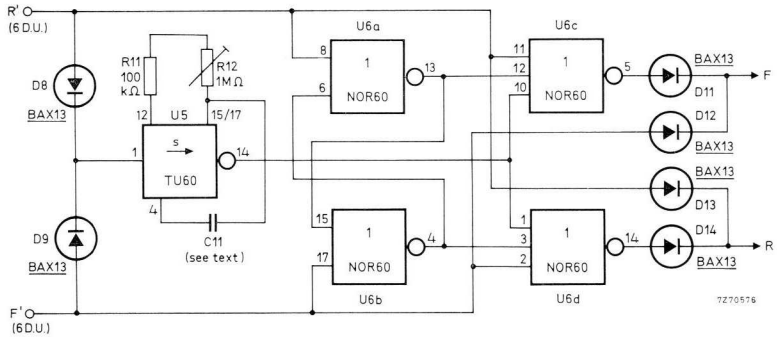


Fig.9-14 Reversing circuit of three-phase reversing switch; the "F" and "R" signals are fed into the circuit of Fig.9-13.

Fig. 9-15 is the wiring diagram; the connections between D_{11} to D_{14} and the inputs must be as short as possible.

[12]) Application Book: Thyristor and Triac Power Control Using 61-series Modules, Chapter 2; ordering code 9399 266 02601.

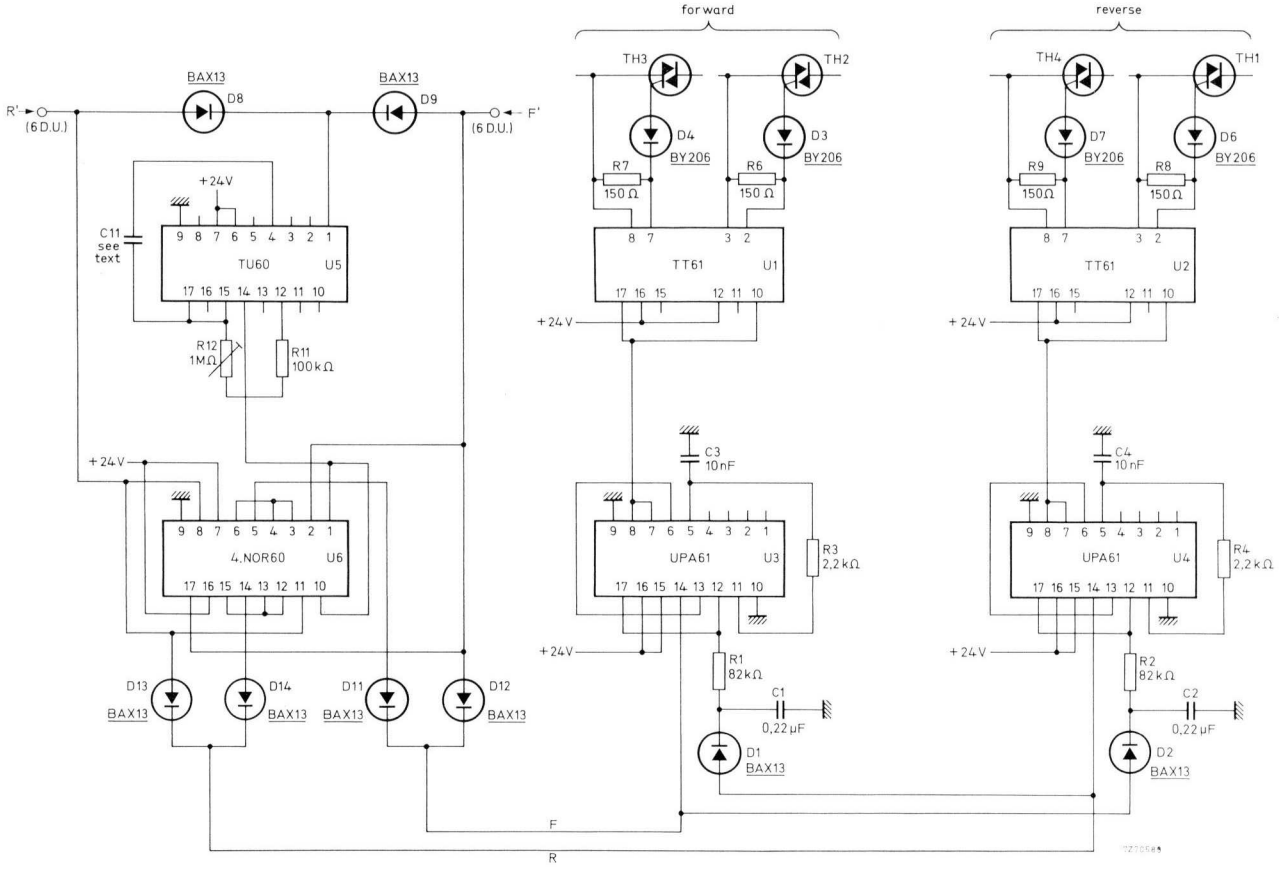


Fig.9-15 Wiring diagram of three-phase reversing switch.

Adjustment (Fig. 9-15):
Adjust R_{12} so that the motor just does not reverse when the F′ or R′ signal is made zero.

9.2.7 STAR/DELTA SWITCH

The star/delta switch of Fig. 9-16 uses the high noise immunity FZ/30-series modules for power control. As seen in Fig. 9-16*b* the motor is permanently delta-connected, the reduced voltage corresponding to start position being obtained through phase control.

Gates U_{1a} U_{1b} U_{2a} produce 200 μs negative-going pulses derived from the *RY*, *YB* and *BR* synchronization voltages. These pulses are passed via gates U_{1c} U_{1d} U_{2b} to the trigger gates together with the 40 kHz pulse generator output. See waveforms in Fig. 9-17. As a result, 200 μs pulse bursts are produced at the triac gates as soon as the motor switch closes, triggering the triacs at 120°. (The operation of the pulse generator is as described in Section 9.2.2, R_{19} and C_3 being the frequency determining elements.)

A preset time after the motor switch has closed, C_1 is sufficiently charged for U_{3a} output to switch to LOW level which overrides the outputs of U_{1a} U_{1b} U_{2a}. As a result, the outputs of gates U_{1c} U_{1d} U_{2b} become HIGH and the triacs are continuously triggered so that full voltage is applied to the motor.

Protection against spurious triggering due to an unsettled d.c. supply is ensured by adding C_2 which must be sufficiently charged before hold-off diode D_{17} becomes reverse-biased allowing the 40 kHz pulse generator to oscillate.

Potentiomters R_{13} R_{14} R_{16} are used to adjust the d.c. gate inputs and thus the instants at which the gate outputs will become negative, these instants being related to the trigger angle.

Phase control reduces the number of triacs required for this star/delta controller, but a disadvantage is the higher r.f.i. during run-up.

Fig. 9-18 is the d.c. supply circuit.

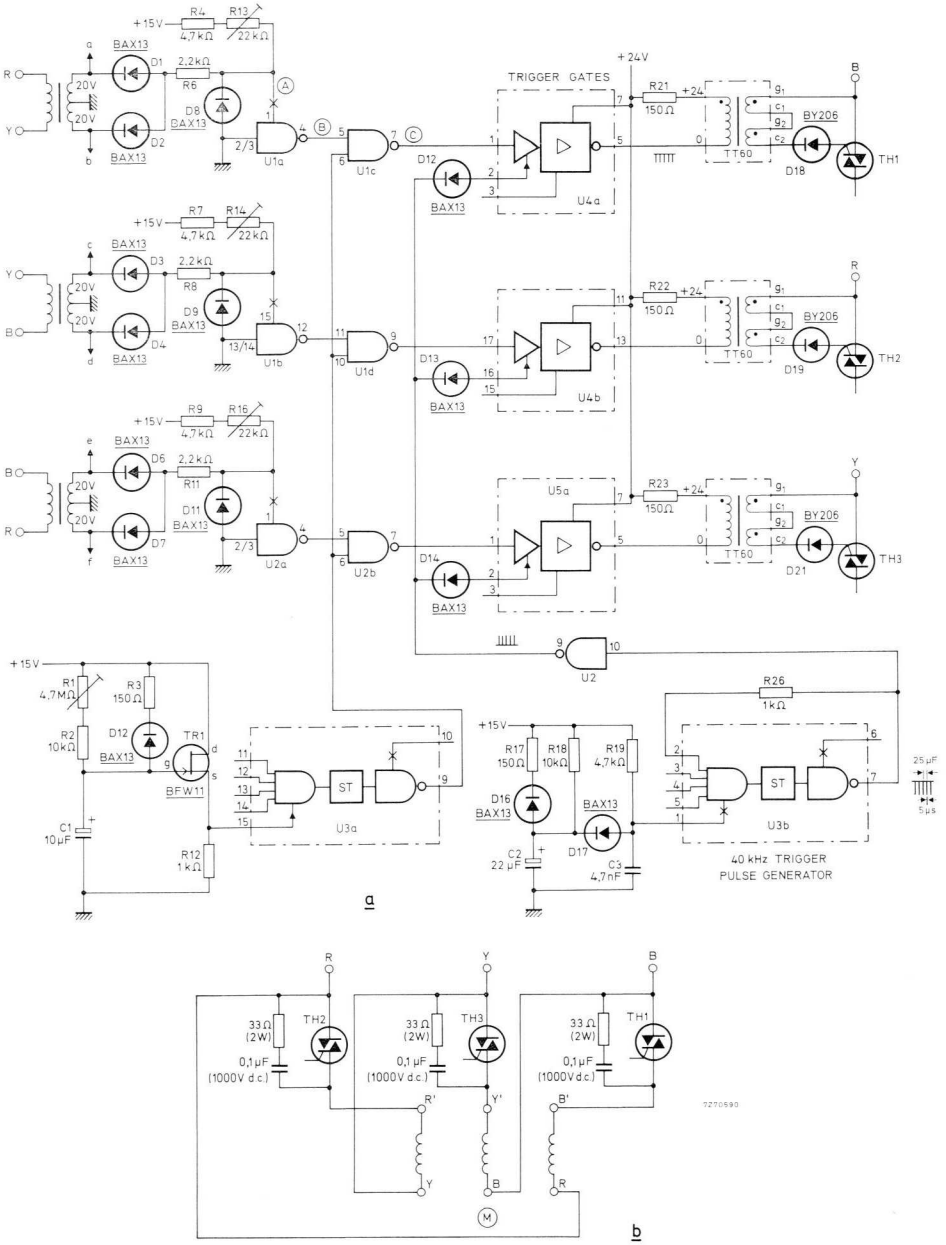


Fig.9-16 Star/delta switch: (a) control circuit, (b) power circuit. Circuit and motor are simultaneously energized.

U_1, U_2 = FZH111/4.NAND30
U_3 = FZH241/2.AST30
U_4 = 2.LRD30
U_5 = $\frac{1}{2}$×2.LRD30.

Adjustment (Fig. 9-16):

1. *While the motor runs with reduced voltage, adjust R_{13} until the voltage between terminals B'R (Fig. 9-16b) is $1/\sqrt{3}$ (0,58) times the r.m.s. line-line voltage; a higher R_{13} value corresponds to a lower voltage. Proceed similarly with R_{14} and R_{16} to adjust the voltages between R'Y and Y'B respectively.*
2. *Set R_1 to maximum resistance and then adjust it so that the peak motor inrush current, due to switching from reduced to full motor voltage, does not exceed the peak value that occurs during motor switch-on; the period of reduced motor voltage can be varied between 50 s and less than 1 s by variation of R_1.*

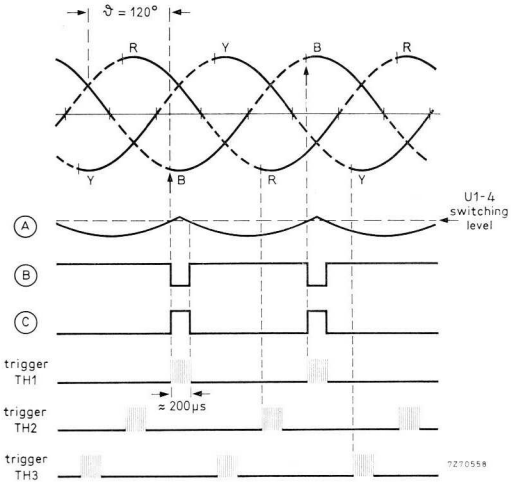


Fig.9-17 Waveforms of star/ delta switch ("star" position).

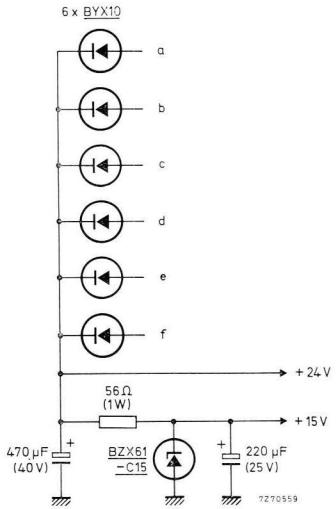


Fig.9-18 D.C. supply for star/ delta switch; *a* to *d* are the secondary terminations of the synchronization transformers (Fig.9-16).

9.2.8 STAR/DELTA AND REVERSING SWITCH

A circuit for a star/delta switch that also provides motor reversal is given in Figs 9-19 and 9-20; it uses circuit modules of the 60-series. The triacs are controlled by reed relays, the trigger circuit being supplied through resistors (R) whose values in Ω equals the line-line voltage (V_{LL}) in volts. Motor reversal is obtained by interchanging two phase leads. Memories I and II pass the commands issued by S_1 and S_3 to the CW- and CCW-rotation reed relays. They are interlocked so that U_{1b}—14 and U_{1d}—5 cannot be simultaneously HIGH; if this were to occur, TH_1 to TH_5 would all be triggered so causing a short-circuit. When the d.c. supply is switched on, both memories are reset (U_{1b}—14 and U_{1d}—5 both LOW) by the positive charge pulse of C_4. The reset line is necessary for clearing the memories before a fresh command is issued.

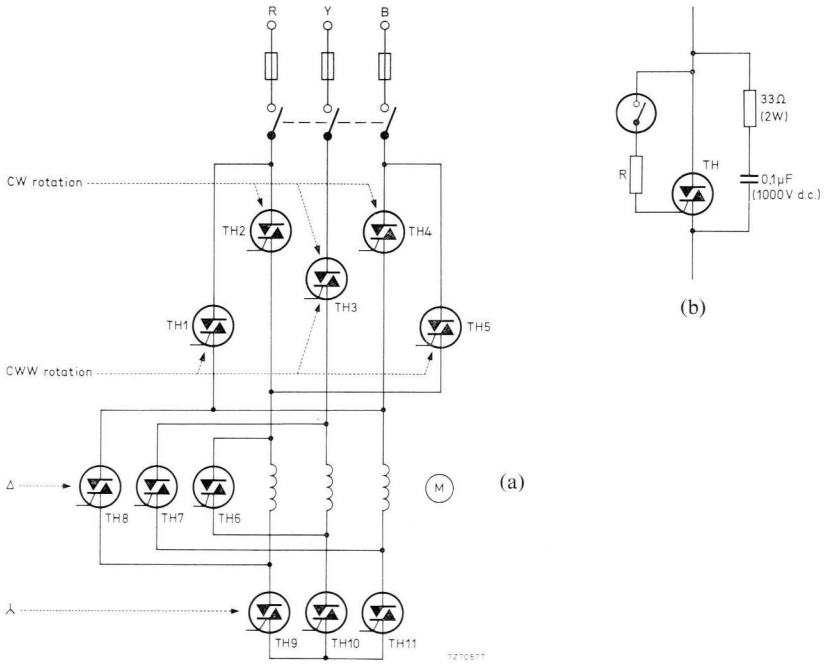


Fig.9-19 Star/delta reversing switch: (a) power circuit, (b) triac arrangement; $R\ (\Omega) = V_{LL}$ (V).

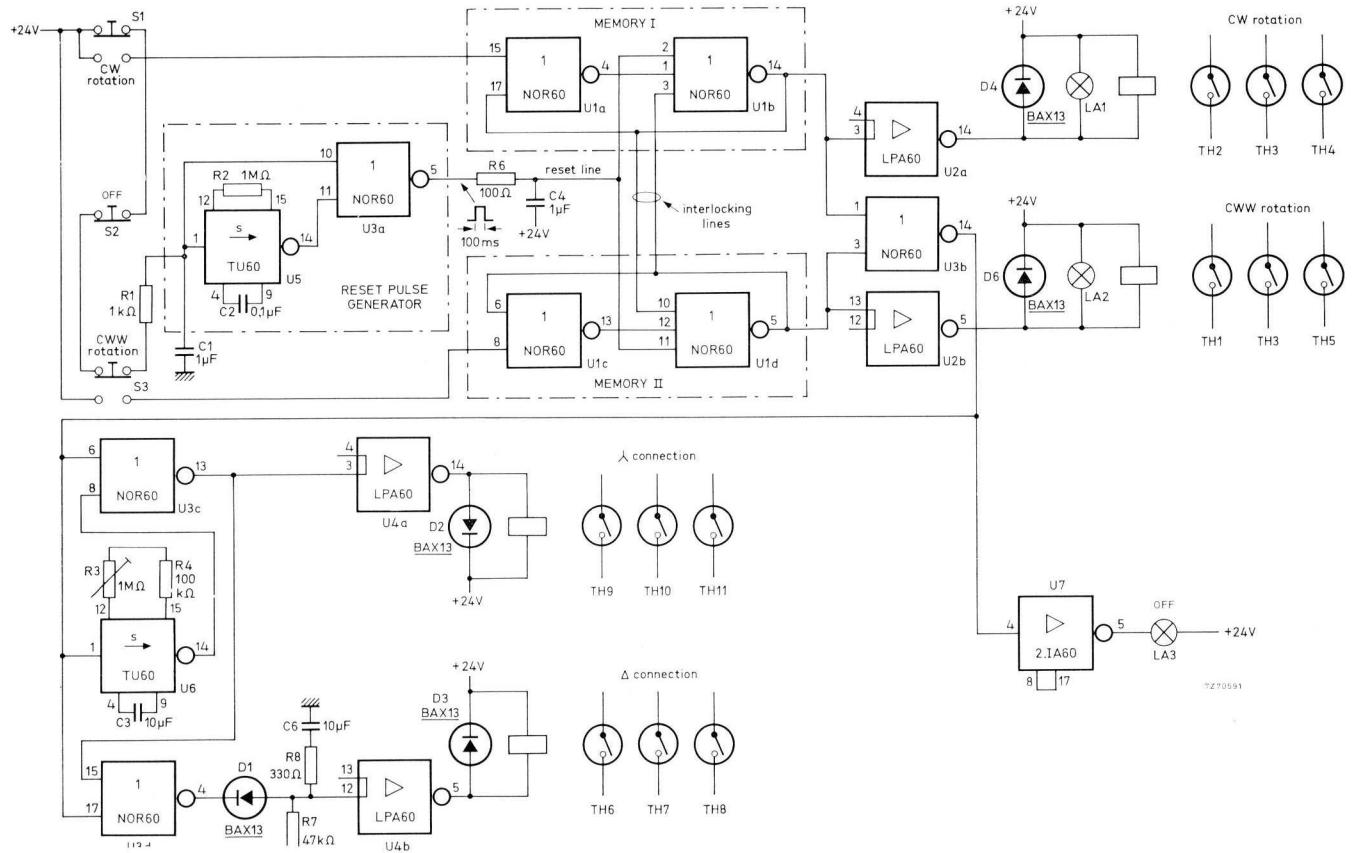


Fig.9-20 Circuit diagram of star/delta & reversing switch.

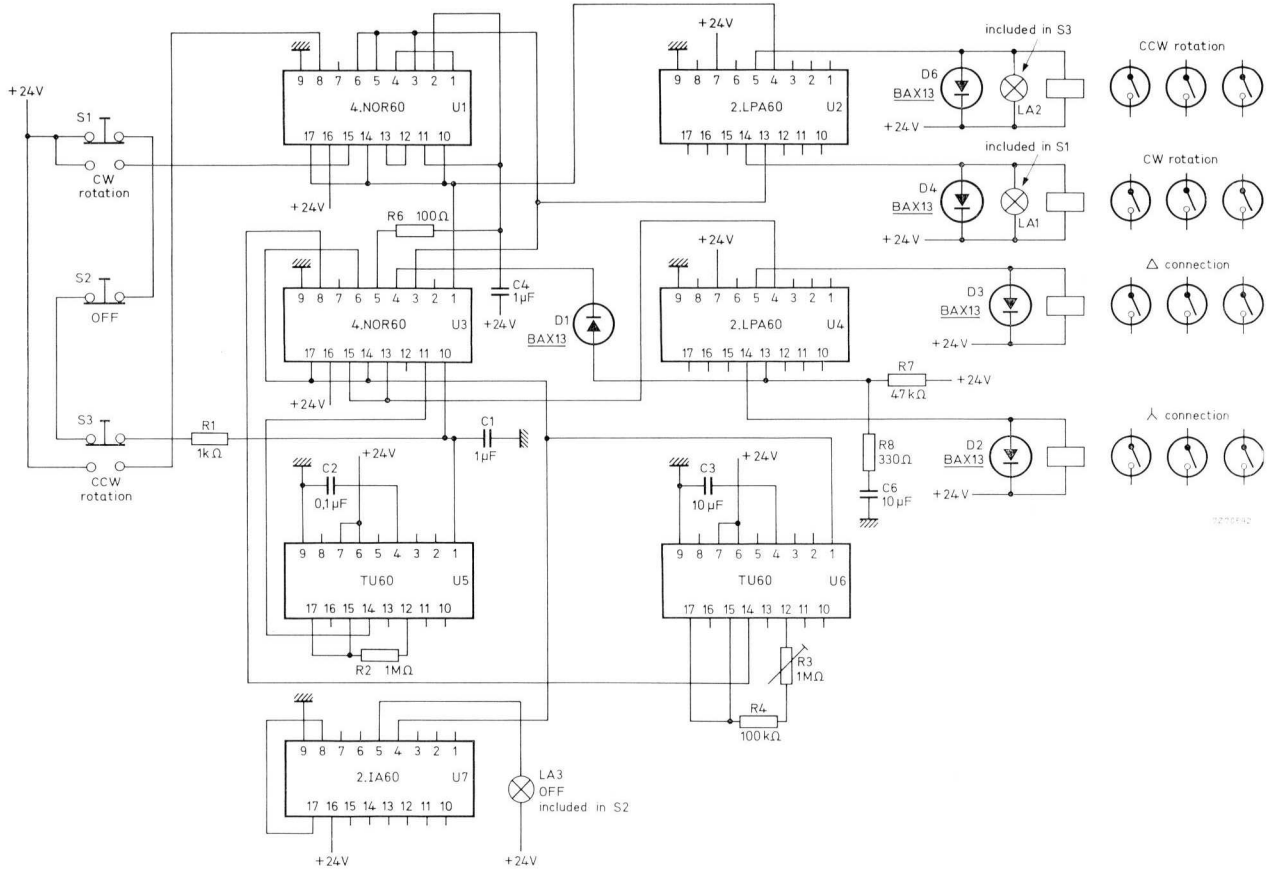


Fig.9-21 Wiring diagram of star/delta & reversing switch; +24 V can be obtained from LSU60.

The period during which the motor is star-connected is determined by timer U_6. To ensure safe switch-over to delta connection, a dead interval during which trigger pulses do not occur is interposed (20 ms for the specified values of R_9 and C_6) allowing $TH_9\ TH_{10}\ TH_{11}$ to turn off before $TH_6\ TH_7\ TH_8$ will conduct. The 0,1 s reset pulse has an identical function when switching from CW to CCW, and vice versa; that is, $TH_1\ TH_3\ TH_5$ will not be triggered until 0,1 s after triggering of $TH_2\ TH_3\ TH_4$ has ceased.

Adjustment (Fig. 9-21):
Set R_3 to maximum resistance and then adjust it so that the peak motor inrush current, due to switching from star to delta, does not exceed the peak value that occurs during motor switch-on; the period during which the motor runs star-connected is adjustable between 0,1 s and 10 s by variation of R_3.

9.3 Solid-state universal switches

9.3.1 Circuit survey

This section deals with general-purpose switches. Care must be exercised when controlling transformers with light load or no load at all because high inrush currents will flow when using a circuit that provides random or synchronous triggering. This can be avoided by using trigger delay (see Section 7.1). The circuits given here incorporate this feature. Full load cycles are supplied by these circuits to obtain zero load-voltseconds, and triac conduction always starts with the same mains voltage polarity to avoid magnetic biasing. Time-proportional controllers are mostly used for heating; normally, the load is resistive but it is inductive (transformer) where a low heater voltage is required for safety reasons. Table 9-4 surveys the circuits discussed.

Table 9-4 Solid-state universal switches

section	circuit	features	number of triacs used
9.3.2	single-phase asynchronous switch	handles resistive & inductive load	1
	single-phase animated-sign control	asynchronous circuit; handles resistive & inductive load; controls up to ten gas-discharge groups	up to 10
	single-phase synchronous switch I	handles resistive & inductive load	1
	single-phase synchronous switch II	handles load having max. 8° phase angle	1
9.3.3	single-phase switch for transformer load	trigger delay 12° to 90°; supplies full load cycles	1
9.3.4	time-proportional controller using TCA280A	suitable for household appliances, e.g. panel heaters; can handle resistive load only	1
	time-proportional controller using NORbits	for railway carriage heating; has therefore high control accuracy of $\pm$ 1 °C over 18 °C to 23 °C range; max. controlled power 25 kW; handles resistive load only	up to 4
9.3.5	single-phase time-proportional controller for transformer load	max. 50° trigger delay; supplies full load cycles	1
9.3.6	three-phase time-proportional controller	handles resistive & inductive load (star- or delta connected); supplies full load cycles	2
9.3.7	three-phase time-proportional controller for transformer load	load can be star- or delta-connected; supplies full load cycles	3

9.3.2 SINGLE-PHASE SWITCHES

Asynchronous switch

Fig. 9-22 shows a very simple switch. As soon as S_1 closes, the triac is triggered; operation is therefore asynchronous. Switch S_1 can be a reed type (actuated by a coil or a permanent magnet) or it can be a toggle switch. The value of R_1

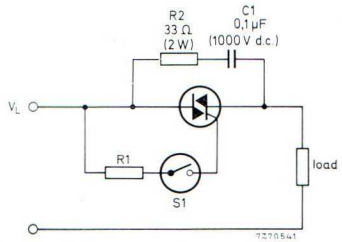


Fig.9-22 Reed-switch controlled triac; R_1 (Ω) = V_L (V).

in ohms is equal to the a.c. input voltage in volts, thus $R_1 = 220\ \Omega$ with a 220 V to 240 V supply. This circuit can drive a resistive or inductive load.

Another simple switch is given in Section 9.2.2.

Animated-sign control

This circuit is a "multiple" triac switch capable of switching independently several groups of gas-discharge tubes, a very useful feature for animated-sign displays. As seen from Fig. 9-23, one master unit controls several slaves, which in turn control the gas-discharge tubes via power switches. Each power switch includes a trigger gate, a TT60 trigger transformer and a triac power control device; all switches are triggered by the 40 kHz pulse source — see Fig. 9-16,

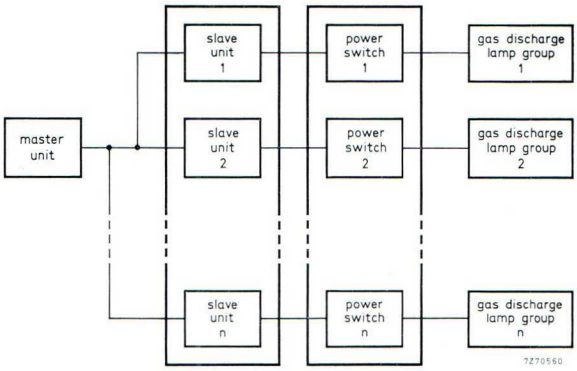
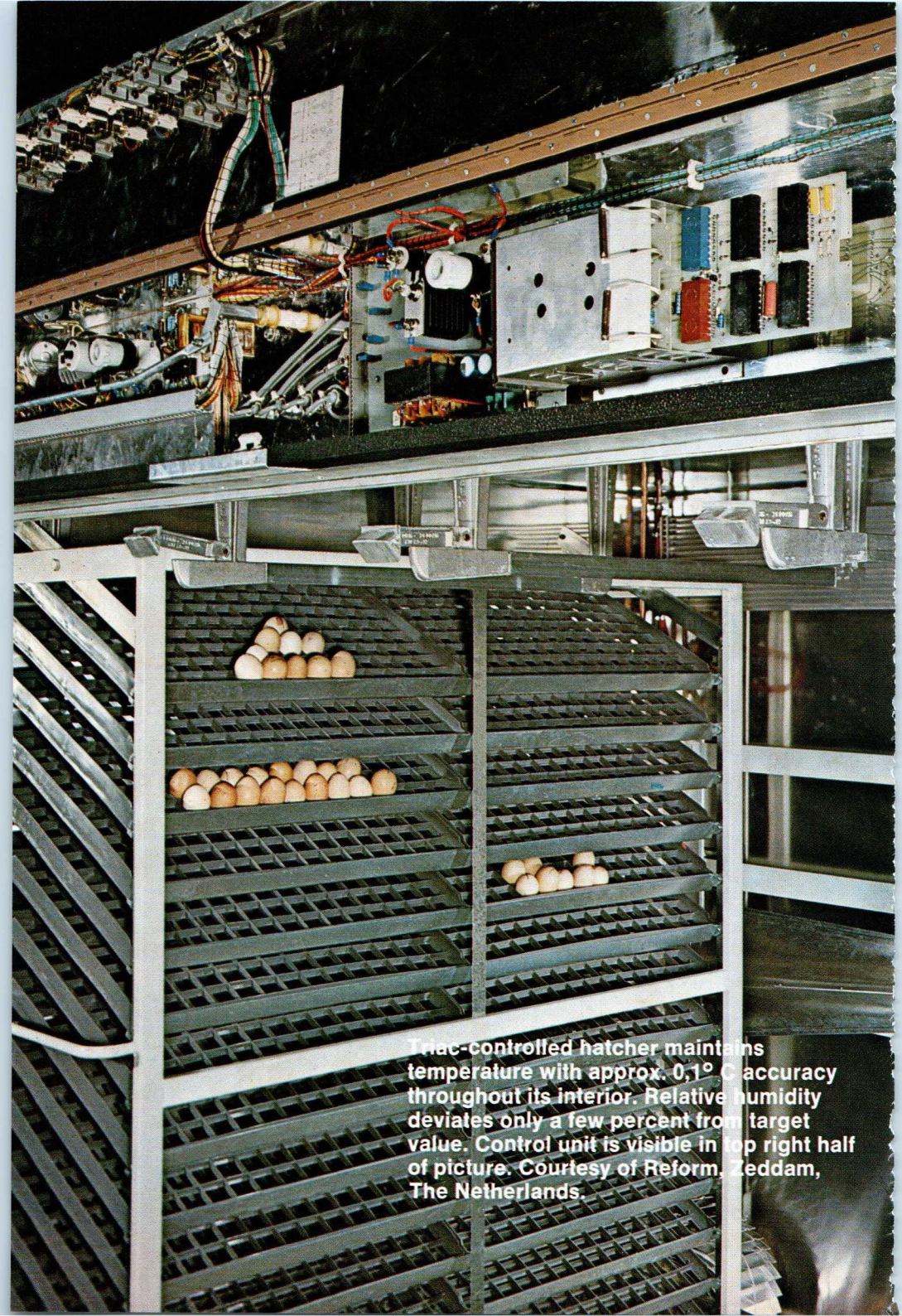
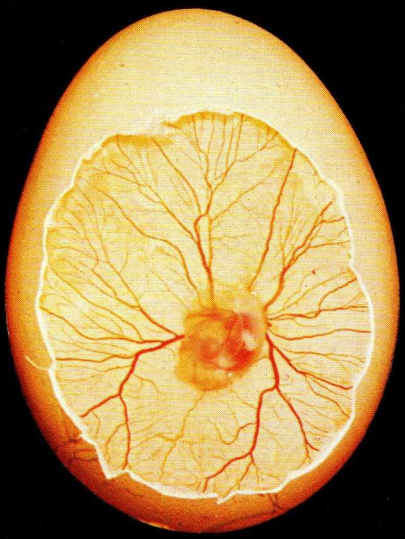
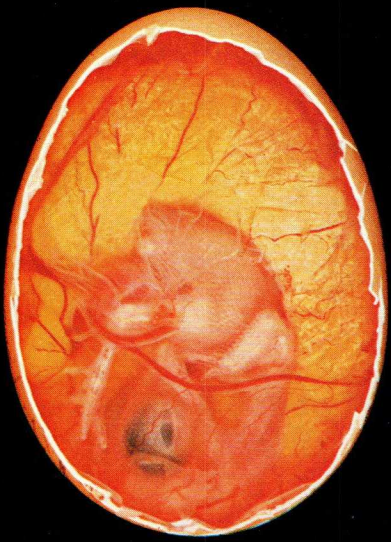


Fig.9-23 Block diagram of animated-sign control systems.

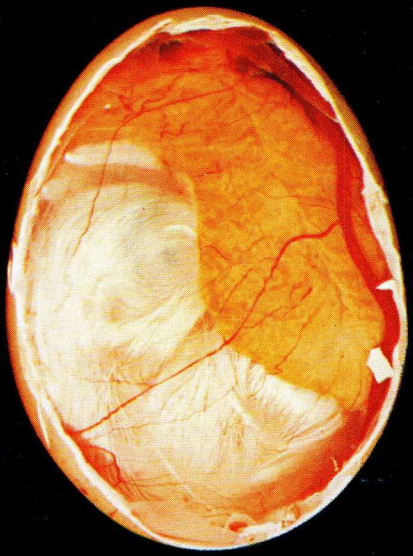


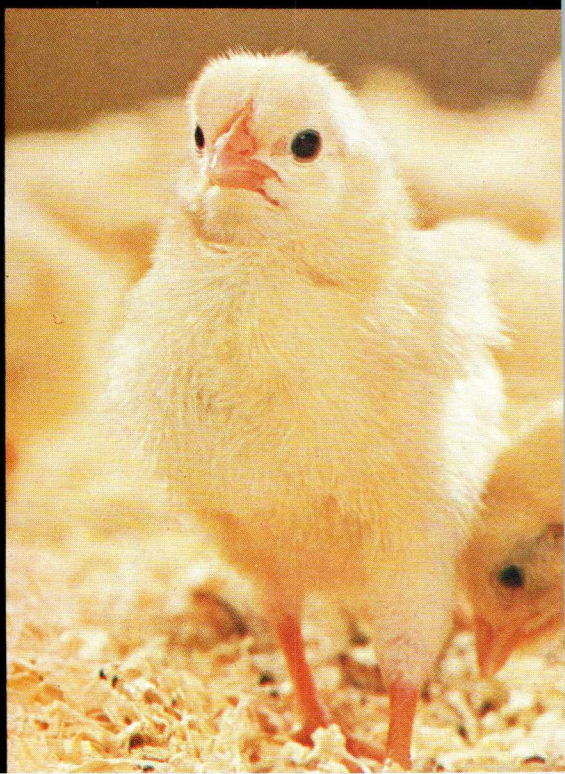
Triac-controlled hatcher maintains temperature with approx. 0,1° C accuracy throughout its interior. Relative humidity deviates only a few percent from target value. Control unit is visible in top right half of picture. Courtesy of Reform, Zeddam, The Netherlands.





From embryo to chick proudly stepping into the world.





Section 9.2.7. Operation is asynchronous but the measured inrush asymmetry of the high-voltage transformers supplying the gas-discharge tubes is not more than 10% (cos φ-factor about 0,7), so there is no risk of a dangerous inrush current. Because a continuous trigger pulse train is generated, triac turn-on is certain. The analogue and digital systems are based on the FZ/30-series of 16- and 20-lead dual in-line integrated circuits.

The *analogue* system shown in Fig. 9-24 uses TU30s to set cycle time; see also the waveforms of Fig. 9-25. The cycle time is completed as soon as all feedback voltages — labelled v_{fb} — are at HIGH level. As a result, $\Sigma v_{fb} = v_{fb1(1)} \cdot v_{fb2(1)} \ldots v_{fb1(n)} \cdot v_{fb2(n)}$ becomes HIGH, and C_1 can charge. The start pulse for re-initiating the cycle is produced as follows. When v_{C1} has reached the trip-on level v_1 of Schmitt trigger *ST*, the input voltage v_i to all slaves becomes HIGH to reset all TU30s (v_{fb1} and v_{fb2} becoming LOW). Because Σv_{fb} becomes LOW, C_1 discharges and *ST* trips off at level v_2; v_i returns to LOW level terminating the start pulse and setting the first TU30s in all slaves. After time t_{d1}, TU30 output v_{fb1} becomes HIGH; this sets the second TU30 whose output v_{fb2} becomes HIGH after additional time t_{d2}. Owing to the action of $U_{1b,c,d}$, output voltage $v_{o(1)}$ will be HIGH during the delay period t_{d2} of the second TU30. The duration of the cycle is equal to the *highest* value of $t_{d1} + t_{d2}$ adjusted for any slave; for the components shown, the maximum cycle time is 20 s. One master can drive up to ten slaves.

Adjustment (Fig. 9-24):

1. *Adjust R_3 in any slave unit to set the dark period t_{d1} of the gas-discharge tubes controlled by that particular unit; dark period $t_{d1} = C_2$ (μF)$\times(R_2 +$ 0,01 MΩ) seconds.*
2. *Adjust R_3 in any slave unit to set the lit period t_{d2} of the gas-discharge tubes controlled by that particular unit; lit period $t_{d2} = C_3$ (μF)$\times(R_3 +$ 0,01 MΩ) seconds.*

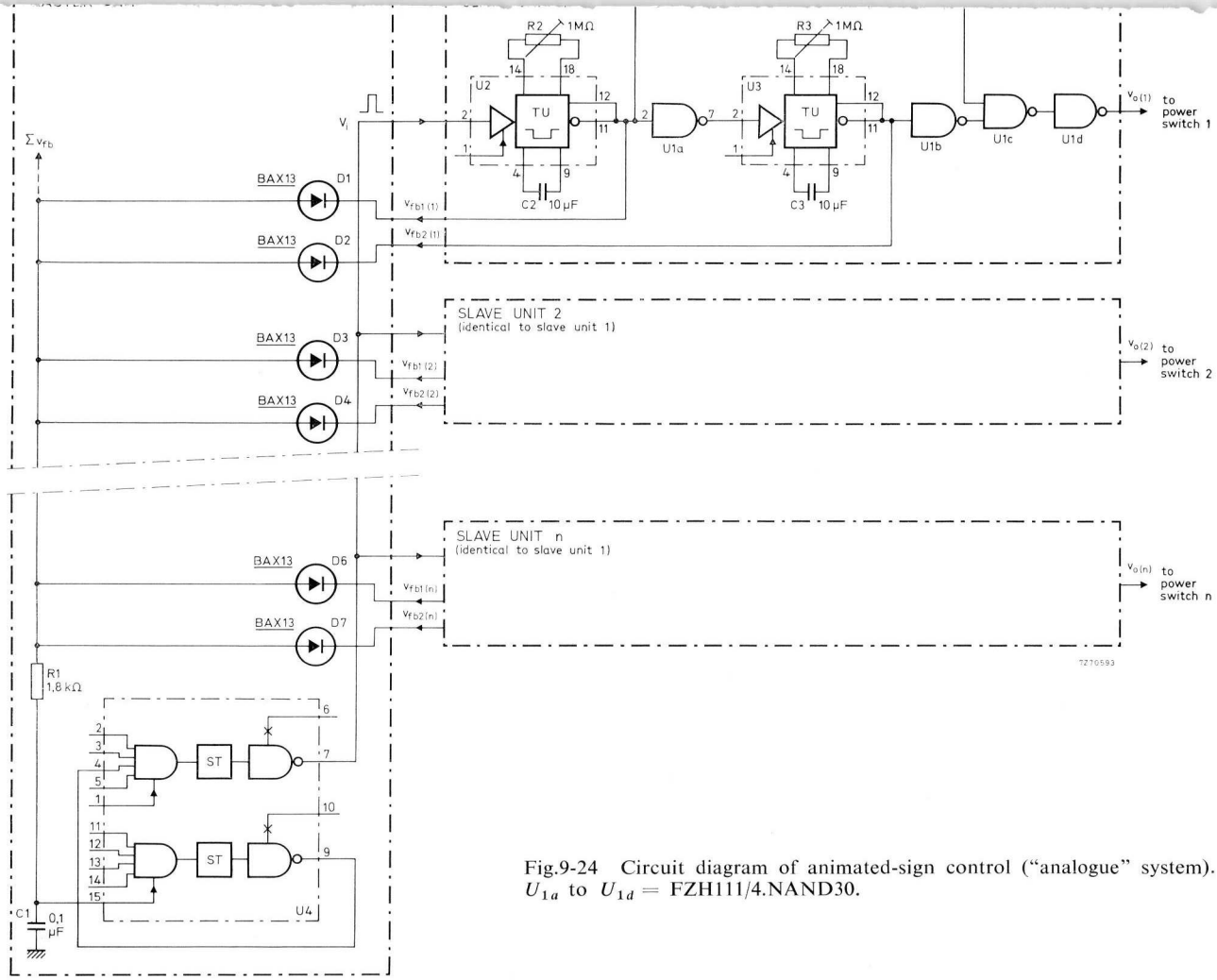


Fig.9-24 Circuit diagram of animated-sign control ("analogue" system). U_{1a} to U_{1d} = FZH111/4.NAND30.

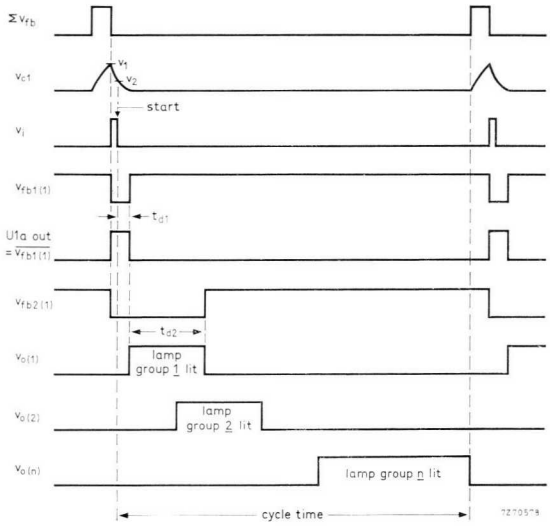


Fig.9-25. Waveforms of analogue control system.

Fig. 9-26 gives the circuit diagram of the *digital* control system. In the master unit, the 50 Hz input is rectified and converted into 100 Hz sync pulses to drive the triple decimal dividers 3×FZJ141/FF34. Each slave unit contains miniature thumbwheel switches S_1 to S_4 and bistable U_4. As soon as the position preset with "start timing" switches S_1 S_2 is reached, Q_1 becomes HIGH and U_4 is set: output v_{o1} goes HIGH and the power switch is "energized". As soon as the position preset with "stop timing" switches S_3 S_4 is reached, Q_2 becomes HIGH and U_4 is reset: output v_{o1} returns to LOW level and the power switch is "de-energized". This system has a *fixed* cycle time (10 s). One master can drive up to 3 slaves. If a higher fan-out is needed, connect 8×FZH141/2.NAND32 dual power NAND gates between $1A \ldots, \overline{1A} \ldots, 1B \ldots, \overline{1B} \ldots$ and the slave inputs, which increases the drive capability to 10 slaves per master.

Adjustment (Fig. 9-26):

1. *Adjust S_1 S_2 in any slave unit (0,1 s and 1 s settings) to set the instant of ignition of the gas-discharge tubes controlled by that particular unit.*
2. *Adjust S_3 S_4 in any slave unit (0,1 s and 1 s settings) to set the instant of extinction of the gas-discharge tubes controlled by that particular unit.*

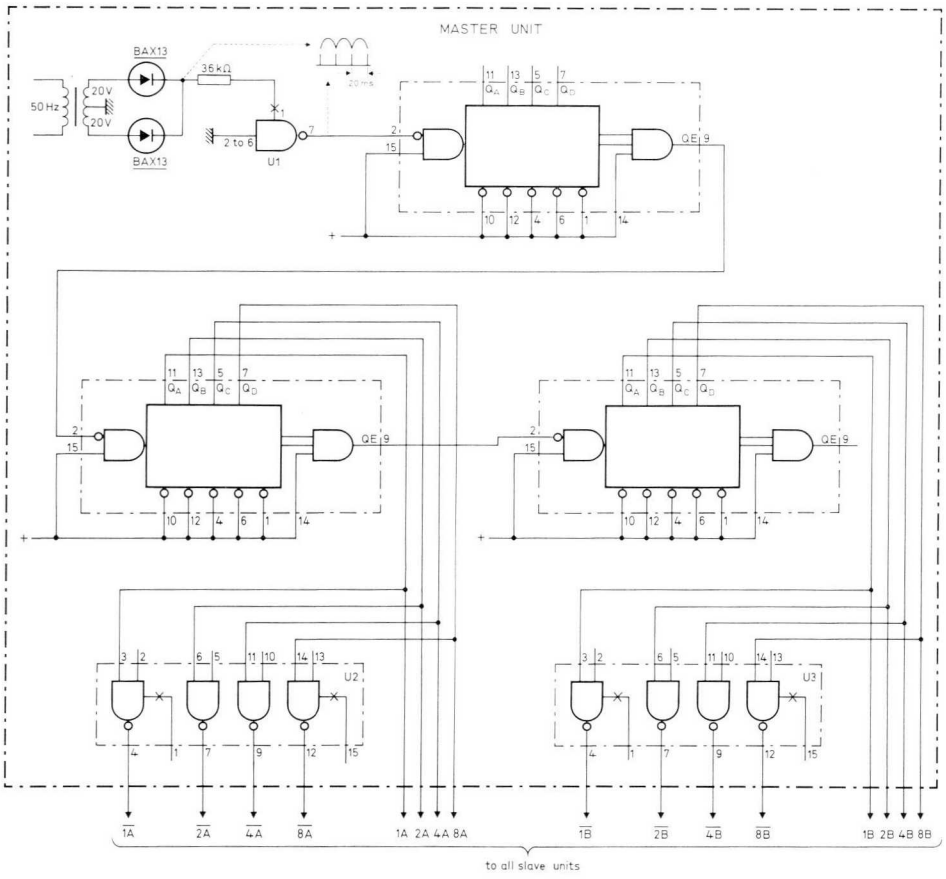
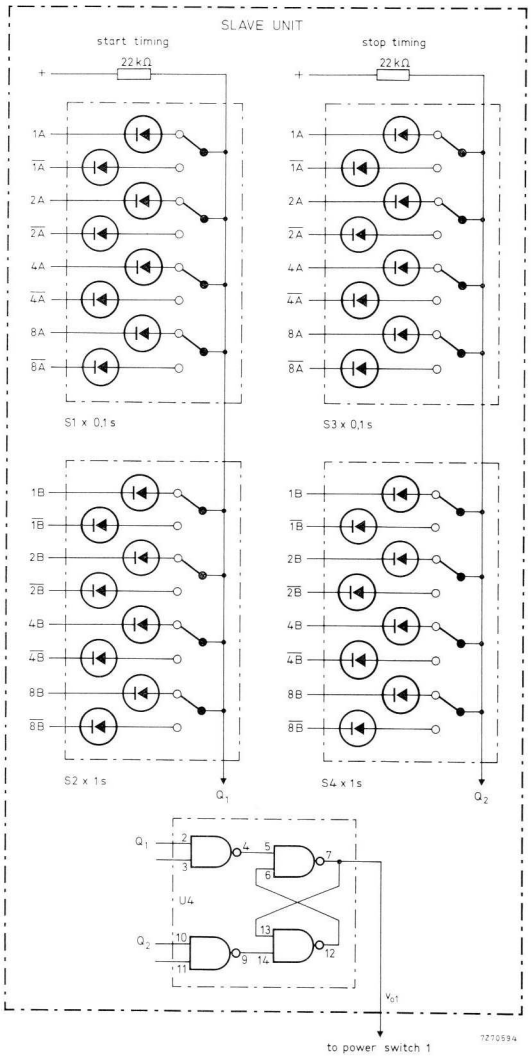


Fig.9-26 (this and opposite page) Circuit diagram of animated-sign control ("digital" system) including master unit and one of identical slave units

+ = d.c. supply (12 V or 15 V)
U_1 = FZH131/2.NAND31
U_2 to U_4 = FZH111/4.NAND30
S_1 to S_4 = miniature thumbwheel switch M1248/PC or MW1248/PC.
The three other units are FZJ141 / FF34.


SLAVE UNIT
start timing
stop timing
22 kΩ
22 kΩ
+
+
1A
1Ā
2A
2Ā
4A
4Ā
8A
8Ā
S1 x 0,1 s
S3 x 0,1 s
1B
1B̄
2B
2B̄
4B
4B̄
8B
8B̄
S2 x 1 s
S4 x 1 s
Q1
Q2
U4
Vo1
to power switch 1
7Z70594

Synchronous switch I

The circuit of Fig. 9-27 uses a silicon controlled switch (TH_1) and a reed relay (RA) to control the triac (TH_2). The mains voltage is rectified, clipped to 24 V and applied to TH_1 and RA. When TH_1 is triggered, it conducts and shorts the relay coil; the reed contact remains open and TH_2 is not triggered. When the trigger signal ceases, TH_1 conducts until the rectified voltage becomes zero, the reed relay becomes energized and the triac is triggered into conduction.

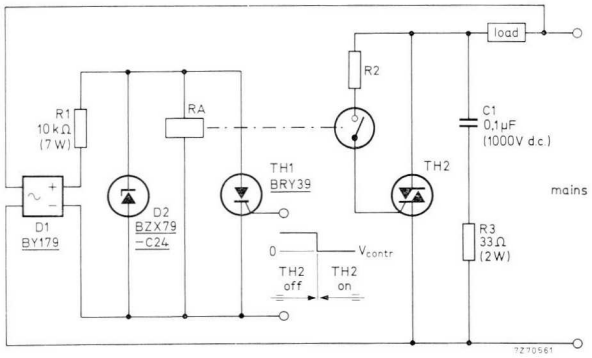


Fig.9-27 Synchronous switch using silicon controlled switch BRY39; R_2 (Ω) = mains voltage (V).

Waveforms are shown in Fig. 9-28. Operation is synchronous as TH_2 turns on when at the end of the half cycle TH_1 has turned off.

A gate series resistor is needed for TH_1 if the control voltage is high; the value of the resistor is: $R_s = (V_{contr} - 0{,}7)$ kΩ where V_{contr} is in volts (about 1 mA gate drive needed). The circuit can switch either a resistive or an inductive load.

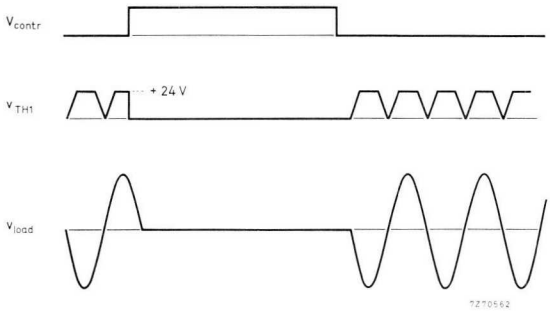


Fig.9-28 Waveforms for Fig.9-27.

Synchronous switch II[13])

The circuit of Fig. 9-29 generates short bursts of trigger pulses each half cycle. The start of the pulse bursts coincides with the mains zero cross-over points (see the waveforms), so that synchronous triggering results. Because the pulse bursts are short, a resistive or slightly inductive load can be driven (max. load phase angle equal to about 8°, which is the pulse burst length). The operation of the pulse generator is explained in Section 9.2.2.

As seen from the waveforms, the circuit only oscillates during the brief periods for which the base of shorting transistor TR_1 is not driven. The voltage across the secondary of the transformer in Fig. 9-29 is delayed in phase by R_1 C_2 R_2, rectified by D_3 D_4, then applied to the base of TR_1. By proper selection of the value of C_2, oscillations are made to start at the mains zero cross-over points.

Triggering is certain to occur for $V_{contr} \geqslant 11{,}4$ V, and triggering will certainly not take place for $V_{contr} \leqslant 1{,}8$ V.

[13]) AN No. 155: Truly Synchronous Switches; ordering code 9339 260 65501.

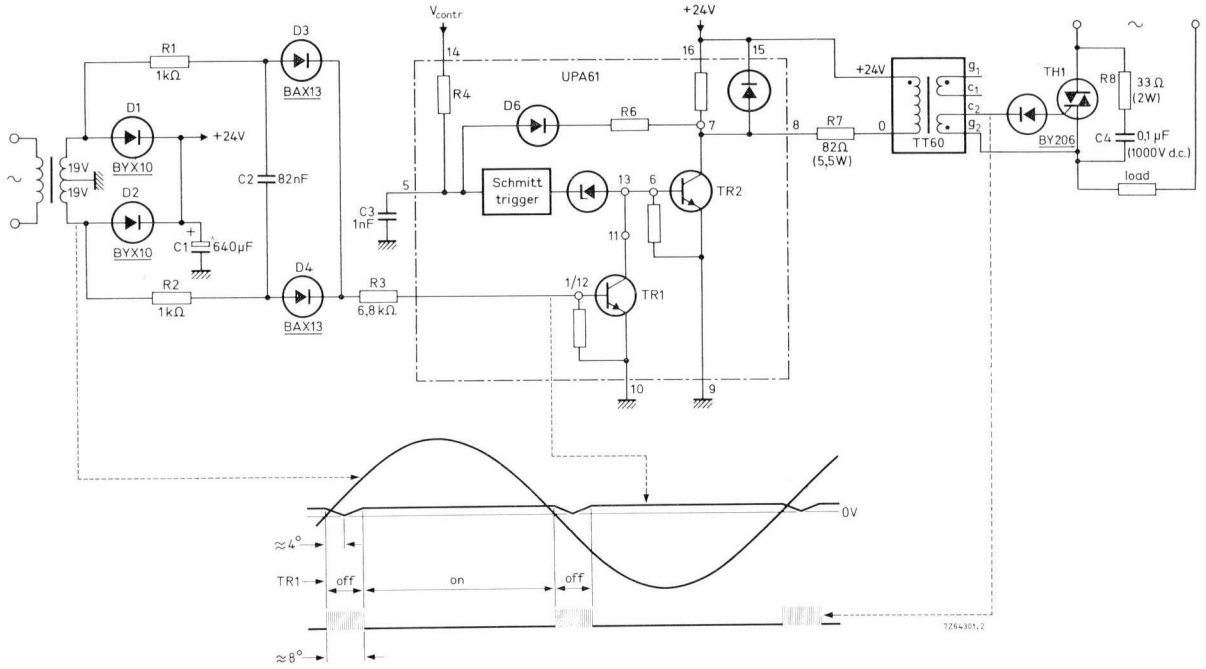


Fig.9-29 Circuit diagram and waveforms of synchronous switch.

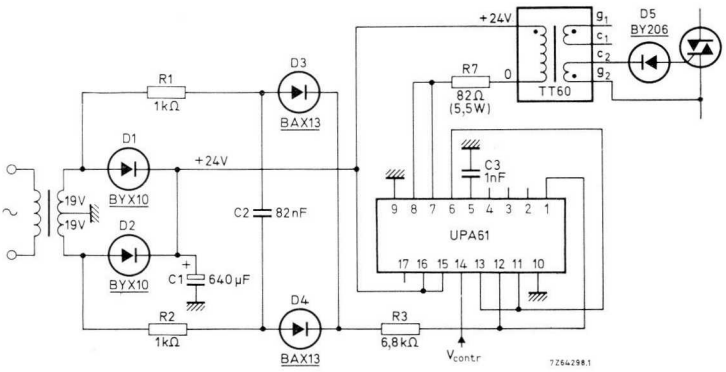


Fig.9-30 Wiring diagram of synchronous switch.

Adjustment (Fig. 9-30):
If necessary increase (decrease) the value of C_2 to retard (advance) the onset of the trigger pulse bursts, so that triggering starts coincidently with the mains zero cross-over points.

9.3.3 Single-phase switch for transformer load[14])

The circuit of Fig. 9-31 is photo-electrically controlled and load voltage is switched on for $I_{contr} \geqslant 3$ mA. The trigger angle, ϑ, is adjustable by varying the rate at which C_3 charges (adjustment of R_7), and this determines the delay at which the negative pulses, which set the difference amplifier, emerge from the ramp function generator. Owing to regenerative feedback via R_{12}, the difference amplifier can be in only one of its extreme states — set or reset — so determining whether the triac will conduct or not. Depending on the state of photo-coupler TR_{31} (conducting or not conducting), the photo-sensitive network directs either *negative* pulses from the differentiated ramp function

[14]) Elektronik, June 1973. J. Dingfelder et al — Ein Triac-Leistungsstellglied für industrielle Anwendungen.

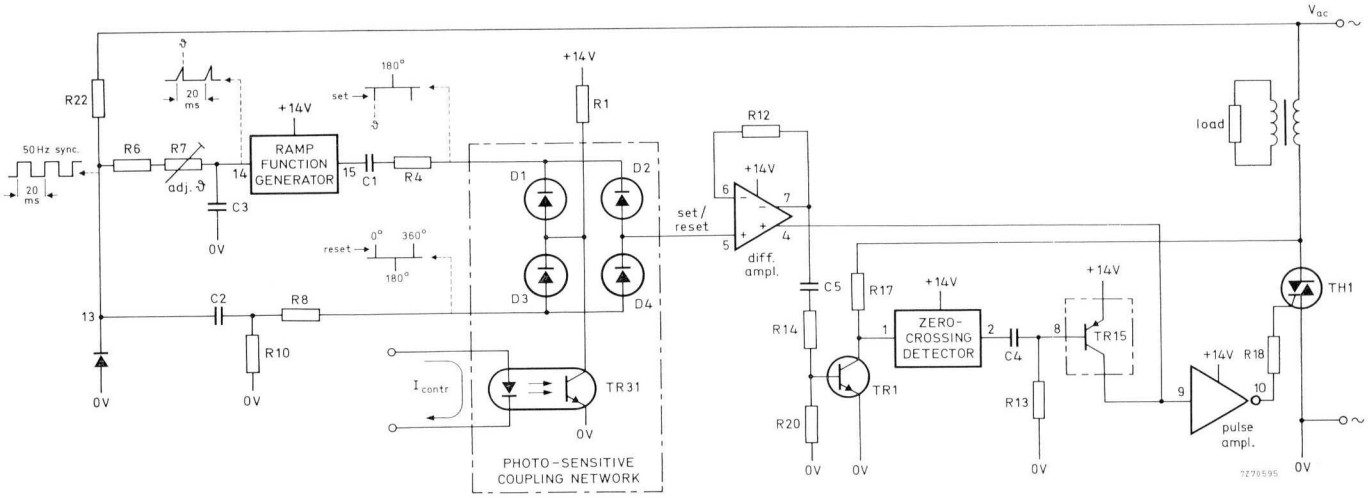


Fig.9-31 Circuit diagram of single-phase switch for transformer load (+14 V is the internal TCA280A supply).

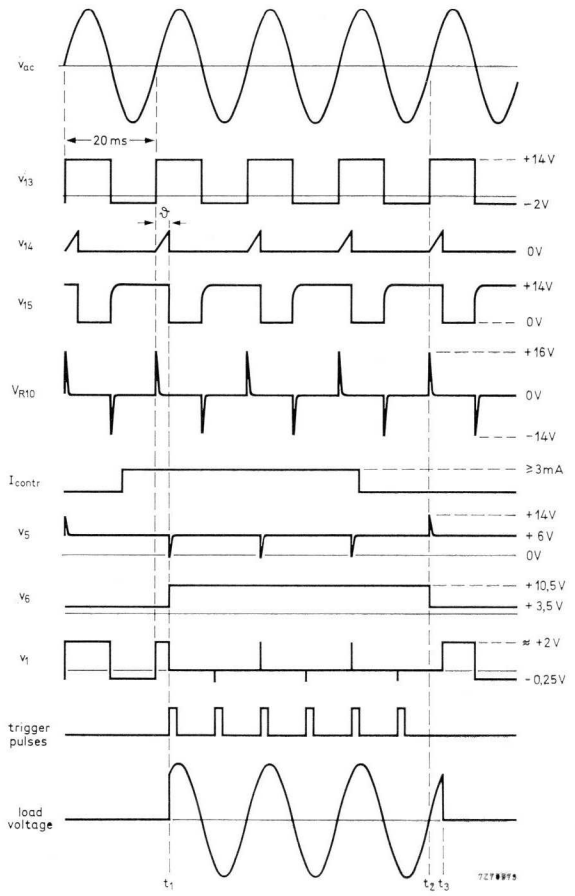


Fig.9-32 Waveforms of single-phase switch for transformer load; v_{13} = voltage at pin 13 of TCA280A, etc.

generator output (available via C_1) or *positive* pulses from the differentiated 50 Hz sync voltage (available via C_2) to input pin 5 of the difference amplifier. See the waveforms in Fig. 9-32. The first of the negative pulses sets the difference amplifier: time t_1 — output, pin 4, of the difference amplifier being high-ohmic, the input of the pulse amplifier accepts trigger pulses and the triac is triggered at the adjusted delay angle ϑ. The first of the positive pulses resets the difference amplifier: time t_2 — output, pin 4, of the difference amplifier swings positive, the input of the pulse amplifier is shorted, and the triac turns off as soon as the load current becomes zero (time t_3). During triac conduction, voltage v_1 in Fig. 9-32 will show spikes due to triac turn-off which will re-start triggering.

Fig. 9-33 illustrates a circuit variant producing negative trigger pulses (cf. Section 4.3).

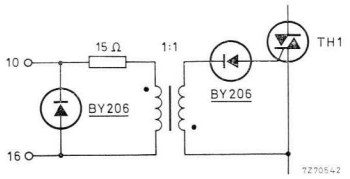


Fig.9-33 Circuit variant producing negative trigger pulses.

Adjustment (Fig. 9-34):
Set R_7 so that the transformer inrush current disappears; observe on an oscilloscope. For the required adjustment, the trigger angle must be roughly equal to the phase angle of the transformer with its load connected. So the adjustment depends on the transformer load.

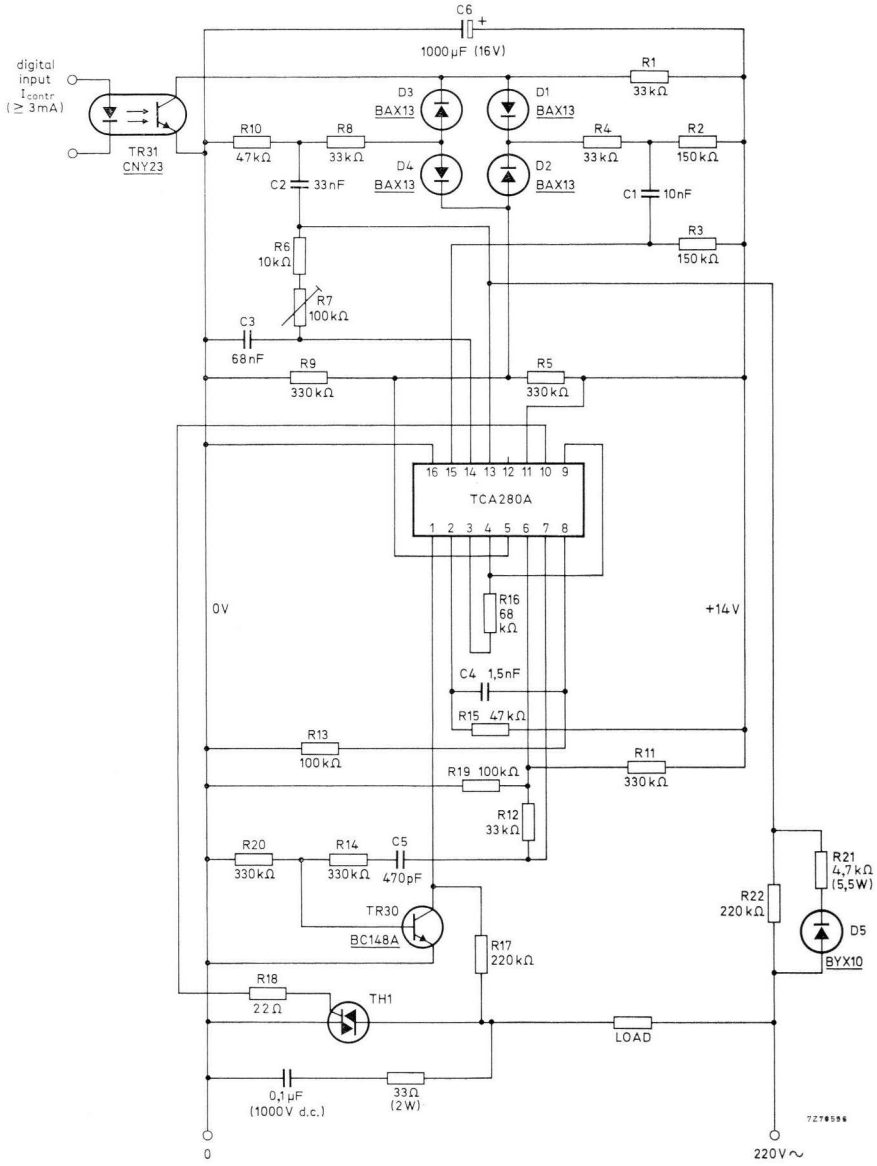


Fig.9-34 Wiring diagram of single-phase switch for transformer load.

9.3.4 Time-proportional controllers for resistive load

Time-proportional controller using TCA280A[15])

This circuit (Fig. 9-35) uses a sawtooth as the timebase for time-proportional control. The sawtooth time function is fed to input pins 5 and 6 of the difference amplifier together with the d.c. output of the temperature-sensitive bridge.

Pin 1 of the zero-crossing detector is connected to the a.c. synchronization voltage. The voltage at pin 2 collapses coincidently with the mains voltage zero crossings; this excites the pulse amplifier and causes triggering of TH_1 provided that the difference amplifier output resistance, pin 7, is high, which is the case for low temperature. For high temperature, the pulse amplifier input is shorted by the positive output of the difference amplifier and trigger pulses do not occur.

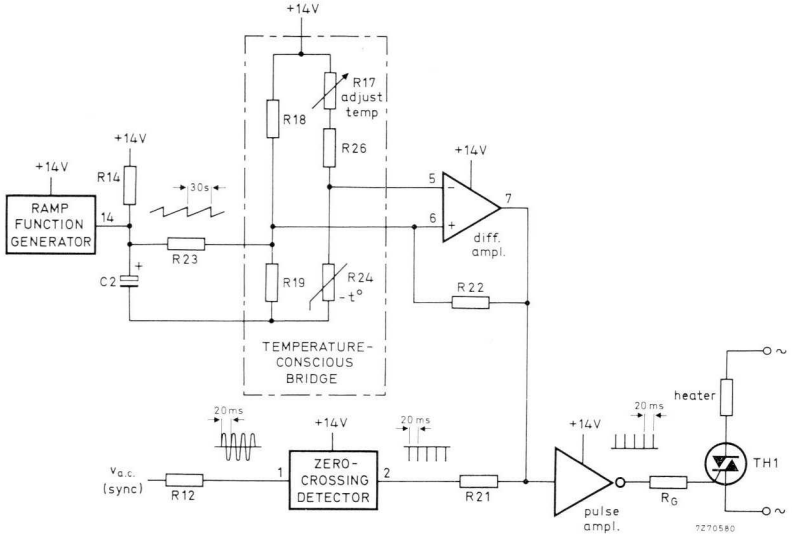


Fig.9-35 Circuit diagram of time-proportional temperature controller (+14 V is the internal TCA280A supply).

[15]) AN No. 213: Time proportional control using TCA280A trigger IC; ordering code 9399 120 71301.

As seen from the waveforms in Fig. 9-36, the duration of the trigger pulse bursts, and so the duty cycle of the triac, varies with deviation of the controlled temperature from the set value (input 6 supplied by ramp function). Regenerative feedback via R_{22} (Fig. 9-35) ensures well-defined switching of the difference amplifier.

The controller produces single trigger pulses located symmetrically with respect to the zero crossings of the mains voltage; so only resistive loads can be handled, but r.f.i. due to triac switching is very low.

Timing capacitor C_2 in Fig. 9-35 must be rated at 16 V so that leakage current is negligible.

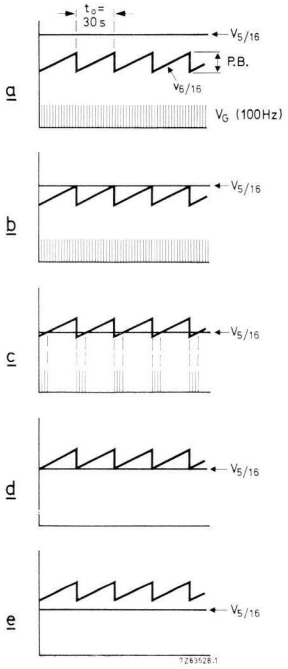


Fig.9-36 Illustrating operation of time-proportional temperature controller (P.B. = proportional band).
(a) operation above P.B. (controlled temperature low)
(b) operation at upper limit or P.B.
(c) operation within P.B.
(d) operation at lower limit of P.B.
(e) operation below P.B. (controlled temperature high).

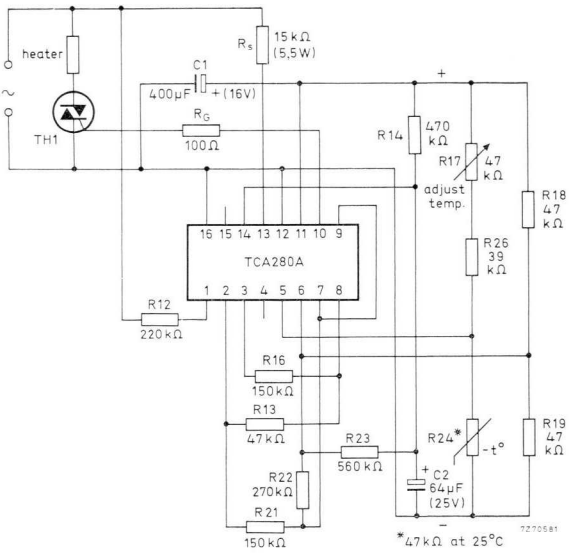


Fig.9-37 Lay-out of time-proportional temperature controller.

Adjustment (Fig. 9-37):

1. *Adjust the proportional band by selection of the value of* R_{23} *(a lower* R_{23}*-value widens the proportional band).*
2. *With* C_2 *adjust the repetition period of time-proportional control (repetition period about 0,14 s/µF).*

Time-proportional temperature controller using 61-series NORbits[16])

In the automatic temperature controller shown in Fig. 9-38, the error amplifier is fed by the temperature-sensitive bridge, R_1 to R_{12}; R_9 is the temperature sensor, and temperature is adjusted with R_1. The system tolerates $\pm 30\%$ mains fluctuations. Circuit operation is as follows.

As long as the output of the rectangular-pulse generator is LOW, amplifier A_6 is held in saturation by the synchronization voltage V_{sync}, except for the short intervals coinciding with the zero crossings of the mains voltage. During these intervals, A_6 is cut off and so cannot short the input to A_4. The pulse generator triggers the triacs which supply power to the heaters. Because the pulse bursts are of short duration, only a resistive load can be controlled. The HIGH output of the rectangular-pulse generator supplies base current to A_6 keeping it in saturation, the trigger pulse generator cannot function, and the triacs do not conduct. (The operation of the trigger pulse generator is explained in Section 9.2.2.)

16) AN No. 167: Time-proportional Temperature Controller; ordering code 9399 260 66701.

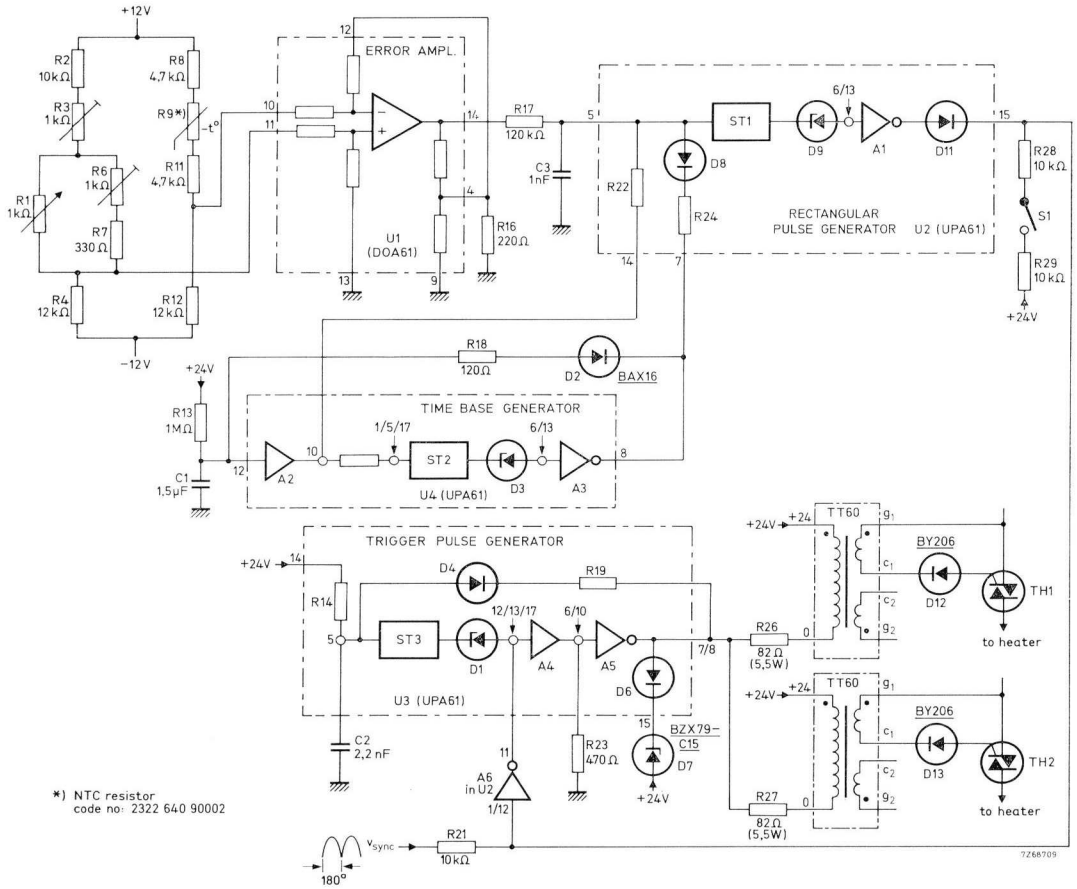


Fig.9-38 Schematic diagram of time-proportional temperature control system. ST_1, ST_2, ST_3 = Schmitt triggers.

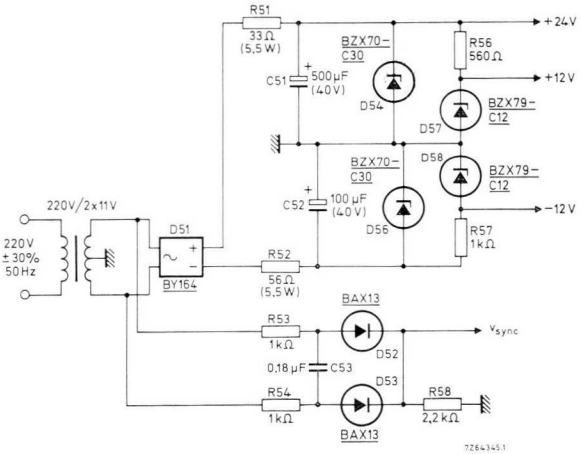


Fig.9-39 D.C. supply and synchronization circuit.

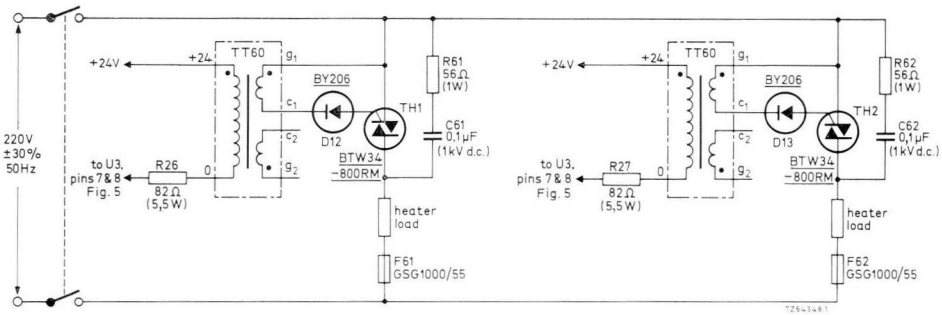


Fig.9-40 Power circuit.

With decreasing temperature, the potential at the inverting input of the error amplifier decreases and that of the amplifier output increases. As a result, the duty cycle of the rectangular-pulse generator output decreases and the average power supplied to the heaters increases, counteracting the decrease in temperature. Closure of S_1 switches off the heater supply.

Fig. 9-39 shows the d.c. supply and synchronization circuit. Network $R_{53}\,C_{53}\,R_{54}$ delays V_{sync}, so that triac triggering starts at the mains zero cross-over points. Fig. 9-40 shows the power circuit. Mounted on an 11 cm extruded aluminium heatsink type 56293 (blackened), each triac can handle 6,25 kW, taking into account 35 °C ambient temperature and $\pm$ 30% a.c. input fluctuations. Because up to four triacs can be triggered, the total power handling capacity is 25 kW.

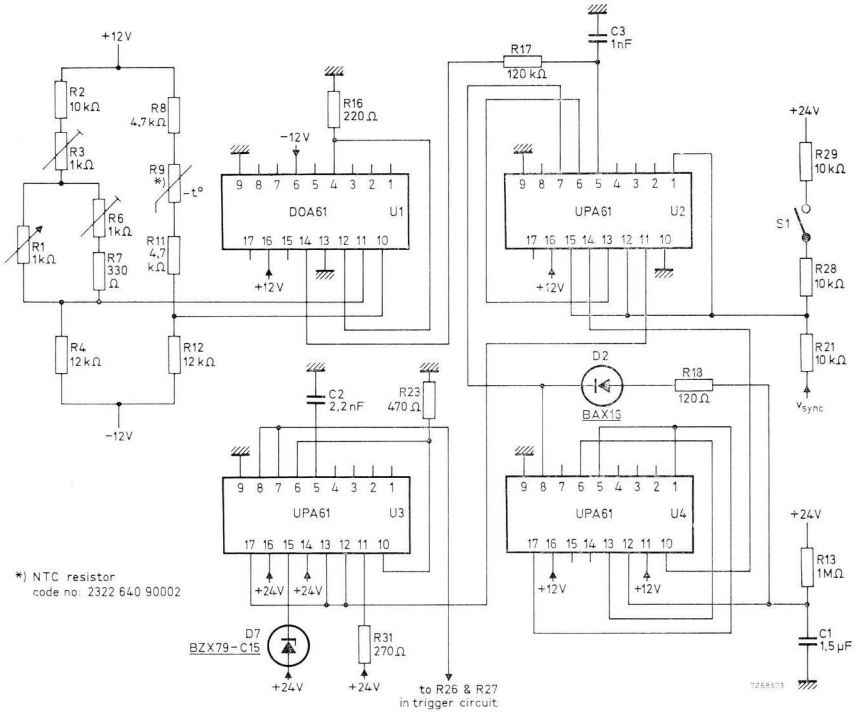


Fig. 9-41 Wiring diagram of time-proportional temperature control system.

Adjustment (Fig. 9-41):

1. *Set R_1, R_3 and R_6 to minimum resistance.*
2. *Expose temperature sensor R_9 to 23 °C and adjust R_3 so that the output of the error amplifier (U_1 pin 14) is zero.*
3. *Set temperature-adjust potentiometer R_1 to maximum resistance.*
4. *Expose temperature sensor R_9 to 18 °C and adjust R_6 so that the output of the error amplifier is zero.*
5. *Increase the value of R_{16} if control instability arises; a value of R_{16} up to 1 kΩ will be satisfactory in most cases.*
6. *It may be necessary for optimum control performance to change the repetition period of the time-proportional control system, this is achieved by changing the value of R_{13} (repetition period t_o read from Fig 9-43 — Section 9.3.5 — when substituting R_{13} for R); if necessary, increase C_1 to obtain a larger value for t_o.*

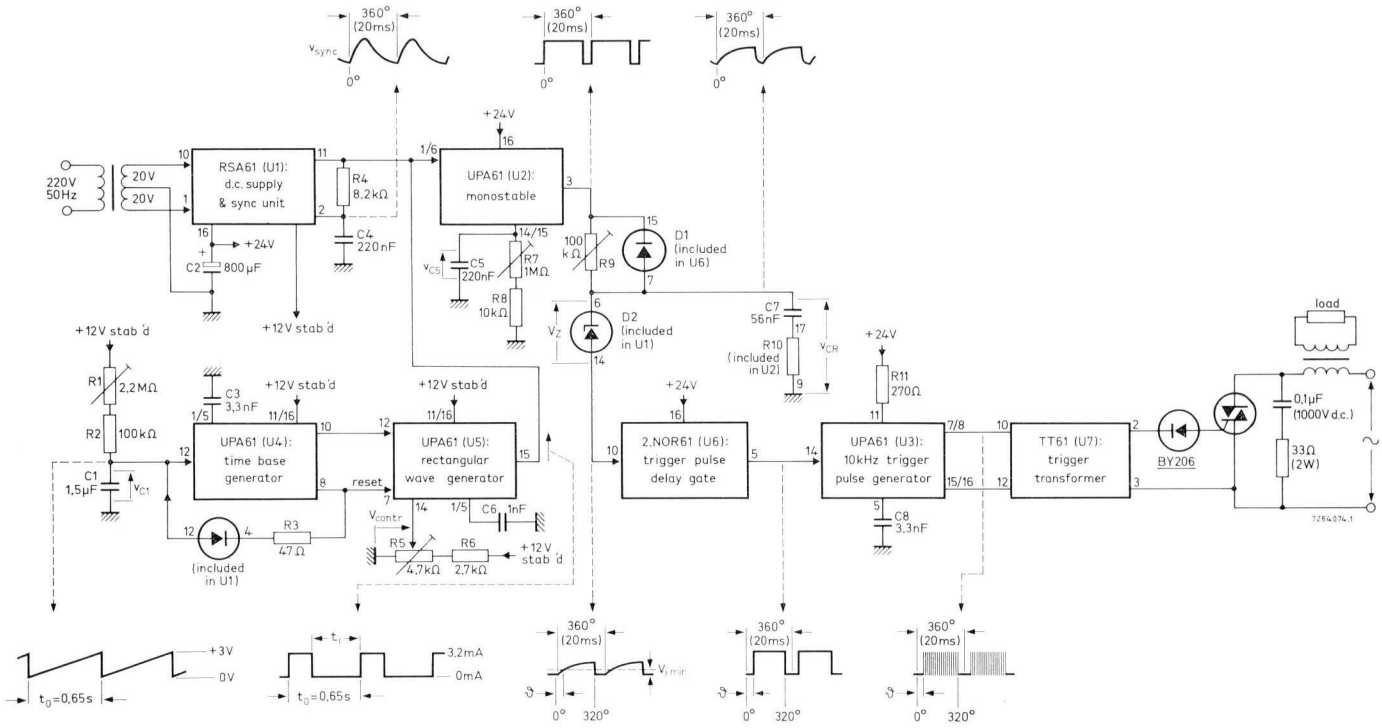


Fig.9-42 Time-proportional controller with adjustable trigger delay (ϑ). For R_1 set to 900 kΩ, the repetition period, t_o, is 0,65 s as shown.

9.3.5 Single-phase time-proportional controller for transformer load[17])

Fig. 9-42 shows a circuit allowing a trigger delay up to about 50°. Circuit operation is clear from the waveforms. The leading edges of the monostable output pulses are delayed while passing through charging network R_9 C_7 R_{10} and the trigger pulse delay gate. The duration of trigger delay, ϑ, depends on the charge rate of C_7 and is adjusted with R_9. Diode D_1 ensures rapid discharge of C_7 at the end of the monostable output pulses, and D_2 provides level shifting. The output of the trigger pulse delay gate will certainly be HIGH (trigger pulses generated) for a d.c. gate input of 4 V or higher; it will become LOW with certainty (trigger pulses inhibited) when the d.c. gate input is 0,4 V, or lower. Average output power is controlled with R_5.

Fig. 9-43 shows the relationship between the repetition frequency (or repetition period) of time-proportional control and $(R_1 + R_2)$ in Fig. 9-42.

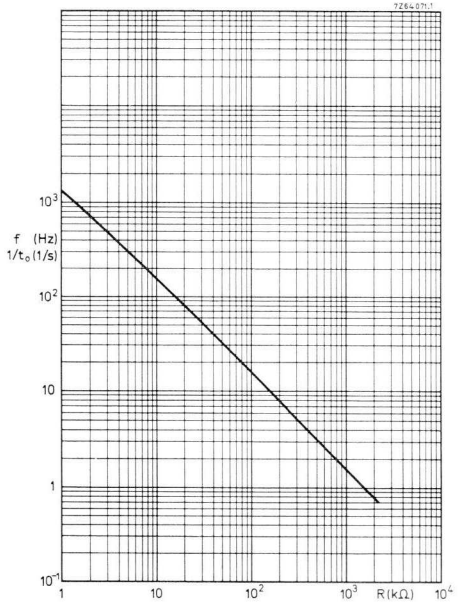


Fig.9-43 Pulse repetition frequency f vs. capacitor charge resistor R $(R_1 + R_2$ in Fig.9-42).

[17]) AN No. 142: Time-proportional Controller for Transformer Loads; ordering code 9399 260 64201.

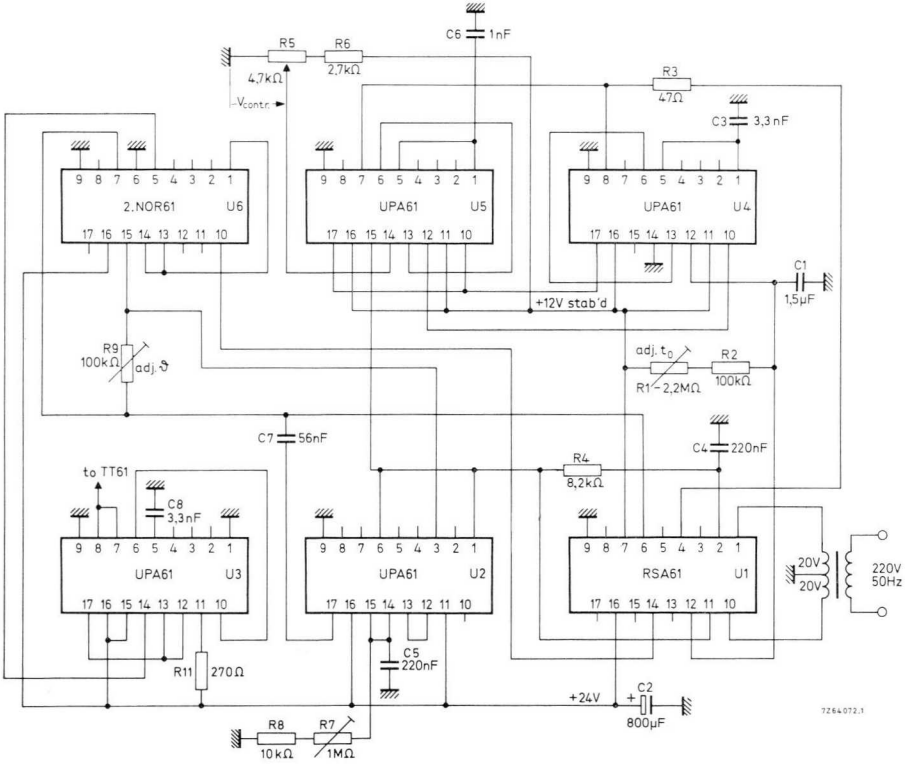


Fig.9-44 Wiring diagram of time-proportional controller with adjustable trigger delay.

Adjustment (Fig. 9-44):

1. *Set the repetition period of time-proportional control, t_o, to the desired value by adjusting R_1 (cf. Fig. 9-43); if necessary increase C_1 to obtain a higher value for t_o.*
2. *Set R_7 to obtain a trigger pulse burst duration (U_3 pin 8) of about 300° (17 ms at a 50 Hz supply).*
3. *The trigger delay required to prevent a repetitive transformer inrush current is obtained as follows:*
   - *3a. Connect a d.c. voltmeter, with not less than 10 kΩ/V resistance, across the transformer primary through a 100 kΩ, 10 µF smoothing filter (the capacitor must be an a.c. type).*
   - *3b. Adjust R_5 so that one or only a few a.c. cycles occur per repetition period t_o.*
   - *3c. With R_9 set the trigger delay so that at the given transformer load the meter deflection becomes zero.*
     Re-adjustment of R_9 may be necessary if the transformer load changes.

9.3.6 THREE-PHASE TIME-PROPORTIONAL CONTROLLER

Fig. 9-45 shows the trigger pattern for the two-triac switch[18]) used in the controller; this pattern allows control of a very inductive load. In the circuit shown in Fig. 9-46 using FZ/30-series modules[19]), the trigger pulse bursts are initiated by the 200 μs sync pulses from gates U_{2a} U_{2b}, these pulses being derived from phases *BY* and *RO* — see waveforms Fig. 9-47. The lengths of the trigger pulse bursts are determined by the TU30 timers U_4 and U_5; that is, the trigger pulses are passed by the trigger pulse gates as long as inputs 1 and 17 are HIGH.

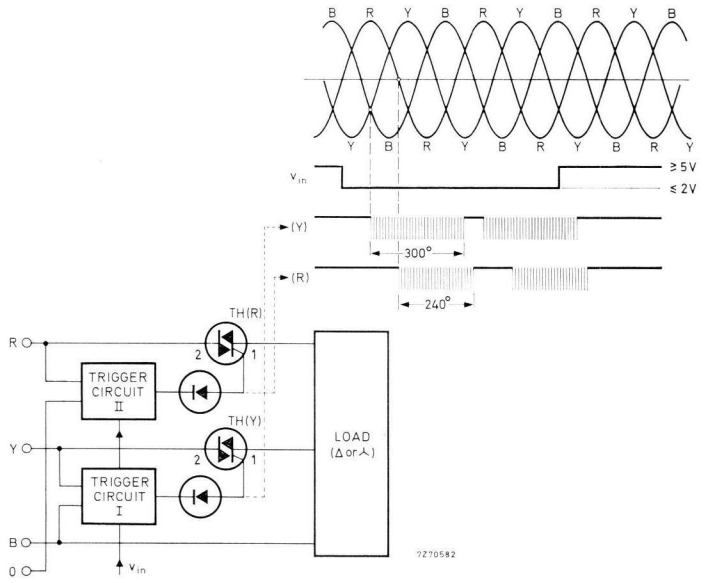


Fig.9-45 Trigger pattern of two-triac switch used in three-phase time-proportional controller.

[18]) Application Book: Thyristor and Triac Power Control Using 61-series Modules; ordering code 9399 266 02601.

[19]) A1 No. 471: FZ/30-Series Circuit Blocks; ordering code 9399 324 47101.

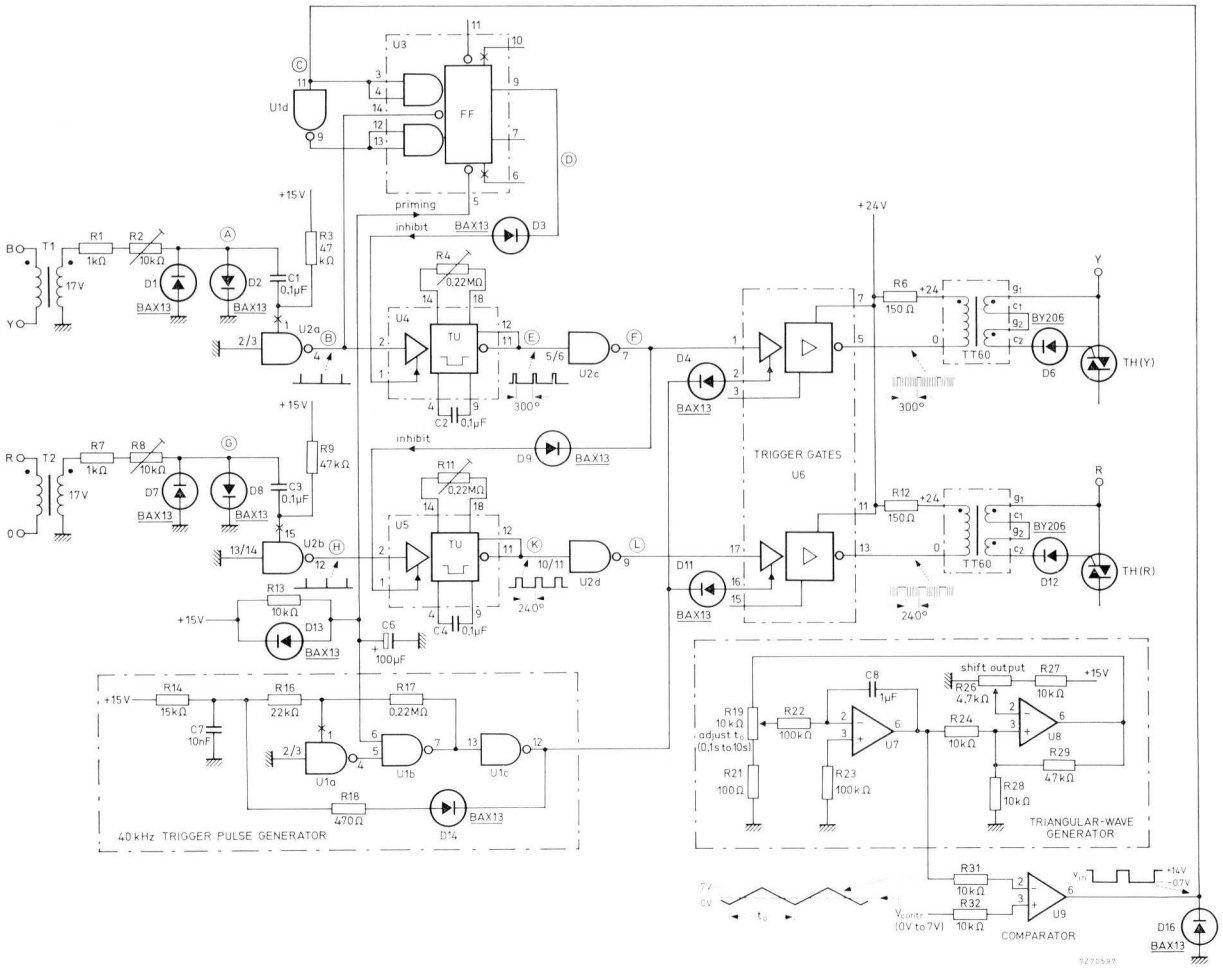

U3
FF
U1d
priming
inhibit
BAX13
D3
+15V
T1
R1 1kΩ
R2 10kΩ
D1
D2
C1 0,1µF
R3 47 kΩ
17V
U2a
2/3
U4
TU
R4 0,22MΩ
C2 0,1µF
5/6
U2c
300°
D4
+24V
R6 150Ω
TT60
BY206
D6
TH(Y)
Y
TRIGGER GATES
U6
T2
R7 1kΩ
R8 10kΩ
D7
D8
C3 0,1µF
R9 47kΩ
U2b
13/14
U5
R11 0,22MΩ
C4 0,1µF
10/11
U2d
240°
D11
R12 150Ω
D12
TH(R)
R
R13 10kΩ
D13
C6 100µF
R14 15kΩ
C7 10nF
R16 22kΩ
R17 0,22MΩ
U1a
U1b
U1c
R18 470Ω
D14
40 kHz TRIGGER PULSE GENERATOR
C8 1µF
R19 10kΩ adjust t_0 (0,1s to 10s)
R22 100kΩ
U7
R21 100Ω
R23 100kΩ
shift output
R26 4,7kΩ
R27 10kΩ
R24 10kΩ
U8
R29 47kΩ
R28 10kΩ
TRIANGULAR-WAVE GENERATOR
7V
0V
t_0
R31 10kΩ
R32 10kΩ
V_{contr} (0V to 7V)
U9
COMPARATOR
V_{th}
+14V
-0,7V
D16
BAX13

Fig.9-46 (opposite page) Circuit diagram of three-phase time-proportional controller.
U_1 U_2 = FZH111/4.NAND30
U_3 = FZJ101/FF30
U_4 U_5 = TU30
U_6 = 2.LRD30
U_7 U_8 U_9 = TBA221.

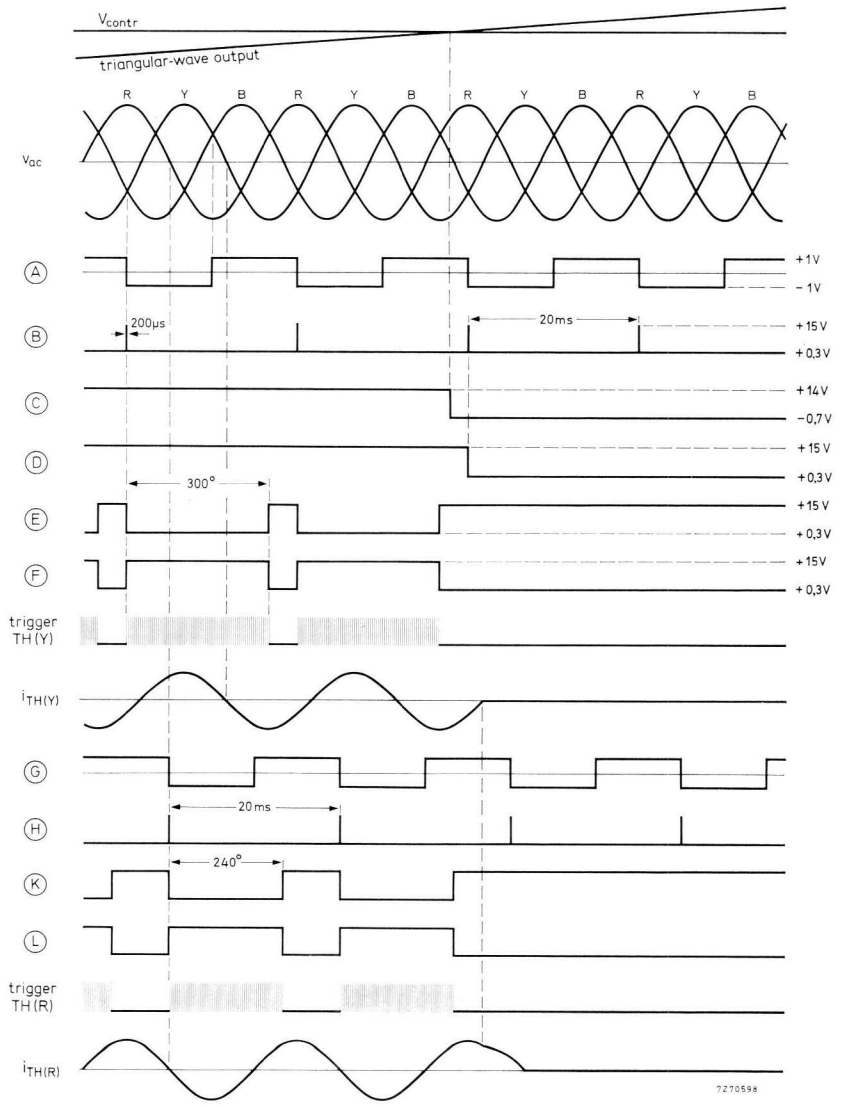


Fig.9-47 Waveforms for Fig.9-46.

The triangular-wave generator provides time-proportional control. When the instantaneous triangular-wave output voltage is below V_{contr}, the comparator produces a HIGH output (v_{in}) which has no effect. When the instantaneous triangular-wave output voltage is larger than V_{contr}, the comparator output becomes LOW (−0,7 V), causing the flip-flop (U_3) Q_1 output to switch to LOW level. This inhibits timer U_4, the HIGH output from which inhibits timer U_5. With the output of gates U_{2c} and U_{2d} LOW, trigger pulses do not occur and the triacs turn off. When V_{contr} increases from 0 V to 7 V, the average a.c. output increases from 0% to 100%.

Network R_{13} C_6 inhibits the trigger pulse generator for 0,1 s after switch-on, so that spurious triggering cannot occur. Because C_6 is initially uncharged, a LOW-level priming voltage is fed to terminal 5 of U_3 causing this flip-flop to reset (Q_1 LOW). Diode D_{13} rapidly discharges C_6 when the circuit is disconnected. Because of the 360° spacing of the sync pulses, the circuit produces an integral number of load cycles.

Adjustment:

1. *Check that phase sequence is according to Fig. 9-47.*
2. *Make sure that T_1 and T_2 in Fig. 9-46 are connected as indicated by the dots.*
3. *Set R_2, Fig. 9-46, so that upon triggering there is no step increase in the voltage between main terminal 1 of TH(Y) and phase B (Fig. 9-45).*
4. *Set R_8, Fig. 9-46, so that upon triggering there is no step increase in the voltage between main terminal 1 of TH(R) and neutral.*
5. *Adjust R_4 so that the trigger pulse bursts fed to TH(Y) have a duration of 300° (about 17 ms with a 50 Hz supply).*
6. *Adjust R_{11} so that the trigger pulse bursts fed to TH(R) have a duration of 240° (about 13 ms with a 50 Hz supply).*
7. *Adjust R_{26} so that the a.c. output power just becomes zero for V_{contr} at zero volts.*
8. *With R_{19} set the required repetition period t_o.*

9.3.7 Three-phase time-proportional controller for transformer load

Transformer inrush currents do not occur if triggering is delayed until the instant when the steady-state primary current passes through zero. The trigger pattern shown in Fig. 9-48b for the circuit of Fig. 9-48*a* meets this specification:

see the dashed and full-line portions of $i_{TH(Y)}$ and $i_{TH(R)}$. Triac $TH(B)$ is permanently conducting; its presence is necessary to obtain the 2 V on-state voltage drop that occurs in the other two phases and thus avoid voltage unbalance between the phases, which could bring about drift of the transformer magnetization with the consequent risk of core saturation. In a particular half cycle, $t_{1\,min}$ and $t_{2\,min}$ are the earliest possible instants of triggering of $TH(Y)$ and $TH(R)$ respectively. As seen, the first half-cycle trigger angle ϑ_Y of $TH(Y)$ is equal to $\varphi_{load} + 30°$ (φ_{load} is the load phase angle) and the first-half cycle trigger angle ϑ_R of $TH(R)$ equals φ_{load}.

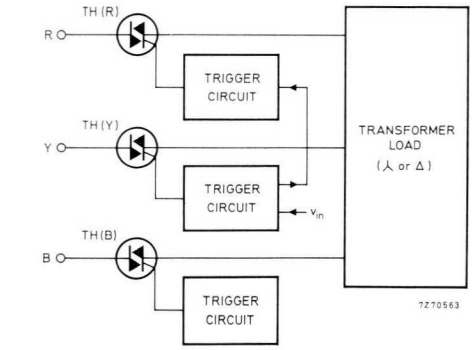
In the circuit diagram of Fig. 9-49, U_3 and U_4 are monostable multivibrators whose output pulse widths determine the first half-cycle trigger angles of the triacs — see waveforms *B* and *G* in Fig. 9-50. For v_{in} HIGH, these monostables are triggered by the sync pulses — waveforms *A* and *F* — from U_{1a} and U_{1d}; the monostables set flip-flops U_{5a} and U_{5b} to start triac triggering. The flip-flops are reset by the sync pulses. For v_{in} LOW, monostable U_3 cannot produce output pulses; U_{5a} remains in the reset state with Q_2 LOW, thus inhibiting U_4. Because U_{5b} also remains reset, inputs 1 and 17 of trigger pulse gates U_{6a} and U_{6b} remain LOW so that the trigger pulses are inhibited. Gate U_{1c} prevent unintentional resetting of U_{5a} — with the consequent interruption of triggering $TH(Y)$ — if v_{in} goes LOW while a sync pulse occurs at the output of gate U_{1a}.

The triangular-wave generator and comparator are discussed in the previous Section.

Adjustment:

1. *Check that the phase sequence is according to Fig. 9-50.*
2. *Ensure that T_1 and T_2 in Fig. 9-49 are connected as indicated by the dots.*
3. *Adjust R_7 to obtain a pulse witdh of about 6 ms at pin 7 of U_3.*
4. *Adjust R_9 to obtain a pulse width of about 4,5 ms at pin 7 of U_4.*
5. *Adjust the triangular-wave generator so that the repetition frequency of v_{in} is about 1 Hz (see previous Section, "Adjustment", item 8).*
6. *With the transformer unloaded adjust R_7 so that there is no d.c. current in phase Y, and adjust R_9 so that there is no d.c. current in phase R.*
7. *Adjust the triangular-wave generator as described in the previous Section, "Adjustment", items 7 and 8.*

Fig.9-49 (opposite page) Circuit diagram of three-phase time-proportional controller for transformer load. Triangular-wave generator and comparator circuit shown in Fig.9-46.
$U_{1a,b,c,d}$ = FZH111/4.NAND30
$U_{2a,b}$ = FZH141/2.NAND32
U_3, U_4 = FZK101/OS30
$U_{5a,b}$ = FZJ121/2.FF32
$U_{6a,b}$ = 2.LRD30
$U_{7a,b}$ = FZH241/2.AST30
U_{8a} = $\frac{1}{2}\times$2.LRD30



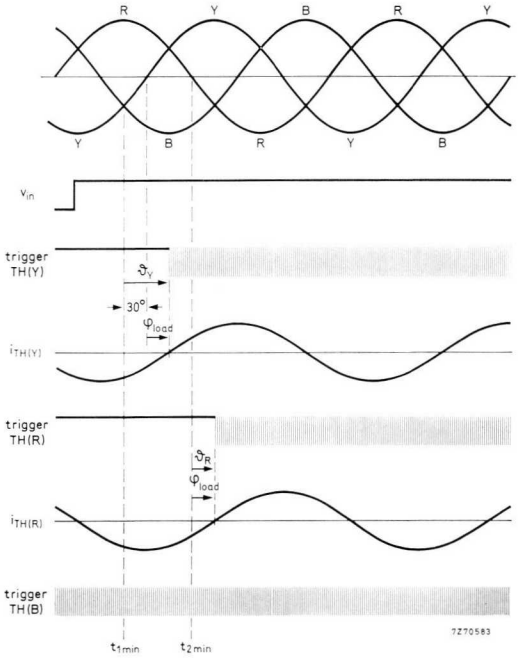
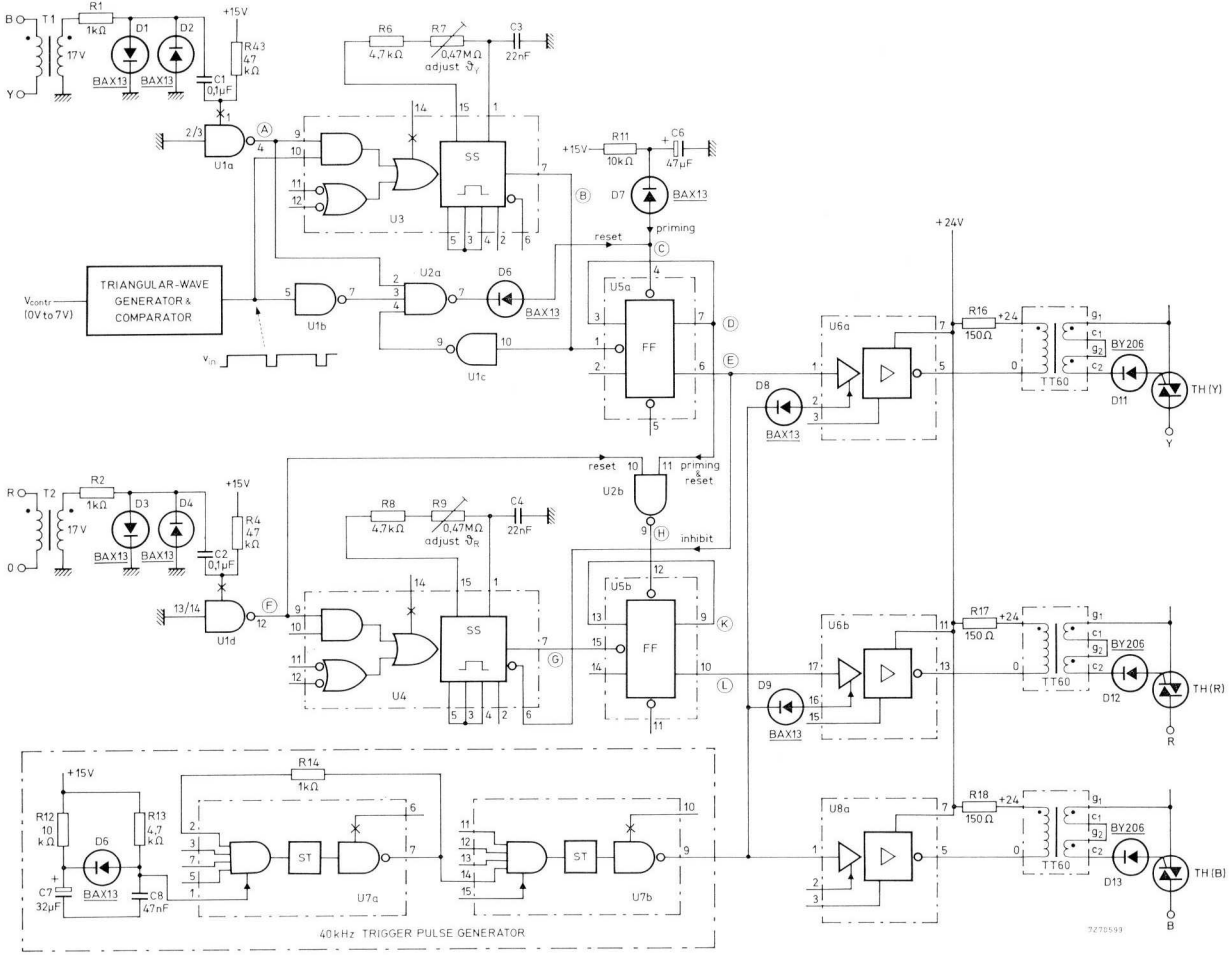


Fig.9-48 Showing (a) power circuit (b) trigger pattern to prevent transformer inrush current; ϑ_Y and ϑ_R are the initial trigger angles of, respectively, $TH(Y)$ and $TH(R)$.


B
T1
Y
17 V
R1
1kΩ
D1
D2
BAX13
BAX13
C1
0,1µF
+15V
R43
47
kΩ
2/3
U1a
A
R6
4,7kΩ
R7
0,47MΩ
adjust ϑf
C3
22nF
14
15
1
SS
U3
9
10
11
12
7
5
3
4
2
6
B
+15V
R11
10kΩ
C6
47µF
D7
BAX13
priming
reset
C
TRIANGULAR-WAVE
GENERATOR &
COMPARATOR
Vcontr
(0V to 7V)
vin
U1b
U2a
D6
BAX13
U1c
U5a
FF
D
E
+24V
U6a
R16
150Ω
+24
g1
c1
g2
BY206
c2
TT60
D11
TH(Y)
Y
D8
BAX13
R
T2
0
17 V
R2
1kΩ
D3
D4
BAX13
BAX13
C2
0,1µF
+15V
R4
47
kΩ
13/14
U1d
F
R8
4,7kΩ
R9
0,47MΩ
adjust ϑR
C4
22nF
U4
SS
G
reset
10
11
priming
&
reset
U2b
H
inhibit
U5b
FF
K
L
U6b
R17
150Ω
+24
BY206
TT60
D12
TH(R)
R
D9
BAX13
R14
1kΩ
+15V
R12
10
kΩ
R13
4,7
kΩ
D6
BAX13
C7
32µF
C8
47nF
ST
U7a
ST
U7b
40kHz TRIGGER PULSE GENERATOR
U8a
R18
150Ω
+24
BY206
TT60
D13
TH(B)
B
7270599

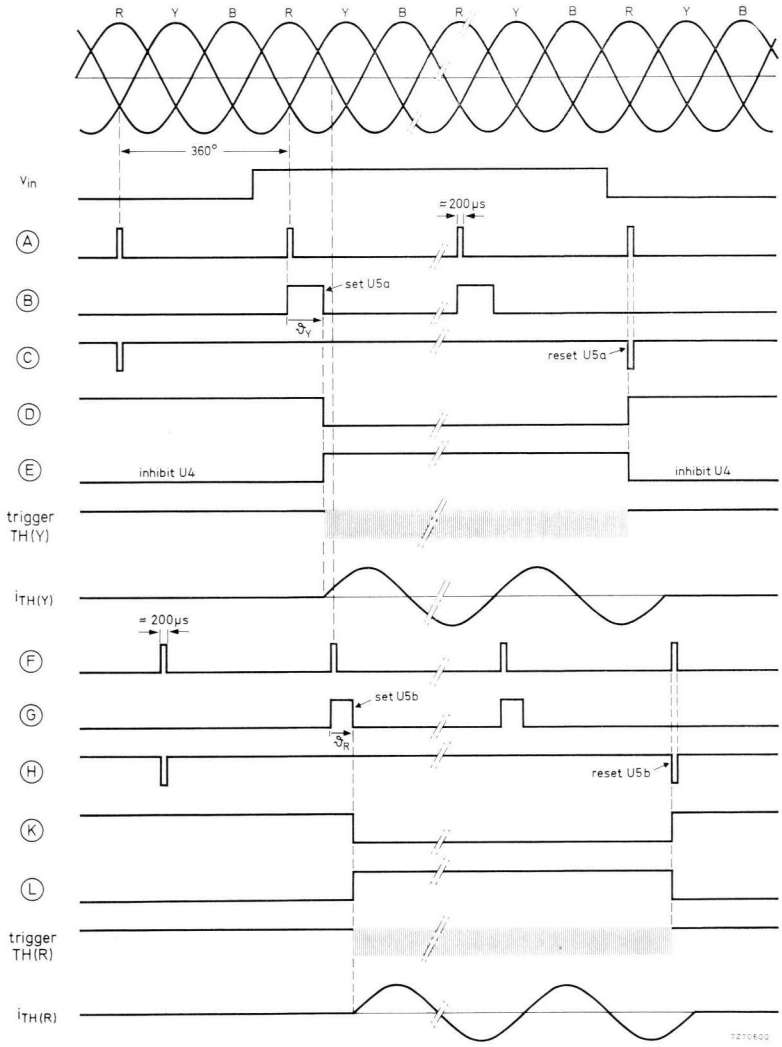


Fig.9-50 Waveforms for Fig.9-49; ϑ_Y and ϑ_R are the initial trigger angles for $TH(Y)$ and $TH(R)$, respectively.

9.4 Solid-state continuous controllers

9.4.1 Circuit survey

Table 9-5 summarizes the circuits discussed here.

Table 9-5 Solid-state continuous controllers

section	circuit	features	number of triacs used
9.4.2	single-phase controller	for resistive & inductive load	1
9.4.3	three-phase full-controlled controller	for resistive & inductive load (star- or delta-connected)	3
9.4.4	2 kVA battery charger	for automatic battery charging	3

9.4.2 Single-phase controller with rectification

In the circuit of Fig. 9-51, a single-phase bridge rectifier is controlled by varying its a.c. input (circuit designed to control the d.c. input to an inverter); a triac functions as the control element (phase control).

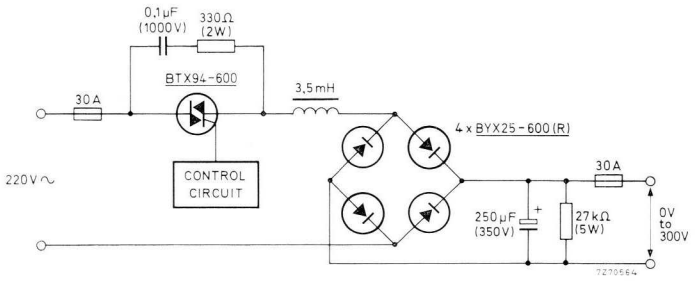


Fig.9-51 0 V to 300 V, 30 A controlled rectifier.

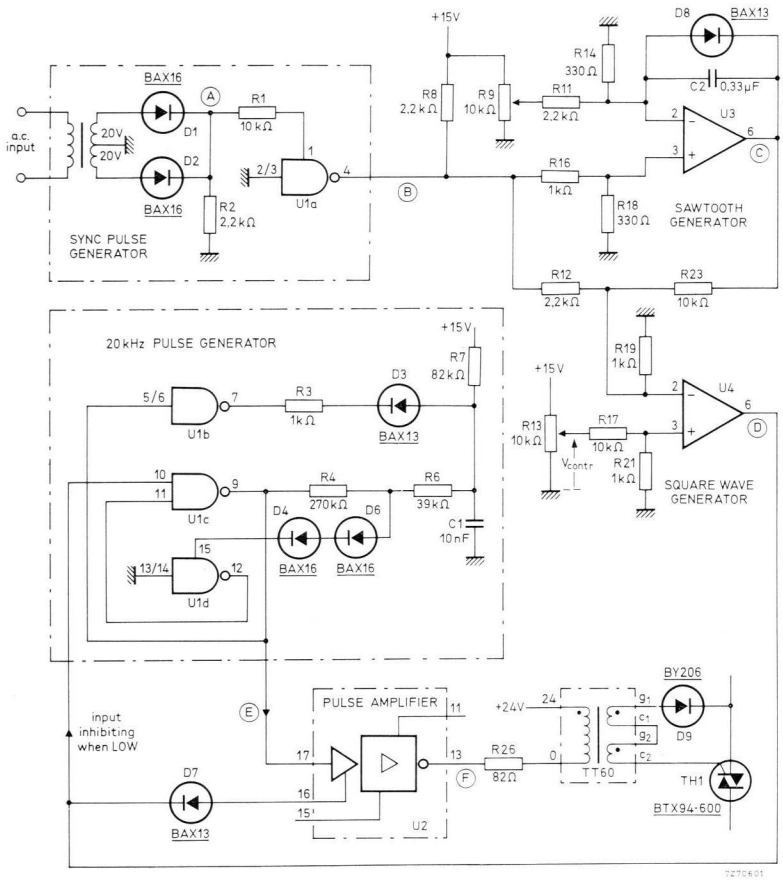


Fig.9-52 Rectifier control circuit; waveforms *A* to *E* in Fig.9-53.
U_1 = FZH111/4.NAND30
U_2 = 2.LRD30
U_3, U_4 = TBA221.

Adjustment (Fig. 9-52):
Set R_{13} to its minimum resistance and adjust R_9 so that the rectifier output is just zero. Set R_{13} to its highest resistance and check that rectifier output is approximately 300 V at 30 A load current.

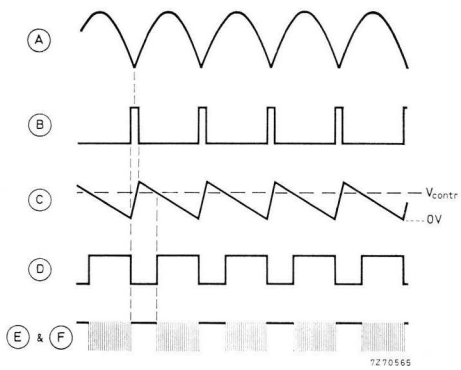


Fig.9-53 Waveforms for Fig.9-52.

The control circuit and its waveforms are given in Figs 9-52 and 9-53. The SYNC PULSE GENERATOR converts the full-wave rectified input *A* into pulses *B*, which coincide with the mains zero crossings; these pulses synchronize the SAWTOOTH GENERATOR. The sawtooth generator output, waveform *C*, is fed via R_{23} to the inverting input of the SQUARE-WAVE GENERATOR, and the variable d.c. voltage V_{contr} is connected to the non-inverting input, so that square wave *D* is produced.

Bistable multivibrator, gates U_{1c} and U_{1d} in the 20 kHz PULSE GENERATOR, is driven through D_4 D_6 by the sawtooth voltage across C_1, this voltage being caused by periodic charging and discharging of the capacitor; discharging of C_1 via D_3 R_3 is effected by saturation of gate II. The pulse generator does not function while its inhibiting input is LOW (C_1 held discharged); this input is connected to the square-wave generator output. Compare waveforms *D* and *E* The pulse generator drives PULSE AMPLIFIER U_2. The duration of the trigger pulse bursts, waveform *F*, increases with V_{contr} and so does the rectifier output.

Sync pulses *B* drive the non-inverting input of U_4 via R_{12}. In this way, square-wave output *D* goes LOW *before* the mains voltage crosses zero, the triac is not triggered into a new half cycle and loss of control does not occur.

Between pulse bursts, U_2 output would be LOW if it were not for D_7 connecting U_2 input pin 16 to the LOW output of U_4 pin 6. As a result, U_4-output transistor is cut off and excessive collector current cannot flow.

The trigger pulse repetition rate depends on $R_7 \times C_1$, and the trigger pulse duration is largely determined by $R_3 \times C_1$. The circuit shown produces 20 kHz pulses with a duration of 10 μs.

9.4.3 THREE-PHASE CONTROLLER[20])

As seen from Fig. 9-54, the three-phase controller consists of a phase shift section for power control, a logic section to obtain the correct mode of triac triggering, and a trigger section to turn on triacs $TH(R)$, $TH(Y)$ and $TH(B)$, which are connected in the phase leads. The waveforms at the top of the diagram clarify circuit operation. The Schmitt triggers (not shown) in the phase shift units are controlled by the sawtooth inputs[21]). The outputs, pins 13, are HIGH during the periods that the Schmitt triggers are tripped on. The instant of trip-on, that is, the triac trigger angle ϑ, is related to the control signal V_{contr}. A higher control signal decreases ϑ, thus increasing the power in the load Triggering can be advanced to $-30°$, so that at full output power interference will be low.

Figs 9-55 and 9-56 are wiring diagrams of the controller.

[20]) AI467: Continuous Three-phase Control System for Triacs; ordering code 9399 254 46701.
[21]) Application Book: Thyristor and Triac Power Control using 61-series Modules, Chapter 1; ordering code 9399 266 02601.

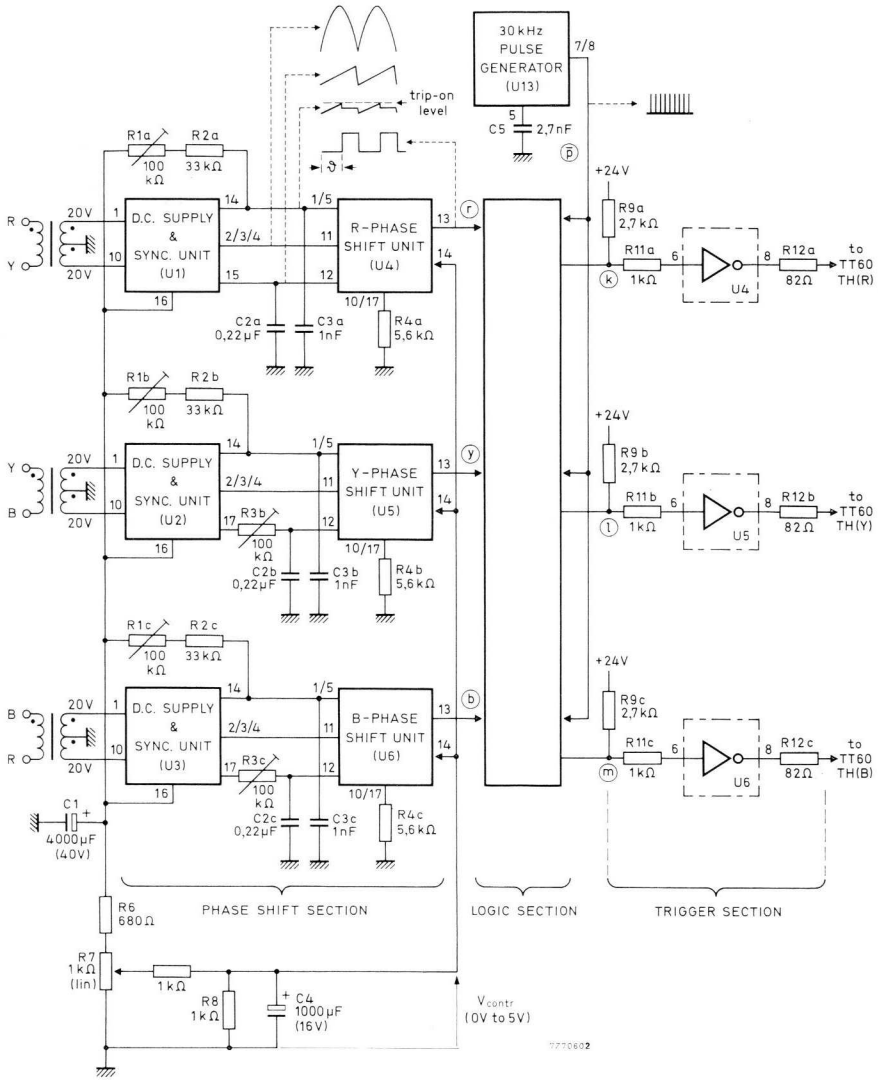


Fig.9-54 Basic diagram of three-phase controller; ϑ = trigger angle.

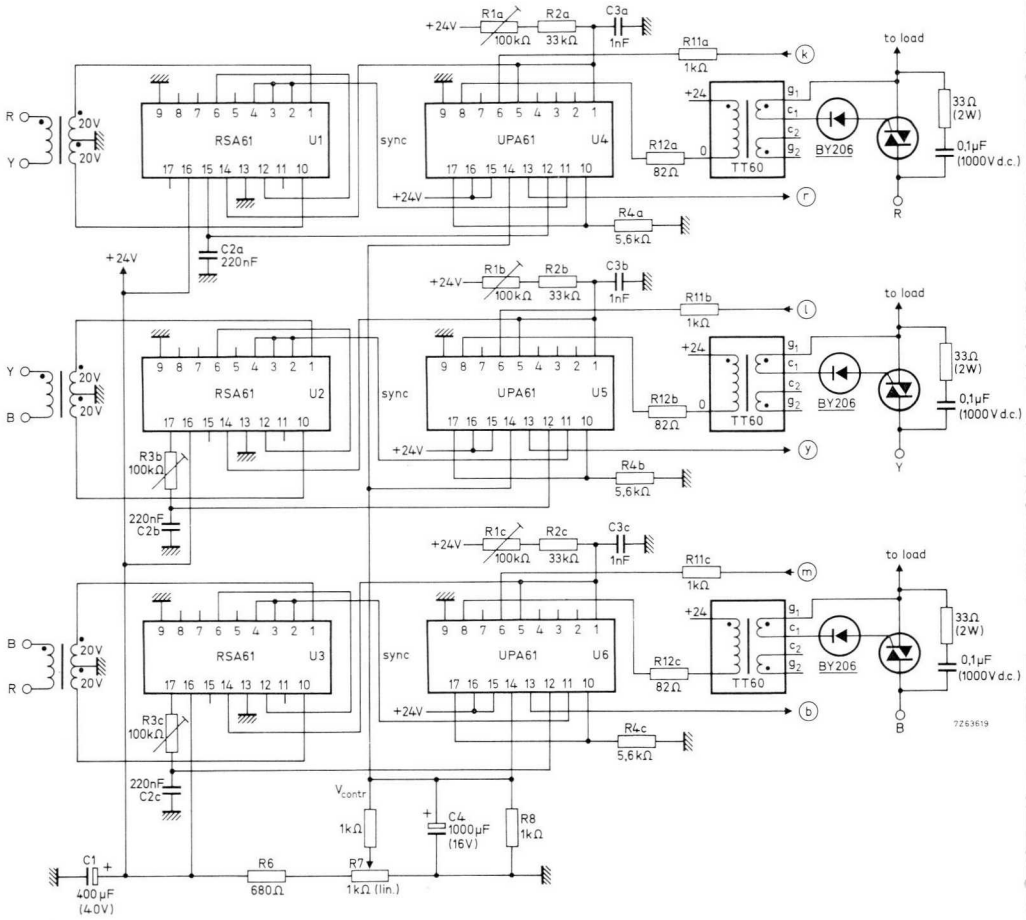


Fig.9-55 Wiring diagram of phase shift, trigger and power section.

Adjustment (Fig. 9-55):

1. *Check that the phase sequence is R-Y-B.*
2. *Set all potentiometers to their mid-position.*
3. *With R_7 adjust V_{cront} to the threshold value at which control must start (for example, 0,2 V).*
4. *Adjust R_{1a} so that the pulses at pin 13 of U_4 are about 0,2 ms wide.*
5. *Increase V_{contr} until the duration of the pulses at pin 13 of U_4 is about 8 ms.*
6. *Adjust R_{1b} R_{1c} so that the pulses at pin 13 of U_5 U_6 have the same duration.*
7. *Reduce V_{contr} so that the pulses at pin 13 of U_4 are again about 0,2 ms wide.*
8. *Adjust R_{3b} R_{3c} so that the pulses at pin 13 of U_5 U_6 have the same duration.*

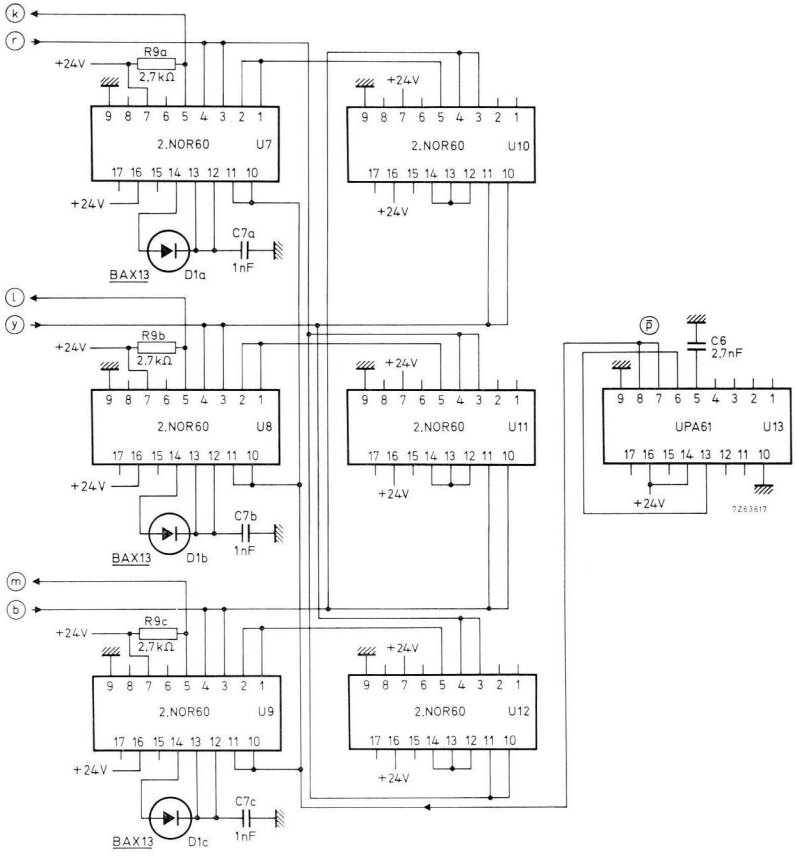


Fig.9-56 Wiring diagram of logic section (U_7 to U_{12}) and 30 kHz trigger pulse generator (U_{13}).

9.4.4 2 kVA TRACTION BATTERY CHARGER

Intended to charge traction batteries this system provides rapid charging to minimize vehicle down time, without the risk of overloading the battery. Charging is a three-period program[22]) comprising:

1. Initial (rapid) charging with high current I_{HIGH}
2. Charging with constant voltage V
3. Final charging with low current I_{LOW}.

Change-over from period to period occurs automatically (by monitoring voltage and current), and a clock is built-in to disconnect the battery once charging is completed, thus preventing over-charging.

As shown in the block diagram, Fig. 9-57, the system is built up as follows: (*a*) regulator controlling output voltage V and the high and low levels, I_{HIGH} and I_{LOW}, of output current, (*b*) three-phase controller as described in the previous Section, (*c*) mains-supplied, triac-controlled step-down transformer, (*d*) three-phase diode bridge. In the power circuit, Fig. 9-58, the RC components across the transformer secondary suppress phase-control transients. The secondary is tapped to provide a wide output voltage range. The voltage and current measuring circuits[23]) provide isolation between charger output and regulator input.

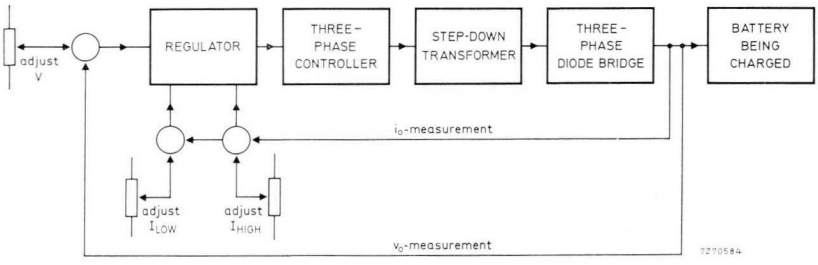


Fig.9-57 Battery charger block diagram.

[22]) VDE 0510/8.70 — Bestimmungen für Akkumulatoren und Akkumulatoren-Anlagen, § 16.

[23]) AN No. 136: D.C. Voltage Transformer; ordering code 9399 260 63601.
AN No. 133: D.C. Current Transformer; ordering code 9399 260 63301.

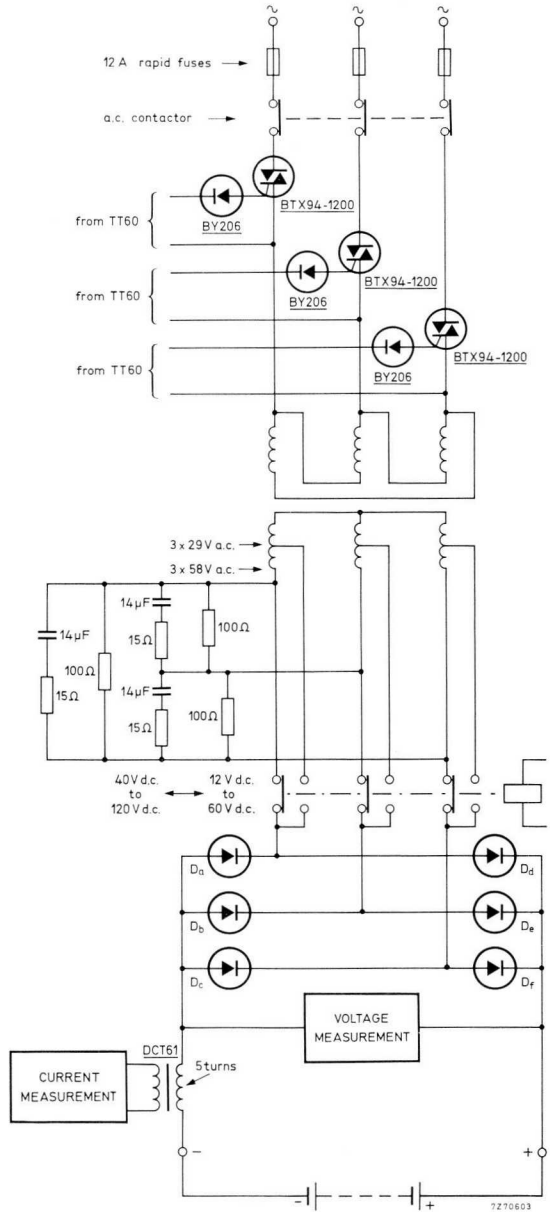


Fig.9-58 Power circuit of automatic battery charger.

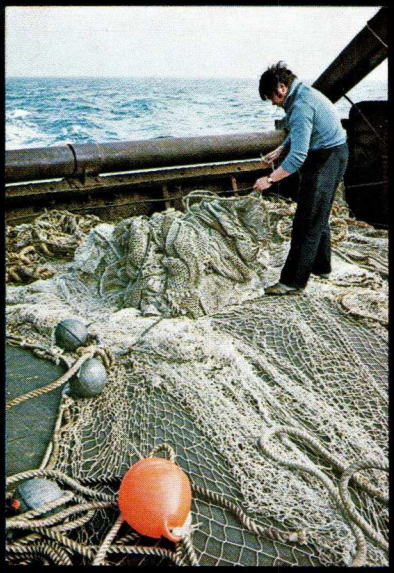
$D_aD_bD_c$ = BYX25-600R on common 56293 heatsink extrusion, 5 cm long

$D_dD_eD_f$ = BYX25-600 on common 56293 heatsink extrusion, 5 cm long.

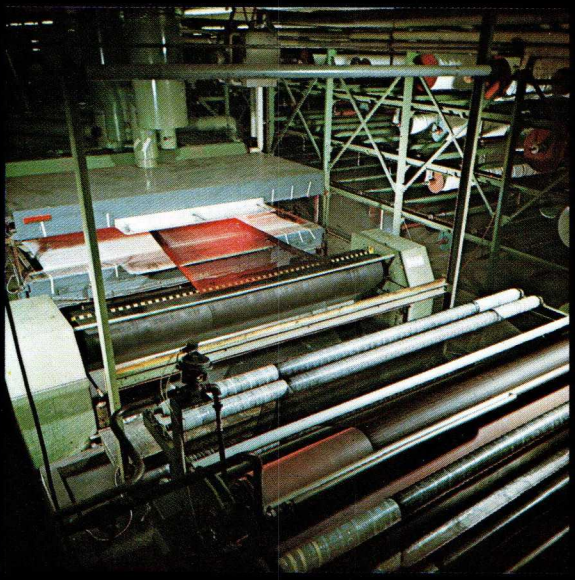
The regulator, Fig. 9-59, contains three DOA61 op amps, A_1, A_2 and A_3, to control the levels of I_{LOW}, I_{HIGH} and V. Diodes D_1 D_2 constitute a "LOWER THAN" gate passing the lower of the op amp output voltages v_{IH} and v_V to control emitter follower TR_1. In the "HIGHER THAN" gate D_4 D_6, TR_1 output is compared with output v_{IL} of A_1 and the higher of the two signals passed, ultimately controlling TR_2. Regulator output V_{contr} is connected to the three-phase controller — Fig. 9-54 in the previous Section.

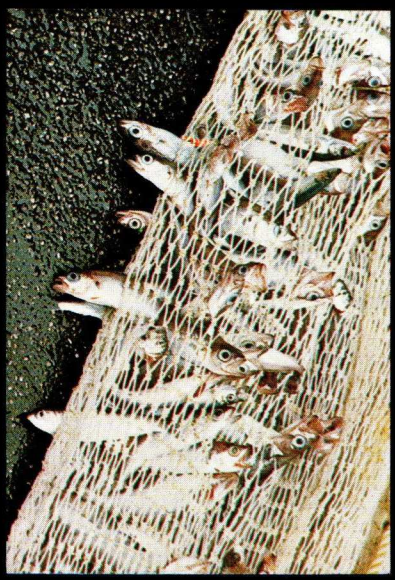
Fig. 9-60 represents the charging process pictorially. The upper graph shows the charger output voltage v_o and current i_o as a function of time. The lower graph gives op amp outputs v_{IL}, v_{IH} and v_V. Change-over to period 2 occurs when v_V falls below v_{IH} (controlled by "LOWER THAN" gate), and change-over to period 3 occurs when v_{IL} rises above v_V (controlled by "HIGHER THAN" gate).

The built-in clock controls the duration of period 3. Its control circuit is according to Fig. 9-61. As soon as v_{IL} exceeds v_V (start of period 3), the DOA61 output becomes negative, and the control gate output switches to HIGH level; the trigger pulse source then oscillates, so triggering the BTW43, which energizes the clock. After the preset time, the clock contact opens and disconnects the charger.



Replacing laborious handwork with modern, triac-controlled fishing net manufacturing machinery paves the way to net profits.





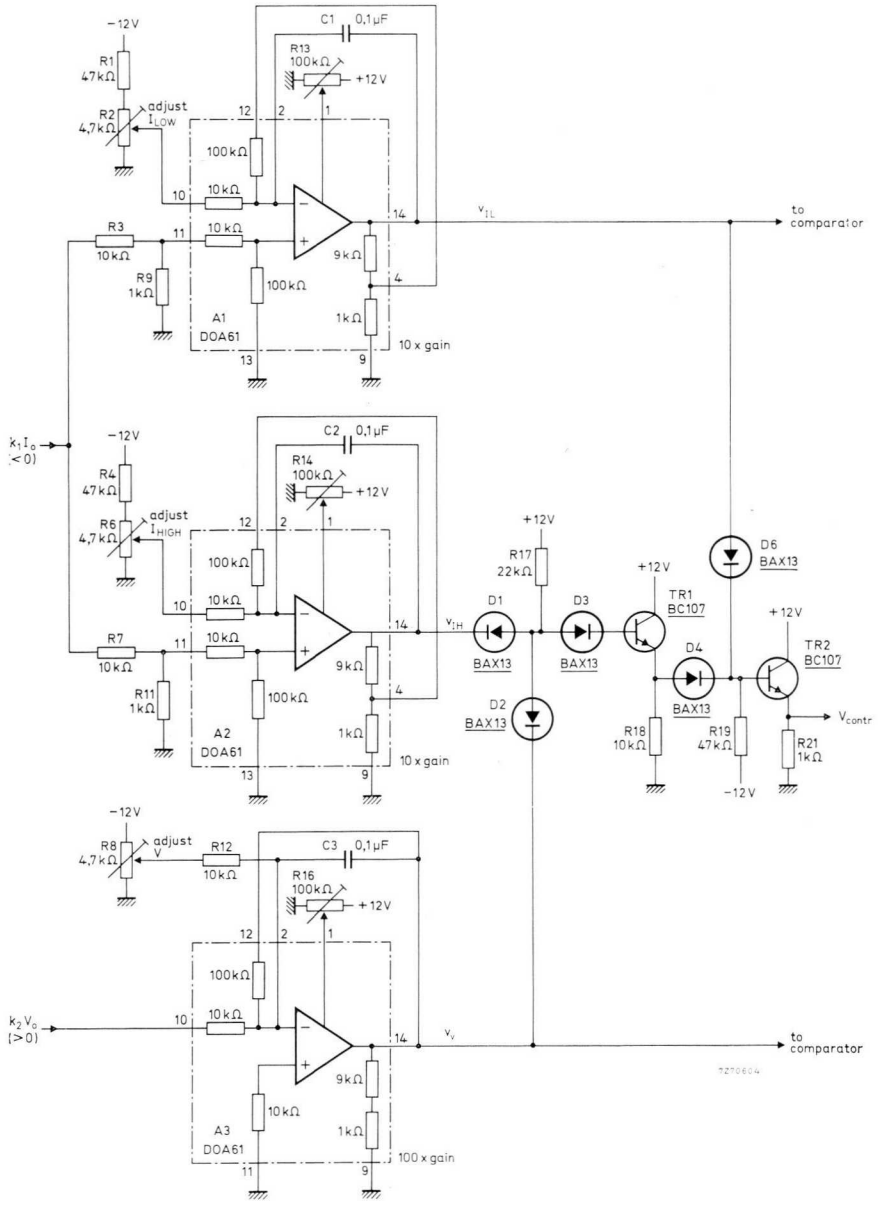


Fig.9-59 Regulator circuit; +12 V and −12 V supplies are stabilized. Modules required: 3 × DOA61.

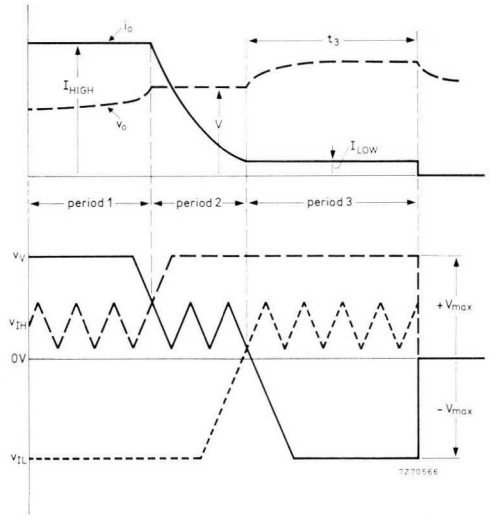


Fig.9-60 Curves illustrating regulator performance.

Adjustment (Figs 5-59 and 5-61):

1. *Set R_2 R_6 R_8 to minimum resistance.*
2. *With the charger unloaded, adjust zero offset potentiometers R_{13} R_{14} R_{16} to make A_1 A_2 A_3 outputs zero.*
3. *Adjust zero offset potentiometer R_{31} to make comparator output zero.*
4. *Set R_6 to about one tenth of its maximum resistance position; note that A_2 output goes maximum positive.*
5. *With A_3 now exerting control, adjust R_8 until charger output voltage has the required value (e.g. 2,45 V/cell for lead-acid batteries, 1,60 V/cell for nickel-cadmium batteries, 1,75 V/cell for nickel-iron batteries*).*
6. *Set R_6 to minimum resistance and check that all op amp outputs are now zero and charger produces no output.*
7. *Connect battery to charger. ENSURE CORRECT POLARITY.*
8. *Set R_2 to obtain low charge current I_{LOW}, e.g. current conforming to 50-hours discharge time*).*
9. *Set R_6 to obtain high charge current I_{HIGH}, e.g. conforming to 5-hours discharge time*).*
10. *Adjust clock to the required duration of the third charging period (three to six hours*).*

*) Consult battery manufacturer's instructions.

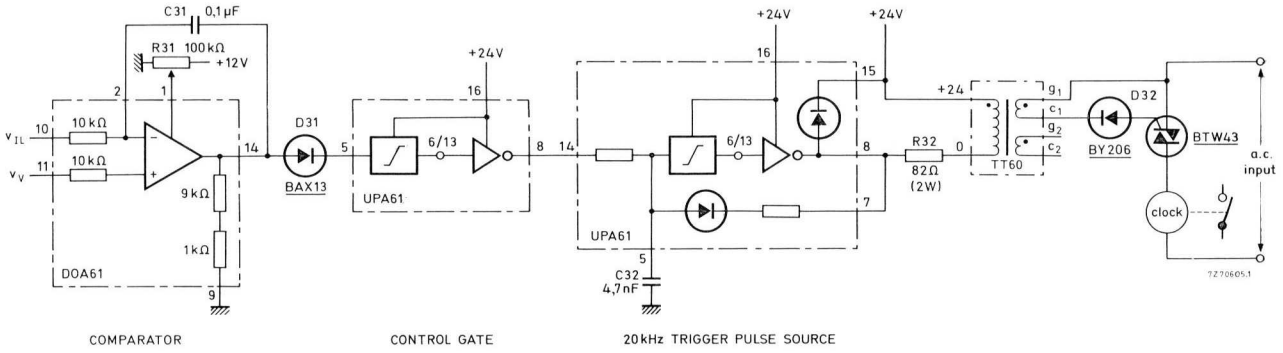


Fig.9-61 Clock control circuit. Modules required: 1 × DOA61, 2 × UPA61.

Brief triac data

The Table below shows the main specifications of our triacs, thus giving an overall impression of their performance. To select the triac best suited to a particular application, our Data Handbook System, Semiconductors and Integrated Circuits, must be consulted.

brief triac data

triac type → description ↓	BTW43	BTX94	BTW34	
max. crest working off-state voltage[a])	400 to 800	400 to 1200	600 to 1200	V
max. repetitive peak off-state voltage[a])	600 to 1200	400 to 1200	600 to 1600	V
min. breakover voltage at max. rated junction temperature[b])	—	500 to 1300	700 to 1600	V
max. r.m.s. on-state current[a]) at 360° conduction angle for:				
$T_{mb} \leqslant 75$ °C	15	—	55	A
$T_{mb} \leqslant 85$ °C	12	25	45	A
max. rate of rise of on-state current after triggering through gate[a])	50	50	50	A/μs
max. non-repetitive peak on-state current, semi-sinusoidal waveform lasting 10 ms, for device having max. rated junction temperature before surge current[a])	100	250	400	A
max. I^2t content of semi-sinusoidal current lasting 10 ms for device having max. rated junction temperature before current surge[a])	50	312	800	A^2s
max. junction temperature[a])	125	125	125	°C
max. rate of rise of off-state voltage that will not trigger any device at rated max. junction temperature[b])	50	100	200	V/μs
max. rate of rise of commutating voltage that will not trigger any device at rated max. junction temperature[b])	10	30	30	V/μs

[a]) rating
[b]) characteristic

Index

Reference is made to page numbers, **bold** type faces indicating the pages containing the main information. Consult the Table of Contents at the beginning of the book for entries not tabulated.

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