ZCU670 Evaluation Board User Guide

UG1532 (v1.0) March 30, 2022

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Chapter 1

Introduction

Overview

The ZCU670 is an evaluation board featuring the ZU67DR Zynq® UltraScale+™ RFSoC DFE device. This board enables the evaluation of applications requiring multi-band (sub-7 GHz, mmWave), multi-std (5G, LTE, etc.), and multi-mode (TDD, FDD) radios, including Milcom and Satcom applications. The ZCU670 board is equipped with all the common board-level features needed for design development, such as DDR4 memory, networking interfaces, an FMC+ expansion port, as well as access to the RFMC 2.0 interface.

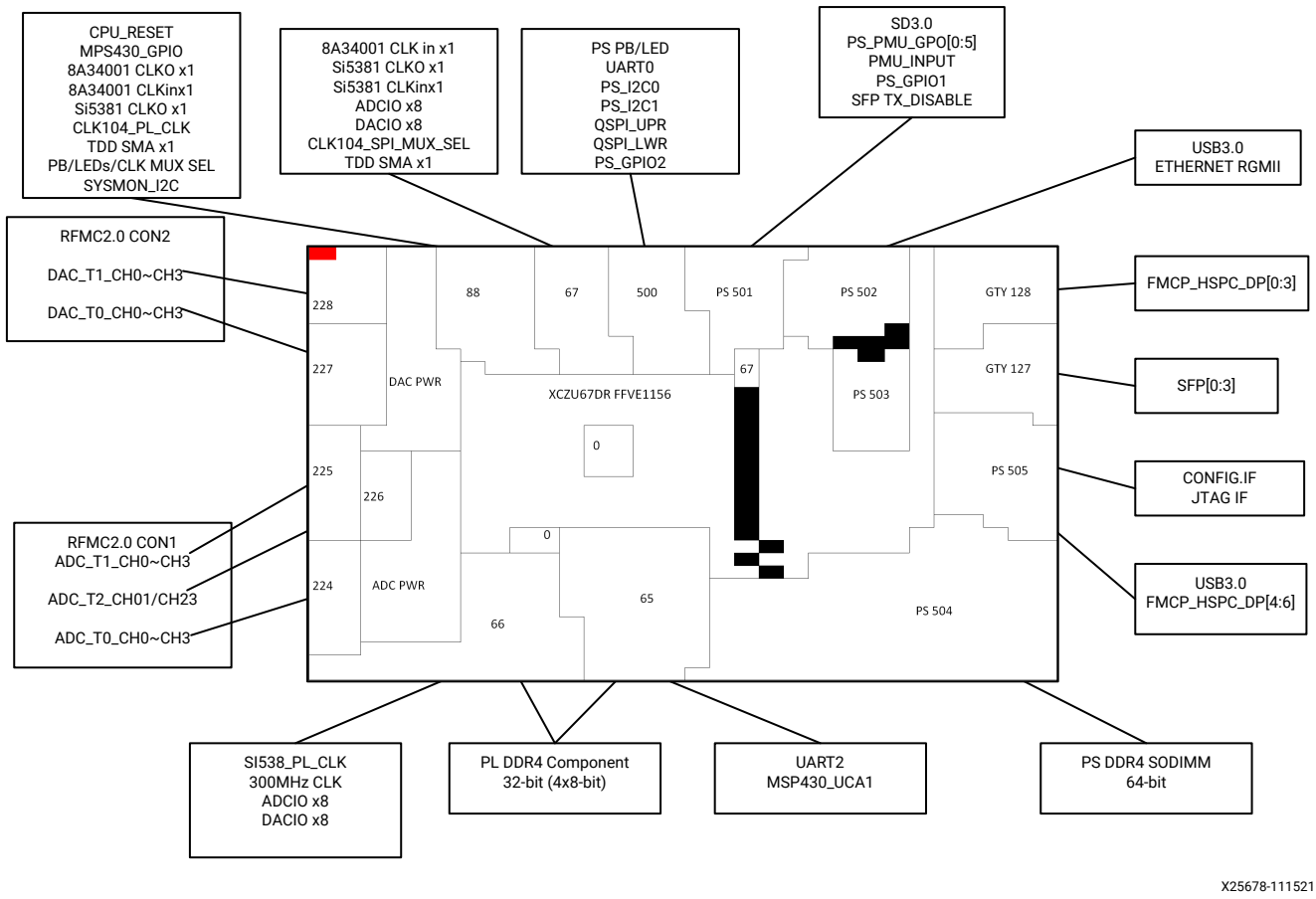
Additional Resources

See Appendix E: Additional Resources and Legal Notices for references to documents, files, and resources relevant to the ZCU670 evaluation board.

Block Diagram

A block diagram of the ZCU670 evaluation board is shown in the following figure.

Figure 1: **Evaluation Board Block Diagram**



Board Features

The ZCU670 evaluation board features are listed here. Detailed information for each feature is provided in Chapter 3: Board Component Descriptions.

- ZU67DR-2, FSVE1156 package
- Form factor: see Board Specifications
- Configuration from:
  - Dual QSPI

    - Micro-SD card
    - USB-to-JTAG bridge
    - PC4 2x7 2 mm JTAG pod flat cable header
- Clocks
    - SI5381 (various frequencies)

      For additional details on this clock, see Table 17, Table 18, and SI5381A 10 Independent Output Any-Frequency Clock Generator U43.
    - CLK104 (various frequencies):

      Optional for DFE. Contact factory for availability.
      - CLK104_PL_CLK
      - CLK104_PL_SYSREF
      - CLK104_AMS_SYSREF
      - CLK104_DAC_REFCLK (direct connect SSMP)
    - 8A34001 IEEE 1588, Synchronous Ethernet (SyncE), and eCPRI clock (various frequencies)

      For additional details on this clock, see Table 17, Table 18, and SI5381A 10 Independent Output Any-Frequency Clock Generator U43.
    - PS_REF_CLK 33.333333...(33 + 1/3 MHz)
    - ADC_CLK_226 (direct connect SSMP)

      For additional details on this clock, see Table 17, Table 18, and Programmable User SI570 Clocks.
    - DAC_CLK_228 (direct connect SSMP)
    - USER_MGT_SI570 (default 156.25 MHz)

      For additional details on this clock, see Table 17, Table 18, and Programmable User SI570 Clocks.
    - USER_SI570_C0 (default 300 MHz)

      For additional details on this clock, see Table 17, Table 18, and Programmable User SI570 Clocks.
    - User SMA clocks

      For more information, see User SMA Clocks.
- PS DDR4 4 GB 64-bit SODIMM
- PL DDR4 C0 I/F 2 GB 32-bit component (4x8-bit)

- PS GTR (bank 505) assignment
  - USB3 (1 GTR)
  - FMCP HSPC DP (3 GTR)
- PL GTY assignment (2 quads, 8 total GTY)
  - 2x2 zSFP+ (4 GTY on bank GTY127)
  - FMCP HSPC DP (4 GTY, bank GTY128)
- PS MIO connectivity
  - PS MIO[0:5, 7:12]: dual QSPI
  - PS MIO[13]: PS_GPIO2
  - PS MIO[14:17]: 2 channels of I2C
  - PS MIO[18:19]: UART0 (1 of 3 FT4232 UART channels)
  - PS MIO[22:23]: PS_PB, PS_LED I/F
  - PS MIO[26]: PMU_INPUT
  - PS MIO[27:30]: SFP[0:3] TX_DISABLE
  - PS MIO[32:37]: PMU_GPO[0:5]
  - PS MIO[38]: PS_GPIO1
  - PS MIO[39:43, 45:51]: SD I/F
  - PS MIO[52:63]: USB3.0
  - PS MIO[64:77]: Ethernet RGMII
- PL I/O connections
  - PL user GPIO pushbutton
  - PL CPU reset pushbutton
  - PL user GPIO LEDs (4)
- Security—PSBATT button battery backup
- SYSMON header
- Operational switches (power on/off, PS_PROG_B, boot mode DIP switch)
- Operational status LEDs (INIT, DONE, PS STATUS, PGOOD)
- Power management
- System controller (MSP430)

The ZCU670 provides a rapid prototyping platform that uses the XCZU67DR-2FSVE1156I device. The ZU67DR contains many useful processor system (PS) hard block peripherals exposed through the multi-use I/O (MIO) interface and a variety of FPGA programmable logic. The following table lists a brief summary of the resources available within the ZU67DR.

Feature set overview, description, and ordering information is provided in the *Zynq UltraScale+ RFSoC DFE Data Sheet: Overview* (DS883).

Table 1: **Zynq UltraScale+ RFSoC ZU67DR Features and Resources**

Feature	Resource Count
Digital front end	Included
14-bit 2.95 GSPS RF-ADC with DDC	8
14-bit 5.9 GSPS ADC RF-DAC with DDC	2
14-bit 10 GSPS RF-DAC with DUC	8
APU: Quad-core Arm® Cortex®-A53 MPCore with CoreSight™	1
RTPU: Dual-core Arm Cortex-R5F MPCore with CoreSight	1
HD I/O	96
HP I/O	312
MIO banks	3 banks, total of 78 pins
PS GTR 6 Gb/s transceivers	4 PS-GTRs
PL GTY 28 Gb/s transceivers	8 GTYs
System logic cells	489,300
CLB flip-flops	447,360
CLB LUTs	223,680
Maximum distributed RAM (Mb)	6.9
Block RAM blocks	648
UltraRAM blocks	160
DSP slices	1,872
100G Ethernet with RS-FEC	1

Board Specifications

Dimensions

Height: 12.225 inches (31.05 cm)

Width: 10.675 inches (27.11 cm)

Thickness: 0.122 inches (0.310 cm)

Note: A 3D model of this board is not available.

See the ZCU670 Evaluation Board website for the XDC listing and board schematics.

Environmental

***Note*:** The operating temperature range is not fully tested across the specified temperature range. It is for general guidelines only. Customers should use the ZCU670 evaluation board for evaluation purposes only in a normal lab environment and should not operate beyond room temperature.

- **Temperature:**

  Operating: 0°C to +45°C

  Storage: –25°C to +60°C

- **Humidity:** 5% to 95% non-condensing

Operating Voltage

+12 V_{DC}

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Chapter 2

Board Setup and Configuration

Standard ESD Measures

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

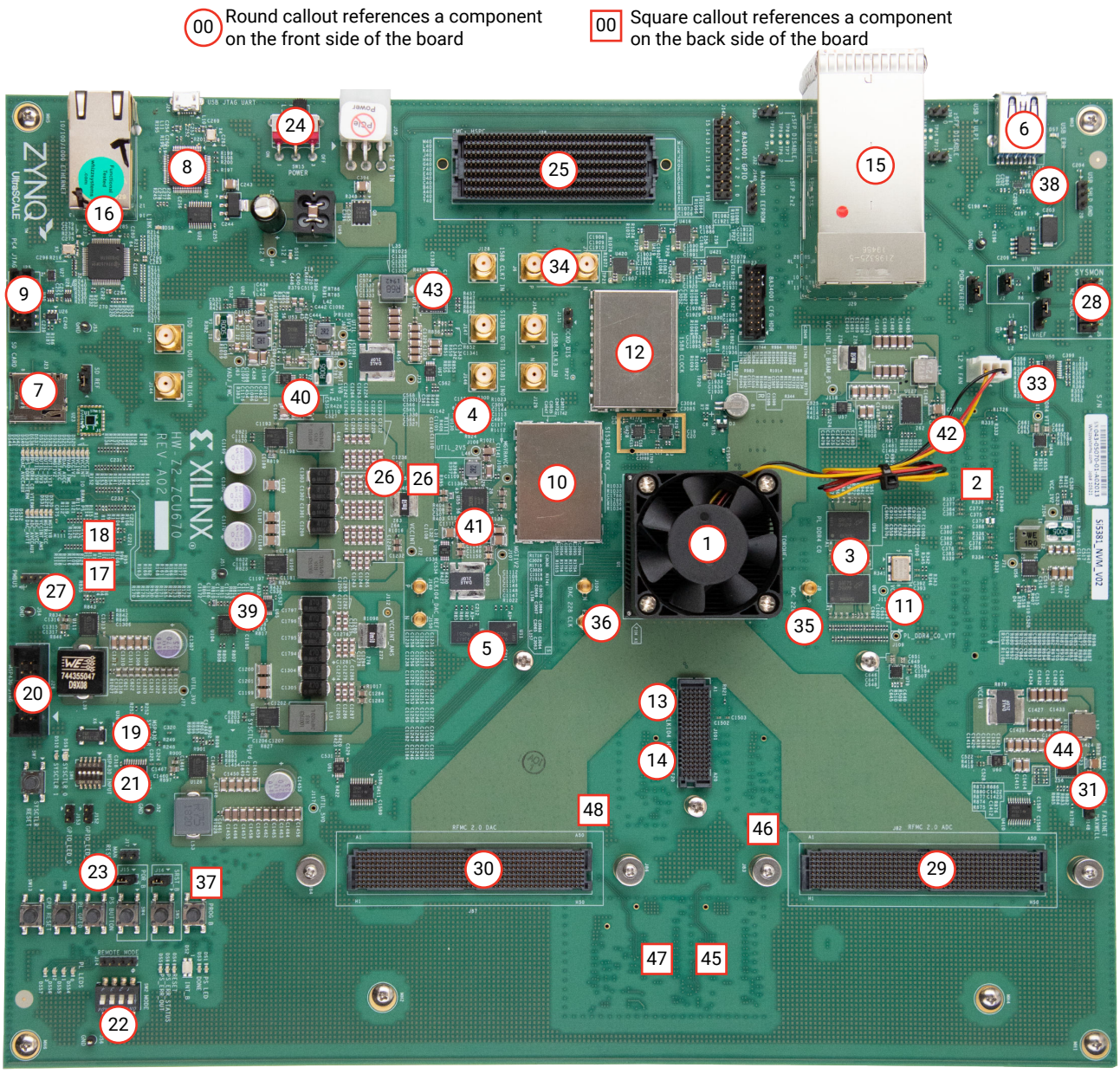
Board Component Location

The following figure shows the ZCU670 board component locations. Each numbered component shown in the figure is keyed to Table 2.

IMPORTANT! *The following figure is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT! *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific ZCU670 version of interest for such details.*

Figure 2: **ZCU670 Component Locations**



Board Component Descriptions

The following table identifies the components and references the respective schematic (038-05023-01) page numbers.

Table 2: **ZCU670 Board Component Locations**

Callout	Ref. Des.	Feature [B]=Bottom	Notes	Schematic Page
1	U1	Zynq® UltraScale+™ RFSoC fansink	XCZU67DR-FFVE115 Ironwood P/N: C19450	
2	J48	DDR4 SODIMM socket with 64-bit DDR4 SODIMM	LOTES ADDR0067-P001A with MICRON MTA4ATF51264HZ-2G6E1 ***Note***: J48 is bottomside.	40
3	U96-U99	DDR4 C0 4x8-bit clamshell component memory (4 GB)	Micron MT40A1G8SA-075 ***Note***: U96 and U97 are bottomside.	65-68
4	U130 (C1)	User PS ref. clock, 33.333333...(33 + 1/3 MHz)	Skyworks (SiLabs) SI570JAC000900DGR	38
5	U11, U12	Dual Quad SPI flash memory (4 Gb total)	Micron MT25QU02GCBB8E12-0SIT	21
6	U6, J18	USB 3 ULPI transceiver [B], USB Micro-AB connector	SMSC USB3320-EZK, WURTH 692122030100	20
7	J23	SD card interface connector	MOLEX 5025700893	24
8	U29, J24	Quad USB_UART, USB micro-B connector	FTDI FT4232Hx-REEL, Hirose ZX62D-AB-5P8(30)	25
9	J25	JTAG 2 mm 2x7 flat-cable connector	Molex 87832-1420	25
10	U43	Fixed frequency clock gen. [B]	Skyworks (SiLabs) SI5381A-E13960-GMR	37
11	U47 (C0)	User Clock, 300 MHz, 3.3V LVDS [B]	Skyworks (SiLabs) 570BAB001614DG	38
12	U48	User MGT Clock, 156.250 MHz, 3.3V LVDS	Skyworks (SiLabs) 570BAB000544DG	38
	U409	Various eCPRI clocks	Renesas 8A34001E-000AJG8	34
13	External	SFP jitter attenuated clock	CLK104 module function (J101)	64
14	J101	CLK104 module connector	Samtec LPAF-20-03.0-L-06-2-K-TR	64
15	J29	Quad zSFP/zSFP+ connector	TE connectivity/AMP 2198325-5	33
16	U33, P1	10/100/1000 MHz Ethernet PHY, RJ45 with magnetics	TI DP83867IRPAP, Wurth 7499111221A	26
17	U17, U15	I2C0 bus switch, expander [B]	TI PCA9544ARGYR, TI TCA6416APWR	22
18	U20, U22	I2C1 bus switches [B]	2 ea. TI TCA9548APWR	23
19	U38	System controller (SC)	TI MSP430F5342	27
20	J24	MSP430 SC emulation cable connector	TYCO 5103308-2	25
21	SW6, SW7	System controller 5-pole DIP switch and reset PB switch	Wurth Electronics, Inc. 416131160805, E-Switch TL3301EP100QG	27
22	SW2	FPGA MODE 4-pole DIP switch	4-pole C&K SDA04H1SBD	10

Table 2: **ZCU670 Board Component Locations** *(cont'd)*

Callout	Ref. Des.	Feature [B]=Bottom	Notes	Schematic Page
23	SW8	User pushbutton switches, active-High	E-switch TL3301EP100QG	42
	SW13	CPU_RESET pushbutton, active-High	E-switch TL3301EP100QG	42
	DS54-DS57	Four single color LEDs, active-High	PL GPIO LEDs, LUMEX SML-LX0603GW-TR	42
	SW1	PS (MIO22) pushbutton	E-switch TL3301EP100QG	9
	SW3	PS_PROG pushbutton	E-switch TL3301EP100QG	10
	SW4, SW5	PS_POR_B, PS_SRST_B pushbuttons	E-switch TL3301EP100QG	10
	J15	2-PIN HDR PS_POR_B	SULLINS PBC02SAAN	10
	J16	2-PIN HDR PS_SRST_B	SULLINS PBC02SAAN	10
	J17	2-PIN HDR MR_B (U5 RST)	SULLINS PBC02SAAN	10
24	SW15	Power ON/OFF slide switch	C&K 1101M2S3AQE2	43
	J50	Power connector	MOLEX 39-30-1060	43
25	J28	FMCP HSPC connector	Samtec ASP_184329_01	28-32
26	-	Power management system (top, [B])	Infineon voltage regulators	47-58
27	J21	PMBUS connector	SULLINS PBC03SAAN	22
28	J5	SYSMON 2X6 vertical male pin header	SULLINS PBC06DAAN	3
29	J82	RFMC 2.0 connector 1	Samtec LPAF-50-03.0-L-08-2-K-TR	61
30	J87	RFMC 2.0 connector 2	Samtec LPAF-50-03.0-L-08-2-K-TR	62
31	J148	2-pin HDR RFSoC selection	SULLINS PBC02SAAN	53
33	U50	Fan controller	Maxim MAX6643LBBAEE++	43
	J57	Fan header (keyed 3-pin)	Molex 22-11-2032	43
34	J6, J7	SMA 8A34001_Q5_OUT_SMA	AMPHENOL 132134-15	35
35	J8, J98	ADC clock connectors	CARLISLE TM14-0084-00	7
36	J99, J100	DAC clock connectors	CARLISLE TM14-0084-00	8
37	U5	PWR-ON reset IC [B]	Maxim MAX16025TE+	10
38	U7	USB3 power switch	Micrel MIC2544A-1YM	20
	J20	USB 3.0 J18 shield header	SULLINS PBC03SAAN	20
	J19	VBUS_SEL option header	SULLINS PBC0S2AAN	20
39	U104	INFINEON PMIC1	Infineon IR35215MTRPBF	44
40	U53	INFINEON PMIC2	Infineon IRPS5401MXI04TRP	47
41	U55	INFINEON PMIC3	Infineon IRPS5401MXI04TRP	49
42	U127	VCCINT PS/block RAM 18A regulator	Infineon IR38164MTRP	50
43	U112	MGTAVCC 4A regulator	Infineon IR38164MTRP	51
44	U123	VCC1V8 8A regulator	Infineon IR38164MTRP	52
45	U115, U116	ADC/DAC AVCC regulators [B]	MPS MPM3683-7	53
46	U114	ADC AVCCAUX 2A regulator [B]	MPS MPM3833C	54
47	U125	DAC AVCCAUX regulator [B]	MPS MPM3833C	55

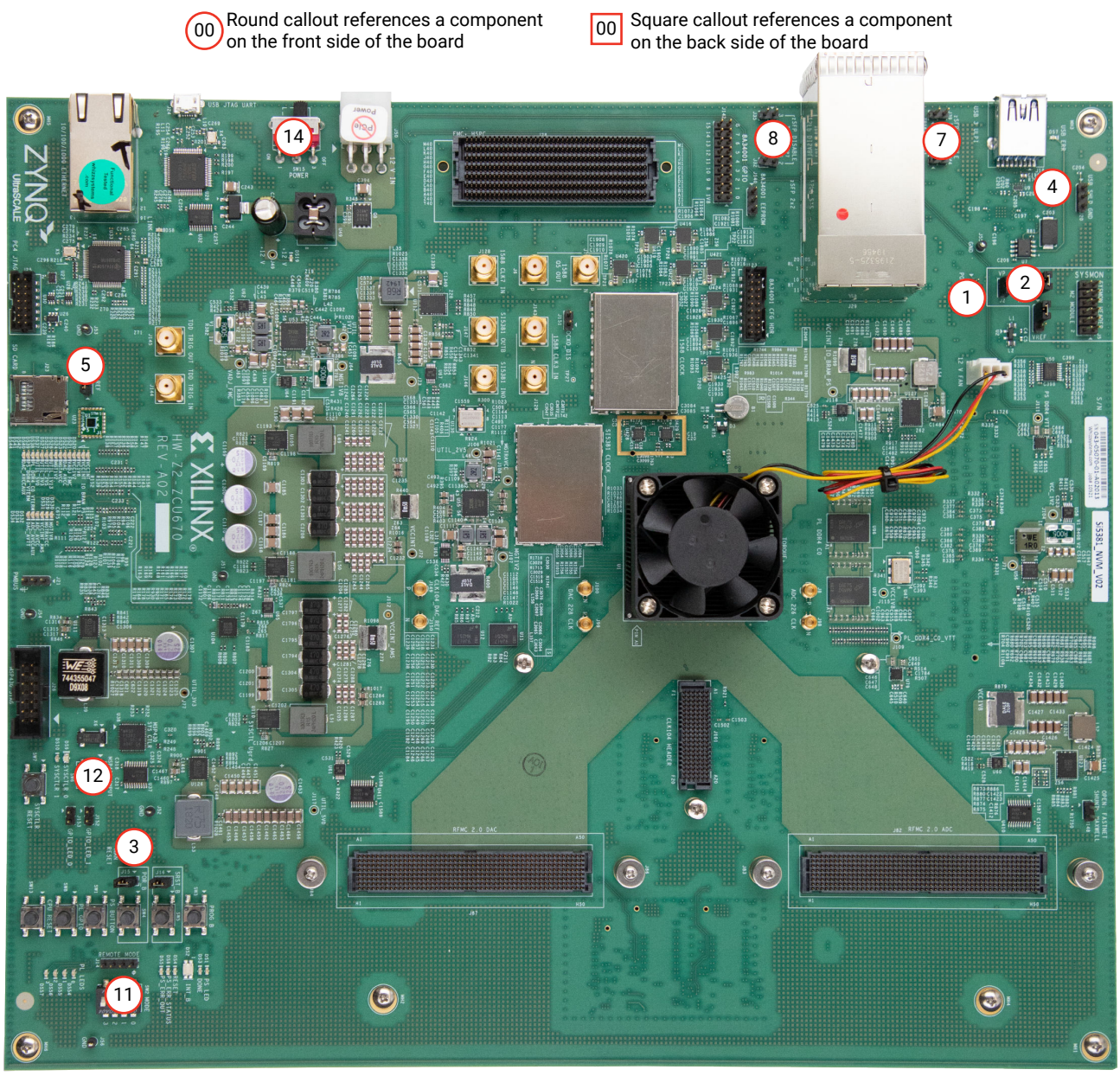
Table 2: **ZCU670 Board Component Locations** *(cont'd)*

Callout	Ref. Des.	Feature [B]=Bottom	Notes	Schematic Page
48	U118	DAC AVTT regulator [B]	MPS MPM3833C	55

Default Jumper and Switch Settings

The following figure shows the ZCU670 board jumper header and switch locations. Each numbered component shown in the figure is keyed to the applicable table in this section. Both tables reference the respective schematic page numbers.

Figure 3: **Board Jumper Header and Switch Locations**



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Jumpers

The following table lists the default jumper settings.

Table 3: **Default Jumper Settings**

Callout	Reference Design	Function	Default	Schematic Page
1	J1	POR_OVERRIDE 1-2: Enable 2-3: Disable	2-3	3
2	J2	SYSMON I2C Address OFF: SYSMON_VP_R floating ON: SYSMON_VP_P pulled down	ON	3
	J3	SYSMON I2C Address OFF: SYSMON_VN_R floating ON: SYSMON_VP_N pulled down	ON	3
	J4	SYSMON VREFP 1-2: 1.25V VREFP connected to fpga 2-3: VREFP connected to GND	1-2	3
3	J15	Reset Sequencer PS_POR_B OFF: Sequencer does not control PS_POR_B ON: Sequencer can control PS_POR_B	ON	10
	J16	Reset Sequencer PS_SRST_B OFF: Sequencer does not control PS_SRST_B ON: Sequencer can control PS_SRST_B	ON	10
	J17	Reset Sequencer inhibit OFF: Sequencer normal operation ON: Sequencer inhibit (resets will stay asserted)	OFF	10
4		ULPI USB3320 U6 ULPIO_VBUS_SEL option jumper	OFF	20
	J19	ON: Selects U17 MIC2544A switch 5V for VBUS		
		OFF: Normal operation, VBUS from J18 USB3.0 conn.		
	J20	USB 3.0 Connector J18 Shield connection options 1-2: J20 shield capacitor C171 to GND 2-3: J20 shield directly to GND	2-3	20
5	J22	SD3.0 U107 IP4856CX25 level-trans. ref. voltage select 1-2: Track SD3.0 J12 socket UTIL_3V3 3.3V 2-3: GND = revert to internal voltage reference	1-2	24

Table 3: **Default Jumper Settings** *(cont'd)*

Callout	Reference Design	Function	Default	Schematic Page
7	J39	zSFP0 J29 LT enable jumper	OFF	33
		ON: zSFP0 TX_DISABLE = GND = enabled		
		OFF: zSFP0 TX_DISABLE = high = disabled		
	J44	zSFP1 J29 LL enable jumper	OFF	33
		ON: zSFP1 TX_DISABLE = GND = enabled		
		OFF: zSFP1 TX_DISABLE = high = disabled		
8	J32	zSFP2 J29 RT enable jumper	OFF	33
		ON: zSFP2 TX_DISABLE = GND = enabled		
		OFF: zSFP2 TX_DISABLE = high = disabled		
	J35	zSFP3 J29 RL enable jumper	OFF	33
		ON: zSFP3 TX_DISABLE = GND = enabled		
		OFF: zSFP3 TX_DISABLE = high = disabled		
31	J148	Voltage selection jumper for Zynq UltraScale+ RFSoC	ON	53
		ON: ADC_AVCC=1.01V for ZU67DR device (DFE)		
		OFF: ADC_AVCC=0.925V for ZU47DR device (Gen3)		

Switches

The following table lists the default switch settings.

Table 4: **Default Switch Settings**

Callout	Reference Design	Function	Default	Schematic Page
11	SW2	RFSoC U1 mode 4-pole DIP switch	0000	10
		Switch OFF = 1 = High; ON = 0 = Low		
		Mode = SW1[4:1] = Mode[3:0]		
		JTAG = ON,ON,ON,ON = 0000		
		QSPI32 = ON,ON,OFF,ON = 0010		
		SD = OFF,OFF,OFF,ON = 1110		
12	SW6	MSP430 U38 5-pole GPIO DIP switch	11111	27
		Switch OFF = 1 = High; ON = 0 = Low		
14	SW15	Main power slide switch	OFF	43

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the ZCU670 board power connector J50. The ATX 6-pin connector has a different pinout than J50. Connecting an ATX 6-pin connector into J50 damages the ZCU670 board and voids the board warranty.*

See Power On/Off Slide Switch for more information.

Zynq UltraScale+ RFSoC XCZU67DR

Zynq UltraScale+ RFSoC ZU67DR uses a multi-stage boot process documented in the Boot and Configuration chapter of the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

Switch SW2 configuration option settings are identified in the following table.

Table 5: **Mode Switch SW2 Configuration Option Settings**

Mode	Mode Pins [3:0]	Mode SW2 [4:1][2]
JTAG	0000	ON,ON,ON,ON
QSPI32	0010[1]	ON,ON,OFF,ON
SD	1110	OFF,OFF,OFF,ON

Notes:
1. Default switch setting.
2. Switch OFF = 1 = High; ON = 0 = Low. See callout 11 in Table 4.

JTAG

Vivado® Design Suite or third-party tools can establish a JTAG connection to the Zynq UltraScale + RFSoC through the FTDI FT4232 USB-to-JTAG/USB UART device (U29) connected to micro-USB connector (J24).

QSPI

Use the following steps to boot from the dual QSPI non-volatile configuration memory.

1. Store a valid Zynq UltraScale+ RFSoC boot image into the QSPI flash devices (U11, U12, MIO[0:12] QSPI interface).
2. Set the boot mode pins SW2 [4:1] as indicated in the table above for QSPI32.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW2 is callout 11 in Figure 3.

SD

Use the following steps to boot from an SD card.

1. Store a valid Zynq UltraScale+ RFSoC boot image file onto an SD card (plugged into SD socket J23) connected to the MIO[39:51] SD interface.
2. Set the boot mode pins SW3 [4:1] as indicated in the table above for SD.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW2 is callout 11 in Figure 3.

See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for more information about Zynq UltraScale+ RFSoC configuration options.

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Chapter 3

Board Component Descriptions

Overview

This chapter provides a description of the board's components and features. Table 2 identifies the components and references the respective schematic page numbers. Component locations are shown in Figure 2.

Component Descriptions

Zynq UltraScale+ RFSoC XCZU67DR

[Figure 2, callout 1]

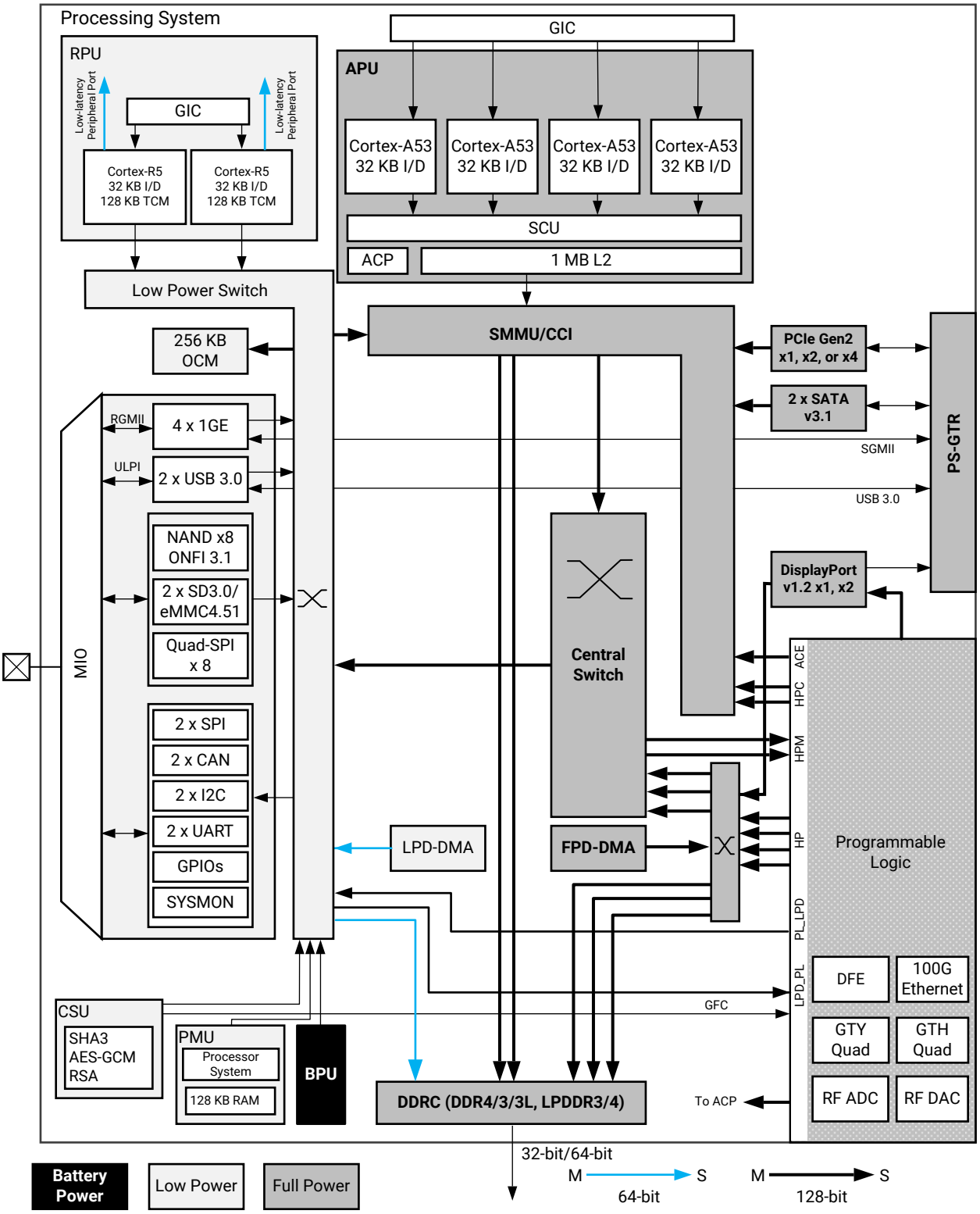
The ZCU670 board is populated with the Zynq® UltraScale+™ RFSoC DFE XCZU67DR-2FSVE1156I, which combines a powerful processing system (PS) and user-programmable logic (PL) in the same device. The processing system in the Zynq UltraScale+ RFSoC features the Arm® flagship Cortex®- A53 64-bit quad-core processor and Cortex-R5F dual-core real-time processor.

The V_{CCINT} supplies are user adjustable through the PMBus with the voltage ranges to support whichever Zynq UltraScale+ RFSoC speed grade is on the evaluation board. See the *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926) for more information.

Top-level Block Diagram

The following figure shows the top-level block diagram for the Zynq UltraScale+ RFSoC.

Figure 4: **Zynq UltraScale+ RFSoC Top-level Block Diagram**



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The Zynq UltraScale+ RFSoC PS block has three major processing units:

- Cortex-A53 application processing unit (APU) Arm v8 architecture-based 64-bit quad-core multiprocessing CPU.
- Cortex-R5F real-time processing unit (RPU) Arm v7 architecture-based 32-bit dual RPU with dedicated tightly-coupled memory (TCM).
- Mali-400 graphics processing unit (GPU) with pixel and geometry processor and 64 KB L2 cache.

The Zynq UltraScale+ RFSoC PS has four high-speed serial I/O (HSSIO) interfaces supporting the following protocols:

- Integrated block for PCI Express® interface-PCIe base specification version 2.1 compliant.
- SATA 3.1 specification compliant interface.
- USB 3.0 interface-compliant to USB 3.0 specification implementing a 5 Gb/s line rate.
- Serial GMII interface-supports a 1 Gb/s SGMII interface.

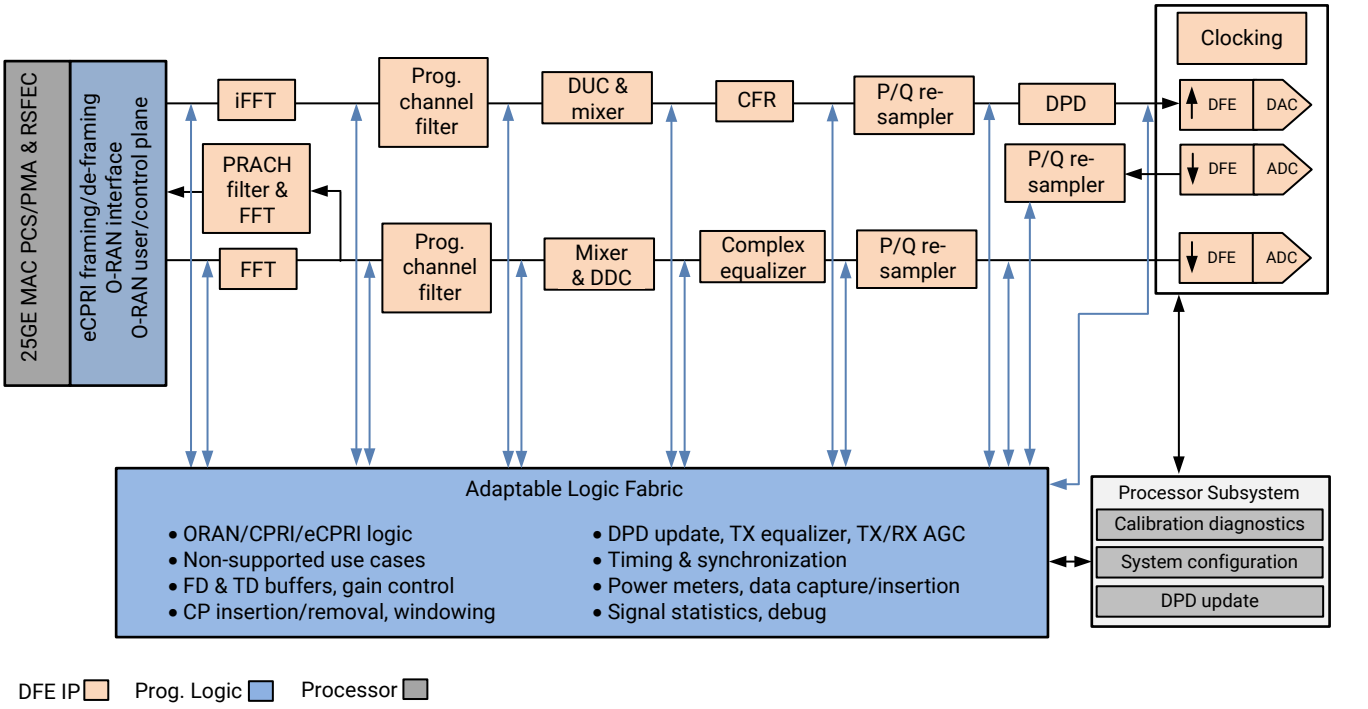
The PS and PL can be coupled with multiple interfaces and other signals to effectively integrate user-created hardware accelerators and other functions in the PL logic that are accessible to the processors. They can also access memory resources in the processing system. The PS I/O peripherals, including the static/flash memory interfaces share a multiplexed I/O (MIO) of up to 78 MIO pins. Zynq UltraScale+ RFSoCs can also use the I/O in the PL domain for many of the PS I/O peripherals. This is done through an extended multiplexed I/O interface (EMIO) and boots at power-up or reset.

The ZCU670 is an evaluation board featuring the ZU67DR Zynq UltraScale+ RFSoC DFE device. This board enables the evaluation of applications requiring multi-band (sub-7 GHz, mmWave), multi-std (5G, LTE, etc.), and multi-mode (TDD, FDD) radios, including Milcom and Satcom applications. The ZCU670 board is equipped with all the common board-level features needed for design development, such as DDR4 memory, networking interfaces, an FMC+ expansion port, as well as access to the RFMC 2.0 interface.

The ZU67DR includes not only the direct RF sampling converters but also a fully dedicated digital front-end (DFE) subsystem with all the required signal processing blocks. With this dedicated IP, the ZCU670 enables ~50% lower power (at 500 MHz) versus equivalent soft IP implementation. The DFE blocks implement the key wireless DFE logic in dedicated blocks and has multiple instances placed within the programmable logic fabric. Each dedicated IP block can be bypassed and appended for maximum flexibility and customization.

The following figure shows the Zynq UltraScale+ RFSoC DFE block diagram.

Figure 5: **Zynq UltraScale+ RFSoC DFE Block Diagram**

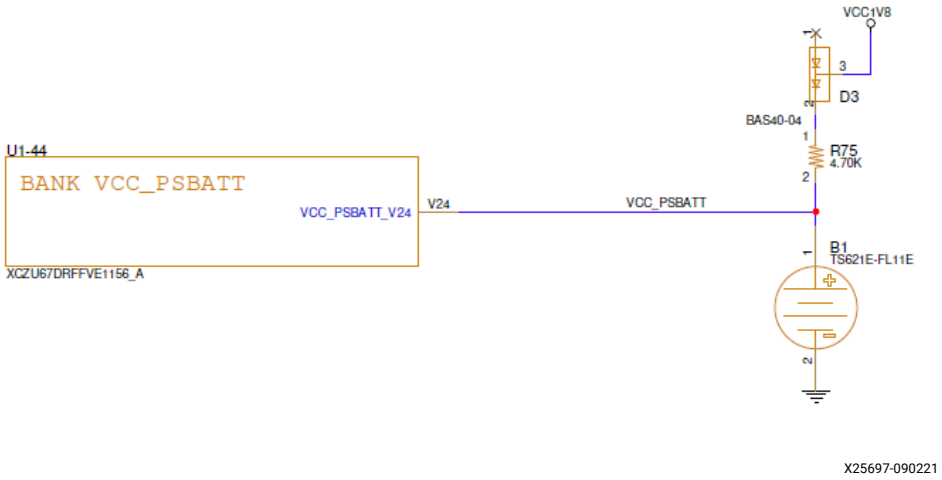


For more information on the Zynq UltraScale+ RFSoC DFE, see the Breakthrough Adaptive Radio Platform website and the *Zynq UltraScale+ RFSoC DFE Data Sheet: Overview* (DS883).

Encryption Key Battery Backup Circuit

The Zynq UltraScale+ RFSoC ZU67DR U1 implements bit stream encryption key technology. The ZCU670 board provides the encryption key backup battery circuit shown in the figure below.

Figure 6: **Encryption Key Battery Backup Circuit**



The Seiko TS621E rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the ZU67DR RFSoC U1 VCC_PSBATT pin AE29. The battery supply current IBATT specification is 150 nA maximum when board power is off. B1 is charged from the VCC1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 ΩK current limit resistor. The nominal charging voltage is 1.42V.

I/O Voltage Rails

The ZU67DR RFSoC PL I/O bank voltages on the ZCU670 board are listed in the following table.

Table 6: **I/O Voltage Rails**

ZU67DR	Power Net Name	Voltage	Connected To
PL Bank 65	VCC1V2	1.2V	PL_DDR4_C0_DQx, MSP430_UCA1, UART2
PL Bank 66	VCC1V2	1.2V	PL_DDR4_C0_Ax, USER_SI570_C0, SI5381_PL_CLK, ADCIO[08:15], DACIO[08:15]
PL Bank 67	VCC1V8	1.8V	ADCIO[00:07], DACIO[0:07], SI5381_CLK2_IN, 8A34001_Q3_OUT, SI5381_CLK_125, CLK104_CLK_SPI_MUX_SEL[0:1]
PL Bank 88	VCC1V8	1.8V	SYSMON_SDA/SCL, CPU_RESET, GPIO_SW_PL, SI5381_CLK104_MUX_SEL, SI53340_MUX_GT_SEL, SI53340_MUX_GTR_SEL, CLK104_PL_CLK, 8A34001_Q2_OUT, MUX_PL_SYSREF, 8A34001_CLK6_IN, GPIO_LED[0:3], MSP430_GPIO[0:3]
PS Bank 500	VCC1V8	1.8V	MIO_LED/PB, UART0, MIO_I2C0/1, PS_GPIO2, QSPI LWR/UPR
PS Bank 501	VCC1V8	1.8V	SDIO I/F, PMU_GPO[0:5], SFP[0:3]_TX_DISABLE, PMU_INPUT
PS Bank 502	VCC1V8	1.8V	ENET I/F, USB (3.0) I/F
PS Bank 503	VCC1V8	1.8V	PS CONFIG I/F, JTAG I/F

Table 6: **I/O Voltage Rails** *(cont'd)*

ZU67DR	Power Net Name	Voltage	Connected To
PS Bank 504	VCC1V2	1.2V	PS_DDR4_SODIMM (64-BIT) I/F

PS DDR4 SODIMM Socket

[Figure 2, callout 2]

The PS-side memory is wired to the Zynq UltraScale+ RFSoC DDRC Bank 504 hard memory controller. A 64-bit single rank DDR4 SODIMM is inserted into socket J48. The ZCU670 is shipped with a DDR4 SODIMM installed:

- Manufacturer: Micron
- Part Number: MTA4ATF51264HZ-2G6E1
- Description:
  - 4 GByte DDR4 260-Pin SODIMM
  - Single Rank (x 16-bit components)
  - 512 Mb x 64-bit
  - 2666 MT/s

The ZCU670 ZU67DR RFSoC (ZU67DR supports 2400MT/s) PS DDR interface performance is documented in the *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926).

The ZCU670 DDR4 SODIMM interface adheres to the constraints guidelines documented in the PCB guidelines for DDR4 section of the *UltraScale Architecture PCB Design User Guide* (UG583). The DDR4 SODIMM interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150).

For additional details, see the Micron MTA4ATF51264HZ-2G6E1 data sheet on the Micron Technology website.

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

PL C0 I/F DDR4 Component Memory

[Figure 2, callout 3]

The 4 GB, 32-bit wide DDR4 memory system is comprised of four 1 Gb x 8 SDRAM (Micron MT40A1G8SA-075), U96-U99. This memory system is connected to PL-side ZU67DR banks 64 and 65. The DDR4 0.6V PL_DDR4_C0_VTT termination voltage is supplied from TPS51200DRCT sink-source regulator U79.

- Manufacturer: Micron
- Part Number: MT40A1G8SA-075
- Description:
  - 8 Gb (1 Gb x 8)
  - 1.2V 78-ball FBGA
  - DDR4-2666

The ZCU670 ZU67DR RFSoC PL DDR interface performance is documented in the *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926).

The ZCU670 board DDR4 32-bit component memory interface adheres to the constraints guidelines documented in the PCB guidelines for DDR4 section of *UltraScale Architecture PCB Design User Guide* (UG583). The ZCU670 DDR4 component interface is a 40Ω impedance implementation. Other memory interface details are also available in the *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150).

For additional details, see the Micron MT40A1G8SA-075 data sheet on the Micron Technology website.

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

PSMIO

The following table provides PS MIO peripheral mapping implemented on the ZCU670 board. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for more information on PS MIO peripheral mapping.

Table 7: **MIO Peripheral Mapping**

MIO[0:25] Bank 500		MIO[26:51] Bank 501		MIO[52:77] Bank 502	
0	QSPI_LWR	26	PMU IN	52	USB0
1	QSPI_LWR	27	MIO27 SFP3_TX_DISABLE_B	53	USB0
2	QSPI_LWR	28	MIO28 SFP2_TX_DISABLE_B	54	USB0
3	QSPI_LWR	29	MIO29 SFP1_TX_DISABLE_B	55	USB0
4	QSPI_LWR	30	MIO30 SFP0_TX_DISABLE_B	56	USB0
5	QSPI_LWR	31	Not assigned/no connect	57	USB0
6	Not assigned/no connect	32	PMU GPO	58	USB0

Table 7: **MIO Peripheral Mapping** *(cont'd)*

MIO[0:25] Bank 500		MIO[26:51] Bank 501		MIO[52:77] Bank 502	
7	QSPI_UPR	33	PMU GPO	59	USB0
8	QSPI_UPR	34	PMU GPO	60	USB0
9	QSPI_UPR	35	PMU GPO	61	USB0
10	QSPI_UPR	36	PMU GPO	62	USB0
11	QSPI_UPR	37	PMU GPO	63	USB0
12	QSPI_UPR	38	GPIO	64	GEM3
13	GPIO	39	SD1	65	GEM3
14	I2C0	40	SD1	66	GEM3
15	I2C0	41	SD1	67	GEM3
16	I2C1	42	SD1	68	GEM3
17	I2C1	43	SD1	69	GEM3
18	UART0	44	Not assigned/no connect	70	GEM3
19	UART0	45	SD1	71	GEM3
20	Not assigned/no connect	46	SD1	72	GEM3
21	Not assigned/no connect	47	SD1	73	GEM3
22	GPIO	48	SD1	74	GEM3
23	GPIO	49	SD1	75	GEM3
24	Not assigned/no connect	50	SD1	76	GEM3
25	Not assigned/no connect	51	SD1	77	GEM3

Quad-SPI Flash Memory (MIO 0–12)

[Figure 2, callout 5]

The Micron dual MT25QU02GCBB8E12-0SIT serial NOR flash Quad-SPI memories are capable of holding the boot image for the Zynq UltraScale+ RFSoC. This interface is used to support QSPI32 boot mode as defined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

The dual Quad-SPI flash memory located at U11/U12 provides 4 Gb of non-volatile storage that can be used for configuration and data storage.

- Part number: MT25QU02GCBB8E12-0SIT (Micron)
- Description:
  - 2 Gb/256 MB
  - 2.7V – 3.6V 24-ball TBGA
  - 90 MHz DTR/133 MHz STR
- Datapath width: 8 bits

- Data rate: Various depending on Single/Dual/Quad mode

The configuration and Quad-SPI section of the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) provides details on using the Quad-SPI flash memory. For more QSPI details, see the Micron MT25QU02GCBB8E12-0SIT data sheet on the Micron Technology website.

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

GPIO (MIO 13, 38)

These two GPIO bits are connected to the U38 MSP430 system controller for general purpose signaling or communications between the Zynq UltraScale+ RFSoC and the MSP430 system controller. These signals are level-shifted by TXS0108E U37. The connections between the U38 system controller and the ZU67DR RFSoC are listed in following table.

Table 8: **System Controller U38 GPIO Connections to ZU67DR U1**

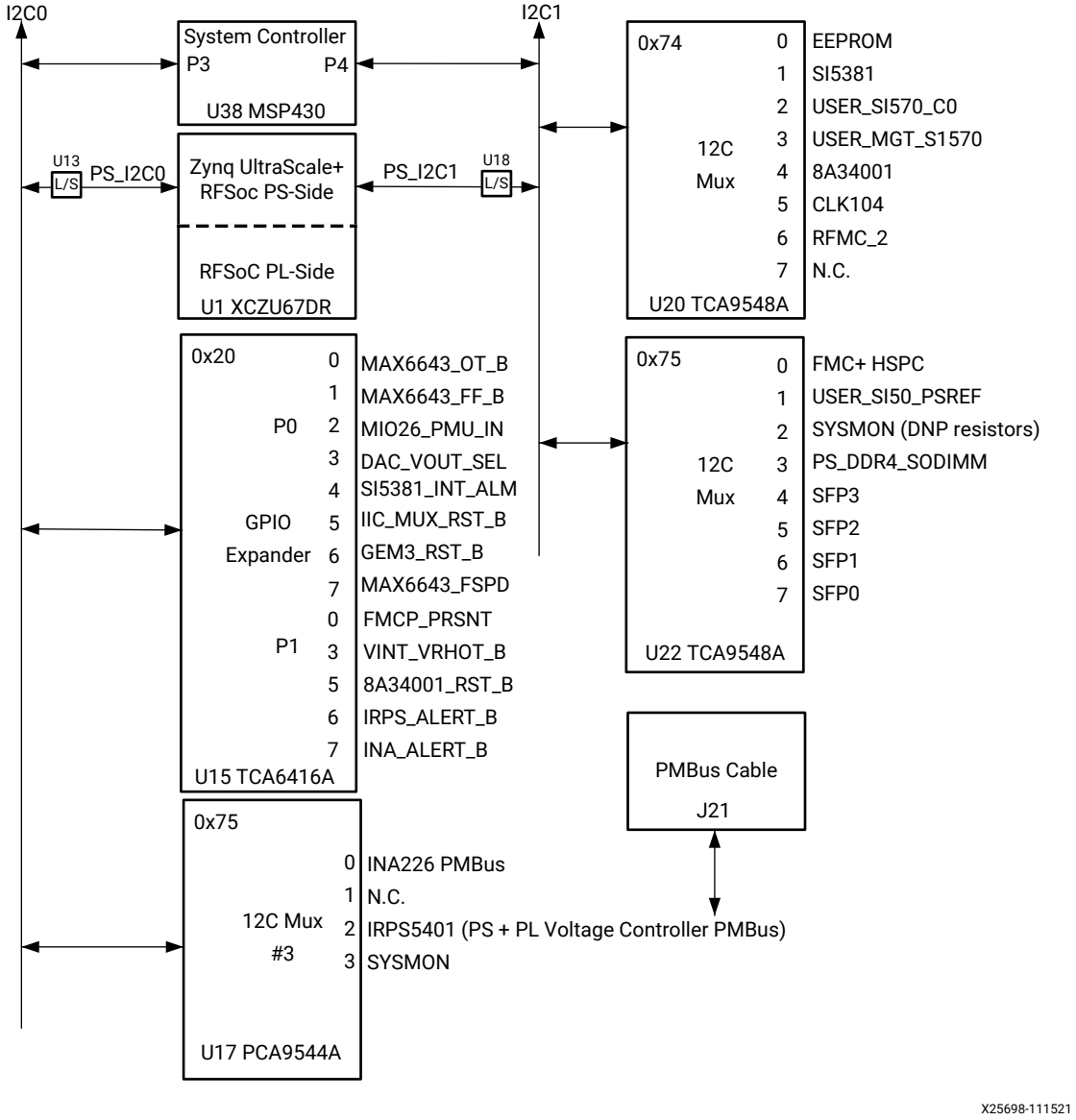
Net Name	MSP430 U38
	Pin Name
MIO38_PS_GPIO1	P1_6
MIO13_PS_GPIO2	P1_7

I2C Bus Topology Overview

I2C0 (MIO 14-15), I2C1 (MIO 16-17)

The following figure shows a high-level view of the I2C0 and I2C1 bus connectivity.

Figure 7: **I2C0 and I2C1 Bus Connectivity Overview**



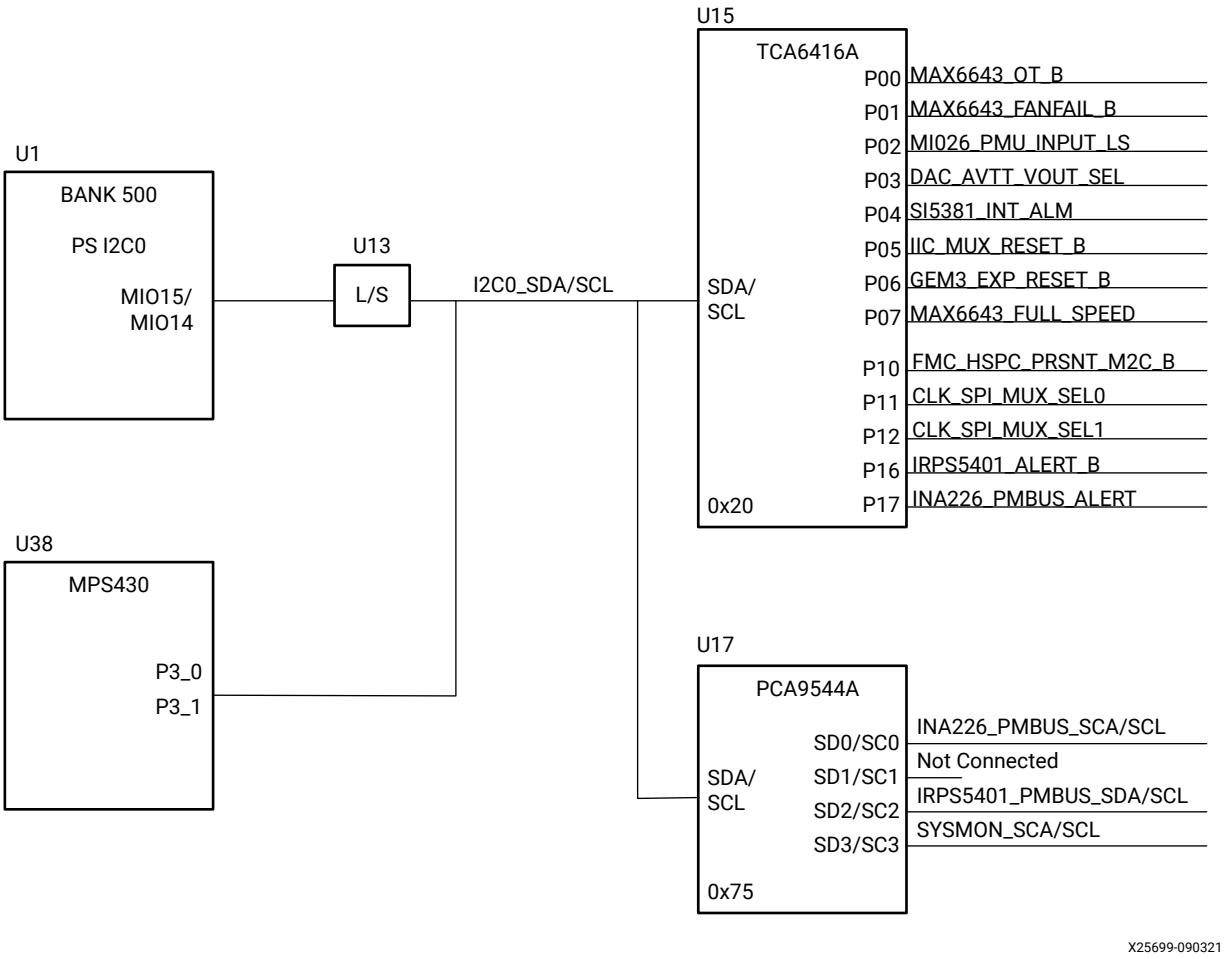
I2C0 (MIO 14-15)

[Figure 2, callout 17]

I2C bus I2C0 connects Zynq UltraScale+ RFSoC U1 PS Bank 500 and the system controller U38 to a GPIO 16-bit port expander (TCA6416A U15) and I2C switch (PCA9544A U17). The port expander enables controlling resets and power system enable pins and accepts various alarm inputs. The I2C0 bus also provides access to the PMBUS power controllers and INA226 power monitors through the U17 PCA9544A switch. TCA6416A U15 is pin-strapped to respond to I2C address `0x20`. The PCA9544A U17 switch is set to `0x75`.

The following figure shows a high-level view of the I2C0 bus connectivity.

Figure 8: **I2C0 Bus Topology**



The following table identifies the devices on each port of the I2C0 U15 TCA6416A port expander.

Table 9: **I2C0 Port Expander TCA6416A U15 Connections**

TCA6416A U15 Pin Name	Schematic Net Name	Connected To		
		Pin Name	Ref. Designator	Device
SDA	I2C0_SDA	Refer to connections shown in the figure above. TCA6416A U15 Addr. 0x20		
SCL	I2C0_SCL			
P00	MAX6643_OT_B	OT_B	U50	MAX6643
P01	MAX6643_FANFAIL_B	FANFAIL_B	U50	MAX6643
P02	MIO26_PMU_INPUT_LS	PS_MIO26	U1	XCZU67DR
P03	DAC_AVTT_VOUT_SEL	G	Q36	NDS331N
P04	SI5381_INT_ALM	INTRB	U43	SI5381A

Table 9: **I2C0 Port Expander TCA6416A U15 Connections** *(cont'd)*

TCA6416A U15 Pin Name	Schematic Net Name	Connected To		
		Pin Name	Ref. Designator	Device
P05	IIC_MUX_RESET_B	RESET_B	U20	TCA9548A
P06	GEN3_EXP_RESET_B	B	U34	SN74LVC1G08
P07	MAX6643_FULL_SPEED	FULLSPD	U50	MAX6643
P10	FMCP_HSPC_PRSNT_M2C_B	PRSNT_M2C_L	J28(H)	ASP_184329_01
		PRSNT_M2C_L	J28(N)	ASP_184329_01
P13	VCCINT_VRHOT_B	VRHOT_ICRIT#	U104	IR35215
P15	8A34001_EXP_RST_B	A	U415	SN74LVC1G08
P16	IRPS5401_ALERT_B	SM_ALERT#	U104	IR35215
		ALERT_B	U53, U55	IRPS5401
		SALERT#	U112, U123, U127	IR38164
P17	INA226_PMBUS_ALERT	ALERT	U57, U58, U59,U60, U61, U62, U63, U64, U65, U67, U71, U75, U77, U124	INA226

The addresses of each target device on the I2C0 U17 PCA9544A switch are identified in the following table.

Table 10: **I2C0 Multiplexer PCA9544A U17 Target Device Addresses**

PCA9544A U17 (Addr 0x75) Port	I2C0 Bus Device	Target Device Address
0	INA226_PMBus (Power Monitors)	0X40-0x43, 0x45-0x4E
1	Not Connected	N/A
2	IRPS5401_PMBus (Voltage Regulators)	0X40, 0x43, 0x44, 0x45, 0x4B, 0x4C
3	SYSMON U1 bank 65	0X32

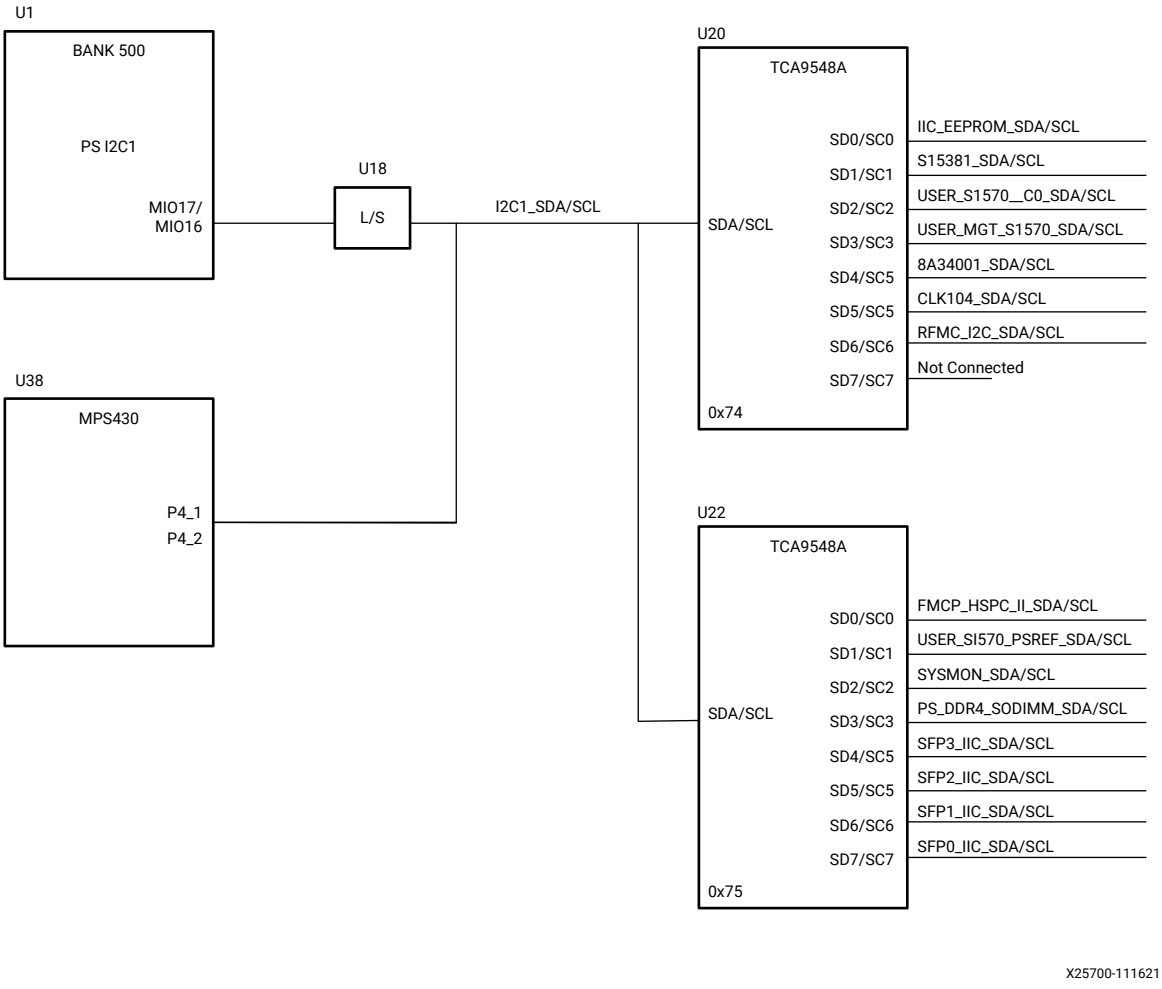
I2C1 (MIO 16-17)

[Figure 2, callout 18]

I2C bus I2C1 connects RFSoC U1 PS Bank 500, PL bank 89, and system controller U38 to two I2C switches (TCA9548A U20 and U22). These I2C1 connections enable I2C communications with various I2C capable target devices. TCA9548A U20 is pin-strapped to respond to I2C address `0x74`. TCA9548A U22 is pin-strapped to respond to I2C address `0x75`.

The following figure shows a high-level view of the I2C1 bus connectivity.

Figure 9: **I2C1 Bus Topology**



The addresses of each target device on the I2C1 U20 and U22 PCA9548A switches are identified in the following tables.

Table 11: **I2C1 TCA9548A U20 Target Device Addresses**

TCA9548A U20 (Addr 0x74) Port	I2C1 Bus Device	Target Device Address
0	EEPROM U16	0X54
1	Si5341 Clock U43	0x76
2	USER SI5381A C0 Clock U47	0X5D
3	USER MGT Si570 Clock U48	0X5D
4	8A34001 (zSFP ClK Recovery) U409	0x5B
5	CLK104 Connector J101	0x2F
6	RFMC LPAF-50 Connector J82	USER
7	No Connection	NA

Table 12: **I2C1 TCA9548A U22 Target Device Addresses**

TCA9548A U22 (Addr 0x75) Port	I2C1 Bus Device	Target Device Address
0	FMCP HSPC J28	0x##
1	USER Si570 C1 Clock U130	0X5D
2	SYSMON U1 BANK 65	0x32
3	PS DDR4 SODIMM SKT. J48	0x51
4	SFP3 P3	0x50
5	SFP2 P2	0x50
6	SFP1 P1	0x50
7	SFP0 P0	0x50

For more information on the TCA9548A, TCA6416A, and PCA9544A, see the Texas Instruments website.

The detailed Zynq UltraScale+ RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

UART0 (MIO 18-19)

[Figure 2, callout 8]

This is the primary Zynq UltraScale+ RFSoC PS-side UART interface and is connected to the FTDI U29 FT4232HL USB-to-Quad-UART Bridge port B through TXS0108E level-shifter U32.

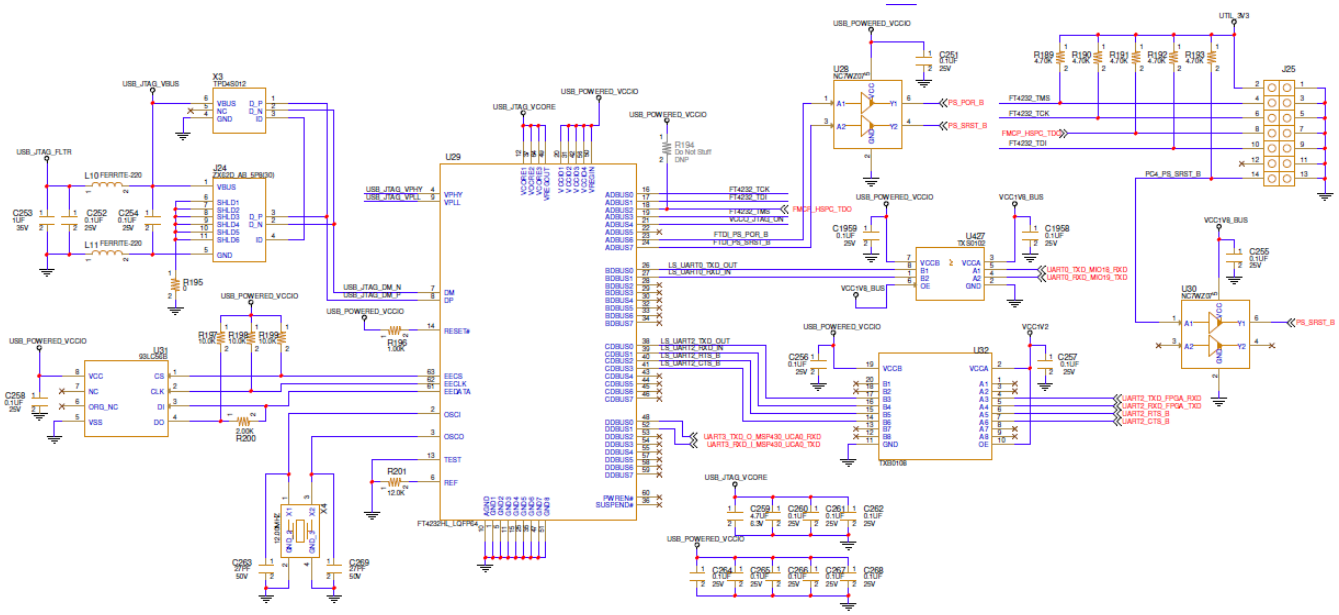
The FT4232HL U29 port assignments are listed in the following table.

Table 13: **FT4232HL Port Assignments**

FT4232HL U29	Zynq UltraScale+ RFSoC U1
Port A JTAG	ZCU670 JTAG Chain
Port B UART0	PS_UART0 (MIO 18-19)
Port C UART2	PL_UART2 Bank 89
Port D UART3	U38 System Controller UART

The FT4232HL interface circuit connectivity is shown in the following figure.

Figure 10: **ZCU670 FT4232HL Connectivity**



For more information on the FT4232HL, see the Future Technology Devices International Ltd. website.

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

GPIO (MIO 22-23)

PS-side pushbutton SW1 is connected to MIO22. PS-side LED DS1, physically placed adjacent to the pushbutton, is connected to MIO23.

PMU GPI (MIO 26)

PS-side MIO 26 is reserved as an input to the PMU for indicating a warm boot. PS bank 501 MIO26 is connected to the I2C0 U15 TCA6416A bus expander (port P02) through level-shifter U27. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for details about the PMU interface.

PMU GPO (MIO 32-37)

The platform management unit (PMU) within the Zynq UltraScale+ RFSoC signals power domain changes using the PMU output pins for deep-sleep mode. The Zynq UltraScale+ RFSoC PMU GPO pins are connected to inputs of the MSP430 system controller through the TXS0108E level-shifter U37. The RFSoC U1 Bank 501 and MSP430 U38 pin numbers are listed in the following table.

Table 14: **XCZU67DR to MSP430 Connections**

Net Name	MSP430 U38
	Pin Name
MIO37_PMU_GPO5	P1_0
MIO36_PMU_GPO4	P1_1
MIO35_PMU_GPO3	P1_2
MIO34_PMU_GPO2	P1_3
MIO33_PMU_GPO1	P1_4
MIO32_PMU_GPO0	P1_5

Through the I2C0 bus U1 PS-side MIO[14:15] pins, the PMU has access to the board power controller PMBus bus (IRPS5401_SDA/SCL) and power monitor PMbus (INA226_PMBUS_SDA/SCL). See Figure 8: I2C0 Bus Topology for additional details.

See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for details about the PMU interface.

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

SDIO (MIO 39-51)

A PS-side interface to an SD card connector is provided for booting and file system storage. This interface is used for the SD boot mode and supports SD3.0 access post boot.

SD Card Interface

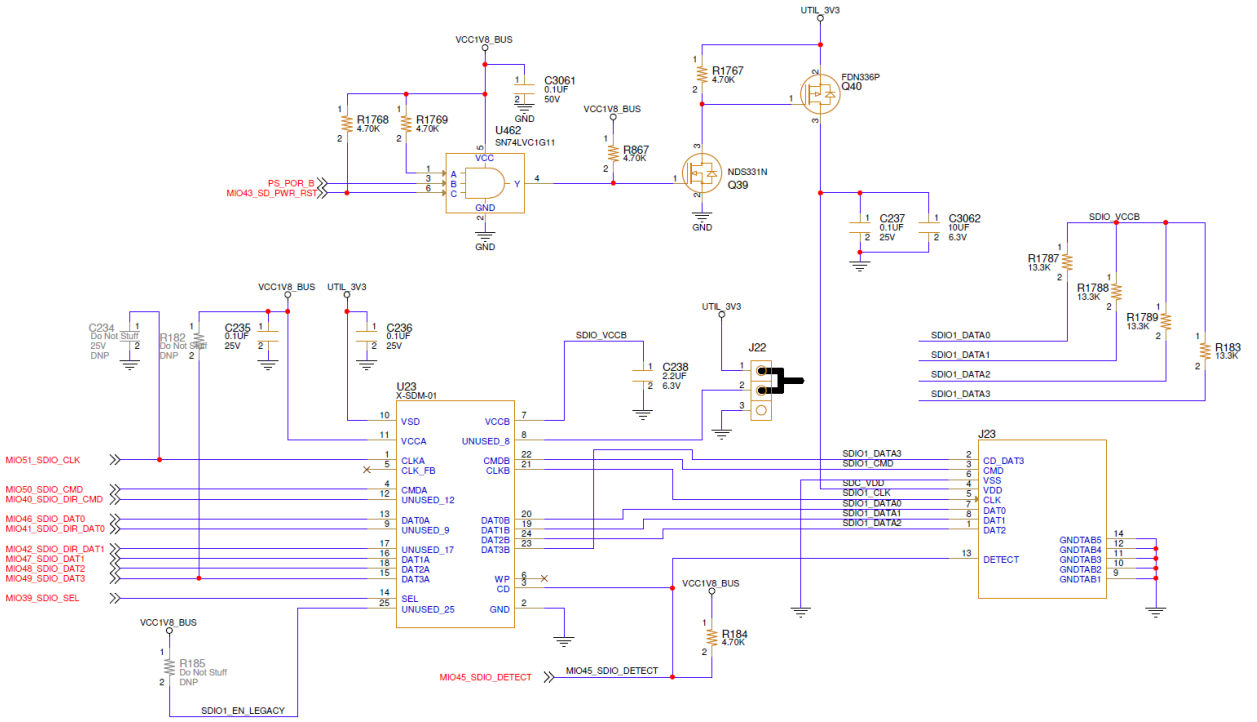
[Figure 2, callout 7]

The ZCU670 board includes a secure digital input/output (SDIO) interface to provide access to general purpose non-volatile SDIO memory cards and peripherals. Information for the SD I/O card specification can be found on the SanDisk Corporation or SD Association websites. The ZCU670 SD card interface supports the SD1_LS configuration boot mode documented in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

The SDIO signals are connected to ZU67DR RFSoC PS bank 501 which has its VCCMIO set to 1.8V. The SD interface nets MIO[46:49]_SDIO_DAT[0:3], MIO50_SDIO_CMD, and MIO51_SDIO_CLK each have a series 30Ω resistor at the Bank 501 source. An NXP NVT4857UK SD 3.0-compliant voltage level-translator U23 is present between the ZU67DR RFSoC and the SD card connector (J23). The NXP NVT4857UK U23 device provides SD3.0 capability with SDR104 performance.

The following figure shows the connections of the SD card interface on the ZCU670 board.

Figure 11: **SD Card Interface**



X25730-091021

The NXP SD3.0 level shifter is mounted on an X-SDM-01 interposer board that has the pin mapping shown in the following table.

Table 15: **NVT4857UK U23 Adapter Pinout**

Adapter Pin Number	NVT4857UKAZ Pin Number	NVT4857UKAZ Pin Name
1	D2	CLKA
2	C3, C2	GND
3	B2	CD
4	C1	CMDA
5	E2	CLK_FB
6	Unused	Unused

Table 15: **NVT4857UK U23 Adapter Pinout** *(cont'd)*

Adapter Pin Number	NVT4857UKAZ Pin Number	NVT4857UKAZ Pin Name
7	B3	VCCB
8	Unused	Unused
9	Unused	Unused
10	A3	VSD
11	A2	VCCA
12	Unused	Unused
13	D1	DAT0A
14	E3	SEL
15	B1	DAT3A
16	E1	DAT1A
17	Unused	Unused
18	A1	DAT2A
19	E4	DAT1B
20	D4	DAT0B
21	D3	CLKB
22	C4	CMDB
23	B4	DAT3B
24	A4	DAT2B
25	Unused	Unused

For more information on the NVT4857UK, see the NXP website.

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

USB0 (MIO 52-63) USB 3.0 Transceiver and USB 2.0

The USB interface on the PS-side serves multiple roles as a host or device controller. The USB 3.0 interface (host mode only) is supported by the RFSoC GTR interface while the USB 2.0 (host and device modes) capabilities of the SMSC USB3320C controller are shared on a common USB 3.0 micro USB type A connector (J18).

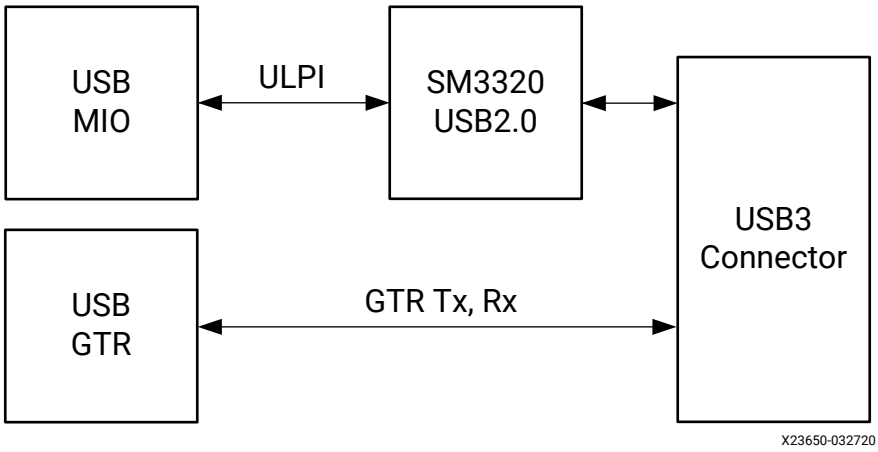
USB 3.0 Transceiver and USB 2.0 ULPI PHY

[Figure 2, callout 6]

The ZCU670 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver (U6) to support a USB connection to the host computer. A USB cable is supplied in the ZCU670 Evaluation Kit (standard-A connector to host computer, USB 3.0 A connector to ZCU670 board connector J18). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI + low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The following figure shows the USB 3.0 interface. USB 3.0 is host mode only.

Figure 12: **USB Interface**



The USB3320 is clocked by a 24 MHz crystal (X2). See the Standard Microsystems Corporation USB3320 data sheet for clocking mode details.

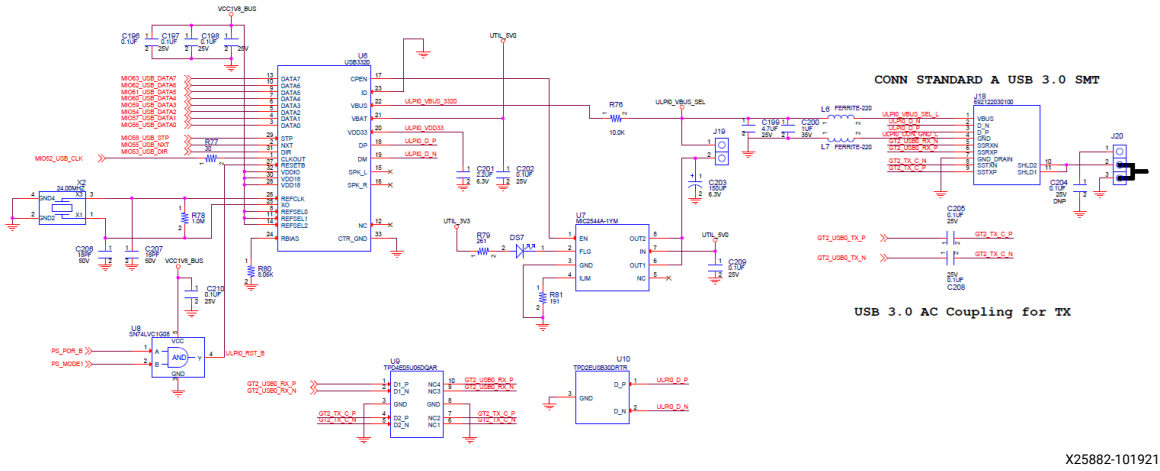
The interface to the USB3320 PHY is implemented through the IP in the ZU67DR RFSoC Processor System (PS). USB OTG support is available for USB 2.0. See Table 3 for USB 2.0 jumper settings.

***Note*:** The shield for the USB 3.0 micro-B connector (J18) can be tied to GND by a jumper on header J20 pins 2-3 (default). The USB shield can optionally be connected through a series capacitor to GND by installing a capacitor (body size 0402) at location C204 and jumping pins 1-2 on header J20.

The USB3320 ULPI U6 transceiver circuit (see the following figure) has a Micrel MIC2544 high-side programmable current limit switch (U7). This switch has an open-drain output fault flag on pin 2, which will turn on LED DS7 if overcurrent or thermal shutdown conditions are detected. DS7 is located adjacent to the USB J18 connector (Figure 2, callout 6).

The following figure shows the ULPI U6 transceiver circuit.

Figure 13: **USB3320 ULPI USB 2.0 Transceiver Circuit**



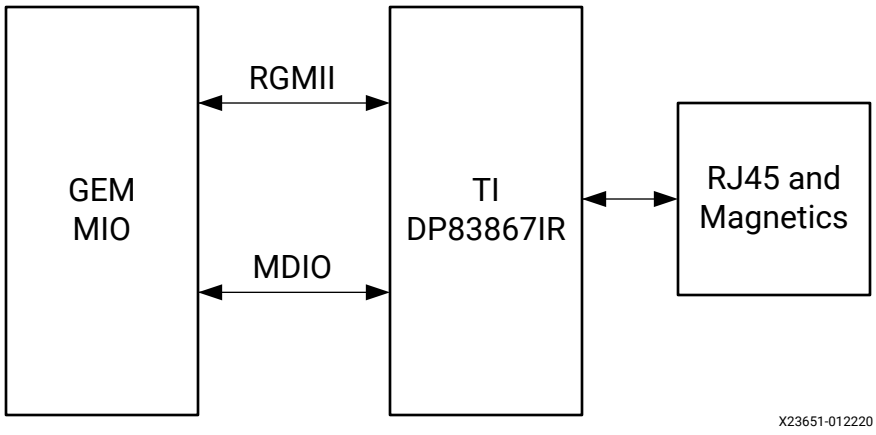
The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

GEM3 Ethernet (MIO 64-77)

[Figure 2, callout 16]

The PS-side Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface, shown in the following figure, which connects to a TI DP83867IRPAP Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector. The RGMII Ethernet PHY is boot strapped to PHY address `5'b01100` (`0x0C`) and Auto Negotiation set to *Enable*. Communication with the device is covered in the TI DP83867 RGMII PHY data sheet on the Texas Instruments website.

Figure 14: **Ethernet Block Diagram**



10/100/1000 MHz Tri-Speed Ethernet PHY

[Figure 2, callout 16]

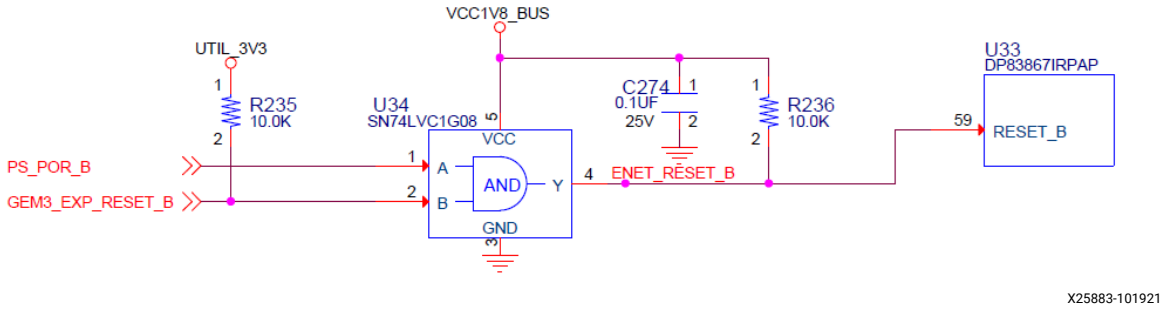
The ZCU670 board uses the TI DP83867IRPAP Ethernet RGMII PHY (U33) (see Texas Instruments website) for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Wurth 7499111221A RJ-45 connector (P1) with built-in magnetics.

Ethernet PHY Reset

The DP83867IRPAP PHY U33 reset circuit is shown in the following figure. The DP83867IRPAP can be reset by the GEN3_EXP_RESET_B signal through the I2C0 TCA6416A U15 bus expander P06 pin 10 or the PS_POR_B signal generated by the MAX16025 U6 POR device pin 11.

SW4 pushbutton at the MAX16025 U5 pin 6 input also triggers a PS_POR_B signal.

Figure 15: **Ethernet PHY Reset Circuit**



Ethernet PHY LED Interface

[Figure 2, callout 16]

The DP83867IRPAP PHY U33 LED interface (LED_0, LED_2) uses the two LEDs embedded in the P1 RJ45 connector bezel. The LED functional description is as shown in the following table.

Table 16: **Ethernet PHY LED Functional Description**

Pin Name	Type	Description
LED_2	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable by means of LEDCR1[11:8] register bits. ***Note*:** This pin is a strap configuration pin for RGZ devices only.
LED_1	S, I/O, PD	By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable by means of LEDCR1[7:4] register bits.

Table 16: **Ethernet PHY LED Functional Description** *(cont'd)*

Pin Name	Type	Description
LED_0	S, I/O, PD	By default, this pin indicates that link is established. Additional functionality is configurable by means of LEDCR1[3:0] register bits.

The LED functions can be re-purposed with a LEDCR1 register write available through the PHYs management data interface, MDIO/MDC. LED_2 is assigned to ACT (activity indicator) and LED_0 indicates link established.

LED_1 (100BASE-T link established) is a separate LED DS8 located on the top side of the board near the RJ45 P1 connector (Figure 2, callout 16).

For more Ethernet PHY details, see the TI DS83867 data sheet on the Texas Instruments website.

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

Programmable Logic JTAG Programming Options

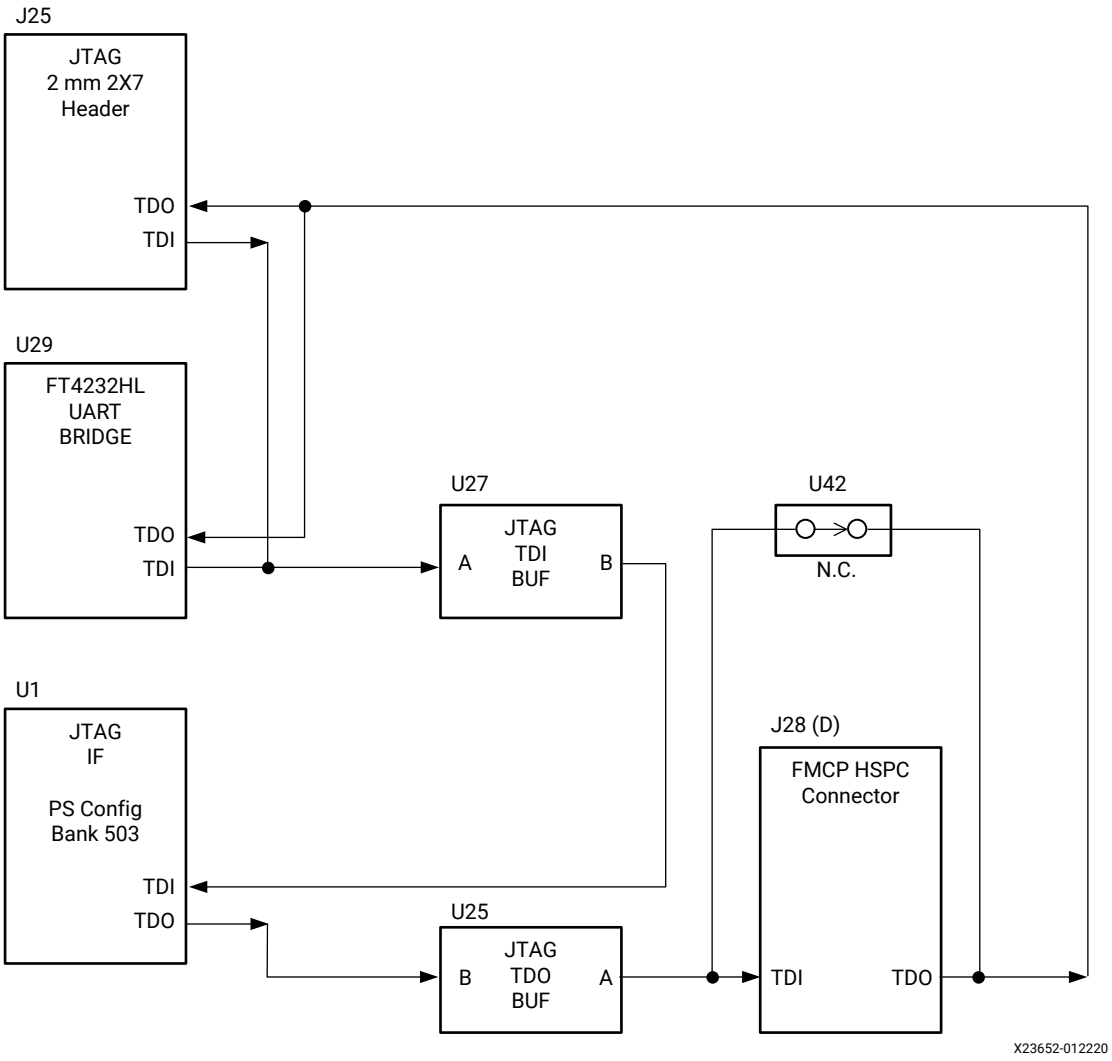
[Figure 2, callouts 8 and 9]

ZCU670 JTAG chain:

- J24 USB micro AB connector connected to U29 FT4232HL USB-JTAG bridge
- J25 2x7 2 mm shrouded, keyed JTAG pod flat cable connector

The ZCU670 board JTAG chain is shown in the following figure.

Figure 16: **JTAG Chain Block Diagram**



Clock Generation

The ZCU670 board provides fixed and variable clock sources for the ZU67DR Zynq UltraScale+ RFSoC. The following table lists the source devices for each clock.

Table 17: **ZCU670 Board Clock Sources**

Clock (Net) Name	Frequency	Clock Source
Fixed Frequency Clocks		
PS_REF_CLK	33.33 MHz	U130 SI570 I2C PROG. OSC. (0x5D)
SI5381_CLK_125	125 MHz	U43 SI5381A PROG. CLK GEN (0x76)
SI5381_GTR_REFCLK_USB3	26 MHz	

Table 17: **ZCU670 Board Clock Sources** *(cont'd)*

Clock (Net) Name	Frequency	Clock Source
Programmable Frequency Clocks		
USER_SI570_C0	300 MHz (Default)	U47 SI570 I2C PROG. OSC. (0x5D)
USER_MGT_SI570_CLOCK	156.25 MHz (Default)	U48 SI570 I2C PROG. OSC. (0x5D)
BUF_GTR_REF_CLK0	–	U429 SI53340 clock multiplexer
BUF_GTR_REF_CLK1	–	
BUF_GTR_REF_CLK3	–	
SI5381_DAC_REFCLK	122.88 MHz (Default)	U43 SI5381A PROG. CLK GEN (0x76)
SI5381_AMS_SYSREF	–	
SI5381_PL_SYSREF	–	
SI5381_ADC_REFCLK	122.88 MHz (Default)	
SI5381_PL_CLK	245.76 MHz (Default)	
SI5381_SMA_SE	10 MHz (Default)	
ADC_CLK_226	User-provided source	J8 (P)/J98 (N) SSMP connector
DAC_CLK_228	User-provided source	J99 (P)/J100 (N) SSMP connector
Various 8A34001 eCPRI clocks	Various	U409 8A34001 (0x58)

The following table lists the connections for each clock.

Table 18: **Clock Connections to ZU67DR U1**

Clock Source Ref. Des. and Pin	Net Name	I/O Standard
U130 SI570 I2C PROG. OSC.		
U130.4	PS_REF_CLK (series R300)	1
U47 SI570 I2C Prog. Oscillator DDR4 C0 I/F (300 MHz Default)		
U47.4	USER_SI570_C0_P	LVDS
U47.5	USER_SI570_C0_N	LVDS
U48 SI570 I2C PROG. OSC. (156.25 MHz Default)		
U48.4	USER_MGT_SI570_CLOCK_P	2
U48.5	USER_MGT_SI570_CLOCK_N	2
U43 SI5381A Programmable Clock Generator		
U43.21	SI5381_DAC_REFCLK_P	2
U43.20	SI5381_DAC_REFCLK_N	2
U43.24	SI5381_AMS_SYSREF_P	LVDS
U43.23	SI5381_AMS_SYSREF_N	LVDS
U43.28	SI5381_PL_SYSREF_P	LVDS
U43.27	SI5381_PL_SYSREF_N	LVDS
U43.35	SI5381_ADC_REFCLK_P	2
U43.34	SI5381_ADC_REFCLK_N	2

Table 18: **Clock Connections to ZU67DR U1** *(cont'd)*

Clock Source Ref. Des. and Pin	Net Name	I/O Standard
U43.38	SI5381_GTR_REF_CLK_P	2
U43.37	SI5381_GTR_REF_CLK_N	2
U43.42	SI5381_PL_CLK_P	LVDS
U43.41	SI5381_PL_CLK_N	LVDS
U43.45	SI5381_GTR_REFCLK_USB3_P	2
U43.44	SI5381_GTR_REFCLK_USB3_N	2
U43.51	SI5381_CLK_125_P	LVDS
U43.50	SI5381_CLK_125_N	LVDS
U43.54	SI5381_SMA_SE (undefined on schematic)	LVCMOS
ADC_CLK_226		
J8 (P) SMA CONN.	ADC_CLK_226_P	See *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
J98 (N) SMA CONN.	ADC_CLK_226_N	See *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
DAC_CLK_228		
J99 (P) SMA CONN.	DAC_CLK_228_P	See *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
J100 (N) SMA CONN.	DAC_CLK_228_N	See *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
U409 8A34001 eCPRI Clock		
U409.A9 (Q1)	8A34001_Q1_OUT_P	2
U409.B9 (Q1)	8A34001_Q1_OUT_N	2
U409.A11 (Q2)	8A34001_Q2_OUT_P	LVDS
U409.B11 (Q2)	8A34001_Q2_OUT_N	LVDS
U409.A12 (Q3)	8A34001_Q3_OUT_P	LVDS
U409.B12 (Q3)	8A34001_Q3_OUT_N	LVDS
U409.M8 (Q7)	8A34001_Q7_OUT_P	2
U409.L8 (Q7)	8A34001_Q7_OUT_N	2
U409.A6 (Q8)	8A34001_Q8_OUT_P	LVDS
U409.B6 (Q8)	8A34001_Q8_OUT_N	LVDS
U409.M6 (Q11)	8A34001_Q11_OUT_P	2
U409.L6 (Q11)	8A34001_Q11_OUT_N	2

Notes:

1. U1 ZU67DR Bank 503 supports LVCMOS18 level inputs.
2. Series capacitor coupled, U1 MGT (I/O standards do not apply).

SI5381A 10 Independent Output Any-Frequency Clock Generator U43

[Figure 2, callout 10]

- Clock generator: Skyworks Solutions, Inc. (SiLabs) SI5381A-E13960-GMR
- I2C programmable
- Jitter: <72 fs RMS typical
- Differential and single-ended factory default outputs

The SI5381A data sheet addendum for the Skyworks Solutions, Inc. (SiLabs) SI5381A-E13960-GMR documents the pre-programmed output frequencies:

- Inputs:
  - XAXB: 54.000000 MHz
  - Crystal mode
  - IN0: SMA Input J146
  - IN1: 8A34001_Q7_OUT
  - IN2: SI5381_CLK2_IN
  - FB_IN: SI5381_FEEDBACK (U43.OUT9)
- Outputs:
  - OUT0A: 122.88 MHz
  - Enabled, Diff_920mV
  - OUT0: Unused
  - OUT1: Unused
  - OUT2: N/C
  - OUT3: 122.88 MHz
  - Enabled, Diff_920 mV
  - OUT4: Unused
  - OUT5: 245.76 MHz
  - Enabled, LVDS Pulled to 1.2V
  - OUT6: 26 MHz
  - Enabled, LVDS

- OUT7: Unused
- OUT8: 10 MHz
- Enabled, LVCMOS (J147)
- OUT9: Unused

Programmable User SI570 Clocks

[Figure 2, callouts 4, 11, and 12]

The ZCU670 board has three I2C programmable SI570 low-jitter 3.3V LVDS differential oscillators, one assigned to the DDR4 component memory interface bank (Bank 65 I/F C0: U47), one assigned to the PS reference clock (Bank 503 U1.M25 PS_REF_CLK), and one assigned to GTY131 (U48).

On power-up, the user clocks default to a pre-programmed output frequency: DDR4 I/F U47 to 300.000 MHz, PS_REF_CLK U130 to 33.333333...MHz (33 + 1/3 MHz), and GTY I/F U48 to 156.250 MHz.

User applications can change the output frequency of each SI570 within the range of 10 MHz to 810 MHz through the I2C1 bus interface. Power cycling the ZCU670 board reverts user clocks to their default settings.

These oscillators can also be reprogrammed from MSP430 system controller U38 (see TI MSP430 System Controller on the Texas Instruments website for more system controller information and the ZCU670 Evaluation Board website for the *ZCU670 System Controller GUI Tutorial* (XTP698).

DDR4 memory interface C0 (U47) SI570:

- Programmable oscillator: Skyworks Solutions, Inc. (SiLabs) 570BAB001614DG (10 MHz-810 MHz, 300 MHz default)
- I2C `0x5D`
- LVDS differential output
- Total stability: 61.5 ppm

PS reference clock (U130) SI570:

- Programmable oscillator: Skyworks Solutions, Inc. (SiLabs) SI570JAC000900DGR (10 MHz-160 MHz, 33.333333...MHz (33 + 1/3 MHz) default)
- I2C `0x5D`
- LVCMOS single-ended output
- Total stability: 61.5 ppm

GTY SI570:

- Programmable oscillator: Skyworks Solutions, Inc. (SiLabs) SI570BAB000544DG (10 MHz-810 MHz, 156.250 MHz default)
- I2C `0x5D`
- LVDS differential output
- Total stability: 61.5 ppm

The SI5341A and SI570 data sheets can be found on the Silicon Labs website.

User SMA Clocks

[Figure 2, callout 34]

The ZCU670 board provides four clock inputs using single-ended (J128, J146) and three pairs of SMAs (J8/J98, J99/J100, J129, J143). This provides for single-ended 1588 eCPRI 1 PPS input and an AC coupled user clock input. This also provides for differential user ADC, DAC, and AC coupled 1588 eCPRI clock inputs.

The single-ended 1 PPS input from J128 is connected to Renesas (IDT) 8A34001 U409.J1. The single-ended AC coupled user input connects to Skyworks Solutions, Inc. (SiLabs) SI5381A U43.63 (IN0).

The ADC differential pair feeds into Zynq UltraScale+ RFSoC U1 ADC Bank 226. The P-side SMA J8 signal ADC_CLK_226_P connects to U1.AB5. The N-side SMA J98 signal ADC_CLK_226_N connects to U1.AB4. The DAC differential pair feeds into Zynq UltraScale+ RFSoC U1 ADC Bank 228. The P-side SMA J99 signal ADC_CLK_226_P connects to U1.J5. The N-side SMA J100 signal ADC_CLK_226_N connects to U1.J4 The differential 1588 eCPRI clock signal pair is series capacitor coupled to the Skyworks Solutions, Inc. (SiLabs) SI5381A. The P-side SMA J129 signal 8A31004_CLK3_P connects to U409.E1 CLK3_P. The N-side SMA J143 signal 8A31004_CLK3_N connects to U409.E2 CLK3_N.

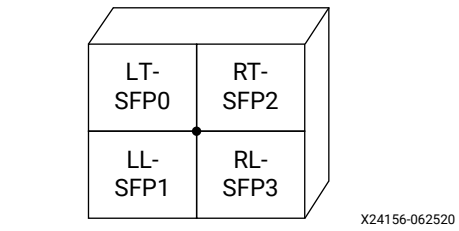
See *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926). The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

zSFP/zSFP+ Module Connectors

[Figure 2, callout 15]

The ZCU670 board hosts a quad zSFP/zSFP+ connector (J29) that accept zSFP or zSFP+ modules. The connectors are housed within a single 2x2 zSFP cage assembly. The following figure shows the zSFP/zSFP+ module locations within J29.

Figure 17: **Quad-zSFP Connector zSFP Locations**



The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

The following table lists the zSFP+ module control and status connections.

Table 19: **zSFP Control and Status Board Connections**

zSFP Control/ Status Signal	Board Connection	
SFP0 J29 LT[1, 2]		
SFP_TX_FAULT	Test Point TP11	High = Fault
		Low = Normal Operation
SFP_TX_DISABLE	Jumper J39 Switch Q6 U1.K16	Off = SFP Disabled
		On = SFP Enabled
SFP_MOD_DETECT	Test Point J12	High = Module not present
		Low = Module Present
SFP_RS0	PU R262 / PD R269	PU R262 = Full RX bandwidth
		PD R269 = Reduced RX bandwidth
SFP_RS1	PU R263 / PD R264	PU R263 = Full TX bandwidth
		PD R264 = Reduced TX bandwidth
SFP_LOS	Test Point TP13	High = Loss of receiver signal
		Low = Normal operation
SFP1 J29 LL[1, 2]		
SFP_TX_FAULT	Test Point TP14	High = Fault
		Low = Normal Operation
SFP_TX_DISABLE	Jumper J44 Switch Q7 U1.K17	Off = SFP Disabled
		On = SFP Enabled
SFP_MOD_DETECT	Test Point TP15	High = Module not present
		Low = Module Present
SFP_RS0	PU R270 / PD R273	PU R270 = Full RX bandwidth
		PD R273 = Reduced RX bandwidth

Table 19: **zSFP Control and Status Board Connections** *(cont'd)*

zSFP Control/ Status Signal	Board Connection	
SFP_RS1	PU R271 / PD R274	PU R271 = Full TX bandwidth
		PD R274 = Reduced TX bandwidth
SFP_LOS	Test Point TP16	High = Loss of receiver signal
		Low = Normal operation
SFP2 J29 RT [1, 2]		
SFP_TX_FAULT	Test Point TP5	High = Fault
		Low = Normal Operation
SFP_TX_DISABLE	Jumper J32 Switch Q4 U1.K14	Off = SFP Disabled
		On = SFP Enabled
SFP_MOD_DETECT	Test Point TP6	High = Module not present
		Low = Module Present
SFP_RS0	PU R279 / PD R281	PU R279 = Full RX bandwidth
		PD R281 = Reduced RX bandwidth
SFP_RS1	PU R280 / PD R282	PU R280 = Full TX bandwidth
		PD R282 = Reduced TX bandwidth
SFP_LOS	Test Point TP7	High = Loss of receiver signal
		Low = Normal operation
SFP3 J29 RL [1, 2]		
SFP_TX_FAULT	Test Point TP8	High = Fault
		Low = Normal Operation
SFP_TX_DISABLE	Jumper J35 Switch Q5 U1.K15	Off = SFP Disabled
		On = SFP Enabled
SFP_MOD_DETECT	Test Point TP9	High = Module not present
		Low = Module Present
SFP_RS0	PU R284 / PD R290	PU R284 = Full RX bandwidth
		PD R290 = Reduced RX bandwidth
SFP_RS1	PU R285 / PD R291	PU R285 = Full TX bandwidth
		PD R291 = Reduced TX bandwidth
SFP_LOS	Test Point TP10	High = Loss of receiver signal
		Low = Normal operation

Notes:

1. The RS0/RS1 PU/PD resistors are not populated. There are pull-down resistors built into the zSFP modules that select the lower bandwidth mode of the module.
2. BW selection is also available through I2C control.

User I/O

[Figure 2, callout 23, 24, and 25]

The ZCU670 board provides these user and general purpose I/O capabilities:

- Four single color LEDs (callout 23)
  - LED_0: DS54
  - LED_1: DS55
  - LED_2: DS56
  - LED_3: DS57
- One user pushbutton and a CPU reset PB switch (callouts 24 and 25)
  - GPIO_SW_PL: SW8
  - CPU_RESET: SW13

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

Power and Status LEDs

[Figure 2, area of callouts 17 and 18]

The following table defines the power and status LEDs. For user controlled GPIO LED details, see User I/O.

Table 20: **Power and Status LEDs**

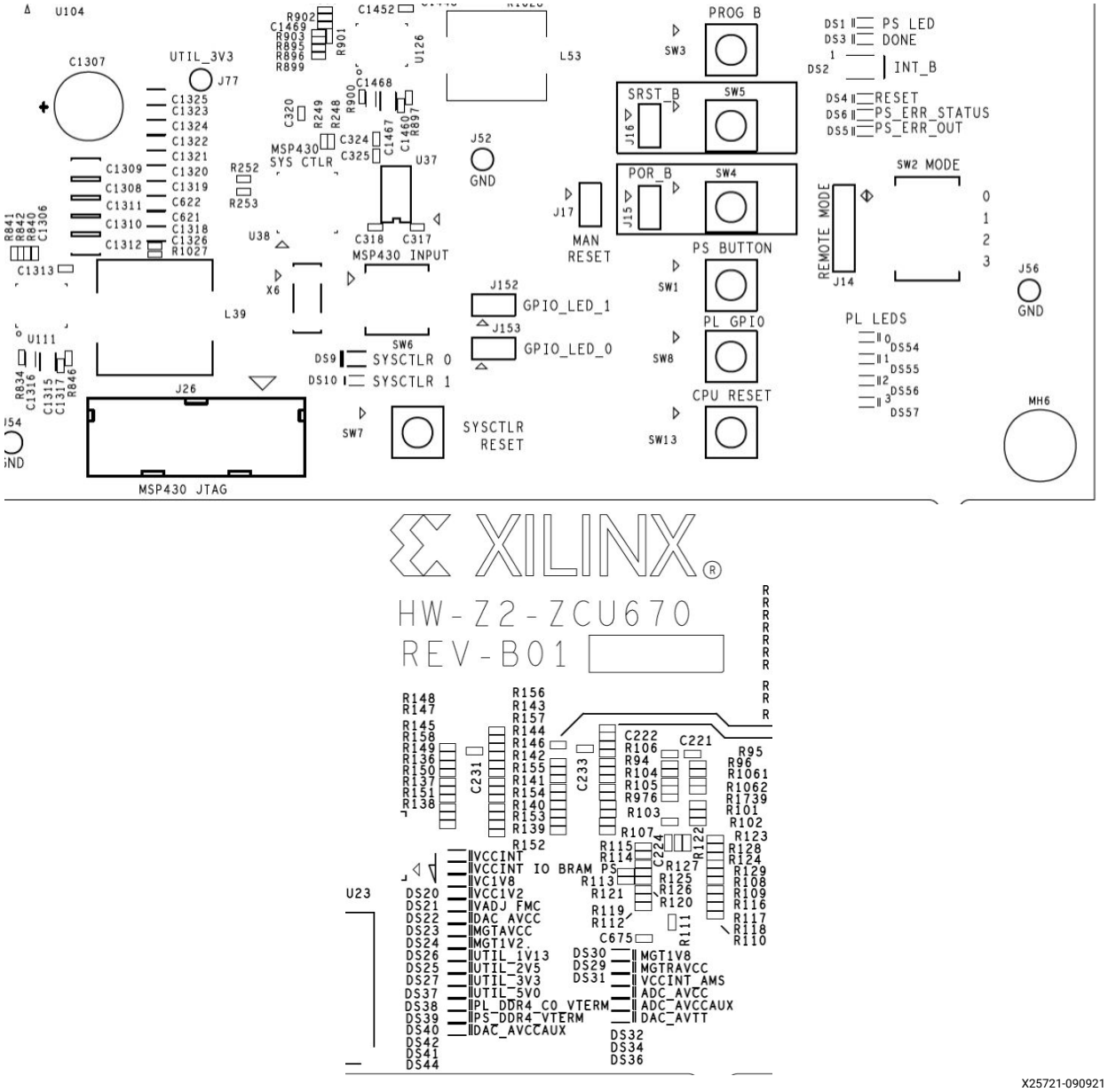
Ref. Des.	Schematic Net Name	LED Color	Description
DS1	MIO23_LED	Green	RFSoC U1 Bank 500 GPIO LED
DS2	PS_INIT_B	Green/ Red	Green: FPGA initialization was successful Red: FPGA initialization is in progress
DS3	PS_DONE	Green	RFSoC U1 bit file download is complete
DS4	PS_RESET_B	Red	POR U5 asserts RESET_B low when any of the monitored voltages (IN_) falls below its respective threshold, any EN_ goes low, or MR is asserted.
DS5	PS_ERR_OUT	Red	PS error out is asserted for accidental loss of power, an error in the PMU that holds the CSU in reset, or an exception in the PMU.
DS6	PS_ERR_STATUS	Red	PS error status indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.
DS7	USB3 MIC2544 U7 FLG	Green	PS USB 3.0 ULPI VBUS power error
P1-R	ENET_LED_0	Green	EPHY U33 link established (all speeds) (RJ45 bezel right)
DS8	ENET_LED_1	Green	EPHY U33 1000BASE-T link established
P1-L	ENET_LED_2	Green	EPHY U33 link activity (RJ45 bezel left)
DS9	MSP430_LED0	Blue	MSP430 U38 GPIO LED
DS10	MSP430_LED1	Green	MSP430 U38 GPIO LED
DS19	VCC12_SW	Green	12VDC power on

Table 20: **Power and Status LEDs** *(cont'd)*

Ref. Des.	Schematic Net Name	LED Color	Description
DS20	VCCINT_PG	Green	VCCINT 0.85VDC power On
DS21	VCCINT_IO_BRAM_PS_PG	Green	VCCPSINTFP/LP/block RAM/I/O 0.85VDC power on
DS22	VCC1V8_PG	Green	VCC1V8 1.8VDC power on
DS23	VCC1V2_PG	Green	VCC1V2 1.2VDC power on
DS24	VADJ_FMC_PG	Green	VADJ_FMC 1.8VDC (nom.) power on
DS25	MGTAVCC_PG	Green	MGTAVCC 0.9VDC power on
DS26	DAC_AVCC_PG	Green	ADC_AVCC 0.925V power on
DS27	MGT1V2_PG	Green	MGT1V2 1.2VDC power on
DS29	MGTRAVCC_PG	Green	MGTRAVCC 0.85VDC power on
DS30	MGT1V8_PG	Green	MGT1V8 1.8VDC power on
DS31	VCCINT_AMS_PG	Green	VCCINT_AMS 0.85VDC power on
DS32	ADC_AVCC_PG	Green	ADC_AVCC 0.925VDC power on
DS34	ADC_AVCCAUX_PG	Green	ADC_AVCCAUX 1.8VDC power on
DS36	DAC_AVTT_PG	Green	DAC_AVTT 2.5VDC power on
DS37	UTIL_1V13_PG	Green	UTIL_1V13 1.13VDC power on
DS38	UTIL_2V5_PG	Green	UTIL_2V5 2.5VDC power on
DS39	UTIL_3V3_PG	Green	UTIL_3V3 3.3VDC power on
DS40	UTIL_5V0_PG	Green	UTIL_5V0 5VDC power on
DS41	PS_DDR4_VTERM_0V60_PG	Green	PS_DDR4_VTERM 0.6VDC power on
DS42	PL_C0_DDR4_VTERM_0V60_PG	Green	PL_C0_DDR4_VTERM 0.6VDC power on
DS44	DAC_AVCCAUX_ON	Green	DAC_AVCCAUX 1.8VDC power on

The following figure shows the GPIO and power status LED areas of the board.

Figure 18: **GPIO and Power Status LED Areas**



Multi-Gigabit Transceivers

The ZU67DR Zynq UltraScale+ RFSoC has 4 GTR gigabit transceivers (6 Gb/s capable) on the PS-side and 8 GTY gigabit transceivers (28 Gb/s capable) on the PL-side. All 4 GTR and all 8 GTY transceivers are allocated.

GTY Transceivers

The GTY transceivers in the ZU67DR are grouped into two channels or quads. The reference clock for a quad can be sourced from the quad above or the quad below the GTY quad of interest. The two GTY quads used on the ZCU670 board have the connectivity listed below. The following table shows the MGTY assignments.

Table 21: **ZCU670 ZU67DR GTY Mapping**

ZCU670 ZU67DR-FSVE1156 GTY Mapping			
ZU67DR-FSVE1156	SFP3	ch3	GTY Quad 127
	SFP2	ch2	
	SFP1	ch1	
	SFP0	ch0	
	USER_MGT_REFCLK	refclk1	
	8A34001_CLK1	refclk0	
	FMCP_HSPC_DP3	ch3	GTY Quad 128
	FMCP_HSPC_DP2	ch2	
	FMCP_HSPC_DP1	ch1	
	FMCP_HSPC_DP0	ch0	
	8A34001_Q11_OUT	refclk1	
	8A34001_CLK2_IN	refclk0	

zSFP+

Four MGTs are provided by PL-side MGT banks 127 and 128 for the quad (2x2 connector) zSFP+ interface. Available GTY reference clocks include two sets of clocks to/from IDT 8A34001 U409. Each zSFP+ connector provides an I2C based control interface. This I2C interface is accessible for each individual zSFP+ module through the I2C multiplexer topology on the ZCU670.

For additional information on GTY transceivers, see the *UltraScale Architecture GTY Transceivers User Guide* (UG578).

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

PS GTR Transceivers

The PS-side GTR transceiver Bank 505 supports USB (3.0). The remainder of the GTR transceivers are connected to the FMC+ connector.

Bank 505 USB0 lane 2 supports the USB0 (USB3.0) interface described in USB 3.0 Transceiver and USB 2.0 ULPI PHY. The PS-side GTR transceiver provides USB 3.0 host-only connectivity. See Appendix A: VITA57.4 FMCP Connector Pinout.

Bank 505 lanes 0, 1, and 3 support FMC+ over J28.

Bank 505 reference clocks are connected to the U43 SI5341A clock generator as described in SI5381A 10 Independent Output Any-Frequency Clock Generator U43.

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

FPGA Mezzanine Card Interface

The ZCU670 evaluation board supports the VITA 57.4 FPGA mezzanine card plus (FMC+ or FMCP) specification by providing a subset implementation of the high pin count connector at J28 (HSPC). FMC+ connectors use a 14 x 40 form factor, populated with 560 pins. The connector is keyed so that a mezzanine card, when installed on the ZCU670 evaluation board, faces away from the board.

FMCP Connector J28

Samtec SEAF series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector. More information about SEAF series connectors is available on the Samtec, Inc. website. More information about the VITA 57.4 FMC+ specification is available on the VITA FMC Marketing Alliance website.

The 560-pin FMC+ connector defined by the FMC specification (see Appendix A: VITA57.4 FMCP Connector Pinout) provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 24 transceiver differential pairs
- 6 transceiver differential clocks
- 4 differential clocks
- 239 ground and 19 power connections

FMCP Connector J28

[Figure 2, callout 25]

The HSPC connector J28 implements a subset of the full FMCP connectivity:

- 68 single-ended or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- 8 transceiver differential pairs
- 2 transceiver differential clocks
- 2 differential clocks
- 239 ground and 16 power connections

See the FPGA Mezzanine Card (FMC) VITA 57.4 specification on the VITA FMC Marketing Alliance website for additional information on the FMCP HSPC connector.

The detailed RFSoC connections for the feature described in this section are documented in the ZCU670 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

Cooling Fan Connector

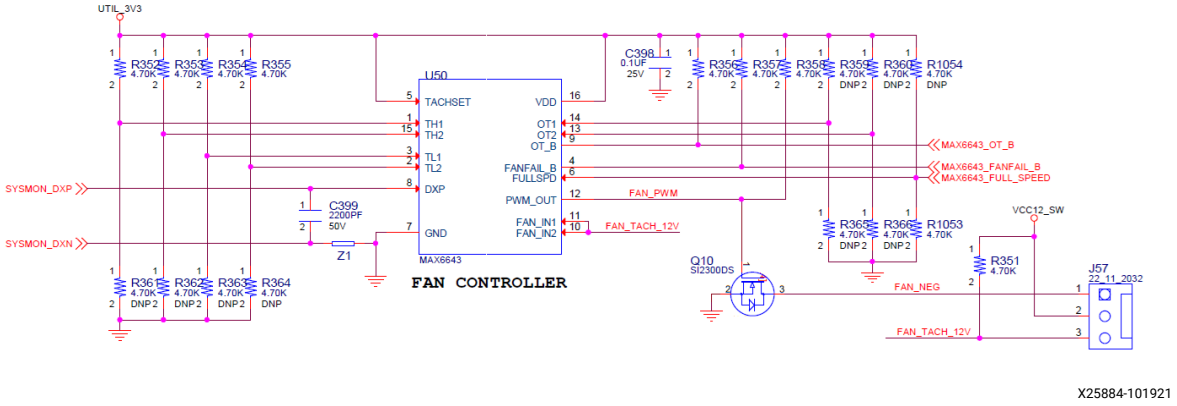
[Figure 2, near callout 33]

The ZCU670 uses the Infineon MAX6643 (U50) fan controller, which autonomously controls the fan speed by controlling the pulse width modulation (PWM) signal to the fan based on the die temperature sensed via the FPGA's DXP and DXN pins. The fan rotates slowly (acoustically quiet) when the RFSoC is cool and rotates faster as the FPGA heats up (acoustically noisy). The fan speed (PWM) versus the RFSoC die temperature algorithm along with the over temperature set point and fan failure alarm mechanisms are defined by the strapping resistors on the MAX6643 device. The over temperature and fan failures alarms can be monitored by any available processor in the RFSoC by polling the I2C expander U15 on the I2C0 bus. See the MAX6643 data sheet on the Maxim Integrated Circuits website for more information on the device circuit implementation on this board.

The ZCU670 cooling fan circuit is shown in the following figure.

Note: At initial power on, it is normal for the fan controller to energize at full speed for a few seconds.

Figure 19: **ZCU670 Cooling Fan Circuit**



VADJ_FMC Power Rail

The ZCU670 evaluation board implements the ANSI/VITA 57.1 section 5.5.1 IPMI support functionality. The power control of the VADJ_FMC power rail is managed by the U38 system controller. This rail powers the FMCP HSPC (J28) VADJ pins, as well as the ZU67DR HP banks 66 and 67. The valid values of the VADJ_FMC rail are 1.2V, 1.5V, and 1.8V.

At power on, the system controller detects if an FMC module is installed on J28:

- If no card is attached to the FMCP connector, the VADJ voltage is set to 1.8V.
- When an FMC card is attached, its IIC EEPROM is read to find a VADJ voltage supported by both the ZCU670 board and the FMC module, within the available choices of 0.0V, 1.2V, 1.5V, and 1.8V.
- If no valid information is found in an FMC card IIC EEPROM, the VADJ_FMC rail is set to 0.0V.

The system controller user interface allows the FMC IPMI routine to be overridden and an explicit value can be set for the VADJ_FMC rail. Override mode is useful for FMC mezzanine cards that do not contain valid IPMI EPROM data defined by the ANSI/VITA57.1 specification.

ZCU670 MSP430 System Controller

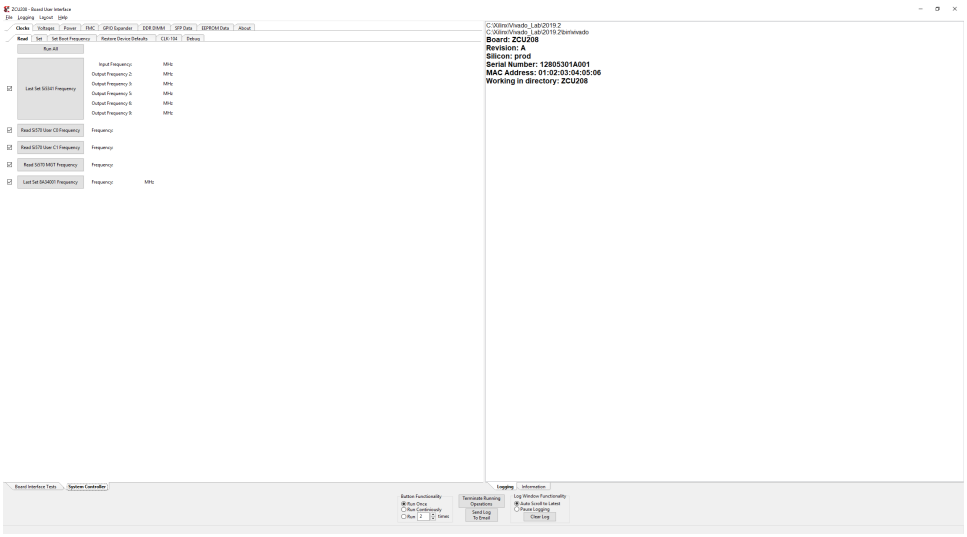
[Figure 2, callout 19]

The ZCU670 board includes an on-board MSP430 (U38) with integrated power advantage demonstration and system controller firmware. A host PC resident system controller board user interface is provided on the ZCU670 Evaluation Board website. The board user interface allows the query and control of select programmable features such as clocks, FMC functionality, and power system parameters. The ZCU670 website also includes the *ZCU670 System Controller GUI Tutorial* (XTP698) and *ZCU670 Software Install and Board Setup Tutorial* (XTP699).

These steps briefly summarize these instructions.

1. Ensure that the Skyworks Solutions, Inc. (SiLabs) VCP USB-UART drivers are installed *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033).
2. Download the board user interface host PC application from the board documentation website.
3. Connect the micro-USB cable to the ZCU670 USB-UART connector (J24).
4. Power-cycle the ZCU670.
5. Observe that SYSCTLR LED0 (DS9) blinks and LED1 (DS10) is illuminated.

6. Launch the board user interface application.



On first use of the board user interface, go to the **FMC → Set VADJ → Boot-up** tab and click **USE FMC EEPROM Voltage**. The board user interface buttons gray out during command execution and return to their original appearance when ready to accept a new command.

See the *ZCU670 System Controller GUI Tutorial* (XTP698) and the *ZCU670 Software Install and Board Setup Tutorial* (XTP699) for more information on installing and using the system controller board user interface utility.

Switches

[Figure 2, callouts 23 and 24]

The ZCU670 board includes the following power, configuration, and reset switches:

- SW15 power on/off slide switch (callout 24)
- SW3 (PS_PROG_B), active-Low pushbutton (callout 23)
- SW4 (POR_B), active-Low pushbutton (callout 23)
- SW5 (SRST_B), active-Low pushbutton (callout 23)
- SW2 U1 RFSoC PS bank 503 4-pole mode DIP switch (callout 23)

Power On/Off Slide Switch

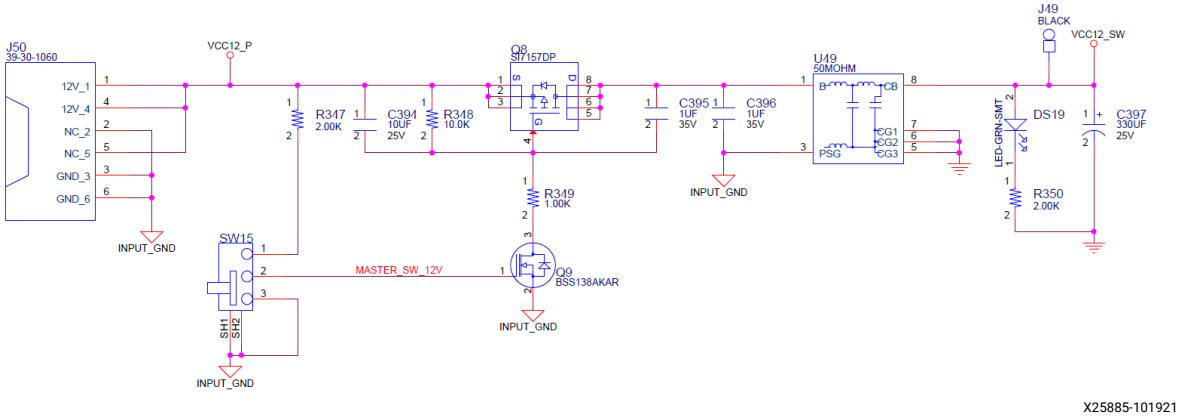
[Figure 2, callout 24]

The ZCU670 board power switch is SW15. Sliding the switch actuator from the *off* to *on* position applies 12V power from J50, a 6-pin mini-fit connector. Green LED (DS19) illuminates when the ZCU670 board power is on. See Board Power System for details on the onboard power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the ZCU670 board power connector J50. The ATX 6-pin connector has a different pinout than J50. Connecting an ATX 6-pin connector into J50 damages the ZCU670 board and voids the board warranty.*

The following figure shows the power connector J50, power switch SW2, and LED indicator DS19.

Figure 20: **ZCU670 Power Input**



Program_B Pushbutton

[Figure 2, callout 23]

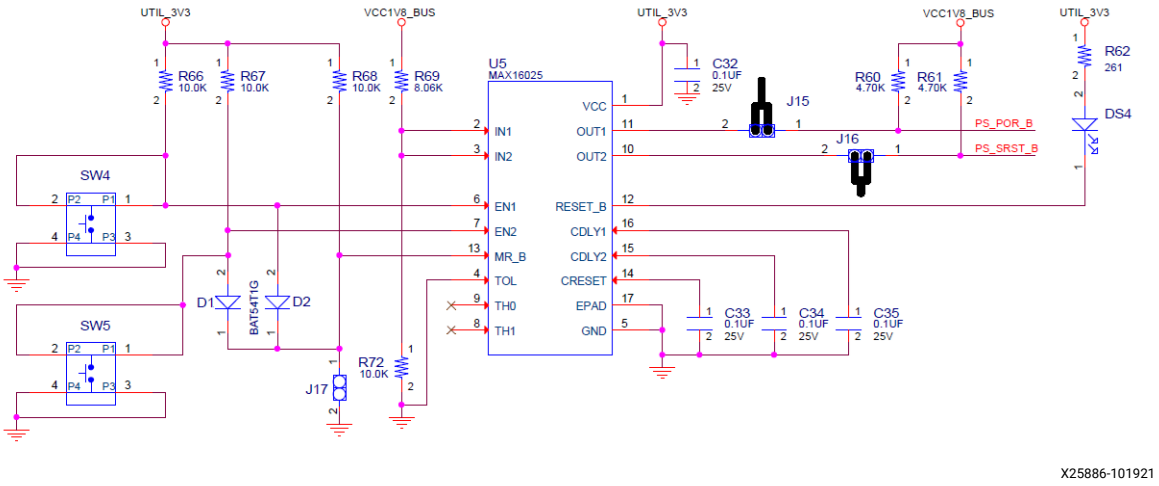
PS_PROG_B pushbutton switch SW3 grounds the ZU67DR RFSoC PS_PROG_B pin when pressed. This action clears programmable logic configuration, which the PS software can then act on. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for information about the Zynq UltraScale+ RFSoC configuration.

System Reset Pushbuttons

[Figure 2, callout 23]

The following figure shows the reset circuitry for the processing system.

Figure 21: **POR_B SW4 and PS SRST_B SW5 Pushbutton Switches**



PS_POR_B Reset

Depressing and then releasing pushbutton SW4 causes net PS_POR_B to strobe Low. This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B must be generated by the power supply power-good signal. When the voltage at IN1 is below its threshold or EN1 (P.B. switch SW4 is pressed) goes Low, OUT1 (PS_POR_B) goes Low.

PS_SRST_B Reset

Depressing and then releasing pushbutton SW5 causes net PS_SRST_B to strobe Low. This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps. When the voltage at IN2 is below its threshold or EN2 (P.B. switch SW5 is pressed) goes Low, OUT2 (PS_SRST_B) goes Low.

Active-Low Reset Output RESET_B asserts when any of the monitored voltages (IN_) falls below its respective threshold, any EN_ goes Low, or MR is asserted. RST_B remains asserted for the reset time-out period after all of the monitored voltages exceed their respective threshold, all EN_ are High, all OUT_ are high, and MR is de-asserted. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for more information about resets.

Board Power System

[Figure 2, callout 39, 40, and 41]

The ZCU670 evaluation board uses power management ICs (PMIC) and regulators from Infineon Integrated Circuits and MPS to supply the core and auxiliary voltages listed in the following table. Reference schematic 038-05003-01.

Table 22: **ZCU670 Power System Devices**

Ref. Des., PMBUS ADDR	Controller or Regulator	Rail Name	Voltage (V)	Max. Current (A)	INA226 Power Monitor	INA226 PMBUS ADDR	Sense Resistor (Ω)	Schem. Page
PMIC1 U104 (0X40)	IR35215_PWM1/2	V_{CCINT}	0.85	60	U65	0x40	R440: 0.0005	44
	IR35215_PWM1_L2	V_{CCINT_AMS}	0.85	28	U61	0x49	R1098: 0.0005	
PMIC2 U53 (0X44)	IRPS5401_A	V_{CC1V2}	1.2	6	U58	0x43	R408: 0.005	47
	IRPS5401_B	UTIL_1V13	1.13	500 mA	NA	NA	NA	
	IRPS5401_C	VADJ_FMC	1.8	6	U62	0x45	R382: 0.005	
	IRPS5401_D	Tied to channel C						
	IRPS5401_LDO	MGT1V8	1.8	500 mA	U64	0x48	R787: 0.005	
PMIC3 U55 (0X45)	IRPS5401_A	NC	NA	NA	NA	NA	NA	49
	IRPS5401_B	UTIL_2V5	2.5	500 mA	NA	NA	NA	
	IRPS5401_C	MGT1V2_BUS	1.2	7	U63	0x47	R400: 0.002	
	IRPS5401_D	Tied to C						
	IRPS5401_LDO	MGTRAVCC	0.85	500 mA	NA	NA	NA	
U127 (0X4B)	IR38164	$V_{CCINT\_IO\_BRAM\_PS\_BUS}$	0.85	18	U57	0x41	R1099: 0.0005	50
U112 (0x43)	IR38164	MGTAVCC_BUS	0.9	4	U67	0x46	R455: 0.002	51
U123 (0x4C)	IR38164	VCC1V8_BUS	1.8	8	U60	0x42	R879: 0.002	52
U115	MPM3683-7	ADC_AVCC_BUS	1.01	4	U75	0x4C	R499: 0.005	53
U116	MPM3683-7	DAC_AVCC_BUS	0.925	6	U77	0x4E	R504: 0.005	53
U114	MPM3833C	ADC_AVCCAUX	1.8	2	U71	0x4D	R475: 0.005	54
U125	MPM3833C	DAC_AVCCAUX	1.8	1.5	U124	0x4B	R889: 0.005	55
U118	MPM3833C	DAC_AVTT_BUS	2.5/3.0	1.5	U59	0x4A	R869: 0.005	55
U111	IR3889	UTIL_3V3	3.3	15	NA	NA	NA	57
U126	IR3889	UTIL_5V0	5	10	NA	NA	NA	58
U79	TPS51200	PL_DDR4_C0_VTT	0.6	+/- 3.0	NA	NA	NA	59

The FMCP HSPC (J28) V_{ADJ} pins and RFSoC U1 banks 66 and 67 V_{CCO} pins are wired to the programmable rail VADJ_FMC. The VADJ_FMC rail is programmed to 1.80V by default.

Documentation describing PMBUS programming for the Infineon power controllers as well as PMIC and voltage regulator data sheets are available on the Infineon Integrated Circuits website.

Non-PMBus ADC and DAC voltage regulator data sheets can be viewed on the MPS website.

The PCB layout and power system design meet the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583).

RECOMMENDED: *To ensure reliable operation, Xilinx recommends running the* `report_power` *command in the Vivado tools for designs targeting this board. The reported rail current requirements must not exceed the values listed in the following table.*

Table 23: **Device Rail Maximum Current**

Device Rail	Maximum Current (Amps)
V_{CCINT}	60
V_{CCINT_IO} + V_{CCBRAM} + $V_{CC\_PSINTLP}$ + $V_{CC\_PSINTFP}$ + $V_{CC\_PSINTFP\_DDR}$	18
$MGTYV_{CCAUX}$ + $V_{PS\_MGTRAVTT}$	0.5
$MGTYA_{VCC}$	4
$V_{PS\_MGTRAVCC}$	0.5
$MGTYA_{VTT}$ + V_{CC_PSPLL}	7
V_{CCINT_AMS}	28
V_{ADC_AVCC}	4
$V_{ADC\_AVCCAUX}$	2
V_{DAC_AVCC}	6
$V_{DAC\_AVCCAUX}$	1.5
V_{DAC_AVTT}	1.5
V_{CCAUX} + V_{CCAUX_IO} + V_{CCO} 1.8V + V_{CCAUX_IO} + V_{CC_PSAUX} + $V_{CC\_PSDDR\_PLL}$ + $V_{CCO\_PSIO0\_500}$ + $V_{CCO\_PSIO1\_501}$ + $V_{CCO\_PSIO2\_502}$ + $V_{CCO\_PSIO3\_503}$ + V_{CCADC} + V_{CC_PSADC}	8
V_{CCO} 1.2V + $V_{CCO\_PSDDR\_504}$	6
V_{CCO} #V (# corresponds to VADJ programmed voltage)	6

The total device power must remain under 50W. To assist the Vivado tools in reporting when power exceeds this amount, add this XDC constraint:

```
set_operating_conditions -design_power_budget 50 ;# (50W max power)
```

Monitoring Voltage and Current

Voltage and current monitoring and control are available for the Infineon power system controllers through the Infineon PowIRCenter graphical user interface. The PMBus interface controllers and regulators are accessed through 1x3 PMBus connector J21, that is provided for use with the Infineon PowIRCenter USB cable (Infineon part number USB005) and can be ordered from the Infineon Integrated Circuits website. The associated Infineon PowerTool GUI can be downloaded from the Infineon website. This is the simplest and most convenient way to monitor the voltage and current values for the Infineon PMBus programmed power rails listed in Table 22.

Each Infineon PMIC controller is capable of reporting the voltage and current of its controlled rail to the Infineon GUI for display to the user. Fourteen rails have a TI INA226 PMBus power monitor circuit with connections to the rail series current sense resistor. This arrangement permits the INA226 to report the sensed parameters separately on the INA226_PMBUS. The rails configured with the INA226 power monitors are shown in Table 22.

As described in I2C0 (MIO 14-15), the I2C0 bus provides access to the PMBus power controllers and the INA226 power monitors through the U17 PCA9544A bus switch. All PMBus controlled Infineon regulators are tied to the IRPS5401_SDA/SCL PMBUS, while the INA226 power monitors are separated on to INA226_PMBUS.

Figure 8 and Table 10 document the I2C0 bus access path to the Infineon PMBus controllers and INA226 power monitor op amps. Also refer to schematic 038-05070-01. Power rail measurements are accessible to the system controller and RFSoC PL logic through their respective I2C0 bus connections.

VITA57.4 FMCP Connector Pinout

The following figure shows the pinout of the FPGA plus mezzanine card (FMCP) high pin count (HSPC) connector defined by the VITA 57.4 FMC specification. For a description of how the ZCU670 evaluation board implements the FMCP specification, see FPGA Mezzanine Card Interface.

Figure 22: **FMCP HSPC Connector Pinout**

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

X25925-102921

AMD XILINX

Appendix B

Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the ZCU670 board provides for designs targeting the ZCU670 evaluation board. Net names in the constraints listed correlate with net names on the latest ZCU670 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) for more information.

The HSPC FMCP connector J28 is connected to Zynq® UltraScale+™ RFSoC U1 banks powered by the variable voltage VADJ_FMC. The FMC bank I/O standards must be uniquely defined by each customer because different FMC cards implement different circuitry.

IMPORTANT! *To access the XDC file, click the Documentation tab on the ZCU670 Evaluation Board website and select Board Files under Document Type.*

AMD XILINX

Appendix C

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a Support Service Request.

CE Information

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

CE Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

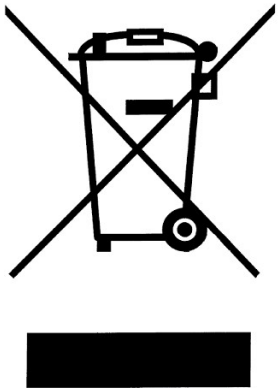
This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

CE Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

AMD XILINX

Appendix D

HW-XM650/755 Balun Daughter Cards for RFSoC EVM

Overview

XM650 and XM755 are the RFMC 2.0 add-on cards for use with the Zynq® UltraScale+™ RFSoC DFE ZCU670 evaluation board. These add-on cards enable ZCU670 connectivity from DAC and ADC for loopback evaluation and for instrumentation use cases. The ZCU670 board supports eight DACs and ten ADCs. The XM650 and XM755 cards provide connectivity of up to 16 DACs and 16 ADCs.

- The XM650 add-on card is a DAC to ADC loopback evaluation with N79 band baluns and filters, no external connectivity.
- The XM755 add-on card is a full break-out of 16 DAC channels x 16 ADC channels to SMA connectivity using Carlisle-CoreHC2 assembly connections.

Note: The following descriptions for pinout and RF tile figures are specific to the ZCU670 evaluation board. For pinouts and tile descriptions for other boards, see the applicable board user guide.

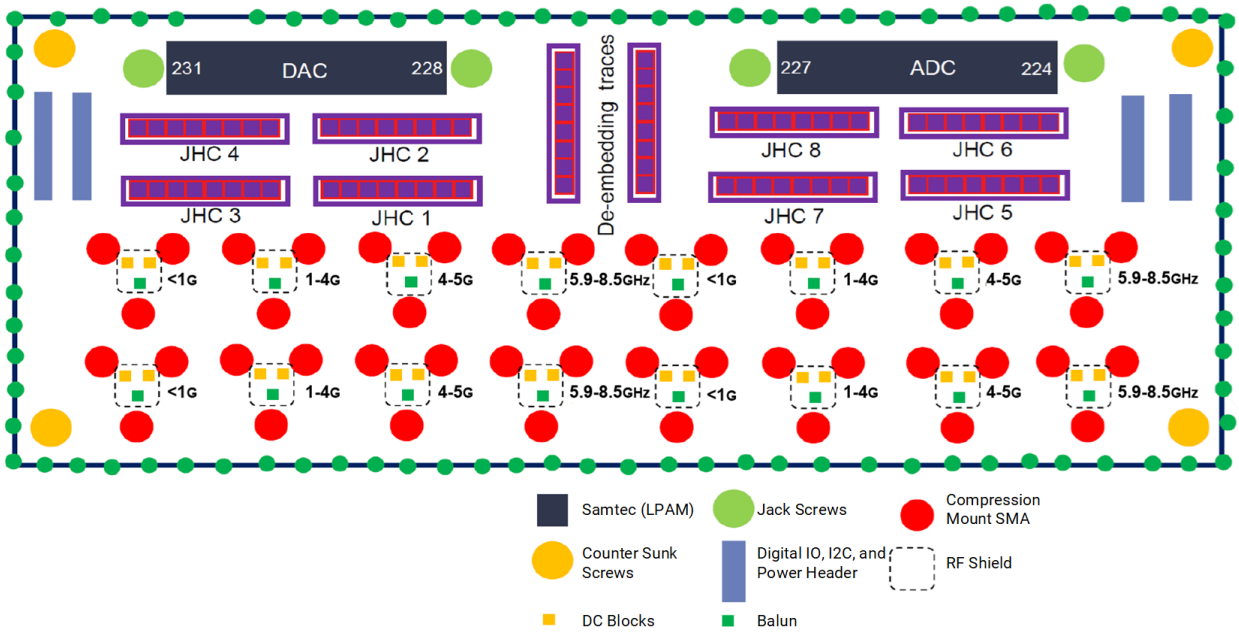
Table 24: **Add-on Board Features**

Feature	Description
Base board	ZCU670
ADC channels	10
DAC channels	8
Balun	XM650: N79 or B46 band with BOM change XM755: Low/mid/high frequency
Filter	XM650: N79 or B46 band with BOM change XM755: No
Interconnection	2x Samtec LPAM 8x50

Block Diagram

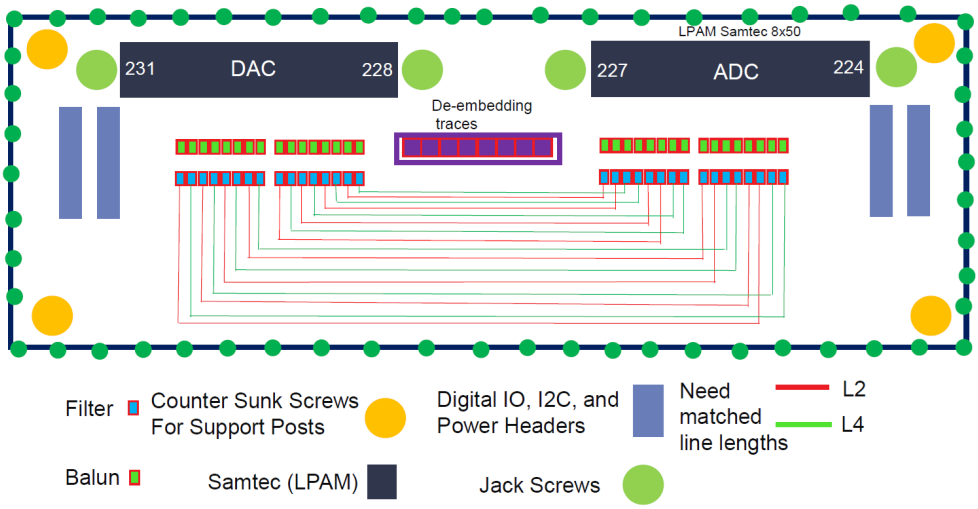
XM755: 16T16R Breakout Add-on Card

Figure 23: **XM755 Block Diagram**



XM650: 16T16R N79 Band Loopback Demo Add-on Card

Figure 24: **XM650 Block Diagram**



Connector

Table 25: **RFMC 2.0 Connector Parameters**

Parameter	Value
Part number	LPAM-50-01.0-L-08-2-K-TR
Data rate	18 Gb/s
Connector type	LP array (.050"/1.27 mm pitch)
I/O pins	8x50
Stack height	.157"/4.00 mm (Mated with LPAF-50-03.0-L-08-2-K-TR)
Make	SAMTEC
Description	Low profile open pin field array, male connector
Data sheet	See the Samtec website

Figure 25: **LPAM-50-01.0-L-08-2-K-TR 3D View**

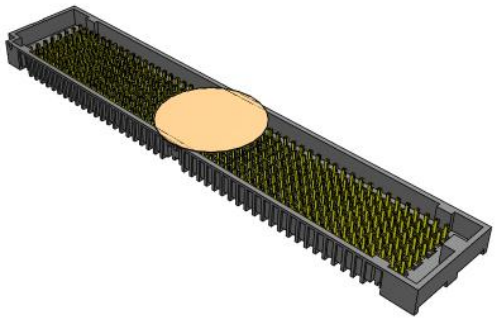
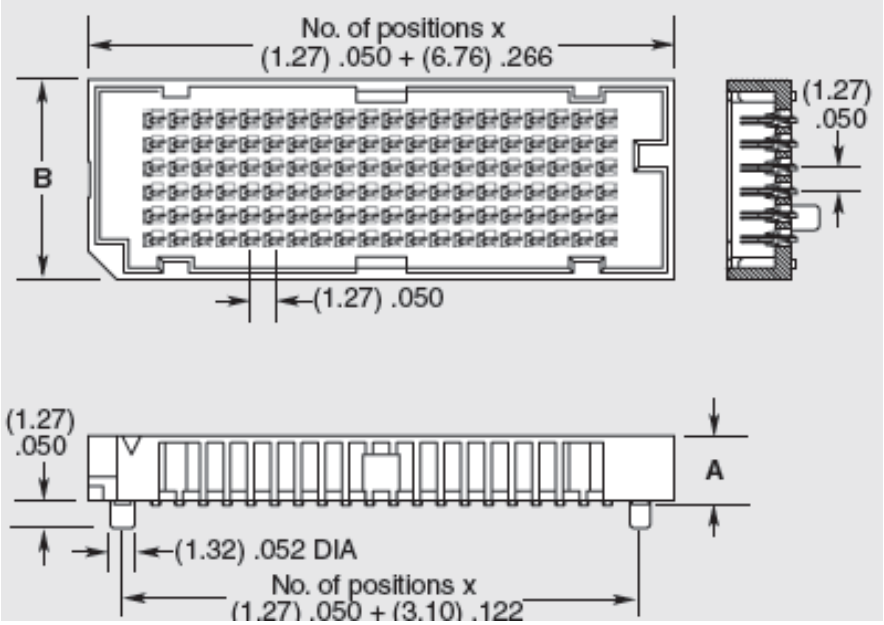


Figure 26: **LPAM Connector Drawing**



XM650/755 Connector Pinouts

The following table lists the connector pinouts for XM650/755.

Table 26: **Connector Pinouts**

J55 DAC								
	A	B	C	D	E	F	G	H
1	GND	DACIO_VADJ	GND	DACIO_VADJ	GND	DAC_AVTT	GND	Spare 1
2	DACIO_00	GND	DACIO_04	GND	DACIO_08	GND	DACIO_12	GND
3	GND	DACIO_02	GND	DACIO_06	GND	DACIO_10	GND	DACIO_14
4	DACIO_01	GND	DACIO_05	GND	DACIO_09	GND	DACIO_13	GND
5	GND	DACIO_03	GND	DACIO_07	GND	DACIO_11	GND	DACIO_15
6	12V	GND	12V	GND	12V	GND	12V	GND
7	GND	12V	GND	12V	GND	12V	GND	12V
8	5v0	GND	5v0	GND	5v0	GND	5v0	GND
9	GND	5v0	GND	5v0	GND	5v0	GND	5v0
10	GND	GND	GND	GND	GND	GND	GND	GND
11	GND	GND	GND	GND	GND	GND	GND	GND
12	GND	GND	GND	GND	GND	GND	GND	GND
13	GND	GND	GND	GND	GND	GND	GND	GND
14	GND	GND	GND	GND	GND	DAC_T1_CH3_N	DAC_T1_CH3_P	GND
15	GND	GND	GND	GND	GND	GND	GND	GND
16	GND	GND	GND	GND	GND	GND	GND	GND
17	GND	GND	GND	GND	GND	GND	GND	GND
18	GND	GND	GND	GND	GND	GND	GND	GND
19	GND	GND	GND	GND	GND	DAC_T1_CH2_N	DAC_T1_CH2_P	GND
21	GND	GND	GND	GND	GND	GND	GND	GND
22	GND	GND	GND	GND	GND	GND	GND	GND

Table 26: **Connector Pinouts** *(cont'd)*

J55 DAC								
23	GND	GND	GND	GND	GND	GND	GND	GND
24	GND	GND	GND	GND	GND	DAC_T1_CH1_N	DAC_T1_CH1_P	GND
25	GND	GND	GND	GND	GND	GND	GND	GND
26	GND	GND	GND	GND	GND	GND	GND	GND
27	GND	GND	GND	GND	GND	GND	GND	GND
28	GND	GND	GND	GND	GND	GND	GND	GND
29	GND	GND	GND	GND	GND	DAC_T1_CH0_N	DAC_T1_CH0_P	GND
30	GND	GND	GND	GND	GND	GND	GND	GND
31	GND	GND	GND	GND	GND	GND	GND	GND
32	GND	GND	GND	GND	GND	GND	GND	GND
33	GND	GND	GND	GND	GND	GND	GND	GND
34	GND	GND	GND	GND	GND	DAC_T0_CH3_N	DAC_T0_CH3_P	GND
35	GND	GND	GND	GND	GND	GND	GND	GND
36	GND	GND	GND	GND	GND	GND	GND	GND
37	GND	GND	GND	GND	GND	GND	GND	GND
38	GND	GND	GND	GND	GND	GND	GND	GND
39	GND	GND	GND	GND	GND	DAC_T0_CH2_N	DAC_T0_CH2_P	GND
40	GND	GND	GND	GND	GND	GND	GND	GND
41	GND	GND	GND	GND	GND	GND	GND	GND
42	GND	GND	GND	GND	GND	GND	GND	GND
43	GND	GND	GND	GND	GND	GND	GND	GND
44	GND	GND	GND	GND	GND	DAC_T0_CH1_N	DAC_T0_CH1_P	GND
45	GND	GND	GND	GND	GND	GND	GND	GND
46	GND	GND	GND	GND	GND	GND	GND	GND
47	GND	GND	GND	GND	GND	GND	GND	GND
48	GND	GND	GND	GND	GND	GND	GND	GND
49	GND	GND	GND	GND	GND	DAC_T0_CH0_N	DAC_T0_CH0_P	GND

Table 26: **Connector Pinouts** *(cont'd)*

J55 DAC								
50	GND	GND	GND	GND	GND	GND	GND	GND

Table 27: **Connector Pinouts**

J49 ADC								
	A	B	C	D	E	F	G	H
1	GND	GND	GND	GND	GND	GND	GND	GND
2	GND	ADC_T2_CH23_N	ADC_T2_CH23_P	GND	GND	GND	GND	GND
3	GND	GND	GND	GND	GND	GND	GND	GND
4	GND	GND	GND	GND	GND	GND	GND	GND
5	GND	GND	GND	GND	GND	ADC_T1_CH3_N	ADC_T1_CH3_P	GND
6	GND	GND	GND	GND	GND	GND	GND	GND
7	GND	ADC_T2_CH01_N	ADC_T2_CH01_P	GND	GND	GND	GND	GND
8	GND	GND	GND	GND	GND	GND	GND	GND
9	GND	GND	GND	GND	GND	GND	GND	GND
10	GND	GND	GND	GND	GND	ADC_T1_CH2_N	ADC_T1_CH2_P	GND
11	GND	GND	GND	GND	GND	GND	GND	GND
12	GND	GND	GND	GND	GND	GND	GND	GND
13	GND	GND	GND	GND	GND	GND	GND	GND
14	GND	GND	GND	GND	GND	GND	GND	GND
15	GND	GND	GND	GND	GND	ADC_T1_CH1_N	ADC_T1_CH1_P	GND
16	GND	GND	GND	GND	GND	GND	GND	GND
17	GND	GND	GND	GND	GND	GND	GND	GND
18	GND	GND	GND	GND	GND	GND	GND	GND

Table 27: **Connector Pinouts** *(cont'd)*

J49 ADC								
19	GND	GND	GND	GND	GND	GND	GND	GND
20	GND	GND	GND	GND	GND	ADC_T1_CH 0_N	ADC_T1_CH 0_P	GND
21	GND	GND	GND	GND	GND	GND	GND	GND
22	GND	GND	GND	GND	GND	GND	GND	GND
23	GND	GND	GND	GND	GND	GND	GND	GND
24	GND	GND	GND	GND	GND	GND	GND	GND
25	GND	GND	GND	GND	GND	ADC_T0_CH 3_N	ADC_T0_CH 3_P	GND
26	GND	GND	GND	GND	GND	GND	GND	GND
27	GND	GND	GND	GND	GND	GND	GND	GND
28	GND	GND	GND	GND	GND	GND	GND	GND
29	GND	GND	GND	GND	GND	GND	GND	GND
30	GND	GND	GND	GND	GND	ADC_T0_CH 2_N	ADC_T0_CH 2_P	GND
31	GND	GND	GND	GND	GND	GND	GND	GND
32	GND	GND	GND	GND	GND	GND	GND	GND
33	GND	GND	GND	GND	GND	GND	GND	GND
34	GND	GND	GND	GND	GND	GND	GND	GND
35	GND	GND	GND	GND	GND	ADC_T0_CH 1_N	ADC_T0_CH 1_P	GND
36	GND	GND	GND	GND	GND	GND	GND	GND
37	GND	GND	GND	GND	GND	GND	GND	GND
38	GND	GND	GND	GND	GND	GND	GND	GND
39	GND	GND	GND	GND	GND	GND	GND	GND
40	GND	GND	GND	GND	GND	ADC_T0_CH 0_N	ADC_T0_CH 0_P	GND
41	GND	GND	GND	GND	GND	GND	GND	GND

Table 27: **Connector Pinouts** *(cont'd)*

J49 ADC								
42	GND	VCM_ADC_T0_CH23	GND	VCM_ADC_T1_CH23	GND	VCM_ADC_T2_CH23	GND	VCM_ADC_T3_CH23
43	VCM_ADC_T0_CH01	GND	VCM_ADC_T1_CH01	GND	VCM_ADC_T2_CH01	GND	VCM_ADC_T3_CH01	GND
44	GND	3V3	GND	3V3	GND	3V3	GND	3V3
45	3V3	GND	3V3	GND	3V3	GND	3V3	GND
46	GND	ADCIO_02	GND	ADCIO_06	GND	ADCIO_10	GND	ADCIO_14
47	ADCIO_00	GND	ADCIO_04	GND	ADCIO_08	GND	ADCIO_12	GND
48	GND	ADCIO_03	GND	ADCIO_07	GND	ADCIO_11	GND	ADCIO_15
49	ADCIO_01	GND	ADCIO_05	GND	ADCIO_09	GND	ADCIO_13	GND
50	GND	I2C_SCL	GND	I2C_SDA	GND	ADCIO_VADJ	GND	ADCIO_VADJ

CoreHC2 Connector Pin Out (XM755 Only)

Figure 27: **ADC: Eight Receiver Signal Lanes Plus Two Observation Lanes**

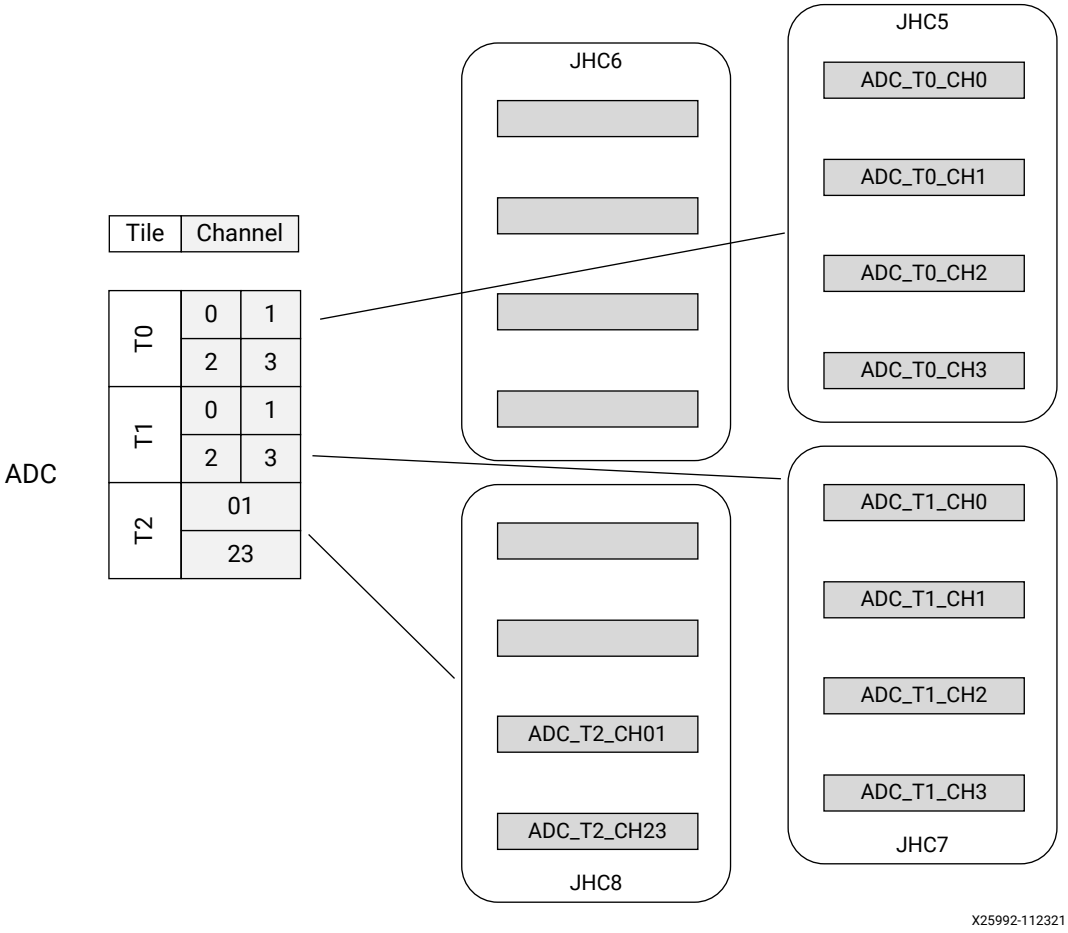
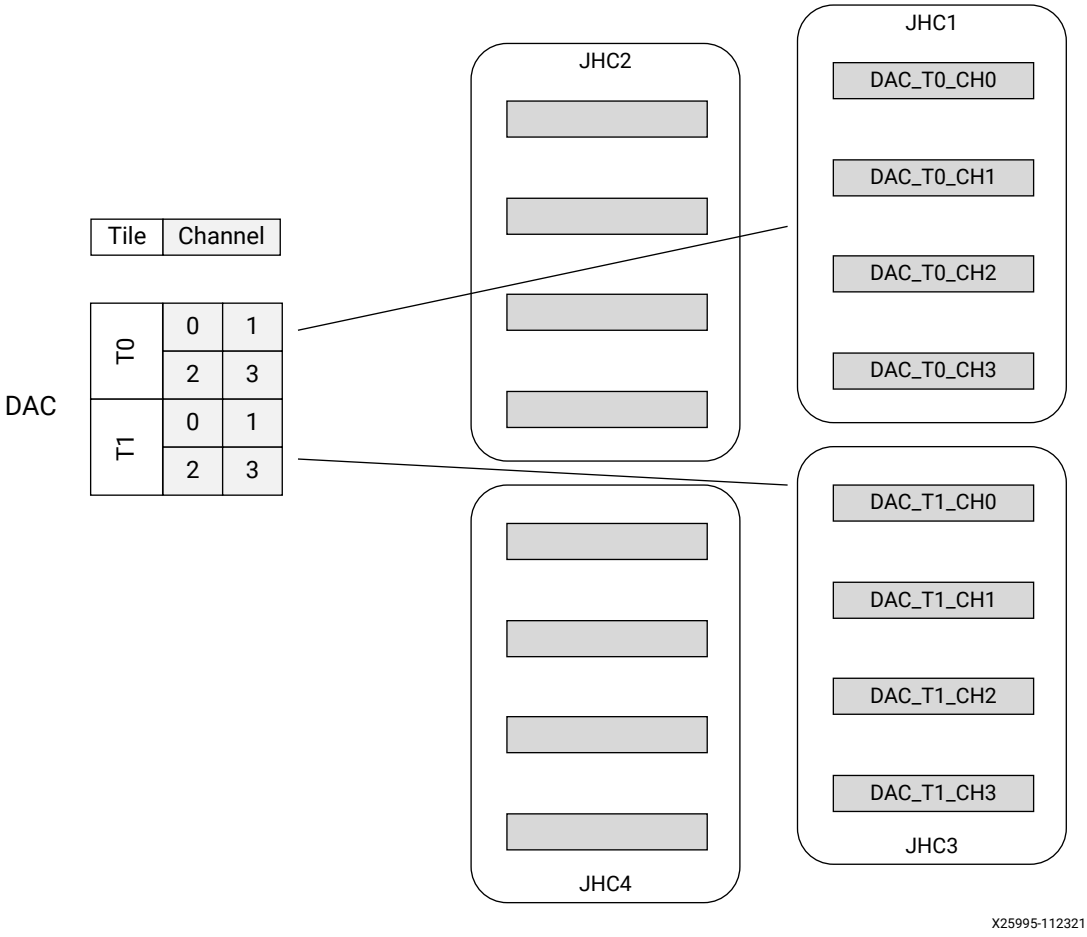


Figure 28: **DAC: Eight Transmitter Signal Lanes**



***Note*:** For ZCU670-specific mapping, see *XM755 to ZCU670 Signal Mapping* (XTP719).

Features

The XM755 balun add-on card uses the 8 x 50 x 2 female LPAM-50-01.0-L-08-2-K-TR connectors and pinout as defined in XM650/755 Connector Pinouts. For signal break-out Carlisle CoreHC2 connectors and cable assemblies are used. Digital I/O and I2C are supported on headers.

The XM755 module features are:

- 16 ADC differential signals to 4 male Carlisle CoreHC2 connector pads
- 16 DACs differential signals to 4 male Carlisle CoreHC2 connector pads
- 2 ADC inputs – compression mount SMAs through low frequency baluns – Minicircuits TCM2-33WX+

- 2 ADC inputs – compression mount SMAs through mid frequency baluns – Anaren BD1631J50100AHF
- 2 ADC inputs – compression mount SMAs through high frequency baluns – Anaren BD3150N50100AHF
- 2 ADC inputs - compression mount SMAs through high freq baluns – Anaren BD60120N50100AHF
- 2 DAC outputs compression mount SMAs through low frequency baluns – Minicircuits TCM2-33WX+
- 2 DAC outputs compression mount SMAs through mid frequency baluns – Anaren BD1631J50100AHF
- 2 DAC outputs compression mount SMAs through high frequency baluns – Anaren BD3150N50100AHF
- 2 DAC outputs - compression mount SMAs through high freq baluns – Anaren BD60120N50100AHF
- 20 DACIO digital I/O pins on a header strip
- 20 ADCIO digital I/O pins on a header strip
- 12V, 5V0, 3V3, VCCADJ DAC, VCCADJ_ADC, DAV_AVTT, and GND, I2C signals access on a header strip

The XM650 balun add-on card demonstrations DAC to ADC loopback with a 16T16R configuration of N79 baluns and filters. There is no external connectivity to the ADC or DAC signals. Digital I/O and I2C are supported on headers.

The XM650 module features are:

- 16 DAC outputs looped back to 16 ADC inputs
- 32 N79 baluns and filters on the card
  - Murata LDB184G7BAAFA065TEMP balun
  - Murata LFB184G70CT6F122 filter
  - B46 or N79 band baluns can be supported with BOM change or rework by customers
- 20 DACIO digital I/O pins on a header strip
- 20 ADCIO digital I/O pins on a header strip
- 12V, 5V0, 3V3, VCCADJ DAC, VCCADJ_ADC, DAV_AVTT, and GND access on a header strip

Board Specifications

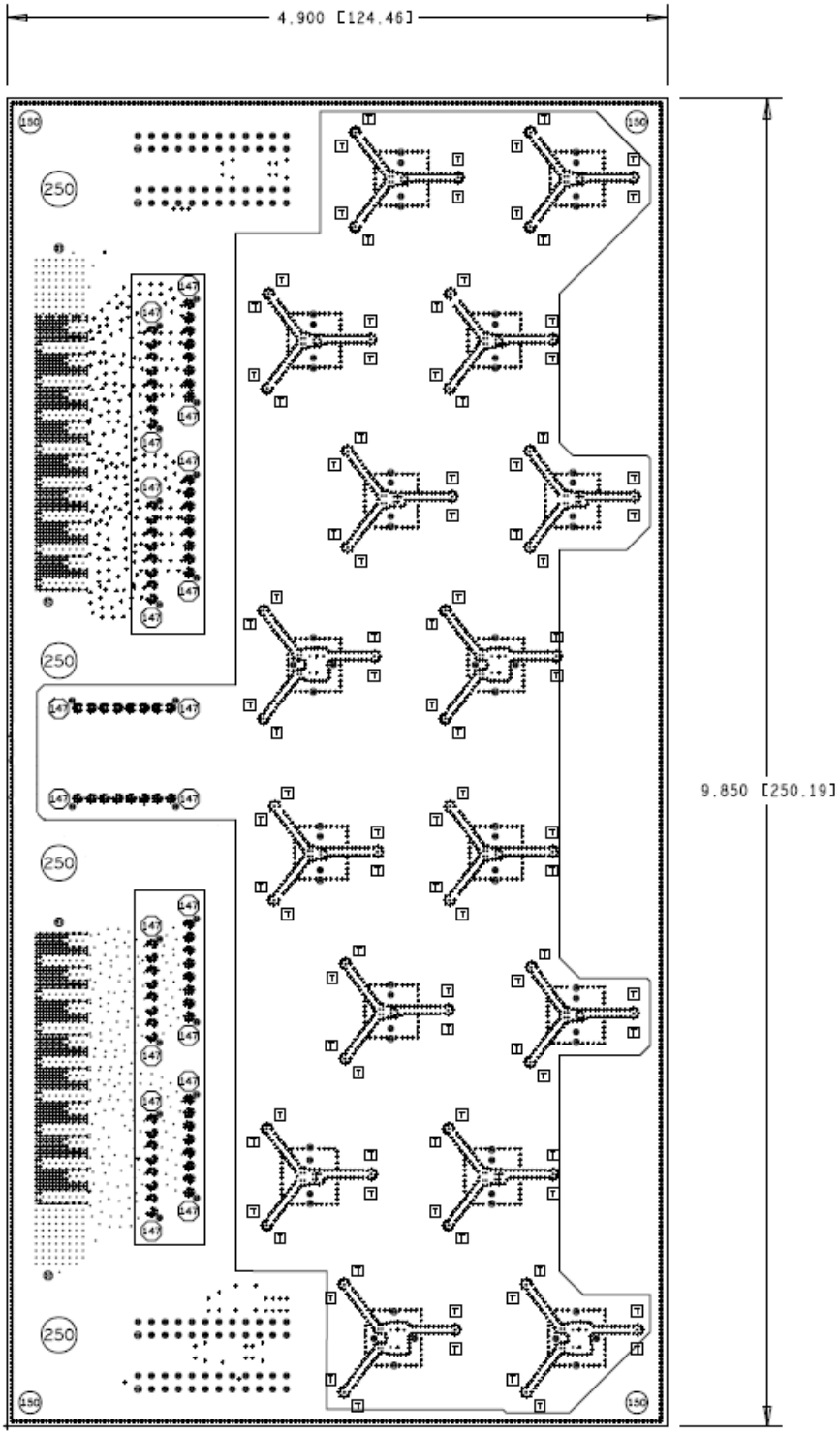
Board Dimensions/Form Factor

When the module is mated with ZCU670 RFMC 2.0 connectors (Samtec LPAF-50-03.0-L-08-2-K-TR), the mated height between the boards will be 4.0 mm. No component is placed on the bottom side of the module.

- **XM755 Dimensions:**

  Length: 9.85" (250.19 mm)
  Width: 4.90" (124.46 mm)
  Thickness: 0.065" (1.651 mm)

Figure 29: **XM755 Board Dimensions**

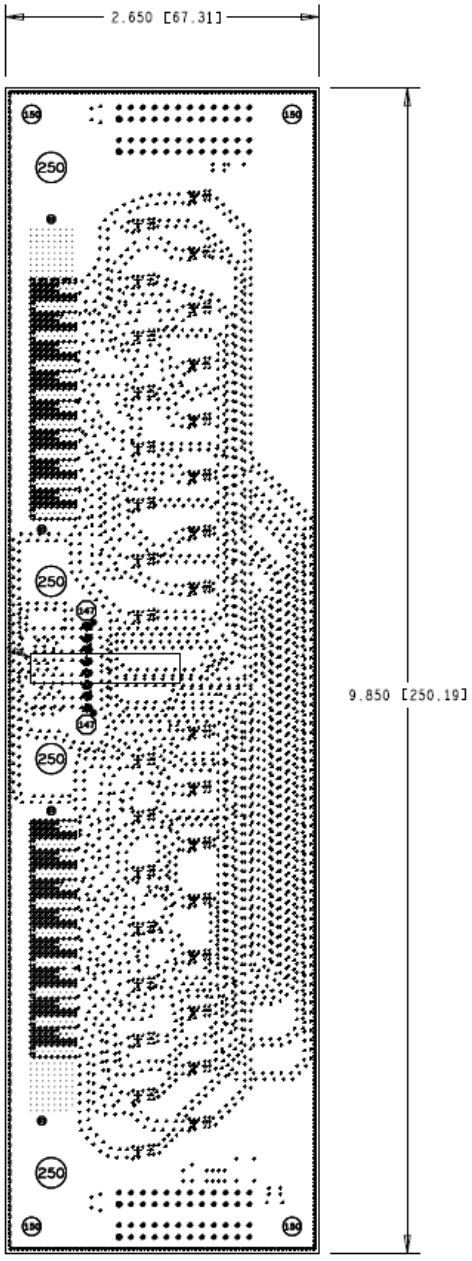


- **XM650 Dimensions:**

  Length: 9.85" (250.19 mm)

Width: 2.65" (67.31 mm)
Thickness: 0.065" (1.651 mm)

Figure 30: **XM650 Board Dimensions**



Mounting Holes/Keepouts

There are four jack screws on the module and two edge standoff, as shown in the figure above. The boards are screwed to the ZCU670 board.

Table 28: **Mounting Screws and Standoff Details**

Parameters	Screw	Standoff
Part number	JSO-0415-01	Keystone 1894
Length	4 mm board stack height	0.625" + rubber bumper
Ordering part number	JSO-0415-01	1894
Description	Jack screw press-in standoff	#4-40 0.625" aluminum standoff
Data sheet	See the Samtec website	–

Functional Description

Cables/SMAs

XM755

Cables: Carlisle Core HC2 8 Channel – Male, 3.5 mm TM40-0157-00

Figure 31: **Carlisle Core HC2 8 Channel–Male Cable**

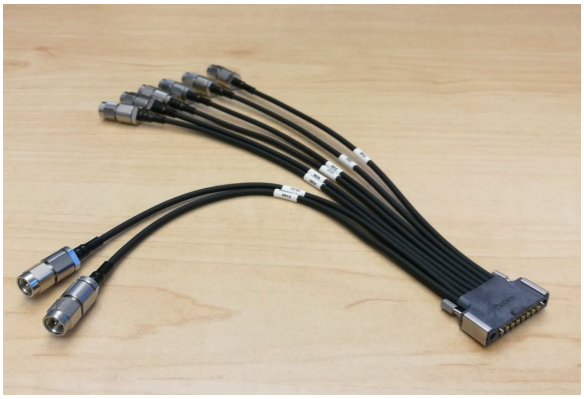
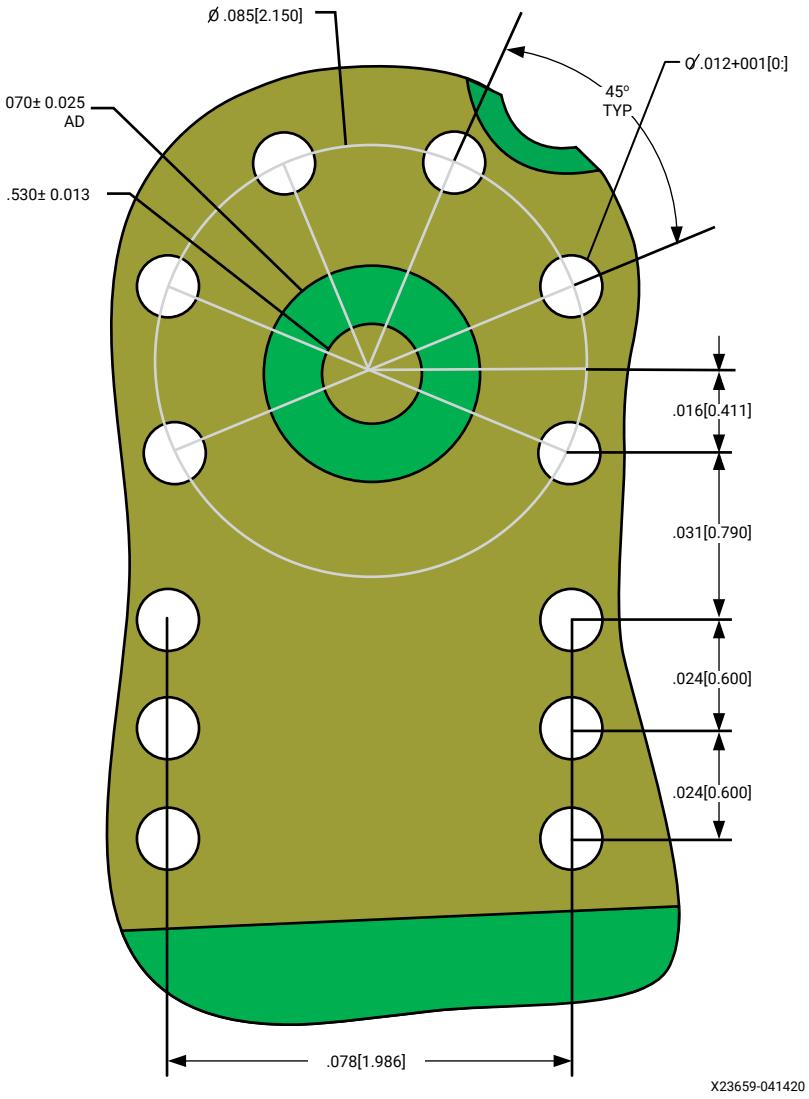


Figure 32: **TM40-0157-00 Landing Pad**



SMAs: Carlisle Compression – Mount SMA, TMB-V5F2-1L1

Figure 33: **TMB-V5F2-1L1 SMA Drawing**

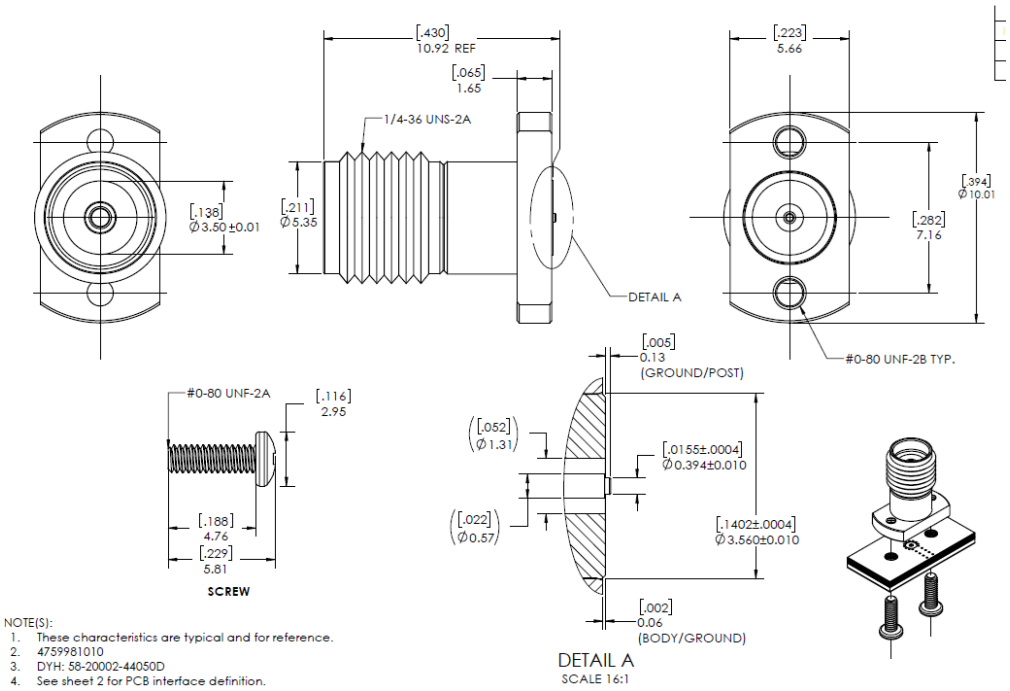


Figure 34: **SMA to SMA Cable: Carlisle TM40-0159-00 6"**

Balun/Filter

XM755

Table 29: **Low Frequency Balun Part Number**

Parameter	Value
Part number	TCM2-33WX+
Manufacturer	Minicircuits
Order P/N	TCM2-33WX+
Vendor	Minicircuits
Description	10 to 3000 MHz RF transformer
Data sheet	See the Minicircuits website

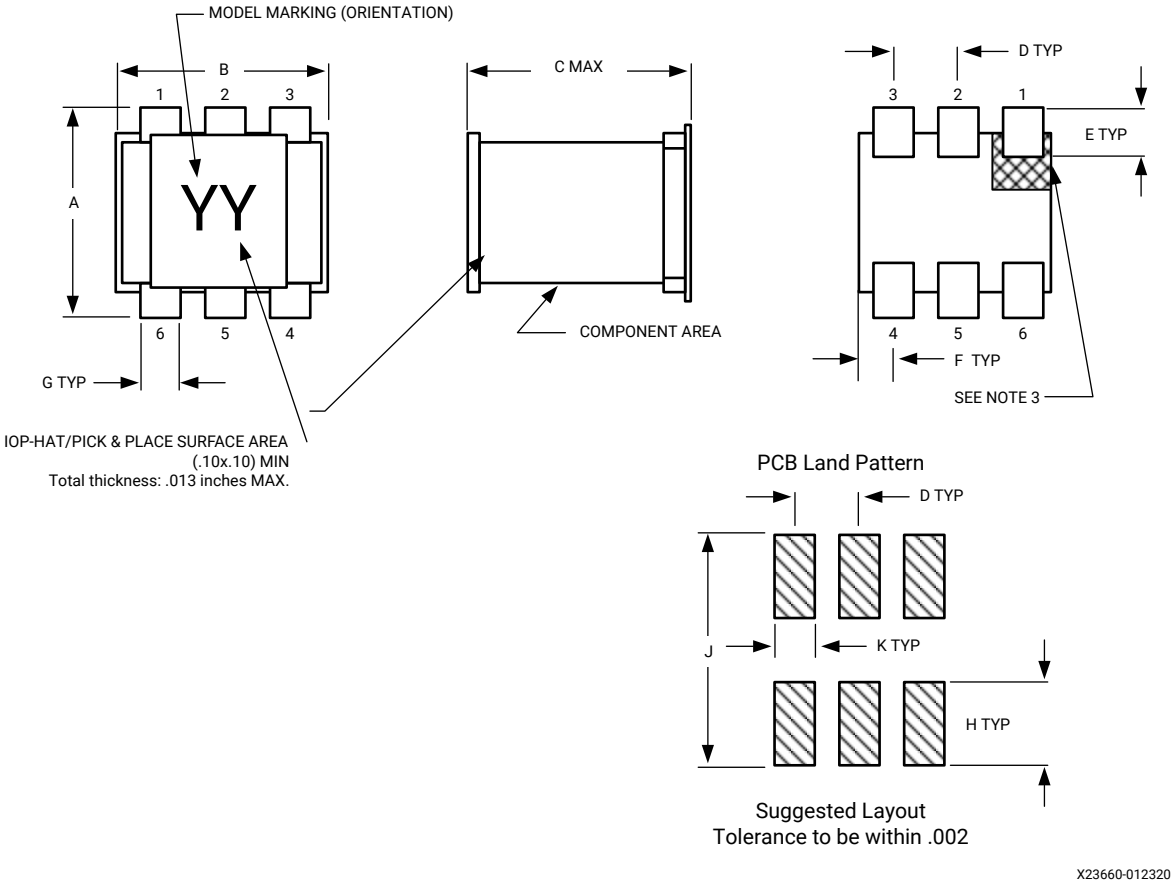
Table 30: **Low Frequency Balun Specifications - Electrical Specifications at 25°**

Parameter	Frequency (MHz)	Minimum	Type	Maximum	Unit
Impedance Ratio (secondary/primary			2		
Frequency range		10	—	3000	MHz
Insertion loss[1]	10-3000	—	1.5	3.0	dB
Amplitude unbalance	10-3000	—	0.7	—	dB
Phase unbalance	10-3000	—	4	—	Degree

Notes:

1. Insertion loss is reference to mid-band loss, 0.8 dB typ.

Figure 35: **Low Frequency Balun Drawing**



The following table lists the outline dimensions for the figure above.

Table 31: **Outline Dimensions (mm)**

A	B	C	D	E	F	G	H	J	K	Wt
0.160	0.150	0.160	0.050	0.040	0.025	0.028	0.065	0.190	0.030	grams
4.06	3.81	4.06	1.27	1.02	0.64	0.71	1.65	4.83	0.76	0.15

Table 32: **Medium Frequency Balun Part Number**

Parameter	Value
Part number	BD1631J50100AHF
Manufacturer	Anaren
Order P/N	1173-1059-2-ND
Vendor	Digikey
Description	Balun 1.6 GHz-3.1 GHz 50/100 0805
Data sheet	See the Anaren website

Figure 36: **Medium Frequency Balun Specifications**

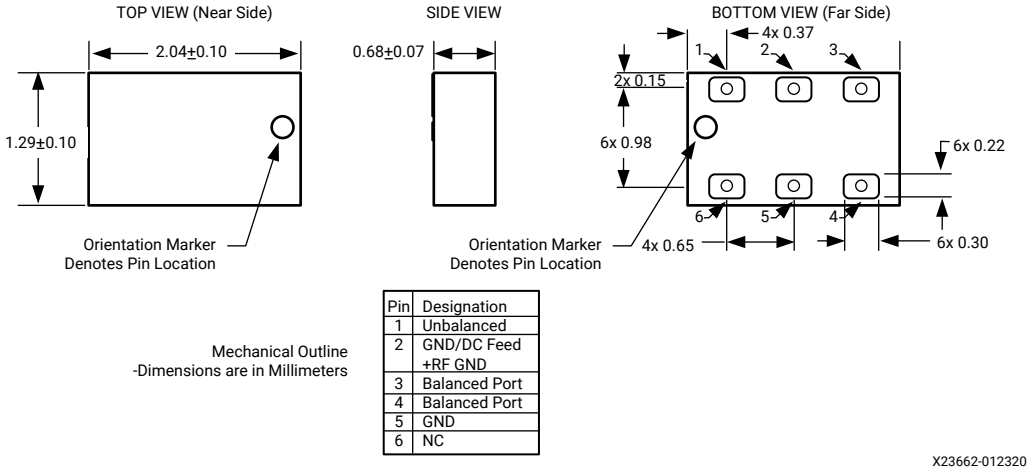
Detailed Electrical Specifications*: Specifications subject to change without notice.

Features:
- 1.6 – 3.1 GHz
- 0.7mm Height Profile
- 50 Ohm to 2 x 50 Ohm
- 802.11 b & g +n Compliant
- Low Insertion Loss
- DCS, PCS & UMTS Compliant
- Input to Output DC Isolation
- Surface Mountable
- Tape & Reel
- Non-conductive Surface
- RoHS Compliant
- Halogen Free

Parameter	ROOM (25°C) Min.	Typ.	Max	Min.	Typ.	Max	Unit
Frequency	2.0		2.5	1.6		3.1	GHz
Unbalanced Port Imp.		50			50		Ω
Balanced Port Imp.**		100			100		Ω
Return Loss	14	17		10	13		dB
Insertion Loss***		0.6	0.8		0.7	1.0	dB
Amplitude Balance		0.15	0.6		0.7	1.0	dB
Phase Balance		2.3	4.8		2.3	4.8	Degrees
Power Handling @85C			0.8			0.8	Watts
Power Handling @100C			0.55			0.55	Watts
Power Handling @105C			0.48			0.48	Watts
Operating Temperature	-55		+105	-55		+105	ºC

* Insertion Loss stated at room temperature (Insertion Loss is approximately 0.1 dB higher at +85 ºC)

Figure 37: **Medium Frequency Balun Drawing**



Pin	Designation
1	Unbalanced
2	GND/DC Feed +RF GND
3	Balanced Port
4	Balanced Port
5	GND
6	NC

Table 33: **High Frequency Balun (4-5 GHz) Part Number**

Parameter	Value
Part number	BD3150N50100AHF
Manufacturer	Anaren
Order P/N	1173-1069-2-ND
Vendor	Digikey
Description	Balun 3.1 GHz-5 GHz 50/100 0404
Data sheet	See the Anaren website

Figure 38: **High Frequency Balun Specifications**

Detailed Electrical Specifications: Specifications subject to change without notice.

Features:

- 3100 – 5000 MHz
- 0.57mm Height Profile
- 50 Ohm to 2 x 50 Ohm
- Low Insertion Loss
- UWB & MMDS
- Surface Mountable
- Tape & Reel
- Non-conductive Surface
- RoHS Compliant
- Halogen Free

Parameter	ROOM (25°C) Min.	Typ.	Max	Min.	Typ.	Max	Unit
Frequency	3100		5000	5000		7000	MHz
Unbalanced Port Impedance		50			50		Ω
Balanced Port Impedance		100			100		Ω
Return Loss	13	15		10	14		dB
Insertion Loss*		0.7	0.9		0.7	0.9	dB
Amplitude Balance		0.8	1.5		0.8	1.3	dB
Phase Balance		3	7		15	20	Degrees
CMRR		26			17		dB
Power Handling @85C			1.0			1.0	Watts
Power Handling @105C			0.6			0.6	Watts
Operating Temperature	-55		+105	-55		+105	ºC

* Insertion Loss stated at room temperature (Insertion Loss is approximately 0.1 dB higher at +85 °C)

Figure 39: **High Frequency Balun Drawing**

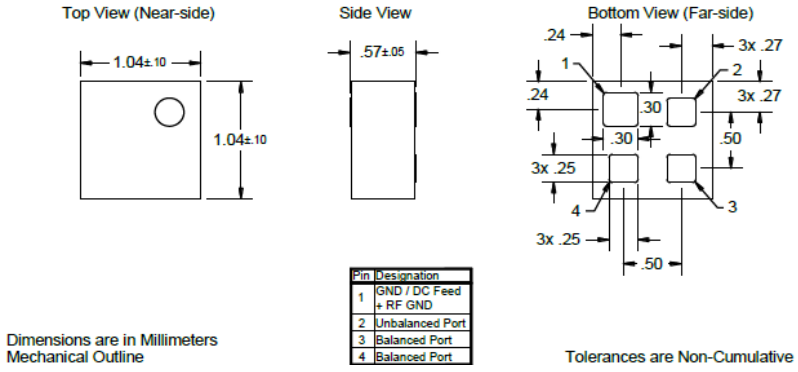


Table 34: **High Frequency Balun (6-12 GHz) Part Number**

Parameter	Value
Part number	BD60120N50100AHF
Manufacturer	Anaren
Order P/N	BD60120N50100AHF-ND
Vendor	Digikey
Description	RF balun 5.9 GHz – 11.7 GHz 50/100Ω 0404
Data sheet	See the Anaren website

Figure 40: **High Frequency Balun Specifications**

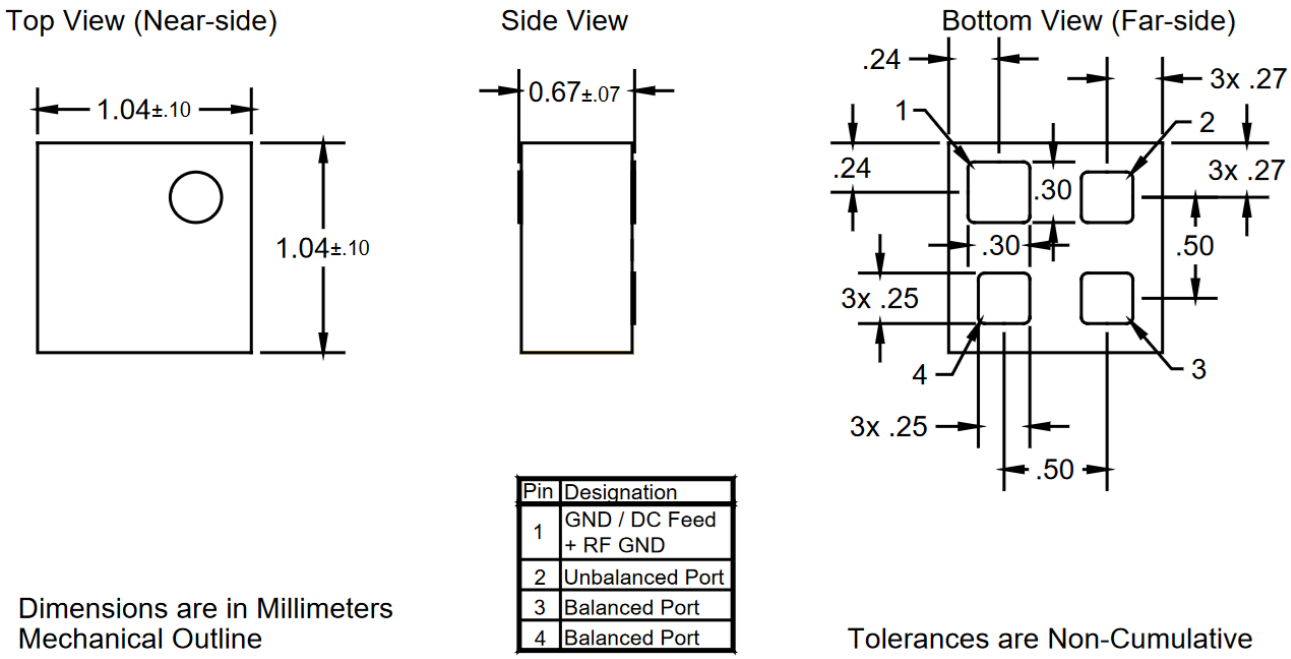
Detailed Electrical Specifications: Specifications subject to change without notice.

Features:
- 5.9 – 11.7 GHz
- Thin Height Profile
- Ultra Low Insertion Loss
- Surface Mountable
- Tape & Reel
- RoHS Compliant
- Halogen Free
- -55°C to 140°C

			ROOM (25˚C)									
	Frequency (GHz)	Port Impedance		Return loss (dB)		Insertion loss (dB)		Amplitude Balance (dB)		Phase Balance (deg)		CMRR (dB)	Power Handling (Watts)
		Unbal.	Bal.	Typ.	Min.	Typ.	Max.	Typ.	Min	Typ.	Max	Typ.	Max.
	5.9-8.5	50	100	22	14	0.4	0.7	0.8	1.3	9	12	21	1@85°C 0.6@105°C
	10.0-11.7	50	100	25	14	0.6	0.9	0.9	1.6	7	13	24	1@85°C 0.6@105°C

* Insertion Loss stated at room temperature (Insertion Loss is approximately 0.1 dB higher at +85 °C)

Figure 41: **High Frequency Balun Drawing**



Pin	Designation
1	GND / DC Feed + RF GND
2	Unbalanced Port
3	Balanced Port
4	Balanced Port

Dimensions are in Millimeters
Mechanical Outline

Tolerances are Non-Cumulative

RF Cages

Table 35: **RF Cages**

Parameter	Value
Part number	LT-7925
Manufacturer	Leader Tech
Order P/N	LT-7925
Vendor	Leader Tech
Description	EMI cage

Table 35: **RF Cages** *(cont'd)*

Parameter	Value
Data sheet	See the Leader Tech website

XM650

Table 36: **N79 Band Pass Filter**

Parameter	Value
Part number	LFB184G70CT6F122TEMP
Manufacturer	Murata
Order P/N	LFB184G70CT6F122TEMP
Vendor	Murata
Description	Band pass filter 4.4 GHz~5 GHz
Data sheet	See the Murata website

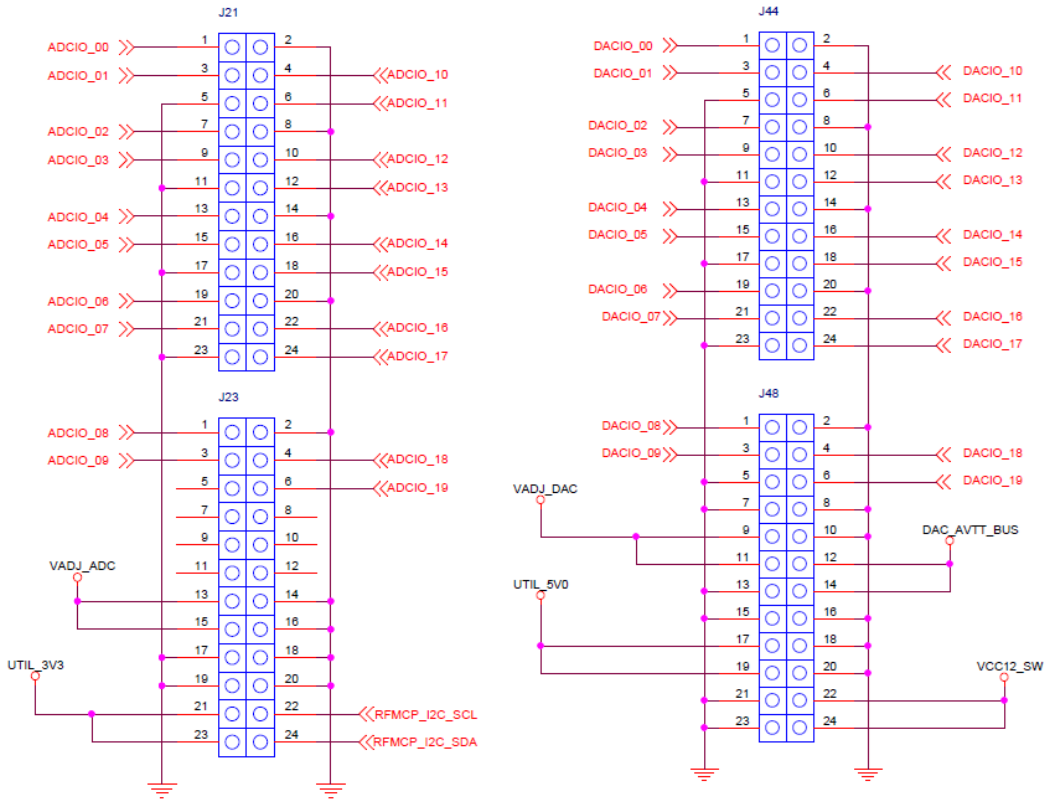
Table 37: **N79 Balun**

Parameter	Value
Part number	LDB184G7BAAFA065TEMP
Manufacturer	Murata
Order P/N	LDB184G7BAAFA065TEMP
Vendor	Murata
Description	Chip multilayer Balun 4.4 GHz~5 GHz
Data sheet	See the Murata website

Header

There are a total of 20 DACIO and 20 ADCIO digital I/O pins on the header strips.

Figure 42: **High ADCIO and DACIO Digital I/O Header Pins**



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Appendix E

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

ZCU670 Evaluation Kit— Master Answer Record 33801

These documents provide supplemental material useful with this guide:

1. *Zynq UltraScale+ RFSoC Data Sheet: Overview* (DS889)
2. *Zynq UltraScale+ RFSoC DFE Data Sheet: Overview* (DS883)
3. *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
4. *Zynq UltraScale+ Device Technical Reference Manual* (UG1085)
5. *UltraScale Architecture PCB Design User Guide* (UG583)
6. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
7. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
8. *Vivado Design Suite User Guide: Using Constraints* (UG903)
9. *Tera Term Terminal Emulator Installation Guide* (UG1036)
10. *UltraScale Architecture System Monitor User Guide* (UG580)
11. *ZCU670 System Controller Tutorial* (XTP698)
12. *ZCU670 Software Install and Board Setup Tutorial* (XTP699)
13. Micron Technology (MTA4ATF51264HZ-2G6E1, MT40A512M16JY-075E, MT25QU02GCBB8E12-0SIT data sheets)
14. Standard Microsystems Corporation (SMSC) (USB3320 data sheet)
15. SanDisk Corporation
16. SD Association
17. Skyworks Solutions, Inc.
18. Silicon Labs (SI570, SI5341B, SI5382A)
19. Texas Instruments (TCA9548A, PCA9544A, TCA6416A, DP83867, MSP430FS342, TPS51200DRCT)
20. PCI-SIG
21. Samtec, Inc. (SEAF, LPAF series connectors)
22. VITA FMC Marketing Alliance (FPGA Mezzanine Card (FMC) VITA 57.1, 57.4 specifications)
23. Maxim Integrated Circuits (MAX16025TE+, MAX6643)
24. Infineon Integrated Circuits (IR35215, IRPS5401, IR38164, IR3889)
25. Monolithic Power Systems (MPM3683, MPM3833)
26. Future Technology Devices International Ltd. (FT4232HL)
27. SNIA Technology Affiliates (SFF-8402, SFF-8432)
28. Nexperia/NXP Semiconductors (IP4856CX25, SC18IS602)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
03/30/2022 Version 1.0	
Initial release.	N/A

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