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# Zynq 7010 / 7020 SOM (System-On Module)



# Hardware User Guide

Version 1.4  
2/3/2015

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# 1 Introduction

The PicoZed Z7010 / Z7020 SOM (System-On Module) is a low cost System-On-Module targeted for broad use in many applications. The features provided by the PicoZed System-On-Module consist of:

- Xilinx XC7Z010-1CLGG400 or Xilinx XC7Z020-1CLG400 AP SOC
  - Primary configuration = QSPI Flash
  - Auxiliary configuration option
    - eMMC (Second Stage Bootloader)
  - Auxiliary primary configuration options via End User Carrier Card
    - JTAG
    - microSD Card or SD Card
- Memory
  - 1 GB DDR3 (x32)
  - 128 Mb QSPI Flash
  - 4GB eMMC
- Interfaces
  - 10/100/1000 Ethernet PHY (Connector required on End User Carrier Card)
  - USB 2.0 OTG PHY (Connector required on End User Carrier Card)
  - Three 100-pin Micro Headers
- On-board Oscillator
  - 33.333 MHz
- Power
  - High-efficiency regulators for VCCINT, VCCPINT, VCCBRAM, VCCAUX, VCCPAUX, VCCPLL, VCCO\_0, VCCO\_DDR, VCCO\_MIO1 and VCCO\_MIO0
  - VCCO\_34, VCCO\_35, and VCCO\_13 are powered from Expansion Card via Three 100-pin Micro Headers
- Software
  - Vivado Design Suite
    - Download from [www.xilinx.com/support/download.html](http://www.xilinx.com/support/download.html)
    - Request a free DVD from [www.xilinx.com/onlinestore/dvd\\_fulfillment\\_request.htm](http://www.xilinx.com/onlinestore/dvd_fulfillment_request.htm)

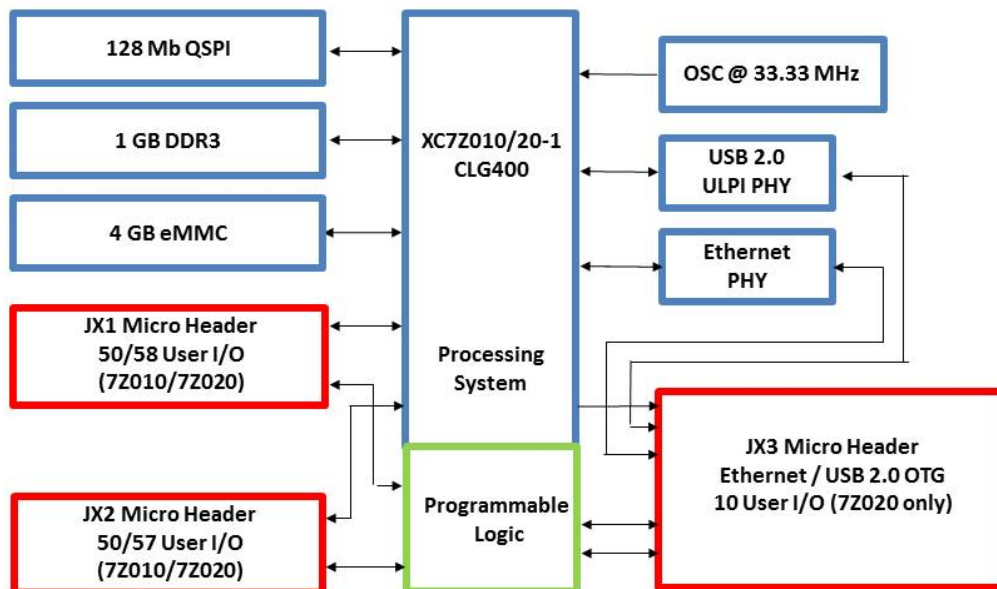


Figure 1 – PicoZed 7010/7020 Block Diagram

## 2 Functional Description

### 2.1 All Programmable SoC

The PicoZed 7010/7020 includes a Xilinx Zynq XC7Z010-1CLG400 or Zynq XC7Z020-1CLG400 AP SoC. The PicoZed 7010/7020 is available in both commercial and industrial temperature grade options.

### 2.2 Memory

Zynq contains a hardened PS memory interface unit. The memory interface unit includes a dynamic memory controller and static memory interface modules. PicoZed 7010/7020 takes advantage of these interfaces to provide system RAM as well as two different non-volatile memory sources.

#### 2.2.1 DDR3L

PicoZed 7010/7020 includes two Micron MT41K256M16HA-125:E DDR3L memory components creating a 256M x 32-bit interface, totaling 1 GB of random access memory. The DDR3L memory is connected to the hard memory controller in the PS of the Zynq AP SoC. The PS incorporates both the DDR controller and the associated PHY, including its own set of dedicated I/Os.

Speed of up to 1,066 MT/s for DDR3L is supported.

The DDR3L interface is designed to use 1.35V SSTL-compatible inputs by default. There is an option to support 1.5V capable DDR3 devices via a resistor change on the PicoZed 7010/7020. This option is provided as a note on the PicoZed 7010/7020 schematics.

DDR3L Termination is utilized on the PicoZed 7010/7020 and configured for fly-by routing topology. Additionally the board trace lengths are matched, compensating for the XC7Z010-CLG400 internal package flight times, to meet the requirements listed in the Zynq-7000 AP SoC PCB Design and Pin Planning Guide (UG933).

All single-ended signals are routed with 40 ohm trace impedance. DCI resistors (VRP/VRN), as well as differential clocks, are set to 80 ohms. DDR3-CKE0 is terminated through 40 ohms to VTT. DDR3-ODT has the same 40 ohm to VTT termination. There was a discrepancy in the original Xilinx documentation regarding whether DDR3-RESET# should have 40 ohms to VTT or 4.7K ohm to GND, which is why a resistor jumper circuit was designed in to give both options. Xilinx has since clarified that 4.7K-ohm to GND is the correct configuration for DDR3-RESET#. The default position of the resistor jumper on production units is 1-2 (GND).

Each DDR3L chip has its own 240-ohm pull-down on ZQ. Note DDR-VREF is not the same as DDR-VTT.

**Table 1 – DDR3L Connections**

Signal Name	Description	Zynq AP SOC pin	DDR3 pin
DDR_CK_P	Differential clock output	L2	J7
DDR_CK_N	Differential clock output	M2	K7
DDR_CKE	Clock enable	N3	K9
DDR_CS_B	Chip select	N1	L2
DDR_RAS_B	RAS row address select	P4	J3
DDR_CAS_B	RAS column address select	P5	K3
DDR_WE_B	Write enable	M5	L3
DDR_BA[2:0]	Bank address	PS_DDR_BA[2:0]	BA[2:0]
DDR_A[14:0]	Address	PS_DDR_A[14:0]	A[14:0]
DDR_ODT	Output dynamic termination	N5	K1
DDR_RESET_B	Reset	B4	T2
DDR_DQ[31:0]	I/O Data	PS_DDR_DQ[31:0]	DDR3_DQ[15:0] x2
DDR_DM[3:0]	Data mask	PS_DDR_DM[3:0]	LDM/UDM x2
DDR_DQS_P[3:0]	I/O Differential data strobe	PS_DDR_DQS_P[3:0]	UDQS/LDQS x2
DDR_DQS_N[3:0]	I/O Differential data strobe	PS_DDR_DQS_N[3:0]	UDQS#/LDQS# x2
DDR_VRP	I/O Used to calibrate input termination	H5	N/A
DDR_VRN	I/O Used to calibrate input termination	G5	N/A
DDR_VREF[1:0]	I/O Reference voltage	P6 / H6	VTTREF

### 2.2.2 Quad-SPI Flash

PicoZed 7010/7020 features a 4-bit SPI (quad-SPI) serial NOR flash. The Spansion S25FL128S (S25FL128SAGBHIA00) is used on this board. The Multi-I/O SPI Flash memory is used to provide non-volatile boot, application code, and data storage. It can be used to initialize the PS subsystem as well as configure the PL subsystem (bitstream). Spansion provides Spansion Flash File System (FFS) for use after booting the Zynq-7000 AP SoC.

The relevant device attributes are:

- 128Mbit
  - Optional densities are available via customization
- x1, x2, and x4 support
- Speeds up to 104 MHz, supporting Zynq configuration rates @ 100 MHz
  - In Quad-SPI mode, this translates to 400Mbs
- Powered from 3.3V

The Quad-SPI Flash connects to the Zynq PS QSPI interface. This requires connection to specific pins in MIO Bank 0/500, specifically MIO[1:6,8] as outlined in the Zynq TRM. Quad-SPI feedback mode is used, thus `qspi_sclk_fb_out/MIO[8]` is connected to a 20K pull-up resistor to 3.3V and nothing else. This allows a QSPI clock frequency greater than `FQSPICLK2`. The 20K pull-up straps `VMODE[1]`, setting the Bank 1 Voltage to 1.8V.

**Table 2 – Quad-SPI Flash Pin Assignment and Definitions**

Signal Name	Description	Zynq Pin	MIO	Quad-SPI Pin
CS	Chip Select	A7 (MIO Bank 0/500)	1	C2
DQ0	Data0	B8 (MIO Bank 0/500)	2	D3
DQ1	Data1	D6 (MIO Bank 0/500)	3	D2
DQ2	Data2	B7 (MIO Bank 0/500)	4	C4
DQ3	Data3	A6 (MIO Bank 0/500)	5	D4
SCK	Serial Data Clock	A5 (MIO Bank 0/500)	6	B2
FB Clock	QSPI Feedback	D5 (MIO Bank 0/500)	8	N/A

**Note:** The QSPI data and clock pins are shared with the `VMODE` set resistors and the `BOOT MODE` select jumper JT4 and switch SW1.

### 2.2.3 eMMC (Multi-Media Controller)

PicoZed 7010/7020 features a Micron MTFC4GMDEA-4M IT eMMC Multi Media Controller and NAND Flash IC. The eMMC is used to provide non-volatile user data storage.

The relevant device attributes are:

- 4GB (default)
- Optional densities available via customization
- Industrial temperature range (-40 to +85 C)
- 4-bit data interface
- 52MHz max clock speed

**Table 3 – eMMC Pin Assignment and Definitions**

Signal Name	Description	Zynq Pin	MIO	eMMC Pin
EMMC_IO0	Data 0	E9 (MIO Bank 0/500)	10	H3
EMMC_CMD	Command	C6 (MIO Bank 0/500)	11	W5
EMMC_CLK	Clock	D9 (MIO Bank 0/500)	12	W6
EMMC_IO1	Data 1	E8 (MIO Bank 0/500)	13	H4
EMMC_IO2	Data 2	C5 (MIO Bank 0/500)	14	H5
EMMC_IO3	Data 3	C8 (MIO Bank 0/500)	15	J2

The eMMC connects to the Zynq PS via six signals by way of two 4-bit MUXs.

The eMMC I/O is multiplexed with direct connections to the Zynq MIO PS\_MIO[0, 15:9] pins allowing the user to use the JX2 MIO[0, 15:9] pins as standard I/O or have access to the eMMC I/O. The Zynq PS\_MIO0 pin can be used as the multiplexer select control signal to give the user software control to select either interface in real time. Software control and hardware control of the multiplexer select line is discussed in further detail below.

#### Software Control of Multiplexer Select

If the user wishes to use software to control the multiplexer select the Zynq PS\_MIO0 pin is utilized. When software controls the multiplexer select signal, the running application can select either eMMC accesses for the Zynq or standard MIO interfaces via the JX2 connector. When using software to control the multiplexer select signal, the JX2 MIO interface becomes limited to 7 I/O pins, MIO[15:9] since the Zynq PS\_MIO0 pin is being used to control the multiplexer select signal. This option offers the user the most flexibility to connect either interface to the Zynq when needed by the application.

*Software control of the Multiplexer Select signal is the default setting for the PicoZed 7010/7020 System-On-Module from the factory, and is enabled by the jumper resistor position at JT1 position 1-2.*

In position 1-2 the Zynq PS\_MIO0 pin is connected to the multiplexer select pins of U1 and U2.

In position 2-3 the Zynq PS\_MIO0 pin is connected to the JX2 MIO0 pin via the multiplexer channel 4 on device U2.

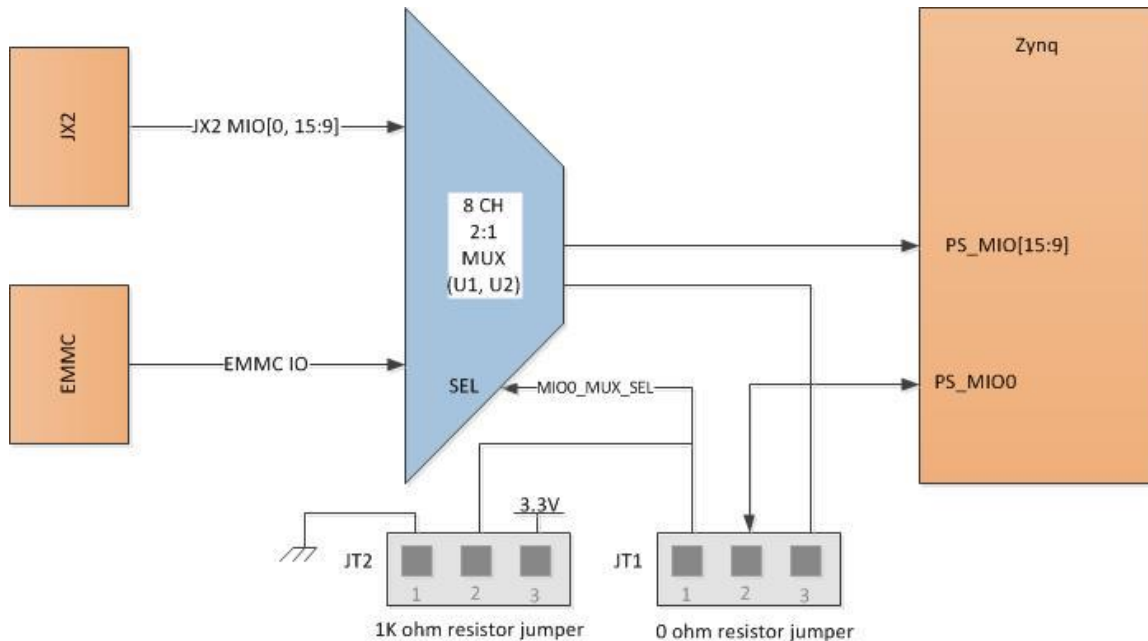
#### Hardware Control of Multiplexer Select (Interface Strapping)

Another user option available is to “hard-wire” one of the two interfaces, JX2 MIO[0,15:9] or eMMC I/O to the Zynq PS\_MIO[0,15:9] pins. This can be done by modifying the resistor jumper position at JT2, which sets the desired interface and JT1, which controls the use of PS\_MIO0.

*The default resistor jumper position for JT2 is 1-2, which selects the eMMC as the selected interface.*

If JT2 resistor jumper position is changed to position 2-3, the JX2 MIO pins become selected by the multiplexers. In this case, it is best to also change the JT1 jumper position to 2-3 to ensure that a full 8-bit peripheral can be connected through the JX2 MIO interface if so desired.

The diagram below shows how the eMMC and JX2 MIO signals are connected to the Zynq via the multiplexer ICs U1 and U2.



**Figure 2 – eMMC / JX2 MIO Multiplexer Block Diagram**

### 2.3 USB 2.0 OTG

Zynq contains a hardened PS USB 2.0 controller. PicoZed 7010/7020 takes advantage of the USB 2.0 controller to provide USB 2.0 On-The-Go signaling to the JX3 connector.

PicoZed 7010/7020 implements one of the two available PS USB 2.0 interfaces. An external PHY with an 8-bit ULPI interface is implemented. A SMSC USB3320 Standalone USB Transceiver Chip is used as the PHY. The PHY features a complete HS-USB Physical Front-End supporting speeds of up to 480Mbs. VDDIO for this device can be 1.8V or 3.3V, and on the PicoZed 7010/7020 is powered at 1.8V. The PHY is connected to MIO Bank 1/501, which is also powered at 1.8V. This is critical since a level translator cannot be used as it would impact the tight ULPI timing required between the PHY and the Zynq device.

Additionally the USB chip must clock the ULPI interface which requires a 24 MHz crystal or oscillator (configured as ULPI Output Clock Mode). On the PicoZed 7010/7020, the 24 MHz oscillator is an Abracon ASDMB CMOS oscillator, ASDMB-24.000MHZ-LC-T.

The USB connector is not populated on the PicoZed 7010/7020 System-on-Module and is designed to have the USB connector reside on the mating carrier card. The four USB connector signals (USB\_P, USB\_N, USB\_ID and USB\_OTG\_CPEN) are connected to the JX3 Micro Header. The table below shows the connections of these four signals at JX3.

**Table 4 – USB 2.0 JX3 Pin Assignments**

Signal Name	JX3 Pin
USB_OTG_N	69
USB_OTG_P	67
USB_ID	63
USB_OTG_CPEN	70

If using the Avnet PicoZed FMC Carrier Card as the mating carrier card, a Micro-AB connector provided by FCI is used. The FCI part number is 10104111-0001LF.

The usb0 peripheral is used on the PS, connected through MIO[28-39] in MIO Bank 1/501. The USB Reset signal is connected to MIO[7]. Signal PS\_MIO7 is a 3.3V signal. It is AND-ed with the power-on reset (PG\_MODULE) signal and then level shifted to 1.8V through a TI TXS0102 level translator before connecting to the USB3320 Pin 27 RESET.

PicoZed 7010/7020 is configured such that either Host Mode (OTG) or Device Mode can be used depending on the circuitry of the carrier card. With a standard connection to a baseboard (no power supply used to provide USB power to the connector) the device will operate in Device Mode. Using the USB\_OTG\_CPEN signal on JX3 allows the user to control an external power source for USB VBUS on the carrier card. Other considerations need to be made to accommodate Host Mode. Refer to the Avnet PicoZed FMC Carrier Card design for an example design for configuring the carrier card for either Host Mode or Device Mode.

**Table 5 – USB 2.0 Pin Assignment and Definitions**

Signal Name	Description	Zynq Bank	MIO	SMSC 3320 Pin
Data[7:0]	USB Data lines	MIO Bank 1/501	28:39	Data[7:0]
CLKOUT	USB Clock	MIO Bank 1/501		1
DIR	ULPI DIR output signal	MIO Bank 1/501		31
STP	ULPI STP input signal	MIO Bank 1/501		29
NXT	ULPI NXT output signal	MIO Bank 1/501		2
REFSEL[2:0]	USB Chip Select	N/C	N/C	8,11,14
DP	DP pin of USB Connector			18
DM	DM pin of USB Connector			19
ID	Identification pin of the USB connector			23
RESET_B	Reset	MIO Bank 1/501	7**	27**

\*\* Connected through AND-gate with PG\_MODULE through level translator (TI TXS0102DQE).

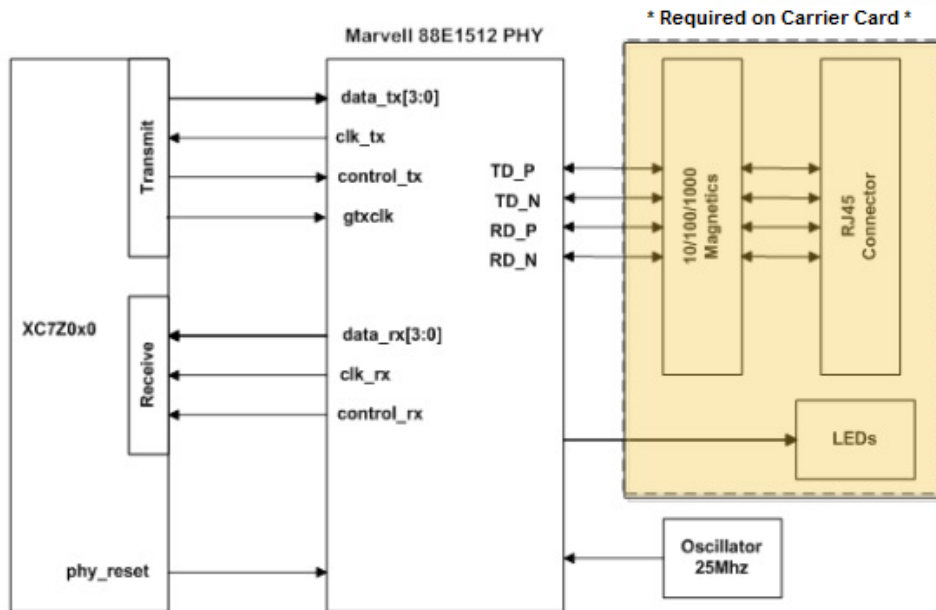
## 2.4 10/100/1000 Ethernet PHY

PicoZed 7010/7020 implements a 10/100/1000 Ethernet port for network connection using a Marvell 88E1512 PHY. This part operates at 1.8V. The PHY connects to MIO Bank 1/501 (1.8V) and interfaces to the Zynq-7000 AP SoC via RGMII.

The RJ-45 interface signals are connected to the JX3 Micro Header.

A high-level block diagram the 10/100/1000 Ethernet interface is shown in the following figure.





**Figure 3 – 10/100/1000 Ethernet Interface**

Zynq requires a voltage reference for RGMII interfaces. Thus PS\_MIO\_VREF, E11, is tied to 0.9V, half the bank voltage of MIO Bank 1/501. The 0.9V is generated through a resistor divider.

The 88E1512 also requires a 25 MHz input clock. An ABRACON ASDMB-25.000MHZ-LC-T is used as this reference.

**Table 6 – Ethernet PHY Pin Assignment and Definitions**

Signal Name	Description	Zynq pin	MIO	88E1512 pin
RX_CLK	Receive Clock	B17	16:27	46
RX_CTRL	Receive Control	D13		43
RXD[3:0]	Receive Data	RXD0: D11		44
		RXD1: A16		45
		RXD2: F15		47
		RXD3: A15		48
TX_CLK	Transmit Clock	A19		53
TX_CTRL	Transmit Control	F14		56
TXD[3:0]	Transmit Data	TXD0: E14	50	
		TXD1: B18	51	
		TXD2: D10	54	
		TXD3: A17	55	
MDIO	Management Data	C11	53	8
MDC	Management Clock	C10	52	7
ETH_RST_N	PHY Reset	B14	47 **	16 **

\*\* Requires a resistor change to the board to use PHY Reset. By default MIO47 is routed to JX3.

The datasheet for the Marvell 88E1512 is not available publicly. An NDA is required for this information. Please contact your local Avnet or Marvell representative for assistance.

## 2.5 User I/O

### 2.5.1 Available PS MIO User Pins

PicoZed 7010/7020 provides 8 user PS MIO pins from bank 500 and 12 user PS MIO pins from bank 501 of the Zynq-7000 AP SoC. The 20 PS MIO pins connect to the Zynq Processor Sub-System for the implementation of peripheral such as USB, SPI, SDIO, CAN, UART, and I2C. These I/O pins can also be used as general purpose IO to connect push buttons, LEDs and/or switches to the Zynq from the carrier card.

Note: The bank 500 PS MIO are shared with the eMMC interface and proper operation of these 8 user PS MIO pins depends on the multiplexer implemented to support the shared interface. Please review section 2.2.3 eMMC (Multi-Media Controller) for details on the multiplexer interface.

**Table 7 – PS MIO User Interface**

Signal Name	Zynq Pin	JX Pin
PS_MIO0	E6 (MIO Bank 500)	JX2.7
PS_MIO9	B5 (MIO Bank 500)	JX2.8
PS_MIO10	E9 (MIO Bank 500)	JX2.1
PS_MIO11	C6 (MIO Bank 500)	JX2.6
PS_MIO12	D9 (MIO Bank 500)	JX2.5
PS_MIO13	E8 (MIO Bank 500)	JX2.2
PS_MIO14	C5 (MIO Bank 500)	JX2.3
PS_MIO15	C8 (MIO Bank 500)	JX2.4
PS_MIO40	D14 (MIO Bank 501)	JX3.43
PS_MIO41	C17 (MIO Bank 501)	JX3.34
PS_MIO42	E12 (MIO Bank 501)	JX3.37
PS_MIO43	A9 (MIO Bank 501)	JX3.36
PS_MIO44	F13 (MIO Bank 501)	JX3.39
PS_MIO45	B15 (MIO Bank 501)	JX3.38
PS_MIO46	D16 (MIO Bank 501)	JX3.41
PS_MIO47	B14 (MIO Bank 501)	JX3.40
PS_MIO48	B12 (MIO Bank 501)	JX3.42
PS_MIO49	C12 (MIO Bank 501)	JX3.44
PS_MIO50	B13 (MIO Bank 501)	JX3.66
PS_MIO51	B9 (MIO Bank 501)	JX3.64

### 2.5.2 Available PL IO User Pins

PicoZed 7010/7020 provides 50 user PL IO pins from bank 34, 50 user PL IO pins from bank 35 of the Zynq-7000 AP SoC. Additionally, the PicoZed 7020 version provides access to 25 more user PL IO pins from bank 13. The 100 PL IO pins on the PicoZed 7010 and the 125 PL IO pins on the PicoZed 7020 connect to the Zynq Programmable Logic Sub-System for user implementation of any feasible interface.

The PL IO pins were routed with matched lengths to each of the JX connectors. The matched pairs, noted by “LVDS” in the net name of Tables 10, 11, and 12 may be used as either single ended I/O or differential pairs depending on the end users design requirements.

Use of these signals for various interfaces depends on the bank voltages assigned. The end user carrier card is responsible for providing VCCO for bank 34, bank 35, and bank13 depending on what it being implemented and whether you are using PicoZed 7010 or PicoZed 7020.

It is recommended that any custom interface to be implemented be run through the Vivado tool suite for a sanity check on place and route and timing closure in advance of end user carrier card manufacturing.

Pin out details of the available PL IO are included in section 2.8: Expansion Headers.

## 2.6 Clock Source

The PicoZed 7010/7020 connects a dedicated 33.3333 MHz clock source to the Zynq-7000 AP SoC's PS. An ABRACON ASDMB-33.333MHZ-LC-T or similar oscillator with 40-ohm series termination is used. The PS infrastructure can generate up to four PLL-based clocks for the PL system.

## 2.7 Reset Sources

### 2.7.1 Zynq Power-on Reset (PS\_POR\_B)

The Zynq PS supports an external power-on reset signal. The power-on reset is the master reset of the entire chip. This signal resets every register in the device capable of being reset. On PicoZed 7010/7020 this signal is labeled PG\_MODULE and it is connected to the power good output of the final stage of the power regulation circuitry. These power supplies have open drain outputs that pull this signal low until the output voltage is valid. If an expansion card is connected to PicoZed 7010/7020, the expansion card should also wire-OR to this net and not release it until the expansion card power is also good. Review the PicoZed 7010/7020 schematic for other devices that are reset by the PG\_MODULE open drain signal.

To stall Zynq boot-up, this signal should be held low. No other signal (PS\_SRST\_B, PROGRAM\_B, or INIT\_B) is capable of doing this as in other Xilinx FPGA architectures.

### 2.7.2 PROGRAM\_B, DONE, PUDC\_B, INIT\_B Pins

INIT\_B, PROGRAM\_B and PUDC\_B all have pull-up resistors to appropriate voltages applied to them. The INIT\_B, PUDC\_B and DONE signals are routed to the carrier card via the Micro Headers, JX1 and JX2.

There is not a DONE LED indicator on the PicoZed 7010/7020 System-On-Module. When PL configuration is complete DONE will go high. It is recommended that the DONE signal be connected to an LED on the carrier card to indicate when the FPGA configuration is complete.

When mating to the Avnet PicoZed FMC Carrier Card a blue LED labeled DONE will illuminate.

### 2.7.3 Processor Subsystem Reset

System reset, labeled PS\_SRST\_B, resets the processor as well as erases all debug configurations. The external system reset allows the user to reset all of the functional logic within the device without disturbing the debug environment. For example, the previous break points set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the OCM. The PL is also reset in system reset. System reset does not re-sample the boot mode strapping pins.

This active-low signal can be asserted via the carrier card through the Micro Header interface.

Note: This signal cannot be asserted while the boot ROM is executing following a POR reset. If PS\_SRST\_B is asserted while the boot ROM is running through a POR reset sequence it will trigger a lock-down event preventing the boot ROM from completing. To recover from lockdown the device either needs to be power cycled or PS\_POR\_B needs to be asserted.

## 2.8 Expansion Headers

### 2.8.1 Micro Headers

PicoZed 7010/7020 features three 100-pin Micro Headers (FCI, 61082-101400LF) for connection to expansion cards.

The JX1 and JX2 connectors interface PL, PS I/O to the expansion card as well as two dedicated analog inputs, the four dedicated JTAG signals, power and control signals. The JX3 connector interfaces to peripheral interfaces such as Ethernet, USB 2.0, 10 Bank 13 PL I/O (Zynq 7020 devices), and 12 Zynq PS MIO.

The connectors are FCI 0.8mm Bergstak®, 100 Position, Dual Row, BTB Vertical Receptacles. These have variable stack heights from 5mm to 16mm, making it easy to connect to a variety of expansion or system boards. Each pin can carry 500mA of current and support I/O speeds in excess of what Zynq can achieve.

PicoZed 7010/7020 does not power the PL VCCIO banks. This is required to be provided by the carrier card. This gives the carrier card the flexibility to control the I/O bank voltages. Separate routes/planes are used for VCCO\_34 and VCCO\_35 such that the carrier card could potentially power these independently. The PicoZed 7010 has two PL I/O banks. Banks 34 and 35 each contain 50 I/O. The PicoZed 7020 contains a third PL I/O bank. Bank 13 is fully connected (25 I/O) on the PicoZed 7020. Bank 13's power has an independent rail, VCCO\_13, which is powered from the carrier card as well.

Within a PL I/O Bank 34 or Bank 35, there are 50 I/O capable of up to 24 differential pairs per bank. Differential LVDS pairs on a -1 speed grade device are capable of 950Mbps of DDR data. Each differential pair from Bank 34 and 35 is isolated by a power or ground pin. Additionally, eight of these I/O can be connected as clock inputs (four MRCC and four SRCC inputs). Each PL bank can also be configured to be a memory interface with up to four dedicated DQS data strobes and data byte groups. Bank 35 adds the capability to use the I/O to interface up to 16 differential analog inputs. One of the differential pairs (JX1\_LVDS\_2\_P) in Bank 34 is shared with PUDC\_B.

The diagrams listed below illustrate the connections on the Micro Headers.

**Table 8 – Micro Header JX1 and JX2 Pin Outs**

Micro Header #1 (JX1)				Micro Header #2 (JX2)			
	Signal Name	Source	Pins	Signal Name	Source	Pins	
PL	Bank 34 I/Os (Except for PUDC_B)	Zynq Bank 34	49	PL	Bank 35 I/Os	Zynq Bank 35	50
	Bank 13 pins (PicoZed 7020)	Bank 13	8		Bank 13 pins (PicoZed 7020)	Bank 13	7
JTAG	TMS_0	Zynq Bank 0	5	PS	PS Pmod MIO[0,9-15]	Zynq Bank 500	8
	TDI_0	Zynq Bank 0			C	Init_B_0	Zynq Bank 0
	TCK_0	Zynq Bank 0		PG_1V8		Expansion	1
	TDO_0	Zynq Bank 0		PG_MODULE		Expansion	1
	Carrier_SRST#	Expansion		Vin	Expansion	5	
Analog	VP_0	Zynq Bank 0	4	Power	GND	Expansion	23
	VN_0	Zynq Bank 0			VCCO_35	Expansion	3
	DXP_0	Zynq Bank 0			VCCO_13	Expansion	1
	DXN_0	Zynq Bank 0					
C	FPGA_DONE	Zynq Bank 0	2		<b>TOTAL</b> 100		
	PUDC_B / IO	Zynq Bank 34					
	PWR_Enable	Expansion	1				
	Vin	Expansion	4				
	GND	Expansion	23				
	VCCO_34	Expansion	3				
	VBATT	Expansion	1				
<b>TOTAL</b>			<b>100</b>				

**Table 9 – Micro Header JX3 Pin Out**

Micro Header #3 (JX3)			
	Signal Name	Source	Pins
PL	Bank 13 I/Os (PicoZed 7020)	Zynq Bank 13 (PicoZed 7020)	<b>20*</b>
PS	Ethernet I/O	501	10
	USB I/O	501	4
	PS MIO[40-51]	Zynq Bank 501	12
MGT	(No Connect)	No Connect	20
Power	MGT_AVCC (No Connect)	No Connect	4
	MGTAVTT (No Connect)	No Connect	2
	VCCO_13	Expansion	2
	GND	Expansion	25
	USB_VBUS_OTG	Expansion	1
<b>TOTAL</b>			<b>100</b>

\* PicoZed 7020 only populates 10 out of 20 JX3 IO Dedicated to Bank 13 Signals

**Table 10 – JX1 Connections**

PicoZed 7010/7020 Pin #	Net Name	JX1 Pin #	JX1 Pin #	Net Name	PicoZed 7010/7020 Pin #
0 - F9	JTAG_TCK	1	2	JTAG_TMS	0 - J6
0 - F6	JTAG_TDO	3	4	JTAG_TDI	0 - G6
N/A	PWR_ENABLE	5	6	CARRIER_SRST#	501 - B10
0 - F11	FPGA_VBATT	7	8	FPGA_DONE	0 - R11
34 - R19	JX1_SE_0	9	10	JX1_SE_1	34 - T19
34 - T11	JX1_LVDS_0_P	11	12	JX1_LVDS_1_P	34 - T12
34 - T10	JX1_LVDS_0_N	13	14	JX1_LVDS_1_N	34 - U12
N/A	<b>GND</b>	15	16	<b>GND</b>	N/A
34 - U13	JX1_LVDS_2_P	17	18	JX1_LVDS_3_P	34 - V12
34 - V13	JX1_LVDS_2_N	19	20	JX1_LVDS_3_N	34 - W13
N/A	<b>GND</b>	21	22	<b>GND</b>	N/A
34 - T14	JX1_LVDS_4_P	23	24	JX1_LVDS_5_P	34 - P14
34 - T15	JX1_LVDS_4_N	25	26	JX1_LVDS_5_N	34 - R14
N/A	<b>GND</b>	27	28	<b>GND</b>	N/A
34 - Y16	JX1_LVDS_6_P	29	30	JX1_LVDS_7_P	34 - W14
34 - Y17	JX1_LVDS_6_N	31	32	JX1_LVDS_7_N	34 - Y14
N/A	<b>GND</b>	33	34	<b>GND</b>	N/A
34 - T16	JX1_LVDS_8_P	35	36	JX1_LVDS_9_P	34 - V15
34 - U17	JX1_LVDS_8_N	37	38	JX1_LVDS_9_N	34 - W15
N/A	<b>GND</b>	39	40	<b>GND</b>	N/A
34 - U14	JX1_LVDS_10_P	41	42	JX1_LVDS_11_P	34 - U18
34 - U15	JX1_LVDS_10_N	43	44	JX1_LVDS_11_N	34 - U19
N/A	<b>GND</b>	45	46	<b>GND</b>	N/A
34 - N18	JX1_LVDS_12_P	47	48	JX1_LVDS_13_P	34 - N20
34 - P19	JX1_LVDS_12_N	49	50	JX1_LVDS_13_N	34 - P20
N/A	<b>GND</b>	51	52	<b>GND</b>	N/A
34 - T20	JX1_LVDS_14_P	53	54	JX1_LVDS_15_P	34 - V20
34 - U20	JX1_LVDS_14_N	55	56	JX1_LVDS_15_N	34 - W20
N/A	<b>VIN_HDR</b>	57	58	<b>VIN_HDR</b>	N/A
N/A	<b>VIN_HDR</b>	59	60	<b>VIN_HDR</b>	N/A
34 - Y18	JX1_LVDS_16_P	61	62	JX1_LVDS_17_P	34 - V16
34 - Y19	JX1_LVDS_16_N	63	64	JX1_LVDS_17_N	34 - W16
N/A	<b>GND</b>	65	66	<b>GND</b>	N/A
34 - R16	JX1_LVDS_18_P	67	68	JX1_LVDS_19_P	34 - T17
34 - R17	JX1_LVDS_18_N	69	70	JX1_LVDS_19_N	34 - R18
N/A	<b>GND</b>	71	72	<b>GND</b>	N/A
34 - V17	JX1_LVDS_20_P	73	74	JX1_LVDS_21_P	34 - W18
34 - V18	JX1_LVDS_20_N	75	76	JX1_LVDS_21_N	34 - W19
N/A	<b>GND</b>	77	78	<b>VCCO_34</b>	N/A
N/A	<b>VCCO_34</b>	79	80	<b>VCCO_34</b>	N/A
34 - N17	JX1_LVDS_22_P	81	82	JX1_LVDS_23_P	34 - P15
34 - P18	JX1_LVDS_22_N	83	84	JX1_LVDS_23_N	34 - P16
N/A	<b>GND</b>	85	86	<b>GND</b>	N/A
13 - U7	BANK13_LVDS_0_P	87	88	BANK13_LVDS_1_P	13 - T9
13 - V7	BANK13_LVDS_0_N	89	90	BANK13_LVDS_1_N	13 - U10
13 - V8	BANK13_LVDS_2_P	91	92	BANK13_LVDS_3_P	13 - T5
13 - W8	BANK13_LVDS_2_N	93	94	BANK13_LVDS_3_N	13 - U5
N/A	<b>GND</b>	95	96	<b>GND</b>	N/A
0 - K9	VP_0_P	97	98	DXP_0_P	0 - M9
0 - L10	VN_0_N	99	100	DXN_0_N	0 - M10

Table 11 – JX2 Connections

PicoZed 7010/7020 Pin #	PicoZed Net	JX2 Pin #	JX2 Pin #	PicoZed Net	PicoZed 7010/7020 Pin #
500 - E9	PS_MIO10	1	2	PS_MIO13	500 – E8
500 - C5	PS_MIO14	3	4	PS_MIO15	500 – C8
500 - D9	PS_MIO12	5	6	PS_MIO11	500 – C6
500 - E6	PS_MIO0	7	8	PS_MIO9	500 – B5
0 - R10	INIT#	9	10	VCCIO_EN	N/A
500 - C7	PG_MODULE	11	12	VIN_HDR	N/A
35 - G14	JX2_SE_0	13	14	JX2_SE_1	35 - J15
N/A	GND	15	16	GND	N/A
35 - C20	JX2_LVDS_0_P	17	18	JX2_LVDS_1_P	35 - B19
35 - B20	JX2_LVDS_0_N	19	20	JX2_LVDS_1_N	35 - A20
N/A	GND	21	22	GND	N/A
35 - E17	JX2_LVDS_2_P	23	24	JX2_LVDS_3_P	35 - D19
35 - D18	JX2_LVDS_2_N	25	26	JX2_LVDS_3_N	35 - D20
N/A	GND	27	28	GND	N/A
35 - E18	JX2_LVDS_4_P	29	30	JX2_LVDS_5_P	35 - F16
35 - E19	JX2_LVDS_4_N	31	32	JX2_LVDS_5_N	35 - F17
N/A	GND	33	34	GND	N/A
35 - L19	JX2_LVDS_6_P	35	36	JX2_LVDS_7_P	35 - M19
35 - L20	JX2_LVDS_6_N	37	38	JX2_LVDS_7_N	35 - M20
N/A	GND	39	40	GND	N/A
35 - M17	JX2_LVDS_8_P	41	42	JX2_LVDS_9_P	35 - K19
35 - M18	JX2_LVDS_8_N	43	44	JX2_LVDS_9_N	35 - J19
N/A	GND	45	46	GND	N/A
35 - L16	JX2_LVDS_10_P	47	48	JX2_LVDS_11_P	35 - K17
35 - L17	JX2_LVDS_10_N	49	50	JX2_LVDS_11_N	35 - K18
N/A	GND	51	52	GND	N/A
35 - H16	JX2_LVDS_12_P	53	54	JX2_LVDS_13_P	35 - J18
35 - H17	JX2_LVDS_12_N	55	56	JX2_LVDS_13_N	35 - H18
N/A	VIN_HDR	57	58	VIN_HDR	N/A
N/A	VIN_HDR	59	60	VIN_HDR	N/A
35 - G17	JX2_LVDS_14_P	61	62	JX2_LVDS_15_P	35 - F19
35 - G18	JX2_LVDS_14_N	63	64	JX2_LVDS_15_N	35 - F20
N/A	GND	65	66	GND	N/A
35 - G19	JX2_LVDS_16_P	67	68	JX2_LVDS_17_P	35 - J20
35 - G20	JX2_LVDS_16_N	69	70	JX2_LVDS_17_N	35 - H20
N/A	GND	71	72	GND	N/A
35 - K14	JX2_LVDS_18_P	73	74	JX2_LVDS_19_P	35 - H15
35 - J14	JX2_LVDS_18_N	75	76	JX2_LVDS_19_N	35 - G15
N/A	GND	77	78	VCCO_35	N/A
N/A	VCCO_35	79	80	VCCO_35	N/A
35 - N15	JX2_LVDS_20_P	81	82	JX2_LVDS_21_P	35 - L14
35 - N16	JX2_LVDS_20_N	83	84	JX2_LVDS_21_N	35 - L15
N/A	GND	85	86	GND	N/A
35 - M14	JX2_LVDS_22_P	87	88	JX2_LVDS_23_P	35 - K16
35 - M15	JX2_LVDS_22_N	89	90	JX2_LVDS_23_N	35 - J16
N/A	GND	91	92	GND	N/A
13 - Y12	BANK13_LVDS_4_P	93	94	BANK13_LVDS_5_P	13 - V11
13 - Y13	BANK13_LVDS_4_N	95	96	BANK13_LVDS_5_N	13 - V10
13 - V6	BANK13_LVDS_6_P	97	98	VCCO_13	N/A
13 - W6	BANK13_LVDS_6_N	99	100	BANK13_SE_0	13 - V5

Table 12 – JX3 Connections

PicoZed 7010/7020 Pin #	PicoZed Net	JX3 Pin #	JX3 Pin #	PicoZed Net	PicoZed 7010/7020 Pin #
N/A	MGTREFCLK0_P	1	2	MGTREFCLK1_P	N/A
N/A	MGTREFCLK0_N	3	4	MGTREFCLK1_N	N/A
N/A	<b>MGTAVCC</b>	5	6	<b>GND</b>	N/A
N/A	<b>MGTAVCC</b>	7	8	MGTRX0_P	N/A
N/A	<b>MGTAVCC</b>	9	10	MGTRX0_N	N/A
N/A	<b>MGTAVCC</b>	11	12	<b>GND</b>	N/A
N/A	MGTTX0_P	13	14	MGTRX1_P	N/A
N/A	MGTTX0_N	15	16	MGTRX1_N	N/A
N/A	<b>GND</b>	17	18	<b>GND</b>	N/A
N/A	MGTTX1_P	19	20	MGTRX2_P	N/A
N/A	MGTTX1_N	21	22	MGTRX2_N	N/A
N/A	<b>GND</b>	23	24	<b>GND</b>	N/A
N/A	MGTTX2_P	25	26	MGTRX3_P	N/A
N/A	MGTTX2_N	27	28	MGTRX3_N	N/A
N/A	<b>GND</b>	29	30	<b>MGTAVTT</b>	N/A
N/A	MGTTX3_P	31	32	<b>MGTAVTT</b>	N/A
N/A	MGTTX3_N	33	34	PS_MIO41	501 – C17
N/A	<b>GND</b>	35	36	PS_MIO43	501 – A9
501 – E12	PS_MIO42	37	38	PS_MIO45	501 – B15
501 – F13	PS_MIO44	39	40	PS_MIO47	501 – B14
501 – D16	PS_MIO46	41	42	PS_MIO48	501 – B12
501 – D14	PS_MIO40	43	44	PS_MIO49	501 – C12
N/A	<b>VCCO_13</b>	45	46	<b>VCCO_13</b>	N/A
N/A	ETH_PHY_LED0	47	48	ETH_PHY_LED1	N/A
N/A	<b>GND</b>	49	50	<b>GND</b>	N/A
N/A	ETH_MD1_P	51	52	ETH_MD2_P	N/A
N/A	ETH_MD1_N	53	54	ETH_MD2_N	N/A
N/A	<b>GND</b>	55	56	<b>GND</b>	N/A
N/A	ETH_MD3_P	57	58	ETH_MD4_P	N/A
N/A	ETH_MD3_N	59	60	ETH_MD4_N	N/A
N/A	<b>GND</b>	61	62	<b>GND</b>	N/A
N/A	USB_OTG_ID	63	64	PS_MIO51	501 – B9
N/A	<b>GND</b>	65	66	PS_MIO50	501 – B13
N/A	USB_OTG_P	67	68	<b>USB_VBUS_OTG</b>	N/A
N/A	USB_OTG_N	69	70	USB_OTG_CPEN	N/A
N/A	<b>GND</b>	71	72	<b>GND</b>	N/A
13-Y7	BANK13_LVDS_7_P	73	74	BANK13_LVDS_8_P	13-Y9
13-Y6	BANK13_LVDS_7_N	75	76	BANK13_LVDS_8_N	13-Y8
N/A	<b>GND</b>	77	78	<b>GND</b>	N/A
13-W10	BANK13_LVDS_9_P	79	80	BANK13_LVDS_10_P	13-U9
13-W9	BANK13_LVDS_9_N	81	82	BANK13_LVDS_10_N	13-U8
N/A	<b>GND</b>	83	84	<b>GND</b>	N/A
13-W11	BANK13_LVDS_11_P	85	86	BANK13_LVDS_12_P	N/A
13-Y11	BANK13_LVDS_11_N	87	88	BANK13_LVDS_12_N	N/A
N/A	<b>GND</b>	89	90	<b>GND</b>	N/A
N/A	BANK13_LVDS_13_P	91	92	BANK13_LVDS_14_P	N/A
N/A	BANK13_LVDS_13_N	93	94	BANK13_LVDS_14_N	N/A
N/A	<b>GND</b>	95	96	<b>GND</b>	N/A
N/A	BANK13_LVDS_15_P	97	98	BANK13_LVDS_16_P	N/A
N/A	BANK13_LVDS_15_N	99	100	BANK13_LVDS_16_N	N/A



## 2.9 Configuration Modes

Zynq-7000 AP SoC devices use a multi-stage boot process that supports both non-secure and secure boot. The PS is the master of the boot and configuration process. Upon reset, the device mode pins are read to determine the primary boot device to be used: NOR, NAND, Quad-SPI, SD Card or JTAG. PicoZed 7010/7020 allows 3 of those boot devices: QSPI is the default, while SD Card and JTAG boot are easily accessible by changing switch settings.

Note: SD Card and JTAG interfaces should be implemented on the end user carrier card.

Zynq has Voltage Mode pins, which are fixed on PicoZed 7010/7020

The boot mode pins are shared with MIO[8:2]. The usage of these mode pins can be and are used as follows:

- MIO[2] / Boot\_Mode[3]
  - sets the JTAG mode
- MIO[5:3] / Boot\_Mode[2:0]
  - select the boot mode
  - Boot\_Mode[1] is fixed since it is only required for NOR boot, which is not supported on PicoZed 7010/7020
- MIO[6] / Boot\_Mode[4]
  - enables the internal PLL
  - fixed to 'enabled' on PicoZed 7010/7020
- MIO[8:7] / Vmode[1:0]
  - configures the I/O bank voltages
  - fixed on PicoZed 7010/7020
  - MIO Bank 0 / 500 (MIO[7] / Vmode[0]) set to '0' for 3.3V
  - MIO Bank 1 / 501 (MIO[8] / Vmode[1]) set to '1' for 1.8V

All mode pins are pulled either high or low through a 20 K $\Omega$  resistor that is either hard wired or connected to a switch or resistor jumper. By default, four mode signals are not jumper-adjustable and are populated as follows:

- MIO[3] / Boot\_Mode[1] is pulled low via 20 K $\Omega$  resistor.
- MIO[6] / Boot\_Mode[4] is pulled low via 20 K $\Omega$  resistor.
- MIO[7] / Vmode[0] is pulled low via 20 K $\Omega$  resistor.
- MIO[8] / Vmode[1] is pulled high via 20 K $\Omega$  resistor.

The other three mode signals, MIO[2], MIO[4] and MIO[5], are configurable via a jumper resistor or switch setting.

MIO[2] is pulled either high or low via a 0 ohm resistor jumper JT4. Default setting from the factory is pulled low (position 1-2) and puts the Zynq in Cascade JTAG mode.

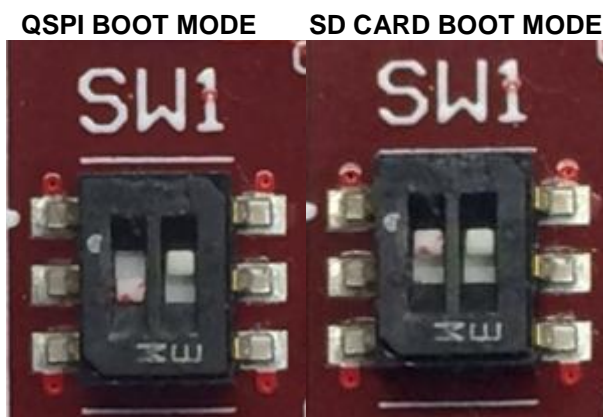
MIO[5:4] is pulled high or low via a two channel dip switch SW1. Setting the switch positions will determine whether the Zynq boots from QSPI, the microSD card, or JTAG.

The table below shows the available boot mode configuration setting using JT4 and SW1.

**Table 13 – PicoZed 7010/7020 Configuration Modes**

BOOT MODE	JT4	SW1 (1-3)	SW1 (4-6)
QSPI	X	LOW (2-3)	HIGH (4-5)
SD CARD *	X	HIGH (1-2)	HIGH (4-5)
JTAG *	X	LOW (2-3)	LOW (5-6)
INDEP JTAG *	HIGH (2-3)	LOW (2-3)	LOW (5-6)
CASCADE JTAG *	LOW (1-2)	LOW (2-3)	LOW (5-6)

\*Interfaces on the End User Carrier Card



**Figure 4: PicoZed 7010/7020 Boot Mode Switch**

Expected configuration time using a 50MB/s QSPI flash is 250ms.

Zynq has many other configuration options; PicoZed 7010/7020 uses this configuration:

- V<sub>CC0\_0</sub> is tied to 3.3V on PicoZed 7010/7020.
- PUDC\_B can be pulled high or low on PicoZed 7010/7020 via a resistor (JT5). This active-low input enables internal pull-ups during configuration on all SelectIO pins. By default, JT5 is populated with a 1K resistor in the 1-2 position, which pulls up PUDC\_B and disables the pull-ups during configuration. PUDC\_B is shared with Bank 34 I/O IO\_L3P and is connected to the Micro Header.
- Init\_B is pulled high via a 4.7KΩ resistor (RP2.2), but also connected to the Micro Header.
- Program\_B is pulled high via a 4.7KΩ resistor (RP2.4).
- CFGBVS is pulled high via a 4.7KΩ resistor (RP2.1).

The PS is responsible for configuring the PL. Zynq will not automatically reconfigure the PL as in standard FPGAs by toggling PROG. Likewise, it is not possible to hold off Zynq boot up with INIT\_B as this is now done with POR. If the application needs to reconfigure the PL, the software design must do this, or you can toggle POR to restart everything. When PL configuration is complete and the end user is using the Avnet PicoZed FMC Carrier Card, a blue LED will illuminate.

### 2.9.1 JTAG Connections

PicoZed 7010/7020 requires an external JTAG cable connector populated on the carrier card for JTAG operations. JTAG signals are routed from Bank 0 of the Zynq to the Micro Header JX1. The following table shows the JTAG signal connections between the Zynq and the Micro Header.

The Zynq Bank 0 reference voltage, V<sub>CC0\_0</sub>, is connected to 3.3V. The JTAG Vref on the End User Carrier Card should be connected to 3.3V to ensure compatibility between the interfaces. For reference, see the PicoZed FMC Carrier Card schematics.

**Table 14 – PicoZed 7010/7020 JTAG Connections**

SoC Pin #	PicoZed 7010/7020 Net	JX1 Pin #
F9	JTAG_TCK	1
J6	JTAG_TMS	2
F6	JTAG_TDO	3
G6	JTAG_TDI	4

## 2.10 Power Supplies

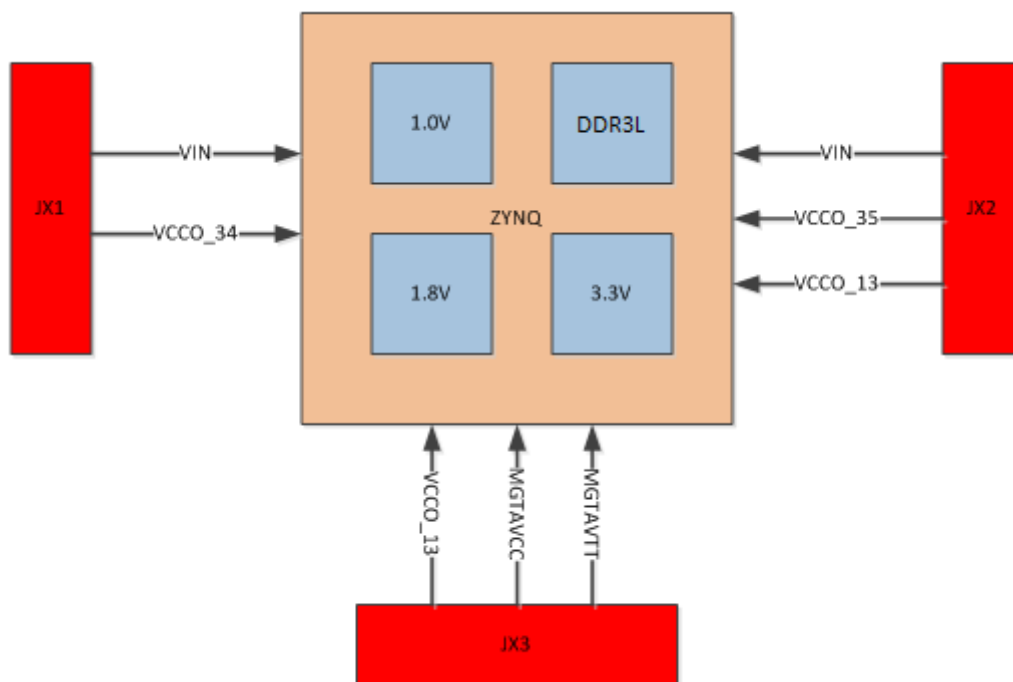
### 2.10.1 Voltage Rails and Sources

PicoZed 7010/7020 is powered through the Micro Header connection between itself and the carrier card.

There are five regulators that reside on the PicoZed 7010/7020 that provide 1.0V, 1.35V, 1.8V, 3.3V and 0.675V power rails. These voltages are used to power the peripheral devices on the PicoZed System-On-Module. These regulators are powered from the end user carrier card via the VIN pins on the Micro Headers and are expected to carry 5V or 12V to the PicoZed System-On-Module for the input to the regulators.

There are also three bank voltages that are supplied from the end user carrier card to the PicoZed System-On-Module. Bank 34 (VCCO\_34), Bank 35 (VCCO\_35) and Bank 13 (VCCO\_13) are generated on the end user carrier card and connected to the PicoZed 7010/7020 System-On-Module via the Micro Headers. The voltage at which these banks operate is up to the carrier card design as all I/O that connect to these banks is exclusive to the Micro Headers (no on-board device is connected to these banks).

The diagram below shows a high level depiction of the power scheme for PicoZed 7010/7020 System-On-Module.



**Figure 5: PicoZed 7010/7020 Power Scheme**

The table below shows the various voltage rails names on the schematic, the associated voltage for each rail, where they are connected on the Zynq 7010/7020, and where the voltage originates from.

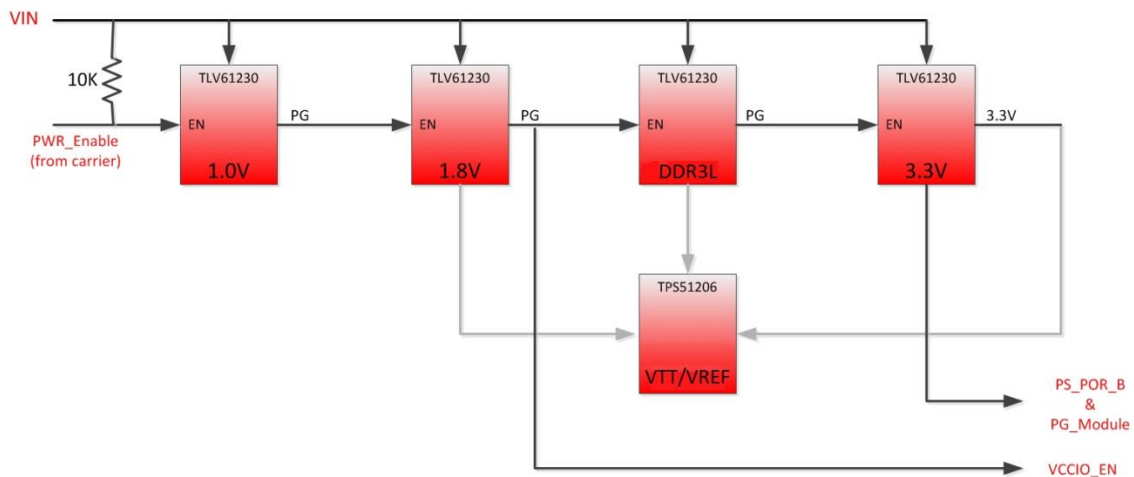
**Table 15 – PicoZed 7010/7020 Voltage Rails**

Schematic Voltage Name	Voltage Level	Zynq Connection	Voltage Origination
1.0V	1.0V	VCCINT	SOM
		VCCBRAM	
		VCCPINT	
VCCO_DDR3	1.35V	VCCO_DDR_502 (Bank 502)	
VTTREF	0.675V	PS_DDR_VREF0 (Bank 502)	
		PS_DDR_VREF1 (Bank 502)	
1.8V	1.8V	VCCO_MIO1_501 (Bank 501)	
		VCCAUX	
		VCCPAUX	
3.3V	3.3V	VCCO_0 (Bank 0)	
		VCC_MIO0_500 (Bank 500)	
VCCO_34	1.8V/2.5V/3.3V	VCCO_34 (Bank 34)	JX1
VCCO_35	1.8V/2.5V/3.3V	VCCO_35 (Bank 35)	JX2
VCCO_13	1.8V/2.5V/3.3V	VCCO_13 (Bank 13)	JX2/JX3

### 2.10.2 Voltage Regulators

The following power solution provides the power rails of the PicoZed 7010/7020. Sequencing of the supplies is implemented by cascading the POWER GOOD outputs of each supply in the sequence. 3.3V is the last supply to come up, therefore the POWER GOOD for the 3.3V supply is used to drive the PG\_MODULE net and is used as the power-on reset control for Zynq (U11.pin C7), Ethernet PHY (U4.pin 16), and USB-Host PHY (U5.pin 27).

This net is also connected to the Micro Headers so power supplies on the end user carrier card can also control this signal.



**Figure 6 – Regulation Circuitry (VCCIO\_EN is PG\_1V8)**

This circuit sequences power-up of PicoZed 7010/7020. 1.0V comes up first, then 1.8V, then VCCO\_DDR3 and then 3.3V. PG\_MODULE is connected to PS\_POR\_B on Zynq, thus when the power supplies are valid, PS\_POR\_B is released.

When the PicoZed 7010/7020 is mated to an end user carrier card, the POWER GOOD outputs

of the end user carrier card should also be tied to the PG\_MODULE net on JX1.pin 8. If the end user carrier card power supplies do not have POWER GOOD outputs, a voltage supervisor or open-drain buffer should be used to complement this circuit.

PicoZed 7010/7020 also provides a power good signal to the end user carrier card to signal that Vccint and Vccaux are both up and the end user carrier card is free to bring up the Vcco supplies. This signal is called VCCIO\_EN (PG\_1V8) and is tied to JX2.pin 10.

NOTE: VCCIO\_EN is provided by the power good output of the 1.8V regulator.

The table below shows the maximum output current for each regulator on the PicoZed 7010/7020 System-On-Module.

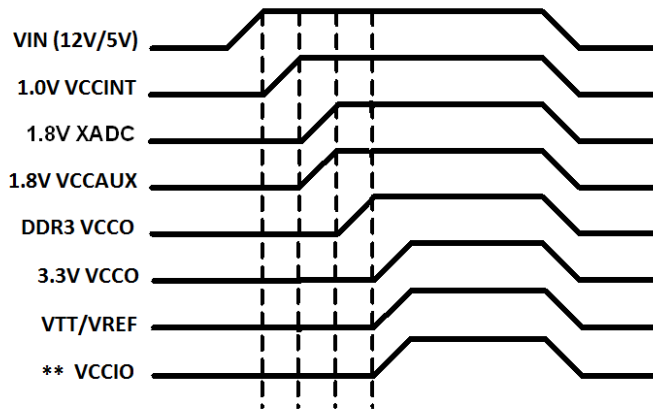
**Table 16 – Voltage Rails w/ Max Output Current**

TI Part Number	Voltage (V)	Max Current (A)
TLV62130	1.0	3
TLV62130	1.8	3
TLV62130	1.35	3
TLV62130	3.3	3
TPS51206	0.675	2

### 2.10.3 Power Supply Sequencing

When attached to an end user carrier card, the carrier card must provide an active-high, power enable signal, PWR\_ENABLE. This controls the first PicoZed 7010/7020 regulator (U19, 1.0V) turning on. This should be an open drain design such that this signal will float high (pulled high to 5V or 12V on PicoZed 7010/7020). This may allow for the special circumstance of the end user carrier card controlling the powering of the PicoZed 7010/7020 for low power applications.

Sequencing for the power supplies follows the recommendations for the Zynq device. VCCINT/VCCPINT/VCCBRAM and VCCAUX/VCCPAUX supplies are tied together on the PicoZed 7010/7020 platform to create a low cost design. The following diagram illustrates the supply sequencing:

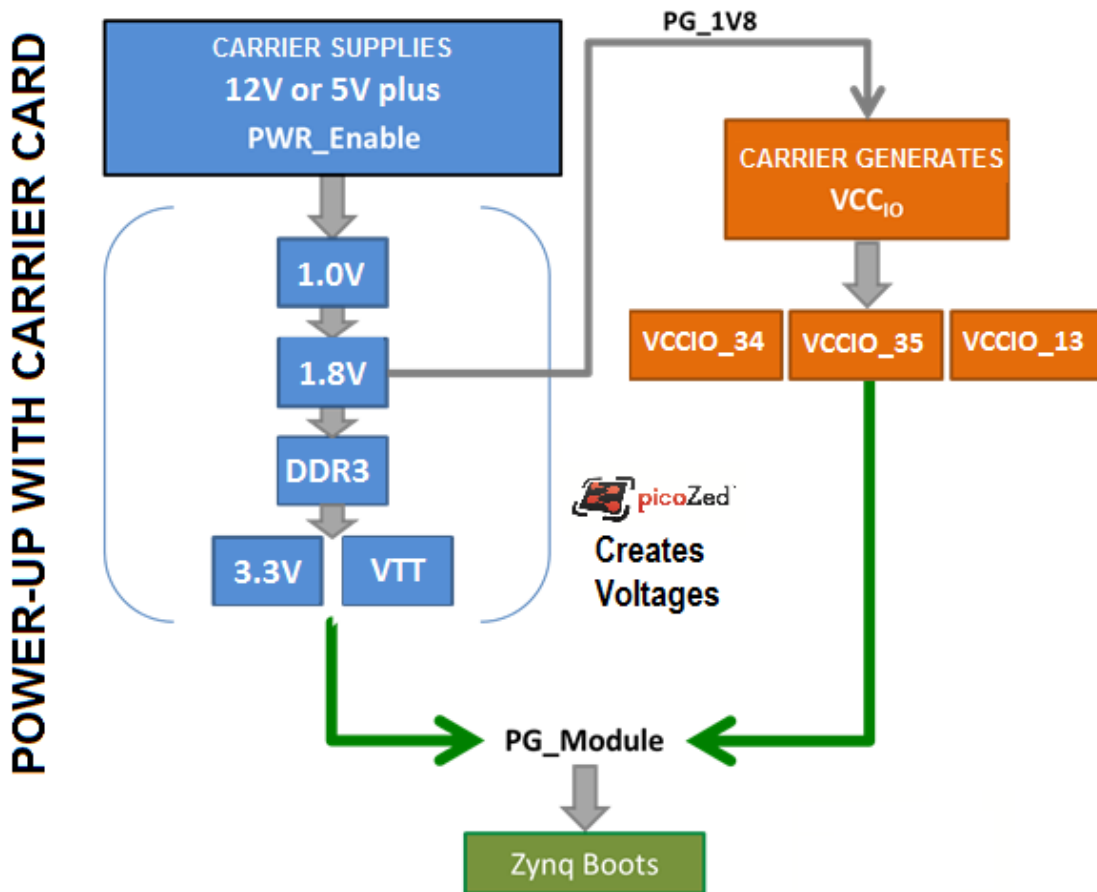


\*\* VCCIO driven from end user carrier card

**Figure 7 – Power Supply Sequencing**

As noted above, if connected to an end user carrier card, the 1.8V power supply's power good output should be used as the enable to the VCCIO regulators via the PG\_1V8 (VCCIO\_EN) signal on the Micro Headers.

The following diagram illustrates sequencing with an expansion card:



**Figure 8 – Power Sequencing with Carrier Card**

## 2.10.4 PCB Bypass / Decoupling Strategy

The PicoZed 7010/7020 design follows the PCB decoupling strategy as outlined in UG933 for the 7Z020, CLG400 package. The PicoZed 7010 depopulates a few of these capacitors while maintaining the listed requirements.

Package	Device	V <sub>CCINT</sub> <sup>(3)</sup>					V <sub>CCBRAM</sub>				V <sub>CCAUX</sub>			V <sub>CCAUX_IO</sub>			V <sub>CCO</sub> per Bank <sup>(4)(5)</sup>				Bank 0
		680 μF	330 μF	100 μF	4.7 μF	0.47 μF	100 μF	47 μF	4.7 μF	0.47 μF	47 μF	4.7 μF	0.47 μF	47 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	47 μF	
CLG400	Z-7010	0	0	1	1	2	0	1	1	1	1	1	1	NA	NA	NA	1	2	4	1	
CLG400	Z-7020	0	1	0	2	4	1	0	1	1	1	1	1	NA	NA	NA	1	2	4	1	

Figure 9 – CLG400 PL Decoupling

Package	Device	V <sub>CCPINT</sub>			V <sub>CCPAUX</sub> <sup>(2)</sup>			V <sub>CCO_DDR</sub>			V <sub>CCO_MIO0</sub>			V <sub>CCO_MIO1</sub>			V <sub>CCPLL</sub> <sup>(1)(3)</sup>	
		100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	100 μF	4.7 μF	0.47 μF	10 μF	0.47 μF
CLG400	Z-7010	1	1	3	1	1	1	1	4	1	1	1	1	1	1	1	1	
CLG400	Z-7020	1	1	3	1	1	1	1	4	1	1	1	1	1	1	1	1	

Figure 10 – CLG400 PS Decoupling

## 2.10.5 Power Good LED

A green status LED, D1, illuminates with the U18 3.3V power rail. Since this regulator is the last one in the sequence to come up, it is an effective indication that all regulators are on.

## 2.10.6 Power Estimation

Since the total power consumption of the system heavily depends on many factors with regard to the configuration/utilization of the Zynq device, it is highly recommended that the end user perform some power estimation and analysis using the Xilinx Power Estimator (XPE). This tool is very useful for plugging in various parameters and getting an estimated power consumption estimate for the system.

The XPE tool can be downloaded from the following link:

[http://www.xilinx.com/products/design\\_tools/logic\\_design/xpe.htm](http://www.xilinx.com/products/design_tools/logic_design/xpe.htm)

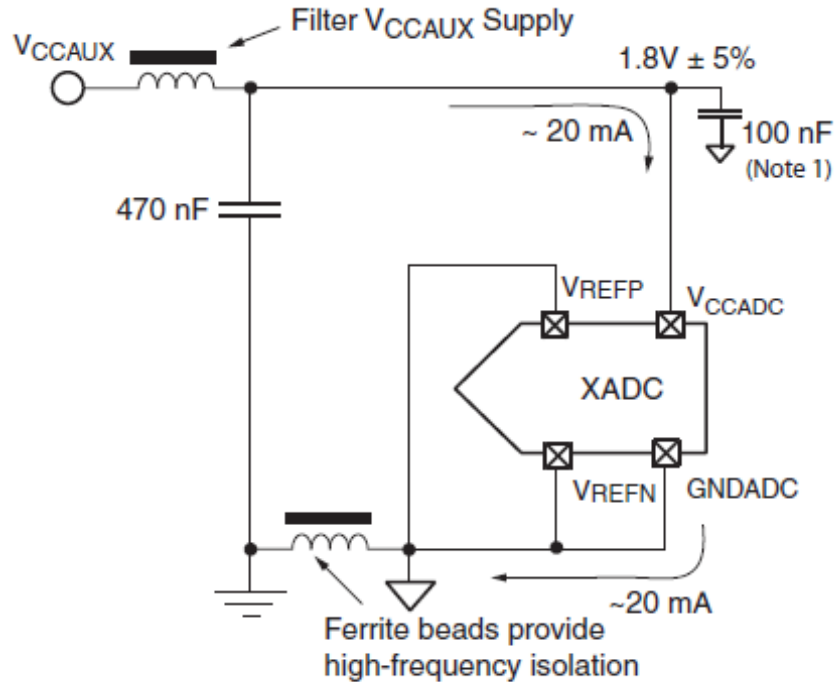
When designing the PicoZed 7010/7020 power system, this tool was used to ensure that the SOM system could supply enough power to the Zynq and its on-board peripherals using worst case parameters including logic utilization, operating frequency and temperature.

Since the power supply for the VCCIO rails for banks 34, 35, and 13 are supplied from the carrier card, it is important to make sure that the end user carrier card power supplies are adequate to power these rails over the desired and/or estimated operating scenario.

NOTE: When designing a custom PicoZed Carrier Board, be sure to use XPE (Xilinx Power Estimator) to estimate the power needed by the FPGA. The designer will need this figure in sizing the input supply to the SOM. In addition to the XPE results for the core power supplies, V<sub>ccint</sub>/V<sub>ccpint</sub> (1V) and V<sub>ccaux</sub>/V<sub>ccpaux</sub>/V<sub>ccpll</sub> (1.8V), you will need to add an additional 2.4W to your power estimate to compensate for the additional power that is needed for the peripherals on the PicoZed System-On-Modules such as memory and USB and Ethernet PHY devices.

## 2.10.7 XADC Power Configuration

The XADC component is powered from the filtered 1.8V V<sub>CCaux</sub> supply utilizing the on-chip reference as shown below.



UG480\_c6\_01\_091012

**Figure 11 – XADC Power Configuration**

### 2.10.8 Battery Backup - Device Secure Boot Encryption Key

Zynq power rail  $V_{CCBATT}$  is a 1.0V to 1.89V voltage typically supplied by a battery. This supply is used to maintain an encryption key in battery-backed RAM for device secure boot. The encryption key can alternatively be stored in eFuse which does not require a battery.

As specified in the Zynq TRM, if the battery is not used, connect  $V_{CCBATT}$  to either ground or  $V_{CCAUX}$ . On PicoZed,  $V_{CCBATT}$  is connected to net FPGA\_VBATT and is tied through a 0  $\Omega$  resistor (R14) to the PicoZed  $V_{CCAUX}$  supply, which is 1.8V. However, FPGA\_VBATT is also extended to the end user carrier card. To apply an external battery to Zynq from the end user carrier card, the 0-ohm resistor, R14, should be removed from the PicoZed System-On-Module.

### 2.10.9 Cooling Fan

An unpopulated-header JP1, labeled FAN, is available in the event a fan is needed for high performance designs. This header provides two ground connections and one connection to the VIN voltage. PicoZed 7010/7020 also provides a resistor option for a 3.3V fan via JT3. Two mounting holes (MTG[3:4]) near the Zynq device are provided where an active or passive heat sink might be secured.



## 3 Zynq-7000 AP SoC I/O Bank Allocation

### 3.1 PS MIO Allocation

There are 54 I/O available in the PS MIO. The table below lists the number of required I/O per peripheral and the MIO locations where the interface exists.

**Table 17 – PS MIO Interface Requirements**

Interface	I/O Required	MIO
QSPI FLASH	7	1-6, 8
USB Host	13	7, 28-39
ETHERNET	15	16-27, 47, 52-53
eMMC / Micro Header General Purpose	6	10-15
Micro Header General Purpose	13	0, 9, 40-46, 48-51
<b>TOTAL</b>	<b>54</b>	

The Micro Header GPIO assignments aren't specifically defined interfaces such as those that are defined in Table 17. The table below provides the MIO locations of the PS MIO general purpose pins and the functions that they are intended to support. The end user is encouraged to utilize the Zynq TRM in defining the MIO peripheral mappings that they would like to utilize on a custom PicoZed carrier card.

**Table 18 – PS GPIO Assignments**

MIO	Voltage	Function
7	3.3V	USB RESET
8	3.3V	QSPI FB CLK
0, 9	3.3V	PS GPIO
10-15	3.3V	eMMC or PS GPIO
40-46, 48-51	1.8V	PS GPIO
47	1.8V	PS GPIO or ETHERNET RESET

## 3.2 Zynq-7000 AP SoC Bank Voltages

The I/O bank voltage assignments are shown in the table below.

**Table 19 – Zynq Bank Voltage Assignments**

<b>PS-Side</b>	
<b>Bank</b>	<b>Voltage (default)</b>
MIO Bank 0/500	3.3V
MIO Bank 1/501	1.8V
DDR3L	1.35V
<b>PL-Side</b>	
Bank0	3.3V
Bank 34	Carrier Card – Vcco_34
Bank 35	Carrier Card – Vcco_35
Bank 13	Carrier Card – Vcco_13

PL I/O Banks 34, 35, and 13 are powered from the end user carrier card. These bank supplies are designed to be independent on the PicoZed 7010/7020. Maximum flexibility is allowed to the designer for these banks as the voltage level and standards are left to the end user carrier card design. The designer of the end user carrier card VCCO supplies is provided the choice of whether the IO banks use a shared voltage supply or independent voltage supplies.

## 4 Mechanical

PicoZed 7010/7020 measures 2.25" x 4.00" (57.15 mm x 101.6 mm)

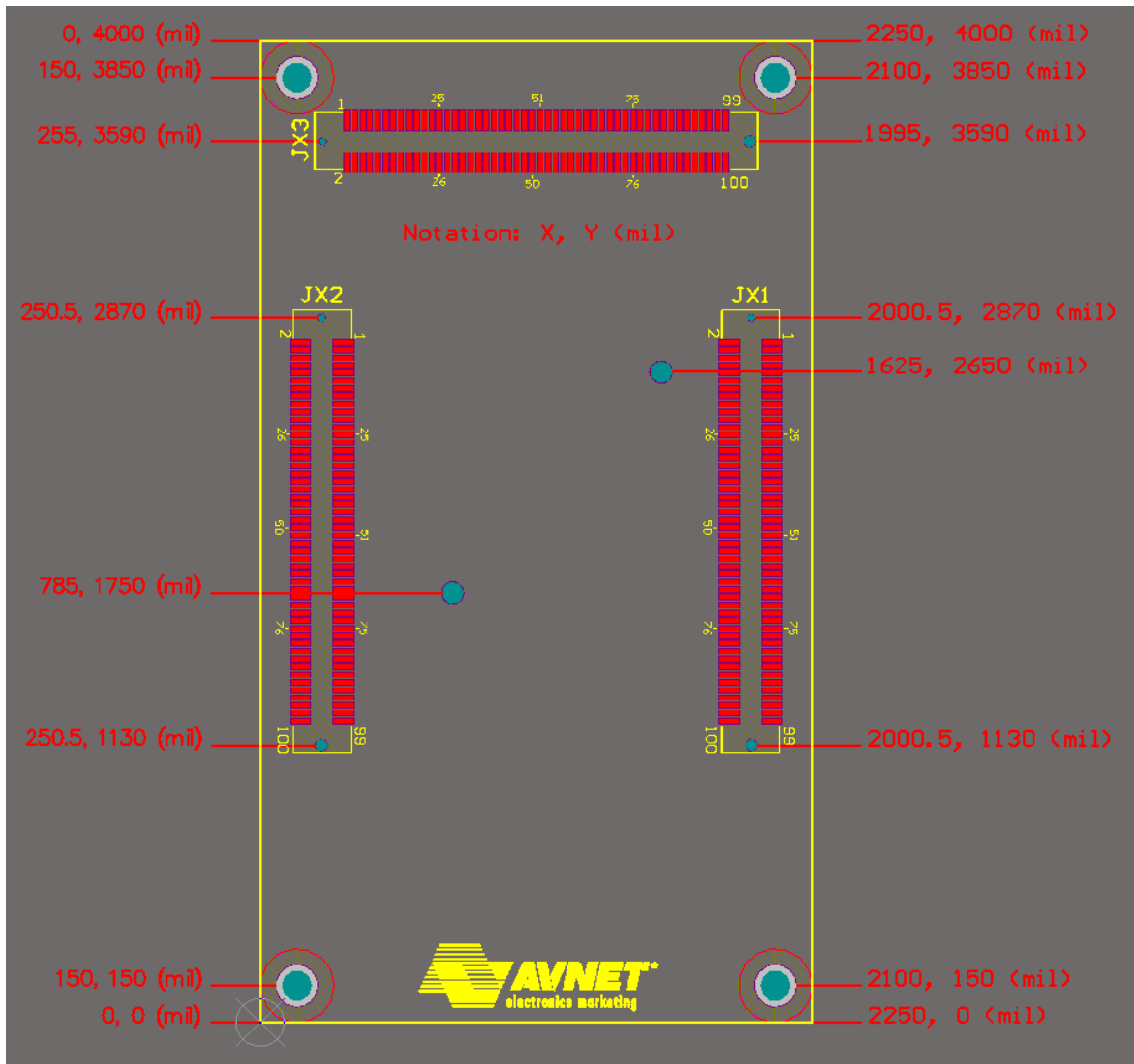


Figure 12 – PicoZed 7010/7020 Top View Mechanical Dimensions

PicoZed 7010/7020 has a maximum vertical dimension of 0.366" (9.3mm)

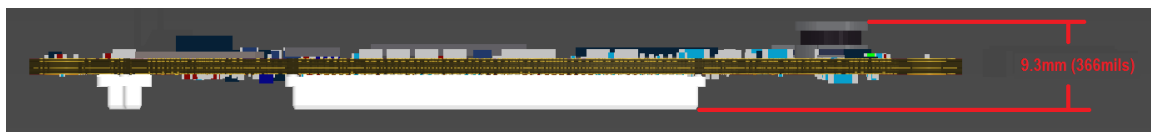


Figure 13 – PicoZed 7010/7020 Side View Vertical Dimension

## 5 Revision History

Rev date	Rev #	Reason for change
6 Oct 14	1.0	Initial PicoZed 7010/7020 Hardware User Guide
30 Oct 14	1.1	DDR3L documented and Diagram Updates
2 Dec 14	1.2	Diagram Update Figure 5 and PL IO LVDS support
8 Dec 14	1.3	Removed AR numbers for DDR3 and reference UG933
3 Feb 15	1.4	Swapper JX3 pin listing in Table 7 for JX3.64/JX3.66