

Intellian Technologies

Project Name : IRIDIUM BDU
MODEL No :
VERSION : Ver 0.8
DATE : 2020.02.17

Page Description

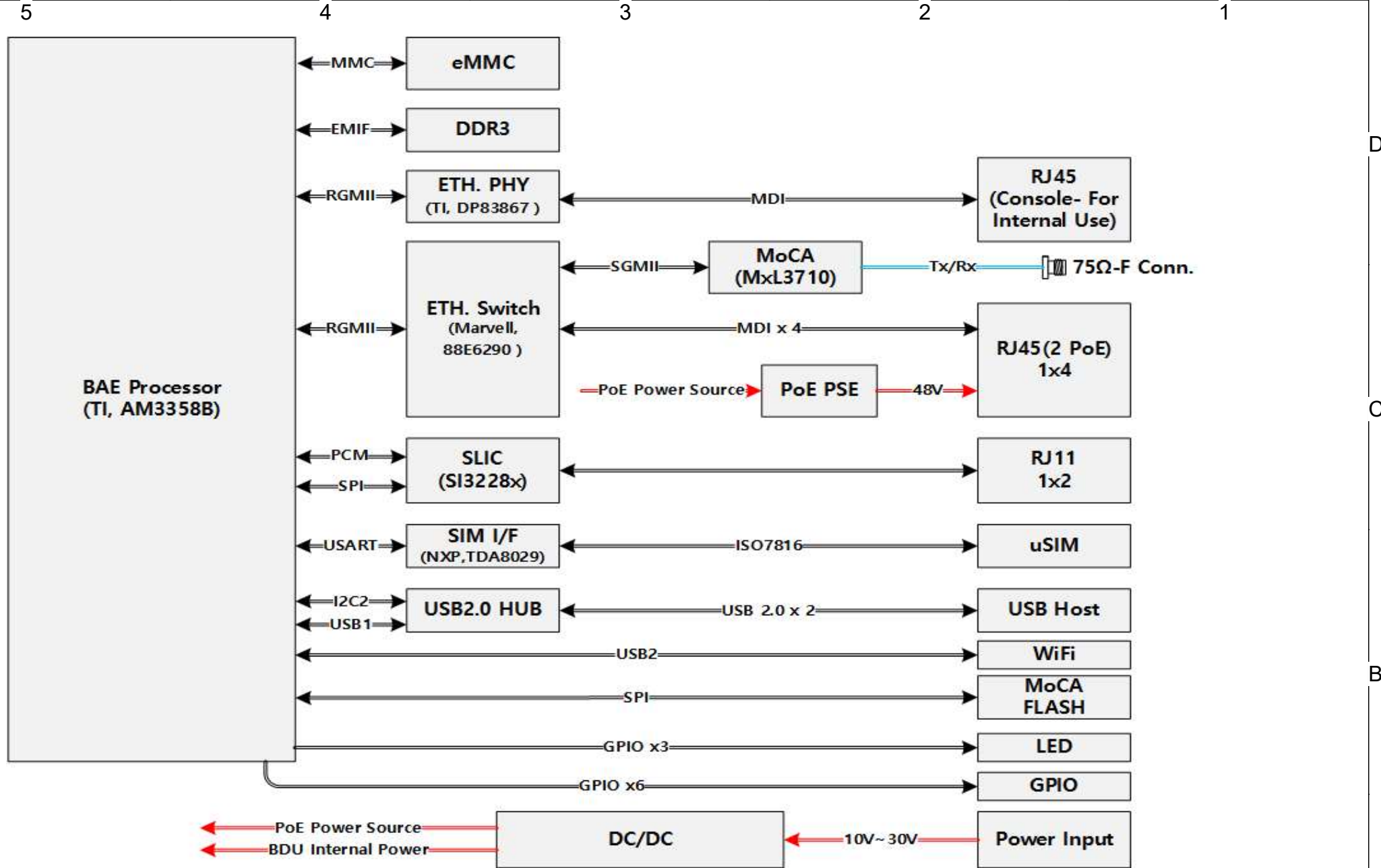
Revision History


Rev.	DATE	CONTENTS
Ver 0.1	2018.09.10	Initial Draft
Ver 0.2	2019.02.20	PoE I2C Interface , ETH. PHY Strap Change
Ver 0.3	2019.04.18	
Ver 0.4	2019.05.08	Newly Added USB HUB RGMII Power Rail changed
Ver 0.5	2019.06.xx	PoE Power LED Color Chane
Ver 0.6	2019.10.xx	ADU Power Control Fuse Swith changed
Ver 0.7	2019.10.23	Added Filter for EMI Suppresion
Ver 0.8	2020.02.17	R846, R847, R848 newly added for working voltage 12 and 24 D90,91,92,D93 newly added for working voltage 12 and 24 Changed SN74AHC1G08DCKR to SN74LVC1G08DCKR Deleted D64, R32,33 Value Changed Newly added clock source divider at MoCA PHY which used for Debug Newly added which used for Fan Control Changed B6 to U94 for power protection

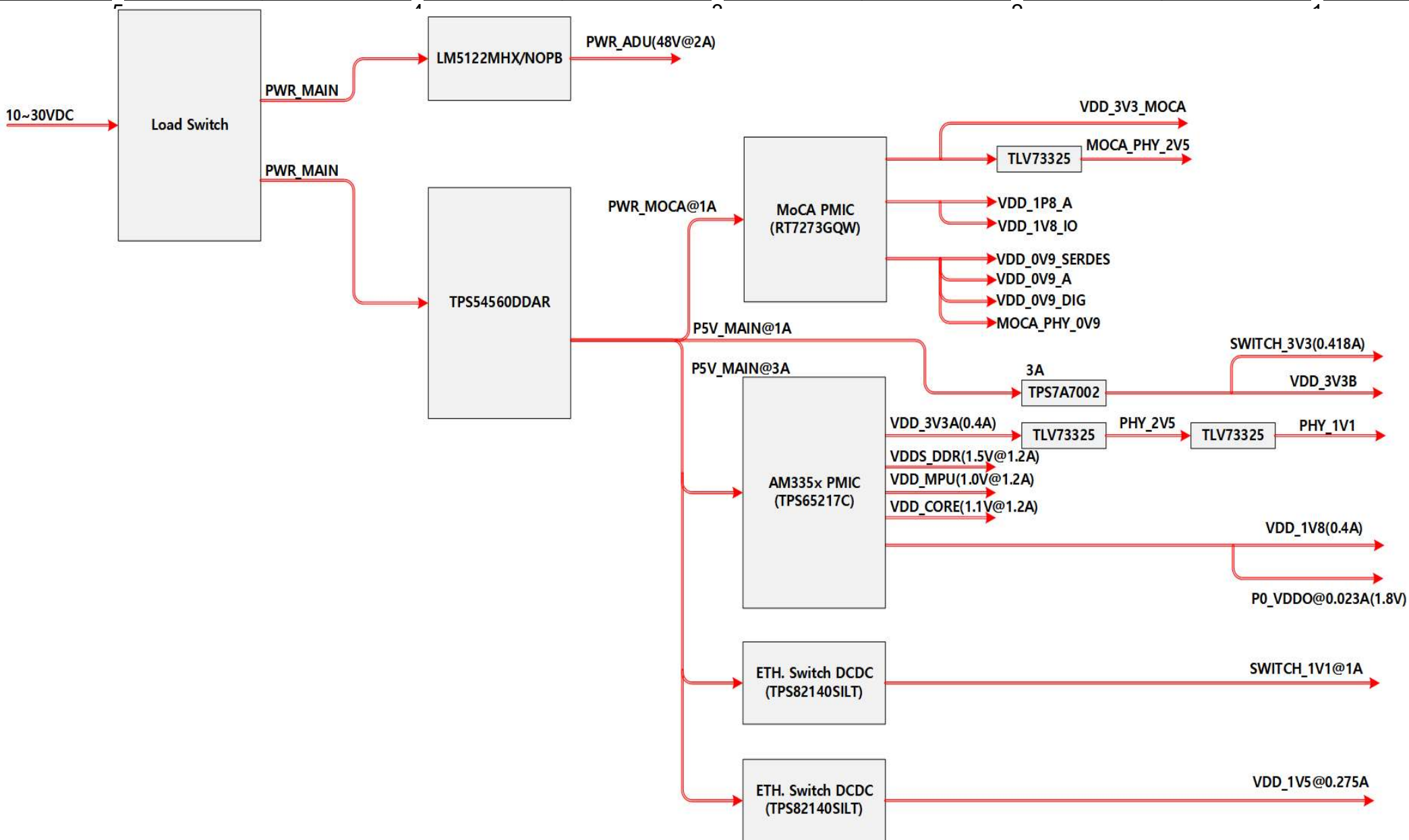
Stack Up Information


Low Speed Signal	Layer 1
GND	Layer 2
High Speed Signal - Eth / eMMC / DDR	Layer 3
High Speed Signal - Eth / eMMC / DDR	Layer 4
Power	Layer 5
Low Speed Signal	Layer 6

APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea		
DRAWN : SR.CHOI - [19/04/18]		TITLE: IRIDIUM BDU		
CHECKED :				
APPROVED:				
ENGINEER : SR.CHOI - [YY/MM/DD]		SIZE A3	DWG NO. 00-Title	REV E
ARTWORK :		DATE: Wednesday, February 19, 2020	SHEET 1 OF 25	

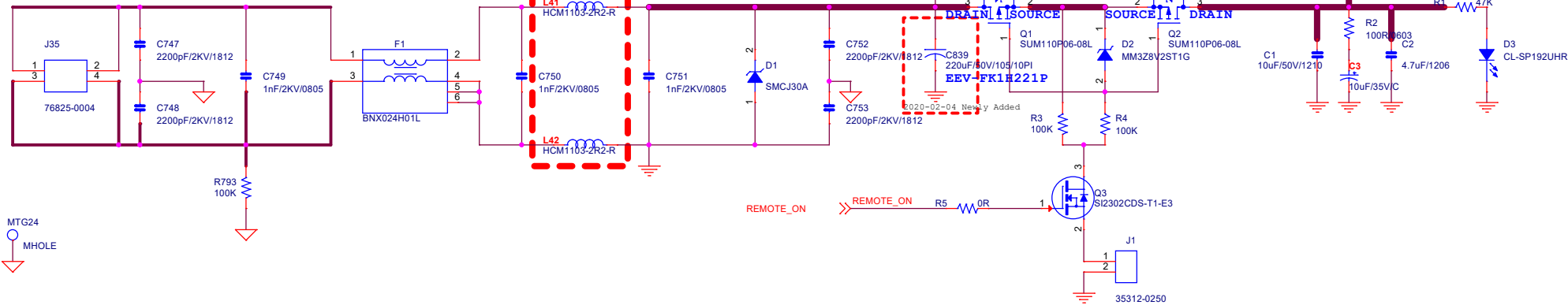


APPROVALS		 Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea		
DRAWN	: SR.CHOI - [YY/MM/DD]			
CHECKED	: Checker - [YY/MM/DD]	TITLE:		
APPROVED	: Approver - [YY/MM/DD]	IRIDIUM BDU		
ENGINEER	: SR.CHOI - [YY/MM/DD]	SIZE	DWG NO. BDU-0001	REV
ARTWORK	: HY.PARK - [YY/MM/DD]	A3	00. Block Diagram	C
DATE: Wednesday, February 19, 2020		SHEET 2 OF 25		



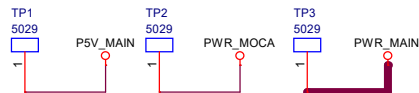
APPROVALS		 Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN	: SR.CHOI - [YY/MM/DD]		
CHECKED	: Checker - [YY/MM/DD]		
APPROVED	: Approver - [YY/MM/DD]		
ENGINEER	: SR.CHOI - [YY/MM/DD]		
ARTWORK	: HY.PARK - [YY/MM/DD]	TITLE:	
		Iridium Certus BDU	
SIZE	DWG NO.	<Doc>	REV
A3	01. POWER RAIL		A
DATE:	Wednesday, February 19, 2020		SHEET 3 OF 25

POWER Input Range : 10V to 30V



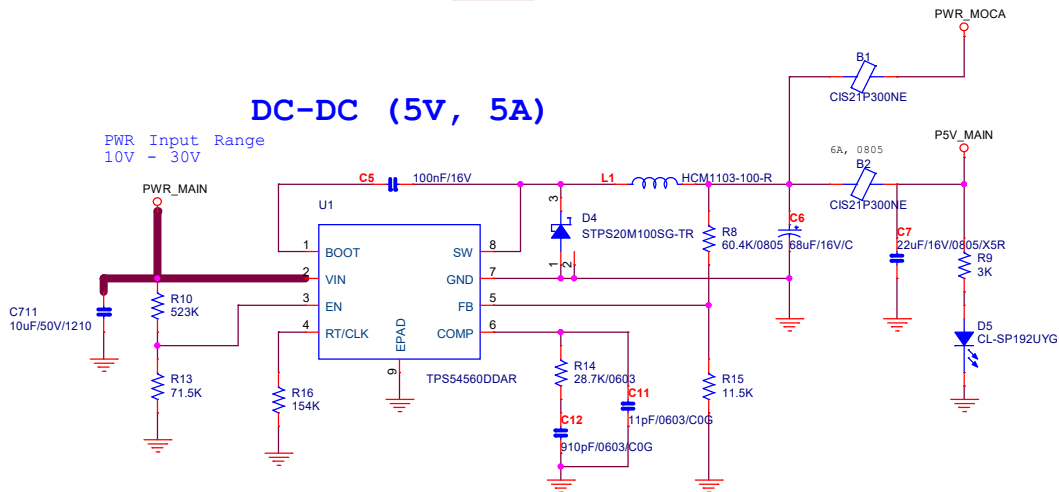
MTG24
MHOLE

Test point Resfer to below URL
<https://www.digikey.com/product-detail/en/keystone-electronics/5029/36-5029TR-ND/3904815>

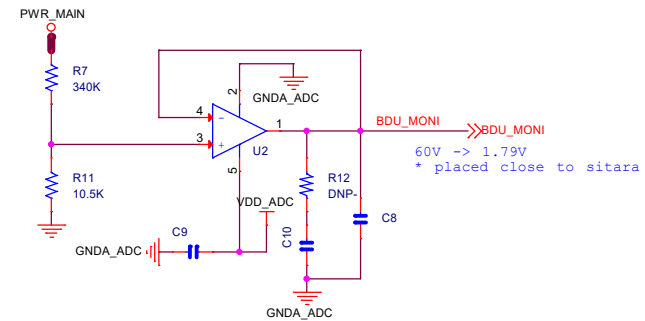


DC-DC (5V, 5A)

PWR Input Range
10V - 30V

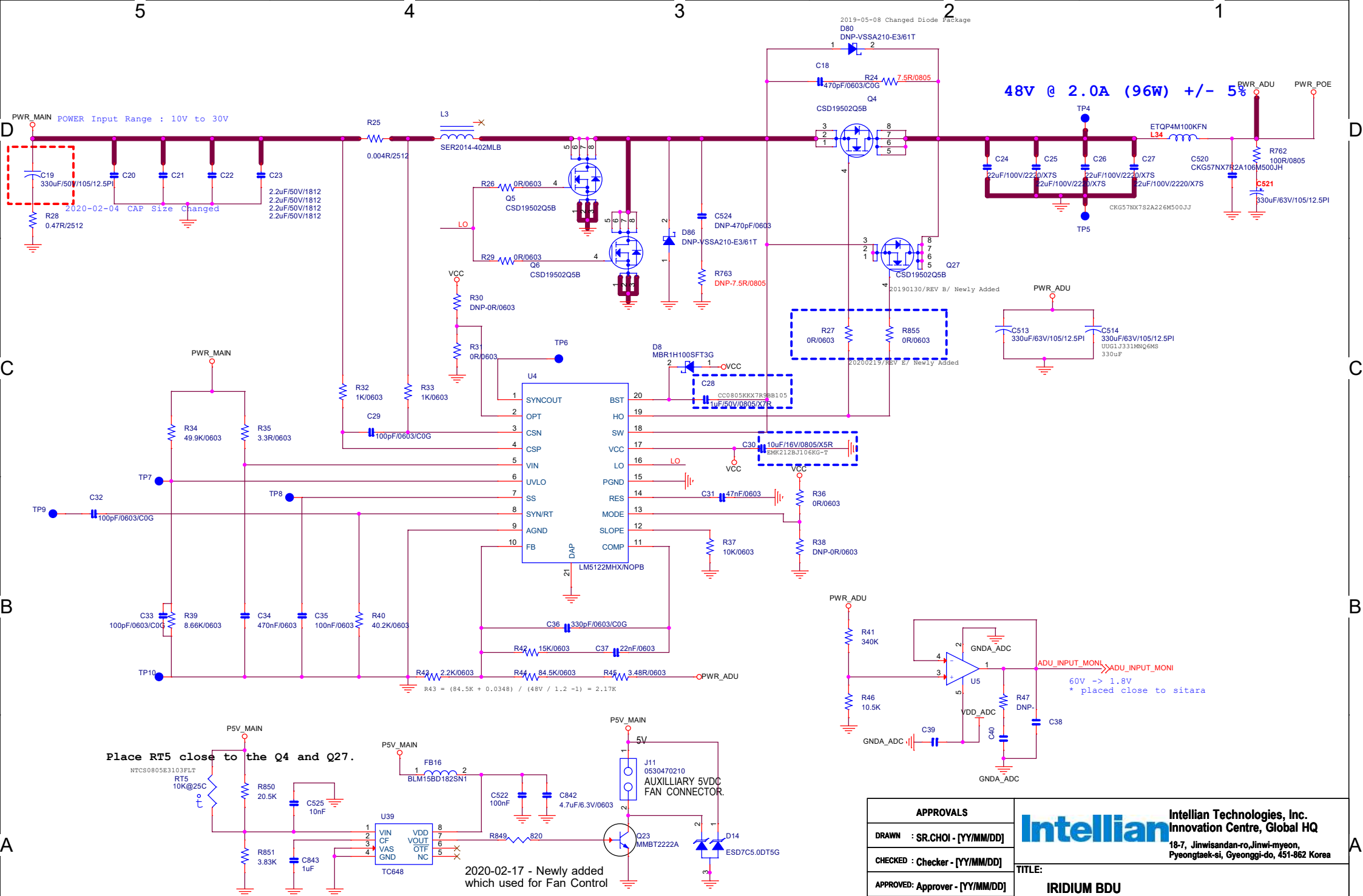


$$V_{out} = 0.8 * (1 + R1/R2)$$

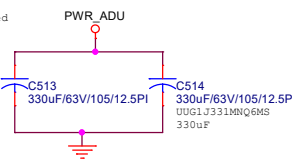
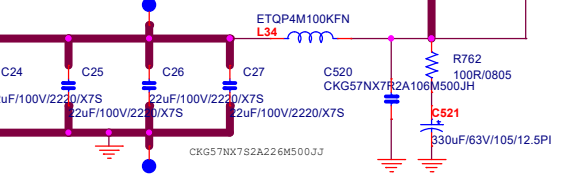


60V -> 1.79V
* placed close to sitara

APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea		
DRAWN	: SR.CHOI - [YY/MM/DD]			
CHECKED	: Checker - [YY/MM/DD]	TITLE:		
APPROVED	: Approver - [YY/MM/DD]	IRIDIUM BDU		
ENGINEER	: SR.CHOI - [YY/MM/DD]	SIZE	DWG NO. <Doc>	REV
ARTWORK	: HY.PARK - [YY/MM/DD]	A3	02 - POWER - MAIN	A
DATE: Wednesday, February 19, 2020		SHEET 4 OF 25		



48V @ 2.0A (96W) +/- 5%



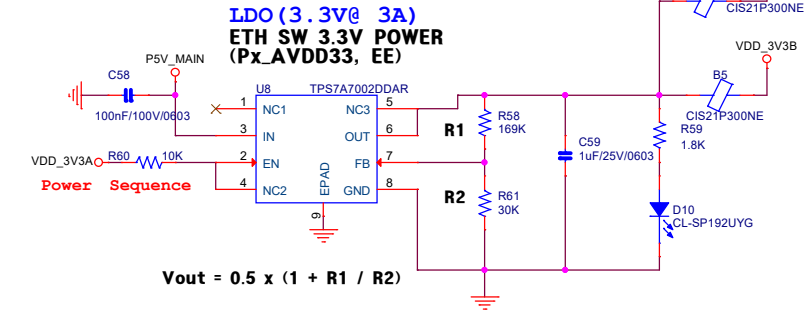
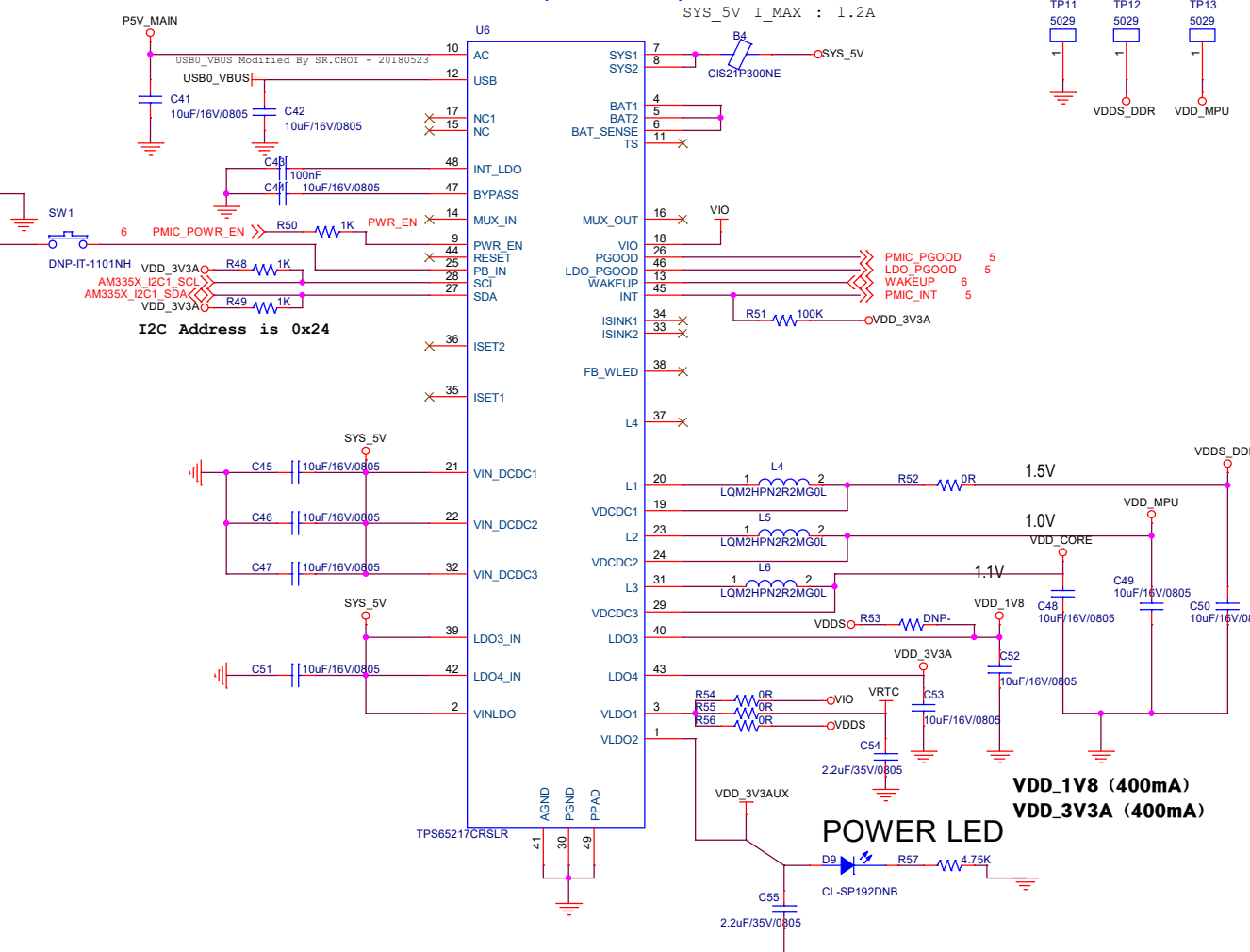
Place RT5 close to the Q4 and Q27.

2020-02-17 - Newly added which used for Fan Control

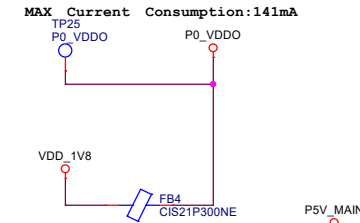
APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea		
DRAWN : SR.CHOI - [YY/MM/DD] CHECKED : Checker - [YY/MM/DD] APPROVED: Approver - [YY/MM/DD] ENGINEER : SR.CHOI - [YY/MM/DD] ARTWORK : HY.PARK - [YY/MM/DD]	TITLE: IRIDIUM BDU			SIZE A3
DATE: Monday, February 24, 2020		SHEET 5 OF 25		

PMIC (CPU Power)

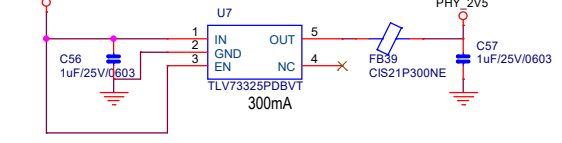
Test point Refer to below URL
<https://www.digikey.com/product-detail/en/keystone-electronics/5029/36-5029TR-ND/3904815>



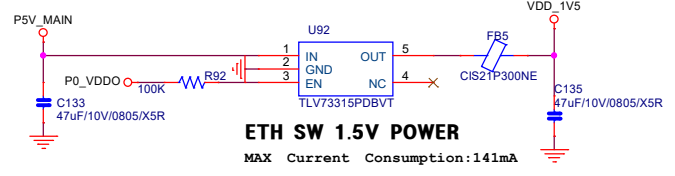
ETH SW 1.8V POWER (P0, GPIO)



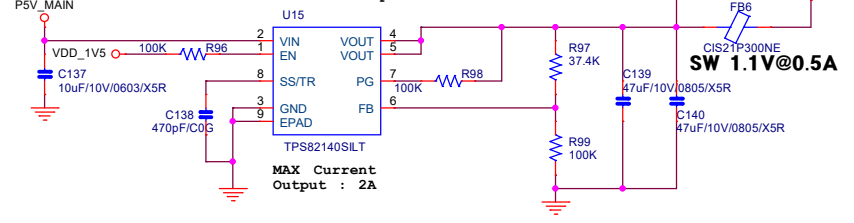
LDO 2.5V@0.3A



ETH SW 1.5V POWER



ETH SW 1.1V POWER



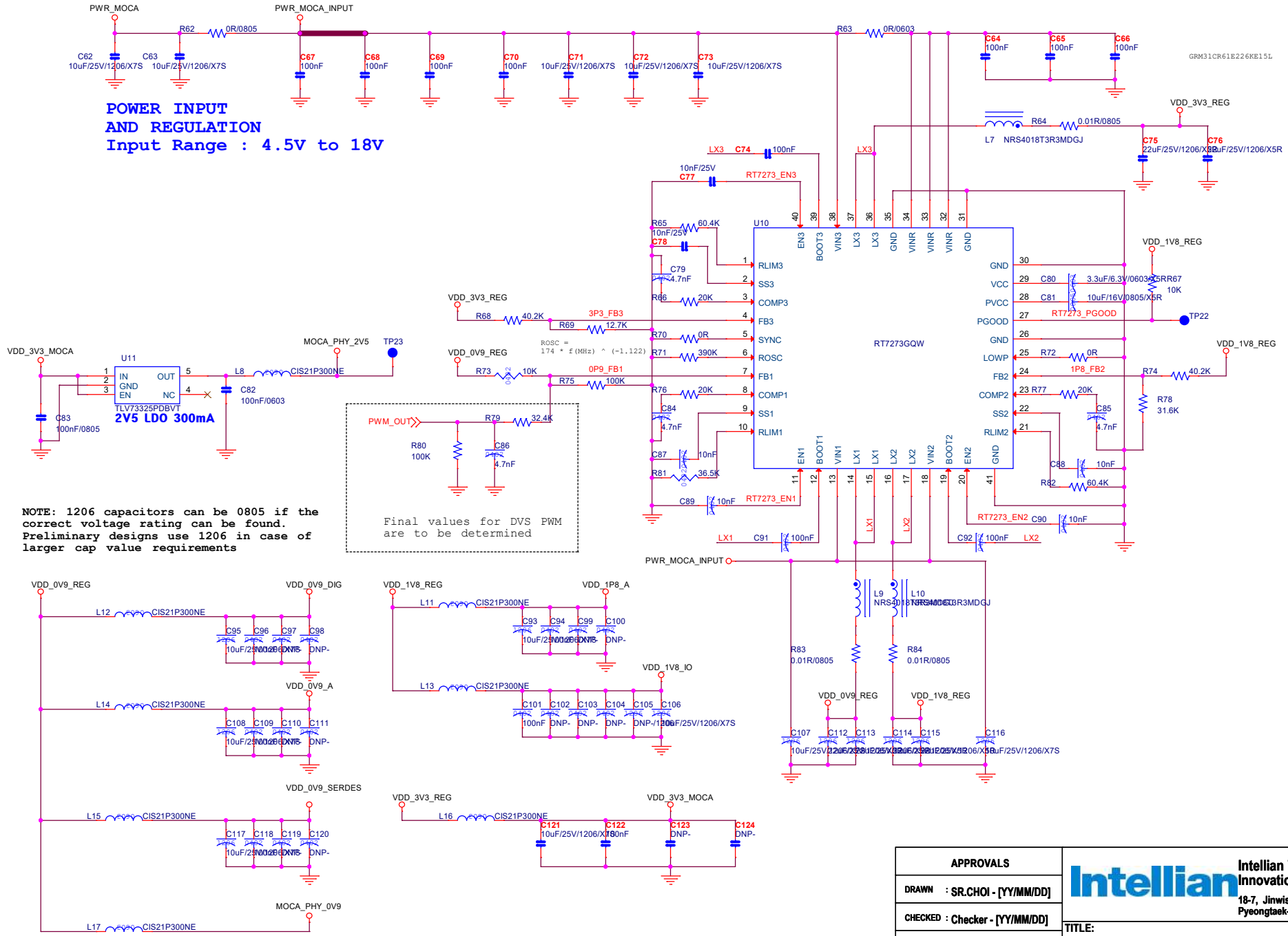
APPROVALS	
DRAWN : SR.CHOI - [YY/MM/DD]	
CHECKED :	
APPROVED:	
ENGINEER : SR.CHOI - [YY/MM/DD]	
ARTWORK :	

Intellian Intellian Technologies, Inc.
 Innovation Centre, Global HQ
 18-7, Jinwisandan-ro, Jinwi-myeon,
 Pyeongtaek-si, Gyeonggi-do, 451-862 Korea

TITLE:
IRIDIUM BDU

SIZE	DWG NO.	REV
A3	00002	A
04. POWER AM3358		
DATE: Wednesday, February 19, 2020	SHEET 6 OF 25	

POWER INPUT AND REGULATION
Input Range : 4.5V to 18V

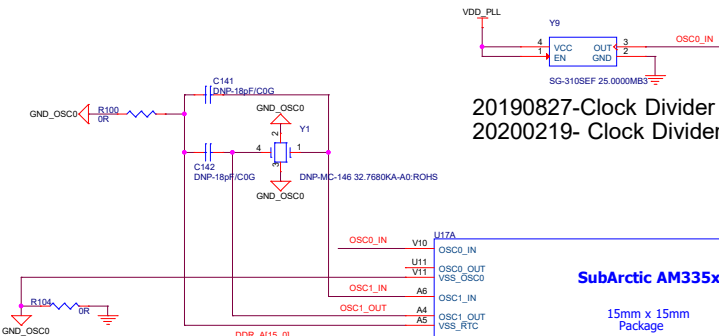


NOTE: 1206 capacitors can be 0805 if the correct voltage rating can be found. Preliminary designs use 1206 in case of larger cap value requirements

Final values for DVS PWM are to be determined

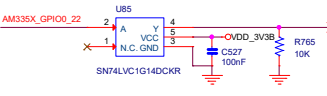
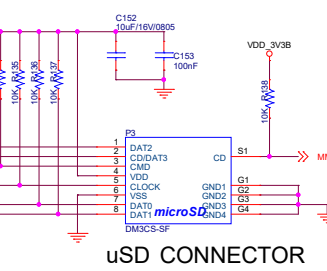
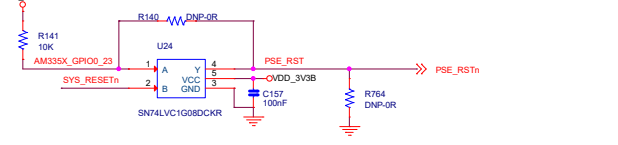
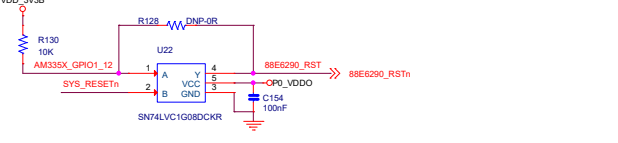
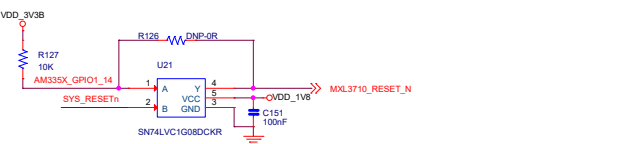
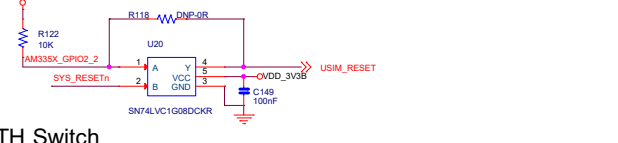
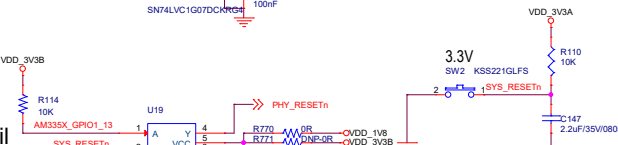
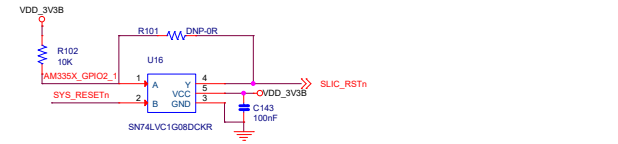
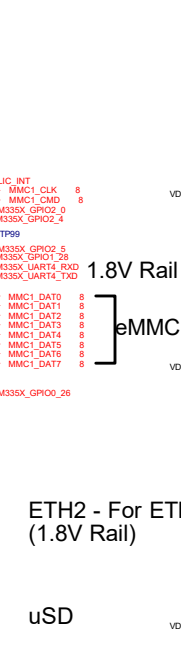
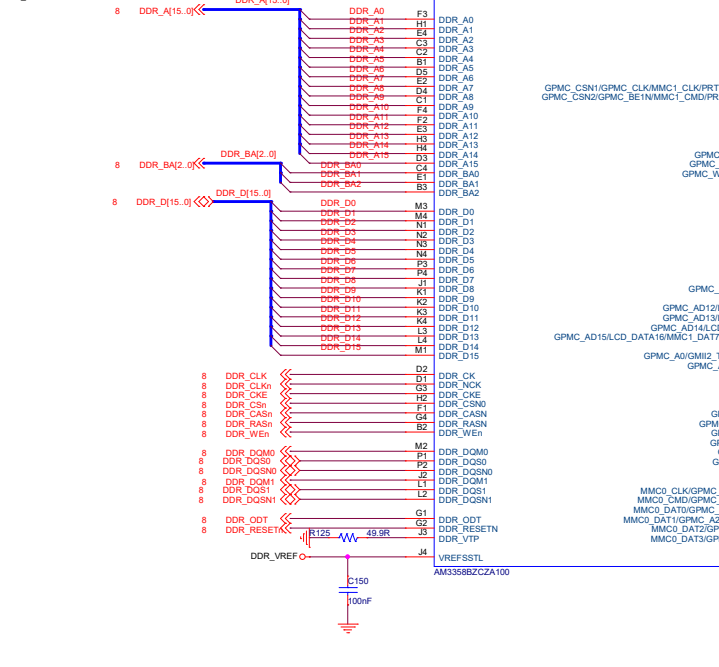
APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN : SR.CHOI - [YY/MM/DD]	CHECKED : Checker - [YY/MM/DD]		
APPROVED: Approver - [YY/MM/DD]	TITLE: IRIDIUM BDU		
ENGINEER : SR.CHOI - [YY/MM/DD]	SIZE: A3	DWG NO. <Doc>	REV A
ARTWORK : HY.PARK - [YY/MM/DD]	DATE: Wednesday, February 19, 2020	SHEET 7 OF 25	

20190827-Clock Divider Circuit modified
20200219- Clock Divider was deleted



SubArctic AM335x

15mm x 15mm Package



APPROVALS	DRAMM : SR.CHOI - [18/05/28]
CHECKED :	
APPROVED:	
ENGINEER : SR.CHOI - [18/05/28]	
ARTWORK :	

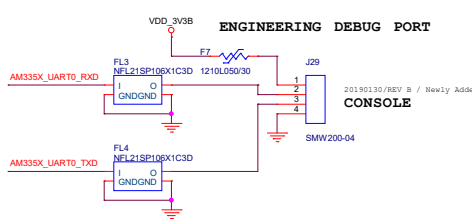
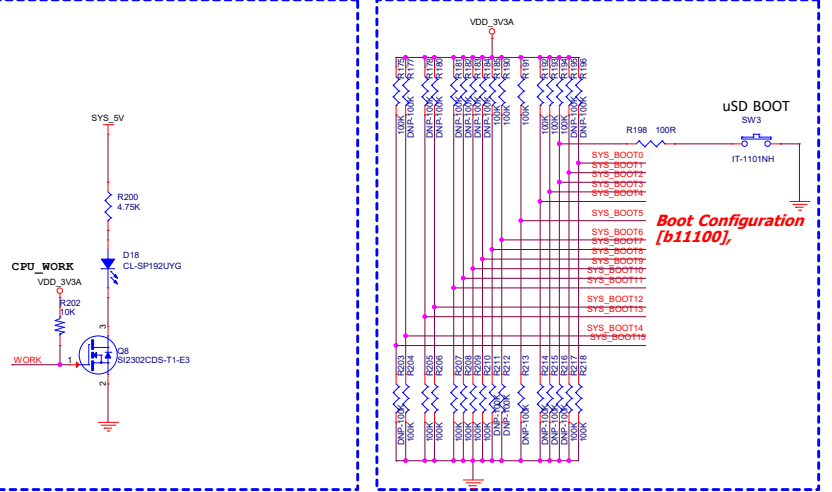
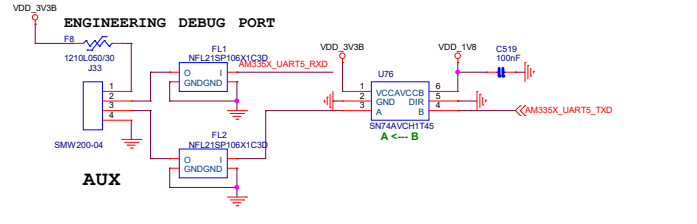
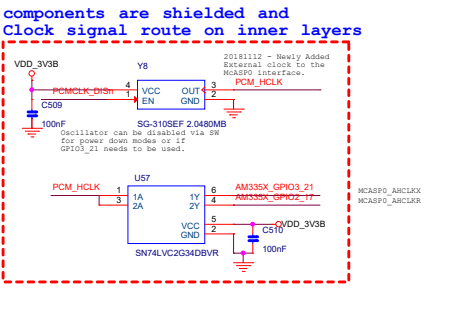
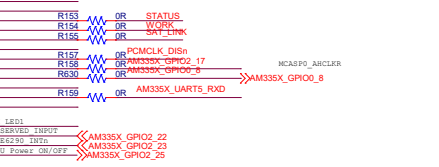
Intellian Intellian Technologies, Inc.
Innovation Centre, Global HQ
18-7, Jinwisandan-ro, Jinwi-myeon,
Pyeongtaek-si, Gyeonggi-do, 451-862 Korea

TITLE: **IRIDIUM CERTUS C700 BDU**

SIZE	00004	REV	B
A3	04. CPU AM335x 1/3		
DATE:	Wednesday, February 19, 2020	SHEET	8 OF 25



ETH1, SPI1, SMI, UART5_TXD (1.8V Rail)



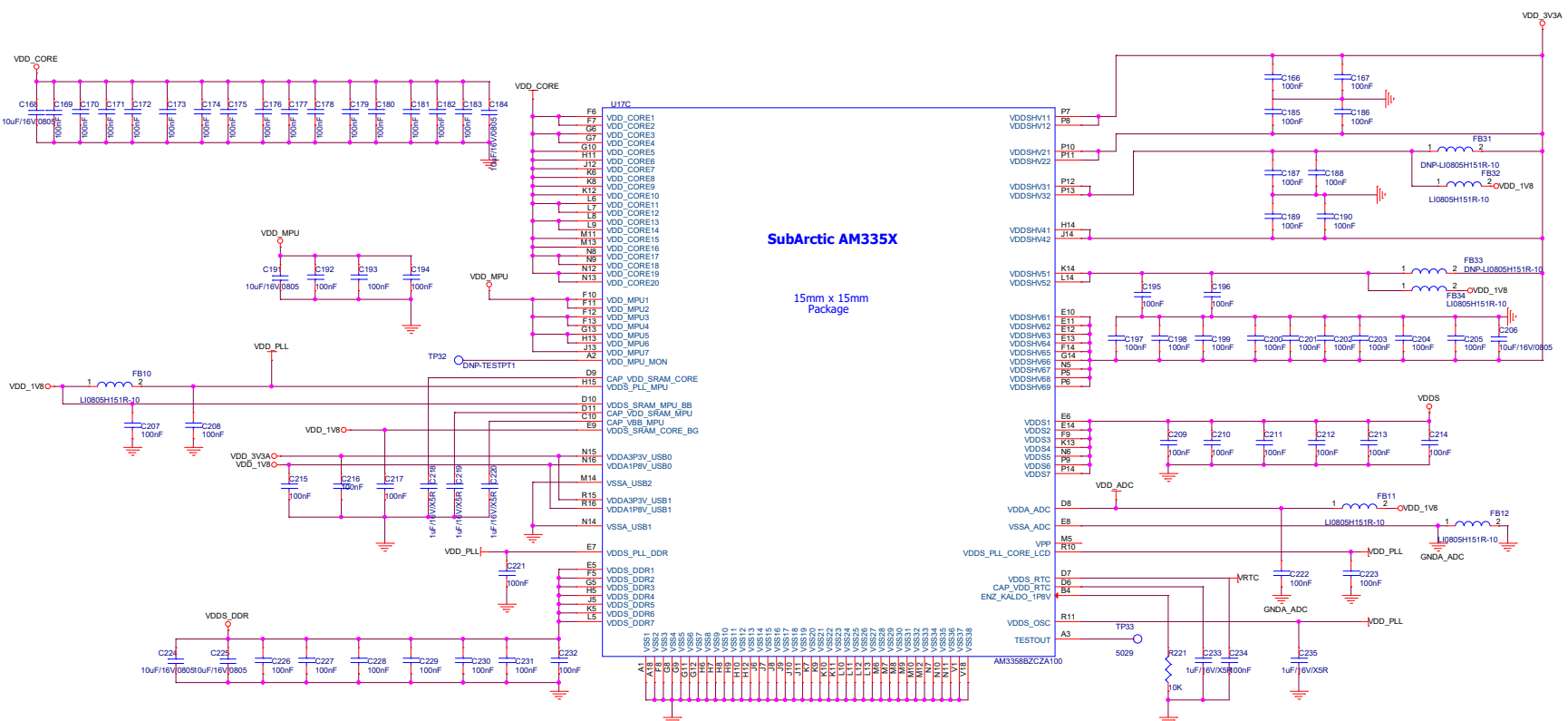
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DRAWN	SR.CHOI - [18/09/12]	
CHECKED		
APPROVED		
ENGINEER	SR.CHOI - [18/05/28]	
ARTWORK		

Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea


Intellian

TITLE: IRIDIUM Certus BDU

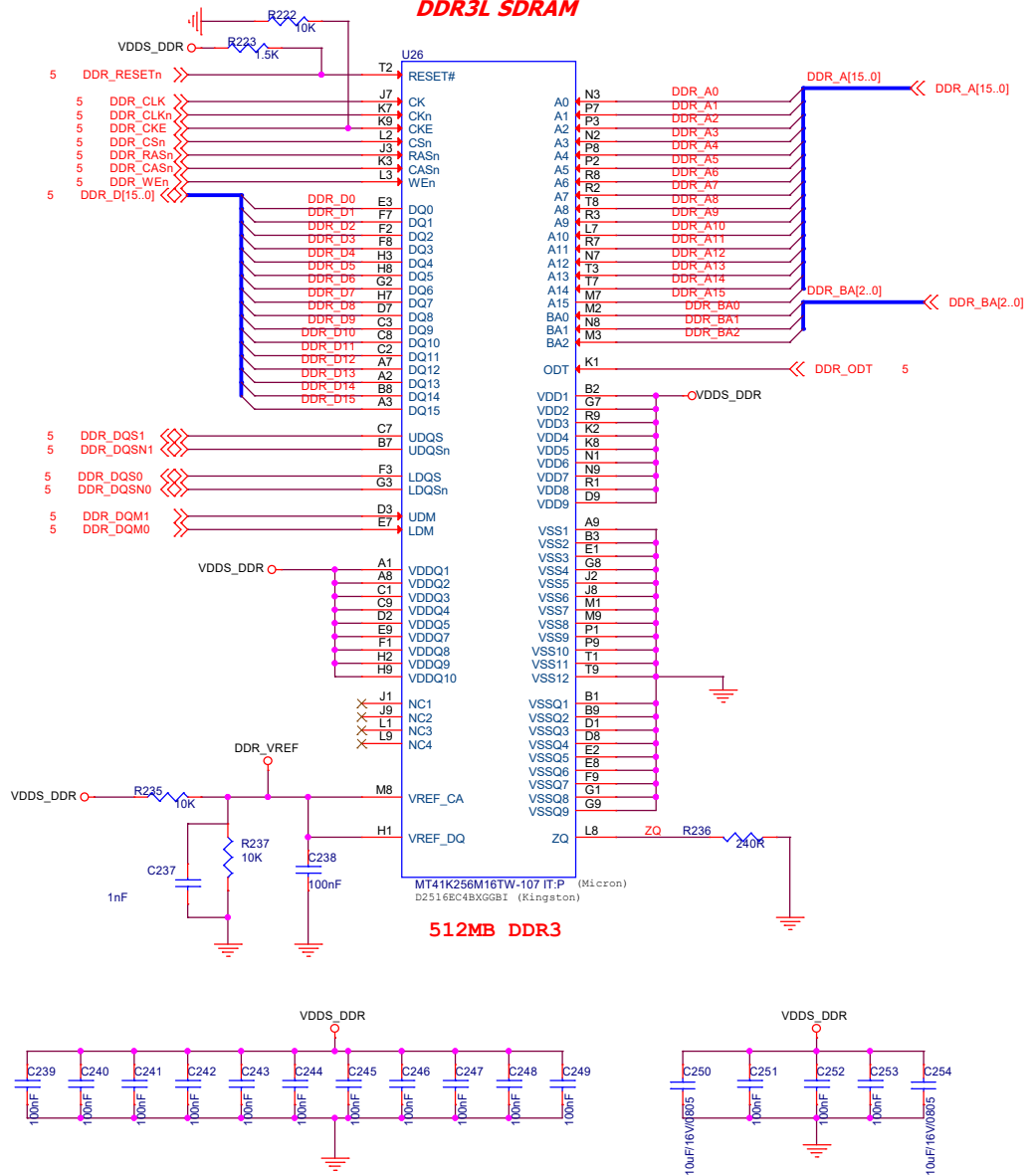
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A3	07_CPU AM335x 2/3	A	
DATE:	Monday, February 24, 2020	SHEET	9 OF 25



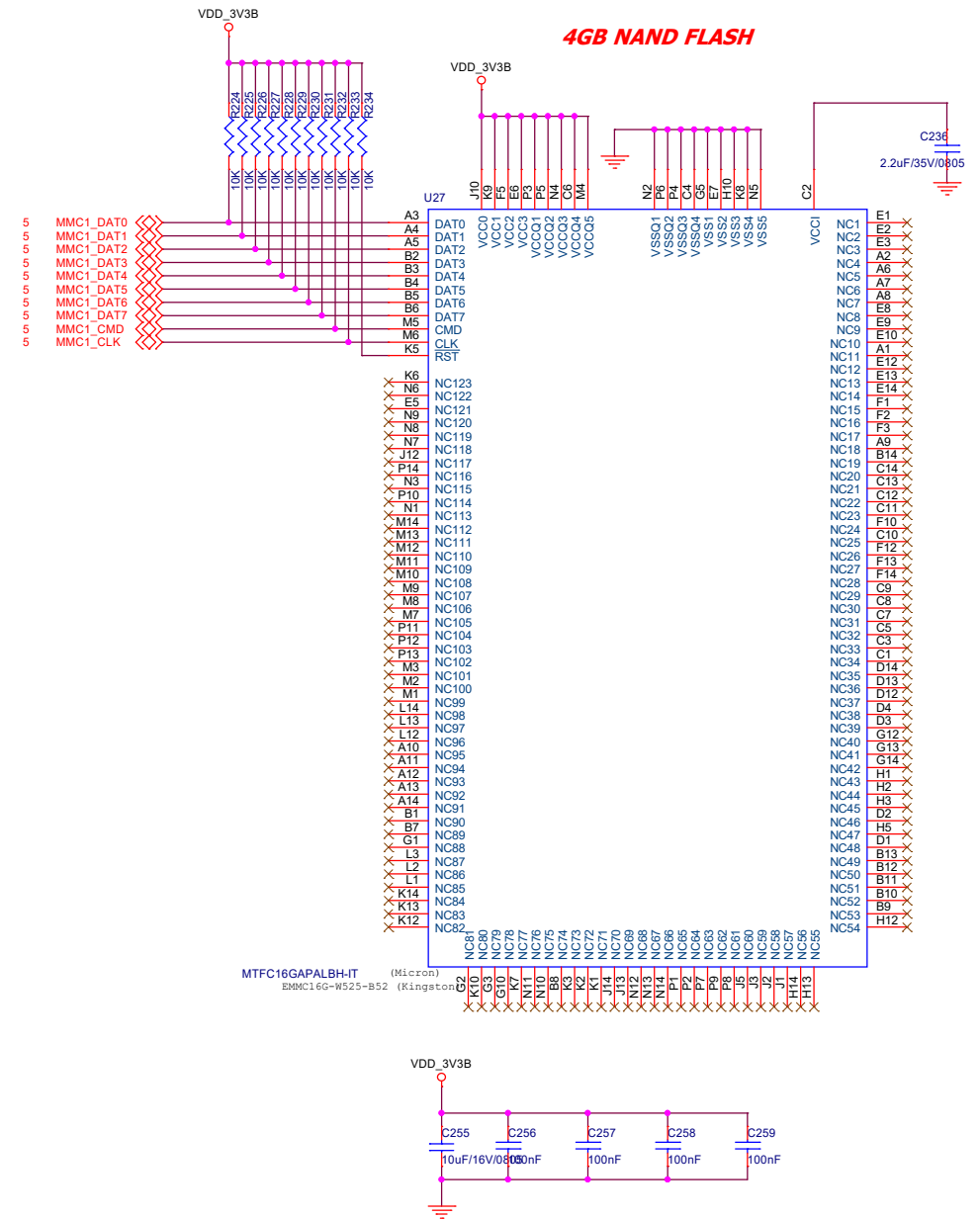
SubArctic AM335X
15mm x 15mm Package

APPROVALS		 Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwi-sandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN :	SR.CHOI - [18/05/20]		
CHECKED :			
APPROVED :			
ENGINEER :	SR.CHOI - [18/05/20]		
ARTWORK :		TITLE: IRIDIUM BDU	
SIZE	DWG NO.	REV	
A3	00006	B	
DATE: Wednesday, February 19, 2020		SHEET 10 OF 25	

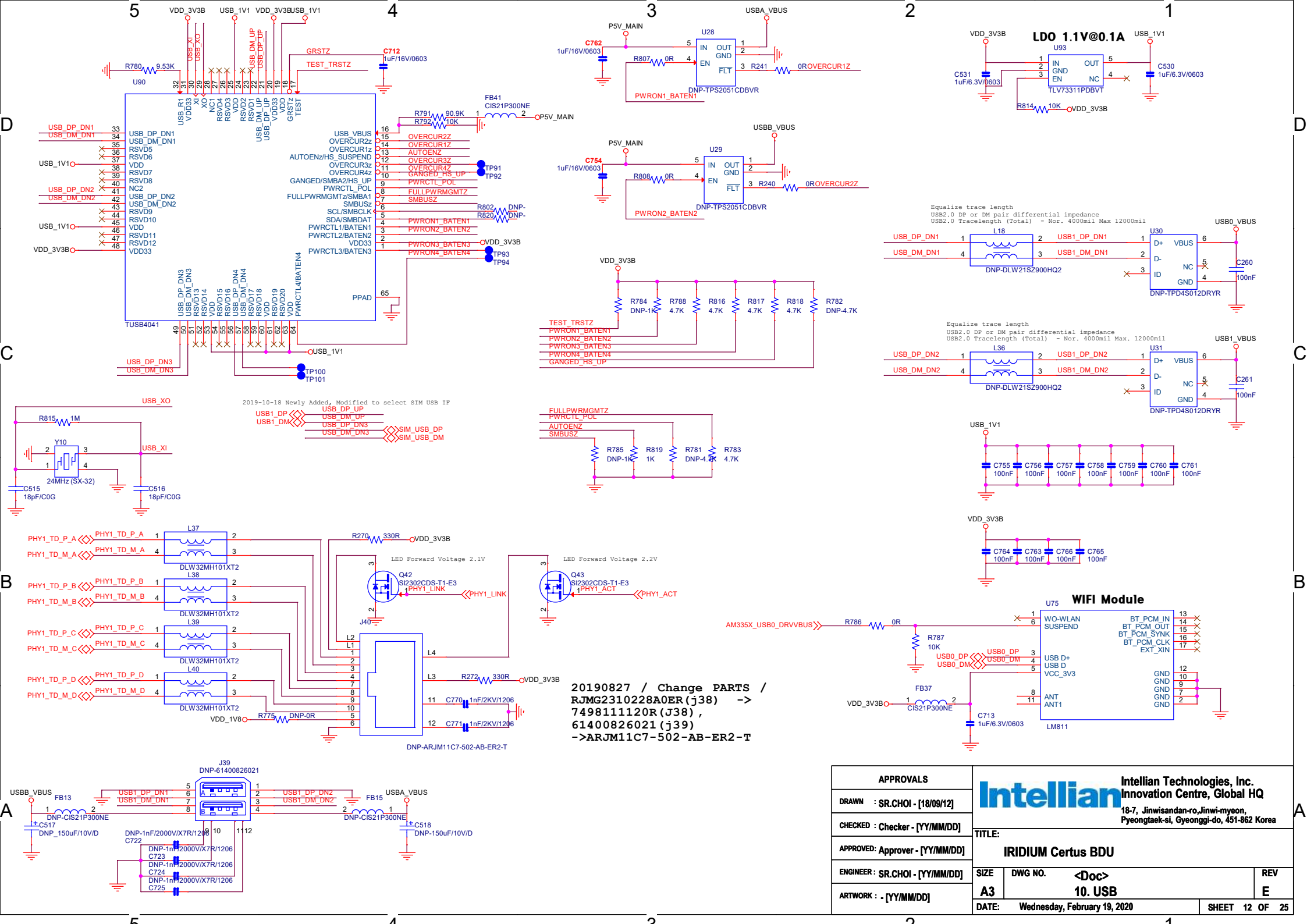
DDR3L SDRAM



4GB NAND FLASH



APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN : SR.CHOI - [18/09/10]			
CHECKED :		TITLE:	
APPROVED:		IRIDIUM CERTUS C700 BDU	
ENGINEER : SR.CHOI - [18/09/10]		SIZE	DWG NO. 00007
ARTWORK :		REV A	
DATE: Wednesday, February 19, 2020		SHEET 11 OF 25	



2019-10-18 Newly Added, Modified to select SIM USB IF

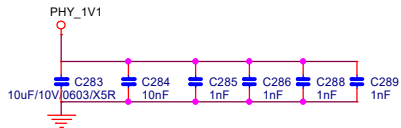
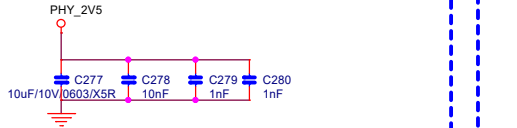
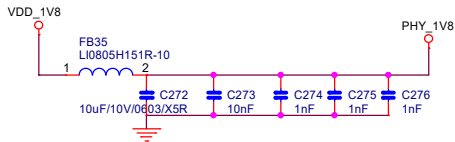
USB1_DP UP
 USB1_DM UP
 USB1_DP_DN3
 USB1_DM_DN3
 SIM_USB_DP
 SIM_USB_DM

FULLPWRMGMTZ
 PWRCTL_POL
 AUTOENZ
 SMBUSZ

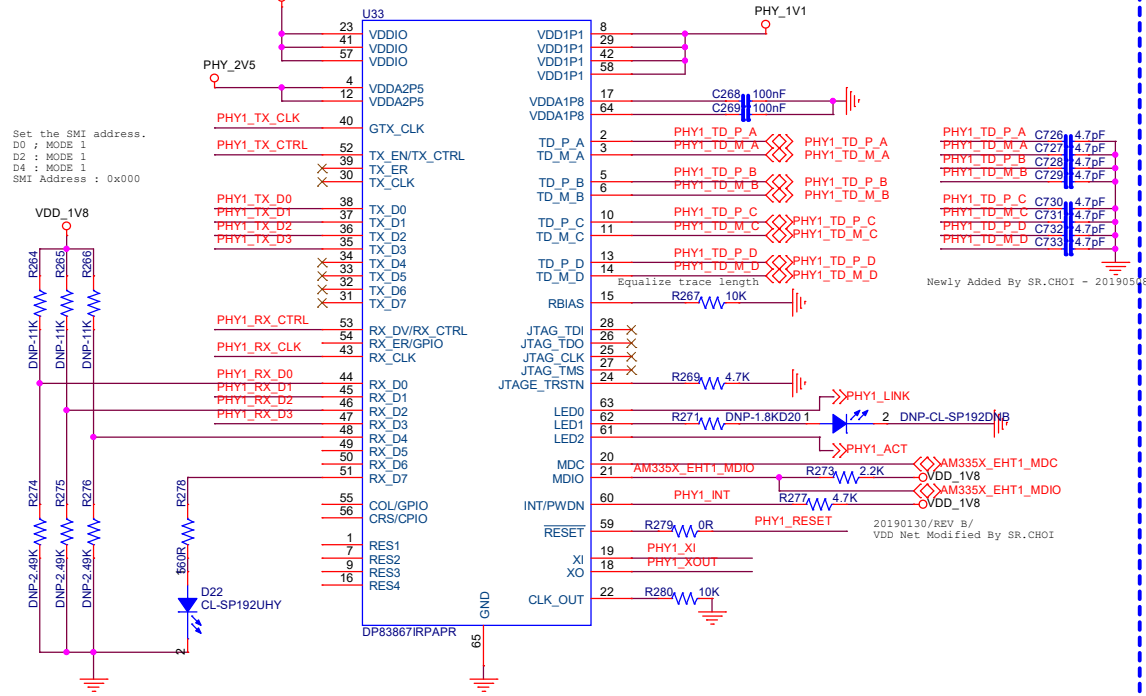
20190827 / Change PARTS /
 RJMG2310228A0ER (j38) ->
 7498111120R (J38) ,
 61400826021 (j39)
 ->ARJM11C7-502-AB-ER2-T

APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN	: SR.CHOI - [18/09/12]		
CHECKED	: Checker - [YY/MM/DD]	TITLE:	
APPROVED	: Approver - [YY/MM/DD]	IRIDIUM Certus BDU	
ENGINEER	: SR.CHOI - [YY/MM/DD]	SIZE	DWG NO. <Doc>
ARTWORK	: - [YY/MM/DD]	A3	10. USB
		DATE: Wednesday, February 19, 2020	REV E
		SHEET 12	OF 25

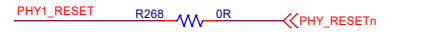
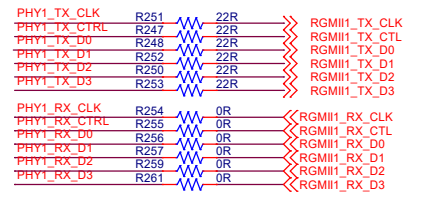
PYH1_POWER



PHY1 CHIP (Addr : 0x00)

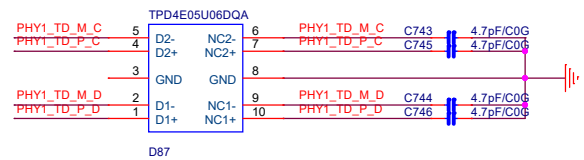
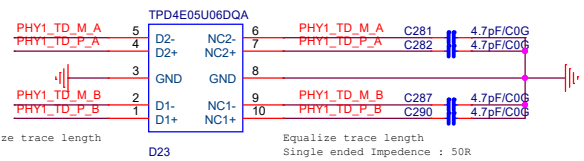
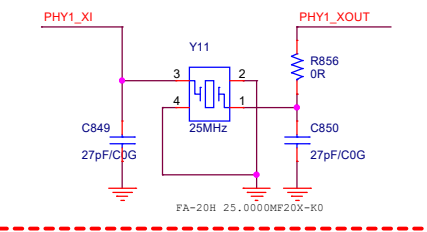


PHY1 OFF PAGE NET NAME



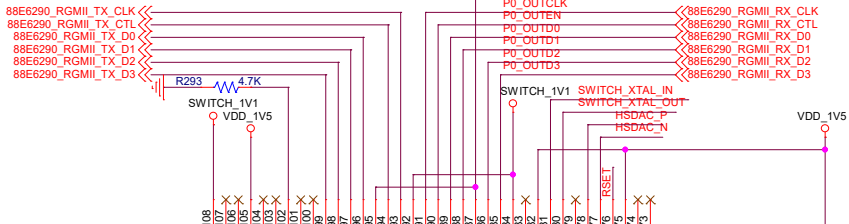
STRAP Modified By SR.CHOI - 20180523
 Delete PHY_RX1588 , PHY_TX1588 NET

2020-02-19



Beginning of VDDA2P5 ramp up to VDDA1P8 stable -> 25ms
 There is no sequencing requirement for other supplies when operating in threesupply mode.

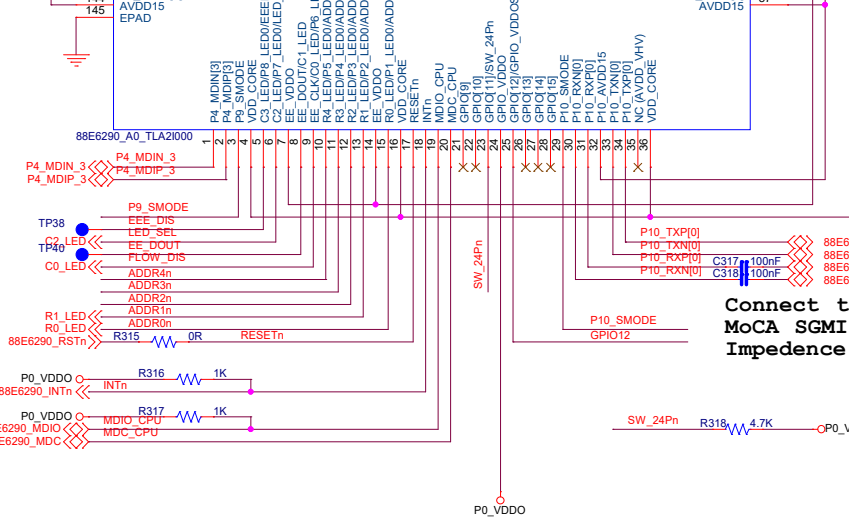
APPROVALS		Intellian Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea		
DRAWN :	SR.CHOI - [18/05/28]			
CHECKED :		TITLE:		
APPROVED:		OneWeb_AIM (Antenna Interface Module)		
ENGINEER :	SR.CHOI - [18/05/28]	SIZE	DWG NO. 00010	REV
ARTWORK :		A3	10. GIGA_EHT1	B
		DATE: Wednesday, February 19, 2020	SHEET 13 OF 25	



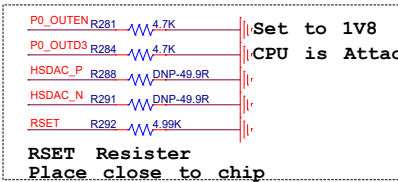
**REAR Ports
10/100 Mbps**

- P1_MDIP_0 P1_MDIP_0
- P1_MDIN_0 P1_MDIN_0
- P1_MDIP_1 P1_MDIP_1
- P1_MDIN_1 P1_MDIN_1
- P1_MDIP_2 P1_MDIP_2
- P1_MDIN_2 P1_MDIN_2
- P1_MDIP_3 P1_MDIP_3
- P1_MDIN_3 P1_MDIN_3
- P2_MDIP_0 P2_MDIP_0
- P2_MDIN_0 P2_MDIN_0
- P2_MDIP_1 P2_MDIP_1
- P2_MDIN_1 P2_MDIN_1
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- P4_MDIN_1 P4_MDIN_1
- P4_MDIP_2 P4_MDIP_2
- P4_MDIN_2 P4_MDIN_2

Peridot - 144 LQFP

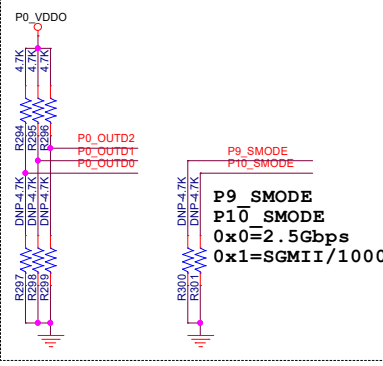


Connect to
MoCA SGMII I/F
Impedance : Sigle ended :50R

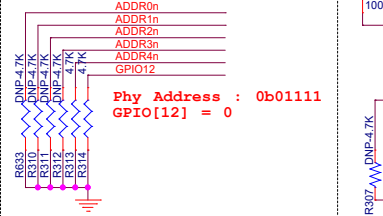


RSET Resister
Place close to chip

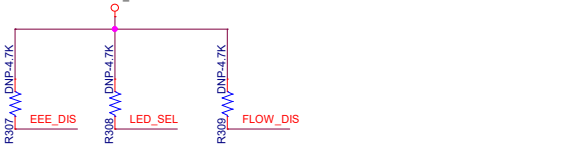
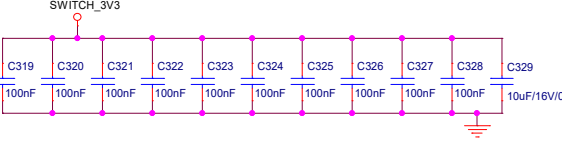
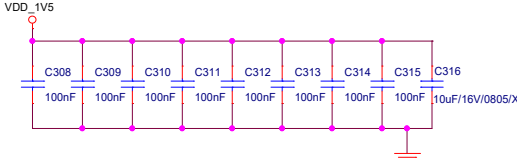
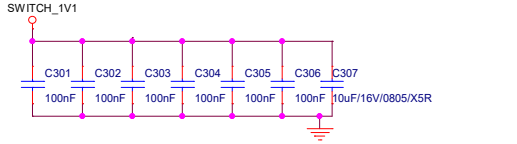
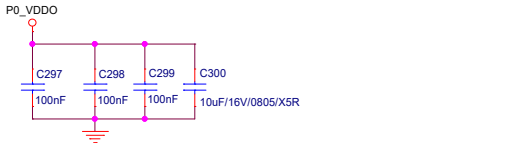
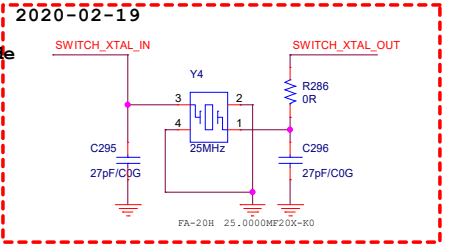
Port 0 Configuration Summary
PO_OUTn[2:0]
= 0b000 : Full Duplex MII PHY
= 0b001 : MII PHY
= 0b010 : MII MAC
= 0b100 : RMII PHY
= 0b101 : RMII MAC
= 0b110 : Disabled
= 0b111 : RGMII



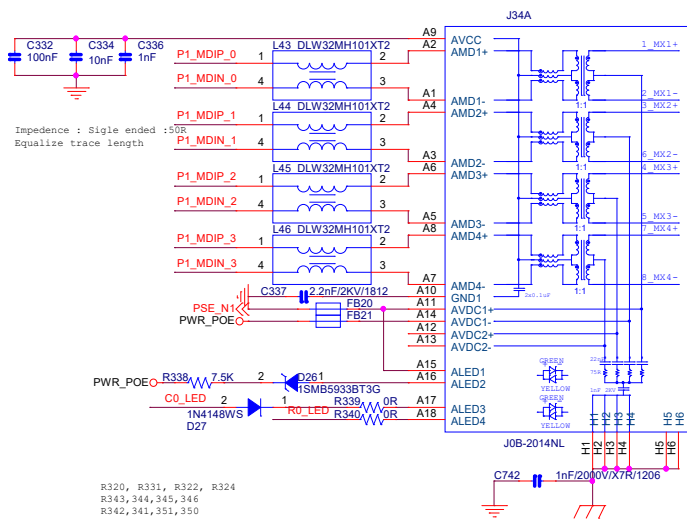
ADDR[4:0] sets
the device's
SMI address.
(INVERTED Value)



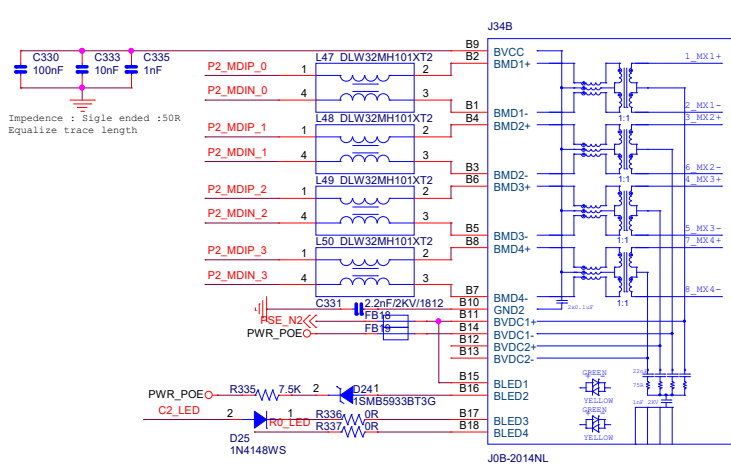
Phy Address : 0b01111
GPIO[12] = 0



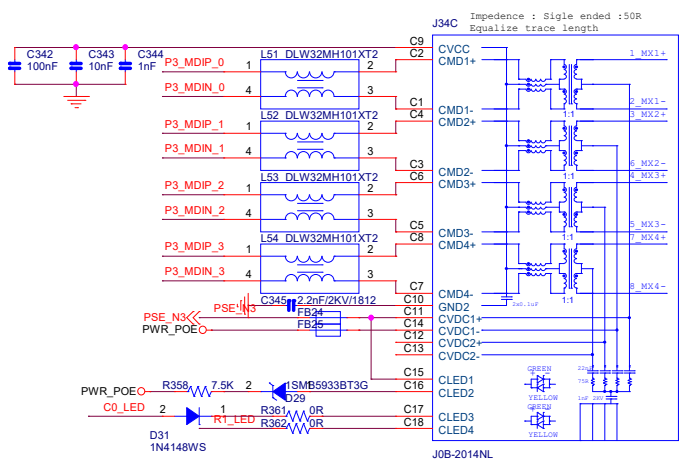
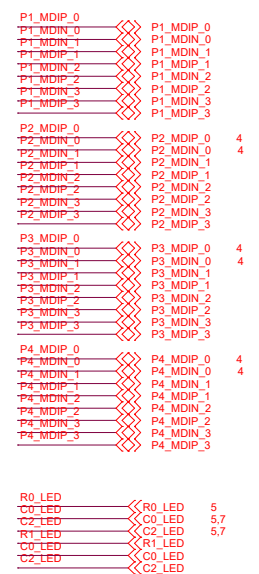
APPROVALS		Intellian	Intellian Technologies, Inc. Innovation Centre, Global HQ	
DRAWN :	SH.CHO - [18/01/22]		18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
CHECKED :		TITLE:		REV
APPROVED:		New Ethernet Switch (88E6290)		A
ENGINEER :	SH.CHO - [18/01/22]	SIZE	DWG NO.	
ARTWORK :		A3	02-ETH Switch Main	
		DATE:	Wednesday, February 19, 2020	SHEET 14 OF 25



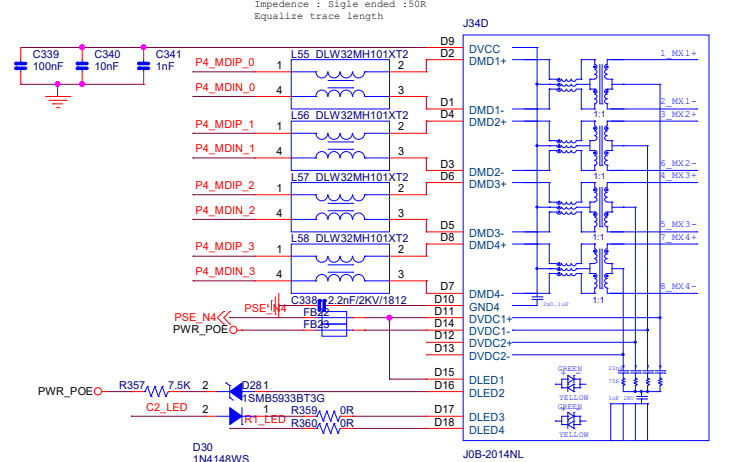
R320, R331, R322, R324
R343, 344, 345, 346
R342, 341, 351, 350



Impedance : Single ended :50R
Equalize trace length



Impedance : Single ended :50R
Equalize trace length



Impedance : Single ended :50R
Equalize trace length

APPROVALS		Intellian Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN : SH.CHO - [18/01/22]			
CHECKED :		TITLE:	
APPROVED:		New Ethernet Switch (88E6290)	
ENGINEER : SH.CHO - [18/01/22]		SIZE	REV
ARTWORK :		DWG NO. 13. 88E6290 ETH Ports 1	E
		DATE: Wednesday, February 19, 2020	SHEET 15 OF 25

CONFIG SWITCH	OFF	ON
1 OPERATION MODE	+1	0
2 JTAG SELECT	+ENABLE	DISABLE
3 DVS ENABLE	+ENABLE	DISABLE
4 MMI 0	MAC	+PHY
5 PHY_ADDR[3]	0	+1
6 PHY_ADDR[2]	0	+1
7 PHY_ADDR[1]	0	+1
8 PHY_ADDR[0]	+1	0

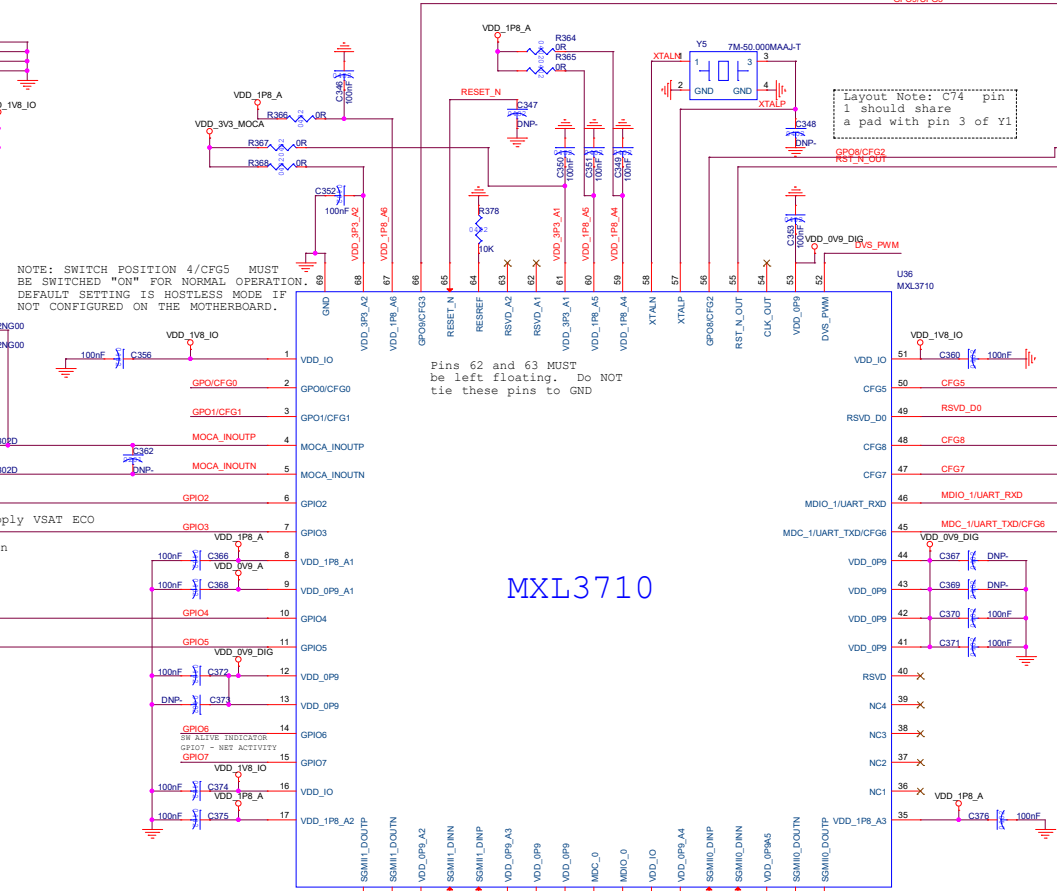
*Default Setting

CFG5	CFG7	CFG8	CFG9	GPIO0/CFG3	GPIO0/CFG2	GPIO1/CFG1	GPIO3/CFG4	GPIO3/CFG5
R347	R348	R349	R350	R351	R352	R353	R354	R355
DNP-1K	DNP-1K	DNP-1K	DNP-1K	DNP-1K	DNP-1K	DNP-1K	DNP-1K	DNP-1K

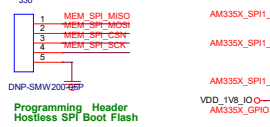
NOTE: SWITCH POSITION 4/CFG5 MUST BE SWITCHED "ON" FOR NORMAL OPERATION. DEFAULT SETTING IS HOSTLESS MODE IF NOT CONFIGURED ON THE MOTHERBOARD.

Pins 62 and 63 MUST be left floating. Do NOT tie these pins to GND

MXL3710

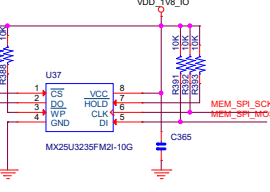


Hostless SPI Boot Flash - 32 Mbit SPI NOR Flash

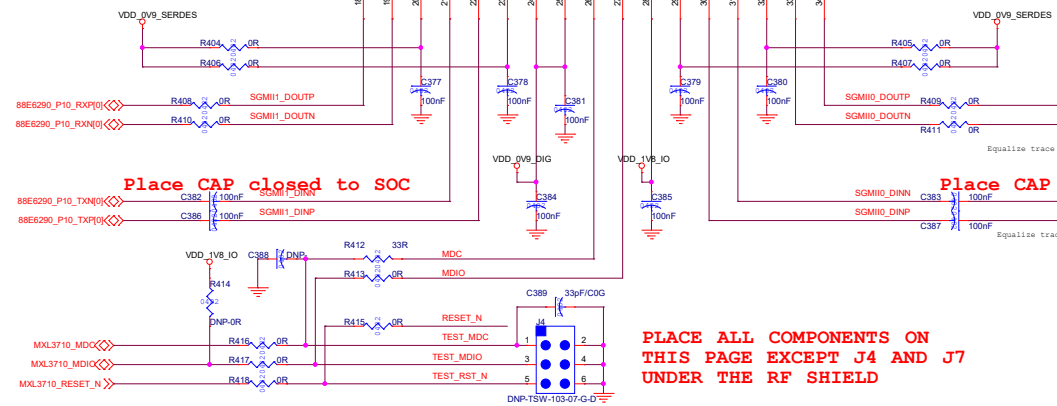


2019-04-22 Newly added
2019-0619 Added Sel Ctrl

FLASH MEMORY



(logic low = SxA to Dx, logic high = SxB to Dx).



Place CAP closed to SOC

Place CAP closed to SOC

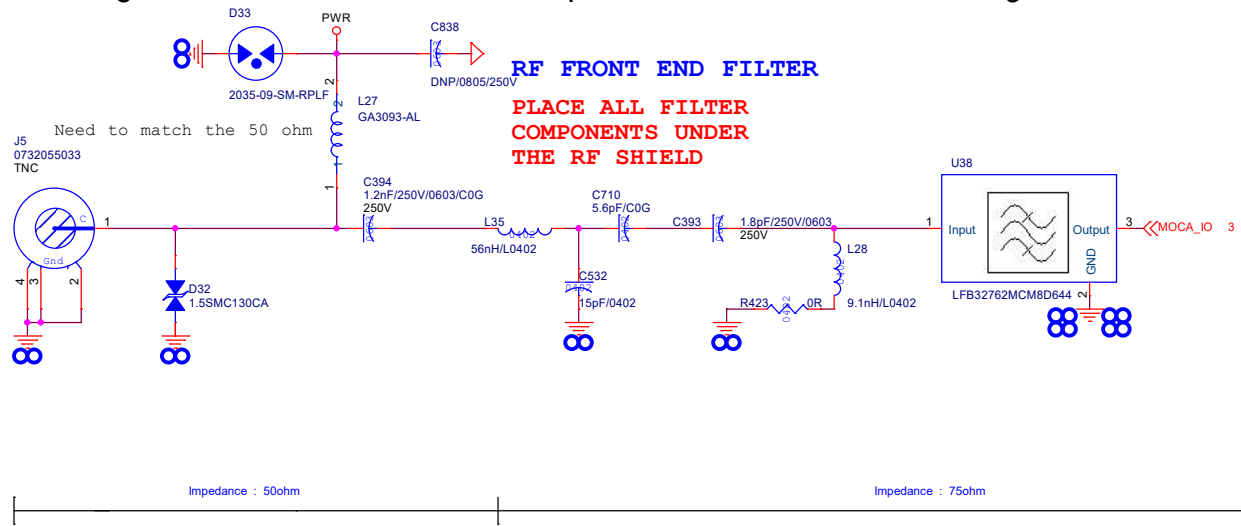
PLACE ALL COMPONENTS ON THIS PAGE EXCEPT J4 AND J7 UNDER THE RF SHIELD

SILKSCREEN NOTE:

MDC	GND
MDIO	GND
RESET N	GND

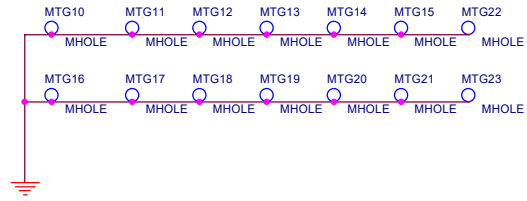
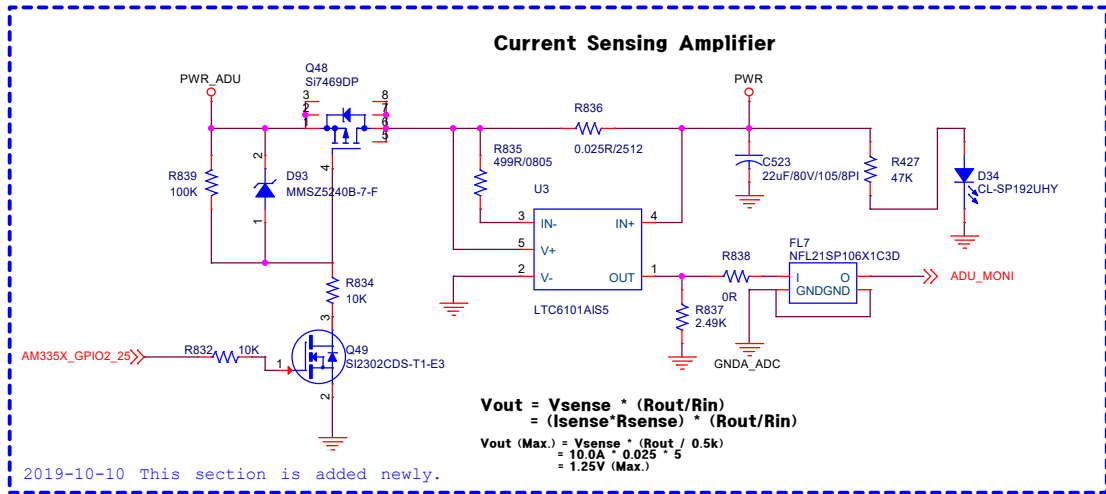
To hold MXL3710 in reset, install a jumper across pins 5 and 6 on J4. This may be used for programming the SPI Flash during hostless operation

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DRAWN : SR.CHOI - [YY/MM/DD]		Innovation Centre, Global HQ	
CHECKED : Checker - [YY/MM/DD]		18-7, Jimulsandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
APPROVED: Approver - [YY/MM/DD]		TITLE:	<Title>
ENGINEER : SR.CHOI - [YY/MM/DD]	SIZE	DWG NO.	<Doc>
ARTWORK : HY.PARK - [YY/MM/DD]	A3	DATE:	[DRAWING_NAME]
		Wednesday, February 19, 2020	REV A
			SHEET 16 OF

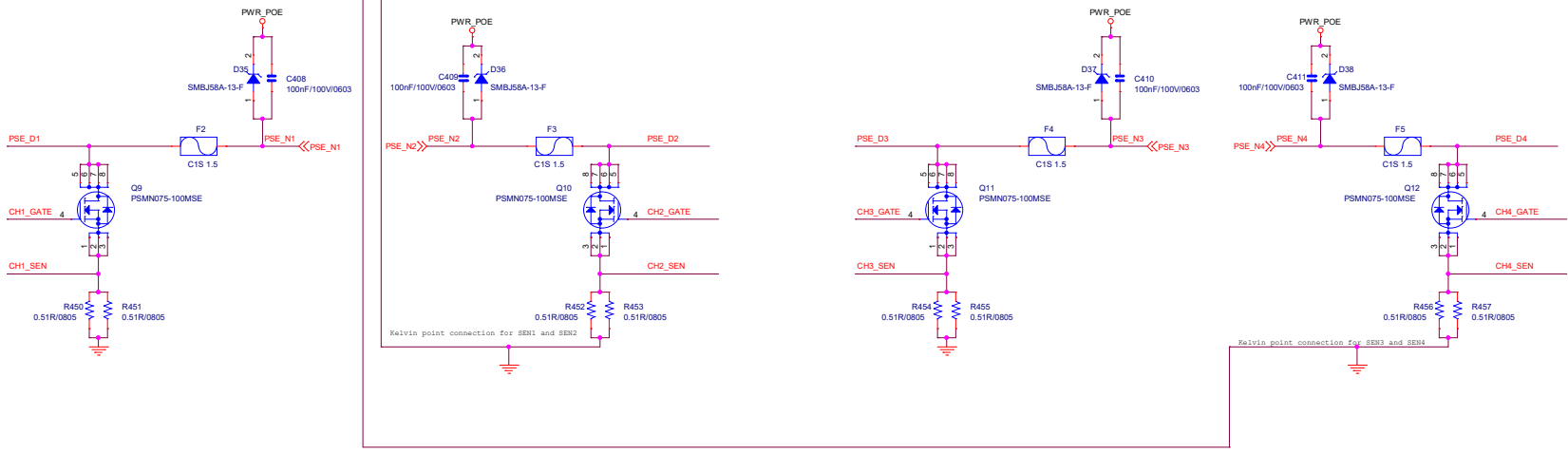
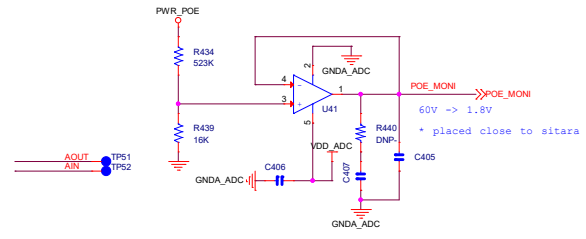
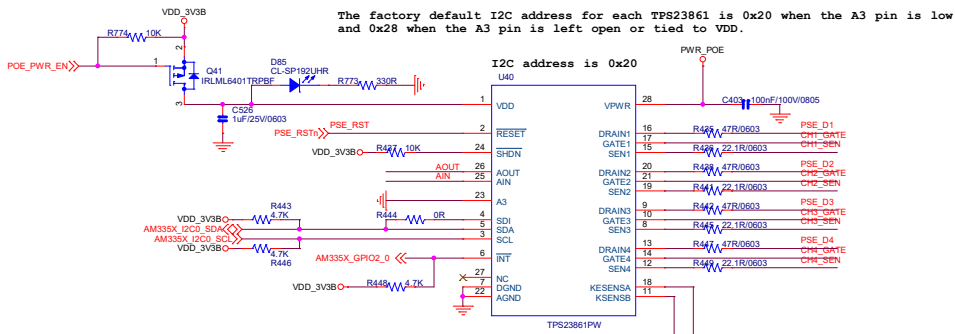


SILKSCREEN
NOTE:
COMMON IN

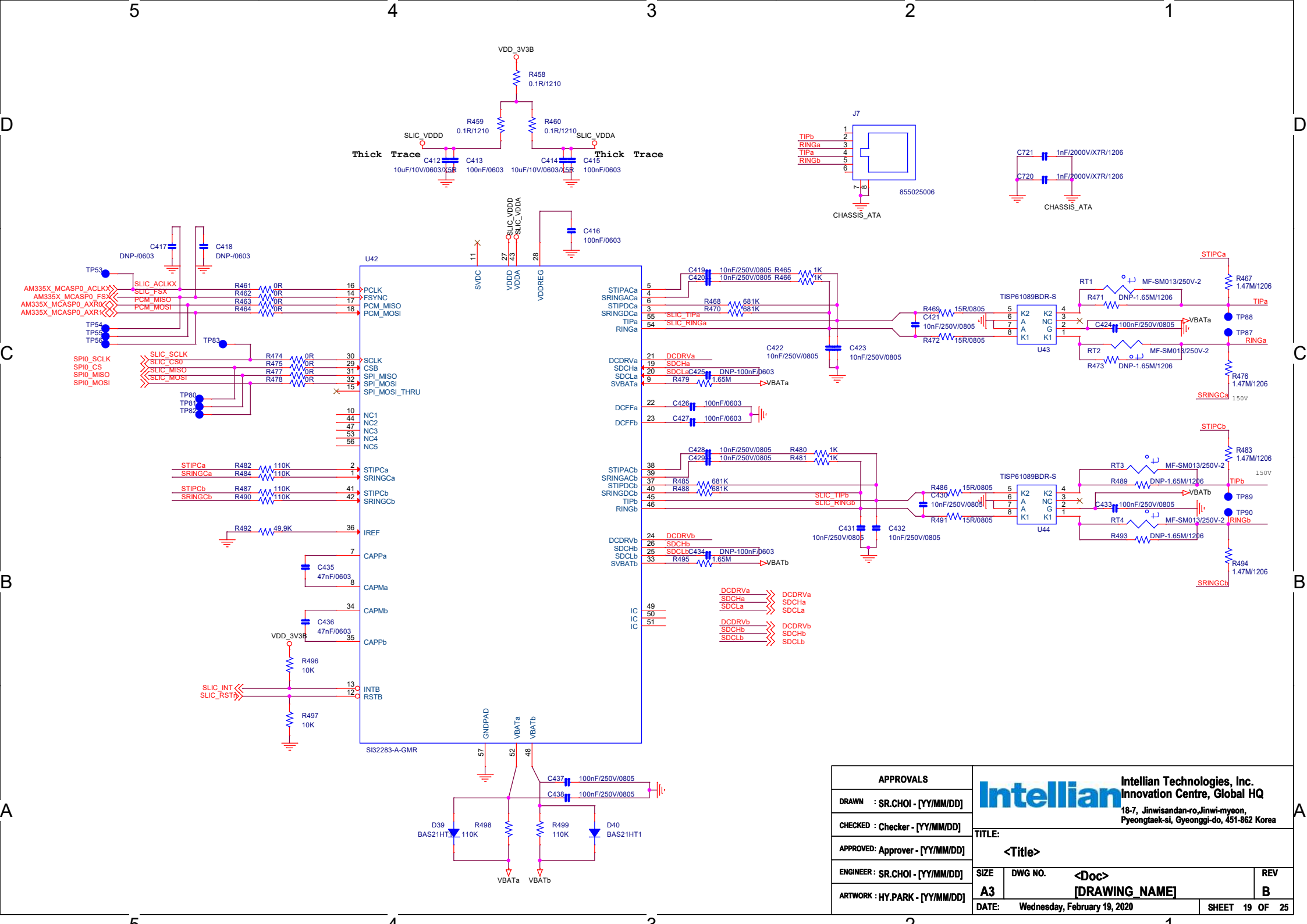
⊗ Denotes multiple, isolated, GND vias



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DRAWN : SR.CHOI - [YY/MM/DD]				
CHECKED : Checker - [YY/MM/DD]		TITLE:		
APPROVED: Approver - [YY/MM/DD]		<Title>		
ENGINEER : SR.CHOI - [YY/MM/DD]		SIZE	DWG NO. <Doc>	REV
ARTWORK : HY.PARK - [YY/MM/DD]		A3	15. MoCA RF Interface	B
DATE: Monday, February 24, 2020		SHEET 17 OF 25		

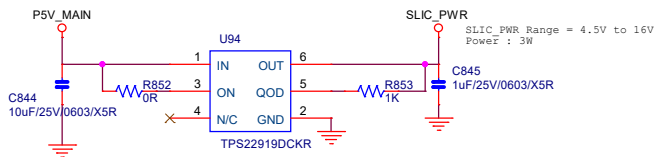


APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jimuisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea		
DRAWN	: SR.CHOI - [19/06/14]			
CHECKED	: Checker - [YY/MM/DD]	TITLE:		
APPROVED	: Approver - [YY/MM/DD]	<Title>		
ENGINEER	: SR.CHOI - [YY/MM/DD]	SIZE	DWG NO.	REV
ARTWORK	: [YY/MM/DD]	A3	18.PoE	B
DATE: Wednesday, February 19, 2020		SHEET 18 OF		

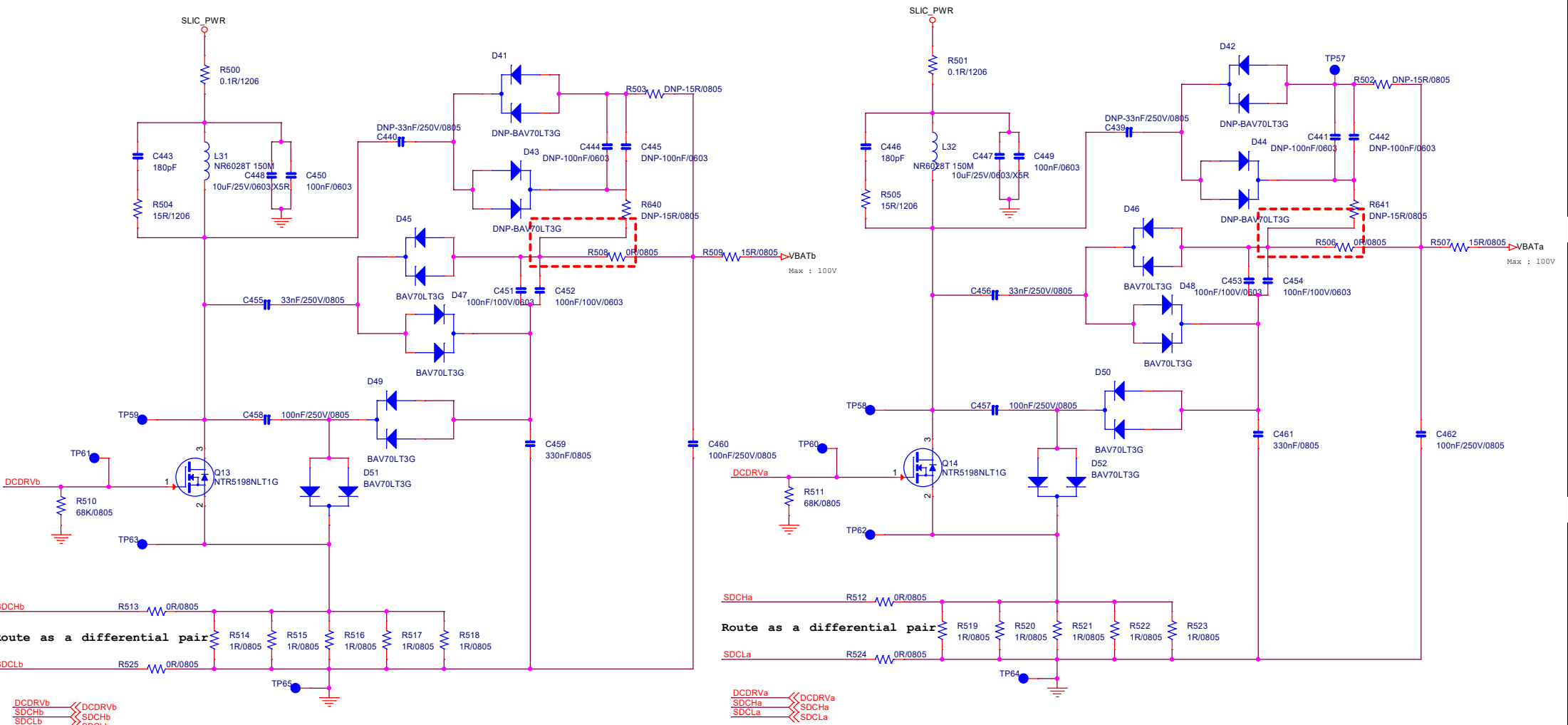


APPROVALS		Intellian Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN : SR.CHOI - [YY/MM/DD]			
CHECKED : Checker - [YY/MM/DD]		TITLE: <Title>	
APPROVED: Approver - [YY/MM/DD]		SIZE: A3	DWG NO. <Doc>
ENGINEER : SR.CHOI - [YY/MM/DD]		[DRAWING_NAME]	
ARTWORK : HY.PARK - [YY/MM/DD]		DATE: Wednesday, February 19, 2020	REV: B
		SHEET 19	OF 25

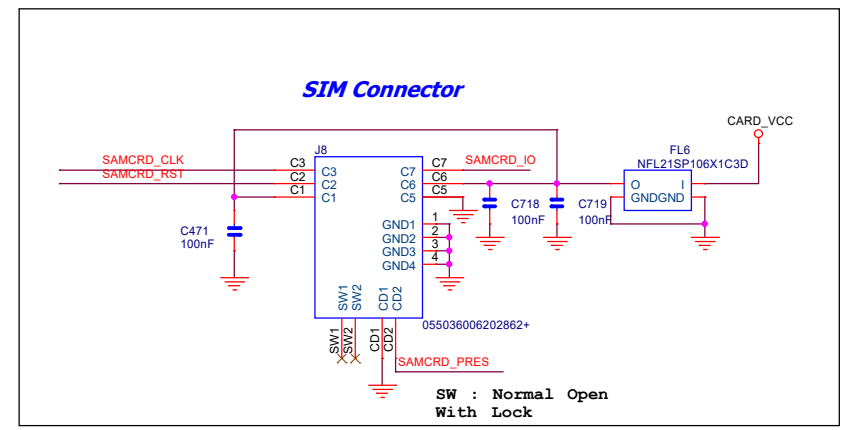
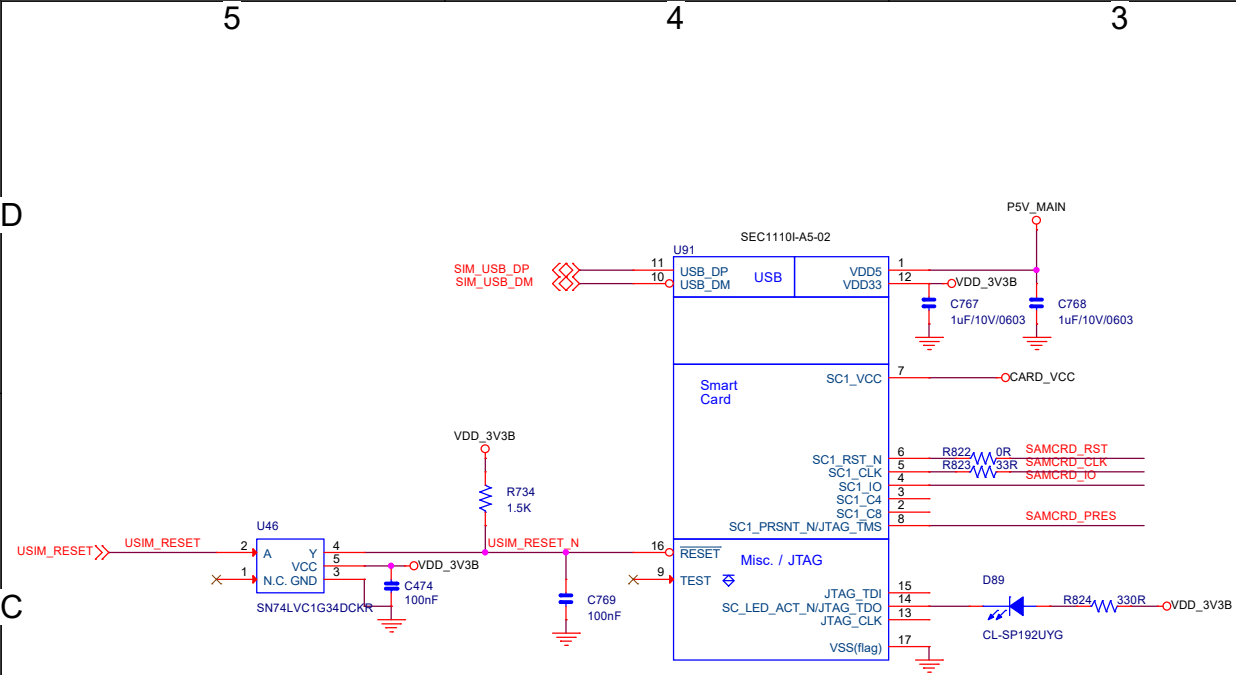
20200217- Changed B6 to U94 for power protection



SLIC_PWR Range = 4.5V to 16V

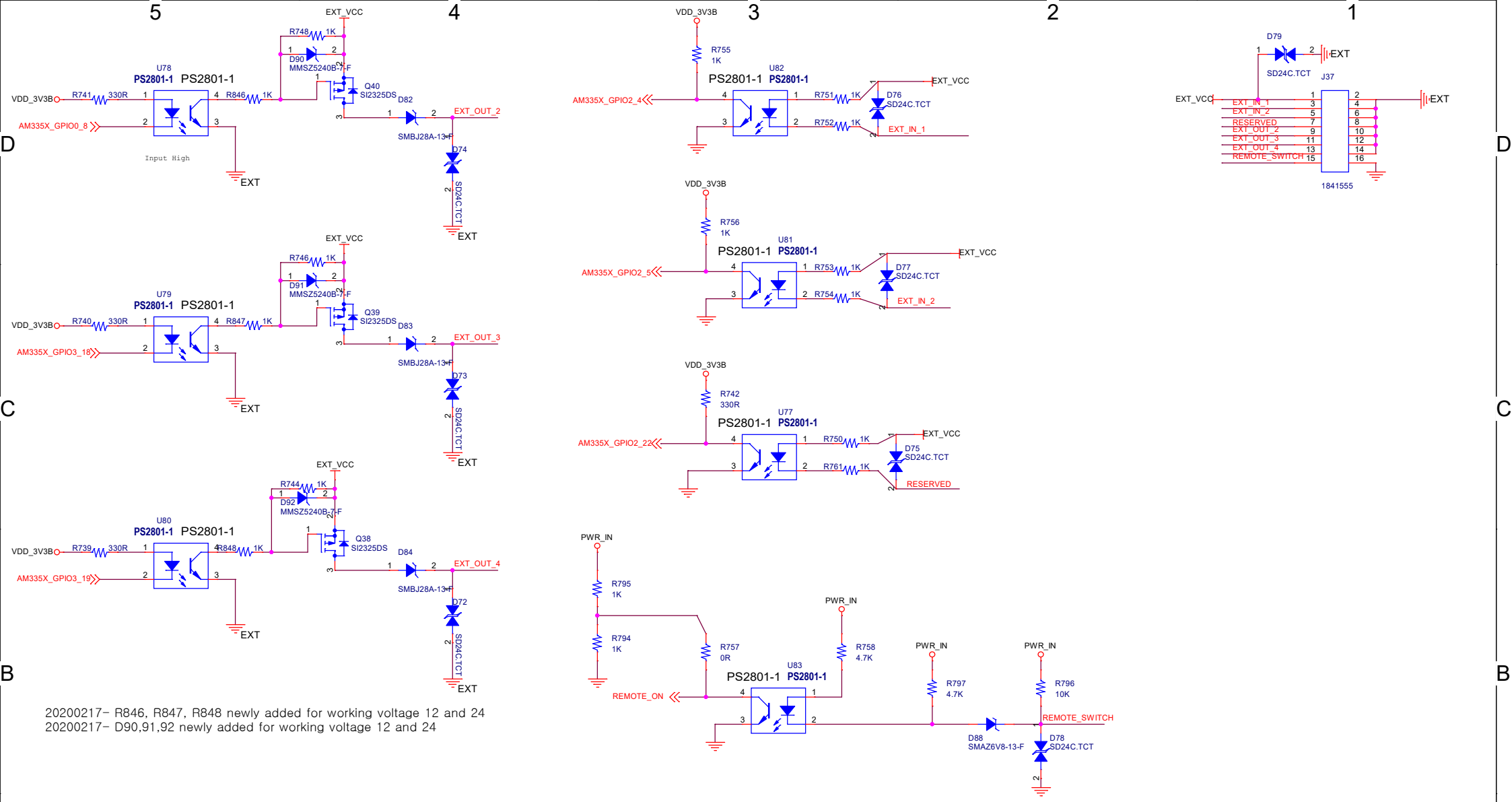


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DRAWN	: SR.CHOI - [YY/MM/DD]			
CHECKED	: Checker - [YY/MM/DD]	TITLE:		
APPROVED	: Approver - [YY/MM/DD]	Iridium Certus BDU		
ENGINEER	: SR.CHOI - [YY/MM/DD]	SIZE	DWG NO. <Doc>	REV
ARTWORK	: HY.PARK - [YY/MM/DD]	A3	21. SLIC - DCDC	A
DATE: Wednesday, February 19, 2020		SHEET 20 OF 25		



- 20190417 - Changed UART4 to UART1
- 20190619 - Change Control IC TDA8029 to SEC1110
Reset Position move to SDWN_N
- 20190827 - Change VDD_3V3B net

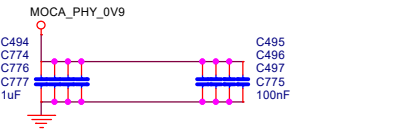
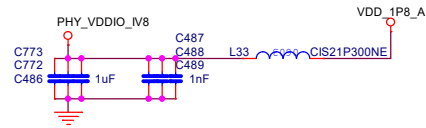
APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN	: SR.CHOI - [YY/MM/DD]		
CHECKED	: Checker - [YY/MM/DD]		
APPROVED	: Approver - [YY/MM/DD]		
ENGINEER	: SR.CHOI - [YY/MM/DD]		
ARTWORK	: HY.PARK - [YY/MM/DD]	TITLE: Iridium Certus BDU	
SIZE	DWG NO.	<Doc>	REV
A3	[DRAWING_NAME]		B
DATE:	Wednesday, February 19, 2020		SHEET 21 OF 25



20200217- R846, R847, R848 newly added for working voltage 12 and 24
 20200217- D90,91,92 newly added for working voltage 12 and 24

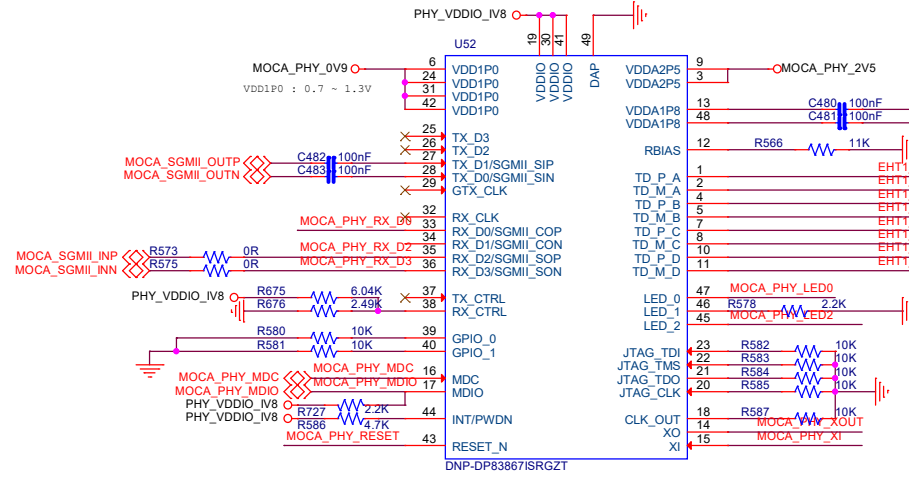
APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN : SR.CHOI - [YY/MM/DD]	CHECKED : Checker - [YY/MM/DD]		
APPROVED: Approver - [YY/MM/DD]	ENGINEER : SR.CHOI - [YY/MM/DD]	TITLE: External GPIO	
ARTWORK : HY.PARK - [YY/MM/DD]	ARTWORK : HY.PARK - [YY/MM/DD]	SIZE: A3	DWG NO. <Doc> [DRAWING_NAME]
DATE: Monday, February 24, 2020	DATE: Monday, February 24, 2020	REV: A	SHEET 22 OF 25

MOCA_PYH_POWER

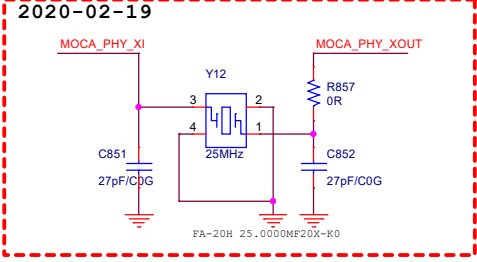


20191007- Added Decap

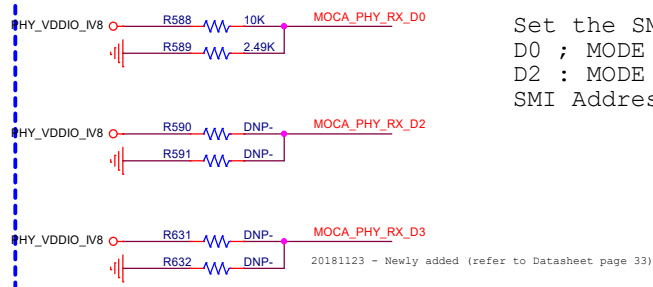
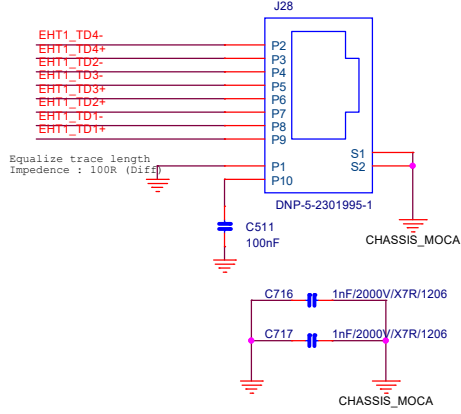
MOCA PHY



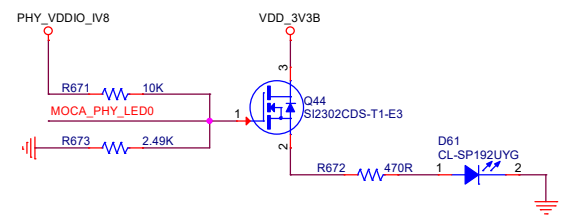
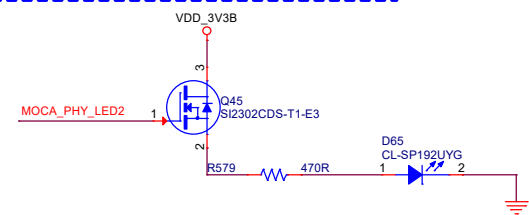
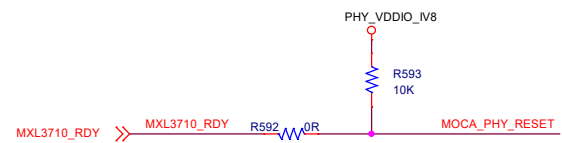
20190508-Newly Added
20190827-Delete Resistor



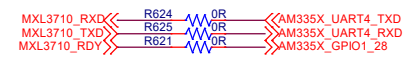
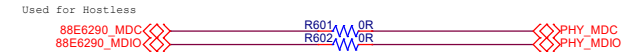
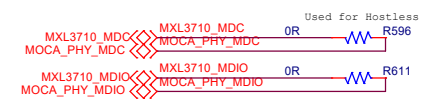
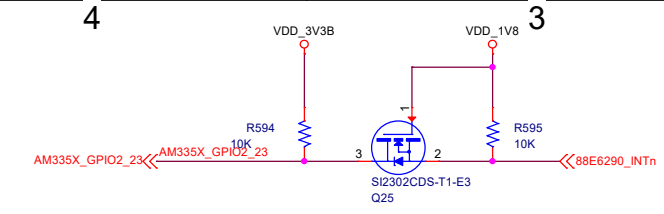
2020-02-19



Set the SMI address.
D0 ; MODE 2
D2 : MODE 1
SMI Address : 0b001



APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN : SR.CHOI - [18/09/21]			
CHECKED : SR.CHOI - [18/09/21]			
APPROVED: Approver - [YY/MM/DD]			
ENGINEER : SR.CHOI - [18/09/21]			
ARTWORK : - [YY/MM/DD]		TITLE: AIM	
SIZE	DWG NO.	REV	
A3	00001	C	
DATE: Thursday, February 20, 2020		SHEET 23 OF 25	



2020-02-18 Delete LINK_STATUS0,1 Net

APPROVALS		Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea		
DRAWN	: SR.CHOI - [YY/MM/DD]			
CHECKED	: Checker - [YY/MM/DD]			
APPROVED	: Approver - [YY/MM/DD]			
ENGINEER	: SR.CHOI - [YY/MM/DD]	TITLE: Iridium Certus BDU		
ARTWORK	: HY.PARK - [YY/MM/DD]	SIZE A3	DWG NO. <Doc> 26. LEVEL TRANSLATOR	REV A
		DATE: Wednesday, February 19, 2020	SHEET 24 OF 25	

5

4

3

2

1

D

D

C

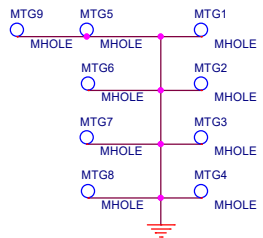
C


B

B

A

A



APPROVALS		 Intellian Technologies, Inc. Innovation Centre, Global HQ 18-7, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, 451-862 Korea	
DRAWN : SR.CHOI - [YY/MM/DD]			
CHECKED : Checker - [YY/MM/DD]			
APPROVED : Approver - [YY/MM/DD]			
ENGINEER : SR.CHOI - [YY/MM/DD]	TITLE:		
ARTWORK : HY.PARK - [YY/MM/DD]	Iridium Certus BDU		
	SIZE	DWG NO. <Doc>	REV
	A3	26. LEVEL TRANSLATOR	A
	DATE: Wednesday, February 19, 2020		SHEET 25 OF 25