

FILE

ID 302.

INTERNAL DOCUMENT 250

I.O.S.

Final Report for JRC (Ispra)

Contract No. 2236-83-11

(related DoE Contract PECD 7/9/175-153/83)

"Development of a low frequency transponder
system for penetrator instrumentation"

C.G. Flewellen

[*This document should not be cited in a published bibliography, and is supplied for the use of the recipient only.*]

NATURAL ENVIRONMENT
COUNCIL
RESEARCH
INSTITUTE OF OCEANOGRAPHIC SCIENCES

INSTITUTE OF OCEANOGRAPHIC SCIENCES

Wormley, Godalming,
Surrey GU8 5UB
(042-879-4141)

(Director: Dr. A. S. Laughton, FRS)

Bidston Observatory,
Birkenhead,
Merseyside L43 7RA
(051-653-8633)

(Assistant Director: Dr. D. E. Cartwright, FRS)

Final Report for JRC (Ispra)
Contract No. 2236-83-11
(related DoE Contract PECD 7/9/175-153/83)

"Development of a low frequency transponder
system for penetrator instrumentation"

C.G. Flewellen

INTERNAL DOCUMENT NO. 250
1985

Institute of Oceanographic Sciences,
Wormley, Godalming, Surrey GU8 5UB

Contents

1. Project Title
2. Objectives
3. Introduction
4. Technical Status
 - 4.1 General
 - 4.2 Transponder Design
 - 4.3 Shipborne System
 - 4.4 Sea Trials
5. Conclusions and Recommendations for Further Development

- Annex A. Transponder Design
- Appendix A1. TFORTH Assembly Listings
- Appendix A2. PATSY Machine Code Listing
- Appendix A3. PATSY Index
- Appendix A4. PATSY Glossary
- Appendix A5. Software Notes
- Appendix A6. Circuit Diagrams
- Annex B. Shipborne System Handbook (supplied in separate cover)



1. PROJECT TITLE

Development of a low frequency transponder system for penetrator instrumentation.

2. OBJECTIVES

- 2.1 To create and demonstrate a technique whereby
 - (a) the penetrated depth and position of a model HLW penetrator embedded in deep ocean sediment may be determined, and
 - (b) a communication channel to the penetrator may be established to telemeter parameters measured in-situ.
- 2.2 To transfer to a competent industrial organisation the technology necessary to manufacture, test, operate and market this technique world wide.

3. INTRODUCTION

For convenience the work can be considered in two phases, A and B.

Phase A consisted of the design of a 3.5 kHz transponder, the construction of 3 units, testing one on 'Discovery' Cruise 141 (October 1983), and testing two on 'Tyro' in March 1984, with provision of penetrators and other mechanical work by BRE, and the loan by IOS of essential associated ship-based equipment.

In Phase B the detailed interests of DoE and JRC diverged and became the subject of separate extensions to the Phase A work. Phase B for JRC consisted of acquiring a number of transponders and the ship-based receiving equipment. The first part of the ship-based electronics was delivered to the JRC in December 1984 and completed in 1985. A desk top transponder and 6 fully operational transponders were ordered by the JRC and it is expected that these will be delivered in July 1986 in time for the international hole closure experiment (HOCUS) planned for September 1986 in Jabuka Trench in the Adriatic.

As work developed on the transponder, the JRC became interested in the possibility of the system to transmit information over long time periods from deep sea sediment formations and re-transmit this data from a surface receiver via the European Space Agency's Meteosat satellite communication system. The Institute of Oceanographic Sciences provided a signal format for the transponder so that the JRC could undertake tests in the North Atlantic during the international long core cruise,

June - July 1985 on the Marion Dufresne.

4. TECHNICAL STATUS

4.1 General The choice of the frequency of 3.5 kHz for the acoustic link between buried penetrator and ship is justified, following a theoretical assessment, for three reasons: an acceptable level of signal attenuation in the sediment, an available transducer of moderate size capable of handling the necessary power, and several widely used seismic reflection profiling systems operating at this frequency which can form the shipboard end of the link.

By making the penetrator unit a transponder, the penetration depth is obtained directly by the profiler interrogation when the ship is overhead. Using ship navigation whilst manoeuvring within transponder range the geodetic location of the penetrator can be determined. Also the penetrator may be relocated long after deployment, for a period of years, limited essentially by transponder battery capacity.

An acoustic channel having been established, data can be communicated simultaneously with transponder location. The pulse interval form of modulation is chosen because of its inherent power efficiency and flexible dynamic range and because of the simplicity of use with the shipboard line-scan recorder of the profiling system, and because of IOS experience applying it successfully for telemetry from towed nets, dredges and other instruments over the past 15 years. For periods when simultaneous location is not important, it can be preferable to communicate without surface interrogation, the penetrator unit acting instead in a free or 'pinger' mode for the telemetry.

4.2 Transponder design (see also Annex A) For flexibility and reduction of chip count the penetrator transponder/pinger/telemetry unit is designed around a micro-processor, Fig. 1. The acoustic transducer is the most expensive and critical single component and is supplied by Bell Electronics Ltd, using ceramic from ITC Inc. By discussion with BRE it was agreed to multiplex up to 8 channels in the telemetry and to use a 12 bit A/D conversion. The 8 channels can be scanned at long preset intervals, stored and later telemetered. This slow rate of sampling is adequate for all sensors post emplacement, but inadequate for 'transient' sensors required during descent or settlement phases. For this reason the unit has a fast sampling and 'soft' storage mode of

finite preset duration, after which the stored data is replayed at a slower rate suitable for transmission by the acoustic link's pulse interval code.

Software to control the telemetry for various modes of operation has been written and can be assembled to suit individual missions if necessary, for example for different water depths or combinations of sensors. A typical mission might consist of the following:-

State 1 : Steady pinging during descent while sampling at a medium rate until interrupted by bottom detection sensor,

initiating:-

State 2 : Fast sampling during deceleration to limit of data storage, followed by

State 3 : Pinger telemetry mode for 60 minutes then, unless receiver interrogated, to

State 4 : 'Asleep', only receiver and threshold circuits powered up, until received interrogation pulse interrupts and powers circuitry into

State 5 : Transponder telemetry, listening between 1.99 and 2.01 secs interval since previous pulse, for as long as interrogations continue. If 9 consecutive pulses are missed unit returns to State 3, then State 4.

Numerical parameters underlined above are preset under software control.

Further information on the transponder software is contained in Annex A, which actually includes work carried out under a DoE contract subsequent to the period of this contract, but relevant for future transponders JRC may require.

4.3 Shipborne System (see also Annex B) The IOS 3.5 kHz reflection profiler is a high resolution system designed to be operated from any research or survey vessel, provided a suitable towing boom is fitted. It consists of four major components: line-scan recorder, transceiver, correlator and towed fish containing a transducer array. The first two are commercially available from Raytheon Ocean Systems Inc. The other two items were designed by IOS because commercial equivalents were found to have inadequate source levels, giving poor results over deep ocean sediments, and were found to have poor towing stability. A long FM swept pulse is generated for transmission and

passes through a matched filter (correlator) on reception. The heavy towed fish design has been used for echo-sounding and other purposes for 20 years and can be towed stably up to 15 knots on its faired armoured cable. The towing boom should have a minimum SWL of 2 tonnes and project around 2 m from either beam, preferably near midships.

Further details can be found in Annex B, of which one copy has been provided in plastic cover sheets and ring binder to form a shipborne manual.

4.4 Sea Trials Three 3.5 kHz, 100 watt transponders were designed, built and mounted in the tail end of 1800 kg BRE penetrators. One was launched from RRS Discovery Cruise 141 in November 1983 and the other two from MS Tyro in March 1984.

4.4.1 Discovery November 1983 Three wire tests were performed in water depths from 4600 m to 5400 m. The transponder replied to the 3.5 kHz profiler down to 2W of transmitted power but continued to transpond erratically on noise during the first wire test. Before the latter two tests the noise performance of the receiver was greatly improved, and the acoustic dynamic range of the acoustic threshold set satisfactorily.

Before the transponder could be mounted in the end of the penetrator the latter had to receive some attention as the thread was tight and somewhat corroded and the 'O' ring face had been damaged by a punch mark.

The penetrator was launched at 1133Z on 9th November but was never heard from again. A recording through the 3.5 kHz profiler fish was later replayed and the penetrator was heard to whine all the way to the bottom; strongly suggesting that the transponder had become damaged, possibly the cavity was acting as a resonator. The double doppler shift between this signal and its bottom echo allowed the terminal velocity to be estimated as $55 \text{ m/s} \pm 2 \text{ m/s}$. This was somewhat higher than the travel time indicated.

4.4.2 M.S. Tyro March 1984 After the failure on Discovery a temporary cowling was quickly designed to take the drag away from the rubber-boot of the transducer.

(i) The first drop This unit was intended to be set to free-ping at 2 Hz for 20 minutes (unfortunately this had to be changed to 50 minutes for test purposes and not changed back). Further work had to be done on the thread and 'O' ring surfaces of the two penetrators to be used before both transponders could be fitted. Mastic tape was wound round the joint in the hope that it would seal any hair-line scratches. The penetrator was launched tail-first and after initial turbulent noise had died away the 2 Hz pings could be seen.

The transponder continued to ping for about 50 minutes and although transmitted to at a 2 second repetition rate, timed out and then repeated the pinging sequence. Eventually, with the transmission rate now at 1 pulse per second, transponding started. By this time the ship had drifted more than 1.5 km from the dropping site. There was no sign of any modulation on the two telemetry signals. Channel 0 carrying the received signal strength was right up against the reference trace as though continually zero.

To judge the range of the transponder the ship steamed off at 5 kts for half an hour. As soon as the engines were restarted the transponder quitted its transponding mode and started free-pinging again. However, the pings could still be seen, through ship's noise, out to about 6 km horizontal range. When the ship had returned to the station and stopped engines, the pings were seen again but drifting erratically. It was two pinging sequences later before transponding started again.

It was possible, by correlating the sub-bottom echoes from the transponder with those from the profiler, to estimate that the penetration depth was about 23 m. Also the rate of approach of the bottom echo on the drop allowed the terminal velocity to be measured as 44 m/s \pm 1 m/s. This ties in well with the penetration depth but is about 9 m/s slower than the other penetrators of the same shape. This suggests that the protective cowling was producing a lot of extra drag.

(ii) The second drop Experience from the first drop indicated that the free-pinging was a nuisance so it was written out of the software. The receiver sensitivity was reduced by 12 dB as the first transponder had been too sensitive yet there had been 12 dB more power available from the 3.5 kHz transceiver.

The penetrator was launched but there was no sign of the transponder. During the fall there was the same high level of 'hootng' from the penetrator as had been recorded on Discovery and it is possible that the fate of the transponder was the same.

4.4.3 Discussion Two out of three transponders gave no results at all. What are the likely reasons for these failures?

(1) The one that did work was free-pinging during the descent while the failures were programmed to transpond. However, these two would undoubtedly have replied at random, excited by turbulent and later ship's noise, but did not.

(2) Mechanical damage to the electronics. Heavy components were supported against high accelerations.

(3) Damage to the transducer, flooding or separation of transponder. There is strong evidence for this. Turbulence-generated noise was visible on the 3.5 kHz dry-paper recorder in all three cases; however it was at a lower level in the successful drop, in fact after half a minute the pinging of the transponder could be seen all the way to the bottom as the turbulence noise faded out.

Originally it had been intended to mount the electronics in its own pressure case; later to save this expenditure a decision was made to do away with it and use the penetrator body as the pressure case. Clearly this was a mistake, as it is difficult to obtain the high quality precision finish needed for 'O' ring seals and transducer end cap thread on such a large heavy piece of mild steel.

The lack of wire tests on MS Tyro for whatever reason was a serious omission; tests would have shown up the 50 minute instead of 20 minute pinger state, so the transponder state and direct depth would have been reached much sooner and before the ship had drifted too far away and engines re-started; wire tests might also have indicated any telemetry problems.

Some positive points did emerge from the wire tests on Discovery and the successful drop on Tyro. On both occasions the acoustic signal levels confirmed the calculations that the acoustic link is viable through sediment and ocean. Due to turbulence noise the pinger mode is correct for the drop and engines should be off when interrogating to change to transponder mode.

Opportunities for sea trials cannot often be scheduled when convenient for instrument development. Preparations for Discovery and Tyro tests were both rather rushed; it could turn out that the delay because of industrial action preventing penetrator work on Discovery Cruise 153 in November 1984 may turn out to be helpful giving longer to prepare for the Marion Dufresne cruise in June/July 1985.

For these future penetrator drops the electronics should have its own pressure case, protective transducer shrouds should be better engineered and attached to the penetrator body rather than the transducer end cap, and wire tests must precede deployment.

5. CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER DEVELOPMENT

It is believed that the first objective 2.1 has just about been achieved, but needs further demonstration especially with sensors and telemetry. The second objective 2.2 has not been attempted yet owing to the somewhat hesitant progress in the first. However discussions have begun with industry with a view to sub-contracting production of several units as a prelude to a possible licence to manufacture.

Recently in discussions with JRC staff, methods for possible long term monitoring of a penetrator have been proposed. A moored surface buoy with a hydrophone would pick up the pinger telemetry signals from the penetrator, then decode them into a suitable format for onward radio transmission via the Meteosat satellite communication channel. It is the IOS view that the difficult technical aspects of this approach are (i) the achievement of a reliable long-life deep ocean moored buoy and (ii) the design of an automatic acoustic receiver/decoder. In connection with the latter it should be noted that the present acoustic coding system is optimised for a shipborne receiver based on a line-scan recorder with manual read off. Modifications to the penetrator electronics would be relatively straightforward and the buoy receiver could incorporate signal processing features of the IOS automatic depth tracker (PEST). There are trade-offs between penetrator battery life and the need for error-correcting codes in the acoustic link.

ANNEX A

TRANSPONDER DESIGN

1. INTRODUCTION

Because this project has been a collaborative one with the DoE (BRE) UK, and because work on the design under DoE funding progressed beyond the nominal end of this contract, it was not considered sensible to report on the design as it stood strictly at the end of this JRC contract period, but to describe the design as it exists for future penetrator instrumentation. At the time of writing in fact JRC have ordered further units and they will be provided to the design described here.

2. ORGANISATION OF THE ANNEX

The next section (3) outlines the basic theory including fundamental constraints and chosen compromises, leading to the acoustic method and calculation of parameters. The following section describes briefly the hardware, software and operating procedure including preparation, launch and post penetration telemetry. The detailed design information of software and hardware is provided in the Appendices A1 to A5.

3. THEORY

3.1 System constraints

There are some obvious bounds set by the laws of physics which can be used to define the optimum performance to be aimed for. There are other soft limits imposed by the cost of the system and ship's time, the volume available in the penetrator for instrumentation and batteries and the quality and quantity of the data that is to be transmitted. There are trade-offs and compromises that can be made in the latter case.

Signal to noise ratio

The signal level received by the ship from the transmitter, in 30 to 40 metres of mud and 6000 metres of water, should be higher than the noise in poor weather conditions, i.e. a signal to noise ratio better than 0 dB must be achieved. When transponding is to be used to fix the position of the penetrator the signal to noise level at the transponder must be even higher. The listening conditions at the transducer are considerably better, as deep in the mud there will be a

lower noise background than at the ship where also more power is available for transmission to the transponder.

Operating frequency

In deep water the noise from a variety of sources reaches a minimum in the range 1 to 20 kHz. The actual noise levels are very dependent on the weather conditions, local shipping and particularly self noise from the research ship's main engines and thruster as well as auxiliary equipment. The main source of loss in the acoustic signal path is due to inverse square-law spreading and is frequency independent and inevitable. However, attenuation is frequency dependent, being an exponential function of frequency in both water and mud and very much higher in the latter. It is therefore desirable to use the lowest frequency possible to get a signal through the sediment. Although noise levels will rise with reducing frequency the strongest constraint is set by the physical dimensions of the transducer since as its maximum dimension becomes smaller than a wave-length in water its radiation resistance becomes high and its beam-angle wide. The high radiation resistance, due to poor coupling into the water, means that the transducer can be over stressed either electrically or mechanically before the desired power level can be reached. The wide-beam angle, wasting power in directions other than near vertical can cancel out the benefits of reduced attenuation.

Data encoding

Amplitude and phase modulation of a carrier are impractical in deep water for at least three reasons:-

(1) Signal to noise ratios better than 20 dB are rarely achieved so there would be very limited dynamic range.

(2) Acoustic signals do not travel by simple "line-of-sight" paths but by multiple paths differing by only fractions of a wave-length due to small angle scattering and turbulence. The combination of signals produces randomly varying amplitude and phase distortions.

(3) Reverberation from layers within the sediment and from the water surface interfere with the direct signal, although the effect can in theory be removed if the pattern of echoes is constant or only changing slowly.

Frequency modulation suffers like phase modulation unless frequency shifting is used when the bandwidth required becomes excessive.

Time modulation, using the time delay between two short pulses to carry the information, can be very efficient and can have a large dynamic range. Its disadvantage is that it is slow, though signals can be multiplexed to increase the effective data rate.

Transmission pulse length

The shortest length possible is controlled by the bandwidth of the transducer being approximately equal to the reciprocal of the bandwidth. However, the longer the pulse the better, as it will contain proportionally more energy. If the coding scheme requires pulses to be transmitted in rapid succession then a long pulse would be a limitation specially as additional time must be allowed after each pulse for power amplifier capacitors to recharge. A range of between 2 and 20 msec seems sensible.

Total energy for transmission

This is essentially limited by the volume in the package that can be allocated to batteries. Lithium cells having about twice the energy-density of alkaline cells would make available several megajoules. Note: the kinetic energy of a 1800 kg penetrator at its terminal velocity is of the same order. It has been estimated that AAA alkaline cells would allow up to a megabit of information to be sent.

Listening time

Several hours would be reasonable, but much longer would become expensive in ship's time and increase the risk of losing data due to a worsening of the weather or because the ship has drifted too far off station and must make noise manoeuvring back again.

Resolution

Digital coding say using frequency shift keying could have unlimited resolution by merely extending the number of bits in a sequence but is very expensive in energy. Pulse interval telemetry (P.I.T.) uses only one pulse per data word (plus one reference pulse)

and the resolution is limited only by the maximum time that can be allowed to elapse between the pulses. P.I.T. is, however, a form of analogue modulation and will suffer from timing noise. This will arise from amplitude noise riding on the signal and more important variations in path-length as the receiving "fish" heaves up and down with the swell.

The approximate bit resolution of P.I.T. can be calculated as follows. The rise time t_r of each pulse will be less than half the pulse length, the exact fraction being dependent upon the type and order of the band defining filters used. If the signal pulse voltage into the detector is V_s , the leading edge is rising at V_s/t_r volts per second. In the presence of added noise, V_n rms, the threshold detector time jitter will therefore be $\Delta t = (V_n/V_s) t_r$ (rms), assuming that $V_s > 2V_n$ i.e. signal to noise ratio greater than 6 dB. In general this jitter will be present at both reference and signal channel pulses, though uncorrelated, so the time interval jitter will be $\sqrt{2} t_r (V_n/V_s)$. If the maximum, or full scale, time interval is t_o , the time interval resolution of the channel is therefore 1 part in $2^{-\frac{1}{2}} (t_o/t_r) (V_s/V_n)$. For the parameters used here, $t_o = 2$ secs, $t_r = 2$ msec, $V_s/V_n > 2$, so the resolution is better than 1 in 1414, i.e. between 10 and 11 bits. The bit rate is thus around 5 bits/second for a single channel. However increasing the number of channels from 1 to N is straightforward, the only decision required concerns whether the pulse intervals for different channels will be allowed to overlap, in which case for $(N + 1)$ pulses transmitted $10N$ bits equivalent are communicated. In previous underwater applications of P.I.T. overlapping intervals have been allowed and not found to cause undue confusion using a form of direct line scan recorder display. However this feature clearly relies on the recognition of which pulse belongs to which channel at every new frame of pulses.

If the shipborne receiving transducer is heaving at a rate V m/s between the arrival of reference and signal channel pulse, the timing error introduced in addition to the random noise component above is given by $(V/C) t_d$ where C is the sound speed (~1500 m/s) and t_d the signal delay. Generally V will be less than 1.5 m/s, in which case the error amounts to less than 0.1% of the signal.

Transmission and bottom reverberation

If transponding is used to synchronise data transmissions then the surface reverberation of the pulse sent from the ship and its bottom and sub-bottom echoes appear mixed in with the data pulses. This interference can be reduced by separating the transmitter and receiving hydrophone, by cutting down the power transmitted or more effectively by designing the telemetry system to send data up at its own rate (free-pinging) controlled by a local crystal oscillator.

Singing round

This can occur during transponding if the transponder responds to the echo of one of its earlier transmissions. In certain critical water depths, when the round trip time for the echo is a multiple of the repetition period, a permanent oscillation can be set up. This problem can usually be avoided by making the transponder receiver not sufficiently sensitive to hear its own echoes and by arranging that it listens in the narrow time window surrounding the expected interrogation pulse arrival time.

Two or more transponders in the area could interfere with each other in a more complex way.

Pulse repetition rate

If pulse interval telemetry is used then the desired resolution sets the fastest rate and there seems to be no good reason for using a slower rate as it would increase the time taken to receive all the data.

Timing of sampling

Certain sensors, particularly accelerometers, are likely to be affected by acoustic pick-up during transmissions. There is also the probability of electrical interference to sensitive sensor processing circuitry at the same time. Sampling must either be synchronised with the quiet periods during a transmission sequence or performed in a different phase and logged for later transmission.

3.2 The selected parameters

3.5 kHz was selected for the operating frequency being the lowest frequency for which a practical transducer could be designed and also

the frequency already used by IOS for sub-bottom profiling. The transducer designed for this job had a bandwidth of about 400 Hz. Allowing for the spread between different units, the choice of 200 Hz as the design bandwidth seemed reasonable. This sets the minimum pulse length to 5 ms and this was adopted.

After due consideration free-pinging pulse interval telemetry was chosen to transmit the logged data. One of the benefits of this type of transmission is that if the signal is received on a synchronously swept dry-paper recorder a graphical display is produced without any processing other than amplification and filtering.

The power amplifier was built to provide 100 watts of acoustic power consuming about 200 watts in the process. The energy taken from batteries to produce a 5 ms pulse was thus 1 joule.

The receiver was designed with a bandwidth of 200 Hz and automatic gain control so that the triggering threshold would adjust itself to suit the received signal level while remaining too insensitive to allow sing-round.

It was decided to use a 2 second repetition rate and multiplex a number of data channels by scaling and offsetting each one individually. Thus it would be possible in say an hour to transmit 1800 samples in each of 5 channels with a resolution of 10 bits.

3.3 Sonar calculations

Assuming:-

Operating frequency	= 3.5 kHz
Water depth	= 6000 m
Penetration depth	= 35 m
Attenuation in mud	= 0.1 dB/m-kHz = 12 dB one way
Power of ship's system with directivity index	= 2 Kw = 10 dB
Power of telemetry system with directivity index and with 5 msec pulse, bandwidth	= 100 W = 5 dB = 200 Hz
Sea-state 6 noise in 200 Hz bandwidth	= -42 dB re Pa

(1) Sound pressure level at transducer

Fish source level	= 33 dB re 1 watt
+ 50.8 dB re 1 watt/Pa @ 1 metre	= 83.8
+ 10 dB directivity index	= 94 dB re Pa

Losses:

Spreading loss over 6000 m	= 75.6 dB
Water attenuation (@ 0.25 dB/km)	= 1.5 dB
Scattering loss	= 3.0 dB
Loss due to acoustic impedance mismatch at the bottom	= 1.0 dB
Attenuation through sediment	= 12 dB

Total	= 93 dB
-------	---------

Thus sound pressure level at transducer = 1 dB re Pa

(2) Sound pressure level at the ship

Transducer source level	= 20 dB re 1 watt
+ 50.8 dB re 1 watt/Pa @ 1 metre	= 70.8
+ 5 dB directivity index	= 76 dB

With the same losses the level at the surface will be

= -17 dB re Pa

This is about the same level as the profiler's bottom echo assuming 30% reflectance.

(3) Sing-round level at transponder

The total losses will be greater by 6 dB because of the double path plus the remaining losses repeated

= 93 dB	
Extra distance	= +6
Other water losses	= +5.5
Mud attenuation	= +12

Total	= 116.5 dB
-------	------------

With a transponder source level of 76 dB re Pa the sound pressure level back at the transponder will be

= -40.5 dB re Pa
About 40 dB below the expected level from the ship. This assumes 100% reflection at the surface.

(4) Noise level at transducer

The level near the surface will be about -42 dB re Pa and there will be a few dBs drop in the water-column due to attenuation, scattering and refraction. It is expected that the noise will receive a similar attenuation in the mud, as the signal.

Allowing 15 dB for these losses

Noise level at transducer = -57 dB re Pa

Ship's noise could, however, add considerably to this.

(5) Transducer receiving sensitivity

at 1 m on axis = -95 dB re 1V/Pa

4. SYSTEM DESCRIPTION

4.1 Hardware (see Fig. 1)

4.1.1 The transducer

This is a commercially produced item using a piezo-electric ring mounted off from a base-plate and surrounded by a rubber boot filled with oil. The base-plate carries a thread and 'O' ring seal compatible with an I.O.S. designed pressure case.

One of the disadvantages of a ring transducer is that the electro-acoustic coupling is poor and this both raises the impedance seen into the electrical terminals and narrows the bandwidth. Limits are thus imposed on the maximum power that can be transmitted and the form of modulation that can be used.

4.1.2 The pressure case

Earlier plans to use the penetrator as a pressure case were discarded due to the difficulty of machining a heavy penetrator to the necessary precision. A standard 6 inch outside diameter 30 inch long tube takes the transducer at one end and at the other, an end plate with 16 electrical connections via underwater plugs.

4.1.3 The circuitry (see Appendix A6)

One long printed circuit board carries a low power microprocessor and support chips, a daughter board of additional random access memory

where data are logged and the analogue components. The analogue and digital elements of the board are deliberately separated to reduce mutual interference.

The analogue part comprises:-

(i) The transmitter. Essentially this is two power transistors driven through a buffer from the microprocessor and coupled through an output transformer to the transducer via a tuning choke.

(ii) The receiver. A signal from the transducer is extracted by a tertiary winding on the output transformer through a matched pad. The matched pad prevents the transmitter being loaded down by the receiver during transmission but ensures that maximum power is absorbed from the transducer on reception. The signal is amplified up by a low-noise first stage and two band-pass filter stages with a gain controlled stage between them. Detection is approximately square-law in the region of 50 mV, the switching point of the following comparator. The output from this is sharpened up to provide a negative logic signal to interrupt the microprocessor.

(iii) The analogue to digital converter. One of 8 (expandable to 16) analogue signals between +5 and -5 volts are selected by a multiplexer for digitising. During conversion the signal is held steady by the sample and hold circuit. 12 bits are converted in about 30 microseconds.

(iv) The supply switch. Transistors are used to control the +12 and -12 volt supplies to off-board sensor conditioning circuitry to allow them to be switched off to conserve power between samples at low sampling rates.

The digital part of the board consists of a HD6303 microprocessor that can address 16K of read-only-memory (ROM) and up to 40K of static random-access-memory (SRAM), controls the analogue to digital converter and generates pulses to drive the transmitter.

4.2 Software (see Fig. 2 and Appendices A1-A5)

A 'tuned' version of the FORTH language is resident in one 8K ROM. This also contains an editor, driver routines for an external bubble memory and an elementary monitor program. A further 8K of ROM has the compiled procedures which constitute PATSY, the run-time program, that samples, logs and transmits data using P.I.T.

FORTH plus PATSY can be viewed as a dictionary of procedures or 'words' on to the end of which additional words may be compiled at any time. This allows the user, through a standard terminal and interfacing box, to create test routines at the last minute to, for instance, check the calibration and correct functioning of sensors and test the memory used for data storage. It is even possible in an emergency to recompile a new version of the main program without the use of a development system and produce code that will execute immediately and at full operational speed.

4.3 Sampling and data transmission sequence

This is the description of a typical sequence.

4.3.1 Preparation

After test and diagnostics have been run the user can preset a number of parameters such as the number cycles of sampling or transmission of different data sets and the scaling to be applied to each channel for transmission. To reduce the work-load these parameters can be given default values by executing SETUP and then only alterations need be made. The main program can then be executed triggering a series of pings at one a minute. The terminal can now be disconnected and the electronics sealed into its pressure case.

The optical-switch used to sense the instant of contact with the sediment is also used to inform the computer of the instant of launch by the removal of a shutter blocking the optical path. Ten seconds after the shutter is initially introduced this is acknowledged by the ping rate changing to once every ten seconds. (Because the telemetry system and sensor package must be connected to each other before the optical switch can be connected, a shorting plug must be substituted for the optical switch, i.e. the unconnected optical switch is equivalent to a connected but blocked switch. The exchange of the lead from shorting plug to optical switch must then be performed within 10 seconds). It is hoped that this cumbersome procedure can be eliminated in the future.

4.3.2 Descent through the water-column

As the penetrator is released and the optical switch unblocked PHASE1 sampling starts. Sampling of tilt, temperature and

acceleration proceeds at 10 Hz interleaved with pinging at the same frequency. These medium sampled data values are stored for later transmission. Meanwhile two accelerometers are sampled at 500 Hz and stored in a rolling-buffer. One minute into the fall the optical switch is enabled to interrupt on contact with the sediment.

4.3.3 Deceleration through the sediment

This, PHASE2, of the sampling is instigated by an interrupt from the optical switch or, as a backup, by the deceleration signals exceeding a threshold. PHASE2 is similar to PHASE1 except that it times-out after 2 seconds and no pings are transmitted.

4.3.4 Transmission of resting attitude

This is a live transmission using free running pinging at 1/2 Hz repetition rate of tilt and accelerometer signals for a few minutes.

4.3.5 First transponding session

Ten minutes of transponding at this time, before the ship has had a chance to drift away, allows the penetration depth of the transducer to be determined acoustically. (Doppler shift imposed on the 10 Hz pinging during the fall through the water-column also allows the terminal velocity to be calculated).

4.3.6 Logged data transmissions

The fast rate (500 Hz) data that has been sampled into rolling-buffers is backed up to a point 1/2 second before deceleration commenced and is copied into other buffers before being transmitted by free running P.I.T. The medium rate (10 Hz) data sampled through the water-column follows similarly encoded. This sequence is not in the correct temporal order but it is considered desirable to transmit the more important fast rate data first before anything can go wrong. It might help the immediate interpretation of the logged data if the samples in each batch were transmitted in reverse order.

4.3.7 Second transponding session

By the time the complete logged data set has been sent 1 to 2 hours will have passed during which the ship can have drifted several miles from the launch site. A suitable period of transponding at this stage will allow the penetrator's position to be fixed and for the

ship to manoeuvre back to a point overhead.

4.3.8 Second session of live pinging

This is a good opportunity, for 5 to 10 minutes, to find out whether the attitude of the penetrator has changed and to get a stable temperature measurement in case temperature compensation needs to be applied to any of the data.

4.3.9 Logged data transmission with JRC format

One of the accelerometer channels is retransmitted with a different format to provide data for tests on the Meteosat transceiver.

4.3.10 The end

Rather than simply stopping the program it might as well repeat itself indefinitely by looping back to transmit the fast data again (Section 4.3.5).

In future it may be required that after several repetitions of the logged data the telemetry system should reduce power consumption to a minimum and sample and log data at a slow rate over months or years and come fully awake to transmit that data on demand.

FIGURE 1
SYSTEM FLOW CHART

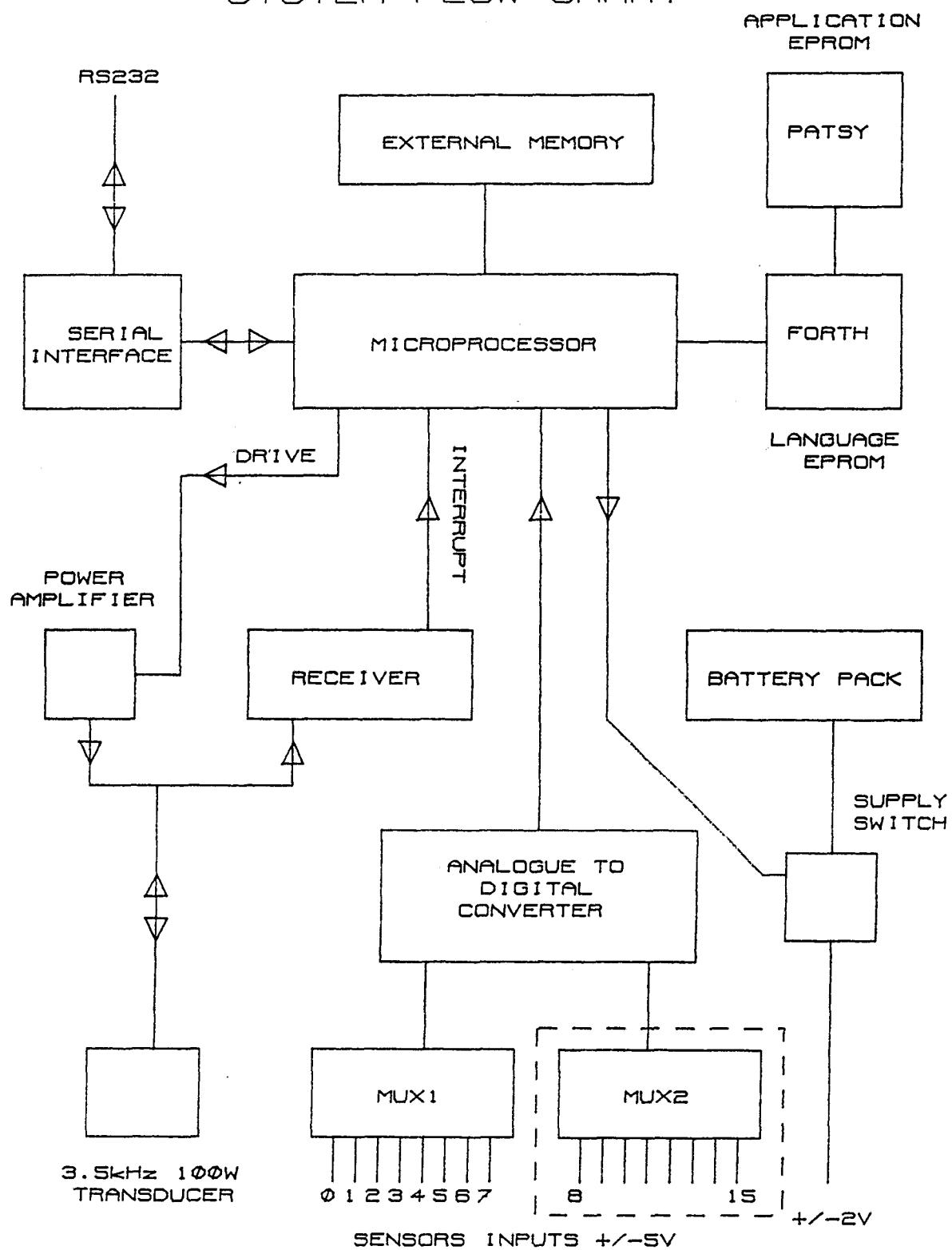


FIGURE 2
MEMORY MAP

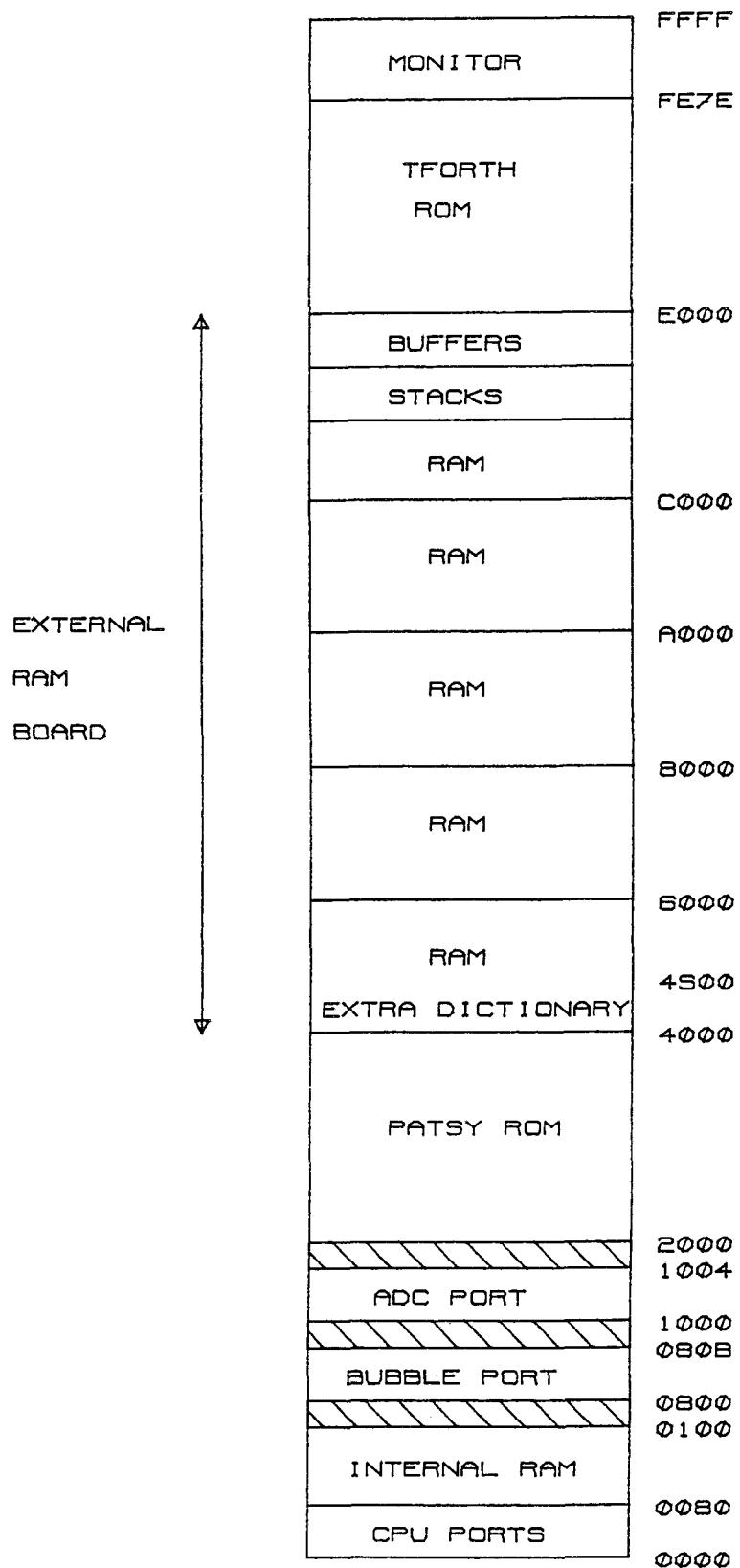
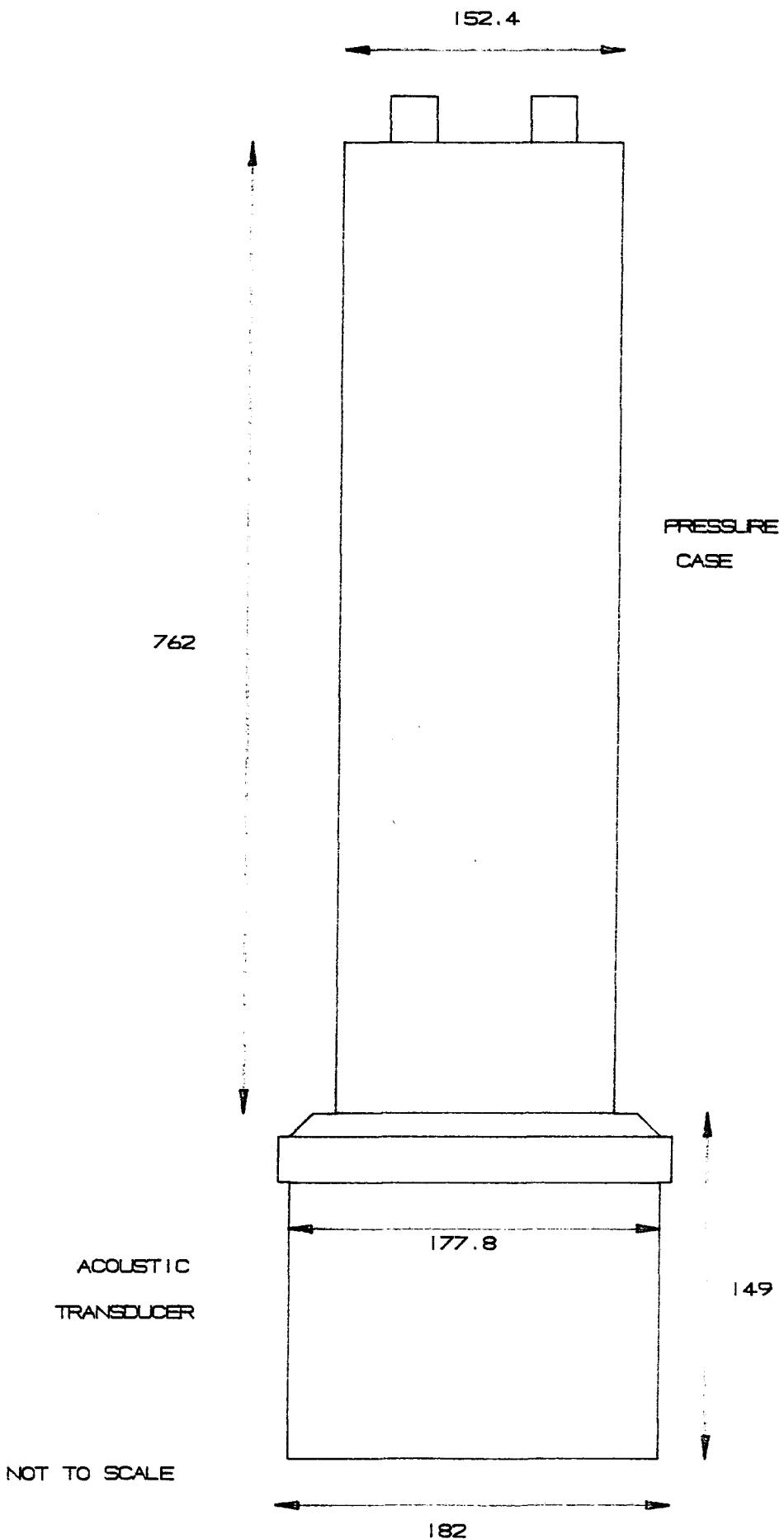


FIGURE 3

TELEMETRY SYSTEM OUTLINE



APPENDIX A1 TFORTH ASSEMBLY LISTING

FORTH

SSB MNEMONIC ASSEMBLER PAGE 1

```
1:      NAM    FORTH
2: * FILENAME "FORTH1.SRC"
3: * TURBO FORTH FOR PENETRATOR
4: * STARTING IN ROM AT $E000
5: *
0008      NBLK   EQU    8
E000      MEMEND EQU    68*NBLK+$DDE0
DFFF      MEMTOP EQU    $DFFF "
0011      ACIAC   EQU    $11
0012      ACIAD   EQU    $12
11: *
0080      NBLK   EQU    8
0080      MUDFLG RMB    2
0082      HLFNCYC RMB   2
0084      OVRFWS RMB   2
0086      SIGFLG RMB   2
0088      DWNCNT RMB   2
18: *
19: * INTERRUPT VECTORS
00D0      ORG    $D0
00D0 7E FF95 21: SCI    JMP   TRAP      serial interrupt
00D3 7E FF95 22: TOF    JMP   TRAP      Timer over-flow interrupt
00D6 7E FF95 23: OCF    JMP   TRAP      Output compare interrupt
00D9 7E FF95 24: ICF    JMP   TRAP      Input capture interrupt
00DC 7E FF95 25: IRQ1   JMP   TRAP      PIA interrupts.
26: *
00E0      ORG    $E0
00E0      N     RMB    10
00EA      RMB    6
00F0      XTEMP  RMB    2
00F2      UP    RMB    2
32: *
2000      ORG    $2000
34: *
2000 C5 35: FCB    $C5
2001 46 36: FCC    "FORT"
2002 4F 52
2004 54
2005 C8 37: FCB    $C8
2006 FD D0 38: FDB    NOOP-7
2008 BD E9C5 39: FORTH JSR    D0DOES
200B 7E EFD2 40: JMP    DOVOC
200E 81 A0 41: FDB    $81A0
2010 20 2D 42: FDB    TASK-7
2012 00 00 43: FDB    0
2014 54 44: FCC    "Turbo-forth for 6303 1984"
2015 75 72
2017 62 6F
2019 2D 66
201B 6F 72
201D 74 68
201F 20 66
2021 6F 72
2023 20 36
2025 33 30
2027 33 20
2029 31 39
202B 38 34
202D 84 45: FCB    $84
```

FORTH

SSB MNEMONIC ASSEMBLER PAGE 2

202E 54	46:	FCC	"TAS"
202F 41 53			
2031 CB	47:	FCB	\$CB
2032 20 00	48:	FDB	FORTH-8
2034 39	49:	TASK	RTS
2035	50:	REND	EQU *
	51:		*
4000	52:	ORG	\$4000
4000	53:	UORIG	RMB 6
4006	54:	XSPZER	RMB 2
4008	55:	XRZERO	RMB 2
400A	56:	XTIB	RMB 2
400C	57:	XWIDTH	RMB 2
400E	58:	XWARN	RMB 2
4010	59:	XFENCE	RMB 2
4012	60:	XDP	RMB 2
4014	61:	XVOCL	RMB 2
4016	62:	XBLK	RMB 2
4018	63:	XIN	RMB 2
401A	64:	XOUT	RMB 2
401C	65:	XSCR	RMB 2
401E	66:	XQFSET	RMB 2
4020	67:	XCONT	RMB 2
4022	68:	XCURR	RMB 2
4024	69:	XSTATE	RMB 2
4026	70:	XBASE	RMB 2
4028	71:	XDPL	RMB 2
402A	72:	XFLD	RMB 2
402C	73:	XCSP	RMB 2
402E	74:	XRNUM	RMB 2
4030	75:	XHLD	RMB 2
4032	76:	XDELAY	RMB 2
4034	77:	XCOLUMN	RMB 2
4036	78:	IOSTAT	RMB 2
4038	79:		RMB 8
4040	80:	XUSE	RMB 2
4042	81:	XPREV	RMB 2
4044	82:		RMB 4
	83:		*
E000	84:	ORG	\$E000
E000 01	85:	ORIG	NOP
E001 7E F081	86:	JMP	CENT
E004 01	87:		NOP
E005 7E F0C9	88:	JMP	WENT
E008 18 9F	89:	FDB	6303,0002
E00A 00 02			
E00C 00 00	90:	FDB	0
E00E 00 7F	91:	BACKSP	FDB \$7F
E010 40 00	92:	UPINIT	FDB UORIG
E012 DC FE	93:	SINIT	FDB \$DCFE
E014 DD DF	94:	RINIT	FDB \$DDDF
E016 DD 00	95:		FDB \$DD00
E018 00 1F	96:		FDB 31
E01A 00 01	97:		FDB 1
E01C 20 35	98:	FENCIN	FDB REND
E01E 40 48	99:	DPINIT	FDB UORIG+\$48
E020 20 08	100:	VOCINT	FDB FORTH
E022 00 64	101:	COLINT	FDB 100
E024 00 00	102:	DELINT	FDB 0
	103:		*

FORTH

SSB MNEMONIC ASSEMBLER PAGE 3

E026 83	104:	FCB	\$83	
E027 4C	105:	FCC	"LI"	
E028 49				
E029 D4	106:	FCB	\$D4	
E02A 00 00	107:	FDB	0	
E02C DF F0	108: LIT	STX	XTEMP	
E02E 38	109:	FCB	\$38	PULX
E02F EC 00	110:	FDB	\$ED00	LDD 0, X
E031 08	111:	INX		
E032 08	112:	INX		
E033 3C	113:	FCB	\$3C	PSHX
E034 DE F0	114:	LDX	XTEMP	
E036 ED 00	115:	FDB	\$ED00	STD 0, X
E038 09	116:	DEX		
E039 09	117:	DEX		
E03A 39	118:	RTS		
	119: *			
E03B 86	120:	FCB	\$86	
E03C 43	121:	FCC	"CLITE"	
E03D 4C 49				
E03F 54 45				
E041 D2	122:	FCB	\$D2	
E042 E0 26	123:	FDB	LIT-6	
E044 DF F0	124: CLITER	STX	XTEMP	
E046 38	125:	FCB	\$38	PULX
E047 4F	126:	CLR A		
E048 E6 00	127:	LDA B	0, X	
E04A 08	128:	INX		
E04B 3C	129:	FCB	\$3C	PSHX
E04C DE F0	130:	LDX	XTEMP	
E04E ED 00	131:	FDB	\$ED00	STD 0, X
E050 09	132:	DEX		
E051 09	133:	DEX		
E052 39	134:	RTS		
	135: *			
E053 87	136:	FCB	\$87	
E054 45	137:	FCC	"EXECUT"	
E055 58 45				
E057 43 55				
E059 54				
E05A C5	138:	FCB	\$C5	
E05B E0 3B	139:	FDB	CLITER-9	
E05D EC 02	140: EXEC	FDB	\$EC02	LDD 2, X
E05F 08	141:	INX		
E060 08	142:	INX		
E061 37	143:	PSH B		
E062 36	144:	PSH A		
E063 39	145:	RTS		
	146: *			
E064 87	147:	FCB	\$87	
E065 30	148:	FCC	"OBRANC"	
E066 42 52				
E068 41 4E				
E06A 43				
E06B C8	149:	FCB	\$CB	
E06C E0 53	150:	FDB	EXEC-10	
E06E 08	151: ZBRAN	INX		
E06F 08	152:	INX		
E070 EC 00	153:	FDB	\$ED00	LDD 0, X
E072 39	154:	RTS		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 4

	155: *			
E073 86	156:	FCB	\$86	
E074 28	157:	FCC	"(LOOP"	
E075 4C 4F				
E077 4F 50				
E079 A9	158:	FCB	\$A9	
E07A E0 64	159:	FDB	ZBRAN-10	
E07C 4F	160:	XLOOP	CLR A	
E07D C6 01	161:	LDA	B #1	
E07F 20 0E	162:	BRA	XLOOP2	
	163: *			
E081 87	164:	FCB	\$87	
E082 28	165:	FCC	"(+LOOP"	
E083 2B 4C				
E085 4F 4F				
E087 50				
E088 A9	166:	FCB	\$A9	
E089 E0 73	167:	FDB	XLOOP-9	
E08B 08	168:	XLOOP	INX	
E08C 08	169:		INX	
E08D EC 00	170:	FDB	\$EC00	LDD D,X
E08F DF F0	171:	XLOOP2	STX	XTEMP
E091 4D	172:	TST	A	
E092 2A 11	173:	BPL	XPLOF	
E094 8D 09	174:	BSR	XPLOPS	
E096 0D	175:	SEC		
E097 E2 07	176:	SBC	B 7,X	
E099 A2 06	177:	SBC	A 6,X	
E09B 2A 19	178:	BPL	ZBYES	
E09D 20 0C	179:	BRA	XPLONO	
E09F 30	180:	XPLOPS	TSX	
E0A0 E3 04	181:	FDB	\$E304	ADD D 4,X
E0A2 ED 04	182:	FDB	\$ED04	STD 4,X
E0A4 39	183:	RTS		
E0A5 8D FB	184:	XPLOF	BSR	XPLOPS
E0A7 A3 06	185:	FDB	\$A306	SUB D 6,X
E0A9 2B 0B	186:	BMI	ZBYES	
E0AB 38	187:	XPLONO	FCB	\$38 PULX
E0AC 31	188:	INS		
E0AD 31	189:	INS		
E0AE 31	190:	INS		
E0AF 31	191:	INS		
E0B0 3C	192:	FCB	\$3C	PSHX
E0B1 DE F0	193:	LDX	XTEMP	
E0B3 86 01	194:	LDA	A #1	
E0B5 39	195:	RTS		
E0B6 DE F0	196:	ZBYES	LDX	XTEMP
E0B8 4F	197:	CLR	A	
E0B9 39	198:	RTS		
	199: *			
E0BA 84	200:	FCB	\$84	
E0BB 28	201:	FCC	"(DO"	
E0BC 44 4F				
E0BE A9	202:	FCB	\$A9	
E0BF E0 81	203:	FDB	XLOOP-10	
E0C1 32	204:	XDO	PUL	A
E0C2 33	205:		PUL	B
E0C3 DD	206:	FCB	\$DD,XTEMP	STD XTEMP
E0C4 F0				
E0C5 08	207:	INX		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 5

E0C6 08	208:	INX	
E0C7 EC 02	209:	FDB \$EC02	LDD 2,X
E0C9 37	210:	PSH B	
E0CA 36	211:	PSH A	
E0CB EC 00	212:	FDB \$EC00	LDD 0,X
E0CD 37	213:	PSH B	
E0CE 36	214:	PSH A	
E0CF 08	215:	INX	
E0D0 08	216:	INX	
E0D1 DC	217:	FCB \$DC,XTEMP	LDD XTEMP
E0D2 F0			
E0D3 37	218:	PSH B	
E0D4 36	219:	PSH A	
E0D5 39	220:	RTS	
	221: *		
E0D6 81	222:	FCB \$81	
E0D7 C9	223:	FCB \$C9	
E0D8 EO BA	224:	FDB XDO-7	
E0DA DF F0	225: I	STX XTEMP	
E0DC 30	226:	TSX	
E0DD EC 02	227:	FDB \$EC02	LDD 2,X
E0DF DE F0	228:	LDX XTEMP	
E0E1 ED 00	229:	FDB \$ED00	STD 0,X
E0E3 09	230:	DEX	
E0E4 09	231:	DEX	
E0E5 39	232:	RTS	
	233: *		
E0E6 85	234:	FCB \$85	
E0E7 44	235:	FCC "DIGI"	
E0E8 49 47			
E0EA 49			
E0EB D4	236:	FCB \$D4	
E0EC EO D6	237:	FDB I-4	
E0EE A6 05	238: DIGIT	LDA A 5,X	
E0F0 80 30	239:	SUB A #\$30	
E0F2 2B 19	240:	BMI DIGIT2	
E0F4 81 0A	241:	CMP A #\$A	
E0F6 2B 0A	242:	BMI DIGITO	
E0F8 81 11	243:	CMP A #\$11	
E0FA 2B 11	244:	BMI DIGIT2	
E0FC 81 2B	245:	CMP A #\$2B	
E0FE 2A 0D	246:	BPL DIGIT2	
E100 80 07	247:	SUB A #7	
E102 A1 03	248: DIGITO	CMP A 3,X	
E104 2A 07	249:	BPL DIGIT2	
E106 C6 01	250:	LDA B #1	
E108 A7 05	251:	STA A 5,X	
E10A E7 03	252: DIGIT1	STA B 3,X	
E10C 39	253:	RTS	
E10D 5F	254: DIGIT2	CLR B	
E10E 08	255:	INX	
E10F 08	256:	INX	
E110 E7 02	257:	STA B 2,X	
E112 20 F6	258:	BRA DIGIT1	
	259: *		
E114 86	260:	FCB \$86	
E115 28	261:	FCC "(FIND"	
E116 46 49			
E118 4E 44			
E11A A9	262:	FCB \$A9	

FORTH

SSB MNEMONIC ASSEMBLER PAGE 6

E11B E0 E6	263:	FDB	DIGIT-B	
E11D 08	264:	PFIND	INX	
E11E 08	265:		INX	
E11F EC 00	266:	FDB	\$EC00	LDD 0,X
E121 DD	267:	FCB	\$DD,N	STD N
E122 E0				
E123 EC 02	268:	FDB	\$EC02	LDD 2,X
E125 DD	269:	FCB	\$DD,N+2	STD N+2
E126 E2				
E127 DF F0	270:	STX	XTEMP	
E129 DE E0	271:	LDX	N	
E12B E6 00	272:	PFIND1	LDA B 0,X	
E12D D7 E6	273:		STA B N+6	
E12F C4 3F	274:	AND B	#\$3F	
E131 08	275:	INX		
E132 DF E0	276:	STX	N	
E134 DE E2	277:	LDX	N+2	
E136 A6 00	278:	LDA A 0,X		
E138 08	279:	INX		
E139 DF E4	280:	STX	N+4	
E13B 11	281:	CBA		
E13C 26 24	282:	BNE	PFIND4	
E13E DE E4	283:	PFIND2	LDX N+4	
E140 A6 00	284:	LDA A 0,X		
E142 08	285:	INX		
E143 DF E4	286:	STX	N+4	
E145 DE E0	287:	LDX	N	
E147 E6 00	288:	LDA B 0,X		
E149 08	289:	INX		
E14A DF E0	290:	STX	N	
E14C 5D	291:	TST B		
E14D 2A 10	292:	BPL	PFIND8	
E14F C4 7F	293:	AND B	#\$7F	
E151 11	294:	CBA		
E152 27 17	295:	BEQ	FOUND	
E154 EE 00	296:	PFIND3	LDX 0,X	
E156 26 D3	297:	BNE	PFIND1	
E158 DE F0	298:	LDX	XTEMP	
E15A 4F	299:	CLR A		
E15B 5F	300:	CLR B		
E15C ED 02	301:	FDB	\$ED02	STD 2,X
E15E 39	302:	RTS		
E15F 11	303:	PFIND8	CBA	
E160 27 DC	304:	BEQ	PFIND2	
E162 DE E0	305:	PFIND4	LDX N	
E164 E6 00	306:	PFIND9	LDA B 0,X	
E166 08	307:	INX		
E167 2A FB	308:	BPL	PFIND9	
E169 20 E9	309:	BRA	PFIND3	
E16B DE F0	310:	FOUND	LDX XTEMP	
E16D DC	311:	FCB	\$DC,N	LDD N
E16E E0				
E16F C3	312:	FCB	\$C3	ADD D #
E170 00 02	313:	FDB	2	
E172 ED 02	314:	FDB	\$ED02	STD 2,X
E174 09	315:	DEX		
E175 09	316:	DEX		
E176 09	317:	DEX		
E177 09	318:	DEX		
E178 D6 E6	319:	LDA B	N+6	

FORTH

SSB MNEMONIC ASSEMBLER PAGE 7

E17A 4F	320:	CLR A	
E17B ED 04	321:	FDB \$ED04	STD 4,X
E17D ED 02	322:	FDB \$ED02	STD 2,X
E17F 39	323:	RTS	
	324: *		
E180 87	325:	FCB \$87	
E181 45	326:	FCC "ENCLOS"	
E182 4E 43			
E184 4C 4F			
E186 53			
E187 C5	327:	FCB \$C5	
E188 E1 14	328:	FDB PFIND-9	
E18A E6 03	329:	ENCLOS LDA B 3,X	
E18C DF F0	330:	STX XTEMP	
E18E EE 04	331:	LDX 4,X	
E190 7F 00E0	332:	CLR N	
E193 A6 00	333:	ENCL2 LDA A 0,X	
E195 27 1F	334:	BEQ ENCL6	
E197 11	335:	CBA	
E198 26 06	336:	BNE ENCL3	
E19A 08	337:	INX	
E19B 7C 00E0	338:	INC N	
E19E 20 F3	339:	BRA ENCL2	
E1A0 96 E0	340:	ENCL3 LDA A N	
E1A2 36	341:	PSH A	
E1A3 A6 00	342:	ENCL4 LDA A 0,X	
E1A5 27 15	343:	BEQ ENCL7	
E1A7 11	344:	CBA	
E1A8 27 06	345:	BEQ ENCL5	
E1AA 08	346:	INX	
E1AB 7C 00E0	347:	INC N	
E1AE 20 F3	348:	BRA ENCL4	
E1B0 D6 E0	349:	ENCL5 LDA B N	
E1B2 17	350:	TBA	
E1B3 4C	351:	INC A	
E1B4 20 0A	352:	BRA ENCL8	
E1B6 D6 E0	353:	ENCL6 LDA B N	
E1B8 37	354:	PSH B	
E1B9 5C	355:	INC B	
E1BA 20 02	356:	BRA ENCL7+2	
E1BC D6 E0	357:	ENCL7 LDA B N	
E1BE 96 E0	358:	LDA A N	
E1CO DE F0	359:	ENCL8 LDX XTEMP	
E1C2 09	360:	DEX	
E1C3 09	361:	DEX	
E1C4 09	362:	DEX	
E1C5 09	363:	DEX	
E1C6 A7 03	364:	STA A 3,X	
E1C8 E7 05	365:	STA B 5,X	
E1CA 32	366:	PUL A	
E1CB A7 07	367:	STA A 7,X	
E1CD 4F	368:	CLR A	
E1CE A7 02	369:	STA A 2,X	
E1DO A7 04	370:	STA A 4,X	
E1D2 A7 06	371:	STA A 6,X	
E1D4 39	372:	RTS	
	373: *		
E1D5 84	374:	FCB \$84	
E1D6 45	375:	FCC "EMI"	
E1D7 4D 49			

FORTH

SSB MNEMONIC ASSEMBLER PAGE 8

E1D9 D4	376:	FCB	\$D4	
E1DA E1 80	377:	FDB	ENCLOS-10	
E1DC A6 03	378:	EMIT	LDA A 3,X	
E1DE 08	379:	INX		
E1DF 08	380:	INX		
E1E0 DF F0	381:	STX	XTEMP	
E1E2 BD F481	382:	JSR	PEMIT	
E1E5 DE F2	383:	LDX	UP	
E1E7 6C 1B	384:	INC	XOUT+1-UORIG,X	
E1E9 26 02	385:	BNE	*+4	
E1EB 6C 1A	386:	INC	XOUT-UORIG,X	
E1ED DE F0	387:	LDX	XTEMP	
E1EF 39	388:	RTS		
	389: *			
E1F0 83	390:	FCB	\$83	
E1F1 4B	391:	FCC	"KE"	
E1F2 45				
E1F3 D9	392:	FCB	\$D9	
E1F4 E1 D5	393:	FDB	EMIT-7	
E1F6 DF F0	394:	KEY	STX XTEMP	
E1F8 BD F498	395:	JSR	PKEY	
E1FB DE F0	396:	KEY1	LDX XTEMP	
E1FD 09	397:	DEX		
E1FE 09	398:	DEX		
E1FF A7 03	399:	STA A 3,X		
E201 4F	400:	CLR A		
E202 A7 02	401:	STA A 2,X		
E204 39	402:	RTS		
	403: *			
E205 89	404:	FCB	\$89	
E206 3F	405:	FCC	"?TERMINA"	
E207 54 45				
E209 52 4D				
E20B 49 4E				
E20D 41				
E20E CC	406:	FCB	\$CC	
E20F E1 F0	407:	FDB	KEY-6	
E211 DF F0	408:	QTERM	STX XTEMP	
E213 BD F4B1	409:	JSR	PQTER	
E216 20 E3	410:	BRA	KEY1	
	411: *			
E218 82	412:	FCB	\$82	
E219 43	413:	FCC	"C"	
E21A D2	414:	FCB	\$D2	
E21B E2 05	415:	FDB	QTERM-12	
E21D DF F0	416:	CR	STX XTEMP	
E21F BD F4BC	417:	JSR	PCR	
E222 DE F0	418:	LDX	XTEMP	
E224 39	419:	RTS		
	420: *			
E225 85	421:	FCB	\$85	
E226 43	422:	FCC	"CMOV"	
E227 4D 4F				
E229 56				
E22A C5	423:	FCB	\$C5	
E22B E2 18	424:	FDB	CR-5	
E22D EC 02	425:	CMOVE	FDB \$EC02	LDD 2,X
E22F DD	426:	FCB	\$DD,N	STD N
E230 E0				
E231 08	427:	INX		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 9

E232 08	428:	INX	
E233 EC 02	429:	FDB \$EC02	LDD 2,X
E235 DD	430:	FCB \$DD,N+2	STD N+2
E236 E2			
E237 08	431:	INX	
E238 08	432:	INX	
E239 EC 02	433:	FDB \$EC02	LDD 2,X
E23B DD	434:	FCB \$DD,N+4	STD N+4
E23C E4			
E23D 08	435:	INX	
E23E 08	436:	INX	
E23F DF F0	437:	STX XTEMP	
E241 DC	438: CMOV2	FCB \$DC,N	LDD N
E242 EO			
E243 83	439:	FCB \$83	SUB D #
E244 00 01	440:	FDB 1	
E246 DD	441:	FCB \$DD,N	STD N
E247 EO			
E248 25 10	442:	BCS CMOV3	
E24A DE E4	443:	LDX N+4	
E24C A6 00	444:	LDA A 0,X	
E24E 08	445:	INX	
E24F DF E4	446:	STX N+4	
E251 DE E2	447:	LDX N+2	
E253 A7 00	448:	STA A 0,X	
E255 08	449:	INX	
E256 DF E2	450:	STX N+2	
E258 20 E7	451:	BRA CMOV2	
E25A DE F0	452: CMOV3	LDX XTEMP	
E25C 39	453:	RTS	
	454: *		
E25D 82	455:	FCB \$82	
E25E 55	456:	FCC "U"	
E25F AA	457:	FCB \$AA	
E260 E2 25	458:	FDB CMOVE-B	
E262 09	459: USTAR	DEX	
E263 09	460:	DEX	
E264 09	461:	DEX	
E265 09	462:	DEX	
E266 A6 07	463:	LDA A 7,X	
E268 E6 09	464:	LDA B 9,X	
E26A 3D	465:	FCB \$3D	MUL
E26B ED 04	466:	FDB \$ED04	STD 4,X
E26D A6 06	467:	LDA A 6,X	
E26F E6 08	468:	LDA B 8,X	
E271 3D	469:	FCB \$3D	MUL
E272 ED 02	470:	FDB \$ED02	STD 2,X
E274 EC 07	471:	FDB \$EC07	LDD 7,X
E276 3D	472:	FCB \$3D	MUL
E277 ED 00	473:	FDB \$ED00	STD 0,X
E279 A6 06	474:	LDA A 6,X	
E27B E6 09	475:	LDA B 9,X	
E27D 3D	476:	FCB \$3D	MUL
E27E E3 00	477:	FDB \$E300	ADD D 0,X
E280 24 02	478:	BCC USTAR2	
E282 6C 02	479:	INC 2,X	
E284 E3 03	480: USTAR2	FDB \$E303	ADD D 3,X
E286 24 02	481:	BCC USTAR3	
E288 6C 02	482:	INC 2,X	
E28A ED 07	483: USTAR3	FDB \$ED07	STD 7,X

FORTH

SSB MNEMONIC ASSEMBLER PAGE 10

E28C A6 05	484:	LDA A 5,X	
E28E A7 09	485:	STA A 9,X	
E290 A6 02	486:	LDA A 2,X	
E292 A7 06	487:	STA A 6,X	
E294 08	488:	INX	
E295 08	489:	INX	
E296 08	490:	INX	
E297 08	491:	INX	
E298 39	492:	RTS	
	493: *		
E299 82	494:	FCB \$82	
E29A 55	495:	FCC "U"	
E29B AF	496:	FCB \$AF	
E29C E2 5D	497:	FDB USTAR-5	
E29E 86 11	498:	USLASH LDA A #17	
E2A0 08	499:	INX	
E2A1 A7 00	500:	STA A 0,X	
E2A3 EC 03	501:	FDB \$EC03	LDD 3,X
E2A5 A1 01	502:	USL1 CMP A 1,X	
E2A7 22 09	503:	BHI USL3	
E2A9 25 04	504:	BCS USL2	
E2AB E1 02	505:	CMP B 2,X	
E2AD 24 03	506:	BCC USL3	
E2AF 0C	507:	USL2 CLC	
E2B0 20 03	508:	BRA USL4	
E2B2 A3 01	509:	USL3 FDB \$A301	SUB D 1,X
E2B4 0D	510:	SEC	
E2B5 69 06	511:	USL4 ROL 6,X	
E2B7 69 05	512:	ROL 5,X	
E2B9 6A 00	513:	DEC 0,X	
E2BB 27 06	514:	BEQ USL5	
E2BD 59	515:	ROL B	
E2BE 49	516:	ROL A	
E2BF 24 E4	517:	BCC USL1	
E2C1 20 EF	518:	BRA USL3	
E2C3 DD	519:	USL5 FCB \$DD, XTEMP	STD XTEMP
E2C4 F0			
E2C5 EC 05	520:	FDB \$EC05	LDD 5,X
E2C7 ED 03	521:	FDB \$ED03	STD 3,X
E2C9 DC	522:	FCB \$DC, XTEMP	LDD XTEMP
E2CA F0			
E2CB ED 05	523:	FDB \$ED05	STD 5,X
E2CD 08	524:	INX	
E2CE 39	525:	RTS	
	526: *		
E2CF 83	527:	FCB \$83	
E2D0 41	528:	FCC "AN"	
E2D1 4E			
E2D2 C4	529:	FCB \$C4	
E2D3 E2 99	530:	FDB USLASH-5	
E2D5 08	531:	AND	INY
E2D6 08	532:	INX	
E2D7 EC 00	533:	FDB \$EC00	LDD 0,X
E2D9 E4 03	534:	AND B 3,X	
E2DB A4 02	535:	AND A 2,X	
E2DD ED 02	536:	FDB \$ED02	STD 2,X
E2DF 39	537:	RTS	
	538: *		
E2E0 82	539:	FCB \$82	
E2E1 4F	540:	FCC "O"	

FORTH

SSB MNEMONIC ASSEMBLER PAGE 11

E2E2 D2	541:	FCB	\$D2	.
E2E3 E2 CF	542:	FDB	AND-6	
E2E5 08	543:	OR	INX	
E2E6 08	544:	INX		
E2E7 EC 00	545:	FDB	\$EC00	LDD 0,X
E2E9 EA 03	546:	ORA	B 3,X	
E2EB AA 02	547:	ORA	A 2,X	
E2ED ED 02	548:	FDB	\$ED02	STD 2,X
E2EF 39	549:	RTS		
	550: *			
E2F0 83	551:	FCB	\$83	
E2F1 58	552:	FCC	"X0"	
E2F2 4F				
E2F3 D2	553:	FCB	\$D2	
E2F4 E2 EO	554:	FDB	OR-5	
E2F6 08	555:	XOR	INX	
E2F7 08	556:	INX		
E2F8 EC 00	557:	FDB	\$EC00	LDD 0,X
E2FA E8 03	558:	EOR	B 3,X	
E2FC A8 02	559:	EOR	A 2,X	
E2FE ED 02	560:	FDB	\$ED02	STD 2,X
E300 39	561:	RTS		
	562: *			
E301 83	563:	FCB	\$83	
E302 53	564:	FCC	"SP"	
E303 50				
E304 C0	565:	FCB	\$C0	
E305 E2 F0	566:	FDB	XOR-6	
E307 EF 00	567:	SPAT	STX 0,X	
E309 09	568:	DEX		
E30A 09	569:	DEX		
E30B 39	570:	RTS		
	571: *			
E30C 83	572:	FCB	\$83	
E30D 53	573:	FCC	"SP"	
E30E 50				
E30F A1	574:	FCB	\$A1	
E310 E3 01	575:	FDB	SPAT-6	
E312 DE F2	576:	SPSTOR	LDX UP	
E314 EE 06	577:	LDX	6,X	
E316 39	578:	RTS		
	579: *			
E317 83	580:	FCB	\$83	
E318 52	581:	FCC	"RF"	
E319 50				
E31A A1	582:	FCB	\$A1	
E31B E3 0C	583:	FDB	SPSTOR-6	
E31D 32	584:	RPSTOR	PUL A	
E31E 33	585:	PUL	B	
E31F BE E014	586:	LDS	RINIT	
E322 37	587:	PSH	B	
E323 36	588:	PSH	A	
E324 39	589:	RTS		
	590: *			
E325 82	591:	FCB	\$82	
E326 3B	592:	FCC	";"	
E327 D3	593:	FCB	\$D3	
E328 E3 17	594:	FDB	RPSTOR-6	
E32A BD E358	595:	SEMIS	JSR	FROMR
E32D 39	596:	RTS		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 12

E32E 85	597: *		
E32F 4C	598: FCB	\$85	
E330 45 41	599: FCC	"LEAV"	
E332 56			
E333 C5	600: FCB	\$C5	
E334 E3 25	601: FDB	SEMS-5	
E336 DF FO	602: LEAVE	STX XTEMP	
E338 30	603: TSX		
E339 EC 02	604: FDB	\$EC02	LDD 2,X
E33B ED 04	605: FDB	\$ED04	STD 4,X
E33D DE FO	606: LDX	XTEMP	
E33F 39	607: RTS		
	608: *		
E340 82	609: FCB	\$82	
E341 3E	610: FCC	">"	
E342 D2	611: FCB	\$D2	
E343 E3 2E	612: FDB	LEAVE-8	
E345 08	613: TOR	INX	
E346 08	614: INX		
E347 DF FO	615: STX	XTEMP	
E349 EE 00	616: LDX	O,X	
E34B 32	617: PUL A		
E34C 33	618: PUL B		
E34D 3C	619: FCB	\$3C	PSHX
E34E 37	620: PSH B		
E34F 36	621: PSH A		
E350 DE FO	622: LDX	XTEMP	
E352 39	623: RTS		
	624: *		
E353 82	625: FCB	\$82	
E354 52	626: FCC	"R"	
E355 BE	627: FCB	\$BE	
E356 E3 40	628: FDB	TOR-5	
E358 DF FO	629: FROMR	STX XTEMP	
E35A 38	630: FCB	\$38	PULX
E35B 18	631: FCB	\$18	XGDX
E35C 38	632: FCB	\$38	PULX
E35D 18	633: FCB	\$18	XGDX
E35E 3C	634: FCB	\$3C	PSHX
E35F DE FO	635: LDX	XTEMP	
E361 ED 00	636: FDB	\$ED00	STD O,X
E363 09	637: DEX		
E364 09	638: DEX		
E365 39	639: RTS		
	640: *		
E366 81	641: FCB	\$81	
E367 D2	642: FCB	\$D2	
E368 E3 53	643: FDB	FROMR-5	
E36A DF FO	644: R	STX XTEMP	
E36C 30	645: TSX		
E36D EC 02	646: FDB	\$EC02	LDD 2,X
E36F DE FO	647: LDX	XTEMP	
E371 ED 00	648: FDB	\$ED00	STD O,X
E373 09	649: DEX		
E374 09	650: DEX		
E375 39	651: RTS		
	652: *		
E376 82	653: FCB	\$82	
E377 30	654: FCC	"O"	

FORTH

SSB MNEMONIC ASSEMBLER PAGE 13

E378 BD	655:	FCB	\$BD	
E379 E3 66	656:	FDB	R-4	
E37B EC 02	657: ZEQU	FDB	\$EC02	LDD 2,X
E37D 27 03	658:	BEO	ZEQU2	
E37F 4F	659:	CLR A		
E380 C6 FF	660:	LDA B	#\$FF	
E382 5C	661: ZEQU2	INC B		
E383 ED 02	662:	FDB	\$ED02	STD 2,X
E385 39	663:	RTS		
	664: *			
E386 82	665:	FCB	\$82	
E387 30	666:	FCC	"0"	
E388 BC	667:	FCB	\$BC	
E389 E3 76	668:	FDB	ZEQU-5	
E38B 5F	669: ZLESS	CLR B		
E38C A6 02	670:	LDA A	2,X	
E38E 2A 01	671:	BPL	ZLESS2	
E390 5C	672:	INC B		
E391 4F	673: ZLESS2	CLR A		
E392 ED 02	674:	FDB	\$ED02	STD 2,X
E394 39	675:	RTS		
	676: *			
E395 81	677:	FCB	\$81	
E396 AB	678:	FCB	\$AB	
E397 E3 86	679:	FDB	ZLESS-5	
E399 EC 02	680: PLUS	FDB	\$EC02	LDD 2,X
E39B E3 04	681:	FDB	\$E304	ADD D 4,X
E39D ED 04	682:	FDB	\$ED04	STD 4,X
E39F 08	683:	INX		
E3A0 08	684:	INX		
E3A1 39	685:	RTS		
	686: *			
E3A2 82	687:	FCB	\$82	
E3A3 44	688:	FCC	"D"	
E3A4 AB	689:	FCB	\$AB	
E3A5 E3 95	690:	FDB	PLUS-4	
E3A7 EC 04	691: DPLUS	FDB	\$EC04	LDD 4,X
E3A9 E3 08	692:	FDB	\$E308	ADD D 8,X
E3AB ED 08	693:	FDB	\$ED08	STD 8,X
E3AD EC 02	694:	FDB	\$ED02	LDD 2,X
E3AF E9 07	695:	ADC B	7,X	
E3B1 A9 06	696:	ADC A	6,X	
E3B3 ED 06	697:	FDB	\$ED06	STD 6,X
E3B5 08	698:	INX		
E3B6 08	699:	INX		
E3B7 08	700:	INX		
E3B8 08	701:	INX		
E3B9 39	702:	RTS		
	703: *			
E3BA 85	704:	FCB	\$85	
E3BB 4D	705:	FCC	"MINU"	
E3BC 49 4E				
E3BE 55				
E3BF D3	706:	FCB	\$D3	
E3C0 E3 A2	707:	FDB	DPLUS-5	
E3C2 4F	708: MINUS	CLR A		
E3C3 5F	709:	CLR B		
E3C4 A3 02	710:	FDB	\$A302	SUB D 2,X
E3C6 ED 02	711:	FDB	\$ED02	STD 2,X
E3C8 39	712:	RTS		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 14

E3C9 86	713: *			
E3CA 44	714:	FCB	\$86	
E3CB 4D 49	715:	FCC	"DMINU"	
E3CD 4E 55				
E3CF D3	716:	FCB	\$D3	
E3D0 E3 BA	717:	FDB	MINUS-8	
E3D2 4F	718:	DMINUS	CLR A	
E3D3 5F	719:		CLR B	
E3D4 A3 04	720:	FDB	\$A304	SUB D 4, X
E3D6 ED 04	721:	FDB	\$ED04	STD 4, X
E3D8 CC	722:	FCB	\$CC	LDD #
E3D9 00 00	723:	FDB	0	
E3DB E2 03	724:	SBC	B 3, X	
E3DD A2 02	725:	SBC	A 2, X	
E3DF ED 02	726:	FDB	\$ED02	STD 2, X
E3E1 39	727:		RTS	
	728: *			
E3E2 84	729:	FCB	\$84	
E3E3 4F	730:	FCC	"OVE"	
E3E4 56 45				
E3E6 D2	731:	FCB	\$D2	
E3E7 E3 C9	732:	FDB	DMINUS-9	
E3E9 EC 04	733:	OVER	FDB	\$EC04 LDD 4, X
E3EB ED 00	734:	FDB	\$ED00	STD 0, X
E3ED 09	735:		DEX	
E3EE 09	736:		DEX	
E3EF 39	737:		RTS	
	738: *			
E3F0 84	739:	FCB	\$84	
E3F1 44	740:	FCC	"DRO"	
E3F2 52 4F				
E3F4 D0	741:	FCB	\$D0	
E3F5 E3 E2	742:	FDB	OVER-7	
E3F7 08	743:	DROP	INX	
E3F8 08	744:		INX	
E3F9 39	745:		RTS	
	746: *			
E3FA 84	747:	FCB	\$84	
E3FB 53	748:	FCC	"SWA"	
E3FC 57 41				
E3FE D0	749:	FCB	\$D0	
E3FF E3 F0	750:	FDB	DROP-7	
E401 EC 02	751:	SWAP	FDB	\$EC02 LDD 2, X
E403 DD	752:	FCB	\$DD, XTEMP	STD XTEMP
E404 F0				
E405 EC 04	753:	FDB	\$EC04	LDD 4, X
E407 ED 02	754:	FDB	\$ED02	STD 2, X
E409 DC	755:	FCB	\$DC, XTEMP	LDD XTEMP
E40A F0				
E40B ED 04	756:	FDB	\$ED04	STD 4, X
E40D 39	757:		RTS	
	758: *			
E40E 83	759:	FCB	\$83	
E40F 44	760:	FCC	"DU"	
E410 55				
E411 D0	761:	FCB	\$D0	
E412 E3 FA	762:	FDB	SWAP-7	
E414 EC 02	763:	DUP	FDB	\$EC02 LDD 2, X
E416 ED 00	764:		FDB	\$ED00 STD 0, X

FORTH

SSB MNEMONIC ASSEMBLER PAGE 15

E418 09	765:	DEX	
E419 09	766:	DEX	
E41A 39	767:	RTS	
	768: *		
E41B 82	769:	FCB \$82	
E41C 2B	770:	FCC "+"	
E41D A1	771:	FCB \$A1	
E41E E4 0E	772:	FDB DUP-6	
E420 EC 04	773: PSTORE	FDB \$EC04	LDD 4,X
E422 DF F0	774:	STX XTEMP	
E424 EE 02	775:	LDX 2,X	
E426 E3 00	776:	FDB \$E300	ADD D O,X
E428 ED 00	777:	FDB \$ED00	STD O,X
E42A DE F0	778:	LDX XTEMP	
E42C 08	779:	INX	
E42D 08	780:	INX	
E42E 08	781:	INX	
E42F 08	782:	INX	
E430 39	783:	RTS	
	784: *		
E431 86	785:	FCB \$86	
E432 54	786:	FCC "TOGGL"	
E433 4F 47			
E435 47 4C			
E437 C5	787:	FCB \$C5	
E438 E4 1B	788:	FDB PSTORE-5	
E43A BD E3E9	789: TOGGLE	JSR OVER	
E43D BD E45E	790:	JSR CAT	
E440 BD E2F6	791:	JSR XOR	
E443 BD E401	792:	JSR SWAP	
E446 BD E482	793:	JSR CSTORE	
E449 39	794:	RTS	
	795: *		
E44A 81	796:	FCB \$81	
E44B C0	797:	FCB \$C0	
E44C E4 31	798:	FDB TOGGLE-9	
E44E DF F0	799: AT	STX XTEMP	
E450 EE 02	800:	LDX 2,X	
E452 EC 00	801:	FDB \$EC00	LDD O,X
E454 DE F0	802:	LDX XTEMP	
E456 ED 02	803:	FDB \$ED02	STD 2,X
E458 39	804:	RTS	
	805: *		
E459 82	806:	FCB \$82	
E45A 43	807:	FCC "C"	
E45B C0	808:	FCB \$C0	
E45C E4 4A	809:	FDB AT-4	
E45E DF F0	810: CAT	STX XTEMP	
E460 EE 02	811:	LDX 2,X	
E462 4F	812:	CLR A	
E463 E6 00	813:	LDA B O,X	
E465 DE F0	814:	LDX XTEMP	
E467 ED 02	815:	FDB \$ED02	STD 2,X
E469 39	816:	RTS	
	817: *		
E46A 81	818:	FCB \$81	
E46B A1	819:	FCB \$A1	
E46C E4 59	820:	FDB CAT-5	
E46E EC 04	821: STORE	FDB \$EC04	LDD 4,X
E470 DF F0	822:	STX XTEMP	

FORTH

SSB MNEMONIC ASSEMBLER PAGE 16

E472 EE 02	823:	LDX	2, X	
E474 ED 00	824:	FDB	\$ED00	STD 0, X
E476 DE F0	825:	LDX	XTEMP	
E478 08	826:	INX		
E479 08	827:	INX		
E47A 08	828:	INX		
E47B 08	829:	INX		
E47C 39	830:	RTS		
	831: *			
E47D 82	832:	FCB	\$82	
E47E 43	833:	FCC	"C"	
E47F A1	834:	FCB	\$A1	
E480 E4 6A	835:	FDB	STORE-4	
E482 E6 05	836: CSTORE	LDA B	5, X	
E484 DF F0	837:	STX	XTEMP	
E486 EE 02	838:	LDX	2, X	
E488 E7 00	839:	STA B	0, X	
E48A DE F0	840:	LDX	XTEMP	
E48C 08	841:	INX		
E48D 08	842:	INX		
E48E 08	843:	INX		
E48F 08	844:	INX		
E490 39	845:	RTS		
	846: *			
E491 C1	847:	FCB	\$C1	
E492 BA	848:	FCB	\$BA	
E493 E4 7D	849:	FDB	CSTORE-5	
E495 BD E86C	850: COLON	JSR	QEXEC	
E498 BD E827	851:	JSR	SCSP	
E49B BD E648	852:	JSR	CURENT	
E49E BD E44E	853:	JSR	AT	
E4A1 BD E639	854:	JSR	CONTXT	
E4A4 BD E46E	855:	JSR	STORE	
E4A7 BD EE59	856:	JSR	CREATE	
E4AA BD E903	857:	JSR	RBAK	
E4AD 39	858:	RTS		
	859: *			
E4AE C1	860:	FCB	\$C1	
E4AF BB	861:	FCB	\$BB	
E4B0 E4 91	862:	FDB	COLON-4	
E4B2 BD E895	863: SEMI	JSR	QCSP	
E4B5 BD E044	864:	JSR	CLITER	
E4B8 39	865:	FCB	\$39	
E4B9 BD E6F6	866:	JSR	CCOMM	
E4BC BD E917	867:	JSR	SMUDGE	
E4BF BD E8F5	868:	JSR	LBAK	
E4C2 39	869:	RTS		
	870: *			
E4C3 88	871:	FCB	\$88	
E4C4 43	872:	FCC	"CONSTAN"	
E4C5 4F 4E				
E4C7 53 54				
E4C9 41 4E				
E4CB D4	873:	FCB	\$D4	
E4CC E4 AE	874:	FDB	SEMI-4	
E4CE BD EE59	875: CON	JSR	CREATE	
E4D1 BD E917	876:	JSR	SMUDGE	
E4D4 BD E53E	877:	JSR	THREE	
E4D7 BD E6D9	878:	JSR	ALLOT	
E4DA BD E6E4	879:	JSR	COMMA	

FORTH SSB MNEMONIC ASSEMBLER PAGE 17

E4DD BD E952	880:	JSR	PSCODE
E4E0 DF FO	881:	DOCON	STX XTEMP
E4E2 38	882:	FCB	\$38 PULX
E4E3 EC 00	883:	FDB	\$EC00 LDD O,X
E4E5 DE FO	884:	LDX	XTEMP
E4E7 ED 00	885:	FDB	\$ED00 STD O,X
E4E9 09	886:	DEX	
E4EA 09	887:	DEX	
E4EB 39	888:	RTS	
	889: *		
E4EC 88	890:	FCB	\$88
E4ED 56	891:	FCC	"VARIABL"
E4EE 41 52			
E4F0 49 41			
E4F2 42 4C			
E4F4 C5	892:	FCB	\$C5
E4F5 E4 C3	893:	FDB	CON-11
E4F7 BD E4CE	894:	VAR	JSR CON
E4FA BD E952	895:	JSR	PSCODE
E4FD 32	896:	DOVAR	PUL A
E4FE 33	897:		PUL B
E4FF ED 00	898:	FDB	\$ED00 STD O,X
E501 09	899:	DEX	
E502 09	900:	DEX	
E503 39	901:	RTS	
	902: *		
E504 84	903:	FCB	\$84
E505 55	904:	FCC	"USE"
E506 53 45			
E508 D2	905:	FCB	\$D2
E509 E4 EC	906:	FDB	VAR-11
E50B BD E4CE	907:	USER	JSR CON
E50E BD E952	908:	JSR	PSCODE
E511 DF FO	909:	DOUSER	STX XTEMP
E513 38	910:	FCB	\$38 PULX
E514 EC 00	911:	FDB	\$EC00 LDD O,X
E516 DE FO	912:	LDX	XTEMP
E518 D3	913:	FCB	\$D3,UP ADD D UP
E519 F2			
E51A ED 00	914:	FDB	\$ED00 STD O,X
E51C 09	915:	DEX	
E51D 09	916:	DEX	
E51E 39	917:	RTS	
	918: *		
E51F 81	919:	FCB	\$81
E520 B0	920:	FCB	\$B0
E521 E5 04	921:	FDB	USER-7
E523 BD E4EO	922:	ZERO	JSR DOCON
E526 00 00	923:	FDB	O
	924: *		
E528 81	925:	FCB	\$81
E529 B1	926:	FCB	\$B1
E52A E5 1F	927:	FDB	ZERO-4
E52C BD E4EO	928:	ONE	JSR DOCON
E52F 00 01	929:	FDB	1
	930: *		
E531 81	931:	FCB	\$81
E532 B2	932:	FCB	\$B2
E533 E5 28	933:	FDB	ONE-4
E535 BD E4EO	934:	TWO	JSR DOCON

FORTH

SSB MNEMONIC ASSEMBLER PAGE 18

E538 00 02	935:	FDB	2
	936: *		
E53A 81	937:	FCB	\$81
E53B B3	938:	FCB	\$B3
E53C E5 31	939:	FDB	TWO-4
E53E BD E4EO	940: THREE	JSR	DOCON
E541 00 03	941:	FDB	3
	942: *		
E543 82	943:	FCB	\$82
E544 42	944:	FCC	"B"
E545 CC	945:	FCB	\$CC
E546 E5 3A	946:	FDB	THREE-4
E548 BD E4EO	947: BL	JSR	DOCON
E54B 00 20	948:	FDB	\$20
	949: *		
E54D 85	950:	FCB	\$85
E54E 46	951:	FCC	"FIRS"
E54F 49 52			
E551 53			
E552 D4	952:	FCB	\$D4
E553 E5 43	953:	FDB	BL-5
E555 BD E4EO	954: FIRST	JSR	DOCON
E558 DD EO	955:	FDB	MEMEND/NBLK-68*NBLK
	956: *		
E55A 85	957:	FCB	\$85
E55B 4C	958:	FCC	"LIMI"
E55C 49 4D			
E55E 49			
E55F D4	959:	FCB	\$D4
E560 E5 4D	960:	FDB	FIRST-8
E562 BD E4EO	961: LIMIT	JSR	DOCON
E565 EO 00	962:	FDB	MEMEND
	963: *		
E567 85	964:	FCB	\$85
E568 42	965:	FCC	"B/BU"
E569 2F 42			
E56B 55			
E56C C6	966:	FCB	\$C6
E56D E5 5A	967:	FDB	LIMIT-8
E56F BD E4EO	968: BBUF	JSR	DOCON
E572 00 40	969:	FDB	64
	970: *		
E574 85	971:	FCB	\$85
E575 42	972:	FCC	"B/SC"
E576 2F 53			
E578 43			
E579 D2	973:	FCB	\$D2
E57A E5 67	974:	FDB	BBUF-8
E57C BD E4EO	975: BSCR	JSR	DOCON
E57F 00 10	976:	FDB	16
	977: *		
E581 87	978:	FCB	\$87
E582 2B	979:	FCC	"+ORIGI"
E583 4F 52			
E585 49 47			
E587 49			
E588 CE	980:	FCB	\$CE
E589 E5 74	981:	FDB	BSCR-8
E58B BD E02C	982: PORIG	JSR	LIT
E58E EO 00	983:	FDB	ORIG

FORTH

SSB MNEMONIC ASSEMBLER PAGE 19

E590 BD E399	984:	JSR	PLUS
E593 39	985:	RTS	
	986: *		
E594 82	987:	FCB	\$82
E595 53	988:	FCC	"8"
E596 B0	989:	FCB	\$B0
E597 E5 81	990:	FDB	PORIG-10
E599 BD E511	991: SZERO	JSR	DOUSER
E59C 00 06	992:	FDB	XSPZER-UORIG
	993: *		
E59E 82	994:	FCB	\$82
E59F 52	995:	FCC	"R"
E5A0 B0	996:	FCB	\$B0
E5A1 E5 94	997:	FDB	SZERO-5
E5A3 BD E511	998: RZERO	JSR	DOUSER
E5A6 00 08	999:	FDB	XRZERO-UORIG
	1000: *		
E5A8 83	1001:	FCB	\$83
E5A9 54	1002:	FCC	"TI"
E5AA 49			
E5AB C2	1003:	FCB	\$C2
E5AC E5 9E	1004:	FDB	RZERO-5
E5AE BD E511	1005: TIB	JSR	DOUSER
E5B1 00 0A	1006:	FDB	XTIB-UORIG
	1007: *		
E5B3 85	1008:	FCB	\$85
E5B4 57	1009:	FCC	"WIDT"
E5B5 49 44			
E5B7 54			
E5B8 C8	1010:	FCB	\$C8
E5B9 E5 A8	1011:	FDB	TIB-6
E5BB BD E511	1012: WIDTH	JSR	DOUSER
E5BE 00 0C	1013:	FDB	XWIDTH-UORIG
	1014: *		
E5C0 87	1015:	FCB	\$87
E5C1 57	1016:	FCC	"WARNIN"
E5C2 41 52			
E5C4 4E 49			
E5C6 4E			
E5C7 C7	1017:	FCB	\$C7
E5C8 E5 B3	1018:	FDB	WIDTH-8
E5CA BD E511	1019: WARN	JSR	DOUSER
E5CD 00 0E	1020:	FDB	XWARN-UORIG
	1021: *		
E5CF 85	1022:	FCB	\$85
E5D0 46	1023:	FCC	"FENC"
E5D1 45 4E			
E5D3 43			
E5D4 C5	1024:	FCB	\$C5
E5D5 E5 C0	1025:	FDB	WARN-10
E5D7 BD E511	1026: FENCE	JSR	DOUSER
E5DA 00 10	1027:	FDB	XFENCE-UORIG
	1028: *		
E5DC 82	1029:	FCB	\$82
E5DD 44	1030:	FCC	"D"
E5DE D0	1031:	FCB	\$D0
E5DF E5 CF	1032:	FDB	FENCE-8
E5E1 BD E511	1033: DP	JSR	DOUSER
E5E4 00 12	1034:	FDB	XDP-UORIG
	1035: *		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 20

E5E6 88	1036:	FCB	\$88
E5E7 56	1037:	FCC	"VOC-LIN"
E5E8 4F 43			
E5EA 2D 4C			
E5EC 49 4E			
E5EE CB	1038:	FCB	\$CB
E5EF E5 DC	1039:	FDB	DP-5
E5F1 BD E511	1040: VOCLIN	JSR	DOUSER
E5F4 00 14	1041:	FDB	XVOCL-UORIG
	1042: *		
E5F6 83	1043:	FCB	\$83
E5F7 42	1044:	FCC	"BL"
E5F8 4C			
E5F9 CB	1045:	FCB	\$CB
E5FA E5 E6	1046:	FDB	VOCLIN-11
E5FC BD E511	1047: BLK	JSR	DOUSER
E5FF 00 16	1048:	FDB	XBLK-UORIG
	1049: *		
E601 82	1050:	FCB	\$82
E602 49	1051:	FCC	"I"
E603 CE	1052:	FCB	\$CE
E604 E5 F6	1053:	FDB	BLK-6
E606 BD E511	1054: IN	JSR	DOUSER
E609 00 18	1055:	FDB	XIN-UORIG
	1056: *		
E60B 83	1057:	FCB	\$83
E60C 4F	1058:	FCC	"OU"
E60D 55			
E60E D4	1059:	FCB	\$D4
E60F E6 01	1060:	FDB	IN-5
E611 BD E511	1061: OUT	JSR	DOUSER
E614 00 1A	1062:	FDB	XOUT-UORIG
	1063: *		
E616 83	1064:	FCB	\$83
E617 53	1065:	FCC	"SC"
E618 43			
E619 D2	1066:	FCB	\$D2
E61A E6 0B	1067:	FDB	OUT-6
E61C BD E511	1068: SCR	JSR	DOUSER
E61F 00 1C	1069:	FDB	XSCR-UORIG
	1070: *		
E621 86	1071:	FCB	\$86
E622 4F	1072:	FCC	"OFFSE"
E623 46 46			
E625 53 45			
E627 D4	1073:	FCB	\$D4
E628 E6 16	1074:	FDB	SCR-6
E62A BD E511	1075: OFSET	JSR	DOUSER
E62D 00 1E	1076:	FDB	XOFSET-UORIG
	1077: *		
E62F 87	1078:	FCP	\$87
E630 43	1079:	FCC	"CONTEX"
E631 4F 4E			
E633 54 45			
E635 58			
E636 D4	1080:	FCB	\$D4
E637 E6 21	1081:	FDB	OFSET-9
E639 BD E511	1082: CONTEXT	JSR	DOUSER
E63C 00 20	1083:	FDB	XCONT-UORIG
	1084: *		

FORTH SSB MNEMONIC ASSEMBLER PAGE 21

E63E 87	1085:	FCB	\$87
E63F 43	1086:	FCC	"CURREN"
E640 55 52			
E642 52 45			
E644 4E			
E645 D4	1087:	FCB	\$D4
E646 E6 2F	1088:	FDB	CONTXT-10
E648 BD E511	1089: CURENT	JSR	DOUSER
E64B 00 22	1090:	FDB	XCURR-UORIG
	1091: *		
E64D 85	1092:	FCB	\$85
E64E 53	1093:	FCC	"STAT"
E64F 54 41			
E651 54			
E652 C5	1094:	FCB	\$C5
E653 E6 3E	1095:	FDB	CURENT-10
E655 BD E511	1096: STATE	JSR	DOUSER
E658 00 24	1097:	FDB	XSTATE-UORIG
	1098: *		
E65A 84	1099:	FCB	\$84
E65B 42	1100:	FCC	"BAS"
E65C 41 53			
E65E C5	1101:	FCB	\$C5
E65F E6 4D	1102:	FDB	STATE-8
E661 BD E511	1103: BASE	JSR	DOUSER
E664 00 26	1104:	FDB	XBASE-UORIG
	1105: *		
E666 83	1106:	FCB	\$83
E667 44	1107:	FCC	"DP"
E668 50			
E669 CC	1108:	FCB	\$CC
E66A E6 5A	1109:	FDB	BASE-7
E66C BD E511	1110: DPL	JSR	DOUSER
E66F 00 28	1111:	FDB	XDPL-UORIG
	1112: *		
E671 83	1113:	FCB	\$83
E672 46	1114:	FCC	"FL"
E673 4C			
E674 C4	1115:	FCB	\$C4
E675 E6 66	1116:	FDB	DPL-6
E677 BD E511	1117: FLD	JSR	DOUSER
E67A 00 2A	1118:	FDB	XFLD-UORIG
	1119: *		
E67C 83	1120:	FCB	\$83
E67D 43	1121:	FCC	"CS"
E67E 53			
E67F D0	1122:	FCB	\$D0
E680 E6 71	1123:	FDB	FLD-6
E682 BD E511	1124: CSP	JSR	DOUSER
E685 00 2C	1125:	FDB	XCSP-UORIG
	1126: *		
E687 82	1127:	FCB	\$82
E688 52	1128:	FCC	"R"
E689 A3	1129:	FCB	\$A3
E68A E6 7C	1130:	FDB	CSP-6
E68C BD E511	1131: RNUM	JSR	DOUSER
E68F 00 2E	1132:	FDB	XRNUM-UORIG
	1133: *		
E691 83	1134:	FCB	\$83
E692 48	1135:	FCC	"HL"

FORTH

SSB MNEMONIC ASSEMBLER PAGE 22

E693 4C
E694 C4 1136: FCB \$C4
E695 E6 87 1137: FDB RNUM-5
E697 BD E4E0 1138: HLD JSR DOCON
E69A 40 30 1139: FDB XHLD
1140: *
E69C 87 1141: FCB \$87
E69D 43 1142: FCC "COLUMN"
E69E 4F 4C
E6A0 55 4D
E6A2 4E
E6A3 D3 1143: FCB \$D3
E6A4 E6 91 1144: FDB HLD-6
E6A6 BD E511 1145: COLUMNS JSR DOUSER
E6A9 00 34 1146: FDB XCOLUMNS-UORIG
1147: *
E6AB 82 1148: FCB \$82
E6AC 31 1149: FCC "1"
E6AD AB 1150: FCB \$AB
E6AE E6 9C 1151: FDB COLUMNS-10
E6B0 BD E52C 1152: ONEP JSR ONE
E6B3 BD E399 1153: JSR PLUS
E6B6 39 1154: RTS
1155: *
E6B7 82 1156: FCB \$82
E6B8 32 1157: FCC "2"
E6B9 AB 1158: FCB \$AB
E6BA E6 AB 1159: FDB ONEP-5
E6BC BD E535 1160: TWOP JSR TWO
E6BF BD E399 1161: JSR PLUS
E6C2 39 1162: RTS
1163: *
E6C3 84 1164: FCB \$84
E6C4 48 1165: FCC "HER"
E6C5 45 52
E6C7 C5 1166: FCB \$C5
E6C8 E6 B7 1167: FDB TWOP-5
E6CA BD E5E1 1168: HERE JSR DP
E6CD BD E44E 1169: JSR AT
E6D0 39 1170: RTS
1171: *
E6D1 85 1172: FCB \$85
E6D2 41 1173: FCC "ALLO"
E6D3 4C 4C
E6D5 4F
E6D6 D4 1174: FCB \$D4
E6D7 E6 C3 1175: FDB HERE-7
E6D9 BD E5E1 1176: ALLOT JSR DP
E6DC BD E420 1177: JSR PSTORE
E6DF 39 1178: RTS
1179: *
E6E0 81 1180: FCB \$81
E6E1 AC 1181: FCB \$AC
E6E2 E6 D1 1182: FDB ALLOT-8
E6E4 BD E6CA 1183: COMMA JSR HERE
E6E7 BD E46E 1184: JSR STORE
E6EA BD E535 1185: JSR TWO
E6ED BD E6D9 1186: JSR ALLOT
E6F0 39 1187: RTS
1188: *

FORTH

SSB MNEMONIC ASSEMBLER PAGE 23

E6F1	82	1189:	FCB	\$82	
E6F2	43	1190:	FCB	"C"	
E6F3	AC	1191:	FCB	\$AC	
E6F4	E6	E0	1192:	FDB	COMM-4
E6F6	BD	E6CA	1193:	JSR	HERE
E6F9	BD	E482	1194:	JSR	CSTORE
E6FC	BD	E52C	1195:	JSR	ONE
E6FF	BD	E6D9	1196:	JSR	ALLOT
E702	39	1197:	RTS		
		1198: *			
E703	81	1199:	FCB	\$81	
E704	AD	1200:	FCB	\$AD	
E705	E6	F1	1201:	FDB	COMM-5
E707	BD	E3C2	1202:	JSR	MINUS
E70A	BD	E399	1203:	JSR	PLUS
E70D	39	1204:	RTS		
		1205: *			
E70E	81	1206:	FCB	\$81	
E70F	BD	1207:	FCB	\$BD	
E710	E7	03	1208:	FDB	SUB-4
E712	BD	E707	1209:	JSR	SUB
E715	BD	E37B	1210:	JSR	ZEQU
E718	39	1211:	RTS		
		1212: *			
E719	81	1213:	FCB	\$81	
E71A	BC	1214:	FCB	\$BC	
E71B	E7	OE	1215:	FDB	EQUAL-4
E71D	EC	02	1216:	LESS	FDB \$EC02
					LDD 2,X
E71F	A1	04	1217:	CMP A	4,X
E721	2E	09	1218:	BGT	LESST
E723	26	04	1219:	BNE	LESSF
E725	E1	05	1220:	CMP B	5,X
E727	22	03	1221:	BHI	LESST
E729	5F	1222:	LESSF	CLR B	
E72A	20	02	1223:	BRA	LESSX
E72C	C6	01	1224:	LESST	LDA B #1
E72E	4F	1225:	LESSX	CLR A	
E72F	ED	04	1226:	FDB	\$ED04
					STD 4,X
E731	08	1227:		INX	
E732	08	1228:		INX	
E733	39	1229:	RTS		
		1230: *			
E734	81	1231:	FCB	\$81	
E735	BE	1232:	FCB	\$BE	
E736	E7	19	1233:	FDB	LESS-4
E738	BD	E401	1234:	JSR	SWAP
E73B	BD	E71D	1235:	JSR	LESS
E73E	39	1236:	RTS		
		1237: *			
E73F	83	1238:	FCB	\$83	
E740	52	1239:	FCB	"RO"	
E741	4F				
E742	D4	1240:	FCB	\$D4	
E743	E7	34	1241:	FDB	GREAT-4
E745	BD	E345	1242:	JSR	TOR
E748	BD	E401	1243:	JSR	SWAP
E74B	BD	E358	1244:	JSR	FROMR
E74E	BD	E401	1245:	JSR	SWAP
E751	39	1246:	RTS		
		1247: *			

FORTH

SSB MNEMONIC ASSEMBLER PAGE 24

E752 85	1248:	FCB	\$85
E753 53	1249:	FCC	"SPAC"
E754 50 41			
E756 43			
E757 C5	1250:	FCB	\$C5
E758 E7 3F	1251:	FDB	ROT-6
E75A BD E548	1252: SPACE	JSR	BL
E75D BD E1DC	1253:	JSR	EMIT
E760 39	1254:	RTS	
	1255: *		
E761 83	1256:	FCB	\$83
E762 4D	1257:	FCC	"MI"
E763 49			
E764 CE	1258:	FCB	\$CE
E765 E7 52	1259:	FDB	SPACE-8
E767 BD E3E9	1260: MIN	JSR	OVER
E76A BD E3E9	1261:	JSR	OVER
E76D BD E738	1262:	JSR	GREAT
E770 BD E06E	1263:	JSR	ZBRAN
E773 27 03	1264:	BEQ	MIN2
E775 BD E401	1265:	JSR	SWAP
E778 BD E3F7	1266: MIN2	JSR	DROP
E77B 39	1267:	RTS	
	1268: *		
E77C 83	1269:	FCB	\$83
E77D 4D	1270:	FCC	"MA"
E77E 41			
E77F D8	1271:	FCB	\$D8
E780 E7 61	1272:	FDB	MIN-6
E782 BD E3E9	1273: MAX	JSR	OVER
E785 BD E3E9	1274:	JSR	OVER
E788 BD E71D	1275:	JSR	LESS
E78B BD E06E	1276:	JSR	ZBRAN
E78E 27 03	1277:	BEQ	MAX2
E790 BD E401	1278:	JSR	SWAP
E793 BD E3F7	1279: MAX2	JSR	DROP
E796 39	1280:	RTS	
	1281: *		
E797 84	1282:	FCB	\$84
E798 2D	1283:	FCC	"-DU"
E799 44 55			
E79B DO	1284:	FCB	\$DO
E79C E7 7C	1285:	FDB	MAX-6
E79E BD E414	1286: DDUP	JSR	DUP
E7A1 BD E06E	1287:	JSR	ZBRAN
E7A4 27 03	1288:	BEQ	DDUP2
E7A6 BD E414	1289:	JSR	DUP
E7A9 39	1290: DDUP2	RTS	
	1291: *		
E7AA 88	1292:	FCB	\$88
E7AB 54	1293:	FCC	"TRavers"
E7AC 52 41			
E7AE 56 45			
E7B0 52 53			
E7B2 C5	1294:	FCB	\$C5
E7B3 E7 97	1295:	FDB	DDUP-7
E7B5 BD E401	1296: TRAV	JSR	SWAP
E7B8 BD E3E9	1297: TRAV2	JSR	OVER
E7BB BD E399	1298:	JSR	PLUS
E7BE BD E044	1299:	JSR	CLITER

FORTH

SSB MNEMONIC ASSEMBLER PAGE 25

E7C1 7F	1300:	FCB	\$7F
E7C2 BD E3E9	1301:	JSR	OVER
E7C5 BD E45E	1302:	JSR	CAT
E7C8 BD E71D	1303:	JSR	LESS
E7CB BD E06E	1304:	JSR	ZBRAN
E7CE 27 E8	1305:	BEQ	TRAV2
E7D0 BD E401	1306:	JSR	SWAP
E7D3 BD E3F7	1307:	JSR	DROP
E7D6 39	1308:	RTS	
	1309: *		
E7D7 86	1310:	FCB	\$86
E7D8 4C	1311:	FCC	"LATES"
E7D9 41 54			
E7DB 45 53			
E7DD D4	1312:	FCB	\$D4
E7DE E7 AA	1313:	FDB	TRAV-11
E7EO BD E648	1314: LATEST	JSR	CURENT
E7E3 BD E44E	1315:	JSR	AT
E7E6 BD E44E	1316:	JSR	AT
E7E9 39	1317:	RTS	
	1318: *		
E7EA 83	1319:	FCB	\$83
E7EB 4C	1320:	FCC	"LF"
E7EC 46			
E7ED C1	1321:	FCB	\$C1
E7EE E7 D7	1322:	FDB	LATEST-9
E7F0 BD E535	1323: LFA	JSR	TWO
E7F3 BD E707	1324:	JSR	SUB
E7F6 39	1325:	RTS	
	1326: *		
E7F7 83	1327:	FCB	\$83
E7F8 4E	1328:	FCC	"NF"
E7F9 46			
E7FA C1	1329:	FCB	\$C1
E7FB E7 EA	1330:	FDB	LFA-6
E7FD BD E53E	1331: NFA	JSR	THREE
E800 BD E707	1332:	JSR	SUB
E803 BD E52C	1333:	JSR	ONE
E806 BD E3C2	1334:	JSR	MINUS
E809 BD E7B5	1335:	JSR	TRAV
E80C 39	1336:	RTS	
	1337: *		
E80D 83	1338:	FCB	\$83
E80E 50	1339:	FCC	"FF"
E80F 46			
E810 C1	1340:	FCB	\$C1
E811 E7 F7	1341:	FDB	NFA-6
E813 BD E52C	1342: PFA	JSR	ONE
E816 BD E7B5	1343:	JSR	TRAV
E819 BD E53E	1344:	JSR	THREE
E81C BD E399	1345:	JSR	PLUS
E81F 39	1346:	RTS	
	1347: *		
E820 84	1348:	FCB	\$84
E821 21	1349:	FCC	"!CS"
E822 43 53			
E824 DO	1350:	FCB	\$DO
E825 E8 OD	1351:	FDB	PFA-6
E827 BD E307	1352: SCS	JSR	SPAT
E82A BD E682	1353:	JSR	CSP

FORTH

SSB MNEMONIC ASSEMBLER PAGE 26

E82D BD E46E 1354:	JSR	STORE
E830 39 1355:	RTS	
E831 86 1356: *		
E832 3F 1357:	FCB	\$86
E833 45 52 1358:	FCC	"?ERRO"
E835 52 4F		
E837 D2 1359:	FCB	\$D2
E838 E8 20 1360:	FDB	SCSP-7
E83A BD E401 1361: QERR	JSR	SWAP
E83D BD E06E 1362:	JSR	ZBRAN
E840 27 05 1363:	BEQ	QERR2
E842 BD EDD8 1364:	JSR	ERROR
E845 20 03 1365:	BRA	QERR3
E847 BD E3F7 1366: QERR2	JSR	DROP
E84A 39 1367: QERR3	RTS	
E84B 85 1368: *		
E84C 3F 1369:	FCB	\$85
E84D 43 4F 1370:	FCC	"?COM"
E84F 4D		
E850 DO 1371:	FCB	\$DO
E851 E8 31 1372:	FDB	QERR-9
E853 BD E655 1373: QCMP	JSR	STATE
E856 BD E44E 1374:	JSR	AT
E859 BD E37B 1375:	JSR	ZEQU
E85C BD E044 1376:	JSR	CLITER
E85F 11 1377:	FCB	\$11
E860 BD E83A 1378:	JSR	QERR
E863 39 1379:	RTS	
E864 85 1380: *		
E865 3F 1381:	FCB	\$85
E866 45 58 1382:	FCC	"?EXE"
E868 45		
E869 C3 1383:	FCB	\$C3
E86A E8 4B 1384:	FDB	QCMP-8
E86C BD E655 1385: QEXEC	JSR	STATE
E86F BD E44E 1386:	JSR	AT
E872 BD E044 1387:	JSR	CLITER
E875 12 1388:	FCB	\$12
E876 BD E83A 1389:	JSR	QERR
E879 39 1390:	RTS	
E87A 86 1391: *		
E87B 3F 1392:	FCB	\$86
E87C 50 41 1393:	FCC	"?PAIR"
E87E 49 52		
E880 D3 1394:	FCB	\$D3
E881 E8 64 1395:	FDB	QEXEC-8
E883 BD E707 1396: QPAIRS	JSR	SUB
E886 BD E044 1397:	JSR	CLITER
E889 13 1398:	FCB	\$13
E88A BD E83A 1399:	JSR	QERR
E88D 39 1400:	RTS	
E88E 84 1401: *		
E88F 3F 1402:	FCB	\$84
E890 43 53 1403:	FCC	"?CS"
E892 DO 1404:	FCB	\$DO

FORTH

SSB MNEMONIC ASSEMBLER PAGE 27

E893 E8 7A 1405:	FDB	QPAIRS-9
E895 BD E307 1406: QCSP	JSR	SPAT
E898 BD E682 1407:	JSR	CSP
E89B BD E44E 1408:	JSR	AT
E89E BD E707 1409:	JSR	SUB
E8A1 BD E044 1410:	JSR	CLITER
E8A4 14 1411:	FCB	\$14
E8A5 BD E83A 1412:	JSR	QERR
E8A8 39 1413:	RTS	
	1414: *	
E8A9 88 1415:	FCB	\$88
E8AA 3F 1416:	FCC	"?LOADIN"
E8AB 4C 4F		
E8AD 41 44		
E8AF 49 4E		
E8B1 C7 1417:	FCB	\$C7
E8B2 E8 8E 1418:	FDB	QCSP-7
E8B4 BD E5FC 1419: QLOAD	JSR	BLK
E8B7 BD E44E 1420:	JSR	AT
E8BA BD E37B 1421:	JSR	ZEQU
E8BD BD E044 1422:	JSR	CLITER
E8C0 16 1423:	FCB	\$16
E8C1 BD E83A 1424:	JSR	QERR
E8C4 39 1425:	RTS	
	1426: *	
E8C5 87 1427:	FCB	\$87
E8C6 43 1428:	FCC	"COMPIL"
E8C7 4F 4D		
E8C9 50 49		
E8CB 4C		
E8CC C5 1429:	FCB	\$C5
E8CD E8 A9 1430:	FDB	QLOAD-11
E8CF BD E853 1431: COMPIL	JSR	QCOMP
E8D2 BD E358 1432:	JSR	FROMR
E8D5 BD E414 1433:	JSR	DUP
E8D8 BD E45E 1434:	JSR	CAT
E8DB BD E6F6 1435:	JSR	CCOMM
E8DE BD E6B0 1436:	JSR	ONEP
E8E1 BD E414 1437:	JSR	DUP
E8E4 BD E44E 1438:	JSR	AT
E8E7 BD E6E4 1439:	JSR	COMMA
E8EA BD E6BC 1440:	JSR	TWOP
E8ED BD E345 1441:	JSR	TOR
E8FO 39 1442:	RTS	
	1443: *	
E8F1 C1 1444:	FCB	\$C1
E8F2 DB 1445:	FCB	\$DB
E8F3 E8 C5 1446:	FDB	COMPIL-10
E8F5 BD E523 1447: LBRAK	JSR	ZERO
E8F8 BD E655 1448:	JSR	STATE
E8FB BD E46E 1449:	JSR	STORE
E8FE 39 1450:	RTS	
	1451: *	
E8FF 81 1452:	FCB	\$81
E900 DD 1453:	FCB	\$DD
E901 E8 F1 1454:	FDB	LBRAK-4
E903 BD E044 1455: RBRAK	JSR	CLITER
E906 CO 1456:	FCB	\$CO
E907 BD E655 1457:	JSR	STATE
E90A BD E46E 1458:	JSR	STORE

FORTH

SSB MNEMONIC ASSEMBLER PAGE 28

E90D 39	1459:	RTS	
	1460: *		
E90E 86	1461:	FCB	\$86
E90F 53	1462:	FCC	"SMUDG"
E910 4D 55			
E912 44 47			
E914 C5	1463:	FCB	\$C5
E915 E8 FF	1464:	FDB	RBRAK-4
E917 BD E7EO	1465: SMUDGE	JSR	LATEST
E91A BD E044	1466:	JSR	CLITER
E91D 20	1467:	FCB	\$20
E91E BD E43A	1468:	JSR	TOGGLE
E921 39	1469:	RTS	
	1470: *		
E922 83	1471:	FCB	\$83
E923 48	1472:	FCC	"HE"
E924 45			
E925 D8	1473:	FCB	\$D8
E926 E9 OE	1474:	FDB	SMUDGE-9
E928 BD E044	1475: HEX	JSR	CLITER
E92B 10	1476:	FCB	16
E92C BD E661	1477:	JSR	BASE
E92F BD E46E	1478:	JSR	STORE
E932 39	1479:	RTS	
	1480: *		
E933 87	1481:	FCB	\$87
E934 44	1482:	FCC	"DECIMA"
E935 45 43			
E937 49 4D			
E939 41			
E93A CC	1483:	FCB	\$CC
E93B E9 22	1484:	FDB	HEX-6
E93D BD E044	1485: DEC	JSR	CLITER
E940 0A	1486:	FCB	10
E941 BD E661	1487:	JSR	BASE
E944 BD E46E	1488:	JSR	STORE
E947 39	1489:	RTS	
	1490: *		
E948 87	1491:	FCB	\$87
E949 28	1492:	FCC	"(;CODE"
E94A 3B 43			
E94C 4F 44			
E94E 45			
E94F A9	1493:	FCB	\$A9
E950 E9 33	1494:	FDB	DEC-10
E952 BD E358	1495: PSCODE	JSR	FROMR
E955 BD E7EO	1496:	JSR	LATEST
E958 BD E813	1497:	JSR	PFA
E95B BD E044	1498:	JSR	CLITER
E95E BD	1499:	FCB	\$BD
E95F BD E3E9	1500:	JSR	OVER
E962 BD E482	1501:	JSR	CSTORE
E965 BD E6B0	1502:	JSR	ONEP
E968 BD E46E	1503:	JSR	STORE
E96B 39	1504:	RTS	
	1505: *		
E96C C5	1506:	FCB	\$C5
E96D 3B	1507:	FCC	";COD"
E96E 43 4F			
E970 44			

FORTH

SSB MNEMONIC ASSEMBLER PAGE 29

E971 C5	1508:	FCB	\$C5
E972 E9 48	1509:	FDB	PSCODE-10
E974 BD E895	1510: SEMIC	JSR	QCSP
E977 BD E8CF	1511:	JSR	COMPILE
E97A BD E952	1512:	JSR	PSCODE
E97D BD E8F5	1513:	JSR	LBRAK
E980 BD EA8E	1514:	JSR	QSTACK
E983 39	1515:	RTS	
	1516: *		
E984 87	1517:	FCB	\$87
E985 3C	1518:	FCC	"<BUILD"
E986 42 55			
E988 49 4C			
E98A 44			
E98B D3	1519:	FCB	\$D3
E98C E9 6C	1520:	FDB	SEMIC-8
E98E BD E523	1521: BUILDS	JSR	ZERO
E991 BD E4CE	1522:	JSR	CON
E994 BD E52C	1523:	JSR	ONE
E997 BD E6D9	1524:	JSR	ALLOT
E99A 39	1525:	RTS	
	1526: *		
E99B 85	1527:	FCB	\$85
E99C 44	1528:	FCC	"DOES"
E99D 4F 45			
E99F 53			
E9A0 BE	1529:	FCB	\$BE
E9A1 E9 84	1530:	FDB	BUILDS-10
E9A3 BD E358	1531: DOES	JSR	FROMR
E9A6 BD E7E0	1532:	JSR	LATEST
E9A9 BD E813	1533:	JSR	PFA
E9AC BD E53E	1534:	JSR	THREE
E9AF BD E399	1535:	JSR	PLUS
E9B2 BD E044	1536:	JSR	CLITER
E9B5 7E	1537:	FCB	\$7E
E9B6 BD E3E9	1538:	JSR	OVER
E9B9 BD E482	1539:	JSR	CSTORE
E9BC BD E6B0	1540:	JSR	ONEP
E9BF BD E46E	1541:	JSR	STORE
E9C2 BD E952	1542:	JSR	PSCODE
E9C5 BD E36A	1543: DODDOES	JSR	R
E9C8 BD E53E	1544:	JSR	THREE
E9CB BD E399	1545:	JSR	PLUS
E9CE 39	1546:	RTS	
	1547: *		
E9CF 85	1548:	FCB	\$85
E9D0 43	1549:	FCC	"COUN"
E9D1 4F 55			
E9D3 4E			
E9D4 D4	1550:	FCB	\$D4
E9D5 E9 98	1551:	FDB	DOES-8
E9D7 BD E414	1552: COUNT	JSR	DUP
E9DA BD E6B0	1553:	JSR	ONEP
E9DD BD E401	1554:	JSR	SWAP
E9EO BD E45E	1555:	JSR	CAT
E9E3 39	1556:	RTS	
	1557: *		
E9E4 84	1558:	FCB	\$84
E9E5 54	1559:	FCC	"TYP"
E9E6 59 50			

FORTH

SSB MNEMONIC ASSEMBLER PAGE 30

E9E8 C5	1560:	FCB	\$C5
E9E9 E9 CF	1561:	FDB	COUNT-B
E9EB BD E79E	1562: TYPE	JSR	DDUP
E9EE BD E06E	1563:	JSR	ZBRAN
E9F1 27 23	1564:	BEQ	TYPE3
E9F3 BD E3E9	1565:	JSR	OVER
E9F6 BD E399	1566:	JSR	PLUS
E9F9 BD E401	1567:	JSR	SWAP
E9FC BD E0C1	1568:	JSR	XDO
E9FF BD E0DA	1569: TYPE2	JSR	I
EA02 BD E45E	1570:	JSR	CAT
EA05 BD E044	1571:	JSR	CLITER
EA08 7F	1572:	FCB	\$7F
EA09 BD E2D5	1573:	JSR	AND
EA0C BD E1DC	1574:	JSR	EMIT
EA0F BD E07C	1575:	JSR	XLOOP
EA12 27 EB	1576:	BEQ	TYPE2
EA14 20 03	1577:	BRA	TYPE4
EA16 BD E3F7	1578: TYPE3	JSR	DROP
EA19 39	1579: TYPE4	RTS	
	1580: *		
EA1A 89	1581:	FCB	\$89
EA1B 2D	1582:	FCC	"-TRAILIN"
EA1C 54 52			
EA1E 41 49			
EA20 4C 49			
EA22 4E			
EA23 C7	1583:	FCB	\$C7
EA24 E9 E4	1584:	FDB	TYPE-7
EA26 BD E414	1585: DTRAIL	JSR	DUP
EA29 BD E523	1586:	JSR	ZERO
EA2C BD E0C1	1587:	JSR	XDO
EA2F BD E3E9	1588: DTRAL2	JSR	OVER
EA32 BD E3E9	1589:	JSR	OVER
EA35 BD E399	1590:	JSR	PLUS
EA38 BD E52C	1591:	JSR	ONE
EA3B BD E707	1592:	JSR	SUB
EA3E BD E45E	1593:	JSR	CAT
EA41 BD E548	1594:	JSR	BL
EA44 BD E707	1595:	JSR	SUB
EA47 BD E06E	1596:	JSR	ZBRAN
EA4A 27 05	1597:	BEQ	DTRAL3
EA4C BD E336	1598:	JSR	LEAVE
EA4F 20 06	1599:	BRA	DTRAL4
EA51 BD E52C	1600: DTRAL3	JSR	ONE
EA54 BD E707	1601:	JSR	SUB
EA57 BD E07C	1602: DTRAL4	JSR	XLOOP
EA5A 27 D3	1603:	BEQ	DTRAL2
EA5C 39	1604:	RTS	
	1605: *		
EA5D 84	1606:	FCB	\$84
EA5E 28	1607:	FCC	/ . . /
EA5F 2E 22			
EA61 A9	1608:	FCB	\$A9
EA62 EA 1A	1609:	FDB	DTRAIL-12
EA64 BD E36A	1610: PDOTQ	JSR	R
EA67 BD E9D7	1611:	JSR	COUNT
EA6A BD E414	1612:	JSR	DUP
EA6D BD E6B0	1613:	JSR	ONEP
EA70 BD E358	1614:	JSR	FROMR

FORTH

SSB MNEMONIC ASSEMBLER PAGE 31

EA73 BD E399	1615:	JSR	PLUS
EA76 BD E345	1616:	JSR	TOR
EA79 BD E9EB	1617:	JSR	TYPE
EA7C 39	1618:	RTS	
	1619: *		
EA7D C2	1620:	FCB	\$C2
EA7E 2E	1621:	FCC	". "
EA7F A2	1622:	FCB	\$A2
EA80 EA 5D	1623:	FDB	PDOTQ-7
EA82 BD E044	1624: DOTQ	JSR	CLITER
EA85 22	1625:	FCB	\$22
EA86 BD E655	1626:	JSR	STATE
EA89 BD E44E	1627:	JSR	AT
EA8C BD E06E	1628:	JSR	ZBRAN
EA8F 27 17	1629:	BEQ	DOTQ1
EA91 BD E8CF	1630:	JSR	COMPIL
EA94 BD EA64	1631:	JSR	PDOTQ
EA97 BD EC5C	1632:	JSR	WORD
EA9A BD E6CA	1633:	JSR	HERE
EA9D BD E45E	1634:	JSR	CAT
EAA0 BD E6B0	1635:	JSR	ONEP
EAA3 BD E6D9	1636:	JSR	ALLOT
EAA6 20 OC	1637:	BRA	DOTQ2
EAA8 BD EC5C	1638: DOTQ1	JSR	WORD
EAA9 BD E6CA	1639:	JSR	HERE
EAAE BD E9D7	1640:	JSR	COUNT
EAB1 BD E9EB	1641:	JSR	TYPE
EAB4 39	1642: DOTQ2	RTS	
	1643: *		
EAB5 86	1644:	FCB	\$86
EAB6 3F	1645:	FCC	"?STAC"
EAB7 53 54			
EAB9 41 43			
EABB CB	1646:	FCB	\$CB
EABC EA 7D	1647:	FDB	DOTQ-5
EABE BD E044	1648: QSTACK	JSR	CLITER
EAC1 12	1649:	FCB	\$12
EAC2 BD E58B	1650:	JSR	PORIG
EAC5 BD E44E	1651:	JSR	AT
EAC8 BD E52C	1652:	JSR	ONE
EACB BD E707	1653:	JSR	SUB
EACE BD E307	1654:	JSR	SPAT
EAD1 BD E71D	1655:	JSR	LESS
EAD4 BD E52C	1656:	JSR	ONE
EAD7 BD E83A	1657:	JSR	QERR
EADA BD E307	1658: QSTAC2	JSR	SPAT
EADD BD E02C	1659:	JSR	LIT
EAE0 DO 00	1660:	FDB	\$D000
EAE2 BD E71D	1661:	JSR	LESS
EAE5 BD E06E	1662:	JSR	ZBRAN
EAE8 27 06	1663:	BEQ	QSTAC3
EAEA BD E535	1664:	JSR	TWO
EAEF BD E83A	1665:	JSR	QERR
EAFO 39	1666: QSTAC3	RTS	
	1667: *		
EAF1 86	1668:	FCB	\$86
EAF2 45	1669:	FCC	"EXPEC"
EAF3 58 50			
EAF5 45 43			
EAF7 D4	1670:	FCB	\$D4

FORTH

SSB MNEMONIC ASSEMBLER PAGE 32

EAF8 EA B5	1671:	FDB	QSTACK-9
EAFA BD E3E9	1672:	EXPECT	JSR OVER
EAFD BD E399	1673:	JSR	PLUS
EB00 BD E3E9	1674:	JSR	OVER
EB03 BD E0C1	1675:	JSR	XDO
EB06 BD E1F6	1676:	EXPEC2	JSR KEY
EB09 BD E414	1677:	JSR	DUP
EBOC BD E044	1678:	JSR	CLITER
EBOF OE	1679:	FCB	\$OE
EB10 BD E58B	1680:	JSR	PORIG
EB13 BD E44E	1681:	JSR	AT
EB16 BD E712	1682:	JSR	EQUAL
EB19 BD E06E	1683:	JSR	ZBRAN
EB1C 27 27	1684:	BEQ	EXPEC3
EB1E BD E3F7	1685:	JSR	DROP
EB21 BD E044	1686:	JSR	CLITER
EB24 08	1687:	FCB	8
EB25 BD E3E9	1688:	JSR	OVER
EB28 BD E0DA	1689:	JSR	I
EB2B BD E712	1690:	JSR	EQUAL
EB2E BD E414	1691:	JSR	DUP
EB31 BD E358	1692:	JSR	FROMR
EB34 BD E535	1693:	JSR	TWO
EB37 BD E707	1694:	JSR	SUB
EB3A BD E399	1695:	JSR	PLUS
EB3D BD E345	1696:	JSR	TOR
EB40 BD E707	1697:	JSR	SUB
EB43 20 32	1698:	BRA	EXPEC6
EB45 BD E414	1699:	EXPEC3	JSR DUP
EB48 BD E044	1700:	JSR	CLITER
EB4B OD	1701:	FCB	\$D
EB4C BD E712	1702:	JSR	EQUAL
EB4F BD E06E	1703:	JSR	ZBRAN
EB52 27 OE	1704:	BEQ	EXPEC4
EB54 BD E336	1705:	JSR	LEAVE
EB57 BD E3F7	1706:	JSR	DROP
EB5A BD E548	1707:	JSR	BL
EB5D BD E523	1708:	JSR	ZERO
EB60 20 03	1709:	BRA	EXPEC5
EB62 BD E414	1710:	EXPEC4	JSR DUP
EB65 BD E0DA	1711:	EXPEC5	JSR I
EB68 BD E482	1712:	JSR	CSTORE
EB6B BD E523	1713:	JSR	ZERO
EB6E BD E0DA	1714:	JSR	I
EB71 BD E6B0	1715:	JSR	ONEP
EB74 BD E46E	1716:	JSR	STORE
EB77 BD E1DC	1717:	EXPEC6	JSR EMIT
EB7A BD E07C	1718:	JSR	XLOOP
EB7D 27 87	1719:	BEQ	EXPEC2
EB7F BD E3F7	1720:	JSR	DROP
EB82 39	1721:	RTS	
	1722:	*	
EB83 85	1723:	FCB	\$85
EB84 51	1724:	FCC	"QUER"
EB85 55 45			
EB87 52			
EB88 D9	1725:	FCB	\$D9
EB89 EA F1	1726:	FDB	EXPECT-9
EB8B BD E5AE	1727:	QUERY	JSR TIB
EB8E BD E44E	1728:	JSR	AT

FORTH SSB MNEMONIC ASSEMBLER PAGE 33

EB91 BD E6A6 1729:	JSR	COLUMNS
EB94 BD E44E 1730:	JSR	AT
EB97 BD EAFA 1731:	JSR	EXPECT
EB9A BD E523 1732:	JSR	ZERO
EB9D BD E606 1733:	JSR	IN
EBA0 BD E46E 1734:	JSR	STORE
EBA3 39 1735:	RTS	
1736: *		
EBA4 C1 1737:	FCB	\$C1
EBA5 80 1738:	FCB	\$80
EBA6 EB 83 1739:	FDB	QUERY-8
EBA8 BD E5FC 1740:	NULL	JSR BLK
EBA9 BD E44E 1741:	JSR	AT
EBAE BD E06E 1742:	JSR	ZBRAN
EBA1 27 29 1743:	BEQ	NULL2
EBA3 BD E52C 1744:	JSR	ONE
EBA6 BD E5FC 1745:	JSR	BLK
EBA9 BD E420 1746:	JSR	PSTORE
EBC0 BD E523 1747:	JSR	ZERO
EBCF BD E606 1748:	JSR	IN
EBC2 BD E46E 1749:	JSR	STORE
EBC5 BD E5FC 1750:	JSR	BLK
EBC8 BD E44E 1751:	JSR	AT
EBCB BD E57C 1752:	JSR	BSCR
EBCF BD F185 1753:	JSR	MOD
EBD1 BD E37B 1754:	JSR	ZEQU
EBD4 BD E06E 1755:	JSR	ZBRAN
EBD7 27 09 1756:	BEQ	NULL3
EBD9 BD E86C 1757:	JSR	QEXEC
EBCD BD E358 1758:	NULL2	JSR FROMR
EBCF BD E3F7 1759:	JSR	DROP
EBC2 39 1760:	NULL3	RTS
1761: *		
EBC3 84 1762:	FCB	\$84
EBC4 46 1763:	FCC	"FIL"
EBC5 49 4C		
EBC7 CC 1764:	FCB	\$CC
EBC8 EB A4 1765:	FDB	NULL-4
EBCA BD E401 1766:	FILL	JSR SWAP
EBCD BD E345 1767:	JSR	TOR
EBC0 BD E3E9 1768:	JSR	OVER
EBC3 BD E482 1769:	JSR	CSTORE
EBC6 BD E414 1770:	JSR	DUP
EBC9 BD E6B0 1771:	JSR	ONEP
EBCF BD E358 1772:	JSR	FROMR
EBCF BD E52C 1773:	JSR	ONE
ECD2 BD E707 1774:	JSR	SUB
ECD5 BD E22D 1775:	JSR	CMOVE
ECD8 39 1776:	RTS	
1777: *		
ECD9 85 1778:	FCB	\$85
ECD4 45 1779:	FCC	"ERAS"
ECD8 52 41		
ECD3 53		
ECD6 C5 1780:	FCB	\$C5
ECD7 EB E3 1781:	FDB	FILL-7
ECD11 BD E523 1782:	ERASE	JSR ZERO
ECD14 BD EBEA 1783:	JSR	FILL
ECD17 39 1784:	RTS	
1785: *		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 34

EC18 86	1786:	FCB	\$86
EC19 42	1787:	FCC	"BLANK"
EC1A 4C 41			
EC1C 4E 4B			
EC1E D3	1788:	FCB	\$D3
EC1F EC 09	1789:	FDB	ERASE-8
EC21 BD E548	1790: BLANKS	JSR	BL
EC24 BD EBEA	1791:	JSR	FILL
EC27 39	1792:	RTS	
	1793: *		
EC28 84	1794:	FCB	\$84
EC29 48	1795:	FCC	"HOL"
EC2A 4F 4C			
EC2C C4	1796:	FCB	\$C4
EC2D EC 18	1797:	FDB	BLANKS-9
EC2F BD E02C	1798: HOLD	JSR	LIT
EC32 FF FF	1799:	FDB	\$FFFF
EC34 BD E697	1800:	JSR	HLD
EC37 BD E420	1801:	JSR	PSTORE
EC3A BD E697	1802:	JSR	HLD
EC3D BD E44E	1803:	JSR	AT
EC40 BD E482	1804:	JSR	CSTORE
EC43 39	1805:	RTS	
	1806: *		
EC44 83	1807:	FCB	\$83
EC45 50	1808:	FCC	"PA"
EC46 41			
EC47 C4	1809:	FCB	\$C4
EC48 EC 28	1810:	FDB	HOLD-7
EC4A BD E6CA	1811: PAD	JSR	HERE
EC4D BD E044	1812:	JSR	CLITER
EC50 44	1813:	FCB	\$44
EC51 BD E399	1814:	JSR	PLUS
EC54 39	1815:	RTS	
	1816: *		
EC55 84	1817:	FCB	\$84
EC56 57	1818:	FCC	"WOR"
EC57 4F 52			
EC59 C4	1819:	FCB	\$C4
EC5A EC 44	1820:	FDB	PAD-6
EC5C BD E5FC	1821: WORD	JSR	BLK
EC5F BD E44E	1822:	JSR	AT
EC62 BD E06E	1823:	JSR	ZBRAN
EC65 27 0B	1824:	BEQ	WORD2
EC67 BD E5FC	1825:	JSR	BLK
EC6A BD E44E	1826:	JSR	AT
EC6D BD F314	1827:	JSR	BLOCK
EC70 20 06	1828:	BRA	WORD3
EC72 BD E5AE	1829: WORD2	JSR	TIB
EC75 BD E44E	1830:	JSR	AT
EC78 BD E606	1831: WORD3	JSR	IN
EC7B BD E44E	1832:	JSR	AT
EC7E BD E399	1833:	JSR	PLUS
EC81 BD E401	1834:	JSR	SWAP
EC84 BD E18A	1835:	JSR	ENCLOS
EC87 BD E6CA	1836:	JSR	HERE
EC8A BD E044	1837:	JSR	CLITER
EC8D 22	1838:	FCB	34
EC8E BD EC21	1839:	JSR	BLANKS
EC91 BD E606	1840:	JSR	IN

FORTH

SSB MNEMONIC ASSEMBLER PAGE 35

EC94 BD E420 1841:	JSR	PSTORE
EC97 BD E3E9 1842:	JSR	OVER
EC9A BD E707 1843:	JSR	SUB
EC9D BD E345 1844:	JSR	TOR
ECA0 BD E36A 1845:	JSR	R
ECA3 BD E6CA 1846:	JSR	HERE
ECA6 BD E482 1847:	JSR	CSTORE
ECA9 BD E399 1848:	JSR	PLUS
ECAC BD E6CA 1849:	JSR	HERE
ECAF BD E680 1850:	JSR	ONEP
ECB2 BD E358 1851:	JSR	FROMR
ECB5 BD E22D 1852:	JSR	CMOVE
ECB8 39 1853:	RTS	
1854: *		
ECB9 88 1855:	FCB	\$88
ECBA 28 1856:	FCC	"(NUMBER"
ECBB 4E 55		
ECBD 4D 42		
ECBF 45 52		
ECC1 A9 1857:	FCB	\$A9
ECC2 EC 55 1858:	FDB	WORD-7
ECC4 BD E680 1859: PNUMB	JSR	ONEP
ECC7 BD E414 1860:	JSR	DUP
ECCA BD E345 1861:	JSR	TOR
ECCD BD E45E 1862:	JSR	CAT
ECD0 BD E661 1863:	JSR	BASE
ECD3 BD E44E 1864:	JSR	AT
ECD6 BD E0EE 1865:	JSR	DIGIT
ECD9 BD E06E 1866:	JSR	ZBRAN
ECDC 27 3A 1867:	BEQ	PNUMB4
ECDE BD E401 1868:	JSR	SWAP
ECE1 BD E661 1869:	JSR	BASE
ECE4 BD E44E 1870:	JSR	AT
ECE7 BD E262 1871:	JSR	USTAR
ECEA BD E3F7 1872:	JSR	DROP
ECED BD E745 1873:	JSR	ROT
ECFO BD E661 1874:	JSR	BASE
ECF3 BD E44E 1875:	JSR	AT
ECF6 BD E262 1876:	JSR	USTAR
ECF9 BD E3A7 1877:	JSR	DPLUS
ECFC BD E66C 1878:	JSR	DPL
ECFF BD E44E 1879:	JSR	AT
ED02 BD E680 1880:	JSR	ONEP
ED05 BD E06E 1881:	JSR	ZBRAN
ED08 27 09 1882:	BEQ	PNUMB3
ED0A BD E52C 1883:	JSR	ONE
ED0D BD E66C 1884:	JSR	DPL
ED10 BD E420 1885:	JSR	PSTORE
ED13 BD E358 1886: PNUMB3	JSR	FROMR
ED16 20 AC 1887:	BRA	PNUMB
ED18 BD E358 1888: PNUMB4	JSR	FROMR
ED1B 39 1889:	RTS	
1890: *		
ED1C 86 1891:	FCB	\$86
ED1D 4E 1892:	FCC	"NUMBE"
ED1E 55 4D		
ED20 42 45		
ED22 D2 1893:	FCB	\$D2
ED23 EC B9 1894:	FDB	PNUMB-11
ED25 BD E523 1895: NUMB	JSR	ZERO

FORTH

SSB MNEMONIC ASSEMBLER PAGE 36

ED28 BD E523 1896:	JSR	ZERO
ED2B BD E745 1897:	JSR	ROT
ED2E BD E414 1898:	JSR	DUP
ED31 BD E6B0 1899:	JSR	ONEP
ED34 BD E45E 1900:	JSR	CAT
ED37 BD E044 1901:	JSR	CLITER
ED3A 2D 1902:	FCC	"-"
ED3B BD E712 1903:	JSR	EQUAL
ED3E BD E414 1904:	JSR	DUP
ED41 BD E345 1905:	JSR	TOR
ED44 BD E399 1906:	JSR	PLUS
ED47 BD E02C 1907:	JSR	LIT
ED4A FF FF 1908:	FDB	\$FFFF
ED4C BD E66C 1909: NUMB1	JSR	DPL
ED4F BD E46E 1910:	JSR	STORE
ED52 BD ECC4 1911:	JSR	PNUMB
ED55 BD E414 1912:	JSR	DUP
ED58 BD E45E 1913:	JSR	CAT
ED5B BD E548 1914:	JSR	BL
ED5E BD E707 1915:	JSR	SUB
ED61 BD E06E 1916:	JSR	ZBRAN
ED64 27 18 1917:	BEQ	NUMB2
ED66 BD E414 1918:	JSR	DUP
ED69 BD E45E 1919:	JSR	CAT
ED6C BD E044 1920:	JSR	CLITER
ED6F 2E 1921:	FCC	". "
ED70 BD E707 1922:	JSR	SUB
ED73 BD E523 1923:	JSR	ZERO
ED76 BD E83A 1924:	JSR	QERR
ED79 BD E523 1925:	JSR	ZERO
ED7C 20 CE 1926:	BRA	NUMB1
ED7E BD E3F7 1927: NUMB2	JSR	DROP
ED81 BD E358 1928:	JSR	FROMR
ED84 BD E06E 1929:	JSR	ZBRAN
ED87 27 03 1930:	BEQ	NUMB3
ED89 BD E3D2 1931:	JSR	DMINUS
ED8C 39 1932: NUMB3	RTS	
1933: *		
ED8D 85 1934:	FCB	\$85
ED8E 2D 1935:	FCC	"-FIN"
ED8F 46 49		
ED91 4E		
ED92 C4 1936:	FCB	\$C4
ED93 ED 1C 1937:	FDB	NUMB-9
ED95 BD E548 1938: DFIND	JSR	BL
ED98 BD EC5C 1939:	JSR	WORD
ED9B BD E6CA 1940:	JSR	HERE
ED9E BD E639 1941:	JSR	CONTXT
EDA1 BD E44E 1942:	JSR	AT
EDA4 BD E44E 1943:	JSR	AT
EDA7 BD E11D 1944:	JSR	PFIND
EDAA BD E414 1945:	JSR	DUP
EDAD BD E37B 1946:	JSR	ZEQU
EDBO BD E06E 1947:	JSR	ZBRAN
EDB3 27 0C 1948:	BEQ	DFIND2
EDB5 BD E3F7 1949:	JSR	DROP
EDB8 BD E6CA 1950:	JSR	HERE
EDBB BD E7E0 1951:	JSR	LATEST
EDBE BD E11D 1952:	JSR	PFIND
EDC1 39 1953: DFIND2	RTS	

FORTH

SSB MNEMONIC ASSEMBLER PAGE 37

	1954: *		
EDC2 87	1955:	FCB	\$87
EDC3 28	1956:	FCC	"(ABORT"
EDC4 41 42			
EDC6 4F 52			
EDC8 54			
EDC9 A9	1957:	FCB	\$A9
EDCA ED BD	1958:	FDB	DFIND-8
EDCC BD F055	1959: PABORT	JSR	ABORT "
EDCF 39	1960:	RTS	
	1961: *		
EDDO 85	1962:	FCB	\$85
EDD1 45	1963:	FCC	"ERRO"
EDD2 52 52			
EDD4 4F			
EDD5 D2	1964:	FCB	\$D2
EDD6 ED C2	1965:	FDB	PABORT-10
EDD8 BD E5CA	1966: ERROR	JSR	WARN
EDDB BD E44E	1967:	JSR	AT
EDDE BD E38B	1968:	JSR	ZLESS
EDE1 BD E06E	1969:	JSR	ZBRAN
EDE4 27 03	1970:	BEQ	ERROR2
EDE6 BD EDCC	1971:	JSR	PABORT
EDE9 BD E6CA	1972: ERROR2	JSR	HERE
EDEC BD E9D7	1973:	JSR	COUNT
EDEF BD E9EB	1974:	JSR	TYPE
EDF2 BD EA64	1975:	JSR	PDOTQ
EDF5 04	1976:	FCB	4,7
EDF6 07			
EDF7 20	1977:	FCC	" ? "
EDFB 3F 20			
EDFA BD F3D9	1978:	JSR	MESS
EDFD BD E312	1979:	JSR	SPSTOR
EE00 BD E606	1980:	JSR	IN
EE03 BD E44E	1981:	JSR	AT
EE06 BD E5FC	1982:	JSR	BLK
EE09 BD E44E	1983:	JSR	AT
EE0C BD F00A	1984:	JSR	QUIT
EE0F 39	1985:	RTS	
	1986: *		
EE10 83	1987:	FCB	\$83
EE11 49	1988:	FCC	"ID"
EE12 44			
EE13 AE	1989:	FCB	\$AE
EE14 ED DO	1990:	FDB	ERROR-8
EE16 BD EC4A	1991: IDDOT	JSR	PAD
EE19 BD E044	1992:	JSR	CLITER
EE1C 20	1993:	FCB	32
EE1D BD E044	1994:	JSR	CLITER
EE20 5F	1995:	FCB	\$5F
EE21 BD EBEA	1996:	JSR	FILL
EE24 BD E414	1997:	JSR	DUP
EE27 BD E813	1998:	JSR	PFA
EE2A BD E7F0	1999:	JSR	LFA
EE2D BD E3E9	2000:	JSR	OVER
EE30 BD E707	2001:	JSR	SUB
EE33 BD EC4A	2002:	JSR	PAD
EE36 BD E401	2003:	JSR	SWAP
EE39 BD E22D	2004:	JSR	CMOVE
EE3C BD EC4A	2005:	JSR	PAD

FORTH

SSB MNEMONIC ASSEMBLER PAGE 38

EE3F BD E9D7 2006:	JSR	COUNT
EE42 BD E044 2007:	JSR	CLITER
EE45 1F 2008:	FCB	31
EE46 BD E2D5 2009:	JSR	AND
EE49 BD E9EB 2010:	JSR	TYPE
EE4C BD E75A 2011:	JSR	SPACE
EE4F 39 2012:	RTS	
EE4F 39 2013: *		
EE50 86 2014:	FCB	\$86
EE51 43 2015:	FCC	"CREAT"
EE52 52 45		
EE54 41 54		
EE56 C5 2016:	FCB	\$C5
EE57 EE 10 2017:	FDB	IDDOT-6
EE59 BD ED95 2018:	CREATE	JSR DFIN
EE5C BD E06E 2019:	JSR	ZBRAN
EE5F 27 1F 2020:	BEQ	CREAT2
EE61 BD E3F7 2021:	JSR	DROP
EE64 BD EA64 2022:	JSR	PDOTQ
EE67 08 2023:	FCB	8
EE68 07 2024:	FCB	7
EE69 72 2025:	FCC	"redef: "
EE6A 65 64		
EE6C 65 66		
EE6E 3A 20		
EE70 BD E7FD 2026:	JSR	NFA
EE73 BD EE16 2027:	JSR	IDDOT
EE76 BD E044 2028:	JSR	CLITER
EE79 04 2029:	FCB	4
EE7A BD F3D9 2030:	JSR	MESS
EE7D BD E75A 2031:	JSR	SPACE
EE80 BD E6CA 2032:	CREATE	JSR HERE
EE83 BD E414 2033:	JSR	DUP
EE86 BD E45E 2034:	JSR	CAT
EE89 BD E5BB 2035:	JSR	WIDTH
EE8C BD E44E 2036:	JSR	AT
EE8F BD E767 2037:	JSR	MIN
EE92 BD E6B0 2038:	JSR	ONEP
EE95 BD E6D9 2039:	JSR	ALLOT
EE98 BD E414 2040:	JSR	DUP
EE9B BD E044 2041:	JSR	CLITER
EE9E A0 2042:	FCB	\$AO
EE9F BD E43A 2043:	JSR	TOGGLE
EEA2 BD E6CA 2044:	JSR	HERE
EEA5 BD E52C 2045:	JSR	ONE
EEA8 BD E707 2046:	JSR	SUB
EEAB BD E044 2047:	JSR	CLITER
EEAE 80 2048:	FCB	\$80
EEAF BD E43A 2049:	JSR	TOGGLE
EEB2 BD E7E0 2050:	JSR	LATEST
EEB5 BD E6E4 2051:	JSR	COMMA
EEB8 BD E648 2052:	JSR	CURENT
EEBB BD E44E 2053:	JSR	AT
EEBE BD E46E 2054:	JSR	STORE
EEC1 39 2055:	RTS	
EEC1 39 2056: *		
EEC2 C9 2057:	FCB	\$C9
EEC3 5B 2058:	FCC	"[COMPILE"
EEC4 43 4F		
EEC6 4D 50		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 39

EEC8 49 4C
EECA 45
EECB DD 2059: FCB \$DD
EECC EE 50 2060: FDB CREATE-9
EECE BD ED95 2061: BCOMP JSR DFIND
EED1 BD E37B 2062: JSR ZEQU
EED4 BD E523 2063: JSR ZERO
EED7 BD E83A 2064: JSR QERR
EEDA BD E3F7 2065: JSR DROP
EEDD BD E044 2066: JSR CLITER
EEE0 BD 2067: FCB \$BD
EEE1 BD E6F6 2068: JSR CCOMM
EEE4 BD E6E4 2069: JSR COMMA
EEE7 39 2070: RTS
2071: *
EEE8 C7 2072: FCB \$C7
EEE9 4C 2073: FCC "LITERA"
EEEA 49 54
EEEC 45 52
EEEE 41
EEEF CC 2074: FCB \$CC
EEFO EE C2 2075: FDB BCOMP-12
EEF2 BD E655 2076: LITER JSR STATE
EEF5 BD E44E 2077: JSR AT
EEF8 BD E06E 2078: JSR ZBRAN
EEFB 27 09 2079: BEQ LITER2
EEFD BD E8CF 2080: JSR COMPIL
EF00 BD E02C 2081: JSR LIT
EF03 BD E6E4 2082: JSR COMMA
EF06 39 2083: LITER2 RTS
2084: *
EF07 C8 2085: FCB \$C8
EF08 44 2086: FCC "DLITERA"
EF09 4C 49
EF0B 54 45
EF0D 52 41
EF0F CC 2087: FCB \$CC
EF10 EE E8 2088: FDB LITER-10
EF12 BD E655 2089: DLITER JSR STATE
EF15 BD E44E 2090: JSR AT
EF18 BD E06E 2091: JSR ZBRAN
EF1B 27 09 2092: BEQ DLITE2
EF1D BD E401 2093: JSR SWAP
EF20 BD EEF2 2094: JSR LITER
EF23 BD EEF2 2095: JSR LITER
EF26 39 2096: DLITE2 RTS
2097: *
EF27 89 2098: FCB \$89
EF28 49 2099: FCC "INTERPRE"
EF29 4E 54
EF2B 45 52
EF2D 50 52
EF2F 45
EF30 D4 2100: FCB \$D4
EF31 EF 07 2101: FDB DLITER-11
EF33 BD ED95 2102: INTERP JSR DFIND
EF36 BD E06E 2103: JSR ZBRAN
EF39 27 1F 2104: BEQ INTERS
EF3B BD E655 2105: JSR STATE
EF3E BD E44E 2106: JSR AT

FORTH

SSB MNEMONIC ASSEMBLER PAGE 40

EF41 BD E71D 2107:	JSR	LESS
EF44 BD E06E 2108:	JSR	ZBRAN
EF47 27 0C 2109:	BEQ	INTER3
EF49 BD E044 2110:	JSR	CLITER
EF4C BD 2111:	FCB	\$BD
EF4D BD E6F6 2112:	JSR	CCOMM
EF50 BD E6E4 2113:	JSR	COMMA
EF53 20 24 2114:	BRA	INTER7
EF55 BD E05D 2115:	INTER3	JSR EXEC
EF58 20 1F 2116:	INTER4	BRA INTER7
EF5A BD E6CA 2117:	INTER5	JSR HERE
EF5D BD ED25 2118:	JSR	NUMB
EF60 BD E66C 2119:	JSR	DPL
EF63 BD E44E 2120:	JSR	AT
EF66 BD E6B0 2121:	JSR	ONEP
EF69 BD E06E 2122:	JSR	ZBRAN
EF6C 27 05 2123:	BEQ	INTER6
EF6E BD EF12 2124:	JSR	DLITER
EF71 20 06 2125:	BRA	INTER7
EF73 BD E3F7 2126:	INTER6	JSR DROP
EF76 BD EEF2 2127:	JSR	LITER
EF79 BD EA8E 2128:	INTER7	JSR QSTACK
EF7C 20 B5 2129:	BRA	INTERP
EF7E 39 2130:	RTS	
	2131: *	
EF7F 89 2132:	FCB	\$89
EF80 49 2133:	FCC	"IMMEDIAT"
EF81 4D 4D		
EF83 45 44		
EF85 49 41		
EF87 54		
EF88 C5 2134:	FCB	\$C5
EF89 EF 27 2135:	FDB	INTERP-12
EF8B BD E7E0 2136:	IMMED	JSR LATEST
EF8E BD E044 2137:	JSR	CLITER
EF91 40 2138:	FCB	\$40
EF92 BD E43A 2139:	JSR	TOGGLE
EF95 39 2140:	RTS	
	2141: *	
EF96 8A 2142:	FCB	\$8A
EF97 56 2143:	FCC	"VOCABULAR"
EF98 4F 43		
EF9A 41 42		
EF9C 55 4C		
EF9E 41 52		
EFA0 D9 2144:	FCB	\$D9
EFA1 EF 7F 2145:	FDB	IMMED-12
EFA3 BD E98E 2146:	VOCAB	JSR BUILDS
EFA6 BD E02C 2147:	JSR	LIT
EFA9 81 A0 2148:	FDB	\$81AO
EFAB BD E6E4 2149:	JSR	COMMA
EFAE BD E648 2150:	JSR	CURENT
EFB1 BD E44E 2151:	JSR	AT
EFB4 BD E535 2152:	JSR	TWO
EFB7 BD E707 2153:	JSR	SUB
EFBA BD E6E4 2154:	JSR	COMMA
EFBD BD E6CA 2155:	JSR	HERE
EFC0 BD E5F1 2156:	JSR	VOCLIN
EFC3 BD E44E 2157:	JSR	AT
EFC6 BD E6E4 2158:	JSR	COMMA

FORTH

SSB MNEMONIC ASSEMBLER PAGE 41

EFC9 BD E5F1 2159:	JSR	• VOCLIN
EFCC BD E46E 2160:	JSR	STORE
EFCF BD E9A3 2161:	JSR	DOES
EFD2 BD E68C 2162: DOVOC	JSR	TWOP
EFD5 BD E639 2163:	JSR	CONTXT
EFD8 BD E46E 2164:	JSR	STORE
EFDB 39 2165:	RTS	
2166: *		
EFDC 8B 2167:	FCB	\$8B
EFDD 44 2168:	FCC	"DEFINITION"
EFDE 45 46		
EFE0 49 4E		
EFE2 49 54		
EFE4 49 4F		
EFE6 4E		
EFE7 D3 2169:	FCB	\$D3
EFE8 EF 96 2170:	FDB	VOCAB-13
EFEA BD E639 2171: DEFIN	JSR	CONTXT
EFEF BD E44E 2172:	JSR	AT
EFF0 BD E648 2173:	JSR	CURENT
EFF3 BD E46E 2174:	JSR	STORE
EFF6 39 2175:	RTS	
2176: *		
EFF7 C1 2177:	FCB	\$C1
EFF8 A8 2178:	FCB	\$A8
EFF9 EF DC 2179:	FDB	DEFIN-14
EFFB BD E044 2180: PAREN	JSR	CLITER
EFFE 29 2181:	FCC	")"
EFFF BD EC5C 2182:	JSR	WORD
F002 39 2183:	RTS	
2184: *		
F003 84 2185:	FCB	\$84
F004 51 2186:	FCC	"QUI"
F005 55 49		
F007 D4 2187:	FCB	\$D4
F008 EF F7 2188:	FDB	PAREN-4
F00A BD E523 2189: QUIT	JSR	ZERO
F00D BD E5FC 2190:	JSR	BLK
F010 BD E46E 2191:	JSR	STORE
F013 BD E8F5 2192:	JSR	LBRAK
F016 BD E31D 2193: QUIT2	JSR	RPSTOR
F019 BD E21D 2194:	JSR	CR
F01C BD EB8B 2195:	JSR	QUERY
F01F BD EF33 2196:	JSR	INTERP
F022 BD E655 2197:	JSR	STATE
F025 BD E44E 2198:	JSR	AT
F028 BD E37B 2199:	JSR	ZEQU
F02B BD E06E 2200:	JSR	ZBRAN
F02E 27 E6 2201:	BEQ	QUIT2
F030 BD E535 2202:	JSR	TWO
F033 BD E45E 2203:	JSR	CAT
F036 BD E044 2204:	JSR	CLITER
F039 BF 2205:	FCB	\$BF
F03A BD E2D5 2206:	JSR	AND
F03D BD E535 2207:	JSR	TWO
F040 BD E482 2208:	JSR	CSTORE
F043 BD EA64 2209:	JSR	PDOTQ
F046 03 2210:	FCB	3
F047 20 2211:	FCC	" OK"
F048 4F 4B		

FORTH SSB MNEMONIC ASSEMBLER PAGE 42

F04A 20 CA	2212:	QUIT3	BRA	QUIT2
F04C 39	2213:		RTS	
	2214:	*		
F04D 85	2215:		FCB	\$85
F04E 41	2216:		FCC	"ABOR"
F04F 42 4F				
F051 52				
F052 D4	2217:		FCB	\$D4
F053 F0 03	2218:		FDB	QUIT-7
F055 BD E312	2219:	ABORT	JSR	SPSTOR
F058 BD E93D	2220:		JSR	DEC
F05B BD EA8E	2221:		JSR	QSTACK
F05E BD F28F	2222:		JSR	DRZERO
F061 BD E21D	2223:		JSR	CR
F064 BD EA64	2224:		JSR	PDOTQ
F067 08	2225:		FCB	8
F068 46	2226:		FCC	"Forth-84"
F069 6F 72				
F06B 74 68				
F06D 2D 38				
F06F 34				
F070 BD 2008	2227:		JSR	FORTH
F073 BD EFEA	2228:		JSR	DEFIN
F076 BD F00A	2229:		JSR	QUIT
F079 39	2230:		RTS	
	2231:	*		
F07A 84	2232:		FCB	\$84
F07B 43	2233:		FCC	"COL"
F07C 4F 4C				
F07E C4	2234:		FCB	\$C4
F07F F0 4D	2235:		FDB	ABORT-8
F081 8E 2034	2236:	COLD	EQU	*
F081 8E 2034	2237:	CENT	LDS	#REND-1
F084 CE F133	2238:		LDX	#ERAM
F087 09	2239:	COLD2	DEX	
F088 A6 00	2240:		LDA	A 0,X
F08A 36	2241:		PSH	A
F08B 8C F0FE	2242:		CPX	#RFORTH-8
F08E 26 F7	2243:		BNE	COLD2
F090 8E 00DE	2244:		LDS	#N-2
F093 CE F0FE	2245:		LDX	#JMPTAB+15
F096 09	2246:	COLD3	DEX	
F097 A6 00	2247:		LDA	A 0,X
F099 36	2248:		PSH	A
F09A 8C F0EF	2249:		CPX	#JMPTAB
F09D 26 F7	2250:		BNE	COLD3
F09F 8E 400F	2251:		LDS	#XFENCE-1
F0A2 FE E022	2252:		LDX	COLINT
F0A5 FF 4034	2253:		STX	XCOLUMN
F0A8 FE E024	2254:		LDX	DELINT
F0AB FF 4032	2255:		STX	XDELAY
F0AE FE E020	2256:		LDX	VOCINT
F0B1 FF 4014	2257:		STX	XVOCL
F0B4 FE E01E	2258:		LDX	DPINIT
F0B7 FF 4012	2259:		STX	XDF
F0BA FE E01C	2260:		LDX	FENCIN
F0BD FF 4010	2261:		STX	XFENCE
F0C0 CE DDE0	2262:		LDX	#\$DDE0
F0C3 FF 4040	2263:		STX	XUSE
F0C6 FF 4042	2264:		STX	XPREV

FORTH

SSB MNEMONIC ASSEMBLER PAGE 43

F0C9 8E 400F	2265:	WENT	LDS	#XFENCE-1
F0CC CE E01C	2266:		LDX	#FENCIN
F0CF 09	2267:	WARM2	DEX	
F0D0 A6 00	2268:		LDA A	0,X
F0D2 36	2269:		PSH A	
F0D3 8C E012	2270:		CPX	#\$INIT
F0D6 26 F7	2271:		BNE	. WARM2
F0D8 BE E014	2272:		LDS	RINIT
F0DB FE E010	2273:		LDX	UPINIT
F0DE DF F2	2274:		STX	UP
F0E0 CE F055	2275:		LDX	#ABORT
F0E3 3C	2276:		FCB	\$3C PSHX
F0E4 86 00	2277:		LDA A	#0
F0E6 97 02	2278:		STA A	02
F0E8 86 40	2279:		LDA A	#\$40
F0EA 97 00	2280:		STA A	00
F0EC 7E E31D	2281:		JMP	RPSTOR
F0EF 7E FF95	2282:	JMPTAB	JMP	TRAP
F0F2 7E FF95	2283:		JMP	TRAP
F0F5 7E FF95	2284:		JMP	TRAP
F0F8 7E FF95	2285:		JMP	TRAP
F0FB 7E FF95	2286:		JMP	TRAP
	2287:	*		
F0FE C5	2288:		FCB	\$C5
F0FF 46	2289:		FCC	"FORT"
F100 4F 52				
F102 54				
F103 C8	2290:		FCB	\$C8
F104 FD D0	2291:		FDB	NOOF-7
F106 BD E9C5	2292:	RFORTH	JSR	DODOES
F109 7E EFD2	2293:		JMP	DOVOC
F10C 81 A0	2294:		FDB	\$81A0
F10E 20 2D	2295:		FDB	TASK-7
F110 00 00	2296:		FDB	0
F112 54	2297:		FCC	"Turbo-Forth for 6303 1984"
F113 75 72				
F115 62 6F				
F117 2D 46				
F119 6F 72				
F11B 74 68				
F11D 20 66				
F11F 6F 72				
F121 20 36				
F123 33 30				
F125 33 20				
F127 31 39				
F129 38 34				
F12B 84	2298:		FCB	\$84
F12C 54	2299:		FCC	"TAS"
F12D 41 53				
F12F CB	2300:		FCB	\$CB
F130 20 00	2301:		FDB	FORTH-8
F132 39	2302:	RTASK	RTS	
F133 43	2303:	ERAM	FCC	"Chris Flewellen"
F134 68 72				
F136 69 73				
F138 20 46				
F13A 6C 65				
F13C 77 65				
F13E 6C 6C				

FORTH

SSB MNEMONIC ASSEMBLER PAGE 44

F140 65 6E			
F142 84	2304:	FCB	\$84
F143 53	2305:	FCC	"S->"
F144 2D 3E			
F146 C4	2306:	FCB	\$C4
F147 F0 7A	2307:	FDB	COLD-7
F149 BD E414	2308: STOD	JSR	DUP
F14C BD E38B	2309:	JSR	ZLESS
F14F BD E3C2	2310:	JSR	MINUS
F152 39	2311:	RTS	
	2312: *		
F153 81	2313:	FCB	\$81
F154 AA	2314:	FCB	\$AA
F155 F1 42	2315:	FDB	STOD-7
F157 BD E262	2316: STAR	JSR	USTAR
F15A 08	2317:	INX	
F15B 08	2318:	INX	
F15C 39	2319:	RTS	
	2320: *		
F15D 84	2321:	FCB	\$84
F15E 2F	2322:	FCC	"/MO"
F15F 4D 4F			
F161 C4	2323:	FCB	\$C4
F162 F1 53	2324:	FDB	STAR-4
F164 BD E345	2325: SLMOD	JSR	TOR
F167 BD F149	2326:	JSR	STOD
F16A BD E358	2327:	JSR	FROMR
F16D BD F9BC	2328:	JSR	MSLASH
F170 39	2329:	RTS	
	2330: *		
F171 81	2331:	FCB	\$81
F172 AF	2332:	FCB	\$AF
F173 F1 5D	2333:	FDB	SLMOD-7
F175 BD F164	2334: SLASH	JSR	SLMOD
F178 BD E401	2335:	JSR	SWAP
F17B BD E3F7	2336:	JSR	DROP
F17E 39	2337:	RTS	
	2338: *		
F17F 83	2339:	FCB	\$83
F180 4D	2340:	FCC	"MO"
F181 4F			
F182 C4	2341:	FCB	\$C4
F183 F1 71	2342:	FDB	SLASH-4
F185 BD F164	2343: MOD	JSR	SLMOD
F188 BD E3F7	2344:	JSR	DROP
F18B 39	2345:	RTS	
	2346: *		
F18C 85	2347:	FCB	\$85
F18D 2A	2348:	FCC	"*/MO"
F18E 2F 4D			
F190 4F			
F191 C4	2349:	FCB	\$C4
F192 F1 7F	2350:	FDB	MOD-6
F194 BD E345	2351: SSMOD	JSR	TOR
F197 BD F998	2352:	JSR	MSTAR
F19A BD E358	2353:	JSR	FROMR
F19D BD F9BC	2354:	JSR	MSLASH
F1A0 39	2355:	RTS	
	2356: *		
F1A1 82	2357:	FCB	\$82

FORTH

SSB MNEMONIC ASSEMBLER PAGE 45

F1A2 2A	2358:	FCB	"*"
F1A3 AF	2359:	FCB	\$AF
F1A4 F1 8C	2360:	FDB	SSMOD-8
F1A6 BD F194	2361: SSLASH	JSR	SSMOD
F1A9 BD E401	2362:	JSR	SWAP
F1AC BD E3F7	2363:	JSR	DROP
F1AF 39	2364:	RTS	
	2365: *		
F1B0 85	2366:	FCB	\$85
F1B1 4D	2367:	FCC	"M/MO"
F1B2 2F 4D			
F1B4 4F			
F1B5 C4	2368:	FCB	\$C4
F1B6 F1 A1	2369:	FDB	SSLASH-5
F1B8 BD E345	2370: MSMOD	JSR	TOR
F1BB BD E523	2371:	JSR	ZERO
F1BE BD E36A	2372:	JSR	R
F1C1 BD E29E	2373:	JSR	USLASH
F1C4 BD E358	2374:	JSR	FROMR
F1C7 BD E401	2375:	JSR	SWAP
F1CA BD E345	2376:	JSR	TOR
F1CD BD E29E	2377:	JSR	USLASH
F1DO BD E358	2378:	JSR	FROMR
F1D3 39	2379:	RTS	
	2380: *		
F1D4 83	2381:	FCB	\$83
F1D5 41	2382:	FCC	"AB"
F1D6 42			
F1D7 D3	2383:	FCB	\$D3
F1D8 F1 BO	2384:	FDB	MSMOD-8
F1DA BD E414	2385: ABS	JSR	DUP
F1DD BD E38B	2386:	JSR	ZLESS
F1EO BD E06E	2387:	JSR	ZBRAN
F1E3 27 03	2388:	BEQ	ABS2
F1E5 BD E3C2	2389:	JSR	MINUS
F1E8 39	2390: ABS2	RTS	
	2391: *		
F1E9 84	2392:	FCB	\$84
F1EA 44	2393:	FCC	"DAB"
F1EB 41 42			
F1ED D3	2394:	FCB	\$D3
F1EE F1 D4	2395:	FDB	ABS-6
F1FO BD E414	2396: DABS	JSR	DUP
F1F3 BD E38B	2397:	JSR	ZLESS
F1F6 BD E06E	2398:	JSR	ZBRAN
F1F9 27 03	2399:	BEQ	DABS2
F1FB BD E3D2	2400:	JSR	DMINUS
F1FE 39	2401: DABS2	RTS	
	2402: *		
F1FF 83	2403:	FCB	\$83
F200 55	2404:	FCC	"US"
F201 53			
F202 C5	2405:	FCB	\$C5
F203 F1 E9	2406:	FDB	DABS-7
F205 BD E4E0	2407: USE	JSR	DOCON
F208 40 40	2408:	FDB	XUSE
	2409: *		
F20A 84	2410:	FCB	\$84
F20B 50	2411:	FCC	"PRE"
F20C 52 45			

FORTH

SSB MNEMONIC ASSEMBLER PAGE 46

F20E D6	2412:	FCB	\$D6
F20F F1 FF	2413:	FDB	USE-6
F211 BD E4EO	2414: PREV	JSR	DOCON
F214 40 42	2415:	FDB	XPREV
	2416: *		
F216 84	2417:	FCB	\$84
F217 2B	2418:	FCC	"+BU"
F218 42 55			
F21A C6	2419:	FCB	\$C6
F21B F2 0A	2420:	FDB	PREV-7
F21D BD E044	2421: PBUF	JSR	CLITER
F220 44	2422:	FCB	\$44
F221 BD E399	2423:	JSR	PLUS
F224 BD E414	2424:	JSR	DUP
F227 BD E562	2425:	JSR	LIMIT
F22A BD E712	2426:	JSR	EQUAL
F22D BD E06E	2427:	JSR	ZBRAN
F230 27 06	2428:	BEQ	PBUF2
F232 BD E3F7	2429:	JSR	DROP
F235 BD E555	2430:	JSR	FIRST
F238 BD E414	2431: PBUF2	JSR	DUP
F23B BD F211	2432:	JSR	PREV
F23E BD E44E	2433:	JSR	AT
F241 BD E707	2434:	JSR	SUB
F244 39	2435:	RTS	
	2436: *		
F245 86	2437:	FCB	\$86
F246 55	2438:	FCC	"UPDAT"
F247 50 44			
F249 41 54			
F24B C5	2439:	FCB	\$C5
F24C F2 16	2440:	FDB	PBUF-7
F24E BD F211	2441: UPDATE	JSR	PREV
F251 BD E44E	2442:	JSR	AT
F254 BD E44E	2443:	JSR	AT
F257 BD E02C	2444:	JSR	LIT
F25A 80 00	2445:	FDB	\$8000
F25C BD E2E5	2446:	JSR	OR
F25F BD F211	2447:	JSR	PREV
F262 BD E44E	2448:	JSR	AT
F265 BD E46E	2449:	JSR	STORE
F268 39	2450:	RTS	
	2451: *		
F269 BD	2452:	FCB	\$BD
F26A 45	2453:	FCC	"EMPTY-BUFFER"
F26B 4D 50			
F26D 54 59			
F26F 2D 42			
F271 55 46			
F273 46 45			
F275 52			
F276 D3	2454:	FCB	\$D3
F277 F2 45	2455:	FDB	UPDATE-9
F279 BD E555	2456: MTBUF	JSR	FIRST
F27C BD E562	2457:	JSR	LIMIT
F27F BD E3E9	2458:	JSR	OVER
F282 BD E707	2459:	JSR	SUB
F285 BD EC11	2460:	JSR	ERASE
F288 39	2461:	RTS	
	2462: *		

FORTH		SSB MNEMONIC ASSEMBLER PAGE 47
F289 83	2463:	FCB \$83
F28A 44	2464:	FCC "DR"
F28B 52		
F28C B0	2465:	FCB \$B0
F28D F2 69	2466:	FDB MTBUF-16
F28F BD E523	2467: DRZERO	JSR ZERO
F292 BD E62A	2468:	JSR OFSET
F295 BD E46E	2469:	JSR STORE
F298 39	2470:	RTS
	2471: *	
F299 83	2472:	FCB \$83
F29A 44	2473:	FCC "DR"
F29B 52		
F29C B1	2474:	FCB \$B1
F29D F2 89	2475:	FDB DRZERO-6
F29F BD E02C	2476: DRONE	JSR LIT
F2A2 07 DO	2477:	FDB \$7DO
F2A4 BD E62A	2478:	JSR OFSET
F2A7 BD E46E	2479:	JSR STORE
F2AA 39	2480:	RTS
	2481: *	
F2AB 86	2482:	FCB \$86
F2AC 42	2483:	FCC "BUFFE"
F2AD 55 46		
F2AF 46 45		
F2B1 D2	2484:	FCB \$D2
F2B2 F2 99	2485:	FDB DRONE-6
F2B4 BD F205	2486: BUFFER	JSR USE
F2B7 BD E44E	2487:	JSR AT
F2BA BD E414	2488:	JSR DUP
F2BD BD E345	2489:	JSR TOR
F2C0 BD F21D	2490: BUFFR2	JSR PBUF
F2C3 BD E06E	2491:	JSR ZBRAN
F2C6 27 F8	2492:	BEQ BUFFR2
F2C8 BD F205	2493:	JSR USE
F2CB BD E46E	2494:	JSR STORE
F2CE BD E36A	2495:	JSR R
F2D1 BD E44E	2496:	JSR AT
F2D4 BD E38B	2497:	JSR ZLESS
F2D7 BD E06E	2498:	JSR ZBRAN
F2DA 27 1A	2499:	BEQ BUFFR3
F2DC BD E36A	2500:	JSR R
F2DF BD E6BC	2501:	JSR TWOP
F2E2 BD E36A	2502:	JSR R
F2E5 BD E44E	2503:	JSR AT
F2E8 BD E02C	2504:	JSR LIT
F2EB 7F FF	2505:	FDB \$FFFF
F2ED BD E2D5	2506:	JSR AND
F2F0 BD E523	2507:	JSR ZERO
F2F3 BD F4FA	2508:	JSR RW
F2F6 BD E36A	2509: BUFFR3	JSR R
F2F9 BD E46E	2510:	JSR STORE
F2FC BD E36A	2511:	JSR R
F2FF BD F211	2512:	JSR PREV
F302 BD E46E	2513:	JSR STORE
F305 BD E358	2514:	JSR FROMR
F308 BD E6BC	2515:	JSR TWOP
F30B 39	2516:	RTS
	2517: *	
F30C 85	2518:	FCB \$85

FORTH

SSB MNEMONIC ASSEMBLER PAGE 48

F30D 42	2519:	FCB	"BLOC"
F30E 4C 4F			
F310 43			
F311 CB	2520:	FCB	\$CB
F312 F2 AB	2521:	FDB	BUFFER-9
F314 BD E62A	2522: BLOCK	JSR	OFFSET
F317 BD E44E	2523:	JSR	AT
F31A BD E399	2524:	JSR	PLUS
F31D BD E345	2525:	JSR	TOR
F320 BD F211	2526:	JSR	PREV
F323 BD E44E	2527:	JSR	AT
F326 BD E414	2528:	JSR	DUP
F329 BD E44E	2529:	JSR	AT
F32C BD E36A	2530:	JSR	R
F32F BD E707	2531:	JSR	SUB
F332 BD E414	2532:	JSR	DUP
F335 BD E399	2533:	JSR	PLUS
F338 BD E06E	2534:	JSR	ZBRAN
F33B 27 49	2535:	BEQ	BLOCK5
F33D BD F21D	2536: BLOCK3	JSR	PBUF
F340 BD E37B	2537:	JSR	ZEQU
F343 BD E06E	2538:	JSR	ZBRAN
F346 27 1B	2539:	BEQ	BLOCK4
F348 BD E3F7	2540:	JSR	DROP
F34B BD E36A	2541:	JSR	R
F34E BD F2B4	2542:	JSR	BUFFER
F351 BD E414	2543:	JSR	DUP
F354 BD E36A	2544:	JSR	R
F357 BD E52C	2545:	JSR	ONE
F35A BD F4FA	2546:	JSR	RW
F35D BD E535	2547:	JSR	TWO
F360 BD E707	2548:	JSR	SUB
F363 BD E414	2549: BLOCK4	JSR	DUP
F366 BD E44E	2550:	JSR	AT
F369 BD E36A	2551:	JSR	R
F36C BD E707	2552:	JSR	SUB
F36F BD E414	2553:	JSR	DUP
F372 BD E399	2554:	JSR	PLUS
F375 BD E37B	2555:	JSR	ZEQU
F378 BD E06E	2556:	JSR	ZBRAN
F37B 27 C0	2557:	BEQ	BLOCK3
F37D BD E414	2558:	JSR	DUP
F380 BD F211	2559:	JSR	PREV
F383 BD E46E	2560:	JSR	STORE
F386 BD E358	2561: BLOCK5	JSR	FROMR
F389 BD E3F7	2562:	JSR	DROP
F38C BD E6BC	2563:	JSR	TWOF
F38F 39	2564:	RTS	
	2565: *		
F390 86	2566:	FCB	\$86
F391 28	2567:	FCB	"(LINE"
F392 4C 49			
F394 4E 45			
F396 A9	2568:	FCB	\$A9
F397 F3 0C	2569:	FDB	BLOCK-8
F399 BD E345	2570: PLINE	JSR	TOR
F39C BD E044	2571:	JSR	CLITER
F39F 40	2572:	FCB	\$40
F3A0 BD E56F	2573:	JSR	BBUF
F3A3 BD F194	2574:	JSR	SSMOD

FORTH

SSB MNEMONIC ASSEMBLER PAGE 49

F3A6 BD E358 2575: JSR FROMR
F3A9 BD E57C 2576: JSR BSCR
F3AC BD F157 2577: JSR STAR
F3AF BD E399 2578: JSR PLUS
F3B2 BD F314 2579: JSR BLOCK
F3B5 BD E399 2580: JSR PLUS
F3B8 BD E044 2581: JSR CLITER
F3BB 40 2582: FCB \$40
F3BC 39 2583: RTS
2584: *
F3BD 85 2585: FCB \$85
F3BE 2E 2586: FCC ".LIN"
F3BF 4C 49
F3C1 4E
F3C2 C5 2587: FCB \$C5
F3C3 F3 90 2588: FDB PLINE-9
F3C5 BD F399 2589: DLINE JSR PLINE
F3C8 BD EA26 2590: JSR DTRAIL
F3CB BD E9EB 2591: JSR TYPE
F3CE 39 2592: RTS
2593: *
F3CF 87 2594: FCB \$87
F3D0 4D 2595: FCC "MESSAG"
F3D1 45 53
F3D3 53 41
F3D5 47
F3D6 C5 2596: FCB \$C5
F3D7 F3 BD 2597: FDB DLINE-8
F3D9 BD E5CA 2598: MESS JSR WARN
F3DC BD E44E 2599: JSR AT
F3DF BD E06E 2600: JSR ZBRAN
F3E2 27 20 2601: BEQ MESS3
F3E4 BD E79E 2602: JSR DDUP
F3E7 BD E06E 2603: JSR ZBRAN
F3EA 27 25 2604: BEQ MESS4
F3EC BD E044 2605: JSR CLITER
F3EF 04 2606: FCB 4
F3F0 BD E62A 2607: JSR OFSET
F3F3 BD E44E 2608: JSR AT
F3F6 BD E57C 2609: JSR BSCR
F3F9 BD F175 2610: JSR SLASH
F3FC BD E707 2611: JSR SUB
F3FF BD F3C5 2612: JSR DLINE
F402 20 0D 2613: MESS2 BRA MESS4
F404 BD EA64 2614: MESS3 JSR PDOTQ
F407 06 2615: FCB 6
F408 65 2616: FCC "err # "
F409 72 72
F40B 20 23
F40D 20
F40E BD F814 2617: JSR DOT
F411 39 2618: MESS4 RTS
2619: *
F412 84 2620: FCB \$84
F413 4C 2621: FCC "LOA"
F414 4F 41
F416 C4 2622: FCB \$C4
F417 F3 CF 2623: FDB MESS-10
F419 BD E5FC 2624: LOAD JSR BLK
F41C BD E44E 2625: JSR AT

FORTH

SSB MNEMONIC ASSEMBLER PAGE 50

F41F BD E345 2626:	JSR	TOR
F422 BD E606 2627:	JSR	IN
F425 BD E44E 2628:	JSR	AT
F428 BD E345 2629:	JSR	TOR
F42B BD E523 2630:	JSR	ZERO
F42E BD E606 2631:	JSR	IN
F431 BD E46E 2632:	JSR	STORE
F434 BD E57C 2633:	JSR	BSCR
F437 BD F157 2634:	JSR	STAR
F43A BD E5FC 2635:	JSR	BLK
F43D BD E46E 2636:	JSR	STORE
F440 BD EF33 2637:	JSR	INTERP
F443 BD E358 2638:	JSR	FROMR
F446 BD E606 2639:	JSR	IN
F449 BD E46E 2640:	JSR	STORE
F44C BD E358 2641:	JSR	FROMR
F44F BD E5FC 2642:	JSR	BLK
F452 BD E46E 2643:	JSR	STORE
F455 39 2644:	RTS	
	2645: *	
F456 C3 2646:	FCB	\$C3
F457 2D 2647:	FCC	"--"
F458 2D		
F459 BE 2648:	FCB	\$BE
F45A F4 12 2649:	FDB	LOAD-7
F45C BD EBB4 2650:	ARROW	QLOAD
F45F BD E523 2651:	JSR	ZERO
F462 BD E606 2652:	JSR	IN
F465 BD E46E 2653:	JSR	STORE
F468 BD E57C 2654:	JSR	BSCR
F46B BD E5FC 2655:	JSR	BLK
F46E BD E44E 2656:	JSR	AT
F471 BD E3E9 2657:	JSR	OVER
F474 BD F185 2658:	JSR	MOD
F477 BD E707 2659:	JSR	SUB
F47A BD E5FC 2660:	JSR	BLK
F47D BD E420 2661:	JSR	PSTORE
F480 39 2662:	RTS	
	2663: *	
F481 D7 E0 2664:	PEMIT	STA B N
F483 DF E1 2665:	STX	N+1
F485 7D 0002 2666:	PEMIT2	TST \$2
F488 2B FB 2667:	BMI	PEMIT2
F48A D6 11 2668:	PEMIT3	LDA B ACIAC
F48C C5 20 2669:	BIT B	#\$20
F48E 27 FA 2670:	BEQ	PEMIT3
F490 97 13 2671:	STA A	ACIAD+1
F492 DE F2 2672:	LDX	UP
F494 E7 36 2673:	STA B	IOSTAT-UORIG,X
F496 D6 E0 2674:	LDA B	N
F498 DE E1 2675:	LDX	N+1
F49A 39 2676:	RTS	
	2677: *	
F49B D7 E0 2678:	PKEY	STA B N
F49D DF E1 2679:	STX	N+1
F49F D6 11 2680:	LDA B	ACIAC
F4A1 59 2681:	RQL B	
F4A2 24 FB 2682:	BCC	PKEY+4
F4A4 96 12 2683:	LDA A	ACIAD
F4A6 84 7F 2684:	AND A	#\$7F

FORTH

SSB MNEMONIC ASSEMBLER PAGE 51

F4A8 DE F2	2685:	LDX UP
F4AA E7 37	2686:	STA B IOSTAT+1-UORIG, X
F4AC D6 EO	2687:	LDA B N
F4AE DE E1	2688:	LDX N+1
F4B0 39	2689:	RTS
	2690: *	
F4B1 96 11	2691: PQTER	LDA A ACIAC
F4B3 84 80	2692:	AND A #\$80
F4B5 27 04	2693:	BEO PQTER2
F4B7 96 12	2694:	LDA A ACIAD
F4B9 86 01	2695:	LDA A #1
F4BB 39	2696: PQTER2	RTS
	2697: *	
F4BC 86 OD	2698: PCR	LDA A #\$D
F4BE 8D C1	2699:	BSR PEMIT
F4C0 86 OA	2700:	LDA A #\$A
F4C2 8D BD	2701:	BSR PEMIT
F4C4 86 00	2702:	LDA A #0
F4C6 DE F2	2703:	LDX UP
F4C8 E6 33	2704:	LDA B XDELAY+1-UORIG, X
F4CA 5A	2705: PCR2	DEC B
F4CB 2B EE	2706:	BMI PQTER2
F4CD 37	2707:	PSH B
F4CE 8D B1	2708:	BSR PEMIT
F4D0 33	2709:	PUL B
F4D1 20 F7	2710:	BRA PCR2
	2711: *	
F4D3 83	2712:	FCB \$83
F4D4 44	2713:	FCC "DR"
F4D5 52		
F4D6 C2	2714:	FCB \$C2
F4D7 F4 56	2715:	FDB ARROW-6
F4D9 BD E4EO	2716: DRB	JSR DOCON
F4DC 00 EO	2717:	FDB \$00EO
	2718: *	
F4DE 85	2719:	FCB \$85
F4DF 44	2720:	FCC "DRIV"
F4E0 52 49		
F4E2 56		
F4E3 C5	2721:	FCB \$C5
F4E4 F4 D3	2722:	FDB DRB-6
F4E6 EC 02	2723: DRIVE	FDB \$EC02 LDD 2, X
F4E8 3C	2724:	FCB \$3C PSHX
F4E9 FE F4DC	2725:	LDX DRB+3
F4EC BD FDD8	2726:	JSR BUBBLE
F4EF 38	2727:	FCB \$38 PULX
F4F0 4F	2728:	CLR A
F4F1 ED 02	2729:	FDB \$ED02 STD 2, X
F4F3 39	2730:	RTS
	2731: *	
F4F4 83	2732:	FCB \$83
F4F5 52	2733:	FCC "R/"
F4F6 2F		
F4F7 D7	2734:	FCB \$D7
F4F8 F4 DE	2735:	FDB DRIVE-8
F4FA BD E745	2736: RW	JSR ROT
F4FD BD F4D9	2737:	JSR DRB
F500 BD E6BC	2738:	JSR TWOP
F503 BD E46E	2739:	JSR STORE
F506 BD E401	2740:	JSR SWAP

FORTH

SSB MNEMONIC ASSEMBLER PAGE 52

F509 BD F4D9 2741:	JSR	DRB
F50C BD E46E 2742:	JSR	STORE
F50F BD E06E 2743:	JSR	ZBRAN
F512 27 05 2744:	BEQ	RW2
F514 BD E52C 2745:	JSR	ONE
F517 20 03 2746:	BRA	RW3
F519 BD E535 2747: RW2	JSR	TWO
F51C BD F4E6 2748: RW3	JSR	DRIVE
F51F BD E79E 2749:	JSR	DDUP
F522 BD E06E 2750:	JSR	ZBRAN
F525 27 19 2751:	BEQ	RW4
F527 BD EA64 2752:	JSR	PDOTQ
F52A 0F 2753:	FCB	15
F52B 42 2754:	FCC	"BUBBLE ERROR # "
F52C 55 42		
F52E 42 4C		
F530 45 20		
F532 45 52		
F534 52 4F		
F536 52 20		
F538 23 20		
F53A BD F814 2755:	JSR	DOT
F53D BD F00A 2756:	JSR	QUIT
F540 39 2757: RW4	RTS	
	2758: *	
F541 C1 2759:	FCB	\$C1
F542 A7 2760:	FCB	\$A7
F543 F4 F4 2761:	FDB	RW-6
F545 BD ED95 2762: TICK	JSR	DFIND
F548 BD E37B 2763:	JSR	ZEOU
F54B BD E523 2764:	JSR	ZERO
F54E BD E83A 2765:	JSR	QERR
F551 BD E3F7 2766:	JSR	DROP
F554 BD EEF2 2767:	JSR	LITER
F557 39 2768:	RTS	
	2769: *	
F558 86 2770:	FCB	\$86
F559 46 2771:	FCC	"FORGE"
F55A 4F 52		
F55C 47 45		
F55E D4 2772:	FCB	\$D4
F55F F5 41 2773:	FDB	TICK-4
F561 BD E648 2774: FORGET	JSR	CURENT
F564 BD E44E 2775:	JSR	AT
F567 BD E639 2776:	JSR	CONTXT
F56A BD E44E 2777:	JSR	AT
F56D BD E707 2778:	JSR	SUB
F570 BD E044 2779:	JSR	CLITER
F573 18 2780:	FCB	\$18
F574 BD E83A 2781:	JSR	QERR
F577 BD F545 2782:	JSR	TICK
F57A BD E414 2783:	JSR	DUP
F57D BD E5D7 2784:	JSR	FENCE
F580 BD E44E 2785:	JSR	AT
F583 BD E71D 2786:	JSR	LESS
F586 BD E044 2787:	JSR	CLITER
F589 15 2788:	FCB	\$15
F58A BD E83A 2789:	JSR	QERR
F58D BD E414 2790:	JSR	DUP
F590 BD E523 2791:	JSR	ZERO

FORTH

SSB MNEMONIC ASSEMBLER PAGE 53

F593 BD E58B 2792:	JSR	PORIG
F596 BD E71D 2793:	JSR	LESS
F599 BD E044 2794:	JSR	CLITER
F59C 15 2795:	FCB	\$15
F59D BD E83A 2796:	JSR	QERR
F5A0 BD E414 2797:	JSR	DUP
F5A3 BD E7FD 2798:	JSR	NFA
F5A6 BD E5E1 2799:	JSR	DP
F5A9 BD E46E 2800:	JSR	STORE
F5AC BD E7F0 2801:	JSR	LFA
F5AF BD E44E 2802:	JSR	AT
F5B2 BD E639 2803:	JSR	CONTXT
F5B5 BD E44E 2804:	JSR	AT
F5B8 BD E46E 2805:	JSR	STORE
F5BB 39 2806:	RTS	
	2807: *	
F5BC 84 2808:	FCB	\$84
F5BD 42 2809:	FCC	"BAC"
F5BE 41 43		
F5C0 CB 2810:	FCB	\$CB
F5C1 F5 58 2811:	FDB	FORGET-9
F5C3 BD E02C 2812: BACK	JSR	LIT
F5C6 26 03 2813:	FDB	\$2603
F5C8 BD E6E4 2814:	JSR	COMMA
F5CB BD E044 2815:	JSR	CLITER
F5CE 7E 2816:	FCB	\$7E
F5CF BD E6F6 2817:	JSR	CCOMM
F5D2 BD E6E4 2818:	JSR	COMMA
F5D5 39 2819:	RTS	
	2820: *	
F5D6 C5 2821:	FCB	\$C5
F5D7 42 2822:	FCC	"BEGI"
F5D8 45 47		
F5DA 49		
F5DB CE 2823:	FCB	\$CE
F5DC F5 BC 2824:	FDB	BACK-7
F5DE BD E853 2825: BEGIN	JSR	QCOMP
F5E1 BD E6CA 2826:	JSR	HERE
F5E4 BD E52C 2827:	JSR	ONE
F5E7 39 2828:	RTS	
	2829: *	
F5E8 C5 2830:	FCB	\$C5
F5E9 45 2831:	FCC	"ENDI"
F5EA 4E 44		
F5EC 49		
F5ED C6 2832:	FCB	\$C6
F5EE F5 D6 2833:	FDB	BEGIN-8
F5F0 BD E853 2834: ENDIF	JSR	QCOMP
F5F3 BD E535 2835:	JSR	TWO
F5F6 BD E883 2836:	JSR	QPAIRS
F5F9 BD E6CA 2837:	JSR	HERE
F5FC BD E401 2838:	JSR	SWAP
F5FF BD E46E 2839:	JSR	STORE
F602 39 2840:	RTS	
	2841: *	
F603 C4 2842:	FCB	\$C4
F604 54 2843:	FCC	"THE"
F605 48 45		
F607 CE 2844:	FCB	\$CE
F608 F5 E8 2845:	FDB	ENDIF-8

FORTH

SSB MNEMONIC ASSEMBLER PAGE 54

F60A BD F5F0	2846:	THEN	JSR	ENDIF
F60D 39	2847:		RTS	
	2848: *			
F60E C2	2849:		FCB	\$C2
F60F 44	2850:		FCC	"D"
F610 CF	2851:		FCB	\$CF
F611 F6 03	2852:		FDB	THEN-7
F613 BD E8CF	2853:	DO	JSR	COMPILE
F616 BD E0C1	2854:		JSR	XDO
F619 BD E6CA	2855:		JSR	HERE
F61C BD E53E	2856:		JSR	THREE
F61F 39	2857:		RTS	
	2858: *			
F620 C4	2859:		FCB	\$C4
F621 4C	2860:		FCC	"L00"
F622 4F 4F				
F624 DO	2861:		FCB	\$DO
F625 F6 0E	2862:		FDB	DO-5
F627 BD E53E	2863:	LOOP	JSR	THREE
F62A BD E883	2864:		JSR	QPAIRS
F62D BD E8CF	2865:		JSR	COMPILE
F630 BD E07C	2866:		JSR	XLOOP
F633 BD F5C3	2867:		JSR	BACK
F636 39	2868:		RTS	
	2869: *			
F637 C5	2870:		FCB	\$C5
F638 28	2871:		FCC	"+L00"
F639 4C 4F				
F63B 4F				
F63C DO	2872:		FCB	\$DO
F63D F6 20	2873:		FDB	LOOP-7
F63F BD E53E	2874:	PLOOP	JSR	THREE
F642 BD E883	2875:		JSR	QPAIRS
F645 BD E8CF	2876:		JSR	COMPILE
F648 BD E08B	2877:		JSR	XPLOOP
F648 BD F5C3	2878:		JSR	BACK
F64E 39	2879:		RTS	
	2880: *			
F64F C5	2881:		FCB	\$C5
F650 55	2882:		FCC	"UNTI"
F651 4E 54				
F653 49				
F654 CC	2883:		FCB	\$CC
F655 F6 37	2884:		FDB	PLOOP-8
F657 BD E52C	2885:	UNTIL	JSR	ONE
F65A BD E883	2886:		JSR	QPAIRS
F65D BD E8CF	2887:		JSR	COMPILE
F660 BD E06E	2888:		JSR	ZBRAN
F663 BD F5C3	2889:		JSR	BACK
F666 39	2890:		RTS	
	2891: *			
F667 C3	2892:		FCB	\$C3
F668 45	2893:		FCC	"EN"
F669 4E				
F66A C4	2894:		FCB	\$C4
F66B F6 4F	2895:		FDB	UNTIL-8
F66D BD F657	2896:	END	JSR	UNTIL
F670 39	2897:		RTS	
	2898: *			
F671 C5	2899:		FCB	\$C5

FORTH

SSB MNEMONIC ASSEMBLER PAGE 55

F672 41	2900:	FCB	"AGAI"
F673 47	41		
F675 49			
F676 CE	2901:	FCB	\$CE
F677 F6	67	2902:	FDB END-6
F679 BD	E52C	2903:	AGAIN JSR ONE
F67C BD	E883	2904:	JSR QPAIRS
F67F BD	E044	2905:	JSR CLITER
F682 7E		2906:	FCB \$7E
F683 BD	E6F6	2907:	JSR CCOMM
F686 BD	E6E4	2908:	JSR COMMA
F689 39		2909:	RTS
		2910:	*
F68A C6		2911:	FCB \$C6
F68B 52		2912:	FCC "REPEA"
F68C 45	50		
F68E 45	41		
F690 D4		2913:	FCB \$D4
F691 F6	71	2914:	FDB AGAIN-8
F693 BD	E345	2915:	REPEAT JSR TOR
F696 BD	E345	2916:	JSR TOR
F699 BD	F679	2917:	JSR AGAIN
F69C BD	E358	2918:	JSR FROMR
F69F BD	E358	2919:	JSR FRÓMR
F6A2 BD	E535	2920:	JSR TWO
F6A5 BD	E707	2921:	JSR SUB
F6A8 BD	F5F0	2922:	JSR ENDIF
F6AB 39		2923:	RTS
		2924:	*
F6AC C2		2925:	FCB \$C2
F6AD 49		2926:	FCC "I"
F6AE C6		2927:	FCB \$C6
F6AF F6	8A	2928:	FDB REPEAT-9
F6B1 BD	EBCF	2929:	IF JSR COMPIL
F6B4 BD	E06E	2930:	JSR ZBRAN
F6B7 BD	E02C	2931:	JSR LIT
F6BA 26	03	2932:	FDB \$2603
F6BC BD	E6E4	2933:	JSR COMMA
F6BF BD	E044	2934:	JSR CLITER
F6C2 7E		2935:	FCB \$7E
F6C3 BD	E6F6	2936:	JSR CCOMM
F6C6 BD	E6CA	2937:	JSR HERE
F6C9 BD	E523	2938:	JSR ZERO
F6C0 BD	E6E4	2939:	JSR COMMA
F6CF BD	E535	2940:	JSR TWO
F6D2 39		2941:	RTS
		2942:	*
F6D3 C4		2943:	FCB \$C4
F6D4 45		2944:	FCC "ELS"
F6D5 4C	53		
F6D7 C5		2945:	FCB \$C5
F6D8 F6	AC	2946:	FDB IF-5
F6DA BD	E535	2947:	ELSE JSR TWO
F6DD BD	E883	2948:	JSR QPAIRS
F6EO BD	E044	2949:	JSR CLITER
F6E3 7E		2950:	FCB \$7E
F6E4 BD	E6F6	2951:	JSR CCOMM
F6E7 BD	E6CA	2952:	JSR HERE
F6EA BD	E523	2953:	JSR ZERO
F6ED BD	E6E4	2954:	JSR COMMA

FORTH

SSB MNEMONIC ASSEMBLER PAGE 56

F6F0 BD E401 2955:	JSR	SWAP
F6F3 BD E535 2956:	JSR	TWO
F6F6 BD F5F0 2957:	JSR	ENDIF
F6F9 BD E535 2958:	JSR	TWO
F6FC 39 2959:	RTS	
	2960: *	
F6FD C5 2961:	FCB	\$C5
F6FE 57 2962:	FCC	"WHIL"
F6FF 48 49		
F701 4C		
F702 C5 2963:	FCB	\$C5
F703 F6 D3 2964:	FDB	ELSE-7
F705 BD F6B1 2965: WHILE	JSR	IF
F708 BD E6BC 2966:	JSR	TWOP
F70B 39 2967:	RTS	
	2968: *	
F70C 86 2969:	FCB	\$86
F70D 53 2970:	FCC	"SPACE"
F70E 50 41		
F710 43 45		
F712 D3 2971:	FCB	\$D3
F713 F6 FD 2972:	FDB	WHILE-8
F715 BD E523 2973: SPACES	JSR	ZERO
F718 BD E782 2974:	JSR	MAX
F71B BD E79E 2975:	JSR	DDUP
F71E BD E06E 2976:	JSR	ZBRAN
F721 27 0E 2977:	BEQ	SPACE3
F723 BD E523 2978:	JSR	ZERO
F726 BD EOC1 2979:	JSR	XDO
F729 BD E75A 2980: SPACE2	JSR	SPACE
F72C BD E07C 2981:	JSR	XLOOP
F72F 27 F8 2982:	BEQ	SPACE2
F731 39 2983: SPACE3	RTS	
	2984: *	
F732 82 2985:	FCB	\$82
F733 3C 2986:	FCC	"<"
F734 A3 2987:	FCB	\$A3
F735 F7 0C 2988:	FDB	SPACES-9
F737 BD EC4A 2989: BDIGS	JSR	PAD
F73A BD E697 2990:	JSR	HLD
F73D BD E46E 2991:	JSR	STORE
F740 39 2992:	RTS	
	2993: *	
F741 82 2994:	FCB	\$82
F742 23 2995:	FCC	"#"
F743 BE 2996:	FCB	\$BE
F744 F7 32 2997:	FDB	BDIGS-5
F746 BD E3F7 2998: EDIGS	JSR	DROP
F749 BD E3F7 2999:	JSR	DROP
F74C BD E697 3000:	JSR	HLD
F74F BD E44E 3001:	JSR	AT
F752 BD EC4A 3002:	JSR	PAD
F755 BD E3E9 3003:	JSR	OVER
F758 BD E707 3004:	JSR	SUB
F75B 39 3005:	RTS	
	3006: *	
F75C 84 3007:	FCB	\$84
F75D 53 3008:	FCC	"SIG"
F75E 49 47		
F760 CE 3009:	FCB	\$CE

FORTH

SSB MNEMONIC ASSEMBLER PAGE 57

F761 F7 41	3010:	FDB	EDIGS-5
F763 BD E745	3011: SIGN	JSR	ROT
F766 BD E38B	3012:	JSR	ZLESS
F769 BD E06E	3013:	JSR	ZBRAN
F76C 27 07	3014:	BEQ	SIGN2
F76E BD E044	3015:	JSR	CLITER
F771 2D	3016:	FCC	"-"
F772 BD EC2F	3017:	JSR	HOLD
F775 39	3018: SIGN2	RTS	
	3019: *		
F776 81	3020:	FCB	\$81
F777 A3	3021:	FCB	\$A3
F778 F7 5C	3022:	FDB	SIGN-7
F77A BD E661	3023: DIG	JSR	BASE
F77D BD E44E	3024:	JSR	AT
F780 BD F1BB	3025:	JSR	MSMOD
F783 BD E745	3026:	JSR	ROT
F786 BD E044	3027:	JSR	CLITER
F789 09	3028:	FCB	9
F78A BD E3E9	3029:	JSR	OVER
F78D BD E71D	3030:	JSR	LESS
F790 BD E06E	3031:	JSR	ZBRAN
F793 27 07	3032:	BEQ	DIG2
F795 BD E044	3033:	JSR	CLITER
F798 07	3034:	FCB	7
F799 BD E399	3035:	JSR	PLUS
F79C BD E044	3036: DIG2	JSR	CLITER
F79F 30	3037:	FCC	"0"
F7A0 BD E399	3038:	JSR	PLUS
F7A3 BD EC2F	3039:	JSR	HOLD
F7A6 39	3040:	RTS	
	3041: *		
F7A7 82	3042:	FCB	\$82
F7A8 23	3043:	FCC	"#"
F7A9 D3	3044:	FCB	\$D3
F7AA F7 76	3045:	FDB	DIG-4
F7AC BD F77A	3046: DIGS	JSR	DIG
F7AF BD E3E9	3047:	JSR	OVER
F7B2 BD E3E9	3048:	JSR	OVER
F7B5 BD E2E5	3049:	JSR	OR
F7B8 BD E37B	3050:	JSR	ZEQU
F7BB BD E06E	3051:	JSR	ZBRAN
F7BE 27 EC	3052:	BEQ	DIGS
F7C0 39	3053:	RTS	
	3054: *		
F7C1 82	3055:	FCB	\$82
F7C2 2E	3056:	FCC	"."
F7C3 D2	3057:	FCB	\$D2
F7C4 F7 A7	3058:	FDB	DIGS-5
F7C6 BD E345	3059: DOTR	JSR	TOR
F7C9 BD F149	3060:	JSR	STOD
F7CC BD E358	3061:	JSR	FROMR
F7CF BD F7D9	3062:	JSR	DDOTR
F7D2 39	3063:	RTS	
	3064: *		
F7D3 83	3065:	FCB	\$83
F7D4 44	3066:	FCC	"D."
F7D5 2E			
F7D6 D2	3067:	FCB	\$D2
F7D7 F7 C1	3068:	FDB	DOTR-5

FORTH

SSB MNEMONIC ASSEMBLER PAGE 58

F7D9 BD E345 3069:	DDOTR	JSR	TOR
F7DC BD E401 3070:		JSR	SWAP
F7DF BD E3E9 3071:		JSR	OVER
F7E2 BD F1F0 3072:		JSR	DABS
F7E5 BD F737 3073:		JSR	BDIGS
F7E8 BD F7AC 3074:		JSR	DIGS
F7EB BD F763 3075:		JSR	SIGN
F7EE BD F746 3076:		JSR	EDIGS
F7F1 BD E358 3077:		JSR	FROMR
F7F4 BD E3E9 3078:		JSR	OVER
F7F7 BD E707 3079:		JSR	SUB
F7FA BD F715 3080:		JSR	SPACES
F7FD BD E9EB 3081:		JSR	TYPE
F800 39	3082:	RTS	
	3083: *		
F801 82	3084:	FCB	\$82
F802 44	3085:	FCC	"D"
F803 AE	3086:	FCB	\$AE
F804 F7 D3	3087:	FDB	DDOTR-6
F806 BD E523	3088: DDOT	JSR	ZERO
F809 BD F7D9	3089:	JSR	DDOTR
F80C BD E75A	3090:	JSR	SPACE
F80F 39	3091:	RTS	
	3092: *		
F810 81	3093:	FCB	\$81
F811 AE	3094:	FCB	\$AE
F812 F8 01	3095:	FDB	DDOT-5
F814 BD F149	3096: DOT	JSR	STOD
F817 BD F806	3097:	JSR	DDOT
F81A 39	3098:	RTS	
	3099: *		
F81B 81	3100:	FCB	\$81
F81C BF	3101:	FCB	\$BF
F81D F8 10	3102:	FDB	DOT-4
F81F BD E44E	3103: QUEST	JSR	AT
F822 BD F814	3104:	JSR	DOT
F825 39	3105:	RTS	
	3106: *		
F826 84	3107:	FCB	\$84
F827 4C	3108:	FCC	"LIS"
F828 49 53			
F82A D4	3109:	FCB	\$D4
F82B F8 1B	3110:	FDB	QUEST-4
F82D BD E93D	3111: LIST	JSR	DEC
F830 BD E21D	3112:	JSR	CR
F833 BD E414	3113:	JSR	DUP
F836 BD E61C	3114:	JSR	SCR
F839 BD E46E	3115:	JSR	STORE
F83C BD EA64	3116:	JSR	PDOTQ
F83F 06	3117:	FCB	6
F840 53	3118:	FCC	"SCR # "
F841 43 52			
F843 20 23			
F845 20			
F846 BD F814	3119:	JSR	DOT
F849 BD E044	3120:	JSR	CLITER
F84C 10	3121:	FCB	\$10
F84D BD E523	3122:	JSR	ZERO
F850 BD EOC1	3123:	JSR	XDO
F853 BD E21D	3124: LIST2	JSR	CR

FORTH

SSB MNEMONIC ASSEMBLER PAGE 59

F856 BD E0DA 3125:	JSR	I
F859 BD E53E 3126:	JSR	THREE
F85C BD F7C6 3127:	JSR	DOTR
F85F BD E75A 3128:	JSR	SPACE
F862 BD E0DA 3129:	JSR	I
F865 BD E61C 3130:	JSR	SCR
F868 BD E44E 3131:	JSR	AT
F86B BD F3C5 3132:	JSR	DLINE
F86E BD E07C 3133:	JSR	XLOOP
F871 27 EO 3134:	BEQ	LIST2
F873 BD E21D 3135:	JSR	CR
F876 39 3136:	RTS	
	3137: *	
F877 85 3138:	FCB	\$85
F878 49 3139:	FCC	"INDE"
F879 4E 44		
F87B 45		
F87C D8 3140:	FCB	\$DB
F87D F8 26 3141:	FDB	LIST-7
F87F BD E21D 3142: INDEX	JSR	CR
F882 BD E6B0 3143:	JSR	ONEP
F885 BD E401 3144:	JSR	SWAP
F888 BD E0C1 3145:	JSR	XDO
F88B BD E21D 3146: INDEX2	JSR	CR
F88E BD E0DA 3147:	JSR	I
F891 BD E53E 3148:	JSR	THREE
F894 BD F7C6 3149:	JSR	DOTR
F897 BD E75A 3150:	JSR	SPACE
F89A BD E523 3151:	JSR	ZERO
F89D BD E0DA 3152:	JSR	I
F8A0 BD F3C5 3153:	JSR	DLINE
F8A3 BD E211 3154:	JSR	QTERM
F8A6 BD E06E 3155:	JSR	ZBRAN
F8A9 27 03 3156:	BEQ	INDEX3
F8AB BD E336 3157:	JSR	LEAVE
F8AE BD E07C 3158: INDEX3	JSR	XLOOP
F8B1 27 D8 3159:	BEQ	INDEX2
F8B3 BD E21D 3160:	JSR	CR
F8B6 39 3161:	RTS	
	3162: *	
F8B7 85 3163:	FCB	\$85
F8B8 54 3164:	FCC	"TRIA"
F8B9 52 49		
F8BB 41		
F8BC C4 3165:	FCB	\$C4
F8BD F8 77 3166:	FDB	INDEX-8
F8BF BD E53E 3167: TRIAD	JSR	THREE
F8C2 BD F175 3168:	JSR	SLASH
F8C5 BD E53E 3169:	JSR	THREE
F8C8 BD F157 3170:	JSR	STAR
F8CB BD E53E 3171:	JSR	THREE
F8CE BD E3E9 3172:	JSR	OVER
F8D1 BD E399 3173:	JSR	PLUS
F8D4 BD E401 3174:	JSR	SWAP
F8D7 BD E0C1 3175:	JSR	XDO
F8DA BD E21D 3176: TRIAD2	JSR	CR
F8DD BD E0DA 3177:	JSR	I
F8E0 BD F82D 3178:	JSR	LIST
F8E3 BD E211 3179:	JSR	QTERM
F8E6 BD E06E 3180:	JSR	ZBRAN

FORTH

SSB MNEMONIC ASSEMBLER PAGE 60

F8E9 27 03	3181:	BEQ	TRIAD3
F8EB BD E336	3182:	JSR	LEAVE
F8EE BD E07C	3183:	TRIAD3	JSR XLOOP
F8F1 27 E7	3184:	BEQ	TRIAD2
F8F3 BD E21D	3185:	JSR	CR
F8F6 BD E044	3186:	JSR	CLITER
F8F9 OF	3187:	FCB	\$OF
F8FA BD F3D9	3188:	JSR	MESS
F8FD BD E21D	3189:	JSR	CR
F900 39	3190:	RTS	
	3191: *		
F901 85	3192:	FCB	\$85
F902 56	3193:	FCC	"VLIS"
F903 4C 49			
F905 53			
F906 D4	3194:	FCB	\$D4
F907 F8 B7	3195:	FDB	TRIAD-8
F909 BD E044	3196:	VLIST	JSR CLITER
F90C 80	3197:	FCB	\$80
F90D BD E611	3198:	JSR	OUT
F910 BD E46E	3199:	JSR	STORE
F913 BD E639	3200:	JSR	CONTXT
F916 BD E44E	3201:	JSR	AT
F919 BD E44E	3202:	JSR	AT
F91C BD E611	3203:	VLIST1	JSR OUT
F91F BD E44E	3204:	JSR	AT
F922 BD E6A6	3205:	JSR	COLUMNS
F925 BD E44E	3206:	JSR	AT
F928 BD E044	3207:	JSR	CLITER
F92B 20	3208:	FCB	32
F92C BD E707	3209:	JSR	SUB
F92F BD E738	3210:	JSR	GREAT
F932 BD E06E	3211:	JSR	ZBRAN
F935 27 0C	3212:	BEQ	VLIST2
F937 BD E21D	3213:	JSR	CR
F93A BD E523	3214:	JSR	ZERO
F93D BD E611	3215:	JSR	OUT
F940 BD E46E	3216:	JSR	STORE
F943 BD E414	3217:	VLIST2	JSR DUP
F946 BD EE16	3218:	JSR	IDDOT
F949 BD E75A	3219:	JSR	SPACE
F94C BD E75A	3220:	JSR	SPACE
F94F BD E813	3221:	JSR	PFA
F952 BD E7F0	3222:	JSR	LFA
F955 BD E44E	3223:	JSR	AT
F958 BD E414	3224:	JSR	DUP
F95B BD E37B	3225:	JSR	ZEOU
F95E BD E211	3226:	JSR	QTERM
F961 BD E2E5	3227:	JSR	OR
F964 BD E06E	3228:	JSR	ZBRAN
F967 27 B3	3229:	BEQ	VLIST1
F969 BD E3F7	3230:	JSR	DROP
F96C BD E21D	3231:	JSR	CR
F96F 39	3232:	RTS	
	3233: *		
F970 B3	3234:	FCB	\$B3
F971 44	3235:	FCC	"D+"
F972 2B			
F973 AD	3236:	FCB	\$AD
F974 F9 01	3237:	FDB	VLIST-8

.FORTH

SSB MNEMONIC ASSEMBLER PAGE 61

F976 BD E38B 3238: DPLMI JSR ZLESS
F979 BD E06E 3239: JSR ZBRAN
F97C 27 03 3240: BEQ DPLMI2
F97E BD E3D2 3241: JSR DMINUS
F981 39 3242: DPLMI2 RTS
3243: *
F982 82 3244: FCB \$82
F983 28 3245: FCC "+"
F984 AD 3246: FCB \$AD
F985 F9 70 3247: FDB DPLMI-6
F987 BD E38B 3248: PLMI JSR ZLESS
F98A BD E06E 3249: JSR ZBRAN
F98D 27 03 3250: BEQ PLMI2
F98F BD E3C2 3251: JSR MINUS
F992 39 3252: PLMI2 RTS
3253: *
F993 82 3254: FCB \$82
F994 4D 3255: FCC "M"
F995 AA 3256: FCB \$AA
F996 F9 82 3257: FDB PLMI-5
F998 BD E3E9 3258: MSTAR JSR OVER
F99B BD E3E9 3259: JSR OVER
F99E BD E2F6 3260: JSR XOR
F9A1 BD E345 3261: JSR TOR
F9A4 BD F1DA 3262: JSR ABS
F9A7 BD E401 3263: JSR SWAP
F9AA BD F1DA 3264: JSR ABS
F9AD BD E262 3265: JSR USTAR
F9B0 BD E358 3266: JSR FROMR
F9B3 BD F976 3267: JSR DPLMI
F9B6 39 3268: RTS
3269: *
F9B7 82 3270: FCB \$82
F9B8 4D 3271: FCC "M"
F9B9 AF 3272: FCB \$AF
F9BA F9 93 3273: FDB MSTAR-5
F9BC BD E3E9 3274: MSLASH JSR OVER
F9BF BD E345 3275: JSR TOR
F9C2 BD E345 3276: JSR TOR
F9C5 BD F1F0 3277: JSR DABS
F9C8 BD E36A 3278: JSR R
F9CB BD F1DA 3279: JSR ABS
F9CE BD E29E 3280: JSR USLASH
F9D1 BD E358 3281: JSR FROMR
F9D4 BD E36A 3282: JSR R
F9D7 BD E2F6 3283: JSR XOR
F9DA BD F987 3284: JSR PLMI
F9DD BD E401 3285: JSR SWAP
F9EO BD E358 3286: JSR FROMR
F9E3 BD F987 3287: JSR PLMI
F9E6 BD E401 3288: JSR SWAP
F9E9 39 3289: RTS
3290: *
F9EA 83 3291: FCB \$83
F9EB 43 3292: FCC "C/"
F9EC 2F
F9ED CC 3293: FCB \$CC
F9EE F9 B7 3294: FDB MSLASH-5
F9FO BD E4E0 3295: CL JSR DOCON
F9F3 00 40 3296: FDB \$40

FORTH

SSB MNEMONIC ASSEMBLER PAGE 62

	3297: *		
F9F5 84	3298: FCB	\$84	
F9F6 54	3299: FCC	"TEX"	
F9F7 45 58			
F9F9 D4	3300: FCB	\$D4	
F9FA F9 EA	3301: FDB	CL-6	
F9FC BD E6CA	3302: TEXT	JSR	HERE
F9FF BD F9FO	3303: JSR	CL	
FA02 BD E6B0	3304: JSR	ONEP	
FA05 BD EC21	3305: JSR	BLANKS	
FA08 BD EC5C	3306: JSR	WORD	
FA0B BD E6CA	3307: JSR	HERE	
FA0E BD EC4A	3308: JSR	PAD	
FA11 BD F9FO	3309: JSR	CL	
FA14 BD E6B0	3310: JSR	ONEP	
FA17 BD E22D	3311: JSR	CMOVE	
FA1A 39	3312: RTS		
	3313: *		
FA1B 84	3314: FCB	\$84	
FA1C 4C	3315: FCC	"LIN"	
FA1D 49 4E			
FA1F C5	3316: FCB	\$C5	
FA20 F9 F5	3317: FDB	TEXT-7	
FA22 BD E414	3318: LINE	JSR	DUP
FA25 BD E02C	3319: JSR	LIT	
FA28 FF FO	3320: FDB	\$FFFF0	
FA2A BD E2D5	3321: JSR	AND	
FA2D BD E044	3322: JSR	CLITER	
FA30 17	3323: FCB	\$17	
FA31 BD E83A	3324: JSR	QERR	
FA34 BD E61C	3325: JSR	SCR	
FA37 BD E44E	3326: JSR	AT	
FA3A BD F399	3327: JSR	PLINE	
FA3D BD E3F7	3328: JSR	DROP	
FA40 39	3329: RTS		
	3330: *		
FA41 C6	3331: FCB	\$C6	
FA42 45	3332: FCC	"EDITO"	
FA43 44 49			
FA45 54 4F			
FA47 D2	3333: FCB	\$D2	
FA48 FA 1B	3334: FDB	LINE-7	
FA4A BD E9C5	3335: EDITOR	JSR	DODOES
FA4D 7E EFD2	3336: JMP	DOVOC	
FA50 81 A0	3337: FDB	\$81AO	
FA52 FD 2C	3338: FDB	C-4	
FA54 20 12	3339: FDB	FORTH+10	
	3340: *		
FA56 85	3341: FCB	\$85	
FA57 57	3342: FCC	"WHER"	
FA58 48 45			
FA5A 52			
FA5B C5	3343: FCB	\$C5	
FA5C FA 41	3344: FDB	EDITOR-9	
FA5E BD E414	3345: WHERE	JSR	DUP
FA61 BD E57C	3346: JSR	BSCR	
FA64 BD F175	3347: JSR	SLASH	
FA67 BD E414	3348: JSR	DUP	
FA6A BD E61C	3349: JSR	SCR	
FA6D BD E46E	3350: JSR	STORE	

FORTH		SSB MNEMONIC ASSEMBLER PAGE 63
FA70 BD EA64 3351:	JSR	PDOTQ
FA73 06 3352:	FCB	6
FA74 53 3353:	FCC	"SCR # "
FA75 43 52		
FA77 20 23		
FA79 20		
FA7A BD E93D 3354:	JSR	DEC
FA7D BD F814 3355:	JSR	DOT
FA80 BD E401 3356:	JSR	SWAP
FA83 BD F9F0 3357:	JSR	CL
FA86 BD F164 3358:	JSR	SLMOD
FA89 BD F9F0 3359:	JSR	CL
FA8C BD F157 3360:	JSR	STAR
FA8F BD E745 3361:	JSR	ROT
FA92 BD F314 3362:	JSR	BLOCK
FA95 BD E399 3363:	JSR	PLUS
FA98 BD E21D 3364:	JSR	CR
FA9B BD F9F0 3365:	JSR	CL
FA9E BD E9EB 3366:	JSR	TYPE
FAA1 BD E21D 3367:	JSR	CR
FAA4 BD E6CA 3368:	JSR	HERE
FAA7 BD E45E 3369:	JSR	CAT
FAAA BD E707 3370:	JSR	SUB
FAAD BD F715 3371:	JSR	SPACES
FAB0 BD E044 3372:	JSR	CLITER
FAB3 5E 3373:	FCB	\$5E
FAB4 BD E1DC 3374:	JSR	EMIT
FAB7 BD FA4A 3375:	JSR	EDITOR
FABA BD F00A 3376:	JSR	QUIT
FABD 39 3377:	RTS	
	3378: *	
FABE 87 3379:	FCB	\$87
FABF 23 3380:	FCC	"#LOCAT"
FAC0 4C 4F		
FAC2 43 41		
FAC4 54		
FAC5 C5 3381:	FCB	\$C5
FAC6 20 2D 3382:	FDB	TASK-7
FAC8 BD E68C 3383: NLOC	JSR	RNUM
FACB BD E44E 3384:	JSR	AT
FACE BD F9F0 3385:	JSR	CL
FAD1 BD F164 3386:	JSR	SLMOD
FAD4 39 3387:	RTS	
	3388: *	
FAD5 85 3389:	FCB	\$85
FAD6 23 3390:	FCC	"#LEA"
FAD7 4C 45		
FAD9 41		
FADA C4 3391:	FCB	\$C4
FADB FA BE 3392:	FDB	NLOC-10
FADD BD FAC8 3393: NLEAD	JSR	NLOC
FAEO BD FA22 3394:	JSR	LINE
FAE3 BD E401 3395:	JSR	SWAP
FAE6 39 3396:	RTS	
	3397: *	
FAE7 84 3398:	FCB	\$84
FAE8 23 3399:	FCC	"#LA"
FAE9 4C 41		
FAEB C7 3400:	FCB	\$C7
FAEC FA D5 3401:	FDB	NLEAD-8

FORTH

SSB MNEMONIC ASSEMBLER PAGE 64

FAEE BD FADD 3402:	NLAG	JSR	NLEAD
FAF1 BD E414 3403:		JSR	DUP
FAF4 BD E345 3404:		JSR	TOR
FAF7 BD E399 3405:		JSR	PLUS
FAFA BD F9FO 3406:		JSR	CL
FAFD BD E358 3407:		JSR	FROMR
FB00 BD E707 3408:		JSR	SUB
FB03 39 3409:		RTS	
	3410: *		
FB04 85 3411:		FCB	\$85
FB05 2D 3412:		FCC	"-MOV"
FB06 4D 4F			
FB08 56			
FB09 C5 3413:		FCB	\$C5
FBOA FA E7 3414:		FDB	NLAG-7
FBOC BD FA22 3415:	MMOVE	JSR	LINE
FB0F BD F9FO 3416:		JSR	CL
FB12 BD E22D 3417:		JSR	CMOVE
FB15 BD F24E 3418:		JSR	UPDATE
FB18 39 3419:		RTS	
	3420: *		
FB19 81 3421:		FCB	\$81
FB1A C8 3422:		FCB	\$C8
FB1B FB 04 3423:		FDB	MMOVE-8
FB1D BD FA22 3424:	H	JSR	LINE
FB20 BD EC4A 3425:		JSR	PAD
FB23 BD E6B0 3426:		JSR	ONEP
FB26 BD F9FO 3427:		JSR	CL
FB29 BD E414 3428:		JSR	DUP
FB2C BD EC4A 3429:		JSR	PAD
FB2F BD E482 3430:		JSR	CSTORE
FB32 BD E22D 3431:		JSR	CMOVE
FB35 39 3432:		RTS	
	3433: *		
FB36 81 3434:		FCB	\$81
FB37 C5 3435:		FCB	\$C5
FB38 FB 19 3436:		FDB	H-4
FB3A BD FA22 3437:	ER	JSR	LINE
FB3D BD F9FO 3438:		JSR	CL
FB40 BD EC21 3439:		JSR	BLANKS
FB43 BD F24E 3440:		JSR	UPDATE
FB46 39 3441:		RTS	
	3442: *		
FB47 81 3443:		FCB	\$81
FB48 D3 3444:		FCB	\$D3
FB49 FB 36 3445:		FDB	ER-4
FB4B BD E414 3446:	S	JSR	DUP
FB4E BD E52C 3447:		JSR	ONE
FB51 BD E707 3448:		JSR	SUB
FB54 BD E044 3449:		JSR	CLITER
FB57 OE 3450:		FCB	\$E
FB58 BD E0C1 3451:		JSR	XDO
FB5B BD E0DA 3452:	S2	JSR	I
FB5E BD FA22 3453:		JSR	LINE
FB61 BD E0DA 3454:		JSR	I
FB64 BD E6B0 3455:		JSR	ONEP
FB67 BD FBOC 3456:		JSR	MMOVE
FB6A BD E02C 3457:		JSR	LIT
FB6D FF FF 3458:		FDB	\$FFFF
FB6F BD E08B 3459:		JSR	XLOOP

FORTH

SSB MNEMONIC ASSEMBLER PAGE 65

FB72 27 E7 3460:	BEQ	S2
FB74 BD FB3A 3461:	JSR	ER
FB77 39 3462:	RTS	
3463: *		
FB78 81 3464:	FCB	\$81
FB79 C4 3465:	FCB	\$C4
FB7A FB 47 3466:	FDB	S-4
FB7C BD E414 3467: DEL	JSR	DUP
FB7F BD FB1D 3468:	JSR	H
FB82 BD E044 3469:	JSR	CLITER
FB85 OF 3470:	FCB	\$F
FB86 BD E414 3471:	JSR	DUP
FB89 BD E745 3472:	JSR	ROT
FB8C BD E0C1 3473:	JSR	XDO
FB8F BD E0DA 3474: DEL2	JSR	I
FB92 BD E680 3475:	JSR	ONEP
FB95 BD FA22 3476:	JSR	LINE
FB98 BD E0DA 3477:	JSR	I
FB9B BD FB0C 3478:	JSR	MMOVE
FB9E BD E07C 3479:	JSR	XLOOP
FBA1 27 EC 3480:	BEQ	DEL2
FBA3 BD FB3A 3481:	JSR	ER
FBA6 39 3482:	RTS	
3483: *		
FBA7 81 3484:	FCB	\$81
FBA8 CD 3485:	FCB	\$CD
FBA9 FB 78 3486:	FDB	DEL-4
FBAB BD E68C 3487: M	JSR	RNUM
FBAE BD E420 3488:	JSR	PSTORE
FBB1 BD E21D 3489:	JSR	CR
FBB4 BD E75A 3490:	JSR	SPACE
FBB7 BD FADD 3491:	JSR	NLEAD
FBB8 BD E9EB 3492:	JSR	TYPE
FBB9 BD E044 3493:	JSR	CLITER
FBC0 5F 3494:	FCB	\$5F
FBC1 BD E1DC 3495:	JSR	EMIT
FBC4 BD FAEE 3496:	JSR	NLAG
FBC7 BD E9EB 3497:	JSR	TYPE
FBCA BD FAC8 3498:	JSR	NLOC
FBCD BD FB14 3499:	JSR	DOT
FBD0 BD E3F7 3500:	JSR	DROP
FBD3 39 3501:	RTS	
3502: *		
FBD4 81 3503:	FCB	\$81
FBD5 D4 3504:	FCB	\$D4
FBD6 FB A7 3505:	FDB	M-4
FBD8 BD E414 3506: T	JSR	DUP
FBDB BD F9F0 3507:	JSR	CL
FBDE BD F157 3508:	JSR	STAR
FBE1 BD E68C 3509:	JSR	RNUM
FBE4 BD E46E 3510:	JSR	STORE
FBE7 BD E414 3511:	JSR	DUP
FBEA BD FB1D 3512:	JSR	H
FBED BD E523 3513:	JSR	ZERO
FBFO BD FBAB 3514:	JSR	M
FBF3 39 3515:	RTS	
3516: *		
FBF4 81 3517:	FCB	\$81
FBF5 CC 3518:	FCB	\$CC
FBF6 FB D4 3519:	FDB	T-4

FORTH

SSB MNEMONIC ASSEMBLER PAGE 66

FBF8 BD E61C	3520:	L	JSR	SCR
FBFB BD E44E	3521:		JSR	AT
FBFE BD F82D	3522:		JSR	LIST
FC01 BD E523	3523:		JSR	ZERO
FC04 BD FBAB	3524:		JSR	M
FC07 39	3525:		RTS	
	3526:	*		
FC08 81	3527:		FCB	\$81
FC09 D2	3528:		FCB	\$D2
FC0A FB F4	3529:		FDB	L-4
FC0C BD EC4A	3530:	REP	JSR	PAD
FC0F BD E6B0	3531:		JSR	ONEP
FC12 BD E401	3532:		JSR	SWAP
FC15 BD FB0C	3533:		JSR	MMOVE
FC18 39	3534:		RTS	
	3535:	*		
FC19 81	3536:		FCB	\$81
FC1A D0	3537:		FCB	\$D0
FC1B FC 08	3538:		FDB	REP-4
FC1D BD E52C	3539:	P	JSR	ONE
FC20 BD F9FC	3540:		JSR	TEXT
FC23 BD FC0C	3541:		JSR	REP
FC26 39	3542:		RTS	
	3543:	*		
FC27 81	3544:		FCB	\$81
FC28 C9	3545:		FCB	\$C9
FC29 FC 19	3546:		FDB	P-4
FC2B BD E414	3547:	INS	JSR	DUP
FC2E BD FB4B	3548:		JSR	S
FC31 BD FC0C	3549:		JSR	REP
FC34 39	3550:		RTS	
	3551:	*		
FC35 83	3552:		FCB	\$83
FC36 54	3553:		FCC	"TO"
FC37 4F				
FC38 D0	3554:		FCB	\$D0
FC39 FC 27	3555:		FDB	INS-4
FC3B BD E523	3556:	TOP	JSR	ZERO
FC3E BD E68C	3557:		JSR	RNUM
FC41 BD E46E	3558:		JSR	STORE
FC44 39	3559:		RTS	
	3560:	*		
FC45 85	3561:		FCB	\$85
FC46 43	3562:		FCC	"CLEA"
FC47 4C 45				
FC49 41				
FC4A D2	3563:		FCB	\$D2
FC4B FC 35	3564:		FDB	TOP-6
FC4D BD E61C	3565:	CLEAR	JSR	SCR
FC50 BD E46E	3566:		JSR	STORE
FC53 BD E044	3567:		JSR	CLITER
FC56 10	3568:		FCB	\$10
FC57 BD E523	3569:		JSR	ZERO
FC5A BD E0C1	3570:		JSR	XDO
FC5D BD E0DA	3571:	CL2	JSR	I
FC60 BD FB3A	3572:		JSR	ER
FC63 BD E07C	3573:		JSR	XLOOP
FC66 27 F5	3574:		BEQ	CL2
FC68 39	3575:		RTS	
	3576:	*		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 67

FC69 85	3577:	FCB	\$85
FC6A 46	3578:	FCC	"FLUS"
FC6B 4C 55			
FC6D 53			
FC6E C8	3579:	FCB	\$C8
FC6F FC 45	3580:	FDB	CLEAR-8
FC71 BD E044	3581: FLUSH	JSR	CLITER
FC74 08	3582:	FCB	8
FC75 BD E523	3583:	JSR	ZERO
FC78 BD E0C1	3584:	JSR	XDO
FC7B BD E02C	3585: FL2	JSR	LIT
FC7E 7F FF	3586:	FDB	\$7FFF
FC80 BD F2B4	3587:	JSR	BUFFER
FC83 BD E3F7	3588:	JSR	DROP
FC86 BD E07C	3589:	JSR	XLOOP
FC89 27 FO	3590:	BEQ	FL2
FC8B 39	3591:	RTS	
	3592: *		
FC8C 84	3593:	FCB	\$84
FC8D 43	3594:	FCC	"COP"
FC8E 4F 50			
FC90 D9	3595:	FCB	\$D9
FC91 FC 69	3596:	FDB	FLUSH-8
FC93 BD E57C	3597: COPY	JSR	BSCR
FC96 BD F157	3598:	JSR	STAR
FC99 BD E62A	3599:	JSR	OFFSET
FC9C BD E44E	3600:	JSR	AT
FC9F BD E399	3601:	JSR	PLUS
FCA2 BD E401	3602:	JSR	SWAP
FCA5 BD E57C	3603:	JSR	BSCR
FCA8 BD F157	3604:	JSR	STAR
FCAB BD E57C	3605:	JSR	BSCR
FCAE BD E3E9	3606:	JSR	OVER
FCB1 BD E399	3607:	JSR	PLUS
FCB4 BD E401	3608:	JSR	SWAP
FCB7 BD E0C1	3609:	JSR	XDO
FCBA BD E414	3610: COPY2	JSR	DUP
FCBD BD E0DA	3611:	JSR	I
FCC0 BD F314	3612:	JSR	BLOCK
FCC3 BD E535	3613:	JSR	TWO
FCC6 BD E707	3614:	JSR	SUB
FCC9 BD E46E	3615:	JSR	STORE
FCCC BD E680	3616:	JSR	ONEP
FCCF BD F24E	3617:	JSR	UPDATE
FCD2 BD E07C	3618:	JSR	XLOOP
FCD5 27 E3	3619:	BEQ	COPY2
FCD7 BD E3F7	3620:	JSR	DROP
FCDA BD FC71	3621:	JSR	FLUSH
FCDD 39	3622:	RTS	
	3623: *		
FCDE 86	3624:	FCB	\$86
FCDF 44	3625:	FCC	"DELET"
FCEO 45 4C			
FCE2 45 54			
FCE4 C5	3626:	FCB	\$C5
FCE5 FC 8C	3627:	FDB	COPY-7
FCE7 BD E345	3628: DELETE	JSR	TOR
FCEA BD FAEE	3629:	JSR	NLAG
FCED BD E399	3630:	JSR	PLUS
FCFO BD E36A	3631:	JSR	R

FORTH

SSB MNEMONIC ASSEMBLER PAGE 68

FCF3 BD E707 3632:	JSR	SUB
FCF6 BD FAEE 3633:	JSR	NLAG
FCF9 BD E36A 3634:	JSR	R
FCFC BD E3C2 3635:	JSR	MINUS
FCFF BD E68C 3636:	JSR	RNUM
FD02 BD E420 3637:	JSR	PSTORE
FD05 BD FADD 3638:	JSR	NLEAD
FD08 BD E399 3639:	JSR	PLUS
FD0B BD E401 3640:	JSR	SWAP
FD0E BD E22D 3641:	JSR	CMOVE
FD11 BD E358 3642:	JSR	FROMR
FD14 BD EC21 3643:	JSR	BLANKS
FD17 BD F24E 3644:	JSR	UPDATE
FD1A 39 3645:	RTS	
3646: *		
FD1B 81 3647:	FCB	\$81
FD1C C2 3648:	FCB	\$C2
FD1D FC DE 3649:	FDB	DELETE-9
FD1F BD EC4A 3650: B	JSR	PAD
FD22 BD E45E 3651:	JSR	CAT
FD25 BD E3C2 3652:	JSR	MINUS
FD28 BD FBAB 3653:	JSR	M
FD2B 39 3654:	RTS	
3655: *		
FD2C 81 3656:	FCB	\$81
FD2D C3 3657:	FCB	\$C3
FD2E FD 1B 3658:	FDB	B-4
FD30 BD E52C 3659: C	JSR	ONE
FD33 BD F9FC 3660:	JSR	TEXT
FD36 BD EC4A 3661:	JSR	PAD
FD39 BD E9D7 3662:	JSR	COUNT
FD3C BD FAEE 3663:	JSR	NLAG
FD3F BD E745 3664:	JSR	ROT
FD42 BD E3E9 3665:	JSR	OVER
FD45 BD E767 3666:	JSR	MIN
FD48 BD E345 3667:	JSR	TOR
FD4B BD E36A 3668:	JSR	R
FD4E BD E68C 3669:	JSR	RNUM
FD51 BD E420 3670:	JSR	PSTORE
FD54 BD E36A 3671:	JSR	R
FD57 BD E707 3672:	JSR	SUB
FD5A BD E345 3673:	JSR	TOR
FD5D BD E414 3674:	JSR	DUP
FD60 BD E6CA 3675:	JSR	HERE
FD63 BD E36A 3676:	JSR	R
FD66 BD E22D 3677:	JSR	CMOVE
FD69 BD E6CA 3678:	JSR	HERE
FD6C BD FADD 3679:	JSR	NLEAD
FD6F BD E399 3680:	JSR	PLUS
FD72 BD E358 3681:	JSR	FROMR
FD75 BD E22D 3682:	JSR	CMOVE
FD78 BD E358 3683:	JSR	FROMR
FD7B BD E22D 3684:	JSR	CMOVE
FD7E BD F24E 3685:	JSR	UPDATE
FD81 BD E523 3686:	JSR	ZERO
FD84 BD FBAB 3687:	JSR	M
FD87 39 3688:	RTS	
3689: *		
FD88 82 3690:	FCB	\$82
FD89 50 3691:	FCC	"P"

FORTH SSB MNEMONIC ASSEMBLER PAGE 69

FD8A AE	3692:	FCB	\$AE		
FD8B FA	56	3693:	FDB	WHERE-8	
FD8D BD	E044	3694:	PDOT	JSR	CLITER
FD90 40		3695:	FCB	\$40	
FD91 BD	E535	3696:	JSR	TWO	
FD94 BD	E482	3697:	JSR	CSTORE	
FD97 39		3698:	RTS		
		3699: *			
FD98 83		3700:	FCB	\$83	
FD99 4D		3701:	FCC	"MO"	
FD9A 4F					
FD9B CE		3702:	FCB	\$CE	
FD9C FD	88	3703:	FDB	PDOT-5	
FD9E 7E	FE86	3704:	MON	JMP	START
FDA1 39		3705:	RTS	Dummy	
		3706: *			
FDA2 84		3707:	FCB	\$84	
FDA3 4C		3708:	FCC	"LIN"	
FDA4 49	4E				
FDA6 CB		3709:	FCB	\$CB	
FDA7 FD	98	3710:	FDB	MON-6	
FDA9 BD	E53E	3711:	LINK	JSR	THREE
FDAC BD	F157	3712:	JSR	STAR	
FDAF BD	E044	3713:	JSR	CLITER	
FDB2 DO		3714:	FCB	\$DO	
FDB3 BD	E399	3715:	JSR	PLUS	
FDB6 BD	E414	3716:	JSR	DUP	
FDB9 BD	E044	3717:	JSR	CLITER	
FDBC 7E		3718:	FCB	\$7E	
FDBD BD	E401	3719:	JSR	SWAP	
FDC0 BD	E482	3720:	JSR	CSTORE	
FDC3 BD	E6B0	3721:	JSR	ONEP	
FDC6 BD	F545	3722:	JSR	TICK	
FDC9 BD	E401	3723:	JSR	SWAP	
FDCC BD	E46E	3724:	JSR	STORE	
FDCF 39		3725:	RTS		
		3726: *			
FDD0 84		3727:	FCB	\$84	
FDD1 4E		3728:	FCC	"NOO"	
FDD2 4F	4F				
FDD4 DO		3729:	FCB	\$DO	
FDD5 FD	A2	3730:	FDB	LINK-7	
FDD7 39		3731:	NOOP	RTS	
		3732: *			
OB00		3733:	BUB	EQU \$OB00	
		3734: *			
FDD8 36		3735:	BUBBLE	PSH A	
FDD9 B6	OB02	3736:	LDA A	BUB+2	
FDDC 85	01	3737:	BIT A	#01	
FDDE 27	04	3738:	BEQ	BB1	
FDE0 C6	20	3739:	LDA B	#\$20	
FDE2 32		3740:	BBO	PUL A	
FDE3 39		3741:	RTS		
FDE4 5D		3742:	BB1	TST B	
FDE5 27	FB	3743:	BEQ	BBO	
FDE7 5A		3744:	DEC B		
FDE8 27	07	3745:	BEQ	READ	
FDEA 5A		3746:	DEC B		
FDEB 27	45	3747:	BEQ	WRITE	
FDED C6	21	3748:	LDA B	#\$21	

FORTH

SSB MNEMONIC ASSEMBLER PAGE 70

FDEF 20 F1	3749:	BRA	BBO	
FDF1 EC 00	3750: READ	FDB	\$EC00	LDD O,X
FDF3 B7 0804	3751:	STA A	BUB+4	
FDF6 F7 0805	3752:	STA B	BUB+5	
FDF9 CC	3753:	FCB	\$CC	LDD #
FDFA 00 01	3754:	FDB	1	
FDFF B7 0806	3755:	STA A	BUB+6	
FE00 F7 0807	3756:	STA B	BUB+7	
FE02 EE 02	3757:	LDX	2,X	
FE04 86 05	3758:	LDA A	#5	
FE06 B7 0801	3759:	STA A	BUB+1	
FE09 B6 0802	3760: RD1	LDA A	BUB+2	
FE0C 85 01	3761:	BIT A	#1	
FE0E 26 F9	3762:	BNE	RD1	
FE10 86 01	3763:	LDA A	#1	
FE12 B7 0801	3764:	STA A	BUB+1	
FE15 F6 0802	3765: RD2	LDA B	BUB+2	
FE18 2B OC	3766:	BMI	RD3	
FE1A C5 20	3767:	BIT B	#\$20	
FE1C 27 F7	3768:	BEQ	RD2	
FE1E B6 0800	3769:	LDA A	BUB	
FE21 A7 00	3770:	STA A	O,X	
FE23 08	3771:	INX		
FE24 20 EF	3772:	BRA	RD2	
FE26 C5 02	3773: RD3	BIT B	#2	
FE28 26 03	3774:	BNE	RDERR	
FE2A 5F	3775:	CLR B		
FE2B 32	3776:	PUL A		
FE2C 39	3777:	RTS		
FE2D F6 0803	3778: RDERR	LDA B	BUB+3	
FE30 32	3779:	PUL A		
FE31 39	3780:	RTS		
	3781: *			
FE32 EC 00	3782: WRITE	FDB	\$EC00	LDD O,X
FE34 B7 0804	3783:	STA A	BUB+4	
FE37 F7 0805	3784:	STA B	BUB+5	
FE3A CC	3785:	FCB	\$CC	LDD #
FE3B 00 01	3786:	FDB	1	
FE3D B7 0806	3787:	STA A	BUB+6	
FE40 F7 0807	3788:	STA B	BUB+7	
FE43 EE 02	3789:	LDX	2,X	
FE45 86 06	3790:	LDA A	#6	
FE47 B7 0801	3791:	STA A	BUB+1	
FE4A B6 0802	3792: WT1	LDA A	BUB+2	
FE4D 85 01	3793:	BIT A	#1	
FE4F 26 F9	3794:	BNE	WT1	
FE51 86 02	3795:	LDA A	#2	
FE53 B7 0801	3796:	STA A	BUB+1	
FE56 F6 0802	3797: WT2	LDA B	BUB+2	
FE59 2B OC	3798:	BMI	WT3	
FE5B C5 40	3799:	BIT B	#\$40	
FE5D 27 F7	3800:	BEQ	WT2	
FE5F A6 00	3801:	LDA A	O,X	
FE61 B7 0800	3802:	STA A	BUB	
FE64 08	3803:	INX		
FE65 20 EF	3804:	BRA	WT2	
FE67 C5 02	3805: WT3	BIT B	#2	
FE69 26 03	3806:	BNE	WTERR	
FE6B 5F	3807:	CLR B		
FE6C 32	3808:	PUL A		

FORTH

SSB MNEMONIC ASSEMBLER PAGE 71

FE6D 39	3809:	RTS		
FE6E F6 0803	3810: WTERR	LDA B	BUB+3	
FE71 32	3811:	PUL	A	
FE72 39	3812:	RTS		
	3813: *			
	3814: *			
	3815: *			
	3816: * MONITOR			
	3817: *			
00EF	3818: STACK	EQU	\$00EF	
00FA	3819:	ORG	\$00FA	
00FA	3820: XTEMPM	RMB	2	
00FC	3821: SP	RMB	2	
00FE	3822: XHI	RMB	1	
00FF	3823: XLOW	RMB	1	
	3824: *			
FE7E	3825:	ORG	\$FE7E	
	3826: *			
FE7E CC	3827: FTHSTR	FCB	\$CC	LDD #
FE7F OC 0A	3828:	FDB	\$OC0A	
FE81 DD	3829:	FCB	\$DD	STD
FE82 10	3830:	FCB	ACIAC-1	
FE83 7E E001	3831:	JMP	ORIG+1	
FE86 8E 00EF	3832: START	LDS	#STACK	
FE89 9F FC	3833:	STS	SP	
FE8B CC	3834:	FCB	\$CC	LDD #
FE8C OC 0A	3835:	FDB	\$OC0A	
FE8E DD	3836:	FCB	\$DD	STD
FE8F 10	3837:	FCB	ACIAC-1	
FE90 9E FC	3838: CONTRL	LDS	SP	
FE92 CE FFDA	3839:	LDX	#MESSG1	
FE95 BD FF09	3840:	JSR	JDATA1	
FE98 BD FF08	3841:	JSR	PDATA3	
FE9B BD FF10	3842:	JSR	INCH	
FE9E 16	3843:	TAB		
FE9F BD FF62	3844:	JSR	OUTS	
FEA2 CE FFE2	3845:	LDX	#FCTABL	
FEA5 E1 00	3846: NXTCHR	CMP B	0, X	
FEA7 27 0A	3847:	BEQ	GOODCH	
FEA9 08	3848:	INX		
FEAA 08	3849:	INX		
FEAB 08	3850:	INX		
FEAC 8C FFEE	3851:	CPX	#FCTBEN	
FEAF 26 F4	3852:	BNE	NXTCHR	
FEB1 20 DD	3853:	BRA	CONTRL	
FEB3 EE 01	3854: GOODCH	LDX	1, X	
FEB5 6E 00	3855:	JMP	0, X	
FEB7 BD 57	3856: INHEX	BSR	INCH	
FEB9 80 30	3857: INHEX2	SUB A	#'0	
FEBB 2B D3	3858:	BMI	CONTRL	
FEBD 81 09	3859:	CMP A	#9	
FEBF 2F 0A	3860:	BLE	IN1HG	
FEC1 81 11	3861:	CMP A	#\$11	
FEC3 2B C8	3862:	BMI	CONTRL	
FEC5 81 16	3863:	CMP A	#\$16	
FEC7 2E C7	3864:	BGT	CONTRL	
FEC9 80 07	3865:	SUB A	#7	
FECA 39	3866: IN1HG	RTS		
FECC 86 07	3867: ERRORM	LDA A	#7	
FECE 8D 28	3868:	BSR	OUTCH	

FORTH

SSB MNEMONIC ASSEMBLER PAGE 72

FED0 86 3F	3869:	LDA A #?'?
FED2 8D 27	3870:	BSR OUTCH
FED4 20 BA	3871:	BRA CONTRL
FED6 8D 09	3872: BADDR	BSR BYTE
FED8 97 FE	3873:	STA A XHI
FEDA 8D 05	3874:	BSR BYTE
FEDC 97 FF	3875:	STA A XLOW
FEDE DE FE	3876:	LDX XHI
FEE0 39	3877:	RTS
FEE1 8D D4	3878: BYTE	BSR INHEX
FEE3 48	3879: BYTE2	ASL A
FEE4 48	3880:	ASL A
FEE5 48	3881:	ASL A
FEE6 48	3882:	ASL A
FEE7 16	3883:	TAB
FEE8 8D CD	3884:	BSR INHEX
FEEA 1B	3885:	ABA
FEEB 16	3886:	TAB
FEEC 39	3887:	RTS
FEED 44	3888: OUTHL	LSR A
FEEE 44	3889:	LSR A
FEEF 44	3890:	LSR A
FEFO 44	3891:	LSR A
FEF1 84 0F	3892: OUTHR	AND A #\$F
FEF3 8B 30	3893:	ADD A #'0
FEF5 81 39	3894:	CMP A #'9
FEF7 23 02	3895:	BLS OUTCH
FEF9 8B 07	3896:	ADD A #7
FEFB 37	3897: OUTCH	PSH B
FEFC D6 11	3898: OUTC1	LDA B ACIAC
FEFE C5 20	3899:	BIT B #\$20
FF00 27 FA	3900:	BEQ OUTC1
FF02 97 13	3901:	STA A ACIAD+1
FF04 33	3902:	PUL B
FF05 39	3903:	RTS
FF06 8D F3	3904: PDATA2	BSR OUTCH
FF08 08	3905: PDATA3	INX
FF09 A6 00	3906: JDATA1	LDA A O,X
FF0B 81 04	3907:	CMP A #4
FF0D 26 F7	3908:	BNE PDATA2
FF0F 39	3909:	RTS
FF10 96 11	3910: INCH	LDA A ACIAC
FF12 48	3911:	ASL A
FF13 24 FB	3912:	BCC INCH
FF15 96 12	3913:	LDA A ACIAD
FF17 84 7F	3914:	AND A #\$7F
FF19 20 E0	3915:	BRA OUTCH
FF1B 8D 42	3916: CHANGE	BSR BADDRS
FF1D DE FE	3917:	LDX XHI
FF1F 8D 3A	3918:	BSR OUT2HS
FF21 09	3919:	DEX
FF22 8D EC	3920: CHA1	BSR INCH
FF24 81 0A	3921:	CMP A #\$A
FF26 27 19	3922:	BEQ LF
FF28 81 5E	3923:	CMP A #\$5E
FF2A 27 0E	3924:	BEQ UA
FF2C BD FEB9	3925:	JSR INHEX2
FF2F 8D B2	3926:	BSR BYTE2
FF31 A7 00	3927:	STA A O,X
FF33 A1 00	3928:	CMP A O,X

FORTH

SSB MNEMONIC ASSEMBLER PAGE 73

FF35 27 EB	3929:	BEQ	CHA1
FF37 7E FECC	3930:	JMP	ERRORM
FF3A 86 OA	3931: UA	LDA A	#\$A
FF3C 8D BD	3932:	BSR	OUTCH
FF3E 09	3933:	DEX	
FF3F 20 01	3934:	BRA	LF1
FF41 08	3935: LF	INX	
FF42 DF FE	3936: LF1	STX	XHI
FF44 CE FFDB	3937:	LDX	#MESSG1+1
FF47 8D C0	3938:	BSR	JDATA1
FF49 CE 00FE	3939:	LDX	#XHI
FF4C 8D OB	3940:	BSR	OUT4HS
FF4E 20 CD	3941:	BRA	CHANGE+2
FF50 A6 00	3942: OUT2H	LDA A	0, X
FF52 08	3943:	INX	
FF53 36	3944: OUT2HA	PSH A	
FF54 8D 97	3945:	BSR	OUTHL
FF56 32	3946:	PUL A	
FF57 20 98	3947:	BRA	OUTHR
FF59 8D F5	3948: OUT4HS	BSR	OUT2H
FF5B 8D F3	3949: OUT2HS	BSR	OUT2H
FF5D 20 03	3950:	BRA	OUTS
FF5F BD FED6	3951: BADDRS	JSR	BADDR
FF62 86 20	3952: OUTS	LDA A	#\$20
FF64 20 95	3953:	BRA	OUTCH
FF66 CE FFDA	3954: PRINT	LDX	#MESSG1
FF69 8D 9E	3955:	BSR	JDATA1
FF6B DE FC	3956:	LDX	SP
FF6D 08	3957:	INX	
FF6E 8D EB	3958:	BSR	OUT2HS
FF70 8D E9	3959:	BSR	OUT2HS
FF72 8D E7	3960:	BSR	OUT2HS
FF74 8D E3	3961:	BSR	OUT4HS
FF76 8D E1	3962:	BSR	OUT4HS
FF78 CE 00FC	3963:	LDX	#SP
FF7B 20 DC	3964:	BRA	OUT4HS
FF7D 37	3965: GO	PSH B	
FF7E BD FF5F	3966:	JSR	BADDRS
FF81 0F	3967:	SEI	
FF82 6E 00	3968:	JMP	0, X
FF84 9F FC	3969: SWIENT	STS	SP
FF86 30	3970:	TSX	
FF87 6D 06	3971:	TST	6, X
FF89 26 02	3972:	BNE	SW1
FF8B 6A 05	3973:	DEC	5, X
FF8D 6A 06	3974: SW1	DEC	6, X
FF8F BD FF66	3975: REG	JSR	PRINT
FF92 7E FE90	3976:	JMP	CONTRL
FF95 CE FFA0	3977: TRAP	LDX	#MESSG2
FF98 BD FF09	3978:	JSR	JDATA1
FF9B 9F FC	3979:	STS	SP
FF9D 30	3980:	TSX	
FF9E 20 EF	3981:	BRA	REG
FFA0 54	3982: MESSG2	FCC	"TRAPPED AT "
FFA1 52 41			
FFA3 50 50			
FFA5 45 44			
FFA7 20 41			
FFA9 54 20			
FFAB 04	3983:	FCB	4

FORTH

SSB MNEMONIC ASSEMBLER PAGE 74

```

FFAC CE FFDA 3984: LCMD    LDX    #MESSG1
FFAF BD FF09 3985:      JSR    JDATA1
FFB2 BD FF5F 3986:      JSR    BADDRS
FFB5 BD FEE1 3987: LCMD1   JSR    BYTE
FFB8 A7 00 3988:       STA A 0,X
FFBA A1 00 3989:       CMP A 0,X
FFBC 27 03 3990:       BEQ . LCMD2
FFBE 7E FECC 3991:      JMP    ERRORM
FFC1 08 3992: LCMD2   INX
FFC2 DF FA 3993:       STX    XTEMPM
FFC4 86 0F 3994:       LDA A #$F
FFC6 94 FB 3995:       AND A XTEMPM+1
FFC8 26 EB 3996:       BNE   LCMD1
FFCA CE FFDA 3997:      LDX    #MESSG1
FFCD BD FF09 3998:      JSR    JDATA1
FFD0 CE 00FA 3999:      LDX    #XTEMPM
FFD3 BD FF59 4000:      JSR    OUT4HS
FFD6 DE FA 4001:       LDX    XTEMPM
FFD8 20 DB 4002:       BRA   LCMD1
FFDA 0A 4003: MESSG1  FCB   $A,$D,0,0,0,4,$2A,4
FFDB 0D 00
FFDD 00 00
FFDF 04 2A
FFE1 04
FFE2 4D 4004: FCTABL FCC   "M"
FFE3 FF 1B 4005:      FDB   CHANGE
FFE5 52 4006:       FCC   "R"
FFE6 FF 8F 4007:      FDB   REG
FFE8 58 4008:       FCC   "X"
FFE9 FF 7D 4009:      FDB   GO
FFE9 4C 4010:       FCC   "L"
FFEC FF AC 4011:      FDB   LCMD
        4012: *
FFEE FF 95 4013: FCTBEN FDB   TRAP
FFF0 00 D0 4014:      FDB   SCI
FFF2 00 D3 4015:      FDB   TOF
FFF4 00 D6 4016:      FDB   OCF
FFF6 00 D9 4017:      FDB   ICF
FFF8 00 DC 4018:      FDB   IRQ1
FFFA FF 84 4019:      FDB   SWIENT    SWI
FFFC FE 86 4020:      FDB   START     NMI
FFFE FE 7E 4021:      FDB   FTHSTR    RESET
        4022: *
        4023: END

```

NO ERROR(S) DETECTED

SYMBOL TABLE:

ABORT	F055	ABS	F1DA	ABS2	F1E8	ACIAC	0011
ACIAD	0012	AGAIN	F679	ALLOT	E6D9	AND	E2D5
ARROW	F45C	AT	E44E	B	FD1F	BACK	F5C3
BACKSP	E00E	BADDR	FED6	BADDRS	FF5F	BASE	E661
BBO	FDE2	BB1	FDE4	BBUF	E56F	BCOMP	EECE
BDIGS	F737	BEGIN	F5DE	BL	E548	BLANKS	EC21
BLK	E5FC	BLOCK	F314	BLOCK3	F33D	BLOCK4	F363
BLOCK5	F386	BSCR	E57C	BUB	0800	BUBBLE	FDD8
BUFFER	F2B4	BUFFR2	F2C0	BUFFR3	F2F6	BUILDS	E98E
BYTE	FEE1	BYTE2	FEE3	C	FD30	CAT	E45E
CCOMM	E6F6	CENT	F081	CHA1	FF22	CHANGE	FF1B

FORTH

SSB MNEMONIC ASSEMBLER PAGE 75

CL	F9F0	CL2	FC5D	CLEAR	FC4D	CLITER	E044
CMOV2	E241	CMOV3	E25A	CMOVE	E22D	COLD	F081
COLD2	F087	COLD3	F096	COLINT	E022	COLON	E495
COLUMNS	E6A6	COMMA	E6E4	COMPIL	E8CF	CON	E4CE
CONTRL	FE90	CONTXT	E639	COPY	FC93	COPY2	FCBA
COUNT	E9D7	CR	E21D	CREAT2	EE80	CREATE	EE59
CSP	E682	CSTORE	E482	CURENT	E648	DABS	F1F0
DABS2	F1FE	DDOT	F806	DDOTR	F7D9	DDUP	E79E
DDUP2	E7A9	DEC	E93D	DEFIN	EFEA	DEL	FB7C
DEL2	FB8F	DELETE	FCE7	DELINT	E024	DFIND	ED95
DFIND2	EDC1	DIG	F77A	DIG2	F79C	DIGIT	E0EE
DIGITO	E102	DIGIT1	E10A	DIGIT2	E10D	DIGS	F7AC
DLINE	F3C5	DLITE2	EF26	DLITER	EF12	DMINUS	E3D2
DO	F613	DOCON	E4E0	DODOES	E9C5	DOES	E9A3
DOT	F814	DOTQ	EA82	DOTQ1	EAA8	DOTQ2	EAB4
DOTR	F7C6	DOUSER	E511	DOVAR	E4FD	DOVOC	EFD2
DP	E5E1	DPINIT	E01E	DPL	E66C	DPLMI	F976
DPLMI2	F981	DPLUS	E3A7	DRB	F4D9	DRIVE	F4E6
DRONE	F29F	DROP	E3F7	DRZERO	F28F	DTRAIL	EA26
DTRAL2	EA2F	DTRAL3	EA51	DTRAL4	EA57	DUP	E414
DWNCNT	0088	EDIGS	F746	EDITOR	FA4A	ELSE	F6DA
EMIT	E1DC	ENCL2	E193	ENCL3	E1A0	ENCL4	E1A3
ENCL5	E1B0	ENCL6	E1B6	ENCL7	E1BC	ENCL8	E1C0
ENCLOS	E18A	END	F66D	ENDIF	F5F0	EQUAL	E712
ER	FB3A	ERAM	F133	ERASE	EC11	ERROR	EDD8
ERROR2	EDE9	ERRORM	FECC	EXEC	E05D	EXPEC2	EB06
EXPEC3	EB45	EXPEC4	EB62	EXPEC5	EB65	EXPEC6	EB77
EXPECT	EAFA	FCTABL	FFE2	FCTBEN	FFEE	FENCE	E5D7
FENCIN	E01C	FILL	EBEA	FIRST	E555	FL2	FC7B
FLD	E677	FLUSH	FC71	FORGET	F561	FORTH	2008
FOUND	E16B	FROMR	E358	FTHSTR	FE7E	GO	FF7D
GOODCH	FEB3	GREAT	E738	H	FB1D	HERE	E6CA
HEX	E928	HLD	E697	HLFCYC	0082	HOLD	EC2F
I	E0DA	ICF	OOD9	IDDOT	EE16	IF	F6B1
IMMEDI	EF8B	IN	E606	IN1HG	FECB	INCH	FF10
INDEX	F87F	INDEX2	F88B	INDEX3	F8AE	INHEX	FE87
INHEX2	FEB9	INS	FC2B	INTER3	EF55	INTER4	EF58
INTER5	EF5A	INTER6	EF73	INTER7	EF79	INTERP	EF33
IOSTAT	4036	IRQ1	OODC	JDATA1	FF09	JMPTAB	FOEF
KEY	E1F6	KEY1	E1FB	L	FBF8	LATEST	E7E0
LBRAK	E8F5	LCMD	FFAC	LCMD1	FFB5	LCMD2	FFC1
LEAVE	E336	LESS	E71D	LESSF	E729	LESST	E72C
LESSX	E72E	LF	FF41	LF1	FF42	LFA	E7F0
LIMIT	E562	LINE	FA22	LINK	FDA9	LIST	F82D
LIST2	F853	LIT	E02C	LITER	EEF2	LITER2	EF06
LOAD	F419	LOOP	F627	M	FBAB	MAX	E782
MAX2	E793	MEMEND	E000	MEMTOP	DFFF	MESS	F3D9
MESS2	F402	MESS3	F404	MESS4	F411	MESSG1	FFDA
MESSG2	FFAO	MIN	E767	MIN2	E778	MINUS	E3C2
MMOVE	FB0C	MOD	F185	MON	FD9E	MSLASH	F9BC
MSMOD	F1B8	MSTAR	F998	MTBUF	F279	MUDFLG	0080
N	00E0	NBLK	0008	NFA	E7FD	NLAG	FAEE
NLEAD	FADD	NLOC	FAC8	NOOP	FDD7	NULL	EBA8
NULL2	EBDC	NULL3	E8E2	NUMB	ED25	NUMB1	ED4C
NUMB2	ED7E	NUMB3	ED8C	NXTCHR	FEA5	OCF	OOD6
OFFSET	E62A	ONE	E52C	ONEP	E6B0	OR	E2E5
ORIG	E000	OUT	E611	OUT2H	FF50	OUT2HA	FF53
OUT2HS	FF5B	OUT4HS	FF59	OUTC1	FEFC	OUTCH	FEFB
OUTHL	FEED	OUTHR	FEF1	OUTS	FF62	OVER	E3E9
OVRFW5	0084	P	FC1D	PABORT	EDCC	PAD	EC4A

FORTH SSB MNEMONIC ASSEMBLER PAGE 76

PAREN	EFFB	PBUF	F21D	PBUF2	F238	PCR	F4BC
PCR2	F4CA	PDATA2	FF06	PDATA3	FF08	PDOT	FD8D
PDOTQ	EA64	PEMIT	F481	PEMIT2	F485	PEMIT3	F48A
PFA	E813	PFIND	E11D	PFIND1	E12B	PFIND2	E13E
PFIND3	E154	PFIND4	E162	PFIND8	E15F	PFIND9	E164
PKEY	F49B	PLINE	F399	PLMI	F987	PLMI2	F992
PLOOP	F63F	PLUS	E399	PNUMB	ECC4	PNUMB3	ED13
PNUMB4	ED18	PORIG	E58B	PQTER	F4B1	PQTER2	F4BB
PREV	F211	PRINT	FF66	PSCODE	E952	PSTORE	E420
QCOMP	E853	QCSP	E895	QERR	E83A	QERR2	E847
QERR3	E84A	QEXEC	E86C	QLOAD	E8B4	QPAIRS	E883
QSTAC2	EADA	QSTAC3	EAFO	QSTACK	EABE	QTERM	E211
QUERY	EB8B	QUEST	F81F	QUIT	F00A	QUIT2	F016
QUIT3	F04A	R	E36A	R BRAK	E903	RD1	FE09
RD2	FE15	RD3	FE26	RDERR	FE2D	READ	FDF1
REG	FF8F	REND	2035	REP	FC0C	REPEAT	F693
RFORTH	F106	RINIT	E014	RNUM	E68C	ROT	E745
RPSTOR	E31D	RTASK	F132	RW	F4FA	RW2	F519
RW3	F51C	RW4	F540	RZERO	E5A3	S	FB4B
S2	FB5B	SCI	OODO	SCR	E61C	SCSP	E827
SEMI	E4B2	SEMIC	E974	SEMIS	E32A	SIGFLG	0086
SIGN	F763	SIGN2	F775	SINIT	E012	SLASH	F175
SLMOD	F164	SMUDGE	E917	SP	00FC	SPACE	E75A
SPACE2	F729	SPACE3	F731	SPACES	F715	SPAT	E307
SPSTOR	E312	SSLASH	F1A6	SSMOD	F194	STACK	00EF
STAR	F157	START	FE86	STATE	E655	STOD	F149
STORE	E46E	SUB	E707	SW1	FF8D	SWAP	E401
SWIENT	FF84	SZERO	E599	T	FB08	TASK	2034
TEXT	F9FC	THEN	F60A	THREE	E53E	TIB	E5AE
TICK	F545	TOF	OOD3	TOGGLE	E43A	TOP	FC3B
TOR	E345	TRAP	FF95	TRAV	E7B5	TRAV2	E7B8
TRIAD	F8BF	TRIAD2	F8DA	TRIADS	F8EE	TWO	E535
TWOP	E6BC	TYPE	E9EB	TYPE2	E9FF	TYPE3	EA16
TYPE4	EA19	UA	FF3A	UNTIL	F657	UORIG	4000
UP	OOF2	UPDATE	F24E	UPINIT	E010	USE	F205
USER	E50B	USL1	E2A5	USL2	E2AF	USL3	E2B2
USL4	E2B5	USL5	E2C3	USLASH	E29E	USTAR	E262
USTAR2	E284	USTAR3	E28A	VAR	E4F7	VLIST	F909
VLIST1	F91C	VLIST2	F943	VOCAB	EFA3	VOCINT	E020
VOCLIN	E5F1	WARM2	FOCF	WARN	E5CA	WENT	FOC9
WHERE	FA5E	WHILE	F705	WIDTH	E5BB	WORD	EC5C
WORD2	EC72	WORD3	EC78	WRITE	FE32	WT1	FE4A
WT2	FE56	WT3	FE67	WTERR	FE6E	XBASE	4026
XBLK	4016	XCOLUMN	4034	XCONT	4020	XCSP	402C
XCURR	4022	XDELAY	4032	XDO	E0C1	XDP	4012
XDPL	4028	XFENCE	4010	XFLD	402A	XHI	00FE
XHLD	4030	XIN	4018	XLOOP	E07C	XLOW	00FF
XOFSET	401E	XOR	E2F6	XOUT	401A	XPOLOF	EOA5
XPLONO	EOAB	XPLOOP	E08B	XPLOP2	E08F	XPLOPS	E09F
XPREV	4042	XRNUM	402E	XRZERO	4008	XSCR	401C
XSPZER	4006	XSTATE	4024	XTEMP	00F0	XTEMFM	00FA
XTIB	400A	XUSE	4040	XVOCL	4014	XWARN	400E
XWIDTH	400C	ZBRAN	E06E	ZYES	E0B6	ZEQU	E37B
ZEQU2	E382	ZERO	E523	ZLESS	E38B	ZLESS2	E391

APPENDIX A2 PATSY MACHINE CODE LISTING

*ROLLING-BUFFER CODE

*

*The code part of an array created by

*ROLLING-BUFFER is :-

* JSR ROLLBF

* 00 00 00

* Address of pointer field in RAM

* Address of last element

*

*The pointer field immediately precedes

*the array and contains the address of

*the next element to be accessed.

*

*

N EQU \$E0 Scratch area
XTEMP EQU \$FO

0000 DF FO	ROLLBF	STX XTEMP	Save data stack pointer
0002 38		PUL X	Copy return address which is
0003 3C		PSH X	also the parameter pointer
0004 EE 03		LDX 3,X	X = the pointer field address
0006 EC 00		LDD 0,X	D = the next element address
0008 DD EO		STD N	Save it in scratch area
000A C3 0002		ADD D #2	Advance to next element
000D ED 00		STD 0,X	and store if back in pointer field
000F 38		PUL X	Remove return address
0010 A3 05		SUB D 3,X	Last element's address?
0012 23 09		BLS RB1	Lower or same?
0014 EC 03		LDD 3,X	No. D = pointer field address
0016 EE 03		LDX 3,X	and so does X
0018 C3 0002		ADD D #2	First element address is 2 on from
001B ED 00		STD 0,X	pointer field. Now save it there.
001D DE FO	RB1	LDX XTEMP	Recover data stack pointer
001F DC EO		LDD N	and element's address
0021 ED 00		STD 0,X	Push it onto the stack
0023 09		DEX	and adjust the stack
0024 09		DEX	pointer
0025 39		RTS	Put here by RETURN

*Note. This is called as a subroutine but the return address is removed from the stack so when RTS is executed it is the underlying return address that is used.

*

*

*ARRAY+ CODE

*This is practically the same as for ROLLING-BUFFER

*

0000 DF FO	ARRAYF	STX XTEMP	
0002 38		PUL X	
0003 3C		PSH X	
0004 EE 03		LDX 3,X	
0006 EC 00		LDD 0,X	
0008 DD EO		STD N	
000A C3 0002		ADD D #2	
000D ED 00		STD 0,X	
000F 38		PUL X	
0010 A3 05		SUB D 3,X	

```
0012 23 06      BLS ARP1
0014 EC 05      LDD 5,X Get last element's address
0016 EE 03      LDX 3,X X = pointer field
0018 ED 00      STD 0,X Point to last element
001A DE F0      ARP1   LDX XTEMP
001C DC E0      LDD N
001E ED 00      STD 0,X
0020 09          DEX
0021 09          DEX
0022 39          RTS
*
*
*TISR Timer interrupt service routine.
*----
*This routine counts down the whole number of counter cycles
*required by long delays.
*
        TIMCNT EQU $0B Timer control register.
        TIMOCR EQU $0B Timer o/p compare reg.
        OVFLWS EQU $84 No. of complete counter cycles
        CORRFG EQU $90 Small residual correction flag
```

```
0000 DC 08      TISR   LDD TIMCNT Dummy read
0002 DE 84      LDX OVFLWS
0004 27 05      BEQ TIS1   Down to zero yet?
0006 09          DEX     No. Decrement the count.
0007 DF 84      STX OVFLWS and store it back
0009 26 12      BNE TIS2   Has it become zero?
000B 96 08      TIS1   LDA A TIMCNT Yes. Read control reg.
000D 84 F7      AND A #$F7 and mask off interrupt
000F 97 08      STA A TIMCNT enable bit.
0011 7D 0091    TST CORRFG+1 Correction needed?
0014 27 07      BEQ TIS2   If no then skip
0016 DC 0B      LDD TIMOCR Subtract the 128
0018 83 0080    SUB D #128 that was added by DELAY
001B 20 02      BRA TIS3
001D DC 0B      TIS2   LDD TIMOCR Read TIMOCR and write to it
001F DD 0B      TIS3   STD TIMOCR to clear the flag.
0021 3B          RTI     Put here by TFORTH RTI.
```

```
*
*
*SISR Signal interrupt service routine
*----
*
*The interrupt flag is cleared by first reading the control
*register then the timer i/p capture register.
*
```

```
        TIMICR EQU $0D
        SIGFLG EQU $86

0000 96 08      SISR   LDA A TIMCNT Read control reg.
0002 D6 0D      LDA B TIMICR Dummy read TIMICR
0004 84 EF      AND A #$EF Mask off interrupt
0006 97 08      STA A TIMCNT enable bit.
0008 4F          CLR A
0009 5F          CLR B
000A DD 86      STD SIGFLG Clear SIGFLG
000C 3B          RTI     Put here by TFORTH RTI
```

```
*  
*  
*MSISR Mud sensor interrupt service routine  
*----  
*  
*Two interrupts vector here though the second should  
*not occur.  
*  
*  
MUDFLG EQU $80 Set on optical switch interrupt  
ADCDAT EQU $1000 ADC data port  
ADCCNT EQU $1002 ADC control port  
  
0000 B6 1002 MSISR LDA A ADCCNT Get interrupt flag - MSB  
0003 2B 05 BMI MS1 Is it set?  
0005 B6 1000 LDA A ADCDAT No. Read to clear other  
0008 20 07 BRA MS2 unused interrupt flag  
000A B6 1000 MS1 LDA A ADCDAT Dummy read to clear flag  
000D 86 FF LDA A #$FF Set MUDFLG  
000F 97 80 STA A MUDFLG  
0011 3B MS2 RTI  
*  
*  
*SERIAL Serial interrupt service routine  
*----  
*This interrupt should not happened  
*  
*  
0000 96 11 SERIAL LDA A $11 Read serial interface control reg.  
0002 84 EB AND A #$EB Mask off interrupt enable bit  
0004 97 11 STA A $11  
0006 3B RTI  
*  
*  
*TIMER-0'FLOW interrupt service routine  
*  
*Should this accidentally happen the double byte read of  
*TIMCNT and the adjacent register ($09), the high byte  
*of the timer followed by a write to TIMCNT will clear  
*the interrupt flag. The enable bit is also masked off.  
*  
*  
0000 DC 08 TOF LDD TIMCNT Get TIMOCR and read timer  
0002 84 FB AND A #$FB Mask off interrupt  
0004 97 08 STA A TIMCNT enable bit.  
0006 3B RTI  
*  
*  
*SORT  
*----  
*  
*The PING-LIST generated by PREPARE need not be in  
*order of delay values. This routine compares adjacent  
*values and swaps them if they are in the wrong order  
*and progresses through the list. This is repeated from  
*the start unless the previous pass resulted in no swaps.  
*  
0000 3C SORT PSH X Save data stack pointer  
0001 86 01 SRT1 LDA A #1 Set pass flag
```

0003 36 PSH A and save it.
0004 CE **** LDX #PING-LIST+2 Start of list

0007 EC 00 SRT2 LDD 0,X Compare two values
0009 A3 02 SUB D 2,X
000B 2F 13 BLE SRT3 in order?
000D A6 00 LDA A 0,X No
000F E6 02 LDA B 2,X Swap them
0011 A7 02 STA A 2,X
0013 E7 00 STA B 0,X.
0015 A6 01 LDA A 1,X
0017 E6 03 LDA B 3,X
0019 A7 03 STA A 3,X
001B E7 01 STA B 1,X
001D 32 PUL A Get pass flag
001E 4F CLR A Clear it
001F 36 PSH A and save it again
0020 08 INX Advance through list
0021 08 INX
0022 8C **** CPX #PING-LIST+16 End?
0025 26 E0 BNE SRT2 Try next pair if not
0027 32 PUL A Yes. Get pass flag
0028 4D TST A Any swaps during this pass?
0029 27 D6 BEQ SRT1 If yes then try once more
002B 38 PUL X No finished
002C 39 RTS

*
*CHECK
*
*This checks for three possibilities.
* Values less than 20 mSec. (or negative)
* Values that are too large.
* Values too close (< 20 mSec. apart)
*There are eight values in the list but room for 10.
*The 9th and 10th values are zeroed. The 9th acts as a
*delimiter in this routine and the 10th is left to terminate
*the PING-LIST.
*In the first phase values less than 20 are lost by shifting
*the whole list up.
*Values too large are then replaced by a maximum value. It
*does not matter if there are more than one of these as the
*last phase will sort this out.
*Finally pairs of values are checked for a difference of less
*than 20 where-upon the second replaces the first.
*

0000 3C CHECK PSH X Save data stack pointer
0001 CE **** LDX #PING-LIST
0004 4F CLR A
0005 5F CLR B
0006 ED 12 STD 18,X Add delimiter
0008 ED 14 STD 20,X Terminate list
000A 86 08 LDA A #8 No. of passes
000C 36 PSH A
000D CE **** CHK1 LDX #PING-LIST
0010 EC 02 LDD 2,X 1st entry
0012 83 0014 SUB D #20 Less than 20 mSecs?
0015 2A 10 BPL CHK3
0017 EC 04 CHK2 LDD 4,X Yes, shift remaining
0019 ED 02 STD 2,X values up the list
001B 08 INX

001C 08	INX
001D 8C ****	CPX #PING-LIST+16
0020 26 F5	BNE CHK2
0022 32	PUL A Get No. of passes
0023 4A	DEC A Try another pass?
0024 36	PSH A
0025 26 E6	BNE CHK1 Last pass?
0027 32	CHK3
0028 CE ****	PUL A
002B EC 02	CHK4
002D 26 07	LDX #PING-LIST
002F CC 07AD	LDD 2,X If this is zero then
0032 ED 02	BNE CHK5 whole list was <20
0034 20 11	LDD #1965 Set maximum delay
0036 83 0799	STD 2,X
0039 25 05	BRA CHK7 and skip to next phase
003B CC 0799	SUB D #1945
003E ED 02	BCS CHK6 Greater than 1945?
0040 08	LDD #1965 Set = maximum
0041 08	STD 2,X
0042 8C ****	CHK6
0045 26 E4	INX
0047 CE ****	CHK7
004A EC 04	CHK8
004C 27 1F	LDX #PING-LIST
004E A3 02	LDD 4,X Get 2nd value. If this
0050 83 0013	BEQ CHK12 is zero, we're finished
0053 2A 11	SUB D 2,X Is it more than 19
0055 3C	SUB D #19 from previous?
0056 EC 04	BPL CHK11
0058 ED 02	CHK9
005A 27 07	PSH X
005C 08	LDD 4,X Over-write previous with
005D 08	STD 2,X it and shift the remainder
005E 8C ****	BEQ CHK10 of the list up
0061 26 F3	INX
0063 38	CHK10
0064 20 E4	PUL X
0066 08	BRA CHK8 Loop back until delimiter
0067 08	CHK11 INX found
0068 8C ****	INX
006B 26 DD	CPX #PING-LIST+16
006D 38	BNE CHK8
006E 39	PUL X Recover data stack pointer
*	RTS

*
*
*SAMPLE

*
*The ADC and multiplexer are accessed through a 16-bit parallel port. The least significant 12 lines are programmed as inputs from the ADC and 3 of the most significant bits are set-up as outputs to the multiplexer. The control line CA2 is used to switch the S&H chip while CB2 triggers the converter. The end of conversion is detected by CB1.
*

0000 EC 02 SAMPLE LDD 2,X Get channel No. in last
0002 58 ASL B 4 bits. Multiplexer
0003 58 ASL B address lines are the

```
0004 58      ASL B    high 4 bits so
0005 58      ASL B    multiply by 16
0006 F7 1000  STA B ADCDAT Select channel
0009 B6 1002  LDA A ADCCNT

000C 84 37      AND A #$37 Turn S&H to
000E B7 1002  STA A ADCCNT hold.
0011 7C 1000  INC ADCDAT+1 Dummy write triggers
0014 7D 1002  SM1   TST ADCCNT+1 conversion
0017 2A FB      BPL SM1 Finished yet?
0019 B6 1002  LDA A ADCCNT
001C 8A 08      ORA A #8 Turn S&H to
001E B7 1002  STA A ADCCNT sample
0021 FC 1000  LDD ADCDAT Fetch data (12 bits)
0024 84 0F      AND A #%00000111 Mask off high 4 bits
0026 83 0800  SUB D #$800 0 volts = 1/2 F.S.
0029 43      COM A negate because converter
002A 50      NEG B uses negative logic
002B 26 01      BNE SM2
002D 4C      INC A
002E ED 02  SM2   STD 2,X Push result onto
0030 39      RTS     data stack and return.
```

*

*

*DELAY

*

*The first part of this routine waits for a previous delay
*to run out. If OVER-FLOWS is non-zero the interrupt service
*ought to be counting it down to zero. However, to avoid an
*infinite hold-up here, a check is made of the status of
*the CPU interrupt mask. Once the timer output compare flag
*has become set we can prepare the next delay.
*The delay value is 32 bits long, the high order word
*representing the number of complete cycles the counter must
*go through while the low order word is added to the previous
*target in the timer output compare register.
*If the addend is too small (<128) the software may not be
*finished by the time the target is reached. This results in
*a time jump of 2^{16} microseconds. If this is the case 128 is
*added and a correction flag is set. The flag is used in the
*interrupt service to subtract off the 128 when OVER-FLOWS
*reaches zero.
*If OVER-FLOWS is non-zero for this current delay the
*timer output compare interrupt is enabled.

*

```
0000 DC 84  DELAY  LDD OVFLWS Zero yet?
0002 27 05      BEQ DL3    If so don't wait
0004 07      TPA    Fetch CPU status bits
0005 85 10      BIT A #$10 Are interrupts masked?
0007 27 F7  DL2   BEQ DELAY If no then wait
0009 7B 40 08  DL3  TIM #$40 TIMCNT Test bit 6 of TIMCONT
000C 27 FB      BEQ DL3 Wait until flag is set
000E EC 02      LDD 2,X Get high order word
0010 08      INX    of delay
0011 08      INX
0012 DD 84      STD OVFLWS
0014 EC 02      LDD 2,X Get low order word
0016 08      INX    of delay
0017 08      INX
```

0018 7F 0091 CLR CORRFG+1 Reset correction flag
001B 4D TST A High byte zero?
001C 26 08 BNE DL4 If not delay is at least
001E 5D TST B 250 microseconds
001F 2B 05 BMI DL4 If low byte +ve. it

0021 CB 80 ADD B #128 is < 128 therefore + 128
0023 7C 0091 INC CORRFG and set correction flag
0026 D3 0B DL4 ADD D TIMOCR Set up new
0028 DD 0B STD TIMOCR target value
002A DC 84 LDD OVFLWS
002C 27 06 BEQ DLS If zero then skip
002E 96 08 LDA A TIMCNT
0030 8A 08 ORA A #8 Enable timer output
0032 97 08 STA A TIMCNT compare interrupt
0034 96 02 DLS LDA A PORT1 Turn off ADC mute
0036 84 FB AND A #\$FB that may have been
0038 97 02 STA A PORT1 left on by PING
003A 39 RTS

*
*
*PULSE
*-----
*
*PORT1 bits 0 and 1 drive the power amplifier through buffers;
*so to generate a push-pull drive one is initially turned-on
*and then they are toggled at intervals of 143 microseconds.
*During the pulse AGC is muted to prevent the receiver becoming
*deafened by the transmission. An additional time is allowed
*after the pulse when the signal is still decaying and the
*power amplifier reservoir capacitors are recharging. By
*adding 10 mSecs. to the timer target, saved at the start of
*PULSE, the total time taken for PULSE is independent of the
*actual pulse duration and any soft-ware jitter. But the pulse
*may not be much longer than 9 mSecs.
*

HLFCYC EQU \$82
PNGSTR EQU \$8C

0000 DC 0B PULSE LDD TIMOCR Save current target
0002 DD 8C STD PNGSTR
0004 EC 02 LDD 2,X Get half cycle count
0006 08 INX off stack
0007 08 INX
0008 D7 82 STA B HLFCYC
000A DC B4 PL1 LDD OVFLWS
000C 27 05 BEQ PL2 OVFLWS zero?
000E 07 TPA
000F 85 10 BIT A #\$10 Are interrupts enabled?
0011 27 F7 BEQ PL1
0013 7B 40 08 TIM #\$40 TIMCNT Wait until flag set
0016 27 FB BEQ PL2
0018 96 02 LDA A PORT1 Turn on one power
001A 8A 01 ORA A #1 transistor
001C 97 02 STA A PORT1
001E 7B 40 08 PL3 TIM #\$40 TIMCNT Wait until flag is set
0021 27 FB BEQ PL3 1st time it is still set
0023 CC 008F LDD #143 1/2 cycle of 3.5 kHz.
0026 D3 0B ADD D TIMOCR Set up new target
0028 DD 0B STD TIMOCR

```
002A 96 02      LDA A PORT1 Toggle power amplifier
002C 88 03      EOR A #3 to create push-pull drive
002E 8A 04      ORA A #4 Turn on AGC mute
0030 97 02      STA A PORT1
0032 7A 00B2    DEC HLFCYC Pulse finished yet?
0035 26 E7      BNE PL3

0037 96 02      LDA A PORT1 Yes
0039 84 FC      AND A #$FC Turn off both transistors
003B 97 02      STA A PORT1
003D CC 2710    LDD #10000 Add 10 mSecs. to target
0040 D3 8C      ADD D PNGSTR as it was at start of
0042 DD 0B      STD TIMOCR pulse
0044 39         RTS
```

*

*

*WAIT

*

*Assuming a delay is running, the flag SIGFLG is set at the
*beginning of this routine. If a signal interrupt occurs before
*the delay finishes the routine exits as the interrupt clears
*SIGFLG. Otherwise an exit occurs at the end of the time delay
*with SIGFLG still set.

*

```
0000 CC 0001  WAIT   LDD #1 Set flag initially
0003 FD 0086      STD SIGFLG
0006 7D 0087  WT1   TST SIGFLG+1 Has it been cleared
0009 27 0F          BEQ WT3     by interrupt service?
000B FC 0084      LDD OVFLWS
000E 27 05          BEQ WT2
0010 07
0011 85 10          BIT A #$10
0013 27 F1          BEQ WT1
0015 7B 40 08 WT2   TIM #$40 TIMCNT Timer timed out?
0018 27 EC          BEQ WT1
001A 39          WT3   RTS
```

*

*

*DOWN?

*

*This procedure is called with an accelerometer value on the
*stack. Its purpose is to cause the water column sampling,
*PHASE1, to be aborted if either 10 samples of deceleration
*exceed a threshold or the optical switch interrupts and sets
*a flag MUDFLG. Should either happen a value is pushed onto the
*data stack to indicate which and the return stack pointer is
*incremented by 10. This alteration to the return stack throws
*away DOWN?'s return address and two sets of DO-LOOP control
*parameters to expose PHASE1's return address.

*

DWNCONT EQU \$88

```
0000 B6 1002  DOWN   LDA A ADCCNT Is optical switch interrupt
0003 85 10          BIT A #1 enable bit set?
0005 26 04          BNE DW1
0007 08
0008 08          INX No Drop value from
0009 20 2C          INX stack and return
                                BRA DW4
```

000B EC 02 DW1 LDD 2,X Remove value from stack
000D 08 INX
000E 08 INX
000F 7D 0080 TST MUDFLG Has optical switch
0012 26 13 BNE DW2 triggered and set MUDFLG?
0014 83 **** LDD #THSHLD No. Is value greater
0017 2D 1E BLT DW4 than threshold?

0019 7C 0088 INC DWNCNT Yes
001C 96 88 LDA A DWNCNT Have 10 values
001E 81 0A CMP A #10 exceeded threshold?
0020 2D 15 BLT DW4 If not return
0022 CC 0001 LDD #1 Yes 1=triggered by deceleration
0025 20 03 BRA DW3
0027 CC 0002 DW2 LDD #2 2=triggered by mud switch
002A ED 00 DW3 STD 0,X Push trigger code onto
002C 09 DEX the stack
002D 09 DEX
002E C6 0A LDA B #10
0030 DF F0 STX XTEMP Save data stack pointer
0032 30 TSX Copy return stack pointer into X
0033 3A ABX add 10 to it
0034 35 TXS and put it back
0035 DE F0 LDX XTEMP Recover data stack pointer
0037 39 RTS
*
*

APPENDIX A3 PATSY INDEX

The following is a listing of the procedures that during compiling are appended to the FORTH vocabulary and constitute the user program. In order that the compiled code can be placed in ROM variables that would normally contain their own data space instead have a field that points to RAM elsewhere. The pointer DATA keeps track of the allocation of RAM space to variables.

INDEX

30 (CHECKSUMS, ?B, U., CODE, DATA, RTI)
31 (CASE)
32 (CONSTANTS)
33 (DECLARING WORDS)
34 (UTILITIES)
35 (INTERRUPT SERVICE ROUTINES)
36 (DUMMY INTERRUPTS SERVICES, LINK, GETSET)
37 (VARIABLES, ARRAYS)
38 (CURRENT-TABLE, TABLE?, READ-TABLE)
39 (TABLE-ENTRY, READ-LIST, SCALE, SORT)
40 (CHECK, RELATIVES)
41 (LIST1)
42 (LIST2)
43 (LIST3)
44 (SAMPLE, DELAY)
45 (PULSE, WAIT, DOWN?)
46 (PREPARE1/2/3, P15?, PING, WATER?, TRANSMIT, SYNC.)
47 (RESET, BACKUP)
48 (PHASE1A)
49 (PHASE1B)
50 (PHASE2)
51 (SAMPLE-NOW, MARK)
52 (DATA TRANSMISSION BY PINGING)
53 (TRANSPOND)
54 (PARAMETERS)
55 (FILL-TABLE, SETUP)
56 (JRC)
57 (MARION DUFRESNE)
58
59
60 (SATDATA TEST)

SCR # 3

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

SCR # 4

0 (ERROR MESSAGES)
1 Empty stack
2 Dictionary full
3 Has incorrect address mode
4 Isn't unique
5
6 Bubble memory range?
7 Full stack
8 Bubble memory error
9
10
11
12
13
14
15 FORTH INTEREST GROUP

SCR # 5
0 (ERROR MESSAGES ...)
1 Compilation only, use in definition
2 Execution only
3 Conditionals not paired
4 Definition not finished
5 In protected dictionary
6 Use only when loading
7 Off current editing screen
8 Declare vocabulary
9
10
11
12
13
14
15

FORTH INTEREST GROUP

```
SCR # 30
0 ( CHECKSUMS, ?B, U., CODE, DATA, RTI )
1 : PATSY ; HEX
2 : CHECKSUMS HEX 0 1 CR BEGIN 2000 0 DO DUP I E000 + AND
3   IF SWAP I E000 + C9 + SWAP
4   THEN LOOP DUP 0 D. SWAP 0 D. 0 SWAP CR DUP + DUP 0=
5   UNTIL DROP DROP ;
6 : BINARY 2 BASE ! ;
7 : OCTAL 8 BASE ! ;
8 : ?B BASE 9 DUP DECIMAL . BASE ! ;
9 : U. O D. ;
10 : CODE ?PEXEC !CSP CURRENT @ CONTEXT ! CREATE HEX ;
11 O USER DATA 4800 DATA !
12 : RETURN ?CSP 39 C, SMUDGE ;
13 : RTI ?CSP 3B C, SMUDGE [COMPILE] [ ; IMMEDIATE
14
15 -->
```

```
SCR # 31
0 ( CASE )
1 : CASE    ?COMP CSP @ !CSP 4 ; IMMEDIATE
2 : OF      4 ?PAIRS COMPILE OVER COMPILE =
3   [COMPILE] IF 5 ; IMMEDIATE
4 : ENDOF   5 ?PAIRS [COMPILE] ELSE 4 ; IMMEDIATE
5
6 : ENDCASE 4 ?PAIRS
7   BEGIN SP@ CSP @ = 0=
8   WHILE 2 [COMPILE] THEN
9     REPEAT CSP ! COMPILE DROP ; IMMEDIATE
10
11
12
13
14
15 -->
```

```
SCR # 32
0 ( CONSTANTS )
1 HEX 1000 CONSTANT ADCDAT 1002 CONSTANT ADCCONT
2 O CONSTANT PORT1DIR 2 CONSTANT PORT1
3 8 CONSTANT TIMCONT 9 CONSTANT COUNTER
4 B CONSTANT TIMOCR D CONSTANT TIMICR
5 80 CONSTANT MUDFLAG 82 CONSTANT HLFCYC
6 84 CONSTANT OVER-FLOWS 86 CONSTANT SIGFLAG
7 88 CONSTANT DOWN-COUNT 8A CONSTANT CYCLES
8 BC CONSTANT PNGSTR BE CONSTANT TIME-ERROR
9 266 CONSTANT THRESHOLD 90 CONSTANT CORRFG
10
11
12
13
14
15 -->
```

SCR # 33

```
0 ( DECLARING WORDS )
1 : VAR <BUILD$ DATA @ DUP , ! 2 DATA +! DOES> @ ;
2 : ROLLING-BUFFER <BUILD$ 2 * DATA @ DUP , DUP 2+
3     SWAP ! DATA @ + DUP , 2+ DATA ! ;CODE
4     DFF0 , 383C , EEO3 , ECOO , DDE0 , C3 C, 2 ,
5     EDO0 , 38 C, A305 , 2309 , ECO3 , EEO3 , C3 C,
6     2 , EDO0 , DEFO , DCEO , EDO0 , 0909 , RETURN
7 : ARRAY+ <BUILD$ 2 * DATA @ DUP , DUP 2+ SWAP !
8     DATA @ + DUP , 2+ DATA ! ;CODE
9     DFF0 , 383C , EEO3 , ECOO , DDE0 , C3 C, 2 ,
10    EDO0 , 38 C, A305 , 2306 , EC05 , EEO3 , EDO0 ,
11    DEFO , DCEO , EDO0 , 0909 , RETURN
12 : ARRAY <BUILD$ 2 * DATA @ , DATA +! DOES> @ ;
13 : CHANNEL-TABLE <BUILD$ DATA @ DUP , 30 ERASE
14     30 DATA +! DOES> @ ;
15 -->
```

SCR # 34

```
0 ( UTILITIES )
1 : I/O-INIT O PORT1 C! 4F PORT1DIR C! O PORT1 C!
2     O ADCCONT ! F000 ADCDAT ! 3C2C ADCCONT ! ;
3 : SUPPLIES-ON PORT1 C@ 8 OR PORT1 C! ;
4 : SUPPLIES-OFF PORT1 C@ F7 AND PORT1 C! ;
5 CODE ENABLE-INTERRUPTS E C, RETURN
6 CODE DISABLE-INTERRUPTS F C, RETURN
7 : ENABLE-OPTICAL-SWITCH ADCCONT C@ DROP ADCDAT C@ DROP
8     ADCCONT DUP C@ 1 OR SWAP C! ;
9 : DISABLE-OPTICAL-SWITCH ADCCONT DUP C@ 3E AND SWAP C!
10 : DISABLE-SIGNAL TIMCONT DUP DUP C@ SWAP 5 + C@ DROP
11     EF AND SWAP C! ;
12 : ENABLE-SIGNAL TIMCONT DUP DUP C@ SWAP 5 + C@ DROP
13     10 OR SWAP C! ;
14 : MSEC. 03E8 U* ;
15 -->
```

SCR # 35

```
0 ( INTERRUPT SERVICE ROUTINES )
1
2     ( TIMER )
3 CODE TISR DC C, TIMCONT C, DE C, OVER-FLOWS C, 2705 , 09 C,
4     DF C, OVER-FLOWS C, 2612 , 96 C, TIMCONT C, 84F7 , 97 C,
5     TIMCONT C, 7D C, CORRFG 1+ , 2707 , DC C, TIMOCR C, 83 C,
6     80 , 2002 , DC C, TIMOCR C, DD C, TIMOCR C, RTI
7
8     ( SIGNAL )
9 CODE SISR 96 C, TIMCONT C, D6 C, TIMICR C, 84EF , 97 C,
10    TIMCONT C, 4F5F , DD C, SIGFLAG C, RTI
11
12     ( MUD SENSOR )
13 CODE MSISR B6 C, ADCCONT , 2B04 , B6 C, ADCDAT , 2007 ,
14     B6 C, ADCDAT , 86FF , 97 C, MUDFLAG C, RTI
15 -->
```

```
SCR # 36
0 ( DUMMY INTERRUPTS SERVICES, LINK, GETSET )
1 CODE SERIAL 9611 , 85EB , 9711 , RTI
2
3 CODE TIMER-0' FLOW DC08 , 84FB , 9708 , RTI
4
5 : LINK 3 * DO + DUP 7E SWAP C! 1+ ! ;
6
7
8
9 : GETSET I/O-INIT 0 OVER-FLOWS ! O MUDFLAG ! O SIGFLAG !
10 O DOWN-COUNT ! ENABLE-INTERRUPTS SUPPLIES-ON ;
11
12
13
14
15 -->
```

```
SCR # 37
0 ( VARIABLES, ARRAYS )
1 CHANNEL-TABLE TABLE1 CHANNEL-TABLE TABLE2
2 CHANNEL-TABLE TABLE3 ? TABLE1 6 + VAR TABLE
3 DECIMAL
4 O VAR NO.1 O VAR NO.2 O VAR NO.3 O VAR NO.4
5 O VAR NO.5 O VAR NO.6 O VAR NO.7 O VAR NO.8 O VAR NO.9
6 O VAR ACELN1LIVE O VAR ACELN2LIVE O VAR TILT1LIVE
7 O VAR TILT2LIVE O VAR TEMPLIVE O VAR BACKBY
8 1250 ARRAY+ ACELN1FAST 1250 ARRAY+ ACELN2FAST
9 10 ARRAY PING-LIST O VAR SIGNAL
10 1600 ARRAY+ ACELN1 1600 ARRAY+ ACELN2
11 1600 ARRAY+ TILT1 1600 ARRAY+ TILT2
12 1600 ARRAY+ TEMP
13 4000 ROLLING-BUFFER ACELNRB1 4000 ROLLING-BUFFER ACELNRB2
14 ." Next free RAM location would be " HEX DATA @ U.
15 DECIMAL -->
```

```
SCR # 38
0 ( CURRENT-TABLE, TABLE?, READ-TABLE )
1 : CURRENT-TABLE CASE
2   1 OF ? TABLE1 6 + TABLE ! ENDOF
3   2 OF ? TABLE2 6 + TABLE ! ENDOF
4   3 OF ? TABLE3 6 + TABLE ! ENDOF
5   ENDCASE ;
6 : TABLE? TABLE @ CASE
7   ? TABLE1 6 + OF ." TABLE 1" ENDOF
8   ? TABLE2 6 + OF ." TABLE 2" ENDOF
9   ? TABLE3 6 + OF ." TABLE 3" ENDOF ENDCASE ;
10 : READ-TABLE CR TABLE? TABLE @ @ CR
11 ."           CHAN.   F.S. (MSEC.) F.S. (VALUE) OFFSET (MSEC.) " CR
12 8 O DO I O 12 D.R DUP I 6 * + @ S->D 12 D.R
13           DUP I 6 * + 2+ @ S->D 12 D.R
14           DUP I 6 * + 4 + @ S->D 12 D.R
15 CR LOOP DROP ; -->
```

SCR # 39
0 (TABLE-ENTRY, READ-LIST, SCALE, SORT)
1 : TABLE-ENTRY >R ROT R> SWAP TABLE @ @ SWAP 8 MOD DUP 0<
2 IF B +
3 THEN 6 * + 4 + DUP >R ! R 2 - ! R> 4 - ! READ-TABLE ;
4 : READ-LIST Z2 2 DO PING-LIST I + @ . 2 +LOOP ;
5
6 : SCALE 6 * TABLE @ @ + DUP @ 0=
7 IF DROP DROP 0
8 ELSE DUP >R DUP @ SWAP 2+ @ */JR @ MOD R> 4 + @ +
9 THEN ;
10
11 CODE SORT 3C C, 8601 , 3A C, CE C, PING-LIST 2+ , EC00 , A302 ,
12 2F13 , A600 , E602 , A702 , E700 , A601 , E603 , A703 ,
13 E701 , 32 C, 4F C, 36 C, 0808 , 8C C, PING-LIST 10 + ,
14 26E0 , 32 C, 4D C, 27D6 , 3B C, RETURN
15 -->

SCR # 40
0 (CHECK, RELATIVES)
1 CODE CHECK 3C C, CE C, PING-LIST , 4F5F , ED12 , ED14 , 8608 ,
2 36 C, CE C, PING-LIST , EC02 , 83 C, 14 , 2A10 , EC04 ,
3 ED02 , 0808 , 8C C, PING-LIST 10 + , 26F5 , 32 C, 4A C, 36 C,
4 26E6 , 32 C, CE C, PING-LIST , EC02 , 2607 , CC C, 762 ,
5 ED02 , 2011 , 83 C, 74E , 2505 , CC C, 74E , ED02 , 0808 ,
6 8C C, PING-LIST 12 + , 26E4 , CE C, PING-LIST , EC04 , 271F ,
7 A302 , 83 C, 13 , 2A11 , 3C C, EC04 , ED02 , 2707 , 0808 ,
8 8C C, PING-LIST 12 + , 26F3 , 38 C, 20E4 , 0808 , 8C C,
9 PING-LIST 10 + , 26DD , 38 C, RETURN
10 : RELATIVES 0 10 DO PING-LIST I + 2+ @ DUP
11 IF PING-LIST I + @ - A - PING-LIST I + 2+ !
12 ELSE DROP
13 ENDIF -2 +LOOP ;
14
15 DECIMAL -->

SCR # 41
0 (LIST1)
1 : LIST1 SIGNAL @ 0 SCALE PING-LIST 2+ !
2 ACELN1FAST @ 1 SCALE PING-LIST 4 + !
3 ACELN2FAST @ 2 SCALE PING-LIST 6 + !
4 O PING-LIST 8 + !
5 O PING-LIST 10 + !
6 O PING-LIST 12 + !
7 O PING-LIST 14 + !
8 O PING-LIST 16 + ! ;
9
10
11
12
13
14
15 DECIMAL -->

SCR # 42

```
0 ( LIST2 )
1 : LIST2 SIGNAL @ 0 SCALE PING-LIST 2+ !
2     ACELN1 @ 1 SCALE PING-LIST 4 + !
3     ACELN2 @ 2 SCALE PING-LIST 6 + !
4     TILT1 @ 3 SCALE PING-LIST 8 + !
5     TILT2 @ 4 SCALE PING-LIST 10 + !
6     TEMP @ 6 SCALE PING-LIST 12 + !
7     O PING-LIST 14 + !
8     O PING-LIST 16 + ! ;
9
10
11
12
13
14
15 -->
```

SCR # 43

```
0 ( LIST3 )
1 : LIST3 SIGNAL @ 0 SCALE PING-LIST 2+ !
2     ACELN1LIVE @ 1 SCALE PING-LIST 4 + !
3     ACELN2LIVE @ 2 SCALE PING-LIST 6 + !
4     TILT1LIVE @ 3 SCALE PING-LIST 8 + !
5     TILT2LIVE @ 4 SCALE PING-LIST 10 + !
6     TEMPLIVE @ 6 SCALE PING-LIST 12 + !
7     O PING-LIST 14 + !
8     O PING-LIST 16 + ! ;
9
10
11
12
13
14
15 -->
```

SCR # 44

```
0 ( SAMPLE, DELAY )
1 CODE SAMPLE EC02 , 5858 , 5858 , F7 C, ADCDAT , B6 C,
2     ADCCONT , 8437 , B7 C, ADCCONT , 7C C, ADCDAT 1+ ,
3     7D C, ADCCONT 1+ , 2AFB , B6 C, ADCCONT , 8A08 ,
4     B7 C, ADCCONT , FC C, ADCDAT , 840F , 83 C, 800 ,
5     4350 , 2601 , 4C C, ED02 , RETURN
6
7 CODE DELAY DC C, OVER-FLOWS C, 2705 , 07 C, 8510 , 27F7 ,
8     7B40 , TIMCONT C, 27FB , EC02 , 0808 , DD C, OVER-FLOWS C,
9     EC02 , 0808 , 7F C, CORRFG 1+ , 4D C, 2608 , 5D C, 2B05 ,
10    CB80 , 7C C, CORRFG 1+ , D3 C, TIMOCR C, DD C, TIMOCR C,
11    DC C, OVER-FLOWS C, 2706 , 96 C, TIMCONT C, 8A08 , 97 C,
12    TIMCONT C, 96 C, PORT1 C, 84FB , 97 C, PORT1 C, RETURN
13
14
15 -->
```

SCR # 45

```
0 ( PULSE, WAIT, DOWN? )
1 CODE PULSE DCOB , DD8C , EC02 , 0808 , D782 , DC84 ,
2 2705 , 07 C, 8510 , 27F7 , 7B40 , TIMCONT C, 27FB ,
3 96 C, PORT1 C, 8A01 , 97 C, PORT1 C, 7B40 , TIMCONT C,
4 27FB , CC C, 8F , D3 C, TIMOCR C, DD C, TIMOCR C, 96 C,
5 PORT1 C, 8803 , 8A04 , 97 C, PORT1 C, 7A C, HLFNCYC ,
6 26E7 , 96 C, PORT1 C, 84FC , 97 C, PORT1 C, CC C,
7 2710 , D3 C, PNGSTR C, DD C, TIMOCR C, RETURN
8 CODE WAIT CC C, 1 , FD C, SIGFLAG-, 7D C, SIGFLAG 1+ ,
9 270F , FC C, OVER-FLOWS , 2705 , 07 C, 8510 ,
10 27F1 , 7B40 , TIMCONT C, 27EC , RETURN
11 CODE DOWN? B6 C, ADCCONT , 8501 , 2604 , 0808 , 202C ,
12 EC02 , 0808 , 7D C, MUDFLAG , 2613 , 83 C, THRESHOLD ,
13 2D1E , 7C C, DOWN-COUNT , 96 C, DOWN-COUNT C, 810A ,
14 2D15 , CC C, 1 , 2003 , CC C, 2 , EDOO , 0909 , C60A ,
15 DFF0 , 30 C, 3A35 , DEFO , RETURN DECIMAL -->
```

SCR # 46

```
0 ( PREPARE1/2/3, P15?, PING, WATER?, TRANSMIT, SYNC. )
1 : PREPARE1 LIST1 SORT CHECK RELATIVES ;
2 : PREPARE2 LIST2 SORT CHECK RELATIVES ;
3 : PREPARE3 LIST3 SORT CHECK RELATIVES ;
4 : P15? PORT1 C@ 32 AND ;
5 : PING 35 PULSE ;
6 : WATER? BEGIN PING 100 O DO 100 MSEC. DELAY
7   P15? IF LEAVE THEN LOOP P15? UNTIL ;
8 : TRANSMIT 18 O DO PING-LIST 2+ I + @ -DUP
9   IF PING MSEC. DELAY
10  ELSE LEAVE ENDIF 2 +LOOP ;
11 : SYNC. TIMICR @ 10000 + TIMCONT C@ 247 AND TIMCONT C!
12   TIMOCR ! O OVER-FLOWS ! O 10 O DO O SAMPLE DUP
13   SIGNAL ! OVER > IF DROP SIGNAL @
14   ELSE COUNTER @ 8600 + TIMOCR ! LEAVE THEN LOOP ;
15 -->
```

SCR # 47

```
0 ( RESET, BACKUP )
1 : RESET 6 + @ DUP 2+ SWAP ! ;
2 : BACKUP 2 * SWAP 6 + DUP >R @ @ SWAP - DUP R @ - DUP O >
3   IF DROP
4   ELSE SWAP DROP R 2+ @ +
5   ENDIF R> @ ! #
6 : TRANSFER ' ACELN1FAST RESET ' ACELN2FAST RESET
7   ' ACELNRB1 BACKBY @ BACKUP ' ACELNRB2 BACKBY @ BACKUP
8   1250 O DO ACELNRB1 @ ACELN1FAST !
9   ACELNRB2 @ ACELN2FAST ! LOOP
10  ' ACELN1FAST RESET ' ACELN2FAST RESET ;
11 : CLEAR ' ACELN1 RESET ' ACELN2 RESET ' TILT1 RESET
12   ' TILT2 RESET ' TEMP RESET ;
13
14
15 -->
```

```
SCR # 48
0 ( PHASE1A )
1 DECIMAL
2 : PHASE1A 600 0 DO
3   50 MSEC. DELAY
4   1 SAMPLE ACELN1 !
5   2 SAMPLE ACELN2 !
6   3 SAMPLE TILT1 !
7   4 SAMPLE TILT2 !
8   6 SAMPLE TEMP !
9   50 MSEC. DELAY
10          LOOP
11  ENABLE-OPTICAL-SWITCH ;
12
13
14
15 -->
```

```
SCR # 49
0 ( PHASE1B )
1 DECIMAL
2 : PHASE1B 0 DO
3   24 0 DO 2 MSEC. DELAY 1 SAMPLE DUP ACELNRB1 ! DOWN?
4                           2 SAMPLE DUP ACELNRB2 ! DOWN?
5          LOOP
6   4 MSEC. DELAY 1 SAMPLE DUP ACELN1 ! ACELNRB1 !
7   2 SAMPLE DUP ACELN2 ! ACELNRB2 !
8   3 SAMPLE TILT1 !
9   4 SAMPLE TILT2 !
10  1 SAMPLE ACELNRB1 ! 2 SAMPLE ACELNRB2 ! 6 SAMPLE TEMP !
11  24 0 DO 2 MSEC. DELAY 1 SAMPLE DUP ACELNRB1 ! DOWN?
12                           2 SAMPLE DUP ACELNRB2 ! DOWN?
13  LOOP LOOP 0 ;
14
15 -->
```

```
SCR # 50
0 ( PHASE2 )
1
2 : PHASE2 0 DO
3   48 0 DO 2 MSEC. DELAY 1 SAMPLE ACELNRB1 !
4                           2 SAMPLE ACELNRB2 !
5          LOOP
6   4 MSEC. DELAY 1 SAMPLE DUP ACELN1 ! ACELNRB1 !
7   2 SAMPLE DUP ACELN2 ! ACELNRB2 !
8   3 SAMPLE TILT1 !
9   4 SAMPLE TILT2 !
10  1 SAMPLE ACELNRB1 !
11  2 SAMPLE ACELNRB2 !
12  6 SAMPLE TEMP !           LOOP
13  DISABLE-OPTICAL-SWITCH ;
14
15 -->
```

```
SCR # 51
0 ( SAMPLE-NOW, MARK )
1 : SAMPLE-NOW O SIGNAL !
2   1 SAMPLE ACELN1LIVE ! 2 SAMPLE ACELN2LIVE !
3   3 SAMPLE TILT1LIVE ! 4 SAMPLE TILT2LIVE !
4   6 SAMPLE TEMPLIVE ! ;
5
6 : MARK 2 = IF ' ACELNRB1 1000 BACKUP ' ACELNRB2 1000 BACKUP
7   5 O DO 51 ACELNRB1 +! LOOP
8   ' ACELNRB1 5 BACKUP 250 BACKBY..!
9   ELSE 1250 BACKBY ! THEN ;
10
11 : PREPARE4 SIGNAL @ DUP O<
12   IF O ELSE 8 / THEN 20 + PING-LIST 2+ !
13   22 4 DO O PING-LIST I + ! 2 +LOOP
14   SORT CHECK RELATIVES ;
15 -->
```

```
SCR # 52
0 ( DATA TRANSMISSION BY PINGING )
1 : FAST-DATA-PINGING ' ACELN1FAST RESET ' ACELN2FAST RESET
2   PREPARE1 O DO TRANSMIT TIME-ERROR @ 34464 + 1
3   DELAY PREPARE1 LOOP ;
4
5 : MEDIUM-DATA-PINGING CLEAR PREPARE2 O DO
6   TRANSMIT TIME-ERROR @ 34464 + 1 DELAY PREPARE2
7   LOOP ;
8
9 : LIVE-PINGING SAMPLE-NOW PREPARE3 O DO
10  TRANSMIT TIME-ERROR @ 34464 + 1 DELAY SAMPLE-NOW
11  PREPARE3 LOOP ;
12
13 : READY? BEGIN PING O 600 O DO DROP O 300 O DO DROP
14  100 MSEC. DELAY P15? IF O LEAVE ELSE 1 THEN LOOP
15  IF 1 LEAVE ELSE O THEN LOOP UNTIL ; -->
```

```
SCR # 53
0 ( TRANSPOND )
1 : TRANSPOND PREPARE4 O 1 ROT ROT DO O=
2   IF SYNC. TRANSMIT PREPARE4 80 MSEC. DELAY 20 MSEC.
3   ELSE 10 MSEC. DELAY DISABLE-SIGNAL PING 980 MSEC.
4   DELAY 1000 MSEC.
5   THEN DELAY ENABLE-SIGNAL WAIT SIGFLAG @
6   LOOP DROP ;
7
8 : SKIPLINE 2000 MSEC. DELAY ;
9
10 : ANNOUNCE 5 O DO PING 90 MSEC. DELAY LOOP ;
```

SCR # 54

```
0 ( PARAMETERS )
1 HERE 0 , 0 , 0 , 2000 , 2048 , 100 , 2000 , 2048 , 200 ,
2 0 , 0 , 0 , 0 , 0 , 0 , 0 , 0 , 0 , 0 , 0 , 0 ,
3 0 , 0 , 0 , 2000 , 2048 , 100 , 2000 , 2048 , 200 ,
4 900 , 614 , 1000 , 900 , 614 , 1100 , 0 , 0 , 0 ,
5 750 , 1229 , 1250 , 0 , 0 , 0 ,
6 0 , 0 , 0 , 2000 , 2048 , 100 , 2000 , 2048 , 200 ,
7 900 , 614 , 1000 , 900 , 614 , 1100 , 0 , 0 , 0 ,
8 750 , 1229 , 1250 , 0 , 0 , 0 ,
9 360 , 32000 , 20 , 150 , 150 , 1250 , 1600 , 900 , 150 , 1250 ,
10 CONSTANT PARAMETERS .
11
12
13
14
15 -->
```

SCR # 55

```
0 ( FILL-TABLE, SETUP )
1 : FILL-TABLE DO PARAMETERS I 2 * + @ TABLE @ @ I 24
2   MOD 2 * + ! LOOP ;
3 : SETUP 18432 DUP 56000 SWAP - ERASE
4   1 CURRENT-TABLE 24 0 FILL-TABLE READ-TABLE
5   2 CURRENT-TABLE 48 24 FILL-TABLE READ-TABLE
6   3 CURRENT-TABLE 72 48 FILL-TABLE READ-TABLE
7 CR PARAMETERS 144 + DUP @ ." TIME-ERROR = " DUP . TIME-ERROR !
8 CR 2 + DUP @ ." NO.1 = " DUP U. NO.1 ! CR 2 + DUP @
9 ." NO.2 = " DUP . NO.2 ! CR 2 + DUP @ ." NO.3 = " DUP . NO.3 !
10 CR 2 + DUP @ ." NO.4 = " DUP . NO.4 ! CR 2 + DUP @
11 ." NO.5 = " DUP . NO.5 ! CR 2 + DUP @ ." NO.6 = " DUP .
12 NO.6 ! CR 2 + DUP @ ." NO.7 = " DUP . NO.7 ! CR 2 + DUP @
13 ." NO.8 = " DUP . NO.8 ! CR 2 + @ ." NO.9 = " DUP . NO.9 !
14 CR GETSET ;
15 -->
```

SCR # 56

```
0 ( JRC )
1 : JRC ? ACELN1FAST RESET 0 DO PING 40 MSEC. DELAY
2   PING 90 MSEC. DELAY PING 190 MSEC. DELAY
3   PING 240 MSEC. DELAY
4   ACELN1FAST @ DUP 63 AND 10 * DUP 1+ MSEC. DELAY PING
5   679 SWAP - MSEC. DELAY
6   4032 AND 10 64 */ DUP 1+ MSEC. DELAY PING
7   679 SWAP - MSEC. DELAY 20000 TIME-ERROR @ + 0 DELAY
8   LOOP ;
9
10
11
12
13
14
15 -->
```

SCR # 57
0 (MARION DUFRESNE)
1 : TRIAL1 ? SERIAL 0 LINK ? TIMER-O'FLOW 1 LINK
2 ? TISR 2 LINK ? SISR 3 LINK ? MSISR 4 LINK
3 DISABLE-OPTICAL-SWITCH READY? WATER? ANNOUNCE
4 CLEAR ? ACELNRB1 RESET ? ACELNRB2 RESET
5 PHASE1A NO.1 @ PHASE1B
6 NO.2 @ PHASE2 MARK TRANSFER 3 CURRENT-TABLE
7 NO.3 @ LIVE-PINGING
8 NO.4 @ TRANSPOND SKIPLINE
9 BEGIN 1 CURRENT-TABLE
10 NO.5 @ FAST-DATA-PINGING SKIPLINE 2 CURRENT-TABLE
11 NO.6 @ MEDIUM-DATA-PINGING SKIPLINE
12 NO.7 @ TRANSPOND SKIPLINE
13 NO.8 @ LIVE-PINGING SKIPLINE
14 NO.9 @ JRC SKIPLINE
15 AGAIN ;

SCR # 58

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

SCR # 59

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

VOCABULARY

PATSY

TRIAL1 JRC SETUP FILL-TABLE* PARAMETERS SKIPLINE TRANSPOUND
READY? LIVE-PINGING MEDIUM-DATA-PINGING FAST-DATA-PINGING PREPARE4
MARK SAMPLE-NOW PHASE2 PHASE1B PHASE1A CLEAR TRANSFER BACKUP
RESET SYNC. TRANSMIT WATER? PING P15? PREPARE3 PREPARE2
PREPARE1 DOWN? WAIT PULSE DELAY SAMPLE LIST3 LIST2 LIST1
RELATIVES CHECK SORT SCALE READ-LIST TABLE-ENTRY READ-TABLE
TABLE? CURRENT-TABLE ACELNRB2 ACELNRB1 TEMP TILT2 TILT1
ACELN2 ACELN1 SIGNAL PING-LIST ACELN2FAST ACELN1FAST BACKBY
TEMPLIVE TILT2LIVE TILT1LIVE ACELN2LIVE ACELN1LIVE NO.9 NO.8
NO.7 NO.6 NO.5 NO.4 NO.3 NO.2 NO.1 TABLE TABLE3 TABLE2
TABLE1 GETSET LINK TIMER-0'FLOW SERIAL MSISR SISR TISR
MSEC. ENABLE-SIGNAL DISABLE-SIGNAL DISABLE-OPTICAL-SWITCH ENABLE-OPTICAL
-SWITCH
DISABLE-INTERRUPTS ENABLE-INTERRUPTS SUPPLIES-OFF SUPPLIES-ON
I/O-INIT CHANNEL-TABLE ARRAY ARRAY+ ROLLING-BUFFER VAR CORRFG
THRESHOLD TIME-ERROR PNGSTR CYCLES DOWN-COUNT SIGFLAG OVER-FLOWS
HLFCYC MUDFLAG TIMICR TIMOCR COUNTER TIMCONT PORT1 PORT1DIR
ADCCONT ADCDAT ENDCASE ENDOF OF CASE RTI RETURN DATA
CODE U. ?B OCTAL BINARY CHECKSUMS PATSY TASK FORTH
NOOP LINK MON P. WHERE EDITOR LINE TEXT C/L M/ M*
+- D+- VLIST TRIAD INDEX LIST ? . D. D.R .R #S
SIGN #> <# SPACES WHILE ELSE IF REPEAT AGAIN END
UNTIL +LOOP LOOP -DO THEN ENDIF BEGIN BACK FORGET
R/W DRIVE DRB --> LOAD MESSAGE .LINE (LINE) BLOCK BUFFER
DR1 DRO EMPTY-BUFFERS UPDATE +BUF PREV USE DABS ABS
M/MOD */ */MOD MOD / /MOD * S->D COLD ABORT QUIT
(DEFINITIONS VOCABULARY IMMEDIATE INTERPRET DLITERAL LITERAL
[COMPILE] CREATE ID. ERROR (ABORT) -FIND NUMBER (NUMBER)
WORD PAD HOLD BLANKS ERASE FILL QUERY EXPECT ?STACK
. (" .") -TRAILING TYPE COUNT DOES> <BUILD ;CODE (;CODE)
DECIMAL HEX SMUDGE] [COMPILE ?LOADING ?CSP ?PAIRS
?EXEC ?COMP ?ERROR !CSP PFA NFA LFA LATEST TRAVERSE
-DUP MAX MIN SPACE ROT > < = - C, , ALLOT HERE
2+ 1+ COLUMNS HLD R# CSP FLD DPL BASE STATE CURRENT
CONTEXT OFFSET SCR OUT IN BLK VOC-LINK DP FENCE WARNING
WIDTH TIB RO SO +ORIGIN B/SCR B/BUF LIMIT FIRST BL
3 2 1 0 USER VARIABLE CONSTANT ; : C! ! C@ @
TOGGLE +! DUP SWAP DROP OVER DMINUS MINUS D+ + OK
0= R R> >R LEAVE ;S RP! SP! SP@ XOR OR AND U/
U* CMOVE CR ?TERMINAL KEY EMIT ENCLOSURE (FIND) DIGIT
I (DO) (+LOOP) (LOOP) OBRANCH EXECUTE CLITER LIT

EDITOR

C B. DELETE COPY FLUSH CLEAR TOP I P R L T M
D S E H -MOVE #LAG #LEAD #LOCATE TASK FORTH NOOP
LINK MON P. WHERE EDITOR LINE TEXT C/L M/ M* +-
D+- VLIST TRIAD INDEX LIST ? . D. D.R .R #S #
SIGN



APPENDIX A4 PATSY GLOSSARY

A.4 PATSY GLOSSARY

Many words in FORTH receive parameters from a data stack and may return some. The notation used here is :-

S:L < WORD >
 n1 n2 --- n3
 (Description of the function of the word)

n1 and n2 are 16 bit values on the stack before execution, the right-most being at the top of the stack.
--- denotes the function being performed and
n3 a value returned to the stack. eg.

13:9 + n1 n2 --- sum
 Return to the stack the sum n1+n2

S and L are respectively the screen and line numbers of the word in the index.

Other words created during compiling can later be executed to assist the compiler to build a control structure like CASE or to create new classes of word such as data types with a user defined format and run-time behaviour. The notation used is :-

12:11 < STRING >
 n < WORD > < STRING >
This creates a new FORTH word of name < STRING > and class
< WORD > using a parameter n. eg.

37:9 PING-LIST
 10 ARRAY PING-LIST
Creates a one dimensional array of 10 elements called PING-LIST with a call to the run-time code provided by the word ARRAY

Not all the words in the index are defined in the glossary as some are redundant and others speak for themselves.

30:1 PATSY

A dummy word to mark the start of the extension to the FORTH dictionary.

30:10 CODE

CODE < string >RETURN

Creates a machine code word of name < string > and sets the number base to hexadecimal. Double or single bytes may then be stored into the word using "," and "c,".

30:11 DATA

A FORTH variable containing a pointer to variable space in RAM. It is initialised to 4800 hex.

30:12 RETURN

Completes a code definition.

30:13 RTI

Completes either a high level or code word that is an interrupt service routine.

31:1 CASE,OF,ENDOF,ENDCASE

These words build a CASE structure when used during compiling. The form created will be :-

CASE value OF ... ENDOF
value OF ... ENDOF etc.
... ENDCASE

The words between OF and ENDOF are executed if the number on the stack at run-time is equal to value otherwise words preceding ENDCASE are executed.

33:1 VAR

n VAR < string >

Creates a variable of name < string > that points to a 16 bit location in RAM initialised to n. When < string > is executed the address of that RAM location is pushed onto the stack.

33:2 ROLLING-BUFFER

n ROLLING-BUFFER < string >

Creates a one dimensional array, < string >, of n elements. Each time an array of this type is executed the address of the next element is returned until the end of the array is passed when the address of the first element is pushed onto the stack.

33:7 ARRAY+

n ARRAY+ < string >

Creates an array like ROLLING-BUFFER except that when the last element is reached this one's address is repeated for any further calls. ie the array saturates.

33:12 ARRAY

n ARRAY < string >

Creates a one dimensional array of name < string > which at run-time returns the address of the first element (less 2 for technical reasons).

33:13 CHANNEL-TABLE

CHANNEL-TABLE < string >

Builds an 8 by 3 array to hold scaling parameters for
8 data channels.

34:1 I/O-INIT

This word initialises the CPU 8 bit port by defining which
lines are to be inputs or outputs and then programs the 16 bit
parallel port that interfaces to the analogue to digital
converter.

34:3 SUPPLIES-ON

34:4 SUPPLIES-OFF

These words control the supplies for external sensors.

34:5 ENABLE-INTERRUPTS

34:6 DISABLE-INTERRUPTS

All interrupts to the CPU can be masked or unmasked by
these words.

34:7 ENABLE-OPTICAL-SWITCH

34:9 DISABLE-OPTICAL-SWITCH

These words control interrupts from the optical switch.
The state of the switch can also be sensed via bit 5 of the
CPU port PORT1.

34:10 DISABLE-SIGNAL

34:12 ENABLE-SIGNAL

Interrupts from the receiver during transponding can be
inhibited or enabled by these words.

34:14 MSEC.

n --- ud

Multiplies the single precision number n by 1000 to
generate an unsigned double precision number ud. If n is in
mSec. then ud is in micro-seconds. eg.

10 MSEC. DELAY

35:3 TISR (Timer Interrupt Service Routine)

For delays longer than 2^{16} micro-seconds the number of
complete cycles of the counter is stored in OVER-FLOWS. This
interrupt service decrements OVER-FLOWS on successive
interrupts and on reaching zero it disables itself.
See notes for details of timer operation.

35:9 SISR (Signal Interrupt Service Routine)

When a receiver interrupt occurs this routine clears a
flag SIGFLAG and disables itself. SIGFLAG is sensed during
transponding.

35:12 MSISR (Mud Sensor Interrupt Service Routine)

If the optical switch makes a transition when enabled
to interrupt this routine checks that this is the source of
the interrupt and if it is sets the flag MUDFLAG which is
sampled regularly during PHASE1 of sampling.

36:1 SERIAL

Should an interrupt ever be generated by the serial interface it will be vectored here to disable the interrupt.

36:3 TIMER-0'FLOW

This interrupt like SERIAL should never happen, but if it does it is disabled here.

36:5 LINK

add n ---

Interrupts vector through high addresses in the ROM containing the language; to avoid having to reprogram this ROM every time a service routine is relocated, the vectors point to a table of jumps in RAM. When FORTH starts up from cold the jump table is filled in with default addresses. LINK must be used to overwrite these addresses with the addresses of the service routines. n is the jump number.

n interrupt service routine

0 SERIAL

1 TIMER-0'FLOW

2 TISR

3 SISR

4 MSISR

Used thus : SERIAL 0 LINK

36:9 GETSET

This initialises ports, clears some flags, enables interrupts and turns on the supplies for the sensors.

37:1 TABLE1, TABLE2

37:2 TABLE3

Three arrays of type CHANNEL-TABLE are declared.

37:2 TABLE

This variable is declared and initialised to point into TABLE1

37... The remainder of the program variables and arrays are declared.

38:1 CURRENT-TABLE

n ---

The value of n can be 1,2 or 3 . The variable TABLE is filled with the address of the corresponding table. If n is out of range no change is made.

38:6 TABLE?

--- "string"

Prints the name of the table currently pointed to by TABLE.

38:10 READ-TABLE

The parameters in the current table are displayed in a tabulated form.

39:1 TABLE-ENTRY

n1 n2 n3 n4 ---

Parameters n2,n3 and n4 are filled into channel n1 of the current table. n1 is treated modulo 8 so no damage can be done if n1 is not in the range 0 to 7. The modified contents of the table are then displayed using READ-TABLE.

39:4 READ-LIST

This word prints out the values in the PING-LIST. See notes for the function of the PING-LIST

39:6 SCALE

n1 n2 --- n3

The sensor value n1 is scaled according to the parameters of channel n2 of the current table. n3 is the scaled result. See notes for further imformation about scaling.

39:11 SORT

This word takes the PING-LIST and rearranges its contents into ascending numerical order.

40:1 CHECK

Like SORT this word processes the PING-LIST - It eliminates possible negative delays, delays that are too long or pairs of delays that are too close. At present it is biassed towards dropping the later of two delays less than 20 msec. apart.

40:10 RELATIVES

This word converts a list of delays from zero in the PING-LIST into a list of delay differences. See notes for the details of PING-LIST editing.

41:1 LIST1

42:1 LIST2

43:1 LIST3

These LIST words read the next samples from selected arrays, SCALEs them and enters them into the PING-LIST. The order in which the sensors are read is irrelevant as the PING-LIST will be SORTed later.

44:1 SAMPLE

n1 --- n2

This is the procedure that samples analogue channel n1 and delivers a signed value n2 between -2047 and +2048. First the channel number is fed to the multiplexer then the sample-and-hold chip is switched to hold and a conversion triggered. At the end of conversion the sample-and-hold chip is returned to the sampling state and the output from the analogue to digital converter is inverted (negative logic is used) and adjusted to represent a 2's complement number.

44:7 DELAY

ud ---

This word is the heart of the pulse interval telemetry. The unsigned double precision number ud is split into a high and a low word. The low word is added into the 16 bit counter to produce a delay of that number of micro-seconds. If the high byte is non-zero then it represents the number of complete cycles of count that must be executed before the counter reaches its target and the delay is finished. The high order word is stored in OVER-FLOWS and the timer interrupt is enabled. Each time the target count is reached an interrupt occurs and OVER-FLOWS is decremented.

A crucial aspect of DELAY is that it does not waste "ud" micro-seconds instead it waits for any previous delay to time-out then sets up the new delay and returns. See notes for a more detailed explanation of the use of the timer.

45:1 PULSE

n ---

Generate a transmission pulse of n half-cycles. This word waits for any current delay to time out, saves the state of the count for later and turns on the AGC mute. This will be turned off again by the following DELAY and prevents the receiver gain being affected by the pulse. The power transistors are toggled on and off "n" times to generate the pulse. Before returning the count saved at the start has 10 mSec. added to it so that the whole word takes 10 mSec. to run regardless of the actual time taken to execute the soft-ware. This coherent timing principle is described in more detail later.

45:8 WAIT

This word is used during transponding and waits for a signal interrupt with a delay running. A return occurs either when the interrupt has occurred and cleared SIGFLAG or because the time has run out in which case SIGFLAG will still be set.

45:11 DOWN?

n1 --- (n2)

This word is called regularly after each fast sampling of an accelerometer. n1 is a sampled value but if the optical switch is not yet enabled it is dropped and DOWN? returns. If an optical switch interrupt has occurred MUDFLAG will be set and n2 is set to 2. Otherwise the value of n1 is compared with a threshold and after 10 values have exceeded it n2 is set to 1. With n2 either 1 or 2 DOWN? performs an exceptional return by exiting 2 levels of DO LOOP. Should these loops exit in the normal way then a value of zero is left on the stack.

Thus 0 means bottom not detected within the time allowed.

1 means a significant deceleration has occurred.

2 means the optical switch has worked.

DOWN? will cause a crash if not called within a double DO LOOP!

46:1 PREPARE1
46:2 PREPARE2
46:3 PREPARE3

These words fetch, scale data and edit them into the PING-LIST

46:4 P15?

--- f

The state of the optical switch is read through port1 bit 5 and returned as f, a boolean flag.

46:5 PING

35 half-cycles = 5 mSec. at 3.5 kHz.

46:6 WATER?

The unblocked state of the optical switch is tested 10 times a second. As long as this state is false PINGS are generated every 10 seconds.

46:8 TRANSMIT

This word actually implements the pulse interval telemetry by reading a PING-LIST of delays. If a value is non-zero then a 5 mSec. PING is generated and a DELAY corresponding the value is started. If a zero value is read then TRANSMIT exits immediately. (At least one zero value at the end of the list is guaranteed).

46:11 SYNC.

It is neccessary to synchronise the timing of delays and pings with the arrival time of received signals. The narrow-band signal has a slow rise and if the time at which it passes the detector threshold is used there will be some jitter as the amplitude of the pulses vary. The detector pulse is sensed on a timer input line to generate an interrupt but at the same time the current state of the counter is captured. SYNC. provisionally uses this count to set up a delay of 10 mSec. and then starts sampling the signal through channel zero. It makes 10 attempts to find a peak and if it does it uses the time this occurs as a timing reference since it is essentially independent of the signal amplitude. If no peak is found then the timing defaults to 10 mSec. from detector transision.

The highest value of signal sampled is stored in the variable SIGNAL and can transponded back to the ship so that adjustments to the transmitted interrogation pulse can be made.

47:1 RESET

add ---

This word resets a ROLLING-BUFFER or auto-incrementing ARRAY+ given the run-time address of the array. Used thus :-
' TILT2 RESET

47:2 BACKUP

add n ---

Data is being continually sampled at 500 Hz. into ROLLING-BUFFERs from the instant of launch. When the mud is sensed sampling continues for a further fixed time (2 Sec. currently). In order to preserve some of the data sampled before landing the ROLLING-BUFFERs can be backed-up say 2.5 Sec.

"add" is the run time address of the particular ROLLING-BUFFER and "n" the positive number of samples to be backed-up. BACKUP is aware of the cyclic nature of the buffers. Used thus :-

* ACELNRB1 1250 BACKUP

47:6 TRANSFER

The ROLLING-BUFFERS consume much of the data storage space but only a portion of them contain interesting data. This portion is TRANSFERed to auto-incrementing arrays after being backed-up by the amount in BACKBY so that the data space can be reallocated to store slow-sampled data.

47:11 CLEAR

This word RESETS all the medium-sampled data arrays in one go.

49:2 PHASE1

n ---

This sampling procedure takes 1/10 Sec. to cycle through once. n is the number of cycles. Fast data is sampled every 2 mSecs. and every 100 mSecs. a complete set of medium data is also sampled. However, as this latter cannot be completed in 2 mSecs., 4 mSecs. is allowed with the fast data being sampled twice in this time.

DOWN? tests for the arrival at the sediment only if the optical switch is enabled to interrupt and this can be delayed say 1 minute into the descent to prevent false triggering during and immediately after launch.

50:2 PHASE2

n ---

This routine is similar to PHASE1 except that DOWN? is not called. However, having a separate routine allows the duration of post-trigger sampling to be chosen independently.

51:1 SAMPLE-NOW

This samples sensors into variables for immediate live transmission.

51:6 MARK

n ---

After PHASE1 and PHASE2 of sampling the number left on the stack indicates the way in which PHASE1 was exited. If this is 2, the optical switch triggered, MARK backs up through the accelerometer arrays to the trigger instant and adds a small offset to 5 samples of accelerometer 1.

51:11 PREPARE4

Only the received signal level is transmitted during transponding. PREPARE4 replaces negative values of SIGNAL by zero, scale the values down by 8 and provides an offset of 20 mSecs. This value is entered into the PING-LIST and the remaining values zeroed before the list is edited.

52:1 FAST-DATA-PINGING

n ---

This performs n 2 second cycles of data transmission from the fast sampled data arrays. TIME-ERROR contains a small number which adjusts the time of the whole loop to exactly 2 seconds by taking into account the initial tolerance of the crystal oscillator.

52:5 MEDIUM-DATA-PINGING

52:9 LIVE-PINGING

n ---

These do the same job as FAST-DATA-PINGING on medium and live data respectively.

52:13 READY?

This complicated and messy routine performs a simple function. PINGS are generated once per minute as long as the optical switch is unblocked. The state of the optical switch is tested every 1/10 Sec. and should it remain continuously blocked for 30 Secs. the routine exits.

53:1 TRANSPOND

n ---

This performs n 2 Second cycles of transponding. If SYNC. detects a pulse in a 10 mSec. window the a reference pulse followed by the signal data pulse are transmitted. There is a pause until the signal interrupt is enabled at the beginning of the next window. Should there be no pulse the reference pulse alone is transmitted indented by an additional 10 mSecs. and after 1 second the signal interrupt is enabled.

Thus if the pulse is missed a 1 second window is opened so there is a 50% chance of the transponder synchronising. If the interrogation pulse is outside this window the operator need only jump the phase of the 2 second pulses by one second by switching from edge to centre keying or vice versa.

54: PARAMETERS

--- n

HERE places the value of the current dictionary pointer on the stack and the interpreter precedes to execute the instructions to store successive 16 bit values into the dictionary. A constant is then declaring with the value left by HERE.

This table is used later by SETUP to fill the scaling tables with reasonable default values and initialise the cycle number variables NO.1 to NO.9.

55:1 FILL-TABLE

n1 n2 ---

This is a DO LOOP that fills 24 constants from the table of PARAMETERS into one of the scaling tables. n1 is the limit and n2 the initial value for the DO LOOP.

55:3 SETUP

SETUP first zeroes all the data space in RAM then uses FILL-TABLE to copy default values into the scaling tables. Other constants including a default value for TIME-ERROR are then copied into their respective variables. SETUP ends by executing GETSET so if no changes are to be made the main program can be run immediately.

56:1 JRC

n ---

This executes n 2 second cycles of transmission of the data from one accelerometer using a modified form of P.I.T.. To encode one 12 bit word into P.I.T. using a 2 Sec. repetition rate would require a time resolution of 2/4096 or about 1/2 mSec. but if the 12 bits is split into two channels of 6 bits each occupying a third of the time the minimum time to be resolved increases by 64/3 to say 10 mSec. and should thus be more easily decoded by an autonomous listening station for subsequent transmission by satelite to a ground station.

The sequence starts with four synchronising pulses spaced by the binary intervals 50, 100 and 200 mSec. If one or two of these pulses are missing it should be possible to reconstruct the timing as each possible pair of pulses has a unique time separation.

For each of the 2 six bit groups one pulse is generated in one of 64 ten mSec. cells.

APPENDIX A5 SOFTWARE NOTES

A5. NOTES

(1) TFORTH Conventional FORTH is a list processing language and has a kernel which interprets the high level words. This structure is an advantage to the language as the kernel only requires a primitive instruction set and can thus be implemented on a wide variety of computers. However, the imposition of the inner interpreter between every word executed has a time penalty.

The action of threading through nested words by the FORTH virtual machine is nearly equivalent to the way CPU would tackle nested subroutines. TFORTH has been developed to compile words as a series of 3 byte subroutine calls rather than as lists of 2 byte addresses and terminates them with a subroutine return instruction. The result is run-time code which takes slightly more memory but is quicker.

To the user the language behaves exactly like FORTH and retains all its other characteristics.

(2) THE TIMER The HD 6303 microprocessor has an internal 16 bit counter which is clocked continuously at 1 MHz. Associated with the counter are three registers:-

The input capture register that makes a copy of the current count when a transition occurs on the timer input line.

A register that freezes the count when accessed; the counter runs on though.

The output compare register which can be loaded with a target count such that when the counter matches this value a previously programmed 0 or 1 is output to the timer output pin (not used in this application), a flag is set and an interrupt may be generated.

By adding a new delay onto the previous target and making this the new target a series of contiguous time delays can be generated independent of the time taken by the software, provided delays are kept greater than about 40 microseconds.

To generate delays longer than 2 16 microseconds the target value is set up using the least significant 16 bits of the delay and an interrupt enabled. Each time the count passes the target an interrupt is generated and the high order part of the delay is decremented.

A problem might arise if, although the total delay is large (100s of msec), the least significant 16 bits is small. In this case the counter will have passed the target before the software has set it up so an extra full cycle will be added to the delay.

DELAY adds 128 to any residual that was less than 128 and sets a flag (CORRFG) which enables the interrupt service to knock 128 off the last cycle of count. With delays resolved to the nearest 1 msec the problem only occurred at one value of delay, 852 msec since this is equal to $13 * 2^{16} + 32$.

An important feature of DELAY is that it does not waste the specified delay instead it initially waits for any previous delay to be complete, sets up the new delay and then returns to allow additional software to executed while the delay is running.

(3) SCALING SCALE multiplies a signed 12 bit digitised value from a sensor by a/b and adds an offset c.

a = the full scale time delay
b = the full scale digitised value
c = some additional time delay in msec.

If, for example, an accelerometer generates +10 g full scale this is equivalent to +5 volts and +2048 when digitised. We require a display with 100 msec = 1 g therefore:-

a = $10 * 100 = 1000$
b = 2048

and c is chosen to displace 0 g away from the reference ping say by 100 msec. Before the offset is added the scaled value is reduced modulo a. This allows a smaller value of b to be used to magnify the display without the delay going outside the bounds of + or -a. If in

the above example b was chosen to be 1024, 1000 msec would now represent 5 g, i.e. 200 msec/g but 6 g would be displayed as 1 g, 7 g as 2 g, etc.

Small adjustments to a, b and c can be made to compensate for sensor gain or offset errors.

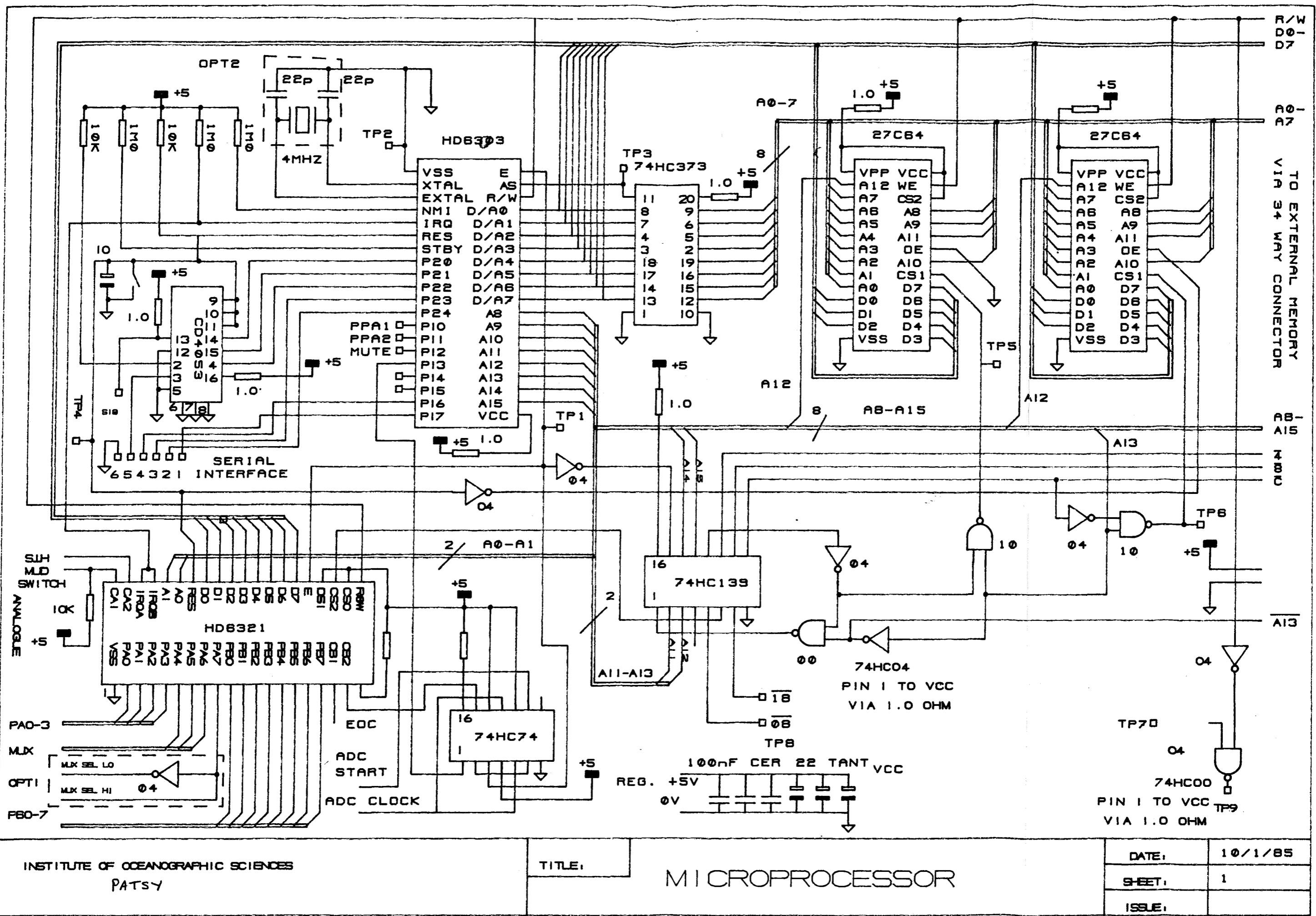
(4) PING-LIST EDITING The scaling process might generate unobtainable values of delay, say negative values or values greater than 2000 msec. The time delays originally entered into the PING-LIST would normally be in channel-number order and each represents a delay from zero. The word TRANSMIT requires a series of delays from the end of one PING to the beginning of the next.

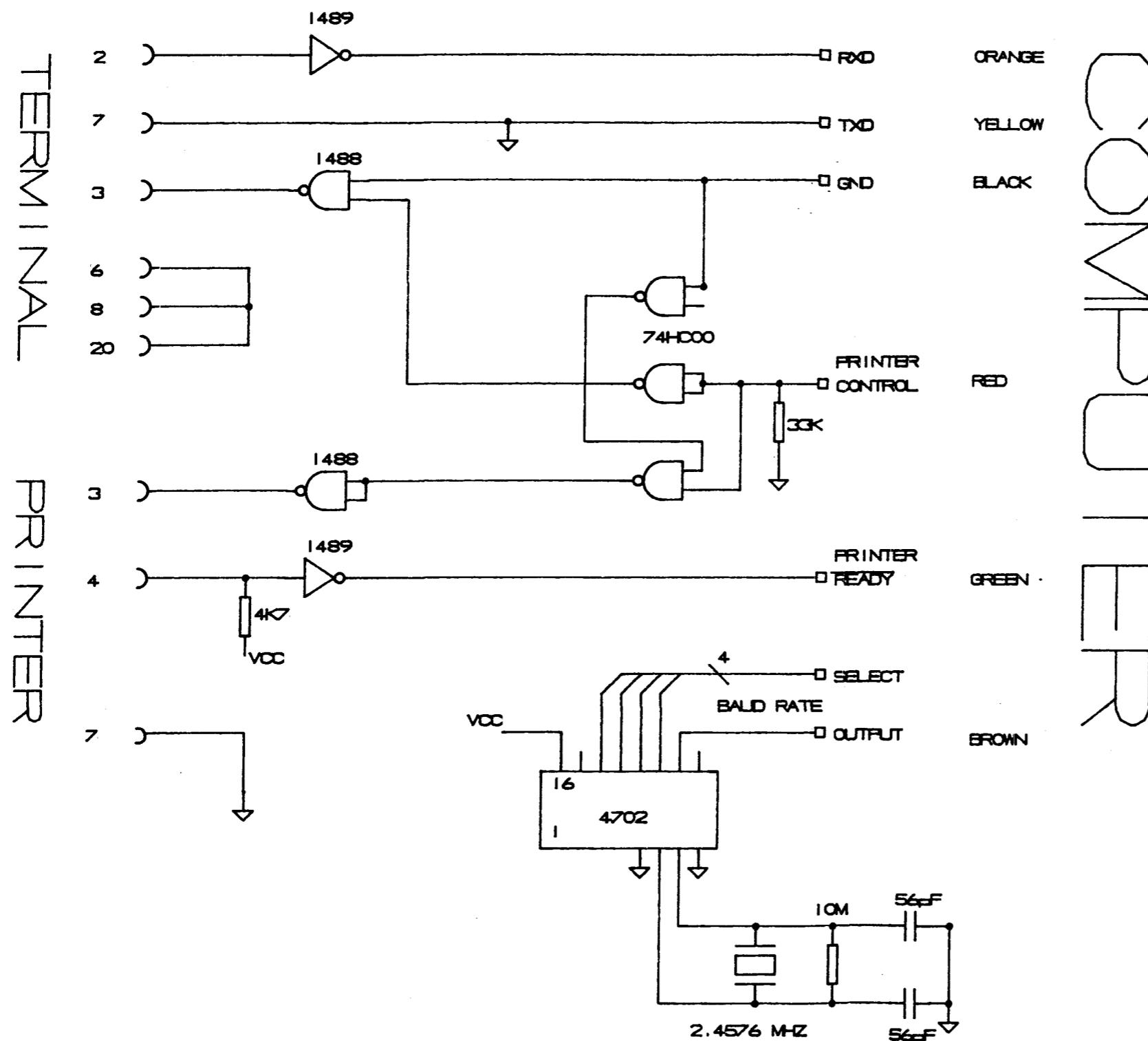
SORT puts the delays into ascending numerical order so that the successive differences are all positive.

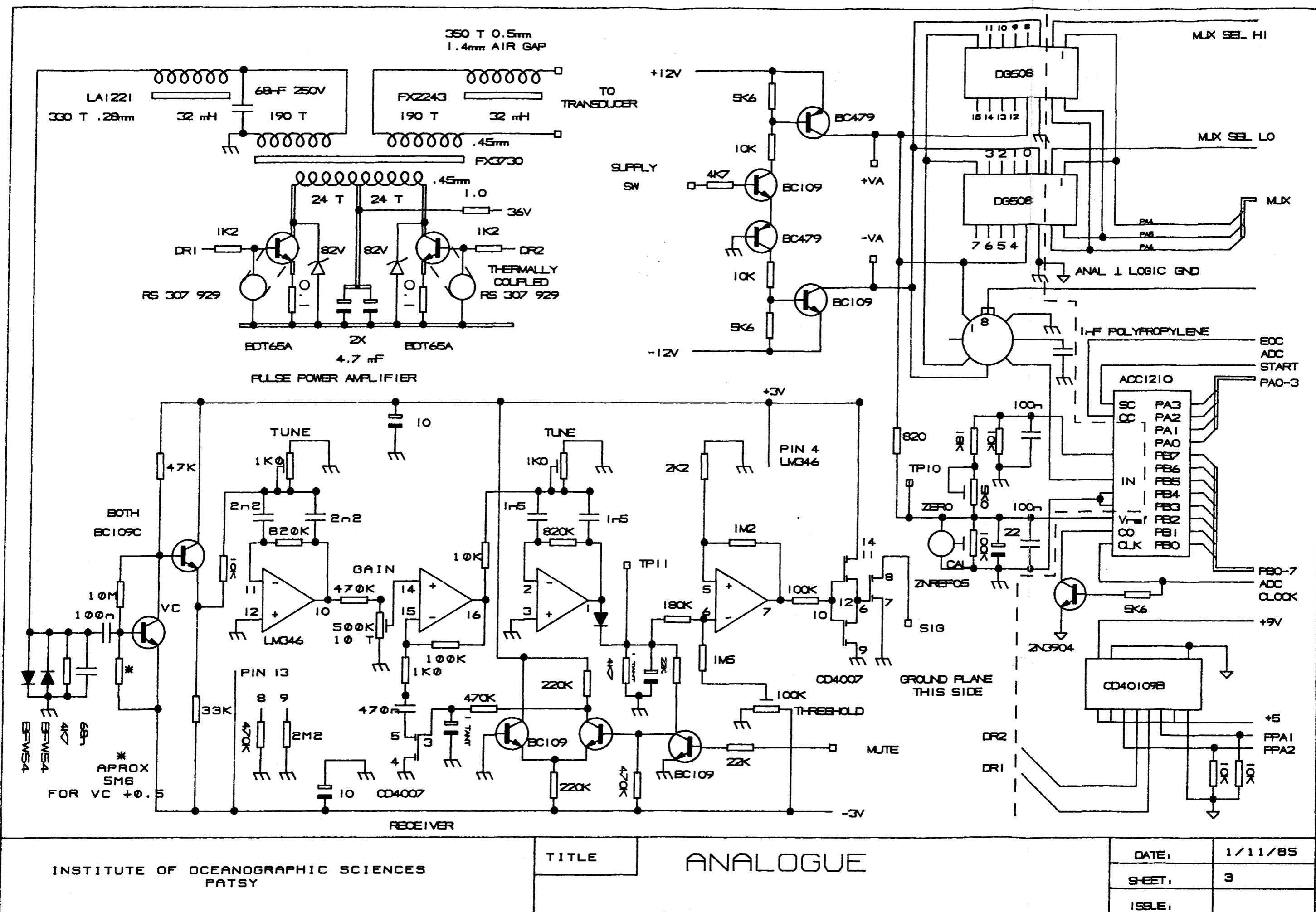
CHECK removes or substitutes any rogue values that are too large, too small (or negative) and deletes the second of any pair that differ by less than 20 msec.

RELATIVES converts the CHECKed list into a series of delays between PINGS.

APPENDIX A6 CIRCUIT DIAGRAMS







* OTHER INPUTS
TO GROUND

