A 197.1-μW Wireless Sensor SoC With an Energy-Efficient Analog Front-End and a Harmonic Injection-Locked OOK TX

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***Abstract*— This paper presents an integrated ultra-low-power (ULP) wireless sensor system-on-chip (SoC) that can be used for voltage sensing in both Internet of Things applications and bio-potential monitoring. In order to increase the energy efficiency of the analog front-end (AFE), we propose a noise and power efficient push-pull low noise instrumentation amplifier (LNIA) with a built-in ripple reduction loop based on capacitor reuse. A low-power ISM-band harmonic injection locked on-off-keying transmitter (OOK-TX) is also implemented for energy efficient wireless connectivity. Circuit implementations, design considerations, and detailed analysis are presented to improve the overall energy efficiencies of the SoC including the AFE, TX and, the power management unit. The proposed ULP-SoC is fabricated in 130 nm CMOS technology with a total area of 1.92 mm^2. The total power consumption of the proposed system-on-chip is 197.1 μW which is one of the lowest among state-of-the-art wireless sensor SoC.**

***Index Terms*— Low noise instrumentation amplifier, offset cancellation, ripple reduction loop, injection locked TX, system-on-chip.**

I. Introduction

THE Internet of Things (IoT) devices, as an effective interface between human and the physical environment, have an extensive breadth of applications, ranging from implantable devices for healthcare to infrastructure monitoring [1]–[3]. Such devices usually gather different input information from sensors and send the data out wirelessly to portable devices such as mobiles and laptops for easy access of data. The difficulty of access to external power source has put a stringent power budget constraint on all kinds of IoT systems, therefore, an ultra-low-power system-on-chip (ULP-SoC) solutions with efficient wireless connectivity is highly desirable [4].

State-of-the-art ULP wireless sensor SoCs are however limited in two aspects, the base-band analog front-end (AFE) and the wireless transmitter (TX). The AFE usually consists of a low noise instrumentation amplifier (LNIA) and an analog-to-digital converter (ADC) where mostly the LNIA dominates the base-band power consumption [5]–[7] which is hard to reduce without penalty due to the strict design trade-off between noise and current consumption. Fig. 1(a) summarizes the recent trend for the LNIA in the last decade comparing the power consumption versus input referred noise [6]–[20]. The most straight-forward method to reduce the power efficiency factor (PEF) is by reducing the supply which is also evident in [12]–[16] where a PEF of less than four has been achieved. Interestingly, it can be noticed that recent works have been able to push the PEF below 1.5 [12]–[15] where the main design concept is based on stacking three to five g_m cells leveraging current reuse. However, such aggressive stacking of g_m cells leaves significant limited headroom for each transistor which is not robust across process, voltage, and temperature (PVT) and also results in a limited dynamic range. The goal of the proposed work is to achieve a PEF that is less than 1.5 without stacking the g_m cells.

Similarly, the wireless transmitter (TX) acts as the most power hungry block in the entire SoC. Although the Bluetooth Low Energy (BLE) radios have been developed for the past few years to specifically target the IoT applications [21]–[24], the power consumption of these modules are still limited to milliwatts level which substantially reduces the device life time. Sub-GHz radios for biomedical/IoT applications have emerged to further reduce the power consumption in the last decade [25]–[39] where the performance of the reported works is summarized in Fig. 1(b). It can be observed that the energy efficiency is limited among the reported work with an active power consumption of less than 200 μW. The objective of this work is to deliver an energy efficient sub-GHz TX with less than 200 μW of active power consumption.

In this work, an integrated ULP wireless sensor SoC is proposed where the main contributions are elaborated and summarized as below:

i) System architecture of the proposed ULP wireless sensor SoC with design choices and specifications for each block.

ii) Basic concept and circuit implementation of the proposed LNIA are presented where 1) an energy efficient LNIA is proposed with a push-pull input stage, and 2) a noise efficient built-in ripple reduction loop (RRL) based on capacitor reuse is introduced (Section III).

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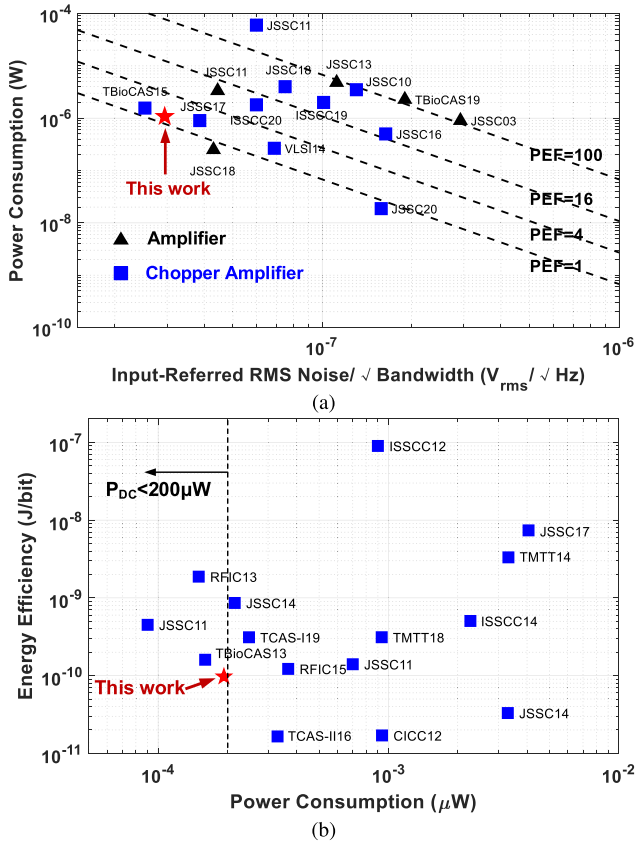

Fig. 1. Survey on (a) the power consumption vs. the input referred noise of LNIA in recent years (2003-2020), and (b) energy efficiency vs. power consumption of sub-GHz radio in recent years (2011-2020).

iii) A simple ULP on-off-keying (OOK) TX based on harmonic injection locking (IL) and frequency multiplying is implemented. Detailed design choices and circuit implementation are presented (Section IV).

iv) Circuit implementation and design considerations of the nanowatt power management unit (PMU) are discussed in where a pW voltage reference with improved line sensitivity (LS) and low process variation is proposed (Section V).

Finally, Section VI presents measurement results followed by conclusions in Section VII.

II. Proposed System Architecture

Fig. 2 illustrates the simplified system-level diagram of the proposed SoC. The AFE consists of a LNIA, a low pass filter (LPF), a buffer and a successive approximation analog-to-digital converter (SAR-ADC). The LNIA senses and amplifies the voltage signal from the sensors with a targeted bandwidth of 300 Hz. The amplified signal is then band limited by the following low pass filter (LPF) for the anti-aliasing purpose. An 8-bit SAR-ADC digitizes the amplified analog signal which is then fed into the wireless TX for data transmission. A buffer stage is inserted in between the LPF and the SAR-ADC to effectively drive the sampling capacitor. The LNIA is chopped by a 20 kHz clock to reduce the effect of the DC offset and flicker noise. The ADC oversamples the amplified signal at 2.5 kHz yielding an theoretical improvement on the signal-to-quantization noise (SQNR) by 6 dB.

An OOK harmonic injection-locked transmitter (ILTX) is implemented because of its simple structure and digital-intensive design. The ILTX operates in the industrial, scientific, and medical (ISM) band where the antenna can be realized with a smaller form factor compared to other sub-GHz frequency band. The ring oscillator (RO) is harmonically injection locked with the 20.3 MHz master clock generated by the crystal oscillator (XTAL-OSC). The edge-combining power amplifier (ECPA) combines the multi-phase outputs of the RO to boost up the carrier frequency to 913 MHz and matches to the 50 Ω impedance of the antenna at the same time. The 20.3 MHz XTAL-OSC is also divided to provide the clock for base-band circuits (eg. chopper and SAR-ADC). The PMU comprises with regulators and reference voltage/current generators to power up each block and provide stable current and voltage references required on-chip. One 0.5 V supply and three 1 V supplies generated from the 1.2 V global VDD regulate the analog and digital blocks, respectively. The I2C digital interface communicates with the outside and loads the calibration digits and initial setup into the chip.

III. Design and Modeling of the AFE

This section presents the basic concept and working principle of the propsoed LNIA and the built-in RRL followed by the circuit implementation. Detailed analysis of the behavioral model regarding the input-referred noise, offset and the parasitic effects is discussed. Finally, the design consideration for the SAR-ADC is also presented.

A. Basic Concept of the Proposed LNIA

Supply scaling has been proven to be the most effective approach to save power. Recent works on LNIA all originate from the inverter-based structure due to its compatibility with low supply operation and high noise efficiency. The squeezed-inverter based architecture proposed in [16], though energy efficient, is susceptible to PVT variations that requires additional calibration steps. More importantly, the upmodulated DC offset could potentially saturate the amplifier that reduces its range of operation. [14], [15] further improve the noise efficiency by stacking multiple inverter-based g_m cells at the sacrifice of signal swing at the output. Additionally, the RRL demonstrated in [40], though effectively removes the amplified upmodulated offset, needs a current buffer (CB) with at least one cascoded device which makes it infeasible with ultra-low supply operation. Moreover, the auxiliary g_m cell contributes to power and noise overhead. Therefore, a better solution with a more energy efficient implementation is preferred.

Fig. 3 shows the evolution of a conventional inverter-based LNIA into our proposed structure with the built-in RRL. Even though the inverter-based topology effectively doubles the transconductance [14], [15], [41], the NMOS and PMOS transistors are biased to the same common-mode level which lacks the degree of freedom to optimize the transconductance of each device individually. Thus push-pull biasing is used which biases the NMOS and the PMOS separately by de-coupling the DC bias through the capacitor, C_C, to optimize the g_m/I_d.

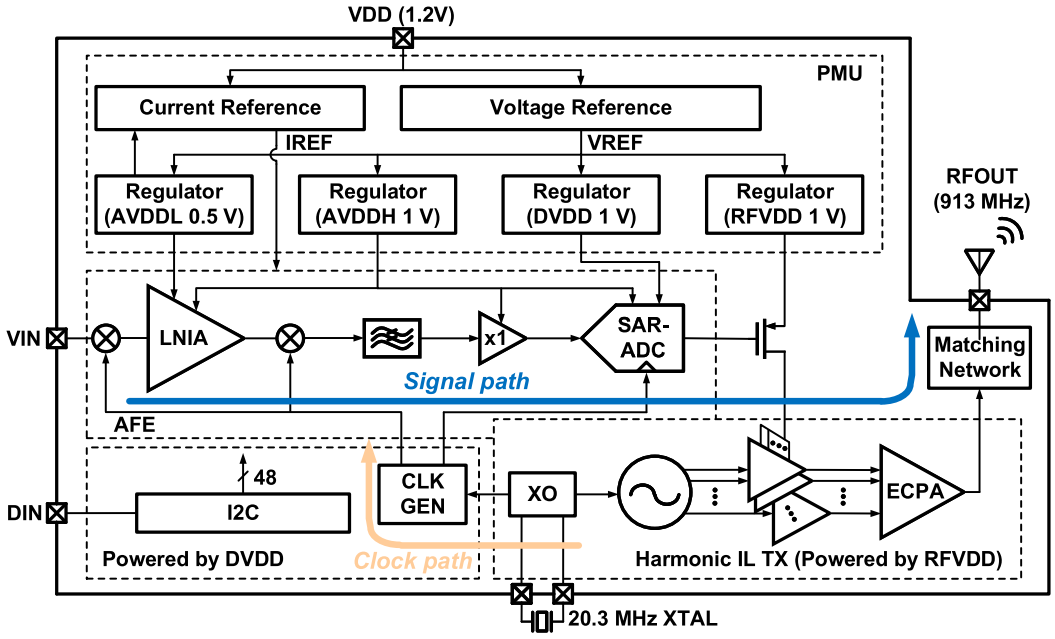

Fig. 2. System diagram of the proposed SoC.

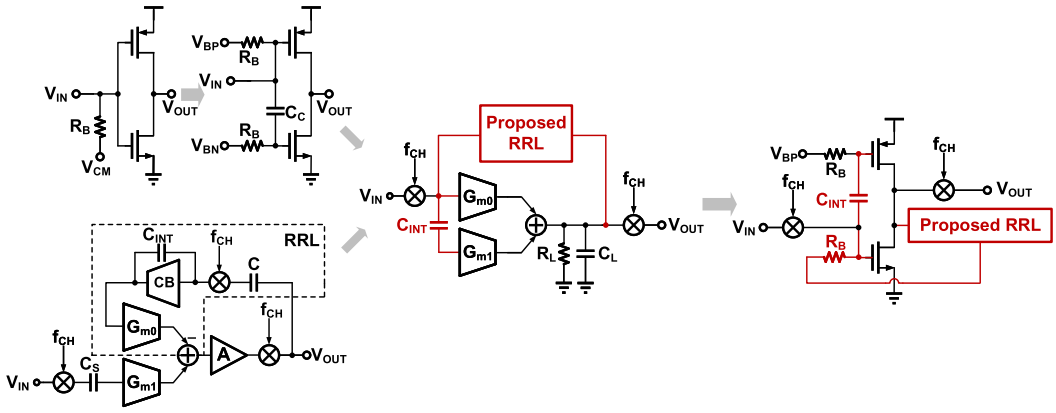

Fig. 3. Evolution process of proposed IA with built-in RRL reusing the AC coupling capacitor.

However, the push-pull biasing requires separate generation of the bias voltages which is inefficient. In addition, an RRL is also desired for DC measurement and prevents the amplified DC offset from saturating the following stages.

By combining the features of the push-pull topology with the RRL, a push-pull amplifier with a built-in RRL can be realized as shown in Fig. 3. The initial offset of the input transistors is sensed and integrated by the RRL while the error information is fed back to the NMOS transistor through a large resistor, R_{B}, to null out the initial offset. There are several additional advantages besides the maximized g_m/I_d in the proposed combination. First, the conventional RRL feeds back the integrated offset information to the input transistors through an auxiliary g_{m} cell which is not in the signal path and thus contributes only noise current to the output. Though this noise current can be minimized by designing a large transconductance ratio between the input and the feedback auxiliary g_{m} cells, the maximum offset voltage that the RRL can handle is severely limited as it is inversely proportional to this ratio. The proposed approach ensures that the RRL auxiliary g_{m} cell is in the signal path instead of the feedback path. Thus the overall signal-to-noise ratio (SNR) can be maintained large even without sacrificing the maximum offset voltage the loop can handle. Secondly, the RRL provides an inherent DC biasing for the NMOS transistor. Hence, no additional biasing voltage needs to be generated in the push-pull topology. Last but not the least, the AC coupling capacitor, C_{INT}, functions as a integrating capacitor at the same time such that no additional capacitor is required in the RRL.

B. Circuit Implementation

Fig. 4(a) illustrates the schematic of the proposed LNIA The capacitively-coupled topology is adopted where the gain is determined by the ratio of the input capacitor, C_{S}, and feedback capacitor, C_{F}. The amplifier is realized by a two-stage

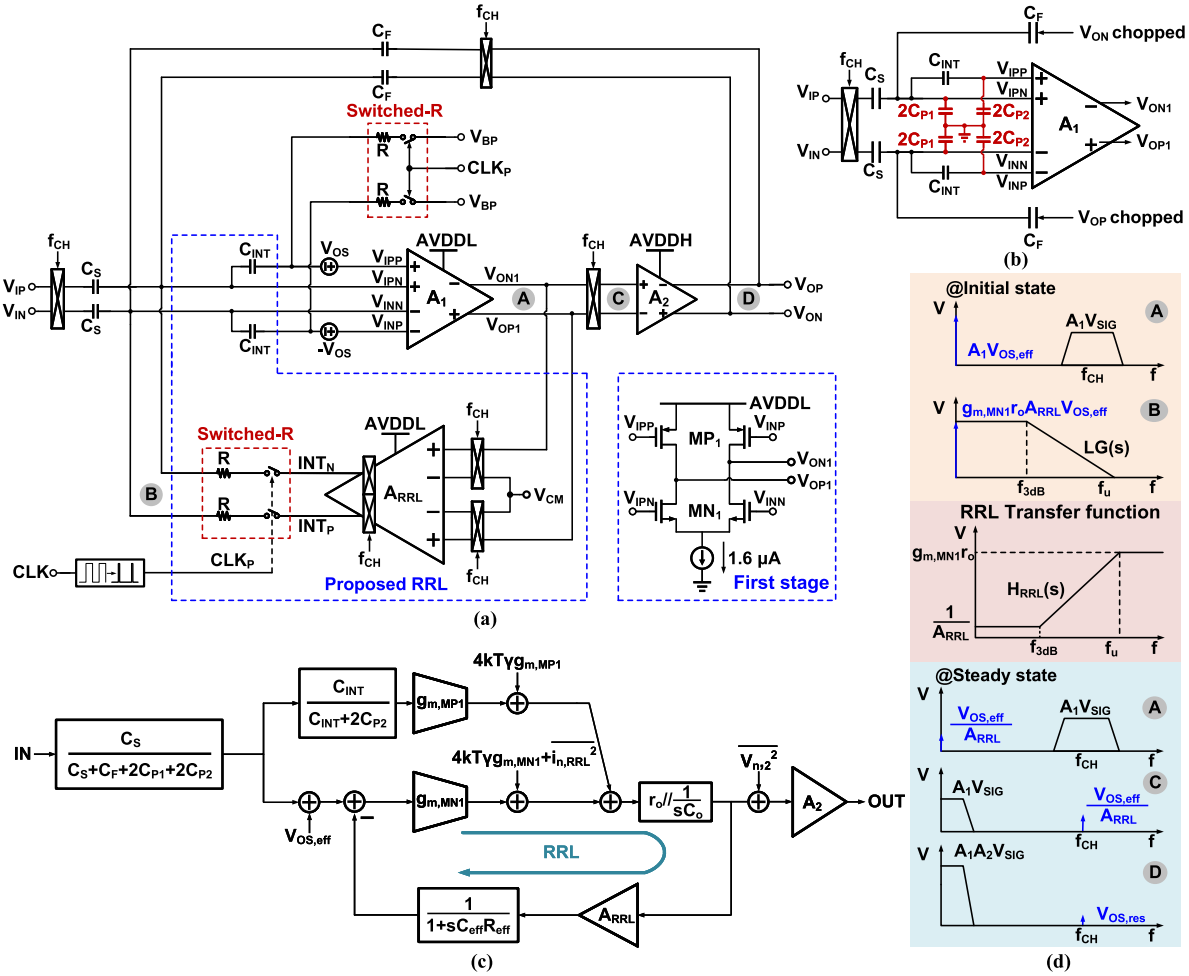

Fig. 4. (a) Simplified circuit diagram of the proposed LNIA, (b) parasitic effects at the input of the first stage, (c) block diagram with the built-in RRL, and (d) signal, offset propagation, and transfer function in frequency domain at critical nodes.

design where the first stage is the proposed push-pull topology. Initially, the signal is up-modulated to the chopping frequency, f_{CH}, whereas, the amplifier offset is at DC at the input of the first stage push-pull amplifier. Both the DC offset and signal are then amplified by the first stage amplifier, A_1, and compared with a reference voltage, V_{CM}, through a pair of additional operational transconductance amplifier (OTA). Therefore, the loop reacts to the amplified offset which is then integrated onto the C_{INT} to bias the NMOS input pair of the first stage. The other PMOS input pair is biased through the switched resistors to an on-chip voltage reference, V_{BP}. Another chopper is placed after the first-stage amplifier to down-convert the signal back to base-band and up-modulate the residue offset to f_{CH}. A folded-cascode amplifier is implemented in the second stage where its bandwidth is much smaller than the first stage, therefore, the residual offset is further attenuated by the low pass characteristic of the second stage amplifier. Note that as the dominant pole is placed at the output of the second stage amplifier, the miller compensation capacitor is not required.

The power consumption is further reduced by powering the first and second stage amplifier with separate supplies, AVDDL and AVDDH, where AVDDL is 0.5 V and AVDDH is 1 V. The schematic of the first stage amplifier is shown in Fig. 4(a). A tail current source is added only on the NMOS side to avoid large PVT-related current variation and enhances the common-mode rejction ratio (CMRR) of the first stage. A second order passive RC-LPF is placed after the LNIA where the capacitors are implemented via the dual-MIM capacitor with a density of 4 fF/μm^2 to save area. Each single capacitor is split into two identical parts with one of them flipped upside down to match the unequal parasitics on top and bottom plates.

C. LNIA Modeling and Parasitic Effects

Considering the parasitic capacitors at the input of the first stage illustrated in Fig. 4(b), the proposed LNIA can be modeled mathematically with the capacitor network at the input of the first stage amplifier as shown in Fig. 4(c). The input signal is first divided by the capacitive divider formed by C_S, C_F, and the parasitic capacitor C_{P1} between V_{IPN} and V_{INN}. In contrast to the NMOS transconductor where the signal is directly applied to its input after the capacitive divider, the signal applied to the PMOS transconductor is first divided by another capacitive divider formed by C_{INT} and the parasitic capacitor C_{P2} between V_{IPP} and V_{INP}. The current of

the two transconductors are summed at the output yielding the gain of the first stage,

$$A_1(s) = \left(g_{\mathrm{m,MN1}} + \frac{C_{\mathrm{INT}}}{C_{\mathrm{INT}} + 2C_{\mathrm{P2}}} g_{\mathrm{m,MP1}}\right) \frac{r_{\mathrm{o}}}{1 + s r_{\mathrm{o}} C_{\mathrm{o}}}$$

The effective input DC offset is modeled as a voltage signal, $V_{\mathrm{OS,eff}}$, added at the input of the first stage on the NMOS side expressed as,

$$V_{\mathrm{OS,eff}} = V_{\mathrm{OS,MN1}} + \left(1 + \frac{2C_{\mathrm{P2}}}{C_{\mathrm{INT}}}\right) V_{\mathrm{OS,MP1}}$$

which is sensed by the RRL with the error signal subtracted from the NMOS path for ripple reduction. The loop gain of the RRL shown in Fig. 3(d) can be calculated as below,

$$LG(s) = g_{\mathrm{m,MN1}} r_{\mathrm{o}} \left(\frac{1}{1 + s r_{\mathrm{o}} C_{\mathrm{o}}}\right) \cdot A_{\mathrm{RRL}} \left(\frac{1}{1 + s R_{\mathrm{eff}} C_{\mathrm{eff}}}\right)$$

where R_{eff} is the effective resistance of the switched-resistor equal to R/D (D is the duty cycle of the pulsed clock), and C_{eff} is the effective capacitance of the capacitive network at the input calculated to be,

$$C_{\mathrm{eff}} = 2C_{\mathrm{P1}} + \frac{2C_{\mathrm{P2}} C_{\mathrm{INT}}}{2C_{\mathrm{P2}} + C_{\mathrm{INT}}}$$

As R_{eff} and C_{eff} are much larger than r_{o} and C_{o}, it can be simplified to a first-order system with the 3dB corner frequency, f_{3dB}, and unity gain frequency, f_{u}, expressed as follow respectively,

$$f_{\mathrm{3dB}} = \frac{1}{2\pi R_{\mathrm{eff}} C_{\mathrm{eff}}}, \quad f_{\mathrm{u}} = \frac{g_{\mathrm{m,MN1}} r_{\mathrm{o}} A_{\mathrm{RRL}}}{2\pi R_{\mathrm{eff}} C_{\mathrm{eff}}}$$

The closed loop transfer function the input DC offset sees will be,

$$H_{\mathrm{RRL}}(s) = \frac{g_{\mathrm{m,MN1}} r_{\mathrm{o}} (1 + s R_{\mathrm{eff}} C_{\mathrm{eff}})}{1 + g_{\mathrm{m,MN1}} r_{\mathrm{o}} A_{\mathrm{RRL}} + s R_{\mathrm{eff}} C_{\mathrm{eff}}}$$

which is also illustrated in Fig. 4(d). At the steady state, the offset at the output of the first stage is attenuated by approximately A_{RRL}. This residue offset is further filtered by the second stage after getting chopped to f_{CH} since the bandwidth of the second stage is much lower.

D. LNIA Noise Analysis

The main noise contributors of the LNIA include the NMOS/PMOS transconductors, the second stage amplifier and the RRL.Therefore, the input referred noise power spectral density (PSD) can be obtained as follows:

$$\frac{\overline{v_{\mathrm{ni,total}}^2}}{\Delta f} = \left(\frac{C_{\mathrm{S}} + C_{\mathrm{F}} + 2C_{\mathrm{P1}} + 2C_{\mathrm{P2}}}{C_{\mathrm{S}}}\right)^2 \cdot \left(\overline{v_{\mathrm{ni,MN1}}^2} + \overline{v_{\mathrm{ni,MP1}}^2} + \overline{v_{\mathrm{ni,2}}^2} + \overline{v_{\mathrm{ni,RRL}}^2}\right)$$

where $\overline{v_{\mathrm{ni,MN1}}^2}$, $\overline{v_{\mathrm{ni,MP1}}^2}$, $\overline{v_{\mathrm{ni,2}}^2}$, and $\overline{v_{\mathrm{ni,RRL}}^2}$ denote the noise PSD of M_{N1}, M_{P1}, second stage amplifier, and the RRL that are referred back to the input of the first stage amplifier, respectively, which can be calculated as follows:

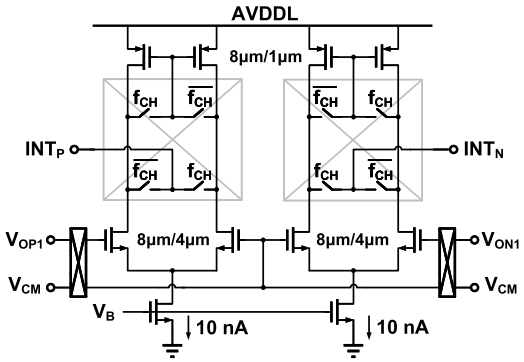

Fig. 5. Transistor-level schematic of the amplifiers in the RRL.

$$\overline{v_{\mathrm{ni,MN1}}^2} = \frac{4kT\gamma\, g_{\mathrm{m,MN1}}}{\left(G_{\mathrm{m,MP1}} + G_{\mathrm{m,MN1}}\right)^2}$$

$$\overline{v_{\mathrm{ni,MP1}}^2} = \frac{4kT\gamma\, g_{\mathrm{m,MP1}}}{\left(G_{\mathrm{m,MP1}} + G_{\mathrm{m,MN1}}\right)^2}$$

$$\overline{v_{\mathrm{ni,2}}^2} = \frac{\overline{v_{\mathrm{n2}}^2}}{\left(G_{\mathrm{m,MP1}} + G_{\mathrm{m,MN1}}\right)^2 R_{\mathrm{L}}^2}$$

$$\overline{v_{\mathrm{ni,RRL}}^2} = \frac{\overline{i_{\mathrm{n,RRL}}^2}}{\left(G_{\mathrm{m,MP1}} + G_{\mathrm{m,MN1}}\right)^2}$$

where

$$G_{\mathrm{m,MN1}} = g_{\mathrm{m,MN1}},\ G_{\mathrm{m,MP1}} = \frac{C_{\mathrm{INT}}}{C_{\mathrm{INT}} + 2C_{\mathrm{P2}}} g_{\mathrm{m,MP1}}$$

It can be noted that the noise contribution of the second stage is negligible after referring back to the input, yielding the total input-referred noise PSD as follow,

$$\frac{\overline{v_{\mathrm{n,total}}^2}}{\Delta f} = \left(\frac{C_{\mathrm{S}} + C_{\mathrm{F}} + 2C_{\mathrm{P1}} + 2C_{\mathrm{P2}}}{C_{\mathrm{S}}}\right)^2 \cdot \frac{4kT\gamma\, g_{\mathrm{m,MN1}} + 4kT\gamma\, g_{\mathrm{m,MP1}} + \overline{i_{\mathrm{n,RRL}}^2}}{\left(\frac{C_{\mathrm{INT}}}{C_{\mathrm{INT}} + 2C_{\mathrm{P2}}} g_{\mathrm{m,MP1}} + g_{\mathrm{m,MN1}}\right)^2}$$

The first stage amplifier dominates the total noise contribution. Though the effective g_{m} of the NMOS transistor is slightly degraded by the capacitor network at the input, this degradation can be negligible as C_{INT} is much larger than C_{P2} while the RRL function is still preserved. The noise of the RRL can also be kept to a minimum when referring back to the input, thus its power consumption can be reduced. Fig. 5 shows the chopper amplifiers in the RRL with the size of the transistors.

Fig. 6 shows the output transient simulated waveform of the proposed LNIA when a 1 mV input-referred offset is considered to demonstrate the effectiveness of the RRL. The initial 1 mV offset is amplified to more than 1.6 V_{pp} at the start of the simulation as it directly sees the open loop gain of the two-stage amplifier. The RRL is turned ON at 5 ms and starts to react to the initial offset. The ripple reduction is complete after around 60 ms leaving a 4 mV_{pp} differential

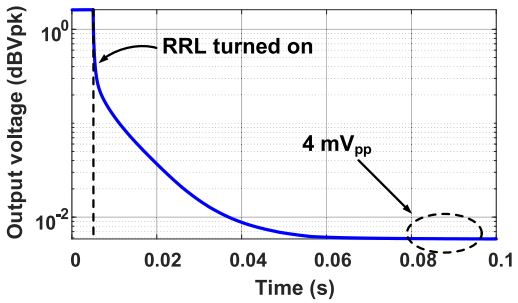

Fig. 6. Simulated proposed LNIA output with 1mV added offset when the RRL is enabled.

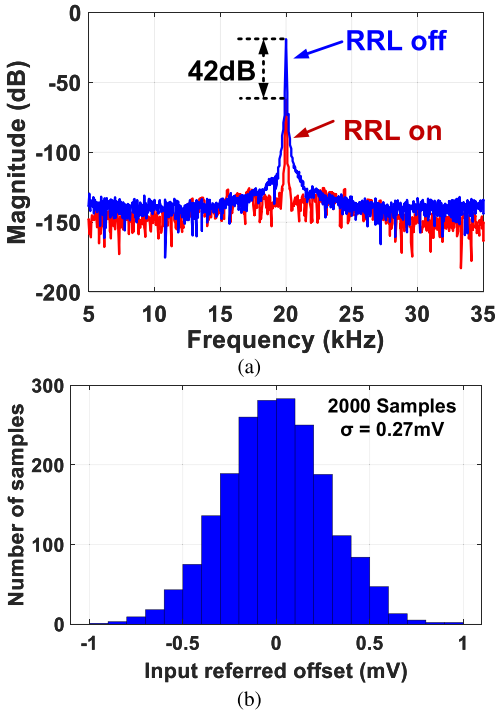

Fig. 7. (a) Upmodulated residue offset at LNIA output with RRL ON/OFF, and (b) Monte-Carlo simulation results for RRL OTA.

residue offset at the output which further implies that the input-referred offset is 40 μV.

The residue upmodulated offset is compared between the two cases with the RRL switched ON/OFF as shown in Fig. 7(a). The 20 kHz chopping frequency creates a spur in the output spectrum representing the residue offset. Simulation results shows the effectiveness of the proposed approach that reduces the residue offset by 42 dB with the RRL ON. Careful design considerations in both schematic and layout, such as choice of large transistor sizes and common-centroid layout, are followed to ensure that the impact of the offset voltages due to the RRL itself can be mitigated. Fig. 7(b) illustrates the results of Monte-Carlo simulations on the input-referred offset of the OTA in the RRL. A 1-σ value of 0.27 mV across 2000 samples is achieved in this design to sufficiently minimize the impact of the RRL offset.

Similar to the capacitively-coupled topology, the input impedance of the proposed LNIA is determined by the amount of current charging and discharging C_S during the chopping

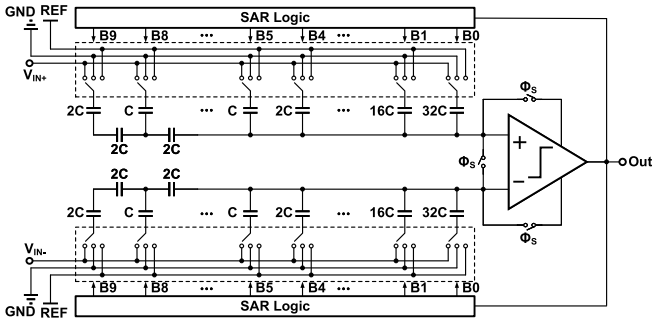

Fig. 8. Simplified schematic of the SAR-ADC.

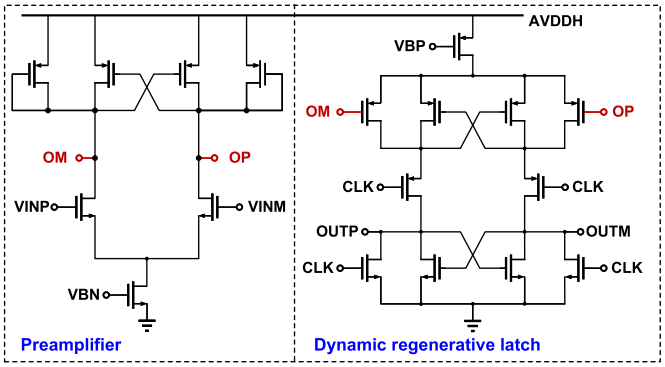

Fig. 9. Transistor-level schematic of the comparator.

period, estimated to be $1/2f_{CH}C_S$. Since the input to the first stage is considered to be virtual ground, the effective capacitance at this node including C_{INT} only weakly affects the input impedance of the proposed LNIA, which is still limited by the chopping frequency and the input capacitor, simulated to be 1.52 MΩ. The previously reported input impedance boosting techniques such as positive feedback [17] or auxiliary path [10] can be easily integrated into this design to further boost the input impedance to hundreds of MΩ or a few GΩ.

E. SAR-ADC

The SAR-ADC chosen in this work is based on the design in [42]. A hybrid digital-to-analog converter (DAC) with half binary and half C-2C is implemented as shown in Fig. 8 to accommodate both the area and mismatch where the equivalent sampling capacitor is only $41C$. A larger C is chosen to minimize the mismatch effect with a value of 70 fF whose 1-σ mismatch is 0.39% yielding a total sampling capacitor of 2.87 pF.

The transistor-level schematic of the comparator is shown in Fig. 9. A preamplifier is employed to isolate the kickback noise from the following dynamic latch. A NMOS input pair is selected in the preamplifier as it provides a higher g_m/I_d while its offset and flicker noise can be reduced by the offset-cancellation circuit. The PMOS cross-coupled load boosts the gain with the diode connected PMOS transistors setting the output common-mode level at half of supply. The gain of the preamplifier is 25 dB with a total power consumption of 20 nW. A sub-threshold dynamic regenerative latch is implemented with thick gate-oxide devices to reduce

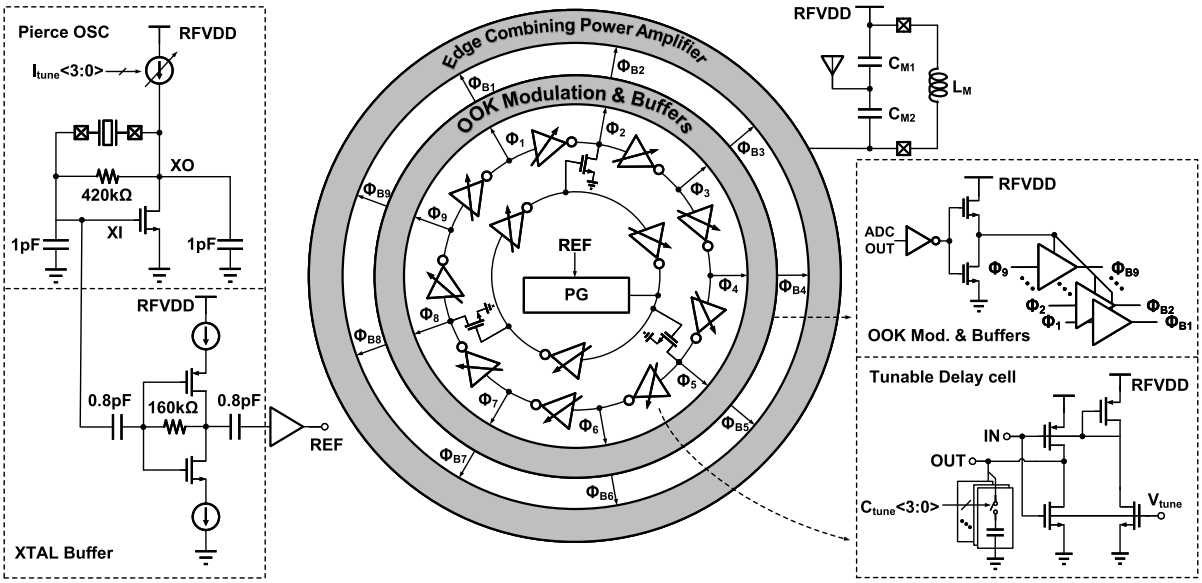

Fig. 10. Simplified schematic of the proposed harmonic ILTX.

its leakage power. Stacked design is employed to further cut down the leakage to pA level.

Table I summarizes the simulated noise breakdown of the SAR-ADC where the quantization noise dominates the overall noise occupying a 96.4% of the total noise. The second and third noise contributors are the comparator noise (2.4%) and kT/C noise (1.2%) resulting in an overall SNR of 55.7 dB.

IV. Design of the Harmonic ILTX

Energy efficient wireless transmission plays a crucial role in wireless SoC as the power consumption of the TX occupies a significant portion of the overall budget. A power oscillator based TX is proposed in [43], where the local LC oscillator, the PA and the antenna are combined into one single unit. However the loop antenna tends to be sensitive to frequency pulling due to the objects moving in proximity with the antenna. The OOK TX in [44] consisting of a RO-based local oscillator driving an inverter-based PA, though simple, runs at the carrier frequency, where the RO adds more power overhead. The architecture in [25] combines the IL RO and the frequency-multiplying PA, namely the ECPA, where the RO is able to run at a lower frequency with reduced power consumption. In this work, the harmonic IL scheme is implemented to further save the RO power. The delay cells in the RO are calibrated to suppress the reference spur induced by the harmonic IL. The proposed harmonic ILTX employs OOK modulation to allow the TX staying in idle mode while transmitting a "0" to conserve power.

Fig. 10 shows the proposed harmonic ILTX. The pierce oscillator (OSC) drives the XTAL and generates a 20.3 MHz reference. The biasing current of the pierce OSC is programmable such that it can be reduced after the XTAL starts up. The XTAL buffer comprises of a self-biased inverter stage and the AC-coupling capacitors, which converts the sine wave into square wave.

TABLE I
Noise Breakdown of the ADC

	Simulated results	Percentage
Quantization noise (V^2)	1.14e-7	96.4%
kT/C noise (V^2)	1.44e-9	1.2%
Comparator noise (V^2)	2.85e-9	2.4%
Total noise (V^2)	1.19e-7	100%
SNR (dB)	55.7	

The ROs are injection locked to the harmonic frequency of the reference through a pulse generator (PG) where the cascade injection [25] is adopted to isolate the phase mismatch of individual inverters in the first RO. The 5th harmonic is selected in this design to balance the trade-off between the RO power consumption and the frequency difference between the carrier and the reference spur. A 9$\times$ frequency multiplication is realized by interpolating the nine-phase output of the second RO via the ECPA. The delay cells of the ROs are implemented with both coarse and fine tunability to overcome the PVT sensitive carrier-to-spur ratio (CSR). A small voltage-to-frequency gain is preferred in this design to weaken any interference and noise impact on the RO free-running frequency from the tuning nodes. Therefore, bulk tuning is chosen which is realized by changing the bulk voltage of both NMOS and PMOS devices through a diode connected transistor to avoid imbalance in rise and fall times. The simulated gain is 48 MHz/V within a 0.2 V voltage range. Moreover, it also has the advantages of providing rail-to-rail swing and low supply compatibility. The simulated ± 1-σ variation of the RO is 28 MHz, therefore, an additional 4-bit binary-encoded coarse tuning is implemented to ensure that the RO frequency

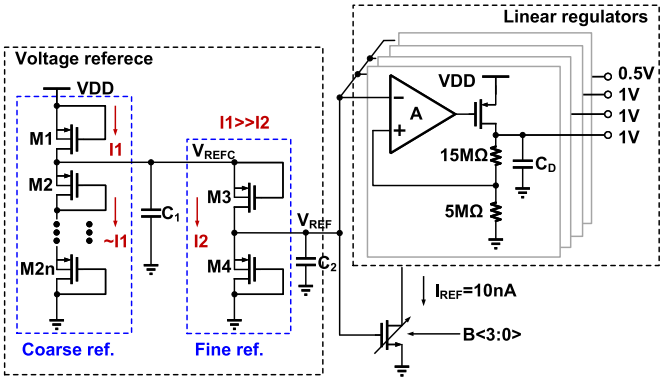

Fig. 11. PMU with the all-PMOS voltage reference.

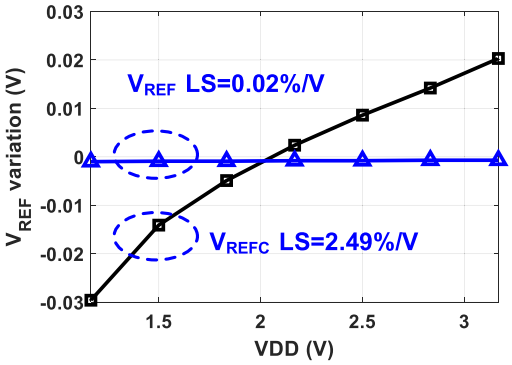

Fig. 12. Simulation results on the voltage variation of coarse and fine output across VDD.

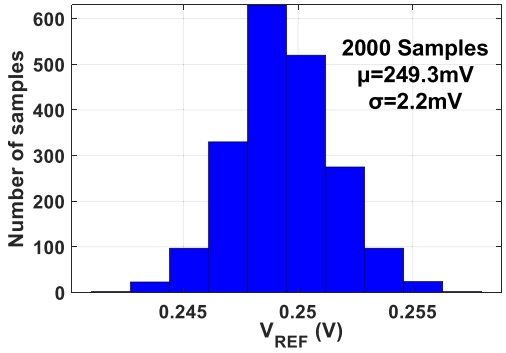

Fig. 13. Simulated V_{REF} variation.

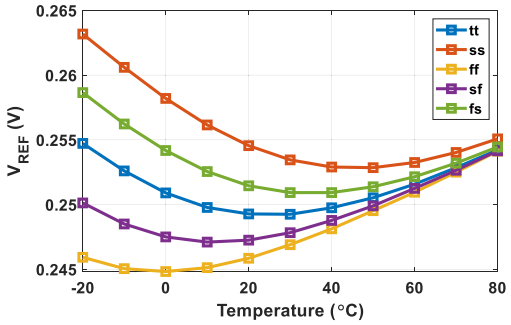

Fig. 14. Simulated temperature variation of the voltage regulator under five process corners.

is able to cover the entire variation range. A buffer chain is inserted before the ECPA to reduce the short-circuit current by strengthening the RO output signal and perform the OOK modulation simultaneously. The tapped-C matching network is chosen where the inductor, L_M, is placed off-chip to conserve area. The ratio of the two capacitor is designed to be C_{M1}:C_{M2} = 8:1 boosting the 50 Ω load by approximately 65×. Lumped element models of the bond-pads, bond-wires and PCB routings are included in the simulation setup to precisely capture the parasitic effects.

V. Design of the PMU

The PMU comprises of three sub-blocks, the voltage and current reference generator, and the regulators which will be discussed in the following.

A. Voltage Reference

The 2-transistor family originated in [45] has been a promising architecture and a number of its variants have been developed. In this work, a pW-voltage reference is proposed using all-PMOS implementation consisting of coarse and fine reference with improved LS as shown in Fig. 11. With the gate and source of M1 tied together to VDD, its leakage current, I_1, can stay independent from any VDD variation to the first order. Therefore, the line regulation can be improved at the coarse reference output, V_{REFC}, as it is mainly a function of I_1. An identical part as the fine reference consisting of M3 and M4 is placed at the output of the coarse reference circuit to generate the fine regulated output, V_{REF}, to further improve the line sensitivity. The current flow through the fine reference circuit, I_2, is designed to be much smaller than I_1 to minimize the loading effect. The output of the voltage reference is designed to be 0.25 V. Only PMOS transistors are used in this implementation to maintain a low process variation and achieve a lower flicker noise. Two 2 pF dual-MIM capacitors, C_1 and C_2, are added at the output of both coarse and fine reference circuits to bypass the high frequency noise. Fig. 12 depicts the simulated LS of the V_{REFC} and V_{REF} respectively. The LS after the fine reference is able to improve more than 100× over a wide range of VDD variation. The monte-carlo simulation results on the variation of V_{REF} are also shown in Fig. 13. The untrimmed simulated σ/μ is less than 1%. The simulated temperature variation of the voltage reference over five process corners is shown in Fig. 14. The worst-case temperature coefficient happens at ff corner which is approximately 371.6 ppm/°C from −20 to 80 °C whereas the best-cast happens at tt corner which is approximately 218 ppm/°C. The simulated power consumption under room temperature and typical corner is 166.8 pW.

B. Regulators and Current Reference

Four linear regulators with one 0.5 V output and three 1 V outputs are implemented to power the analog, digital and RF blocks in the SoC respectively. The low-dropout (LDO) topology is chosen leaving a 0.2 V headroom for the PMOS power transistor. The voltage regulator consists

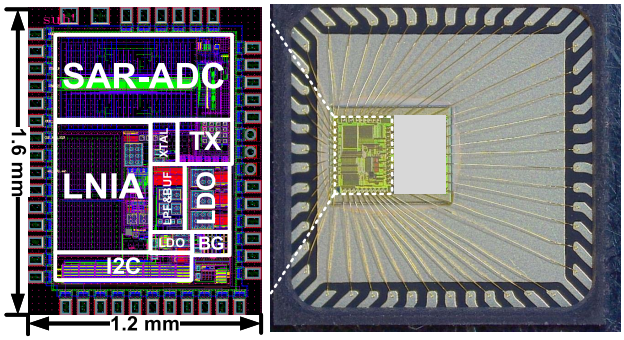

Fig. 15. Chip layout and die micrograph in a QFN package.

of the OTA driving the PMOS power transistor with the output voltage fed back to the OTA through the resistive divider. Folded cascode amplifier with PMOS input pair is selected due to the below-VDD common-mode level. The OTA current consumption and the current through the resistive divider dominates the regulator quiescent current consumption. To minimize this quiescent current, the OTA is designed to operate in sub-threshold and consumes less than 15 nA (including biasing current). Large resistors in the resistive dividers (Fig. 11) further limits current. Lastly, to maintain the stability of the loop, the dominant pole is placed at the output of the OTA to ensure the loop dynamic is not affected under different load conditions. A 10 pF dual-MIM capacitor, C_D, as the bypass capacitor is added at the regulator output to filter out the high frequency components on the power line. Local decoupling capacitors realized by MOS capacitors are also included inside each block. The simulated quiescent current of the four regulators are 280 nA which consists of the current from the amplifiers and the current through the resistors. It is worth to mention that the regulators implemented in this work are only for the purpose of demonstrating a complete SoC. The maximum efficiency of the regulators is limited to less than 85% due to the large dropout voltage through the power transistor. Digital regulators [46] or switching regulators [47] can be promising alternatives to substantially improve the efficiency. A 10 nA current reference is simply generated by connecting the V_{REF} (0.25 V) voltage reference output to the gate of a NMOS transistor. The line sensitivity of the current reference can be maintained within 1%/V as the voltage is well regulated by the voltage reference. An 4-bit binary-encoded calibration is included to correct the V_{th} variation across process.

VI. Measurement Results

This section presents the measurement results of the prototype SoC. Fabricated in 130 nm CMOS technology, the proposed SoC consumes a total area of 1.92 mm^2 including pads and an active area of 1.17 mm^2. The prototype is encapsulated in a cost-efficient 48-pin QFN package with both the layout and the die micrograph shown in Fig. 15. The active area is mainly dominated by the LNIA and the SAR-ADC which are 0.32 mm^2 and 0.54 mm^2 respectively where most of the area is consumed by the MIM capacitors.Benefiting from the digital-intensive architecture, the TX only occupies an area

TABLE II
Power and Area Breakdown of the SoC

	Power (μW)	Active area (mm^2)
LNIA	1.08	0.32
SAR-ADC	0.22	0.54
TX	193.7	0.08
PMU	1.2	0.12
Others	0.91	0.11
Total	197.1	1.17

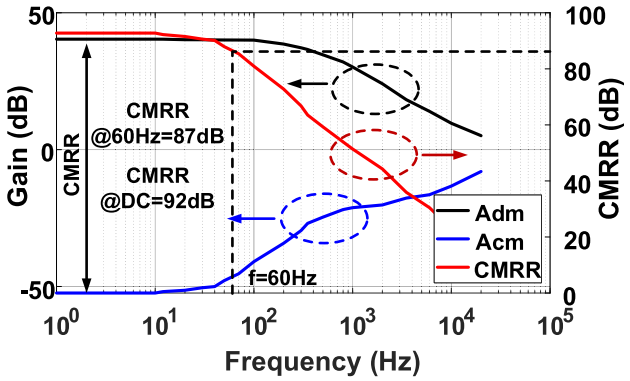

Fig. 16. Measured LNIA gain and CMRR.

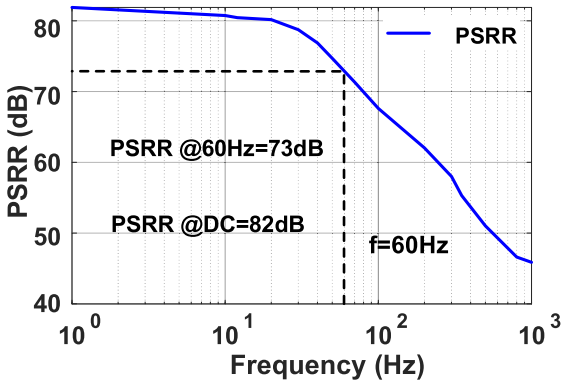

Fig. 17. Measured LNIA PSRR.

of 0.08 mm^2 including the XTAL-OSC (Pierce OSC and XTAL buffer). The PMU consumes a total area of 0.12 mm^2 where the 0.5 V LDO, the 1 V LDO and the voltage reference occupies an area of 0.013 mm^2, 0.025 mm^2 and 0.015 mm^2, respectively. The rest of the area is consumed by the current reference and the current mirrors for distributing the bias current for each block. Table II summaries the power and area breakdown of the proposed SoC.

Fig. 16 shows the measured frequency response of the proposed LNIA with the targeted closed-loop differential gain of 40 dB and a 3 dB bandwidth of 300 Hz. The common-mode gain is also measured across the frequency shown in Fig. 16. A -52 dB of DC common-mode gain is observed resulting in a 92 dB CMRR at DC. The CMRR is mainly determined by the mismatch of the capacitors, C_S, C_F and C_{INT}, whose values are 10 pF, 0.1 pF and 5 pF. This mismatch can be further mitigated by the input chopper. Because of the ultra-low current of the second stage amplifier and its large

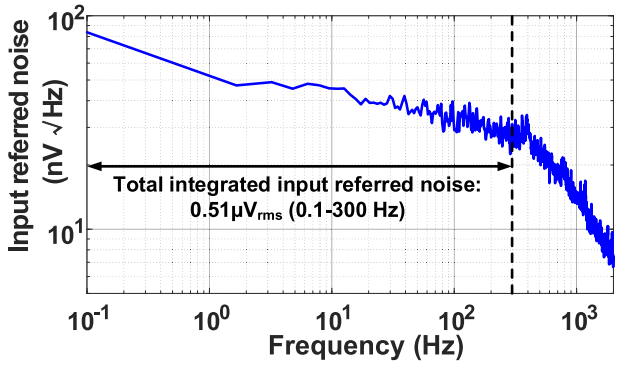

Fig. 18. Measured LNIA input-referred noise.

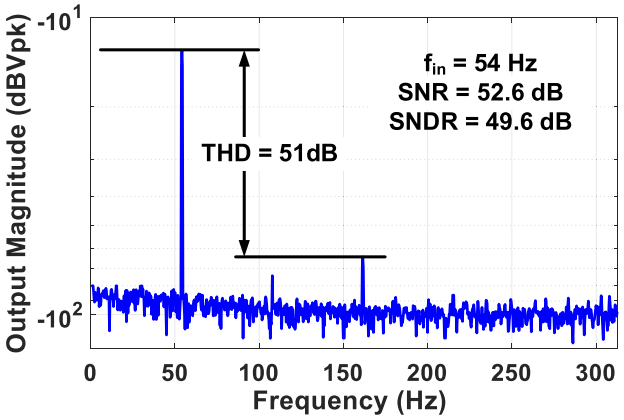

Fig. 19. Measured ADC output spectrum.

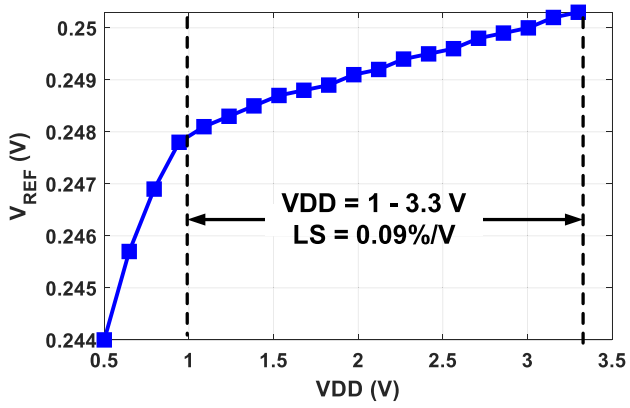

Fig. 20. Measured LS of the voltage reference.

input devices, the CMRR starts to degrade due to the increase of the common-mode gain in second stage amplifier. However, a CMRR of 87 dB can be still maintained at 60 Hz. The power supply rejection ratio (PSRR) of the LNIA is also measured by switching to the external supply through the I2C to isolate the assistance of on-chip regulators. Fig. 17 demonstrates the measured PSRR when the same signal is injected at both the supplies. It is observed that the PSRR at DC and 60Hz are 82 dB and 73 dB respectively. It is worth mentioning that any supply variation in the first stage amplifier will be converted to common-mode input for the second stage.

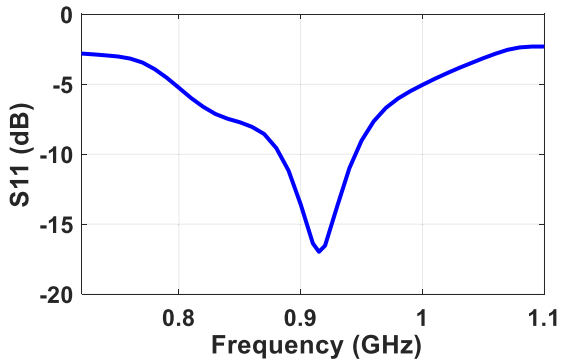

Fig. 21. Measured S11.

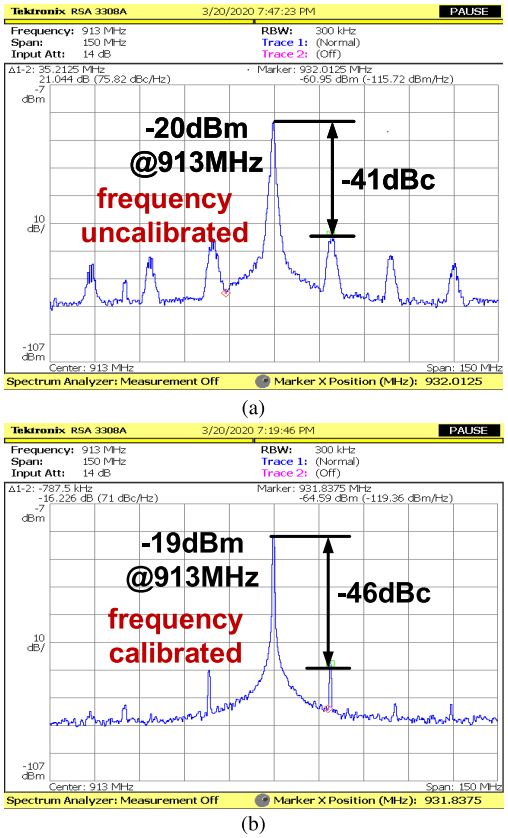

Fig. 22. Measured TX output spectrum (a) without and (b) with frequency calibration.

Therefore, the PSRR of the entire LNIA is mainly dominated by the CMRR and PSRR of the second stage amplifier.

The input-referred noise is measured by shorting the two differential input together. Its noise PSD after referring back to the input is shown in Fig. 18. With the help of the chopper, the input-referred noise within the band of the interest is mostly dominated by the thermal noise. The total integrated noise is calculated by integrating the noise from 0.1 to 300 Hz which is 0.51 μV_{rms} yielding an equivalent noise PSD of 29.4 nV/$\sqrt{Hz}$. Results show that the $1/f$ noise corner is below 1 Hz. The total power consumption of the LNIA is 1.08 μW leading to a noise-efficiency factor (NEF) and PEF of 1.62 and 1.39, respectively. The first-stage amplifier consuming 854 nW dominates the overall power consumption.

TABLE III

PERFORMANCE SUMMARY AND COMPARISON OF THE PROPOSED SoC WITH STATE-OF-THE-ART

		This work	TBioCAS'19 [19]	JSSC'14 [44]	JSSC'13 [11]	JSSC'20 [14]*	JSSC'18 [15]**	JSSC'18 [17]	JSSC'17 [16]
		SoC				AFE			
Tech. (nm)		130	130	350	130	180	180	40	180
VDD (V)		1.2	0.9	1.8	1.35	0.95	0.9	1.2	0.2/0.8
Area (mm^2)		1.17	6.25	11.25	8.25	0.18	0.01	0.113	1
Wireless trans.		Yes	Yes	Yes	Yes	No	No	No	No
TX duty cycle (%)		100	0.38	100	0.013	-	-	-	-
Power (μW)		197.1 (OOK)	74 (BFSK) 322 (QPSK)	942.9	397	0.0132	0.23	7.3	0.79
Blocks		1-ch. LNIA, ADC, TX, PMU	3-ch. LNIA, ADC,TX, DSP, PMU	4-ch. LNIA, ADC, TX, DSP, EH	4-ch. LNIA, ADC, TX, DSP, EH	1-ch. LNIA,	1-ch. LNIA	1-ch. LNIA, ADC	1-ch. LNIA, PGA
AFE	**g_m stacking**	No	No	No	No	Yes	Yes	No	No
	Number of stacks	-	-	-	-	3	2	-	-
	Gain (dB)	40	39-57	0-40	40-78	36	25.4	26	57.8
	BW (Hz)	300	0.5-150	400	320	240	10K	1-200/5K	670
	IRN (μV_{rms})	0.51	2.32	15.3	2	3.01	6.7	2/7	0.94
	CMRR/PSRR (dB)	92/82	60/-	-	>70/-	>95/>68	82/81	-	85/80
	NEF/PEF	1.62/1.39	2.79/-	-	7.69	1.08/1.12	1.26/1.53	7/4.9	2.1/1.6
	Power/Ch. (μW)	1.08	2.28	2.57	4.8	0.0132	0.23	2.4	0.79
ADC	**Topology**	SAR	SAR	SAR	SAR	-	-	$\Delta\Sigma$	-
	Resolution	7.95	12	9.4	8	-	-	15	-
	f_s (kHz)	1.25	0.256	100	>0.64	-	-	400	-
TX	**Frequency (MHz)**	913	401	403	402/433	-	-	-	-
	P_{out} (dBm)	-19	-15	-18	-18.5	-	-	-	-
	Data rate (Mb/s)	2 (OOK)	0.55 (BFSK) 11 (QPSK)	-	0.2 (BFSK)	-	-	-	-
	Power (μW)	193.7	3020 (BFSK) 3530 (QPSK)	762 (OOK)	160	-	-	-	-
	Energy eff. (nJ/bit)	0.097	5.49 (BFSK) 0.32 (QPSK)		0.8	-	-	-	-

NEF=$V_{rms}\sqrt{\frac{2 \cdot I_{total}}{\pi \cdot 4kT \cdot BW}}$ $\quad$ PEF $= P_{total} \cdot \frac{2 \cdot V_{rms}^2}{\pi \cdot 4kT \cdot V_T \cdot BW}$ $\quad$ Energy efficiency $= \frac{\text{Power}}{\text{Data rate}}$

EH - Energy Harvester PGA - Programmable Gain Amplifier

* - Data of three-stacked version is used ** - Data of two-stacked version is used

The second-stage, RRL, and the rest of the circuits including biasing and chopper consume 140 nW, 79.8 nW, and 10 nW, respectively.

The AFE is tested by applying a 54Hz single tone with a full-scale peak-to-peak input at the LNIA input. The digitized output of the SAR-ADC is captured by the TLA 714 logic analyzer. Fig. 19 demonstrates the measured 2048-point FFT results. The measured total harmonic distortion (THD) is 51dB which captures the distortion of the entire signal chain from the LNIA to the SAR-ADC. The THD is mainly limited by the linearity of the second stage amplifier and the DAC element mismatch in the SAR-ADC. The measured SNR and signal-to-noise and distortion ratio (SNDR) of the AFE is 52.6 dB and 49.6 dB which corresponds to a system effective number of bits (ENOB) of 7.95 bits. The reduced SNR is mainly caused by the ground coupling between different blocks.

The LS of the voltage reference is measured by sweeping the VDD from 0.5 V to 3.3 V. It can be noticed that the voltage reference is able to function in between the VDD range of 1-3.3 V as shown in Fig. 20. Yet the LS drops to 0.09%/V which is around 0.07%/V higher than the simulation results. The main reason for this is because of the diode leakage of the electrostatic discharge (ESD). An ultra-low leakage interface with a high impedance termination is highly recommended for measuring the circuit.

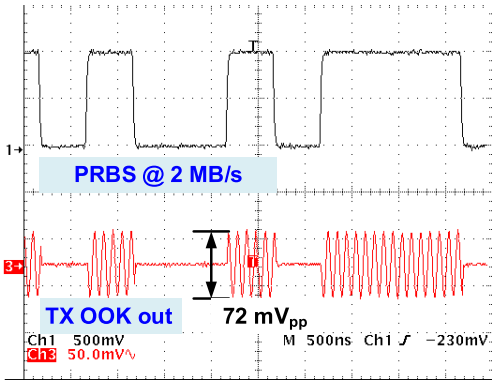

Fig. 23. Measured OOK transient output of the TX with 2 Mb/s PRBS bit stream.

The TX is measured by disabling the AFE with only the PMU connected. The output matching of the TX is first measured with its S11 shown in Fig. 21. The RF output is captured by the spectrum analyzer with the input data from the ADC set to "1". Fig. 22(a) shows the measured output spectrum of the proposed OOK TX. The RF output has a power of -20 dBm at 913 MHz. Notice that the reference spurs due to the harmonic IL are high yielding a CSR of 41 dB. The fundamental tone is also noisy which is because the free-running frequency of the ROs are too high or

low that is about to exceed the lock range of the IL. After the RO frequency is corrected, a 5 dB CSR improvement is observed and the fundamental tone is much cleaner with the output power increases to −19 dBm as shown in Fig. 22(b). The active power consumption of the TX is 251.2 μW where the XTAL OSC and the PG, the ROs including the tuning circuits, the buffer, and the ECPA consume 4.5 μW, 84.6 μW, 62.5 μW, and 104.6 μW, respectively. With the OOK modulation, the average power consumption of the TX is able to reduce to 193.7 μW. The OOK modulation is measured by applying a 2 Mb/s pseudo random bit sequence (PRBS) to the transmitter where Fig. 23 depicts the output transient waveform on the TX OOK output. The overall active power consumption of the wireless SoC is 254.6 μW with an average power consumption of 197.1 μW under the OOK modulation.

Table III summarizes and compares the performance of the proposed ULP wireless SoC with state-of-the-art. Our work consumes the lowest active power (at 100% duty cycle) with a higher carrier frequency while achieving the lowest energy efficiency. Although the TX output power is slightly lower compared to other works, it is still reliable to support far-field communication. When comparing separately against state-of-the-art AFE works, it demonstrates the lowest noise efficiency factor (NEF) and PEF among the works without stacking g_m cells. It is also worth to mention that this work even achieves a better PEF than [15] where two g_m cells are stacked to save power.

VII. Conclusion

This work demonstrates a fully integrated ULP wireless SoC prototype. The proposed push-pull LNIA with built-in RRL achieves both low offset and input referred noise while consuming only 1.08 μW with a comparable NEF and PEF to state-of-the-art. The harmonic ILTX architecture with mostly digital intensive design and the frequency calibration scheme achieve an improved energy efficiency and spur suppression. The ULP-SoC prototype consumes only 197.1 μW of power under OOK modulation and 1.17mm^2 of active area which is one of the lowest compared against state-of-the-art.

Acknowledgment

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